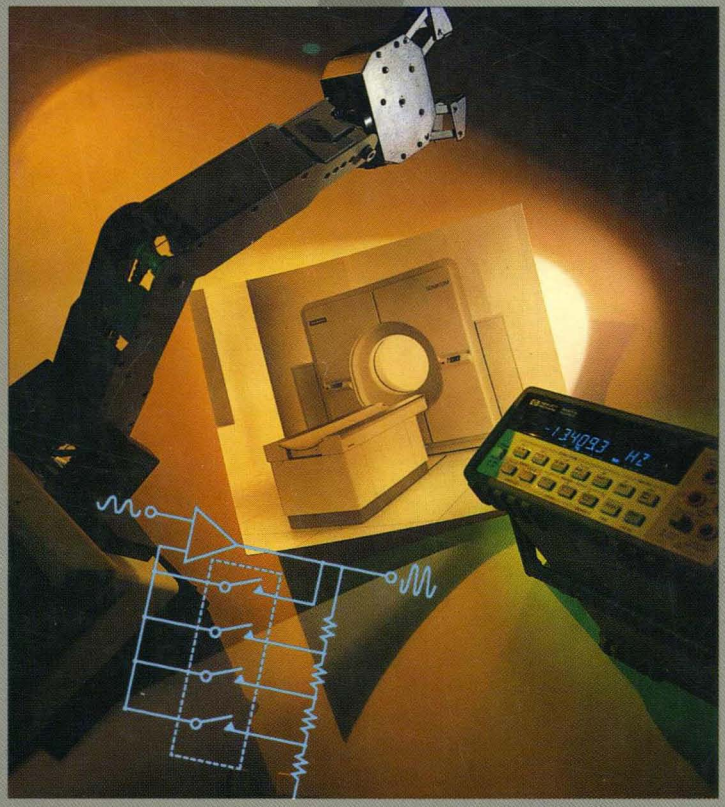
Analog Integrated Circuits

1994



Siliconix

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Analog Integrated Circuits
1994

Analog Integrated Circuits Data Book

1994

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Warning Regarding Life Support Applications

Siliconix products are not sold for applications in any medical equipment intended for use as a component of any life support system unless a specific written agreement pertaining to such intended use is executed between the manufacturer and Siliconix. Such agreement will require the equipment manufacturer either to contract for additional reliability testing of the Siliconix parts and/or to commit to undertake such testing as a part of its manufacturing process. In addition, such manufacturer must agree to indemnify and hold Siliconix harmless from any claims arising out of the use of the Siliconix parts in life support equipment.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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About Siliconix

Siliconix is a leading manufacturer of semiconductor products for the computer, communications, automotive, industrial, and hi-rel markets. The company's products bridge the interface gap between real-world analog signals and the digitally operated microprocessor, providing both discrete and integrated solutions to

- sense, convert, and control signals at a system's input
- regulate and manage the system's power supplies
- provide useful signals and power at the output.

As a member of TEMIC, the microelectronics enterprise of Daimler-Benz, Siliconix has expanded its worldwide presence and is further equipped to serve its customers on an international scale by sharing the technologies and applications expertise of its sister companies and by taking advantage of a combined international sales network.

In keeping with this global perspective, the company has aggressively pursued world-class standards of cycle time, yields, and average outgoing quality in its manufacturing facilities in the United States and Asia. Siliconix' continuous improvement efforts have resulted in dramatic improvements for each of these areas and in numerous quality awards from its customers. The company has pursued international quality certifications as well, and received ISO 9001 certification for its Santa Clara facilities in November 1993. Our booklet "Making Continuous Improvement A Way of Business" tells more about our commitment to quality. You can request a copy by calling (800) 554–5565.

The Company's manufacturing operations include wafer fabrication, assembly, and product testing. All wafer fabrication is done in Santa Clara, where the facilities include a four-inch wafer fab and a Class 1, six-inch wafer fab. High-volume assembly and product testing for plastic- and ceramic-packaged products are handled in the Company's facilities in Taiwan, the Philippines, and China.

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About This Data Book

The products detailed in this data book include analog switches and multiplexers, wideband video switches, multiplexers, crosspoints, buffers, amplifiers, and voltage converters. These products are designed for applications in the industrial, instrumentation, computer peripherals, communications, automotive, and military markets. Siliconix serves these markets with products of unequaled performance, quality and reliability through the use of its leading design, processing, packaging, and testing technologies.

The product specifications listed in this data book are arranged in a simplified format. The electrical tables and performance curves contain detailed information, simplifying the tasks of design and component engineers. Each of the data sheets is controlled by the Siliconix Quality Assurance organization, which guarantees all stated limits.

For More Information

To request additional literature please call 1-800-554-5565. Literature and samples can also be requested from our sales representatives. See the sales office listings in Section 6.

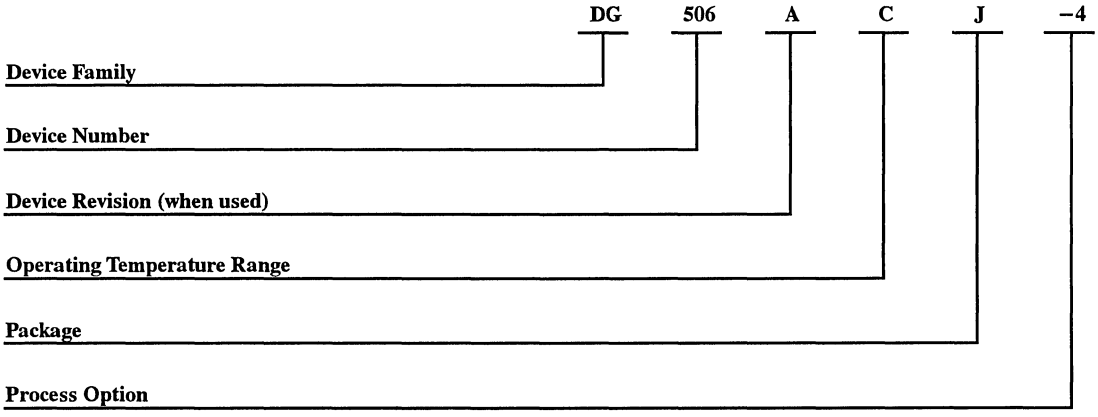
Customer service representatives are available during normal West Coast business hours to provide information on orders placed with the factory.

For Technical Support

In addition to the individual data sheets, which provide Application Hints, Siliconix offers a number of Applications Notes and Technical Articles to help you with your designs. Please refer to the Application Note listing in Section 5, and use our FaxBack system 408-970-5600 to obtain copies.

Ordering Information

Integrated Circuits Nomenclature



Device Family
(1 or 2 Letters)

DG — Analog Switches and Analog Multiplexers
Si — Siliconix Integrated Circuits

Device Number

(3- or 4-Digit Numbers)

Operating Temperature Range

(1 Letter)

A — −55 to 125°C
B — −25 to 85°C
C — 0 to 70°C
D — −40 to 85°C
E — −40 to 105°C

Package
(1 Letter)

A — Metal Can
J — Dual-In-Line Package — Plastic DIP
K — Dual-In-Line Package — Ceramic DIP
L — Flat Package
M — CerQuad J-Leaded Chip Carrier
N — Plastic J-Leaded Chip Carrier — PLCC
P — Dual-In-Line Package — Sidebraze
R — Dual-In-Line Package — Sidebraze
W — Wide-Body Small-Outline Package (SOIC)
Y — Narrow-Body Small-Outline Package (SOIC)
Z — Leadless Chip Carrier — LCC

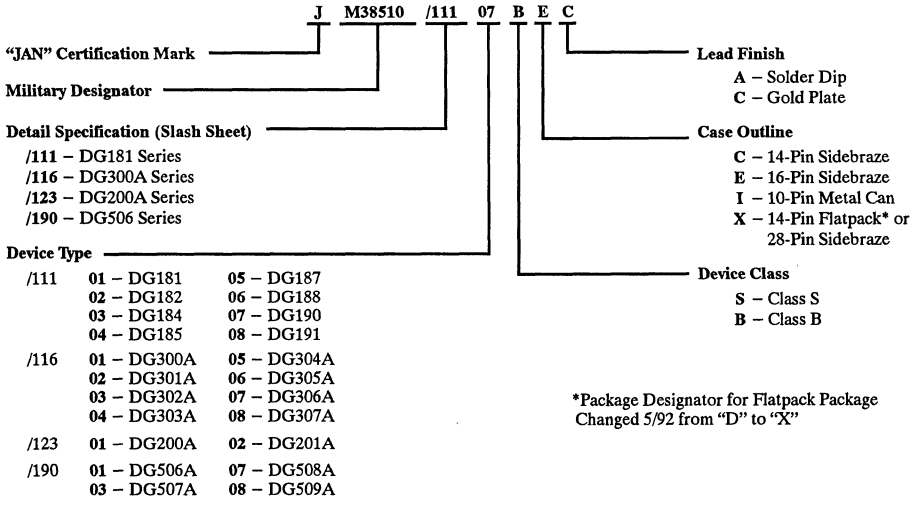
Process Option

/883— Processing to the current revision of MIL-STD-883, Level B. Compliant Non-JAN
−4 — Ruggedized Plastic Flow

All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages or sales office for complete information.

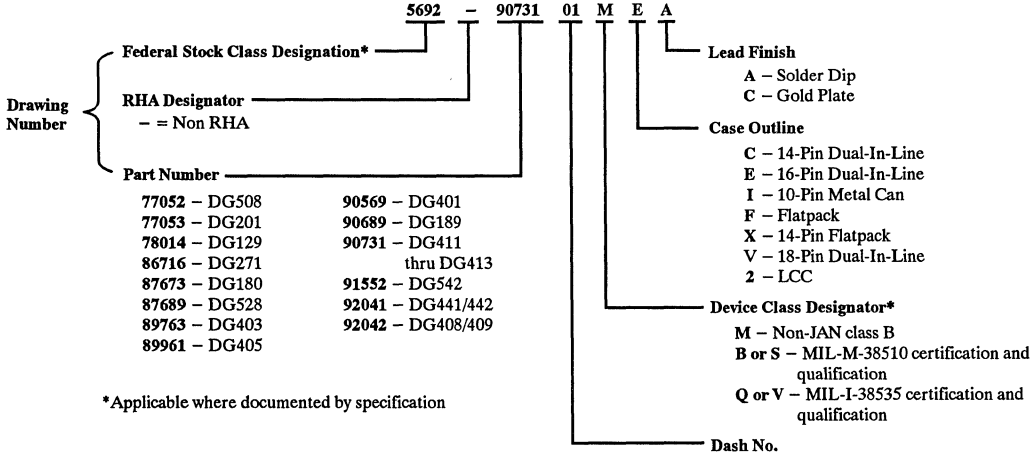
Military Nomenclature

MIL-M-38510



*Package Designator for Flatpack Package Changed 5/92 from "D" to "X"

Standard Military Drawing



*Applicable where documented by specification

About Analog Switches

Siliconix is the world's leading supplier of high-performance, precision solid-state analog switches. For more than twenty years, we've combined new technologies with our experience and expertise to produce new families of leading-edge products.

Our DG4XX and DG6XX families of analog switches and multiplexers are one way Siliconix maintains its high reputation for innovation. These new devices can be used to upgrade existing products or to open new doors to high-performance analog switching. The DG4XX family includes all the most popular functions—SPST, SPDT, and DPST—in single and dual switch configurations, along with several SPST quads. Packaging options include both plastic and ceramic DIP, mini DIP, PLCC, and plastic SOIC packages for surface-mount assembly. These are available in both industrial (−40 to 86°C) and military (−55 to 125°C) temperature ranges. The growing DG6XX series goes even further, giving you the fastest switching times and lowest on-resistance available. The DG641/DG642, for example, are the industry's first analog switches with on-resistance below 10 Ω, while the DG611/612/613 achieve switching speeds of 15 ns.

The DG2XX, DG3XX, and DG5XX families provide adequate performance for many applications. Siliconix also offers its popular JFET (DG18X) family of switches. Single-supply operation, charge injection optimization, and a wide range of packaging options, including small outline and PLCC, are additional benefits.

CMOS

Since CMOS analog switches are parallel combinations of p- and n-channel MOSFETs, the effective on-resistance is a combination of the PMOS and NMOS resistance curves (Figure 2). This gives a fairly constant on-resistance over the entire analog voltage range. New CMOS switches also have the advantage of very low quiescent supply current because, other than for channel leakage, no current flows in the driver except when a control input transition occurs.

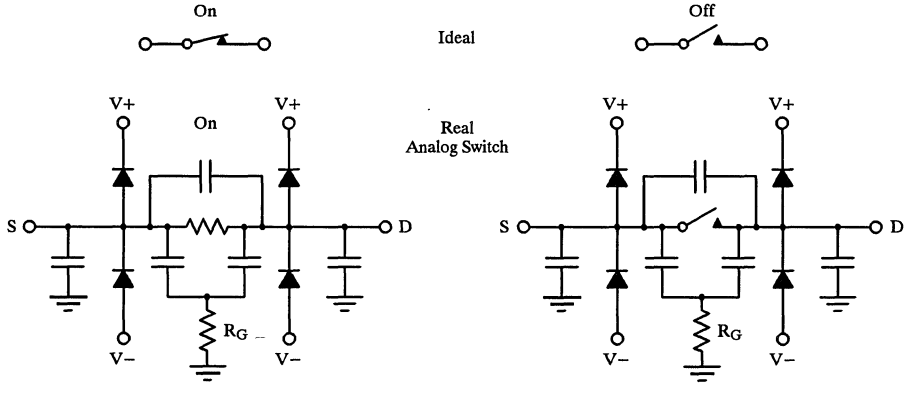


Figure 1. Comparison of the "Ideal" Switch to a Solid-State Analog Switch

Metal-Gate and Silicon-Gate CMOS

Both metal- and silicon-gate technologies are incorporated into our CMOS processes, but each is used with separate product lines. The mature metal-gate process is used for our DG2XX, DG3XX, and DG5XX families. Our newer silicon-gate process (DG4XX family) is recommended for applications needing state-of-the-art performance and versatility.

Figure 3 gives a comparison of on-resistance curves for a JFET (DG180), a D/CMOS (DG642), a metal-gate CMOS (DG201A), and a silicon-gate CMOS (DG400) analog switch.

D/CMOS "T" Switches

Siliconix manufactures analog switches and multiplexers for wideband/video applications using double-diffused MOS (DMOS) technology. DMOS FETs are n-channel enhancement-mode MOSFETs which exhibit very low capacitance and on-resistance compared to conventional CMOS devices. The result is wide bandwidth switches which feature crosstalk and off-isolation performance as high as 100 dB at 5 MHz and 3 dB bandwidths in excess of 500 MHz. These devices are ideal for broadcast video, digital data routing, high-end workstation networks and imaging applications from medical to military. The DG54x family of wideband/video "T" switches includes the DG540, DG541 and DG542 devices. The DG61X family of high-speed non-T switches boast 15-ns switching times. The DG64X family offers very low on-resistance.

Important Switch Parameters

Each switch family in the Siliconix product line has a set of optimized characteristics that make it suitable for certain types of applications. Several major specifications should be compared and prioritized before selecting an analog switch for a particular circuit.

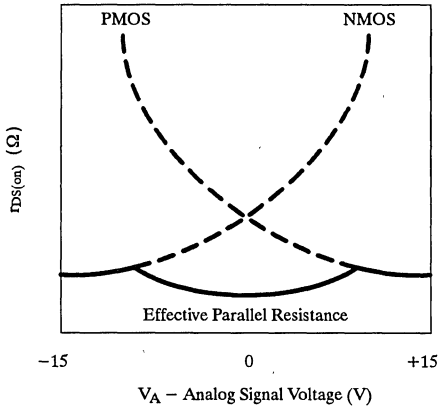


Figure 2. Graph of CMOS Switch Resistance vs. Analog Signal

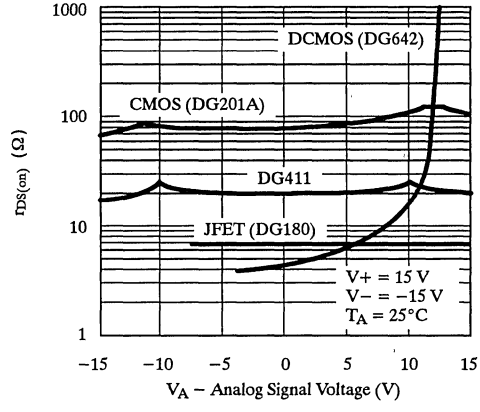


Figure 3. On-Resistance for Several Analog Switch Technologies

On-Resistance ($r_{DS(on)}$)

This specification is the dc resistance of the channel when the analog switch is in the on state. The on-resistance of an analog switch depends upon the device type and the analog signal magnitude. Although the resistance may vary across the entire analog signal range, the worst case is normally specified on the data sheet.

Switching Speed

Switching speed is the elapsed time from the application of the control signal on the input pin to the appearance (or disappearance) of the analog signal at the output. Switching speed can be affected by the load on the analog switch. Each data sheet shows a switching time test circuit with a standard load for comparison purposes.

Switch Current

The amount of current that can be fed through the switch channel is sometimes important. For example, the DG411 can handle up to 100 mA of pulsed current or 30 mA of continuous current, while the DG180 can handle up to 200 mA of continuous current.

Break-Before-Make vs. Make-Before-Break

For most analog switch applications, break-before-make switching is desired. Because it is often necessary to disconnect one signal source before connecting another to avoid source crosstalk. However, make-before-break switching is critical in some control circuits, such as the feedback resistor gain selector for programmable gain op amps, to avoid opening the loop.

Electrostatic Discharge Sensitivity (ESDS)

Electrostatic discharge is the transfer of charge that occurs when an object makes contact with a device at a different potential. The standard MIL-883C, method 3015, classifies three levels of voltage protection that a device must withstand on all pins. Class 1 devices are protected to 1999 V, Class 2 from 2000 to 3999 V, and Class 3 protection is greater than 4000 V. Beginning with DG411 series, most of our new devices have Class 2 ratings and are marked accordingly.

Charge Injection

Charge injection is the transfer of charge to a load from the driver to the FET channels during switching. In a sample-and-hold circuit, charge injection is critical as the charge added or subtracted from the holding capacitor is seen as an offset error. The lower the charge injection the better. The DG4XX family, especially the DG441 and DG411 series, are designed for balanced (linear and crossing near zero) charge injection. The DG601 and DG611 use internal compensation to minimize the charge injection seen by applications sensitive to this parameter.

Power Supplies and Power Consumption

A bipolar supply means positive and negative voltages are used, while single supply means the negative supply is grounded. Most analog designs use bipolar supplies, but a growing number of designers are turning to single-supply operation to save board space and cost. Most of our devices work well with bipolar supplies, but not all function properly in the single supply mode. The DG4XX family for analog switches and multiplexers not only functions superbly in a single-supply mode, but it is fully characterized and specified with V+ at 12 V and V- at GND. The less the power consumed by a device within a system the better. Some members of the DG4XX family draw under 1 μA of supply current compared to the milliamperes required by previous products.

Interfacing

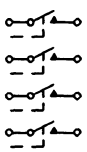
The two most common logic families are TTL and CMOS. The standard logic levels for both families are displayed in Table 1. Not all analog switches are compatible with both types of logic. Refer to the functional diagram section for each data sheet to determine the required logic levels.

Microprocessor compatibility is a growing concern when designing with analog switches. Standard analog switches require a constant control signal present on the input to hold the switch in the desired position (on or off). This could tie up a microprocessor control system unless external latches are added to control the switch. The DG42X series has incorporated these latches, complete with control logic, on board to minimize parts count and ease interface to microprocessor-based control systems.

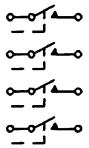
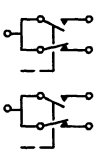
Table 1. Logic Levels for TTL and CMOS Compatibility

Logic	TTL	CMOS
0	≤ 0.8 V	≤ 1.5 V
1	≥ 2.4 V	≥ (V_{CC} – 1.5 V)

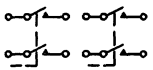
Analog Switch Selector Guide

Functional Configuration	Part Number	Max $r_{DS(on)}$ (Ω)	Max $I_{S(off)}$ (nA)	Max t_{ON} (ns)	Typ Q_{inj} (pC)	Max Supply Range (V)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
1-Channel SPST 	DG417	35	0.25	175	60	44	–	0.035	J, K, Y	8-Pin Package	1-146
	DG418	35	0.25	175	60	44	–	0.035	J, K, Y	8-Pin Package	1-146
2-Channel SPST 	DG180	10	10	400	N/A	36	–	120	A, P, X	JFET	1-4
	DG181	30	1	150	N/A	36	–	120	A, P, X	JFET	1-4
	DG401	35	0.25	150	80	44	–	0.035	J, K, Z	–	1-127
	DG421	35	0.25	250	80	44		0.035	J, K	Latches	1-155
	DG300A	50	1	300	8	44	–	7.65	A, J, K, P	–	1-90
	DG304A	50	1	250	30	44	–	0.3	A, J, K, P	–	1-99
	DG381A	50	1	300	10	44	–	7.65	J	–	1-119
	DG200A	70	2	1000	−10	44	Yes	60	A, J, K	–	1-32
	DG182	75	1	250	N/A	36	–	120	A, P, X	JFET	1-4
4-Channel SPST 	DG641	15	10	70	−19	21	Yes	108	J, Y	Video	1-208
	DG411	35	0.25	175	5	44	–	0.035	J, K, Y, Z	–	1-137
	DG412	35	0.25	175	5	44	–	0.035	J, K, Y, Z	–	1-137
	DG413	35	0.25	175	5	44	–	0.035	J, K, Y, Z	–	1-137
	DG601	35	4	45	13	22	Yes	180	J, K, Y, Z	High Speed	1-189
	DG271	50	1	65	9	44	Yes	225	J, K, Y, Z	High Speed	1-85
	DG201HS	50	1	50	5	44	Yes	240	J, K, Y, Z	High Speed	1-52
	DG540	60	10	70	−25	21	Yes	108	J, N, P	Video	1-179
	DG541	60	10	70	−25	21	Yes	108	J, P, Y	Video	1-179
	DG611	60	0.25	35	1	21	–	0.018	J, K, Y, Z	Glitchless, High Speed	1-200
	DG612	60	0.25	35	1	21	–	0.018	J, K, Y, Z	Glitchless, High Speed	1-200
	DG613	60	0.25	35	1	21	–	0.018	J, K, Y, Z	Glitchless, High Speed	1-163
	DG201B	85	0.5	300	1	44	Yes	0.765	J, K, Y	–	1-44
	DG202B	85	0.5	300	1	44	Yes	0.765	J, K, Y	–	1-44
	DG211B	85	0.5	300	1	44	–	0.35	J, Y	General Purpose	1-68
	DG212B	85	0.5	300	1	44	–	0.35	J, Y	General Purpose	1-68
	DG308B	85	0.5	200	1	44	–	0.03	J, K, Y	General Purpose	1-200
	DG309B	85	0.5	200	1	44	–	0.03	J, K, Y	General Purpose	1-200
	DG441	85	0.5	250	1	44	Yes	1.5	J, K, Y	–	1-163
	DG442	85	0.5	250	1	44	Yes	1.5	J, K, Y	–	1-163
	DG444	85	0.5	250	1	44	–	0.035	J, Y	–	1-171
	DG445	85	0.5	250	1	44	–	0.035	J, Y	–	1-171

Analog Switch Selector Guide (Cont'd)

Functional Configuration	Part Number	Max $r_{DS(on)}$ (Ω)	Max $I_{S(off)}$ (nA)	Max t_{ON} (ns)	Typ Q_{inj} (pC)	Max Supply Range (V)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
4-Channel SPST 	DG221	90	1	550	20	44	Yes	37.5	J, K, Y	Latches	1-75
	DG308A	100	1	200	−10	44	–	0.3	J, K, Y	–	1-107
	DG309	100	1	200	−10	44	–	0.3	J, Y	–	1-107
	DG201A	175	1	600	20	44	Yes	60	J, K, Y, Z	–	1-37
	DG202	175	1	600	20	44	Yes	60	J, K	–	1-37
	DG211	175	5	1000	3	44	–	20.4	J, Y	–	1-60
	DG212	175	5	1000	3	44	–	20.4	J, Y	–	1-60
1-Channel SPDT 	DG642	8	10	100	−40	21	Yes	108	J, Y	Video	1-208
	DG186	10	10	400	N/A	38	–	73	A, P	JFET	1-18
	DG301A	50	1	300	8	44	–	0.3	A, J, K, Z	–	1-90
	DG187	30	1	150	N/A	38	–	73	A, P, X	JFET	1-18
	DG419	35	0.25	175	60	44	–	0.035	J, K, Y	8-Pin Package	1-146
	DG305A	50	1	250	30	44	–	0.3	A, K, P	–	1-99
	DG387A	50	1	300	10	44	–	7.65	A, J, K	–	1-119
	DG188	75	1	250	N/A	38	–	73	A, P, X	JFET	1-18
2-Channel SPDT 	DG189	10	10	400	N/A	36	–	120	P	JFET	1-25
	DG643	15	10	70	−19	21	–	108	J, Y	Video	1-208
	DG190	30	1	150	N/A	36	–	120	P, X	JFET	1-25
	DG403	35	0.25	150	60	44	–	0.035	J, K, Y, Z	–	1-127
	DG423	35	0.25	250	60	44	–	0.035	J, K, N	Latches	1-155
	DG243	50	1	500	60	44	–	0.45	J, N	Latches	1-81
	DG303A	50	1	300	8	44	–	7.65	J, K, P, Z	–	1-90
	DG307A	50	1	250	30	44	–	0.3	J, K, P, Z	–	1-99
	DG390A	50	1	300	10	44	–	7.65	J, K	–	1-119
	DG5043	50	1	1200	30	44	–	9	J	–	1-218
	DG5143	50	0.5	200	60	44	–	0.035	J, K	–	1-221
	DG542	60	10	100	−25	21	Yes	108	J, P, Y	Video	1-179
	DG191	75	1	250	N/A	36	–	120	P, X	JFET	1-25

Analog Switch Selector Guide (Cont'd)

Functional Configuration	Part Number	Max $r_{DS(on)}$ (Ω)	Max $I_{S(off)}$ (nA)	Max t_{ON} (ns)	Typ Q_{Inj} (pC)	Max Supply Range (V)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
2-Channel DPST 	DG183	10	10	400	N/A	36	–	120	P	JFET	1-11
	DG184	30	1	150	N/A	36	–	120	P, X	JFET	1-11
	DG405	35	0.25	150	60	44	–	0.035	J, K, Y, Z	–	1-127
	DG425	35	0.25	250	60	44	–	0.035	J	Latches	1-155
	DG302A	50	1	300	8	44	–	7.65	J, K, P	–	1-90
	DG306A	50	1	250	30	44	–	0.3	J, K, P	–	1-99
	DG384A	50	1	300	10	44	–	7.65	J, K	–	1-119
	DG185	75	1	250	N/A	36	–	120	P, X	JFET	1-11

A = Metal Case
P = Sidebraze
J = Plastic DIP
X = Flatpack
K = CerDIP
Y = SOIC
N = PLCC
Z = LCC

Analog Switch—Switching Speed vs. $r_{DS(on)}$

$r_{DS(on)}$ (Max Ω)	t_{ON} (Max) or t_{OFF} (Max), Whichever is Greater							
	20/35 ns	60/75 ns	125/150 ns	200 ns	250 ns	300 ns	500/600 ns	1 µs
175							DG201A DG202	DG211 DG212
100			DG441 DG444 DG442 DG445	DG308A DG485 DG309A DG894			DG221	
85				DG308B DG309B	DG182 DG188 DG185 DG191	DG201B DG211B DG202B DG212B		DG200A
60	DG611 DG613 DG612	DG540 DG542 DG541						
50		DG271 DG201HS		DG5143	DG304A DG306A DG305A DG307A	DG300A DG381A DG301A DG384A DG302A DG387A DG303A DG390A		DG243 DG5043
35 to 25		DG601	DG181 DG405 DG419 DG184 DG411 DG421 DG187 DG412 DG423 DG190 DG413 DG425 DG401 DG417 DG181 DG403 DG418					
15		DG641 DG643						
10		DG642				DG180 DG180 DG183 DG183 DG186 DG186 DG189 DG189		

Analog Switch—Power Consumption vs. $r_{DS(on)}$

$r_{DS(on)}$ (Max Ω)	Maximum Power Consunption					
	0.018 mW	0.035 mW	0.1 to 1.5 mW	5 to 40 mW	60 to 140 mW	180 to 240 mW
175				DG211 DG212	DG201A DG202	
100		DG444 DG445	DG308A DG442 DG309A DG485 DG441	DG221	DG894 DG894	
85		DG308B DG309B	DG201B DG211B DG202B DG212B		DG182 DG191 DG185 DG200A DG188	
60	DG611 DG613 DG612				DG540 DG542 DG541	
50		DG5143	DG243 DG306A DG304A DG307A DG305A	DG300A DG381A DG301A DG384A DG302A DG387A DG303A DG5043	DG201HS	DG271
35 to 25		DG401 DG417 DG403 DG418 DG405 DG419 DG411 DG421 DG412 DG423 DG413 DG425			DG181 DG187 DG184 DG190	DG601
15					DG641 DG643	
10					DG180 DG189 DG183 DG642 DG188	

Dual DPST JFET Analog Switch

Features

- Standby Power: <1 mW
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- Off Isolation: > 60 dB @ 1 MHz
- Make-Before-Break

Benefits

- Minimizes Standby Power Requirements
- Better Radiation Tolerance
- Less Distortion
- Higher Frequency Switching
- Smooth Closed Loop Response

Applications

- Battery Powered Systems
- Aerospace Control Systems
- Low Distortion Circuits
- High Frequency Switching Circuits

Description

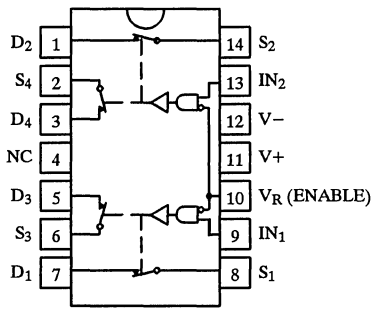
The DG129 is a dual double-pole single-throw analog switch for use in instrumentation, control, and audio communication systems. It is ideally suited for applications requiring a constant on-resistance over the entire analog range.

On-resistance for the DG129 is 20 Ω (typical), and on-leakage is < 2 nA. With all switches off, total power consumption is < 750 µW. These switches have make-before-break action and due to the processing are relatively radiation tolerant. An enable pin (V_R) simplifies interfacing with microprocessor, or other logic.

Each device contains four junction field-effect transistors (JFETs) to achieve constant on-resistance. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the on-off state of each switch. With logic "0" at the driver input the switches will be off. With a logic "1" at the input the switches will be on. In the on-state each switch will conduct current in either direction, and in the off-state each switch will block voltages up to 20 V peak-to-peak.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Four SPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.5 V

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
−55 to 125°C	14-Pin Sidebraze	DG129AP/883
		781401CA

1

Not Recommended for New Designs

Absolute Maximum Ratings

V+ to V− ..... 36 V
V+ to V_D ..... 36 V
V_D or V_S to V− ..... 36 V
V_D to V_S ..... ±22 V
V+ to V_R ..... 25 V
V_R to V− ..... 25 V
V_{IN} to V− ..... 30 V
V+ to V_{IN} ..... 25 V
V_{IN} to V_R ..... ±6 V
Current (any terminal) ..... 30 mA
Storage Temperture ..... −65 to 150°C
Power Dissipation[a]
14-Pin DIP[b] ..... 825 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 11 mW/°C above 75°C

Specifications[a]

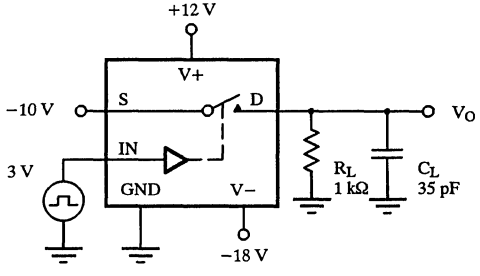
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = −18 V, V_R = 0 V, V_{IN} = 0.8 V or 2.5 V[f]	Temp[b]	A Suffix −55 to 125°C Min[d]	 Typ[c]	 Max[d]	Unit
Switch							
Analog Signal Range	V_{ANALOG}		Full	−10		10	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 10 V	Room Full		20	30 60	Ω
Source-Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V	Room Full	−1 −100	0.03	1 100	nA
Drain-Off Leakage Current	$I_{D(off)}$	V_D = ±10 V, V_S = ∓10 V	Room Full	−1 −100	0.02	1 100	
Channel-On Leakage Current	$I_{D(on)}$	V_D = V_S = −10 V	Room Full	−2 −100	−0.03		
Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.5 V	Room Full		15	60 120	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8 V	Room Full		0.005	0.1 2	
Dynamic							
Turn-On Time	t_{ON}	See Figure 1	Room		0.5	0.6	µs
Turn-Off Time	t_{OFF}		Room		1.1	1.6	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz V_D, V_S = 0	Room		2.4		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		2.4		
Channel-On Capacitance	$C_{D(on)}$		Room		2.8		
Off-Isolation	OIRR	R_L = 75 Ω, f = 1 MHz	Room		> 60		dB
Supply							
Positive Supply Current	I+	One Channel On V_{IN} = 2.5 V	Room		2.5	3	mA
Negative Supply Current	I−		Room	−1.8	−1.6		
Reference Supply Current	I_R		Room	−1.4	−1.1		
Positive Supply Current	I+	All Channel Off Both V_{IN} = 0 V	Room		0.6	25	µA
Negative Supply Current	I−		Room	−25	−0.5		
Reference Supply Current	I_R		Room	−25	−0.5		

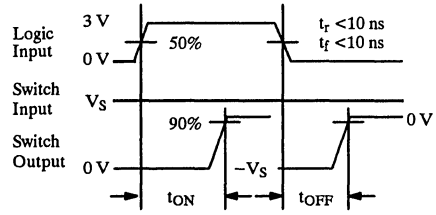
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = −55 to 125°C.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Not Recommended for New Designs

Test Circuits

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Logic "1" = Switch On

Figure 1. Switching Time

Application Hints

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_R Reference Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
12	−18	0	2.5/0.8	−10 to 10
15	−15	0	2.5/0.8	−7 to 13
7	−12	0	2.5/0.8	−5 to 5
5	−15	0	2.5/0.8	−7 to 3
5	−10	0	2.5/0.8	−2 to 3

1

Siliconix
A Member of the TEMIC Group

High-Speed Drivers with Dual SPST JFET Switches

Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Rad Hardness

Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- High Bandwidth Capability
- Fault Protection

Applications

- Audio Switching
- Video Switching
- Sample/Hold
- Guidance and Control Systems
- Aerospace

Description

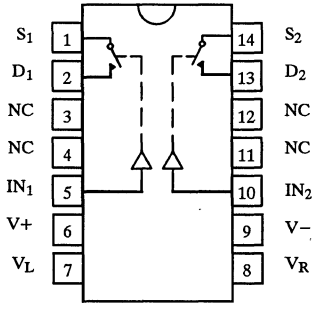
The DG180/181/182 are precision dual single-pole, single-throw (SPST) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG180—10 Ω, DG181—30 Ω, DG182—75 Ω). Reduced errors are achieved through low leakage current ($I_{D(on)}$ < 2 nA). Applications which benefit from the flat JFET on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises four n-channel JFET transistors and a TTL compatible bipolar driver. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than −60 dB at 10 MHz.

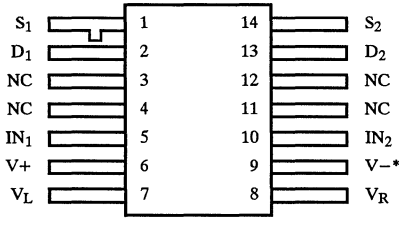
Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

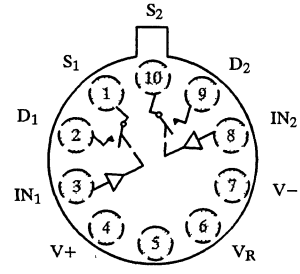
Flat Package



Top View

Refer to JAN38510 Information, Military Section

Metal Can



Top View

*Common to Substrate and Case

Ordering Information – DG180/181/182

Temp Range	Package	Part Number
−25 to 85°C	10-Pin Metal Can	DG180BA
		DG181BA
		DG182BA
	14-Pin Sidebraze	DG180BP
		DG181BP
		DG182BP
−55 to 125°C	10-Pin Metal Can	DG180AA/883, 5962-8767301IA
		DG181AA/883, JM38510/11101BIA
		DG182AA/883, JM38510/11102BIA
	14-Pin Sidebraze	DG180AP/883, 5962-8767301CA
		DG181AP/883, JM38510/11101BCA
		DG182AP/883, JM38510/11102BCA
	14-Pin Flat Pack	5962-8767301XA
		JM38510/11101BXA
		JM38510/11102BXA

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 36 V
V+ to V_D ..... 33 V
V_D to V− ..... 33 V
V_D to V_D ..... ±22 V
V_L to V− ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V− ..... 27 V
V_R to V_{IN} ..... 2 V
Current (S or D) DG180 ..... 200 mA
Current (S or D) DG181, DG182 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... −65 to 150°C
Power Dissipation[a]
10-Pin Metal Can[b] ..... 450 mW
14-Pin Sidebraze[c] ..... 825 mW
14-Pin Flat Pack[d] ..... 900 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 6 mW/°C above 75°C
c. Derate 11 mW/°C above 75°C
d. Derate 10 mW/°C above 75°C

Specifications[a] for DG180

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 2 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		10 1000		15 300	nA
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		10 1000		15 300	
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V	Room Hot	−0.1	−2 −200		−10 −200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration	Room	300					mA
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	240		400		600	ns
Turn-Off Time	t_{off}		Room	140		200		250	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	21					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	17					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	17					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>55					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I−		Room	−2.7	−5		−5		
Logic Supply Current	I_L		Room	3		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

1

Specifications[a] for DG181

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 2 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V		Room Full	18		30 60		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V		Room Hot	0.05		1 100		5 100	nA
		V_S = ±7.5 V, V_D = ∓7.5 V		Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V		Room Hot	0.5		1 100		5 100	
		V_S = ±7.5 V, V_D = ∓7.5 V		Room Hot	0.6		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V		Room Hot	−0.02	−2 −200		−10 −200		
Digital Input										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V		Full	−30	−250		−250		
Dynamic Characteristics										
Turn-On Time	t_{on}	See Switching Time Test Circuit		Room	85		150		180	ns
Turn-Off Time	t_{off}			Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz	V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$		V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω		Room	>50					dB
Power Supplies										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I−			Room	−2.7	−5		−5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	−1	−2		−2		

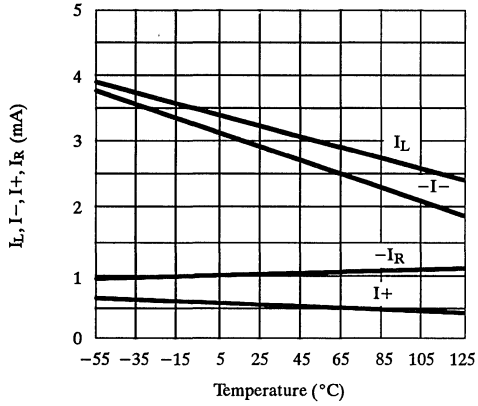
Specifications[a] for DG182

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 2 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−10	15	−10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	35		75 150		100 150	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		1 100		5 100	nA
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.4		1 100		5 100	
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.5		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±10 V	Room Hot	−0.02	−2 −200		−10 −200		
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	t_{off}		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>50					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I−		Room	−2.7	−5		−5		
Logic Supply Current	I_L		Room	3.1		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

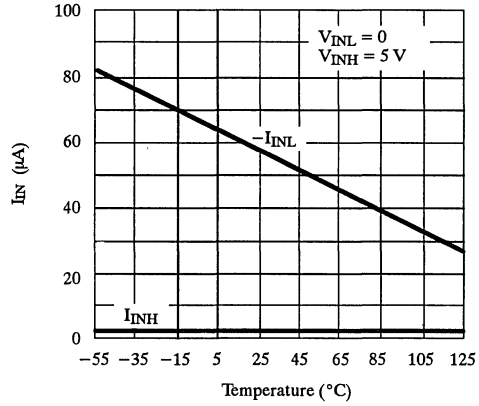
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

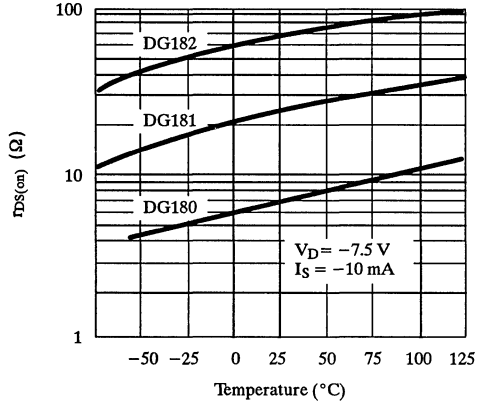
Supply Current vs. Temperature



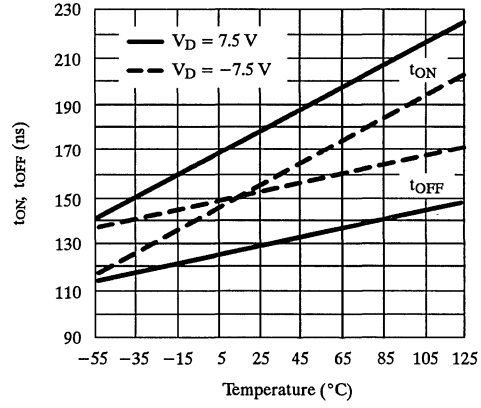
I_{IN} vs. V_{IN} and Temperature



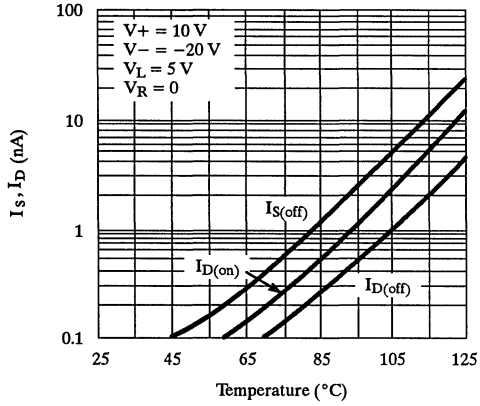
$r_{DS(on)}$ vs. Temperature



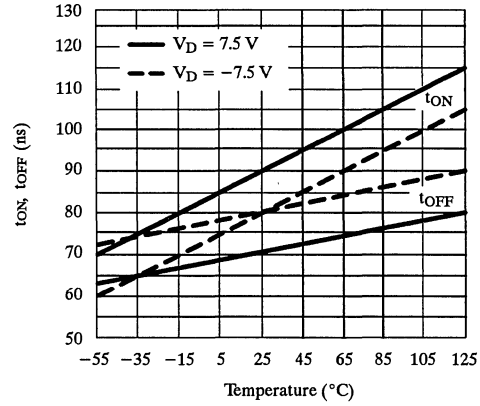
Switching Time vs. V_D and Temperature (DG180)



Leakage vs. Temperature (DG180)

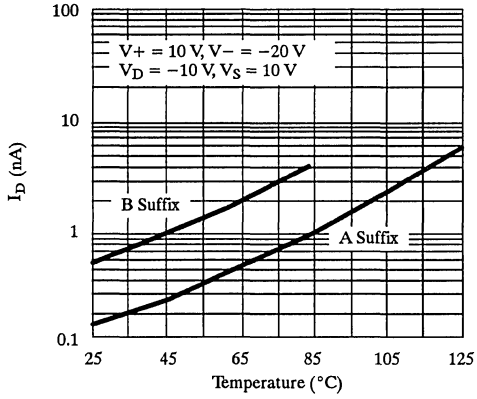


Switching Time vs. V_D and Temperature (DG181/182)

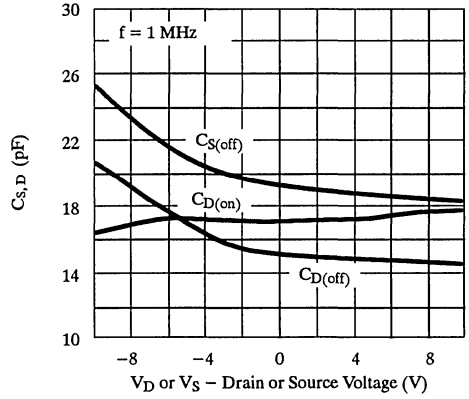


Typical Characteristics (Cont'd)

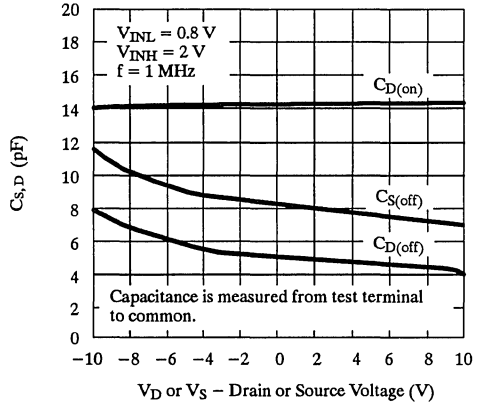
$I_{D(off)}$ vs. Temperature (DG181/182)



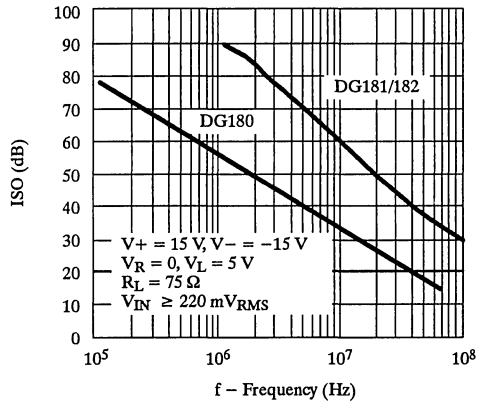
Capacitance vs. V_D or V_S (DG180)



Capacitance vs. V_D or V_S (DG181/182)



Off Isolation vs. Frequency



Schematic Diagram (Typical Channel)

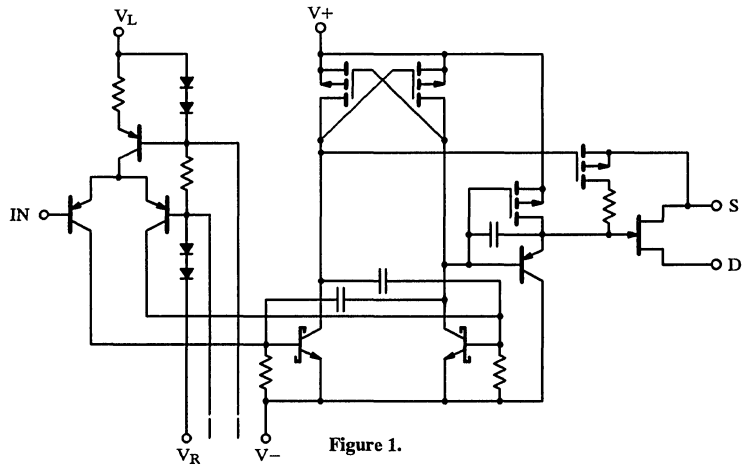
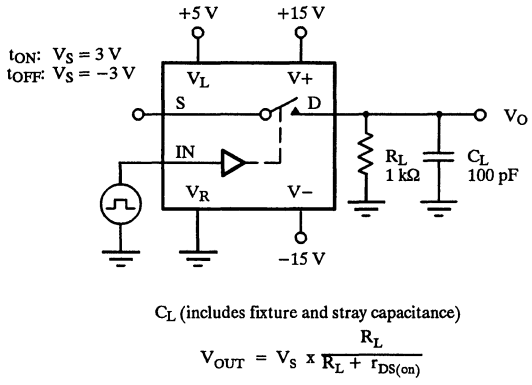


Figure 1.

1

Test Circuits

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.



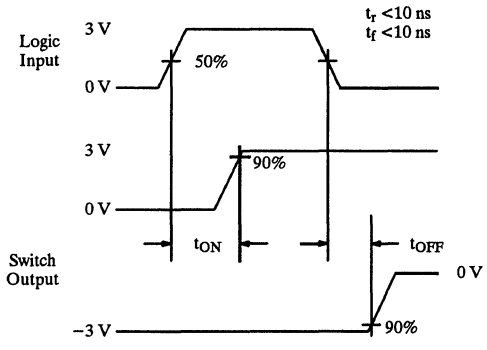


Figure 2. Switching Time

Application Hints[a]

Switch	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}$/$V_{INL(max)}$ (V)	V_S Analog Voltage Range (V)
DG180 DG181	15[b]	−15	5	GND	2.0/0.8	−7.5 to 15
	10	−20	5	GND	2.0/0.8	−12.5 to 10
	12	−12	5	GND	2.0/0.8	−4.5 to 12
DG182	15[b]	−15	5	GND	2.0/0.8	−10 to 15
	10	−20	5	GND	2.0/0.8	−15 to 10
	12	−12	5	GND	2.0/0.8	−7 to 12

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

High-Speed Drivers with Dual DPST JFET Switches

Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Break-Before-Make Switching
- Rad Hardness

Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- Improved Channel Isolation
- Eliminates Inadvertent Shorting Between Channels
- Fault Protection

Applications

- Audio Switching
- Precision Switching
- Video Switching
- Video Routing
- Sample/Hold
- Aerospace

Description

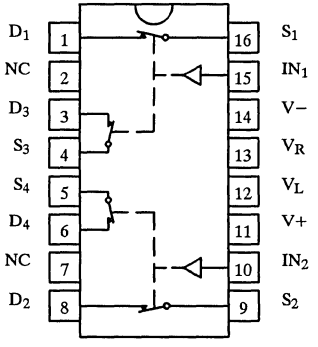
The DG183/184/185 are precision dual double-pole, single-throw (DPST) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG183—10 Ω, DG184—30 Ω, DG185—75 Ω). Reduced errors are achieved through low leakage current ($I_{D(on)}$ < 2 nA). Applications which benefit from the flat JFET on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises four n-channel JFET transistors and a TTL compatible bipolar driver. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than −60 dB at 10 MHz.

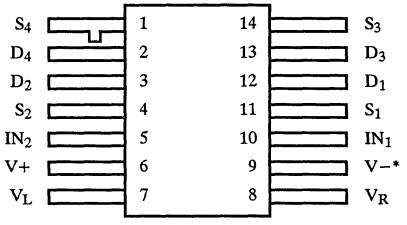
Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Flat Package



Top View

Refer to JAN38510 Information, Military Section

*Common to Substrate and Case

Ordering Information – DG183/184/185

Temp Range	Package	Part Number
−25 to 85°C	16-Pin Sidebraze	DG183BP
		DG184BP
		DG185BP
−55 to 125°C	16-Pin Sidebraze	DG183AP/883
		DG184AP
		DG184AP/883, JM38510/11103BEA
		DG185AP/883, JM38510/11104BEA
	14-Pin Flat Pack	JM38510/11103BXA
		JM38510/11104BXA

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V
Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 36 V
V+ to V_D ..... 33 V
V_D to V− ..... 33 V
V_D to V_D ..... ±22 V
V_L to V− ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V− ..... 27 V
V_R to V_{IN} ..... 2 V

Current (S or D) DG183 ..... 200 mA
Current (S or D) DG184, DG185 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... −65 to 150°C
Power Dissipation[a]
16-Pin Sidebraze[b] ..... 900 mW
14-Pin Flat Pack[c] ..... 900 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 12 mW/°C above 75°C
c. Derate 10 mW/°C above 75°C

Specifications[a] for DG183

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 V or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		10 1000		15 300	nA
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		10 1000		15 300	
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V	Room Hot	−0.1	−2 −200		−10 −200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration	Room	300					mA
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	240		400		600	ns
Turn-Off Time	t_{off}		Room	140		200		220	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	21					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	17					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	17					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>55					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I−		Room	−2.7	−5		−5		
Logic Supply Current	I_L		Room	3.1		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

Specifications[a] for DG184

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 V or 2 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	B Suffix −25 to 85°C Min[d]	 Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V		Room Full	22		30 60		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V		Room Hot	0.06		1 100		5 100	nA
		V_S = ±7.5 V, V_D = ∓7.5 V		Room Hot	0.05		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V		Room Hot	0.4		1 100		5 100	
		V_S = ±7.5 V, V_D = ∓7.5 V		Room Hot	0.3		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V		Room Hot	−0.02	−2 −200		−10 −200		
Digital Input										
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V		Full	−30	−250		−250		
Dynamic Characteristics										
Turn-On Time	t_{on}	See Switching Time Test Circuit		Room	85		150		180	ns
Turn-Off Time	t_{off}			Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz	V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$		V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω		Room	>50					dB
Power Supplies										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		3		3	mA
Negative Supply Current	I−			Room	−2.7	−5.5		−5.5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	−1	−2		−2		

1

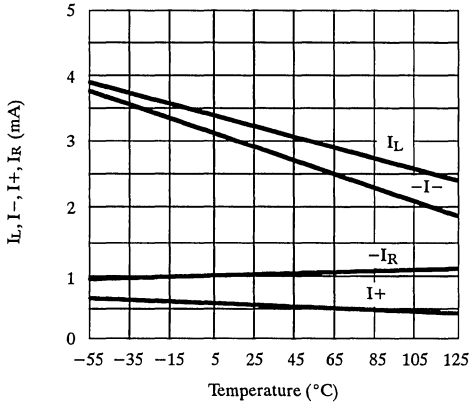
Specifications[a] for DG185

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 V or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	B Suffix −25 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−10	15	−10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	35		75 150		100 150	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		1 100		5 100	nA
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.4		1 100		5 100	
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.3		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±10 V	Room Hot	−0.03	−2 −200		−10 −200		
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	t_{off}		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>50					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		3		3	mA
Negative Supply Current	I−		Room	−2.7	−5.5		−5.5		
Logic Supply Current	I_L		Room	3.1		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

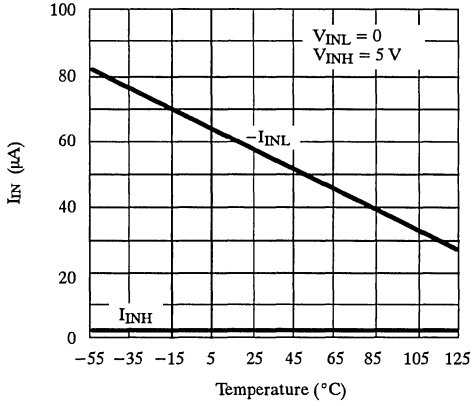
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

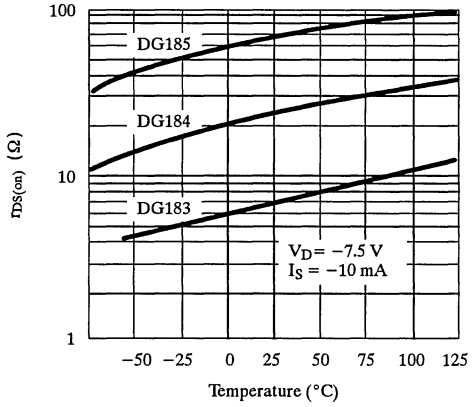
Supply Current vs. Temperature



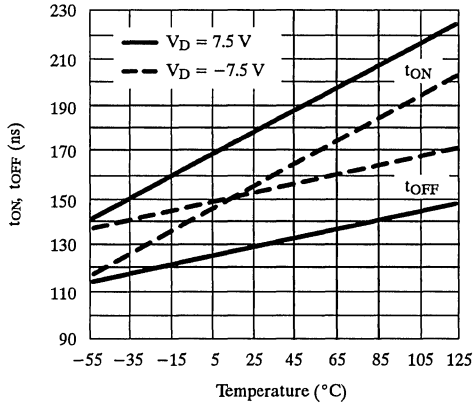
I_{IN} vs. V_{IN} and Temperature



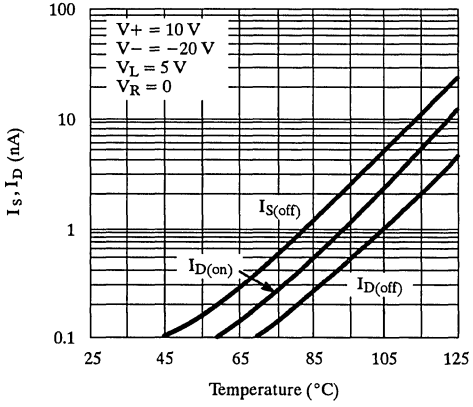
$r_{DS(on)}$ vs. Temperature



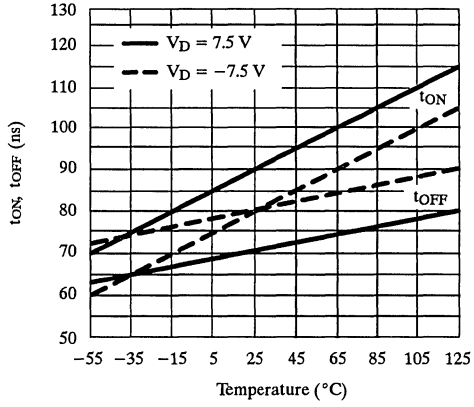
Switching Time vs. V_D and Temperature (DG183)



Leakage vs. Temperature (DG183)



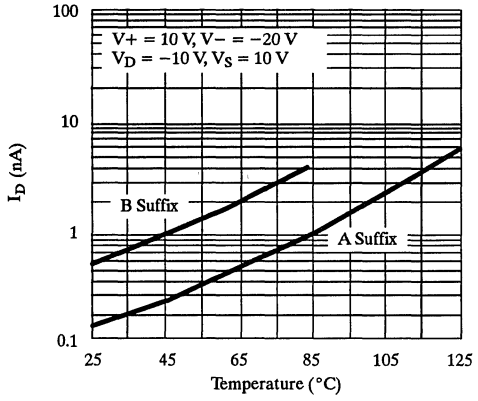
Switching Time vs. V_D and Temperature (DG184/185)



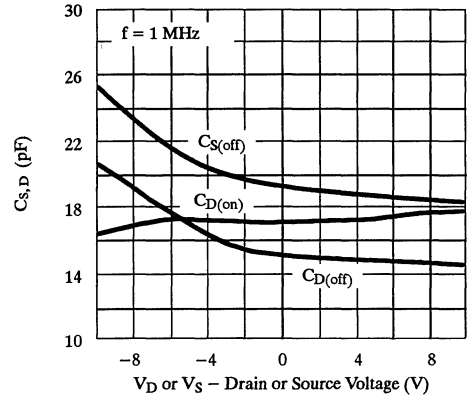
1

Typical Characteristics (Cont'd)

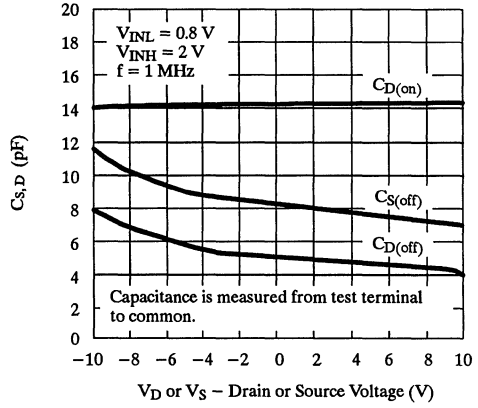
$I_{D(off)}$ vs. Temperature (DG184/185)



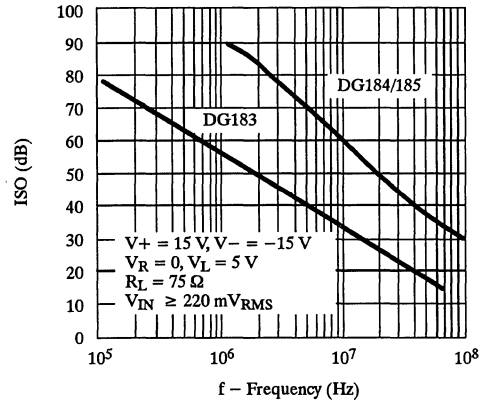
Capacitance vs. V_D or V_S (DG183)



Capacitance vs. V_D or V_S (DG184/185)



Off Isolation vs. Frequency



Schematic Diagram (Typical Channel)

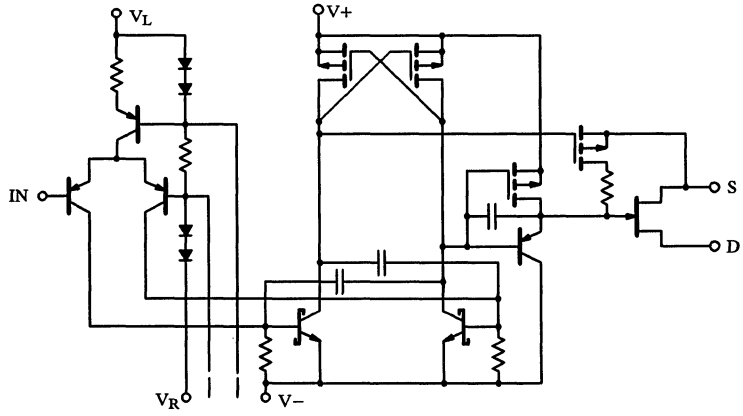
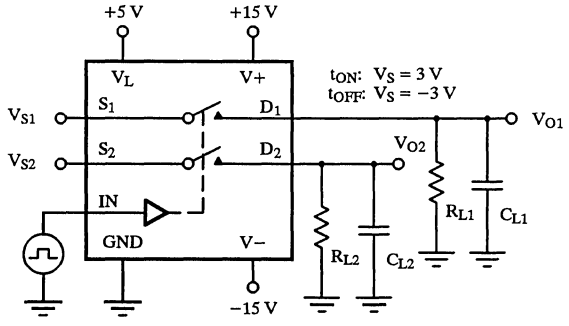


Figure 1.

Test Circuits

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_S \times \frac{R_L}{R_L + r_{DS(on)}}$$

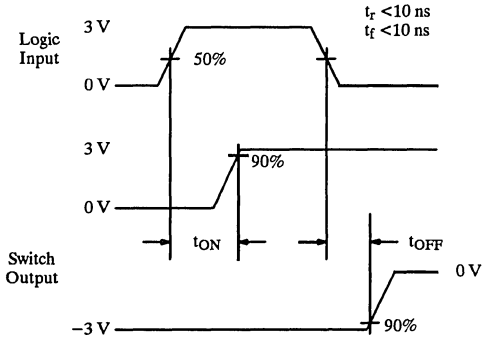


Figure 2. Switching Time

Application Hints[a]

Switch	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}$/ $V_{INL(max)}$ (V)	V_S Analog Voltage Range (V)
DG183 DG184	15[b]	−15	5	GND	2.0/0.8	−7.5 to 15
	10	−20	5	GND	2.0/0.8	−12.5 to 10
	12	−12	5	GND	2.0/0.8	−4.5 to 12
DG185	15[b]	−15	5	GND	2.0/0.8	−10 to 15
	10	−20	5	GND	2.0/0.8	−15 to 10
	12	−12	5	GND	2.0/0.8	−7 to 12

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND.

Siliconix
A Member of the TEMIC Group

High-Speed Drivers with SPDT JFET Switches

Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Rad Hardness

Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- High Bandwidth Capability
- Fault Protection

Applications

- Audio Switching
- Video Switching
- Sample/Hold
- Guidance and Control Systems
- Telemetry

Description

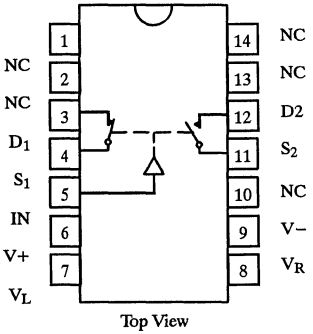
The DG186/187/188 are precision single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG186—10 Ω, DG187—30 Ω, DG188—75 Ω). Reduced errors are achieved through low leakage current ($I_{D(on)}$ < 2 nA). Applications which benefit from the flat JFET on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises two n-channel JFET transistors and a TTL compatible bipolar driver. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than −60 dB at 10 MHz.

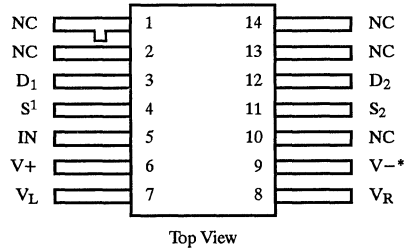
Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

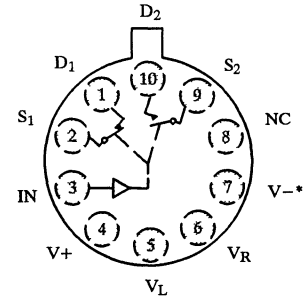
Flat Package



Top View

Refer to JAN38510 Information, Military Section

Metal Can



Top View

*Common to Substrate and Case

Ordering Information – DG186/187/188

Temp Range	Package	Part Number
−25 to 85°C	10-Pin Metal Can	DG186BA
		DG187BA
		DG188BA
	14-Pin Sidebraze	DG186BP
		DG187BP
		DG188BP
−55 to 125°C	10-Pin Metal Can	DG186AA/883
		DG187AA/883, JM38510/11105BIA
		DG188AA/883, JM38510/11106BIA
	14-Pin Sidebraze	DG186AP/883
		DG187AP/883, JM38510/11105BCA
		DG188AP/883, JM38510/11106BCA
	14-Pin Flat Pack	JM38510/11105BXA
		JM38510/11106BXA

Truth Table

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 36 V
V+ to V_D ..... 33 V
V_D to V− ..... 33 V
V_D to V_D ..... ±22 V
V_L to V− ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V− ..... 27 V
V_R to V_{IN} ..... 2 V
Current (S or D) DG186 ..... 200 mA
Current (S or D) DG187, DG188 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... −65 to 150°C
Power Dissipation[a]
10-Pin Metal Can[b] ..... 450 mW
14-Pin Sidebraze[c] ..... 825 mW
14-Pin Flat Pack[d] ..... 900 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 6 mW/°C above 75°C
c. Derate 11 mW/°C above 75°C
d. Derate 10 mW/°C above 75°C

Specifications[a] for DG186

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		10 1000		15 300	nA
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		10 1000		15 300	
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V	Room Hot	−0.1	−2 −200		−10 −200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration	Room	300					mA
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	240		400		425	ns
Turn-Off Time	t_{off}		Room	140		200		225	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	21					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	17					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	17					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>55					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room			0.8		0.8	mA
Negative Supply Current	I−		Room		−3		−3		
Logic Supply Current	I_L		Room			3.2		3.2	
Reference Supply Current	I_R		Room		−2		−2		

Specifications[a] for DG187

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	B Suffix −25 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	22		30 60		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.06		1 100		5 100	nA
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.13		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		1 100		5 100	
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.03		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V	Room Hot	−0.02	−2 −200		−10 −200		
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	85		150		180	ns
Turn-Off Time	t_{off}		Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>50					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room			0.8		0.8	mA
Negative Supply Current	I−		Room		−3		−3		
Logic Supply Current	I_L		Room			3.2		3.2	
Reference Supply Current	I_R		Room		−2		−2		

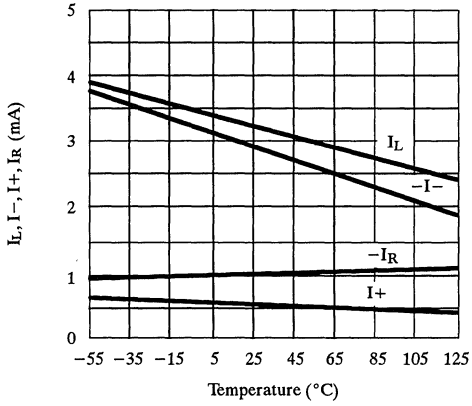
Specifications[a] for DG188

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	B Suffix −25 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−10	15	−10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	35		75 150		100 150	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		1 100		5 100	nA
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		1 100		5 100	
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.50		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±10 V	Room Hot	−0.03	−2 −200		−10 −200		
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	t_{off}		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>50					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room			0.8		0.8	mA
Negative Supply Current	I−		Room		−3		−3		
Logic Supply Current	I_L		Room			3.2		3.2	
Reference Supply Current	I_R		Room		−2		−2		

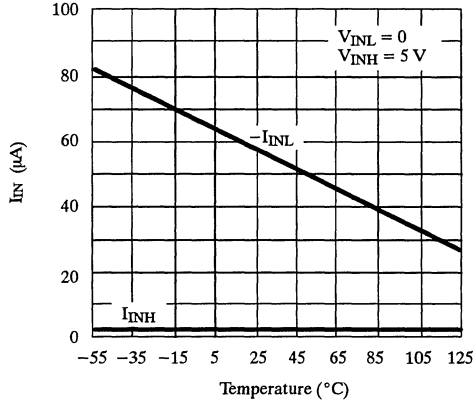
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

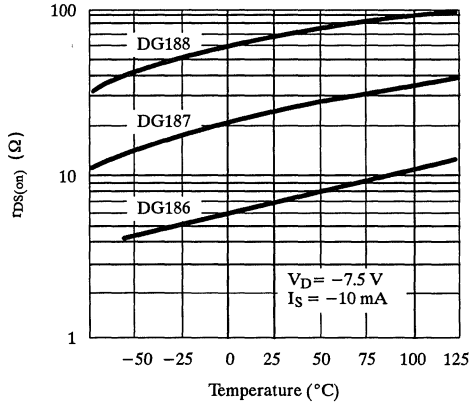
Supply Current vs. Temperature



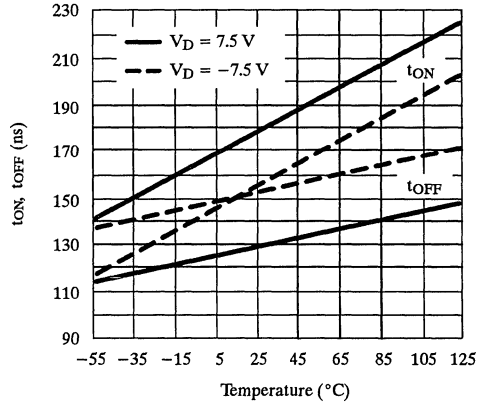
I_{IN} vs. V_{IN} and Temperature



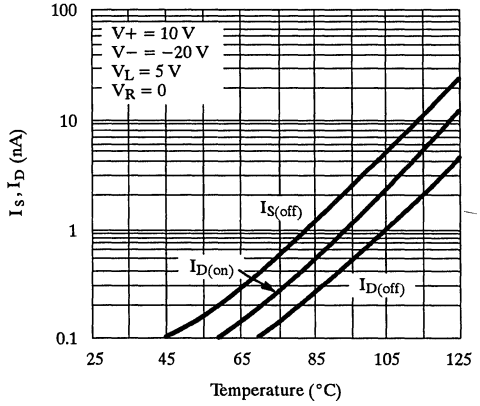
$r_{DS(on)}$ vs. Temperature



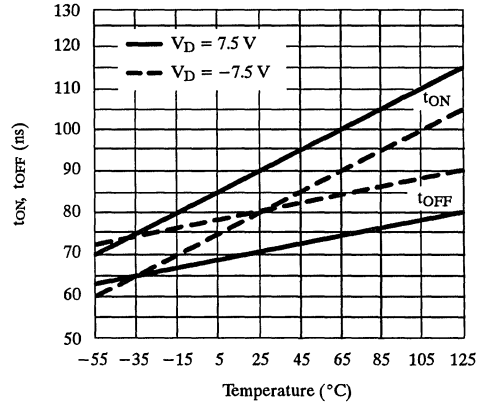
Switching Time vs. V_D and Temperature (DG186)



Leakage vs. Temperature (DG186)

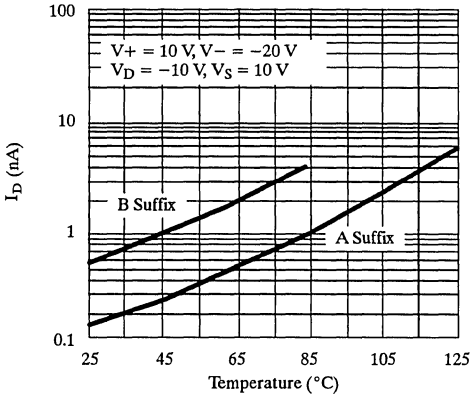


Switching Time vs. V_D and Temperature (DG187/188)

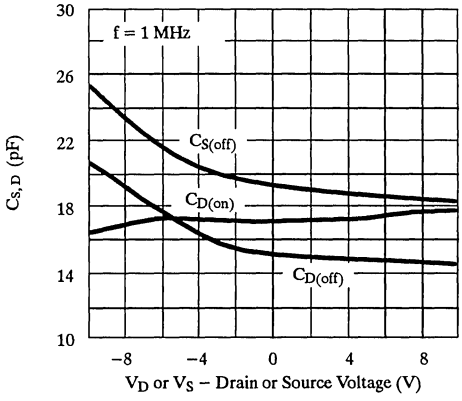


Typical Characteristics (Cont'd)

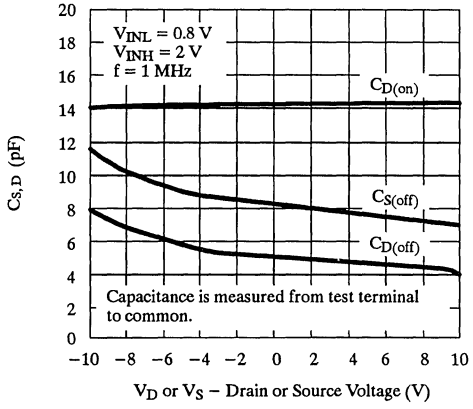
$I_{D(off)}$ vs. Temperature (DG187/188)



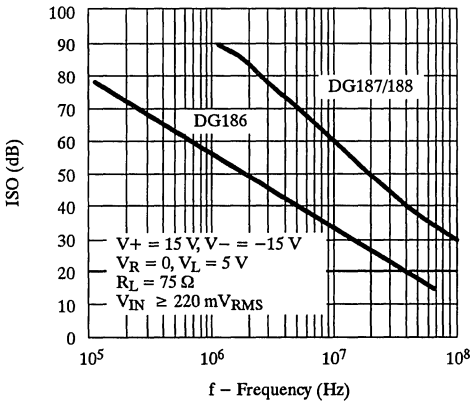
Capacitance vs. V_D or V_S (DG186)



Capacitance vs. V_D or V_S (DG187/188)



Off Isolation vs. Frequency



Schematic Diagram (Typical Channel)

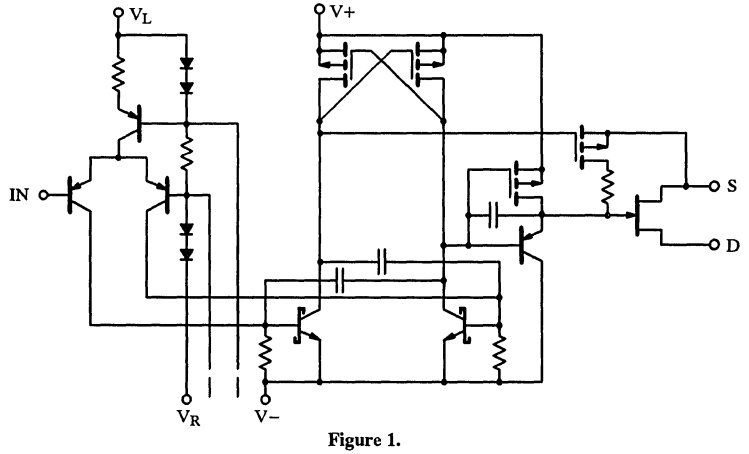


Figure 1.

Test Circuits

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.

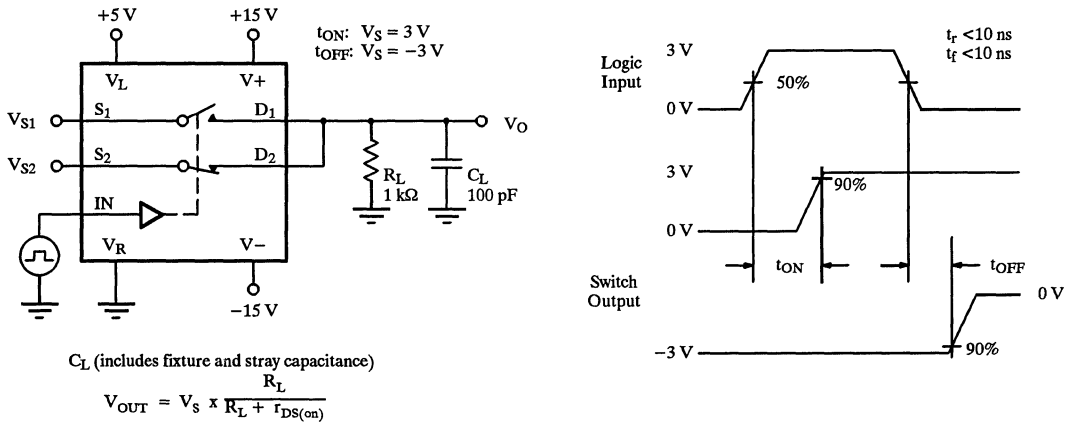


Figure 2. Switching Time

Application Hints[a]

Switch	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}$/$V_{INL(max)}$ (V)	V_S Analog Voltage Range (V)
DG186 DG187	15[b]	−15	5	GND	2.0/0.8	−7.5 to 15
	10	−20	5	GND	2.0/0.8	−12.5 to 10
	12	−12	5	GND	2.0/0.8	−4.5 to 12
DG188	15[b]	−15	5	GND	2.0/0.8	−10 to 15
	10	−20	5	GND	2.0/0.8	−15 to 10
	12	−12	5	GND	2.0/0.8	−7 to 12

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

High-Speed Drivers with Dual SPDT JFET Switches

Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Rad Hardness

Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- High Bandwidth Capability
- Fault Protection

Applications

- Audio Switching
- Video Switching
- Sample/Hold
- Guidance and Control Systems
- Aerospace

Description

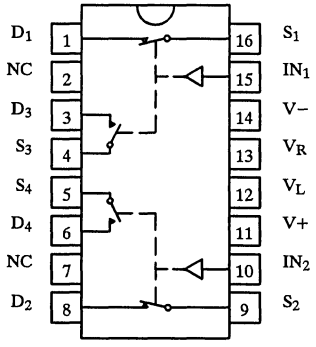
The DG189/190/191 are precision dual single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG189—10 Ω, DG190—30 Ω, DG191—75 Ω). Reduced errors are achieved through low leakage current ($I_{D(on)}$ < 2 nA). Applications which benefit from the flat JFET on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises four n-channel JFET transistors and a TTL compatible bipolar driver. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than −60 dB at 10 MHz.

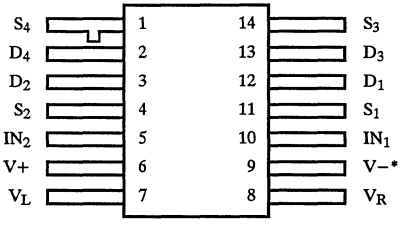
Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Flat Package



Top View

Refer to JAN38510 Information, Military Section

*Common to Substrate and Case

Ordering Information – DG189/190/191

Temp Range	Package	Part Number
−25 to 85°C	16-Pin Sidebraze	DG189BP
		DG190BP
		DG191BP
−55 to 125°C	16-Pin Sidebraze	DG189AP/883, 5962-9068901MEA
		DG190AP/883, JM38510/11107BEA
		DG191AP/883, JM38510/11108BEA
	14-Pin Flat Pack	JM38510/11107BXA
		JM38510/11108BXA

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 36 V
V+ to V_D ..... 33 V
V_D to V− ..... 33 V
V_D to V_D ..... ±22 V
V_L to V− ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V− ..... 27 V
V_R to V_{IN} ..... 2 V

Current (S or D) DG189 ..... 200 mA
Current (S or D) DG190, DG191 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... −65 to 150°C
Power Dissipation[a]
16-Pin Sidebraze[b] ..... 900 mW
14-Pin Flat Pack[c] ..... 900 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 12 mW/°C above 75°C
c. Derate 10 mW/°C above 75°C

Specifications[a] for DG189

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 V or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		10 1000		15 300	nA
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		10 1000		15 300	
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V	Room Hot	−0.1	−2 −200		−10 −200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration	Room	300					mA
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	240		400		425	ns
Turn-Off Time	t_{off}		Room	140		200		225	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	21					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	17					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	17					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>55					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I−		Room	−2.7	−5		−5		
Logic Supply Current	I_L		Room	3.1		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

Specifications[a] for DG190

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 V or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	B Suffix −25 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−7.5	15	−7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	18		30 60		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.06		1 100		5 100	nA
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.1		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		1 100		5 100	
		V_S = ±7.5 V, V_D = ∓7.5 V	Room Hot	0.06		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±7.5 V	Room Hot	−0.02	−2 −200		−10 −200		
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	85		150		180	ns
Turn-Off Time	t_{off}		Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>50					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I−		Room	−2.7	−5		−5		
Logic Supply Current	I_L		Room	3.1		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

1

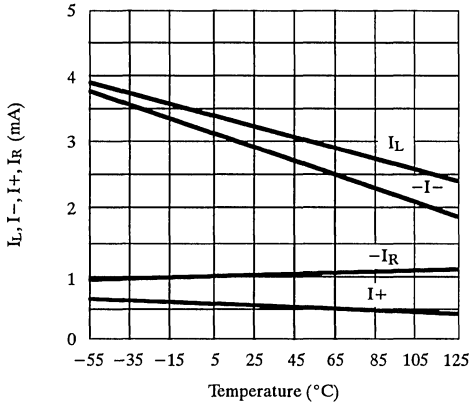
Specifications[a] for DG191

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_L = 5 V V_R = 0 V, V_{IN} = 0.8 V or 2 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B Suffix −25 to 85°C Min[d]	B Suffix −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−10	15	−10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = −7.5 V	Room Full	35		75 150		100 150	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.05		1 100		5 100	nA
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±10 V, V_D = ∓10 V V+ = 10 V, V− = −20 V	Room Hot	0.04		1 100		5 100	
		V_S = ±10 V, V_D = ∓10 V	Room Hot	0.05		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±10 V	Room Hot	−0.03	−2 −200		−10 −200		
Digital Input									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	−30	−250		−250		
Dynamic Characteristics									
Turn-On Time	t_{on}	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	t_{off}		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = −5 V, I_D = 0	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_D = −5 V, I_S = 0	Room	6					
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_D = V_S = 0 V	Room	14					
Off Isolation	OIRR	f = 1 MHz, R_L = 75 Ω	Room	>50					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I−		Room	−2.7	−5		−5		
Logic Supply Current	I_L		Room	3.1		4.5		4.5	
Reference Supply Current	I_R		Room	−1	−2		−2		

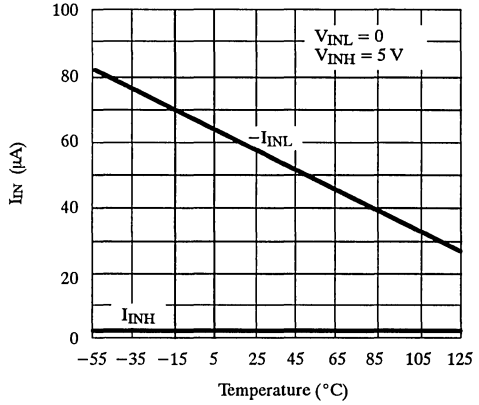
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

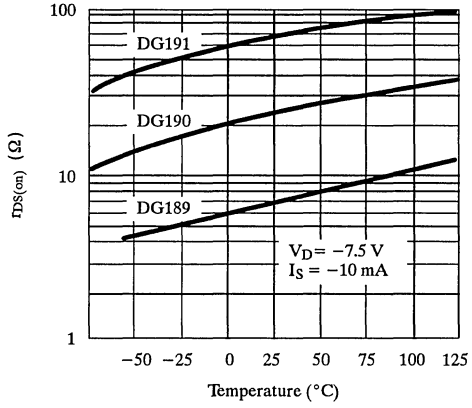
Supply Current vs. Temperature



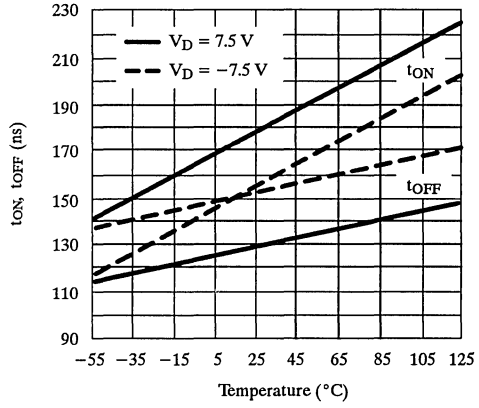
I_{IN} vs. V_{IN} and Temperature



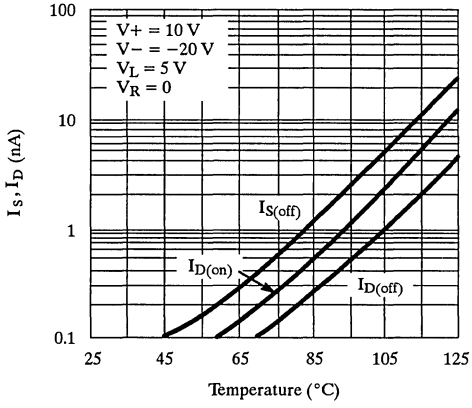
$r_{DS(on)}$ vs. Temperature



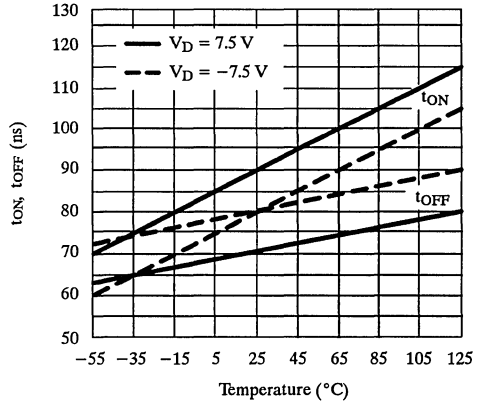
Switching Time vs. V_D and Temperature (DG189)



Leakage vs. Temperature (DG189)



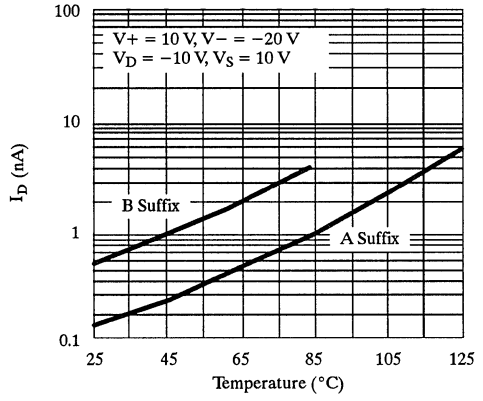
Switching Time vs. V_D and Temperature (DG190/191)



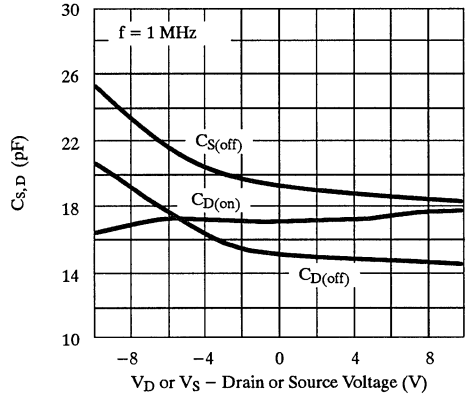
1

Typical Characteristics (Cont'd)

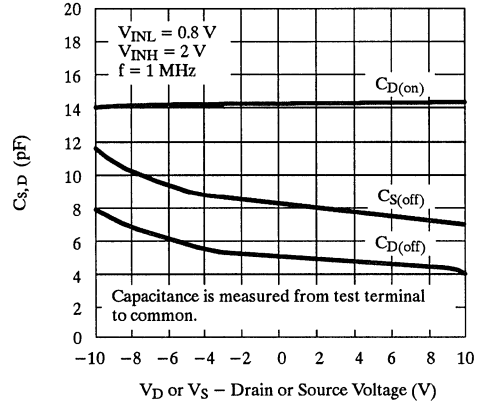
$I_{D(off)}$ vs. Temperature (DG190/191)



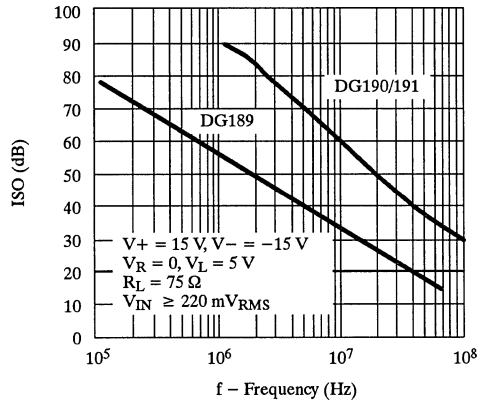
Capacitance vs. V_D or V_S (DG189)



Capacitance vs. V_D or V_S (DG190/191)



Off Isolation vs. Frequency



Schematic Diagram (Typical Channel)

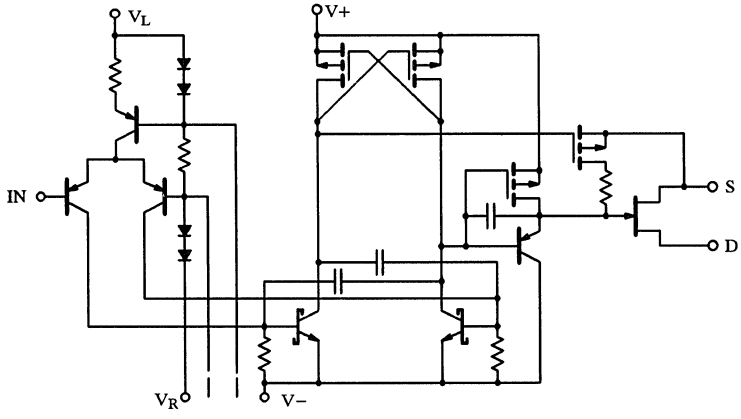


Figure 1.

Test Circuits

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.

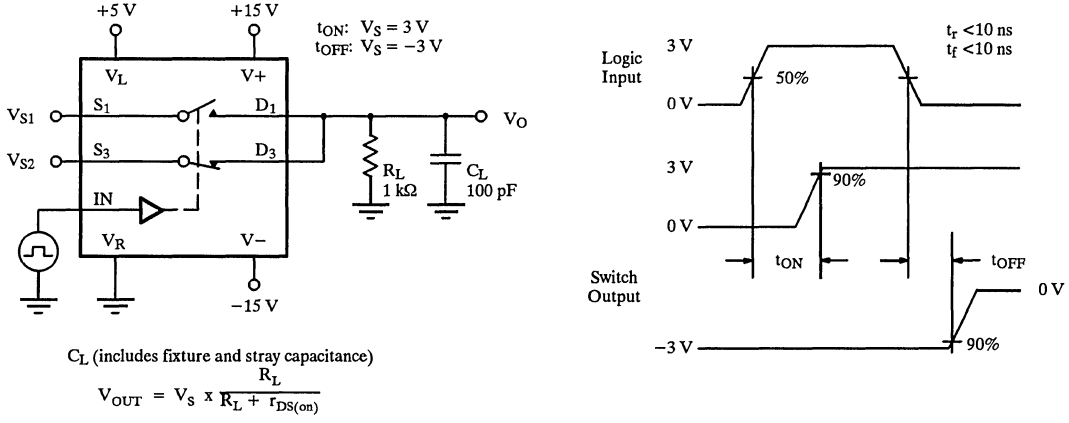


Figure 2. Switching Time

Application Hints[a]

Switch	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}$/ $V_{INL(max)}$ (V)	V_S Analog Voltage Range (V)
DG189 DG190	15[b]	−15	5	GND	2.0/0.8	−7.5 to 15
	10	−20	5	GND	2.0/0.8	−12.5 to 10
	12	−12	5	GND	2.0/0.8	−4.5 to 12
DG191	15[b]	−15	5	GND	2.0/0.8	−10 to 15
	10	−20	5	GND	2.0/0.8	−15 to 10
	12	−12	5	GND	2.0/0.8	−7 to 12

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

Siliconix
A Member of the TEMIC Group

Monolithic Dual SPST CMOS Analog Switch

Features

- ±15 V Input Signal Range
- 44-V Maximum Supply Ranges
- On-Resistance: 45 Ω
- TTL and CMOS Compatibility

Benefits

- Wide Dynamic Range
- Simple Interfacing
- Reduced External Component Count

Applications

- Servo Control Switching
- Programmable Gain Amplifiers
- Audio Switching
- Programmable Filters

Description

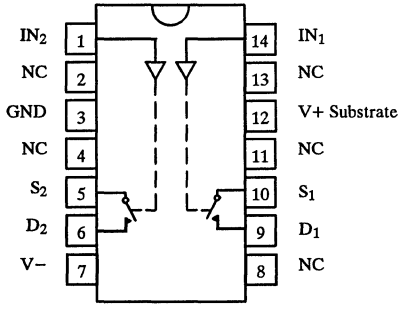
The DG200A is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low on-resistance.

The DG200A is designed on Siliconix' improved PLUS-40 CMOS process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. In the on condition, this bi-directional switch introduces no offset voltage of its own.

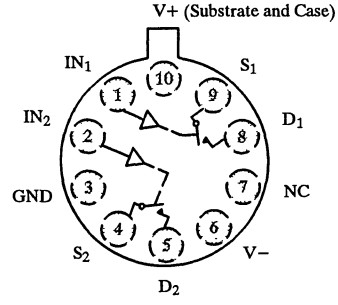
Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Metal Can



Top View

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG200ACJ
−25 to 85°C	14-Pin CerDIP	DG200ABK
	10-Pin Metal Can	DG200ABA
−55 to 125°C	14-Pin CerDIP	DG200AAK
		DG200AAK/883, JM38510/12301BCA
	10-Pin Metal Can	DG200AAA
		DG200AAA/883, JM38510/12301BIC
	14-Pin Sidebraze	JM38510/12301BCC

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 44 V

GND to V− ..... 25 V

Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 30 mA, whichever occurs first

Current (Any Terminal) Continuous ..... 30 mA

Current S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA

Storage Temperature (AX, BX Suffix)..... −65 to 150°C
(CJ Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
10-Pin Metal Can[c] ..... 450 mW
14-Pin CerDIP[d] ..... 825 mW
14-Pin Plastic DIP[e] ..... 470 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 11 mW/°C above 75°C
e. Derate 6.5 mW/°C above 25°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C Suffix Min[d]	B, C Suffix Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −1 mA	Room Full	45		70 100		80 100	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.01	−2 −100	2 100	−5 −100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	±0.01	−2 −100	2 100	−5 −100	5 100	
Channel On Leakage Current[f]	$I_{D(on)}$	V_S = V_D = ±14 V	Room Full	±0.1	−2 −200	2 200	−5 −200	5 200	
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4 V	Room Full	0.0009	−0.5 −1		−1 −10		µA
		V_{IN} = 15 V	Room Full	0.005		0.5 1		1 10	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	−0.0015	−0.5 −1		−1 −10		
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Switching Time Test Circuit	Room	440		1000		1000	ns
Turn-Off Time	t_{OFF}		Room	340		425		425	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room	−10					pC
Source-Off Capacitance	$C_{S(off)}$	f = 140 kHz, V_{IN} = 5 V; V_S = 0 V	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 140 kHz, V_{IN} = 5 V; V_D = 0 V	Room	9					
Channel-On Capacitance	$C_{D(on)}$ + $C_{S(On)}$	V_D = V_S = 0 V, V_{IN} = 0 V	Room	25					
Off Isolation	OIRR	V_{IN} = 5 V, R_L = 75 Ω, V_S = 2 V, f = 1 MHz	Room	75					dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room	90					

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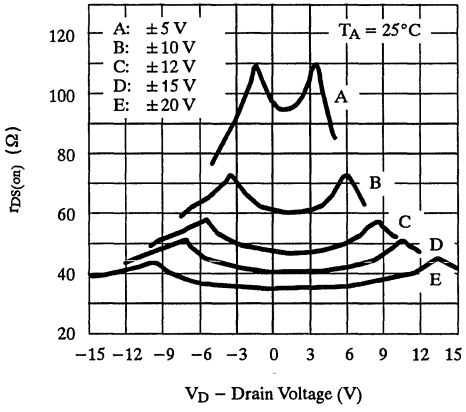
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C Suffix Min[d]	B, C Suffix Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	Both Channels On or Off V_{IN} = 0 V and 2.4 V	Room	0.8		2		2	mA
Negative Supply Current	I−		Room	−0.23	−1		−1		

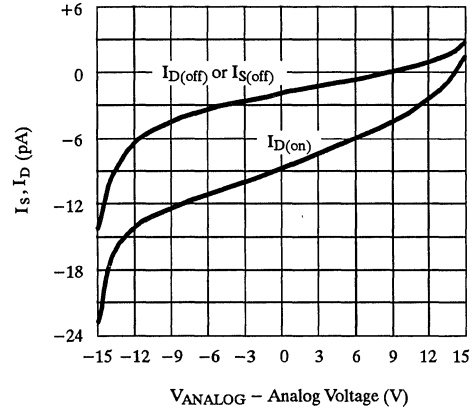
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is aminimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

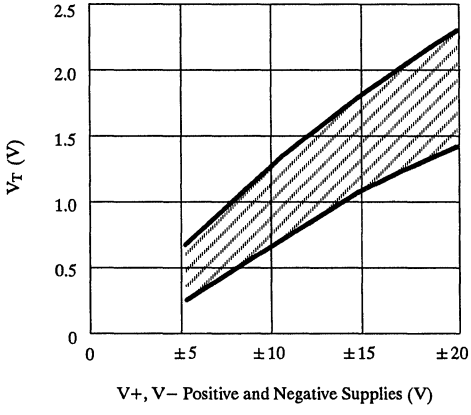
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



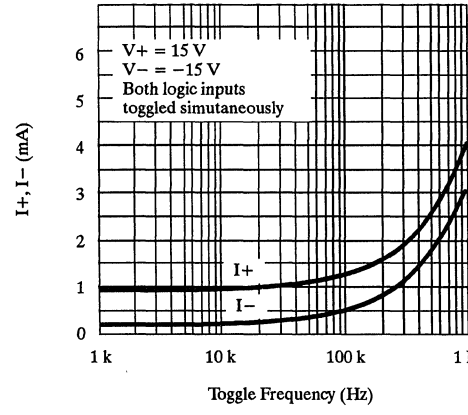
Leakage Currents vs. Analog Voltage



Input Switching Threshold vs. V+ and V− Supply Voltages



Supply Currents vs. Toggle Frequency



Schematic Diagram (Typical Channel)

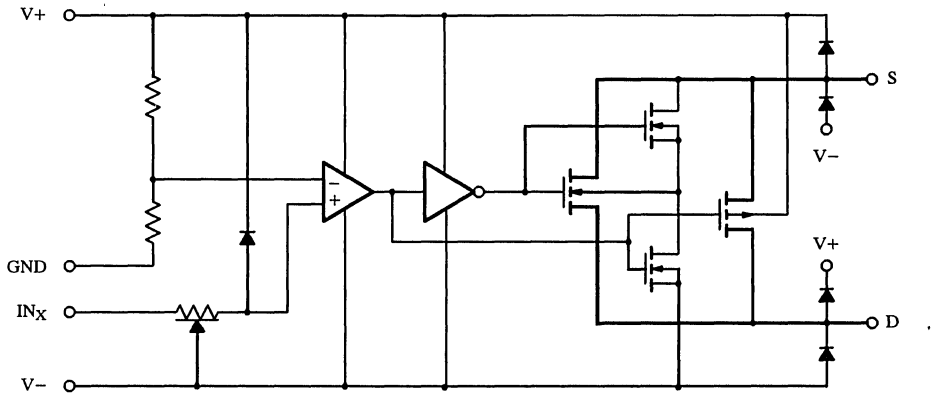


Figure 1.

Test Circuits

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

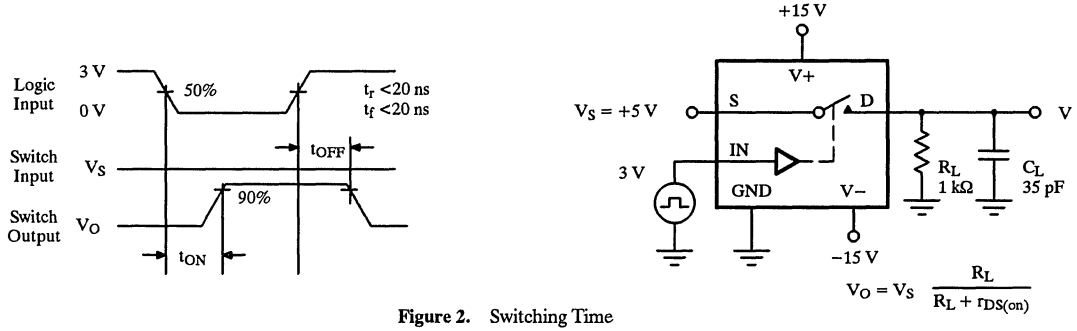


Figure 2. Switching Time

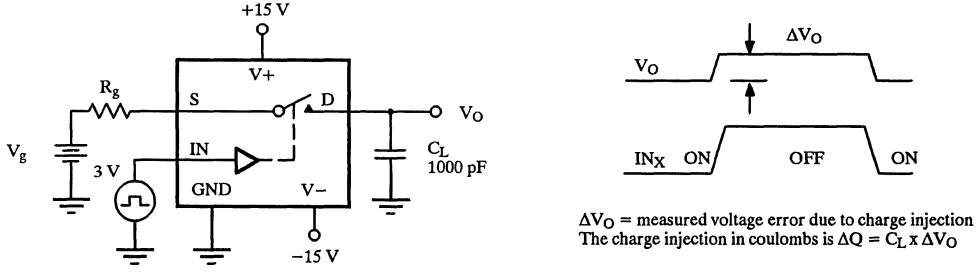


Figure 3. Charge Injection

Test Circuits (Cont'd)

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

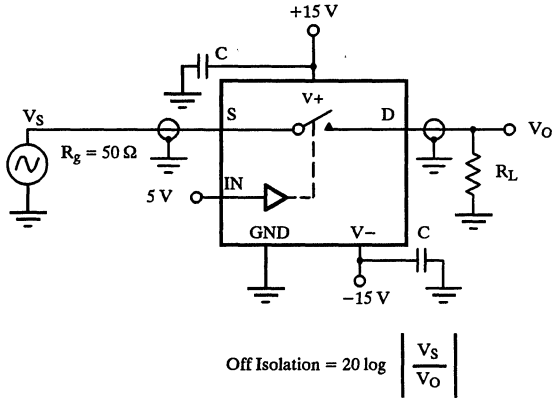


Figure 4. Off Isolation

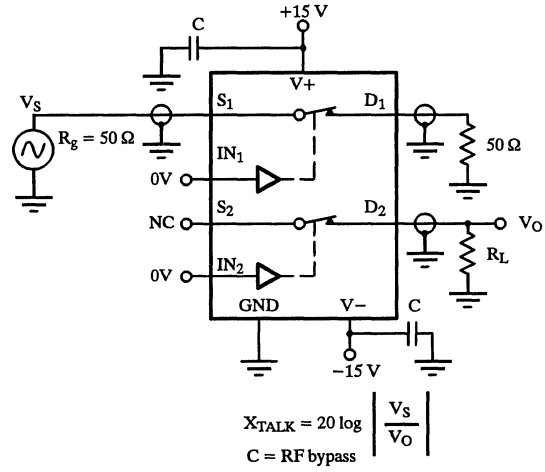


Figure 5. Channel-to-Channel Crosstalk

Monolithic Quad SPST CMOS Analog Switches

Features

- ± 15-V Input Range
- Low Off Leakage—$I_{D(on)}$: 0.1 nA
- Low On-Resistance—$r_{DS(on)}$: 115 Ω
- 44-V Maximum Supply Ratings
- TTL and CMOS Compatible

Benefits

- Wide Input Range
- Low Distortion Switching
- Can Be Driven from Comparators or Op Amps Without Limiting Resistors

Applications

- Disk Drives
- Radar Systems
- Communications Systems
- Sample-and-Hold

Description

The DG201A and DG202 are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. When combining a low on-resistance and a wide signal range (± 15 V) with low charge-transfer these devices are well suited for industrial and military applications.

Built on Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch conducts equally well in both directions when on. When off these switches will block up to 30 V peak-to-peak and have a 44-V absolute maximum power supply rating.

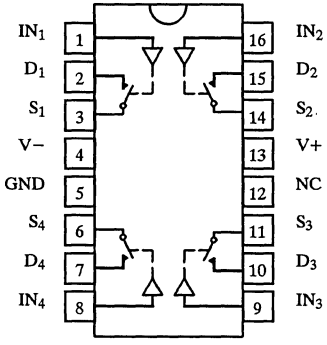
These two devices are differentiated by the type of switch actions (See Truth Table).

The DG201B/DG202B upgrades are recommended for new designs.

Functional Block Diagram and Pin Configuration

DG201A

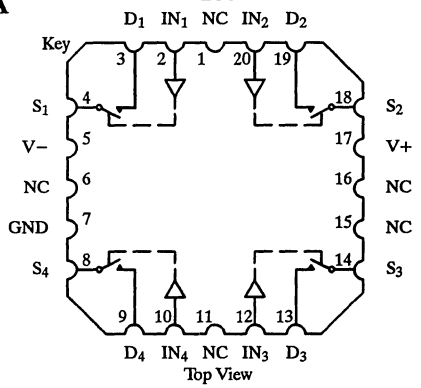
Dual-In-Line and SOIC



Top View

DG201A

LCC



Top View

Ordering Information – DG201A/202

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG201ACJ
		DG202CJ
−25 to 85°C	16-Pin CerDIP	DG201ABK
−40 to 85°C	16-Pin Narrow SOIC	DG201ADY
−55 to 125°C	16-Pin CerDIP	DG201AAK
		DG201AAK/883, JM38510/12302BEA
		7705301EA
		DG202AK
		DG202AK/883
	16-Pin Sidebraze	JM38510/12302BEC
		7705301EC
	LCC-20	DG201AAZ/883, 77053012A

Truth Table

Logic	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for DG201A Logic "1" Input

Absolute Maximum Ratings

Voltages Referenced to V−

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 20 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (K, Z Suffix) ..... −65 to 150°C
(J, Y Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin SOIC[d] ..... 640 mW
16-Pin CerDIP and Sidebraze[e] ..... 900 mW
LCC-20[f] ..... 750 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C
f. Derate 10 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix Min[d]	B, C, D Suffix Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room	115		175		175	Ω
			Full			250		250	
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.02	−1 −100	1 100	−5 −100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	±0.02	−1 −100	1 100	−5 −100	5 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room Full	±0.15	−1 −200	1 200	−5 −200	5 200	
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4 V	Room Full	−0.0004	−1 −1		−1 −10		µA
		V_{IN} = 15 V	Room Full	0.003		1 10		1 10	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	−0.0004	−1 −10		−1 −10		
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Switching Time Test Circuit	Room	480		600		600	ns
Turn-Off Time	t_{OFF}		Room	370		450		450	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room	20					pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel On Capacitance	$C_{D(on)}$ + $C_{S(on)}$	V_D = V_S = 0 V, V_{IN} = 0 V f = 1 MHz	Room	16					
Off Isolation	OIRR	V_{IN} = 5 V, R_L = 75 Ω V_S = 2 V, f = 100 kHz	Room	70					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	90					

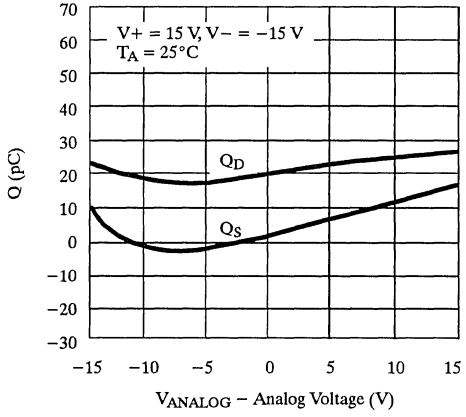
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix Min[d]	B, C, D Suffix Max[d]	Unit
Power Supply									
Positive Supply Current	I+	All Channels On or Off	Room	0.9		2		2	mA
Negative Supply Current	I−		Room	−0.3	−1		−1		

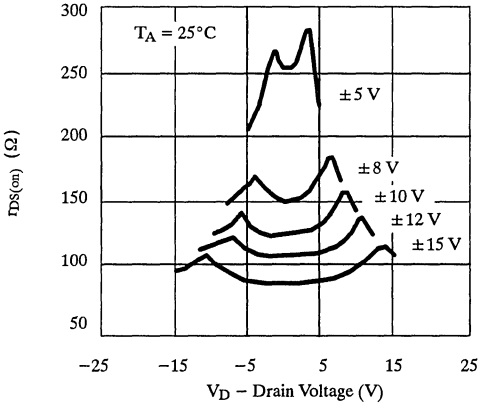
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

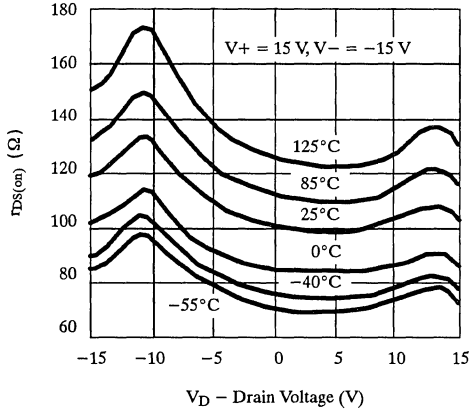
Charge Injection vs. Analog Voltage



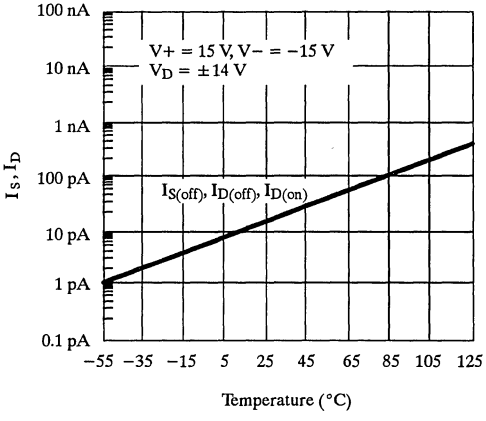
$r_{DS(on)}$ vs, V_D and Power Supply Voltage



$r_{DS(on)}$ vs. V_D and Temperature

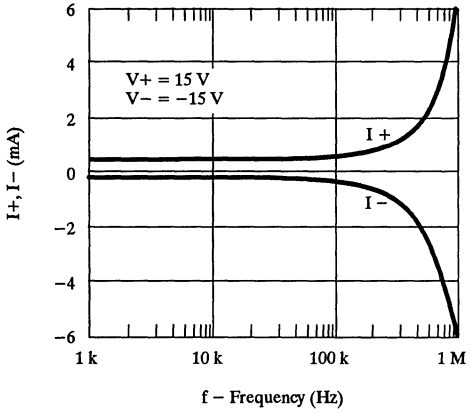


Leakage vs. Temperature

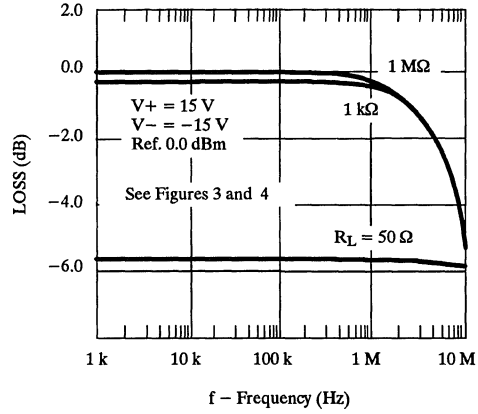


Typical Characteristics (Cont'd)

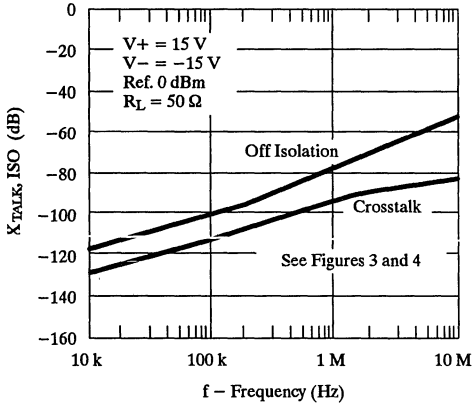
Supply Current vs. Switching Frequency



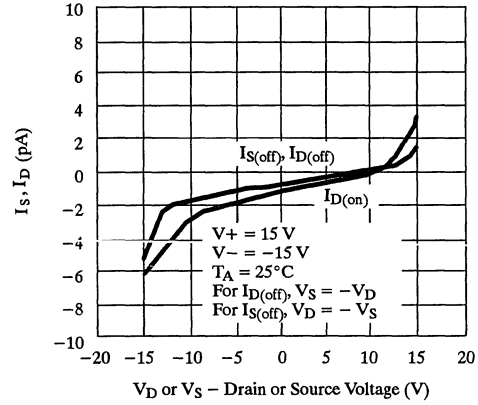
Insertion Loss vs. Frequency



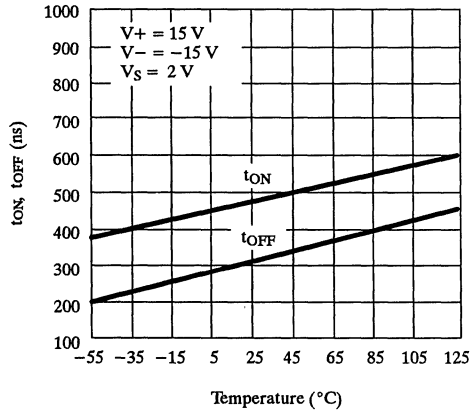
Crosstalk and Off Isolation vs. Frequency



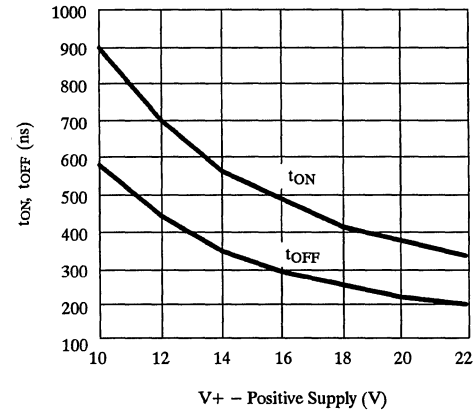
Leakage Current vs. Analog Voltage



Switching Time vs. Temperature



Switching Time vs. Power Supply Voltage



Schematic Diagram (Typical Channel)

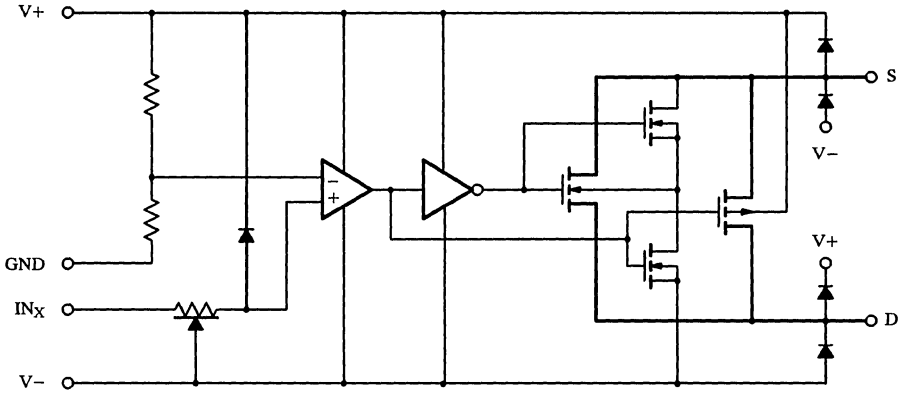


Figure 1.

Test Circuits

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

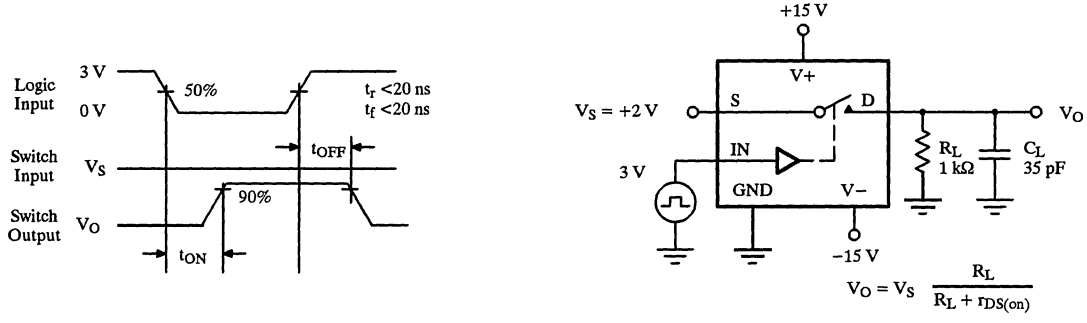


Figure 2. Switching Time

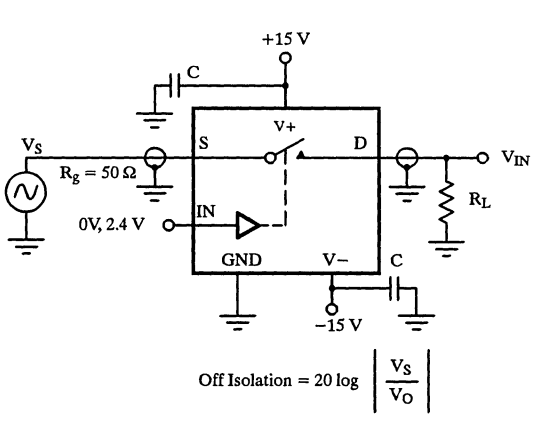


Figure 3. Off Isolation

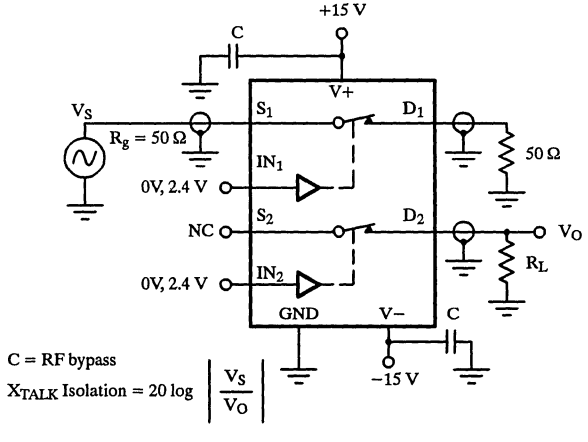
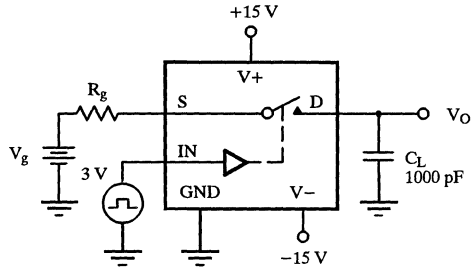
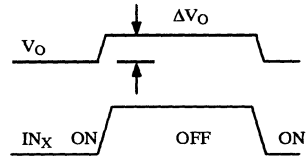


Figure 4. Channel-to-Channel Crosstalk

Test Circuits (Cont'd)





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$

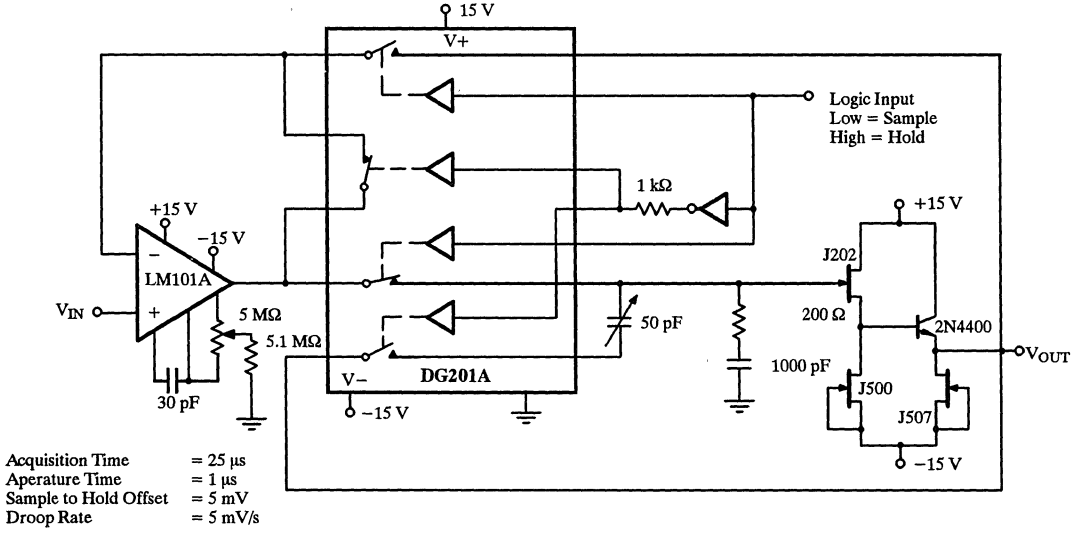
Figure 5. Charge Injection

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	−15	2.4/0.8	−15 to 15
10	−12	2.4/0.8	−12 to 12
12	−10	2.2/0.6	−10 to 10
8[b]	−8	2.0/0.5	−8 to 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

Applications



Acquisition Time = 25 µs
Aperature Time = 1 µs
Sample to Hold Offset = 5 mV
Droop Rate = 5 mV/s

Figure 6. Sample-and-Hold

Applications (Cont'd)

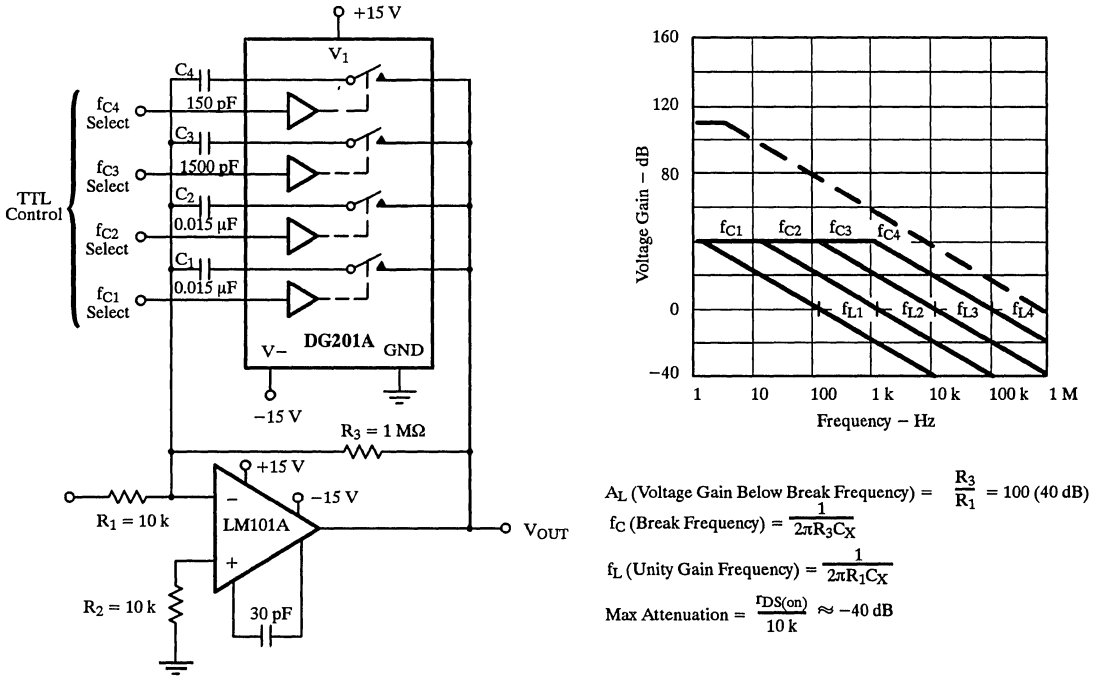


Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

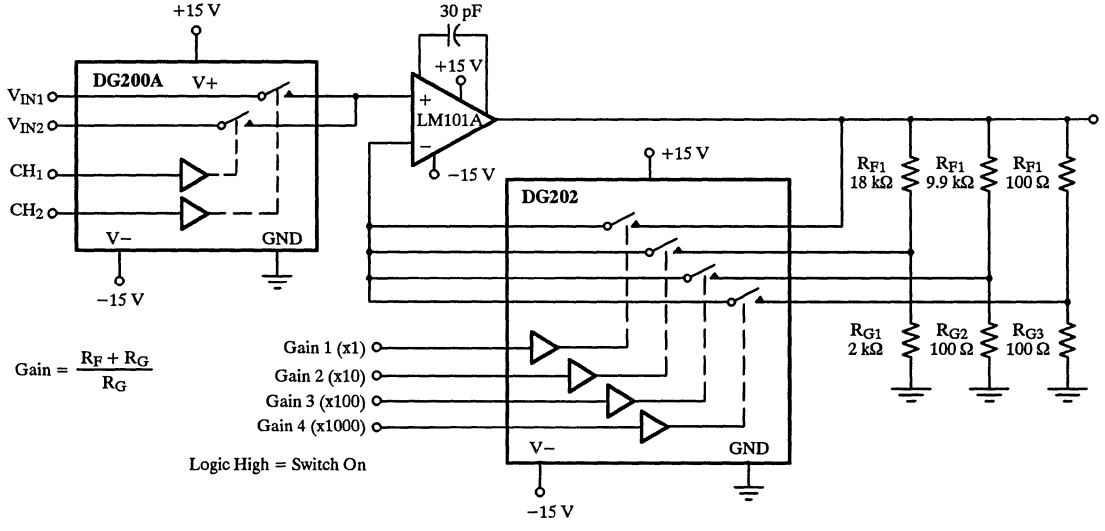


Figure 8. A Precision Amplifier with Digitally Programable Input and Gains

Siliconix
A Member of the TEMIC Group

Improved Quad CMOS Analog Switches

Features

- ±22-V Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance—$r_{DS(on)}$: 45 Ω
- Low Leakage—$I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching—t_{ON}: 120 ns
- Low Glitching—Q: 1 pC

Benefits

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG201A/202

Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

Description

The DG201B/202B analog switches are highly improved versions of the industry-standard DG201A/202. These devices are fabricated in Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG201B and DG202B can handle up to ±22-V input signals, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

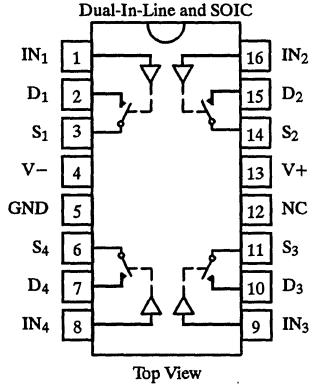
All devices feature true bi-directional performance in the on condition, and will block signals to the supply voltages in the off condition.

The DG201B is a normally closed switch and the DG202B is a normally open switch. (See Truth Table.)

Functional Block Diagram and Pin Configuration

DG201B

Dual-In-Line and SOIC



Top View

Truth Table

Logic	DG201B	DG202B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG201BDJ
		DG202BDJ
	16-Pin CerDIP	DG201BDK
		DG202BDK
	16-Pin Narrow SOIC	DG201BDY
		DG202BDY
−55 to 125°C	16-Pin CerDIP	DG201BAK
		DG201BAK/883
		DG202BAK
		DG202BAK/883

P-32167—Rev. A (11/15/93)

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 30 mA, whichever occurs first
Current, Any Terminal ..... 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Storage Temperature (AK, DK Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 640 mW
16-Pin CerDIP[e] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room Full	45		85 100		85 100	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room	2					
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.01	−0.5 −20	0.5 20	−0.5 −5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	±0.01	−0.5 −20	0.5 20	−0.5 −5	0.5 5	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room Full	±0.02	−0.5 −40	0.5 40	−0.5 −10	0.5 10	
Digital Control									
Input Voltage High	V_{INH}		Full		2.4		2.4		V
Input Voltage Low	V_{INL}		Full			0.8		0.8	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full		−1	1	−1	1	µA
Input Capacitance	C_{IN}		Room	5					pF
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = 2 V See Switching Time Test Circuit	Room Full	120		300		300	ns
Turn-Off Time	t_{OFF}		Room Full	65		200		200	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room	1					pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, f = 1 MHz	Room	16					
Off Isolation	OIRR	C_L = 15 pF, R_L = 50 Ω V_S = 1 V_{RMS}, f = 100 kHz	Room	90					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	95					

1

Specifications[a]

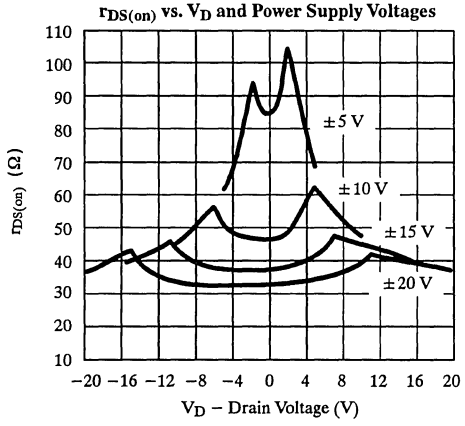
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Power Supply									
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			50 100		50 100	µA
Negative Supply Current	I−		Room Full		−1 −5		−1 −5		
Power Supply Range for Continuous Operation	V_{OP}		Full		±4.5	±22	±4.5	±22	V

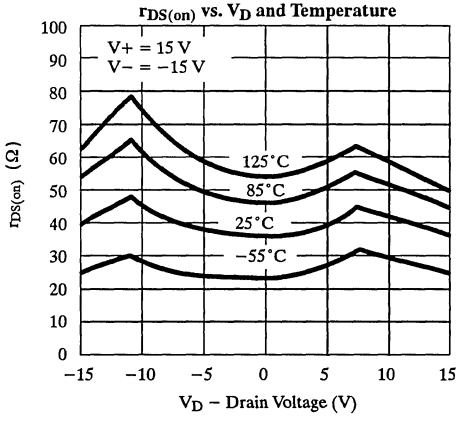
Specifications[a] for Single Supply

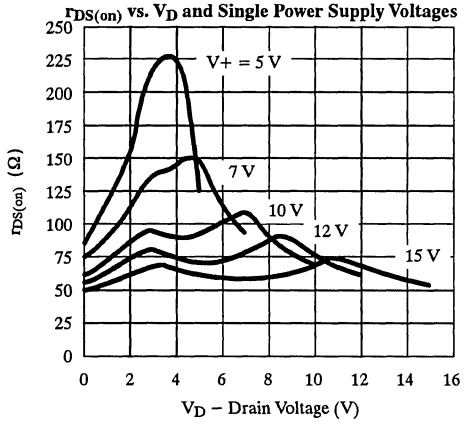
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 8 V, I_S = 1 mA	Room Full	90		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = 8 V See Switching Time Test Circuit	Room	120		300		300	ns
Turn-Off Time	t_{OFF}		Room	60		200		200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	4					pC
Power Supply									
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			50 100		50 100	µA
Negative Supply Current	I−		Room Full		−1 −5		−1 −5		
Power Supply Range for Continuous Operation	V_{OP}		Full		+4.5	+25	+4.5	+25	V

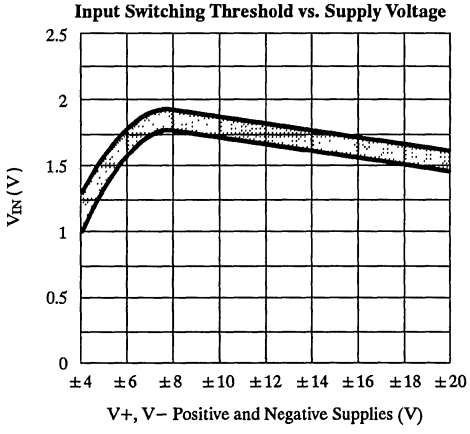
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

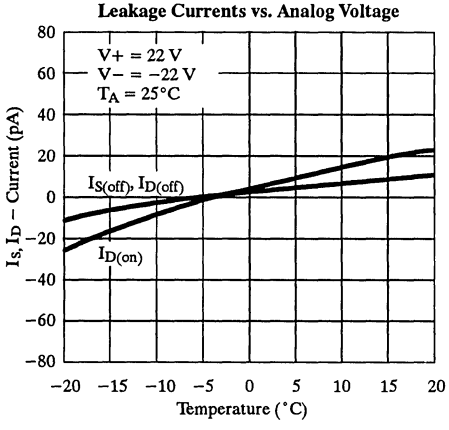
Typical Characteristics

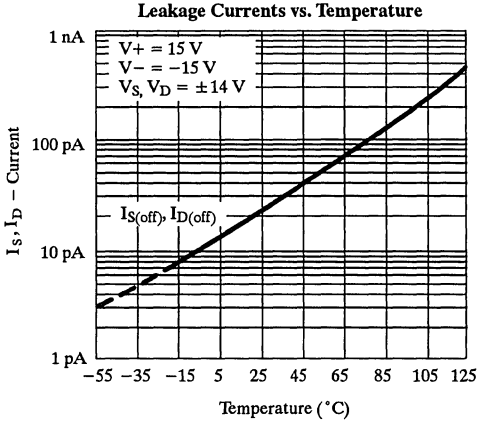












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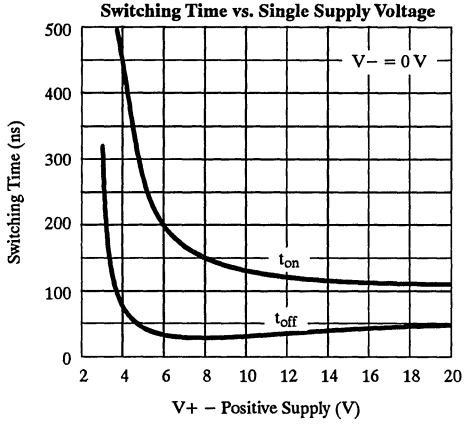
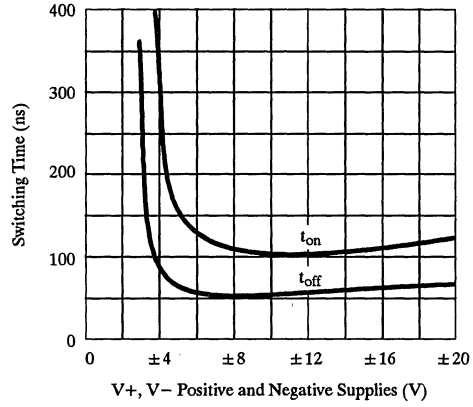
Typical Characteristics (Cont'd)

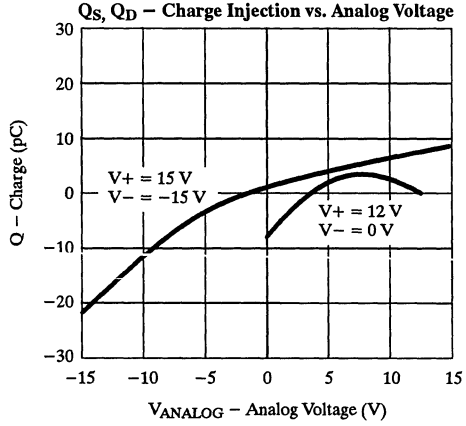
Switching Time vs. Single Supply Voltage



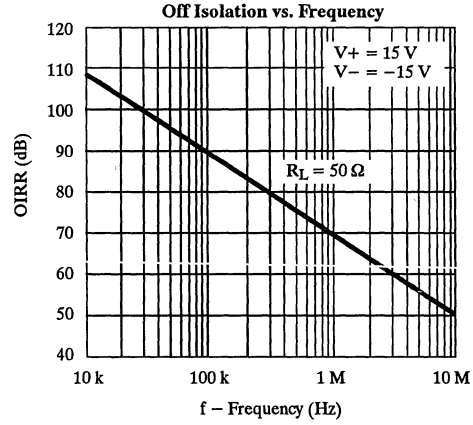
Switching Time vs. Power Supply Voltage



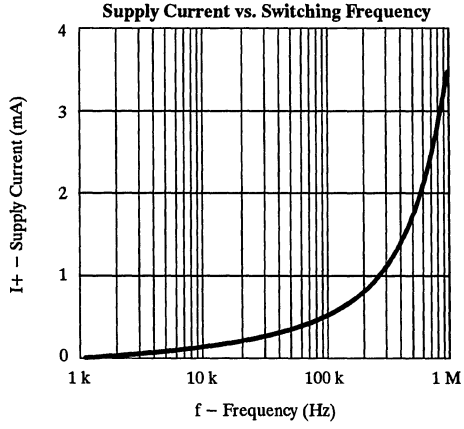
Q_S, Q_D − Charge Injection vs. Analog Voltage



Off Isolation vs. Frequency



Supply Current vs. Switching Frequency



Schematic Diagram (Typical Channel)

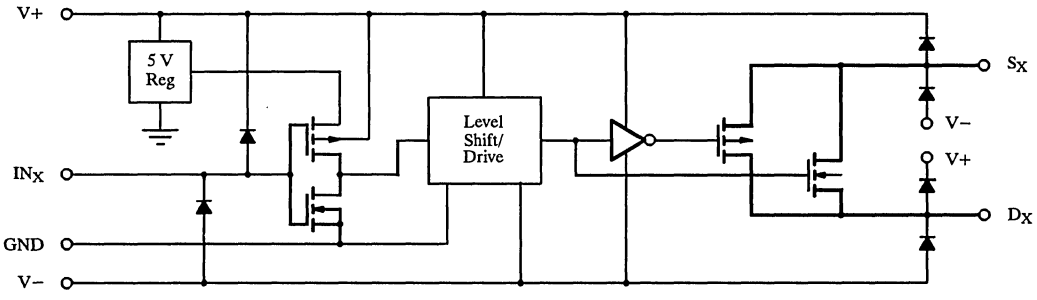
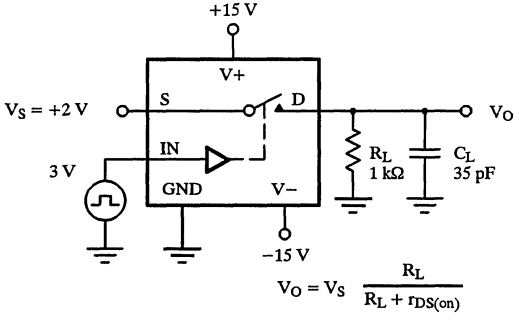


Figure 1.

Test Circuits



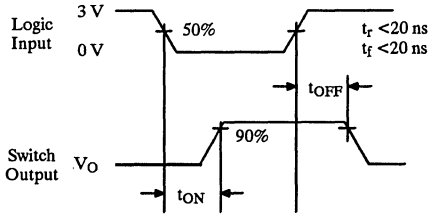


Figure 2. Switching Time

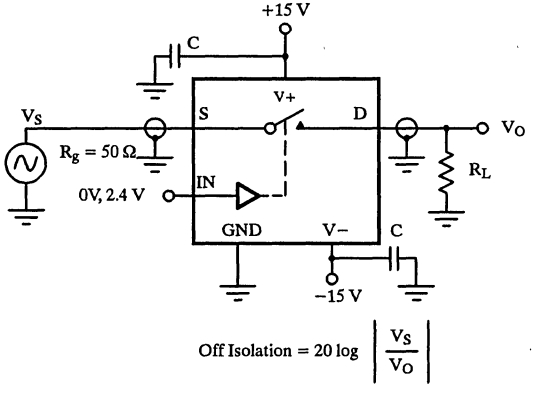


Figure 3. Off Isolation

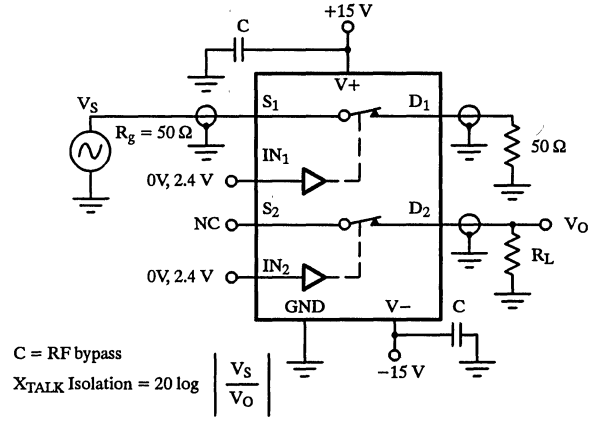


Figure 4. Channel-to-Channel Crosstalk

1

Test Circuits (Cont'd)

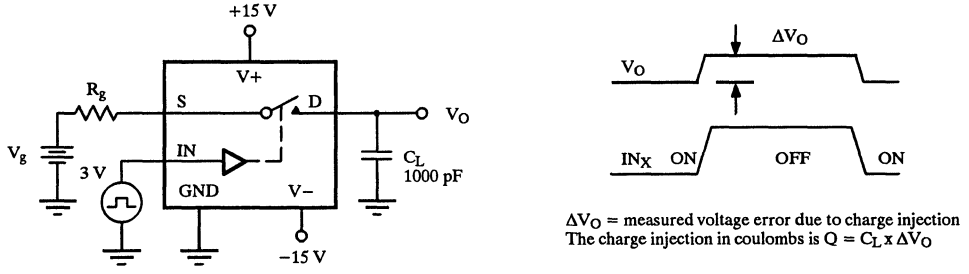


Figure 5. Charge Injection

Applications

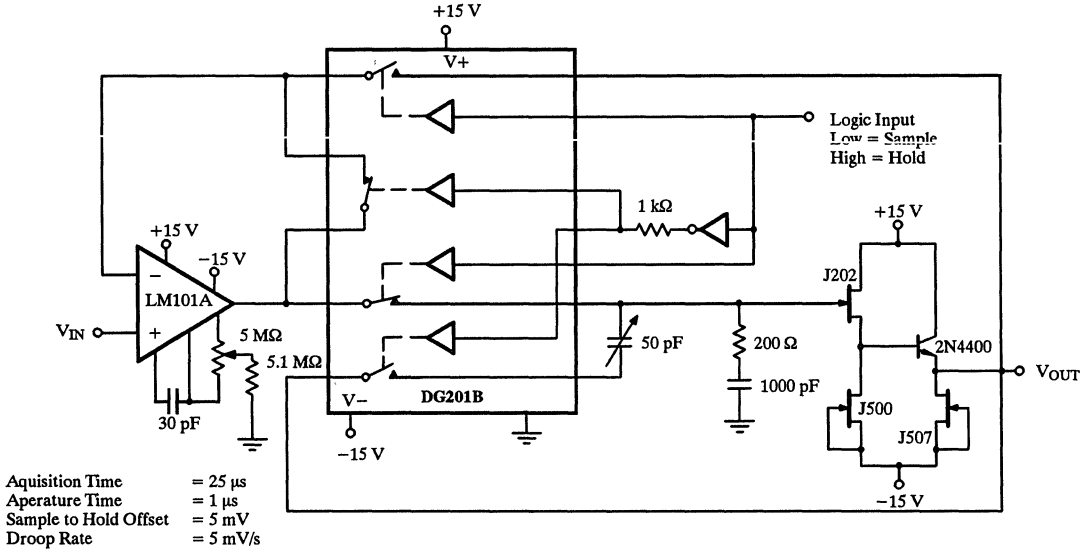


Figure 6. Sample-and-Hold

Applications (Cont'd)

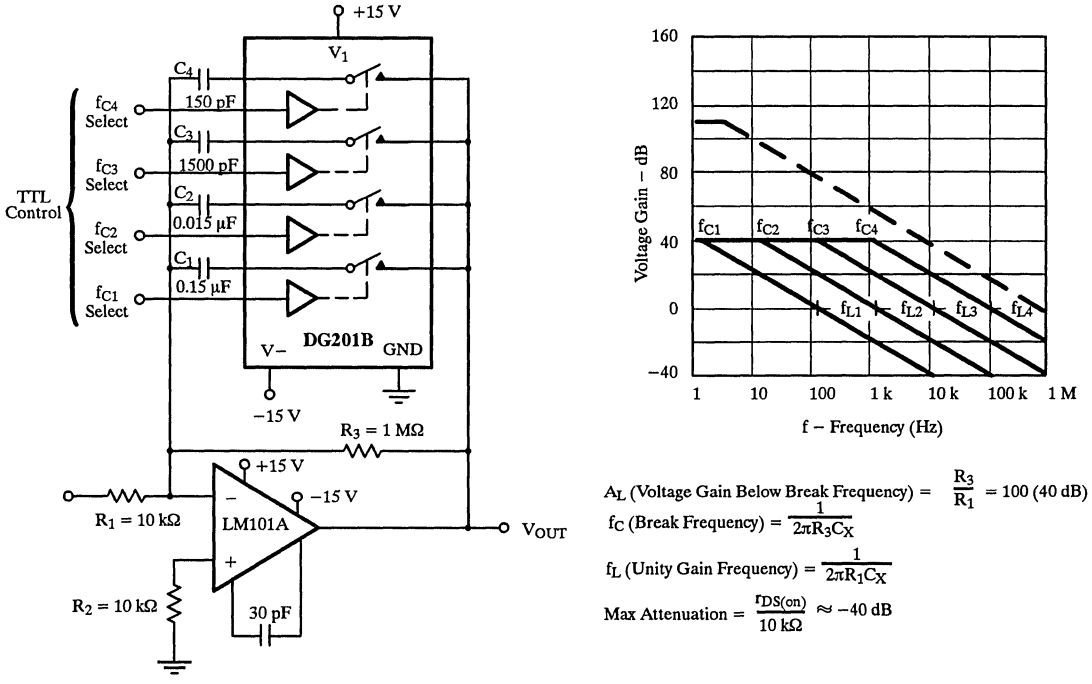


Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

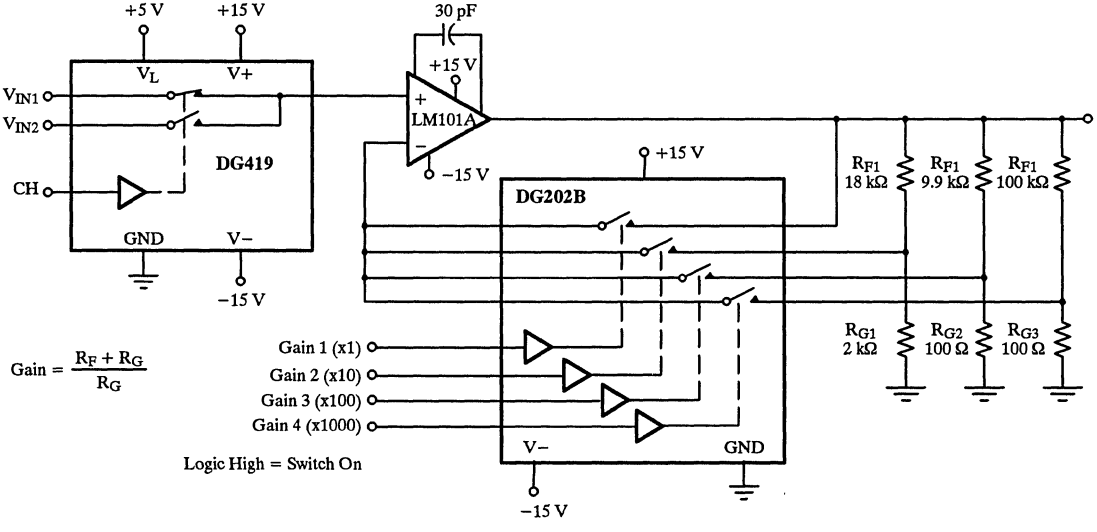


Figure 8. A Precision Amplifier with Digitally Programable Input and Gains

DG201HS

Siliconix
A Member of the TEMIC Group

High-Speed Quad SPST CMOS Analog Switch

Features

- Fast Switching—t_{ON}: 38 ns
- Low On-Resistance: 25 Ω
- Low Leakage: 100 pA
- Low Charge Injection
- TTL/CMOS Logic Compatible
- Single Supply Compatibility
- High Current Rating: −30 mA

Benefits

- Faster Throughput
- Higher Accuracy
- Reduced Pedestal Error
- Upgrades Existing Designs
- Simple Interfacing
- Replaces HI201HS, ADG201HS

Applications

- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Integrator Reset Circuits
- Choppers
- Gain Switching
- Avionics

Description

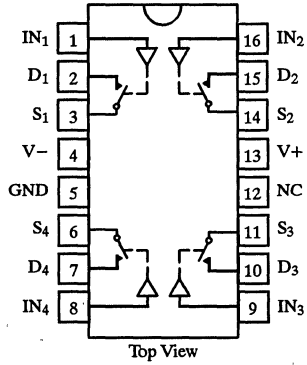
The DG201HS is an improved monolithic device containing four independent analog switches. It is designed to provide high speed, low error switching of analog signals. Combining low on-resistance (25 Ω) with high speed (t_{ON}: 38 ns), the DG201HS is ideally suited for high speed data acquisition requirements.

To achieve high voltage ratings and superior switching performance, the DG201HS is built on a proprietary high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply values, when off.

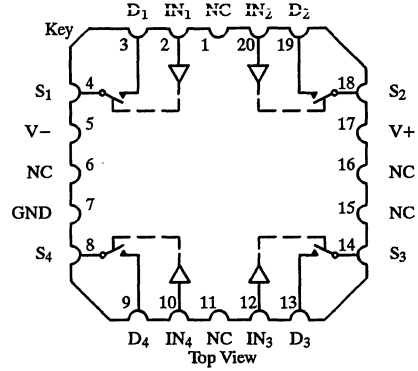
Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

LCC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG201HSDJ
	16-Pin Narrow SOIC	DG201HSDY
−55 to 125°C	16-Pin CerDIP	DG201HSAK/883
	LCC-20	DG201HSAZ/883

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

P-32167—Rev. A (11/15/93)

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −4 V to (V+) +4 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature (A Suffix) ..... −65 to 150°C
(D Suffix) ..... −65 to 125°C
Power Dissipation (Package)b
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin CerDIP[d] ..... 900 mW
16−Pin Narrow Body SOIC[e] ..... 600 mW
LCC-20[d] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 12 mW/°C above 75°C.
e. Derate 7.6 mW/°C above 75°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{IN} = 3 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		V−	V+	V−	V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±8.5 V V+ = 13.5 V, V− = −13.5 V	Room Full	25		50 75		50 75	Ω
$r_{DS(on)}$ Match			Room	3					%
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V− = −16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Full	0.1	−1 −60	1 60	−1 −20	1 20	nA
	$I_{D(off)}$		Room Full	0.1	−1 −60	1 60	−1 −20	1 20	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V V_S = V_D = ∓15.5 V	Room Full	0.1	−1 −60	1 60	−1 −20	1 20	
Digital Control									
Input, High Voltage	V_{INH}		Full		2.4		2.4		V
Input, Low Voltage	V_{INL}		Full			0.8		0.8	
Input Capacitance	C_{in}		Full	5					pF
Input Current	I_{INL} or I_{INH}	V_{IN} under test = 0.8 V, 3 V	Full		−1	1	−1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ±10 V, V_{INH} = 3 V See Figure 3	Room Full	38		50 70		50 70	ns
Turn-Off Time	t_{OFF1}		Room Full	30		50 70		50 70	
	t_{OFF2}		Room	150					
Output Settling Time to 0.1%	t_s		Room	180					
Charge Injection	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	−5					pC
OFF Isloation	OIRR	R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	85					dB

1

Specifications[a] (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 3 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Crosstalk (Channel-to-Channel)	X_{TALK}	Any Other Channel Switches R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	100					dB
Source Off Capacitance	$C_{S(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	30					
Drain-to-Source Capacitance	$C_{DS(off)}$		Room	0.5					
Power Supplies									
Positive Supply Current	I+	V+ = 15 V, V− = −15 V V_{IN} = 0 or 5 V	Room Full	4.5		10		10	mA
Negative Supply Current	I−		Room Full	3.5	−6		−6		
Power Consumption[e]	P_C		Full			240		240	mW

Specifications[a] for Single Supply

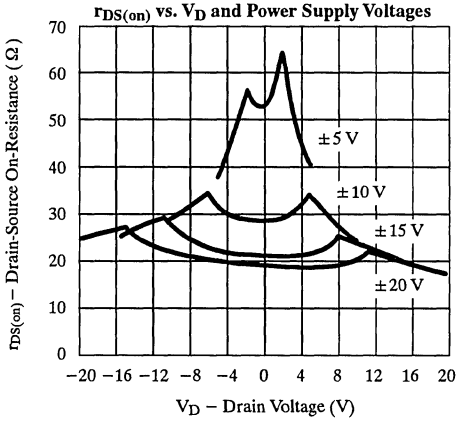
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 10.8 V to 16.5 V V− = GND = 0 V, V_{IN} = 3 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	V+	0	V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 8.5 V V+ = 10.8 V	Room Full	65		90 120		90 120	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V_S = 0.5 V, 10 V V_D = 10 V, 0.5 V	Room Full	0.1	−1 −60	1 60	−1 −20	1 20	nA
	$I_{D(off)}$		Room Full	0.1	−1 −60	1 60	−1 −20	1 20	
Channel On Leakage Current	$I_{D(on)}$ + $I_{S(on)}$	V+ = 16.5 V, V_D = 0.5 V, 10 V	Room Full	0.1	−1 −60	1 60	−1 −20	1 20	
Digital Control									
Input, High Voltage	V_{INH}		Full		2.4		2.4		V
Input, Low Voltage	V_{INL}		Full			0.8		0.8	
Input Capacitance	C_{in}		Full	5					pF
Input Current	I_{INL} or I_{INH}	V+ = 16.5 V V_{IN} under test = 0.8 V, 3 V	Full		−1	1	−1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 2 V V= = 10.8 V, See Figure 3	Room Full			50 70		50 70	ns
Turn-Off Time	t_{OFF1}		Room Full			50 70		50 70	
	t_{OFF2}		Room	150					

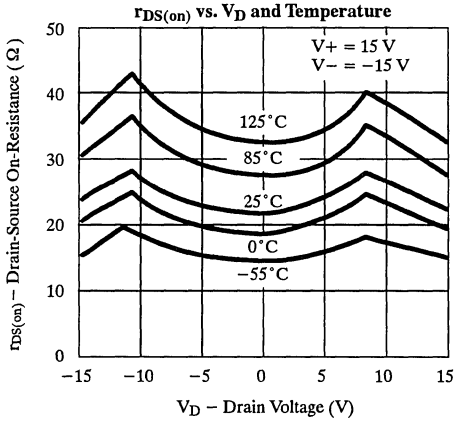
Specifications[a] for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 10.8 V to 16.5 V V− = GND = 0 V, V_{IN} = 3 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Output Settling Time to 0.1%	t_s		Room	180					ns
Charge Injection	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	10					pC
Off Isloation	OIRR	R_L = 1 kΩ, C_L = 10 pF f = 100 kHz	Room	85					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	Any Other Channel Switches R_L = 1 kΩ, C_L = 10 pF, f = 100 kHz	Room	100					dB
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz	Room	10					pF
Drain Off Capacitance	$C_{D(off)}$	f = 1 MHz	Room	10					pF
Channel On Capacitance	$C_{D(on)}$	V_{ANALOG} = 0 V	Room	30					pF
Power Supplies									
Positive Supply Current	I+	V+ = 15 V, V_{IN} = 0 or 5 V	Full			10		10	mA
Power Consumption[e]	P_C	V+ = 15 V, V_{IN} = 0 or 5 V	Full			150		150	mW

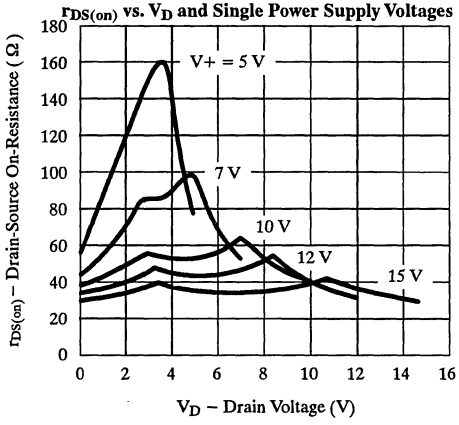
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

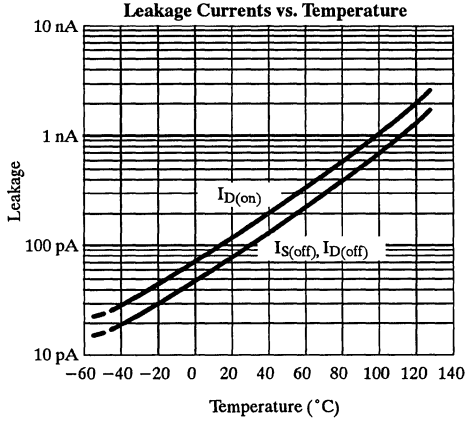
Typical Characteristics

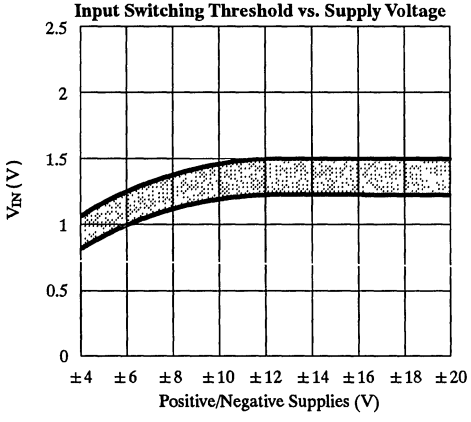


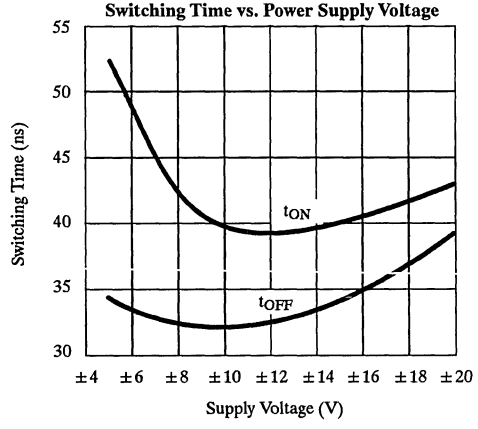


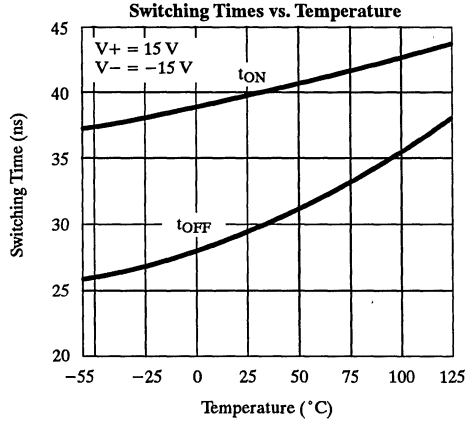
Typical Characteristics (Cont'd)

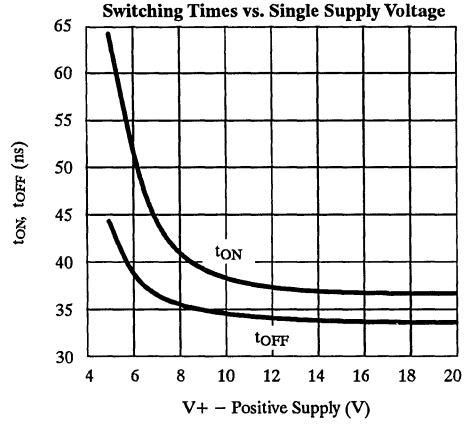




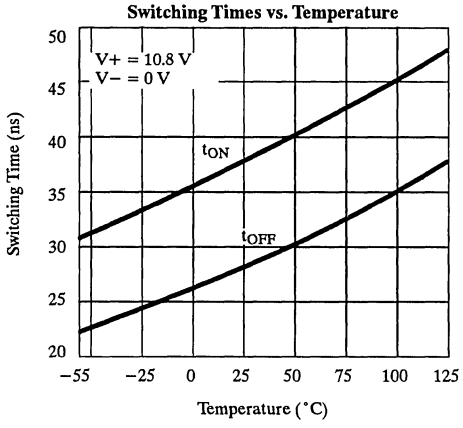


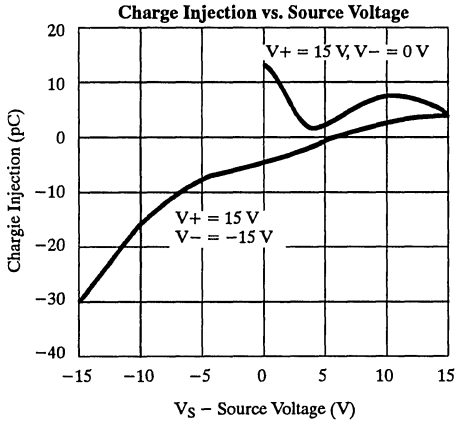


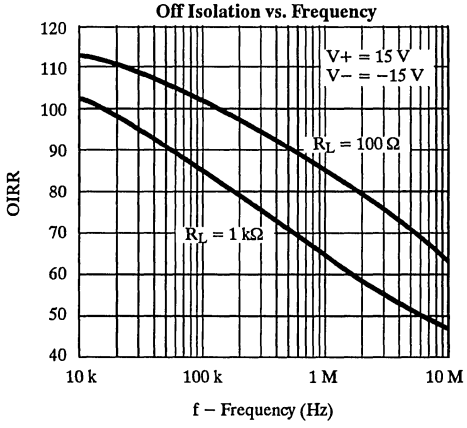




Typical Characteristics (Cont'd)







Test Circuits

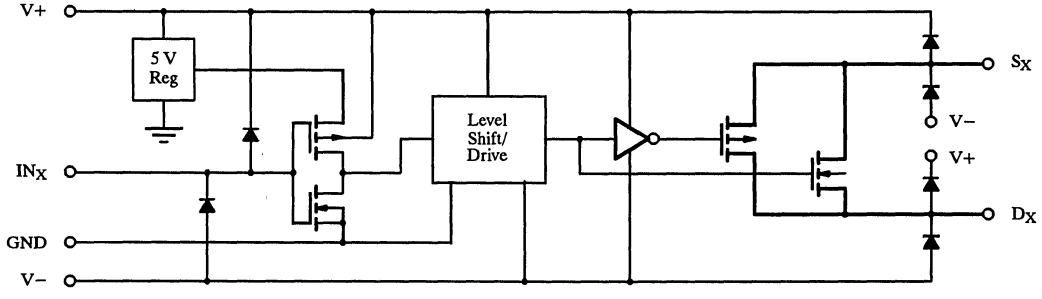
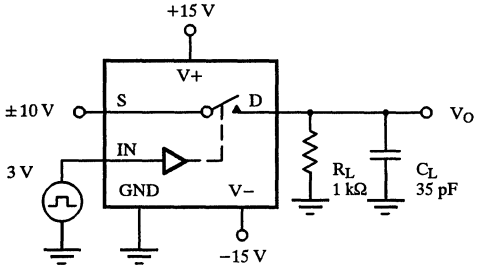
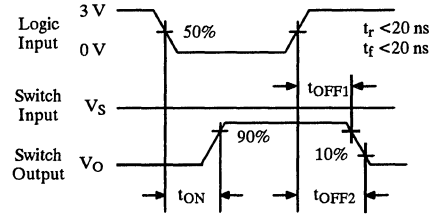


Figure 1.

Test Circuits (Cont'd)

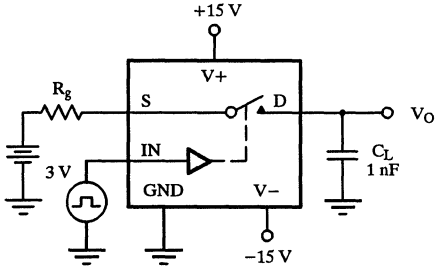


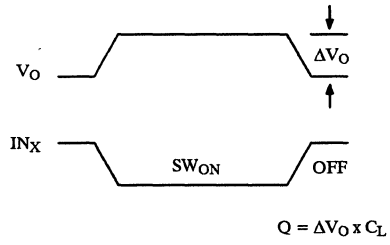


C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

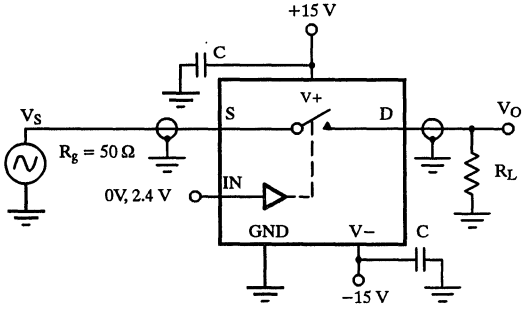
Figure 2. Switching Time





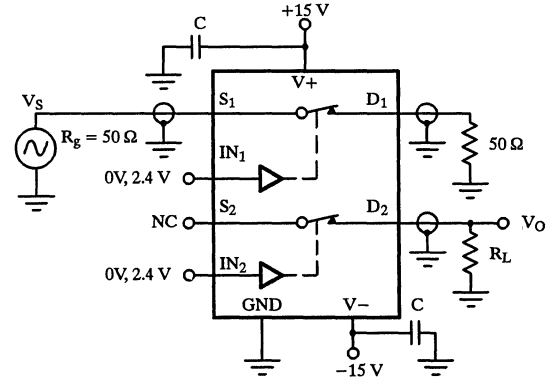
$Q = \Delta V_O \times C_L$

Figure 3. Charge Injection



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

Figure 4. Off Isolation



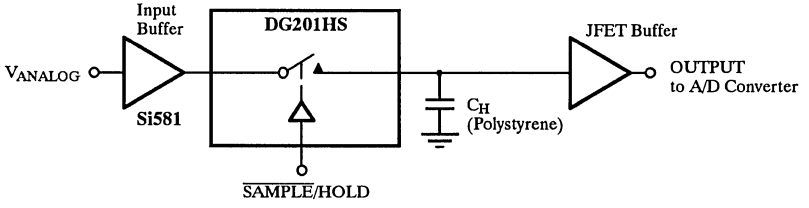
$$X_{TALK}\ \text{Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 5. Crosstalk

Applications

A high-speed, low-glitch analog switch such as Siliconix's DG201HS improves the accuracy and shortens the acquisition and settling times of a sample-and-hold circuit.



Low Cost Monolithic Quad SPST CMOS Analog Switches

Features

- ± 15-V Analog Signal Range
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- On-Resistance—$r_{DS(on)}$: 115 Ω

Benefits

- Wide Signal Range
- Simple Logic Interface
- Reduced Power Consumption

Applications

- Disk Drives
- Test Equipment
- Communication Systems
- Sample-and-Holds

Description

The DG211 and DG212 are low cost quad single-pole single-throw analog switches for use in general purpose switching applications in communication, instrumentation and process control. These devices differ only in that the digital control logic is inverted (see Truth Table). The use of both p- and n-channel devices minimizes on-resistance variation over the analog signal range.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 40 V, both switches will handle ± 15-V input signals with ease, and have a continuous current rating of 20 mA. An epitaxial layer prevents latchup.

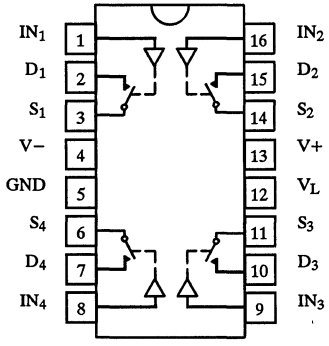
Both devices feature true bi-directional performance (with no offset voltage) in the on condition, and will block signals to 30 V peak-to-peak in the off condition.

For new designs we recommend the silicon-gate DG211A/212A upgrades.

Functional Block Diagram and Pin Configuration

DG211

Dual-In-Line and SOIC



Top View

Truth Table

Logic	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for DG211 Logic "1" Input

Ordering Information – DG211/212

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG211CJ
		DG212CJ
–40°C to 85°C	16-Pin Narrow SOIC	DG211DY
		DG212DY

Absolute Maximum Ratings

V+ to V− ..... 44 V
V_{IN} to GND[a] ..... V−, V+
V_L to GND ..... −0.3 V, 25 V
V_S or V_D to V+[a] ..... 0, −40 V
V_S or V_D to V−[a] ..... 0, 40 V
V+ to GND ..... 25 V
V− to GND ..... −25 V
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 600 mW

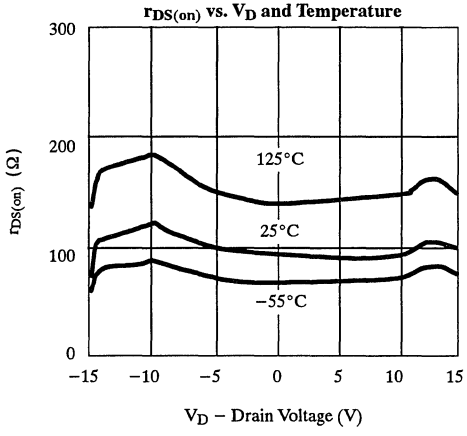
Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 7.6 mW/°C above 75°C

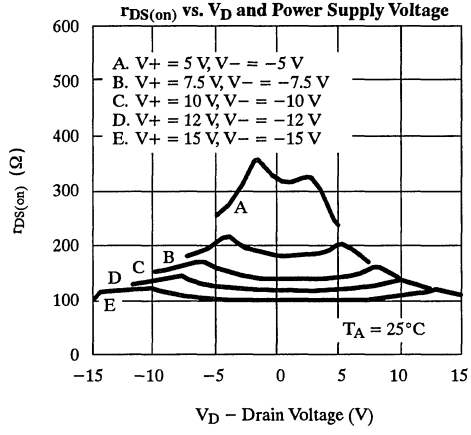
Specifications

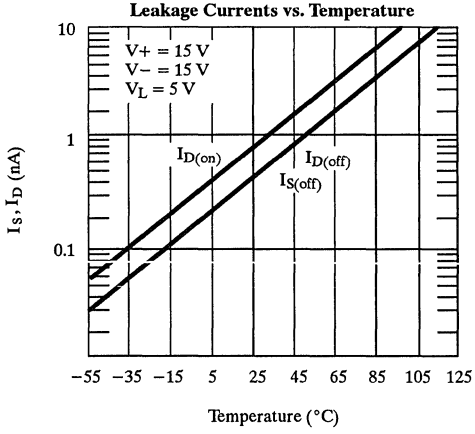
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	Limits Min[c]	Limits Typ[b]	Limits Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	−15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = 1 mA, V_D = ±10 V	Room		115	175	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room	−5	±0.02	5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room	−5	±0.02	5	nA
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±14 V	Room	−5	±0.15	5	nA
Digital Control							
Input Current—Input Voltage High	I_{INH}	V_{IN} = 2.4 V	Room	−1	−0.0004		µA
		V_{IN} = 15 V	Room		0.003	1	µA
Input Current—Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room	−1	−0.0004		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Switching Time Test Circuit, V_S = 2 V	Room		460	1000	ns
Turn-Off Time	t_{OFF1}	See Switching Time Test Circuit, V_S = 2 V	Room		360	500	ns
	t_{OFF2}	See Switching Time Test Circuit, V_S = 2 V	Room		450	450	ns
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room		5		pF
Channel On Capacitance	C_{ON}	V_D = V_S = 0 V, V_{IN} = 0 V, f = 1 MHz	Room		16		pF
Off Isolation	OIRR	V_{IN} = 5 V, R_L = 1 kΩ C_L = 15 pF, V_S = 1 V_{RMS}, f = 100 kHz	Room		70		dB
Channel-to-Channel Crosstalk	X_{TALK}	V_{IN} = 5 V, R_L = 1 kΩ C_L = 15 pF, V_S = 1 V_{RMS}, f = 100 kHz	Room		90		dB
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room		0.35	0.48	mA
Negative Supply Current	I−	V_{IN} = 0 or 5 V	Room		0.3	0.48	mA
Logic Supply Current	I_L	V_{IN} = 0 or 5 V	Room		0.5	1.2	mA

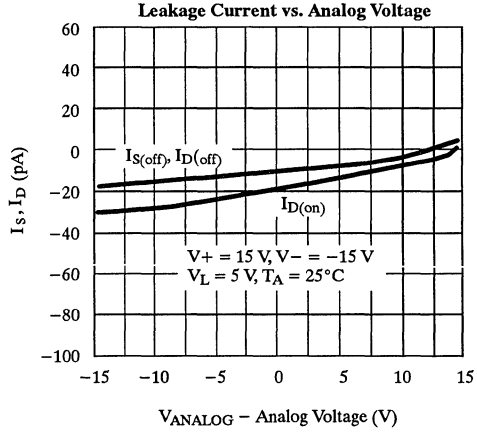
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

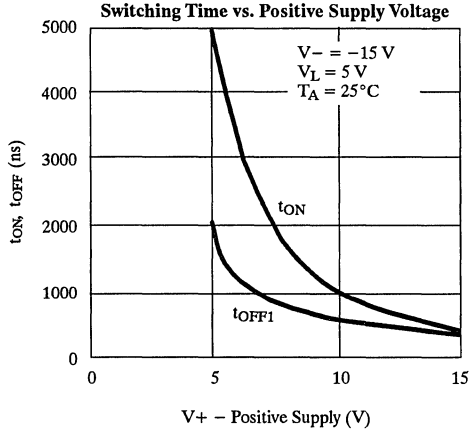
Typical Characteristics

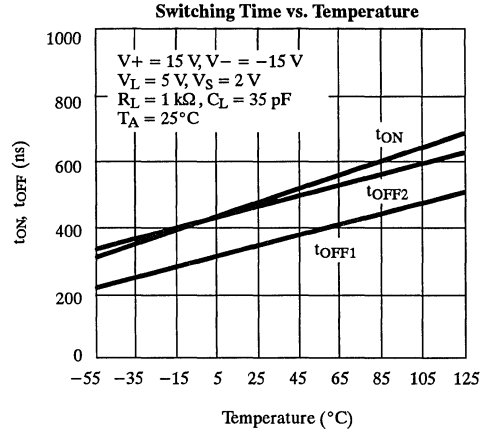






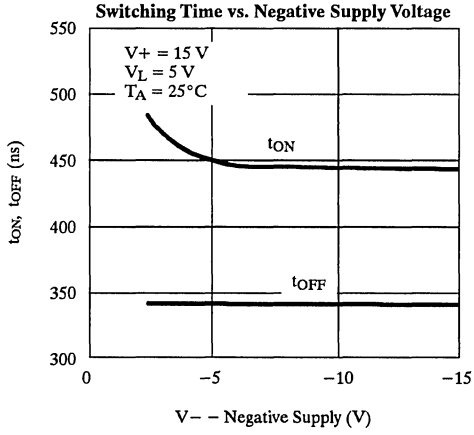




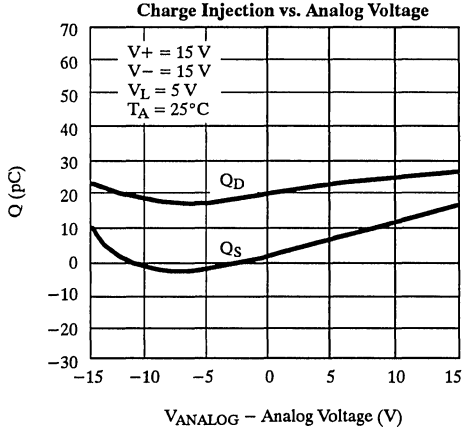


Typical Characteristics (Cont'd)

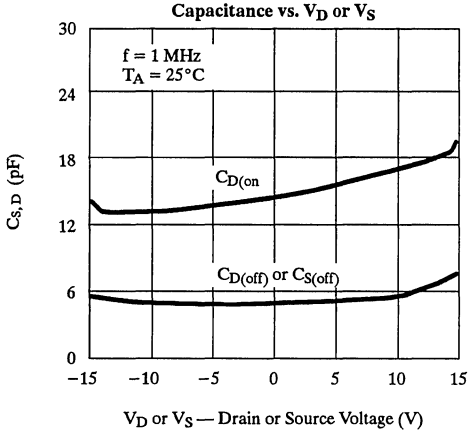
Switching Time vs. Negative Supply Voltage



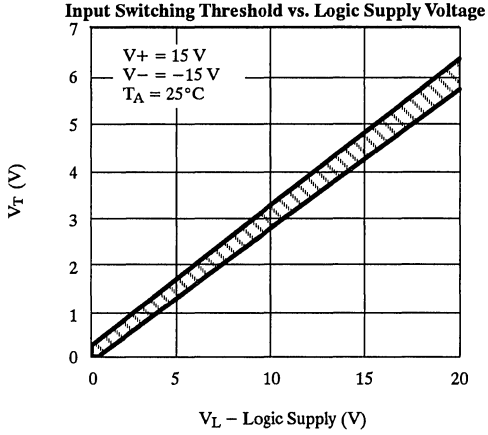
Charge Injection vs. Analog Voltage



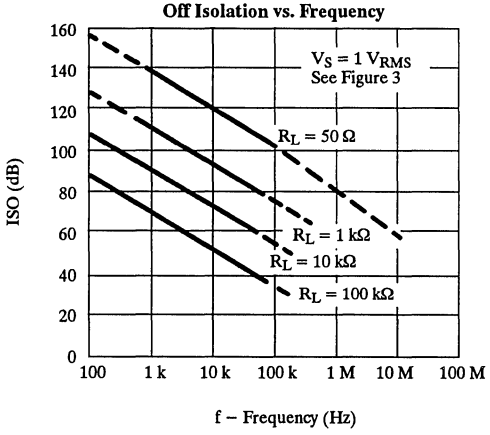
Capacitance vs. V_D or V_S



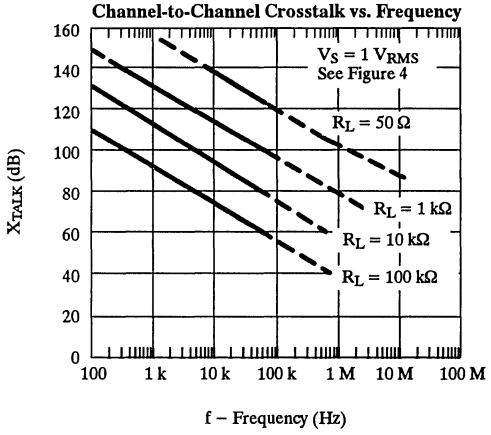
Input Switching Threshold vs. Logic Supply Voltage



Off Isolation vs. Frequency



Channel-to-Channel Crosstalk vs. Frequency



1

Schematic Diagram (Typical Channel)

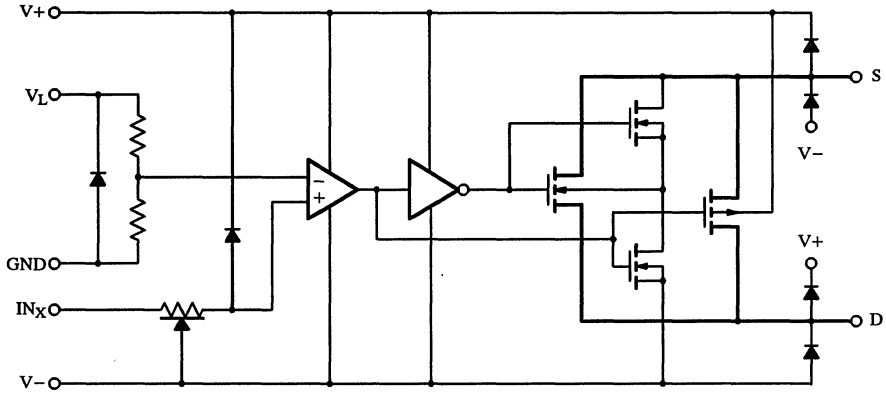
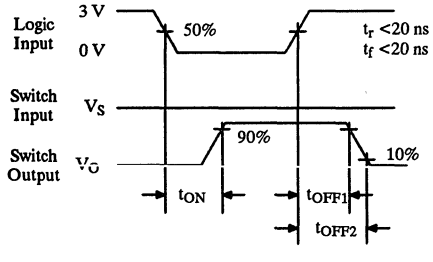


Figure 1.

Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



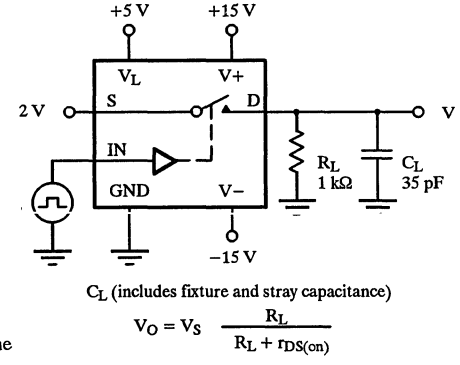


Figure 2. Switching Time

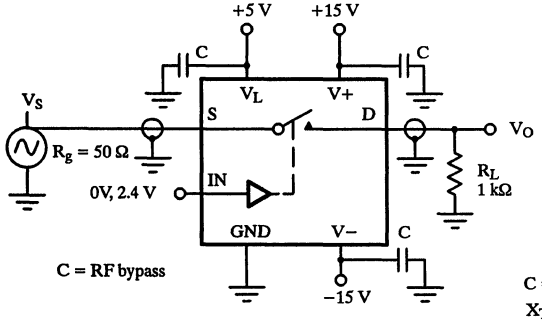


Figure 3. Off Isolation vs. Frequency

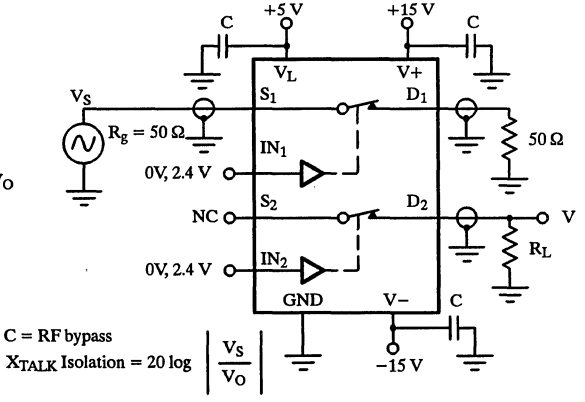


Figure 4. Crosstalk vs. Frequency

Applications Hints[a]

Some applications of the DG211 or DG212 will find the logic control inputs IN_X driven from the output of comparators or op-amps with nearly plus to minus 15-V transitions. In these applications the user can shift the input logic transition voltage from the normal 1.6 V of TTL to zero volts by connecting the V_L pin to the GND pin. In this mode of operation the input offset voltage between IN_X and V_L (= GND) measures less than ±500 mV.

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
20	−20	5	2.4/0.8	−20 to 20
15	−15	5	2.4/0.8	−15 to 15
12	−12	5	2.4/0.8	−12 to 12
10	−10	5	2.4/0.8	−10 to 10
8[b]	−8	5	2.4/0.8	−8 to 8
10	−10	10	5/2	−10 to 10

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

Applications

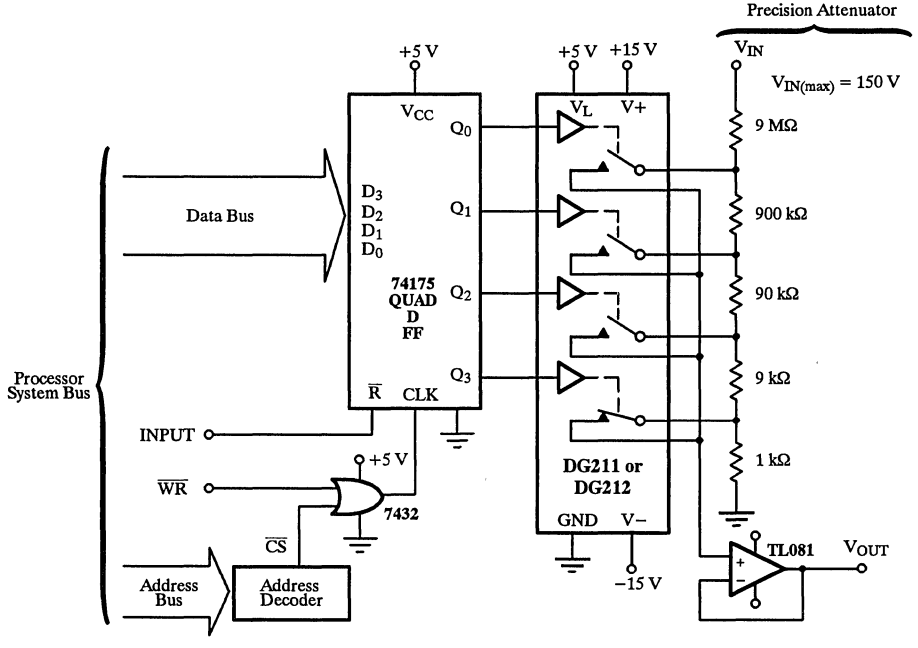


Figure 5. Microprocessor Controlled Analog Signal Attenuator

Applications (Cont'd)

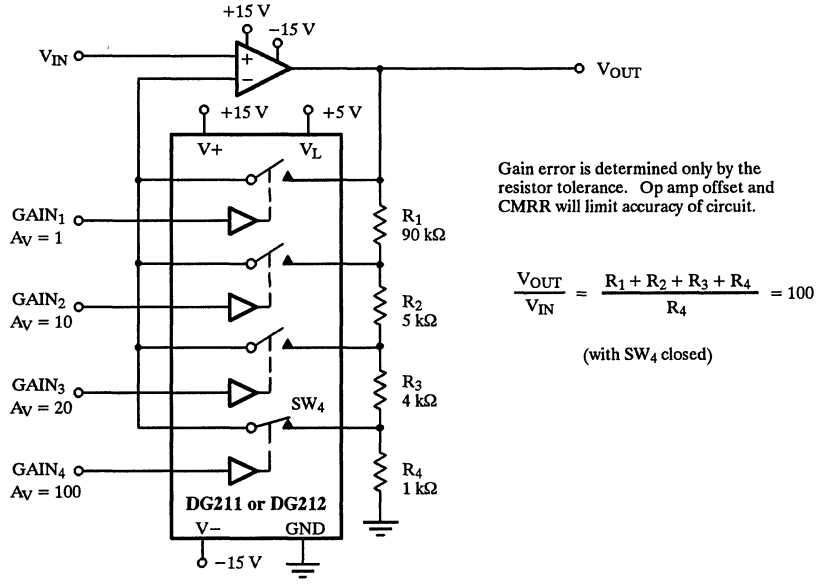
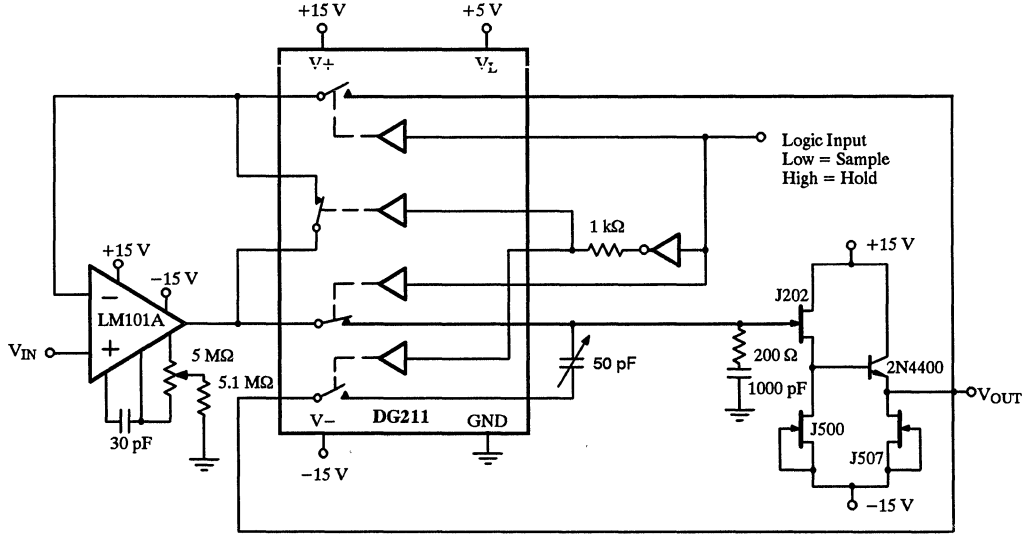


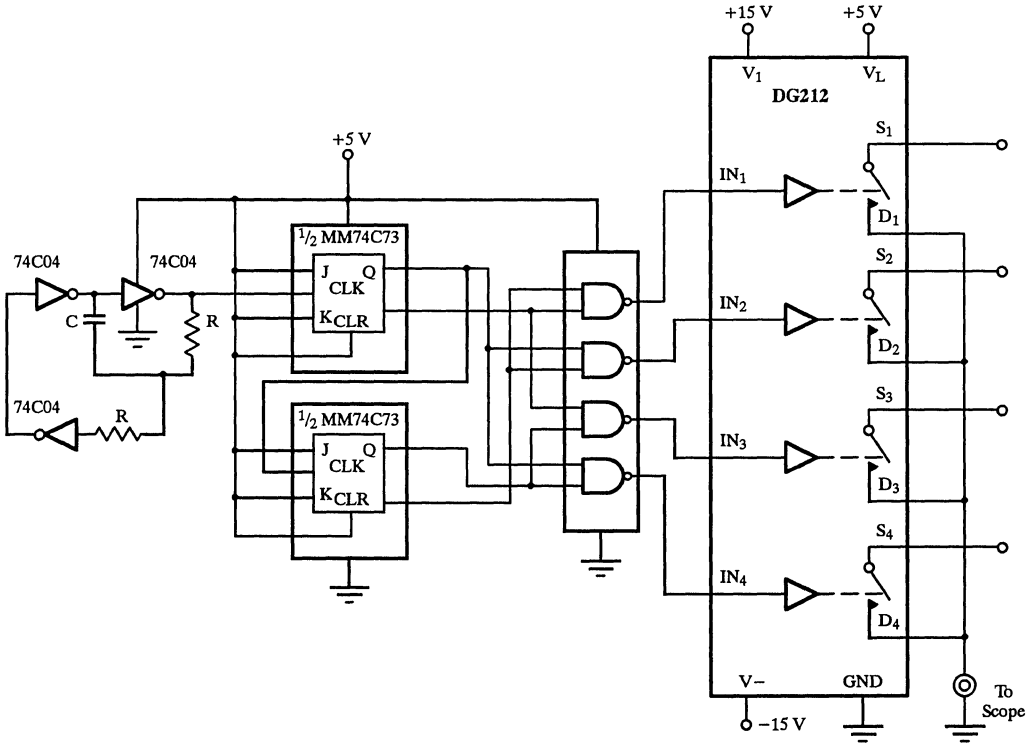
Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

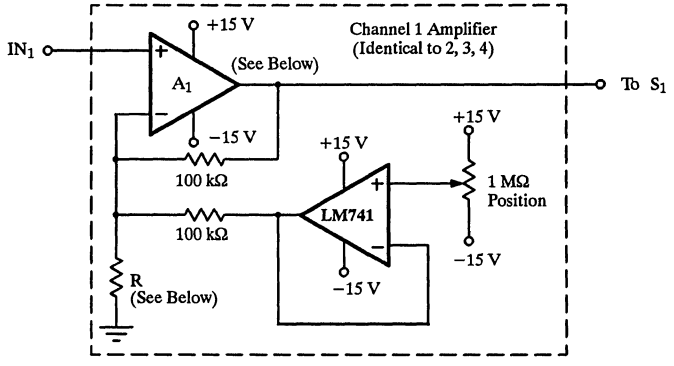


Aquisition Time = 25 µs
Aperature Time = 1 µs
Sample to Hold Offset = 5 mV
Droop Rate = 5 mV/s

Figure 7. DG211 Sample-and-Hold

Applications (Cont'd)





A_1 is op amp with suitable bandwidth, slew rate, etc., for desired signals.
R is added for extra gain according to formula: Voltage Gain = $1 + \frac{100\ k\Omega}{R}$

Figure 8. The "Scope Extender" Which Displays 4-Channels Simultaneously on a Single Trace Scope

Siliconix
A Member of the TEMIC Group

Improved Quad CMOS Analog Swtiches

Features

- ±22-V Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance—$r_{DS(on)}$: 50 Ω
- Low Leakage—$I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching—t_{ON}: 120 ns
- Low Glitching—Q: 1 pC

Benefits

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG211/212

Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

Description

The DG211B/212B analog switches are highly improved versions of the industry-standard DG211/212. These devices are fabricated in Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

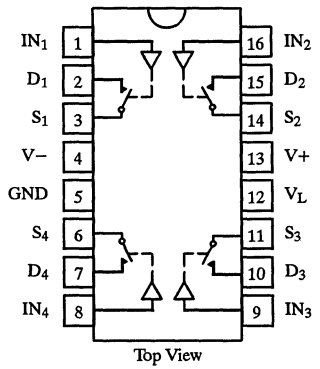
These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG211B and DG212B can handle up to ±22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG211B is a normally closed switch and the DG212B is a normally open switch. (See Truth Table.)

Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

Truth Table

Logic	DG211B	DG212B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG211BDJ
		DG212BDJ
	16-Pin Narrow SOIC	DG211BDY
		DG212BDY

P-32167—Rev. A (11/15/93)

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 30 mA, whichever occurs first
Current, Any Terminal ..... 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 640 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	−15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room Full		45	85 100	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		2		
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	−0.5 −5	±0.01	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	−0.5 −5	±0.01	0.5 5	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room Full	−0.5 −10	±0.02	0.5 10	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full	−1		1	µA
Input Capacitance	C_{IN}		Room		5		pF
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 2 V See Figure 2	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room		1		pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		5		
Channel On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	C_L = 15 pF, R_L = 50 Ω V_S = 1 V_{RMS}, f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X_{TALK}		Room		95		

1

Specifications

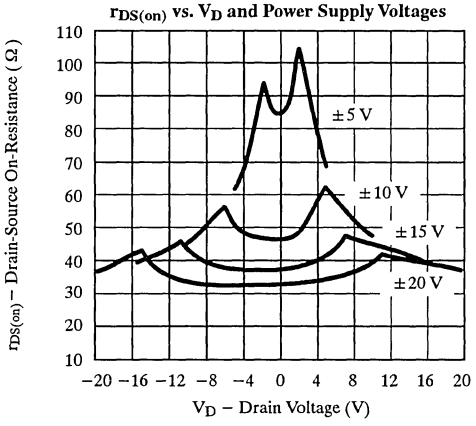
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			10 50	µA
Negative Supply Current	I−		Room Full	−10 −50			
Logic Supply Current	I_L		Room Full			10 50	
Power Supply Range for Continuous Operation	V_{OP}		Full	±4		±22	V

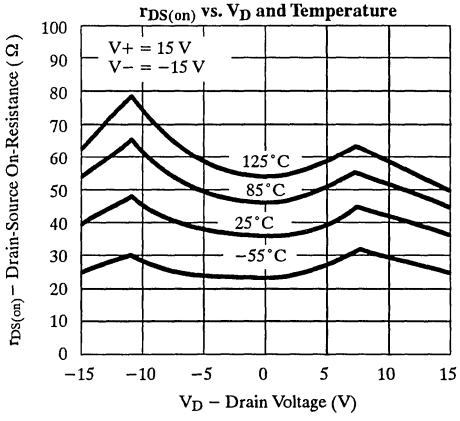
Specifications for Single Supply

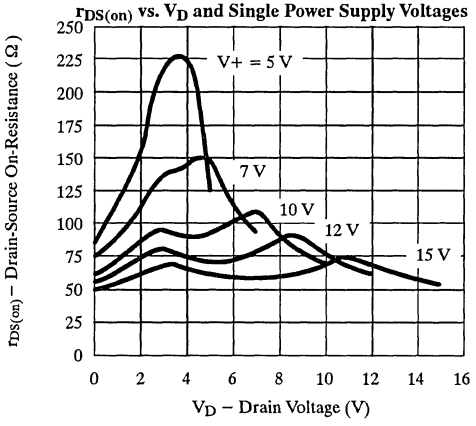
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 8 V, I_S = 1 mA	Room Full		90	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 8 V See Figure 2	Room			300	ns
Turn-Off Time	t_{OFF}		Room			200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room		4		pC
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full			10 50	µA
Negative Supply Current	I−		Room Full	−10 −50			
Logic Supply Current	I_L		Room Full			10 50	
Power Supply Range for Continuous Operation	V_{OP}		Full	+4		+44	V

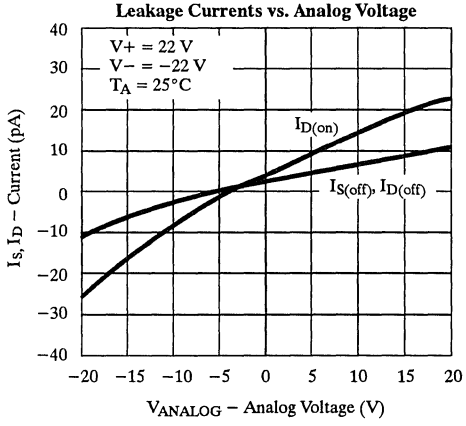
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

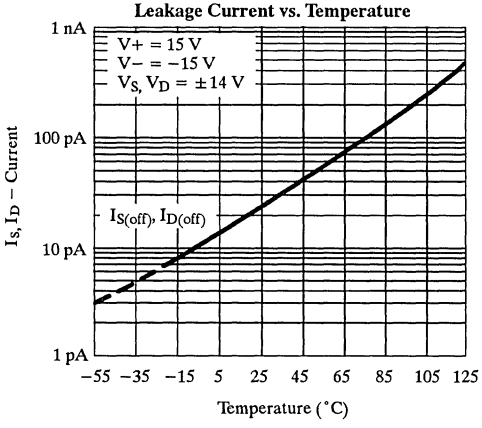
Typical Characteristics

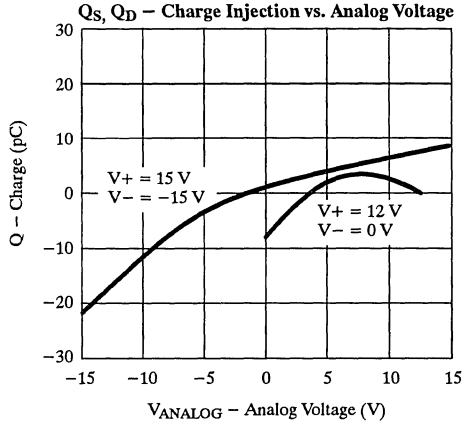












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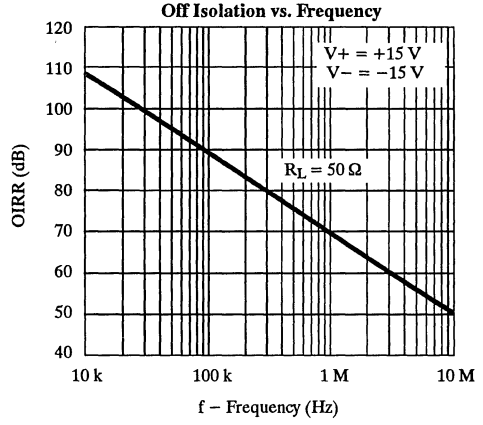
Typical Characteristics (Cont'd)



Schematic Diagram (Typical Channel)

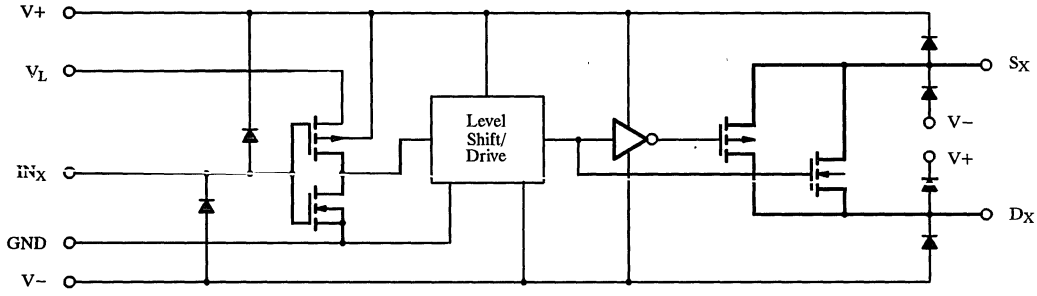
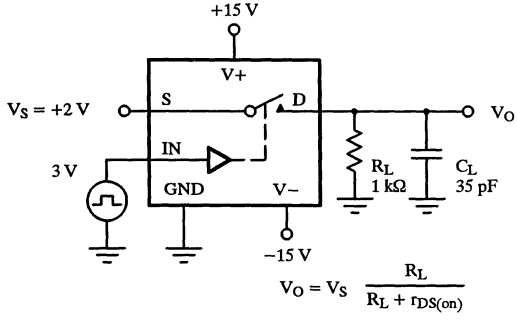


Figure 1.

Test Circuits



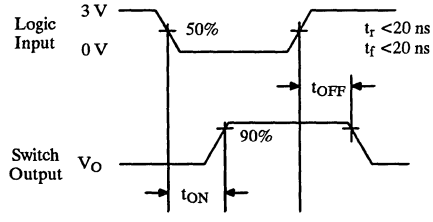


Figure 2. Switching Time

Test Circuits (Cont'd)

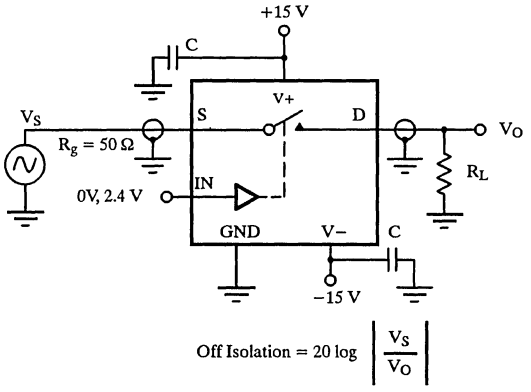


Figure 3. Off Isolation

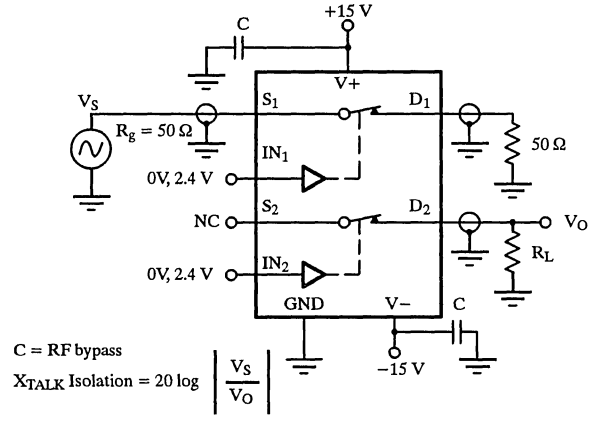
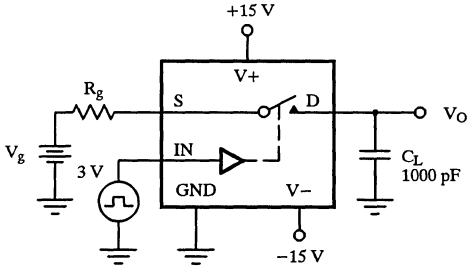
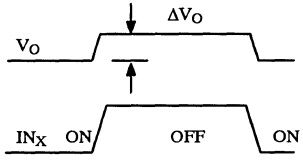


Figure 4. Channel-to-Channel Crosstalk





ΔVO = measured voltage error due to charge injection
The charge injection in coulombs is Q = CL x ΔVO

Figure 5. Charge Injection

Applications

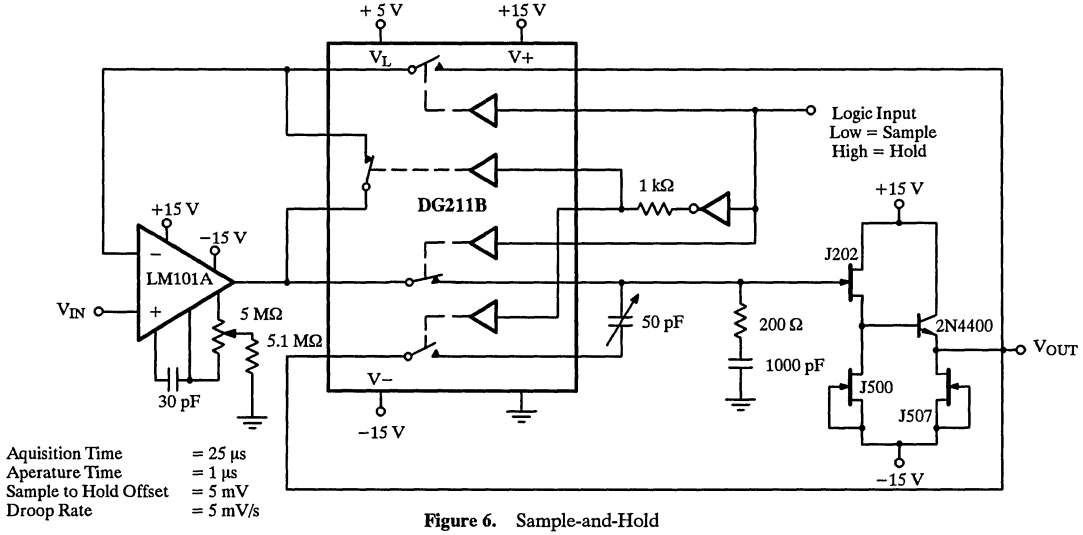


Figure 6. Sample-and-Hold

1

Applications (Cont'd)

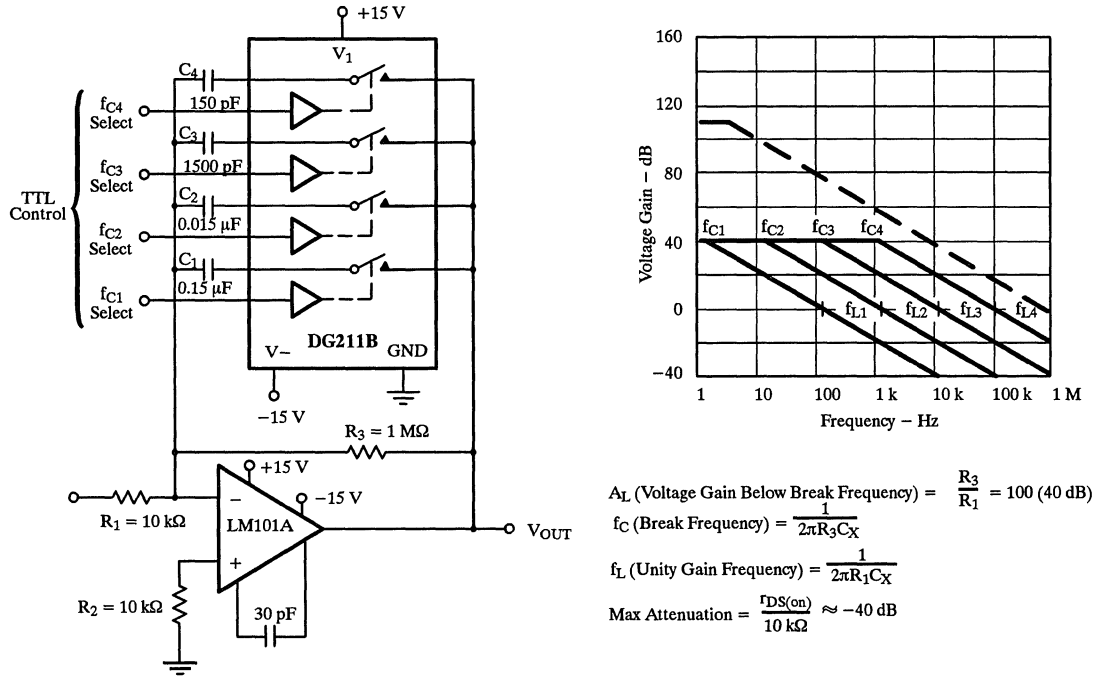


Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

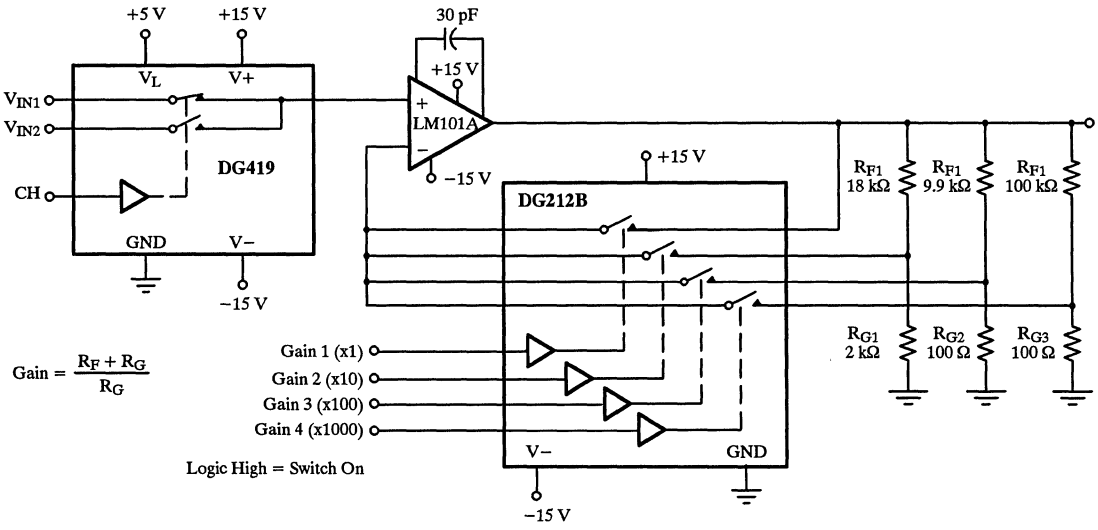


Figure 8. A Precision Amplifier with Digitally Programable Input and Gains

Quad SPST CMOS Analog Switch with Latches

Features

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Built on PLUS-40 Process
- Latches Are Transparent with $\overline{WR}$ Low
- Low On-Resistance: 60 Ω

Benefits

- Compatible with Most µP Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

Applications

- µP Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

Description

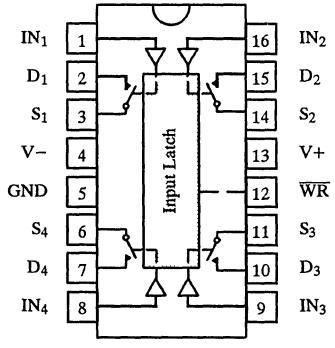
The DG221 is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common $\overline{WR}$ pin, each DG221 can be memory mapped, and addressed as a single data byte for simultaneous switching.

Designed on the Siliconix PLUS-40 CMOS process, the DG221 combines low power and low on-resistance (60 Ω typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition. These switches guarantee a rail-to-rail blocking capability (44 V max), in the off condition.

Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

Four Latchable SPST Switches per Package

Truth Table

IN_X	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X	⌐	Control data latched-in, switches on or off as selected by last IN_X
X	1	Maintains previous state

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG221CJ
−40°C to 85°C	16-Pin Narrow SOIC	DG221DY
−55°C to 125°C	16-Pin CerDIP	DG221AK/883

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 70 mA
Storage Temperature: (AK Suffix) ..... −65 to 150°C
(CJ and DY Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin CerDIP[c] ..... 900 mW
16-Pin Plastic DIP[d] ..... 470 mW
16-Pin SOIC[e] ..... 600 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 12 mW/°C above 75°C
d. Derate 6.5 mW/°C above 25°C
e. Derate 7.7 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8[f] V, $\overline{WR}$ = 0	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±10 V	Room Full	60		90 135		90 135	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.01	−1 −100	1 100	−5 −100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.02	−1 −100	1 100	−5 −100	5 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±14 V	Room Full	±0.01	−1 −200	1 200	−5 −200	5 200	nA
Digital Control									
Input Current	I_{INL}, I_{INH}	V_{IN} = 0 V or = 2.4 V	Room Full	−0.0004	−1 −10	1 10	−1 −10	1 10	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room			550		550	ns
Turn-Off Time	t_{OFF}	See Figure 2	Room			340		340	ns
Turn-On Time Write	t_{ON}, $\overline{WR}$	See Figure 3	Room			550		550	ns
Turn-Off Time Write	t_{OFF}, $\overline{WR}$	See Figure 3	Room			340		340	ns
Write Pulse Width	t_W	See Figure 4	Room	120	150		150		ns
Input Setup Time	t_S	See Figure 4	Room	130	180		180		ns
Input Hold Time	t_H	See Figure 4	Full	0	20		20		ns
Charge Injection	Q	C_L = 1000 pF V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	20					pC
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S, V_D = 0 V	Room	8					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_S, V_D = 0 V	Room	9					pF
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_S, V_D = 0 V	Room	29					pF
Off Isolation	OIRR	V_S = 1 V_{P-P}, f = 100 kHz C_L = 15 pF, R_L = 1 kΩ	Room	70					dB
Interchannel Crosstalk	X_{TALK}	V_S = 1 V_{P-P}, f = 100 kHz C_L = 15 pF, R_L = 1 kΩ	Room	90					dB

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8[f] V, $\overline{WR}$ = 0	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	All Channels On or Off V_{IN} = 0 V or 2.4 V	Full	0.8		1.5		1.5	mA
Negative Supply Current	I−		Room	−0.4	−1		−1		

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Schematic Diagram (Typical Channel)

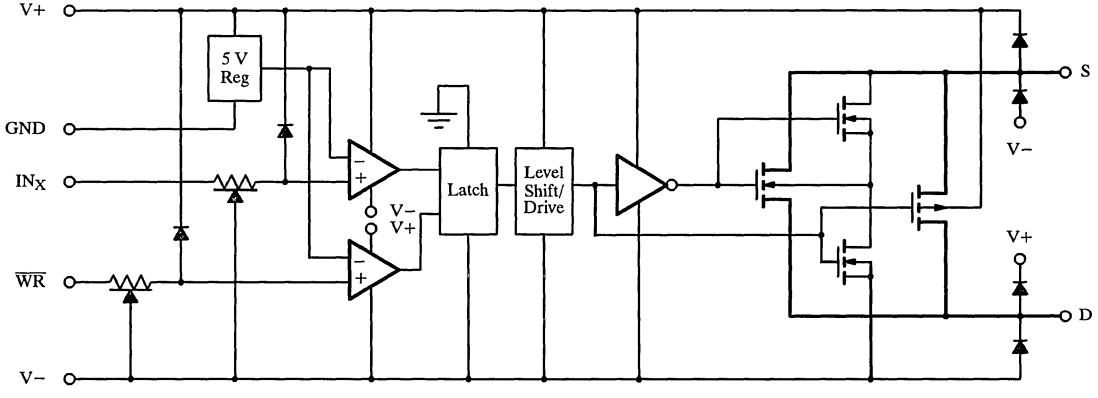
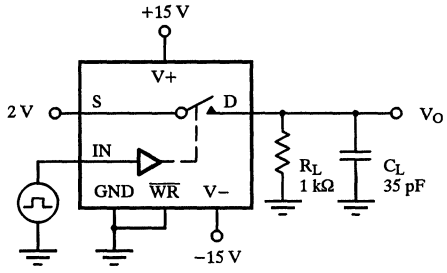
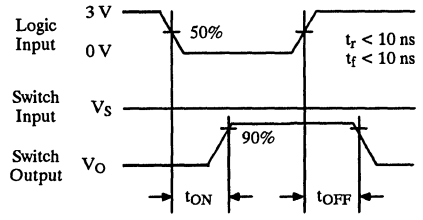


Figure 1.

Test Circuits

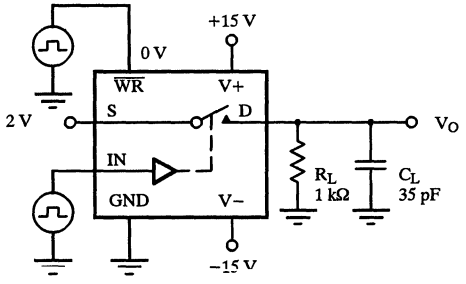


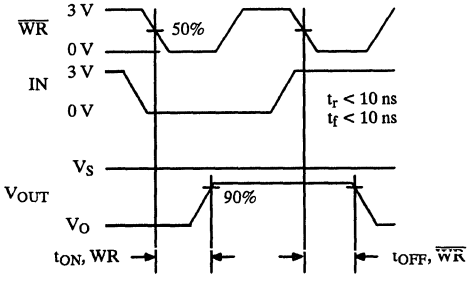


C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

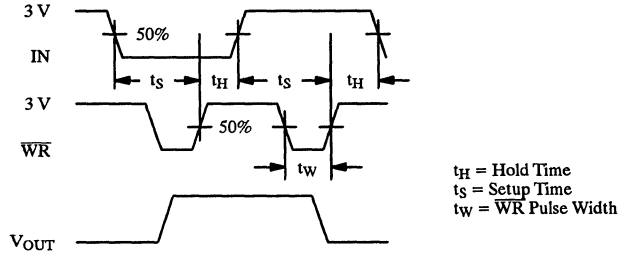




C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

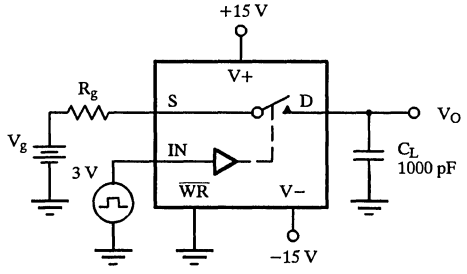
Figure 3. $\overline{WR}$ Switching Time

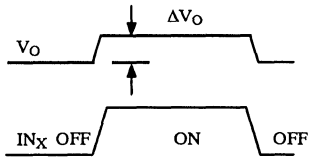


The latches are level sensitive. When $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

Figure 4. $\overline{WR}$ Setup Conditions

Test Circuits (Cont'd)





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

Figure 5. Charge Injection

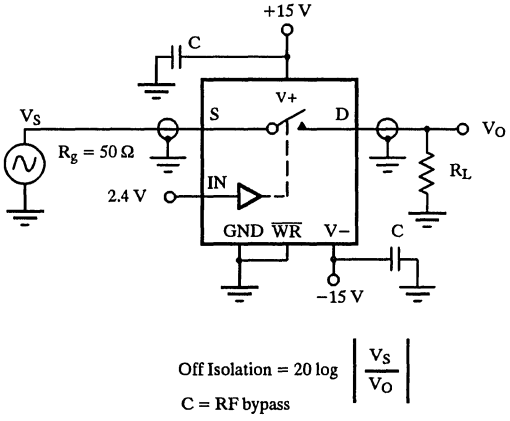


Figure 6. Off Isolation

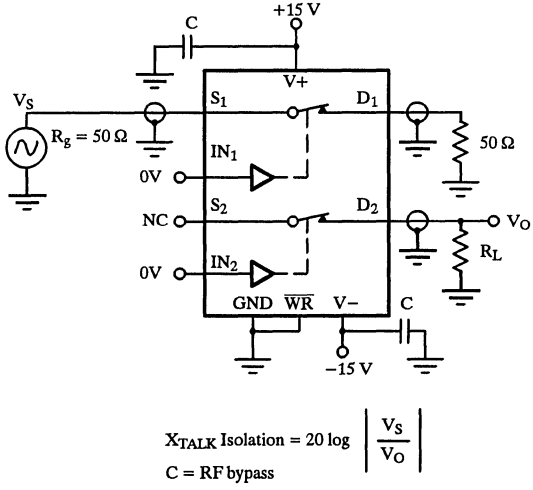


Figure 7. Channel-to-Channel Crosstalk

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	GND (V)	$\overline{WR}$ (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	−15	0	2.4/0.8	2.4/0.8	−15 to 15
20	−20	0	2.4/0.8	2.4/0.8	−20 to 20
10	−10	0	2.4/0.8	2.4/0.8	−10 to 10
10	−5	0	2.4/0.8	2.4/0.8	−5 to 10

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

Applications

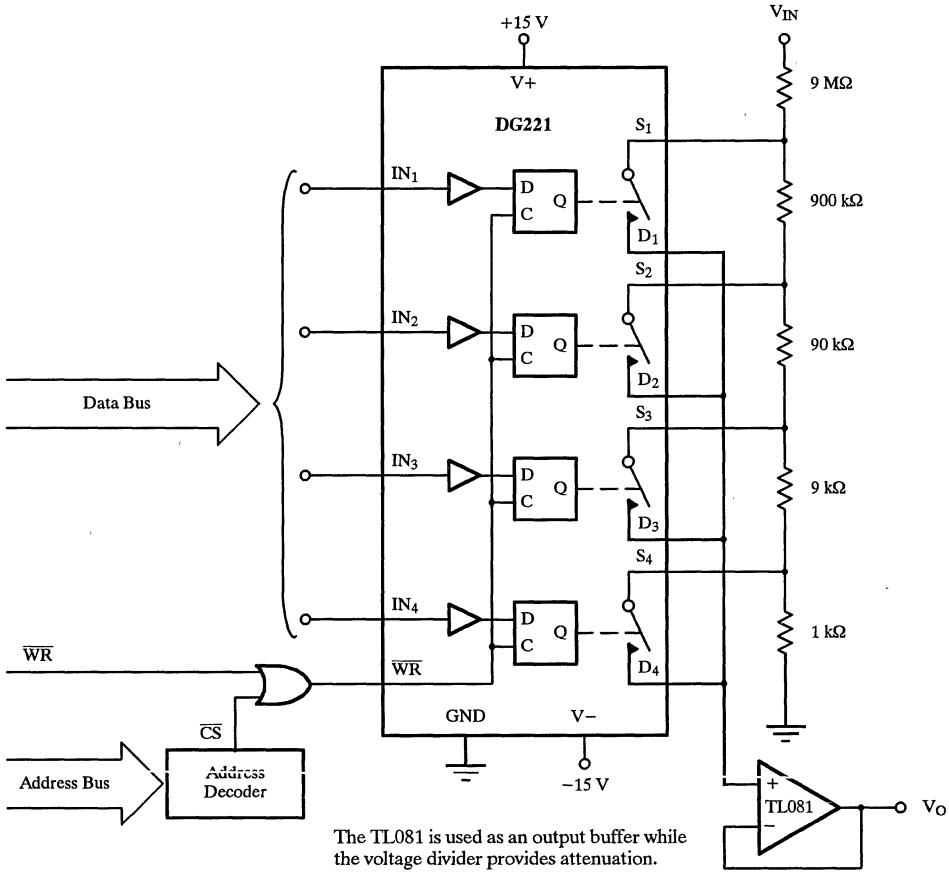


Figure 8. µP-Controlled Analog Signal Attenuator

Truth Table

IN_1	IN_2	IN_3	IN_4	$\overline{WR}$[a]	On Switch
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

Output Attenuation for Figure 8

$\overline{WR}$	IN_1	IN_2	IN_3	IN_4	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

Notes:

a. $\overline{WR}$ may be held at "0" for temporary operation similar to DG201A's. With $\overline{WR}$ at "0" SW_1 will remain on as long as IN_1 is held at "0".

General Purpose Monolithic Dual SPDT CMOS Analog Switch

Features

- PLUS-40 Process
- Make-Before-Break Operation
- Full Rail-to-Rail Analog Signal Range
- True TTL Compatibility
- Low $r_{DS(on)}$: 30 Ω

Benefits

- Low Power
- Reduced Switching Noise
- Reduced Need for Buffers

Applications

- Programmable Gain Amplifiers
- Analog Multiplexing
- Servo Control Systems
- Programmable Filters
- Audio Switching

Description

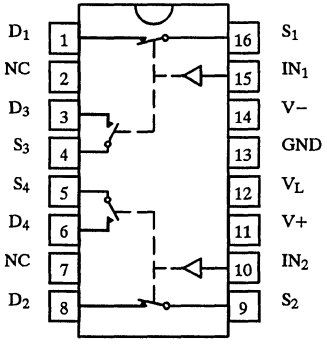
The DG243 is a monolithic dual SPDT analog switch designed for general switching applications in communication, instrumentation, and process control systems. Featuring make-before-break action, the DG243 is used in closed loop systems to switch gain or bandwidth networks without opening the loop.

The DG243 is designed on the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG243CJ

1

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
V_L ..... (GND − 0.3 V) to 44 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA
Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] ..... 450 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.0 V, 0.8 V[e]	Temp[a]	C Suffix 0 to 70°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	−15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±10 V	Room Full		30	50 75	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	−1 −100	±0.3	1 100	nA
	$I_{D(off)}$		Room Full	−1 −100	±0.3	1 100	
Channel On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Full	−2 −200	±0.5	2 200	
Digital Control							
Input Current with V_{IN} Low	I_{IL}	V_{IN}= 0.8 V	Full	−1	−0.005	1	µA
Input Current with V_{IN} High	I_{IH}	V_{IN}= 2.0 V	Full	−1	−0.01	1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, See Figure 2	Room		250	700	ns
Turn-Off Time	t_{OFF}		Room		390	1200	
Charge Injection	Q	C_L = 1000 pF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		60		pC
Off Isolation Reject Ratio	OIRR	R_L = 75 Ω, f = 1 MHz	Room		75		dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room		89		
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room		15		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		17		
Channel-On Capacitance	$C_{D+S(on)}$		Room		45		
Power Supplies							
Positive Supply Current	I+	All Channels On or Off	Room		180	300	µA
Negative Supply Current	I−		Room	−300	−150		
Logic Supply Current	I_L		Room		100	300	
Ground Current	I_{GND}		Room	−300	−140		

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Schematic Diagram (Typical Channel)

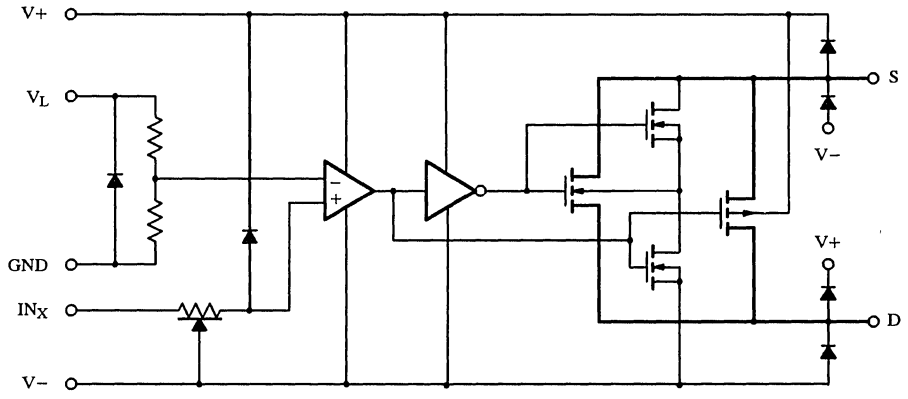
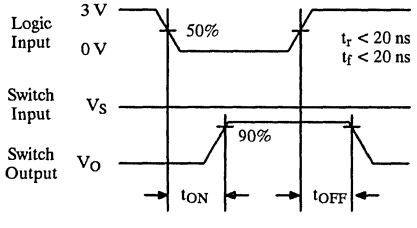
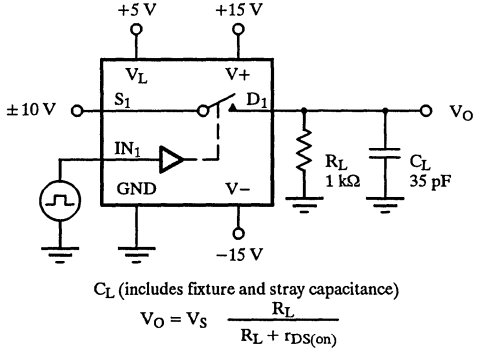


Figure 1.

Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.





C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

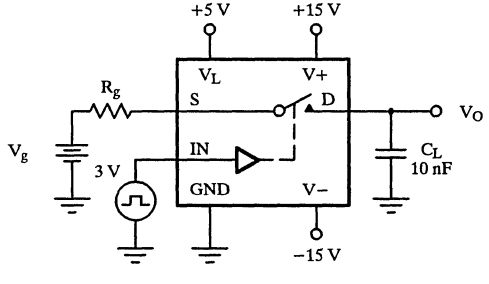


Figure 3. Charge Injection

Applications

The make-before-break operation of the DG243 provides simple transient suppression in these two important applications.

Figure 3 shows a minimum amount of glitching during changes of gain states. The relatively low impedance of the gain setting resistors (10 kΩ, 1 kΩ, and 100 Ω) shunt the injected charge-to-ground minimizing transient effects occurring at the inverting input of the op amp. Consequently, these transients are not amplified to V_{OUT}.

Figure 4 takes advantage of the make-before-break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The best results are obtained by selecting an op amp with the proper offset voltage specification.

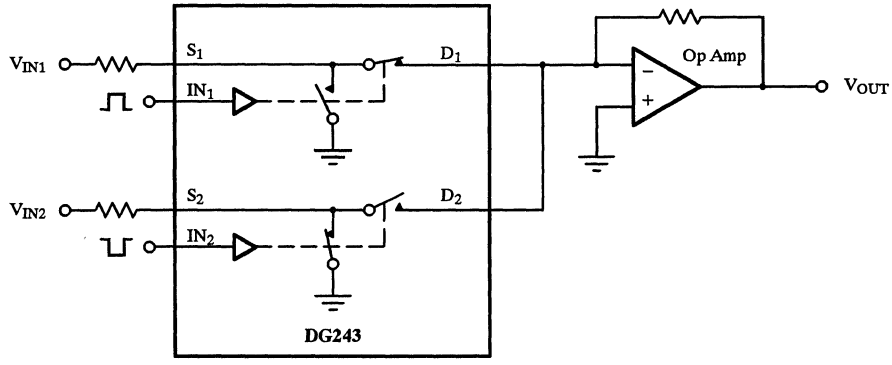
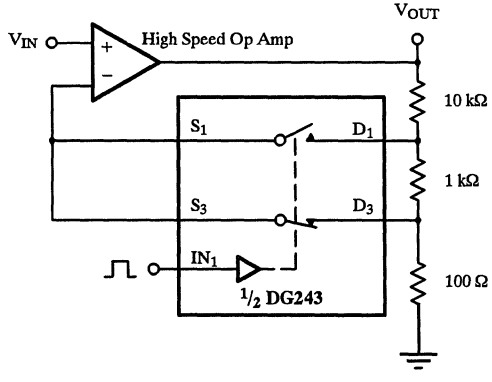
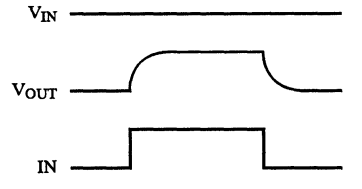


Figure 4. Minimizing Glitches in Audio Switching





Clean transitions no glitches due to op amp open loop.

Figure 5. Make-Before-Break Improves Transient Response in Programmable Gain Amplifiers

High-Speed Quad Monolithic SPST CMOS Analog Switch

Features

- Fast Switching t_{ON}: 55 ns
- Low Charge Injection: 9 pC
- Low $r_{DS(on)}$: 32 Ω
- TTL Compatible
- Low Leakage: 50 pA

Benefits

- Fast Settling Times
- Reduced Switching Glitches
- High Precision

Applications

- High Speed Switching
- Sample/Holds
- Digital Filters
- Op Amp Gain Switching
- Flight Control Systems

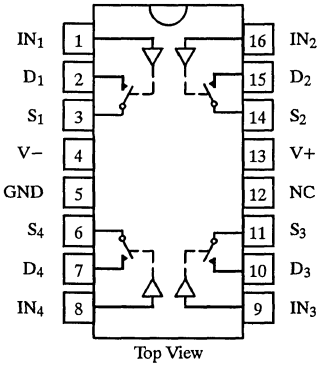
Description

The DG271 high speed quad single-pole single-throw analog switch is intended for applications that require low on-resistance, low leakage currents, and fast switching speeds.

Built on Siliconix' proprietary high voltage silicon gate process to achieve superior on/off performance, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latchup.

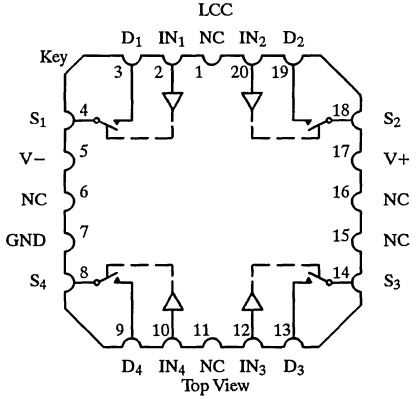
Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

LCC



Top View

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG271CJ
−40 to 85°C	16-Pin Narrow SOIC	DG271DY
−55 to 125°C	16-Pin CerDIP	DG271AK
		DG271AK/883
		5962-8671602MEA
	LCC-20	DG271AZ/883
		5962-8671602M2A

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2 V

Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Storage Temperature (AK, AZ, DY Suffix) ..... −65 to 150°C
(CJ Suffix) ..... −65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Plastic Narrow SOIC[d] ..... 600 mW
16-Pin CerDIP[e] ..... 900 mW
LCC-20[f] ..... 750 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C
f. Derate 10 mW/°C above 75°C

Specifications[a]

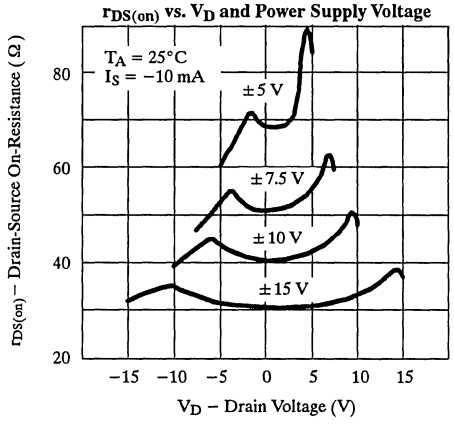
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	C, D Suffix 0 to 70°C, −40 to 85°C Min[d]	C, D Suffix 0 to 70°C, −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = 1 mA, V_D = ±10 V	Room Full	32		50 75		50 75	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	±0.05	−1 −100	1 100	−1 −100	1 100	nA
	$I_{D(off)}$		Room Full	±0.05	−1 −100	1 100	−1 −100	1 100	
Channel On Leakage Current	$I_{D(on)}$ + $I_{S(on)}$	V_S = V_D = ±14 V	Room Full	±0.05	−1 −200	1 200	−1 −200	1 200	
Digital Control									
Input Current with Voltage High	I_{INH}	V_{IN} = 2 V	Room Full	0.010	−1 −10		−1 −10		µA
		V_{IN} = 15 V	Room Full	0.010		1 10		1 10	
Input Current with Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	0.010	−1 −10		−1 −10		
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = ±10 V See Figure 2	Room Full	55		65 80		65 80	ns
Turn-Off Time	t_{OFF}		Room Full	50		65 80		65 80	
Charge Injection	Q	C_L = 100 pF, V_{gen} = 0 V R_{gen} = 0 Ω	Room	9					pC

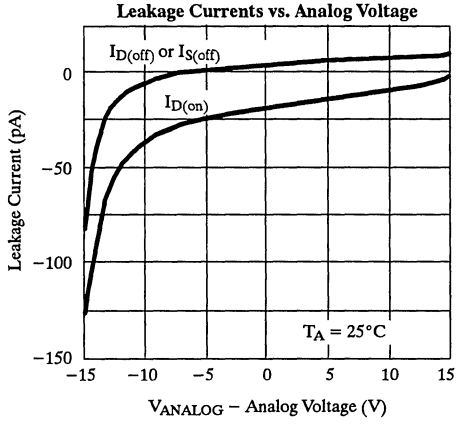
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	C, D Suffix 0 to 70°C, −40 to 85°C Min[d]	C, D Suffix 0 to 70°C, −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Source Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{IN} = 5 V f = 1 MHz	Room	6					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, V_{IN} = 0 V	Room	24					
Off Isolation	OIRR	R_L = 50 Ω, f = 1 MHz	Room	75					dB
Crosstalk	X_{TALK}		Room	95					
Supply									
Positive Supply Current	I+	All Channels On or Off	Room Full	4.3		7.5 11		7.5 11	mA
Negative Supply Current	I−		Room Full	−3.4	−6 −10		−6 −10		

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

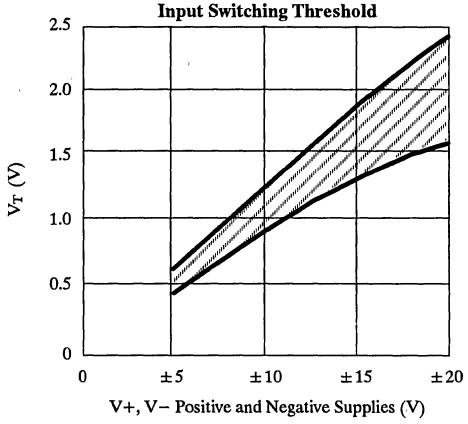
Typical Characteristics



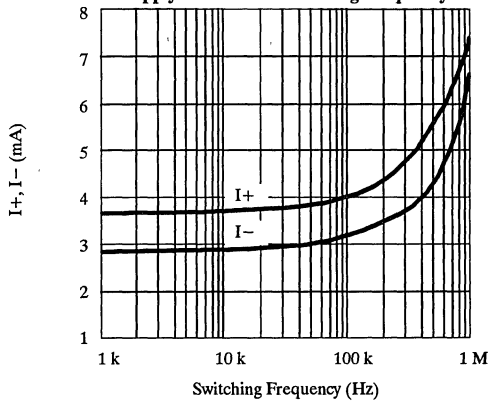


Typical Characteristics (Cont'd)

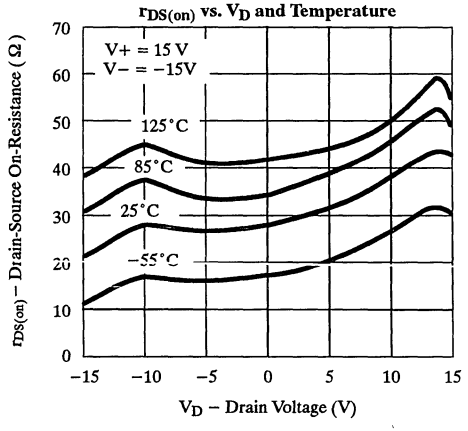
Input Switching Threshold



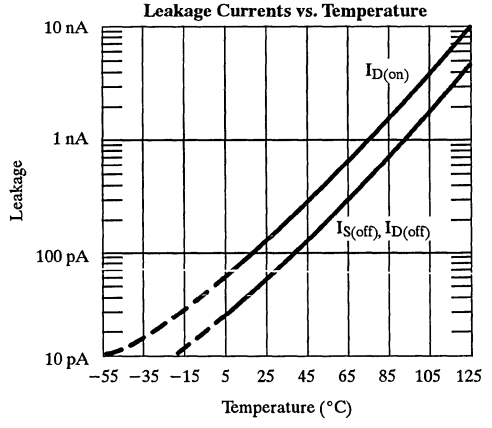
Supply Current vs. Switching Frequency



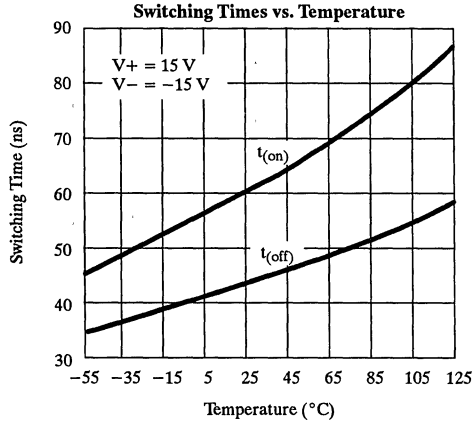
$r_{DS(on)}$ vs. V_D and Temperature



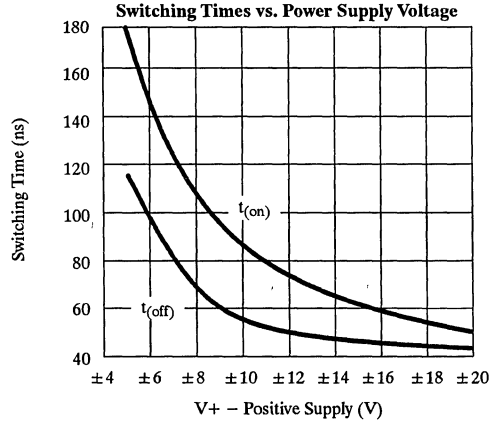
Leakage Currents vs. Temperature



Switching Times vs. Temperature



Switching Times vs. Power Supply Voltage



Schematic Diagram (Typical Channel)

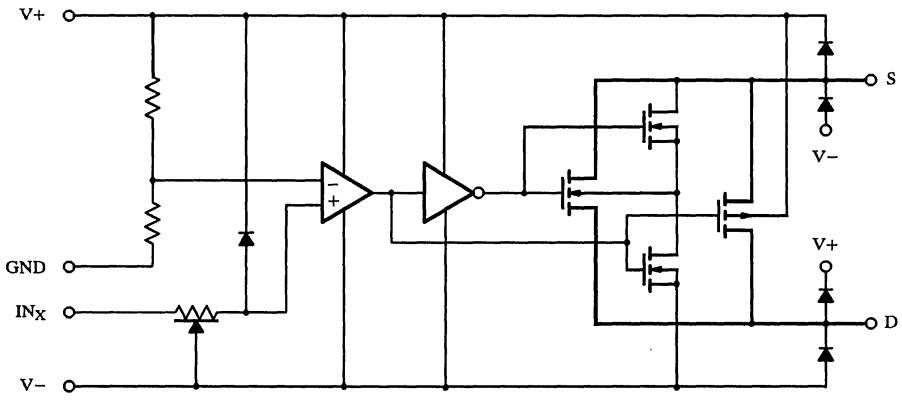
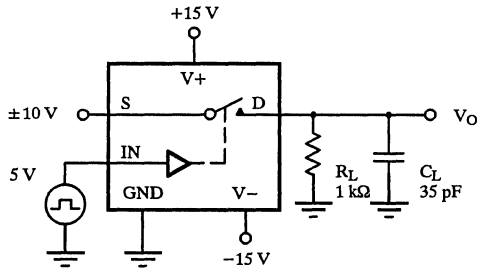


Figure 1.

Test Circuits



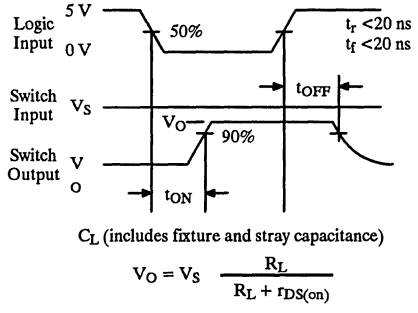


Figure 2. Switching Time

Siliconix
A Member of the TEMIC Group

CMOS Analog Switches

Features

- Analog Signal Range: ± 15 V
- Fast Switching—t_{ON}: 150 ns
- Low On-Resistance—$r_{DS(on)}$: 30 Ω
- Single Supply Operation
- Latch-up Proof
- CMOS Compatible

Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

Description

The DG300A-DG303A family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

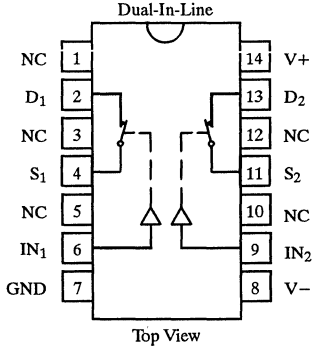
Designed on the Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

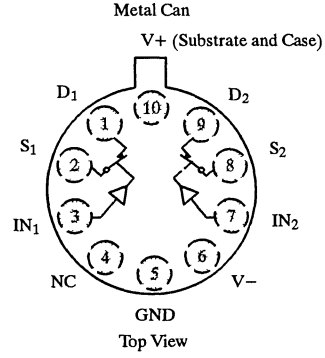
In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

Featuring low power consumption (3.5 mW typ) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V− rail to 0 V.

Functional Block Diagram and Pin Configuration

DG300A





Ordering Information – DG300A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG300ACJ
−25 to 85°C	14-Pin CerDIP	DG300ABK
	10-Pin Metal Can	DG300ABA
−55 to 125°C	14-Pin CerDIP	DG300AAK
		DG300AAK/883
		JM38510/11601BCA
	14-Pin Sidebraze	JM38510/11601BCC
	10-Pin Metal Can	DG300AAA/883
		JM38510/11601BIA

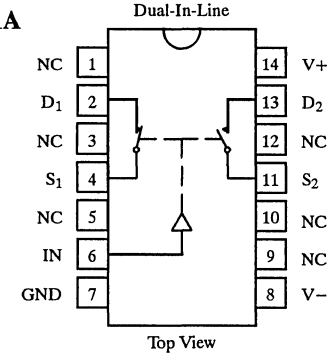
Truth Table

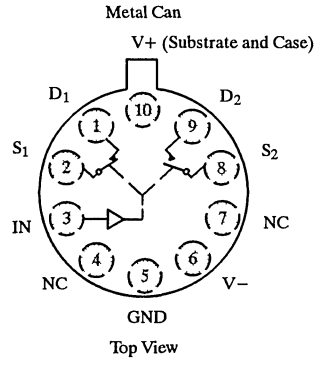
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V
Switches Shown for Logic "1" Input

Functional Block Diagram and Pin Configuration (Cont'd)

DG301A





Ordering Information – DG301A

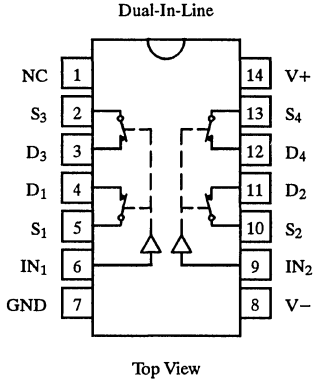
Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG301ACJ
−25 to 85°C	14-Pin CerDIP	DG301ABK
	10-Pin Metal Can	DG301ABA
−55 to 125°C	14-Pin CerDIP	DG301AAK
		DG301AAK/883
		JM38510/11602BCA
	14-Pin Sidebraze	JM38510/11602BCC
	10-Pin Metal Can	DG301AAA
		DG301AAA/883
		JM38510/11602BIA

Truth Table

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V
Switches Shown for Logic "1" Input

DG302A



Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V
Switches Shown for Logic "1" Input

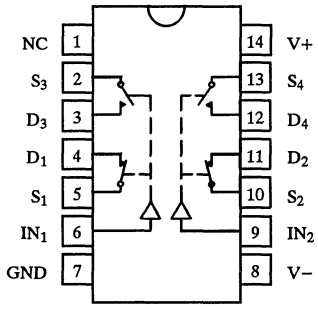
Ordering Information – DG302A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG302ACJ
−55 to 125°C	14-Pin CerDIP	DG302AAK
		DG302AAK/883
		JM38510/11603BCA
	14-Pin Sidebraze	JM38510/11603BCC

Functional Block Diagram and Pin Configuration (Cont'd)

DG303A

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

Ordering Information – DG303A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG303ACJ
−25 to 85°C	14-Pin CerDIP	DG303ABK
−55 to 125°C	14-Pin CerDIP	DG303AAK
−55 to 125°C	14-Pin CerDIP	DG303AAK/883
−55 to 125°C	14-Pin CerDIP	JM38510/11604BCA
−55 to 125°C	14-Pin Sidebraze	JM38510/11604BCC

Absolute Maximum Ratings

Voltages Referenced to V−

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA

(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... −65 to 150°C

(C Suffix) ..... −65 to 125°C

Power Dissipation[b]

14-Pin Plastic DIP[c] ..... 470 mW

14-Pin CerDIP[d] ..... 825 mW

10-Pin Metal Can[e] ..... 450 mW

Notes:

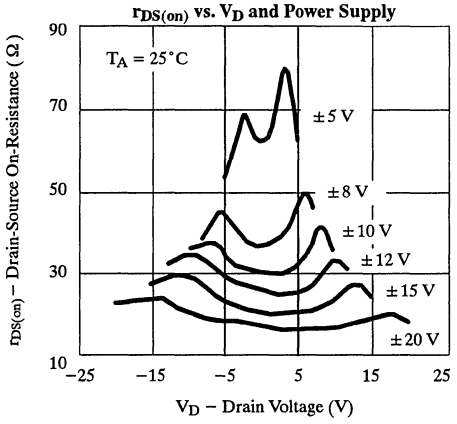
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 11 mW/°C above 75°C
e. Derate 6 mW/°C above 75°C

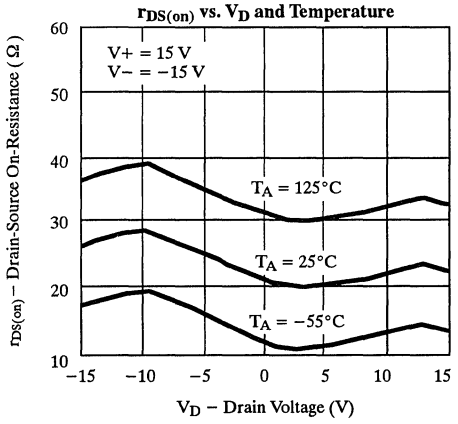
Specifications[a]

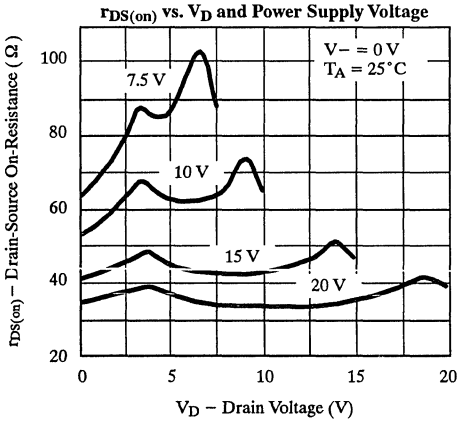
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 0.8 V or V_{IN} = 4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B. C Suffix Min[d]	B. C Suffix Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −10 mA	Room Full	30		50 75		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	±0.1	−1 −100	1 100	−5 −100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	±0.1	−1 −100	1 100	−5 −100	5 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Hot	±0.1	−1 −100	1 100	−5 −100	5 100	nA
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Full	−0.001	−1 −1		−1		µA
		V_{IN} = 15 V	Room Full	0.001		1 1		1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	−0.001	−1 −1		−1		µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room	150		300			ns
Turn-Off Time	t_{OFF}	See Figure 2	Room	130		250			ns
Break-Before-Make Time	t_{OPEN}	DG301A/303A Only See Figure 3	Room	50					ns
Charge Injection	Q	C_L = 1 nF, R_{gen} = 0 Ω, V_{gen} = 0 V See Figure 4	Room	8					pC
Source-Off Capacitance	$C_{S(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room	14					pF
Channel-On Capacitance	$C_{D(on)}$	V_S, V_D = 0 V, f = 1 MHz	Room	40					pF
Input Capacitance	C_{in}	f = 1 MHz, V_{IN} = 0 V	Room	6					pF
		f = 1 MHz, V_{IN} = 15 V	Room	7					pF
Off-Isolation	OIRR	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	62					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	74					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 4 V (One Input) All Others = 0 V	Room Full	0.23		0.5 1		1	mA
Negative Supply Current	I−	V_{IN} = 4 V (One Input) All Others = 0 V	Room Full	−0.001	−10 −100		−100		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)	Room Full	0.001		10 100		100	µA
Negative Supply Current	I−	V_{IN} = 0.8 V (All Inputs)	Room Full	−0.001	−10 −100		−100		µA

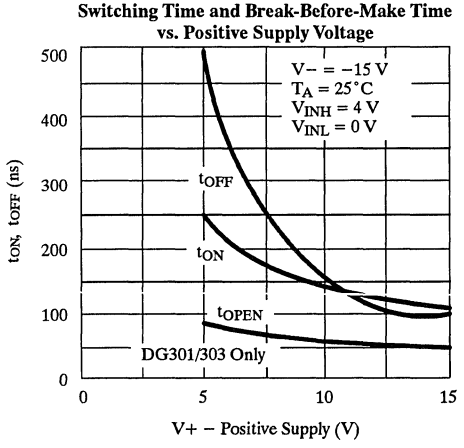
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

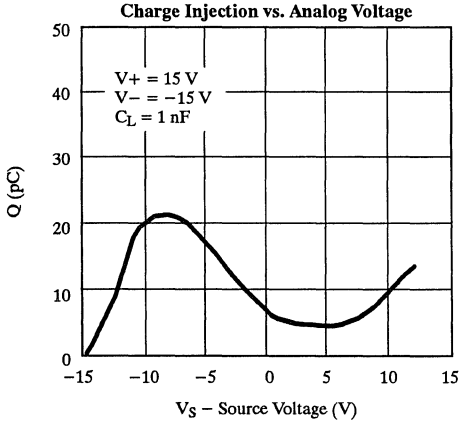
Typical Characteristics

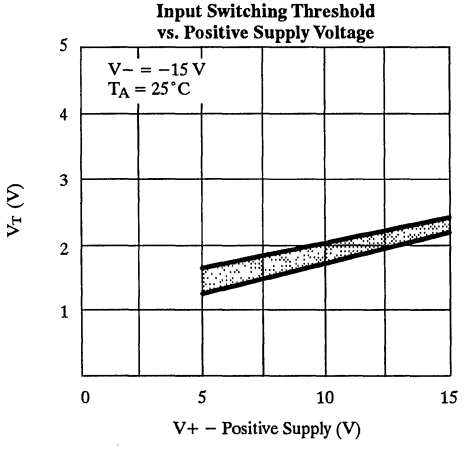




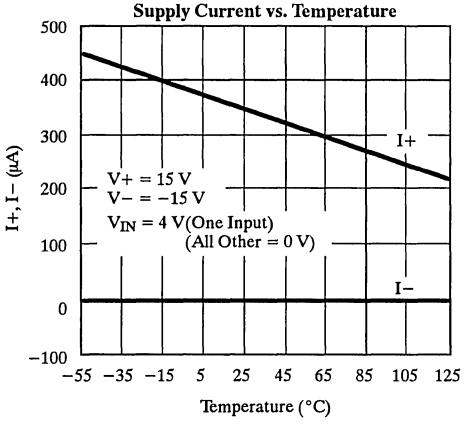


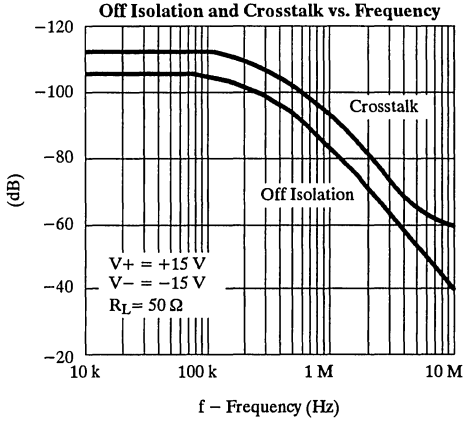


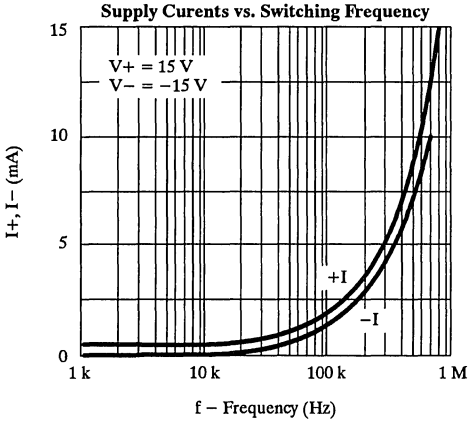


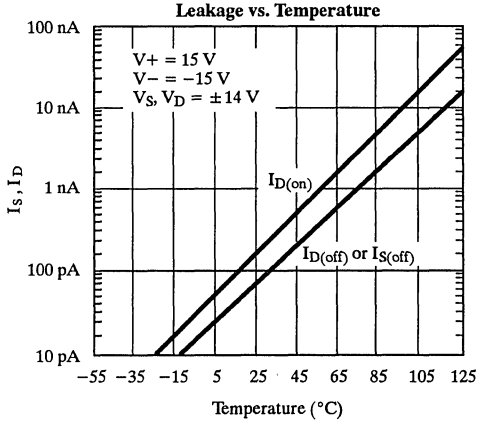


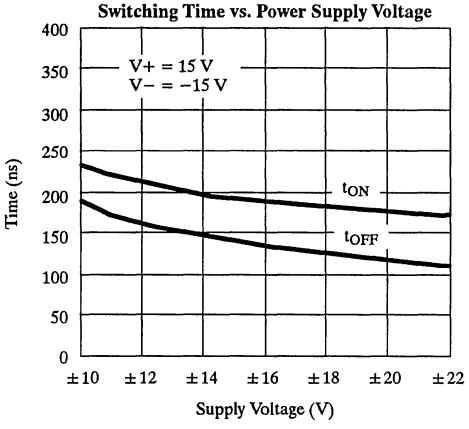
Typical Characteristics (Cont'd)

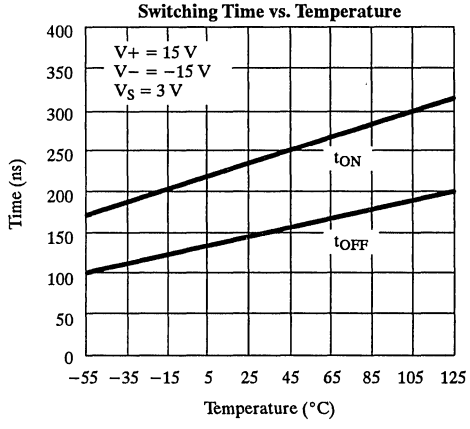












1

Schematic Diagram (Typical Channel)

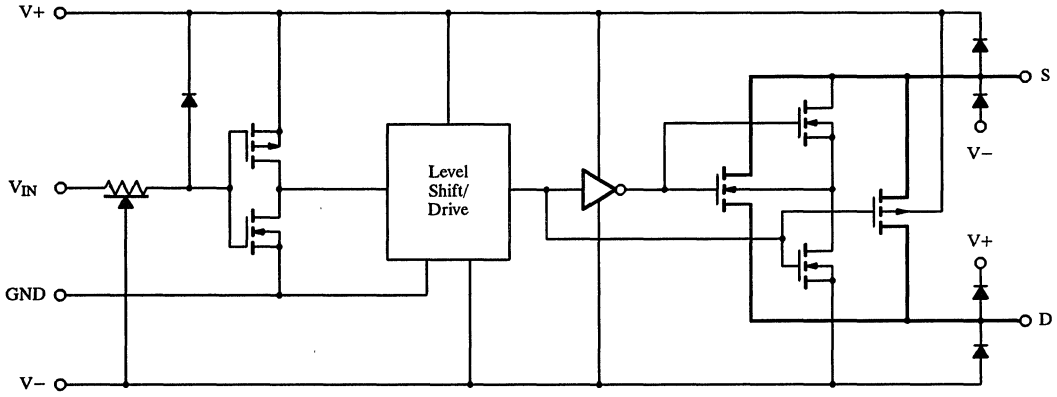
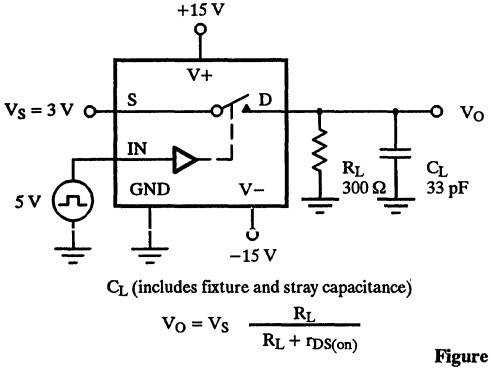


Figure 1.

Test Circuits



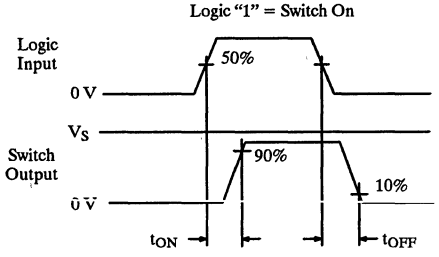
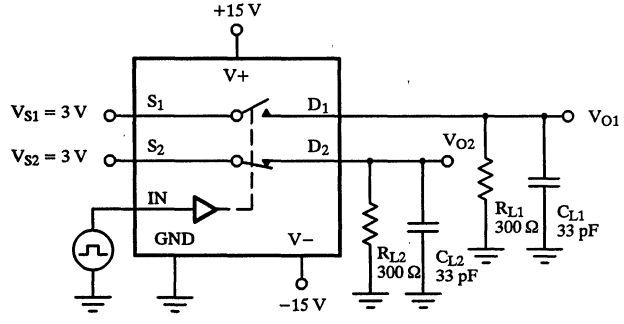


Figure 2. Switching Time



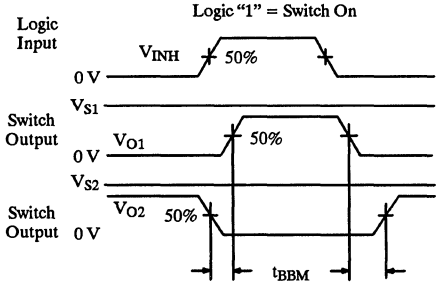


Figure 3. Break-Before-Make SPDT (DG301A, DG303A)

Test Circuits (Cont'd)

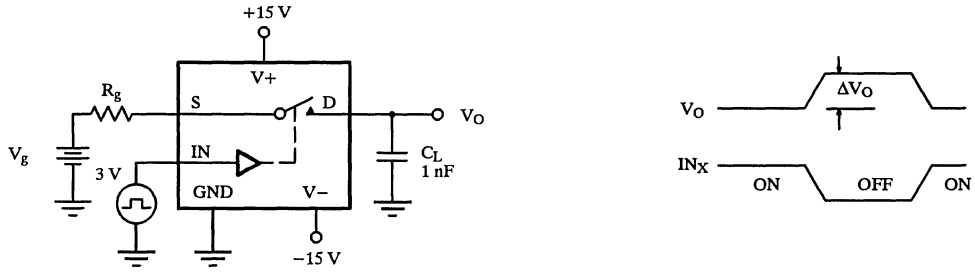


Figure 4. Charge Injection

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	GND Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	−15	0	4/0.8	−15 to 15
20	−20	0	4/0.8	−20 to 20
15	0	0	4/0.8	0 to 15

Note:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

1

Applications

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are: 1) Increased $r_{DS(on)}$; 2) slower switching speed. The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V. (See Input Switching Threshold vs. Positive Supply Voltage Curve.)

Applications (Cont'd)

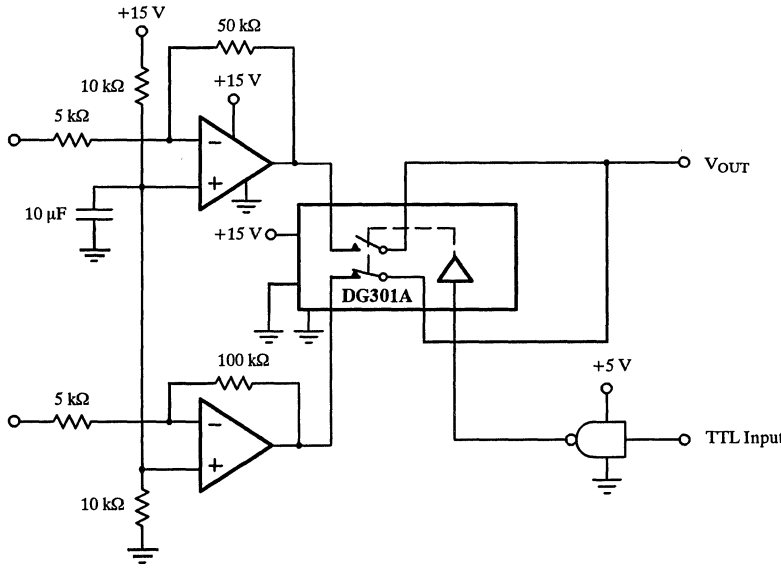


Figure 5. Single Supply Op Amp Switching

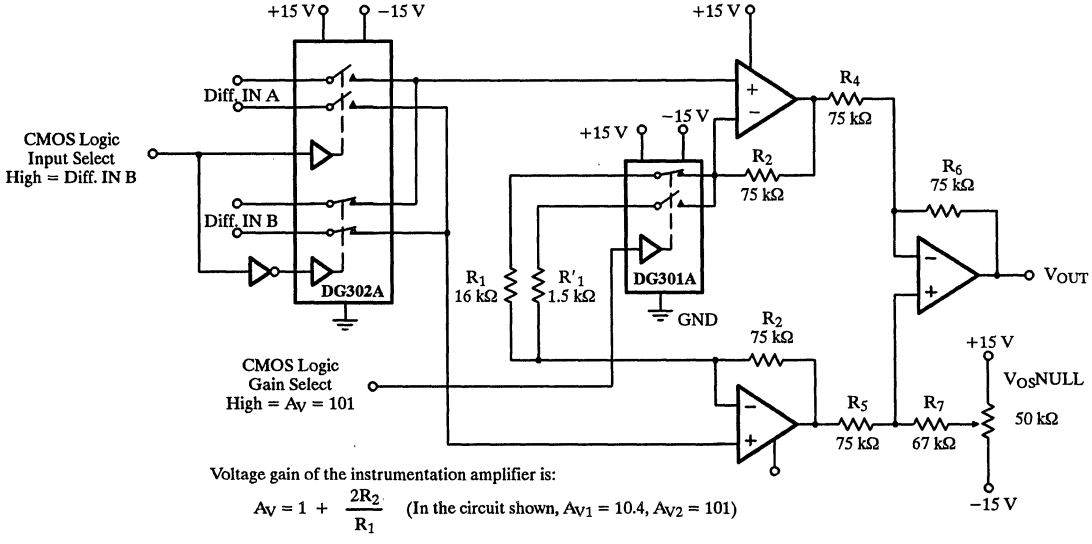


Figure 6. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

DG304A/305A/306A/307A

CMOS Analog Switches

Features

- ± 15-V Input Range
- Fast Switching—t_{ON}: 110 ns
- Low $r_{DS(on)}$: 30 Ω
- Single Supply Operation
- CMOS Logic Levels
- Micropower: 30 nW

Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Low Power Dissipation

Applications

- Low Level Switching Circuits
- Porgrammable Gain Amplifiers
- Portable and Battery Powered Systems

Description

The DG304A through DG307A series of monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat on-resistance over the entire analog range.

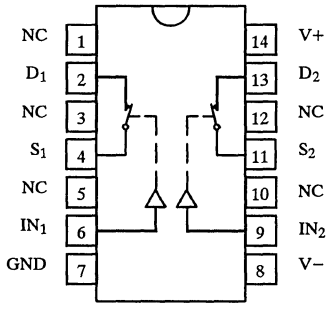
Designed on the Siliconix PLUS-40 CMOS process to achieve low power consumption and excellent on/off switch performance, these switches are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is allowed by connecting the V− rail to 0 V.

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS input compatible.

Functional Block Diagram and Pin Configuration

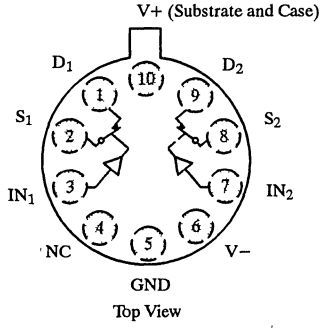
DG304A

Dual-In-Line



Top View

Metal Can



Top View

Ordering Information – DG304A

Temp Range	Package	Part Number
−0 to 70°C	14-Pin Plastic DIP	DG304ACJ
−55 to 125°C	14-Pin CerDIP	DG304AAK/883
		JM38510/11605BCA
	10-Pin Can	JM38510/11605BIA
	14-Pin Sidebraze	JM38510/11605BCC

Truth Table

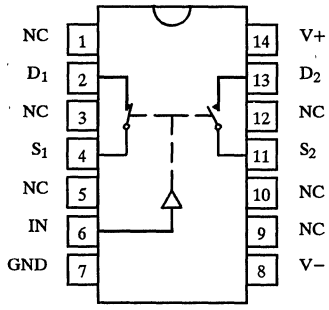
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V
Switches Shown for Logic "1" Input

Functional Block Diagram and Pin Configuration (Cont'd)

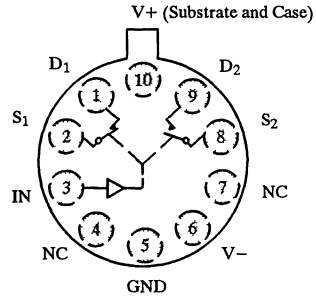
DG305A

Dual-In-Line



Top View

Metal Can



Top View

Ordering Information – DG305A

Temp Range	Package	Part Number
−55 to 125°C	14-Pin CerDIP	JM38510/11605BCA
	10-Pin Can	DG305AAA
		JM38510/11606BIC
	14-Pin Sidebraze	JM38510/11606BCA

Truth Table

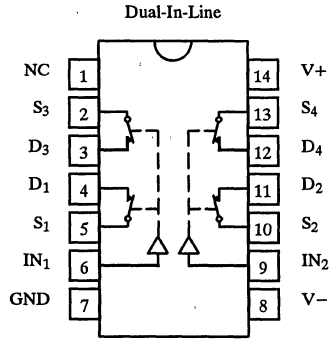
Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V

Switches Shown for Logic "1" Input

DG306A

Dual-In-Line



Top View

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V

Switches Shown for Logic "1" Input

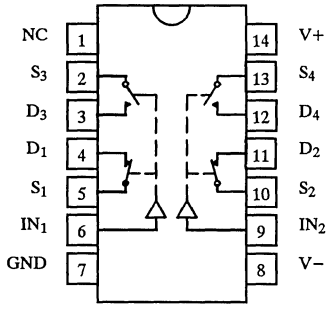
Ordering Information – 306A

Temp Range	Package	Part Number
−0 to 70°C	14-Pin Plastic DIP	DG306ACJ
−55 to 125°C	14-Pin CerDIP	DG306AAK/883
		JM38510/11607BCA
	14-Pin Sidebraze	JM38510/11607BCC

Functional Block Diagram and Pin Configuration (Cont'd)

DG307A

Dual-In-Line



Top View

Four SPST Switches per Package

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V

Switches Shown for Logic "1" Input

Ordering Information – 307A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG307ACJ
−25 to 85°C	14-Pin CerDIP	DG307ABK
−55 to 125°C	14-Pin CerDIP	DG307AAK
	14-Pin CerDIP	DG307AAK/883
	14-Pin CerDIP	JM38510/11608BCA
	14-Pin Sidebraze	JM38510/11608BCC

Absolute Maximum Ratings

Voltages Referenced to V−

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (AAA, AAK, ABK Suffix) −65 to 150°C
(ACJ Suffix) ..... −65 to 125°C

Power Dissipation[b]
14-Pin Plastic DIP[c] ..... 470 mW
14-Pin CerDIP[d] ..... 825 mW
10-Pin Metal Can[e] ..... 450 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 11 mW/°C above 75°C
d. Derate 6.5 mW/°C above 25°C
e. Derate 6 mW/°C above 75°C

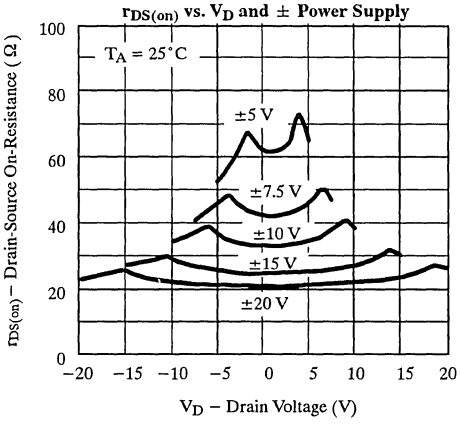
1

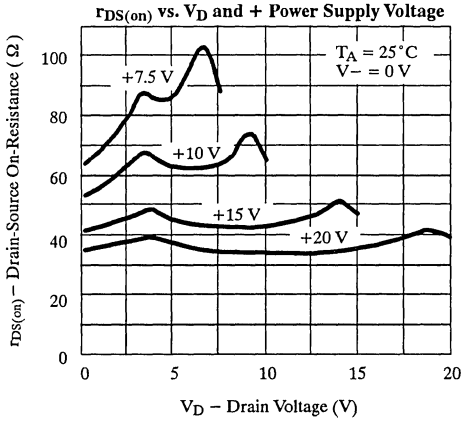
Specifications[a]

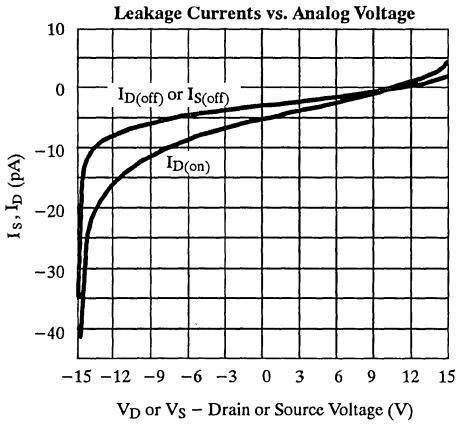
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 3.5 V or 11 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C Suffix −25 to 85°C 0 to 70°C Min[d]	B, C Suffix −25 to 85°C 0 to 70°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 10 mA	Room Full	30		50 75		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.1	−1 −100	1 100	−5 −100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.1	−1 −100	1 100	−5 −100	5 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Full	±0.1	−2 −200	2 200	−5 −200	5 200	nA
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Full	−0.001	−1 −1		−1		µA
		V_{IN} = 15 V	Room Full	0.001		1 1		1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	−0.001	−1 −1		−1		µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room	110		250			ns
Turn-Off Time	t_{OFF}	See Figure 2	Room	70		150			ns
Break-Before-Make Time	t_{OPEN}	DG305A/307A ONLY See Figure 3	Room	50					ns
Charge Injection	Q	C_L = 1 nF, R_{gen} = 0 V_{gen} = 0 V, See Figure 4	Room	30					pC
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V V_S, V_D = 0 V	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_S = 0 V V_S, V_D = 0 V	Room	14					pF
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz, V_S = 0 V V_S, V_D = 0 V	Room	40					pF
Input Capacitance	C_{IN}	f = 1 MHz, V_{IN} = 0 V	Room	6					pF
		f = 1 MHz, V_{IN} = 15 V	Room	7					pF
Off-Isolation	OIRR	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	62					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	74					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 15 V or 0 V (All Inputs)	Room Full	0.001		10 100		100	µA
Negative Supply Current	I−	V_{IN} = 15 V or 0 V (All Inputs)	Room Full	−0.001	−10 −100		−100		µA

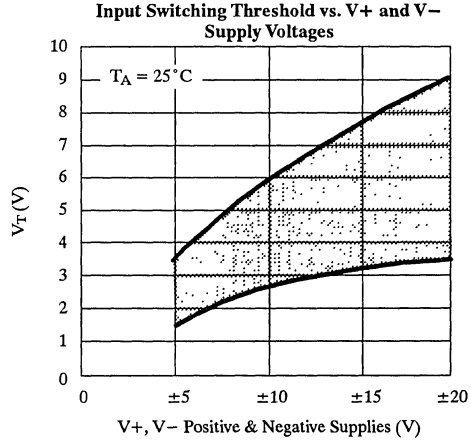
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

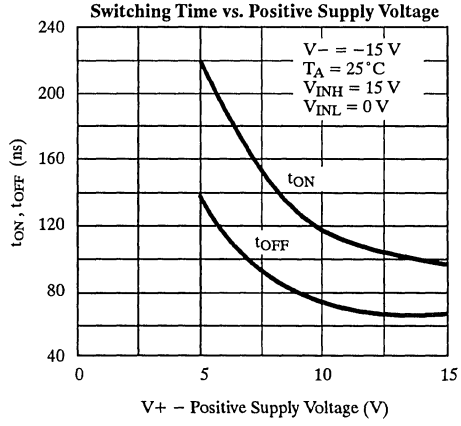
Typical Characteristics

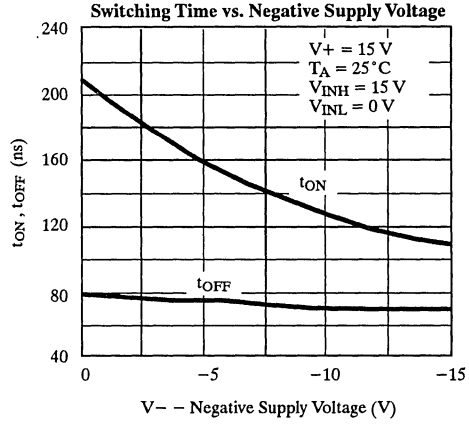












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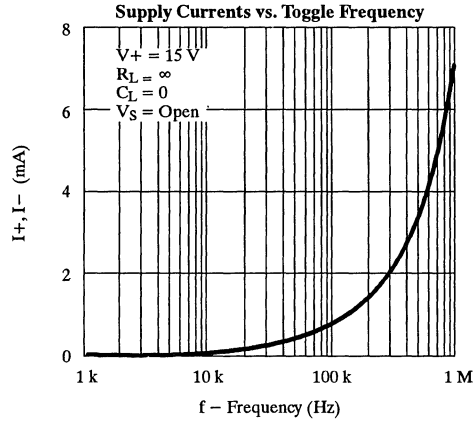
Typical Characteristics (Cont'd)



Schematic Diagram (Typical Channel)

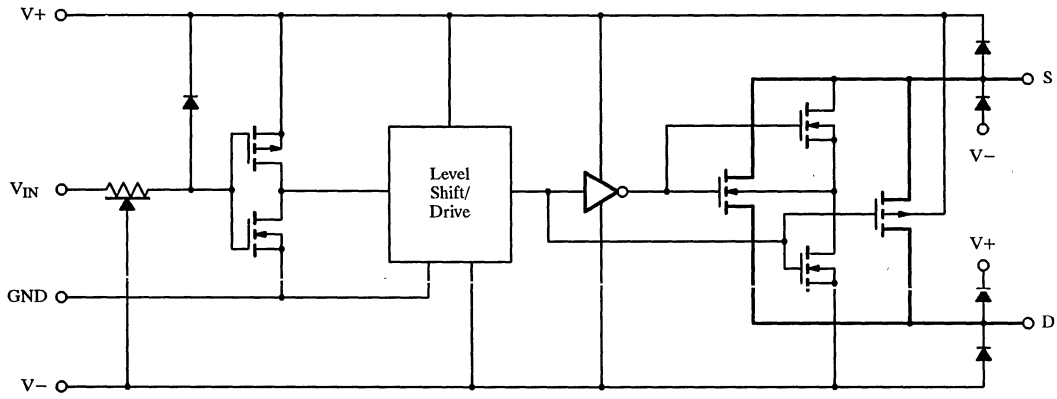
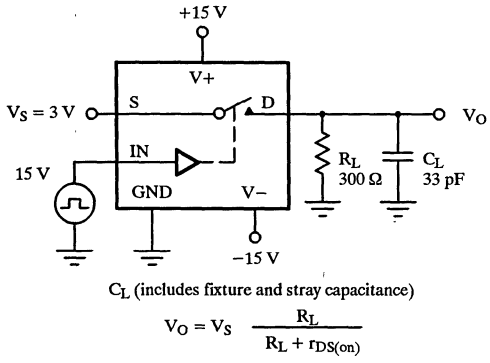


Figure 1.

Test Circuits



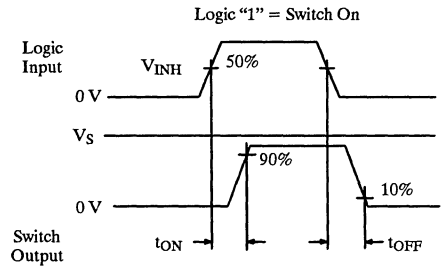
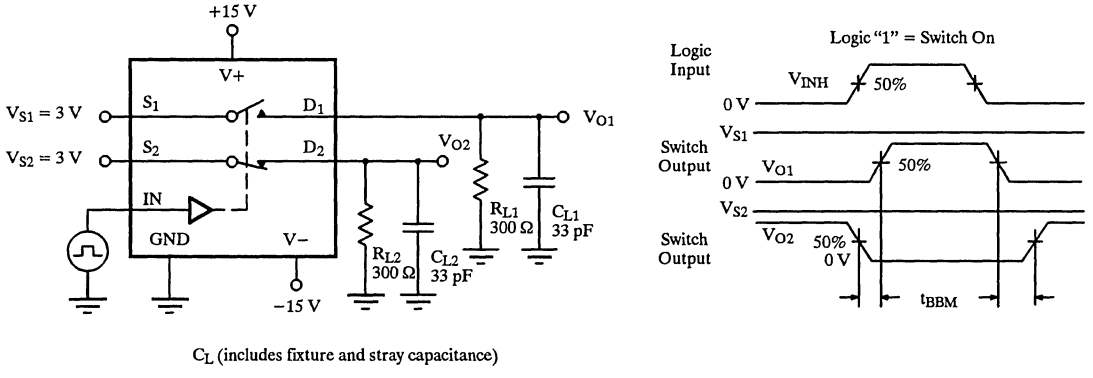


Figure 2. Switching Time

Test Circuits (Cont'd)



C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make SPDT (DG305A, DG307A)

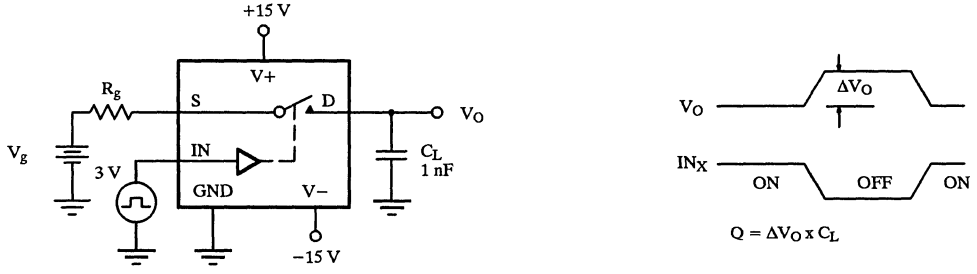


Figure 4. Charge Injection

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	GND Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	−15	0	11/3.5	−15 to 15
20	−20	0	11/3.5	−20 to 20
15	0	0	11/3.5	0 to 15

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

Applications

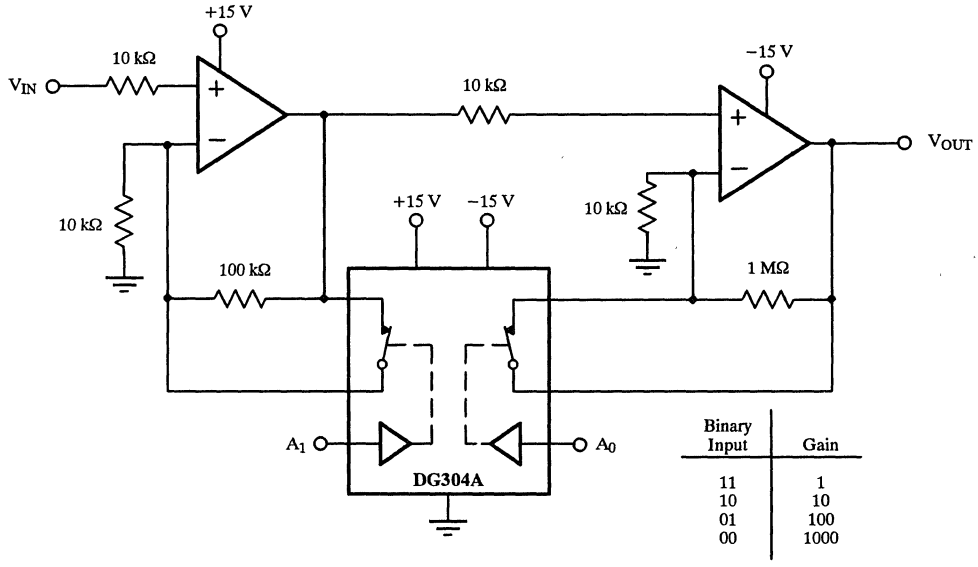


Figure 5. Low Power Binary to 10^n Gain Low Frequency Amplifier

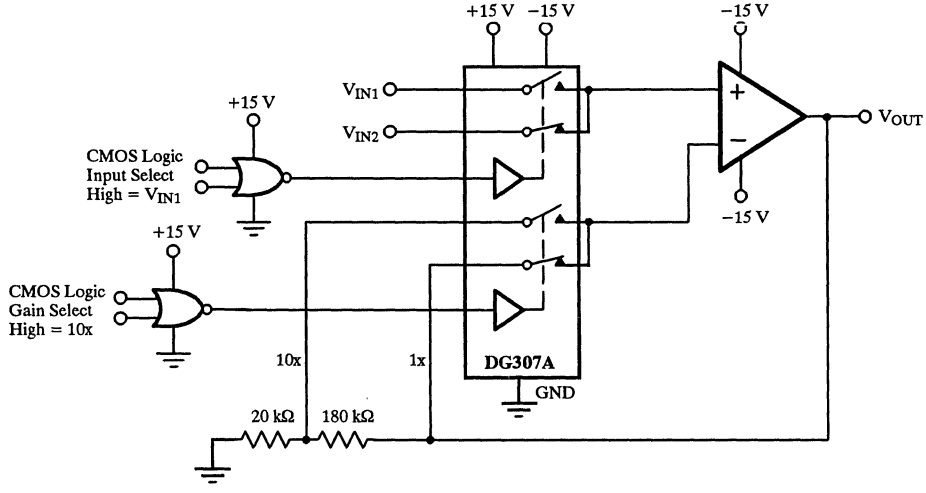


Figure 6. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain

DG308A/DG309

Quad Monolithic SPST CMOS Analog Switches

Features

- ±15-V Analog Input Range
- Low On-Resistance: 60 Ω
- Fast Switching: 130 ns
- Low Power Dissipation: 30 nW
- CMOS Logic Compatible

Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Single or Dual Supply Capability
- Static Protected Logic Inputs

Applications

- Portable and Battery Powered Instrumentation
- Communication Systems
- Computer Peripherals
- High-Speed Multiplexing

Description

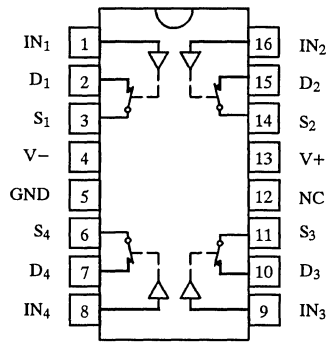
The DG308A and DG309 are quad single-pole single-throw analog switches designed for high speed switching applications in communications, instrumentation, and process control. This series is well suited for applications requiring a low on-resistance over the entire analog range.

Featuring low on-resistance (60 Ω) and fast switching (130 ns), the DG308A is supplied in the "normally open" configuration while DG309 is supplied "normally closed". Input thresholds are high voltage CMOS compatible.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latch up.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Four SPST Switches per Package

Truth Table

Logic	DG308A	DG309
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG308ACJ
		DG309CJ
−40 to 85°C	16-Pin Narrow SOIC	DG308ADY
		DG309DY
−55 to 125°C	16-Pin CerDIP	DG308AAK
		DG308AAK/883
		DG309AK/883

1

Absolute Maximum Ratings

Voltages Referenced to V–
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V–) –2 V to (V+) +2V or 20 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA
Storage Temperature (AK Suffix) ..... –65 to 150°C
(CJ and DY Suffix) ..... –65 to 125°C

Power Dissipation[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[e] ..... 600 mW
16-Pin Cerdip[d] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 12 mW/°C above 75°C
d. Derate 6.5 mW/°C above 25°C
e. Derate 7.6 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 3.5 V or 11 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	C, D Suffix Min[d]	C, D Suffix Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room Full	60		100 150		100 125	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.1	–1 –100	1 100	–5 –100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	±0.1	–1 –100	1 100	–5 –100	5 100	
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Full	±0.1	–1 –100	1 100	–5 –200	5 200	
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 15 V	Full	0.001		1		1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Full	–0.001	–1		–1		
Input Capacitance	C_{IN}		Room	8					pF
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room	130		200		200	ns
Turn-Off Time	t_{OFF}		Room	90		150		150	
Charge Injection	Q	C_L = 0.01 µF, R_{gen} = 0 Ω, V_{gen} = 0 V	Room	–10					pC
Source-Off Capacitance	$C_{S(off)}$	f = 140 kHz, V_S, V_D = 0 V	Room	11					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	8					
Channel-On Capacitance	$C_{D(on)}$		Room	27					
Off-Isolation[f]	OIRR	R_L = 75 , V_S = 2 V_{p-p}, f = 500 kHz	Room	78					dB

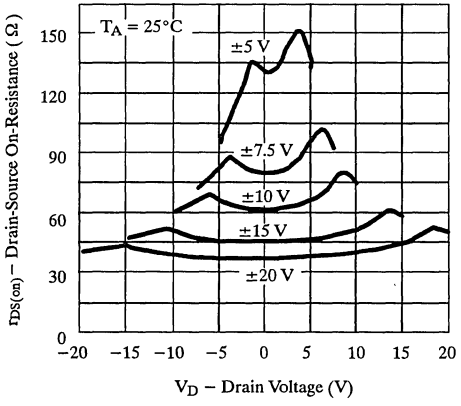
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 3.5 V or 11 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	C, D Suffix Min[d]	C, D Suffix Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	All Channels On or Off V_{IN} = 0 V or 15 V	Room Full	0.001		10 100		10 100	µA
Negative Supply Current	I−		Room Full	−0.001	−10 −100		−100		

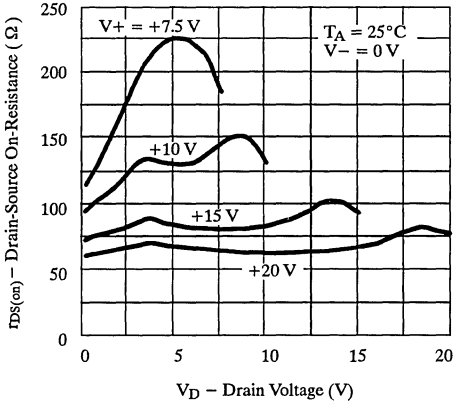
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

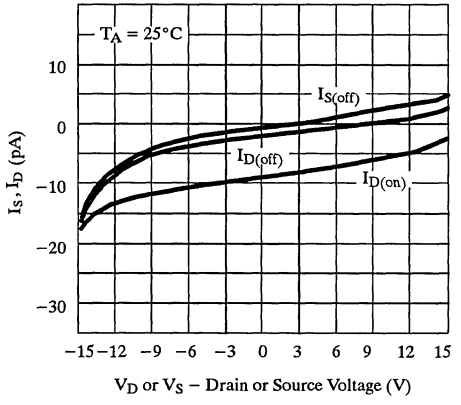
$r_{DS(on)}$ vs. V_D and Power Supply



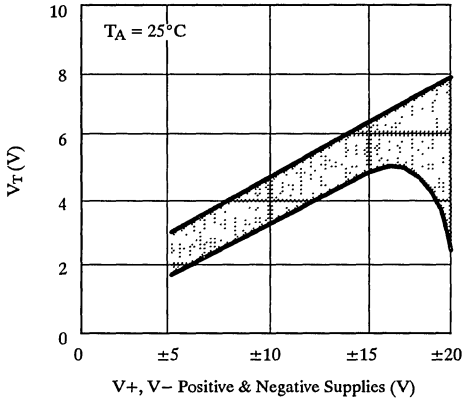
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



Leakage Currents vs. Analog Voltage



Input Switching Threshold vs. V+ and V− Supply Voltages



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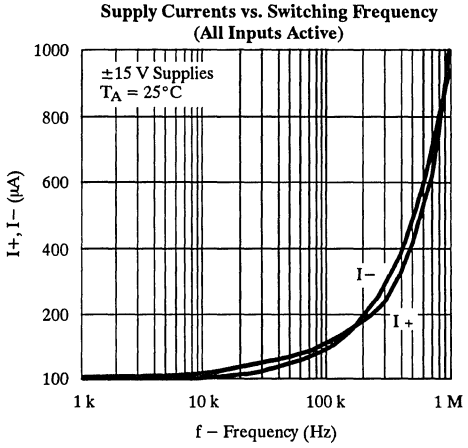
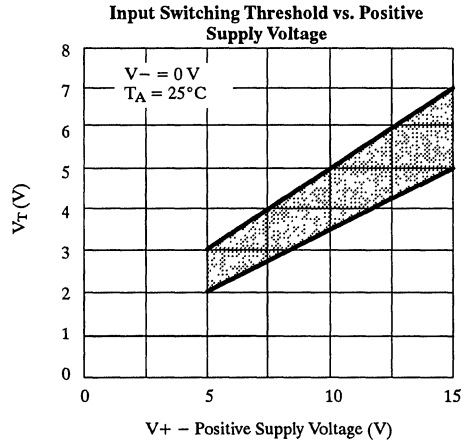
Typical Characteristics (Cont'd)





Schematic Diagram (Typical Channel)

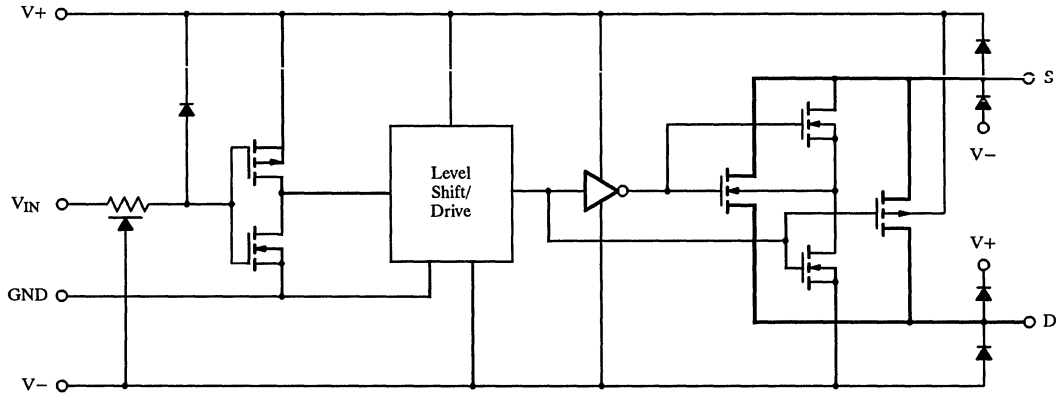
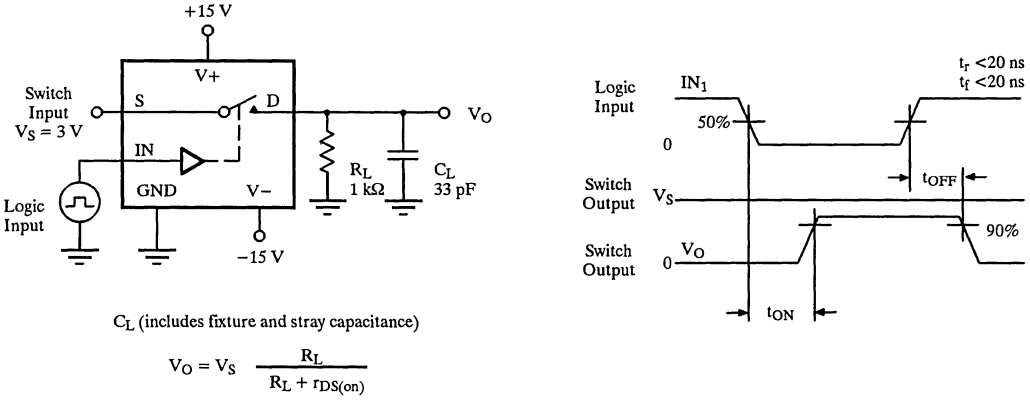


Figure 1.

Test Circuits



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

Applications

Single Supply Operation

The DG308A and DG309 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased $r_{DS(on)}$ and 2) slower switching speed. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single supply operation are V+ and 0 V.

Siliconix
A Member of the TEMIC Group

Improved Quad CMOS Analog Switches

Features

- ±22-V Supply Voltage Rating
- CMOS Compatible Logic
- Low On-Resistance—$r_{DS(on)}$: 45 Ω
- Low Leakage—$I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching—t_{ON}: < 200 ns
- Low Glitching—Q: 1 pC

Benefits

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG308A/309

Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

Description

The DG308B/309B analog switches are highly improved versions of the industry-standard DG308A/309. These devices are fabricated in Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG308B and DG309B can handle up to ±22-V input signals. An epitaxial layer prevents latchup.

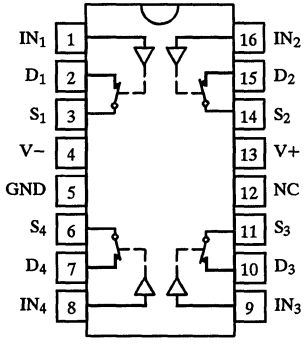
All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG308B is a normally open switch and the DG309B is a normally closed switch. (See Truth Table.)

Functional Block Diagram and Pin Configuration

DG308B

Dual-In-Line



Top View

Truth Table

Logic	DG308B	DG309B
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5V
Logic "1" ≥ 11 V

Switches Shown for DG308B Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG308BDJ
		DG309BDJ
	16-Pin Narrow SOIC	DG308BDY
		DG309BDY
−55 to 125°C	16-Pin CerDIP	DG308BAK
		DG308BAK/883
		DG309BAK
		DG309BAK/883

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 30 mA, whichever occurs first
Current, Any Terminal ..... 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Storage Temperature (AK, Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 640 mW
16-Pin CerDIP[e] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{IN} = 11 V, 3.5 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room Full	45		85 100		85 100	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room	2					%
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	±0.01	−0.5 −20	0.5 20	−0.5 −5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	±0.01	−0.5 −20	0.5 20	−0.5 −5	0.5 5	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room Full	±0.02	−0.5 −40	0.5 40	−0.5 −10	0.5 10	
Digital Control									
Input Voltage High	V_{INH}		Full		11		11		V
Input Voltage Low	V_{INL}		Full			3.5		3.5	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full		−1	1	−1	1	µA
Input Capacitance	C_{IN}		Room	5					pF
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = 3 V, See Figure 2	Room			200		200	ns
Turn-Off Time	t_{OFF}		Room			150		150	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room	1					pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, f = 1 MHz	Room	16					
Off Isolation	OIRR	C_L = 15 pF, R_L = 50 Ω V_S = 1 V_{RMS}, f = 100 kHz	Room	90					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	95					

1

Specifications[a]

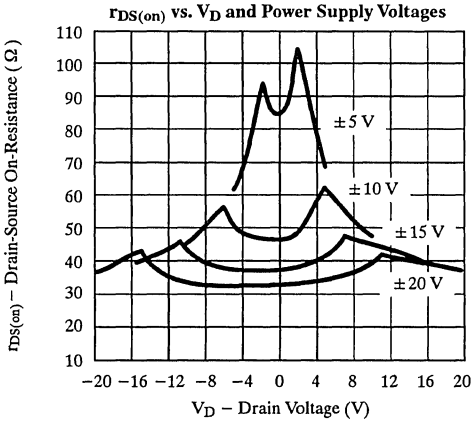
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 11 V, 3.5 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Power Supply									
Positive Supply Current	I+	V_{IN} = 0 or 15 V	Room Full			1 5		1 5	µA
Negative Supply Current	I−		Room Full		−1 −5		−1 −5		
Power Supply Range for Continuous Operation	V_{OP}		Full		±4	±22	±4	±22	V

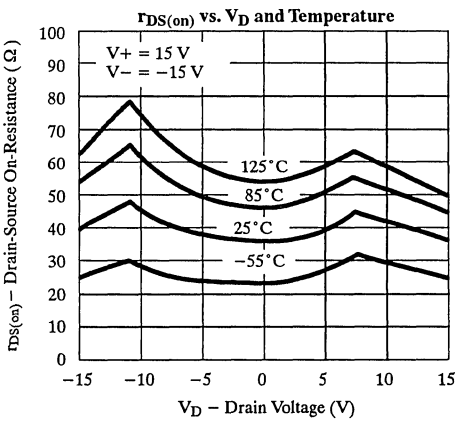
Specifications[a] for Single Supply

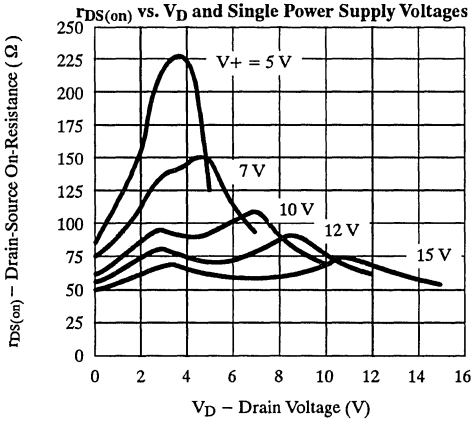
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{IN} = 11 V, 3.5 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 8 V, I_S = 1 mA	Room Full	90		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = 8 V, See Figure 2	Room			300		300	ns
Turn-Off Time	t_{OFF}		Room			200		200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	4					pC
Power Supply									
Positive Supply Current	I+	V_{IN} = 0 or 12 V	Room Full			1 5		1 5	µA
Negative Supply Current	I−		Room Full		−1 −5		−1 −5		
Power Supply Range for Continuous Operation	V_{OP}		Full		4	44	4	44	V

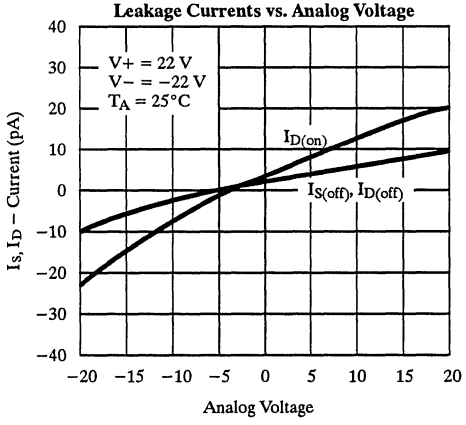
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

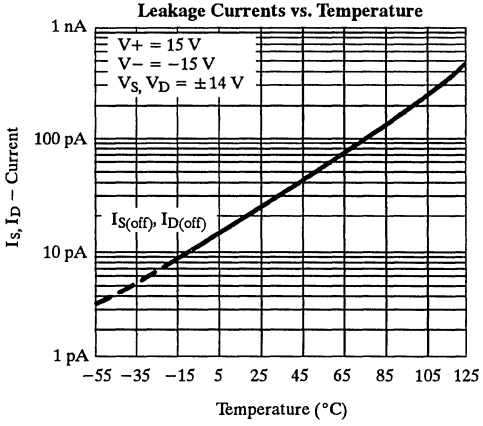
Typical Characteristics

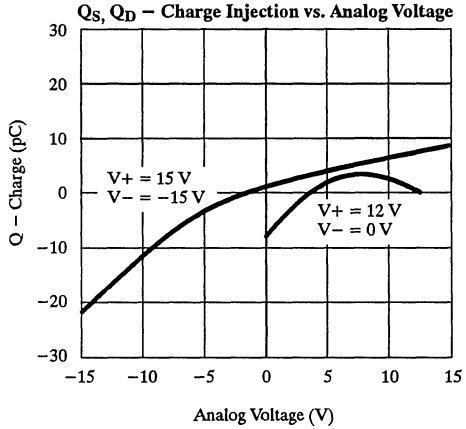












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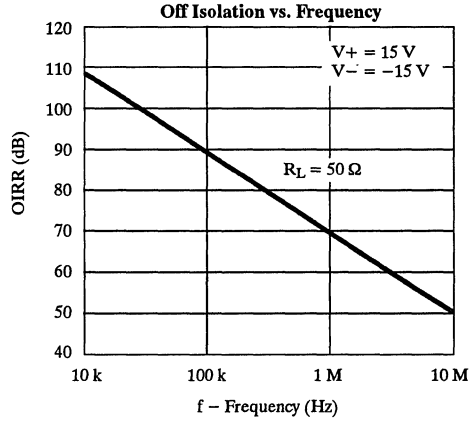
Typical Characteristics (Cont'd)



Schematic Diagram (Typical Channel)

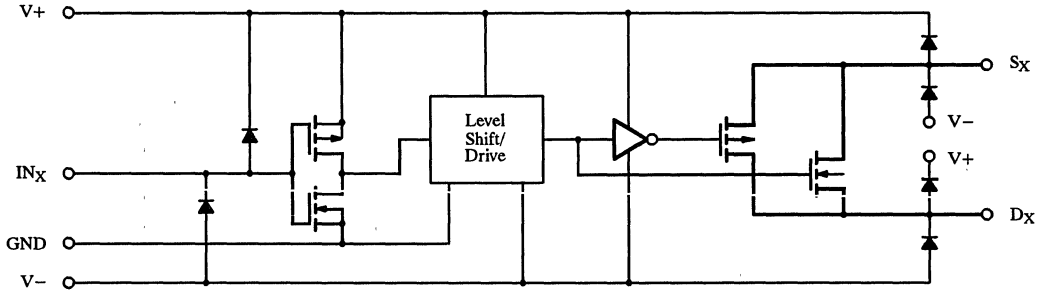
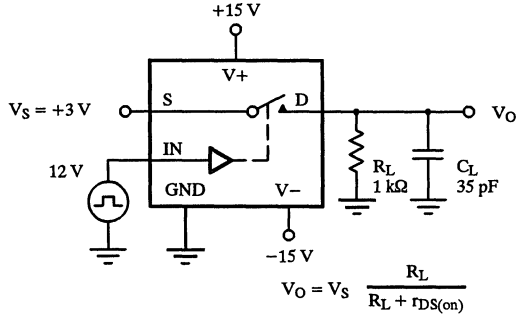


Figure 1.

Test Circuits



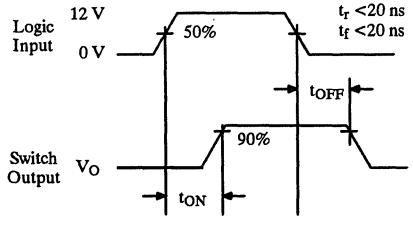


Figure 2. Switching Time

Test Circuits (Cont'd)

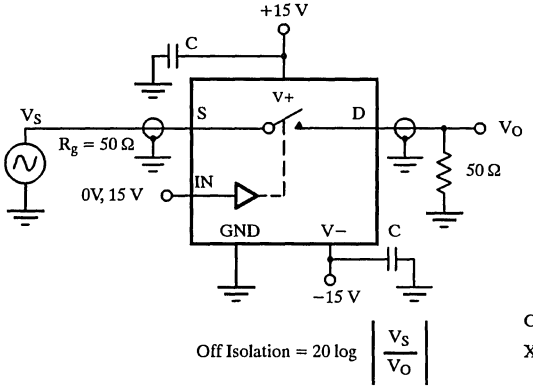


Figure 3. Off Isolation

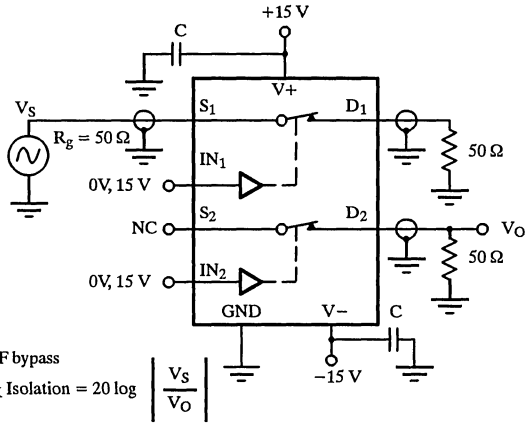
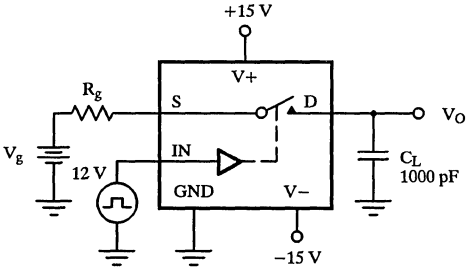
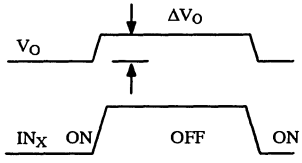


Figure 4. Channel-to-Channel Crosstalk





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

Figure 5. Charge Injection

Applications

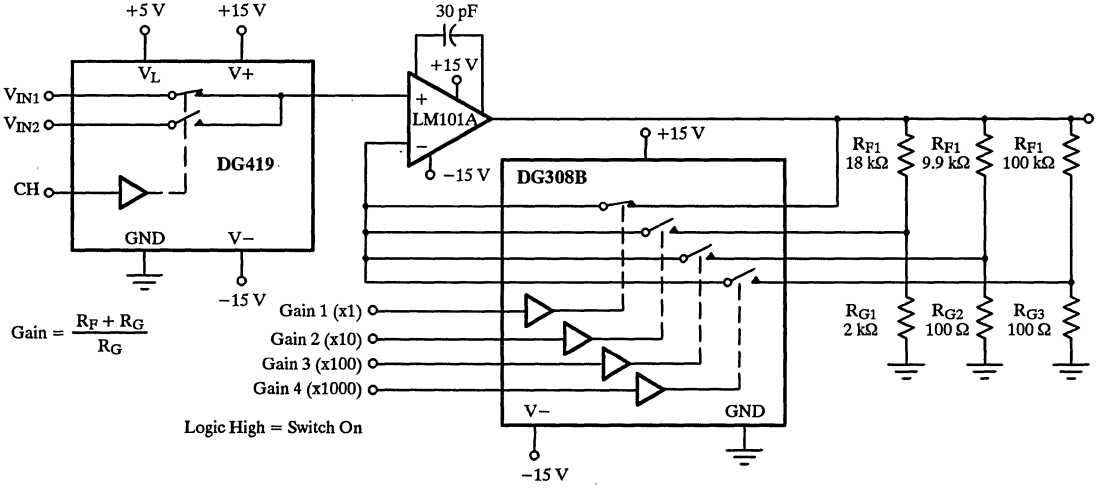


Figure 7. A Precision Amplifier with Digitally Programmable Inputs and Gains

Applications (Cont'd)

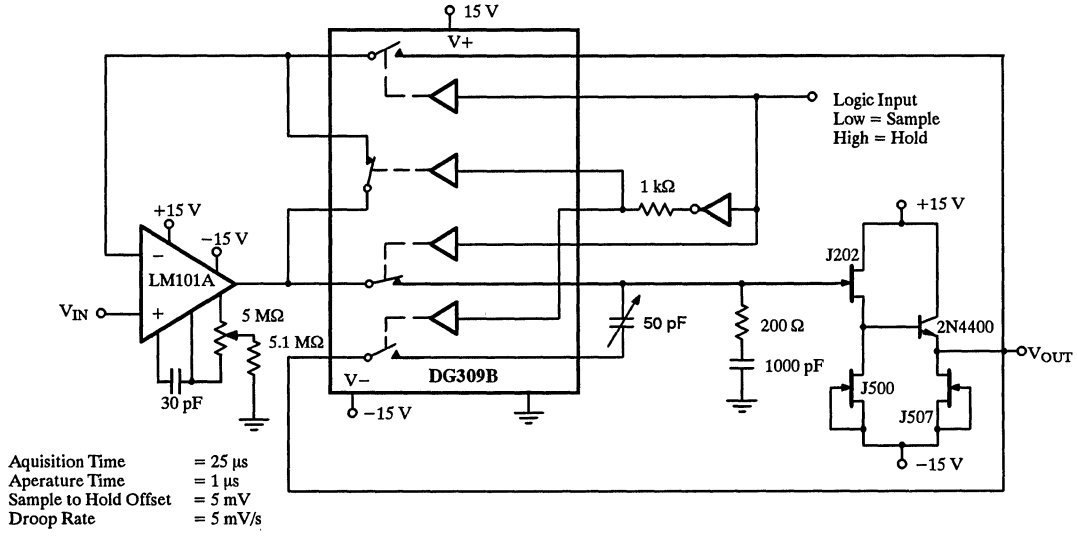
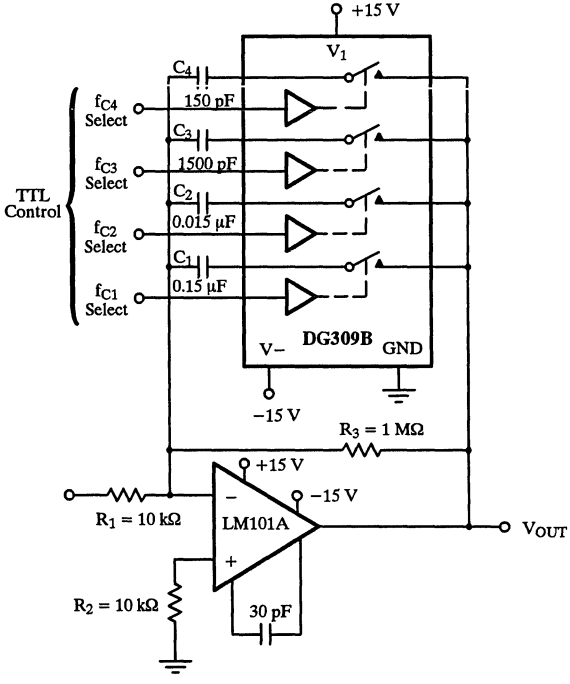
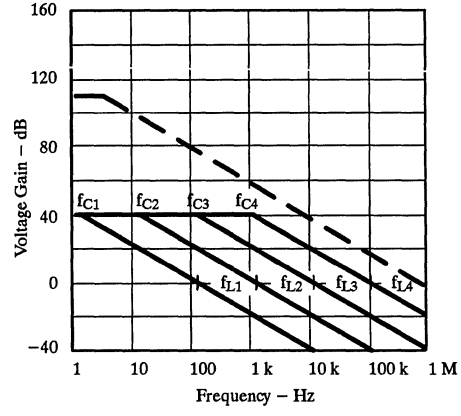


Figure 8. Sample-and-Hold





A_L (Voltage Gain Below Break Frequency) = $\frac{R_3}{R_1}$ = 100 (40 dB)

f_C (Break Frequency) = $\frac{1}{2\pi R_3 C_X}$

f_L (Unity Gain Frequency) = $\frac{1}{2\pi R_1 C_X}$

Max Attenuation = $\frac{r_{DS(on)}}{10\ k\Omega} \approx -40$ dB

Figure 9. Active Low Pass Filter with Digitally Selected Break Frequency

DG381A/384A/387A/390A

CMOS Analog Switches

Features

- ±15-V Input Range
- Low $r_{DS(on)}$: 30 Ω
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

Benefits

- Full Rail-to-Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Sytems

Description

The DG381A–DG390A series of monolithic CMOS analog switches was designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat on-resistance over the entire voltage range.

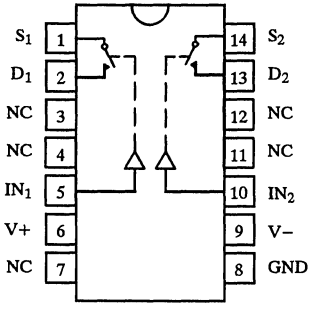
Designed on Siliconix' PLUS-40 CMOS process, these devices achieve low power consumption (3.5 mW typical) and excellent on/off switch performance. These switches are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation is allowed by connecting the V– rail to 0 V.

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS and quasi TTL logic compatible.

Functional Block Diagram and Pin Configuration

DG381A

Dual-In-Line



Top View

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

Ordering Information – DG381A

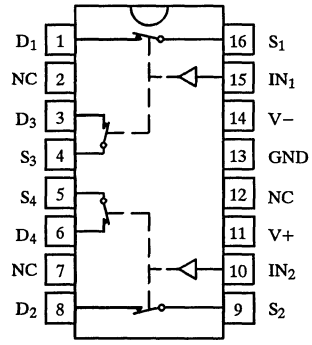
Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG381ACJ
–55 to 125°C	14-Pin CerDIP	DG381AAK/883

1

Functional Block Diagram and Pin Configuration (Cont'd)

DG384A

Dual-In-Line



Top View

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

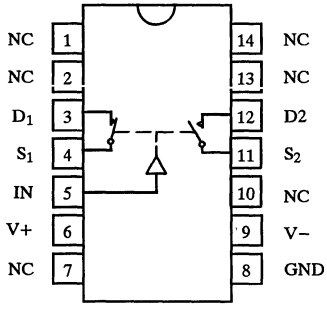
Switches Shown for Logic "1" Input

Ordering Information – DG384A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG384ACJ
−55 to 125°C	16-Pin CerDIP	DG384AAK/883

DG387A

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

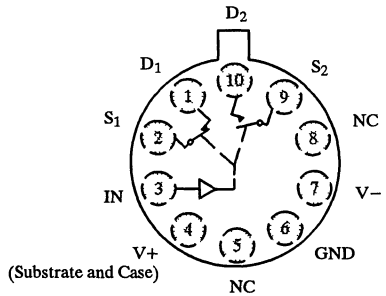
Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

Ordering Information – DG387A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG387ACJ
−55 to 125°C	14-Pin CerDIP	DG387AAK/883
	10-Pin Metal Can	DG387AAA/883

Metal Can

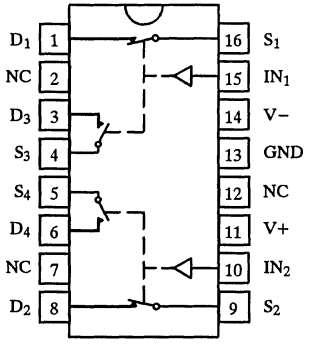


Top View

Functional Block Diagram and Pin Configuration (Cont'd)

DG390A

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V
Switches Shown for Logic "1" Input

Ordering Information – DG390A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG390ACJ
−25 to 85°C	16-Pin CerDIP	DG390ABK
−55 to 125°C		DG390AAK
		DG390AAK/883

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2V or 30 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 30 mA
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Storage Temperature (AAA, AAK, ACK Suffix) . −65 to 150°C
(ACJ Suffix) ..... −65 to 125°C

Power Dissipation[b]
14-Pin Plastic DIP[d] ..... 470 mW
14-Pin CerDIP[c] ..... 825 mW
10-Pin Metal Can[e] ..... 450 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 11 mW/°C above 75°C
d. Derate 6.5 mW/°C above 25°C
e. Derate 6 mW/°C above 75°C

Specifications[a]

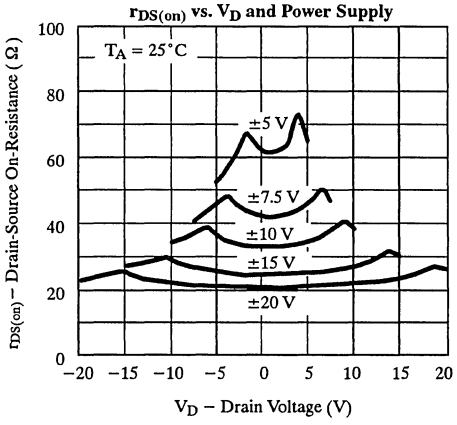
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{IN} = 0.8 V or 4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C Suffix 0 to 70°C, −25 to 85°C Min[d]	B, C Suffix 0 to 70°C, −25 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −10 mA	Room Full	30		50 75		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	±0.1	−1 −100	1 100	−5 −100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	±0.1	−1 −100	1 100	−5 −100	5 100	
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Hot	±0.1	−11 −100	1 100	−5 −100	5 100	

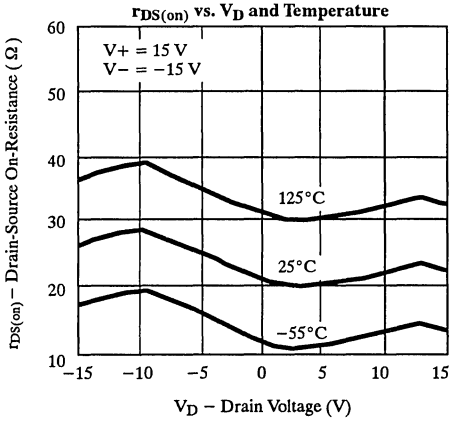
Specifications[a]

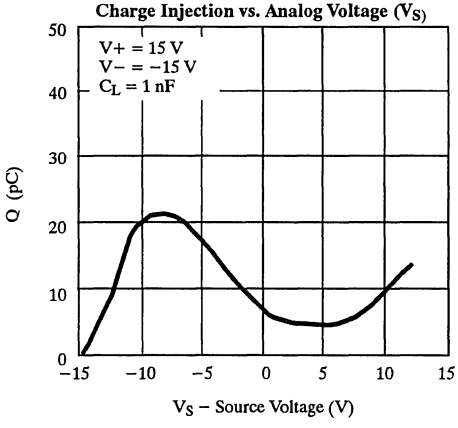
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 0.8 V or 4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C Suffix 0 to 70°C −25 to 85°C Min[d]	B, C Suffix 0 to 70°C −25 to 85°C Max[d]	Unit
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Full	−0.001	−1 −1		−1		µA
		V_{IN} = 15 V	Room Full	0.001		1 1		1	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	−0.001	−1 −1		−1		
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room	150		300			ns
Turn-Off Time	t_{OFF}		Room	130		250			
Break-Before-Make Time	t_{OPEN}	See Figure 3	Room	50					
Charge Injection	Q	C_L = 0.01 µF, R_{gen} = 0 Ω V_{gen} = 0 V	Room	10					pC
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz; V_S, V_D = 0 V	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	14					
Channel-On Capacitance	$C_{D(on)}$		Room	40					
Input Capacitance	C_{IN}	f = 1 MHz, V_{IN} = 0 V	Room	6					
		f = 1 MHz, V_{IN} = 15 V	Room	7					
Off-Isolation	OIRR	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	62					dB
Crosstalk (Channel-to-Channel)	X_{TALK}		Room	74					
Power Supplies									
Positive Supply Current	I+	V_{IN} = 4 V (One Input) (All Others = 0)	Room Full	0.23		0.5 1.0		1	mA
Negative Supply Current	I−		Room Full	−0.001	−10 −100		−100		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)	Room Full	0.001		10 100		100	
Negative Supply Current	I−		Room Full	−0.001	−10 −100		−100		

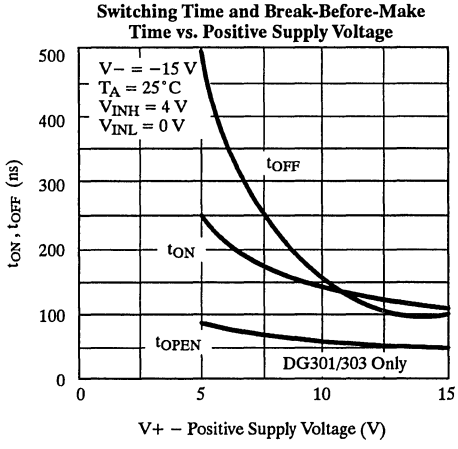
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

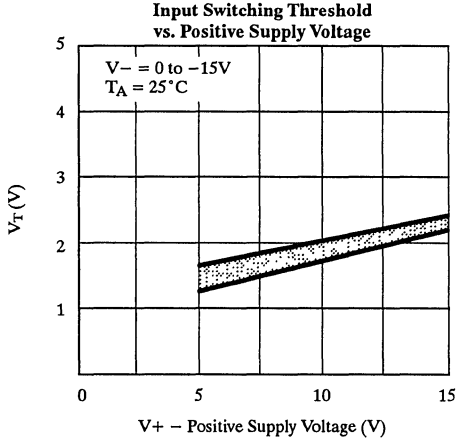
Typical Characteristics

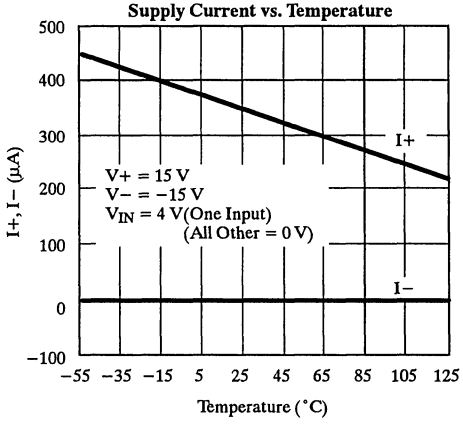






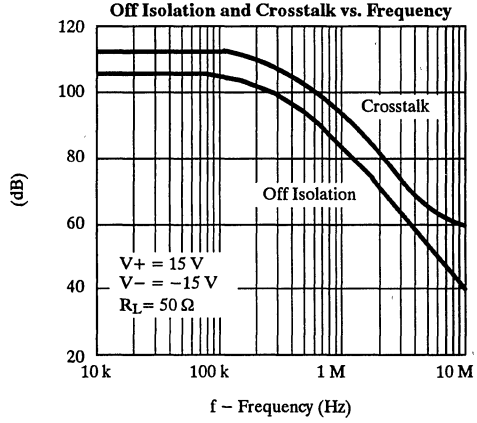




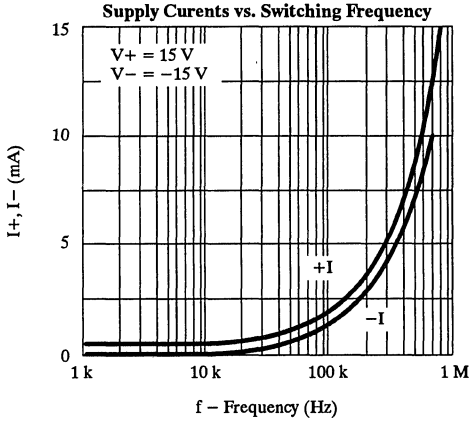


Typical Characteristic (Cont'd)

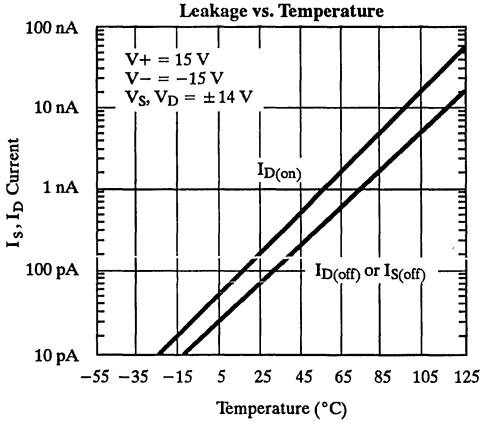
Off Isolation and Crosstalk vs. Frequency



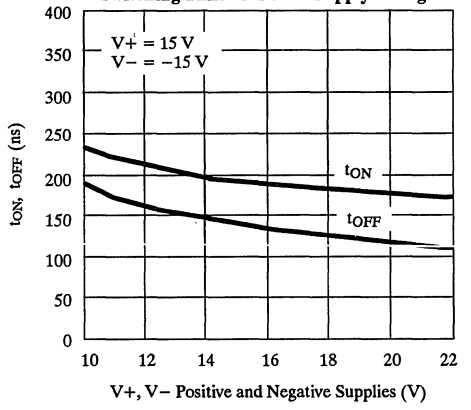
Supply Curents vs. Switching Frequency



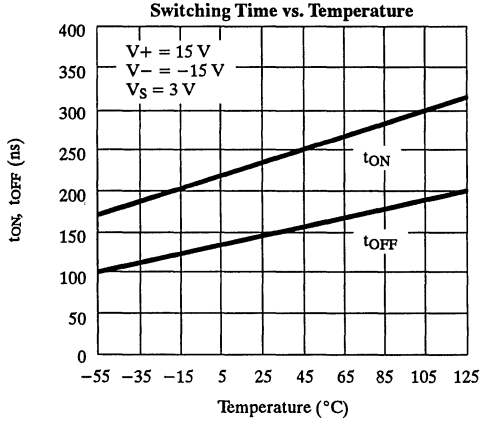
Leakage vs. Temperature



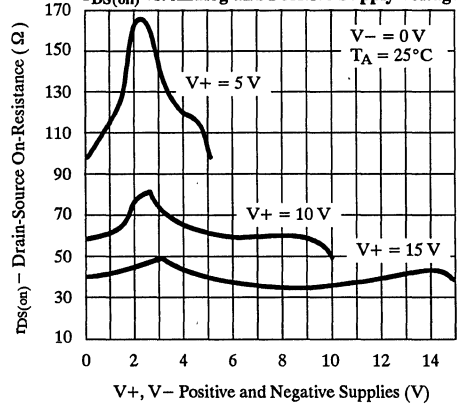
Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature



rDS(on) vs. Analog and Positive Supply Voltage



Schematic Diagram (Typical Channel)

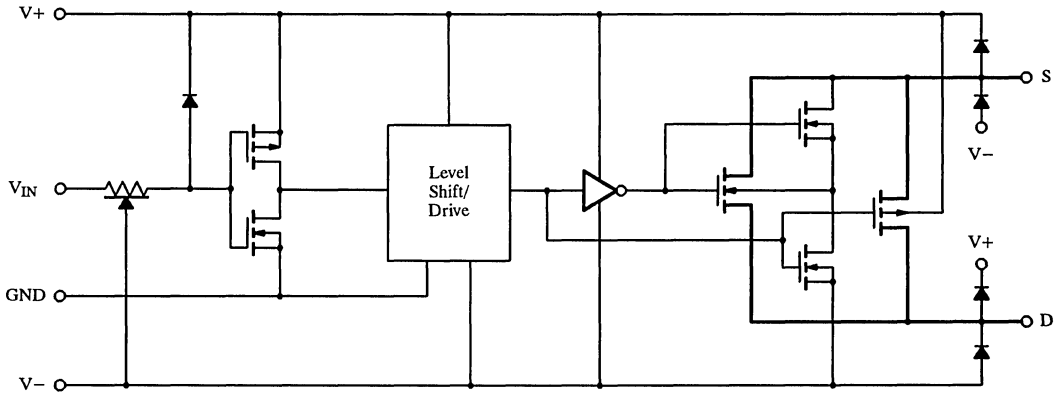
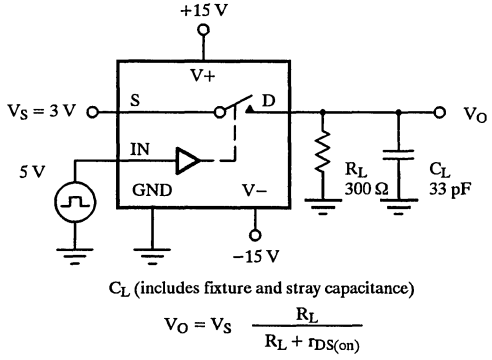


Figure 1.

Test Circuits



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

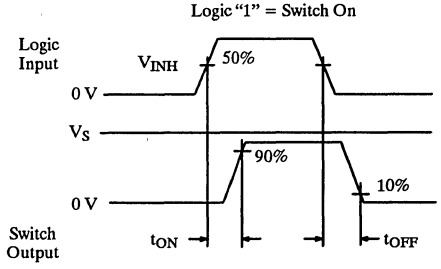
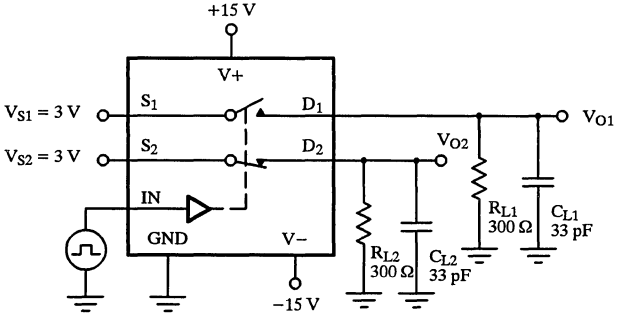


Figure 2. Switching Time



C_L (includes fixture and stray capacitance)

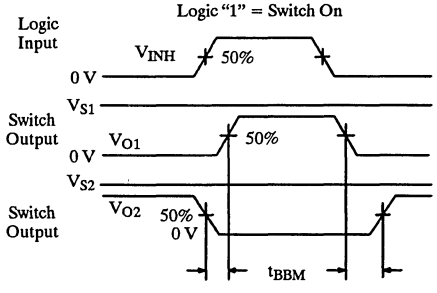


Figure 3. Break-Before-Make SPDT (DG301A, DG303A)

Test Circuits (Cont'd)

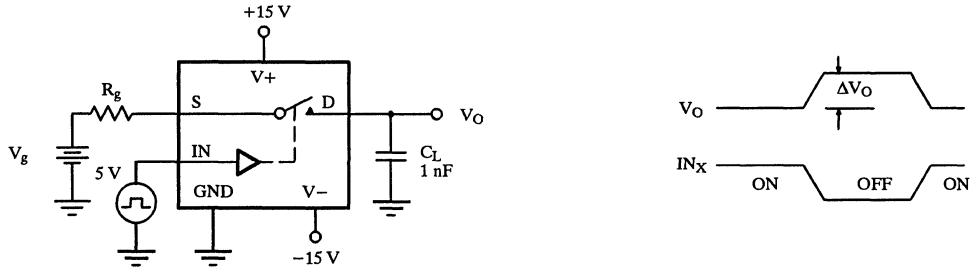


Figure 4. Charge Injection

Applications

The DG381A series of analog switches will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased $r_{DS(on)}$, 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied (see Typical Characteristics). The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V.

In the integrator of Figure 4, R_D controls the discharge rate of the capacitor so that the pulsed or continuous current ratings are not exceeded. During reset SW_1 is closed and SW_2 is open. Opening SW_2 with SW_1 also open will hold the integrator output at its present value.

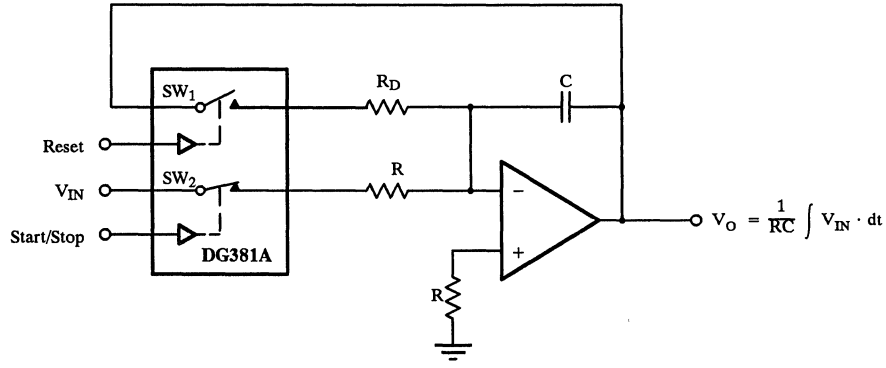


Figure 5. Integrator with Reset and Start/Stop

Low-Power, High-Speed CMOS Analog Switches

Features

- 44-V Supply Max Rating
- ± 15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 20 Ω
- Low Leakage—$I_{D(on)}$: 40 pA
- Fast Switching—t_{ON}: 100 ns
- Ultra Low Power Requirements—P_D: 0.35 µW
- TTL, CMOS Compatible
- Single Supply Capability

Benefits

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

Applications

- Audio and Video Switching
- Sample-and-Hold Circuits
- Battery Operation
- Test Equipment
- Hi-Rel Systems
- PBX, PABX

Description

The DG401/403/405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35 µW, typ) with high speed (t_{ON}: 100 ns, typ), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

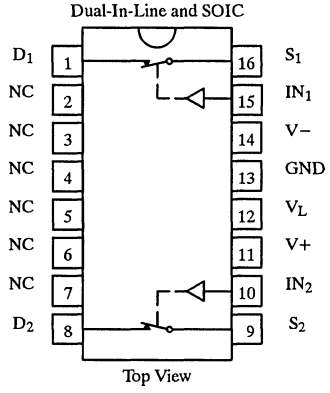
Built on the Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ± 15-V analog range, rivaling JFET performance without the inherent dynamic range limitations.

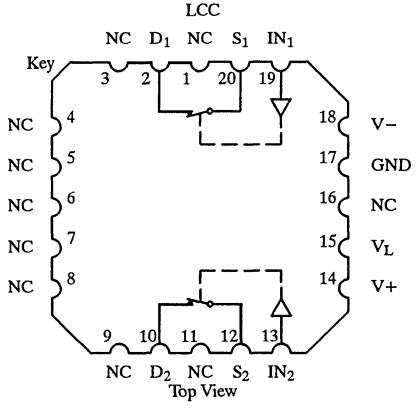
The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

Functional Block Diagrams and Pin Configurations

DG401



DG401



Ordering Information – DG401

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG401DJ
−55 to 125°C	16-Pin CerDIP	DG401AK
		DG401AK/883
	LCC-20	DG401AZ/883

Two SPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

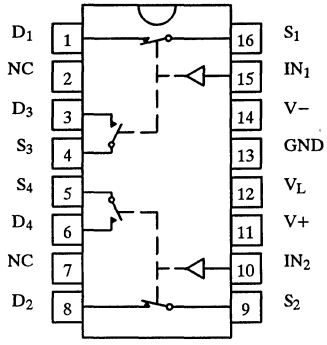
Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

Functional Block Diagrams and Pin Configurations (Cont'd)

DG403

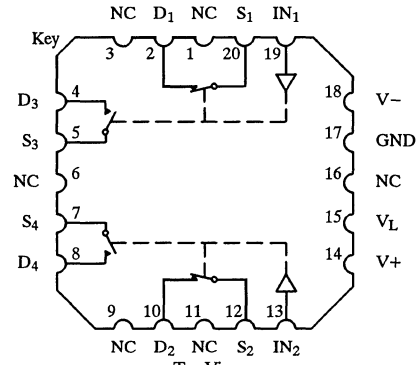
Dual-In-Line and SOIC



Top View

DG403

LCC



Top View

Ordering Information – DG403

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG403DJ
	16-Pin Narrow SOIC	DG403DY
−55 to 125°C	16-Pin CerDIP	DG403AK
		DG403AK/883
	LCC-20	DG403AZ/883

Two SPDT Switches per Package

Truth Table

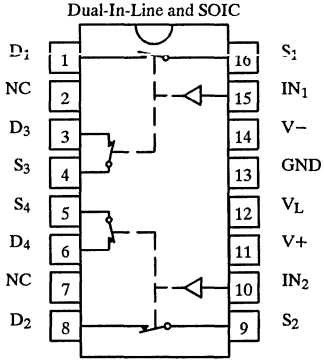
Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

DG405

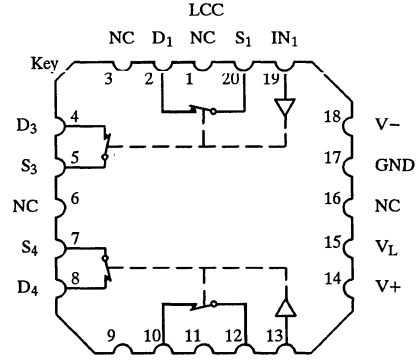
Dual-In-Line and SOIC



Top View

DG405

LCC



Top View

Ordering Information – DG405

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG405DJ
	16-Pin Narrow SOIC	DG405DY
−55 to 125°C	16-Pin CerDIP	DG405AK
		DG405AK/883
	LCC-20	DG405AZ/883

Two DPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
V_L ..... (GND − 0.3 V) to (V+) +0.3 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA
Storage Temperature (AK, AZ Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 450 mW
16-Pin CerDIP[d] ..... 900 mW
16-Pin SOIC[e] ..... 600 mW
LCC-20[f] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C
e. Derate 7.6 mW/°C above 75°C
f. Derate 13 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±10 V V+ = 13.5 V, V− = −13.5 V	Room Full	20		35 45		45 55	Ω
Δ Drain-Source On-Resistance	$\Delta r_{DS(on)}$	I_S = −10 mA, V_D = ±5 V, 0 V V+ = 16.5 V, V− = −16.5 V	Room Full	3		3 5		3 5	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V− = −16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Hot	−0.01	−0.25 −20	0.25 20	−0.5 −5	0.5 5	nA
	$I_{D(off)}$		Room Hot	−0.01	−0.25 −20	0.25 20	−0.5 −5	0.5 5	nA
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V V_S = V_D = ±15.5 V	Room Hot	−0.04	−0.4 −40	0.4 40	−1 −10	1 10	nA
Digital Control									
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V	Full	0.005	−1	1	−1	1	µA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	0.005	−1	1	−1	1	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	100		150		150	ns
Turn-Off Time	t_{OFF}		Room	60		100		100	ns
Break-Before-Make Time Delay (DG403)	t_D	R_L = 300 Ω, C_L = 35 pF	Room	12	5		5		ns
Charge Injection	Q	C_L = 10,000 pF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60					pC
Off Isolation Reject Ratio	OIRR	R_L = 100 Ω, C_L = 5 pF f = 1 MHz	Room	72					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	90					dB

1

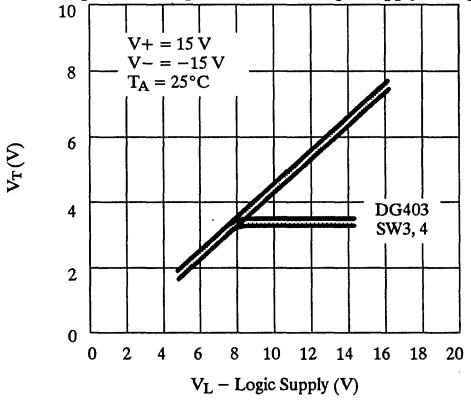
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	12					pF
Drain Off Capacitance	$C_{D(off)}$		Room	12					
Channel On Capacitance	C_D, $C_{S(on)}$		Room	39					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V	Room Full	0.01		1 5		1 5	µA
Negative Supply Current	I−		Room Full	−0.01	−1 −5		−1 −5		
Logic Supply Current	I_L		Room Full	0.01		1 5		1 5	
Ground Current	I_{GND}		Room Full	−0.01	−1 −5		−1 −5		

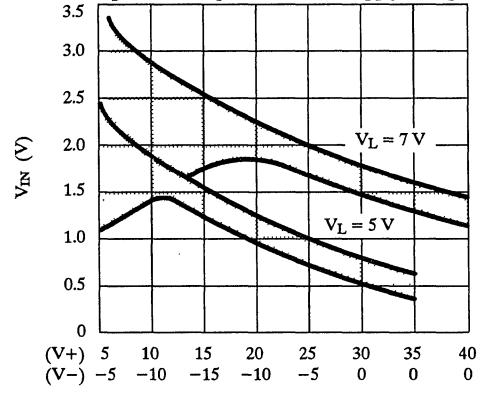
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

Input Switching Threshold vs. Logic Supply Voltage

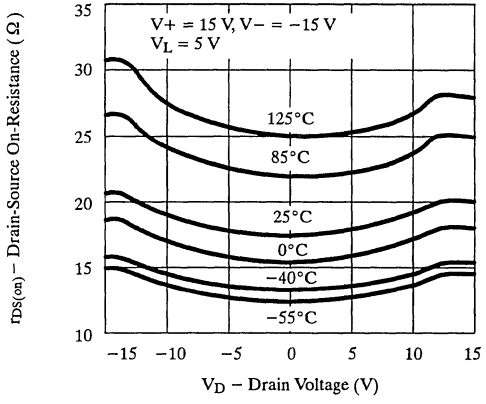


Input Switching Threshold vs. Supply Voltages

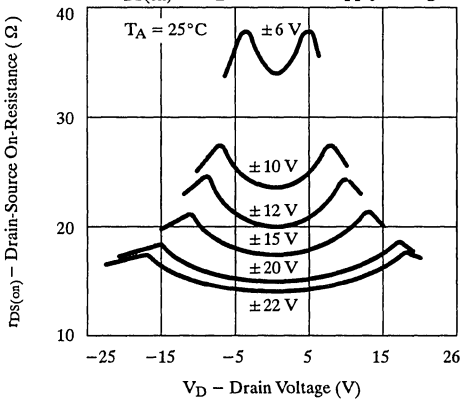


Typical Characteristics (Cont'd)

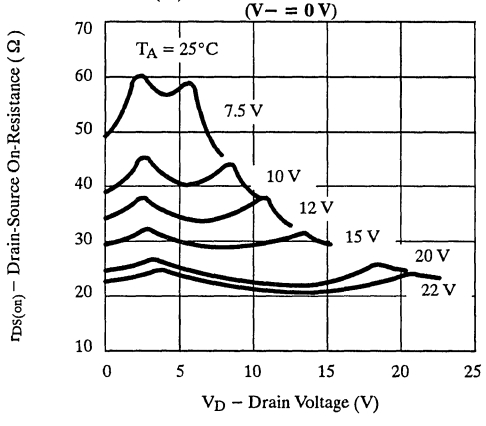
$r_{DS(on)}$ vs. V_D and Temperature



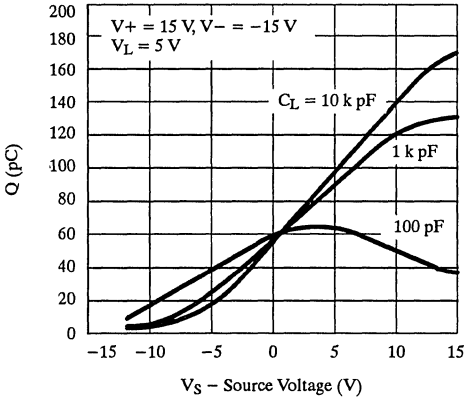
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



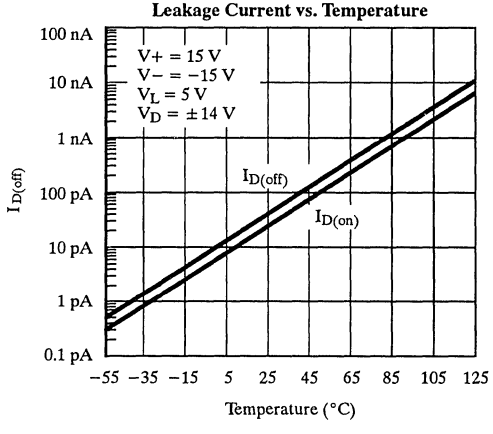
$r_{DS(on)}$ vs. V_D and Power Supply Voltage ($V- = 0$ V)



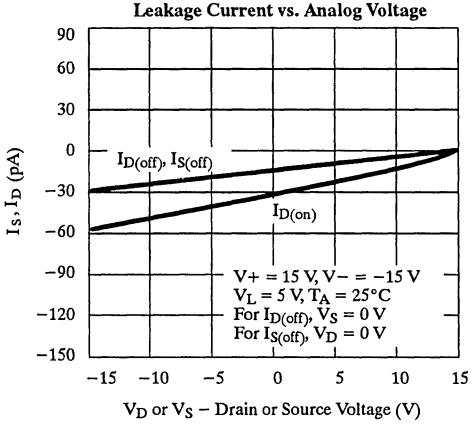
Charge Injection vs. Analog Voltage



Leakage Current vs. Temperature

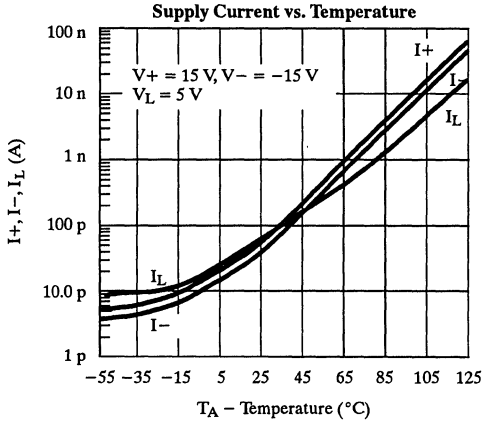


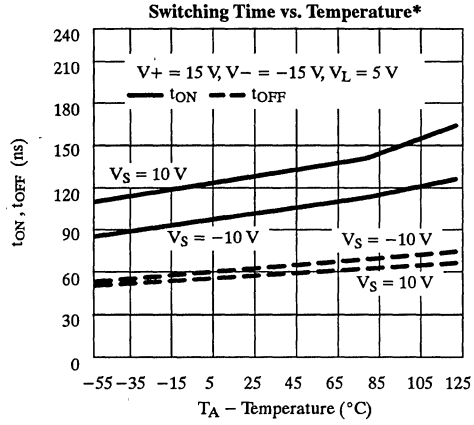
Leakage Current vs. Analog Voltage

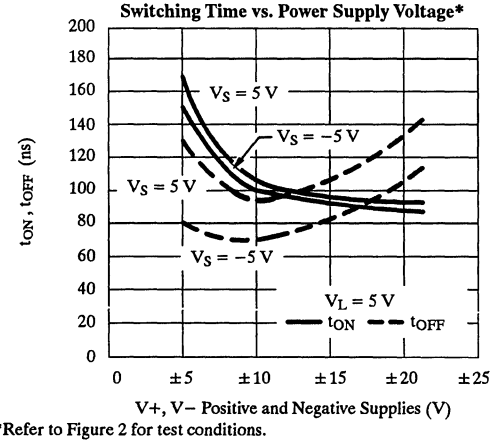


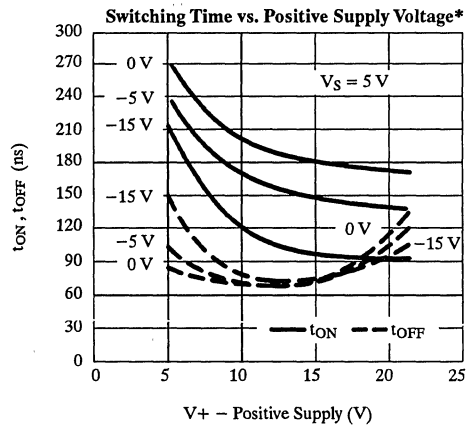
1

Typical Characteristics (Cont'd)









*Refer to Figure 2 for test conditions.

Schematic Diagram (Typical Channel)

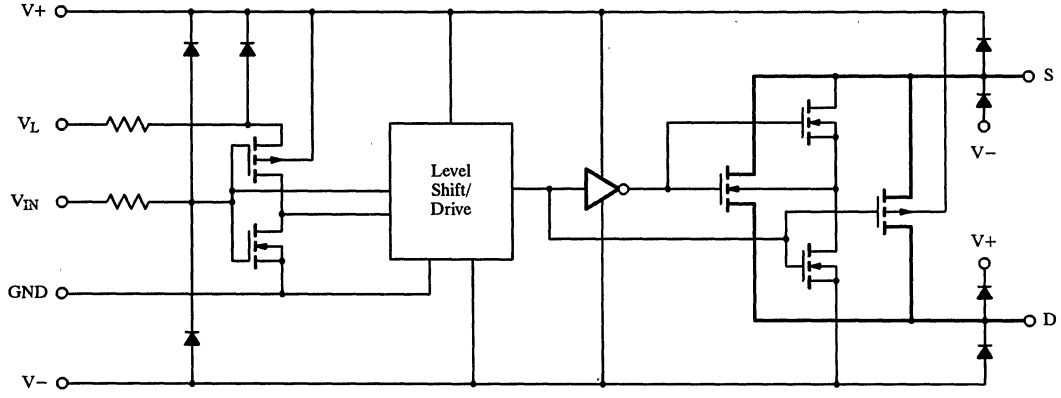
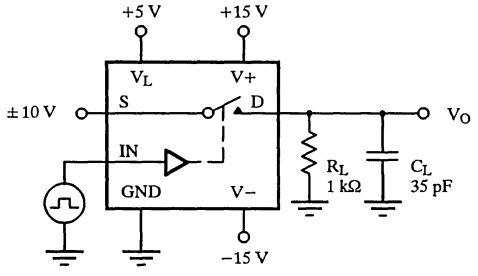
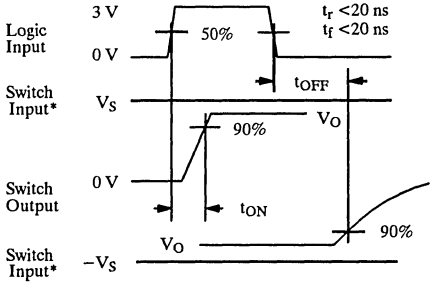


Figure 1.

Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.





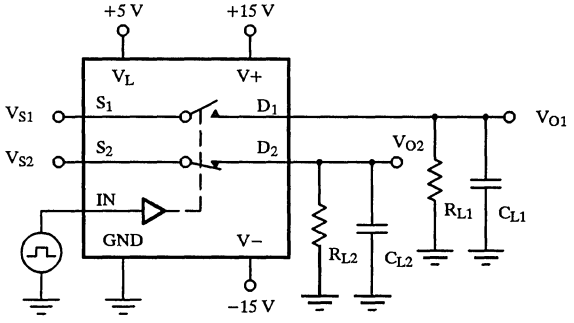
C_L (includes fixture and stray capacitance)

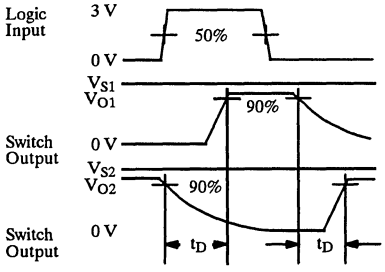
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

*V_S = 10 V for t_{ON}, V_S = −10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

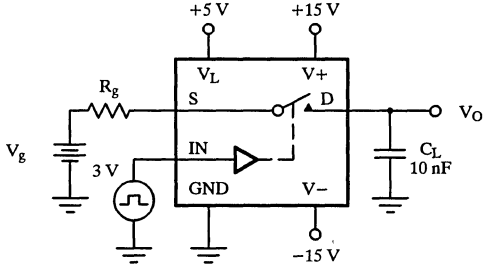
Figure 2. Switching Time





C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make



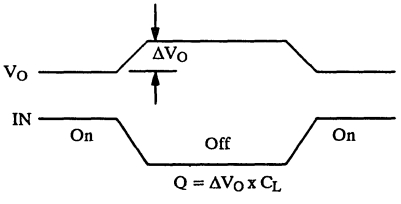


Figure 4. Charge Injection

Test Circuits (Cont'd)

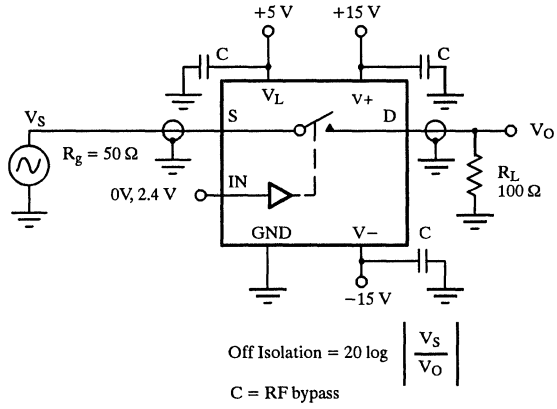


Figure 5. Off Isolation

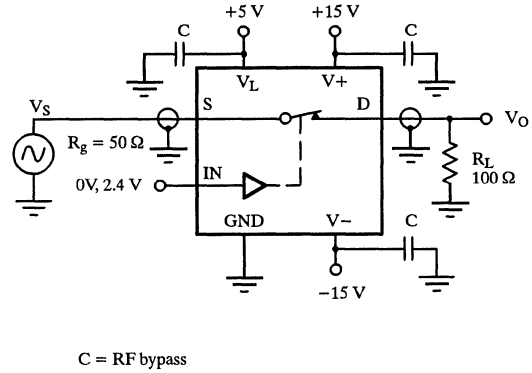


Figure 6. Insertion Loss

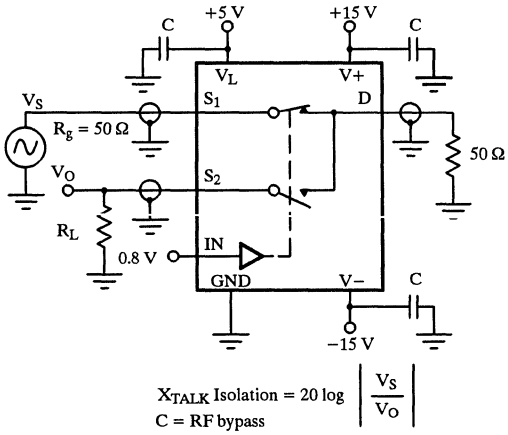


Figure 7. Crosstalk

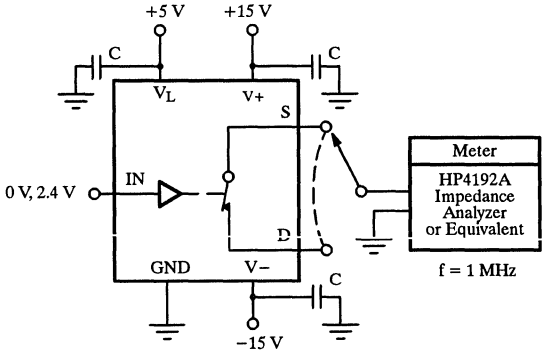


Figure 8. Capacitances

Applications

Stereo Source Selector:

A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low on-resistance (<35 Ω) minimizes total harmonic distortion.

Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

Applications (Cont'd)

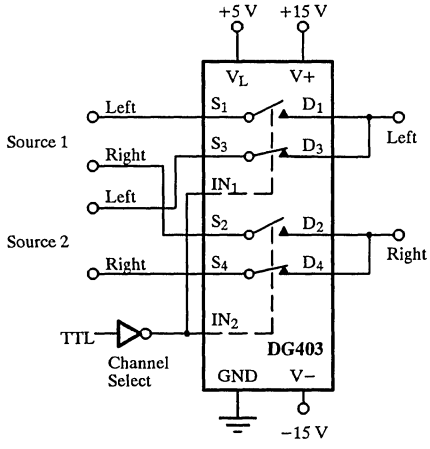


Figure 9. Stereo Source Selector

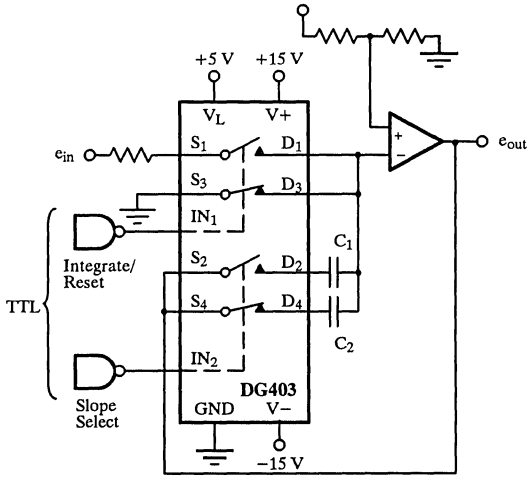


Figure 10. Dual Slope Integrator

Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

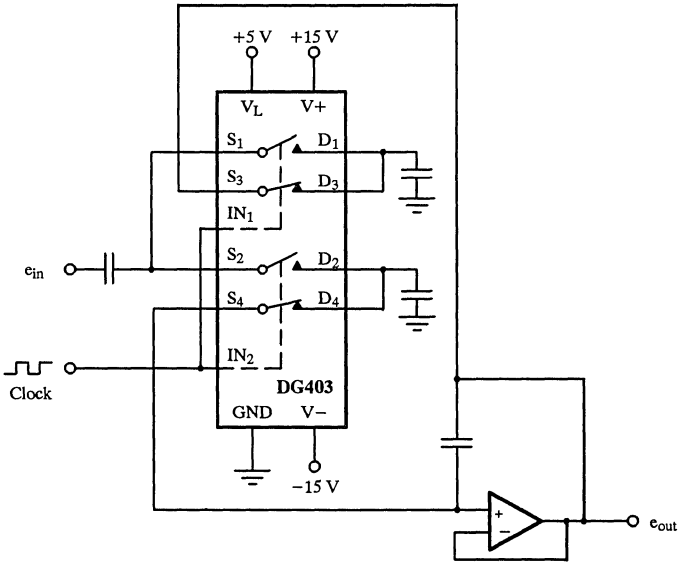


Figure 11. Band-Pass Switched Capacitor Filter

Applications (Cont'd)

Peak Detector:

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input e_{in}. If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{in} goes below e_{out} A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

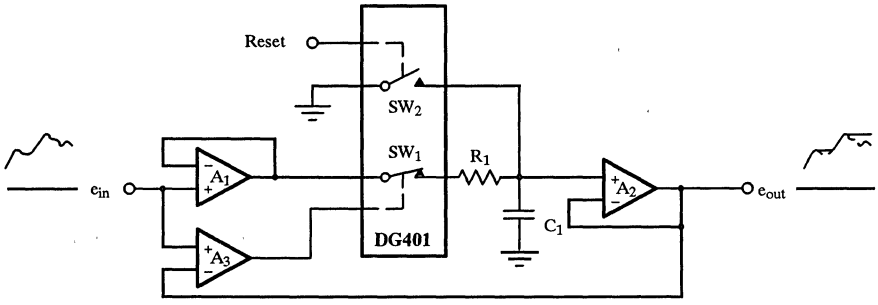


Figure 12. Positive Peak Detector

Precision Monolithic Quad SPST CMOS Analog Switches

Features

- 44-V Supply Max Rating
- ±15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 25 Ω
- Fast Switching—t_{ON}: 110 ns
- Ultra Low Power—P_D: 0.35 µW
- TTL, CMOS Compatible
- Single Supply Capability

Benefits

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

Applications

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Powered Systems
- Computer Peripherals

Description

The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.35 µW) with high speed (t_{ON}: 110 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

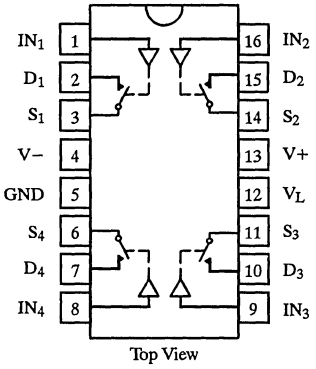
To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG411 and DG412 respond to opposite control logic as shown in the Truth Table. The DG413 has two normally open and two normally closed switches.

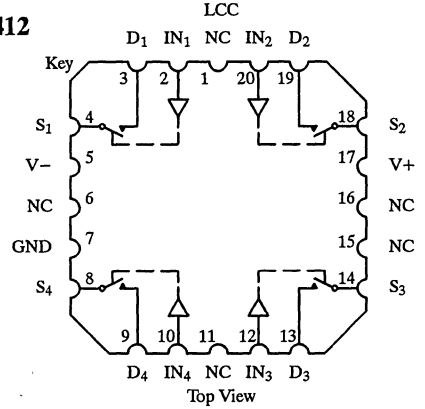
Functional Block Diagram and Pin Configuration

DG411/412 Dual-In-Line and SOIC



Top View

DG411/412 LCC



Top View

Ordering Information – DG411/412

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG411DJ
		DG412DJ
−40 to 85°C	16-Pin Narrow SOIC	DG411DY
		DG412DY
−55 to 125°C	16-Pin CerDIP	DG411AK, DG411AK/883, 5962-9073101MEA
		DG412AK, DG412AK/883, 5962-9073102MEA
	LCC-20	DG411AZ/883, 5962-9073101M2A
		DG412AZ/883, 5962-9073102M2A

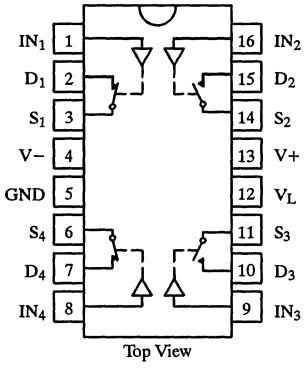
Truth Table

Logic	DG411	DG412
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for DG411 Logic "1" Input

DG413

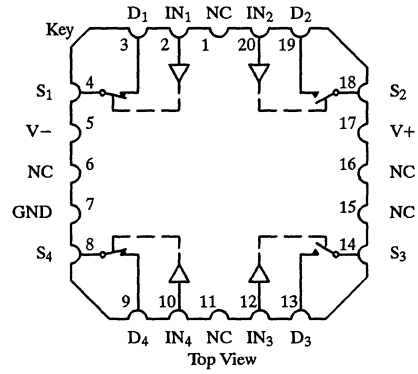
Dual-In-Line and SOIC



Top View

DG413

LCC



Top View

Ordering Information – DG413

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG413DJ
	16-Pin Narrow SOIC	DG413DY
−55 to 125°C	16-Pin CerDIP	DG413AK, DG413AK/883, 5962-9073103MEA
	LCC-20	DG413AZ/883, 5962-9073103M2A

Truth Table

Logic	SW_1, SW_4	SW_2, SW_3
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for DG411 Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
V_L ..... (GND −0.3 V) (V+) +0.3 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% Duty Cycle) ..... 100 mA
Storage Temperature (AK, AZ Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 600 mW
16-Pin CerDIP[e] ..... 900 mW
LCC-20[e] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 25°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 13.5 V, V− = −13.5 V I_S = −10 mA, V_D = ±8.5 V	Room Full	25		35 45		35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V− = −16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Full	±0.1	−0.25 −20	0.25 20	−0.25 −5	0.25 5	nA
	$I_{D(off)}$		Room Full	±0.1	−0.25 −20	0.25 20	−0.25 −5	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V V_S = V_D = ±15.5 V	Room Full	±0.1	−0.4 −40	0.4 40	−0.4 −10	0.4 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.005	−0.5	0.5	−0.5	0.5	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V	Full	0.005	−0.5	0.5	−0.5	0.5	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ±10 V See Figure 2	Room Full	110		175 240		175 220	ns
Turn-Off Time	t_{OFF}		Room Full	100		145 160		145 160	
Break-Before-Make Time Delay	t_D	DG413 Only, V_S = 10 V R_L = 300 Ω, C_L = 35 pF	Room	25					
Charge Injection	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	5					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	85					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	9					
Channel On Capacitance[e]	$C_{D(on)}$		Room	35					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5, V− = −16.5 V V_{IN} = 0 or 5 V	Room Full	0.0001		1 5		1 5	µA
Negative Supply Current	I−		Room Full	−0.0001	−1 −5		−1 −5		
Logic Supply Current	I_L		Room Full	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Full	−0.0001	−1 −5		−1 −5		

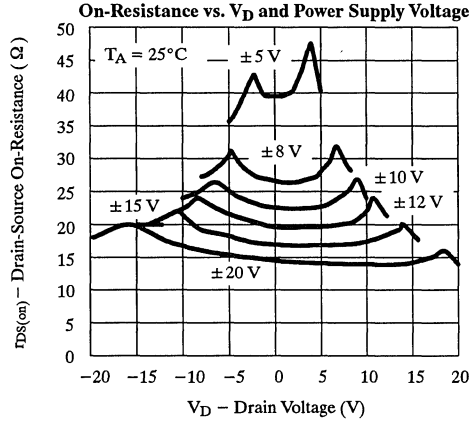
1

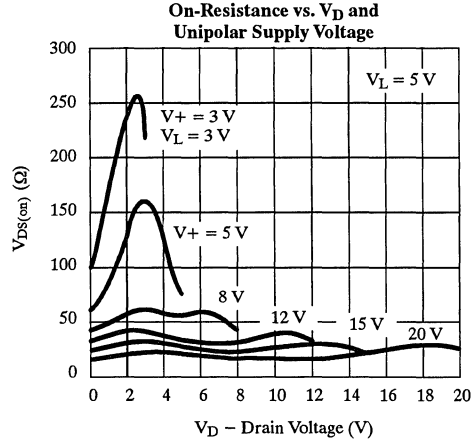
Specifications[a] for Unipolar Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full			12		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 10.8 V, I_S = −10 mA V_D = 3 V, 8 V	Room Full	40		80 100		80 100	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 8 V, See Figure 2	Room Hot	175		250 400		250 315	ns
Turn-Off Time	t_{OFF}		Room Hot	95		125 140		125 140	
Break-Before-Make Time Delay	t_D	DG413 Only V_S = 8 V, R_L = 300 Ω, C_L = 35 pF	Room	25					
Charge Injection	Q	V_g = 6 V, R_g = 0 Ω, C_L = 10 nF	Room	25					pC
Power Supplies									
Positive Supply Current	I+	V+ = 13.5, V_{IN} = 0 or 5 V	Room Hot	0.0001		1 5		1 5	µA
Negative Supply Current	I−		Room Hot	−0.0001	−1 −5		−1 −5		
Logic Supply Current	I_L		Room Hot	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Hot	−0.0001	−1 −5		−1 −5		

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

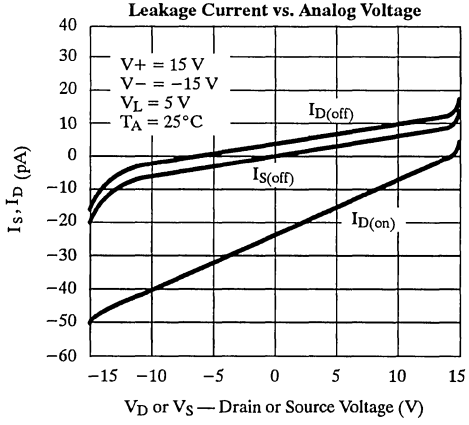
Typical Characteristics



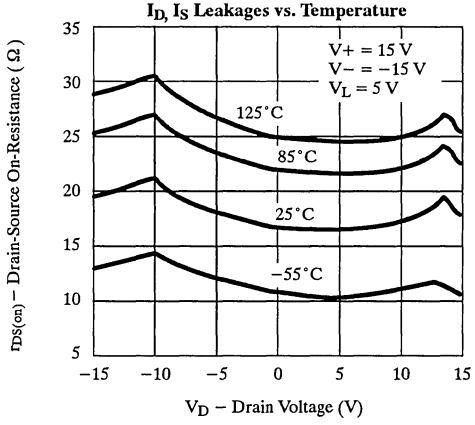


Typical Characteristics (Cont'd)

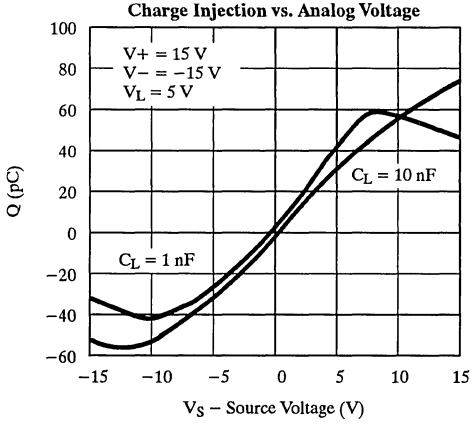
Leakage Current vs. Analog Voltage



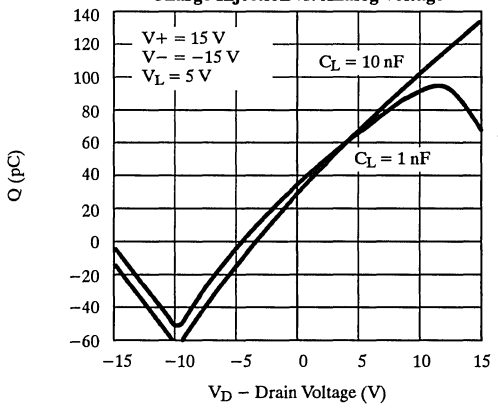
ID, IS Leakages vs. Temperature



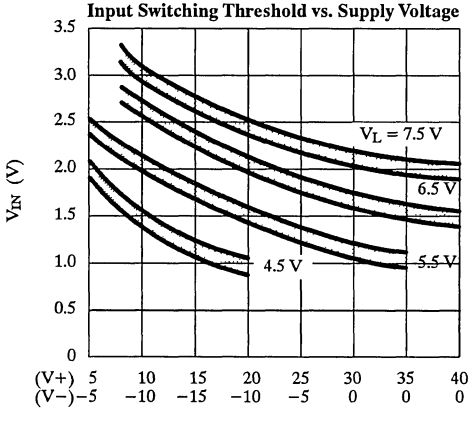
Charge Injection vs. Analog Voltage



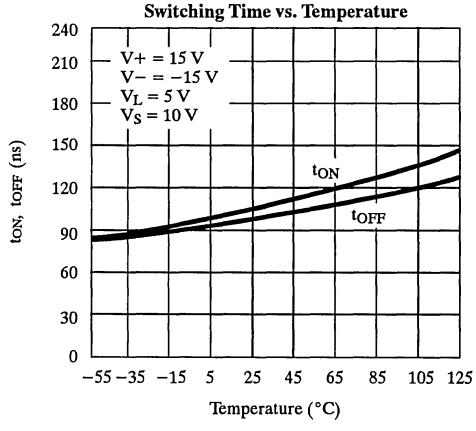
Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Supply Voltage

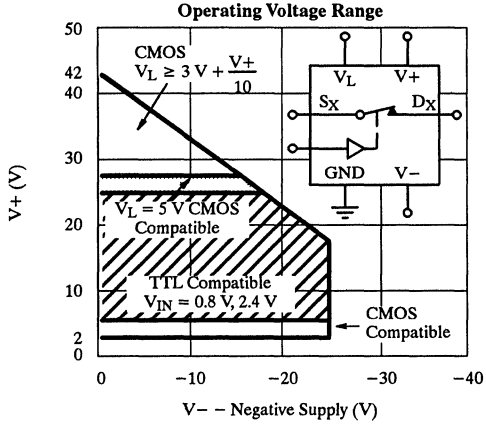


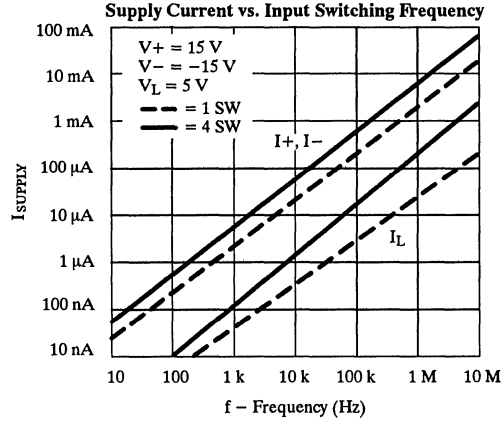
Switching Time vs. Temperature



1

Typical Characteristics (Cont'd)





Schematic Diagram (Typical Channel)

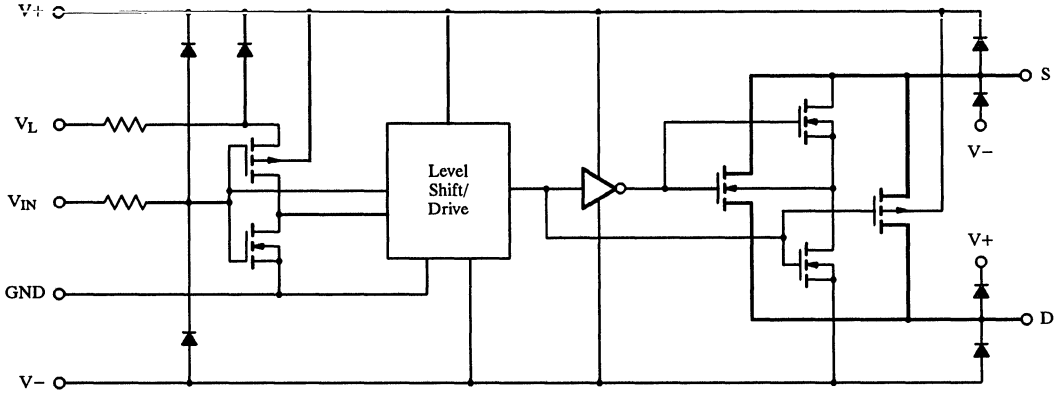
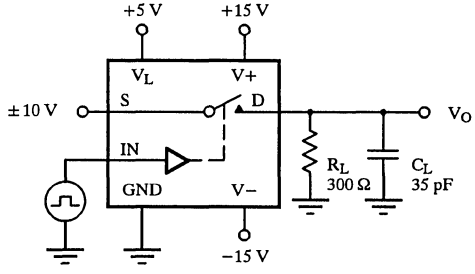


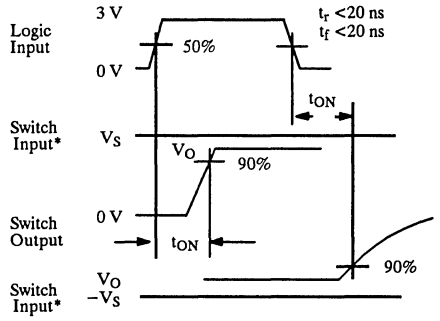
Figure 1.

Test Circuits



C_L (includes fixture and stray capacitance)

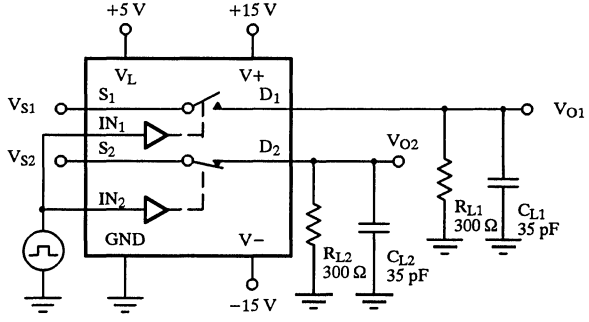
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

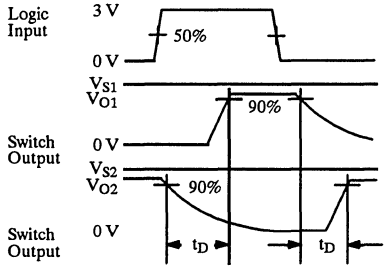


*V_S = 10 V for t_{ON}, V_S = −10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

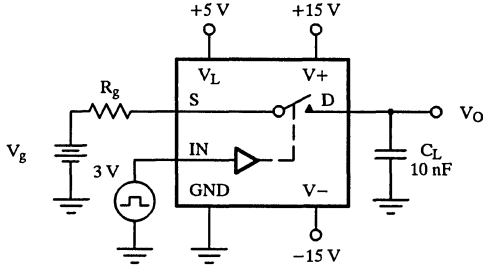
Figure 2. Switching Time

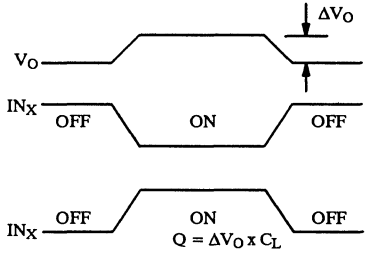




C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make (DG413)





IN_X dependent on switch configuration Input polarity determined by sense of switch.

Figure 4. Charge Injection

Test Circuits (Cont'd)

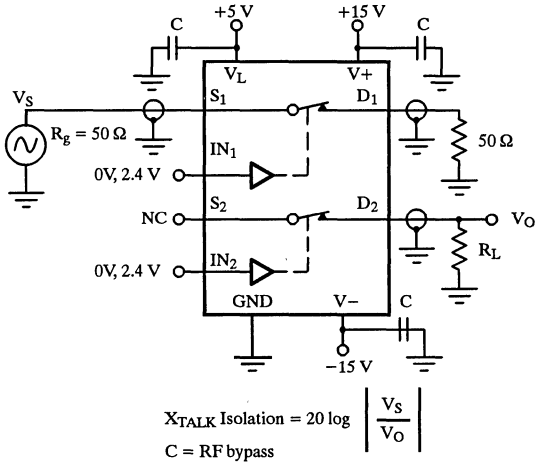


Figure 5. Crosstalk

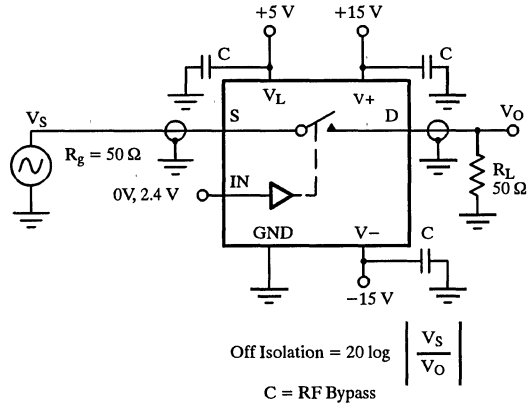


Figure 6. Off Isolation

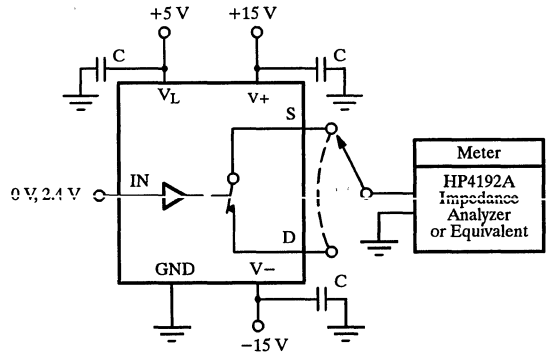


Figure 7. Source/Drain Capacitances

Applications

Single Supply Operation:

The DG411/412/413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V+ is tied to V_L and V− is tied to 0 V. See Input Switching Threshold vs. Supply Voltage curve for V_L versus input threshold requirments.

Applications (Cont'd)

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

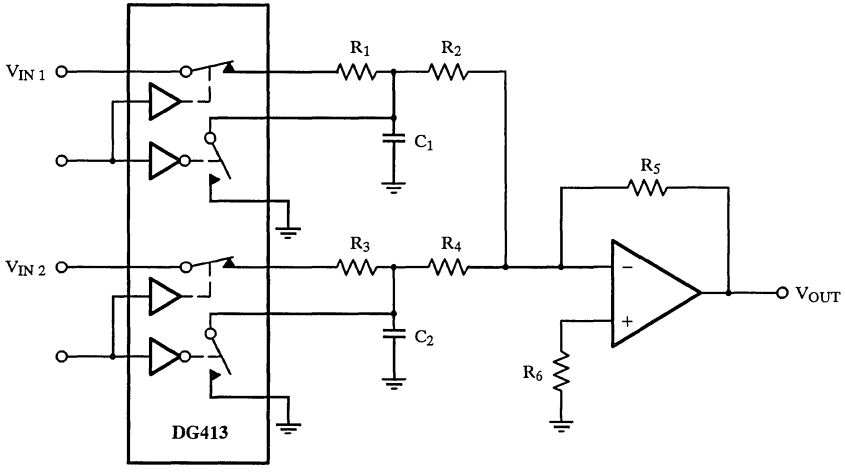


Figure 8. Summing Amplifier

Siliconix
A Member of the TEMIC Group

Precision CMOS Analog Switches

Features

- ±15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 20 Ω
- Fast Switching Action—t_{ON}: 100 ns
- Ultra Low Power Requirements—P_D: 35 nW
- TTL and CMOS Compatible
- MiniDIP and SOIC Packaging
- 44-V Supply Max Rating

Benefits

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

Applications

- Precision Test Equipment
- Precision Instrumentation
- Battery Powered Systems
- Sample-and-Hold Circuits
- Military Radios
- Guidance and Control Systems
- Hard Disk Drives

Description

The DG417/418/419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high-voltage ratings and superior switching performance, the DG417 series is built on Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer prevents latchup.

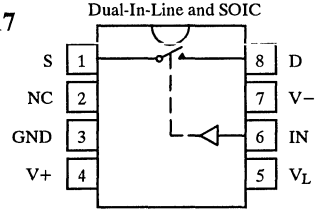
Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417 and DG418 respond to opposite control logic levels as shown in the Truth Table.

Functional Block Diagram and Pin Configuration

DG417

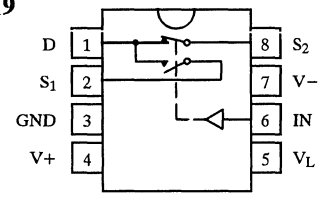
Dual-In-Line and SOIC



Top View

DG419

Dual-In-Line and SOIC



Top View

Truth Table — DG417/418

Logic	DG417	DG418
0	ON	OFF
1	OFF	ON

Logic "0" = ≤ 0.8 V, Logic "1" = ≥ 2.4 V
Switch Shown for DG417 Logic "1" Input

Truth Table — DG419

Logic	SW_1	SW_2
0	ON	OFF
1	OFF	ON

Logic "0" = ≤ 0.8 V, Logic "1" = ≥ 2.4 V
Switches Shown for DG419 Logic "1" Input

Ordering Information — DG417/418

Temp Range	Package	Part Number
−40 to 85°C	8-Pin Plastic MiniDIP	DG417DJ
		DG418DJ
	8-Pin Narrow SOIC	DG417DY
		DG418DY
−55 to 125°C	8-Pin CerDIP	DG417AK, DG417AK/883
		DG418AK, DG418AK/883

Ordering Information — DG419

Temp Range	Package	Part Number
−40 to 85°C	8-Pin Plastic MiniDIP	DG419DJ
	8-Pin Narrow SOIC	DG419DY
−55 to 125°C	8-Pin CerDIP	DG419AK, DG419AK/883

Absolute Maximum Ratings

Voltages Referenced to V−

V+ ..... 44 V

GND ..... 25 V

V_L ..... (GND −0.3 V) to (V+) + 0.3 V

Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) + 2 V
or 30 mA, whichever occurs first

Current, (Any Terminal) Continuous ..... 30 mA

Current (S or D) Pulsed 1 ms, 10% duty cycle ..... 100 mA

Storage Temperature (AK Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]

8-Pin Plastic MiniDIP[c] ..... 400 mW

8-Pin Narrow SOIC[d] ..... 400 mW

8-Pin CerDIP[e] ..... 600 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 6.5 mW/°C above 25°C
e. Derate 12 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±12.5 V V+ = 13.5 V, V− = −13.5 V		Room Full	20		35 45		35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V− = −16.5 V V_D = ∓15.5 V, V_S = ±15.5 V		Room Full	−0.1	−0.25 −20	0.25 20	−0.25 −5	0.25 5	nA
	$I_{D(off)}$		DG417 DG418	Room Full	−0.1	−0.25 −20	0.25 20	−0.25 −5	0.25 5	
			DG419	Room Full	−0.1	−0.75 −60	0.75 60	−0.75 −12	0.75 12	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V V_S = V_D = ±15.5 V	DG417 DG418	Room Full	−0.4	−0.4 −40	0.4 40	−0.4 −10	0.4 10	
			DG419	Room Full	−0.4	−0.75 −60	0.75 60	−0.75 −12	0.75 12	
Digital Control										
Input Current, V_{IN} Low	I_{IL}			Full	0.005	−0.5	0.5	−0.5	0.5	µA
Input Current, V_{IN} High	I_{IH}			Full	0.005	−0.5	0.5	−0.5	0.5	
Dynamic Characteristics										
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ±10 V See Switching Time Test Circuit	DG417 DG418	Room Full	100		175 250		175 250	ns
Turn-Off Time	t_{OFF}		DG417 DG418	Room Full	60		145 210		145 210	
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF V_{S1} = ±10 V, V_{S2} = ∓10 V	DG419	Room Full			175 250		175 250	
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF V_{S1} = V_{S2} = ±10 V	DG419	Room	13	5		5		
Charge Injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω		Room	60					pC
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V		Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		DG417 DG418	Room	8					
Channel On Capacitance	$C_{D(on)}$		DG417 DG418	Room	30					
			DG419	Room	35					

Specifications[a]

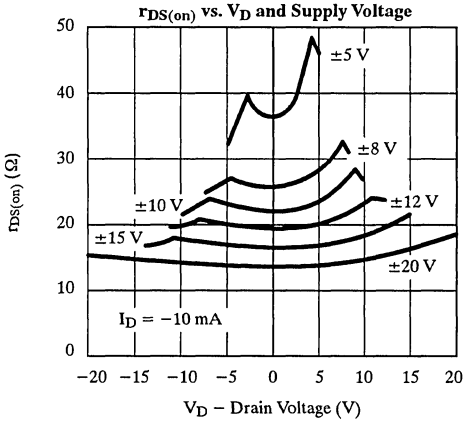
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V	Room Full	0.001		1 5		1 5	µA
Negative Supply Current	I−		Room Full	−0.001	−1 −5		−1 −5		
Logic Supply Current	I_L		Room Full	0.001		1 5		1 5	
Ground Current	I_{GND}		Room Full	−0.0001	−1 −5		−1 −5		

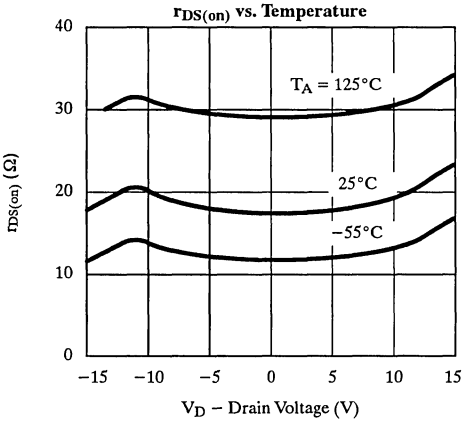
Specifications[a] for Unipolar Supplies

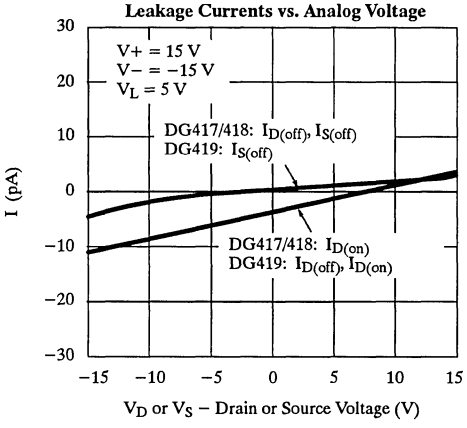
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 3.8 V, V+ = 10.8 V	Room	40					Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V See Switching Time Test Circuit	Room	110					ns
Turn-Off Time	t_{OFF}		Room	40					
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF DG419	Room	60					
Charge Injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	5					pC
Power Supplies									
Positive Supply Current	I+	V+ = 13.2 V, V_L = 5.25 V V_{IN} = 0 or 5 V	Room	0.001					µA
Negative Supply Current	I−		Room	−0.001					
Logic Supply Current	I_L		Room	0.001					
Ground Current	I_{GND}		Room	−0.001					

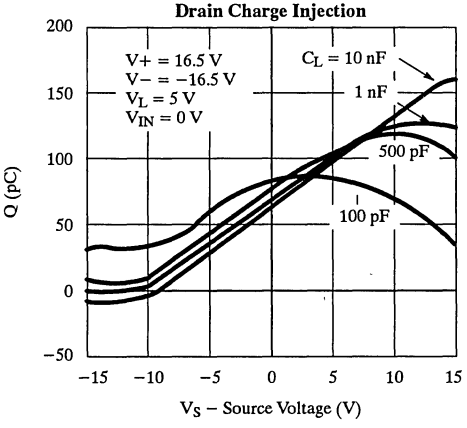
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

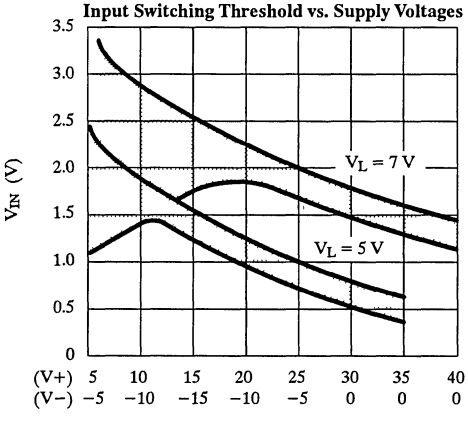
Typical Characteristics

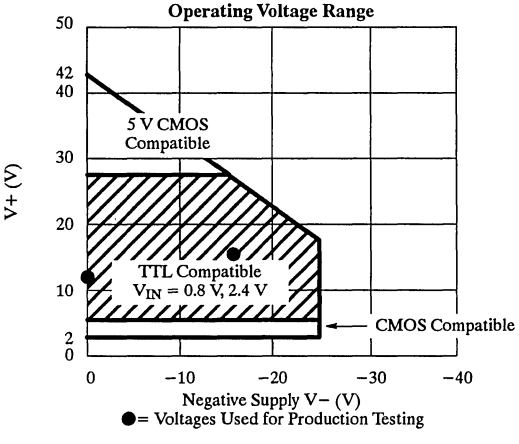












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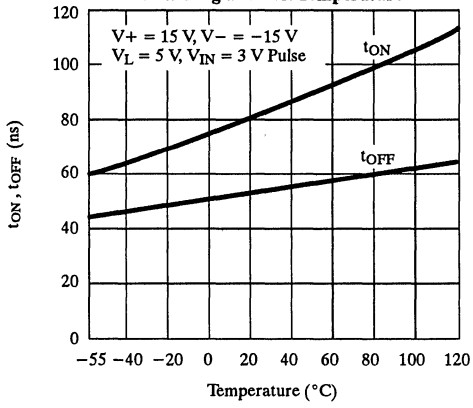
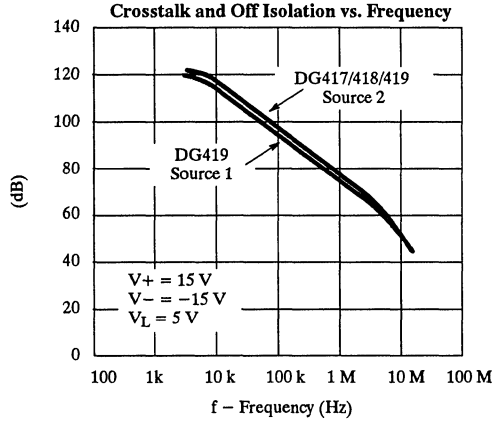
Typical Characteristics (Cont'd)

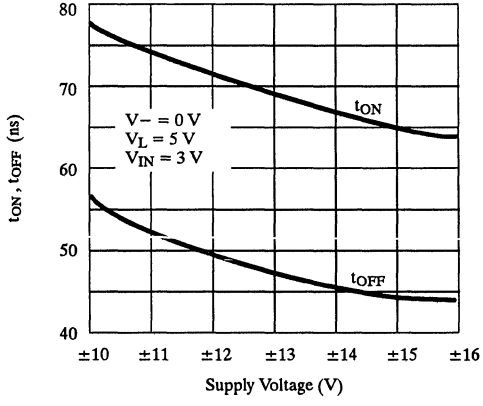
Switching Time vs. Temperature



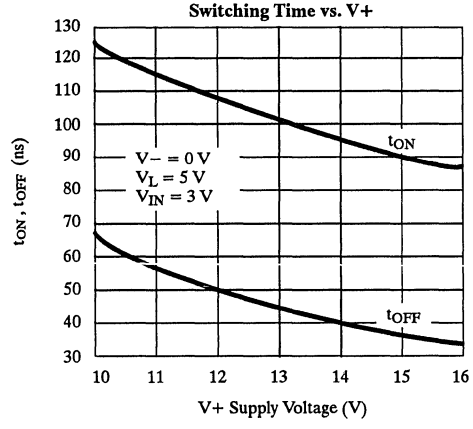
Crosstalk and Off Isolation vs. Frequency



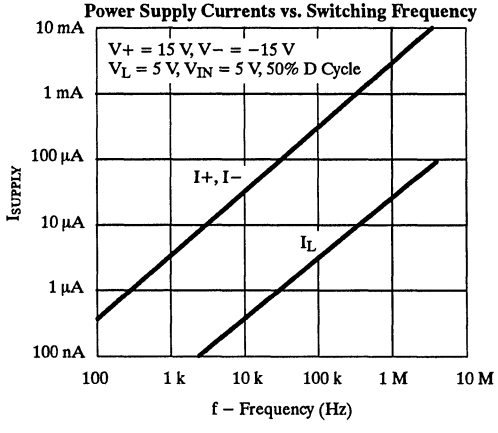
Switching Time vs. Supply Voltages



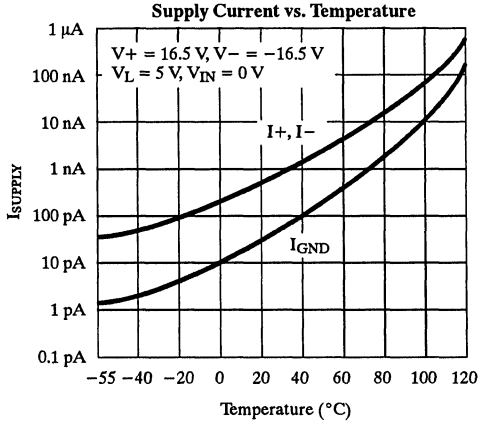
Switching Time vs. V+



Power Supply Currents vs. Switching Frequency



Supply Current vs. Temperature



Schematic Diagram (Typical Channel)

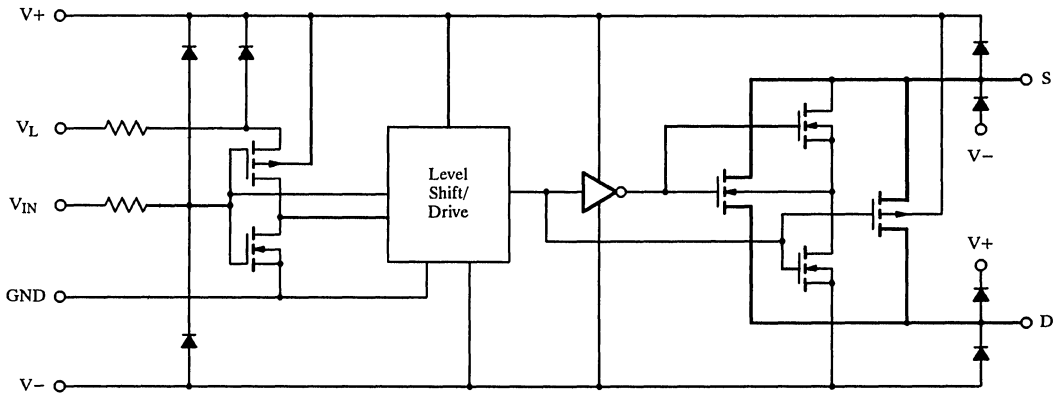
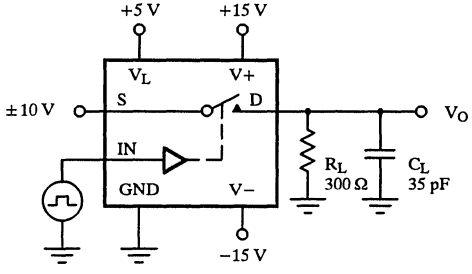


Figure 1.

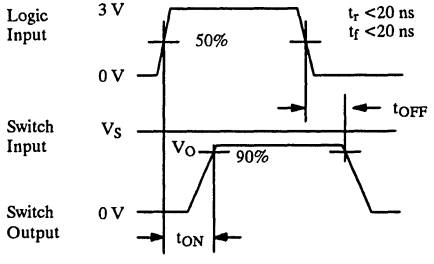
Test Circuits

V_O is the steady state output with the switch on.



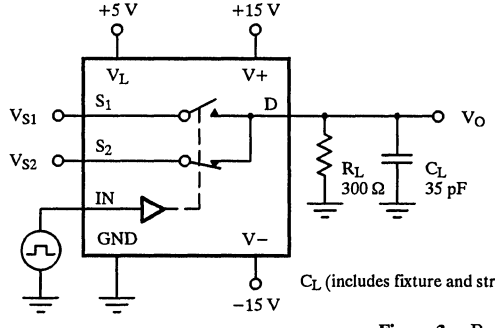
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417/418)



C_L (includes fixture and stray capacitance)

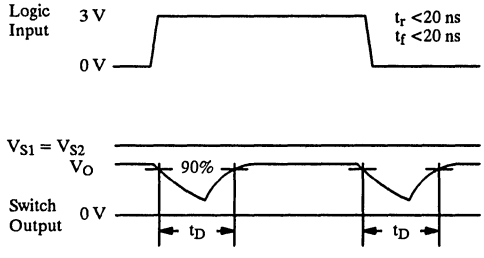
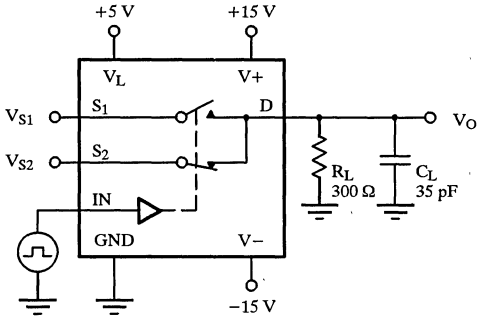


Figure 3. Break-Before-Make (DG419)

Test Circuits (Cont'd)



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

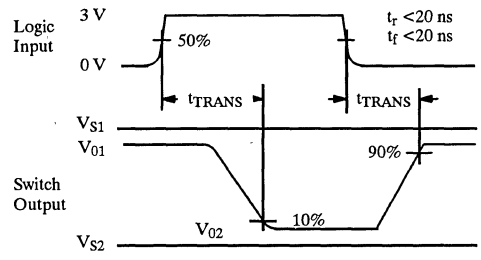
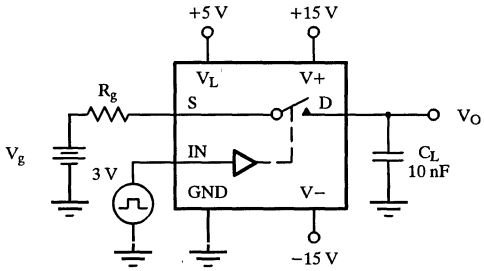
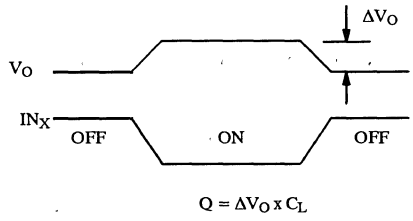


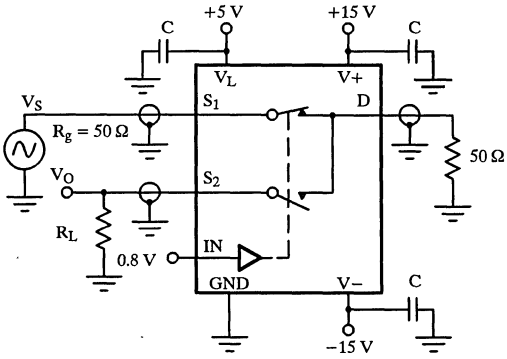
Figure 4. Transition Time (DG419)





$Q = \Delta V_O \times C_L$

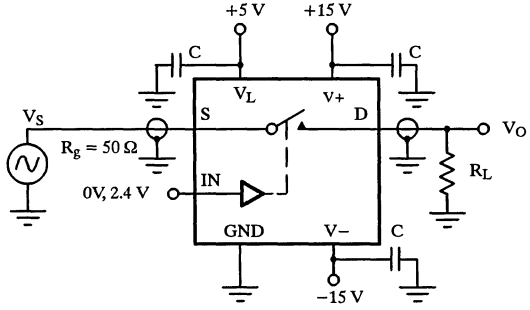
Figure 5. Charge Injection



X_{TALK} Isolation = $20 \log \left| \frac{V_S}{V_O} \right|$

C = RF bypass

Figure 6. Crosstalk (DG419)



Off Isolation = $20 \log \left| \frac{V_S}{V_O} \right|$

Figure 7. Off Isolation

Test Circuits (Cont'd)

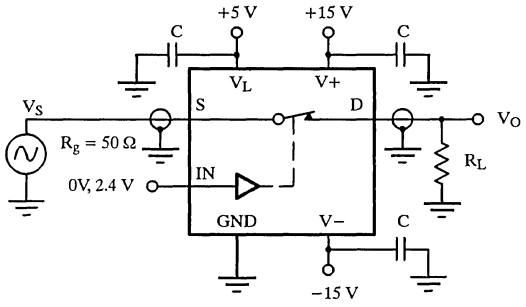


Figure 8. Insertion Loss

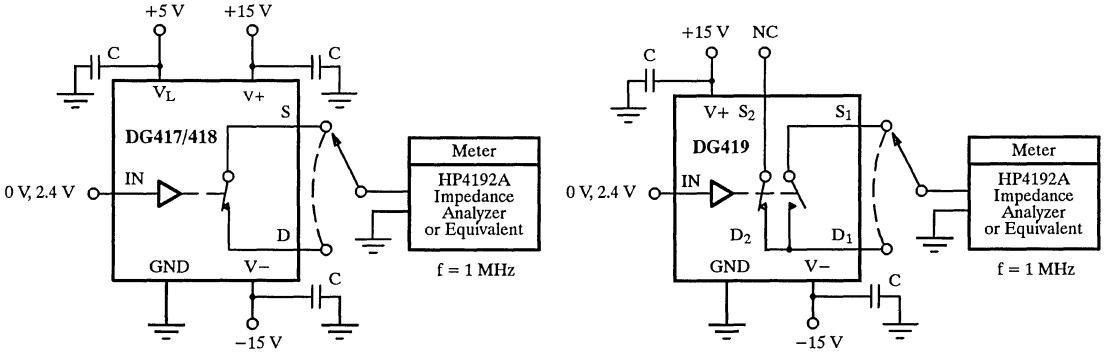


Figure 9. Source/Drain Capacitances

Applications

Switched Signal Powers Analog Switch

The analog switch in Figure 10 derives power from its input signal, provided the input signal amplitude exceeds 4 V and its frequency exceeds 1 kHz.

This circuit is useful when signals have to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse turns on the clamping diode D_1 and charges C_1. The charge stored on C_1 is used to power the chip; operation is satisfactory because the switch requires less than 1 µA of stand-by supply current. Loading of the signal source is imperceptible. The DG419's on-resistance is a low 100 Ω for a 5-V input signal.

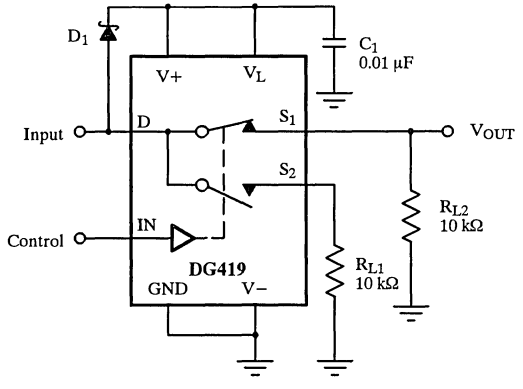


Figure 10. Switched Signal Powers Remote SPDT Analog Switch

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Applications (Cont'd)

Micropower UPS Transfer Switch

When V_{CC} drops to 3.3 V, the DG417 changes states, closing SW_1 and connecting the backup cell, as shown in Figure 11. D_1 prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analog switch is around 100 pA; this ensures that most of the power available is applied to the memory, where it is really needed. In the stand-by mode, hundreds of µA are sufficient to retain memory data.

When the 5-V supply comes back up, the resistor divider senses the presence of at least 3.5 V, and causes a new change of state in the analog switch, restoring normal operation.

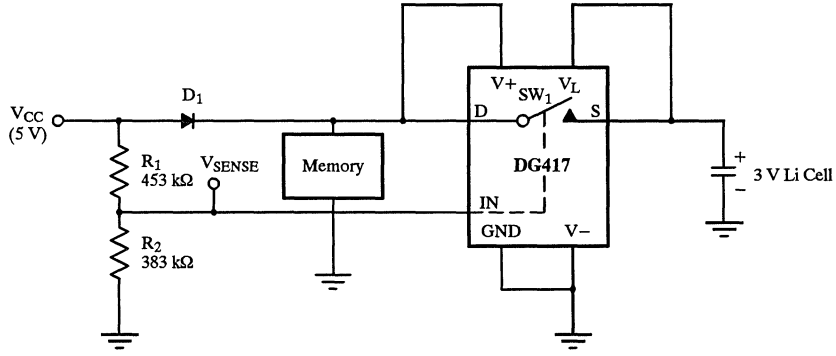


Figure 11. Micropower UPS Circuit

Programmable Gain Amplifier

The DG419, as shown in Figure 12, allows accurate gain selection in a small package. Switching into virtual ground reduces distortion caused by $r_{DS(on)}$ variation as a function of analog signal amplitude.

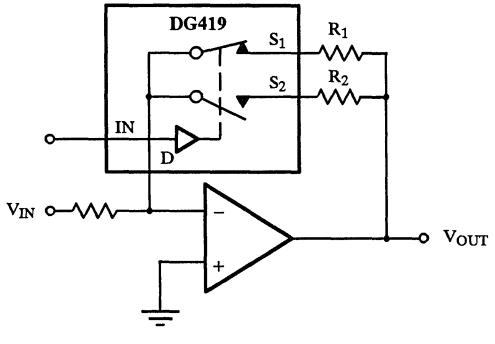


Figure 12. Programmable Gain Amplifier

GaAs FET Driver

The DG419, as shown in Figure 13 may be used as a GaAs FET driver. It translates a TTL control signal into −8-V, 0-V level outputs to drive the gate.

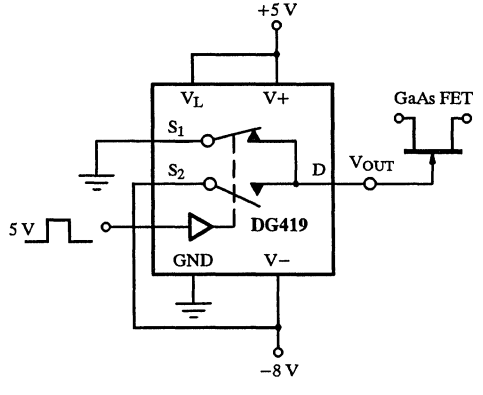


Figure 13. GaAs FET Driver

Low-Power, High-Speed, Latchable CMOS Analog Switches

Features

- Latched Control Inputs
- Rail-to-Rail Analog Input Range
- On-Resistance: 25 Ω
- Fast Switching Action—t_{ON}: 170 ns
- Micropower Requirements—P_D: 35 nW
- TTL and CMOS Logic Compatible
- Low Leakage: 40 pA

Benefits

- µP Compatible
- Wide Dynamic Range
- Reduced Component Count
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Battery-Compatible Operation

Applications

- Data Bus Switching
- Sample-and-Hold Circuits
- Programmable Filters
- µP Controlled Analog Systems
- Portable Instruments
- Telecommunication Systems

Description

The DG421/423/425 are monolithic analog switches featuring latchable logic inputs to simplify interfacing with microprocessors. This series combines fast switching speed (t_{ON}: 170 ns, typ), and low on-resistance ($r_{DS(on)}$: 25 Ω, typ) making it ideally suited for battery powered industrial and military applications that require microprocessor compatible analog switches.

The DG421 has two normally open switches (SPST). The DG423 has two single-pole, double-throw (SPDT) pairs. The DG425 has two normally open pairs (DPST).

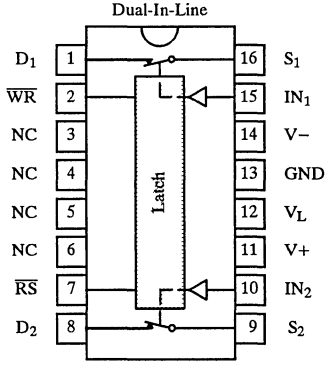
To achieve high-voltage ratings and superior switching performance, the DG421 series is built on Siliconix's high voltage silicon gate CMOS process. Break-before-make is guaranteed for the DG423. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on and blocks input voltages up to the supply rail voltages when off.

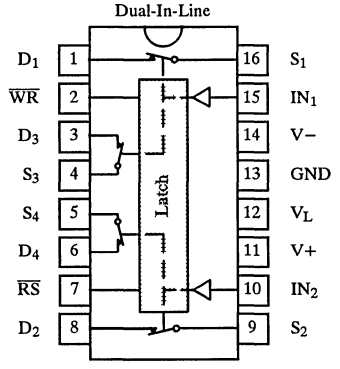
The input data latches become transparent when $\overline{WR}$ is set low. When $\overline{WR}$ goes high the latches store the logic control data. A low on $\overline{RS}$ resets all switches to their default state (all inputs low).

Functional Block Diagram and Pin Configuration

DG421



DG425



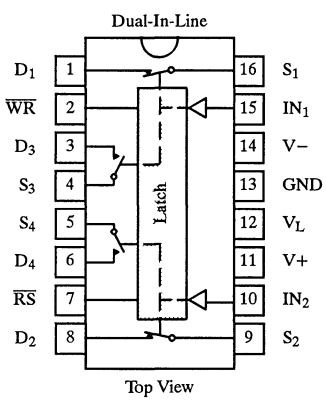
Truth Table – DG421/DG425

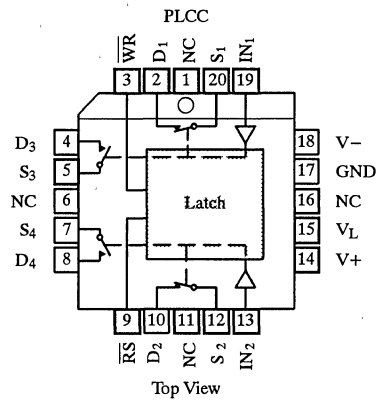
$\overline{WR}$	$\overline{RS}$	IN_X	Switch
0	1	0	OFF
		1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Functional Block Diagram and Pin Configuration

DG423





Truth Table – DG423

$\overline{WR}$	$\overline{RS}$	IN_X	SW_1, SW_2	SW_3, SW_4
0	1	0	OFF	ON
		1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Ordering Information – DG421/423/425

Temp Range	Package	Part Number
−40 to 85°	16-Pin Plastic DIP	DG421DJ
		DG423DJ
		DG425DJ
	20-Pin PLCC	DG423DN

Latch Operation Truth Table

IN_X	$\overline{RS}$	$\overline{WR}$	Latch/Switch X
X	1	0	Transparent latch operation
X	1	↓	Control data latched-in, switches on or off as selected by last IN_X
X	0	X	All latches reset, switches on or off as when IN_X = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 1
X	↓	X	

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
V_L ..... (GND −0.3 V) to (V+) +0.3 V
Digital Inputs[a] V_S, V_D ..... V− minus 2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 40 mA
Current, S or D (Pulsed 1 ms, 10% duty) ..... 100 mA
Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
20-Pin PLCC[d] ..... 800 mW

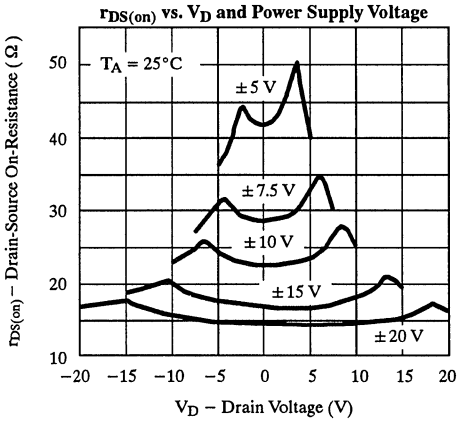
Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 10 mW/°C above 75°C

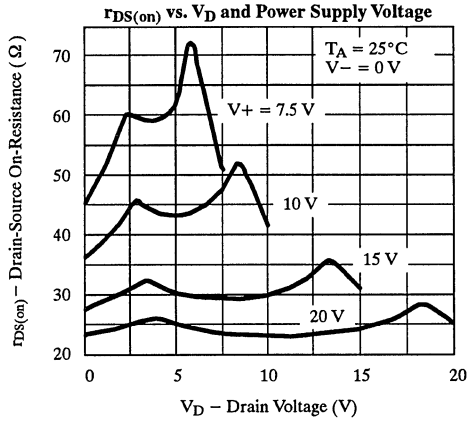
Specifications

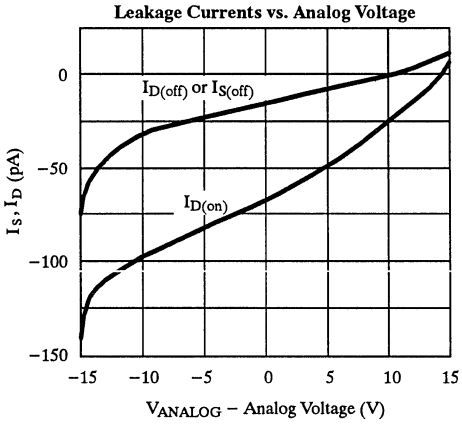
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	−15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±8.5 V V+ = 13.5 V, V− = −13.5 V	Room Full		25	35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V− = −16.5 V V_D = ∓15.5 V, V_S = ±15.5 V	Room Full	−0.25 −5	±0.01	0.25 5	nA
	$I_{D(off)}$		Room Full	−0.25 −5	±0.01	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V	Room Full	−0.4 −10	±0.04	0.4 10	
Digital Control							
Input Current with V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V, all other = 2.4 V	Full	−0.5	0.005	0.5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V, all other = 0.8 V	Full	−0.5	0.005	0.5	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room Full		170	250 300	ns
Turn-Off Time	t_{OFF}		Room Full		140	200 200	
Latch Timing	t_{WW}	R_L = 300 Ω, C_L = 35 pF V_S = ±10 V	Room Full	200 200			
	t_{DW}		Room Full	100 100			
	t_{WD}		Room Full	60 100			
Break-Before-Make Time Delay	t_D	DG423 Only, R_L = 300 Ω, C_L = 35 pF, See Figure 3	Room	5	25		
Charge Injection[d]	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω, See Figure 4	Room		60		pC
Off Isolation Reject Ratio	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		65		dB
Crosstalk (Channel-to-Channel)	X_{TALK}	Between Any Two Channels R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		76		
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz	Full		9		pF
Drain Off Capacitance	$C_{D(off)}$		Full		9		
Channel On Capacitance	$C_{D(on)}$		Full		35		
Power Supply							
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V	Room Full		0.0001	1 5	µA
Negative Supply Current	I−		Room Full	−1 −5	−0.0001		
Logic Supply Current	I_L		Room Full		0.0001	1 5	
Ground Current	I_{GND}		Room Full	−1 −5	−0.0001		

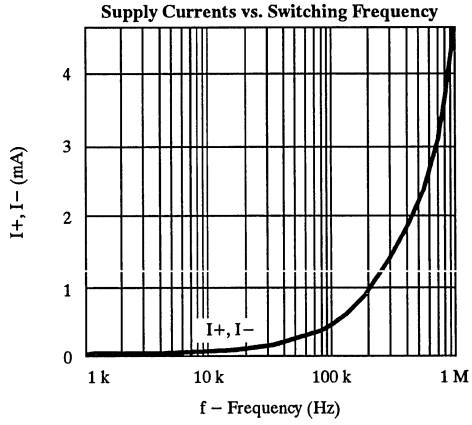
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

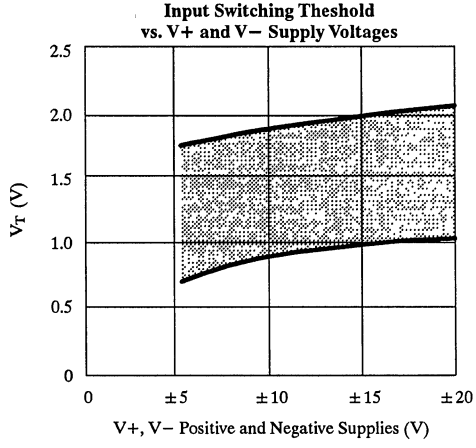
Typical Characteristics











Schematic Diagram (Typical Channel)

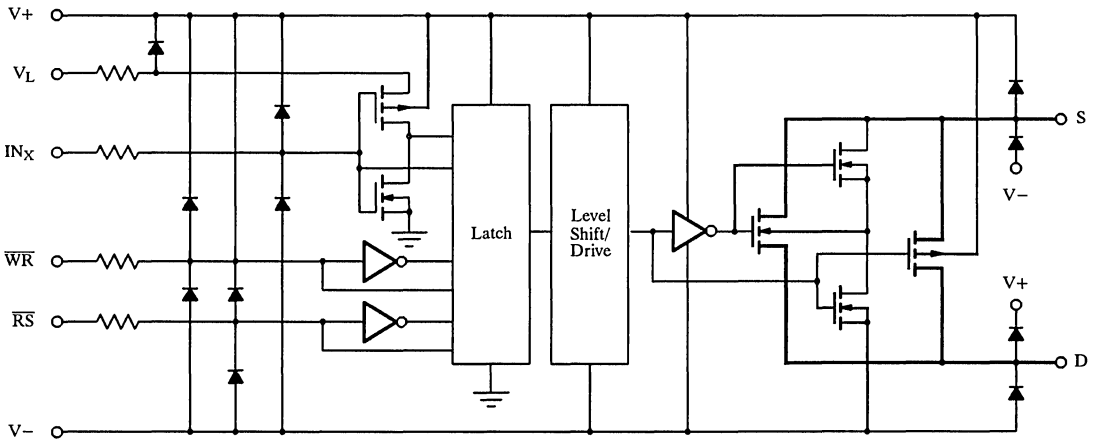
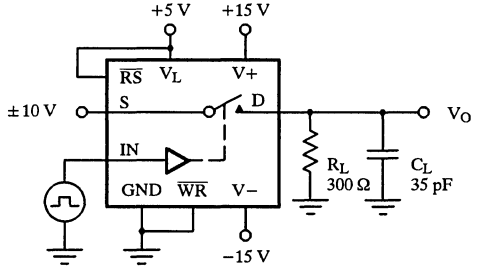


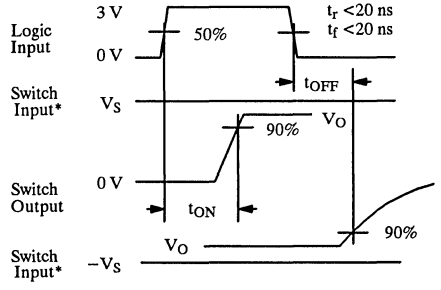
Figure 1.

Test Circuits



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

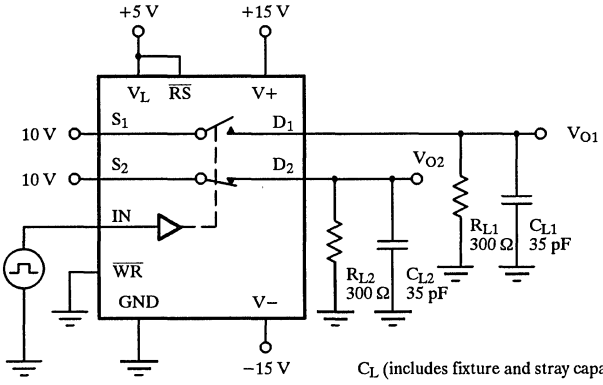


*V_S = 10 V for t_{ON}, V_S = −10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

Test Circuits (Cont'd)



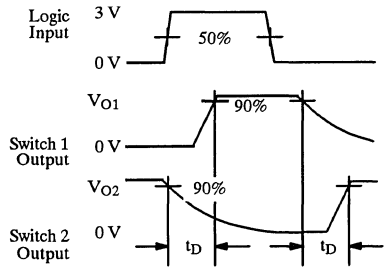
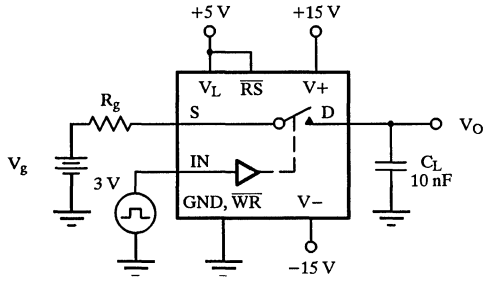


Figure 3. Break-Before-Make



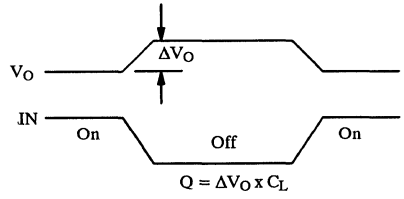


Figure 4. Charge Injection

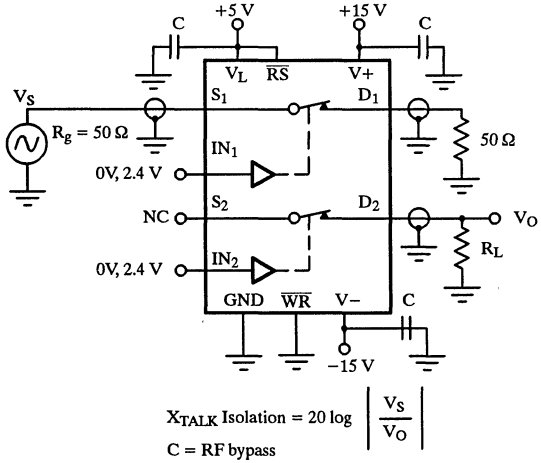


Figure 5. Crosstalk

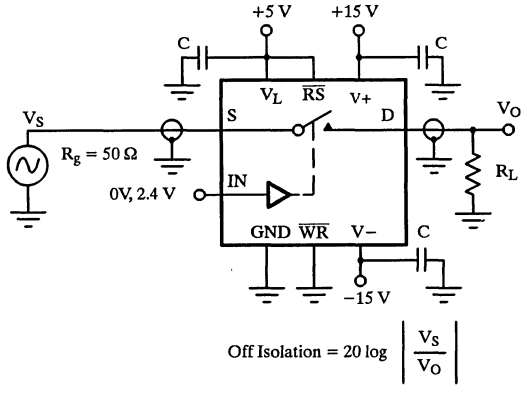


Figure 6. Off Isolation

Test Circuits (Cont'd)

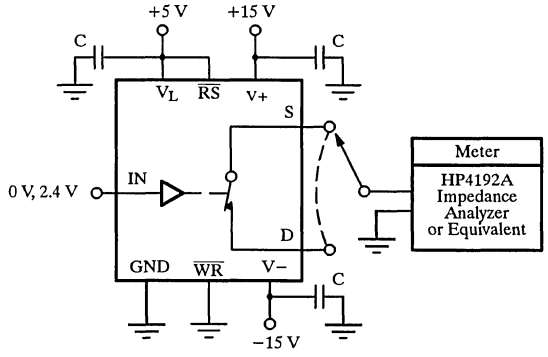


Figure 7. Source/Drain Capacitances

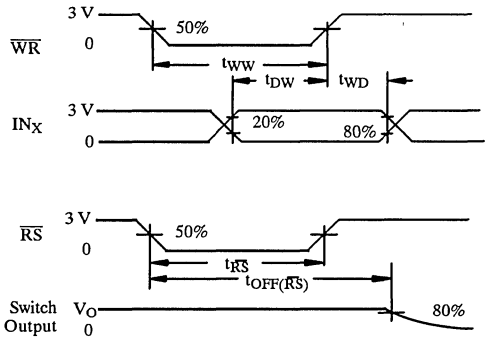
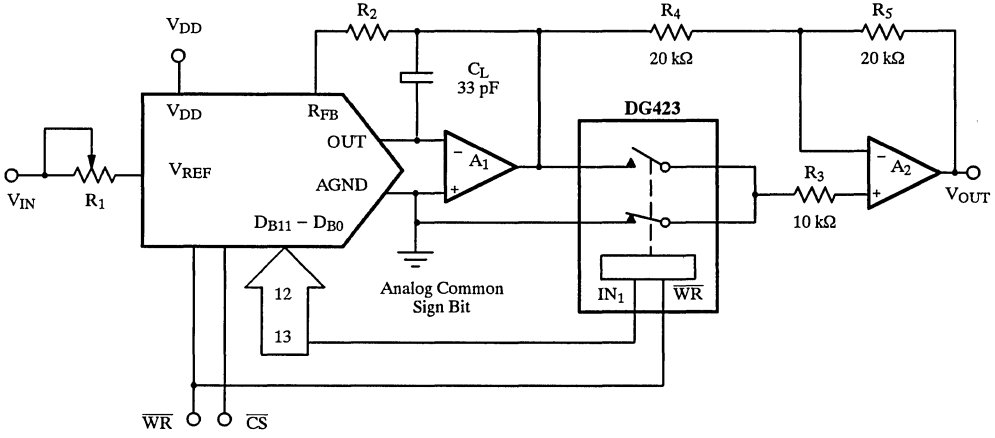


Figure 8. Latch Timing

Applications

Figure 9 shows a circuit configured to increase the effective resolution of the 12-bit DAC to 13 bits. The circuit operates with a sign plus magnitude code. A sign bit of "0" connects R_3 to GND, giving 12-bit resolution per quadrant.



12-Bit Plus Sign Magnitude Code Table

Sign Bit	Digital Input MSB		LSB	Analog Output (V_{OUT})
0	1111	1111	1111	+(4095/4096)V_{IN}
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	+(4095/4096)V_{IN}

Figure 9. 12-Bit Plus Sign Magnitude D/A Converter

Applications

When switch S_1 of Figure 10 is closed, the op amp is placed in the familiar unity-gain non-inverting configuration. When switch S_2 is closed and S_1 is open the gain is given by:

$$A_V = 1 + \frac{R_1}{R_2}$$

The microprocessor system $\overline{WR}$ must gate the decoder output to ensure proper timing.

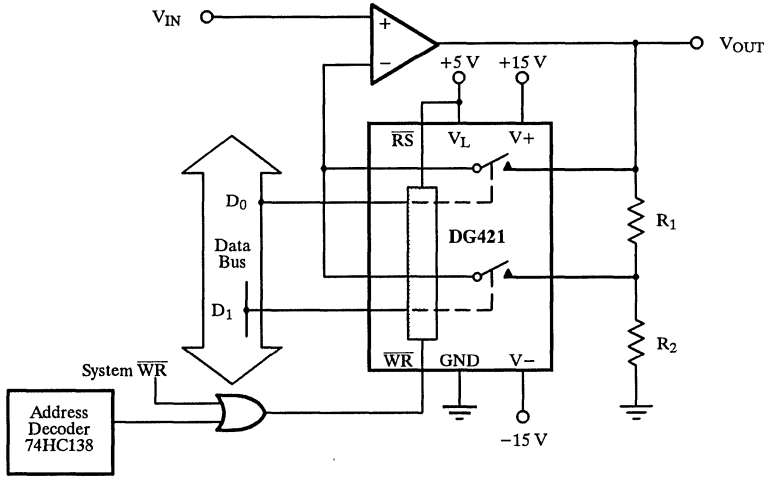
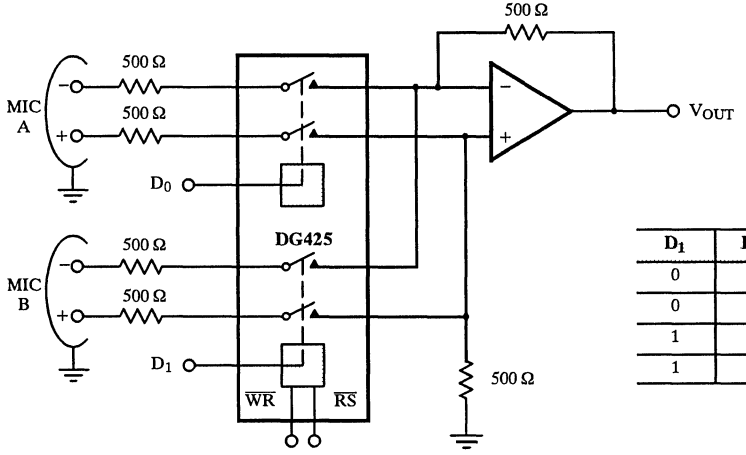


Figure 10. Bus-Controlled Precision Gain-Ranging Circuit

Figure 11 shows a balanced-line microphone input stage that provides selection or summing between two balanced-line microphones and also performs differential-to-single-ended conversion. Either MIC A or MIC B can be selected, and neither and/or both may be summed at the output. This configuration uses "virtual ground" switching, a method which minimizes distortion resulting from the analog switch on-resistance modulation. The actual voltage swings experienced by the analog switch barely exceed 1 V for a 15-V full-scale range input.



D_1	D_2	Output
0	0	None
0	1	MIC A
1	0	MIC B
1	1	MIC A and MIC B

Figure 11. Bus-Controlled Selector for Balanced-Line Microphones

Quad SPST CMOS Analog Switches

Features

- Low On-Resistance: 50 Ω
- Low Leakage: 80 pA
- Low Power Consumption: 0.2 mW
- Fast Switching Action—t_{ON}: 150 ns
- Low Charge Injection—Q: −1 pC
- DG201A/DG202 Upgrades
- TTL/CMOS-Compatible Logic
- Single Supply Capability

Benefits

- Less Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Errors
- Simplifies Retrofit
- Simple Interfacing

Applications

- Audio Switching
- Battery Powered Systems
- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

Description

The DG441/442 monolithic quad analog switches are designed to provide high speed, low error switching of analog and audio signals. The DG441 has a normally closed function. The DG442 has a normally open function. Combining low on-resistance (50 Ω, typ.) with high speed (t_{ON} 150 ns, typ.), the DG441/442 are ideally suited for upgrading DG201A/202 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

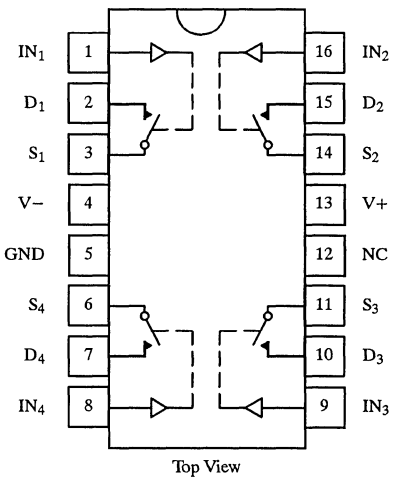
To achieve high voltage ratings and superior switching performance, the DG441/442 are built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

Functional Block Diagram and Pin Configuration

DG441

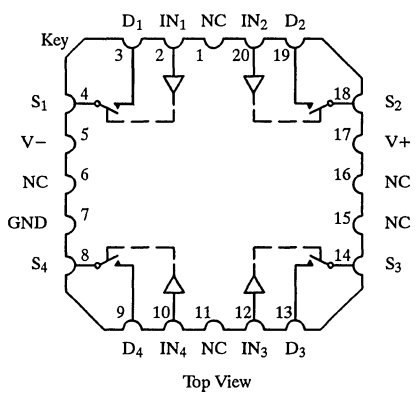
Dual-In-Line and SOIC



Top View

DG441

LCC



Top View

Ordering Information and Truth Table

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG441DJ
		DG442DJ
	16-Pin Narrow SOIC	DG441DY
		DG442DY
−55 to 125°C	16-Pin CerDIP	DG441AK
		DG441AK/883
		5962-9204101MEA
		DG442AK
		DG442AK/883
		5962-9204102MEA
	LCC-20	5962-9204101M2A
		5962-9204102M2A

Truth Table

Logic	DG441	DG442
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for DG441 Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature (AK Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C
Power Dissipation (Package)b
16-Pin Plastic DIP[c] ..... 450 mW
16-Pin CerDIP[d] ..... 900 mW
16-Pin Narrow Body SOIC[d] ..... 900 mW
LCC-20[d] ..... 1200 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 25°C

Specifications[a] for Dual Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±8.5 V V+ = 13.5 V, V− = −13.5 V	Room Full	50		85 100		85 100	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V− = −16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Full	±0.01	−0.5 −20	0.5 20	−0.5 −5	0.5 5	nA
	$I_{D(off)}$		Room Full	±0.01	−0.5 −20	0.5 20	−0.5 −5	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V V_S = V_D = ±15.5 V	Room Full	±0.08	−0.5 −40	0.5 40	−0.5 −10	0.5 10	

Specifications[a] for Dual Supplies (Cont'd)

Parameter		Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Digital Control										
Input Current V_{IN} Low		I_{IL}	V_{IN} under test = 0.8 V, All Other = 2.4 V	Full	−0.01	−500	500	−500	500	nA
Input Current V_{IN} High		I_{IH}	V_{IN} under test = 2.4 V, All Other = 0.8 V	Full	0.01	−500	500	−500	500	
Dynamic Characteristics										
Turn-On Time		t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = ±10 V, See Figure 2	Room	150		250		250	ns
Turn-Off Time	DG441	t_{OFF}		Room	90		120		120	
	DG442			Room	110		210		210	
Charge Injection[e]		Q	C_L = 1 nF, V_S = 0 V, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	−1					pC
Off Isolation[e]		OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	60					dB
Crosstalk[e] (Channel-to-Channel)		X_{TALK}		Room	100					
Source Off Capacitance[e]		$C_{S(off)}$	f = 1 MHz	Room	4					pF
Drain Off Capacitance[e]		$C_{D(off)}$		Room	4					
Channel On Capacitance[e]		$C_{D(on)}$	V_{ANALOG} = 0 V	Room	16					
Power Supplies										
Positive Supply Current		I+	V+ = 16.5 V, V− = −16.5 V, V_{IN} = 0 or 5 V	Full	15		100		100	µA
Negative Supply Current		I−		Room Full	−0.0001	−1 −5		−1 −5		
Ground Current		I_{GND}		Full	−15	−100		−100		

Specifications[a] for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 3 V, 8 V, V+ = 10.8 V	Room Full	100		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V, See Figure 2	Room	300		450		450	ns
Turn-Off Time	t_{OFF}		Room	60		200		200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	2					pC

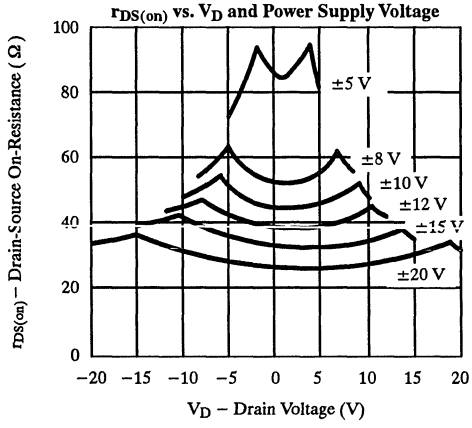
Specifications[a] for Single Supply[a] (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V	Full	15		100		100	µA
Negative Supply Current	I−		Room Full	−0.0001	−1 −100		−1 −100		
Ground Current	I_{GND}		Full	−15	−100		−100		

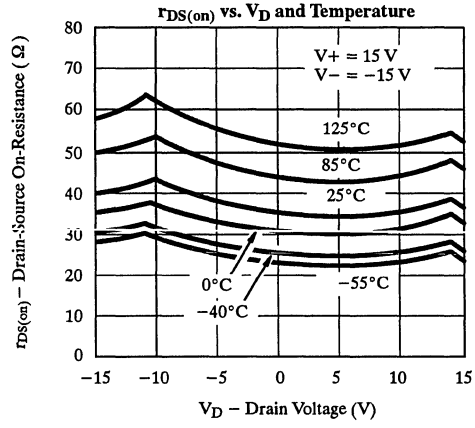
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

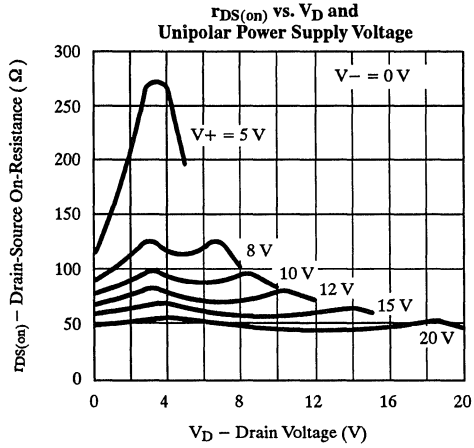
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



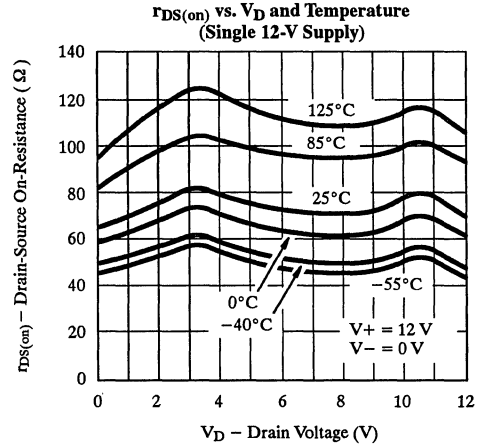
$r_{DS(on)}$ vs. V_D and Temperature



$r_{DS(on)}$ vs. V_D and Unipolar Power Supply Voltage

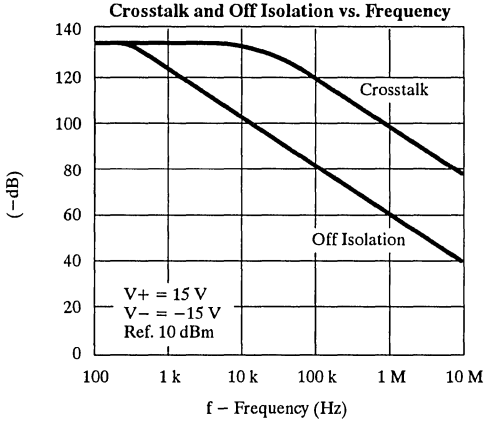


$r_{DS(on)}$ vs. V_D and Temperature (Single 12-V Supply)

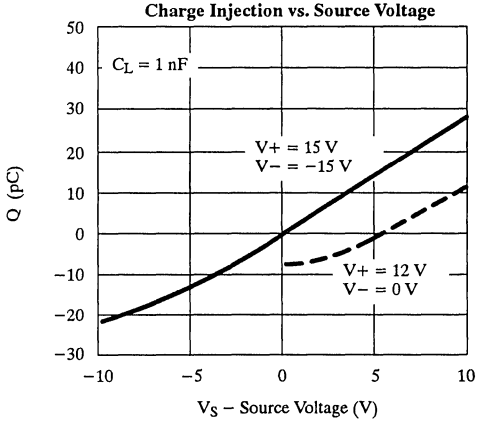


Typical Characteristics (Cont'd)

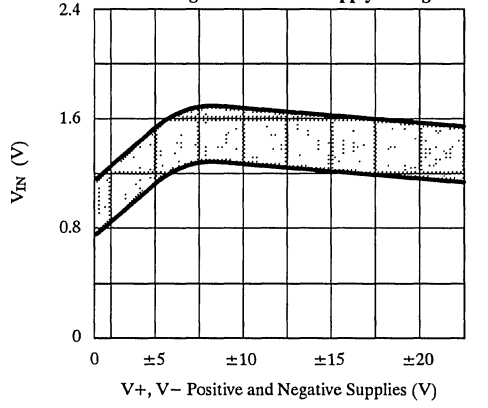
Crosstalk and Off Isolation vs. Frequency



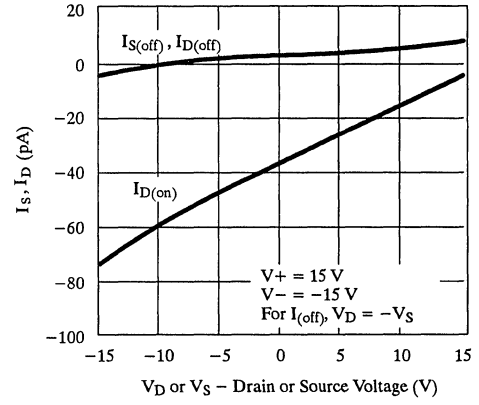
Charge Injection vs. Source Voltage



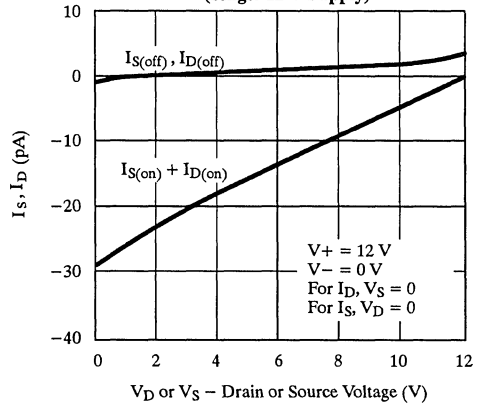
Switching Threshold vs. Supply Voltage



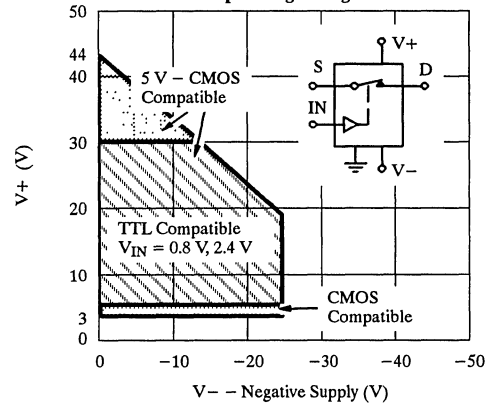
Source/Drain Leakage Currents



Source/Drain Leakage Currents
(Single 12-V Supply)

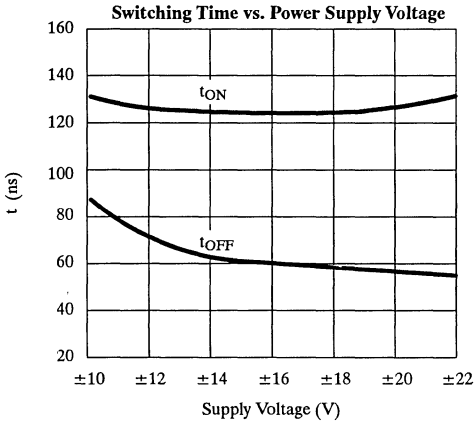


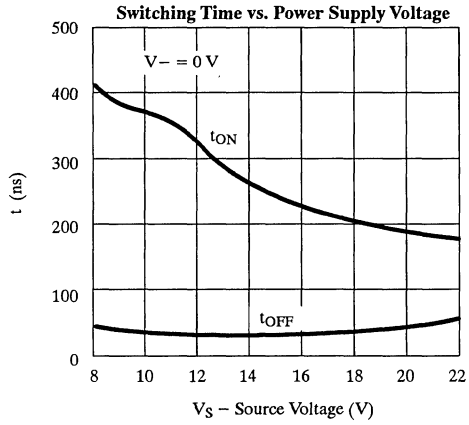
Operating Voltage



1

Typical Characteristics (Cont'd)





Schematic Diagram (Typical Channel)

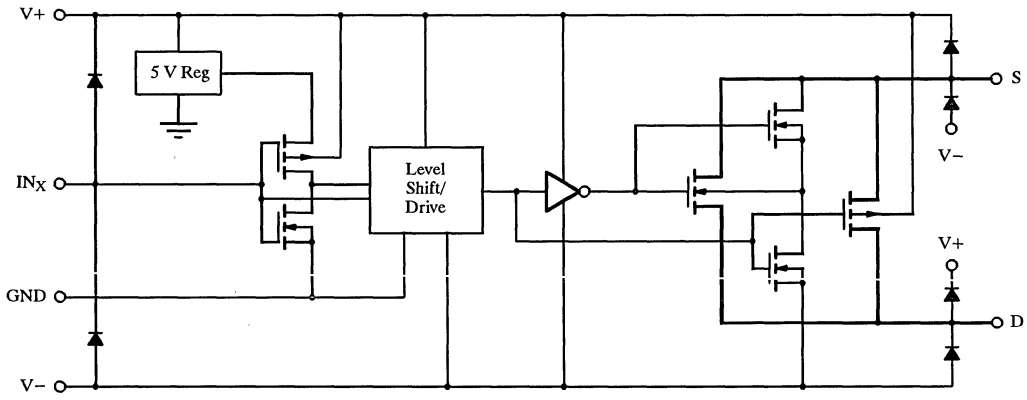
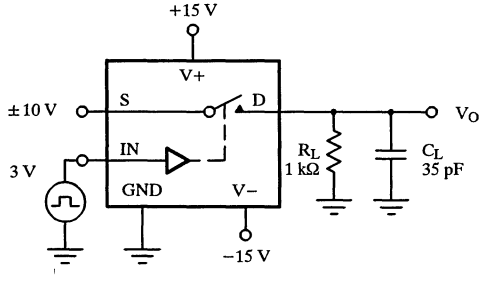
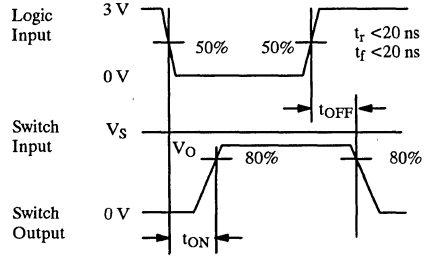


Figure 1.

Test Circuits



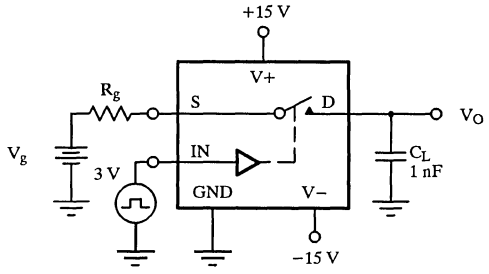
CL (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

Figure 2. Switching Time

Test Circuits (Cont'd)



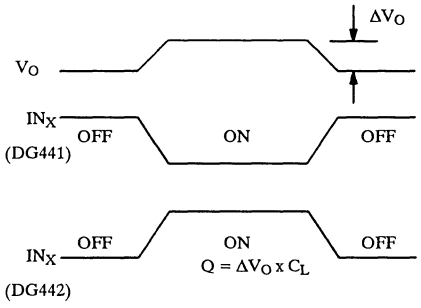


Figure 3. Charge Injection

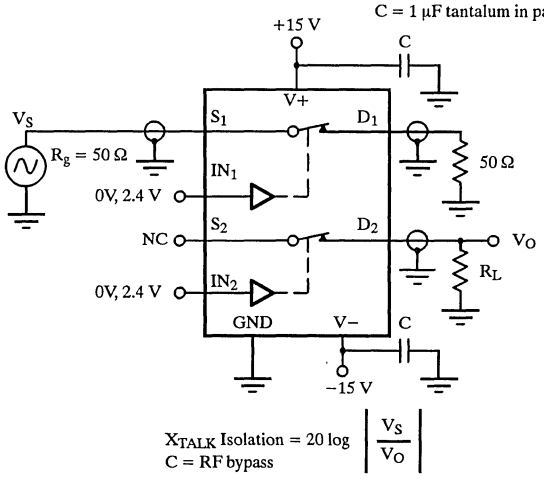


Figure 4. Crosstalk

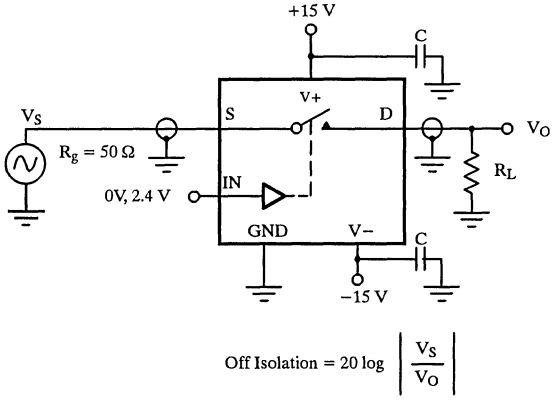


Figure 5. Off Isolation

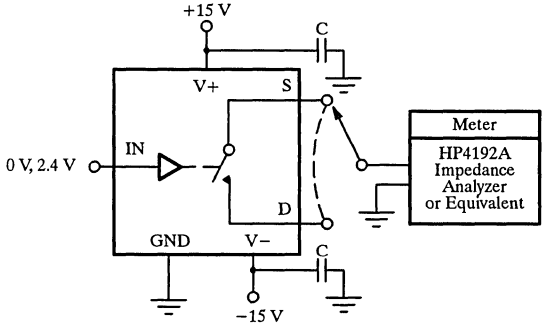


Figure 6. Source/Drain Capacitances

Applications

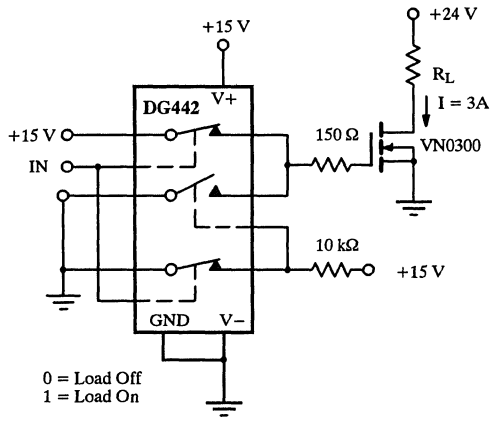


Figure 7. Power MOSFET Driver

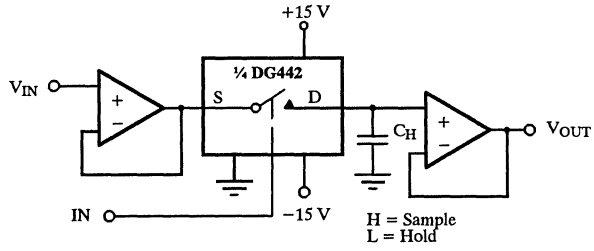


Figure 8. Open Loop Sample-and-Hold

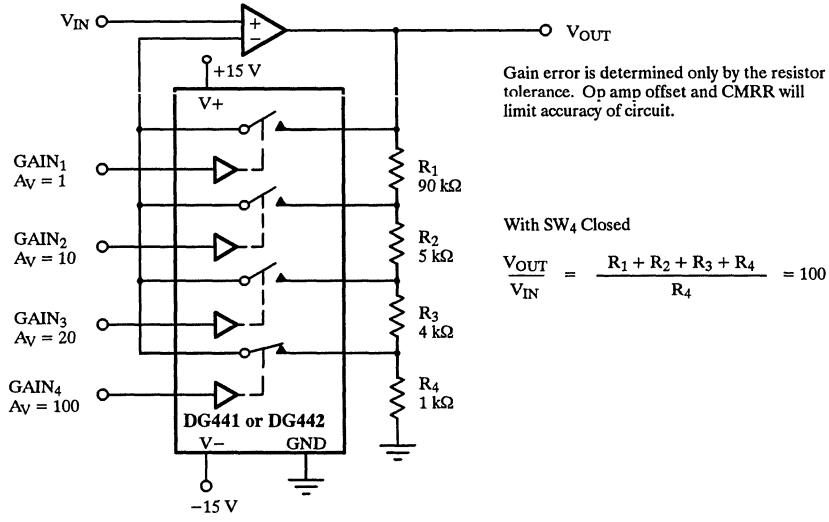


Figure 9. Precision-Weighted Resistor Programmable-Gain Amplifier

Quad SPST CMOS Analog Switches

Features

- Low On-Resistance: 50 Ω
- Low Leakage: 80 pA
- Low Power Consumption: 22 nW
- Fast Switching Action—t_{ON}: 120 ns
- Low Charge Injection
- DG211/DG212 Upgrades
- TTL/CMOS Logic Compatible

Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Errors
- Simple Interfacing

Applications

- Audio Switching
- Battery Powered Systems
- Data Acquisition
- Sample-and-Hold Circuits
- Telecommunication Systems
- Automatic Test Equipment
- Single Supply Circuits
- Hard Disk Drives

Description

The DG444/DG445 monolithic quad analog switches are designed to provide high speed, low error switching of analog signals. The DG444 has a normally closed function. The DG445 has a normally open function. Combining low power (22 nW, typ) with high speed (t_{ON}: 120 ns, typ), the DG444/DG445 are ideally suited for upgrading DG211/212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

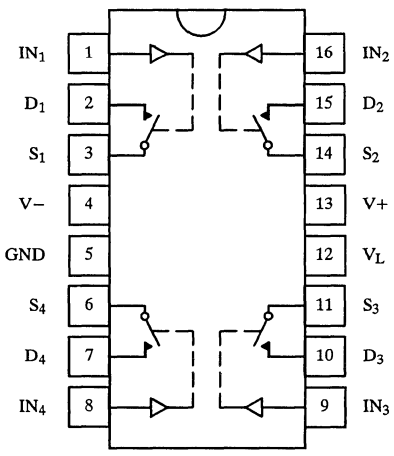
To achieve high-voltage ratings and superior switching performance, the DG444/DG445 are built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

Functional Block Diagram and Pin Configuration

DG444

Dual-In-Line and SOIC



Top View

Truth Table

Logic	DG444	DG445
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V, Logic "1" ≥ 2.4 V
Switches Shown for DG444 Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
−40°C to 85°C	16-Pin Plastic DIP	DG444DJ
		DG445DJ
	16-Pin Narrow SOIC	DG444DY
		DG445DY

1

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
V_L ..... (GND −0.3 V) to (V+) + 0.3 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] ..... 450 mW
16-Pin Narrow Body SOIC[d] ..... 600 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C

Specifications for Dual Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch								
Analog Signal Range[d]	V_{ANALOG}			Full	−15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±8.5 V V+ = 13.5 V, V− = −13.5 V		Room Full		50	85 100	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V− = −16.5 V V_D = ±15.5 V, V_S = ∓15.5 V		Room Full	−0.5 −5	±0.01	0.5 5	nA
	$I_{D(off)}$			Room Full	−0.5 −5	±0.01	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V− = −16.5 V V_S = V_D = ±15.5 V		Room Full	−0.5 −10	±0.08	0.5 10	
Digital Control								
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V		Full	−500	−0.01	500	nA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V		Full	−500	0.01	500	
Dynamic Characteristics								
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ±10 V, See Figure 2		Room		120	250	ns
Turn-Off Time	t_{OFF}		DG441	Room		110	140	
			DG442	Room		160	210	
Charge Injection[e]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω		Room		−1		pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		Room		60		dB
Crosstalk (Channel-to-Channel)[d]	X_{TALK}			Room		100		
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz		Room		4		pF
Drain Off Capacitance	$C_{D(off)}$			Room		4		
Channel On Capacitance	$C_{D(on)}$	V_{ANALOG} = 0 V		Room		16		

Specifications for Dual Supplies (Cont'd)

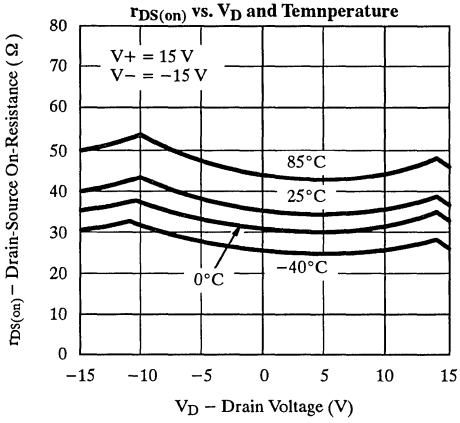
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V	Room Full		0.001	1 5	µA
Negative Supply Current	I−		Room Full	−1 −5	−0.0001		
Logic Supply Current	I_L		Room Full		0.001	1 5	
Ground Current	I_{GND}		Room Full	−1 −5	−0.001		

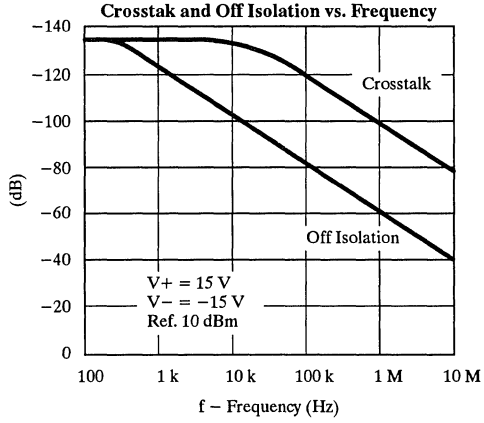
Specifications for Unipolar Supplies

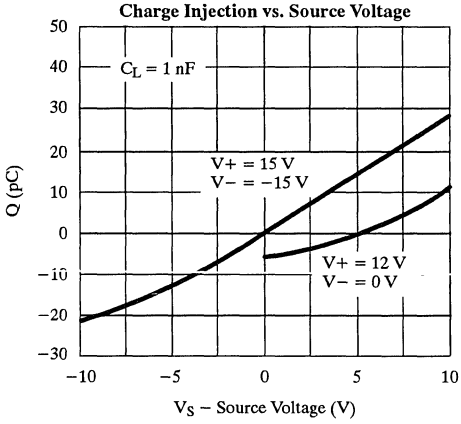
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance[d]	$r_{DS(on)}$	I_S = −10 mA, V_D = 3 V, 8 V V+ = 10.8 V, V_L = 5.25 V	Room Full		100	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V See Figure 2	Room		300	450	ns
Turn-Off Time	t_{OFF}		Room		60	200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room		2		pC
Power Supplies							
Positive Supply Current	I+	V+ = 13.2 V, V_{IN} = 0 or 5 V	Room Full		0.001	1 5	µA
Negative Supply Current	I−	V_{IN} = 0 or 5 V	Room Full	−1 −5	−0.0001		
Logic Supply Current	I_L	V_L = 5.25 V, V_{IN} = 0 or 5 V	Room Full		0.001	1 5	
Ground Current	I_{GND}	V_{IN} = 0 or 5 V	Room Full	−1 −5	−0.001		

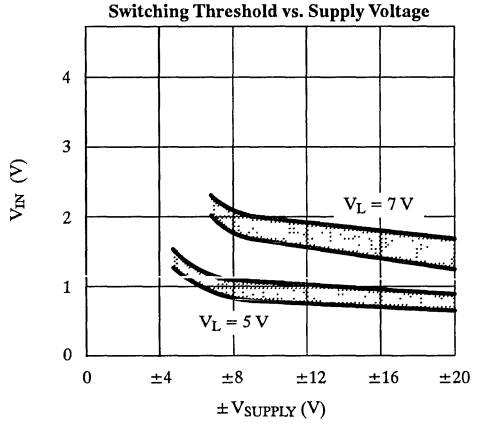
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

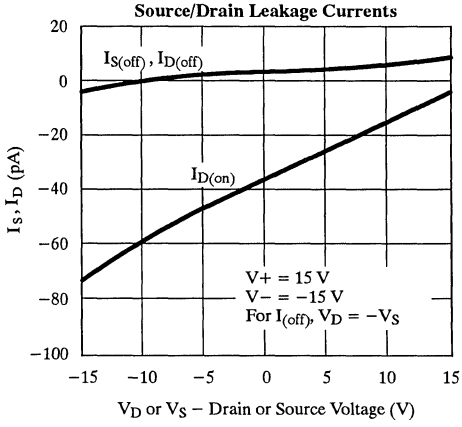
Typical Characteristics

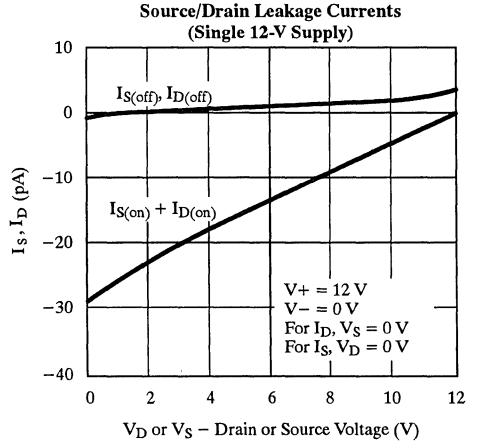




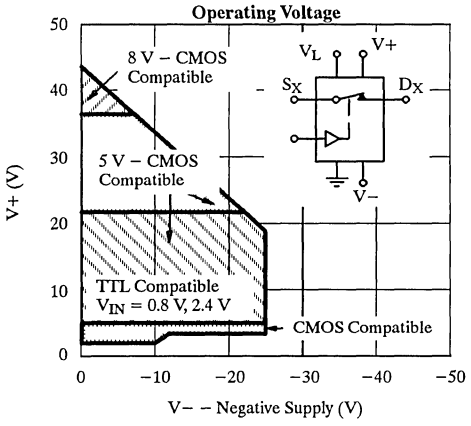


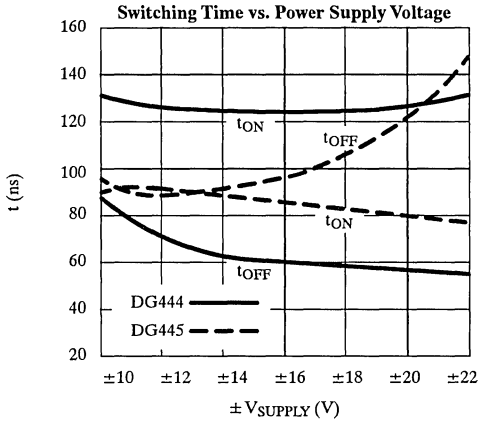


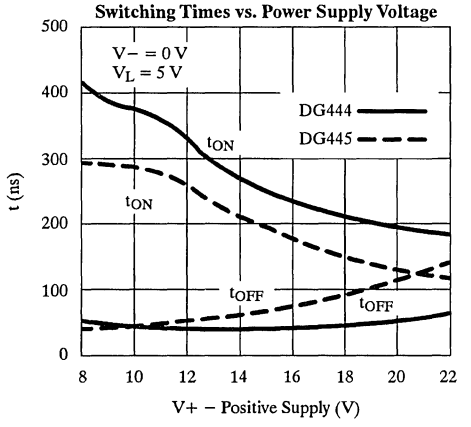


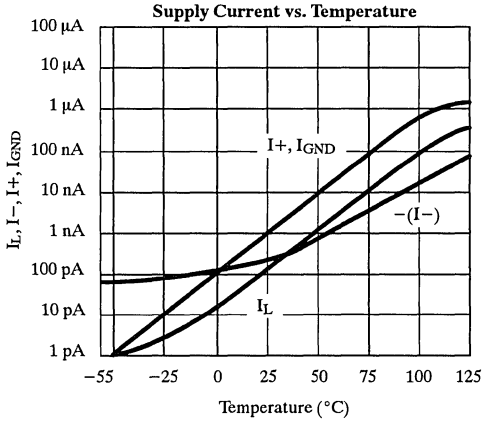


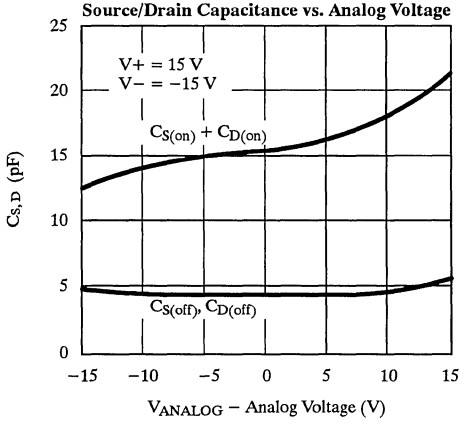
Typical Characteristics (Cont'd)

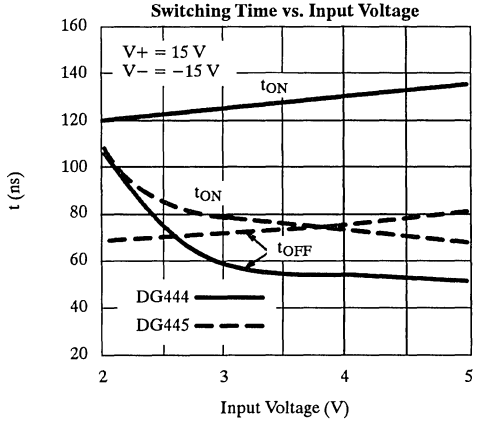












1

Schematic Diagram (Typical Channel)

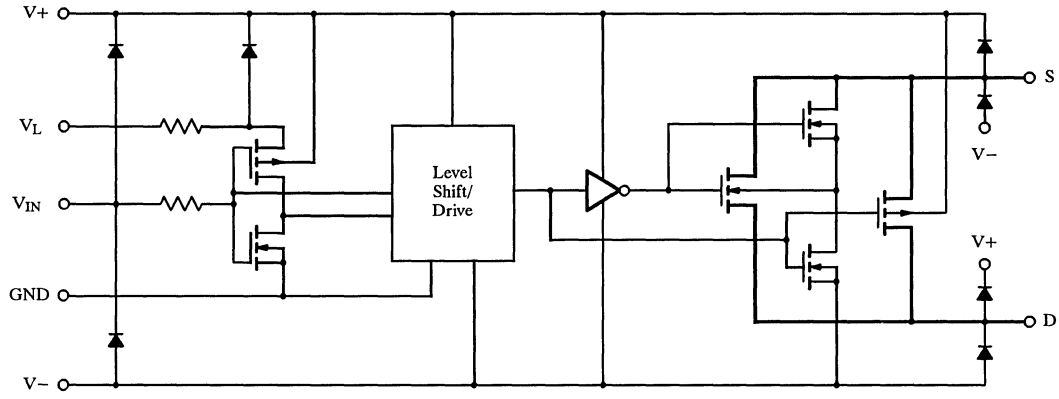
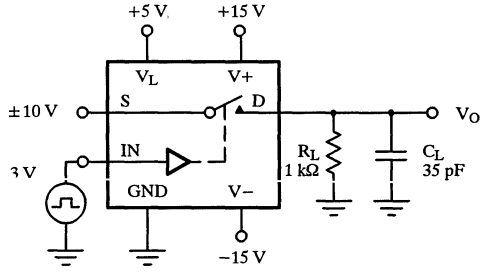
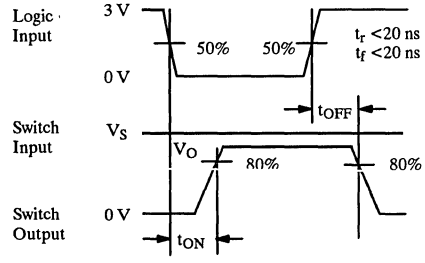


Figure 1.

Test Circuits

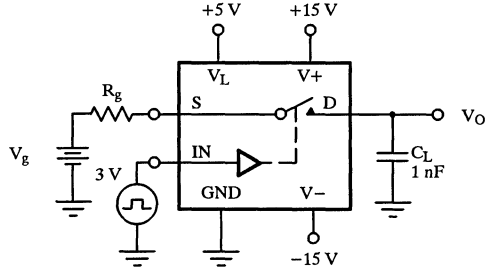


C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG445.

Figure 2. Switching Time



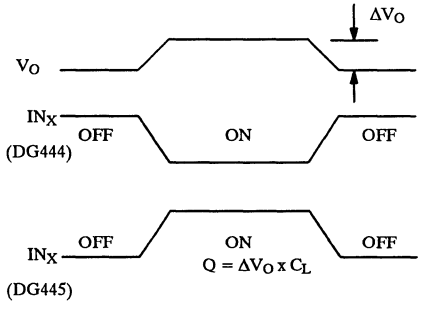


Figure 3. Charge Injection

Test Circuits (Cont'd)

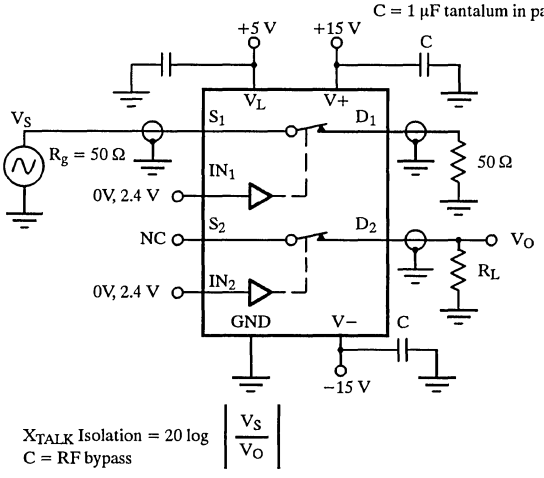


Figure 4. Crosstalk

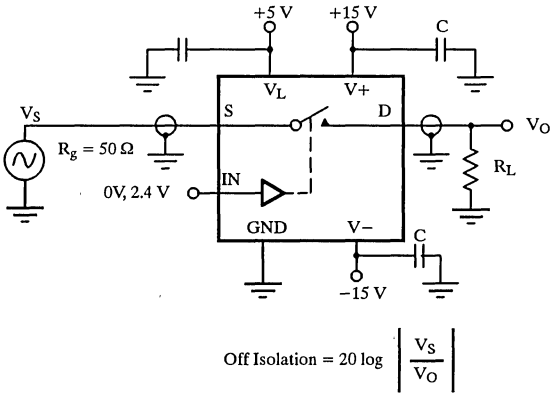


Figure 5. Off Isolation

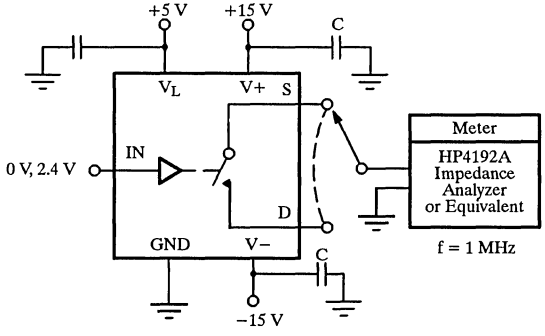


Figure 6. Source/Drain Capacitances

Applications

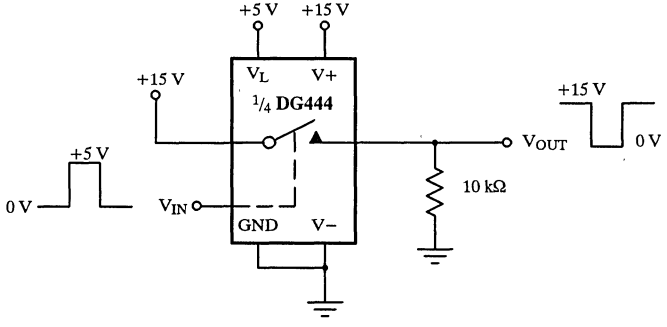


Figure 7. Level Shifter

Applications (Cont'd)

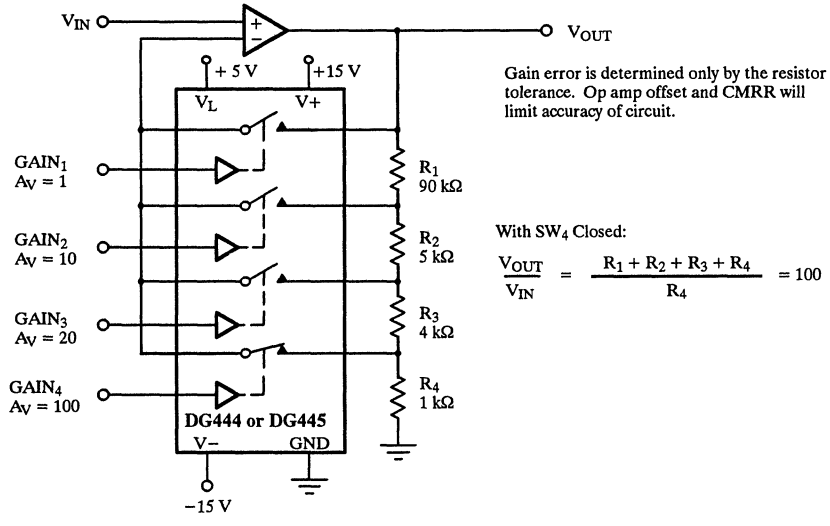


Figure 8. Precision-Weighted Resistor Programmable-Gain Amplifier

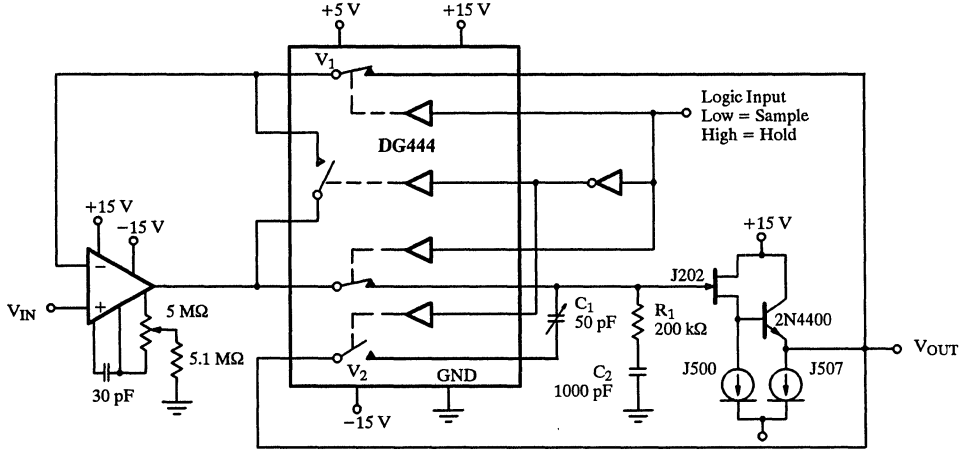


Figure 9. Precision Sample-and-Hold

Wideband/Video "T" Switches

Features

- Wide Bandwidth: 500 MHz
- Low Crosstalk: −85 dB
- High Off-Isolation: −80 dB @ 5 MHz
- "T" Switch Configuration
- TTL Logic Compatible
- Fast Switching—t_{ON}: 45 ns
- Low $r_{DS(on)}$: 30 Ω

Benefits

- Flat Frequency Response
- High Color Fidelity
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption
- Improved Data Throughput

Applications

- RF and Video Switching
- RGB Switching
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLR Systems
- Video Multiplexing

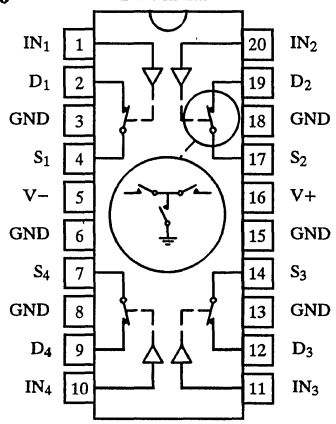
Description

The DG540/541/542 are high performance monolithic wideband/video switches designed for switching RF, video and digital signals. By utilizing a "T" switch configuration on each channel, these devices achieve exceptionally low crosstalk and high off-isolation. The crosstalk and off-isolation of the DG540 are further improved by the introduction of extra GND pins between signal pins.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG540 family is built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on.

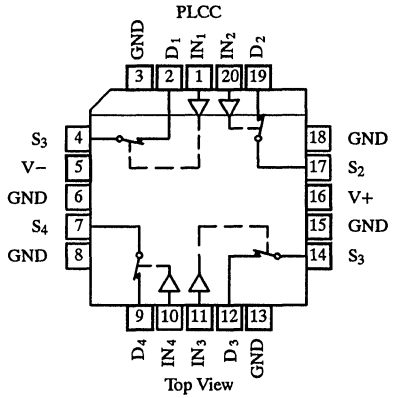
Functional Block Diagrams and Pin Configurations

DG540 Dual-In-Line



Top View

PLCC



Top View

Ordering Information – DG540

Temp Range	Package	Part Number
−40 to 85°C	20-Pin Plastic DIP	DG540DJ
	20-Pin PLCC	DG540DN
−55 to 125°C	20-Pin Sidebraze	DG540AP
		DG540AP/883

Truth Table

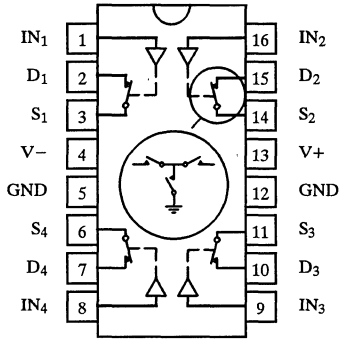
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2 V
Switches Shown for Logic "1" Input

Functional Block Diagrams and Pin Configurations (Cont'd)

DG541

Dual-In-Line and SOIC



Top View

Truth Table – DG541

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2 V

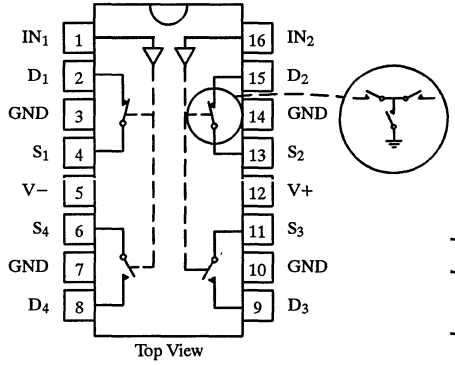
Switches Shown for Logic "1" Input

Ordering Information – DG541

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG541DJ
	16-Pin Narrow SOIC	DG541DY
−55 to 125°C	16-Pin Sidebraze	DG541AP
		DG541AP/883

DG542

Dual-In-Line and SOIC



Top View

Truth Table – DG542

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2 V

Switches Shown for Logic "1" Input

Ordering Information – DG542

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG542DJ
	16-Pin Narrow SOIC	DG542DY
−55 to 125°C	16-Pin Sidebraze	DG542AP
		DG542AP/883

Absolute Maximum Ratings

V+ to V− ..... −0.3 V to 21 V
V+ to GND ..... −0.3 V to 21 V
V− to GND ..... −19 V to +0.3 V
Digital Inputs ..... (V−) −0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V−) −0.3 V to (V−) +14 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 20 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max) ..... 40 mA
Storage Temperature (AP Suffix) ..... −65 to 150°C
(DJ, DN, DY Suffixes) ... −65 to 125°C

Power Dissipation (Package)a
16-Pin Plastic DIP[b] ..... 470 mW
20-Pin Plastic DIP[c] ..... 800 mW
16-Pin Narrow Body SOIC[d] ..... 640 mW
20-Pin PLCC[d] ..... 800 mW
16-, 20-Pin Sidebraze DIP[e] ..... 900 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 6.5 mW/°C above 25°C
c. Derate 7 mW/°C above 25°C
d. Derate 10 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_{INH} = 2 V, V_{INL} = 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffixes −40 to 85°C Min[d]	D Suffixes −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range	V_{ANALOG}	V− = −5 V, V+ = 12 V		Full		−5	8	−5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 0 V		Room Full	30		60 100		60 75	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$			Room	2		6		6	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V		Room Full	−0.05	−10 −500	10 500	−10 −100	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V		Room Full	−0.05	−10 −500	10 500	−10 −100	10 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V		Room Full	−0.05	−10 −1000	10 1000	−10 −100	10 100	
Digital Control										
Input Voltage High	V_{INH}			Full		2		2		V
Input Voltage Low	V_{INL}			Full			0.8		0.8	
Input Current	I_{IN}	V_{IN} = GND or V+		Room Full	0.05	−1 −20	1 20	−1 −20	1 20	µA
Dynamic Characteristics										
On State Input Capacitance[e]	$C_{S(on)}$	V_S = V_D = 0 V		Room	14		20		20	pF
Off State Input Capacitance[e]	$C_{S(off)}$	V_S = 0 V		Room	2		4		4	
Off State Output Capacitance[e]	$C_{D(off)}$	V_D = 0 V		Room	2		4		4	
Bandwidth	BW	R_L = 50 Ω, See Figure 5		Room	500					MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF 50% to 90% See Figure 2	DG540 DG541	Room Full	45		70 130		70 130	ns
			DG542	Room Full	55		100 160		100 160	
Turn Off Time	t_{OFF}		DG540 DG541	Room Full	20		50 85		50 85	
			DG542	Room Full	25		60 85		60 85	
Charge Injection	Q	C_L = 1000 pF, V_S = 0 V See Figure 3		Room	−25					pC
Off Isolation	OIRR	R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz, See Figure 4	DG540	Room	−80					dB
			DG541	Room	−60					
			DG542	Room	−75					
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω f = 5 MHz, See Figure 6		Room	−85					

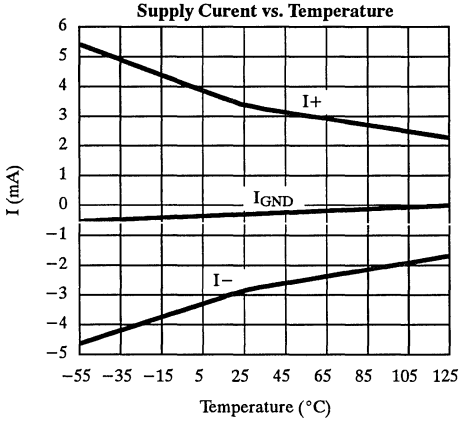
1

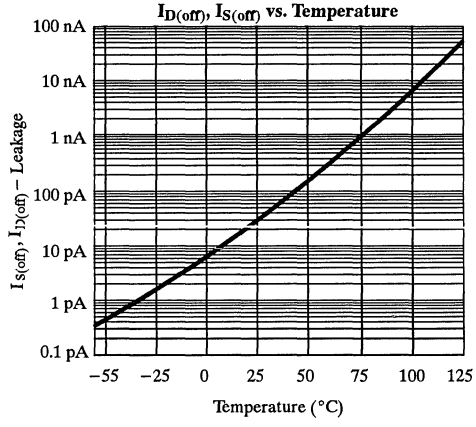
Specifications[a]

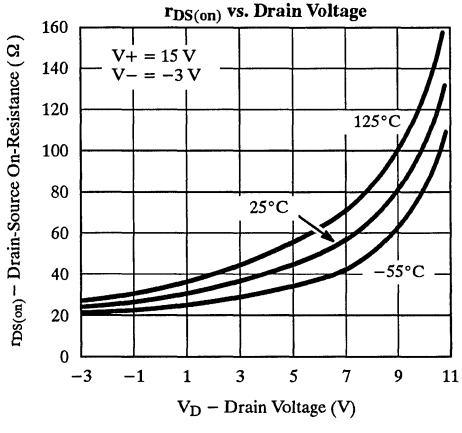
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_{INH} = 2 V, V_{INL} = 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffixes −40 to 85°C Min[d]	D Suffixes −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	All Channels On or Off	Room Full	3.5		6 9		6 9	mA
Negative Supply Current	I−		Room Full	−3.2	−6 −9		−6 −9		

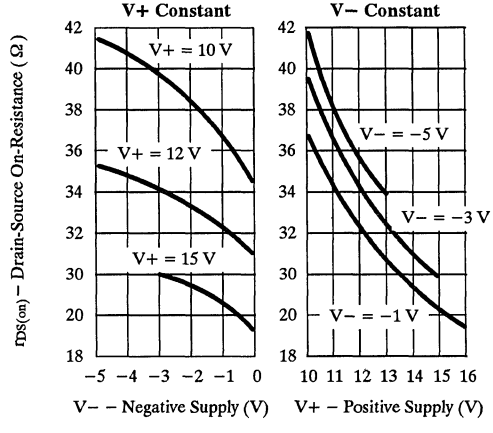
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics



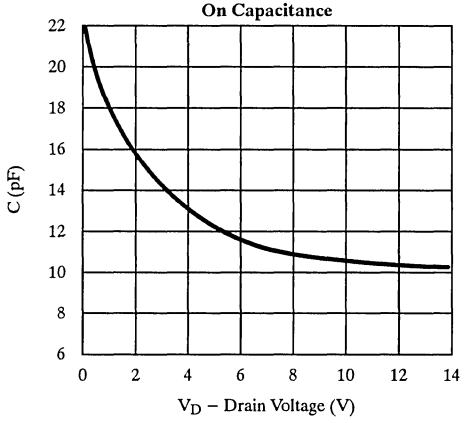




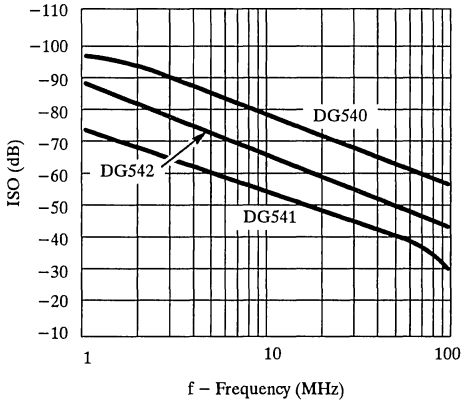


Typical Characteristics (Cont'd)

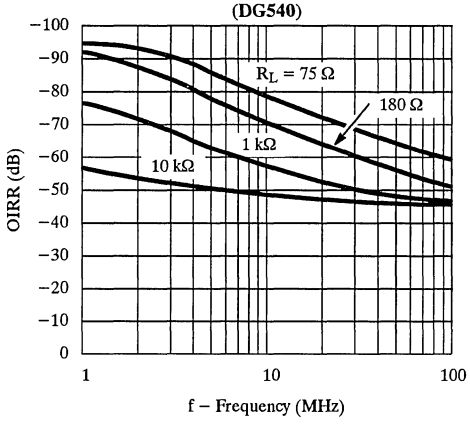
On Capacitance



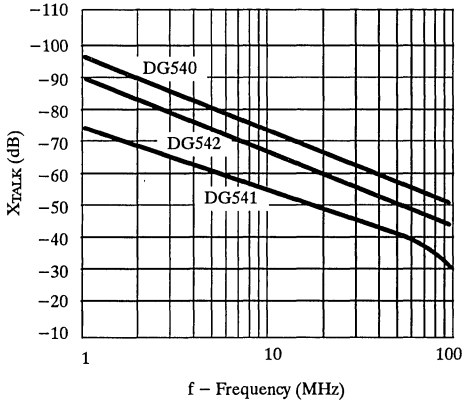
Off Isolation



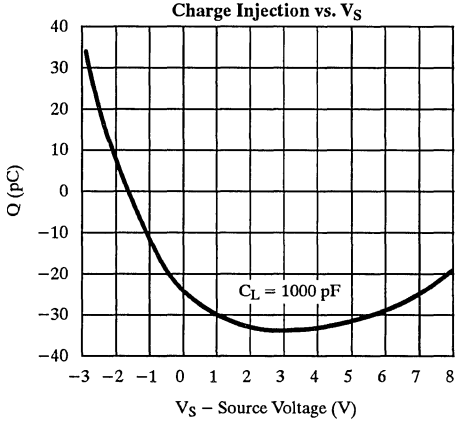
Off Isolation vs. Frequency and Load Resistance (DG540)



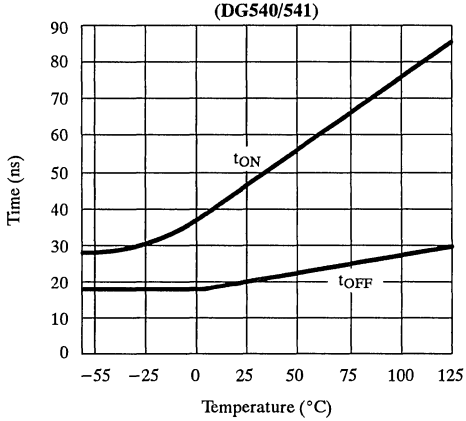
All Hostile Crosstalk



Charge Injection vs. V_S



Switching Times vs. Temperature (DG540/541)



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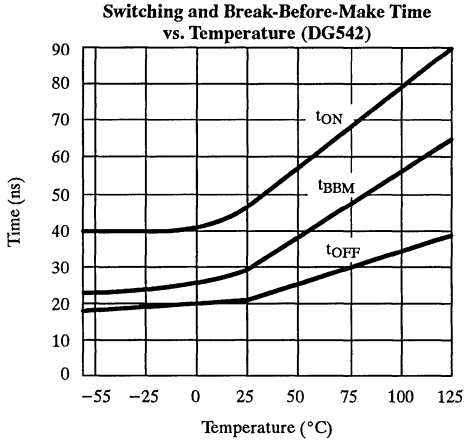
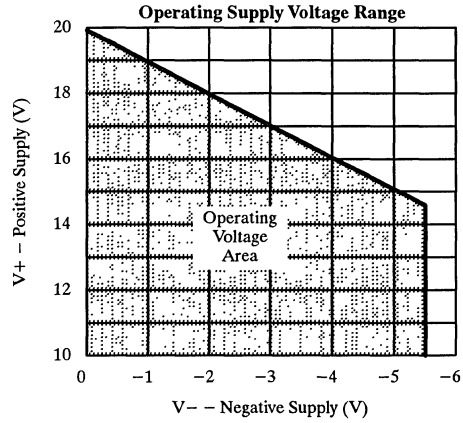
Typical Characteristics (Cont'd)





Schematic Diagram (Typical Channel)

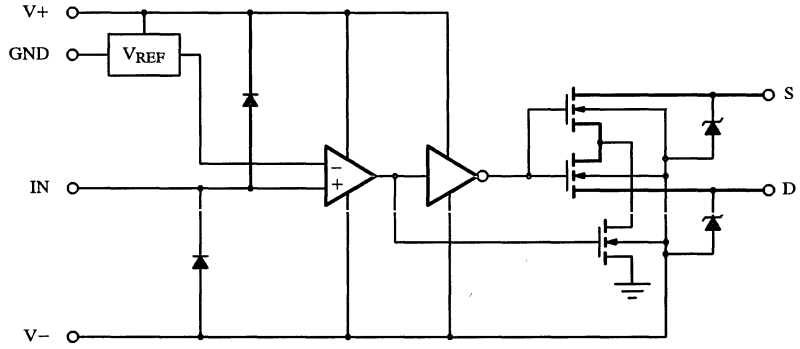
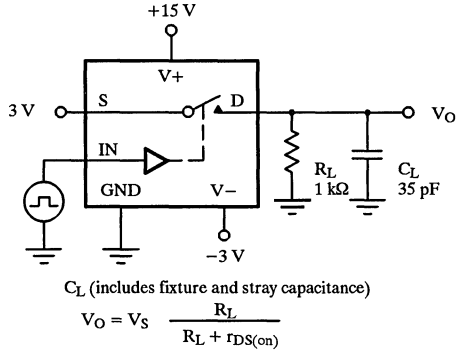


Figure 1.

Test Circuits



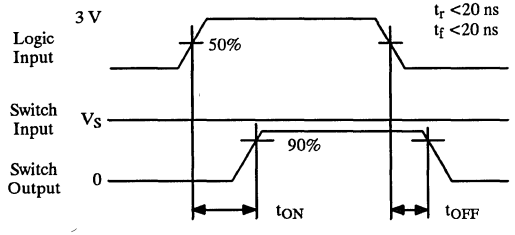
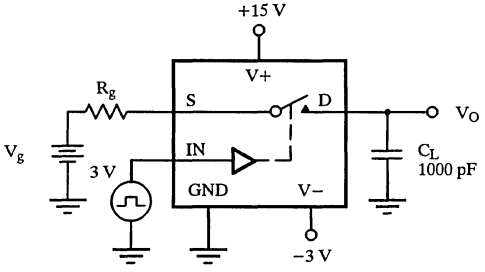
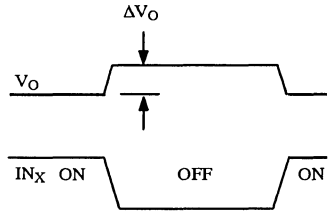


Figure 2. Switching Time

Test Circuits (Cont'd)





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$

Figure 3. Charge Injection

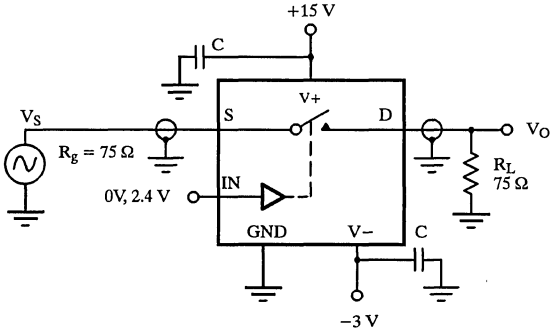


Figure 4. Off Isolation

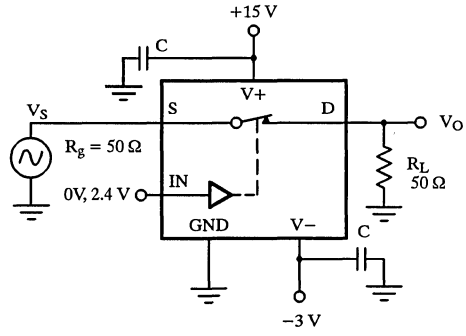
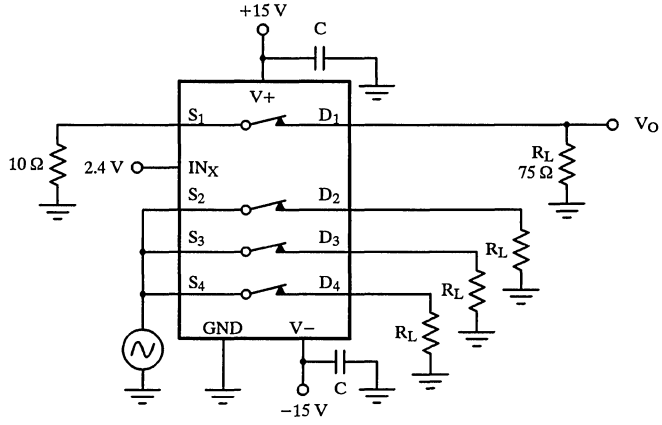


Figure 5. Bandwidth



$$X_{TALK(AH)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

Figure 6. All Hostile Crosstalk

1

Applications

Device Description

The DG540/541/542 family of wideband switches offers true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these "T" switches provide excellent off-isolation with a bandwidth of around 500 MHz (350 MHz for DG541). Silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance [$r_{DS(on)}$] and capacitance [$C_{S(on)}$]. This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The −3-dB bandwidth of the DG540 is typically 500 MHz (into 50 Ω). This measured figure of 500 MHz illustrates that the switch channel can not be represented by a two stage RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi stage network of R's and C's making up the total $r_{DS(on)}$ and $C_{S(on)}$. See Application Note AN502 for more details.

Off-Isolation and Crosstalk

Off-isolation and crosstalk are affected by the load resistance and parasitic inter-electrode capacitances. Higher off-isolation is achieved with lower values of R_L. However, low values of R_L increase insertion loss requiring gain adjustments down the line. Stray capacitances, even a fraction of 1 pF, can cause a large crosstalk increase. Good layout and ground shielding techniques can considerably improve your ac circuit performance.

Power Supplies

A useful feature of the DG54X family is its power supply flexibility. It can be operated from a single positive supply (V+) if required (V− connected to ground).

Note that the analog signal must not exceed V− by more than −0.3 V to prevent forward biasing the substrate p-n junction. The use of a V− supply has a number of advantages:

(291) It allows flexibility in analog signal handling, i.e., with V− = −5 V and V+ = 12 V; up to ±5-V ac signals can be controlled.

(292) The value of on capacitance [$C_{S(on)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(on)}$ for an increasing V body−source. Note, however, that to increase V− normally requires V+ to be reduced (since V+ to V− = 21 V max.). Reduction in V+ causes an increase in $r_{DS(on)}$, hence a compromise has to be achieved. It is also useful to note that optimum video linearity performance (e.g., differential phase and gain) occurs when V− is around −3 V.

(293) V− eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG54X is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential.

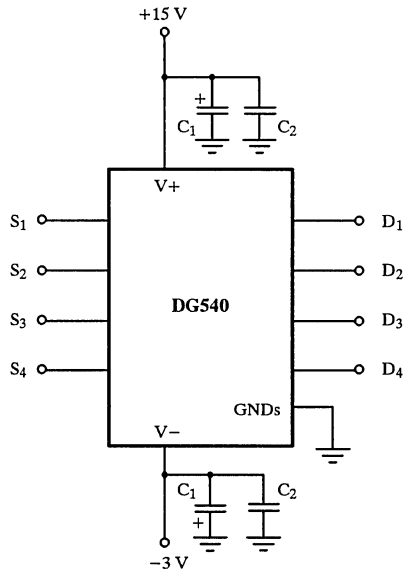
Rules:

(1) Decoupling capacitors should be incorporated on all power supply pins (V+, V−). (See Figure 7.)

(2) They should be mounted as close as possible to the device pins.

(3) Capacitors should have good high frequency characteristics – tantalum bead and/or monolithic ceramic types are adequate.

Suitable decoupling capacitors are 1- to 10-μF tantalum bead, plus 10- to 100-nF ceramic.



C_1 = 10 µF Tantalum
C_2 = 0.1 µF Ceramic

Figure 7. Supply Decoupling

Board Layout

PCB layout rules for good high frequency performance must be observed to achieve the performance boasted by the DG540. Some tips for minimizing stray effects are:

(1) Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.

(2) Keep signal paths as short as practically possible, with all channel paths of near equal length.

(3) Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current flowing through ground path parasitic resistance from coupling between channels.

Figure 8 shows a 4-channel video multiplexer using a DG540.

Figure 9 shows an RGB selector switch using two DG542s.

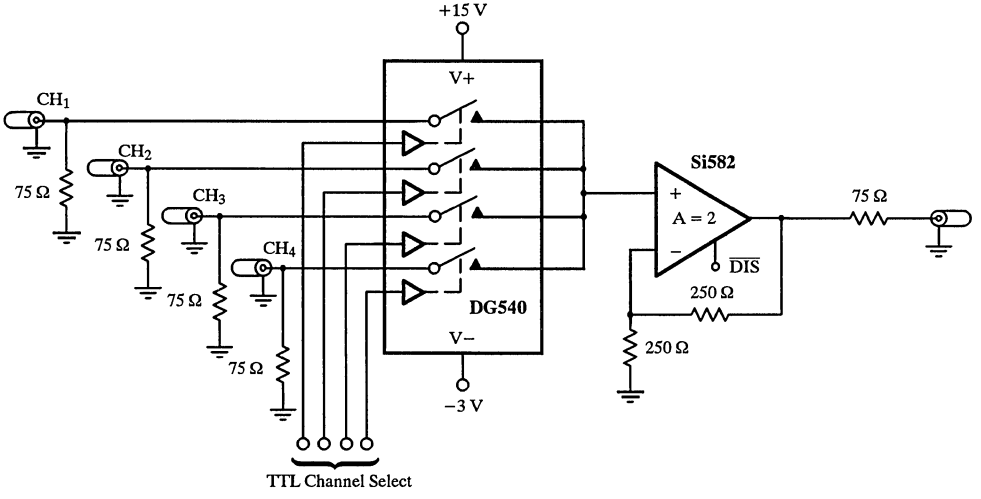


Figure 8. 4 by 1 Video Multiplexing Using the DG540

Applications (Cont'd)

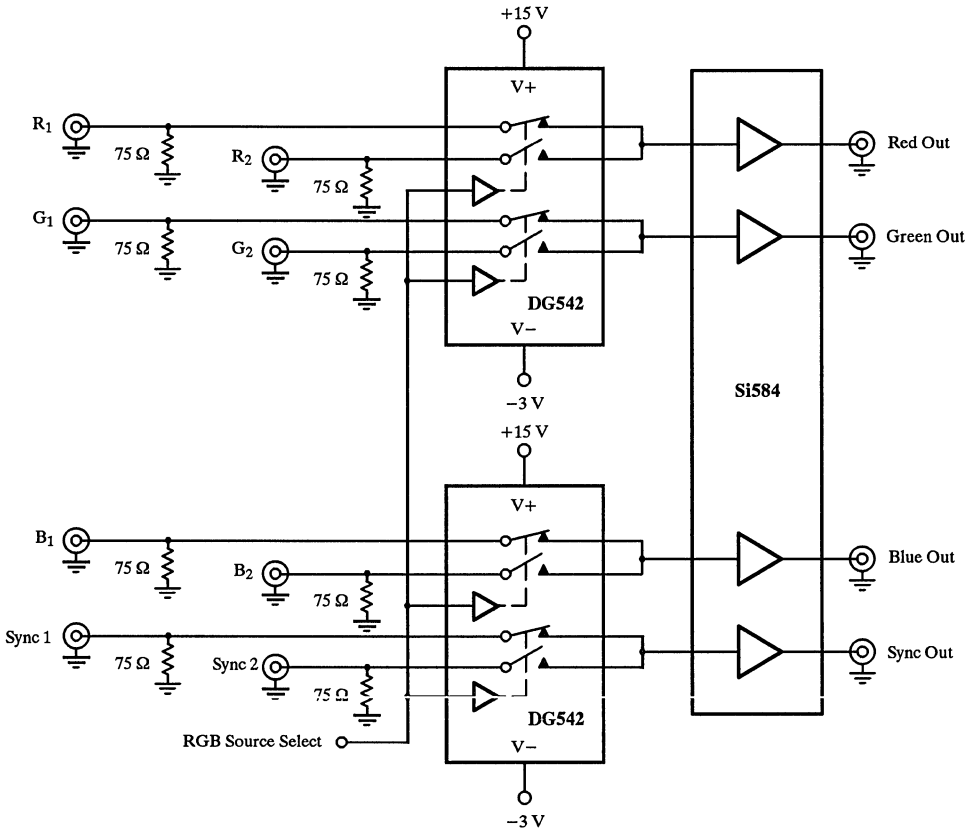


Figure 9. RGB Selector Using Two DG542s

High-Speed Quad CMOS Analog Switch

Features

- Fast Switching Action—t_{ON}: 30 ns
- Low On-Resistance—$r_{DS(on)}$: 20 Ω
- Single-Supply Operation
- Low Charge Injection
- TTL and CMOS Logic Compatible

Benefits

- Improved Data Throughput
- Reduced Switching Errors
- Simplified Power Supply
- Reduced Switching Transients
- Simplified Interfacing
- High Reliability

Applications

- Hard Disk Drives
- Fast Sample-and-Hold Circuits
- Precision Instrumentation
- Computer Peripherals
- Low Noise Op Amp Gain Switching
- High-Rel Systems

Description

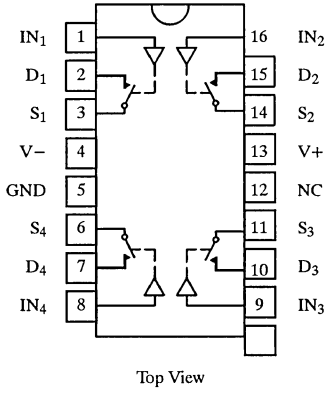
The DG601 is a high performance quad SPST CMOS analog switch intended for applications where fast switching, low charge injection and low on-resistance are required. The DG601 features single-supply operation, and is TTL-compatible with either a single 12-V supply, a single 5-V supply, or with ±5-V supplies.

Applications for the DG601 include 12-V systems requiring TTL or 5-V logic levels, such as disk drives and other computer peripherals. The fast switching time and low charge injection make the DG601 ideal for high speed data acquisition applications such as sample and hold amplifiers, channel selection and gain ranging.

The DG601 is built on the Siliconix proprietary PolyMOS process, allowing low parasitic capacitance to facilitate high speed switching.

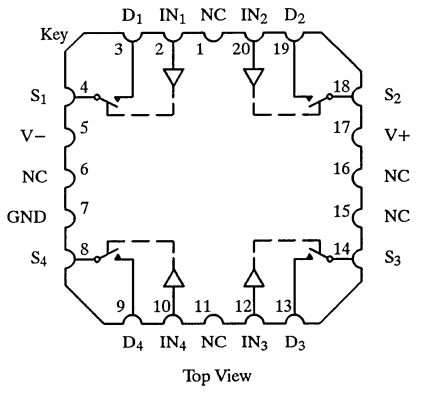
Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

LCC



Top View

Ordering Information

Temp Range	Package	Part Number
40 to 85°C	16-Pin Plastic DIP	DG601DJ
	16-Pin Narrow SOIC	DG601DY
−55 to 125°C	16-Pin CerDIP	DG601AK
		DG601AK/883
	LCC-20	DG601AZ/883

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

1

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 22 V
GND ..... 13 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) plus 2 V or 30 mA, whichever occurs first
Current (any terminal) ..... 30 mA
Current S or D (Pulsed 1 ms at 10% duty cycle) ..... 100 mA
Storage Temperature (AK, AZ Suffixes) ..... −65 to 150°C
(DJ, DY Suffixes) ..... −65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin SOIC[d] ..... 900 mW
16-Pin CerDIP[e] ..... 900 mW
LCC-20[e] ..... 1200 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 7.7 mW/°C above 25°C
e. Derate 12 mW/°C above 75°C

Specifications[a] for Single 12-V Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 10.8 V, I_S = 10 mA, V_D = 2 V, 10 V	Room Full	20		35 50			Ω
On-Resistance Matching[g]	$\Delta r_{DS(on)}$		Room Full	2.2		6 10		6 10	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 13.2 V, V− = 0 V, V_D = 12.2 V, 1 V, V_S = 1 V, 12.2 V	Room Full	±0.01	−4 −100	4 100	−4 −100	4 100	nA
	$I_{D(off)}$		Room Full	±0.01	−4 −100	4 100	−4 −100	4 100	
Channel On Leakage Current	$I_{D(on)}$	V+ = 13.2 V, V− = 0 V, V_S, V_D = 1 V, 12.2 V	Room Full	±0.1	−4 −200	4 200	−4 −200	4 200	
Digital Control									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V	Full	-10^{-5}	−10		−10		µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V	Full	10^{-5}		10		10	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, See Figure 2	Room	30		45		45	ns
Turn-Off Time	t_{OFF}		Room	14		30		30	
Charge Injection	Q	C_L = 1,000 pF, V_{gen} = 6 V, R_{gen} = 0 Ω, See Figure 3	Room	13					pC
Off Isolation Reject Ratio	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	69					dB
Crosstalk	X_{TALK}		Room	88					
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 6 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	20					
Power Supplies									
Positive Supply Current	I+	V+ = 13.2 V, V− = 0 V, V_{IN} = 0 V or 5 V	Room Full	2.2		4 6		4 6	mA
Negative Supply Current	I−		Room Full	−2.1	−4 −6		−4 −6		

Specifications[a] for Dual Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−5	5	−5	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 4.5 V, V− = −4.5 V I_S = −10 mA, V_D = ±3.5 V	Room Full	27		40 60		40 60	Ω
On-Resistance Matching[g]	$\Delta r_{DS(on)}$		Room Full	2		6 10		6 10	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V− = −5.5 V V_D = ∓4.5 V, V_S = ±4.5 V	Room	0.01					nA
	$I_{D(off)}$		Room	0.01					
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V− = 5.5 V V_S = V_D = ±4.5 V	Room	0.1					
Digital Control									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V All Other = 5 V	Room	−10					pA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V All Other = 0 V	Room	10					
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	34					ns
Turn-Off Time	t_{OFF}		Room	20					
Charge Injection	Q	V_{gen} = 0 V, R_{gen} = 0 Ω C_L = 1 nF, See Figure 3	Room	11					pC
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	21					
Power Supplies									
Positive Supply Current	I+	V+ = 5.5 V, V− = −5.5 V V_{IN} = 0 V or 5 V	Room	1.8					mA
Negative Supply Current	I−		Room	−1.8					

Specifications[a] for Single 5-V Supply

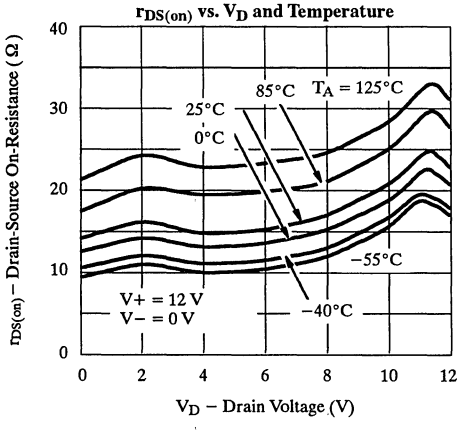
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = 0 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	5	0	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 4.5 V, I_S = −10 mA V_D = 2 V, 3.5 V	Room Full	50		100 140		100 140	Ω
On-Resistance Matching[g]	$\Delta r_{DS(on)}$		Room Full	2		10 15		10 15	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V V_D = 1 V, V_S = 4.5 V	Room	±0.01					nA
	$I_{D(off)}$	V+ = 5.5 V V_D = 4.5 V, V_S = 1 V	Room	±0.01					
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V V_S = V_D = 4.5 V, 1 V	Room	±0.1					

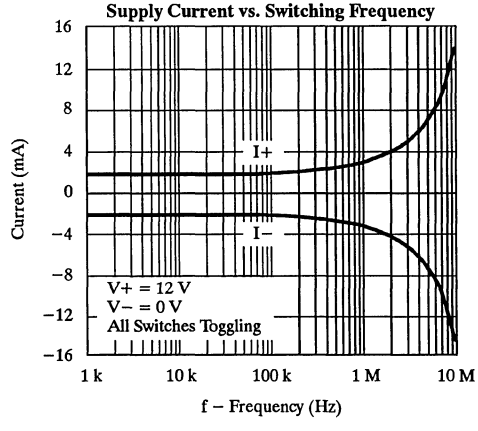
Specifications[a] for Single 5-V Supply (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Digital Control									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V	Room	−10					pA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V	Room	10					
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	32					ns
Turn-Off Time	t_{OFF}		Room	25					
Charge Injection	Q	V_{gen} = 2.5 V, R_{gen} = 0 Ω C_L = 1 nF, See Figure 3	Room	6					pC
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 2.5 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	22					
Power Supplies									
Positive Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 V or 5 V	Room	1.2					mA
Negative Supply Current	I−		Room	−0.8					

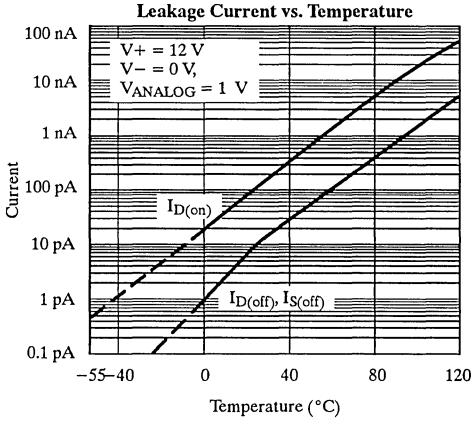
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)}$ compares on-resistance at the specified V_D values.

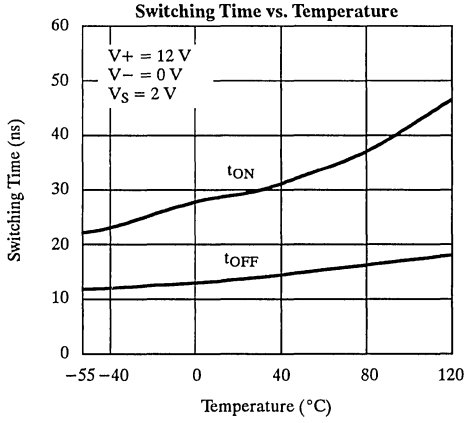
Typical Characteristics

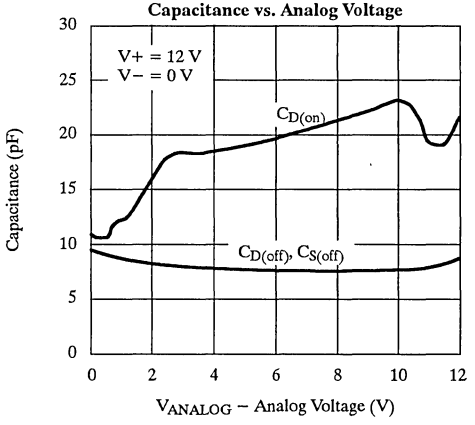


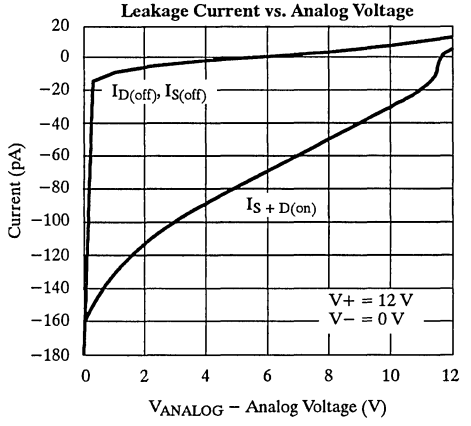


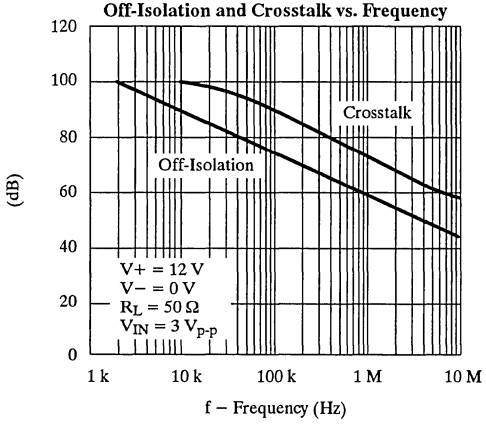
Typical Characteristics (Cont'd)

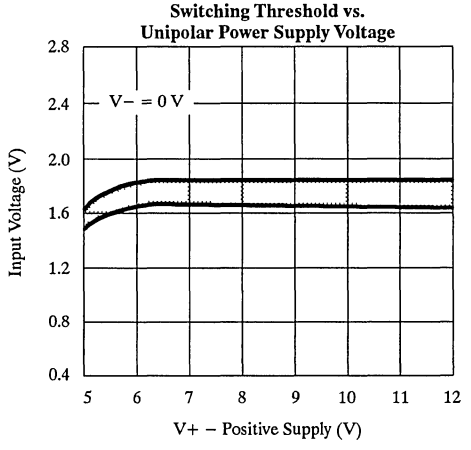












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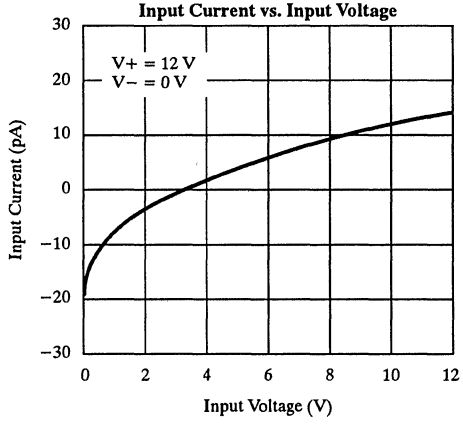
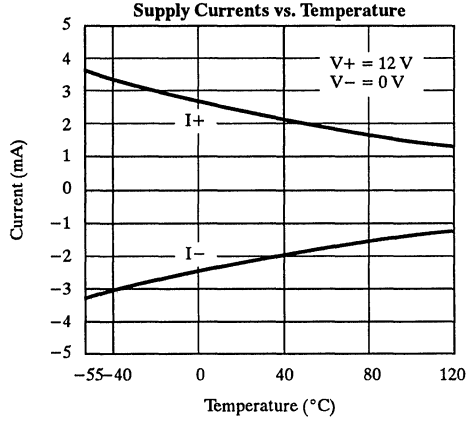
Typical Characteristics (Cont'd)

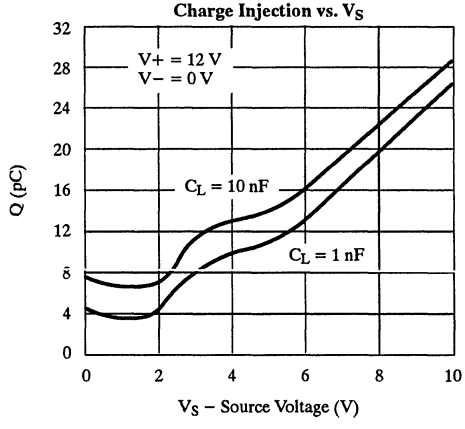
Input Current vs. Input Voltage



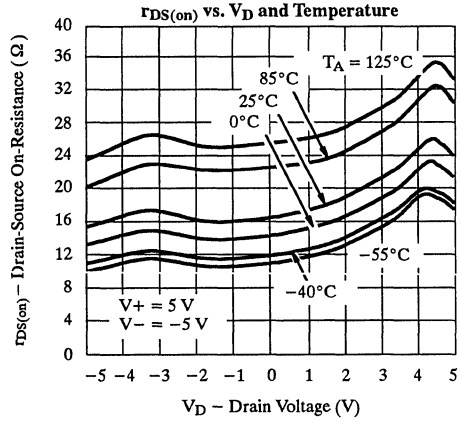
Supply Currents vs. Temperature



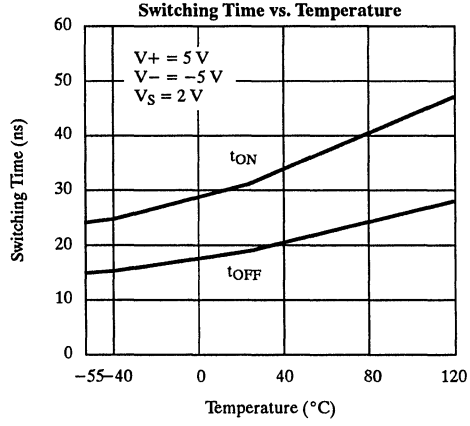
Charge Injection vs. V_S



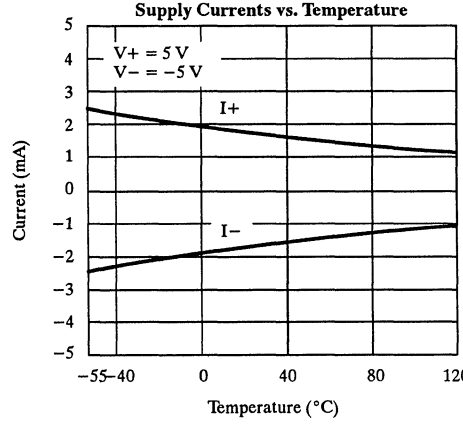
$r_{DS(on)}$ vs. V_D and Temperature



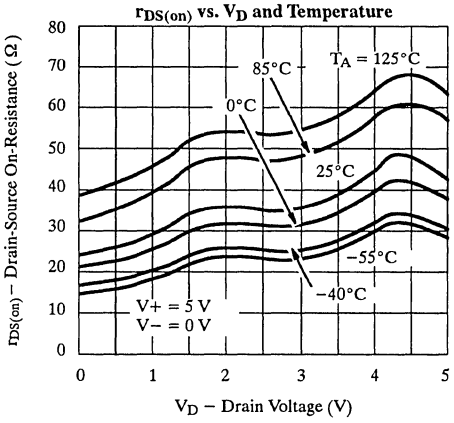
Switching Time vs. Temperature

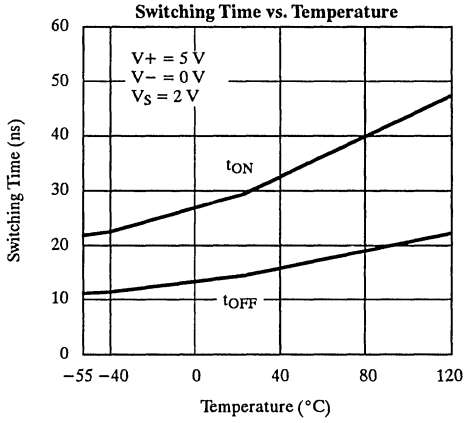


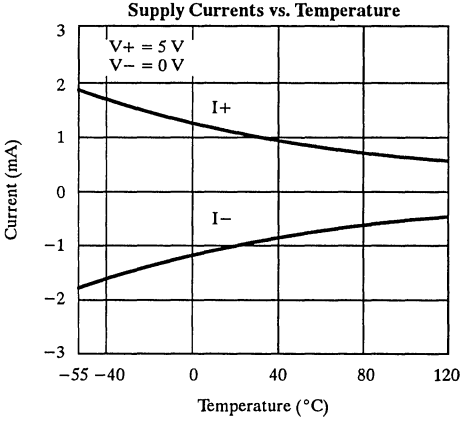
Supply Currents vs. Temperature

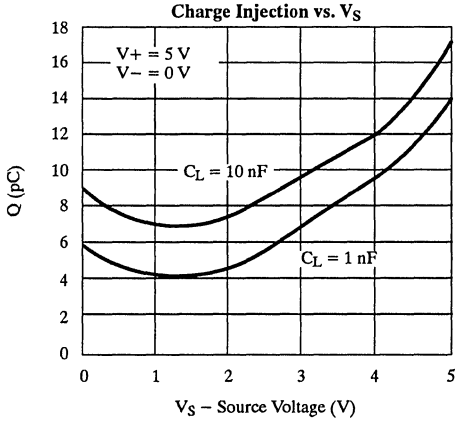


Typical Characteristics (Cont'd)









Schematic Diagram (Typical Channel)

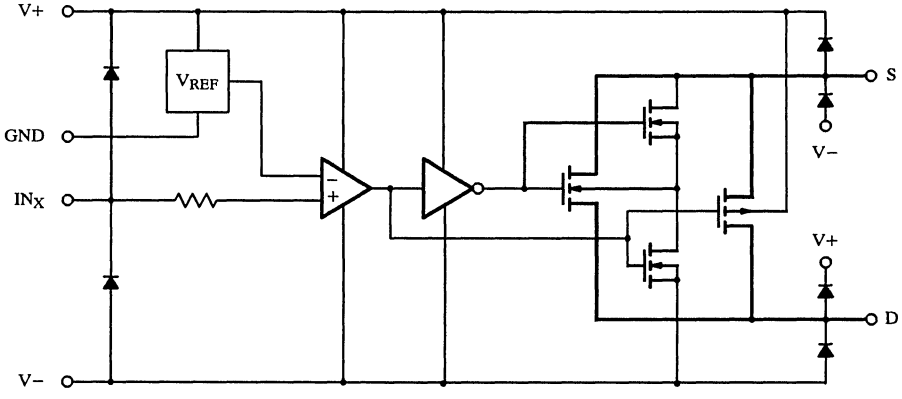
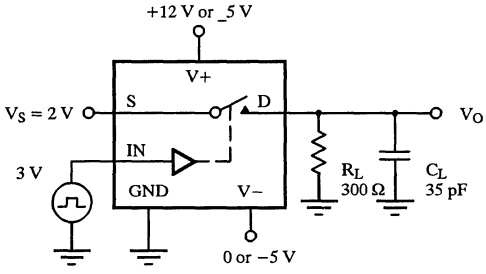
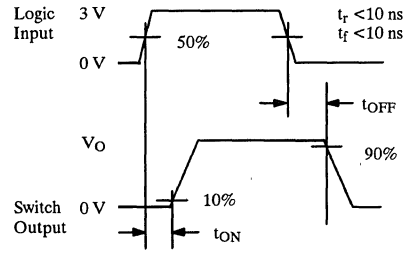


Figure 1

Test Circuits

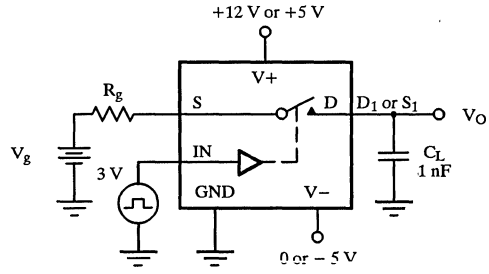




C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2 Switching Time



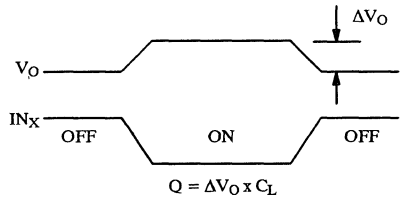
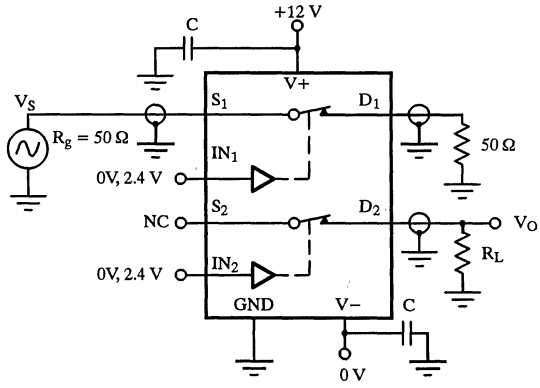


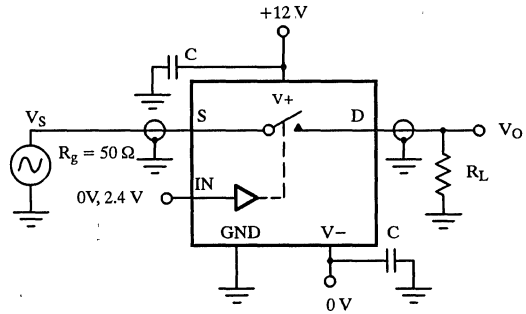
Figure 3 Charge Injection



$$X_{TALK}\ \text{Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 4 Crosstalk



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 5 Off Isolation

Test Circuits (Cont'd)

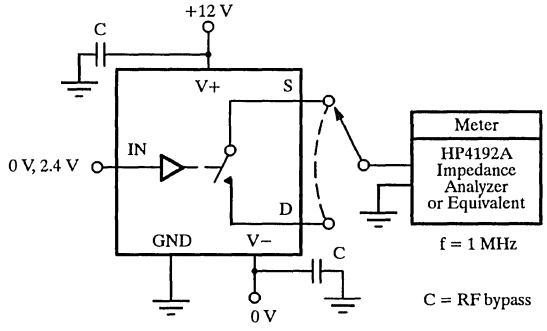


Figure 6 Source/Drain Capacitances

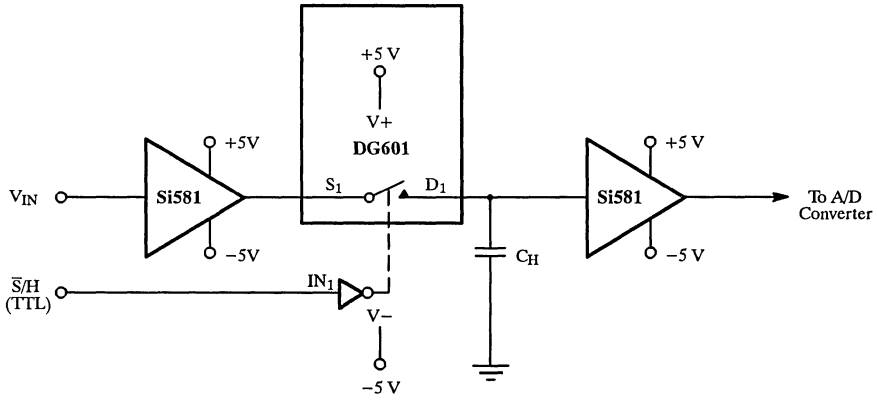


Figure 7 Simple High-Speed Sample-and-Hold Circuit for Data Acquisition System Front Ends

1

Applications

Application Examples

Analog switches are found in a variety of applications. The DG601 is useful in applications that require low-supply voltages, high-speed switching, and/or low on-resistance. Computer peripherals, such as disk drives, are an example of single-supply (12-V or 5-V) systems that use analog switches for sampling, signal conditioning, signal routing, and level translation. High-speed data acquisition systems typically use ±5-V supplies for the flash converters, and they require very fast, accurate switches for the input sample-and-hold amplifiers.

Sample-and-Hold Amplifiers

Figure 7 shows a sample-and-hold amplifier that provides a very fast sample acquisition time with the ±5-V power supplies that are required for high-speed A/D converters. The circuit is controlled by the sample-and-hold input, which is a TTL (5-V CMOS) control line. When a logic "0" is applied to the sample-and-hold input, the switch is turned on. A sample of the input signal is acquired by charging up the hold capacitor (C_H) to the value of the input signal. When a logic "1" is applied, the switch is turned off. The value of the input signal at the time the switch is turned off is held in C_H. The sample-and-hold amplifier is designed for the following features:

Sample-and-Hold Amplifiers (Cont'd)

1. ±5-V Operation

   The DG601 and Si581 buffer are both rated for ±5-V operation.

2. Low Pedestal Error

   This is a result of the low charge injection of the DG601. Pedestal error can be reduced even further by using other switches in the quad to cancel out the injected charge (Figure 8).

3. Fast Acquisition Time

   Sample-and-hold amplifiers take advantage of the fast switching time of the DG601 with a (+5-V supply, t_{ON} is typically 50 ns) and the high slew rate (800 V/µs) of the Si581.

   The 20-µA bias current for the Si581 will result in a 20-mV/µs droop rate, which is adequate for 8-bit operation at a 1-MHz sampling rate. Better droop rate can be achieved with a lower input-bias current buffer, such as a FET input device.

4. TTL-Compatible Operation

Precision Signal Routing

The low on-resistance of the DG601 makes it an ideal choice for digitally controlled analog signal conditioning applications, such as channel selection and gain ranging in low-voltage systems. High-voltage switches (like the DG201A) suffer increased on-resistance and logic incompatibility when operated at lower supply voltages like +12 V. The 30-Ω on-resistance of the DG601 helps to maintain low impedance levels and reduce switch resistance-induced offsets and noise.

Level Translation Applications

The DG601 makes an excellent level translator for use with MOSPOWER drivers, relay drivers, JFET drivers, GaAs FET drivers, DMOS drivers, and other circuits that require high-speed 5-V logic compatibility and an output range up to 12 V. Figure 9 shows one-half of a DG601 acting as the interface between the TTL and the Si9950 half-bridge driver. The Si9950 has a 1000-pF input capacitance, which is difficult to drive from a standard logic gate. The DG601 delivers a fast level translation from a TTL signal to provide 12 V of enhancement on the Si9950. A 180-Ω resistor is placed in series with the Si9950 input to limit the current through the DG601 to 100 mA (worst case). This prevents the current from exceeding the absolute maximum current rating. Increased gate drive current can be handled by connecting two sets of switches in parallel.

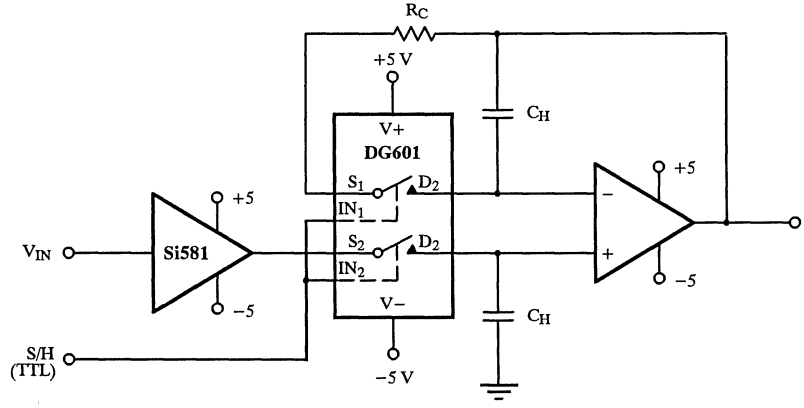


Figure 8 Using On-Board Switches to Cancel Out Charge Ingection

Conclusion

The DG601 has many applications in low-voltage systems, having been designed and specified for 12-V, TTL-compatible operation. It is also excellent in ±5-V and single 5-V supply applications where fast switching speed, low charge injection, and low on-resistance are required. This data sheet highlights some typical applications to assist the design engineer in getting optimum performance in low-voltage mixed analog/digital systems.

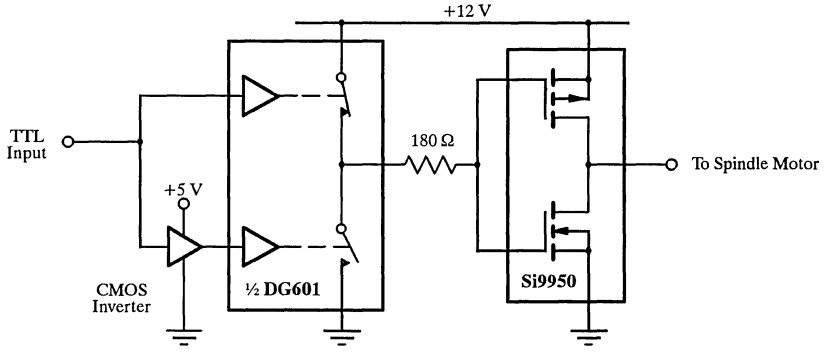


Figure 9 DG601 Provides Level Translation for MOSFET Gate Drive

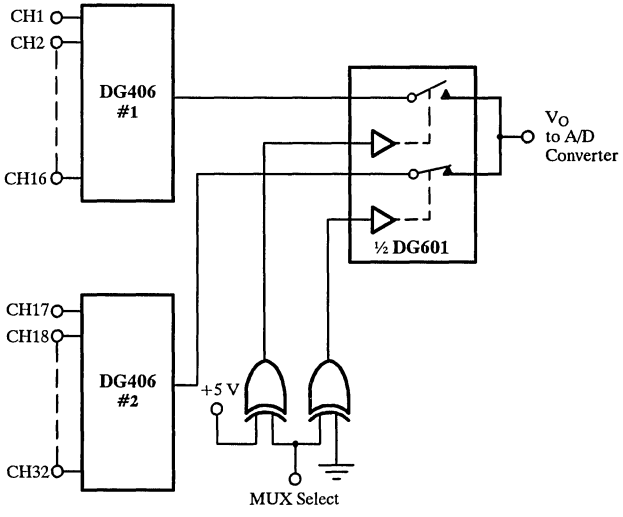


Figure 10 Super Multiplexing Improves Settling Times

Siliconix
A Member of the TEMIC Group

High-Speed, Low-Glitch D/CMOS Analog Switches

Features

- Fast Switching— t_{ON}: 12 ns
- Low Charge Injection: ±2 pC
- Wide Bandwidth: 500 MHz
- 5-V CMOS Logic Compatible
- Low $r_{DS(on)}$: 18 Ω
- Low Quiescent Power : 1.2 nW
- Single Supply Operation

Benefits

- Improved Data Throughput
- Minimal Switching Transients
- Improved System Performance
- Easily Interfaced
- Low Insertion Loss
- Minimal Power Consumption

Applications

- Fast Sample-and-Holds
- Synchronous Demodulators
- Pixel-Rate Video Switching
- Disk/Tape Drives
- DAC Deglitching
- Switched Capacitor Filters
- GaAs FET Drivers
- Satellite Receivers

Description

The DG611/612/613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

Each switch conducts equally well in both directions when on and blocks up to 16 V_{p-p} when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611/612/613 are built on the Siliconix proprietary D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

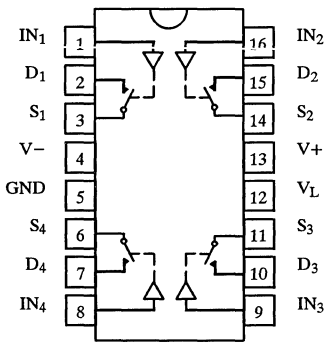
The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

For additional information see Applications Note AN207.

Functional Block Diagram and Pin Configuration

DG611

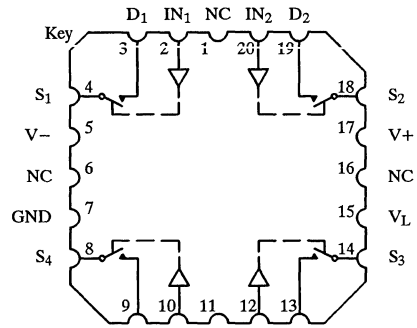
Dual-In-Line and SOIC



Top View

DG611

LCC



Top View

Ordering Information – DG611/612

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG611DJ
		DG612DJ
	16-Pin Narrow SOIC	DG611DY
		DG612DY
−55 to 125°C	16-Pin CerDIP	DG611AK/883
		DG612AK/883
	LCC-20	DG611AZ/883
		DG612AZ/883

Four SPST Switches per Package

Truth Table

Logic	DG611	DG612
0	ON	OFF
1	OFF	ON

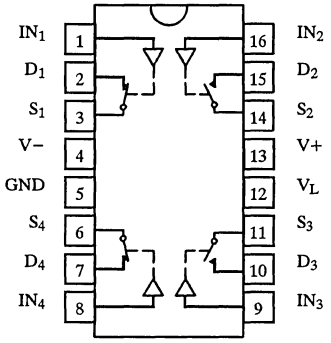
Logic "0" ≤ 1 V
Logic "1" ≥ 4 V

Switches Shown for DG611 Logic "1" Input

Functional Block Diagram and Pin Configuration (Cont'd)

DG613

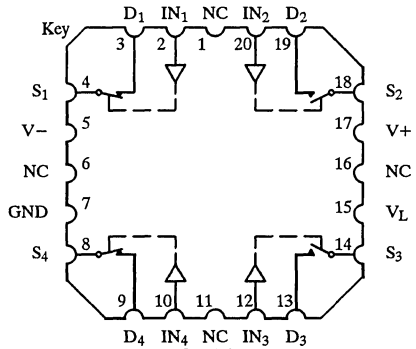
Dual-In-Line and SOIC



Top View

DG613

LCC



Top View

Ordering Information – DG613

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG613DJ
	16-Pin Narrow SOIC	DG613DY
−55 to 125°C	16-Pin CerDIP	DG613AK/883
	LCC-20	DG613AZ/883

Four SPST Switches per Package

Truth Table

Logic	SW_1, SW_4	SW_2, SW_3
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 1 V
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

Absolute Maximum Ratings

V+ to V− ..... −0.3 V to 21 V
V+ to GND ..... −0.3 V to 21 V
V− to GND ..... −19 V to 0.3 V
V_L to GND ..... −1 V to (V+) + 1 V
or 20 mA, whichever occurs first
V_{IN}[a] ..... (V−) −1 V to (V+) + 1 V
or 20 mA, whichever occurs first
V_S, V_D[a] ..... (V−) −0.3 V to (V−) + 16 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... ±30 mA
Current, S or D (Pulsed at 1 µs, 10% Duty Cycle) ..... ±100 mA
Storage Temperature: CerDIP ..... −65 to 150°C
Plastic ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 600 mW
16-Pin CerDIP[e] ..... 900 mW
20-Pin LCC[e] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

CAUTION: ESD (electrostatic discharge) sensitive. All pins are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Use proper ESD control procedures.

Recommended Operating Range

V+ ..... 5 V to 21 V
V− ..... −10 V to 0 V
V_L ..... 4 V to V+

V_{IN} ..... 0 V to V_L
V_{ANALOG} ..... V− to (V+) − 5 V

Specifications[a]

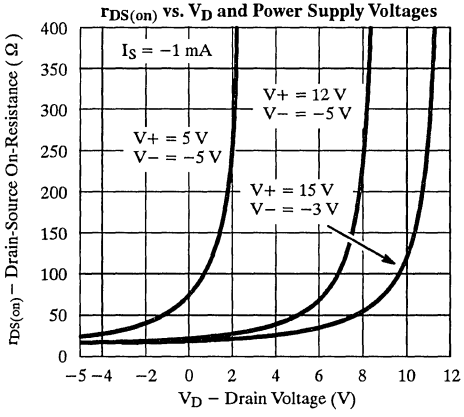
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_L = 5 V, V_{IN} = 4 V, 1 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}	V− = −5 V, V+ = 12 V	Full		−5	7	−5	7	V
Switch On-Resistance	$r_{DS(on)}$	I_S = −1 mA, V_D = 0 V	Room Full	18		45 60		45 60	Ω
Resistance Match Bet Ch.	$\Delta r_{DS(on)}$		Room	2					
Source Off Leakage	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Hot	±0.001	−0.25 −20	0.25 20	−0.25 −20	0.25 20	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V	Room Hot	±0.001	−0.25 −20	0.25 20	−0.25 −20	0.25 20	
Switch On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Hot	±0.001	−0.4 −40	0.4 40	−0.4 −40	0.4 40	
Digital Control									
Input Voltage High	V_{IH}		Full		4		4		V
Input Voltage Low	V_{IL}		Full			1		1	
Input Current	I_{IN}		Room Hot	0.005	−1 −20	1 20	−1 −20	1 20	µA
Input Capacitance	C_{IN}		Room	5					pF
Dynamic Characteristics									
Off State Input Capacitance	$C_{S(off)}$	V_S = 0 V	Room	3					pF
Off State Output Capacitance	$C_{D(off)}$	V_D = 0 V	Room	2					
On State Input Capacitance	$C_{S(on)}$	V_S = V_D = 0 V	Room	10					
Bandwidth	BW	R_L = 50 Ω	Room	500					MHz
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 3 pF, V_S = ±2 V See Test Circuit, Figure 2	Room	12		25		25	ns
Turn-Off Time[e]	t_{OFF}		Room	8		20		20	
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 75 pF, V_S = ±2 V See Test Circuit, Figure 2	Room Full	19		35 50		35 50	
Turn-Off Time	t_{OFF}		Room Full	16		25 35		25 35	
Charge Injection[e]	Q	C_L = 1 nF, V_S= 0 V	Room	4					pC
Ch. Injection Change[e, g]	ΔQ	C_L = 1 nF, | V_S | ≤ 3 V	Room	3		4		4	
Off Isolation[e]	OIRR	R_{IN} = 50 Ω, R_L = 50 Ω, f = 5 MHz	Room	74					dB
Crosstalk[e]	X_{TALK}	R_{IN} = 10 Ω, R_L = 50 Ω, f = 5 MHz	Room	87					
Power Supplies									
Positive Supply Curent	I+	V_{IN} = 0 V or 5 V	Room Full	0.005		1 5		1 5	µA
Negative Supply Current	I−		Room Full	−0.005	−1 −5		−1 −5		
Logic Supply Current	I_L		Room Full	0.005		1 5		1 5	
Ground Current	I_{GND}		Room Full	−0.005	−1 −5		−1 −5		

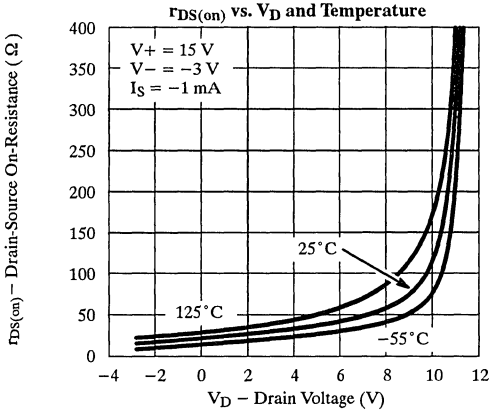
Specifications[a] for Unipolar Supplies

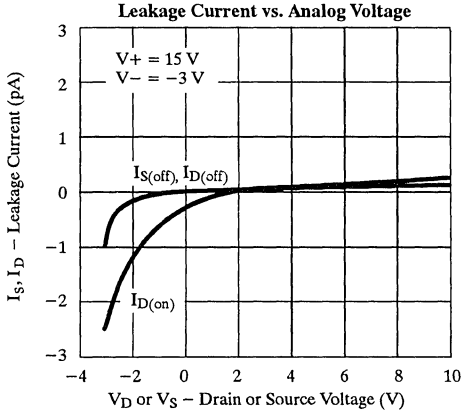
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_L = 5 V, V_{IN} = 4 V, 1 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	7	0	7	V
Switch On-Resistance	$r_{DS(on)}$	I_S = −1 mA, V_D = 1 V	Room	25		60		60	Ω
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 3 pF, V_S = 2 V See Test Circuit, Figure 2	Room	15		30		30	ns
Turn-Off Time[e]	t_{OFF}		Room	10		25		25	

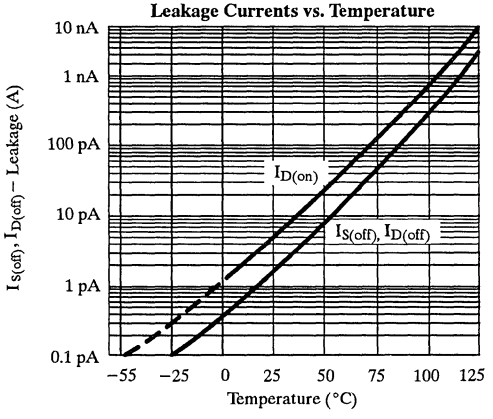
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta Q = |Q \text{ at } V_S = 3\text{ V} - Q \text{ at } V_S = -3\text{ V}|$.

Typical Characteristics





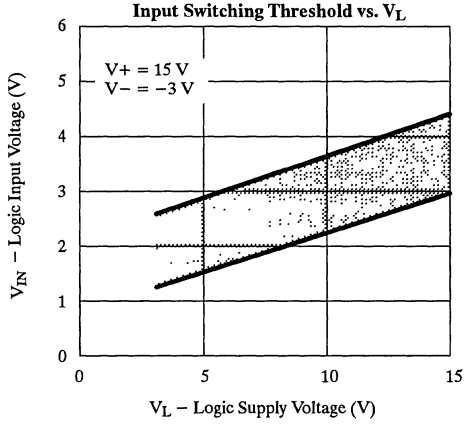




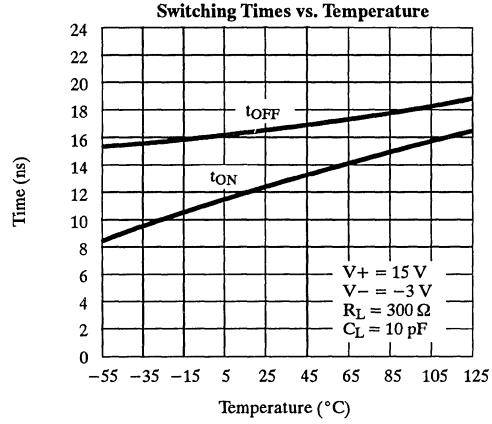
1

Typical Characteristics (Cont'd)

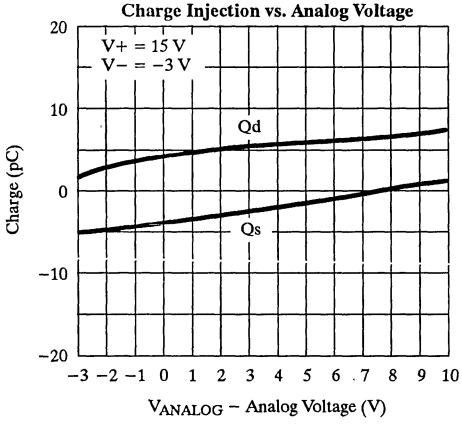
Input Switching Threshold vs. V_L



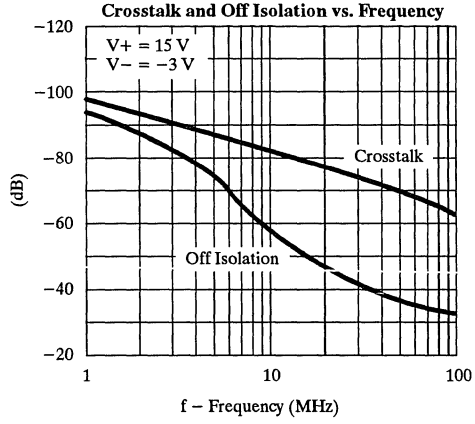
Switching Times vs. Temperature



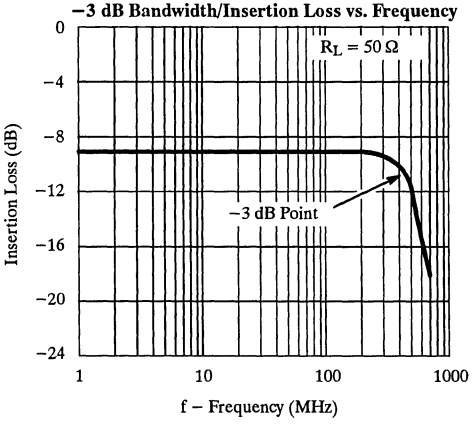
Charge Injection vs. Analog Voltage



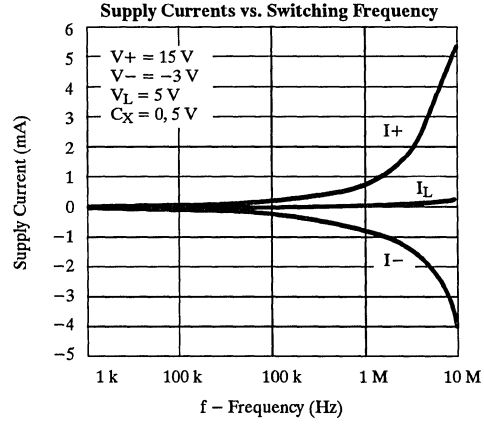
Crosstalk and Off Isolation vs. Frequency



−3 dB Bandwidth/Insertion Loss vs. Frequency



Supply Currents vs. Switching Frequency



Schematic Diagram (Typical Channel)

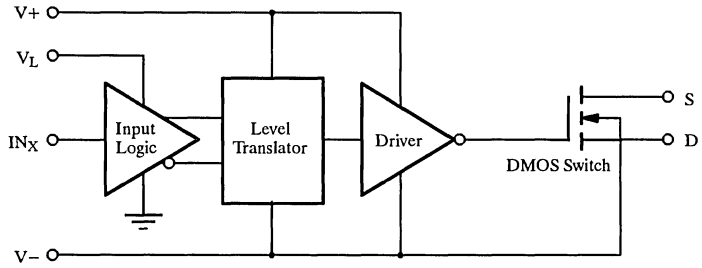
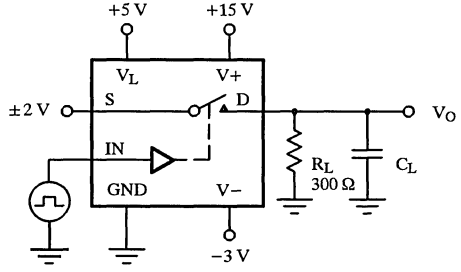


Figure 1.

Test Circuits



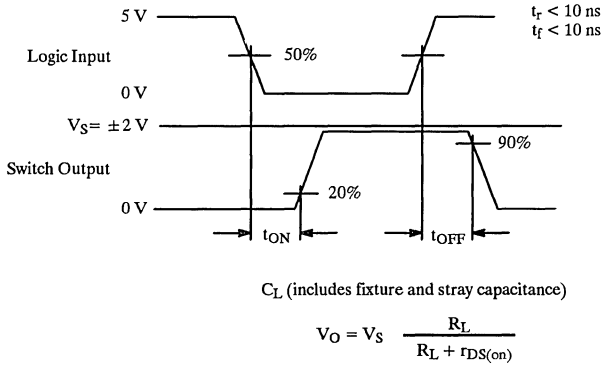


Figure 2. Switching Time

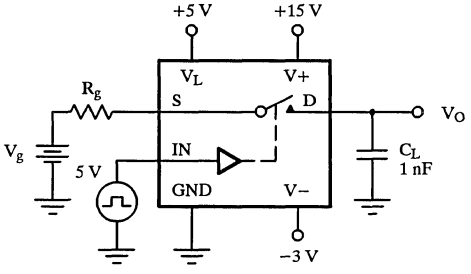


Figure 3. Charge Injection

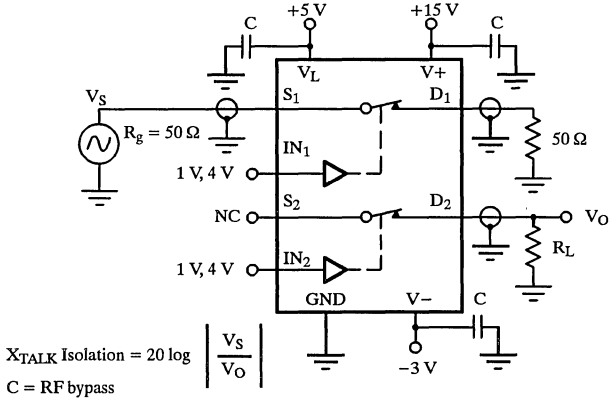


Figure 4. Crosstalk

Applications

High-Speed Sample-and-Hold

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The Si581, a fast input buffer, helps to shorten acquisition and settling times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (See Figure 5.)

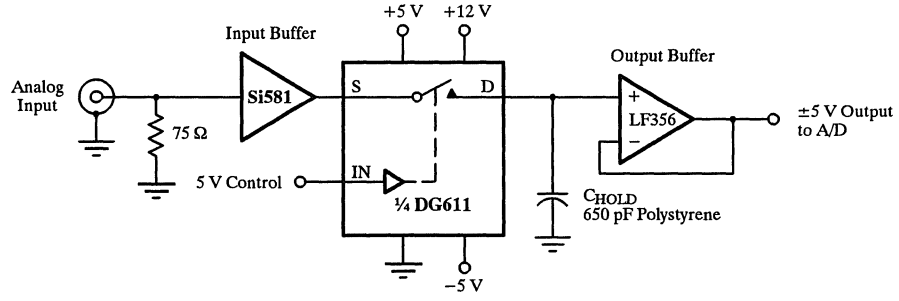


Figure 5. High-Speed Sample-and-Hold

Pixel-Rate Switch

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video sources must be sync locked. The glitch-less analog switch eliminates halos. (See Figure 6.)

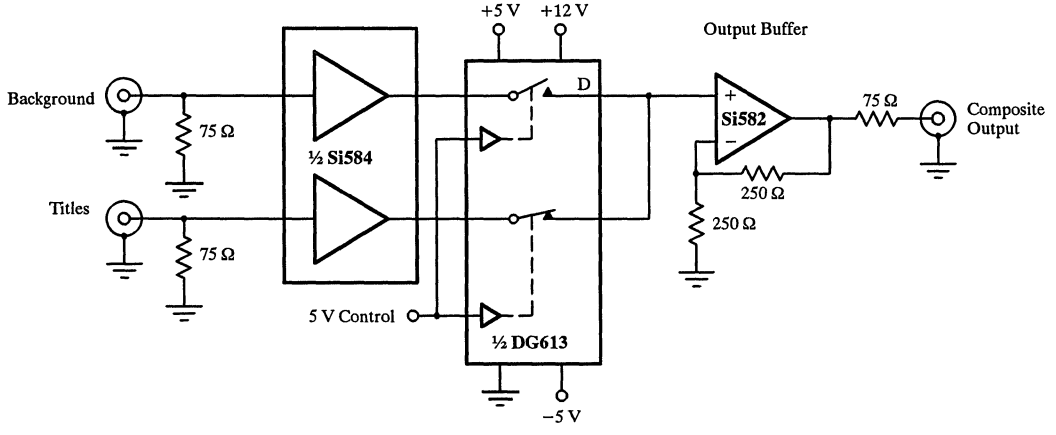


Figure 6. A Pixel-Rate Switch Creates Title Overlays

Applications (Cont'd)

GaAs FET Drivers

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S_1, whereas to turn it off, −8 V are applied via S_2. This high-speed, low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.

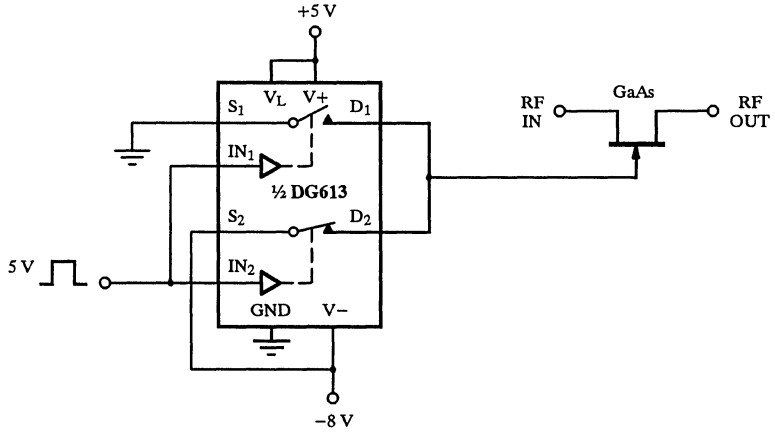


Figure 7. A High-Speed GaAs FET Driver that Saves Power

Siliconix
A Member of the TEMIC Group

Low On-Resistance Wideband/Video Switches

Features

- Wide Bandwidth: 500 MHz
- Low Crosstalk at 5 MHz: −85 dB
- Low $r_{DS(on)}$: 5 Ω, DG642
- TTL Logic Compatible
- Fast Switching: t_{ON} 50 ns
- Single Supply Compatibility
- High Current: 100 mA, DG642

Benefits

- High Precision
- Improved Frequency Response
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Low Power Consumption

Applications

- RF and Video Switching
- RGB Switching
- Video Routing
- Cellular Communications
- ATE
- Radar/FLIR Systems
- Satellite Receivers
- Programmable Filters

Description

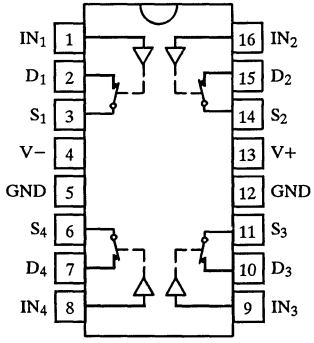
The DG641/642/643 are high performance monolithic video switches designed for switching wide bandwidth analog and digital signals. DG641 is a quad SPST, DG642 is a single SPDT, and DG643 is a dual SPDT function. These devices have exceptionally low on-resistances (5 Ω typ—DG642), low capacitance and high current handling capability.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG641/642/643 are built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on, and blocks up to 14 V_{p-p} when off. An epitaxial layer prevents latchup.

Functional Block Diagram and Pin Configuration

DG641

Dual-In-Line and SOIC



Top View

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

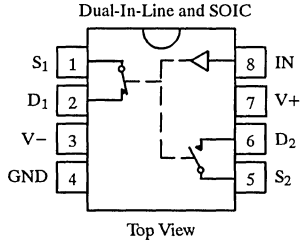
Switches Shown for Logic "1" Input

Ordering Information – DG641

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG641DJ
	16-Pin Narrow SOIC	DG641DY

Functional Block Diagram and Pin Configuration

DG642



Truth Table

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

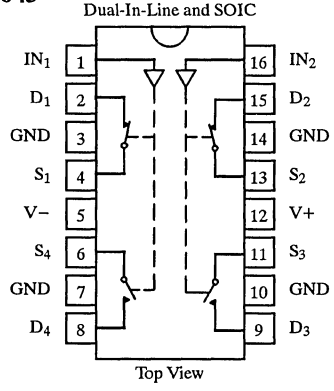
Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

Ordering Information – DG642

Temp Range	Package	Part Number
−40 to 85°C	8-Pin Plastic DIP	DG642DJ
	8-Pin Narrow SOIC	DG642DY

DG643



Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

Ordering Information – DG643

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG643DJ
	16-Pin Narrow SOIC	DG643DY

1

Absolute Maximum Ratings

V+ to V− ..... −0.3 V to 21 V
V+ to GND ..... −0.3 V to 21 V
V− to GND ..... −19 V to +0.3 V
Digital Inputs ..... (V−) −0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V−) −0.3 V to (V−) +14 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal Except S or D) ..... 20 mA
Continuous Current S or D: DG641/643 ..... 75 mA
DG642 ..... 100 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max)
DG641/643 ..... 200 mA
DG642 ..... 300 mA

Storage Temperature ..... −65 to 125°C
Power Dissipation (Package)[b]
8-Pin Plastic DIP and Narrow SOIC[c] ..... 300 mW
16-Pin Plastic DIP[d] ..... 470 mW
16-Pin Narrow SOIC[e] ..... 600 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7.6 mW/°C above 75°C
d. Derate 6 mW/°C above 75°C
e. Derate 10 mW/°C above 75°C

Specifications for DG641 and DG643

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_{INH} = 2.4 V, V_{INL} = 0.8 V[e]	Temp[a]	Limits −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V− = −5 V, V+ = 12 V	Full	−5		8	V
		V− = GND, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 0 V	Room		8	15	Ω
			Full			20	
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		1	2	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room	−10	−0.02	10	nA
			Full	−100		100	
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0V	Room	−10	−0.02	10	
			Full	−100		100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room	−10	−0.1	10	
			Full	−100		100	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room	−1	0.05	1	µA
			Full	−20		20	
Dynamic Characteristics							
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		10	20	pF
Off State Input Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		4	12	
Off State Output Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		4	12	
Bandwidth	BW	R_L = 50 Ω, See Figure 6	Room		500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, See Figure 2	Room		50	70	ns
			Full			140	
Turn Off Time	t_{OFF}		Room		28	50	
			Full			85	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V, See Figure 3	Room		−19		pC
Off Isolation	OIRR	R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz See Figure 4	Room		−60		dB
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω, f = 5 MHz See Figure 5	Room		−87		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or V_{IN} = 5 V	Room		3.5	6	mA
			Full			9	
Negative Supply Current	I−		Room	−6	−3		
			Full	−9			

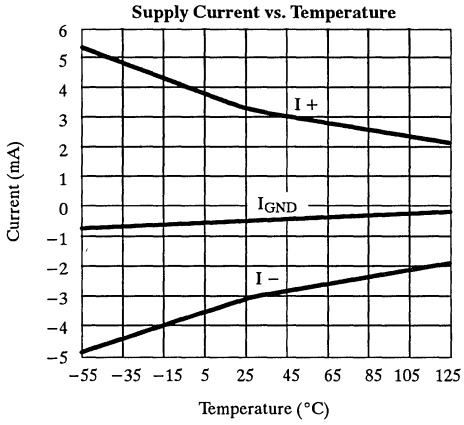
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

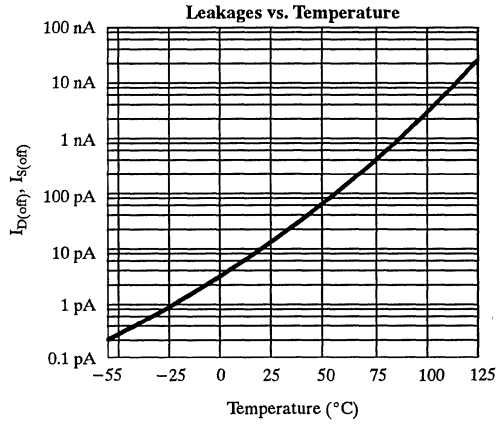
Specifications for DG642

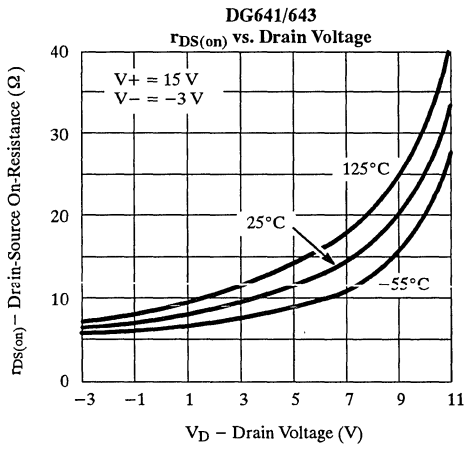
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_{INH} = 2.4 V, V_{INL} = 0.8 V[e]	Temp[a]	Limits −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V− = −5 V, V+ = 12 V	Full	−5		8	V
		V− = GND, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 0 V	Room Full		5	8 9	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		0.5	1	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Full	−10 −200	−0.04	10 200	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0V	Room Full	−10 −200	−0.04	10 200	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Full	−10 −200	−0.2	10 200	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room Full	−1 −20	0.05	1 20	µA
Dynamic Characteristics							
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		19	40	pF
Off State Input Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		8	20	
Off State Output Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		8	20	
Bandwidth	BW	R_L = 50 Ω, See Figure 6	Room		500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, See Figure 2	Room Full		60	100 160	ns
Turn Off Time	t_{OFF}		Room Full		40	60 100	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V, See Figure 3	Room		−40		pC
Off Isolation		R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz See Figure 4	Room		−63		dB
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω, f = 5 MHz See Figure 5	Room		−85		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or V_{IN} = 5 V	Room Full		3.5	6 9	mA
Negative Supply Current	I−		Room Full	−6 −9	−3		

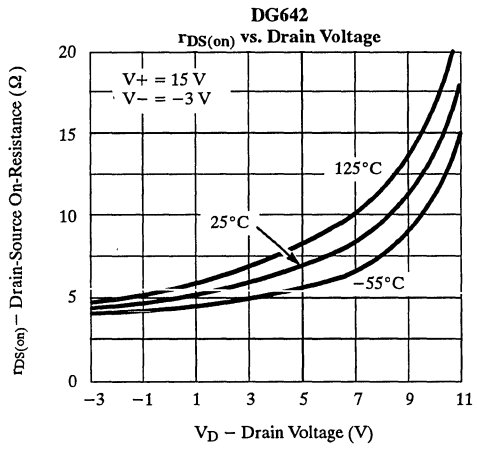
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

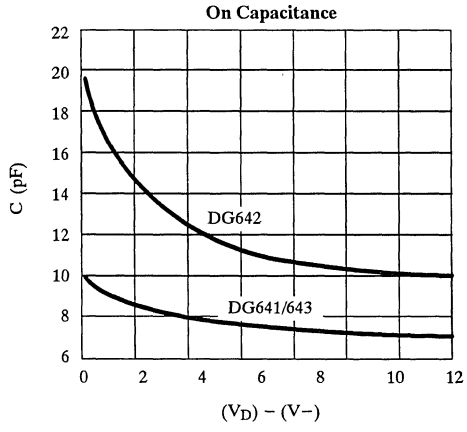
Typical Characteristics

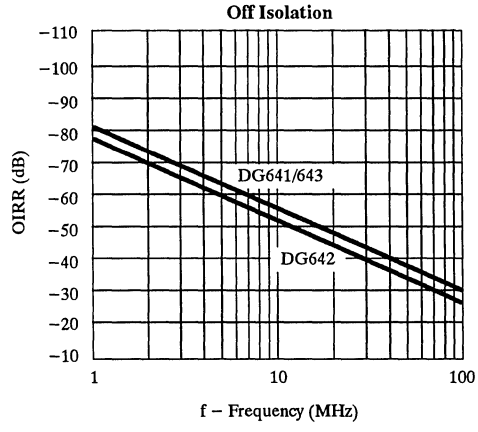




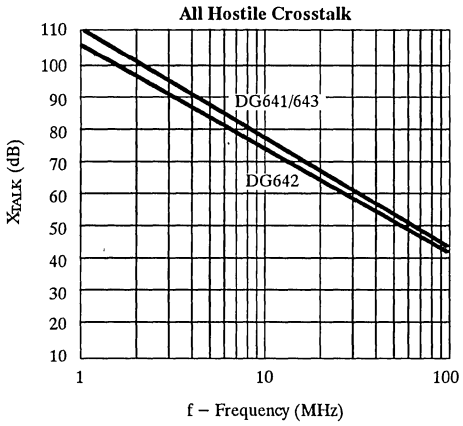


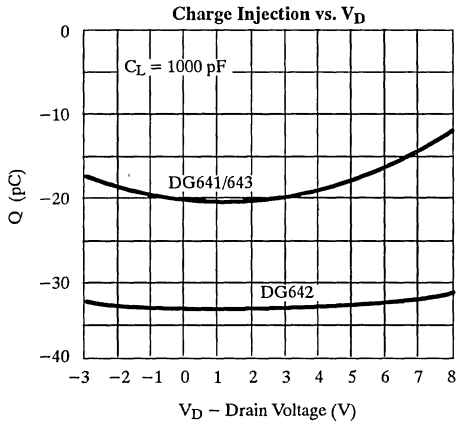


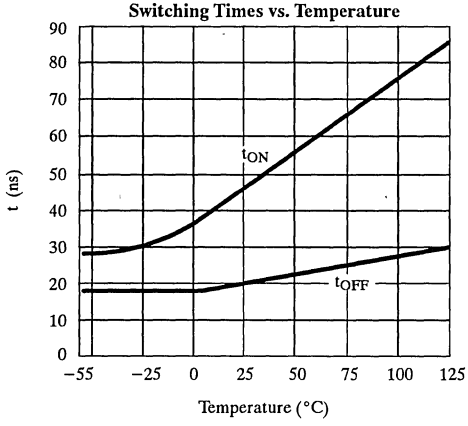


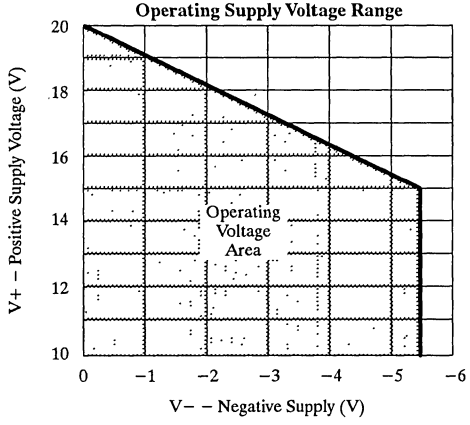


Typical Characteristics









Schematic Diagram (Typical Channel)

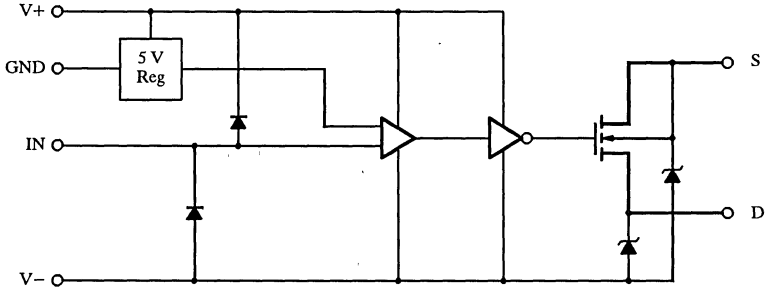


Figure 1.

Test Circuits

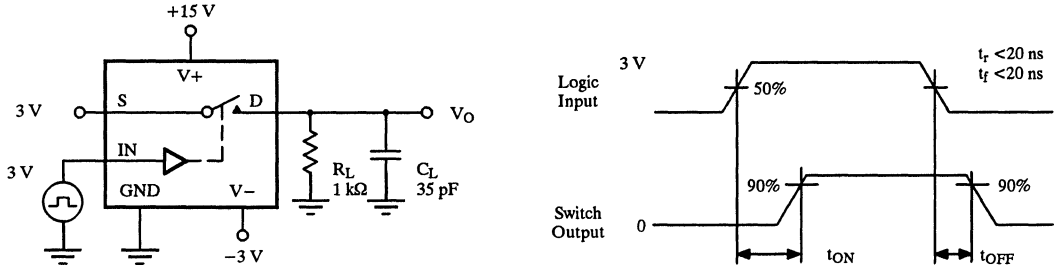


Figure 2. Switching Time

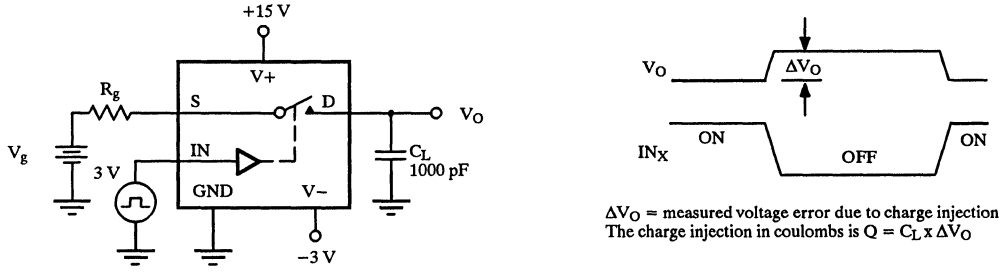


Figure 3. Charge Injection

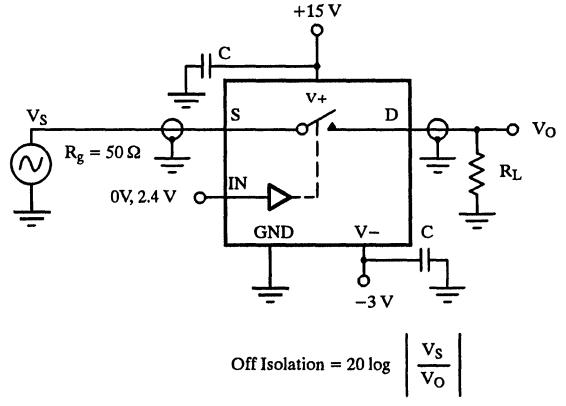


Figure 4. Off Isolation

Test Circuits

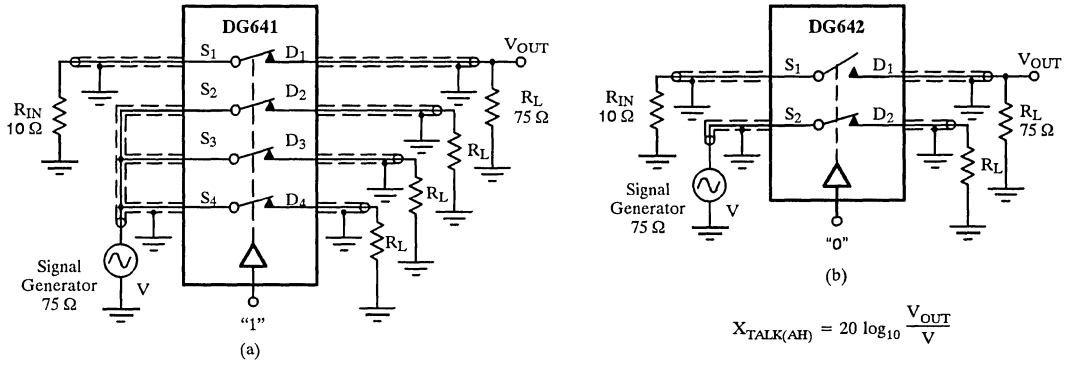


Figure 5. All Hostile Crosstalk – $X_{TALK(AH)}$

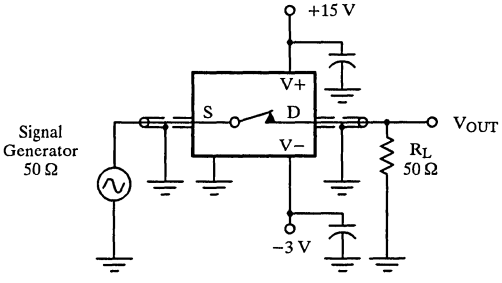


Figure 6. Bandwidth

Applications

Device Description

The DG641/642/643 switches offer true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these switches provide excellent off-isolation with a bandwidth of around 500 MHz. The silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range shown, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance [$r_{DS(on)}$] and capacitance [$C_{S(on)}$]. This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The –3 dB bandwidth of the DG641/642/643 is typically 500 MHz (into 50 Ω).

Applications (Cont'd)

Power Supplies

Power supply flexibility is a useful feature of the DG641/642/643 series. It can be operated from a single positive supply (V+) if required (V− connected to ground).

Note that the analog signal must not exceed V− by more than −0.3 V to prevent forward biasing the substrate p-n junction. The use of a V− supply has a number of advantages:

1. It allows flexibility in analog signal handling, i.e., with V− = −5 V and V+ = 12 V; up to ±5-V ac signals can be controlled.
2. The value of on capacitance [$C_{S(on)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(on)}$ for an increasing V body-source. Note however that to increase V− normally requires V+ to be reduced (since V+ to V− = 21 V max.). A reduction in V+ causes an increase in $r_{DS(on)}$, hence a compromise has to be achieved. It is also useful to note that tests indicate that optimum video linearity performance (e.g., differential phase and gain) occurs when V− is around −3 V.
3. V− eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG641/642/643 series is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential. Suitable decoupling capacitors are 1- to 10-µF tantalum bead, plus 10- to 100-nF ceramic or polyester.

Rules:

1. Decoupling capacitors should be incorporated on all power supply pins (V+, V−). (See Figure 7).
2. They should be mounted as close as possible to the device pins.
3. Capacitors should be of a suitable type with good high frequency characteristics – tantalum bead and/or ceramic disc types are adequate.

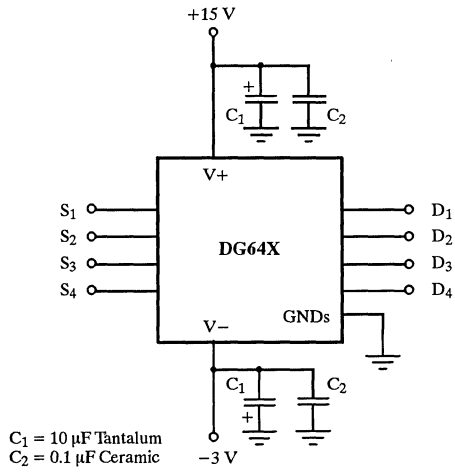


Figure 7. Supply Decoupling

Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by these analog switches. Some tips for minimizing stray effects are:

1. Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.
2. Keep signal paths as short as practically possible, with all channel paths of near equal length.
3. Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current, flowing through ground path parasitic resistance, from coupling between channels.

Figure 8 shows a 4-channel video multiplexer using a DG641.

In Figure 9, two coax cables terminated on 75 Ω bring two video signals to the DG642 switch. The two drains tied together lower the on-state capacitance. An Si582 video amplifier drives a double terminated 75-Ω cable. The double terminated coax cable eliminates line reflections.

Applications (Cont'd)

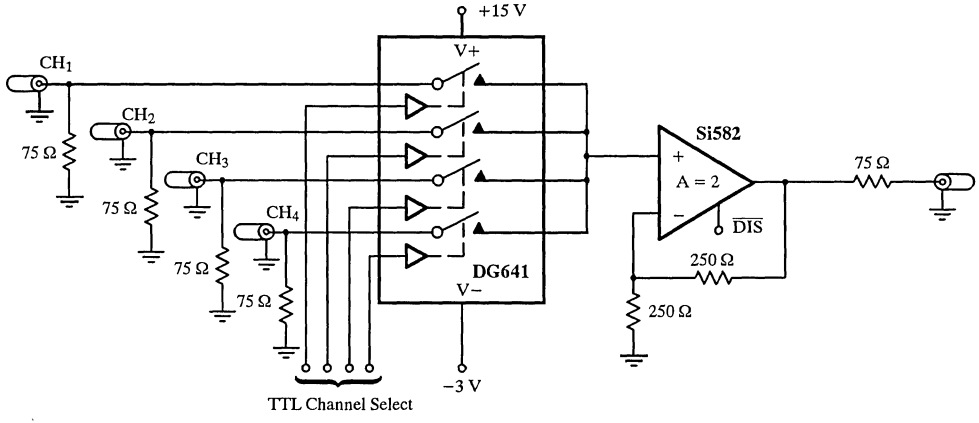


Figure 8. 4 by 1 Video Multiplexing Using the DG641

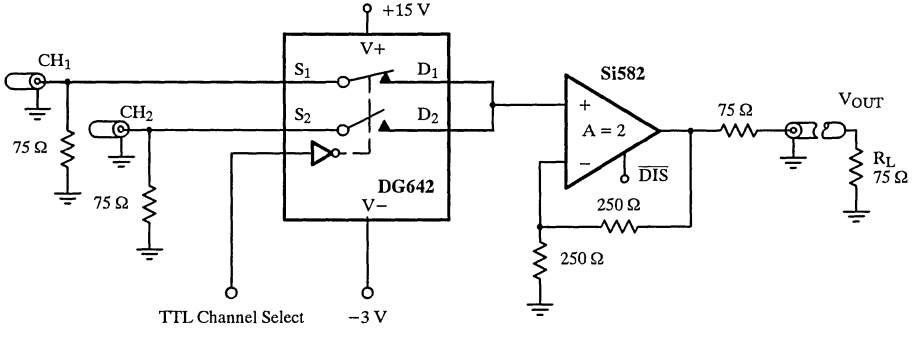


Figure 9. 2-Channel Video Selector Using the DG642

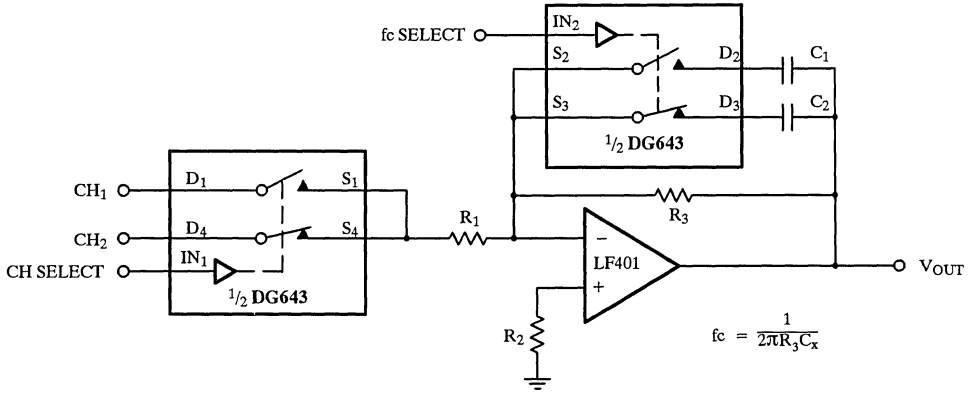


Figure 10. Active Low Pass Filter with Selectable Inputs and Break Frequencies

Siliconix
A Member of the TEMIC Group

Monolithic General Purpose CMOS Analog Switch

Features

- ± 15-V Input Range
- On-Resistance: <50 Ω
- Break-Before-Make Switching
- TTL and CMOS Compatible

Benefits

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

Applications

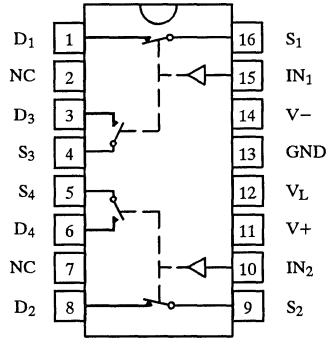
- Audio Switching
- Instrumentation
- Battery Powered Systems

Description

The DG5043 solid state analog switch is recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS-40 high voltage CMOS process, this device provides ease-of-use and performance advantages to the system designer. Key performance features of the DG5043 are 1-µs switching, low power supply requirements, and break-before-make switching. Each switch conducts equally well in either direction, when on, and blocks up to 30 V peak-to-peak when off. Off leakage current is 1-nA maximum. An epitaxial layer prevents latch up. For new designs, DG403 is recommended.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" = ≤ 0.8 V
Logic "1" = ≥ 2 V
Switches shown for Logic "1" input.

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5043CJ

Absolute Maximum Ratings

V+ to V− ..... 44 V
GND to V− ..... 25 V
V_L ..... (GND − 0.3 V) to 44 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA
Storage Temperature ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C

P-32167—Rev. A (11/15/93)

Not Recommended for New Designs

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2 V, 0.8 V[e]	Temp[a]	C Suffix 0 to 70°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	−15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = ±10 V	Room Full			50 75	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_S = V_D = 14 V	Room Full	−1 −100		1 100	nA
		V_S = V_D = −14 V	Room Full	−1 −100		1 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room Full			2 200	
		V_S = V_D = −14 V	Room Full	−2 −200			
Digital Control							
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V	Full	−1		1	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2 V	Full	−1		1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = ±10 V, R_L = 1 kΩ, C_L = 35 pF See Figure 1	Room			1200	ns
Turn-Off Time	t_{OFF}		Room			700	
Charge Injection[d]	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		30		pC
Off Isolation[d]	OIRR	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz	Room		75		dB
Crosstalk (Channel-to-Channel)[d]	X_{TALK}	R_L = 75 Ω, V_S = 2 V_{P-P}, f = 1 MHz	Room		89		
Source Off Capacitance	$C_{S(off)}$	V_D = V_S = 0 V, f = 1 MHz	Room		15		pF
Drain Off Capacitance[d]	$C_{D(off)}$		Room		17		
Channel On Capacitance[d]	$C_{D(on)}$		Room		45		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 or 2.4 V	Full			300	µA
Negative Supply Current	I−		Full	−300			
Logic Supply Current	I_L	V_{IN} = 0 or 2.4 V	Full			300	
Ground Current	I_{GND}		Full	−300			

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

Test Circuits

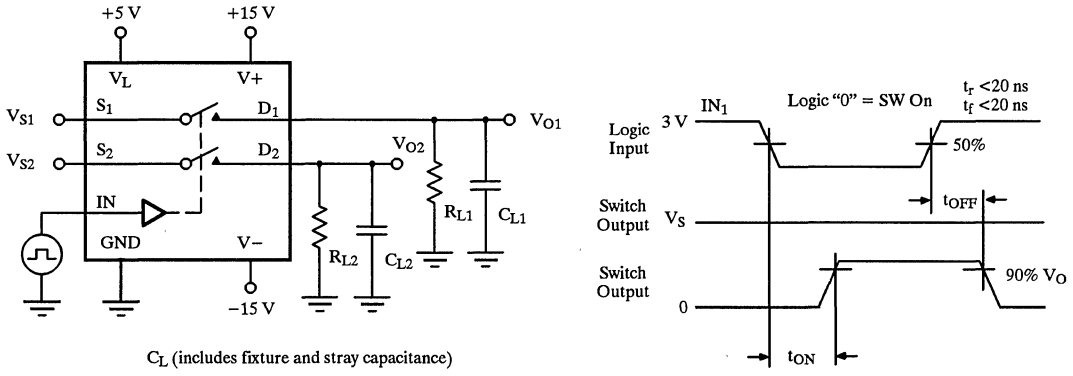


Figure 1. Switching Time

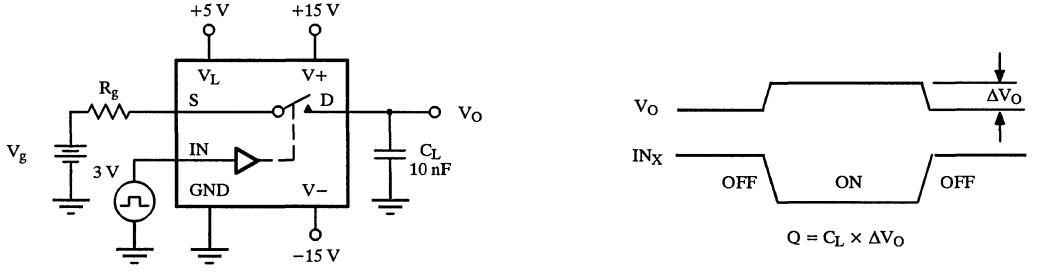


Figure 2. Charge Injection

DG5143

Low-Power, High-Speed CMOS Analog Switch

Features

- ± 15-V Input Range
- On-Resistance: 50 Ω
- Fast Switching Action—t_{ON}: 100 ns
- Low Power—P_D: <350 µW
- TTL and CMOS Compatible

Benefits

- Improved Signal Headroom
- Low Signal Errors
- Break-Before-Make Switching Action
- Reduced Power Consumption
- Simple Interfacing

Applications

- Audio Switching
- Precision Switching
- High-Speed Switching
- Battery Powered Systems

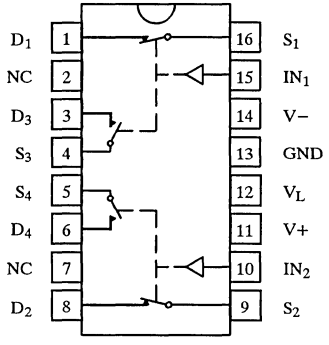
Description

The DG5143 solid state analog switch is built on the Siliconix proprietary high-voltage silicon gate process to achieve high voltage rating and superior switch time on/off performance. Break-before-make switching action guarantees that an on-channel will be turned off before the off-channel can turn on. The DG5143 features ultra-low power supply requirements and TTL and CMOS compatibility.

Each switch conducts equally well in both directions when on and blocks input voltages to the supply values when off. This switch is ideal for battery powered industrial applications with a maximum power supply current of 1 µA. An expitaxial layer prevents latchup.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5143CJ

1

Absolute Maximum Ratings

(V+) – (V–) ..... < 36 V
(V+) – (V_D)[a] ..... < 30 V
(V_D) – (V–)[a] ..... < 30 V
(V_D) – (V_S)[a] ..... < ±22 V
(V_L) – (V–) ..... < 33 V
(V_L) – (V_{IN}) ..... < 30 V
V_L ..... < 20 V
V_{IN}[a] ..... < 20 V

Continuous Current, Any Terminal ..... 30 mA
Peak Current, S or D (pulsed a 1 ms, 10% duty cycle max) . 100 mA
Storage Temperature ..... –65 to 125°
Power Dissipation (Package)[b]
16-Pin Plastic DIP ..... 450 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V, V_L = 5 V V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	C Suffix 0 to 70°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = – 10 mA	Room Full			75 100	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = ∓10 V, V_S = ±10 V	Room Full	–5 –20		5 20	nA
	$I_{D(off)}$		Room Full	–5 –20		5 20	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = –10 to 10 V	Room Full	–2 –40		2 40	
Digital Control							
Input Current with V_{IN} Low	I_{IL}		Full	–1		1	µA
Input Current with V_{IN} High	I_{IH}		Full	–1		1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 1	Room			175	ns
Turn-Off Time	t_{OFF}		Room			150	
Break-Before-Make	$t_{ON} - t_{OFF}$		Room			5	
Charge Injection[d]	Q	C_L = 10,000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room			150	pC
Off Isolation[d]	OIRR	R_L = 100 Ω, C_L ≤ 5 pF, f = 1 MHz	Room	–50			dB
Channel-to-Channel Crosstalk[d]	X_{TALK}	Any Other Channel Switches R_L = 100 Ω, C_L ≤ 5 pF, f = 1 MHz	Room			–50	
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or 5 V Switch Duty Cycle <10%	Room			10	µA
Negative Supply Current	I–		Room	–10			
Logic Supply Current	I_L		Room			10	
Ground Current	I_{GND}		Room	–10			

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
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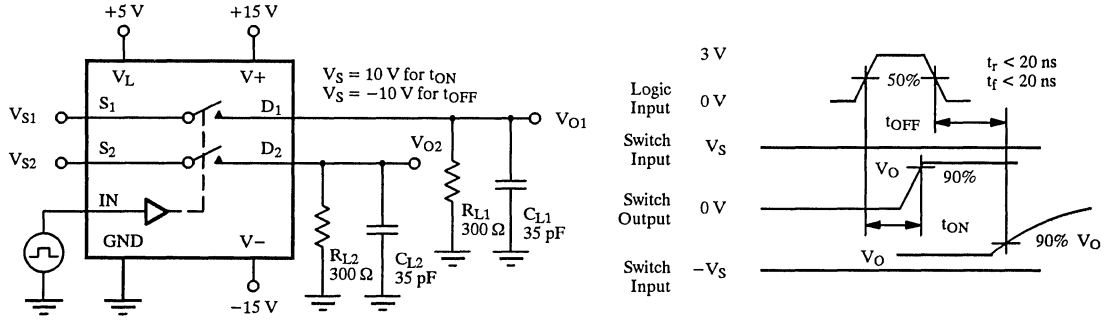
e. V_{IN} = input voltage to perform proper function.

Test Circuits



C_L (includes fixture and stray capacitance)

Figure 1. Switching Time

About Analog Multiplexers

Analog multiplexers represent a higher level of integration than analog switches. They have many (4, 8, 16, or more) inputs with only one or two common outputs. Multiplexers are used where it is necessary to transfer information from many input channels to a common output, most often when only one transmission line is available for all data transfer between various points. The transmitted signals are in either analog or digital form. Siliconix multiplexers handle analog signals, passing bipolar voltages or currents, which are often obtained from transducers. The analog signals represent physical phenomena such as temperature, pressure, velocity, and flow speech. Typical applications include data acquisition, industrial process control, aircraft systems monitoring, medical electronics, telemetry, and telecommunications.

Differential vs. Single-Ended Multiplexing

When is it better to select a differential multiplexer versus a single-ended configuration? Figures 1 and 2 demonstrate both options. Single-ended multiplexing, as shown in Figure 1, applies to systems that have signal sources which are close to full-scale range and referenced to a common point (usually ground). Another case is where different signal sources with small signal amplitude (mV range) are generated by transducers. Instrumentation amplifiers can be used to precondition the signals and provide a common reference. This step reduces feedthrough errors and losses while tailoring each signal source to a desired voltage (or current) to obtain the maximum resolution available in an A/D or D/A converter or other device driven by the multiplexers.

Differential multiplexing (Figure 2) is utilized for low-level switching and in noisy environments. It can tolerate switching transients or some mismatch without a significant degradation of signal accuracy. Major considerations are switch matching ($r_{DS(on)}$, $I_{(off)}$, and capacitance), common-mode rejection, and the system's tolerance to switching transients introduced by the break-before-make switching sequence.

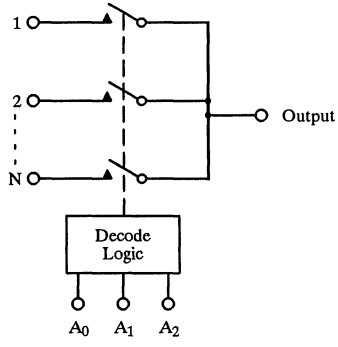


Figure 1. Single-Ended Multiplexing

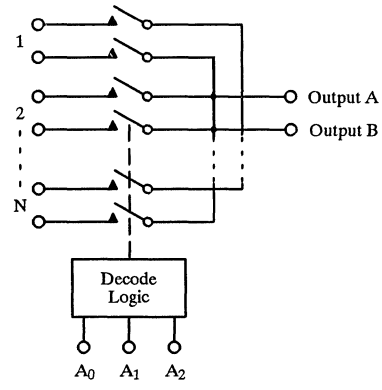


Figure 2. Differential Multiplexing

The DG4XX series of Siliconix multiplexers is designed to reduce switching errors, glitching, and power consumption while providing improved data throughput and increased ruggedness. For data acquisition, hi-rel, and battery operated systems, the rugged DG406/407 and DG408/409 multiplexers are the answer for designs requiring low on-resistance, low charge injection, fast transition time, and single-supply capability.

Other DG4XX family members include the DG428 and DG429, which have on-chip address and control latches to simplify design in microprocessor-based applications, as well as the DG485 octal analog switch array for low-power multiplexing in serial control applications.

D/CMOS Wideband/Video Multiplexers

The DG535 and DG536 are 16-channel wideband/video multiplexers which use the Siliconix D/CMOS process to combine wideband DMOS "T" switches with high-density, high-speed CMOS logic and switch drivers to form monolithic wideband/video multiplexing systems. These devices include on-board latches to hold the address selection data and all of the necessary control logic to facilitate connection into larger arrays, matrices, and multiplexers. The DG534 and DG538 are 4- and 8- channel wideband/video multiplexers which, like the DG535 and DG536, feature address latches and control logic with the addition of data feedback and TTL compatibility. They make excellent wideband/video crosspoints, routers, and multiplexers, reducing board space, power dissipation, component count, and cost, while simplifying system design and improving reliability.

For detailed information on these products, please refer to the individual data sheets and to application notes AN501 and AN502.

Crosspoints

The DG884 is the first monolithic wideband/video crosspoint switch available for commercial use. Any of eight video inputs can simultaneously be routed to any of our outputs. This highly integrated device offers a major reduction of the physical size and component count needed to implement a video switching matrix. The DG884 uses double-diffused DMOS switching elements to maintain low capacitance and low levels of crosstalk among signal paths.

Double-diffused CMOS latches, chip select, reset, readback, and disable functions are all included on the chip to ease system design, save power, and improve system reliability.

Factors Affecting Systems Performance

In any multiplexer application, the following factors should be considered:

1. ***System Attenuation***: Includes loss in the analog signal caused by the multiplexer and the transmission path. This is a frequency dependent factor.

2. ***Channel Isolation:*** At low frequencies, this is principally a function of channel off-leakage currents, and at high frequencies, it is a function of device and system capacitance.

3. ***Crosstalk***: There are several sources of crosstalk, including overlap between switching channels, off-switch capacitance, inter-switch capacitance, stray circuit capacitance, and distortion in the transmission medium.

4. *Noise*: There are several sources of noise, including thermal or Johnson noise generated in any resistance components, crosstalk, leakages, switching transients, as well as thermal EMFs and transmission path pick up.

5. *Switching Rate*: This is important in sampling system where it determines the maximum bandwidth frequency of the multiplexers (via the sampling theorem) and defines crosstalk errors.

6. *Settling Time*: Although settling time is a function for the source and load impedances, the multiplexer's contribution is directly related to the $r_{DS(on)} \times C_{S(on)}$ time constant and to the charge injection of the multiplexer.

Glossary of Terms

Bandwidth

The "3 dB down" point of the frequency response characteristic.

Crosspoint Switch

A two-dimensional array of analog switches or analog multiplexers that allows for the routing of signals from any input to any output.

Crosstalk

A measure of how much of an unwanted signal appears on a given analog channel due to spurious capacitive or inductive coupling from another channel.

D/CMOS

Semiconductor process that combines DMOS FETs and CMOS logic on a monolithic chip.

Differential Gain

Expressed as a percentage, this is a form of distortion that appears as changes in the amplitude of the chrominance (color) signal as a function of luminance (brightness) amplitude.

Differential Multiplexer

An analog multiplexer that selects both the high and the low side of each signal. It can be thought of as two single-ended multiplexers operating in tandem.

Differential Phase

Measured in degrees, this is the phase shift of the color subcarrier resulting from changes in luminance level.

DMOS (Double-Diffused MOS)

A type of field-effect transistor featuring low on-resistance and low capacitance.

Input Capacitance

The capacitive load that the input terminal of an analog switch presents to the signal source. It is specified for two conditions, with the switch on or off.

Insertion Loss

Expressed in dB, this is a measure of the signal loss caused by the impedance of the analog switch at a given frequency.

Off-Isolation

A measure of how much of the signal applied to an "open" switch appears at its output due to parasitic components such as gate-to-channel capacitance and lead inductance.

On-resistance

The dc input-to-output resistance of an analog switch channel when the switch is turned on.

Output Capacitance

The capacitive load that the output of an off switch adds to the output node.

PLCC Package (Plastic Leaded Chip Carrier)

A surface-mount package characterized for its small size and reliable lead-to-printed circuit board mechanical interface

Readback

A feature that allows for the inspection of the control latch contents in a multiplexer or crosspoint switch.

Single-Ended Multiplexer

An array of analog switches that selects one of several analog input signals.

"T" Switch

An analog switch configuration consisting of two series switches and a shunt switch to ground. It is used to improve dramatically the off-isolation of the array.

Video Amplifier

An amplifier, typically with a gain of 2, which is normally used at the output of a video multiplexer or crosspoint to drive a length of double-terminated coaxial cable.

Video Buffer

A current amplifier that is used is to preserve signal quality by eliminating the capacitive loading effect to several video multiplexer inputs on a common signal source. This is normally a unity gain buffer.

Wideband

A relative term that is used in this book to refer to a frequency spectrum that is more than 2 MHz wide.

Analog Multiplexer Selector Guide

Functional Configuration	Part No.	Max $r_{DS(on)}$ (Ω)	Max $I_{S(on)}$ (nA)	Analog Range (V)	Transition Time (μs)	Typical Charge Injection (pC)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
2-Channel Differential	DG534A	90	20	−5 to 10	0.3	−70	–	59.5	J, N, P	Video, Latches	2-86
4-Channel Differential	DG534A	90	20	−5 to 10	0.3	−70	–	59.5	J, N, P	Video, Latches	2-86
	DG538A	90	20	−5 to 10	0.3	−70	–	59.5	J, N, P	Video, Latches	2-86
	DG409	100	1	±15	0.25	20	Yes	0.9	J, K, Y, Z	High Speed	2-11
	DG429	100	1	±15	0.25	4	Yes	1.58	J, K, N	Latchable, High Speed	2-22
	DG509A	400	10	±15	1.0	20	Yes	58.5	J, K, Y	–	2-60
	DG529	400	10	±15	1.0	4	Yes	60	J, K	Latchable	2-70
	DG459	1200	2	−9.5 to 10	0.5	–	Yes	3	J, K, Z	Fault Protected	2-34
8-Channel Single-Ended	DG538A	90	20	−5 to 10	0.3	−70	–	59.5	J, N, P	Video, Latches	2-86
	DG408	100	1	±15	0.2	20	Yes	0.9	J, K, Y	High Speed	2-11
	DG428	100	1	±15	0.25	4	Yes	1.58	J, K, N	Latchable, High Speed	2-22
	DG508A	400	10	±15	1.0	20	Yes	59.5	J, K, Y, Z	–	2-60
	DG528	400	10	±15	1.0	4	Yes	60	J, K	Latchable	2-70
	DG458	1200	2	−9.5 to 10	0.5	–	Yes	3	J, K, Z	Fault Protected	2-34
8-Channel Differential	DG407	100	1	±15	0.3	15	Yes	0.5	J, K, N, Z	High Speed	2-1
	DG507A	400	5	±15	1.0	20	Yes	58.5	J, K, R	–	2-52
16-Channel Single-Ended	DG535	90	10	0 to 10	0.3	−35	–	0.75	J, P	Low Power, Video	2-102
	DG536	90	10	0 to 10	0.3	−35	–	0.75	M, N	Low Power, Video	2-102
	DG406	100	1	±15	0.3	20	Yes	0.47	J, K, N, Z	Low Power, Fast	2-1
	DG506A	400	10	±15	1.0	20	Yes	58.5	J, K, N, R, Z	–	2-52
Specials	DG485	85	20	±15	0.2	17	–	0.11	J, N, Z	8-Ch, Serial Control	2-42
	DG884	90	20	−5 to 8	0.3	−100	–	92.5	M, N	8x4 Video Crosspoint	2-113
	DG894	100	10	−5 to 8	0.2	–	Yes	136	J, W	RGB Video Mux	2-126

J = Plastic DIP
K = CerDIP
M = CLCC
N = PLCC
P = Sidebraze
R = Sidebraze
W = SOIC Wide-Body
Y = SOIC
Z = LCC

16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

Features

- Low On-Resistance—$r_{DS(on)}$: 50 Ω
- Low Charge Injection—Q: 15 pC
- Fast Transition Time—t_{TRANS}: 200 ns
- Low Power: 0.2 mW
- Single Supply Capability
- 44-V Supply Max Rating

Benefits

- Higher Accuracy
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Superior to DG506/507A
- Wide Supply Ranges: ±5 V to ±20 V

Applications

- Data Acquisition Systems
- Audio Signal Routing
- Medical Instrumentation
- ATE Systems
- Battery Powered Systems
- High-Rel Systems
- Single Supply Systems

Description

The DG406 is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407 selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

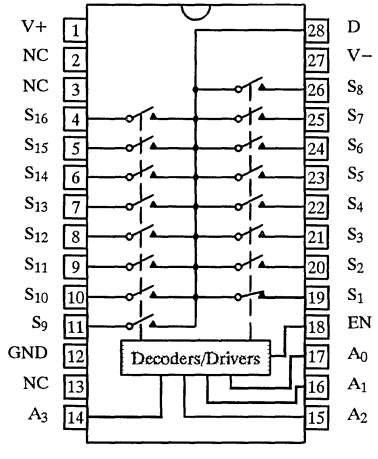
An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406/407 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications. For additional application information, see application note AN206.

Designed in the 44-V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with ±20-V supplies. Additionally single (12-V) supply operation is allowed. An epitaxial layer prevents latchup.

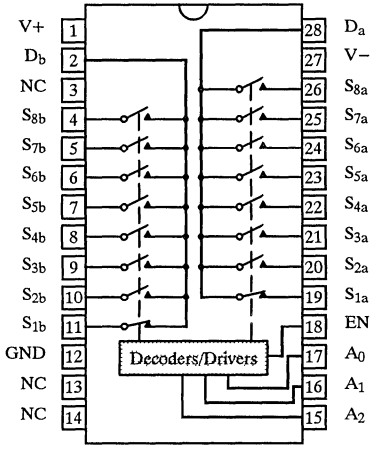
Functional Block Diagrams and Pin Configurations

DG406 Dual-In-Line



Top View

DG407 Dual-In-Line

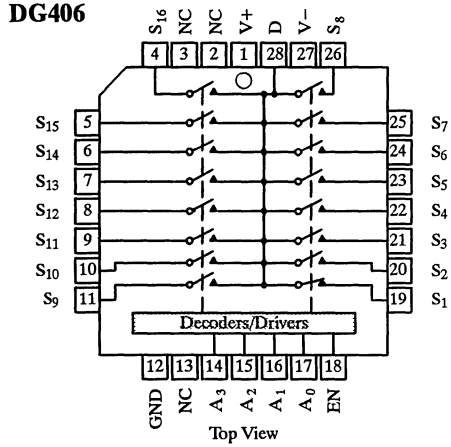


Top View

Functional Block Diagrams and Pin Configurations (Cont'd)

DG406

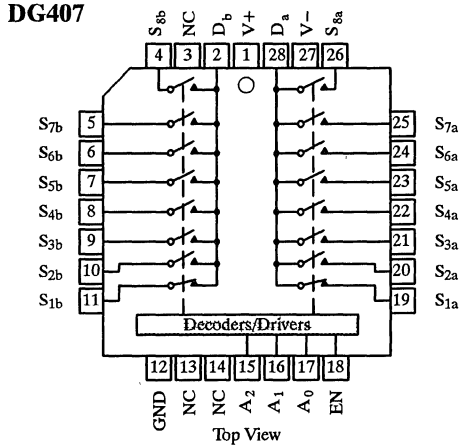
PLCC and LCC



Top View

DG407

PLCC and LCC



Top View

Truth Table — DG406

A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table — DG407

A_2	A_1	A_0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information — DG406

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG406DJ
	28-Pin PLCC	DG406DN
−55 to 125°C	28-Pin CerDIP	DG406AK/883
	LCC-28	DG406AZ/883

Ordering Information — DG407

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG407DJ
	28-Pin PLCC	DG407DN
−55 to 125°C	28-Pin CerDIP	DG407AK/883
	LCC-28	DG407AZ/883

Absolute Maximum Ratings

Voltages Referenced to V−

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first

Current (Any Terminal,) ..... 30 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA

Storage Temperature (AK, AZ Suffix) ..... −65 to 150°C
(DJ, DN Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]

28-Pin Plastic DIP[c] ..... 625 mW

28-Pin CerDIP[d] ..... 1.2 W

28-Pin Plastic PLCC[e] ..... 450 mW

LCC-28[e] ..... 1.35 W

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C
e. Derate 13.5 mW/°C above 75°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −10 mA Sequence Each Switch On		Room Full	50		100 125		100 125	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$	V_D = ±10 V		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_D = ±10 V, V_S = ∓10 V		Room Full	0.01	−0.5 −50	0.5 50	−0.5 −5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$		DG406	Room Full	0.04	−1 −200	1 200	−1 −40	1 40	
			DG407	Room Full	0.04	−1 −100	1 100	−1 −20	1 20	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V Sequence Each Switch On	DG406	Room Full	0.04	−1 −200	1 200	−1 −40	1 40	
			DG407	Room Full	0.04	−1 −100	1 100	−1 −20	1 20	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{AH}	V_A = 2.4 V, 15 V		Full		−1	1	−1	1	µA
Logic Low Input Current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		−1	1	−1	1	
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	7					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Room Full	200		300 400		300 400	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room Full	50	25 10		25 10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	150		200 400		200 400	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room Full	70		150 300		150 300	
Charge Injection	Q	C_L = 1 nF, V_S = 0 V, R_s = 0 Ω		Room	15					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, f = 100 kHz		Room	−69					dB

2

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)										
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	8					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 1 MHz		Room	130					
			DG407	Room	65					
Drain On Capacitance	$C_{D(on)}$		DG406	Room	140					
			DG407	Room	70					
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0 or 5 V		Room Full	13		30 75		30 75	µA
Negative Supply Current	I−			Room Full	−0.01	−1 −10		−1 −10		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room Full	50		100 500		100 200	
Negative Supply Current	I−			Room Full	−0.01	−1 −10		−1 −10		

Specifications[a] for Single Supply

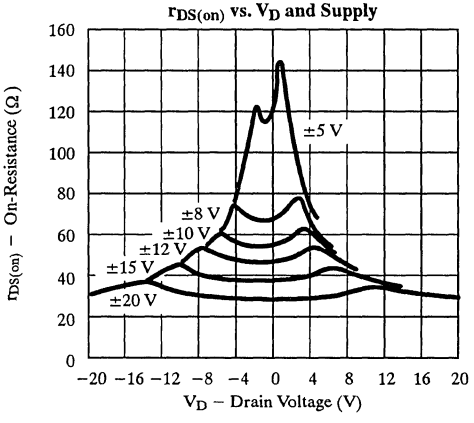
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = 3 V, 10 V, I_S = − 1 mA Sequence Each Switch On		Room	90		120		120	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$			Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V V_D = 10 V or 0.5 V V_S = 0.5 V or 10 V		Room	0.01					nA
Drain Off Leakage Current	$I_{D(off)}$		DG406	Room	0.04					
			DG407	Room	0.04					
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V Sequence Each Switch On	DG406	Room	0.04					
			DG407	Room	0.04					
Dynamic Characteristics										
Switching Time of Multiplexer	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V		Room	300		450		450	ns
Enable Turn-On Time	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V V_{S1} = 5 V		Room	250		600		600	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	150		300		300	
Charge Injection	Q	C_L = 1 nF, V_S= 6 V, R_S = 0		Room	20					pC

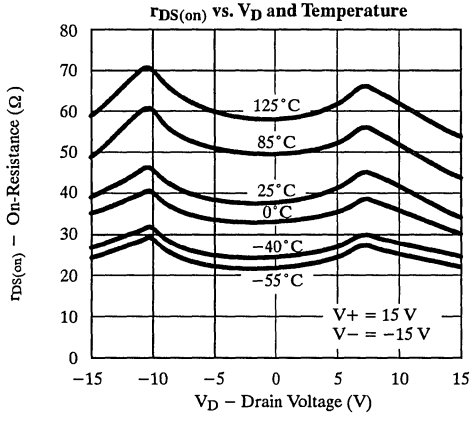
Specifications[a] for Single Supply

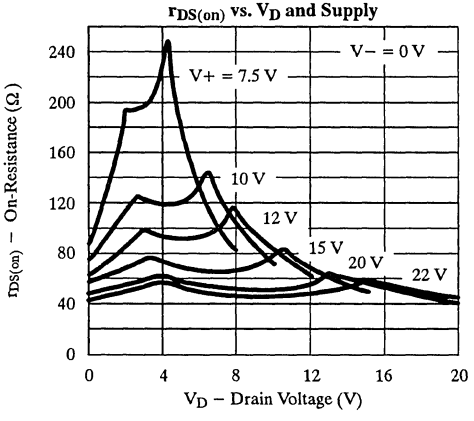
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V_{EN} = 0 V or 5 V, V_A = 0 V or 5 V	Room Full	13		30 75		30 75	µA
Negative Supply Current	I−		Room Full	−0.01	−1 −5		−1 −5		

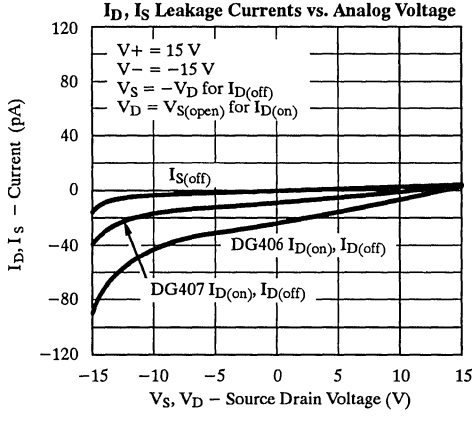
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = r_{DS(on)}$ MAX − $r_{DS(on)}$ MIN.
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

Typical Characteristics





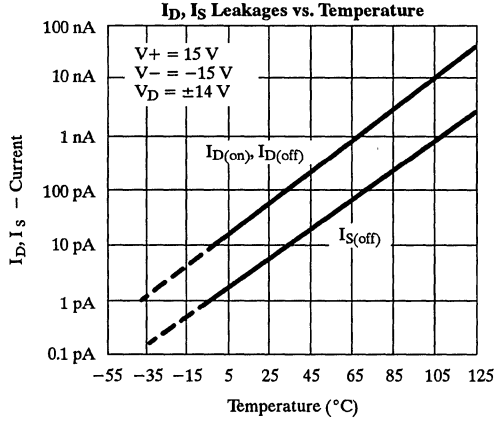




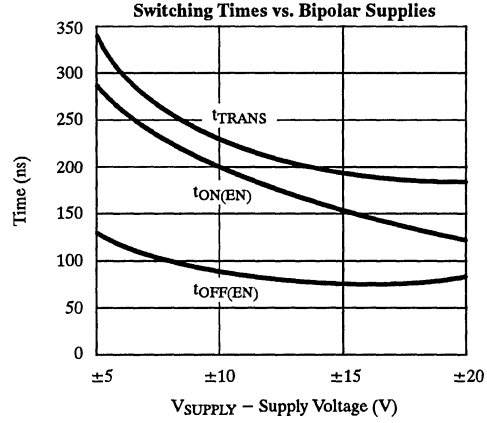
2

Typical Characteristics (Cont'd)

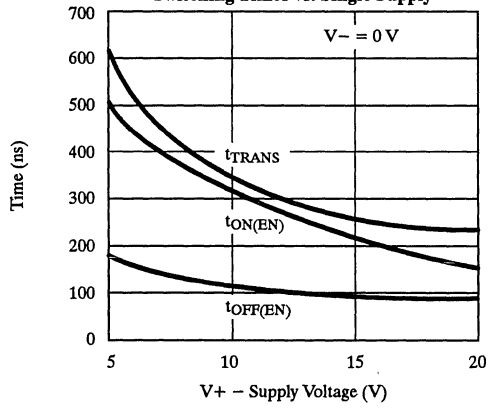
I_D, I_S Leakages vs. Temperature



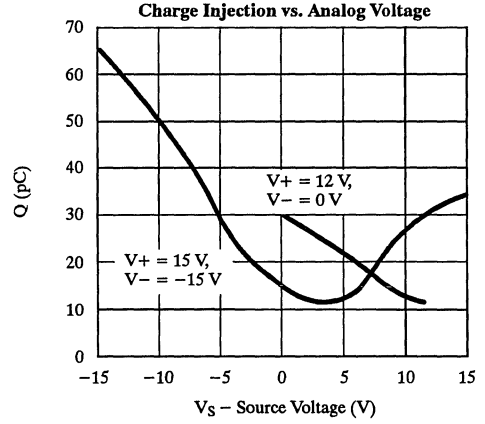
Switching Times vs. Bipolar Supplies



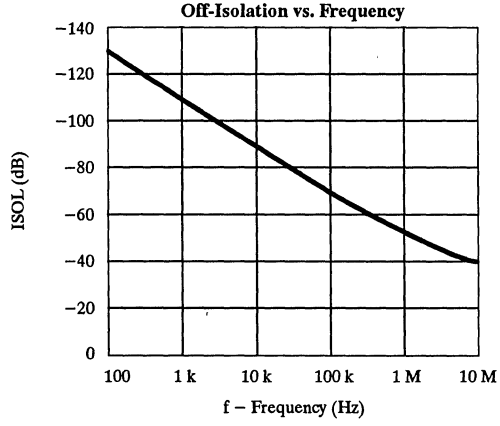
Switching Times vs. Single Supply



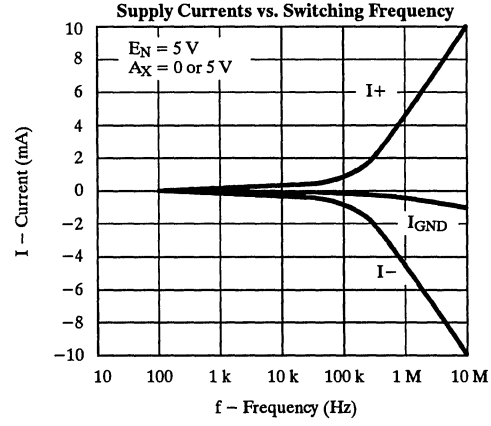
Charge Injection vs. Analog Voltage



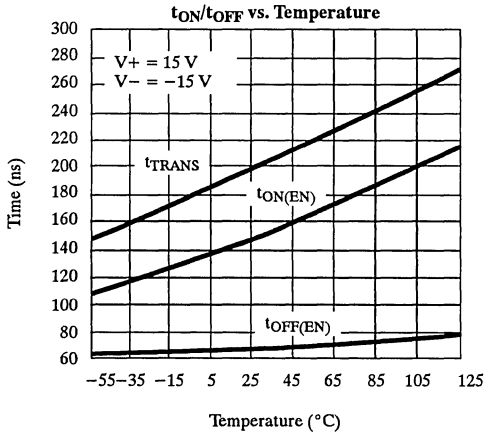
Off-Isolation vs. Frequency

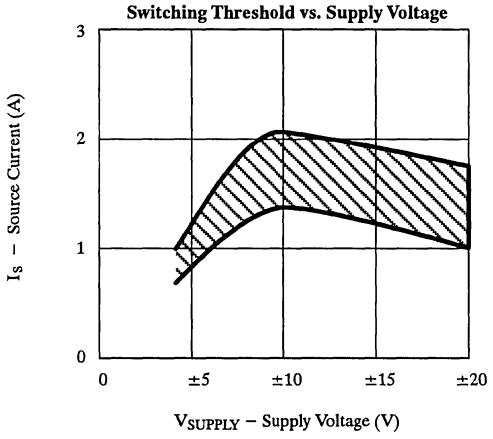


Supply Currents vs. Switching Frequency



Typical Characteristics (Cont'd)





Schematic Diagram (Typical Channel)

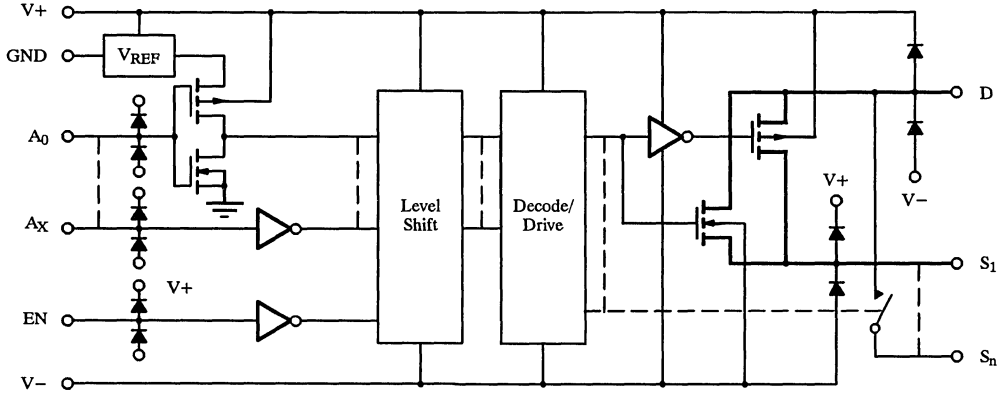
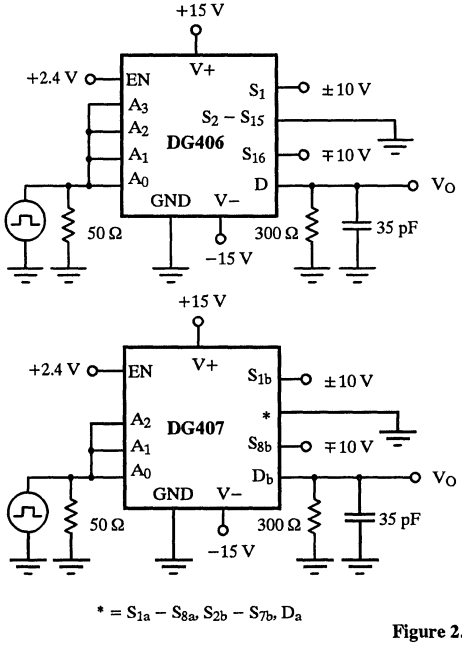


Figure 1.

Test Circuits



* = $S_{1a} - S_{8a}$, $S_{2b} - S_{7b}$, D_a

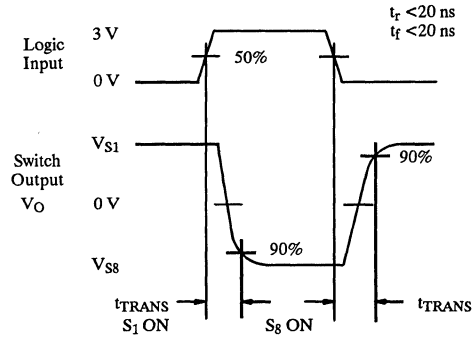
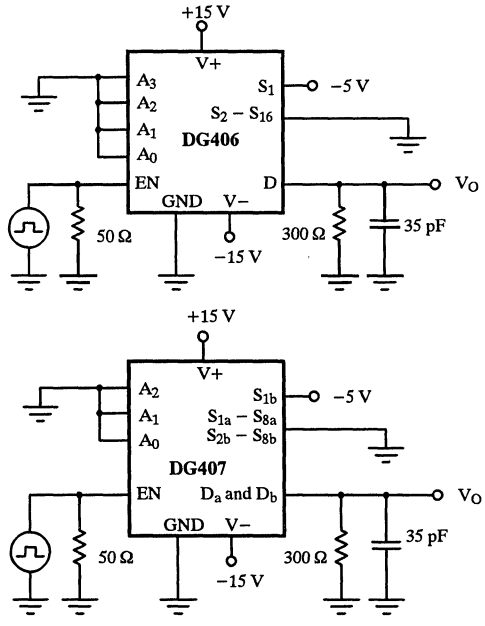


Figure 2. Transition Time



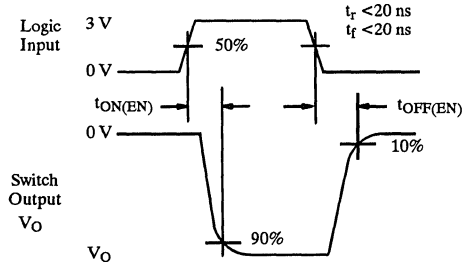


Figure 3. Enable Switching Time

Test Circuits (Cont'd)

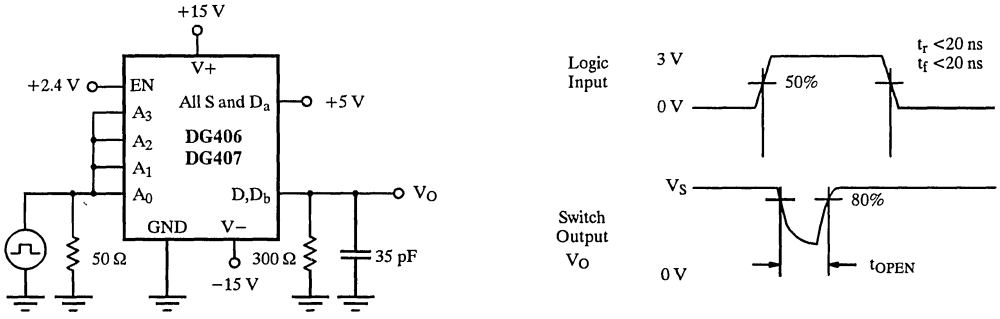


Figure 4. Break-Before-Make Interval

Application Hints

Sampling speed is limited by two consecutive events: the transition time of the multiplexer, and the settling time of the sampled signal at the output.

t_{TRANS} is given on the data sheet. Settling time at the load depends on several parameters: $r_{DS(on)}$ of the multiplexer, source impedance, multiplexer and load capacitances, charge injection of the multiplexer and accuracy desired.

The settling time for the multiplexer alone can be derived from the model shown in Figure 5. Assuming a low impedance signal source like that presented by an op amp or a buffer amplifier, the settling time of the RC network for a given accuracy is equal to $n\tau$:

% Accuracy	# Bits	n
0.25	8	6
0.012	12	9
0.0017	15	11

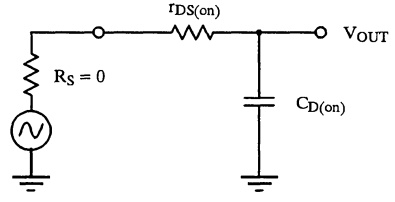


Figure 5. Simplified Model of One Multiplexer Channel

The maximum sampling frequency of the multiplexer is:

$$f_s = \frac{1}{N\,(t_{SETTLING} + t_{TRANS})} \qquad (195)$$

where N = number of channels to scan

$t_{SETTLING} = n\tau = n \times r_{DS(on)} \times C_{D(on)}$

For the DG406 then, at room temp and for 12-bit accuracy, using the maximum limits:

$$f_s = \frac{1}{16\,(9 \times 100\ \Omega \times 100 \times 10^{-12}\ F) + 300 \times 10^{-12}\ s} \qquad (196)$$

or

$$f_s = 694\ kHz \qquad (197)$$

From the sampling theorem, to properly recover the original signal, the sampling frequency should be more than twice the maximum component frequency of the original signal. This assumes perfect bandlimiting. In a real application sampling at three to four times the filter cutoff frequency is a good practice.

Therefore from equation (197) above:

$$f_c = \frac{1}{4} \times f_s = 173\ kHz \qquad (198)$$

From this we can see that the DG406 can be used to sample 16 different signals whose maximum component frequency can be as high as 173 kHz. If for example, two channels are used to double sample the same incoming signal then its cutoff frequency can be doubled.

2

Application Hints (Cont'd)

The block diagram shown in Figure 6 illustrates a typical data acquisition front end suitable for low-level analog signals. Differential multiplexing of small signals is preferred since this method helps to reject any common mode noise. This is especially important when the sensors are located at a distance and it may eliminate the need for individual amplifiers. A low $r_{DS(on)}$, low leakage multiplexer like the DG407 helps to reduce measurement errors. The low power dissipation of the DG407 minimizes on-chip thermal gradients which can cause errors due to temperature mismatch along the parasitic thermocouple paths. Please refer to Application Note AN203 for additional information.

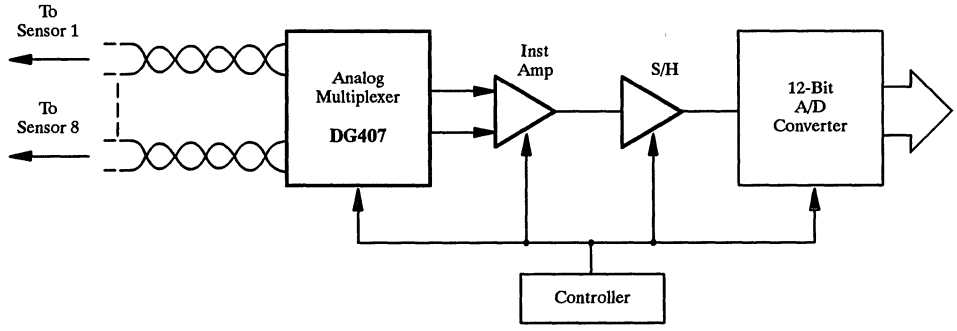


Figure 6. Measuring low-level analog signals is more accurate when using a differential multiplexing technique.

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

Features

- Low On-Resistance—$r_{DS(on)}$: 100 Ω
- Low Charge Injection—Q: 20 pC
- Fast Transition Time—t_{TRANS}: 160 ns
- Low Power—I_{SUPPLY}: 10 µA
- Single Supply Capability
- 44-V Supply Max Rating

Benefits

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Superior to DG508/509A
- Wide Supply Ranges (±5 V to ±20 V)

Applications

- Data Acquisition Systems
- Audio Signal Routing
- ATE Systems
- Battery Powered Systems
- High Rel Systems
- Single Supply Systems
- Medical Instrumentation

Description

The DG408 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409 is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

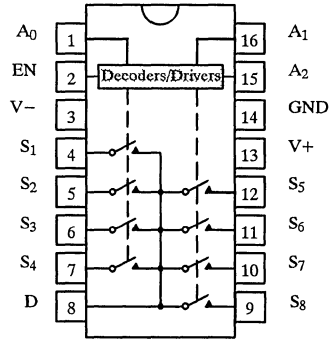
Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44-V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see App Note AN201 and Technical TA201.

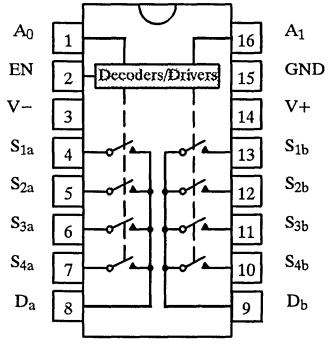
Functional Block Diagrams and Pin Configurations

DG408 Dual-In-Line and SOIC



Top View

DG409 Dual-In-Line and SOIC



Top View

2

Truth Table — DG408

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Truth Table — DG409

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information — DG408

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG408DJ
	16-Pin SOIC	DG408DY
−55 to 125°C	16-Pin CerDIP	DG408AK
		DG408AK/883
		5962-920401MEA
	LCC-20*	5962-920401M2A

Ordering Information — DG409

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG409DJ
	16-Pin SOIC	DG409DY
−55 to 125°C	16-Pin CerDIP	DG409AK
		DG409AK/883
		5962-920402MEA
	LCC-20*	5962-920402M2A

*Block Diagram and Pin Configuration not shown.

Absolute Maximum Ratings

Voltage Referenced to V−

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first

Current (Any Terminal) ..... 30 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA

Storage Temperature (AK Suffix) ..... −65 to 150°C
(DJ, DY Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]

16-Pin Plastic DIP[c] ..... 450 mW

16-Pin Narrow SOIC[d] ..... 600 mW

16-Pin CerDIP[e] ..... 900 mW

LCC-20[f] ..... 750 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 7.6 mW/°C above 75°C.
e. Derate 12 mW/°C above 75°C.
f. Derate 10 mW/°C above 75°C.

Specifications[a]

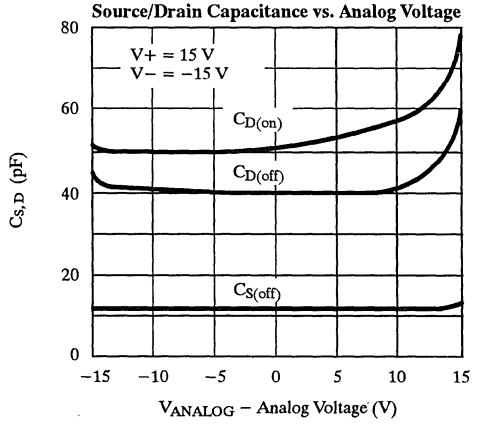
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −10 mA		Room Full	40		100 125		100 125	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$	V_D = ±10 V		Room			15		15	%
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V_{EN} = 0 V		Room Full		−0.5 −50	0.5 50	−0.5 −5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±10 V, V_S = ∓10 V V_{EN} = 0 V	DG408	Room Full		−1 −100	1 100	−1 −20	1 20	
			DG409	Room Full		−1 −50	1 50	−1 −10	1 10	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V Sequence Each Switch On	DG408	Room Full		−1 −100	1 100	−1 −20	1 20	
			DG409	Room Full		−1 −50	1 50	−1 −10	1 10	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{AH}	V_A = 2.4 V, 15 V		Full		−10	10	−10	10	µA
Logic Low Input Current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		−10	10	−10	10	
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Full	160		250		250	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room		10		10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	115		150 225		150	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	105		150		150	
Charge Injection	Q	C_L = 10 nF, V_S = 0 V		Room	20					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, f = 100 kHz		Room	−75					dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	3					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 1 MHz	DG408	Room	26					
			DG409	Room	14					
Drain On Capacitance	$C_{D(on)}$		DG408	Room	37					
			DG409	Room	25					
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0 V or 5 V		Full	10		75		75	µA
Negative Supply Current	I−			Full	1	−75		−75		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room Full	0.2		0.5 2		0.5 2	mA
Negative Supply Current	I−			Full		−500		−500		µA

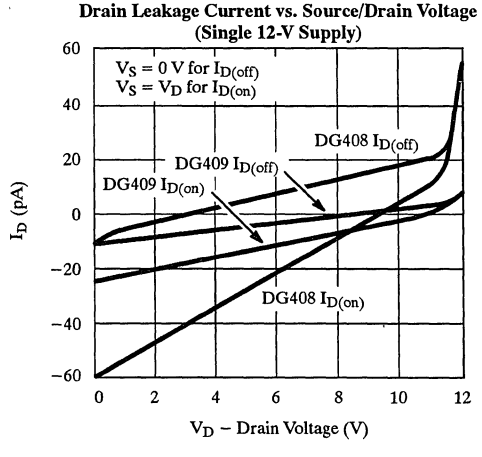
Specifications[a] for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Analog Switch									
Drain-Source On-Resistance[e, f]	$r_{DS(on)}$	V_D = 3 V, 10 V, I_S = − 1 mA	Room	90					Ω
Dynamic Characteristics									
Switching Time of Multiplexer[e]	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V	Room	180					ns
Enable Turn On Time[e]	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V V_{S1} = 5 V	Room	180					
Enable Turn Off Time[e]	$t_{OFF(EN)}$		Room	120					
Charge Injection[e]	Q	C_L = 1 nF, V_S = 6 V, R_S = 0	Room	5					pC

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = r_{DS(on)}$ Max − $r_{DS(on)}$ Min.
h. Worst case isolation occurs on Channel 4 do to proximity to the drain pin.

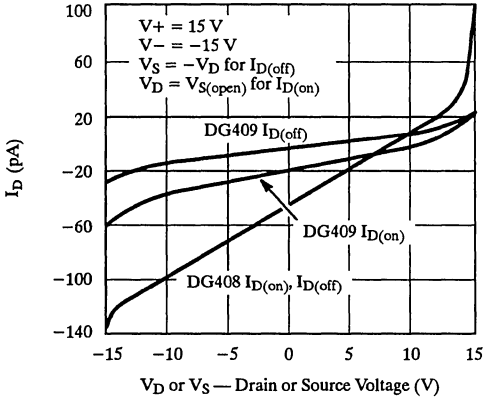
Typical Characteristics



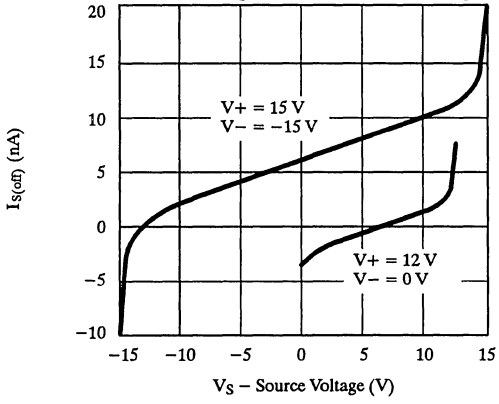


Typical Characteristics (Cont'd)

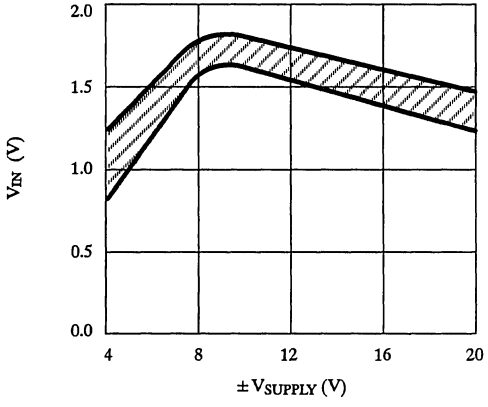
Drain Leakage Current vs. Source/DrainVoltage



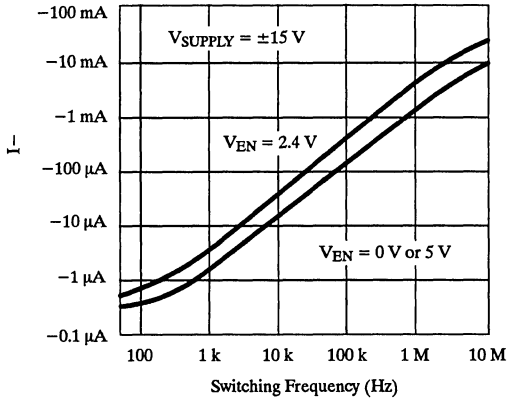
Source Leakage Current vs. Source Voltage



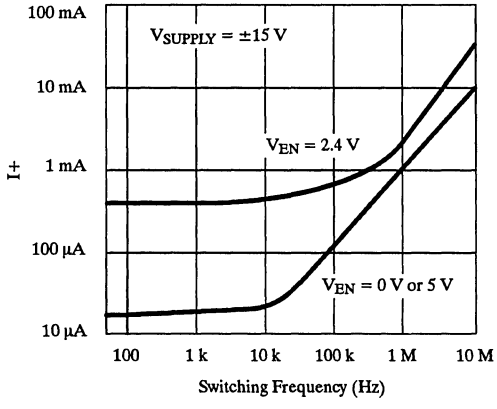
Input Switching Threshold vs. Supply Voltage



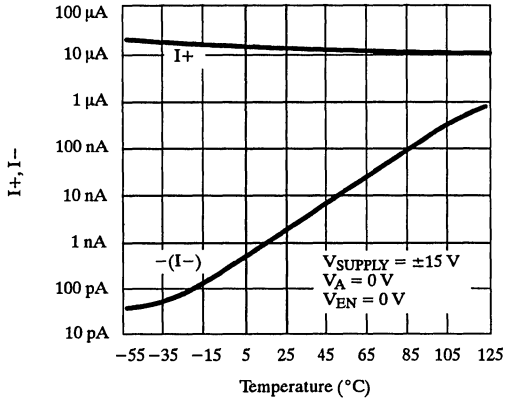
Negative Supply Current vs. Switching Frequency



Positive Supply Current vs. Switching Frequency



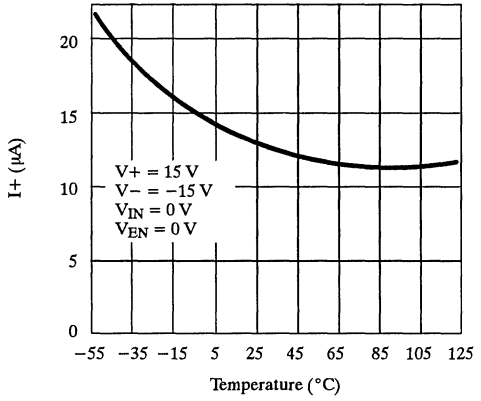
ISUPPLY vs. Temperature



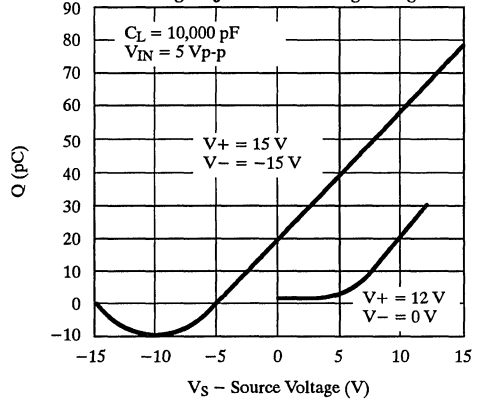
2

Typical Characteristics (Cont'd)

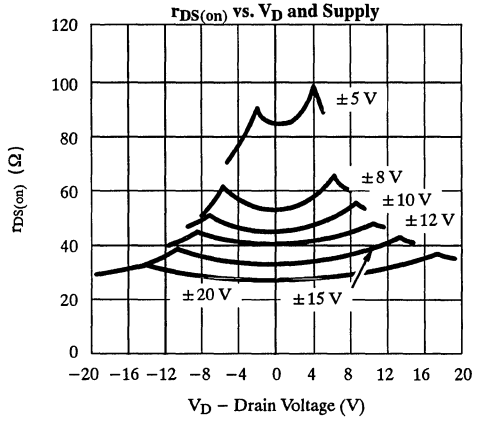
Positive Supply Current vs. Temperature (DG408)



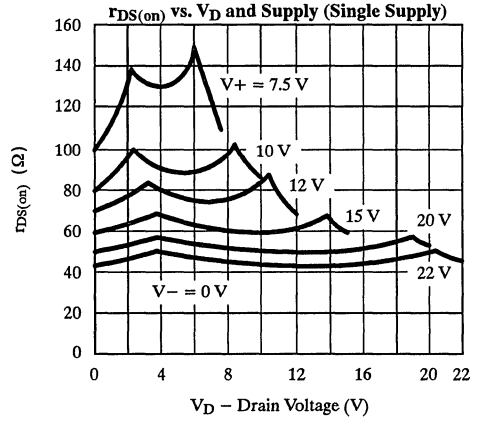
Charge Injection vs. Analog Voltage



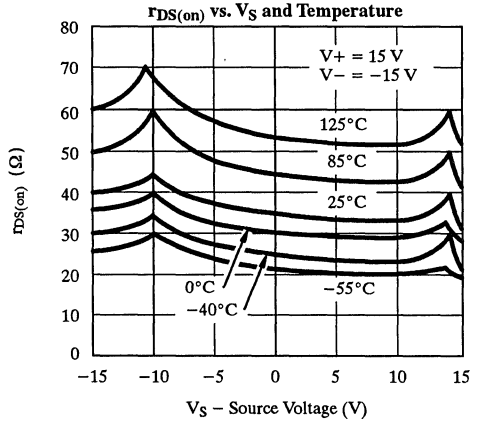
$r_{DS(on)}$ vs. V_D and Supply



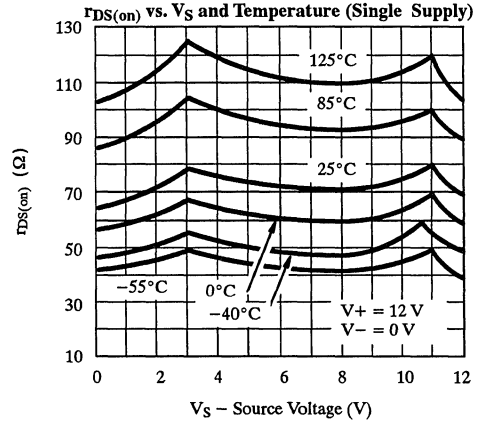
$r_{DS(on)}$ vs. V_D and Supply (Single Supply)



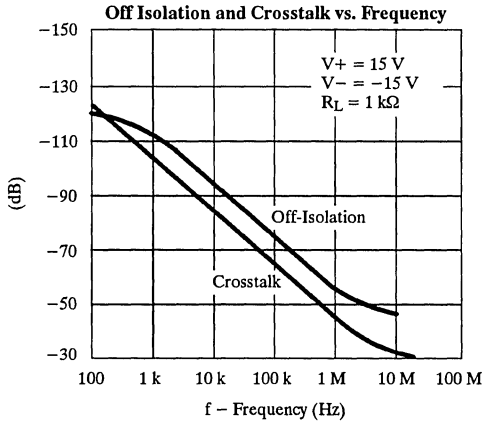
$r_{DS(on)}$ vs. V_S and Temperature

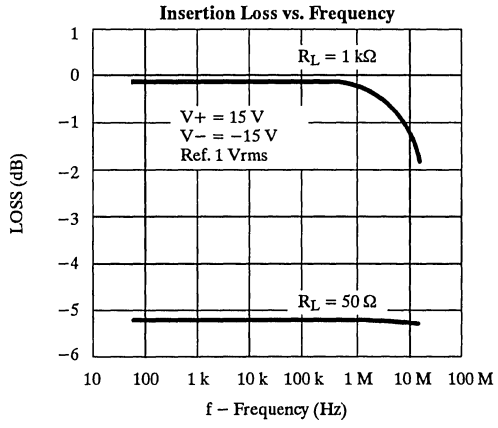


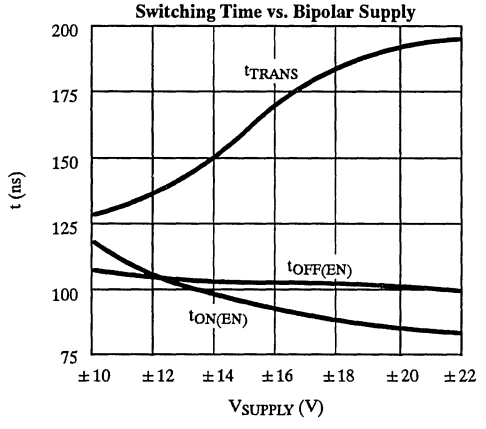
$r_{DS(on)}$ vs. V_S and Temperature (Single Supply)

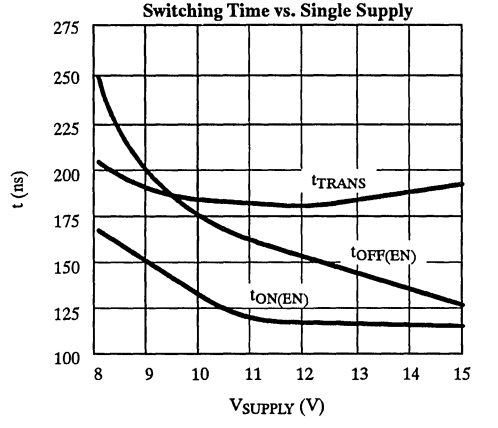


Typical Characteristics (Cont'd)









Schematic Diagram (Typical Channel)

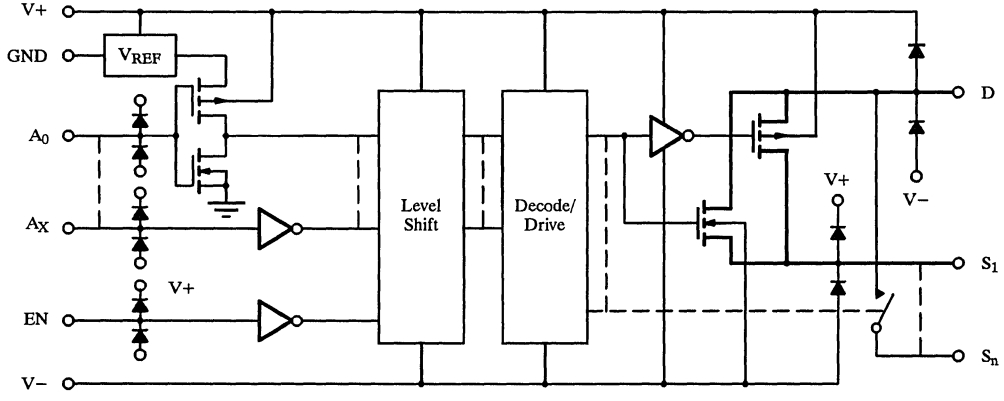
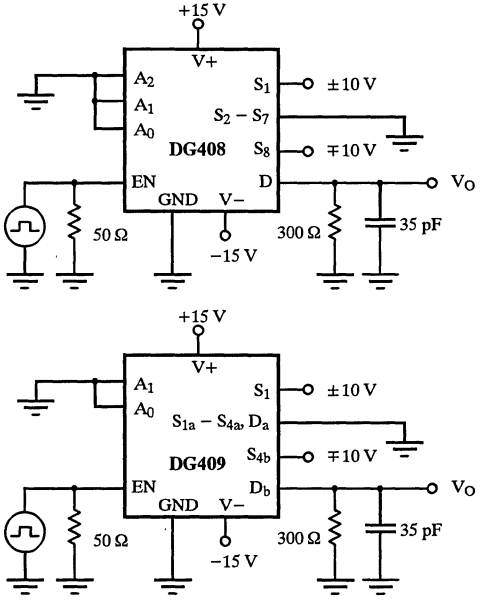


Figure 1.

Test Circuits



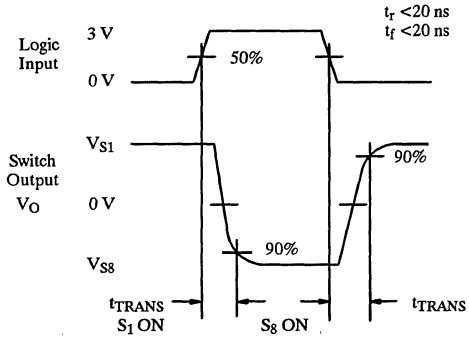
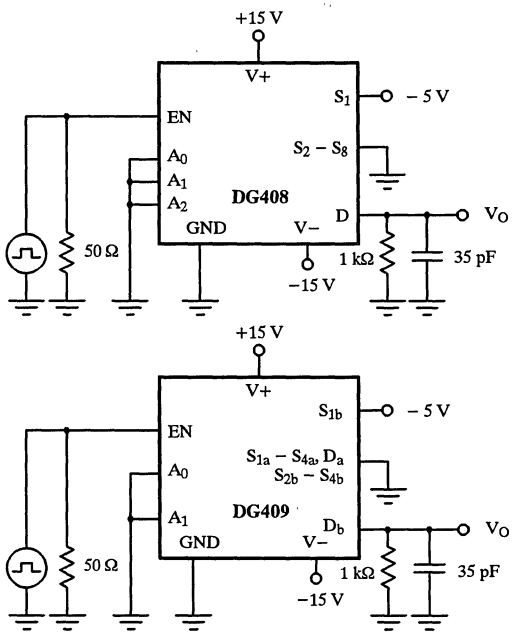


Figure 2. Transition Time



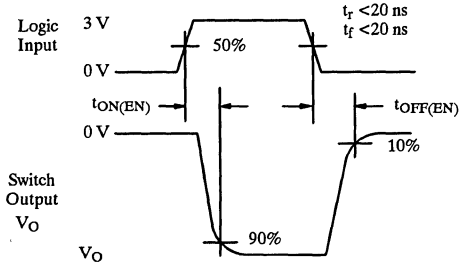


Figure 3. Enable Switching Time

Test Circuits (Cont'd)

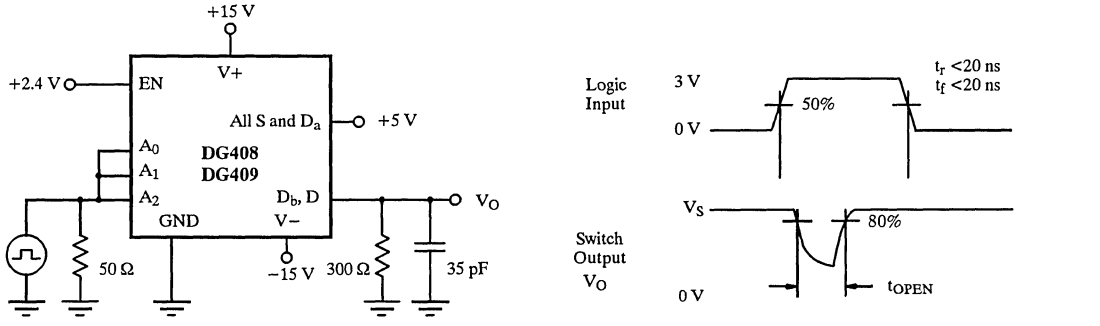


Figure 4. Break-Before-Make Interval

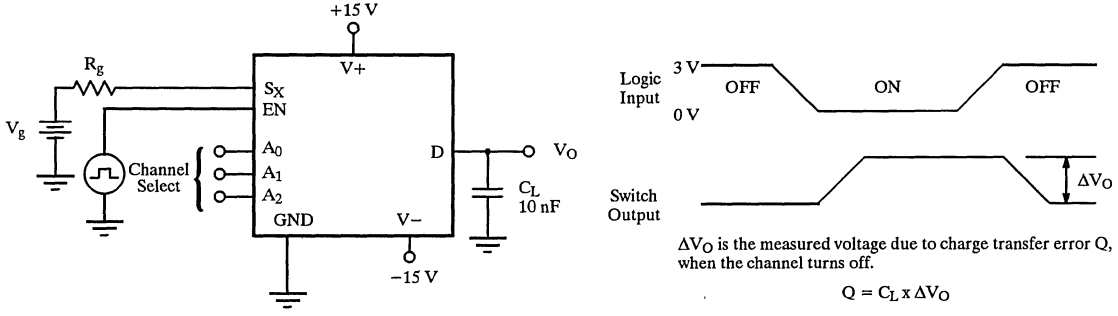


Figure 5. Charge Injection

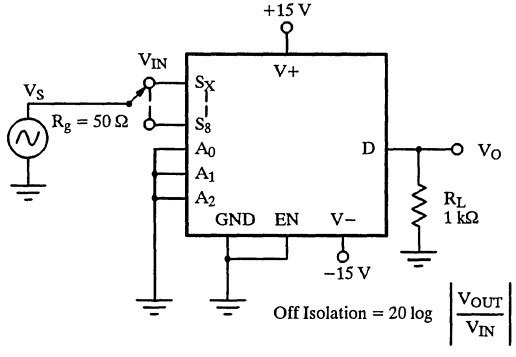


Figure 6. Off Isolation

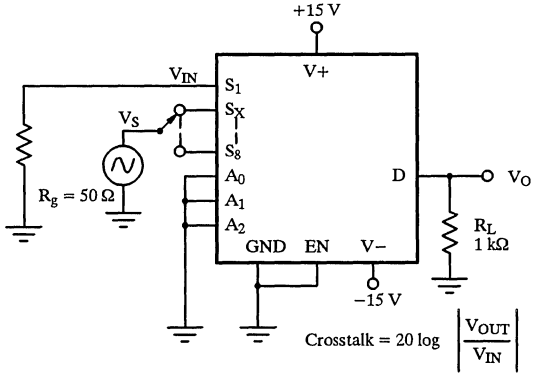


Figure 7. Crosstalk

2

Test Circuits (Cont'd)

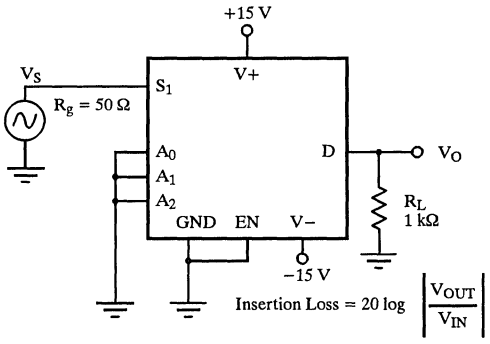


Figure 8. Insertion Loss

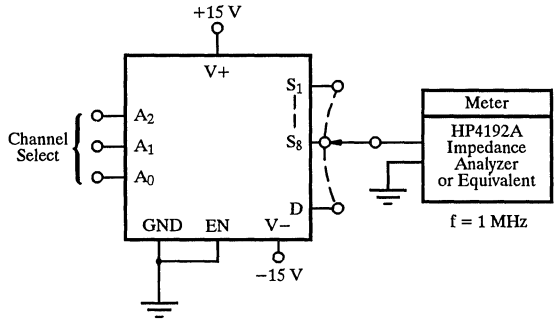


Figure 9. Source Drain Capacitance

Application Hints

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V− value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference $V_S - (V-)$ doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V−, but it preserves the low channel resistance and low leakage characteristics.

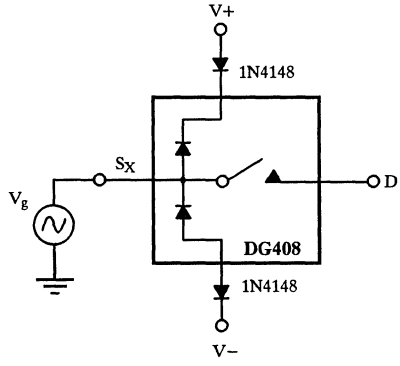
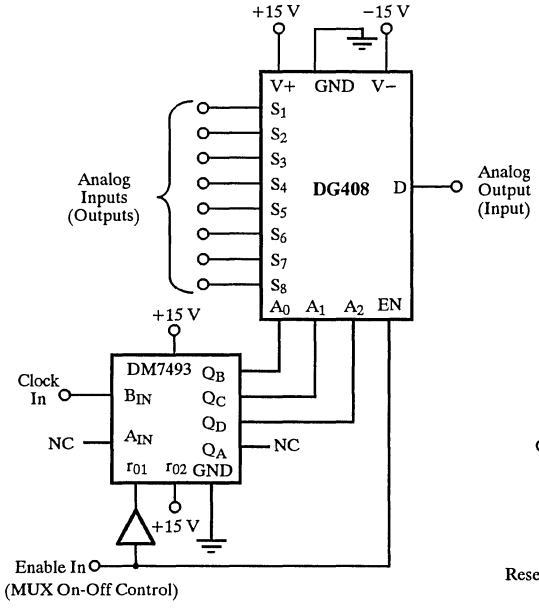


Figure 10. Overvoltage Protection Using Blocking Diodes

Applications

8-Channel Sequential Multiplexer/Demultiplexer



Differential 4-Channel Sequential Multiplexer/Demultiplexer

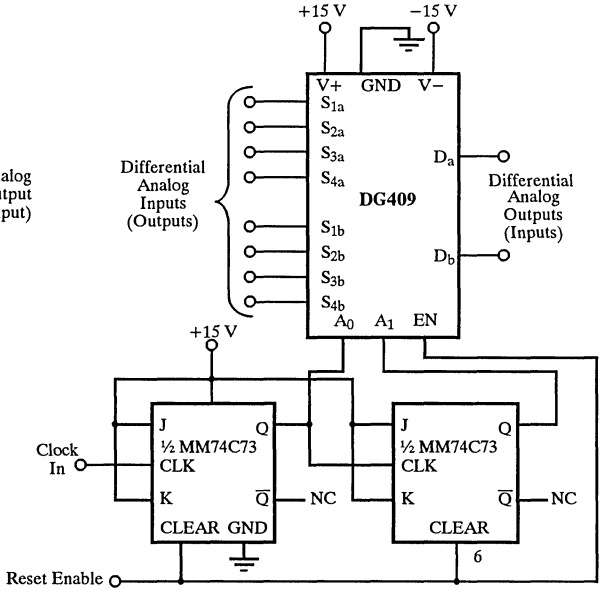


Figure 11.

Single 8-Channel/Differential 4-Channel Latchable Analog Multiplexers

Features

- Low $r_{DS(on)}$: 55 Ω
- Low Charge Injection: 1 pC
- On-Board TTL Compatible Address Latches
- High Speed—t_{TRANS}: 160 ns
- Break-Before-Make
- Low Power Consumption: 0.3 mW

Benefits

- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk
- High Throughput
- Improved Reliability

Applications

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor Controlled Analog Systems
- Medical Instrumentation

Description

The DG428/DG429 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary crosstalk of adjacent input signals.

The DG428 selects one of eight single-ended inputs to a common output, while the DG429 selects one of four differential inputs to a common differential output.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

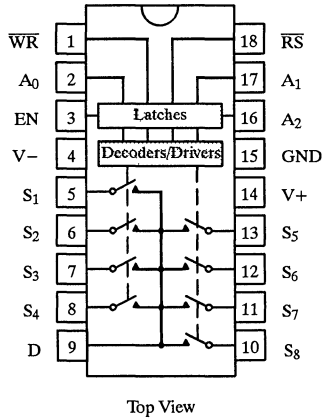
The silicon-gate CMOS process enables operation over a wide range of supply voltages. The absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed and an epitaxial layer prevents latchup.

On-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE.

Functional Block Diagrams and Pin Configurations

DG428

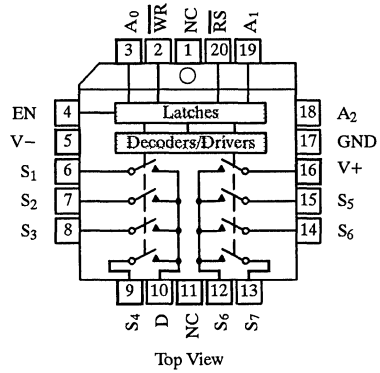
Dual-In-Line



Top View

DG428

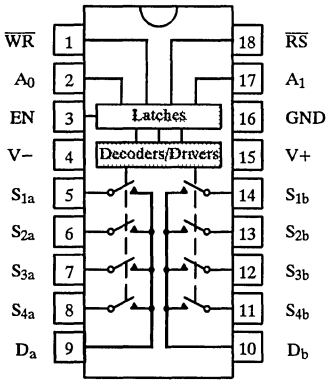
PLCC



Top View

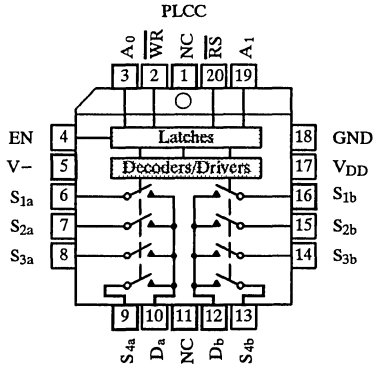
Functional Block Diagrams and Pin Configurations (Cont'd)

DG429 Dual-In-Line



Top View

DG429 PLCC



Top View

Truth Table — DG428
8-Channel Single-Ended Multiplexer

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X	↓	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Truth Table — DG429
Differential 4-Channel Multiplexer

A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching					
X	X	X	↓	1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information — DG428

Temp Range	Package	Part Number
−40 to 85°C	18-Pin Plastic DIP	DG428DJ
	20-Pin PLCC	DG428DN
−55 to 125°C	18-Pin CerDIP	DG428AK
		DG428AK/883

Ordering Information — DG429

Temp Range	Package	Part Number
−40 to 85°C	18-Pin Plastic DIP	DG429DJ
	20-Pin PLCC	DG429DN
−55 to 125°C	18-Pin CerDIP	DG429AK
		DG429AK/883

Absolute Maximum Ratings

Voltage Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal) ..... 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA
Storage Temperature (AK Suffix) ..... −65 to 150°C
(DJ, DN Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
18-Pin Plastic DIP[c] ..... 470 mW
18-Pin CerDIP[d] ..... 900 mW
20-Pin PLCC[e] ..... 800 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6.3 mW/°C above 75°C.
d. Derate 12 mW/°C above 75°C.
e. Derate 10 mW/°C above 75°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, V_{AL} = 0.8 V I_S = −1 mA, V_{AH} = 2.4 V		Room Full	55		100 125		100 125	Ω
Greatest Change in $r_{DS(on)}$ Between Channels[g]	$\Delta r_{DS(on)}$	−10 V < V_S < 10 V I_S = −1 mA		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V_{EN} = 0 V		Room Full	±0.03	−0.5 −50	0.5 50	−0.5 −50	0.5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±10 V V_S = ∓10 V V_{EN} = 0 V	DG428	Room Full	±0.07	−1 −100	1 100	−1 −100	1 100	
			DG429	Room Full	±0.05	−1 −50	1 50	−1 −50	1 50	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V V_{EN} = 2.4 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	DG428	Room Full	±0.07	−1 −100	1 100	−1 −100	1 100	
			DG429	Room Full	±0.05	−1 −50	1 50	−1 −50	1 50	
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Full	0.01		1		1	µA
		V_A = 15 V		Full	0.01		1		1	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Full	−0.01	−1		−1		
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 5		Room Full	150		250 300		250 300	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Full	30	10		10		
Enable and Write Turn-On Time	$t_{ON(EN, WR)}$	See Figures 6 and 7		Room Full	90		150 225		150 225	
Enable and Reset Turn-Off Time	$t_{OFF(EN, RS)}$	See Figures 6 and 8		Room Full	55		150 300		150 300	
Charge Injection	Q	V_{GEN} = 0 V, R_{GEN} = 0 Ω C_L = 1 nF, See Figure 9		Room	1					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 300 Ω, C_L = 15 pF V_S = 7 V_{RMS}, f = 100 kHz		Room	−75					dB

Specifications[a] (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)										
Source Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{EN} = 0 V, f = 1 MHz		Room	11					pF
Drain Off Capacitance	$C_{D(off)}$	V_D = 0 V, V_{EN} = 0 V f = 1 MHz	DG428	Room	40					
			DG429	Room	20					
Drain On Capacitance	$C_{D(on)}$		DG428	Room	54					
			DG429	Room	34					
Minimum Input Timing Requirements										
Write Pulse Width	t_W	See Figure 2		Full		100		100		ns
Ax, EN Data Set Up time	t_S			Full		100		100		
Ax, EN Data Hold Time	t_H			Full		10		10		
Reset Pulse Width	t_{RS}	V_S = 5 V, See Figure 3		Full		100		100		
Power Supplies										
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0, $\overline{RS}$ = 5 V		Room	20		100		100	μA
Negative Supply Current	I−			Room	−0.001	−5		−5		

Specifications[a] for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = +10 V, V_{AL} = 0.8 V I_S = −500 μA, V_{AH} = 2.4 V		Room	80		150		150	Ω
$r_{DS(on)}$ Match[g]	$\Delta r_{DS(on)}$	−10 V < V_S < 10 V I_S = −1 mA		Room	5					%
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, 10 V, V_D = 10 V, 0 V V_{EN} = 0 V		Room Full	±0.03	−0.5 −50	0.5 50	−0.5 −50	0.5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = 0 V, 10 V V_S = 10 V, 0 V V_{EN} = 0 V	DG428	Room Full	±0.07	−1 −100	1 100	−1 −100	1 100	
			DG429	Room Full	±0.05	−1 −50	1 50	−1 −50	1 50	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V, 10 V V_{EN} = 2.4 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	DG428	Room Full	±0.07	−1 −100	1 100	−1 −100	1 100	
			DG429	Room Full	±0.05	−1 −50	1 50	−1 −50	1 50	
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Full			1		1	μA
		V_A = 12 V		Full			1		1	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Full		−1		−1		

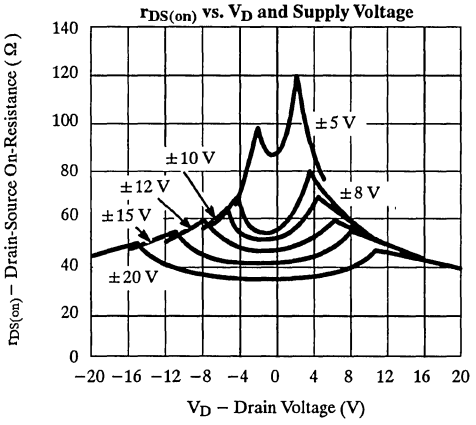
2

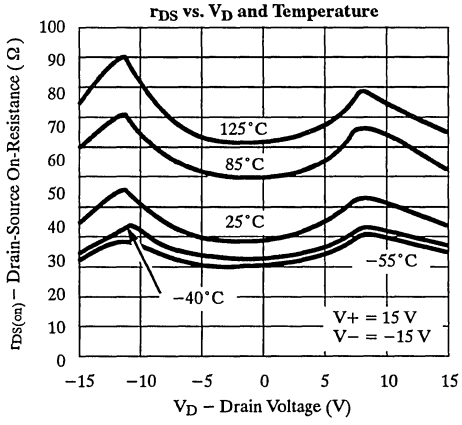
Specifications[a] for Single Supply

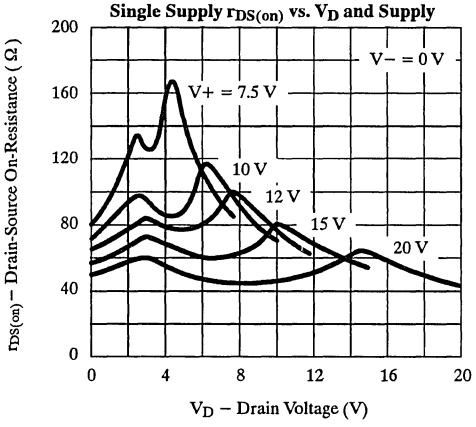
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics									
Transition Time	t_{TRANS}	See Figure 5	Room Full	160		280 350		280 350	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4	Room Full	40	25 10		25 10		ns
Enable and Write Turn-On Time	$t_{ON(EN, WR)}$	See Figures 6 and 7	Room Full	110		300 400		300 400	ns
Enable and Reset Turn-Off Time	$t_{OFF(EN, RS)}$	See Figures 6 and 8	Room Full	70		300 400		300 400	ns
Charge Injection	Q	V_{GEN} = 6 V, R_{GEN} = 0 Ω C_L = 1 nF, See Figure 9	Room	4					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 300 Ω, C_L = 15 pF V_S = 7 V_{RMS}, f = 100 kHz	Room	−75					dB
Minimum Input Timing Requirements									
Write Pulse Width	t_W	See Figure 2	Full		100		100		ns
A_X, EN Data Set Up Time	t_S		Full		100		100		ns
A_X, EN Data Hold Time	t_H		Full		10		10		ns
Reset Pulse Width	t_{RS}	V_S = 5 V, See Figure 3	Full		100		100		ns
Power Supplies									
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0, $\overline{RS}$ = 5 V	Room	20		100		100	µA

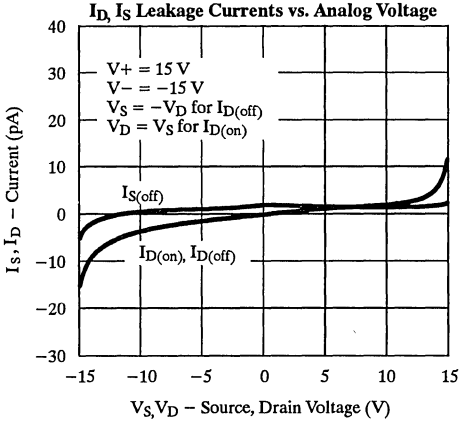
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ MAX - r_{DS(on)}\ MIN}{r_{DS(on)}\ AVE} \right) \times 100\%$

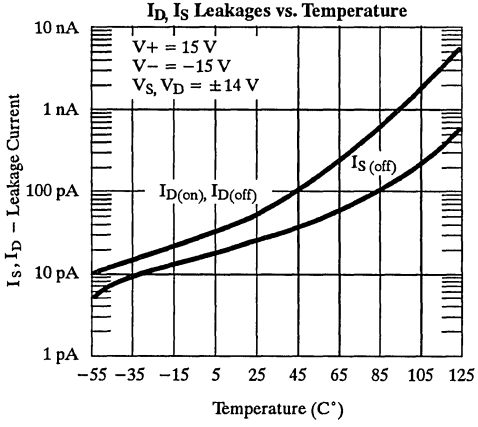
Typical Characteristics

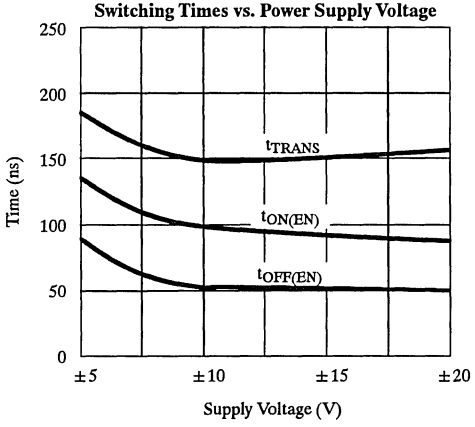








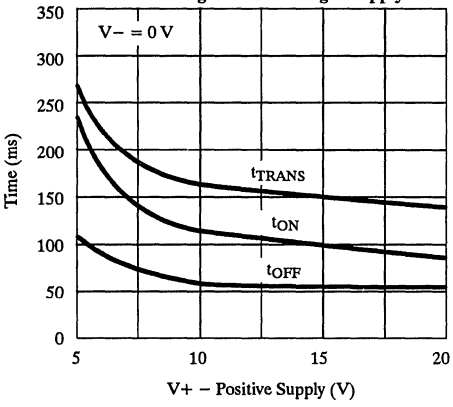




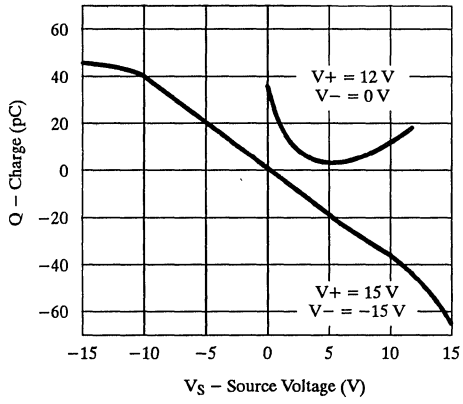
2

Typical Characteristics (Cont'd)

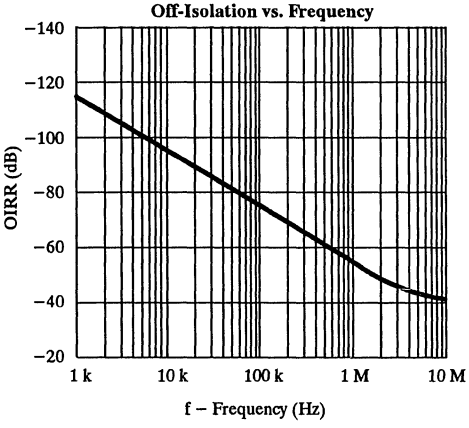
Switching Times vs. Single Supply



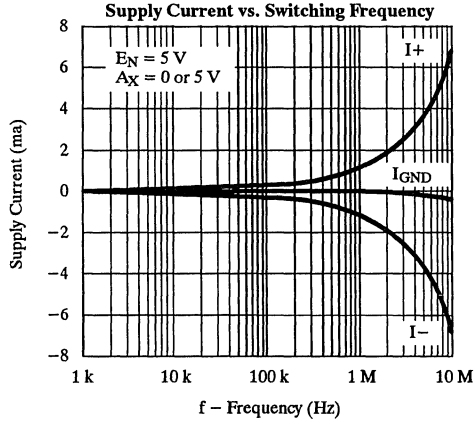
Charge Injection vs. Analog Voltage



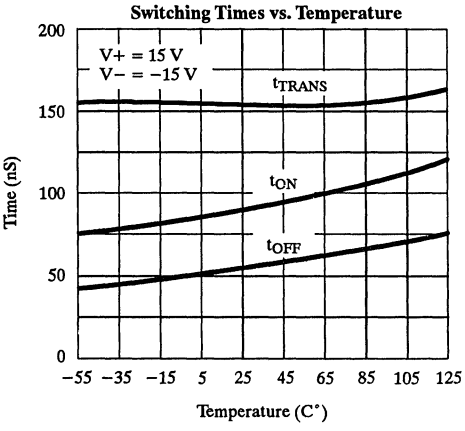
Off-Isolation vs. Frequency



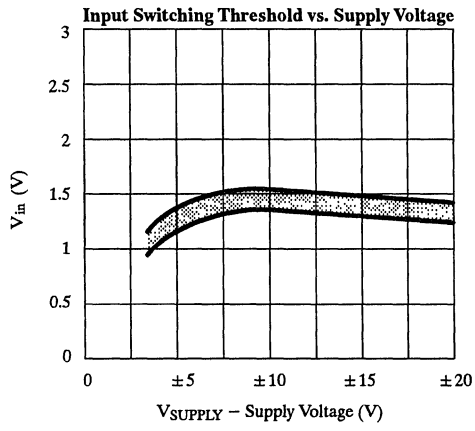
Supply Current vs. Switching Frequency



Switching Times vs. Temperature



Input Switching Threshold vs. Supply Voltage



Schematic Diagram (Typical Channel)

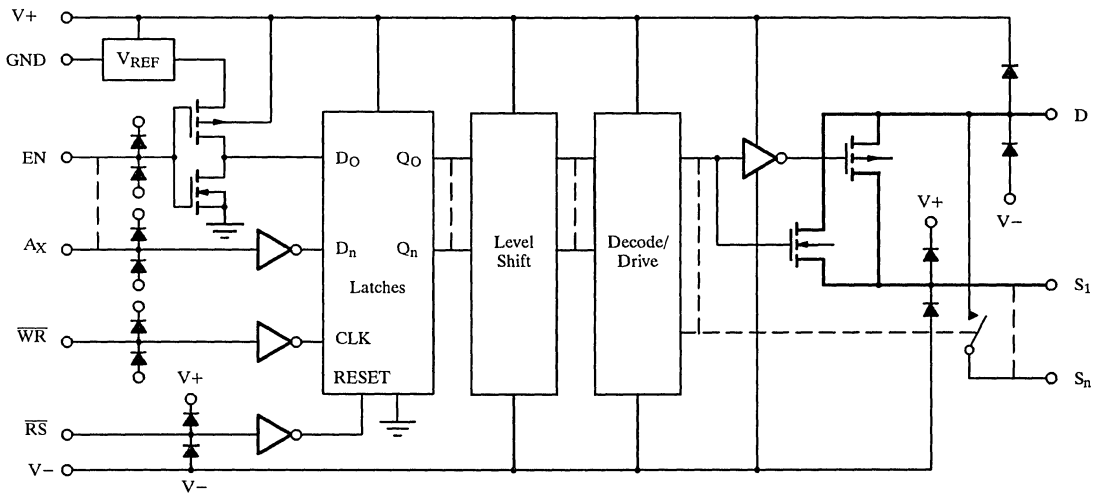


Figure 1.

Detailed Description

The internal structure of the DG428/DG429 includes a 5-V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The input protection on the logic lines A_0, A_1, A_2, EN and control lines $\overline{WR}$, $\overline{RS}$ shown in Figure 1 minimizes susceptibility to ESD that may be encountered during handling and operational transients.

The logic interface is a CMOS logic input with its supply voltage from an internal +5 V reference voltage. The output of the input inverter feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the $\overline{WR}$ input is low, resulting in transparent latch operation. As soon as $\overline{WR}$ returns high the latch holds the data last present on the D_n input, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_n signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting ensures full on/off switch operation for any analog signal level between the V+ and V− supply rails.

The EN pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply or to V+ if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

Timing Diagrams

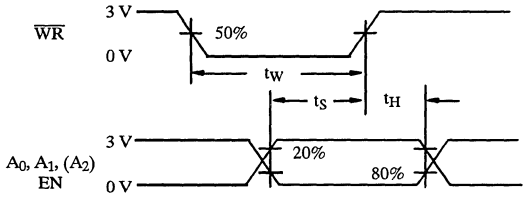


Figure 2.

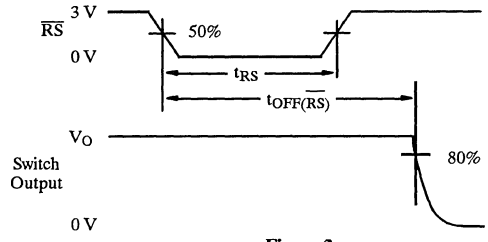
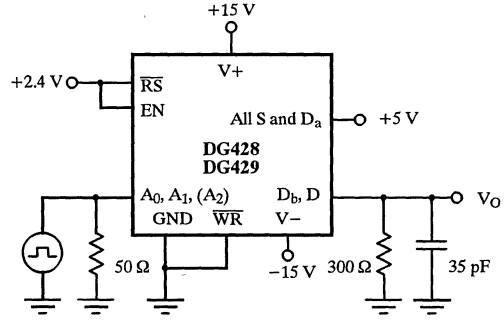


Figure 3.

Test Circuits



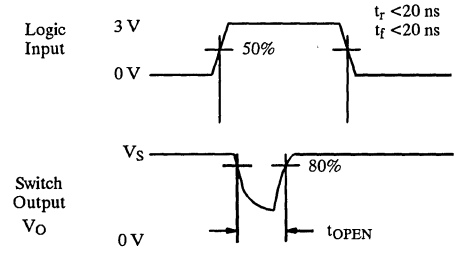
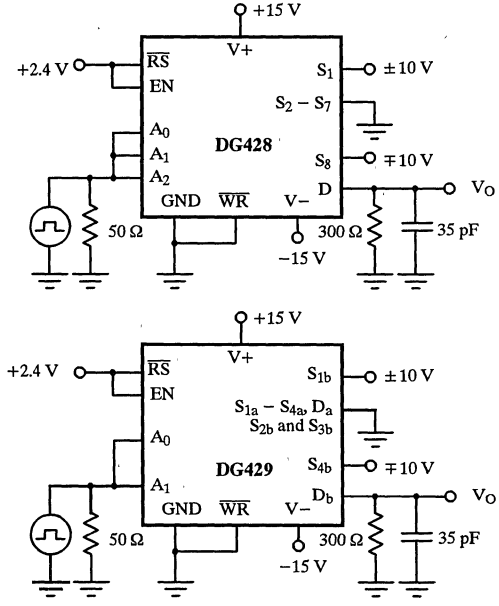


Figure 4. Break-Before-Make



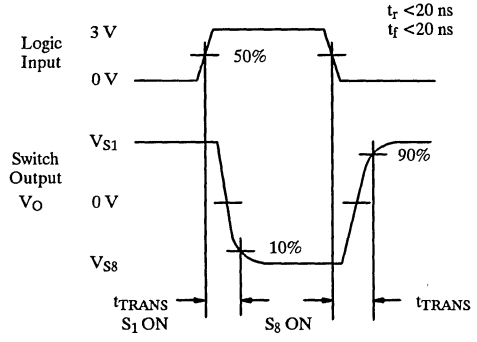
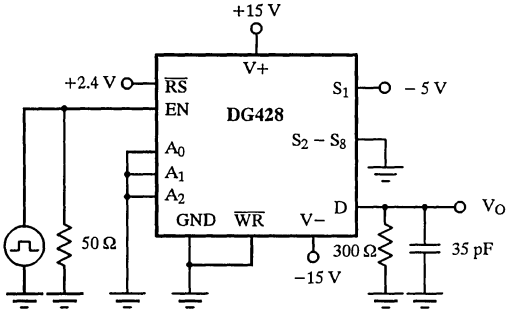
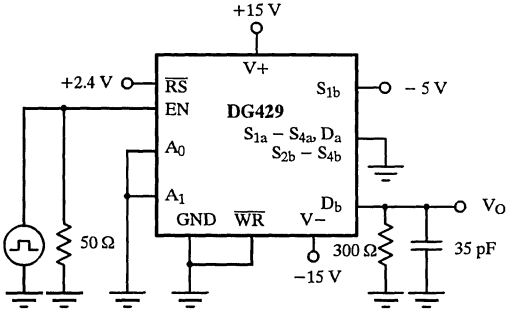


Figure 5. Transition Time

Test Circuits (Cont'd)





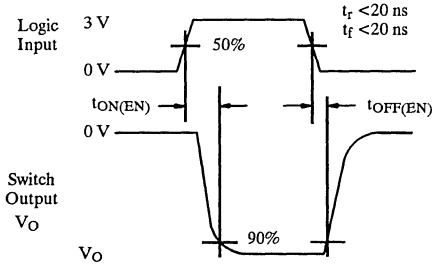
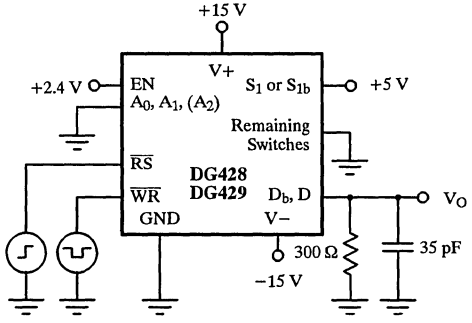


Figure 6. Enable t_{ON}/t_{OFF} Time



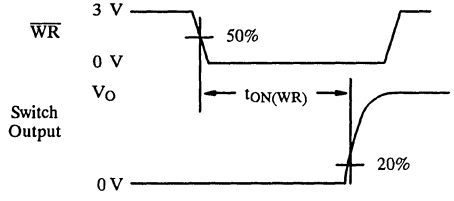


Figure 7. Write Turn-On Time $t_{ON(WR)}$

Test Circuits (Cont'd)

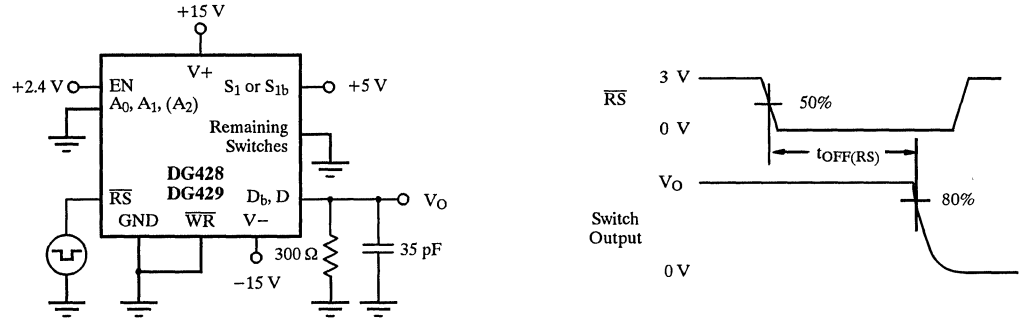


Figure 8. Reset Turn-Off Time $t_{OFF(RS)}$

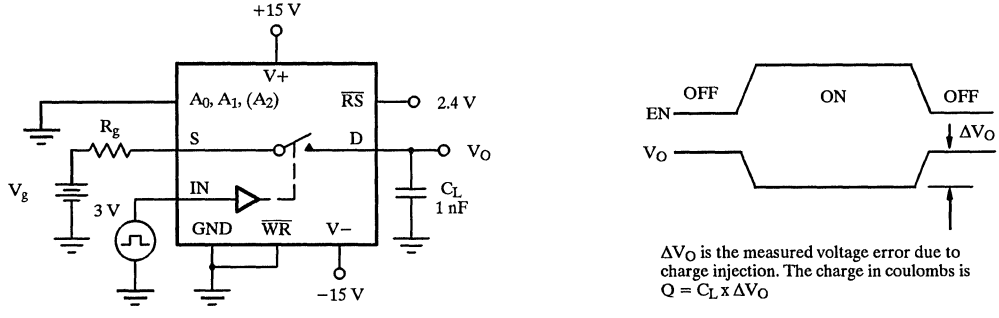


Figure 9. Charge Injection

Applications

Bus Interfacing

The DG428/DG429 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 10).

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A_2, A_1, A_0. In this mode the DG428 is identical to the popular DG408. The same is true of the DG429 versus the popular DG409.

During system power-up, $\overline{RS}$ would be low, maintaining all eight switches in the off state. After $\overline{RS}$ returned high the DG428 maintains all switches in the off state.

Applications (Cont'd)

When the system program performs a write operation to the address assigned to the DG428, the address decoder provides a $\overline{CS}$ active low signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the high state, (positive edge) the input latches of the DG428 save the data from the DATA BUS. The coded information in the A_0, A_1, A_2 and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG428s are cascaded to build 16-line and larger multiplexers.

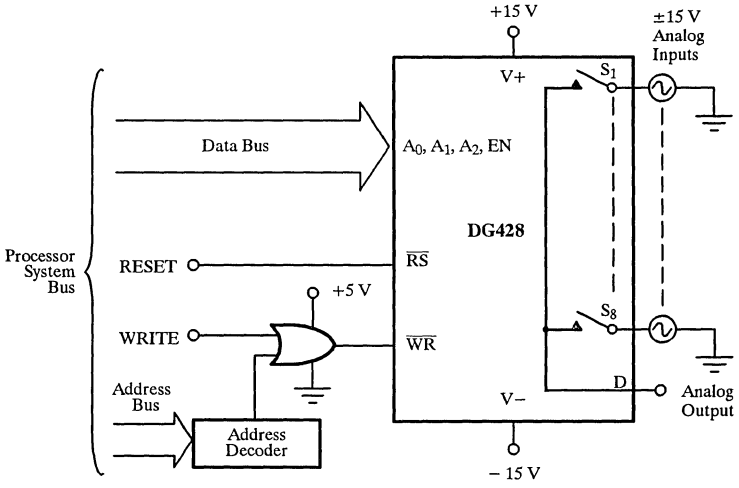


Figure 10. Bus Interface

Fault Protected Single 8-Channel/Differential 4-Channel Analog Multiplexers

Features

- Fault and Overvoltage Protection
- All Channels Off When Power Off
- Latchup-Proof
- Fast Switching—T_A: 200 ns
- Break-Before-Make Switching
- Low On-Resistance: 180 Ω
- Low Power Consumption: 3 mW
- TTL and CMOS Compatible Inputs

Benefits

- Improved Ruggedness
- Power Loss Protection
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface
- Superior Accuracy
- Fast Settling Time

Applications

- Data Acquisition Systems
- Industrial Process Control Systems
- Avionics Test Equipment
- High-Rel Control Systems
- Telemetry

Description

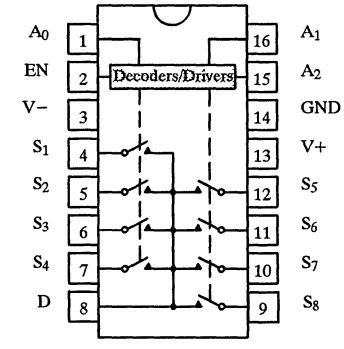
The DG458 and DG459 are 8-channel single-ended and 4-channel differential analog multiplexers, respectively, incorporating fault protection. A series n-p-n MOSFET structure provides device and signal-source protection in the event of power loss or overvoltages. Under fault conditions the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry following it, but also protects the sensors or signal sources which drive the multiplexer.

The DG458 and DG459 can withstand continuous overvoltage inputs up to ±35 V. All digital inputs have TTL compatible logic thresholds. Break-before-make operation prevents channel-to-channel interference.

The DG458 and DG459 are improved pin-compatible replacements for HI-508A/509A and MAX358/359 multiplexers.

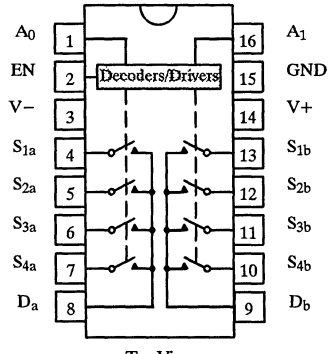
Functional Block Diagrams and Pin Configurations

DG458 Dual-In-Line



Top View

DG459 Dual-In-Line



Top View

Truth Tables and Ordering Information

Truth Table — DG458

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Truth Table — DG459

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG458DJ
		DG459DJ
−55 to 125°C	16-Pin CerDIP	DG458AK/883
		DG459AK/883
	LCC-20	DG458AZ/883
		DG459AZ/883

*Block Diagram and Pin Configuration not shown.

Absolute Maximum Ratings

V+ to V− ..... 44 V
V+ to GND ..... 22 V
V− to GND ..... −25 V
V_{EN}, V_A Digital Input ..... (V−) −4 V to (V+) +4 V
V_S, Analog Input Overvoltage with Power On ..... (V−) −20 V to (V+) +20 V
V_S, Analog Input Overvoltage with Power Off ..... −35 V to +35 V
Continuous Current, S or D ..... 20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Storage Temperature (AK Suffix) ..... −65 to 150°C
(DJ Suffix) ..... −65 to 125°C
Power Dissipation (Package)[a]
16-Pin Plastic DIP[b] ..... 600 mW
16-Pin CerDIP[c] ..... 1000 mW
LCC-20[d] ..... 1000 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 6.3 mW/°C above 25°C.
c. Derate 12 mW/°C above 75°C.
d. Derate 10 mW/°C above 75°C.

Specifications[a]

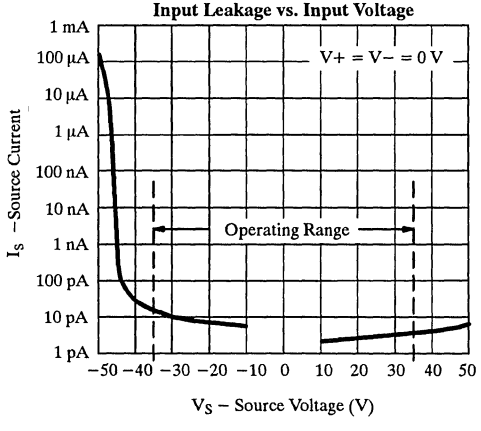
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[g]	V_{ANALOG}			Full		−10	10	−10	10	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±9.5 V, I_S = −400 µA		Room Full	0.45		1.2 1.5		1.5 1.8	kΩ
		V_D = ±5 V, I_S = −400 µA		Room	180		400		400	Ω
$r_{DS(on)}$ Matching Between Channels[h]	$\Delta r_{DS(on)}$	V_D = 0 V, I_S = −400 µA		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V V_S = ±10 V, V_D = ∓10 V		Room Full	0.03	−0.5 −50	0.5 50	−1 −20	1 20	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ±10 V V_S = ∓10 V	DG458	Room Full	0.1	−1 −200	1 200	−1 −50	1 50	
			DG459	Room Full	0.1	−1 −100	1 100	−2 −25	2 25	
Differential Off Drain Leakage Current	I_{DIFF}	DG459 Only		Room		−50	50	−20	20	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V	DG458	Room Full	0.1	−2 −200	2 200	−5 −50	5 50	
			DG459	Room Full	0.05	−2 −100	2 100	−5 −25	5 25	
Fault										
Output Leakage Current (with Overvoltage)	$I_{D(off)}$	V_S = ±33 V, V_D = 0 V See Figure 1		Room	0.02					nA
Input Leakage Current (with Overvoltage)	$I_{S(off)}$	V_S = ±25 V, V_D = ±10 V, See Figure 1		Room	0.005	−5	5	−10	10	µA
Input Leakage Current (with Power Supplies Off)		V_S = ±25 V, V_{SUPS} = 0 V V_D = A_0, A_1, A_2, EN = 0 V		Room	0.001	−2	2	−5	5	
Digital Control										
Input Low Threshold	V_{AL}			Full			0.8		0.8	V
Input Low Threshold	V_{AL}			Full		2.4		2.4		
Logic Input Control	I_A	V_A = 2.4 V or 0.8 V		Full		−1	1	−1	1	µA
Dynamic Characteristics										
Transition Time	t_A	See Figure 2		Room	200		500		500	ns
Break-Before-Make Time	t_{OPEN}	See Figure 3		Room	45	10		10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 4		Room Full	140		250 500		250 500	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room Full	50		250 500		250 500	
Settling Time	t_s	To 0.1 %		Room	0.5					µs
		To 0.01%		Room	1.5					
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 3 V_{RMS}, f = 100 kHz		Room	90					dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	5					pF
Source Off Capacitance	$C_{S(off)}$			Room	5					
Drain Off Capacitance	$C_{D(off)}$		DG458	Room	15					
			DG459	Room	10					
Drain On Capacitance	$C_{D(on)}$		DG458	Room	40					
			DG459	Room	35					

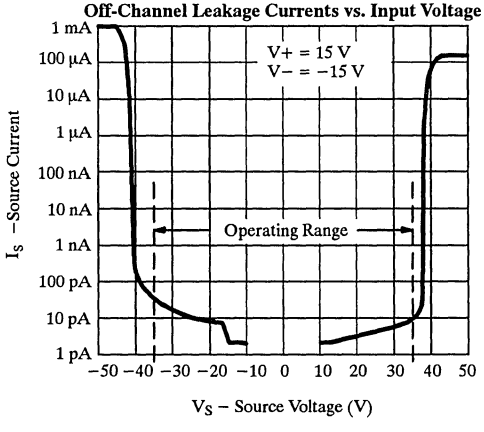
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V_{EN} = 5.0 or 0 V, V_A = 0 V	Room Full	0.05		0.1 0.2		0.1 0.2	mA
Negative Supply Current	I−		Room Full	−0.01	−0.1 −0.2		−0.1 −0.2		
Power Supply Range for Continuous Operation			Room		±4.5	±18	±4.5	±18	V

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. When the analog signal exceeds the +13.5 V or −12 V, $r_{DS(on)}$ starts to rise until only leakage currents flow.
h. $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ MAX - r_{DS(on)}\ MIN}{r_{DS(on)}\ AVE} \right) \times 100\%$

Typical Characteristics

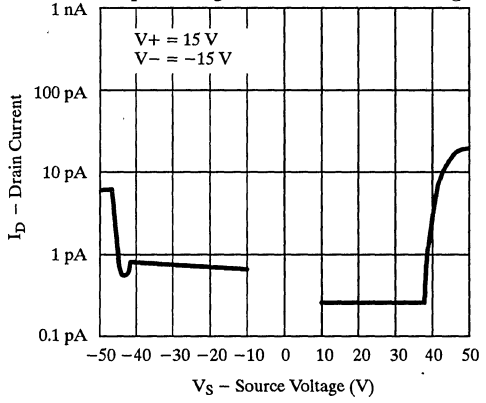




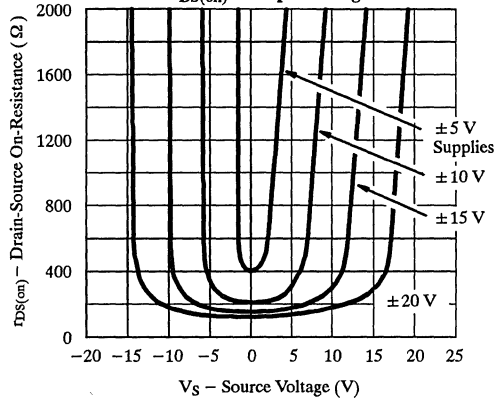
2

Typical Characteristics (Cont'd)

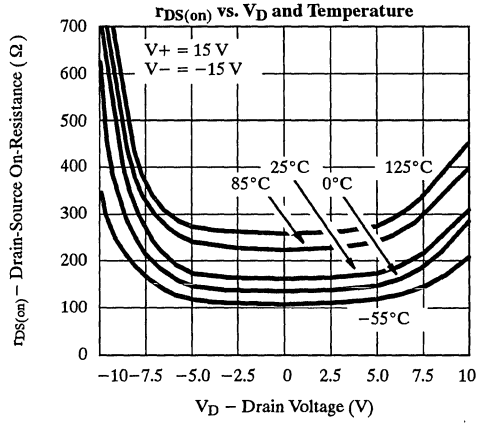
Output Leakage vs. Off-Channel Overvoltage



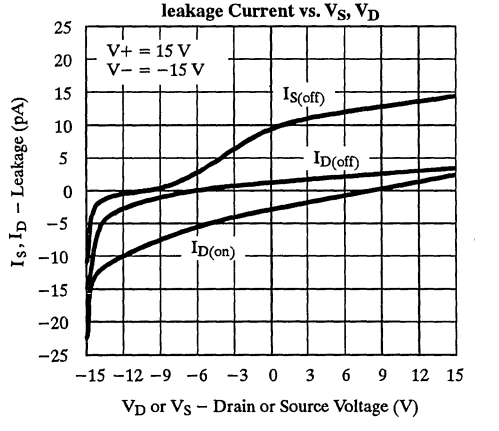
$r_{DS(on)}$ vs. Input Voltage



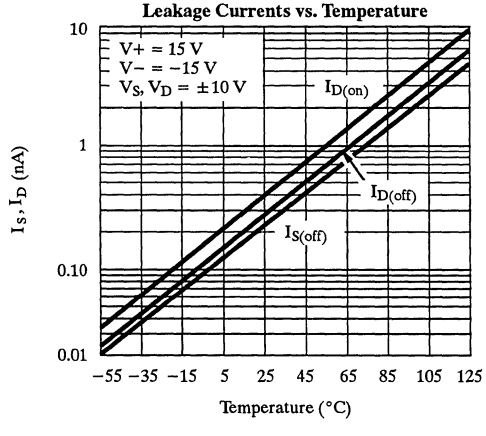
$r_{DS(on)}$ vs. V_D and Temperature



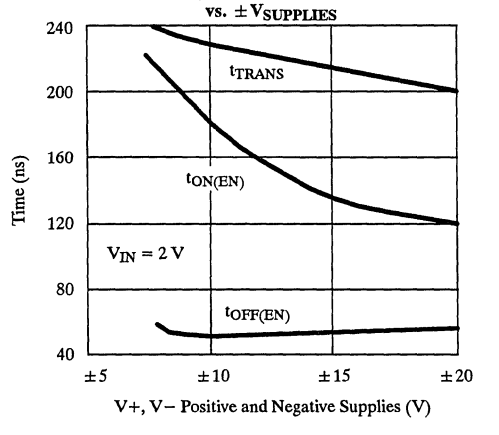
leakage Current vs. V_S, V_D



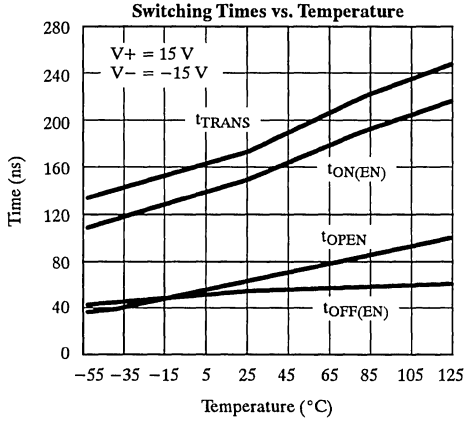
Leakage Currents vs. Temperature

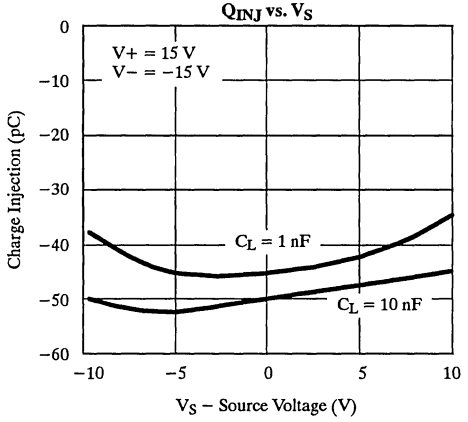


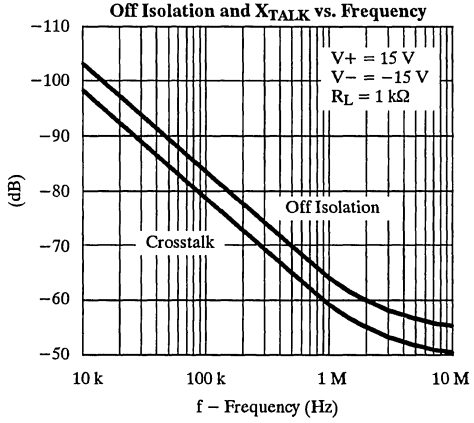
Switching Times (t_{TRANS}, t_{ON}, t_{OFF}) vs. $\pm V_{SUPPLIES}$

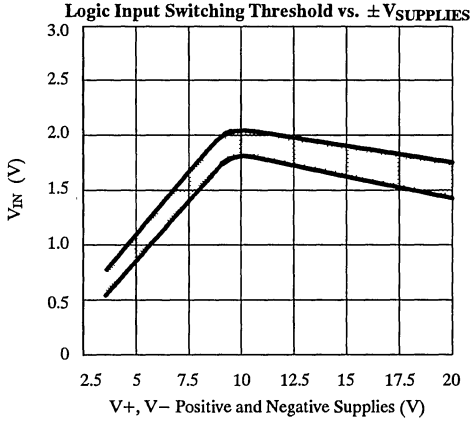


Typical Characteristics (Cont'd)









Schematic Diagram (Typical Channel)

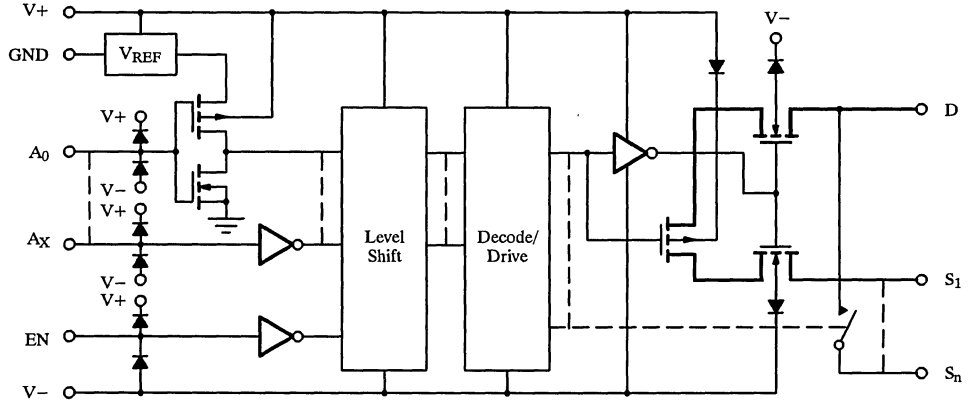


Figure 1.

Test Circuits

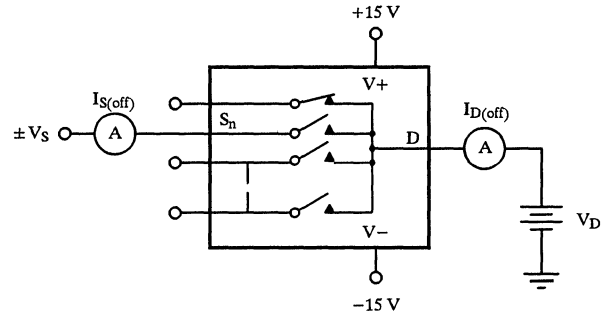


Figure 2. Analog Input Overvoltage

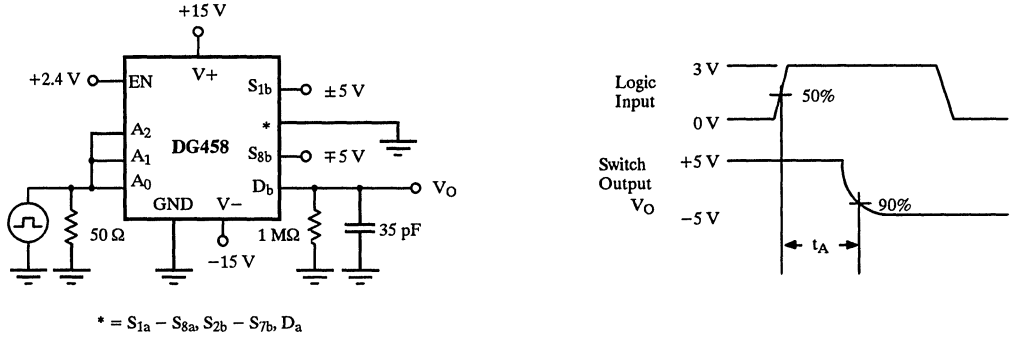


Figure 3. Transition Time

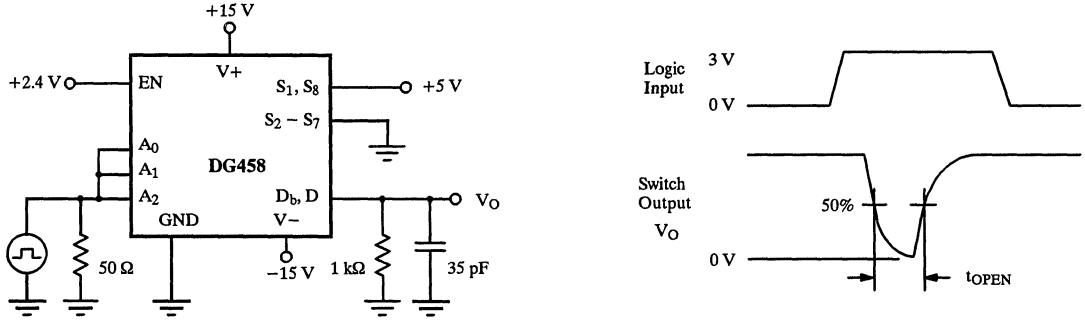


Figure 4. Break-Before-Make Time

Test Circuits (Cont'd)

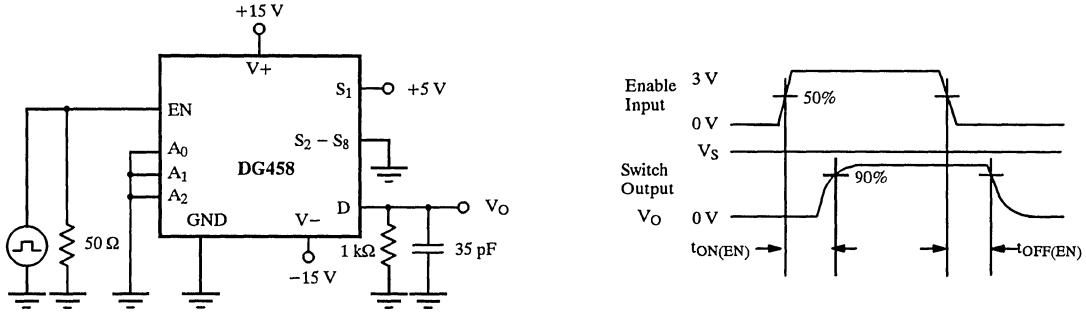


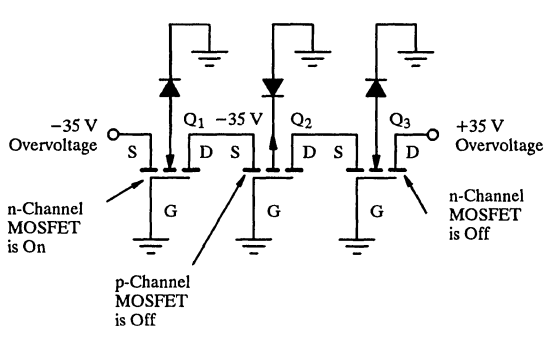
Figure 5. Enable Delay

Detailed Description

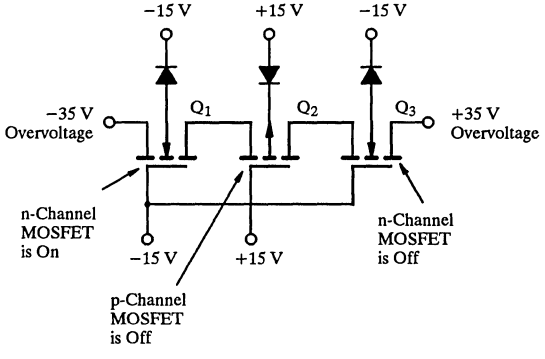
The Siliconix DG458 and DG459 multiplexers are fully fault- and overvoltage-protected for continuous input voltages up to ±35 V whether or not voltage is applied to the power supply pins (V+, V−). These multiplexers are built on a high-voltage junction-isolated silicon-gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 17).

Within the normal analog signal range (±10 V), the $r_{DS(on)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel N-MOS and P-MOS switches.

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut-off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.



(a) Overvoltage with Multiplexer Power Off



(b) Overvoltage with Multiplexer Power On

Figure 6. Overvoltage Protection

Octal Analog Switch Array

Features

- Low On-Resistance: 55 Ω
- Rail-to-Rail Analog Input Range
- Serial Interface
- Low-Power—P_D: 35 nW
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- High Speed—t_{ON}: 170 ns

Benefits

- Low Signal Distortion
- Devices Can Be Chained for System Expansion
- Reduced Board Space
- Reduced Switch Errors
- Reduced Power Supply Requirements
- Simple Interfacing

Applications

- Audio Switching and Routing
- Audio Teleconferencing
- Data Acquisition and Industrial Process Control
- Battery Powered Remote Systems
- Automotive, Avionics and ATE Systems
- Summing Amplifiers

Description

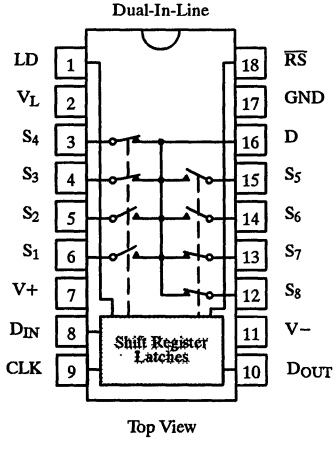
The DG485 is an analog switch array consisting of eight SPST switches connected to a common output. This device may be used as an 8-channel multiplexer in serial control applications. Any, all or none of the eight switches may be closed at any given time. Combining low on-resistance ($r_{DS(on)}$ 55 Ω, typ.) and fast switching (t_{ON}: 170 ns, typ.), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications.

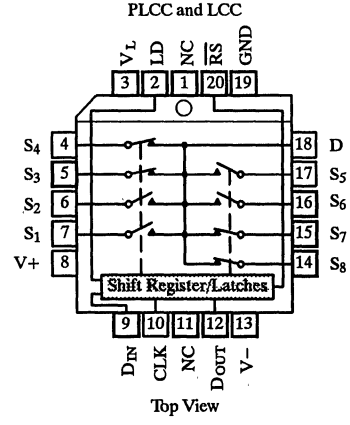
Control data is input serially into the shift register with each clock pulse. The shift register contents can be latched-in (via LD) at any point into an octal latch which in turn controls all switches. $\overline{RS}$ resets the shift register, forcing all latch inputs to a low condition (all switches off). The serial input (D_{IN}) and serial output (D_{OUT}) allow daisy chaining of multiple arrays for large systems.

Built on the Siliconix high voltage silicon gate process the DG485 has a wide 44-V power supply voltage rating. An epitaxial layer prevents latchup.

Each channel conducts equally well in either direction when on and blocks up to rail-to-rail voltages when off.

Functional Block Diagrams and Pin Configurations





Truth Tables and Ordering Information

$\overline{RS}$	CLK*	D_{IN}	D_1	D_n
1	↑	0	0	D_{n-1}
1	↑	1	1	D_{n-1}
1	↓	X	D_1	D_n (No Change)
0	X	X	0	0

*CLK Input Edge Triggered

LD*	D_n	L_n	SW_n
↑	0	0	OFF
↑	1	1	ON
↓	D_n	L_n	(No Change)

*LD Input Level Triggered

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	18-Pin Plastic DIP	DG485DJ
	20-Pin PLCC	DG485DN
−55 to 125°C	LCC-20	DG485AZ/883

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) + 2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature (AZ Suffix) ..... −65 to 150°C
(DJ, DN Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
18-Pin Plastic DIP[c] ..... 470 mW
20-Pin PLCC, LCC[d] ..... 800 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 10 mW/°C above 75°C.

2

Specifications[a]

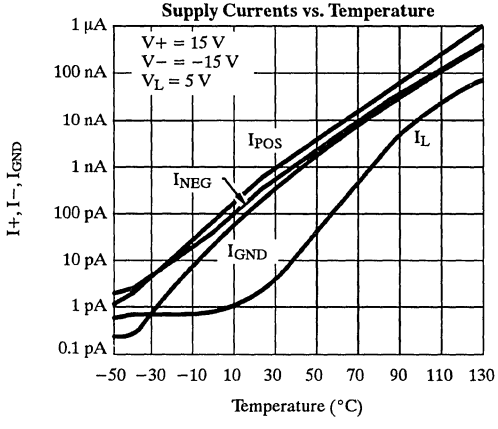
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 13.5 V, V− = −13.5 V I_S = −5 mA, V_D = ±10 V	Room Full	55		85 125		85 125	Ω
Delta Drain-Source On-Resistance[g]	$\Delta r_{DS(on)}$		Room	6					%
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V− = −16.5 V V_D = ∓15.5 V, V_S = ±15.5 V	Room Full	0.01	−1 −20	1 20	−1 −10	1 10	nA
	$I_{D(off)}$		Room Full	0.1	−10 −200	10 200	−10 −50	10 50	
Channel On Leakage Current	$I_{D(on)}$	V± = ±16.5 V V_S = V_D = ±15.5 V One Switch At A Time	Room Full	0.11	−20 −500	20 500	−20 −50	20 50	
		V± = ±16.5 V, V_S = V_D = ±15.5 V All Switches On	Room	0.2					
Input									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	Room Full	−0.0001	−1 −5	1 5	−1 −5	1 5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	Room Full	0.0001	−1 −5	1 5	−1 −5	1 5	
Serial Data Output									
Output Voltage with V_{IN} Low − D_{OUT}	V_{OL}	I_O = 1.6 mA, V+ = 4.5 V	Full	0.25		0.4		0.4	V
Output Voltage with V_{IN} High − D_{OUT}	V_{OH}	I_O = −80 µA, V+ = 16.5 V V_L = 4.75 V	Full	4.4	2.7		2.7		
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = ±10 V See Figures 1, 8	Room Full	170		200 275		200 275	ns
Turn-Off Time	t_{OFF}	V_S = ±10 V See Figures 2, 3, 8	Room Full	150		200 275		200 276	
Data Setup Time	t_{DS}	See Figures 4, 8	Room Full		40 60		40 60		
Data Hold Time	t_{DH}		Room Full		40 60		40 60		
LOAD Hold Time	t_{LH}	See Figures 5, 8	Room Full		100 150		100 150		
$\overline{RESET}$ Hold Time	t_{RH}		Room Full		100 150		100 150		
$\overline{RESET}$ ↑ to $\overline{CLOCK}$ ↑ Delay	t_{DRC}		Room Full		40 60		40 60		
Charge Injection	Q	V_S = 0 V, C_L = 1,000 pF Any One Channel	Room	17					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz See Figure 9	Room	−75					dB

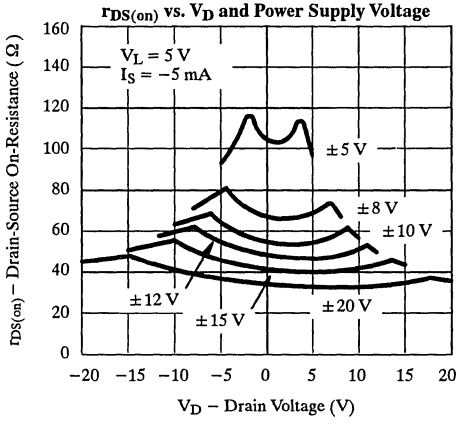
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Maximum Clock Frequency	f_{CLK}		Room	10					MHz
Source Off Capacitance[e]	$C_{S(off)}$	V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz	Room	7					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	43					
On-State Capacitance[e]	$C_{D(on)}$	V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz One Channel On	Room	53					
		V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz All Channels On	Room	122					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V, V_L = 5.25 V D_{OUT} Open	Room Full	0.001		3 10		3 10	µA
Negative Supply Current	I−		Room Full	−0.001	−3 −10		−3 −10		
Logic Supply Current	I_L		Room Full	0.001		3 10		3 10	
Ground Current	I_{GND}		Room Full	−0.001	−3 −10		−3 −10		

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. For each V_D: $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ \text{MAX} - r_{DS(on)}\ \text{MIN}}{r_{DS(on)}\ \text{AVE}} \right)$

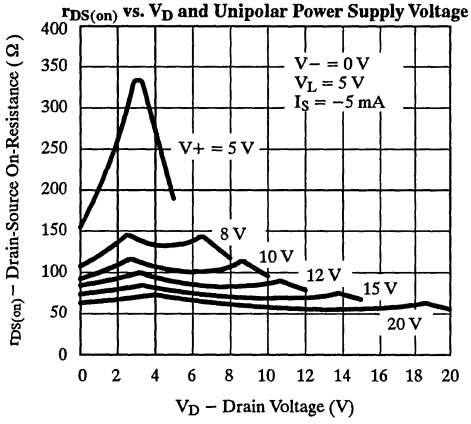
Typical Characteristics

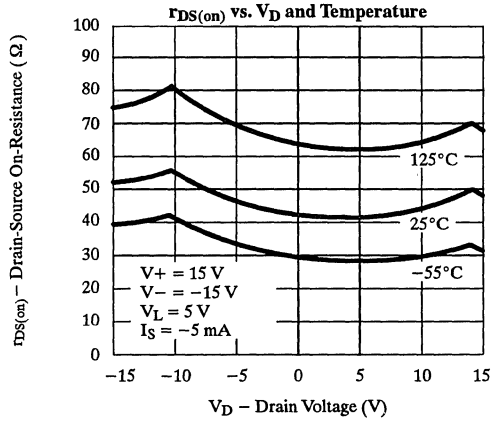


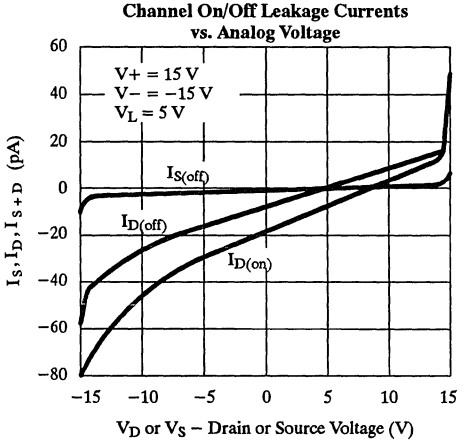


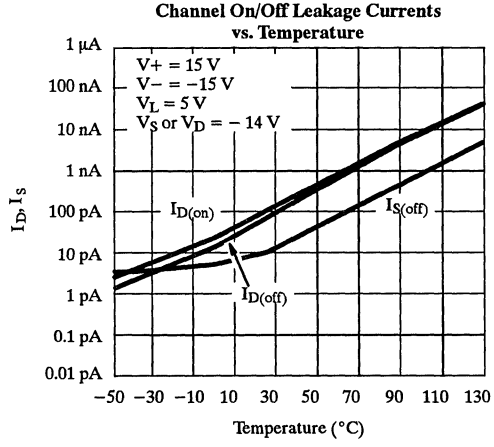
2

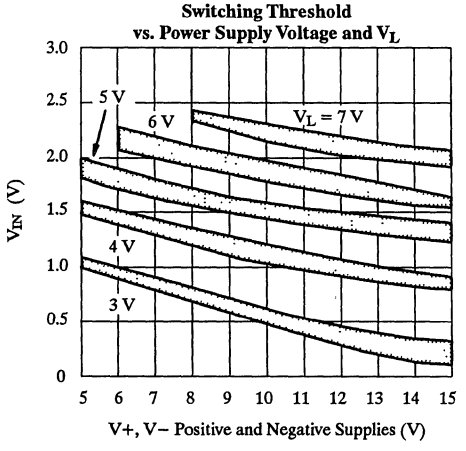
Typical Characteristics (Cont'd)

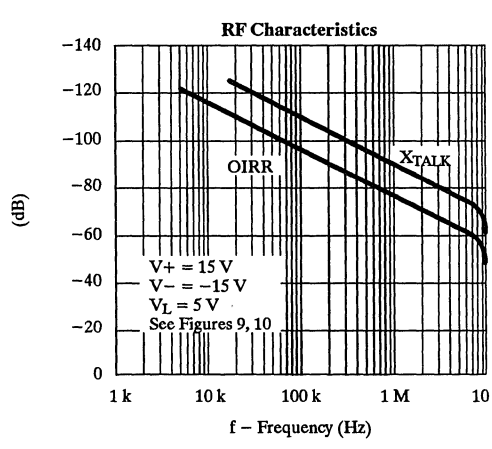




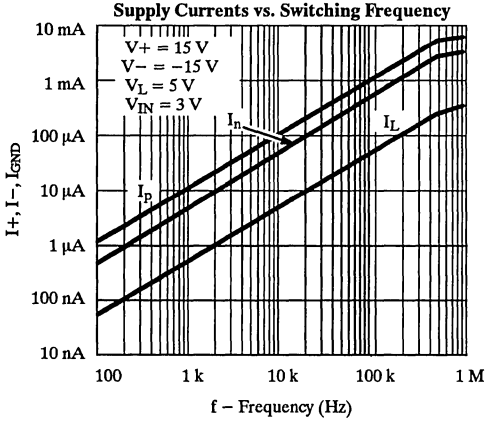


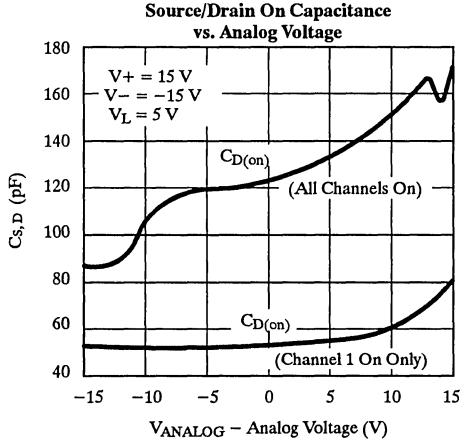


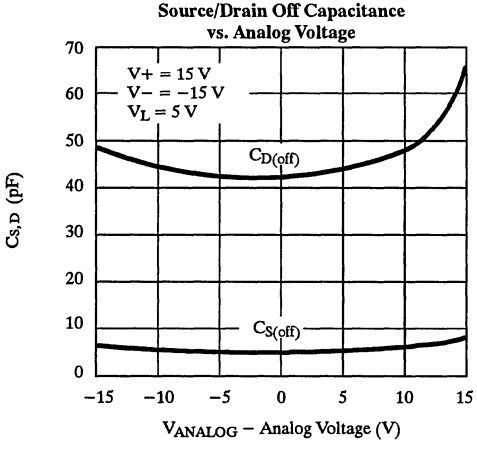


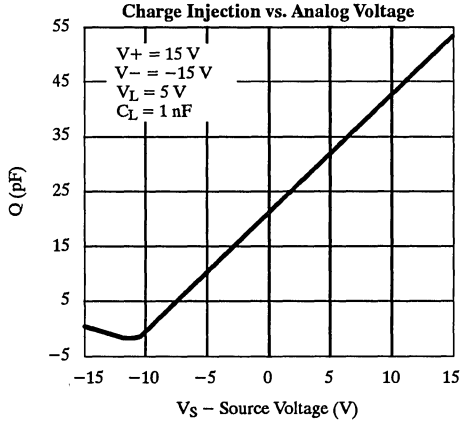


Typical Characteristics (Cont'd)









Timing Diagrams

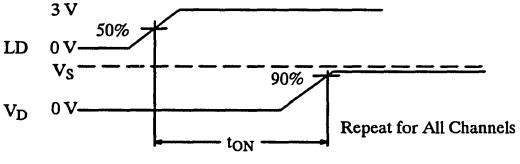


Figure 1. t_{ON} from LD

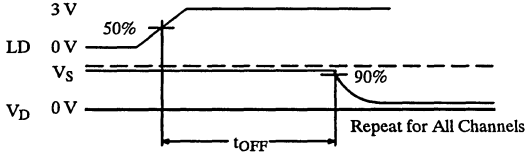


Figure 2. t_{OFF} from LD

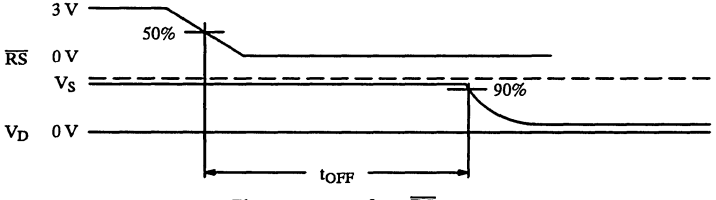


Figure 3. t_{OFF} from $\overline{RS}$

Timing Diagrams (Cont'd)

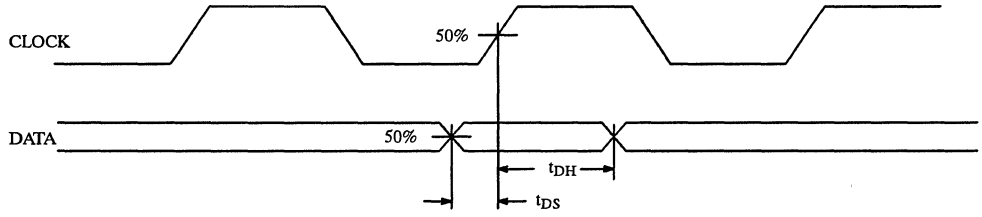


Figure 4. Data Setup and Hold Time

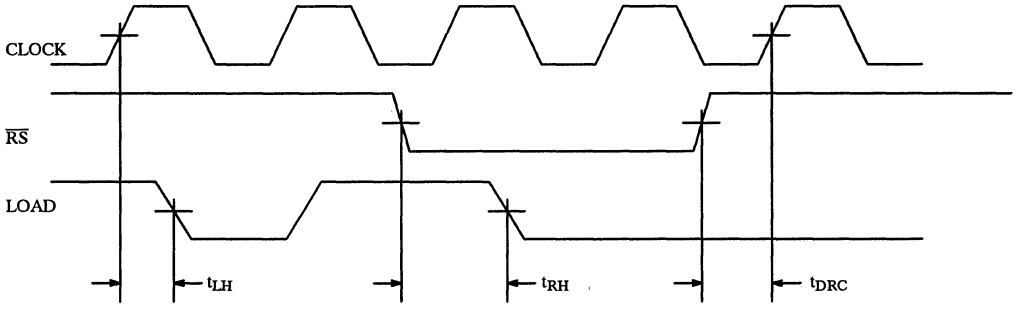
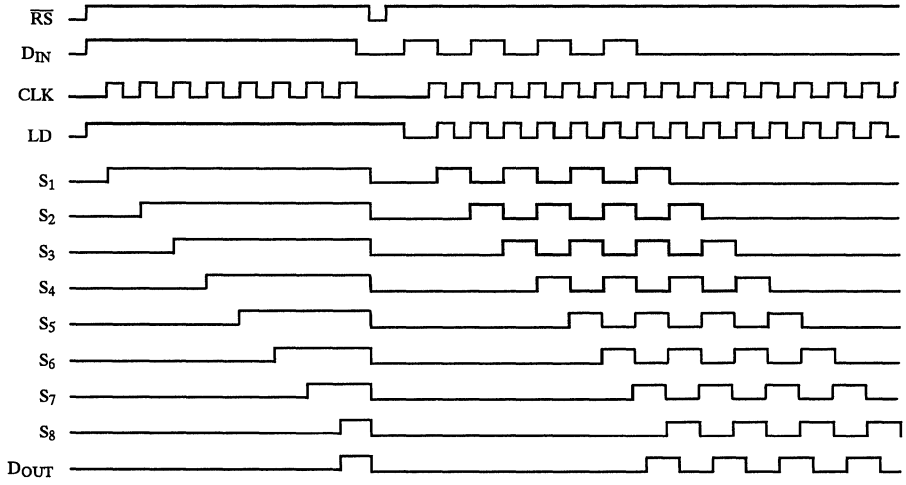


Figure 5. Timing Relationships



$S_1 - S_8$ and D_{OUT} are expected output with the drain connected high. The sources require pull-down of 1 kΩ

Figure 6.

Schematic Diagram (Typical Channel)

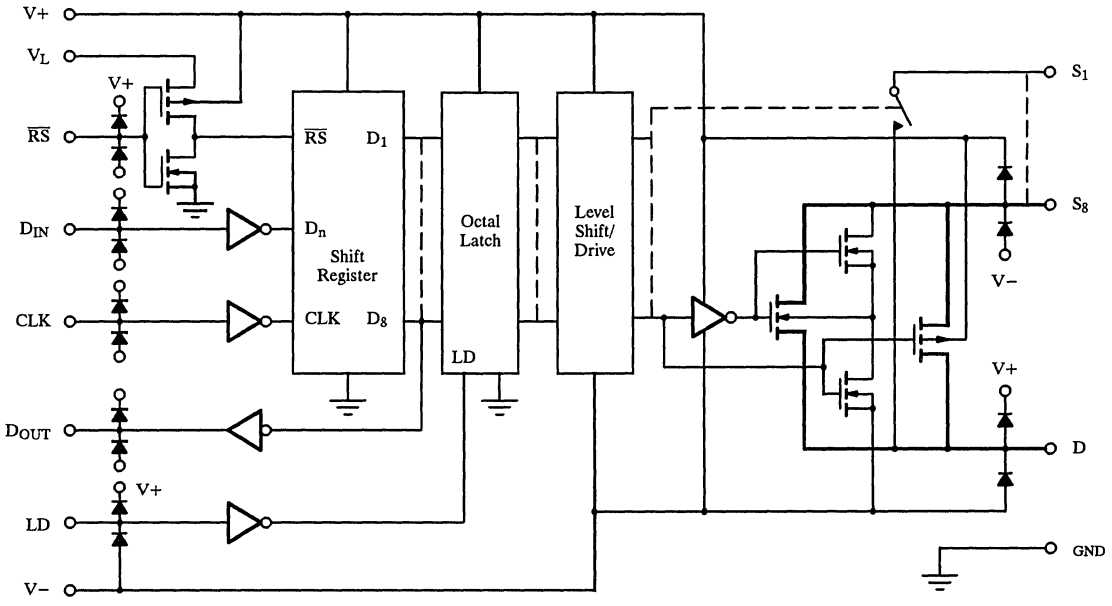


Figure 7.

Test Circuits

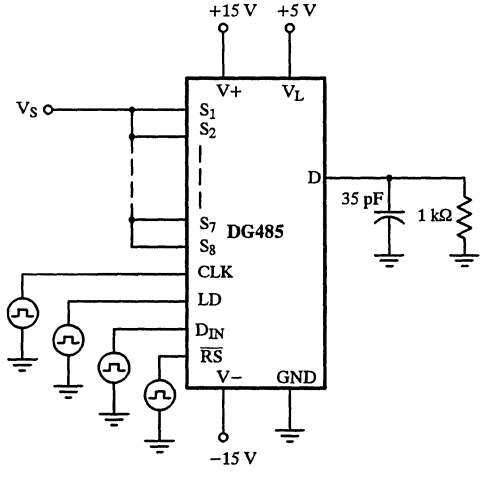


Figure 8. Switching Time Test Circuit

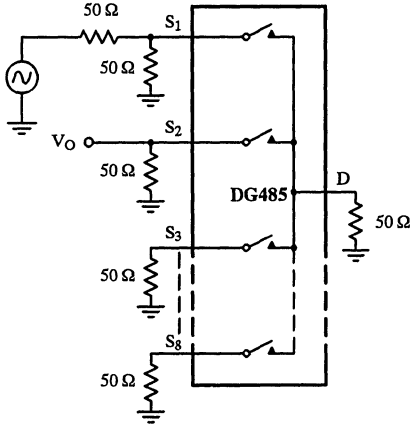


Figure 9. Adjacent Input Crosstalk

2

Test Circuits

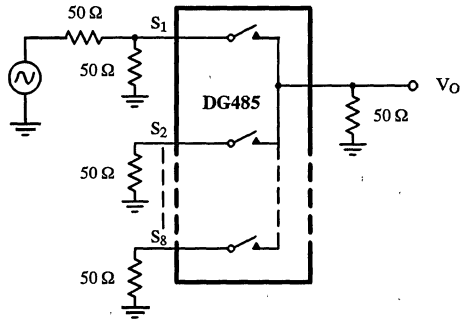
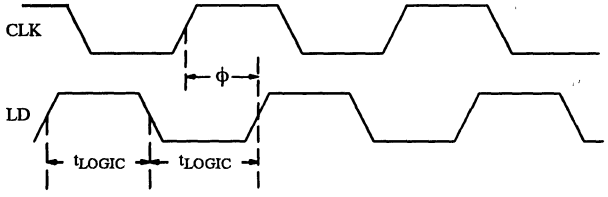


Figure 10. Off Isolation

Applications



ϕ= for CLK and LD inputs of the same frequency. The recommended phase delay of LD from CLK is ½ t_{LOGIC} to t_{LOGIC}:

$t_{LOGIC(MIN)}$: 80 ns at 25°C
150 ns at 125°C

V+ = 15 V
V− = −15 V
GND = 0 V

Figure 11.

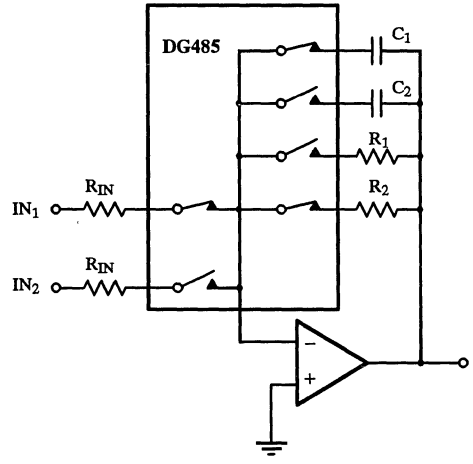


Figure 12. Multi-Function Circuit Provides Input Selection, Gain Ranging and Filtering with One DG485

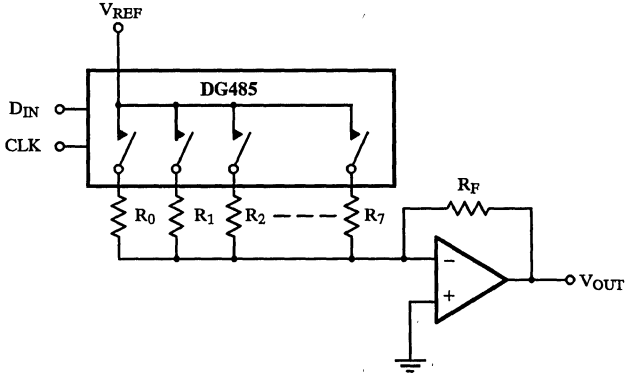


Figure 13. Serial DAC Circuit

Applications (Cont'd)

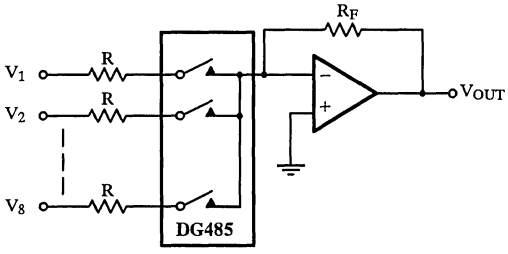


Figure 14. Summing Node Mixer

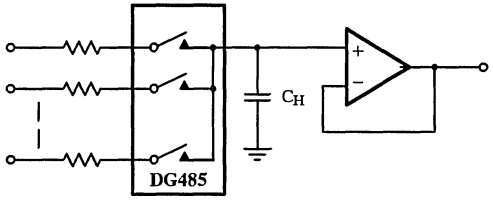


Figure 15. Multiplexing, Sampling Application

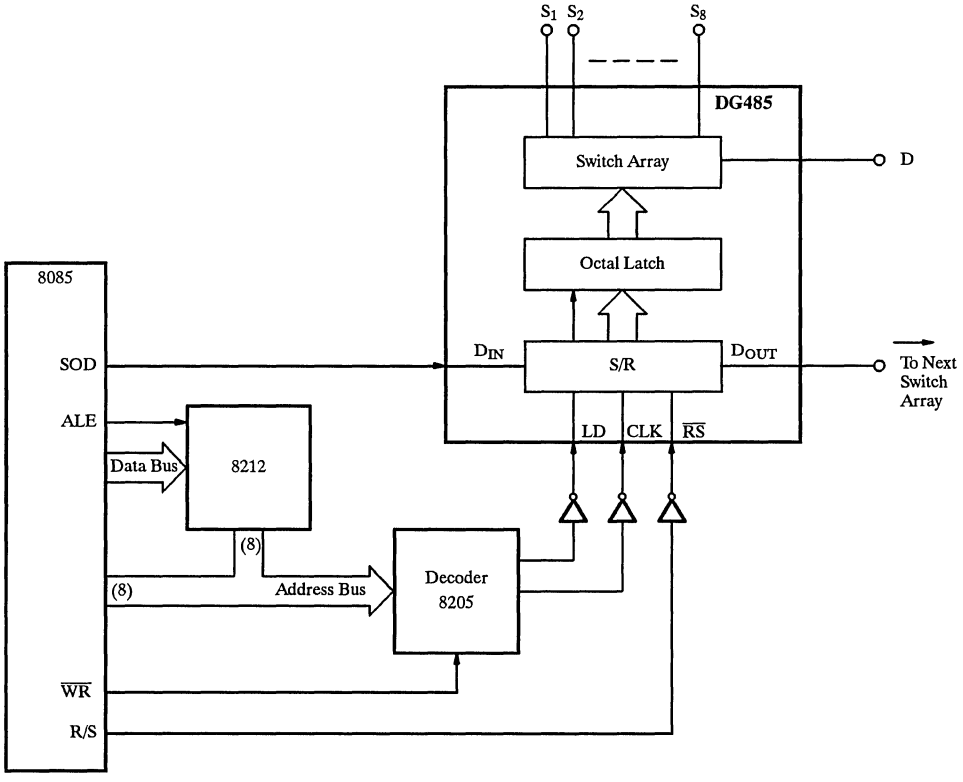


Figure 16. Direct Serial Interface (8085)

Siliconix
A Member of the TEMIC Group

Single 16-Channel/Differential 8-Channel CMOS Analog Multiplexers

Features

- Low On-Resistance: 240 Ω
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

Benefits

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

Applications

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

Description

The DG506A, a 16-channel single-ended analog multiplexer, is designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address (A_0, A_1, A_2, A_3). The DG507A, a differential 8-channel analog multiplexer, is designed to connect one of eight differential inputs to a common differential outputs as determined by its 3-bit binary address (A_0, A_1, A_2) logic. Break-before-make switching action protects against momentary shorting of the input signals.

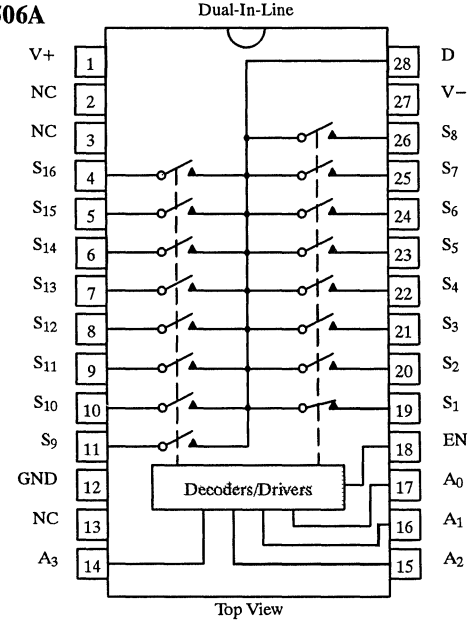
A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

The DG506A/507A are fabricated in the Siliconix PLUS-40 process, which includes improved ESD protection for ruggedness. An epitaxial layer prevents latch up.

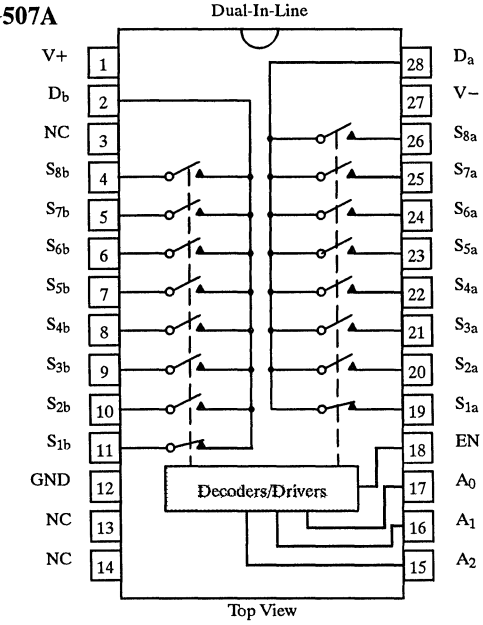
For wideband/video multiplexing, the DG536 is recommended.

Functional Block Diagrams and Pin Configurations

DG506A



DG507A



Functional Block Diagrams and Pin Configurations

Truth Table — DG506A

A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table — DG507A

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information — DG506A

Temp Range	Package	Part Number
0 to 70°C	28-Pin Plastic DIP	DG506ACJ
	28-Pin CerDIP	DG506ACK
−25 to 85°C		DG506ABK
−40 to 85°C	28-Pin PLCC	DG506ADN
−55 to 125°C	28-Pin CerDIP	DG506AAK
		DG506AAK/883
	28-Pin Sidebraze	JM38510/19001BXC
	LCC-20*	DG506AAZ/883

Ordering Information — DG507A

Temp Range	Package	Part Number
0 to 70°C	28-Pin Plastic DIP	DG507ACJ
−55 to 125°C	28-Pin CerDIP	DG507AAK
		DG507AAK/883
	28-Pin Sidebraze	JM38510/19003BXC
	28-Pin LCC	DG507AAZ/883

*Block Diagram and Pin Configuration not shown.

Absolute Maximum Ratings

Voltage Referenced to V−

V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Storage Temperature (CerDIP) ..... −65 to 150°C
(Plastic DIP) ..... −65 to 125°C

Power Dissipation (Package)[b]
28-Pin Plastic DIP[c] ..... 625 mW
28-Pin CerDIP and Sidebraze ..... 1200 mW
28-Pin PLCC[c] ..... 1200 mW
LCC-20,28[d] ..... 1000 mW

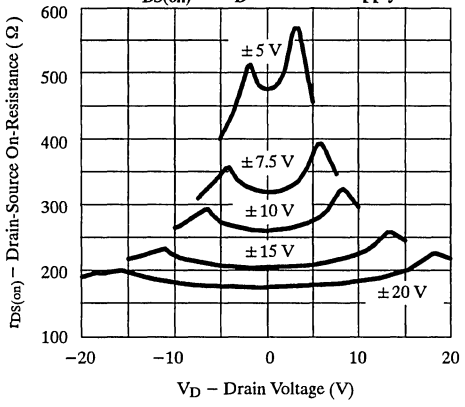
Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 8.3 mW/°C above 75°C.
d. Derate 14 mW/°C above 75°C.

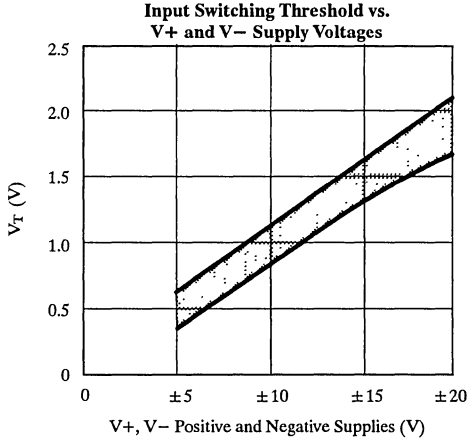
Specifications[a]

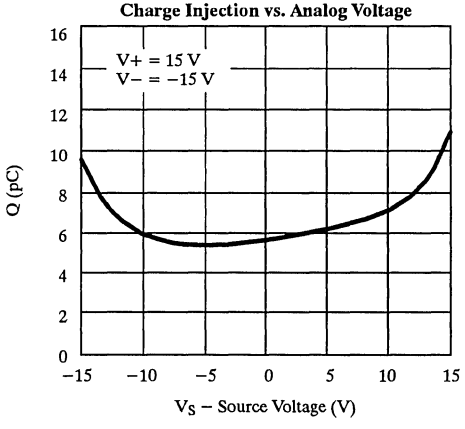
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix 0 to 70°C, −25 to 85°C, −40 to 85°C Min[d]	B, C, D Suffix 0 to 70°C, −25 to 85°C, −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −200 µA		Room Full	240		400 500		450 550	Ω
$r_{DS(on)}$ Matching[g]	$\Delta r_{DS(on)}$	−10 V < V_S < 10 V		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V_{EN} = 0 V		Room Full		−1 −50	1 50	−5 −50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ∓10 V V_S = ±10 V V_{EN} = 0 V	DG506A	Room Full		−10 −300	10 300	−20 −300	20 300	
			DG507A	Room Full		−5 −200	5 200	−10 −200	10 200	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V	DG506A	Room Full		−10 −300	10 300	−20 −300	20 300	
			DG507A	Room Full		−5 −200	5 200	−10 −200	10 200	
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Room Full		−10 −30		−10 −30		µA
		V_A = 15 V		Room Full			10 30		10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Full		−10 −30		−10 −30		
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Room	0.6		1			µs
Break-Before-Make Time	t_{OPEN}	See Figure 4		Room	0.2					
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room	1					
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	0.4					
Charge Injection	Q			Room	6					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room	68					dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 140 kHz		Room	6					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 140 kHz	DG506A	Room	45					
			DG507A	Room	23					
Power Supplies										
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0 V		Room	1.3		2.4		2.4	mA
Negative Supply Current	I−			Room	−0.7	−1.5		−1.5		

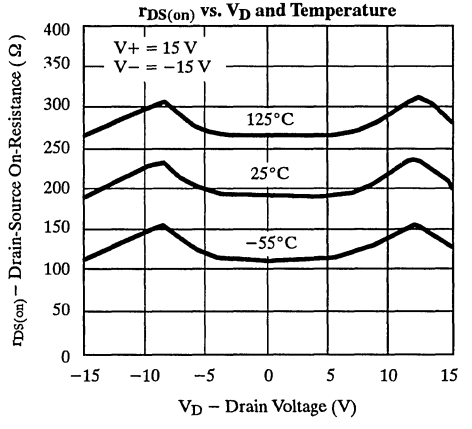
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}MAX - r_{DS(on)}MIN}{r_{DS(on)}AVE} \right)$
h. Off isolation = 20 log $\frac{V_D}{V_S}$, V_S = input to off switch, V_D = output due to V_S.

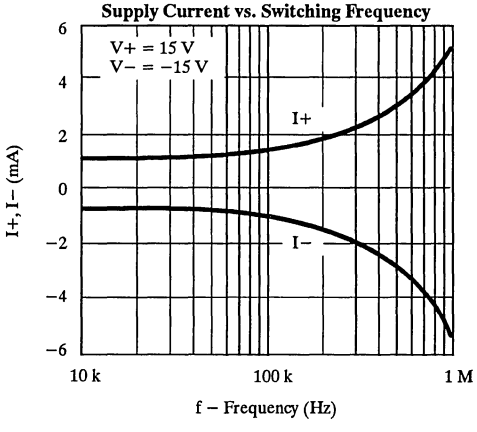
Typical Characteristics

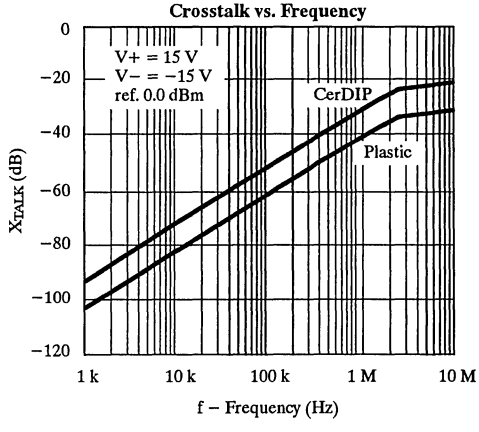








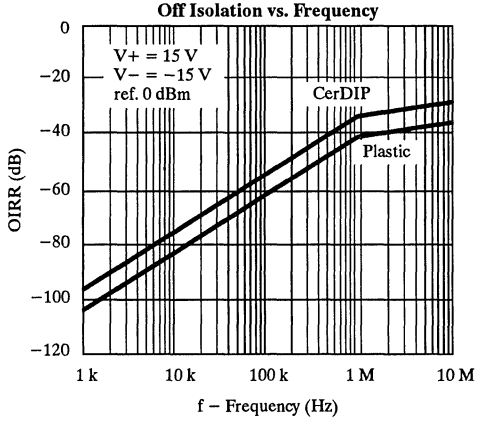




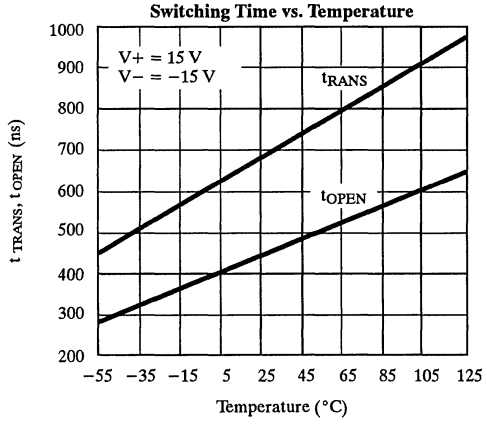
2

Typical Characteristics (Cont'd)

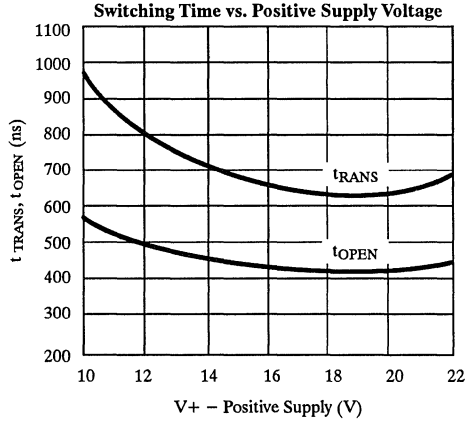
Off Isolation vs. Frequency



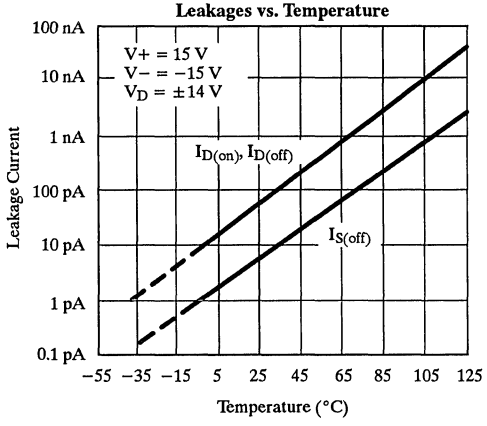
Switching Time vs. Temperature



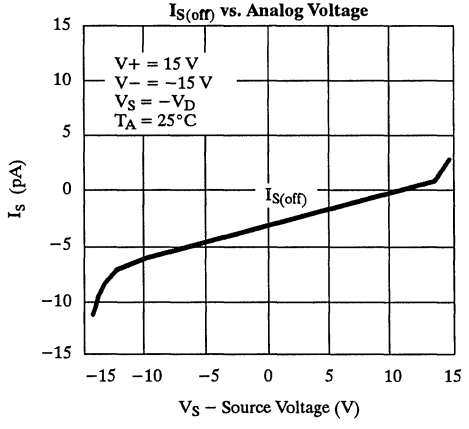
Switching Time vs. Positive Supply Voltage



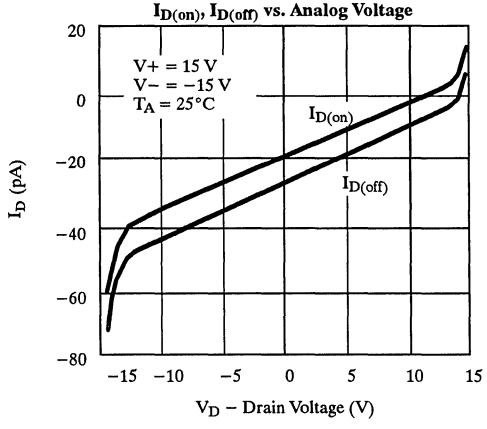
Leakages vs. Temperature



$I_{S(off)}$ vs. Analog Voltage



$I_{D(on)}$, $I_{D(off)}$ vs. Analog Voltage



Schematic Diagram (Typical Channel)

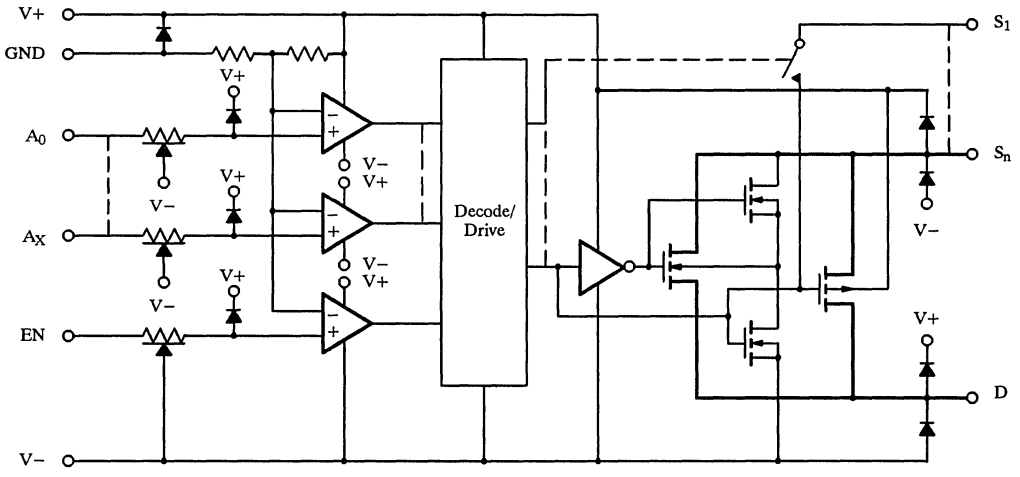
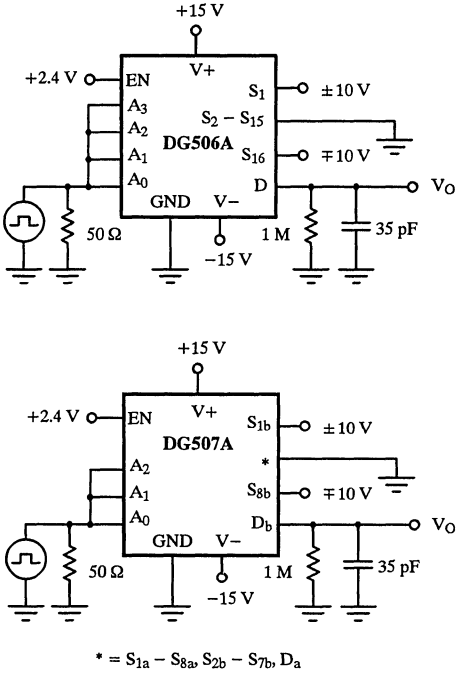


Figure 1.

Test Circuits



* = $S_{1a} - S_{8a}$, $S_{2b} - S_{7b}$, D_a

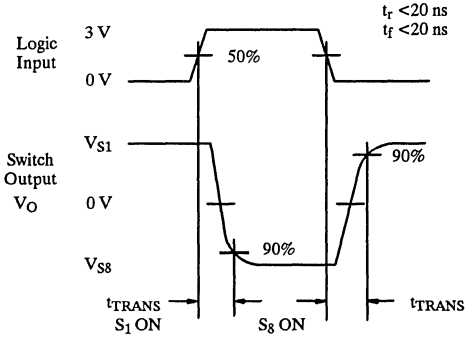


Figure 2. Transition Time

Test Circuits (Cont'd)

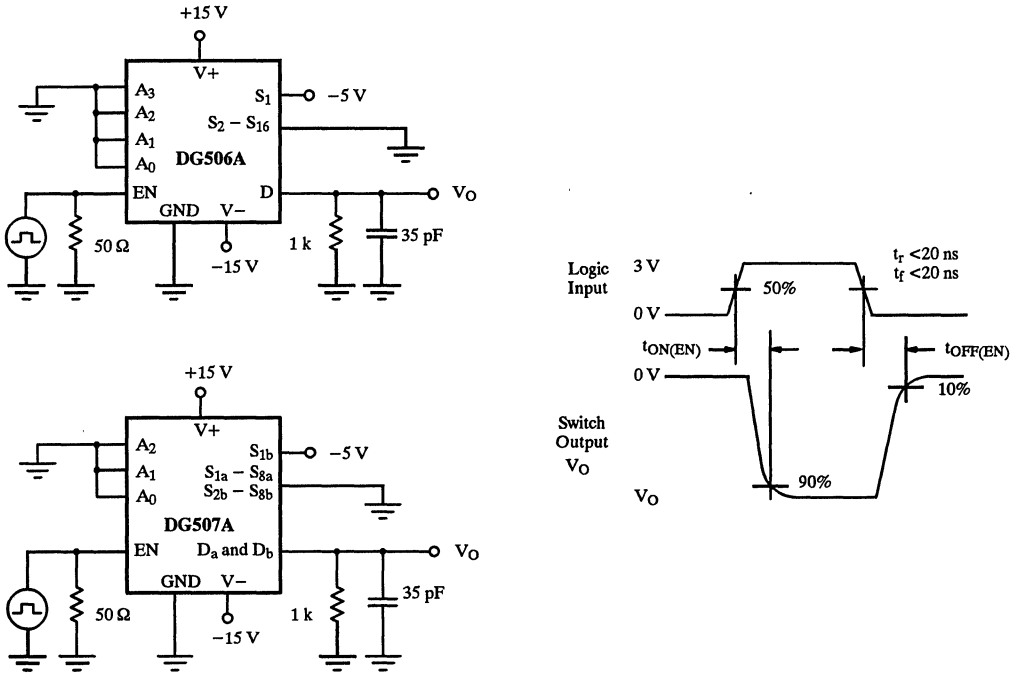


Figure 3. Enable Switching Time

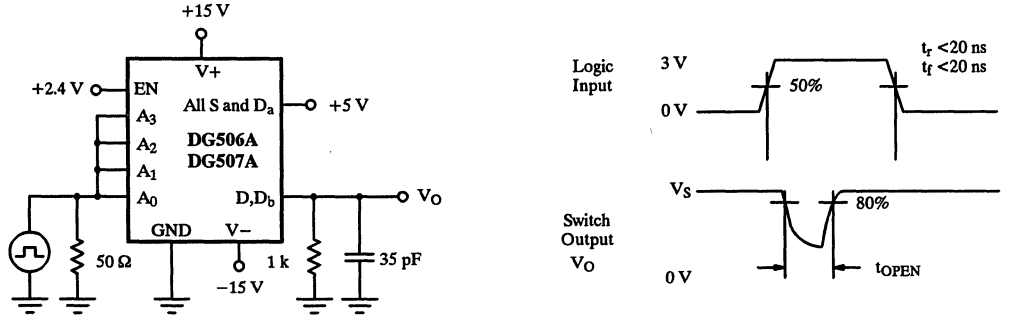


Figure 4. Break-Before-Make Interval

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15[b]	−15	2.4/0.8	−15 to 15
12	−12	2.4/0.8	−12 to 12
10	−10	2.2/0.6	−10 to 10
8[c]	−8	2.0/0.5	−8 to 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V− = −15 V.
c. Operation below ±8 V is not recommended due to shift in $V_{INL(MAX)}$.

Applications

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 5). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V− value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V− rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V−, but it preserves the low channel resistance and low leakage characteristics.

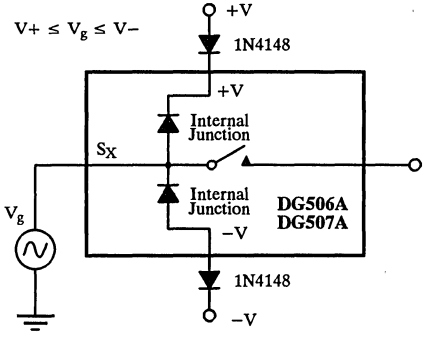


Figure 5. Overvoltage Protection Using Blocking Diodes

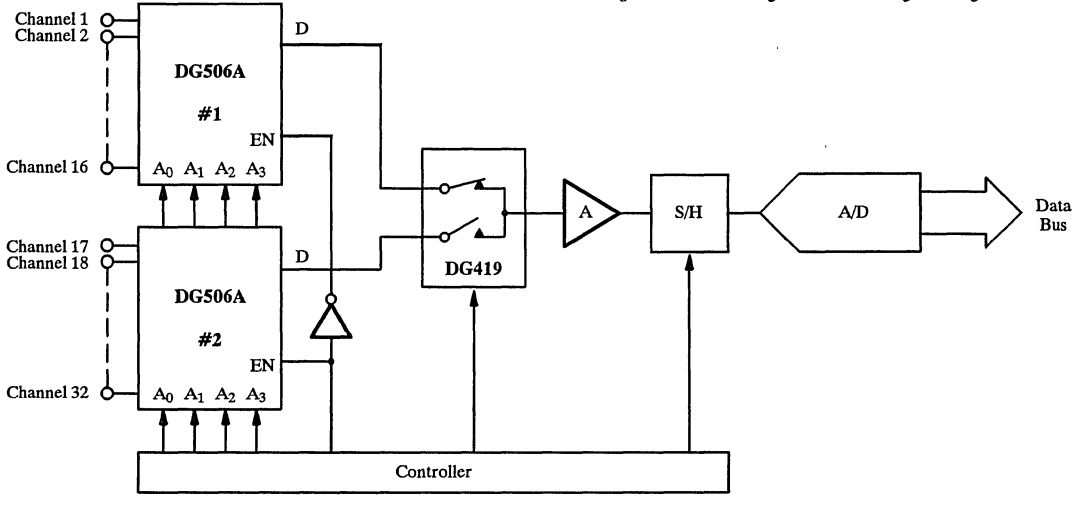


Figure 6. A 32-Channel Data Acquisition System

Siliconix
A Member of the TEMIC Group

Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers

Features

- Low On-Resistance: 240 Ω
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

Benefits

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

Applications

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

Description

The DG508A, an 8-channel single-ended analog multiplexer, is designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2).

The DG509A, a dual 4-channel analog multiplexer, is designed to connect one of four differential inputs to a common output as determined by its 2-bit binary address (A_0, A_1) logic. Break-before-make switching action protects against momentary shorting of the input signals.

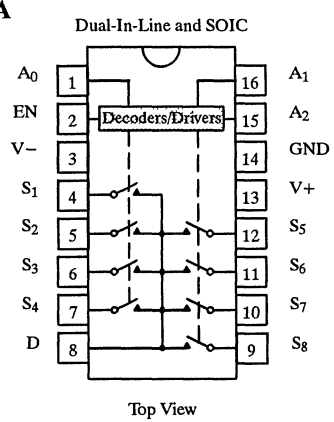
A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

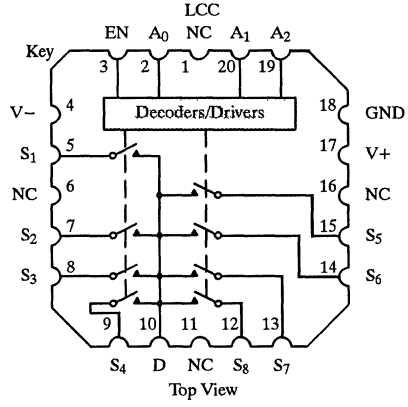
Fabricated in the Siliconix Plus-40 process, the absolute maximum voltage rating is extended to 44 V, allowing increased operating headroom for standard ±15-V signal swings and operation with ±20-V supplies. An epitaxial layer prevents latch up.

For applications requiring address data latching, the DG528/529 is recommended. DG408/409 is recommended for higher precision applications. For wideband/video routing and multiplexing, the DG538A is recommended.

Functional Block Diagrams and Pin Configurations

DG508A





Functional Block Diagrams and Pin Configurations (Cont'd)

Ordering Information – DG508A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG508ACJ
−25 to 85°C	16-Pin CerDIP	DG508ABK
−40 to 85°C	16-Pin Narrow SOIC	DG508ADY
−55 to 125°C	16-Pin CerDIP	DG508AAK
		DG508AAK/883
	LCC-20	DG508AAZ/883
	16-Pin Sidebraze	7705201EA
		7705201EC
	16-Pin Flat Pack	7705201FA
		7705201FC
	16-Pin Sidebraze	JM38510/19007BEA
		JM38510/19007BEC

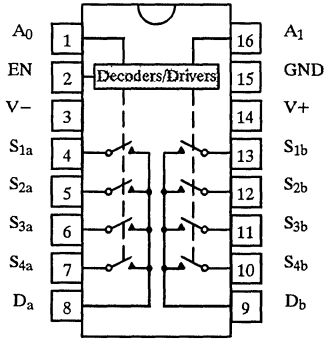
Truth Table — DG508A

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

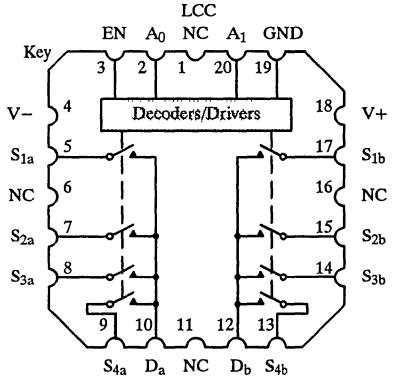
DG509A

Dual-In-Line and SOIC



Top View

LCC



Top View

Ordering Information – DG509A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG509ACJ
−25 to 85°C	16-Pin CerDIP	DG509ABK
−40 to 85°C	16-Pin Narrow SOIC	DG509ADY
−55 to 125°C	16-Pin CerDIP	DG509AAK
		DG509AAK/883
	LCC-20	DG509AAZ/883
	16-Pin Sidebraze	JM38510/19008BEA
		JM38510/19008BEC

Truth Table — DG509A

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Absolute Maximum Ratings

Voltage Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Storage Temperature (K Suffix) ..... −65 to 150°C
(J and Y Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[c] ..... 600 mW
16-Pin CerDIP[d] ..... 900 mW
LCC-20[d] ..... 900 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6.3 mW/°C above 75°C.
d. Derate 12 mW/°C above 75°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −200 µA		Room Full	240		400 500		450 550	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$	−10 V < V_S < 10 V		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_S = ±10 V V_D = ∓10 V		Room Full		−1 −50	1 50	−5 −50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ±10 V V_S = ∓10 V	DG508A	Room Full		−10 −200	10 200	−20 −200	20 200	
			DG509A	Room Full		−10 −100	10 100	−20 −100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V	DG508A	Room Full		−10 −200	10 200	−20 −200	20 200	
			DG509A	Room Full		−10 −100	10 100	−20 −100	20 100	
Digital Control										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V		Room Full	−0.002	−10 −30		−10 −30		µA
		V_A = 15 V		Room Full	0.006		10 30		10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Full	−0.002	−10 −30		−10 −30		
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Room	0.6		1			µs
Break-Before-Make Time	t_{OPEN}	See Figure 4		Room	0.2					
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room	1		1.5			
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	0.4		1.0			
Charge Injection	Q	See Figure 5		Room	6					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room	68					dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 140 kHz		Room	6					
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 140 kHz	DG508A	Room	25					
			DG509A	Room	12					

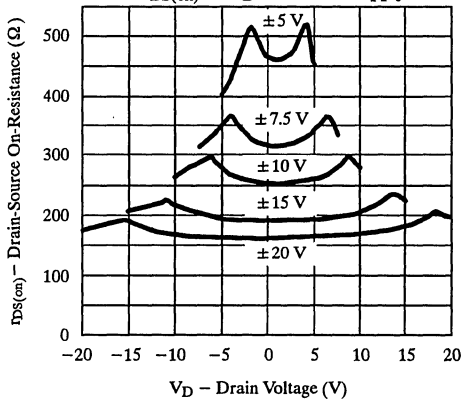
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V_{EN} = 0 V or 2.4 V	Room	1.3		2.4		2.4	mA
Negative Supply Current	I−		Room	−0.7	−1.5		−1.5		

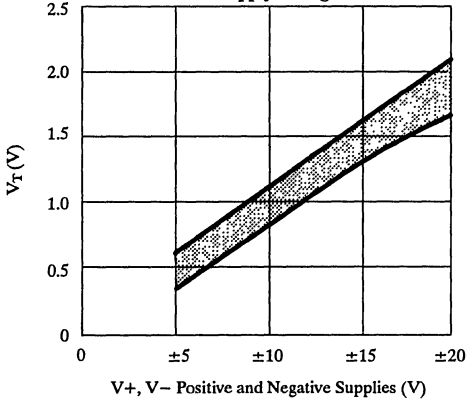
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

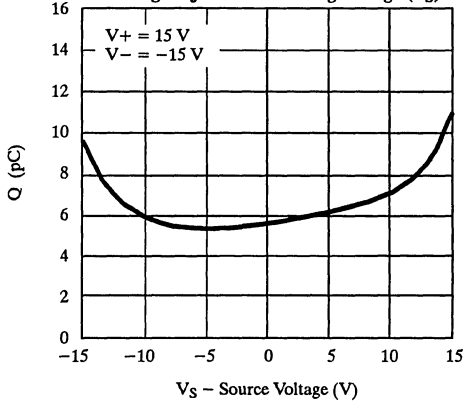
$r_{DS(on)}$ vs. V_D and Power Supply



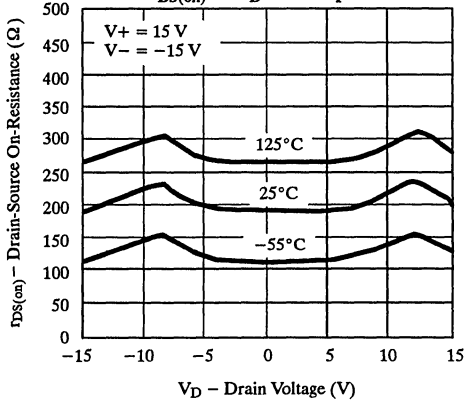
Input Switching Threshold vs. V+ and V− Supply Voltages



Charge Injection vs. Analog Voltage (V_S)



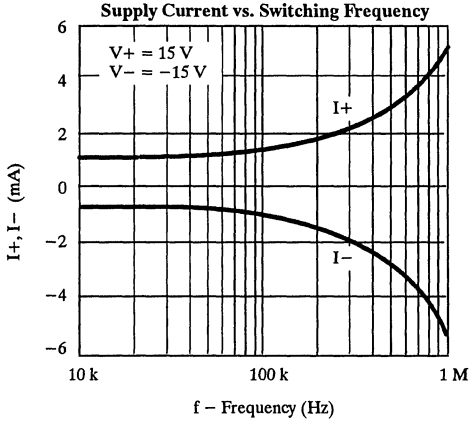
$r_{DS(on)}$ vs. V_D and Temperature



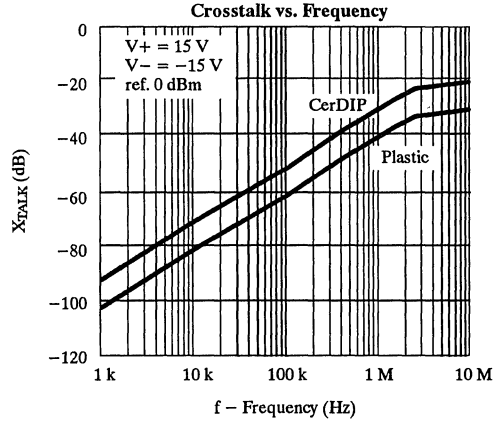
2

Typical Characteristics (Cont'd)

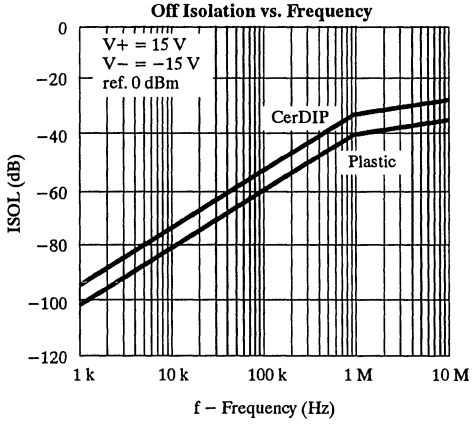
Supply Current vs. Switching Frequency



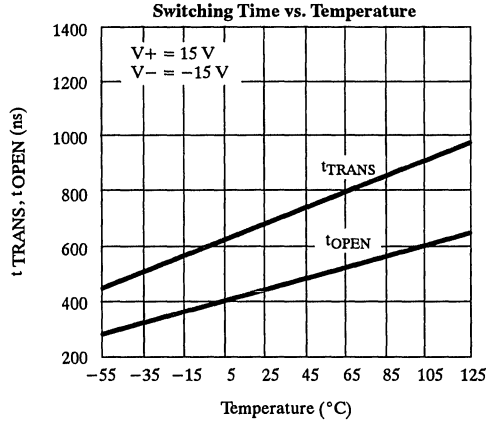
Crosstalk vs. Frequency



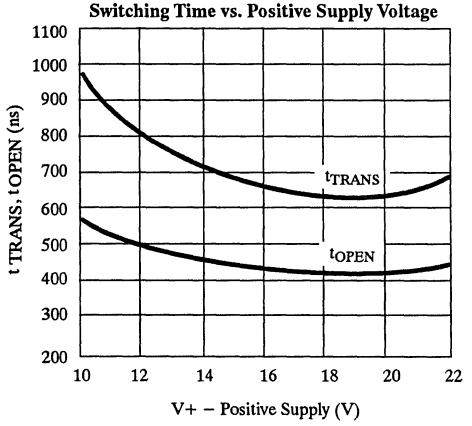
Off Isolation vs. Frequency



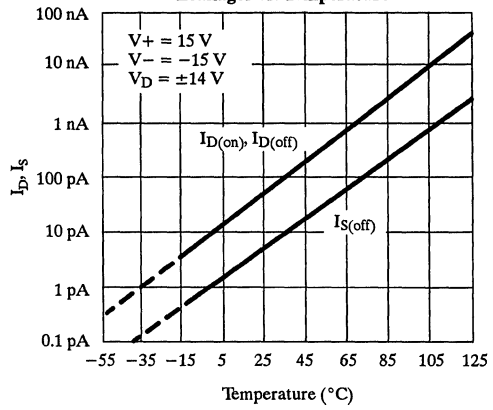
Switching Time vs. Temperature



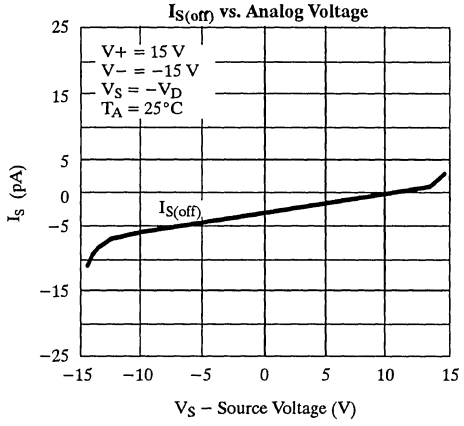
Switching Time vs. Positive Supply Voltage

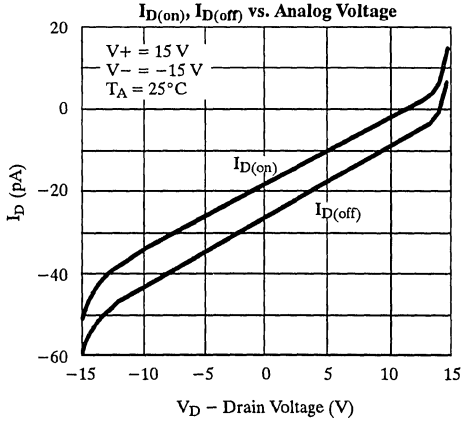


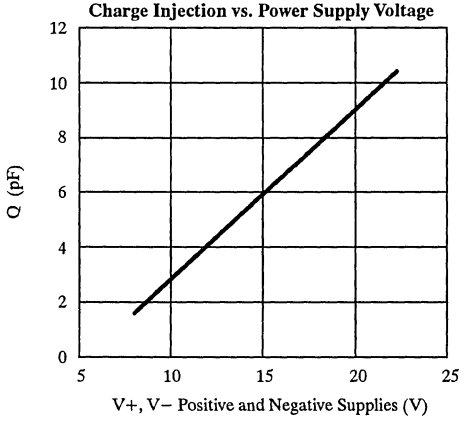
Leakages vs. Temperature



Typical Characteristics (Cont'd)

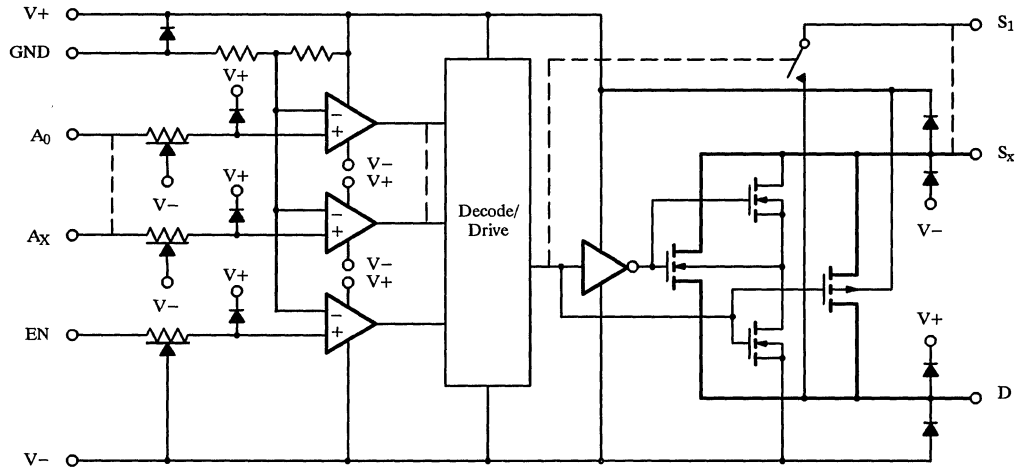




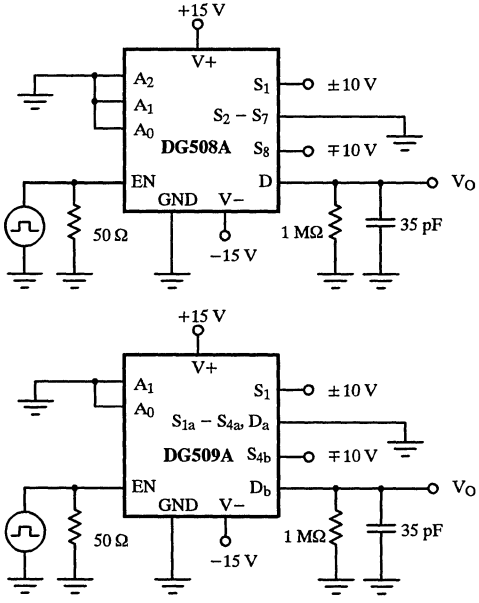


2

Schematic Diagram (Typical Channel)



Test Circuits



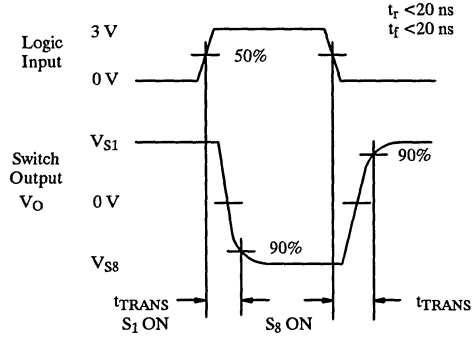


Figure 2. Transition Time

Test Circuits (Cont'd)

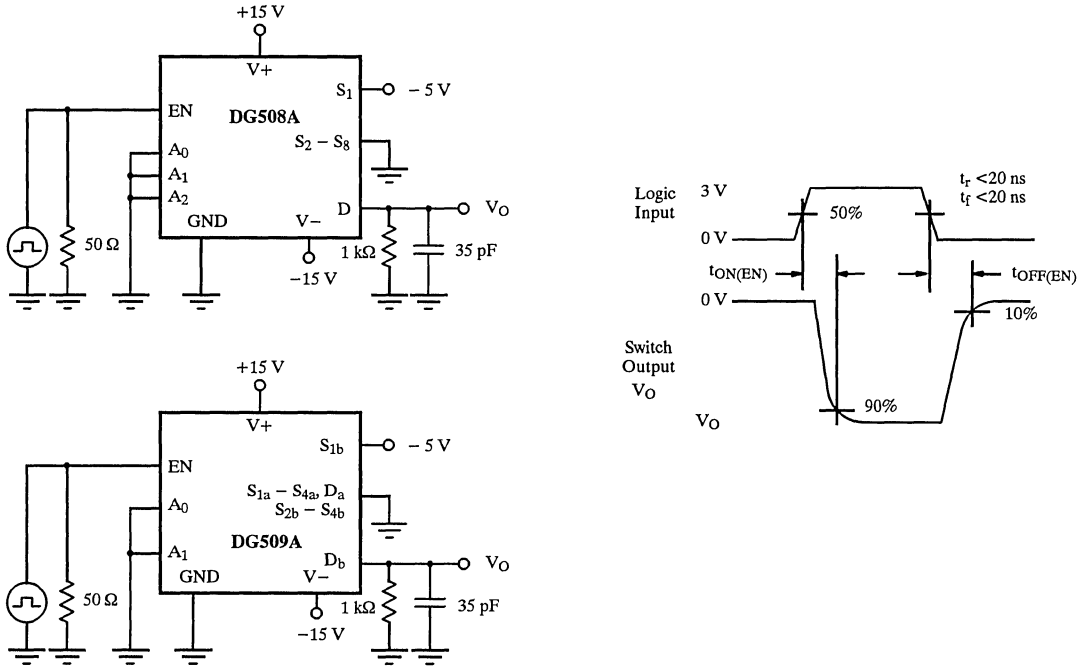


Figure 3. Enable Switching Time

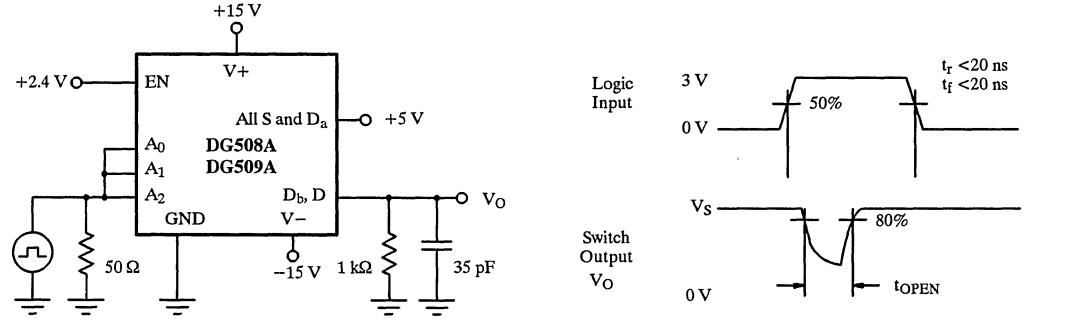
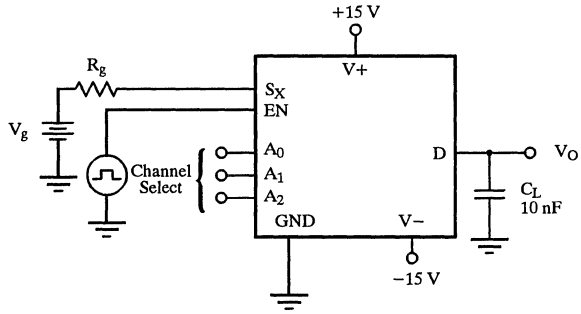
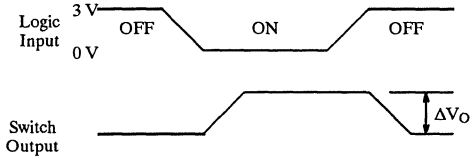


Figure 4. Break-Before-Make Interval

Test Circuits (Cont'd)





ΔV_O is the measured voltage due to charge transfer error Q, when the channel turns off.

$$Q = C_L \times \Delta V_O$$

Figure 5. Charge Injection

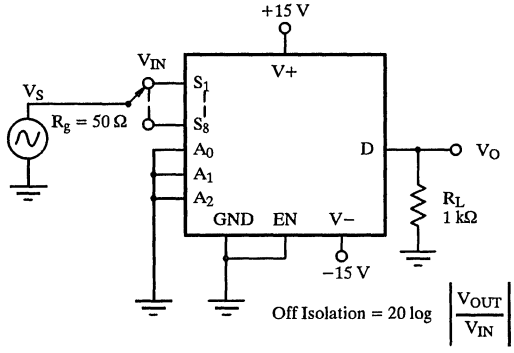


Figure 6. Off Isolation

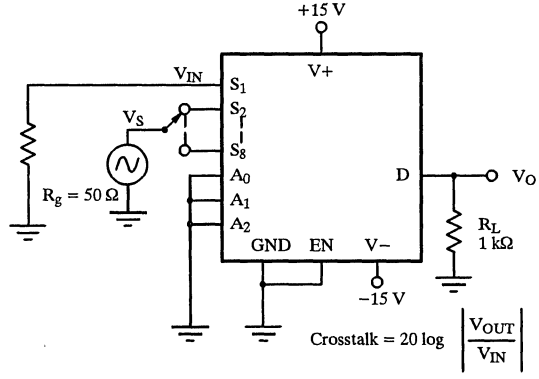


Figure 7. Crosstalk

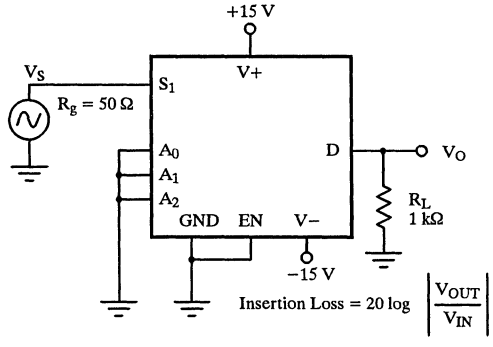


Figure 8. Insertion Loss

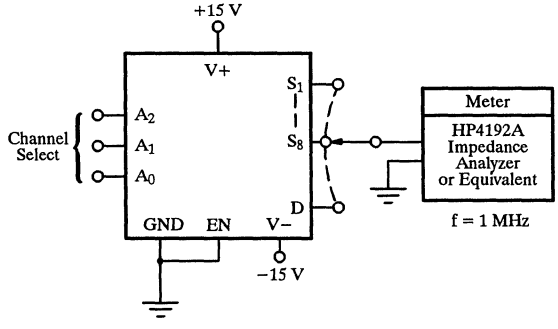


Figure 9. Source Drain Capacitance

Applications

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	−15	2.4/0.8	−15 to 15
10	−12	2.4/0.8	−12 to 12
12	−10	2.4/0.6	−10 to 10
8[b]	−8	2.4/0.4	−8 to 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 11). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V− value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V− rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V−, but it preserves the low channel resistance and low leakage characteristics.

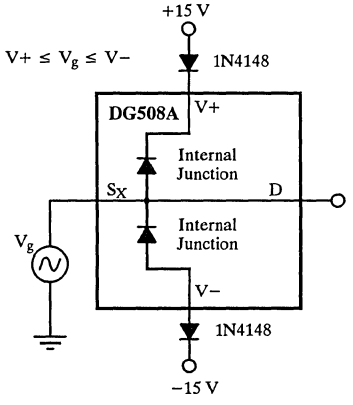


Figure 10. Overvoltage Protection Using Blocking Diodes

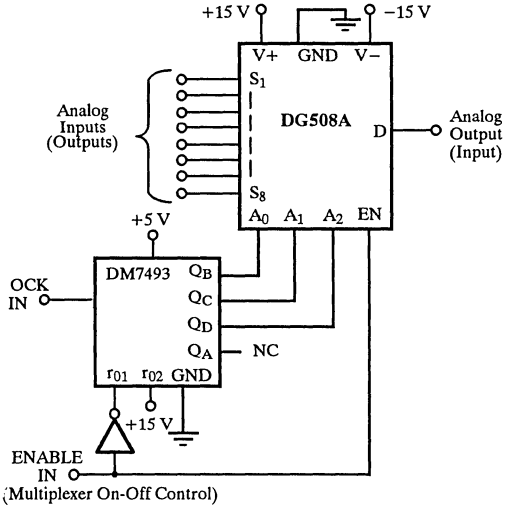


Figure 11. 8-Channel Sequential Multiplexer/ Demultiplexer

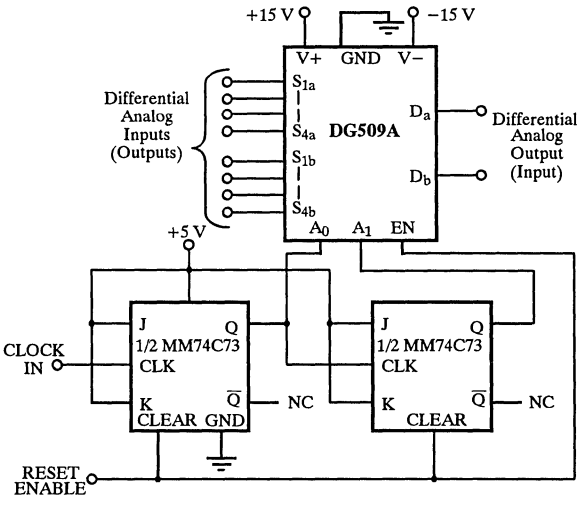


Figure 12. Differential 4-Channel Sequential Multiplexer/ Demultiplexer

Siliconix
A Member of the TEMIC Group

Latchable Single 8-Channel/Differential 4-Channel Analog Multiplexers

Features

- Low $r_{DS(on)}$: 270 Ω
- 44-V Power Supply Rating
- On-Board Address Latches
- Break-Before-Make
- Low Leakage—$I_{D(on)}$: 30 pA

Benefits

- Improved System Accuracy
- Microporcessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk

Applications

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Medical Instrumentation

Description

The DG528 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). DG529, a 4-channel dual analog multiplexer, is designed to connect one of four differential inputs to a common differential output as determined by its 2-bit binary address (A_0, A_1) logic.

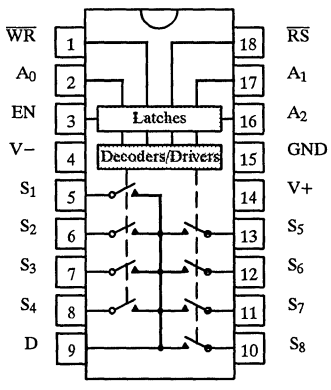
These analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary shorting of the input signals. The DG528/529 are built on the improved PLUS-40 CMOS process. A buried layer prevents latchup.

The on chip TTL-compatible address latches simplify digital interface design and reduce board space in data acquisition systems, process controls, avionics, and ATE.

Functional Block Diagrams and Pin Configurations

DG528

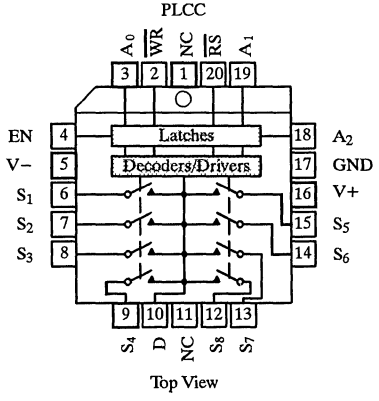
Dual-In-Line



Top View

DG528

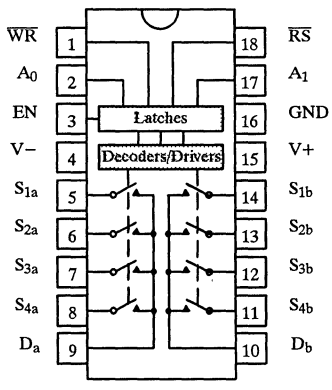
PLCC



Top View

DG529

Dual-In-Line



Top View

Truth Tables

Truth Table — DG528
8-Channel Single-Ended Multiplexer

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X	↓	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Truth Table — DG529
Differential 4-Channel Multiplexer

A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching					
X	X	X	↓	1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information — DG528

Temp Range	Package	Part Number
0 to 70°C	18-Pin Plastic DIP	DG528CJ
	20-Pin PLCC	DG528DN
−25 to 85°C	18-Pin CerDIP	DG528BK
−55 to 125°C		DG528AK
		DG528AK/883
		5962-8768901VA

Ordering Information — DG529

Temp Range	Package	Part Number
0 to 70°C	18-Pin Plastic DIP	DG529CJ
−25 to 85°C	18-Pin CerDIP	DG529BK
−55 to 125°C		DG529AK/883

Absolute Maximum Ratings

Voltage Referenced to V−
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Storage Temperature (AK, BK Suffix) ..... −65 to 150°C
(CJ, DN Suffix) ..... −65 to 125°C

Power Dissipation (Package)[b]
18-Pin Plastic DIP[c] ..... 470 mW
18-Pin CerDIP[d] ..... 900 mW
20-Pin PLCC[e] ..... 800 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6.3 mW/°C above 75°C.
d. Derate 1.2 mW/°C above 75°C.
e. Derate 10 mW/°C above 75°C.

2

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, WR = 0 $\overline{RS}$ = 2.4 V, V_{IN} = 2.4 V, 0.8 μF[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix −40 to 85°C Min[d]	B, C, D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −200 μA		Room Full	270		400 500		450 550	Ω
Greatest Change in $r_{DS(on)}$ Between Channels[f]	$\Delta r_{DS(on)}$	−10 V < V_S < 10 V		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_S = ±10 V V_D = ∓10 V		Room Full	±0.005	−1 −50	1 50	−5 −50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ±10 V V_S = ∓10 V	DG528	Room Full	±0.015	−10 −200	10 200	−20 −200	20 200	
			DG529	Room Full	±0.008	−10 −100	10 100	−20 −100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V V_{EN} = 2.4 V	DG528	Room Full	±0.03	−10 −200	10 200	−20 −200	20 200	
			DG529	Room Full	±0.015	−10 −100	10 100	−20 −100	20 100	
Digital Control										
Logic Input Current	I_{AH}	V_A = 2.4 V		Room Hot	−0.002	−10 −30		−10 −30		μA
Input Voltage High		V_A = 15 V		Room Hot	0.006		10 30		10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Room Hot	−0.002	−10 −30		−10 −30		
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 5		Room	0.6		1			μs
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room	0.2					
EN and $\overline{WR}$ Turn-On Time	$t_{ON(EN, WR)}$	See Figures 6 and 7		Room	1		1.5			
EN and $\overline{WR}$ Turn-Off Time	$t_{OFF(EN, WR)}$	See Figures 6 and 8		Room	0.4		1			
Charge Injection	Q	V_S = 0 V, R_y = 0 Ω, C_L = 10 μF		Room	4					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room	68					dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	2.5					pF
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 140 kHz		Room	5					
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 140 kHz	DG528	Room	25					
			DG529	Room	12					
Minimum Input Timing Requirements										
Write Pulse Width	t_W			Full		300		300		ns
A_X, EN Setup Time	t_S			Full		180		180		
A_X, EN Hold Time	t_H			Full		30		30		
Reset Pulse Width	t_{RS}	V_S = 5 V, See Figure 3		Full		500		500		

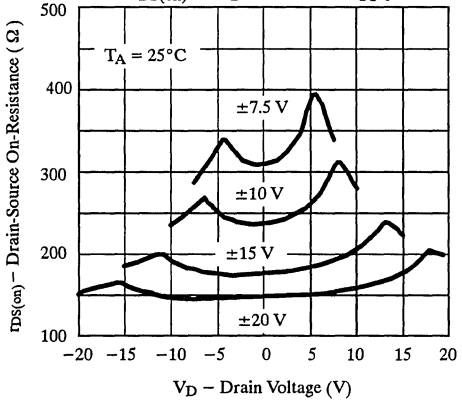
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V, WR = 0 $\overline{RS}$ = 2.4 V, V_{IN} = 2.4 V, 0.8 µF[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix −40 to 85°C Min[d]	B, C, D Suffix −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0	Room			2.5		2.5	mA
Negative Supply Current	I−		Room		−1.5		−1.5		

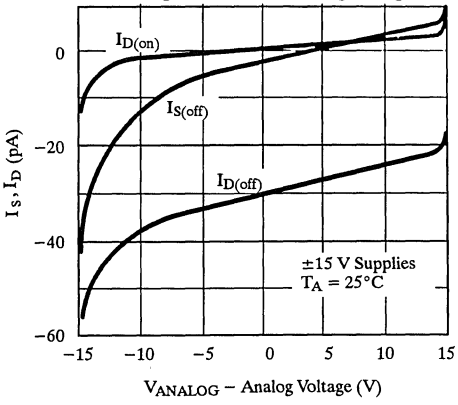
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

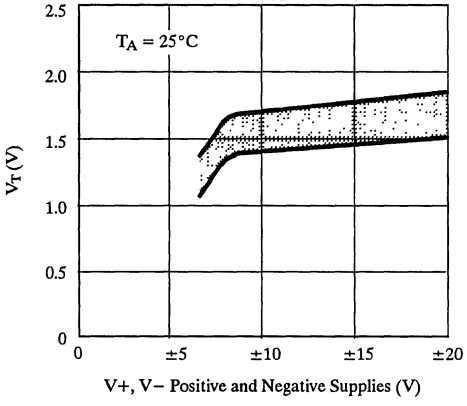
$r_{DS(on)}$ vs. V_D and Power Supply



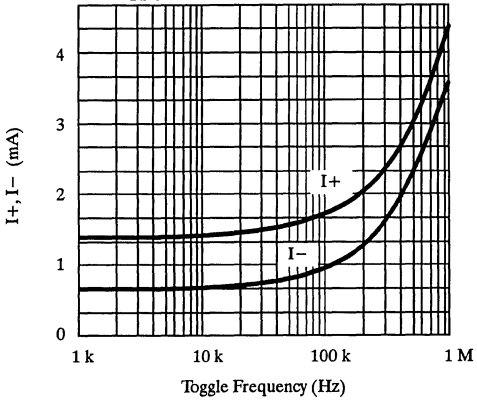
Leakage Currents vs. Analog Voltage



Input Switching Threshold vs. V+ and V− Supply Voltages



Supply Currents vs. Toggle Frequency



2

Schematic Diagram

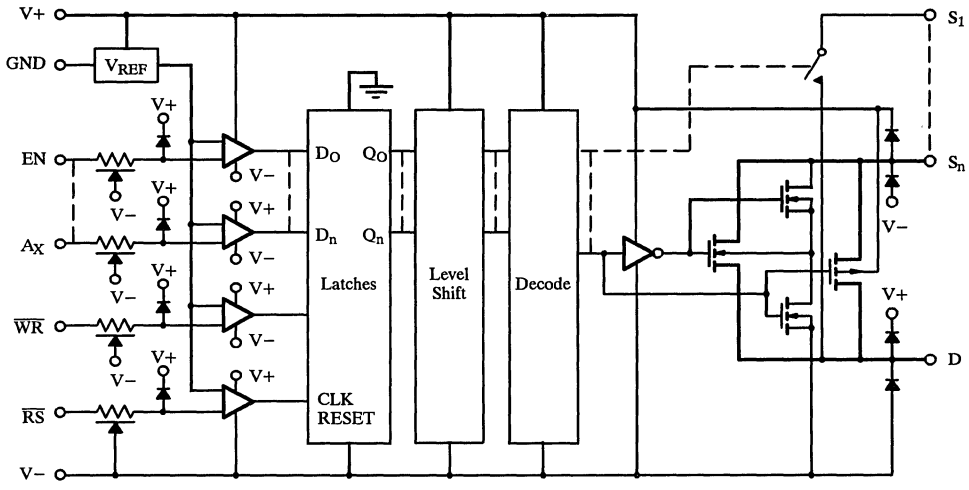


Figure 1.

Detailed Description

The internal structure of the DG528/DG529 includes a 5-V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the $\overline{WR}$ input is low, resulting in transparent latch operation. As soon as $\overline{WR}$ returns high, the latches hold the data last present on the D_X input, subject to the minimum input timing requirements.

Following the latches the Q_X signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full on/off switch operation for any analog signal present between the V+ and V− supply rails.

The EN pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard-wired to the logic supply or to V+ if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

Timing Diagrams

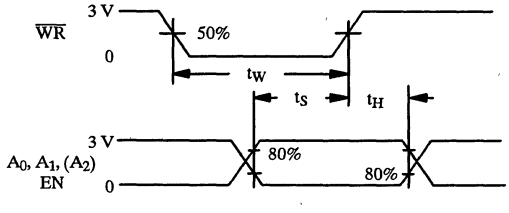


Figure 2.

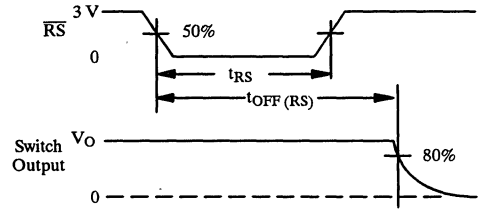


Figure 3.

Test Circuits

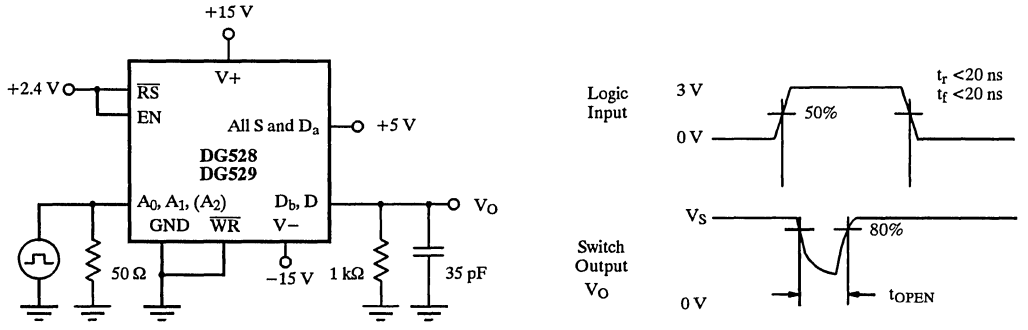


Figure 4. Break-Before-Make

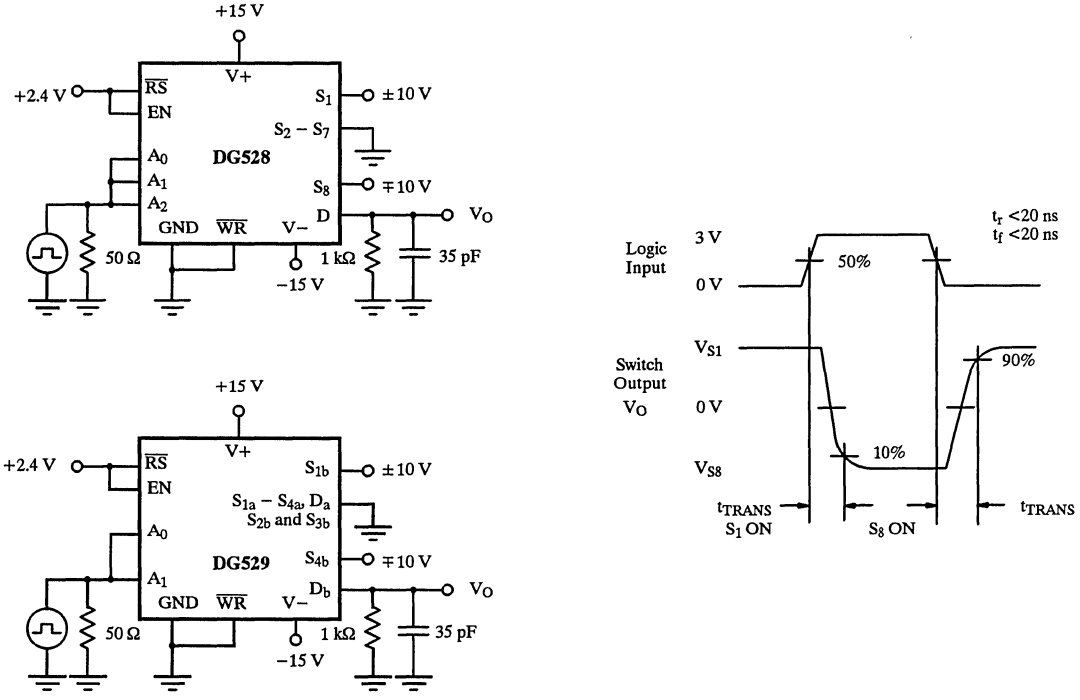


Figure 5. Transition Time

2

Test Circuits (Cont'd)

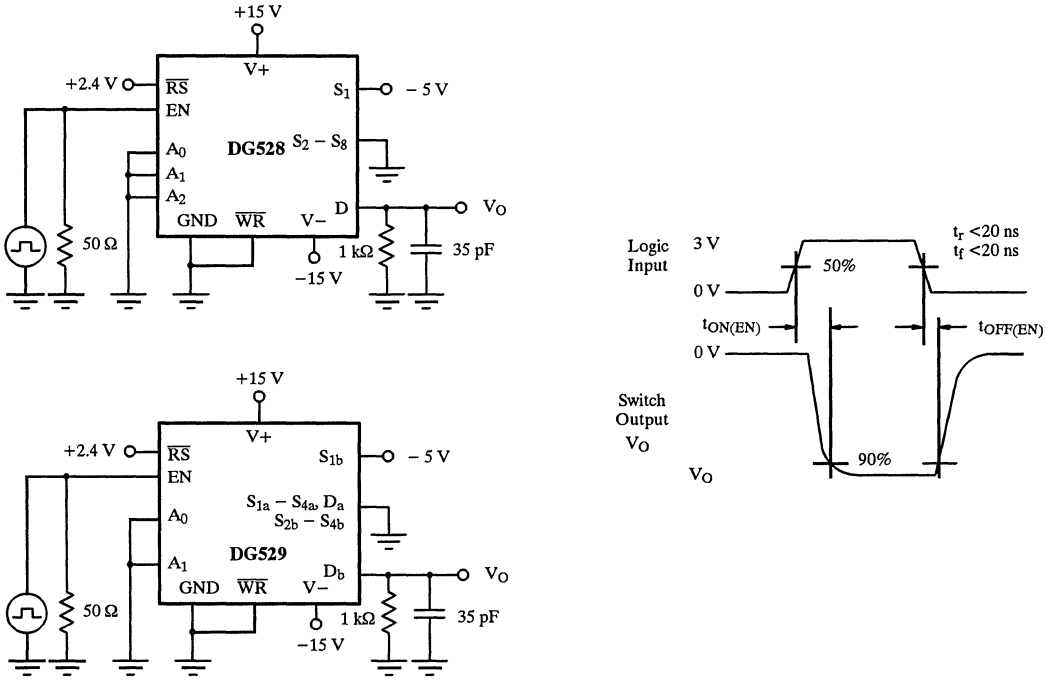


Figure 6. Enable t_{ON}/t_{OFF} Time

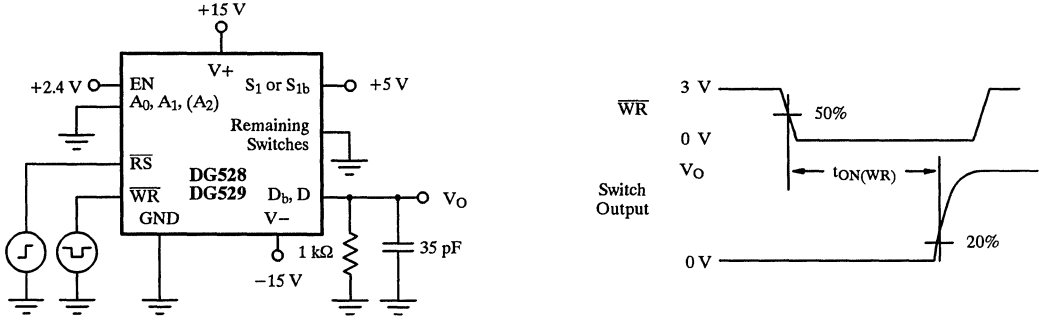


Figure 7. Write Turn-On Time $t_{ON(\overline{WR})}$

Test Circuits (Cont'd)

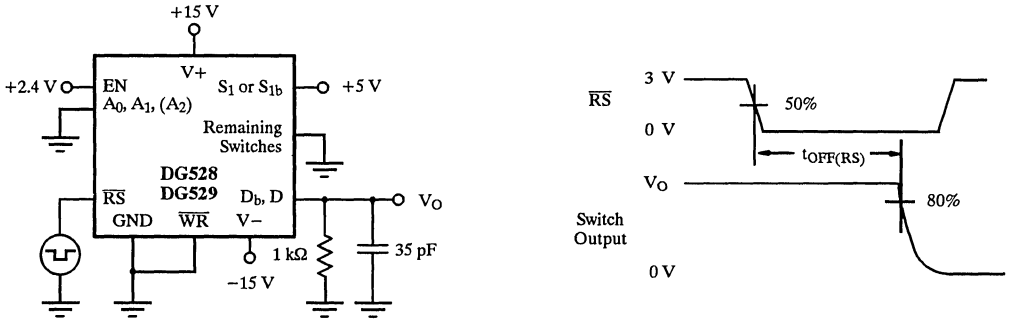


Figure 8. Reset Turn-Off Time $t_{OFF(RS)}$

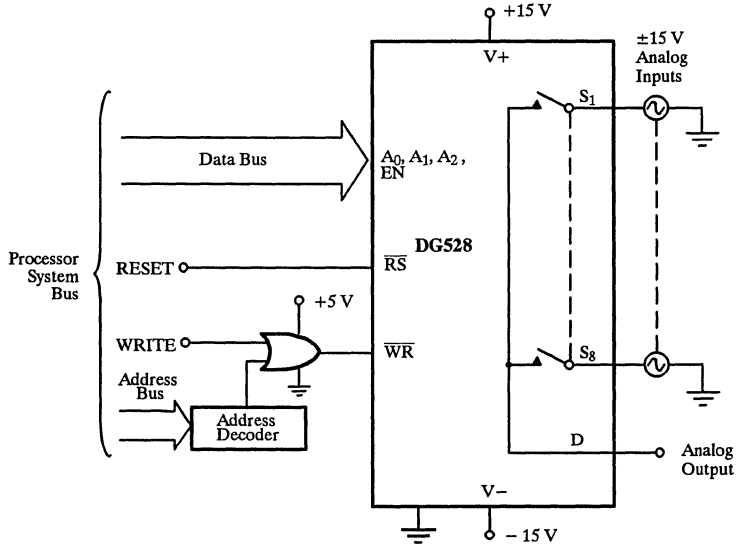


Figure 9. Bus Interface

Applications

Bus Interfacing

The DG528/DG529 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 9).

Applications (Cont'd)

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A_2, A_1, A_0. In this mode the DG528 is identical to the popular DG508A. The same is true of the DG529 versus the popular DG509A.

During system power-up, $\overline{RS}$ would be low, maintaining all eight switches in the off state. After $\overline{RS}$ returned high the DG528 maintains all switches in the off state. When the system program performs a write operation to the address assigned to the DG528, the address decoder provides a $\overline{CS}$ active low signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the high state, (positive edge) the input latches of the DG528 save the data from the DATA BUS. The coded information in the A_0, A_1, A_2 and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger multiplexers.

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
20	−20	2.4/0.8	±20
15[b]	−15	2.4/0.8	±15
8[c]	−8 (min)	2.4/0.8	±8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND.
c. Operation below ±8 V is not recommended.

4-/8-Channel Wideband Video Multiplexers

Features

- Wide Bandwidth: 500 MHz
- Very Low Crosstalk: −97 dB @ 5 MHz
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply
- Low $r_{DS(on)}$: 45 Ω

Benefits

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

Applications

- Wideband Signal Routing and Multiplexing
- Video Switchers
- ATE Systems
- Infrared Imaging

Description

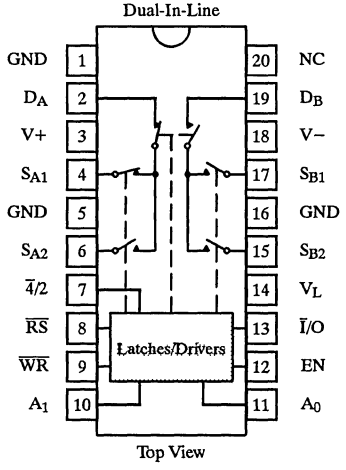
The DG534 is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538 is an 8-channel or dual 4-channel multiplexer. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low on-resistance and low capacitance of the these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG534/DG538 are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of off isolation. Crosstalk is reduced to −97 dB at 5 MHz by including a ground line between each adjacent signal path.

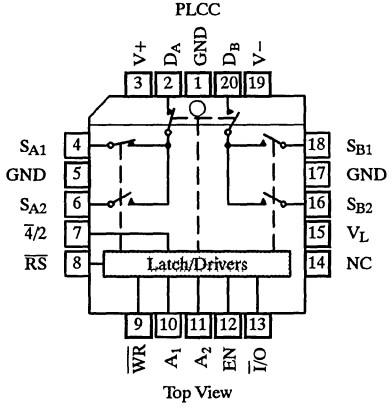
The DG534A/DG538A are recommended for new designs.

Functional Block Diagrams and Pin Configurations

DG534DJ



DG534DN

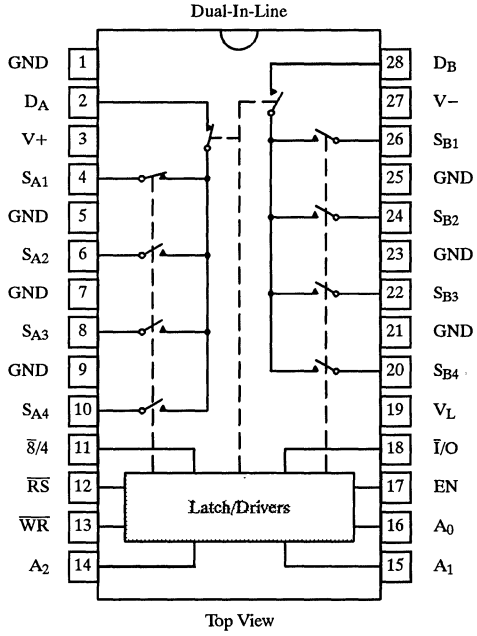


2

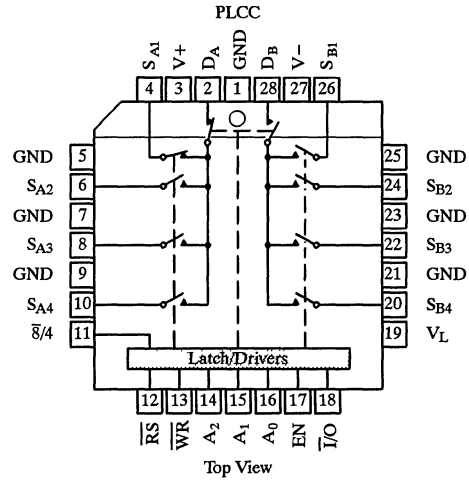
Not Recommended for New Designs

Functional Block Diagrams and Pin Configurations (Cont'd)

DG538DJ



DG538DN



Truth Tables and Ordering Information

Ordering Information – DG534

Temp Range	Package	Part Number
−40 to 85°C	20-Pin Plastic DIP	DG534DJ
	20-Pin PLCC	DG534DN
−55 to 125°C	20-Pin Sidebraze	DG534AP
		DG534AP/883

Truth Table — DG534

I/O	A_1	A_0	EN	WR	RS	4/2[a]	On Switch		
X	X	X	X	↓	1	1	Maintains previous state		
X	X	X	X	X	0	X	None (latches cleared)		
X	X	X	0	0	1	X	None		Latches Transparent
0	0	0	1	0	1	0	S_{A1}	D_A and D_B may be connected externally	
0	0	1	1	0	1	0	S_{A2}		
0	1	0	1	0	1	0	S_{B1}		
0	1	1	1	0	1	0	S_{B2}		
0	X	0	1	0	1	1	S_{A1} and S_{B1}		
0	X	1	1	0	1	1	S_{A2} and S_{B2}		
1	Note b			1	1	Note c			

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2$ V
X = Don't Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With I/O high, A_n pin becomes output and reflects latch contents. See timing diagrams for more detail.
c. 4/2 can be either "1" or "0" but should not change during these operations.

Not Recommended for New Designs

Truth Tables and Ordering Information (Cont'd)

Ordering Information – DG538

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG538DJ
	28-Pin PLCC	DG538DN
−55 to 125°C	28-Pin Sidebraze	DG538AP
		DG538AP/883

Truth Table — DG538

$\overline{I/O}$	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	$\overline{8}/4$[a]	On Switch	
X	X	X	X	X	⌐	1	1	Maintains previous state	
X	X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	X	0	0	1	X	None	Latches Transparent
0	0	0	0	1	0	1	0	S_{A1}	D_A and D_B should be connected externally
0	0	0	1	1	0	1	0	S_{A2}	
0	0	1	0	1	0	1	0	S_{A3}	
0	0	1	1	1	0	1	0	S_{A4}	
0	1	0	0	1	0	1	0	S_{B1}	
0	1	0	1	1	0	1	0	S_{B2}	
0	1	1	0	1	0	1	0	S_{B3}	
0	1	1	1	1	0	1	0	S_{B4}	
0	X	0	0	1	0	1	1	S_{A1} and S_{B1}	
0	X	0	1	1	0	1	1	S_{A2} and S_{B2}	
0	X	1	0	1	0	1	1	S_{A3} and S_{B3}	
0	X	1	1	1	0	1	1	S_{A4} and S_{B4}	
1	Note b				1	1	Note c		

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2$ V
X = Don't Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With $\overline{I/O}$ high, A_n pin becomes output and reflects latch contents. See timing diagrams for more detail.
c. $\overline{8}/4$ can be either "1" or "0" but should not change during these operations.

Absolute Maximum Ratings

V+ to GND ..... −0.3 V to +21 V
V+ to V− ..... −0.3 V to +21 V
V− to GND ..... −10 V to +0.3 V
V_L ..... 0 V to (V+) + 0.3 V
Digital Inputs ..... (V−) −0.3 V to (V+) + 0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V−) −0.3 V to (V−) + 14 V
or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current(S or D) Pulsed 1 ms 10% Duty ..... 40 mA

Storage Temperature (A Suffix) ..... −65 to 150°C
(D Suffix) ..... −65 to 125°C
Power Dissipation (Package)[a]
Plastic DIP[b] ..... 625 mW
PLCC[c] ..... 450 mW
Sidebraze[d] ..... 1200 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 8.3 mW/°C above 75°C.
c. Derate 6 mW/°C above 75°C.
d. Derate 16 mW/°C above 75°C.

2

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V, V_L = 5 V $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN= 2 V		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[g]	V_{ANALOG}	V− = −5 V		Full		−5	8	−5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_S = 0 V V_{AIL} = 0.8 V, V_{AIH} = 2 V Sequence Each Switch On		Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$			Room			9		9	
Source Off Leakage Current	$I_{S(off)}$	V_S = 8 V, V_D = 0 V, EN = 0.8 V		Room Full	0.05	−5 −50	5 50	−5 −50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 0 V, V_D = 8 V, EN = 0.8 V		Room Full	0.1	−20 −500	20 500	−20 −100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 8 V		Room Full	0.1	−20 −1000	20 1000	−20 −200	20 200	
Digital Control										
Input Voltage High	V_{AIH}			Full		2		2		V
Input Voltage Low	V_{AIL}			Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V, or 2 V or 5 V		Room Full	−0.1	−1 −10	1 10	−1 −10	1 10	µA
Address Output Current	I_{AO}	V_{AO} = 2.7 V		Room	−300					
		V_{AO} = 0.4 V		Room	300					
Dynamic Characteristics										
On State Input Capacitance[g]	$C_{S(on)}$		PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance[g]	$C_{S(off)}$		PLCC	Room	3		5		4	
			DIP	Room	4				5	
Off State Output Capacitance[g]	$C_{D(off)}$		PLCC	Room	6		10		8	
			DIP	Room	8				10	
Transition Time	t_{TRANS}			Room Full	170		300 500		300 500	ns
Break-Before-Make Interval	t_{OPEN}			Room Full	80	50 25		50 25		
EN, $\overline{WR}$ Turn On Time	t_{ON}			Room Full	180		300 500		300 500	
EN, Turn Off Time	t_{OFF}			Room Full	95		175 300		175 300	
Charge Injection	Qi			Room	−70					pC
Chip Disabled Crosstalk[f]	$X_{TALK(CD)}$	R_L = 75 Ω, f = 5 MHz EN = 0.8 V	PLCC	Room	−75					dB
			DIP	Room	−65					
Adjacent Input Crosstalk[f]	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz	PLCC	Room	−97					
			DIP	Room	−87					
		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz	PLCC	Room	−80					
			DIP	Room	−70					

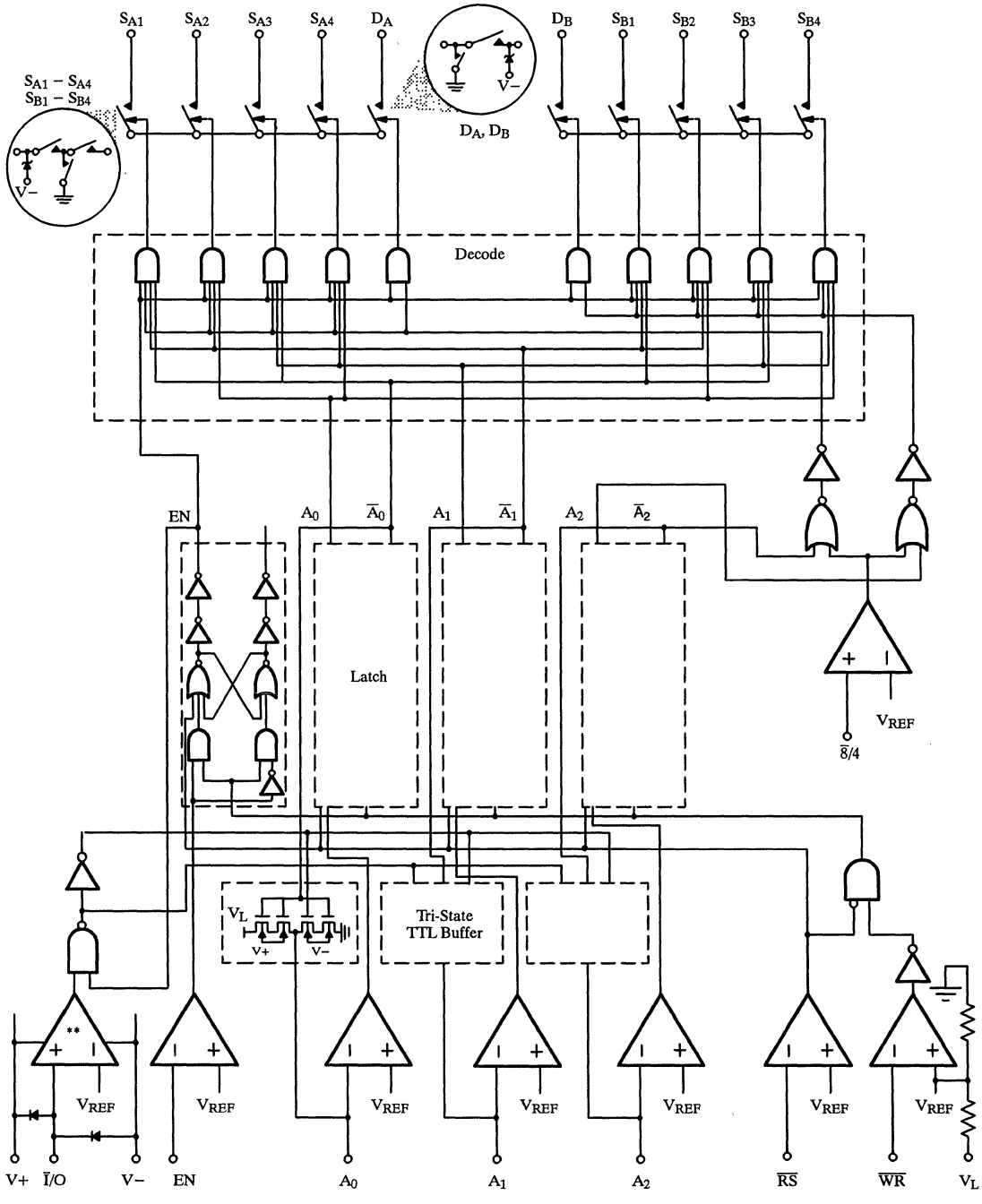
Not Recommended for New Designs

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V, V_L = 5 V $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN = 2 V		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)										
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz	PLCC	Room	−77					dB
			DIP	Room	−72					
		R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz	PLCC	Room	−77					
			DIP	Room	−72					
Differential Crosstalk	$X_{TALK(DIFF)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz		Room	−84					
		R_{IN} = R_L = 75 Ω, f = 5 MHz		Room	−84					
Bandwidth	BW	R_L = 50 Ω		Room	500					MHz
Power Supplies										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or V+		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I−			Room Full	0.6	−1.8 −2		−1.8 −2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V−	Functional Test Only		Full		10	21	10	21	V
	V− to GND			Full		−5.5	0	−5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	I_L			Full	150		500		500	µA
Timing										
Reset to Write	t_{RW}	See Figure 1		Full		50		50		ns
$\overline{WR}$, $\overline{RS}$ Minimum Pulse Width	t_{MPW}			Full		200		200		
A_0, A_1, EN Data Valid to Strobe	t_{DW}			Full		100		100		
A_0, A_1, EN Data Valid after Strobe	t_{WD}			Full		50		50		
Address Bus Tri-State[e]	t_{AZ}			Room	25					
Address Bus Output	t_{AO}			Room	95					
Address Bus Input	t_{AI}			Room	110					

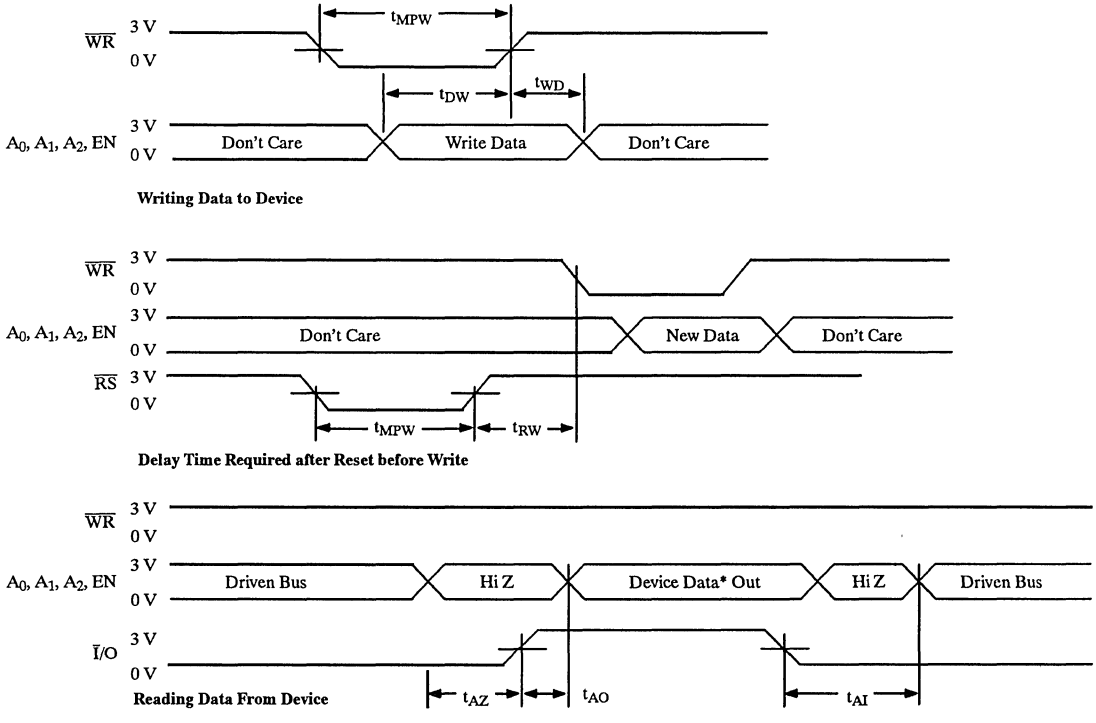
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Defined by system bus requirements.
f. Each individual pin shown as GND must be grounded.
g. Guaranteed by design, not subject to production test.

Control Circuitry



* Decode section includes delay circuitry in AND gating to ensure proper break-before-make operation.
** Typical all digital inputs.

Output Timing Requirements



* Enable must be latched high to read data, otherwise BUS is high Z. V− ≤ −3 V required for readback functionality.

Figure 1.

Applications

To protect against latchup V_L must not exceed V+ by more than 0.3 V. This is easily achieved by generating V_L from V+ using a Zener or a resistor divider network as shown in Figure 2. When an external V_L is available the alternative simple protection circuit shown in Figure 3 should be used to prevent triggering the parasitic SCR during power up. The DG53XA does not require these protection diodes.

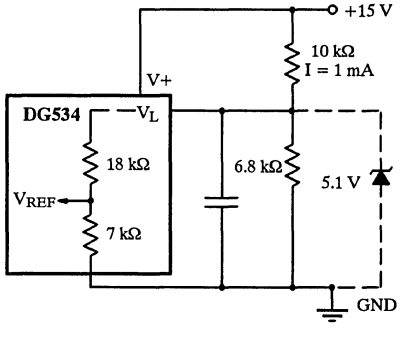


Figure 2. V_L Generated from V+

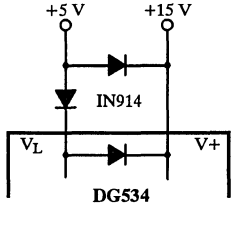


Figure 3. External Diodes Prevent Latchup

Siliconix
A Member of the TEMIC Group

4-/8-Channel Wideband Video Multiplexers

Features

- Wide Bandwidth: 500 MHz
- Very Low Crosstalk: −97 dB @ 5 MHz
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply
- Low $r_{DS(on)}$: 45 Ω
- Single-Ended or Differential Operation
- Latch-up Proof

Benefits

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- High-Speed Readback
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

Applications

- Wideband Signal Routing and Multiplexing
- Video Switchers
- ATE Systems
- Infrared Imaging
- Ultrasound Imaging

Description

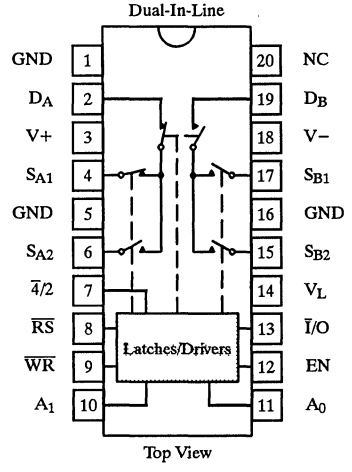
The DG534A is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538A is an 8-channel or dual 4-channel multiplexer. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low on-resistance and low capacitance of the these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG534A/DG538A are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are connected in a "T" configuration to achieve extremely high levels of off isolation. Crosstalk is reduced to −97 dB at 5 MHz by including a ground line between adjacent signal paths. An epitaxial layer prevents latch-up.

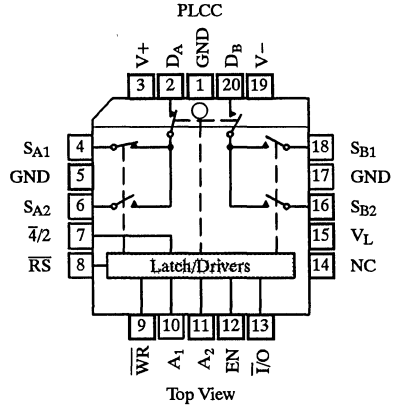
For more information refer to Siliconix Applications Note AN502.

Functional Block Diagrams and Pin Configurations

DG534ADJ

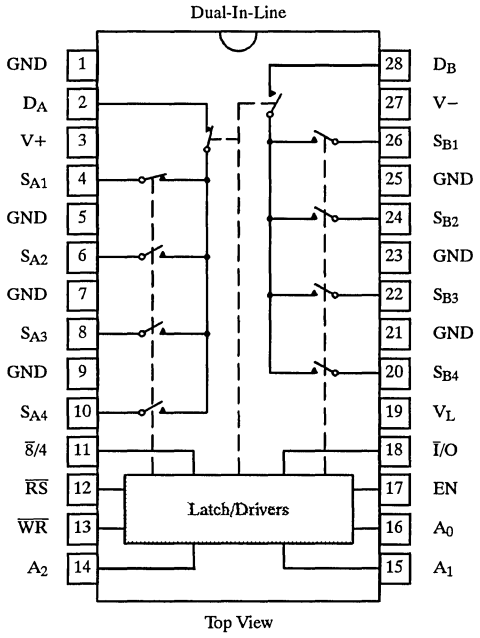


DG534ADN

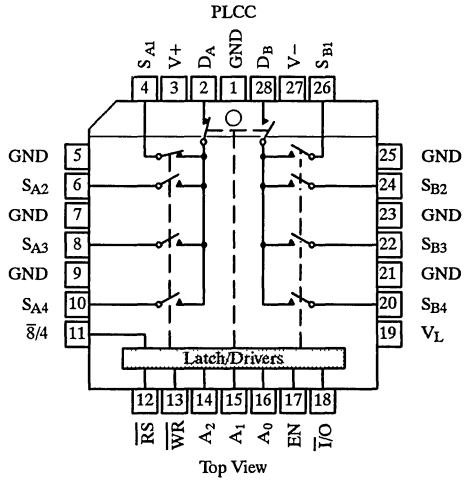


Functional Block Diagrams and Pin Configurations (Cont'd)

DG538ADJ



DG538ADN



Truth Tables and Ordering Information

Ordering Information — DG534A

Temp Range	Package	Part Number
−40 to 85°C	20-Pin Plastic DIP	DG534ADJ
	20-Pin PLCC	DG534ADN
−55 to 125°C	20-Pin Sidebraze	DG534AAP/883

Truth Table — DG534A

I/O	A_1	A_0	EN	WR	RS	4/2[a]	On Switch		
X	X	X	X	⌐	1	1	Maintains previous state		
X	X	X	X	X	0	X	None (latches cleared)		
X	X	X	0	0	1	X	None		Latches Transparent
0	0	0	1	0	1	0	S_{A1}	D_A and D_B may be connected externally	
0	0	1	1	0	1	0	S_{A2}		
0	1	0	1	0	1	0	S_{B1}		
0	1	1	1	0	1	0	S_{B2}		
0	X	0	1	0	1	1	S_{A1} and S_{B1}		
0	X	1	1	0	1	1	S_{A2} and S_{B2}		
1	Note b			1	1	Note c			

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2$ V
X = Don't Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With I/O high, A_n and EN pins become outputs and reflect latch contents. See timing diagrams for more detail.
c. 4/2 can be either "1" or "0" but should not change during these operations.

Truth Tables and Ordering Information (Cont'd)

Ordering Information – DG538A

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG538ADJ
	28-Pin PLCC	DG538ADN
−55 to 125°C	28-Pin Sidebraze	DG538AAP/883

Truth Table — DG538A

$\overline{I}/O$	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	$\overline{8}/4$[a]	On Switch	
X	X	X	X	X	⌐	1	1	Maintains previous state	
X	X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	X	0	0	1	X	None	Latches Transparent
0	0	0	0	1	0	1	0	S_{A1}	
0	0	0	1	1	0	1	0	S_{A2}	
0	0	1	0	1	0	1	0	S_{A3}	
0	0	1	1	1	0	1	0	S_{A4}	
0	1	0	0	1	0	1	0	S_{B1}	
0	1	0	1	1	0	1	0	S_{B2}	
0	1	1	0	1	0	1	0	S_{B3}	
0	1	1	1	1	0	1	0	S_{B4}	
0	X	0	0	1	0	1	1	S_{A1} and S_{B1}	
0	X	0	1	1	0	1	1	S_{A2} and S_{B2}	
0	X	1	0	1	0	1	1	S_{A3} and S_{B3}	
0	X	1	1	1	0	1	1	S_{A4} and S_{B4}	
1	Note b				1	1	Note c		

D_A and D_B should be connected externally

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2$ V
X = Don't Care

Notes:
a. Connect D_A and D_B together externally for single-ended operation.
b. With $\overline{I}/O$ high, A_n and EN pins become outputs and reflect latch contents. See timing diagrams for more detail.
c. $\overline{8}/4$ can be either "1" or "0" but should not change during these operations.

Absolute Maximum Ratings

V+ to GND ..... −0.3 V to +21 V
V+ to V− ..... −0.3 V to +21 V
V− to GND ..... −10 V to +0.3 V
V_L ..... 0 V to (V+) + 0.3 V
Digital Inputs ..... (V−) −0.3 V to (V_L) + 0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V−) −0.3 V to (V−) + 14 V
or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current(S or D) Pulsed 1 ms 10% Duty ..... 40 mA

Storage Temperature (A Suffix) ..... −65 to 150°C
(D Suffix) ..... −65 to 125°C
Power Dissipation (Package)[a]
Plastic DIP[b] ..... 625 mW
PLCC[c] ..... 450 mW
Sidebraze[d] ..... 1200 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 8.3 mW/°C above 75°C.
c. Derate 6 mW/°C above 75°C.
d. Derate 16 mW/°C above 75°C.

Specifications[a]

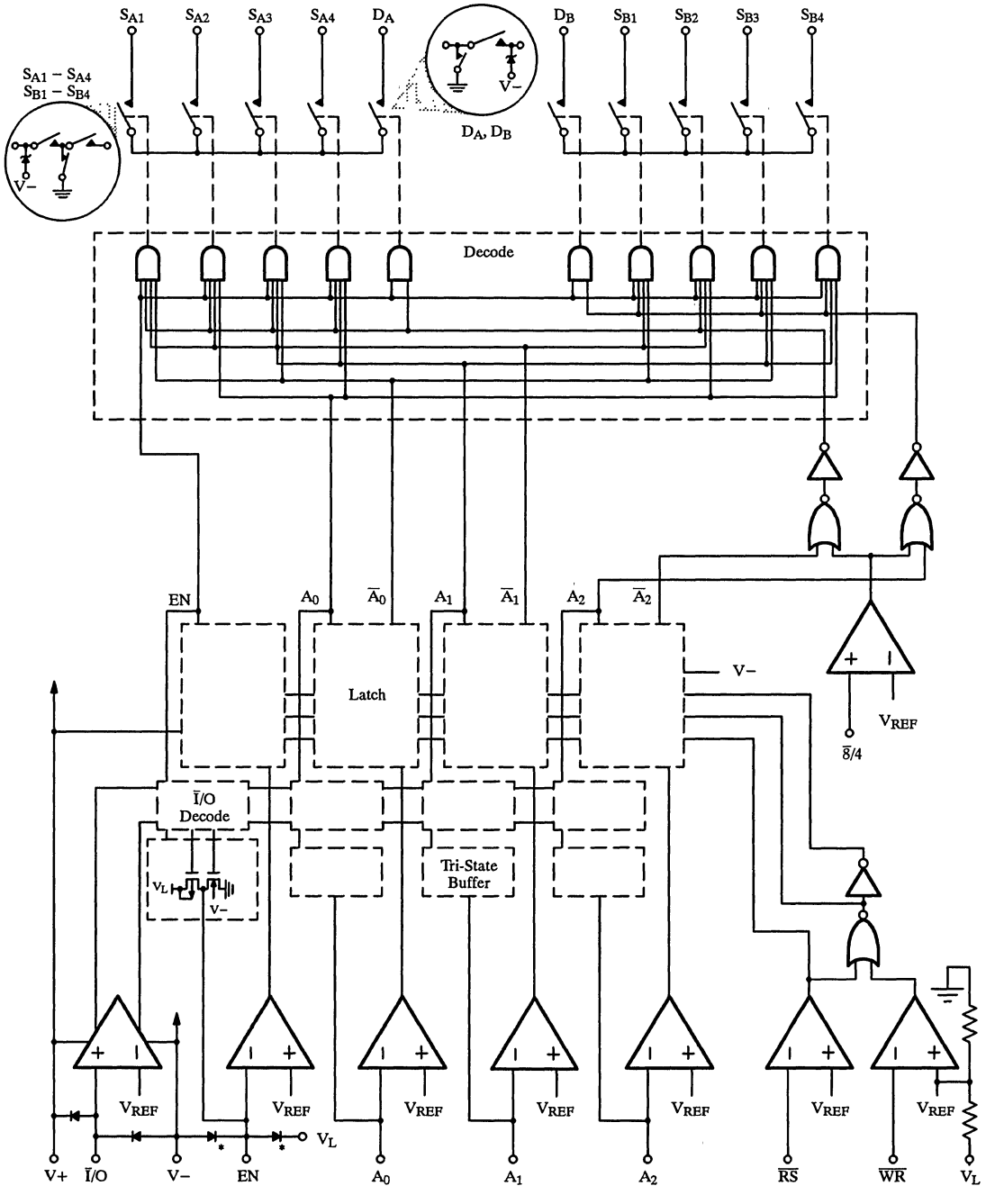
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V, V_L = 5 V $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN = 2 V		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch										
Analog Signal Range[g]	V_{ANALOG}	V− = −5 V		Full		−5	8	−5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_S = 0 V V_{AIL} = 0.8 V, V_{AIH} = 2 V Sequence Each Switch On		Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$			Room			9		9	
Source Off Leakage Current	$I_{S(off)}$	V_S = 8 V, V_D = 0 V, EN = 0.8 V		Room Full	0.05	−5 −50	5 50	−5 −50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 0 V, V_D = 8 V, EN = 0.8 V		Room Full	0.1	−20 −500	20 500	−20 −100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 8 V		Room Full	0.1	−20 −1000	20 1000	−20 −200	20 200	
Digital Control										
Input Voltage High	V_{AIH}			Full		2		2		V
Input Voltage Low	V_{AIL}			Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V, or 2 V or 5 V		Room Full	−0.1	−1 −10	1 10	−1 −10	1 10	µA
Address Output Current	I_{AO}	V_{AO} = 2.7 V		Room	−21		−2.5		−2.5	mA
		V_{AO} = 0.4 V		Room	3.5	2.5		2.5		
Dynamic Characteristics										
On State Input Capacitance[g]	$C_{S(on)}$	See Figure 11	PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance[g]	$C_{S(off)}$	See Figure 12	PLCC	Room	3		5		4	
			DIP	Room	4				5	
Off State Output Capacitance[g]	$C_{D(off)}$		PLCC	Room	6		10		8	
			DIP	Room	8				10	
Transition Time	t_{TRANS}	See Figure 4		Room Full	160		300 500		300 500	ns
Break-Before-Make Interval	t_{OPEN}			Room Full	80	50 25		50 25		
EN, $\overline{WR}$ Turn On Time	t_{ON}	See Figure 2 and 3		Room Full	150		300 500		300 500	
EN, Turn Off Time	t_{OFF}	See Figure 2		Room Full	105		175 300		175 300	
Charge Injection	Qi	See Figure 5		Room	−70					pC
Chip Disabled Crosstalk[f]	$X_{TALK(CD)}$	R_L = 75 Ω, f = 5 MHz EN = 0.8 V, See Figure 8	PLCC	Room	−75					dB
			DIP	Room	−65					
Adjacent Input Crosstalk[f]	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz, See Figure 9	PLCC	Room	−97					
			DIP	Room	−87					
		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz, See Figure 9	PLCC	Room	−80					
			DIP	Room	−70					

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V, V_L = 5 V $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN= 2 V		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)										
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz, See Figure 7	PLCC	Room	−77					dB
			DIP	Room	−72					
		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz, See Figure 7	PLCC	Room	−77					
			DIP	Room	−72					
Differential Crosstalk	$X_{TALK(DIFF)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz, See Figure 10		Room	−84					
		R_{IN} = R_L = 75 Ω f = 5 MHz, See Figure 10		Room	−84					
Bandwidth	BW	R_L = 50 Ω, See Figure 6		Room	500					MHz
Power Supplies										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or 5 V		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I−			Room Full	0.6	−1.8 −2		−1.8 −2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V−	Functional Test Only		Full		10	21	10	21	V
	V− to GND			Full		−5.5	0	−5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	I_L			Full	150		500		500	µA
Timing										
Reset to Write	t_{RW}	See Figure 1		Room Full	−22	50		50		ns
$\overline{WR}$, $\overline{RS}$ Minimum Pulse Width	t_{MPW}			Room Full	60	200		200		
A_0, A_1, EN Data Valid to Strobe	t_{DW}			Room Full	20	100		100		
A_0, A_1, EN Data Valid after Strobe	t_{WD}			Room Full	−20	50		50		
Address Bus Tri-State[e]	t_{AZ}			Room	25					
Address Bus Output	t_{AO}			Room	95					
Address Bus Input	t_{AI}			Room	110					

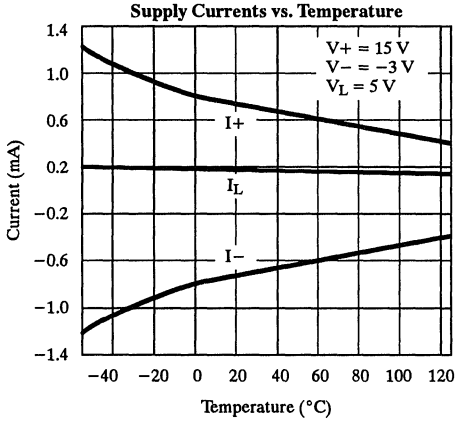
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Defined by system bus requirements.
f. Each individual pin shown as GND must be grounded.
g. Guaranteed by design, not subject to production test.

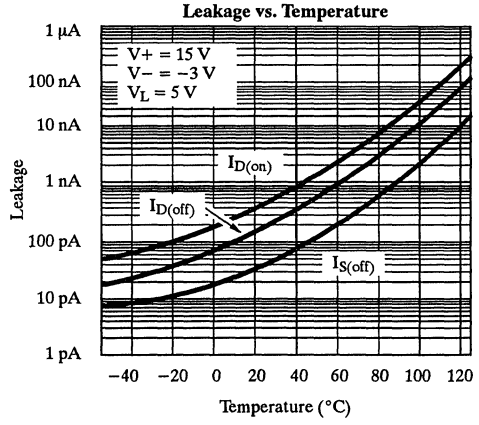
Control Circuitry

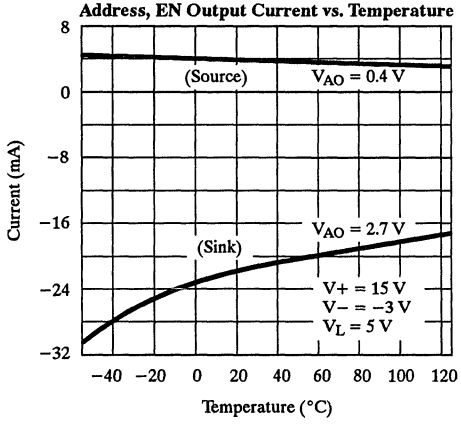


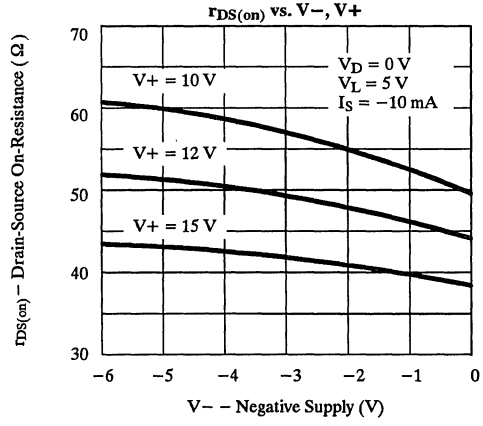
*Typical all Readback (A_X, EN) pins

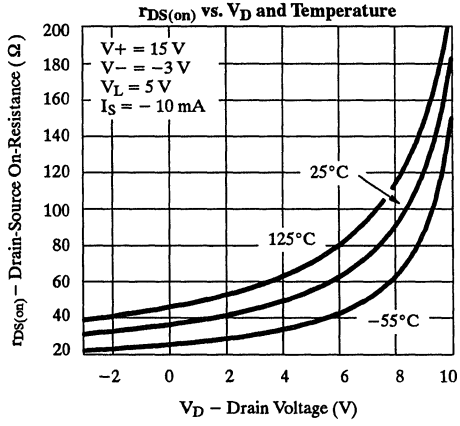
Typical Characteristics

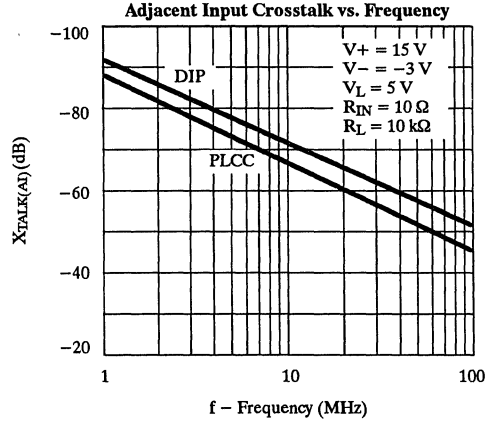






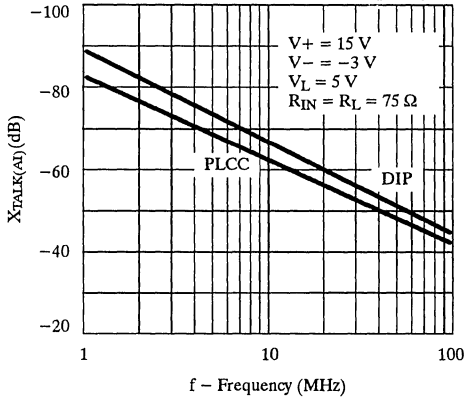




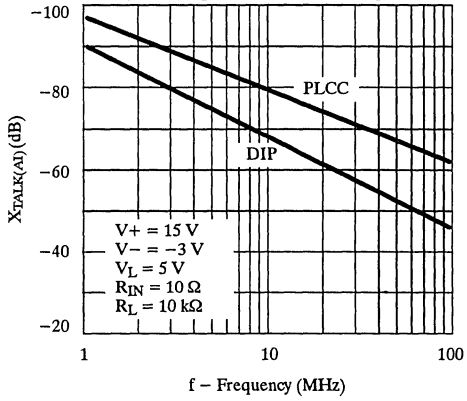


Typical Characteristics (Cont'd)

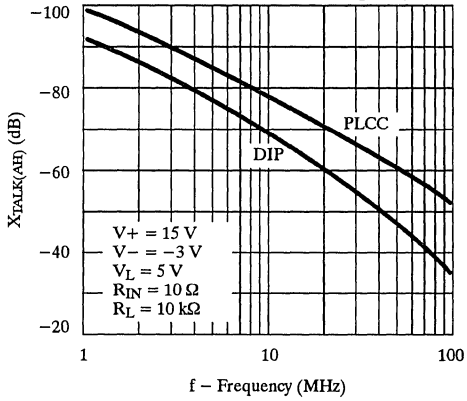
Adjacent Input Crosstalk vs. Frequency



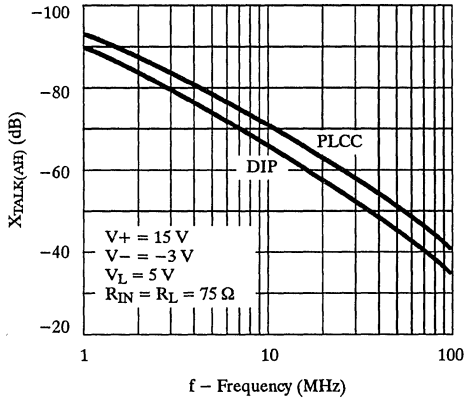
Adjacent Input Crosstalk vs. Frequency



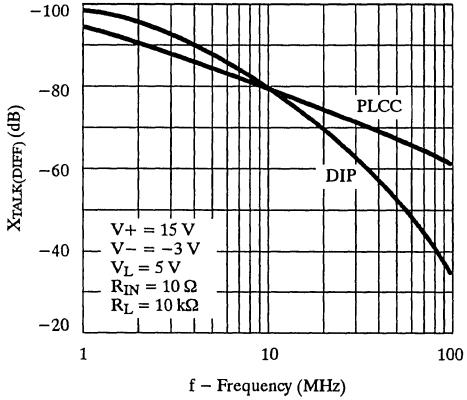
All Hostile Crosstalk vs. Frequency



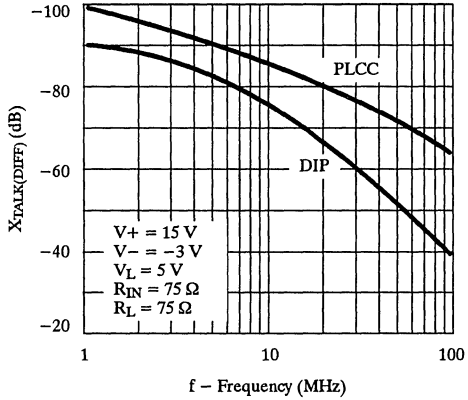
All Hostile Crosstalk vs. Frequency



Differential Crosstalk vs. Frequency

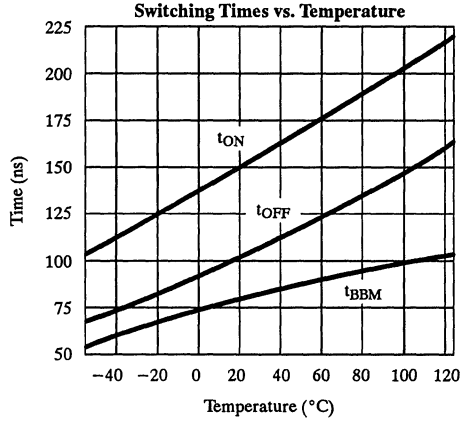


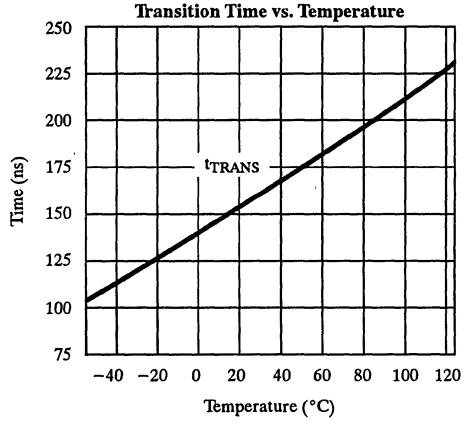
Differential Crosstalk vs. Frequency



2

Typical Characteristics (Cont'd)





Output Timing Requirements

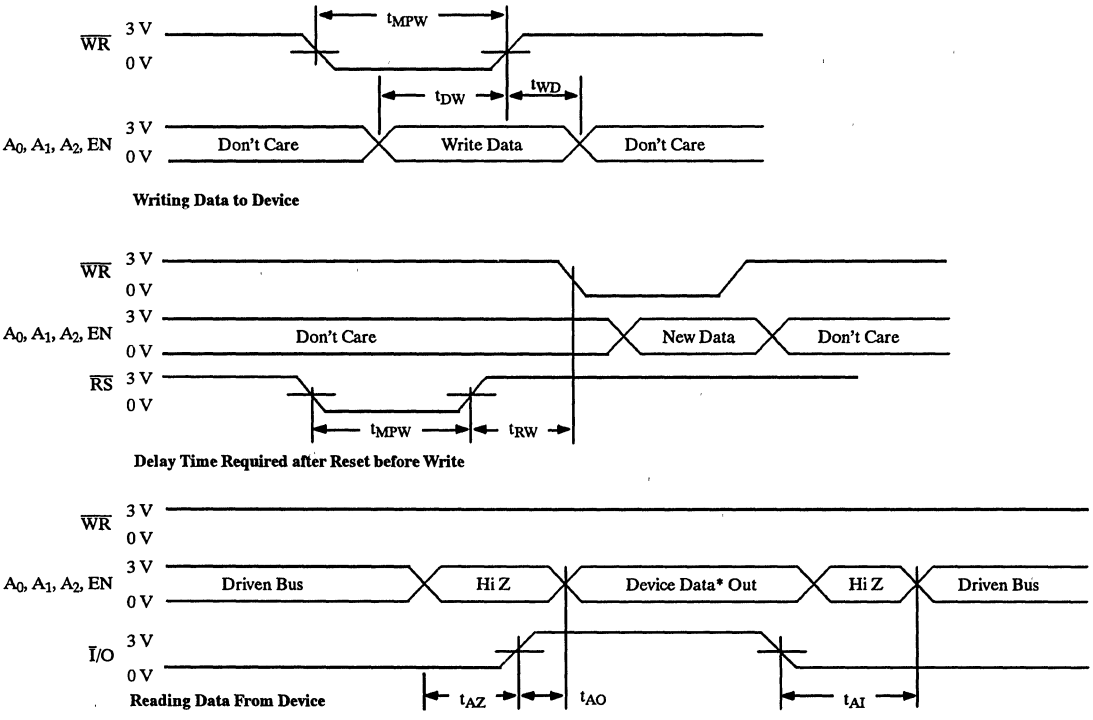


Figure 1.

Test Circuits

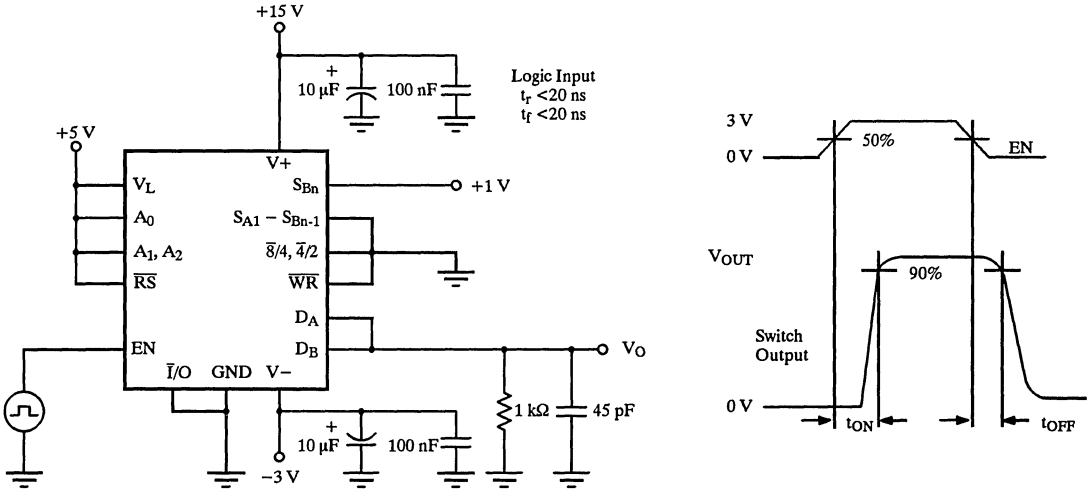


Figure 2. EN, CS, $\overline{CS}$, Turn On/Off Time

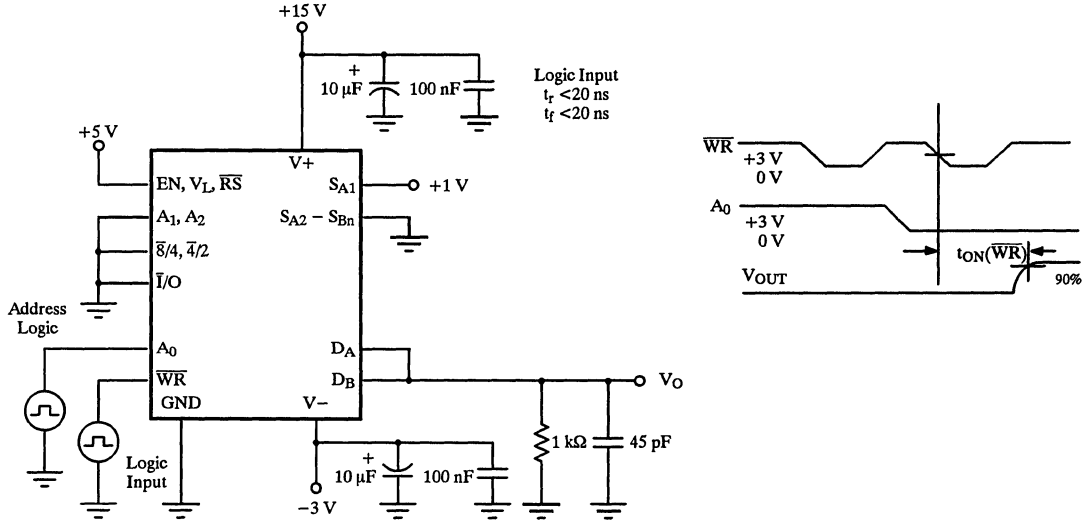


Figure 3. $\overline{WR}$, Turn On Time

2

Test Circuits (Cont'd)

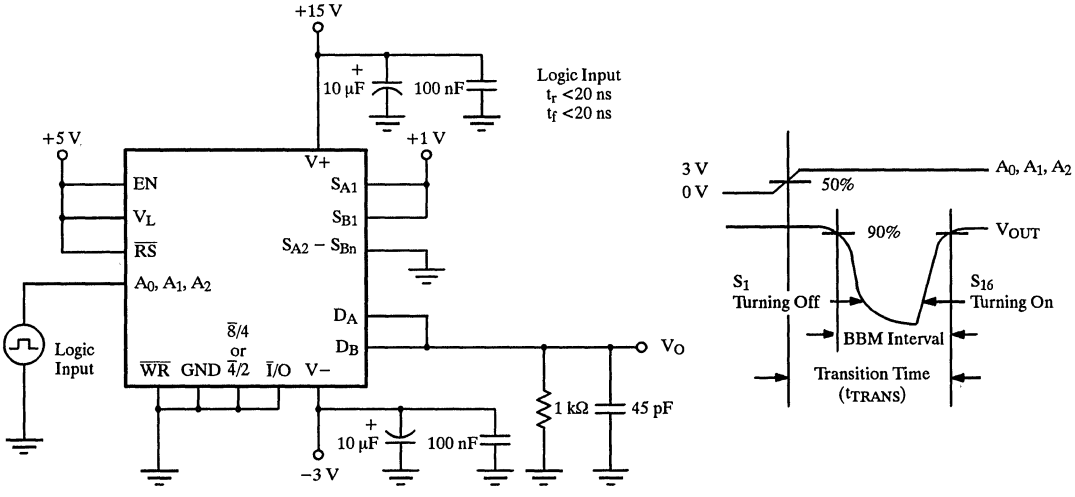
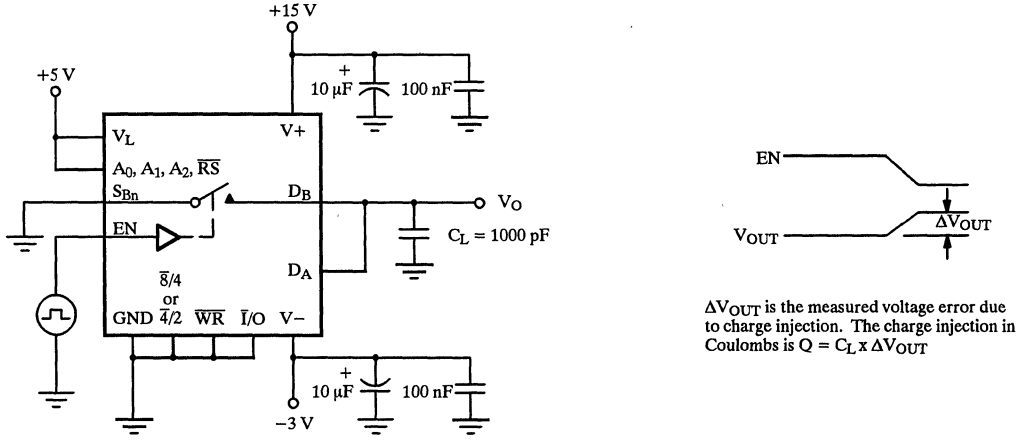


Figure 4. Transition Time and Break-Before-Make Interval



ΔV_{OUT} is the measured voltage error due to charge injection. The charge injection in Coulombs is $Q = C_L \times \Delta V_{OUT}$

Figure 5. Charge Injection

Test Circuits (Cont'd)

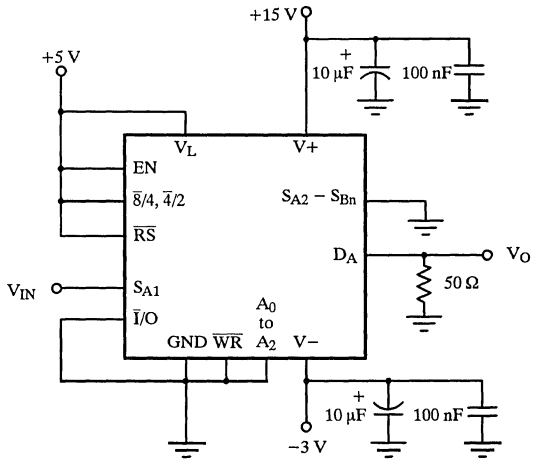


Figure 6. Bandwidth

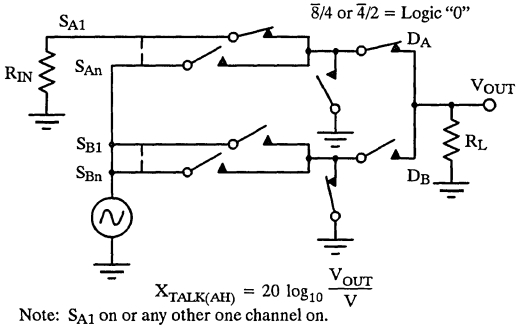


Figure 7. All Hostile Crosstalk

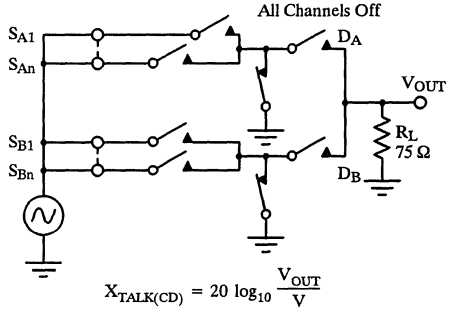


Figure 8. Chip Disabled Crosstalk

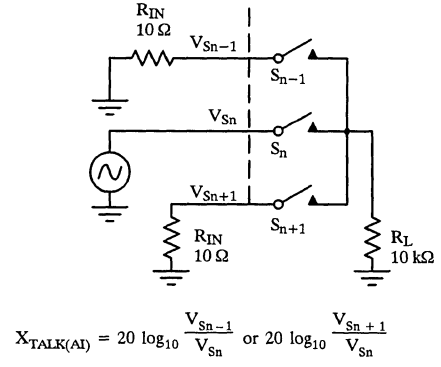


Figure 9. Adjacent Input Crosstalk

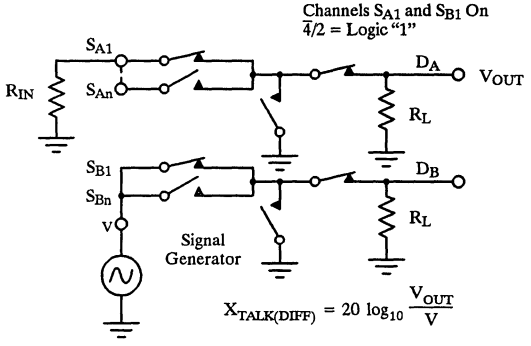


Figure 10. Differential Crosstalk

2

Test Circuits (Cont'd)

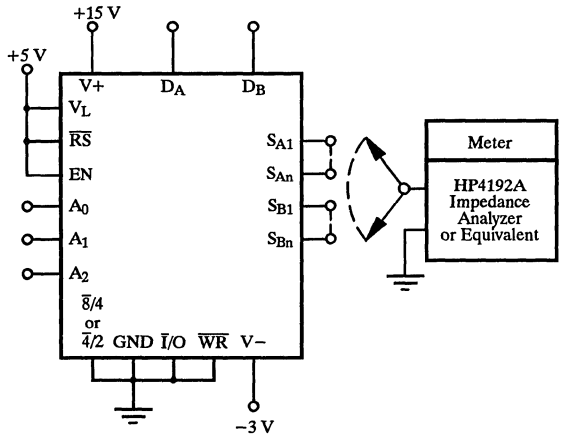


Figure 11. On State Input Capacitance

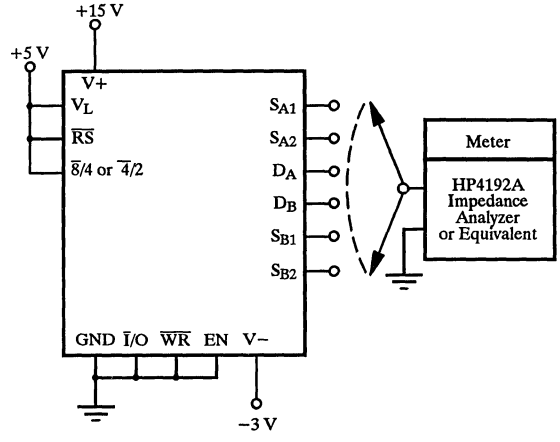
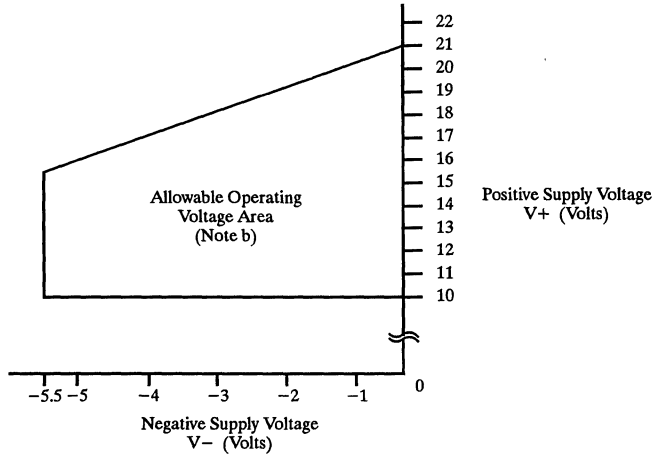


Figure 12. Off State Input/Output Capacitance

Operating Voltage Range



Notes:
a. Both V+ and V− must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10-µF tantalum bead in parallel with 100-nF ceramic disc.
b. Production tested with V+ = 15 V and V− = −3 V.
a. For V_L = 5 V ±10%, 0.8- or 2-V TTL compatibility is maintained over the entire operating voltage range.

Figure 13.

Pin Description

Symbol	Pin Number DG534A	Pin Number DG538A	Description
D_A	2	2	Analog Output/Input
V+	3	3	Positive Supply Voltage
S_{A1}	4	4	Analog Input/Output
S_{A2}	6	6	Analog Input/Output
S_{A3}	–	8	Analog Input/Output
S_{A4}	–	10	Analog Input/Output
$\overline{4}/2$	7	–	4 x 1 or 2 x 2 Select
$\overline{8}/4$	–	11	8 x 1 or 4 x 2 Select
$\overline{RS}$	8	12	Reset
$\overline{WR}$	9	13	Write command that latches A, EN
A_0, A_1, A_2	11, 10, –	16, 15, 14	Binary address inputs that determine which channel(s) is/are connected to the output(s)
EN	12	17	Enable. Input/Output, if EN = 0, all channels are open
$\overline{I}$/O	13	18	Input/Output control. Used to write to or read from the address latches
V_L	14	19	Logic Supply Voltage, usually +5 V
S_{B4}	–	20	Analog Input/Output
S_{B3}	–	22	Analog Input/Output
S_{B2}	15	24	Analog Input/Output
S_{B1}	17	26	Analog Input/Output
V–	18	27	Negative Supply Voltage
D_B	19	28	Analog Output/Input
GND	1, 5, 16	1, 5, 7, 9, 21, 23, 25	Analog and Digital Grounds. All grounds should be connected externally to optimize dynamic performance

Applications

Device Description

The DG534A/538A D/CMOS wideband multiplexers offer single-ended or differential functions. A $\overline{8}/4$ or $\overline{4}/2$ logic input pin selects the single-ended or differential mode.

To meet the high dynamic performance demands of video, high definition TV, digital data routing (in excess of 100 Mbps), etc., the DG534A/538A are fabricated with DMOS transistors configured in 'T' arrangements with second level 'L' configurations (see Functional Block Diagram).

Use of DMOS technology yields devices with very low capacitance and low $r_{DS(on)}$. This directly relates to improved high frequency signal handling and higher switching speeds, while maintaining low insertion loss figures. The 'T' and 'L' switch configurations further improve dynamic performance by greatly reducing crosstalk and output node capacitances.

The DG534A/DG538A are improved pin-compatible replacements for the non-A versions. Improvements include: higher current readback drivers, readback of the EN bit, latchup protection

Frequency Response

A single multiplexer on-channel exhibits both resistance ($r_{DS(on)}$) and capacitance ($C_{S(on)}$). This RC combination causes a frequency dependent attenuation of the analog signal. The −3-dB bandwidth of the DG534A/538A is typically 500 MHz (into 50 Ω). This figure of 500 MHz illustrates that the switch-channel cannot be represented by a simple RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi-stage network of R's and C's making up the total $r_{DS(on)}$ and $C_{S(on)}$.

Applications (Cont'd)

Power Supplies and Decoupling

A useful feature of the DG534A/538A is its power supply flexibility. It can be operated from unipolar supplies (V− connected to 0 V) if required. Allowable operating voltage ranges are shown in Figure 13.

Note that the analog signal must not go below V− by more than 0.3 V (see absolute maximum ratings). However, the addition of a V− pin has a number of advantages:

a. It allows flexibility in analog signal handling, i.e. with V− = −5 V and V+ = 15 V, up to ±5 V ac signals can be accepted.

b. The value of on capacitance ($C_{S(on)}$) may be reduced by increasing the reverse bias across the internal FET body to source junction. V+ has no effect on $C_{S(on)}$.

   It is useful to note that tests indicate that optimum video differential phase and gain occur when V− is −3 V.

c. V− eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG534/538 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

Rules:

a. Decoupling capacitors should be incorporated on all power supply pins (V+, V−, V_L).

b. They should be mounted as close as possible to the device pins.

c. Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable. Recommended decoupling capacitors are 1- to 10-µF tantalum bead, in parallel with 100-nF ceramic or polyester.

d. Additional high frequency protection may be provided by 51-Ω carbon film resistors connected in series with the power supply pins (see Figure 14).

Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG534A/538A. Some tips for minimizing stray effects are:

a. Use extensive ground planes on double sided PCB separating adjacent signal paths. Multilayer PCB is even better.

b. Keep signal paths as short as practically possible with all channel paths of near equal length.

c. Use strip-line layout techniques.

Improvements in performance can be obtained by using PLCC parts instead of DIPs. The stray effects of the quad PLCC package are lower than those of the dual-in-line packages. Sockets for the PLCC packages usually increase crosstalk.

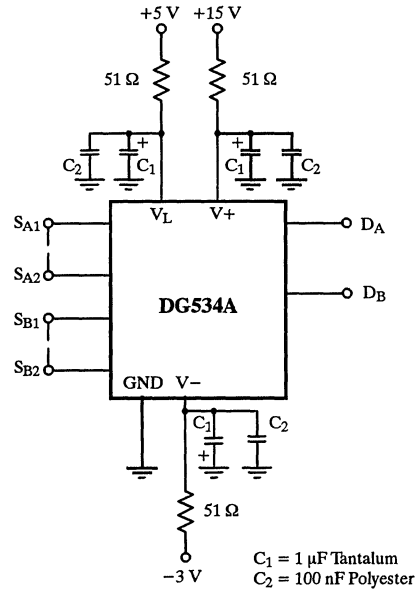


Figure 14. DG534A Power Supply Decoupling

Interfacing

Logic interfacing is easily accomplished. Comprehensive addressing and control functions are incorporated in the design.

The V_L pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to V_L. The actual logic threshold can be raised simply by increasing V_L.

A typical switching threshold versus V_L is shown in Figure 15.

These devices feature an address readback (Tally) facility, whereby the last address written to the device may be output to the system. This allows improved status monitoring and hand shaking without additional external components.

Applications (Cont'd)

This function is controlled by the $\overline{I}$/O pin, which directly addresses the tri-state buffers connected to the EN and address pins. EN and address pins can be assigned to accept data (when $\overline{I}$/O = 0; $\overline{WR}$ = 0; $\overline{RS}$ = 1), or output data (when $\overline{I}$/O = 1; $\overline{WR}$ = 1; $\overline{RS}$ = 1), or to reflect a high impedance and latched state (when $\overline{I}$/O = 0; $\overline{WR}$ = 1; $\overline{RS}$ = 1).

When $\overline{I}$/O is high, the address output can sink or source current. Note that V_L is the logic high output condition. This point must be respected if V_L is varied for input logic threshold shifting.

Further control pins facilitate easy microprocessor interface. On chip address, data latches are activated by $\overline{WR}$, which serves as a strobe type function eliminating the need for peripheral latch or memory I/O port devices. Also, for ease of interface, a direct reset function ($\overline{RS}$) allows all latches to be cleared and switches opened. Reset should be used during power up, etc., to avoid spurious switch action. See Figure 16.

Channel address data can only be entered during $\overline{WR}$ low, when the address latches are transparent and $\overline{I}$/O is low. Similarly, address readback is only operational when $\overline{WR}$ and $\overline{I}$/O are high.

The Siliconix Si582 Video amplifier is recommended as an output buffer to reduce insertion loss and to drive coaxial cables. For low power video routing applications or for unity gain input buffers Siliconix Si581/Si584 are recommended.

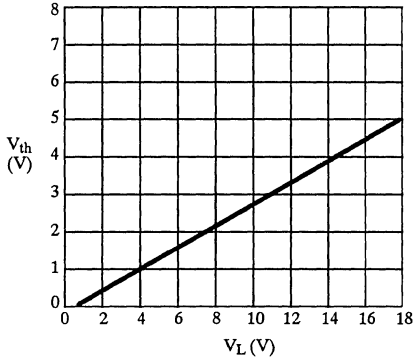


Figure 15. Switching Threshold Voltage vs. V_L

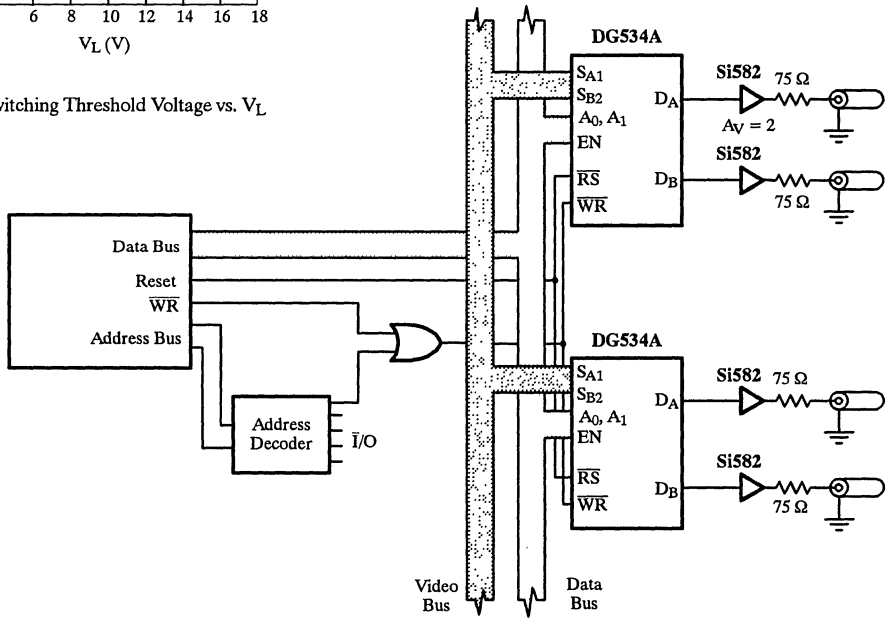


Figure 16. DG534A in a Video Matrix

Siliconix
A Member of the TEMIC Group

16-Channel Wideband Video Multiplexers

Features

- Crosstalk: −100 dB @ 5 MHz
- 300 MHz Bandwidth
- Low Input and Output Capacitance
- Low Power: 75 µW
- Low $r_{DS(on)}$: 50 Ω
- On-Board Address Latches
- Disable Output

Benefits

- High Video Quality
- Reduced Insertion Loss
- Reduced Input Buffer Requirements
- Minimizes Power Consumption
- Simplifies Bus Interface

Applications

- Video Switching/Routing
- High Speed Data Routing
- RF Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems

Description

The DG535/536 are 16-channel multiplexers designed for routing one of 16 wideband analog or digital input signals to a single output. They feature low input and output capacitance, low on-resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "off" isolation. In the on state, the switches pass signals in either direction, allowing them to be used as multiplexers or as demultiplexers.

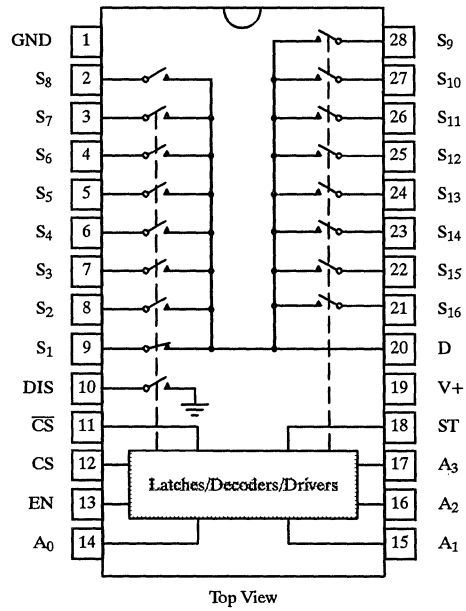
On-chip address latches and decode logic simplify microprocessor interface. Chip Select and Enable inputs simplify addressing in large matrices. Single-supply operation and a low 75-µW power consumption vastly reduces power supply requirements.

Theses devices are built on a proprietary D/CMOS process which creates low-capacitance DMOS FETs and high-speed, low-power CMOS logic on the same substrate.

For more information please refer to Siliconix Application Note AN501.

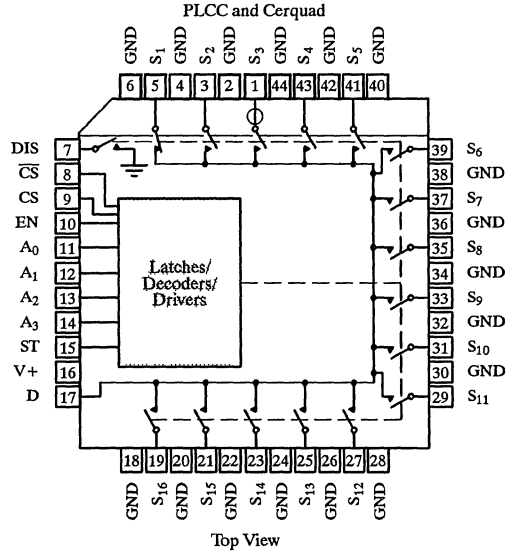
Functional Block Diagrams and Pin Configurations

DG535



Top View

DG536



Top View

Truth Tables and Ordering Information

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG535DJ
	28-Pin Sidebraze	DG535AP
		DG535AP/883
−55 to 125°C	44-Pin PLCC	DG536DN
	44-Pin Cerquad	DG536AM/883

Truth Table

EN	CS	$\overline{CS}$	ST[a]	A_3	A_2	A_1	A_0	Channel Selected	Disable[b]
0	X	X	1	X	X	X	X	None	High Z
X	0	X							
X	X	1							
1	1	0	1	0	0	0	0	S_1	Low Z
				0	0	0	1	S_2	
				0	0	1	0	S_3	
				0	0	1	1	S_4	
				0	1	0	0	S_5	
				0	1	0	1	S_6	
				0	1	1	0	S_7	
				0	1	1	1	S_8	
				1	0	0	0	S_9	
				1	0	0	1	S_{10}	
				1	0	1	0	S_{11}	
				1	0	1	1	S_{12}	
				1	1	0	0	S_{13}	
				1	1	0	1	S_{14}	
				1	1	1	0	S_{15}	
				1	1	1	1	S_{16}	
X	X	X	0	X	X	X	X	Maintains previous switch condition	High Z or Low Z

Logic "0" = $V_{AL} \leq 4.5$ V
Logic "1" = $V_{AH} \geq 10.5$ V
X = Don't Care

Notes:
a. Strobe input (ST) is level triggered.
b. Low Z, High Z = impedance of Disable Output to GND. Disable output sinks current when any channel is selected.

Absolute Maximum Ratings

V+ to GND ..... −0.3 V to +18 V
Digital Inputs ..... (GND − 0.3 V) to (V+ plus 2 V) or 20 mA, whichever occurs first
V_S, V_D ..... (GND − 0.3 V) to V+ plus 2 V) or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current (S or D) Pulsed 1 ms 10% duty cycle ..... 40 mA
Storage Temperature (A Suffix) ..... −65 to 150°C
(D Suffix) ..... −65 to 125°C
Power Dissipation (Package)[a]
28-Pin Plastic DIP[b] ..... 625 mW
28-Pin Sidebraze[c] ..... 1200 mW
44-Pin PLCC[d] ..... 450 mW
44-Pin Cerquad[e] ..... 825 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 8.6 mW/°C above 75°C.
c. Derate 16 mW/°C above 75°C.
d. Derate 6 mW/°C above 75°C.
e. Derate 11 mW/°C above 75°C.

2

Specifications[a]

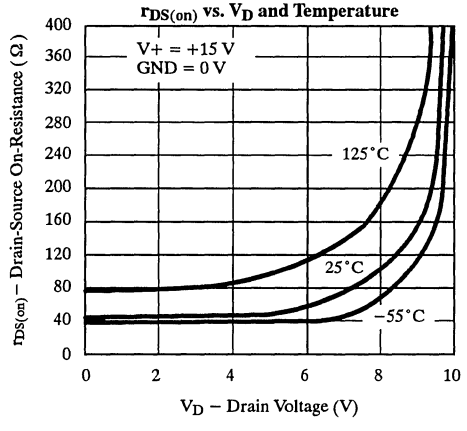
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, ST, CS = 10.5 V $\overline{CS}$ = 4.5 V, V_A = 4.5 or 10.5 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[c]	A Suffix −55 to 125°C Max[c]	D Suffix −40 to 85°C Min[c]	D Suffix −40 to 85°C Max[c]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	10	0	10	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −1 mA, V_D = 3 V EN = 10.5 V Sequence Each Switch On		Room Full	55		90 120		90 120	Ω
Resistance Match	$\Delta r_{DS(on)}$			Room			9		9	
Source Off Leakage Current	$I_{S(off)}$	V_S = 3 V, V_D = 0 V, EN = 4.5 V		Room Full		−10 −100	10 100	−10 −100	10 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 3 V, EN = 10.5 V		Room Full		−10 −1000	10 1000	−10 −100	−10 −100	
Disable Output	$R_{DISABLE}$	$I_{DISABLE}$ = 1 mA, EN = 10.5 V		Room Full	100		200 250		200 250	Ω
Digital Control										
Input Voltage High	V_{AIH}			Full		10.5		10.5		V
Input Voltage Low	V_{AIL}			Full			4.5		4.5	
Address Input Current	I_{AI}	V_A = GND or V+		Room Full	<0.01	−1 −100	1 100	−1 −100	1 100	µA
Address Input Capacitance	C_A			Full	5					pF
Dynamic Characteristics										
On State Input Capacitance[e]	$C_{S(on)}$	V_D = V_S = 3 V	PLCC	Room	32		45		45	pF
			Cerquad	Room	35					
			DIP	Room	40		55		55	
Off State Input Capacitance[e]	$C_{S(off)}$	V_S = 3 V	PLCC	Room	2		8		8	
			Cerquad	Room	5					
			DIP	Room	3					
Off State Output Capacitance[e]	$C_{D(off)}$	V_D = 3 V	PLCC	Room	8		20		20	
			Cerquad	Room	12					
			DIP	Room	9					
Multiplexer Switching Time	t_{TRANS}	See Figure 4		Full			300		300	ns
Break-Before-Make Interval	t_{OPEN}			Full		25		25		
EN, CS, $\overline{CS}$, ST, t_{ON}	t_{ON}	See Figure 2 and 3		Full			300		300	
EN, CS, $\overline{CS}$, ST, t_{OFF}	t_{OFF}	See Figure 2		Full			150		150	
Charge Injection	Q	See Figure 5		Room	−35					pC
Single-Channel Crosstalk	$X_{TALK(SC)}$	R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz See Figure 9	PLCC	Room	−100					dB
			Cerquad	Room	−93					
			DIP	Room	−60					
Chip Disabled Crosstalk	$X_{TALK(CD)}$	R_{IN} = R_L = 75 Ω f = 5 MHz, EN = 4.5 V See Figure 8	PLCC	Room	−85					
			Cerquad	Room	−84					
			DIP	Room	−60					

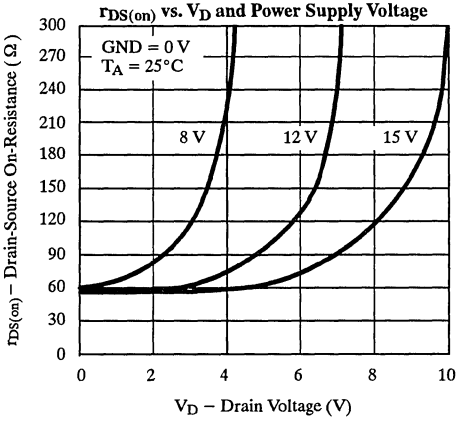
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, ST, CS = 10.5 V $\overline{CS}$ = 4.5 V, V_A = 4.5 or 10.5 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[c]	A Suffix −55 to 125°C Max[c]	D Suffix −40 to 85°C Min[c]	D Suffix −40 to 85°C Max[c]	Unit
Dynamic Characteristics (Cont'd)										
Adjacent Input Crosstalk	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz See Figure 10	PLCC	Room	−92					dB
			Cerquad	Room	−87					
			DIP	Room	−72					
All Hostile Crosstalk[e]	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz See Figure 7	PLCC	Room	−74	−60		−60		
			Cerquad	Room	−74					
			DIP	Room	−60					
Bandwidth	BW	R_L = 50 Ω, See Figure 6		Room	500					MHz
Power Supplies										
Positive Supply Current	I+	Any One Channgel Selected with All Logic Inputs at GND or V+		Room Full	5		50 100		50 100	µA
Supply Voltage Range	V+			Full		10	16.5	10	16.5	V
Minimum Input Timing Requirements										
Strobe Pulse Width	t_{SW}	See Figure 1		Full		200		200		ns
A_0, A_1, A_2, A_3 CS, $\overline{CS}$, EN Data Valid to Strobe	t_{DW}			Full		100		100		
A_0, A_1, A_2, A_3 CS, $\overline{CS}$, EN Data Valid after Strobe	t_{WD}			Full		50		50		

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_A = input voltage to perform proper function.

Typical Characteristics

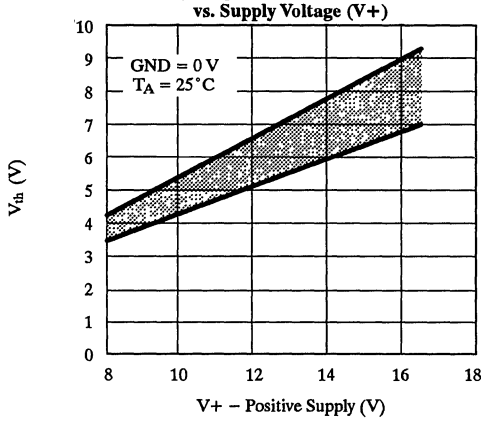




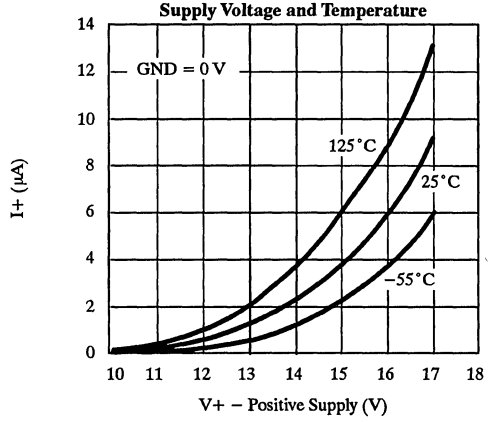
2

Typical Characteristics (Cont'd)

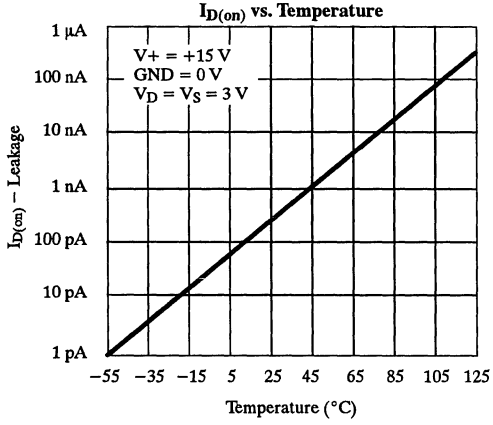
Logic Input Switching Threshold vs. Supply Voltage (V+)



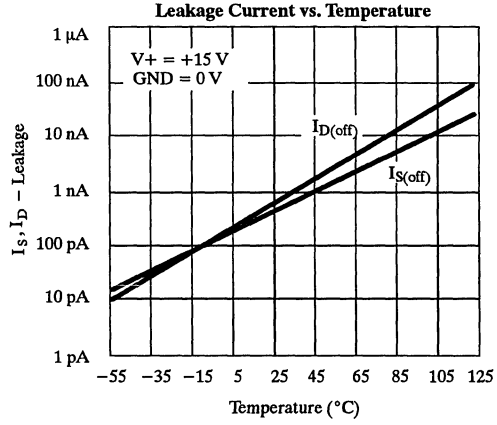
Supply Current vs. Supply Voltage and Temperature



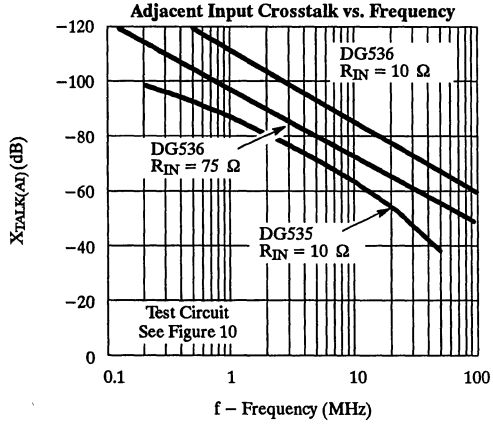
$I_{D(on)}$ vs. Temperature



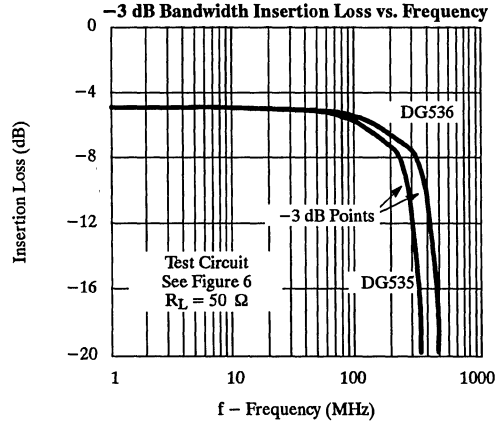
Leakage Current vs. Temperature



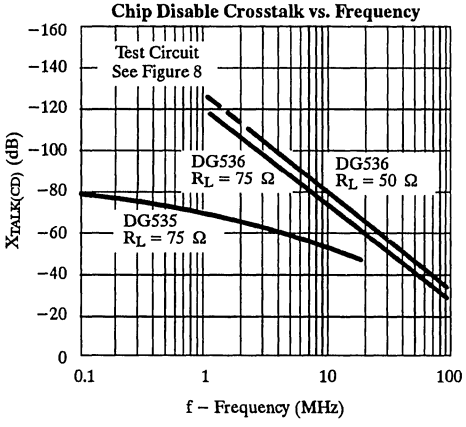
Adjacent Input Crosstalk vs. Frequency

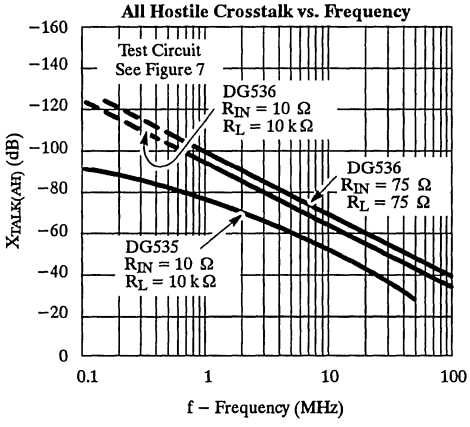


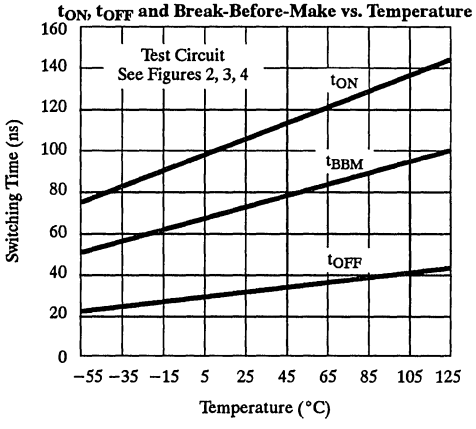
–3 dB Bandwidth Insertion Loss vs. Frequency

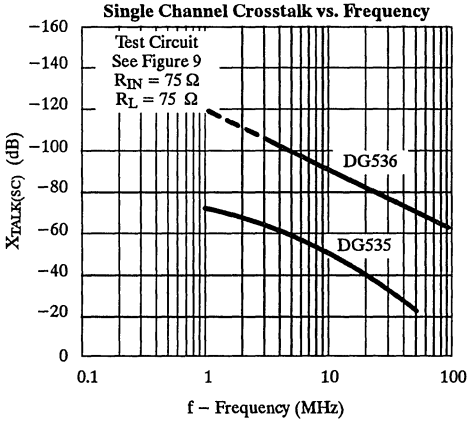


Typical Characteristics (Cont'd)









Input Timing Requirements

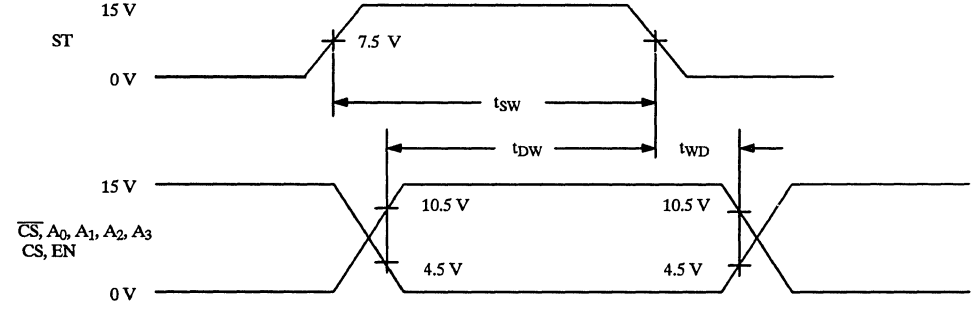


Figure 1.

Test Circuits

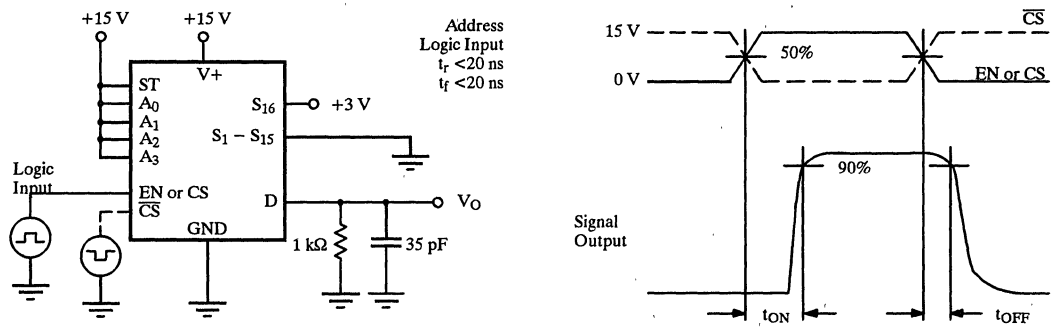


Figure 2. EN, CS, $\overline{CS}$, Turn On/Off Time

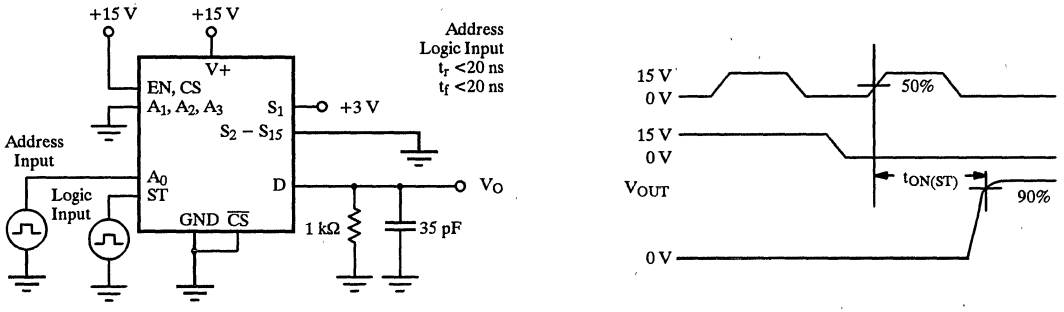


Figure 3. Strobe ST Turn On Time

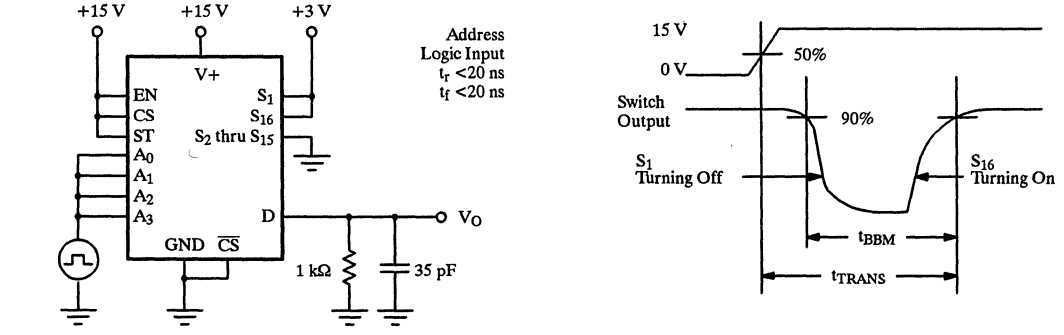
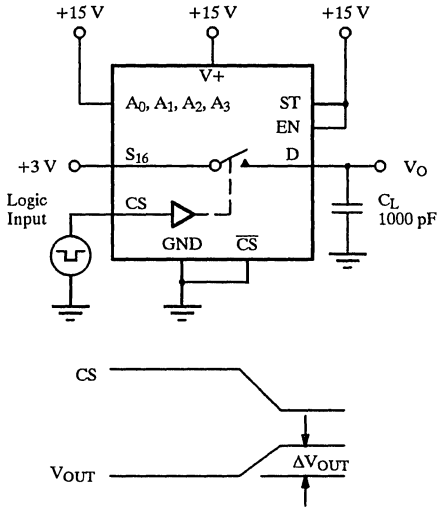


Figure 4. Transition Time and Break-Before-Make Interval

Test Circuits (Cont'd)



ΔV_{OUT} is the measured voltage error due to charge injection. The charge injection in Coulombs is $Q = C_L \times \Delta V_{OUT}$

Figure 5. Charge Injection

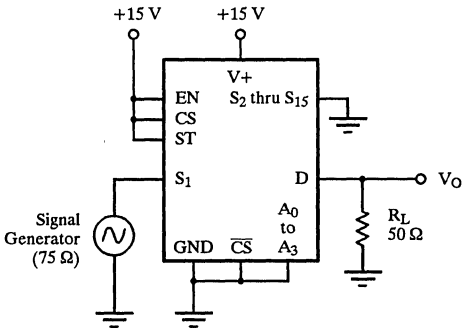


Figure 6. Bandwidth

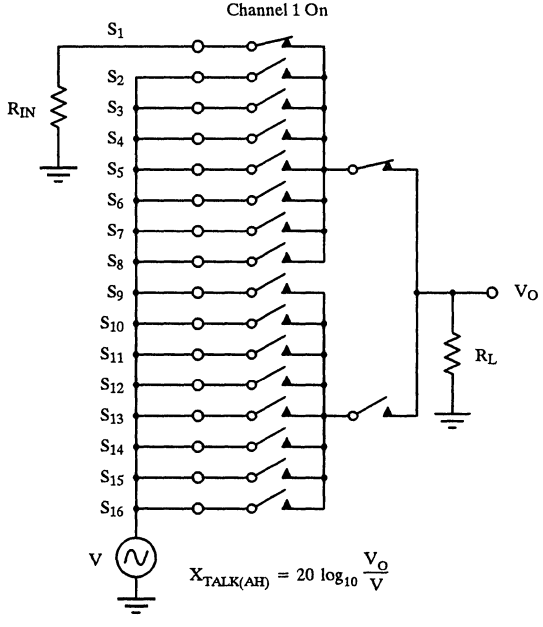


Figure 7. All Hostile Crosstalk

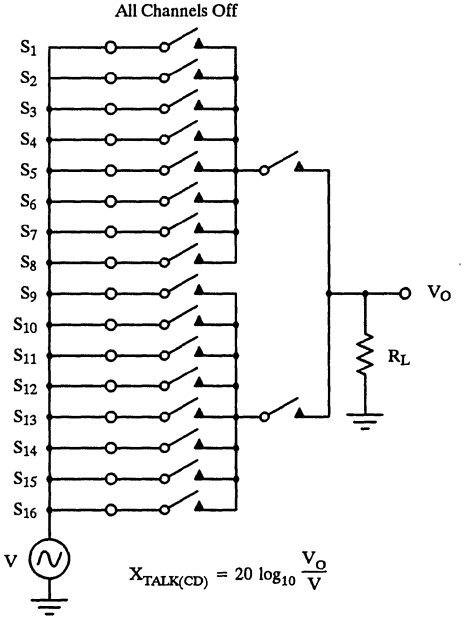
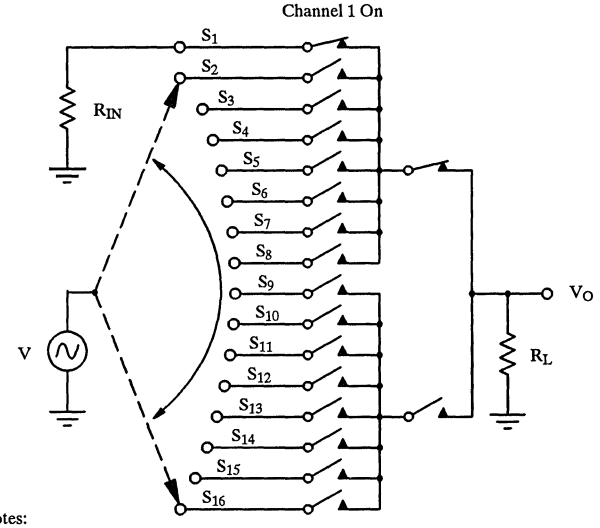


Figure 8. Chip Disabled Crosstalk

2

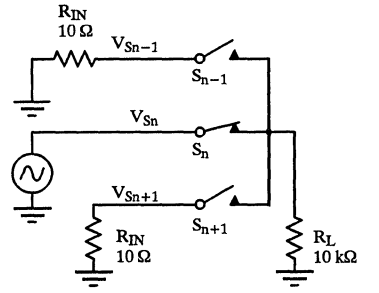
Test Circuits (Cont'd)



Notes:

1. Any individual channel between S_2 and S_{16} can be selected
2. $X_{TALK(SC)} = 20 \log_{10} \frac{V_O}{V}$ is scanned sequentially from S_2 to S_{16}

Figure 9. Single Channel Crosstalk



$$X_{TALK(AI)} = 20 \log_{10} \frac{V_{Sn-1}}{V_{Sn}} \text{ or } 20 \log_{10} \frac{V_{Sn+1}}{V_{Sn}}$$

Figure 10. Adjacent Input Crosstalk

Pin Description

Symbol	Description
S_1 thru S_{16}	Analog inputs/outputs
D	Multiplexer output/demultiplexer input
DIS	Open drain low impedance to analog ground when any channel is selected
$\overline{CS}$, CS, EN	Logic inputs to selected desired multiplexer(s) when using several multiplexers in a system
A_0 thru A_3	Binary address inputs to determine which channel is selected
ST	Strobe input that latches A_0, A_1, A_2, A_3, $\overline{CS}$, CS, EN
V+	Positive supply voltage input
GND	Analog signal ground and most negative potential **All ground pins should be connected externally to ensure dynamic performance**

Detailed Description

The DG535/536 are 16-channel single-ended multiplexers with on-chip address logic and control latches.

The multiplexer connects one of sixteen inputs (S_1, S_2 through S_{16}) to a common output (D) under the control of a 4-bit binary address (A_0 to A_3). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of three independent logic inputs (EN, CS and $\overline{CS}$) are provided on chip. These inputs are gated together (see Figure 11) and only when EN = CS = 1 and $\overline{CS}$ = 0 can an output switch be selected. This necessary logic condition is then latched-in when Strobe (ST) goes low.

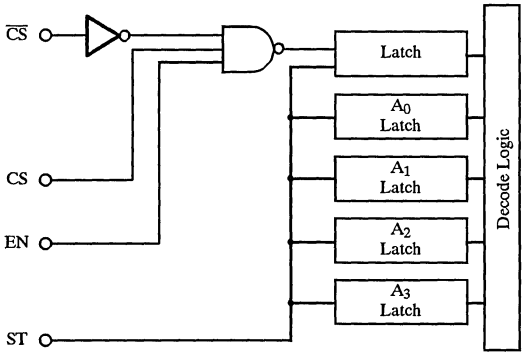


Figure 11. $\overline{CS}$, CS, EN, ST Control Logic

Break-before-make switching prevents momentary shorting when changing from one input to another.

The devices feature a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method SW_2 operates out of phase with SW_1 and SW_3. In the on condition SW_1 and SW_3 are closed with SW_2 open whereas in the off condition SW_1 and SW_3 are open and SW_2 closed. In the off condition the input to SW_3 is effectively the isolation leakage of SW_1 working into the on-resistance of SW_2 (typically 200 Ω).

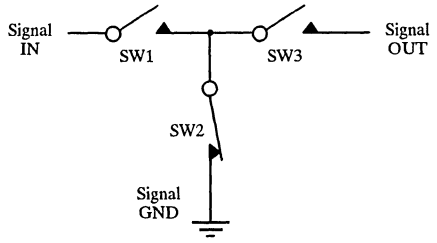


Figure 12. "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535/536 have extensive applications where any high frequency video or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using n-channel DMOS FETs for the "T" and series switches.

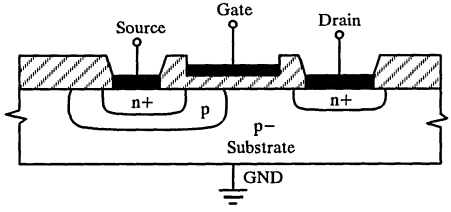


Figure 13. Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e., 20 mA).

Detailed Description (Cont'd)

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS drain terminal (see Figure 13) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

DC Biasing

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing may be necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to ±200 mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.

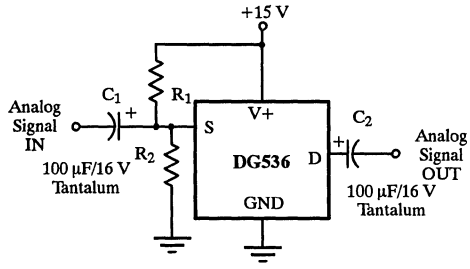


Figure 14. Simple Bias Circuit

R_1 and R_2 are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor C_1 blocks the dc bias voltage from being coupled back to the analog signal source and C_2 blocks the dc bias from the output signal. Both C_1 and C_2 should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies.

Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method is to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

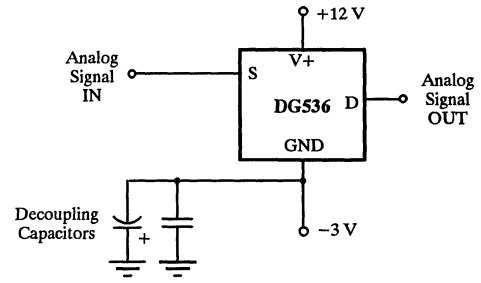


Figure 15. DG536 with Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

Circuit Layout

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.

8 × 4 Wideband Video Crosspoint Array

Features

- Routes Any Input to Any Output
- Wide Bandwidth: 300 MHz
- Low Crosstalk: −85 dB @ 5 MHz
- Double Buffered TTL-Compatible Latches with Readback
- Low $r_{DS(on)}$: 45 Ω
- Optional Negative Supply

Benefits

- Reduced Board Space
- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- High Reliability

Applications

- Wideband Signal Routing and Multiplexing
- High-End Video Systems
- NTSC, PAL, SECAM Switchers
- Digital Video Routing
- ATE Systems

Description

The DG884 contains a matrix of 32 T-switches configured in an 8 × 4 crosspoint array. Any of the IN/OUT pins may be used as an input or output. Any of the IN pins may be switched to any or simultaneously to all OUT pins.

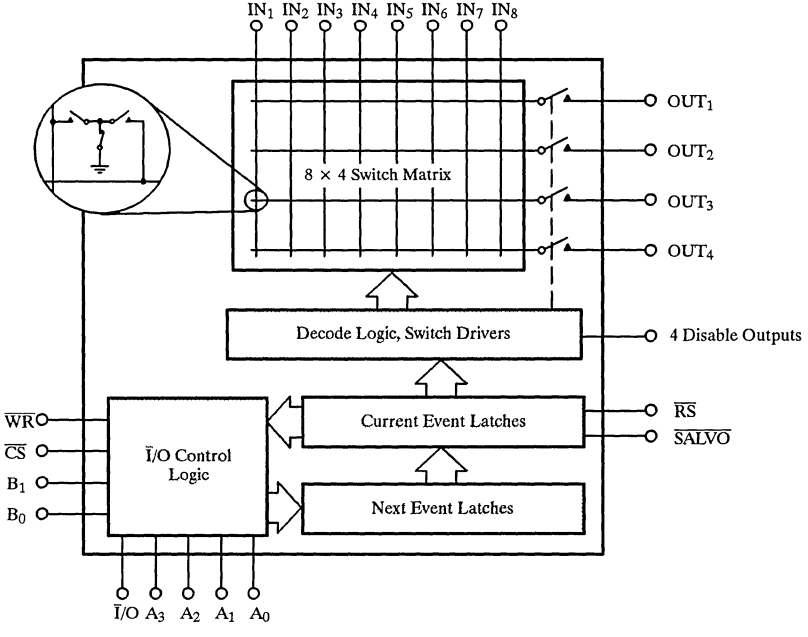
The DG884 is built on a proprietary D/CMOS process that combines low capacitance switching DMOS FETs with low power CMOS control logic and drivers. The ground lines between adjacent signal input pins help to reduce crosstalk. The low on-resistance and low on-capacitance of the DG884 make it ideal for video and wideband signal routing.

Control data is loaded individually into four Next Event latches. When all Next Event latches have been programmed, data is transferred into the Current Event latches via a SALVO command. Current Event latch data readback is available to poll array status.

Output disable capabilities make it possible to parallel multiple DG884s to form larger switch arrays. DIS outputs provide control signals used to place external buffers in a power saving mode.

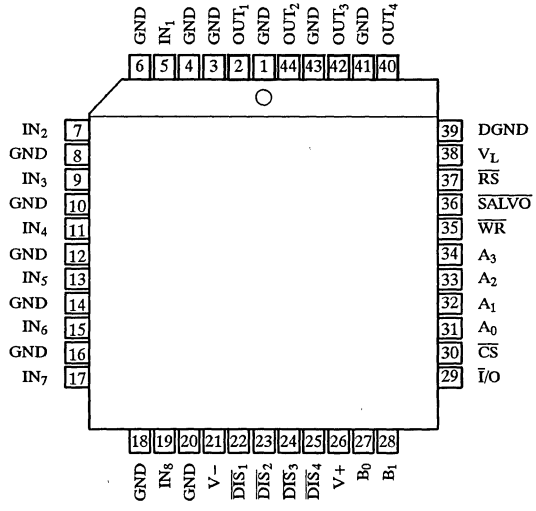
For additional information please refer to AN504.

Functional Block Diagram



Pin Configuration

PLCC and CLCC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	44-Pin PLCC	DG884DN
−55 to 125°C	44-Pin CLCC	DG884AM/883

Truth Tables

$\overline{RS}$	$\overline{I/O}$	$\overline{CS}$	$\overline{WR}$	$\overline{SALVO}$	Actions
1	0	1	↓	1	No change to Next Event latches
1	0	0	↓	1	Next Event latches loaded as defined in table below
1	0	0	0	1	Next Event latches are transparent.
1	0	0	↑	1	Next Event data latched-in
1	0	X	1	↓	Data in all Next Event latches is simultaneously loaded into the Current Event latches, i.e., all new crosspoint addresses change simultaneously when $\overline{SALVO}$ goes low.
1	0	0	X	0	Current Event latches are transparent
1	0	X	1	↑	Current Event data latched-in
1	0	0	0	0	Both next and Current Event latches are transparent
1	1	1	1	1	A_0, A_1, A_2, A_3 – High impedance
1	1	0	1	1	A_0, A_1, A_2, A_3 become outputs and reflect the contents of the Current Event latches. B_0, B_1 determine which Current Event latches are being read
0	X	X	1	1	All crosspoints opened (but data in Next Event latches is preserved)

All other states are not recommended.

Truth Tables (Cont'd)

$\overline{WR}$	B_1	B_0	A_3	A_2	A_1	A_0	Next Event Latches
0	0	0	1	0	0	0	IN_1 to OUT_1 Loaded
				0	0	1	IN_2 to OUT_1 Loaded
				0	1	0	IN_3 to OUT_1 Loaded
				0	1	1	IN_4 to OUT_1 Loaded
				1	0	0	IN_5 to OUT_1 Loaded
				1	0	1	IN_6 to OUT_1 Loaded
				1	1	0	IN_7 to OUT_1 Loaded
				1	1	1	IN_8 to OUT_1 Loaded
			0	X	X	X	Turn Off OUT_1 Loaded
	0	1	1	0	0	0	IN_1 to OUT_2 Loaded
				0	0	1	IN_2 to OUT_2 Loaded
				0	1	0	IN_3 to OUT_2 Loaded
				0	1	1	IN_4 to OUT_2 Loaded
				1	0	0	IN_5 to OUT_2 Loaded
				1	0	1	IN_6 to OUT_2 Loaded
				1	1	0	IN_7 to OUT_2 Loaded
				1	1	1	IN_8 to OUT_2 Loaded
			0	X	X	X	Turn Off OUT_2 Loaded
	1	0	1	0	0	0	IN_1 to OUT_3 Loaded
				0	0	1	IN_2 to OUT_3 Loaded
				0	1	0	IN_3 to OUT_3 Loaded
				0	1	1	IN_4 to OUT_3 Loaded
				1	0	0	IN_5 to OUT_3 Loaded
				1	0	1	IN_6 to OUT_3 Loaded
				1	1	0	IN_7 to OUT_3 Loaded
				1	1	1	IN_8 to OUT_3 Loaded
			0	X	X	X	Turn Off OUT_3 Loaded
	1	1	1	0	0	0	IN_1 to OUT_4 Loaded
				0	0	1	IN_2 to OUT_4 Loaded
				0	1	0	IN_3 to OUT_4 Loaded
				0	1	1	IN_4 to OUT_4 Loaded
				1	0	0	IN_5 to OUT_4 Loaded
				1	0	1	IN_6 to OUT_4 Loaded
				1	1	0	IN_7 to OUT_4 Loaded
				1	1	1	IN_8 to OUT_4 Loaded
			0	X	X	X	Turn Off OUT_4 Loaded

Note: When $\overline{WR}$ = 0 Next Event latches are transparent. Each crosspoint is addressed individually, e.g., to connect IN_1 to OUT_1 thru OUT_4 requires A_0, A_1, A_2 = 0 to be latched with each combination of B_0, B_1. When $\overline{RS}$ = 0, all four $\overline{DIS}$ outputs pull low simultaneously.

Absolute Maximum Ratings

V+ to GND ..... −0.3 V to 21 V

V+ to V− ..... −0.3 V to 21 V

V− to GND ..... −10 V to 0.3 V

V_L to GND ..... 0 V to (V+) + 0.3 V

Digital Inputs ..... (V−) − 0.3 V to (V_L) + 0.3 V
or 20 mA, whichever occurs first

V_S, V_D ..... (V−) − 0.3 V to (V−) + 14 V
or 20 mA, whichever occurs first

CURRENT (any terminal) Continuous ..... 20 mA

CURRENT (S or D) Pulsed 1 ms 10% duty ..... 40 mA

Storage Temperature (A Suffix) ..... −65 to 150°C
(D Suffix) ..... −65 to 125°C

Operating Temperature (A Suffix) ..... −55 to 125°C
(D Suffix) ..... −40 to 85°C

Power Dissipation (Package)[a]

44-Pin Quad J Lead PLCC[b] ..... 450 mW

44-Pin Quad J Lead Hermetic CLCC[c] ..... 1200 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 6 mW/°C above 75°C.
c. Derate 16 mW/°C above 75°C.

2

Specifications[a]

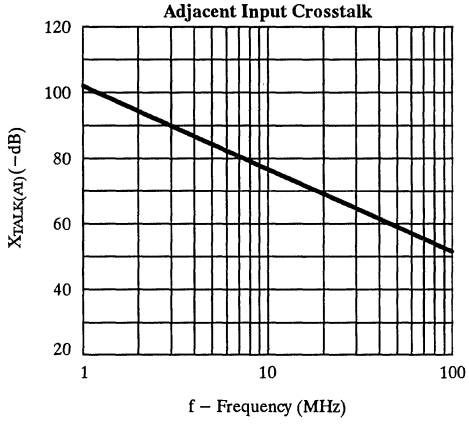
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_L = 5 V, $\overline{RS}$ = 2.0 V $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, I/O = 0.8 V	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}	V− = −5 V	Full		−5	8	−5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 0 V V_{AIH} = 2.0 V, V_{AIL} = 0.8 V Sequence Each Switch On	Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$		Room	3		9		9	
Source Off Leakage Current	$I_{S(off)}$	V_S = 8 V, V_D = 0 V, $\overline{RS}$ = 0.8 V	Room Full		−20 −200	20 200	−20 −200	20 200	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 0 V, V_D = 8 V, $\overline{RS}$ = 0.8 V	Room Full		−20 −200	20 200	−20 −200	20 200	
Total Switch On Leakage Current	$I_{D(on)}$	V_S = V_D = 8 V	Room Full		−20 −2000	20 2000	−20 −200	20 200	
Digital Input/Output									
Input Voltage High	V_{AIH}		Full		2		2		V
Input Voltage Low	V_{AIL}		Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V or 2 V or 5 V	Room Full	0.1	−1 −10	1 10	−1 −10	1 10	µA
Address Output Current	I_{AO}	V_{AO} = 2.7 V, See Truth Table	Room	−600		−200		−200	
		V_{AO} = 0.4 V, See Truth Table	Room	1500	500		500		
$\overline{DIS}$ Pin Sink Current	I_{DIS}		Room	1.5					mA
Dynamic Characteristics									
On State Input Capacitance[e]	$C_{S(on)}$	1 In to 1 Out, See Figure 11	Room	30				40	pF
		1 In to 4 Out, See Figure 11	Room	120				160	
Off State Input Capacitance[e]	$C_{S(off)}$	See Figure 11	Room	8		20		20	
Off State Output Capacitance[e]	$C_{D(off)}$		Room	10		20		20	
Transition Time	t_{TRANS}	See Figure 5	Room					300	ns
Break-Before-Make Interval	t_{OPEN}		Full			10		10	
$\overline{SALVO}$, $\overline{WR}$ Turn On Time	t_{ON}	R_L= 1 kΩ, C_L = 35 pF 50% Control to 90% Output See Figure 3	Room Full			300 500		300	
$\overline{SALVO}$, $\overline{WR}$ Turn Off Time	t_{OFF}		Room Full			175 300		175	
Charge Injection	Q	See Figure 6	Room	−100					pC
Matrix Disabled Crosstalk	$X_{TALK(DIS)}$	R_{IN} = R_L = 75 Ω f = 5 MHz, See Figure 10	Room	−82					dB
Adjacent Input Crosstalk	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz, See Figure 9	Room	−85					
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz, See Figure 8	Room	−66					
Bandwidth	BW	R_L = 50 Ω, See Figure 7	Room	300					MHz

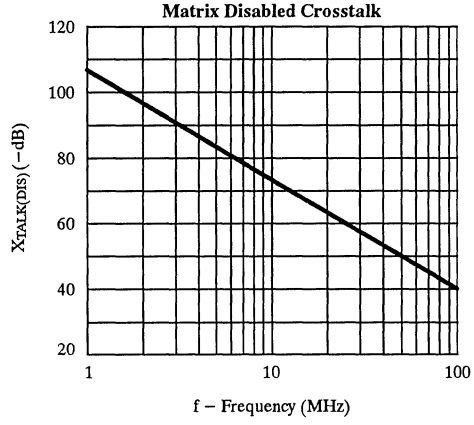
Specifications[a]

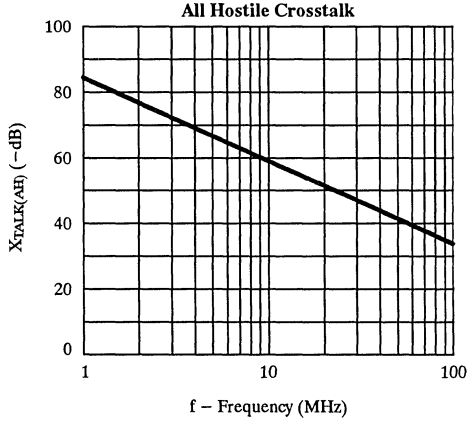
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −3 V V_L = 5 V, $\overline{RS}$ = 2.0 V $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, $\overline{I}$/O = 0.8 V	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	All Inputs At GND or 2 V $\overline{RS}$ = 2 V	Room Full	1.5		3 6		3 6	mA
Negative Supply Current	I−		Room Full	−1.5	−3 −5		−3 −5		
Digital GND Supply Current	I_{DG}		Full	−275	−750		−750		µA
Logic Supply Current	I_L		Full	200		500		500	
Functional Operating Supply Voltage Range[e]	V+ to V−	See Operating Voltage Range (Typical Characteristics) page 2-118	Full		13	20	13	20	V
	V− to GND		Full		−5.5	0	−5.5	0	
	V+ to GND		Full		10	20	10	20	
Minimum Input Timing Requirements									
Address Write Time	t_{AW}	See Figure 1	Full	20	50		50		ns
Minimum $\overline{WR}$ Pulse Width	t_{WP}		Full	50	100		100		
Write Address Time	t_{WA}		Full	−10	10		10		
Chip Select Write Time	t_{CW}		Full	50	100		100		
Write Chip Select Time	t_{WC}		Full	25	75		75		
Minimum $\overline{SALVO}$ Pulse Width	t_{SP}		Full	50	100		100		
SALVO Write Time	t_{SW}		Full	−10	10		10		
Write SALVO Time	t_{WS}		Room	20			50		
Input Output Time	t_{IO}		Room	150	200		200		
Address Output Time	t_{AO}		Room	150	200		200		
Chip Select Output Time	t_{CO}		Room	150	200		200		
Chip Select Address Time	t_{CA}		Room	60			100		
Reset to $\overline{SALVO}$	t_{RS}		Full		50		50		
$\overline{I}$/O Address Input Time	t_{IA}		Room	50					

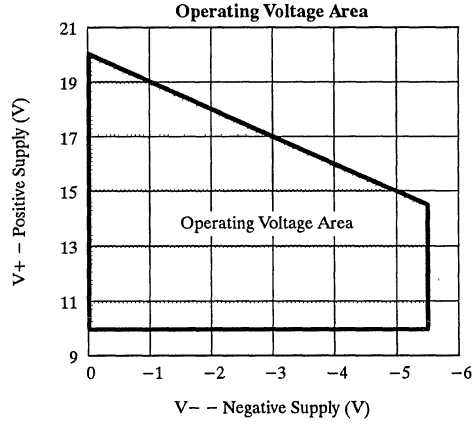
Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.

Typical Characteristics









Timing Diagrams and Parameter Definitions

Symbol	Parameter	Description
T_{AW}	Address to Write	Minimum time address must be valid before $\overline{WR}$ goes high
T_{WA}	Write to Address	Minimum time address must remain valid after $\overline{WR}$ pulse goes high
T_{WP}	$\overline{WR}$ Pulse	Minimum time of $\overline{WR}$ pulse width to write address into Next Event latches
T_{CW}	Chip Select to $\overline{WR}$	Minimum time chip select must be valid before a $\overline{WR}$ pulse
T_{WC}	$\overline{WR}$ to Chip Select	Minimum time chip select must remain valid after $\overline{WR}$ pulse
T_{SP}	$\overline{SALVO}$ Pulse	Minimum time of $\overline{SALVO}$ pulse width
T_{WS}	$\overline{WR}$ to $\overline{SALVO}$	Minimum time from $\overline{WR}$ pulse to $\overline{SALVO}$ to load new address
T_{SW}	$\overline{SALVO}$ to $\overline{WR}$	Minimum time from $\overline{SALVO}$ pulse to $\overline{WR}$ to load current address
T_{IA}	I/O to Address In	Minimum time I/O must be valid before address applied

Timing Diagrams and Parameter Definitions (Cont'd)

Symbol	Parameter	Description
T_{RS}	$\overline{RS}$ to $\overline{SALVO}$	Minimum time $\overline{RS}$ must be valid before $\overline{SALVO}$ pulse
T_{IO}	$\overline{I}$/O to Output	Minimum time $\overline{I}$/O must be valid before address output valid
T_{AO}	Address to Output	Minimum time address B_X must be valid until address A_X output valid
T_{CO}	$\overline{CS}$ to Output	Minimum time $\overline{CS}$ must be valid until A_X output is valid
T_{CA}	$\overline{CS}$ to Address In	Minimum time $\overline{CS}$ must be valid before address applied if $\overline{I}$/O is high

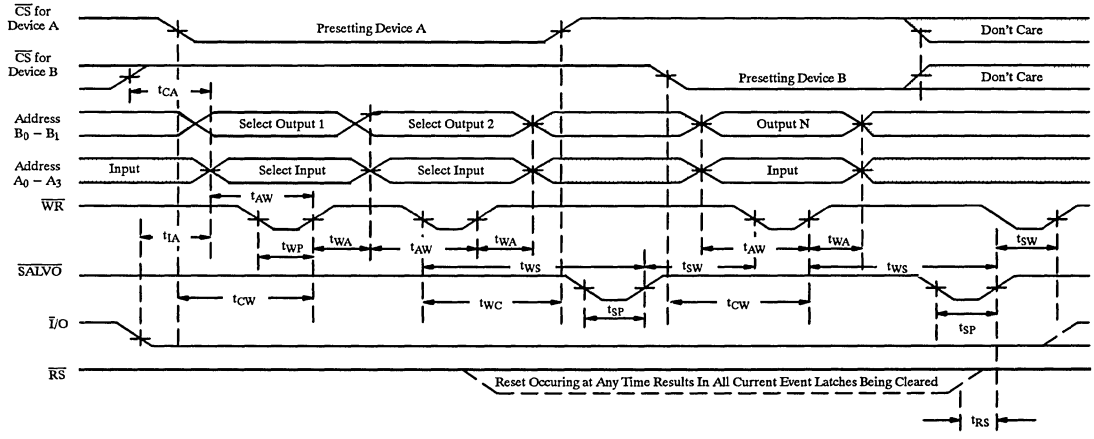


Figure 1. Input Timing Requirements

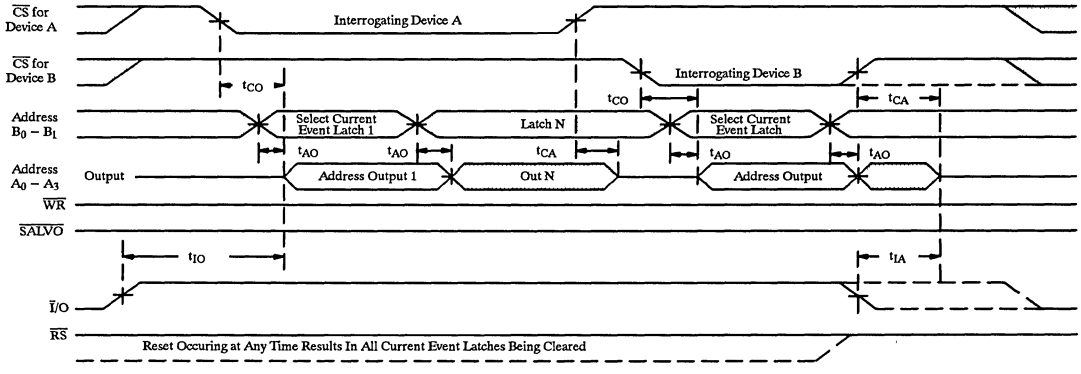


Figure 2. Output Timing Requirements

Test Circuits

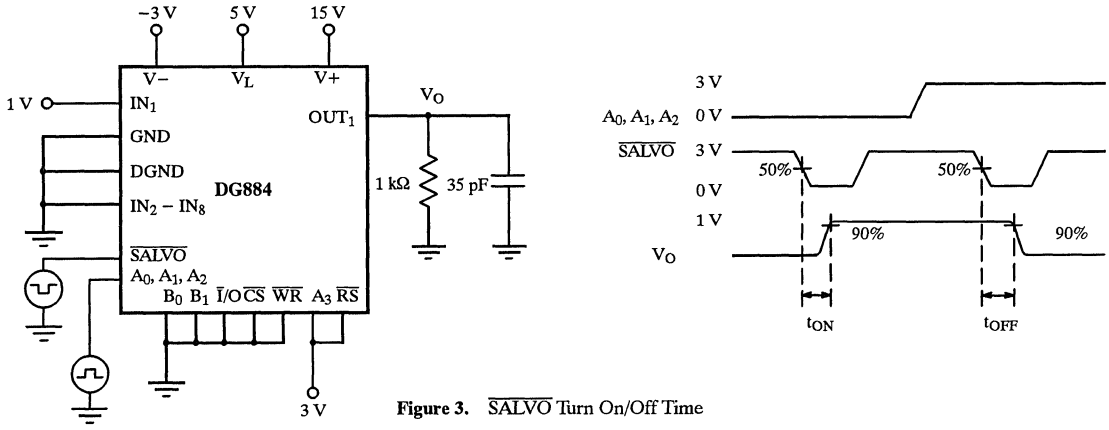


Figure 3. $\overline{\text{SALVO}}$ Turn On/Off Time

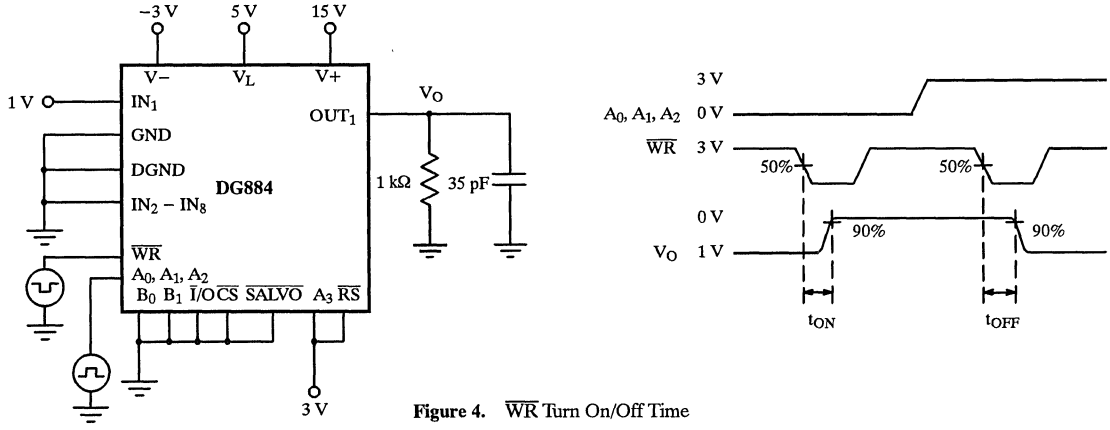


Figure 4. $\overline{\text{WR}}$ Turn On/Off Time

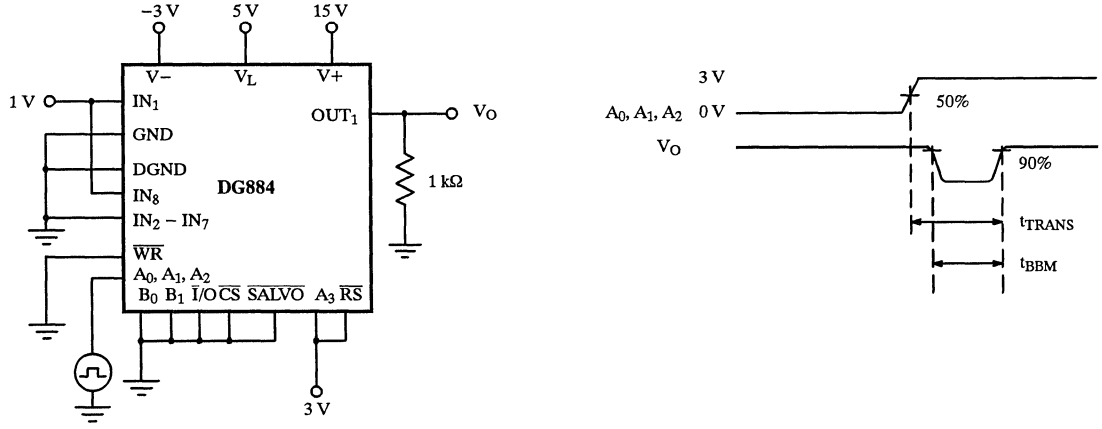


Figure 5. Transition Time and Break-Before-Make Interval

Test Circuits

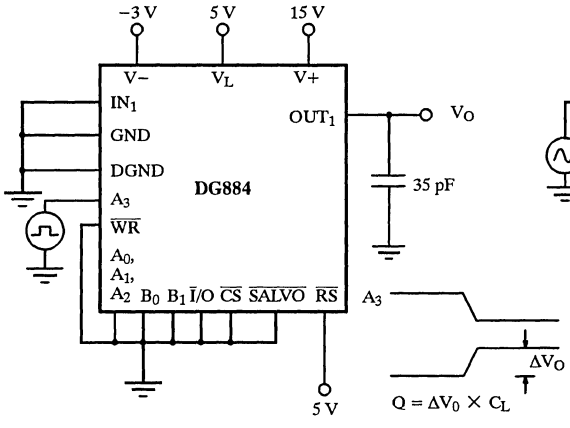


Figure 6. Charge Injection

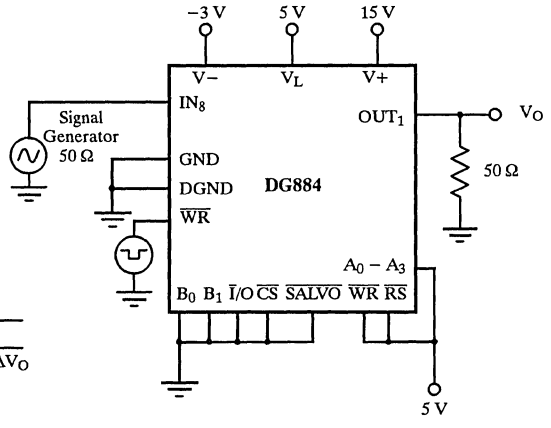


Figure 7. −3 dB Bandwidth

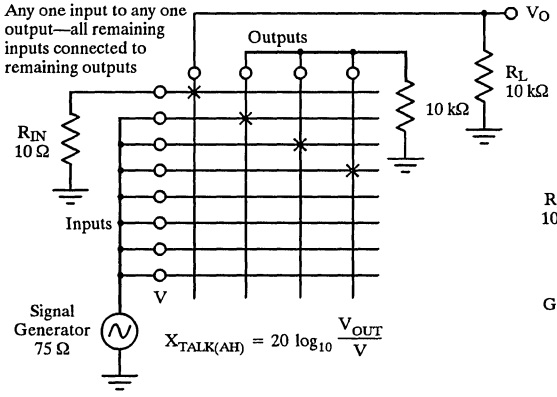


Figure 8. All Hostile Crosstalk

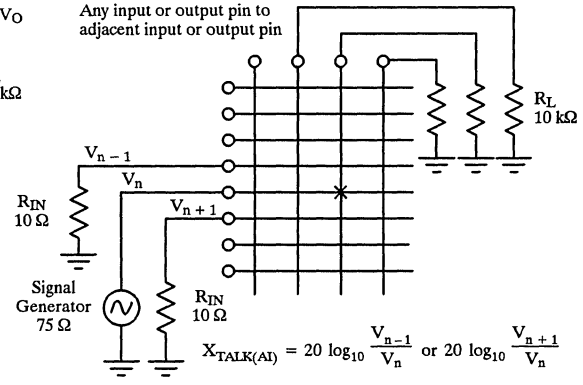


Figure 9. Adjacent Input Crosstalk

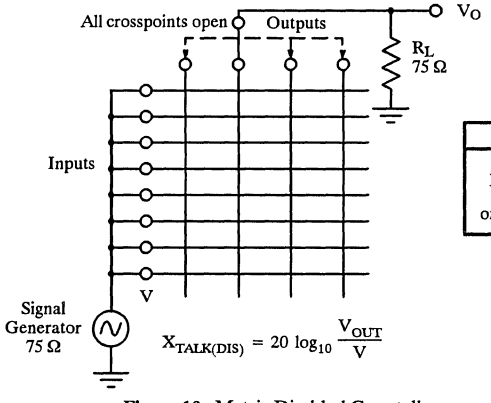


Figure 10. Matrix Disabled Crosstalk

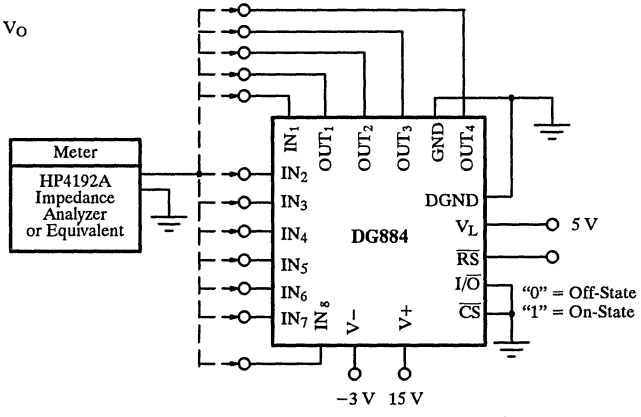


Figure 11. On-State and Off-State Capacitances

2

Pin Description

Pin	Symbol	Description
1, 3, 4, 6, 8, 10, 12, 14, 16, 18, 20, 41, 43	GND	Analog Signal Ground
39	DGND	Digital Ground
26	V+	Positive Supply Voltage
21	V−	Negative Supply Voltage
38	V_L	Logic Supply Voltage—generally 5 V
5, 7, 9, 11, 13, 15, 17, 19	IN_1 to IN_8	8 Analog Input Channels
2, 40, 42, 44	OUT_1 to OUT_4	4 Analog Output Channels
29	$\overline{I/O}$	Determines whether data is being written into the Next Event latches or read from the Current Event latches
30	$\overline{CS}$	Chip Select—a logic input
31, 32, 22, 24	A_0, A_1, A_2, A_3	IN Address—logic inputs or outputs as defined by $\overline{I/O}$ pin, select one of eight IN channels
27, 28	B_0, B_1	OUT Address—logic inputs, select one of four OUT channels
35	$\overline{WR}$	Write command that latches A_0, A_1, A_2, A_3 into the Next Event latches
36	$\overline{SALVO}$	Master write command, that in one action, transfers all the data from Next Event latches into Current Event latches
37	$\overline{RS}$	Reset—a low will clear the Current Event latches
22, 23, 24, 25	$\overline{DIS_1}$ to $\overline{DIS_4}$	Open drain disable outputs—these outputs pull low when the corresponding OUT channel is off

Device Description

The DG884 is the world's first monolithic wideband crosspoint array that operates from dc to >100 MHz. The DG884 offers the ability to route any one of eight input signals to any one of four OUT pins. Any input can be routed to one, two, three or four OUTs simultaneously with no risk of shorting inputs together (guaranteed by design).

Each crosspoint is configured as a "T" switch in which DMOS FETs are used due to their excellent low resistance and low capacitance characteristics. Each OUT line has a series switch that minimizes capacitive loading when the OUT is off.

Interfacing

The DG884 was designed to allow complex matrices to be developed while maintaining a simple control interface. The status of the $\overline{I/O}$ pin determines whether the DG884 is being written to or read from (see Figures 1 and 2).

In order to WRITE to an individual latch, $\overline{CS}$ and $\overline{I/O}$ need to be low, while $\overline{RS}$, $\overline{WR}$ and $\overline{SALVO}$ must be high. The IN to OUT path is selected by using address A_0 through A_3 to define the IN line and address B_0 and B_1 to define the OUT line. That is, The IN defined by A_0 through A_3 is electrically connected to the OUT defined by B_0, B_1. This chosen path is loaded into the Next Event latches when $\overline{WR}$ goes low and returns high again. This operation is repeated up to three more times if other crosspoint connections need to be changed.

Upon completing all crosspoint connections that are to be changed in a single device, other DG884s can be similarly preset by taking the $\overline{CS}$ pin low on the appropriate device. When all DG884s are preset, the Current Event latches are simultaneously changed by a single $\overline{SALVO}$ command applied to all devices. In this manner the crosspoint configuration of any number of devices can be simultaneously updated.

$\overline{DIS}$ Outputs

Four open drain disable OUTs are provided to control external line drivers or to provide visual or electrical signaling. For example, any or all of the $\overline{DIS}$ OUTs can directly interface with a Siliconix Si582 Video Amplifier to place it into a high impedance, low-power standby mode when the corresponding OUT is not being used. (See Figure 15). The $\overline{DIS}$ outputs are low and sink to V− when corresponding OUT is open or $\overline{RS}$ is low.

Device Description (Cont'd)

Reset

The reset function ($\overline{RS}$) allows the resetting of all crosspoints to a known state (open). At power up, the reset facility may be used to guarantee that all switches are open. It should be noted that $\overline{RS}$ clears the Current Event latches, but the Next Event latches remain unchanged. This useful facility allows the user to return the matrix to its previous state (prior to reset) by simply applying the $\overline{SALVO}$ command. Alternatively, the user can reprogram the Next Event latches, and then apply the $\overline{SALVO}$ command to reconfigure the matrix to a new state.

Readback

The $\overline{I}$/O facility enables the user to write data to the Next Event latches or to read the contents of the Current Event latches. This feature permits the central controller to periodically monitor the state of the matrix. If a power loss to the controller occurs, the readback feature helps the matrix to recover rapidly. It also offers a means to perform PC board diagnostics both in production and in system operation.

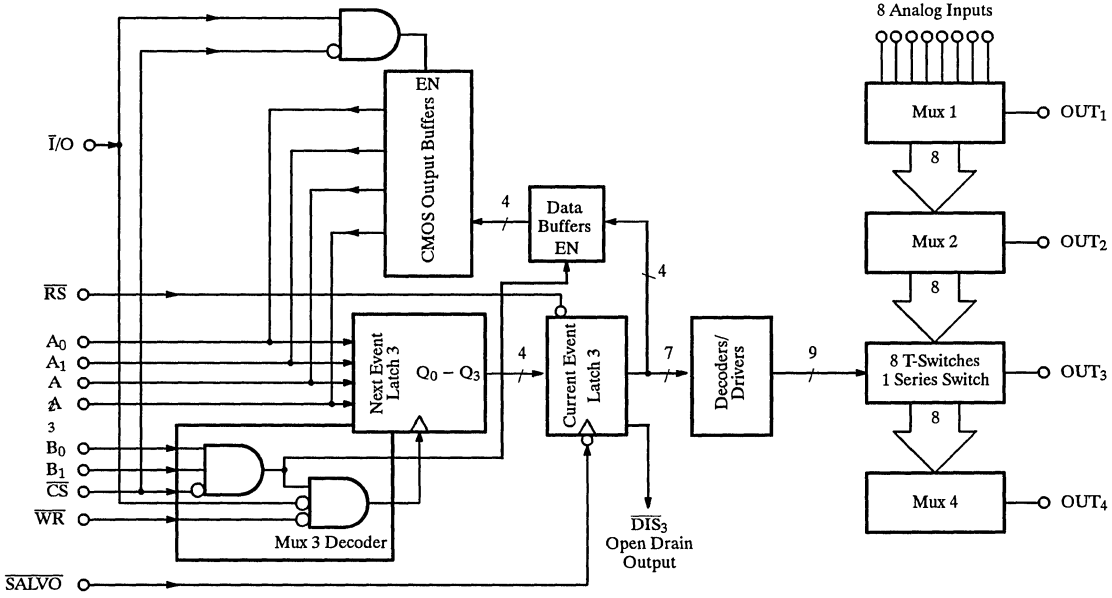
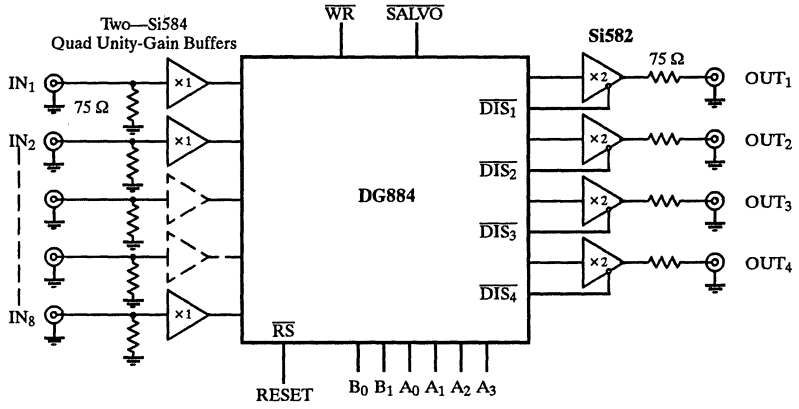


Figure 12. Control Circuitry

2

Applications



Note: $\overline{DIS}$ outputs are used to power down the Si582 amplifiers.

Figure 13. Fully Buffered 8 × 4 Crosspoint

Power Supplies and Decoupling

A useful feature of the DG884 is its power supply flexibility. It can be operated from dual supplies, or a single positive supply (V− connected to 0 V) if required. Allowable operating voltage ranges are shown in Operating Voltage Range (Typical Characteristics) graph, page 2-118.

Note that the analog signal must not go below V− by more than 0.3 V (see absolute maximum ratings). However, the addition of a V− pin has a number of advantages:

1) It allows flexibility in analog signal handling, i.e. with V− = −5 V and V+ = 15 V, up to ±5 V ac signals can be accepted.
2) The value of on-capacitance ($C_{S(on)}$) may be reduced by increasing the value of V−. It is useful to note that optimum video differential phase and gain occur when V− is −3 V. Note that V+ has no effect on $C_{S(on)}$.
3) V− eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG884 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

Rules:

1) Decoupling capacitors should be incorporated on all power supply pins (V+, V−, V_L).
2) They should be mounted as close as possible to the device pins.
3) Capacitors should have good high frequency characteristics—tantalum bead and/or monolithic ceramic disc types are suitable.

Recommended decoupling capacitors are 1- to 10-µF tantalum bead, in parallel with 100-nF monolithic ceramic.

4) Additional high frequency protection may be provided by 51-Ω carbon film resistors connected in series with the power supply pins (see Figure 14).

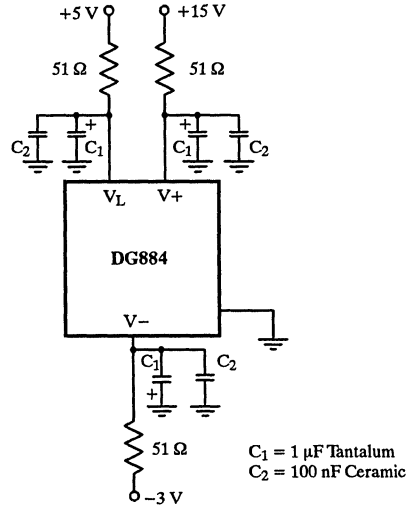


Figure 14. DG884 Power Supply Decoupling

Applications (Cont'd)

The V_L pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to V_L. The actual logic threshold can be raised simply by increasing V_L.

A typical switching threshold versus V_L is shown in Figure 15.

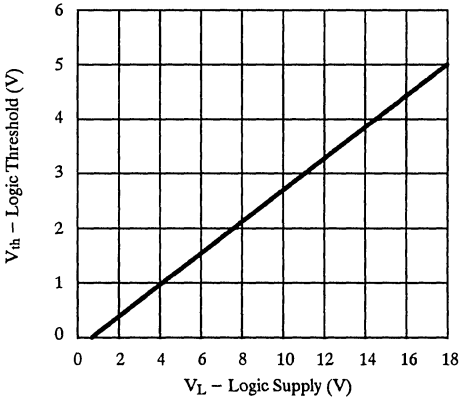


Figure 15. Switching Threshold Voltage vs. V_L

These devices feature an address readback facility whereby the last address written to the device may be read by the system. This allows improved status monitoring and hand shaking without additional external components.

When the $\overline{I}/O$ assigns the address output condition, the A_X address pins can sink or source current for logic low and high, respectively. Note that V_L is the logic high output condition. This point must be respected if V_L is varied for input logic threshold shifting.

Note: Even though these devices are designed to be latchup resistant, V_L must not exceed V+ by more than 0.3 V in operation or during power supply on/off sequencing.

Layout

The PLCC package pinout is optimized so that large crosspoint arrays can be easily implemented with a minimum number of PCB layers (see Figure 16). Crosstalk is minimized and off-isolation is optimized by having ground pins located adjacent to each input and output signal pins. Optimum off-isolation and low crosstalk performance can only be achieved by the proper use of RF layout techniques: avoid sockets, use ground planes, avoid ground loops, bypass the power supplies with high frequency type capacitors (low ESR, low ESL), use striplines to maintain transmission line impedance matching.

For additional information please refer to Application Note AN504.

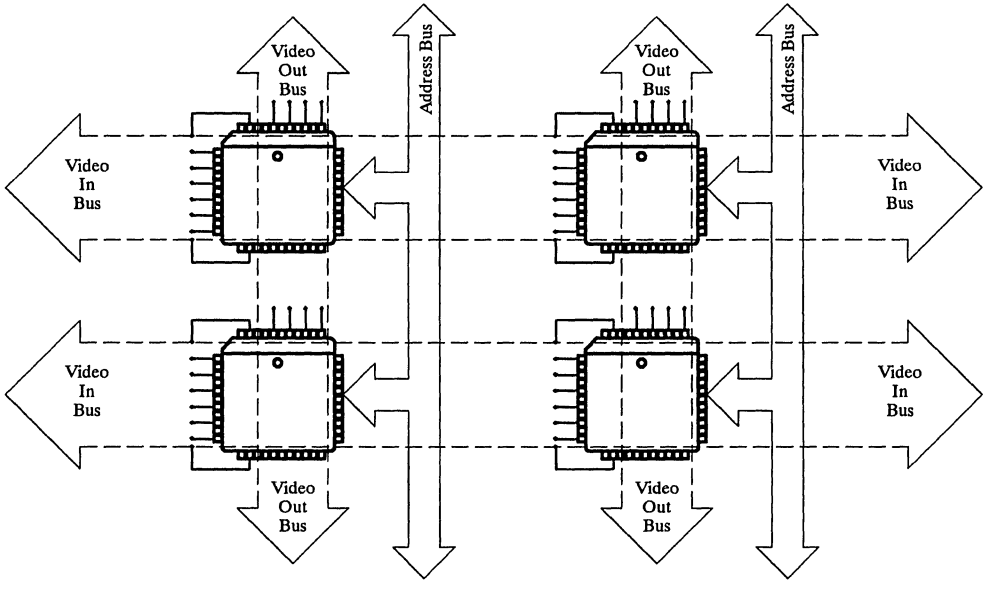


Figure 16. 16 × 8 Expandable Crosspoint Matrix Using DG884

Component Video Selector

Features

- Wide Bandwidth: 200 MHz
- Very Low Crosstalk: −70 dB at 5 MHz
- CMOS Compatible
- I^2C Bus Compatible
- Fast Switching—t_{ON}: <200 ns
- Low $r_{DS(on)}$: 44 Ω
- Single Supply Capability

Benefits

- Low Insertion Loss
- Improved System Performance
- Reduced Power Consumption
- Easily Interfaced
- Future System Expansion via I^2C Bus

Applications

- Component Video Switching: RGB + SYNC, S-VHS, Y-C, etc.
- Audio/Video Routing
- Digital TV
- ATE
- I^2C Bus Audio/Video Systems
- SCART Video Switching

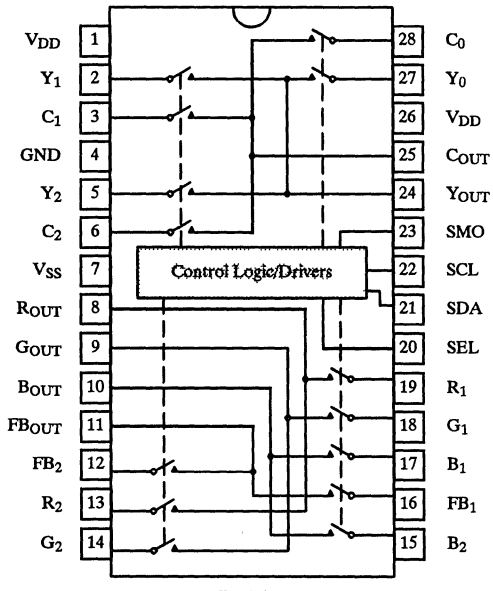
Description

The DG894 is a monolithic video selector designed for switching a variety of component video signals. The low on-resistance and low capacitance of the DG894 make it ideal for video/audio signal routing. Switch control can be through direct CMOS addressing or through the two-wire I^2C bus.

The DG894 is built on the Siliconix proprietary D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. Low-capacitance DMOS FETs are used to achieve high levels of off isolation at low cost.

Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

Truth Table

SMO	SEL	SDA	SCL	Function/Switch On
0	0	I^2C Bus Operation, Address A_0 = "1"		
0	1	I^2C Bus Operation, Address A_0 = "0"		
1	0	0	0	All switches off
1	0	0	1	Y_0, C_0
1	0	1	0	Y_1, C_1
1	0	1	1	Y_2, C_2
1	1	0	0	R_1, G_1, B_1, F_1
1	1	0	1	R_2, G_2, B_2, F_2
1	1	1	0	R_1, G_1, B_1, F_1, Y_1, C_1
1	1	1	1	R_2, G_2, B_2, F_2, Y_2, C_2

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	28-Pin Plastic DIP	DG894DJ
	28-Pin Wide Body SOIC	DG894DW

Absolute Maximum Ratings

V+ to GND ..... −0.3 V to 19 V
V+ to V− ..... −0.3 V to 19 V
V− to GND ..... −10 V to 0.3 V
Digital Inputs ..... GND −0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
Signal Inputs ..... V_{SS} −0.3 V to 8 V
or 20 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 20 mA
Current (Any Terminal) Pulsed 1 ms, 10% Duty Cycle Max . 40 mA
Storage Temperature ..... −65 to 125°C
Power Dissipation (Package)[a]
28-Pin Plastic DIP ..... 625 mW
28-Pin Wide Body SOIC ..... 450 mW

Notes:
a. All leads welded or soldered to PC board.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 12 V, V_{SS} = −5 V V_{INH} = 3 V, V_{INL} = 1.5 V[e]	Temp[a]	Limits −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V_{DD} = 12 V, V_{SS} = GND	Full	0		4	V
		V_{DD} = 12 V, V_{SS} = −5 V	Full	−2		2	
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = −10 mA, V_D = 0 V	Room Full		44 51	100 150	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$		Room		10		
Source Off Leakage Current	$I_{S(off)}$	V_S = 4 V, V_D = 0 V	Room Full	−10 −100	−0.05	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = 4 V, V_S = 0 V	Room Full	−10 −100	−0.05	10 100	
Total Switch On Leakage Current	$I_{D(on)}$	V_D = V_S = 4 V	Room Full	−10 −100	−0.07	10 100	
Input							
Input Voltage High	V_{INH}		Full	3	2.55		V
Input Voltage Low	V_{INL}		Full		2.55	1.5	
Input Threshold	V_{th}		Room		2.55		
Temp Coefficient of Input Threshold	TC_{th}		Full		−200		µV/°C
Input Current	I_{IN}	V_{IN} = GND or V_{DD}	Room Full	−1 −20	0.05	1 20	µA
Output Voltage Low	V_{OL}	Pin 21, During Acknowledge, I_{OL} = 3 mA	Room			0.4	V
Dynamic							
Input Capacitance[d]	C_{in}	Pin 21, 22	Room		3	10	pF
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		10	15	
Off State Input Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		4	8	
Off State Output Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		4	8	
Bandwidth[d]	BW	R_L = 50 Ω, See Figure 1	Room	200	500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, 50% to 90% V_{SS} = −5 V, 0 V, V_S = 3 V, See Figure 1	Room			200	ns
Turn Off Time	t_{OFF}		Room			180	
SCL Max Clock Frequency	$F_{SCL(MAX)}$		Full	100			kHz
Component Crosstalk	$X_{TALK(CO)}$	R_{IN} = 10 Ω, R_L = 1 kΩ f = 5 MHz, See Figure 2 and 3	Room		−85		dB
Channel Crosstalk	$X_{TALK(CH)}$		Room		−85		

2

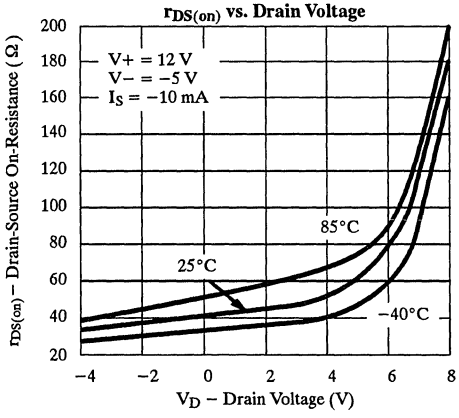
Specifications

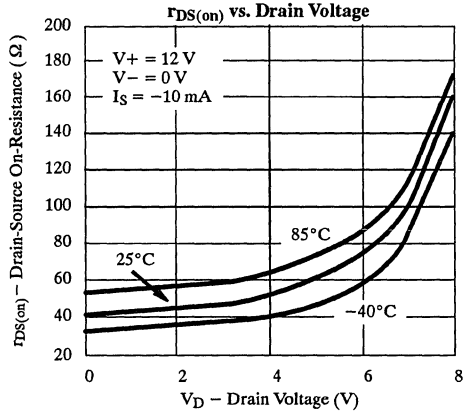
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 12 V, V_{SS} = −5 V V_{INH} = 3 V, V_{INL} = 1.5 V[e]	Temp[a]	Limits −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Supply Voltage							
Positive Supply Current	I+	All Control Inputs 0 V, 5 V	Room Full		3 4	8 10	mA
Negative Supply Current	I−		Room Full	−8 −10	−2.5 −3.0		

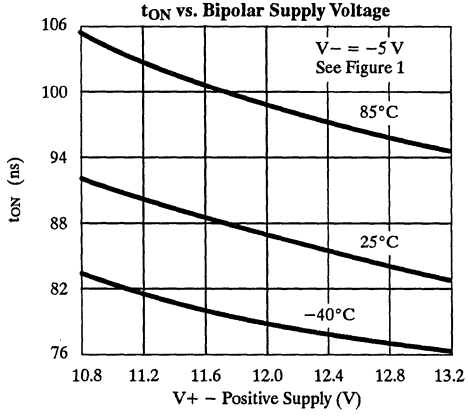
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

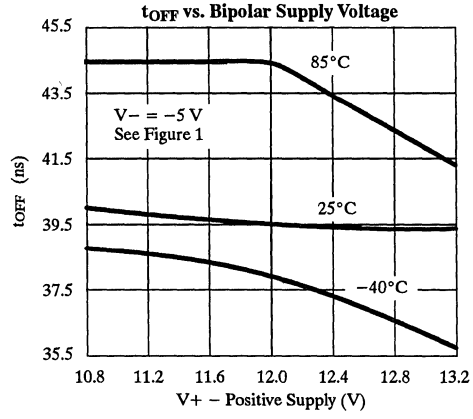
Purchase of Siliconix DG894 components conveys a license to use them in the I²C system as defined by Philips.

Typical Characteristics



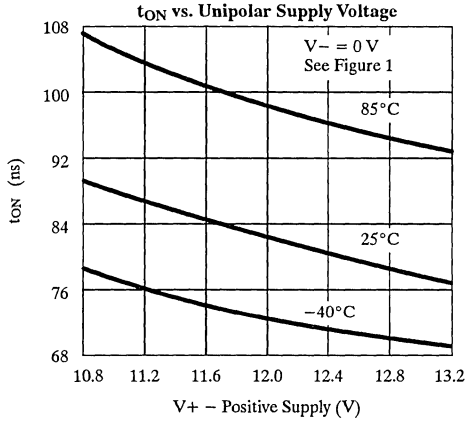




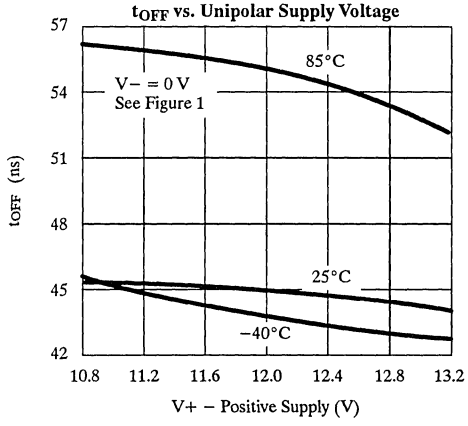


Typical Characteristics (Cont'd)

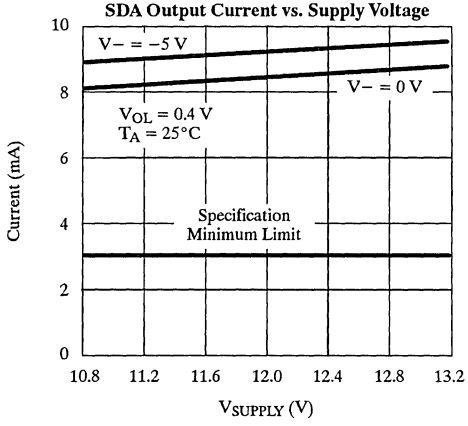
t_{ON} vs. Unipolar Supply Voltage



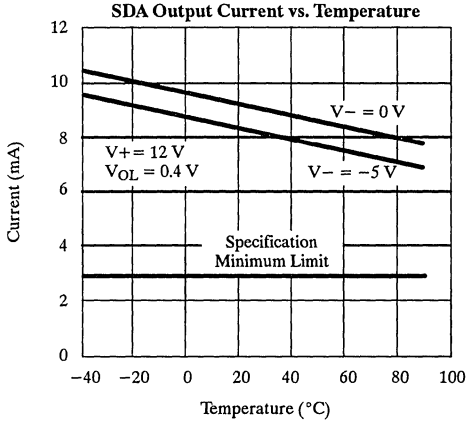
t_{OFF} vs. Unipolar Supply Voltage



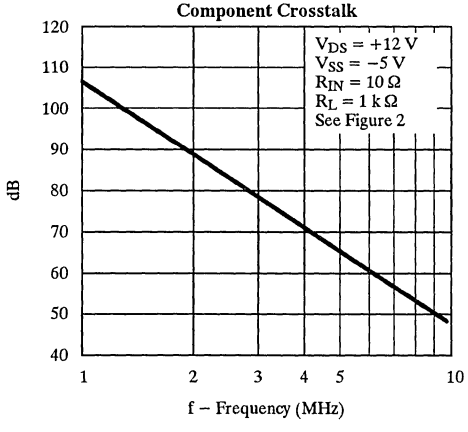
SDA Output Current vs. Supply Voltage



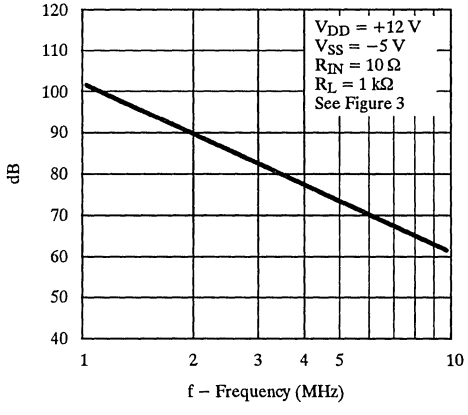
SDA Output Current vs. Temperature



Component Crosstalk

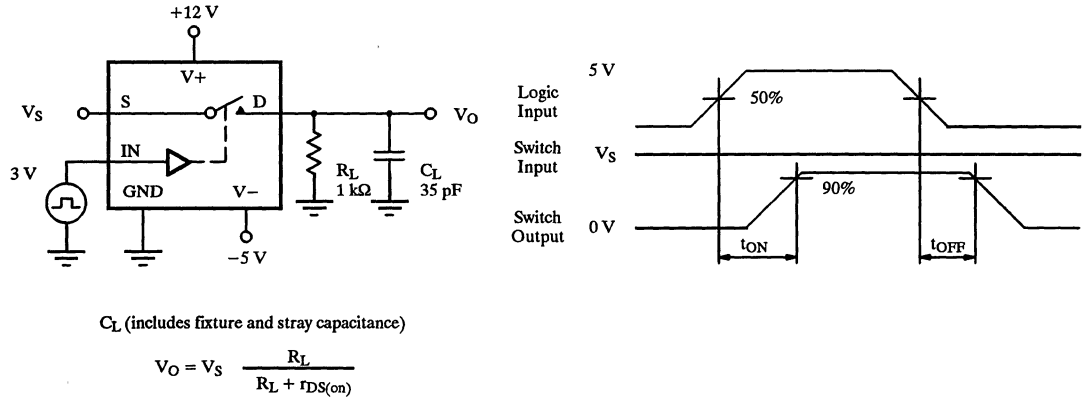


Channel Crosstalk



2

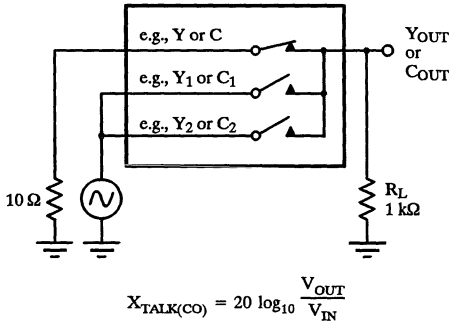
Test Circuits



C_L (includes fixture and stray capacitance)

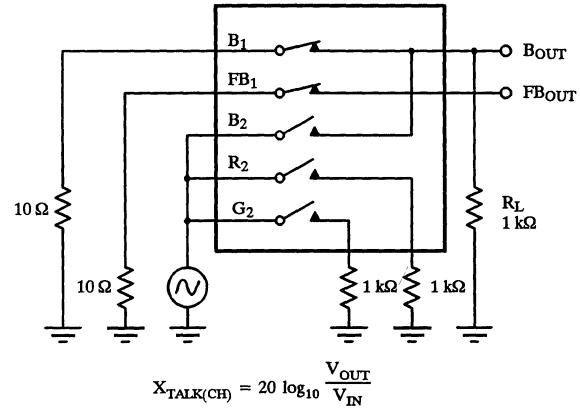
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 1. Switching Time



$$X_{TALK(CO)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

Figure 2. Component Crosstalk



$$X_{TALK(CH)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

Figure 3. Channel Crosstalk

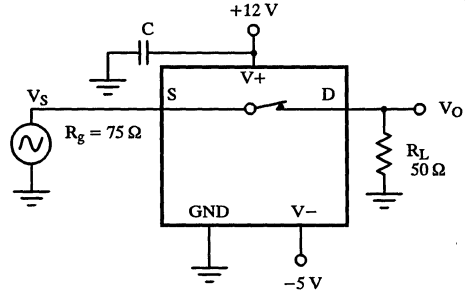


Figure 4. Bandwidth

Operating Voltage Range

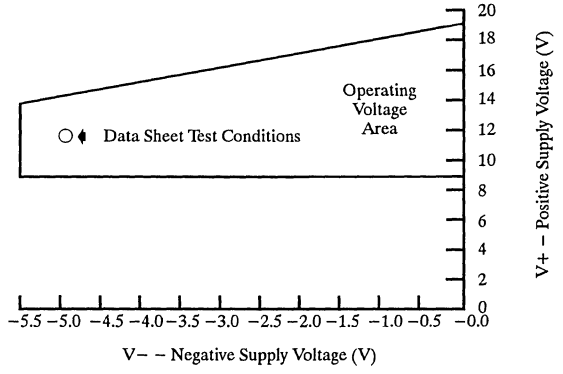


Figure 5.

Pin Description

Symbol	Description
Y_0, Y_1, Y_2	An analog channel input, typically luminance.
C_0, C_1, C_2	An analog channel input, typically chrominance.
R_1, R_2, G_1, G_2, B_1, B_2, FB_1, FB_2	An analog channel input, typically "red", "green", "blue" or "fast blanking", as appropriate.
GND	Analog and digital ground.
V_{DD}	Positive supply voltage[a]
V_{SS}	Negative supply voltage
Y_{OUT}, C_{OUT}	An analog channel output, typically luminance or chrominance, as appropriate
R_{OUT}, G_{OUT}, B_{OUT}, FB_{OUT}	An analog channel output, typically "red", "green", "blue" or "fast blanking", as appropriate.
SMO	A low selects serial mode (I^2C) operation. A high selects CMOS operation.
SDA	Serial data line[b]
SCL	Serial clock line[b]
SEL	CMOS control line or I^2C address[c] select line

Notes:
a. Both V_{DD} pins (Pin 1 and Pin 26) must be connected for proper operation.
b. SDA and SCL pins become CMOS control inputs when SMO = High.
c. The SEL pin, in I^2C bus operation (i.e., with SMO low), is the least significant bit of the device address. This allows two devices to operate on the same I^2C bus, yet retain independent control.

Applications

I²C Bus Operation—RGB Switching

Figure 6 shows an inexpensive RGB + stereo selector. The two audio channels are switched via the C, Y terminals. The Si584 quad video buffer drives four 75-Ω output lines.

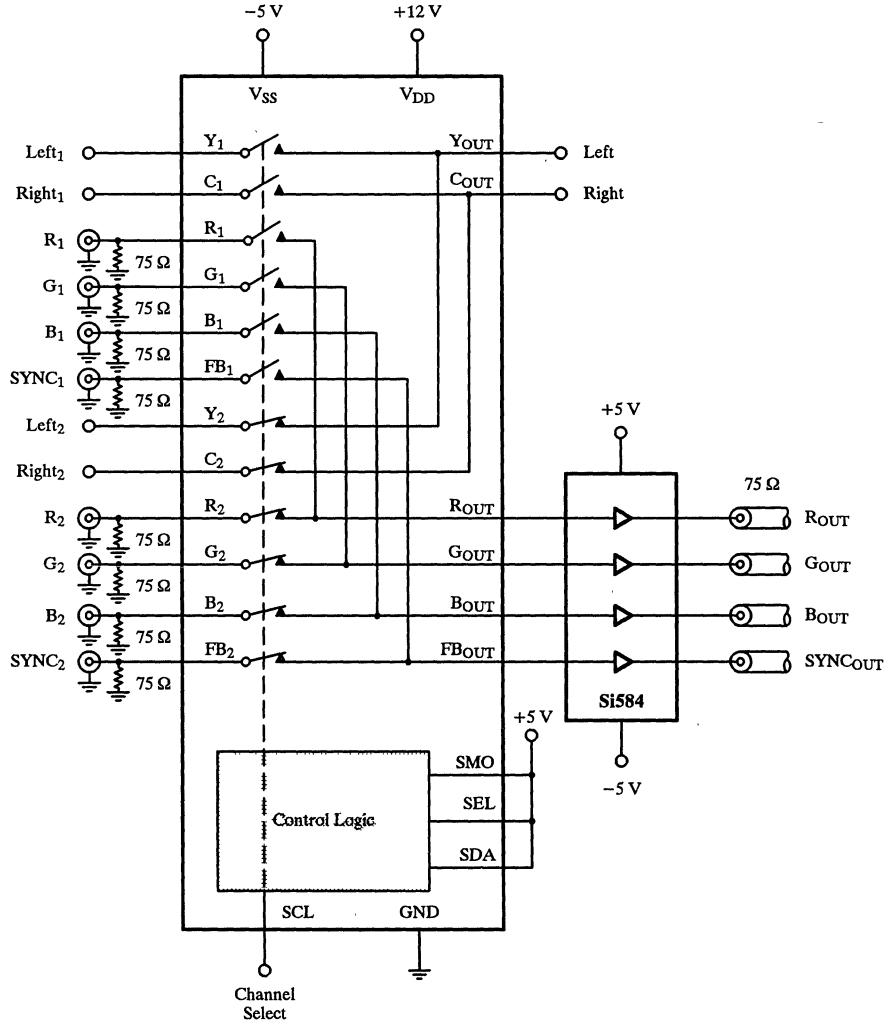


Figure 6.

Applications (Cont'd)

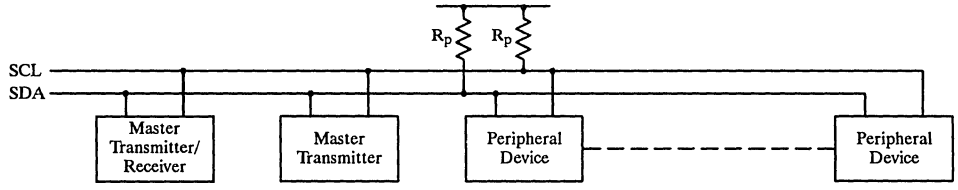


Figure 7.

Characteristics of the I^2C Bus

The I^2C Bus interface is ideally suited for communication between different ICs or modules. Its salient features are:

- Two wire bidirectional serial bus
  - Serial data (SDA) and serial clock (SCL) lines
- Multi-master system (built-in arbitration for multi-master systems)
- Devices have independent clocks
- Master and slave devices can be receivers and/or transmitters.
- Each device has a unique address.
- Maximum bus clock rate of 100 kHz.
- Any number of interfaces may be connected to the bus
  - Limited only by total capacitance of 400 pF
  - Each pin on bus limited to 10-pF capacitance
  - Input levels:
    V_{IL} max = 1.5 V (fixed supply operation)
    V_{IH} min = 3 V (fixed supply operation)
    V_{IL} max = 0.3 V_{DD} (wide range supply operation)
    V_{IH} min = 0.7 V_{DD} (wide range supply operation)

System Configuration

R_p value depends on:

- number of devices on bus
- total bus capacitance
- supply voltage (Figure 7).

Data Transfer on the I^2C Bus

If the bus is not being used, both SDA and SCL lines must be left high.

Every byte put onto the SDA line should be eight bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SDA line low during the ninth clock pulse, then accept the data in subsequent bytes until another start or stop condition is detected.

The eight bit of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device) so, for the DG894, the address is only considered valid if the R/W bit is low.

Data bytes are always acknowledged during the ninth clock pulse by the addressed device. Note that during the acknowledge period the transmitting device must leave the SDA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the DG894 will remain in the state defined by the last complete data byte transmitted.

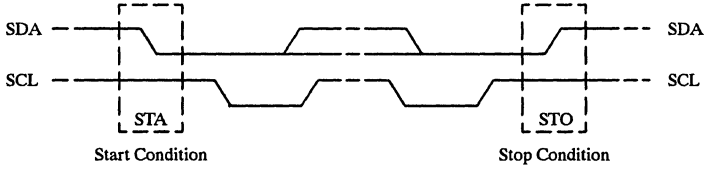


Figure 8. START and STOP Conditions

Applications (Cont'd)

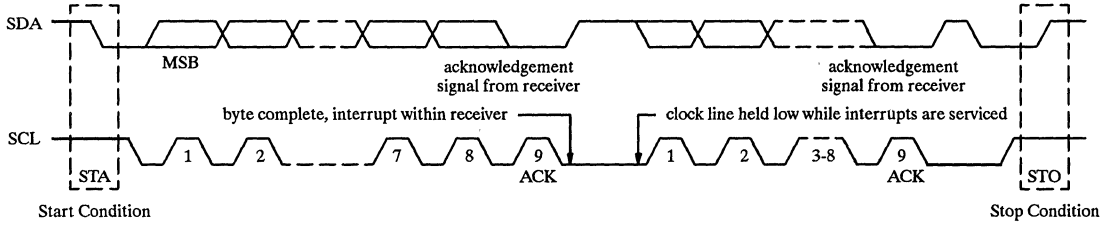


Figure 9. Data Transfer on the I²C Bus

Timing Specifications of the I²C Bus

I²C bus load conditions for timing specifications are as follows:

4 kΩ pull-up resistors to +5 V; 200 pF capacitor to ground. All values are referred to V_{IH} = 3 V, V_{IL} = 1.5 V.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	–	100	kHz
Bus Free Before Start	t_{BUF}	4.7	–	
Start Condition Set-up Time	$t_{SU;STA}$	4.7	–	
Start Condition Hold Time	$t_{HD;STA}$	4	–	
SCL and SDA Low Period	t_{LOW}	4.7	–	
SCL and SDA High Period	t_{HIGH}	4	–	µs
SCL and SDA Rise Time	t_r	–	1.0	
SCL and SDA Fall Time	t_f	–	0.3	
Data Set-Up Time (WRITE)	$t_{SU;DAT}$	0.25	–	
Data Hold Time (WRITE)	$t_{HD;DAT}$	0*	–	

* A transmitter must internally provide at lease a hold time to bridge the undefined region (max 300 ns) of the falling edge of the SCL.

I²C Bus Protocol

The DG894 is a slave receiver type of I²C interface and has four allocated addresses, two of which are user programmable through the SEL pin. Additional addresses may be obtained by a metal mask option for users requiring more than two DG894s on the same I²C bus. Contact Siliconix marketing for further information.

After the correct address has been sent, only one data byte is needed to define the switch configuration. Subsequent data put onto the bus will update the switches until a STOP condition (or another START condition) signals that the device is no longer being addressed. The switches will then remain in their last configuration as long as power is maintained to the chip.

Power on Reset

A power on reset function is provided on the DG894 to turn all switches off following power up if the I²C mode is selected. In the CMOS control mode, the switches are selected according to the state of the control inputs.

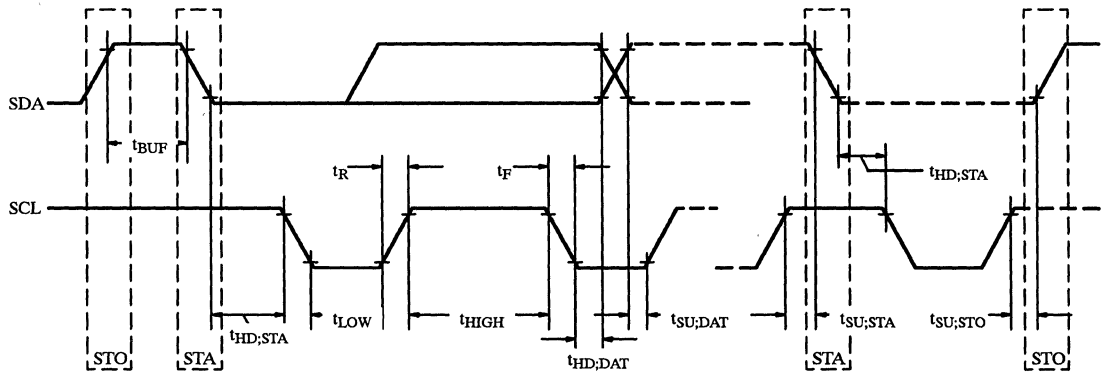


Figure 10. I²C Bus Timing Diagram

Applications (Cont'd)

Minimum Bit Stream to Set Up DG894 Switches

STA	1	1	0	1	1	A_1	A_0	R/W	ACK	X	X	X	D_4	D_3	D_2	D_1	D_0	ACK	STO

Address Byte ⟵⟶ Data Byte

STA = START CONDITION
A_1 = 0 (programmable to "1" with metal mask change)
A_0 = $\overline{SEL}$. Address bit set by use (address is inverse of SEL logic level)
R/W = READ/WRITE bit (must be "0", only WRITE mode allowed for DG894)
ACK = Acknowledge bit ("0") generated by DG894
D_4 = 0 -- R_2, G_2, B_2, and FB_2 switches off
D_4 = 1 -- R_2, G_2, B_2, and FB_2 switches on
D_3 = 0 -- R_1, G_1, B_1, and FB_1 switches off
D_3 = 1 -- R_1, G_1, B_1, and FB_1 switches on
D_2 = 0 -- Y_2, C_2, switches off
D_2 = 1 -- Y_2, C_2, switches on
D_1 = 0 -- Y_1, C_1, switches off
D_1 = 1 -- Y_1, C_1, switches on
D_0 = 0 -- Y_0 and C_0 switches off
D_0 = 1 -- Y_0 and C_0 switches on
STO = STOP CONDITION

About Siliconix Wideband/Video Amplifiers

The Siliconix family of wideband/video amplifiers works together to provide complete system solutions for such applications as video and data communication, signal switching and routing, and high-resolution workstation buffering. Our Si581 and Si584 unity-gain buffers, as well as the Si582 low-gain amplifier, improve linearity and transmission accuracy, while providing reduced power consumption, flat frequency response, and high color fidelity. With the Si582 amplifier at the output of a switching matrix, the Si581/Si584 buffers at the input, and our wideband multiplexers and switches (DG534A, DG535, DG536, DG538A, DG54X, DG61X, DG64X, DG884, or DG894) at the core, we now provide a complete system solution for broadband distribution and back-terminated line-driving applications.

Video Amplifiers

Part Number	Min −3 dB Bandwidth (MHz)	Max Offset Voltge (mV)	Min Slew Rate (V/µs)	Max Settling Time (ns)	Package	Configuration	Page
Si581	400	8	500	2	J, Y	Unity Gain Video Buffer	3-1
Si582	150	5	430	4.5	J, Y	Video Amplifier with Disable	3-8
Si584	135	5	200	6	J, Y	Quad Video Buffer	3-16

J = Plastic DIP Y = SOIC

Unity-Gain Video Buffer

Features

- −3 dB-Bandwidth: 730 MHz
- Low Differential Gain: 0.1%
- Low Differential Phase: 0.01°
- Low Power—P_D: 150 mW
- Fast Settling: 0.2% in 5 ns
- Low Distortion: −65 dBc at 20 MHz

Benefits

- Flat Frequency Response
- High Color Fidelity
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transmission Accuracy

Applications

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems
- Line Drivers

Description

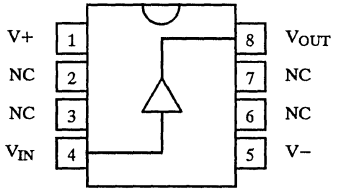
The Si581 is a monolithic closed-loop unity-gain video buffer with a very wide −3-dB bandwidth (730 MHz). Its unique design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si581 features low power dissipation (150 mW, typical), fast settling (0.2% in 5 ns), without signal degradation. Distortion is typically −65 dBc at 20 MHz, gain flatness is less than 0.4 dB from dc to 50 MHz. These performance specifications allow the designer to improve system bandwidth while reducing power dissipation, board space and design complexity. The output is protected against short circuits to ground.

The Si581 uses a complementary bipolar IC process to achieve excellent high frequency performance. All performance is specified and rated for operation with ±5-V supplies, reducing power consumption compared with traditional ±15-V designs.

Functional Block Diagrams and Pin Configurations

Dual-In-Line and SOIC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	8-Pin Plastic DIP	Si581DJ
	8-Pin Narrow SOIC	Si581DY

3

Absolute Maximum Ratings

Supply Voltage ..... ±7 V
Input Voltage Range ..... V− to V+
Output Short Circuit Duration ..... Continuous
Output Current ..... 70 mA

Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering 10s) ..... 300°C
Junction Temperature: T_J ..... 175°C

Specifications

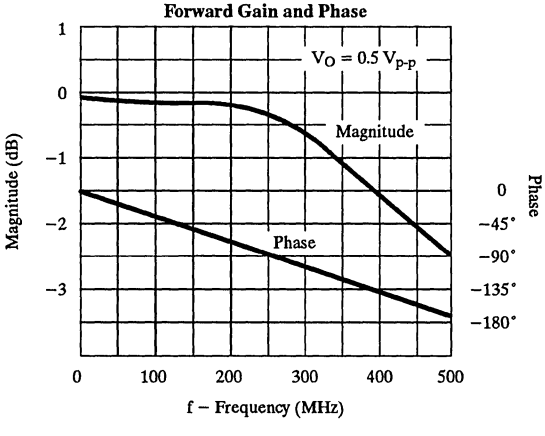
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_S = 50 Ω		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Frequency Domain[h]								
−3-dB Bandwidth[d]	SSBW	V_{OUT} <0.5 V_{p-p}		Room Full	400 300	730		MHz
	MSBW	V_{OUT} = <1 V_{p-p}		Room		450		
	LSBW	V_{OUT} = 5 V_{p-p}		Room Full	55 50	90		
Gain Flatness Peaking[e, g]	GFPH	V_{OUT} <0.5 V_{p-p}, dc to 200 MHz		Room Full		0	0.5 0.8	dB
Gain Flatness Roll Off[e]	GFRH			Room Full		0	0.8 1.2	
Linear Phase Deviation[e]	LPD	dc to 200 MHz		Room Full		0.7	1.5 2	deg
Differential Phase	DP	R_L = 150 Ω $V_{Carrier}$ = 280 mV	f = 3.58 MHz	Room		0.01		
			f = 4.43 MHz	Room		0.01		
Differential Gain	DG	f = 4.43 MHz $V_{Carrier}$ = 280 mV	R_L = 150 Ω	Room		0.1		%
			R_L = 1 kΩ	Room		0.07		
Time Domain[d, h]								
Rise and Fall Time	t_{RS}	V_{IN} = 0.5 V Step Input Rise/Fall time = 300 ps		Room Full		0.4	1 1.4	ns
	t_{RL}	V_{IN} = 5 V Step Input Rise/Fall time ≤ 1 ns		Room Full		4.5	7.5 8.5	
Settling Time	t_{SP}	To ±0.2 %, V_{IN} = 2 V Step		Full		5	10	
Slew Rate	SR			Room Full	500 450	800		V/µs
Distortion and Noise								
2nd Harmonic Distortion[g]	HD_2	V_{IN} = 2 V_{p-p}, f_{IN} = 20 MHz		Room Full		−65	−55 −48	dBc
3rd Harmonic Distortion[g]	HD_3			Full		−65	−55	
Equivalent Input Noise Floor[d]	SNF	f >100 kHz		Room Full		−158	−155 −154	dBm (1 Hz)
Equivalent Input Integrated Noise[d]	INV	100 kHz < f <200 MHz		Room Full		40	57 63	µV
Static, dc								
Small Signal Gain[d]	GA			Room Full	0.96 0.95	0.97		V/V
Integral Endpoint Linearity[d]	ILIN	±2 V Full Scale		Room Full		0.2	0.4 0.8	%FS
Input Offset Voltage[f]	VIO			Room Full		2	8 16	mV
Input Offset Voltage Average Temperature Coefficient[d]	DVIO			Room Full		20	– 100	µV/°C
Input Bias Current[f]	IBN			Room Full		±20	±50 ±100	µA
Input Bias Current Average Temperature Coefficient[d]	DIBN			Room Full		200	– 700	nA/°C
Power Supply Rejection Ratio[g]	PSRR			Full	45	50		dB
Supply Current[f]	I+	No Load		Full		15	20	mA

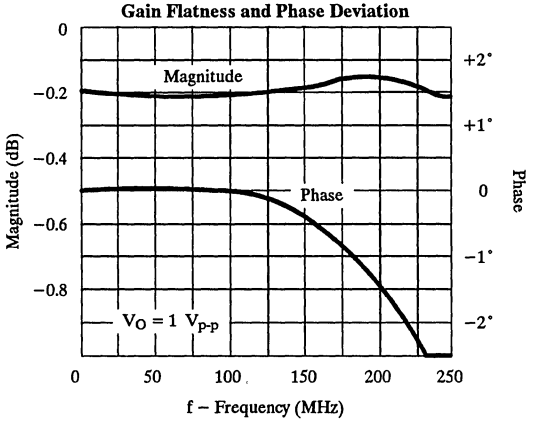
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_S = 50 Ω	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Miscellaneous[d]							
Input Resistance	R_{IN}		Room Full	100 50	160		kΩ
Input Capacitance	C_{IN}		Room Full		1.6	2.2 2.5	pF
Output Impedance	R_O	At dc	Room Full		2	3 3.5	Ω
Output Voltage Range	V_O		Room Full	−3.2 −3	±4	3.2 3	V
Output Current	I_O		Room Full	−50 −45	±70	50 45	mA

Notes:
a. Room = 25°C, Full = −40 to 85°C.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. Gain flatness tests are performed from 0.1 MHz to 200 MHz.
f. Parameter is 100% tested at 25°C and sample tested at 85°C.
g. Parameter is sample tested at 25°C.
h. AC performance is very dependent on layout. Specifications apply only in a 50-Ω microstrip environment.

Typical Characteristics: V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω





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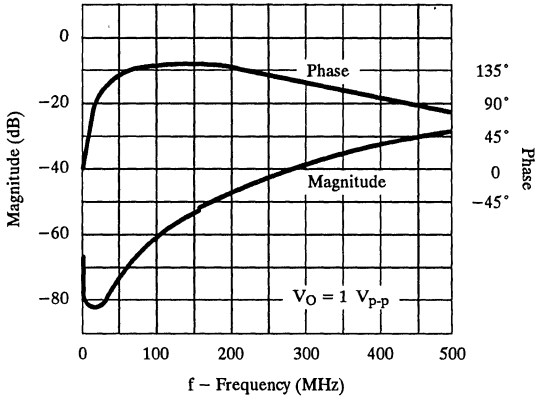
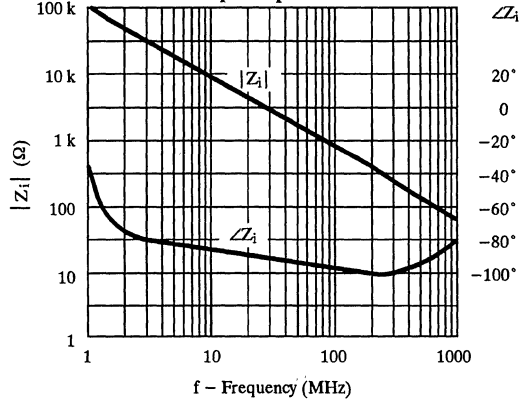
Typical Characteristics: V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω (Cont'd)

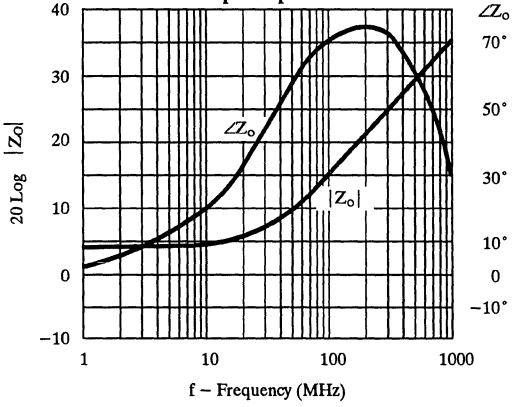
Reverse Gain and Phase



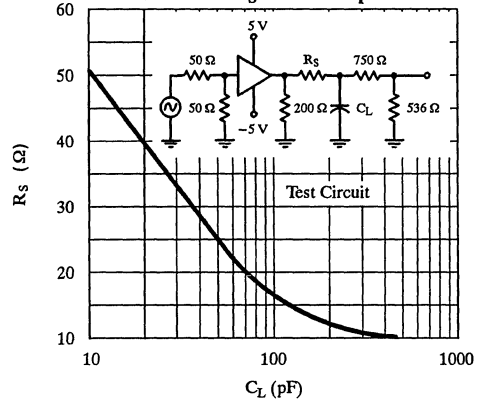
Input Impedance



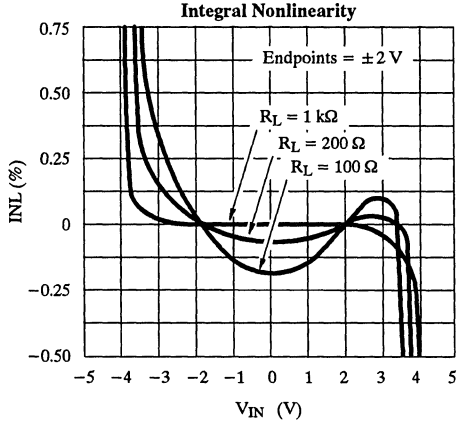
Output Impedance



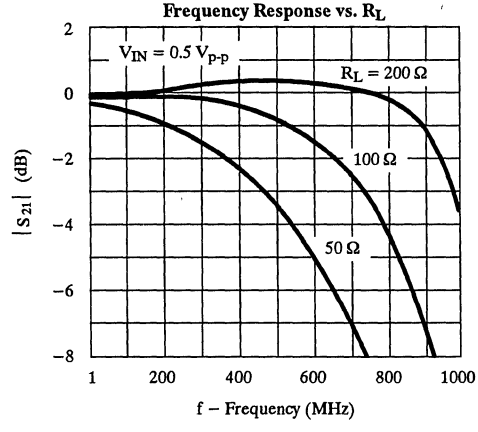
Recommended R_S vs. Load Capacitance



Integral Nonlinearity

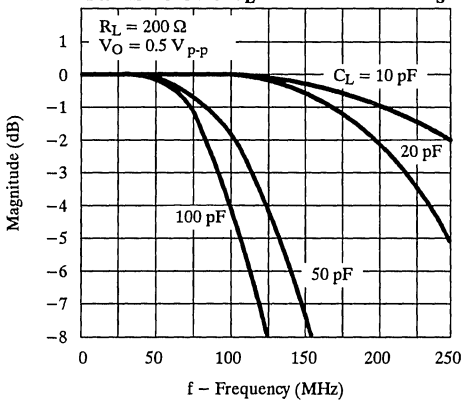


Frequency Response vs. R_L

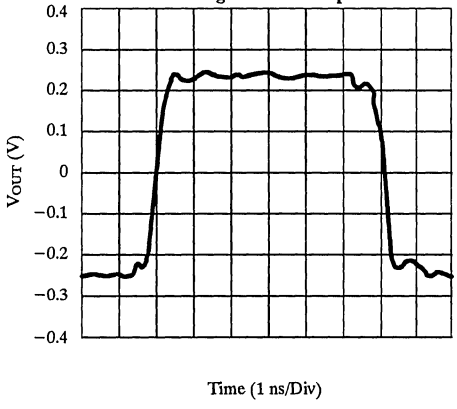


Typical Characteristics: $V_{SUP} = \pm 5$ V, $R_L = 100\ \Omega$, $R_S = 50\ \Omega$ (Cont'd)

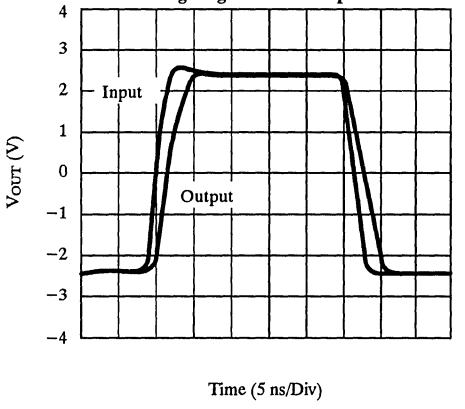
Forward Gain vs. C_L with Recommended R_S



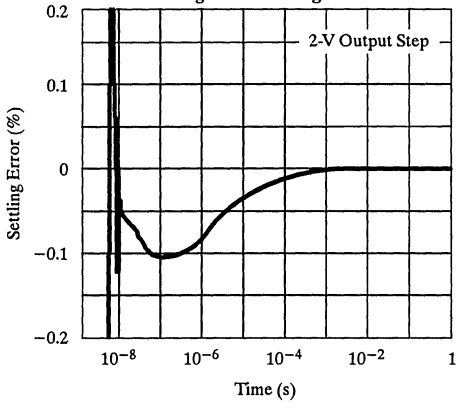
Small Signal Pulse Response



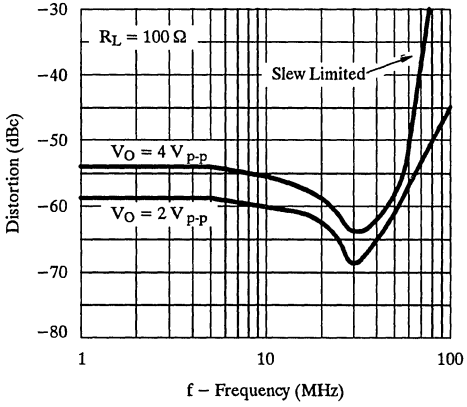
Large Signal Pulse Response



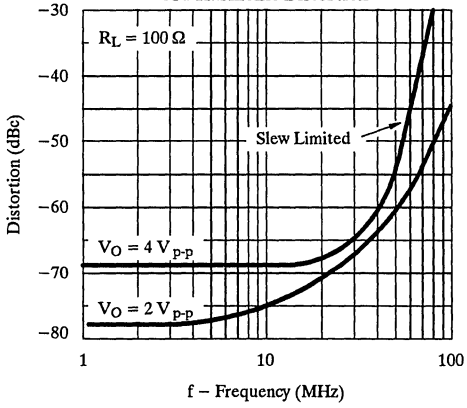
Long-Term Settling Time



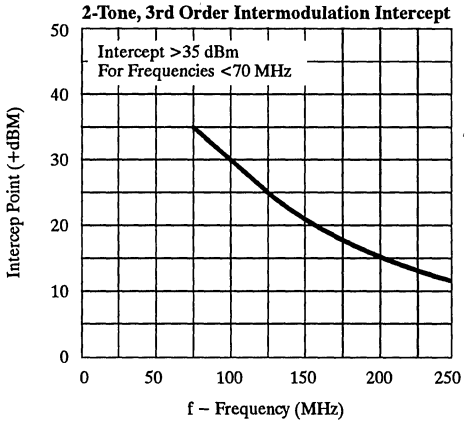
2nd Harmonic Distortion

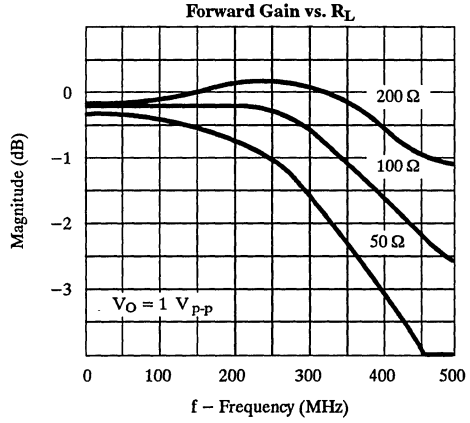


3rd Harmonic Distortion



Typical Characteristics: $V_{SUP} = \pm 5$ V, $R_L = 100\ \Omega$, $R_S = 50\ \Omega$ (Cont'd)





Applications

The Si581 provides the accuracy of a closed-loop amplifier plus unmatched dynamic performance.

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the Si581 which has a typical bandwidth of 730 MHz.

To minimize capacitive feedthrough, the pins which are not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the Si581. On a 0.065-inch epoxy PCB material, a 50-Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only where additional isolation from high-frequency (>400 MHz) resonances of the power supply is needed.

Parasitic or load capacitance directly on the output of the Si581 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The typical characteristic curves illustrate the required resistor value and the resulting performance vs. capacitance.

Precision resistors with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed metal film resistors will work, though they will cause a degradation of ac performance due to their reactive nature at high frequencies.

Applications (Cont'd)

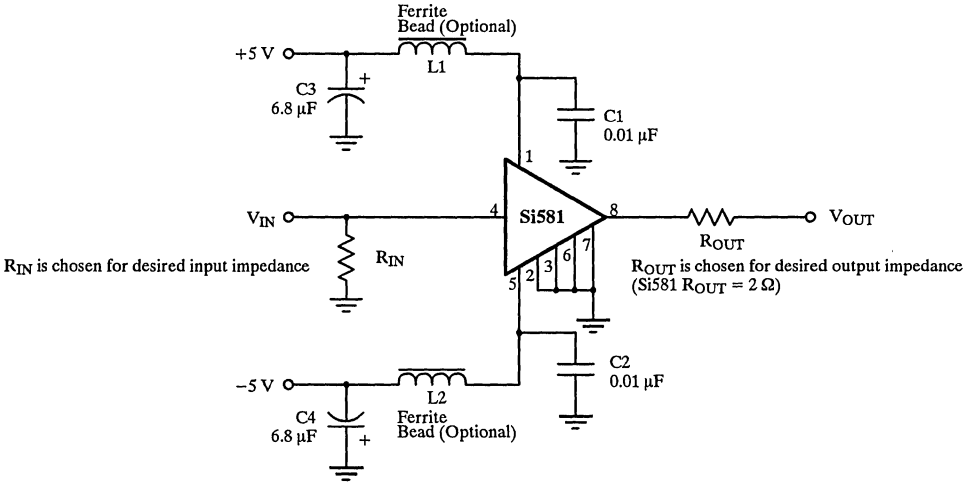


Figure 1. Recommended Decoupling

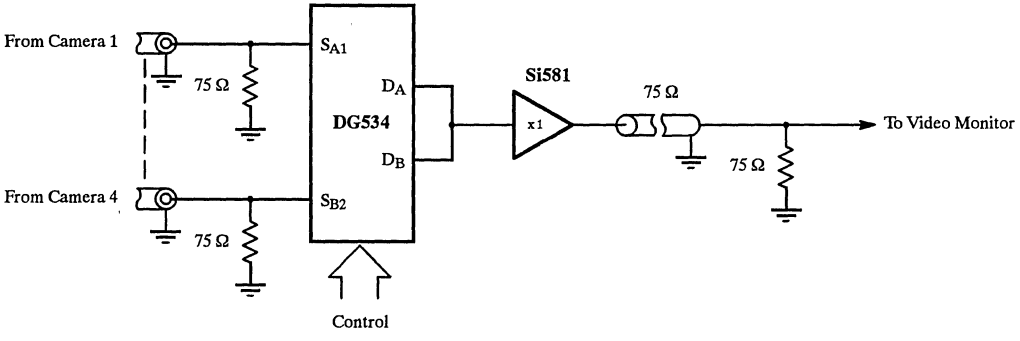


Figure 2. Four Camera High-Definition Closed Circuit TV System

3

Wideband Video Amplifier

Features

- −3-dB Bandwidth: 100 MHz
- Low Differential Gain: 0.01%
- Low Differential Phase: 0.01°
- ±1 to ±8 Closed-Loop Gain Range
- Low Power—P_D: 160 mW
- Fast Settling: 0.05% in 12 ns
- Low Distortion: −60 dBc at 20 MHz
- $\overline{\text{DISABLE}}$ Function

Benefits

- Flat Frequency Response
- High Color Fidelity
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transmission Accuracy
- Small Size
- Automatic Power-Down

Applications

- Coaxial Cable Drivers
- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems

Description

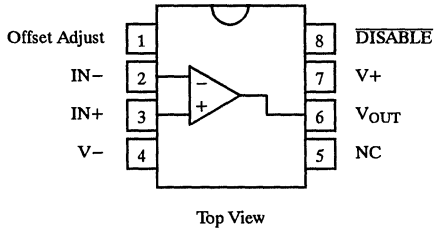
The Si582 is a monolithic video amplifier with a −3-dB bandwidth of 100 MHz. Its unique current-feedback design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and other video amplifiers.

The Si582 features wide bandwidth, low power dissipation (150 mW; typ) and fast settling (0.05% in 12 ns). Distortion is typically −60 dBc at 20 MHz, gain flatness is less than 0.3 dB from dc to 40 MHz. These performance specifications allow the designer to improve system bandwidth while reducing power dissipation, board space and design complexity. The wide bandwidth combined with a 50-mA output current at a gain of 2 provides an excellent high performance solution for video distribution and line driving applications. In addition, digital transmission systems will benefit from its superior pulse response. The output is protected against short circuits to ground.

The Si582 uses a complementary bipolar IC process to achieve excellent high frequency performance. All parameters are specified and rated for operation with ±5 V supplies, reducing power consumption compared with traditional ±15 V designs.

Functional Block Diagrams and Pin Configurations

Dual-In-Line and SOIC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	8-Pin Plastic DIP	Si582DJ
	8-Pin Narrow SOIC	Si582DY

Absolute Maximum Ratings

Supply Voltage ..... ±7 V
Input Voltage Range ..... V− to V+
Output Short Circuit Duration ..... Continuous
Output Current ..... 70 mA
Common Mode Input Voltage ..... V− to V+
Differential Input Voltage ..... 5 V
Disable Input Voltage ..... V− to V+
Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering 10s) ..... 300°C
Junction Temperature: T_J ..... 175°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_F = 250 Ω, A_V = 2		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Frequency Domain[h]								
−3 dB Bandwidth[d]	SSBW	V_{OUT} = ≤0.5 V_{p-p}		Room Full	150 120	200		MHz
	MSBW	V_{OUT} = ≤2 V_{p-p}		Room		100		
	LSBW	V_{OUT} = 5 V_{p-p}, A_V = 5		Full	35	50		
Gain Flatness Peaking[f, h]	GFPL	V_{OUT} ≤0.5 V_{p-p}	dc to 40 MHz	Room		0	0.3	dB
	GFPH		>40 MHz	Room Full		0	0.5 0.7	
Gain Flatness Roll Off[g]	GFR		dc to 75 MHz	Room Full		0.6	1 1.3	
Linear Phase Deviation	LPD	dc to 75 MHz		Room Full		0.2	1 1.2	deg
Differential Phase	DP	A_V = 2, R_F = 250 Ω, R_L = 150 Ω 1 V_{p-p} Video Signal, 3.58 MHz		Room Full		0.01	0.02 0.1	
Differential Gain	DG			Room Full		0.01	0.04 0.05	%
Time Domain[f, h]								
Rise and Fall Time[d]	t_{RS}	V_{IN} = 0.5 V Step		Full		1.6	2.4	ns
	t_{RL}	V_{IN} = 5 V Step		Full		6.5	10	
Settling Time[d]	t_S	To ±0.05 %, V_{IN} = 2 V Step		Full		12	15	
Slew Rate[d]	SR	A_V = 2		Full	430	700		V/µs
	SR_1	A_V = −2		Full		1600		
Distortion and Noise								
2nd Harmonic Distortion[f, h]	HD_2	V_{IN} = 2 V_{p-p}, f_{IN} = 20 MHz		Room Full		−60	−45 −40	dBc
3rd Harmonic Distortion[f, h]	HD_3			Full		−60	−50	
Equivalent Input Noise Floor[d]	SNF	f >100 kHz, 50 Ω on Input		Room Full		−157	−154 −153	dBm (1 Hz)
Equivalent Input Integrated Noise[d]	INV	100 kHz < f <200 MHz		Room Full		40	57 54	µV
Switching (Disable)								
Turn On Time	t_{ON}			Full		100	200	ns
Turn Off Time	t_{OFF}	To 50 dB Attenuation @ 10 MHz		Full		0.2	1	µs
Off Isolation[d]	OI	f_{IN} = 10 MHz, $\overline{DISABLE}$ = "0"		Full	−55	−59		dB
Current to Disable	I_{DIS}			Full	−250	−200		µA
Current to Enable				Full		−80	−60	
Disable Drive Voltage	V_{DISL}	$\overline{DISABLE}$ = "0", I_{DIS} = 250 µA		Full		1	0.5	V
Voltage to Enable	V_{DISH}	$\overline{DISABLE}$ = "1"		Room Full	3.2 4	2.6		
Static, dc								
Input Offset Voltage[f]	VIO			Room Full	−5 −9	±2	5 9	mV
Input Offset Voltage Average Temperature Coefficient[d]	DVIO			Room Full	−40	±20	40	µV/°C
Input Bias Current Non-inverting[f]	IBN			Room Full	−20 −36	10	20 36	µA

3

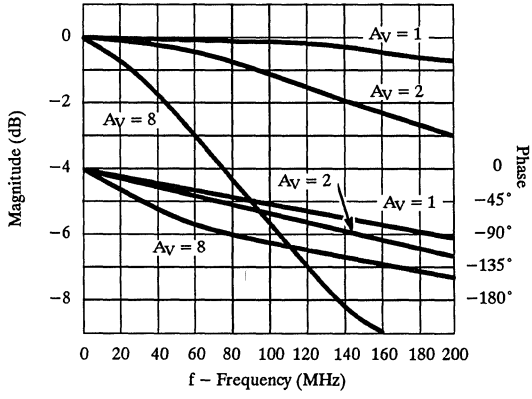
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_F = 250 Ω, A_V = 2	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Static, dc (Cont'd)							
Input Bias Current Non-inverting Temperature Coefficient[d]	DIBN		Room Full	 −200	100	 200	nA/°C
Input Bias Current Inverting[f]	IBI		Room Full	−20 −36	±10	20 36	µA
Input Bias Current Inverting Temperature Coefficient[d]	DIBI		Room Full	 −200	±50	 200	nA/°C
Power Supply Rejection Ratio[g]	PSRR		Full	45			dB
Common Mode Rejection Ratio	CMRR		Full	45			
Supply Current[f]	I+	No Load	Full		16	18	mA
		Disabled, No Load	Full		4	6	
Miscellaneous							
Non-inverting Input Resistance	R_{IN}		Room Full	100 50	200		kΩ
Non-inverting Input Capacitance	C_{IN}		Full		0.5	2	pF
Output Impedance	R_O	At dc	Full		0.1	0.2	Ω
Output Voltage Range	V_O	No Load	Room Full	−3.2 −3	±3.5	3.2 3	V
Common Mode Input Range For Rated Performance	CMIR		Room Full	−2 −1.2	±2.1	2 1.2	
Output Current[d]	I_O		Room Full	−50 −35	±70	50 35	mA

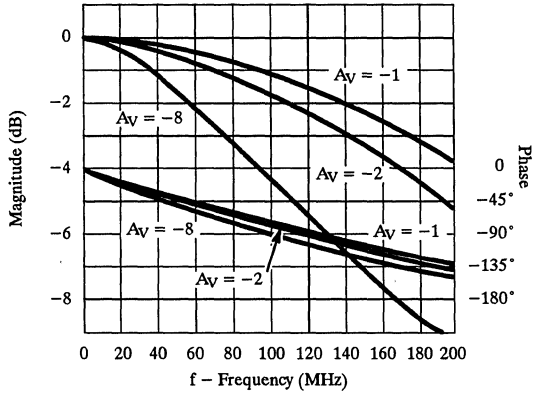
Notes:
a. Room = 25°C, Full = −40 to 85°C.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production testing.
e. Gain flatness tests are performed from 0.1 MHz to 50 MHz, and specifications are guaranteed from dc to 50 MHz.
f. Parameter is 100% tested at 25°C and sample tested at 85°C.
g. Parameter is sample tested at 25°C.
h. Ac performance is very dependent on layout. Specifications apply only in a 50-Ω microstrip environment.

Typical Characteristics

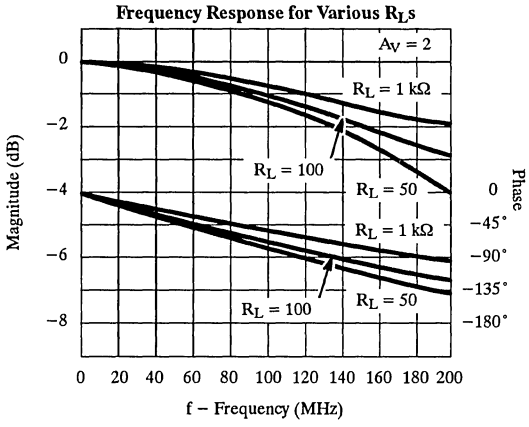
Non-Inverting Frequency Response

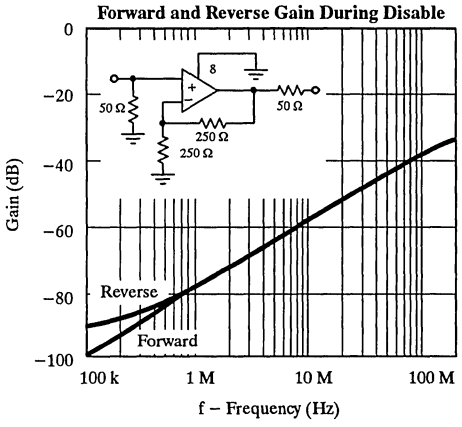


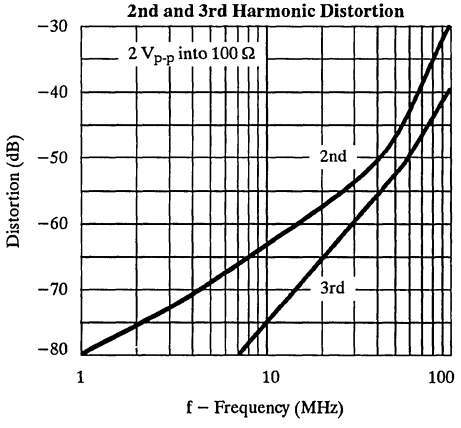
Inverting Frequency Response

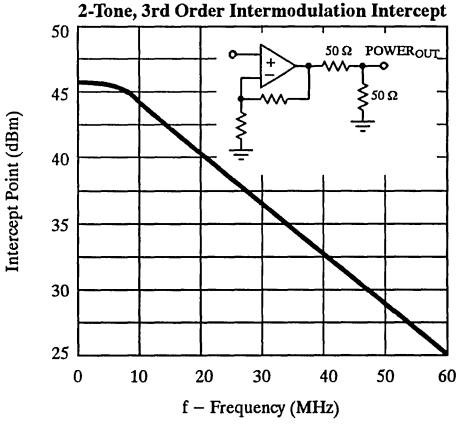


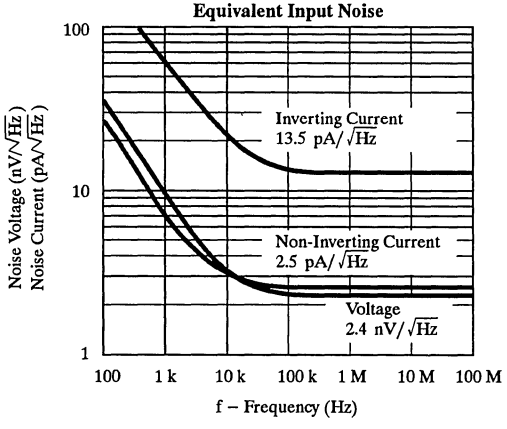
Typical Characteristics

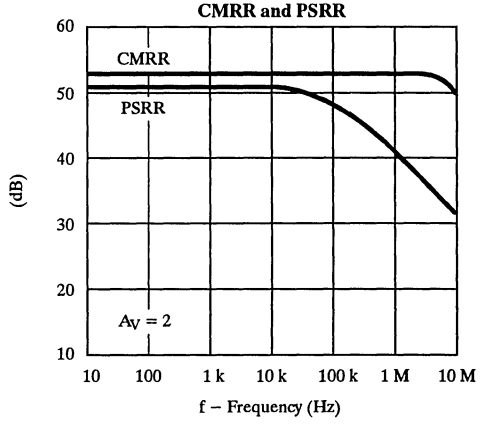








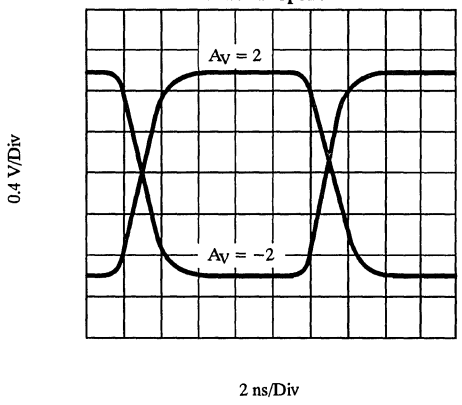




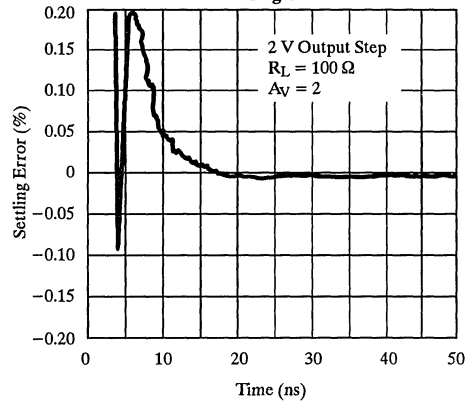
3

Typical Characteristics

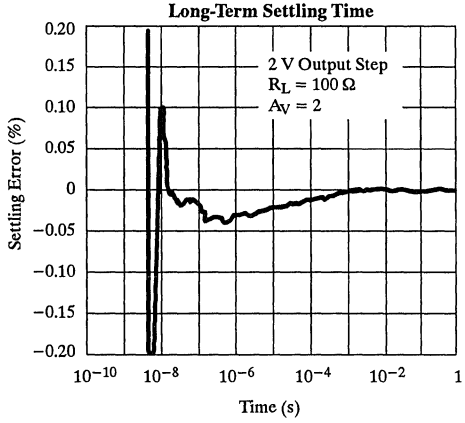
Pulse Response



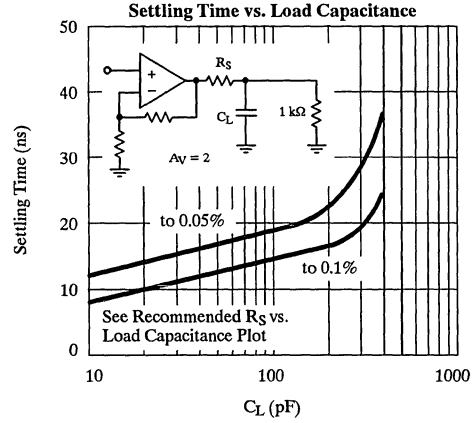
Settling Time



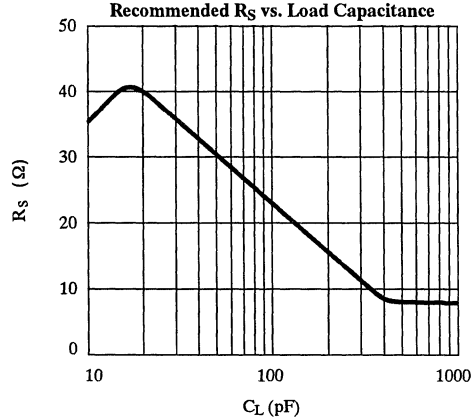
Long-Term Settling Time



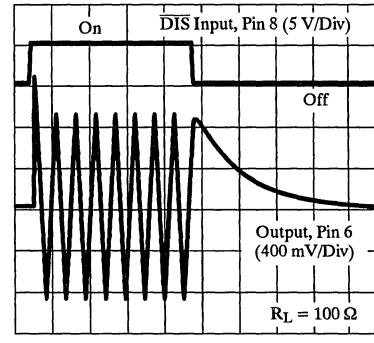
Settling Time vs. Load Capacitance



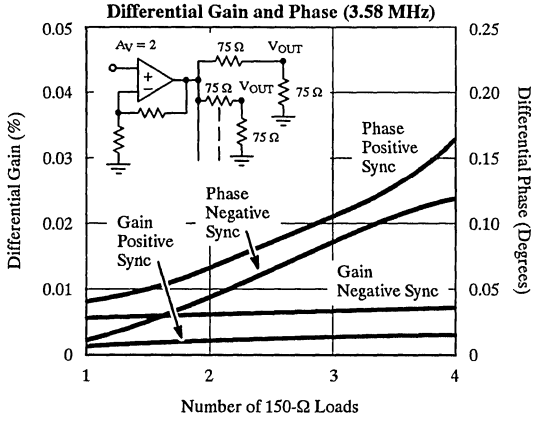
Recommended R_S vs. Load Capacitance

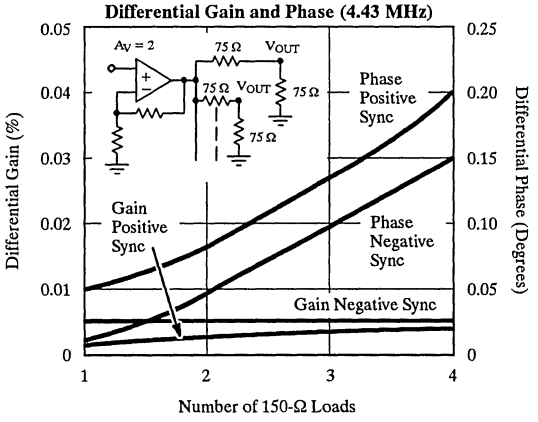


Enable/Disable Response



Typical Characteristics





Applications

Setting Loop Gain

The Si582 uses a current feedback topology instead of the more common voltage feedback, meaning that the closed loop bandwidth and settling time are relatively independent of closed loop gain.

Optimum bandwidth is achieved with a feedback resistor of 220 to 270 Ω. Closed loop gain is then set by a suitable choice of input resistor value. Figure 1 shows the connections for inverting and non-inverting gains. Feedback resistors greater than 270 Ω may be used, but at the expense of bandwidth. Values lower than 220 Ω will cause amplitude peaking in the passband. For example, a feedback resistor value of 100 Ω will create a peak of approximately 4 dB as roll-off is approached.

Under no circumstances should the output be connected directly to the inverting input in the hope of achieving unity gain. This will cause the device to oscillate and draw significant current from the power supply. Unity gain may be achieved with a 220- to 270-Ω resistor in the feedback path with no input resistor. Similarly, capacitive feedback should not be used with the Si582.

Offset Correction

Since the two inputs to the Si582 are quite different internally, the noise and offset performance differs from that of a differential input op-amp. The two input bias currents are unrelated, so that the technique of bias current error cancellation by matching of the inverting and non-inverting input resistances is ineffective.

The equation for output offset is shown in Figure 1, and is the algebraic sum of the equivalent input voltage and current sources which influence dc operation. Pin 1 may be used to correct for the ±10-mV offset by connecting as shown in Figure 1. When not used, pin 1 should be bypassed to signal ground with a 0.1-µF low inductance capacitor.

Disable Operation

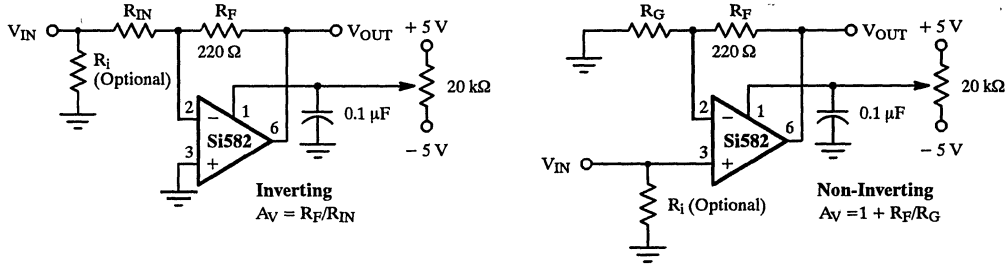
The disable function of the Si582 is obtained by taking pin 8 to ground. A minimum current of 250 µA needs to be sunk, and a maximum voltage of 0.5 V is required for full disable. When the disable function is not required, pin 8 may be left open or could be tied to the +5-V rail.

Disabling the amplifier reduces power supply current and places the output and inverting input pins in a high impedance state (200 kΩ || 0.5 pF)

PCB Layout and Supply Bypassing

The Si582 bandwidth and pulse response are dependent upon good layout and decoupling techniques. Ground plane construction is recommended to preserve as low a ground impedance as possible. Power supply decoupling components should be mounted close to the package and should have good high frequency characteristics to preserve the excellent pulse performance of the device. Figure 2 shows the recommended decoupling circuit. The 10-µF capacitor should be Tantalum or other low ESR/ESL type. For the 0.1-µF capacitor, multi-layer ceramic capacitors are recommended. A low value resistor in series with the 10-µF capacitor's ground lead may be required to reduce output pulse ringing.

Applications



Output Offset = $\pm I_{BN} \times R_S(1 + R_F/R_{IN}) \pm V_{IO}(1 + R_F/R_{IN}) \pm I_{BI}.R_F$

Where:
I_{BI} = Inverting Input Bias Current
I_{BN} = Non-Inverting Input Bias Current
R_S = Non-Inverting Pin Resistance
V_{IO} = Input Offset Voltage
R_i sets the impedance

Figure 1. Si582 Gain Circuits

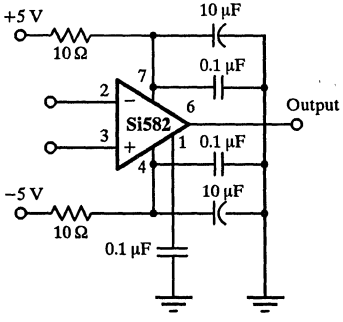


Figure 2. Decoupling the Si582

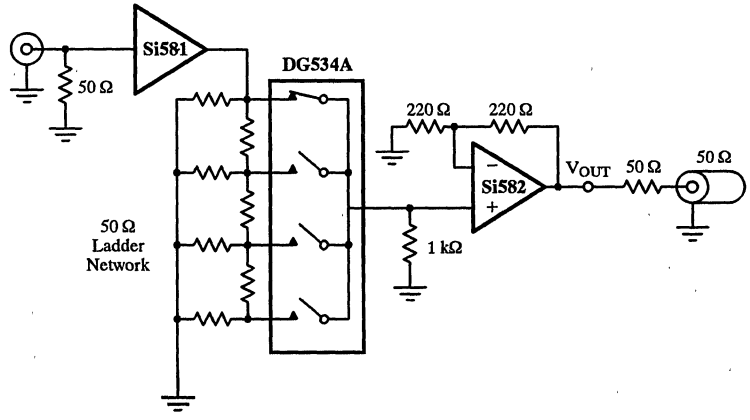


Figure 3. 4-Step Wideband Digitally Controlled Attenuator

Digitally Controlled Attenuator

Figure 3 shows the Si582 in a wideband, digitally controlled attenuator circuit employing the DG534A, a 4 to 1 D/CMOS multiplexer. The Si581 buffers the input and drives the 50-Ω ladder attenuator. Taps are chosen to suit the application, i.e., 0.1-dB or 1-dB steps. The second Si582 buffers the multiplexer for good linearity and, at a gain of two, provides "lossless" cable termination at the output.

Applications

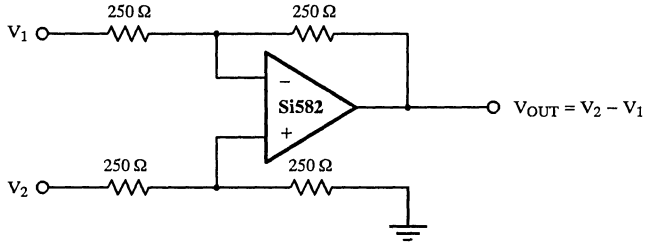


Figure 4. Differential Amplifier

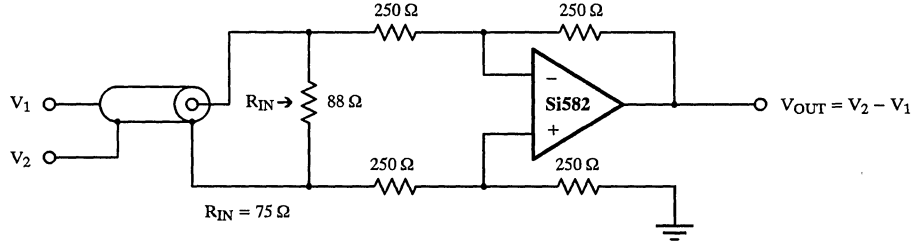


Figure 5. Differential Line Receiver

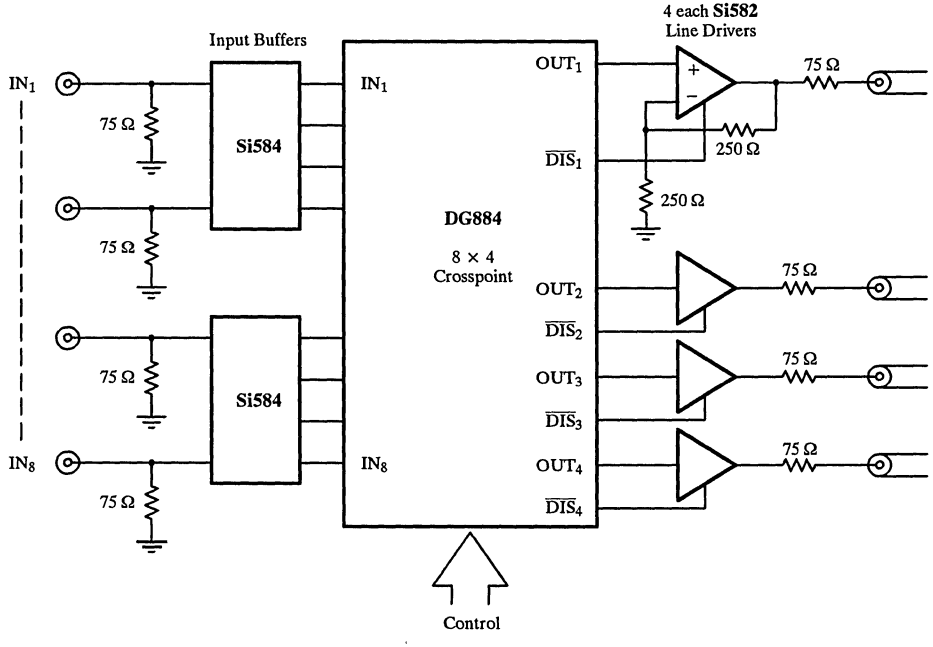


Figure 6. 50 MHz 8 × 4 Video Crosspoint Switch

Quad Unity-Gain Video Buffer

Features

- −3-dB Bandwidth: 120 MHz
- 30-MHz Gain Flatness: 0.1 dB
- High Channel Isolation: 62 dB @ 10 MHz
- Low Differential Gain—0.08%
- Low Differential Phase—0.1°
- Low Power—P_D: 30 mW/Channel
- Fast Settling: 0.1% in 10 ns
- Low Distortion: −58 dBc @ 20 MHz

Benefits

- Flat Frequency Response
- High Color Fidelity
- Improved Transmission Accuracy
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Small Size

Applications

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems

Description

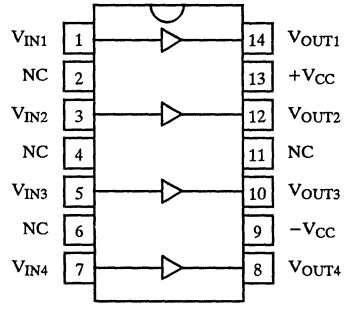
The Si584 is a monolithic closed-loop quad video buffer with a wide −3-dB bandwidth (120 MHz). Its unique design, optimized for high quality video switching, offers a high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si584 features wide bandwidth, low power consumption, fast settling (0.1% in 10 ns), without signal degradation. Third harmonic distortion is typically −58 dBc at 20 MHz, gain flatness is typically 0.1 dB from dc to 30 MHz. These performance specifications allow the designer to improve system bandwidth while reducing system power consumption, board space and design complexity. The outputs are protected against short circuits to ground.

The Si584 is built on an advanced complementary bipolar process to achieve excellent high frequency performance. All performance is specified and rated for operation with ±5-V supplies, reducing power consumption compared with traditional ±15-V designs.

Functional Block Diagrams and Pin Configurations

Dual-In-Line and SOIC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	14-Pin Plastic DIP	Si584DJ
	14-Pin Narrow SOIC	Si584DY

Absolute Maximum Ratings

Supply Voltage	±7 V	Storage Temperature	−65 to 150°C
Input Voltage Range	V− to V+	Lead Temperature (Soldering 10s)	300°C
Output Current	35 mA	Junction Temperature: T_J	175°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V, R_L = 100 Ω, R_S = 50 Ω		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Frequency Domain[g]								
−3 dB Bandwidth[f]	SSBW	V_{OUT} = ≤ 0.5 V_{p-p}		Room Full	135 120	200		MHz
	MSBW	V_{OUT} = 1 V_{p-p}		Room		120		
	LSBW	V_{OUT} = 2 V_{p-p}		Full	70	95		
Gain Flatness Peaking[f]	GFPL	V_{OUT} ≤ 0.5 V_{p-p}	0.1 to 30 MHz	Room Full		0	0.2 0.3	dB
	GFPH		>30 MHz	Room Full		0	0.4 0.7	
Crosstalk	X_{TALK}	f = 10 MHz		Room		62		
Time Domain[d, g]								
Rise and Fall Time	t_{RS1}	V_{IN} = 0.5 V Step		Room Full		1.8	2.8 3.0	ns
	t_{RS2}	V_{IN} = 2 V Step		Room Full		5	7 8	
Settling Time	t_S			Room Full		10	15 20	
Overshoot	OS	V_{IN} = 0.5 V Step		Room Full		3	10 15	%
Slew Rate	SR			Room Full	200 180	450		V/µs
Static, dc								
Small Signal Gain[d]	GA			Room Full	0.96 0.95	0.97		V/V
Integral Endpoint Linearity[d]	I_{LIN}	±1 V Full Scale		Room		0.4	0.6	%
Output Offset Voltage[e]	VIO			Room Full		±0.5	±5 ±8.2	mV
Input Offset Voltage Average Temperature Coefficient[e]	DVIO			Room Full		±9	±40	µV/°C
Input Bias Current[e]	I_B			Room Full		±1	±5 ±10	µA
Power Supply Rejection Ratio[e]	PSRR			Room Full	48 46	56		dB
Supply Current, Total[e]	I+	No Load		Room Full		12	16.5 17	mA
Miscellaneous								
Input Resistance	R_{IN}			Room Full	1 0.3	1.5		MΩ
Input Capacitance	C_{IN}			Room Full		1.8	3 3.5	pF
Output Impedance	R_O	At dc		Room Full		2.5	3.5 5	Ω
Output Voltage Range	V_O	No Load		Room Full	±3.8 ±3.6	±4		V
Output Current, per Buffer[d]	I_O			Room Full	±20 ±12	±25		mA
2nd Harmonic Distortion[f]	HD_2	V_{IN} = 2 V_{p-p}, f_{IN} = 20 MHz		Room Full		−50	−38 −36	dBc
3rd Harmonic Distortion[f]	HD_3			Room Full		−58	−50 −45	
Equivalent Input Noise Floor[d]	SNF	f >100 kHz, 50 Ω on Input		Room Full		−155	−153 −152	dBm (1 Hz)

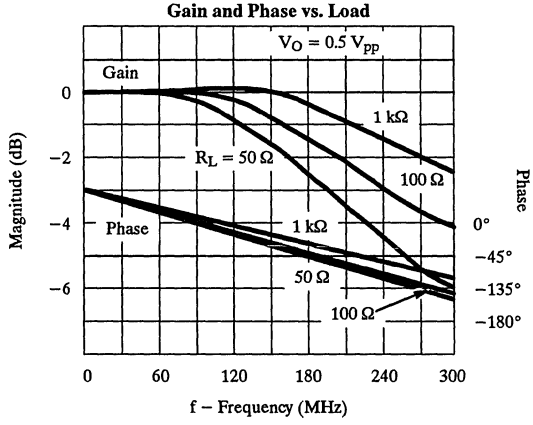
3

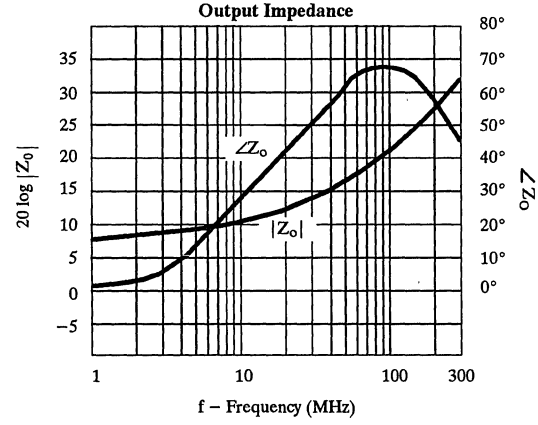
Specifications

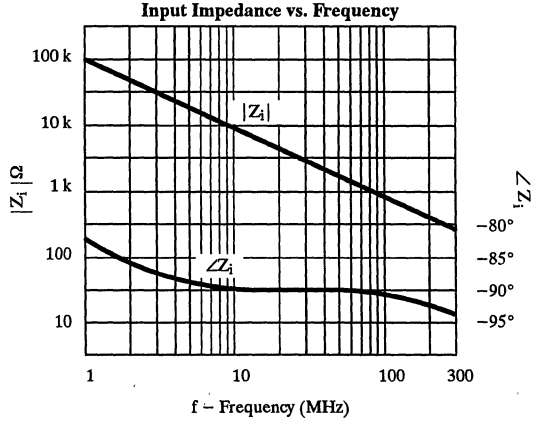
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V, R_L = 100 Ω, R_S = 50 Ω		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Performance Driving a DG884 Crosspoint Switch[d, g]								
2nd Harmonic Distortion	HD_2	See Test Load See Figure 1	V_{IN} = 2 V_{p-p}, f_{IN} = 5 MHz	Room		−60		dBc
3rd Harmonic Distortion	HD_3			Room		−58		
Differential Phase	DP		f = 3.58 or 4.43 MHz	Room		0.1		deg
Differential Gain	DG			Room		0.08		%
Crosstalk (All Hostile)	$X_{TALK(AH)}$		f = 10 MHz	Room		−54		dB

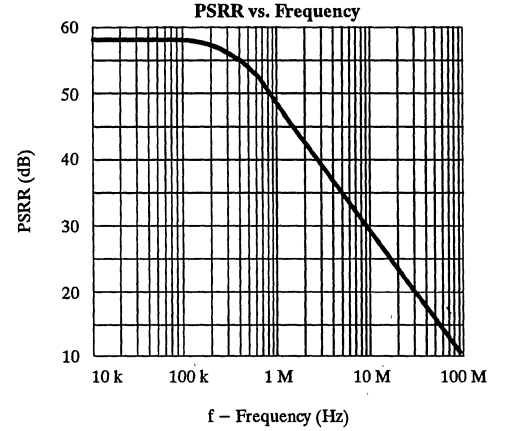
Notes:
a. Room = 25°C, Full = −40 to 85°C.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. Parameter is 100% tested at 25°C and sample tested at 85°C.
f. Parameter is sample tested at 25°C.
g. AC performance is very dependent on layout. Specifications apply only in a 50-Ω microstrip environment.

Typical Characteristics: T_A = 25°C, V_{CC} = ±5 V, R_L = 100 Ω



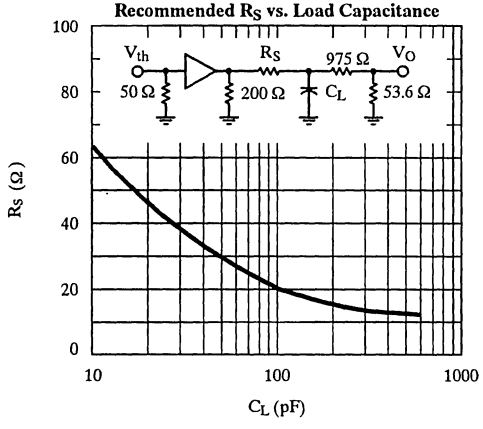




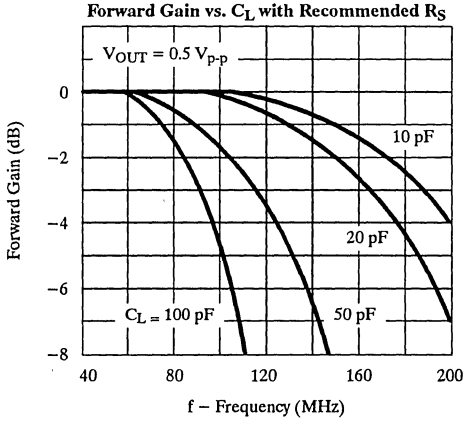


Typical Characteristics: $T_A = 25°C$, $V_{CC} = \pm 5$ V, $R_L = 100\ \Omega$ (Cont'd)

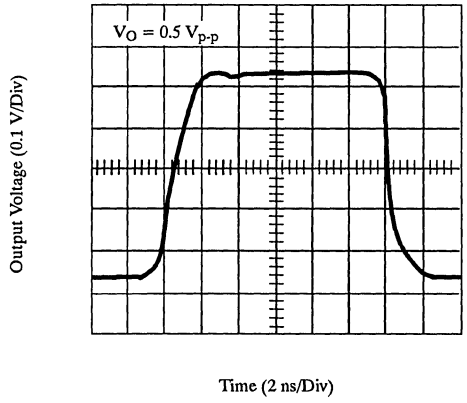
Recommended R_S vs. Load Capacitance



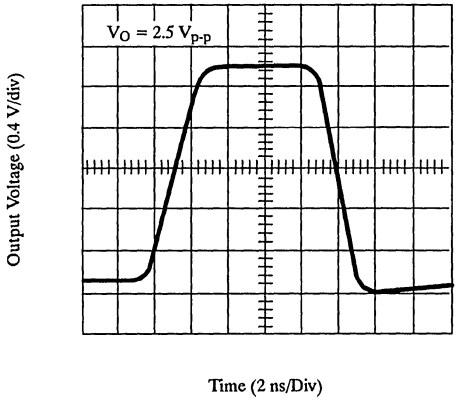
Forward Gain vs. C_L with Recommended R_S



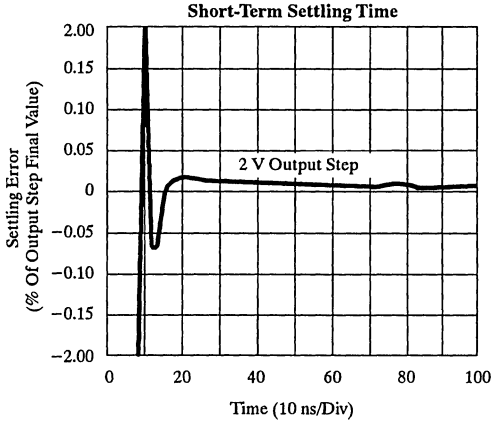
Small Signal Pulse Response



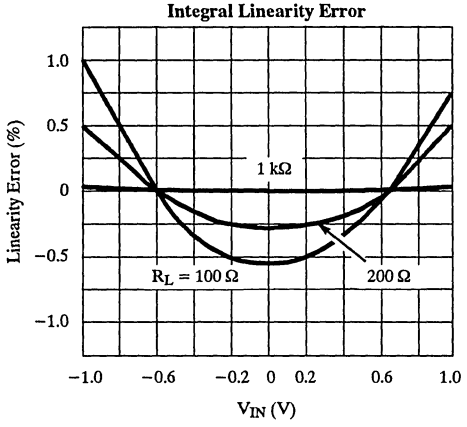
Large Signal Pulse Response



Short-Term Settling Time



Integral Linearity Error



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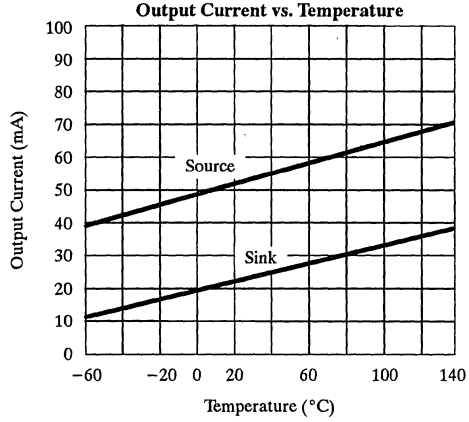
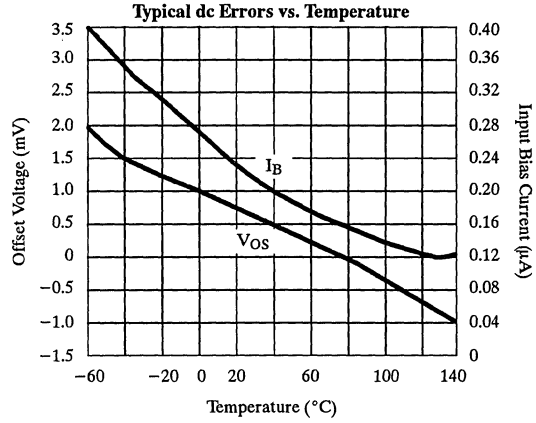
Typical Characteristics: $T_A = 25°C$, $V_{CC} = \pm 5$ V, $R_L = 100\ \Omega$ (Cont'd)

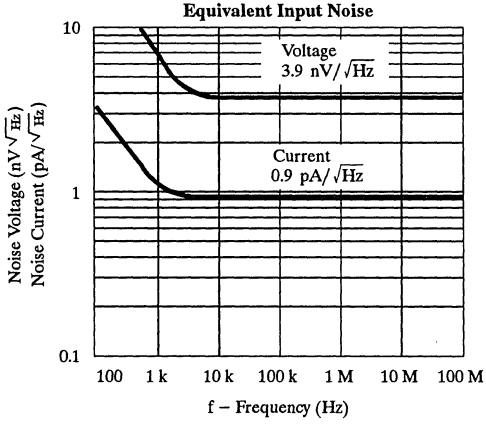
Output Current vs. Temperature



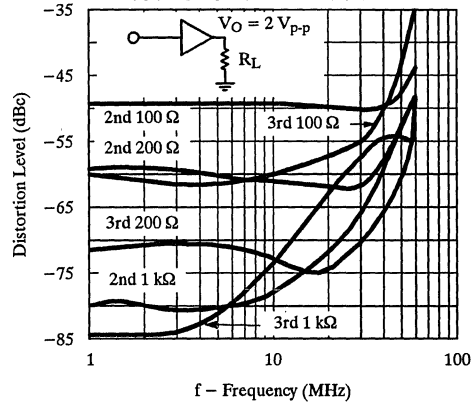
Typical dc Errors vs. Temperature



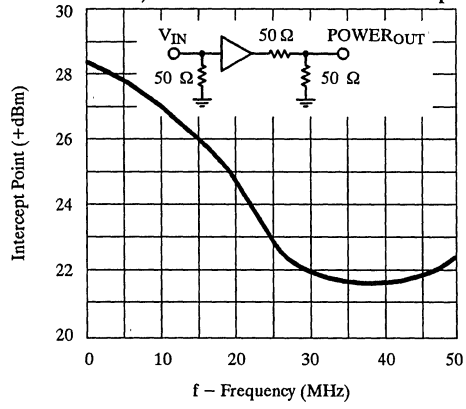
Equivalent Input Noise



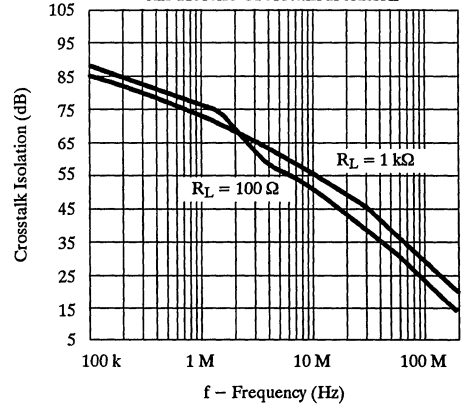
2nd and 3rd Harmonic Distortion



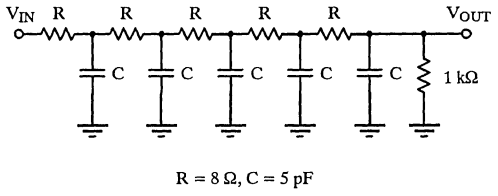
2-Tone, 3rd Order Intermodulation Intercept



All-Hostile Crosstalk Isolation



Test Circuit



R = 8 Ω, C = 5 pF

Figure 1. Test Load

Applications

Operation

The Si584 is a quad unity gain buffer that offers high-speed and low-power operation. Its closed loop topology provides higher accuracy than that normally found in open loop designs. The Si584 was designed to optimize differential gain and phase when driving the distributed capacitance of a video multiplexer or crosspoint such as the DG884.

Board Layout and Crosstalk

High frequency designs demand good PC board layout for best performance. A ground plane and power supply bypassing with high-frequency ceramic capacitors adjacent to the power supply pins are essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and negative supplies. This is accomplished by connecting one side of the bypass capacitors at the same point in the ground plane while keeping the supply sides within 0.1" of the Si584 supply pins.

Crosstalk is strongly dependent on board layout. Closely spaced signal traces on the board will degrade crosstalk due to capacitive coupling. A grounded guard trace between signal traces will reduce crosstalk by reducing intertrace capacitance. For this same reason it is recommended that unused pins (2, 4, 6, 11) be connected to the ground plane.

"All-Hostile" crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven, channel.

Unused Buffers

It is recommended that the inputs of any unused buffers be tied to ground through 50-Ω resistors.

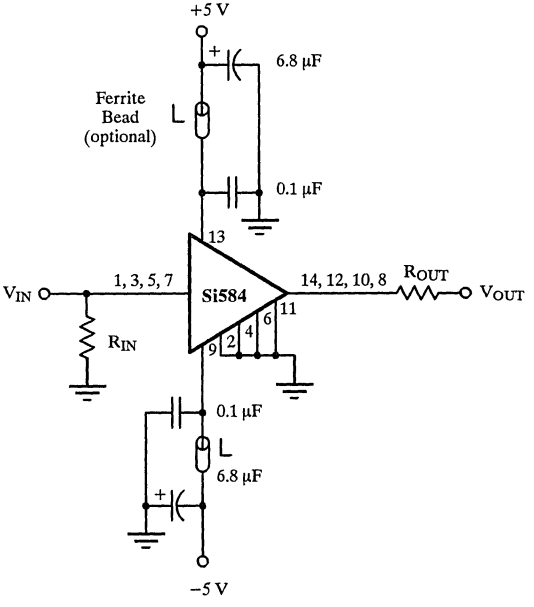


Figure 2. Decoupling the Si584

Minimum Parts Count 80-MHz Video Switcher

Figure 3 illustrates a fully buffered 8 × 4 video switching matrix capable of handling 80-MHz signals with only four ICs. At the heart of this circuit is the DG884 crosspoint. U1 and U2 buffer all eight inputs while U4 can drive a second level of switching elements.

Applications (Cont'd)

It is worth noting that every time a video signal is processed by an active or passive component, its bandwidth is subject to a reduction due to each individual processing element's own bandwidth. That is why, even when switching baseband video, it is better to use a broadband switcher in order to preserve signal quality and fidelity.

For lower bandwidth applications one Si584 output can drive up to four DG884 inputs. This is useful when building larger matrices (8 × 8, 8 × 16, etc.).

Providing the receiving end is properly terminated, the Si584 can also be used as a cable driver for short distances. When driving long cables that may or may not be properly terminated it is better to use a back terminated cable driver with a 6-dB gain. This driving method reduces transmission line reflections. The Si582 is recommended for this type of application.

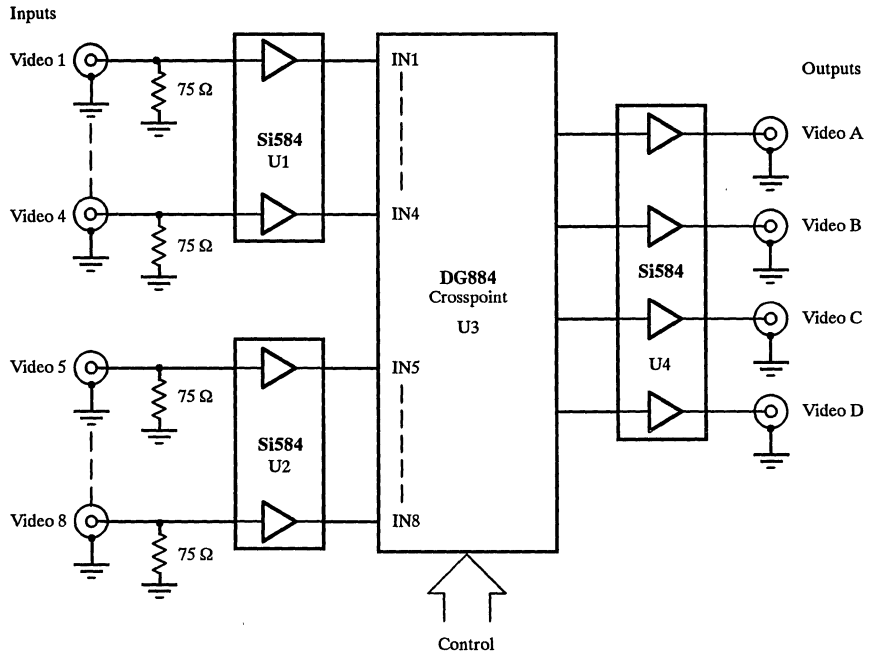


Figure 3. Minimum Parts Count 80 MHz 8 × 4 Video Switching Matrix

About Siliconix Voltage Converters

Siliconix presently supplies three types of power conversion circuits: charge pump voltage converters, high-voltage switchmode regulators, and high-voltage switchmode controllers.

Our family of low-cost switched capacitor voltage converters are used in applications where a single dc supply is available. These monolithic products feature high conversion efficiency, minimum noise and distortion, and minimum space requirements. They can be configured for voltage inversion or voltage doubling, and require only a few external components (typically two electrolytic capacitors). A typical application would be negative rail generation in a circuit with a battery supply.

The Si7660 is a voltage converter that inverts or boosts input voltages from the 1.5- to 10-V range. It features power conversion efficiencies up to 98%. The Si7661 is a higher-voltage version of the Si7660 intended for input voltages from 7.5 V to 20 V.

The high-voltage switchmode regulators and controllers made by Siliconix employ high-performance D/CMOS power IC technology to combine CMOS current-mode controllers with high-voltage input regulation and output switching. This design allows Siliconix to build extremely high efficiency switchmode power supply circuits that can run directly from high-voltage inputs such as PBX or ISDN phone lines, or 100-VAC power lines.

The data sheets for Si91xx family of switchmode regulators and controllers may be found in the ***Siliconix Power Products Data Book***.

Voltage Converters

Part Number	Max Supply Current (mA)	Min Supply Voltage (V)	Max Supply Voltage (V)	Min Output Voltage (V)	Max Output Voltage (V)	Package	Page
Si7660	0.175	1.5	10	−10	20	J, Y	4-1
Si7661	2	4.5	20	−20	40	J	4-7

J = Plastic DIP Y = SOIC

Switched-Capacitor Voltage Converter

Features

- 99.7% Open Circuit Voltage Conversion Efficiency
- 98% Power Efficiency
- Operating Voltage Range of 1.5 to 10 V
- Requires Only Two Capacitors

Benefits

- Inexpensive Negative Supply from Positive Supply
- Easy to Use
- Minimum Parts Count
- Small Size
- No Diode Drop at Output
- Low Cost

Applications

- Conversion of 5-V Logic Supply to ± 5-V Supplies
- Negative Supply for Dynamic RAMs
- RS-232 Power Supply
- Negative Supplies for Analog Circuits
- Data Acquisition Systems
- Hand-Held Instruments
- High-Side Load Switches

Description

The Si7660 is a monolithic CMOS switched-capacitor voltage converter that inverts ($V_{OUT} = -V_{IN}$), doubles ($V_{OUT} = 2\ V_{IN}$), divides ($V_{OUT} = V_{IN}/2$), or multiplies ($V_{OUT} = \pm n\ V_{IN}$) an input voltage. Operation with no external diode is guaranteed over the full temperature range for input voltages ranging from 1.5 V to 10 V.

The Si7660 combines low quiescent current with high efficiency and reliability. Included on chip are an oscillator, control circuitry and four power MOS switches. An epitaxial layer prevents latchup.

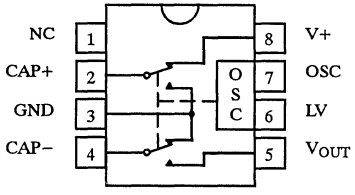
The oscillator, when unloaded, runs at a nominal 12 kHz. The OSC pin may be used to change the running frequency. The LV pin should be tied to ground to improve low voltage operation ($V+ \leq 3.5$ V). For $V+ > 3.5$ V, the LV pin should be left disconnected.

Typical applications include generating a −5-V supply from a 5-V logic supply to power analog circuits, generating 6 V from a 3-V lithium cell, or 3 V from a single 1.5-V cell.

For additional information please refer to Applications Note AN401.

Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	8-Pin Plastic MiniDIP	Si7660CJ
−40 to 85°C	8-Pin Plastic MiniDIP	Si7660DJ
	8-Pin Narrow SOIC	Si7660DY

4

Absolute Maximum Ratings

Supply Voltage (V+ to GND or GND to V_{OUT}) ..... 11 V
Oscillator Input Voltage:
(V+ < 5.5 V) ..... −0.3 V to (V+) +0.3 V
(V+ > 5.5 V) ..... (V+) −5.5 V to (V+) +0.3 V
LV ..... No connection for V+ > 3.5 V
Storage Temperature ..... −65 to 125°C

Power Dissipation:[a]
8-Pin Plastic DIP[b] ..... 300 mW
8-Pin SOIC[b] ..... 300 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 10 mW/°C above 75°C

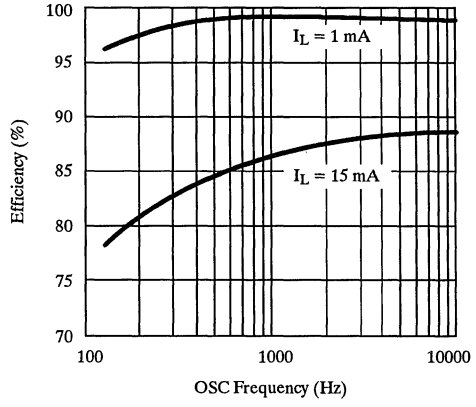
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, C_{OSC} = 0[d]	Temp[a]	Limits Min[b]	Typ[c]	Max[b]	Unit
Input							
Supply Voltage Range Low	$V+_L$	R_L = 10 kΩ, LV = GND	Full	1.5		3.5	V
Supply Voltage Range High	$V+_H$	R_L = 10 kΩ, LV = Open	Full	3		10	V
Supply Current	I+	R_L = ∞, LV = Open	Full		100	175	µA
Output							
Output Source Resistance	R_{OUT}	V+ = 5 V, LV = Open, I_O = 20 mA	Room Full		55	100 120	Ω
		V+ = 2 V, LV = GND, I_O = 3 mA	Full			300	Ω
Power Conversion Efficiency	PE_1	R_L = 5 kΩ	Room	95	98		%
Voltage Conversion Efficiency	$V_{OUT}E_1$	R_L = ∞	Room	99	99.9		%
Dynamic							
Oscillator Frequency[d]	f_{OSC}		Room		12		kHz
Oscillator Impedance	Z_{OSC}	V+ = 2 V, LV = GND	Room		1		MΩ
		V+ = 5 V	Room		100		kΩ

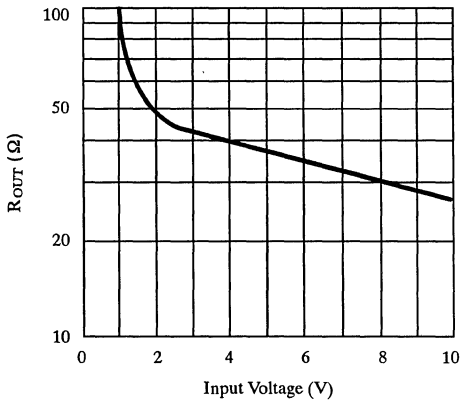
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. For C_{OSC} > 1000 pF, C_1 and C_2 should be increased to 100 µF. C_1 = Pump Capacitor, C_2 = Reservoir Capacitor.

Typical Characteristics

Power Conversion Efficiency vs. OSC Frequency

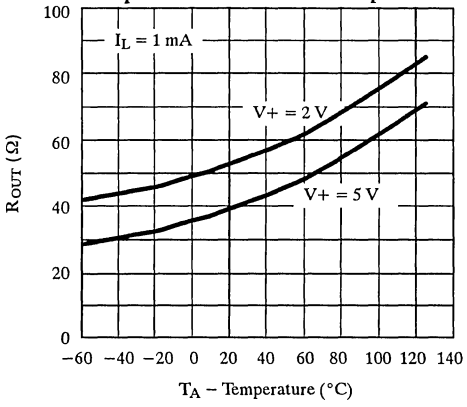


Output Resistance as a Function of Supply Voltage

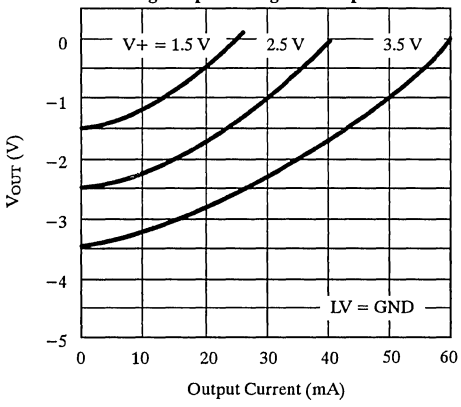


Typical Characteristics (Cont'd)

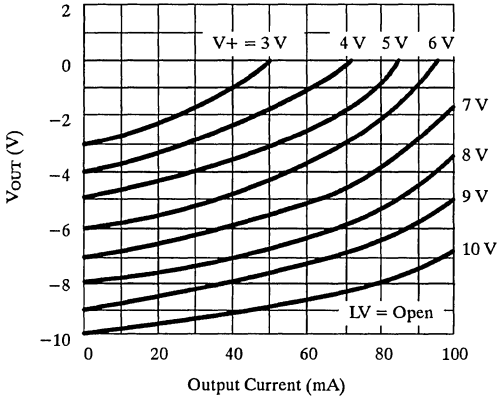
Output Source Resistance vs. Temperature



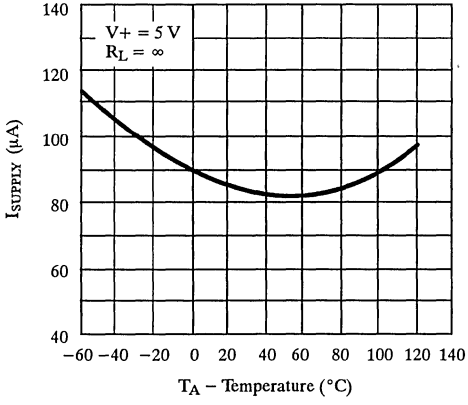
Inverting Output Voltage vs. Output Current



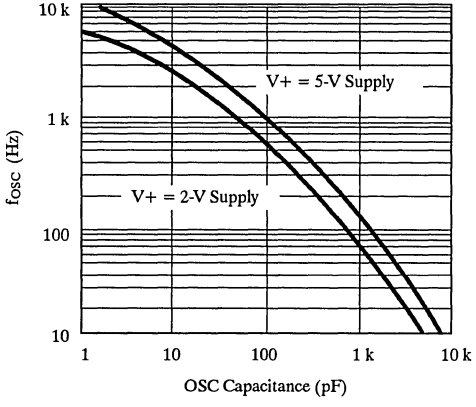
Inverting Output Voltage vs. Output Current



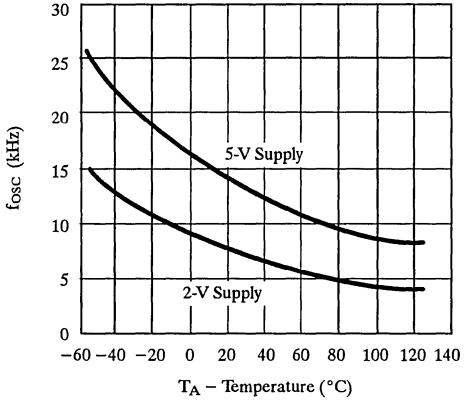
Supply Current vs. Temperature



Oscillation Frequency as a Function of External OSC Capacitance

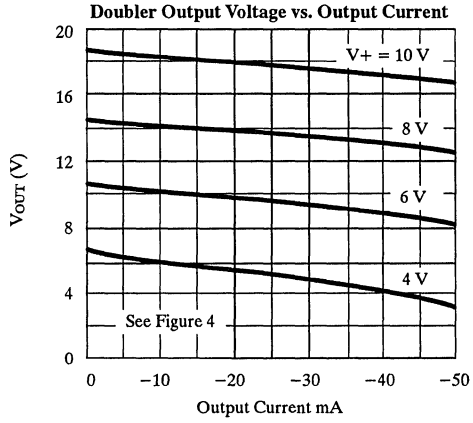


Unloaded Oscillation Frequency as a Function of Temperature



4

Typical Characteristics (Cont'd)



Schematic Diagram

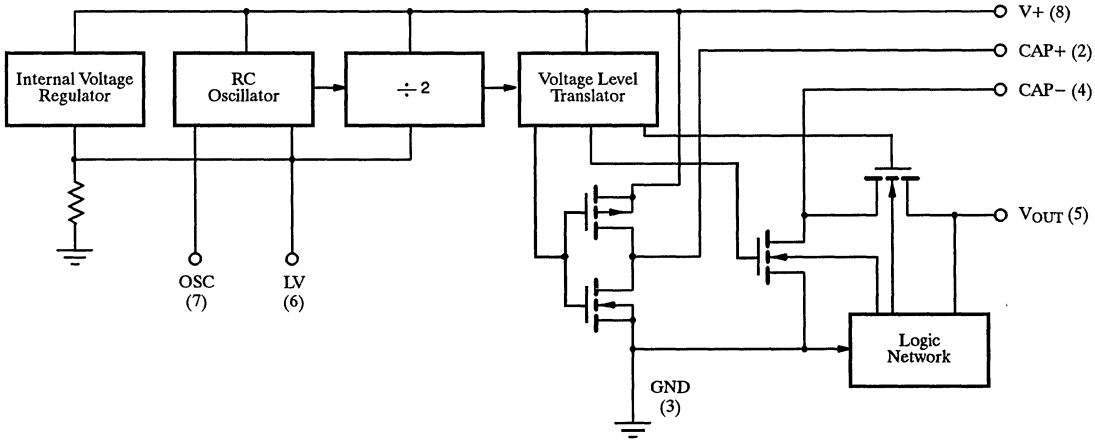


Figure 1.

Test Circuit

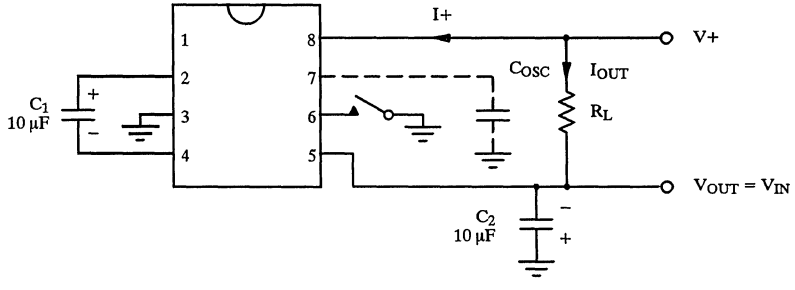


Figure 2.

Applications

There are many applications where a low current supply made with a charge pump does just as well as a conventional, fully regulated negative supply or dc-to-dc converter module. The Si7660 contains all the circuitry necessary to make a charge pump for voltage inversion, doubling, division, multiplication, etc. Only two external capacitors are needed and they may be inexpensive electrolytics. Since the output resistance is in the tens of ohms, heavy load currents will reduce the output voltage and eventually may cause the device to go into shutdown.

If the output ripple of the Si7660 is too great for a particular application, the value of the pump (C_1, Figure 3) and reservoir (C_2, Figure 3) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded. The maximum recommended capacitor size is 1000 µF.

A previous version of the Si7660 required a diode in series with Pin 5 when operating above 6.5 V. The current Si7660 does not require this diode, but will work in existing circuits which have the diode.

Figure 4 shows a circuit that will produce two output voltages utilizing both of the Si7660 features (i.e. inversion and doubling). The combined output current must be limited so the maximum device dissipation is not exceeded.

Two Si7660s can be paralleled to reduce the effective output resistance of the converter. The output voltage at a given current is increased since the voltage drop is halved when the devices are connected as shown in Figure 6.

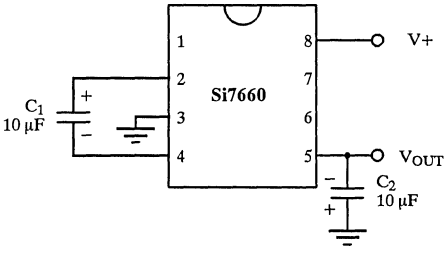


Figure 3. Basic Inverter Circuit

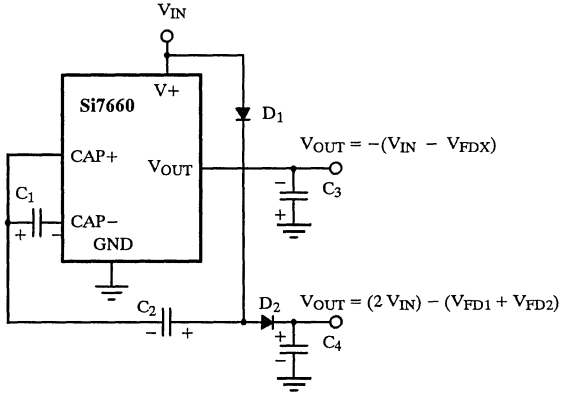


Figure 4. Combination Inverter/Doubler Circuit

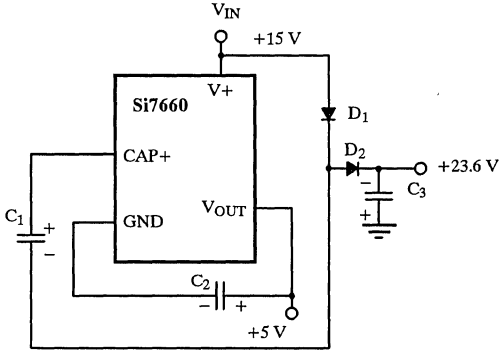


Figure 5. Creating +23.6 V from +15 V and +5 V

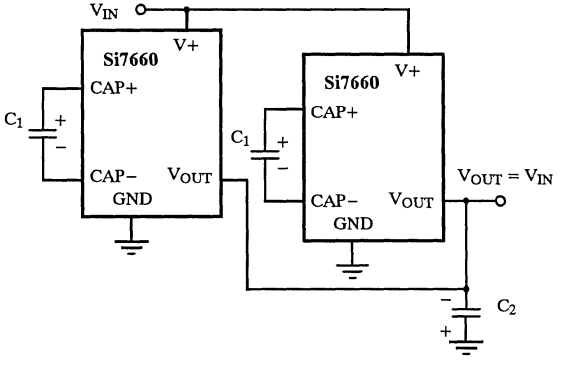


Figure 6. Paralleling Two Si7660s to Reduce the Effective Output Resistance

Applications (Cont'd)

Battery Splitter

To obtain supplies from a single battery or power supply, the circuit shown in Figure 7 offers a simple solution. It generates symmetrical ± output voltages equal to one-half the input voltage. Both output voltages are referenced to Pin 3 (output common). To improve low voltage operation, Pin 6 should be connected to Pin 3 when the input voltage is less than 3.5 V.

High Precision Voltage Divider

A high precision voltage divider is shown in Figure 8. Increasing the load current beyond 100 nA will cause a small loss in accuracy.

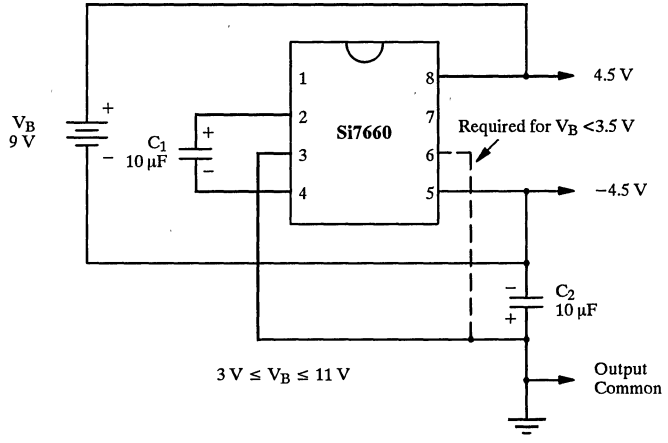


Figure 7. Battery Splitter

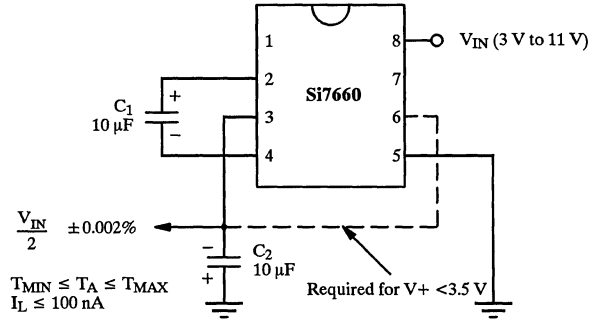


Figure 8. High Precision Voltage Divider

Switched-Capacitor Voltage Converter

Features

- Wide Operating Supply Voltage Range: 4.5 V to 20 V
- 99.7% Open Circuit Voltage Conversion Efficiency
- 95% Power Conversion Efficiency

Benefits

- Inexpensive Negative Supply Generation
- Easy to Use, Requires Only Two External Capacitors
- Minimum Parts Count
- Small Size

Applications

- Conversion of +12-V to ± 12-V Supplies
- RS-232 Power Supply
- Negative Supplies for Analog Circuits
- Data Acquisition Systems
- Handheld Instruments
- High-Side Load Switches

Description

The Si7661 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7661 performs a supply voltage conversion from positive to negative for an input range of +4.5 V to +20 V, resulting in a complementary output voltage of −4.5 V to −20 V with the addition of only two capacitors.

Typical applications for the Si7661 are data acquisition and microprocessor based systems, where a +5- to +20-V supply is available for the digital functions, and an additional −5- to −20-V supply is required for analog devices, such as op amps. The Si7661 is also ideally suited for providing low current, −5-V body bias supply for dynamic RAMs.

Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output n-channel switch substrates are not forward-biased. An epitaxial layer prevents latchup.

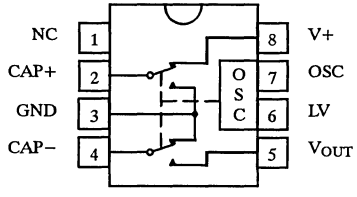
The oscillator, when unloaded, runs at a nominal frequency of 10 kHz for an input supply voltage of 4.5 to 20 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+8 to +20 V), the "LV" pin should be left disconnected.

For applications information refer to AN401.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	8-Pin Plastic MiniDIP	Si7661CJ
−40 to 85°C		Si7661DJ

Absolute Maximum Ratings

Supply Voltage (V+ to GND or GND to V_{OUT}) ..... 22 V
Oscillator Input Voltage
V+ <8 V ..... −0.3 V to (V+) +0.3 V
V+ >8 V ..... (V+) −8 V to (V+) +0.2 V
LV ..... No connection for V+ >9 V
Storage Temperature ..... −65 to 125°C

Power Dissipation:[a]
8-Pin Plastic MiniDIP[b] ..... 500 mW

Notes:
a. All leads welded or soldered to PC board.
b. Derate 6.6 mW/°C above 25°C.

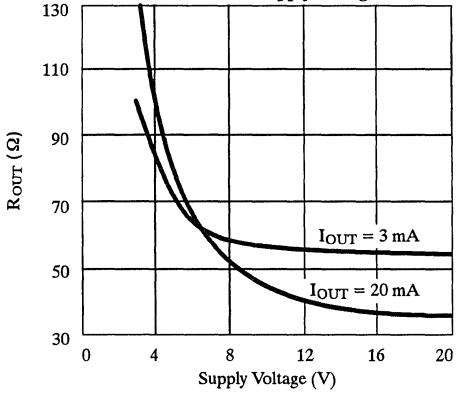
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, C_{OSC} = 0[d]	Temp[a]	Limits Min[b]	Typ[c]	Max[b]	Unit
Input							
Supply Voltage Range Low	$V+_L$	R_L = 10 kΩ, LV = GND	Full	4.5		9	V
Supply Voltage Range High	$V+_H$	R_L = 10 kΩ, LV = Open	Full	8		20	V
Supply Current	I+	V+ = 4.5 V, R_L = ∞, LV = GND	Full		100	200	µA
		V+ = 15 V, R_L = ∞, LV = Open	Full		0.7	2	mA
Output							
Output Source Resistance	R_{OUT}	V+ = 4.5 V, LV = GND, I_{OUT} = 3 mA	Room		35		Ω
		V+ = 15 V, LV = Open, I_{OUT} = 20 mA	Room		30	100	Ω
			Full			120	Ω
Power Conversion Efficiency	P_{EF}	V+ = 15 V, R_L = 2 kΩ	Room		92		%
Voltage Conversion Efficiency	V_{EF}	V+ = 15 V, R_L = ∞	Room	97	99.7		%
Dynamic							
Oscillator Frequency[d]	f_{OSC}	V+ = 15 V	Room		10		kHz
Oscillator Impedance	Z_{OSC}	V+ = 4.5 V, LV = GND	Room		1		MΩ
		V+ = 15 V	Room		100		kΩ

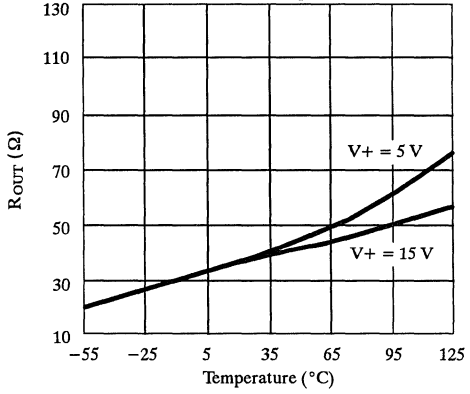
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. For C_{OSC} > 1000 pF, C_1 and C_2 should be increased to 100 µF. C_1 = Pump Capacitor, C_2 = Reservoir Capacitor.

Typical Characteristics

Output Source Resistance as a Function of Supply Voltage

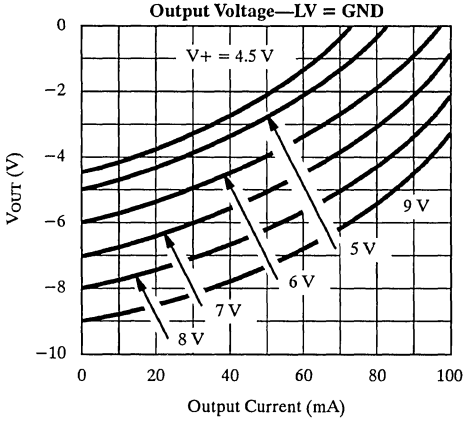


Output Source Resistance as a Function of Temperature

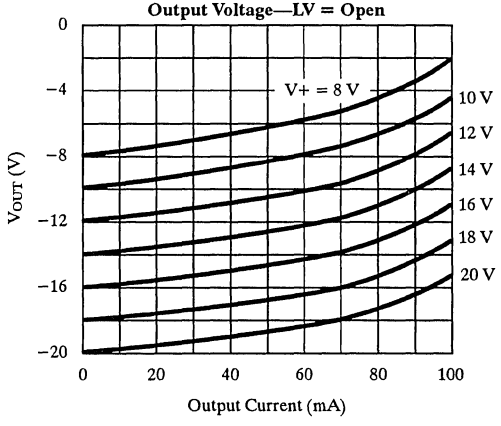


Typical Characteristics (Cont'd)

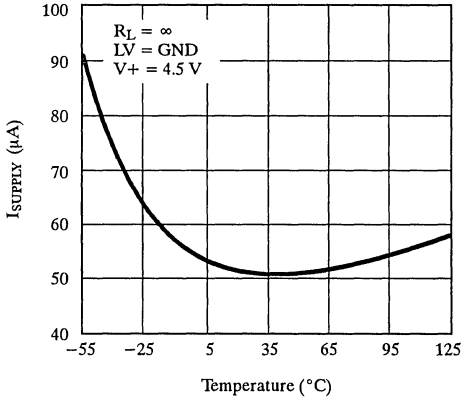
Output Voltage—LV = GND



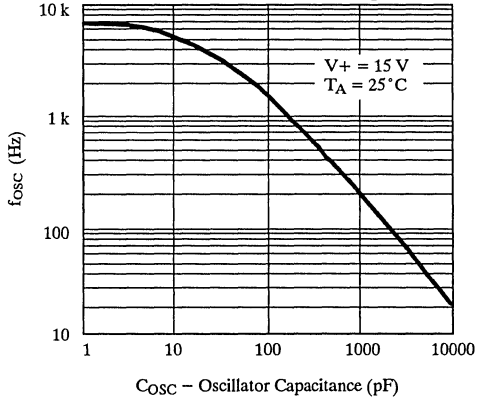
Output Voltage—LV = Open



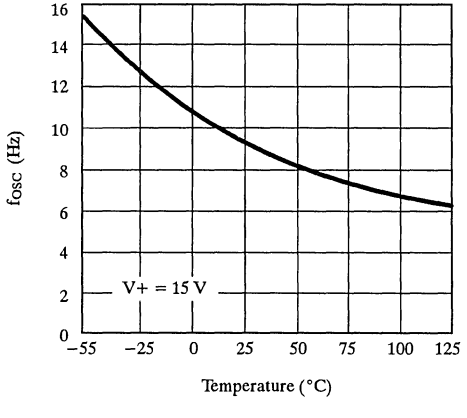
Supply Current vs. Temperature



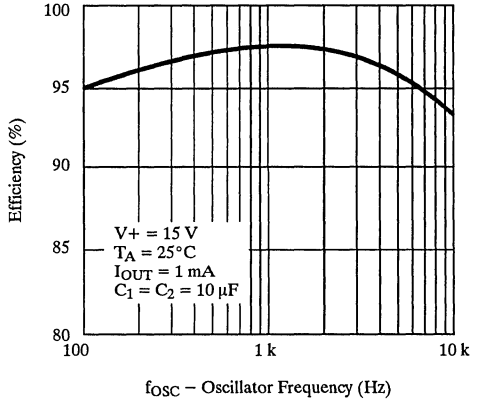
Frequency of Oscillation as a Function of External Oscillator Capacitance



Unloaded Oscillator Frequency as a Function of Temperature



Power Efficiency vs. Oscillator Frequency



4

Schematic Diagram

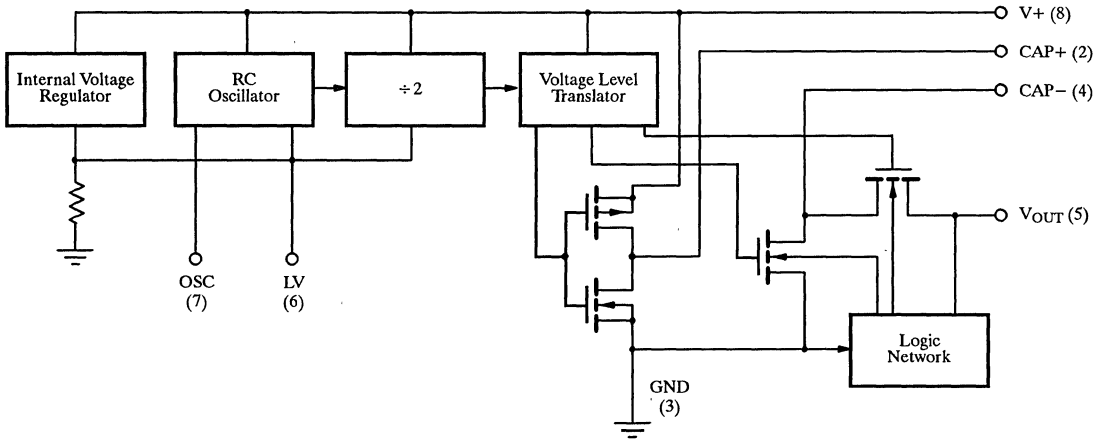


Figure 1.

Test Circuit

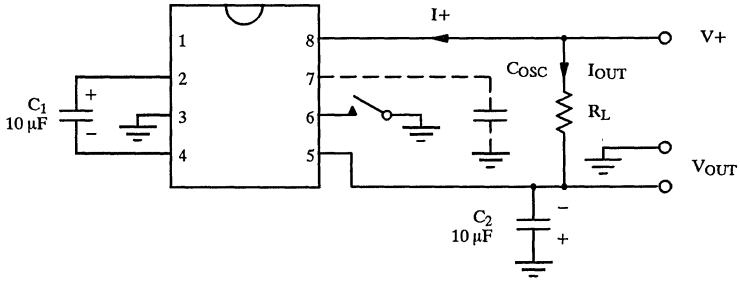


Figure 2.

Applications

The Si7661 contains all the circuitry necessary to make a charge pump for voltage inversion, doubling, division, multiplication, etc. Only two external capacitors are needed and they may be inexpensive electrolytics. Since the output resistance is in the tens of ohms, heavy load currents will reduce the output voltage and eventually may cause the device to go into shutdown.

There are many applications where a low current supply made with a charge pump does just as well as a conventional, fully regulated negative supply or dc-to-dc converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems. In addition, the extended input voltage range of the Si7661 lends itself for use as a negative generator for most op-amp applications.

Applications (Cont'd)

If the output ripple of the Si7661 is too great for a particular application, the value of the pump (C_1, Figure 3) and reservoir (C_2) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000 µF.

When an external clock is used to drive the Si7661 a 1-kΩ resistor should be used between the clock source and the OSC input (Pin 7) as shown in Figure 4.

Figure 5 shows a regulator that will operate with much less than 1-V drop between V+ and V_{OUT} at large output currents. Most three-terminal voltage regulators would exhibit a drop of a volt or more under these conditions.

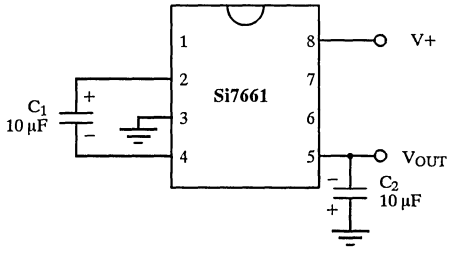


Figure 3. Basic Inverter Circuit

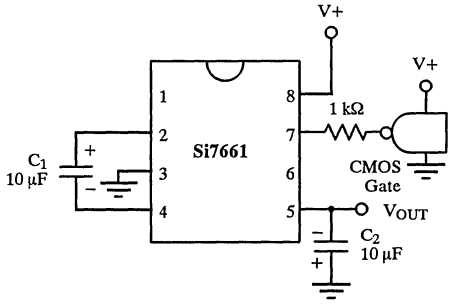


Figure 4. Driving the Si7661 with an External Clock

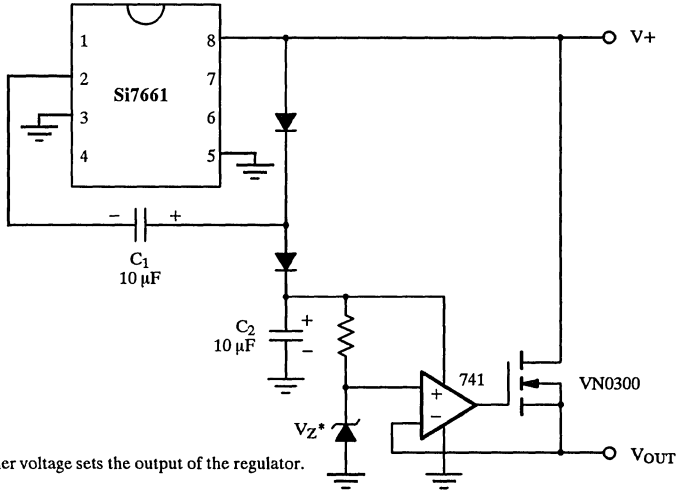


Figure 5. Low Loss Regulator Circuit

Applications (Cont'd)

Battery Splitter

To obtain supplies from a single battery or power supply, the circuit shown in Figure 6 offers a simple solution. It generates symmetrical ± output voltages equal to one-half the input voltage. Both output voltages are referenced to Pin 3 (output common). To improve low-voltage operation, Pin 6 should be connected to Pin 3 when the input voltage is less than 9 V.

High Precision Voltage Divider

A high precision voltage divider is shown in Figure 7. Increasing the load current beyond 100 nA will cause a small loss in accuracy.

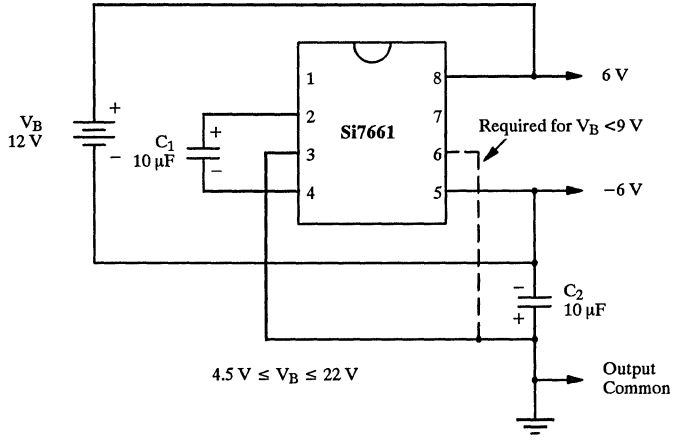


Figure 6. Battery Splitter

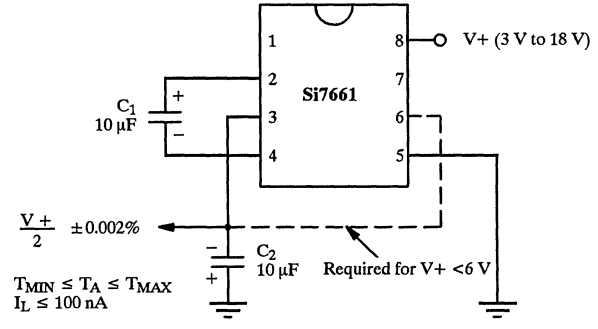


Figure 7. High Precision Voltage Divider

Application Notes

The following literature is designed to help you use Siliconix products in your applications. Call our FaxBack system (408-970-5600) to have the document sent to you immediately via facsimile, or to order a copy to be sent by mail, call 800-554-5565.

Application Note Number	FaxBack Code Number	Title
Analog Switches and Multiplexers		
TA201	9201	High-Performance Multiplexing with the DG408
AN203	9203	Silicon-Gate Switching Functions Optimize Data Acquisition Front Ends
AN204	9204	Serially-Controlled Eight-Channel Analog Switch Array Simplifies Signal Conditioning and Routing
AN205	9205	Overvoltage Protection for CMOS Switches and Multiplexers
AN206	9206	DG406 Multiplexer Optimizes Medical Simulator
AN207	9207	15-ns DG611 Switch Family Combines Benefits of CMOS and DMOS Technologies
DMOS		
AN301	9301	DMOS FET Analog Switches and Switch Arrays
JFETs		
AN101	9101	An Introduction to FETs
AN102	9102	FET Biasing
AN103	9103	The FET Constant-Current Source
AN104	9104	SPICE Parameters for Select JFETs
AN105	9105	FETs As Voltage-Controlled Resistors
LITTLE FOOT® MOSFETs		
AN801	8801	Designing with Complementary Power MOSFETs in Surface-Mount (SO-8) Packages
AN802	8802	Low-Voltage Motor Drive Designs Using N-Channel Dual MOSFETS in Surface-Mount Packages
AN803	8803	Thermal Characteristics of Siliconix's LITTLE FOOT Family of Surface-Mount MOSFETs
AN804	8804	P-Channel MOSFETs, the Best Choice for High-Side Switching
Low-Power FETs		
AN901	8901	Depletion-Mode MOSFETs Expand Circuit Opportunities
Power MOSFETs		
AN601	8601	Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments
Power ICs		
AN701	8701	A 1-Watt Flyback Converter Using the Si9100
AN702	8702	Efficient ISDN Power Converters Using the Si9100
AN703	8703	Designing DC/DC Converters with the Si9110 Switchmode Controller
AN704	8704	Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals
AN705	8705	The Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications
AN706	8706	Motor Drive Circuits Using the D469A
AN707	8707	Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC
AN708	8708	Low-Power Universal-Input Power Supply Achieves High Efficiency
AN709	8709	Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs
AN710	8710	High-Efficiency Buck Converter for Notebook Computers
AN711	8711	HDD Servo Design Using the Si9990CS
AN712	8712	A High-Voltage Half-Bridge Using the Si9901 with the Si9911 or Si9914
Video ICs		
AN501	9501	The DG535/536 Wideband Multiplexers Suit a Wide Variety of Applications
AN502	9502	Microprocessor-Compatible Multiplexers Facilitate Video Switching Designs
AN503	9503	Si581 Wideband Buffer Applications
AN504	9504	Video Crosspoint Switch Simplifies Large Matrix Designs
Voltage Converters		
AN401	9401	Theory and Applications of the Si7660 and Si7661 Voltage Converters

Reliability Information

Introduction

Reliability at Siliconix is ensured with two primary programs: the Reliability Qualification Program and the Reliability Monitoring Program. Siliconix publishes this data by product family and it can be obtained by request through your local sales office.

Qualification Program

Qualification programs of accelerated stress testing are developed for the introduction of new devices (die qualifications), packages, major process changes, new materials or suppliers, new manufacturing equipment, and new manufacturing locations.

A qualification starts after a qualification test plan is developed. This plan specifies the following:

- Purpose and scope
- Device or geometry types and packages being qualified
- Process and assembly specs involved
- Test vehicles and location
- Tests and stresses
- Duration of each stress
- Sample sizes
- Acceptance criteria
- Number of lots required

Monitoring Program

The Reliability Monitoring Program, which includes accelerated life tests, is designed to continuously monitor product reliability. The program furnishes up-to-date failure-rate and failure-mechanism data which can be used to predict and improve long-term reliability performance. The Monitoring Program covers a wide range of technologies and product lines manufactured by Siliconix. In order to accomplish this, products are grouped by similar technologies. For example, components built in the same wafer fab, using the same manufacturing processes, having similar complexity, functionality, and package types are grouped into a technology family. One component or more representing each technology group is monitored according to a quarterly schedule. An internal Reliability Performance Monitor report is issued monthly and is reviewed by all engineering groups to ensure improvement of product reliability.

The short-term and long-term monitor tests are outlined in Tables 1 and 2. Also, the Reliability Monitor Program is summarized in general outline form as a flow chart in Figure 1 and with operating life data in Table 3.

Accelerated Reliability

Accelerated tests were developed to shorten the time required for reliability testing. The life cycle of a component is accelerated by applying stress that is more severe than that encountered under normal operating conditions. This acceleration is produced by elevating temperatures, increasing humidity or pressure, alternating hot and cold temperature, switching power on and off, or some combination of these conditions. The test results are used to predict normal operating performance. In the sections below we present a brief description of each stress.

Summary of Tests

High Temperature Operating Life

The high-temperature operating life accelerated test, commonly referred to as "burn-in," is performed at typically 125°C and 150°C under electrical bias.

The steady state and dynamic life tests determine the ability of a product to survive a host of potential failure modes, surface inversion, dielectric breakdown, and electromigration being typical examples.

Temperature Cycling Test

Temperature cycling exploits the differences in thermal coefficients of expansion between silicon and the other materials used in die fabrication and packaging. Each cycle consists of 10-minute exposures at −65°C and 150°C with a 1-minute transfer at room temperature between the temperature extremes. This test reveals potential weaknesses in die and package materials and construction and in the integration of the die and package.

Thermal Shock Test

The purpose of the thermal shock test is similar to that of temperature cycling. This stress is more extreme, however, due to the fact that the ambient medium is liquid and not air, and the transition time is much shorter than for temperature cycling.

Each cycle consists of a 5-minute exposure at −65°C and 150°C with a maximum 10-second transfer time between the temperature extremes.

Bias Humidity Test

The bias humidity test is used to test plastic packaged devices for the effects of moisture penetration while electrical potentials are applied. The components are placed in a biased condition and then are subjected for 1000 hours to a temperature of 85°C and a relative humidity 85%. This test confirms package integrity.

Pressure Pot Test

In the pressure pot test, water vapor is forced into non-hermetic packages via micro gaps in the package-lead seal. Water is then carried to the die surface via capillary action of the bond wires. Electrical leakage may result. External contamination of the package or lead finish may be transported to the die or may directly cause corrosion of the leads.

Table 1. Short-Term Reliability Monitor

Test	Condition	Sample Size	Test Points
Static Operating Life	125°C or 150°C	50	168 hours
Dynamic Operating Life			
Pressure Pot	121°C, 15 PSIG		48 hours (Plastic)
Thermal Shock	Liquid to liquid. −65°C to 150°C		100 cycles
Solderability	MIL-STD-883D, M2003	15 leads	(245°C ±5°C)
Lead Integrity	MIL-STD-883D, M2004		
Lid Torque	MIL-STD-883D, M2024		(Hermetic)
Marking Permanency	MIL-STD-883D, M2015	16 leads	
Salt Atmosphere	MIL-STD-883D, M1009	15 leads	24 hours (Hermetic)
ESD, Human Body Model	MIL-STD-883D, M3015	12 leads	

Table 2. Long-Term Reliability Monitor

Test	Condition	Sample Size	Test Points
Static Operating Life	125°C or 150°C	50	0, 168, 1000 hours
Dynamic Operating Life			
Biased Humidity (Plastic)	85°C, 85% relative humidity		0, 500, 1000 hours
Temperature Cycling	Air-to-air −65°C to 150°C		0, 250, 1000 cycles
Power Cycling	$\Delta T_J = 100°C$	30	0, 2000, 6000 cycles

Table 3.

High Temperature Operating Life Technology	Number of Units	Equivalent Device Hours at 55°C and 1.0 eV	FITs[a] at 60% CL[b]
Metal-Gate, HVMG	5605	4,618,752,555	0.43
Silicon-Gate, HVSG	4787	3,569,237,924	0.25

Notes:
a. 1 failure per billion device hours
b. Confidence Level

5

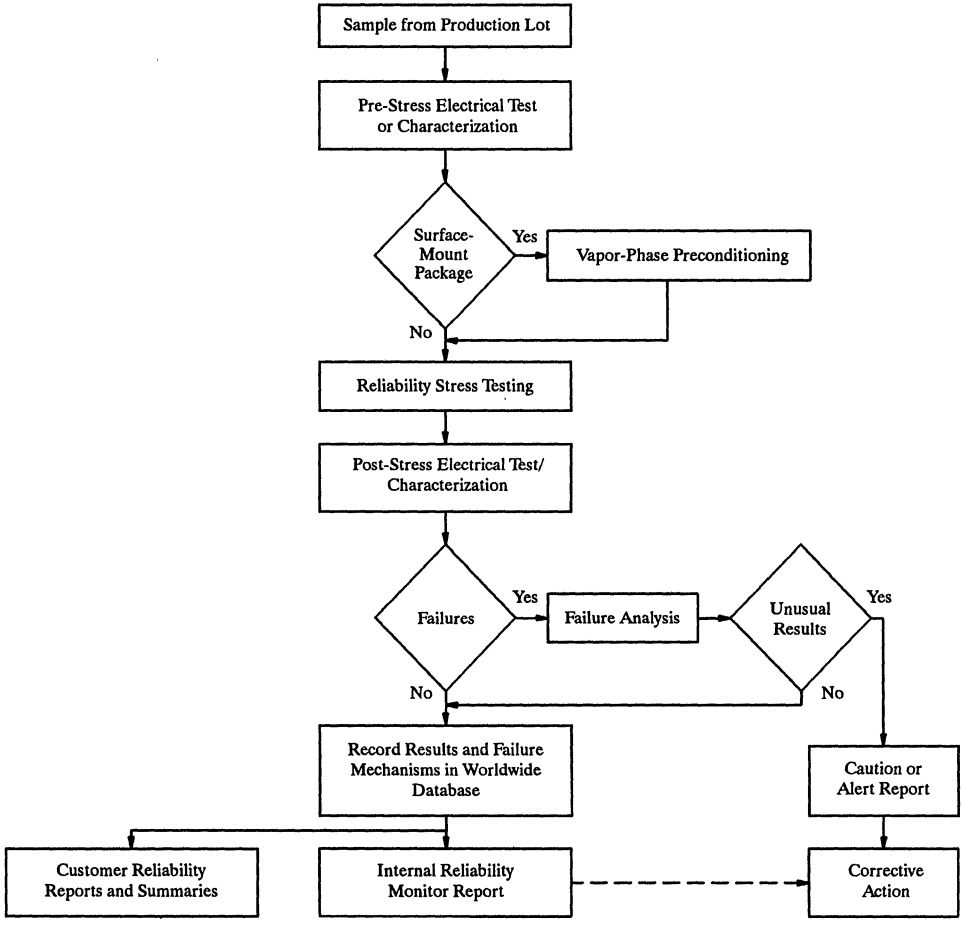
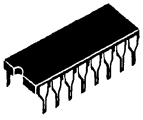
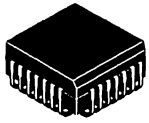


Figure 1. Reliability Monitor Flow (Short- and Long-Term Monitors)

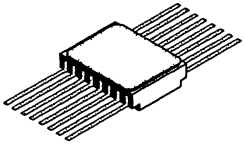
Package Information



CerDIP
8- to 16-Pin

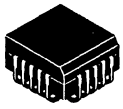


CerQuad
28- and 44-Pin

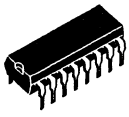


Flatpak
14- and 16-Pin

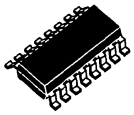
LCC
20- to 28-Pin



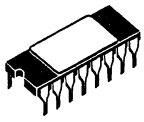
PLCC
20- to 44-Pin



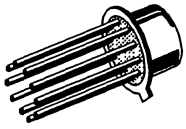
Plastic DIP
8- to 20-Pin



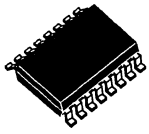
SOIC
8- to 16-Pin



Sidebraze Ceramic
14- to 24-Pin



TO-100 Metal Can
10-Pin



Wide-Body SOIC
16- to 28-Pin

Package Information

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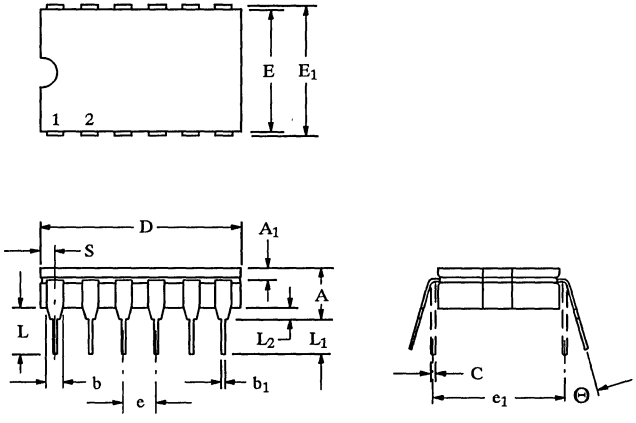
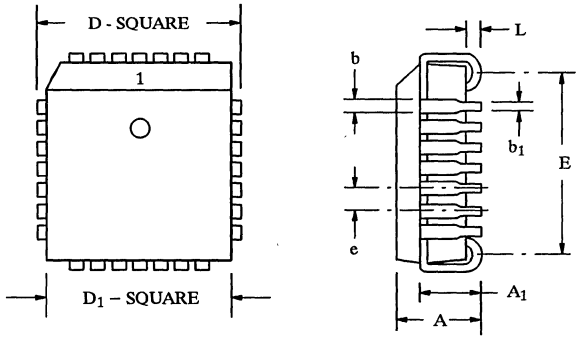
■ CerDIP, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	1.27	2.16	0.050	0.085
b	1.14	1.65	0.045	0.065
b_1	0.38	0.51	0.015	0.020
C	0.20	0.30	0.008	0.012
D–8	9.40	10.16	0.370	0.400
D–14	19.05	19.56	0.750	0.770
D–16	19.05	19.56	0.750	0.770
E	6.60	7.62	0.260	0.300
E_1	7.62	8.26	0.300	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	3.81	0.125	0.150
L_2	0.51	1.14	0.020	0.045
S–8	0.64	1.52	0.025	0.060
S–14	1.65	2.41	0.065	0.095
S–16	0.38	1.14	0.015	0.045
Θ	0°	15°	0°	15°

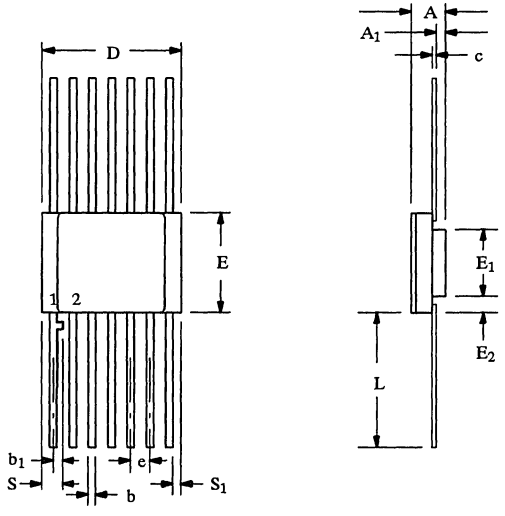
■ CerQuad Package, 28- and 44-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.83	0.165	0.190
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.46	0.56	0.018	0.022
D-28	12.32	12.57	0.485	0.495
D-44	17.40	17.65	0.685	0.695
D_1-28	11.23	11.63	0.442	0.458
D_1-44	16.31	16.71	0.642	0.658
E-28	9.91	10.92	0.390	0.430
E-44	14.99	16.00	0.590	0.630
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

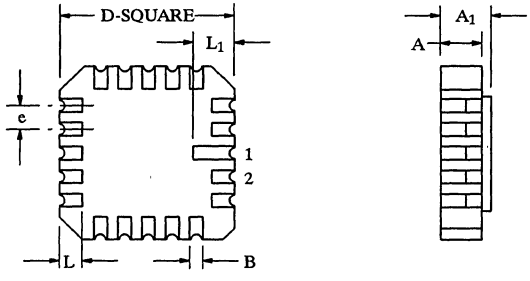
Package Information

■ Flat Package, 14- and 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.54	0.080	0.100
A_1	0.66	1.14	0.026	0.045
b	0.38	0.48	0.015	0.019
b_1	0.20	0.38	0.008	0.015
c	0.10	0.15	0.004	0.006
D-14	8.64	9.14	0.340	0.360
D-16	9.91	10.41	0.390	0.410
E-14	6.10	6.60	0.240	0.260
E-16	6.60	7.11	0.260	0.280
E_1	4.45	4.95	0.175	0.195
E_2	0.76	1.27	0.030	0.050
e	1.27 BSC		0.050 BSC	
L	7.62	8.89	0.300	0.350
S	–	1.14	–	0.045
S_1	0.13	–	0.005	–

■ LCC, 20- to 28-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A_1	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D-20	8.69	9.09	0.342	0.358
D-28	11.23	11.63	0.442	0.458
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L_1	1.96	2.36	0.077	0.093

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Package Information

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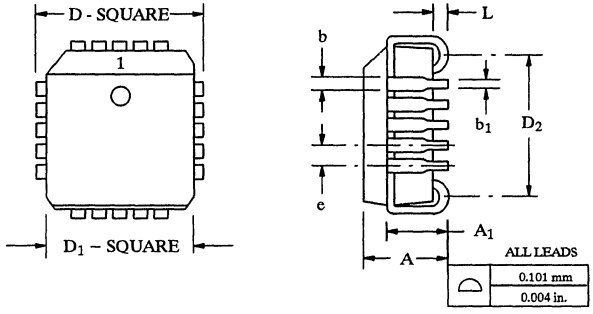
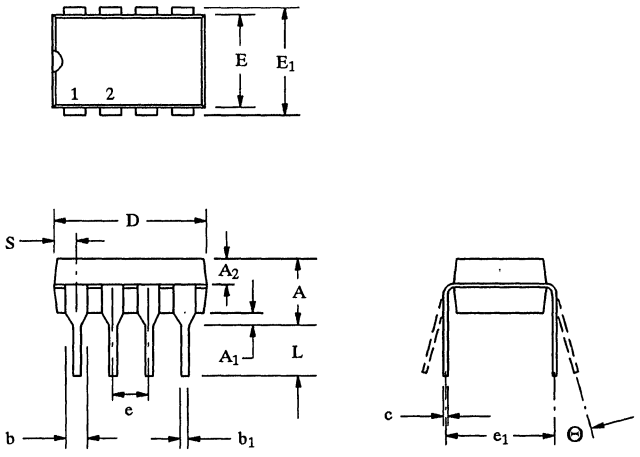
■ PLCC, 20- to 44-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.33	0.55	0.013	0.021
D-20	9.78	10.03	0.385	0.395
D-28	12.32	12.57	0.485	0.495
D-44	17.40	17.65	0.685	0.695
D_1-20	8.89	9.04	0.350	0.356
D_1-28	11.43	11.58	0.450	0.456
D_1-44	16.51	16.66	0.650	0.656
D_2-20	7.37	8.38	0.290	0.330
D_2-28	9.91	10.92	0.390	0.430
D_2-44	14.99	16.00	0.590	0.630
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

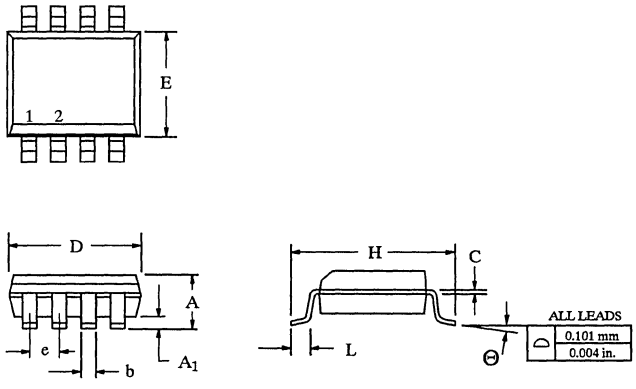
■ Plastic DIP, 8- to 20-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D–8	9.65	11.68	0.380	0.460
D–14	17.27	19.30	0.680	0.760
D–16	18.93	21.33	0.745	0.840
D–20	24.89	26.92	0.980	1.060
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S–8	1.02	2.03	0.040	0.080
S–14	1.02	2.03	0.040	0.080
S–16	0.38	1.52	0.015	0.060
S–20	1.02	2.03	0.040	0.080
Θ	0°	15°	0°	15°

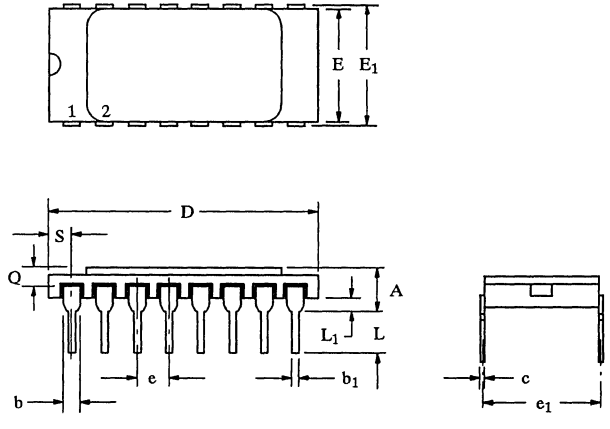
Package Information

SOIC, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

Sidebraze Ceramic, 14- to 24-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.44	0.105	0.175
b	0.97	1.52	0.038	0.060
b_1	0.38	0.53	0.015	0.021
c	0.20	0.30	0.008	0.012
D-14	17.53	19.55	0.690	0.770
D-16	19.56	21.08	0.770	0.830
D-20	24.89	26.16	0.890	1.030
D-24	29.97	31.24	1.180	1.230
E	7.12	7.87	0.280	0.310
E_1	7.37	8.25	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
L_1	0.64	1.39	0.025	0.055
Q	0.25	–	0.010	–
S-14	0.77	2.41	0.030	0.095
S-16	0.51	1.65	0.020	0.065
S-20	0.77	1.65	0.030	0.065
S-24	0.77	2.41	0.030	0.095

Package Information

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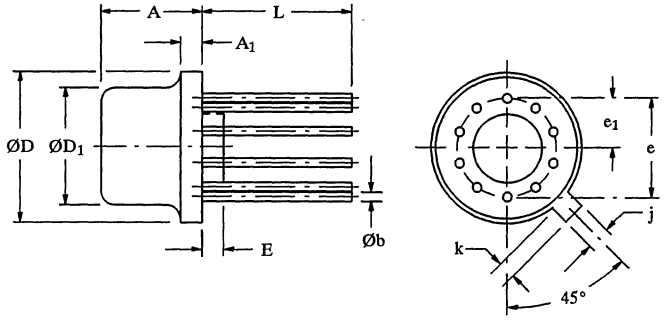
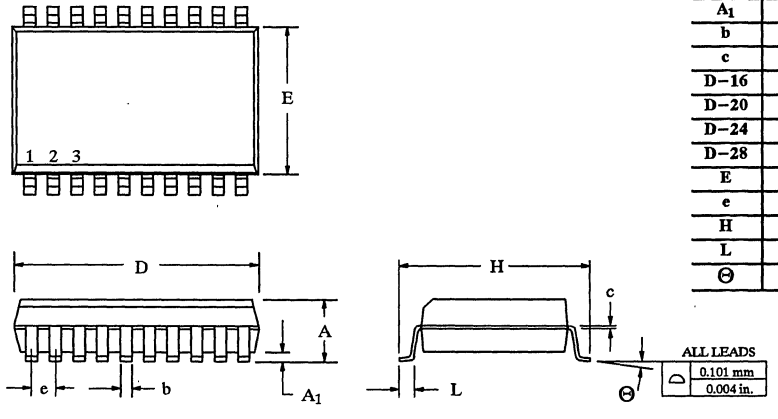
■ TO-100 Metal Can, 10-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.19	4.70	0.165	0.185
A_1	–	1.02	–	0.040
Øb	0.41	0.53	0.016	0.021
ØD	8.51	9.40	0.335	0.370
$ØD_1$	7.75	8.51	0.305	0.335
E	0.25	1.02	0.010	0.040
e	5.84 BSC		0.230 BSC	
e_1	2.92 BSC		0.115 BSC	
j	0.72	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	–	0.500	–

■ Wide-Body SOIC, 16- to 28-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.15	2.90	0.085	0.114
A_1	0.10	0.30	0.004	0.012
b	0.35	0.45	0.014	0.018
c	0.23	0.28	0.009	0.011
D–16	9.95	10.75	0.392	0.423
D–20	12.50	13.30	0.492	0.524
D–24	15.05	15.85	0.593	0.624
D–28	17.60	18.40	0.693	0.724
E	7.25	8.00	0.285	0.315
e	127 BSC		0.050 BSC	
H	9.80	10.60	0.386	0.417
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

Conversion Table

	Original "DG" Part No.	JAN Part No.	Original "DG" Part No.	JAN Part No.
DG180 Series to MIL-M-38510 This family consists of silicon, break-before-make, multi-chip analog switches with drivers.	DG181AP/883	JM38510/11101BCC	DG187AP/883	JM38510/11105BCC
	DG181AP/883	JM38510/11101BCA	DG187AP/883	JM38510/11105BCA
	DG181AA/883	JM38510/11101BIC	DG187AA/883	JM38510/11105BIC
	DG181AA/883	JM38510/11101BIA	DG187AA/883	JM38510/11105BIA
	DG181AL/883	JM38510/11101BXA	DG187AL/883	JM38510/11105BXA
	DG182AP/883	JM38510/11102BCC	DG188AP/883	JM38510/11106BCC
	DG182AP/883	JM38510/11102BCA	DG188AP/883	JM38510/11106BCA
	DG182AA/883	JM38510/11102BIC	DG188AA/883	JM38510/11106BIC
	DG182AA/883	JM38510/11102BIA	DG188AA/883	JM38510/11106BIA
	DG182AL/883	JM38510/11102BXA	DG188AL/883	JM38510/11106BXA
	DG184AP/883	JM38510/11103BEC	DG190AP/883	JM38510/11107BEC
	DG184AP/883	JM38510/11103BEA	DG190AP/883	JM38510/11107BEA
	DG184AL/883	JM38510/11103BXA	DG190AL/883	JM38510/11107BXA
	DG185AP/883	JM38510/11104BEC	DG191AP/883	JM38510/11108BEC
	DG185AP/883	JM38510/11104BEA	DG191AP/883	JM38510/11108BEA
	DG185AL/883	JM38510/11104BXA	DG191AL/883	JM38510/11108BXA
DG200 Series to MIL-M-38510 This family consists of monolithic, silicon, CMOS negative logic analog switches.	DG200AAP/883	JM38510/12301BCC		
	DG200AAK/883	JM38510/12301BCA		
	DG200AAA/883	JM38510/12301BIC		
	DG200AAA/883	JM38510/12301BIA		
	DG201AAP/883	JM38510/1202BCC		
	DG201AAK/883	JM38510/12302BEA		
DG300 Series to MIL-M-38510 This family consists of silicon, CMOS, monolithic, analog switches with drivers.	DG300AAP/883	JM38510/11601BCC	DG304AAP/883	JM38510/11605BCC
	DG300AAK/883	JM38510/11601BCA	DG304AAK/883	JM38510/11605BCA
	DG300AAA/883	JM38510/11601BIA	DG304AAA/883	JM38510/11605BIA
	DG301AAP/883	JM38510/11602BCC	DG305AAP/883	JM38510/11606BCC
	DG301AAK/883	JM38510/11602BCA	DG305AAK/883	JM38510/11606BCA
	DG301AAA/883	JM38510/11602BIA	DG305AAA/883	JM38510/11606BIA
	DG302AAP/883	JM38510/11603BCC	DG306AAP/883	JM38510/11607BCC
	DG302AAK/883	JM38510/11603BCA	DG306AAK/883	JM38510/11607BCA
	DG303AAP/883	JM38510/11604BCC	DG307AAP/883	JM38510/11608BCC
	DG303AAK/883	JM38510/11604BCA	DG307AAK/883	JM38510/11608BCA
DG506 Series to MIL-M-38510 This family consists of monolithic, silicon, CMOS/analog logic microcircuit.	DG506AAR/883	JM38510/19001BXC		
	DG507AAR/883	JM38510/19003BXC		
	DG508AAP/883	JM38510/19007BEA		
	DG508AAP/883	JM38510/19007BEC		
	DG509AAP/883	JM38510/19008BEA		
	DG509AAP/883	JM38510/19008BEC		
	Basic "DG" Part No.	**Standard Military Drawing Part No.**	**Basic "DG" Part No**	**Standard Military Drawing Part No.**
Standard Military Drawings The following analog switches and multiplexers consists of monolithic, silicon CMOS except for the DG180, DG189, and DG129 parts which are silicon, multichip with bipolar driver.	DG129AP	7801401CA	DG409AK	5962–9204202MEA
	DG180AL	8767301AA	DG409AZ	5962–9204202M2A
	DG180AP	8767301CA	DG411AZ	5962–9073101M2A
	DG180AA	8767301IA	DG411AK	5962–9073101MEA
	DG189AP	5962–9068901MEA	DG412AZ	5962–9073102M2A
	DG201AAZ	77053012A	DG412AK	5962–9073102MEA
	DG201AAK	7705301EA	DG413AZ	5962–9073103M2A
	DG201AAP	7705301EC	DG413AK	5962–9073103MEA
	DG201AAL	7705301FA	DG441AK	5962–9204101MEA
	DG201AAL	7705301FC	DG441AZ	5962–9204101M2A
	DG271AZ	5962–86716022A	DG442AK	5962–9204102MEA
	DG271AK	5692–8976301EA	DG442AZ	5962–9204102M2A
	DG401AZ	5962–90569012A	DG508AAP	7705201EA
	DG401AK	5962–9056901EA	DG508AAP	7705201EC
	DG403AK	5692–8976301EA	DG508AAL	7705201FA
	DG405AZ	5962–89961012A	DG528AK	5692–8768901VA
	DG405AK	5962–8996101EA	DG542AP	5962-9155201MEA
	DG408AK	5962–9204201MEA		
	DG408AZ	5962–9204201M2A		

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Process Option Flows

Test and Condition		U.S. Build Only if Specified[a]	U.S. Build or QML Offshore Build	Parts Marked /883 or SMD, as Applicable[c]	
Description	Method Per MIL-STD-883	Space Rated Extended Hi-Rel[b]	Class B S/S JAN Devices	SMD and /883 Compliant Non-JAN Method 5004/5005	Ruggedized Plastic -4 Flow
Traceability to W/L		X	X	X	N/A
SEM		X	N/A	N/A	N/A
Internal Visual	2010	Condition A	Condition B	Condition B	Condition B
Die Shear	2019	X	N/A	N/A	N/A
Bond Strength Cert/Data	2011	X	N/A	N/A	N/A
Stab Bake	1008-C	X	X	X	X
Temp Cycle	1010-C	X	X	X	X
Centrifuge	2001-E	X	X	X	N/A
PIND	2020-A	X	N/A	N/A	N/A
Fine Leak	1014-A or -B	X	X	X	N/A
Gross Leak	1014-C	X	X	X	N/A
1st Electrical	per spec	X	X	X	X
Burn-In	1015-A or -C	72 hrs -A	160 hrs per S/S	160 hrs -A or -C	160 hrs. -A or -C
Interim Electrical Post Burn-In		per spec[d]	Static 25°C PDA per S/S	Static 25°C PDA = 5%	Static 25°C PDA = 5%
Burn-In	1015-A or -C	240 hrs Dyn. (Min.)	per S/S	N/A	N/A
Interim Electrical Post Burn-In	Static[e]	Static 25°C PDA = 5%	N/A	N/A	N/A
	Functional[e]	Functional 25°C PDA = 3% (datalog)	per S/S	N/A	N/A
Final Electrical	Min. Temp.	X	X	X	X
	Max. Temp.	X	X	X	X
Fine Leak	1014-A or -B	X	N/A	N/A	N/A
Gross Leak	1014-C	X	N/A	N/A	N/A
X-Ray	2012	X	N/A	N/A	N/A
QCI A	5005	per spec[d]	X	X	−55, 25, 125°C
QCI B	5005	X	X	X	N/A
QCI C	5005	N/A	X	X	N/A
QCI D	5005	X	X	X	N/A
External Visual	2009	X	X	X	X
Deltas Option		Option	X	N/A	N/A
Solder Dip Option		Option	Option	Option	N/A

Notes:
a. On U. S. builds, unless otherwise specified by 38510 or drawing, parts may be assembled offshore.
b. Space Rated Extended Hi-Rel process option available under customer SCD only.
c. Parts not qualified for /883 or SMD must not be marked as such. A special flow for non-compliant, non-JAN product can be generated as custom. Contact marketing for details.
d. Per spec is a reference to customer SCD.
e. PDA applies to both burn-ins.

Process Option Flows for Chip/Wafer

Standard Die/Chip with Element Evaluation	Standard Die/Chip	Standard Die/Wafer Form
Die ship element evaluation non-compliant/ non-JAN subgroup 1 and 3 performed in-line	Die ship No canned sample	Die Wafer form
Wafer probe Static 25°C (min) per device spec Internal visual Method 2010 cond. B	Wafer probe Static 25°C (min) per device spec Internal visual Method 2010 cond. B	Wafer probe Static 25°C (min) per device spec Internal visual Method 2010 cond. B
Canned sample:* Method 2008 MIL STD 883 Class B device Subgroup 1 (ss−10/0) Internal visual Method 2010 cond. B Subgroup 2 (ss−10/1) Final electrical Static @25°C min/max oper. temp. (per device spec) Subgroup 3 (5 Die min) (s/s = 10/0 or 20/1 wires) Non-Destructive Test Method 2023 wire bond eval. Method 2011 (cert and data) *SEM available	Die prep process	

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Cross Reference

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Siliconix Part Number (Direct Replacement) Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, the specifications should be carefully compared.

Siliconix Approximate Replacement Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeablity is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, the specifications should be carefully compared. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

Industry Part Number	Siliconix Part Number	Approximate Replacement	Page
8100609EA		5962-9056901EA	1-127
8100610EA		5962-9056901EA	1-127
8100611EA		5962-8996101EA	1-127
8100612EA		5962-8976301EA	1-127
8100613EA		5962-8976301EA	1-127
8100614EA		5962-8976301EA	1-127
AD200DIAA	DG200AAA		1-32
AD200DIAP		DG200AAK	1-32
AD200DIBA	DG200ABA		1-32
AD200DICJ		DG200ACJ	1-32
AD200DIPB		DG200ABK	1-32
AD201DIAP		DG411AK	1-137
AD201DIBP		DG411AK	1-137
AD201DICJ		DG411DJ	1-137
AD302DIAP	DG302AAK		1-90
AD302DIBP	DG302AAK		1-90
AD302DICJ	DG302ACJ		1-90
AD303DIAP	DG303AAK		1-90
AD303DIBP	DG303AAK		1-90
AD303DICJ	DG303ACJ		1-90
AD7506DK		DG506ABK	2-52
AD7506JN	DG506ACJ		2-52
AD7506JQ	DG506ACK		2-52
AD7506KN	DG506ACJ		2-52
AD7506KQ	DG506ABK		2-52
AD7506SD		DG506AAK	2-52
AD7506SQ	DG506AAK		2-52
AD7506TE	DG506AAZ/883		2-52
AD7506TQ	DG506AAK		2-52
AD7507JN	DG507ACJ		2-52
AD7507JQ	DG507ABK		2-52
AD7507KN	DG507ACJ		2-52
AD7507KQ	DG507ABK		2-52
AD7507SQ	DG507AAK		2-52
AD7507TE	DG507AAZ/883		2-52
AD7507TQ	DG507AAK		2-52
AD7509KD		DG509ABK	2-60
AD7509KN		DG509ACJ	2-60
AD7509SD		DG509AAK	2-60
ADG200AA		DG200AAA	1-32
ADG200AA/883		DG200AAA/883	1-32
ADG200AP		DG200AAK	1-32
ADG200AP/883		DG200AAK/883	1-32
ADG200BA		DG200ABA	1-32
ADG200BP		DG200ABK	1-32
ADG200CJ		DG200ACJ	1-32
ADG201ABQ	DG441AK		1-163
	DG201ABK		1-37
ADG201AKN	DG441DJ		1-163
	DG201ACJ		1-37
ADG201AKR	DG441DY		1-163
	DG201ADY		1-37
ADG201ATE	5962-9204101M2A		1-163
	DG201AAZ/883		1-37
ADG201ATE/883B	5962-9204101M2A		1-163
	DG201AAZ/883		1-37
ADG201ATQ	DG441AK		1-163
	DG201AAK		1-37
ADG201ATQ/883	DG441AK/883		1-163
	DG201AAK/883		1-37
ADG201CJ	DG441DJ		1-163
	DG201ACJ		1-37
ADG201HSAQ	DG201HSAK883		1-52
	DG271AK		1-85
ADG201HSBQ		DG201HSAK883	1-52
		DG271AK	1-85
ADG201HSJN	DG201HSDJ		1-52
	DG271CJ		1-85
ADG201HSKN	DG201HSDJ	DG271CJ	1-52
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TEL: (914) 997-1265
FAX: (914) 997-1277

Asheville, NC (28801)
TEMIC
46 Haywood Street, Ste. 337
TEL: (704) 252-9827
FAX: (704) 252-5083

WESTERN

Santa Clara, CA (95056)
TEMIC c/o Siliconix Inc.
2201 Laurelwood Road
P.O. Box 54951
TEL: (408) 970-5700
FAX: (408) 970-3950

Irvine, CA (92619-1084)
TEMIC
P.O. Box 51084
TEL: (714) 552-4080
FAX: (714) 552-4181

Houston (77027)
TEMIC
2100 West Loop South, Ste. 800
TEL: (713) 297-8871
FAX: (713) 297-8872

U.S. Sales Representatives

ALABAMA

Huntsville (35803)
Rep, Inc.
11535 Gilleland Road
TEL: (205) 881-9270
FAX: (205) 882-6692

ALASKA

See Washington

ARIZONA

Tempe (85283)
Quadrep Southern
40 W. Baseline Road, Ste. 112
TEL: (602) 839-2102
FAX: (602) 839-2126

ARKANSAS

See Texas (Arlington)

CALIFORNIA (Southern)

San Diego (92130)
Quadrep Southern, Inc.
11995 El Camino Real, Ste. 305
TEL: (619) 755-1188
FAX: (619) 793-9269

Irvine (92718)
Quadrep Southern, Inc.
15215 Alton Parkway, Ste. 200
TEL: (714) 727-4222
FAX: (714) 727-4033

CALIFORNIA (Northern)

San Jose (95134)
Quadrep, Inc.
2635 N. First Street, Ste. 116
TEL: (408) 432-3300
FAX: (408) 432-3428

COLORADO

Littleton (80122)
Quadrep, Inc.
7891 S. Garfield Way
TEL: (303) 771-6886
FAX: (303) 771-6887

CONNECTICUT

Wallingford (06492)
Technology Sales, Inc.
237 Hall Avenue
TEL: (203) 269-8853
FAX: (203) 269-2099

DELAWARE

See New Jersey (Southern)

DISTRICT OF COLUMBIA

See Maryland

FLORIDA

Deerfield Beach (33441)
MEC
400 Fairway Drive Ste. 107
TEL: (305) 426-8944
FAX: (305) 570-8568

Largo (34643)
MEC
10637 Harborside Drive North
TEL: (813) 393-5011
FAX: (813) 393-5202

Winter Park (32789)
MEC
1305 Raintree Place
TEL: (407) 740-0023
FAX: (407) 740-0083

GEORGIA

Tucker (30084)
Rep, Inc.
1944 Northlake Parkway
TEL: (404) 938-4358
FAX: (404) 938-0194

HAWAII

See California (Northern)

IDAHO

Boise (83702)
Q.R. Crown
1524 W. Hays
TEL: (208) 344-9588
FAX: (208) 344-9550

ILLINOIS

Hoffman Estates (60195)
Victory Sales
1030 W. Higgins Road, Ste. 101
TEL: (708) 490-0300
FAX: (708) 490-1499

INDIANA

Indianapolis (46250)
Victory Sales
8041 Knue Road
TEL: (317) 577-4786
FAX: (317) 577-4789

IOWA

Cedar Rapids (52402)
Stan Clothier Company
1930 Street Andrews NE
TEL: (319) 393-1576
FAX: (319) 393-7317

KANSAS

Lenexa (66215)
Stan Clothier Co.
13000 W. 87th Street Parkway, Ste. 105
TEL: (913) 492-2124
FAX: (913) 492-1855

KENTUCKY

See Indiana

LOUISIANA

See Arlington, Texas

MAINE

See Massachusetts

MARYLAND

Towson (21204)
Arbotek Associates, Inc.
102 W. Joppa Road
TEL: (410) 825-0775
FAX: (410) 337-2781

MASSACHUSETTS

Waltham (02154)
Technology Sales, Inc.
332 Second Avenue
TEL: (617) 890-5700
FAX: (617) 890-3913

MICHIGAN

See TEMIC Sales Offices, Troy, MI

MINNESOTA

Eden Prairie (55344)
Stan Clothier
9600 W. 76th Street, Ste. A
TEL: (612) 944-3456
FAX: (612) 944-6904

MISSISSIPPI

See Alabama

MISSOURI

Saint Charles (63303)
Stan Clothier Company
3910 Old Highway 94, South, Ste. 116
TEL: (314) 928-8078
FAX: (314) 447-5214

MONTANA

See Washington

NEBRASKA

See Missouri

NEVADA (Except Clark County)

See Califronia (Northern)

NEVADA (Clark County)

See Arizona

NEW HAMPSHIRE

See Massachusetts

NEW JERSEY

See New York (Metro/L.I.)

NEW MEXICO

See Arizona

U.S. Sales Representatives (Cont'd)

NEW YORK (Upstate)

Fairport (14450)
Technology Sales, Inc
920 Perinton Hills Office Park
TEL: (716) 223-7500
FAX: (716) 223-5526

NEW YORK (Metro/L.I.)

Babylon (11702)
Astrorep Incorporated
103 Cooper Street
TEL: (516) 422-2500
FAX: (516) 422-2504

NORTH CAROLINA

Morrisville (27560)
Rep. Inc.
2500 Gateway Centre Blvd., Ste. 400
TEL: (919) 469-9997
FAX: (919) 481-3879

NORTH DAKOTA

See Minnesota

OHIO

See Indiana

OKLAHOMA

See Texas (Arlington)

OREGON

Portland (97224)
Q.R. Crown , Inc.
17020 SW. Upper Boones Ferry Road,
Ste. 202
TEL: (503) 620-8320
FAX: (503) 639-4023

PENNSYLVANIA (Western)

See Indiana

PENNSYLVANIA (Eastern)

See New York (Metro/L.I.)

PUERTO RICO

San German (00683-0121)
Technology Sales, Inc.
PO Box 122, Edificio Rali, Ste. 216
TEL: (809) 892-4745
FAX: (809) 892-1128

RHODE ISLAND

See Massachusetts

SOUTH CAROLINA

See Tennessee

SOUTH DAKOTA

See Minnesota

TENNESSEE

Jefferson City (37760)
Rep. Inc.
P. O. Box 490
1908 Branner Avenue
TEL: (615) 475-9012/9013
FAX: (615) 475-6340

TEXAS

Arlington (76006)
Ion Associates, Inc.
2221 E. Lamar, Ste. 250
TEL: (817) 695–8000
FAX: (817) 695-8010

Austin (78759)
Ion Associates, Inc.
4412 Spicewood Springs Road, Ste. 202
TEL: (512) 794-9006
FAX: (512) 794-9008

Houston (77014)
Ion Associates, Inc.
14347-A Torrey Chase Blvd.
TEL: (713) 537-7717
FAX: (713) 537-5612

UTAH

See Colorado

VERMONT

See Massachusetts

VIRGINIA

See Maryland

WASHINGTON

Bellevue (98005)
Q.R. Crown, Inc.
375 118th Ave., S.E., Ste. 110
TEL: (206) 453-5100
FAX: (206) 646-8775

WEST VIRGINIA

See Maryland

WISCONSIN

Brookfield (53005)
Victory Sales
405 N. Calhoun Road, Ste. 208
TEL: (414) 789-5770
FAX: (414) 789-5760

WYOMING

See Colorado

Canadian Sales Representatives

Brampton, Ontario (L6T 1K2)
Electronics Sales Professionals (ESP) Inc.
27 Anne Court
TEL: (416) 458-1103
FAX: (416) 458-4469

British Columbia
See Washington

Montreal, Quebec (H2B 1Z2)
Electronics Sales Professionals (ESP) Inc.
2102 Place Etienne-Brule
TEL: (514) 388-6596
FAX: (514) 388-8402

North Gower, Ontario (K0A 2T0)
Electronics Sales Professionals (ESP) Inc.
5936 Third Line Road North RR #3
TEL: (613) 489-3379
FAX: (613) 489-2778

Scarborough, Ontario (M1V 3P6)
Electronics Sales Professionals (ESP) Inc.
60 Wilderness Drive
TEL: (416) 321-9693
FAX: (416) 321-9794

Chip Distributor

FLORIDA

Orlando (32810)
Chip Supply, Inc.
7725 N. Orange Blossom Trail
TEL: (407) 298-7100
TWX: (810) 850-0103
FAX: (407) 290-0164

U. S. Distributors

ALABAMA

Huntsville (35816)
Future Electronics Corp.
4825 University Square, Ste. 12
TEL: (205) 830-2322
FAX: (205) 830-6664

Huntsville (35801)
Marshall Industries
3313 Memorial Parkway South, Ste. 150
TEL: (205) 881-9235
FAX: (205) 881-1490

Huntsville (35816)
Pioneer Tech.
4835 University Square, Ste. 5
TEL: (205) 837-9300
FAX: (205) 837-9358

ARIZONA

Phoenix (85034)
Future Electronics Corp.
4636 E. University Drive, Ste. 245
TEL: (602) 968-7140
FAX: (602) 968-0334

Phoenix (85044)
Marshall Industries
9830 S. 51st Street, Ste. B121
TEL: (602) 496-0290
FAX: (602) 893-9029

Phoenix (85040)
Wyle Laboratories-EMG
4141 E. Raymond Street, Ste. 1
TEL: (602) 437-2088
FAX: (602) 437-2124

Tempe (85281)
Bell Industries
140 S. Lindon Lane #102
TEL: (602) 966-3600
(800) 525-6666
FAX: (602) 967-6584

Tempe (85281)
Hamilton/Hallmark
1626 S. Edward Drive
(800) 332-8638
FAX: (800) 257-0568

CALIFORNIA

Agoura Hills (91301)
Bell Industries
30101 Agoura Court, Ste. 118
TEL: (818) 865-7900
(800) 525-6666
FAX: (818) 991-7695

Agoura Hills (91301)
Pioneer Std.
5126 Clareton Drive, Ste. 160
TEL: (818) 865-5800
FAX: (818) 865-5814

Calabasas (91302-1959)
Marshall Industries
26637 Agoura Road
TEL: (818) 878-7000
FAX: (818) 880-6846

Calabasas (91302)
Wyle Laboratories
26010 Mureau Road, Ste. 150
TEL: (818) 880-9000
FAX: (818) 880-5510

Chatsworth (91311)
Future Electronics Corp.
9301 Oakdale Ave., Ste. 210
TEL: (818) 772-6240
FAX: (818) 772-6247

Costa Mesa (92626)
Hamilton/Hallmark – #29
3170 Pullman Street
TEL: (714) 641-4100
FAX: (714) 641-4122

Culver City (90230)
Hamilton Corporate
10950 W. Washington Blvd.
TEL: (310) 558-2000
FAX: (310) 558-2076

El Monte (91731)
Marshall Corporate
9320 Telstar Avenue
TEL: (818) 307-6000
FAX: (818) 307-6297

Irvine (92718)
Bell Industries
220 Technology Drive, Ste. 100
TEL: (714) 727-4500
(800) 525-6666
FAX: (714) 453-4610

Irvine (92714)
Future Electronics Corp.
1692 Browning Ave.
TEL: (714) 250-4141
FAX: (714) 250-4185

Irvine (92718)
Marshall Industries
1 Morgan
TEL: (714) 859-5050
FAX: (714) 581-5255

Irvine (92718)
Pioneer Std.
217 Technology Drive, Ste. 110
TEL: (714) 753-5090
FAX: (714) 753-5074

Irvine (92714)
Wyle Laboratories-EMG
17872 Cowan Avenue
TEL: (714) 863-9953
TWX: (910) 595-1572
FAX: (714) 863-0473

Los Angeles (90049)
Bell Industries
11812 San Vincente Blvd., Ste. 300
TEL: (310) 826-2355
(800) 525-6666
FAX: (310) 826-1534

Milpitas (95035)
Marshall Industries
336 Los Coches Street
TEL: (408) 942-4600
FAX: (408) 262-1224

Rancho Cordova (95670)
Marshall Industries
3039 Kilgore Ave. Ste. 140
TEL: (916) 635-9700
FAX: (916) 635-6044

Rancho Cordova (95742)
Wyle Distribution Group
Sacramento Division
2951 Sunrise Blvd., Ste. 175
TEL: (916) 638-5282
FAX: (916) 638-1491

Reseda (91335)
JAN Devices
6925 Canby, Bldg. 109
TEL: (818) 708-1100
FAX: (818) 708-7436

Rocklin (95677)
Bell Industries
4311 Anthony Ct , Ste. 100
TEL: (916) 652-0418
(800) 525-6666
FAX: (916) 652-0403

Rocklin (95765)
Hamilton/Hallmark – #35
580 Menlo Drive, Ste. 2
TEL: (916) 624-9781
FAX: (916) 961-0922

San Diego (92123)
Bell Industries
5520 Ruffin Road, Ste. 209
TEL: (619) 576-3924
(800) 525-6666
FAX: (619) 492-9826

San Diego (92122)
Future Electronics Corp.
5151 Shoreham Place, Ste. 220
TEL: (619) 625-2800
FAX: (619) 625-2810

San Diego (92123)
Hamilton/Hallmark – #02
4545 Viewridge Avenue
TEL: (619) 571-7540
FAX: (619) 277-6136

San Diego (92123)
Marshall Industries
5961 Kearny Villa Road
TEL: (619) 627-4140
FAX: (619) 627-4163

San Diego (92123)
Wyle Laboratories-EMG
9525 Chesapeake Drive
TEL: (619) 565-9171
FAX: (619) 565-6512

San Jose (95131)
Hamilton/Hallmark – #03
2105 Lundy Avenue
TEL: (408) 435-3500
FAX: (408) 435-3720

San Jose (95131-1326)
Future Electronics Corp.
2220 O'Toole Avenue
TEL: (408) 434-1122
FAX: (408) 433-0822

San Jose (95134)
Pioneer Tech.
134 Rio Robles
TEL: (408) 954-9100
FAX: (408) 954-9113

San Jose (95119)
Zeus Electronics
6276 San Ignacio Ave., Ste. E
TEL: (408) 629-4789
FAX: (408) 629-4792

Santa Clara (95052)
Wyle Distribution Group
3000 Bowers Avenue
TEL: (408) 727-2500
TWX: (910) 379-6480
FAX: (408) 727-5896

Sunnyvale (94089)
Bell Industries
1161 No. Fairoaks Avenue
TEL: (408) 734-8570
(800) 525-6666
FAX: (408) 734-8875

Woodland Hills (91367)
Hamilton /Avnet – #48
21150 Califa Street
TEL: (818) 594-0404
FAX: (818) 594-8234

Yorba Linda (92686)
Zeus Electronics
22700 Savi Ranch Pkwy.
TEL: (714) 921-9000
FAX: (714) 921-2715

COLORADO

Lakewood (80215)
Future Electronics Corp.
12600 W. Colfax Avenue, Ste. B110
TEL: (303) 232-2008
(800) 950-3532
FAX: (303) 232-2009

Denver (80222)
Bell Industries
1873 S. Bellaire Street, Ste. 100
TEL: (303) 691-9270
(800) 525-6666
FAX: (303) 691-9036

Englewood (80111)
Hamilton/Hallmark – #06
12503 E. Euclid Drive, Ste. 20
TEL: (303) 799-7800
FAX: (303) 790-4991

Thornton (80241)
Marshall Industries
12351 N. Grant Street, Ste A
TEL: (303) 451-8444
FAX: (303) 457-2899

Thornton (80241)
Wyle Distribution Group
451 E. 124th Avenue
TEL: (303) 457-9953
FAX: (303) 457-4831

CONNECTICUT

Cheshire (06410)
Future Electronics Corp.
Westgate Office Center
700 West Johnson Ave.
TEL: (203) 250-0083
FAX: (203) 250-0081

Cheshire (06410)
Hamilton/Hallmark – #21
125 Commerce Court, Unit 6
TEL: (203) 797-2800
FAX: (203) 272-1704

Shelton (06484)
Pioneer Std.
2 Trap Falls Road
TEL: (203) 929-5600
FAX: (203) 929-9791

Meriden (06413)
Bell Industries
1064 E. Main Street
TEL: (203) 639-6000
(800) 525-6666
FAX: (203) 639-6005

Wallingford (06492)
Marshall Industries
20 Sterling Drive
Barnes Industrial Park
TEL: (203) 265-3822
FAX: (203) 284-9285

FLORIDA

Altamonte Springs (32701)
Bell Industries
650 S. North Lake Blvd., Ste. 400
TEL: (407) 339-0078
(800) 525-6666
FAX: (407) 339-0139

Altamonte Springs (32701)
Future Electronics Corp.
650 S. Northlake Blvd.
TEL: (407) 767-8414
FAX: (407) 834-9318

Altamonte Springs (32701)
Marshall Industries
380 S. Northlake Blvd., Ste. 1024
TEL: (407) 767-8585
FAX: (407) 767-8676

Altamonte Springs (32701)
Pioneer Tech.
337 South Northlake Blvd. #1000
TEL: (407) 834-9090
FAX: (407) 834-0865

Deerfield Beach (33442)
Pioneer Tech.
674 S. Military Trail
TEL: (305) 428-8877
FAX: (305) 481-2950

Fort Lauderdale (33309)
Hamilton/Hallmark, – #17
3350 N.W. 53rd Street, Ste. 105
TEL: (305) 484-5016
FAX: (305) 484-4740

Fort Lauderdale (33309)
Marshall Industries
2700 W. Cypress Creek Road, Ste. D114
TEL: (305) 977-4880
FAX: (305) 977-4887

Lake Mary (32746)
Zeus Electronics
37 Skyline Drive, Bldg. D, Ste. 3101
TEL: (407) 333-3055
FAX: (407) 333-9681

Largo (34641)
Future Electronics
2200 Tall Pines Drive, Ste. 108
TEL: (813) 530-1222
FAX: (813) 538-9598

U. S. Distributors (Cont'd)

GEORGIA

Duluth (30136)
Hamilton/Hallmark – #15
3425 Corporate Way
TEL: (404) 447-7500
FAX: (404) 625–5490

Duluth (30136)
Pioneer Tech
4250C Rivergreen Parkway
TEL: (404) 623-1003
FAX: (404) 623-0665

Norcross (30071)
Bell Industries
3000 Business Park Drive #D
TEL: (404) 446-7167
(800) 525-6666
FAX: (404) 446-7264

Norcross (30071)
Future Electronics Corp.
4960 Peachtree Ind., Blvd., Ste. 230
TEL: (404) 441-7676
FAX: (404) 441-7580

Norcross (30093)
Marshall Industries
5300 Oakbrook Pkwy., Ste. 140
TEL: (404) 923-5750
FAX: (404) 923-2743

ILLINOIS

Addison (60101)
Pioneer Std.
2171 Executive Drive, Ste. 200
TEL: (708) 495-9680
FAX: (708) 495-9831

Bensenville (60106)
Hamilton/Hallmark – #10
1130 Thorndale Avenue
TEL: (708) 860-7780
FAX: (708) 773-7969

Elk Grove Village (60007)
Bell Industries
870 Cambridge Drive
TEL: (708) 640-1910
(800) 525-6666
FAX: (708) 640-1928

Hoffman Estates (60195)
Future Electronics Corp.
3150 W. Higgins Road, Ste. 160
TEL: (708) 882-1255
WATS: (800) 933-9841
FAX: (708) 490-9290

Schaumburg (60173)
Marshall Industries
50 E. Commerce Drive, Unit I
TEL: (708) 490-0755
FAX: (708) 490-0569

INDIANA

Fort Wayne (46803)
Bell Industries
3433 E. Washnigton Blvd.
TEL: (219) 422-4300
(800) 525-6666
FAX: (219) 423-3420

Indianapolis (46268)
Bell Industries
P.O. Box 6885
5230 W. 79th Street
TEL: (317) 875-8200
(800) 525-6666
FAX: (317) 875-8219

Indianapolis (46268)
Hamilton/Hallmark – #28
4275 W. 96th Street
TEL: (317) 872-8875
FAX: (317) 876-7165

Indianapolis (46240)
Pioneer Std.
9350 N. Priority Way West Drive
TEL: (317) 573-0880
WATS: (800) 332-5503 (IN)
WATS: (800) 428-9128 (IL, KY)
FAX: (317) 573-0979

IOWA

Cedar Rapids (52402)
Hamilton/Hallmark – #44
2335-A Blairsferry N.E.
TEL: (319) 393-0033
WATS: (800) 332-4757
FAX: (319) 393-7050

KANSAS

Lenexa (66219)
Hamilton/Hallmark – #58
15313 W. 95th
TEL: (913) 888-1055
FAX: (913) 541-7951

Lenexa (66214)
Marshall Industries
10413 W. 84th Terrace
TEL: (913) 492-3121
FAX: (913) 492-6205

Overland Park (66212)
Future Electronics Corp.
8826 Santa Fe Drive, Ste. 150
TEL: (913) 649-1531
FAX: (913) 649-1786

KENTUCKY

Lexington (40511-1001)
Hamilton/Hallmark
1847 Mercer Road, Ste. G
TEL: (606) 259-1475
FAX: (606) 288-4936

MARYLAND

Columbia (21046)
Bell Industries
8945 Guilford Road, Ste. 130
TEL: (410) 290-5100
(800) 525-6666
FAX: (410) 290-8006

Columbia (21046)
Future Electronics Corp.
6716 Alexander Bell Drive, Ste. 101
TEL: (41) 290-0600
FAX: (410) 290-0328

Columbia (21046-2101)
Hamilton/Hallmark – #12
10240 Old Columbia Road
TEL: (410) 988-9800
FAX: (410) 381-2036

Gaithersburg (20877)
Pioneer Tech.
9100 Gaither Road
TEL: (301) 921-0660
FAX: (301) 921-4255

Silver Springs (20904)
Marshall Industries
2221 Broad Birch Drive, Ste. G
TEL: (301) 622-1118
FAX: (301) 622-0451

MASSACHUSETTS

Andover (01810)
Bell Industries
100 Burtt Road, Suite 106
TEL: (508) 474–8880
(800) 525-6666
FAX: (508) 474–8902

Bolton (01740)
Future Electronics Corp.
41 Main Street
TEL: (508) 779–3000
FAX: (508) 779–5143

Burlington (01803)
Wyle
15 Third Ave.
TEL: (617) 272–7300
FAX: (617) 272-6809

Lexington (02173)
Pioneer Std.
44 Hartwell Ave.
TEL: (617) 861-9200
FAX: (617) 863-1547

Peabody (01960)
Hamilton/Hallmark – #18
10 M Centennial Drive
TEL: (508) 532-3701
FAX: (508) 532-9802

Wilmington (01877)
Zeus Electronics
25 Upton Drive
TEL: (508) 658-4776
FAX: (508) 694-2199

Wilmington (01887)
Marshall Industries
33 Upton Drive
TEL: (508) 658-0810
FAX: (508) 657-5931

MICHIGAN

Grand Rapids (49512)
Future Electronics Corp.
4505 Broadmoor SE
TEL: (616) 698-6800
WATS: (800) 334-6808
FAX: (616) 698-6821

Grand Rapids (49512)
Pioneer Std.
4594 Broadmoor Ave. SE, Ste. 235
TEL: (616) 698-1801
FAX: (616) 698-1831

Livonia (48150)
Future Electronics Corp.
35200 Schoolcraft Road, Ste. 106
TEL: (313) 261-5270
FAX: (313) 261-8175

Livonia (48150)
Marshall Industries
31067 Schoolcraft Road
TEL: (313) 525-5850
FAX: (313) 525-5855

Plymouth (48270)
Pioneer Std.
44190 Plymouth Oaks Drive
TEL: (313) 416-2157
FAX: (313) 416-2415

Novi (40375)
Hamilton/Hallmark – #66
41650 Gardenbrook, Ste. 100
TEL: (313) 347-4271
FAX: (313) 347-4021

MINNESOTA

Bloomington (55341)
Hamilton/Hallmark – #63
9401 James Avenue South, Ste. 140
TEL: (612) 881-2600
FAX: (612) 881-9461

Eden Prairie (55344)
Future Electronics Corp.
10025 Valley View Road, Ste. 196
TEL: (612) 944-2200
FAX: (612) 944-2520

Eden Prairie (55344)
Pioneer Std.
7625 Golden Triangle Drive
TEL: (612) 944-3355
FAX: (612) 944-3794

Plymouth (55447)
Marshall Industries
3955 Annapolis Lane
TEL: (612) 559-2211
FAX: (612) 559-8321

MISSOURI

Earth City (63045)
Hamilton/Hallmark – #05
3783 Rider Trail South
TEL: (314) 291-5350
FAX: (314) 291-0362

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12125 Woodcrest Executive Drive,
Ste. 220
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WATS: (800) 727-6805
FAX: (314) 469-7226

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Fairfield (07004)
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271 Route 46 West, Ste. F202-203
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(800) 525-6666
FAX: (201) 227-2626

Fairfield (07006)
Marshall Industries
101 Fairfield Road
TEL: (201) 882-0320
FAX: (201) 882-0095

Fairfield (07006)
Pioneer Std.
14 "A" Madison Road
TEL: (201) 575-3510
FAX: (201) 575-3454

Marlton (08053)
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12 E. Stow Road, Ste. 200, Bldg. 12
TEL: (609) 596–4080
FAX: (609) 596-4266

Mt. Laurel (08054)
Marshall Industries
158 Gaither Drive, Unit 100
TEL: (609) 234-9100 (NJ)
TEL: (215) 627-1920 (PA)
FAX: (609) 778-1819

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Albuquerque (87123)
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11728 Linn N.E.
TEL: (505) 292-2700
(800) 525-6666
FAX: (505) 275-2819

Albuquerque (87109-3147)
Hamilton/Hallmark – #22
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TWX: (910) 989-0614
FAX: (505) 828-0360

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FAX: (607) 722-9562

Endicott (13760)
Marshall Industries
100 Marshall Drive
TEL: (607) 798-1611
FAX: (607) 797-7031

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840 Fairport Park
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FAX: (716) 381-5955

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FAX: (516) 234-6183

Hauppauge (11788)
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933 Motor Parkway
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FAX: (516) 434-7491

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Zeus Electronics
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FAX: (914) 937-2553

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333 Metro Park
TEL: (716) 272-1120
FAX: (716) 272-7182

Rochester (14623)
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1057 E. Henrietta Road
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FAX: (716) 475-9119

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FAX. (315) 451-7258

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FAX: (516) 921-2143

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FAX· (919) 460-1540

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5225 Capitol
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FAX: (919) 790-9022

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3510 Spring Forrest Road
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FAX: (919) 954-0940

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Marshall Industries
5224 Greens Dairy Road
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FAX: (919) 872-2431

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FAX: (216) 587-3906

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FAX: (513) 439-6705

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FAX: (513) 898-9835

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4433 Interpoint Blvd.
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FAX: (216) 449-8987

Solon (44139)
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Tulsa (74146)
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Cornell Oaks Corp. Center
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FAX: (503) 645-1559

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FAX: (503) 646-8256

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Wyle Laboratories-EMG
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TEL: (503) 643-7900
FAX: (503) 646-5466

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Pittsburgh (15238)
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Bell Industries
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(800) 678-0991
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Hamilton/Hallmark – #26
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FAX· (512) 258-3777

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FAX· (512) 835-9829

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FAX: (713) 467-9805

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FAX: (713) 495-5642

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FAX· (214) 644-5064

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FAX: (214) 447-2222

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(800) 525-6666
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FAX: (801) 226-0210

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FAX: (801) 263-0104

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Marshall Industries
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FAX. (801) 972-2524

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(800) 525-6666
FAX: (206) 646-8559

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FAX: (206) 644-7300

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FAX: (206) 489-3411

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Marshall Industries
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FAX: (206) 486-6964

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FAX: (206) 867-0159

Redmond (98052)
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FAX: (414) 771-2847

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FAX: (414) 780-7201

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(800) 525-6666
FAX: (414) 547-6547

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FAX: (414) 797-8270

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Future Electronics Corp.
4606 97th Street
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FAX: (403) 434-0812

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FAX: (604) 294-1206

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1695 Boundary Road
TEL: (604) 294-1166
FAX: (604) 294-1206

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106 King Edward Court
TEL: (204) 786-7711
FAX: (204) 783-8133

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FAX: (416) 458-1613

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FAX: (416) 612-9185

Mississauga (L5T 2L1)
Hamilton/Hallmark – #59
151 Superior Blvd.
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FAX: (416) 564-6033

Ottawa (K2C 3P2)
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Baxter Centre
1050 Baxter Road
TEL: (613) 820-8313
FAX: (613) 820-3271

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Pointe Claire (H9R 5C7)
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FAX: (514) 695-3707

Pointe Claire (H9R 5P7)
Marshall Industries
148 Brunswick Blvd.
TEL: (514) 694-8142
FAX: (514) 694-6989

Quebec (G2E 5G5)
Future Electronics Corp.
1000 Avenue Street Jean-Baptiste, Ste. 100
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FAX: (418) 877-6671

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2795 Rue Halpern
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FAX: (514) 335-2381

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EBV Elektronik
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1150 Wien
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B–1810 Wemmel
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SF-00241 Helsinki
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Postfach 1246 – 25443 Quickborn
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FAX: (49) 511 816048

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FAX: (49) 6151 294171

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Alfred Neye Enatechnik GmbH
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TEL: (49) 89 9099990
FAX: (49) 89 90999940

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Postfach 700159 – 70571 Stuttgart
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CED Ditronic GmbH
Bernbacherstrasse 9
90768 Furth
TEL: (49) 911 752216
FAX: (49) 911 7520064

CED Ditronic GmbH
Ebertshelmer Strasse 12 – 67280 Quirheim
TEL: (49) 6359 83201
FAX: (49) 6359 83201

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FAX: (49) 030 3419003

EBV Elektronik GmbH
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TEL: (49) 7152 300090
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EBV Elektronik GmbH
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Postfach 1109 – 85529 Haar
D–8013 Haar
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FAX: (49) 089 464488

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7000 Stuttgart 1
TEL: (49) 0711 619100
TLX: 722271
FAX: (49) 07512 75958

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TEL: (49) 2132 530072
FAX: (49) 2131 59300087

EBV Elektronik GmbH
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Postfach 1355 – 30929 Burgwedel
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FAX: (49) 5139 5199

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TEL: (49) 069 785037
FAX: (49) 069 7894458

Elkose GmbH Elektronik Vertrieb
ITT Multikomponent GmbH
Elektronik Vertrieb
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Königsberger Strasse 16A – 12207 Berlin
Postfach 420 – 12174 Berlin
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Spoerle Electronic
Kackertstrasse 10 – 52072 Aachen
TEL: (49) 241 889690
FAX: (49) 241 81162

Spoerle Electronic
Rudower Strasse 27-29 – 12351 Berlin
Postfach 47645 – 12315 Berlin
TEL: (49) 30 606011
TLX: 186029
FAX: (49) 30 6014057

Spoerle Electronic
Hildebrandstrasse 11 – 44319 Dortmund
Postfach 130362 – 44313 Dortmund
TEL: (49) 231 218010
TLX: 822555
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TLX: 417983
FAX: (49) 6103 304201

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TEL: (49) 761 510450
TLX: 7721994
FAX: (49) 761 502233

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Rodeweg 18 – 37081 Gottingen
Postfach 3352 – 37023 Gottingen
TEL: (49) 551 9040
TLX: 96733
FAX: (49) 551 90446/48

Spoerle Electronic
Winsbergring 42 – 22525 Hamburg
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TEL: (40) 40 8531340
TLX: 2164536
FAX: (49) 40 85313491

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Spoerle Electronic Rathsbergstrasse 17 – 90411 Nurnberg
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FAX: (40) 911 5215635

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Postfach 35 35
D-74025 Heilbronn
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FAX: (49) 07131 67-2100

ITALY

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FAX: (39) 2 668 02 919

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FAX: (39) 224 09 255

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