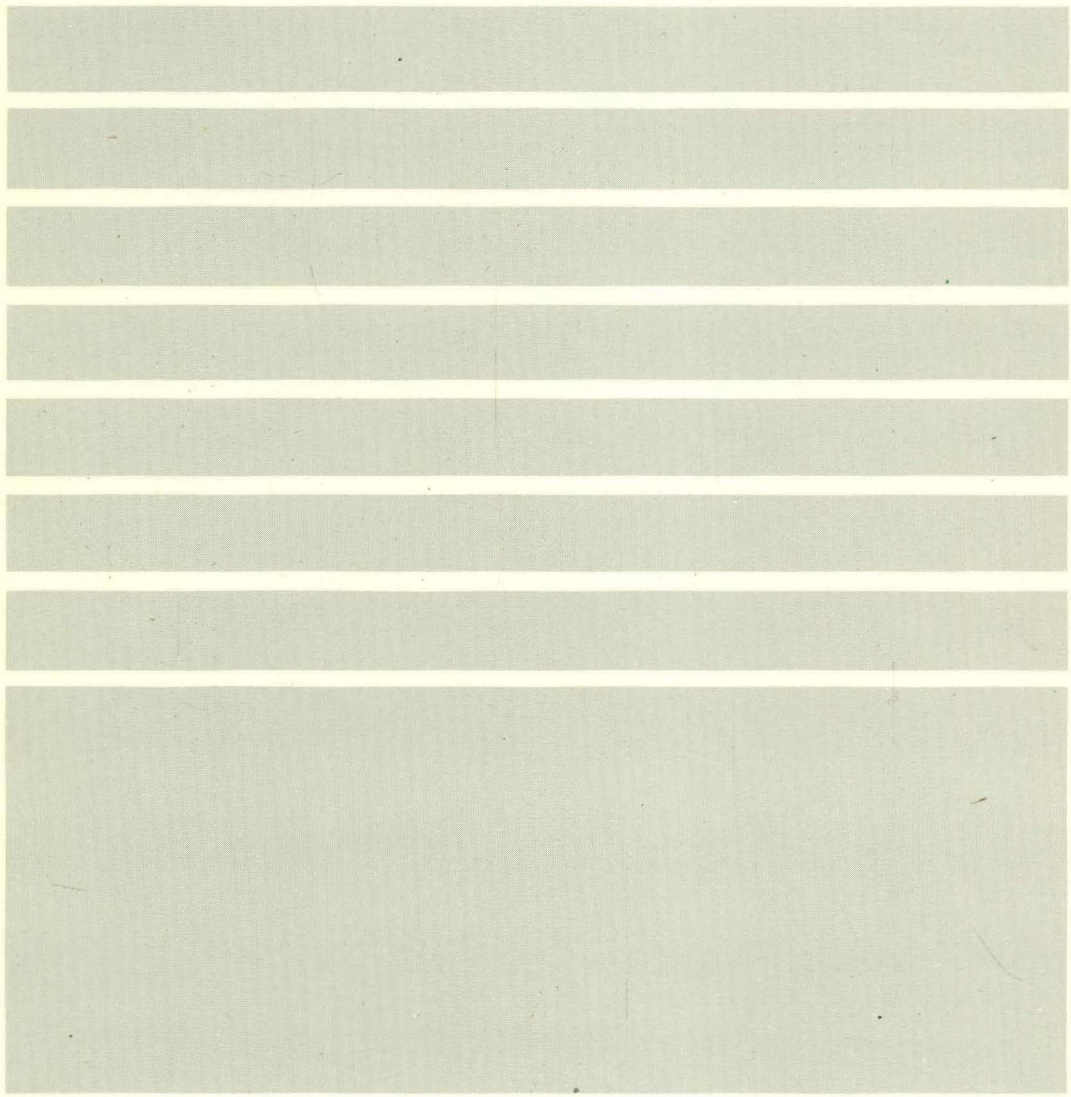
Signetics

Linear Data Manual Volume 1 Communications



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Linear Products

1989 Linear Data Manual Volume 1: Communications

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Preface

Linear Products

The Linear Division, one of four Signetics product divisions, is a major supplier of a broad line of linear integrated circuits ranging from high performance application specific designs to many of the more popular industry standard devices.

A fifth Signetics division, the Military Division, provides military-grade integrated circuits, including Linear. Please consult the Signetics Military data book for information on such devices.

Employing Signetics' high quality processing and screening standards, the Linear Division is dedicated to providing high-quality linear products to our customers worldwide.

The three 1989 Linear Data and Applications Manuals provide extensive technical data and application information for a broad range of products serving the needs of a wide variety of markets.

Volume 1 — Communications:
Contains data and application information concerning our radio and audio circuits, compandors, phase-locked loops, compact disk circuits, and ICs for RF communication, fiber optic communication, telephony and modem applications.

Volume 2 — Industrial:
Contains data and application information concerning our data conversion products (analog-to-digital and digital-to-analog), sample-and-hold circuits, comparators, driver/receiver ICs, amplifiers, position measurement devices, power conversion and control ICs and music/speech synthesizers.

Volume 3 — Video:
Contains data and application information concerning our video products. This includes tuning, video IF and audio IF circuits, sync processors/generators, color decoders and encoders, video processing ICs, vertical deflection circuits, and power supply controllers for video applications.

Each volume contains extensive product-specific application information. In addition there are selector guides and product-specific symbols and definitions to facilitate the selection and understanding of Linear products. A functional Table of Contents for each of the three volumes and a complete product and application note listing is also included.

Although every effort has been made to ensure the accuracy of information in these manuals, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in future editions are welcome.

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Pin-for-Pin Functionally-Compatible*
Cross Reference by Manufacturer

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
AMD	AM26LS30PC	AM26LS30CN	0 to +70	Plastic
	AM26LS31PC	AM26LS31CN	0 to +70	Plastic
	AM26LS32PC	AM26LS32CN	0 to +70	Plastic
	AM25LS33PC	AM26LS33CN	0 to +70	Plastic
	AM6012DC	AM6012F	0 to +70	Ceramic
	DAC-08AQ	DAC-08AF	−55 to +125	Ceramic
	DAC-08CN	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08EN	DAC-08EN	0 to +70	Plastic
	DAC-08EQ	DAC-08EF	0 to +70	Ceramic
	DAC-08HN	DAC-08HN	0 to +70	Plastic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	−55 to +125	Ceramic
	LF198H	LF198H	−55 to +125	Metal Can
	LF198H	SE5537H	−55 to +125	Metal Can
	LF398H	LF398H	0 to +70	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398L	LF398D	0 to +70	Plastic
	LF398L	NE5537D	0 to +70	Plastic
	LF398N	LF398N	0 to +70	Plastic
	LF398N	NE5537N	0 to +70	Plastic
Datel	AM-453-2	NE5534/AF	0 to +70	Ceramic
	AM-453-2C	NE5534/AF	0 to +70	Ceramic
	AM-453-2M	SE5534/AF	−55 to +125	Ceramic
	DAC-UP10BC	NE5020N	0 to +70	Plastic
	DAC-UP8BC	NE5018N	0 to +70	Plastic
	DAC-UP8BM	SE5019F	−55 to +125	Ceramic
	DAC-UP8BQ	SE5018F	−55 to 125	Ceramic
Exar	XR-558CN	NE558F	0 to +70	Ceramic
	XR-558CP	NE558N	0 to +70	Plastic
	XR-558M	SE558F	−55 to +125	Ceramic
	XR-L567CN	NE567F	0 to +70	Ceramic
	XR-L567CP	NE567N	0 to +70	Plastic
	XR-1488CP	MC1488N	0 to +70	Plastic
	XR-1489/ACP	MC1489/AN	0 to +70	Plastic
	XR-1524N	SG3524F	0 to +70	Ceramic
	XR-1524P	SG3524N	0 to +70	Plastic
	XR-2524P	SG3524N	0 to +70	Plastic
	XR-3524N	SG3524F	0 to +70	Ceramic
	XR-3524P	SG3524N	0 to +70	Plastic
	XR-4558CP	NE4558N	0 to +70	Plastic
	XR-5532/A N	NE5532/AF	0 to +70	Ceramic
	XR-5532/A P	NE5532/AN	0 to +70	Plastic
	XR-5534/A CN	NE5534/AF	0 to +70	Ceramic
	XR-5534/A CP	NE5534/AN	0 to +70	Plastic
	XR-5534/A M	SE5534/AF	−55 to +125	Ceramic
	XR-6118CP	NE594N	0 to +70	Plastic
	XR-13600CP	NE5517N	0 to +70	Plastic
Harris	HA-2539N	NE5539N	0 to +70	Plastic
	HA-2420-2/8B	SE5060F	−55 to +125	Ceramic
	HA-2425N	NE5060N	0 to +70	Plastic
	HA-2425B	NE5060F	0 to +70	Ceramic
	HA-5320B	NE5060F	0 to +70	Ceramic

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
	HA1-5102-2	SE5532/AF	−55 to +125	Ceramic
	HA1-5135-2	SE5534/AF	−55 to +125	Ceramic
	HA1-5135-5	NE5534/AF	0 to +70	Ceramic
	HA1-5202-5	NE5532/AF	0 to +70	Ceramic
	HA3-5102-5	NE5532/AN	0 to +70	Plastic
Intersil	ADC0803LCD	ADC0803-1 LCF	−40 to +85	Ceramic
	ADC0804	ADC0804-1 CN	0 to +70	Plastic
	ADC0805	ADC0805-1 LCN	−40 to +85	Plastic
	ICM7555CBA	ICM7555CD	0 to +70	Plastic
	ICM7555IPA	ICM7555IN	−40 to +85	Plastic
	ACM7555CP	ICM7555CN	0 to +70	Plastic
Motorola	AM26LS31PCD	AM26LS31CD	0 to +70	Plastic
	AM26LS31PC	AM26LS31CN	0 to +70	Plastic
	AM26LS32PC	AM26LS32CN	0 to +70	Plastic
	AM26LS32PCD	AM26LS32CD	0 to +70	Plastic
	DAC-08CD	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08ED	DAC-08EN	0 to +70	Plastic
	DAC-08EF	DAC-08EF	0 to +70	Ceramic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	−55 to +125	Ceramic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM311J-8	LM311F	0 to +70	Ceramic
	LM311N	LM311N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM339/A J	LM339/AF	0 to +70	Ceramic
	LM339/A N	LM339/AN	0 to +70	Plastic
	LM358N	LM358N	0 to +70	Plastic
	LM393A/J	LM393/AF	0 to +70	Ceramic
	LM393A/N	LM393/AN	0 to +70	Plastic
	MC1408L	MC1408F	0 to +70	Ceramic
	MC1408P	MC1408N	0 to +70	Plastic
	MC1488L	MC1488F	0 to +70	Ceramic
	MC1488P	MC1488N	0 to +70	Plastic
	MC1489/A L	MC1489/AF	0 to +70	Ceramic
	MC1489/A P	MC1489/AN	0 to +70	Plastic
	MC1496L	MC1496F	0 to +70	Ceramic
	MC1496P	MC1496N	0 to +70	Plastic
	MC3302L	MC3302F	−40 to +85	Ceramic
	MC3302P	MC3302N	−40 to +85	Plastic
	MC3361D	MC3361D	0 to +70	Plastic
	MC3361P	MC3361N	0 to +70	Plastic
	MC3403L	MC3403F	0 to +70	Ceramic
	MC3403P	MC3403N	0 to +70	Plastic
	MC3410CL	MC3410CF	0 to +70	Ceramic
	MC3410L	MC3410F	0 to +70	Ceramic
		NE5410F	0 to +70	Ceramic
	MC3510L	MC5410F	−55 to +125	Ceramic
	NE565N	NE565N	0 to +70	Plastic
	NE592F	NE592F-8	0 to +70	Ceramic
	NE592F	NE592F-14	0 to +70	Ceramic
	NE592N	NE592N-14	0 to +70	Plastic

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Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
	SE592F	SE592F-8	−55 to +125	Ceramic
	SE592F	SE592F-14	−55 to +125	Ceramic
	SE592H	SE592H	−55 to +125	Metal Can
National	ADC0803F	ADC0803-1 LCF	−40 to +85	Ceramic
	ADC0803N	ADC0803-1 LCN	−40 to +85	Plastic
	ADC0805	ADC0805-1 LCN	−40 to +85	Plastic
	ADC0820CCN	ADC0820CNEN	0 to +70	Plastic
	ADC0820CCD	ADC0820CSAN	−40 to +85	Plastic
	ADC0820CD	ADC0820CSEF	−55 to +125	Ceramic
	DAC0800LCJ	DAC-08EF	0 to +70	Ceramic
	DAC0800LJ	DAC-08F	−55 to +125	Ceramic
	DAC0800LCN	DAC-08EN	0 to +70	Plastic
	DAC0801LCJ	DAC-08CF	0 to +70	Ceramic
	DAC0801LCN	DAC-08CN	0 to +70	Plastic
	DAC0802LJ	DAC-08AF	−55 to +125	Ceramic
	DAC0802LCJ	DAC-08HF	0 to +70	Ceramic
	DAC0802LCN	DAC-08HN	0 to +70	Plastic
	DAC0806LCJ	MC1408-6F	0 to +70	Ceramic
	DAC0806LCN	MC1408-6N	0 to +70	Plastic
	DAC0807LCJ	MC1408-7F	0 to +70	Ceramic
	DAC0807LCN	MC1408-7N	0 to +70	Plastic
	DAC0808LCJ	MC1408F	0 to +70	Ceramic
	DAC0808LCN	MC1408N	0 to +70	Plastic
	DAC0808LD	MC1408F	0 to +70	Ceramic
	DS3691N	AM26LS30CN	0 to +70	Plastic
	DS3691M	AM26LS30CD	0 to +70	Plastic
	LF198H	SE5537H	−55 to +125	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398N	NE5537N	0 to +70	Plastic
	LM13600AN	NE5517N	0 to +70	Plastic
	LM13600N	NE5517N	0 to +70	Plastic
	LM1458N	MC1458N	0 to +70	Plastic
	LM161H	SE529H	−55 to +125	Metal Can
	LM161J	SE529F	−55 to +125	Ceramic
	LM2524J	SG3524F	0 to +70	Ceramic
	LM2524N	SG3524N	0 to +70	Plastic
	LM2901N	LM2901N	−40 to +85	Plastic
	LM2903N	LM2903N	−40 to +85	Plastic
	LM3089	CA3089N	−55 to +125	Plastic
	LM319J	LM319F	0 to +70	Ceramic
	LM319N	LM319N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM324AD	LM324AD	0 to +70	Plastic
	LM324AN	LM324AN	0 to +70	Plastic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM3524J	SG3524F	0 to +70	Ceramic
	LM3524N	SG3524N	0 to +70	Plastic
	LM358H	LM358H	0 to +70	Metal Can
	LM358N	LM358N	0 to +70	Plastic
	LM361H	NE529H	0 to +70	Metal Can
	LM361J	NE529D	0 to +70	
	LM361N	NE529N	0 to +70	Plastic
	LM393/AN	LM393/AN	0 to +70	Plastic
	LM555J	NE555F	0 to +70	Ceramic
	LM555N	NE555N	0 to +70	Plastic
	LM556J	SE556-1F	−55 to +125	Ceramic
	LM556N	SE556-1N	−55 to +125	Plastic
	LM556CJ	NE556-1F	0 to +70	Ceramic
	LM556CN	NE556-1N	0 to +70	Plastic
	LM565CN	NE565N	0 to +70	Plastic
	LM566N	SE566N	−55 to +125	Plastic
	LM566CN	NE566N	0 to +70	Plastic
	LM567CN	NE567N	0 to +70	Plastic
	LM733CN	μA733CN	0 to +70	Plastic
	LM741CJ	μA741CF	0 to +70	Ceramic
	LM741CN	μA741CN	0 to +70	Plastic
	LM741J	μA741F	−55 to +125	Ceramic
	LM741N	μA741N	−55 to +125	Plastic
	LM747CJ	μA747CF	0 to +70	Ceramic
	LM747CN	μA747CN	0 to +70	Plastic
	LM747J	μ747F	−55 to +125	Ceramic
	LM747N	μA747N	−55 to +125	Plastic
	LMC555CN	ICM7555CN	0 to +70	Plastic
	LMC555CM	ICM7555CD	0 to +70	Plastic
	μA080/DA	DAC-08F	0 to +70	Ceramic
	μA0801CDC	MC1408F	0 to +70	Ceramic
	μA0801CPC	MC1408N	0 to +70	Plastic
	μA0801EDC	DAC-08EF	0 to +70	Ceramic
	μA0801EPC	DAC-08AF	0 to +70	Ceramic
	μA124J	2M124F	−55 to +125	Ceramic
	μA1458TC	MC1458N	0 to +70	Plastic
	μA1488DC	MC1488F	0 to +70	Ceramic
	μA1488PC	MC1488N	0 to +70	Plastic
	μA1489/A PC	MC1489/AF	0 to +70	Ceramic
	μA1489/A PC	MC1489/AN	0 to +70	Plastic
	μA198HM	NE5537H	0 to +70	Metal Can
	μA198RM	NE5537N	0 to +70	Plastic
	μA2901DC	LM2901F	−40 to +85	Ceramic
	μA2901PC	LM2901N	−40 to +85	Plastic
	μA311RC	LM311F	0 to +70	Ceramic
	μA324DC	LM324F	0 to +70	Ceramic
	μA324PC	LM324N	0 to +70	Plastic
	μA3302DC	MC3302F	−40 to +85	Ceramic
	μA3302PC	MC3302N	−40 to +85	Plastic
	μA339/ADC	LM339/AF	0 to +70	Ceramic
	μA339/APC	LM339/AN	0 to +70	Plastic
	μA3403DC	MC3403F	0 to +70	Ceramic
	μA3403PC	MC3403N	0 to +70	Plastic
	μA398HC	SE5537H	−55 to +125	Metal Can
	μA398RC	SE5537N	−55 to +125	Plastic
	μA555TC	NE555N	0 to +70	Plastic
	μA556PC	NE556-1N, NE556N	0 to +70	Plastic
	μA723DC	μA723CF	0 to +70	Ceramic
	μA723DM	μA723F	−55 to +125	Ceramic
	μA723PC	μA723CN	0 to +70	Plastic
	μA733DC	μA733F	0 to +70	Ceramic
	μA733DM	μA733F	−55 to +125	Ceramic
	μA733PC	μA733N	0 to +70	Plastic
	μA741NM	μA741N	−55 to +125	Plastic
	μA741RC	μA741CF	0 to +70	Ceramic
	μA741TC	μA741CN	0 to +70	Plastic
	μA747DC	μA747CF	0 to +70	Ceramic
	μA747PC	μA747CN	0 to +70	Plastic
	UC3842D	UC3842D	0 to +70	Plastic
	UC3842J	UC3842FE	0 to +70	Ceramic
	UC3842N	UC3842N	0 to +70	Plastic
	UC2842D	UC2842D	0 to +70	Plastic
	UC2842J	UC2842FE	0 to +70	Ceramic
	UC2842N	UC2842N	0 to +70	Plastic

Cross Reference Guide

Manufacturer	Manufacturer Part Number	Signetics Part Number	Temperature Range (°C)	Package
	UC1842J	UC1842FE	-55 to +125	Ceramic
	UC1842N	UC1842N	-55 to +125	Plastic
NEC	μPC1571C	NE571N	0 to +70	Plastic
PMI	CMP-05GP	NE5105N	0 to +70	Plastic
	CMP-05CZ	SE5105F	-55 to +125	Ceramic
	CMP-05BZ	SE5105F	-55 to +125	Ceramic
	CMP-05GZ	SA5105N	-40 to +85	Plastic
	CMP-05FZ	SA5105N	-40 to +85	Plastic
	DAC1408A-6P	MC1408-6N	0 to +70	Plastic
	DAC1408A-6Q	MC1408-6F	0 to +70	Ceramic
	DAC1408A-7N	MC1408-7N	0 to +70	Plastic
	DAC1408A-7Q	MC1408-7F	0 to +70	Ceramic
	DAC1408A-8N	MC1408-8N	0 to +70	Plastic
	DAC1408A-8Q	MC1408-8F	0 to +70	Ceramic
	DAC1508A-8Q	MC1408-8F	-55 to +125	Ceramic
	DAC312FR	AM6012F	0 to +70	Ceramic
	OP27BZ	SE5534AFE	-55 to +125	Ceramic
	OP27CZ	SE5534FE	-55 to +125	Ceramic
	PM747Y	μA747N	-55 to +125	Plastic
	SMP-10AY	SE5060F	-55 to +125	Ceramic
	SMP-10EY	NE5060N	0 to +70	Plastic
	SMP-11AY	SE5060F	-55 to +125	Ceramic
	SMP-11EY	NE5060N	0 to +70	Plastic
Raytheon	RC4805DE	NE5105N	0 to +70	Plastic
	RC4805EDE	NE5105AN	0 to +70	Plastic
	RM4805DE	SE5105F	-55 to +125	Ceramic
	RM4805ADE	SE5105AF	-55 to +125	Ceramic
	RC5532/A DE	NE5532/AF	0 to +70	Ceramic
	RC5532/A NB	NE5532/AN	0 to +70	Plastic
	RC5534/A DE	NE5534/AF	0 to +70	Ceramic
	RC5534/A NB	NE5534/AN	0 to +70	Plastic
	RM5532/A DE	SE5532/AF	-55 to +125	Ceramic
	RM5534/A DE	SE5534/AF	-55 to +125	Ceramic
Silicon General	SG3524J	SG3524F	0 to +70	Ceramic
	SG3526N	SG3526N	0 to +70	Plastic
Sprague	UDN6118A	SA594N	-40 to +85	Plastic
	UDN6118R	SA594F	-40 to +85	Ceramic
	ULN3524A	SG3524	0 to +70	Plastic
	ULN8142M	UC3842N	0 to +70	Plastic
	ULN8160A	NE5560N	0 to +70	Plastic
	ULN8160R	NE5560F	0 to +70	Ceramic
	ULN8161M	NE5561N	0 to +70	Plastic
	ULN8168M	NE5568N	0 to +70	Plastic
	ULN8564A	NE564N	0 to +70	Plastic
	ULN8564R	NE564F	0 to +70	Ceramic
	ULS8564R	SE564F	-55 to +125	Ceramic
TI	ADC0803N	ADC0803-1 LCN	-40 to +85	Plastic
	ADC0804CN	ADC0804-1 CN	0 to +70	Plastic
	ADC0805N	ADC0805-1 LCN	-40 to +85	Plastic
	LM111J	LM111F	-55 to +125	Ceramic
	LM311D	LM311D	0 to +70	Plastic
	LM311J	LM311F	0 to +70	Ceramic
	LM311JG	LM311FE	0 to +70	Ceramic
	LM324D	LM324N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM358P	LM358N	0 to +70	Plastic
	LM393/A P	LM393/AN	0 to +70	Plastic
	MC1458P	MC1458N	0 to +70	Plastic
	NE5532/A JG	NE5532/AF	0 to +70	Ceramic
	NE5532/A P	NE5532/AN	0 to +70	Plastic
	NE5534/A JG	NE5534/AF	0 to +70	Ceramic
	NE5534/A P	NE5534/AN	0 to +70	Plastic
	NE555JG	NE555N	0 to +70	Plastic
	NE555P	NE555N	0 to +70	Plastic
	NE556P	NE556N	0 to +70	Plastic
	NE556J	NE556-1F	0 to +70	Ceramic
	NE556N	NE556-1N	0 to +70	Plastic
	NE592	NE592N14	0 to +70	Plastic
	NE592A	NE592F14	0 to +70	Ceramic
	NE592J	NE592F	0 to +70	Ceramic
	NE592N	NE592N-14	0 to +70	Plastic
	SA556P	SA556N	-40 to +85	Plastic
	SE5534/A JG	SE5534/AF	-55 to +125	Ceramic
	SE555JG	SE555N	-55 to +125	Plastic
	SE556J	SE556-1F	-55 to +125	Ceramic
	SE556N	SE556-1N	-55 to +125	Plastic
	SE592	SE592N14	-55 to +125	Plastic
	SE592J	SE592F-14	-55 to +125	Ceramic
	SE592N	SE592N-14	-55 to +125	Plastic
	SN55107AJ	NE521F	0 to +70	Plastic
	SN55108AJ	SE522F	-55 to +125	Ceramic
	SN75107AJ	NE521F	0 to +70	Plastic
	SN75107AN	NE521N	0 to +70	Plastic
	SN75108AJ	NE522F	0 to +70	Ceramic
	SN75108AN	NE522N	0 to +70	Plastic
	SN75188J	MC1488F	0 to +70	Ceramic
	SN75188N	MC1488N	0 to +70	Plastic
	SN75189AJ	MC1489AF	0 to +70	Ceramic
	SN75189AN	MC1489AN	0 to +70	Plastic
	SN75189J	MC1489F	0 to +70	Ceramic
	SN75189N	MC1489A	0 to +70	Plastic
	TL592A	NE592F14	0 to +70	Ceramic
	TL592P	NE592NB	0 to +70	Plastic
	μA723CJ	μA723CF	0 to +70	Ceramic
	μA723CN	μA723CN	0 to +70	Plastic
	μA723MJ	μA723F	-55 to +125	Ceramic
Unitrode	UC3524J	SG3524F	0 to +70	Ceramic
	UC3524N	SG3524N	0 to +70	Plastic

*THERE MAY BE PARAMETRIC DIFFERENCES BETWEEN SIGNETICS' PARTS AND THOSE OF THE COMPETITION.

Cross Reference Guide by Numeric Listing

NUMERIC	DESCRIPTION	SIGNETICS	ANALOG DEVICES	EXAR	FAIRCHILD	HITACHI	LINEAR TECH	MOTOROLA	NATIONAL	NEC	PMI	RAY-THEON	RCA	SGS/ THOMSON	SILICON GENERAL	SPRAGUE	TI	OTHERS
DAC-08	8-Bit D/A Converter	DAC-08F DAC-08AF DAC-08CF, CN NE5007F, N DAC-08ED, EN NE5008D, F, N SE5008F DAC-08HF, HN NE5009F, N SE5009F	ADDAC-08		µA080/DA µA0801E	HA17008		DAC-08	DAC-0800 DAC-0801 DAC-0802	µPC624	DAC-08							DATEL DAC-08 AMD DAC-08 Harris-HI5618
08031 0804/ 0805	8-Bit A/D Converter	ADC0803LCF, LCN ADC0804CN, LCD, LCF, LCN, ADC0805 LCN							ADC0803 ADC0804 ADC0805								ADC0803 ADC0804 ADC0805	Intersil ADC0803 0840 0805
0820	8-Bit CMOS A/D Converter	ADC0820 CNED ADC0820CNEN	AD7820						ADC0820									Maxim Max150
111	Voltage Comparator	LM111FE	AD111		µA111		LM111	LM111	LM111		PM111	LM111			SG111		LM111	
119	Dual Comparator	LM119F					LT119 LM119		LM119		PM119							
124	Quad OP Amp	LM124F, N			LM124		LT1014	LM124	LM124				CA124		SG124		LM124	
13600	High Performance Dual Transcon Amp	NE5517AN NE5517D, N		XR13600					LM13600/A									
139	Quad Comparator	LM139AF LM139F, N			µA139			LM139	LM139		PM139 CMP-04	LM139		CA139			LM139	
1408/ 1508	8-Bit D/A Converter	MC1408-6F, N MC1408-7F, N MC1408-8D, F, N MC1508-8F	AD1408		µA0801C	HA17408		MC1408/ 1508	DAC0806 0807 0808		DAC-1408	DAC-1408						Harris HI5618
1458/ 1558	Dual Op Amp	MC1458D, N MC1558N SA1458N			µA1458			MC1458 MC1558	LM1458 LM1558	µPC251	OP-14		CA1458	MC1458			MC1458	Harris CM1458 Samsung MC1458 Micro Power MP OP-14
1488	Quad Line Driver	MC1488D, F, N		XR1488	µA1488			MC1488	DS1488					MC1488			SN75188 MC1488	
1489	Quad Line Receiver	MC1489A, D, F, N MC1489D, F, N		XR1489/ A	µA1489/A			MC1489/A	DS1489/A					MC1489	SG1489/A		SN75189/A MC1489/A	
1496/ 1596	Balanced Modulator/ Demodulator	MC1496F, N MC1596F, N			µA796			MC1496 MC1596	LM1496 LM1596						SG1496			Plessey SL1496
1524	Improved SMPS Control Circuit	SG1524CF, CN		XR1524			LT1524						CA1524	SG1524	SG1524	ULN8124	SG1524	Cherry CS1524 Unitrode UC1524
158	Dual Op Amp	LM158FE, N NE532FE, N						LM158	LM158					LM158			LM158	Intersil CA158
193	Dual Comparator	LM193AFE LM193FE			µA193			LM193/A	LM193/A								LM193/A	

Cross Reference Guide by Numeric Listing (Continued)

NUMERIC	DESCRIPTION	SIGNETICS	ANALOG DEVICES	EXAR	FAIRCHILD	HITACHI	LINEAR TECH	MOTOROLA	NATIONAL	NEC	PMI	RAYTHEON	RCA	SGS/ THOMSON	SILICON GENERAL	SPRAGUE	TI	OTHERS
198	Sample-and-Hold Amp	LF198FE, H SE5537FE, H			μA198		LF198		LF198									AMD LF198 Harris HA2430
211	Voltage Comparator	LM211D, FE, N	AD211					LM211	LM211		PM211				SG211		LM211	
219	Dual Comparator	LM219D, F, N							LM219					TDE0119				
224	Quad Op Amp	LM224D, F, N SA534D, F, N			μA224	HA17224		LM224	LM224					LM224			LM224	
239	Quad Voltage Comparator	LM239AN LM239F, N			μA239			LM239	LM239		PM239 CMP-04	LM239	CA239				LM239	
2524	Improved SMPS Control IC	SG2524CN													SG2524			Cherry CS2524 Unitrode UC2524
258	Dual Op Amp	LM258N SA532D, N			μA258	HA17258		LM258	LM258	μPC258			CA258	LM258			LM258	
2577	Sync with Vert Osc and Driver	TDA2577A												TDA2577				
2593	Horizontal Combination	TDA2593												TDA2593				Plessey TA2593
26LS31	Quad Hi-Speed Line Driver	AM26LS31 CD, CN, IN, MN			AM26LS31			AM26LS31	DS26LS31								AM26LS31	AMD AM26LS31
2901	Quad Voltage Comparator	LM2901D, F, N			μA2901			LM2901	LM2901								LM2901	
2902	Quad Op Amp	LM2902D, N SA534D, F, N			μA2902			LM2902	LM2902								LM2902	
2903	Dual Voltage Comparator	LM2903D, FE, N			μA2903			LM2903	LM2903								LM2903	
2904	Dual Op Amp	LM2904D, N			μA2904			LM2904	LM2904								LM2904	
293	Dual Comparator	LM293AFE, AN LM293FE, N						LM293/A	LM293/A								LM293/A	
3089	FM IF System	CA3089N							LM3089				CA3089					
311	Voltage Comparator	LM311D, FE, N			μA311			LM311	LM311								LM311	
319	High-Speed Dual Comparator	LM319D, F, N							LM319	μPC319				LM319				
324	Quad Op Amp	LM324AD, AN LM324D, F, N			μA324	HA17324		LM324/A	LM324/A					LM324			LM324	Samsung LM324
3302	Quad Voltage Comparator	MC3302D, F, N			μA3303			MC3302										
3303	Quad Op Amp	MC3303F, N			μA3303			MC3303						MC3303			M3303	
3361	Low Power FM IF	MC3361D, N						MC3361										Samsung MC3361
339	Quad Voltage Comparator	LM339AF, AN LM339D, F, N			μA339			LM339/A	LM339/A	μPC339	PM339	LM339	CA339	LM339			LM339	
3403/ 3503	Quad Op Amp	MC3403D, F, N MC3505, F, N		μA3403				MC3403 MC3503				RM4137		MC3403 MC3503			MC3403 MC3503	

Cross Reference Guide by Numeric Listing (Continued)

NUMERIC	DESCRIPTION	SIGNETICS	ANALOG DEVICES	EXAR	FAIRCHILD	HITACHI	LINEAR TECH	MOTOROLA	NATIONAL	NEC	PMI	RAYTHEON	RCA	SGS/ THOMSON	SILICON GENERAL	SPRAGUE	TI	OTHERS
3410/ 3510	10-Bit D/A Converter	MC3410F MC3410CF MC3510F						MC3410/C MC3510										Harris HI-5610
3524	SMPS Control Circuit	SG3524D, F, N		XR3524			LT3524		LM3524				CA3524	SG3524	SG3524	ULN3524	SG3524	Cherry CS3524 Unitrode UC3524
3524C	Improved SMPS Control Circuit	SG3524C, D, N														SG3524B		Unitrode UC3524A
3526	SMPS	SG3526F, N						SG3526							SG3526	ULN8126		Unitrode UC3526
358	Dual Op Amp	LM358AD, AN LM358D, N NE532D, N				HA17358		LM358/A	LM358/A	µPC358	OP-221		CA358/A	LM358			LM358/A	Sanyo LA6358
361	See 529																	
3842	SMPS IC	UC3842N, D						UC3842AN							SG3842M			Unitrode UC3842N/D Cherry CS3842AN
387	See 542																	
393	Dual Comparator	LM393AFE, AN LM393D, N LM393FE-Sole Source				HA17393		LM393/A	LM393/A					LM393			LM393/A	Sanyo LA6393
398	Sample-and-Hold Amp	LF398D, FE, H, N NE5537D, FE, H, N			µA398		LF398		LF398		SMP-10							AMD LF398 Harris HA2425
4558	Dual General Purpose Op Amp	NE4558D, FE, N SA4558FE, N SE4558FE, N		XR4588				MC4558					RC4558					
5007	See DAC-08C																	
5008	See DAC-08E																	
5009	See DAC-08H																	
5018	8-Bit Converter Voltage Out	NE5018D, F, N SE5018F																AMD AM6081 Datel DAC µP8B
5019	8-Bit D/A Converter Voltage Out	NE5019F, N SE5019F																Datel DAC µP8BM
5020	10-Bit D/A Converter Voltage Out	NE5020F, N																Datel DAC µP10
5060	High-Speed Precision Sample-and-Hold Amp	NE5060F	AD583								SMP-10 SMP-11							Harris HA2420 HA2425 HA5320
5105	High-Speed Precision Comparator	NE5105D, N SA5105AN (NE5105AD, AN-sole source)									CMP-05	RCA805						

Cross Reference Guide by Numeric Listing (Continued)

NUMERIC	DESCRIPTION	SIGNETICS	ANALOG DEVICES	EXAR	FAIRCHILD	HITACHI	LINEAR TECH	MOTOROLA	NATIONAL	NEC	PMI	RAYTHEON	RCA	SGS/ THOMSON	SILICON GENERAL	SPRAGUE	TI	OTHERS
5118	8-Bit D/A Converter Current Out	NE5118F, N SE5118F																Datel DAC-UP
5170	Octal Line Driver	NE5170A, N																Unitrode UC5170
5180	Octal Line Receiver	NE5180A, N																Unitrode UC5180
529	High-Speed Comparator	NE529D, F, H, N SE529F, H							LM161 LM361									
531	High Slew Rate Op Amp	NE531FE, H, N										RC4531						Harris HA2515
532	See 358																	
542	Low Noise Dual PreAmp	NE542N							LM367									
5517	See 13600																	
5532	Dual Low Noise Op Amp	NE5532AFE, AN NE5532D, FE, N SE5532AFE, FE		XR5532/A								RC5532/A					NE5532/A	Harris HA35102-5
5533	Dual Low Noise Op Amp	NE5533AN NE5533D, N		XR5533													NE5533/A	
5534	Low Noise Op Amp	NE5534AD, AN (NE5534AFE-sole source) NE5534D, FE, N SA5534AD, AN SA5534N SE5534AFE, AN SE5534FE, N		XR5534							OP-27	RC5534/A					NE5534/A	Analog Systems MA332 Datel AM453-2C Harris HA5101/11
5537	See 398																	
5539	Fast Op Amp	NE5539D, F, N SE5539, F, H	AD5539															Harris HA2539
555	Timer	NE555D, FE, N SA555D, N SE555CN, FE, N		XR555	μA555	HA17555		NE555 MC1455	LM555	μPC555		RC555	CA555	NE555			NE555	Intersil NE555
556	Dual Timer	NE556D, F, N SA556N SE556CN, F, N			μA556			NE556 MC1456	LM556					NE556			NE556	Samsung NE556
5560	SMPS Control Circuit	NE5560D, F, N SE5560F, N														ULN8160 *disc		Cherry CS5560C IPS *disc IP5560C
5561	SMPS Control Circuit	NE5561D, FE, N SE5561FE, N														ULN8161 *disc		Cherry CS5561 IPS *disc IP5561C
5568	SMPS Control Circuit	NE5568D, N														ULN8168 *disc		Cherry CS5568 IPS *disc IP5568C

Cross Reference Guide by Numeric Listing (Continued)

NUMERIC	DESCRIPTION	SIGNETICS	ANALOG DEVICES	EXAR	FAIRCHILD	HITACHI	LINEAR TECH	MOTOROLA	NATIONAL	NEC	PMI	RAYTHEON	RCA	SGS/ THOMSON	SILICON GENERAL	SPRAGUE	TI	OTHERS
558	Quad Timer	NE558D, F, N SA558N SE558F, N		XR558														
564	High Frequency Phase-Locked Loop	NE564N (NE564D, F-sole source)														ULN8564		
565	Phase-Locked Loop	NE565D, F, N SE565F, N						NE565	LM565									
566	Function Generator	NE566D, F, N SE566F, N							LM566									
567	Tone Decoder Phase-Locked Loop	NE567D, F, FE, N SE567FE, F, N (SE567D-sole source)		XR567 XR2567					LM567									MCE MCE-567 Samsung LM567
571	Compandor	NE571D, F, N (SA571D, F, N-sole source)								μPC1571C								
583	See 5060																	
592	Video Amplifier	NE592 D14, D8, F14, F8, H, HD14, HD8, HN14, HN8, N14, N8 SA592D8, N8 SE592 F14, F8, H, N14, N8			μA592C			NE592	LM592								NE592 TL592	Intersil NE592
594	Vacuum Fluorescent, Display Driver	NE594D, F, N SA594D, F, N SE594F, N		XR6118												ULN6188		Sanyo LB1290 Toshiba TD62781
6012	12-Bit D/A Converter	AM6012F (AM6012D-sole source)		XR3464					NS8464		DAC312							AMD AM6012 Harris HI562A
6081	See 5018																	
6456	1GHz Prescaler	SAB6456PN, TD																Siemens SD4211
723	Precision Voltage Regulator	μA723CD, CF, CN μA723F, N SA723CN			μA723	HA17723		MC1723	LM723			RC723 LM723	CA723 LM723	LM723	SG723		μA723	Intersil LM723
733	Differential Video Amp	μA733CF, CN μA733F, N			μA733	HA17733		MC1733	LM733								μA733	Intersil μA733
741	General Purpose Op Amp	μA741CD, CFE, CN μA741FE, N SA741CFE, CN			μA741	HA17741		MC1741	LM741		OP-02			LM741	SG741		μA741	Micropower MPOP-02 Plessey SL562 Samsung LM741

Cross Reference Guide by Numeric Listing (Continued)

NUMERIC	DESCRIPTION	SIGNETICS	ANALOG DEVICES	EXAR	FAIRCHILD	HITACHI	LINEAR TECH	MOTOROLA	NATIONAL	NEC	PMI	RAYTHEON	RCA	SGS/ THOMSON	SILICON GENERAL	SPRAGUE	TI	OTHERS
747	Dual Op Amp	µA747CD, CF, CN µA747F, N SA747CN			µA747	HA17747		MC1747	LM747	µPC1418	OP-04 PM747	RC747	CA747				µA747	Micropower MPOP-04
75188	See 1488																	
75189	See 1489																	
7555	CMOS TIMER	ICM7555CN, CD ICM7555IN, ID ICM7555MN							LMC555								TLC555	Intersil- ICM7555
7820	See 0820																	
8126	See 3526																	
8160	See 5560																	
8161	See 5561																	
8168	See 5568																	
8464	See 6012																	
8564	See 564																	

SO Availability List

Linear Products

PART NUMBER	SMD PACKAGE	DESCRIPTION
ADC0820D	SOL-20	8-Bit CMOS A/D
*DAC08ED	SO-16	8-Bit D/A Converter
*LF398D	SO-14	Sample-and-Hold Amp
LM1870D	SOL-20	Stereo Demodulator
LM2901D	SO-14	Quad Volt Comparator
LM2903D	SO-8	Dual Volt Comparator
LM311D	SO-8	Voltage Comparator
LM319D	SO-14	High-Speed Dual Comparator
LM324AD	SO-14	Quad Op Amp
LM324D	SO-14	Quad Op Amp
LM339D	SO-14	Quad Volt Comparator
LM358AD	SO-8	Dual Op Amp
LM358D	SO-8	Dual Op Amp
LM393D	SO-8	Dual Comparator
*MC1408-8D	SO-16	8-Bit D/A Converter
MC1458D	SO-8	Dual Op Amp
MC1488D	SO-14	Quad Line Driver
MC1489D	SO-14	Quad Line Receiver
MC1489AD	SO-14	Quad Line Receiver
MC3302D	SO-14	Quad Volt Comparator
MC3361D	SOL-16	Low Power FM IF
MC3403D	SO-14	Quad Low Power Op Amp
NE4558D	SO-8	Dual Op Amp
*NE5018D	SOL-24	8-Bit D/A Converter
*NE5019D	SOL-24	8-Bit D/A Converter
*NE5036D	SO-14	6-Bit A/D Converter
NE5037D	SO-16	6-Bit A/D Converter
NE5044D	SO-16	Prog 7-Channel Encoder
NE5045D	SO-16	7-Channel Decoder
NE5090D	SOL-16	Address Relay Driver
NE5105/AD	SO-8	High-Speed Comparator
NE5170A	PLCC-28	Octal Line Driver
NE5180A	PLCC-28	Octal Line Receiver
NE5204D	SO-8	High-Frequency Amp
NE5205D	SO-8	High-Frequency Amp
NE521D	SO-14	High-Speed Dual Comparator
NE5212D8	SO-8	Transimedance Amplifier
NE522D	SO-14	High-Speed Dual Comparator
NE5230D	SO-8	Low Voltage Op Amp
NE527D	SO-14	High-Speed Comparator
NE529D	SO-14	High-Speed Comparator

PART NUMBER	SMD PACKAGE	DESCRIPTION
NE532D	SO-8	Dual Op Amp
*NE544D	SOL-16	Servo Amp
*NE5512D	SO-8	Dual Hi-Perf Op Amp
*NE5514D	SOL-16	Quad Hi-Perf Op Amp
NE5517D	SO-16	Dual Hi-Perf Amp
NE5520D	SOL-16	LVDT Signal Cond Ckt
*NE5532D	SOL-16	Dual Low-Noise Op Amp
*NE5533D	SOL-16	Low-Noise Op Amp
NE5534AD	SO-8	Low-Noise Op Amp
NE5534D	SO-8	Low-Noise Op Amp
NE5537D	SO-14	Sample-and-Hold Amp
NE5539D	SO-14	Hi-Freq Amp Wideband
NE555D	SO-8	Single Timer
NE556D	SO-14	Dual Timer
NE5560D	SO-16	SMPS Control Ckt
NE5561D	SO-8	SMPS Control Ckt
NE5562D	SOL-20	SMPS Control Ckt
NE5568D	SO-8	SMPS Control Ckt
NE558D	SOL-16	Quad Timer
NE5592D	SO-14	Dual Video Amp
NE564D	SO-16	Hi-Frequency PLL
*NE565D	SO-14	Phase Locked Loop
NE566D	SO-8	Function Generator
NE567D	SO-8	Tone Decoder PLL
NE568D	SOL-20	PLL
NE571D	SOL-16	Compandor
NE572D	SOL-16	Prog Compandor
*NE587D	SOL-20	7 Seq LED Driver (Anode)
*NE589D	SOL-20	7 Seq LED Driver (Cath)
NE5900D	SOL-16	Call Progress Decoder
NE592D14	SO-14	Video Amp
NE592D8	SO-8	Video Amp
NE592HD14	SO-14	Hi-Gain Video Amp
NE592HD8	SO-8	Hi-Gain Video Amp
*NE594D	SOL-20	Vac Fluor Disp Driver
NE602D	SO-8	Double Bal Mixer/ Oscillator
NE604D	SO-16	Low Power FM IF System
NE605	SOL-20	FM IF System
NE612D	SO-8	Double Balanced Mixer/Oscillator
NE614D	SO-16	Low Power FM IF System
*PCD3311TD	SO-16	DTMF/Melody Generator

SO Availability List

PART NUMBER	SMD PACKAGE	DESCRIPTION
PCD3312TD	SO-8	DTMF/Melody Generator With ICC
PCD3315TD	SOL-28	Repertory Pulse Dial
PCD3360TD	SO-16	Progress Tone Ringer
PCF2100TD	SOL-28	LCD Duplex Driver (40)
PCF2111TD	VSO-40	LCD Duplex Driver (64)
PCF2112TD	VSO-40	LCD Duplex Driver (32)
PCF8570TD	SO-8	Static RAM (256 × 8)
PCF8571TD	SO-8	1K Serial RAM
PCF8573TD	SO-16	Clock/Timer
PCF8574TD	SO-16	Remote I/O Expander
PCF8576TD	VSO-56	MUX/Static Driver
PCF8577TD	VSO-40	32-/64-Segment LCD Driver
SA5105/AD	SO-8	High-Speed Comparator
SA5230D	SO-8	Low Voltage Op Amp
SA5212D8	SO-8	Transimpedance Amp
SA532D	SO-8	Dual Op Amp
SA534D	SO-14	Dual Op Amp
SA555D	SO-8	Single Timer
SA571D	SOL-16	Compandor
SA572D	SOL-16	Compandor
*SA594D	SOL-20	Vac Fluor Disp Driver
SA602D	SO-8	Double Bal Mixer/ Oscillator
SA604D	SO-16	Lower Power FM IF System

PART NUMBER	SMD PACKAGE	DESCRIPTION
SAA3004TD	SOL-20	R/C Transmitter
SG3524D	SO-16	SMPS Control Circuit
TDA1001BTD	SO-16	Noise Suppressor
TDA1005ATD	SO-16	Stereo Decoder
TDA3047TD	SO-16	IR Preamp
TDA3048TD	SO-16	IR Preamp
TDA5040TD	SO-8	Brushless DC Motor Driver
TDA7010TD	SO-16	FM Radio Circuit
TDA7050TD	SO-8	Mono/Stereo Amp
TDD1742TD	SOL-28	Frequency Synthesizer
ULN2003D	SO-16	Transistor Array
ULN2004D	SO-16	Transistor Array
μA723CD	SO-14	Voltage Regulator
μA741CD	SO-8	Single Op Amp
μA747CD	SO-14	Dual Op Amp

NOTE:
*Non-standard pinout.

NOTE:
For information regarding additional SO products released since the publication of this document, contact your local Signetics Sales Office.

Ordering Information for Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC

Linear Products

Signetics' Linear integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order
$250 per line item per order

Military Product:

$250 per line item per order

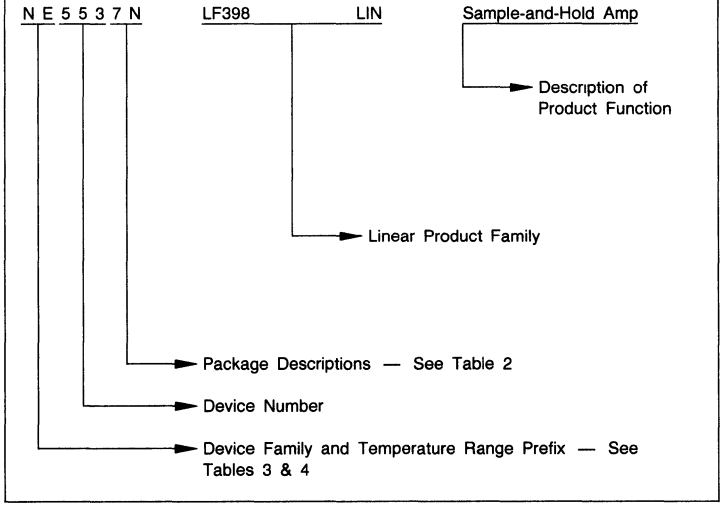
Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that an SE prefix (−55°C to +125°C) indicates only the operating temperature range of a device and *not* its military qualification status. The military qualification status of any Linear product can be determined by either looking in the Military Data Manual and/or contacting your local sales office.

Table 1. Part Number Description

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
N E 5 5 3 7 N	LF398	LIN	Sample-and-Hold Amp



Ordering Information

Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	−55°C to +125°C
SA	−40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard

Ordering Information for Prefixes HE, OM, PC, PN, SA, TD, TE

Linear Products

Signetics' integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors.

Minimum Factory Order:
Commercial Product:

$ 1000 per order

$ 250 per line item per order

Table 1 provides part number information concerning Signetics/Philips integrated circuits.

Table 2 provides package suffixes and descriptions for all presently existing types. Letters following the device number not used in Table 2 are considered to be part of the device number.

Table 3 provides explanations on the various prefixes employed in the part number descriptions. As noted in Table 3, Signetics/Philips device operating temperature is defined by the appropriate prefix.

OPERATING TEMPERATURE:
The third letter of the prefix, in a three-letter prefix, is the temperature designator.

The letters A to F give information about the operating temperature:

A: Temperature range not specified. See data sheet.
e.g. TDA2541N

B: 0 to +70°C
e.g. PCB8573PN

C: −55°C to +125°C
e.g. PCC2111PN

D: −25°C to +70°C
e.g. PCD8571PN

E: −25°C to +85°C
e.g. PCE2111PN

F: −40°C to +85°C
e.g. PCF2111PN

Table 1. Part Number Description

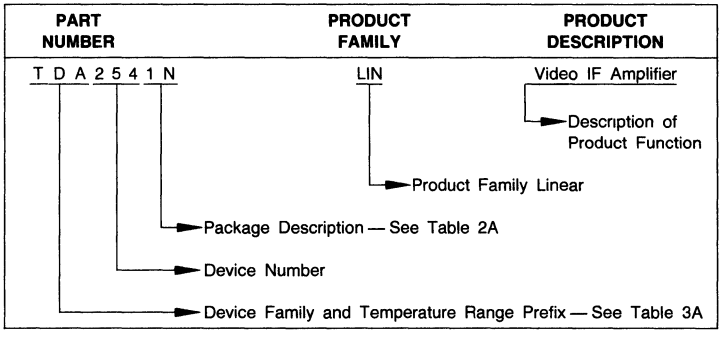


Table 2. Package Description

SUFFIX	PACKAGE DESCRIPTION
PN	8-, 14-, 16-, 18-, 20-, 24-, 28-, 40-lead plastic DIP
TD	Microminiature Package (SO)
DF	14-, 16-, 18-, 22-, 24-lead ceramic DIP
U	Single in-line plastic (SIP) and SIP power packages

Table 3. Device Prefix

PREFIX	DEVICE FAMILY
HEx	CMOS circuit
OM	Linear circuit
PCx	CMOS circuit
PNx	NMOS circuit
SAx	Digital circuit
TDx	Linear circuit
TEx	Linear circuit

Signetics

Linear Products

Section 2
Quality and Reliability

INDEX

SIGNETICS' ZERO DEFECTS PROGRAM

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressures. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable — zero defects — is, in fact, achievable.

The IC supplier committed to a standard of zero defects provides a competitive advantage to today's electronics OEM. That advantage can be summed up in four words: *reduced cost of ownership.* As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that the quality-conscious supplier represents a viable cost reduction resource. Consistently high quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures.

REDUCING THE COST OF OWNERSHIP THROUGH TOTAL QUALITY PERFORMANCE

Quality involves more than just IC's that work. It also includes cost-saving advantages that come with error-free service — on-time delivery of the right quantity of the right product at the agreed-upon price. Beyond the product, you want to know you can place an order and feel confident that no administrative problems will arise to tie up your time and personnel.

Today, as a result of Signetics' growing appreciation of the concern with cost of ownership, our quality improvement efforts extend out from the traditional areas of product conformance into every administrative function, including order entry, scheduling, delivery, shipping, and invoicing. Driving this process is a Corporate Quality Improvement Team, comprised of the president and his staff, which oversees the activities of 30 other Quality Improvement Teams throughout the company.

LINEAR PRODUCT QUALITY

Signetics has put together a winning process for the manufacturing of Linear Integrated Circuits. The circuits produced by our Linear Division must meet rigid criteria as defined in our design rules and as evaluated through product characterization over the device operating temperature range.

Product conformance to specification is measured throughout the manufacturing cycle. Signetics calls the first submittal to a Product or Quality Assurance gate our Estimated Process Quality or EPQ. It is an internal measure used to drive our Quality Improvement Programs toward our goal of Zero Defects. All product acceptance sampling plans have zero as their acceptance criteria. Only shipments that demonstrate zero defects during these acceptance tests may be shipped to our customers. This is in accordance with our commitment to our Zero Defect policy.

Our standard is Zero Defects and our customers' statistics and awards for outstanding product quality demonstrate our advance toward this goal. Nowhere is this more evident than at our Electrical and Visual-Mechanical Outgoing Product Assurance inspection gates. Over the past eight years, the measured defect level at the first submission to Electrical Product Assurance for Linear products has dropped from over 4000PPM (0.4%) to under 50PPM (0.005%) (See Figure 1a). Similarly our Visual-Mechanical (body defects, lead bend, etc.) defect level has improved remarkably (see Figure 1b). The results from our Quality Improvement Program have allowed Signetics to take the industry leadership position with its Zero Defects Limited Warranty policy. No longer is it necessary to negotiate a mutually acceptable AQL between buyer and Signetics. Signetics will replace any lot in which a customer finds one verified defective part.

QUALITY DATABASE REPORTING SYSTEM — QA05

The capabilities of our manufacturing process are measured and the results are recorded through our corporate-wide QA05 database system. The QA05 system collects the results on all finished lots and feeds this data back to concerned organizations where appropriate corrective actions can be taken. The QA05 reports Estimated Process Quality (EPQ) data which are the sample inspection results for first submittal lots to Quality Assurance inspection for electrical, visual/mechanical, hermeticity, and documentation. Data from this system is available upon request and is distributed routinely to our customers who have formally adopted our Ship-to-Stock program.

CUSTOMER/VENDOR COOPERATION IS AT THE HEART OF ZERO DEFECTS AND REDUCED COSTS

Working to a zero defects standard requires that emphasis be consistently placed, not on "catching" defects, but on preventing them from ever occurring. This strong preventive focus, which demands that quality be "built-in" rather than "inspected in," includes a much greater attention to ongoing communication on quality-related issues. At Signetics, a focus on this cooperative approach has resulted in better service to all customers and the development of two innovative customer/vendor programs: Ship-to-Stock and Self-Qual.

Signetics' Ship-to-Stock Program

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into inventory or to the assembly line from the customer's receiving dock without incoming inspection. This program was developed at the request of several major customers after they had worked with us and had a chance to experience the data exchange and joint corrective action that occurs as part of our quality improvement program.

The key elements of the Ship-to-Stock program are:

- Signetics and customer agree on a list of products to be certified, complete device correlation, and sign a specification.
- The product Estimated Product Quality (EPQ) must be 300ppm or less for the past 3 months.
- Signetics will share Quality (QA05) and Reliability data on a regular basis.
- Signetics will alert Ship-to-Stock customers of any changes in quality or reliability which could adversely impact their product.

Any customer interested in the benefits of the Ship-to-Stock program should contact his local Signetics sales office for a brochure and further details.

As a result of their participation in the Ship-to-Stock Program, many of our customers have eliminated costly incoming testing on selected ICs. We will work together with any customer interested to establish a Ship-to-Stock Program, and identify the products to be included in the program and finalize all neces-

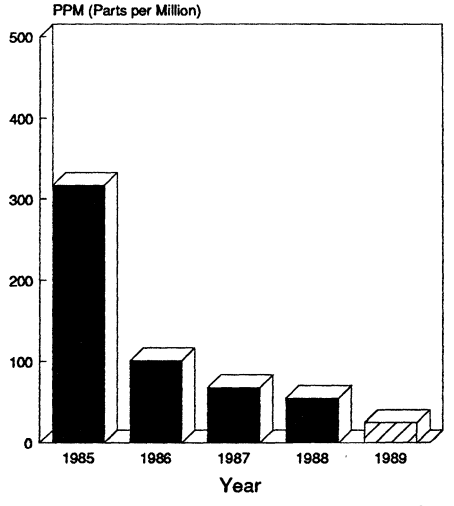


Figure 1a. Product Electrical Quality

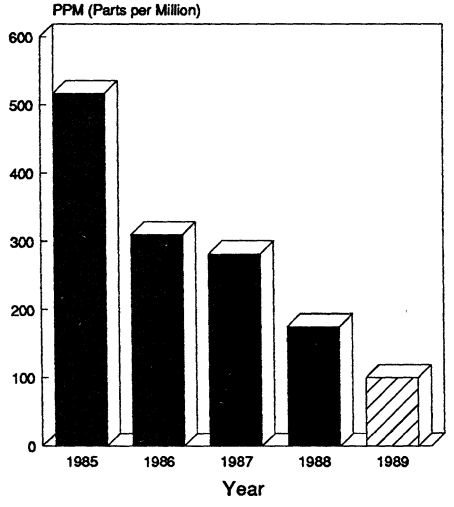


Figure 1b. Visual-Mechanical Quality

sary terms and conditions. From that point, the specified products can go directly from the receiving dock to the assembly line or into inventory. Signetics then provides, free of charge, monthly reports on those products.

In our efforts to continually reduce cost of ownership, we are now using the experience we have gained with Ship-to-Stock to begin developing a Just-in-Time Program. With Just-in-Time, products will be delivered to the receiving dock just as they are needed, permitting continuous-flow manufacturing and eliminating the need for expensive inventories.

Signetics Self-Qual Program

Like Ship-to-Stock, our Self-Qual Program employs a cooperative approach based on ongoing information exchange. At Signetics, formal qualification procedures are required for all new or changed materials, processes, products, and facilities. Prior to 1983, we created our qualification programs independently. Our major customers would then test samples to confirm our findings. Now, under the new Self-Qual Program, customers can be directly involved in the prequalification stage. When we feel we have a promising enhancement to offer, customers will be invited to participate in the development of the qualification plan. This eliminates the need to duplicate expensive qualification testing and also adds another dimension to our ongoing efforts to build in quality.

WE WANT TO WORK WITH YOU

At Signetics, we know that our success depends on our ability to support all our customers with the defect-free, higher density, higher performance products needed to compete effectively in today's demanding business environment. To achieve this goal, quality in another arena — that of communications — is vital. Here are some specific ways we can maintain an ongoing dialogue and information exchange between your company and ours on the quality issue:

- Periodical face-to-face exchanges of data and quality improvement ideas between the customer and Signetics can help prevent problems before they occur.
- Test correlation data is very useful. Line pull information and field failure reports also help us improve product performance.
- When a problem occurs, provide us as soon as possible with whatever specific data you have. This will assist us in taking prompt corrective action.

Quality products are, in large measure, the result of quality communication. By working together, by opening up channels through which we can talk openly to each other, we will insure the creation of the innovative, reliable, cost effective products that help insure a competitive edge.

QUALITY AND RELIABILITY ASSURANCE

Signetics' Linear Division Quality and Reliability Assurance Department is involved in all stages of the production of our Linear ICs:

- Product Design and Process Development
- Wafer Fabrication
- Assembly
- Inspection and Test
- Product Reliability Monitoring
- Customer liaison

The result of this continual involvement at all stages of production enables us to provide feedback to refine present and future designs, manufacturing processes, and test methodology to enhance both the quality and reliability of the products delivered to our customers.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 5×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. All circuit designs are computer-checked using the latest CAD software for adherence to design rules. Simulations are performed for functionality and parametric performance over the full operating ranges of voltage and temperature before going to production. These steps allow us to meet device specifications not only the first time, but also every time thereafter.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees.

RELIABILITY MEASUREMENT PROGRAMS

Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production product on a regularly established basis (see Table I below).

DESCRIPTION OF STRESSES

SHTL — Static High Temperature Life: SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem.

HTSL — High Temperature Storage Life: This stress exposes the parts to elevated temperatures (150°C – 175°C) with no applied bias.

THBS — Biased Temperature-Humidity, Static: This accelerated temperature and humidity bias stress is performed at 85°C and 85% relative humidity (85°C/85% RH).

TMCL — Temperature Cycling, Air-to-Air: The device is cycled between the specified upper and lower temperature without power in an air or nitrogen environment. Normal temperature extremes are −65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per Mil-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe.

PPOT — Pressure Pot: This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination in-

Table I. RELIABILITY ASSURANCE PROGRAMS

RELIABILITY FUNCTION	TYPICAL STRESS	FREQUENCY
New Process Qualification	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product
SURE III	High Temperature Operating Life Biased Temperature-Humidity, Static High Temperature Storage Life Pressure Pot Temperature Cycle Thermal Shock	Each fab process family, every four weeks
Product Monitor	Pressure Pot Thermal Shock	Each package type and technology family at each assembly plant, every week

duced leakage problems, and general glassivation stability and integrity

TMSK — Thermal Shock, Liquid-to-Liquid: Similar to TMCL, however, heating and cooling are done by immersing the units in hot and cold inert liquid. Temperature extremes are −65°C to +150°C with a minimum 5 minute dwell and less than 10 second transition per Mil-STD-883C, Method 1011.4, Condition C. Since heat transfer by conduction is generally much faster than by convection, the liquid-based thermal shock causes more rapid temperature changes in the part.

PRODUCT QUALIFICATION

Linear products are subjected to rigorous qualification procedures for all new products or redesigns to current products. Qualification testing consists of:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static bias
- High Temperature Storage Life: T_J = 175°C, 1000 hours, unbiased
- Temperature Humidity Biased Life. 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 20 psig, 127°C, 168 hours, unbiased
- Temperature Cycle: −65°C to +150°C, 500 cycles, 10 minute dwell, air to air, unbiased

Formal qualification procedures are required for all new or changed products, processes, and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

ONGOING RELIABILITY ASSESSMENT PROGRAMS

The SURE Program

The SURE (Systematic and Uniform Reliability Evaluation) program audits products from each of Signetics Linear Division's process families: Bipolar Junction, Single Layer Metal, Dual Layer Metal, Gold-Doped and Schottky, Oxide Isolated and ACMOS, under a variety of accelerated stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements

The Audit Program

Samples are selected from each process family every four weeks and are subjected to each of the following stresses.

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static bias
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker· 20 psig, 127°C, 72 hours, unbiased
- Thermal Shock. −65°C to +150°C, 300 cycles, 5 minute dwell, liquid-to-liquid, unbiased
- Temperature Cycling· −65°C to +150°C, 1000 cycles, 10 minute dwell, air-to-air, unbiased

The Product Monitor Program

In addition, each Signetics assembly plant performs Pressure Cooker and Thermal Shock SURE Product Monitor stresses on a weekly basis on each molded package by pin count per the same conditions as the SURE Program

Product Reliability Reports

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms, and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing

Reliability Engineering

In addition to the product performance monitors encompassed in the Linear SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

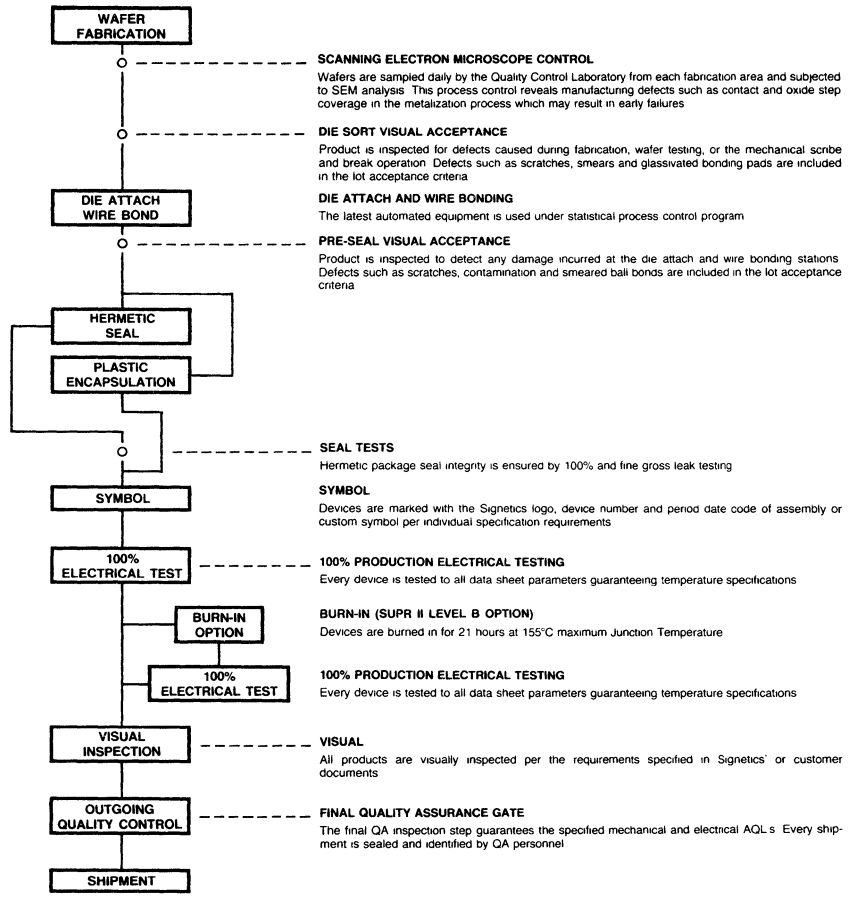
- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Device or generic group failure rate studies
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in some evaluation programs.

Failure Analysis

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional, and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

LINEAR DIVISION LINEAR PROCESS FLOW



SIGNETICS' MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilizes manufacturing facilities for wafer fabrication, package assembly, and test in three states and three overseas countries as shown in Table II. All wafer fabrication is performed in Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Pebei and Anam, are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. Signetics has on-site quality assurance personnel at each subcontractor to audit assembly processes and procedures.

All Signetics Linear products are electrically tested in Signetics operated facilities. These facilities report to the manufacturing organization (DMO or AMO) operating the facility at which they are located.

Table II. Signetics' Linear Product Manufacturing Facilities

WAFER FABRICATION FACILITIES		
Designation	**Location**	**Process Families**
Fab 01	Sunnyvale, California	Bipolar Junction Isolated
Fab 09	Orem, Utah	Bipolar Gold Doped
Fab 16	Sunnyvale, California	Oxide Isolated
Fab 21	Orem, Utah	Bipolar Schottky
Fab 22	Albuquerque, New Mexico	ACMOS
ASSEMBLY FACILITIES		
Designation	**Location**	**Package**
SigKor	Seoul, Korea	DIP, SO, and PLCC
SigThai	Bangkok, Thailand	DIP and CERDIP
Orem	Orem, Utah	Military "Jan" Hermetic
Pebei	Kaohsiung, Taiwan	SO
Anam	Seoul, Korea	SO and Metal Can
TEST FACILITIES		
Designation	**Location**	**Package**
TA03	Sunnyvale, California	Wafer Sort, Final Test and Quality Assurance
SigKor	Seoul, Korea	Final Test and Quality Assurance
SigThai	Bangkok, Thailand	Final Test and Quality Assurance
Sacto	Sacramento, California	Military Final Test and Quality Assurance

SYMBOLIZATION INFORMATION

Signetics' Linear Division products are symboled with the following information on each package:

- Signetics' Logo
- Product Identification and Package Designator
- Traceability Code*
- Assembly Date and Plant Codes*
- Product Revision Level*
- SUPR II B Processing Code (if applicable)

* May appear on the backside of SO 8, 14 & 16 lead packages due to space limitations on topside symbol.

Example:

S NE5534N line 1
FBW5491 line 2
8901VCB line 3

Line 1:
S = Signetics' Logo
NE5534 = Product type designation
N = Package type:
N = Dual-in-Line Plastic
F = Dual-in-Line CerDip
D = Small Outline (SO) Surface Mount
A = Plastic Leaded Chip Carrier (PLCC)
E or H = Metal Header

Line 2:
FBW5491 = 7 character Traceability Code assigned to each Assembly Lot which maintains product traceability back to the Wafer Fabrication. (May be truncated on SO-8 and metal headers.)

Line 3:
8901 = (YYWW) Assembly Date Code (YYWW) specifies the year (YY) and week number (WW) that begins the 4 week assembly period during which the product was manufactured. Thus, 8901 indicates that the product was packaged during the first four weeks of 1989. The first digit of the year may be omitted on some packages: 901.

V = Assembly Plant Code which indicates the assembly facility in which the finished product was packaged.
Assembly Plants Codes are:
V = Signetics Bangkok, Thailand
K = Signetics Seoul, Korea
B = Philips Kaohsiung, Taiwan
L = Anam Seoul, Korea
C = Product Revision Level
B = SUPR II B Burn-in Processing Code (if present) indicates that the product was processed through 100% SUPR II B Burn-in for 21 hours under biased operation at a junction temperature (Tj) of 155°C

Signetics

Linear Products

Section 3
Small Area Networks

3

INDEX

Introduction to I²C

THE I²C CONCEPT

The Inter-IC bus (I²C) is a 2-wire serial bus designed to provide the facilities of a small area network, not only between the circuits of one system, but also between different systems; e.g., teletext and tuning.

Philips/Signetics manufactures many devices with built-in I²C interface capability, any of which can be connected in a system by simply "clipping" it to the I²C bus. Hence, any collection of these devices around the I²C bus is known as "clips."

The I²C bus consists of two bidirectional lines: the Serial Data (SDA) line and the Serial Clock (SCL) line. The output stages of devices connected to the bus (these devices could be NMOS, CMOS, I²C, TTL, ...) must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C bus can be transferred at a rate up to 100kbits/sec. The physical bus length is limited to 13 feet and the number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

The inherent synchronization process, built into the I²C bus structure using the wired-AND technique, not only allows fast devices to communicate with slower ones, but also eliminates the "Carrier Sense Multiple Access/Collision Detect" (CSMA/CD) effect found in some local area networks, such as Ethernet.

Master-slave relationships exist on the I²C bus; however, there is no central master. Therefore, a device addressed as a slave during one data transfer could possibly be the master for the next data transfer. Devices are also free to transmit or receive data during a transfer.

To summarize, the I²C bus eliminates interfacing problems. Since any peripheral device can be added or taken away without affecting any other devices connected to the bus, the I²C bus enables the system designer to build various configurations using the same basic architecture.

Application areas for the I²C bus include:

- Video Equipment
- Audio Equipment
- Computer Terminals
- Home Appliances
- Telephony
- Automotive
- Instrumentation
- Industrial Control

Signetics

I²C Bus Specification

Linear Products

INTRODUCTION

For 8-bit applications, such as those requiring single-chip microcomputers, certain design criteria can be established:

- **A complete system usually consists of at least one microcomputer and other peripheral devices, such as memories and I/O expanders.**
- **The cost of connecting the various devices within the system must be kept to a minimum.**
- **Such a system usually performs a control function and does not require high-speed data transfer.**
- **Overall efficiency depends on the devices chosen and the interconnecting bus structure.**

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be resolved to decide which device will be in control of the bus and when. And if different devices with different clock speeds are connected to the bus, the bus clock source must be defined.

All these criteria are involved in the specification of the I²C bus.

THE I²C BUS CONCEPT

Any manufacturing process (NMOS, CMOS, I²L) can be supported by the I²C bus. Two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Each device is recognized by a unique address – whether it is a microcomputer, LCD driver, memory or keyboard interface – and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, while a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually microcomputers, let's consider the case of a data transfer between two microcomputers connected to the I²C bus (Figure 1). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would follow in this way:

1) Suppose microcomputer A wants to send information to microcomputer B
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master transmitter) sends data to microcomputer B (slave receiver)
   - microcomputer A terminates the transfer.
2) If microcomputer A wants to receive information from microcomputer B
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master receiver) receives data from microcomputer B (slave transmitter)
   - microcomputer A terminates the transfer.

Even in this case, the master (microcomputer A) generates the timing and terminates the transfer.

The possibility of more than one microcomputer being connected to the I²C bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event, an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all devices to the I²C bus.

If two or more masters try to put information on to the bus, the first to produce a one when the other produces a zero will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Arbitration and Clock Generation).

Generation of clock signals on the I²C bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow slave

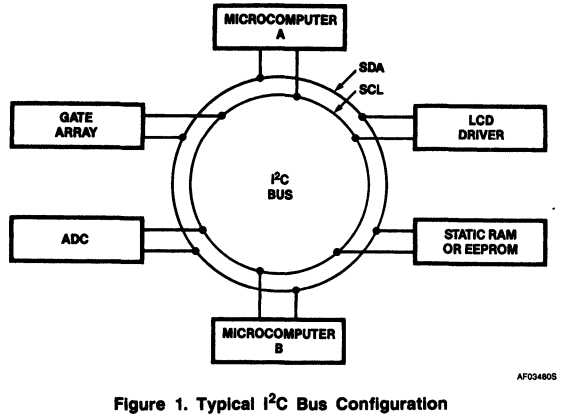


Figure 1. Typical I²C Bus Configuration

I²C Bus Specification

Table 1. Definition of I²C Bus Terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

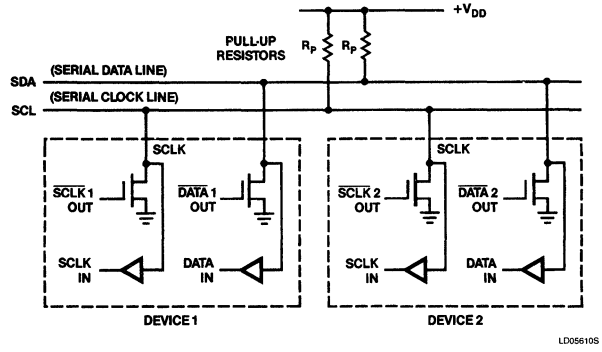


Figure 2. Connection of Devices to the I²C Bus

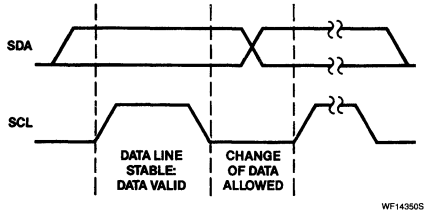


Figure 3. Bit Transfer on the I²C Bus

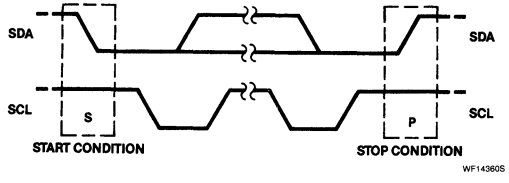


Figure 4. Start and Stop Conditions

device holding down the clock line or by another master when arbitration takes place.

GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 2). When the bus is free, both lines are High. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C bus can be transferred at a rate up to 100kbit/s. The number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, I²L) which can be connected to the I²C bus, the levels of the logical 0 (Low) and 1 (High) are not fixed and depend on the appropriate level of V_{DD} (see Electrical Specifications). One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the High period of the clock. The High or Low state of the data line can only change when the clock signal on the SCL line is Low (Figure 3).

Start and Stop Conditions

Within the procedure of the I²C bus, unique situations arise which are defined as start and stop conditions (see Figure 4).

A High-to-Low transition of the SDA line while SCL is High is one such unique case. This situation indicates a start condition.

A Low-to-High transition of the SDA line while SCL is High defines a stop condition.

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition. This bus free situation will be described later in detail.

Detection of start and stop conditions by devices connected to the bus is easy if they possess the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

TRANSFERRING DATA

Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit.

I²C Bus Specification

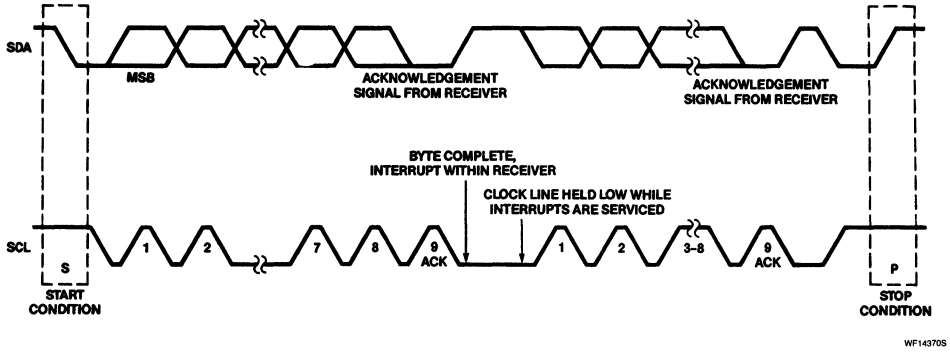


Figure 5. Data Transfer on the I²C Bus

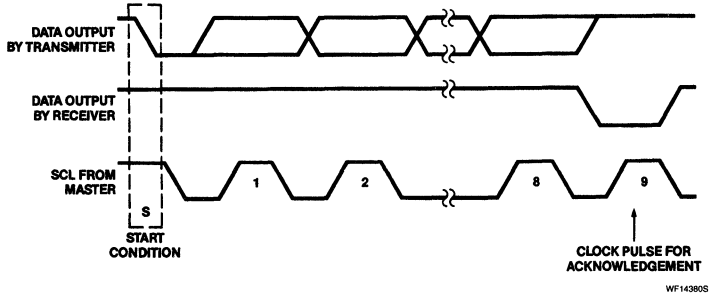


Figure 6. Acknowledge on the I²C Bus

Data is transferred with the most significant bit (MSB) first (Figure 5). If a receiving device cannot receive another complete byte of data until it has performed some other function, for example, to service an internal interrupt, it can hold the clock line SCL Low to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases the clock line SCL.

In some cases, it is permitted to use a different format from the I²C bus format, such as CBUS compatible devices. A message which starts with such an address can be terminated by the generation of a stop condition, even during the transmission of a byte. In this case, no acknowledge is generated.

Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitting device releases the SDA line (High) during the acknowledge clock pulse.

The receiving device has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable Low during the high period of this clock pulse (Figure 6). Of course, setup and hold times must also be taken into account and these will be described in the Timing section.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with a CBUS address.

When a slave receiver does not acknowledge on the slave address, for example, because it is unable to receive while it is performing some real-time function, the data line must be left High by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver does acknowledge the slave address, but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave not generating the acknowledge on the first byte following. The slave leaves the data line High and the master generates the STOP condition.

In the case of a master receiver involved in a transfer, it must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate the STOP condition.

ARBITRATION AND CLOCK GENERATION

Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C bus. Data is only valid during the clock High period on the SCL line; therefore, a defined clock is needed if the bit-by-bit arbitration procedure is to take place.

Clock synchronization is performed using the wired-AND connection of devices to the SCL LINE. This means that a High-to-Low transi-

I²C Bus Specification

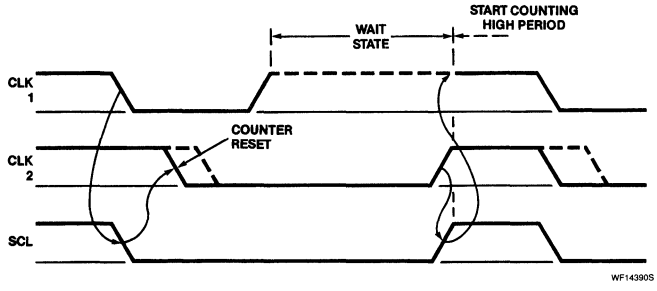


Figure 7. Clock Synchronization During the Arbitration Procedure

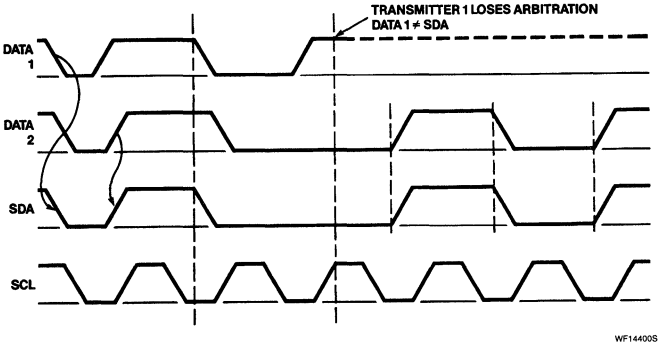


Figure 8. Arbitration Procedure of Two Masters

tion on the SCL line will affect the devices concerned, causing them to start counting off their Low period. Once a device clock has gone Low it will hold the SCL line in that state until the clock High state is reached (Figure 7). However, the Low-to-High change in this device clock may not change the state of the SCL line if another device
clock is still within its Low period. Therefore, SCL will be held Low by the device with the longest Low period. Devices with shorter Low periods enter a High wait state during this time.

When all devices concerned have counted off their Low period, the clock line will be released and go High. There will then be no difference between the device clocks and the state of the SCL line and all of them will start counting their High periods. The first device to complete its High period will again pull the SCL line Low.

In this way, a synchronized SCL clock is generated for which the Low period is determined by the device with the longest clock Low period while the High period on SCL is determined by the device with the shortest clock High period.

Arbitration

Arbitration takes place on the SDA line in such a way that the master which transmits a High level, while another master transmits a Low level, will switch off its DATA output stage since the level on the bus does not correspond to its own level.

Arbitration can carry on through many bits. The first stage of arbitration is the comparison of the address bits. If the masters are each trying to address the same device, arbitration continues into a comparison of the data. Because address and data information is used on the I²C bus for the arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master does lose arbitration during the addressing stage, it is possible that the winning master is trying to address it. Therefore, the losing master must switch over immediately to its slave receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course more may be involved, depending on how many masters are connected to the bus. The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a High output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. As control of the I²C bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Use of the Clock Synchronizing Mechanism as a Handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receiving devices to cope with fast data transfers, either on a byte or bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slave devices can then hold the SCL line Low, after reception and acknowledge of a byte, to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcomputer without a hardware I²C interface on-chip can slow down the bus clock by extending each clock Low period. In this way, the speed of any master is adapted to the internal operating rate of this device.

I²C Bus Specification

FORMATS

Data transfers follow the format shown in Figure 9. After the start condition, a slave address is sent. This address is 7 bits long; the eighth bit is a data direction bit (R/$\overline{W}$). A zero indicates a transmission (WRITE); a one indicates a request for data (READ). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another start condition, and address another slave without first generating a stop condition. Various combinations of read/write formats are then possible within such a transfer.

At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.

The stop condition is generated by the master.

During a change of direction within a transfer, the start condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

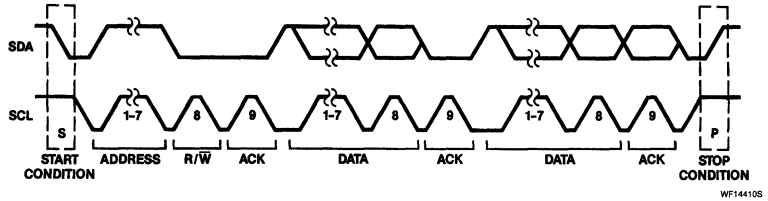
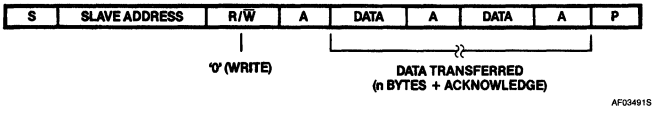


Figure 9. A Complete Data Transfer

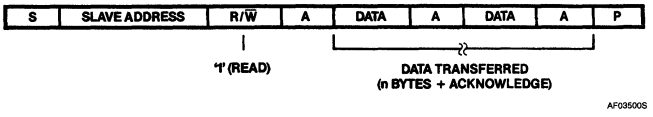
Possible Data Transfer Formats are:

a) Master transmitter transmits to slave receiver. Direction is not changed.

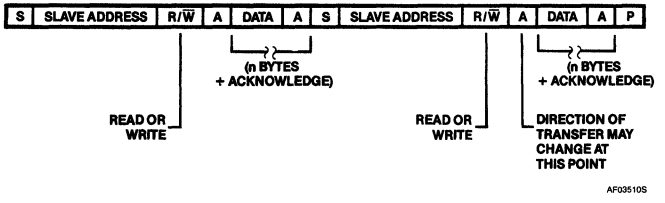
A = ACKNOWLEDGE
S = START
P = STOP



b) Master reads slave immediately after first byte.



c) Combined formats.



NOTES:
1 Combined formats can be used, for example, to control a serial memory During the first data byte, the internal memory location has to be written After the start condition is repeated, data can then be transferred
2 All decisions on auto-increment or decrement of previously accessed memory locations, etc , are taken by the designer of the device
3 Each byte is followed by an acknowledge as indicated by the A blocks in the sequence
4 I²C devices have to reset their bus logic on receipt of a start condition so that they all anticipate the sending of a slave address

I²C Bus Specification

ADDRESSING

The first byte after the start condition determines which slave will be selected by the master. Usually, this first byte follows that start procedure. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge, although devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

Definition of Bits in the First Byte

The first seven bits of this byte make up the slave address (Figure 10). The eighth bit (LSB – least significant bit) determines the direction of the message. A zero on the least significant position of the first byte means that the master will write information to a selected slave; a one in this position means that the master will read information from the slave.

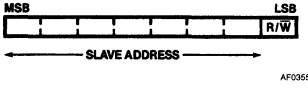


Figure 10. The First Byte After the Start Procedure

When an address is sent, each device in a system compares the first 7 bits after the start condition with its own address. If there is a match, the device will consider itself addressed by the master as a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

The slave address can be made up of a fixed and a programmable part. Since it is expected that identical ICs will be used more than once in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of eight identical devices can be connected to the same bus.

The I²C bus committee is available to coordinate allocation of I²C addresses.

The bit combination 1111XXX of the slave address is reserved for future extension purposes.

The address 1111111 is reserved as the extension address. This means that the addressing procedure will be continued in the next byte(s). Devices that do not use the extended addressing do not react at the reception of this byte. The seven other possibilities in group 1111 will also only be used for extension purposes but are not yet allocated.

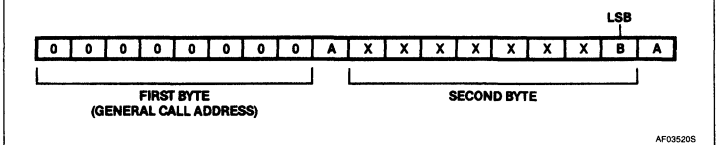


Figure 11. General Call Address Format

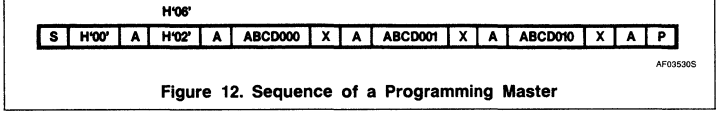


Figure 12. Sequence of a Programming Master

The combination 0000XXX has been defined as a special group. The following addresses have been allocated:

FIRST BYTE			
Slave Address		R/$\overline{W}$	
0000	000	0	General call address
0000	000	1	Start byte
0000	001	X	CBUS address
0000	010	X	Address reserved for different bus format
0000	011	X	To be defined
0000	100	X	
0000	101	X	
0000	110	X	
0000	111	X	

No device is allowed to acknowledge at the reception of the start byte.

The CBUS address has been reserved to enable the intermixing of CBUS and I²C devices in one system. I²C bus devices are not allowed to respond at the reception of this address.

The address reserved for a different bus format is included to enable the mixing of I²C and other protocols. Only I²C devices that are able to work with such formats and protocols are allowed to respond to this address.

General Call Address

The general call address should be used to address every device connected to the I²C bus. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If a device does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging.

The meaning of the general call address is always specified in the second byte (Figure 11).

There are two cases to consider:
1. When the least significant bit B is a zero.
2. When the least significant bit B is a one

When B is a zero, the second byte has the following definition:

00000110 (H'06') Reset and write the programmable part of slave address by software and hardware. On receiving this two-byte sequence, all devices (designed to respond to the general call address) will reset and take in the programmable part of their address.
Precautions must be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

00000010 (H'02') Write slave address by software only. All devices which obtain the programmable part of their address by software (and which have been designed to respond to the general call address) will enter a mode in which they can be programmed. The device will not reset.

I²C Bus Specification

An example of a data transfer of a programming master is shown in Figure 12 (ABCD represents the fixed part of the address).

00000100 (H'04') Write slave address by hardware only. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two-byte sequence. The device will not reset.

00000000 (H'00') This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore these codes.

When B is a one, the two-byte sequence is a hardware general call. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master does not know in advance to which device the message must be transferred, it can only generate this hardware general call and its own address, thereby identifying itself to the system (Figure 13).

The seven bits remaining in the second byte contain the device address of the hardware master. This address is recognized by an intelligent device, such as a microcomputer, connected to the bus which will then direct the information coming from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems an alternative could be that the hardware master transmitter is brought in the slave receiver mode after the system reset. In this way, a system configuring master can tell the hardware master transmitter (which is now in slave receiver mode) to which address data must be sent (Figure 14). After this programming procedure, the hardware master remains in the master transmitter mode.

Start Byte

Microcomputers can be connected to the I²C bus in two ways. If an on-chip hardware I²C bus interface is present, the microcomputer can be programmed to be interrupted only by requests from the bus. When the device possesses no such interface, it must constantly monitor the bus via software. Obviously, the more times the microcomputer monitors, or polls, the bus, the less time it can spend carrying out its intended function.

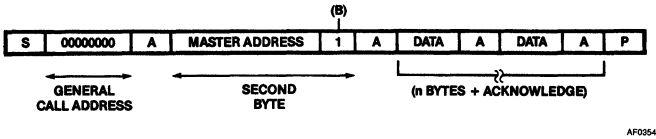


Figure 13. Data Transfer From Hardware Master Transmitter

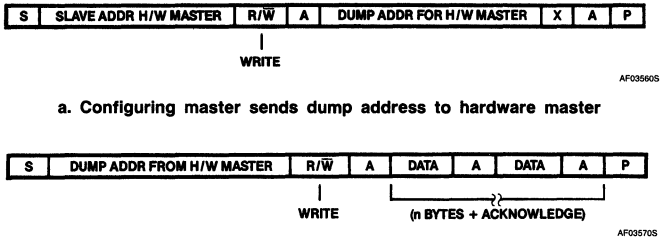


Figure 14. Data Transfer of Hardware Master Transmitter Capable of Dumping Data Directly to Slave Devices

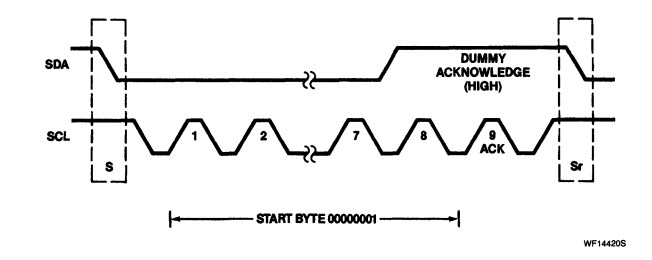


Figure 15. Start Byte Procedure

Therefore, there is a difference in speed between fast hardware devices and the relatively slow microcomputer which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Figure 15). The start procedure consists of:

a) A start condition, (S)
b) A start byte 00000001
c) An acknowledge clock pulse
d) A repeated start condition, (Sr)

After the start condition (S) has been transmitted by a master requiring bus access, the start byte (00000001) is transmitted. Another microcomputer can therefore sample the SDA line on a low sampling rate until one of the seven zeros in the start byte is detected. After detection of this Low level on the SDA line, the microcomputer is then able to switch to a higher sampling rate in order to find the second start condition (Sr) which is then used for synchronization.

A hardware receiver will reset at the reception of the second start condition (Sr) and will therefore ignore the start byte.

After the start byte, an acknowledge-related clock pulse is generated. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the start byte.

I²C Bus Specification

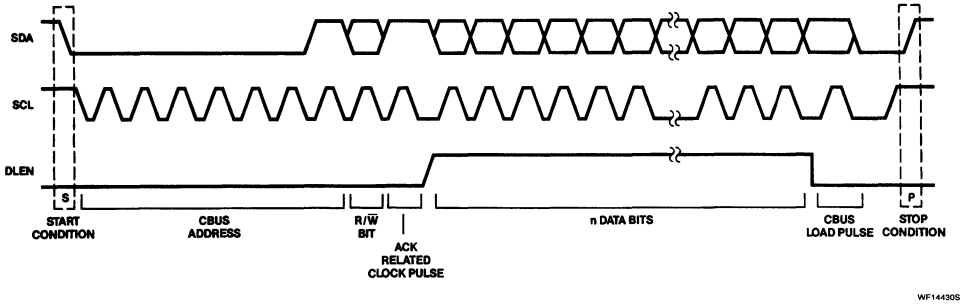


Figure 16. Data Format of Transmissions With CBUS Receiver/Transmitter

CBUS Compatibility

Existing CBUS receivers can be connected to the I²C bus. In this case, a third line called DLEN has to be connected and the acknowledge bit omitted. Normally, I²C transmissions are multiples of 8-bit bytes; however, CBUS devices have different formats.

In a mixed bus structure, I²C devices are not allowed to respond on the CBUS message. For this reason, a special CBUS address (0000001X) has been reserved. No I²C device will respond to this address. After the transmission of the CBUS address, the DLEN line can be made active and transmission, according to the CBUS format, can be performed (Figure 16).

After the stop condition, all devices are again ready to accept data.

Master transmitters are allowed to generate CBUS formats after having sent the CBUS address. Such a transmission is terminated by a stop condition, recognized by all devices. In the low speed mode, full 8-bit bytes must always be transmitted and the timing of the DLEN signal adapted.

If the CBUS configuration is known and no expansion with CBUS devices is foreseen, the user is allowed to adapt the hold time to the specific requirements of device(s) used.

ELECTRICAL SPECIFICATIONS OF INPUTS AND OUTPUTS OF I²C DEVICES

The I²C bus allows communication between devices made in different technologies which might also use different supply voltages.

For devices with fixed input levels, operating on a supply voltage of +5V ± 10%, the following levels have been defined:

V_{ILmax} = 1.5V (maximum input Low voltage)

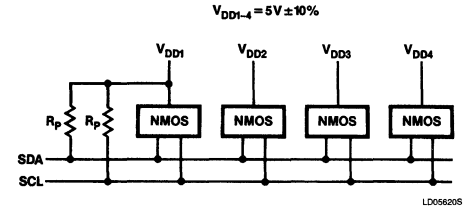


Figure 17. Fixed Input Level Devices Connected to the I²C Bus

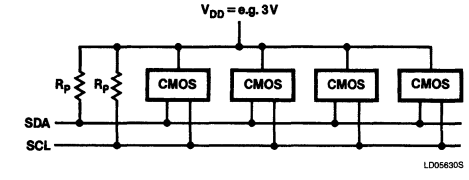


Figure 18. Devices With a Wide Range of Supply Voltages Connected to the I²C Bus

V_{IHmin} = 3V (minimum input High voltage)

Devices operating on a fixed supply voltage different from +5V (e.g. I²L), must also have these input levels of 1.5V and 3V for V_{IL} and V_{IH}, respectively.

For devices operating over a wide range of supply voltages (e.g. CMOS), the following levels have been defined:

V_{ILmax} = 0.3V_{DD} (maximum input Low voltage)

V_{IHmin} = 0.7V_{DD} (minimum input High voltage)

For both groups of devices, the maximum output Low value has been defined:

V_{OLmax} = 0.4V (max. output voltage Low) at 3mA sink current

The maximum low-level input current at V_{OLmax} of both the SDA pin and the SCL pin of an I²C device is −10μA, including the leakage current of a possible output stage.

The maximum high-level input current at 0.9V_{DD} of both the SDA pin and SCL pin of an I²C device is 10μA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA pin and the SCL pin of an I²C device is 10pF.

Devices with fixed input levels can each have their own power supply of +5V ± 10%. Pull-up resistors can be connected to any supply (see Figure 17).

However, the devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (see Figure 18).

I²C Bus Specification

When devices with fixed input levels are mixed with devices with V_{DD}-related levels, the latter devices have to be connected to one common supply line of +5V ± 10% along with the pull-up resistors (Figure 19).

Input levels are defined in such a way that:

1. The noise margin on the Low level is 0.1 V_{DD}.
2. The noise margin on the High level is 0.2 V_{DD}.
3. Series resistors (R_S) up to 300Ω can be used for flash-over protection against high voltage spikes on the SDA and SCL line (due to flash-over of a TV picture tube, for example) (Figure 20).

The maximum bus capacitance per wire is 400pF. This includes the capacitance of the wire itself and the capacitance of the pins connected to it.

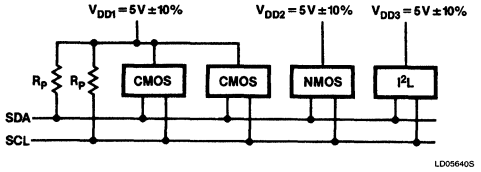


Figure 19. Devices With V_{DD} Related Levels Mixed With Fixed Input Level Devices on the I²C Bus

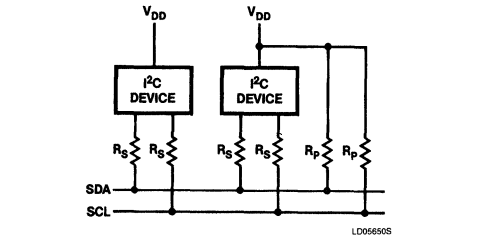


Figure 20. Serial Resistors (R_S) for Protection Against High Voltage

TIMING

The clock on the I²C bus has a minimum Low period of 4.7μs and a minimum High period of 4μs. Masters in this mode can generate a bus clock with a frequency from 0 to 100kHz.

All devices connected to the bus must be able to follow transfers with frequencies up to 100kHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch the Low periods. In the latter case the frequency is reduced.

Figure 21 shows the timing requirements in detail. A description of the abbreviations used is shown in Table 2. All timing references are at V_{ILmax} and V_{ILmin}.

LOW-SPEED MODE

As explained previously, there is a difference in speed on the I²C bus between fast hardware devices and the relatively slow microcomputer which relies on software polling. For this reason a low speed mode is available on the I²C bus to allow these microcomputers to poll the bus less often.

Start and Stop Conditions

In the low-speed mode, data transfer is preceded by the start procedure.

Data Format and Timing

The bus clock in this mode has a Low period of 130μs ± 25μs and a High period of 390μs ± 25μs, resulting in a clock frequency of approx. 2kHz. The duty cycle of the clock has this Low-to-High ratio to allow for more efficient use of microcomputers without an on-chip hardware I²C bus interface. In this mode also, data transfer with acknowledge is obligatory. The maximum number of bytes transferred is not limited (Figure 22).

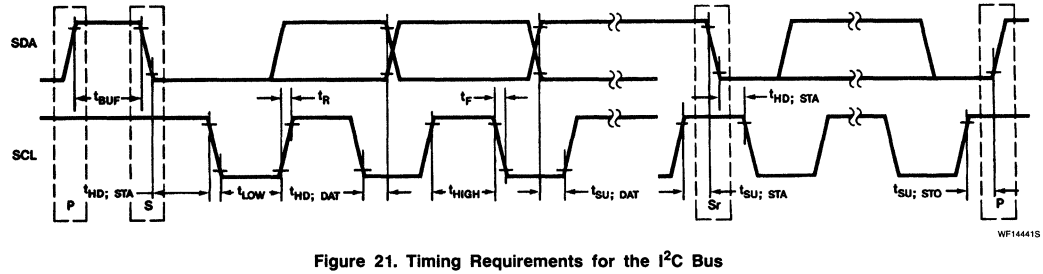


Figure 21. Timing Requirements for the I²C Bus

I²C Bus Specification

Table 2. Timing Requirement for the I²C Bus

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
f_{SCL}	SCL clock frequency	0	100	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		μs
$t_{HD;\ STA}$	Hold time start condition. After this period the first clock pulse is generated	4		μs
t_{LOW}	The Low period of the clock	4.7		μs
t_{HIGH}	The High period of the clock	4		μs
$t_{SU,\ STA}$	Setup time for start condition (Only relevant for a repeated start condition)	4.7		μs
$t_{HD,\ DAT}$	Hold time DATA for CBUS compatible masters for I²C devices	 5 0*		 μs μs
$t_{SU,\ DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	μs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;\ STO}$	Setup time for stop condition	4.7		μs

NOTES:
All values referenced to V_{IH} and V_{IL} levels.
* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.

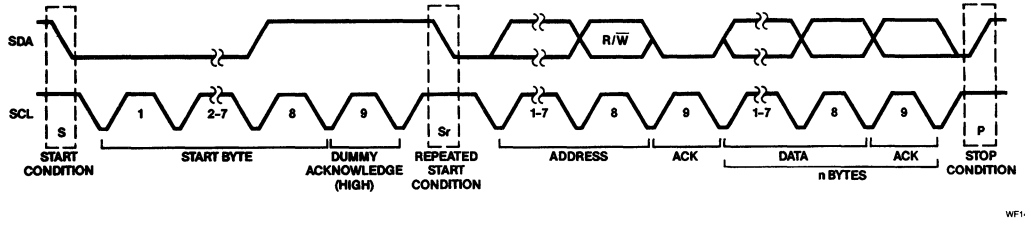


Figure 22. Data Transfer Low-Speed Mode

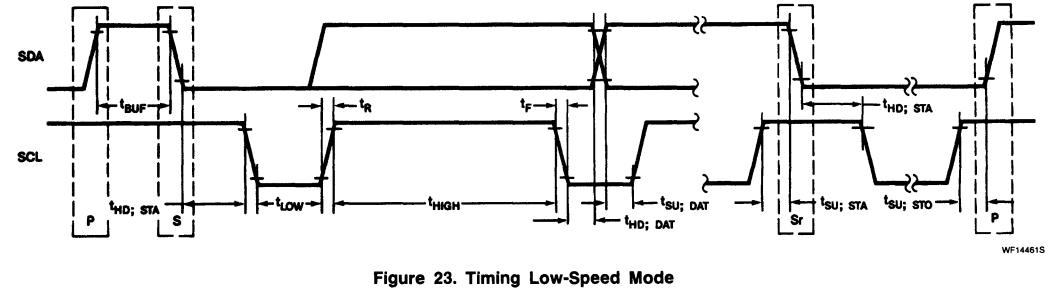


Figure 23. Timing Low-Speed Mode

I²C Bus Specification

LOW SPEED MODE

CLOCK	: $t_{LOW} = 130\mu s \pm 25\mu s$
DUTY CYCLE	: $t_{HIGH} = 390\mu s \pm 25\mu s$
	: 1:3 Low-to-High (Duty cycle of clock generator)
START BYTE	: 0000 0001
MAX. NO. OF BYTES	: UNRESTRICTED
PREMATURE TERMINATION OF TRANSFER	: NOT ALLOWED
ACKNOWLEDGE CLOCK BIT	: ALWAYS PROVIDED
ACKNOWLEDGEMENT OF SLAVES	: OBLIGATORY

In this mode, a transfer cannot be terminated during the transmission of a byte.

The bus is considered busy after the first start condition It is considered free again one minimum clock Low period, 105μs, after the detection of the stop condition. Figure 23 shows the timing requirements in detail, Table 3 explains the abbreviations.

Table 3. Timing Low Speed Mode

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{BUF}	Time the bus must be free before a new transmission can start	105		μs
$t_{HD;\ STA}$	Hold time start condition. After this period the first clock pulse is generated	365		μs
$t_{HD;\ STA}$	Hold time (repeated start condition only)	210		μs
t_{LOW}	The Low period of the clock	105	155	μs
t_{HIGH}	The High period of the clock	365	415	μs
$t_{SU,\ STA}$	Setup time for start condition (Only relevant for a repeated start condition)	105	155	μs
$t_{HD;\ DAT}$	Hold time DATA for CBUS compatible masters for I²C devices	 5 0*		 μs μs
$t_{SU,\ DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	μs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;\ STO}$	Setup time for stop condition	105	155	μs

NOTES:
All values referenced to V_{IH} and V_{IL} levels
* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.

I²C Bus Specification

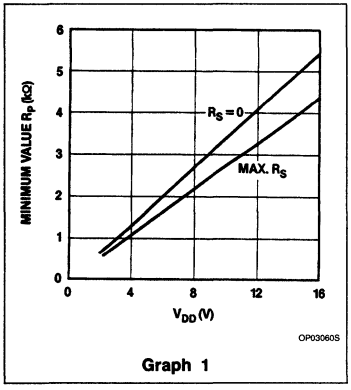
APPENDIX A

Maximum and minimum values of the pull-up resistors R_P and series resistors R_S (See Figure 20).

In a I²C bus system these values depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices (input current + leakage current)

1) The supply voltage limits the minimum value of the R_P resistor due to the specified 3mA as minimum sink current of the output stages, at 0.4V as maximum low voltage. In Graph 1, V_{DD} against R_{Pmin} is shown.

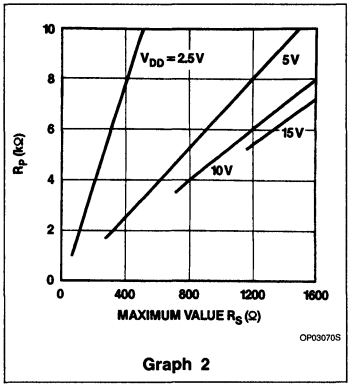


Graph 1

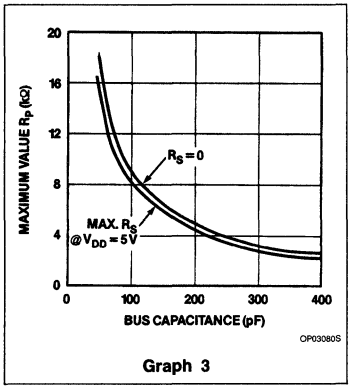
The desired noise margin of 0.1 V_{DD} for the low level limits the maximum value of R_S.

In Graph 2, R_{Smax} against R_P is shown.

2) The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of R_P because of the specified rise time of 1μs.



Graph 2

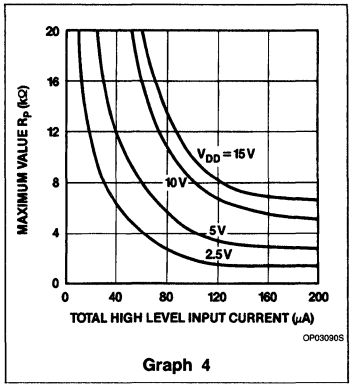


Graph 3

In Graph 3, the bus capacitance – R_{Pmax} relationship is shown.

3) The maximum high-level input current of each input/output connection has a specified value of 10μA max. Due to the desired noise margin of 0.2 V_{DD} for the high level, this input current limits the maximum value of R_P. This limit is dependent on V_{DD}.

In Graph 4 the total high-level input current – R_{Pmax} relationship is shown.



Graph 4

I²C LICENSE

Purchase of Signetics or Philips I²C components conveys a license under the Philips I²C patent rights to use these components in an I²C system, provided that the system conforms to the I²C standard specification as defined by Philips.

AN168

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

Linear Products

Application Note

Author: Carl Fenger

INTRODUCTION

The I^2C (Inter-IC) bus is becoming a popular concept which implements an innovative serial bus protocol that needs to be understood On the hardware level I^2C is a collection of microcomputers (MAB8400, PCD3343, 83C351, 84CXX) and peripherals (LCD/LED drivers, RAM, ROM, clock/timer, A/D, D/A, IR transcoder, I/O, DTMF generator, and various tuning circuits) that communicate serially over a two-wire bus, serial data (SDA) and serial clock (SCL). The I^2C structure is optimized for hardware simplicity. Parallel address and data buses inherent in conventional systems are replaced by a serial protocol that transmits both address and bidirectional data over a 2-line bus. This means that interconnecting wires are reduced to a minimum; only V_{CC}, ground and the two-wire bus are required to link the controller(s) with the peripherals or other controllers. This results in reduced chip size, pin count, and interconnections. An I^2C system is therefore smaller, simpler, and cheaper to implement than its parallel counterpart.

The data rate of the I^2C bus makes it suited for systems that do not require high speed. An I^2C controller is well suited for use in systems such as television controllers, telephone sets, appliances, displays or applications involving human interface. Typically an I^2C system might be used in a control function where digitally-controllable elements are adjusted and monitored via a central processor.

The I^2C bus is an innovative hardware interface which provides the software designer the flexibility to create a truly multi-master environment. Built into the serial interface of the controllers are status registers which monitor all possible bus conditions: bus free/busy, bus contention, slave acknowledgement, and bus interference. Thus an I^2C system might include several controllers on the same bus each with the ability to asynchronously communicate with peripherals or each other. This provision also provides expandability for future add-on controllers. (The I^2C system is also ideal for use in environments where the bus is subject to noise. Distorted transmissions are immediately detected by the hardware and the information presented to the software.) A slave acknowledgement on every byte also facilitates data integrity.

An I^2C system can be as simple or sophisticated as the operating environment demands. Whether in a single master or multi-master system, noisy or 'safe', correct system operation can be insured under software control.

CONTROLLERS

Currently the family of I^2C controllers include the MAB8400, and the PCD 3343 (the PCD3343 is basically a CMOS version of the MAB8400). The MAB8400 is based on the 8048 architecture with the I^2C interface built-in. The instruction set for the MAB8400 is similar to the 8048, with a few instructions added and a few deleted. Tables 1 and 2 summarize the differences.

Programs for the MAB8400 and PCD 3343 may be assembled on an 8048-assembler using the macros listed in Appendix A. The serial I/O instructions involve moving data to and from the S0, S1, and S2 serial I/O control registers. The block diagram of the I^2C interface is shown in Figure 1.

SERIAL I/O INTERFACE

A block diagram of the Serial Input/Output (SIO) is shown in Figure 1. The clock line of the serial bus (SCL) has exclusive use of Pin 3, while the Serial Data (SDA) line shares Pin 2 with parallel I/O signal P23 of port 2. Consequently, only three I/O lines are available for port 2 when the I^2C interface is enabled.

Communication between the microcomputer and interface takes place via the internal bus of the microcomputer and the Serial Interrupt Request line Four registers are used to store data and information controlling the operation of the interface:

- data shift register S0
- address register S0'
- status register S1
- clock control register S2.

THE I^2C BUS INTERFACE: SERIAL CONTROL REGISTERS S0, S1

All serial I^2C transfers occur between the accumulator and register S0. The I^2C hardware takes care of clocking out/in the data, and receiving/generating an acknowledge. In addition, the state of the I^2C bus is controlled and monitored via the bus control register S1 A definition of the registers is as follows:

Data Shift Register S0 — S0 is the data shift register used to perform the conversion between serial and parallel data format. All transmissions or receptions take place through register S0 MSB first. All I^2C bus receptions or transmissions involve moving data to/from the accumulator from/to S0.

Table 1. MAB8400 Family Instructions not in the MAB8048 Instruction Set

SERIAL I/O	REGISTER	CONTROL	CONDITIONAL BRANCH

MOV A,Sn
MOV Sn,A
MOV Sn,#data
EN SI
DIS SI
	DEC @Rr
	DJNZ @Rr,addr
		SEL MB2
		SEL MB3
			JNTF addr

Table 2. MAB8048 Instructions not in the MAB8400 Family Instruction Set

DATA MOVES	FLAGS	BRANCH	CONTROL

MOVX A,@R
MOVX @R,A
MOVP3 A,@A
MOVD A,P
MPVD P,A
ANLD P,A
ORLD P,A
	CLR F0
	CPL F0
	CLR F1
	CPL F1
		*JNI addr
		JF0 addr
		JF1 addr
		
		*replaced by
		JT0, JNT0
			ENTOCLK

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

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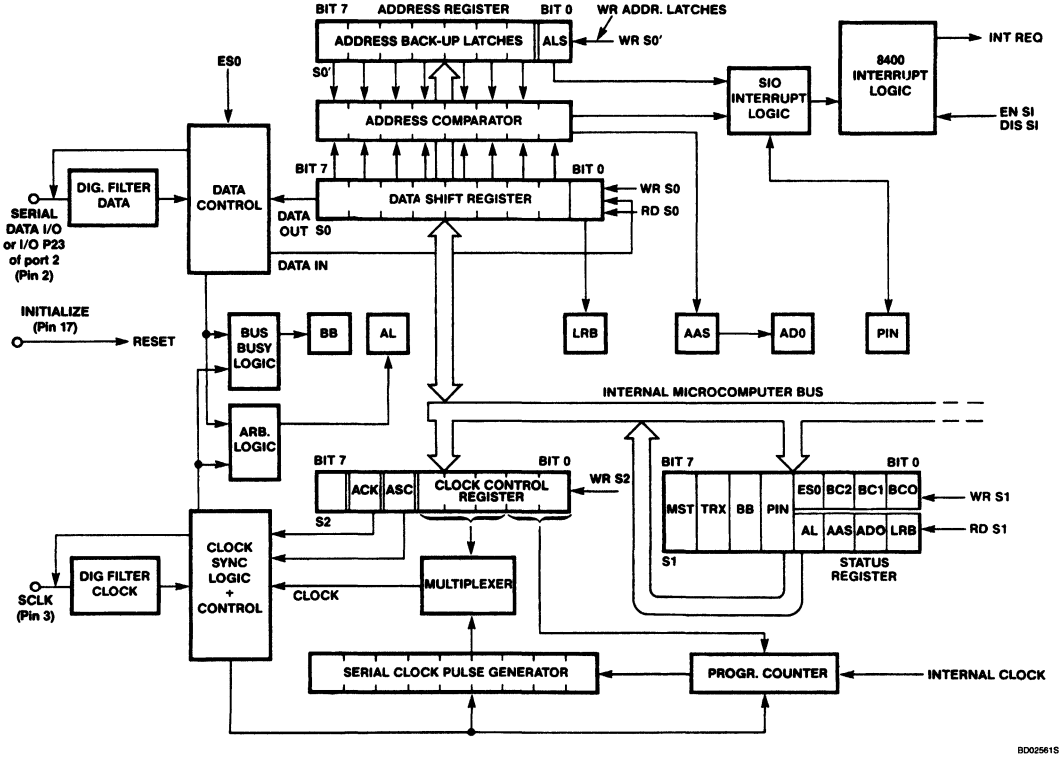

Figure 1. Block Diagram of the MAB8400 SIO Interface

Address Register S0′ — In multi-master systems, this register is loaded with a controller's slave address. When activated, (ALS = 0), the hardware will recognize when it is being addressed by setting the AAS (Addressed As Slave) flag. This provision allows a master to be treated as a slave by other masters on the bus.

Status Register S1 — S1 is the bus status register. To control the SIO interface, information is written to the register. The lower 4 bits in S1 serve dual purposes; when written to, the control bits ES0, BC2, BC1, BC0 are programmed (Enable Serial Output and a 3-bit counter which indicates the current number of bits left in a serial transfer). When reading the lower four bits, we obtain the status information AL, AAS, AD0, LRB (Arbitration Lost, Addressed As Slave, Address Zero (the general call has been received), the Last Received Bit (usually the acknowledge bit)). The upper 4 bits are the MST, TRX, BB, and PIN control bits (Master, Transmitter, Bus Busy, and Pending Interrupt Not). These bits define what role the controller has at any particular time. The values of the master and transmitter bits define the controller as either a master or slave (a master initiates a transfer and generates the serial clock; a slave does not), and as a transmitter or receiver. Bus Busy keeps track of whether the bus is free or not, and is set and reset by the 'Start' and 'Stop' conditions which will be defined. Pending Interrupt Not is reset after the completion of a byte transfer + acknowledge, and can be polled to indicate when a serial transfer has been completed. An alternative to polling the PIN bit is to enable the serial interrupt; upon completion of a byte transfer, an interrupt will vector program control to location 07H.

SERIAL CLOCK/ACKNOWLEDGE CONTROL REGISTER S2

Register S2 contains the clock-control register and acknowledge mode bit. Bits S20 – S24 program the bus clock speed. Bit S26 programs the acknowledge or not-acknowledge mode (1/0). The various I^2C bus clock speed possibilities are shown in Table 3.

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Table 3. Clock Pulse Frequency Control When Using a 4.43MHz Crystal

HEX S20 – S24 CODE	DIVISOR	APPROX. f_{CLOCK} (kHz)
0	Not Allowed	
1	39	114
2	45	98
3	51	87
4	63	70
5	75	59
6	87	51
7	99	45
8	123	36
9	147	30
A	171	26
B	195	23
C	243	18
D	291	15
E	339	13
F	387	11
10	483	9.2
11	579	7.7
12	675	6.6
13	771	5.8
14	963	4.6
15	1155	3.8
16	1347	3.3
17	1539	2.9
18*	1923	2.3
19*	2307	1.9
1A*	2691	1.7
1B*	3075	1.4
1C	3843	1.2
1D	4611	1.0
1E	5379	0.8
1F	6147	0.7

*only values that may be used in the low speed mode (ASC = 1)

These speeds represent the frequency of the serial clock bursts and do not reflect the speed of the processor's main clock (i.e. it controls the bus speed and has no effect on the CPU's execution speed).

BUS ARBITRATION

Due to the wire-AND configuration of the I^2C bus, and the self-synchronizing clock circuitry of I^2C masters, controllers with varying clock speeds can access the bus without clock contention. During arbitration, the resultant clock on the bus will have a low period equal to the longest of the low periods; the high period will equal the shortest of the high periods. Similarly, when two masters attempt to drive the data line simultaneously, the data is 'ANDed', the master generating a low while the other is driving a high will win arbitration. The resultant bus level will be low, and the loser will withdraw from the bus and set its 'Arbitration Lost' flag (S1 bit 3).

The losing Master is now configured as a slave which could be addressed during this very same cycle. These provisions allow for a number of microcomputers to exist on the same bus. With properly written subroutines, software for any one of the controllers may regard other masters as transparent.

I^2C PROTOCOL AND ASSEMBLY LANGUAGE EXAMPLES

I^2C data transfers follow a well-defined protocol. A transfer always takes place between a master and a slave. Currently a microcomputer can be master or slave, while the 'CLIPS' peripherals are always slaves. In a 'bus-free' condition, both SCL and SDA lines are kept logical high by external pull-up resistors. All bus transfers are bounded by a 'Start' and a 'Stop' condition. A 'Start' condition is defined as the SDA line making a high-to-low transition **while the SCL line is high.** At this point, the internal hardware on all slaves are activated and are prepared to clock-in the next 8 bits and interpret it as a 7-bit address and a R/$\overline{W}$ control bit (MSB first). All slaves have an internal address (most have 2 – 3 programmable address bits) which is then compared with the received address. The slave that recognized its address will respond by pulling the data line low during a ninth clock generated by the master (all I^2C byte transfers require the master to generate 8 clock pulses plus a ninth acknowledge-related clock pulse). The slave-acknowledge will be registered by the master as a '0' appearing in the LRB (Last Received Bit) position of the S1 serial I/O status register. If this bit is high after a transfer attempt, this indicates that a slave did not acknowledge, and that the transfer should be repeated.

After the desired slave has acknowledged its address, it is ready to either send or receive data in response to the master's driving clock. All other slaves have withdrawn from the bus. In addition, for multi-master systems, the start condition has set the 'Bus Busy' bit of the serial I/O register S1 on all masters on the bus. This gives a software indication to other masters that the bus is in use and to wait until the bus is free before attempting an access.

There are two types of I^2C peripherals that now must be defined: there are those with only a chip address such as the I/O expander, PCF8574, and those with a chip address plus an internal address such as the static RAM, PCF8570. Thus after sending a start condition, address, and R/$\overline{W}$ bit, we must take into account what type of slave is being addressed. In the case of a slave with only a chip address, we have already indicated its address and data direction (R/$\overline{W}$) and are therefore ready to send or receive data. This is performed by the master generating bursts of 9 clock pulses for each byte that is sent or received. The transaction for writing one byte to a slave with a chip address only is shown in Figure 3.

In this transfer, all bus activity is invoked by writing the appropriate control byte to the serial I/O control register S1, and by moving data to/from the serial bus buffer register S0. Coming from a known state (MOV S1,#18H-Slave, Receiver, Bus not Busy) we first load the serial I/O buffer S0 with the desired

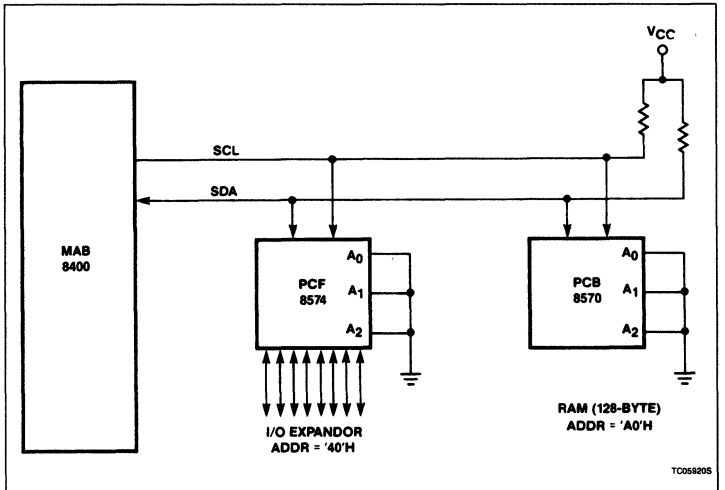

Figure 2. Schematic for Assembly Examples

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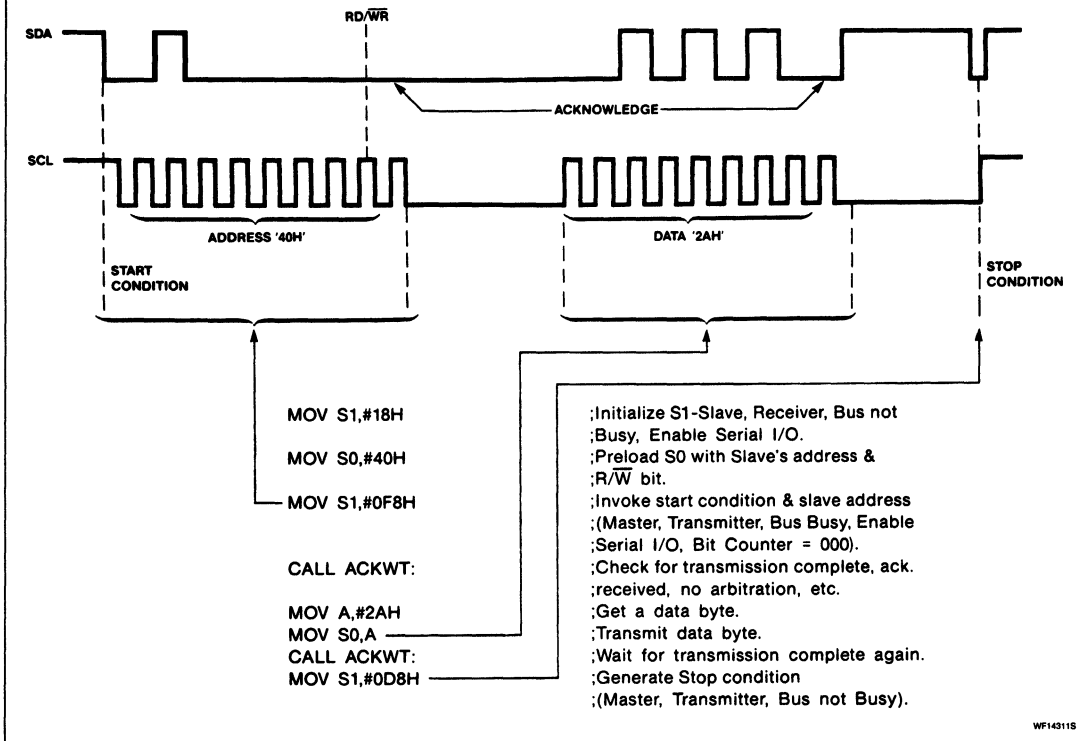

Figure 3

slave's address (MOV S0,#40H). To transmit this preceded by a start condition, we must first examine the control register S1, which, after initialization, looks like this:

MAS-TER	TRANS	BUS BUSY	PIN	ESO	BC2	BC1	BC0
0	0	0	1	1	0	0	0

To transmit to a slave, the Master, Transmitter, Bus Busy, PIN (Pending Interrupt Not), and ESO (Enable Serial Output) must be set to a 1. This results in an 'F8H' being written to S1. This word defines the controller as a Master Transmitter, invokes the transfer by setting the 'Bus Busy' bit, clears the Pending Interrupt Not (an inverted flag indicating the completion of a complete byte transfer), and activates the serial output logic by setting the Enable Serial Output (ESO) bit.

BIT COUNTER S12, S11, S10

BC2, BC1, and BC0 comprise a bit-counter which indicates to the logic how long the word is to be clocked out over the serial data line. By setting this to a 000H, we are telling it to produce 9 clocks (8 bits plus an acknowledge clock) for this transfer. The bit counter will then count off each bit as it is transmitted. The bit counter possibilities are shown in Table 4.

Thus the bit counter keeps track of the number of clock pulses remaining in a serial transfer. Additionally, there is a not-acknowledge mode (controlled through bit 6 of clock control register S2) which inhibits the acknowledge clock pulse, allowing the possibility of straight serial transfer. We may thus define the word size for a serial transfer (by preloading BC2, BC1, BC0 with the appropriate control number), with or without an acknowledge-related clock pulse being generated. This makes the controller able to transmit serial data to most any serial device regardless of its protocol (e.g., C-bus devices).

CHECKING FOR SLAVE ACKNOWLEDGE

After a 'Start' condition and address have been issued, the selected slave will have recognized and acknowledged its address by

Table 4. Binary Numbers in Bit-Count Locations BC2, BC1 and BC0

BC2	BC1	BC0	BITS/BYTE WITHOUT ACK	BITS/BYTE WITH ACK
0	0	1	1	2
0	1	0	2	3
0	1	1	3	4
1	0	0	4	5
1	0	1	5	6
1	1	0	6	7
1	1	1	7	8
0	0	0	8	9

pulling the data line low during the ninth clock pulse. During this period, the software (which runs on the processor's 4MHz clock) will have been either waiting for the transfer to be completed by polling the PIN bit in S1 which goes low on completion of a transfer/reception (whose length is defined by the preloaded Bit-counter value), or by the hardware in Serial Interrupt mode. The serial interrupt (vectored to 07H) is enabled via the EN SI (enable serial interrupt) instruction.

At the point when PIN goes low (or the serial interrupt is received) the 9-bit transfer has been completed. The acknowledgement bit will now be in the LRB position of register S1, and may be checked in the routine 'ACKWT' (Wait for Acknowledge) as shown in Figure 4.

This routing must go one step further in multimaster systems; the possibility of an Arbitration Lost situation may occur if other masters are present on the bus. This condition may be detected by checking the 'AL' bit (bit 3). If arbitration has been lost, provisions for reattempting the transmission should be taken. If arbitration is lost, there is the possibility that the controller is being addressed as a Slave. If this condition is to be recognized, we must test on the 'AAS' bit (bit 2). A 'General Call' address (00H) has also been defined as an 'all-call' address for all slaves; bit 1, AD0, must be tested if this feature is to be recognized by a Master.

After a successful address transfer/acknowledge, the slave is ready to be sent its data. The instruction MOV SO,A will now automatically send the contents of the accumulator out on the bus. After calling the ACKWT routine once more, we are ready to terminate the transfer. The Stop condition is created by the instruction 'MOV S1, #0D8H'. This resets the bus-busy bit, which tells the hardware to generate a Stop — the data line makes a low-to-high transition while the clock remains high. All bus-busy flags on other masters on the bus are reset by this signal.

The transfer is now complete — PCF8574 I/O Expandor will transfer the serial data stream to its 8 output pins and latch them until further update.

```
ACKWT:  MOV A,S1        ;Get bus status word
                        ;from S1.
        JB4 ACKWT       ;Poll the PIN bit
                        ;until it goes low
                        ;indicating transfer
                        ;completed
        JBO BUSERR      ;Jump to BUSERR
                        ;routine if acknowledge
                        ;not received.
        RET             ;transfer complete,
                        ;acknowledge received - return.
```

Figure 4

MASTER READS ONE BYTE FROM SLAVE

A read operation is a similar process; the address, however, will be 41H, the LSB indicating to the I/O device that a read is to be performed. During the data portion of a read, the I/O port 8574 will transmit the contents of its latches in response to the clock generated by the master. The Master/Receiver in this case generates a low-level acknowledge on reception of each byte (a 'positive' acknowledge). Upon completion of a read, the master must generate a 'negative' acknowledge during the ninth clock to indicate to the slaves that the read operation is finished. This is necessary because an arbitrary number of bytes may be read within the same transfer. A negative acknowledge consists of a high signal on the data line during the ninth clock of the last byte to be read. To accomplish this, the master 8400 must leave the acknowledge mode just before the final byte, read the final byte (producing only 8 clock pulses), program the bit-counter with 001 (preparing for a one-bit negative acknowledge pulse), and simply move the contents of S0 to the accumulator. This final instruction accomplishes two things simultaneously: it transfers the final byte to the accumulator and produces one clock pulse on the SCL line. The structure of the serial I/O register S0 is such that a read from it causes a double-buffered transfer from the I^2C bus to S0, while the original contents of S0 are transferred to the accumulator. Because the number of clocks produced on the bus is determined by the control number in the Bit Counter, by presetting it to 001, only one clock is generated. At this point in time the slave is still waiting for an acknowledge; the bus is high due to the pull-up, as single clock pulse in this condition is interpreted as a 'negative' acknowledge. The slave has now been informed that reading is completed; a Stop condition is now generated as before. The read process (one byte from a slave with only a chip address) is shown in Figure 5.

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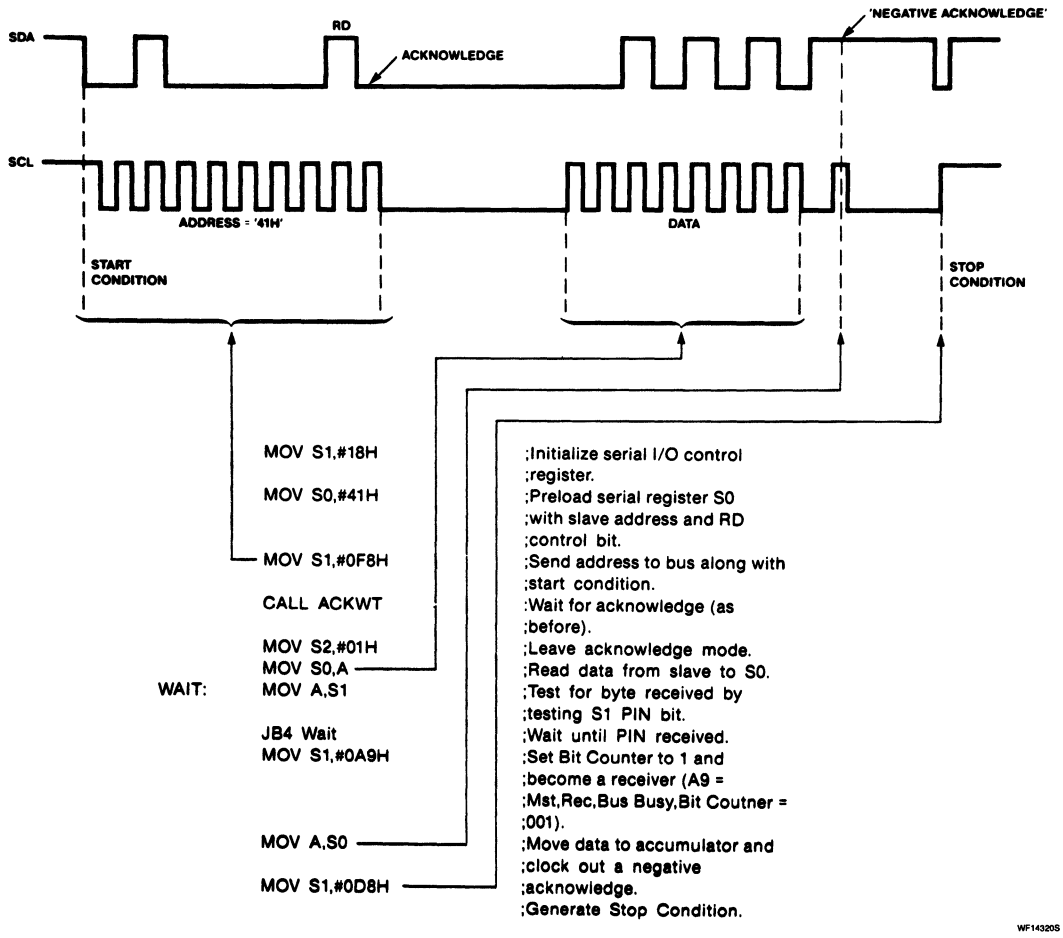

Figure 5

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

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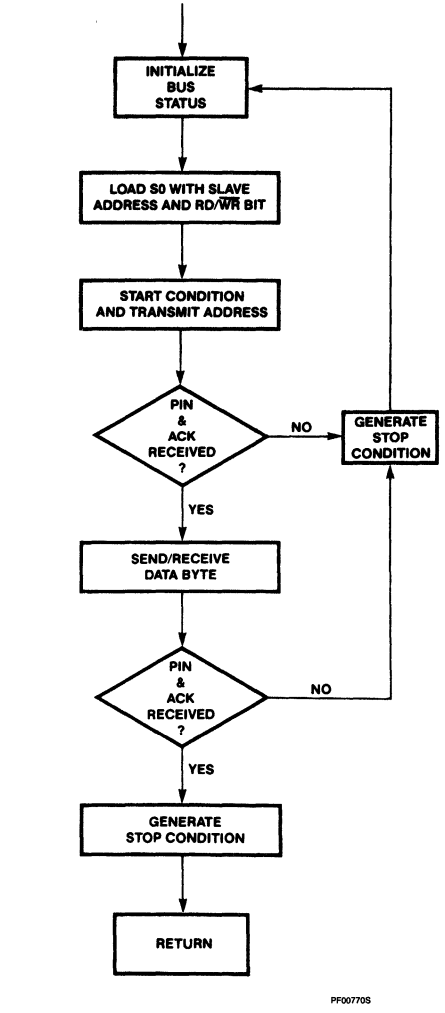

Figure 6. Flowchart for Reading/Writing One Byte to an I^2C Peripheral; Single-Master, Single-Address Slave

```
        MOV S1, #18H      ;Initialize bus-status register
                          ;Master, Transmitter,
                          ;Bus-not-Busy, Enable SIO.
        MOV S0, #0A0H     ;Load S0 with RAM's chip
                          ;address.
        MOV S1, #0F8H     ;Start cond. and transmit
                          ;address.
        CALL ACKWT        ;Wait until address received.
        MOV A,#00H        ;Set up for transmitting RAM
                          ;location address.
        MOV S0,A          ;Transmit first RAM address.
        CALL ACKWT        ;Wait.
        MOV S1, #18H      ;Set up for a repeated Start
                          ;condition.
        MOV A,#0A1H       ;Get RAM chip address & RD bit.
        MOV S0,A          ;Send out to bus
        MOV S1,#0F8H      ;preceded by repeated Start.

        CALL ACKWT        ;Wait.
        MOV A,S0          ;First data byte to S0.
        CALL ACKWT        ;Wait
        MOV A,S0          ;Second data byte to S0.
                          ;And First data byte to Acc.
        CALL ACKWT        ;Wait.
        MOV R0,A          ;Save first byte in R0.
        MOV A,S0          ;Third data byte to S0
                          ;and second data byte to Acc.
        CALL ACKWT        ;Wait.
        MOV R1,A          ;Save second data byte
                          ;in R1.
        MOV S2,#01H       ;Leave ack. mode.
                          ;Bit Counter=001 for neg ack.
        MOV A,S0          ;Third data byte to acc
                          ;negative ack. generated.
        MOV R2,A          ;Save third data byte in R2.
WAIT1:  MOV A,S1          ;Get bus status.
        JB4 WAIT1         ;Wait until transfer complete.
        MOV S1,#0D8H      ;Stop condition.
        MOV S2,#41H       ,Restore acknowledge mode.
```

DF05700S

Figure 7

These examples apply to a slave with a chip address — more than one byte can be written/read within the same transfer; however, this option is more applicable to I^2C devices with sub-addresses such as the static RAMs or Clock/Calendar. In the case of these types of devices, a slightly different protocol is used. The RAM, for example, requires a chip address and an internal memory location before it can deliver or accept a byte of information. During a write operation, this is done by simply writing the secondary address right after the chip address — the peripheral is designed to interpret the second byte as an internal address. In the case of a Read operation, the slave peripheral must send data back to the Master after it has been addressed and sub-addressed. To accomplish this, first the Start, Address, and Sub-address is transmitted. Then we have a **repeated** start condition to reverse the direction of the data transfer, followed by the chip address and RD, then a data string (w/ acknowledges). This repeated Start does not affect other peripherals — they have been deactivated and will not reactivate until a Stop condition is detected. I^2C peripherals are equipped with auto-incrementing logic which will automatically transmit or receive data in consecutive (increasing) locations. For example, to read 3 consecutive bytes to PCB8571 RAM locations 00, 01 and 02, we use the following format as shown in Figure 7.

This routine reads the contents of location 00, 01 and 02 of the PCB8571 128-byte RAM and puts them in registers R0, R1, and R2. The auto-incrementing feature allows the programmer to indicate only a starting location, then read an arbitrary block of consecutive memory addresses. The WAIT 1 loop is required to poll for the completion of the final byte because the ACKWT routine will not recognize the negative acknowledge as a valid condition.

BUS ERROR CONDITIONS: ACKNOWLEDGE NOT RECEIVED

In the above routines, should a slave fail to acknowledge, the condition is detected during the 'ACKWT' routine. The occurrence may indicate one of two conditions: the slave has failed to operate, or a bus disturbance has occurred. The software response to either event is dependent on the system application. In either case, the 'BusErr' routine should reinitialize the bus by issuing a 'Stop' condition. Provision may then be taken to repeat the transfer an arbitrary number of times. Should the symptom persist, either an error condition will be entered, or a backup device can be activated.

These sample routines represent single-master systems. A more detailed analysis of multi-master/noisy environment systems will be treated in further application notes. Examples of more complex systems can be found in the 'Software Examples' manual; publication 9398 615 70011.

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APPENDIX A

Only the 8048 assembler is capable of assembling MAB8400 source code when it has at least a "DATA" or "Define Byte" assembler directive, possibly in combination with a MACRO facility.

The new instructions can be simply defined by MACROs. The instructions which are not in the MAB8400 should not be in the MAB8400 source program.

An example of a macro definitions list is given here for the Intel Macro Assembler.

This list can be copied in front of a MAB8400 source program; the new instructions are added to the MAB8400 source program by calling the MACRO via its name in the opcode field and (if required) followed by an operand in the operand field.

MACRO DEFINITIONS

```
LINE  SOURCE STATEMENT

    1 $MACROFILE
    2 ;MACROS FOR 8048 ASSEMBLER RECOGNITION
    3 ;OF 8400 COMMANDS
    4                   MOVS0A      MACRO       ;MOV S0,A
    5                   DB 3CH
    6                   ENDM
    7                   MOVAS0      MACRO       ;MOV A,S0
    8                   DB 0CH
    9                   ENDM
   10                   MOVS1A      MACRO       ;MOV S1,A
   11                   DB 3DH
   12                   ENDM
   13                   MOVAS1      MACRO       ;MOV A,S1
   14                   DB 0DH
   15                   ENDM
   16                   MOVS2A      MACRO       ;MOV S2,A
   17                   DB 3EH
   18                   ENDM
   19                   MOVS0       MACRO L     ;MOV S0,#DATA
   20                   DB 9CH,L
   21                   ENDM
   22                   MOVS1       MACRO L     ;MOV S1,#DATA
   23                   DB 9DH,L
   24                   ENDM
   25                   MOVS2       MACRO L     ;MOV S2,#DATA
   26                   DB 9EH,L
   27                   ENDM
   28                   ENSI        MACRO       ;EN SI
   29                   DB 85H
   30                   ENDM
   31                   DISSI       MACRO       ;DIS SI (Disable serial
                                                 interrupt)
   32                   DB          95H
   33                   ENDM
   34;
   35; PORT 0 INSTRUCTIONS:
   36;                  INAP0       MACRO       ;IN A,P0
   37                   DB          08H
   38                   ENDM
   39;
   40                   OUTP0A      MACRO       ;OUTL P0,A
   41                   DB          38H
   42                   ENDM
   43;
   44                   ORLP0       MACRO L     ;ORL P0,#DATA
   45                   DB          88H,L
   46                   ENDM
   47;
   48                   ANLP0       MACRO L     ;ANL P0,#DATA
   49                   DB          98H,L
   50                   ENDM
   51;
```

MACRO DEFINITIONS (Continued)

```
LINE    SOURCE STATEMENT

52; DATA MEMORY INSTRUCTIONS:
53                  DECARO      MACRO           ;DEC @R0
54                  DB          0C0H
55                  ENDM
56;
57                  DECAR1      MACRO           ;DEC @R1
58                  DB          OC1H
59                  ENDM
60;
61; SELECT MEMORY BANK INSTRUCTIONS:
62                  SELMB2      MACRO           ;SEL MB2
63                  DB          0A5H
64                  ENDM
65;
66                  SELMB3      MACRO           ;SEL MB3
67                  DB          0B5H
68                  ENDM
69;
70; CONDITIONAL JUMP INSTRUCTIONS:
71                  DJNZA0      MACRO L         ;DJNZ @R0,ADDR
72                  DB          0E0H,L AND 0FFH
73                  ENDM
74;
75                  DJNZA1      MACRO L         ;DJNZ @R1,ADDR
76                  DB          0E1H,L AND 0FFH
77                  ENDM
78;
79                  JNTF        MACRO L         ;JUMP IF TIMERFLAG IS
                                                 NON ZERO
80                  DB          06H,L AND 0FFH
81                  ENDM
82
83; END OF MACRO DEFINITIONS
```

THE 8400 INSTRUCTIONS BUILT FROM THE MACRO LIST

LOC/OBJ	LINE	SOURCE STATEMENT		
0000	1	ORG 0		
	2	MOVAS0		;MACRO for MOV A,S0
0000 0C	3 +	DB	0CH	
	4	MOVAS1		;MACRO for MOV A,S1
0001 0D	5 +	DB	0DH	
	6	MOVS0A		;MACRO for MOV S0,A
0002 3C	7 +	DB	3CH	
	8	MOVS1A		;MACRO For MOV S1,A
0003 3D	9 +	DB	3DH	
	10	MOVS2A		;MACRO For MOV S2,A
0004 3E	11 +	DB	3EH	
	12	MOVS0	56H	;MACRO For MOV S0, #56H
0005 9C	13 +	DB	9CH,56H	
0006 56				
	14	MOVS1	9FH	;MACRO for MOV S1, #9FH
0007 9D	15 +	DB	9DH,9FH	
0008 9F				
	16	MOVS2	0E8H	;MACRO for MOV S2, #0E8H
0009 9E	17 +	DB	9EH,0E8H	
000A E8				
	18	ENS1		;MACRO for EN S1
000B 85	19 +	DB	85H	
	20	DISSI		;MACRO for DIS SI
000C 95	21 +	DB	95H	
	22	INAP0		;MACRO for IN A,P0
000D 08	23 +	DB	08H	
	24	OUTP0A		;MACRO for OUTL P0,A
000E 38	25 +	DB	38H	
	26	ORLP0	5AH	;MACRO for ORL P0,A
000F 88	27 +	DB	88H,5AH	
0010 5A				
	28	ANLP0	2FH	;MACRO for ANL P0,A
0011 98	29 +	DB	98H,2FH	
0012 2F				
	30	DECAR0		;MACRO for DEC @R0
0013 C0	31 +	DB	0C0H	
	32	DECAR1		;MACRO for DEC @R1
0014 C1	33 +	DB	0C1H	
	34	SELMB2		;MACRO for SEL MB2
0015 A5	35 +	DB	0A5H	
	36	SELMB3		;MACRO for SEL MB3
0016 B5	37 +	DB	0B5H	
	38	DJNZA0	567H	;MACRO for DJNZ @R0, 567H
0017 E0	39 +	DB	0E0H,567H AND 0FFH	
0019 67				
	40	DJNZA1	0EFEH	;MACRO for DJNZ @R1, 0EFEH
0019 E1	41 +	DB	0E1H,0EFEH AND 0FFH	
001A FE				
	42	JNTF	789H	;MACRO for JNTF 789H
001B 06	43 +	DB	06H, 789H AND 0FFH	
001C 89				
	44	END		

Signetics

Linear Products

Section 4
RF Communications

4

INDEX

FREQUENCY SYNTHESIS

Synthesizers

PHASE-LOCKED LOOPS

COMPANDORS

NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

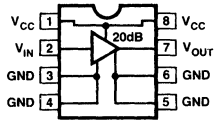
The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **Bandwidth (min.)**
  200 MHz, ±0.5dB
  350 MHz, −3dB
- **20dB insertion gain**
- **4.8dB (6dB) noise figure**
  Z_O = 75Ω (Z_O = 50Ω)
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD12760S

APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

ORDERING INFORMATION

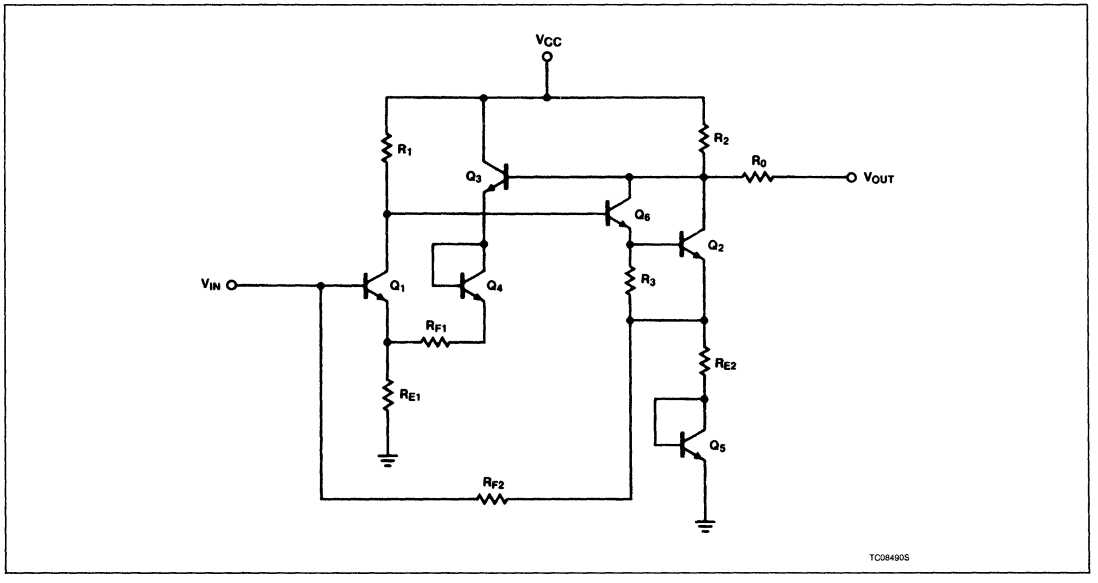
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade	 0 to +70 −40 to +85	 °C °C
P_{DMAX}	Maximum power dissipation[1, 2] T_A = 25°C (still-air) N package D package	 1160 780	 mW mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz, over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f = 100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm
t_R	Rise time			5		ps
	Propagation delay			5		ps

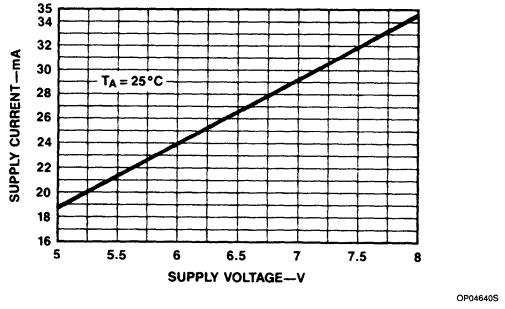


Figure 1. Supply Current vs Supply Voltage

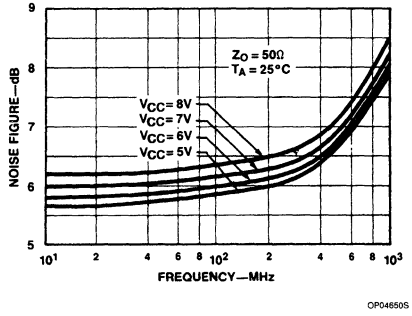


Figure 2. Noise Figure vs Frequency

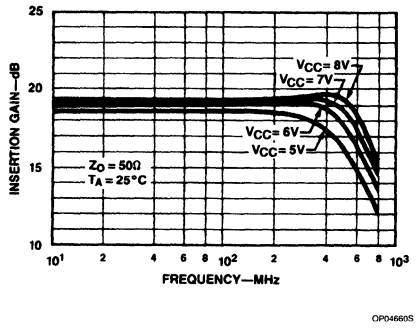


Figure 3. Insertion Gain vs Frequency (S_{21})

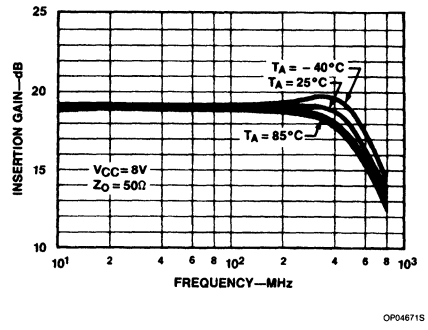


Figure 4. Insertion Gain vs Frequency (S_{21})

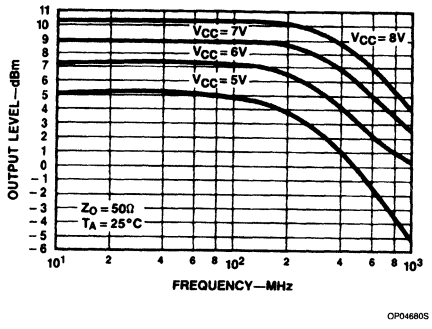


Figure 5. Saturated Output Power vs Frequency

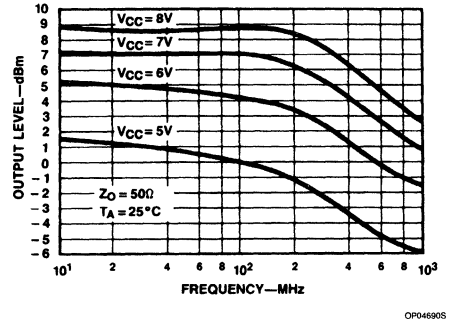


Figure 6. 1dB Gain Compression vs Frequency

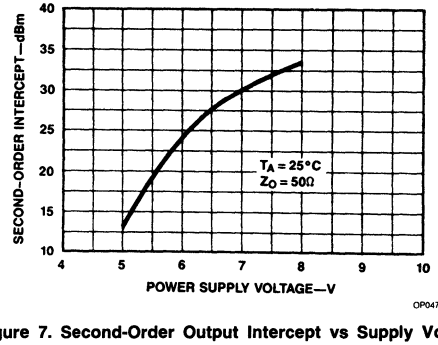


Figure 7. Second-Order Output Intercept vs Supply Voltage

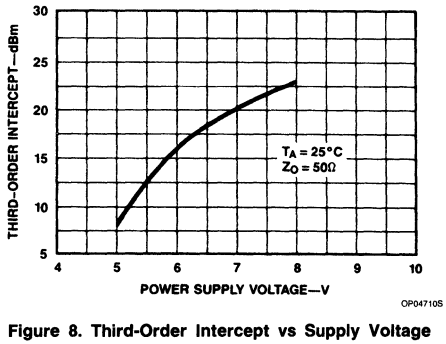


Figure 8. Third-Order Intercept vs Supply Voltage

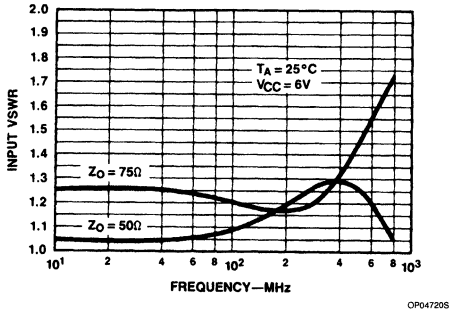


Figure 9. Input VSWR vs Frequency

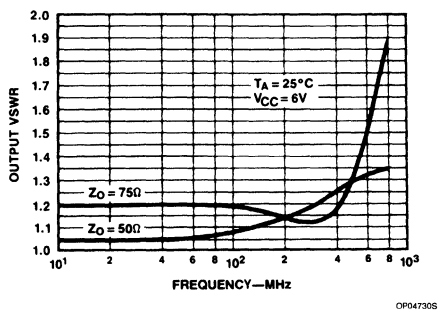


Figure 10. Output VSWR vs Frequency

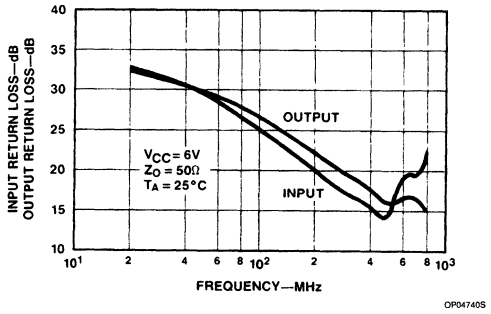


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

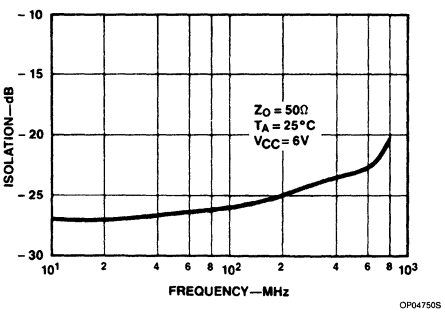


Figure 12. Isolation vs Frequency (S_{12})

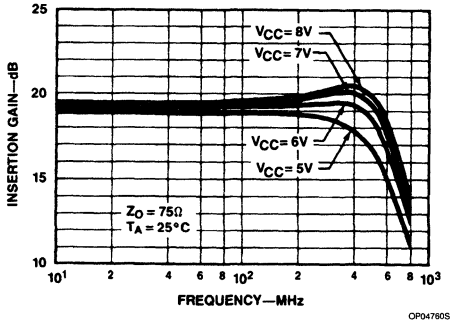


Figure 13. Insertion Gain vs Frequency (S_{21})

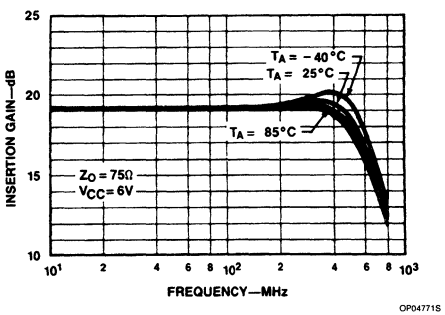


Figure 14. Insertion Gain vs Frequency (S_{21})

Wide-band High-Frequency Amplifier | NE/SA5204

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} \text{dB} \quad (2)$$

where $I_{C1} = 5.5\text{mA}$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26\text{mV}$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\,R_{E1} \quad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8\text{V}$, $I_{C1} = 5\text{mA}$ and $I_{C3} = 7\text{mA}$ (currents rated at $V_{CC} = 6\text{V}$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where $V_{CC} = 6\text{V}$, $R_2 = 225\Omega$, $I_{C2} = 7\text{mA}$ and $I_{C6} = 5\text{mA}$.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

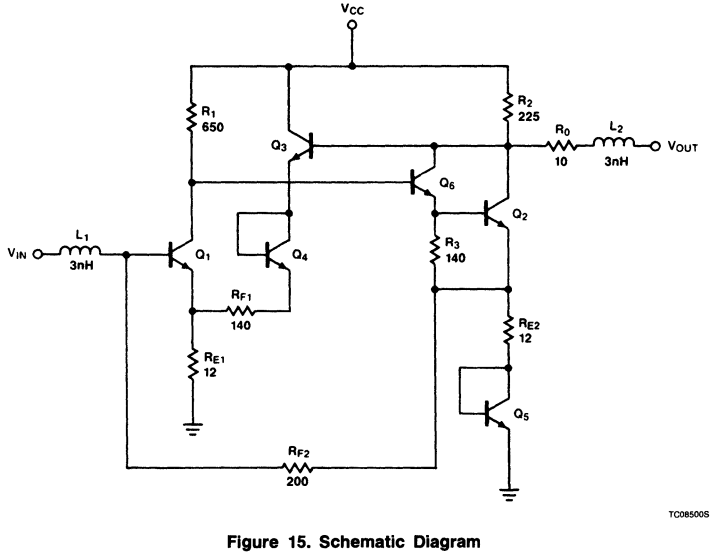


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

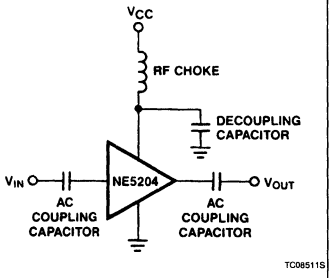
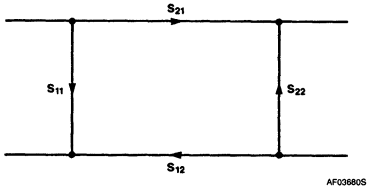


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

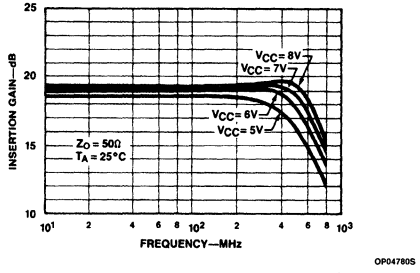
$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

b.

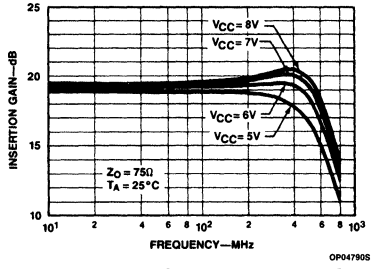
Figure 17

50Ω System

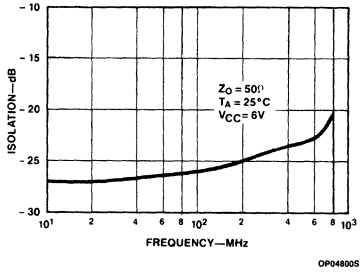


a. Insertion Gain vs Frequency (S_{21})

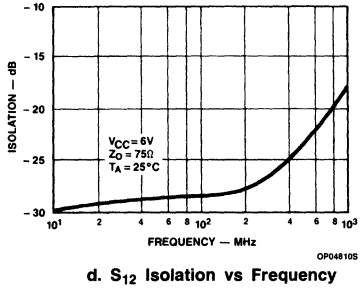
75Ω System



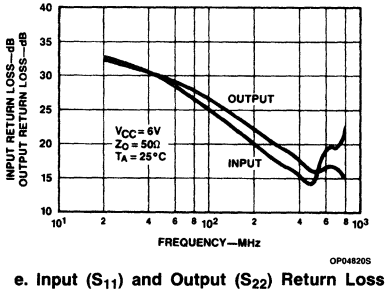
b. Insertion Gain vs Frequency (S_{21})



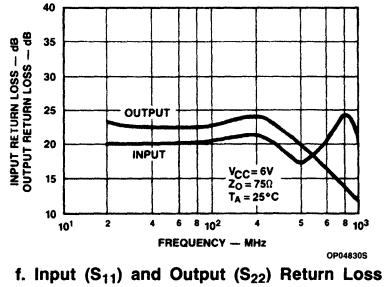
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

Actual S-parameter measurements, using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B), are shown in Figure 18.

Values for Figure 20 are measured and specified in the data sheet to ease adaptation and comparison of the NE5204 to other high-frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5204

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\text{NE5204}\ Z_D} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain
V_I = Insertion Voltage Gain

Measured value for the NE5204 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10\text{Log}\ |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20\text{Log}\ S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing-wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20\text{Log}\ |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20\text{Log}\ |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to non-linearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

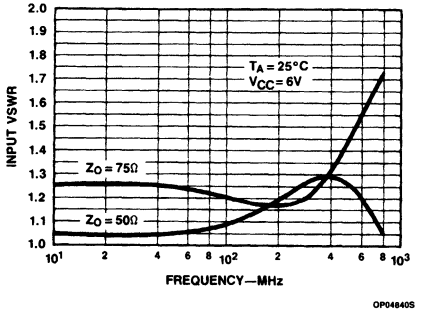
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second-order IMR is equal to the difference between the second-order intercept and the fundamental output level. The third-order IMR is equal to twice the difference between the third-order intercept and the fundamental output level. These are expressed as:

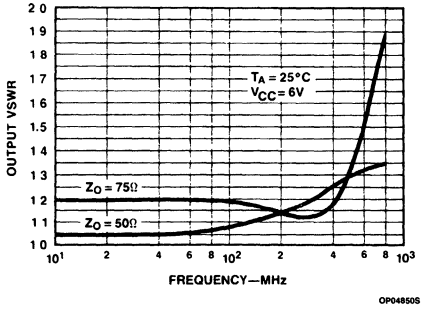
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second- and third-order output intercepts in dBm, and IMR_2 and IMR_3 are the second- and third- order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small-signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point, the intermodulation products no longer follow the straight-line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be care-



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ful, however, not to select levels which are too low, because the test equipment may not be able to recover the signal from the noise. For the NE5204, an output level of –10.5dBm was chosen with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers*; by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985, published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

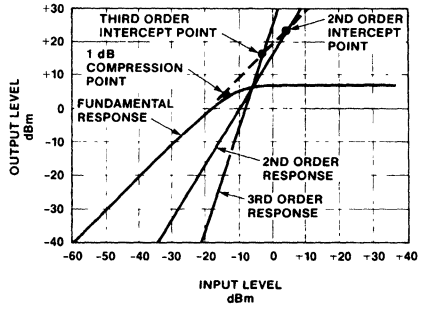


Figure 20

NE/SA/SE5205
Wide-band High-Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES

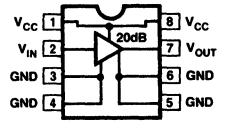
- **600MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **MIL-STD processing available**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

PIN CONFIGURATIONS

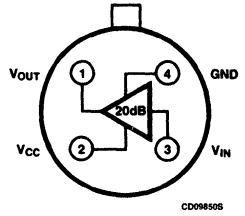
N, FE, D Packages



TOP VIEW

CD12760S

EC Package



CD09850S

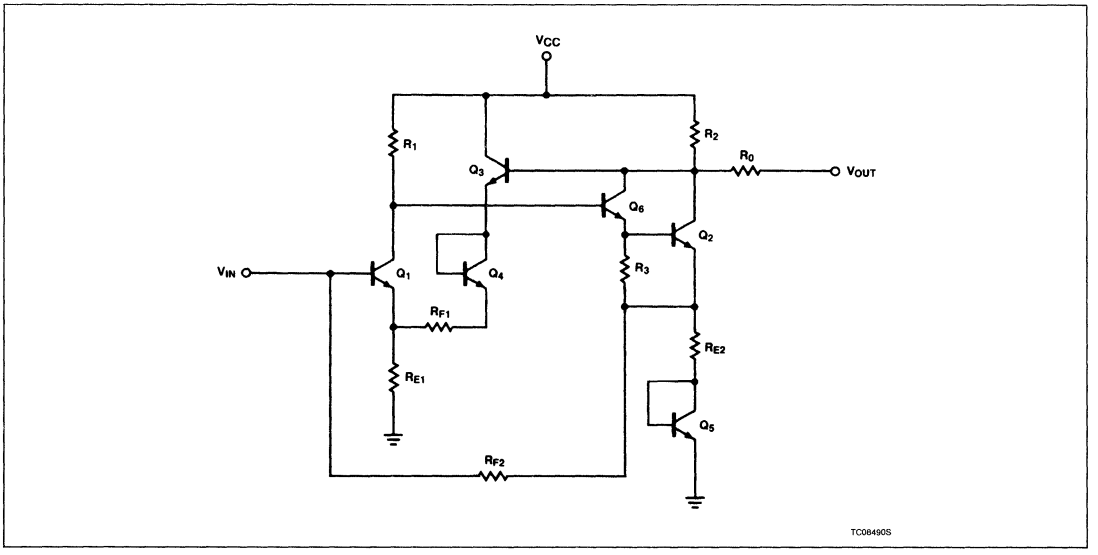
NOTE:
Tab denotes Pin 1

Wide-band High-Frequency Amplifier — NE/SA/SE5205

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
4-Pin Metal can	0 to +70°C	NE5205EC
8-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	−40°C to +85°C	SA5205D
8-Pin Plastic DIP	−40°C to +85°C	SA5205N
8-Pin Cerdip	−40°C to +85°C	SA5205FE
8-Pin Cerdip	−55°C to +125°C	SE5205FE
8-Pin Plastic DIP	−55°C to +125°C	SE5205N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	−40 to +85	°C
	SE grade	−55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1, 2]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW
	EC package	1250	mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

4

DC ELECTRICAL CHARACTERISTICS

at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC − f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC − f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC − f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC − F_{MAX}				10			dB
S12	Isolation	f = 100MHz		−25			−25		dB
		DC − f_{MAX}	−18			−18			dB
t_R	Rise time			5			5		ps
	Propagation delay			5			5		ps

Wide-band High-Frequency Amplifier — NE/SA/SE5205

DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	±0.5dB EC					500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
f_{MAX}	Bandwidth	-3dB EC				600			MHz
f_{MAX}	Bandwidth	-3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+7.0			+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24			+24		dBm

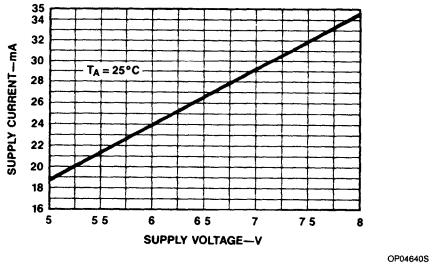


Figure 1. Supply Current vs Supply Voltage

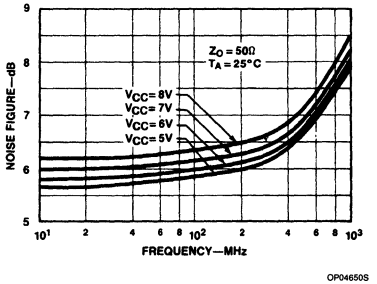


Figure 2. Noise Figure vs Frequency

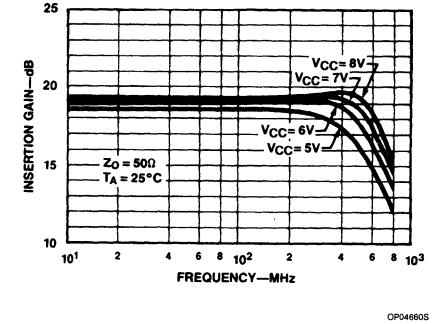


Figure 3. Insertion Gain vs Frequency (S_{21})

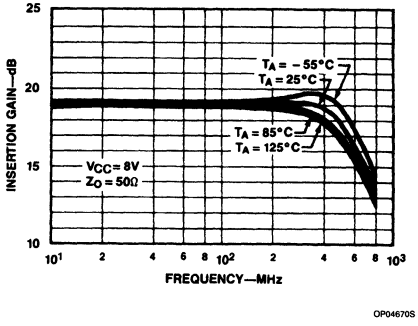


Figure 4. Insertion Gain vs Frequency (S_{21})

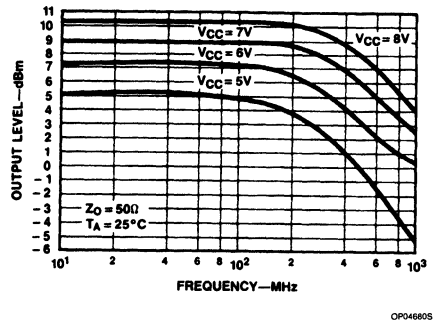


Figure 5. Saturated Output Power vs Frequency

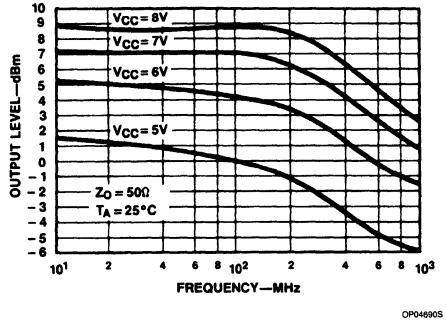


Figure 6. 1dB Gain Compression vs Frequency

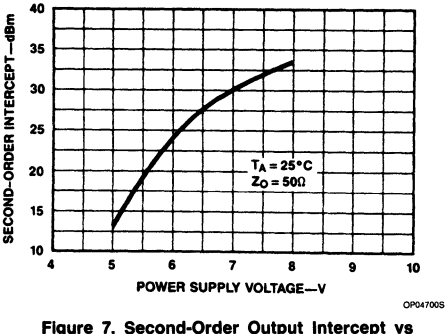


Figure 7. Second-Order Output Intercept vs Supply Voltage

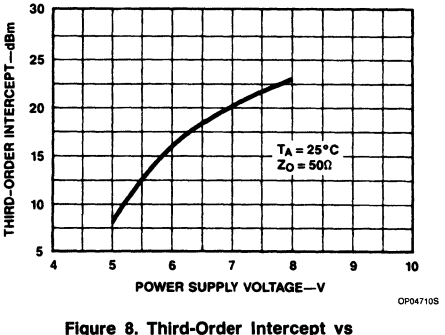


Figure 8. Third-Order Intercept vs Supply Voltage

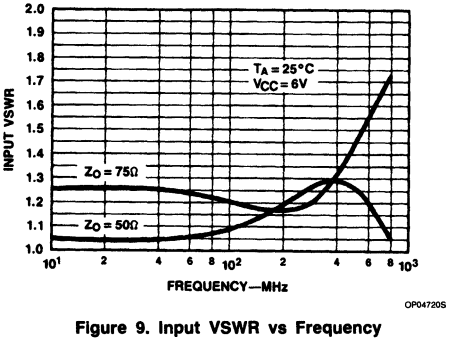


Figure 9. Input VSWR vs Frequency

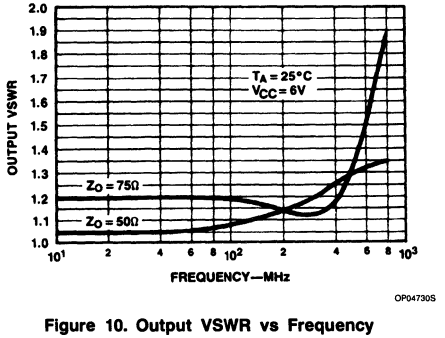


Figure 10. Output VSWR vs Frequency

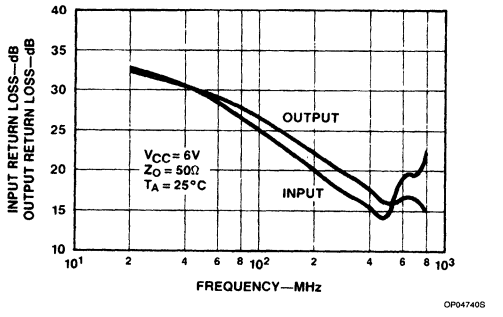


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

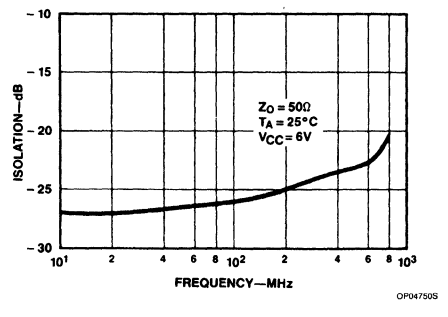


Figure 12. Isolation vs Frequency (S_{12})

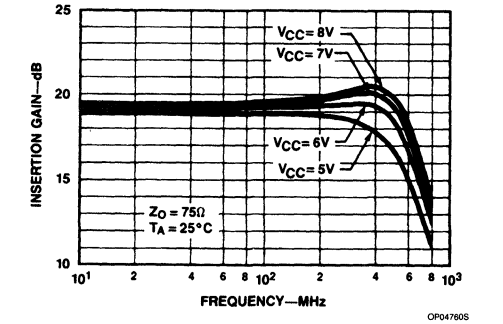


Figure 13. Insertion Gain vs Frequency (S_{21})

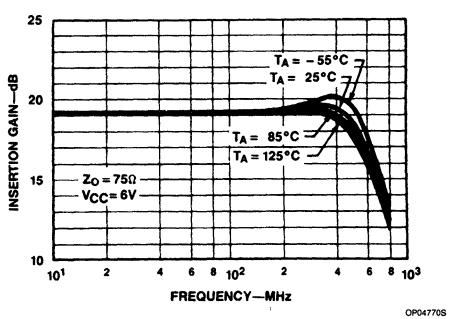


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0} \right\} \text{dB} \quad (2)$$

where I_{C1} = 5.5mA, R_{E1} = 12Ω, r_b = 130Ω, KT/q = 26mV at 25°C and R_0 = 50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where R_{E1} = 12Ω, V_{BE} = 0.8V, I_{C1} = 5mA and I_{C3} = 7mA (currents rated at V_{CC} = 6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1} = 140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where V_{CC} = 6V, R_2 = 225Ω, I_{C2} = 7mA and I_{C6} = 5mA.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

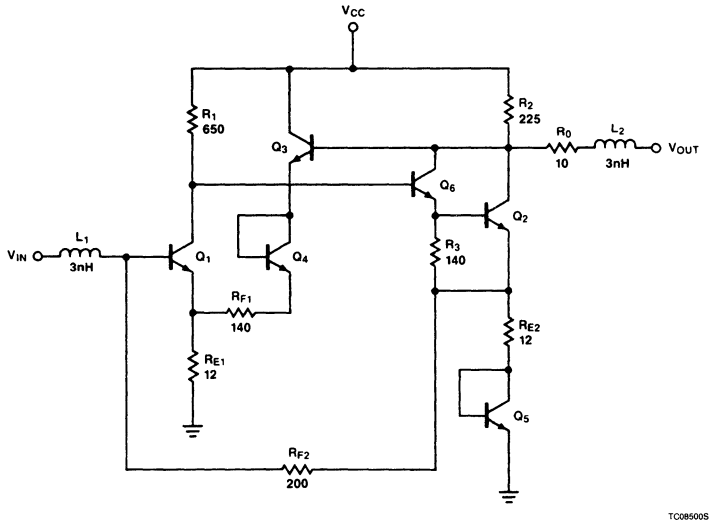


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

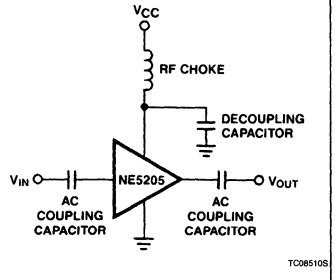


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

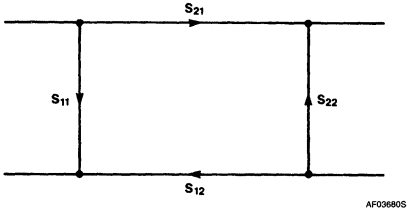


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

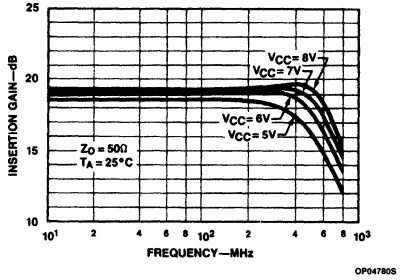
AF03690S

Figure 17b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

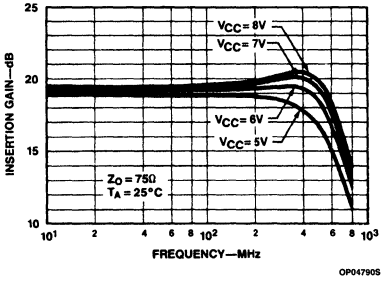
Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

50Ω System

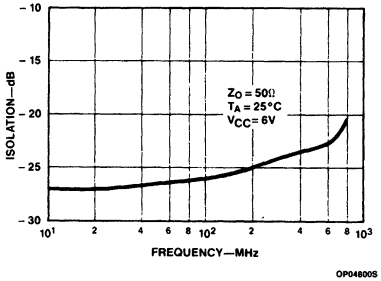


a. Insertion Gain vs Frequency (S_{21})

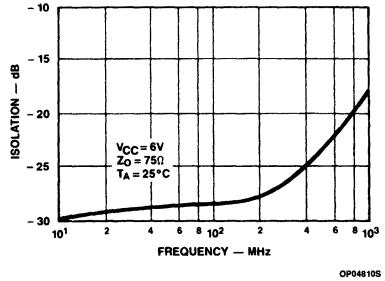
75Ω System



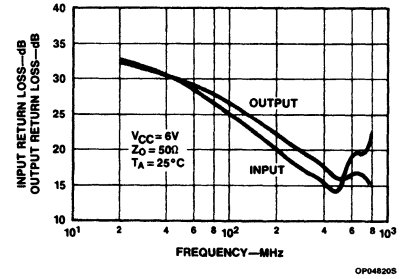
b. Insertion Gain vs Frequency (S_{21})



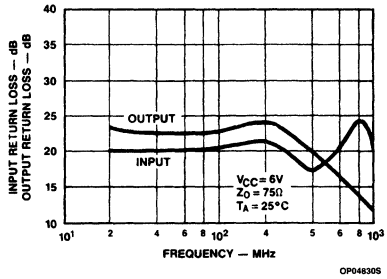
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

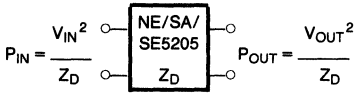


f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$

$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

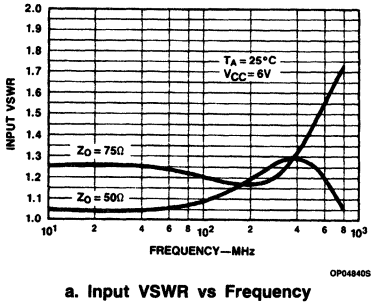
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

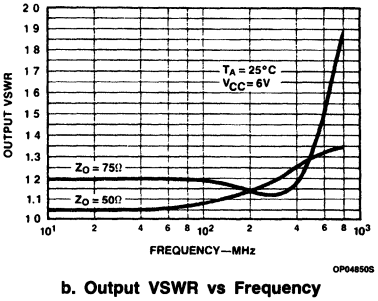
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

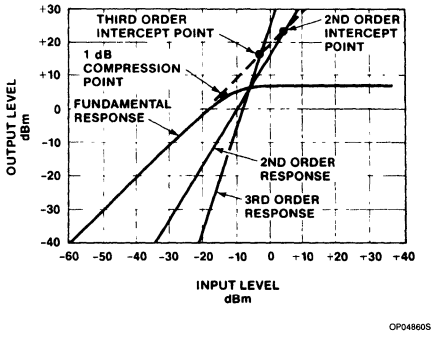


Figure 20

4

Signetics

NE/SE5539
High Frequency Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

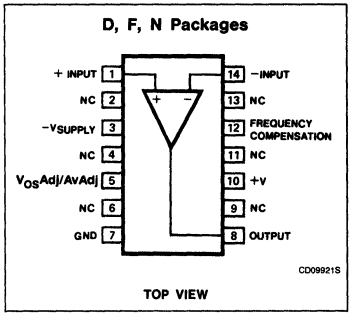
FEATURES

- **Bandwidth**
  - **Unity gain – 350MHz**
  - **Full power – 48MHz**
  - **GBW – 1.2 GHz at 17dB**
- **Slew rate: 600/Vμs**
- **A_{VOL}: 52dB typical**
- **Low noise – 4nV/$\sqrt{Hz}$ typical**
- **MIL-STD processing available**

APPLICATIONS

- **High speed datacomm**
- **Video monitors & TV**
- **Satellite communications**
- **Image processing**
- **RF instrumentation & oscillators**
- **Magnetic storage**
- **Military communications**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

ABSOLUTE MAXIMUM RATINGS[1]

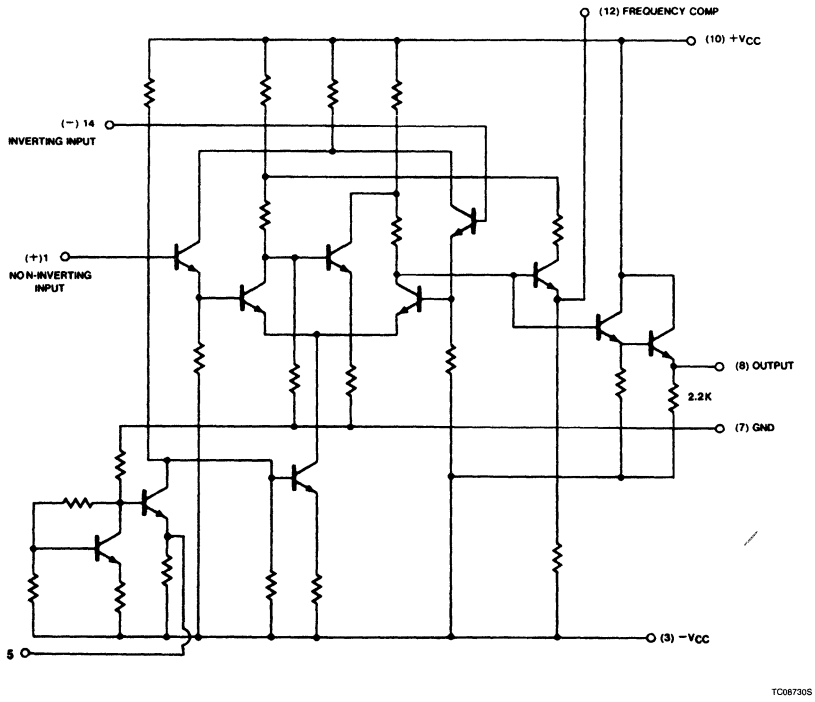
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

High Frequency Operational Amplifier — NE/SE5539

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				-Swing				-1.7	-2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				-Swing	-1.5	-2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				-Swing	-2.0	-2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				-Swing	-1.1	-1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				-Swing	-1.4	-1.8		

High Frequency Operational Amplifier — NE/SE5539

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_0 = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		$nV/\sqrt{Hz}$
	Input noise current	1MHz		6			6		$pA/\sqrt{Hz}$

NOTE:
1 External compensation

4

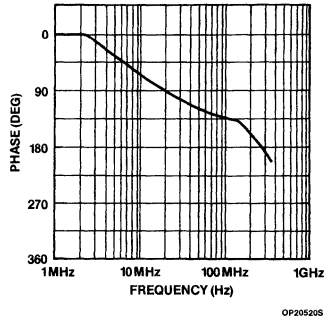
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2$[1]		120		MHz
t_S	Settling time	$A_{CL} = 2$[1]		23		ns
SR	Slew rate	$A_{CL} = 2$[1]		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$[1]		4.5		ns
	Full power response	$A_{CL} = 2$[1]		20		MHz

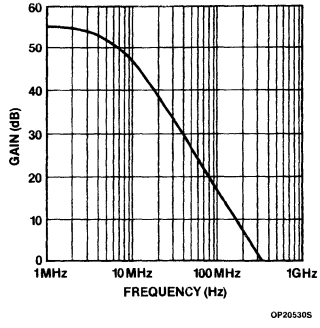
NOTE:
1 External compensation

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

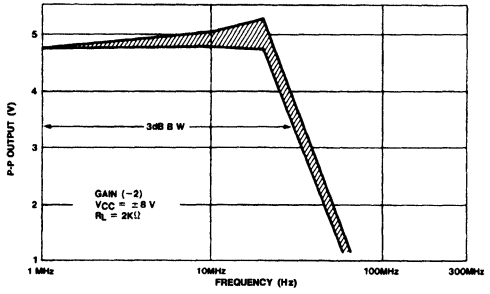


NE5539 Open-Loop Gain



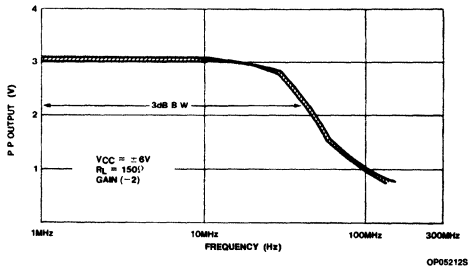
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



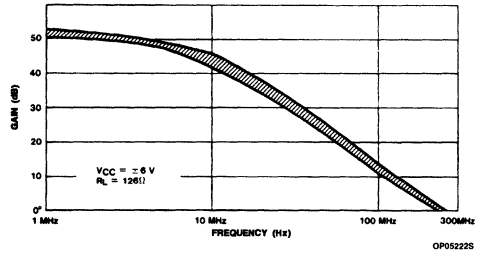
OP05202S

Power Bandwidth (NE)



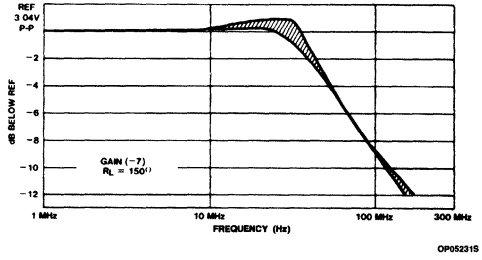
OP05212S

SE5539 Open-Loop Gain vs Frequency



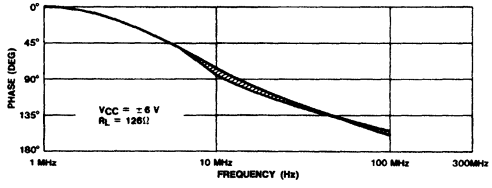
OP05222S

Power Bandwidth

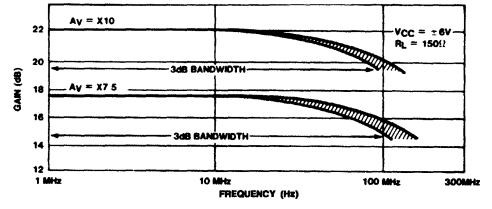


OP05231S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05251S

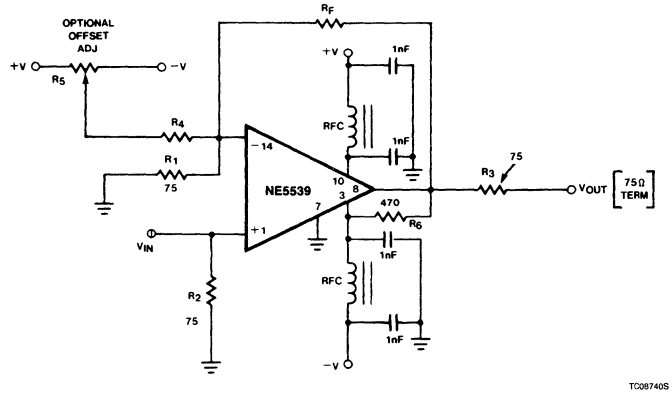
NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05241S

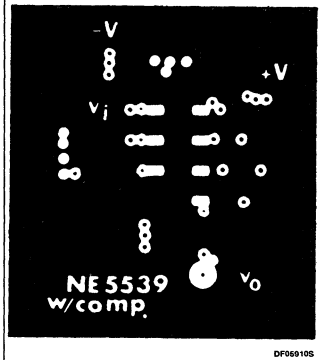
CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

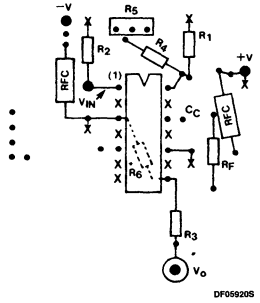


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON
R_5 = 20k TRIMPOT (CERMET)
R_F = 1 5k (28dB GAIN)
R_6 = 470Ω 5% CARBON
RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV)

Top Plane Copper[1] (Component Side)

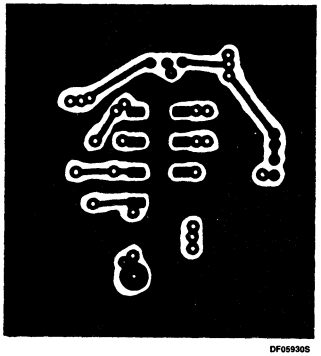


Component Side (Component Layout)



NOTES:
(X) indicates ground connection to top plane
*R_6 is on bottom side

Bottom Plane Copper[1]



NOTE:
1 Bond edges of top and bottom ground plane copper

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

High Frequency Operational Amplifier | NE/SE5539

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:

1 The input signal was 200mV and the output 2V V_{CC} was ±8V.

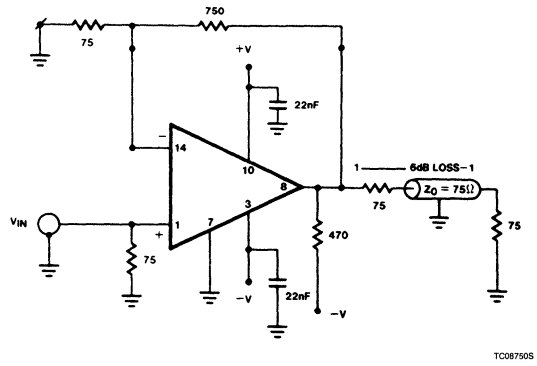


Figure 2. NE5539 Video Amplifier

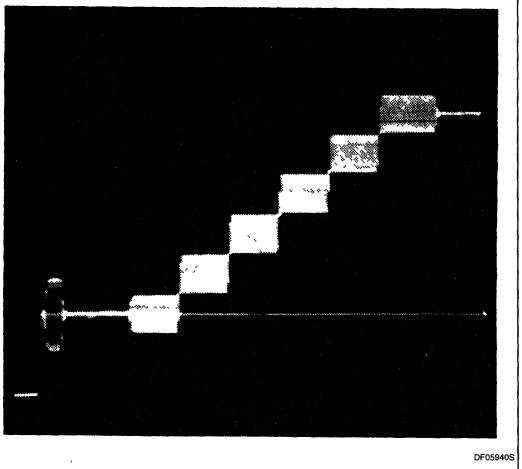


Figure 3. Input Signal

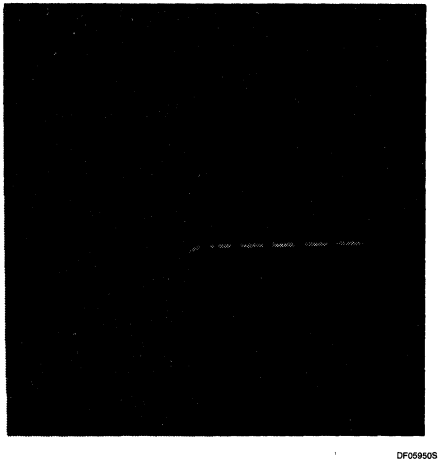


Figure 4. Differential Gain < 0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

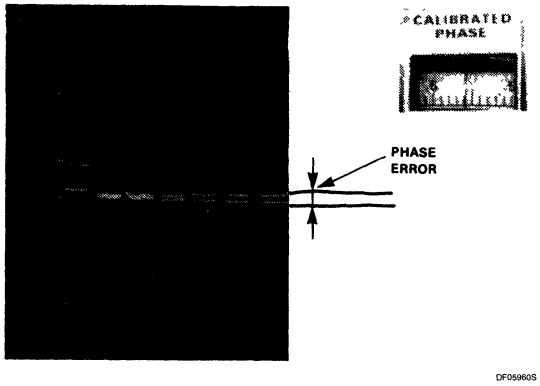


Figure 5. Differential Phase +0.1°

APPLICATIONS

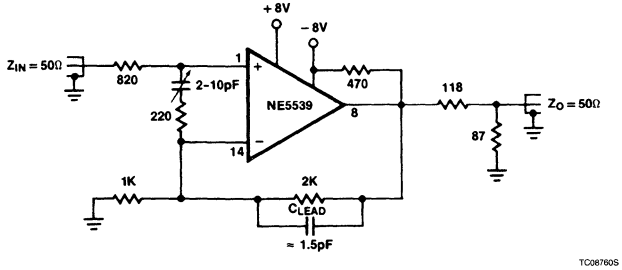


Figure 6. Non-Inverting Follower

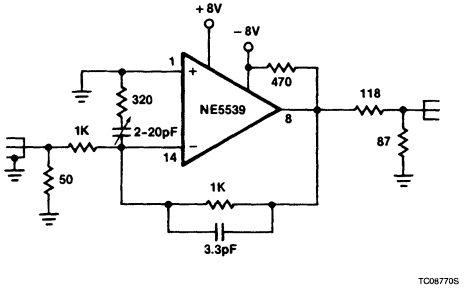


Figure 7. Inverting Follower

Signetics

AN140
Compensation Techniques for Use with the NE/SE5539

Application Note

Linear Products

NE5539 DESCRIPTION

The Signetics NE/SE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today With a unity gain bandwidth of 350MHz and a slew rate of 600V/μs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the NE/SE5539

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1 The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude This zero improves the phase margin

To determine components, it can be shown that the optimal conditions for amplifier stability occur when·

$$(R1)(C_{DIST}) = (R_F)(C_{LEAD}) \quad (1)$$

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{LEAD} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{LEAD} = C_{DIST}\frac{R1}{R_F} \quad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary (Reference Figure 1). For practical applications, the following equations can be used to determine proper lag-lead components.

$$\frac{R_F}{R1/R_{LAG}} \geqslant 7 \quad (4)$$

Therefore,

$$R_{LAG} \leqslant \frac{R_F}{7 - R_F/R1} \quad (5)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{LAG} may now be approximated using:

$$W_{LAG} \cong \frac{2\pi(GBW)}{10}\ \text{Rad/Sec} \quad (6)$$

$$W_{LAG} = \frac{\pi(GBW)}{5}\ \text{Rad/Sec} \quad (7)$$

where

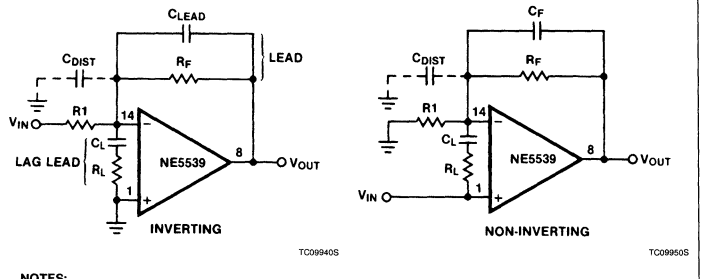
$$W_{LAG} = \frac{1}{(R_{LAG})(C_{LAG})} \quad (8)$$

therefore,

$$\frac{\pi(GBW)}{5} = \frac{1}{(R_{LAG})(C_{LAG})} \quad (9)$$

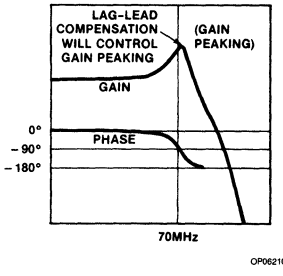
and

$$C_{LAG} = \frac{5}{\pi R_{LAG}(GBW)} \quad (10)$$

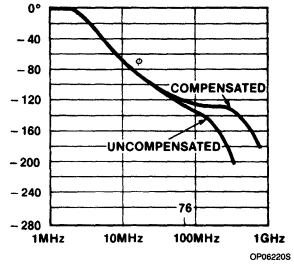


NOTES:
$C_L = C_{LAG}$
$R_L = R_{LAG}$

Figure 1. Standard Lag-Lead Compensation



a. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)



b. Open-Loop Phase

Figure 2

Compensation Techniques for Use with the NE/SE5539 AN140

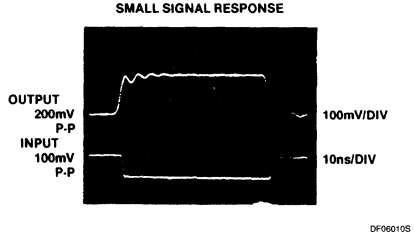


Figure 3. Compensated Pulse Response

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz, see Figures 2a and 2b) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains The result of using this technique is shown for a pulse amplifier in Figure 3.

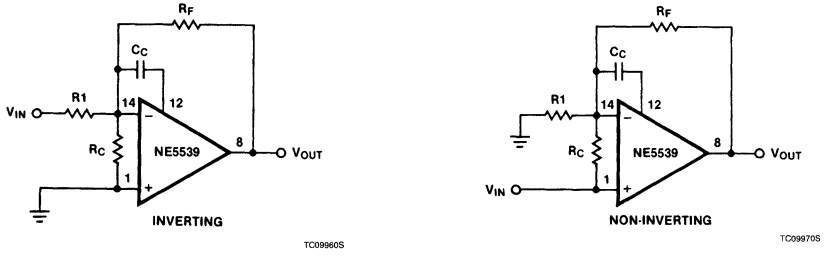


Figure 4. Pin 12 Compensation

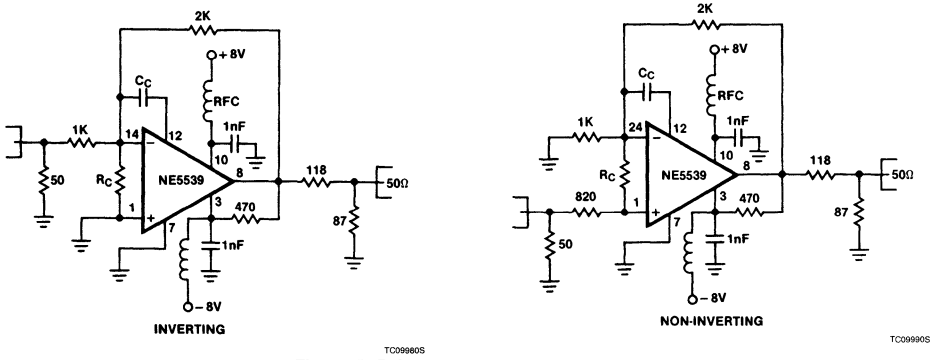


Figure 5. Pulse Response Test Circuits

Compensation Techniques for Use with the NE/SE5539 AN140

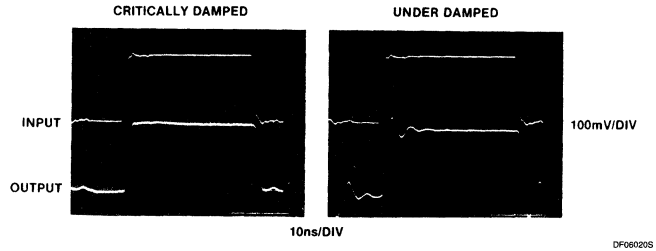


Figure 6. Small Signal Response — Non-Inverting

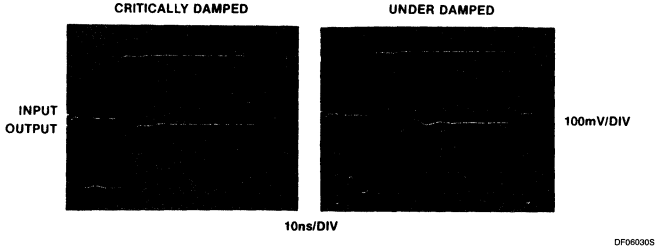


Figure 7. Small Signal Response — Inverting

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the NE/SE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most importantly, both methods are equally effective; i.e., a good wide-band amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using Pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

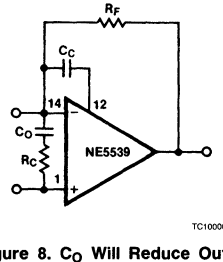


Figure 8. C_O Will Reduce Output Offset and Noise

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01μF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE NE/SE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1 A_2}{1 - (B_F A_2)} + A_3 (1 + B_F A_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11a. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12a and 12b. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to Pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13a through 13f. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

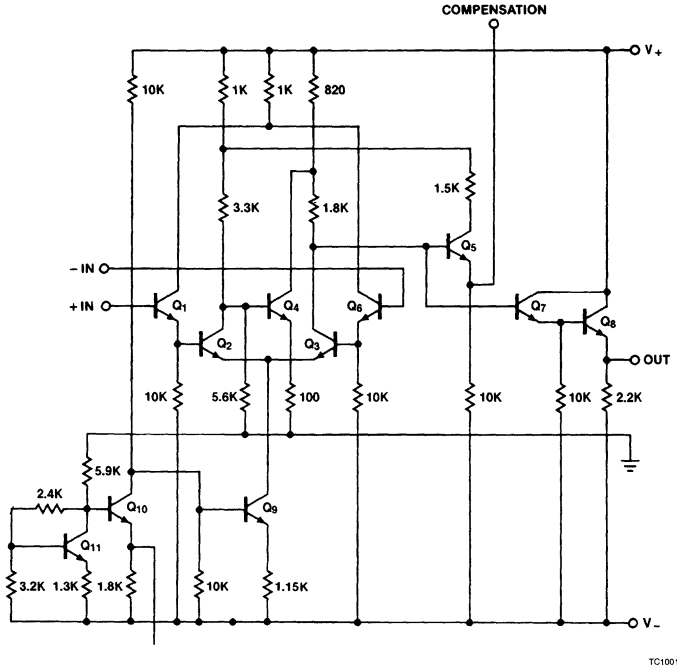


Figure 9. Complete Schematic of NE/SE5539

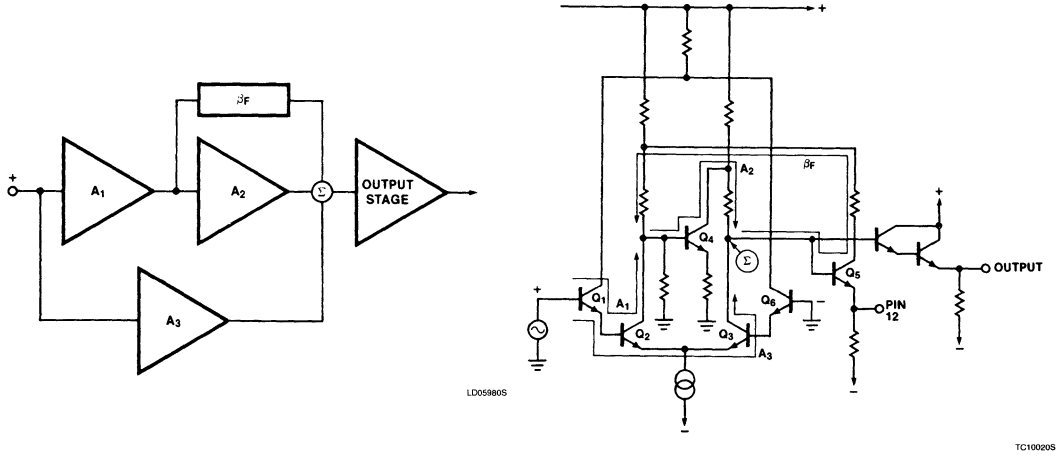
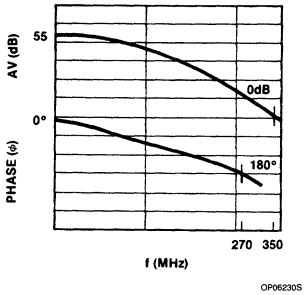


Figure 10. Internal Sections

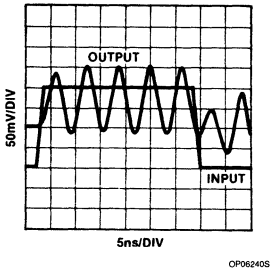
Compensation Techniques for Use with the NE/SE5539 AN140

COMPUTER ANALYSIS

The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. These models are then combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.



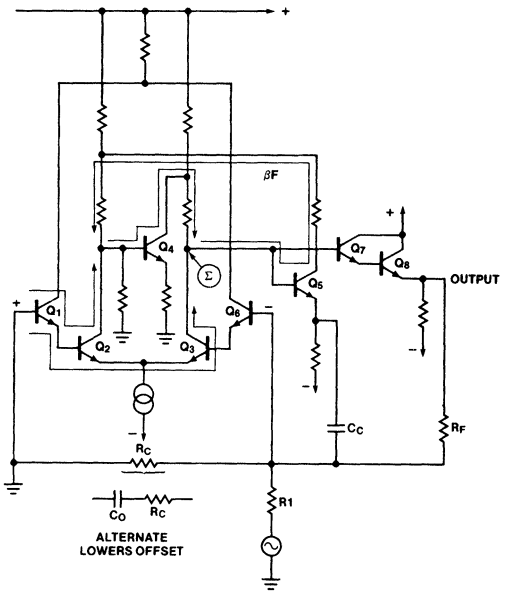
a. Open-Loop Gain — No Compensation (Computer Simulation)



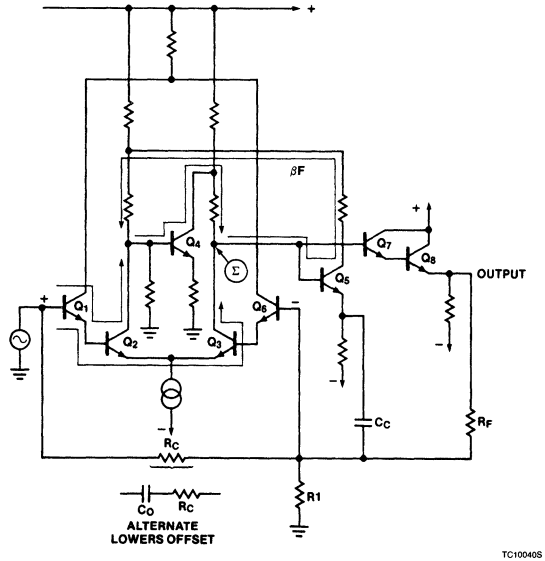
b. Closed-Loop Non-Inverting Response — No Compensation (Computer Simulation — Oscillation is Evident)

Figure 11

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.

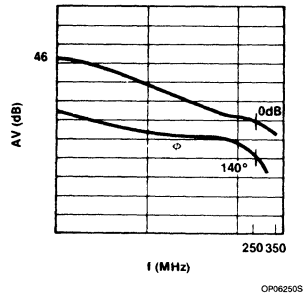


a. Pin 12 Compensation Showing Internal Connections — Inverting

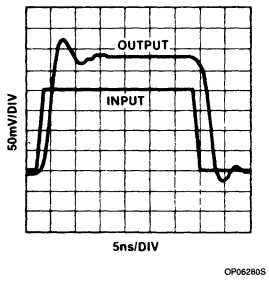


b. Pin 12 Compensation Showing Internal Connections — Non-Inverting

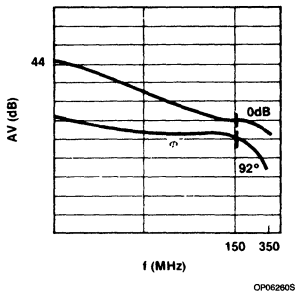
Figure 12



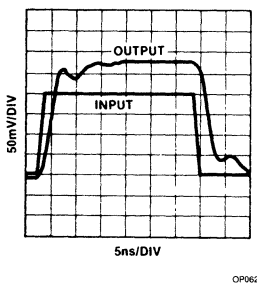
a. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 1pF$, (Computer Simulation)



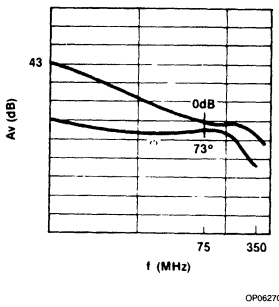
b. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 1pF$, $A_V = 3$ (Computer Simulation — Underdamped)



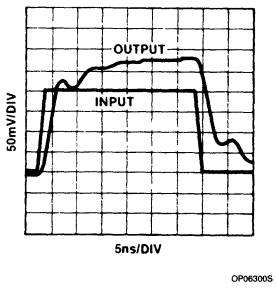
c. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 2pF$ (Computer Simulation)



d. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 2pF$, Av = 3 (Computer Simulation — Critically-Damped)



e. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 3pF$, (Computer Simulation)



f. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 3pF$, $A_V = 3$ (Computer Simulation — Overdamped)

Figure 13

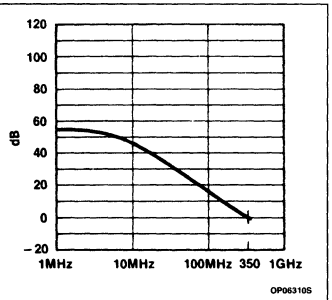


Figure 14. Actual Open-Loop Gain Measured in Lab

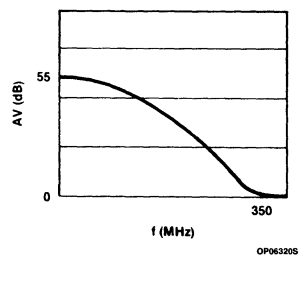


Figure 15. Computer-Generated Open-Loop Gain

1. J. Millman and C. C. Halkias: *Integrated Electronics: Analog and Digital Circuits and Systems,* McGraw-Hill Book Company, New York, 1972.

2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sangiovanni-Vincentelli: "Spice Version 2G," University of California, Berkeley, California, August 10, 1981.

3. Signetics: *Analog Data Manual 1983,* Signetics Corporation, Sunnyvale, California 1983.

Signetics

NE5592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

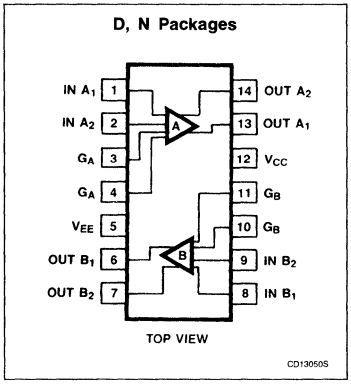
FEATURES

- **110MHz unity gain bandwidth**
- **Adjustable gain from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

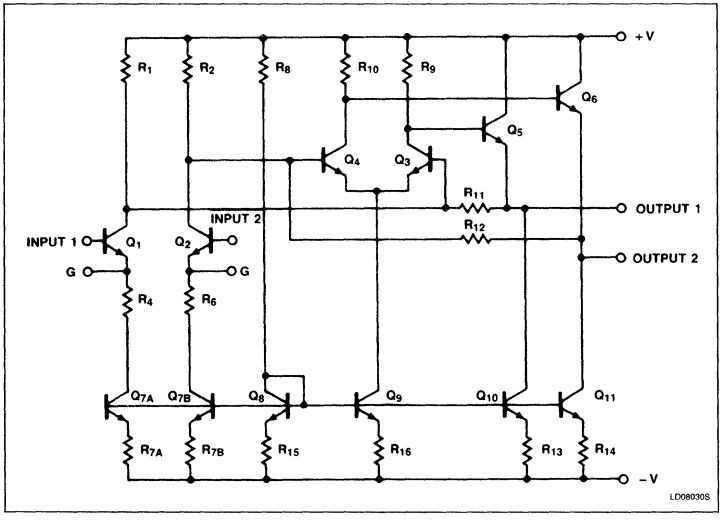
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1]		
	D package	1.03	W
	N package	1.48	W

NOTE:
1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = ±6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage is $V_S = ±6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	μA
I_{BIAS}	Input bias current			5	20	μA
	Input noise voltage	BW 1kHz to 10MHz		4		$nV/\sqrt{Hz}$
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f < 100kHz V_{CM} ± 1V, f = 5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S = ± 0.5V	50	85		dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; f = 100kHz (output referenced) $R_L = 1k\Omega$	65	70		dB
V_{OS}	Output offset voltage gain select pins open	$R_L = \infty$ $R_L = \infty$		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$		35	44	mA

DC ELECTRICAL CHARACTERISTICS $V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

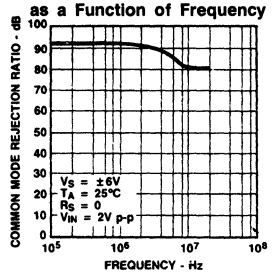
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $R_S = \phi$	55			dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		70		dB
V_{OS}	Output offset voltage gain select pins connected together	$R_L = \infty$			1.5	V
	gain select pins open	$R_L = \infty$			1.0	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$			47	mA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	$V_{OUT} = 1V_{P-P}$		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$		7.5	12	ns

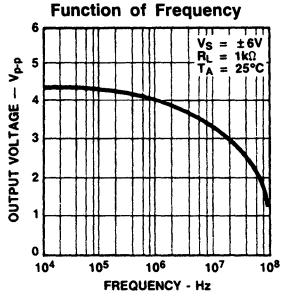
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



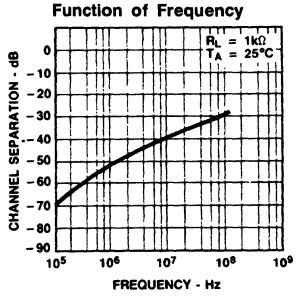
OP18580S

Output Voltage Swing as a Function of Frequency



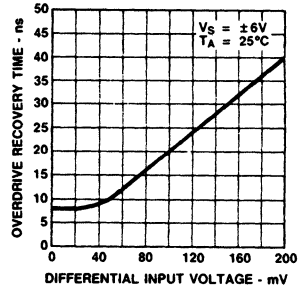
OP18590S

Channel Separation as a Function of Frequency



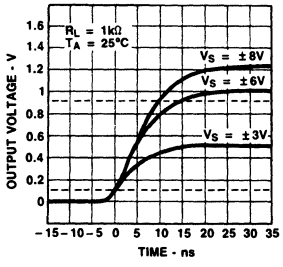
OP18600S

Differential Overdrive Recovery Time



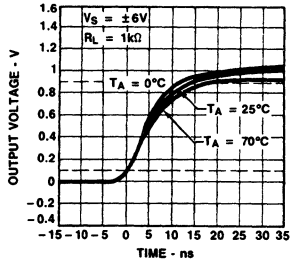
OP18610S

Pulse Response as a Function of Supply Voltage



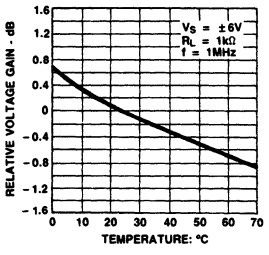
OP18620S

Pulse Response as a Function of Temperature



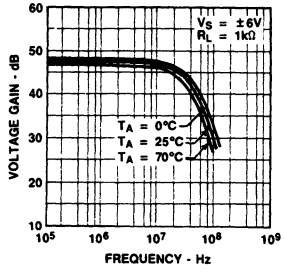
OP18630S

Voltage Gain as a Function of Temperature



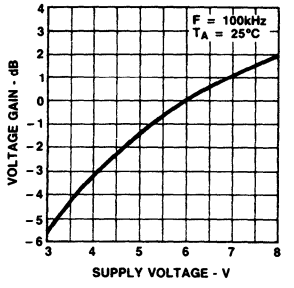
OP18640S

Gain vs Frequency as a Function of Temperature



OP18650S

Voltage Gain as a Function of Supply Voltage

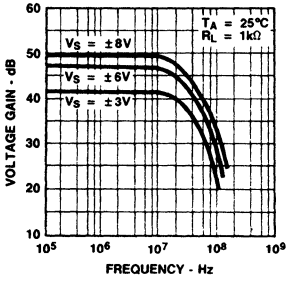


OP18660S

4

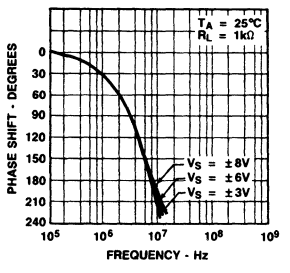
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



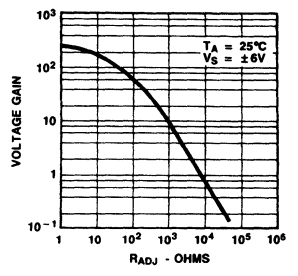
OP18670S

Phase vs Frequency as a Function of Supply Voltage



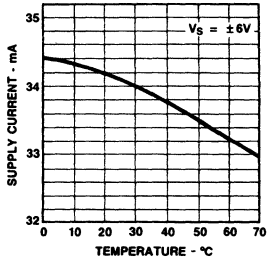
OP18680S

Voltage Gain as a Function of R_{ADJ}



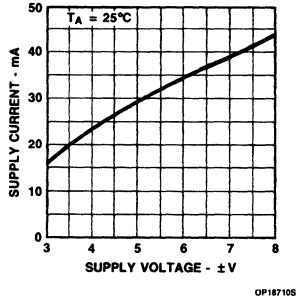
OP18690S

Supply Current as a Function of Temperature



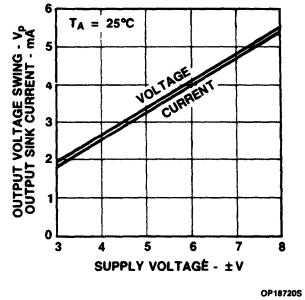
OP18700S

Supply Current as a Function of Supply Voltage



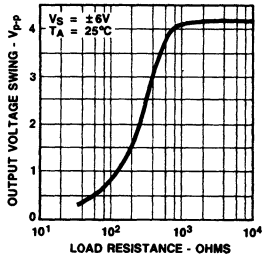
OP18710S

Output Voltage Swing and Sink Current as a Function of Supply Voltage



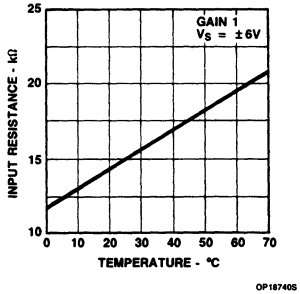
OP18720S

Output Voltage Swing as a Function of Load Resistance



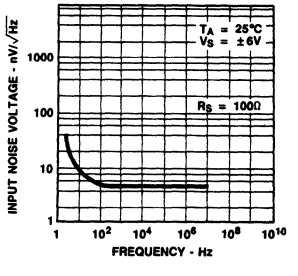
OP18730S

Input Resistance as a Function of Temperature



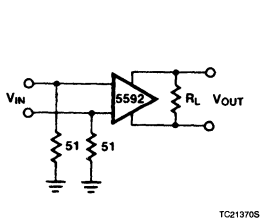
OP18740S

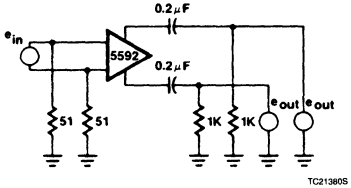
Input Noise Voltage as a Function of Frequency

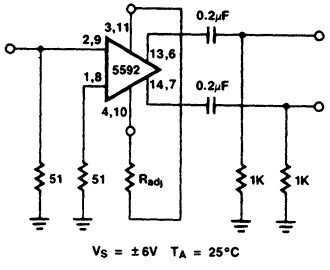


OP18750S

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.







4

Signetics

NE/SA/SE592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

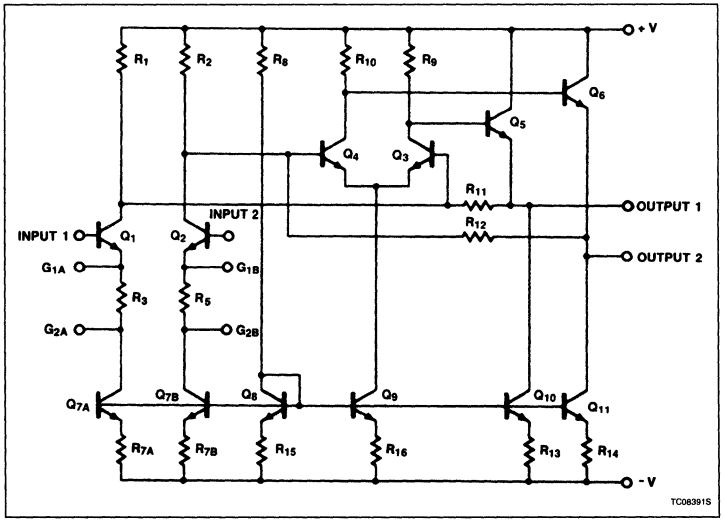
FEATURES

- **120MHz unity gain bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**
- **MIL-STD processing available**

APPLICATIONS

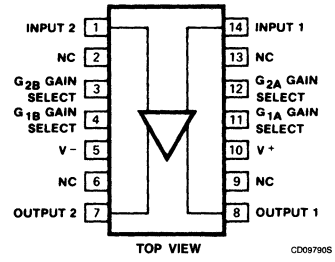
- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

EQUIVALENT CIRCUIT

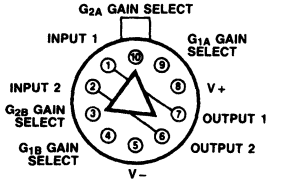


PIN CONFIGURATIONS

D, F, N Packages

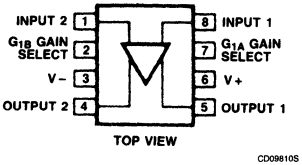


H Package*



NOTES:
Pin 5 connected to case
*Metal cans (H) not recommended for new designs

D, F, N, Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	−55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin Cerdip	−55°C to +125°C	SE592F8
8-Pin Plastic DIP	−40°C to +85°C	SA592N8
8-Pin SO	0 to +70°C	NE592D8
8-Pin SO	−40°C to +85°C	SA592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	−55°C to +125°C	SE592H

NOTE:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i e , NE592HD8

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range		
	SE592	−40 to +85	°C
	NE592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1]		
	F-14 package	1.17	W
	F-8 package	0.79	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	H package	0.83	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTE:
1. Derate above 25°C at the following rates
   F-14 package at 9.3mW/°C
   F-8 package at 6.3mW/°C
   D-14 package at 7 8mW/°C
   D-8 package at 6.3mW/°C
   H package at 6.7mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2, 4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	V_{CM}± 1V, f < 100kHz	60	86		60	86		dB
	Gain 2[4]	V_{CM}± 1V, f = 5MHz		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open
4. Applies to 10- and 14-pin versions only.

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$ for NE592; $-40°C \leq T_A \leq 85°C$ for SA592, $-55°C \leq T_A \leq 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250		600	200		600	V/V
	Gain 2[2, 4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 2[2, 4]		8.0			8.0			kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	50			50			dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.2	V
	Gain 3[3]	$R_L = \infty$			1.0			1.0	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

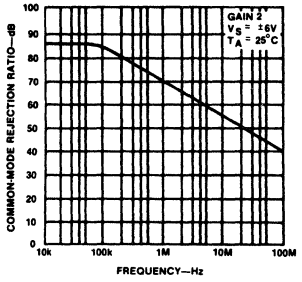
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2, 4]			90			90		MHz
t_R	Rise time								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		10.5			10.5		ns
	Gain 2[2, 4]			4.5	12		4.5	10	ns
t_{PD}	Propagation delay								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		7.5			7.5		ns
	Gain 2[2, 4]			6.0	10		6.0	10	ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

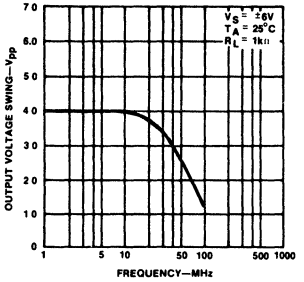
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



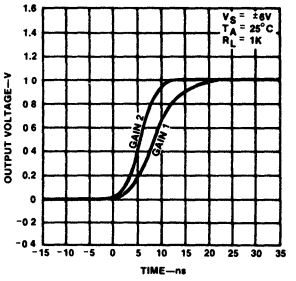
OP04421S

Output Voltage Swing as a Function of Frequency



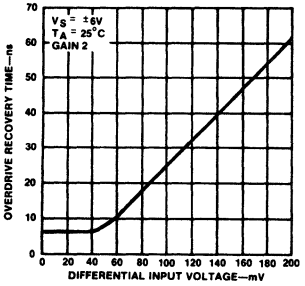
OP04430S

Pulse Response



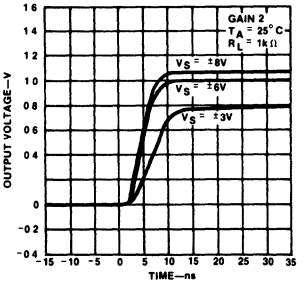
OP04440S

Differential Overdrive Recovery Time



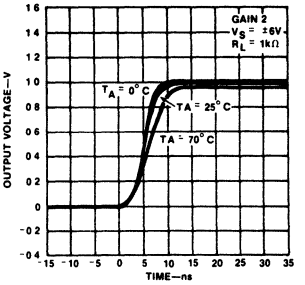
OP04450S

Pulse Response as a Function of Supply Voltage



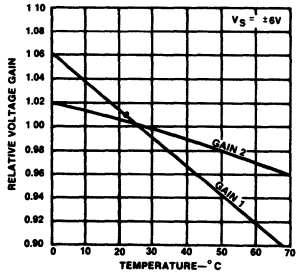
OP04460S

Pulse Response as a Function of Temperature



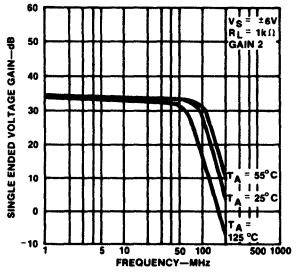
OP04470S

Voltage Gain as a Function of Temperature



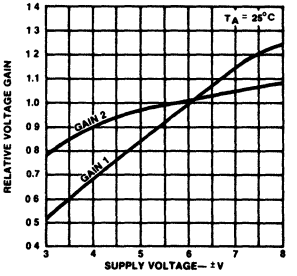
OP04480S

Gain vs Frequency as a Function of Temperature



OP04490S

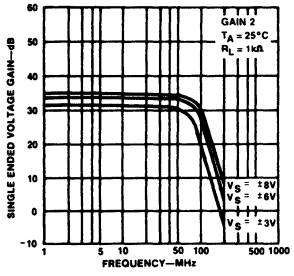
Voltage Gain as a Function of Supply Voltage



OP04500S

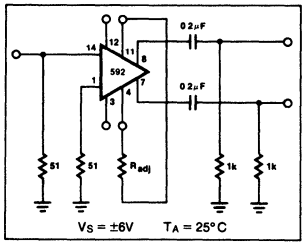
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



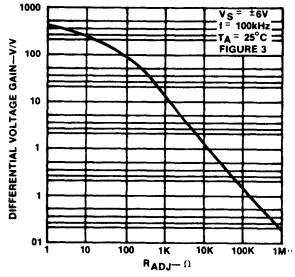
OP04510S

Voltage Gain Adjust Circuit



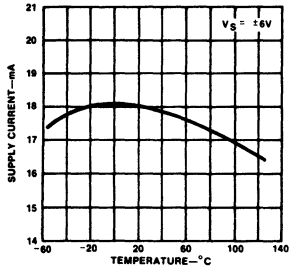
OP04521S

Voltage Gain as a Function of RADJ (Figure 3)



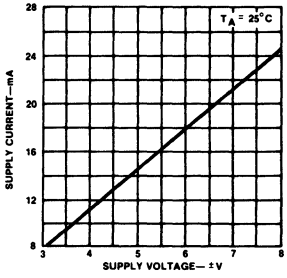
OP04530S

Supply Current as a Function of Temperature



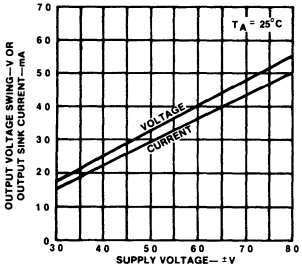
OP04540S

Supply Current as a Function of Supply Voltage



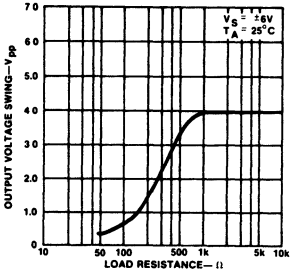
OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage



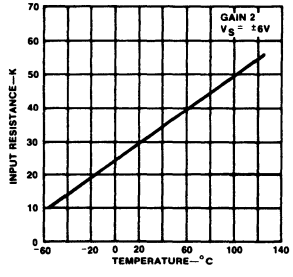
OP04560S

Output Voltage Swing as a Function of Load Resistance



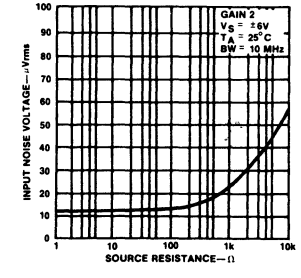
OP04570S

Input Resistance as a Function of Temperature



OP04580S

Input Noise Voltage as a Function of Source Resistance

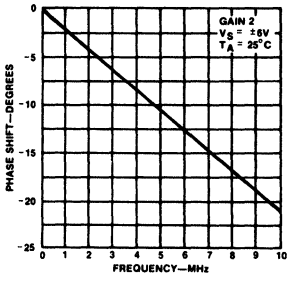


OP04590S

4

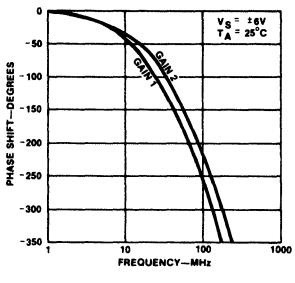
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency



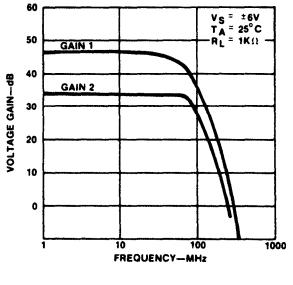
OP04600S

Phase Shift as a Function of Frequency



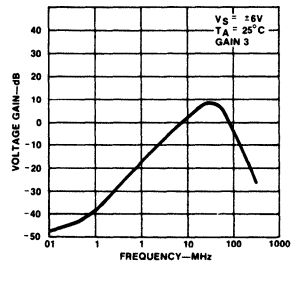
OP04610S

Voltage Gain as a Function of Frequency



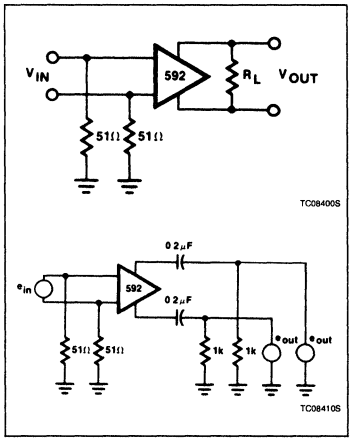
OP04620S

Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

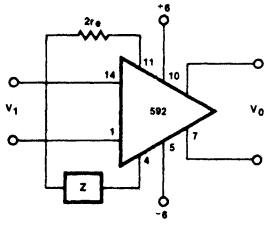


OP04630S

TEST CIRCUITS T_A = 25°C, unless otherwise specified.



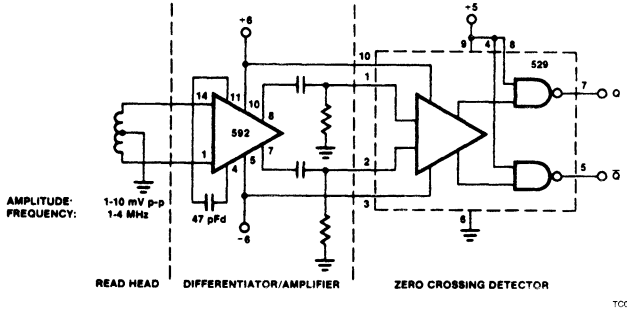
TYPICAL APPLICATIONS



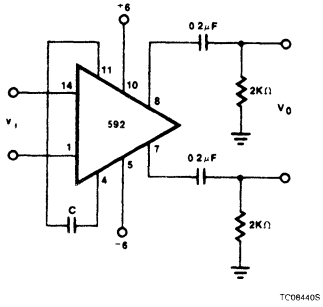
NOTE:

$$\frac{V_O(s)}{V_I(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration



Disc/Tape Phase-Modulated Readback Systems

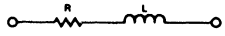
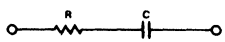
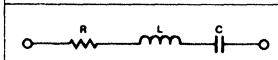
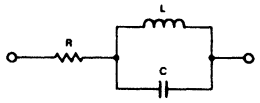


NOTE:
For frequency $F_1 << 1/2\,\pi\,(32)\,C$

$$V_O \cong 1.4 \times 10^4 C \frac{dV_I}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\ s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

TC08422S

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω
$S = j\omega$
$\omega = 2\pi f$

AN141
Using the NE/SA/SE592 Video Amplifier

Application Note

Linear Products

VIDEO AMPLIFIER PRODUCTS

NE/SA/SE592 Video Amplifier

The 592 is a two-stage differential output, wide-band video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins $G_{1A} - G_{1B}$ and $G_{2A} - G_{2B}$, respectively. As shown by Figure 1, the emitter circuits of the differential pair return through independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus, the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400V/V. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single-ended gains are one-half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer, the input bias current required by the 592 may be passed directly through the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a DC path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output DC offset, they should be small — ideally 0Ω. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V – 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \quad (1)$$

$$= \frac{0.005V}{5\mu A}$$

$$= 1.00k\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of PNP transistors and standard level-shifting techniques used in lower frequency devices. Thus, without the aid of level shifting, the output common-mode voltage present on the NE592 is typically 2.9V. Most applications, therefore, require capacitive coupling to the load.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources.

Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 2, the overall gain at low frequencies is a negative 48dB.

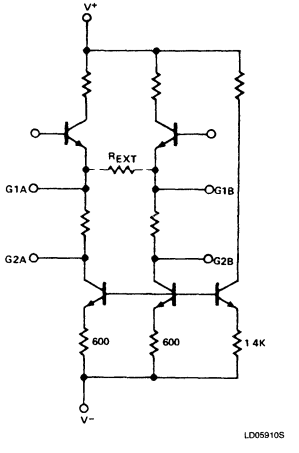
Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB, or unity.

Referring to Figure 3, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA, causing the quantity of 2 r_e to be approximately 32Ω. Overall device gain is thus given by

$$\frac{V_{O(s)}}{V_{IN(s)}} = \frac{1.4 \times 10^4}{Z_{(S)} + 32} \quad (2)$$

where $Z_{(S)}$ can be resistance or a reactive impedance. Table 2 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 2 is the gain calculation to determine the voltage gain as a function of frequency.



NOTE:
All resistor values are in ohms

Figure 1. 592 Input Structure

Table 1. Video Amplifier Comparison File

PARAMETER	NE/SA/SE592	733
Bandwidth (MHz)	120	120
Gain	0,100,400	10,100,400
R_{IN} (k)	4 – 30	4 – 250
V_{P-P} (Vs)	4.0	4 0

Using the NE/SA/SE592 Video Amplifier

AN141

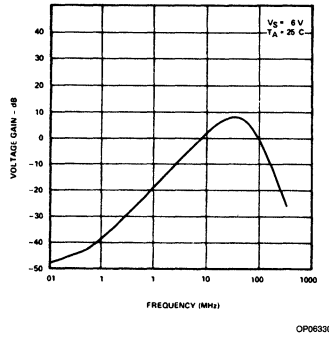
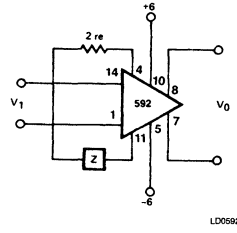


Figure 2. Voltage Gain as a Function of Frequency (All Gain Select Pins Open)



NOTE:

$$\frac{V_0(s)}{V_1(s)} = \frac{1\,4 \times 10^4}{Z(s) + 2re} = \frac{1\,4 \times 10^4}{Z(s) + 32}$$

Figure 3. Basic Gain Configuration for NE592, N14

Differentiation

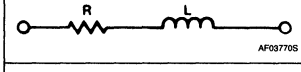
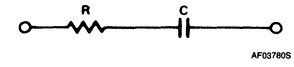
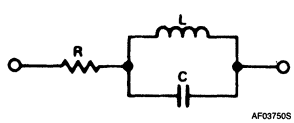
With the addition of a capacitor across the gain select terminals, the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common-mode rejection for proper operation. Figure 4 shows a differential amplifier configuration with transfer function.

Disc File Decoding

In recovering data from disc or drum files, several steps must be taken to precondition the linear data. The NE592 video amplifier, coupled with the 8T20 bidirectional one-shot, provides all the signal conditioning necessary for phase-encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV_{P-P} to 3mV_{P-P} for oxide coated disc files and 1 to 20mV_{P-P} for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

Table 2. Filter Networks

Z NETWORK	FILTER TYPE	$\frac{V_0(s)}{V_1(s)}$ TRANSFER FUNCTION
 AF03770S	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
 AF03780S	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
 AF03790S	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
 AF03750S	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include 2 r_e, or approximately 32Ω
S = jΩ
Ω = 2πf

The classical approach to peak time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 5. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wideband AC-coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common-mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at DC due to the capacitance across the gain select terminals.

The output of the first stage amplifier is routed to a linear phase shift low-pass filter. The filter is a single-stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$$L = 2R/\omega_C$$

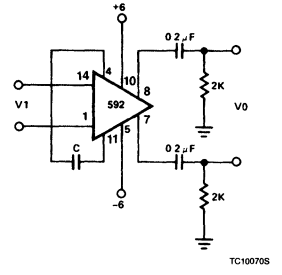
where

R = characteristic impedance (Ω)

$$C = 1/\omega_C$$

where

ω_C = cut-off frequency (radians/sec)



NOTES:
For frequency $F_1 << 1/2\pi(32)C$

$$V_0 \cong 1\,4 \times 10^4 C \frac{dv_i}{dT}$$

All resistor values are in ohms

Figure 4. Differential with High Common-Mode Noise Rejection

Using the NE/SA/SE592 Video Amplifier AN141

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common-mode noise rejection.

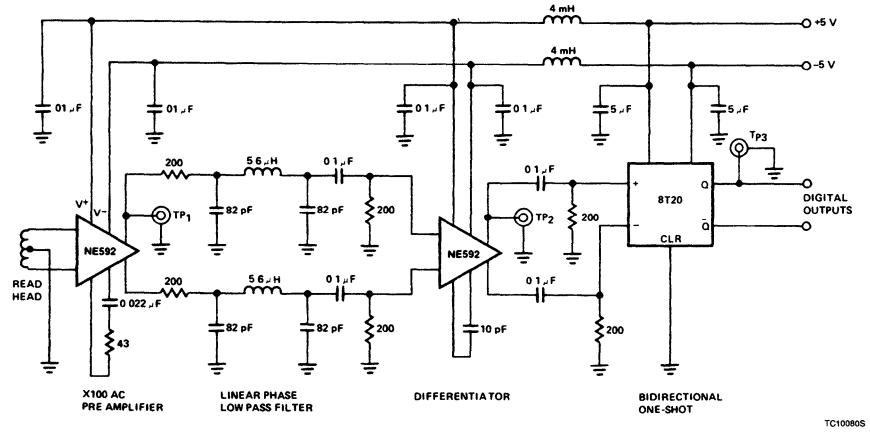
The output of the differentiator/amplifier is connected to the 8T20 bidirectional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 5 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 7.

Automatic Gain Control

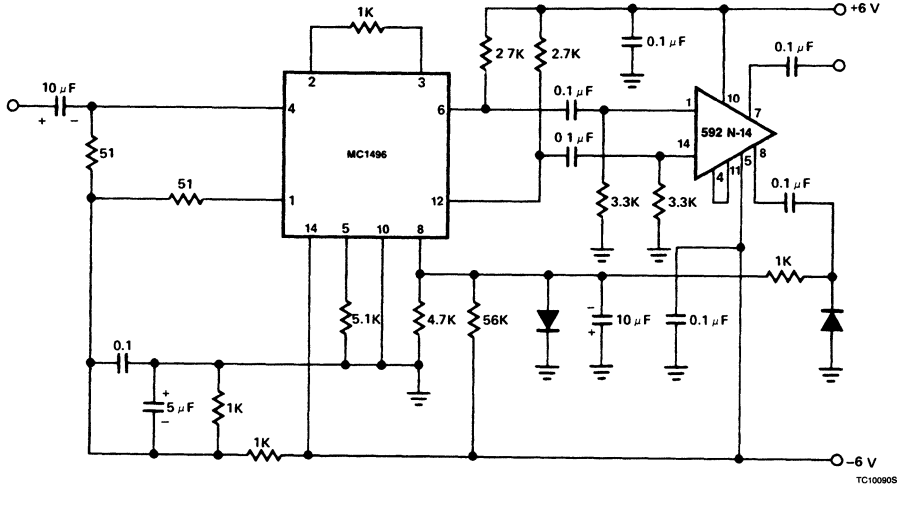
The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system.

The signal is fed to the signal input of the MC1496 and RC-coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass through unattenuated. Rectifying and filtering one of the NE592 outputs produces a DC signal which is proportional to the AC signal amplitude. After filtering; this control signal is applied to the MC1496 causing its gain to change.



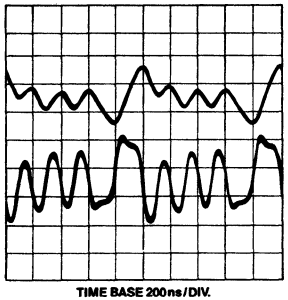
NOTE:
All resistor values are in ohms

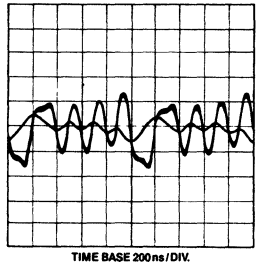
Figure 5. 5MHz Phase-Encoded Data Read Circuitry



NOTE:
All resistor values are in ohms

Figure 6. Wide-band AGC Amplifier





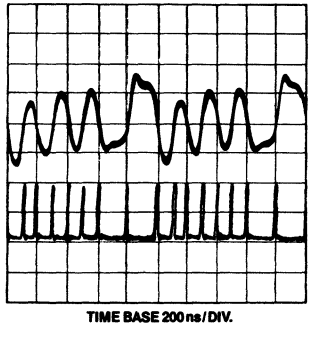


Figure 7. Test Results of Disc File Decoder Circuit

Signetics

MC1496/MC1596
Balanced Modulator/ Demodulator

Product Specification

Linear Products

DESCRIPTION

The MC1496 is a monolithic double-balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of −55°C to +125°C. The MC1496 is intended for applications within the range of 0°C to +70°C.

FEATURES

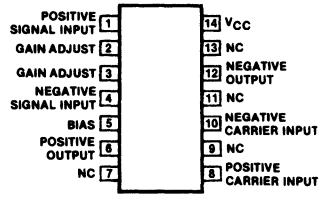
- **Excellent carrier suppression**
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common-mode rejection — 85dB typ**

APPLICATIONS

- **Suppressed carrier and amplitude modulation**
- **Synchronous detection**
- **FM detection**
- **Phase detection**
- **Sampling**
- **Single sideband**
- **Frequency doubling**

PIN CONFIGURATION

F, N Packages



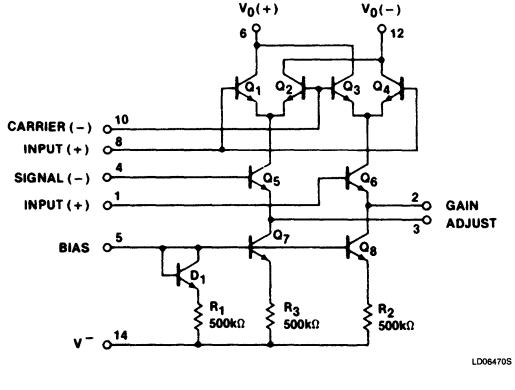
TOP VIEW

CD11131S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to +70°C	MC1496F
14-Pin Plastic	0 to +70°C	MC1496N
14-Pin Cerdip	−55°C to +125°C	MC1596F
14-Pin Plastic	−55°C to +125°C	MC1596N

EQUIVALENT SCHEMATIC



LD06470S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Applied voltage	30	V
$V_8 - V_{10}$	Differential input signal	±5.0	V
$V_4 - V_1$	Differential input signal	$(5 \pm I_5\ R_e)$	V
$V_2 - V_1$, $V_3 - V_4$	Input signal	5.0	V
I_5	Bias current	10	mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package N package	 1190 1420	 mW mW
T_A	Operating temperature range MC1496 MC1596	 0 to +70 −55 to +125	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +12V_{DC}$; $V_{CC} = -8.0V_{DC}$; $I_5 = 1.0mA_{DC}$; $R_L = 3.9k\Omega$; $R_E = 1.0k\Omega$; $T_A = 25°C$, unless otherwise specified.

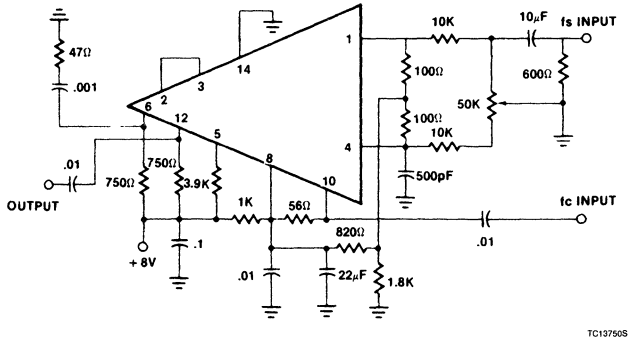
SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{IP} C_{IP}	Single-ended input impedance Parallel input resistance Parallel input capacitance	Signal port, f = 5.0MHz		200 2.0			200 2.0		 kΩ pF
R_{OP} C_{OP}	Single-ended output impedance Parallel output resistance Parallel output capacitance	f = 10MHz		40 5.0			40 5.0		 kΩ pF
I_{BS} I_{BC}	Input bias current $I_{BS} = \frac{I_1 + I_4}{2}$ $I_{BC} = \frac{I_8 + I_{10}}{2}$			 12 12	 25 25		 12 12	 30 30	μA μA
I_{IOS} I_{IOC}	Input offset current $I_{IOS} = I_1 - I_4$ $I_{IOC} = I_8 - I_{10}$			 0.7 0.7	 5.0 5.0		 0.7 0.7	 7.0 7.0	μA μA
TCI_{IO} I_{OO}	Average temperature coefficient of input offset current Output offset current $I_6 - I_{12}$			2.0 14	 50		2.0 15	 80	nA/°C μA
TCI_{OO} V_O	Average temperature coefficient of output offset current Common-mode quiescent output voltage (Pin 6 or Pin 12)			90 8.0			90 8.0		nA/°C V_{DC}
I_{D+} I_{D-}	Power supply current $I_6 + I_{12}$ I_{14}			2.0 3.0	3.0 4.0		2.0 3.0	4.0 5.0	mA_{DC}
P_D	DC power dissipation			33			33		mW

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +12V_{DC}$; $V_{CC} = -9.0V_{DC}$; $I_5 = 1.0mA_{DC}$; $R_L = 3.9k\Omega$; $R_E = 1.0k\Omega$; $T_A = +25°C$, unless otherwise specified.

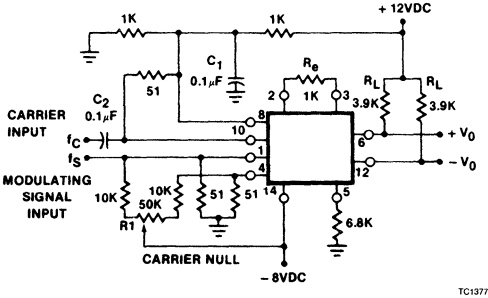
SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	$V_C = 60mV_{RMS}$ sinewave and offset adjusted to zero							
		$f_C = 1.0kHz$		40			40		μV_{RMS}
		$f_C = 10MHz$		140			140		
		$V_C = 300mV_{P-P}$ squarewave:							
		Offset adjusted to zero		0.04	0.2		0.04	0.4	mV_{RMS}
		$f_C = 1.0kHz$							
		Offset not adjusted $f_C = 1.0kHz$		20	100		20	200	
V_{CS}	Carrier suppressions	$f_S = 10kHz$, $300mV_{RMS}$ sinewave							
		$f_C = 500kHz$, $60mV_{RMS}$ sinewave	50	65		40	65		dB
		$f_C = 10MHz$, $60mV_{RMS}$ sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) ($R_L = 50\Omega$)	Carrier input port, $V_C = 60mV_{RMS}$ sinewave $f_S = 1.0kHz$, $300mV_{RMS}$ sinewave		300			300		MHz
		Signal input port, $V_S = 300mV_{RMS}$ sinewave $\lvert V_C \rvert = 0.5V_{DC}$		80			80		MHz
A_{VS}	Signal gain	$V_S = 100mV_{RMS}$; $f = 1.0kHz$ $\lvert V_C \rvert = 0.5V_{DC}$	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, $f_S = 1.0kHz$		5.0			5.0		V_{P-P}
A_{CM}	Common-mode gain	Signal port, $f_S = 1.0kHz$ $\lvert V_C \rvert = 0.5V_{DC}$		-85			-85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		V_{P-P}

4

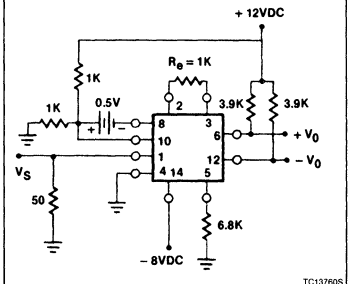
TEST CIRCUITS



Carrier Rejection and Suppression



Carrier Rejection and Suppression



Signal Gain and Output Swing

Signetics

Linear Products

AN189
Balanced Modulator/ Demodulator Applications Using the MC1496/MC1596

Application Note

BALANCED MODULATOR/ DEMODULATOR APPLICATIONS USING MC1496/MC1596

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

THEORY OF OPERATION

As Figure 1 suggests, the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S

To accomplish this the differential pairs Q1 – Q2 and Q3 – Q4, with their cross-coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With a low level signal, V_S driving the third differential amplifier Q5 – Q6, the output voltage will be full wave multiplication of V_C and V_S. Thus for sine wave signals, V_{OUT} becomes:

$$V_{OUT} = E_x E_y \left[\cos(\omega x + \omega y)t + \cos(\omega x - \omega y)t \right] \quad (1)$$

As seen by equation (1) the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals. (See Figure 4.)

BIASING

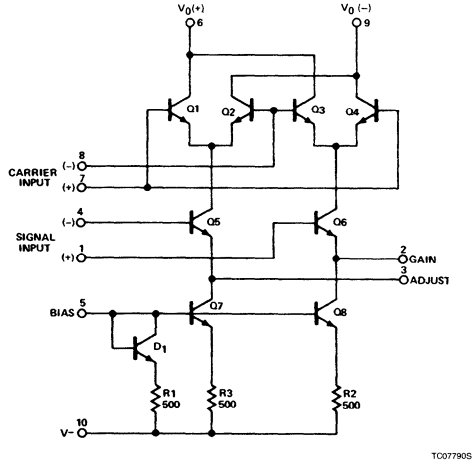
Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single-ended or dual supplies.

Internally provided with the device are two current sources driven by a temperature-compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q_7 and Q_8 will be identical to the current set at Pin 5. Figures 2 and 3 illustrate typical biasing arrangements from split and single-ended supplies, respectively.

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

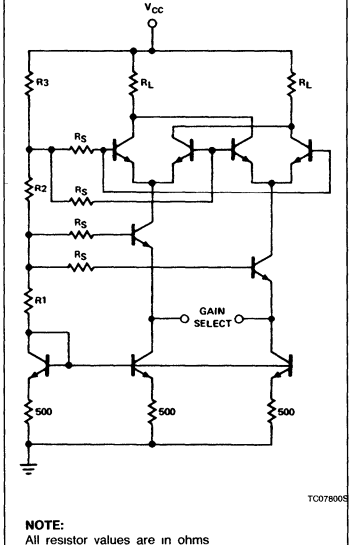
The transistors are connected in a cascode fashion. Therefore, sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2V are sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 3. This configuration assumes the presence of symmetrical supplies. Explaining the DC biasing technique is probably best accomplished by



NOTE:
All resistor values are in ohms

Figure 1. Balanced Modulator Schematic



NOTE:
All resistor values are in ohms

Figure 2. Single-Supply Biasing

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

AN189

an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than $4V_{P-P}$
2. Positive and negative supplies of 6V are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

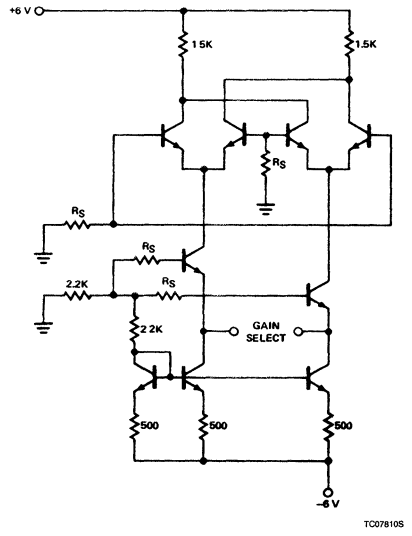
As a matter of convenience, the carrier signal ports are referenced to ground. If desired, the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at DC ground, the quiescent operating point of the outputs should be at one-half the total positive voltage or 3V for this case. Thus, a collector load resistor is selected which drops 3V at 2mA or 1.5kΩ. A quick check at this point reveals that with these loads and current levels the peak-to-peak output swing will be greater than 4V. It remains to set the current source level and proper biasing of the signal ports.

The voltage at Pin 5 is expressed by

$$V_{BIAS} = V_{BE} = 500 \times I_S$$

where I_S is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at Pin 5 becomes 1.7V. Because of the cascode configuration, both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence, the remaining voltage of the negative supply (−6V + 1.7V = −4.3V) is split between these transistors by biasing the signal transistor bases at −2.15V.



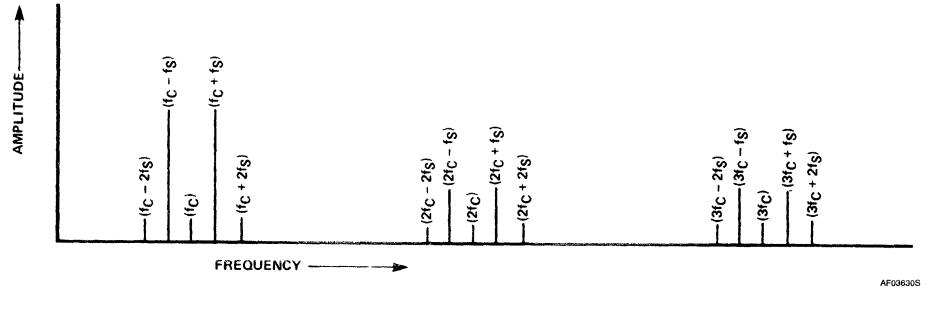
NOTE.
All resistor values are in ohms

Figure 3. Dual Supply Biasing

Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient DC voltage is applied to each bias point to avoid collector saturation over the expected signal swings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs, the output, as mentioned, contains the sum and difference frequencies while attenuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 4.



NOTES:
f_C Carrier Fundemental
f_S Modulating Signal
$f_C \pm f_S$ Fundemental Carrier Sidebands
$f_C \pm nf_S$ Fundemental Carrier Sideband Harmonics
nf_C Carrier Harmonics
$nf_C \pm nf_S$ Carrier Harmonic Sidebands

Figure 4. Modulator Frequency Spectrum

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

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Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 5. Degeneration also allows the maximum signal level of the modulation to be increased. In general, linear response defines the maximum input signal as

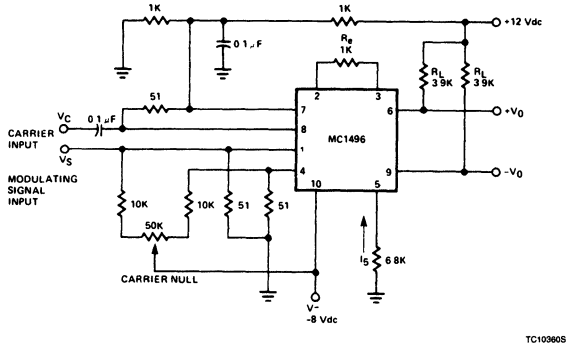
$$Vs \leqslant 15 \cdot R_E(Peak)$$

and the gain is given by

$$A_{VS} = \frac{R_L}{R_E + 2r_e} \qquad (2)$$

This approximation is good for high levels of carrier signals. Table 1 summarizes the gain for different carrier signals.

As seen from Table 1, the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed, the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 4) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.



NOTE:
All resistor values are in ohms

Figure 5. Double Sideband Suppressed Carrier Modulator

Table 1. Voltage Gain and Output Spectrum vs Input Signal

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level DC	$\frac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level DC	$\frac{R_L}{R + 2r_e}$	f_M
Low-level AC	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level AC	$\frac{0.637R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$...

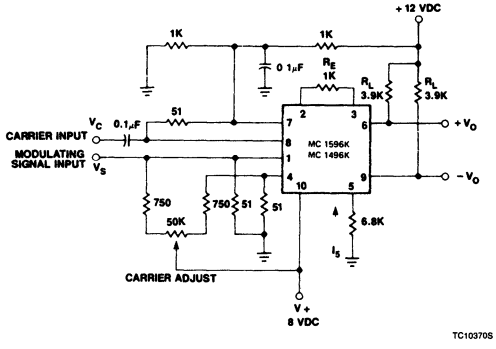
AM MODULATOR

The basic current of Figure 5 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown, the carrier null circuit is changed from Figure 5 to have a wider range so that wider control is achieved. All connections are shown in Figure 6.

AM DEMODULATION

As pointed out in Equation 1, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action, the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7.

Amplifying and limiting of the AM carrier is accomplished by IF gain block providing 55dB



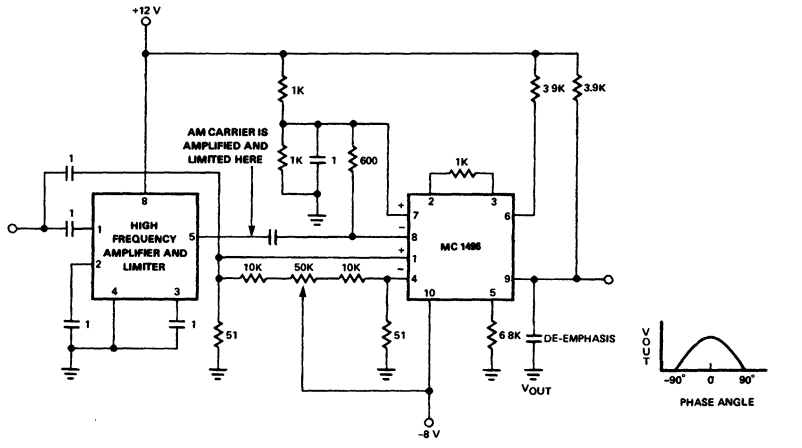
NOTE:
All resistor values are in ohms

Figure 6. AM Modulator

4

Balanced Modulator/Demodulator Applications Using the MC1496/MC1596

AN189

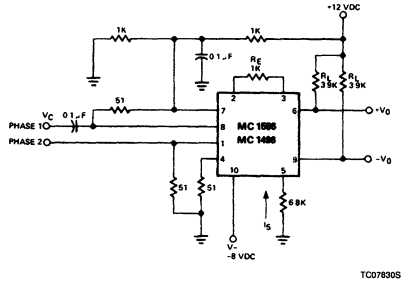


NOTE:
All resistor values are in ohms

Figure 7. AM Demodulator

of gain or higher with limiting of 400μV. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the synchronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7.

Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.



NOTE:
All resistor values are in ohms

Figure 8. Phase Comparator

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned, the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 8. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become DC while the undesired sum component is filtered out. The DC component is related to the phase angle by the graph of Figure 9. At 90° the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180°, respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion gain rather than a loss for greater resolution. Used in conjunction with a phase-locked loop, for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 8, a frequency doubler schematic is shown in Figure 10. Departure from Figure 8 is primarily the removal of the low-pass filter. The output then contains the sum component which is twice the frequency of the input, since both input signals are the same frequency.

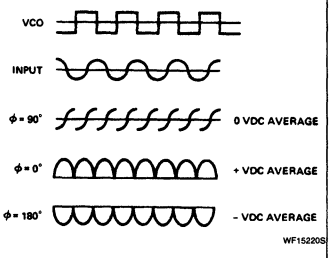
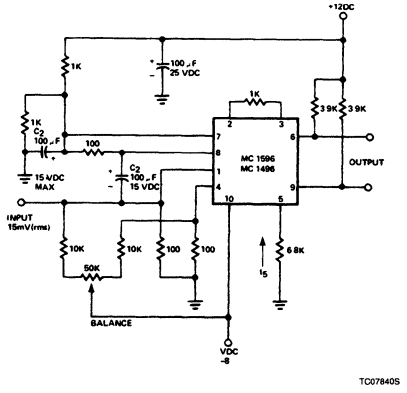


Figure 9. Phase Detector ± Voltages



NOTE:
All resistor values are in ohms

Figure 10. Low Frequency Doubler

4

Signetics

NE/SA602
Double-Balanced Mixer and Oscillator

Product Specification

Linear Products

DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

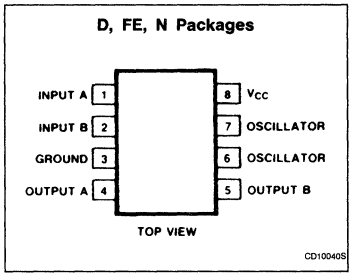
FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

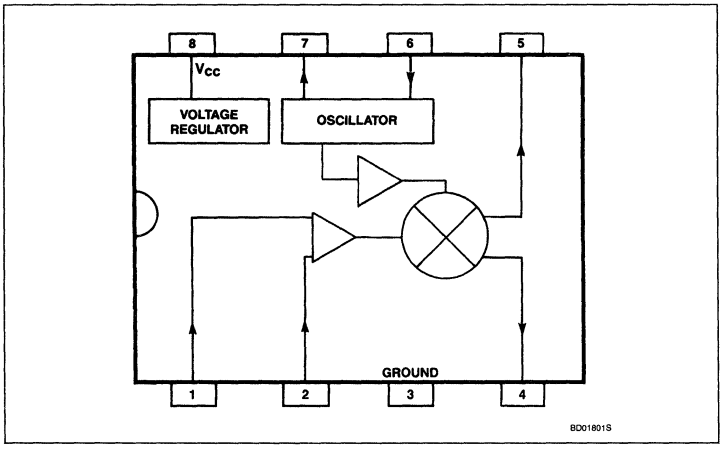
APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602N
8-Pin Plastic SO	0 to +70°C	NE602D
8-Pin Cerdip	0 to +70°C	NE602FE
8-Pin Plastic DIP	−40°C to +85°C	SA602N
8-Pin Plastic SO	−40°C to +85°C	SA602D
8-Pin Cerdip	−40°C to +85°C	SA602FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range NE602 SA602	0 to +70 −40 to +85	°C °C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0	6.0	dB
	Third-order intercept point	RF_{IN} = −45dBm: f_1 = 45.0 f_2 = 45.06		−15	−17	dBm
	Conversion gain at 45MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

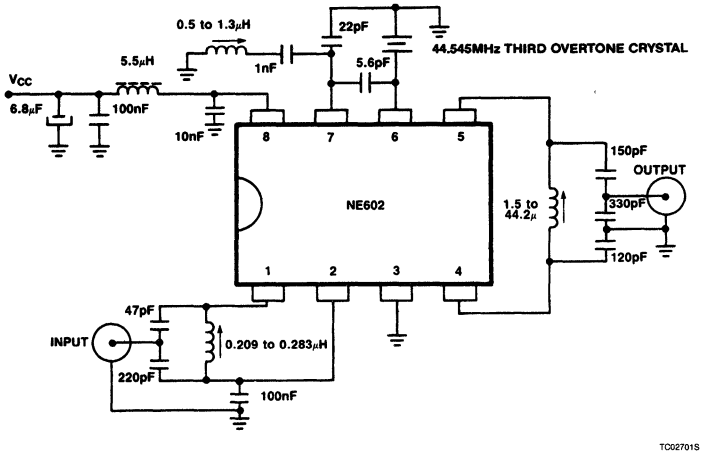


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE/SA602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602 is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio 2nd IF and demodulator, the SA602 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE602 should be appropriately scaled.

Double-Balanced Mixer and Oscillator NE/SA602

Besides excellent low power performance well into VHF, the NE/SA602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedence is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least 200mV$_{P-P}$.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

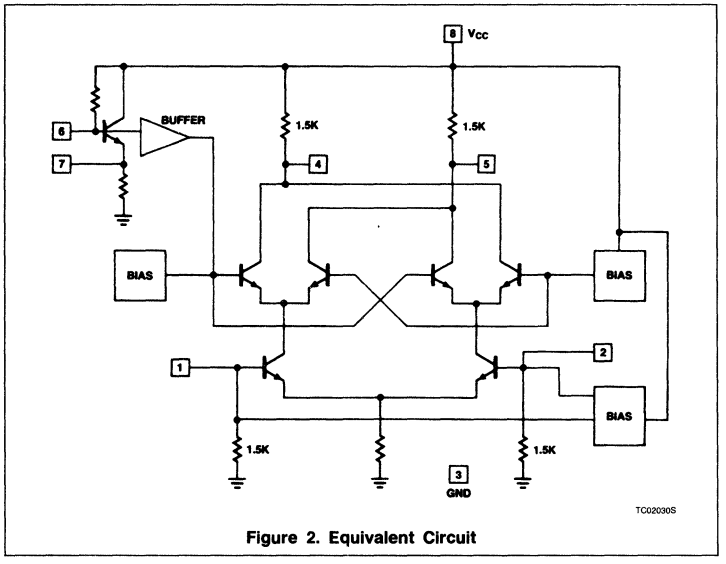
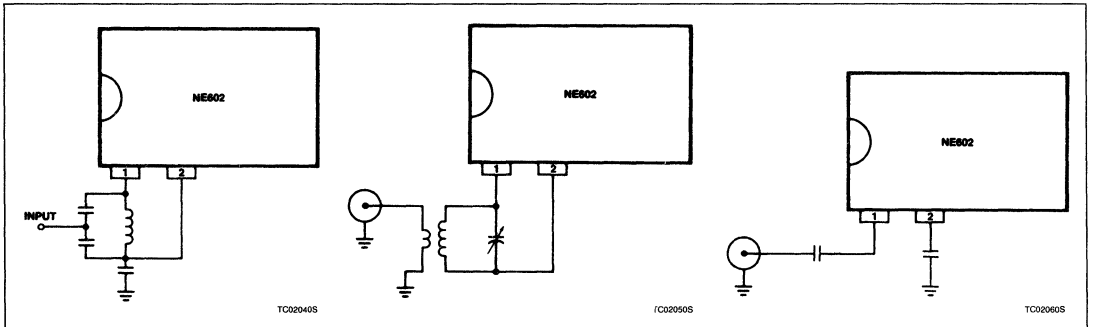


Figure 2. Equivalent Circuit

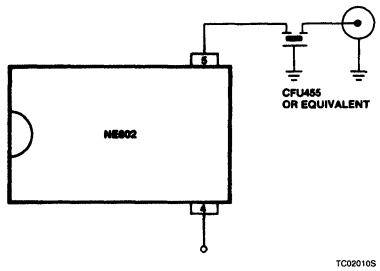


a. Single-Ended Tuned Input

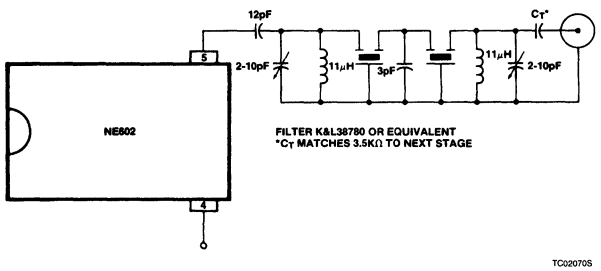
b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

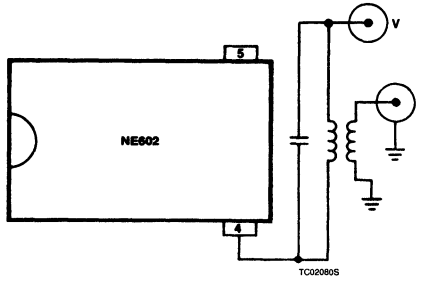
Figure 3. Input Configuration



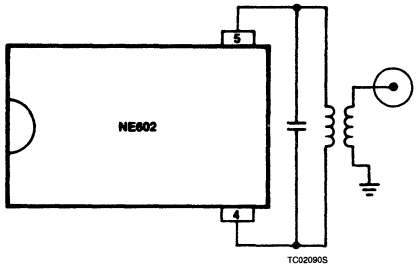
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

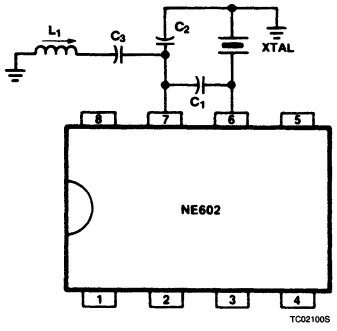


c. Single-Ended IFT

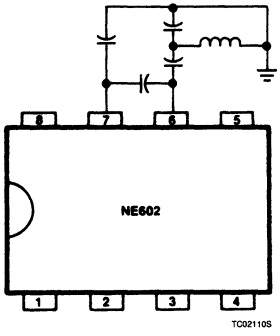


d. Balanced Output

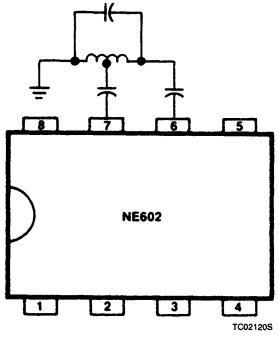
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

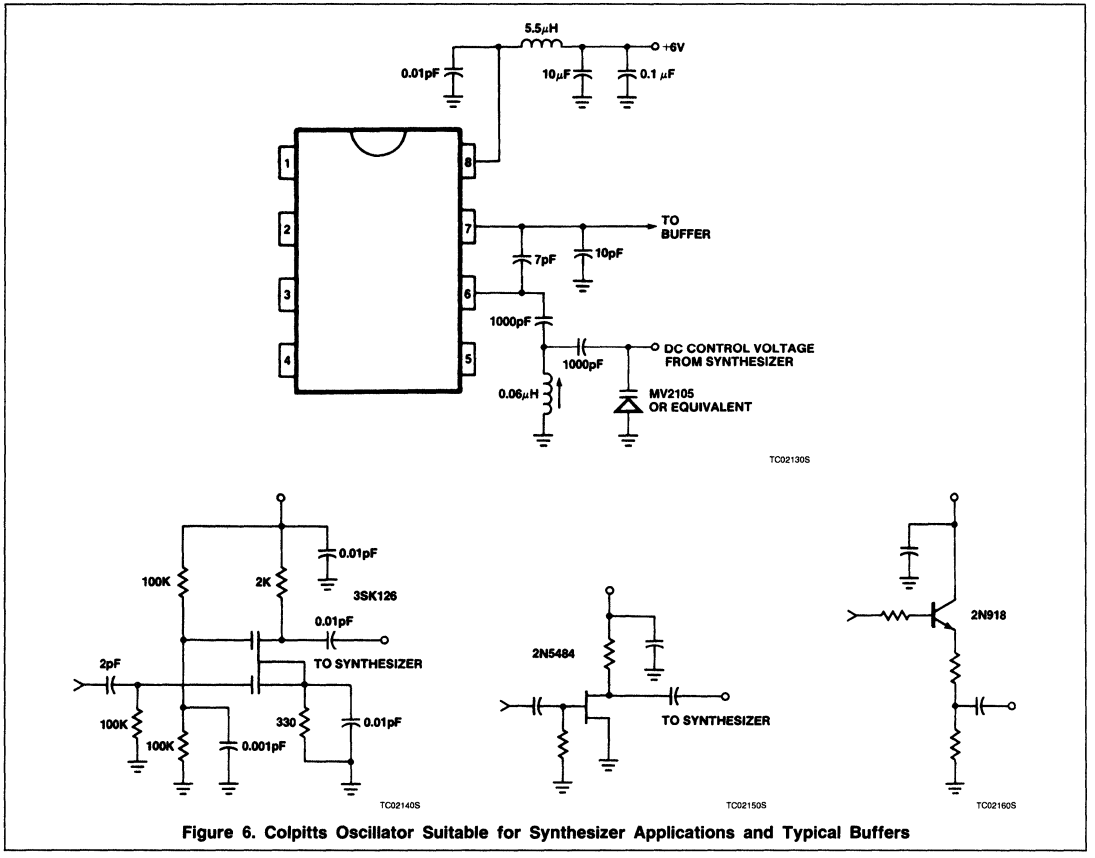


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

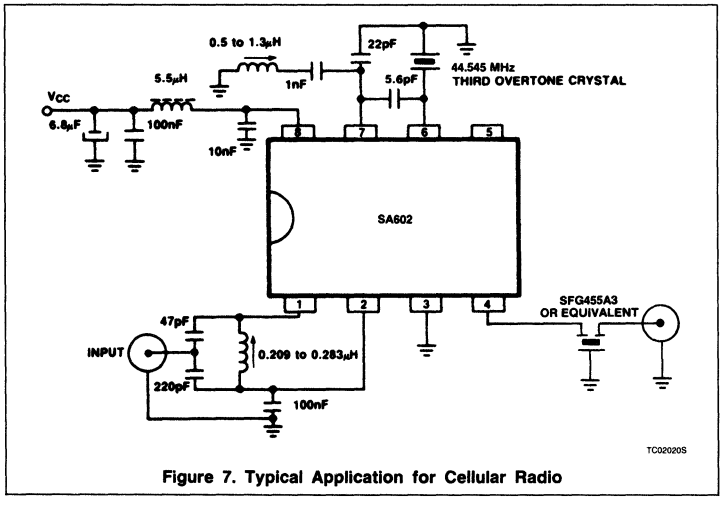


Figure 7. Typical Application for Cellular Radio

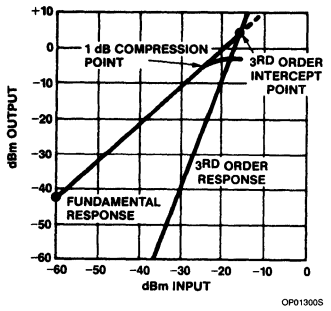


Figure 8. NE/SA602 Third-Order Intermod and 1dB Compression Point Performance

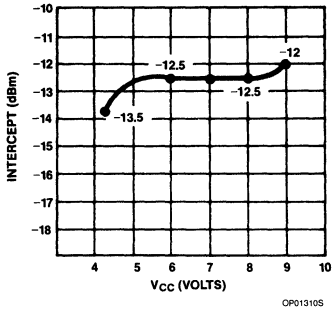


Figure 9. Input Third-Order Intercept Point vs V_{CC}

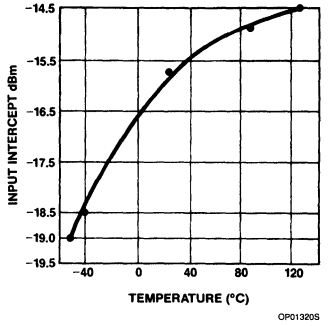


Figure 10. Third-Order Intercept Point vs Temperature

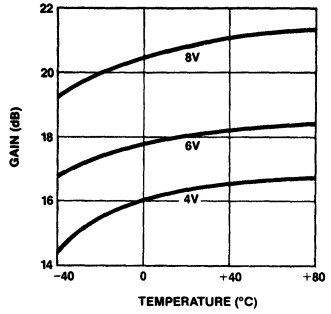


Figure 11

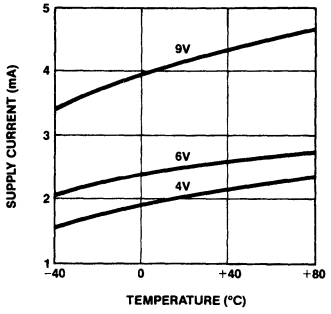


Figure 12

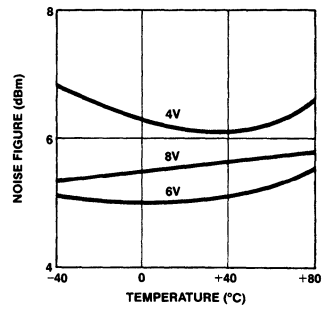


Figure 13

4

Signetics

AN1981
New Low Power Single Sideband Circuits

Application Note

Linear Products

by Robert J. Zavrel Jr.

INTRODUCTION

Several new integrated circuits now permit RF designers to resurrect old techniques of single-sideband generation and detection. The high cost of multi-pole crystal filters limits the use of the SSB mode to the most demanding applications, yet the advantages of SSB over full-carrier AM and FM are well-documented (Ref 1 & 2). The use of multi-pole filters can now be circumvented by reviving some older techniques without sacrificing performance. This has been made possible by the availability of some new RF and digital integrated circuits.

DESCRIPTION

Figure 1 shows the frequency spectrum of a 10MHz full-carrier double-sideband AM signal using a 1kHz modulating tone. This well-known type of signal is used by standard AM broadcast radio stations. Full-carrier AM's advantage is that envelope detection can be used in the receiver. Envelope detection is a simple and economical technique because it simplifies receiver circuitry. Figure 2 shows the time domain "envelope" of the same AM signal.

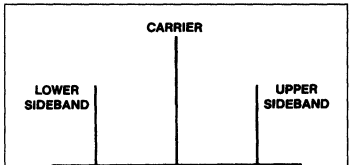


Figure 1. Frequency Domain Display of a 10MHz Carrier AM Modulated by a 1kHz Tone (Spectrum Analyzer Display)

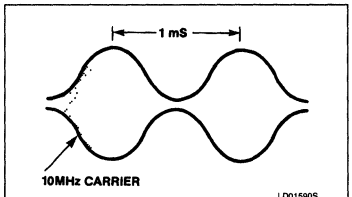


Figure 2. Time Domain Display of the Same Signal Shown in Figure 1. (Oscilloscope Display)

The 1kHz tone example of Figures 1 and 2 serves as a simple illustration of an AM signal. Typically, the sidebands contain complex waveforms for voice or data communications. In the full-carrier double sideband mode (AM), all the modulation information is contained in both sidebands, while the carrier "rides along" without contributing to the transfer of intelligence. Only one sideband without the carrier is needed to effectively transmit the modulation information. This mode is called "single-sideband suppressed carrier". Because of its reduced bandwidth, it has the advantages of improved spectrum utilization, better signal-to-noise ratios at low signal levels, and improved transmitter efficiency when compared with either FM or full-carrier AM. A finite frequency allocation using SSB can support three times the number of channels when compared with comparable FM or AM full-carrier systems.

There are three basic methods of single-sideband generation. All three use a balanced modulator to produce a double-sideband suppressed carrier signal. The undesired sideband is then removed by phase and amplitude nulling (the phasing method), high Q multi-pole filters (the filter method), or a "third" method which is a derivation of the phasing technique called here the "Weaver" method for the apparent inventor. The reciprocal of the generator functions is employed to produce sideband detectors. Generators start with audio and produce the SSB signal; detectors receive the SSB signal and reproduce the audio. Since the sideband signal is typically produced at radio frequencies, it can be amplified and applied to an antenna or used as a subcarrier.

Reproduction of the audio signal in a full-carrier AM receiver is simplified because the carrier is present. The signal envelope, which contains the carrier and the sidebands, is applied to a non-linear device (typically a diode). The effect of envelope detection is to multiply the sideband signal by the carrier; this results in the recovery of the audio waveform. The mathematical basis for this process can be understood by studying trigonometric identities.

Since the carrier is not present in the received SSB signal, the receiver must provide it for proper audio detection. This signal from the local oscillator (LO) is applied to a mixer (multiplier) together with the SSB signal and detection occurs. This technique is called product detection and is necessary in all SSB methods. A major problem in SSB receivers is the ability to maintain accurate LO frequencies to prevent spectral shifting of the audio signal. Errors in this frequency will result in a "Donald Duck" sound which can render the signal unintelligible for large frequency errors.

Theory of Single-Sideband Detection

Figures 3 through 8 illustrate the three methods of SSB generation and detection. Since they are reciprocal operations, the circuitry for generation and detection is similar with all three methods. Duplication of critical circuitry is easy to accomplish in transceiver applications by using appropriate switching circuits.

Figures 3 and 4 show the generation and detection techniques employed in the filter method. In the generator a double sideband signal is produced while the carrier is eliminated with the balanced modulator. Then the undesired sideband is removed with a high Q crystal bandpass filter. A transmit mixer is usually employed to convert the SSB signal to the desired output frequency. The detection scheme is the reciprocal. A receive mixer is used to convert the selected input frequency to the IF frequency, where the filter removes the undesired SSB response. Then the signal is demodulated in the product detector. A major drawback to the filter method is the fact that the filter is fixed-tuned to one frequency. This necessitates the receive and transmit mixers for multi-frequency operation.

Figures 5 and 6 show block diagrams of a generator and demodulator which use the phase method. Figure 6 also includes a mathematical model. The input signal (Cos(Xt)) is fed in-phase to two RF mixers where "X" is the frequency of the input signal. The other inputs to the mixers are fed from a local oscillator (LO) in quadrature (Cos(Yt) and Sin(Yt)), where "Y" is the frequency of the LO signal. By differentiating the output of one of the mixers and then summing with the other, a single sideband response is obtained. Switching the mixer output that is differentiated will change the selected sideband, upper (USB) or lower (LSB). In most cases the mixer outputs will be the audio passband (300 to 3000Hz). Differentiating the passband involves a 90 degree phase shift over more than three octaves. This is the most difficult aspect of using the phasing method for voice band SSB.

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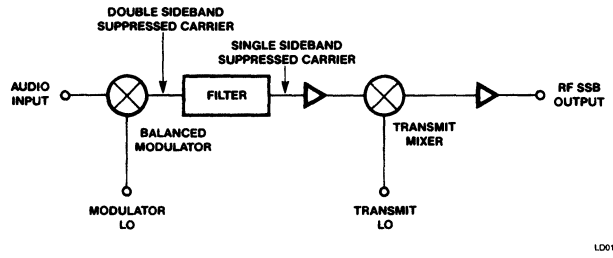

Figure 3. Filter Method SSB Generator

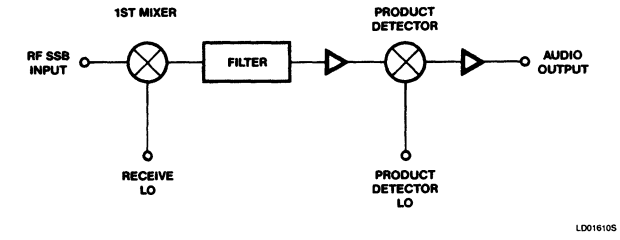

Figure 4. Filter Method SSB Detector

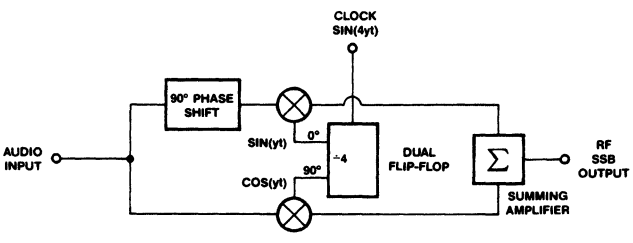

Figure 5. Phasing Method Generator

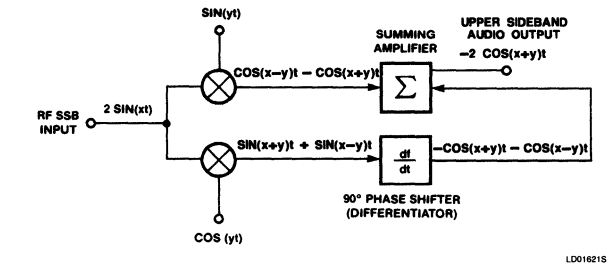

Figure 6. Phasing Method Detector with Simplified Mathematical Model

For voice systems, difficulty of maintaining accurate broadband phase shift is eliminated by the technique used in Figures 7 and 8. The "Weaver" method is similar to the phasing method because both require two quadrature steps in the signal chain. The difference between the two methods is that the Weaver method uses a low frequency (1.8kHz) subcarrier in quadrature rather than the broadband 90 degree audio phase shift. The desired sideband is thus "folded over" the 1.8kHz subcarrier and its energy appears between 0 and 1 5kHz. The undesired sideband appears 600Hz farther away between 2.1 and 4.8kHz. Consequently, sideband rejection is determined by a low-pass filter rather than by phase and amplitude balance. A very steep low-pass response in the Weaver method is easier to achieve than the very accurate phase and amplitude balance needed in the phasing method. Therefore, better sideband rejection is possible with the Weaver method than with the phasing method.

Quadrature Dual Mixer Circuits

One of the two critical stages in the phasing method and both critical stages in the Weaver method require quadrature dual mixer circuits. Figures 9 and 10 show two methods of obtaining quadrature LO signals for dual mixer applications. Other methods exist for producing quadrature LO signals, particularly use of passive LC circuits. LC circuits will not maintain a quadrature phase relationship when the operating frequency is changed. The two illustrated circuits are inherently broad-banded; therefore, they are far more flexible and do not require adjustment. These circuits are very useful for SSB circuits, but also can be applied to FSK, PSK, and QPSK digital communications systems.

The NE602 is a low power, sensitive, active, double-balanced mixer which shows excellent phase characteristics up to 200MHz. This makes it an ideal candidate for this and many other applications.

The circuit in Figure 9 uses a divide-by-four dual flip-flop that generates all four quadratures. Most of the popular dual flip-flops can be used in different situations. The HEF4013 CMOS device uses very little power and can maintain excellent phase integrity at clock rates up to several megahertz. Consequently, the HEF4013 can be used with the ubiquitous 455kHz intermediate frequency with excellent power economy. For higher clock rates (up to 120MHz for up to 30MHz operation), the fast TTL 74F74 is a good choice. It has been tested to 30MHz operating frequencies with good results (> 30 dB SSB rejection). At lower frequencies (5MHz) sideband rejection increases to nearly 40dB with the circuits shown. The ultimate low frequency rejection is mainly a function of the audio phase shifter.

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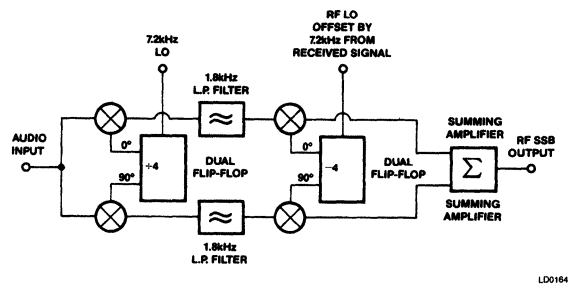

Figure 7. Weaver Method Generator

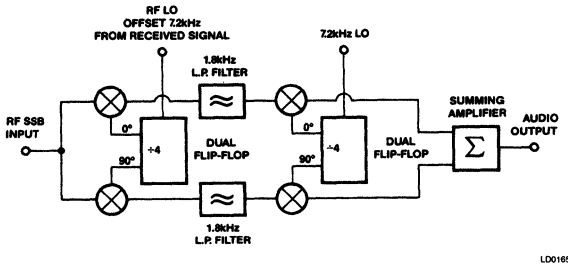

Figure 8. Weaver Method Detector

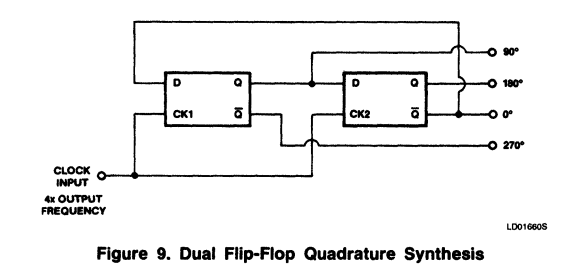

Figure 9. Dual Flip-Flop Quadrature Synthesis

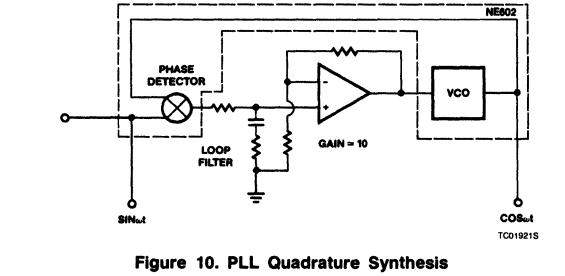

Figure 10. PLL Quadrature Synthesis

Better performance is possible by employing higher tolerance resistors and capacitors.

The circuit in Figure 10 shows another technique for producing a broadband quadrature phase shift for the LO. The advantage of this circuit over the flip-flops is that the clock frequency is identical to the operating frequency; however, phase accuracy is more difficult to achieve. A PLL will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is zero. The DC amplifier will help the accuracy of the quadrature condition by presenting gain to the VCO control circuit. The other problem that can arise is that PLL circuits tend to be noisy. Sideband noise is troublesome in both SSB and FM systems, but SSB is less sensitive to phase noise problems in the LO.

Figure 11 shows a circuit that is effective for driving the 74F74, or other TTL gates, with a signal generator or analog LO. The NE5205 provides about 20dB gain with 50Ω input and output impedances from DC to 450MHz. Minimum external components are required. The 1kΩ resistor is about optimum for "pulling" the input voltage down near the logic threshold. A 50Ω output level of 0dBm can be used to drive the NE5205 and 74F74 to 100MHz. Two NE5205s can be cascaded for even more sensitivity while maintaining extremely wide bandwidth. An advantage of using digital sources for the LO is that low-frequency power supply ripple will not cause hum in the receiver front end. This is a common problem in direct conversion designs.

Figure 12 shows the interface circuitry between the 74F74 and the NE602 LO ports. The total resistance reflects conservative current drain from the 74F74 outputs, while the tap on the voltage divider is optimized for proper NE602 operation. The low signal source impedance further helps maintain phase accuracy, and the isolation capacitor is miniature ceramic for DC isolation.

Audio Amplifiers and Switching

Using active mixers (NE602) in these types of circuits gives conversion gain, typically 18dB. More traditional applications use passive diode ring mixers which yield conversion loss, typically 7dB. Consequently, the detected audio level will be about 25dB higher when using the NE602. This fact can greatly reduce the first audio stage noise and gain requirements and virtually eliminate the "microphonic" effect common to direct conversion receivers. Traditional direct conversion receivers use passive audio LC filters at the mixer output and low noise, discrete JFETs or bipolars in the first stages. The very high audio sensitivity required by these amplifiers makes them respond to mechanical vibration—thus the "microphonics" result. The

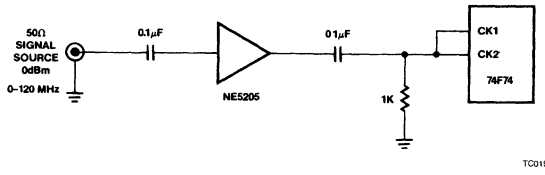

Figure 11. FAST TTL Driver from Analog Signal Source Using NE5205

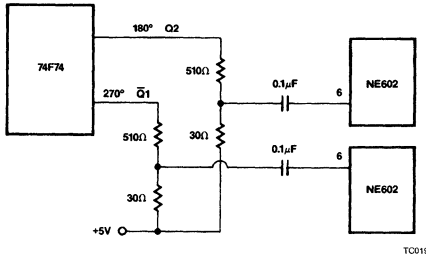

Figure 12. Interface Circuitry Between 74F74 and the NE602s

conversion gain allows use of a simple op amp stage (Figure 13) set up as an integrator to eliminate ultra-sonic and RF instability. The NE5534 is well known for its low noise, high dynamic range, and excellent audio characteristics (Reference 12) and makes an ideal audio amp for the 602 detector.

The sideband select function is easily accomplished with an HEF4053 CMOS analog switch. This triple double-pole switch drives the phase network discussed in the next section and also chooses one of two amplitude balance potentiometers, one for each sideband. Figure 14 illustrates this circuit. A buffer op amp is used with the two sideband select sections to reduce THD, maintain amplitude integrity, and not change the filter network input resistance values. The gain distribution within both legs of the receiver was found to be very consistent (within 1dB), thus the amplitude balance pots may be eliminated in less demanding applications. The NE602s have excellent gain as well as phase integrity.

Audio Phase Shift Circuits

The two critical stages for the phasing method are a dual quadrature mixer and a broadband audio phase shifter (differentiator). There are several broadband, phase shift techniques available Figure 15 shows an analog all-pass differential phase shift circuit. When the inputs are shorted and driven with a microphone circuit, the outputs will be 90 degrees out-of-phase over the 300 to 3000Hz band. This "splitting" and phase shift is necessary for the phasing generator. For phasing demodulation the two audio detectors are fed to the two inputs. The outputs are then summed to affect the sideband rejection and audio output

Standard 1% values are shown for the resistors and capacitors, although better gain tolerances can be obtained with 0.1% laser-trimmed integrated resistors. Polystyrene capacitors are preferred for better value tolerance and audio performance. Two quad op amps fit nicely into this application. One op amp serves as a switch buffer and the other three form a phasing section. The NE5514 quad op amps perform well for this application Careful attention to active filter configurations can yield highly linear and very high dynamic range circuits. Yet these characteristics are much easier to achieve at audio than the common IF RF frequencies. This fact, coupled with the lack of IF tuned circuits, shielding, and higher power requirements make audio IF systems attractive indeed:

Figure 16 shows a "tapped" analog delay circuit which uses weighted values of resistors to affect the phase shift. Excellent phase and amplitude balance are possible with this technique, but the price for components is high It should be stressed that the audio phase shift accuracy and amplitude balance are the limiting factors for SSB rejection when using the phase method; thus the higher cost may be justified in some applications.

Audio Processing

The summing amplifier is a conventional, inverting op amp circuit. It may be useful to configure a low-pass filter around this amplifier, and thus help the sharp audio filters which follow. Audio filters are necessary to shape the desired bandpass. Steep slope audio bandpass filters can be built from switched capacitor filters or from active filters requiring more op amps. Switched capacitor filters have the disadvantage of requiring a clock frequency in the RF range. Harmonics can cause interference problems if careful design techniques are not used. Also, better dynamic range is obtained with active filter techniques using "real" resistors although much work is being done with SCF's and performance is improving.

Direct conversion receivers rely heavily on audio filters for selectivity. Active analog or switched capacitor filters can produce the high Q and dynamic ranges necessary. Signal strength or "S-meters" can be constructed from the NE602's companion part, the NE604. The "RSSI" or "received signal strength indicator" function on the 604 provides a logarithmic response over a 90dB dynamic range and is easy to use at audio frequencies. Finally, the AGC (automatic gain control) function can also be performed in the audio section. Attack and delay times can be independently set with excellent distortion specifications with the NE572 compandor IC. The audio-derived AGC eliminates the need for gain controlling and RF stage, but relies on an excellent receiver front-end dynamic range. In ACSSB (Amplitude Compandored Single-Side Band) systems transmitter compression and receiver expansion are defined by individual system specifications.

Phasing-Filter Technique

High quality SSB radio specifications call for greater than 70dB sideband rejection. Using the circuits described in this paper for the phasing method, rejection levels of 35dB are obtainable with good reliability. Coupled with an inexpensive two-pole crystal or ceramic filter, the 70dB requirement is obtained. Also, the filtering ahead of the NE602 greatly improves the intermodulation performance of the receiver Figure 17 shows a complete SSB receiver using the Phasing-Filter technique. The sensitivity of the NE602 allows low gain stages and low power consumption for the RF amplifier and first mixer. A new generation of low power CMOS frequency synthesizers is now available from several manufacturers including the TDD1742 and dual chip HEF4750/51 solutions.

Direct Conversion Receiver

The antenna can be connected directly to the input of the NE602 (via a bandpass filter) to form a direct conversion SSB receiver using

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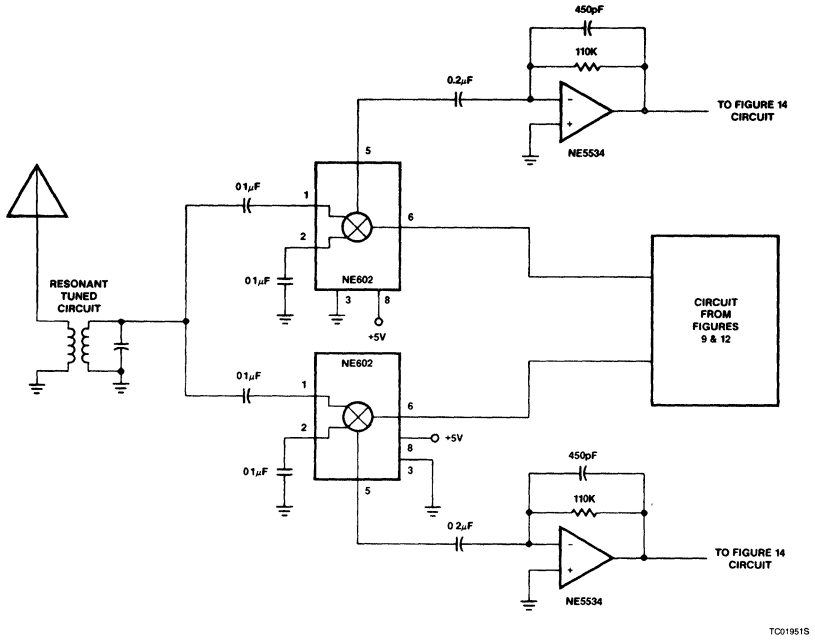

Figure 13. Phasing Method Detector for Direct Conversion Receiver

the phasing method. 35dB sideband rejection is adequate for many applications, particularly where low power and portable battery operation are required. Figure 13 shows a typical circuit for direct conversion applications.

There are many other applications which can make use of SSB technology. Cordless telephones use FM almost exclusively. Eavesdropping could be greatly reduced for systems which employ SSB rather than FM. Furthermore, the better signal-to-noise ratio will extend the range, and battery life will be extended because no carrier is needed.

SSB is also used for subcarriers on microwave links and coaxial lines. Telephone communications networks that use SSB are called FDM or Frequency Domain Multiplex systems. The low power and high sensitivity of the NE602 can offer FDM designers new techniques for system configuration.

Weaver Method Receiver Techniques

The same quadrature dual mixer can be used for the first stage in both the phasing and Weaver method receiver. The subcarrier stage in the Weaver method receiver can use CMOS analog switches (HEF4066) for great power economy. Figure 18 shows a circuit for the subcarrier stage. A 1.8kHz subcarrier requires a 7.2kHz clock frequency. If switched capacitor filters are used for the low-pass and audio filters, a single clock generator can be used for all circuits with appropriate dividers. Furthermore, if the receiver is used as an IF circuit, the fixed LO signal could also be derived from the same clock. This has the added advantage that harmonics from the various circuits will not interfere with the received signal.

Results

The circuit shown in Figures 13, 14, and 15 has a 10dB S/N sensitivity of 0.5μV with a dynamic range of about 80dB. Single-tone audio harmonic distortion is below 0.05% with two-tone intermodulation products below 55dB at RF input levels only 5dB below the 1dB compression point. The sideband rejection is about 38dB at a 9MHz operating frequency. The good audio specifications are a side benefit to direct conversion receivers. When used with inexpensive ceramic or crystal filters, this circuit can provide these specifications with > 70dB sideband rejection.

Conclusions

Single sideband offers many advantages over FM and full-carrier double-sideband modulation These advantages include: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Many of the disadvantages can now be overcome by using old techniques and new state-of-the-art integrated circuits. Effective and inexpensive circuits can use direct conversion techniques with good results. 35dB sideband rejection with less than 1μV sensitivity is obtained with the NE602 circuits. 70dB sideband rejection and superior sensitivity are obtained by using phasing-filter techniques. Either the phasing or Weaver methods can be used in either the direct conversion or IF section applications. The filter and phase-filter methods can be used in only the IF application.

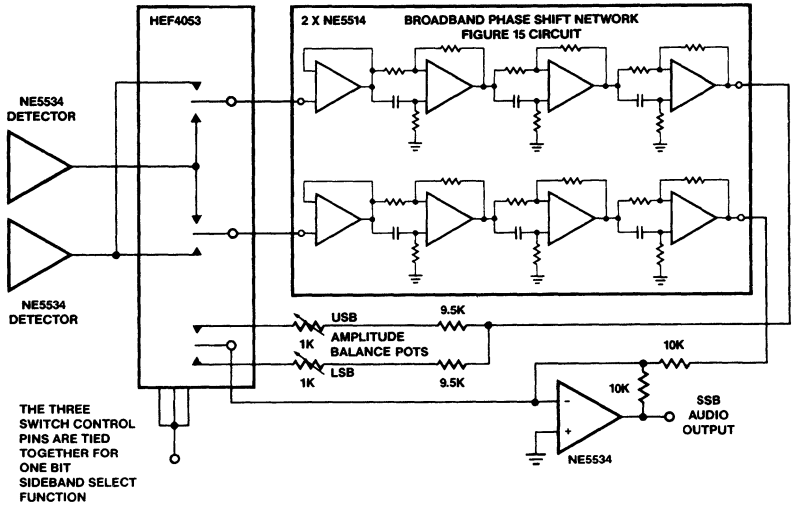

Figure 14. Sideband Select Switching Function

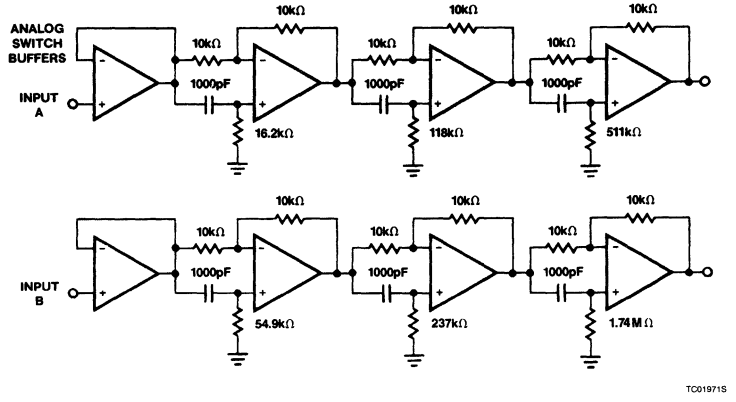

Figure 15

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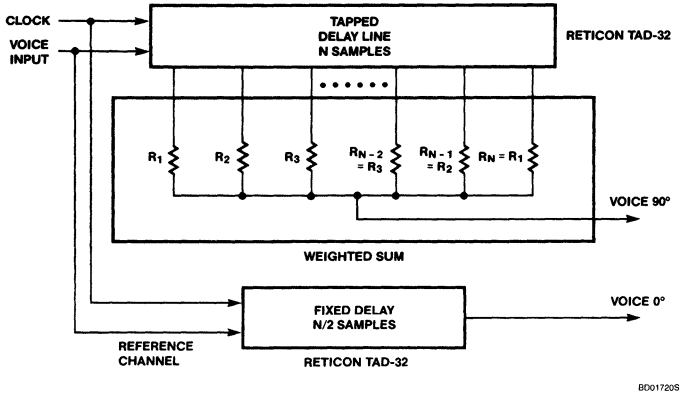
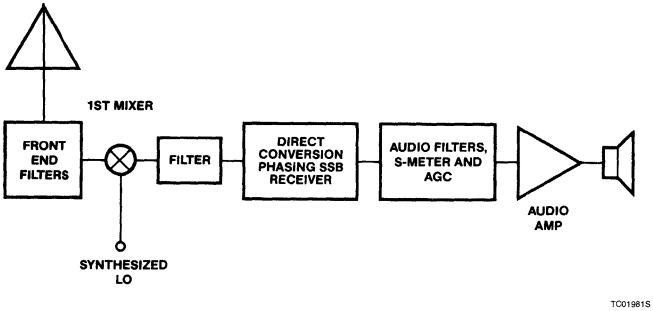


Figure 16. Broadband 90° Audio Phase Shift Technique Using Tapped Delay Line (Reference 4)



Receivers built using this technique can exhibit excellent characteristics without resorting to expensive multi-pole filters or an IF Amplifier chain

Figure 17. Complete Phasing-Filter Receiver

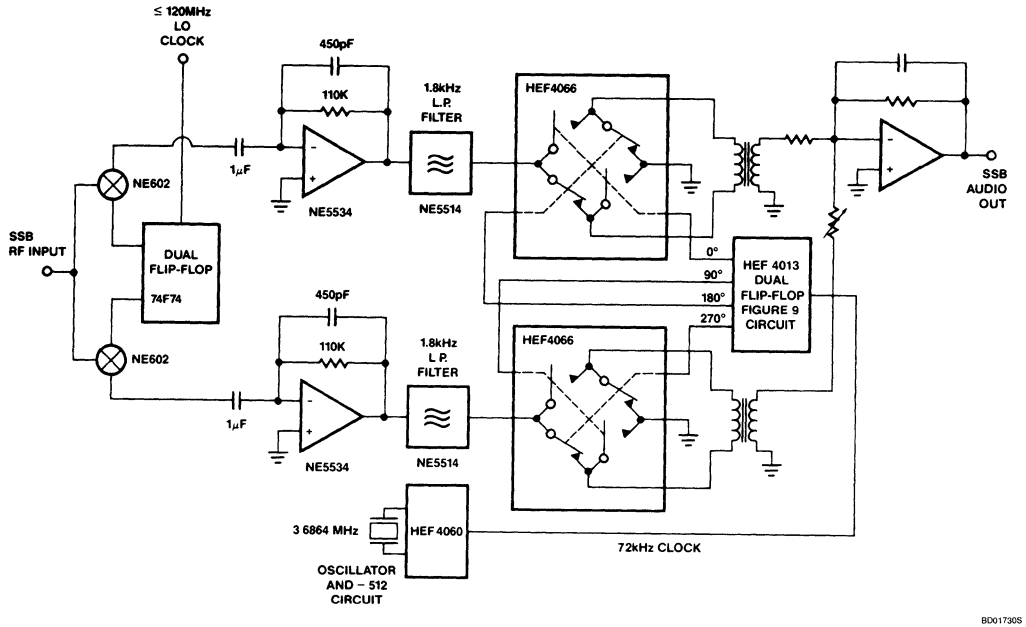


Figure 18. Weaver Method Receiver Concept Example For ⩽30MHz Operation

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Signetics

AN1982

Applying the Oscillator of the NE602 in Low Power Mixer Applications

Linear Products

Application Note

by Donald Anderson

INTRODUCTION

For the designer of low power RF systems, the Signetics NE602 mixer/oscillator provides mixer operation beyond 500MHz, a versatile oscillator capable of operation to 200MHz, and conversion gain, with only 2.5mA total current consumption. With a proper understanding of the oscillator design considerations, the NE602 can be put to work quickly in many applications.

DESCRIPTION

Figure 1 shows the equivalent circuit of the device. The chip is actually three subsystems: A Gilbert cell mixer (which provides differential input gain), a buffered emitter follower oscillator, and RF current and voltage regulation. Complete integration of the DC bias permits simple and compact application. The simplicity of the oscillator permits many configurations.

While the oscillator is simple, oscillator design isn't. This article will not address the rigors of oscillator design, but some practical guidelines will permit the designer to accomplish good performance with minimum difficulty.

Either crystal or LC tank circuitry can be employed effectively. Figure 2 shows the four most commonly used configurations in their most basic form.

In each case the Q of the tank will affect the upper frequency limits of oscillation: the higher the Q the higher the frequency. The NE602 is fabricated with a 6GHz process, but the emitter resistor from Pin 7 to ground is nominally 20k. With 0.25mA typical bias current, 200MHz oscillation can be achieved with high Q and appropriate feedback.

The feedback, of course, depends on the Q of the tank. It is generally accepted that a minimum amount of feedback should be used, so even if the choice is entirely empirical, a good trade-off between starting characteristics, distortion, and frequency stability can be quickly determined.

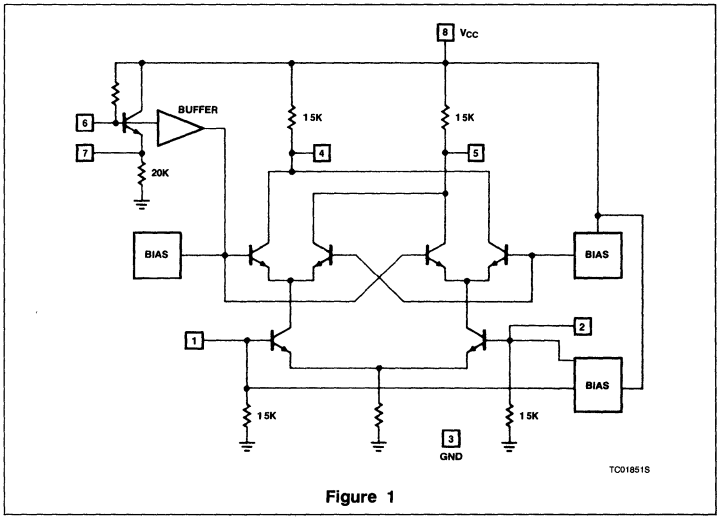
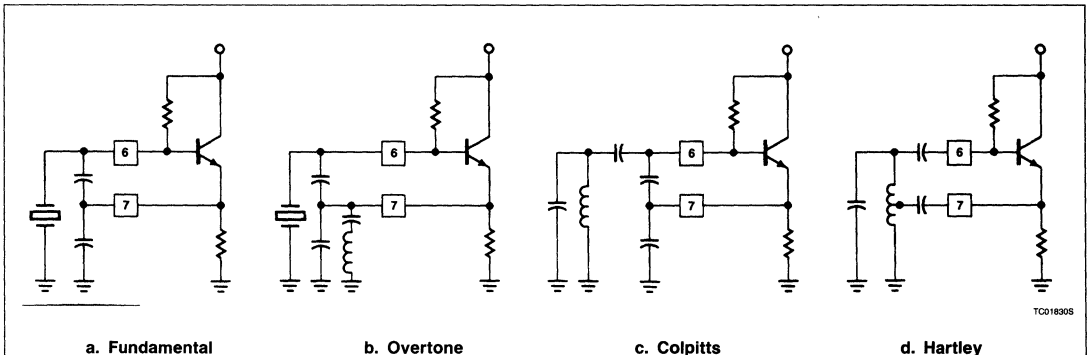


Figure 1



a. Fundamental Crystal **b. Overtone Crystal** **c. Colpitts L/C Tank** **d. Hartley L/C Tank**

Figure 2

Applying the Oscillator of the NE602 in Low Power Mixer Applications

AN1982

Crystal Circuit Considerations

Crystal oscillators are relatively easy to implement since crystals exhibit higher Q's than LC tanks. Figure 3 shows a complete implementation of the SA602 (extended temperature version) for cellular radio with a 45MHz first IF and 455kHz second IF.

The crystal is a third overtone parallel mode with 5pF of shunt capacitance and a trap to suppress the fundamental.

LC Tank Circuits

LC tanks present a little greater challenge for the designer. If the Q is too low, the oscillator won't start. A trick which will help if all else fails is to shunt Pin 7 to ground with a 22k resistor. In actual applications this has been effective to 200MHz with high Q ceramic capacitors and a tank inductor of 0.08μH and a Q of 90. Smaller resistor value will upset DC bias because of inadequate base bias at the input of the oscillator. An external bias resistor could be added from V_{CC} to Pin 6, but this will introduce power supply noise to the frequency spectrum.

The Hartley configuration (Figure 2D) offers simplicity. With a variable capacitor tuning the tank, the Hartley will tune a very large range since all of the capacitance is variable. Please note that the inductor must be coupled to Pin 7 with a low impedance capacitor. The Colpitts oscillator will exhibit a smaller tuning range since the fixed feedback capacitors limit variable capacitance range; however, the Colpitts has good frequency stability with proper components.

Synthesized Frequency Control

The NE602 can be very effective with a synthesizer if proper precautions are taken to minimize loading of the tank and the introduction of digital switching transients into the spectrum. Figure 4 shows a circuit suitable for aircraft navigation frequencies (108 – 118MHz) with 10.7MHz IF.

The dual gate MOSFET provides a high degree of isolation from prescaler switching spikes. As shown in Figure 4, the total current consumption of the NE602 and 3SK126 is typically 3mA. The MOSFET input is from the emitter of the oscillator transistor to avoid loading the tank. The Gate 1 capacitance of the MOSFET in series with the 2pF coupling capacitor adds slightly to the feedback capacitance ratio. Use of the 22k resistor at Pin 7 helps assure oscillation without upsetting DC bias.

For applications where optimum buffering of the tank, or minimum current are not mandatory, or where circuit complexity must be minimized, the buffers shown in Figure 5 can be considered.

The effectiveness of the MRF931 (or other VHF bipolar transistors) will depend on frequency and required input level to the prescaler. A bipolar transistor will generally provide the least isolation. At low frequencies the transistor can be used as an emitter follower, but by VHF the base emitter junction will start to become a bidirectional capacitor and the buffer is lost.

The 2N5484 has an IDSS of 5mA max. and the 2SK126 has IDSS of 6mA max. making them suitable for low parts count, modest current buffers. The isolation is good

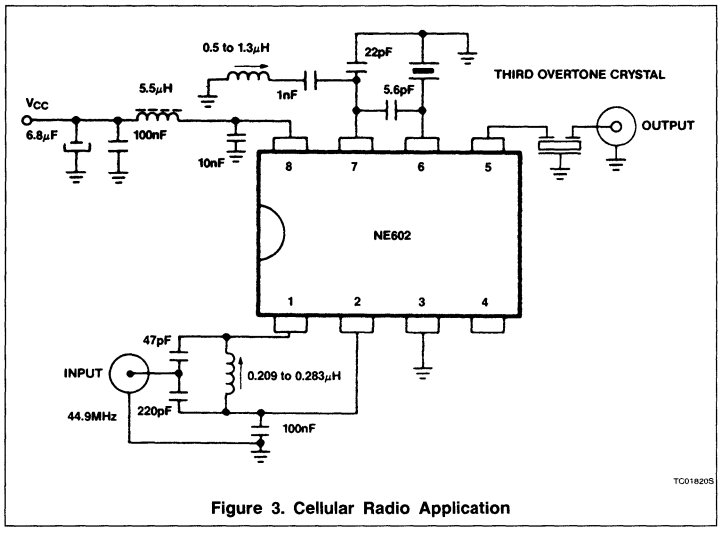


Figure 3. Cellular Radio Application

Injected LO

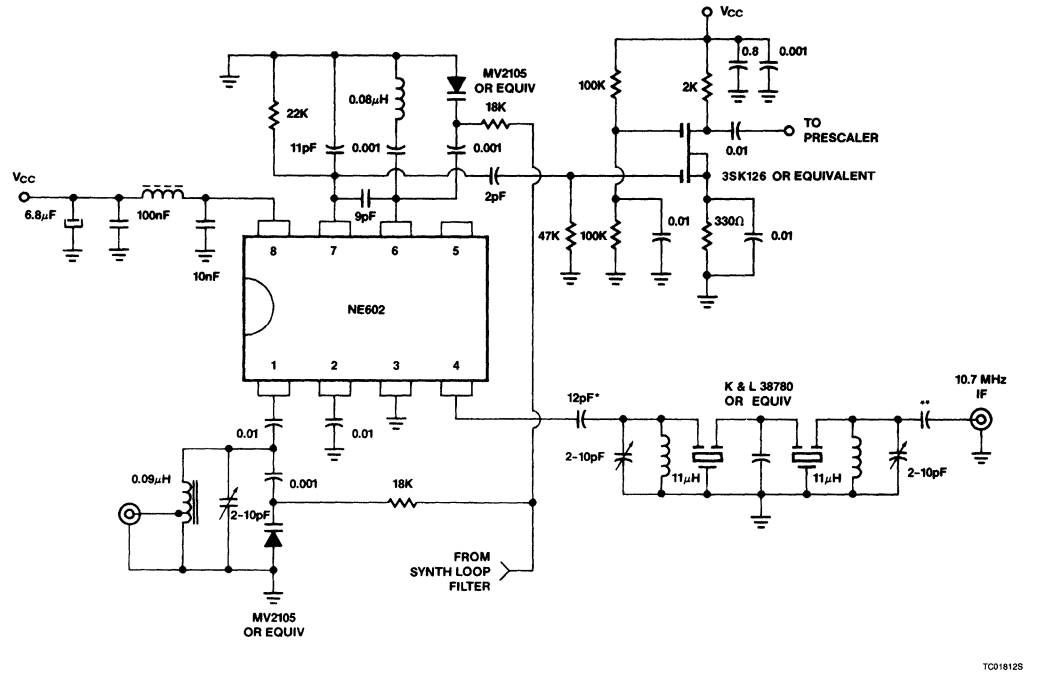
If the application calls for a separate local oscillator, it is acceptable to capacitively-couple 200 to 300mV at Pin 6

Summary

The NE602 can be an effective low power mixer at frequencies to 500MHz with oscillator operation to 200MHz. All DC bias is provided internal to the device so very compact designs are possible. The internal bias sets the oscillator DC current at a relatively low level so the designer must choose frequency selective components which will not load the transistor. If the guidelines mentioned are followed, excellent results will be achieved.

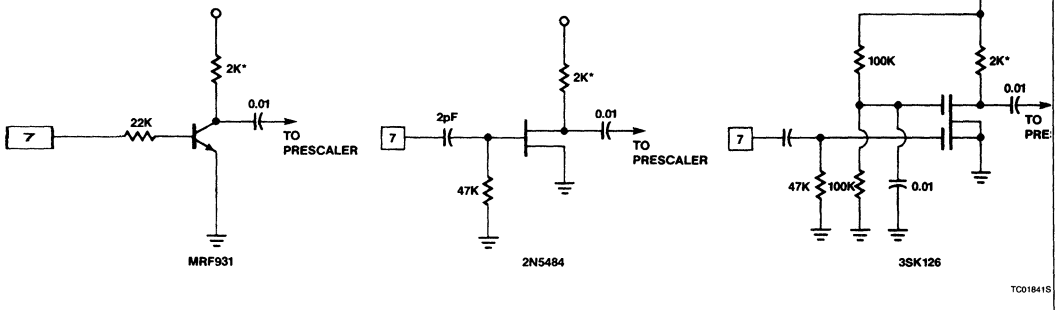
Applying the Oscillator of the NE602 in Low Power Mixer Applications

AN1982



NOTES:
* Permits impedance match of NE602 output, ie 1 5K//3pF to 3 5K filter impedance
** Choose for impedance match to next stage

Figure 4



NOTE:
* 2K or as necessary for current limits or prescaler impedance match

Figure 5

Signetics

NE612
Double-Balanced Mixer and Oscillator

Product Specification

Linear Products

DESCRIPTION

The NE612 is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

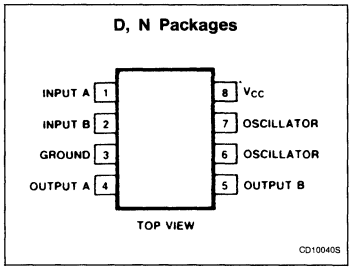
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

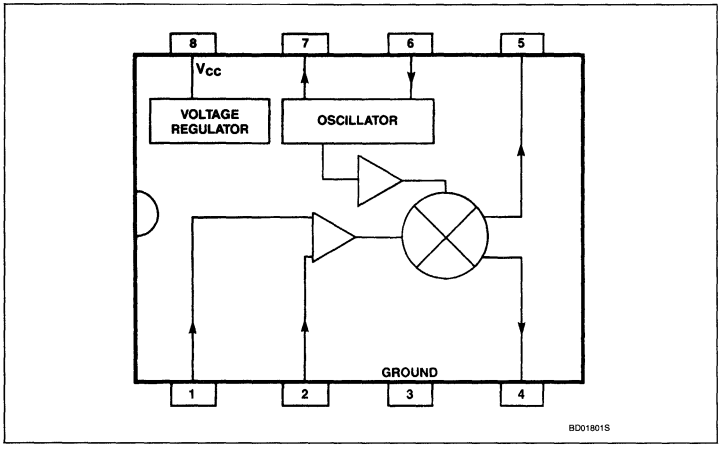
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LANs**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



Double-Balanced Mixer and Oscillator — NE612

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612N
8-Pin Plastic SO	0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4 5		8.0	V
	DC current drain			2 4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 49MHz			5.0		dB
	Third-order intercept point at 49MHz	$RF_{IN} = -45dBm$		−15		dBm
	Conversion gain at 49MHz		14	18		dB
R_{IN}	RF input resistance		1 5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

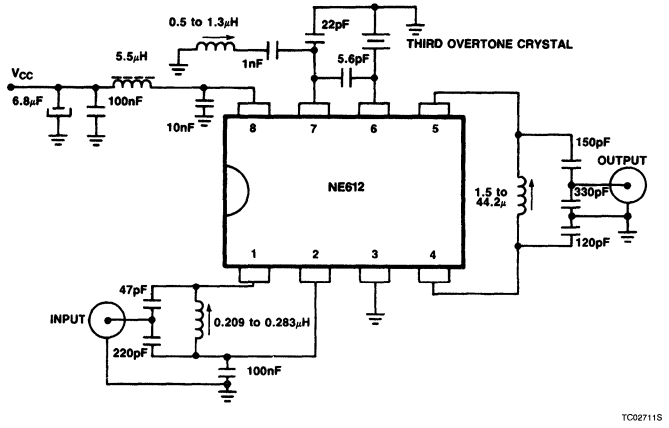


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Double-Balanced Mixer and Oscillator | NE612

Besides excellent low power performance well into VHF, the NE612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be $200mV_{P-P}$ minimum to $300mV_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits Figure 5a is appropriate for cordless telephones. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

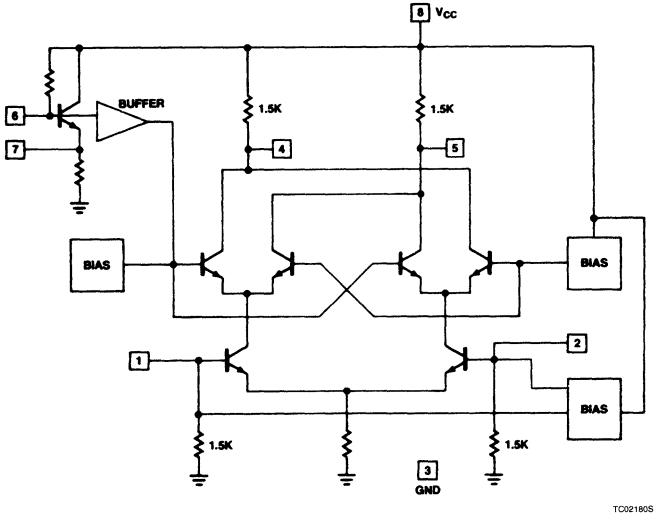
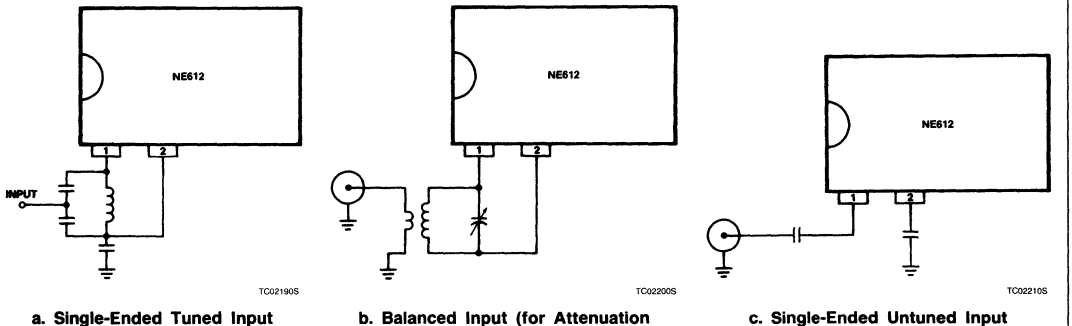


Figure 2. Equivalent Circuit

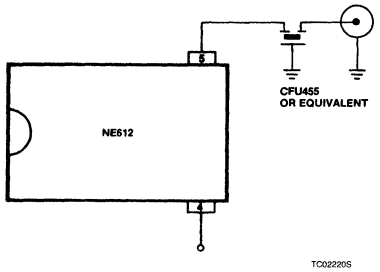


a. Single-Ended Tuned Input

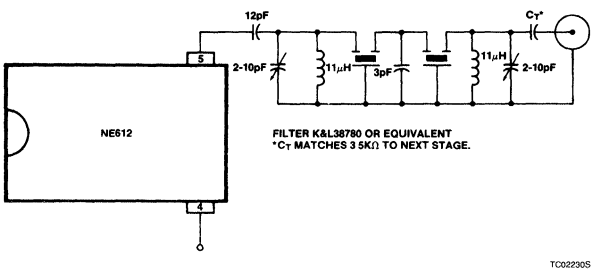
b. Balanced Input (for Attenuation of Second Order Products)

c. Single-Ended Untuned Input

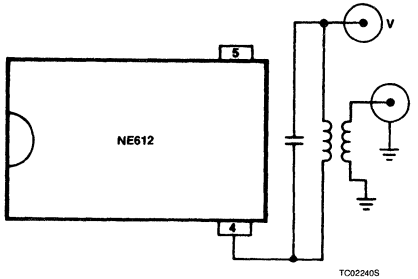
Figure 3. Input Configuration



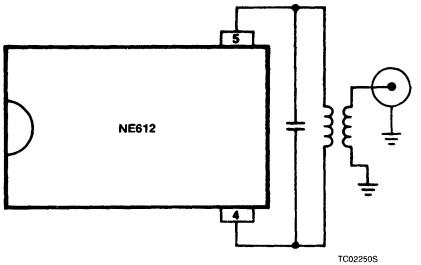
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

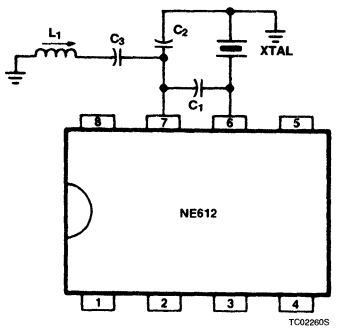


c. Single-Ended IFT

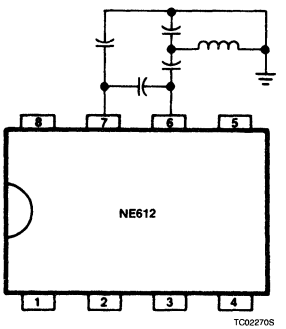


d. Balanced Output

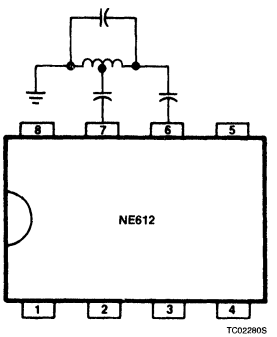
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

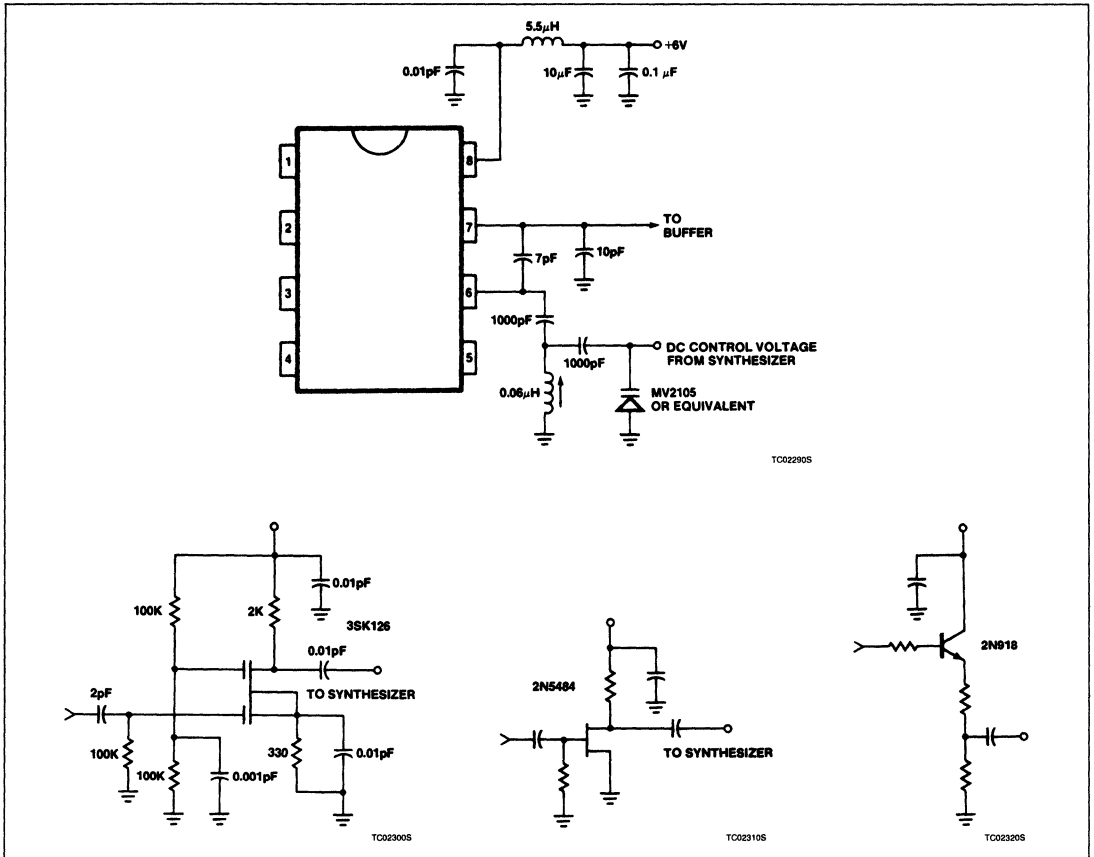


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

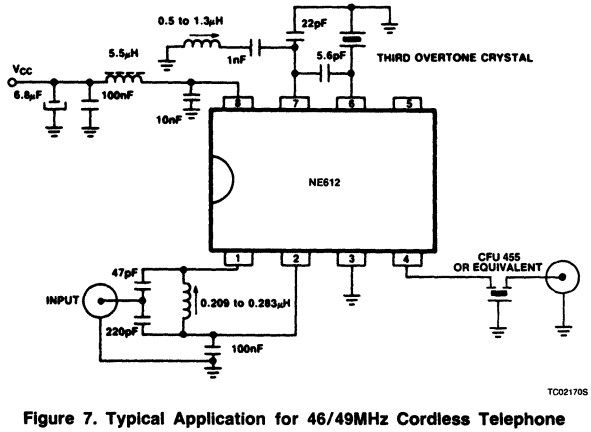


Figure 7. Typical Application for 46/49MHz Cordless Telephone

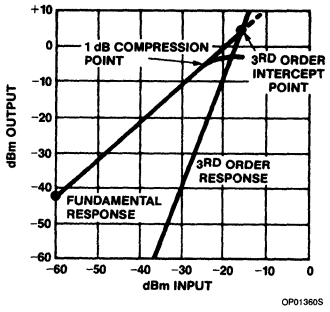


Figure 8. NE612 Third-Order Intermod and 1dB Compression Point Performance

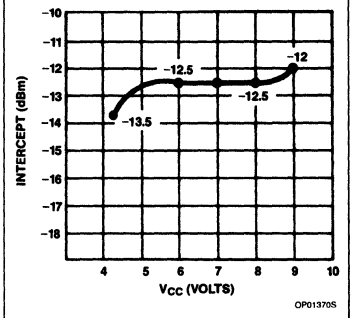


Figure 9. Input Third-Order Intercept Point vs V_{CC}

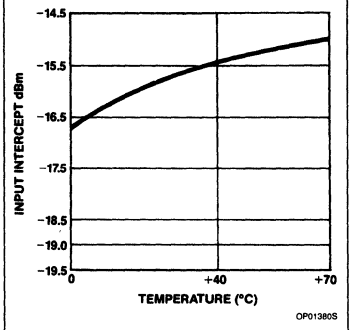


Figure 10. Third-Order Intercept Point vs Temperature

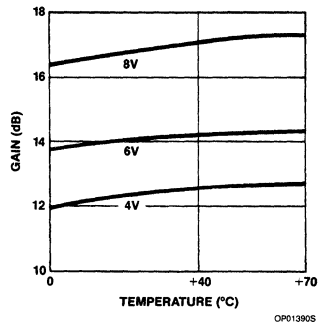


Figure 11

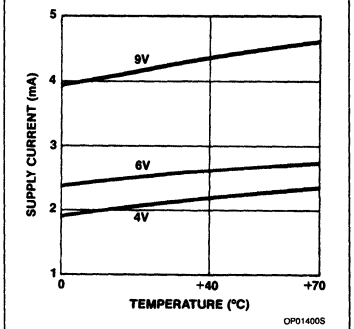


Figure 12

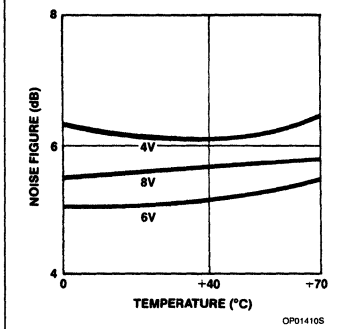


Figure 13

Signetics

TDA1574
FM Front-End IC

Product Specification

Linear Products

DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the RF/IF section of car radios and home receivers. The circuit comprises a mixer, oscillator and a linear IF amplifier for signal processing, plus the following additional features.

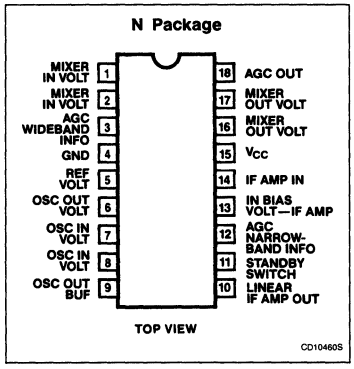
FEATURES

- **Keyed automatic gain control (AGC)**
- **Regulated reference voltage**
- **Buffered oscillator output**
- **Electronic standby switch**
- **Internal buffered mixer driving**

APPLICATIONS

- **FM radio**
- **Radio communication**
- **Auto radio**
- **High-performance stereo FM**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT102HE)	0 to +70°C	TDA1574N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC} = V_{15-4}$	Supply voltage (Pin 15)	18	V
$V_{16,\ 17-4}$	Mixer output voltage (Pins 16 and 17)	35	V
V_{11-4}	Standby switch input voltage (Pin 11)	23	V
V_{5-4}	Reference voltage (Pin 5)	7	V
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C
θ_{JA}	Thermal resistance from junction to ambient (in free air)	80	°C/W

NOTE:
1. All Pins are short-circuit protected to ground.

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tank-transfer function to obtain low-order 2nd harmonics.

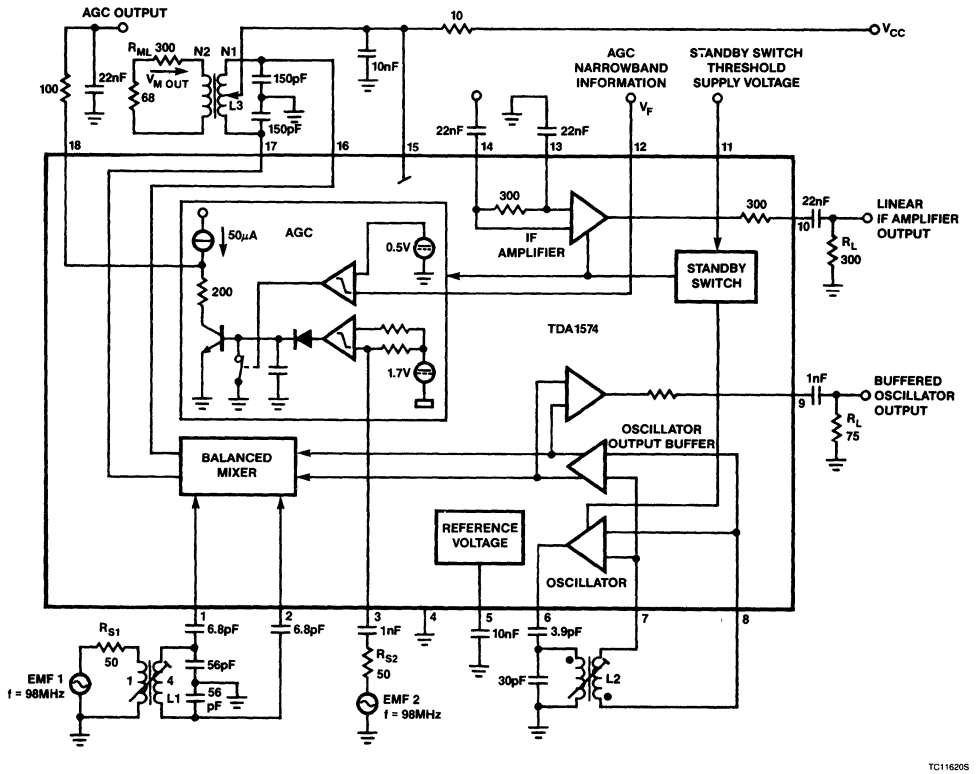
Linear IF amplifier

The IF amplifier is a one-stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage, The level-dependent, current sinking output has an active load which sets the AGC threshold.

BLOCK DIAGRAM AND TEST CIRCUIT



NOTES:
Coil Data
L1 TOKO MC-108, 514HNE-150023S14, L = 0 078μH
L2 TOKO MC-111, E516HNS-200057, L = 0 08μH
L3 TOKO coil set 7P, N1 = 5 5 + 5 5 turns, N2 = 4 turns

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{15-4} = 8.5V$; $T_A = 25°C$; measured in test circuit (Block Diagram), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 15)					
$V_{CC} = V_{15-4}$	Supply voltage	7		16	V
$I_{CC} = I_{15}$	Supply current (except mixer)	16	23	30	mA
V_{5-4}	Reference voltage (Pin 5)	4.0	4.2	4.4	V
Mixer					
	DC characteristics				
$V_{1,\ 2-4}$	Input bias voltage (Pins 1 and 2)		1		V
$V_{16,\ 17-4}$	Output voltage (Pins 16 and 17)	4		35	V
$I_{16} + I_{17}$	Output current (Pin 16 + Pin 17)		4.5		mA
	AC characteristics (f_I = 98MHz)				
NF	Noise figure		9		dB
NF	Noise figure including transforming network		11		dB
$EMF1_{IP3}$	3rd order intercept point		115		dBμV
	Conversion power gain				
Gp	$10 \log \frac{4(V_{M(out)}\ 10.7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$		14		dB
$R_{1,\ 2-4}$	Input resistance (Pins 1 and 2)		12		Ω
$C_{16,\ 17}$	Output capacitance (Pins 16 and 17)		13		pF
Oscillator					
	DC characteristics				
$V_{7,\ 8-4}$	Input voltage (Pins 7 and 8)		1.3		V
V_{6-4}	Output voltage (Pin 6)		2		V
	AC characteristics (f_{OSC} = 108.7MHz)				
	Residual FM (Bandwidth 300Hz to 15kHz);				
Δf	de-emphasis = 50μs		2.2		Hz
Linear IF amplifier					
	DC characteristics				
V_{13-4}	Input bias voltage (Pin 13)		1.2		V
V_{10-4}	Output voltage (Pin 10)		3.5		V
	AC characteristics (f_I = 10.7MHz)				
	Input impedance				
R_{14-13}		240	300	360	Ω
C_{14-13}			13		pF
	Output impedance				
R_{10-4}		240	300	360	Ω
C_{10-4}			3		pF
	Voltage gain				
G_{VIF}	$20 \log \frac{V_{10-4}}{V_{14-13}}$	27	30		dB
ΔG_{VIF}	$T_A = -40$ to $+85°C$		0		dB
	1 dB compression point (RMS value)				
$V_{10-4RMS}$	at V_{CC} = 8.5V		900		mV
$V_{10-4RMS}$	at V_{CC} = 7.5V		500		mV
	Noise figure				
NF	at $R_S = 300\Omega$		6.5		dB

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{15-4} = 8.5V$; $T_A = 25°C$; measured in test circuit (Block Diagram), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Keyed AGC					
	DC characteristics				
V_{18-4}	Output voltage range (Pin 18)	0.5		$V_{CC}-0.3$	V
	AGC output current				
	at $I_3 = \phi$ or				
$-I_{18}$	$V_{12-4} = 450mV$; $V_{18-4} = V_{CC}/2$	25	50	100	μA
	at $V_{3-4} = 2V$ and				
I_{18}	$V_{12-4} = 1V$; $V_{18-4} = V_{15-4}$	2		5	mA
	Narrow-band threshold				
V_{18-4}	at $V_{3-4} = 2V$; $V_{12-4} = 550mV$			1	V
V_{18-4}	at $V_{3-4} = 2V$; $V_{12-4} = 450mV$	$V_{CC}-0.3$			V
	AC characteristics ($f_I = 98MHz$)				
	Input impedance				
R_{3-4}			4		kΩ
C_{3-4}			3	–	pF
	Wide-band threshold (RMS value)				
	(see Figures 1, 2, 3 and 4)				
$EMF2_{RMS}$	at $V_{12-4} = 0.7V$; $V_{18-4} = V_{CC}/2$; $I_{18} = 0$		19		mV
Oscillator output buffer (Pin 9)					
V_{9-4}	DC output voltage		6.0		V
	Oscillator output voltage (RMS value)				
V_{9-4RMS}	at $R_L = \infty$		110		mV
V_{9-4RMS}	at $R_L = 75Ω$	25			mV
R_{9-15}	DC ouput impedance		2.5		kΩ
	Signal purity				
THD	total harmonic distortion		−15		dBC
	Spurious frequencies				
f_S	at EMF1 = 1V; $R_{S1} = 50Ω$		−35		dBC
Electronic standby switch (Pin 11) Oscillator; linear IF amplifier; AGC at $T_A = -40$ to $+85°C$					
	Input switching voltage				
V_{11-4}	for threshold ON; $V_{18-4} \geqslant V_{CC}-3V$	0		2.3	V
V_{11-4}	for threshold OFF; $V_{18-4} \leqslant 0.5V$	3.3		23	V
	Input current				
$-I_{11}$	at ON condition; $V_{11-4} = 0V$			150	μA
I_{11}	at OFF condition; $V_{11-4} = 23V$			10	μA
	Input voltage				
V_{11-4}	at $I_{11} = \phi$			4.4	V

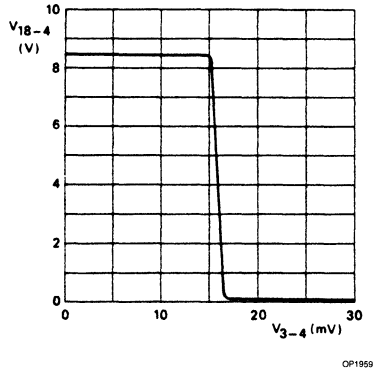


Figure 1. Keyed AGC Output Voltage V_{18-4} as a Function of RMS Input Voltage V_{3-4}. Measured in Test Circuit (Block Diagram) at $V_{12-4} = 0.7V$; $I_{18} = \phi$

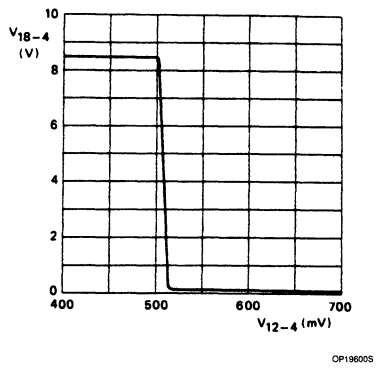


Figure 2. Keyed AGC Output Voltage V_{18-4} as a Function of Input Voltage V_{12-4}. Measured in Test Circuit (Block Diagram) at $V_{3-4} = 2V$; $I_{18} = \phi$

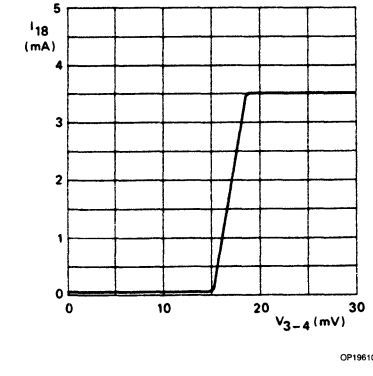


Figure 3. Keyed AGC Output Current I_{18} as a Function of RMS Input Voltage V_{3-4}. Measured in Test Circuit (Block Diagram) at $V_{12-4} = 0.7V$; $V_{18-4} = 8.5V$

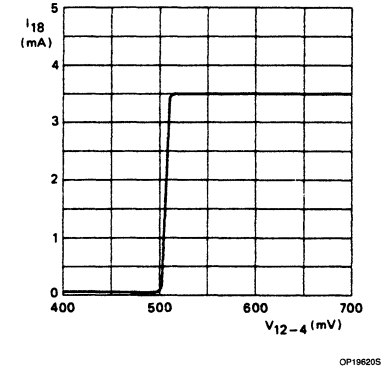
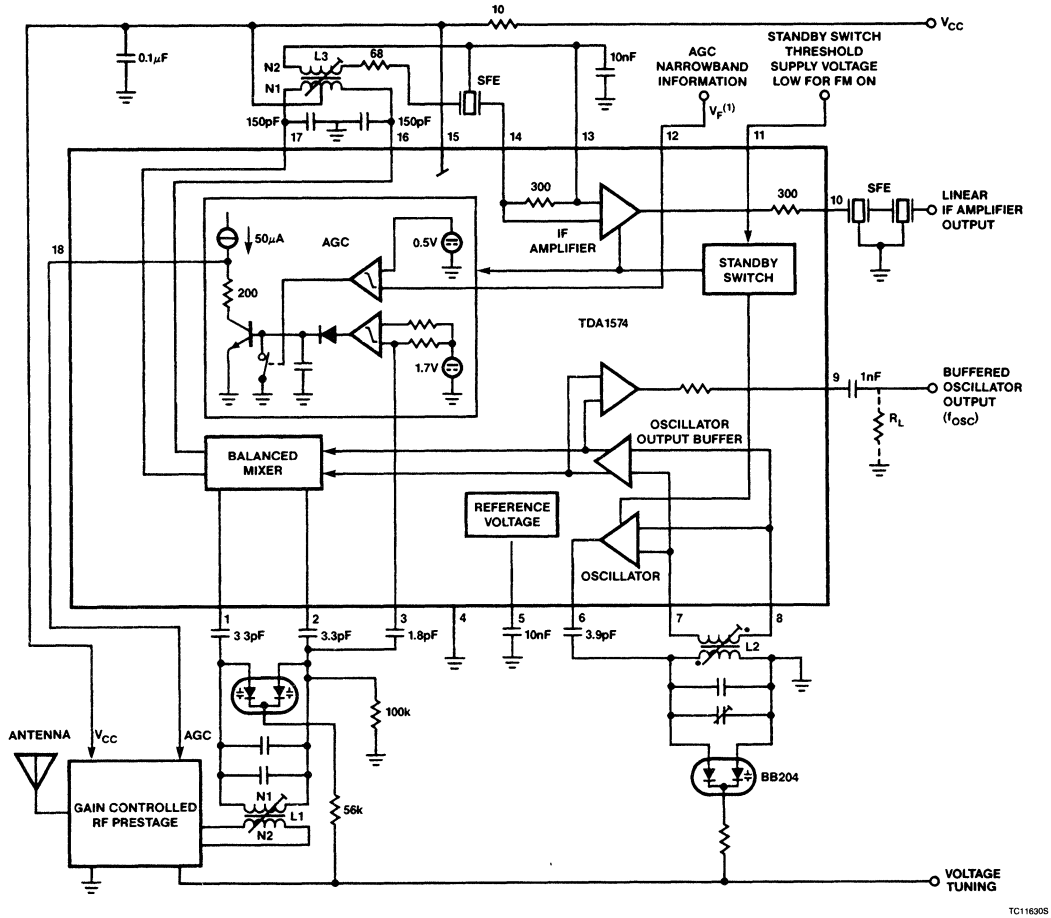


Figure 4. Keyed AGC Output Current I_{18} as a Function of Input Voltage V_{12-4}. Measured in Test Circuit (Block Diagram) at $V_{3-4} = 2V$; $V_{18-4} = 8.5V$



NOTES:
1 Field strength indication of main IF amplifier

Coil Data:
L1 TOKO MC-108, N1 = 5 5 turns, N2 = 1 turn
L2 } see Block Diagram
L3 }

Figure 5. TDA1574 Application Diagram

Signetics

TDA5030A
VHF Mixer/Oscillator Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA5030A performs the VHF mixer, VHF oscillator, SAW filter IF amplifier, and UHF IF amplifier functions in television tuners.

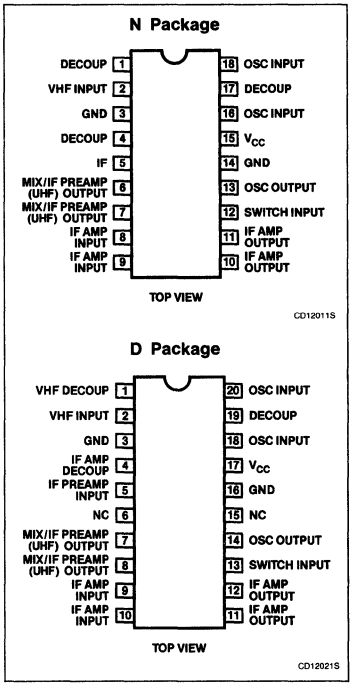
FEATURES

- **A balanced VHF mixer**
- **An amplitude-controlled VHF local oscillator**
- **A surface acoustic wave filter IF amplifier**
- **A UHF IF preamplifier**
- **A buffer stage for driving an external prescaler with the local oscillator signal**
- **A voltage stabilizer**
- **A UHF/VHF switching circuit**

APPLICATIONS

- **Mixer/oscillator**
- **TV tuners**
- **CATV**
- **LAN**
- **Demodulator**

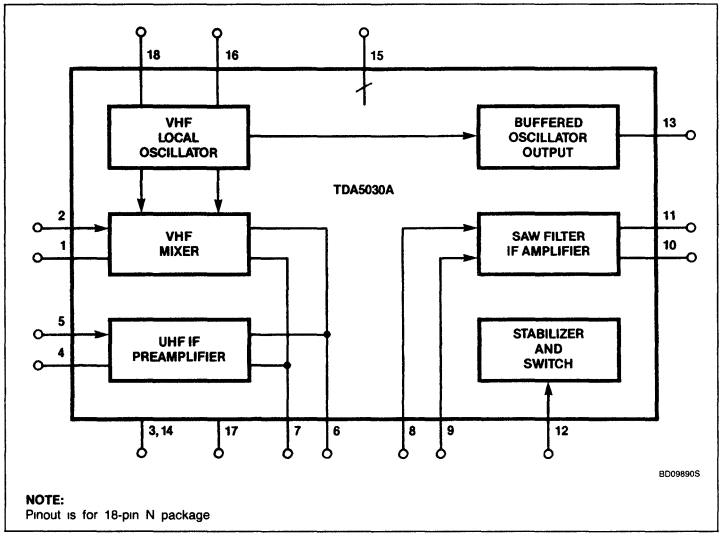
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102A)	−25°C to +85°C	TDA5030AN
20-Pin Plastic SO DIP (SOT-163A)	−25°C to +85°C	TDA5030ATD

BLOCK DIAGRAM



NOTE:
Pinout is for 18-pin N package

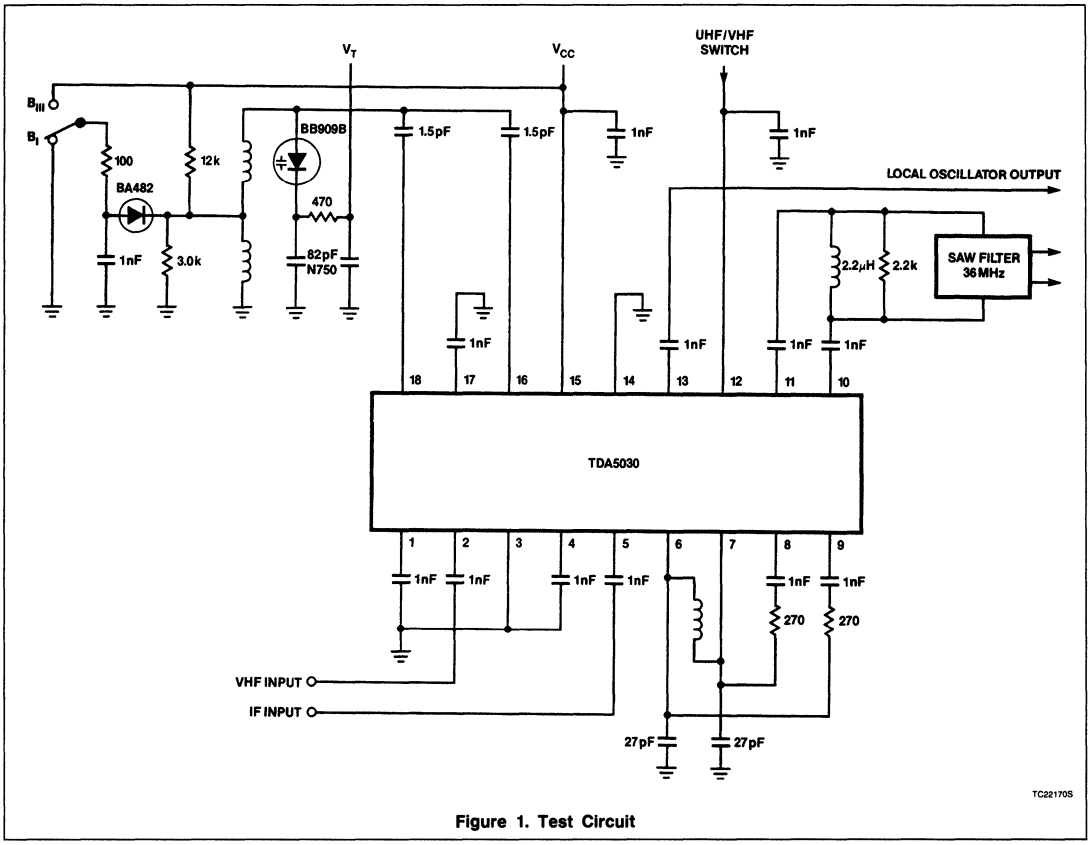


Figure 1. Test Circuit

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 15)	14	V
V_I	Input voltage (Pin 1, 2, 4, and 5)	0 to 5	V
V_{12}	Switching voltage (Pin 12)	0 to V_{CC}+0.3	V
$-I_{10, 11, 13}$	Output currents	10	mA
t_{SS}	Storage-circuit time on outputs (Pin 10 and 11)	10	s
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +85	°C
T_J	Junction temperature	+125	°C
θ_{JA}	Thermal resistance from junction to ambient	+55	°C/W

DC AND AC ELECTRICAL CHARACTERISTICS Measured in circuit of Figure 1; V_{CC} = 12V; T_A = 25°C, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{CC}	Supply voltage	10		13.2	V
I_{CC}	Supply current		42	55	mA
V_{12}	Switching voltage VHF	0		2.5	V
V_{12}	Switching voltage UHF	9.5		V_{CC}+0.3	V
I_{12}	Switching current UHF			0.7	mA
VHF mixer (including IF amplifier)					
f_R	Frequency range	50		470	MHz
NF	Noise figure (Pin 2) 50MHz 225MHz 300MHz		 7 5 9 10	 9 10 12	 dB dB dB
G	Optimum source admittance (Pin 2) 50MHz 225MHz 300MHz		 0.5 1.1 1.2		 ms ms ms
G_I	Input conductance (Pin 2) 50MHz 225MHz 300MHz		 0.23 0.5 0.67		 ms ms ms
C_I	Input capacitance (Pin 2) 50MHz		 2.5		 pF
V_{2-3}	Input voltage for 1% cross-modulation (in channel); $R_P > 1k\Omega$; tuned circuit with C_P = 22pF; f_{RES} = 36MHz	97	99		dBμV
V_{2-14}	Input voltage for 10kHz pulling (in channel) at < 300MHz	100			dBμV
A_V	Voltage gain	22.5	24.5	26.5	dB
UHF preamplifier (including IF amplifier)					
G_I	Input conductance (Pin 5)		0.3		ms
C_I	Input capacitance (Pin 5)		3 0		pF
NF	Noise figure		5	6	dB
V_{5-14}	Input voltage for 1% cross-modulation (in channel)	88	90		dBμV
A_V	Voltage gain	31.5	33.5	35.5	dB
G_5	Optimum source admittance		3.3		ms

4

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Measured in circuit of Figure 1; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
VHF mixer					
$Yc_{2-6,\ 7}$	Conversion transadmittance		5.7		ms
Z_O	Output impedance		1.6		kΩ
VHF oscillator					
f_R	Frequency range	70		520	MHz
Δf	Frequency shift ΔV_{CC} = 10%; 70 to 330MHz			200	kHz
Δf	Frequency drift ΔT = 15k; 70 to 330MHz			250	kHz
Δf	Frequency drift from 5sec to 15min after switching on			200	kHz
SAW filter IF amplifier					
$Z_{8,\ 9}$	Input impedance $Z_{10,\ 11}$ = 2kΩ, f = 36MHz		340+j100		Ω
$Z_{8,\ 9-10,\ 11}$	Transimpedance		2.2		kΩ
$Z_{10,\ 11}$	Output impedance $Z_{8,\ 9}$ = 1.6kΩ; f = 36MHz		50+j40		Ω
VHF local oscillator buffer stage					
	Output voltage				
V_{13}	R_L = 75Ω; f < 100MHz	14	20		mV
V_{13}	R_L = 75Ω; f > 100MHz	10	20		mV
Z_{13}	Output impedance f = 100MHz		90		Ω
$\frac{RF}{(RF+LO)}$	RF signal on LO output; R_L = 50Ω; V_I = 1V; f ≤ 225MHz			10	dB

Signetics

CA3089
FM IF System

Product Specification

Linear Products

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram shows the CA3089 features, which include a three-stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8V to +18V.

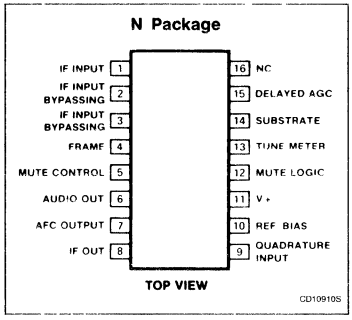
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at −3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

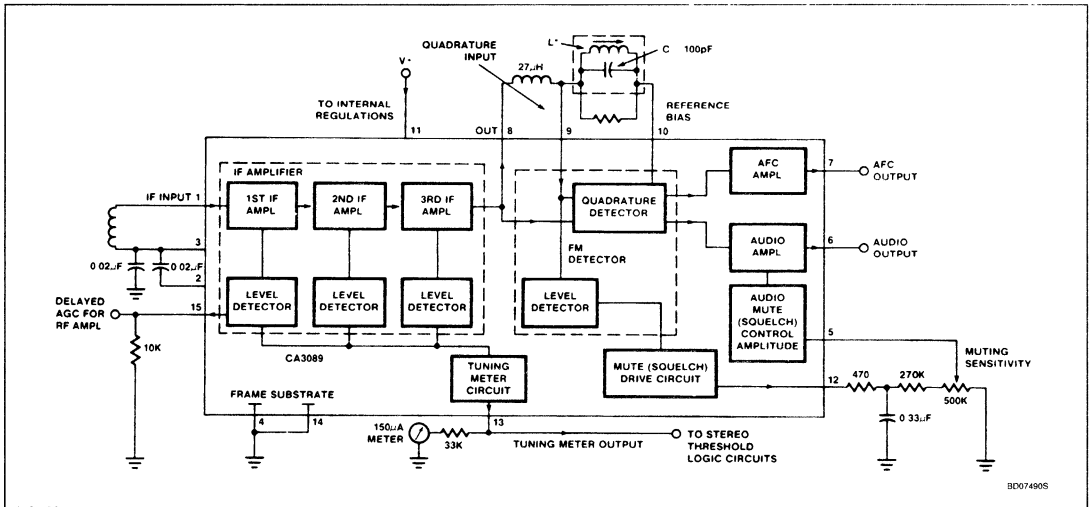
PIN CONFIGURATION



APPLICATIONS

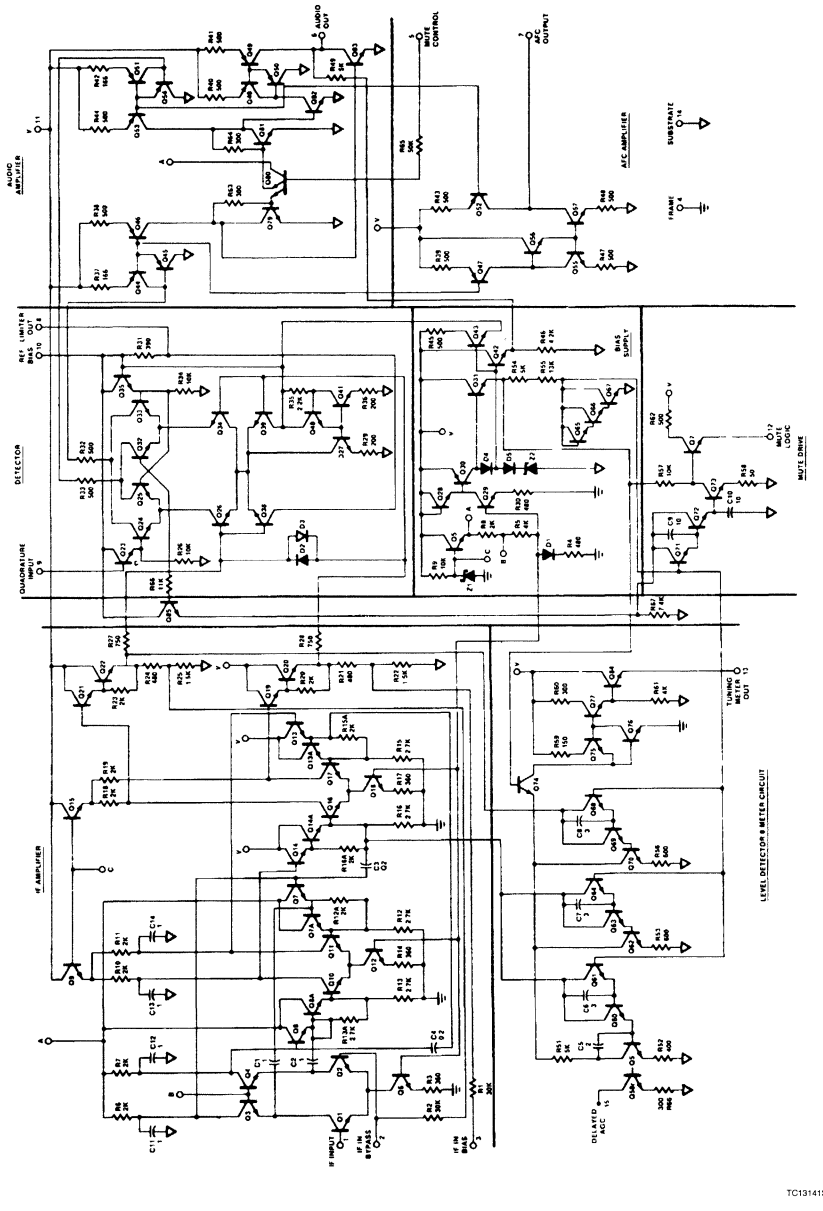
- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

BLOCK DIAGRAM



NOTES:
1 All resistor values are typical and in ohms $Q_O \simeq 75$ (G I EX27825 or equivalent)
2 L tunes with 100pF (C) at 10 7MHz

EQUIVALENT SCHEMATIC



NOTES:
1 All resistance values are typical and in ohms
2 All capacitance values are in picofarads

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	CA3089N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	DC supply voltage: between terminals 11 and 4 between terminals 11 and 14	 18 18	 V V
	DC current (out of Terminal 15)	2	mA
P_D	Device dissipation: up to $T_A = 60°C$ above $T_A = 60°C$	 600 derate linearly 6.7	 mW mW/°C
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

4

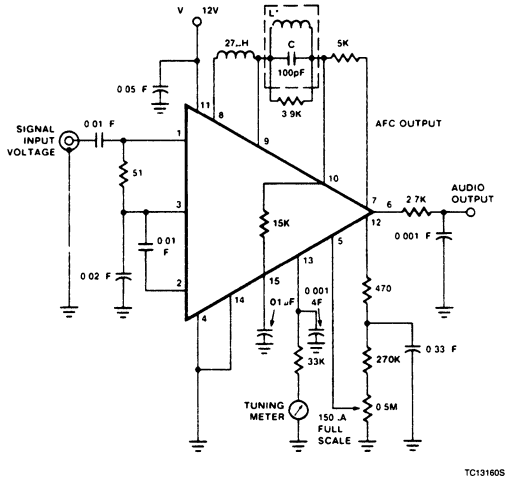
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Static (DC) Characteristics						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages[4]						
V_1	Terminal 1 (1F input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (AC return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (DC bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7	Terminal 7 (AFC)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (DC reference)	No signal input, non-muted	5.0	5.6	6.0	V
Dynamic Characteristics						
$V_{I(LIM)}$	Input limiting voltage (-3dB point)[3]			10	25	μV
	AMR AM rejection (Terminal 6)[4]	$V_{IN} = 0.1V$, $f_O = 10.7MHz$, $f_{MOD} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (Terminal 6)[3]		400	500	600	mV
	Total harmonic distortion:[1]					
THD	Single tuned (Terminal 6)[3]			0.5	1.0	%
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$, $V_{IN} = 0.1$		0.1		%
S + N/N	Signal plus noise-to-noise ratio (Terminal 6)[3]	Deviation = ± 75kHz, $V_{IN} = 0.1V$	60	70		dB
MU_{IN}	Mute input (Terminal 5)	$V_5 = 2.5V$	50	70		dB
MU_{OUT}	Mute output (Terminal 12)	$V_{IN} = 50\mu V$			0.5	V
		$V_{IN} = 0V$	4.0			V
MTR	Meter output (Terminal 13)	$V_{IN} = 0.1V$	2.5	3.5		V
		$V_{IN} = 500\mu V$	1.0	1.5		V
		$V_{IN} = 0V$			0.7	V
AGC	Delay AGC (Terminal 15)	$V_{IN} = 0.01V$			0.5	V
		$V_{IN} = 10\mu V$	4.0	5.0		V
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$, $V_{IN} = 0.1$		0.1		%

NOTES

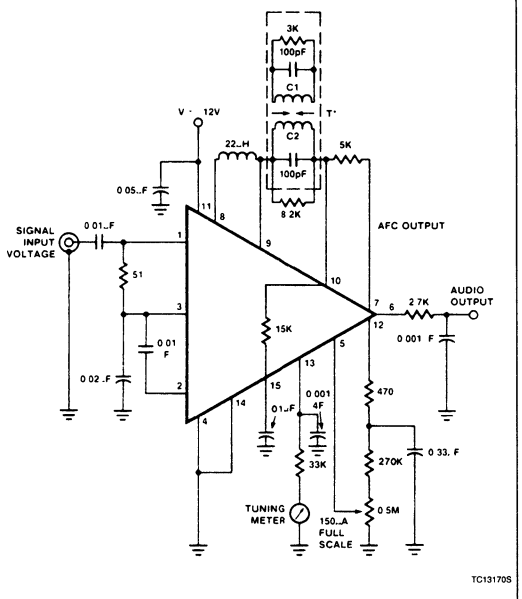
1. THD characteristics and audio level are essentially a function of the phase and Q characteristics of the network connected between Terminals 8, 9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS



NOTES:
1 L tunes with 100pF (C) at 10 7MHz.
2 All resistor values are typical and in ohms
3. Q_O (unloaded) $\simeq$ 75 (G I automatic mfg div EX27825 or equivalent)

Figure 1. Test Circuit Using a Single-Tuned Detector Coil



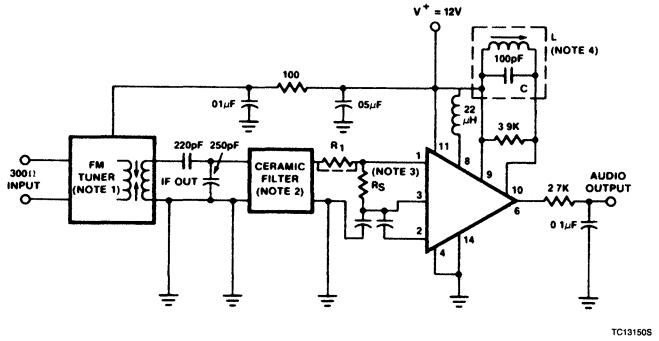
NOTES:
All resistor values are typical and in ohms

T. Pri — Q_O (unloaded) $\simeq$ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32' dia form) Sec – Q (unloaded) $\simeq$ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32' dia form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C = 150mV)
Above values permit proper operation of mute (squelch) circuit 'E' type slugs, spacing 4mm

Figure 2. Test Circuit Using a Double-Tuned Detector Coil

4

TEST CIRCUITS



NOTES:
All resistor values are typical and in ohms.
1 Waller 4SN3FIC or equivalent
2 Murate SFG 10.7mA or equivalent
3. R_S will affect stability depending on circuit layout To increase stability R_S is decreased Range of R_S is 330 to 50Ω, $R_1 + R_S \leqslant 330\Omega$
4 L tunes with 100pF (C) at 10 7MHz Q_O unloaded ≃ 75 (G I EX27825 or equivalent)

Performance data at f_O = 98MHz, f_{MOD} = 400Hz, deviation = ± 74kHz ± 74kHz

– 3dB limiting sensitivity	2μV (antenna level)
20dB quieting sensitivity	1μV (antenna level)
30dB quieting sensitivity	1 5μV (antenna level)

Figure 3. Typical FM Tuner With a Single-Tuned Detector Coil

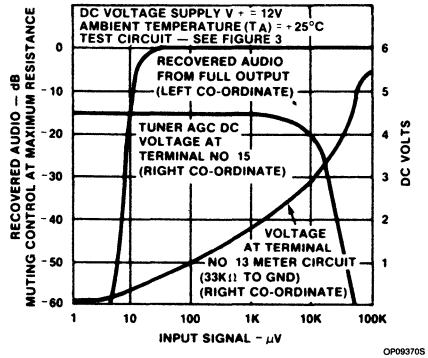
SYSTEM DESIGN CONSIDERATIONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input bypass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good bypass capacitors would be ceramic disc with values in the range of 0.01 to 0.05μF.

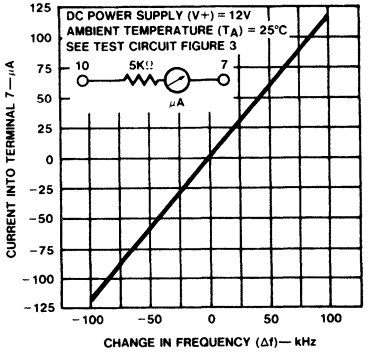
The input impedance of the CA3089 is approximately 10,000Ω. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50Ω and 100Ω is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

Muting Action, Tuner AGC
(Tuning meter output as a function of input signal voltage.)



AFC Characteristics
(Current at Terminal 7 as a function of change in frequency.)



Signetics

MC3361
Low Power FM IF

Product Specification

Linear Products

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SOL (surface-mounted miniature package).

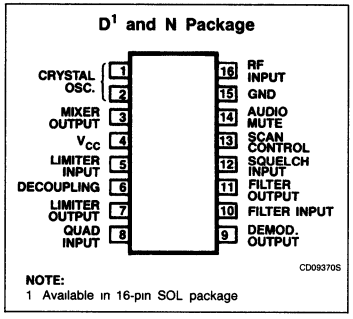
FEATURES

- **2.0V to 8.0V operation**
- **Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}**
- **Excellent sensitivity: 2.0μV for −3dB limiting typ**
- **Low external parts count**
- **Operation to 60MHz**

APPLICATIONS

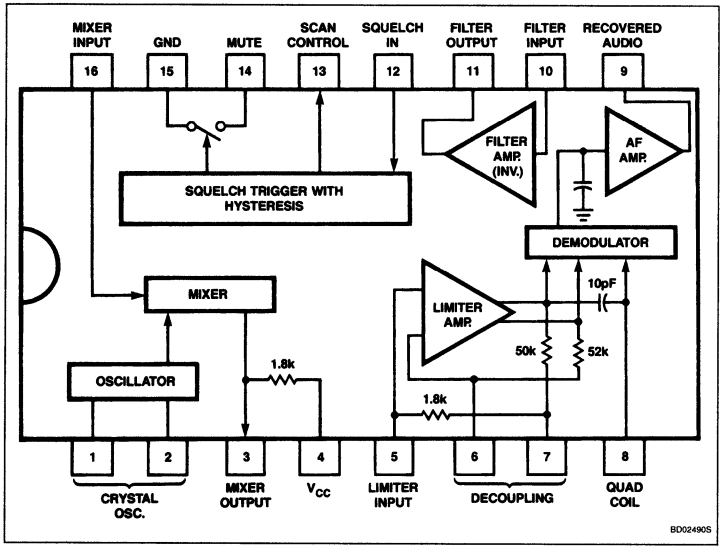
- **Cordless telephone**
- **Narrow band receivers**
- **Remote control**

PIN CONFIGURATION



NOTE:
1 Available in 16-pin SOL package

BLOCK DIAGRAM



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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40 to +85°C	MC3361N
16-Pin Plastic; SOL	−40 to +85°C	MC3361D

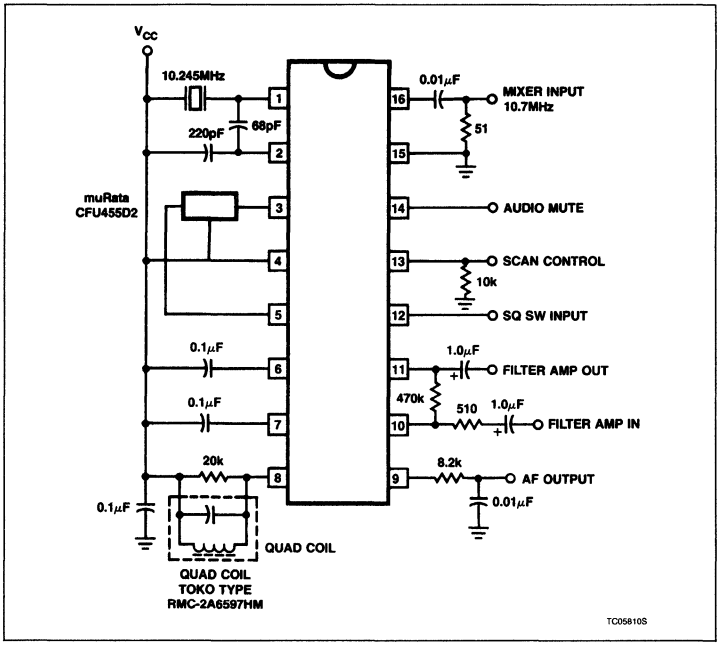
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	−0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature range		−40 to +85	°C
T_{STG}	Storage temperature range		−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = ±3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.)

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off squelch on	4			4.2 5.4	7.0 9.0	mA
Input limiting voltage	16	−3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	V_{IN} = 10mV_{RMS}	100	150	270	mV_{RMS}
Filter gain (10kHz)		V_{IN} = 1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13	V_{12} = 1.0V_{DC}			0.5	V_{DC}
Scan function high (mute on)	13	V_{12} = GND	3.5			V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



Signetics

AN1992
Using the Signetics MC3361 Demonstration Board

Application Note

Linear Products

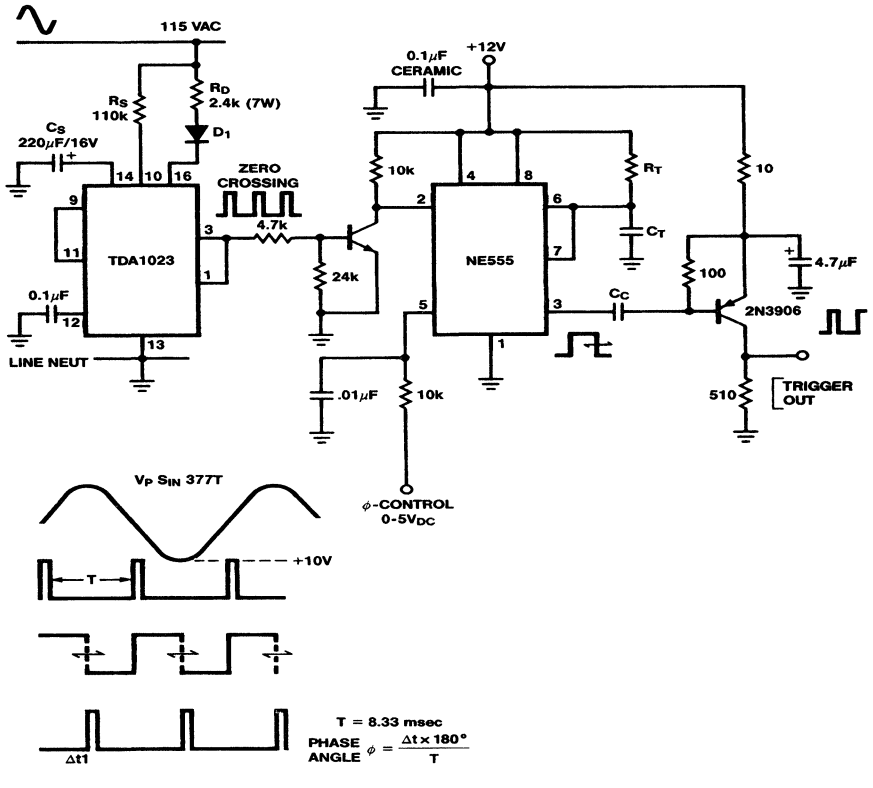
Author: Michael M. Sera

INTRODUCTION

Circuit Description

This demo is set up to show the functions of the Signetics MC3361. The MC3361 is a Low Power Narrow-Band FM IF. It is designed for use as the second IF of FM dual conversion communications equipment. The MC3361 includes the following:

- Oscillator
- Mixer
- Limiting amplifier
- Quadrature discriminator
- Active filter
- Squelch
- Scan control
- Mute switch



NOTE:
This is the schematic of the Signetics MC3361 demonstration board The input and output connections are AC-coupled to protect the device from any DC that may be introduced at the inputs The supply is capacitively decoupled to ground to help eliminate any AC on the supply line

Figure 1. Schematic of the Signetics MC3361 Demonstration Board

Using the Signetics MC3361 Demonstration Board

AN1992

The application outlined here does not demonstrate the absolute maximum performance of the Signetics MC3361. It is merely an example given to show the flexibility of the part.

In general, the external components used for each application tend to be the limiting factors in each application. In order to make the demo board suitable for general usage, the Local Oscillator (LO) is supplied externally.

This allows the input frequency to operate anywhere within the limitations of the part. The inputs have not been matched for any one particular frequency.

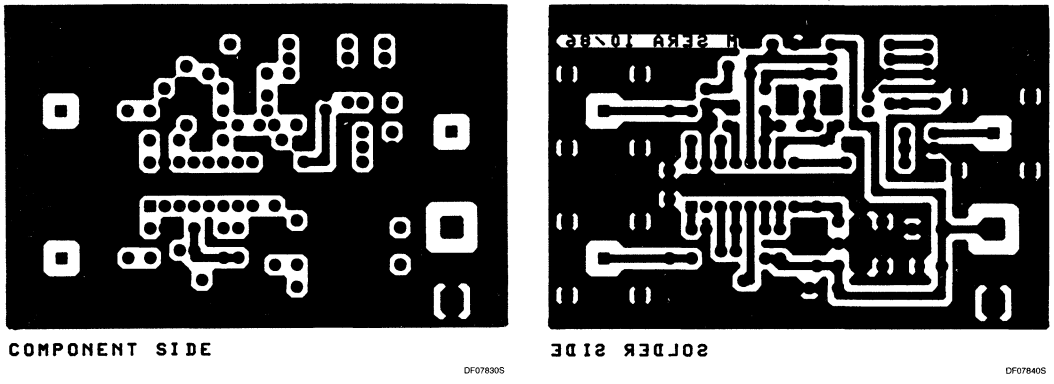


Figure 2. Layout of the Signetics MC3361 Demonstration Board

PARTS LIST

Capacitors

C1	0.1μF
C2	0.1μF
C3	0.1μF
C4	10μF Elect
C5	0 1μF
C6	0 1μF
C7	0.1μF
C8	0.1μF
C9	0 47μF
C10	0.01μF
C11	0 001μF
C12	0.001μF
C13	0.01μF
C14	0 1μF
C15	0 1μF

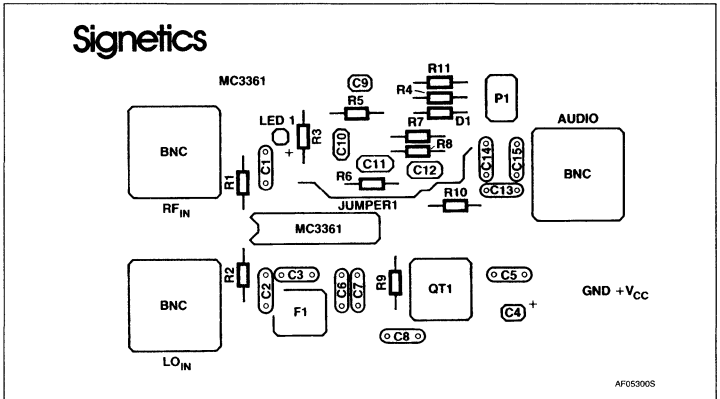


Figure 3. Part Layout for Demonstration Board

Resistors[1]

R1	51	¼ W
R2	51	¼ W
R3	330	¼ W
R4	68k	¼ W
R5	120k	¼ W
R6	390k	¼ W
R7	750	¼ W
R8	18k	¼ W
R9	20k	¼ W
R10	7.5k	¼ W
R11	51k	¼ W

NOTE:
1. All resistors are 5%

Miscellaneous

MC3361	SIGNETICS MC3361
LED1	Red LED
D1	Diode (1N4148)
P1	50k Potentiometer (BOURNS 3299 144C 50K)
Q1	Quad Tank (TOKO RMC 2A6597HK[1])
F1	455kHz Filter (MURUTA CFU455D2[2])
BNC	BNC Connector (KINGS KC-79-232-MO6)

NOTES:
1 TOKO AMERICA INC
West Touhy Ave
Skokie, IL 60077
Tel· (213) 677-3640
CA (408) 996-7575

2 MURUTA ERIE
1453 Lincoln Street
Carlisle, PA 17013
Tel (717) 249-2232

Using the Signetics MC3361 Demonstration Board AN1992

Matching the input will increase the sensitivity of the part. See Appendix II for matching network.

LAYOUT

The board layout uses basic RF techniques, i.e , GND on both top and bottom layers, very short input and output lead lengths and wide traces, with decoupling capacitors on the supply lines.

Operation of the MC3361 Demonstration Board

In this application the MC3361 is set up as an FM receiver. The input is mixed with the LO to convert the input signal down to 455kHz. The signal then goes through an external (455kHz) ceramic bandpass filter. Next, the 455kHz signal goes through a limiting amplifier. The audio is finally recovered using an FM demodulator and then amplified by an audio amp.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This 'noise band' is monitored by an active filter and a detector. A squelch control circuit mutes the audio output signal when the 'noise band' is above a certain level set by P1 The squelch control circuit also provides a scan control output (Pin 13) which can be used to drive an LED, as we have done on the application board.

DEMONSTRATION BOARD CONNECTIONS AND ADJUSTMENTS

RF_{IN} (RF Input) — An RF signal source with FM content should be connected here. The Maximum frequency is shown on the graph (Figure 2). Set the signal generator to FM and adjust the peak deviation to 3kHz. Set the modulation frequency to 1kHz. The RF amplitude can be varied from as low as 2μV to as high as 1V.

LO_{IN} (Local Oscillator Input) — Should be 455kHz above or below the RF input at approximately 0dBm with *no* deviation. This input is normally configured with a Colpitts crystal oscillator (see Appendix I), but for ease of flexibility we chose to feed the LO externally.

AUDIO (Audio Output) — The audio recovered from the RF signal can be seen at this point. Use an oscilloscope adjusted to trigger at the audio frequency (1kHz). Remember that the RF input must have some FM content in order to see a signal here

Power Supply — The Signetics MC3361 will operate with a supply voltage as low as 2.0V and up to 8 0V. The demo board will function with a supply voltage as low as 3.5V. The demo board consumes 4.7mA (Mute off) and 8.2mA (Mute on, LED current included) at 5.0V. A regulated supply with at least $+3.5V_{DC}$ should be connected to the $+V_{CC}$ terminal of the board. The same supply's ground should be connected to the GND terminal.

QT1 (Quad Tank) — This is the 'silver can' located near the supply inputs. It has been adjusted at the factory. If it needs to be adjusted, see Testing.

P1 (Potentiometer) — This adjusts the sensitivity of the mute function. This will cause the AUDIO to be muted at varying levels of RF input amplitudes.

The Red LED (Mute ON Indicator) — When lit, the audio signal is muted. P1 (potentiometer located near Audio Out connection) adjusts the mute sensitivity. The sensitivity can be checked by varying the RF input amplitude.

TESTING AND ADJUSTING THE DEMONSTRATION BOARD

Equipment Required

Power Supply: HP 6216A or equivalent

Signal Generator: HP 8640B or equivalent

Signal Generator: HP 8640B or equivalent

Oscilloscope: Philips PM3243 or equivalent

To test the MC3361 demonstration board, you should carefully follow the instructions listed below.

1. Connect a +5V regulated power supply to $+V_{CC}$.
2. Connect the supply ground to GND.
3. Connect #1 Signal Generator to RF_{IN}; note the frequency on the display. Set the signal generator to FM with a peak deviation of 3kHz and a modulation frequency of 1kHz. The amplitude should be adjusted to around −20dBm ($22mV_{RMS}$).
4. Connect #2 Signal Generator to LO_{IN}, noting the frequency of the #1 Signal Generator connected to RF_{IN}; add or subtract 455kHz from that number and adjust the #2 Signal Generator to this frequency. The amplitude should be set at 0dBm ($220mV_{RMS}$). Make sure *no* modulation is applied at this input.
5. Connect an oscilloscope to AUDIO. The oscilloscope should trigger off of a signal near 1kHz. The Red LED should not be lit. If the Red LED is lit, adjust P1 until the Red LED turns off.
6. Once all the connections have been made, you should see a clean sine wave on the oscilloscope.
7. Peak the amplitude of the sine wave seen at the AUDIO output by adjusting QT1. This will tune the Quadrature Detector.
8. To test the sensitivity of the circuit, vary the input amplitude of the RF_{IN} signal. The sine wave will start to get noisy around −100dBm. As you decrease the amplitude even more, the 'noise band' will increase, causing the Squelch Control circuit to trigger. When the Squelch Control circuit does trigger, the audio output will go to 0V and the Red LED will be on.
9. The Squelch Control circuit's sensitivity can be controlled by P1. Adjust P1 to trigger at the desired RF input level.
10. The RF_{IN} frequency can also be varied, just as long as the LO_{IN} is 455kHz above or below the RF_{IN} frequency. Figure 4 shows the sensitivity vs. frequency of the demonstration board.

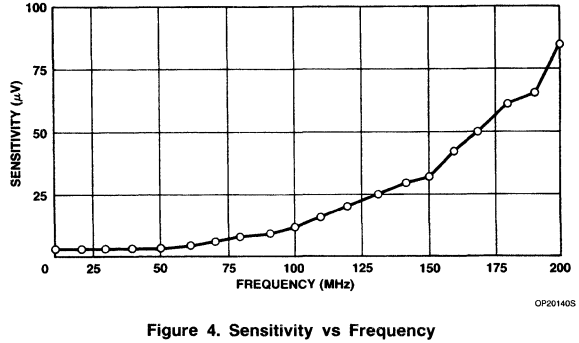


Figure 4. Sensitivity vs Frequency

Using the Signetics MC3361 Demonstration Board AN1992

SENSITIVITY VS FREQUENCY

Figure 4 shows the sensitivity of the demonstration board over frequency (V_{CC} = 5.0V). The inputs are 50Ω terminated to suit most inputs. Note that the inputs are not matched for any one frequency; matching the input to one desired frequency will increase the sensitivity.

APPENDIX I

The LO can be supplied using a Colpitts crystal oscillator tuned to the desired frequency. Figure 5 shows a Colpitts crystal oscillator tuned to 10.245MHz, which would accommodate an input of 10.7MHz.

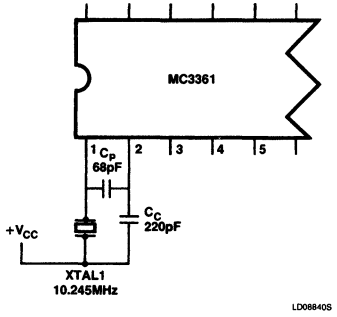


Figure 5. Schematic of a Colpitts Crystal Oscillator

4

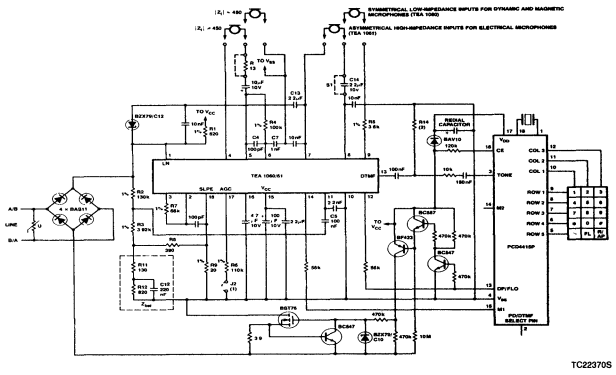
Using the Signetics MC3361 Demonstration Board AN1992

APPENDIX II

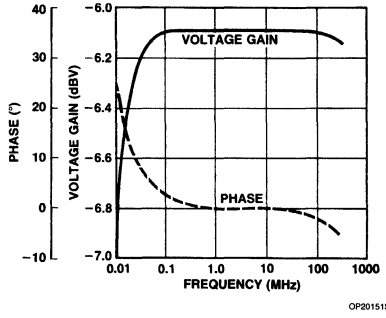
The input has a 50Ω termination resistor for matching the input to most (50Ω) signal sources. This way the device is not limited to any one particular frequency. Figure 6 shows the frequency response of the input as it is on the demonstration board.

Figure 7 uses a matching network tuned to 10MHz. The network is called a capacitor divider. It basically transforms the input impedance to match the device input impedance of 3.3kΩ and 2.2pF at 10MHz. The matched input has an increase gain of 16dBV over the 50Ω termination network.

REF: *Ferromagnetic Core Design Application & Handbook*, Doug DeMaw.

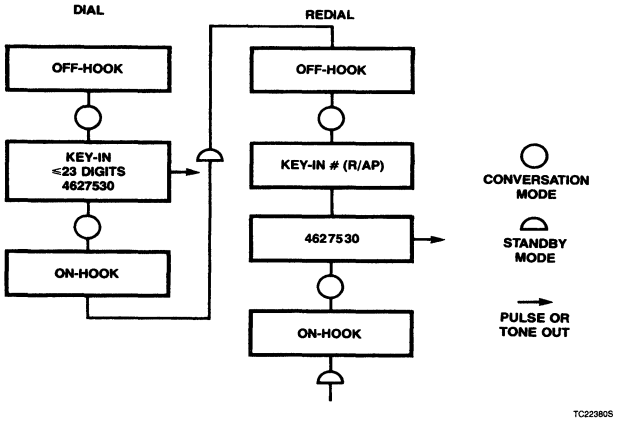


a. Broadband Termination

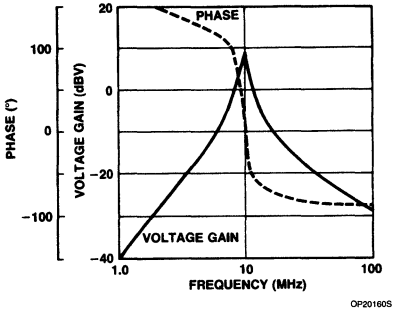


b. Voltage Transfer Ratio With Broadband Termination

Figure 6. Voltage Transfer Ratio of the Demonstration Board



a. Typical Input Matching Network



b. Typical Network Voltage Transfer Ratio Input Matching (at 10.7MHz)

Figure 7

4

Signetics

NE/SA604A
High-Performance Low-Power FM IF System

Preliminary Specification

Linear Products

DESCRIPTION

The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature package).

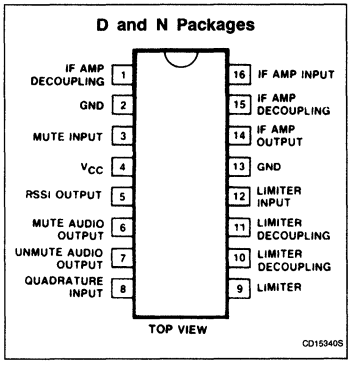
FEATURES

- **Low-power consumption 3.3mA typical**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs – muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA604A meets cellular radio specifications**

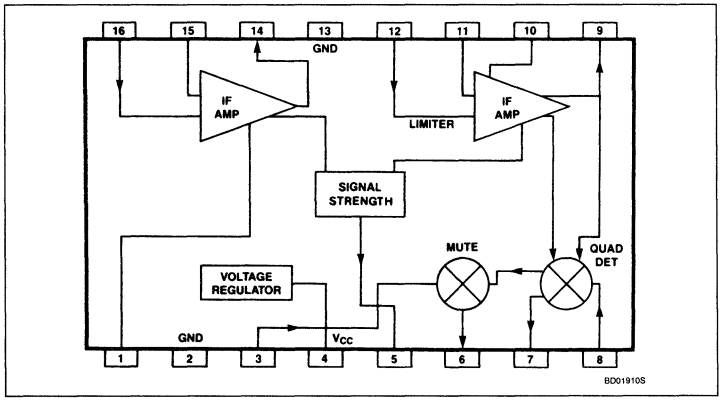
APPLICATIONS

- **Cellular Radio FM IF**
- **High performance communications receivers**
- **Intermediate freqency amplification and detection up to 21MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE604AN
16-Pin Plastic SO (Surface-mounted miniature package)	0 to +70°C	NE604AD
16-Pin Plastic DIP	−40 to +85°C	SA604AN
16-Pin Plastic SO (Surface-mounted miniature package)	−40 to +85°C	SA604AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating temperature NE604A SA604A	 0 to 70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS	NE604A			SA604A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Power supply voltage range		4.5		8.0	4.5		8.0	V
	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. IF frequency = 455kHz; IF level = −47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

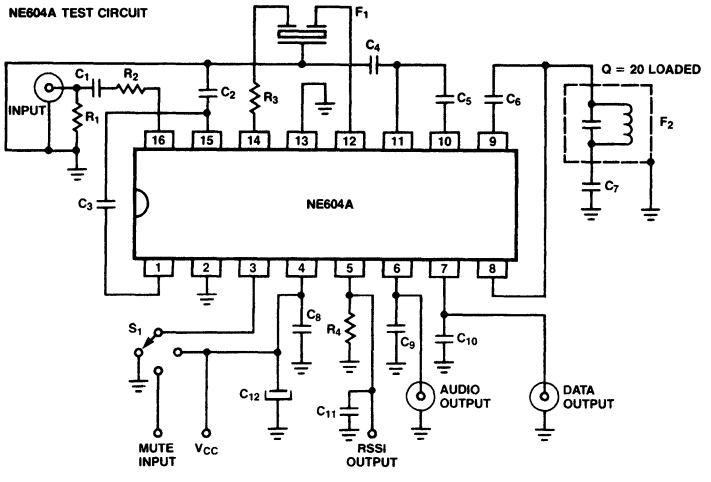
SYMBOL	PARAMETER	TEST CONDITIONS	NE604A			SA604A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input limiting-3dB	Test at Pin 16		−92			−92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{rms}
	Recovered audio level	150pF de-emphasis		530			530		mV_{rms}
	SINAD sensitivity	RF level −97dBm		16			16		dB
	THD		−35	−42		−34	−42		dB
	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = −118dBm	0	160	550	0	160	650	mV
		RF level = −68dBm	2.0	2.65	3.0	1.09	2.65	3.1	V
		RF level = −18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k Pin 5		90			90		dB
	RSSI accuracy	R_4 = 100k Pin 5		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		Ω

NOTE:

1 NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

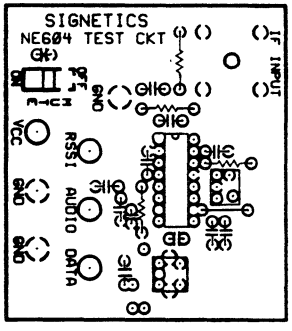
NE604(50)	NE604A (1 5k)/NE605 (1.5k)
−97dBm	−118dBm
−47dBm	−68dBm
+3 dBm	−18dBm

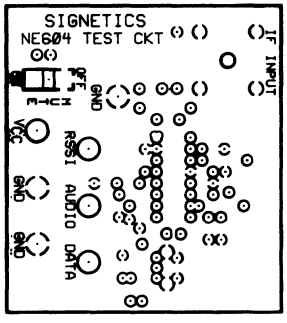
2 The NE605 and NE604A are both derived from the same basic die. The NE605 performance plot NE604A.



NOTES:

C1 10nF +80–20% 63V K10000-Z5V Ceramic
C2 100nF ±10% 50V
C3 100nF ±10% 50V
C4 100nF ±10% 50V
C5 100nF ±10% 50V
C6 10pF ±2% 100V NPO Ceramic
C7 100nF ±10% 50V
C8 100nF ±10% 50V
C9 15nF ±10% 50V
C10 150pF ±2% 100V N1500 Ceramic
C11 1nF ±10% 100V K2000-Y5P Ceramic
C12 6.8uF ±20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ±1% ¼W Metal Film
R2 1500Ω ±1% ¼W Metal Film
R3 1500Ω ±5% ⅛W Carbon Composition
R4 100kΩ ±1% ¼W Metal Film





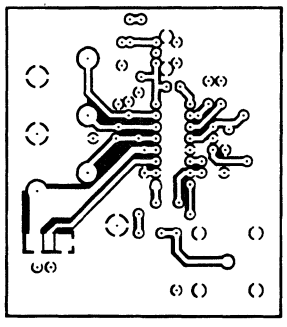


Figure 1. NE604A Test Circuit

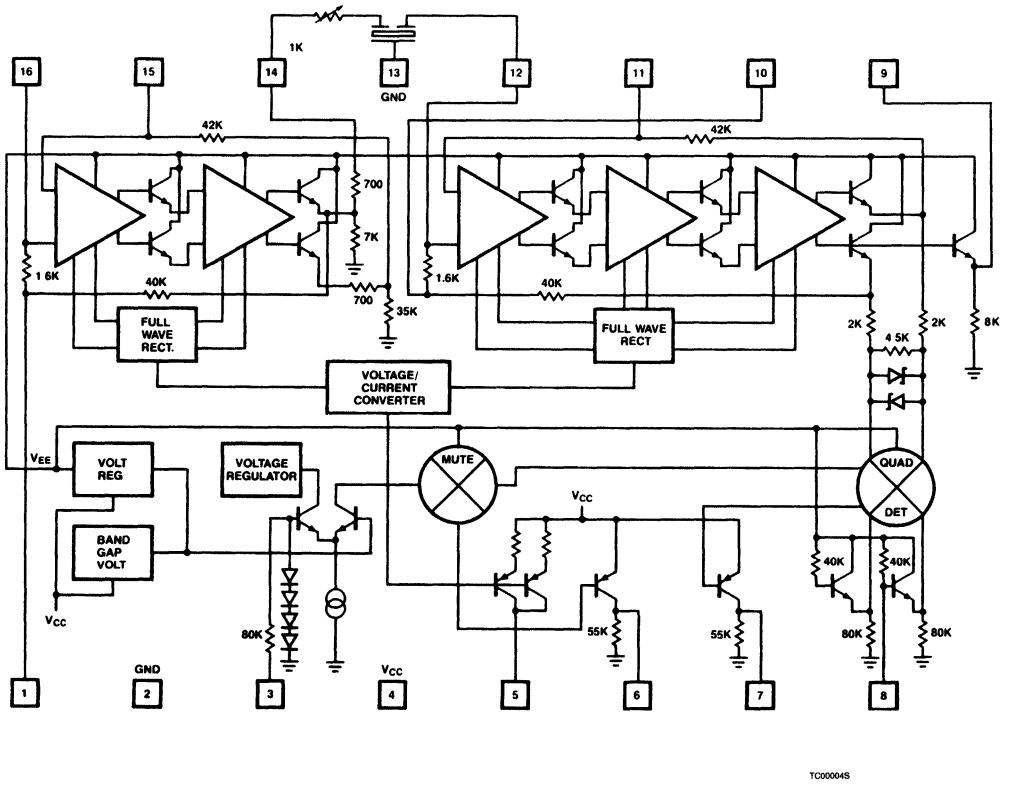


Figure 2. Equivalent Circuit

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A can not be evaluated independent of circuit, components, and board layout. A physicial layout which correlates to the electrical limits is shown in Figure 1. The configuration can be used as the basis for production layout.

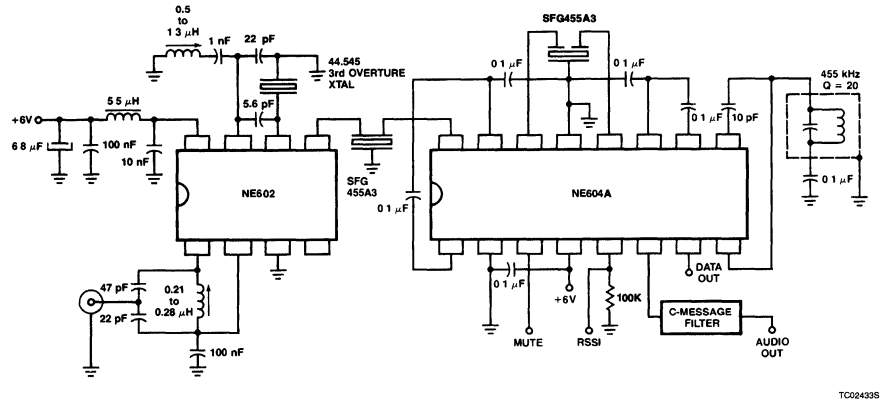
The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF AMPLIFIERS

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2 the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bankwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including the RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin



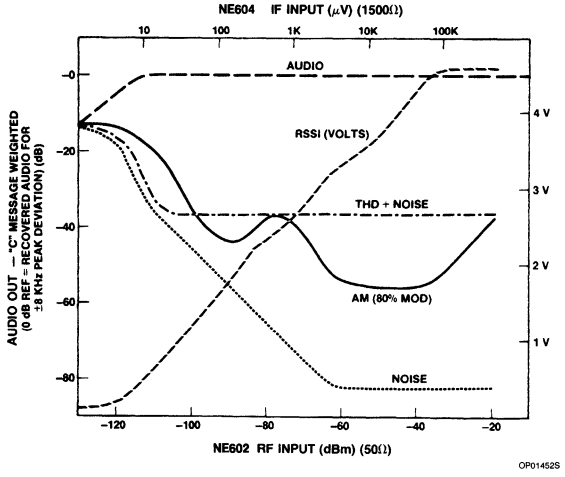


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

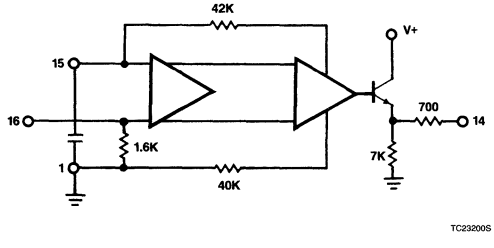


Figure 4. First Limiter Bias

to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned Examples of impedance/gain adjustment are shown in Figure 7 Reduce gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

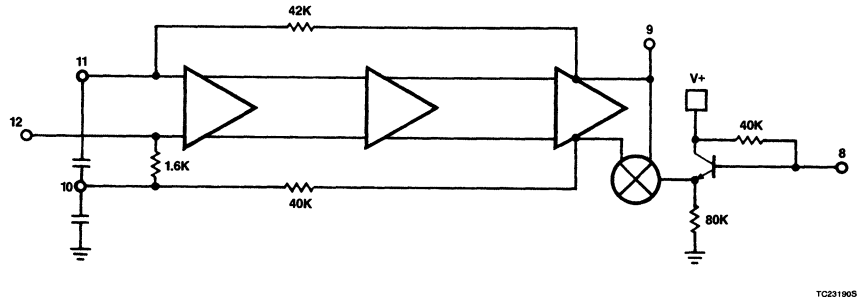


Figure 5. Second Limiter and Quadrature Detector

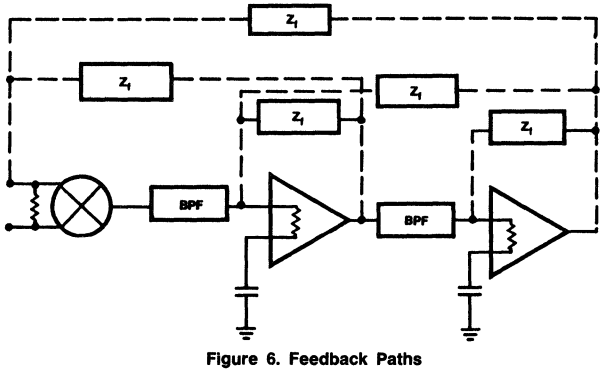


Figure 6. Feedback Paths

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and grounds, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptible with this layout. Every layout must be evaluated on its own merit, don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

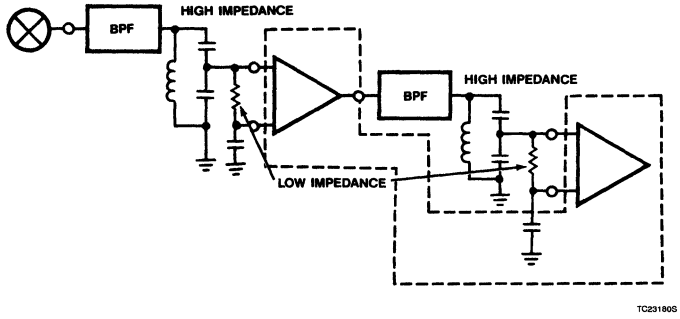
As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrow-band selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean nonexistent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

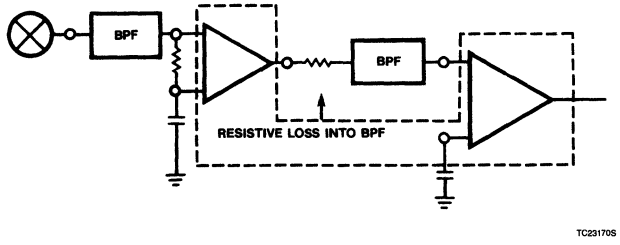
The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single ended to an external capacitor at Pin 9. There is a 90° phase shift across the phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multipler at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

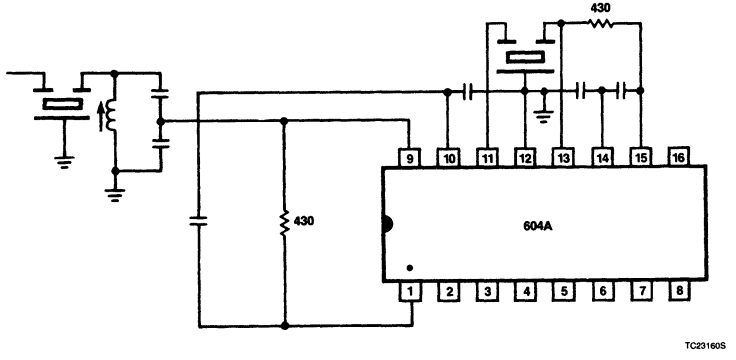


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

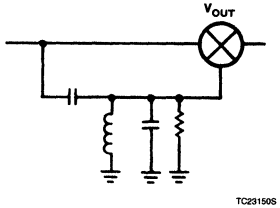


Figure 9.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the nonlinearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first order effects only.

Frequency Discriminator Design Equations for NE604A

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_N \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_3 will be:

$$\phi = \angle V_O - \angle V_N = \text{tg}^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10. Is the plot of ϕ vs $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of

$$\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}.$$

The signal V_o would have a phase shift of $\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \text{ Sin } \omega t$ (3)

$$\rightarrow V_O = A \text{ Sin}\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \text{ Sin } \omega t \quad (4)$$

$$\text{Sin}\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

after low pass filtering

$$\rightarrow V_{OUT} = \frac{1}{2}A^2 \quad (5)$$

$$\text{COS}\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] = \frac{1}{2}A^2 \text{ Sin}\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\left(\frac{\omega}{\omega_1}\right) = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is the discriminated FM output.

NOTE: $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p.311. Example: At 455kHz IF, with ±5kHz FM deviation. The max/min normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the ϕ vs. normalized frequency curves (Figure 10) and draw a vertical

straight line at $\left(\frac{\omega}{\omega_1}\right) = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discrimination FM signal. (Eq.6)

→Choose a Q = 20.

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10\text{pF}$ and $C_P = 164\text{pF}$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH, should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1\text{pF}$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. This response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resis-

tance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts The output of the comparator will be the logical output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10 MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers It is essentially independent of the IF frequency Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1Ω resistor from the output of the first limiter (Pin 14) to the input of the interstage filter With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an inband signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

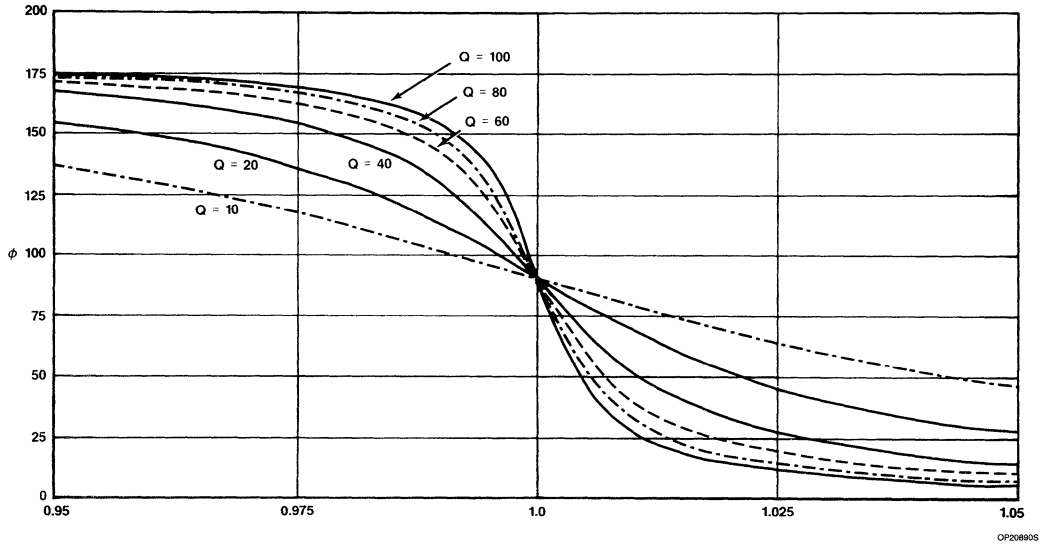


Figure 10. Phase vs. Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Signetics

AN1991
Audio Decibel Level Detector With Meter Driver

Application Note

Linear Products

Author: Robert J. Zavrel Jr.

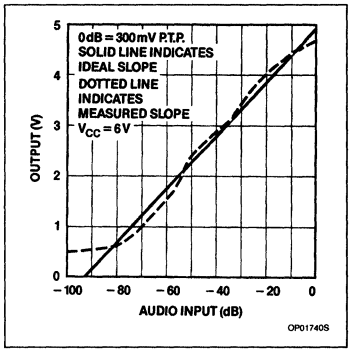
DESCRIPTION

Although the NE604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The NE604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

A sensitive audio level indicator circuit can be constructed using two integrated circuits: the NE604 and NE532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5μV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0 – 5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (< 0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.



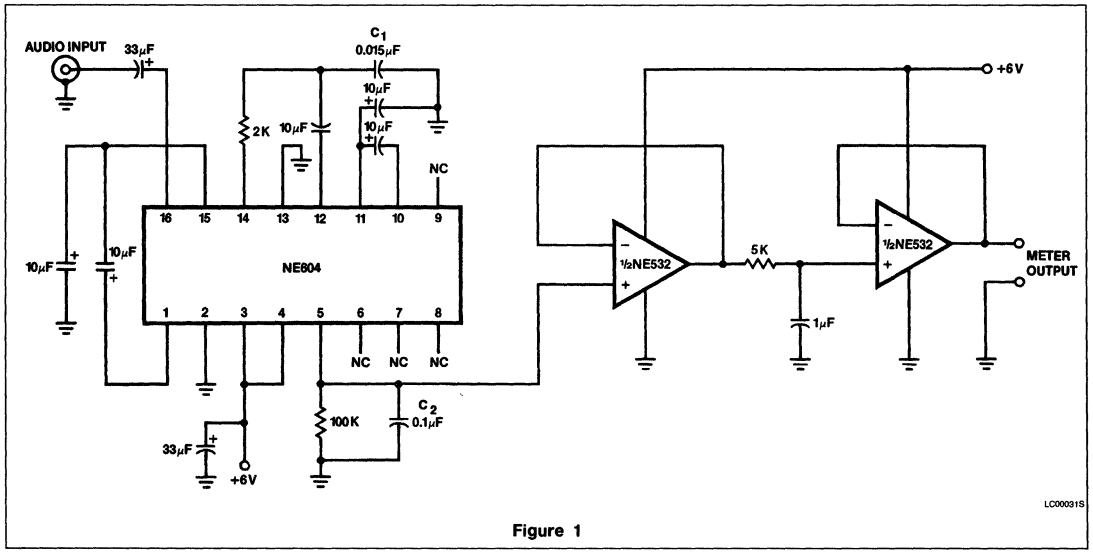


Figure 1

Audio Decibel Level Detector With Meter Driver AN1991

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1μF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1 Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

Signetics

Linear Products

AN1993

High Sensitivity Applications of Low-Power RF/IF Integrated Circuits

Application Note

ABSTRACT

This paper discusses four high sensitivity receivers and IF (Intermediate Frequency) strips which utilize intermediate frequencies of 10.7MHz or greater. Each circuit utilizes a low-power VHF mixer and high-performance low-power IF strip. The circuit configurations are

1. 45 or 49MHz to 10.7MHz narrowband,
2. 90MHz to 21.4MHz narrowband,
3. 100MHz to 10.7MHz wideband, and
4. 152.2MHz to 10.7MHz narrowband.

Each circuit is presented with an explanation of component selection criteria, (to permit adaptation to other frequencies and bandwidths). Optional configurations for local oscillators and data demodulators are summarized.

INTRODUCTION

Traditionally, the use of 10.7MHz as an intermediate frequency has been an attractive means to accomplish reasonable image rejection in VHF/UHF receivers. However, applying significant gain at a high IF has required extensive gain stage isolation to avoid instability and very high current consumption to get adequate amplifier gain bandwidth. By enlightened application of two relatively new low power ICs, Signetics NE602 and NE604A, it is possible to build highly producible IF strips and receivers with input frequencies to several hundred megahertz, IF frequencies of 10.7 or 21.4MHz, and sensitivity less than 2μV (in many cases less than 1μV). The Signetics new NE605 combines the function of the NE602 and the NE604A. All of the circuits described in this paper can also be implemented with the NE605. The NE602 and NE604A were utilized for this paper to permit optimum gain stage isolation and filter location.

THE BASICS

First let's look at why it is relevant to use a 10.7 or 21.4MHz intermediate frequency. 455kHz ceramic filters offer good selectivity and small size at a low price. Why use a higher IF? The fundamental premise for the answer to this question is that the receiver architecture is a hetrodyne type as shown in Figure 1.

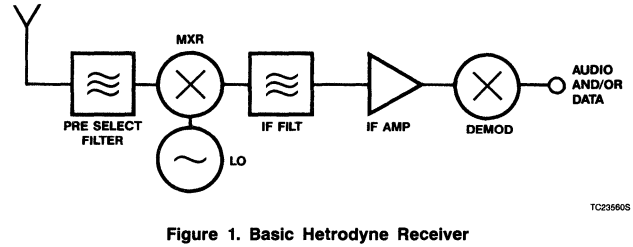


Figure 1. Basic Hetrodyne Receiver

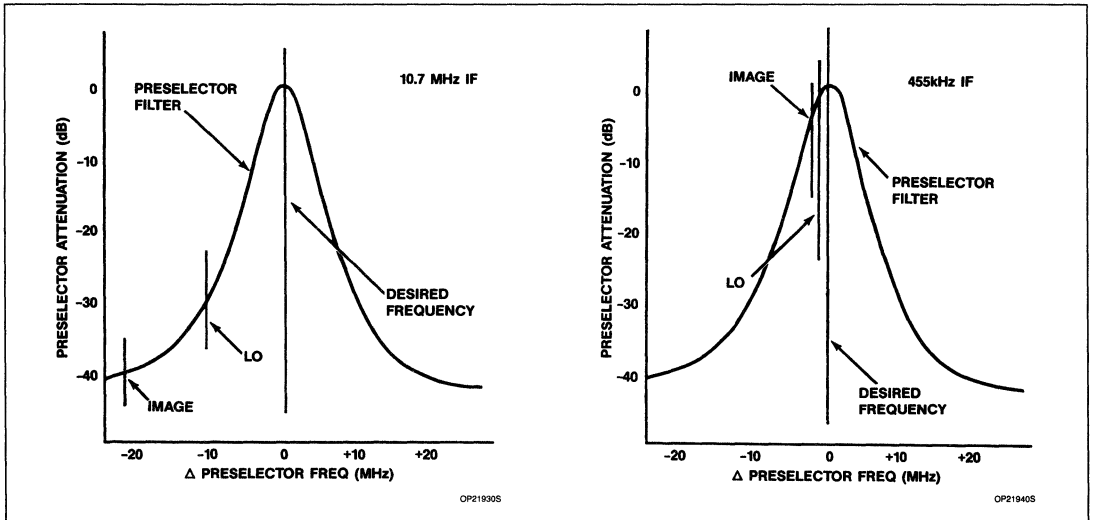


Figure 2. Effects of Preselection on Images

High Sensitivity Applications of Low-Power RF/IF Integrated Circuits

AN1993

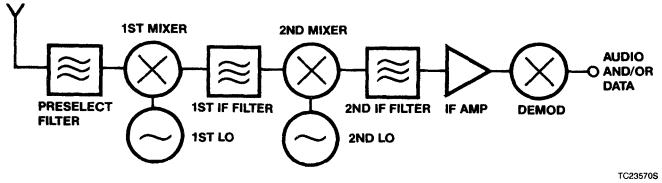


Figure 3. Dual Conversion

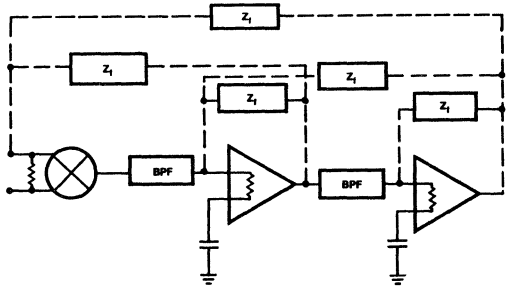


Figure 4. Feedback Paths

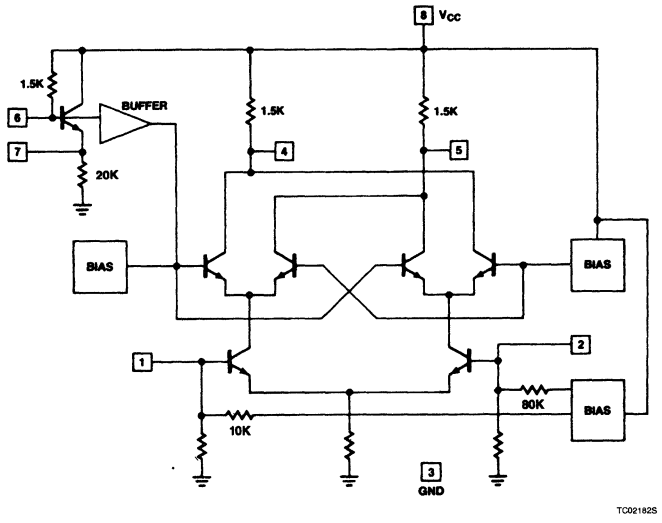


Figure 5. NE602 Equivalent Circuit

A pre-selector (bandpass in this case) precedes a mixer and local oscillator. An IF filter follows the mixer. The IF filter is only supposed to pass the difference (or sum) of the local oscillator (LO) frequency and the preselector frequency.

The reality is that there are always two frequencies which can combine with the LO: The pre-selector frequency and the "image" frequency. Figure 2 shows two hypothetical pre-selection curves. Both have 3dB bandwidths of 2MHz. This type of pre-selection is typical of consumer products such as cordless telephone and FM radio. Figure 2A shows the attenuation of a low side image with 10.7MHz. Figure 2B shows the very limited attenuation of the low side 455kHz image.

If the single conversion architecture of Figure 1 were implemented with a 455kHz IF, any interfering image would be received almost as well as the desired frequency. For this reason, dual conversion, as shown in Figure 3, has been popular.

In the application of Figure 3, the first IF must be high enough to permit the pre-selector to reject the images of the first mixer and must have a narrow enough bandwidth that the second mixer images and the intermod products due to the first mixer can be attenuated There's more to it than that, but those are the basics. The multiple conversion hetrodyne works well, but, as Figure 3 suggests, compared to Figure 2 it is more complicated. Why, then, don't we use the approach of Figure 2?

THE PROBLEM

Historically there has been a problem: Stability! Commercially available integrated IF amplifiers have been limited to about 60dB of gain. Higher discrete gain was possible if each stage was carefully shielded and bypassed, but this can become a nightmare on a production line. With so little IF gain available, in order to receive signals of less than 10μV it was necessary to add RF gain and this, in turn, meant that the mixer must have good large signal handling capability. The RF gain added expense, the high level mixer added expense, both added to the potential for instabilities, so the multiple conversion started looking good again.

But why is instability such a problem in a high gain high IF strip? There are three basic mechanisms. First, ground and the supply line are potentially feedback mechanisms from stage-to-stage in any amplifier. Second, output pins and external components create fields which radiate back to inputs. Third, layout capacitances become feedback mechanisms. Figure 4 shows the fields and capacitances symbolically.

If Z_F represents the impedance associated with the circuit feedback mechanisms (stray capacitances, inductances and radiated fields), and Z_{IN} is the equivalent input imped-

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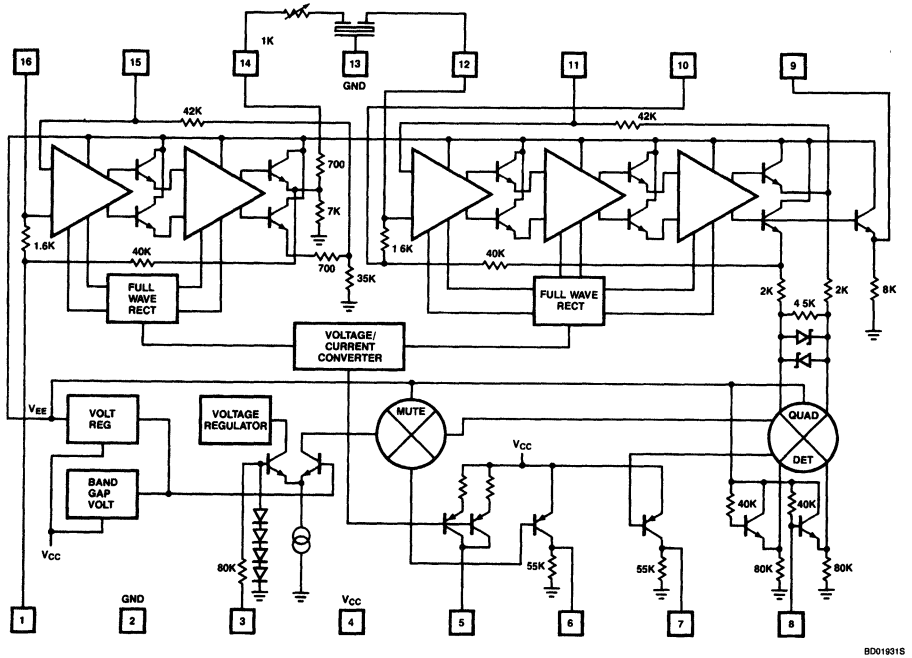

Figure 6. NE604A Equivalent Circuit

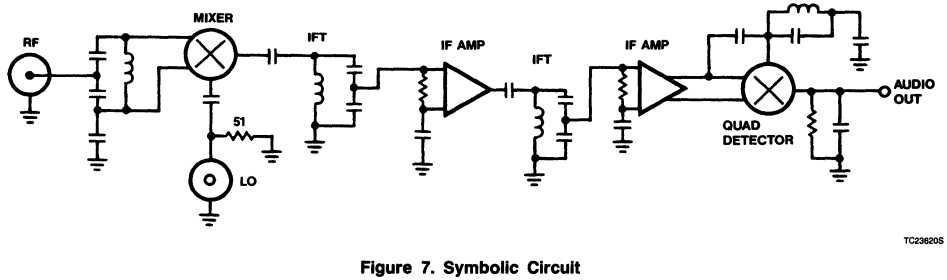

Figure 7. Symbolic Circuit

ance, a divider is created. This divider must have an attenuation factor greater than the gain of the amplifier if the amplifier is to remain stable.

- If gain is increased, the input-to-output isolation factor must be increased.
- As the frequency of the signal or amplifier bandwidth increases, the impedance of the layout capacitance decreases thereby reducing the attenuation factor.

The layout capacitance is only part of the issue. In order for traditional 10.7MHz IF amplifiers to operate with reasonable gain bandwidth, the amount of current in the amplifiers needed to be quite high. The CA3089 operates with 25mA of typical quiescent current. Any currents which are not perfectly differential must be carefully bypassed to ground. The higher the current, the more difficult the challenge. And limiter outputs and quadrature components make excellent field generators which add to the feedback scenario. The higher the current, the larger the field.

THE SOLUTION

The NE602 is a double balanced mixer suitable for input frequencies in excess of 500MHz. It draws 2.5mA of current. The NE604A is an IF strip with over 100dB of gain and a 25MHz small signal bandwidth. It draws 3.5mA of current. The circuits in this paper will demonstrate ways to take advantage of this low current and 75dB or more of the NE604A gain in receivers and IF strips that would not be possible with traditional integrated circuits. No special tricks are used, only good layout, impedance planning and gain distribution.

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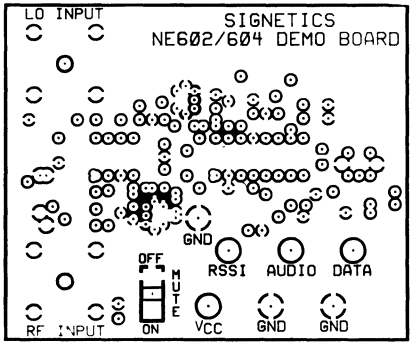

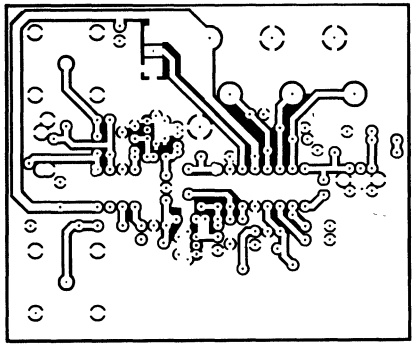

Figure 8. Circuit Board Layout

THE MIXER

The NE602 is a low power VHF mixer with built-in oscillator. The equivalent circuit is shown in Figure 5. The basic attributes of this mixer include conversion gain to frequencies greater than 500MHz, a noise figure of 4.6dB @ 45MHz, and a built-in oscillator which can be used up to 200MHz. LO can be injected.

For best performance with any mixer, the interface must be correct. The input impedance of the NE602 is high, typically 3kΩ in parallel with 3pF. This is not an easy match from 50Ω. In each of the examples which follow, an equivalent 50:1.5k match was used. This compromise of noise, loss, and match yielded good results. It can be improved upon. Match to crystal filters will require special attention, but will not be given focus in this paper.

This oscillator is a single transistor with an internal emitter follower driving the mixer. For best mixer performance, the LO level needs to be approximately 220mV$_{RMS}$ at the base of the oscillator transistor (Pin 6). A number of oscillator configurations are presented at the end of this paper. In each of the prototypes for this paper, the LO source was a signal generator. Thus, a 51Ω resistor was used to terminate the signal generator. The LO is then coupled to the mixer through a DC blocking capacitor. The signal generator is set for 0dBm. The impedance at the LO input (Pin 6) is approximately 20kΩ. Thus, required power is very low, but 0dBm across 51Ω does provide the necessary 220mV$_{RMS}$.

The outputs of the NE602 are loaded with 1.5kΩ internal resistors. This makes interface to 455kHz ceramic filters very easy. Other filter types will be addressed in the examples.

THE IF STRIP

The basic functions of the NE604A are ordinary at first glance: Limiting IF, quadrature detector, signal strength meter, and mute switch. **However, the performance of each of these blocks is superb.** The IF has 100dB of gain and 25MHz bandwidth. This feature will be exploited in the examples. The signal strength indicator has a 90dB log output characteristic with very good linearity. There are two audio outputs with greater than 300kHz bandwidth (one can be muted greater than 70dB). The total supply current is typically 3.5mA. This is the other factor which permits high gain and high IF.

Figure 6 shows an equivalent circuit of the NE604A. Each of the IF amplifiers has a 1.6kΩ input impedance. The input impedance is achieved by splitting a DC feedback bias resistor. The input impedance will be manipulated in each of the examples to aid stability.

BASIC CONSIDERATIONS

In each of the circuits presented, a common layout and system methodology is used. The basic circuit is shown symbolically in Figure 7.

At the input, a frequency selective transformation from 50Ω to 1.5kΩ permits analysis of the circuit with an RF signal generator. A second generator provides LO. This generator second generator provides LO. This generator is terminated with a 51Ω resistor. The output of the mixer and the input of the first limiter are both high impedance (1.5Ω nominal). As indicated previously, the input impedance of the limiter must be low enough to attenuate feedback signals. So, the input impedance of the first limiter is modified with an external resistor. In most of the examples, a 430Ω external resistor was used to create a 330Ω input impedance (430//1.5kΩ). The first IF filter is thus designed to present 1.5kΩ to the mixer and 330Ω to the first limiter.

The same basic treatment was used between the first and second limiters. However, in each of the 10.7MHz examples, this interstage filter is not an L/C tank; it is a ceramic filter. This will be explained in the first example.

After the second limiter, a conventional quadrature detector demodulates the FM or FSK information from the carrier and a simple low pass filter completes the demodulation process at the audio outputs.

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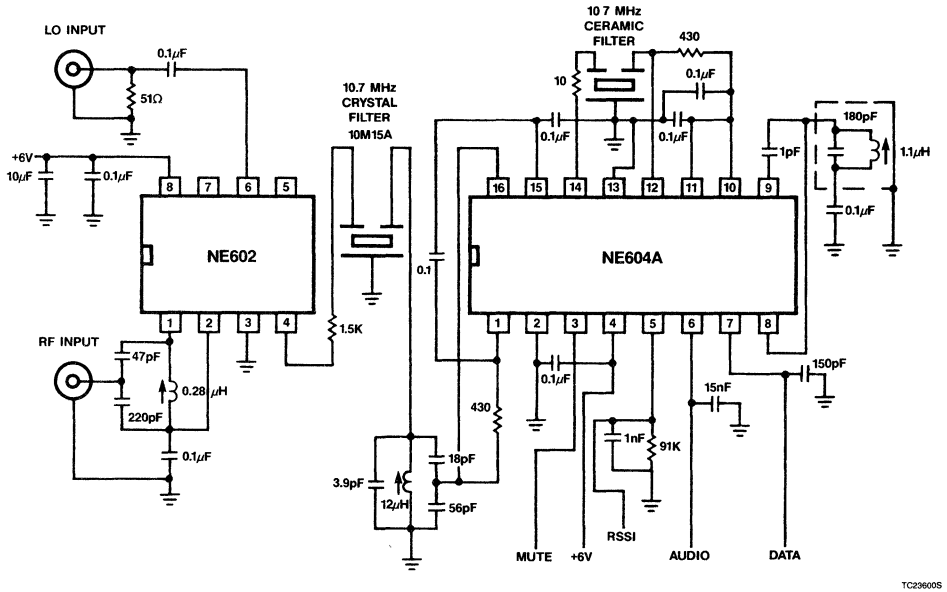


Figure 9. NE602/604A Demonstration Circuit with RF Input of 45MHz and IF of 21.4MHz ± 7.5kHz

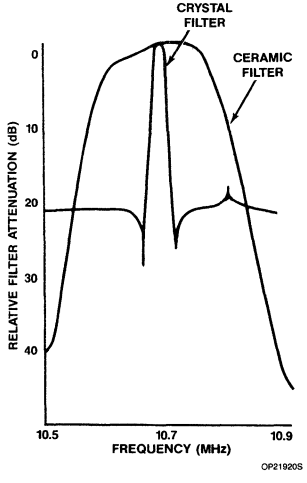
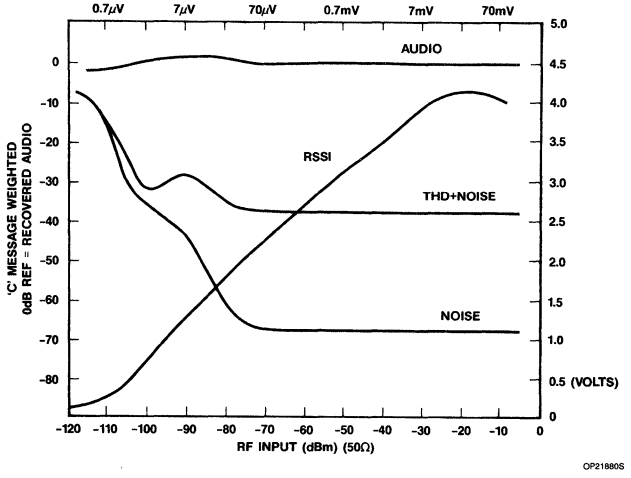


Figure 10. Passband Relationship



- ◆ 45MHz RF Input
- ◆ 55.7MHz LO (0dBm)
- ◆ 10.7MHz IF
- ◆ 15kHz IF BW
- ◆ 7kHz deviation

Figure 11. VHF or UHF 2nd Conversion (Narrow Band)

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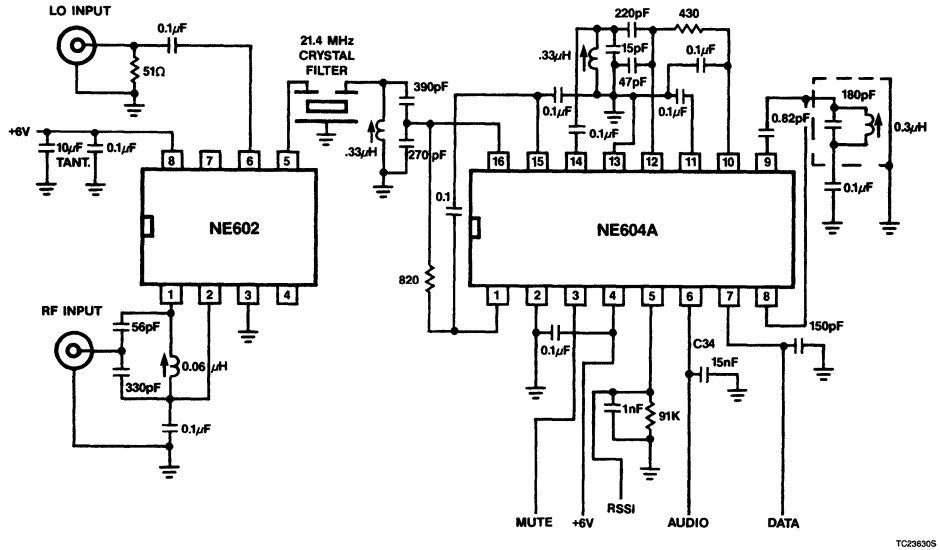


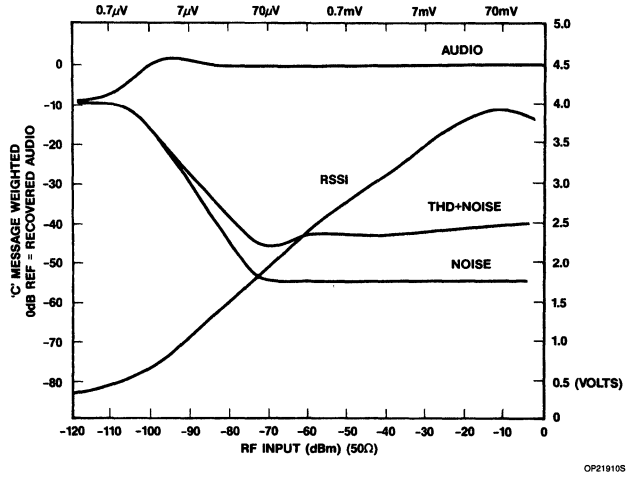
Figure 12. NE602/604A Demonstration Circuit with RF Input of 90MHz and IF of 21.4MHz ± 7.5kHz

As mentioned, a single layout was used for each of the examples. The board artwork is shown in Figure 8. Special attention was given to: (1) Creating a maximum amount of ground plane with connection of the component side and solder side ground at locations all over the board; (2) careful attention was given to keeping a ground ring around each of the gain stages. The objective was to provide a shunt path to ground for any stray signal which might feed back to an input; (3) leads were kept short and relatively wide to minimize the potential for them to radiate or pick up stray signals; finally (and very important), (4) RF bypass was done as close as possible to supply pins and inputs, with a good (10μF) tantalum capacitor completing the system bypass.

EXAMPLE: 45MHz to 10.7MHz NARROWBAND

As a first example, consider conversion from 45MHz to 10.7MHz. There are commercially available filters for both frequencies so this is a realistic combination for a second IF in a UHF receiver. This circuit can also be applied to cordless telephone or short range communications at 46 or 49MHz. The circuit is shown in Figure 9.

The 10.7MHz filter chosen is a type commonly available for 25kHz channel spacing. It has a 3dB bandwidth of 15kHz and a termination requirement of 3kΩ/2pF. To present 3kΩ to the input side of the filter, a 1.5kΩ resistor was used between the NE602 output (which has a 1.5kΩ impedance) and the filter. Layout capacitance was close enough to 2pF that no



- ◆ 90MHz RF Input
- ◆ 68.6MHz LO (0dBm)
- ◆ 21.4MHz IF
- ◆ 15kHz IF BW
- ◆ 7kHz deviation

Figure 13. UHF Second Conversion (Narrow Band) or VHF Single Conversion (Narrow Band)

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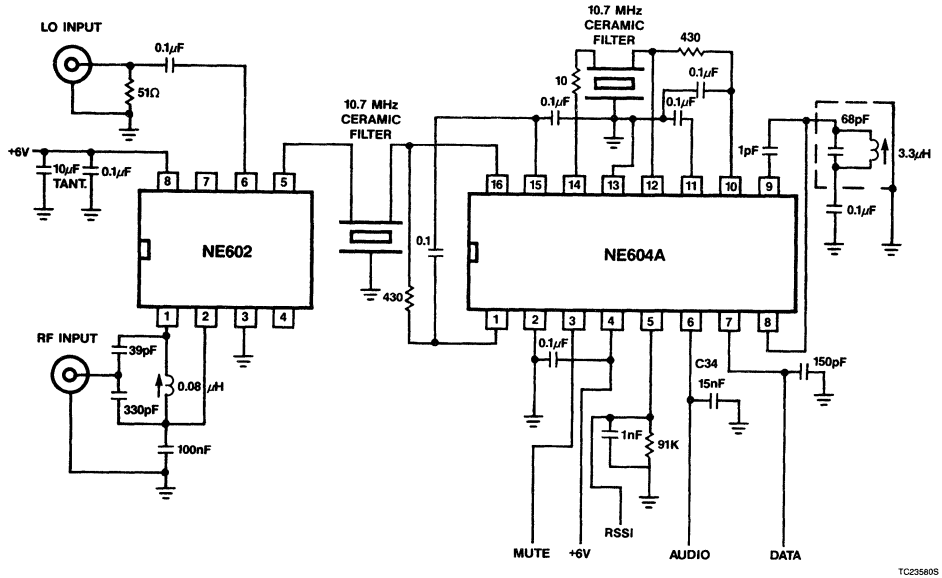


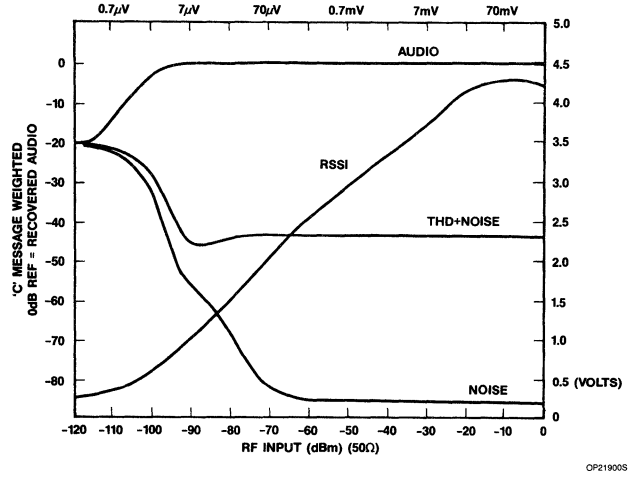
Figure 14. NE602/604A Demonstration Circuit with RF Input of ~100MHz and IF of 10.7MHz ± 140kHz

adjustment was necessary. This series-resistance approach introduces an insertion loss which degrades the sensitivity, but it has the benefit of simplicity.

The secondary side of the crystal filter is terminated with a 10.7MHz tuned tank. The capacitor of the tank is tapped to create a transformer with the ratio for 3k:330. With the addition of the 430Ω resistor in parallel with the NE604A 1.6kΩ internal input resistor, the correct component of resistive termination is presented to the crystal filter. The inductor of the tuned load is adjusted off resonance enough to provide the 2pF capacitance needed. (Actual means of adjustment was for best audio during alignment).

If appropriate or necessary for sensitivity, the same type of tuned termination used for the secondary side of the crystal filter can also be used between the NE602 and the filter. If this is desired, the capacitors should be ratioed for 1.5k:3k. Alignment is more complex with tuned termination on both sides of the filter. This approach is demonstrated in the fourth example.

A ceramic filter is used between the first and second limiters. It is directly connected between the output of the first limiter and the input of the second limiter. Ceramic filters act much like ceramic capacitors, so direct connection between two circuit nodes with different DC levels is acceptable. At the input to the second limiter, the impedance is again reduced by the addition of a 430Ω external resistor in parallel with the internal 1.6kΩ input load resistor. This presents the 330Ω



- ♦ 94.7MHz RF Input
- ♦ 84MHz LO (0dBm)
- ♦ 10.7MHz IF
- ♦ 280kHz IF BW
- ♦ 75kHz deviation

Figure 15. FM Broadcast Receiver (Wide Band)

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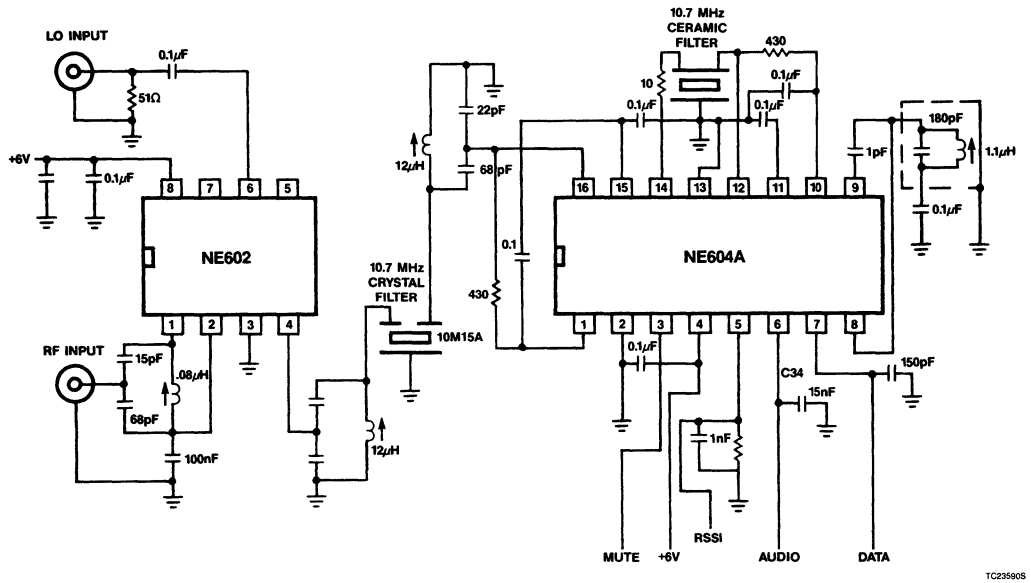
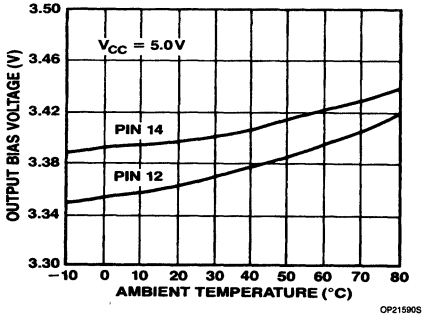


Figure 16. NE602/604A Demonstration Circuit with RF Input of 152.2MHz and IF of 10.7MHz ± 7.5kHz

termination to the ceramic filter which the manufacturers recommend.

On the input side of the ceramic filter, no attempt was made to create a match. The output impedance of the first limiter is nominally 1kΩ. Crystal filters are tremendously sensitive to correct match. Ceramic filters are relatively forgiving. A review of the manufacturers' data shows that the attenuation factor in the passband is affected with improper match, but the degree of change is small and the passband stays centered. Since the principal selectivity for this application is from the crystal filter at the input of the first limiter, the interstage ceramic filter only has to suppress wideband noise. The first filter's passband is right in the center of the ceramic filter passband. (The crystal filter passband is less than 10% of the ceramic filter passband). This passband relationship is illustrated in Figure 10.

After the second limiter, demodulation is accomplished in the quadrature detector. Quadrature criteria is not the topic of this paper, but it is noteworthy that the choice of loaded Q will affect performance. The NE604A is specified at 455kHz using a quadrature capacitor of 10pF and a tuning capacitor of 180pF. (180pF gives a loaded Q of 20 at 455kHz). A careful look at the quadrature equations (Ref 3.) suggests that at 10.7MHz a value of about 1pF should be substituted for the 10pF at 455kHz.



- ♦ 152.2MHz RF Input
- ♦ 141.5MHz LO (0dBm)
- ♦ 10.7kHz IF
- ♦ 15kHz IF BW
- ♦ 7kHz deviation

Figure 17. VHF Single Conversion (Narrow Band)

The performance of this circuit is presented in Figure 11. The −12dB SINAD (ratio of Signal to Noise And Distortion) was achieved with a 0.6μV input.

EXAMPLE: 90MHz to 21.4MHz NARROWBAND

This second example, like the first, used two frequencies which could represent the intermediate frequencies of a UHF receiver. This circuit can also be applied to VHF single conversion receivers if the sensitivity is appropriate. The circuit is shown in Figure 12.

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Most of the fundamentals are the same as explained in the first example. The 21.4MHz crystal filter has a 1.5kΩ/2pF termination requirement so direct connection to the output of the NE602 is possible. With strays there is probably more than 2pF in this circuit, but the performance is good nonetheless. The output of the crystal filter is terminated with a tuned impedance-step-down transformer as in the previous example. Interstage filtering is accomplished with a 1kΩ 330 step-down ratio. (Remember, the output of the first limiter is 1kΩ and a 430Ω resistor has been added to make the second limiter input 330Ω). A DC blocking capacitor is needed from the output of the first limiter. The board was not laid out for an interstage transformer, so an "XACTO" knife was used to make some minor mods. Figure 13 shows the performance. The +12dB SINAD was with 1.6μV input.

EXAMPLE: 100MHz to 10.7MHz WIDEBAND

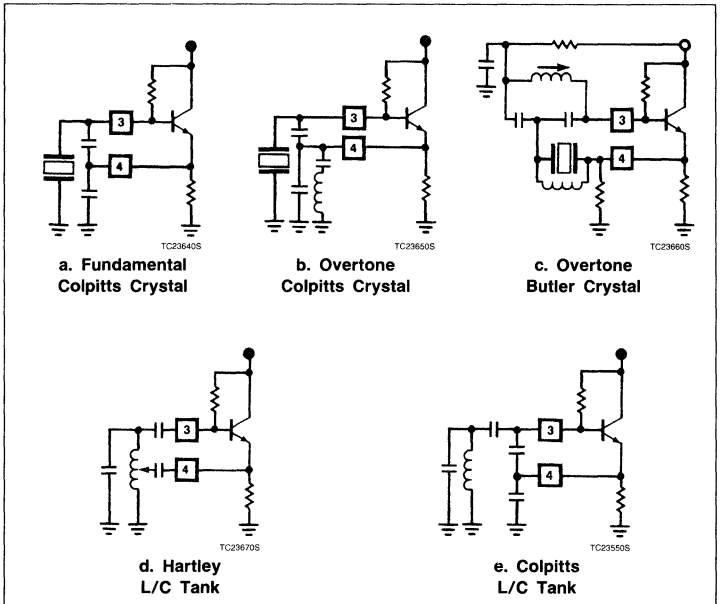
This example represents three possible applications: (1) low cost, sensitive FM broadcast receivers, (2) SCA (Subsidiary Communications Authorization) receivers and (3) data receivers. The circuit schematic is shown in Figure 14. While this example has the greatest diversity of application, it is also the simplest. Two 10.7MHz ceramic filters were used. The first was directly connected to the output of the NE602. The second was directly connected to the output of the first IF limiter. The secondary sides of both filters were terminated with 330Ω as in the two previous examples. While the filter bandpass skew of this simple single conversion receiver might not be tolerable in some applications, to a first order the results are excellent. (Please note that sensitivity is measured at +20dB in this wideband example.) Performance is illustrated in Figure 15. +20dB SINAD was measured with 1.8μV input.

EXAMPLE: 152.2MHz to 10.7MHz NARROWBAND

In this example (see Figure 16) a simple, effective, and relatively sensitive single conversion VHF receiver has been implemented. All of the circuit philosophy has been described in previous examples. In this circuit, tuned-transformed termination was used on the input and output sides of the crystal filter. Performance is shown in Figure 17. The +12dB SINAD sensitivity was 0.9μV.

OSCILLATORS

The NE602 contains an oscillator transistor which can be used to frequencies greater than 200MHz. Some of the possible configurations are shown in Figures 18 and 19.



a. Fundamental Colpitts Crystal

b. Overtone Colpitts Crystal

c. Overtone Butler Crystal

d. Hartley L/C Tank

e. Colpitts L/C Tank

Figure 18. Oscillator Configurations

L/C

When using a synthesizer, the LO must be externally buffered. Perhaps the simplest approach is an emitter follower with the base connected to Pin 7 of the NE602. The use of a dual-gate MOSFET will improve performance because it presents a fairly constant capacitance at its gate and because it has very high reverse isolation.

CRYSTAL

With both of the Colpitts crystal configurations, the load capacitance must be specified. In the overtone mode, this can become a sensitive issue since the capacitance from the emitter to ground is actually the equivalent capacitive reactance of the harmonic selection network. The Butler oscillator uses an overtone crystal specified for series mode operation (no parallel capacitance). It may require an extra inductor (L_o) to null out C_o of the crystal, but otherwise is fairly easy to implement (see references).

The oscillator transistor is biased with only 220μA. In order to assure oscillation in some configurations, it may be necessary to increase transconductance with an external resistor from the emitter to ground. 10kΩ to 20kΩ are acceptable values. Too small a resistance can upset DC bias (see references).

DATA DEMODULATION

It is possible to change any of the examples from an audio receiver to an amplitude shift keyed (ASK) or frequency shift keyed (FSK) receiver or both with the addition of an external op amp(s) or comparator(s). A simple example is shown in Figure 20. ASK decoding is accomplished by applying a comparator across the received signal strength indicator (RSSI). The RSSI will track IF level down to below the limits of the demodulator (−120dBm RF input in most of the examples). When an in-band signal is above the comparator threshold, the output logic level will change.

FSK demodulation takes advantage of the two audio outputs of the NE604A. Each is a PNP current source type output with 180° phase relationship. With no signal present, the quad tank tuned for the center of the IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the IF center, one output voltage will increase and the other will decrease by a corresponding absolute value. Thus, if a comparator is differentially connected across the two out-

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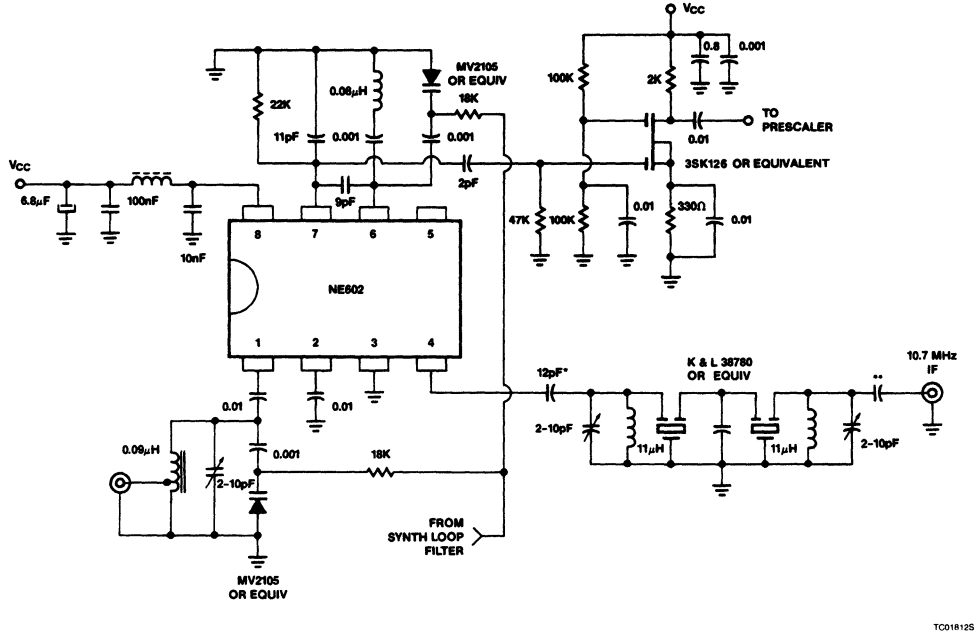
puts, a frequency shift in one direction will drive the comparator output to one supply rail, and a frequency shift in the opposite direction will cause the comparator output to swing to the opposite rail. Using this technique, and L/C filtering for a wide IF bandwidth, NRZ data at rates greater than 4Mb have been processed with the new NE605.



* Permits impedance match of NE602 output of 1.8k/8pF to 3 0k filter impedance
* * Choose for impedance match to

Figure 19. Typical Varactor Tuned Application

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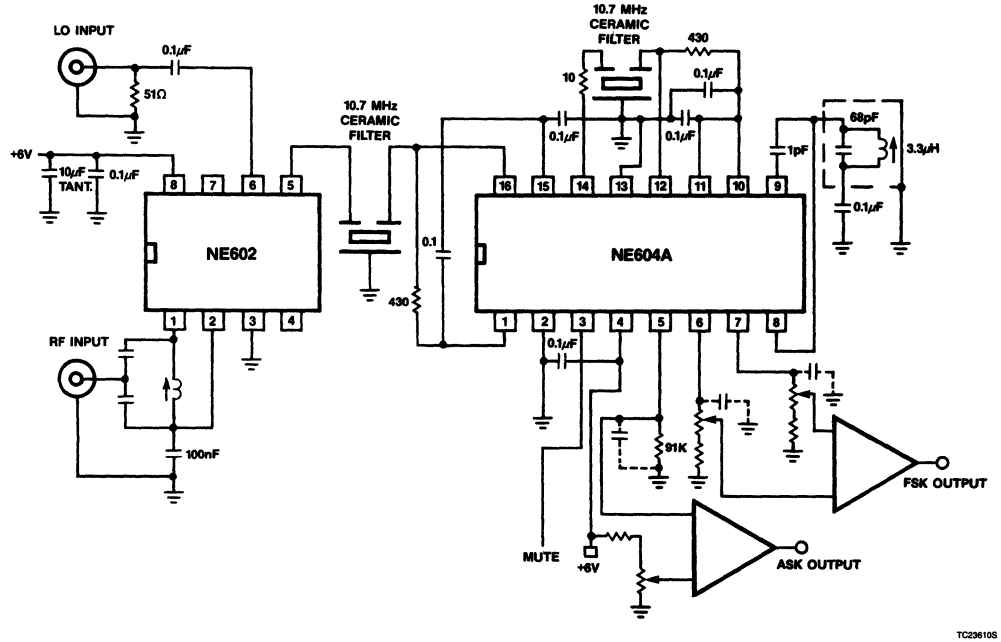

Figure 20. Basic NE602/604A Data Receiver

SUMMARY

The NE602, NE604A and NE605 provide the RF system designer with the opportunity for excellent receiver or IF system sensitivity with very simple circuitry. IFs at 455kHz, 10.7MHz and 21.4MHz with 75 to 90dB gain are possible without special shielding. The flexible configuration of the built-in oscillator of the NE602/605 add to ease of implementation. Either data or audio can be recovered from the NE604A/605 outputs.

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5) Signetics; "NE/SA602 Double Balanced Mixer and Oscillator", *Linear Data and Applications Manual,* Signetics, 1985.

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Signetics

NE/SA605
High-Performance Low Power Mixer FM IF System

Preliminary Specification

Linear Products

DESCRIPTION

The NE/SA605 is a high performance monolithic low power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features higher mixer input intercept, higher IF bandwidth (25MHz) and temperature compensated RSSI, and limiters permitting higher performance application. The NE/SA605 is available in a 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

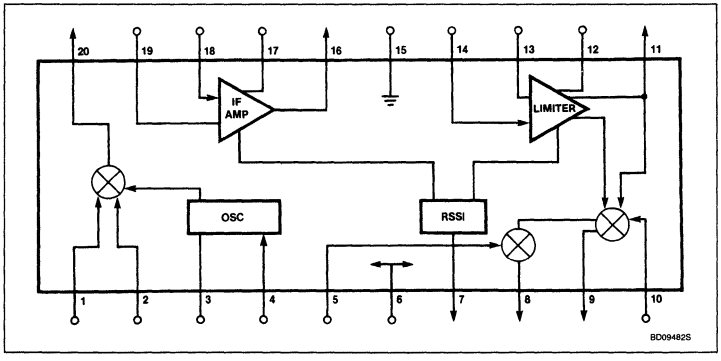
FEATURES

- **Low-power consumption 5.7mA typical at 6V**
- **Mixer input to > 500MHz**
- **Mixer conversion power gain of 13dB at 45MHz**
- **Mixer noise figure of 4.6dB at 45MHz**
- **XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)**
- **102dB of limiter gain**
- **25MHz limiter small signal bandwidth**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs - muted and unmuted**
- **Low external component count; suitable for crystal/ceramic/LC filters**

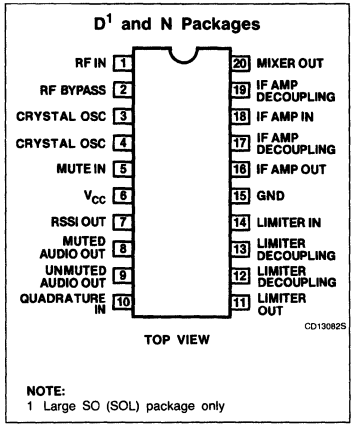
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE605N
20-Pin Plastic SOL (Surface-mounted)	0°C to +70°C	NE605D
20-Pin Plastic DIP	-40 to +85°C	SA605N
20-Pin Plastic SOL (Surface-mounted)	-40 to +85°C	SA605D

BLOCK DIAGRAM



PIN CONFIGURATION



NOTE:
1 Large SO (SOL) package only

- **Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz**
- **SA605 meets cellular radio specifications**
- **ESD hardened**

APPLICATIONS

- **High performance communications receivers**
- **Cellular Radio FM IF**
- **Single conversion VHF/UHF receivers**
- **SCA receivers**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**
- **Log amps**
- **Wideband low current amplification**

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating temperature		
	NE605	0 to +70	°C
	SA605	−40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE605			SA605			
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (on)		1.7			1.7			V
	(off)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; RF frequency = 455kHz, R17 = 5.1k; RF level = 45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE605			SA605			
			Min	Typ	Max	Min	Typ	Max	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHZ
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order intercept point	f1 = 45.0; f2 = 45.06MHz		−10			−10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		−1.7			−1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting −3dB, $R_{17} = 5.1k$	Test at Pin 18		−113			−113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, $R_{10} = 100k$	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Unmuted audio level, $R_{11} = 100k$	150pF de-emphasis		530			530		mV_{RMS}
	SINAD sensitivity	RF level −118dBm		16			16		dB
THD	Total harmonic distortion		−35	−42		−34	−42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB

AC ELECTRICAL CHARACTERISTICS (Continued) Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; RF frequency = 455kHz, R17 = 5.1k; RF level = 45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE605			SA605			
			Min	Typ	Max	Min	Typ	Max	
	IF RSSI output, $R_9 = 100k$[1]	IF level = −118dBm	0	160	550	0	160	650	mV
	1.5k input	IF level = −68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = −18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	$R_9 = 100k\Omega$ Pin 16		90			90		dB
	RSSI accuracy	$R_9 = 100k\Omega$ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output impedance			58			58		kΩ
	Muted audio output impedance	Test at Pin 18		58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	$4.5V = V_{CC}$, RF level = −27dBm		480			480		mV_{RMS}
	System RSSI output	RF level = −27dBm, $4.5V = V_{CC}$		4.3			4.3		V

NOTE:

1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE604A (1.5k)/NE605 (1.5k)
−97dBm	−118dBm
−47dBm	−68dBm
+3dBm	−18dBm

The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A

CIRCUIT DESCRIPTION

The NE/SA605 is an RF/IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz with 39.7dBV of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dBV of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third order intercept of −10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations, either Hartley or Colpitts. For crystal oscillators, the Colpitts configuration is used up to 150MHz.

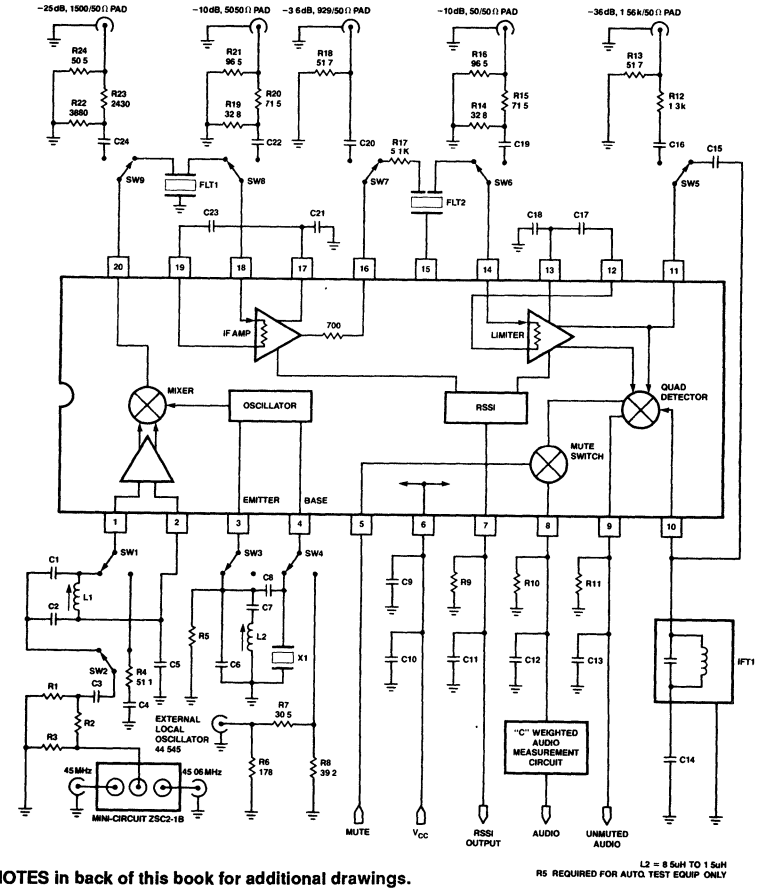
The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dBV insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dBV insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.



See NOTES in back of this book for additional drawings.

Figure 1. NE/SA605 45MHz Test Circuit and Application Circuit (Relays as shown)

Application Component List

C1 100pF NPO Ceramic
C2 390pF NPO Ceramic
C5 100nF ±10% Monolithic Ceramic
C6 22pF NPO Ceramic
C7 1nF Ceramic
C8 5.6pF NPO Ceramic (minimum)
C9 100nF ±10% Monolithic Ceramic
C10 15μF Tantalum (minimum)
C11 100nF ±10% Monolithic Ceramic
C12 15nF ±10% Ceramic
C13 150pF ±2% N1500 Ceramic
C14 100nF ±10% Monolithic Ceramic
C15 10pF NPO Ceramic
C17 100nF ±10% Monolithic Ceramic
C18 100nF ±10% Monolithic Ceramic
C21 100nF ±10% Monolithic Ceramic
C23 100nF ±10% Monolithic Ceramic
Flt1 Ceramic Filter Murata SFG455A3 or equiv
Flt2 Ceramic Filter Murata SFG455A3 or equiv
IFT1 455kHz (Ce = 180pF) RMC-2A6597H
L1 147-160nH Coilcraft UNI-10/142-04J08S
L2 0.5-1.3μH, 800nH nominal
Coilcraft UNI-10/143-16J12S
Coilcraft SLOTTEN-04-01
Toko 113KN-2K353HM
X1 44.545MHz Crystal ICM4712701
R9 100k ±1% 1/4W Metal Film
R17 5.1k ±5% 1/4W Carbon Composition
R5 Not used in application; required for auto test equipment only
R10 100k ±1% 1/4W Metal Film (optional)
R11 100k ±1% 1/4W Metal Film (optional)

Signetics

NE/SA614A
Low Power FM IF System

Linear Products

Preliminary Specification

DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature package).

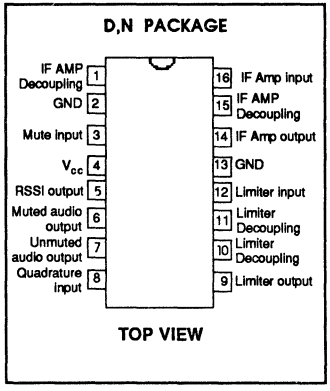
FEATURES

- **Low-power consumption 3.3mA typical**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs - muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA614A meets consumer cellular radio specifications**

APPLICATIONS

- **Consumer cellular radio FM IF**
- **Consumer communications receivers**
- **Intermediate frequency amplification and detection up to 25MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**

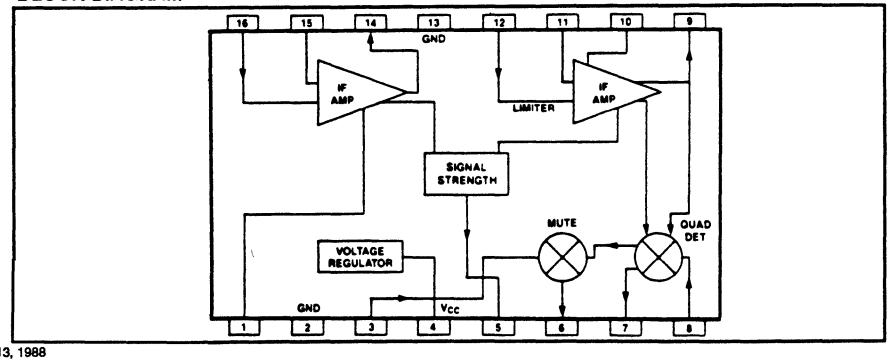
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614AN
16-Pin Plastic SO (Surface-mounted miniature package);	0 to +70°C	NE614AD
16-Pin Plastic DIP	-40 to +85°C	SA614AN
16-Pin Plastic SO (Surface-mounted miniature package);	-40 to +85°C	SA614AD

BLOCK DIAGRAM



September 13, 1988

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	-65 to +150	°C
Operating temperature		
NE614A	0 to 70	°C
SA614A	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C; V_{CC} = +6V unless otherwise stated

PARAMETER	TEST CONDITIONS	NE614A			SA614A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Power supply voltage range		4.5		8.0	4.5		8.0	V
DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
Mute switch input threshold (on)		1.7			1.7			V
(off)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS Typical reading at T_A = 25°C; V_{CC} = +6V unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

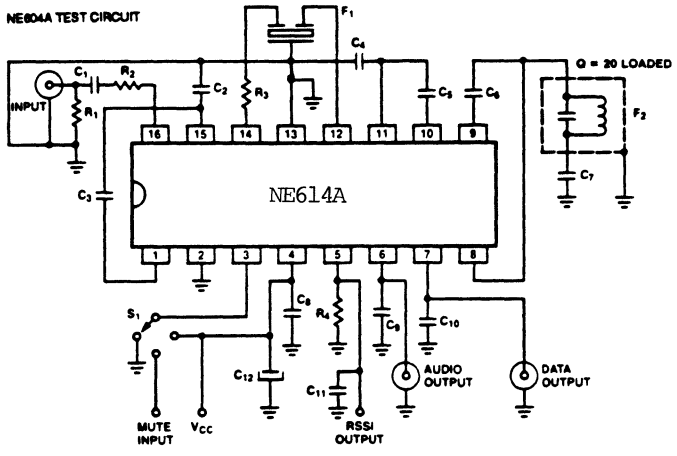
PARAMETER	TEST CONDITIONS	NE/SA614A			UNIT
		MIN	TYP	MAX	
Input limiting - 3dB	Test at Pin 16		-92		dBm/50Ω
AM rejection	80% AM 1kHz	25	33		dB
Recovered audio level	15nF de-emphasis	60	175	260	mV_{rms}
Recovered audio level	150pF de-emphasis		530		mV_{rms}
SINAD sensitivity	RF level -97dBm		12		dB
THD		-30	-42		dB
Signal-to-noise ratio	No modulation for noise		68		dB
RSSI output	RF level = -118dBm	0	160	800	mV
	RF level = -68dBm	1.7	2.50	3.3	V
	RF level = -18dBm	3.6	4.80	5.8	V
RSSI range	R_1 = 100k Pin 5		80		dB
RSSI accuracy	R_1 = 100k Pin 5		±2.0		dB
IF input impedance		1.4	1.6		kΩ
IF output impedance		0.85	1.0		kΩ
Limiter input impedance		1.4	1.6		kΩ
Unmuted audio output resistance			58		kΩ
Muted audio output resistance			58		kΩ

NOTE:

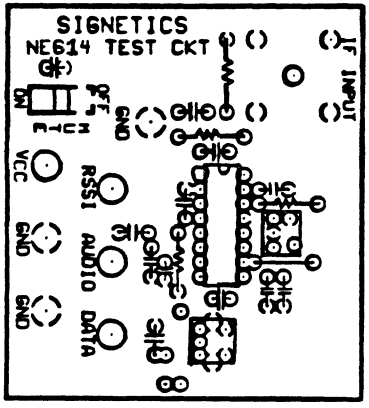
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

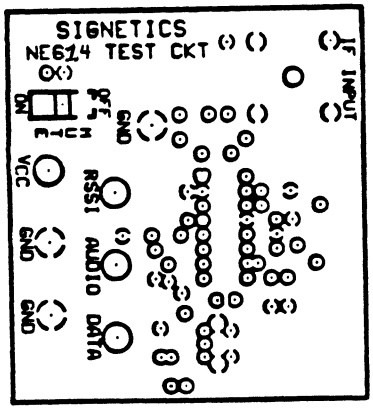
NE614A (50)	NE614A (1.5k)/NE615 (1.5k)
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1 10nF +80-20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V
C3 100nF ± 10% 50V
C4 100nF ± 10% 50V
C5 100nF ± 10% 50V
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V
C8 100nF ± 10% 50V
C9 15nF ± 10% 50V
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8uF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film





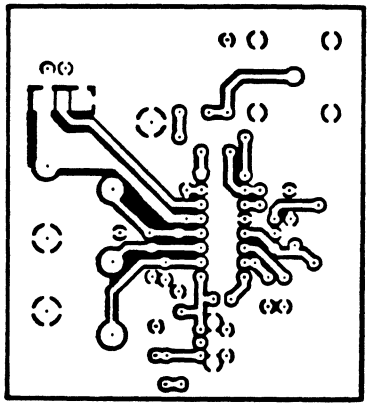


Figure 1. NE614A Test Circuit

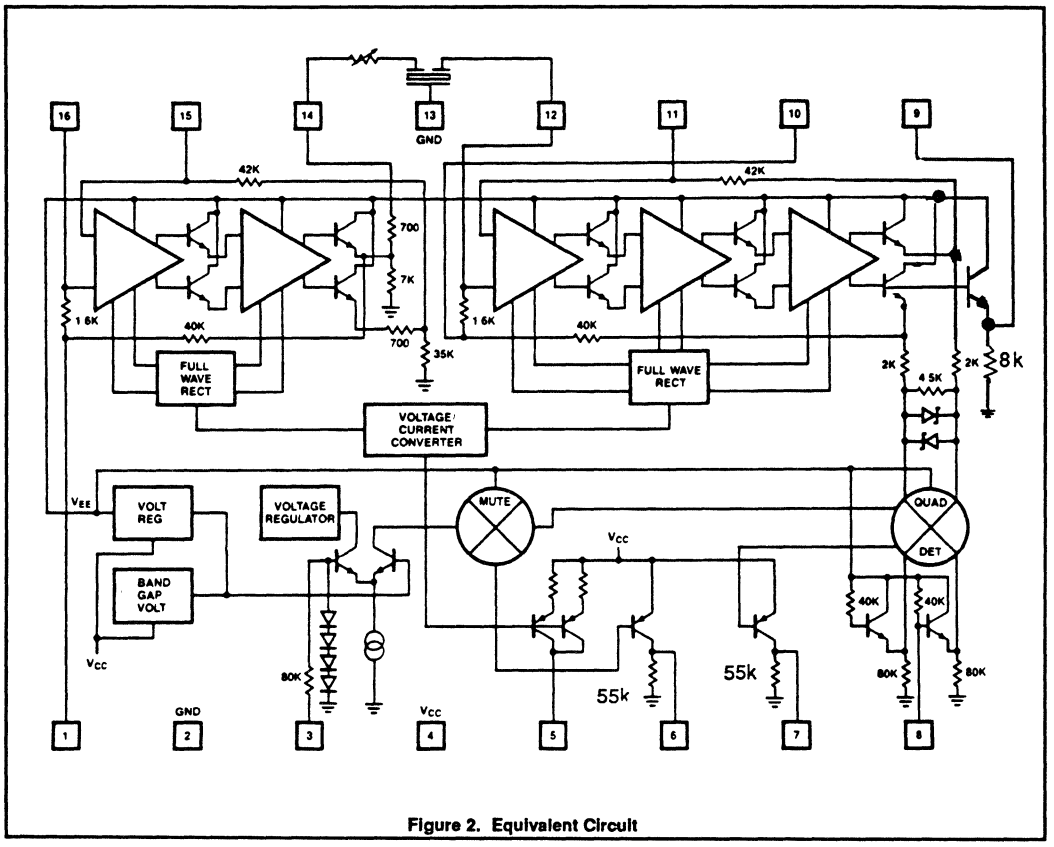


Figure 2. Equivalent Circuit

Circuit Description

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A can not be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2 the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feed-

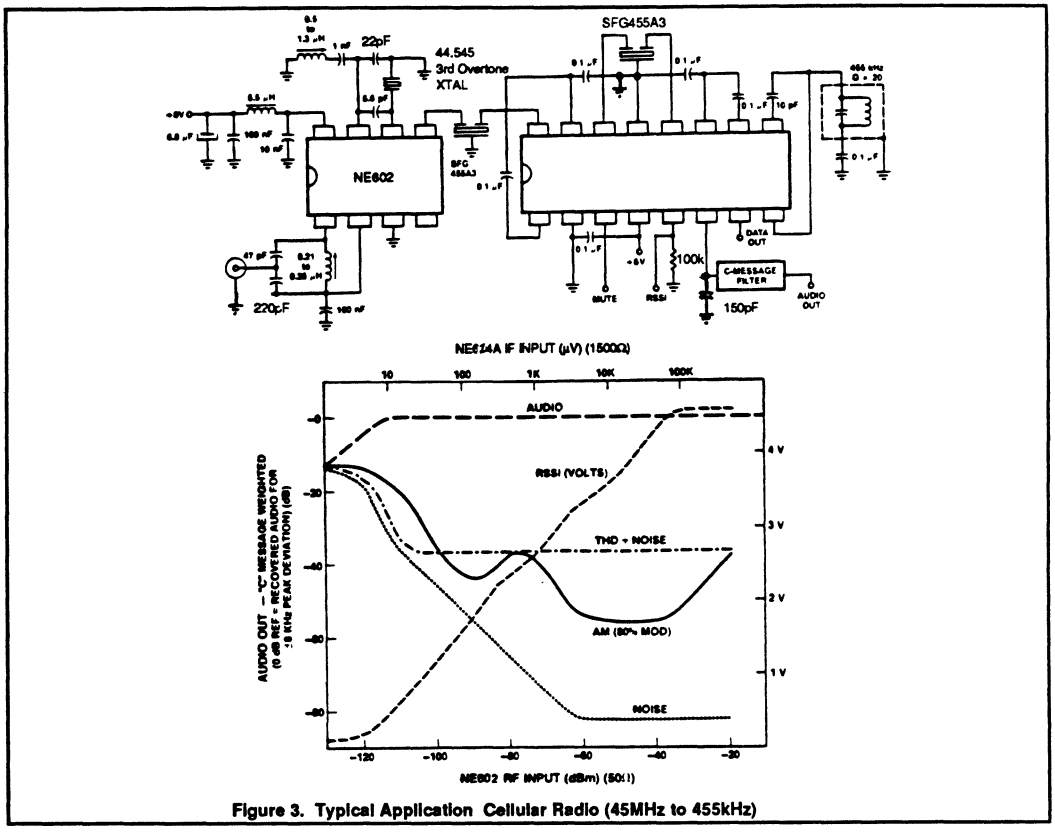


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

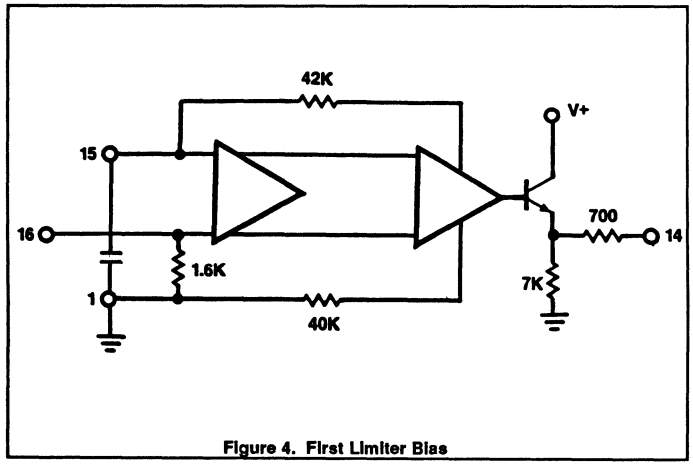


Figure 4. First Limiter Bias

back (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including the RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the

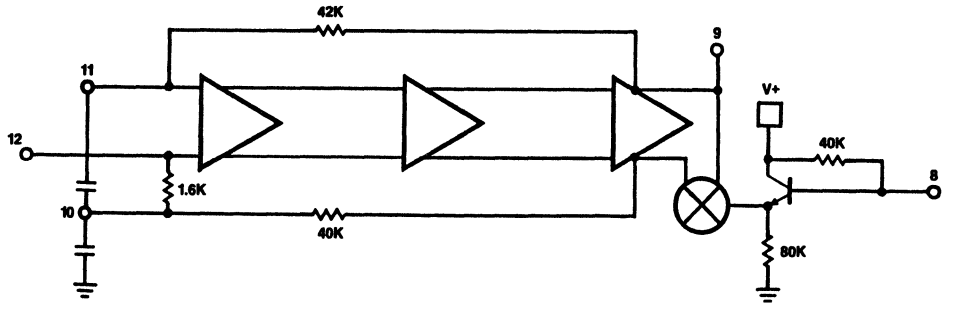


Figure 5. Second Limiter and Quadrature Detector

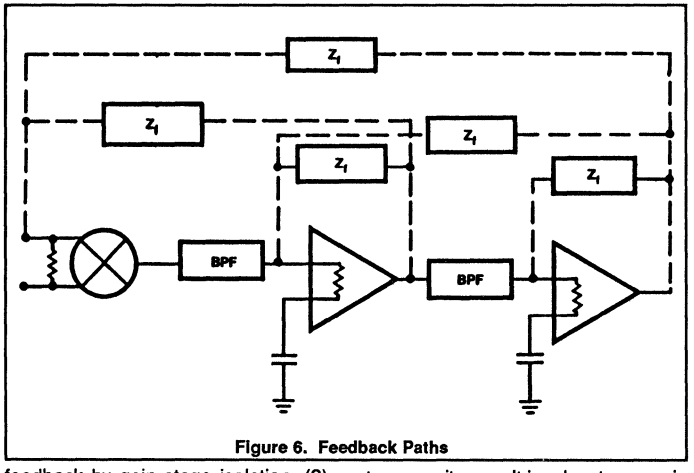


Figure 6. Feedback Paths

feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

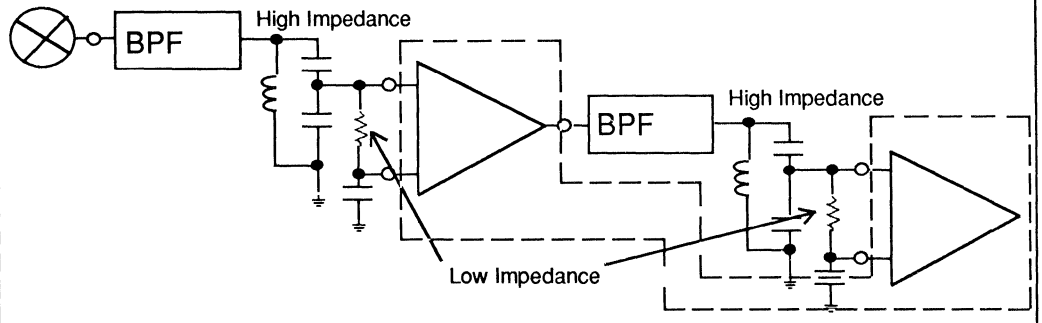
A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

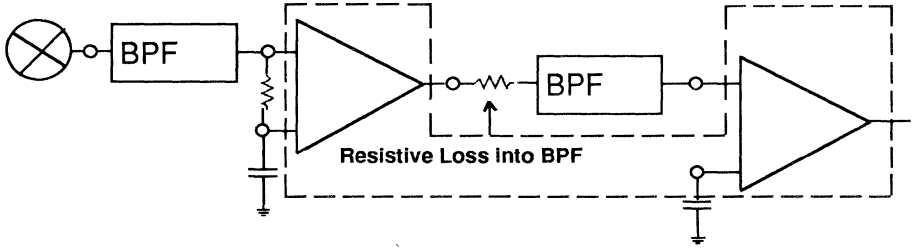
The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{cc} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptible with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

the filters. The input filter is a crystal type for narrow-band selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

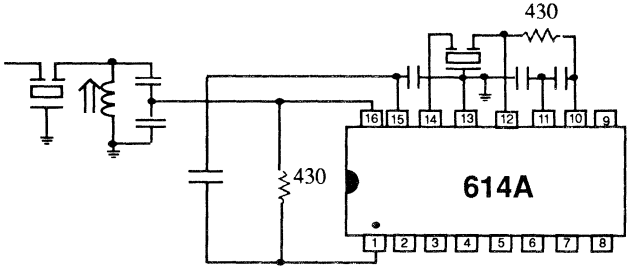


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the nonlinearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first order effects only.

Frequency discriminator design equations for NE614A

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_N \qquad (1a)$$

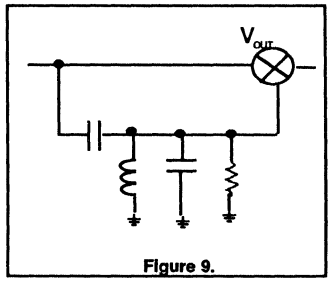


Figure 9.

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \qquad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \qquad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_s will be:

$$\phi = \angle V_O - \angle V_N = \qquad (2)$$

$$tg^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right]$$

Figure 10. Is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of

$$\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$$

The signal V_o would have a phase shift of $\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t$ (3)

$$\Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_N \cdot V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] \qquad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] \qquad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\left(\frac{\omega}{\omega_1}\right) = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \qquad (6)$$

For $\frac{2Q_1\omega}{\omega_1} \ll \frac{\pi}{2}$

Which is the discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.)

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley,1980, p.311. Example: At 455kHz IF, with ±5kHz FM deviation. The max/min normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the ϕ vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\left(\frac{\omega}{\omega_1}\right) = 1.01$. The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq.6)

$\Rightarrow$ Choose a Q = 20.

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$$C_p + C_s = 174pF \text{ and } L = 0.7mH.$$

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_s = 10pF and C_p =164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_s = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. This response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be the logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB . The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

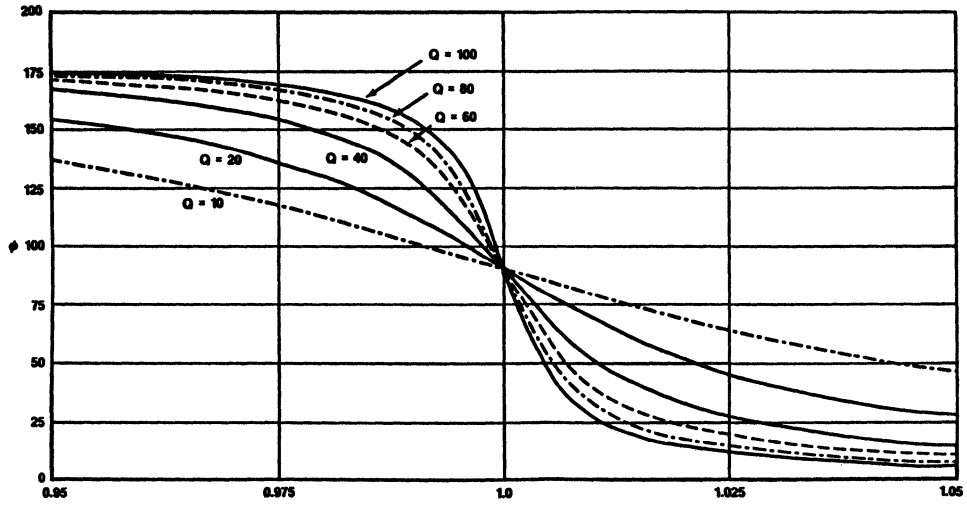


Figure 10. Phase vs. Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

Signetics

NE/SA615
High-Performance Low Power Mixer FM IF System

Preliminary Specification

Linear Products

DESCRIPTION

The NE/SA615 is a consumer monolithic low power FM IF system incorporating a mixer/osc, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 is available in a 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package).

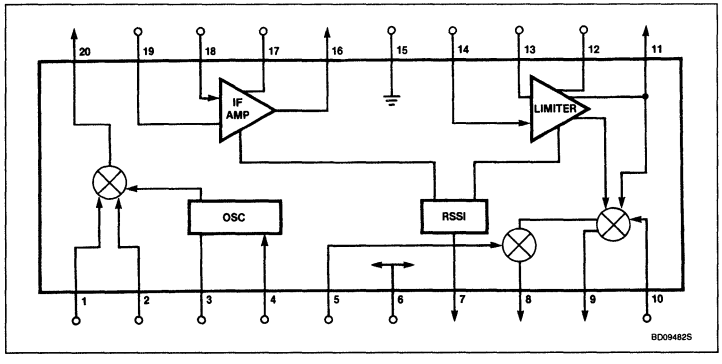
FEATURES

- **Low-power consumption 5.7mA typical at 6V**
- **Mixer input to > 500MHz**
- **Mixer conversion power gain of 13dB at 45MHz**
- **Mixer noise figure of 4.6dB at 45MHz**
- **XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)**
- **102dB of limiter gain**
- **25MHz limiter small signal bandwidth**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs - muted and unmuted**
- **Low external component count; suitable for crystal/ceramic/LC filters**

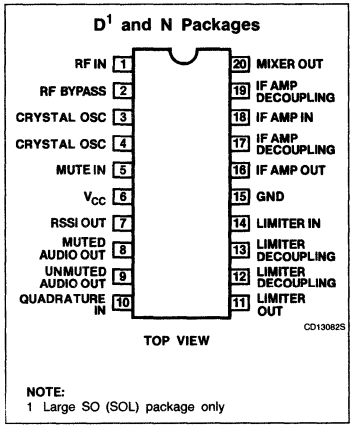
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE615N
20-Pin Plastic SOL (Surface-mounted)	0°C to +70°C	NE615D
20-Pin Plastic DIP	-40°C to +85°C	SA615N
20-Pin Plastic SOL (Surface-mounted)	-40°C to +85°C	SA615D

BLOCK DIAGRAM



PIN CONFIGURATION



NOTE:
1 Large SO (SOL) package only

- **Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz**
- **SA615 meets cellular radio specifications**
- **ESD hardened**
- **Will handle IF frequencies up to 25MHz**

APPLICATIONS

- **Consumer cellular radio FM IF**
- **Single conversion VHF/UHF receivers**
- **SCA receivers**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**
- **Log amps**
- **Wideband low current amplification**

4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating temperature NE605 SA605	 0 to +70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			NE/SA615			
			Min	Typ	Max	
	Power supply voltage range		4.5		8.0	V
	DC current drain			5.7	7.4	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 45MHz, + 14.5dBV RF input step-up; IF frequency = 455kHz, $R_{17} = 5.1k$; RF level = −45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			NE/SA615			
			Min	Typ	Max	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order intercept point	f1 = 45.0; f2 = 45.06MHz		−12		dBm
	Conversion power gain	Matched 14.5dBV step-up 50Ω source	8.0	13 −1.7		dB dB
R_{IN}	RF input resistance	Single-ended input	3.0	4.7		kΩ
C_{IN}	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting −3dB, $R_{17} = 5.1k$	Test at Pin 18		−109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, $R_{10} = 100k$	15nF de-emphasis	60	175	260	mV_{RMS}
	Unmuted audio level, $R_{11} = 100k$	150pF de-emphasis		530		mV_{RMS}
	SINAD sensitivity	RF level −118dBm		12		dB
THD	Total harmonic distortion		−30	−42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB

AC ELECTRICAL CHARACTERISTICS (Continued) Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. RF frequency = 45MHz, + 14.5dBV RF input step-up; IF frequency = 455kHz, $R_{17} = 5.1k$; RF level = −45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			NE/SA615			
			Min	Typ	Max	
	IF RSSI output, $R_9 = 100k$[1]	IF level = −118dBm	0	160	800	mV
		IF level = −68dBm	1.7	2.5	3.3	V
		IF level = −18dBm	3.6	4.8	5.8	V
	RSSI range	$R_9 = 100k\Omega$ Pin 7		80		dB
	RSSI accuracy	$R_9 = 100k\Omega$ Pin 7		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		kΩ
	Unmuted audio output impedance			58		kΩ
	Muted audio output impedance	Test at Pin 18		58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = −27dBm		480		mV_{RMS}
	System RSSI output	RF level = −27dBm, 4.5V = V_{CC}		4.3		V

NOTE:

1. NE614 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE614 (50)	NE614A (1.5k)/NE615 (1.5k)
−97dBm	−118dBm
−47dBm	−68dBm
+3dBm	−18dBm

The NE615 and NE614 are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.

CIRCUIT DESCRIPTION

The NE/SA615 is an RF/IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz with 39.7dBV of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dBV of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert Cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third order intercept of −10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations, either Hartley or Colpitts. For crystal oscillators, the Colpitts configuration is used up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dBV insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dBV insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

High-Performance Low Power Mixer FM IF System | NE/SA615

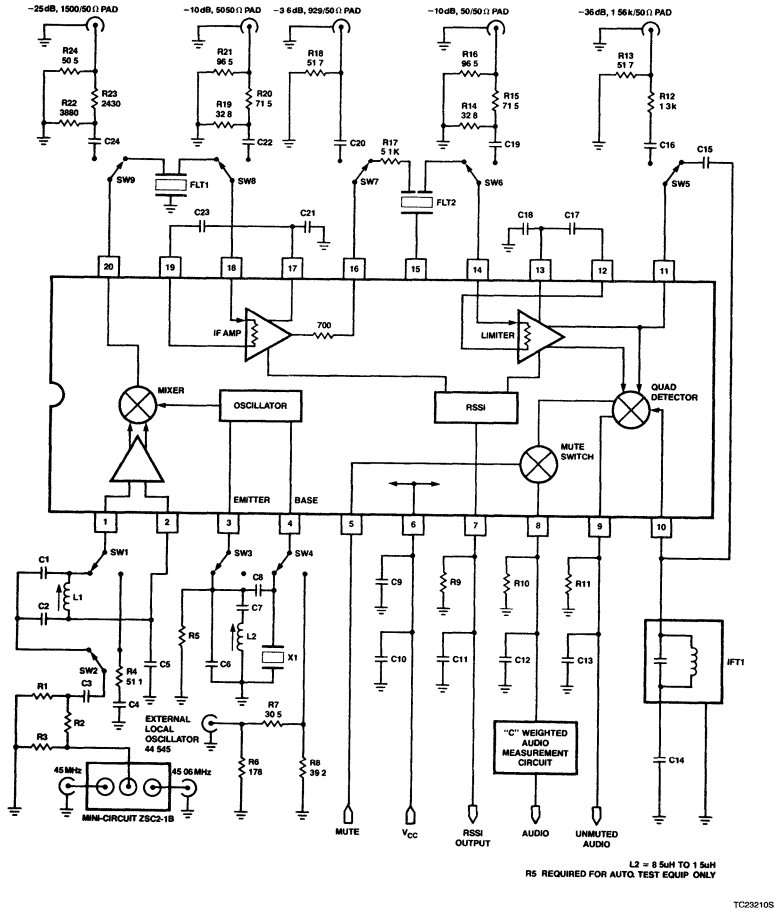


Figure 1. NE/SA615 45MHz Test Circuit and Application Circuit (Relays as shown)

Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	5.6pF NPO Ceramic (minimum)
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
Flt1	Ceramic Filter Murata SFG455A3 or equiv
Flt2	Ceramic Filter Murata SFG455A3 or equiv
IFT1	455kHz (Ce = 180pF) RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	0.5-1.3μH, 800nH nominal Coilcraft UNI-10/143-16J12S Coilcraft SLOTTEN-04-01 Toko 113KN-2K353HM
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

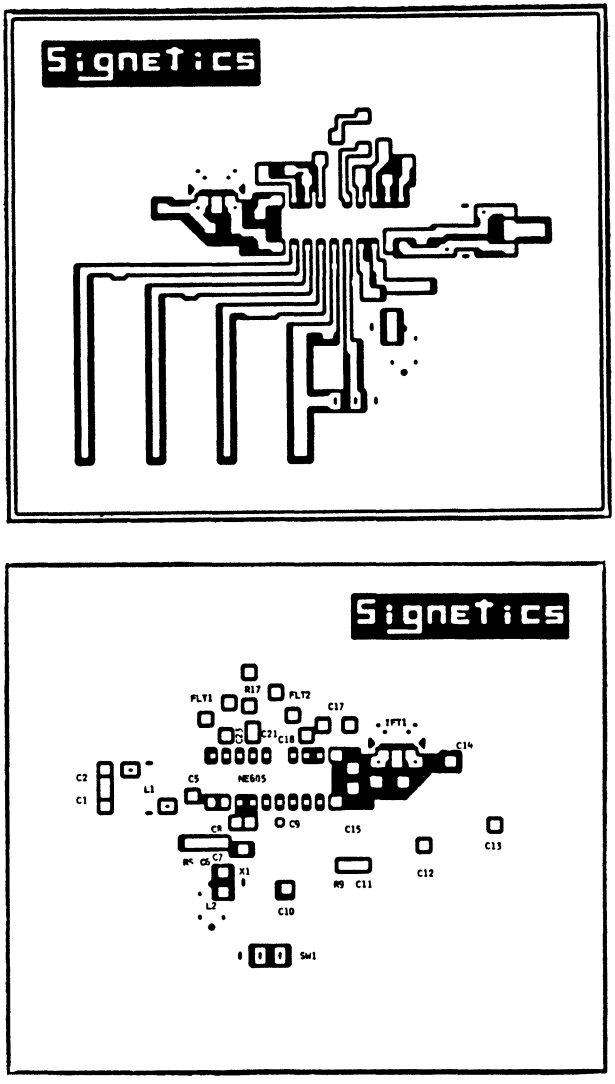


Figure 2. Layout for NE/SA615 Test and Application Board

Signetics

TDA1576
FM-IF (Quadrature Detector)

Product Specification

Linear Products

DESCRIPTION

TDA1576 is an IC which provides all the functions of a comprehensive FM-IF system. The block diagram of the TDA1576 includes a 4-stage FM-IF Amplifier/Limiter with level detector, quadrature FM detector, FM detector, internal regulator, AFC output, and audio meeting circuit. The TDA1576 is ideal for application areas that require low distortion characteristics (THD).

FEATURES

- **Symmetrical limiting IF amplifier**
- **Symmetrical quadrature demodulator**
- **Internal muting circuit**
- **Symmetrical AFC output**
- **Field-strength indication output**
- **Detune-detector**
- **Reference voltage output**
- **Electronic smoothing of the supply voltage**
- **Standby on/off switching circuit**

APPLICATIONS

- **High-fidelity receiver**
- **Communication receiver**
- **Automotive receiver**
- **TVRO**

ORDERING INFORMATION

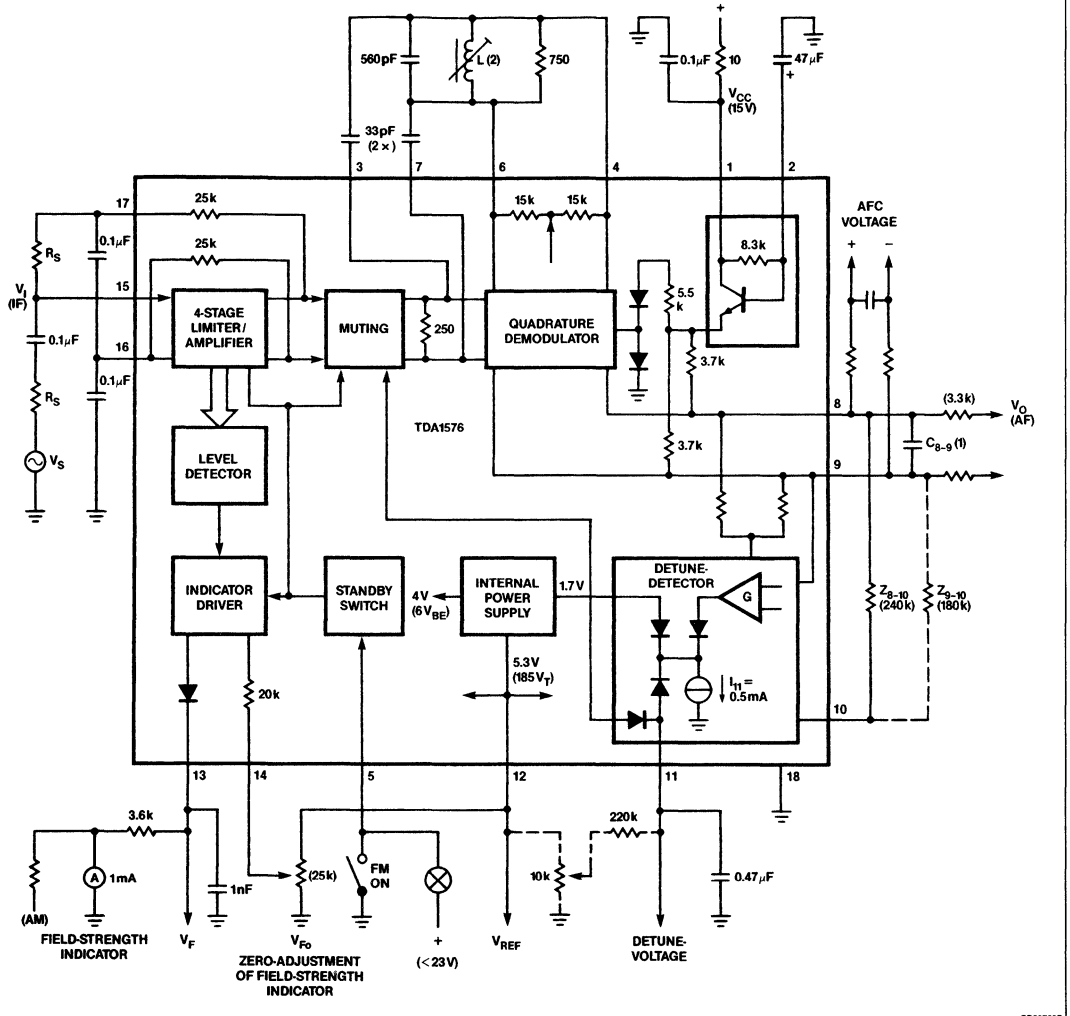
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102C)	−30°C to +80°C	TDA1576N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{1-18}$	Supply voltage (Pin 1)	23	V
	Voltages		
V_{2-18}	at Pin 2	V_{CC}	V
$-V_{2-18}$		0	V
V_{5-18}	at Pin 5	23	V
$-V_{5-18}$		0	V
V_{12-18}	at Pin 12	7	V
$-V_{12-18}$		0	V
V_{13-18}	at Pin 13	6	V
V_{14-18}	at Pin 14	23	V
$-V_{14-18}$		0	V
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C
θ_{CRA}	Thermal resistance from crystal to ambient	80	°C/W

FM-IF (Quadrature Detector) TDA1576

BLOCK DIAGRAM AND TEST CIRCUIT



NOTES:
1 For de-emphasis $\tau = 50\mu s$ $C_{8-9} = 6.8nF$ For stereo operation $C_{8-9} = 56pF$
2 L = 0.38µH, Q_O = 70, Q_L = 20, adjusted to minimum 2nd harmonic distortion (d_2), at V_I = 1mV, coil 6 turns CuL (0.25mm) on coil former KAN (C)

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 8.5V f_O = 10.7MHz, $\Delta f = \pm 22.5$kHz, f_M = 400Hz; $R_S = 60\Omega$; de-emphasis $\tau = 50\mu s$ (C_{8-9} = 6.8nF), T_A = 25°C; measured in the Block Diagram, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion. V_1 = 1mV; $\Delta f = \pm 75$kHz.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range (Pin 1)	7.5		20	V
I_{CC}	Supply current, without load ($I_{12} = I_{13} = 0$)	10	16	23	mA
IF amplifier/detector					
V_I	Sensitivity at -3dB before limiting		22	30	μV
V_I V_I	IF sensitivity for S + N/N = 26dB S + N/N = 46dB		8 35		μV μV
$V_{3-7(P-P)}$	IF output voltage (peak-to-peak value) V_I = 1mV, $Z_{3-18} = Z_{7-18}$		680		mV
R_{3-7}	IF output resistance		250		Ω
R_{4-6} C_{4-6}	Detector input impedance		30 1		kΩ pF
R_8, R_9	Output resistance		3.7		kΩ
$V_{8-18} = V_{9-18}$	DC output voltage		5.5		V
V_O	AF output voltage, Q_L = 20	60	67	75	mV
d_{TOT} d_{TOT}	Total distortion single tuned circuit, Q_L = 20 two tuned circuits		0.1 0.02		% %
S + N/N	Signal pulse noise-to-noise ratio B = 250Hz to 15kHz, V_I > 1mV		76		dB
α	AM rejection, V_I = 10mV FM: f_M = 70Hz, $\Delta f = \pm 22.5$kHz AM: f_M = 1kHz, m = 0.3		54		dB[1]
V_I	IF input voltage range, α > 40dB	0.5		500	mV
α_{100}	Hum suppression at f = 100Hz $V_{CC} = V_{1-18} = 100mV_{RMS}$ $C_{2-18} = 47\mu F$	43	48		dB
$\frac{\Delta V_{8-9}}{\Delta f_O}$	AFC tuning slope at Q_L = 20		8.5		mV/kHz
$\pm \Delta V_{8-9}$ $\pm \Delta V_{8-9}$	AFC offset voltages, Q_L = 20 at V_I = 1mV at V_I = 30μV to 500mV (reference at 1mV and muting)		25	100 50	mV mV
Field-strength indication					
V_I	Indicator sensitivity, I_{14} = 0	20		600	mV
$V_F = V_{13-18}$	Field-strength indicator voltage R_{13-18} = 3.6kΩ, I_{14} = 0, V_I = 0		0	200	mV
$V_F = V_{13-18}$	V_I = 250mV	3.2	3.6	4.1	V
$-I_{13}$	Available output current	2			mA
V_{13-18}	Reverse voltage at the output for FM 'off', V_{5-18} > 3.5V	5			V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 8.5V f_O = 10.7MHz; Δf = ± 22.5kHz; f_M = 400Hz; R_S = 60Ω; de-emphasis τ = 50μs (C_{8-9} = 6.8nF); T_A = 25°C; measured in the Block Diagram, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion: V_1 = 1mV; Δf = ± 75kHz.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Detune-detector					
I_{10}	Quiescent input current; V_{10-9} = 0		20	100	nA
V_{11-18}	Output voltage range	1.8		5.0	V
I_{11}	Available output current	0.35	0.5	0.65	mA
A_V	Voltage gain; $\Delta V_{11}/\Delta(\pm V_{10-9})$ at I_{11} = 0.25mA		3.3		
V_{10-9}	Input offset voltage (Pin 10) at V_{11-18} = 2.5V		20		mV
Reference voltage					
$V_{REF} = V_{12-18}$	Output voltage; $-I_{12}$ = 1mA		5.1		V
$-I_{12}$	Available output current		2.5		mA
Standby switch					
$V_{5\ ON}$ $V_{5\ OFF}$	Required control voltage within the rated ambient temperature and supply voltage ranges for FM 'on' for FM 'off'	 3.5		2	 V V
$-I_5$	Input switching current for FM 'on'			100	μA

NOTE:
1. Simultaneously measured.

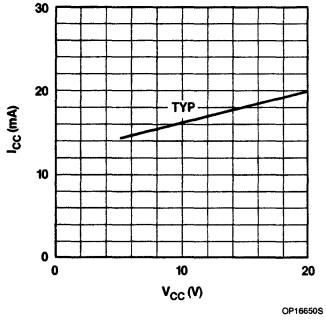
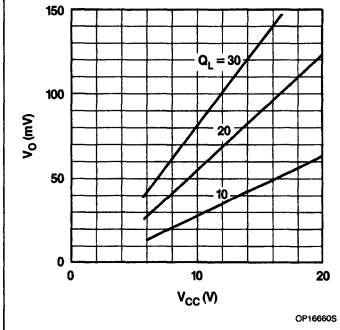
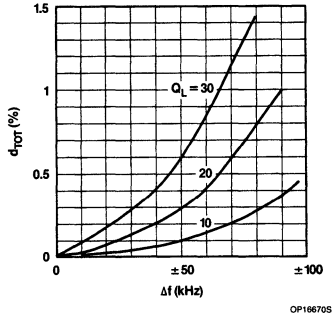


Figure 1. Supply Current Consumption; Without Load



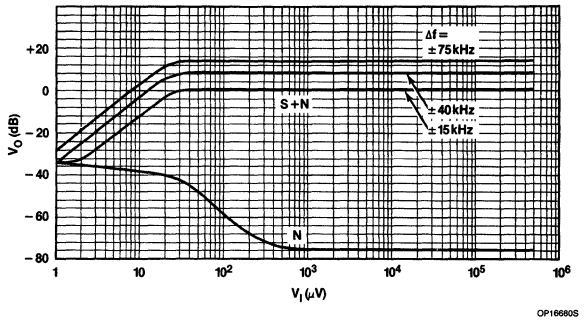
NOTE:
V_{CC} = 1mV(IF), Δf = + 15kHz, f_M = 400Hz, typical values

Figure 2. AF Output Voltage



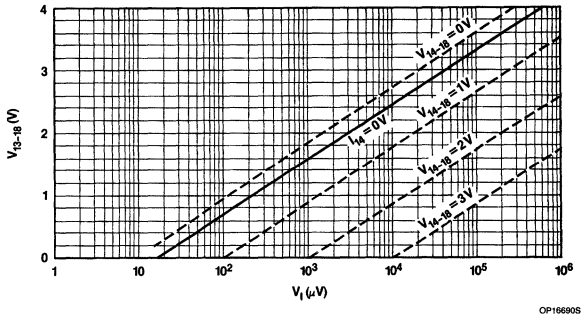
NOTE:
V_I = 1mV (IF), f_M = 400Hz, adjusted at minimum 2nd harmonic distortion, typical values

Figure 3. Total Distortion for Single Tuned Circuit



NOTE:
S = Signal Voltage, N = Noise Voltage, V_{CC} = 15V, f_M = 400Hz, B = 250Hz to 16kHz, Q_L = 20, C_{8-9} = 6 8nF, Typical Values.

Figure 4. AF Output Voltage Level as a Function of IF Input Voltage



NOTE:
R_{13-18} = 3 6kΩ

Figure 5. Voltage at Field-Strength Indicator Output (Proportional to V_{12-18})

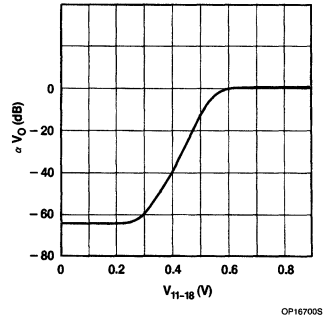


Figure 6. Attenuation of Output Voltage (αV_O) as a Function of the Muting Control Voltage V_{11-18}

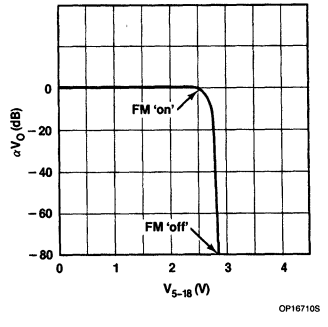
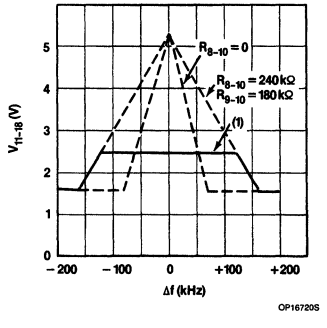
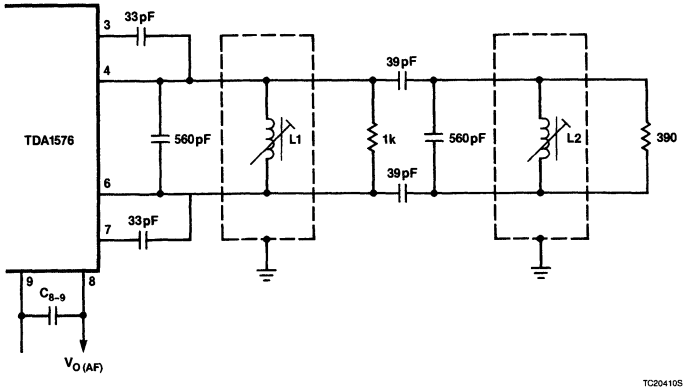


Figure 7. FM 'on'/FM 'off' Standby Switch; Attenuation of Output Voltage (αV_O) as a Function of Control Voltage V_{5-18}



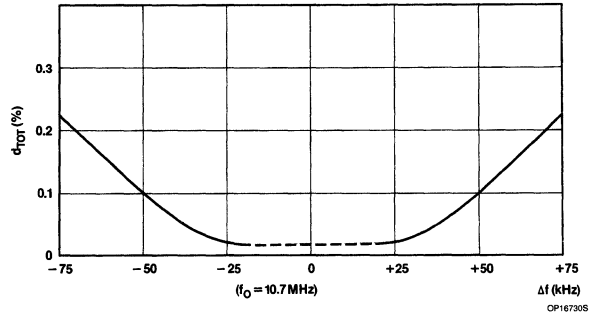
NOTES:
1 Limited by external preset ($\alpha \cdot V_{12-18}$).

Figure 8. Detune-Detector Output Voltage V_{CC} = 7.5 to 20V; Q_L = 20



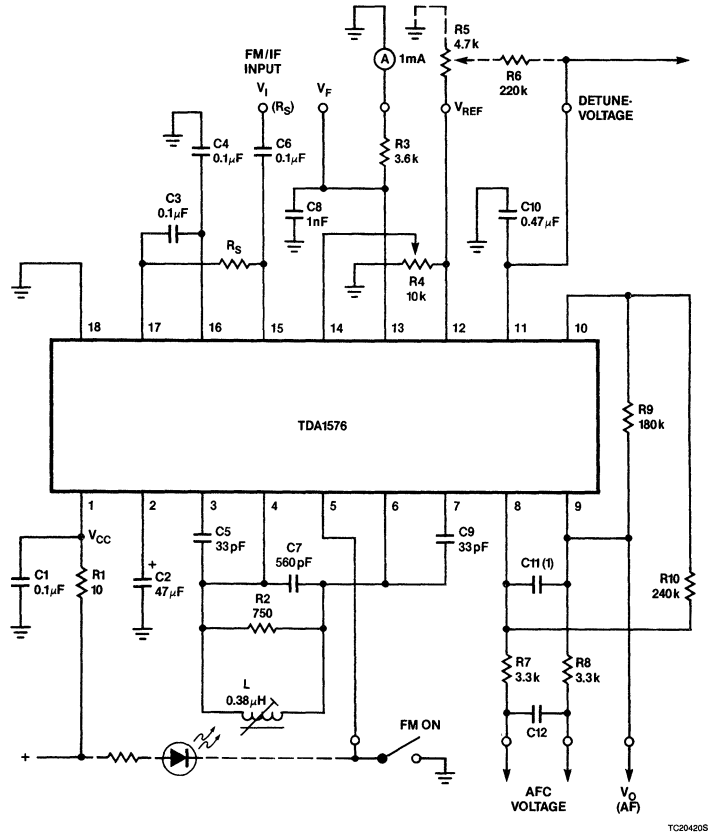
NOTES:
Adjustment of the demodulator circuit is obtained with an IF signal which is higher than the 3dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min d_2 distortion, and then L2 to min d_2 distortion Coil data L1 = L2 = 0 38μH, Q_O = 70, coil former KAN (C)

Figure 9. Example of the TDA1576 When Using a Demodulator With Two Tuned Circuits



NOTES:
f_M = 400Hz, C_{8-9} = 6 8nF, Δf = ± 75kHz, V_O = 330mV for a frequency deviation Δf = ± 75kHz

Figure 10. Total Distortion as a Function of Detuning



NOTES:
1 For mono C11 = 6 8nF, for stereo C11 = 56pF

Figure 11. Application Example of Using TDA1576

HEF4750V
Frequency Synthesizer

Product Specification

Linear Products

DESCRIPTION

The HEF4750V frequency synthesizer is one of a pair of LOCMOS devices, primarily intended for use in high-performance frequency synthesizers; e.g., in all communication, instrumentation, television and broadcast applications. A combination of analog and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOCMOS integrated circuits offer low-cost single-loop synthesizers with full professional performance.

FEATURES

- **Wide choice of reference frequency using a single crystal**
- **High-performance phase comparator — low phase —low noise spurii**
- **System operation to > 1GHz**
- **Typical 15MHz input at 10V**
- **Flexible programming:**
  - **frequency offsets**
  - **ROM compatible**
  - **fractional channel capability**
- **Program range 6½ decades, including up to 3 decades of prescaler control**
- **Division range extension by cascading**
- **Built-in phase modulator**
- **Fast lock feature**
- **Out-of-lock indication**
- **Low power dissipation and high noise immunity**

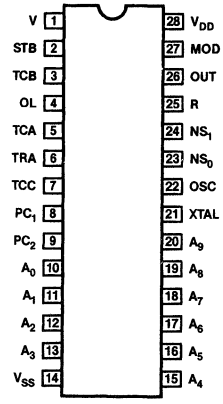
APPLICATIONS

Some examples of applications for the HEF4750V in combination with the HEF4751V are:

- **VHF/UHF mobile radios**
- **HF SSB transceivers**
- **Airborne and marine communications and navaids**
- **Broadcast transmitters**
- **High quality radio and television receivers**
- **High-performance citizens band equipment**
- **Signal generators**

PIN CONFIGURATION

F Package



TOP VIEW

CD11210S

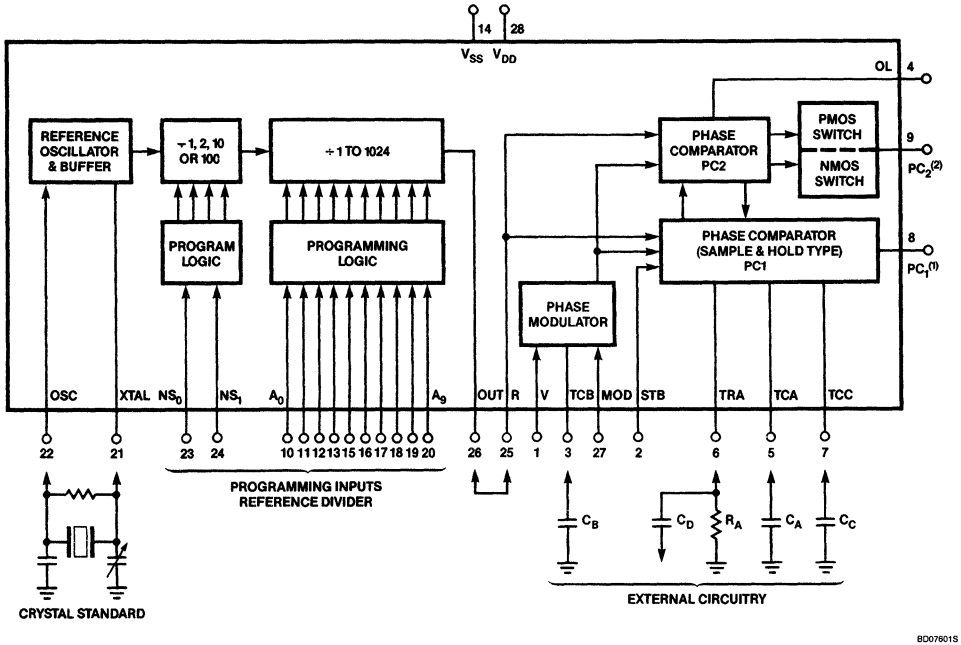
PIN NO.	SYMBOL	DESCRIPTION
1	V	Phase comparator input
2	STB	Strobe input
3	TCB	Timing capacitor C_B pin
4	OL	Out-of-lock indication
5	TCA	Timing capacitor C_A pin
6	TRA	Biasing pin (resistor R_A)
7	TCC	Timing capacitor C_C pin
8	PC_1	Analog phase comparator output
9	PC_2	Digital phase comparator output
10	A_0	Programming inputs/programmable divider
11	A_1	Programming inputs/programmable divider
12	A_2	Programming inputs/programmable divider
13	A_3	Programming inputs/programmable divider
14	V_{SS}	
15	A_4	Programming inputs/programmable divider
16	A_5	Programming inputs/programmable divider
17	A_6	Programming inputs/programmable divider
18	A_7	Programming inputs/programmable divider
19	A_8	Programming inputs/programmable divider
20	A_9	Programming inputs/programmable divider
21	XTAL	Reference oscillator/buffer output
22	OSC	Reference oscillator/buffer input
23	NS_0	Programming inputs, prescaler
24	NS_1	Programming inputs, prescaler
25	R	Phase comparator input, reference
26	OUT	Reference divider output
27	MOD	Phase modulation input

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Cerdip	−40°C to +85°C	HEF4750VDF
28-Pin Cerdip	−55°C to +125°C	HEC4750VDF

Frequency Synthesizer | HEF4750V

BLOCK DIAGRAM



NOTES:
1 PC_1 = analog output
2 PC_2 = 3-state output

Block Diagram Comprising Five Basic Functions: Phase Comparator 1 (PC_1), Phase Comparator 2 (PC_2), Phase Modulator, Reference Oscillator and Reference Divider (These Functions are Described Separately)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	−0.5 to +15	V
V_I	Voltage on any input	−0.5 to V_{DD} +0.5	V
±I	DC current into any input or output	10	mA
P_D	Power dissipation per package for T_A = 0 to +85°C	500	mW
P_D	Power dissipation per output for T_A = 0 to +85°C	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature HEF4750V HEC4750V	 −40 to +85 −55 to +125	 °C °C

DC ELECTRICAL CHARACTERISTICS

HEF4750V, HEC4750V V_{DD} = 10V ± 5%; voltages are referenced to V_{SS} = 0V, unless otherwise specified. For definitions see Note 1.

SYMBOL	PARAMETER	LIMITS									UNIT
		T_A = −40°C			T_A = +25°C			T_A = +85°C			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{DD}	Quiescent device current[2]			100			100			750	μA
$\pm I_{IN}$	Input current; logic inputs, MOD[3]			300			300			1000	nA
	Output leakage current at ½ V_{DD}[3, 4]										
$\pm I_Z$	TCA, hold-state			20		0.05	20			60	nA
	TCC, analog										
$\pm I_Z$	switch OFF			20		0.05	20			60	nA
	PC_2, high impedance										
$\pm I_Z$	OFF-state			50			50			500	nA
	Logic input voltage										
V_{IL}	LOW			$0.3V_{DD}$			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{IH}	HIGH	$0.7V_{DD}$			$0.7V_{DD}$			$0.7V_{DD}$			V
	Logic output voltage[3]										
V_{OL}	LOW; at $\|I_O\| < 1\mu A$			50			50			50	mV
V_{OH}	HIGH	$V_{DD}-50mV$			$V_{DD}-50mV$			$V_{DD}-50mV$			mV
	Logic output current LOW; at V_{OL} = 0.5V[3]										
I_{OL}	outputs OL, PC_2, OUT	5.5			4.6			3.6			mA
I_{OL}	output XTAL	2.8			2.4			1.9			mA
	Logic output current HIGH; at $V_{OH} = V_{DD} - 0.5V$[3]										
$-I_{OH}$	outputs OL, PC_2, OUT	1.5			1.3			1.0			mA
$-I_{OH}$	output XTAL	1.4			1.2			0.9			mA
I_O	Output TCC sink current[3, 4, 5]					2.1					mA
$-I_O$	Output TCC source current[3, 4, 6]					1.9					mA
R_I	Internal resistance of TCC |output swing| ⩽ 200mV specified output range: 0.3 V_{DD} to 0.7 V_{DD}[3, 4]					0.7					kΩ
ΔV	Output TCC voltage with respect to TCA input voltage[3, 4, 7]		0			0			0		V
I_O	Output PC_1 sink current[3, 4, 9]					1.1					mA
$-I_O$	Output PC_1 source current[3, 4, 9]					1.0					mA
R_I	Internal resistance of PC_1 |output swing| ⩽ 200mV specified output range: 0.3 V_{DD} to 0.7 V_{DD}[3, 4]					1.4					kΩ

DC ELECTRICAL CHARACTERISTICS (Continued)

HEF4750V, HEC4750V V_{DD} = 10V ± 5%; voltages are referenced to V_{SS} = 0V, unless otherwise specified. For definitions see Note 1.

SYMBOL	PARAMETER	LIMITS									UNIT
		T_A = −40°C			T_A = +25°C			T_A = +85°C			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ΔV	Output PC_1 voltage with respect to TCC input voltage[3, 4, 10]		0			0			0		V
V_{EOR}	EOR generation $V_{EOR} = V_{DD} - V_{TCA}$[3, 4, 8, 11]		0.9			0.7			0.6		V
	Source current; HIGH at $V_{OUT} = \frac{1}{2} V_{DD}$; output in ramp mode[3, 4]										
I_O	TCA					13					mA
I_O	TCB					2.5					mA

AC ELECTRICAL CHARACTERISTICS

General Note

The dynamic specifications are given for the circuit built-up with external components as given in Figure 6, under the following conditions; for definitions see Note 1; for definitions of times see Figure 17; V_{DD} = 10V ± 5%; T_A = 25°C; input transition times ⩽ 20ns; R_A = 68kΩ ± 30% (see also Note 4); C_A = 270pF; C_B = 150pF; C_C = 1nF; C_D = 10nF; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Slew rate [11]					
S_{TCA}	TCA	R_A = minimum		52		V/μs
S_{TCA}	TCA	R_A = maximum		28		V/μs
S_{TCB}	TCB	R_A = minimum		20		V/μs
S_{TCB}	TCB	R_A = maximum		10		V/μs
	Ramp linearity[13]					
l_{TCA}	TCA			2		%
l_{TCB}	TCB			2		%
t_{CBCA}	Start of TCA ramp delay			200		ns
t_{RCA}	Delay of TCA hold			40		ns
t_{VCA}	Delay of TCA discharge			60		ns
t_{VCB}	Start of TCB ramp delay			60		ns
t_{rCB}	TCB ramp duration	V_{MOD} = 4V		250		ns
		V_{MOD} = 6V		350		ns
		V_{MOD} = 8V		450		ns
t_{rCB}	Required TCB min. ramp duration[14]			150		ns
	Pulse width					
t_{PWVL}	V: LOW			20		ns
t_{PWVH}	V: HIGH			20		ns
t_{PWRL}	R: LOW			20		ns
t_{PWRH}	R: HIGH			20		ns
t_{PWSL}	STB: LOW			20		ns
t_{PWSH}	STB: HIGH			20		ns
	Fall time					
t_{fCA}	TCA			50		ns
t_{fCB}	TCB			50		ns

AC ELECTRICAL CHARACTERISTICS (Contined)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{PR}	Prescaler input frequency	All division ratios		30		MHz
f_{DIV}	Binary divider frequency	All division ratios		30		MHz
f_{OSC}	Crystal oscillator frequency			10		MHz
	Average power supply current	Locked state				
I_{CC}	with speed-up 1.10[15]			3.6		mA
I_{CC}	without speed-up[16]			3.2		mA

NOTES:

1. Definitions.
   R_A = external biasing resistor between pins TRA and V_{SS} , 68 kΩ± 30%
   C_A = external timing capacitor for time/voltage converter, between pins TCA and V_{SS}
   C_B = external timing capacitor for phase modulator, between pins TCB and V_{SS}
   C_C = external hold capacitor between pins TCC and V_{SS}
   C_D = decoupling capacitor between pins TRA and V_{DD}
   Logic inputs. V, R, STB, A_0 to A_9, NS_0, NS_1, OSC
   Logic outputs· OL, PC_2, XTAL, OUT
   Analog signals: TCA, TCB, TCC and MOD
2. TRA at V_{DD}, TCA, TCB, TCC and MOD at V_{SS}, logic inputs at V_{SS} or V_{DD}
3. All logic inputs at V_{SS} or V_{DD}
4. R_A connected; its value chosen such that $I_{TRA} = 100\mu A$
5. The analog switch is in the ON position (see Figure 1)

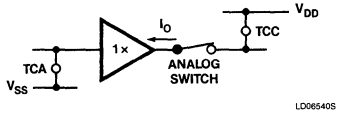


Figure 1. Equivalent Cicuit for Note 5

6. The analog switch is in the ON position (see Figure 2)

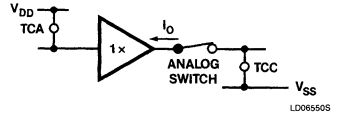


Figure 2. Equivalent Circuit for Note 6

7. This guarantees the DC voltage gain, combined with DC offset Input condition $0.3V_{DD} \leq V_{TCA} \leq 0.7V_{DD}$ $\Delta V = V_{TCC} - V_{TCA}$

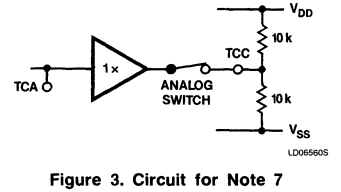


Figure 3. Circuit for Note 7

8. See Figure 4.

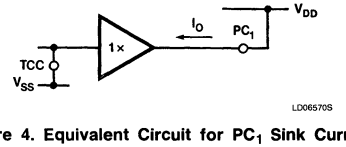


Figure 4. Equivalent Circuit for PC_1 Sink Current

9. See Figure 5.

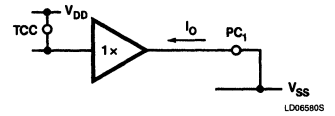


Figure 5. Equivalent Circuit for PC_1 Source Circuit

10. This guarantees the DC voltage gain, combined with DC offset.
Input condition. 0.3 $V_{DD} \leqslant V_{TCC} \leqslant 0.7V_{DD}$.
$\Delta V = V_{PC1} - V_{TCC}$.

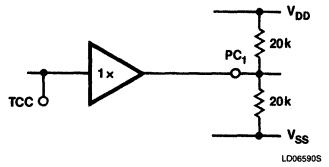


Figure 6. Circuit for Note 10

11. Switching level at TCA, generating an Ex-OR signal, during increasing input voltage
12. See Figure 7.

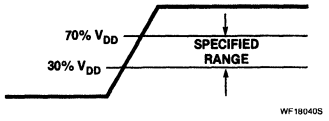
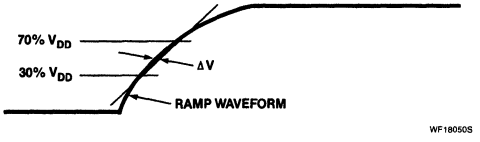


Figure 7. Waveform at the Output

13. Definition of the ramp linearity at full swing See Figure 8.



NOTE:

Linearity = $\frac{\Delta V}{\frac{1}{2} V_{DD}} \times 100\%$

Figure 8. ΔV is the Maximum Deviation of the Ramp Waveform to the Straight Line, Which Joins the 30% V_{DD} and 70% V_{DD} Points

14. The external components and modulation input voltage must be chosen such that this requirement will be fulfilled, to ensure that C_A is sufficiently discharged during that time.

15. Circuit connections for power supply current specification, with speed-up 1:10. V and R are in the range of PC_1, such that the output voltage at PC_1 is equal to 5V
f_{OSC} = 5MHz (external clock)
f_{STB} = 12.5kHz
f_V = 125kHz

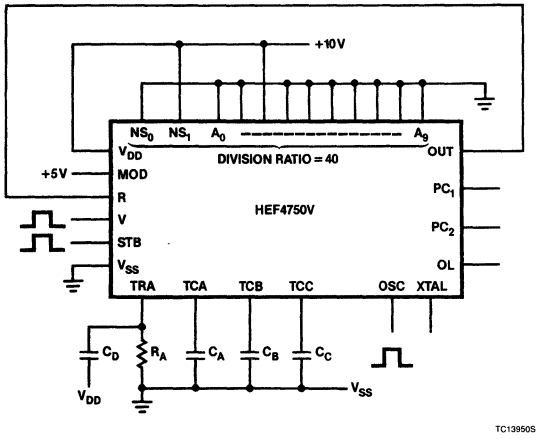


Figure 9. Circuit for Note 15

16. Circuit connections for power supply current specification, without speed-up. V and R are in the range of PC_1, such that the output voltage at PC_1 is equal to 5V.
f_{OSC} = 5MHz (external clock)
f_{STB} = 12.5kHz
f_V = 12.5kHz

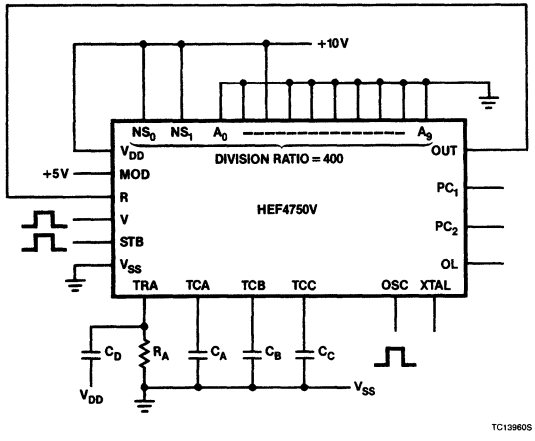


Figure 10. Circuit for Note 16

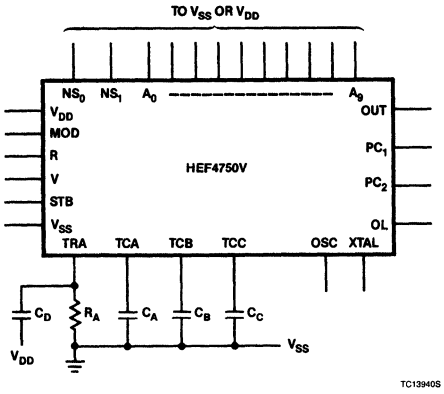


Figure 11. Test Circuit for Measuring AC Characteristics

FUNCTIONAL DESCRIPTION

Phase Comparator 1

Phase comparator 1 (PC_1) is built around a SAMPLE and HOLD circuit. A negative-going transition at the V input causes the hold capacitor (C_A) to be discharged and, after a specified delay, caused by the Phase Modulator by means of an internal V' pulse, it produces a positive-going ramp. A negative-going transition at the R input terminates the ramp. Capacitor C_A holds the voltage that the ramp has attained. Via an internal sampling switch this voltage is transferred to C_C and in turn buffered and made available at output PC_1.

If the ramp terminates before an R input is present, an internal end of ramp (EOR) signal is produced. These actions are illustrated in Figure 12.

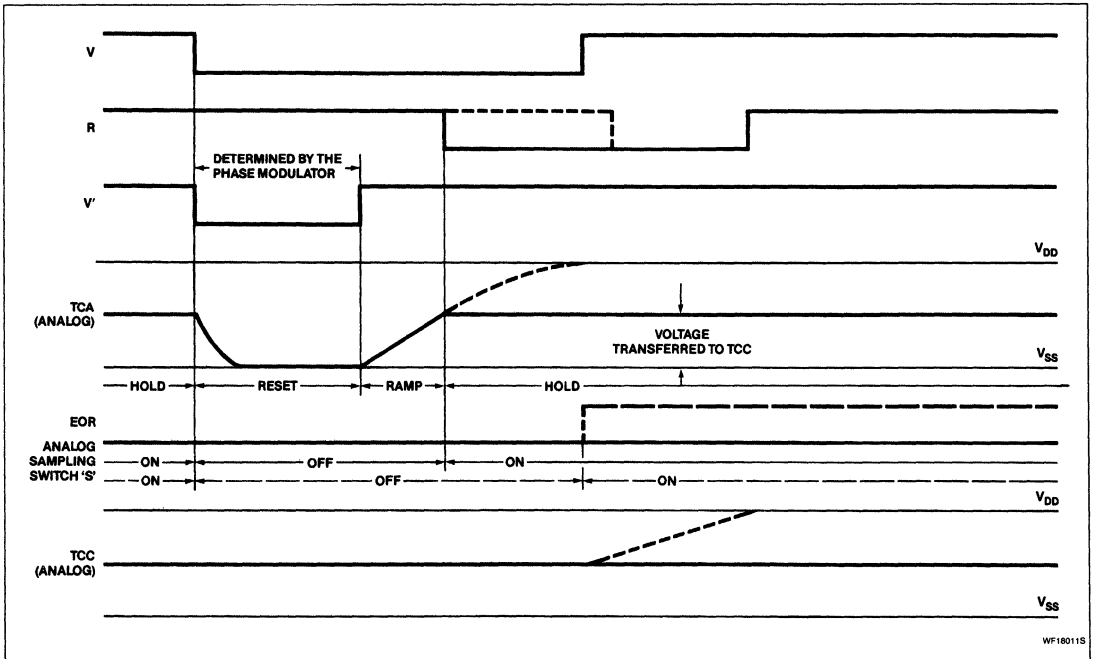


Figure 12. Waveforms Associated With PC_1

The result phase characteristic is shown in Figure 13 PC_1 is designed to have a high gain, typically 3200 V/cycle (at 12 5kHz) This enables a low noise performance.

Phase Comparator 2

Phase comparator 2 (PC_2) has a wide range, which enables faster lock times to be achieved than otherwise would be possible It has a linear ±360°C phase range, which corresponds to a gain of typically 5V/cycle. This digital phase comparator has three stable states

- Reset state
- V' leads R state
- R leads V' state

Conversion from one state to another takes place according to the state diagram of Figure 14

Output produces positive or negative-going pulses with variable width; they depend on the phase relationship of R and V'. The average output voltage is a linear function of the phase difference Output PC_2 remains in the high-impedance OFF state in the region in which PC_1 operates. The resultant phase characteristic is shown in Figure 15.

Strobe Function

The strobe function is intended for applications requiring extremely fast lock times. In normal operation the additional strobe input (STB) can be connected to the V input and the circuit will function as described in the previous sections.

In single, phase-locked loop type frequency synthesizers, the comparison frequency generally used is either the nominal channel spacing or a sub-multiple, PC_2 runs at the higher frequency (a higher reference frequency must also be used), while strobing takes place on the lower frequency, thereby obtaining a decrease in lock time In a system using the Universal Divider HEF4751V, the output OFS cycles on the lower frequency, the output OFF cycles on the higher frequency

Out-of-Lock Function

There are a number of situations in which the system goes from the locked to the out-of-lock state (OL goes HIGH)

1. When V' leads R, however out of the range of PC_1.

2 When R leads V'.

3 When an R pulse is missing.

4 When a V pulse is missing

5 When two successive STB commands occur, the first without corresponding V signal.

Phase Modulator

The phase modulator only uses one external capacitor, C_B at pin TCB A negative-going transition at the V input causes C_B to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage (at MOD), the ramp terminates, C_B discharges and a start signal to the C_A ramp at TCA is produced. A linear phase modulation is reached in this way. If no modulation is required, the MOD input must be connected to a fixed voltage of a certain positive value up to V_{DD}. Care must be taken that the V' pulse is never smaller than the minimum value to ensure that the external capacitor of $PC_1(C_A)$ can be discharged during that time Since the V' pulse width is directly related to the TCB ramp duration, there is a requirement for the minimum value of this ramp duration.

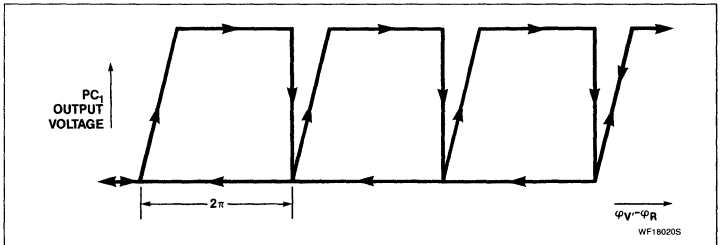


Figure 13. Phase Characteristic of PC_1

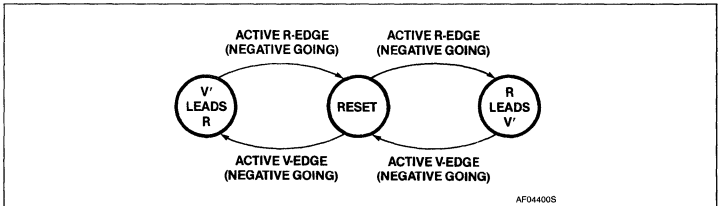


Figure 14. State Diagram of PC_2

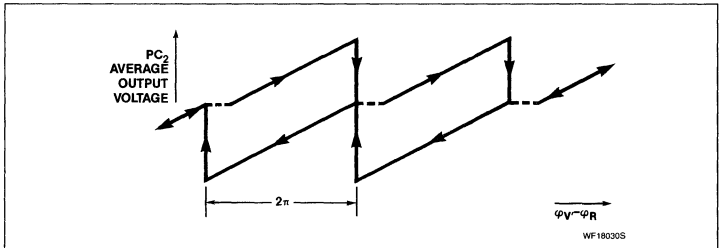


Figure 15. Phase Characteristics of PC_2

Reference Oscillator

The reference oscillator normally operates with an external crystal as shown in the block diagram. The internal circuitry can be used as a buffer amplifier in case an external reference should be required

Reference Divider

The reference divider consists of a binary divider with a programmable division ratio of 1-to-1024 and a prescaler with selectable division ratios of 1, 2, 10 and 100, according to the following tables:

Binary divider

N (A_0 TO A_9)	DIVISION RATIO
0	1024
$0 \leqslant N \leqslant 1023$	N

Prescaler

PROGRAMMING WORD (NS_0, NS_1)	DIVISION RATIO
0	1
1	2
2	10
3	100

In this way, suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a 'stand-alone' programmable divider by connecting input TRA to V_{DD}, which causes all internal analog currents to be switched off.

Biasing Circuitry

The biasing circuitry uses an external current source or resistor, which has to be connected between the TRA and V_{SS} pins. This circuitry supplies all analog parts of the circuit. Consequently the analog properties of the device, such as gain, charge currents, speed, power dissipation, impedance levels, etc., are mainly determined by the value of the input current at TRA. The TRA input must be decoupled to V_{DD}, as shown in Figure 16. The value of C_D has to be chosen such that the TRA input is 'clean', e.g., 10nF at $R_A = 68k\Omega$.

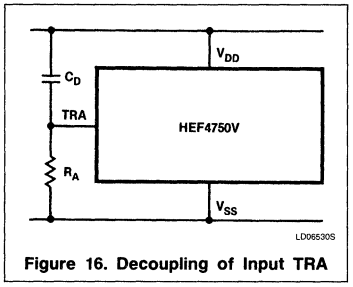
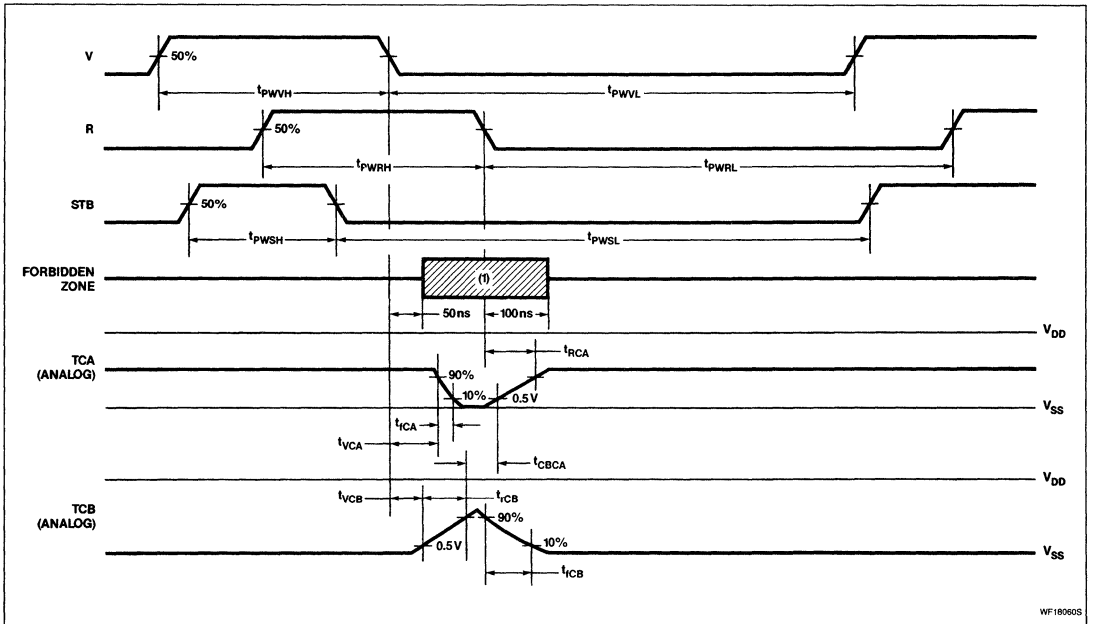


Figure 16. Decoupling of Input TRA



NOTE:
1 Forbidden zone in the locked state for the positive edge of V and R and both edges of STB

Figure 17. Waveforms Showing Times in the Locked State

Signetics

HEF4751V
Universal Divider

Product Specification

Linear Products

DESCRIPTION

The HEF4751V is a universal divider (UD) intended for use in high-performance phase-locked loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) ÷ 10/11 prescalers.

The system comprising one HEF4751V UD together with prescalers is a fully-programmable divider with a maximum configuration of 5 decimal stages, a programmable mode M stage ($1 \leqslant M \leqslant 16$, non-decimal fraction channel selection), and a mode H stage (H = 1 or 2, stage for half-channel offset). Programming is performed in BCD code in a bit-parallel, digit-serial format. To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal program. The decade selection address is generated by an internal program counter which may run continuously or on demand. Two or more universal dividers can be cascaded. Each extra UD (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single UD. The UD provides a fast output signal flip-flop at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

FEATURES

(in combination with HEF4750V) are:

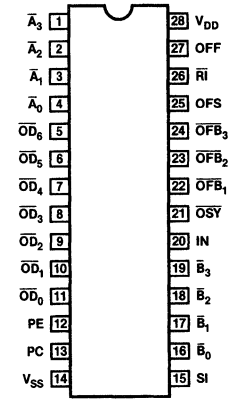
- **Wide choice of reference frequency using a single crystal**
- **High-performance phase comparator — low phase noise — low spurii**
- **System operation to > 1GHz**
- **Typical 15MHz input at 10V**
- **Flexible programming:**
  - **frequency offsets**
  - **ROM compatible**
  - **fractional channel capability**
- **Program range 6.5 decades, including up to 3 decades of prescaler control**
- **Division range extension by cascading**
- **Built-in phase modulator**
- **Fast lock feature**
- **Out-of-lock indication**
- **Low power dissipation and high noise immunity**

APPLICATIONS

- **VHF/UHF mobile radios**
- **HF SSB transceivers**
- **Airborne and marine communications and navigations**
- **Broadcast transmitters**
- **High quality radio and television receivers**
- **Signal generators**

PIN CONFIGURATION

F,N Packages



TOP VIEW

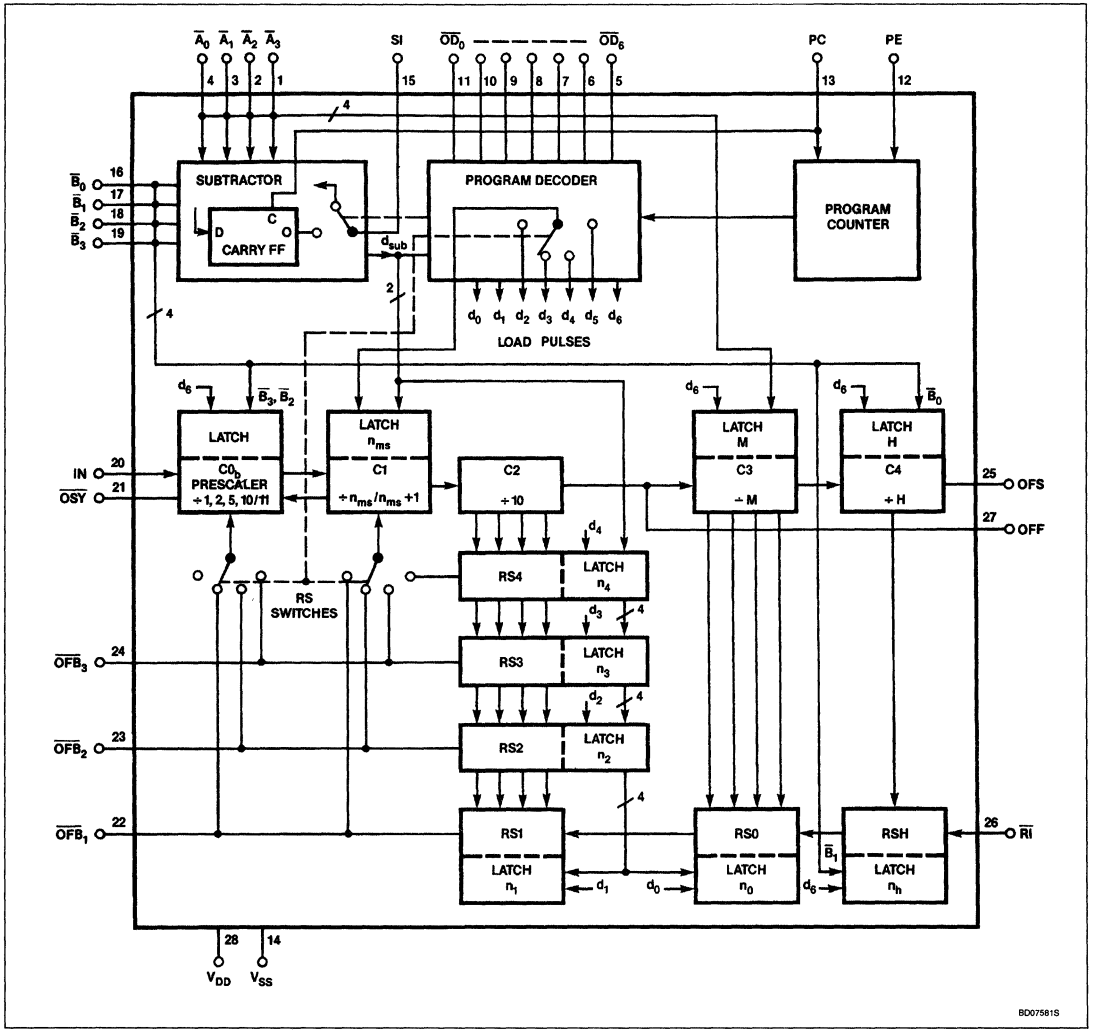
CD11200S

PIN NO.	SYMBOL	DESCRIPTION
1	$\overline{A}_3$	Data inputs
2	$\overline{A}_2$	
3	$\overline{A}_1$	
4	$\overline{A}_0$	
5	$\overline{OD}_6$	Data address outputs
6	$\overline{OD}_5$	
7	$\overline{OD}_4$	
8	$\overline{OD}_3$	
9	$\overline{OD}_2$	
10	$\overline{OD}_1$	
11	$\overline{OD}_0$	
12	PE	Program enable
13	PC	Program clock
14	V_{SS}	
15	SI	Borrow input
16	$\overline{B}_0$	Data inputs
17	$\overline{B}_1$	
18	$\overline{B}_2$	
19	$\overline{B}_3$	
20	IN	Input
21	$\overline{OSY}$	Sync output
22	$\overline{OFB}_1$	Prescaler control outputs
23	$\overline{OFB}_2$	
24	$\overline{OFB}_3$	
25	OFS	Output signal (slow)
26	$\overline{RI}$	Rate input
27	OFF	Output signal (FAST)
28	V_{DD}	

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−40°C to +85°C	HEF4751VPN
28-Pin Cerdip (SOT-135A)	−55°C to +125°C	HEC4751VDBF

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	−0.5 to +15	V
V_I	Voltage on any input	−0 5 to V_{DD} +0.5	V
±I	DC current into any input or output	10	mA
P_{TOT}	Total power dissipation per package for T_A = 0 to +85°C	500	mW
P_D	Power dissipation per output for T_A = 0 to +85°C	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

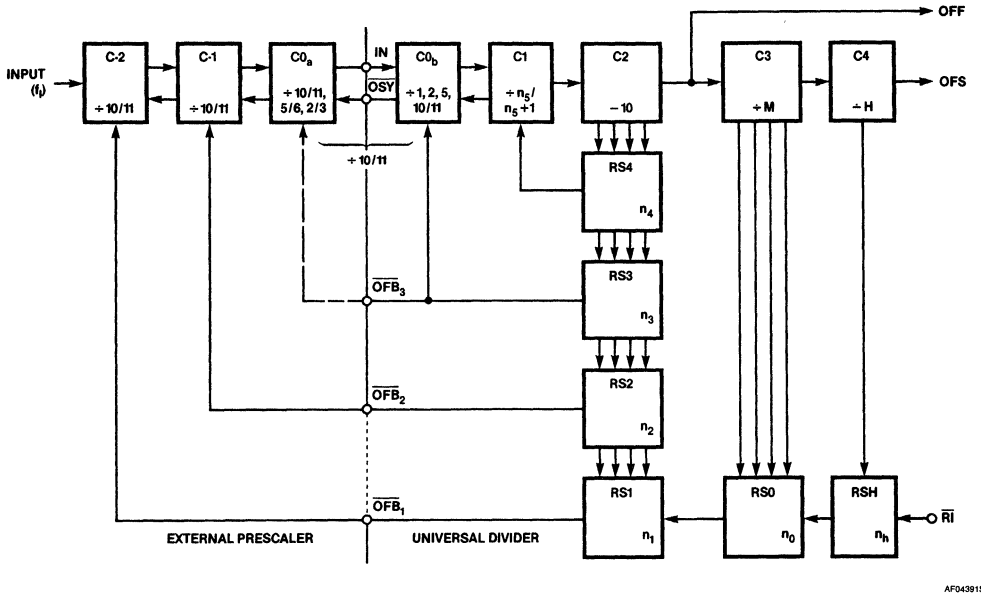
DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V

SYMBOL	PARAMETER	V_{DD} (V)	V_{OH} (V)	V_{OL} (V)	LIMITS						UNIT
					T_A = −40°C		T_A = +25°C		T_A = +85°C		
					Min	Max	Min	Max	Min	Max	
I_{OL}	Output (sink) current LOW	4.75		0.4	1.6		1.4		1.1		mA
		5		0.4	1.7		1.5		1.2		mA
		10		0 5	2.9		2.7		2.2		mA
$-I_{OH}$	Output (source) current HIGH	5	4.6		1.0		0 85		0 55		mA
		5	2.5		3 0		2.5		1.7		mA
		10	9.5		3 0		2.5		1.7		mA

AC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_A = 25°C; input transition times ⩽ 20ns.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{DD} (V)	LIMITS			UNIT
				Min	Typ	Max	
t_{PHL}	Propagation delay IN → $\overline{OSY}$ HIGH-to-LOW	C_L = 10pF	5		135	270	ns
			10		45	90	ns
	Output transition times						
t_{THL}	HIGH-to-LOW	C_L = 50pF	5		30	60	ns
			10		12	25	ns
t_{TLH}	LOW-to-HIGH	C_L = 50pF	5		45	90	ns
			10		20	40	ns
f_{MAX}	Maximum input frequency; IN	δ = 50% ; CO_b ratio > 1	5	4	8		MHz
			10	12	24		MHz
f_{MAX}	Maximum input frequency, IN	δ = 50% ; CO_b ratio = 1	5	2	4		MHz
			10	6	12		MHz
f_{MAX}	Maximum input frequency; PC		5	0.15	0.3		MHz
			10	0.5	1.0		MHz
Typical Formula for P (μW)							
P_D	Dynamic power dissipation per package (P)[1]	5V	1 200 $f_I + \Sigma(f_O C_L) \times V_{DD}^2$				
		10V	5 400 $f_I + \Sigma(f_O C_L) \times V_{DD}^2$				

NOTE:
f_I = input frequency (MHz)
f_O = output frequency (MHz)
C_L = load capacitance (pF)
$\Sigma(f_O C_L)$ = sum of outputs
V_{DD} = supply voltage (V)



NOTES:
$1 \leqslant M \leqslant 16$; $1 \leqslant H \leqslant 2$, $n_5 > 0$, $f_i/f_{OFS} = \{(n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1)\ M + n_0\}\ H + n_h$

Figure 1. The HEF4751V UD Used in a System With 3 (Fast) Prescalers

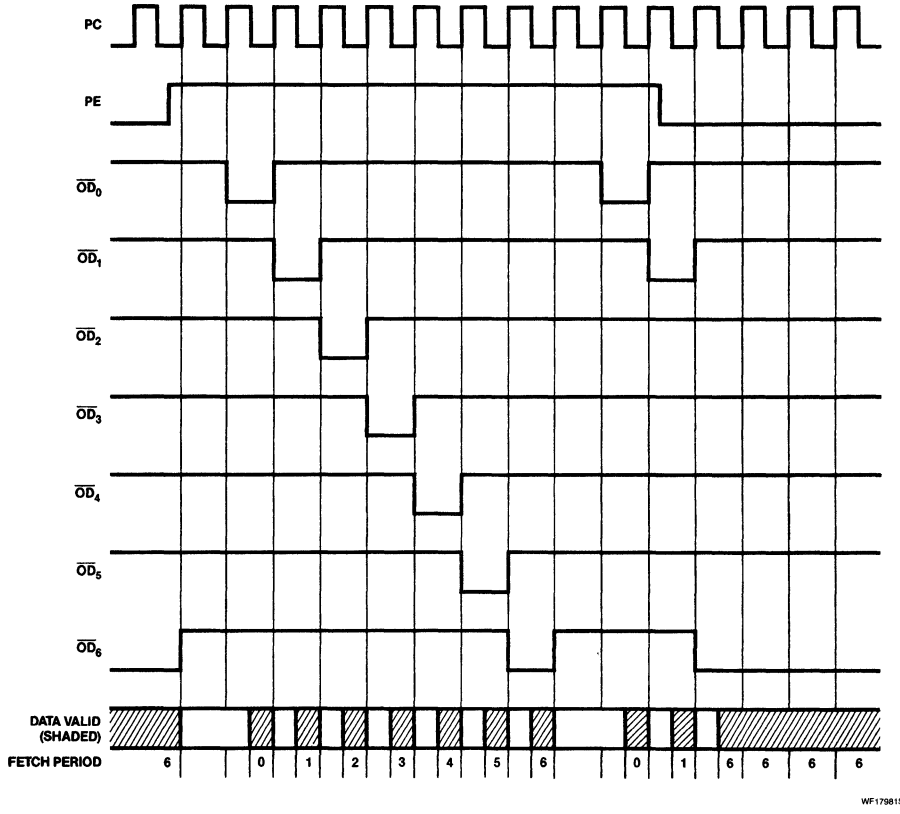


Figure 2. Timing Diagram Showing Program Data Inputs

Allocation of Data Input

FETCH PERIOD	INPUTS								
	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	$\overline{A}_0$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$	S1
0	n_{0A}				n_{0B}				b_{in}
1	n_{1A}				n_{1B}				X
2	n_{2A}				n_{2B}				X
3	n_{3A}				n_{3B}				X
4	n_{4A}				n_{4B}				X
5	n_{5A}				n_{5B}				X
6	M				$C0_b$ control		½ channel control		X

Allocation of Data Input $\overline{B}_3$ to $\overline{B}_0$ During Fetch Period 6

$\overline{B}_3$	$\overline{B}_2$	CO_b DIVISION RATIO
L	L	1
L	H	2
H	L	5
H	H	10/11

$\overline{B}_1$	$\overline{B}_0$	½ CHANNEL CONFIGURATION
L	L	H = 1
L	H	H = 2, $n_h = 0$
H	H	H = 2; $n_h = 1$
H	L	test state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

PROGRAM DATA INPUT (see also Figures 1 and 2)

The programming process is timed and controlled by input PC and PE When the program enable (PE) input is HIGH, the positive edges of the program clock (PC) signal step through the internal program counter in a sequence of 8 states. Seven states define fetch periods, each indicated by a LOW signal at one of the corresponding data address outputs ($\overline{OD}_0$ to $\overline{OD}_6$) These data address signals may be used to address the external program source The data fetched from the program source is applied to inputs $\overline{A}_0$ to $\overline{A}_3$ and $\overline{B}_0$ to $\overline{B}_3$ When PC is LOW in a fetch period, an internal load pulse is generated. The data is valid during this time and has to be stable When PE is LOW, the programming cycle is interrupted on the first positive edge of PC. On the next negative edge at input PC, fetch period 6 is entered. Data may enter asynchronously in fetch period 6.

Ten blocks in the UD need program input signals (see Block Diagram). Four of these ($C0_b$, C3, C4 and RSH) are concerned with the configuration of the UD and are programmed in fetch period 6. The remaining blocks (RS0 to RS4 and C1) are programmed with number P, consisting of six internal digits n_0 to n_5.

$$P = (n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) \cdot M + n_0$$

These digits are formed by a substractor from two external numbers A and B and a borrow-in (b_{in})

$P = A - B - b_{in}$ or if this result is negative; $P = A - B - b_{in} + M \cdot 10^5$.

The numbers A and B, each consisting of six four bit digits n_A to n_{5A} and n_{0B} to n_{5B}, are applied in fetch period 0 to 5 to the inputs $\overline{A}_0$ to $\overline{A}_3$ (data A) and $\overline{B}_0$ to $\overline{B}_3$ (data B) in binary coded negative logic.

$$A = (n_{5A} \cdot 10^4 + n_{4A} \cdot 10^3 + n_{3A} \cdot 10^2 + n_{2A} \cdot 10 + n_{1A}) \cdot M + n_{0A}$$

$$B = (n_{5B} \cdot 10^4 + n_{4B} \cdot 10^3 + n_{3B} \cdot 10^2 + n_{2B} \cdot 10 + n_{1B}) \cdot M + n_{0B}$$

Borrow-in (b_{in}) is applied via input SI in fetch period 0 (SI = HIGH borrow; SL = LOW· no borrow).

Counter C1 is automatically programmed with the most significant non-zero digit (n_{ms}) from the internal digits n_5 to n_2 of number P The counter chain C – 2 to C1 (Figure 1) is fully programmable by the use of pulse rate feedback.

Rate feedback is generated by the rate selectors RS4 to RS0 and RSH, which are programmed with digits n_4 to n_0 and n_h, respectively In fetch period 6 the fractional counter C3, half-channel counter C4 and $C0_b$ are programmed and configured via data B inputs. Counter C3 is programmed in fetch period 6 via data A inputs in negative logic (except all HIGH is understood as: M = 16). The counter C0 is a side steppable 10/11 counter composed of an internal part $C0_b$ and an external part $C0_a$. $C0_b$ is configured via $\overline{B}_3$ and $\overline{B}_2$ to a division ratio of 1 or 2 or 10/11; $C0_a$ must have the complementary ratio 10/11 or 5/6 or 2/3 or 1, respectively. In the latter case, $C0_b$ comprises the whole C0 counter with internal feedback. $C0_a$ is then not required.

The half channel counter C4 is enabled with $\overline{B}_0$ = HIGH and disabled with $\overline{B}_0$ = LOW With C4 enabled, a half channel offset can be programmed with input $\overline{B}_1$ = HIGH, and no offset with $\overline{B}_1$ = LOW.

FEEDBACK TO PRESCALERS (see also Figures 3 and 4)

The counters C1, C0, C – 1 and C – 2 are side-steppable counters, i.e., their division ratio may be increased by one, by applying a pulse to a control terminal for the duration of one division cycle. Counter C2 has 10 states, which are accessible as timing signals for the rate selectors RS1 and RS4. A rate selector, programmed with n (n_1 to n_4 in the UD) generates n of 10 basic timing periods an active signal. Since $n \leqslant 9$, 1 of 10 periods is always non-active. In this period RS1 transfers the output of rate selector RS0, which is timed by counter C3 and programmed with n_0. Similarly, RS0 transfers RSH output during one period of C3. Rate selector RSH is timed by C4 and programmed with n_h. In one of the two states of C4, if enabled, or always, if C4 is disabled, RSH transfers the LOW active signal at input $\overline{RI}$ to RS0. If $\overline{RI}$ is not used it must be connected to HIGH. The feedback output signals of RS1, RS2 and RS3 are externally available as active LOW signals at outputs $\overline{OFB}_1$, $\overline{OFB}_2$ and $\overline{OFB}_3$.

Output $\overline{OFB}_1$ is intended for the prescaler at the highest frequency (if present), $\overline{OFB}_2$ for

the next (if present) and $\overline{OFB}_3$ for the lowest frequency prescaler (if present) A prescaler needs a feedback signal, which is timed on one of its own division cycles in a basic timing period. The timing signal at $\overline{OSY}$ is LOW during the last UD input period of a basic timing period and is suitable for timing of the feedback for the last external prescaler. The synchronization signal for a preceding prescaler is the OR-function of the sync. input and sync. output of the following prescaler (all sync. signals active LOW).

CASCADING OF UDs (see Figure 6)

A UD is programmed into the 'slave' mode by the program input data. $n_{2A} = 11$, $n_{2B} = 10$, $n_{3A} = n_{4A} = n_{3B} = n_{4B} = n_{5B} = 0$. A UD operating in the slave mode performs the function of two extra programmable stages C2′ and C3′ to a 'master' (not slave) mode operating UD More slave UDs may be used, every slave adding two lower significant digits to the system.

Output $\overline{OFB}_3$ is converted to the borrow output of the program data subtractor, which is valid after fetch period 5. Input SI is the borrow input (both in master and in slave mode), which has to be valid in fetch period 0. Input SI has to be connected to output $\overline{OFB}_3$ of a following slave, if not present to LOW. For proper transfer of the borrow from a lower to a higher significant UD subtractor, the UDs have to be programmed sequentially in order of significance or synchronously if the program is repeated at least the number of UDs in the system.

Rate input $\overline{RI}$ and output OFS must be connected to rate output $\overline{OFB}_1$ and the input IN of the next slave UD. The combination thus formed retains the full programmability and features of one UD.

OUTPUT (see Figure 5)

The normal output of the UD is the slow output OFS, which consists of evenly spaced LOW pulses.

This output is intended for accurate phase comparison. If a better frequency acquisition time is required, the fast output OFF can be used. The output frequency on OFF is a factor M • H higher than the frequency on OFS. However, phase jitter of maximum ±1 system input period occurs at OFF, since the division ratio of the counters preceding OFF are varied by slow feedback pulse trains from rate selectors following OFF.

4

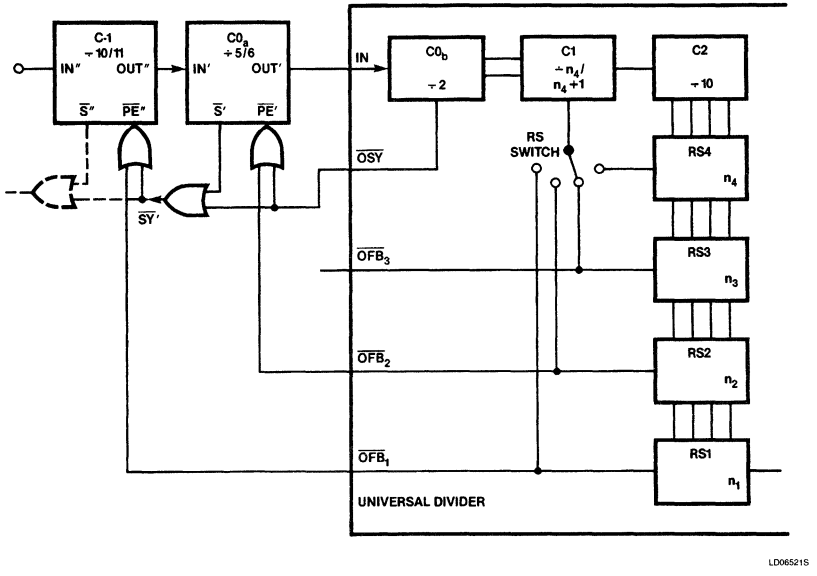
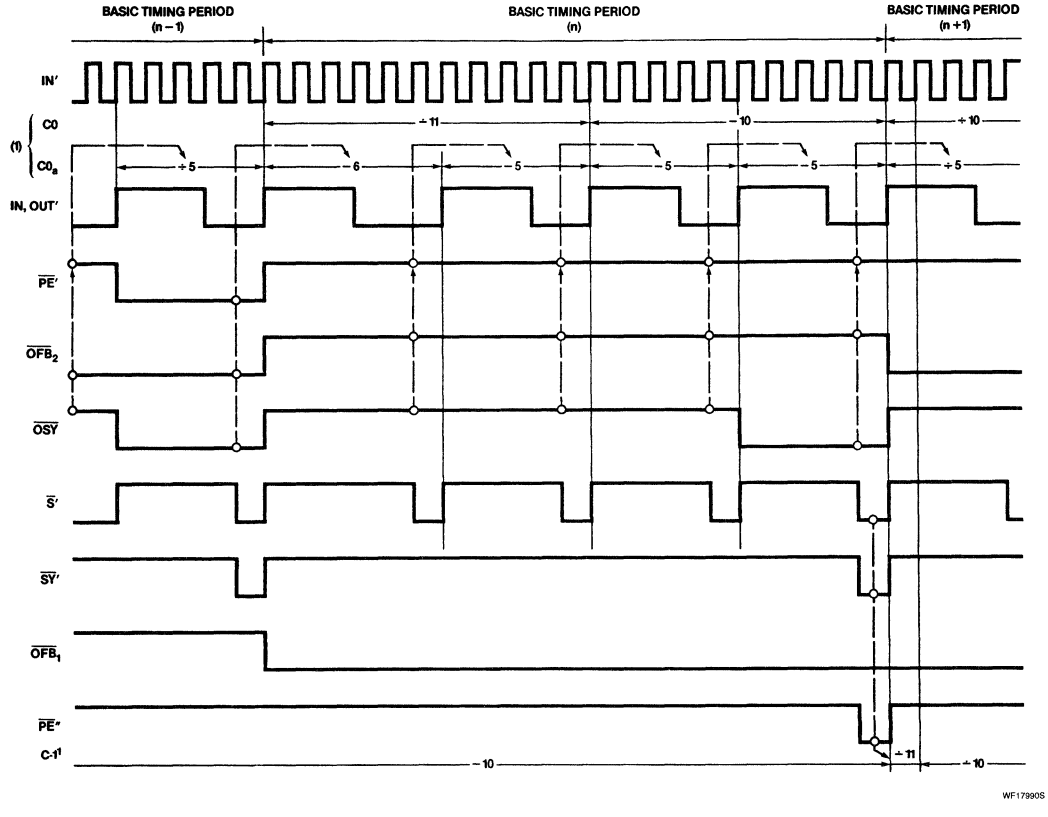


Figure 3. Block Diagram Showing Feedback to Prescalers



NOTE:
1 Scaling factor

Figure 4. Timing Diagram Showing Signals Occurring In Figure 3

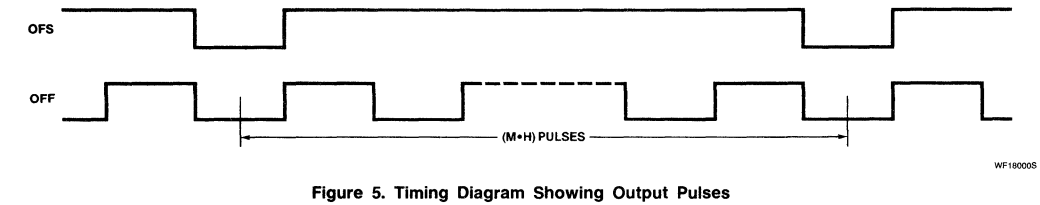


Figure 5. Timing Diagram Showing Output Pulses

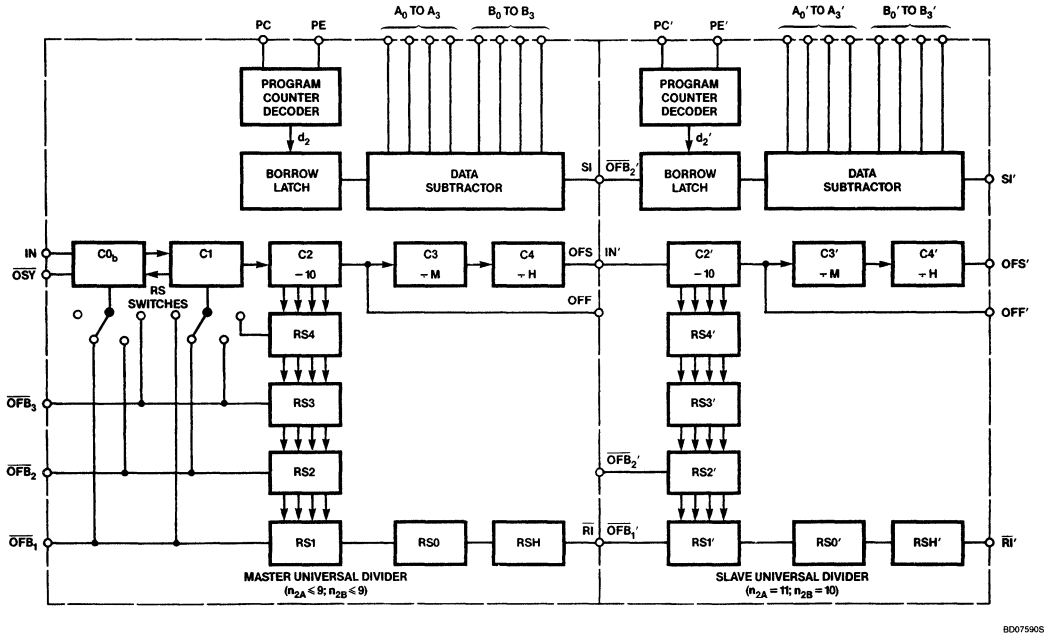


Figure 6. Block Diagram Showing Cascading of UDs

Signetics

SAA1057
PLL Radio Tuning Circuit

Product Specification

Linear Products

DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.

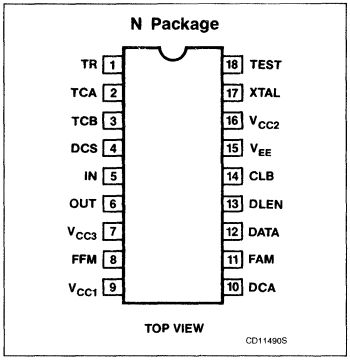
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit-programmable divider for selecting the required frequency.
- A sample-and-hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample-and-hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4MHz quartz crystal. The reference frequency can be chosen either 32kHz or 40kHz for the digital phase detector (that means 1kHz and 1.25kHz for the sample-and-hold phase detector), which results in tuning steps of 1kHz and 1.25kHz for AM, and 10kHz and 12.5kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30V.
- BUS: this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32,767. Latch B contains the control information.

FEATURES

- **On-chip prescaler with up to 120MHz input frequency**
- **On-chip AM and FM input amplifiers with high sensitivity (30mV and 10mV, respectively)**
- **Low current drain (typically 16mA for AM and 20mA for FM) over a wide supply voltage range (3.6V to 12V)**
- **On-chip amplifier for loop filter for both AM and FM (up to 30V tuning voltage)**
- **On-chip programmable current amplifier (charge pump) to adjust the loop gain**
- **Only one reference frequency for both AM and FM**
- **High signal purity due to a sample and hold phase detector for the in-lock condition**
- **High tuning speed due to a powerful digital memory phase detector during the out-lock condition**
- **Tuning steps for AM are: 1kHz or 1.25kHz for a VCO frequency range of 512kHz to 32MHz**
- **Tuning steps for FM are: 10kHz or 12.5kHz for a VCO frequency range 70MHz to 120MHz**
- **Serial 3-line bus interface to a microcomputer**
- **Test/features**

PIN CONFIGURATION



APPLICATIONS

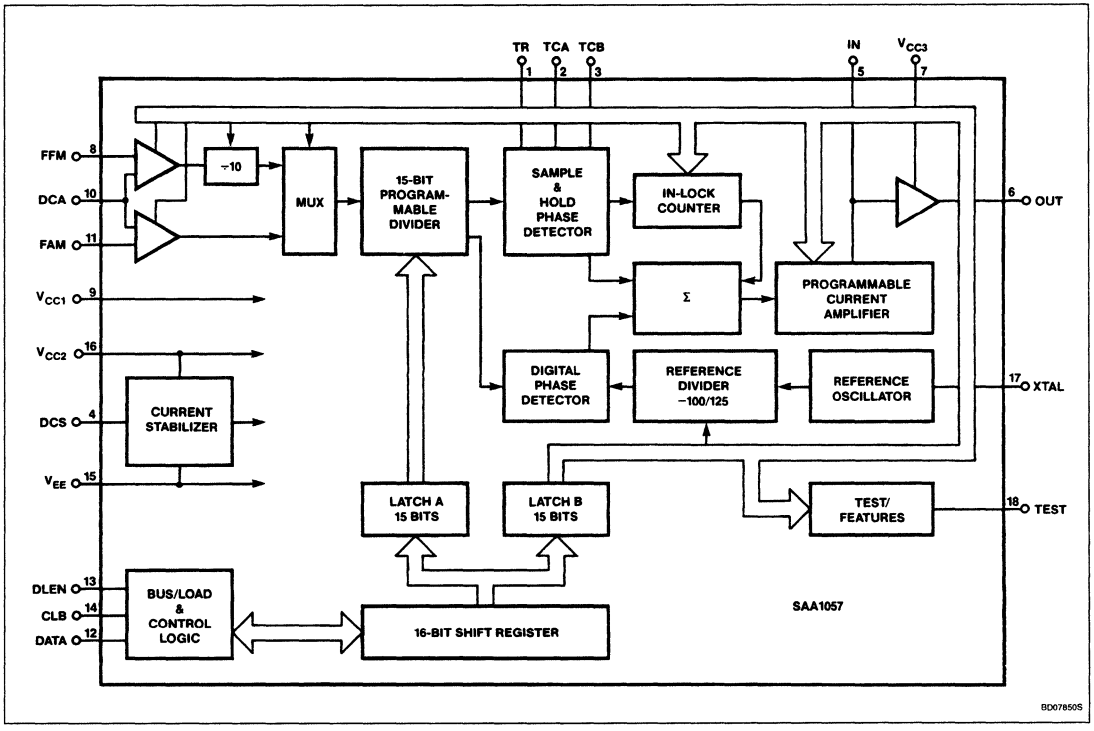
- **Hi-Fi radios**
- **Auto radios**
- **Communication receivers**

PLL Radio Tuning Circuit | SAA1057

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−25°C to +80°C	SAA1057N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1}; V_{CC2}	Supply voltage; logic and analog part	−0.3 to 13.2	V
V_{CC3}	Supply voltage; output amplifier	V_{CC2} to +32	V
P_{TOT}	Total power dissipation	800	mW
T_A	Operating ambient temperature range	−30 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC AND AC CHARACTERISTICS V_{EE} = 0V; V_{CC1} = V_{CC2} = 5V; V_{CC3} = 30V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC1}	Supply voltages		3.6	5	12	V
V_{CC2}			3.6	5	12	V
V_{CC3}			V_{CC2}		31	V
	Supply currents[1]					
I_{TOT}	AM mode	$I_{TOT} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1';		16		mA
I_{TOT}	FM mode	PDM = '0' I_{OUT} = 0		20		mA
I_{CC3}			0.3	0.8	1.2	mA
RF inputs (FAM, FFM)						
f_{FAM}	AM input frequency		512kHz		32	MHz
f_{FFM}	FM input frequency		70		120	MHz
$V_{I(RMS)}$	Input voltage at FAM		30		500	mV
$V_{I(RMS)}$	Input voltage at FFM		10		500	mV
R_I	Input resistance at FAM			2		kΩ
R_I	Input resistance at FFM			135		Ω
C_I	Input capacitance at FAM			3.5		pF
C_I	Input capacitance at FFM			3		pF
V_S/V_{NS}	Voltage ratio allowed between selected and non-selected input			−30		dB
Crystal oscillator (XTAL)[2]						
f_{XTAL}	Maximum input frequency		4			MHz
R_S	Crystal series resistance				150	Ω
BUS inputs (DLEN, CLB, DATA)						
V_{IL}	Input voltage LOW		0		0.8	V
V_{IH}	Input voltage HIGH		2.4		V_{CC1}	V
$-I_{IL}$	Input current LOW	V_{IL} = 0.8V			10	μA
I_{IH}	Input current HIGH	V_{IH} = 2.4V			10	μA

DC AND AC CHARACTERISTICS (Continued) V_{EE} = 0V; V_{CC1} = V_{CC2} = 5V; V_{CC3} = 30V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BUS inputs timing[3] (DLEN, CLB, DATA)						
$t_{CLBlead}$	Lead time for CLB to DLEN		1			µs
t_{Tlead}	Lead time for DATA to the first CLB pulse		0.5			µs
$t_{CLBlag1}$	Setup time for DLEN to CLB		5			µs
t_{CLBH}	CLB pulse width HIGH		5			µs
t_{CLBL}	CLB pulse width LOW		5			µs
$t_{DATAlead}$	Setup time for DATA to CLB		2			µs
$t_{DATAhold}$	Hold time for DATA to CLB		0			µs
$t_{DLENhold}$	Hold time for DLEN to CLB		2			µs
$t_{CLBlag2}$	Setup time for DLEN to CLB load pulse		2			µs
t_{DIST}	Busy time from load pulse to next start of transmission	After word 'B' to other device	5			µs
	Busy time					
t_{DIST}	Asynchronous mode		0.3			ms
t_{DIST}	Synchronous mode[6]		1.3			ms
Sample-and-hold circuit[4, 5] (TR, TCA, TCB)						
V_{TCA}, V_{TCB}	Minimum output voltage			1.3		V
V_{TCA}, V_{TCB}	Maximum output voltage				V_{CC2} – 0.7	V
C_{TCA}	Capacitance at TCA	REFH = '1'			2.2	nF
C_{TCA}	(external)	REFH = '0'			2.7	nF
t_{DIS}	Discharge time at TCA	REFH = '1'			5	µs
t_{DIS}		REFH = '0'			6.25	µs
R_{TR}	Resistance at TR (external)		100			Ω
V_{TR}	Voltage at TR during discharge			0.7		V
C_{TCB}	Capacitance at TCB (external)				10	nF
I_{BIAS}	Bias current into TCA, TCB in-lock				10	nA
Programmable current amplifier (PCA)						
± I_{DIG}	Output current of the digital phase detector			0.4		mA
	Current gain of PCA $V_{CC2} \geq 5V$ (only for P1)					
	CP3 CP2 CP1 CP0					
G_{P1}	P1 0 0 0 0			0.023		dB
G_{P2}	P2 0 0 0 1			0.07		dB
G_{P3}	P3 0 0 1 0			0.23		dB
G_{P4}	P4 0 1 1 0			0.7		dB
G_{P5}	P5 1 1 1 0			2.3		dB
S_{TCB}	Ratio between the output current of S/H into PCA and the voltage on C_{TCB}			1.0		µA/V
ΔV_{TCB}	Offset voltage on TCB 12 in-lock				1	V

DC AND AC CHARACTERISTICS (Continued) V_{EE} = 0V; V_{CC1} = V_{CC2} = 5V; V_{CC3} = 30V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Output amplifier (IN, OUT)						
V_{IN}	Input voltage in-lock; equal to internal reference voltage			1.3		V
	Output voltages					
V_{OUT}	minimum $-I_{OUT}$ = 1mA				0.5	V
V_{OUT}	maximum I_{OUT} = 1mA		V_{CC3} – 2			V
V_{OUT}	maximum I_{OUT} = 0 1mA		V_{CC3} – 1			V
$\pm I_{OUT}$	Maximum output current, V_{OUT} = ½ V_{CC3}		5			mA
Test output (TEST)[7]						
V_{TL}	Output voltage LOW				0.5	V
V_{TH}	Output voltage HIGH				12	V
I_{TOFF}	Output current OFF, V_{TH}				10	μA
I_{TON}	Output current ON, V_{TL}		150			μA
Ripple rejection (see Figure 4)						
	At f_{RIPPLE} = 100Hz					
	$\Delta V_{CC1}/\Delta V_{OUT}$			77		dB
	$\Delta V_{CC2}/\Delta V_{OUT}$			70		dB
	$\Delta V_{CC3}/\Delta V_{OUT}$ $V_{OUT} \leqslant V_{CC3} - 3V$			60		dB

NOTES:

1. When the bus is in the active mode (see BRM in Control information), 4 5mA should be added to the figures given
2. Pin 17 (XTAL) can also be used as input for an external clock The circuit for that is given in Figure 3 The values given in Figure 3 are a typical application example
3. See BUS information in section "Operation Description"
4. The output voltage at TCB and TCA is typically ½ V_{CC2} + 0 3V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2} + 0.3V.
5. Crystal oscillator frequency f_{XTAL} = 4MHz
6. The busy-time after word 'A' to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057 When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5μs will be sufficient
7. Open-collector output

OPERATION DESCRIPTION

Control Information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Figure 2.

FM FM/AM selection; '1' = FM, '0' = AM

REFH Reference frequency selection; '1' = 1.25kHz, '0' = 1kHz (sample-and-hold phase detector)

CP3, CP2, CP1, CP0 Control bits for the programmable current amplifier (see section Characteristics)

SB2 enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA Load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 Phase detector mode

PDM1	PDM0	DIGITAL PHASE DETECTOR
0	X	Automatic on/off
1	0	on
1	1	off

BRM Bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 Test bit; must be programmed always '0'

T2 Test bit; selects the reference frequency (32 or 40kHz) to the TEST pin

T1 Test bit; must be programmed always '0'

T0 Test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (PIN 18)
0	0	0	0	1
0	1	0	0	Reference frequency
0	0	0	1	Output programmable counter
0	1	0	1	Output in-lock counter '0' = out-lock '1' = in-lock

APPLICATION INFORMATION

Initialize Procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.

For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/Asynchronous Operation

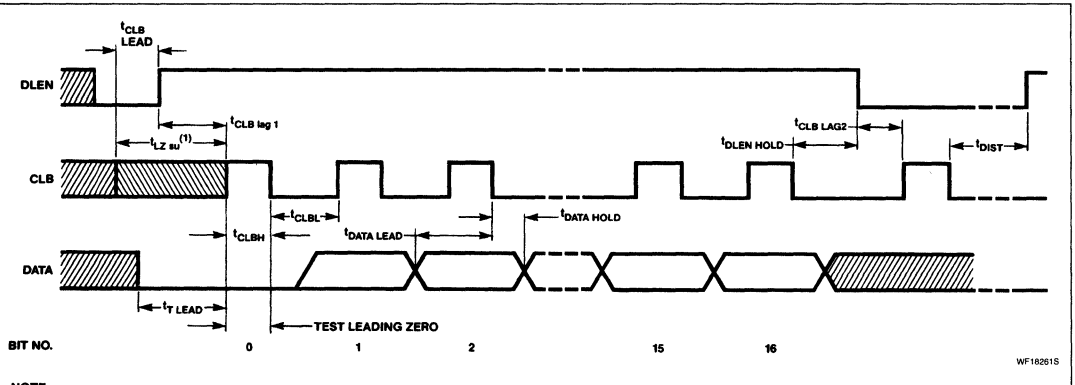
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g., search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the Use of the Programmable Current Amplifier

The lowest current gain (0.023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition.

Transient Times of the Bus Signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



NOTE:
1 During the zero setup time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted This can be of use when an I^2C bus is used for other devices on the same data and clock lines

Figure 1. BUS Format

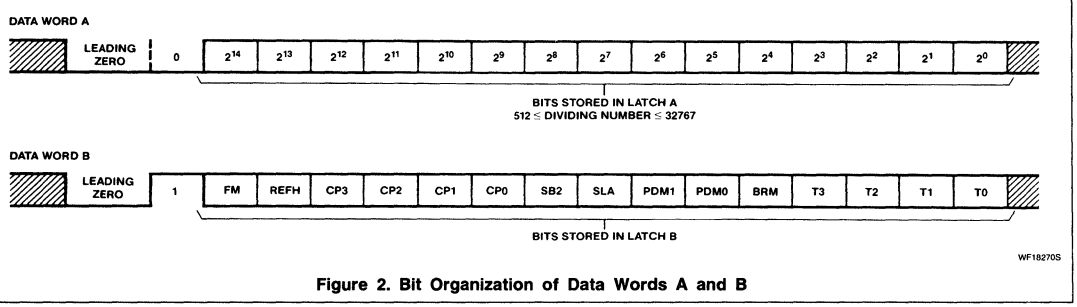


Figure 2. Bit Organization of Data Words A and B

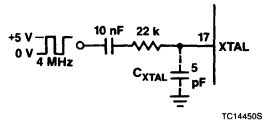
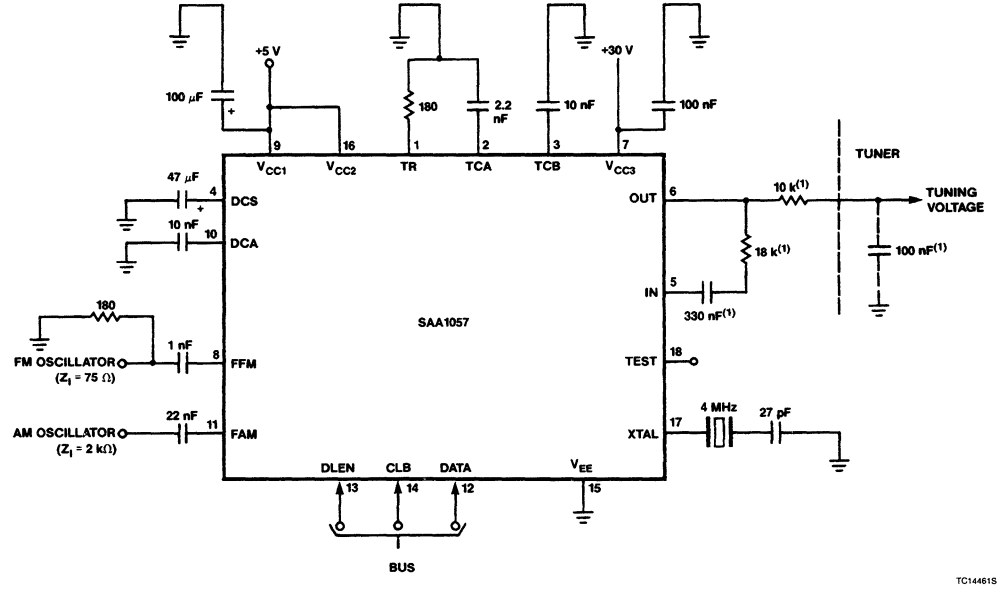


Figure 3. Circuit Configuration Showing External 4MHz Clock



NOTE:
Values depend on the tuner diode characteristics

Figure 4. Application Example of the SAA1057 PLL Frequency Synthesizer Module

Signetics

AN196
Single-Chip Synthesizer for Radio Tuning

Application Note

Linear Products

Authors: J. Matull and J. Van Straaten

To remain competitive, manufacturers of domestic radios must not only produce a comprehensive range of reliable equipment with the required performance at the right price, but must also meet the needs of the market with regard to styling, ease of operation and available functions. Although the widespread use of integrated circuits has allowed vast improvements of performance and reliability and has increased the range of available facilities, the integrated circuits are not always optimally matched, resulting in partial redundancy and a large number of peripheral components. We foresaw this problem and were able to avoid it by using a total systems approach to manufacture our comprehensive range of ideally-matched integrated circuits for signal processing and digital control of tuning, displays and analog functions in all classes of radio. We can now, therefore, devote our design resources and considerable knowledge of integration technologies and techniques to reducing radio manufacturers' development and assembly costs by minimizing the number of integrated circuits needed to implement the wide range of features and facilities required in today's radios.

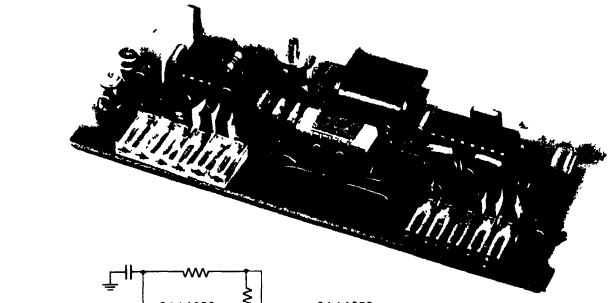
If a radio must incorporate facilities such as search tuning and/or tuning by direct entry of frequency at a keyboard, variable-capacitance diode tuning must be used and a stable local oscillator signal can be generated by indirect frequency synthesis with a phase-locked loop (PLL) controlled by a microcomputer. We have now used bipolar technology to combine analog circuits with several types of logic (I^2L, ECL and miniwatt) so that all the functions previously performed by three integrated circuits can be performed by a single 18-pin LSI integrated circuit called synthesizer module SAA1057. The component economy afforded by the SAA1057 is amply illustrated by Figure 1 which shows that tuning synthesizer functions which previously required the use of three integrated circuits and a large number of peripheral components can now be performed by the SAA1057 and only 16 peripheral components.

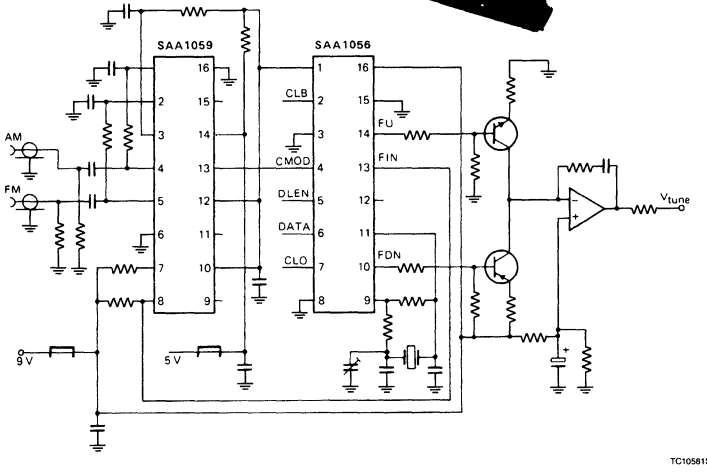
The SAA1057 is not only economical with regard to the required number of components. It also consumes very little current (< 20mA) and is able to meet the varied performance requirements of all classes of radio from battery-powered portables to mains-powered hi-fi tuners. For example, a novel twin-phase detector system in the PLL achieves the fast tuning often required for car radios and also ensures that, when the PLL is locked, the VCO signal has high spectral purity to ensure low distortion in hi-fi tuners. The wide frequency range (AM 512kHz to 32MHz, FM 70MHz to 120MHz) and high maximum tuning voltage (30V) make the SAA1057 suitable for multi-waveband mains sets. The low current consumption combined with the wide supply voltage range (3.6V to 12V) due to internal stabilization allow it to be used in battery-powered portables.

In addition to the basic function of tuning by direct entry of frequency, the SAA1057 can also provide the following software-controlled facilities:

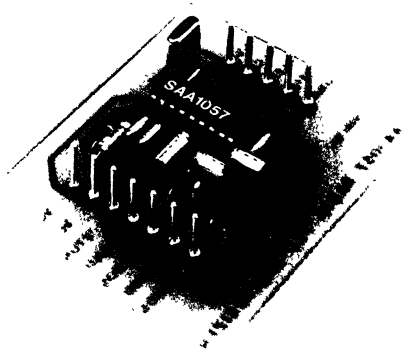
- Search tuning with muted interstation noise
- Continuous up/down step tuning (manual tuning)
- Accurate storage and automatic tuning to preset frequencies
- Loading of frequency data in synchronism with the sampling frequency to prevent disturbance of the tuning lock
- Feed out of a number of internal signals for alignment purposes
- Adjustment of PLL current gain over 40dB range (0.023 to 2.3) to eliminate switching of external loop filter components during waveband selection.

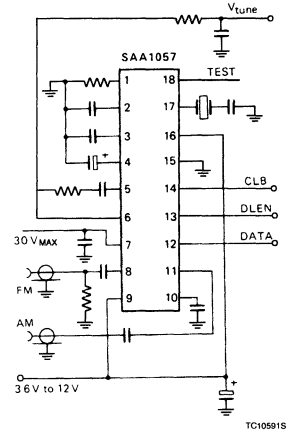
Single-Chip Synthesizer for Radio Tuning AN196





a. Three Integrated Circuits and 36 Peripheral Components





b. Synthesizer Module SAA1057 and 16 Peripheral Components

Figure 1. Basic Radio Tuning Synthesizers

Single-Chip Synthesizer for Radio Tuning AN196

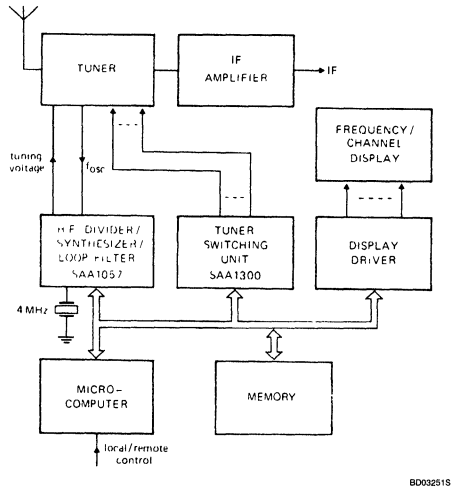


Figure 2. Integrated Circuits for Tuning Systems Using SAA1057

BIPOLAR CIRCUITS

Remote control	
TDB2033	Gain-controlled remote IR receiver amplifier
Frequency synthesizer	
SAA1057	Radio tuning PLL frequency synthesizer
Display drivers	
SAA1060	32-segment LED
SAA1062/T	20 static outputs for LCD
SAA1063	32-segment FTD
Tuner switching	
SAA1300	5-line switching circuit

As the word 'module' in the name of the SAA1057 indicates, this new IC is part of a modular, data bus-compatible, digitally-controlled tuning system in accordance with the system's design philosophy followed for other circuits in our range of ICs for digital systems in radios. The modular approach minimizes radiation and reduces wiring and screening costs because:

- all the sensitive signal processing circuits for the tuning systems are now in the SAA1057 which can be mounted in the ideal position close to the tuner
- internal HF dividers eliminate the need for an external prescaler
- two sensitive, internally-switched VCO inputs to the SAA1057 allow direct connection of the FM and AM local oscillator signals without additional impedance matching, amplification or switching
- the crystal-controlled reference oscillator for the PLL operates at the same frequency for the AM and FM waveband and causes little radiation because it generates a low level sinewave
- the separate microcomputer and memory can be mounted close to the keyboard and their capacity can be tailored to meet the demands of specific radios
- the frequency display driver can be mounted close to its display

As shown in Figure 2, the data bus compatibility of tuning systems using the SAA1057 also allows the simple addition of circuits as required for waveband switching and for driving LED, LCD or fluorescent displays of preset station number, waveband and channel number. Other facilities which can be simply and economically accommodated are analog signal control, extra display functions, and remote control via an infrared data link.

OPERATING PRINCIPLES OF FREQUENCY SYNTHESIS

A basic digitally-controlled PLL for radio tuning is shown in Figure 3. The output from the voltage-controlled local oscillator in the radio is converted into a pulse train, and frequency divided by a programmable divider, before being applied to one of the inputs of the phase detector. The output from the crystal-controlled reference oscillator is converted into a pulse train, and frequency divided by one of two ratios, before being applied to the other input of the phase detector. The phase detector output, which is proportional to the relative phase (and therefore the frequency) of the two input signals, is passed through the low-pass loop filter to remove the high-frequency components and fed back to the VCO as the tuning control voltage. The loop is locked, and the radio correctly tuned, when $f_{OSC} = Nf_{REF}$ where N is the programmable division ratio determined by selecting the frequency of the required broadcast.

BRIEF DESCRIPTION OF THE FUNCTIONS OF THE SAA1057 (Figure 4)

Local Oscillator Inputs

The local oscillator signals from the radio are applied to inputs FFM for FM and FAM for AM. Since these inputs have a sensitivity of 30mV to 500mV (AM) and 10mV to 500mV (FM), the local oscillator signals can be directly applied without preamplification or buffering. A separate pin (DCA) allows the bias circuitry of the internal input amplifiers to be decoupled by an external capacitor. The input frequency range is 512kHz to 32MHz for AM and 70MHz to 120MHz for FM, the FM signals being passed through an internal divide-by-ten HF prescaler which is switched off by software to minimize current consumption while tuning the AM band. Since the AM and FM local oscillator signals are automatically selected by software, they need not be externally switched during waveband selection.

Programmable Divider

This 15-bit frequency divider, which is designed in a special manner to minimize current consumption, is programmed with a binary-coded divisor (N) to synthesize the required frequency for the voltage-controlled local oscillator in the radio. The local oscillator frequency (f_{OSC}) is usually the IF above the tuned frequency. The dividing number is $(32f_{OSC})/f_{REF}$ for AM and $(3.2f_{OSC})/f_{REF}$ for

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MOS CIRCUITS

Display drivers	
PCE2100 PCE2110 PCE2111	40-segment LCD 60-segment LCD + 2 LEDs } in duplex mode 64-segment LCD
PCE2112	32-segment LCD static
SAA1061	16 static outputs for LED drive and switching functions
SAB3044	2-digit LED
Single-chip 8-bit microcomputers	
MAB8021	With 1k byte ROM and 28-pin package
MAB8048	With 1k byte ROM and 40-pin package
MAB84XX	NMOS family with 1 to 4k byte ROM and I^2C bus
MAB85XX	CMOS family with 0.5 to 4k byte ROM and I^2C bus
Memories	
PCD8571	128 × 8-bit CMOS memory with serial I/O
PCB1400	100 × 16-bit EEPROM with serial I/O
Infrared remote-control receivers	
SAB3023	Receiver and analog memory
SAB3033	Receiver and analog memory
SAB3042	Receiver and decoder with C-bus
SAB3028	Receiver and decoder with I^2C bus
Infrared remote-control transmitters	
SAB3004	7 × 64 commands
SAB3021	2 × 64 commands
SAB3027	32 × 64 commands

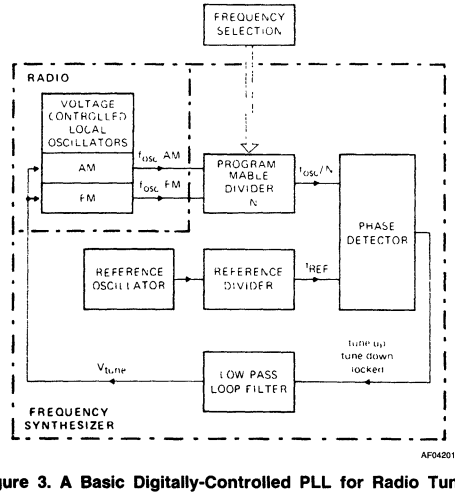

Figure 3. A Basic Digitally-Controlled PLL for Radio Tuning

FM, where f_{REF} is the output frequency from the reference frequency divider (40kHz or 32kHz). The minimum divisor is 512 and the maximum divisor is 32,767. The frequency-divided local oscillator signal is applied as one of the inputs to a dual-phase detector system

Reference Frequency Oscillator

This stable, temperature-compensated oscillator is controlled by an inexpensive 4MHz crystal (series resistance $< 150\Omega$) connected in series with a capacitor between Pin 17 of the SAA1057 and the common return line. The reference frequency may alternatively be derived from a stable external source. In this case, a 4MHz squarewave of $5V_{P-P}$ may be connected to Pin 17 via a series-connected 10nF capacitor and 22kΩ resistors.

Reference Frequency Divider

This circuit divides the frequency of the signal from the reference oscillator by 125 or 100 to obtain a reference frequency of 32kHz or 40kHz for the dual-phase detector system under the control of software. If the selected reference frequency is 32kHz, the minimum tuning step is 1kHz on AM and, due to the divide-by-ten HF divider, 10kHz on FM. If the selected reference frequency is 40kHz, the minimum tuning steps for AM and FM are 1.25kHz and 12.5kHz, respectively. If larger tuning steps are required, integer multiples of these tuning steps can be selected by software.

Phase Detector System

To simplify the design of the PLL loop filter, the SAA1057 incorporates a novel dual-phase detector system that uses the same reference frequency for AM and FM. One of the phase detectors is a high-speed digital memory (flip-flop) type, the other is a high gain and analog memory (sample and hold) type. The digital phase detector operates at the reference frequency, generates about 100 times as much tuning current as the analog phase detector and provides high-speed tuning over a wide frequency range. The analog phase detector operates at 1/32 of the reference frequency, has no region of uncertainty in its transfer characteristic and provides increased spectral purity of the local oscillator signal when the PLL is locked. The 'hold' voltage from the analog phase detector is converted into a DC current and summed with the output pulses from the digital phase detector to provide a current proportional to tuning error. This current drives a gain-programmable amplifier to generate the tuning voltage output.

The analog phase detector is always operating, but the digital phase detector can be switched on/off by setting/resetting the in-lock detector with features/test bits in the software (e.g., to minimize noise during step tuning). If the software does not include any features/test bits, the digital phase detector is automatically switched on if the tuning error exceeds the phase range of the analog phase

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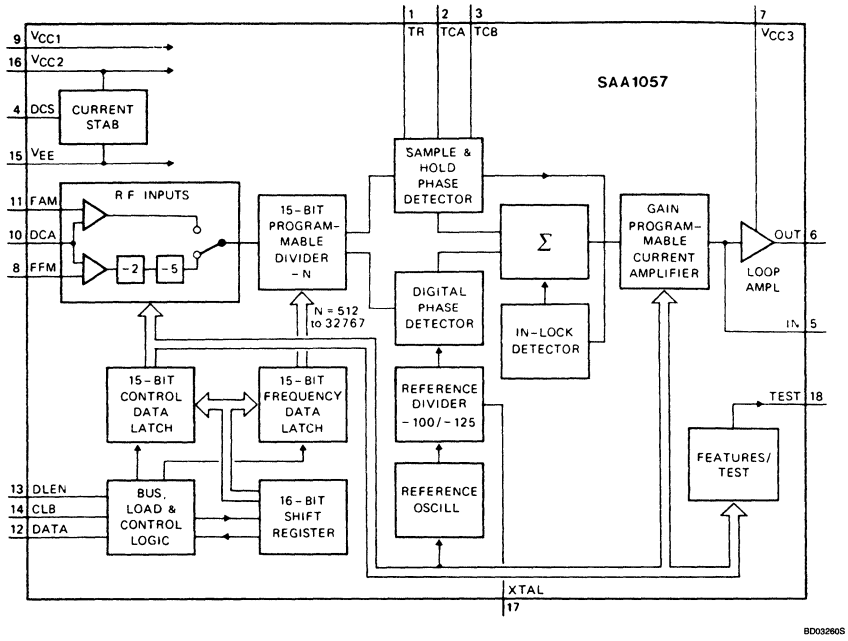

Figure 4. Block Diagram of the SAA1057

detector. This could occur, for example, as the result of executing a large frequency change. When the in-lock detector determines that the tuning error has been reduced to within the operating range of the analog phase detector for three consecutive sampling periods, the digital phase detector is automatically switched off again.

Gain-Programmable Current Amplifier

The sum of the output currents from the two phase detectors drives a gain-programmable bidirectional current source which replaces the normally-used resistor between the charge pump and loop amplifier of a PLL. This allows the loop gain of the PLL to be software programmed over a 40dB range within the limits 0.023 to 2.3, thereby eliminating the need to switch loop filter components during waveband selection.

Loop Amplifier

The loop amplifier is capable of providing a tuning voltage output of up to 30V and only requires a series-connected RC network between its input and output to form an active low-pass loop filter. The supply voltage for the loop amplifier (V_{CC3}) need not be stabilized but it should be adequately filtered.

Reception of Frequency and Control Data

Data for the SAA1057 consists of serially-transmitted 17-bit frequency setting and control words from a microcomputer. Both types of word incorporate a zero start bit which is tested to identify a correct transmission. Each word also contains a latch selection bit which is 0 for a frequency setting word and 1 for a control word. The incoming data is transmitted via an asychronous data highway with separate data (DATA), clock (CLB) and enable (DLEN) lines. The logic levels on the lines are TTL-compatible and are independent of supply voltage.

Sixteen bits of each incoming data word are loaded into a shift register. The bus, load and control logic then checks that the transmission is valid by checking that the first bit is zero and that the word length is correct during the HIGH period of the DLEN line. If valid, the data word is then transferred to the appropriate latch by the next pulse on the clock line.

A frequency-setting word includes fifteen bits which define the required frequency expressed as a 15-bit binary-coded divisor (512 to 32767) for the programmable divider.

A control word includes fifteen bits for the following purposes:

- one bit (FM) to control the switch to select the required input from the AM or FM local oscillator. If the AM input is selected, the divide-by-ten prescaler is switched off to conserve power
- one bit (REFH) to program the divisor for the reference frequency divider
- four bits (CP0 to CP3) to set the gain of the gain-programmable current amplifier
- one bit (SB2) to determine whether the remaining eight features/test bits should be used or not
- one feature bit (SLA) which determines whether frequency setting data is loaded into the programmable divider immediately after reception (asynchronous loading) or synchronized with the sampling frequency (synchronous loading). Synchronous loading is for minimizing noise during manual tuning without muting
- two features bits (PDM0 and PDM1) which set the operating mode of the digital phase detector as previously described

Single-Chip Synthesizer for Radio Tuning AN196

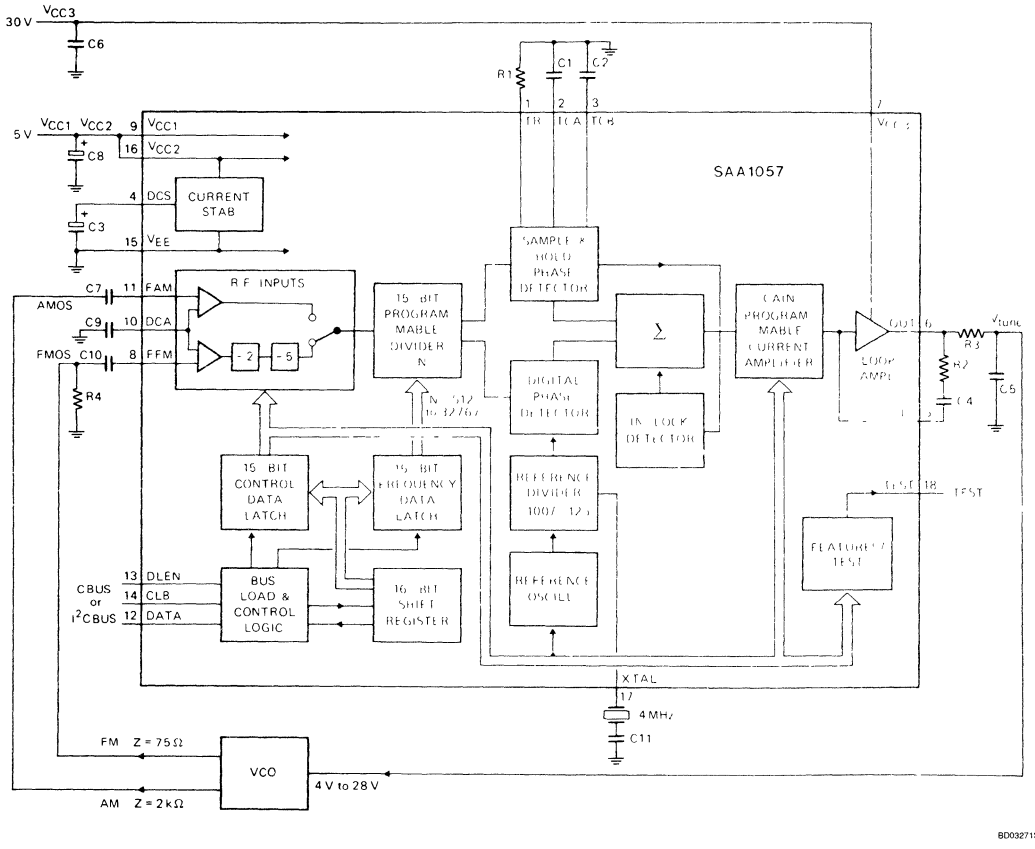

Figure 5. An AM/FM Frequency Synthesizer Using the SAA1057

- one feature bit (BRM) which sets the bus receiver into an automatic mode so that it is switched off to conserve power after a data transmission
- four test bits (T0 to T3) which can route the reference signal, the output from the programmable divider or the output level from the in-lock detector to the TEST pin for alignment purposes

TECHNIQUES USED TO OBTAIN THE HIGH PERFORMANCE OF THE SAA1057

Many new circuit techniques have been used in the SAA1057 to achieve the high performance, application flexibility and low power consumption A description of the techniques listed here is beyond the scope of this article but further information can be found in the references

- travelling-wave dividers in the divide-by-ten prescaler ensure low current consumption and high sensitivity for the RF inputs
- a tail-end divider is used to increase the speed of the digital phase detector
- a rate-select technique in the programmable divider minimizes phase jump in the digital phase detector
- current consumption is minimized by using stacked logic for the three different types of digital circuits (I^2L, ECL and miniwatt) In this way, many of the logic circuits act as current sources for other logic circuits
- use of a bandgap current reference ensures that the current consumption remains constant over a wide range of supply voltage and operating temperature
- the op amps at the RF inputs have an input bias current of less than 10nA and also have a very high slew rate
- the tuning voltage is derived from a 30V op amp with a low bias current and a high slew rate

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BASIC APPLICATION OF THE SAA1057

Figure 5 is the circuit diagram of a complete frequency synthesizer using the SAA1057. The functions and values for each component in the diagram are as follows

REF	FUNCTION	VALUE
R_1	Defines the current in the analog phase detector	180Ω
R_2	Loop filter resistor (value depends on V_{CO})	18kΩ
R_3	Low-pass filter resistor (value depends on V_{CO})	100Ω min 10kΩ typ
R_4	Matching resistor for 75Ω FM input	180Ω
C_1	Sample capacitor (low leakage type)	2.2nF typ
C_2	Hold capacitor (low leakage type)	10nF typ
C_3	Decoupling of internal reference voltage	47μF
C_4	Loop filter capacitor (value depends on V_{CO})	330nF typ
C_5	Low-pass filter capacitor, normally located in the tuner (value depends on loop frequency)	100nF typ
C_6	Power supply filtering	100nF
C_7	DC blocking	1nF
C_8	Power supply filtering	100μF
C_9	Decoupling of RF input stages	10nF
C_{10}	DC blocking	11nF
C_{11}	Series capacitor for crystal (value depends on crystal)	33pF

PERFORMANCE OF THE CIRCUIT FOR FM

Tuning range	87.5 (88) to 108 MHz
Tuning steps	10 kHz or 12.5 kHz
Intermediate frequency	10 7 MHz (variable in steps of 10 kHz or 12.5 kHz)
Tuning voltage of the VCO	4 to 28 V
VCO gain	0.3 to 3 MHz/V
Ref. frequency	32 kHz
Prog. divider ratios	9820 (9870) to 11870
Time to tune across band	< 400 ms
Gain of current amplifier	0.3
Loop filter time constant	1 ms
RMS ripple on tuning voltage noise (20 Hz to 20 kHz)	5 μV
1 kHz	< 1 μV (0 3 μV)

ACKNOWLEDGEMENT

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Signetics

AN197
Analysis and Basic Application of the SAA1057

Application Note

Linear Products

Author. J Matuli

INTRODUCTION

Early digital tuning systems for AM/FM radio receivers were constructed from ICs out of standard logic families (ECL, TTL etc.)

Later, first dedicated ICs for PLL frequency synthesizers have appeared on the market, but there were still several packages required for the complete tuning system. The partitioning of functions depends on the semiconductor technologies used. The tuning part of a digital tuning system typically requires three packages· a prescaler in ECL or Schottky TTL (speed), a programmable divider and other digital functions in either LOCMOS, NMOS or I^2L (packing density, current consumption) and a loop amplifier with FET inputs (low bias current) and a bipolar output stage (current, slew rate).

Now, more sophisticated ICs for digital tuning of radio receivers are showing The SAA1057, being described in this report, belongs to this new generation of radio PLL frequency synthesizers It comprises all of the functions of a digital PLL frequency synthesizer and all active components from the inputs for the local oscillators to the output for the varactor tuning voltage on one monolithic chip, requiring only a minimum of external passive components.

SYSTEM DESCRIPTION

A functional block diagram of the SAA1057 is shown in Figure 1. This system is designed to handle both AM and FM local oscillator frequencies in a microcomputer-controlled radio receiver. Attention has been paid to the power consumption of the IC in order to permit its use in portable as well as in mains operated radios

An important property of the SAA1057 is its very low radiation. This is due to the compact one-chip design which does not require an external prescaler and its control line and due to the crystal controlled reference oscillator which operates with a low sine-wave voltage swing.

RF Inputs

Separate inputs are provided for the AM and FM local oscillators. Amplifiers at the inputs offer high sensitivity for easy interfacing to the radio's VCOs. No external buffers are required. A built-in divide-by-10 prescaler for FM permits a maximum input frequency of 120MHz while the AM input can directly handle up to 32MHz.

An input multiplexer permits both oscillators to be operating at the same time, thus saving cost for switching the oscillators in the radio On AM, the prescaler is switched off in order to reduce the current drain of the chip

There is one pin, DCA, for the decoupling of the input amplifiers' bias circuitry

Programmable Divider

This 15 bit divider is programmed with a binary coded dividing number, N, in order to synthesize a desired frequency f_{VCO} In view of the current consumption, this divider was designed according to the rate select technique. This implies a minimum permissible dividing number, N_{min}, which is equal to 512 in the SAA 1057. The maximum dividing number, N_{max}, is given by the 15 bit length as 32767

Two outputs of the programmable divider are fed to the phase detectors. They differ in frequency by a factor of 32.

Reference Oscillator

This oscillator is designed to operate with a low-cost 4MHz crystal Only one pin is required for this stable, temperature-compensated oscillator

In case of an externally available 4MHz signal of sufficient stability, the pin XTAL can be supplied with a resistor from that source.

Reference Divider

This divider generates the reference frequency for the digital phase detector from the 4MHz crystal frequency. This reference frequency is either 32kHz or 40kHz. It can be changed under software control and outputted at the pin TEST in case that is desired, e g for aligning the frequency of the reference oscillator

With these two reference frequencies, the minimum step size for changing the VCO's frequency is 1kHz and 1 25kHz on AM On FM, the step size is 10kHz and 12 5kHz due to the divide-by-10 prescaler. Larger steps in VCO frequency (integer multiples of the values given above) can be achieved under software control.

Phase Detectors

A novel phase detector concept is used in the SAA1057, permitting the use of the same reference frequency on AM and FM, thereby facilitating the design of the loop filter.

Two phase and frequency sensitive detectors are used in this concept, a high-speed digital flip-flop type detector and a high-gain analog sample and hold type detector. The digital phase detector (PD) operates at the reference frequency and provides for high tuning speed. The analog PD operates at 1/32 of the reference frequency and provides for improved spectral purity of the radio's VCO after lock has been achieved There is no region of uncertainty in the analog PD's transfer characteristic.

The analog PD is always operating. The digital PD can be switched on/off either under software control (see also 2.9) or automatically If no features/test bits are selected, the digital PD is automatically switched on if the operating range of the analog PD is exceeded, e.g. when a jump in frequency is executed. It is automatically switched off again if the operating range of the analog PD has not been exceeded during three consecutive sampling periods. That is accomplished by the in-lock detector. This detector can be set and reset under software control to establish the different modes of PD operation.

The "hold" voltage of the analog PD is converted to a DC current and summed with the output pulses of the digital PD.

Gain-Programmable Current Amplifier

The output current of the phase detector configuration is passed through a gain-programmable amplifier. This is an equivalent for the normally used series resistor from the charge pump to the loop amplifier. The advantage of this solution is that the loop gain can be programmed under software control without any changes in hardware.

Loop Amplifier

The on-chip loop amplifier requires only a CR series connection between its input and output pins to build a basic loop filter. Tuning voltages of up to 30 volts can be generated. The supply voltage for this amplifier, V_{CC3}, need not be stabilized; however, it should be sufficiently filtered.

Analysis and Basic Application of the SAA1057 AN197

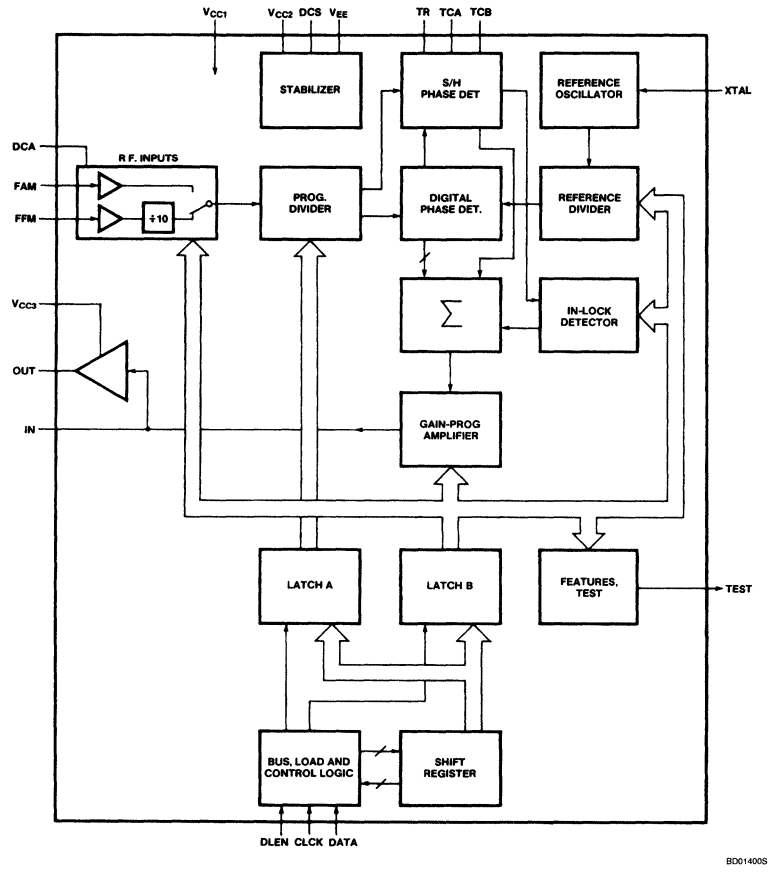

Figure 1. Functional Block Diagram

Data Reception

The SAA1057 requires both frequency and control information from an external microcomputer. This information is received via an asynchronous serial data link with separate data (DATA), shift clock (CLCK) and enable (DLEN) lines. This structure with the associated timing requirements used to be called CBUS. The logic levels on these CBUS lines are TTL compatible, independent of the supply voltage.

Incoming data is received in a shift register. A bus, load and control logic performs a format check on received data and a decision on whether the transmission was valid or not. Only correctly received data are transferred to one of the two latches. Frequency information is stored in latch A and control information in latch B.

Features/Test

In addition to the basic PLL operation of the SAA1057 there are a few features and test functions which can be enabled by certain bits in the control information.

Examples are synchronous loading of frequency data to prevent an out-of-lock condition due to that transmission, disabling of the digital phase detector to avoid tuning noise in case of step tuning, and outputting of the reference frequency, e.g., for the alignment of the crystal oscillator frequency. Details are described in the application section of this report.

Analysis and Basic Application of the SAA1057 AN197

Table 1. Description of Components

R1	Defines current in S/H detector	e g. R1 = 390	Ω
R2	Loop filter resistor, depends on VCO	e.g. R2 = 18	kΩ
R3	Low-pass filter resistor	min. R3 = 100	Ω
R4	Matching resistor for FM input	e.g. R4 = 180	Ω
C1	Sample capacitor, low leakage type	typ. C1 = 2.2	nF
C2	Hold capacitor, low leakage type	typ. C2 = 10	nF
C3	Decoupling of internal reference voltage	typ. C3 = 10	nF
C4	Loop filter capacitor, depends on VCO	e.g. C4 = 330	nF
C5	LOW-pass filter capacitor, mostly located in tuner, depends on loop frequency	e.g. C5 = 100	nF
C6	Power supply filter capacitor	e.g. C6 = 100	nF
C7	DC blocking capacitor	typ. C7 = 1	nF
C8	Power supply filter capacitor	e.g. C8 = 100	nF
C9	Decoupling of RF input stages	typ. C9 = 10	nF
C10	DC blocking capacitor	typ. C10 = 22	nF
C11	Series capacitor for crystal	e.g. C11 = 33	pF
Y1	Crystal for reference oscillator, f = 4.000MHz		

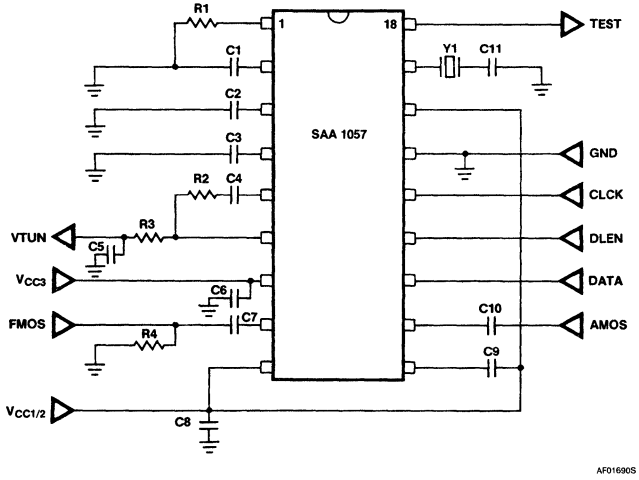

Figure 2. Basic Application

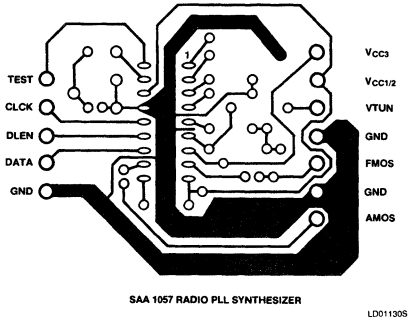

Figure 3. Bottom View of PC Board

Power Supply

Besides the already mentioned supply voltage for the loop amplifier there are two pins for the supply of the whole circuit: V_{CC1} and V_{CC2}. The supply voltage may be chosen in the range from 3.6 to 12 volts without significant influence on the supply current due to the internal stabilizer, which is decoupled at pin DCS. The supply voltage should be well filtered.

APPLICATION

The circuit diagram for the basic application of the SAA1057 in an AM/FM radio receiver is shown in Figure 2; a short description of the components is given in Table 1.

Analysis and Basic Application of the SAA1057 AN197

As there are many ways in which radio receivers can be different from each other, e.g. number of wave bands, supply voltages, tuning voltage range, V/F characteristic of the VCO, the synthesizer circuitry has to be designed for a specific application.

In this chapter information is given on all of the components in the circuit diagram and on the software requirements of the SAA1057 for a number of receiver tuning procedures.

A typical lay-out of a printed circuit board for the application of the SAA1057 is given in Figure 3. There are two connectors; one for the supply voltages and the connection of the radio receiver and one for the CBUS from the microcomputer or a synthesizer controller, like the SYCO II.

Interfacing of the Tuner's Oscillators

The oscillator frequency lines are either realized on a PC board or as a screened cable, depending on their length, among others. The output at the AM VCO is not critical; it can be an inductive or capacitive tap at the resonant circuit, provided the output voltage is at least 30 millivolts rms into a load of 2 kΩ. The minimum required FM oscillator voltage is 10 millivolts rms, the input resistance of the SAA 1057 is 135Ω. In order to minimize the voltage standing wave ratio, VSWR, a resistor, R4, is used to match the input resistance, R_{iFM}, to that of the connecting cable, Z_o. Ignoring the capacitances, R4 can be calculated according to

$$R4 = \frac{R_{iFM} \cdot Z_o}{R_{iFM} - Z_o} \quad (1)$$

Let $Z_o = 75\Omega$, then

$$R4 = \frac{135 \cdot 75}{135 - 75} = 169\Omega$$

The closest standard resistor is R4 = 180 ohms.

The DC blocking capacitors, C7 and C10, should be chosen so that their series reactance at the lowest VCO frequency is small compared to the input impedance. Thus,

$$C7 > > \frac{1}{2 \cdot \pi \cdot f_{FM,min} \cdot R_{iFM}} \quad (2)$$

and

$$C10 > > \frac{1}{2 \cdot \pi \cdot f_{AM,min} \cdot R_{iAM}} \quad (3)$$

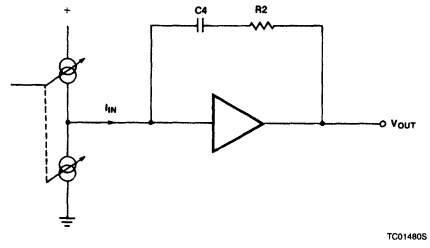

Figure 4. Loop Filter Principle

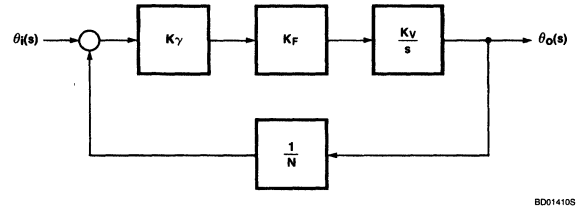

Figure 5. PLL Block Diagram

Interfacing of the Tuning Voltage

The output of the loop amplifier is connected to the varicap tuning diodes via a CR low-pass filter, R3 and C5.

Although there is no lower limit of R3, a minimum of about 100Ω should be used to avoid capacitive loading of the loop amplifier output. For C5, there is normally a lower limit given by the design of the varactor tuned resonant circuits in the radio.

The cut-off frequency of the low-pass filter, f_{1p}, should be less than the sampling frequency, f_s, of the phase detector in order to attenuate potential ripple at this frequency. On the other hand, the cut-off frequency should be high compared to the loop's natural frequency, f_n, to keep the decrease of the phase margin as small as possible. f_n depends on the F/V characteristic of the VCO, the dividing number, N, and the loop filter design.

Thus, the choice of the low-pass filter's cut-off frequency is a compromise between ripple rejection at the sampling frequency and loss of phase margin.

$$f_n < f_{1p} < f_s \quad (4)$$

or

$$\frac{1}{\omega_n} > R3 \cdot C5 > \frac{1}{2\pi \cdot f_s} \quad (5)$$

with $\omega_n = 2 \cdot \pi \cdot f_n$

f_s = 1kHz or 1.25kHz

Designing the Loop Filter

Due to the on-chip loop amplifier and gain-programmable current amplifier, the loop filter consists of only two external components, R2 and C4. The loop filter principle is shown in Figure 4.

As outlined earlier, the commonly used series resistor between charge pump and loop amplifier input is replaced by a gain-programmable current amplifier in the SAA1057. Therefore, the loop filter transfer function evaluates to

$$K_F = \frac{V_{OUT}\ (s)}{I_{IN}\ (s)} = \frac{1 + sT}{sC4} \quad (6)$$

with T = R2 · C4.

The basic block diagram of a PLL in terms of gain is shown in Figure 5.

The output to input ratio reflects a second order system:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_\varphi \cdot K_F \cdot K_V}{s + \frac{K_\varphi \cdot K_F \cdot K_V}{N}} \quad (7)$$

with K_φ = gain of digital phase detector including current amplifier
K_F = gain of loop filter as given in Equation (6)
K_V = gain of VCO
N = integer divisor

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Table 2. Loop Filter Input Current vs. Gain Programming

CP3	CP2	CP1	CP0	I_{dig}
0	0	0	0	0.01mA
0	0	0	1	0.03mA
0	0	1	0	0.1mA
0	1	1	0	0.3mA
1	1	1	0	1.0mA

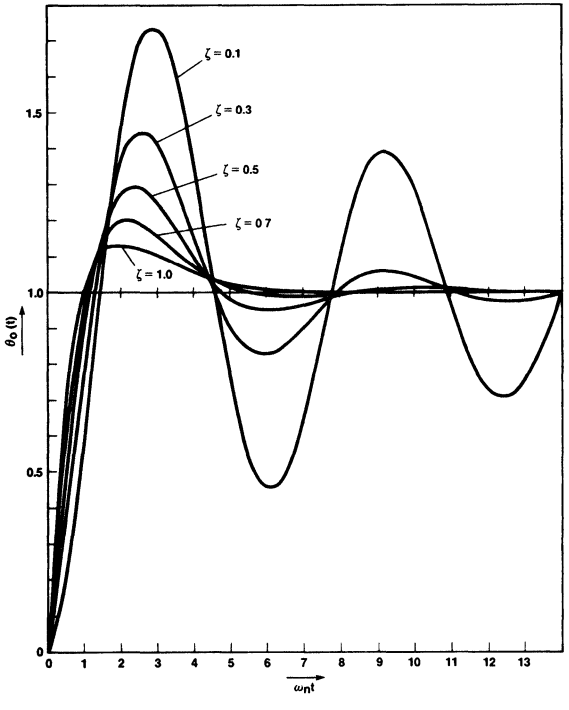

Figure 6. Type 2. Second Order Step Response

Substituting K_F yields

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_\varphi \cdot K_V}{C} \cdot (1 + sT)}{s^2 + s \cdot \frac{K_\varphi \cdot K_V \cdot R2}{N} + \frac{K_\varphi \cdot K_V}{C4 \cdot N}} \quad (8)$$

clearly showing the Characteristic Equation of a second order polynomial:

$$C.E. = s^2 + s \cdot 2\zeta \cdot \omega_n + \omega_n^2 \quad (9)$$

By comparison of coefficients one obtains

$$\omega_n = \sqrt{\frac{K\varphi \cdot K_V}{C4 \cdot N}} \quad (10)$$

$$\zeta = \omega_n \cdot \frac{R2 \cdot C4}{2} \quad (11)$$

with ω_n = loop bandwidth or natural frequency

ζ = damping factor

The gain of the phase detector, $K\mu$, is the output current of the P.D. times the gain of the programmable current amplifier. In order to simplify the calculation, we re-write Equation (10) as follows:

$$\omega_n = \sqrt{\frac{I_{dig} \cdot S_{vco}}{C4 \cdot N}} \quad (12)$$

with I_{dig} = current programmed according to Table 2

and

$$S_{VCO} = \frac{df_{VCO}}{dV_{tune}} \quad (13)$$

being the slope of the VCO's F/V characteristic.

Since neither S_{VCO} nor N remain constant over a larger frequency band, ω_n and ζ should be calculated for several points in the wave band considered, in order to find the appropriate constants for best loop performance. See the Appendix for a design example.

The lock-up time not only depends on the loop filter components but also on the current gain setting. The longest time which can occur is that for a jump from one end of a wave band to the other. It consists of two parts:

$$t_{band} \approx t_{slew} + t_{settle} \quad (14)$$

The output pulses of the digital phase detector can be assumed to have an average duty cycle of 50 o/o during most of the slew time. Therefore, t_{slew} can be approximated as

$$t_{slew} \approx 2 \cdot \frac{C4 \cdot \Delta V_{tune}}{I_{dig}} \quad (15)$$

The settling time, t_{settle}, depends on ω_n and can be estimated from

$$t_{settle} \approx \frac{\omega_n t}{\omega_n} \quad (16)$$

with $\omega_n t$ taken from Figure 6 for a certain overshoot and ω_n as given by Equation (12).

The output phase response of a type 2 second order system (Figure 5) to a phase step input is shown in Figure 6. The curves can also be used for frequency inputs and outputs. The required damping factor, ζ, for a given overshoot can be taken from the plot. Also, the natural frequency, ω_n, can be calculated if ζ and the lock-up time, t_{settle}, are known.

The Analog Phase Detector

In the analog PD a comparison of the relative phase of two digital signals is performed. In principle, a voltage ramp is started by the crystal controlled reference frequency and stopped by the high-speed output of the programmable divider. As only every 32nd output pulse is sampled, the phase jitter of that rate-multiplier type divider is eliminated. The ramp voltage is transferred to the hold capacitor, C2. Any deviation from the ramp's center voltage is converted to a current, amplified in the gain-programmable current amplifier, and fed into the loop amplifier.

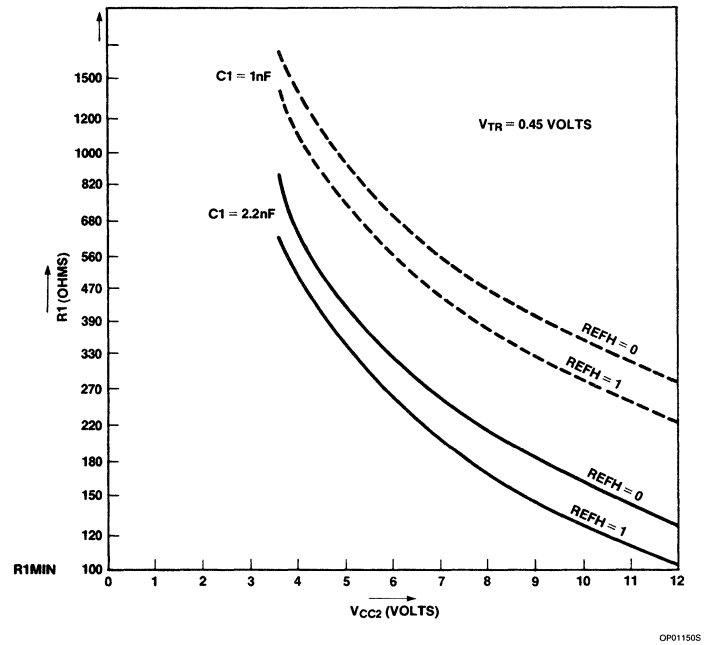

Figure 7. Maximum R1 as a Function of V_{CC2}

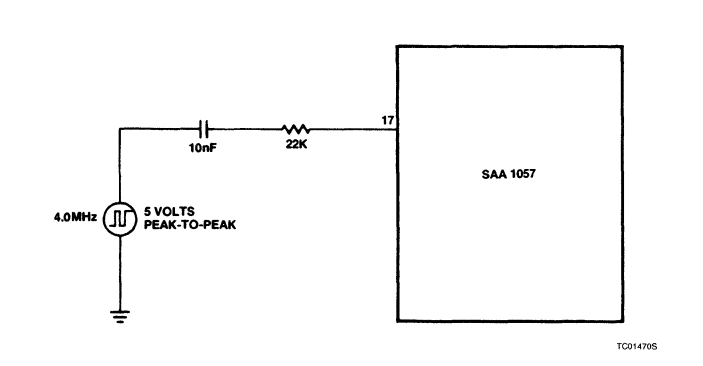

Figure 8. Connection of an External 4MHz Source

Table 3. Loop Filter Input Current Per Volt Change of the Hold Capacitor Voltage

CP3	CP2	CP1	CP0	I_{analog} PER VOLT
0	0	0	0	0.03=μA
0	0	0	1	0.1=μA
0	0	1	0	0.3=μA
0	1	1	0	1.0=μA
1	1	1	0	3.5=μA

The voltage ramp is generated by first charging the capacitor, C1, with internal circuitry and then discharging it with a constant current, which is defined by an external resistor, R1. Thus, the slope of the ramp, i.e. the gain of the analog PD, can be changed by changing the component values of C1 and R1. There are two limitations. For R1, there exists a minimum value of 100 ohms in order to limit the discharge current to a safe value and for C2, there is a maximum value given for both reference frequencies to permit complete pre-charging of that capacitor.

The maximum ramp amplitude depends on the supply voltage, V_{CC2}, and is typically

$$V_{ramp} = V_{CC2} - 2V \quad (17)$$

The time required for a discharge of C1 from $V_{TCA,max}$ to $V_{TCA,min}$ depends on the value of C1 and the discharge current, which is defined by R1. The maximum time is

$$t_{ramp} = \frac{C1 \cdot V_{ramp}}{I_{dis}} \quad (18)$$

With

$$I_{dis} = \frac{V_{TR}}{R1} \quad (19)$$

and the maximum permitted time, t_{dis}, we can calculate the maximum value of resistor R1 to be

$$R1_{max} = \frac{t_{dis} \cdot V_{TR}}{C1 \cdot (V_{CC2} - 2)} \quad (20)$$

V_{TR} is the voltage at pin 1 of the SAA1057 during the discharging of capacitor, C1. The dependency of the upper limit of R1 on V_{CC2} is shown in Figure 7 for two different values of C1.

The center voltage is typically

$$V_{r,o} = \frac{V_{CC2}}{2} + 0.3V \quad (21)$$

giving an operating range of the analog PD of

$$V_{SH} = V_{r,o} \pm \frac{V_{ramp}}{2} \quad (22)$$

As the maximum output current of the analog PD depends on V_{CC2}, only a "gain" constant of 1.5μA/V is specified, i.e. a deviation of 1 volt from the center voltage, $V_{r,o}$, produces an output current of 1.5μA. This current is amplified in the gain-programmable amplifier and then fed into the loop amplifier. In Table 3 there are given some loop filter input current values for different gain settings of the gain-programmable amplifier.

To obtain the maximum currents obtainable from the analog PD, the values in Table 3 have to be multiplied by $1/2 \cdot V_{ramp}$.

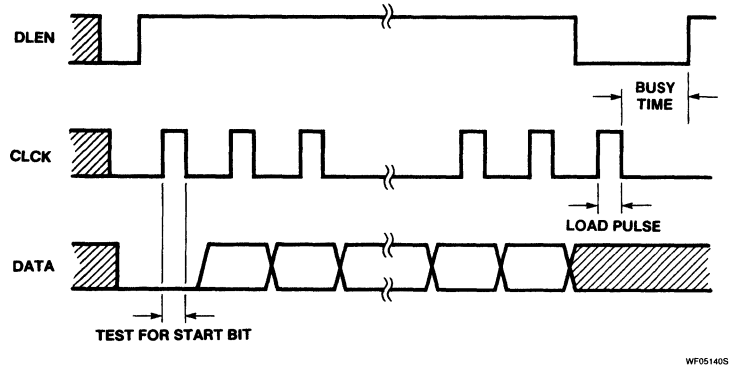

Figure 9. CBUS Timing

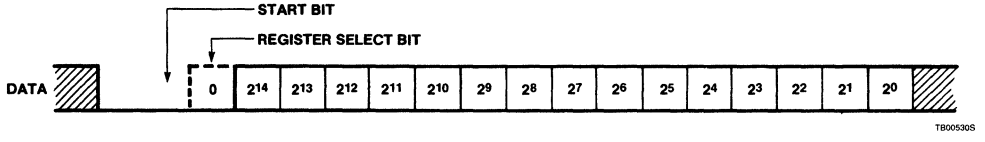

Figure 10. Data Word for Frequency

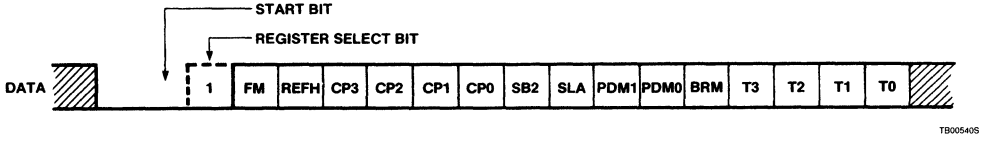

Figure 11. Data Word for Control Information

Generating the Reference Frequency

The simplest way of completing the reference frequency oscillator is to connect a 4MHz quartz crystal from pin 17 (XTAL) to ground.

Any crystal with a series resistance of not more than 150Ω will do. As crystal frequencies are normally specified for a certain external capacitance, a series capacitor, C11, should be connected in series with the crystal, Y1. If the crystal spec is properly chosen, a fixed capacitor will normally do. If we assume a mis-alignment of 50ppm the resulting VCO frequency of e.g. 100MHz would be offset by 5kHz, i.e., half the step size. That is normally unimportant. In special applications, however, it might be necessary to tune the crystal. There is room for a series trimmer capacitor on the PC board.

Table 4. Frequency Programming Range

INPUT		$\frac{f_{REF}}{32}$ = 1kHz	$\frac{f_{REF}}{32}$ = 1.25kHz
AM	f_{min} =	512kHz	640kHz
	f_{max} =	32767kHz	40958.75kHz
FM	f_{min} =	5.12MHz	6.40MHz
	f_{max} =	327.67MHz	409.5875MHz

Another way of generating the reference frequency is the use of an external 4MHz source of satisfactory stability. In Figure 8 it is shown how to connect such an external source.

Please note that the stray capacitance at pin 17 should not exceed 8pF.

Transmitting Data to the SAA1057

All information is entered serially into the SAA 1057. The timing of the CBUS data transmission is shown in Figure 9.

There are two checks performed on data received in the SAA1057:

- a test for the start bit
- a test for correct word length.

The start bit is tested during the high time of the first clock pulse. It has to be '0' to indicate the beginning of a proper transmission.

Table 5. Phase Detector Mode

PDM1	PDM0	DIGITAL PD
0	0	Automatic on/off
0	1	Automatic on/off
1	0	On
1	1	Off

Table 6. TEST Signals

T3	T2	T1	T0	OUTPUT AT TEST (PIN 18)
0	0	0	0	Reference frequency
0	1	0	0	Output of prog divider
0	0	0	1	Output of in-lock detector
0	1	0	1	low = out-of-lock
				high = in-lock

Table 7. Control Information

TRANSMISSION	SB2	SLA	PDM1	PDM0
Control 1	1	0	0	X
Control 2	1	1	0	X
Control 3	1	1	1	1

X = don't care

The word length is defined as the number of clock pulses during the time interval DLEN = '1', i.e., the number of data bits plus 1 (start bit). The word length for the SAA1057 is 17.

Correctly received data are transferred to their latch by another pulse on the CLCK line, the so-called load pulse Clock pulses need not be symmetric; however, minimum high and low times should be observed.

Due to internal data shifting there is a time after the reception of the load pulse during which the SAA1057 does not react to information on the CBUS lines. This time is called busy time. Under worst case conditions this busy time is as long as 1.3 milliseconds, i.e. a following data transmission to the SAA1057 must not start before 1.3 milliseconds have passed since the trailing edge of the load pulse. If the following transmission is, however, intended for a different device, e.g. a display driver, it may start as early as 5μs after the load pulse for the SAA1057.

Frequency Information

The organization of the data word for the setting of frequency is shown in Figure 10.

Frequency is expressed as a dividing number, N, for the programmable divider according to the following formulae

$$N_{AM} = \frac{32 \cdot f_{OSC,AM}}{f_{REF}} \quad (23)$$

$$N_{FM} = \frac{32 \cdot f_{OSC,FM}}{10 \cdot f_{REF}} \quad (24)$$

with f_{OSC} being the VCO frequency (normally the sum of tuning frequency and IF) and

f_{REF} being the reference frequency at the digital PD of either 32kHz or 40kHz.

The dividing number has then to be converted to binary notation in a 15-bit format as shown in Figure 10 and a '0' added for the register select bit, thereby defining latch A as the destination of the data word.

Due to the applied divider principle, the minimum dividing number is $N_{min} = 512$. In case a smaller value is transmitted, N = 512 will be programmed The maximum dividing number of $N_{max} = 32767$ results from the 15-bit length. The total programming range of the SAA1057 is given in Table 4.

Concerning the usability of the given programming range the frequency limits of the SAA1057 (AM. 0.512 to 32MHz, FM: 60 to 120MHz) as well as any relevant licensing regulations (e.g., FCC, GPO etc.) have to be observed.

Control Information

The organization of the data word for the transmission of control information is shown in Figure 11.

By setting the control bits either low or high the mode of operation of the SAA1057 is programmed The register select bit is always '1' to define latch B as the destination of control information.

Control bit FM — With the control bit FM either the frequency at the AM input (FM = '0') or one tenth of the frequency at the FM input (FM = '1') is switched to the input of the programmable divider. In AM mode (FM = '0') a part of the FM signal path is switched off in order to reduce the current drain of the chip

Control bit REFH — With the control bit REFH the reference divider can be programmed for two different dividing numbers, $N_{r0} = 125$ and $N_{r1} = 100$. In connection with the 4MHz reference oscillator this results in the reference frequencies $f_{r0} = 32$kHz and $f_{r1} = 40$kHz and the sampling frequencies $f_{s0} = 1$kHz (REFH = '0') and $f_{s1} = 1.25$kHz (REFH = '1'), respectively.

Control bits CP3 to CP0 — With the control bits CP3 through CP0 the gain of the gain-programmable current amplifier is influenced. In addition to a minimum gain there are 4 steps available which may be combined at will. In Table 2 there are given some programming examples and the resulting loop filter input currents under control of the digital PD. With a given loop filter the PLL gain can be changed under software control in a range of 1 to 100 with intermediate values resulting from programming of bit combinations. The current from the analog PD depends on the amount of phase error and the supply voltage, V_{CC2}, as outlined in section 3 4. See also Table 3 for some current values.

Control bit SB2 — With the control bit SB2 it can be chosen whether the features/test bits (lower half of control word) shall be used (SB2 = '1') or not (SB2 = '0') In case of SB2 = '0' the lower 8 bits of the control word are interpreted as all "zeros" independent of the actual transmitted bit pattern. Please note, that the length of the control word must not be shortened in view of the format requirements of the SAA1057. In case of SB2 = '1' the actual value of the lower 8 bits is used

Control bit SLA — With this control bit it can be chosen whether transmitted frequency information is loaded into the programmable divider immediately after reception (SLA = '0') or synchronized to the sampling frequency (SLA = '1').

Asynchronous loading is mandatory for frequency changes of more than 31 tuning steps, e.g., when recalling a pre-programmed station from memory Synchronous loading (SLA = '1') is recommended for manual tuning without muting in order to minimize tuning noise.

Control bits PDM1, PDM0 — With these control bits the operating mode of the phase detectors is selected according to Table 5.

The meaning of automatic on/off is that in case of a phase error exceeding the operating range of the analog PD the digital PD is

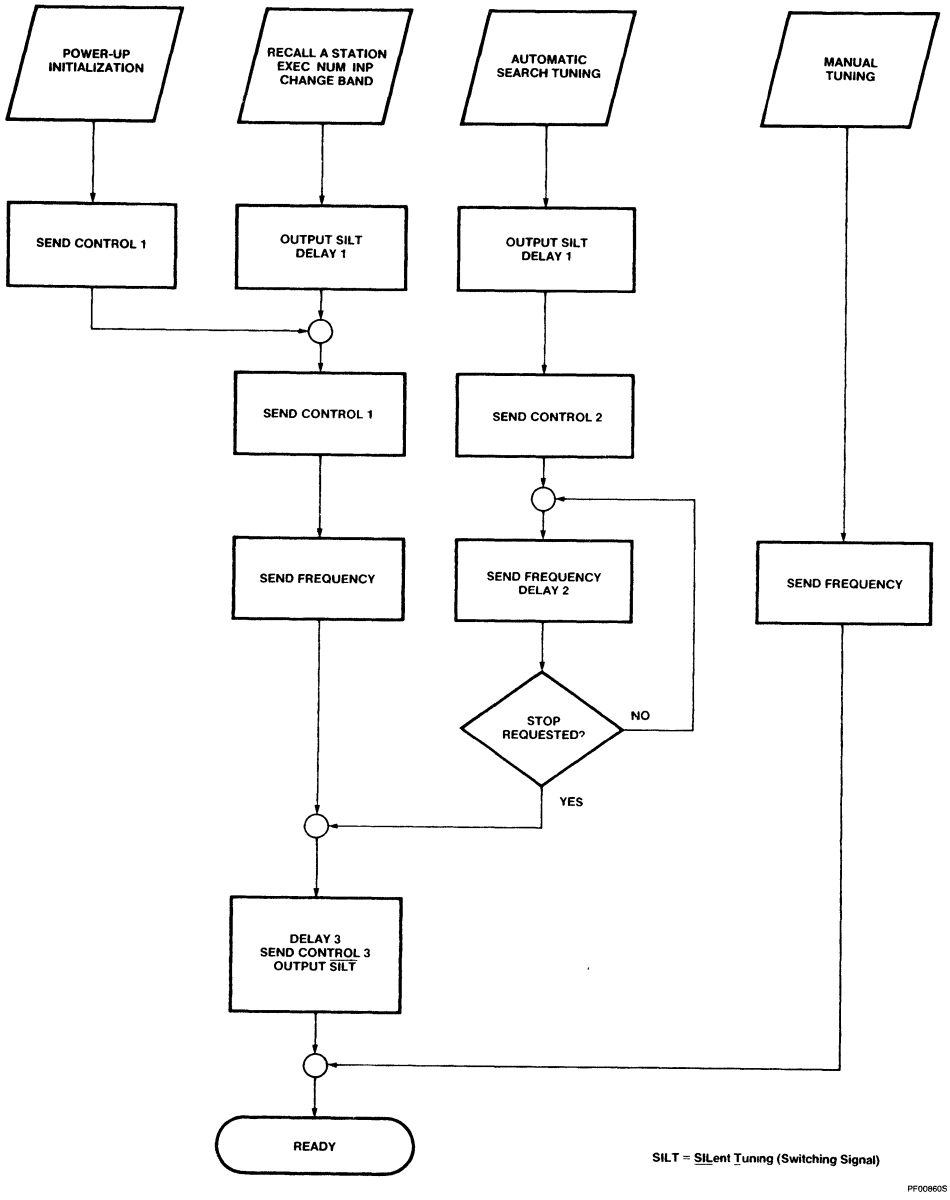

Figure 12. Data Sequences for the Synthesizer

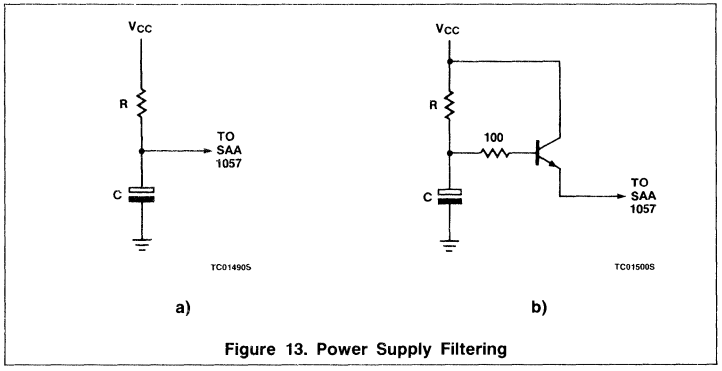

Figure 13. Power Supply Filtering

automatically switched on. It is switched off again as described in section 2.5, i.e. if the analog PD's operating range has not been exceeded during three consecutive sampling periods. For the in-lock condition it is recommended to switch the digital PD permanently off in order to improve the digital PD permanently off in order to improve the VCO's spectral purity. Otherwise, induced disturbances could cause a temporary out-of-lock condition and, thus, an audible noise.

Control bit BRM — With this control bit the bus receiver mode is selected, i.e. whether the bus receiver is permanently switched on (BRM = '0') or automatically switched off after each data transmission (BRM = '1') in order to reduce the current drain.

Control bits T3 to T0 — These bits are test bits. T3 and T1 must always be programmed low. With T2 and T0 a few internal signals can be put out at Pin 18 (TEST) as shown in Table 6.

Software Considerations

After power has been applied to the SAA 1057, an initialization must be performed before any meaningful data transmission takes place. This initialization can either consist of a train of at least 10 clock pulses on the CLCK line and afterwards a transmission of control information (word B) or by transmitting that control information twice, as it contains a sufficient number of clock pulses.

A number of radio tuning operations is executed with the audio part being mute in order to suppress any tuning noise. This applies to recalling of stored stations, executing numerical frequency inputs, changing of wave bands and to automatic search tuning. During manual tuning undistorted listening should be possible. From the above there result a few different sequences of data transmissions from a μC to the SAA1057, as shown in Figure 12.

It is assumed that at power-up the receiver is silent. Therefore, no SILT signal need be output to operate switching or squelch circuitry.

In Table 7 a proposal is made for a few control bits which are not dictated by tuner characteristics or test signals.

FM and REFH depend on the current waveband and the desired VCO step size. CP3 to CP0 depend on the tuner characteristics and tuning time specification, their programming need not be the same for each control word. The word "control 3" sets the synthesizer to synchronous loading of frequency data, i.e. no extra control information is required in case of manual tuning, and switches the digital phase detector off for best spectral purity of the tuner's VCO.

The different delays shown in Figure 12 serve for the following purposes. 'Delay 1' is intended to permit the audio squelch circuitry to reach a certain muting depth before tuning changes. The time is typically in the range between 0 and 50 milliseconds. 'Delay 2' is to adjust search tuning sweep speed to a specified value. The time depends largely on the frequency step size and on receiver time constants. In case of the minimum step size there might be no delay allowed at all. Time is typically between 0 and 50 milliseconds. During 'delay 3' the actual tuning process takes place. In order to permit any frequency to be tuned to, this time is normally between 200 and 500 milliseconds.

The path for manual tuning in Figure 12 depends on the type of actuator, e.g. tuning knob or plus/minus buttons. In case of a tuning knob the tuning speed depends on the user's action. In case of plus/minus buttons and one step per operation it is nearly the same. But in case of an auto-repeat function some time delay is required to adjust the speed, as shown for the path of automatic search tuning.

Please note, that between consecutive transmissions to the SAA1057 there has to be a minimum time delay of 1.3 milliseconds (SLA = '1'). This need not necessarily be a restriction, as processing of data in the microcomputer, e.g. BCD to binary conversion or operating a display driver, also takes time.

Power Supply Requirements

As shown in Figure 2, two different supply voltages are required for the SAA1057. $V_{CC1/2}$ is between 3.6 and 12 volts and V_{CC3} between V_{CC2} and 31 volts, depending on the varactor diodes used in the tuner. If the full programming range of the gain-programmable current amplifier is to be used, $V_{CC1/2}$ should, however, not be less than 5 volts.

Power supply ripple cannot be neglected because of the limited ripple rejection of the SAA1057. For the calculation of permissible power supply ripple let us assume the following:

- we use an FM tuner
- the maximum slope is S_{VCO} = 3MHz/V
- the desired signal-to-noise ratio is SNR = 75dB
- SNR is based on a deviation of $\Delta f = \pm$ 40kHz
- SNR depends on supply ripple only

From the data sheet it can be seen that the rejection of V_{CC2} and V_{CC3} ripple is dominating. If we assume both voltages to be of equal influence each of them has to give an SNR which is 3dB better than specified. The permissible supply ripple voltage (peak-to-peak) can be calculated from

$$V_{r,\,VCCi} = \frac{2 \cdot \Delta f}{S_{VCO}} \cdot 10^{\frac{(r_{VCCi} - SNR - 3dB)}{20}} \qquad (25)$$

with i = 2 or 3, indicating V_{CC2}, V_{CC3}
r_{VCCi} = ripple rejection of V_{CCi} in dB

For the data assumed above we will get
$V_{r,VCC2}$ = 0.6mV peak-to-peak
$V_{r,VCC3}$ = 6mV peak-to-peak

In other words, if the power supply ripple in the basic application of Figure 2 is not greater than indicated above, an overall signal-to-noise ratio of 75dB can be achieved with a VCO slope of 3MHz/V and no other noise sources being present.

If, however, the actual power supply ripple is larger than the limit calculated for a desired SNR, additional filtering has to be used. The design of a filter circuit depends on the permitted voltage drop. If a drop of several volts is acceptable, a circuit as given in Figure 13a can be used. If the drop should be less than 1V, Figure 13b could be used.

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Let us assume that a stabilized supply voltage of 8V with a maximum ripple of 5mV peak-to-peak is available. We choose the filter circuit of Figure 13a to generate the supply voltage $V_{CC1/2}$. The attenuation is given by

$$a = 20 \cdot \log\sqrt{1 + (\omega RC)^2} \quad (26)$$

The required attenuation is $20 \cdot \log (5/0.6) = 18.5$dB. In order not to operate the SAA1057 below 5V, the drop across R should be less than 3V. Thus,

$$R_{max} = \frac{3V}{18mA} = 167\Omega$$

We select
$R = 150\Omega$
$C = 100\mu F$

and obtain an attenuation of
$a = 21$dB @ $f_r = 120$Hz

Now let us calculate component values for Figure 13b as a filter for V_{CC3}. Let us assume a supply voltage of 30V with a ripple of 1 $V_{P\text{-}P}$ and a maximum tuning voltage of 27V. The allowed voltage drop should be less than 1V. The required filter attenuation is 20 log $(1/0.006) = 44.4$dB. Again the attenuation is given by Equation (26). The voltage drop is

$$\Delta V = V_{BE} + \frac{I_E \cdot R}{B} \quad (27)$$

with

I_E = load current = I_{CC3}

B = DC gain of transistor

We select
$R = 10k\Omega$
$C = 22\mu F$

and obtain
$a = 44.4$dB @ fr = 120Hz
$\Delta V = 0.7V$ @ $V_{BE} = 0.6V$
B = 100
$I_E = 1$mA

In case of higher attenuation, i.e. a larger time constant $R \cdot C$, a speed-up path for a quick charging of C at power-on should be provided. Otherwise, V_{CC3} could reach its nominal value too late and tuning to the desired frequency can be delayed.

SUMMARY

This report has described a new microcomputer-controlled AM/FM radio PLL frequency synthesizer IC, the SAA1057, and its basic application.

There are several unique design ideas realized in the IC. The most important is the combination of a digital and an analog phase detector, giving improvements in tuning speed as well as in spectral purity of the VCO. The use of the same reference frequency for both AM and FM tuning simplifies the design of the loop filter. The PLL gain can be programmed in a range of 1 to 100 under software control, thereby eliminating the need for switching of external loop filter components.

For the basic application to AM/FM radios there is information given on hardware, software, power supply and a design example for the calculation of the loop filter.

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APPENDIX

Design Example

Based on the Circuit Diagram of Figure 2 a PLL frequency synthesizer for an FM radio shall be designed. The following tuner data are given:

tuning range	f_{RF} = 88 to 108MHz
tuning steps	Δf_{RF} = 10kHz
intermediate frequency	f_{IF} = 10.70MHz
tuning voltage	V_{tune} = 4 to 28V
VCO gain	S_{VCO} = 3.0 to 0.3MHz/V

S_{VCO} is assumed to decrease linearly from the low end of the tuning range to the high end.

From the tuning step size it is obvious to use REFH = 0, i.e., 32kHz reference frequency. Using Equation (24) we can calculate the min and max values of the dividing number, N, for the programmable divider:

$N_{min} = 9870$
$N_{max} = 11870$

The tuning time from one end of the band to the other is assumed to be not longer than 0.4 seconds. If we split this time into equal parts for the slew and settle times, we can calculate capacitor C4 by rewriting equation (15) as

$$C4 \approx \frac{t_{slew} \cdot I_{dig}}{2 \cdot \Delta V_{tune}} \quad (15a)$$

For the first trial a medium value is taken for the loop filter current, e.g.

$I_{dig} = 0.1$mA (CP = 0010)

We then get from Equation (15a)

$C4 \approx 0.4\mu F$

We choose the closest standard capacitor value of

$C4 = 0.33\mu F$

and calculate an approximate slew time of

$t_{slew} \approx 0.16$ seconds

Now we have to determine the lower limit of the loop's natural frequency and see if the actual frequency is larger. From Figure 6 we read $\omega_n t = 7$ for a maximum overshoot of 1 o/o at an optimum damping factor of 0.7. We re-write Equation (16) as

$$\omega_n = \frac{\omega_n \cdot t}{t_{settle}} \quad (16a)$$

and calculate

$\omega_{n,min} \geq 35 s^{-1}$

with $t_{settle} = 0.2$ seconds being our initial assumption. Using Equation (12) we calculate the loop's natural frequency for the low and high ends of the tuning range.

$\omega_{n,low} = 304\ s^{-1}$
$\omega_{n,high} = 88\ s^{-1}$

As both values are well above the minimum, the settling time will not be larger than assumed and we will not have to change the assumptions made so far.

Now, we have to solve for resistor, R2. Looking at Equation (11) we quickly realize that the damping factor, ζ, will change with ω_n, thereby influencing the overshoot. Let us try to solve this dilemma by calculating R2 for the mid of the tuning range. We take

$N = 10870$
$S_{VCO} = 1.7$MHz/V
$I_{dig} = 0.1$mA
$\zeta = 0.7$
$C4 = 0.33\mu F$

and get

$\omega_n = 218\ s^{-1}$
$R2 = 19500\Omega$

We choose a standard resistor value of

$$R2 = 18k\Omega$$

and check the damping factor with the aid of Equation (11) at the ends of the tuning range end get

$$\zeta_{low} = 0.87$$
$$\zeta_{high} = 0.25$$

The low end value is still good. At the high end the response is highly under-damped, resulting in $\omega_n t = 18$ for a maximum overshoot of 1 o/o. That would mean a settling time of

$$t_{settle} = 0.2 \text{ seconds}$$

which is equal to our assumption. In reality, the digital phase detector will be switched off earlier due to the action of the analog PD. Thus, tuning from one end of the band to the other is achieved in less than 0.4 seconds. If the calculated damping factor ζ_{high} is regarded too small, a new calculation can be started with a higher current gain, e.g. $I_{dig} = 0.3mA$ (CP = 0110). This would result in $\zeta_{high} = 0.45$ and $\zeta_{low} = 1.56$ which is now too large.

For normal applications it seems to be satisfactory to use only one value for the gain-programmable amplifier. Using more than one value within one wave-band requires additional software in the μC because the tuning frequency has to be checked against some cross-over frequency.

For the low-pass filter, R3 and C5, we get from Equation (5) by using $\omega_n = \omega_{n,low}$

$$4.6ms > R3 \cdot C5 > 0.32ms$$

We choose the filter time constant to be 1 millisecond, resulting in component values of e.g.

$$R3 = 10k\Omega$$
$$C5 = 0.1\mu F$$

As the filter capacitor might be designed in view of RF reasons, a modification may be necessary which, however, should include R3 to maintain the time-constant of the low-pass filter.

ADDENDUM

The currently available samples of the SAA1057 are stamped as N 1653. These samples require an extra current of approximately 10μA at room temperature into Pin 4. This extra current can most easily be realized by connecting a resistor between Pins 4 and 16. In this case, the supply voltage $V_{CC1/2}$ shall not be changed, once a resistor value has been fixed. For a nominal supply voltage of $V_{CC1/2} = 5V$, a resistor value of 270kΩ is an adequate solution at room temperature. At ambient temperatures above approximately 40 to 45°C it may be necessary to increase the resistor value.

TDD1742
CMOS Frequency Synthesizer

Product Specification

Linear Products

DESCRIPTION

The TDD1742 is a CMOS low-current frequency synthesizer IC designed for VHF/UHF portable or mobile transceivers. This IC combines in a single chip many features of the HEF4751 (divider circuit), and HEF4750 (synthesizer), including a high-gain phase comparator, using a sample-and-hold technique. A multiplexed or bus-structured programming sequence has been adopted to allow interfacing to an external ROM or a microcontroller. Operation down to a 7V supply rail is possible with a maximum input frequency of 8.5MHz.

Figure 1 shows the functional block diagram of the TDD1742 with the principal features of a reference oscillator, programmable reference and main dividers, the two phase comparators, phase modulator, and the programming input interfaces.

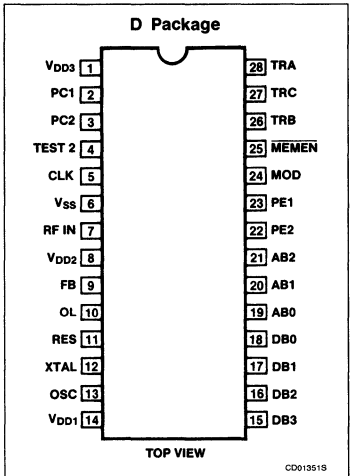
FEATURES

- **Single-chip with on-board sample-and-hold capacitor**
- **Low power requirements**
- **High-performance phase comparator with low phase noise and spurious response**
- **Auxiliary digital phase comparator for fast locking**
- **On-board phase modulator**
- **Simple interface to memory**
- **Microprocessor controllable**
- **Power-on reset circuitry**

APPLICATIONS

- **Cellular radio**
- **Digital frequency synthesizers**
- **Communications equipment (HF-UHF)**
- **Portable transceivers**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	V_{DD3}	Main power supply, +7 to +10V
2	PC1	High-gain phase comparator (analog)
3	PC2	Low-gain phase comparator (digital)
4	Test 2	Test pin
5	CLK	Clock output
6	V_{SS}	Ground
7	RF IN	RF input
8	V_{DD2}	Power supply for TTL-compatible stages, +5V ±10%
9	FB	Feedback to prescaler
10	OL	Out-of-lock indication
11	RES	Power-on reset
12	XTAL	Reference oscillator/buffer output
13	OSC	Reference oscillator/buffer input
14	V_{DD1}	Main power supply; +7 to +10V
15	DB3	Data bus inputs
16	DB2	Data bus inputs
17	DB1	Data bus inputs
18	DB0	Data bus inputs
19	AB0	Address bus
20	AB1	Address bus
21	AB2	Address bus
22	PE2	Program enable 2
23	PE1	Program enable 1
24	MOD	Phase modulation input
25	$\overline{\text{MEMEN}}$	Memory enable
26	TRB	Bias resistor R_B
27	TRC	Bias resistor R_C
28	TRA	Bias resistor R_A

ORDERING INFORMATION

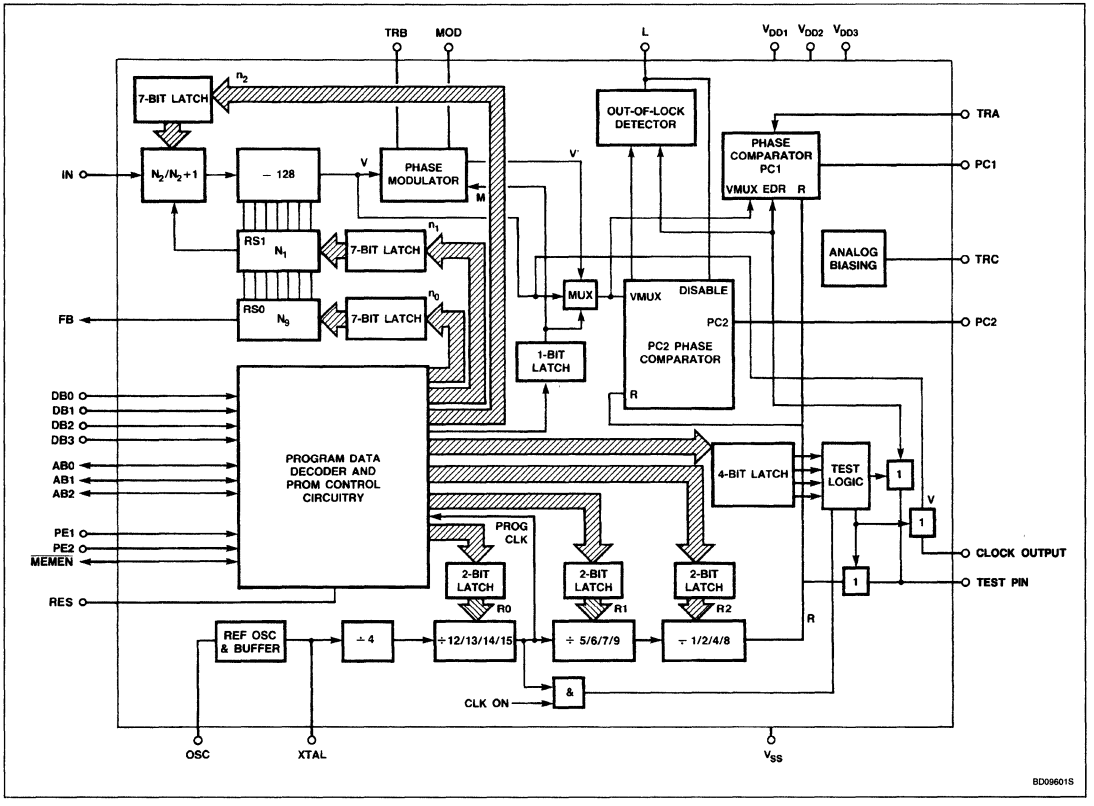
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-136A)	−40°C to +85°C	TDD1742TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD1}, V_{DD2}, V_{DD3}	Supply voltage	−0.5 to +15	V
	Voltage on any input	−0.5 to V_{DD1} +0.5	V
$V_{DD2}-V_{DD1}$	Relative supply voltage	0.5	V
$V_{DD3}-V_{DD1}$	Relative supply voltage	0.5	V
	Direct current into any input	±10	mA
	Direct current into any output	±10	mA
P_D	Power dissipation T_A = 0 to +85°C	500	mW
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature	−40 to +85	°C

CMOS Frequency Synthesizer TDD1742

BLOCK DIAGRAM



PIN DESCRIPTIONS AND FUNCTIONS

SYMBOL	DESCRIPTION
Inputs	
DB0 to DB3	TTL-compatible data bus inputs.
PE1, PE2	TTL-compatible program enable inputs which initiate the programming cycle or strobe the internal data latches.
IN	Input to the main programmable divider, usually from a prescaler (8 5MHz max.).
OSC	Input to reference oscillator which, together with the XTAL output and an external crystal, is used to generate the reference frequency Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
RES	Power-on reset; following power-up, an initial pulse is applied to this pin to set the internal counters.
MOD	High-impedance linear phase modulator input, which applies a voltage-controlled delay to the output of the programmable divider before being applied to the phase comparator input.
Outputs	
PC1	High gain phase comparator output is used when the system is in lock to give low levels of noise and spurious outputs. This comparator uses a sample-and-hold technique similar to that used in the HEF4750, but in the TDD1742 the sample-and-hold capacitor is on-chip
PC2	Low gain digital phase comparator which enables fast lock times to be achieved when the system initially is out-of-lock. This comparator is inhibited when the phase is within the locking range of PC1, i.e., 3-state output.
OL	Out-of-lock flag which is HIGH when the digital phase comparator PC2 is in operation, i.e., when the system is out-of-lock.
FB	Feedback output to control the modulus of the external prescaler
XTAL	Output to form crystal oscillator circuit in combination with the OSC input.
Bidirectional pins	
AB0 – AB2	TTL-compatible bidirectional address bus. Provides address output to an external memory or receives output from a microcomputer. The outputs are all 3-State with internal pulldowns.
$\overline{\text{MEMEN}}$	Mode control and memory enable pin At general reset, the mode of operation can be set to microcomputer mode, $\overline{\text{MEMEN}}$ LOW, or memory mode, $\overline{\text{MEMEN}}$ HIGH. For further information, see PROGRAMMING section.
TRA	Current mirror pin for control of the gain of PC1.
TRB	Current mirror pin for control of the phase modulator gain.
TRC	Current mirror pin for analog biasing.
T_2	Test pin should be left unconnected.

DC ELECTRICAL CHARACTERISTICS at V_{DD_1} = 7.4V, V_{DD_2} = 5.0V, V_{DD_3} = 7.4V; T_A = 25°C; voltages are referenced to V_{SS}, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
	Supply voltage				
V_{DD1}	Pin 14	7		10	V
V_{DD2}	Pin 8	4.5		5	V
V_{DD3}	Pin 1	7		10	V
I_{DD1}	Quiescent device current [2, 3]			1.5	mA
I_{DD2}				100	μA
I_{DD3}				1.5	mA
$\pm I_{IN}$	Input current logic inputs, MOD [2, 3]			300	nA
	Output leakage current at ½ V_{DD} [2, 3]				
$\pm I_Z$	PC2, high-impedance OFF-state			50	nA
$\pm I_Z$	$\overline{\text{MEMENB}}$, high-impedance state			1.6	μA
I_Z	I/O current, high-impedance state AB0 to AB2	5		30	μA
	Logic input voltage				
	LOW				
V_{IL}	CMOS inputs CMOS I/O			$0.3V_{DD1}$	V
V_{IL}	TTL inputs TTL I/O's			0.8	V
	HIGH				
V_{IH}	CMOS Inputs CMOS I/O	$0.7V_{DD1}$			V
V_{IH}	TTL inputs TTL I/O's	2			V
	Logic output voltage[2]				
	$\lvert I_O \rvert < 1\mu A$				
V_{OL}	LOW			50	mV
V_{OH}	HIGH[2]	$V_{DD1}-50$			mV

DC ELECTRICAL CHARACTERISTICS (Continued) at V_{DD_1} = 7.4V, V_{DD_2} = 5.0V, V_{DD_3} = 7.4V; T_A = 25°C; voltages are referenced to V_{SS}, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Logic output voltage LOW[2]				
	Output $\overline{MEMENB}$				
V_{OL}	I_{OL} = 4mA			1	V
	Output PC2				
V_{OL}	I_{OL} = 1.5mA			0.5	V
	Outputs CLK, OL				
V_{DL}	I_{OL} = 1mA			0.5	V
	Output XTAL at:				
V_{OL}	I_{OL} = 3mA			0.5	V
	Output FB				
V_{OL}	I_{OL} = 1mA			0.5	V
	Outputs AB0, AB1, AB2				
V_{OL}	I_{OL} = 0.2mA			0.4	V
	Logic output voltage HIGH[2, 3]				
	Output PC2				
V_{OH}	I_{OH} = −1.5mA	V_{DD1} − 0.5			V
	Outputs CLK, OL				
V_{OH}	I_{OH} = −1mA	V_{DD1} − 0.5			V
	Output XTAL at:				
V_{OH}	I_{OH} = −3mA	V_{DD1} − 1			V
	Output FB				
V_{OH}	I_{OH} = −1mA	V_{DD2} − 1			V
	Outputs AB0, AB1 at:				
V_{OH}	I_{OH} = 0.2mA	2.4			V
	Output AB2 at:				
V_{OH}	I_{OH} = 0.8mA	2.4			V
I_O	Output PC1 sink current [2, 3, 4]	1			mA
$-I_O$	Output PC1 source current [2, 3, 5]	1			mA
R_{IN}	Internal resistance of PC1, locked state |output swing| ⩽200mV, specified output range: [2, 3] 0 5V_{DD} − 0.5V to 0.5V_{DD} + 0.5V		2.0		Ω

4

AC ELECTRICAL CHARACTERISTICS The dynamic specification is given for the circuit, built up with the external components as given in Figure 4, unless otherwise specified.

SYMBOL	DESCRIPTION	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{IN}	Programmable divider input frequency, all division ratios	Square wave input	8.5			MHz
f_{DIV}	Reference divider input frequency, all division ratios	Square wave input	9			MHz
f_{OSC}	Crystal oscillator frequency		9	12		MHz
C_{IN}	Input capacity IN, OSC				3	pF
C_{IN}	Input capacity DB0 to DB3, PE1, PE2, AB0 to AB2				5	pF
t_{PDHL} t_{PDLH}	FB feedback output to external[6] prescaler delays IN → FB	C_L = 10pF		35 35	70 70	ns ns
I_{DD}	Average power supply current [3, 7]	Locked state				
I_{DD1}				2		mA
I_{DD2}				0.15		mA
I_{DD3}				0.45		mA

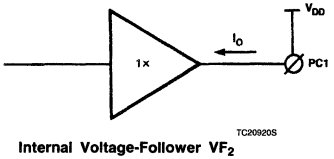
NOTES:

1. Definitions:
   R_A = External biasing resistor between pins TRA and V_{SS}
   R_B = External biasing resistor between pins TRB and V_{SS}
   R_C = External biasing resistor between pins TRC and V_{SS}
   C_A = Decoupling capacitor between pins TRA and V_{DD}
   C_B = Decoupling capacitor between pins TRB and V_{DD}
   C_C = Decoupling capacitor between pins TRC and V_{DD}

   CMOS logic inputs . OSC, RES
   CMOS logic outputs · OL, PC2, XTAL, CLK
   CMOS logic I/O : MEMENB
   TTL logic inputs : DB0 to DB3, PE1, PE2
   TTL logic output : FB
   TTL logic I/O : AB0 to AB2
   Analog inputs : MOD, IN
   Analog output : PC1
   Analog biasing pins : TRA, TRB, TRC

2. All logic inputs at V_{SS} or V_{DD}
3. R_A connected, its value chosen such that $I_{TRA} = 20\mu A$
   R_B connected, its value chosen such that $I_{TRB} = 20\mu A$
   R_C connected, its value chosen such that $I_{TRC} = 20\mu A$
4. **EQUIVALENT CIRCUIT:**

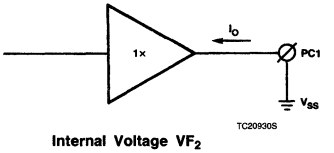
   INPUT FORCED LOW BY 2 PRECEDING R PULSES



Internal Voltage-Follower VF_2

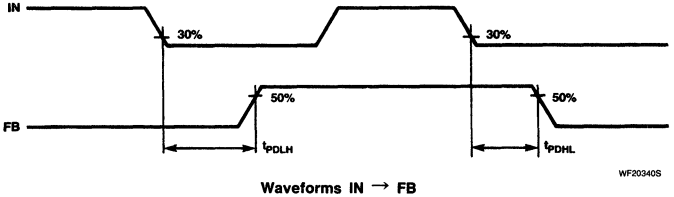
5. **EQUIVALENT CIRCUIT·**

   INPUT FORCED HIGH BY 2 PRECEDING V PULSES



Internal Voltage VF_2

6.



Waveforms IN → FB

7. f_{OSC} = 5MHz, external clock, division ratio 420
   f_{IN} = 2MHz, division ratio 168

REFERENCE OSCILLATOR AND DIVIDER CHAIN

The reference oscillator chain comprises a crystal oscillator and dividers to give the required reference frequency drive to the phase comparators.

A single inverter is used as an oscillator stage and oscillates satisfactorily with crystals up to 9MHz. Alternatively, an external reference source may be applied to the input of this inverter (OSC pin) at logic level drive or at a lower level (300mV min) if a biasing resistor is connected from OSC to XTAL. The reference divider chain comprises a fixed ÷4 stage followed by three cascaded programmable dividers with ratios of ÷12/13/14/15, ÷5/6/7/9 and ÷1/2/4/8. The output of this last stage is applied as one input to the two phase comparators. Hence, a number of division ratios are possible between 240 and 4320, enabling all the usual VHF and UHF channel spacings to be accommodated with reference crystals in the range 1 – 9MHz.

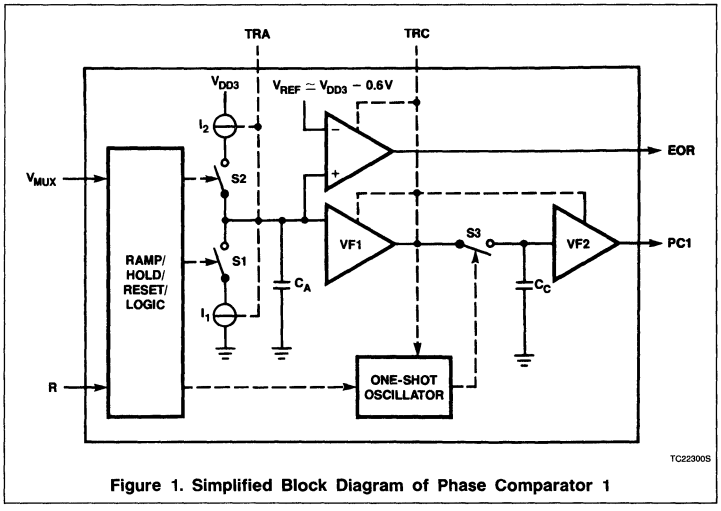


Figure 1. Simplified Block Diagram of Phase Comparator 1

MAIN PROGRAMMABLE DIVIDER

The main programmable divider is a rate feedback binary divider. Referring to the Block Diagram, the programmable divider uses a fixed 7-bit binary divider (÷128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider ($\div n_2/n_2 + 1$) and the other rate selector controls an external dual modulus prescaler (÷A/A + 1).

The overall division ratio (N) is given by:

$$N = (128\ n_2 + n_1)A + n_0$$

where $0 \leqslant n_0 \leqslant 127$
$0 \leqslant n_1 \leqslant 127$
$1 \leqslant n_2 \leqslant 127$

To remain fully programmable, the maximum allowable division ratio for the external prescaler is ÷128/129. Providing that this ratio is not exceeded, the divider may be programmed to divide by any number between 128 × A and approx. 16383 × A. The maximum allowable input frequency to the main LOPSY divider is 8.5MHz using a 7V rail and this is one of the parameters which determine the selection of a suitable prescaler. The output from the programmable divider is fed to the phase comparators via the phase modulator. The phase modulator is bypassed if not selected.

PHASE COMPARISON

The TDD1742 contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analog output, 4500 volts/cycle at 10kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.

Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

Phase Comparator 1 (See Figure 1)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1

A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.

A negative-going transition at the R input terminates the linear ramp. Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2μs), the sample switch S3 is closed for approximately 1μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.

The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.

If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Figures 2 and 3.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\ I_{TRA}}{F_R}$$

where:
I_{TRA} is in μA
F_R is the phase comparator reference frequency in kHz.

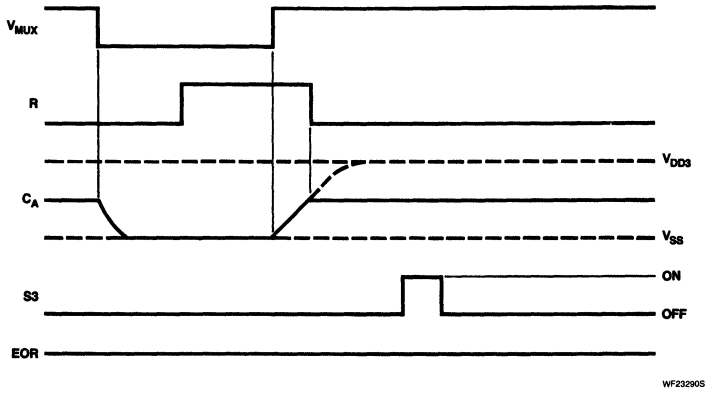
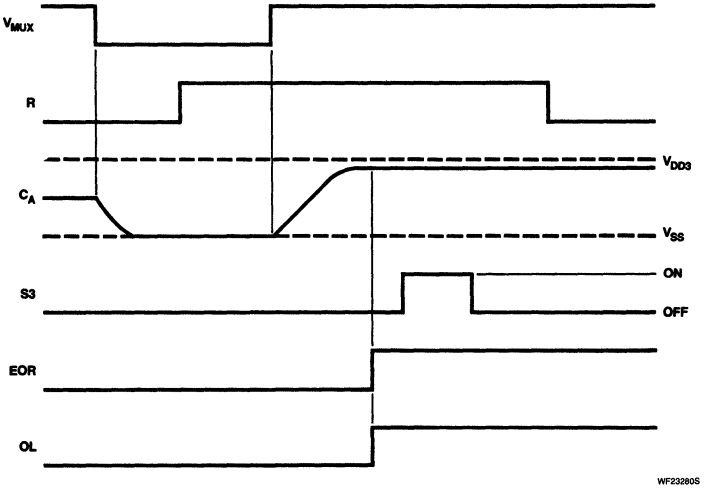


Figure 2. Waveforms of Phase Comparator 1; In-Lock Condition



NOTES:
When V_{MUX} leads R the output signal at Pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at Pin 2 (PC1) remains LOW.

Figure 3. Waveforms of Phase Comparator 1; Out-of-Lock Condition

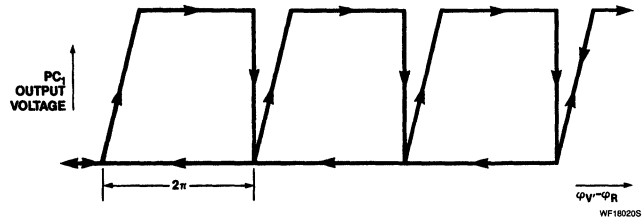


Figure 4. Phase Characteristic of Output PC1

Phase comparator 2 (See Figure 5).

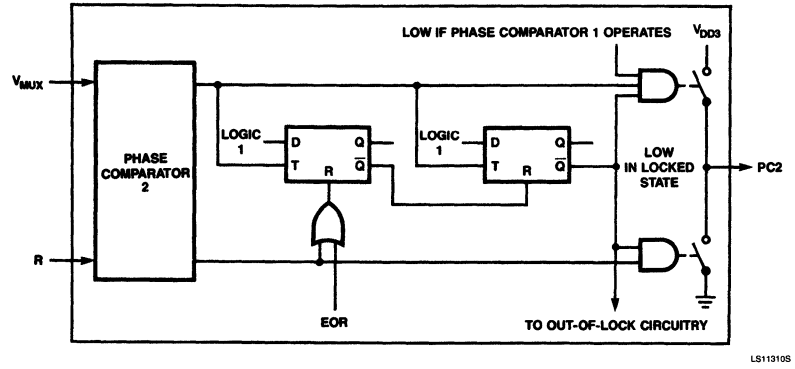


Figure 5. Simplified Block Diagram of Phase Comparator 2

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1. Phase Comparator 2: Stable States and Corresponding Output Levels

STATE	V_{MUX} LEADS R	R LEADS V_{MUX}
Reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Figure 6.

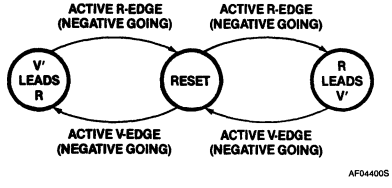


Figure 6. Transition of State; Phase Comparator 2

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.

The average output voltage is a linear function of the phase difference. Output at Pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX} + R^*$
  or
- $2R + V_{MUX}$

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

Out-of-Lock Function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R however, out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.

In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase Modulator (See Figure 8)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between Pin 26 and ground.

The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{TRB}} \text{ ns/volt of input applied to Pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V′ level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V′ pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Figure 9. The phase

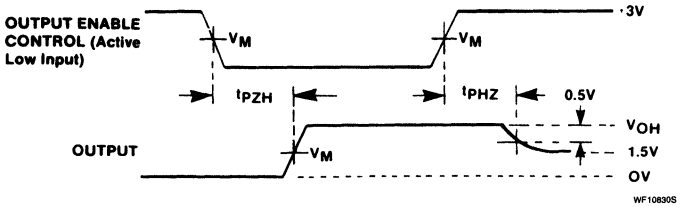


Figure 7. Phase Characteristic of Output PC2

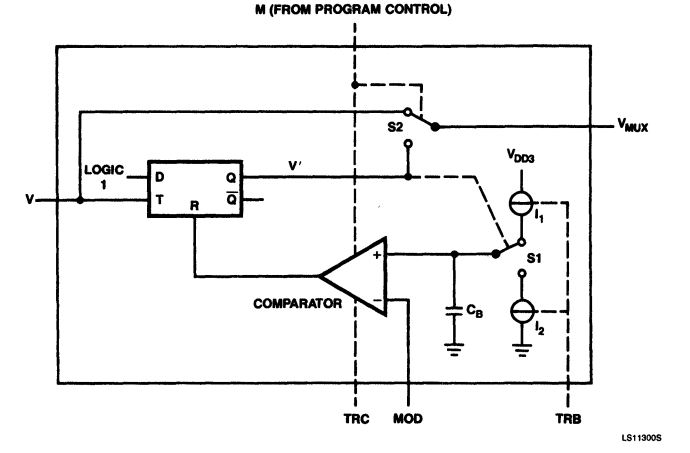


Figure 8. Simplified Block Diagram of the Phase Modulator

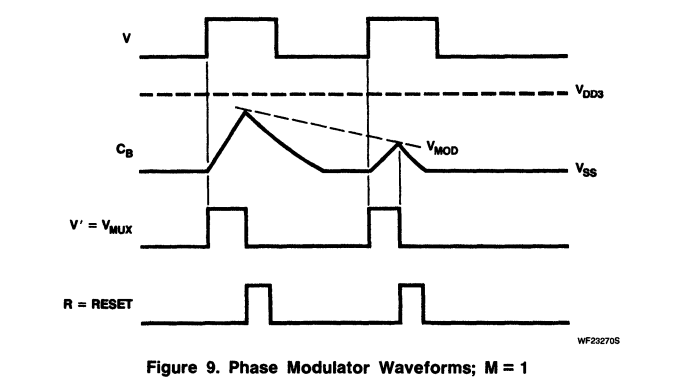


Figure 9. Phase Modulator Waveforms; M = 1

*This means apply two successive active V_{MUX} edges followed by one active R edge.

modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve this, the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

PROGRAM CONTROL

A multiplexed or bus structured sequence allows the TDD1742 to be interfaced to a microcontroller or a PROM

The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742 is programmed with a total of 32 bits which are organized as eight 4-bit words The address bus is 3 bits wide and the data bus is 4 bits wide Both buses are TTL compatible The data words are described in detail in Tables 3 to 7.

Microcontroller Mode

If Pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742 when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE-OR condition; see Figure 10 and Table 2). One frame of 8 words is necessary to completely program the TDD1742. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.

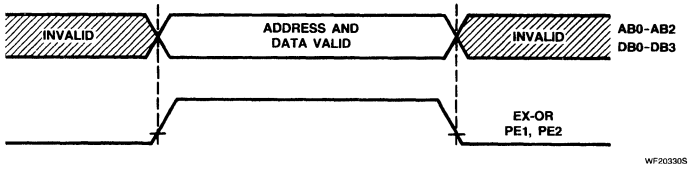


Table 2. Truth Table for Program Enable Function; Microcontroller Mode

PE1	PE2	LOAD
0	0	No
1	0	Yes
0	1	Yes
1	1	No

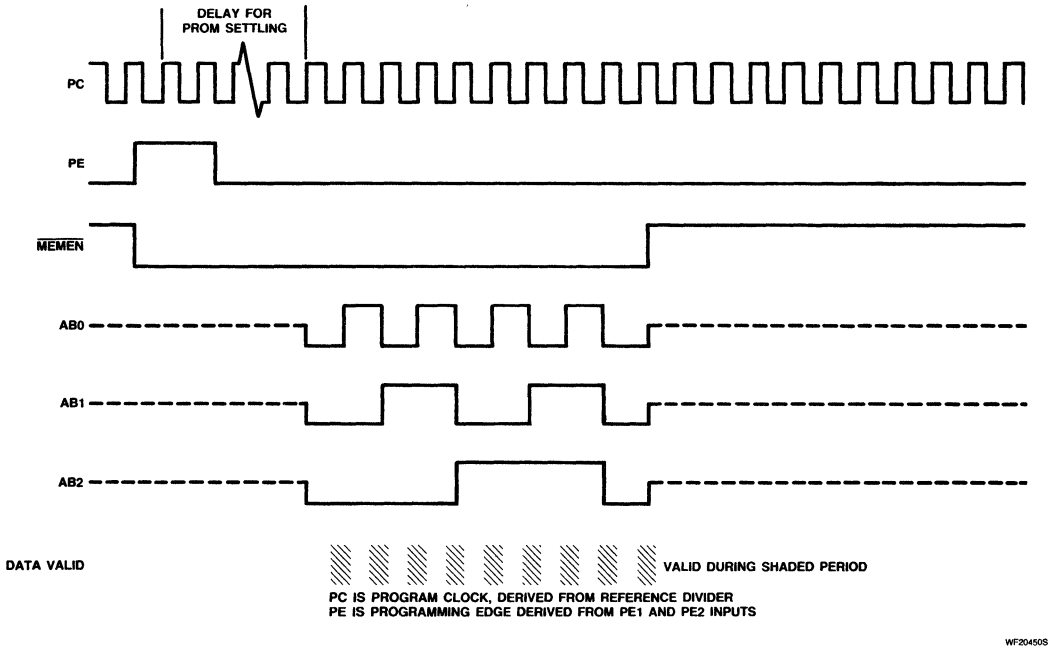
Figure 10. Waveforms for Program Enable Function; Microcontroller Mode

Memory Mode (PROM)

If Pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742 is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (Pin 23) or PE2 (Pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (Pin 11).

At the start of a programming sequence Pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses During the second half of each address period, data from the memory is latched into the TDD1742 so that the access time of the PROM is not critical.

NOTE:
The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$ After the full 32 bits have been read the address returns to address 000 before going 3-State This step transfers data from the internal data latches to the appropriate divider latches Pin 25 now returns to a high impedance state and power is removed from the memory Figure 11 shows the timing for a reset initiated programming sequence, the timing is similar for program enable initiated sequence



NOTES:
1. Delay time for PROM settling
2. The program clock is derived from the reference divider chain
3. Data is valid during the shaded period

Figure 11. Timing Diagram for TDD1742 PROM Control

DATA MEMORY MAPS

In Table 3 n_0, n_1 and n_2 comprises the main programmable divider. $n_0$0 is the LSB of n_0, $n_0$6 the MSB and so forth. If M is 1 the modular is ON.

Table 3. Bit Programming of the Eight 4-Bit Words

ADDRESS			DATA			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	See Table 4			
0	0	1	$n_0$3	$n_0$2	$n_0$1	$n_0$0
0	1	0	$R_0$0	$n_0$6	$n_0$5	$n_0$4
0	1	1	$n_1$3	$n_1$2	$n_1$1	$n_1$0
1	0	0	$R_0$1	$n_1$6	$n_1$5	$n_1$4
1	0	1	$n_2$3	$n_2$2	$n_2$1	$n_2$0
1	1	0	M	$n_2$6	$n_2$5	$n_2$4
1	1	1	$R_2$1	$R_2$0	$R_1$1	$R_1$0

Table 4. Memory Map For Address 000

DB3	DB2	DB1	DB0	PROGRAM CLOCK TO OUTPUT CLK	MODE
0	0	X	X	Yes	Idle
0	1	0	0	No	Idle
All Other Combinations				Not defined	Not defined

Where
X = Don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000

Table 5. Reference Divider Control; Part 1

$R_0$1	$R_0$0	Division Ratio
0	0	12
0	1	13
1	0	14
1	1	15

NOTE:
$R_0$0 and $R_0$1, control the ÷ 12/13/14/15 portion of the reference divider.

Table 6. Reference Divider Control; Part 2

$R_1$1	$R_1$0	Division Ratio
0	0	9
0	1	5
1	0	6
1	1	7

NOTE:
$R_1$0 and $R_1$1 control the ÷ 5/6/7/9 portion of the reference divider

Table 7. Reference Divider Control; Part 3

$R_2$1	$R_2$0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	8

NOTE:
$R_2$0 and $R_2$1 control the ÷1/2/4/8 portion of the reference divider.

Current Biasing

Current biasing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between Pin 28 (TRA) and ground. The value of the resistor must be such that $I_{TRA} = 20\mu A$, which acts as gain control for analog phase comparator 1

Bias Resistor B: is connected between Pin 26 (TRB) and ground. The value of the resistor must be such that $I_{TRB} = 3$ to $25\mu A$, which acts as gain control for the phase modulator.

Bias Resistor C: is connected between Pin 27 (TRC) and ground. The value of the resistor must be such that $I_{TRC} = 5$ to $30\mu A$, which provides biassing for the remainder of the analog circuitry.

4

Signetics

AN177
An Overview of the Phase-Locked Loop (PLL)

Application Note

Linear Products

Portions of this Phase-Locked Loop section were edited by Dr. J.A. Connelly

INTRODUCTION

The basic phase-locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922. Since that time, PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems involved in these applications frequently are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been at microwave frequencies and employ complex phase shifters, signal splitters, modulation, and demodulation schemes such as biphase and quadraphase. Because of the high frequencies involved in microwave applications, most all components of these PLL systems are made from discrete as opposed to integrated circuits. However, in other communication system applications such as FSK and FM and AM demodulation where frequencies are below approximately 100MHz, monolithic PLLs have found wide application because of their low cost versus high performance.

A block diagram representation of a PLL is shown in Figure 1. Phase-locked loops operate by producing an oscillator frequency to match the frequency of an input signal, f_i. In this locked condition, any slight change in f_i first appears as a change in phase between f_i and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match f_i. The locking onto a phase relationship between f_i and the local oscillator accounts for the name phase-locked loop.

A MECHANICAL ANALOG TO THE PLL

To better visualize the frequency and phase relationships in a PLL, consider the mechanical system shown in Figure 2 which is a dual to the electronic PLL. This mechanical system has two identical, heavy disks with two separate center shafts attached to each disk. Each shaft is presumed to be mounted on a bearing that allows each massive disk to be rotated in either direction when some external force is applied. The shafts are coupled together by a spring whose end points are fixed to each shaft. This spring can be twisted in either direction, depending upon the relative positions of the shafts. The spring cannot "kink up" due to the shafts passing through the center of the spring.

Now suppose the sequence of events shown in Figure 3 occurs to the mechanical system. The disks are simply represented like clock faces with positional reference markers. Initially, both disks are stationary in a neutral position. Then the left disk, or input, is advanced slowly clockwise through an angle θ_1 position. The right disk, or output, initially doesn't move as the spring begins to tighten. As the input continues to move and when it reaches θ_2, begins to turn and tracks the input with a positional phase shift error of

$$\theta_e = \theta_2 \qquad (1)$$

At any point in time, with both disks slowly turning at the same speed, there will be some inherent phase error between the disks, or

$$\theta_e = \theta_3 - \theta_4 \qquad (2)$$

This positional phase error in the mechanical system is analogous to the phase error in the electronic PLL. When the input disk coasts to a stop, the output also gradually comes to a stop with a fixed phase error equal to that in Equation 2 or

$$\theta_e = \theta_5 - \theta_6 = \theta_3 - \theta_4 \qquad (3)$$

The spring has a residual stored twist in one direction due to θ_e.

Now consider that the disks are first returned to their neutral positions. Then the input disk is instantaneously rotated through an angle of θ_1 as shown in Figure 4. The output disk can't respond instantaneously because of its large mass. It doesn't move instantaneously and the spring develops considerable torque. Then, as shown in the sequence of events in Figure 4, the output disk begins accelerating after some delay due to the large phase error. It swings past the stopped position of the input disk due to its momentum, reaches a peak overshoot, and gradually ascillates about θ_1 with a damped response, finally coming to rest with some small residual phase error. The input twist of θ_1 represents the application of a step of position or phase to the system, and the response of the output disk is typical for a second-order, underdamped system. This same type of second-order behavior occurs in the PLL system for an instantaneous change of input phase.

As a final example, consider the events in Figure 5 where both disks are rotating at a constant rate. Applying a strobing light (strobotac) simultaneously to both disks and adjusting its flashing rate to one flash per disk rotation will cause the positional markers to appear stationary. There will be a constant phase error in this case just as there was in Figure 3. Now suppose the revolution rate of the input disk gradually increases by a small amount to a new rate. The positional marker will appear to walk around the disk. The output first senses the increased rate of the input through an increase in the phase error.

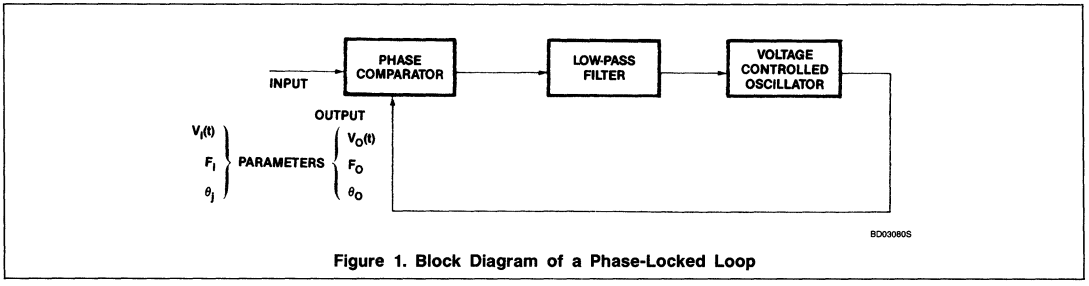


Figure 1. Block Diagram of a Phase-Locked Loop

An Overview of the Phase-Locked Loop (PLL) AN177

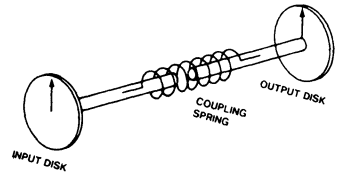


Figure 2. Mechanic Analog to PLL

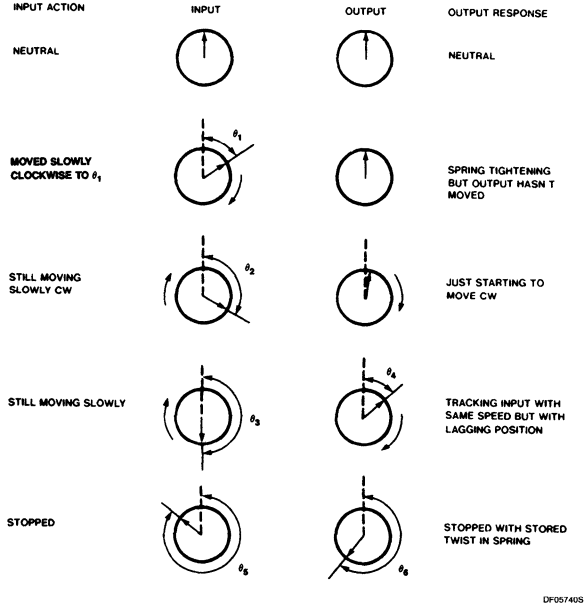


Figure 3. Disk Sequence Showing Output Tracking Input With Phase Error

Then, after some delay, the rate of the output gradually increases to track the input. Both positional markers appear to be walking around each disk at the same rate until the strobotac is adjusted for the higher input and output rate. Then the strobe light again freezes the markers, producing a phase error at this higher rate that is larger than before the input rate was increased. This gradual increase in the input rate to the mechanical system simulates a ramp change in the input frequency to the PLL system. The response to the output disk simulates the behavior of the oscillator in the PLL.

If the rate of the input disk is alternately increased and decreased by some small amount compared to the nominal revolution rate, the positional markers will appear to walk both clockwise and counter clockwise, momentarily appearing stationary when the strobing light rate equals the disk revolution rate. This "walking" represents a changing phase error which is occurring at the modulation rate. Thus the phase error can be thought of as a useable demodulated output signal.

The disk-spring mechanical system is a helpful analog for visualizing frequency, phase, transient, and steady-state responses in the electronic phase-locked loop system. In this example, the positions of the disk marker and rotation rates are analogous to phase and frequency in the electronic PLL system. The spring acts as a phase comparator to constantly sense the relative positions or phases of the disks. The torque developed in this spring acts as the driving force or input signal to turn the second disk.

Thus the spring torque simulates a voltage which controls the rate or frequency of the output disk or oscillator. Hence the second disk is analogous to a voltage-controlled oscillator (VCO). The large mass of the disks together with their angular momentum slows down the systems response time and simulates a low-pass filter in the electronic PLL system. This describes the lagging of the VCO free-running frequency to the input signal in an analog phase-locked loop.

EXAMPLES OF PLL APPLICATIONS

Now consider the action of the voltage-controlled oscillator, phase comparator and low pass filter in the PLL. The VCO generates a signal that is periodic Normally, the rate or frequency of the VCO is primarily determined by the value of a capacitance connected to this oscillator. This action of starting the VCO running by itself is analogous to disconnecting the spring from one of the shafts in the mechanical system and starting the output disk rotating at a constant rate through some external means such as a motor. In the PLL system this frequency is called the oscillator's free running frequency, (f_O'), because it occurs when the system is unlocked and there is no coupling between input and output frequencies. With the PLL, the VCO frequency can be shifted above and below f_O' by applying a voltage to the optional fine tune input.* This signal generator property is just one of the many uses of the PLL. Specifically with integrated circuit PLLs, frequency ranges from less than 1.0Hz to more than 50MHz can be produced just by selecting the right value of capacitance from a chart on the data sheet.

Selecting f_O' and then changing it by a control voltage makes the VCO well suited for converting digital data that is represented by two different voltage levels into two different frequencies. A "1" voltage level can be related to a frequency called a mark, and an "0" level to a frequency called a space. This technique, called frequency shift keying, or (FSK), is typical of data being transmitted over telephone and radio links where it is impractical to use DC voltage level shifts. Essentially this is what a modem (modulator-demodulator) does as it converts data to tones to go out of the system into a transmission link. Then it reverses the process and converts received tones to "1"s and "0"s at the receiver for the system to use. Sometimes confusion arises because different

*Some oscillators have frequencies controlled by an input current rather than a voltage and are referred to as current-controlled oscillators (CCO)

names are used for the same thing. For example,

A shift up in frequency = "1" = Mark
A shift down in frequency = "0" = Space

If voice or music is applied to the VCO instead of digital data, the oscillator's frequency will move or modulate with the voice or music. This is frequency modulation (FM) and is simply moving the frequency in relation to some input voltage which represents intelligence. Of course, as in the modem case, the process has to be reversed and the PLL can do this also. The PLL is a complete working system that can be used to send and receive signals. In fact the PLL can create the signal, or select a signal, decode it and reproduce it. Now let's look at how this works.

The VCO is connected to a section where its frequency is put together with an incoming signal or signals. In a radio this is known as a "mixer" where signals are mixed together. In a PLL it is usually called a *Phase Comparator.* Other names for this function are *phase detector* or *multiplier* — either analog or digital. (Differences between analog and digital phase comparators will be explained later in this chapter.) The purpose of this phase comparator is to produce an output which represents how far the VCO frequency is from that of the incoming signal. Comparing these frequencies and producing an error signal proportional to their difference allows the VCO frequency to shift from f_O' and become the same frequency as the input signal. This is exactly what happens with the VCO frequency — first "capturing" the input frequency, and then locking onto it. A similar type of action can be visualized in the mechanical system by having the coupling spring disconnected at one end with the two disks rotating at different rates. When their rotation rates are approximately equal, the spring is suddenly connected, and the output disk's speed will gradually become equal to and track the inputs rate as in Figure 5.

When the VCO shifts frequency and locks to the input, the signal frequency is duplicated. If the input signal contains static or noise, the VCO output will be an exact reproduction of the signal frequency without the static or noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

The error signal used to keep the VCO exactly synchronized with an incoming signal can be amplified, filtered, and used to "clock" the signal or give synchronizing information necessary to look at the signal. For example, in some digital memories and transmission systems, data are stored in a code and looked at or strobed at a rate which must be synchronized to the data. This strobing may be at twice or one-half the data rate. By setting f_O' equal to twice or one-half the data rate, the PLL will lock to the data and give an exact synchronized clock This shows another application of the PLL for multiplying or dividing frequencies.

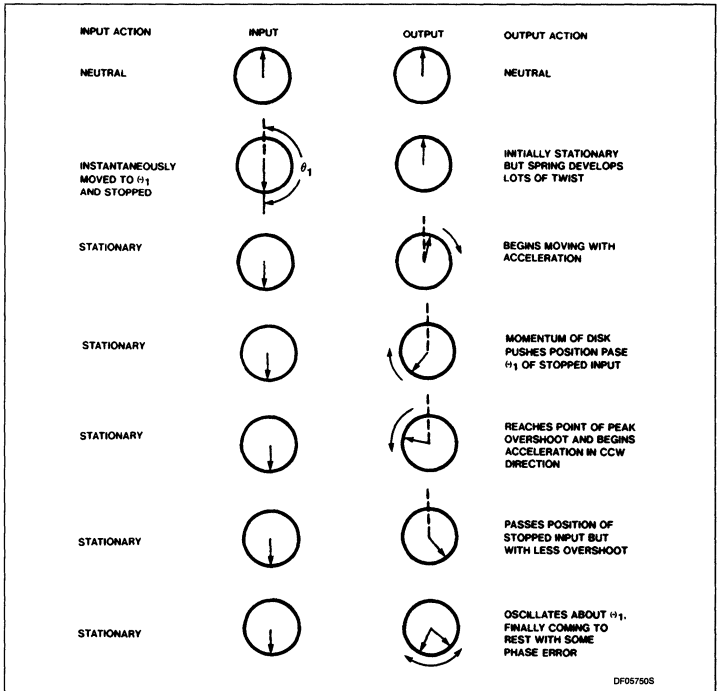


Figure 4. Disk Sequence Showing Ouput Response to a Sudden Position Input

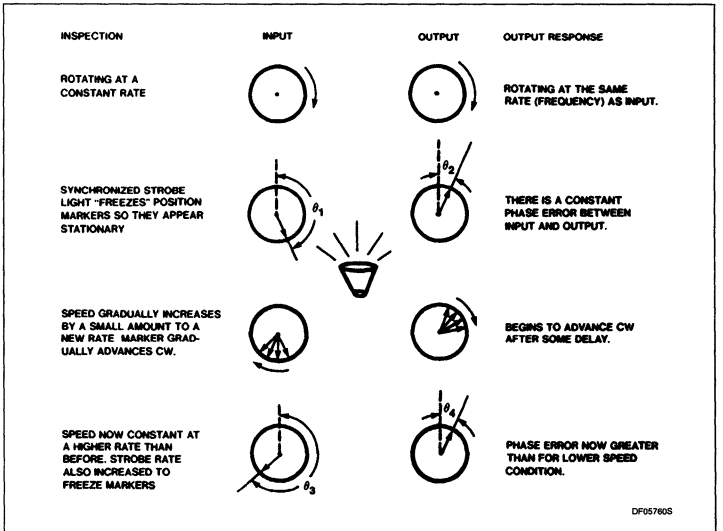


Figure 5. Disk Sequence Showing Output Behavior Due to Changes in Input Speed

An Overview of the Phase-Locked Loop (PLL) AN177

PLLs can separate a signal of one frequency from among many others as, for example, is done in television and radio reception. This selectivity or capture range is controlled in the PLL by the low-pass filter (LPF) which allows the PLL to only see signals close to the frequency of interest. The time constant of the LPF is set easily by the selection of a resistor and capacitor network. This network determines how far away in frequency an input signal can be from f_O' and still permit the PLL to respond and capture. Once locking is activated, the PLL system will continue to track the input frequency unless the instantaneous phase error exceeds the system's capability.

The error signal which drives the VCO and keeps the system locked is a usable output. In the FSK example the oscillator's frequency is shifted with each "1" or "0" digital input. Converting these frequency shifts back to the "1" and "0" signals automatically occurs in a PLL because a mark input generates an error signal to move the VCO up to that frequency. When the mark changes to a space, the error signal jumps suddenly down, forcing the VCO to follow. The error signal then is exactly the data that generated the FSK signals. *A PLL for FSK can convert data to tones for transmission to a remote point. Then another PLL can reconvert the data tones back to voltage levels, all without tuned circuits.*

The PLL system decodes FM signals in a similar way. The frequency variations caused by voltages from a microphone into one VCO serve as the input signal to another PLL, which reverses the action since the error signal driving the second PLL's VCO is exactly the same as the original microphone voltage.

Decoding of an amplitude-modulated (AM) input signal is another application of the PLL. This application is more involved than FM demodulation because a phase shift network, a second-phase comparator, and another low-pass filter are required. This application is discussed in detail later. However, it should be pointed out that AM demodulation with PLLs offers improved system linearity than the more commonly employed technique of nonlinear diode detection. Tone decoding is a special case of AM demodulation. When performed with PLLs, the second-phase comparator is called a quadrature-phase detector (QPD). The QPD produces a maximum output error voltage whenever the input and oscillator frequencies are locked to the free-running frequency, f_O', unlike the regular phase comparator which has a nominal zero error voltage under this same condition.

These application examples show that with the PLL, a system can.

1. Generate a signal
2. Modulate a signal (encode)
3. Select a signal from among many
4. Demodulate (decode)
5. Recreate (reconstitute) a signal frequency with reduced noise
6. Multiply and divide frequency

TYPES OF PLLS

Generally speaking, the monolithic PLLs can be classified into two groups — digital and analog. While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

The phase comparator is perhaps the most important part of the PLL system since it is here that the input and VCO frequencies are simultaneously compared. Some digital PLLs employ a two-input Exclusive-OR gate as the phase comparator. When the digital loop is locked to f_O', there is an inherent phase error of 90° that is represented by asymmetry in the output waveform. Also, the phase comparator's output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase comparators achieve locking by synchronizing the "edges" of the input and VCO frequency waveshapes. The phase comparator produces an error voltage that is proportional to the time difference between the edges; i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the Exclusive-OR approach. However, time jitter on the input and VCO frequencies is translated into phase error jitter that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle. This is a key consideration in PLL applications utilizing counters where waveshapes usually aren't symmetrical; i.e., 50% duty cycle. For the TTL family, it is easier to provide the edge matching function on the falling edges ("1" to "0") transition of the waveform. CMOS, I^2L, and ECL are better suited for leading edge triggering ("0" to "1").

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals. Since this mixing is true analog multiplication, the phase comparator's output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications.

Another way of distinguishing between digital and analog phase comparators is by thinking of the similarities and differences between voltage comparators and operational amplifiers. Voltage comparators are specially designed for digital applications where response time between output levels has been minimized at the expense of system linearity. Feedback is seldom used to maintain linear system relationships, with the comparator normally running open-loop. Op amps, on the other hand, are designed for a linear input-output relationship, with negative feedback being employed to further improve the system linearity.

PLL TERMINOLOGY

The following is a brief glossary of frequently encountered terms in PLL literature.

Free-running Frequency (f_O', ω_O') — Also called the *center frequency,* this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_O and ω_O which are used for the general oscillator frequency (Many references use f_O and ω_O for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context.) The appropriate units for f_O' and ω_O' are Hz and radians per second, respectively.

Lock Range ($2f_L$, $2\omega_L$)* — The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency, unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_O'. The deviations from f_O' are referred to as the *Tracking Range* or *Hold-in Range.*(See Figure 6). The tracking range is therefore one-half of the lock range.

Capture Range ($2f_C$, $2\omega_C$)** — Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_O' with the equal deviations called the *Lock-in* or

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Pull-in Ranges The capture range can never exceed the lock range.

Lock-up Time (t_L)* ** — The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter *The lock-up time is inversely proportional to the selectivity bandwidth.* Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Phase Comparator Conversion Gain (K_d) — The conversion constant relating the phase comparator's output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO Conversion Gain (K_O) — The conversion constant relating th e oscillator's frequency shift from f_O' to the applied input voltage. K_O has units of radians per second per volt (rad/sec/V). K_O is a linear function of ω_O' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_O'.

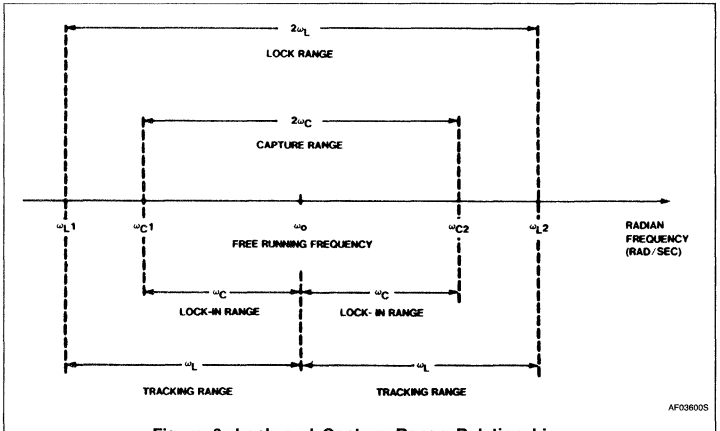

Figure 6. Lock and Capture Range Relationships

Loop Gain (K_V) — The product of K_d, K_O, and the low-pass filters gain at DC. K_d is evaluated at the appropriate input signal level and K_O at the appropriate ω_O'. K_V has units of $(sec)^{-1}$.

Closed-Loop Gain (CLG) — The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_V}{1 + K_V} \quad (4)$$

Natural Frequency (ω_n) — The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_O' and at which the phase error swing is the greatest.

Damping Factor (ζ) — The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Loop Noise Bandwidth (B_L) — A loop property relating ω_n and ζ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

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NOTES:
* Also called Synchronization Range.
** Also called Acquisition Range.
***Also called Acquisition Time

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Modeling the PLL

Application Note

Linear Products

INTRODUCTION

The phase-locked loop is a feedback system comprised of a phase comparator, a low-pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 1. Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. However, the parameters in the equations are somewhat different since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

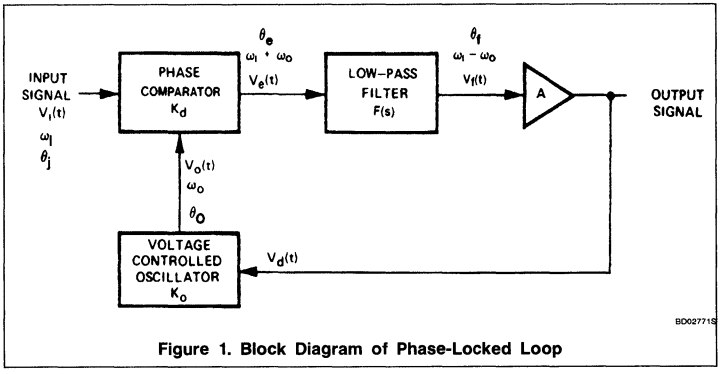


Figure 1. Block Diagram of Phase-Locked Loop

PHASE-LOCKED LOOP OPERATION

The basic principle of the PLL operation can be briefly explained as follows:

With no signal input applied to the system, the VCO control voltage $V_d(t)$ is equal to zero. The VCO operates at a set frequency, f_O' (or the equivalent radian frequency ω_O') which is known as the free-running frequency. When an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified, and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between ω_O and the input signal. If the input frequency ω_i is sufficiently close to ω_O, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of θ_e where

$$\theta_e = \theta_o - \theta_i \qquad (1)$$

is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_i and thus keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_O$ shown in Figure 1. *When the loop is in lock,* the VCO duplicates the input frequency so that the difference frequency component $(\omega_i - \omega_O)$ is zero; *hence, the output of the phase comparator contains only a DC component.* The low-pass filter removes the sum frequency component $(\omega_i + \omega_O)$ but passes the DC component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always DC, so the lock range is independent of the band edge of the low-pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. However, the difference component may fall outside the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low-pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low-pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as '*the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal*'. The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low-pass filter together with the closed-loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency-selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as '*the frequency range usually centered about the VCO initial free-running frequency over which the loop can track the input signal once lock has been achieved*'.

When the loop is in lock, the difference frequency component at the output of the phase comparator (error voltage) is DC and will always be passed by the low-pass filter. Thus, the lock range is limited by the range of

error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a DC parameter and is not affected by the band edge of the low-pass filter.

THE CAPTURE TRANSIENT

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows. Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

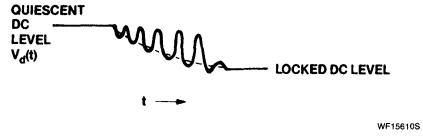
$$\Delta\omega = \frac{d\theta_e}{dt} \qquad (2)$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_e is the phase difference between the input signal and VCO signals.

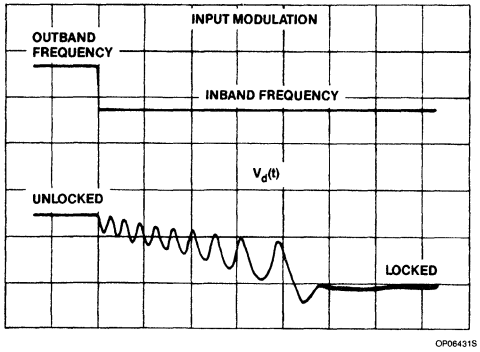
If the feedback loop of the PLL were opened between the low-pass filter and the VCO control input, then for a given condition of ω_O and ω_I the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_I and ω_O were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation.

Now suppose that the feedback loop is closed by connecting the low-pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If, during this modulation process, the VCO frequency moves closer to ω_I (i.e., decreasing $\Delta\omega$), then $\frac{d\theta_e}{dt}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_I, $\frac{d\theta_e}{dt}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 2a. Because of its asymmetry, the beat note waveform contains a finite DC component that pushes the average value of the VCO toward ω_I, and lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state DC error voltage remains.

Figure 2b displays an oscillogram of the loop error voltage $V_d(t)$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low-pass filter attenuation becomes less, and the amplitude of the beat note increases.



a. VCO Control Voltage Variation During Capture Transient



b. Oscillogram Showing a Capture Process

Figure 2. Asynchronous Error Beat Frequency During the Capture Transient

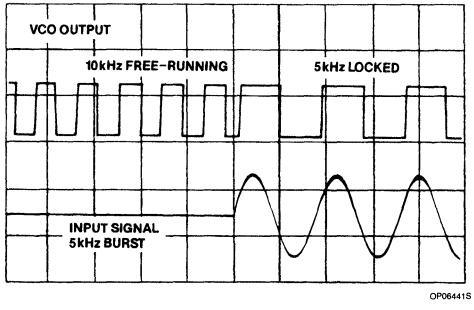


Figure 3. Exhibited by First-Order Fast Capture Transient

The total time taken by the PLL to establish lock is called *the pull-in time.* Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low-pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first-order loop (no low-pass filter) and the input tone-burst frequency was within its lock and capture range.

EFFECT OF THE LOW-PASS FILTER

In the operation of the loop, the low-pass filter serves a dual function.

First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Decreasing the low-pass filter bandwidth has the following effects on system performance (Long Time Constant):

a. The capture process becomes slower, and the pull-in time increases.

b. The capture range decreases.

c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low-pass filter.

d. The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low-pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

MATHEMATICALLY DEFINING PLL OPERATION

As mentioned previously, the phase comparator is basically an analog multiplier that forms the product of an RF input signal, $v_i(t)$, and the output signal, $v_o(t)$, from the VCO. Refer to Figure 1 and assume that the two signals to be multiplied can be described by

$$v_i(t) = V_I \sin \omega_I t \quad (3)$$

$$v_o(t) = V_O \sin (\omega_O t + \theta_e) \quad (4)$$

where ω_I, ω_O, and θ_e are the frequency and phase difference (or phase error) characteristics of interest. The product of these two signals is an output voltage given by

$$v_e(t) = K_1 V_I V_O (\sin \omega_I t)\,[\sin(\omega_O t + \theta_e)] \quad (5)$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of $v_e(t)$ is directly proportional to the amplitude of the input signal V_I. The two cases of an unlocked loop ($\omega_I \neq \omega_O$) and of a locked loop ($\omega_I = \omega_O$) are now considered separately.

Unlocked State ($\omega_I \neq \omega_O$)

When the two frequencies to the phase comparator are not synchronized, the loop is not locked. Furthermore, the phase angle difference θ_e in Equations 4 and 5 is meaningless for this case since it can be eliminated by appropriately choosing the time origin.

Using trigonometric identities, Equation 5 can be rewritten as

$$v_e(t) = \frac{K_1 V_I V_O}{2}\,[\cos(\omega_I - \omega_O)t - \cos(\omega_I + \omega_O)t] \quad (6)$$

When $v_e(t)$ is passed through the low-pass filter, F(s), the sum frequency component is removed, leaving

$$v_f(t) = K_2 V_I V_O \cos\,(\omega_I - \omega_O)t \quad (7)$$

where K_2 is a constant. After amplification, the control voltage for the VCO appears as

$$v_d(t) = A K_2 V_I V_O \cos\,(\omega_I - \omega_O)t \quad (8)$$

This equation shows that a beat frequency effect is established between ω_I and ω_O, causing the VCO's frequency to deviate by $\pm\Delta\omega$ from ω_O' in proportion to the signal amplitude ($AK_2V_IV_O$) passing through the filter. If the amplitude of V_I is sufficiently large and if signal limiting or saturation does not occur, the VCO output frequency will be shifted from ω_O' by some $\Delta\omega$ until lock is established where

$$\omega_I = \omega_O = \omega_O' \pm \Delta\omega \quad (9)$$

If lock cannot be established, then either V_I is too small to drive the VCO to produce the necessary $\pm\Delta\omega$ deviation or ω_I is beyond the dynamic range of the VCO, i.e., $\omega_I \gtrless \omega_O' \pm \Delta\omega$. Remedies for these no lock conditions are:

1. Increase V_I either internally or externally to the loop by providing additional amplification.
2. Increase the internal loop gain by adjusting upward (larger −3dB frequency) the response of the low-pass filter.
3. Shift ω_O' closer to the expected ω_I. Establishing frequency lock leads to the second case where $\omega_I = \omega_O$.

Locked State ($\omega_I = \omega_O$)

When ω_I and ω_O are frequency synchronized, the output signal from the phase comparator for $\omega_I = \omega_O = \omega$ and a phase shift of θ_e is

$$v_e(t) = K_1 V_I V_O (\sin \omega t)\,\sin(\omega t + \theta_e) = \frac{K_1 V_I V_O}{2}[\cos\theta_e - \cos\,(2\omega t + \theta_e)] \quad (10)$$

The low-pass filter removes the high frequency, AC component of $v_e(t)$, leaving only the DC component. Thus,

$$v_f(t) = K_2 V_I V_O \cos\theta_e \quad (11)$$

After amplification the DC voltage driving the VCO and maintaining lock within the loop is

$$v_d(t) = V_D = A K_2 V_I V_O \cos\theta_e \quad (12)$$

Suppose ω_I and ω_O are perfectly synchronized to the free-running frequency ω_O'. For this case, V_D will be zero, indicating that θ_e must be ±90°. Thus V_D is proportional to the phase difference or phase error between θ_I and θ_o centered about a reference phase angle of ±90°. If ω_I changes slightly from ω_O', the first effect will be a change in θ_e from ±90°. V_D will adjust and settle out to some nonzero value to correct ω_O; under this condition frequency lock is maintained with $\omega_I = \omega_O$. The phase error will be shifted by some amount $\Delta\theta$ from the reference phase angle of ±90°. This concept can be simplified by redefining θ_e as

$$\theta_e = \theta_r \pm \Delta\theta \quad (13)$$

where θ_r is the inherent, reference phase shift of ±90° and $\Delta\theta$ is the departure from this reference value. Now the VCO control voltage becomes

$$V_D = A K_2 V_I V_O \cos\,(\theta_r \pm \Delta\theta) = \pm A K_2 V_I V_O \sin\Delta\theta \quad (14)$$

Since the sine function is odd, a momentary change in $\Delta\theta$ contains information about which way to adjust the VCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta\theta$ changes can be tracked is −90° to +90°. This corresponds to a θ_e range from 0 to 180°.

In addition to being an error signal, V_D represents the demodulated output of an FM input applied as $v_{in}(t)$ assuming a linear VCO characteristic. Thus, FM demodulation can be accomplished with the PLL without the inductively-tuned circuits that are employed with conventional detectors.

DETERMINING PLL MODEL PARAMETERS

Since the PLL is basically an electronic servo loop, many of the analytical techniques developed for control systems are applicable to phase-locked systems. Whenever phase lock is established between $v_i(t)$ and $v_o(t)$ the linear model of Figure 4 can be used to predict the performance of the PLL system. Here θ_i and θ_o represent the phase angles associated with the input/output waveshapes, respectively; F(s) represents a generalized voltage transfer function for the low-pass filter in the s complex frequency domain; and K_d and K_o are conversion gains of the phase comparator and VCO, respectively, each having units as shown. The 1/s term associated with the VCO accounts for the inherent 90° phase shift in the loop since the VCO converts a voltage to a frequency and

since phase is the integral of frequency Thus the VCO functions as an integrator in the feedback loop.

Specific values of K_d and K_o for all of Signetics' general purpose PLLs can be found in the sections describing the particular loop of interest. However, sometimes it may be desired to determine these conversion gains exactly for a specific device The measurement scheme shown in Figure 5 can be used to determine K_d and K_o for a loop under lock. The function of the Khron-Hite filters is to extract the fundamental sinusoidal frequency component of their square wave inputs for application to the Gain-Phase Meter If the input signal from the Function Generator is sinusoidal, then the first Khron-Hite filter may be eliminated. It is recommended to use high impedance oscilloscope probes so as to not distort the input of VCO waveshapes, thereby potentially altering their phase relationships. The frequency counter can be driven from the scope as shown, or connected directly to the input or VCO, provided its input impedance is large

The procedure to follow for obtaining K_d and K_o is as follows:

1 Establish the desired external bias and gain conditions for the PLL under test.

2 With the Function Generator turned off, set the free-running frequency of the loop via the timing capacitor and timing resistor if appropriate Monitor f_O' with the Frequency Counter.

3. Turn on the Function Generator and check to make sure the amplitude of the input signal is appropriate for the particular loop under test.

4. Adjust the input frequency for lock. Lock is discernable on a dual-trace scope when the input and VCO waveforms are synchronized and stationary with respect to each other. One should be especially careful to check that locking has not occurred between the VCO and some harmonic frequency. Carefully inspect both waveshapes, making sure each has the same period. (If a second Frequency Counter is available, an alternate scheme can be used to confirm frequency locking. One frequency counter is used to monitor the input signal frequency, and the second counter is used for the VCO frequency. When the two counters display the same frequency, the PLL is locked.)

5. Set the input frequency to the free-running frequency and note the Gain-Phase Meter display It should be approximately 90°± 10°nominally. Record the phase error, θ_e, the VCO control voltage, V_D, and the input frequency, f_I.

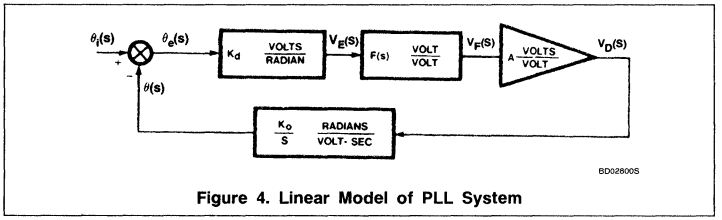


Figure 4. Linear Model of PLL System

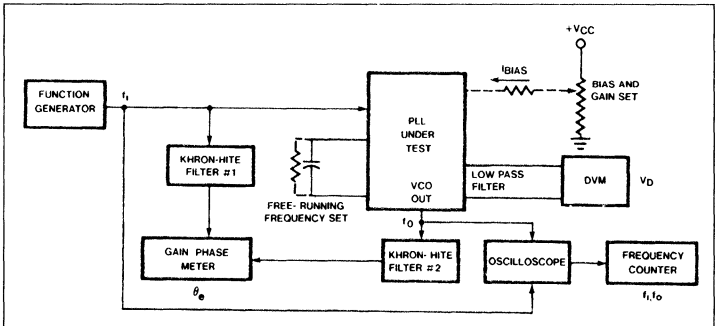


Figure 5. Measurement Scheme for K_d and K_o Determinations

6. Adjust f_I for frequencies above and below f_O' and record θ_e and V_D for each f_I, as appropriate.

7. Making a plot of V_D versus θ_e is useful for checking the measurement data and the system's linearity The slope of this plot ($\Delta V_D/\Delta\theta_e$) is K_d in units of V/°. Multiplying this slope by $180/\pi$ gives the desired K_d in volts/radian.

8. A plot of $f_I = f_O$ versus V_D while the loop remains locked will check the VCO linearity. The slope of this plot is K_o at the particular free-running frequency. The units of slope taken directly from the graph are Hz/V. Multiplying this slope figure by 2π gives the desired K_o in units of radians/volt-sec.

K_d is generally constant over wide frequency ranges, but is linearly related to the input signal amplitude. K_o is constant with input signal level but does vary linearly with f_O'. Often it is convenient to specify a normalized K_o as

$$K_{O(norm)} = \frac{K_O}{f_O'}\ \frac{rad}{V} \qquad (15)$$

The K_o value at any desired free-running frequency then can be estimated as

$$K_o\ (@\ any\ f_O') = K_{O(norm)} f_O' \qquad (16)$$

The loop gain for the PLL system is

$$K_v = K_d K_o A \qquad (17)$$

(Often when the gain A is due to an amplifier internal to the IC, A will be included in either K_d or K_o This is further illustrated in the article on the 565 PLL.)

MODELING THE PLL SYSTEM WITH VARIOUS LOW-PASS FILTERS

The open-loop transfer function for the PLL is

$$T(s) = \frac{K_V F(s)}{s} \qquad (18)$$

Using linear feedback analysis techniques, and assuming that the VCO is in the forward path, the closed-loop transfer characteristics H(s) can be related to the open-loop performance as

$$H(s) = \frac{T(s)}{1 + T(s)} \qquad (19)$$

and the roots of the characteristic system polynomial can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

Zero-Order Filter — F(s) = 1

The simplest case is that of the first-order loop where F(s) = 1 (no filter). The closed-loop transfer function then becomes

$$T(s) = \frac{K_V}{S + K_V} \quad (20)$$

This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 6a. The open-loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency-modulated input signal. Since there is no low-pass filter in this case, sum frequency components are also present at the phase comparator output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

First-Order Filter

With the addition of a single-pole low-pass filter F(s) of the form

$$F(s) = \frac{1}{1 + \tau_1 s} \quad (21)$$

where $\tau_1 = R_1C_1$, the PLL becomes a second-order system with the root locus shown in Figure 6b. Again, an open-loop pole is located at the origin because of the integrating action of the VCO. Another open-loop pole is positioned on the real axis at $-1/\tau_1$ where τ_1 is the time constant of the low-pass filter.

One can make the following observations from the root locus characteristics of Figure 6b:

a. As the loop gain K_V increases for a given choice of τ_1, the imaginary part of the closed-loop poles increases: thus, the natural frequency of the loop increases and the loop becomes more and more underdamped.

b. If the filter time constant is increased, the real part of the closed-loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 6b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

First-Order Lag-Lead Filter

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 6c. This type of a filter has the transfer function

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s} \quad (22)$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. By proper choice of R_2, this type of filter confines the root locus to the left half-plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first- and second-order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second-order loop and as $R_2 \rightarrow \infty$, the loop behaves as a first-order loop due to a pole-zero cancellation. However, as first-order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

Second- and Higher-Order Filters

Second- and higher-order filters, as well as active filters, occasionally are designed and incorporated within the PLL to achieve a particular response not possible or easily obtained with zero- or first-order filters. Adding more poles and more gain to the closed-loop transfer function reduces the inherent stability of the loop. Thus the designer must exercise extreme care and utilize complex stability analysis if second-order (and higher) filters or active filters are to be considered.

CALCULATING LOCK AND CAPTURE RANGES

In terms of the basic gain expression in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the DC loop gain (2-sided lock range).

$$2\omega_L = 4\pi f_L = K_V F(0) \quad (23)$$

where F(0) is the value of the low-pass filters transfer function at DC.

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as (2-sided capture range).

$$2\omega_C = 4\pi f_C \simeq K_V |F(i\omega_C)| \quad (24)$$

where $F(i\omega_C)$ is the magnitude of the low-pass filter transfer function evaluated at ω_C. Solution of Equation 24 frequently involves a "trial and error" process since the capture range is a function of itself. *Note that at all times the capture range is smaller than the lock range.* For the simple first-order lag filter of Figure 6b, the capture range can be approximated as

$$2\omega_C \simeq 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_V}{\tau_1}} \quad (25)$$

This approximation is valid for

$$\tau_1 > > \frac{1}{2\omega_L} \quad (26)$$

Equations 23 and 24 show that the capture range increases as the low-pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 7 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 7a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO conversion gain ($1/K_o$) and goes through zero as $\omega_i = \omega_O'$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back, the cycle repeats itself, but is inverted, as shown in Figure 7b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

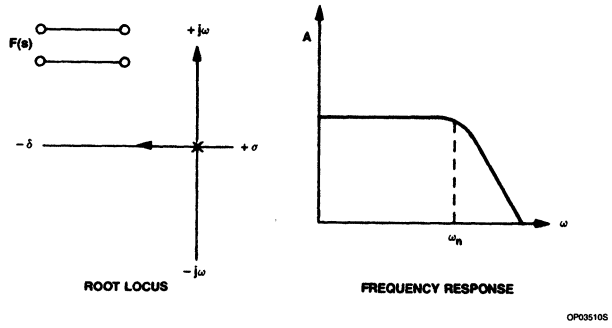
$$2\omega_C = \omega_3 - \omega_1 \quad (27)$$

and

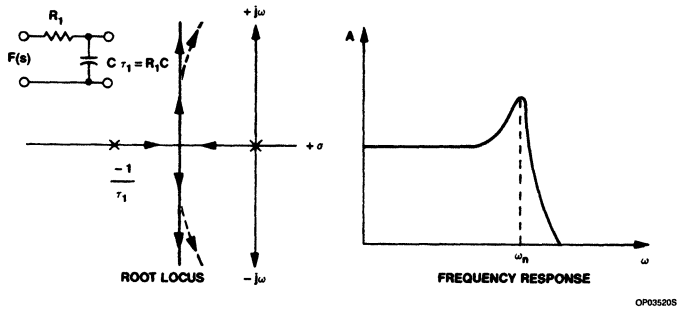
$$2\omega_L = \omega_2 - \omega_4 \quad (28)$$

Note that, as indicated by the transfer characteristics of Figure 7, the PLL system has an inherent selectivity about the free-running frequency, ω_O'. It will respond only to the input signal frequencies that are separated from ω_O' by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

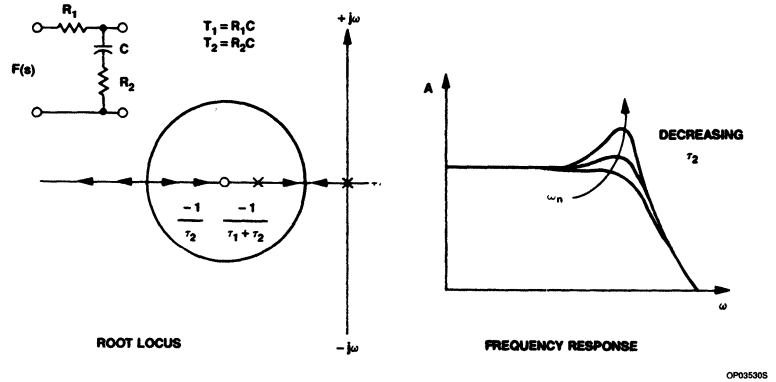
4



a. Zero-Order Filter



b. First-Order Simple Lag Filter



c. First-Order Lag-Lead Filter

Figure 6. Root Locus and Frequency Response Plots

DETERMINING LOOP RESPONSE

The transient response of a PLL can be calculated using the model of Figure 4 and Equations 18 and 19 as starting points. Combining these equations gives

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_V F(s)}{s + K_V F(s)} \quad (29)$$

The phase error which keeps the system in lock is

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \quad (30)$$

Define a phase error transfer function

$$E(s) = \frac{\theta_e(s)}{\theta_i(s)} = 1 - \frac{\theta_o(s)}{\theta_i(s)}$$

$$= 1 - H(s) \quad (31)$$

As an example of the utilization of these equations, consider the most common case of a loop employing a simple first-order lag filter where

$$F(s) = \frac{1}{1 + s\tau_1} \quad (32)$$

For this filter, Equations 29 and 31 become

$$H(s) = \frac{K_V/\tau_1}{s^2 + s/\tau_1 + K_V/\pi_1} \quad (33)$$

$$E(s) = \frac{s(s + 1/\tau_1)}{s^2 + s/\tau_1 + K_V/\tau_1} \quad (34)$$

Both equations are second-order and have the same denominator which can be expressed as

$$D(s) = s^2 + s/\tau_1 + K_V/\tau_1$$
$$= s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (35)$$

Where ω_n and ζ are, respectively, the system's undamped natural frequency and damping factor defined as

$$\omega_n = \sqrt{K_V/\tau_1} \quad (36)$$

$$\zeta = \frac{1}{2\sqrt{K_V\tau_1}} = \frac{\omega_n}{2K_V} \quad (37)$$

The system is considered overdamped for $\zeta > 1.0$, and critically damped $\zeta = 1.0$. Now examine this PLL system's response to various types of inputs.

Step-of-Phase Input

Consider a unit step-of-phase as the input signal. This input is shown in Figure 8 and can be thought of as simply shifting the time axis by a unit step (one radian or one degree, depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_i(s) = \frac{1}{s} \quad (38)$$

The phase of VCO output and the system's phase error are represented by

$$\theta_o(s) = \frac{H(s)}{s} = \frac{\omega_n^2}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (39)$$

$$\theta_e(s) = \frac{E(s)}{s} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (40)$$

(depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_o(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin\left(\omega_n t\sqrt{1-\zeta^2} + \Psi\right) \quad (41)$$

where $\Psi = \arctan\frac{\sqrt{1-\zeta^2}}{\zeta}$ (42)

and $\zeta \neq 1$.

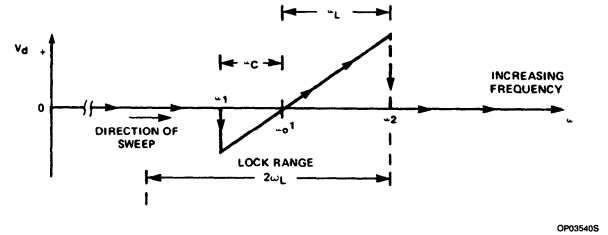
$$\theta_e(t) = \frac{e^{-\zeta\omega_n(t)}}{\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi) \quad (43)$$

When $\zeta = 1$, these phase responses are

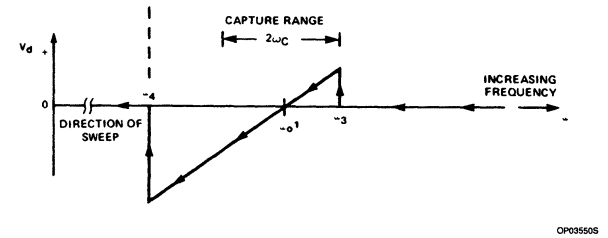
$$\theta_o(t) = 1 - (1 - \omega_n t)e^{-\omega_n t} \quad (44)$$

and

$$\theta_e(t) = (1 + \omega_n t)e^{-\omega_n t} \quad (45)$$



a. Input Frequency Increasing



b. Decreasing Input Frequency

Figure 7. Typical PLL Frequency-to-Voltage Transfer Characteristics

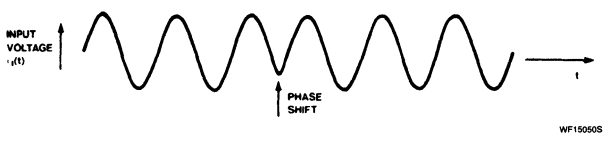


Figure 8. Input Signal Representing a Unit Step of Phase at Constant Frequency

Figure 9 is a plot of the VCO phase response and the phase error transient for various damping factors. Note from this figure that an underdamped system has overshoot which can cause the loop to break lock if this overshoot is too large. The critical condition for maintaining lock is to keep the phase error within the dynamic range for the phase comparator of $-\pi/2$ to $\pi 2$ radians. For the underdamped case, the peak phase-error overshoot is

$$\theta_e(max) = e - \zeta\pi/> \sqrt{1-\zeta^2} \quad (46)$$

which must be less than $\pi/2$ to maintain lock. Lock can also be broken for the overdamped and critically-damped loops if the input phase shift is too large where the phase error exceeds $\pm\pi/2$ radians.

The analysis and equations given are based upon the small-signal model of Figure 4. If the signal amplitudes become too large, one or more functional blocks in the system can saturate, causing a slew rate type limiting action that may break lock.

The *transient change* in the VCO frequency due to the unit step-of-phase input can be found by taking the time derivative of Equation 41 or alternatively by finding the inverse Laplace transform of

$$\omega_o(s) = s\theta_o(s) = \frac{\omega_n{}^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \quad (47)$$

which is

$$\omega_O(t) = \frac{\omega_n e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin \omega_n t \sqrt{1-\zeta^2} \quad (48)$$

Unit Step-of-Frequency Input

This type of input occurs when the input frequency is instantaneously changed from one frequency to another as is done in FSK and modem applications. For this input, as shown in Figure 10,

$$\theta_i(s) = \frac{1}{s^2} \quad (49)$$

The VCO output phase is

$$\theta_o(s) = \frac{\omega_n{}^2}{s^2(s^2 + 2\zeta\omega_n s + \omega_n{}^2)} \quad (50)$$

The transient time expression for the VCO *phase change* is

$$\theta_o(t) = t - \frac{2\zeta}{\omega_n} + \frac{e^{-\zeta\omega_n t}}{\omega_n\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + 2\Psi) \quad (51)$$

for $\zeta \neq 1$.

The time expression for the VCO *frequency change* for a unit step-of-frequency input is the same as the time response VCO phase change due to a step-of-phase input (Equation 41), or

$\omega_O(t)$ for frequency step input = $\theta_o(t)$ for phase step input Thus

$$\omega_O(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n t \sqrt{1-\zeta^2} + \Psi) \quad (52)$$

for $\zeta \neq 1$.

Unit Ramp-of-Frequency Input

This form of input signal represents sweeping the input frequency at a constant rate and direction as shown in Figure 11. The amplitude and phase of the input remain constant; the input frequency changes linearly with time Since the input signal to the PLL model is a phase, a unit ramp-of-frequency appears as a phase acceleration type input that can be mathematically described as

$$\theta_i(s) = \frac{1}{s^3} \quad (53)$$

The VCO output phase change is

$$\theta_o(s) = \frac{\omega_n{}^2}{s^3(s^2 + 2\zeta\omega_n s + \omega_n{}^2)} \quad (54)$$

The time expression for the VCO phase change is

$$\theta_o(t) = \frac{t^2}{2} - \frac{2\zeta t}{\omega_n} + \frac{2\zeta}{\omega_n{}^2}\left[2\zeta(1-\omega_n{}^2) + \left(\frac{1-4\zeta^2\omega_n{}^2+4\zeta^2\omega_n{}^4}{1-\zeta^2}\right)^{1/2} \times e^{-\zeta\omega_n t} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi')\right] \quad (55)$$

where $\Psi = \text{arc tan}\dfrac{\sqrt{1-\zeta^2}}{\zeta(1-2\omega_n{}^2)} + \Psi$

and Ψ is given in Equation 42.

PLL BUILDING BLOCKS

VCO

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_O (in radian/V-sec)

$$K_O = \frac{\Delta\omega_O}{\Delta V_d} \quad (56)$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_d = \frac{\Delta\omega_O}{K_O} \quad (57)$$

The gain K_O can be found from the data sheet. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Comparator

All of Signetics' analog phase-locked loops use the same form of phase comparator — often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 12.

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has an equivalent collector resistance R_C and whose differential gain at balance is the ratio of R_C to the dynamic emitter resistance, r_e, of Q1 and Q2.

$$A_d = \frac{R_C}{r_e} = \frac{\frac{R_C}{0.026}}{I_E/2} = \frac{R_C I_E}{0.052} \quad (58)$$

where I_E is the total DC bias current for the differential amplifier pair.

The switching stage formed by Q3 – Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by –1. That is, when the base of Q4 is positive, R_{C2} receives I_1 and when the base of Q6 is positive, R_{C2} receives $i_2 = i_1$. Since the circuit is called a multiplier, performing the multiplication will gain further insight into the action of the phase comparator.

Consider an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

$$v_i(t) + v_k(t) = V_i\sin(\omega_i t + \theta_i) + v_k\sin(\omega_k t + \theta_k) \quad (59)$$

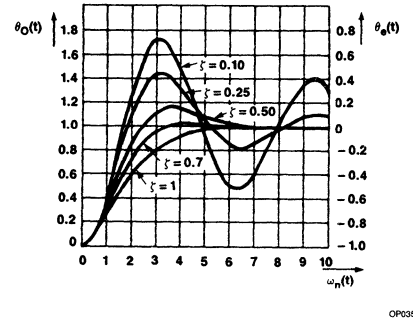


Figure 9. VCO Phase and Loop Phase Error Transient Responses for Various Damping Factors

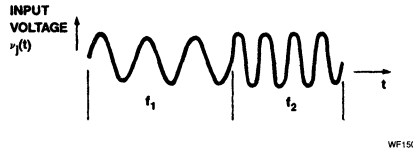


Figure 10. Input Signal for a Unit Step-of-Frequency at Constant Phase

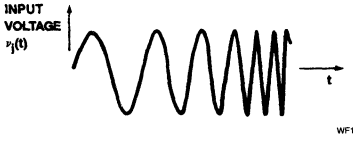


Figure 11. Input Signal for a Unit Ramp-of-Frequency Input

where θ_I and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$v_o(t) = \sum_{n=0}^{\infty} \frac{4}{\pi(2n+1)} \sin[(2n+1)\omega_O t] \quad (60)$$

where ω_O is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationships, and inserting the differential stage gain A_d gives:

$$v_e(t) = \frac{2A_d}{\pi} \left[\sum_{n=0}^{\infty} \frac{V_I}{(2n+1)} \cos[(2n+1)\omega_O t - \omega_I t - \theta_I] - \sum_{n=0}^{\infty} \frac{V_I}{(2n+1)} \cos[(2n+1)\omega_O t + \omega_I t + \theta_I] + \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos[(2n+1)\omega_O t - \omega_k t - \theta_k] - \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos[(2n+1)\omega_O t + \omega_k t + \theta_k] \right] \quad (61)$$

Assuming that temporarily V_k is zero, if ω_1 is close to ω_O, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock-up by modulating the VCO. As ω_O is driven closer to ω_I, this difference component becomes lower and lower in frequency until $\omega_O = \omega_I$ and lock is achieved. The first term then becomes

$$v_e(t) = V_E = \frac{2A_d V_I}{\pi} \cos\theta_I \quad (62)$$

which is the usual phase comparator formula showing the DC component of the phase comparator during lock. This component must equal the voltage necessary to keep the VCO at ω_O. It is possible for ω_O to equal ω_I momentarily during the lock-up process and, yet, for the phase to be incorrect so that ω_O passes through ω_I without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_I = \omega_O$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_I = (2n+1)\omega_O$, giving the DC phase comparator component

$$V_e(t) = V_E = \frac{2A_d V_I}{\pi(2n+1)} \cos\theta_I \quad (63)$$

showing that the loop can lock to odd harmonics of the free-running frequency. The (2n + 1) term in the denominator shows that the phase comparator's output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase comparator's output during lock is (assuming A_d is constant) also a function of the input amplitude V_I. Thus, for a given DC phase comparator output V_E, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_I between 0 and 180°, the lower V_I becomes, the more the lock range is reduced.

Note from the second term that during lock the lowest possible frequency is $\omega_O + \omega_I = 2\omega_I$. A sum frequency component is always present at the phase comparator output. This component is usually greatly attenuated by the low-pass filter capacitor connected to the phase comparator output. However, when rapid tracking is required (as with high-speed FM detection or FSK), the requirement for a relatively high frequency cutoff in the low-pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

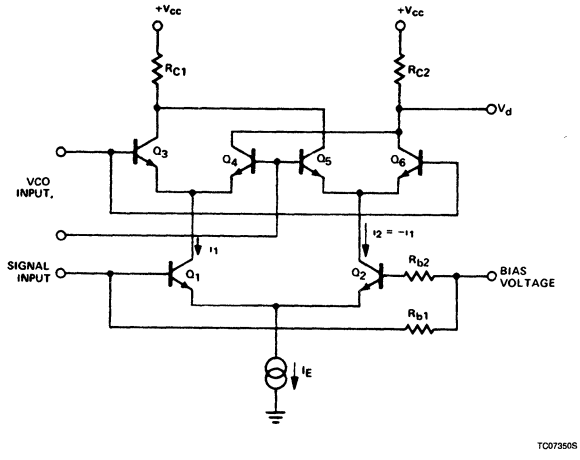


Figure 12. Integrated Phase Comparator Circuit

Suppose that other frequencies represented by V_k are present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_I, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. However, suppose lock has been achieved so that $\omega_O = \omega_I$. In order for lock to be maintained, the average phase comparator output must be constant. If $\omega_O = \omega_k$ is relatively low in frequency, the phase θ_I must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_I. However, it has been stated that the phase θ_I can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. This effect can be reduced by decreasing the cutoff frequency of the low-pass filter so that the $\omega_O - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_O - \omega_I$ is likewise attenuated) when the low-pass filter capacitor is large.

The third term can have a DC component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)(\omega_O - \omega_I)$ is zero and θ_k makes its appearance. This will have an effect on θ_1 which will change the θ_1 versus frequency ω_1. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_I term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_I is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase comparator output will have a component at the locked frequency ω_O at the output. For example, a DC offset at the input differential stage will appear as a square wave of fundamental ω_O at the phase comparator output. This is usually small and well attenuated by the low-pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, only those close to the locked frequency need be considered.

Quadrature-Phase Detector (QPD)

The quadrature-phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_I is 90°, the quadrature-phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature-phase detector is given by

$$V_q = \frac{2A_qV_I}{\pi} \sin \theta_I \qquad (64)$$

where V_I is the constant or modulated AM signal and $\theta_I \approx 90°$ in most cases so that sine $\theta_I = 1$ and

$$V_q = \frac{2A_qV_I}{\pi} \qquad (65)$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

INITIAL PLL SETUP CHOICES

In a given application, maximum PLL effectiveness can be achieved if the designer understands the tradeoffs which can be made. Generally speaking, the designer is free to select the frequency, lock range, capture range, and input amplitude.

FREE-RUNNING FREQUENCY SELECTION

Setting the center or free-running frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming frequency so that the tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow-band operation (reduced tracking speed).

All of Signetics' loops use a phase comparator in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range, however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase comparator discussion would suggest that the PLL cannot lock to subharmonics because the phase comparator cannot produce a DC component if ω_I is less than ω_O.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at ω_O For example, a square wave of fundamental $\omega_O/3$ will have a substantial component at ω_O to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven. (The resultant internal limiting generates harmonic frequencies.) Locking to even harmonics or subharmonics is the least satisfactory, since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial, even harmonic, content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest ω_O. This magnitude can be used to estimate the capture and lock ranges

All of Signetics' loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature-compensated over the entire military temperature range (−55 to +125°C) To benefit from this inherent stability, however, the designer must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the designer may wish to trade some stability for lower cost external components.

GUIDELINES FOR LOCK RANGE CONTROL

Two things limit the lock range. First, any VCO can swing only so far; it the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase comparator is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. The 564 contains an internal limiter circuit between the signal input and one input to the phase comparator. This circuit limits the amplitude of large input signals such as those from TTL outputs to approximately 100mV before they are applied to the phase comparator. The limiter significantly improves the AM rejection of the PLL for input signal amplitudes greater than 100mV.

This happens so often with low input amplitudes that even the full ± 90° phase range of the phase comparator cannot generate enough voltage to allow tracking wide deviations When this occurs, the effective lock range is reduced Weak input signals cause a reduction of tracking capability and greater phase errors Conversely, a strong input signal will allow the use of the entire VCO swing capability and keeps the VCO phase (referred to the input signal) very close to 90° throughout the range Note that the lock range does not depend on the low-pass filter. However, if a low-pass filter *is* in the loop, it will have the effect of limiting the maximum rate at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained When tracking at this rate, the phase difference is at its limit of 0° or 180° It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that the output contains a significant and often bothersome signal at twice the input frequency. The phase comparator's output contains both sum and difference frequencies During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present. This sum frequency component can then be filtered out with an external low-pass filter.

INPUT LEVEL AMPLITUDE SELECTION

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the lock and capture ranges become independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold, since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase comparator gain and will result in a lock range which becomes constant with amplitude as the phase comparator gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

CAPTURE RANGE CONTROL

There are two main reasons for making the low-pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase comparator's output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase comparator to drive the VCO towards the input frequency

If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speeds

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a. Input phase

b. Low-pass filter characteristic

c. Loop damping

d. Deviation of input frequency from center frequency

e. In-band input amplitude

f. Out-band signals and noise

g. Center frequency

Fortunately, it is usually sufficient to know how to improve the lock-up time and what must be sacrificed to get faster lock-up. Consider an operational loop or tone decoder where occasionally the lock-up transient is too long. What can be done to improve the situation — keeping in mind the factors that influence lock?

a. Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the

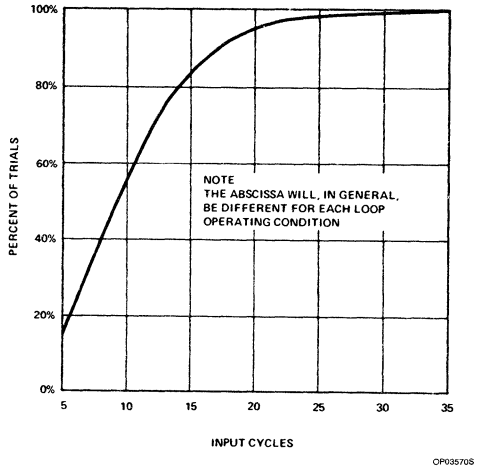


Figure 13. Probability of Lock vs Input Cycles

VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of a pulse train and the transmitted tone phase related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b. Low-pass filter — The larger the low-pass filter time constant, the longer will be the lock-up time. The lock-up time can be reduced by decreasing the filter time constant, but in doing so, some of the noise immunity and out-band signal rejection will be sacrificed. This is unfortunate, since this is what necessitated the use of a large filter in the first place. Also present will be a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low-pass capacitor automatically increases the bandwidth. Speed is gained only at the expense of added bandwidth.

c. Loop damping — A simple first-order low-pass filter of the form

$$F(s) = \frac{1}{1 + s\tau} \quad (66)$$

produces a loop damping of

$$\zeta = \tfrac{1}{2}\sqrt{\frac{1}{\pi K_V}} \quad (67)$$

Damping can be increased not only by reducing π, as discussed above, but also by reducing the loop gain K_V. Using the loop gain reduction to control bandwidth or capture and lock ranges achieves better damping for narrow bandwidth operation. The penalty for this damping is that more phase comparator output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d. Input frequency deviation from free-running frequency — Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low-pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e. In-band input amplitude — Since input amplitude is one factor in the phase comparator's gain K_d, and since K_d is a factor in the loop gain K_V damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low-pass capacitor can charge with the reduced phase comparator output (see d above).

f. Out-band signals and noise — Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g. Center frequency — Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies, on the average, will be detected before the lower frequencies.

However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with measurements of PLL operation. The techniques suggested are meant to help the designer in evaluating the performance of the PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the test equipment may be limited, techniques are described which require a minimum of standard test items.

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low-pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to DC, the calibration may be done in steps. Moreover, loop measurements may be made by applying a constant frequency to the loop input and the modulating signal to the low-pass filter terminal to simulate the effect of a FM input so that an FM generator may be omitted for many measurements.

FREE-RUNNING FREQUENCY

Free-running frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the

loop. The loop should be connected in its final configuration with the chosen values of input, bypass, and low-pass filter capacitors. No input signal should be present. As the free-running frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor, unless the capacity added by the measurement probe is much less than the timing capacitor value, since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a DC voltage for production readout or automated testing, a calibrated phase-locked loop can be used as a frequency meter.

CAPTURE AND LOCK RANGES

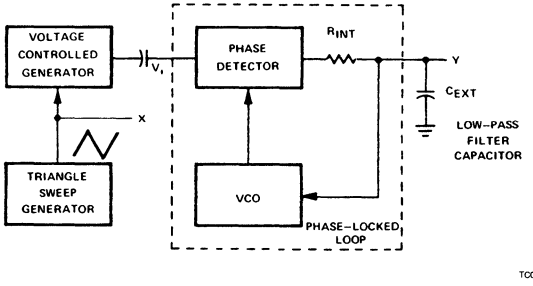
Figure 14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 14b shows the type of trace which results. The lock range is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the conversion gain K_o for the VCO at the particular free-running frequency.

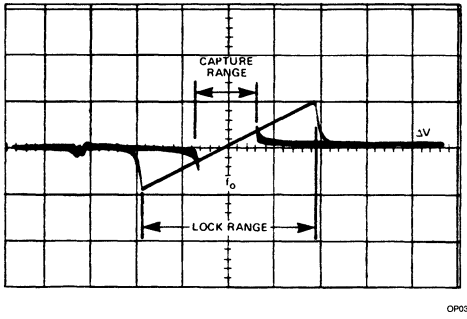
By using the sweep technique, the effect on free-running frequency, capture range, and lock range of the input amplitude, supply voltage, low-pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be much lower than the free-running frequency, especially when the capture range is below 10% of the free-running frequency. Otherwise, the *apparent* capture and lock range will be functions of sweep frequency. It is best to start sweeping as slowly as possible and, if desired, increase the rate until the capture range begins to show an apparent reduction — indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the free-running frequency. In the case of the 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 15, showing the output level versus frequency for one value of input amplitude.

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop



a. Measurement Setup



b. Oscilloscope Display

Figure 14. Capture and Lock Ranges

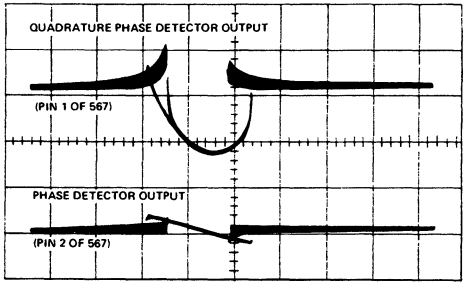


Figure 15. Quadrature-Phase Detector and Phase Comparator Outputs of the NE567 PLL

VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the DC voltage at the low-pass filter, or the AC beat frequency components at the low-pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straight-forward. The loop is simply set up for FM detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP333A) can be used to measure distortion at the FM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase comparator output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured.

NATURAL FREQUENCY AND DAMPING

Circuits and mathematical expressions for the natural frequencies and dampings are given in Figure 16 for two first-order low-pass filters. Because of the integrator action of the PLL in converting frequency to phase, the order of the loop always will be one greater than the order of the LPF. Hence, both these first-order LPFs produce a second-order PLL system.

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency-modulated signal of the desired amplitude to the loop. Figure 16 shows that the natural frequency is a function of K_d, which is, in turn, a function of input amplitude. As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $\omega_m = \omega_n$ and the output amplitude will peak.

Damping is a function of K_d, K_o, and the low-pass filter. Since K_o and K_d are functions of the free-running frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency-modulated within the lock range by a square wave. The low-pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 17. Figure 18 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 19, which gives the transient phase error due to a step in input frequency.

An expression for calculating the damping for any underdamped second-order system ($\zeta < 1.0$) when the normalized peak overshoot is known is

$$M_p = 1 + e^{-\zeta\pi/\sqrt{1-\zeta^2}} \qquad (68)$$

Examination of Figure 18 shows that the normalized peak overshoot of the error voltage is approximately 1.4. Using this value for M_p in Equation 68 gives a damping of $\zeta \cong 0.28$.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB down point will give the damping. Figure 19 tabulates some approximate relationships.

NOISE

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise

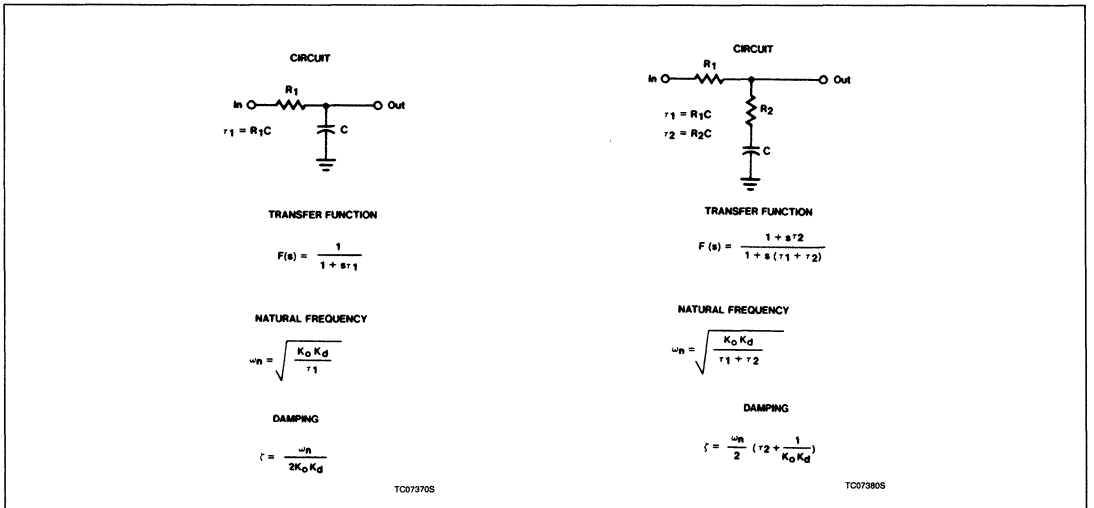


Figure 16. First-Order Low-Pass Filters

components near the center frequency are converted to phase noise. When the phase noise becomes so great that the ±90° permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

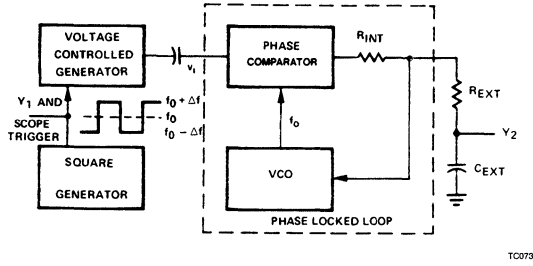
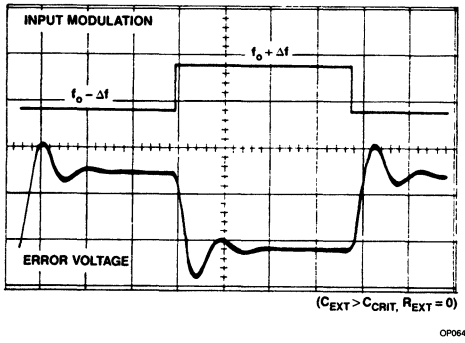
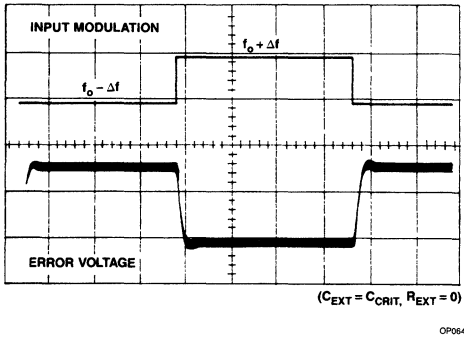


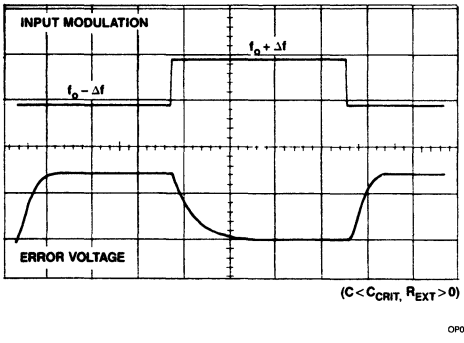
Figure 17. Measurement Setup for Display of PLL Transient Response



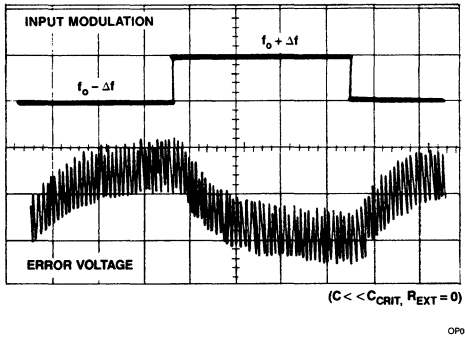
a. Underdamped With $\zeta \simeq 0.28$



b. Critically Damped With $\zeta \simeq 1.0$

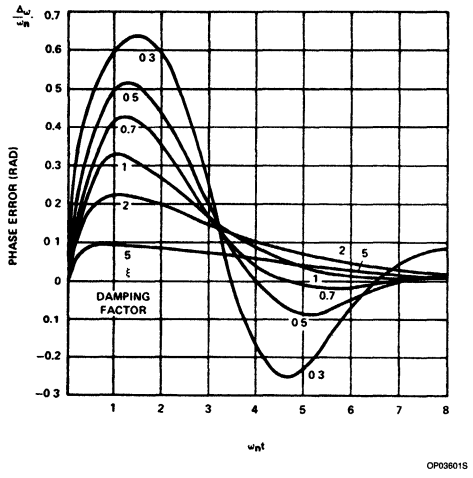


c. Overdamped With $\zeta \simeq 10$



d. Highly Overdamped With $\zeta > 10$

Figure 18. Transient Response of PLL Error Voltage to Square Wave Frequency Modulation for Various Damping Conditions



a. Transient Phase Error as an Indication of Damping

ζ	PEAK AMPLITUDE / LOW FREQUENCY AMPLITUDE	$\omega - 3dB$ / ω_n
0.3	6.0dB	1.8
0.5	3.2dB	2.1
0.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	0.5dB	10

b. Ratio of Peak Amplitude to Low Frequency Amplitude of Error Voltage From Modulating Frequency Response

Figure 19. Estimating the Damping in a Second-Order PLL

Signetics

NE/SE564
Phase-Locked Loop

Product Specification

Linear Products

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

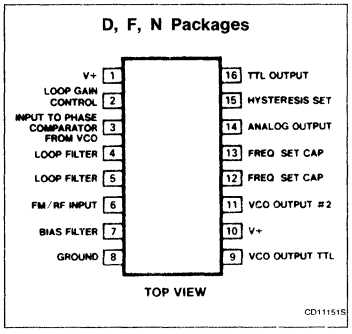
FEATURES

- **Operation with single 5V supply**
- **TTL-compatible inputs and outputs**
- **Guaranteed operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (externally controlled)**

APPLICATIONS

- **High-speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**
- **Various satcom/TV systems**

PIN CONFIGURATION

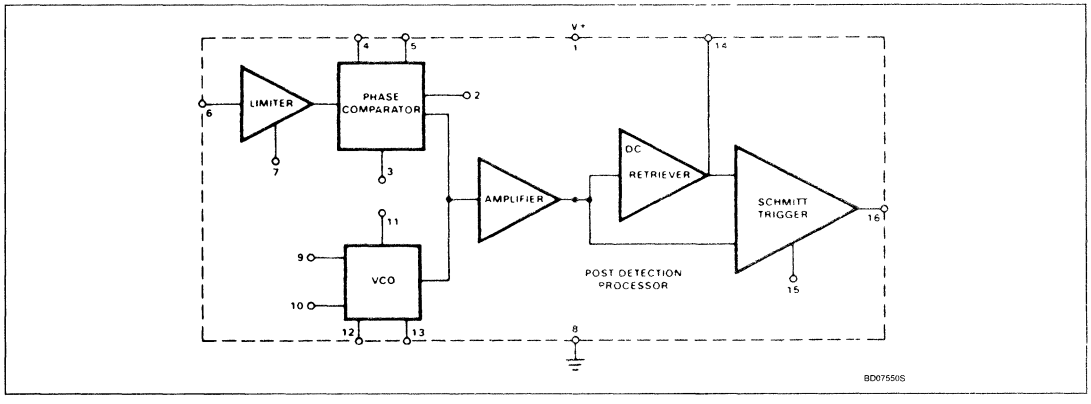


4

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE564D
16-Pin Plastic DIP	0 to +70°C	NE564N
16-Pin Plastic DIP	−55°C to +125°C	SE564N
16-Pin Cerdip	−55°C to +125°C	SE564F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Supply voltage Pin 1 Pin 10	 14 6	V
I_{OUT}	(Sink) Max (Pin 9)	10	mA
P_D	Power dissipation	600	mW
T_A	Operating ambient temperature NE SE	 0 to +70 −55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

NOTE:
Operation above 5V will require heatsinking of the case.

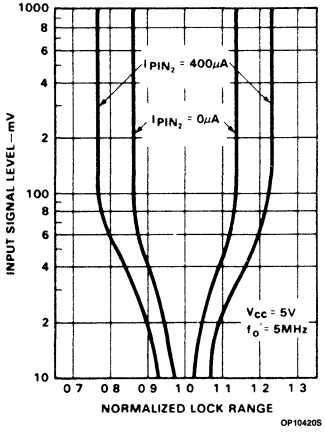
DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C, f_O = 5MHz, I_2 = 400μA, unless otherwise specified.

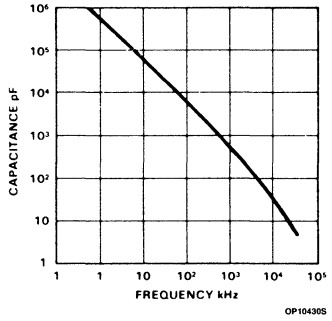
SYMBOL	PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Maximum VCO frequency	C_1 = 0 (stray)	50	65		45	60		MHz
	Lock range	Input ≥ 200mV$_{RMS}$ T_A = 25°C T_A = 125°C T_A = −55°C T_A = 0°C T_A = 70°C	40 20 50	70 30 80		40	70 70 40		% of f_O
	Capture range	Input ≥ 200mV$_{RMS}$, R_2 = 27Ω	20	30		20	30		% of f_O
	VCO frequency drift with temperature	f_O = 5MHz, T_A = −55°C to +125°C T_A = 0 to +70°C = 0 to +70°C f_O = 500kHz, T_A = −55°C to +125°C T_A = 0 to +70°C		500 300 	1500 800 		 600 500		PPM/°C
	VCO free-running frequency	C_1 = 91pF R_C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_O
	Demodulated output voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = −55°C 1%T = 70°C 1%T = 125°C	 16 8 6 12	 28 14 10 16		 16 8 	 28 14 13 15 		 mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 1% V_{CC} = 4.5V V_{CC} = 5.5V	 7 8	 12 14		 7 8	 12 14		 mV$_{RMS}$ mV$_{RMS}$
I_{CC}	Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	 V_{OUT} = 5V, Pins 16, 9 I_{OUT} = 2mA, Pins 16, 9 I_{OUT} = 6mA, Pins 16, 9		 1 0.3 0.4	 20 0.6 0.8		 1 0.3 0.4	 20 0.6 0.8	 μA V V

TYPICAL PERFORMANCE CHARACTERISTICS

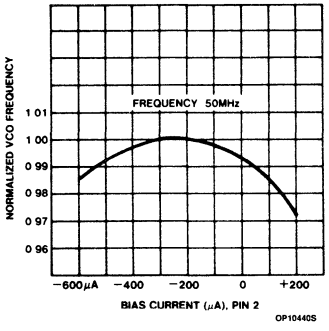
Lock Range vs Signal Input



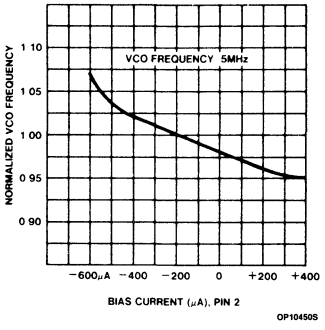
VCO Capacitor vs Frequency



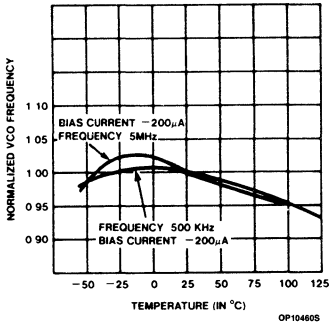
Typical Normalized VCO Frequency as a Function of Pin 2 Bias Current



Typical Normalized VCO Frequency as a Function of Pin 2 Bias Current



Normalized VCO Frequency as a Function of Temperature



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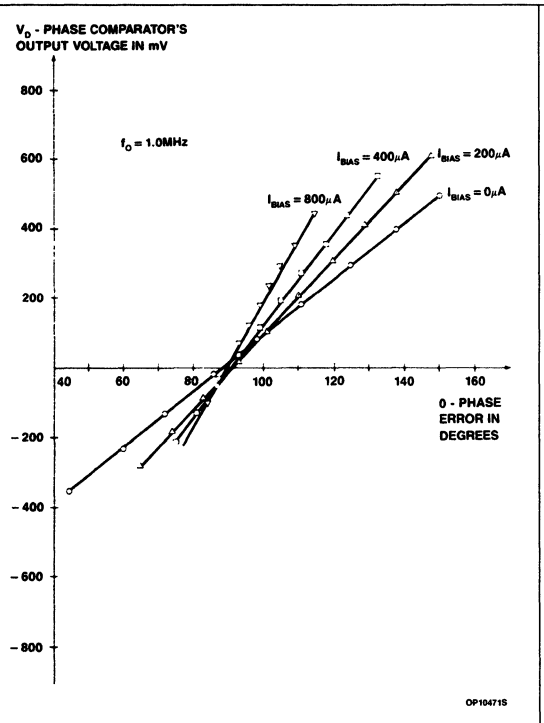
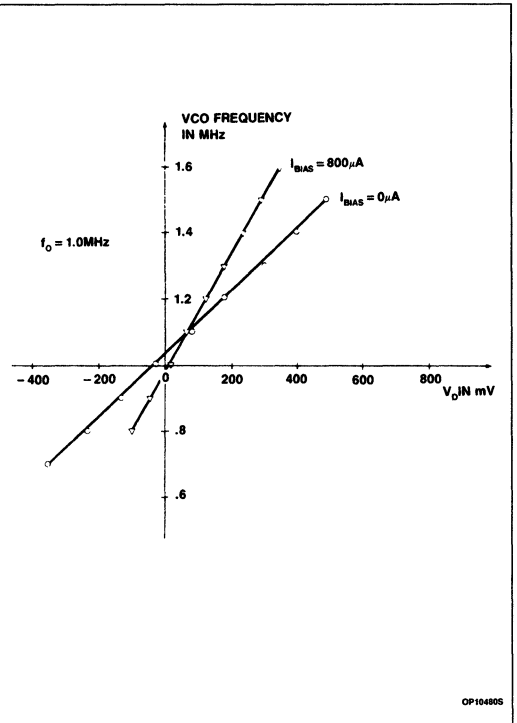
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

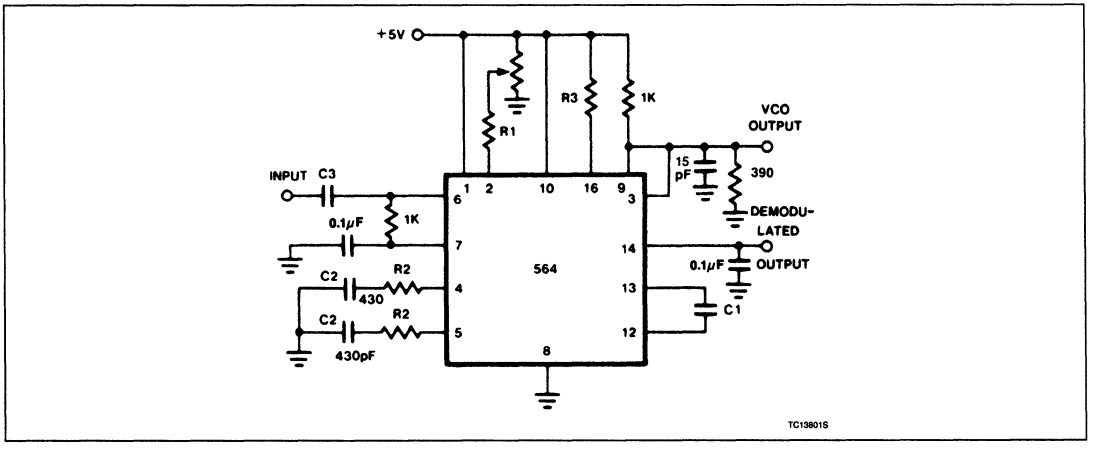


Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current (K_D)



VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)

TEST CIRCUIT



FUNCTIONAL DESCRIPTION (Figure 1)

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

K_{VCO} = conversion gain of the VCO

f_{IN} = frequency of the input signal

f_O = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow-band signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25} - Q_{26}$ form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \simeq \frac{1}{22\ R_C\ (C_1 + C_S)} \quad (2)$$

4

EQUIVALENT SCHEMATIC

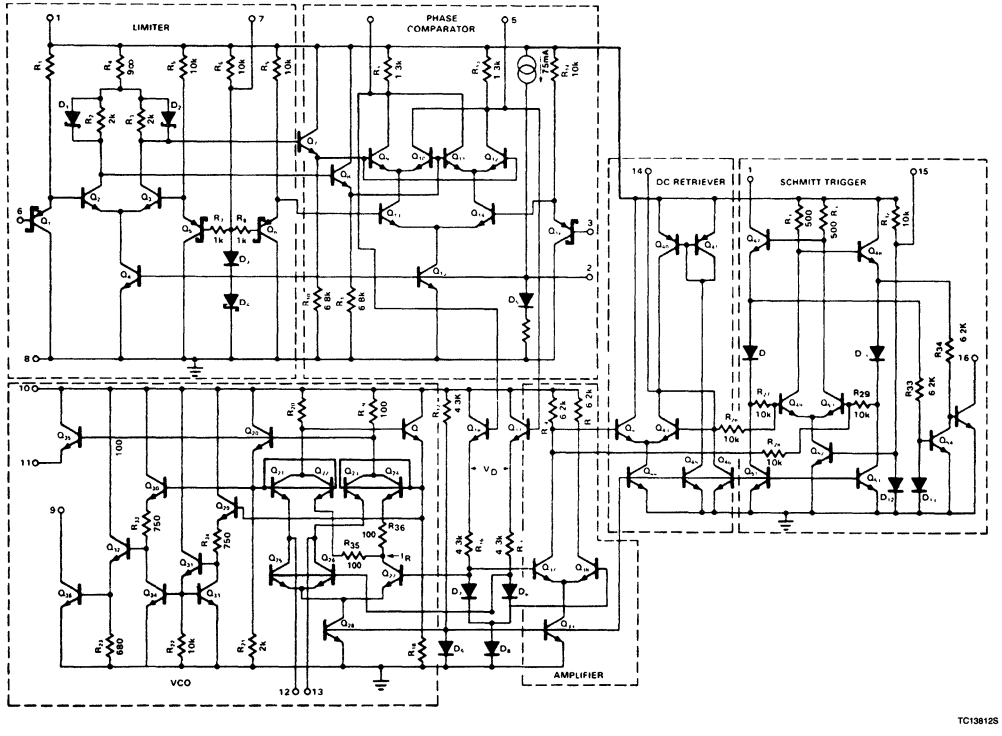


Figure 1

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)

C_1 = external frequency setting capacitor

C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

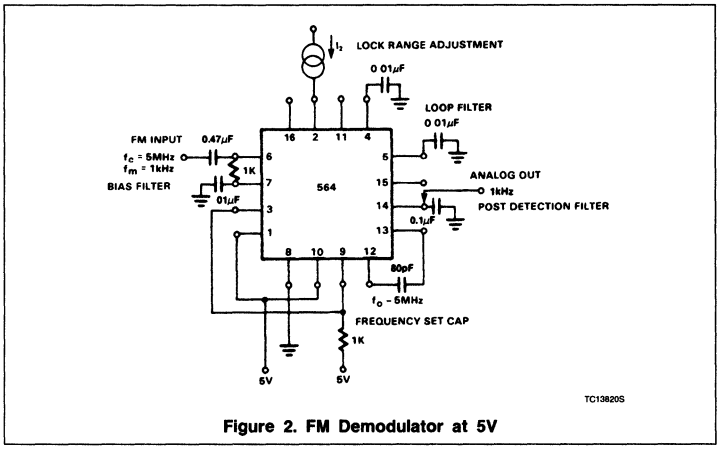


Figure 2. FM Demodulator at 5V

Phase Comparator Section

The phase comparator consists of a double-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transductance amplifier $Q_{42} - Q_{43}$ together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} V_{IN} dt \qquad (3)$$

g_M = transconductance of the amplifier

C_2 = capacitor at the output (Pin 14)

V_{IN} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of $Q_{49} - Q_{50}$ with positive feedback being provided by $Q_{47} - Q_{48}$. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula

The free-running frequency of the VCO is shown by the following equation:

$$f_O \simeq \frac{1}{22\ R_C\ (C_1 + C_S)} \qquad (4)$$

$R_C = 100\Omega$

C_1 = external cap in farads

C_S = stray capacitance

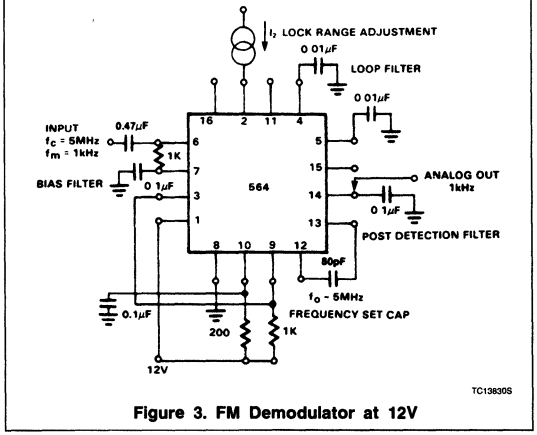


Figure 3. FM Demodulator at 12V

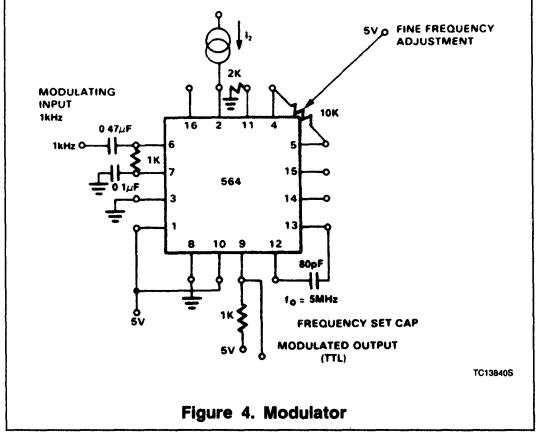


Figure 4. Modulator

The loop filter diagram shown is explained by the following equation:

$$F_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (Internal)*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer function at

$$\omega = \frac{1}{RC_3}$$

NOTE:
*Refer to Figure 1.

APPLICATIONS

FM Demodulator

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 2 and 3, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques

The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 5. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

The lock range graph indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 7 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high-frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.

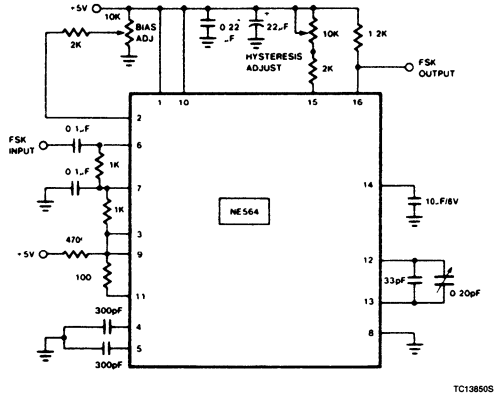
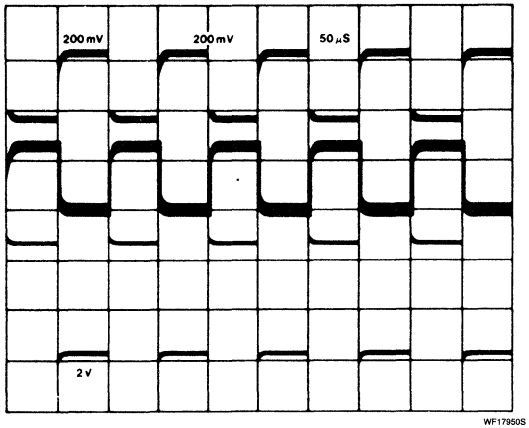
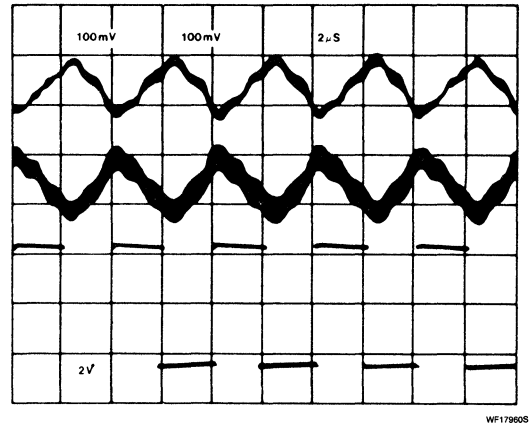


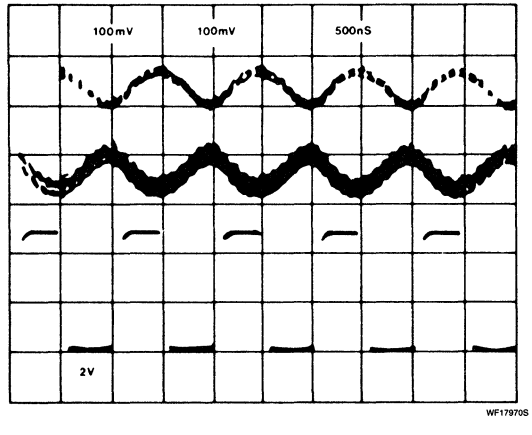
Figure 5. 10.8MHz FSK Decoder Using the 564



a. Data Rate = 20k Baud



b. Data Rate = 500k Baud



c. Data Rate = 2.0m Baud

NOTES:
1 Top trace = Pin 4
2. Center trace = Pin 5
3 Bottom trace = Pin 16

Figure 6. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO:

   If ÷ N in feedback loop, then $f_O = N \times f_{IN}$.
2. Calculate value of the VCO frequency set capacitor:

$$C_O \simeq \frac{1}{2200\ f_O}$$

3. Set I_2 (current sinking into Pin 2) for ≅ 100μA. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pins 4 – 5 for exact center frequency, if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section).
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in

duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO offset.

8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 – 50μF on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

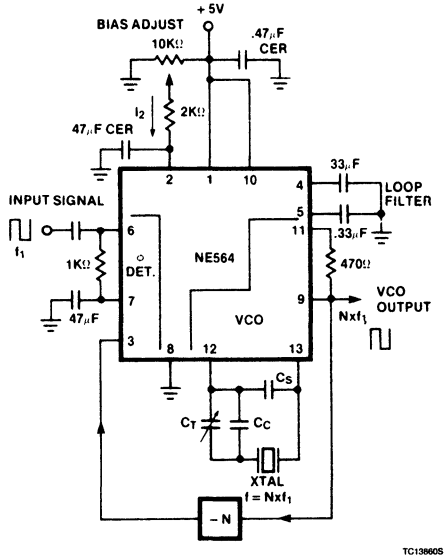


Figure 7. NE564 Phase-Locked Frequency Multiplier with VCXO

Signetics

AN179
Circuit Description of the NE564

Application Note

Linear Products

CIRCUIT DESCRIPTION Of The NE564

The 564 contains the functional blocks shown in Figure 1. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the 564 has internal circuitry for an input signal limiter, a DC retriever, and a Schmitt trigger. The complete circuit for the 564 is shown in Figure 1.

Limiter

The input limiter functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the 564's limiter are that it is capable of accepting TTL signals, operates at high frequencies up to 50MHz, and remains functional with variable supply voltages between 5 and 12V *

Signal limiting is accomplished in the 564 with a differential amplifier whose output voltage is clipped by diodes D_1 and D_2 (see Figure 2) Schottky diodes are used because their limiting occurs between 0 3 to 0.4V instead of the 0.6 to 0.7V for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5V operation. When limiting, the DC voltage across R_2 R_3 remains at the Schottky diode voltage. Good high-frequency performance for Q_2 and Q_3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q_4 (See Figure 1).

Base biasing for Q_3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5V amplitude or a low-level, AC coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 2 with the addition of the vertical Schottky PNP transistors Q_1 and Q_5 as shown in Figure 3. The input signal voltage appears as a collector-base voltage for Q_1, which presents no problems for either high TTL level inputs or low-level analog inputs. Q_5 is in turn diode-biased by D_3 and D_4 (see Figure 1) which places the base voltages of Q_1 and Q_5 at approximately 1.0V. This same biasing network establishes a 1.3V bias at the base of Q_{13} for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q_9 through Q_{12}) after buffering the level shifting through the $Q_7 - Q_8$ emitter-followers.

*When operating above $5V_{DC}$, a limiting resistor must be used from V_{CC} to Pin 10 of the 564

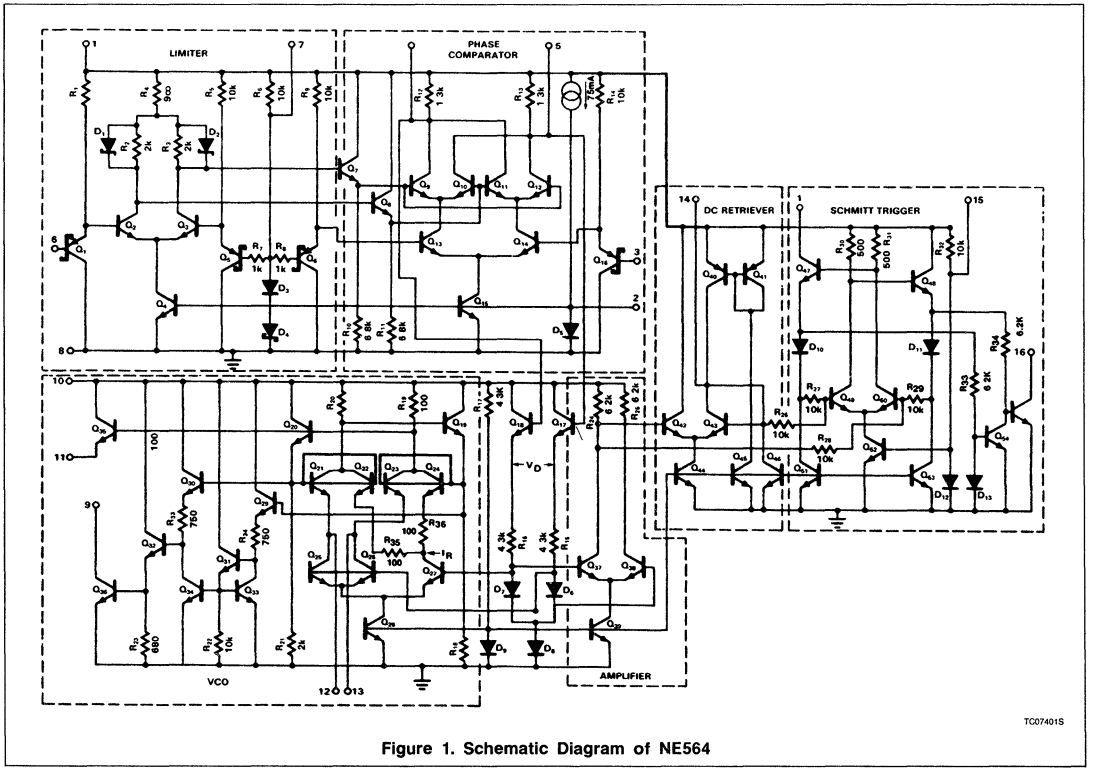


Figure 1. Schematic Diagram of NE564

Circuit Description of the NE564 AN179

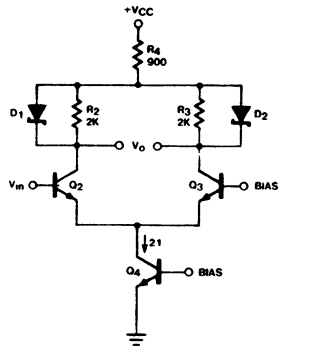


Figure 2. Basic Limiter Stage

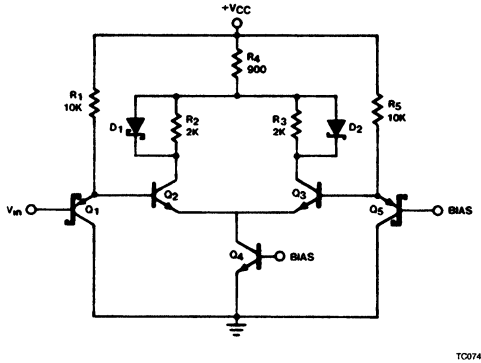


Figure 3. Limiter Stage With Input Buffering

Phase Comparator

The phase comparator section of the 564 is shown in Figure 4. It is basically the conventional, double-balanced mixer commonly used in PLL circuits, with a few exceptions. The transconductance, g_M, for the $Q_{13} - Q_{14}$ differential amplifier is directly proportional to the mirror current in Q_{15}. Thus, by externally sinking or sourcing current at Pin 2, g_M can be changed to alter the phase comparator's conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5V operation. If the current is externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.

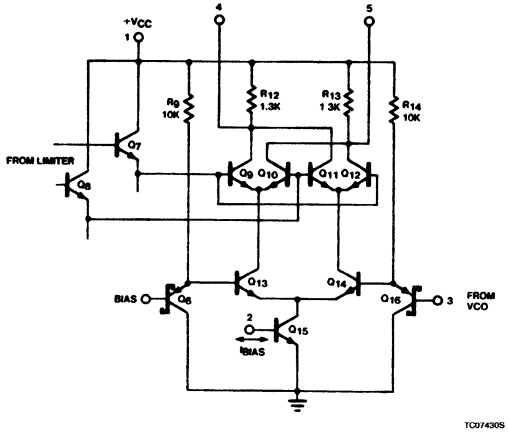


Figure 4. Phase Comparator Section

Circuit Description of the NE564 AN179

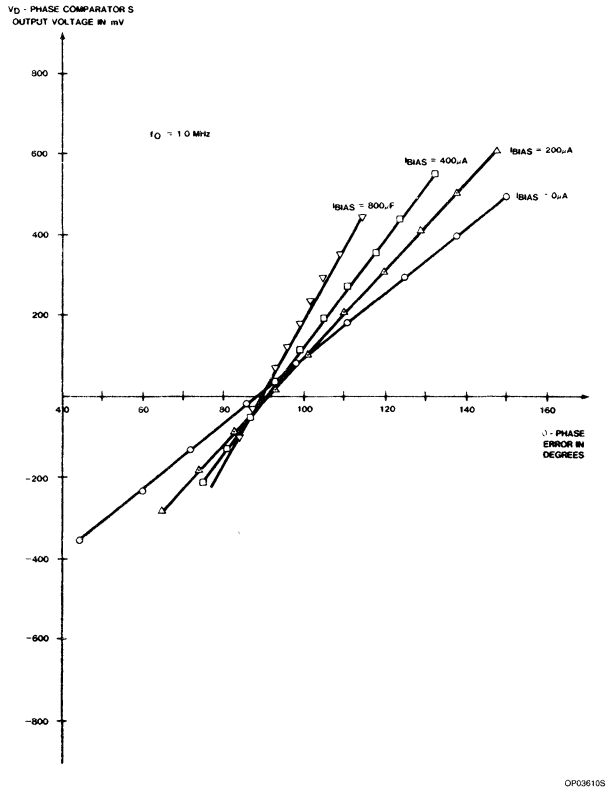


Figure 5. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

Circuit Description of the NE564 AN179

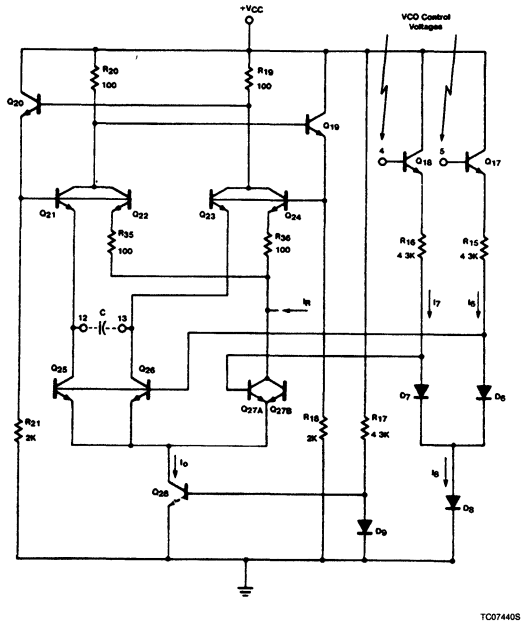


Figure 6. VCO Section of NE564

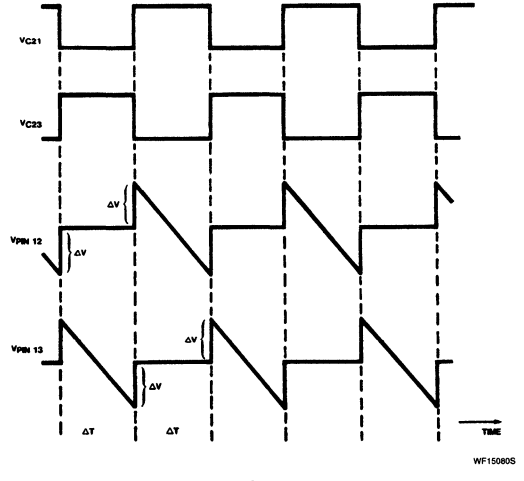


Figure 7. VCO Waveshapes

The variation of K_d with bias current at Pin 2 is shown in the experimental results of Figure 5. Note that the inherent 90° phase error in the loop produces an approximate zero-phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 5 can be expressed as

$$K_d \simeq 0.46\left(\frac{\text{volts}}{\text{rad}}\right) + 7.3 \times 10^{-4}\left(\frac{\text{volts}}{\text{rad} \times \mu A}\right) \times I_{BIAS}\ (\mu A) \quad (1)$$

Equation 1 is valid for bias current less than 800μA where saturation occurs within the phase comparator.

The current level established in Q_{15} of Figure 3 determines all other quiescent currents in the phase comparator (Q_9 through Q_{14}). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (Pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_o) also depends upon the bias current at Pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 6 consists of Q_{19}, Q_{20}, Q_{21}, and Q_{23} with current sinks of Q_{25} and Q_{26}. The master current sink of Q_{28} keeps the total current constant by altering the ratio of currents in $Q_{25} - Q_{26}$ and the dummy current sink of Q_{27}.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through $Q_{17} - Q_{18}$ and $R_{15} - R_{16}$, the VCO control voltage is applied differentially to the base of Q_{27} and to the common bases of Q_{25} and Q_{26}.

The VCO control voltages from the phase comparator are the Pin 4 and Pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + \tfrac{1}{2}V_{DM} \quad (2)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} - \tfrac{1}{2}V_{DM} \quad (3)$$

where V_{CM} and V_{DM} are the respective common-mode and difference-mode voltages.

Circuit Description of the NE564 AN179

Emitter-followers Q_{17} and Q_{18} convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \frac{1}{R_{15}}\left[V_{CM} - \tfrac{1}{2}V_{DM} - 3\ V_{BE}\right] \quad (4)$$

$$I_7 = \frac{1}{R_{16}}\left[V_{CM} + \tfrac{1}{2}V_{DM} - 3V_{BE}\right] \quad (5)$$

These individual currents are summed in D_8 and become with $R_{15} = R_{16} = R$.

$$I_8 = I = I_6 + I_7 = \tfrac{2}{R}(V_{CM} - 3\ V_{BE}) \quad (6)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \frac{I}{2}(1 - \frac{V_{DM}}{RI}) \quad (7)$$

$$I_7 = \frac{I}{2}(1 + \frac{V_{DM}}{RI}) \quad (8)$$

Now consider variations in I_6 and I_7 while I remains constant.

Let 'x' indicate the current imbalance such that

$$I_6 = (1 - x)I = \frac{I}{2}(1 - \frac{V_{DM}}{RI}) \quad (9)$$

$$I_7 = xI = \frac{I}{2}(1 + \frac{V_{DM}}{RI}) \quad (10)$$

where $0 \leqslant x \leqslant 1$. Thus x is defined to be

$$x = \frac{I}{2}(1 + \frac{V_{DM}}{RI}) \quad (11)$$

Currents I_6 and I_7 establish proportional currents in Q_{25}, Q_{26}, and Q_{27} in a manner similar to the analysis above since the current in Q_{28} is a constant, or

$$I_O = I_{C28} = I_{E25} + I_{E26} + I_{E27A} + I_{E27B}$$

It can be shown that the $D_7 - D_8$ diode pair will cause identical differential currents to be reflected in both the $Q_{25} - Q_{26}$ and the $Q_{27A} - Q_{27B}$ differential amplifier pairs. Consequently, the constant-current of I_O, jointly shared by the differential amplifier pairs, will divide in each pair with the same x factor imbalance as in Equation 11.

$$I_{E25} + I_{E26} = xI_O \quad (12)$$

$$I_{E25} = I_{E26} = \frac{x}{2}I_O \quad (13)$$

$$I_{E27A} + I_{E27B} = (1 - x)I_O \quad (14)$$

$$I_{E27A} = I_{E27B} = (\frac{1-x}{2})I_O \quad (15)$$

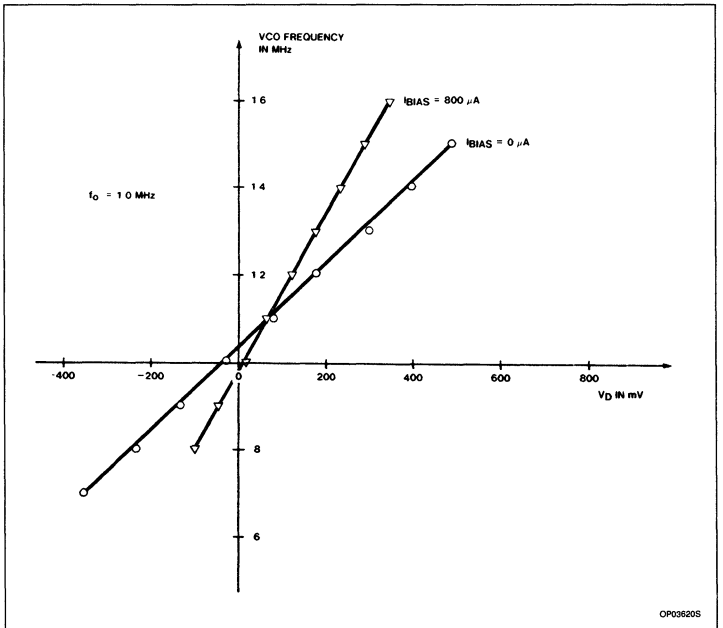


Figure 8. VCO Output as a Function of Input Voltage and Bias Current

Now consider placing a capacitor between the collectors of Q_{25} and Q_{26} (Pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q_{21} and Q_{23} and constantly discharged by Q_{25} and Q_{26}. When the Q_{21} and Q_{22} pair conducts, Q_{23} and Q_{24} will be off, causing a negative ramp voltage to appear at Pin 13 and a constant voltage at Pin 12 as shown in Figure 7. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q_{25} and Q_{26}, which act as constant-current sinks with current amplitudes as in Equation 13.

During each half-cycle, the capacitor voltage changes linearly by $2\Delta V$ volts in ΔT seconds where

$$\Delta V = 2R_{20}I_O\left(\frac{x}{2} + \frac{1-x}{2}\right) = R_{20}I_O \quad (16)$$

and

$$\Delta T = \frac{C2\Delta V}{I_{E25}}. \quad (17)$$

Combining these two equations with Equation 13 gives a half period of

$$\Delta T = \frac{4C\ R_{20}}{x} \quad (18)$$

Utilizing Equation 11 with the ΔT expression gives the desired VCO frequency expression of

$$f_O = f_O'(1 + \frac{V_{DM}}{RI}) = f_O'\left[\frac{V_{DM}}{2(V_{CM} - 3\ V_{BE})}\right] \quad (19)$$

where f_O' is the VCO's free-running frequency given by

$$f_O' = \frac{1}{22\ R_{20}C} \quad (20)$$

Equation 19 shows that the oscillator frequency is a linear function of the differential voltage from the phase comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the $Q_{25} - Q_{26}$ transistor pair and the dummy Q_{27}. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_o = \frac{\partial f_O}{\partial V_{DM}} = \frac{f_O'}{RI}\ \frac{Hz}{V} \quad (21)$$

which is valid as long as the transistor's V_{BE} changes are small with respect to the common-mode voltage. Both f_O and K_o are in-

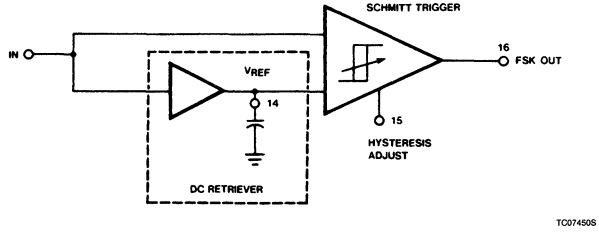


Figure 9. Post Detection Processor for FSK

versely proportional to R, which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 6.

Experimental determination of K_o can be found from the data of Figure 8 where K_o is the slope of either line. Numerically these results are for $I_{BIAS} = 0$.

$$K_o = 0.95\frac{MHz}{V} = 5.9 \times 10^6\frac{rad}{volt\text{-}sec} \quad (22)$$

and for $I_{BIAS} = 800\mu A$

$$K_o = 1.7\frac{MHz}{V} = 10.45 \times 10^6\frac{rad}{volt\text{-}sec} \quad (23)$$

It must be noted that the specific values obtained for K_o in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_o at other free-running frequencies can be obtained by linearly scaling K_o to the desired f_O'. Thus, it is sometimes convenient to define a normalized K_o as

$$K_{o(norm)} = \frac{K_o}{f_O'} = 5.9\ \frac{rad}{V}(I_{BIAS} = 0)$$

$$= 10.45\frac{rad}{V}(I_{BIAS} = 800\mu A) \quad (24)$$

The K_o estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_o(\text{any } f_O') = K_{o(norm)}f_O'. \quad (25)$$

The additional VCO circuitry of Q_{29} through Q_{36} functions to produce the TTL and ECL compatible outputs at Pins 9 and 11.

Amplifier

The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 1. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at Pin 14 produces a stable DC reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at Pin 14 is directly proportional to the difference between the input frequency and f_O'. Thus Pin 14 provides the demodulated output for an FM input signal.

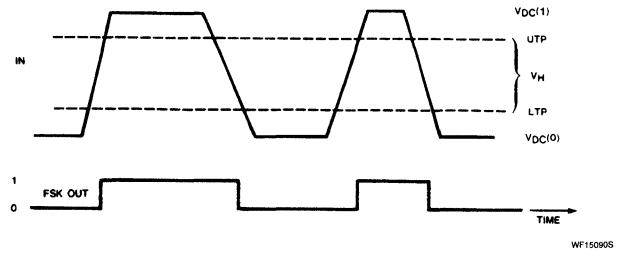
Schmitt Trigger

In FSK applications, the Pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However, at high data rates, V_{DM} will contain a considerable amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also, since the control voltage for the comparator depends upon K_o and the deviations of the mark and space frequencies from f_O', the filtering has to be optimized for each different system utilized. However the necessary DC reference level for the comparator is present in the PLL but buried in carrier-frequency feedthrough which appears as noise in the system. A Schmitt trigger with variable hysteresis can be used successfully to decode the FSK data without the need for extensive filtering.

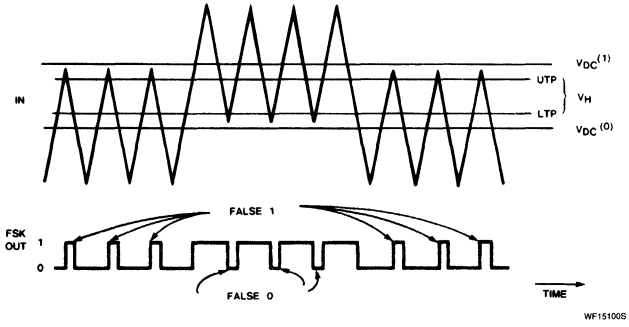
Consider the system shown in Figure 9 where the input signal is the single-ended output derived from the amplifier section of the 564. The DC retriever functions to establish a DC reference voltage for the Schmitt trigger. The upper and lower trigger points are adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be negligible and the ideal situation depicted in Figure 10 results. Increased data rate produces the carrier feedthrough shown in Figure 10b, where false FSK outputs result because the feedthrough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis, as in Figure 10c, produces the desired FSK output in the presence of carrier feedthrough.

Another important factor to be considered is the temperature drift of the f_O' in the VCO. Small changes in f_O' will change the DC level of the input voltage to the Schmitt trigger. This DC voltage shift would produce errors in the FSK output in narrow-band systems where the mark and space deviations in f_{IN} are less than the f_O' change with temperature. However, this effect can be eliminated if the DC or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_O' with temperature do not affect the FSK output.

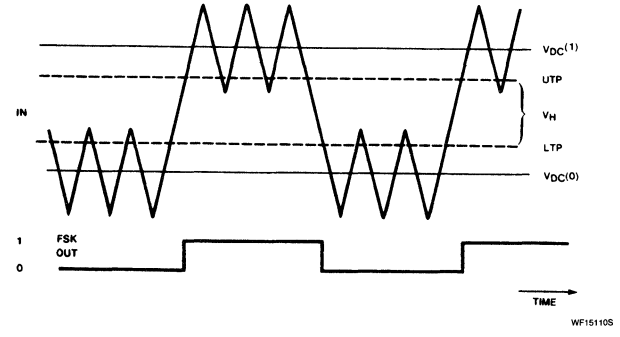
4



a. Low Data Rates With Negligible Carrier Feedthrough



b. False FSK Outputs Due to Feedthrough and Low Hysteresis



c. Increased Hysteresis Restores Proper FSK Output in the Presence of Feedthrough

Figure 10. Waveshapes for FSK Decoding in the Post Detection Processor

AN180
Frequency Synthesis with the NE564

Application Note

FREQUENCY SYNTHESIS WITH THE NE564

Frequency multiplication can be achieved with the PLL in two ways:

a. Locking to a harmonic of the input signal.
b. Insertion of a counter (digital frequency divider) in the loop.

Harmonic locking is simpler and usually can be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. However, a limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

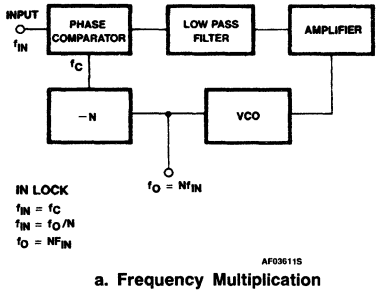
A block diagram of the second scheme is shown in Figure 1a. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input reference frequency so that the VCO is actually running at a multiple of the reference frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications, it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency is DC and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal), if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication, it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more under-damped loop transient response.

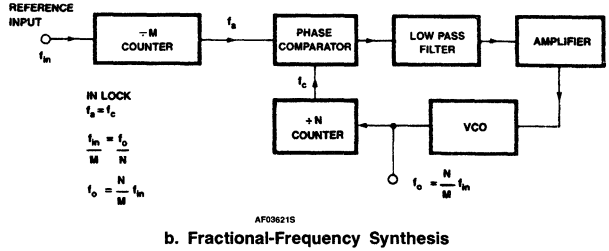
Producing a large number of frequencies with close spacing requires a counter with a large N for the system of Figure 1a. Large N values, in turn, require reference frequencies too low to be practical for commercially available crystals. To overcome this difficulty, a second counter (÷M) is inserted as a prescaler as in Figure 1b to divide down the reference frequency input. This also gives more programming flexibility, since the synthesized output frequencies are functions of both M and N integers, each of which can be changed separately. As an example of fractional frequency synthesis, the two counters can be set to generate an output frequency exactly 16/3 of the input reference frequency. In this case N = 16, M = 3, and the initial f_O' is set to approximately 16/3 times the reference frequency input. The output always will be exactly 16/3 of the input frequency as long as the PLL remains in lock.

PLL frequency synthesizers based upon Figure 1b find wide applications in many types of communications systems that require precisely spaced channels having narrow bandwidths which are centered around relatively high frequencies. For example, Citizens Band (CB) transceiver applications require forty channels corresponding to forty different reference frequencies, each separated by 10kHz bandwidths and centered in the 26 – 27MHz range. Channel 4 uses 27.005MHz; Channel 5 uses 27.015MHz; Channel 6 uses 27.025MHz; and so on. These frequencies could be produced by using forty different crystals — one for each channel. However, this becomes expensive and adds unnecessary complexity to the system. Frequency-mixing techniques have been employed to reduce the number of crystals needed to less than one crystal per channel. For example, one common mixer design uses 14 crystals for 23 channels. As a general rule, most practical approaches that use numerous crystals and mixers to produce discrete frequencies require more than one crystal for every two channel frequencies produced. As the number of channels grows large, frequency synthesis using PLLs becomes more attractive, especially since usually only one or two crystals are needed. Frequency stability of all channels will be essentially the same as that of the crystal reference frequency. Reduced system complexity, size, weight, and power consumption are key advantages of PLL synthesizers.

Since the function of frequency synthesizers is to generate frequencies and not to linearly decode or demodulate input signals, digital PLLs are more commonly used than analog loops.



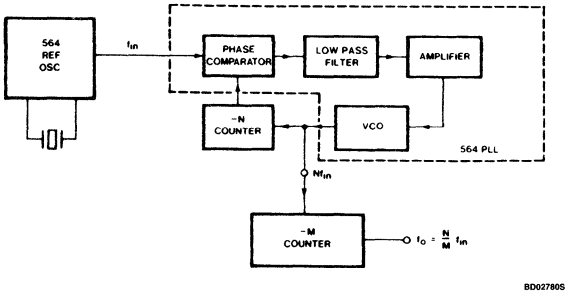
a. Frequency Multiplication



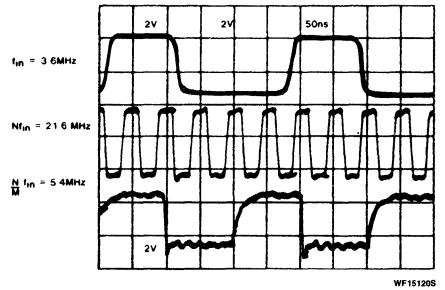
b. Fractional-Frequency Synthesis

Figure 1. Frequency Synthesis Using PLLs

Frequency Synthesis with the NE564 AN180

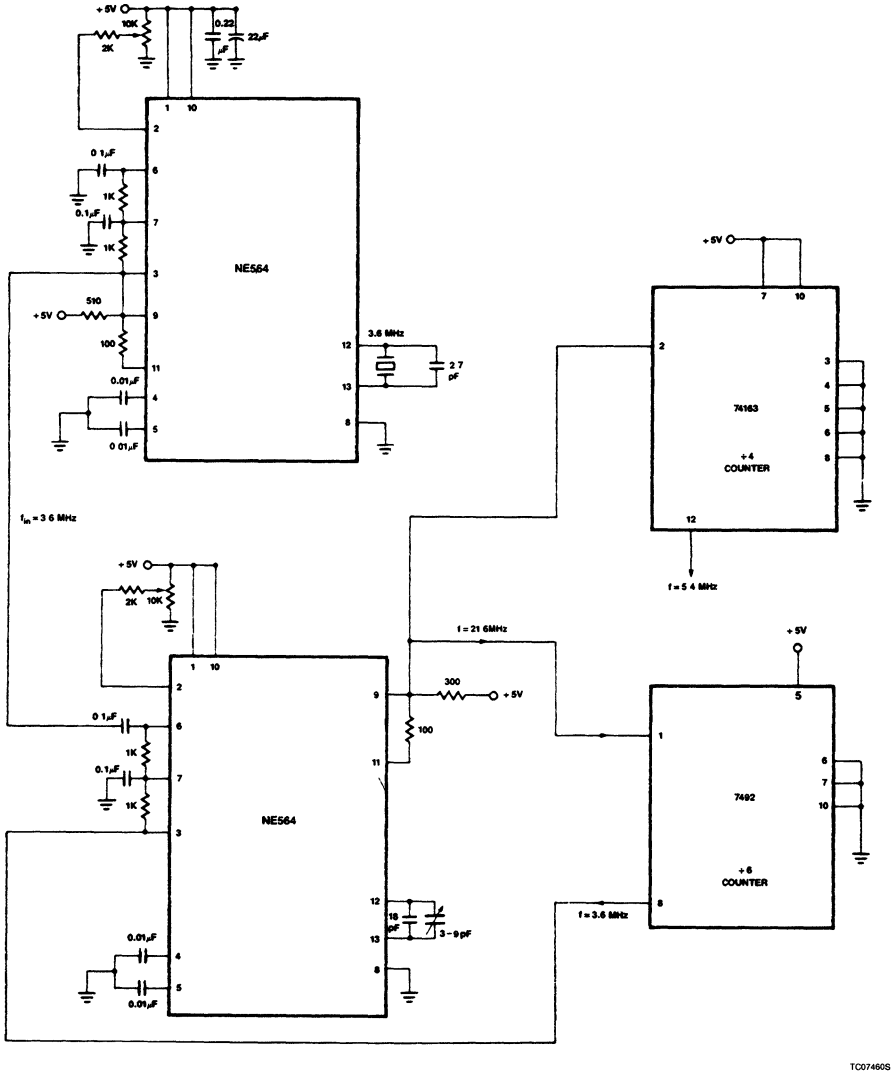


a. Block Diagram Organization



b. Waveshapes

Figure 2. Fractional Frequency Synthesis With the 564



c. Circuit Implementation

Figure 2. Fractional Frequency Synthesis With the 564 (Continued)

Frequency Synthesis with the NE564 AN180

Analog PLLs also can be used for frequency synthesis applications. The 564 is particularly well suited for these applications because the loop is open between the VCO output and the phase comparator input. Also, the phase comparator input and VCO output are compatible with TTL counters.

NE564 FREQUENCY SYNTHESIS WITH CRYSTAL CONTROL

The system shown in Figure 2 has been used to generate frequencies of 5.4MHz and 21.6MHz from a 3.6MHz crystal-controlled source. This reference signal input is produced by using the crystal as the frequency-determining element in the VCO of a second PLL. The thermal stability of all three frequencies will be the same as the stability afforded by the crystal. It may be necessary to place a small detuning capacitor in parallel with the crystal to precisely tune the PLL to the crystal's resonant frequency and to prevent oscillations at harmonics of the resonant frequency. The value of this tuning capacitance must always be kept considerably less than the value required to produce an f_O' without the crystal present. Otherwise the crystal will lose control and the input reference frequency will be set by the capacitor alone.

A recommendation for improved 564 operation is to utilize a divide-by-N counter in the loop which produces "square" waves for the phase comparator that have as close to a 50% duty cycle as possible. Normally, counters with even N values produce square wave outputs perfectly compatible for the phase comparator. Counters for odd N values more commonly produce unsymmetrical outputs that can be less desirable inputs to the phase comparator. An easy modification to "square up" odd divide-by-N counter outputs is to insert a single toggling flip-flop stage between the counter output and the phase comparator's input. This produces an effective 2N multiplication of the input frequency within the PLL. The extra factor of two is removed by a second toggle flip-flop whose input is the output from the first flip-flop. This is the same system as was previously shown in Figure 2a where the +N counter becomes a +2N and M = 2 for the second counter.

Signetics

AN1801
10.8MHz FSK Decoder With NE564

Application Note

Linear Products

FSK DEMODULATION WITH THE 564

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 1 shows a high-frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 4a to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

Figure 2b indicates that the ±1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies

A more thorough analysis confirms these lock range conclusions and serves as a guide for designing other systems. The closed-loop gain of the PLL is equal to the system's lock range and is found as the product of K_d and K_o adjusted to 10.8MHz

$$2\omega_L = K_V = K_d K_o \qquad (1)$$

$$2\omega_L = \left(0.46 \frac{\text{volt}}{\text{radian}}\right)\left(0.875 \frac{\text{MHz}}{\text{volt}}\right) \times \left(2\pi \times 10.8 \times 10^6 \frac{\text{radian}}{\text{sec}}\right)$$

$$2\omega_L = 2.73 \times 10^7 \frac{\text{radian}}{\text{sec}} \quad \text{(Lock range total)}$$

Thus Pin 2 could be left as an open circuit and the internally set closed-loop gain would be adequate for tracking the mark and space input frequencies. However, to be safe, a bias adjustment as shown in Figure 1 is recommended to allow for K_d and K_o variations from device to device.

Designing for a capture range of approximately 700kHz gives a low-pass filter time constant of

$$\omega_c \cong \sqrt{\frac{\omega L}{\tau}} \qquad 2\omega_L = K_V = 2.73 \times 10^7 \qquad (2)$$

$$(2\pi \times 700 \times 10^3) \cong \sqrt{\frac{2.73 \times 10^7}{\tau}}$$

$$\tau = 1.18\text{ms}$$

Therefore, choose the low-pass filter capacitor as

$$C = \frac{\tau}{R} = \frac{1.41\mu s}{1.3k} \simeq 1\text{nF} \qquad (3)$$

Two 1nF capacitors were selected for the design

Capacitive coupling was used for the FSK input and is recommended to avoid DC feedthrough. This DC voltage would act as a DC offset to shift f_O' from 10.8MHz Balanced biasing with the 1.0kΩ resistors from Pin 7 to Pins 3 and 6 also is recommended to establish symmetrical, quiescent current conditions in the limiter and phase comparator sections of the 564 The 470Ω pull-up resistor for the VCO output was found to give a rise time less than 10ns. This rise time was further reduced by adding the 100Ω resistor between Pins 9 and 11. Figure 3 shows an unmodulated 10 8MHz input signal and the VCO output. Note the approximate 90° phase lag of the VCO output

A 0.1μF DC retriever capacitor (Pin 14) has less than 1Ω impedance at f_O, and represents a good compromise between high baud rates (~100k baud) at f_O' and higher-order filtering If very high baud rates are used, this capacitor could be made smaller with an accompanying increase in the Schmitt trigger hysteresis voltage. The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 5 for 20k, 500k, and 2M baud rates with square wave FSK modulation Note the magnitude and phase relationships of the phase comparator's output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.

The phase comparator's outputs exhibit the waveshapes shown in Figure 4 when the FM input is changed from a square wave FSK modulation to a triangular sweep at a 100Hz modulation rate. The amplitude of the triangular sweep was increased from that used with square wave modulation, causing the loop to be driven in and out of lock The loop is locked during the smooth, linear portions of the phase comparator's waveshapes and locked during the remaining portions. Lock and capture frequencies were measured for a Pin 2 bias current of 375μA and f_O' = 10.8MHz as:

Lock. $f_{L1} = 6.2\text{MH}_z$ $f_{L2} = 16.4\text{MH}_z$

Capture: $f_{C1} = 9.3\text{MH}_z$ $f_{C2} = 12\ 2\text{MH}_z$ *P

When the loop is locked, the phase detector's outputs represent the demodulated FM output. When unlocked, high frequency harmonics are present, increasing in amplitude until lock is achieved.

4

10.8MHz FSK Decoder With NE564 AN1801

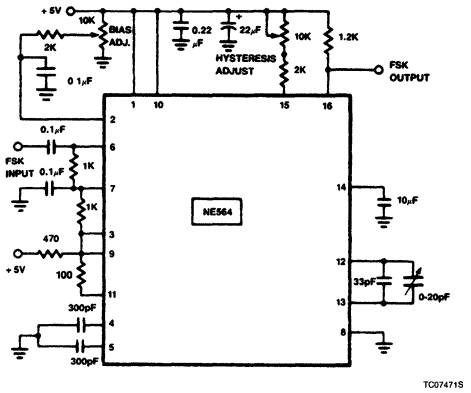
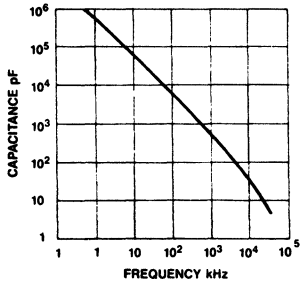
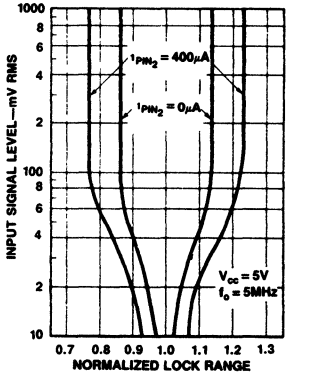


Figure 1. 10.8MHz FSK Decoder Using the NE564

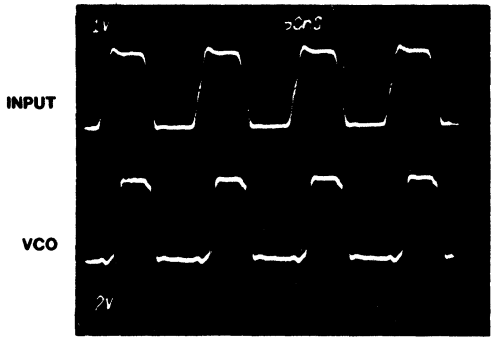


a. VCP Timing Capacitor vs Frequency



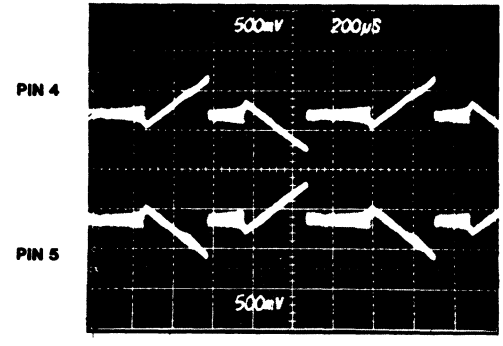
b. Lock Range vs Input Signal Level and Bias Current

Figure 2. NE564 Characteristics



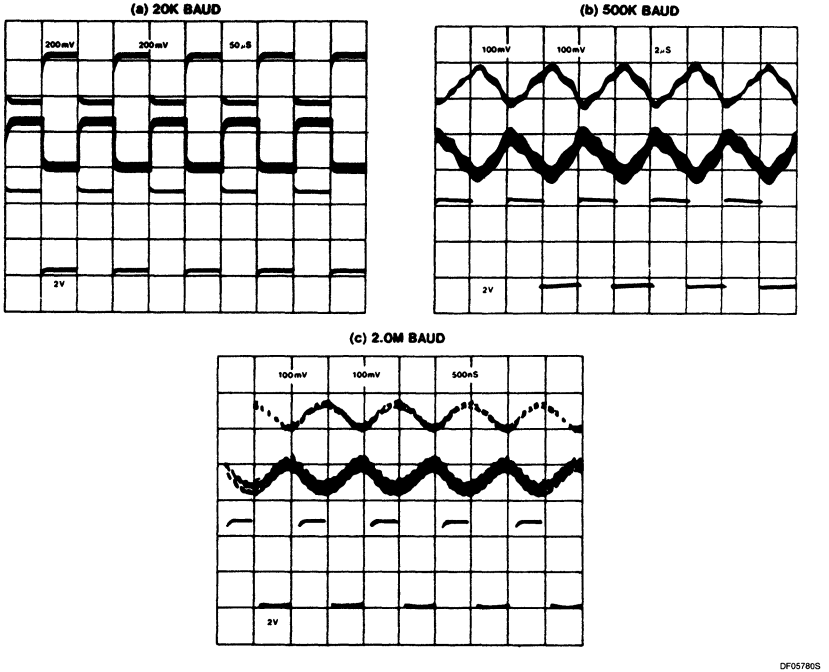
WF15130S

Figure 3. PLL Input and VCO Output for Phase and Frequency Lock at 10.8MHz



DF05770S

Figure 4. Phase Comparator Outputs Showing Lock and Capture Ranges



DF05780S

NOTE:
Top trace — Pin 4
Center trace — Pin 5
Bottom trace — Pin 16

Figure 5. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs for Various Data Rates

Signetics

AN181
A 6MHz FSK Converter Design Example for the NE564

Application Note

Linear Products

Design Example

It is desired to design an FSK converter operating at 6MHz with deviation of ±1%. Supply voltage is 5V. Input to the 564 is from a radio receiver with an amplitude of $0.5V_{RMS}$. Worst case S/N is 10dB. An overall loop damping factor of 0.5 is specified (ζ).

Using the circuit in Figure 1

First the frequency determining capacitor must be established. Using the equation

$$f_O = \frac{1}{22R_CC_O}$$

where R_C is the internal resistance in the VCO oscillator equal to 100Ω. Given two parameters the third is calculated f_O = 6MHz; therefore

$$C_O = \frac{1}{22 \times 100 \times 6 \times 10^6} = 75pF.$$

A parallel 2 – 20pF trimmer and a 68pF ±5% fixed mica capacitor is chosen.

Next, signal level versus bias current and lock range is examined.

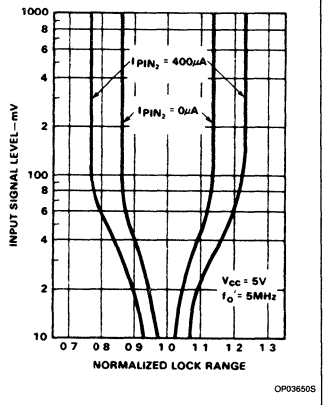


Figure 2. Lock Range vs Signal Input

The signal input to the 564 is specified to be $0.5V_{RMS}$; in the lock range graph, the input level is well within the limiting region of the 564. Thus, no external AM limiter circuit is required and a 10dB S/N (3.1:1) min. should provide reliable communication with a narrow deviation of ±1% (±60kHz) and there is no problem with adequate lock range as it pertains to bias current. We are free to use any loop gain necessary. The bias current sinking into Pin 2 is set to an initial value of 200μA.

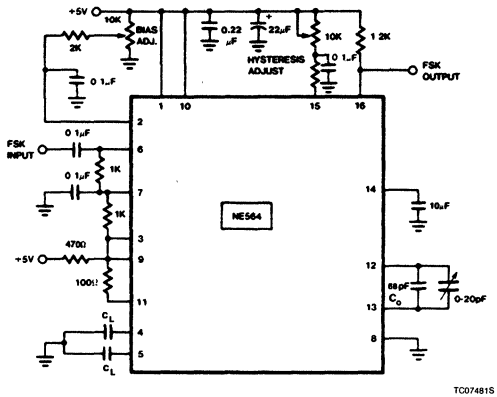


Figure 1. FSK Decoder Using the 564

It's now possible to determine the damping factor of the closed-loop. First, the natural frequency of the loop is calculated from the relationship

$$\omega_n = \sqrt{\frac{K_OK_D}{\tau}} \qquad (1)$$

where

K_O = VCO conversion gain in $\frac{\text{radians}}{\text{sec} \cdot \text{volt}}$

K_D = Phase detector conversion gain in $\frac{\text{volts}}{\text{radian}}$

τ = loop filter time constant in seconds.

For f_O = 6MHz and I_B = 200μA, K_O may be derived from Figure 3a by first constructing an extrapolated transfer line with slope one-quarter of the angle between the existing I_B = 0 and I_B = 800 plots.

Interpolation gives

$$K_O \cong \frac{(1.48 - 1.25MHz)}{(0.4 - 0.2V)} = \frac{\Delta f_O}{\Delta V_O};$$

Multiplying Δf_O by 2π results in

$$K_O = \frac{1.45 \times 10^6 \text{rad/sec}}{0.2V}$$

$$= 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$$

Next, using the K_D graph (Figure 3b), ±1 radian (–90° ± 57°); i.e., $\Delta\theta$ = 1 radian, results in an output of 0.6V/rad.

Therefore, $K_D = \frac{0.6}{\text{rad}} = 0.6$ V/rad at I_B = 200μA.

The value obtained for K_O is for data taken at 1MHz and must be multiplied by 6 in order to find the correct value.

Therefore, $K_O = 6 \times 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$

$$(6MH_z) = 4.34 \times 10^7 \frac{\text{radians}}{\text{sec} \cdot \text{volt}}$$

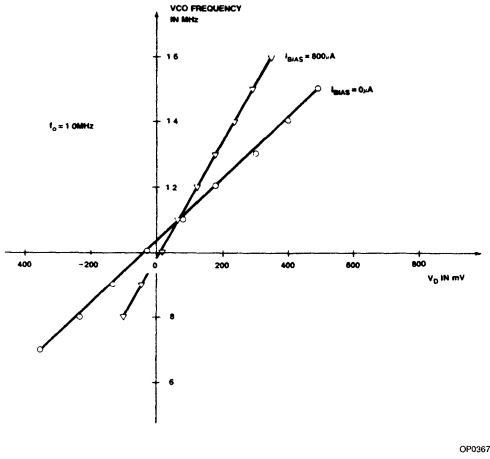
$$K_OK_D = K_V = (4.34 \times 10^7)(0.6) = 2.6 \times 10^7$$

The damping factor specified (0.5) is now used to determine the necessary filter time constant (Pins 4, 5).

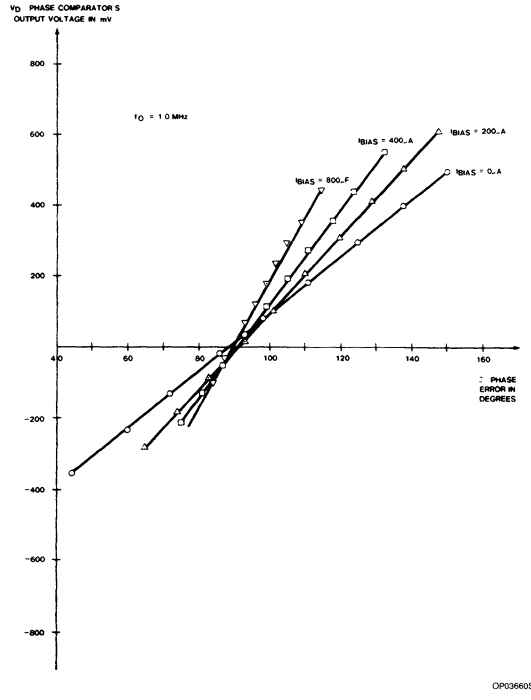
$$\zeta = \frac{1}{2\sqrt{\frac{K_OK_D}{\tau}\,\tau}} = \frac{1}{2\sqrt{K_V\tau}} = \frac{\omega_n}{2K_V} \qquad (2)$$

$$\therefore \tau = \frac{1}{(4)(2.6 \times 10^7)(0.5)^2} = 38ns$$

A 6MHz FSK Converter Design Example for the NE564 AN181



a. VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)



b. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current (K_D)

Figure 3.

Note that the filters on Pins 4 and 5 operate differentially with the net effect that break frequency is

$$\omega_p = \frac{1}{RC} \text{(single pole filter } -3\text{dB freg.)}$$

Now solving for ω_n using (1)

$$\omega_n = \left[\frac{(2.6 \times 10^7)}{(3.8 \times 10^{-8})}\right]^{1/2} = 26 \times 10^6 \text{ radians/sec}$$

f_n = 4.16MHz (natural frequency of the loop and approximate one-sided capture B W)

The value of the loop filter capacitor may be determined by dividing the time constant by the value of the internal resistance, 1 3kΩ.

$$C_L = \frac{\tau}{1.3k\Omega} = \frac{3.8 \times 10^{-8}}{1\,3 \times 10^3} = 29pF$$

This value filter time constant will give a less-than-critically-damped response allowing the fast excursion in V_{CO} frequency necessary to good FSK reception. The tradeoff between response speed and carrier frequency harmonic rejection will have to be considered. A longer time constant gives more carrier rejection but slower response and less damping (Refer to equation 2)

The next step is to test the circuit under actual operating conditions with the specified FSK signal. The level on Pin 15 (hysteresis adjust) must be set in the vicinity of +1.4V in order to attain proper FSK demodulation. Final signal tests may be carried out with noise injected through a resistive summing network at the input (Pin 6) to simulate the 10dB S/N

Note that the loop filter response actually operates on the frequency spectrum above (+) and below (–) the carrier center frequency, or center of deviation, for a symmetric FM or FSK signal. This may be seen in Figure 4

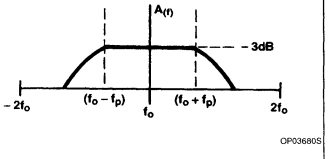


Figure 4. Bandpass Effect of Loop Filter

Signetics

AN182
Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

Linear Products

Application Note

Author: Les Hadley

INTRODUCTION

In order to obtain a local clock signal in Multiplexed Data Transmission systems, a phase and frequency coherent method of signal extraction is required. A Master-Slave system using the quartz crystal as the primary frequency determining element in a phase-lock loop VCO is used to reproduce a phase coherent clock from an asynchronous Data Stream.

The NE564, a versatile phase-locked loop (PLL) operating at frequencies to 50MHz, has inputs and outputs designed to be TTL compatible. The Signetics NE564 is used to generate the phase-locked, crystal-stabilized clock reference signal.

Its particular adaptation, for use with a crystal-controlled VCO instead of the usual RC control elements, requires a brief review of the principles of the Phase-Lock Loop design.

The NE564 Phase-Locked Loop is a fully contained system, including limiter, phase detector, VCO, DC amplifiers, DC retriever and output comparator (reference Figure 1). For the clock regeneration system to be discussed, the portions of the NE564 implemented are the input limiter, phase detector and VCO.

The signal limiter amplifies low level inputs (until saturation is reached, which is typically 60mV$_{P-P}$ for the NE564). The signal limiter output is fed to the phase detector, where the "unknown" input is compared to the "known" VCO frequency of the NE564. The differential error signal that is generated is fed through a DC amplifier and a voltage-to-current converter. The change in the current generated forces the VCO frequency to vary in its frequency and/or phase relationship, such that a θ of 90° lagging is obtained (the actual phase relationship may be somewhat less than 90° depending upon the K_dK_o (gain) product of the NE564 at the operating frequency and bias current). The external filtering incorporated at Pins 4 and 5 control the dynamic frequency response and loop stability criteria.

The NE564 is a first order system; therefore, the use of single capacitors (at Pins 4 and 5) will automatically create a "second-order" system. An RC series filter combination will cause a lead-lag condition that will permit dynamic selectivity, along with closed-loop stability.

LOOP GAIN FUNCTIONS

The phase detector conversion gain (K_d) and the VCO conversion gain (K_o) determine, in large part, the lock range, capture range and linearity characteristics of the NE564. These device parameters are both dependent upon bias current and operating frequency. Some typical curves for each of the parameters are shown for the NE564 in Figures 2 and 3.

THE CLOCK REGENERATOR CIRCUIT

The basic building blocks of the clock regenerator circuit are shown in Figure 4. The PLL is shown as a frequency multiplier incorporating a divide by "N" in the VCO phase detector feedback loop. The functions of the ringing circuit and the NE527 high-speed comparator will be discussed later.

The waveforms of Figure 5 indicate the waveforms transmitted over a T1 line. The bipolar signal transmitted has "no" DC components induced in the transmission line (reference should be made to the effect of normal mode and common effects on signal information). When transmitted over telephone wire pairs, the resultant signal (at the receive end) will have been degraded in both waveshape and signal-to-noise ratios. Typical attenuation factors for a T1 line are −30dB per 6000 feet.

In addition, pair-to-pair crosstalk can degrade signal-to-noise ratios. The energy transmitted in the bipolar system of signal transfer is centered at 772kHz (generated by the bit format).

At the receiving end the bipolar signal information is converted to a unipolar pulse train after being amplified, filtered and fed through an automatic level control circuit. Some types

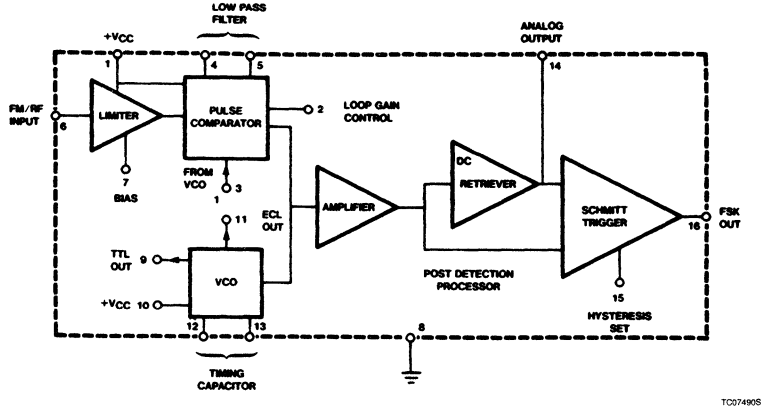


Figure 1

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

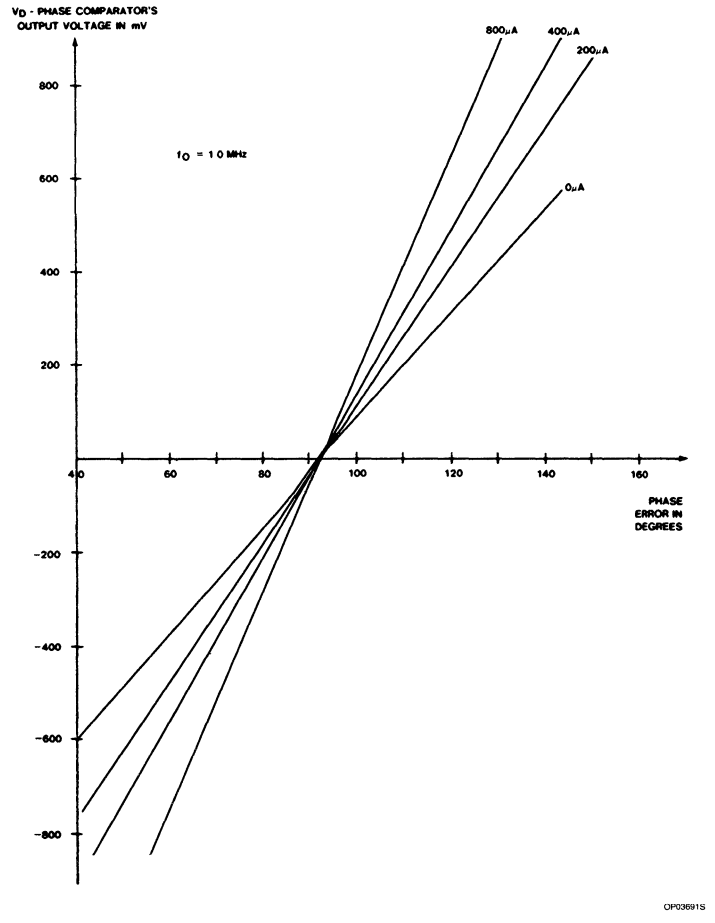


Figure 2. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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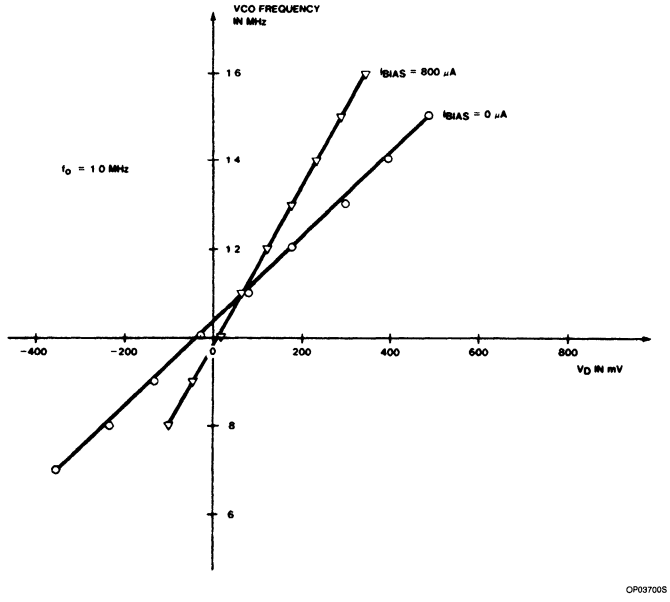

Figure 3. VCO Output Frequency as a Function of Input Voltage and Bias Current

of PCM systems use the rectified and filtered DC (average) to control the phase of the regenerator clock; however, in newer systems, bipolar signals are preprocessed (or preconditioned) by terminal common equipment resulting in unipolar information.

T1 Data Transmission

The bipolar signal, as transmitted on a T1 line, appears below with the original binary, converted unipolar and clock waveform (reference Figure 5).

The bipolar signal, when transmitted over standard wire pairs, will be degraded both in wave shape and signal-to-noise by the time it reaches the signal repeater. This is due to the attenuation factor of the cable which is nearly -30dB for 6000 ft. In addition, pair to pair crosstalk degrades signal-to-noise. The energy in the transmitted bipolar signal is centered at 772kHz due to the particular bit format. Bipolar signals have no DC offset.

At each receiving station the bipolar signal is amplified, filtered and fed through an automatic level control circuit. A full wave rectified signal is then sent to the clock regeneration circuit. This is essentially the format followed by some of the original T1 repeater equipment. The clock regeneration circuit described here could be adapted to this system.

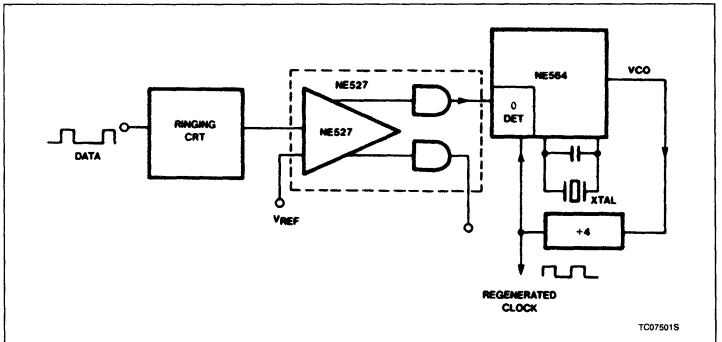

Figure 4

THE T1 SPECTRUM

The bipolar signal is similar to NRZ data in that it does not contain carrier information. In order to give the PLL coherent frequency information sufficient to obtain "capture" and lock, carrier components must be obtained from the data stream. The time duration of the frequency information fed to the PLL is also important in order to obtain accurate and stable information to update the PLL. In order to begin the extraction of frequency information, the positive-going portions of the bipolar data signals are used to drive a class "C" transistor tank circuit (reference Figure 4) which is sharply tuned to the basic clock frequency (1.544MHz). Each positive half cycle of data then starts a wave train of coherent information which is phase synchronous with each succeeding positive data bit. When the LC tank is optimally tuned, relatively extended periods without data bits can be tolerated with minimal loss of frequency and phase information. The combination of good short-term frequency stability of the high "Q" LC tank, coupled with the long-term stability of the crystal-controlled VCO, is the founda-

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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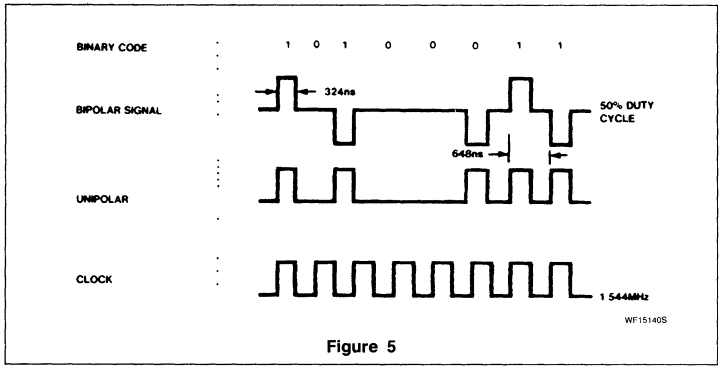


Figure 5

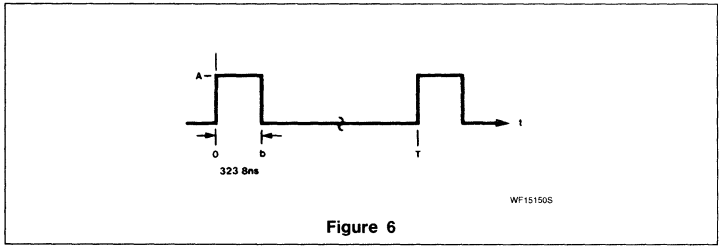


Figure 6

tion of the NE564 clock regeneration system accuracy.

It must be emphasized that data pulse synchronization of the preprocessing circuit must be frequency coherent with the fundamental period of the time base to be extracted. That is, if the time period of the clock is $1/f_C = T$, where f_C is the clock frequency, then the spacing between any positive code bit sequence must be $n \times T$ (reference Figure 6).

Looking at the spectral analysis of the relative energy available to the clock extraction circuitry (with a worst-case duty cycle of 1 of 16) will demonstrate the need for enchancing the particular desired frequency component before applying the signal to the Phase-Lock Loop. For $f_O = 1.544$MHz, the period is $T = 647.67$ns. The pulse or bit width is 323.8ns.

Here the bit duration 323.8ns = b. The Fourier expansion of the discrete spectrum is related by the following equation:

$$F_{(n)} = \frac{(Ab)}{T}\left|\frac{\sin(\frac{n\pi b}{t})}{\frac{n\pi b}{t}}\right| \quad n = 0,1,2 \ldots \quad (1)$$

The basic frequency component resulting from various bit spacing factors is defined by the equation

$$f = \frac{1}{T} \quad (2)$$

where $f \leqslant f_O = 1.544$MHz

If we consider the special case of a single pulse present out of 16 bipolar or 32NRZ periods, then

$T = 16$ bipolar bit times
$= 16 \times 647.67\text{ns} = 10.36\mu s$
$f = 96.5$kHz

Accordingly, the spectral lines will be spaced in multiples of 96.5kHz The spectrum for this particular worst case condition is shown in Figure 7 below

Solving equation 1 for the relative amplitude of the 1.544MHz spectral component with the pulse spacing shown,

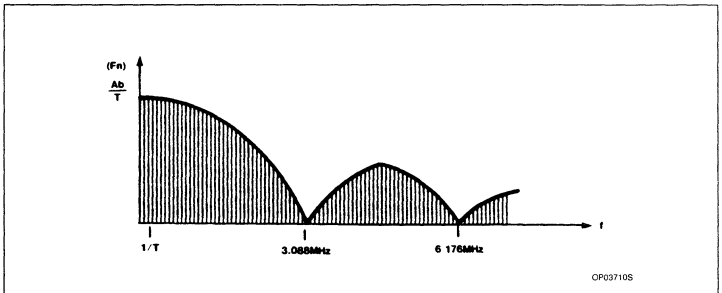
$$F_{(16)}\left(\frac{Ab}{T}\right)\left|\frac{\sin(\frac{16\pi b}{t})}{(\frac{16\pi b}{t})}\right|$$

where $T = 2nb$, $n = 16$

$$= \left(\frac{Ab}{(2)(16)b}\right)\frac{\sin(\frac{16\pi b}{32b})}{(\frac{16\pi b}{32b})} = \frac{A}{32}\frac{2}{\pi}$$
$$= (0\ 02)A$$
$$= -34\text{dB}$$

It is evident that as the bit spacing increases to the point where f_O is the 16th harmonic of the fundamental, very little f_O energy is available to drive a phase-lock regeneration circuit. $F_{(16)}$ is also ineffective since it is an even subharmonic of f_O The PLL will not normally lock to even harmonics; in fact, an error signal is produced which tends to force the VCO out of lock This fact further stresses the need for preprocessing in the frequency domain The class "C" pulsed resonant tank significantly multiplies the magnitude of the f_O spectral component and filters out unwanted subharmonics.

The loop error voltage available from the phase detector for phase correction of the VCO is directly related to the product of the incoming coherent spectral energy multiplied in the balanced mixer with the reference signal derived from the VCO Since the phase error information is integrated in the loop filters, the instantaneous magnitude of the DC error voltage is proportional to the time integral of coherent mixer products. Thus, as the magnitude and time duration of the desired frequency component is increased in the



NOTE:
= 96 5kHz spacing

Figure 7

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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preprocessing circuitry, the VCO phase accuracy is greatly improved. Capture time is obviously enhanced also.

The signal from the tuned tank is buffered by a FET follower N-channel enhancement mode device (reference Figure 12). This provides power gain with virtually no loading on the tank circuit and avoids degrading the "Q". The NE527 comparator is used to provide waveform shaping and symmetry correction. The voltage threshold is set up by a resistive divider with adjustment set for equal duty cycle symmetry. (Note: Recent tests have shown that best crystal lock range symmetry is achieved when the input signal to Pin 6 of the NE564 is maintained at a level between 500 to 800mVP-P.) The coupling network provides the necessary attenuation plus a low impedance signal source which is critical to good Phase Detector operation.

In the particular circuit shown in Figure 12, the 1.544MHz information is applied to the phase detector input of the NE564 Phase-Lock Loop. The VCO, however, is operated at four (4) times this frequency to order to take advantage of economical and readily available crystals. The VCO signal is fed through a divide-by-four counter (74HCT73) to provide the Phase Detector reference and final regenerated clock signal. To avoid loading, the clock signal (1.544MHz) is buffered by the 75451 peripheral driver which provides a high-speed open collector TTL output The input signal is AC coupled in order to reduce DC bias errors in the Phase Detector caused by "O" level variations.

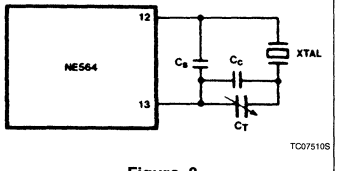


Figure 8

The Crystal[1]

The crystal used was chosen to match the NE564 VCO drive characteristics. It is an "AT" cut oscillator crystal which operates near the anti-resonate or "parallel" mode in this circuit. The crystal may have to be fine-tuned, as indicated in Figure 8. The pulling characteristic of the crystal is adequate to allow for 0 to 70°C operational drift plus initial and aging accuracy tolerance factors and still retain lock between master and slave station VCXOs. The average lock range at room temperature with one of sixteen data bits present is typically 1000Hz for a 6.176MHz crystal with a capture range greater than 500Hz.

For VCO operation at 6.176MHz, C_S is 22pF, C_C is 18pF, and C_t, a 1 – 8pF trimmer capacitor (reference Figure 8).

NE564 CRYSTAL-CONTROLLED VCO

As shown in Figure 8, the crystal is operated with a series capacitor. When properly trimmed, this allows the crystal to operate near the series resonant mode. A crystal manufactured to operate in the series resonant mode will do so only if it sees a pure resistance looking into the oscillator terminals. The circuit below shows an oscillator which looks inductive with the equivalent crystal circuit and trimmer capacitor C_t (reference Figure 9)

If L_O is small and the internal gain of the device high over a wide frequency range, L_O may resonate with the C_O of the crystal at a very high frequency. Under certain conditions the circuit may even tend to operate in the 3rd overtone mode unless measures are taken to roll-off the circuit gain. This is the purpose of C_S in Figure 8. Since the gain of the VCO is a factor in spurious oscillation, the current injected into Pin 2 will also have an effect in this respect. (K_O increases with I_2). At higher operating frequencies this parameter may become more critical in attaining stable start ups in the desired frequency mode. Obviously the size of C_S must be smaller than the value needed to cause free running near the desired frequency without the crystal connected.

CRYSTAL SPECIFICATION

Crystals may be manufactured to operate in either the series mode with no external capacitance (purely resistive load) or in the parallel mode with a specified value of load capacitance. The 564 tends to operate at a frequency above the specified value when a series mode crystal is used. For a design frequency of 6.176000MHz and zero load capacitance. Referring to Figure 8, for C_s = 10pF and C_T = 10pF the average center frequency for an NE564 sample measured in the lab was 6181.192kHz. For the same C_s, but with C_T equal to 60pF, f_O measured 6176.565kHz. A second crystal showed a spread of 6176.600kHz to 6180.855kHz. The effect of the VCO was to pull the crystal to a frequency above its design value. This effect is then nearly tuned out by the external capacitances C_S and C_T. If C_T is sufficiently increased, the crystal will see a purely resistive load and operate at its rated frequency.

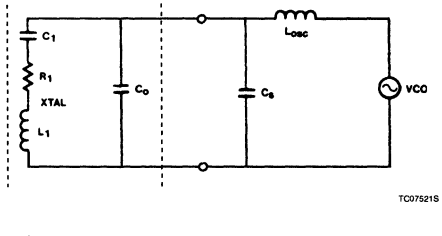
A second approach is to specify a crystal which is to operate near the anti-resonate or parallel mode. Normally this is done with a certain value of external load capacitance specified by the customer which matches the existing circuit parameters. The maximum difference between series and parallel resonance for any crystal is 0.5% of f_O (series resonant mode); for f_r = 6.126MHz, 0.5% of f_r = 30kHz. The usual value would be lower than this.

$$f_a = f_r \sqrt{1 + \frac{1}{r_O}}$$

r_O = electromechanical coupling factor, f_a = parallel resonant frequency). The particular cut of the crystal material determines the drift response over temperature. For oscillator applications, the AT cut offers the best overall stability over a wide frequency and temperature range. Final design uses second approach.

For a stability or total tolerance of ±15ppm over the rated operating range of −20°C to +70°C, a certain manufacturer's crystal actually performed as shown above (Refer to Figure 11).

Calibration accuracy is the allowable frequency tolerance at the reference temperature, i.e., ±10ppm @ 25°C.



NOTES:
C_O = XTAL Shunt capacitors
C_1 = Equivalent XTAL series resonant arm capacitance
L_1 = Equivalent Motional Inductance
R_1 = Equivalent crystal series resistance
C_S = External shunt or stray capacitance

Figure 9

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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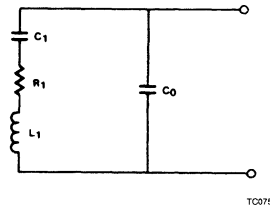


NOTES:
C_1 = Motional capacitance
C_0 = Shunt capacitance
R_1 = Equivalent Resistance
L_1 = Equivalent inductance

Figure 10. Basic Crystal Equivalent Circuit

Figure 11. Design Example

Third, is a long-term drift spec which determines the customer's maximum allowable drift due to aging effects. An acceptable value in quality crystals is ±2ppm/year.

Using our reference crystal of 6 176MHz and the above specifications, the crystal limits over a 1 year period would be:

Temperature stability:	±15ppm × 6.176 =±93Hz
Calibration tolerance:	±10ppm × 6.176 =±62Hz
@25°C Long term drift:	±2ppm × 1 × 6.176 =±12Hz
Total:	(±167Hz)

The above figure of ±167Hz then determines the capture and lock range over which two crystal stabilized VCOs must track under worst case conditions when the exact same crystal specifications are used for master and slave units within an operational system.

Crystal Specifications

'AT' Cut Oscillator Type

Fundamental mode operation HC-33 Case (Standard)

Calibration tolerance:
±10ppm @ 25°C

Temperature stability:
±15ppm; −15°C to +65°C

Circuit operating condition:
Parallel resonance

Frequency specified: 6 176000MHz

Part designation:
Croven #A330 DEF-32 or equivalent

Setup Procedure[2]

Referring to Figure 12, the following setup procedure will aid the user in establishing proper circuit operation.

Regulated supply voltage of +5V and −6V are required. Current drain on the +5V line is ~ 100mA, and 6mA for the −6V.

With proper voltage applied, (1) First check the supply currents to be sure they are in the range indicated above. (2) Check the operation of the NE564 VCXO by looking at Pin 9 with an oscilloscope (see Figure 13). A reasonably symmetric square wave should be present, having a frequency near 6.1MHz. (3) Attach a DVM across the 2k resistor which feeds Pin 2 of the NE564 and adjust for a reading of 2.00V, indicating a 1mA $_{DC}$ current flowing into Pin 2 (The (+) lead of the DVM should be connected to the end of the 2k resistor which ties to the wiper of the 10k pot and the (−) lead to Pin 2 of the 564; reference Figure 14). (4) The exact center frequency is set by adjusting C_t, the crystal trimmer cap, for exactly 6 176000MHz with no signal input (this sets the center frequency of the VCXO to free-run in the center of the capture range) (5) Enable strobe 'A' and 'B' with a +2.7V min. to +5V max. level Apply a standard 1.544MBS NRZ data signal to the input terminal, terminated in 50Ω. The amplitude should be +3 to +5V (0 to peak). Set the duty cycle for 1 bit in a 16-bit period Note the data generator must be driven from a crystal-controlled master oscillator also adjusted for a center data rate of 1.544 000MBS. Monitor the buffered output of the ringing circuit with a scope connected to the source of the SD213 (Figure 15). The waveform should appear as in Figure 17. (6) Adjust tank trimmer cap C_T for a maximum amplitude and note that the cycle period should be 647ns. (7) Now monitor the comparator output signal at Pin 7 and adjust R_t for a 50% duty cycle. The same signal will appear at Pin 5 of the NE527 except it will be inverted. The signal on Pin 7 of the NE527 and Pin 6 of the NE564 should appear as shown in Figure 19. Now attach one lead of a dual-trace scope to Pin 7 of the NE527 and the other to Pin 3 of the NE564 as shown (Figure 16).

The two signals should be in phase-locked with an approximate 90° differential as shown in Figure 20 (data signal applied to @ 1 544MBS) If lock does not occur, a slight trimming of the crystal trimmer C_T should correct for slight differences in master-to-slave crystal tolerance. It is recommended that master and slave crystals be of the exact same design and specification to insure optimal tracking over time and temperature A recommended manufacturer and part number appears at the end of this application note for your convenience.

Once lock is attained, move one lead of the dual-trace scope to the buffered output of the 75451 Pin 3, leaving the other scope probe on Pin 6 of the NE564. The phase-locked waveform should appear as in Figure 25. If a data word generator is being used, you may check overall operation for various bit patterns by synchronizing the scope trigger on the "end of word" pulse, then observe the phase error effect as different combinations are fed in

PHASE JITTER[3]

When operating with real-time data transmission, the PLL loop filters must be optimized to minimize regenerated clock jitter. A good grade of mylar capacitor is recommended as connected to Pins 4 and 5 of the NE564 A simple pair of shunt-connected loop filter caps of 0.33μF to 0.76μF was found to be adequate.

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

AN182

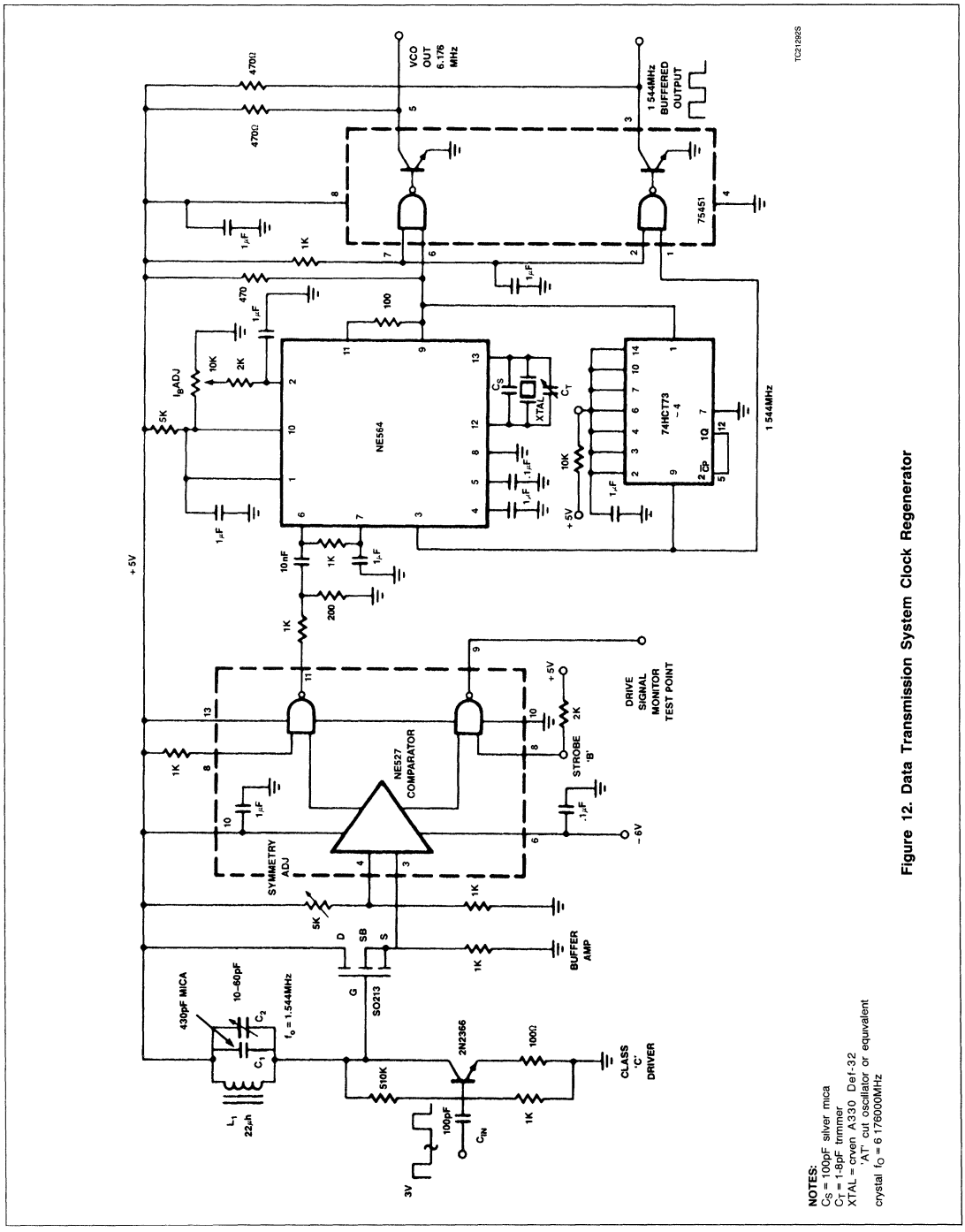
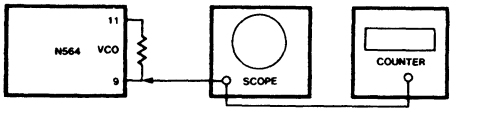


Figure 12. Data Transmission System Clock Regenerator

NOTES:
C_S = 100pF silver mica
C_T = 1-8pF trimmer
XTAL = crven A330 Def-32
'AT' cut oscillator or equivalent
crystal f_O = 6 176000MHz

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

AN182



NOTE:
Check VCO free-running frequency and output waveshape

Figure 13. Check VCO Free-Running Frequency and Output Waveshape

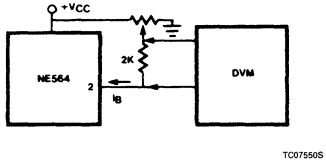


Figure 14

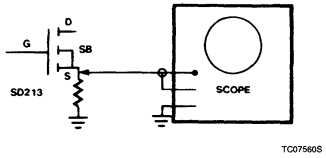


Figure 15

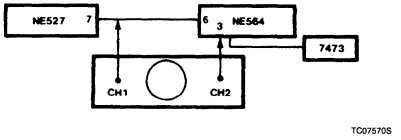


Figure 16

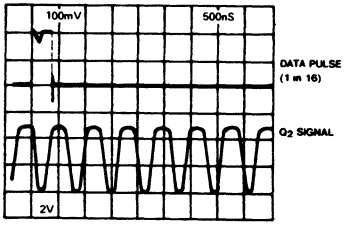


Figure 17. Ringing Circuit Response (1 Data Pulse in 16)

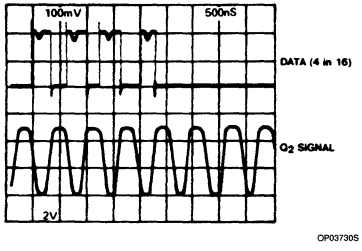


Figure 18. Ringing Circuit Response (4 Data Pulses in 16)

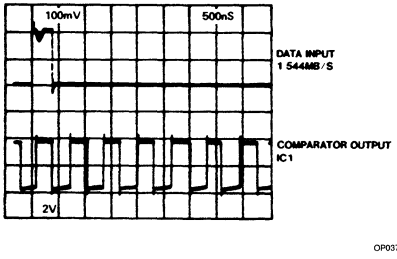


Figure 19. Ringing Circuit to Square Wave Conversion

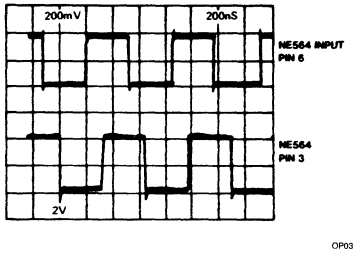


Figure 20. Phase Comparator Signals (in Lock)

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

AN182

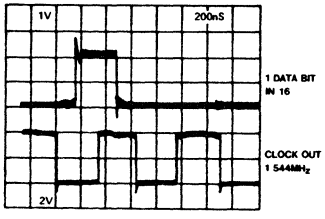


Figure 21. Regenerated Clock Signals

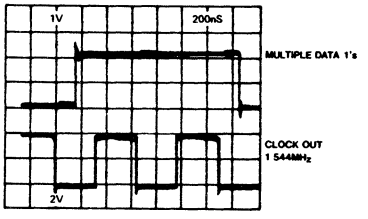


Figure 22. Regenerated Clock Signals

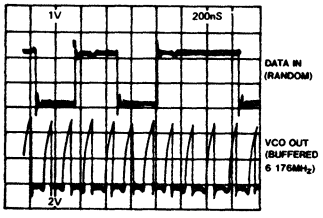


Figure 23. Regenerated Clock Signals Relative to NE564 VCO Signal

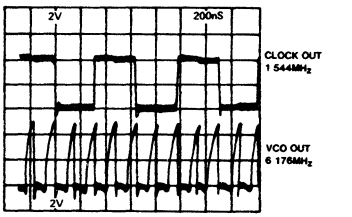


Figure 24. Regenerated Clock Signal Relative to NE564 VCO Signal

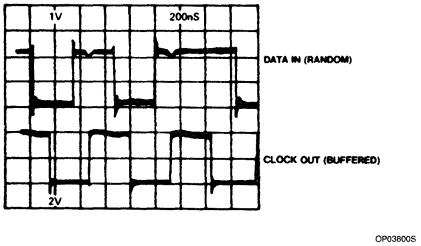


Figure 25. Regenerated Clock Signal Relative to Random NRZ Data Signal

NOTES:
1. Recent versions of this circuit no longer require series capacitors C_C and C_T See Figure 12
2. Input levels to the NE564 have been reduced for this application to ≃ 800mVp-p. See Figure 12
3. Improved operation regarding clock jitter is obtained by carefully decoupling the divider counter ICs and the PLL's V_{CC} line This is accomplished by adding a small series "R" into the V_{CC} line with the bypass capacitor to ground

References

1. "Fourier Analysis" by Hwei P. Hsu. Simon & Schuster Tech Outlines
2. "Pulse and Digital Circuits" by Millman and Taub McGraw Hill
3. "Phaselock Techniques" by Floyd M. Gardner Wiley, 1966

Signetics

NE/SE565
Phase-Locked Loop

Product Specification

Linear Products

DESCRIPTION

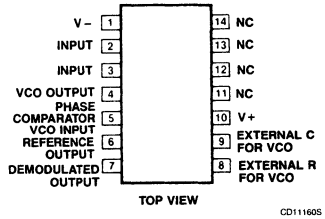
The NE/SE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low pass filter as shown in the Block Diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (±6V to ±12V)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from $< \pm 1\%$ to $> \pm 60\%$**
- **Frequency adjustable over 10 to 1 range with same capacitor**

PIN CONFIGURATIONS

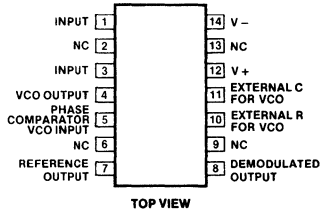
F, N Packages



TOP VIEW

CD11160S

D Package[1]



TOP VIEW

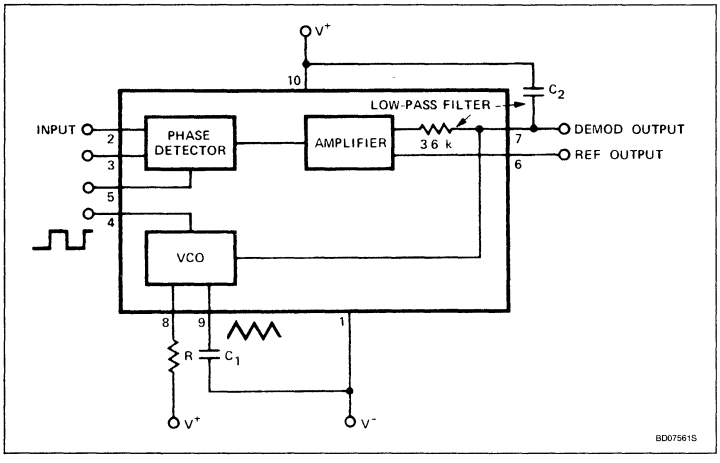
CD11170S

NOTE:
1 SO and non-standard pin out

APPLICATIONS

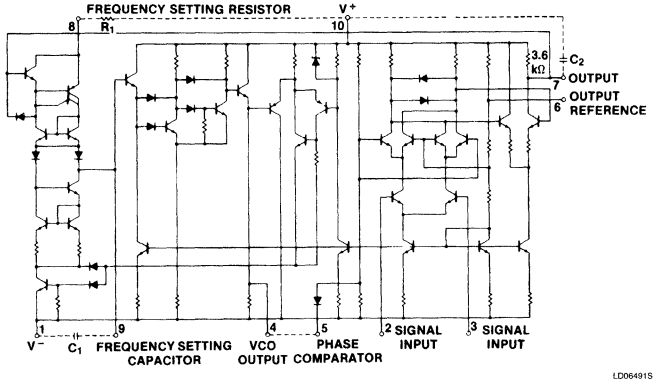
- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wide-band FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

BLOCK DIAGRAM



BD07561S

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE565D
14-Pin Cerdip	0 to +70°C	NE565F
14-Pin Plastic DIP	0 to +70°C	NE565N
14-Pin Cerdip	−55°C to +125°C	SE565F
14-Pin Plastic DIP	−55°C to +125°C	SE565N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C, unless otherwise specified

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE565 SE565	 0 to +70 −55 to +125	 °C °C
P_D	Power dissipation	300	mW

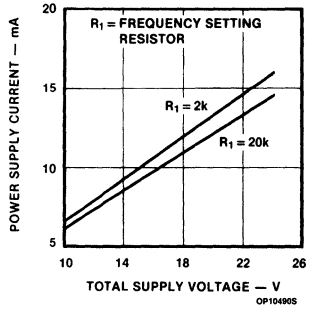
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
			Min	Typ	Max	Min	Typ	Max	
Supply requirements									
V_{CC}	Supply voltage		±6		±12	±6		±12	V
I_{CC}	Supply current			8	12.5		8	12.5	mA
Input characteristics									
	Input impedance[1]		7	10		5	10		kΩ
	Input level required for tracking	f_O = 50kHz, ±10% frequency deviation	10			10			mV_{RMS}
VCO characteristics									
f_C	Center frequency Maximum value distribution[2]	 Distribution taken about f_O = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	300 −10	500 0	 +10	 −30	500 0	 +30	kHz %
	Drift with temperature Drift with supply voltage	f_O = 50kHz f_O = 50kHz, V_{CC} = ±6 to ±7V		500 0.1	 1.0		600 0.2	 1.5	ppm/°C %/V
	Triangle wave output voltage level linearity		1.9	2.4 0.2	3	1.9	2.4 0.5	3	V_{P-P} %
	Square wave logical "1" output voltage logical "0" output voltage	 f_O = 50kHz f_O = 50kHz	 +4.9	 +5.2 −0.2	 +0.2	 +4.9	 +5.2 −0.2	 +0.2	 V V
	Duty cycle	f_O = 50kHz	45	50	55	40	50	60	%
t_R	Rise time			20	100		20		ns
t_F	Fall time			50	200		50		ns
I_{SINK}	Output current (sink)		0.6	1		0.6	1		mA
I_{SOURCE}	Output current (source)		5	10		5	10		mA
Demodulated output characteristics									
V_{OUT}	Output voltage level	Measured at Pin 7	4.25	4.5	4.75	4.0	4.5	5 0	V
	Maximum voltage swing[3]			2			2		V_{P-P}
	Output voltage swing	±10% frequency deviation	250	300		200	300		mV_{P-P}
THD	Total harmonic distortion			0.2	0.75		0.4	1.5	%
	Output impedance[4]			3.6			3.6		kΩ
V_{OS}	Offset voltage (V6 − V7)			30	100		50	200	mV
	Offset voltage vs temperature (drift)			50			100		μV/°C
	AM rejection		30	40			40		dB

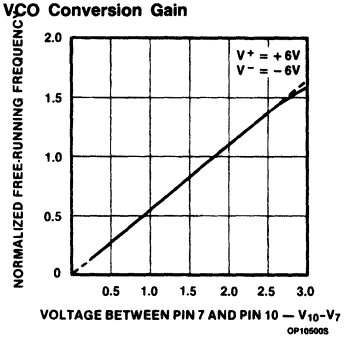
NOTES:
1. Both input terminals (Pins 2 and 3) must receive identical DC bias. This bias may range from 0V to −4V
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

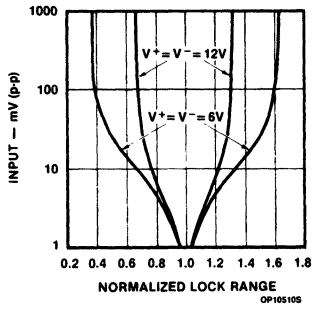
Power Supply Current as a Function of Supply Voltage



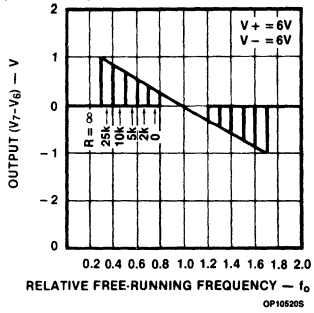
VCO Conversion Gain



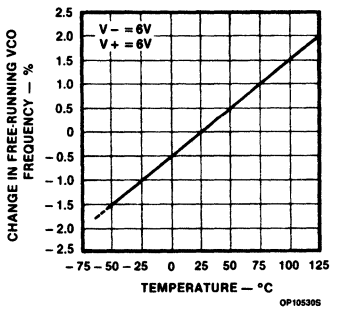
Lock Range as a Function of Input Voltage



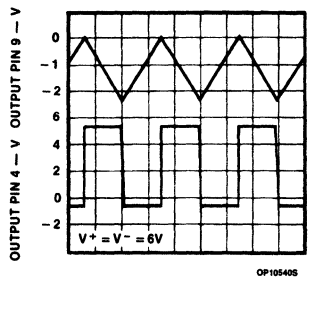
Lock Range as a Function of Gain Setting Resistance (Pins 6 – 7)



Change in Free-Running VCO Frequency as a Function of Temperature



VCO Output Waveform



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO:

$$f_O \simeq \frac{1}{4R_1C_1} \text{ in Hz}$$

Lock range: $f_L = \pm \frac{8f_O}{V_{CC}}$ in Hz

Capture range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase-Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average DC level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_O \simeq \frac{1.2}{4R_1C_1}$$

and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000Ω with an optimum value on the order of 4000Ω. The source can be direct coupled if the DC resistances seen from Pins 2 and 3 are equal and there is no DC voltage difference between the pins. A short between Pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a DC reference voltage that is close to the DC potential of the demodulated output (Pin 7). Thus, if a resistance is connected between Pins 6 and 7, the gain of the output stage can be reduced with little change in the DC voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_O to approximately ±20% of f_O (at ±6V).

A small capacitor (typically 0.001μF) should be connected between Pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between Pin 7 and the positive supply, and an internal resistance of approximately 3600Ω.

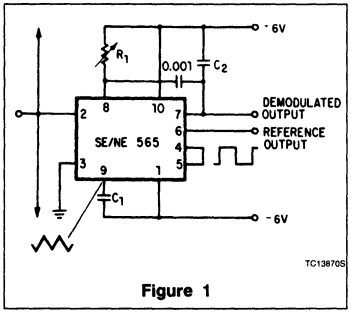


Figure 1

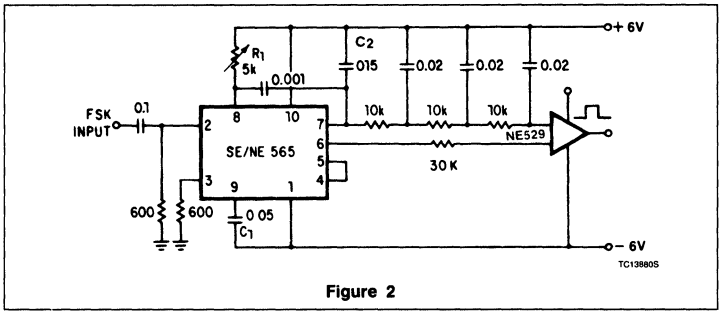


Figure 2

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" to "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

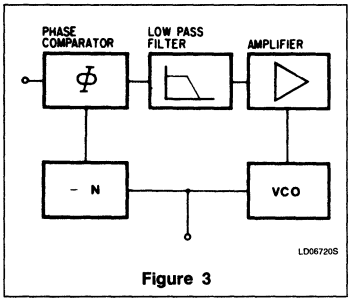


Figure 3

The input connection is typical for cases where a DC voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect at 600Ω input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at Pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

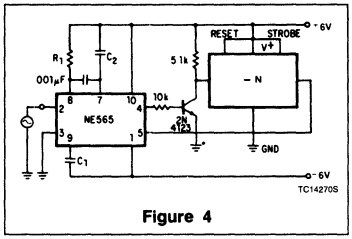


Figure 4

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this, a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase-Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (Pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000Ω.

Phase-Locked Loop NE/SE565

The Phase-Locked Loop is tuned to 67kHz with a 5000Ω potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (Pin 7) passes through a three-stage low pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at Pin 7, thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz

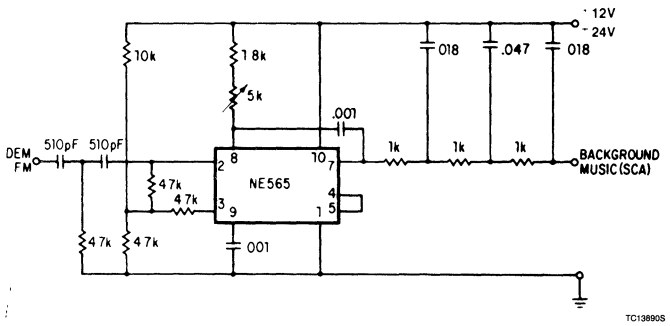


Figure 5

AN183
Circuit Description of the NE565 PLL

Application Note

CIRCUIT DESCRIPTION OF THE NE565 PLL

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. The loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 1. I_1 is the charging current created by the application of the control voltage V_C. In the initial state, Q_3 is off and the current I_1 charges capacitor C_1 through the diode D_2. When the voltage on C_1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q_3. This provides a current sink and essentially grounds the emitters of Q_1 and Q_2. The charging current I_1 now flows through D_1, Q_1 and Q_3 to ground. Since the base-emitter voltage of Q_2 is the same as that of Q_1, an equal current flows through Q_2. This discharges the capacitor C_1 until the lower triggering threshold is reached, at which point the cycle repeats itself. Because the capacitor C_1 is charged and discharged with the constant current I_1, the VCO produces a triangle waveform as well as the square wave output of the Schmitt trigger.

The complete circuit for the 565 is shown in Figure 2. Transistors $Q_1 - Q_7$ and diodes $D_1 - D_3$ form the precision current source. The base of Q_1 is the control voltage input to the VCO. This voltage is transferred to Pin 8 where it is applied across the external resistor R_1. This develops a current through R_1 which enters Pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q_1 base current, all the current that enters Pin 8 appears at the anodes of diodes D_2 and D_3. When Q_8 (controlled by the Schmitt trigger) is on, D_3 is reverse-biased and all the current flows through D_2 to the duplicating current source $Q_5 - Q_7$, $R_2 - R_3$ and appears as the capacitor discharge current at the collector of Q_5. When Q_8 is off, the duplicating current source $Q_5 - Q_7$, $R_2 - R_3$ floats and the charging current passes through D_3 to charge C_1.

The Schmitt trigger (Q_{11}, Q_{12}) is driven from the capacitor triangle waveform by the emitter-follower Q_9. Diodes $D_6 - D_9$ prevent saturation of Q_{11} and Q_{12}, enhancing the switching speed. The Schmitt trigger output is buffered by emitter-follower Q_{13} and is brought out to Pin 4, and is also connected back to the current source by the differential amplifier ($Q_{14} - Q_{16}$).

When operated from dual symmetrical supplies, the square wave on Pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below the positive supply. The triangle waveform on Pin 9 is approximately centered between the positive and negative supplies and has an amplitude of 2V with supply voltages of ± 5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase comparator is again of the doubly-balanced modulator type. Transistors Q_{20} and Q_{24} form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q_{20} and Q_{24} through external resistors to ground.

The switching stage Q_{18}, Q_{19}, Q_{22} and Q_{23} is driven from the Schmitt trigger via Pin 5 and D_{11}. Diodes D_{12} and D_{13} limit the phase comparator output, and differential amplifier Q_{26} and Q_{27} provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to Pin 7) and the collector resistance R_{24} (typically 3.6kΩ). The voltage on Pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q_1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is nominally equal to the output voltage on Pin 7. This allows differential stages to be both biased and driven by connecting them to Pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R_1 and C_1 and is given approximately by

$$f_O' \simeq \frac{1.2}{4R_1C_1} \qquad (1)$$

When the phase comparator is in the limiting mode ($V_{IN} \geq 200mV_{P\text{-}P}$), the lock range can be calculated from the expression:

$$2\omega_L = 2K_oK_dA\theta_d \qquad (2)$$

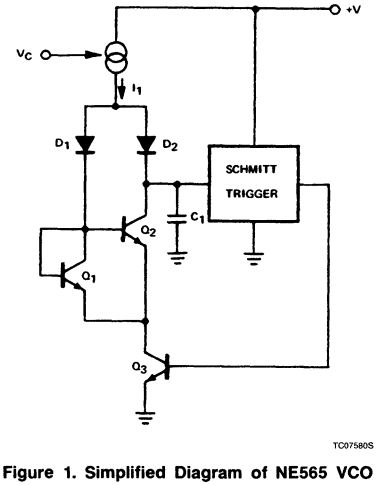


Figure 1. Simplified Diagram of NE565 VCO

Circuit Description of the NE565 PLL AN183

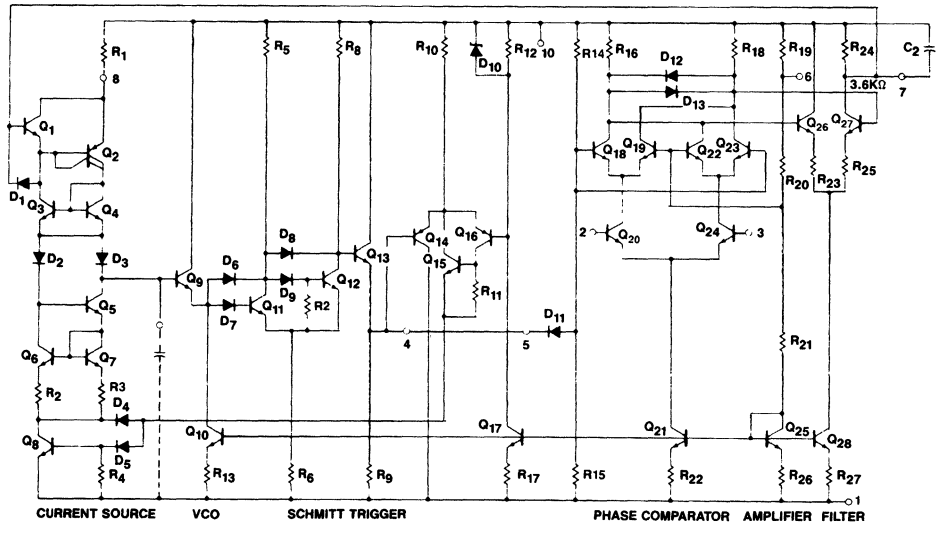


Figure 2. Circuit Diagram of 565

where K_o is the VCO conversion gain, K_d is the phase comparator's conversion gain, A is the amplifier gain, and θ_d is the maximum phase error over which the loop can remain in lock. Specific values for the terms of Equation 2 for the 565 are

$$K_d = \frac{1.4}{\pi} V/rad \quad (3)$$

$$A = 1.4 \quad (4)$$

$$e_d = \frac{\pi}{2} rad \quad (5)$$

$$K_o = \frac{50 f_O'}{V_{CC}} \frac{rad}{Volt\text{-}sec} \quad (6)$$

where V_{CC} is the total supply voltage applied to the circuit.

The tracking range for the 565 then becomes:

$$f_L \cong \pm \frac{\omega_L}{2\pi} \cong \pm \frac{8 f_O}{V_{CC}} Hz \quad (7)$$

to each side of the free-running frequency, or a total lock range of:

$$2f_L \cong \pm \frac{16 f_O}{V_{CC}} Hz \quad (8)$$

The capture range, over which the loop can acquire lock with the input signal, is given approximately by:

$$2\omega_C \cong 2\sqrt{\frac{\omega_L}{\tau}} \quad (9)$$

where ω_L is the one-sided tracking range

$$\omega_L = 2\pi f_L \quad (10)$$

and τ is the time constant of the loop filter

$$\tau = RC_2 \quad (11)$$

The lock-in range can be written as:

$$f_C \cong \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}} = \pm \frac{1}{2\pi} \sqrt{\frac{32\pi f_O'}{V_{CC}}} \quad (12)$$

to each side of the free-running frequency or a total capture range of:

$$f_C \cong \frac{1}{\pi} \sqrt{\frac{32\pi f_O'}{\tau V_{CC}}} \quad (13)$$

This approximation works well for narrow capture ranges ($f_C = \frac{1}{3} f_L$) but becomes too large as the limiting case is approached ($f_C = f_L$).

When it is desired to operate the 565 out of its limiting mode ($V_{IN} < 200mV_{P\text{-}P}$ or $32mV_{RMS}$), K_d can be estimated from the graph in Figure 3 for the specific input voltage anticipated. The previous calculations for the lock and capture ranges remain valid with the new value of K_d from the graph being used to replace the K_dA product in Equation 2. In Figure 3, the DC amplifier gain A has been included in the K_d value.

Circuit Description of the NE565 PLL AN183

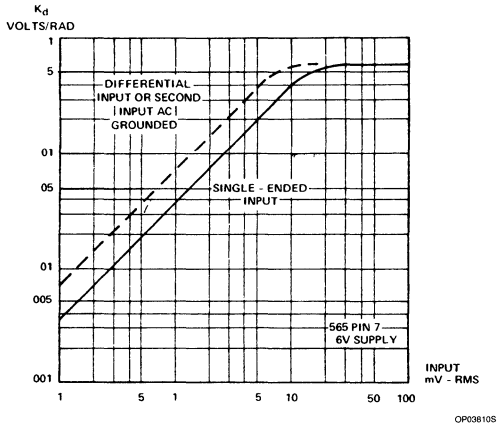


Figure 3. Phase Comparator's Conversion Gain, K_d, for the 565 as a Function of Input Signal Amplitude

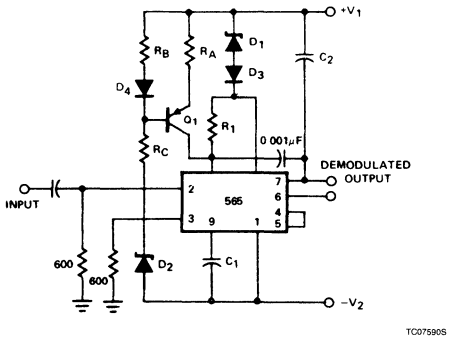


Figure 4. Narrow Bandwidth FM Demodulator Using the 565

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into Pin 8 and increase the value of R_1. One scheme for this is shown in Figure 4. The basis for this scheme is the fact that the output voltage controls only the current through R_1, while the current through Q_1 remains constant. Thus, if most of the charging current is due to Q_1 the total current can be varied only a small amount due to the small change in current through R_1. Consequently, the VCO can track the input signal over a small frequency range, yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

Diode D_1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available D_4 is a diode which should be matched to the emitter-base junction of Q_1 for temperature stability In addition, D_1 and D_2 should have the same breakdown voltages and D_3 and D_4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across Pins 10 and 1 of the phase-locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The free-running frequency can be found by·

$$f_O' \simeq \frac{2R_B}{(R_B + R_C)R_AC_1} + \frac{1}{4R_1C_1} \text{ Hz} \quad (14)$$

and the total range is given by:

$$2f_L \cong \frac{22.4V_D(R_B + R_C)R_Af_O'}{(|V_1| + |V_2| - V_z - V_D)[8R_BR_1 + R_A(R_B + R_C)]} \text{Hz} \quad (15)$$

where V_D is the forward-biased diode voltage ($\simeq$0.7V), V_Z is the zener diode breakdown voltage, V_1 is the positive supply voltage, and V_2 is the negative supply voltage.

When the output excursion at Pin 7 need be only a volt or so, diodes D_1, D_2 and D_3 may be replaced by short circuits.

The value of R_1 can be selected to give a prescribed output voltage for a given frequency deviation

$$R_1 = \frac{R_A(R_B + R_C)f_O'}{R_B(|V_1| + |V_2| - 0.7)\Delta f} \quad (16)$$

where Δf is the desired frequency deviation per volt of output

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For best temperature stability, diode D_1 should be a base-collector shorted transistor of the same type as Q_1.

When the 565 is connected normally, feedback to the VCO from the phase comparator is internal That is, an amplifier makes the Pin 8 voltage track the Pin 7 (phase comparator output) voltage. Since the capacitor C_1 charge current is determined by the current through resistance R_1, the frequency is a function of the voltage at Pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into Pin 8 is no longer a function of the Pin 8 voltage but only of the Pin 7 voltage This makes a greater charge-discharge current variation possible, allowing a greater lock range Figure 5 shows such a circuit in which the μA741 operational amplifier is set for a differential gain of 5, feeding current to Pin 8 through the 33kΩ resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the designer should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500μA, which also specifies the Pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

Many times it would be advantageous to be able to break the feedback connection between the output (Pin 7) and the control voltage terminal (Q_1) of the VCO. This can be easily done once it is seen that it is the *current* into Pin 8 which controls the VCO frequency. Replacing the external resistor R_1 with a current source, such as in Figure 6, effectively breaks the internal voltage feedback connection. The current flowing into Pin 8 is now independent of the voltage on Pin 8. The output voltage (on Pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 6 This scheme allows the addition of enough gain for the loop to stay in lock over a 100:1 frequency range or, conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0° and 180°. In addition, it is now possible to do special filtering to improve the performance in certain applications For in-

Circuit Description of the NE565 PLL AN183

stance, in frequency multiplication applications, it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

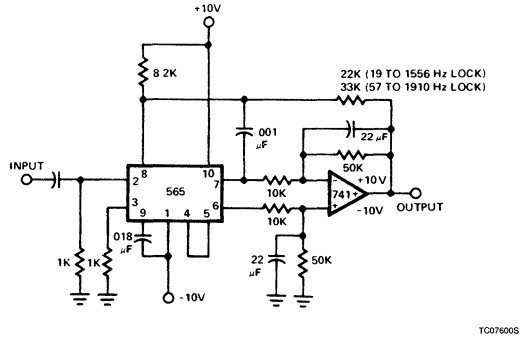


Figure 5. Expanded Lock Range Configuration for the 565

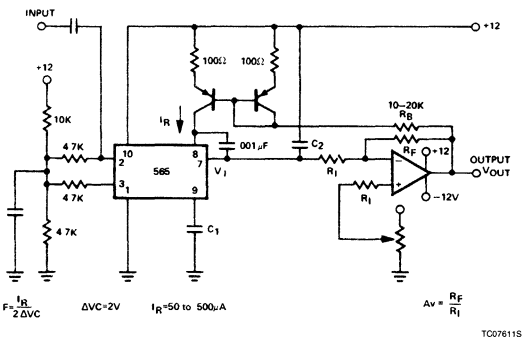


Figure 6. Increased Loop Gain and Lock Range for the 565

AN184
Typical Applications with NE565

Application Note

FSK DEMODULATION

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal

FSK Demodulation with the 565

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 1. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output (Pin 7).

The loop filter capacitor C_2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency components. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300 baud or bits per second, or 150Hz). The free-running frequency should be adjusted (with R_1) so that the DC voltage level at the output is the same as that at Pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6.

The input connection is typical for cases where a DC voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance).

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 2. Here, a constant current is injected into Pin 8 by means of transistor Q_1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift The basis for this scheme is the fact that the output voltage (control voltage for the VCO) controls

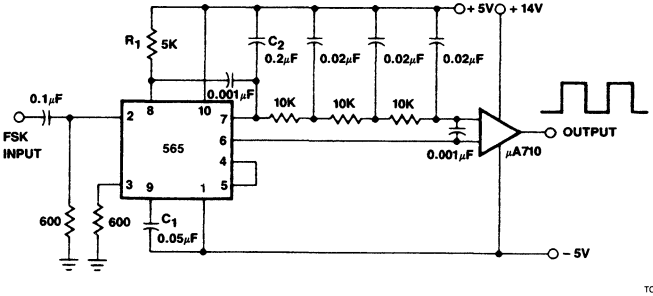


Figure 1. FSK Decoder Using the 565

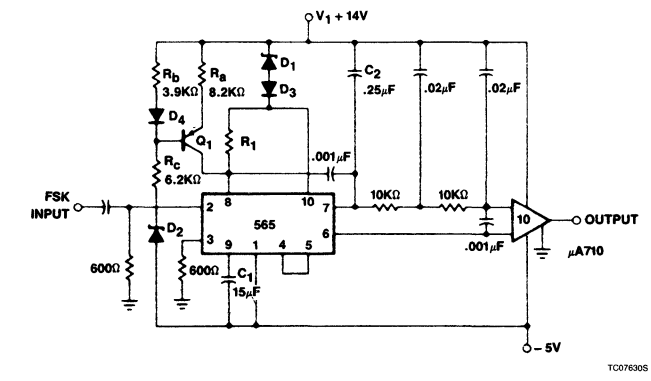
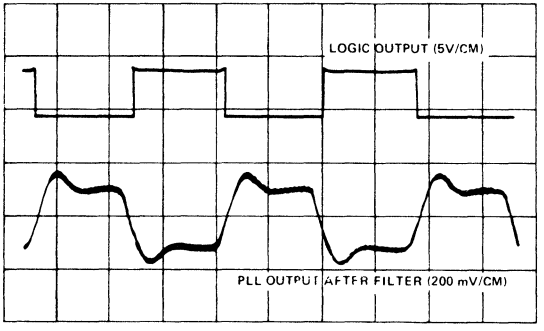
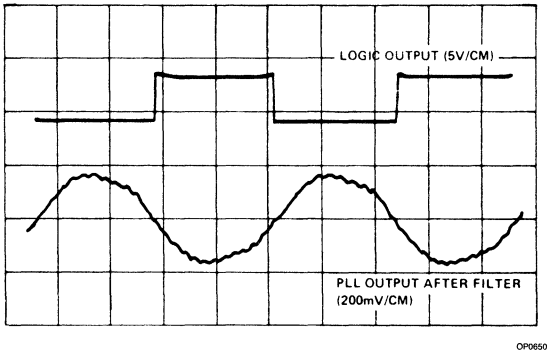


Figure 2. FSK Decoder With Expanded 565 Output Voltage Range

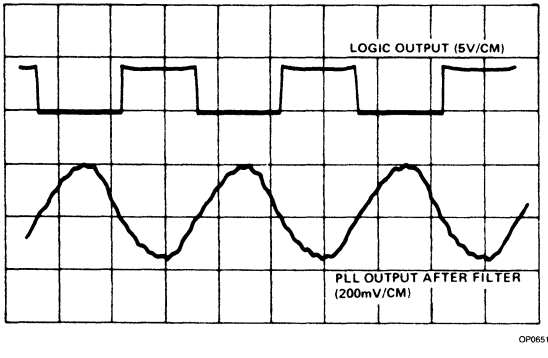
only the current through R_1, while the current through Q_1 remains constant. Thus, if most of the capacitor charging current is due to Q_1, the current variation due to R_1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25μF loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs. Figure 3 shows the output of the μA710 comparator and the output of the 565 phase-locked loop.



a. 100 Baud



b. 200 Baud



c. 300 Baud

Figure 3

Typical Applications with NE565

AN184

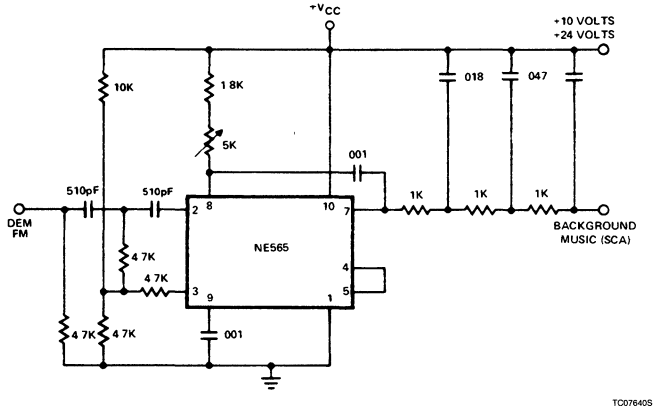


Figure 4. SCA Decoder

SCA Demodulator Using the 565

This application involves demodulation of a frequency-modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (Subsidiary Carrier Authorization or storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency-modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 4 to a point between the FM discriminator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial-free background music.

4

Signetics

NE/SE566
Function Generator

Product Specification

Linear Products

DESCRIPTION

The NE/SE566 Function Generator is a voltage-controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten-to-one frequency range by proper selection of an external resistance and modulated over a ten-to-one range by the control voltage, with exceptional linearity.

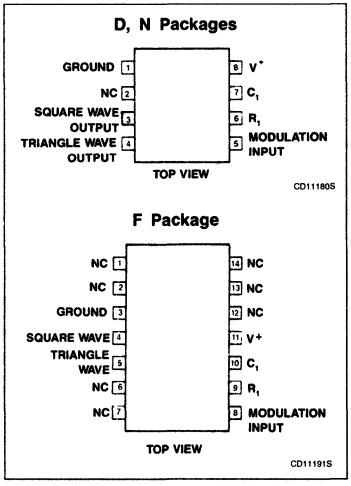
FEATURES

- **Wide range of operating voltage (up to 24V; single or dual)**
- **High linearity of modulation**
- **Highly stable center frequency (200ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10-to-1 range with same capacitor**

APPLICATIONS

- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

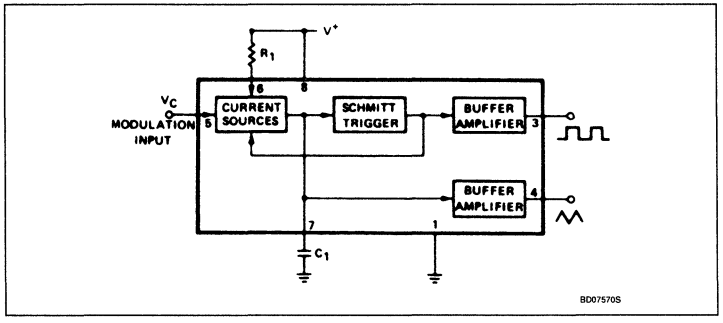
PIN CONFIGURATIONS



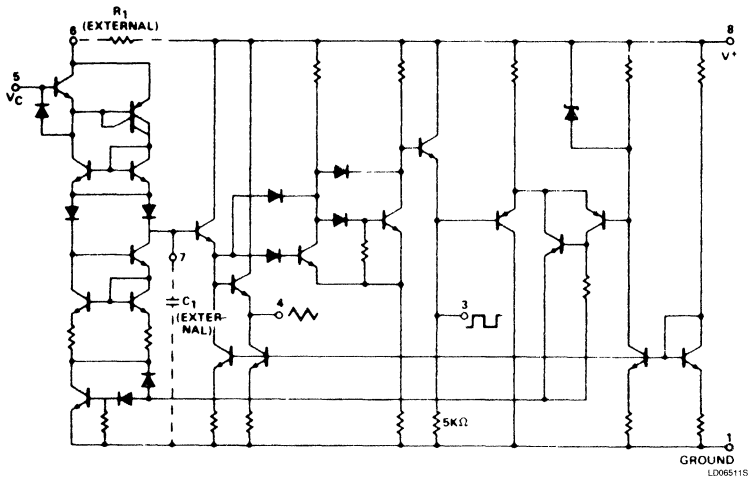
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE566D
14-Pin Cerdip	0 to +70°C	NE566F
8-Pin Plastic DIP	0 to +70°C	NE566N
14-Pin Cerdip	−55°C to +125°C	SE566F
8-Pin Plastic DIP	−55°C to +125°C	SE566N

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range		
	NE566	0 to +70	°C
	SE566	−55 to +125	°C
P_D	Power dissipation	300	mW

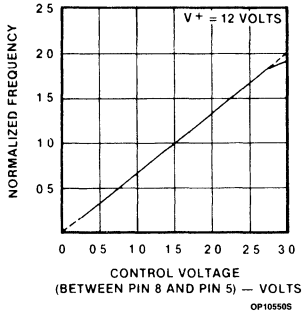
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	SE566			NE566			UNIT
		Min	Typ	Max	Min	Typ	Max	
General								
T_A	Operating ambient temperature range	−55		125	0		70	°C
V_{CC}	Operating supply voltage	±6		±12	±6		±12	V
I_{CC}	Operating supply current		7	12.5		7	12.5	mA
VCO[1]								
f_{MAX}	Maximum operating frequency		1			1		MHz
	Frequency drift with temperature		500			600		ppm/°C
	Frequency drift with supply voltage		0.1	1		0.2	2	%/V
	Control terminal input impedance[2]		1			1		MΩ
	FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
	Maximum sweep rate		1			1		MHz
	Sweep range		10:1			10:1		
Output								
	Triangle wave output							
	impedance		50			50		Ω
	voltage	1.9	2.4		1.9	2.4		V_{P-P}
	linearity		0.2			0.5		%
	Square wave input							
	impedance		50			50		Ω
	voltage	5	5.4		5	5.4		V_{P-P}
	duty Cycle	45	50	55	40	50	60	%
t_R	Rise time		20			20		ns
t_F	Fall Time		50			50		ns

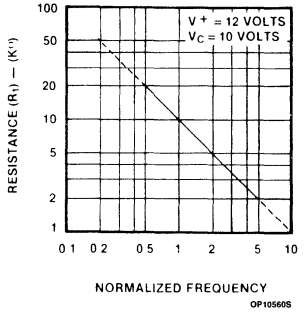
NOTES:
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
2. The bias voltage (V_C) applied to the control terminal (Pin 5) should be in the range $\frac{3}{4}V+ \leq V_C \leq V+$.

TYPICAL PERFORMANCE CHARACTERISTICS

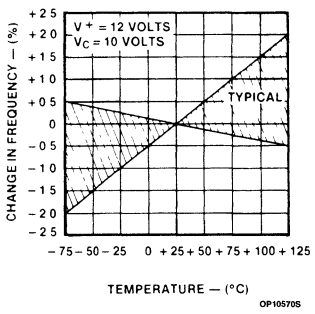
Normalized Frequency as a Function of Control Voltage



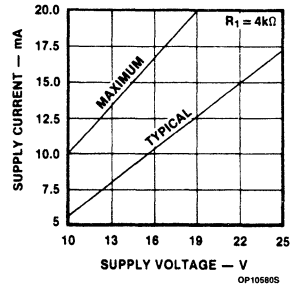
Normalized Frequency as a Function of Resistance (R1)



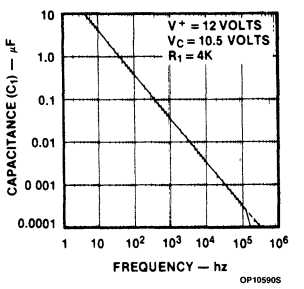
Change in Frequency as a Function of Temperature



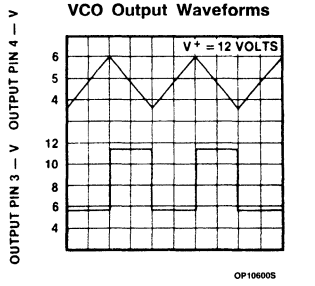
Power Supply Current as a Function of Supply Voltage



Frequency as a Function of Capacitance (C1)



VCO Output Waveforms



OPERATING INSTRUCTIONS

The NE/SE566 Function Generator is a general purpose voltage-controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (Pin 5) must be biased externally with a voltage (V_C) in the range

$$\tfrac{3}{4}V+ \leqslant V_C \leqslant V+$$

where V_{CC} is the total supply voltage In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then AC coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate DC bias voltage is applied to the control terminal The frequency is given approximately by

$$f_O = \frac{2[(V+) - (V_C)]}{R_1 C_1 V+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$

A small capacitor (typically 0 001μF) should be connected between Pins 5 and 6 to eliminate possible oscillation in the control current source

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply as shown in Figure 2 In this case the square wave output has the proper DC levels for logic circuitry. RTL can be driven directly from Pin 3. For DTL or TTL gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between Pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for TTL circuitry which requires a fast fall time (< 50ns) and a large current sinking capability

Function Generator NE/SE566

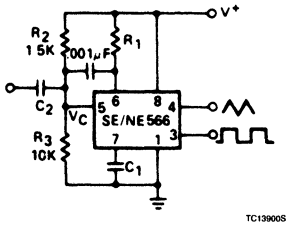


Figure 1

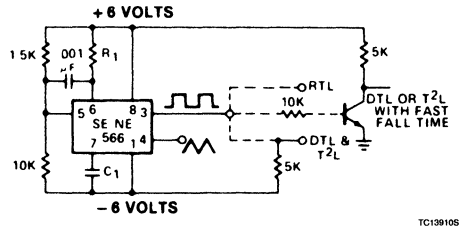


Figure 2

AN185
Circuit Description of the NE566

Application Note

CIRCUIT DESCRIPTION OF THE 566 PLL

The 566 is the voltage-controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 1. Transistor Q_{18} provides a buffered triangle waveform output. (The triangle waveform is available at capacitor C_1 also, but any current drawn from Pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q_{19} by Pin 4 The circuit will operate at frequencies up to 1MHz and may be programmed by the voltage applied on the control terminal (Pin 5), by injecting current into Pin 6, or by changing the value of the external resistor and capacitor (R_1 and C_1).

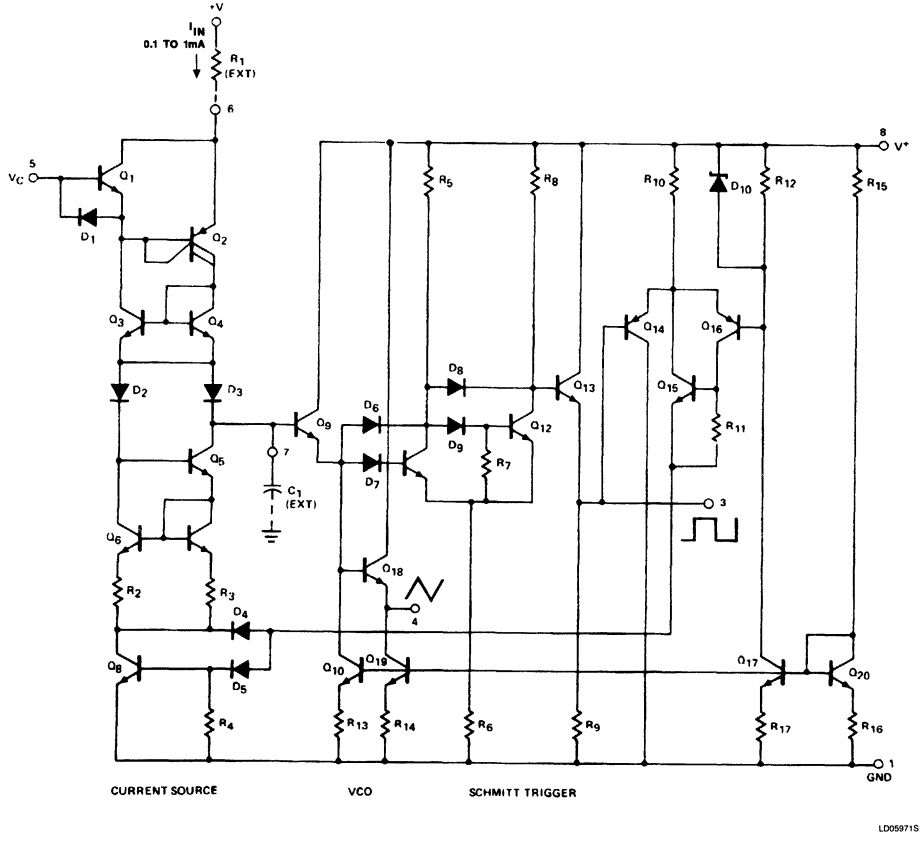


Figure 1. Circuit Diagram of the NE566

Signetics

AN186
Waveform Generators With the NE566

Application Note

Linear Products

WAVEFORM GENERATORS

The oscillator portion of many of the PLLs can be used as a precision, voltage-controllable waveform generator. Specifically, the 566 Function Generator contains the oscillator of the 565 PLL. Most of the applications which follow are designs using the 566. Many of these designs can be modified slightly to utilize the oscillator section of the 564 if higher frequency performance is desired.

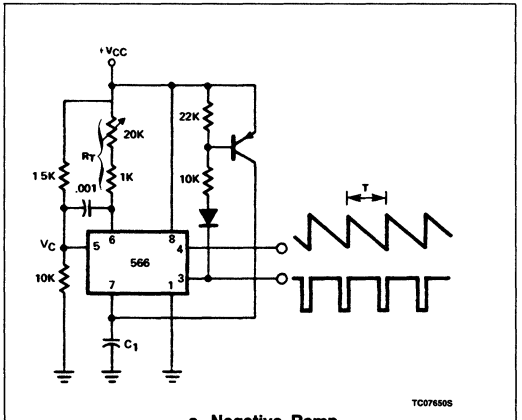
Ramp Generators

Figure 1 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the Pin 3 output rapidly discharges C_1 at the end of the charging period so that charging can resume instantaneously. The PNP transistor of the negative ramp generator likewise rapidly charges the timing capacitor C_1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period

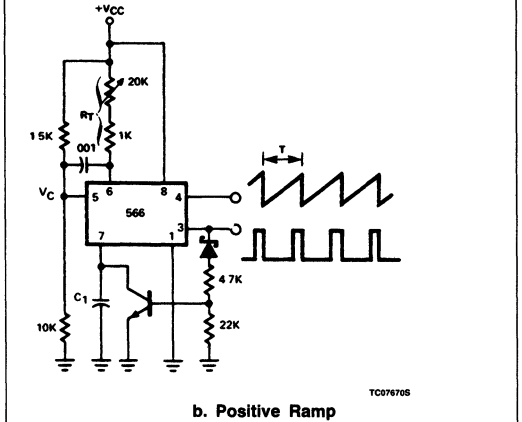
T is $\frac{1}{2f_O}$

where f_O is the 566 free-running frequency in normal operation. Therefore,

$$T = \frac{1}{2f_O} = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \quad (1)$$

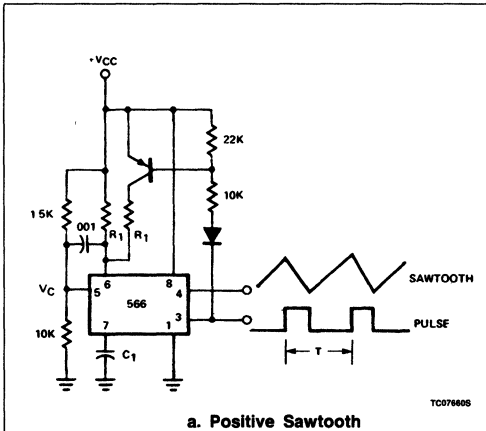


a. Negative Ramp

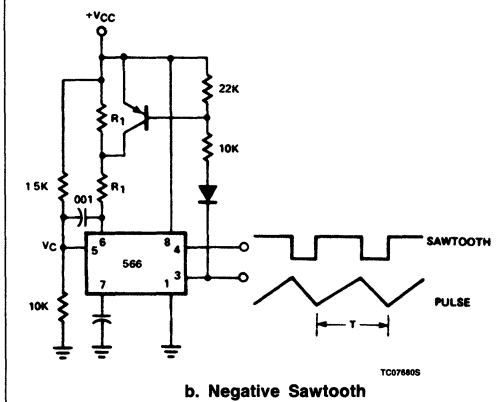


b. Positive Ramp

Figure 1. Ramp Generators



a. Positive Sawtooth



b. Negative Sawtooth

Figure 2. Sawtooth and Pulse Generators

Waveform Generators With the NE566 — AN186

where V_C is the bias voltage at Pin 5 and R_T is the total resistance between Pin 6 and V_{CC}. Note that a short pulse is available at Pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

Sawtooth and Pulse Generator

Figure 2 shows how the Pin 3 output of the 566 can be used to provide different charge and discharge currents for C_1 so that a sawtooth output is available at Pin 4 and a pulse at Pin 3. The PNP transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

$$T = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \quad (2)$$

where R_T is the combined resistance between Pin 6 and V_{CC} for the interval considered.

Triangle-to-Sine Converters

Conversion of triangle wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

In Figure 3, the non-linear $I_{DS} \cdot V_{DS}$ transfer characteristic of a P-channel junction FET is used to shape the triangle waveform.

The amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

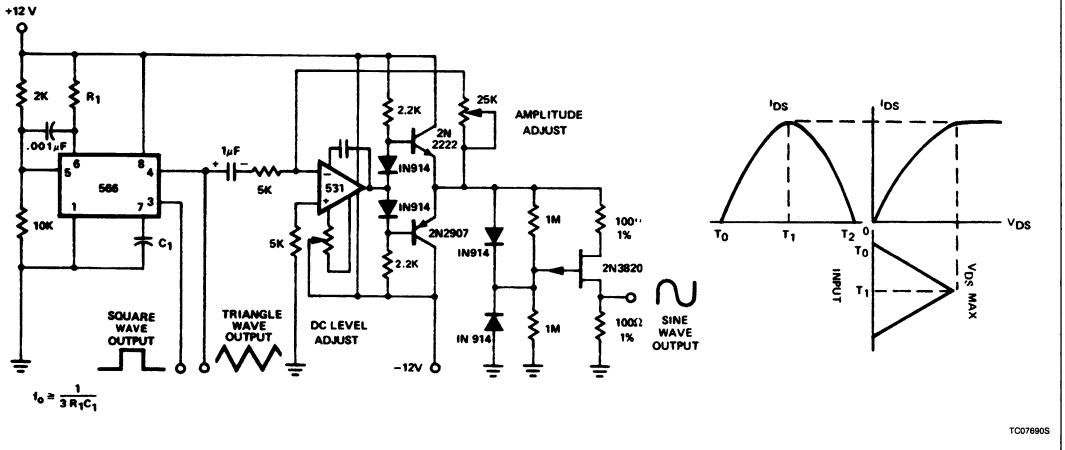


Figure 3. Triangle-to-Sine Converters

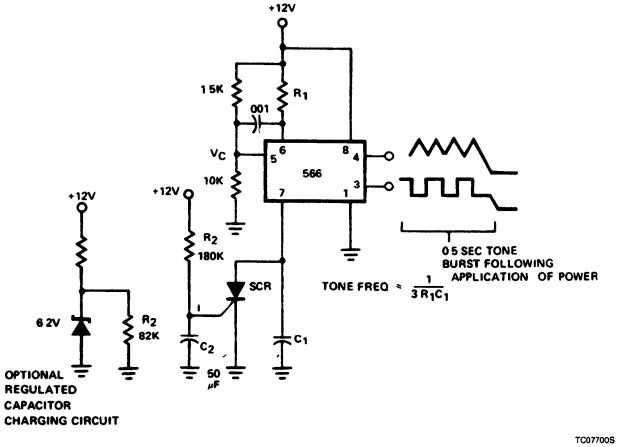
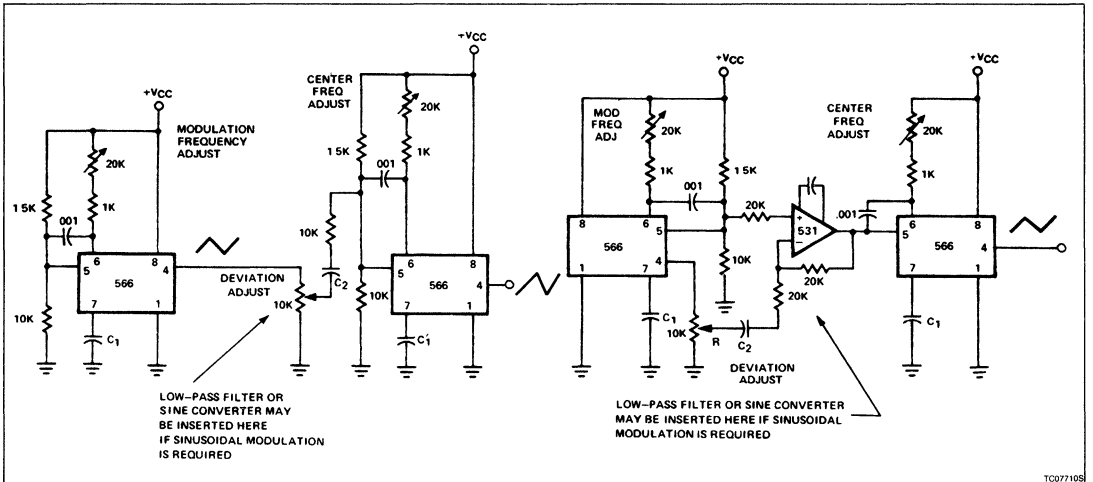


Figure 4. Single-Burst Tone Generator

Waveform Generators With the NE566 AN186



a. Small Frequency Deviations to ±20% **b. Large Frequency Deviations to ±100%**

Figure 5. Frequency-Modulated Generators

Single-Tone Burst Generator

Figure 4 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is a communications network alert signal. Cessation of the tone is accomplished at the SCR, which shunts the timing capacitor C_1 charge current when activated. The SCR is gated on when C_2 charges up to the gate voltage which occurs in 0.5 seconds. Since only 70μA are available for triggering, the SC must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R_2 (and increasing C_2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R_2, $R_2' = 82k\Omega$.

If the SCR is replaced by an NPN transistor, the tone can be switched on and off at will at the transistor base terminal.

Low Frequency FM Generators

Figure 5 shows FM generators for low frequency (less than 0.5MHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C_1 selects the modulation frequency adjustment range and C_1' selects the center frequency. Capacitor C_2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

Signetics

NE/SE567
Tone Decoder/Phase-Locked Loop

Product Specification

Linear Products

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

FEATURES

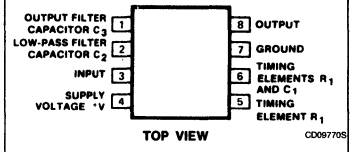
- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14%)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20–to-1 range with an external resistor**
- **Military processing available**

APPLICATIONS

- **Touch-Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

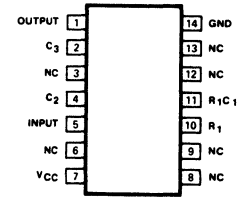
PIN CONFIGURATIONS

FE, D, N Packages



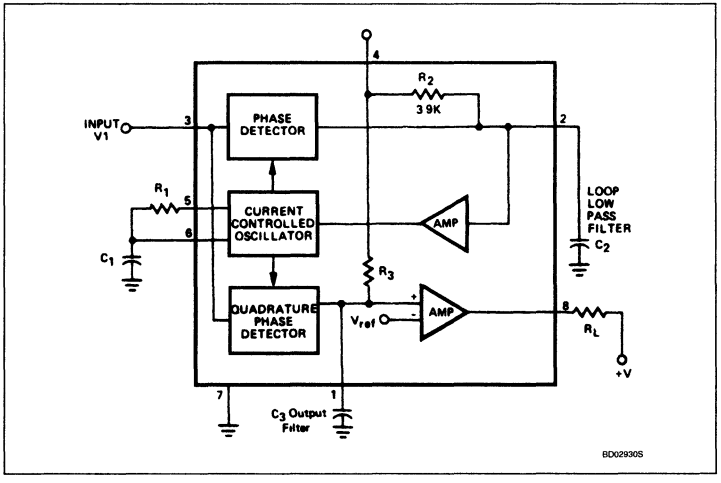
TOP VIEW CD09770S

F Package



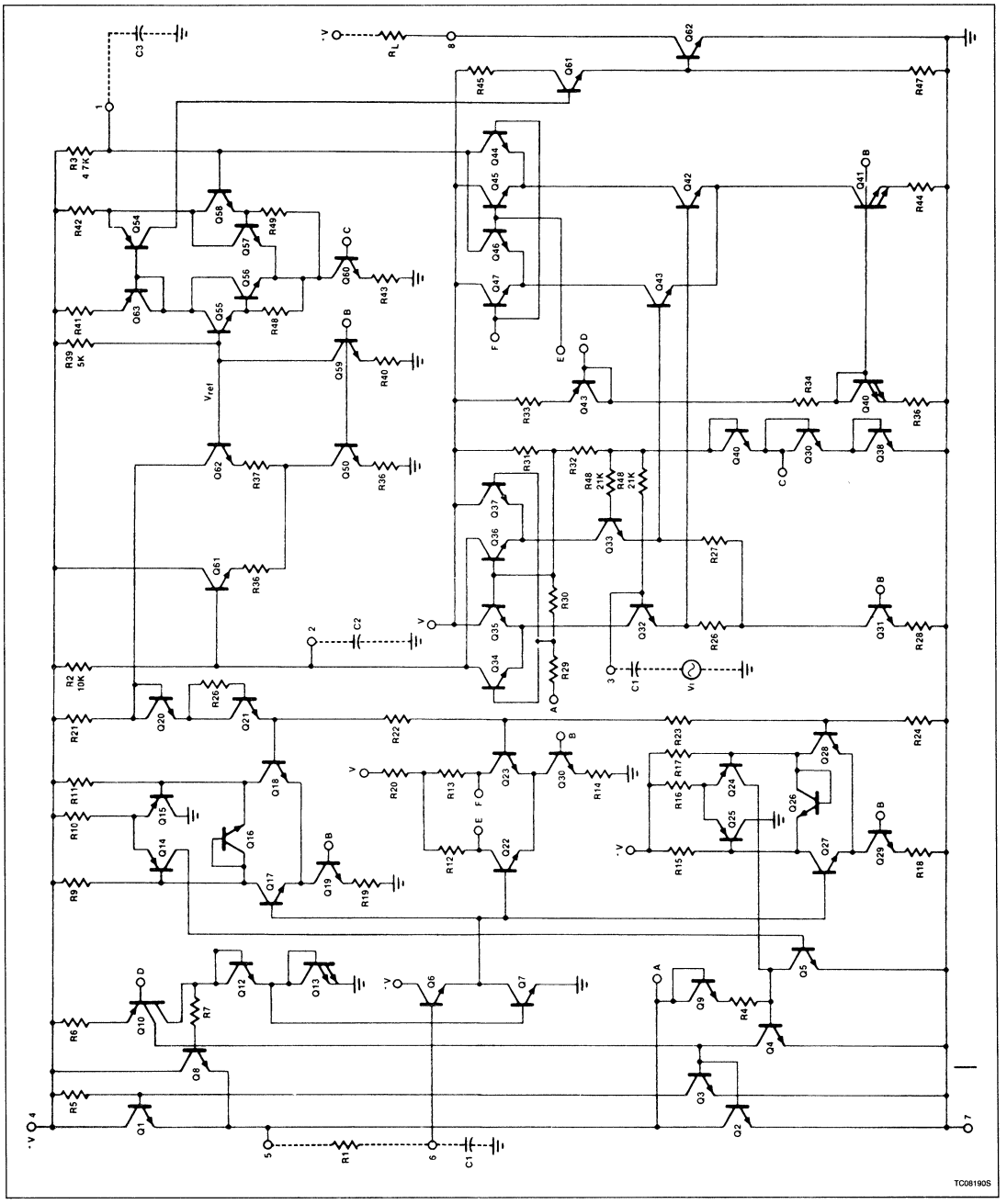
TOP VIEW CD09780S

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT & T.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE567D
14-Pin Cerdip	0 to +70°C	NE567F
8-Pin Cerdip	0 to +70°C	NE567FE
8-Pin Plastic DIP	0 to +70°C	NE567N
8-Pin Plastic SO	−55°C to +125°C	SE567D
14-Pin Cerdip	−55°C to +125°C	SE567F
8-Pin Cerdip	−55°C to +125°C	SE567FE
8-Pin Plastic DIP	−55°C to +125°C	SE567N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature NE567 SE567	 0 to +70 −55 to +125	 °C °C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 + V_S	V
V−	Negative voltage at input	−10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	300	mW

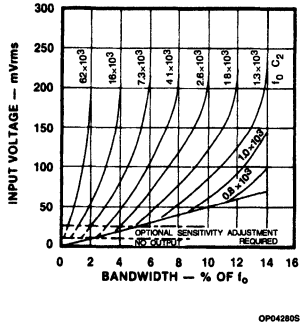
DC ELECTRICAL CHARACTERISTICS $V+ = 5.0V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	−55 to +125°C 0 to +70°C		35 ±140 35 ±60			35 ±140 35 ±60		ppm/°C ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	−10	0	+10	−10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1\ R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth — variation with temperature	$V_I = 300mV_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detectionbandwidth — variation with supply voltage	$V_I = 300mV_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	$I_L = 100mA$, $f_I = f_O$		20	25		20	25	mV_{RMS}
	Largest no-output input voltage[4]	$I_L = 100mA$, $f_I = f_O$	10	15		10	15		mV_{RMS}
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	$B_n = 140kHz$		−6			−6		dB
Output									
	Fastest on-off cycling rate			$f_O/20$			$f_O/20$		
	"1" output leakage current	$V_8 = 15V$		0.01	25		0.01	25	μA
	"0" output voltage	$I_L = 30mA$ $I_L = 100mA$		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V V
t_F	Output fall time[3]	$R_L = 50Ω$		30			30		ns
t_R	Output rise time[3]	$R_L = 50Ω$		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current — activated	$R_L = 20kΩ$		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:
1 Frequency determining resistor R_1 should be between 2 and 20kΩ
2 Applicable over 4.75V to 5.75V See graphs for more detailed information
3 Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off
4 With $R_2 = 130kΩ$ from Pin 1 to V+ See Figure 1

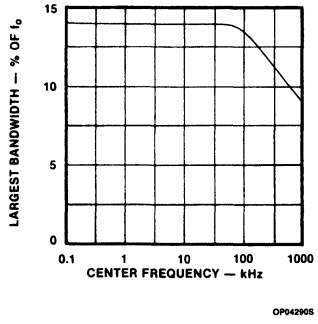
TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Input Signal Amplitude



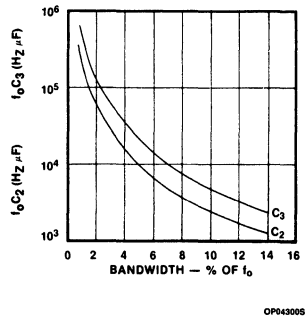
OP04280S

Largest Detection Bandwidth vs Operating Frequency



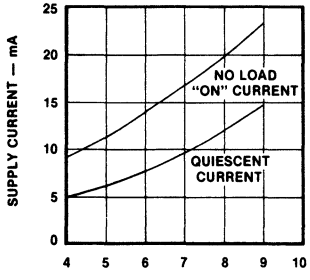
OP04290S

Detection Bandwidth as a Function of C_2 and C_3



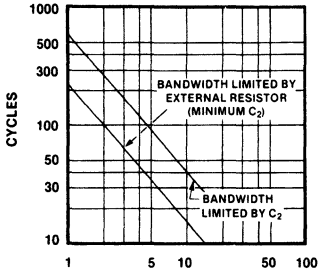
OP04300S

Typical Supply Current vs Supply Voltage



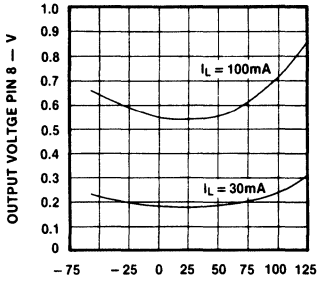
OP04310S

Greatest Number of Cycles Before Output

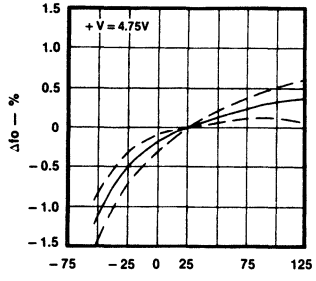


OP04320S

Typical Output Voltage vs Temperature

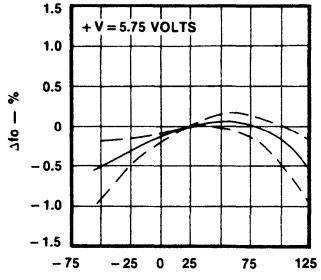


Typical Frequency Drift With Temperature (Mean and SD)



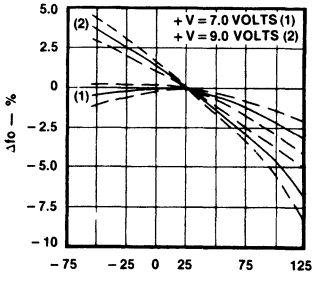
OP04340S

Typical Frequency Drift With Temperature (Mean and SD)



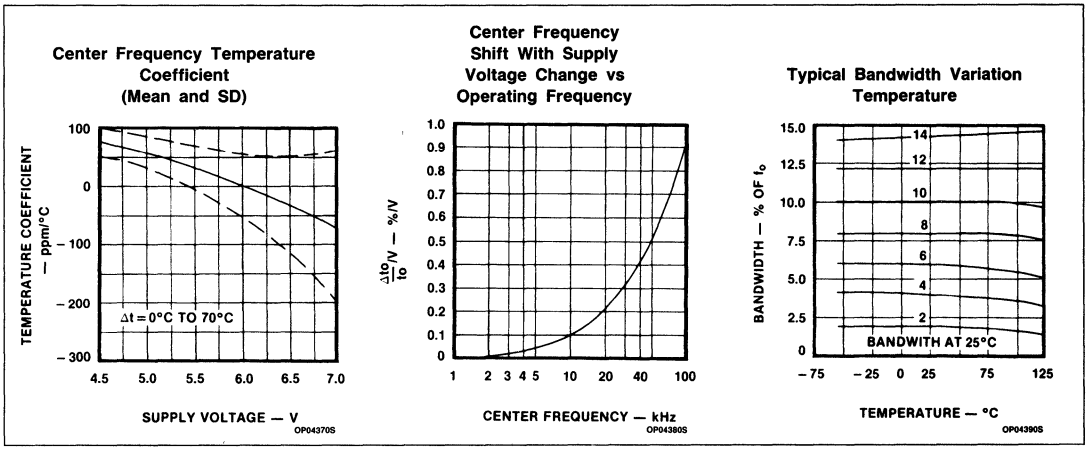
OP04350S

Typical Frequency Drift With Temperature (Mean and SD)



OP04360S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



DESIGN FORMULAS

$$f_O \cong \frac{1}{1.1R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_I}{f_OC_2}} \text{ in \% of } f_O,$$

$$V_I \leqslant 200mV_{RMS}$$

Where

V_I = Input voltage (V_{RMS})

C_2 = Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY

CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

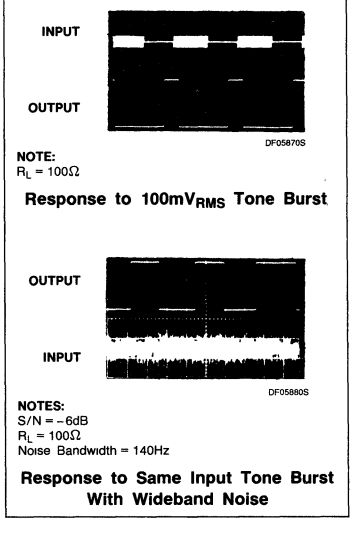
A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

TYPICAL RESPONSE



2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of f_OC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constand bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_OC_2 product (f_O (Hz), $C_2(\mu F)$).
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the

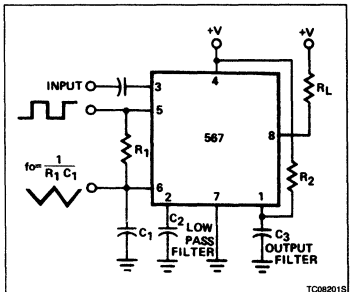


Figure 1

output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

4. Optional resistor R_2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \approx (+V - 1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n + 1)$ f_O, and will give an output for signals near $(4n + 1)$ f_O where $n = 0, 1, 2$, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can

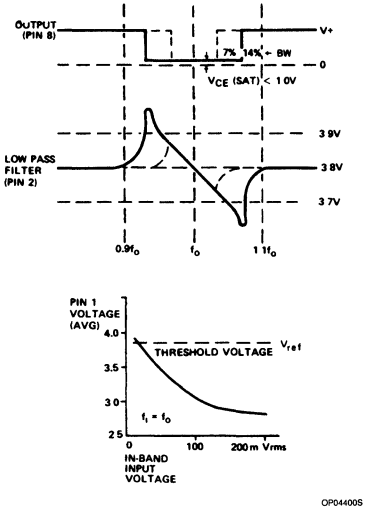


Figure 2

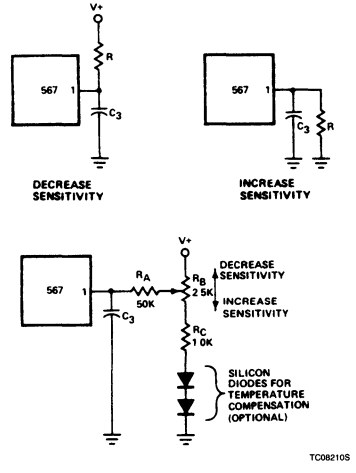


Figure 3

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O}\mu F$$

$$C_3 = \frac{260}{f_O}\mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

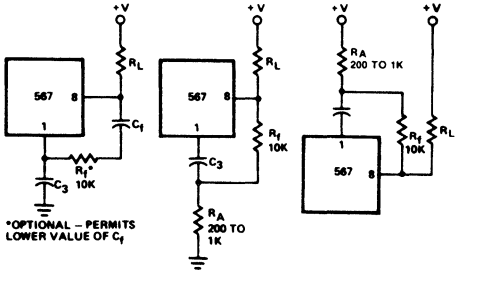


Figure 4

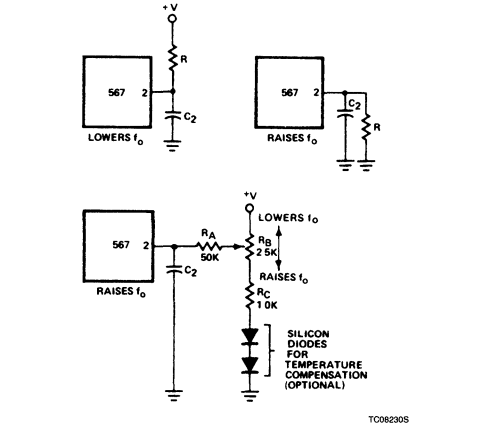


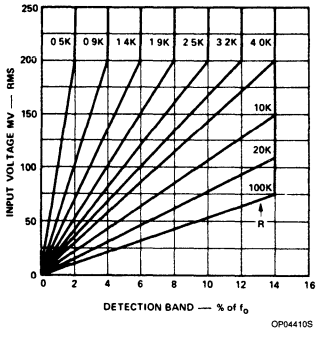
Figure 5

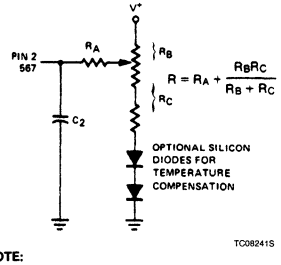
SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.





NOTE:

$$\frac{130}{f_O}\left(\frac{10k+R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k+R}{R}\right)$$

Adjust control for symmetry of detection band edges about f_O

Figure 6

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

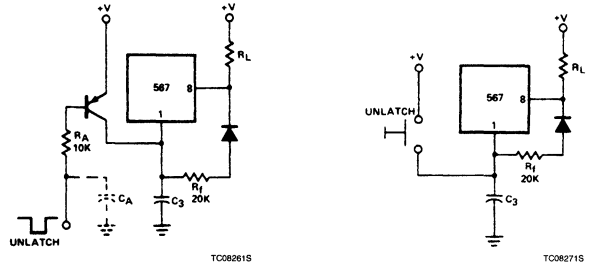
REDUCTION OF C1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

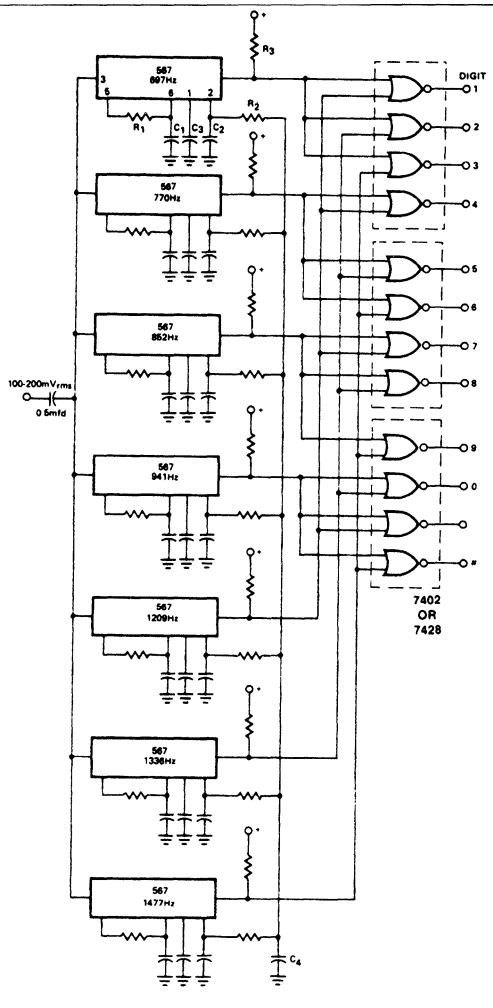
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.



NOTE:
C_A prevents latch-up when power supply is turned on

Figure 7. Output Latching

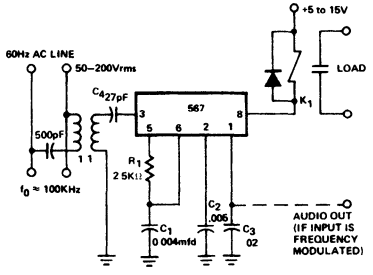
TYPICAL APPLICATIONS



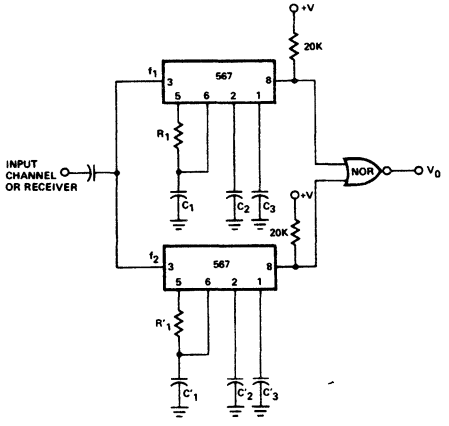
Touch-Tone® Decoder

NOTES:
Component values (Typical)
R_1 = 26 8 to 15kΩ
R_2 = 24 7kΩ
R_3 = 20kΩ
C_1 = 0 10mF
C_2 = 1 0mF 5V
C_3 = 2 2mF 6V
C_4 = 250μF 6V

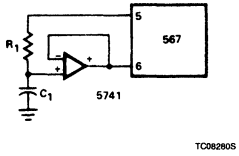
TYPICAL APPLICATIONS (Continued)



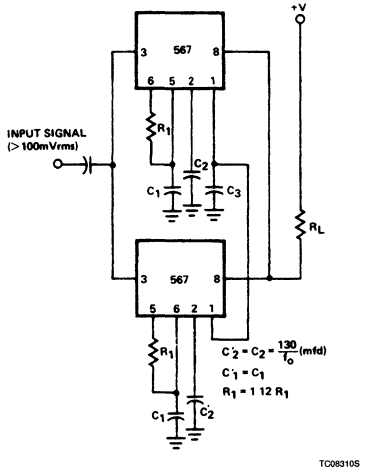
Carrier-Current Remote Control or Intercom



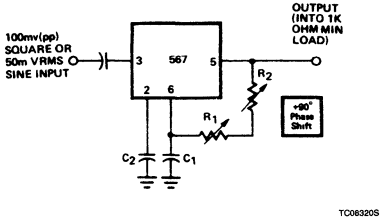
Dual-Tone Decoder



Precision VLF



24% Bandwidth Tone Decoder



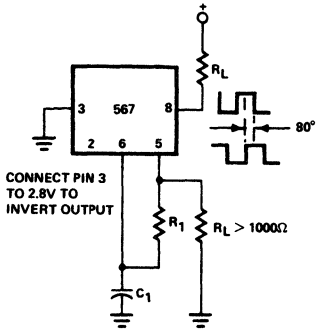
NOTES
$R_2 = R_1/5$
Adjust R_1 so that $\phi = 90°$ with control midway.

0° to 180° Phase Shifter

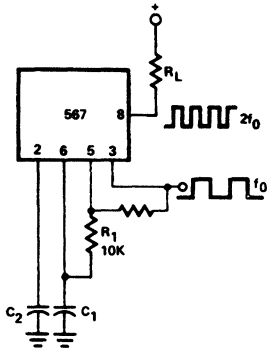
NOTES:
1 Resistor and capacitor values chosen for desired frequencies and bandwidth
2 If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible

Tone Decoder/Phase-Locked Loop NE/SE567

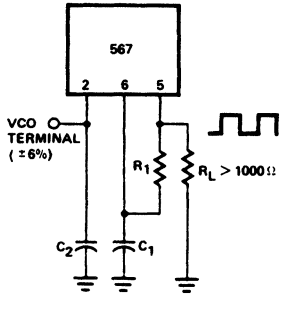
TYPICAL APPLICATIONS (Continued)



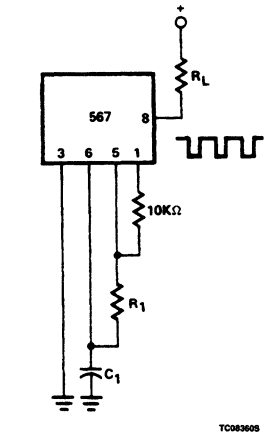
Oscillator With Quadrature Output



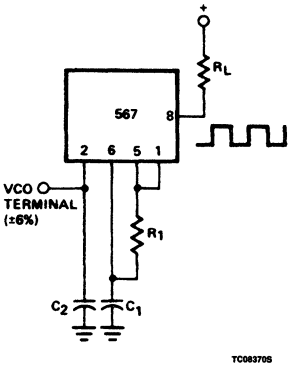
Oscillator With Double Frequency Output



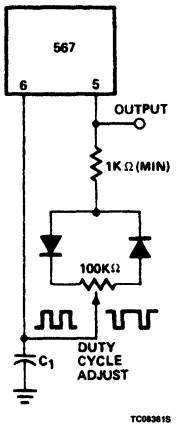
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator

AN187
Circuit Description of the NE567 Tone Decoder

Application Note

CIRCUIT DESCRIPTION OF THE NE567 TONE DECODER

The NE567 is a PLL designed specifically for frequency sensing or tone decoding. The NE567 has a controlled oscillator, a phase comparator and a second auxiliary or quadrature-phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature-phase detector output. During lock, the quadrature-phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder free-running frequency and bandwidth are specified by the free-running frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range. The complete circuit diagram of the NE567 is shown in Figure 1.

The current-controlled oscillator is shown in simplified form in Figure 2. It provides both a square wave output and a quadrature output. The control current I_C sweeps the oscillator ±7% of the free-running frequency, which is set by external components R_1 and C_1.

Transistors Q_1 through Q_6 form a flip-flop which can switch Pin 5 between V_{BE} and $+V - V_{BE}$. Thus, the R_1C_1 network is driven from a square wave of $+V - 2V_{BE}$ peak-to-peak volts. On the positive portion of the square wave, C_1 is charged through R_1 until V_1 is reached. A comparator circuit driven from C_1 at Pin 6 then supplies a pulse which resets the flip-flop so that Pin 5 switches to V_{BE} and C_1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop, and C_1 resumes charging.

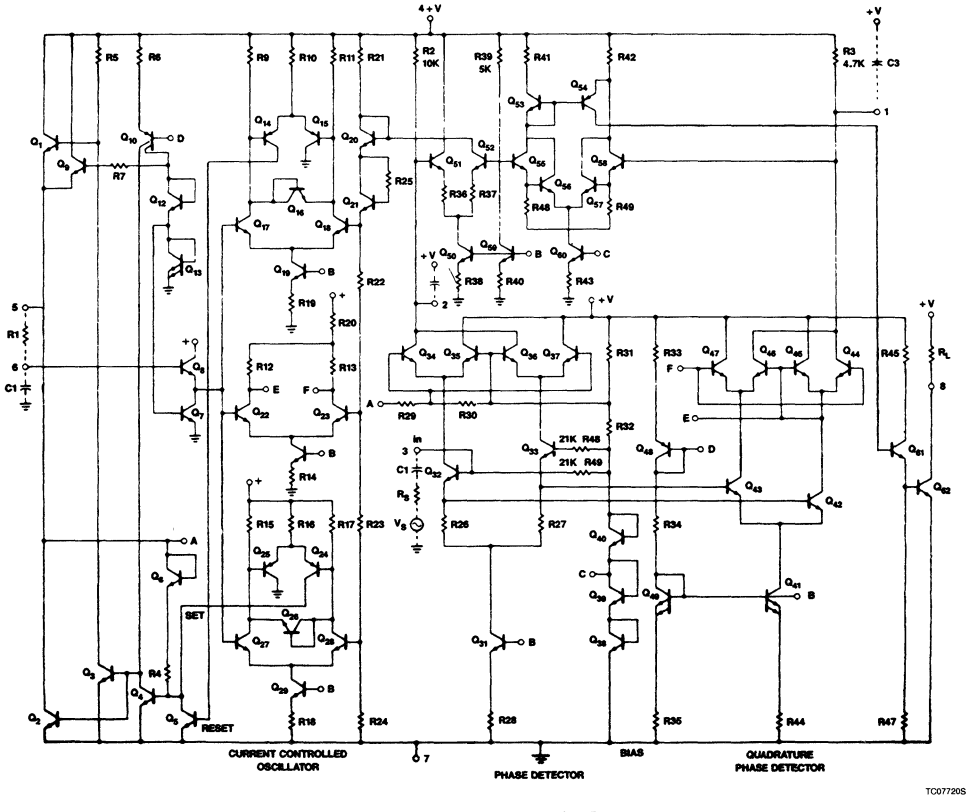


Figure 1. Circuit Diagram of NE567

Circuit Description of the NE567 Tone Decoder AN187

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

$$V_1 - V_2 = (+V - 2V_{BE})\left[\frac{R_{22} + R_{23}}{R_{21} + R_{22} + R_{23} + R_{24}}\right]$$

$$= K(+V - 2V_{BE}) \quad (1)$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 3 shows the Pin 5 and Pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of +V and dependent only on the time constant R_1C_1 of the external components. Moreover, if $(V_1 + V_2)/2 = +V/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase-shifted from the square wave.

A differential stage (Q_{22} and Q_{23}) amplifies the triangular wave with respect to $(V_1 + V_2)/2$ to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase-shifted about 80°, but no operating compromises result from this slight deviation from true quadrature.)

One source of error in this oscillator scheme is current drawn by the comparators from the R_1C_1 mode. An emitter-follower, therefore, is inserted at X to minimize this drain and Q_{21} placed in series with Q_{20} to drop the comparator sensing voltage one V_{BE} to compensate for the V_{BE} drop in the emitter-follower.

In order to insure that the square wave drops quickly and accurately to V_{BE}, an active clamp scheme is applied to the collector of Q_2. The base of Q_9 is held at $2V_{BE}$ so that as Q_2 is turned on its base current, its collector

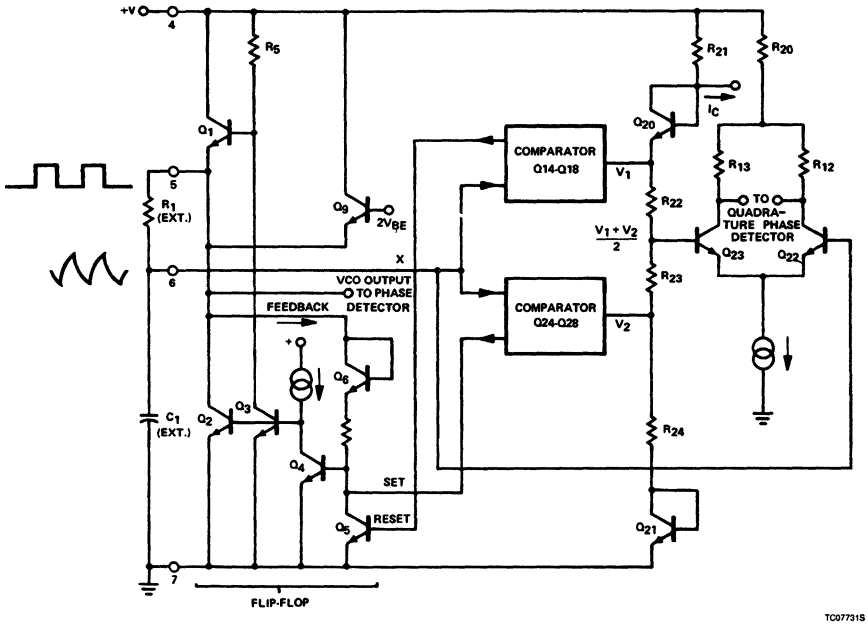


Figure 2. Simplified Diagram of NE567 Tone Decoder Current-Controlled Oscillator

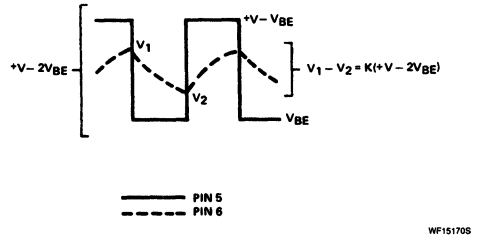


Figure 3. Current-Controlled Oscillator Waveshapes in the NE567

Circuit Description of the NE567 Tone Decoder AN187

is held at V_{BE}. Because Q_2 and Q_3 have the same geometry and their base-emitter voltages are the same, the maximum Q_2 current, when clamped, is essentially the same as the collector current of Q_3 (as limited by R_5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making R_{21} somewhat less than R_{24} and restoring the proper voltage for 50% duty cycle by drawing I_C of 100μA for the R_{21}, Q_{20} junction. When I_C is then varied between 0 and 200μA, the frequency changes by ±7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_C, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of free-running frequency with temperature and supply voltage changes when $I_C \neq 0$, I_C is also made a function of $+V - 2V_{BE}$.

A doubly balanced multiplier formed by Q_{32} through Q_{37} (Figure 1) functions as the phase comparator. The input signal is applied to the base of Q_{32}. Transistors $Q_{34} - Q_{37}$ are driven by a square wave taken from the CCO at the collector of Q_2. Phase comparator input bias is provided by three diodes, Q_{38} through Q_{40}, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R_{26} and R_{27}, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop DC amplifier is formed by Q_{51} and Q_{52}. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full ±7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mV_{RMS}. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels, since this greatly facilitates operation of the quadrature lock detector. Emitter-resistors R_{36} and R_{37} help stabilize the gain over the required temperature range. Another function of the DC amplifier is to allow a higher impedance level at the low pass filter terminal (Pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter-resistors help stabilize the loop gain over the temperature range.

The quadrature-phase detector (QPD), formed by a second doubly-balanced multiplier $Q_{42} - Q_{47}$ is driven from the quadrature output (E, F, in Figure 1) of the CCO. The signal input comes from the emitters of the input transistors Q_{32} and Q_{33}.

The output stage, Q_{53} through Q_{62}, compares the average QPD current in the low pass output filter R_3C_3 with a temperature-compensated current in R_{39} (forming the threshold voltage V_t).

Since R_3 is slightly lower in value than R_{39}, the output stage is normally off. When the lock and the QPD current I_q occurs, Pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (Pin 8) of the power NPN output transistor can drive both 100 – 200mA loads and logic elements, including TTL.

The K_o conversion gain for the NE567 tone decoder is given by

$$K_o = 0.44\omega_O' \left(\frac{\text{radians}}{\text{volt-sec}} \right) \qquad (2)$$

while the K_d conversion gain depends upon the input signal level as shown in Figure 4. These parameters can be used to calculate the lock and capture range as has been illustrated previously.

The NE567 tone decoder is a specialized loop which can be setup to respond to a given tone (constant frequency) within its bandwidth. The free-running frequency is set by a resistor R_1 and capacitor C_1. The bandwidth is controlled by the low-pass filter capacitor C_2. A third capacitor C_3 integrates the output of the quadrature-phase detector (QPD) so that the DC lock-indicating component can switch the power output stage on when lock is present. The NE567 is optimized for stability and predictability of free-running frequency and bandwidth.

Two events must occur before an output is given. First, the loop portion of the NE567 must achieve lock. Second, the output capacitor C_3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low-pass filter. Thus, C_2 must be as small as possible. However, C_2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 5, reprinted from the NE567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C_2 and the input amplitude is 200mV_{RMS} or greater. The response time is given in cycles of free-running frequency. For example, a 2% bandwidth at a free-running frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 6 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only $^{30}/_{180} = 1/6$ of the time will the lock-up time be longer than half the worst-case lock-up time. Figure 7 shows some actual measurements of lock-up time for a setup having a worst-case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

The lower curve on the graph of Figure 5 shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C_2 required for this minimum response time is

$$C_{2(min)} = \frac{130}{f_O'} \left[\frac{10k + R_A}{R_A} \right] \mu F \qquad (3)$$

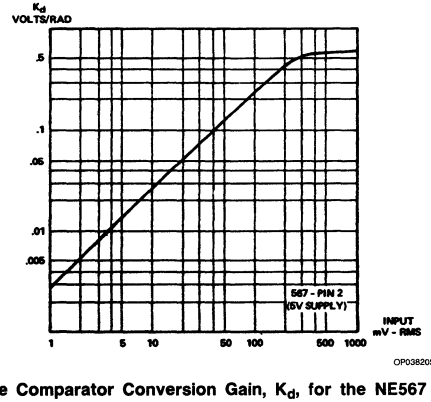


Figure 4. Phase Comparator Conversion Gain, K_d, for the NE567 Tone Decoder

Circuit Description of the NE567 Tone Decoder AN187

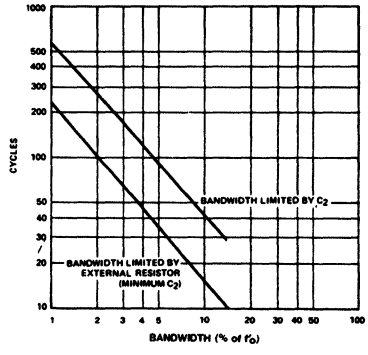


Figure 5. Greatest Number of Cycles Before Output for the NE567 Tone Decoder

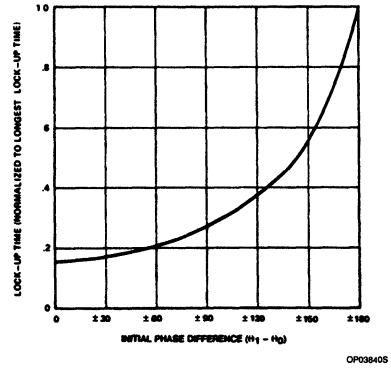


Figure 6. Lock-Up Time vs Initial Phase for the NE567 Tone Decoder

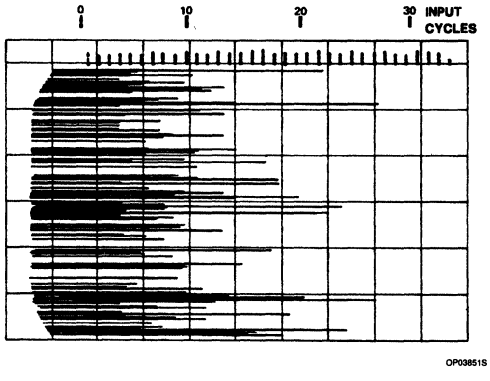


Figure 7. Lock-Up Time Variation Due to Random Initial Phase for the NE567 Tone Decoder

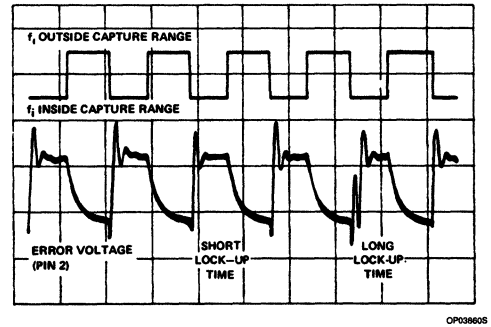


Figure 8. Lock-Up Transient Response for NE567 Tone Decoder

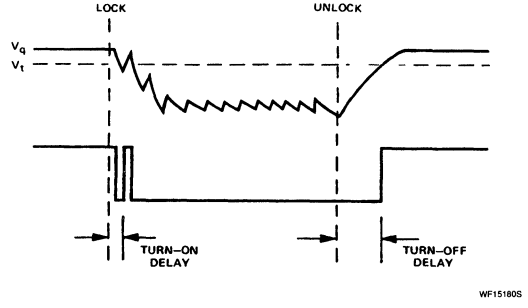
It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value of C_2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect on the lock-up time — usually negligible in comparison to the variation caused by input phase.

Lock-up transients can be displayed on a two-channel scope with case. Figure 8 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at Pin 2, the low-pass filter voltage. The input frequency is offset slightly from the free-running frequency so that the locked and unlocked voltages are different. It is apparent that, while the C_2 decay during unlock is always the same, the lock transient is different each time.

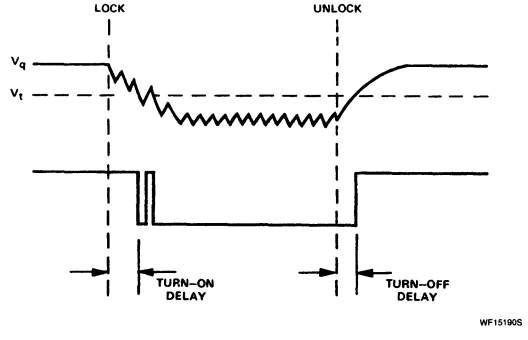
This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing so, a favorable initial phase is created that is not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C_2 or input amplitude is seen. However, the *repetition rate must be readjusted for worst-case lock-up after each such change.*

Once lock is achieved, the quadrature-phase detector output at Pin 1 is integrated by C_3 to extract the DC component. As C_3 charges from its quiescent value V_q (see Figure 9) to its final value ($V_q \cdot \Delta V$), it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant ($\tau = 4700C_3$) expires before V_t is crossed so that C_3 does not greatly influence the response time. However, as shown in Figure 9a, the turn-off delay time can be quite long when C_3 is large. Figure 9b shows how desensitizing the output stage by connecting a high-value resistor between Pin 1 and Pin 4 (positive supply voltage) can equalize the turn-on and turn-off time. If turn-off delay is important in the

Circuit Description of the NE567 Tone Decoder AN187



a. V_q Slightly Greater Than V_t



b. V_q Much Greater Than V_t

Figure 9. Effect of Threshold Voltage Adjustment on Tone Decoder Turn-On and Turn-Off Delay

overall response time, then desensitizing can reduce the total delay.

But why not make C_3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large second harmonic component of the free-running frequency that must be filtered out. Also, noise, out-band signals, and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C_3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C_3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C_3. What must be done, then, is to make C_3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a. After the center frequency has been set, adjust C_2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 7) suggests that worst-case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction (see data sheet).

b. Check lock-up time by observing the waveform at Pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.

c. Starting with a large value of C_3 (say 10 C_2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.

d. Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.

e. Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a. Relax the bandwidth requirement.

b. Operate the entire system at higher frequency when this option is available.

c. Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurrence of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.

d. Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth, and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.

e. If the system design permits, send the tone to be detected continuously at a low level (say 25mV_{RMS}) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing the signal amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as ⅓ to ½ the free-running frequency when C_3 is small. This is equivalent to ASK (amplitude shift keying).

Signetics

AN188
Selected Circuits Using the NE567

Application Note

Linear Products

Touch-Tone® Decoder

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the pushbutton dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 1. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mV$_{RMS}$. Capacitor C_4 decouples the seven units. The seven R_2 resistors and capacitor C_4 can be eliminated at the expense of a somewhat slower response at low input voltages (50 to 100mV$_{RMS}$). The bandwidth can be controlled in the normal manner by selecting C_2 to be 4.7μF for the three lower frequencies and 2.2μF for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. An external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for DC bias, it goes to a common point with the six other R_2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two NE567s which are being activated. Capacitor C_4 decouples the AC currents at the common point.

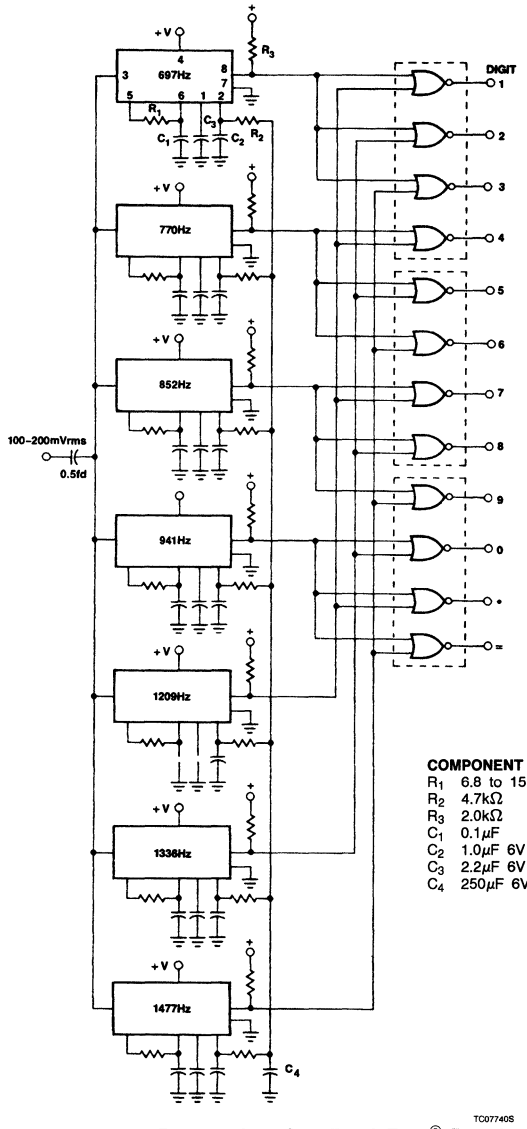
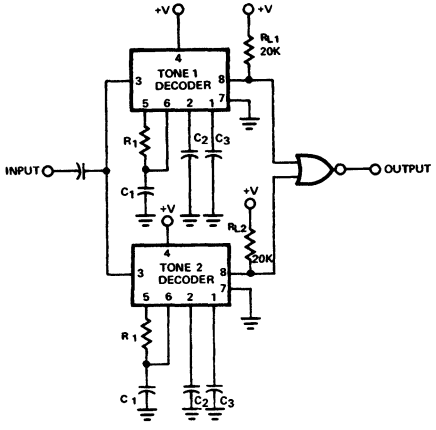


Figure 1. Low Cost Touch-Tone® Decoder

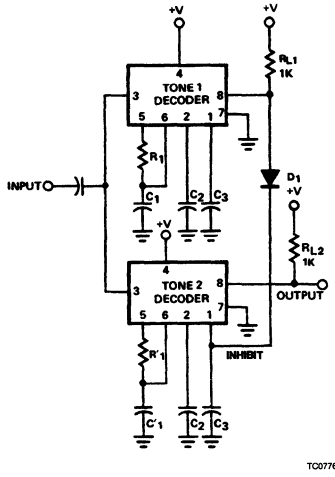
TONE DECODER APPLICATIONS (NE567)

The NE567 is a special purpose PLL intended solely for use as a tone decoder. It contains a complete PLL including VCO, phase comparator, and amplifier as well as a quadrature-phase detector of multiplier. If the signal amplitude at the lock frequency is above a minimal value, the driver amplifier turns on, driving a load with as much as 200mA. Thus the 567 gives an output whenever an in-band tone is present. The 567 is optimized for both free-running frequency and bandwidth stability.

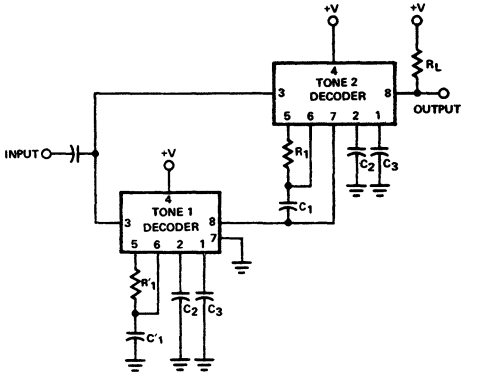
®Touch-Tone is a registered trademark of Bell Laboratories



a. NORing Outputs Together



b. Disabling the Second Decoder Until Enabled by the First



c. Blocking Power to the Second Decoder (Pin 7) Until the First is Enabled

Figure 2. Detection of Two Simultaneous or Sequential Tones

Dual-Tone Decoder

Two 567 tone decoders connected as shown in Figure 2a permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1 C_1 and R_1' C_1' are chosen respectively for tones 1 and 2. If sequential tones (tone 1 followed by tone 2) are to be decoded, then C_3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated.

Note that the wrong sequence (tone 2 followed by tone 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 2b shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_{L1} and D_1 until activated by tone 1. A further variation is given in Figure 2c. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

Selected Circuits Using the NE567 AN188

High-Speed, Narrow-Band Tone Decoder

The circuit of Figure 2a may be used to obtain a fast, narrow-band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mV$_{RMS}$ at all times to prevent detection band shrinkage and C_2 should be between $130/f_O$ and $1300/f_O\mu F$ where f_O is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

Low-Cost Frequency Indicator

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is at 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

Phase Modulator

If a phase-locked loop is locked onto a signal at the free-running frequency, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low-pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase comparator so that the VCO voltage is constant and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase comparator output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 4a. The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 4b shows an implementation of this circuit using the 567.

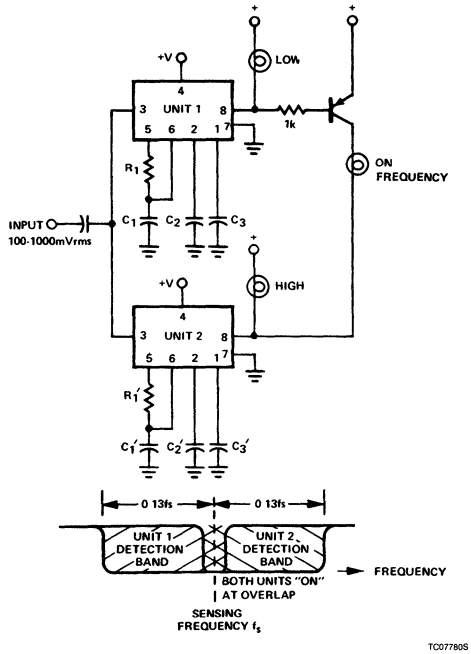
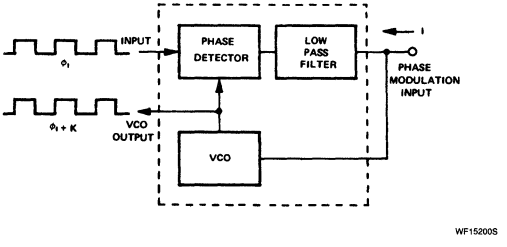
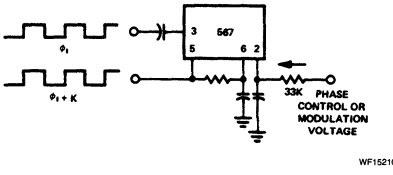


Figure 3. Low Cost Frequency Detector With Lamp Readout



a. Block Diagram



b. Circuit Implementation With the NE567

Figure 4. Phase Modulation Using the PLL

Signetics

NE568
150MHz Phase-Locked Loop

Preliminary Specification

Linear Products

DESCRIPTION

The NE568 is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate ±20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20-pin dual in-line and 20-pin SO (surface-mounted) plastic packages.

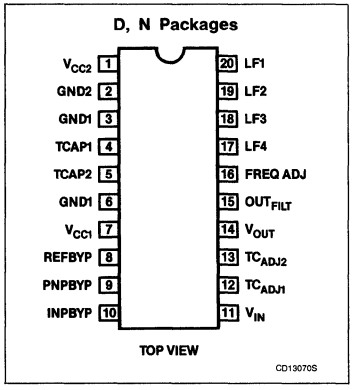
FEATURES

- **Operation to 150MHz**
- **High linearity buffered output**
- **Series or shunt loop filter component capability**
- **Temperature compensated**

APPLICATIONS

- **Satellite receivers**
- **Fiber-optic video links**
- **VHF FSK demodulators**
- **Clock recovery**

PIN CONFIGURATION

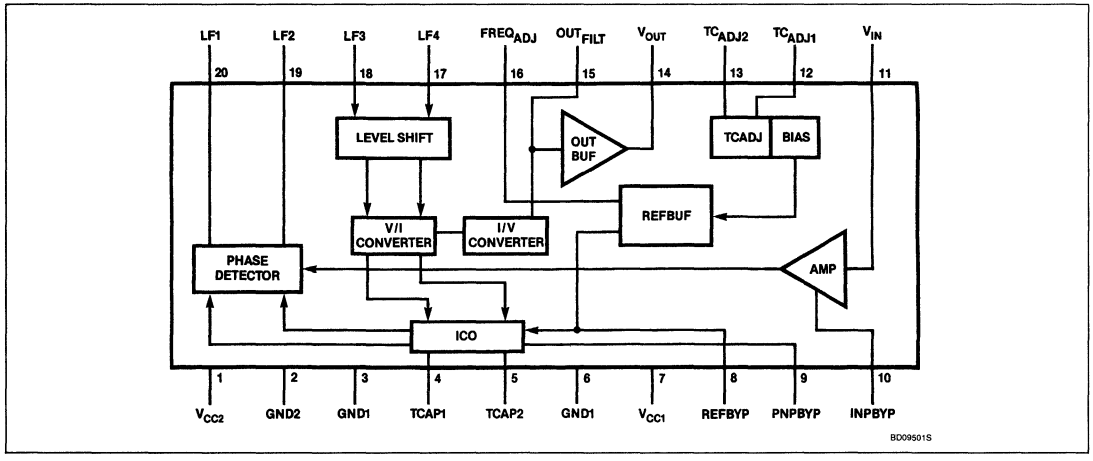


4

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL Package	0 to +70°C	NE568D
20-Pin Plastic DIP	0 to +70°C	NE568N

BLOCK DIAGRAM



150MHz Phase-Locked Loop | NE568

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation	500	mW

ELECTRICAL CHARACTERISTICS

The electrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test setup is not necessarily optimum. The NE568 is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1 – 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 5V$, $f_O = 70MHz$, Test Circuit Figure 1, $f_{IN} = -20dBm$, $R_4 = 0\Omega$ (ground), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current			60	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±20%, Input = −20dBm		1.0	4.0	%
	Lock range[2]	Input = −20dBm	±25	±35		% of f_O
	Capture range[2]	Input = −20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 14	0.40	0.52		V_{P-P}
	AM rejection	V_{IN} = −20dBm (30% AM) referred to ±20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, $R_2 = 1.2k\Omega$, $C_2 = 17pF$, $R_4 = 0\Omega$ ($C_2 + C_{STRAY} = 20pF$)	−15	0	+15	%
f_O	Drift with supply	4.75V to 5.25V		1		%/V

NOTES:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design
4. Input impedance depends on package and layout capacitance See Figures 4 and 5
5. Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}) Nonlinearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

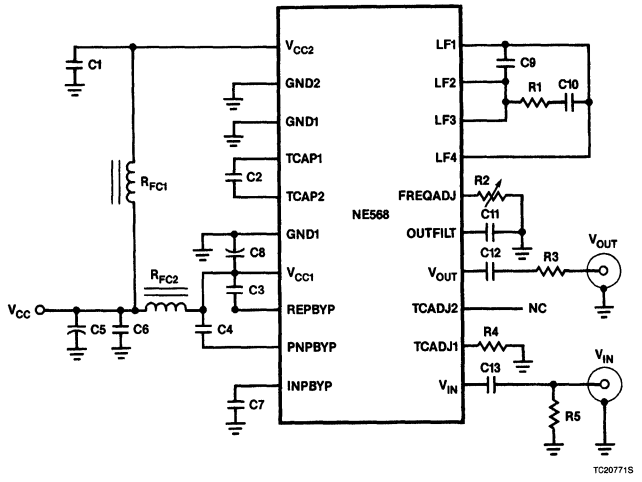


Figure 1. Test and Application Circuit

FUNCTIONAL DESCRIPTION

The NE568 is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \text{ F}$$

where

$$C^* = C_2 + C_{STRAY}.$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See Figure 6 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568 was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constants are:

$K_D = 0.127V/Radian$ (Phase Detector Constant)

$$K_O = 4.2 \times 10^9 \frac{\text{Radians}}{\text{V-sec}} \text{ (ICO Constant)}$$

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)(f_O)} \text{ F}$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 56pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10MHz$, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1 f_{BW}} \text{ F}$$

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568D

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	34pF	±2%	Ceramic OR chip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	56pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip	1/8W
R_2	1.2kΩ		Trim pot	1/8W
R_3[3]	43Ω	±10%	Chip	1/8W
R_4[4]	4.7kΩ	±10%	Chip	1/8W
R_5[3]	50Ω	±10%	Chip	1/8W
RFC_1[5]	10μH	±10%	Surface mount	
RFC_2[5]	10μH	±10%	Surface mount	

NOTES:
1. $C_2 + C_{STRAY} = 20pF$
2. $C_2 + C_{STRAY} = 36pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 62\Omega$, $R_5 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance

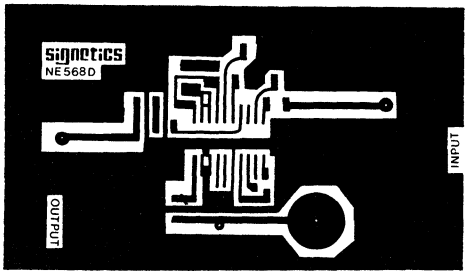
For the test circuit, R_1 was chosen to be 27Ω. The calculated value of C_{10} is 590pF; 560pF was chosen as a production value. (In actual satellite receiver applications, improved video with low carrier/noise has been observed with a wider loop-filter bandwidth.)

A typical application of the NE568 is demodulation of FM signals. In this mode of operation, a second single-pole filter is available at Pin 15 to minimize high frequency feedthrough to the output. The roll-off frequency is set by an internal resistor of 350Ω ±20%, and an external capacitor from Pin 15 to ground. The value of the capacitor is:

$$C11 = \frac{1}{2\pi\ (350) f_{BW}}\ F$$

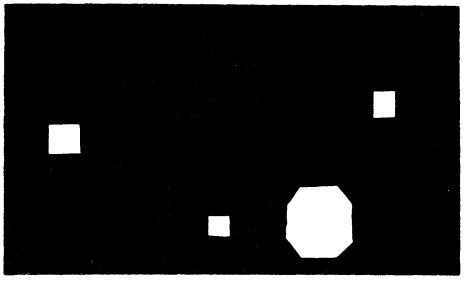
Two final components complete the active part of the circuitry. A resistor from Pin 12 to ground sets the temperature stability of the circuit, and a potentiometer from Pin 16 to ground permits fine tuning of the free-running oscillator frequency. The Pin 16 potentiometer is normally 1.2kΩ. Adjusting this resistance controls current sources which affect the charge and discharge rates of the timing capacitor and, thus, the frequency. The value of the temperature stability resistor is chosen from the graph in Figure 6; the respective timing capacitor needs to be changed.

The final consideration is bypass capacitors for the supply lines. The capacitors should be ceramic chips, preferably surface-mount types. They must be kept very close to the device. The capacitors from Pins 8 and 9 return to V_{CC1} before being bypassed with a separate capacitor to ground. This assures that no differential loops are created which might cause instability. The layouts for the test circuits are recommended.



DF07740S

a. Component Side Top of Board



DF07730S

b. Back of Board

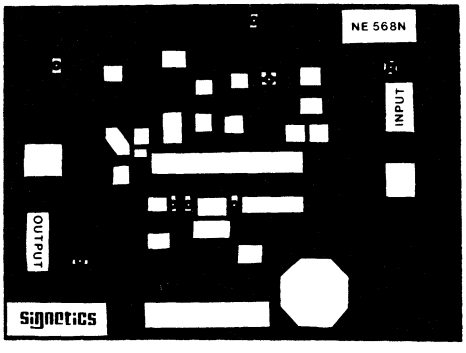
NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent. Mount on bottom (back) of board. Add stand-off in each corner.
2. Back and top side ground must be connected at 8 point minimum.

Figure 2

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568N

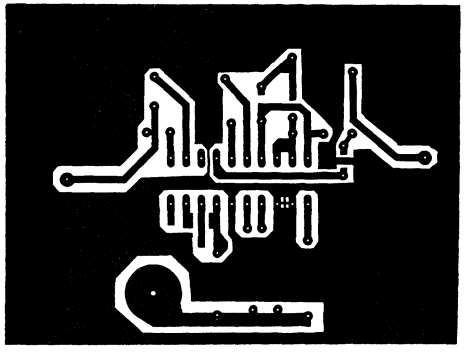
C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	17pF	±2%	Ceramic OR chip	50V
C_2[2]	34pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic OR chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	56pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic OR chip	50V
C_{12}	100nF	±10%	Ceramic OR chip	50V
C_{13}	100nF	±10%	Ceramic OR chip	50V
R_1	27Ω	±10%	Carbon	¼W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Carbon	¼W
R_4[4]	4.7kΩ	±10%	Carbon	¼W
R_5[3]	50Ω	±10%	Carbon	¼W
RFC_1	10μH	±10%		
RFC_2	10μH	±10%		

NOTES:
1. $C_2 + C_{STRAY} = 20pF$ for test configuration with $R_4 = 0\Omega$.
2. $C_2 = 34pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$
3. For 50Ω setup $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω applications
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 17pF$.



DF07750S

a. Component Side for Leaded Components



DF07760S

b. Solder Side of Board and Chip Capacitors

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent mounted on the component side of the board
2. Component side and solder side ground planes must be connected at 8 points minimum

Figure 3

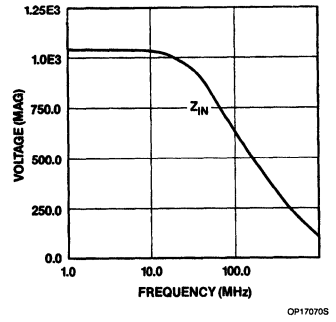


Figure 4. NE568 Input Impedance with CP = 0.5pF 20-Pin SO Package

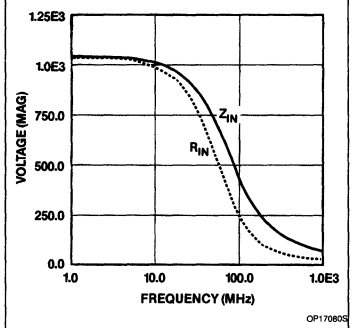


Figure 5. NE568 Input Impedance with CP = 1.49pF 20-Pin Dual In-Line Plastic Package

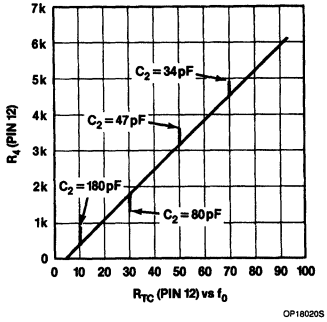


Figure 6

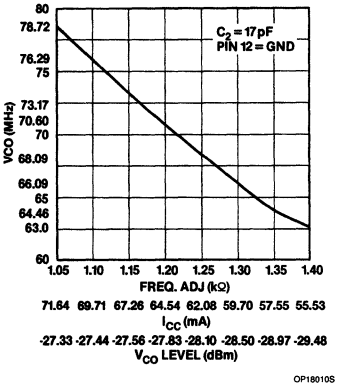


Figure 7. Typical VCO Frequency vs R_2 Adjustment

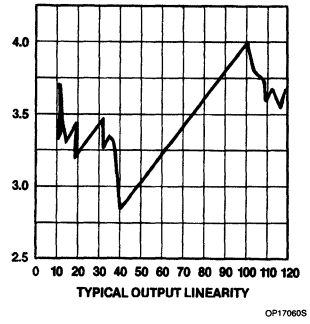


Figure 8. Typical Output Linearity

Signetics

AN174
Applications for Compandors: NE570/571/SA571

Application Note

Linear Products

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{IN} so that the gain is proportional to the average value of (V_{IN}). Thus, when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \left[\frac{2\ R_3\ V_{IN}\ (\text{avg})}{R_1\ R_2\ I_B};\right]^2$$

$I_B = 140\mu A$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I = 3V/R_1 = 3V/10k = 300\mu A$. The ΔG cell input current should be limited to $I = 2.8V/R_2 = 2.8V/20k = 140\mu A$. If it is necessary to handle larger input voltages than 0 ±2.8V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{IN1} and C_{IN2}. It is now necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the DC gain provided by R_3, R_4. The output will bias up to

$$V_{OUT\ DC} = (1+\frac{R_3}{R_4})\ \ V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $\frac{1}{2}V_{CC}$.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC COMPRESSOR

Figure 2 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3 V_{IN}\ (\text{avg})}\right]^{1/2}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no DC feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{DC} and the capacitor C_{DC} must be provided. The op amp output will bias up to

$$V_{OUT\ DC} = (1 + \frac{2R_{DC}}{R4})\ V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

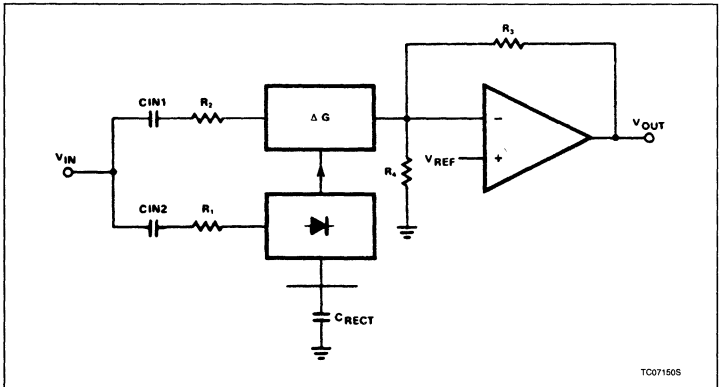


Figure 1. Basic Expandor

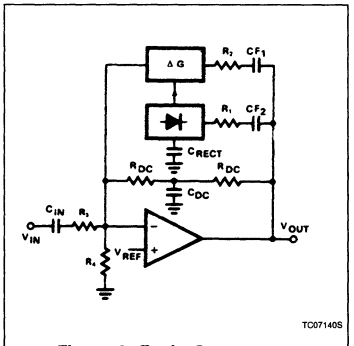


Figure 2. Basic Compressor

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the ΔG cell). The THD trim terminal provides

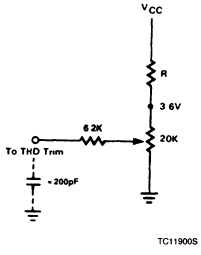


Figure 3. THD Trim Network

a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering $\pm 30\mu A$ into 100Ω resistor tied to 1.8V.

LOW LEVEL MISTRACKING

The compandor will follow a 2-to-1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of < 100nA that produces errors at low levels. The magnitude of the error can be estimated. For a full-scale rectifier input signal of $\pm 200\mu A$, the average input current will be $127\mu A$. When the input signal level drops to a $1\mu A$ average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

It is possible to deviate from the 2-to-1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_A or R_B, (but not both), is required. The voltage on C_{RECT} is 2 × V_{BE} plus V_{IN} avg. For low level inputs V_{IN} avg is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is placed from C_{RECT} to AND we will bleed off a current

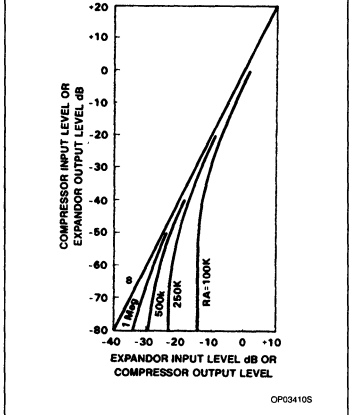


Figure 5. Mistracking With R_A

I = 1.3V/R_A. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed 1.3V/R_A and the expandor output will become active. For large input signals, R_A will have little effect. The result of this is that we will deviate from the 2-to-1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{BE} drops, so the low level tracking will drift with temperature. If a negative supply is available, if would be desirable to tie R_A to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{BE} temperature drift.

R_B will supply an extra current to the rectifier equal to (V_{CC} – 1.3V)R_B. In this case, the expandor transfer characteristic will deviate towards 1-to-1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor, this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_B value of approximately 2.5M would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

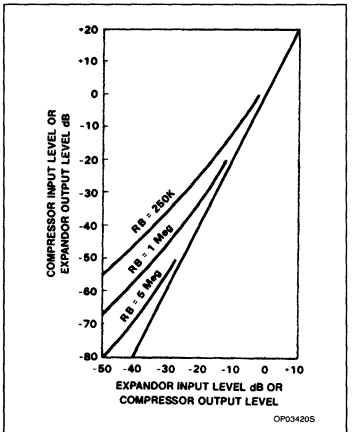


Figure 6. Mistracking With R_B

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant 10k × C_{RECT}. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards

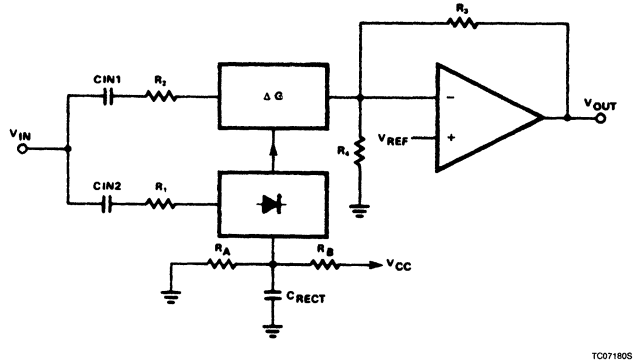


Figure 4. Expandor With Low Level Mistracking

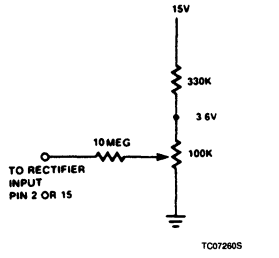


Figure 7. Rectifier Bias Current Compensation

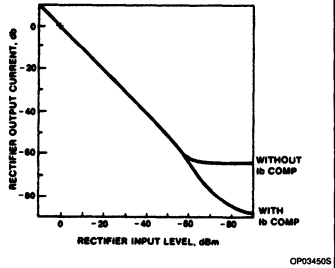


Figure 8. Rectifier Performance With Bias Current Compensation

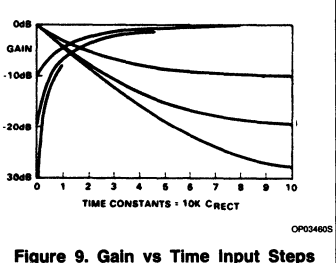


Figure 9. Gain vs Time Input Steps of ±10, ±20, ±30dB

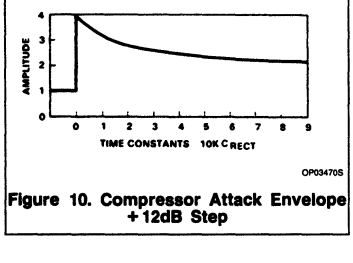


Figure 10. Compressor Attack Envelope +12dB Step

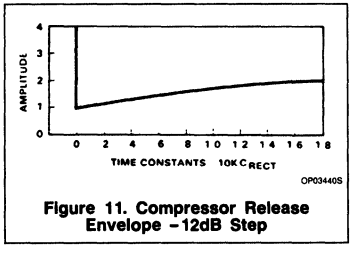


Figure 11. Compressor Release Envelope -12dB Step

its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t = 0.15 in the figure. The CCITT recommends an attack time of 3 ± 2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ± 9ms. This corresponds to t = 0.675 in the figure, which again suggests a 20ms RC product. Since R_1 = 10k, the CCITT recommendations will be met if $C_{RECT} = 2\mu F$.

There is a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a 1μF C_{RECT} will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where $C_{RECT} = 2\mu F$, the ripple would cause 0.1% distortion at 1kHz and 0.33% at 800Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{RECT}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires ½ of an NE570/571, ½ of an LM339 quad comparator, and a PNP transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or −1V peak, a comparator threshold is exceeded. The PNP is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10k. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about 0.7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on Pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to > 1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two PNP transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then Pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one PNP transistor and one capacitor C_4 need be used. The release time will then be the product 5k × C_4 since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 are not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

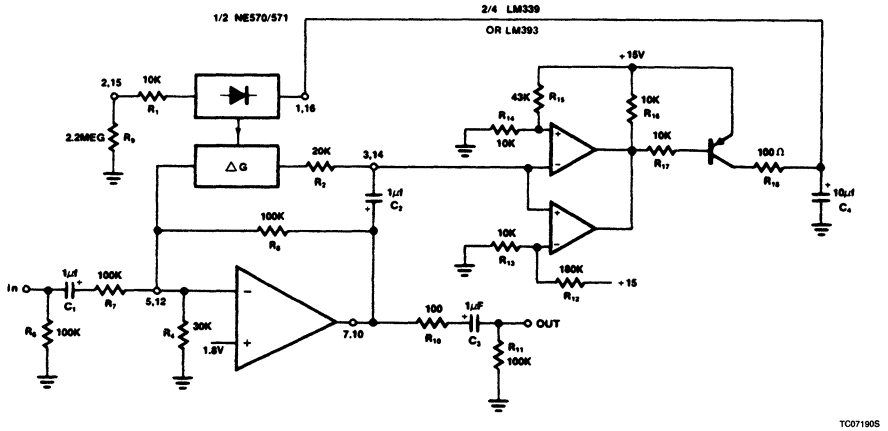
Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either Pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10μV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply (+V_{CC} and ground), it must have an input common-mode range down to less than 1.8V.

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

4

Applications for Compandors: NE570/571/SA571 AN174



+15V Pin 13
GND Pin 4
R_1, R_2, R_4 are internal to the NE570/571

Figure 12. Fast Attack, Slow Release Hard Limiter

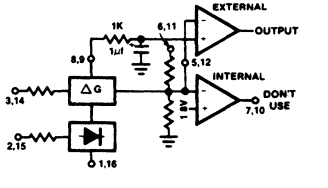


Figure 13. Use of External Op Amp

Figure 14 shows the implementation of an N2 compressor. The input level of 0.245V_{RMS} is stepped up to 1.41V_{RMS} by the 600Ω: 20kΩ matching transformer. The 20k input resistor properly terminates the transformer. An internal 20kΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4kΩ output resistor and the 4kΩ: 600Ω output transformer. The 0.275V_{RMS} output level requires a 1.4V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{\text{Gain}^2 \times 2\ R_3\ V_{IN}\ \text{avg}}{R_1\ I_B}$$

$$= \frac{1^2 \times 2 \times 20\text{k} \times 1.27}{10\text{k} \times 140\mu\text{A}}$$

$$= 36.3\text{k}$$

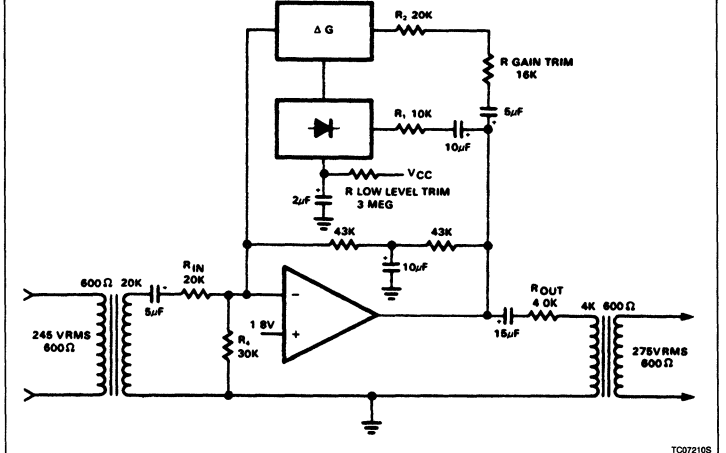


Figure 14. N2 Compressor

The external resistance required will thus be 36.3k – 20k = 16.3k.

The Bell-compatible low level tracking characteristic is provided by the low level trim resistor from C_{RECT} to V_{CC}. As shown in Figure 6, this will skew the system to a 1:1 transfer characteristic at low levels. The 2μF rectifier capacitor provides attack and release times of 3ms and 13.5ms, respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides DC feedback to bias the output at DC.

An N2 expandor is shown in Figure 15. The input level of 3.27V_{RMS} is stepped down to 1.33V by the 600Ω:100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω:600Ω output transformer. With this configuration, the 3.46V transformer output requires a 3.46V op amp

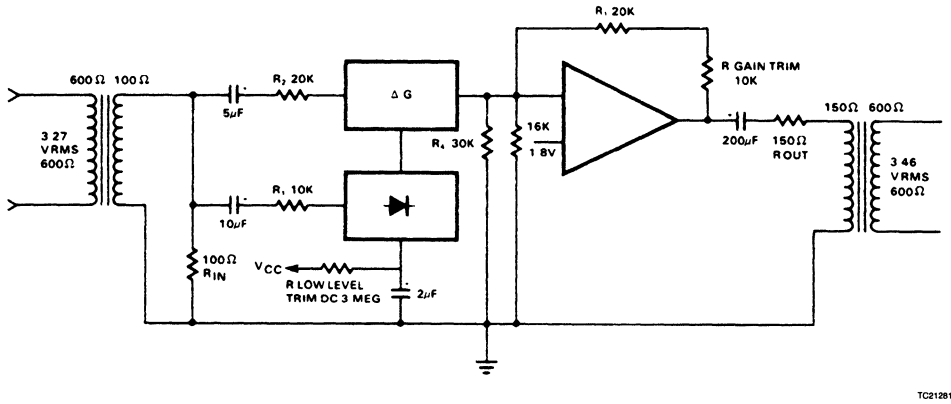


Figure 15. N2 Expandor

output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{IN}\ \text{avg}}$$

$$= \frac{10k \times 20k \times 140\mu A \times 2.6}{2 \times 1.20}$$

$$= 30.3k$$

An external addition to R_3 of 10k is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{RECT} to V_{CC} of about 3M provides matching of the Bell low-level tracking curve, and the 2μF value of C_{RECT} provides the proper attack and release times. A 16k resistor from the summing node to ground biases the output to $7V_{DC}$.

VOLTAGE-CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage-controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of −6dB/V. Trim networks are shown to null out distortion and DC shift, and to fine trim gain to 0dB with 0V of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20} = 100k), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant ($C_6 \times R_1$) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a −6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9V of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a 0V bias at A_1's output.

With a 0V control voltage, R_{19} should be adjusted for 0dB gain. At 1V(−6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output DC bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than 0.1% distortion at any gain with a DC output voltage variation of only a few millivolts. The clipping level (140μA into Pin 3, 14) is ±10V peak. A signal-to-noise ratio of 90dB can be obtained.

If several VCAs must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hook-up is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dB for an input range of +14 to −43dB at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}\ (\text{avg})}\right);$$

$$I_B = 140\mu A$$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})} \text{ where}$$

$$\frac{V_{IN}}{V_{IN}\ (\text{avg})} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{RECT}, and an internal 10k resistor.

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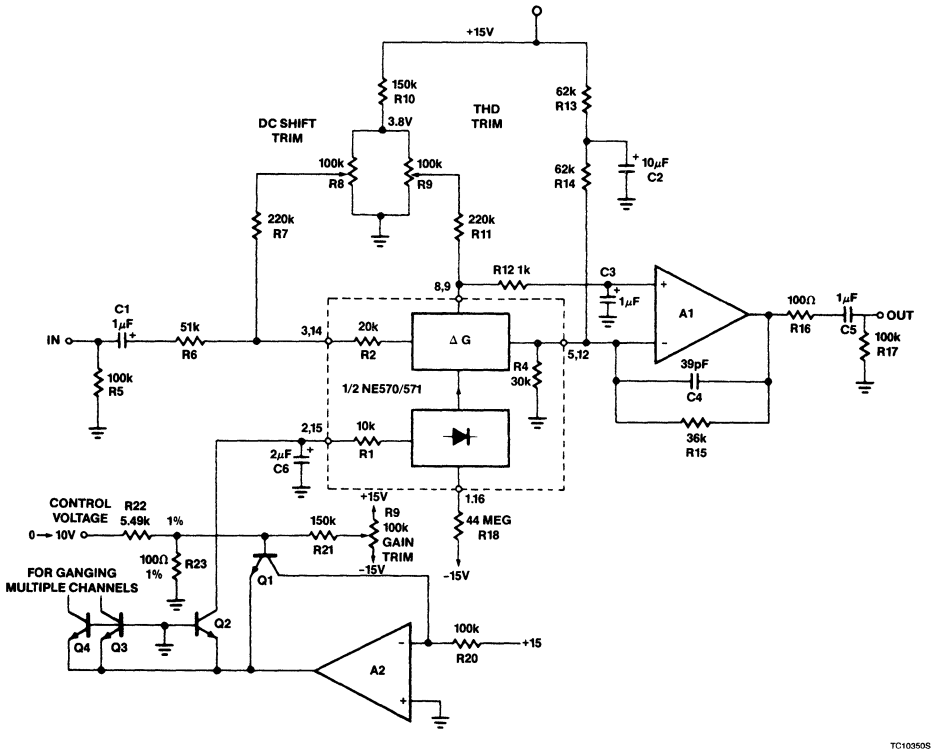

Figure 16. Voltage-Controlled Attenuator

$\tau = 10k\ C_{RECT}$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation:

$$THD = \left(\frac{1\mu F}{C_{RECT}}\right)\left(\frac{1kHz}{freq.}\right) \times 0.2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hook-up to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI-FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 2) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about 0.6V/μs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply $10k \times C_{RECT}$, but is really:

$$\left(10k + 2\left(\frac{0.026V}{I_{RECT}}\right)\right) \times C_{RECT}$$

Applications for Compandors: NE570/571/SA571 AN174

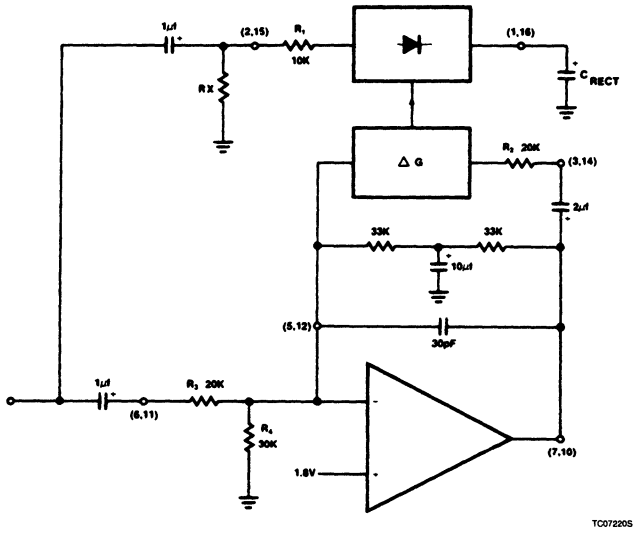

Figure 17. Automatic Level Control

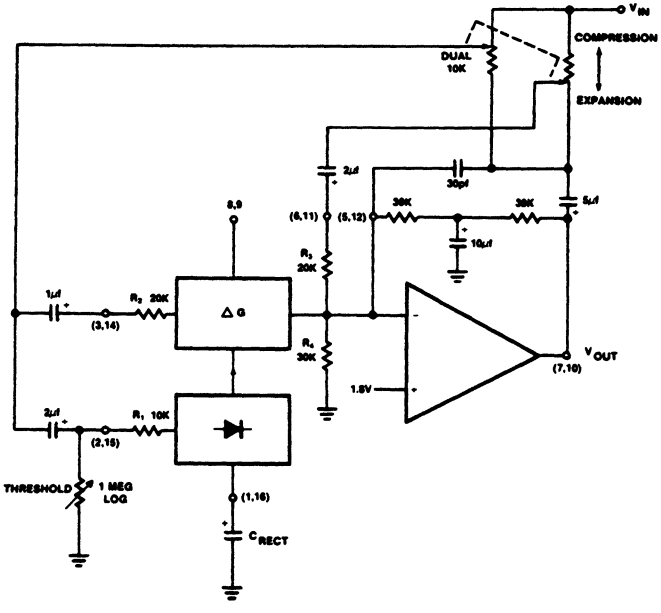

Figure 18. Variable Slope Compressor-Expandor

When the rectifier input level drops from 0dBm to −30dBm, the time constant increases from $10.7k \times C_{RECT}$ to $32.6k \times C_{RECT}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded, the output will attempt to swing rail to rail. This compressor is limited to approximately a $7V_{P-P}$ output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1µF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system

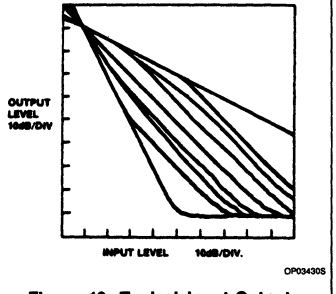

Figure 19. Typical Input-Output Tracking Curves of Variable Ratio Compressor-Expandor

Applications for Compandors: NE570/571/SA571 AN174

is changing gain, the change in the background noise level can sometimes be heard.

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dB. Trim networks are shown for distortion (THD) and DC shift. The distortion trim should be done first, with an input of 0dB at 10kHz. The DC shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

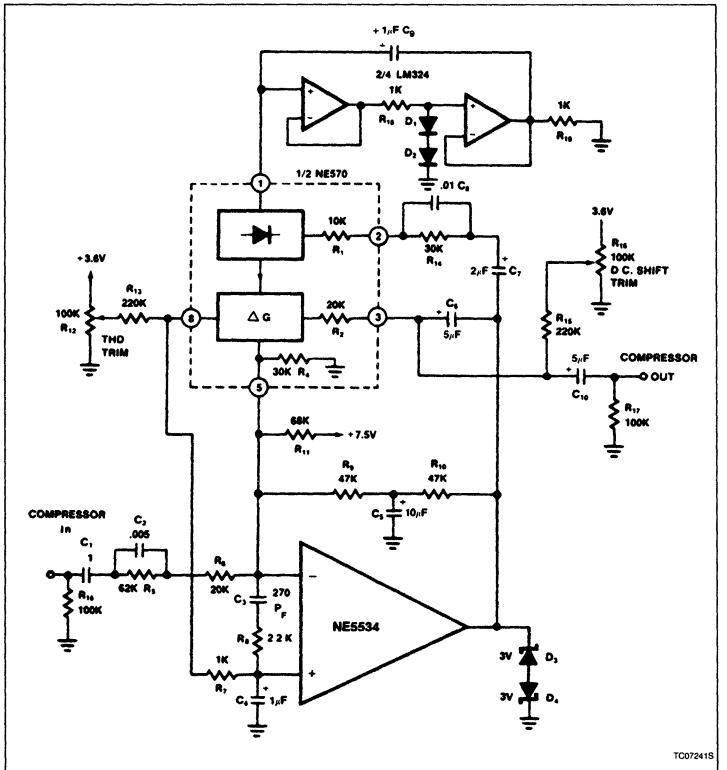

Figure 20. Hi-Fi Compressor With Pre-emphasis

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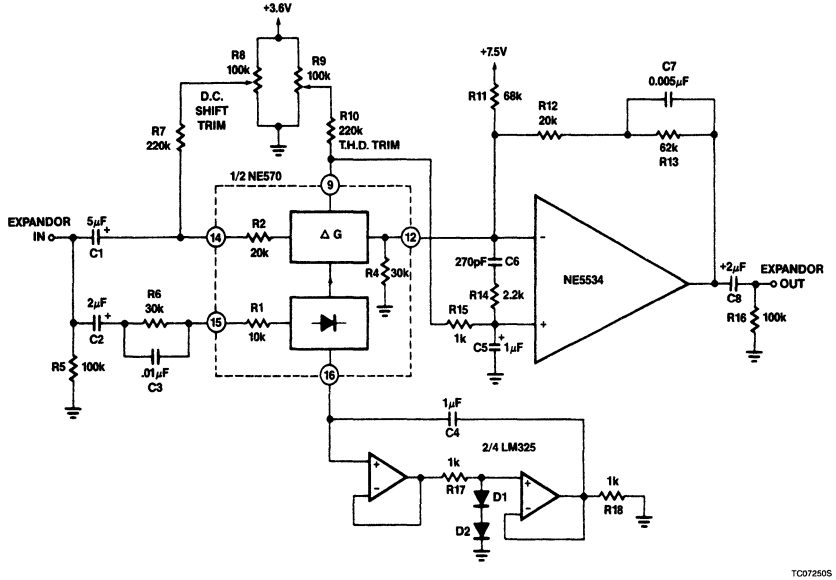


Figure 21. Hi-Fi Expandor With De-emphasis

4

Signetics

AN176
Compandor Cookbook

Application Note

Linear Products

Compandors are versatile, low cost, dual-channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? Compandor is the contraction of the two words compressor and expandor. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape: to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max. dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal (note that the larger signal would *not* be clipped when transmitted).

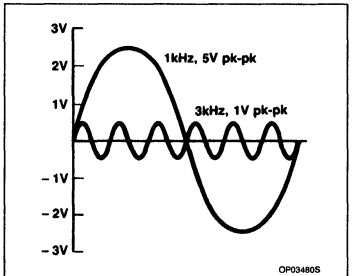


Figure 1. Original Signal Input

Figure 2. Wide-Band Noise Floor of Transmission Line

The received/playback signal is processed (expanded) in exactly the same — only inverted — ratio as the input signal was compressed. The end result is a clean, undistorted signal with a high signal-to-noise ratio.

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of

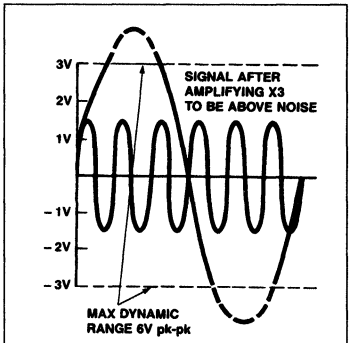


Figure 3

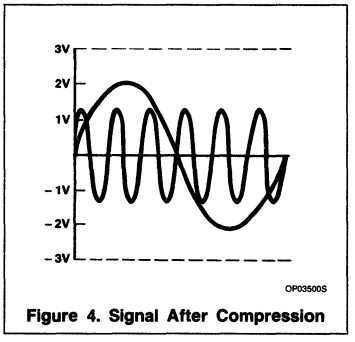
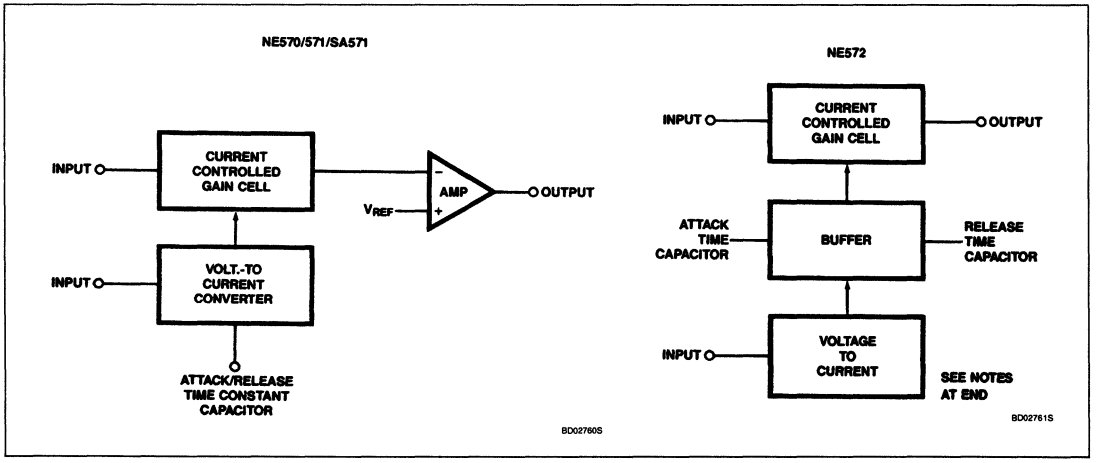


Figure 4. Signal After Compression

BLOCK DIAGRAMS



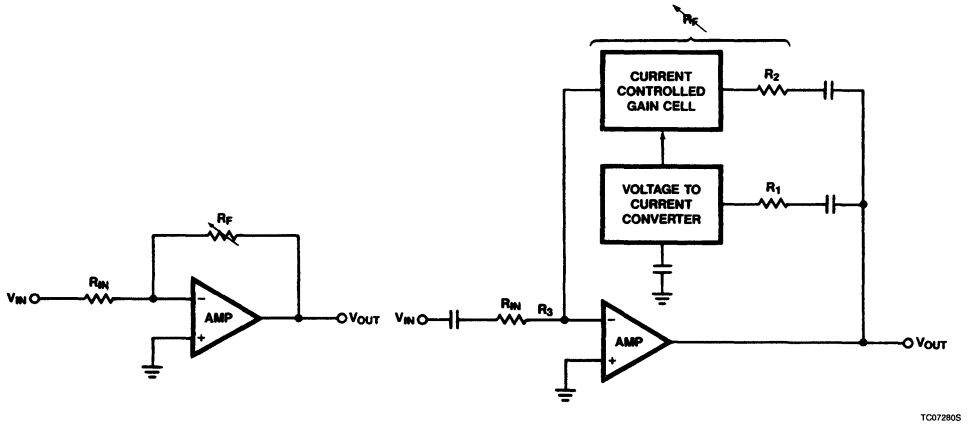


Figure 5. Basic Compressor

three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For comprehensive technical information consult the Compandor Product Guide or the Linear Data Manual.

The basic blocks in a compandor are the current-controlled variable gain cell (ΔG), voltage-to-current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572).

The operational amplifier is the main signal path and output drive.

The full-wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a Compressor, Expandor, and Automatic Level Controller or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium, such as telephone lines, RF and satellite transmissions, and magnetic tape. The Compressor can also limit the level of a signal.
2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.
3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.
4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. A NE570/571 has been used in all of the circuits. If high-fidelity audio or separately programmable attack and decay time are needed, the NE572 with a low noise op amp should be used.

The compressor (see Figure 5) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $A_V = -R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F) (See Figure 5).

As the input signal increases above the crossover level of 0dB, the variable resistor decreases in value. This causes the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dB, an increase in input signal causes the variable resistor to increase in value, thereby causing the output signal's amplitude to increase.

In the compressor configuration, the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$\text{Gain comp.} = \left[\frac{R_1 R_2 I_B}{2\ R_3 V_{IN(avg)}}\right]^{1/2}$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$

$V_{IN(avg)} = 0.9(V_{IN(RMS)})$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 6 is designed around a system supply of 6V, thus the output DC level should be 3V.

$$V_{OUT\ DC} = (1 + (2R_{DC}/R_4))\ V_{REF}$$

where: $R_4 = 30k$
$V_{REF} = 1.8V$
R_{DC} is external

manipulating the equation, the result is. . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.

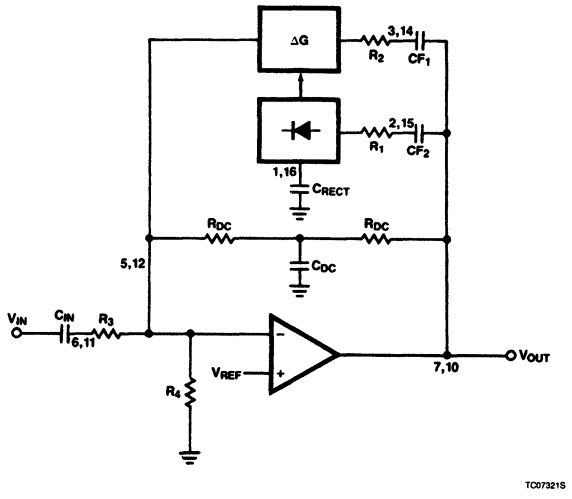
   a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

   b) if larger than 3.0V peak, R_1 will *also* need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies ($X_C = 1/(6.28xf)$).
4) The C_{RECT} should be 1μF to 2μF for initial setup. This directly affects Attack and Release times.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) Pre-emphasis may be used to reduce noise-pumping, breathing, etc., if present. See the NE570/571 data sheet for specific details.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.
8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 7). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $A_V = -R_F/R_{IN}$.



NOTES:
Max AC current into:
· Gaincell is 140μA peak
· Rectifier is 300μA peak
All components are internal, except the caps and R_{DC}

Figure 6. Basic Compressor

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase (refer to Figure 10).

Below the crossover level, an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

In the expandor configuration the rectifier is connected to the input.

The complete equation for the expandor gain is:

$$\text{Gain expandor} = (2R_3V_{IN}(avg))/R_1R_2I_B$$

where: $R_1 = 10k$
$R_2 = 20k$
$R_3 = 20k$
$I_B = 140\mu A$
$V_{IN}(avg) = 0.9\ (V_{IN(RMS)})$

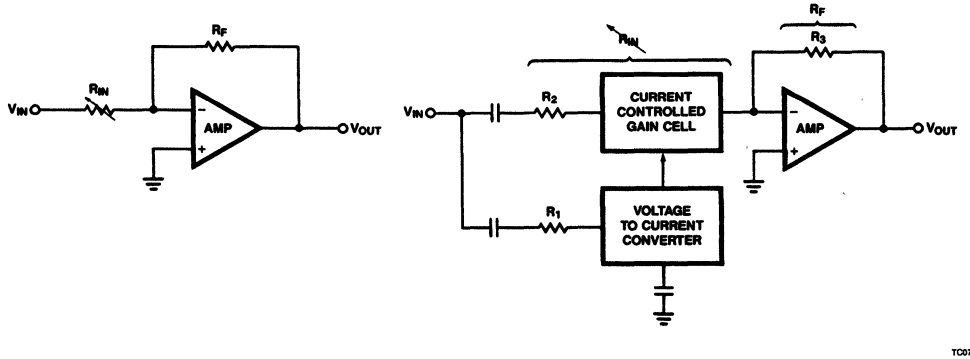


Figure 7. Basic Expandor

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EXPANDOR RECIPE

1) DC bias the output halfway between the supply and ground to get maximum headroom. The circuit in Figure 8 is designed around a system supply of 6V so the output DC level should be 3V.

$V_{OUT\ DC} = (1 + R_3/R_4)V_{REF}$
where: $R_3 = 20k$
$R_4 = 30k$
$V_{REF} = 1.8V$

Note that when using a supply voltage higher than 6V the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would also affect the expandor's AC gain and thus cause a mismatch in a companding system.)

2) Analyze the input signal's anticipated amplitude:

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will *also* need to be increased. (see INGREDIENTS)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.
4) The C_{RECT} should be 1μF to 2μF for initial setup.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the Hi-Fi Expandor application in the Linear Data Manual.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.
8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 9), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the Compressor) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

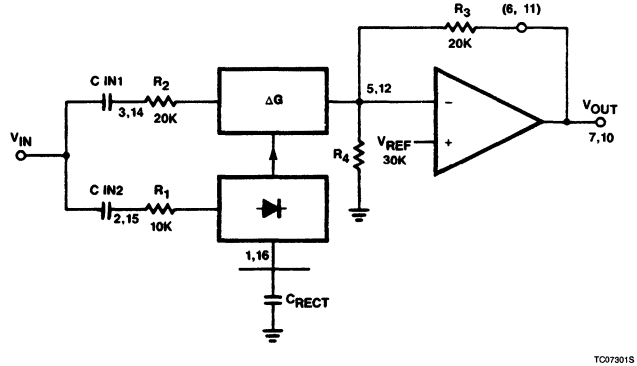
As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

The complete gain equation for the ALC is:

$$\text{Gain} = \frac{R_1 R_2 I_B}{2\ R_3\ V_{IN(avg)}}$$

$$\text{Output level} = \frac{R_1 R_2 I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

$$\text{where}\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$



NOTE:
All components are internal except caps

Figure 8. Basic Expandor

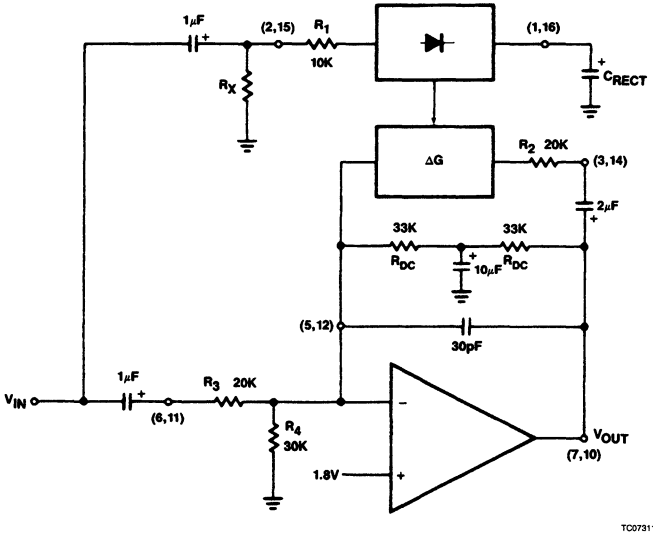


Figure 9. Automatic Level Control

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added. The modified gain equation is:

$$\text{Gain max.} = \frac{\left(\frac{R_1 + R_X}{1.8V}\right) \times R_2 \times I_B}{2\ R_3}$$

$R_X \cong$ ((desired max gain) $\times$ 26k) – 10k

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10kΩ) limits input current to the rectifier. This current should not exceed an AC peak value of ± 300μA. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ±3.0V peak (i.e., 10k $\times$ 300μA = 3.0V).

R_2 (20kΩ) limits input current to the variable gain cell. This current should not exceed an AC peak value of ± 140μA. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ±2.8V (i.e., 20k $\times$ 140μA).

R_3 (20kΩ) acts in conjunction with R_4 as the feedback resistor (R_F) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30kΩ) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{OUT\ DC} = (1 + (R_3/R_4))V_{REF}$
(for the Expandor)
$V_{OUT\ DC} = (1 + (2R_{DC}/R_4))V_{REF}$
(for the Compandor, ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output halfway between the supply rails for largest headroom (usually some positive voltage and ground).]

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: 10k $\times$ C_{RECT}

The total harmonic distortion (THD) is approximated by:

$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$

NOTES:
The NE572 differs from the 570/571 in that:
1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 10 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of +16dB and minimum amplitude of –80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (–40dB is increased to –20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the –60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

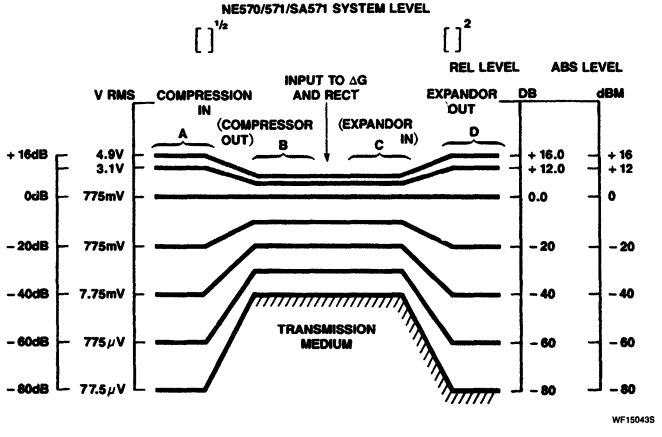


Figure 10. System Levels of a Complete Companding System

WHAT IS COMPANDING??

Shown here are some scope pictures of what three functions of the compandor look like in the kitchen, responding to tone bursts of varying amplitudes.

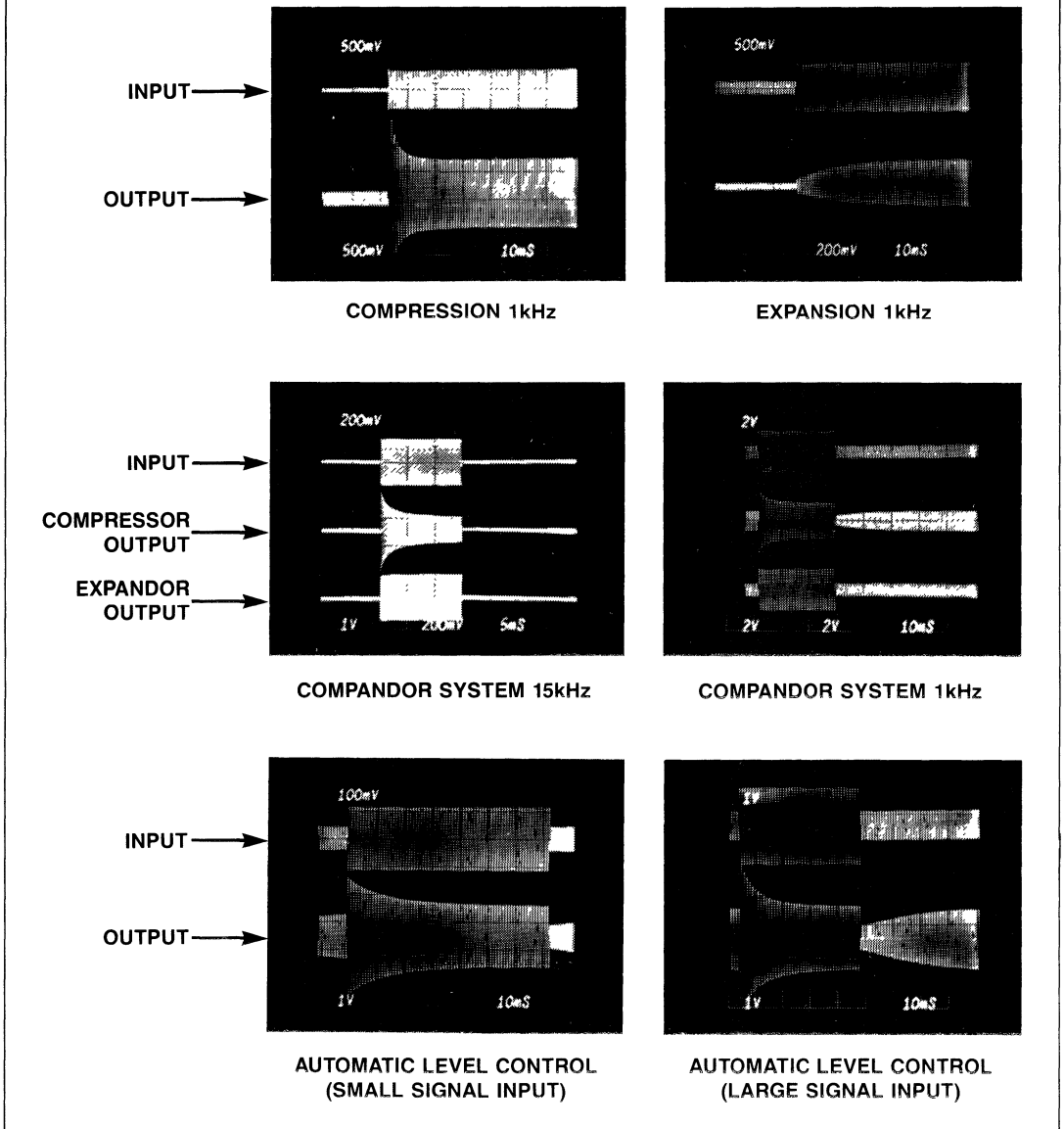


Figure 11

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APPLICATION BOARD

Shown below is the schematic (Figure 12) for Signetics' NE570/571 evaluation/demo board. This board provides one channel of Expansion and one channel of Compression (which can be switched to Automatic Level Control).

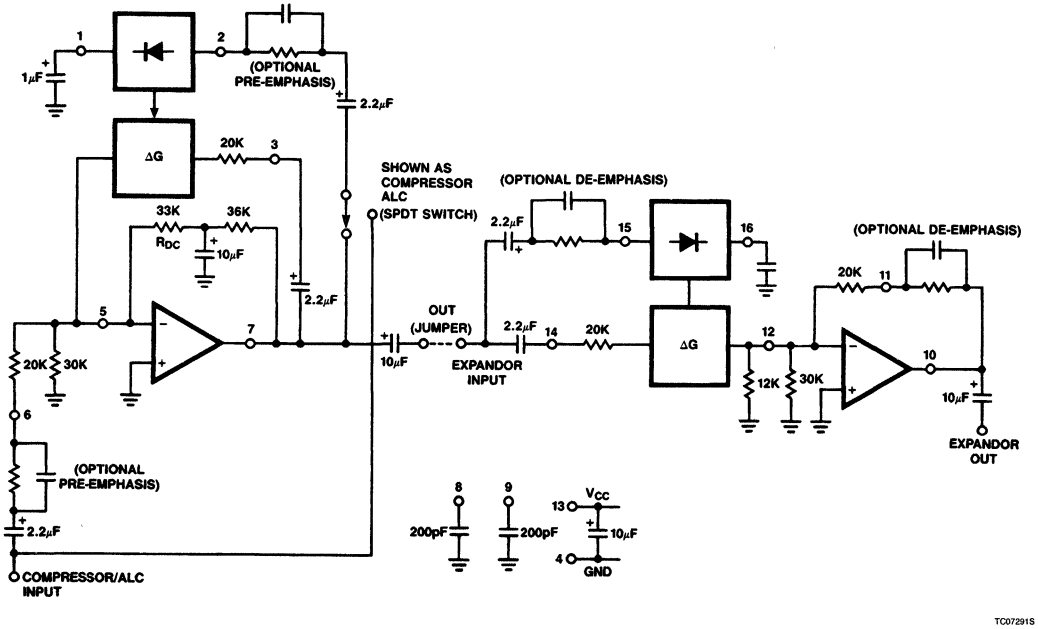


Figure 12

Signetics

NE570/571/SA571
Compandor

Product Specification

Linear Products

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

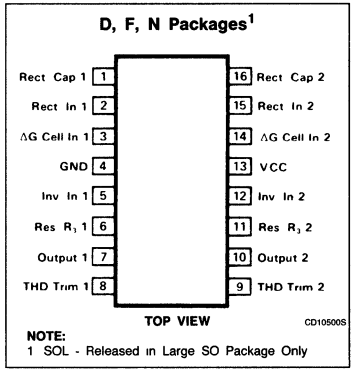
FEATURES

- **Complete compressor and expandor in one IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

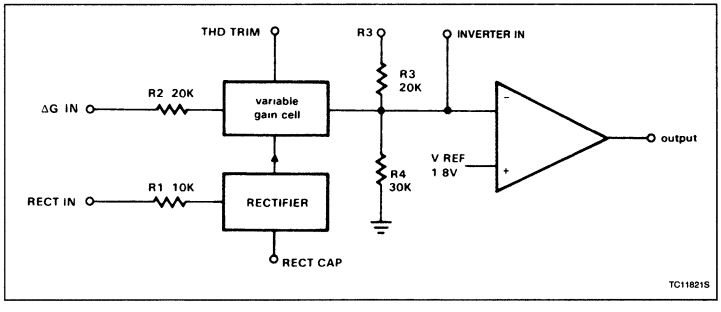


NOTE:
1 SOL - Released in Large SO Package Only

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic Cerdip	0 to +70°C	NE571N
16-Pin Cerdip	−40°C to +85°C	SA571F
16-Pin Plastic DIP	−40°C to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive supply 570 571	 24 18	V_{DC}
T_A	Operating ambient temperature range NE SA	 0 to +70 −40 to +85	 °C °C
P_D	Power dissipation	400	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15V$. Except where indicated, the 571 specifications are identical to those of the 570.

SYMBOL	PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/μs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±50		±30	±100	mV
	Expandor output noise	No signal, 15Hz − 20kHz[1]		20	45		20	60	μV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
	Gain change[2, 4]	−40°C < T < 70°C 0°C < T < 70°C		±0.1 ±0.1	 ±0.2		±0.1 ±0.1	 ±0.4	dB
	Reference drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+2, −25 ±5	+10, −40 ±10		+2, −25 ±5	+20, −50 ±20	mV
	Resistor drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+8, −0 +1.−0					%
	Tracking error (measured relative to value at unity gain) equals [$V_O - V_O$ (unity gain)] dB − V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = −30dBm, V_1 = 0dB		±0.2 +0.2	 −0.5, +1		 +0.2	 −1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{-t/\tau} + G_{final},\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

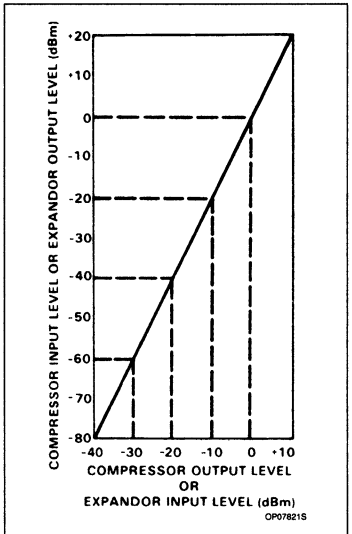
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

The output stage is capable of ± 20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

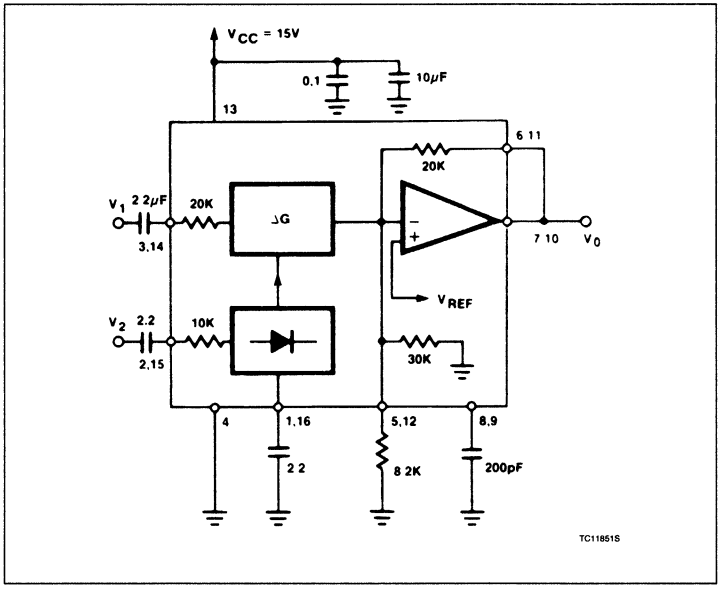
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (< 0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to −80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

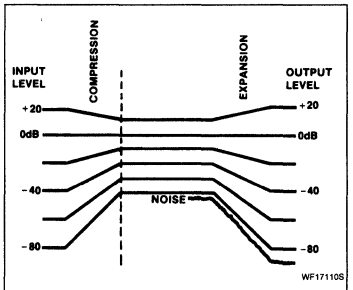


Figure 1. Restricted Dynamic Range Channel

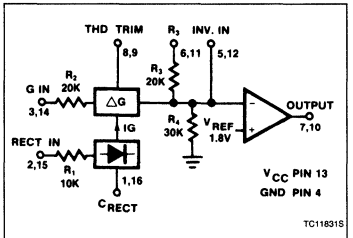


Figure 2. Chip Block Diagram (1 of 2 Channels)

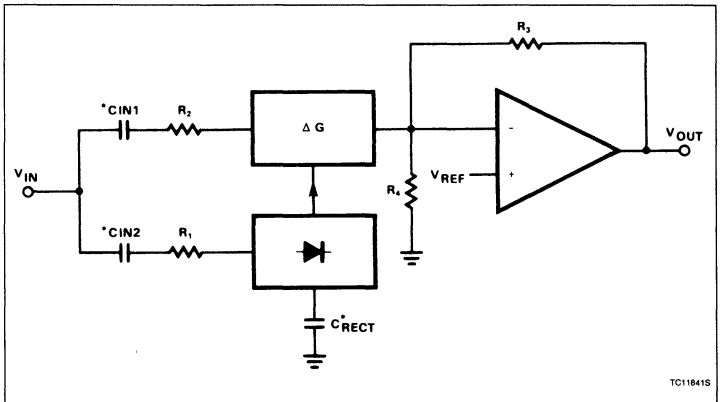
The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DC\ TOT}}{30k}\right) 1.8V$$



NOTES:

$$GAIN = \frac{2\ R_3\ V_{IN}\ (avg)}{R_1\ R_2\ I_B}$$

$I_B = 140\mu A$

*External components

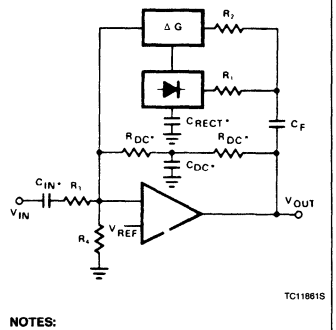
Figure 3. Basic Expandor

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4} V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k} \right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN}\ (avg)} \right)^{1/2}$$

$I_B = 140\mu A$
*external components

Figure 4. Basic Compressor

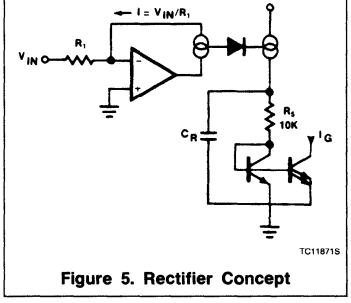
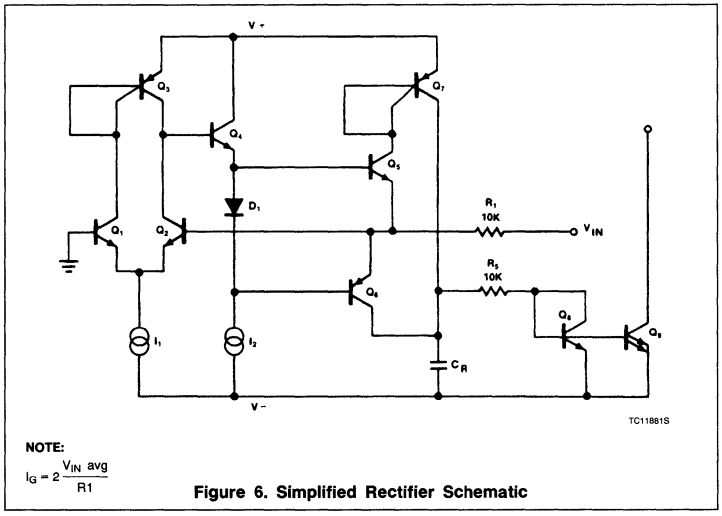


Figure 5. Rectifier Concept

CIRCUIT DETAILS — RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$$I_G = 2 \frac{V_{IN}\ avg}{R1}$$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

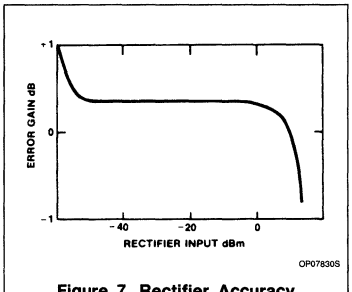


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, −20dBm, and −40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

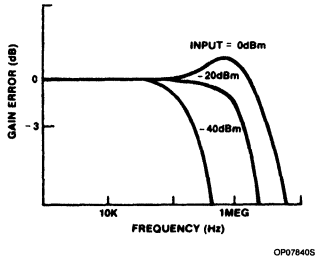


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

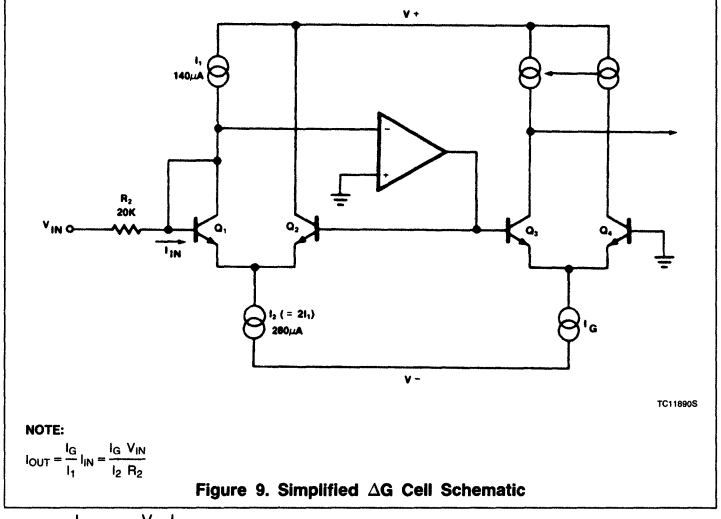
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G\, V_{IN}}{I_2\, R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2} \frac{I_G}{I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

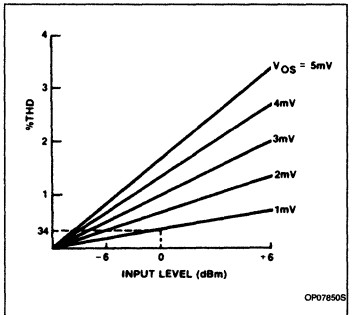


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

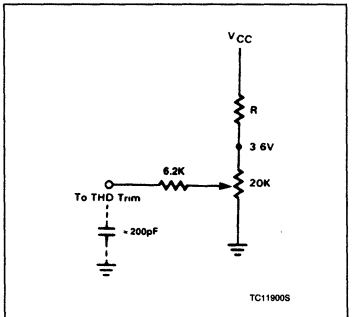


Figure 11. THD Trim Network

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

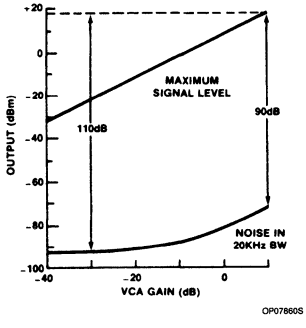


Figure 12. Dynamic Range of NE570

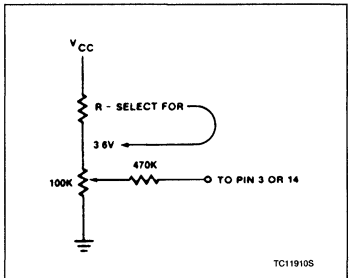


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

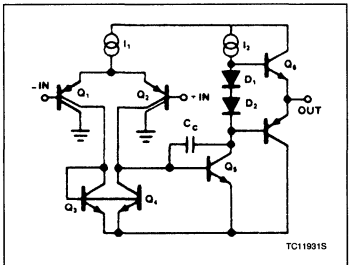


Figure 14. Operational Amplifier

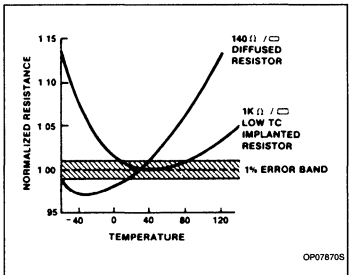


Figure 15. Resistance vs Temperature

Signetics

NE/SA572
Programmable Analog Compandor

Product Specification

Linear Products

DESCRIPTION

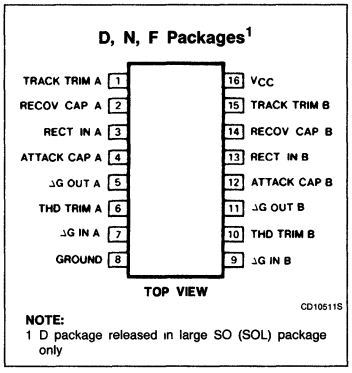
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1 D package released in large SO (SOL) package only

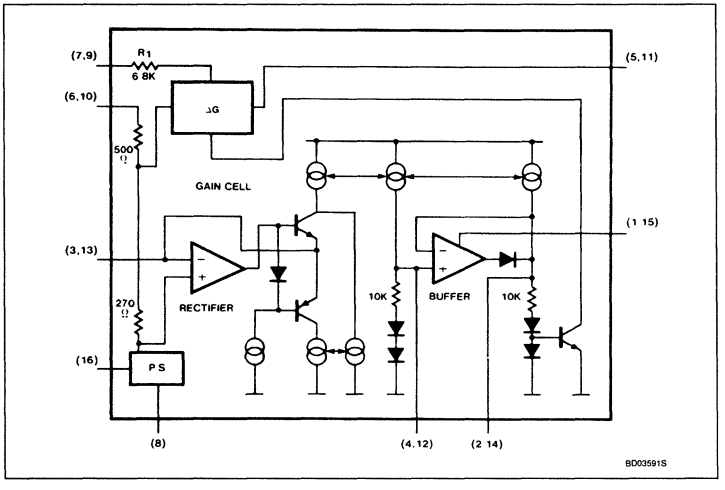
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	−40°C to +85°C	SA572D
16-Pin Cerdip	−40°C to +85°C	SA572F
16-Pin Plastic DIP	−40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 −40 to +85	°C
P_D	Power dissipation	500	mW

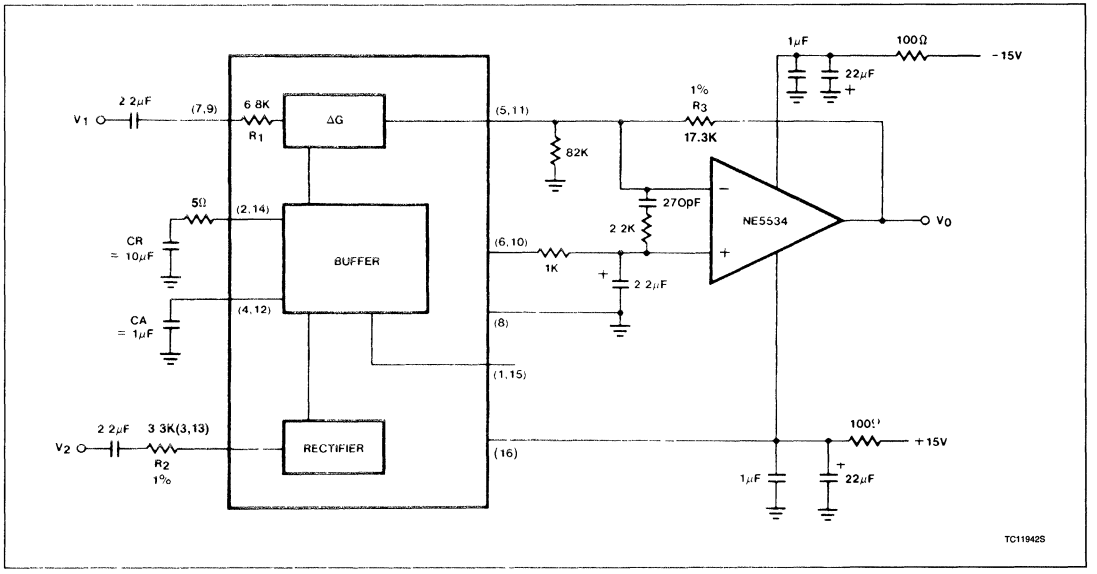
DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A = 1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R = 10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 − 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = $[V_O - V_O$ (unity gain)]dB $- V_2$dB	Rectifier input V_2 = +6dB V_1 = 0dB V_2 = −30dB V_1 = 0dB		±0.2 ±0.5	 −1.5 +0.8		±0.2 ±0.5	 −2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

Programmable Analog Compandor | NE/SA572

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications The NE572 is a dual channel gain control IC Each channel has a linearized, temperature-compensated gain cell and an improved level sensor In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BEQ3-Q4} = \Delta_{BEQ1-Q2}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin.

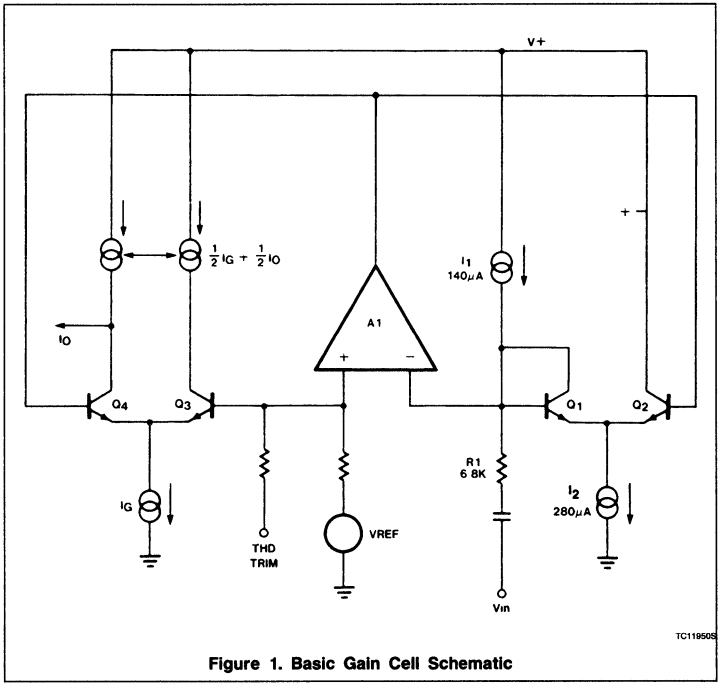


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

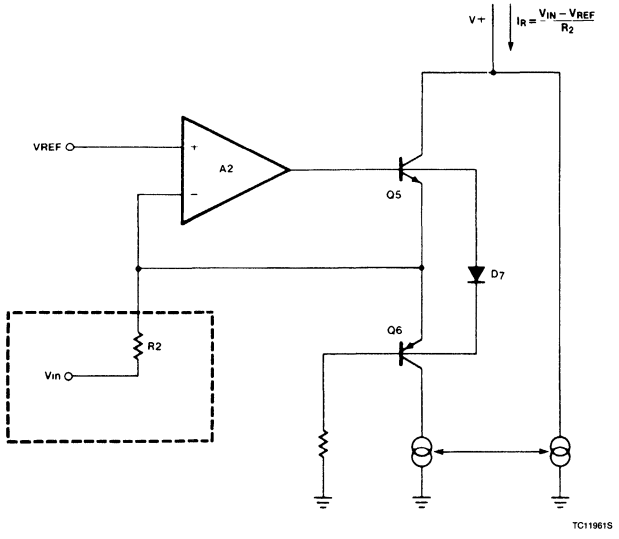


Figure 2. Simplified Rectifier Schematic

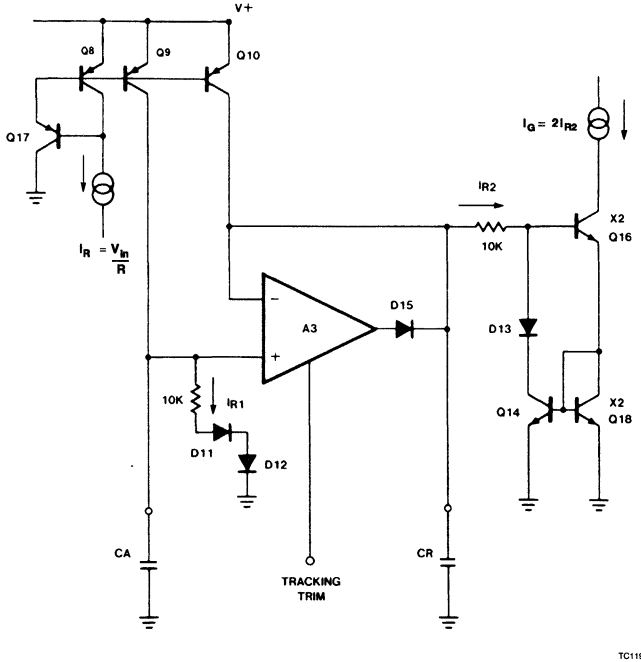


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR · R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

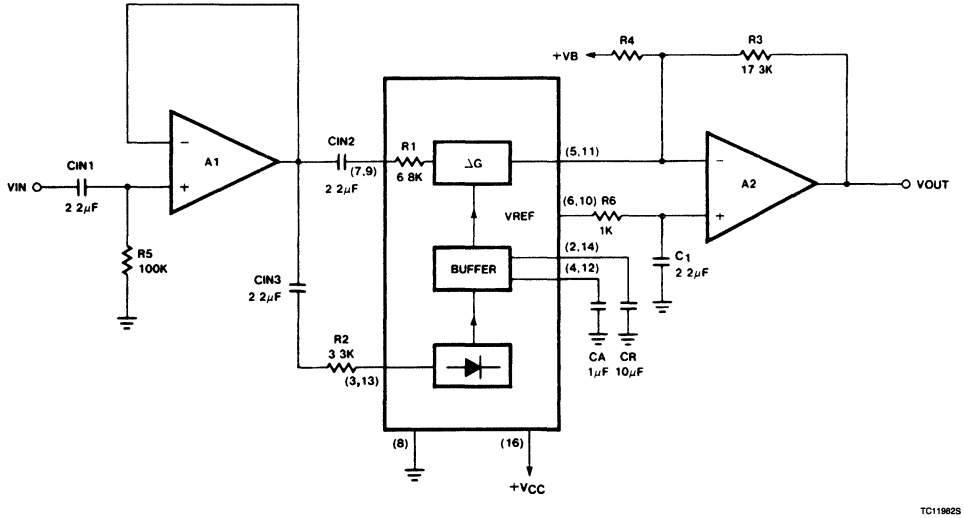


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

($I_1 = 140\mu A$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right)$$

$$- V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

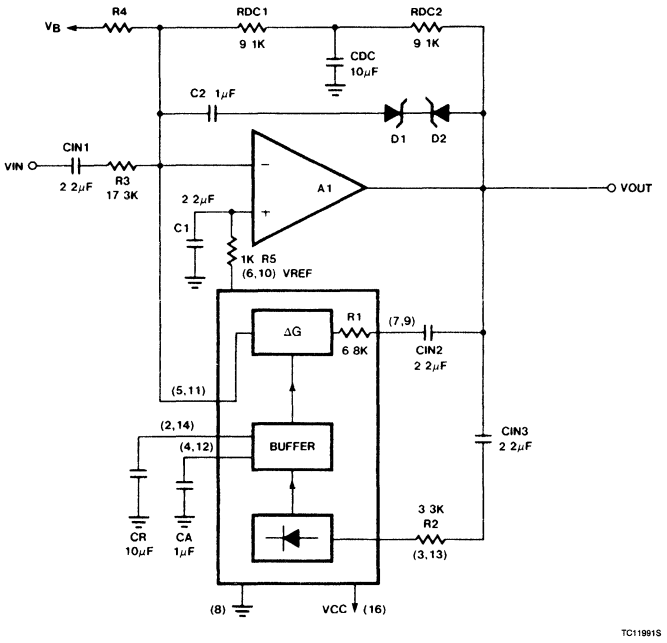


Figure 5. Basic Compressor Schematic

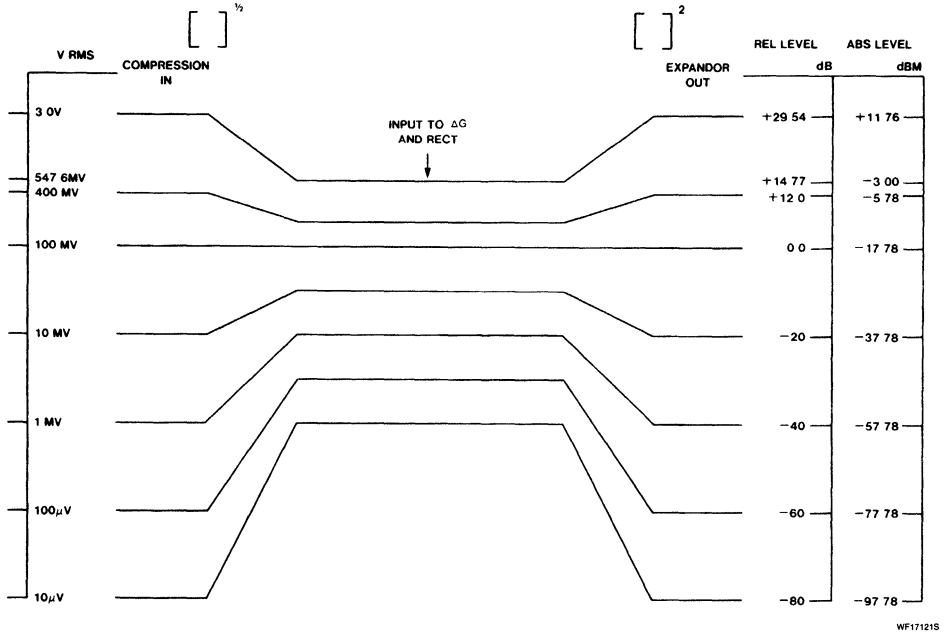


Figure 6. NE572 System Level

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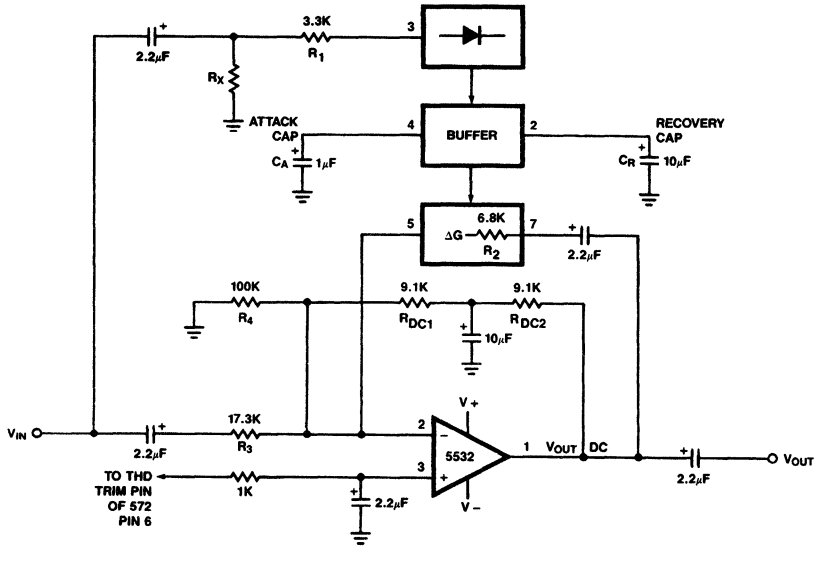
Signetics

AN175
Automatic Level Control Using the NE572

Application Note

Linear Products

NE572 AUTOMATIC LEVEL CONTROL



$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

WHERE $R_4 = 100k$
$R_{DC1} = R_{DC2} = 9\ 1k$
$V_{REF} = 2\ 5V$

$$\text{OUTPUT LEVEL} = \left(\frac{R_1 R_2 I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

$$\text{GAIN} = \frac{R_1 R_2 I_B}{2R_3 V_{IN}\ (avg)}$$

WHERE $R_1 = 6\ 8k$ (Internal)
$R_2 = 3\ 3k$
$R_3 = 17\ 3k$
$I_B = 140\mu A$

ATTACK TIME = (10k) C_A

RECOVERY TIME = (10k) C_R

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X

$$\text{GAIN MAX} = \frac{\frac{R_1 + R_X}{2\ 5V} \times R_2 \times I_B}{2R_3}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1\ 11$$
(FOR SINE WAVES)

NOTE:
Pin numbers are for side A of the NE572.

Signetics

NE/SA575
Low Voltage Compandor

Product Specification

Linear Products

DESCRIPTION

THE NE/SA575 is a precision dual gain-control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

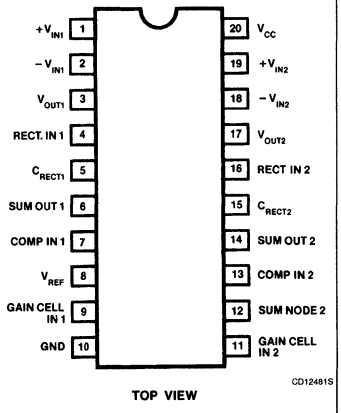
- **Operating voltage range from 3V to 7V**
- **Reference voltage of $100mV_{RMS}$ = 0dB**
- **One dedicated summing op amp per channel and two extra uncommitted op amps**
- **600Ω drive capability**
- **Single or split supply operation**
- **Wide input/output swing capability**

APPLICATIONS

- **Portable communications**
- **Cellular radio**
- **Cordless telephone**
- **Consumer audio**
- **Portable broadcast mixers**
- **Wireless microphones**
- **Modems**
- **Electric organs**
- **Hearing aids**

PIN CONFIGURATION

D[1] and N Packages



TOP VIEW

NOTE:
1 Available in large SO package only

ORDERING INFORMATION

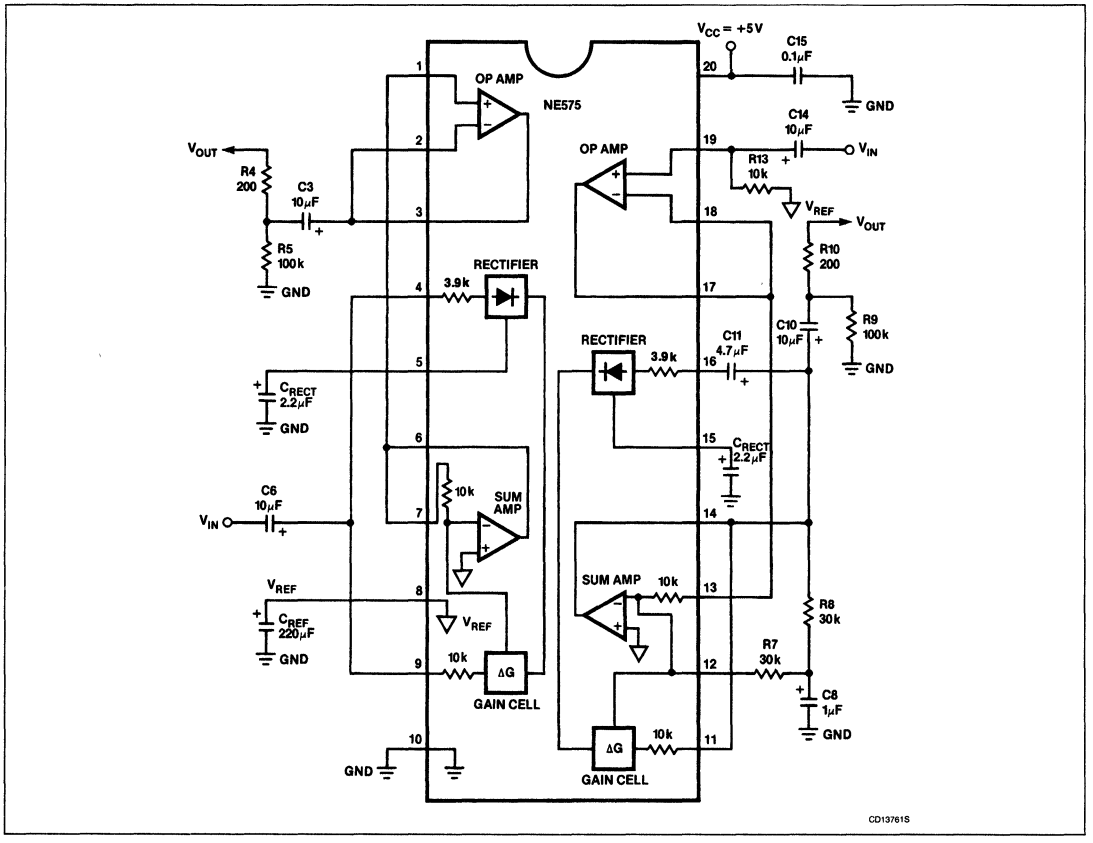
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE575N
20-Pin Plastic SOL	0°C to +70°C	NE575D
20-Pin Plastic DIP	-40°C to +85°C	SA575N
20-Pin Plastic SOL	-40°C to +85°C	SA575D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE575	SA575	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

Low Voltage Compandor NE/SA575

BLOCK DIAGRAM



See NOTES in back of this book for additional drawings.

ELECTRICAL CHARACTERISTICS

Typical values are at $T_A = 25°C$. Minimum and Maximum values are for the full operating temperature range 0 to 70°C for NE575, −40 to +85°C for SA575 $V_{CC} = 5V$, unless otherwise specified Both channels are tested in the Expandor mode (see Figure 1)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE575			SA575			
			Min	TYP	Max	Min	Typ	Max	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4	5 5	3	4	5.5	mA
V_{REF}	Reference voltage[2]	$V_{CC} = 5V$	2 4	2 5	2 6	2 4	2 5	2 6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3 5kHz		0 12	1 0		0.12	1 5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S=0Ω		6	20		6	30	μV
0dB	Unity gain level	1kHz	−1 0		1 0	−1.5		1 5	dB
V_{OS}	Output voltage offset	No signal	−100		100	−150		150	mV
	Output DC shift	No signal to 0dB	−50		50	−100		100	mV
	Tracking error relative to 0dB	1kHz, +6dB to −30dB	−0 5		0.5	−1 0		1.0	dB
	Crosstalk	1kHz, 0dB, $C_{REF} = 220\mu F$		−80	−65		−80	−65	dB
For operational amplifier									
V_O	Output swing	$R_L = 10k\Omega$	V_{CC} −0.4	V_{CC} −0.2		V_{CC} −0 4	V_{CC} −0 2		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN}=0 5V to 4 5V	−0 3		0 3	−0.5		0 5	μA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	$R_L = 10k\Omega$		80			80		dB
SR	Slew rate	Unity gain		1			1		V/μs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1 Operation down to $V_{CC} = 2V$ is possible, but performance is significantly reduced See curve in Figure 5
2 Reference voltage, V_{REF}, is typically at $1/2V_{CC}$

DESCRIPTION OF OPERATION

This section describes the basic subsystems and applications of the NE/SA575 Compandor More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE575 low voltage compandor in an Expandor (1·2), Compressor (2.1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively

The NE575 has two channels for a complete companding system. The left channel A can be configured as a 1·2 Expandor while the right channel B can be configured as either a 2·1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell In addition, the NE575 also has two additional high performance uncommitted op amps which can be utilized for applications such as filtering, pre-emphasis/de-emphasis or buffering

Figure 4 shows the complete schematic for the applications demo board Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit The switch S1 toggles the circuit between compressor and ALC mode Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz A circuit schematic for voice (300Hz to 3kHz) is shown in Figure 6

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted Capacitors C3, C5, C8 and C12 are for DC blocking, and R4 and R8 provide termination (for the capacitors) In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R5 and R12 provide DC reference voltage to the amplifiers of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple. Figure 5 shows the PC board layout of the applications demo board.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from −34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of −30 to +10dB.

In the compressor mode, the typical input dynamic range was from −42dB to +18dB with a tracking error of ±0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from −42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For inputs greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R7 and R8 to 20kΩ each. The second is to add a current limiting resistor in series with C13 at Pin 13. The third is to add a compensation capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 of V_{CC} which biases the summing amplifier at 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3, C5, R3 and R4 can be eliminated thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2 respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.9k\times 100\mu A}$$

where $V_{IN}(avg) = 0.901V_{IN(RMS)}$

Equation 2.

$$\tau = 10k\times C_{RECT} = 10k\times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8, C12, R8 and R9 could be eliminated and only R5, R6, R7, C7 and C13 would be required. If the external components R5, R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4 respectively.

Equation 3.

$$\text{Compressor Gain} = \left[\frac{3.9k\times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

Equation 4.

$$\tau_R = \tau_A = 10k\times C_{RECT} = 10k\times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13, C8, R8 and R9 could be eliminated. Concerning the compressor, removing R5, R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6 respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.9k\times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k\times C_{RECT} = 10k\times C9$$

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Linear Products

Section 5
Data Communications

INDEX

5

Symbols and Definitions for Line Drivers

Current Into or Out of Slew Control Pin (I_{SLEW})

Differential Output Voltage (V_O or $\overline{V}_O$, V_T or $\overline{V}_T$)

For a differential line driver (i.e., an RS-422 driver) this is the differential output voltage for an input voltage which is a logic HIGH (V_O) or LOW ($\overline{V}_O$) V_O is usually measured with no applied output load while V_T is the differential output voltage with a specified output load.

Enable

For line drivers and receivers having an $\overline{\text{ENABLE}}$ (or ENABLE) input, the application of a specified logic voltage to this input will force the outputs into a high resistance (High-Z) state. In this state, the circuit has a minimal loading effect on the transmission or bus line being driven by the output.

Failsafe (FS)

For line receivers having a FAILSAFE (FS) input, the application of specified voltages to this input will force the outputs to correspondingly specified logic states, V_{OFS} (defined below), when fault conditions occur on the transmission line.

Failsafe Output Voltage (V_{OFS})

For line receivers· the voltage to which the outputs are forced when specified fault conditions occur on the transmission line and when a specified voltage is applied to the FAILSAFE (FS) input.

Hysteresis (V_H)

For line receivers: the difference between the high and low threshold voltages, V_{TH} and V_{TL} (defined below).

Input Current (I_{IN})

For a line receiver· the current flowing into the transmission line input at a specified input voltage.

Input Clamp Voltage (V_{CL})

For a line driver: the input voltage applied to an input below which the driver clamps this voltage. V_{CL} is specified for a particular current flowing from the driver into the voltage source.

Input High Current (I_{IH})

The current flowing into or out of a Logic input when a specified Logic HIGH voltage is applied to that input (2.7V).

Input High Current (I_I)

The current into or out of a Logic input when V_{CC} is applied to that input (5.5V).

Input High Threshold Voltage (V_{TH})

For a line receiver: the differential input voltage at the transmission line input above which the output is in a defined logic state.

Input High Voltage (V_{IH})

The range of input voltages recognized by a logic input as a logic HIGH.

Input Low Current (I_{IL})

The current flowing into or out of a logic input when a specified logic LOW voltage is applied to that input.

Input Low Threshold Voltage (V_{TL})

For a line receiver: the differential input voltage below which the output is in a defined logic state

Input Low Voltage (V_{IL})

The range of input voltages recognized by a logic input as a logic LOW.

Input Resistance (R_{IN})

For a line receiver· the DC resistance of the transmission line input over a specified input voltage range.

Mode

For line drivers having a MODE input the application of specified voltages to this input will force the driver outputs to comply with correspondingly specified EIA transmission standards, e g., RS-232 or RS-423.

Negative Power Supply Current (I_{EE})

Open-Circuit Input Voltage (V_{IOC})

For a line receiver the voltage to which the transmission line input of the circuit reverts when no external connection is made at this input.

Output Current High-Z (I_O)

The current flowing into or out of an output when that output is in a High-Z state (see ENABLE definition). I_O is specified at a particular applied output voltage.

Output High Voltage (V_{OH})

The HIGH voltage at an output (for a driver or receiver) for specified load conditions, i.e., R_L or I_{OUT}, and input voltages.

Output Low Voltage (V_{OL})

The LOW voltage at an output (for a driver or receiver) for specified load conditions, i.e., R_L or I_{OUT}, and input voltages.

Output Leakage Current (I_X)

The current flowing into or out of an output when no power is applied to the circuit. I_{CEX} is specified at a particular applied output voltage and input conditions.

Output Resistance (R_{OUT})

For a line driver: the output resistance over a specified output voltage range.

Output Short-Circuit Current (I_S)

The current flowing into or out of an output when the output is connected to the generator circuit ground for a line receiver or digital ground for a line driver.

Output Unbalance Voltage ($|V_{OH}| - |V_{OL}|$, $|V_T| - |\overline{V}_T|$)

For a line driver: the difference between the absolute values of V_{OH} and V_{OL} or V_T and $\overline{V}_T$.

Output Offset Voltage (V_{OS} or $\overline{V}_{OS}$)

For a differential line driver, i.e. RS-422, the difference between the actual voltage at the center of the output load and the generator circuit ground. V_{OS} is measured with V_T at the output and $\overline{V}_{OS}$ with $\overline{V}_T$ at the output.

Positive Power Supply Current (I_{CC})

Propagation Delay (t_{PXX})

The time delay between specified reference points on the input and output waveforms of a line driver or receiver. The symbol X can be H, L or Z specifying HIGH, LOW or High-Z, respectively; i.e , t_{PLZ} is the propagation delay for the output of a line driver to change from an output LOW to a High-Z state after the application of a signal to the $\overline{\text{ENABLE}}$ input.

Rise and Fall Times (t_R and t_F)

For a line driver: the time delays between the 10% and 90% points on the rising and falling output waveforms following a change in the logic voltage at the input.

5

Signetics

AM26LS30

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

Preliminary Specification

Linear Products

DESCRIPTION

The AM26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all the requirements of EIA Standard RS-422 or as four independent single-ended RS-423 line drivers.

In the differential mode, the outputs have individual 3-State controls. In the high impedance state, these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system consists of the AM26LS30 differential line driver and up to twelve AM26LS32 line receivers, or the AM26LS32 line receiver and up to thirty-two AM26LS30 differential drivers.

A slew control pin allows the use of an external capacitor to control slew rate for suppression of near-end cross talk to receivers in the cable.

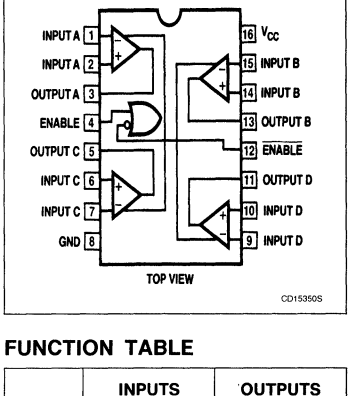
The AM26LS30 is constructed using high speed oxide isolated bipolar processing.

FEATURES

- **Dual RS-422 line driver or quad RS-423 line driver**
- **Driver outputs do not clamp line with power off or in high impedance state**
- **Individual 3-State controls when used in differential mode**
- **Low I_{CC} and I_{EE} power consumption**
  - **RS-422 differential mode: 35mW/driver typ**
  - **RS-423 single-ended mode: 26mW/driver typ**
- **Individual slew rate control for each output**
- **50Ω transmission line drive capability (RS-422 into virtual ground)**
- **Low current PNP inputs compatible with TTL, MOS and CMOS**
- **High capacitive load drive capability**
- **Exact replacement for DS16/3691**
- **High speed oxide isolated bipolar processing**

PIN CONFIGURATION

D, F and N Packages



TOP VIEW

CD15350S

FUNCTION TABLE

MODE	INPUTS		OUTPUTS	
	A (D)	B (C)	A (D)	B (C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

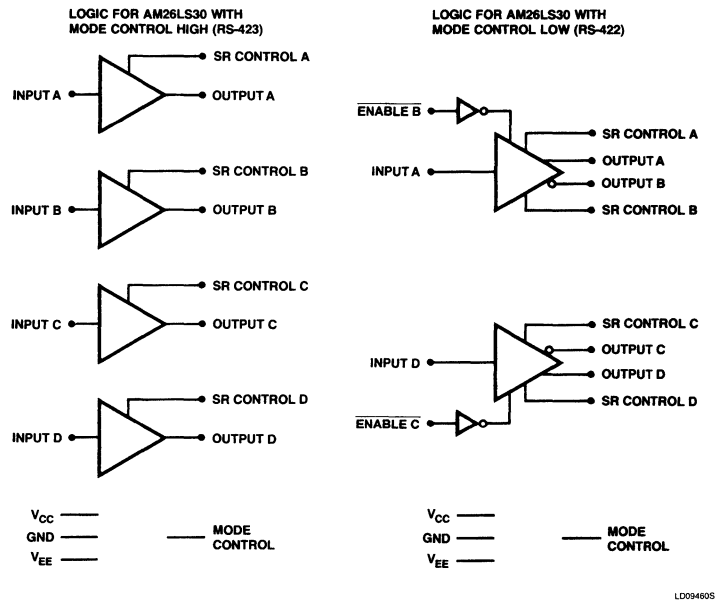
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	AM26LS30CN
16-Pin Plastic SO	0 to +70°C	AM26LS30CD
16-Pin Plastic DIP	−40°C to +85°C	AM26LS30IN
16-Pin Plastic SO	−40°C to +85°C	AM26LS30ID
16-Pin Plastic DIP	−55°C to +125°C	AM26LS30MN
16-Pin Ceramic DIP	−55°C to +125°C	AM26LS30MF

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	7	V
V_{EE}	V–	–7	V
V_{IN}	Input voltage	– 5V to V_{CC}	V
V_{OUT}	Output voltage (Power Off)	±13.5	V
P_D	Power dissipation	600	mW
T_A	Ambient temperature range AM26LS31C	0 to +70	°C
	AM26LS31I	–40 to +85	°C
	AM26LS32M	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

POWER DISSIPATION TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
N	1,488mW	11.9mW/°C	25°C
D	1,262mW	10.1mW/°C	25°C
F	1,250mW	10.0mW/°C	25°C

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Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

DC ELECTRICAL CHARACTERISTICS over the operating temperature range. The following conditions apply unless otherwise specified AM26LS30M, $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = GND$, AM26LS30C, $T_A = 0$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$; AM26LS30I, $T_A = -40$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$ **RS-422 Connection**, Mode Voltage $\leq$ 0 8V

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]		LIMITS			UNITS
				Min	Typ[1]	Max	
V_O	Differential output	$R_L = \infty$	$V_{IN} = 2.0V$		3 6	6 0	V
$\overline{V_O}$	Voltage, $V_{A, B}$		$V_{IN} = 0.8V$		-3.6	-6 0	V
V_T	Differential output	$R_L = 100\Omega$	$V_{IN} = 2.0V$	2.0	2 4		V
$\overline{V_T}$	Voltage, $V_{A, B}$		$V_{IN} = 0.8V$	-2 0	-2 4		V
V_{OS} , $\overline{V_{OS}}$	Common mode offset voltage	$R_L = 100\Omega$			2.5	0.4	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in differential output voltage	$R_L = 100\Omega$			0.005	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in common mode offset voltage	$R_L = 100\Omega$			0.005	3 0	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$		4.0	4 8		V
V_{CMR}	Output voltage common mode range	$V_{\overline{ENABLE}} = 2.4V$		± 10			V
I_{XA}	Output leakage	$V_{CC} = 0V$	$V_{CMR} = 10V$			20	μA
I_{XB}	current		$V_{CMR} = -10V$			-20	μA
I_{OX}	Off state (high Z)	$V_{CC} = Max$	$V_{CMR} \leq 10V$			20	μA
	output current		$V_{CMR} > -10V$			-20	μA
I_{SA}, I_{SB}	Output short circuit	$V_{IN} = 2.4V$	$V_{OA} = 0V$		-80	-150	mA
	current		$V_{OB} = 6V$		80	150	mA
		$V_{IN} = 0.4V$	$V_{OA} = 6V$		80	150	mA
			$V_{OB} = 0V$		-80	-150	mA
I_{CC}	Supply current				18	30	mA
V_{IH}	High level input voltage			2 0			V
V_{IL}	Low level input voltage					0.8	V
I_{IH}	High level input current	$V_{IN} = 2.4V$			1 0	40	μA
		$V_{IN} \leq V_{CC}$			10	100	μA
I_{IL}	Low level input current	$V_{IN} = 0.4V$			-30	-200	μA
V_I	Input clamp voltage	$I_{IN} = -12mA$				-1 5	V

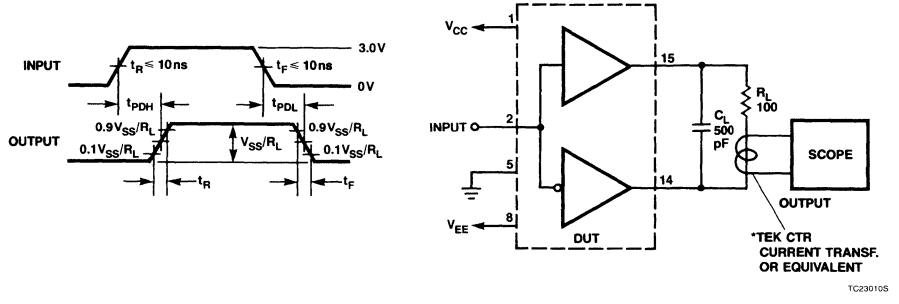
Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

AC ELECTRICAL CHARACTERISTICS EIA RS-422 Connection, V_{CC} = 5 0V, V_{EE} = GND, Mode = 0 4V, T_A = 25°C

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]	LIMITS			UNIT
			Min	Typ[1]	Max	
t_r	Rise time	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_f	Fall time	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_{PDH}	Output propagation delay	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_{PDL}	Output propagation delay	R_L = 100Ω, C_L = 500pF, Figure 1		120	200	ns
t_{PLZ}	Output enable to output	R_L = 450Ω, C_L = 500pF, Figure 2		180	300	ns
t_{PHZ}				250	350	ns
t_{PZL}	Output enable to output	R_L = 450Ω, C_L = 500pF, Figure 2		250	350	ns
t_{PZH}				180	300	ns

NOTES:
1 Typical limits are at V_{CC} = 5V, V_{EE} = GND, 25°C ambient and maximum loading
2 Symbols and definitions correspond to EIA RS-422 where applicable
3 RL connected between each output and its complement



NOTE:
*Current probe is the easiest way to display a differential waveform

Figure 1. Switching Time Waveforms and AC Test Circuits for EIA RS-422 Connection

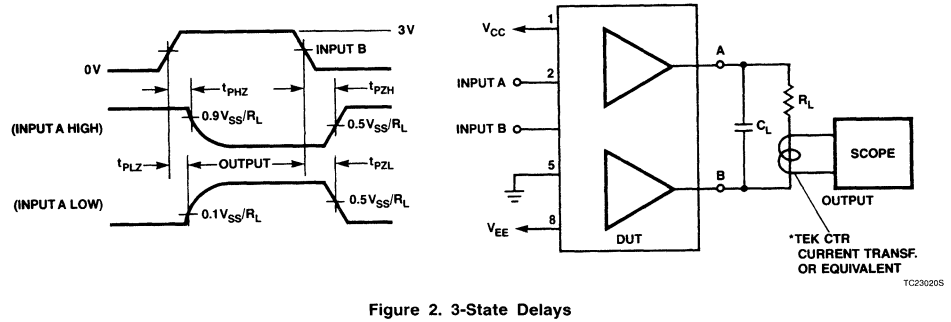


Figure 2. 3-State Delays

Dual Differential RS-422 Party Line/ Quad Single-Ended RS-423 Line Driver

AM26LS30

DC ELECTRICAL CHARACTERISTICS

over the operating temperature range. The following conditions apply unless otherwise specified: AM26LS30 $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = -5.0V \pm 10\%$, AM26LS30 $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5.0\%$, $V_{EE} = -5.0V \pm \%5$, **RS-423 Connection**, Mode Voltage $\geq 2.0V$.

SYMBOL[2]	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[1]	Max	
V_O	Output voltage	$R_L = \infty$ Note 3	$V_{IN} = 2.4V$	4.0	4.4	6.0	V
$\overline{V_O}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	-4.0	-4.4	-6.0	V
V_T	Output voltage	$R_L = 450\Omega$	$V_{IN} = 2.4V$	3.6	4.1		V
$\overline{V_T}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4\ 75V$	$V_{IN} = 0\ 4V$	-3.6	-4.1		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, $R_L = 450\Omega$			0.02	0.4	V
I_{X+}	Output leakage power off	$V_{CC} = V_{EE} = 0V$	$V_O = 6V$		2.0	20	μA
I_{X-}			$V_O = -6V$		-2.0	-20	μA
I_{S+}	Output short circuit current	$V_O = 0V$	$V_{IN} = 2.4V$		-80	-150	mA
I_{S-}			$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew control current	$V_{SLEW} = V_{EE} + 0.9V$			±140		μA
I_{CC}	Positive supply current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative supply current	$V_{IN} = 0\ 4V$, $R_L = \infty$			-10	-22	mA
V_{IH}	High level input voltage			2.0			V
V_{IL}	Low level input voltage					0.8	V
I_{IH}	High level input current		$V_{IN} = 2.4V$		1.0	40	μA
			$V_{IN} \leq V_{CC}$		10	100	μA
I_{IL}	Low level input current	$V_{IN} = 0\ 4V$			=nl30	-200	μA
V_I	Input clamp voltage	$I_{IN} = -12mA$				-1.5	V

AC ELECTRICAL CHARACTERISTICS

EIA RS-423 Connection, $V_{CC} = 5.0V$, $V_{EE} = -5V$, Mode = 2.4V, $T_A = 25°C$.

SYMBOL[2]	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[1]	Max	
t_r	Rise time	$R_L = 450\Omega$, $C_L = 500pF$	$C_C = 0pF$		120	300	ns
		Figure 3	$C_C = 50pF$		3.0		μs
t_f	Fall time	$R_L = 450\Omega$, $C_L = 500pF$	$C_C = 0pF$		120	300	ns
		Figure 3	$C_C = 50pF$		3 0		μs
S_{RC}	Slew rate coefficient	$R_L = 450\Omega$, $C_L = 500pF$, Figure 3			0.06		μs/pF
t_{PDH}	Output propagation delay	$R_L = 450\Omega$, $C_L = 500pF$, Figure 3 $C_C = 0pF$			180	300	ns
t_{PDL}	Output propagation delay	$R_L = 450\Omega$, $C_L = 500pF$, Figure 3 $C_C = 0pF$			180	300	ns

NOTES:
1 Typical limits are at $V_{CC} = 5\ 0V$, $V_{EE} = -5V$, 25°C ambient and maximum loading
2 Symbols and definitions correspond to EIA RS-423 where applicable
3 Output voltage is +3 9V minimum and −3 9V minimum at −55°C

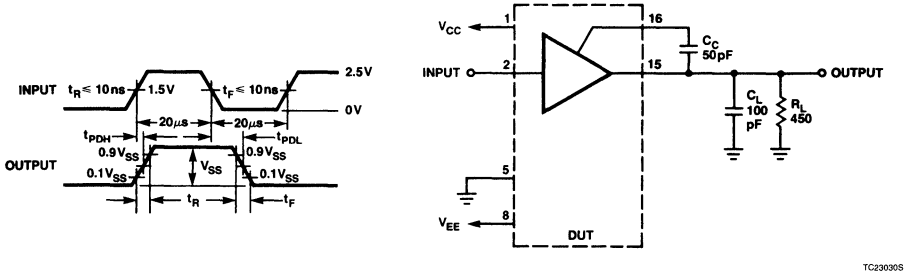


Figure 3. Switching Time Waveforms and AC Test Circuits for EIA RS-423 Connection

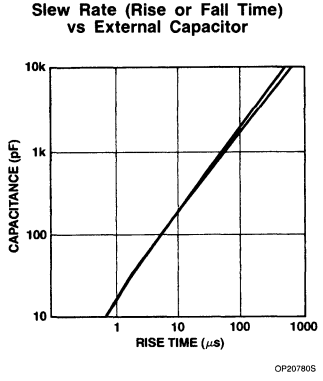


Figure 4

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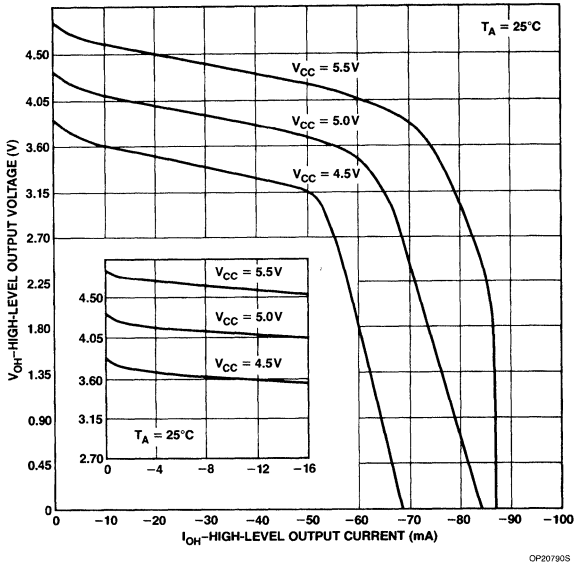


Figure 5

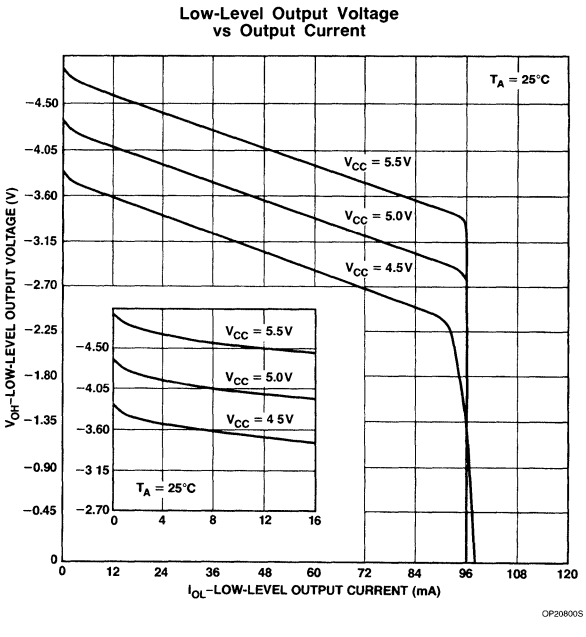


Figure 6

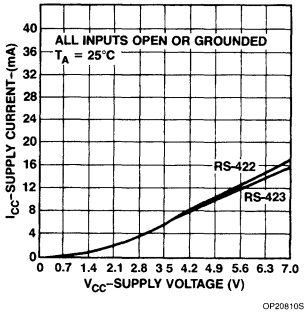

Supply Current
vs Supply Voltage
ALL INPUTS OPEN OR GROUNDED
T_A = 25°C
I_{CC}–SUPPLY CURRENT–(mA)
40
36
32
28
24
20
16
12
8
4
0
RS-422
RS-423
0 0.7 1.4 2.1 2.8 3 5 4.2 4.9 5.6 6.3 7.0
V_{CC}–SUPPLY VOLTAGE (V)
OP20810S

Figure 7

5

Signetics

AM26LS31
Quad High-Speed Differential Line Driver

Product Specification

Linear Products

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-state outputs and logical ORed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

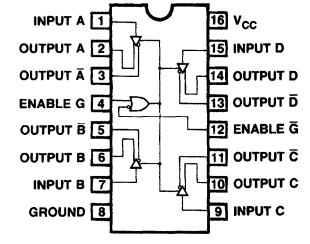
- **Output skew of 2.0ns typical**
- **Input to output delay: 12ns**
- **Operation from single +5V**
- **16-pin DIP and SO packages**
- **Four line drivers in one package**
- **Output short-circuit protection**
- **Complementary outputs**
- **Meets EIA standard RS-422**
- **High output drive capability for 100Ω terminated transmission lines**
- **Available in military and commercial temperature range**
- **Advanced low power Schottky processing**
- **Outputs won't load line when V_{CC} = 0V**

APPLICATIONS

- **Data communications equipment**
- **Computer peripherals**
- **Workstations**
- **Automatic test equipment**

PIN CONFIGURATION

D, F, and N Packages



TOP VIEW

CD14751S

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	AM26LS31CN
16-Pin SO	0 to +70°C	AM26LS31CD
16-Pin Plastic DIP	−40°C to +85°C	AM26LS31IN
16-Pin SO	−40°C to +85°C	AM26LS31ID
16-Pin Cerdip	−55°C to +125°C	AM26LS31MF
16-Pin Plastic DIP	−55°C to +125°C	AM26LS31MN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7	V
V_{IN}	Input voltage	7	V
	Output off-state voltage	5 5	V
T_A	Operating temperature range		
	AM26LS31MF	−55 to +125	°C
	AM26LS31MN	−55 to +125	°C
	AM26LS31IN	−40 to +85	°C
	AM26LS31ID	−40 to +85	°C
	AM26LS31CN	0 to +70	°C
	AM26LS31CD	0 to +70	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 10sec max.)	300	°C

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
F	1250mW	10mW/°C	25°C
N	1488mW	11.9mW/°C	25°C
D	1126mW	9mW/°C	25°C

5

DC AND AC ELECTRICAL CHARACTERISTICS

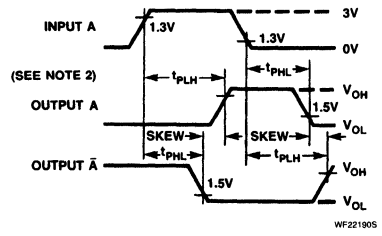
V_{CC} = 5V± 10%, T_A = −55 to +125°C for AM26LS31MF and AM26LS31MN;
V_{CC} = 5V± 5%, T_A = −40 to +85°C for AM26LS31IN and AM26LS31ID;
V_{CC} = 5V± 5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD,
unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = −20mA	2 5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0 5	V
V_{IH}	Input High voltage	V_{CC} = Min	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		−0.26	−0 36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0 001	20	μA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0 001	0 1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max , V_O = 5 5V V_O = 0.5V		0 6 −0 050	20 −20	μA μA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	−30		−150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A=25°C, load[2]		12	40	ns

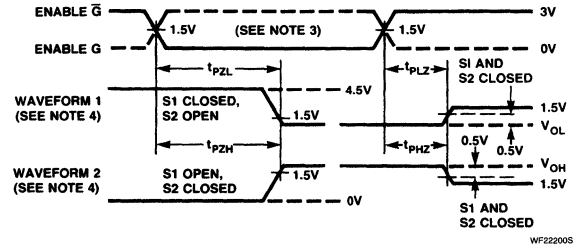
NOTES:
1. All typical values are T_A = +25°C, V_{CC} = 5 0V
2. C_L = 30pF, V_{IN} = 1 3V to V_{OUT} = 1 3V, V_{PULSE} = 0V to 3 0V

TIMING DIAGRAMS

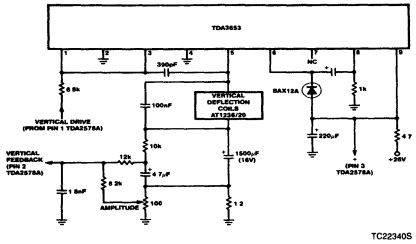
PARAMETER MEASUREMENT INFORMATION



Propagation Delay Times and Skew



Enable and Disable Times



Test Circuit

NOTES:

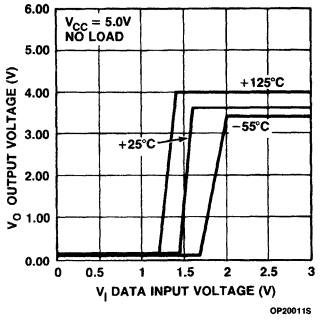
1. All pauses are supplied by generators having the following characteristics PRR ⩽ 1MHz, Z_{OUT} = 50Ω, 1R ⩽ 15ns, 1F ⩽ 6ns
2. When measuring propagation delay times and skew, switches S1 and S2 are open.
3. Each enable is tested separately.
4. Waveform 1 is for an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. C_L includes probe and jig capacitance

5

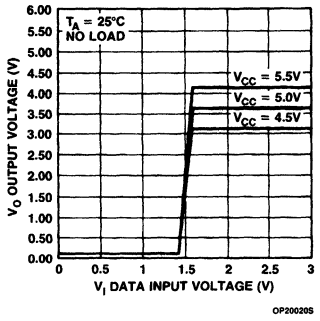
Quad High-Speed Differential Line Driver | AM26LS31

TYPICAL PERFORMANCE CHARACTERISTICS

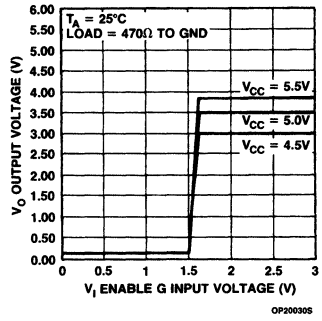
Output Voltage vs Data Input Voltage



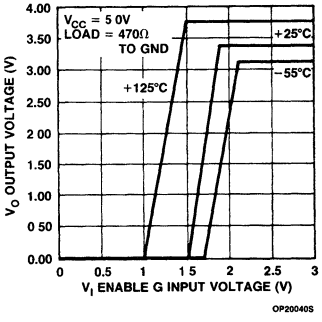
Output Voltage vs Data Input Voltage



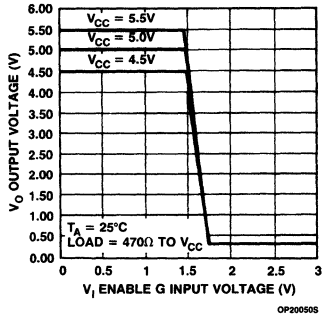
Output Voltage vs Enable G Input Voltage



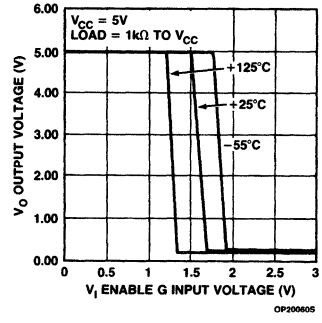
Output Voltage vs Enable G Input Voltage



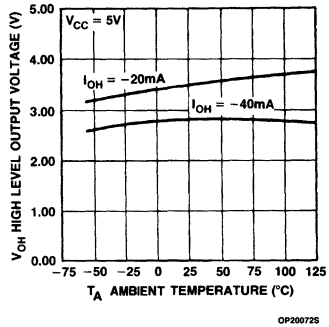
Output Voltage vs Enable G Input Voltage



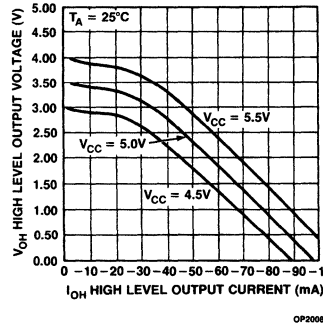
Output Voltage vs Enable G Input Voltage



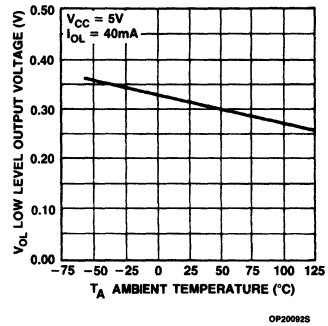
High Level Output Voltage vs Ambient Temperature



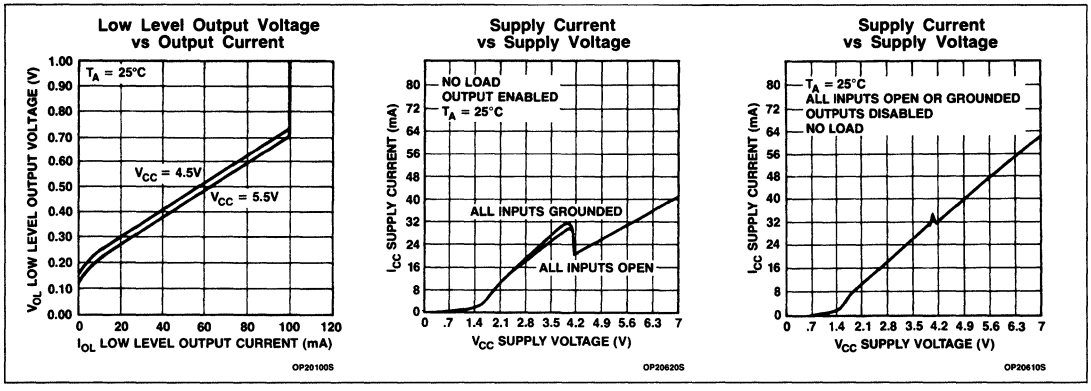
High Level Output Voltage vs Output Current



Low Level Output Voltage vs Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



5

Signetics

AM26LS32/33
Quad High Speed Differential Line Receivers

Objective Specification

Linear Products

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers with the AM26LS32 designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

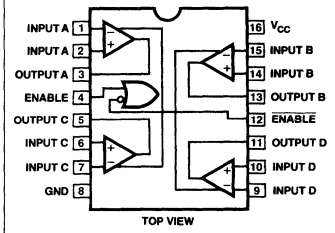
The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

FEATURES

- **Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32**
- **±0.2V sensitivity over the input voltage range on AM26LS32**
- **±0.5V sensitivity on AM26LS33**
- **6k minimum input impedance**
- **60mV input hysteresis**
- **The AM26LS32 meets all the requirements of RS-422 and RS-423**
- **Operation from single +5V supply**
- **Fail safe input-output relationship. Output always high when inputs are open**
- **3-State drive, with choice of complementary output enables, for receiving directly onto a data bus**
- **3-State outputs disabled during power up and power down**

PIN CONFIGURATION

F, D and N Packages



TOP VIEW

CD15350S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	AM26LS32CN
16-Pin SO	0 to +70°C	AM26LS32CD
16-Pin Plastic DIP	-40°C to +85°C	AM26LS32IN
16-Pin SO	-40°C to +85°C	AM26LS32ID
16-Pin Cerdip	-55°C to +125°C	AM26LS32MF
16-Pin Plastic DIP	-55°C to +125°C	AM26LS32MN
16-Pin Plastic DIP	0 to +70°C	AM26LS33CN
16-Pin SO	0 to +70°C	AM26LS33CD
16-Pin Plastic DIP	-40°C to +85°C	AM26LS33IN
16-Pin SO	-40°C to +85°C	AM26LS33ID
16-Pin Cerdip	-55°C to +125°C	AM26LS33MF
16-Pin Plastic DIP	-55°C to +125°C	AM26LS33MN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	−65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
F	1,524mW	12.19mW/°C	25°C
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V± 10% for AM26LS32/33MX, V_{CC} = 5.0V± 5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	Typ[1]	Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, $-7V \leq V_{CM} \leq +7V$		0.2	0.06	0.2	V
		AM26LS33, $-15V \leq V_{CM} \leq +15V$		0.5	0.06	0.5	V
R_{IN}	Input resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-10V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+10V \leq V_{IN} \leq -15V$				−2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = min., $I_{OH} = -440\mu A$, $\Delta V_{IN} = +1.0V$, $V_{\overline{ENABLE}} = 0.8V$	Com'l	2.7	3.4		V
			Mil	2.5	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = min., $V_{\overline{ENABLE}} = 0.8V$, $\Delta V_{IN} = +1.0V$	I_{OL} = 4.0mA		0.3	0.4	V
			I_{OL} = 8.0mA			0.45	V
V_{IL}	Enable LOW voltage					0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = min., $I_{IN} = -18mA$				−1.5	V
I_O	Off state (high impedance) output current	V_{CC} = max.	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 5.0V± 10% for AM26LS32/33MX, V_{CC} = 5.0V± 5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

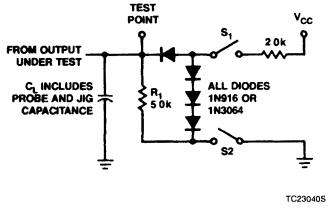
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	LIMITS AM26LS32/33 Typ[1]	LIMITS AM26LS32/33 Max	UNIT
I_{IL}	Enable LOW current	V_{IN} = 0.4V			-0.2	-0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	μA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	μA
I_{SC}	Output short circuit current	V_{CC} = max. ΔV_{IN} = +1V, V_{OUT} = 0V		-15	-60	-85	mA
I_{CC}	Power supply current	V_{CC} = max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		60		mV
			AM26LS33		120		mV
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pf (see test condition)			TBD	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pf (see test condition)			TBD	25	ns
t_{LZ}	Enable to output	T_A = 25 = C, V_{CC} = 5.0V C_L = 5pF (see test condition)			TBD	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			TBD	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			TBD	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			TBD	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V

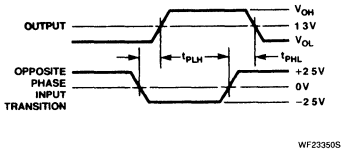
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	ENABLES $\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$VTL \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
X	L	H	Z

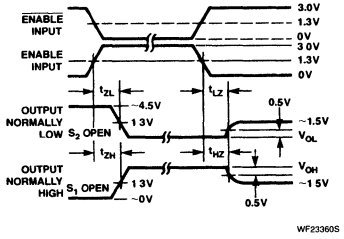
NOTES:
H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate
E = enable, $\overline{E}$ = $\overline{\text{enable}}$



Load Test Circuit for 3-State Outputs



Propagation Delay[1, 4]



Enable and Disable Times[2, 3, 4]

NOTES:
1 Diagram shown for $\overline{\text{Enable}}$ Low
2 Enable is tested with $\overline{\text{Enable}}$ High, $\overline{\text{Enable}}$ is tested with Enable Low
3 S_1 and S_2 of Load Circuit are closed except where shown
4 Pulse Generator for All Pulses Rate ≤ 1.0MHz, $Z_O = 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6.0$ns

5

Signetics

MC1488
Quad Line Driver

Product Specification

Linear Products

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

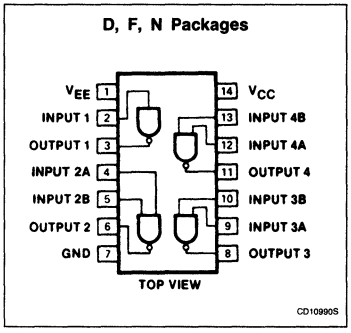
FEATURES

- **Current limited output: ± 10mA Typ**
- **Power-off source impedance: 300Ω min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

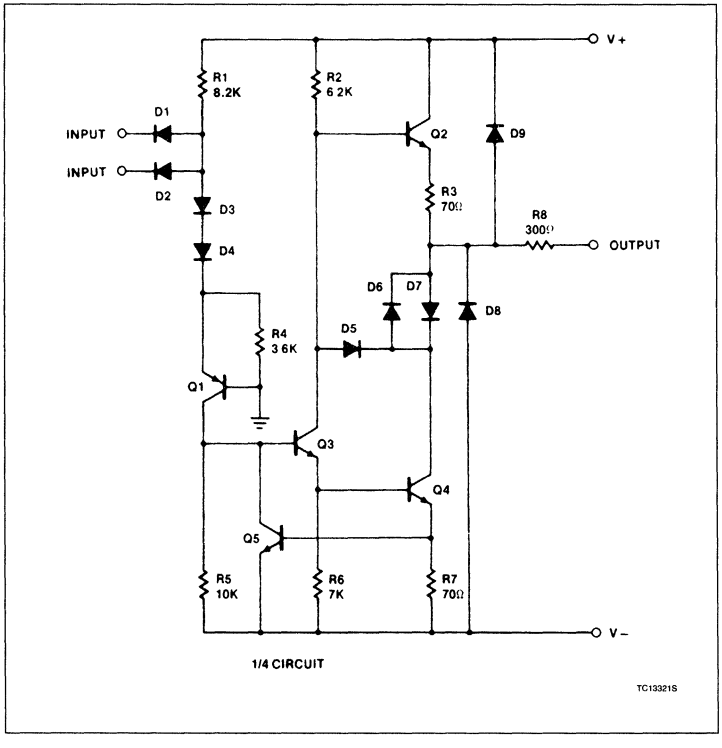
APPLICATIONS

- **Computer port driver**
- **Digital transmission over long lines**
- **Slew rate control**
- **TTL/DTL to MOS translation**

PIN CONFIGURATION



CIRCUIT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +75°C	MC1488D
14-Pin Plastic DIP	0 to +75°C	MC1488N
14-Pin Ceramic DIP	0 to +75°C	MC1488F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	+15	V
	V–	–15	V
V_{IN}	Input voltage	$-15 \leqslant V_{IN} \leqslant 7.0$	V
V_{OUT}	Output voltage	±15	V
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating ambient temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:
1 Derate above 25°C, at the following rates
F package at 9.5mW/°C
N package at 11.4mW/°C.
D package at 8.3mW/°C

5

DC AND AC ELECTRICAL CHARACTERISTICS

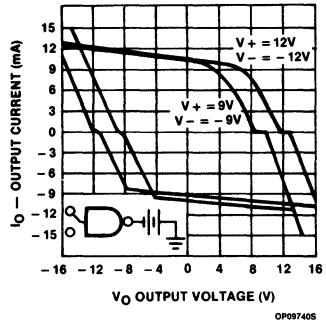
$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$, unless otherwise specifed. All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$[1].

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
I_{IH} I_{IL}	Logic "0" input current Logic "1" input current	$V_{IN} = 0V$ $V_{IN} = +5.0V$			−1.0 0.005	−1.6 10.0	mA μA
V_{OH}	High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	V+ = 9.0V V− = −9.0V	6.0	7.0		V
			V+ = 13.2V V− = −13.2V	9.0	10.5		V
V_{OL}	Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	V+ = 9.0V V− = −9.0V	−6.0	−6.8		V
			V+ = 13.2V V− = −13.2V	−9.0	−10.5		V
I_{SC+}	High level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{SC-}	Low level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
R_{OUT}	Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
I+	Positive supply current (output open)	$V_{IN} = 1.9V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		15.0 19.0 25.0	20.0 25.0 34.0	mA mA mA
		$V_{IN} = 0.8V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		4.5 5.5 8.0	6.0 7.0 12.0	mA mA mA
I−	Negative supply current (output open)	$V_{IN} = 1.9V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		−13.0 −18.0 −25.0	−17.0 −23.0 −34.0	mA mA mA
		$V_{IN} = 0.8V$	V+ = 9.0V, V− = −9.0V V+ = 12V, V− = −12V V+ = 15V, V− = −15V		−1 −1 −0.01	−15 −15 −2.5	μA μA mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[2] F package N package D package					 1190 1420 1040	 mW mW mW
t_{PD1}	Propagation delay to "1"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
t_{PD0}	Propagation delay to "0"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
t_R	Rise time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
t_F	Fall time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

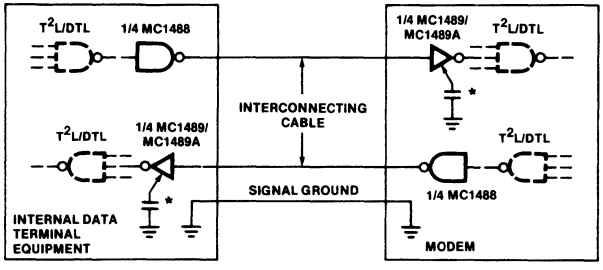
NOTES:

1. Voltage values shown are with respect to network ground terminal Positive current is defined as current into the referenced pin.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11 4mW/°C.
   D package at 8.3mW/°C.

TYPICAL PERFORMANCE CHARACTERISTICS



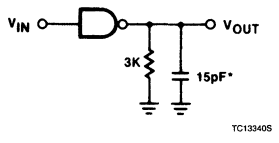
Output Voltage and Current-Limiting Characteristics



NOTE:
*Optional for noise filtering

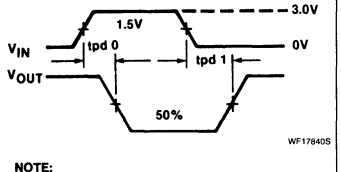
RS-232C Data Transmission

AC LOAD CIRCUIT



NOTE:
*C_L includes probe and jig capacitance

SWITCHING WAVEFORMS



NOTE:
t_R and t_F are measured between 10% and 90% of the output waveform

APPLICATIONS

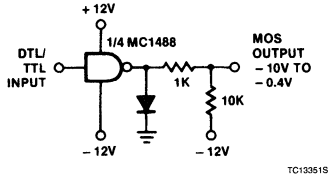
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current-limiting characteristics of the MC1488 For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

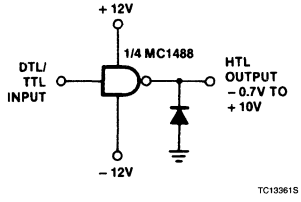
where C is the required capacitor, I_{SC} is the short-circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V/μs. Using the worst-case output short-circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

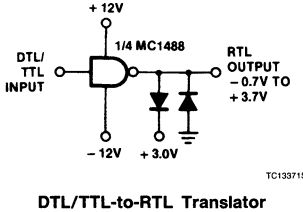
TYPICAL APPLICATIONS



DTL/TTL-to-MOS Translator



DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

5

Signetics

MC1489/MC1489A
Quad Line Receivers

Product Specification

Linear Products

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS-232C.

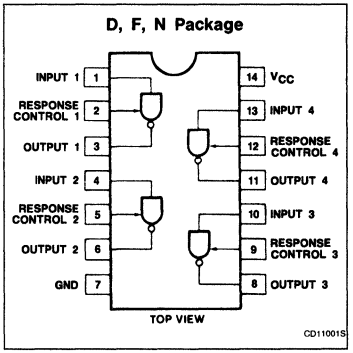
FEATURES

- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

APPLICATIONS

- **Computer port inputs**
- **Modems**
- **Eliminating noise in digital circuitry**
- **MOS-to-TTL/DTL translation**

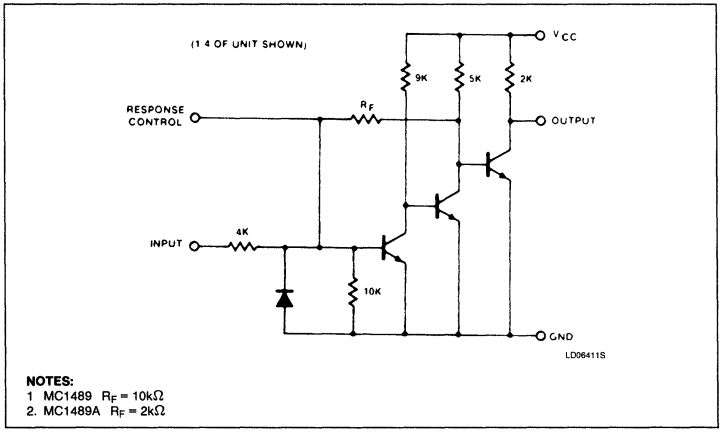
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	MC1489N
14-Pin Plastic DIP	0 to +70°C	MC1489AN
14-Pin Cerdip	0 to +70°C	MC1489F
14-Pin Cerdip	0 to +70°C	MC1489AF
14-Pin Plastic SO	0 to +70°C	MC1489D
14-Pin Plastic SO	0 to +70°C	MC1489AD

EQUIVALENT SCHEMATIC



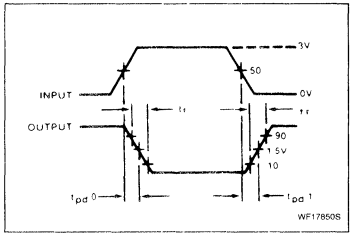
NOTES:
1. MC1489 $R_F = 10k\Omega$
2. MC1489A $R_F = 2k\Omega$

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	10	V
V_{IN}	Input voltage range	±30	V
I_{OUT}	Output load current	20	mA
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1 Derate above 25°C, at the following rates
F package at 9 5mW/°C
N package at 11 4mW/°C
D package at 8 3mW/°C

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5 0V ±1%, 0°C ≤ T_A ≤ +75°C, unless otherwise specified [1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0 45V, I_{OUT} = 10mA	1 0		1 5	1 75		2.25	V
V_{IL}	Input low threshold voltage	T_A = 25°C, V_{OUT} ≥ 2.5V, I_{OUT} = −0 5mA	0 75		1 25	0 75		1 25	V
I_{IN}	Input current	V_{IN} = +25V	+3 6	+5 6	+8 3	+3 6	+5 6	+8.3	mA
		V_{IN} = −25V	−3 6	−5 6	−8 3	-3 6	−5 6	−8 3	
		V_{IN} = +3V	+0 43	+0 53		+0 43	+0 53		
		V_{IN} = −3V	−0 43	−0.53		−0 43	−0.53		
V_{OH}	Output high voltage	V_{IN} = 0 75V, I_{OUT} = −0.5mA	2 6	3 8	5 0	2 6	3.8	5 0	V
		Input = Open, I_{OUT} = −0 5mA	2 6	3 8	5 0	2 6	3 8	5 0	V
V_{OL}	Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0 33	0 45		0 33	0.45	V
I_{SC}	Output short-circuit current	V_{IN} = 0.75V		3 0			3 0		mA
I_{CC}	Supply current	V_{IN} = 5 0V		20	26		20	26	mA
P_D	Power dissipation	V_{IN} = 5 0V		100	130		100	130	mW

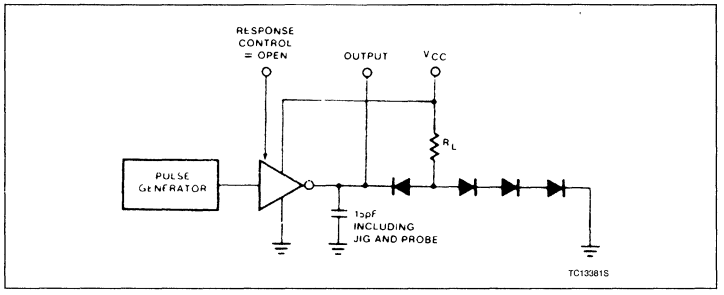
NOTES:
1. Voltage values shown are with respect to network ground terminal Positive current is defined as current into the referenced pin
2 These specifications apply for response control pin = open

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5 0V ±1%, T_A = 25°C, unless otherwise specified [1, 2]

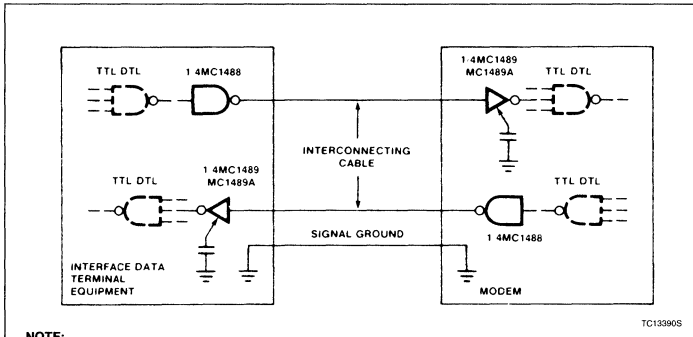
SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PD1}	Input to output "high" Propagation delay	R_L = 3 9kΩ (AC test circuit)		25	85		25	85	ns
t_{PD0}	Input to output "low" Propagation delay	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
t_R	Output rise time	R_L = 3 9kΩ (AC test circuit)		110	175		110	175	ns
t_F	Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES:
1 Voltage values shown are with respect to network ground terminal Positive current is defined as current into the referenced pin
2 These specifications apply for response control pin = open

AC TEST CIRCUIT

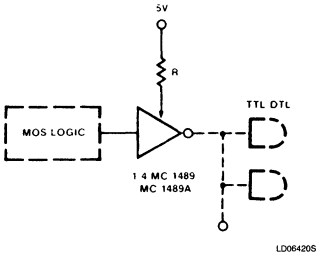


TYPICAL APPLICATIONS



NOTE:
*Optional for noise filtering

RS-232C Data Transmission



MOS-to-TTL/DTL Translator

Signetics

AN113
Using the MC1488/1489 Line Drivers and Receivers

Application Note

Linear Products

LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria For instance, the device may be extremely wide-band or be intended for use in party line systems. Some include built-in hysteresis in the receiver while others do not

The EIA Standard

The Electronic Industries Association (EIA) has produced a number of specifications dealing with the transmission of data between data terminal and communications equipment One of these is EIA Standard RS-232C, which delineates much information about signal levels and hardware configurations in data systems

MC1488/1489

As line driver and receiver, the MC1488 and MC1489 meet or exceed the RS-232C specification

Standard RS-232C defines, the voltage level as being from 5 to 15V with positive voltage representing a logic 0. The MC1488 meets these requirements when loaded with resistors from 3k to 7kΩ

Output slew rates are limited by RS-232C to 30V/μs. To accomplish this specification, the MC1488 is loaded at its output by capacitance as shown by the typical hook-up diagram of Figure 1. A graph of slew rate vs output capacitance is given in Figure 2. For the standard 30V/μs, a capacitance of 400pF is selected.

The short-circuit current charges the capacitance with the relationship

$$C = \frac{I_{SC}\Delta T}{\Delta V}$$

Where C is the required capacitor, I_{SC} is the short-circuit current value, and $\Delta V/\Delta T$ is the slew rate.

Using the worst-case output short-circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output to limit the output slew rate to 30V/μs in accordance with the EIA standard.

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver Thus, the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst-case voltage levels. In addition to output protection, the MC1488 includes a 300Ω, resistor to ensure that the output impedance of the driver will be at least 300Ω, even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300Ω resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. To prevent this, series diodes should be included in both supply lines as pictured in Figure 3.

The companion receiver, MC1489, is also designed to meet RS-232C specifications for receivers It must detect a voltage from ± 3 to ± 25V as logic signals but cannot generate an input differential voltage of greater than 2V should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 4 shows the shift in high and low trip points as a function of the programming resistance.

APPLICATIONS

The design of the MC1488 and MC1489 makes them very versatile with many possible applications The MC1488 output current limiting enables the user to define the output voltage levels independent of supply voltages. Figure 5 shows the MC1488 as a TTL-to-MOS Translator, while Figures 6 and 7 illustrate TTL-to-HTL and TTL-to-MOS Translators

The MC1489 response control node allows the user to modify the input threshold voltage levels. This is accomplished by adding a resistor between the response control pin and an external power supply. Figure 4 shows the shift thus provided. This feature and the fact that the inputs are designed to withstand ± 30V permit the use of the MC1489 for level translation as shown in the MOS-to-TTL Translator of Figure 8. This feature is also useful for level shifting, as illustrated in Figure 9

The response control node can also be used to filter out high frequency, high energy noise pulses. Figures 10 and 11 give typical noise pulse rejection curves for various sized external capacitors.

5

Using the MC1488/1489 Line Drivers and Receivers AN113

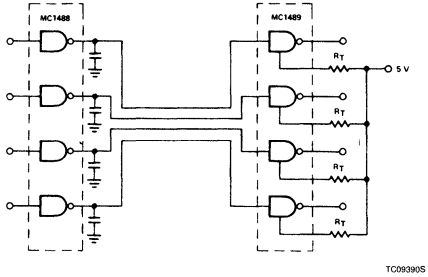


Figure 1. Typical Line Driver-Receiver Application

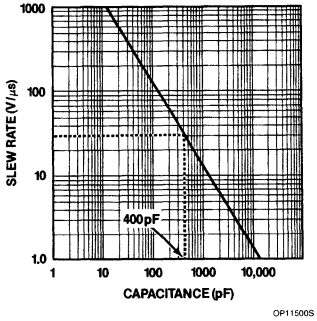


Figure 2. Output Slew Rate vs Load Capacitance

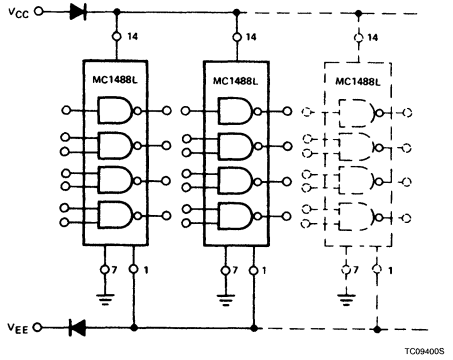
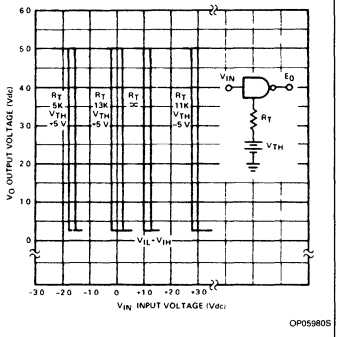
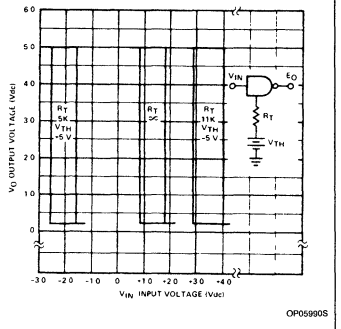


Figure 3. Protection From Power Supply Malfunction



a. MC1489



b. MC1489A

Figure 4. Hysteresis as a Function of Programming Resistance

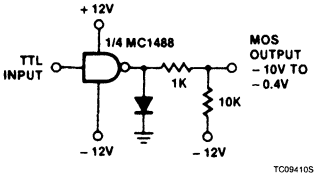


Figure 5. TTL-to-MOS Translator

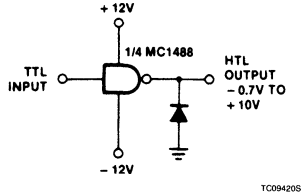


Figure 6. TTL-to-HTL Translator

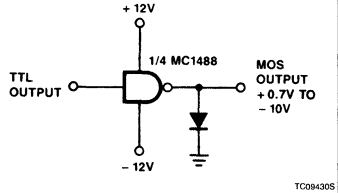


Figure 7. TTL-to-MOS Translator

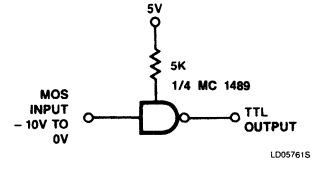


Figure 8. MOS-to-TTL Translator

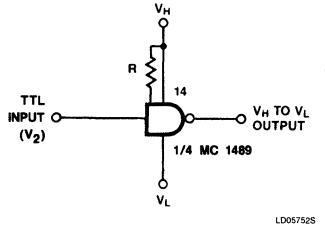


Figure 9. Level Shifter[1]

NOTE:
1 $V_2 \leq 5V$, $3V \leq V_H - V_L \leq 10V$

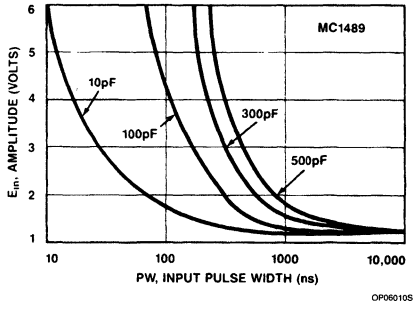


Figure 10. Turn-on Threshold vs Capacitance From Response Control Pin to GND

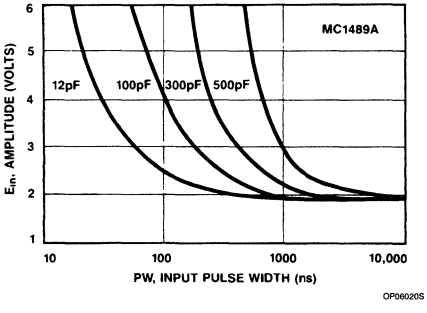


Figure 11. Turn-on Threshold vs Capacitance From Response Control Pin to GND

5

Signetics

NE5170
Octal Line Driver

Preliminary Specification

Linear Products

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features: (1) output slew rate, (2) output voltage level, and (3) 3-State control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES

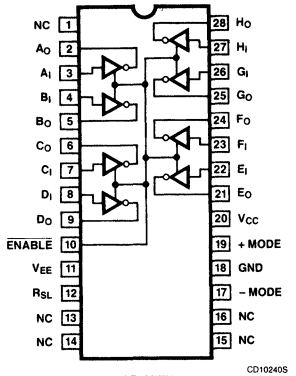
- **Meets EIA RS-232C/423A and CCITT V.10/X.26**
- **Simple slew rate programming with a single external resistor**
- **0.1 to 10V/μs slew rate range**
- **High/Low programmable voltage output modes**
- **TTL compatible inputs**

APPLICATIONS

- **High-speed modems**
- **High-speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

PIN CONFIGURATIONS

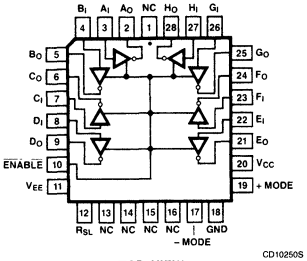
N Package



TOP VIEW

CD10240S

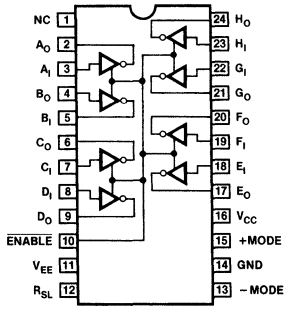
A Package



TOP VIEW

CD10250S

D Package



TOP VIEW

CD12300S

FUNCTION TABLE

$\overline{\text{ENABLE}}$	LOGIC INPUT	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	$\geqslant$9V
L	H	−5 to −6V	−5 to −6V	$\leqslant$−9V
H	X	Hi-Z	Hi-Z	Hi-Z

NOTES:
1 V_{CC} = +10V and V_{EE} = −10V, R_L = 3kΩ
2 V_{CC} = +12V and V_{EE} = −12V, R_L = 3kΩ

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5170N
28-Pin PLCC	0 to +70°C	NE5170A
24-Pin SO package	0 to +70°C	NE5170D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and - MODE	-15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{ENABLE}$, Data)	-1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = -10V ±10%, ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output High voltage	V_{IN} = 0.8V, R_L = 3kΩ[4]	5	6	V
		R_L = 450Ω[4]	4.5	6	
		R_L = 3kΩ[5], C_L = 2500pF	V_{CC} - 3		
V_{OL}	Output Low voltage	V_{IN} = 2 0V, R_L = 3kΩ[4]	-6	-5	V
		R_L = 450Ω[4]	-6	-4.5	
		R_L = 3kΩ[5], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = |V_{EE}|, R_L = 450Ω[4]		0.4	V
I_{CEX}	Output leakage current	|V_O| = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	-100	100	μA
V_{IH}	Input High voltage		2 0		V
V_{IL}	Input Low voltage			0 8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	-400	0	μA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	μA
I_{OS}	Output short circuit current[1]	V_O = 0V	-150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = -15mA	-1.5		V
I_{CC}	Supply current	No Load		35	mA
I_{EE}		No Load	-45		mA

NOTES:
1 Maximum current per driver Do not exceed maximum power dissipation if more than one output is on
2 High-impedance mode
3 Minimum value of the resistor used to set the slew rate
4 V_{OH}, V_{OL} at R_L = 450Ω will be ≥ ≥90% of V_{OH}, V_{OL} at R_L = ∞.
5 High Output Mode; +MODE pin = V_{CC}, -MODE pin = V_{EE}, 9V ≤ V_{CC} ≤ 13V, -9V ≥ V_{EE} ≥ -13V

5

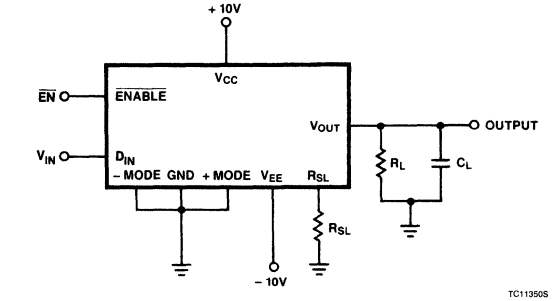
Octal Line Driver | NE5170

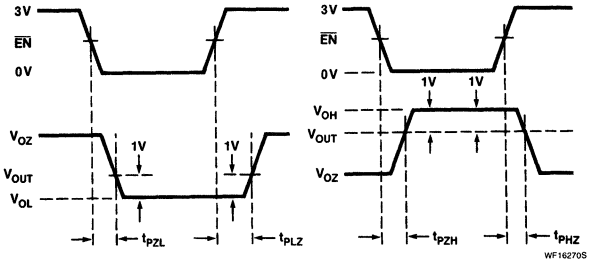
AC ELECTRICAL CHARACTERISTICS $V_{CC} = +10V$; $V_{EE} = -10V$; Mode = GND, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHZ}	Propagation delay output high to high-impedance	$R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		5	μs
t_{PLZ}	Propagation delay output low to high-impedance	$R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		5	μs
t_{PZH}	Propagation delay high-impedance to high output	$R_{SL} = 200k$ $R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		150	μs
t_{PZL}	Propagation delay high-impedance to low output	$R_{SL} = 200k$ $R_L = 450$, $C_L = 50pF$ or $R_L = 3k$, $C_L = 2500pF$		150	μs
SR	Output slew rate[1]	$R_{SL} = 2k$	8	12	V/μs
		$R_{SL} = 20k$	0.8	1.2	
		$R_{SL} = 200k$	0 06	0.14	

NOTE:
SR: Load condition. (A) For $R_{SL} < 4k\Omega$ use $R_L = 450\Omega$; $C_L = 50pF$; (B) for $R_{SL} > 4k\Omega$ use either $R_L = 450\Omega$, $C_L = 50pF$ or $R_L = 3k\Omega$, $C_L = 2500pF$.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS





NOTES:
1 See AC electrical characteristics table for values of R_{SL}, R_L and C_L
2 V_{IN} pulse Frequency = 1kHz, duty cycle = 50%, $Z_{OUT} = 50\Omega$, $t_r = t_f \leq 10ns$

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula.

$$R_{SL}\ (\text{in } k\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS-423A. Approximations for cable length and data rate are given by:

Max data rate (in kb/s) = 300/t

Cable length (in feet) = 100 × t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS-423A and RS-232C. The high output mode meets the specifications of RS-232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the −MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

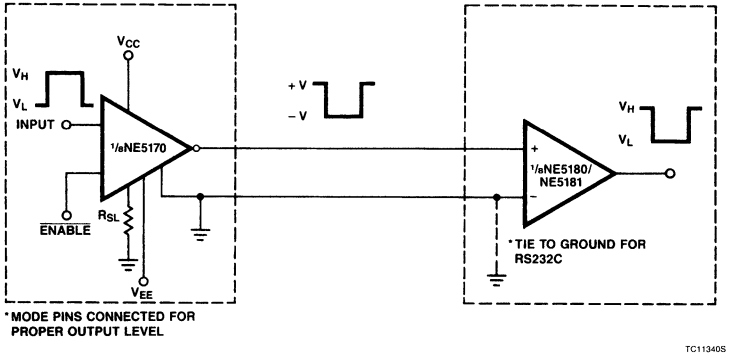


Figure 1. RS-232C/RS-423A Data Transmission

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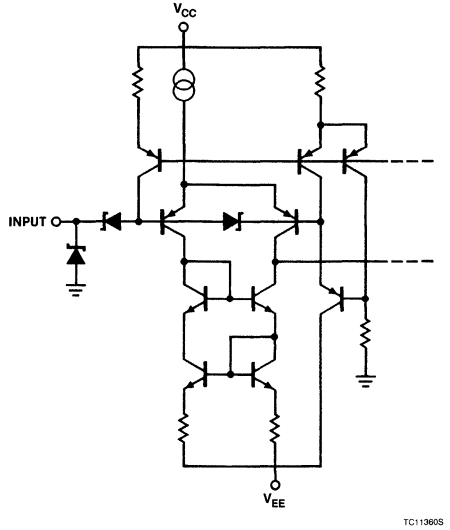


Figure 2. Input Stage Schematic

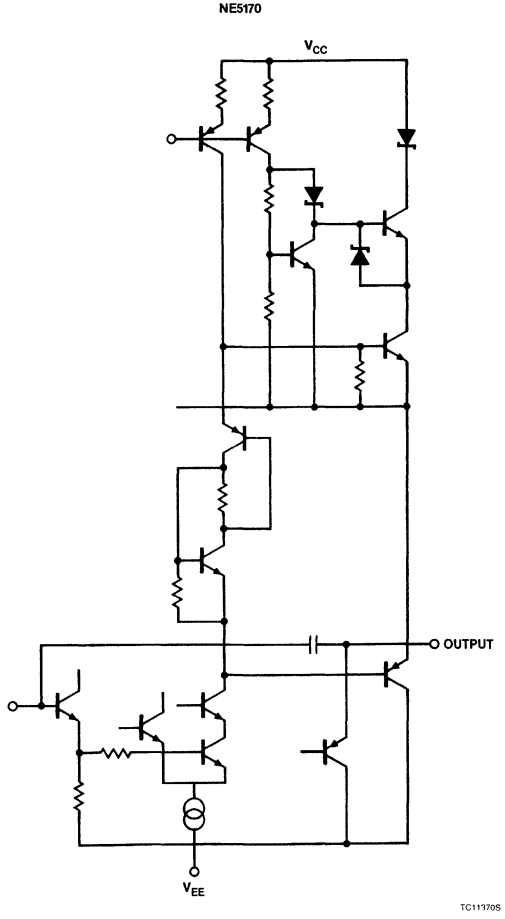


Figure 3. Output Stage Schematic

Octal Line Driver | NE5170

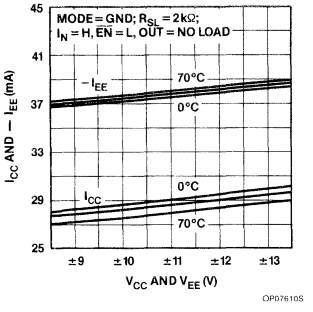


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

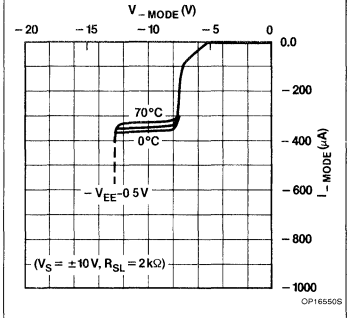


Figure 7. Typical −MODE Current vs −MODE Voltage

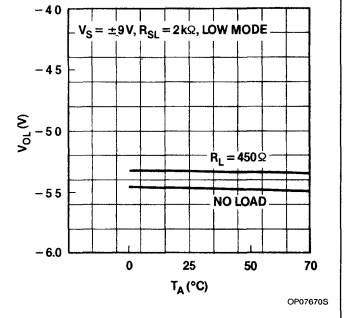


Figure 10. Typical Output Low Voltage vs Temperature

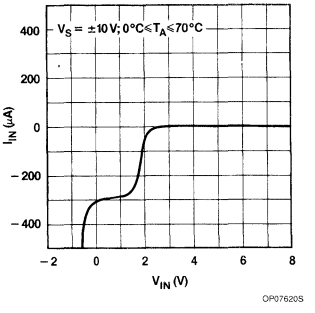


Figure 5. Typical Input Current vs Input Voltage

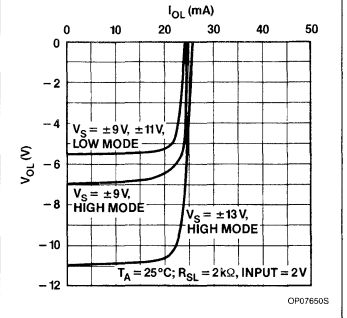


Figure 8. Typical Output Low Voltage vs Load Current

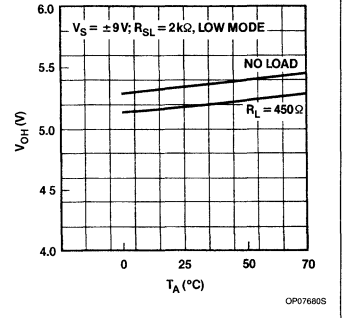


Figure 11. Typical Output High Voltage vs Temperature

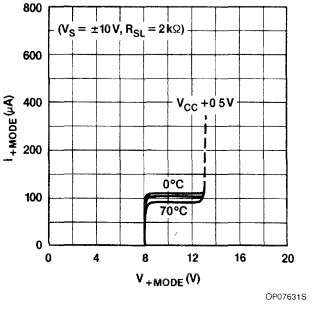


Figure 6. Typical +MODE Current vs +MODE Voltage

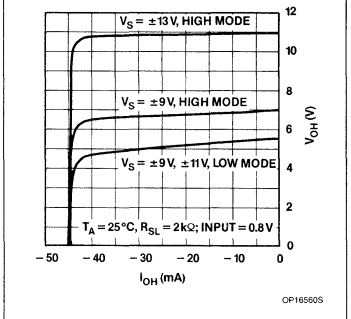


Figure 9. Typical Output High Voltage vs Load Current

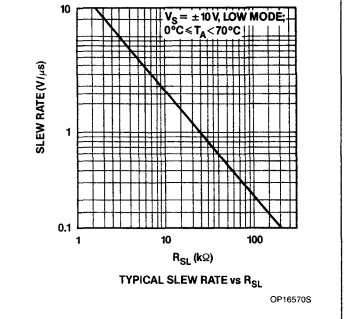


Figure 12. Typical Slew Rate vs R_{SL}

NE5180/NE5181
Octal Differential Line Receivers

Preliminary Specification

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

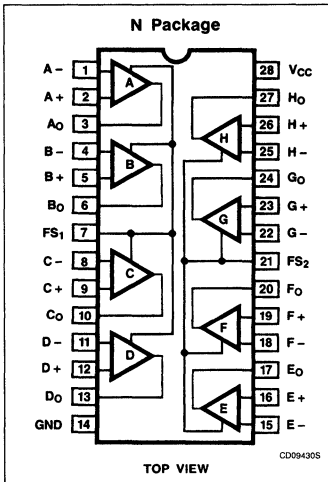
- **Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28**
- **Single +5V supply — TTL compatible outputs**
- **Differential inputs withstand ±25V**
- **Failsafe feature**
- **Input noise filter (NE5180 only)**
- **Internal hysteresis**
- **Available in SMD PLCC**

APPLICATIONS

- **High-speed modems**
- **High-speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

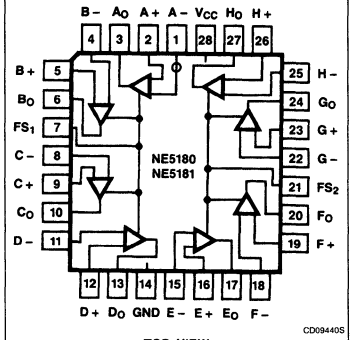
PIN CONFIGURATIONS

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200mV^1$	X	H
$V_{ID} < -200mV^1$	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1 V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5180N
28-Pin Plastic DIP	0 to +70°C	NE5181N
28-Pin PLCC	0 to +70°C	NE5180A
28-Pin PLCC	0 to +70°C	NE5181A

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ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$

SYMBOL	PARAMETER	RATING	UNIT
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common-mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Output sink current	50	mA
V_{FS}	Failsafe voltage	−0.3 to V_{CC}	V
I_{OS}	Output short-circuit time	1	sec

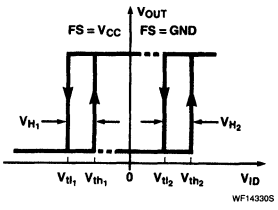


Figure 1. V_{tl}, V_{th}, V_H Definitions

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $0°C \leq T_A \leq +70°C$, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNIT
				Min	Max	Min	Max	
R_{IN}	DC input resistance	$3V \leq \lvert V_{IN} \rvert \leq 25V$		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	$0 \leq I_{OUT} \leq 8mA$, $V_{failsafe} = 0V$		0.45		0.45	V
			$0 \geq I_{OUT} \geq -400\mu A$, $V_{failsafe} = V_{CC}$	2.7		2.7		
V_{TH}	Differential input high[4] threshold	$V_{OUT} \geq 2.7V$, $I_{OUT} = -440\mu A$	$R_S = 0$[1]		0.2		0.2	V
			$R_S = 500$[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	$V_{OUT} \leq 0.45V$, $I_{OUT} = 8mA$	$R_S = 0$[1]	−0.2		−0.2		V
			$R_S = 500$[1]	−0.4		−0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	$V_{ID} = 1V$, $I_{OUT} = -440\mu A$		2.7		2.7		V
V_{OL}	Low level output voltage	$V_{ID} = -1V$	$I_{OUT} = 4mA$[2]		0.4		0.4	V
			$I_{OUT} = 8mA$[2]		0.45		0.45	
I_{OS}	Short-circuit output current	$V_{ID} = 1V$, Note 3		20	100	20	100	mA
I_{CC}	Supply current	$4.75V \leq V_{CC} \leq 5.25V$, $V_{ID} = -1V$; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	$V_{IN} = +10V$		3.25		3.25	mA
			$V_{IN} = -10V$	−3.25		−3.25		

NOTES
1 R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C)
3 Only 1 output may be shorted at a time and then only for a maximum of 1 second
4 See Figure 1 for threshold and hysteresis definitions

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $0°C \leq T_A \leq +70°C$

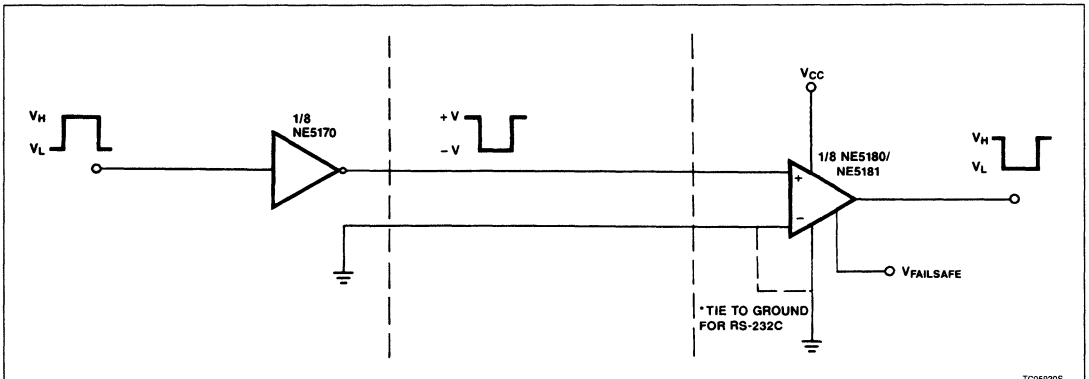
SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay — low to high	$C_L = 50pF$, $V_{ID} = \pm 1V$		500		100	ns
t_{PHL}	Propagation delay — high to low	$C_L = 50pF$, $V_{ID} = \pm 1V$		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, $V_{ID} = \pm 200mV$[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, $V_{ID} = \pm 500mV$	5.5		NA		MHz

NOTE:
1 $V_{ID} = \pm 1V$ for NE5181

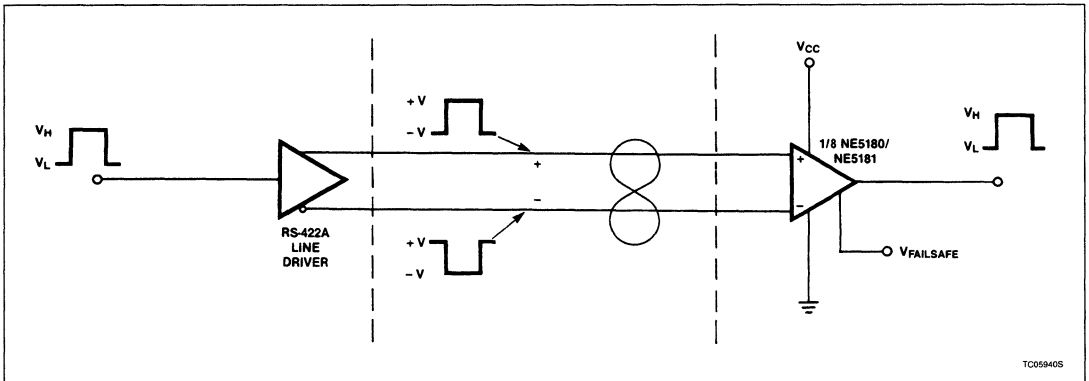
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides

APPLICATIONS

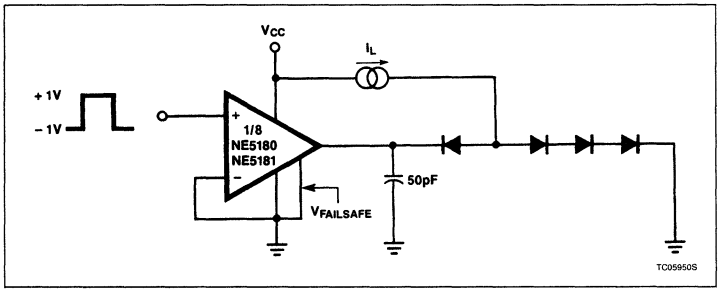


RS-232C/RS-423C Data Transmission

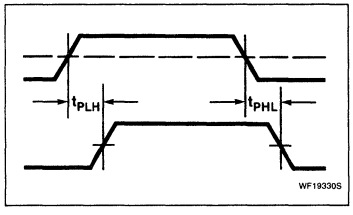


RS-422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



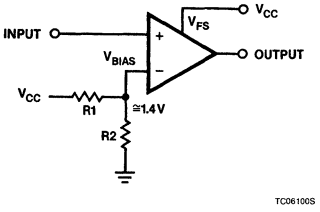
a logic "1" output under fault conditions, while a connection to ground provides a logic "0" There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1\,4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ± 500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).



NOTE:
Two silicon diodes may be used in place of R2

Figure 2. Single-Input Failsafe Programming

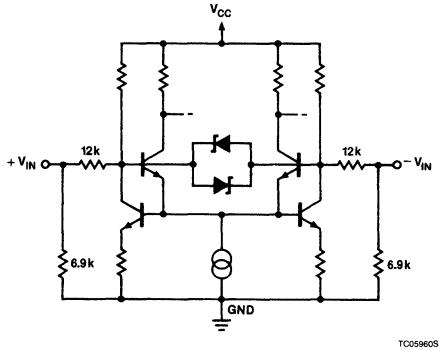


Figure 3. Differential Input Stage

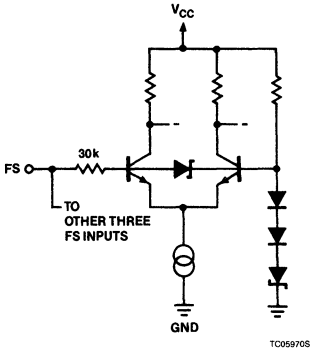


Figure 4. Failsafe Input Stage

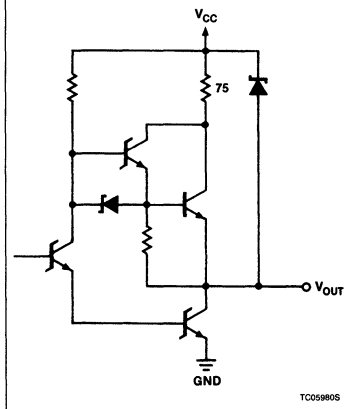


Figure 5. Output Stage

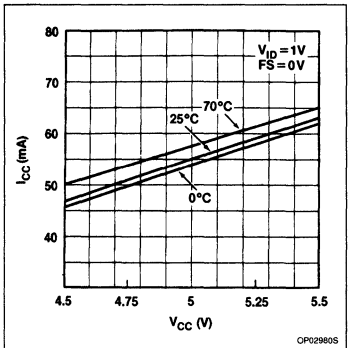


Figure 6. Typical Supply Current vs Supply Voltage

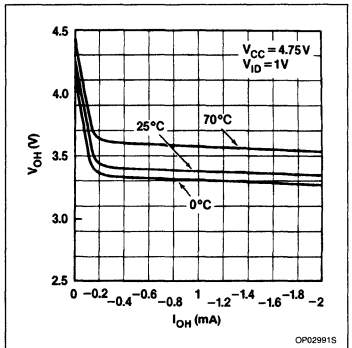


Figure 7. Typical High Level Output Voltage vs Output Current

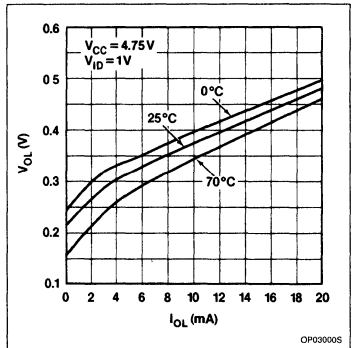
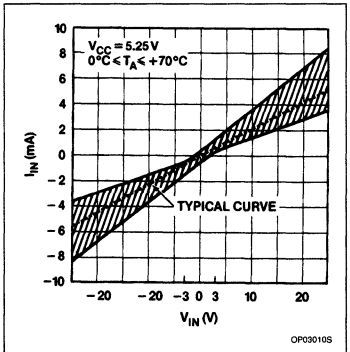


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded

Figure 9. Input Current vs Input Applied Voltage*

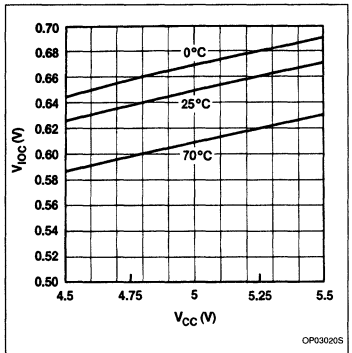


Figure 10. Typical V_{IOC} vs V_{CC}

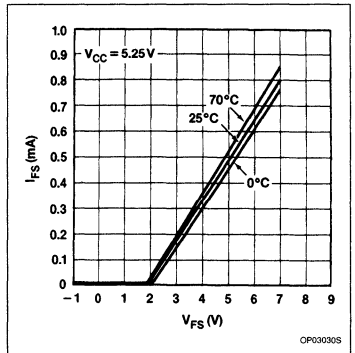


Figure 11. Typical FS Input Current vs FS Applied Voltage

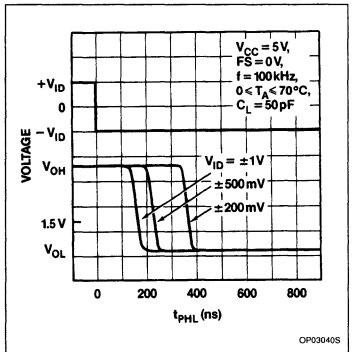


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

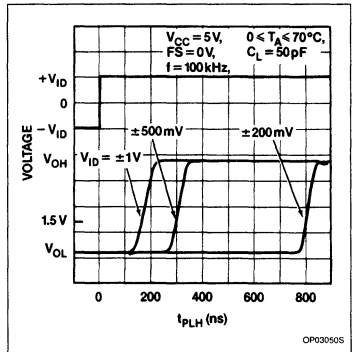


Figure 13. NE5180: Propagation Delay at Various Input Amplitudes

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Signetics

NE5050
Power Line Modem

Product Specification

Linear Products

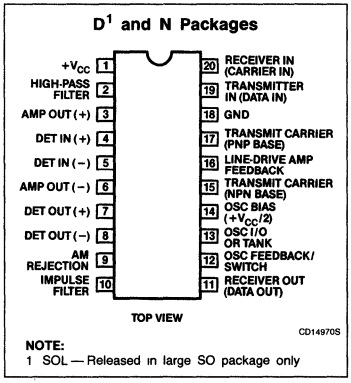
DESCRIPTION

The NE5050 is a modem for power line, coaxial cable, and twisted-pair communications. The modem incorporates features to overcome line impulse noise and line impedance modulation. The modem's transmitter incorporates a Colpitts oscillator, positive logic, carrier-on/-off switch, and a line driver. The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage, an impulse filter, and an SR flip-flop. One NE5050 can be used to transmit and receive with Amplitude Shift Key (ASK) carrier-on/-off modulation. With two NE5050s, Frequency Shift Key (FSK) modulation can be implemented. The transmitter input and the receiver output accept TTL or CMOS serial data.

FEATURES

- **High receiver sensitivity — typ. 1.5mV_{RMS}**
- **Receiver input overload protected for signals up to 70V_{P-P}**
- **High data rates — 300kbit/s ASK NRZ over twisted-pair**
- **The modem reaches the Nyquist limit of 1 bit per carrier cycle**
- **Has listen-while-talking for carrier sense multiple access/collision detect (CSMA/CD) networking capability**
- **Increased noise immunity with balance interstage ports for bandpass filtering**
- **Flexible oscillator can be made with LC tank (Colpitts), with crystal (Pierce), or accept external clock**

PIN CONFIGURATION



NOTE:
1 SOL — Released in large SO package only

- **Signals are processed in real-time making this modem suitable for repeater/carrier translation applications**

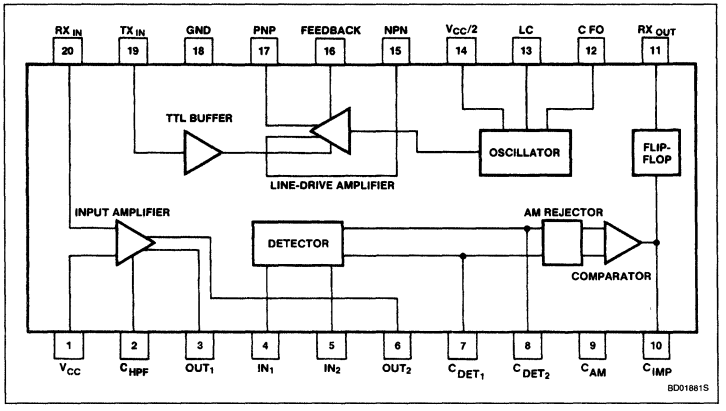
APPLICATIONS

- **Twisted-pair communications**
- **Coaxial cable communications**
- **120/277V_{RMS}, 50 or 60Hz, power line communications**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE5050N
20-Pin Plastic SOL	0 to +70°C	NE5050D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
V_{LOGIC}	Logic supply voltage	18	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation[1]	700	mW

NOTE:
1 The power dissipation is based on V_{CC} = 12V, T_J = +150°C, TX_{OFF} I_{CC} = 20mA, TX_{ON} I_{CC} = 50mA, θ_{JA} = 61°C/W 20-pin plastic package

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{CC} = 12V, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		10	12	16	V
I_{CC}	Supply current	TX_{OFF}	5	8	11	mA
I_{CC}	Supply current	TX_{ON}[1]	18	24	30	mA
V_{LOGIC}	Logic voltage			5	16	V
P_D	Power dissipation	RX_{OFF}, TX_{OFF} RX_{ON}, TX_{ON}, 100Ω load		100 300	220 660	mW mW
V_{IHMIN}	TX TTL input	TX_{ON}, Pin 19	2.4			V
V_{ILMAX}	TX TTL input	TX_{OFF}, Pin 19			0.8	V
V_{OLMAX}	RX open-collector output	I_{OL} = 5mA, Pin 11			0.4	V
I_{OLMAX}	RX open-collector output	Pin 11			5	mA
	TX data rate[2]	f_{CXR}=120kHz, 500kHz	DC	1k	300k	bit/s
	RX data rate[2]	f_{CXR}=120kHz, 500kHz	0.1	1k	300k	bit/s
	Carrier cycles per bit, TX and RX[2]		1			cycle
Broadband I/O ports, carrier						
	RX input sensitivity	1:1 input transformer	3.5	1.5		mV_{RMS}
	RX input signal level	V_{CC} ± 35V = −25V, +51V			70	V_{P-P}
	RX input impedance	Pin 20		9		kΩ
	RX line impedance modulation rejection	120HzAM 2V/20mV, 1kbit/s	40			dB
	RX carrier frequency[2]		0.1	120	500	kHz
	RX detector differential input impedance	Pin 4, Pin 5, each		27		kΩ
PSRR	RX power supply rejection ratio	60Hz and 120Hz		80		dB
	Broadband port impedance	RX_{OFF} and TX_{OFF}		7.3		kΩ
	TX output signal level	TX_{ON}, 100Ω load		8		V_{P-P}
	TX driver output impedance	TX_{OFF}		40		kΩ
	TX driver output impedance	TX_{ON}		1.2		Ω
	TX amplitude temperature drift	External oscillator		+140		ppm/°C
	TX amplitude temperature drift	LC oscillator		+0.23		%/°C
	TX output current capability	TX_{ON}, Pins 15, 17		40		mA peak

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DC ELECTRICAL CHARACTERISTICS (Continued)

$T_A = +25°C$, $V_{CC} = 12V$, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	TX output THD (total harmonic distortion)	TX_{ON}, LC oscillator		1	2	%
	TX line drive amplifier BW	At 6dB gain		500		kHz
	TX carrier frequency[2]		DC	120	500	kHz
	TX oscillator temperature drift	Temperature range		+60		ppm/°C
	TX oscillator initial frequency accuracy	Same LC tank		±1		%
	TX carrier feedthrough (leakage)	TX_{OFF}		−90		dBmO

ABBREVIATIONS:
TX = transmitter
RX = receiver

NOTES:
1 TX looped back to RX, data = 1kbit/s TTL, NRZ, 50% duty cycle ASK.
2. The NE5050 modem reaches the theoretical maximum data density for a given (fixed) carrier frequency. This limit is set by the maximum data bandwidth required before intersymbol interference occurs. The minimum specified limits are not tested in production. They are guaranteed by design and by characterization.

PIN FUNCTION DESCRIPTION

Pin 1: $+V_{CC}$
For decoupling V_{CC} to ground a 0.1μF capacitor must be placed close to Pin 1 and Pin 18.

Pin 2: C_{HPF}
High-pass filter, rejects 60Hz and its harmonics, rejects low frequencies, directing them to ground. Capacitor to ground: C_{HPF} = 10nF for f_{CXR} = 120kHz and C_{HPF} = 4.7nF for f_{CXR} = 300kHz. The input amplifier provides a high-pass function: a +20dB/decade frequency response, with a DC attenuation of −50dB. A frequency of 100kHz is amplified by +24dB. The −3dB point of this high-pass filter is given by the equation:

$$10^9/C_{HPF}\ (F) = f_{-3dB}\ (Hz)$$

Pin 3: OUT_1
RX amplifier differential (+) output. Low impedance output. See Pin 6. Pin 3 can be connected to Pin 4 directly. A differential, bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 4, Pin 5: IN_1, IN_2
AM detector (±) inputs. High-impedance inputs = 27kΩ each. They require DC bias voltage from Pins 3 and 6 or around 4.5V. Pin 3 can be connected to Pin 4 directly. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by series resistors. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 6: OUT_2
RX amplifier differential (−) output. Low impedance output. See Pin 3. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 7, Pin 8: C_{DET}
Amplitude detector (±) output capacitor between Pins 7 and 8. t_{DET} is the time it takes for C_{DET} to charge from 0mV to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. t_{DET} is a term in a sum of delays, the sum being the total receiver delay, t_D. See below in 'Receiver Delays' the relation between t_D and the maximum bit rate. The C_{DET} capacitor value is given by:

$$C_{DET}\ (F) = t_{DET}\ (sec)/10^5$$

Pin 9: C_{AM}
Line impedance modulation rejection capacitor. A 0.1μF capacitor to ground provides about 4s of delay for the transition from receive data to standby. The C_{AM} value is determined in function of the bit rate, or, more precisely, minimum bit time, to assure proper capture of leading bits in a bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic). Its value should be:

$$C_{AM}\ (F) = 10^{-4}/\text{bit rate [bits/s]}$$

Pin 10: C_{IMP}
Impulse noise rejection capacitor. At 1kbit/s a 10nF capacitor to ground provides 350μs of delay and impulse rejection. This capacitor determines the receiver impulse noise immunity (transmission channel with non-Gaussian noise). t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. t_{IMP} is a term in a sum of delays, the sum being the total receiver delay, t_D. See 'Receiver Delays' for the relation between t_D and the maximum bit rate. The C_{IMP} capacitor value is determined by the equation:

$$C_{IMP}\ (F) = t_{IMP}\ (s)/85k\Omega$$

The following equation determines t_{IMP}:

Maximum rejected or expected impulse noise width (s) < t_{IMP} (s)

Pin 11: RX Data Output
Open-collector RX output. RX data output.

$$I_{OLMAX} = 5mA = V_{LOGIC}/R_{PULL\text{-}UP}$$

Pin 12: C_{F0}
Oscillator feedback input. C_{FO} = 27 to 51pF capacitor between Pins 12 and 13. C_{F1} = capacitor between Pins 12 and GND. If the on-chip oscillator is used, C_{F1} may be omitted. If external oscillations are injected at Pin 13, C_{F0} must be removed and C_{F1} must be connected to GND. Grounding Pin 12 disables the oscillator.

Pin 13: Oscillator I/O
Colpitts LC oscillator tank, Pierce crystal oscillator, or external oscillator input.

On-chip LC oscillator — oscillator output. External oscillator tank present. Parallel LC components attached between Pins 13 and 14. C_{F0} attached between Pin 12 and Pin 13. A resistor between Pins 13 and 14 can decrease the oscillation amplitude to the desired level. Amplitudes above 2V peak may have THD > 2%. C_{F1} is not used. The amplitude varies with temperature; thermistor compensation recommended at Pin 16.

On-chip crystal oscillator — oscillator output. Two external capacitors in series, C_{13} and C_{14}. C_{13} is connected to Pin 13 and C_{14} is connected to Pin 14. The external crystal is attached between Pin 13 and the connection of C_{13} and C_{14} An optional inductor L, attached between Pins 13 and 14, tuned at the oscillation frequency by C_{13} and C_{14} prevents oscillations at the crystal overtones. C_{F0} and C_{F1} are not used.

External oscillator — oscillator input. Parallel LC components attached between Pins 13 and 14 provide bias to Pin 13 and perform bandpass filtering. If a square wave is generated from a microprocessor by clock division, a series LC from the divider output to Pin 13 will perform additional bandpass filtering. $C_{F1} = 0.1\mu F$ is connected to ground. C_{F0} is not used. If a sinusoidal wave is available, a 50Ω resistor may replace the parallel LC bandpass filter and a 0.1μF capacitor may replace the series LC bandpass filter. The amplitude is constant over temperature.

Pin 14: $+V_{CC}/2$
Oscillator bias at $+V_{CC}/2$. A 0 1μF decoupling capacitor to GND is optional. Parallel LC components attached between Pins 13 and 14.

Pin 15: TX Carrier Output (NPN Transistor Base)
Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

NPN external Darlington transistor — Drives 1Ω loads.

NPN external transistor drive —
$1\Omega - 0.5W - R_{E1}$ to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E1} between Pins 15 and 16 for 50Ω loads.

Pin 16: TX Line Driver Feedback
$R_{FEEDBACK}$ adjusts the driver amplifier gain Minimum gain ($R_{FEEDBACK} = 0$) is 2 (6dB). A thermistor can compensate the LC oscillator amplitude variation. R_{E1} resistor (and NPN EB junction) to Pin 15. R_{E2} resistor (and PNP EB junction) to Pin 17. The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20. The R_{DRIVE} value is the assumed line impedance. The C_{DRIVE} impedance is $1/(2 \times f_{CXR}\ C_{DRIVE})$.

Pin 17: TX Carrier Output (PNP Transistor Base)
Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

PNP external Darlington transistor — Drives 1Ω loads.

PNP external transistor drive — $1\Omega - 5.0W - R_{E2}$ to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E2} between Pins 16 and 17 for 50Ω loads.

Pin 18: Ground

Pin 19: TX Data Input
Transmitter TTL data input. Logic 1 will turn the transmit driver on, and sinusoidal carrier will be sent to the line from a low impedance source Logic 0 will turn the driver off, to high output impedance.

Pin 20: RX Carrier Input
Receiver carrier input. Withstands an overvoltage of $+V_{CC} \pm 35V$. DC bias connected through the line coupling transformer secondary to $+V_{CC}$ (Pin 1). The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20.

DESCRIPTION OF OPERATION

The NE5050 modem has been designed for transmitting and receiving control and data signals over the AC power lines, coaxial cables and twisted-pair cables. The modem overcomes line impulse noise and line impedance modulation. Two carrier modulation methods can be used: carrier on/off ASK, NRZ data and non-coherent FSK

The power line is not an ideal medium for communication. The line noise, interference, and losses are caused by. impulse noise, CW interference, line impedance modulation, and distribution transformer attenuation. NE5050 was designed to support both ASK and non-coherent FSK communications in this environment.

Listen-While-Talk

The IC modem is always in the receive mode, even when transmitting (it receives its own carrier) This capability permits remote RX and TX functionality testing for each system node In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the modem transmits carrier to other receivers and receives its own carrier.

On-Chip Collision Detection

The listen-while-talk capability enables this IC to perform CSMA/CD (carrier-sense, multiple-access/collision detect) networks. Collision is detected when the local TX intends to transmit and the line is not clear.

In Dense Data Traffic

The RX data output (RX_{OUT}) does not have time to go into the standby (lower power consumption, inverted logic) mode. In this case the RX_{OUT} is in positive logic (carrier-on = 1, carrier-off = 0). A collision is detected at the local node when the local TX is off and the local $RX_{OUT} = 1$. Collision: remote carrier present and detected. Abort local transmission. If, however, standby occurs (bursts of high-speed data) a proper value of C_{AN} will insure capture of all leading bits except for the first "10" transition.

In Rare Data Traffic

The RX_{OUT} is in standby most of the time. In this case the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A logic sequence from the local TX insures proper RX offset adjustment (preamble, the first "10" bits). The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is proportional to the value of the AM rejection capacitor at Pin 9. For C_{AM} = 10nF, the "receive data" to "standby" transition occurs after 4 seconds from the last "1". Therefore, long strings of "0"s can be transmitted and received. The standby function may be disabled with proper bias at Pin 9 (external components).

TX-to-RX and RX-to-TX Switching Times

With the listen-while-talk capability the TX-to-RX and the RX-to-TX switching times have the meaning of TX_{ON}-to-TX_{OFF} and TX_{OFF}-to-TX_{ON} switching times, respectively. The TX-to-RX and RX-to-TX minimum switching times can be calculated from the maximum data rate. Since one bit can last a minimum of 3μs (NRZ ASK data), this may be considered the minimum switching time.

Data Rate

The maximum data rate is 300kbit/s NRZ ASK. This data rate was achieved on a twisted-pair cable with a 150kHz, 50% duty cycle square wave for data. The data rate depends on the BPF (between Pins 3 – 4 and 5 – 6), on the AM detector capacitor for delay, C_{DET} (between Pins 7 and 8), on C_{AM} (Pin 9) for capture of leading bits, and on the desired impulse noise immunity for delay, C_{IMP} (Pin 10).

AC Line Coupling Network

One or two (120V or 240V and 277V AC RMS) coupling capacitors rated 600V are connected in series with the primary of a 1:1 transformer and connected to the AC line. The transformer secondary may be tuned to the carrier frequency by a capacitor (TOKO

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transformer, low data rates) or no secondary tuning capacitor for higher data rates (AIE Magnetics transformer). Two back-to-back zener diodes must be placed between Pins 1 and 20 for the IC transient protection (1N4744 or 1N6275). The transformer secondary carries DC bias current between Pins 1 and 20 of the IC. This coupling network itself attenuates to below the RX input sensitivity the 50 or 60Hz and their harmonic frequencies. In a coaxial cable application the transformer can be replaced with a coupling capacitor.

Receiver (RX)

The typical RX sensitivity is $1.5mV_{RMS}$. For less sensitivity, adjust the turn ratio of the coupling transformer or insert loss in the bandpass filter. The RX-only function can be implemented by not using the oscillator and by grounding the TX input. The maximum data rate is 300kbit/s. The power supply rejection ratio (PSRR) is 80dB for 60Hz and 120Hz. The RX is composed of the following blocks:

The Input Amplifier/Limiter limits its output signals to $1.2V_{P-P}$. The maximum input carrier signal can be $70V_{P-P}$. The gain is 24dB. The input amplifier bandpass characteristic has the upper −3dB frequency internally fixed at 300kHz. The lower −3dB frequency is adjustable with the C_{HPF} capacitor from Pin 2 to GND. For maximum RX sensitivity C_{HPF} = 10nF at f_{CXR} = 120kHz. A C_{HPF} = 0.1μF value attenuates 60Hz by 50dB and 120Hz by 45dB.

The Bandpass Filter is differential RLC bandpass filter which can be connected from Pins 3, 6 to Pins 4, 5. The LC values are the same as the oscillator LC values (see Pins 13 and 14). The formulae relating the BW_{-3dB} to the RLC values are:

$$BW_{-3dB} / \omega_{CXR} = (\omega_{CXR} * L) / (2 * R) = 1 / Q$$

$$BW_{-3dB} / \omega_{CXR} = 1 / (\omega_{CXR} * 2 * C * R) = 1 / Q$$

$$BW_{-3dB} = (\omega_{CXR} * \omega_{CXR} * L) / (2 * R)$$

$$BW_{-3dB} = 1 / (2 * C * R) \text{ and } \omega_{CXR} = 2 \times f_{CXR}.$$

If no bandpass filter is required, connect Pin 3 to 4 and Pin 5 to 6 ($R_1 = R_2 = 0\Omega$).

The Amplitude Detector is a Gilbert phase detector with a single differential input. The compared signals are always in phase and the demodulated output is a full rectified wave, function of the bias current, the carrier amplitude, and the collector load. The detected voltage is developed across a differential capacitive load between Pin 7(+) and Pin 8(−). DC offset is caused by line impedance modulation.

The AM Rejection Circuit stabilizes the DC average value of the envelope by adding or subtracting a series voltage to the voltage of the detector capacitor. The AM rejection is 40dB at a modulation rate of 120Hz. The value of the AM rejection capacitor C_{AM} (Pin 9 to GND) determines the transition times to and from receive data and standby.

The Slicing Comparator has current output and a fixed threshold of 50mV.

The Impulse Filter consists of a capacitor, C_{IMP}, at the output of the comparator, from Pin 10 to GND. This capacitor is charged or discharged with constant current from the comparator, causing the voltage variation to be a constant slope in time. Narrow current impulses will not last long enough to fully charge or discharge the capacitor.

$2V_{BE}$ Voltage Hysteresis provides a voltage interval in which the C_{IMP} voltage ramps and in which both inputs to the SR flip-flop are zero.

The Flip-Flop is an SR type, with an open-collector transistor output at Pin 11. The transistor can switch a maximum load of 5mA.

Receiver Delays and Maximum Data Rate

The total receiver delay is a sum of delays, where t_{DET} (sec) is the detector delay, t_{IMP} (sec) is the impulse filter delay, and 2μs is the approximate receiver delay with no C_{DET} and no C_{IMP}:

$$t_D \text{ (sec)} = \text{total receiver delay} = t_{DET} \text{ (sec)} + t_{IMP} \text{ (sec)} + 2\mu s$$

The maximum bit rate, in the no-return-to-zero, amplitude shift keying data format is determined by: Maximum bit rate MRZ ASK (bit/sec) $< 1/t_D$ (sec^{-1})

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall determine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100 bits/sec and at 50 kbits/sec, the C_{IMP} / C_{DET} capacitor ratio ranges from 100:1 to 1:1.

Transmitter, TX

The transmitter includes an oscillator, a line driver, and a drive switch.

The TTL Switch is a low power TTL gate that switches on/off the bias current for the line driver. A logic "1" at Pin 19 (TX_{IN}) enables the line driver and carrier is being sent on the line. A logic "0" disables the driver.

The Oscillator is a differential transistor pair. It can be configured as a Colpitts LC oscillator, as a Pierce crystal oscillator, or used with external input (microprocessor clock divided to the carrier frequency). When the TX drive is off, the carrier leak is less than −90dBmO. Pin 18 can be used as input for an external oscillator. Grounding Pin 12 disables the oscillation process.

The Line Driver is a class AB push-pull stage with optional external complementary transistor pair for increased current capability. The TX output impedance is 40Ω in the off-state (receive mode) and less than 2Ω in the on-state (transmit mode). Note that in the transmit mode one receives its own signal. To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16.

By itself the NE5050 is capable of driving a consumer line impedance of 50Ω (40mA peak/80mA peak non-repetitive), the THD being less than 2%. With complementary transistors, 10Ω industrial loads can be driven. With complementary Darlington transistors, 1Ω industrial loads can be driven.

One design objective was to provide the user with a flexible IC modem for residential as well as for industrial AC lines, for twisted-pair, and for coaxial cables. The IC modem can be used for control functions and data applications. Practical observations of power line noise point to a data rate upper boundary of 1kbit/sec. The main sources of interference are the light dimmers. Software for error correction can be used for improved error rates. Two system configurations can be implemented: an ASK system and a non-coherent FSK system. The non-coherent FSK system can continue to transmit ASK data if the other channel is made unusable by CW interference. High-voltage transient protection and filtering are accomplished with user-selected external components.

Additional flexibility is provided by the chip architecture: one-IC real-time repeater, one-IC dual-frequency gateway, external oscillator input port, the listen-while-talk capability (CSMA/CD), immediate TX-to-RX switching, ASK and FSK, and ASK-multinode single-frequency network.

The modem can be used for control systems and data applications in homes and other consumer environments and in industry.

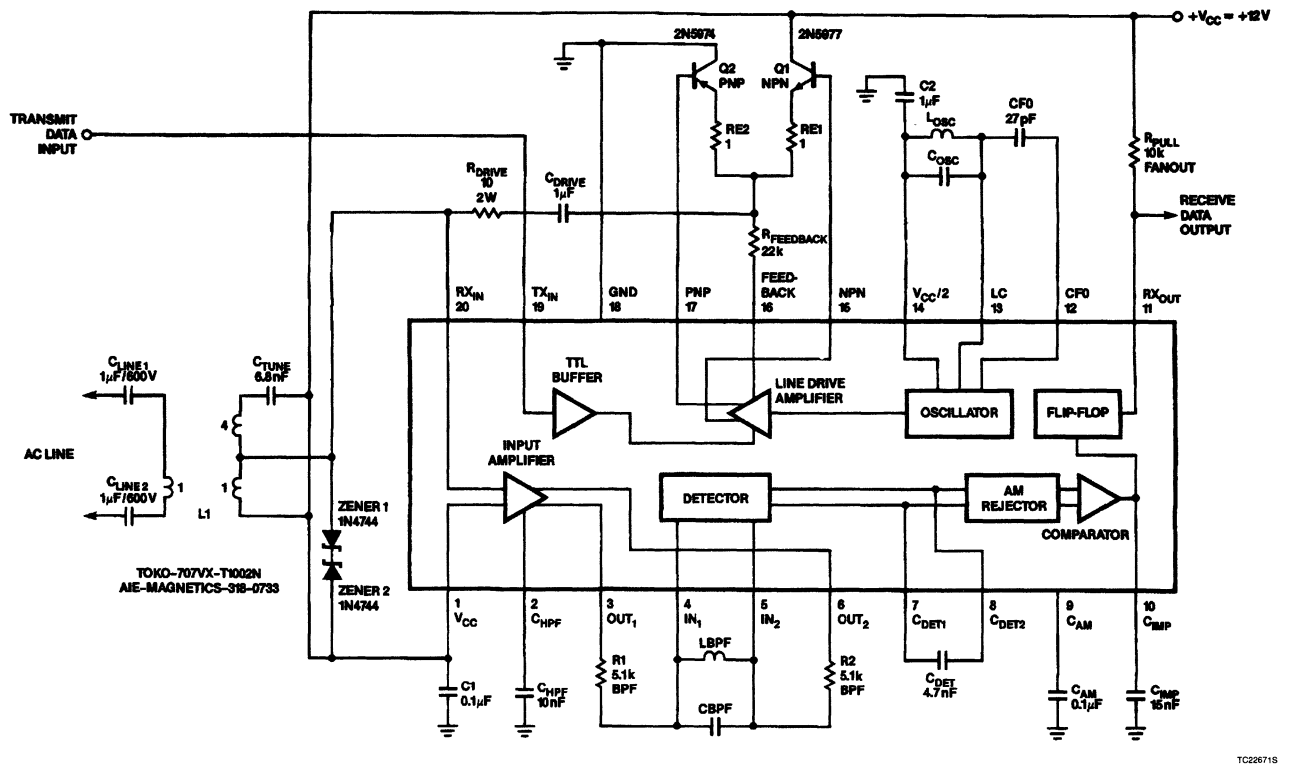

Figure 1. Typical Application Circuit for 1kbit/s on the 120/277V AC Line

Signetics

Linear Products

AN1951
NE5050: Power Line Modem Application Board Cookbook

Application Note

Author: Michael J. Sedayao

INTRODUCTION

Applications Disclaimer

The applications outlined within this cookbook in no way specify the absolute maximum performance of the NE5050 Power Line Modem. They are merely examples given to show the flexibility of the part. In general, the external components used for each application tend to be the limiting factors in each application. For example, the component drift for capacitors that provide a load on the oscillator would cause a corresponding drift in the oscillator frequency, although there is nothing wrong with the chip itself. On the other hand, external drive transistors provide a larger transmitter voltage than what would normally be available from direct drive with the chip.

Only careful characterization of the operating environment (whether it is the power line, twisted pair, or coaxial cable) coupled with a knowledge of the external component limitations, can ensure reliable operation for a given application. Often, operating problems originate with an applications fault rather than with the chip itself.

One reason that the part may not always work in every situation is the same reason that it can work in so many situations — the part is extremely flexible. Operation is dependent on the values of the external components. For instance:

- To change the carrier frequency, change the oscillator capacitor and inductor. To receive the same signal, however, the BPF values must also be changed to the same values. Active filters or no filters can be used. The tuning capacitor must also be changed so that the transformer secondary locks onto the carrier. The oscillator can also be driven with an external source.
- To adjust the limiting of the data rate, the detection capacitor has to be changed. If the data rate is increased without adjusting this capacitor, the bit rate will be RC-filtered out.
- Adjusting the impulse capacitor will provide protection from transients of a certain duration, but leaves a vulnerability to longer ones or a succession of smaller ones.

Each of these cases should illustrate the fact that the performance of the board is extremely application and environment dependent. The environmental parameters and goals of data transmission should be determined before specifying component values. Proper operation depends on it.

Summary of Operation

The AC power line is, in general, not ideal for data communication. Impulse noise, large magnitude voltage transients (> 1kV typical), line impedance modulation, and other factors, have prohibited its use as an effective medium for transmitting data and control signals.

The NE5050 Power Line Modem (PLM) has been designed to overcome these problems while affording the user the flexibility of tailoring the design to his/her own needs. The PLM can be used to transmit over power lines or twisted-pair cables using two forms of modulation — carrier on/off ASK (Amplitude Shift-Keying) and non-coherent FSK (Frequency Shift-Keying). To use it in the FSK mode, two devices will be required for each transceiver in order to bandpass and generate the two different frequencies representing logical 0 and 1. If one of the two frequencies used fails, the remaining frequency can be used in the ASK mode. The applications referred to in this cookbook only refer to the single-carrier ASK form. Some of the features of the IC include:

Listen-While-Talk

The modem is always in the receive mode, even when transmitting (it receives its own signal). This capability permits RX and TX remote functionality testing for each system node since it requires no other transceivers. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the IC transmits an ASK carrier to the other receivers, including its own. It is up to the user to design protocol to arbitrate ownership of the line. In some protocols, such as in General Electric's HOMENET®, the listen-while-talk feature is not desired and so the receiver is disabled during transmission mode.

On-Chip Collision Detection

The listen-while-talk capability enables a controller to perform CSMA/CD (Carrier Sense, Multiple Access/Collision Detect) functions. To summarize (for further information, the reader is referred to IEEE 802.3 and to general articles describing ETHERNET or other probabilistic network protocols), any node can access the line to transmit signals at any time provided the line is not being used. The procedure is as follows. A receiver listens to the line to see if there are any carriers present (Carrier Sense). Every receiver is also listening to the line (hence, Multiple Access). If a transmitter is on, each node waits until the line is free before transmitting. Priorities may be established by the controller. A collision is detected if, while transmitting a message, an incoming transmission originating from another node is detected.

The PLM performs a similar operation for both dense and rare data traffic situations. In dense data traffic, the RX data output (RX_{OUT}) does not have time to go into the standby (low power consumption, inverted logic mode). In this case, the RX_{OUT} is in positive logic (carrier on = 1, carrier off = 0). A collision is detected at the local node when the local TX is off and the local RX_{OUT} = 1. Therefore, a remote carrier is present and has been detected, so abort local transmission. The line is busy. Wait until the line is clear.

In rare data traffic, the RX_{OUT} is usually in the standby mode. In this case, the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A "10" logic sequence from the local TX insures proper RX offset adjustment (the preamble contains the first two "10" bits) and collision detection can be performed with the next "10" bits. The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is typically 4 seconds and this time is independent of the data rate. This enables long strings of "0's" to be transmitted and received.

To eliminate the standby mode and to have the modem in the receive-data mode at all times, the bias at Pin 9 should be altered. A 10MΩ resistor from Pin 9 to a potential of $2.2V_{DC}$ will perform this change. The 2.2V potential may be generated between two resistors: 1MΩ from V_{CC} = 12V and 220kΩ to ground.

Power Supply Decoupling (C1 and C2)

Capacitor $C_1 = 0.1\mu F$ at Pin 1 decouples the supply voltage, V_{CC}. The capacitor $C_2 = 0.1\mu F$ at Pin 14 is optional and decouples the supply for the oscillator section. This

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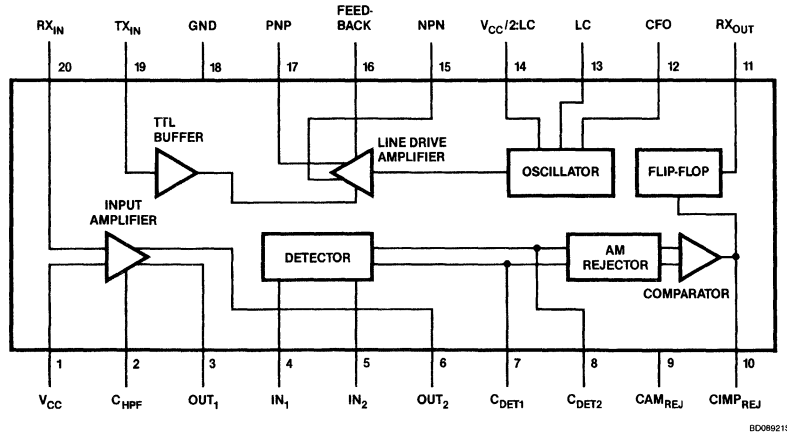

Figure 1. Block Diagram

supply, $V_{CC}/2$, is internally generated. C_1 is essential for clean operation and should be placed as close as possible to the IC, between Pins 1 and 18.

AC Line Coupling

The line transformer, a Toko America 707VX-T1002N, has a primary-to-secondary coil ratio, L_1:L_2, of 1:1. One end of coil L_1 goes to the power line via line capacitor C_{LINE}. The secondary signal is tapped off between L_2 and L_3 and then goes to the receive input (Pin 20.) The other turn ratio is L_1:L_3 at 1·4. The L_2 secondary is connected between Pins 1 (V_{CC}) and 20 (RX_{IN}) It carries about $1mA_{DC}$ current into Pin 20 for biasing. The $L_2 + L_3$ secondary is tuned to the carrier frequency by a tuning capacitor C_{TUNE} = 6.8pF. This transformer is suitable *only* for data rates up to 10kBits/sec because of envelope distortion

To tune the transformer for maximum sensitivity, connect a BNC "T" connector to the output of the waveform generator One output should go to an oscilloscope and the other should be connected to the prongs of the power cord of the board (make sure ground is also connected to one prong). Then send the 100% AM modulated pulse train (ASK) to the board. The carrier envelope is a square-wave pattern. Tune the transformer for maximum carrier amplitude. To do this take a jewel-head screwdriver and adjust the transformer core. Maximum sensitivity is reached at maximum amplitude at the carrier frequency

Another manufacturer that provides good transformers for both power line and twisted-pair communication is AIE Magnetics (Address and telephone numbers for TOKO and AIE Magnetics are listed in the External Components Section).

Line and Tuning Capacitors (C_{LINE} and C_{TUNE})

C_{LINE} = 1μF AC-couples the transformer to the power line and is rated to withstand 600V. Its main function is to filter out the 60 and 120Hz signals from the line power and to pass only the higher frequency carrier signals. C_{LINE} and the primary inductance of the transformer act as a voltage divider that attenuates 60Hz signals by 100dB Line voltage signals are less than a millivolt on the secondary of the coupling transformer. Remember to discharge this capacitor before removing the insulating backplane and changing components.

C_{TUNE} = 6.8nF tunes the transformer secondary winding to the carrier frequency (100kHz) Make sure to change this capacitor in addition to the LCs of the oscillator and bandpass filter sections when changing the carrier frequency.

TRANSCEIVER EXTERNAL COMPONENTS

Figure 1 is a block diagram of the NE5050. It comes in a 20-pin DIP (Dual In-Place package) in both plastic and SO (Small Outline). This section describes the external components that must be added and the characteristics to expect at those pins.

Receiver

Input Filter C_{HPF} (Pin 2)

The input amplifier limits its output signals to $1.2V_{P-P}$ differential. On Pin 20, the maximum input carrier signal can be $70V_{P-P}$, centered at V_{CC}. The amplifier gain is 24dB at the carrier frequency The input amplifier bandpass characteristic has an upper −3dB frequency internally fixed The lower −3dB frequency is set by C_{HPF}. C_{HPF} actually suppresses the lower order harmonics. With C_{HPF} = 100nF, 60 and 120Hz are rejected more than 40dB (see Figure 2). For lower values of C_{HPF}, this rejection increases along the frequency spectrum. For a 1nF capacitor, amplifier response has large peaking near 500kHz. Response for values of 10, 100, and 1000nF are also shown over the frequency range 0.01 − 100MHz.

C_{HPF} is connected from Pin 2 to ground For carrier frequencies above 100kHz, typical values for C_{HPF} are between 2 and 20nF. The amplifier has differential outputs (Pins 3 and 6). The DC voltage at these pins is 4.6V.

Inter-Stage Bandpass Filter R1, R2, C_{BPF}, L_{BPF} (Pins 3, 4, 5, 6)

If all necessary bandpass filtering is performed in the line-coupling network, then the BPF between input amplifier output and AM detector input is not needed It is also possible to bypass use of the filter in most twisted-pair applications. Otherwise, for ASK operation, L_{BPF} and C_{BPF} should match the LC tank components L_{OSC} and C_{OSC} of the oscillator in order to have effective carrier sense. The carrier frequency is simply defined as

$$\omega_{CXR} = \frac{1}{\sqrt{L_{BPF} \times C_{BPF}}}$$

The bandpass characteristics are governed by the following equations relating 3dB band-

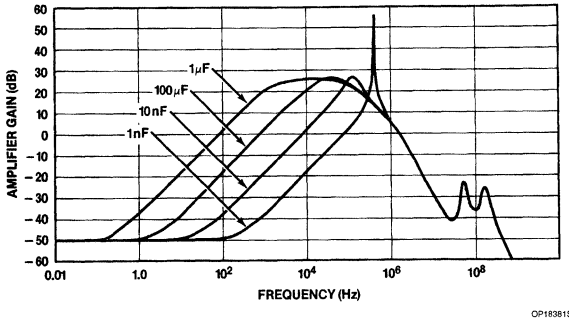

Figure 2. Receiver Amplifier Gain vs Frequency for Different Values of C_{HPF}

width to carrier frequency ω_{CXR} and components R_1, $R_2 = R$, L_{BPF}, and C_{BPF}.

$$BW_{-3dB} = \frac{(\omega_{CXR}{}^2 \times L_{BPF})}{(2 \times R)}$$

$$BW_{-3dB} = \frac{1}{(C_{BPF} \times 2 \times R)}$$

These equations can easily be manipulated to express the Quality factor, Q:

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{(\omega_{CXR} \times L_{BPF})}{(2 \times R)} = \frac{1}{Q}$$

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{1}{(\omega_{CXR} \times C_{BPF} \times 2 \times R)} = \frac{1}{Q}$$

Since this is a passive filter, a good deal of signal attenuation should be expected. If there is trouble getting signals through, consider shorting out the bandpass by shorting Pin 3 to Pin 4 and Pin 5 to Pin 6. If this does not work, trace signal from RX_{IN} (Pin 20) and follow through.

Depending on the filtering configuration, Pins 4 and 5, the AM detection input requires DC biasing. If no DC path is provided from Pin 3 to 4 and from 6 to 5 (series capacitors present for DC open-circuit), then the network in Figure 3 can be used.

Active bandpass filters may be used if gain is desired in the signal. This allows more room for tweaking. Remember, the goal is to bandpass the broadband signal (ω_{CXR} = 100kHz for the industrial operation) and *not* the baseband signal (1kBits/s for the same application) as can be seen from the above equations For more details on alternative BPFs, see the section on High Performance Industrial Operation.

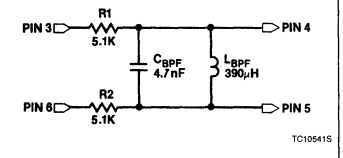

Figure 3. Single-Pole Bandpass Filter for 118kHz Operation

AM Detection C_{DET} (Pins 7 and 8)

The capacitor C_{DET} is the load across the collectors of a Gilbert multiplier cell (Pins 7 and 8) that is being multiplied by itself. So compared signals are always in phase and demodulated output is a function of carrier amplitude (hence, detects AM signals), bias current, and collector load. (Internally there are resistors in the collectors of the cell so the part *will* run without C_{DET} included.) Since it is the load, it has to be charged and discharged, and thus delays the transition of the signal. C_{DET} introduces a delay in signal transmission because of its integrating action. The combination of C_{DET} and the collector resistors provides an RC low-pass filtering action on the received signal The carrier (broadband) is filtered out and only the envelope (baseband) is passed. Consequently, C_{DET} provides the limiting value for the data rate. The 4.7nF value is fine for 1kBit/sec operation, but, if an increased data rate is desired, the value of the capacitor should be reduced. Similarly, for a longer delay and reduced data rate, increase C_{DET} (see Figure 4).

If C_{DET} is removed altogether, a reduction in signal delay should be observed (full-wave rectification). There will still be a signal if the impulse capacitor is connected. Removing both C_{DET} and C_{IMP} should eliminate signal delay entirely.

Probing at this point (Pins 7 and 8) should reveal a square wave with rising edges following a $1 - \exp(-t/RC_{DET})$ type of curve. Similarly, the falling edge should show an $(\exp(-t/RC_{DET}))$ type of characteristic. Probing on the complementary pin will just show the inversion of the signal. This should be expected since just the charging and discharging of the detection capacitor are being observed.

AM Rejection C_{AM} (Pin 9)

The AM rejection circuit tracks the average DC value of the envelope by adding or subtracting a series voltage to the voltage on the C_{DET}. (It operates as a negative feedback voltage mechanism for changes on the AM detector load by the additional DC components on the line.) AM rejection is better than 40dB. $C_{AM} = 0.1\mu F$ typical for 40dB rejection for 120Hz AM. This value will suffice for most power line applications. For a different case, look at the Twisted-Pair Applications.

If the received signal remains at the zero state after a 1-to-0 (on-to-off) transition for more than 4 seconds, the RX_{OUT} pin will drift to the logic High level and stay there until the signal changes state again. This is known as the standby mode. This feature can be defeated by externally applying a $2.2V_{DC}$ signal (see HOMENET application). Any protocol should take this feature into account if it does not externally defeat the feature through the hardware.

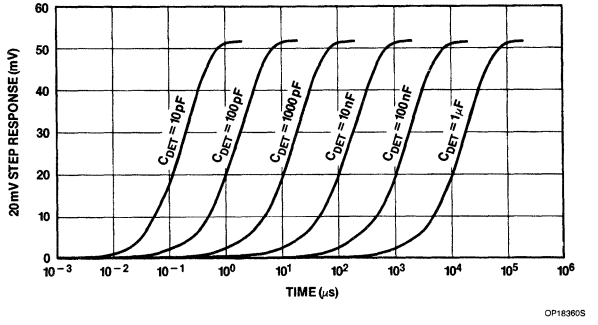

Figure 4. Comparative Delay of AM Detector for Different Values of C_{DET}

Impulse Rejection C_{IMP} (Pin 10)
This capacitor allows the device to absorb the line transients that sometimes reach peak values of several thousand volts. It also reduces the effect of the glitches caused by different line loads. C_{IMP} is charged or discharged with constant current from the comparator which causes the voltage variation at Pin 10 to be of constant slope versus time. Narrow current impulses will not last long enough to fully charge or discharge C_{IMP} ($I_{CIMP} = C_{IMP} \times (\Delta V/\Delta T)$) The baud rate depends on the size of C_{IMP} Typically, rejected impulse width $\leq C_{IMP} \times 35k\Omega$ (sec) $\leq$ minimum data width.

The delay in recovering data that is introduced by this stage is

$$t_{DELAY} = C_{IMP} \times 35k\Omega.$$

If this point is probed, a square wave with a well-defined slope on the rising and falling edges should be seen. The slope is a function of the output current of the comparator and the capacitance on this pin (I_{CIMP} and C_{IMP}).

Logic Output R_{PULL} (Pin 11)
This is an open-collector output and needs a pull-up resistor to let it swing to a High value The listed value of 10kΩ is fine. It can be decreased for a maximum $I_{OL} = 10mA$. Also shown in the diagram is an optional supply $V_{LOGIC} = +5V$ provided by the user to give TTL-level compatibility. Otherwise, the output should swing all the way to +12V and all the way down to ground.

The point can be probed while the signal is transmitted to see if the IC is receiving its own transmission. Carrier feedthrough may be seen on the output signal

Transmitter

The transmitter input (TX_{IN}) is at Pin 19. A logic "1" enables the line driver and sends the carrier on the line A logic "0" disables the carrier, which constitutes the on/off Amplitude Shift-Keying. When in the receive mode, this pin should be grounded. Make sure that the TX_{IN} levels are TTL compatible. Signals that are more than one V_{BE} (0.7V) below ground turn on a diode that disables the transmitter External components to be set for the transmitter are as follows:

Carrier Frequency (R_{OSC}, C_{OSC}, L_{OSC}, C_{F0}, C_{F1})
The carrier frequency is set internally by a differential-pair Colpitts Oscillator. To set the frequency externally, apply the signal to LC (Pin 13). Pin 13 is the input for external operation and the load for use of the on-board oscillator.

If an external carrier is not desired, set the oscillator frequency by the 5 external components listed above. (Note: $C_{F1} = 0$ in this application. Increasing it merely raises the level of AC feedback to the oscillator. It would only be important in the wideband operation since it provides a reference for the other end of the differential pair.) The design equation for the ω_0 is (ω_0 should equal ω_{CXR}):

$$\omega_0 = \frac{1}{\sqrt{L_{OSC} \times C_{EQ}}}$$

$$(\omega_0 = 2\pi f_0)$$

where C_{EQ} is given by

$$C_{EQ} = C_{OSC} + \frac{C_{F0} \times C_{F1}}{C_{F0} + C_{F1}}$$

Since $C_{F0} >> C_{F1}$, then

$$C_{EQ} = C_{OSC} + C_{F0}$$

Carrier leakage in the off state is minimal and should have no effect on the receive input, RX_{IH} (Pin 20)

Output Stage (Q1, Q2, R_{E1}, R_{E2})
The line driver is a class AB push-pull output stage with optional external complementary transistor pair for increased current drive capability. The TX output impedance is 40kΩ in the off state (RX_{ON}, receive mode) and less than 2Ω in the on state (TX_{ON}, transmit mode).

By itself, the NE5050 is capable of driving a *consumer* line impedance of 50Ω *without* the drive transistors Q1 and Q2. To do this, set $R_{E1} = R_{E2} = 10\Omega$, placing R_{E1} between Pins 15 and 16, and R_{E2} between Pins 16 and 17; select $R_{DRIVE} = 50\Omega$ The voltage divider effect is evident

With the external drive transistors, however, the PLM is capable of driving an *industrial* line impedance of 10Ω. Merely set $R_{E1} = R_{E2} = 1\Omega$ and set $R_{DRIVE} = 10\Omega$.

Feedback ($R_{FEEDBACK}$)
To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16. $R_{FEEDBACK} = 75k\Omega$ is fine for $V_{CC} = +15V$ operation. For $V_{CC} = +12V$, use a 22kΩ resistor. If you are not using external drive transistors and are using $V_{CC} = +12V$, then use a 56kΩ resistor.

Transmitter Drive (R_{DRIVE}, C_{DRIVE})
R_{DRIVE} and C_{DRIVE} provide impedance matching for the output of the driver for coupling back through the transformer. R_{DRIVE} provides the real component and C_{DRIVE} the complex. R_{DRIVE} should be set to 50Ω for consumer applications, with no external transistors needed (set R_{E1} and R_{E2} as above), or for industrial applications, use $R_{DRIVE} = 10\Omega$ with the drive transistors, setting R_{E1} and R_{E2} as indicated

INDUSTRIAL APPLICATION

Electrical Hazards to the User

WARNING: ELECTRICAL SHOCK HAZARD! DO NOT PROCEED UNTIL YOU HAVE READ THIS SECTION !

In addition to being a supply of $110V_{AC}$, the power line is a near-infinite source of current and it only takes 100mA to kill a human being. (It takes about 80mA to fibrillate the heart and give a serious shock. Approach the board testing as though you were going to repair a television set.) So remember, 110V of AC line voltage is present on the line cord, the line coupling capacitor (C_{LINE}), and on the transformer primary. Please exercise extreme caution when using these boards. Even if the cord is not plugged into the AC power line, C_{LINE} can retain charge. After being unplugged, if touched before discharged, it can give a severe electric shock.

Certain measures have been made to protect the user from being exposed to the power line. A silicone resin has been applied to the line cord on the top of the board and a mylar plate has been attached via four nuts to the bottom of the board. Before changing components, please use the following procedure:

1. Unplug the cord from the AC line. Always use one hand when plugging or unplugging the cord. A good procedure to follow would be to set the board down first and then plug it in with the same hand, keeping the other in your pocket. Holding the board in one hand (exposed AC) and the plug in the other could turn *you* into the load if you are careless.
2. Discharge the coupling capacitor by holding the unplugged cord by the insulated portion of the plug and then short the plug prongs with an insulated screwdriver. Be sure to hold the screwdriver by its insulated handle. As you touch the screwdriver to the prongs, you should hear a slight 'pop' from the discharge. If you don't hear the pop, it could be an indication that the line capacitor is bad.

   NOTE:
   Transient protection must be incorporated between Pins 1 and 20 when following this procedure (i.e Back-to-Back zeners or transient absorbers).
3. Remove the plastic nuts, screws, and the mylar plate.
4. After changing components and soldering, *replace* the nuts and mylar plate. *NEVER* operate the board or plug it into the AC line without the cover. It is very easy to leave a wire or a piece of solder on the bench and short the AC line when you set the board down. This is a possible fire hazard and will usually trip the

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circuit breaker for your area, killing the power in the area. (This actually happened while testing application boards.)

Do not attempt to remove the silicone from the line cord on the top of the board. This isolates you from the line while probing the component side. Do not defeat this safety feature.

Do not operate on metallic or other types of conductive surfaces. Always operate with the mylar plate on the backplane of the board. Refer to #4 above for what can happen if you leave the board off.

Do not keep drinks or liquids in the area. A spilled drink can be disastrous.

NOTE:
Signetics provides these NE5050 Power Line Modem Application Boards for design and development purposes only. Signetics assumes no liability and makes no guarantees regarding the performance of these boards. By acceptance of these demo boards, the user agrees to follow the instructions described in this manual and releases Signetics from any liability and claims resulting from use of these boards including but not limited to third party claims

OBSERVING THE NE5050 DEMONSTRATION BOARD PERFORMANCE

Operation of the NE5050 Demonstration Board

Figure 5 is the schematic for the NE5050 demonstration board. The demo board is designed to operate at a carrier frequency of 118kHz. From left to right on the schematic, the board is coupled to the power line via a 1-1 ratio Toko brand transformer. Two high voltage 47μF capacitors provide blocking of the 50/60Hz high voltage from the power line (and pass the high-frequency carrier). The presence of a times-4 wound secondary coil is used in series with C_{TUNE} to set up a secondary which is resonant with the carrier frequency. This resonance should be tuned via the transformer core to provide minimum attenuation of the carrier frequency

The signal (and whatever line noise is present) is then presented differentially to the input amplifier (Pins 1 and 20). Two 15V, 1W zener diodes are connected between these pins to protect the IC from high voltage spikes (note that this can happen, for example, when discharging the line capacitors by shorting the plug). The input amplifier is also configured as a high-pass filter whose characteristics are determined by the value of the capacitor on Pin 2 (C_{LPF}). See Figure 3 for bode plots. The input amplifier/filter will provide about a 20dB boost of the carrier frequency The signal is then output to Pins 3 and 6 to an externally-connected band-pass filter. On the demonstration board this is a single-pole RCL filter tuned to approximately 118kHz.

Pins 4 and 5 form the input to the amplitude detector which performs signal decoding via amplitude detection and amplitude modulation cancellation. This detector will trigger at the presence of a signal at a level of $20 - 30mV_{RMS}$ The amplitude modulation cancellation stage allows for continuous amplitude modulation of the carrier frequency without loss of data (as long as the amplitude fluctuations are above the detector threshold).

The final stage is the impulse filter which rejects short-duration impulses of a duration determined by the value of the impulse capacitor (C_{IMP}) connected at Pin 10. Pin 11 is the open-collector output which provides a TTL-level demodulated output. This output is connected to a 10k resistor pull-up which is tied to the output post labeled "V_{LOGIC}". The TTL level signal appears at the post labeled "REC". An NPN transistor forms an open-collector inverted output at the post labeled "REC OC."

The transmitter section consists of an oscillator whose frequency is determined by the externally connected LC tank at Pins 13 and 14. These are of the same value as the LC tank used for the band-pass filter at Pins 4 and 5. This oscillator is internally connected to a line-drive amplifier which drives an external class AB amplifier consisting of a power NPN and PNP transistor. The line drive amplifier is turned off and on by the presence of a logic "0" or logic "1" level appearing at the transmit input, Pin 19. This results in the ASK encoding; digital information is transmitted via the presence or absence of the carrier frequency. $R_{FEEDBACK}$ is used to improve harmonic distortion; R_{DRIVE} is matched to the anticipated average load. The high-frequency carrier is transmitted to the transformer for induction to the power line.

Some additional features of the demonstration board are.

JMPR-Standby Defeat

This jumper, when connected, inhibits the NE5050 from going into "standby mode". As a power-saving feature, the NE5050's output transistor (driving Pin 11) will deactivate after approximately 4 seconds of no-data traffic (go into "standby") This will result in a logic "1" level at the open-collector output, Pin 11 By closing this jumper, this feature will be defeated by introducing a DC voltage at Pin 9.

JMPR-RCV Suppress (Receiver Suppress)

This jumper, when connected, will force Pin 11 to a Low state during transmission of a logic "1" level This feature is provided to prevent "echoes" of transmitted messages from feeding back to the receiver. This can occur because of the time delay of transmitted signals traveling back through the receiver filters (primarily the impulse filter). In multiple transceiver networks, this echo may be undesirable because it can simulate the presence of another transmitter on the line during the short duration between the end of a transmission and the presence of the "echo". Because collision (and hence arbitration) can only occur during the transmission of a logic "0" (absence of carrier) condition, suppressing the receiver will not eliminate any useful information regarding the line status. Note that closing this jumper will result in a low state at the output (Pin 11) during transmissions of a logic "1".

Inputs/Outputs

Inputs to the NE5050 demonstration board consist of a V_{LOGIC} input, and a XMIT input. The V_{LOGIC} input is simply the voltage level that will appear at the output pin (marked REC) during a logic "1" condition. For most TTL interfaces, this will be + 5V. This is to be externally applied A DC power supply of + 12 to + 18V is required to power the board.

The XMIT input is a TTL-level input which either activates or deactivates the line-drive amplifier which drives the power line (or selected medium) with a carrier. A logic "1" will activate the transmitter, resulting in a presence-of-carrier condition. A logic "0" will deactivate the transmitter resulting in an absence-of-carrier. Be sure that the levels are TTL and have a common ground with the demo board.

Outputs of the demo board consist of a REC OC (Receive, Open-Collector), a REC (Receive), and an LED visual output. The REC OC is an inverted, open-collector output, appropriate for interfaces requiring an inverted logic, open-collector output (such as GE's HOMENET). REC is a positive logic output which will provide output voltage levels according to the V_{LOGIC} voltage level which is externally applied. The LED provides an inverted-logic visual indicator, activated during the presence of a "0" at the output, and turned off during the presence of a "1".

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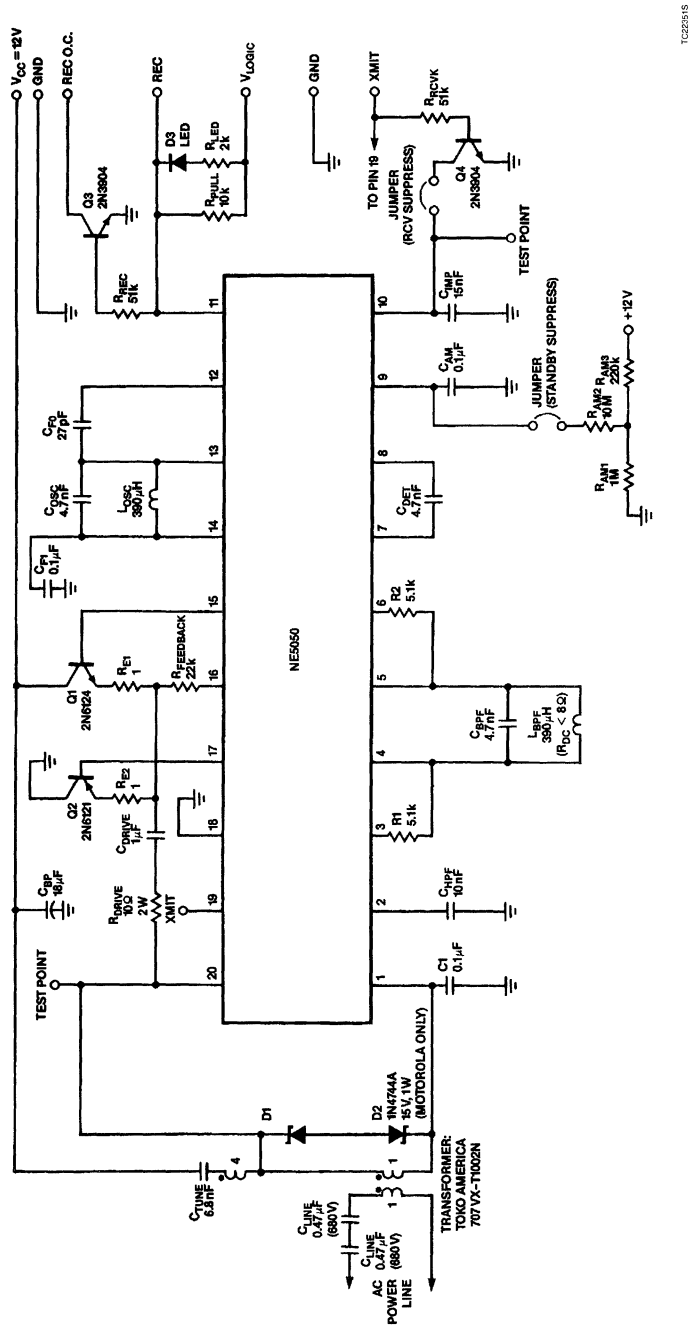

Figure 5. NE5050 Demonstration Board Schematic

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Transient Protection

The latest revision of the NE5050 demo board incorporates two back-to-back zener diodes (Motorola 1N4744A) which provide 15V overvoltage protection for the NE5050. The NE5050 has been designed to endure ± 35V transients, but for additional protection during worst-case conditions (such as the sudden discharge of the line capacitor by shorting the prongs of the plug), these devices have been added. The diodes are connected between Pins 1 and 20 of the IC. Other devices may be used instead (such as surge protectors), as long as they are fast enough to prevent fast-rising high voltage impulses from reaching plus or minus 35V.

120/240V_{AC} Compatibility

This incorporates two series line capacitors, each rated for 680V. This makes the new demo boards compatible with both 120 and 240V_{AC} power line.

BENCH TUNING AND TESTING

Testing and tuning of the NE5050 demonstration boards can be accomplished safely without plugging the boards into the power line. This test procedure is, therefore, done in the absence of the line voltage. Note that the boards are configured to a receiver threshold of 20mV peak-to-peak, with an impulse rejection time of approximately 570μs. The carrier frequency has been set to 118kHz (± 10% due to component variations).

Receiver Testing:

1. Make sure to ground the XMIT input to deactivate the local oscillator.
2. Apply V_{CC} = 12V at the input pin marked "V_{CC}", and 0V at "GND".
3. Measure V_{CC} = 12V at Pins 1 and 20.
4. Make sure the voltage at Pin 3 equals the voltage at Pin 6.
5. With an external frequency source (either another NE5050 demonstration board or a generator), create a 100kHz carrier frequency modulated with a 500Hz envelope (see Figure 6a).
6. Apply this ASK signal to the plug-input of the demonstration board.
7. View this signal with an oscilloscope at Pin 3 or 6. It should appear as illustrated in Figure 6b.
8. Next, view the signal after the band-pass filter, at Pin 4 or 5. It will appear as is shown in Figure 6c.
9. While viewing the ASK signal at Pin 4, adjust the frequency of the source until a maximum amplitude is observed. This should occur at near 118kHz. (See Figure 6d.)
10. Further maximize the carrier amplitude by tuning the core of the Toko transformer with a small screwdriver (See Figure 6e)
11. Next, probe Pins 7 and 8, the detector output. It will look like Figure 6f.
12. Next, look at how the impulse filter affects the output signal This is done by probing Pin 10. You will see a trapezoidal trace with ramps of duration of about 570μs. This rise time is determined by C_{IMP} at Pin 10.
13. The Pin 10 signals are photographed in Figure 6g.
14. Apply at V_{LOGIC} a $5V_{DC}$ supply. View the recovered TTL level square wave at the output marked REC (Figure 6h) Note that any pulse of less than about 570μs will be removed by the impulse filter.

Transmitter Testing:

- Power the board and test as covered above (see Figure 6i)
- Connect a 10Ω, 2W resistor to simulate a load across the plug
- Apply a 500Hz TTL-level square-wave to the pin marked "XMIT"
- The corresponding ASK signal will appear across the 10Ω load at the plug
- Disconnect the resistor and the amplitude should double
- Tune the transformer core to obtain maximum signal amplitude at the plug output

Experiment with the NE5050 board before plugging it into the power line. Here are some additional procedures for observing each section.

Receiver— Turn the transmitter, TX, off by grounding TX_{IN} (Pin 19) If this is not done, the signal coming is the local oscillator. Remove the line coupling transformer and the bandpass filter to permit broadband operation (the filtering action of the transformer with C_{TUNE} is no longer needed). Replace the line coupling transformer secondary with a 50Ω resistor. Connect Pin 20 of the IC to the line coupling capacitor, C_{TUNE}. Inject ASK input signals at the cord prongs from a 50Ω generator. Connect the signal side to one prong and the ground side to the other. Now run the following checks:

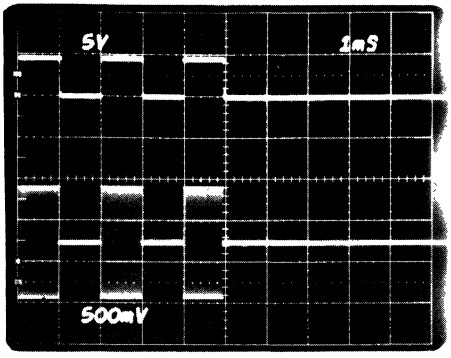
- Sweep the carrier frequency
- Change the carrier amplitude (sensitivity specified to 1.5mV_{RMS} typical, guaranteed minimum 3.5mV_{RMS} over 0 to + 70°C, the consumer temperature range).
- Change the data rate; observe the theoretical maximum: Data rate ratio to carrier frequency (1 Bit/cycle). Note that the data rate is limited directly by the value of the impulse capacitor C_{IMP}.
- Sweep V_{CC} from 12 to 18V
- Remove and replace C_{DET} (AM detector cap) and C_{IMP} (impulse filter cap) and observe RX_{OUT} (Pin 11)
- Decrease C_{LPF} (changing the input high-pass filter characteristics) to 1nF for maximum sensitivity at f_C = 300kHz
- Sweep the carrier frequency from 100Hz to 500kHz
- Increase C_{LPF} to 0.1μF; use low carrier frequencies and low data rates
- Sweep the carrier down to DC
- Decrease the ASK data rate
- Observe the general limitations of the IC modem with the given external components

TRANSMITTER— Replace the 50Ω resistor, R_{DRIVE}, with a 10Ω, ½W resistor. Monitor prongs of cord on the oscilloscope. Similar tests to those done in the receiver can now be done:

- Inject TTL and CMOS data at TX_{IN} (Pin 19)
- Sweep V_{CC}
- Observe the TX output (4V_{P-P} into a 10Ω load, R_L, connected between R_{DRIVE} and ground)
- Open TX_{IN} and observe the THD (total harmonic distortion) of the unmodulated carrier
- Ground TX_{IN} and observe the −90dB carrier suppression at TX_{OUT} and at the prongs
- Check the RX_{OUT} Pin to make sure that it is always receiving what it is sending

Should you have any recommendations or questions in the course of your development, please call Mike Sedayao at (408) 991-4637 or Dan Hanton at (408) 991-4730. We would be glad to assist you.

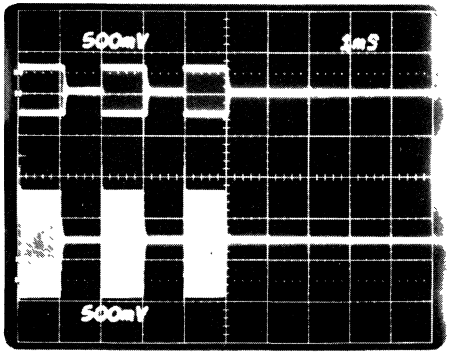
The NE5050 demonstration board kits are available from your local Signetics distributor (order #NE5050 EVN MSC). These kits are for typical power line performance. Each kit contains 2 samples, 2 demonstration boards with samples, and this application note. Each kit has an estimated cost of $266.00.



EXTERNAL 500Hz

EXTERNAL ASK INTO
PCB PLUG (RX INPUT)
f_{CXR} = 100kHz

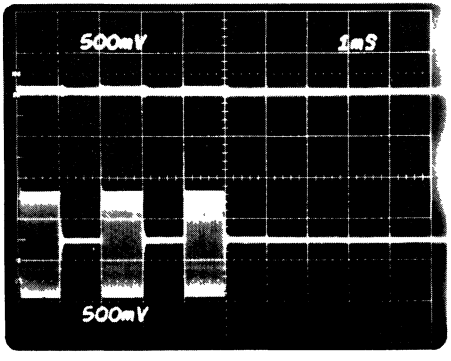
a.



PIN 3 OR PIN 6
(RX AMPLIFIER OUTPUT)

EXTERNAL ASK AT THE
PCB PLUG (RX_{IN})
f_{CXR} = 100kHz

b.



PIN 4 OR PIN 5
(DETECTOR INPUT)

EXTERNAL ASK AT THE
PCB PLUG (RX_{IN})
f_{CXR} = 100kHz

c.

Figure 6. Oscilloscope Plots of NE5050 PCB Bench Testing

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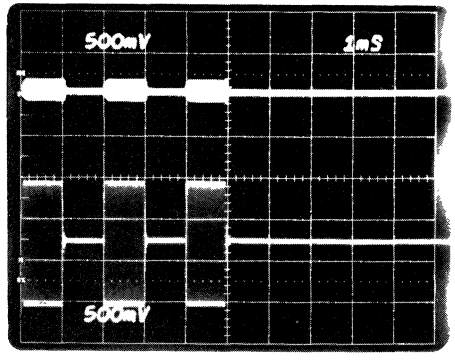
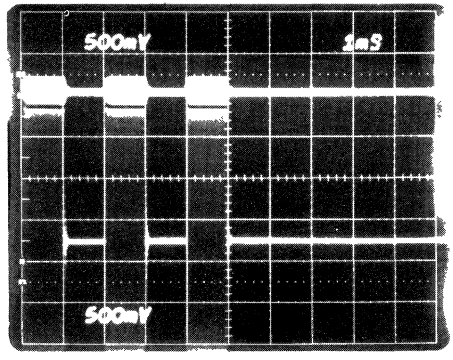


PIN 4
(DETECTOR IN)

RX_{IN}
f_{CXR} = 125kHz

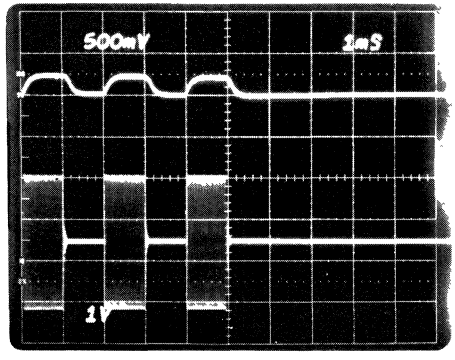
d.



PIN 4
(DETECTOR IN)

RX_{IN}
f_{CXR} = 125kHz
(TRANSFORMER TUNED)

e.

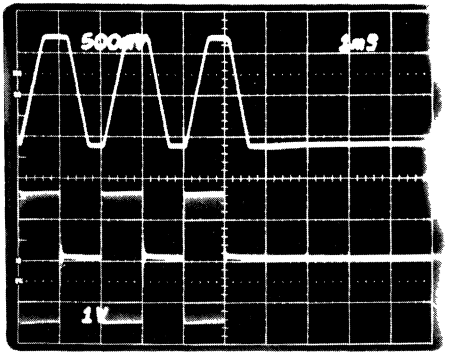


PIN 7 OR PIN 8
(DETECTOR OUTPUT)

RX_{IN}

f.

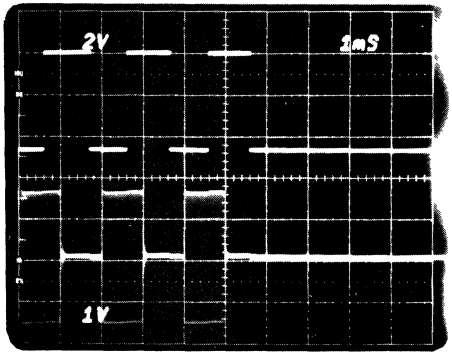
Figure 6. Oscilloscope Plots of NE5050 PCB Bench Testing (Continued)



PIN 10
(IMPULSE FILTER)
DELAY ~ 500μs

RX_{IN}

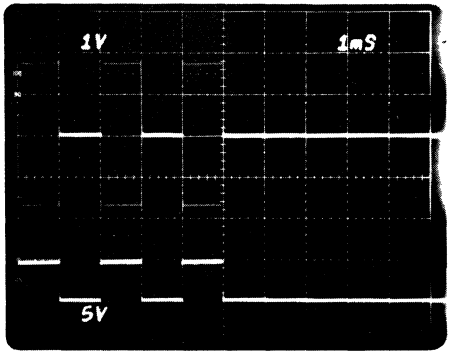
g.



RX_{OUT} "REC"
(PIN 11)

RX_{IN}

h.



PCB PLUG
(ACROSS 10Ω LOAD)

'XMIT' (PIN 19)
(TX_{IN})

i.

Figure 6. Oscilloscope Plots of NE5050 PCB Bench Testing (Continued)

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GUIDE FOR NE5050 CAPACITOR SELECTION

The NE5050 is connected to several external capacitors which must be optimized for different noise environments. Here is how to select the approximate values:

- **C_{LPF}: For rejection of low frequencies**

The input amplifier also provides a fixed high-pass function. The low −3dB point of this filter is given by the equation:

$10^{-3}/C_{LPF}$ [F] = f_{-3dB} [Hz].

This provides a + 20dB/decade response, with a DC attenuation of −50dB. A carrier around 100kHz is boosted by + 24dB. See Figure 2.

- **C_{AM}: AM Rejection Capacitor**

This capacitor must be adjusted as a function of the bit rate (or more precisely, minimum-bit time). Its value should be:

C_{AM} [F] = 10^{-4}/bit rate [bits/sec].

This is to assure proper capture of leading bits in a bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic).

- **C_{DET}: AM Detector Capacitor**

Its value is given by:

C_{DET} [F] = t_{DET} [sec]/10^5; see Figure 4.

t_{DET} is the time it takes for C_{DET} to charge from 0 to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. This delay is a term in a sum of delays, the sum being the total receiver delay, t_D [sec]. See below in "Receiver Delays" the relation between t_D and the maximum bit rate

- **C_{IMP}: Impulse Filter Capacitor**

This capacitor determines the receiver impulse-noise immunity (transmission channel with non-Gaussian noise) This capacitor is determined by the equation:

C_{IMP} [F] = t_{IMP} [sec]/35kΩ [ohm].

t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. The following equation determines t_{IMP}:

Maximum rejected or expected impulse-noise width [sec] < t_{IMP} [sec].

This delay is a term in a sum of delays, the sum being the total receiver delay, t_D [sec]. See 'Receiver Delays' the relation between t_D and the maximum bit rate.

- **Receiver Delays: Maximum bit rate**

The total receiver delay is a sum of delays, where t_{DET} [sec] is the detector delay, t_{IMP} [sec] is the impulse-filter delay, and 2μs is the receiver delay with no C_{DET} and no C_{IMP}:

t_D [sec] = total receiver delay =
t_{DET} [sec] + t_{IMP} [sec] + 2μs

The maximum bit rate, in the no-return-to-zero, amplitude-shift keying data format is determined by:

Maximum bit rate NRZ ASK
[bit/sec] < $1/t_D$ [sec^{-1}]

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall determine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed) For twisted-pair or coaxial cables the calculated values are close to optimal Based on power line applications made at 100Bit/sec and at 50kBit/sec, the C_{IMP}/C_{DET} capacitor ratio ranged from 100 1 to 1 1

Observing AC Line Transmission

To observe full data transmission, reconnect the line-coupling transformer, bandpass filter, and the initial values for capacitors C_{IPF}, C_{IMP}, and C_{AM}.

Take two boards, setting one up as the transmitter and the other as the receiver Supply + 12V to + 15V and ground to each of them. On the receiver, short the TX_{IN} to ground. Attach a pulse generator to the TX_{IN} of the transmitter, remembering to connect the ground of the generator to the ground of the board Review safety precautions before plugging into AC line

Receiver sensitivity is $1mV_{RMS}$. It's recommended to start with about $4V_{P-P}$ to ensure a strong square wave for transmission. To center the bandpass of the transformer to the incoming carrier frequency, adjust the transformer coupling with a jewel head screwdriver.

To monitor the receiver, connect oscilloscope probes to the following circuit points:

- RX_{IN} (Pin 20, AC line signal with noise)
- OUT1 and OUT2 differentially (Pins 3 and 6, RX amplifier output)
- C_{DET1} and C_{DET2} differentially (Pins 7 and 8, AM detector output, the device can also be operated with this capacitor removed. Observe reduction in delay.)
- C_{AMREJ} (Pin 9, AM rejection)
- C_{IMPREJ} (Pin 10, impulse filter; as with the detector capacitor, the device can be operated without this part. There will also be a reduction in the delay.)
- RX_{OUT} (Pin 11, receive data output)

Loud, high power-consuming electrical equipment could be set up nearby to produce in-band disturbances, such as impulses. Also, switch fluorescent lights on and off to see the effect of the transients on the data transmission. To transmit the data, inject TTL signals (CMOS signals are fine because they typically swing from positive to negative rails. TTL thresholds are typically 0.8V for logic 0 and 2.0V for logic 1) into the TX_{IN} (Pin 19) of the other modem located nearby. Make sure that the signals do not go below ground; if they go more than one diode drop below ground, an internal diode turns on and redirects any signal from TX_{IN} into the substrate of the device. So if just injecting a pulse train is desired, choose a pulse generator that has TTL output rather than the symmetrical output that swings both positive and negative. After observing these signals, gradually separate the distance between the TX modem and the RX modem, trying different electrical outlets on the same floor, different floors, and different buildings.

Potential Sources of Interference

There are several sources of signal interference to consider. Among the most important and most likely to occur are the following:

Impulse noise — This form of interference is caused by electrical impulses present on the line. It is present in the baseband and in the frequency interval ($\omega_{CARRIER} \pm 2 \times \omega_{DATA}$) used for data communications. Because the frequency spectrum of a delta (Dirac) impulse is continuous, it would be present in any band. (A delta Dirac impulse is defined to be of infinite amplitude and zero time duration. Thus, its Fourier transform would give it an infinite bandwidth with value unity.)

This translates into a carrier of short duration in the receiver. If data carrier bursts are longer than the impulse bursts, it is possible to filter out narrow data by low-pass filtering (integrating) or by the constant charging and discharging of a capacitor (time domain filtering). Observe the waveform at Pin 10 to see this.

Distributor transformer attenuation — The transformers that separate domestic dwellings or different floors in a factory offer safety features for the people in the buildings, but can also attenuate signals trying to pass through. The maximum attenuation between any two locations within the same house is around 50dB in the 10 − 550kHz range. House-to-house attenuation could be from 10dB for the same distribution transformer to 30dB for separate transformers.

In residential areas, the power line network should not extend beyond the building. High-frequency blocking may be necessary to implement this separation Consult the EIA (Electrical Industries Association) for up-to-

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date information on how to implement the blocking. The consensus is that the blocking should be done at the electric power meter

CW (Continuous Wave) interference — This type of interference is usually caused by tones present on the AC line. They can be generated by mercury-vapor fluorescent lamps. If in the frequency band of the receiver, they may affect the received data and can cause bit errors. The CW interference has spectral components at multiples of 60kHz. It is amplitude-modulated by a 120Hz envelope.

Line impedance modulation — The impedance of the AC power line varies according to the number and power consumption requirements of the various equipment connected to the line. 120Hz impedance modulation also occurs as a result of rectification at 60Hz. Different conditions exist, of course, for the residential and the industrial environments.

The effect of the impedance modulation is best illustrated by observing the waveforms on Pins 7 and 8 (AM detection) and on Pin 9 (AM rejection). The data signal varies in amplitude because of the varying impedance on the line. The AM rejection circuit forces the comparator to track the DC average of the demodulated data and keeps the comparator from changing states This can be envisioned as a 50mV "window" (comparator threshold) "surfing" on the input waveform

A good example of the kinds of noise on the power line and how the NE5050 eliminates them is shown in Figure 5.

The top trace shows the signal at Pin 20, RX_{IN}. The signal has already come from the line, and gone through the line capacitor and coupling transformer. If the trace is followed from left to right, three squares over show the effects of Continuous Wave interference. These signals start to produce an amplitude variation where the signal should clearly be cut off. It also starts to distort the logic 1-to-0 and 0-to-1 transitions. At about the seventh block, the effects of impedance modulation

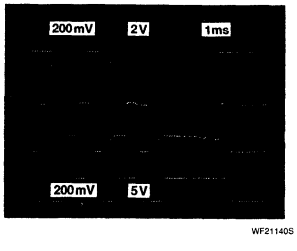


Figure 7. Oscilloscope Traces of RX_{IN}, Output of Bandpass Filter, Impulse Rejection, and RX_{OUT}

on the signal can be seen. What should clearly be a square-shaped signal is now distorted into jagged edges of increasing magnitude

The second trace is the output of the single-pole bandpass filter and the input of the AM detector (Pins 4 and 5) After RX_{IN}, the signal was amplified and then filtered before coming out of Pins 3 and 6 and going into the bandpass filter. At the end of the signal there is some ringing, and in the third block the effects of the impedance modulation still show slight amplitude variations.

Trace three shows the output of the slicing comparator at the impulse rejection range. The slope of the signal is directly related to C_{IMP} At this point the signal has now gone through the AM detector and the AM rejector AM rejection was successful since the impedance modulation effects do not show up on the third block.

The bottom trace shows the output, RX_{OUT}, at Pin 11. Resistor R_{PULL} connects Pin 11 to the logic High voltage. This signal is a square wave, just the output of the flip-flop that was fed internally by the comparator. Comparing the top and bottom traces, a delay is evident This is caused by the charging of the AM detection and the impulse rejection capacitors.

Troubleshooting Board Problems

Because all components, discrete or integrated, are not exactly the same, always expect to see a difference in performance as different components are used Not every application board is the same in the sense that the frequency, filter Q, transmitted power, etc., vary ± 10%; otherwise, they are all fully functional. To help solve eventual problems, a list of cures has been accumulated for different situations. Short of doing a pin-for-pin, part-for-part test, these are some of the things that can be done to get the system running prior to identifying the specific problem.

Assuming that the setup is configured in the send/receive mode and connected to the power line, there are three possible solutions to use to get the signal through.

Increase power supply — Bringing the power supply of the part to about +15V may reduce the total harmonic distortion (THD) of the transmitter if the driver swings more than $8V_{P-P}$. For higher voltage swing, increase $R_{FEEDBACK}$ for lower negative feedback. This also increases the swing of the voltage output of the transmitter. Sending out a larger signal over the power lines increases the signal-to-noise ratio.

[To operate the board at supply voltages in excess of +15V (but not beyond +18V), connect an 82kΩ resistor between Pin 1 (V_{CC}) and Pin 15 (feedback) to create a DC bias at this point so that the upper drive transistor will not break down. This is a process limitation.]

Reducing or shorting output resistor R_{DRIVE} — This 10Ω resistor drops the transmit voltage by a little Reducing or bypassing this resistor increases the voltage sent over the AC lines. The overall effect is similar to solution #1.

Bypassing the bandpass filter — Although this is usually done only in wideband applications, it is possible that the loss of signal occurs because the signal is being filtered out That may occur because of BPF or oscillator component skew. The carrier may be filtered out instead of the noise. In removing the BPF, more noise is introduced because of the wider frequency band, but, once the signal is identified, the BPF can be reconfigured to pass the carrier frequency in the center of its bandwidth.

NE5050 DEMONSTRATION BOARD ADJUSTMENTS

5

Summary

The demonstration board comes configured in a particular mode of operation (i.e., carrier frequency, filter parameters, impulse filtering, etc.) but is easily modifiable. BE SURE TO DISCONNECT THE BOARD FROM THE POWER LINE AND DISCHARGE THE LINE CAPACITORS BEFORE REMOVING THE BACKING OR CHANGING COMPONENTS. Here are some basic adjustments that can be made:

1. Carrier Frequency
   Both transmitter and receiver are tuned to approximately 118kHz. This may be altered by changing C_{BPF}, L_{BPF}, C_{OSC}, and L_{OSC}. Center frequency is determined by the equation $f(Hertz) = 1/[2*pi*\{(LC)^{1/2}\}]$.
2. Impulse Filter
   The impulse filter consists of a capacitor tied to Pin 10. This capacitor results in a rejection of impulses (short-duration, high-bandwidth noise) that can appear after the bandpass filter. This filter will ignore short pulses of duration determined by the equation Impulse Rejection Time (in seconds) = 38k $*C_{IMP}$. The demonstration board comes with a 15nF impulse capacitor, resulting in an impulse rejection time of 570μs. This means that any pulse or state-change that is shorter than 570μs will be ignored by the IC. This impulse rejection time may be changed by altering this capacitor value. Note that the value of this capacitor subsequently places a ceiling on the maximum baud rate by placing a minimum allowable time for symbol encoding.

3. Input High-Pass Filter
   The input stage of the NE5050 consists of a gain/high-pass filter stage. The transfer function of this filter can be modified by changing the value of the capacitor at Pin 2. See Figure 3 for this filter's characteristics.
4. Receiver Bandpass Filter
   The receiver bandpass filter consists of a differential single-pole LC stage connected to Pins 3, 4, 5, and 6. The center frequency is given in Part 1 above The sharpness of this filter is determined by the value of the R1 and R2. By increasing the value of these resistors, we may increase the filter Q (which also increases insertion loss). Figure 8 shows some typical performance curves of this filter with different values of resistors.
5. The demonstration board is designed to deliver maximum power into a 10Ω load. This may be changed by simply matching the value of R_{DRIVE} to the equivalent impedance of the transmission medium. Be sure to use at least a 2W resistor.
6. Transformer Tuning
   The Toko transformer provided has an adjustable core which should be tuned to provide minimum carrier attenuation at the desired carrier frequency This can be accomplished by observing the envelope of a continuous carrier (generated by another transmitter and applied through the power line side of the transformer) and turning the core to a point of maximum carrier amplitude.

The value for C_{TUNE}, 6.8nF, was found to be the best tuning possible for the secondary of the TOKO transformer. One could also try to tune the primary of the transformer.

The TOKO transformer is not recommended in networks with a large number of nodes, and is not recommended for high bit rates, for two reasons:

a) In the receive mode the NE5050 IC input impedance is 9kΩ at the carrier frequency (Pin 20). The TOKO transformer lowers the receive-mode input impedance of the printed circuit board to 200Ω This is OK for few nodes. This TOKO transformer design does not facilitate the use of many nodes in a single network. A possible substitute transformer is the AIE Magnetics transformer which has 2kΩ at the carrier frequency

b) The TOKO transformer has limited capability for high-speed data transmission rates (to 10kbit/sec) while the AIE transformer enables data rates in excess of 100kbit/sec. The AIE transformer is broadband and does not require tuning.

7. Transient Protection
   Note that no guaranties are given regarding the breakdown voltage of either transformer For transient protection, the user is directed to the following standard:

IEEE Standard 587 (ANSI C62.41 - 1981)
Condition:
Long Branch Circuits — 0.5μs - 100kHz oscillatory wave 6kV.
Short Branch Circuits — 1.2 × 50μs impulse wave 6kV.

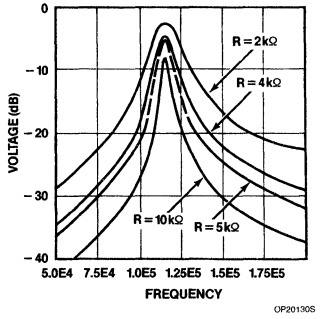


Figure 8. Typical Response for One-Pole BPF and Different Resistor Values

LAYOUT OF BOARD

Shown in Figure 9 is a copy of the layout Imagine looking from the top and actually seeing "through" the board to the metallization layer (solder side) Look on the back and the pattern will be reversed. This has been done so that the engineer may look at the components on top (component side) and see how they are interconnected on the back side (solder side).

List of External Components

These component values reflect the NE5050 demonstration board which has been designed for 118kHz operation into a line impedance of 10Ω.

Component	Value
Capacitors	
C_{LINE}	0.47μF/680V (2)
C_{TUNE}	6.8nF
C_{PS}	10uF
C_{DRIVE}	1μF
C_1	0 1μF
C_{LPF}	10nF
C_{BPF}	4.7nF
C_{OSC}	4.7nF
C_{DET}	4.7nF
C_{F0}	27pF
C_{F1}	.1μF
C_{AM}	1μF
C_{IMP}	15nF
Resistors	
R_{DRIVE}	10Ω/2W
R_1	5.1kΩ
R_2	5.1kΩ
R_{E2}	1Ω
R_{E1}	1Ω
$R_{FEEDBACK}$	22kΩ
R_{AM1}	1MΩ
R_{AM2}	20MΩ
R_{AM3}	220kΩ
R_{OC}	51kΩ
R_{PULL}	10kΩ
R_{LED}	2kΩ
R_{RCVS}	51kΩ
Inductors	
L_{OSC}	390μH
L_{BPF}	390μH
Transistors	
Q1	2N6124 (NPN)
Q2	2N6121 (PNP)
Q3	2N3904
Q4	2N3904
Miscellaneous	
Transformer Toko America* #707VX - T1002N Diodes: Motorola 1N4744A 1 LED	

*Toko America, Inc
5520 West Touhy Avenue
Skokie, IL 60077
(312) 677-3640
In California (408) 996-7575

AIE Magnetics
A Division of Vernitron Corporation
701 Murfreesboro Road
Nashville, TN 37210
(615) 244-9024

Advance Transformer Company
2950 Northwestern Avenue
Chicago, IL 60618
(312) 267-8100

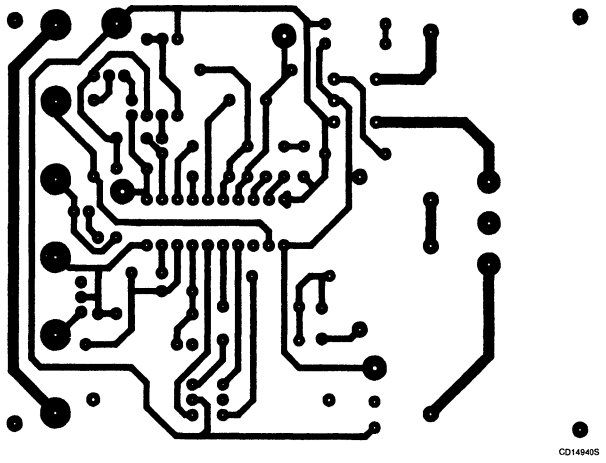
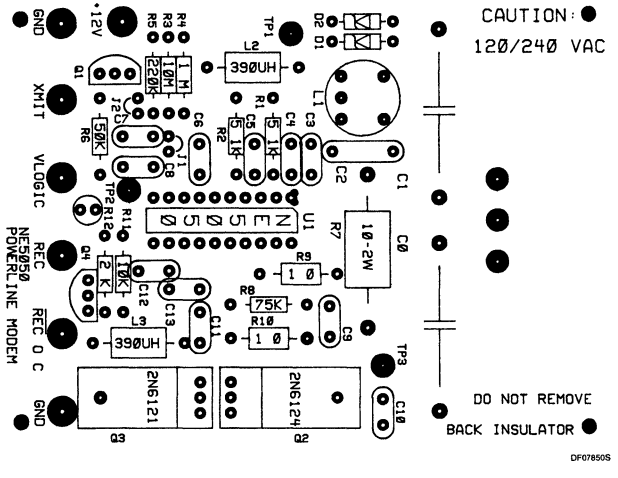


Figure 9. Layout of Application Board



*J1 JMPR – Standby suppress
J2. JMPR – Receive suppress

Figure 10. Component Reference on Layout of Board (Top View)

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HIGH-PERFORMANCE INDUSTRIAL APPLICATION

In a hostile environment, the carrier frequency and filtering scheme must be judiciously chosen. This is usually done over the frequency domain and after a thorough characterization of the environment it is designed for. The carrier frequency is then chosen to be in the range of least interference. To ensure the suppression of out-of-band signals, whether it is noise or other carrier frequencies (for a multicarrier system, see the Multicarrier Operation section), a high Q filter with large stopband suppression is desirable. This suggests the use of multipole passive filters or active filters. The problem in using multipole passive filters is that the passive elements tend to overattenuate the signal.

The configuration shown in Figure 7 illustrates one alternative to the single-pole filter given in the normal 100kHz industrial operation. The problem presented was that certain fluorescent light bulbs added significant interference to line transmission and caused bit-error-rate problems. The light bulbs produce spectral components at 60 and 120kHz that contribute to impedance modulation effects in that range. With a carrier near 100kHz, the single-pole passive bandpass filter with its 6dB/octave roll-off did not provide sufficient stopband suppression to get around the spikes at 120kHz. The solution was to move the carrier to a higher frequency (260kHz) beyond the effect of the lights and to select a filter with a much higher Q in order to eliminate as much noise as possible in the spectrum near the carrier.

The outputs of the input amplifier are Pins 3 and 6 which feed into the high-Q ceramic filters. The ones used are Toko 262Cs with a center frequency of 262kHz. These filters have a BW of greater than 8kHz and an insertion loss of 6dB. Given the center frequency and BW, the Q is approximately 32. The outputs of the ceramic filters then feed into the two-pole LC filter on the right part of the diagram. C1, L1, C4, and L2 provide the center frequency.

Resistors R1, R2, R3A, R4A, R5A, R6A, R3, and R4 provide DC biasing to the middle of the supply range, 6V. Resistors R3 and R4 buffer the NE592 Differential Amplifier, and C2 and C3 AC-couple the signal to the second LC tank which is buffered by R7 and R8. The NE592 is used to amplify the signal which has been attenuated by the ceramic filter and the input resistors. The NE592 has an adjustable gain, in this case, the gain (differential) has been set to 200. (This is the middle of the gain range and should be adjusted to give the desired signal.) The output is then sent to the input of the AM detector, Pins 4 and 5.

There are additional changes to be made for the high-performance application. C_{OSC} and L_{OSC} have been changed to 1nF and 390μH to match the change made in the bandpass filter. C_{TUNE} has been changed to 1nF for the same reason. C_{IMP} has been raised to 12nF to provide a suppression of impulses with duration under 450μs.

The filter shown in this example should by no means be taken as the best possible example. It was only tailored for the application and environmental conditions in Signetics' laboratory. Any conventional filter with a differential input and output can be used. In most cases, the cost of external components to the user and the amount of available space on the board will be the limiting factors.

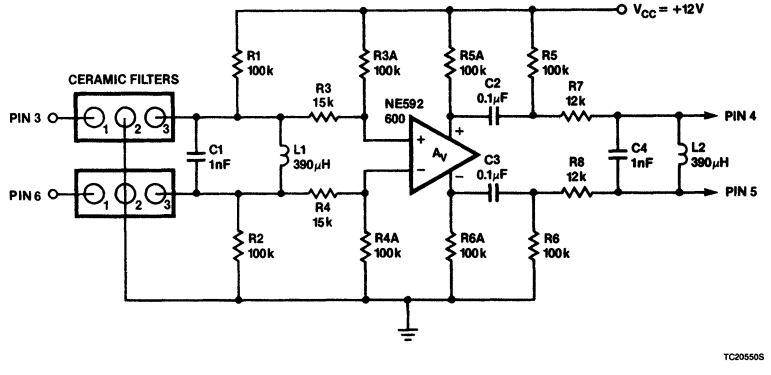

Figure 11. Ceramic Filter with Two-Pole Filter for High-Performance Industrial Operation (F_C = 260kHz)

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OTHER APPLICATIONS

On the following pages are several applications for the NE5050 that demonstrate its flexibility. As mentioned in the disclaimer, these do not denote the maximum performance of the part, they just describe potential applications.

CONSUMER OPERATION

The consumer application is similar to the industrial operation outlined earlier, except that it uses a drive resistor of 50Ω instead of 10Ω. Use the same safety precautions, outlined under Electrical Hazards to the User.

A major difference between this application and that of the industrial environment is the lack of external drive transistors for the transmitter.

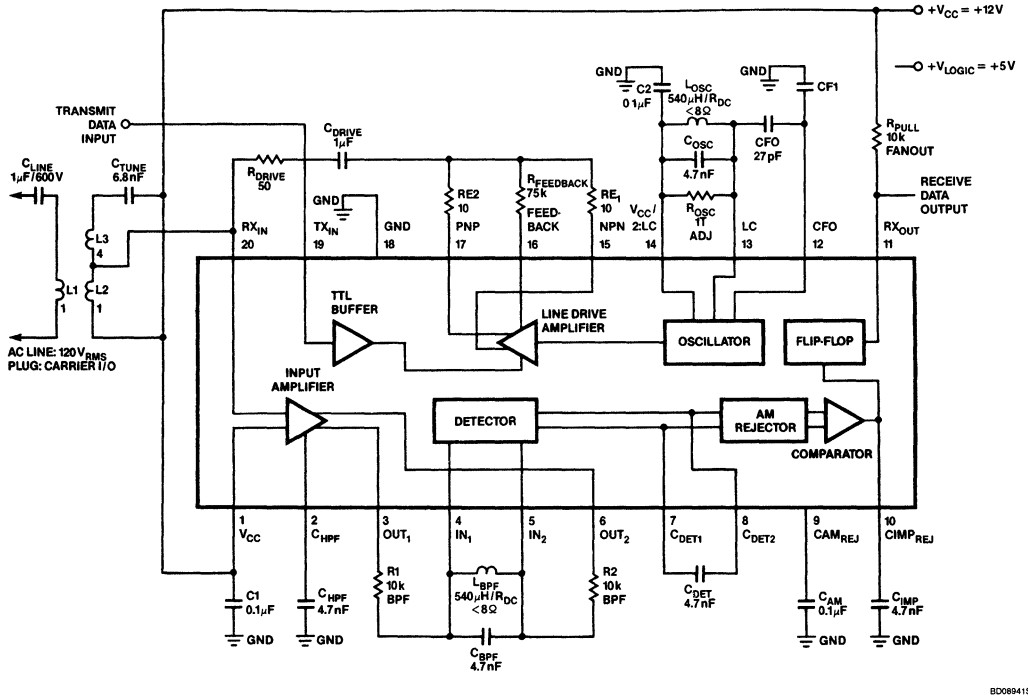

Figure 12. 100kHz Consumer Operation

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SPLIT-SECONDARY OPERATION

This operation is similar to the industrial operation except that the transmitted signal is sent on a separate secondary winding. Note that the turns ratios are 10:40 for the received signal. The turns ratio for the transmitted signal back to the line is 1:10. For this application, the transmitted input is not being received back into the device, so collision detection is not used. This is to be expected since TX_{OUT} and RX_{IN} are transmitted and received on different secondaries.

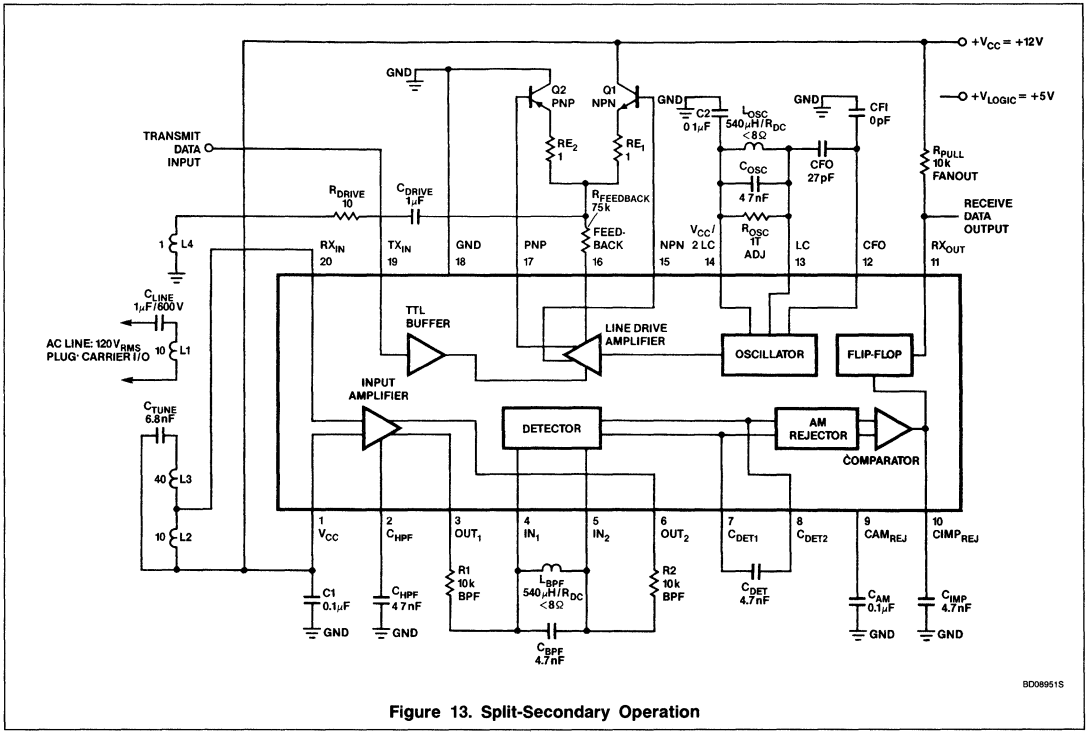

Figure 13. Split-Secondary Operation

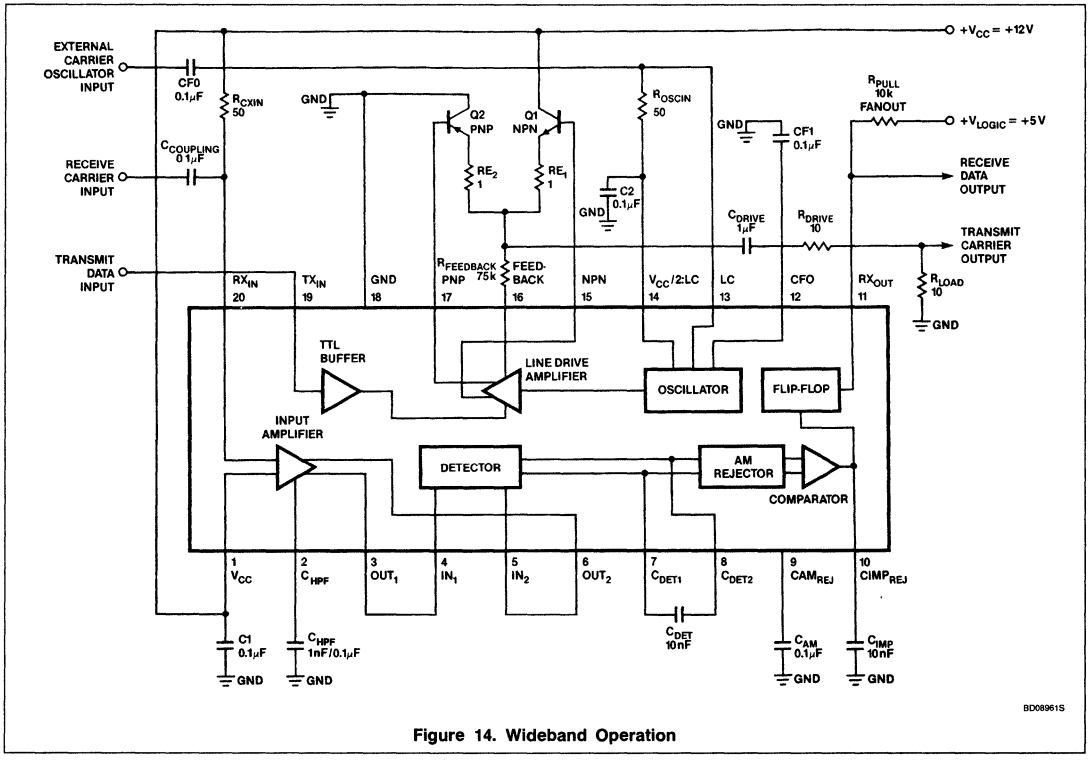

Figure 14. Wideband Operation

WIDEBAND OPERATION

For wideband operation, note in Figure 10 that the bandpass filter is not utilized and the output of the input amplifier is shorted directly to the AM detector to permit all frequencies to pass through. Also note the absence of any transformer coils. The receive input and the transmit output are just AC-coupled to their respective sources and destinations. The external carrier oscillator input is AC-coupled directly to Pin 13 to the LC tank input. It goes through a 50Ω resistor to Pin 14. Pin 12 has a capacitor to ground to prevent the Colpitts oscillator from building up oscillations itself.

This application is ideal for testing the frequency response of the receiver and transmitter. For single frequencies, the 50Ω resistor between Pin 13 and Pin 14 can be replaced with a tuned LC tank circuit.

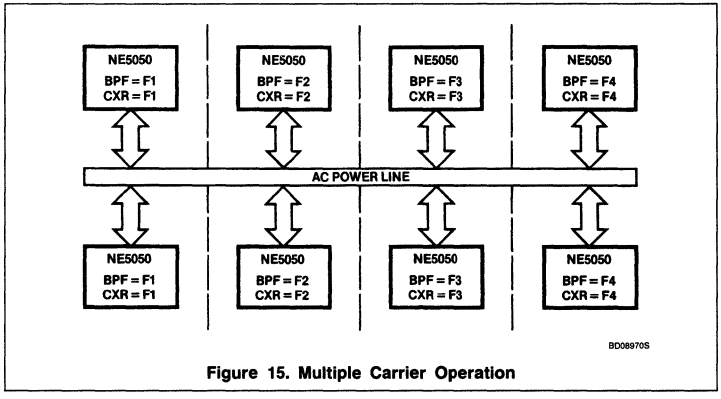

Figure 15. Multiple Carrier Operation

MULTICARRIER OPERATION

This application enables use of multiple points on the network without interference from adjacent transceivers using the same medium. Set up the boards as in the consumer or industrial applications, but use different values for the carrier frequency and the bandpass filter. It is suggested that each carrier be separated as much as possible over the working range of the NE5050. The frequencies should not be multiple integers of each other. This ensures that any harmonics will be suppressed far enough not to interfere with other carriers in the spectrum of operation.

In this type of application, the stopband suppression of the bandpass filters plays a large role in the efficiency of carrier transmission, so active filters should be considered.

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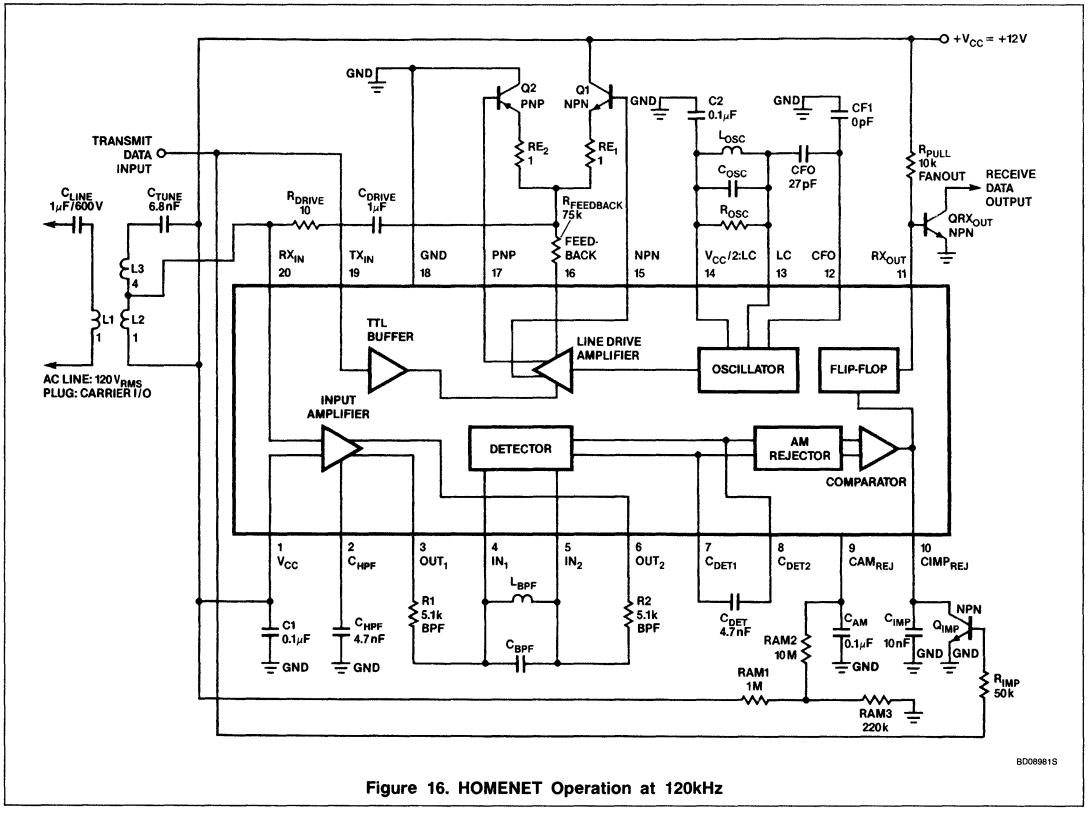

Figure 16. HOMENET Operation at 120kHz

GENERAL ELECTRIC'S HOMENET OPERATION[1]

HOMENET is a software package copyrighted by General Electric Company for the purposes of power line and twisted-pair communication in a residential environment. The software package is called the HOMENET Link Layer and is compatible with the X-10 Home Control System manufactured by BSR and GE.

A working diagram is shown in Figure 12. Technical highlights are as follows:

1. The receiver is disabled while in the transmit mode. This is done by having the transmit input drive an NPN transistor. When turned on, it discharges the impulse capacitor and pulls the comparator output Low (Pin 10). The flip-flop cannot change state. When the data is Low, the oscillator is suppressed and no carrier is detected.
2. HOMENET wants the signal inverted and with an open collector so the user can pick the logic voltage for the receive output (typically +5V).
3. In order to prevent the receive output from going into the standby mode (typically 4 seconds after a TX_{IN} 1-to-0 transition, the RX_{OUT} pin will drift High), the AM rejection pin is externally biased to 2.2V DC with the resistors shown to prevent the comparator from triggering.

NOTE:

1 The HOMENET Link Layer is available as a software package with the Commodore 64 Personal Computer. Current version number available by contacting. The Industry Standards Staff, General Electric Corporation, Fairfield, CT 06431

TWISTED-PAIR APPLICATIONS

Data transmission over twisted-pair cable enables much higher data rates because the media is usually free of the noise and impedance modulation problems of the power line. Transmission over longer distances is also possible. Many of the same reasons can be applied to coaxial cable. The NE5050 provides an easy interface for twisted-pair operation.

Figure 13 shows the characteristics of the cable used Four rolls of cable were used. Each roll had over a kilometer of cable which was linked together to create about 15,000 feet of media. The operation is straightforward and is shown in the schematic in Figure 14

This version has no external drive transistors and has no drive resistor. The receive input comes directly from the end of the secondary (no tuning capacitor); the tap is left unconnected. The other end of the secondary is biased to the power supply. The transformer made by AIE Magnetics connects itself to the twisted-pair wire. The center tap is grounded to the shield of the cable. Only a single-pole filter is used. The AIE transformer was chosen because it enabled the high transmission rates.

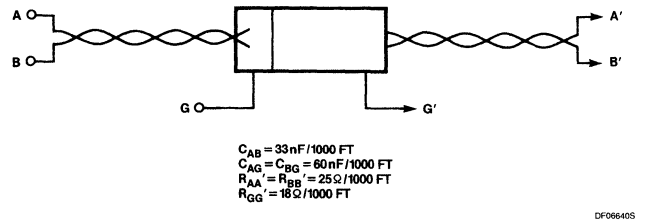

Figure 17. Parameters of Shielded Twisted-Pair Cable

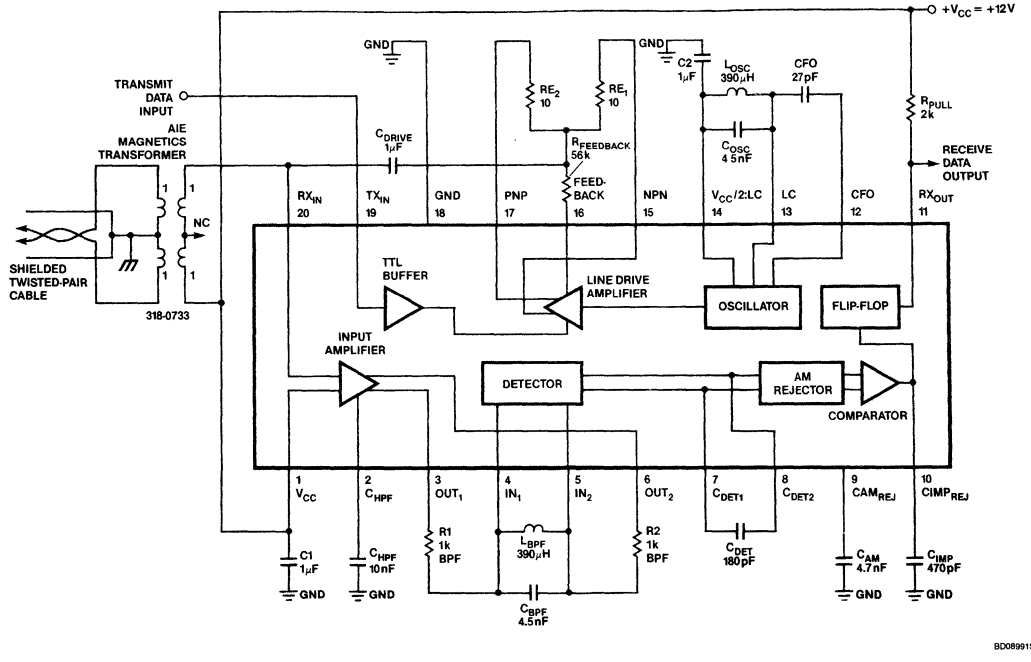

Figure 18. Twisted-Pair Operation: 15,000ft Unequalized Cable at 20kBits/sec

Faster transmission is possible if the cable lengths are shortened. As a rule of thumb, shortening the cable enables a doubling of the transmission rates provided it doesn't exceed the part's (or the transformer's) broadband limitations. Remember, when changing the data rate, C_{AM} has to be adjusted accordingly. Because of the less noisy environment, high voltage transients are absent and C_{IMP} plays less of a role in maintaining a lower bit-error-rate. It will, however, keep the rate-limiting effect outlined earlier.

An additional case was performed in the lab incorporating the following changes:

1. Pin 2 has a 10μF capacitor in series with a 2.2kΩ resistor. The resistor was added to reduce the ringing effects on the RX_{IN}, Pin 20, due to the response of components at higher data rates and higher carrier frequencies. The components will cause the parts to ring. (The transformer is a potential source. The IC will not ring unaided.)
2. R1 = R2 = 1kΩ, C_{BPF} = C_{OSC} = 470pF, L_{BPF} = L_{OSC} = 390μH
3. C_{DET} = 68pF
4. C_{AM} = 1 5nF
5. C_{IMP} = 12pF
6. Connect a 10Ω resistor between the ends of the primary of the transformer (AIE Magnetics 318-0733). This resistor shunts the two twisted wires.

Performance under these changes resulted in a 100kbits/sec data rate over 3,000 feet of shielded twisted-pair wire using a carrier frequency of 370kHz.

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Twisted-Pair Cable Operation at 20kbit/sec

The Belden cable used was 2-conductor, 24 gauge, shielded; trade # is 9452. Fifteen spools were connected in series, 1000 feet each. Longer transmission distance can be achieved if the cable is not shielded (less capacitive loss) The cable is unequalized.

Cable measurements:

Conductor-to-conductor capacitance = 33nF/1000 ft.

Conductor resistance = 25Ω/1000 ft., one conductor

Conductor-to-shield capacitance = 62nF/1000 ft.

Shield resistance = 18Ω/1000 ft

The carrier frequency is about 125kHz.
The transmitted bit pattern is 1101 0100 1000 0000.
One bit lasts 50μs; therefore, the NRZ data rate is 20kbit/sec.

In Figure 20A the oscillator in the receiver modem is turned off; this prevents crosstalk to the local receiver (possible crosstalk cause· usage of unshielded inductors). This crosstalk creates a first type of jitter in the receiver. In the transmitter there is synchronization between the data and the carrier zero-crossings. The absence of data-to-carrier synchronization creates a second type of jitter in the receiver. From top to bottom: Trace 1 is the transmitter input data, trace 2 is the carrier signal at the transmitter, trace 3 is the carrier at the receiver input, and trace 4 is the demodulated data at the receiver output.

A D-type edge-triggered flip-flop is used to achieve transmitter data-to-carrier synchronization. In the transmitter, the oscillator carrier from Pin 13 is amplified, shaped, and injected as clock signal into the flip-flop. The data is applied at the D input of the flip-flop. The flip-flop output, Q, is connected to the transmitter data input, Pin 19.

Figure 20b illustrates the effect of the two types of jitter upon received data. The oscillator in the receiver is on, and in the transmitter data is applied directly to Pin 19 (data-to-carrier not synchronized). From top to bottom: Trace 1 is the transmitter input data, trace 2 is the carrier signal at the transmitter, trace 3 is the carrier at the receiver input, and trace 4 is the demodulated data at the receiver output. Notice the jitter present in trace 4.

Figure 20c shows data transmission at 25kbit/sec. From top to bottom: Trace 1 is the transmitter input data, trace 2 is the carrier signal at the transmitter, trace 3 is the carrier at the receiver input, and trace 4 is the demodulated data at the receiver output. Notice the absence of jitter in trace 4.

LINE IMPEDANCE MODULATION

The NE5050 receiver has 40dB of AM rejection. To test this, the NE5050 transmitter can be configured to generate 40dB of AM that looks like line impedance modulation. Therefore, an NE5050 can be used to test itself (see Figure 4).

The following are oscilloscope plots of receiver waveforms which demonstrate the effect of impedance modulation on the carrier.

Notice in photographs Figures 20B and C that the AM occurs in the middle of the pulse.

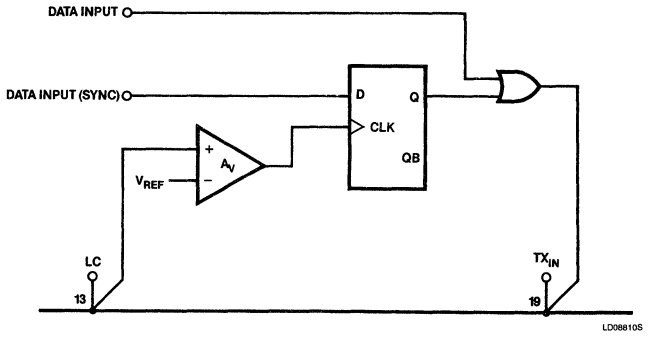
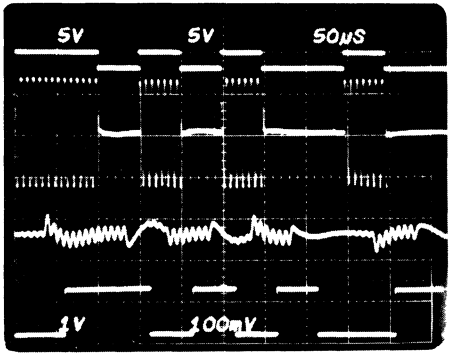
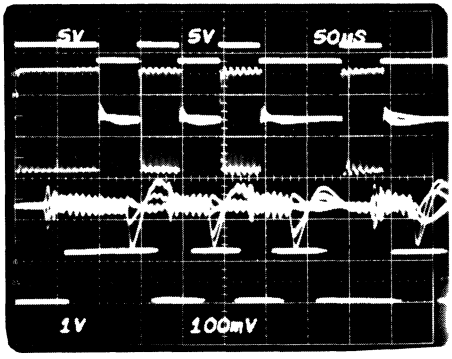


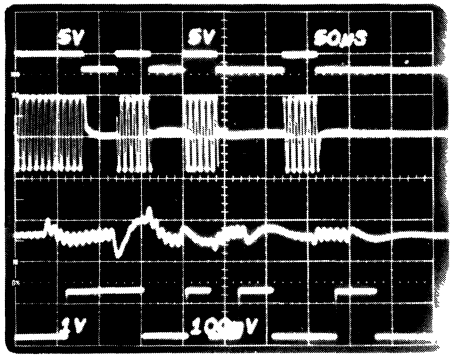
Figure 19. NE5050 Transmitter Data-to-Carrier Synchronization



a.



b.



c.

Figure 20. Twisted-Pair

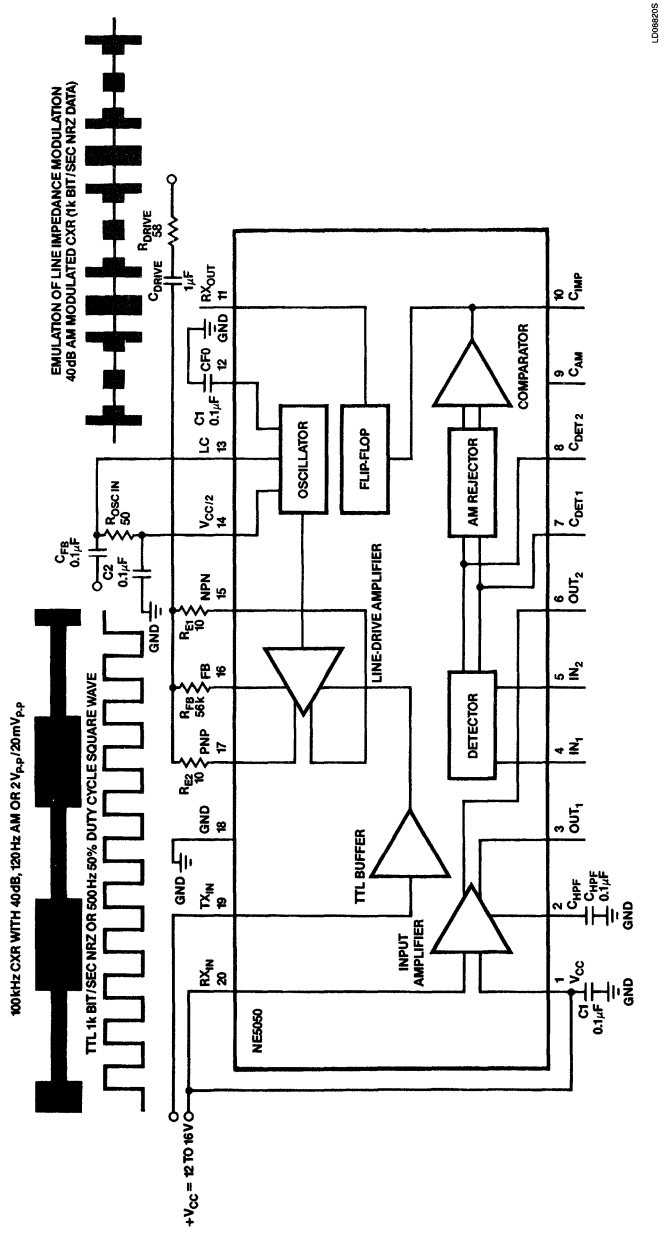
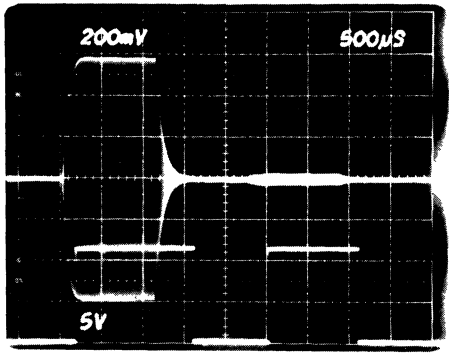
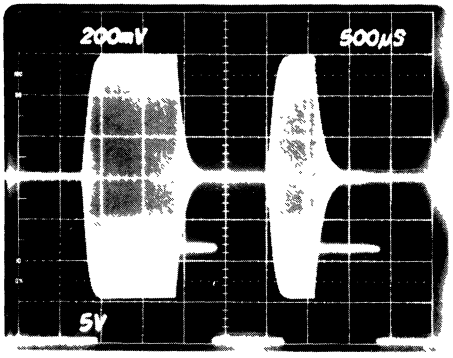


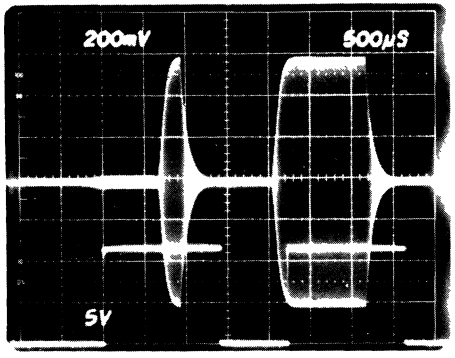
Figure 21. NE5050 Emulation of AC Line Impedance Modulation



a.

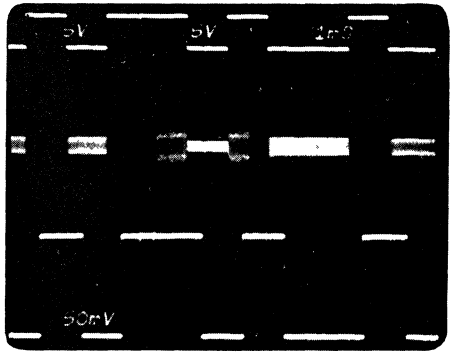


b.



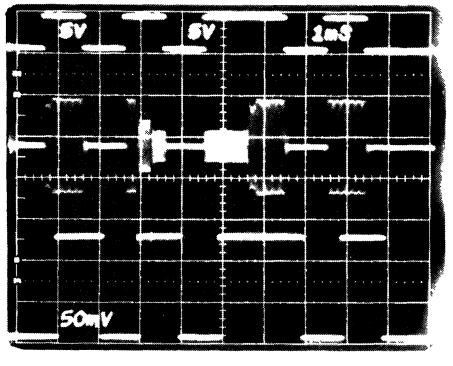
c.

Figure 22. Receiver AM Rejection: General Aspect



OUT-OF-BAND CW INTERFERENCE FROM THE RADIO SHACK POWER LINE TELEPHONE SET

d.



VISIBLE LINE IMPEDANCE MODULATION CAUSED BY 2 LIGHT DIMMERS (IMPULSES PRESENT)

e.

Figure 22. Receiver AM Rejection: General Aspect (Continued)

NE5050 at 50kbit/sec NRZ Data Over the 277V_{RMS} Power Line

50kbit/sec NRZ data was transmitted in the laboratory environment over 20 meters, with 277V_{RMS} AC voltage present and the fluorescent ceiling lights on. A first requirement was to reject the 0 to 100kHz frequency band using a high-pass filter. A 1.5V_{P-P} 10kHz, CW interference had to be filtered out. The AIE Magnetics transformer is used.

The carrier frequency is set around 475kHz using the following components, either in series or in parallel: L = 390μH/8Ω and C = 390pF. In parallel to the LC oscillator tank a 20kΩ potentiometer is used to adjust the transmitted amplitude.

The bit width is 20μs and the observed jitter is < 4μs peak-to-peak. The carrier amplitude at the receiver is between 0.75 to 2V_{P-P}

No external transistors were used. For external transistors the following complementary

NPN-PNP pairs can be used:

2N4401 – 2N4403 or 2N4400 – 2N4402.

For transient protection two back-to-back 1N4744 zener diodes were used.

A 1010 1110 0000 0000 repetitive bit pattern was transmitted.

The BPF resistors are 100Ω, C_{DET} = 390pF, C_{AM} = 2200pF, C_{IMP} = 270pF.

Figure 24a illustrates the transmitted bit pattern (top trace) and the line carrier amplitude (bottom trace).

Figure 24b illustrates the received ASK carrier (top) and the demodulated data (bottom).

Figure 24c illustrates received ASK carrier (top) and the jitter increase in the received data (bottom: jitter < 4μs). Additional noise was deliberately added. Notice the drop in carrier amplitude caused by the low impedance of the noise source.

Over the 20 meters a 6dB carrier attenuation was observed.

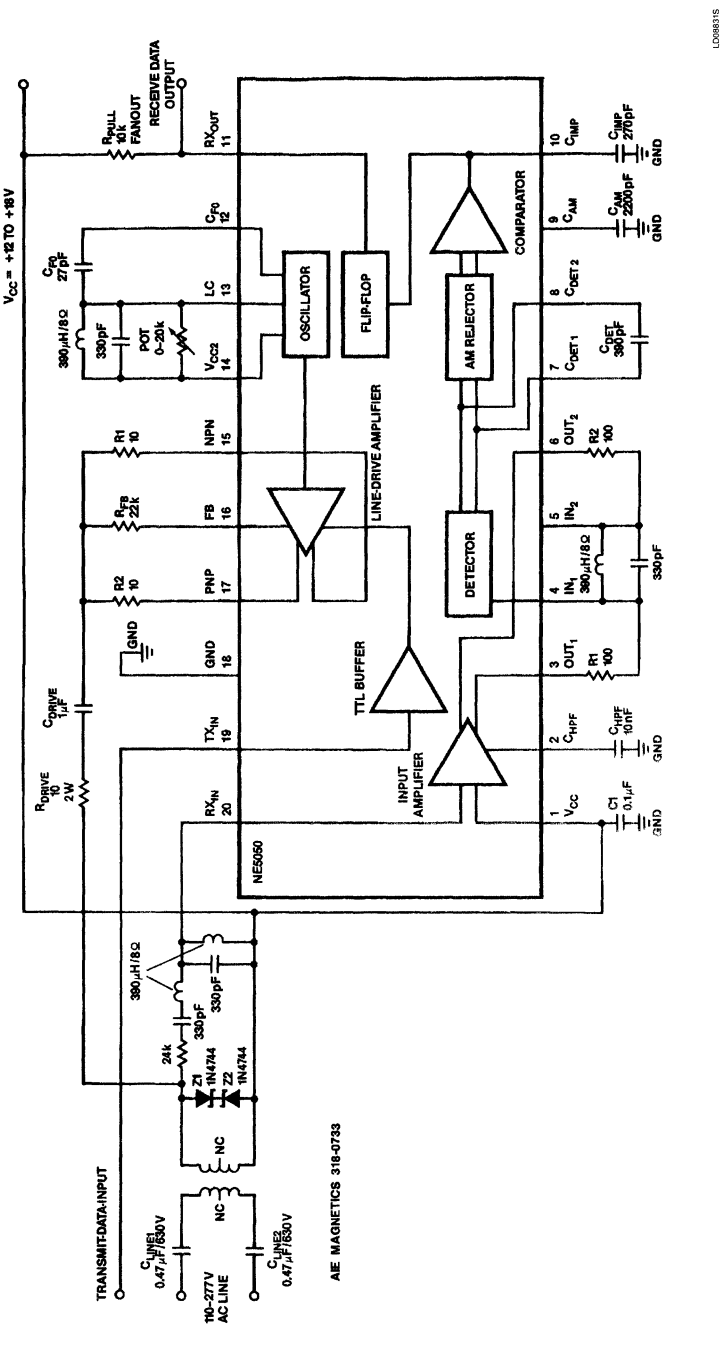


Figure 23. 50kBit/sec on the 277V_{RMS}, Neon Lighting, Ceiling Wires

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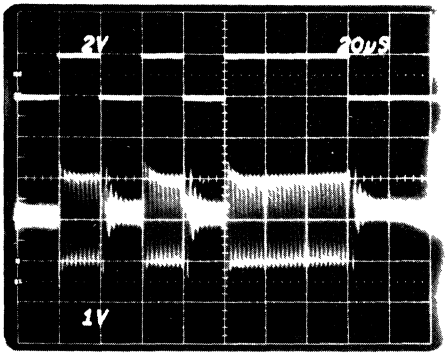
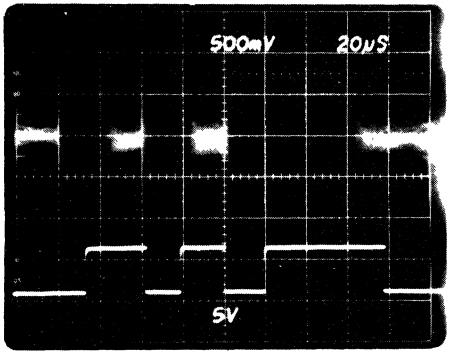
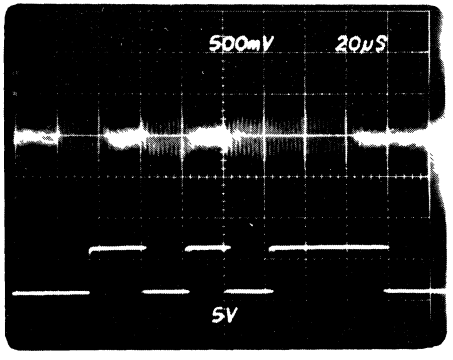


a.



b.



c.

Figure 24. 50kBits/sec

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5

Signetics

NE5080
High-Speed FSK Modem Transmitter

Preliminary Specification

Linear Products

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

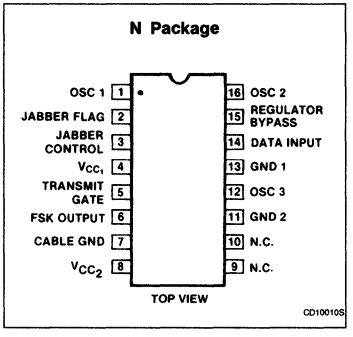
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half- or full-duplex operation**
- **Jabber function on-chip**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

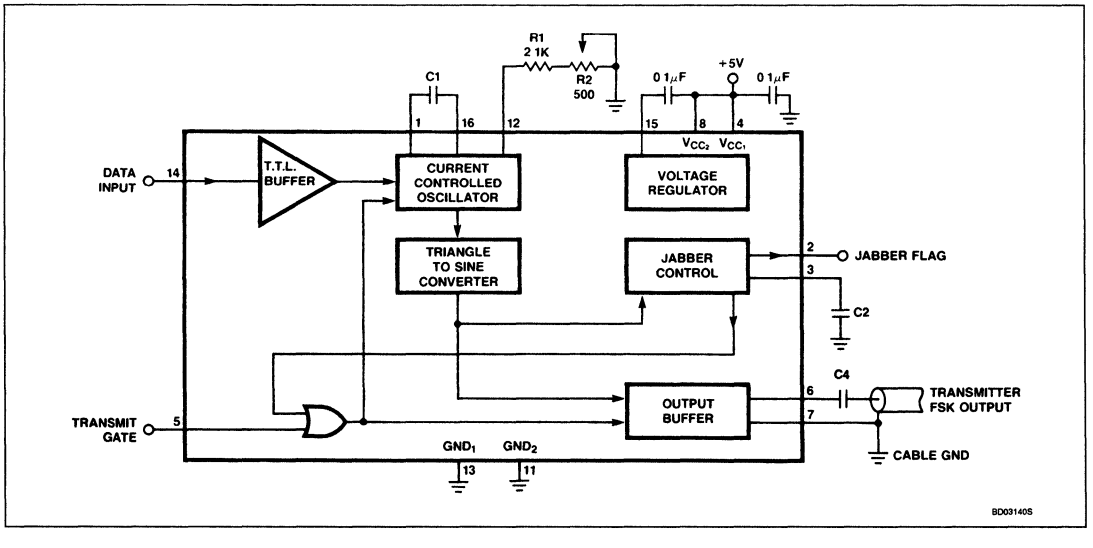
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE5080N

BLOCK DIAGRAM



High-Speed FSK Modem Transmitter — NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:

1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies. See "Determining Component Values."

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	−0.3 to $+V_{CC}$	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to +70	°C
T_J	Max junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

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DC ELECTRICAL CHARACTERISTICS $V_{CC1,\ 2} = 4.75 - 5.25V$, $T_A = 0°C$ to $+70°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_1	Output frequency (Logic high)	Data input $\geq 2.0V$ (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input $\leq 0.8V$ (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input $\geq 2.0V$ or $\leq 0.8V$ Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate $\geq 2.0V$	100			$k\Omega$
R_{ON}	Output impedance (gated on)	Transmit gate $\leq 0.8V$			37.5	Ω
C_O	Output capacitance	Transmit gate $\geq 2.0V$ or $\leq 0.8V$			10	pF
V_F	Feedthrough	Transmit gate $\geq 2.0V$ 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate $\leq 0.8V$ Input $\geq 2.0V$ or $\leq 0.8V$		1.25		μA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Input current	$V_{IN} = 0.4V$			−1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	μA
I_{IL}	Input current	VG = 0.4V			−1.6	mA
	Jabber flag					
V_{OH}	Logic high	$I_{OH} = -400\mu A$	2.4			V
V_{OL}	Logic low	$I_{OL} = 4.0mA$			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		μs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	μs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

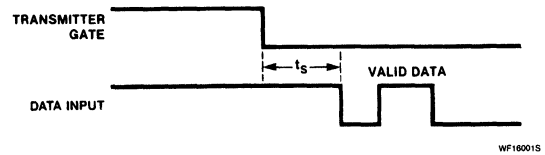

Figure 1. Setup Time, t_S

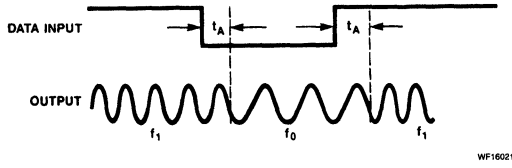

Figure 2. Delay Time, t_A

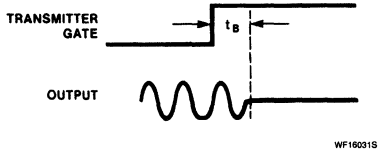

Figure 3. Delay Time, t_B

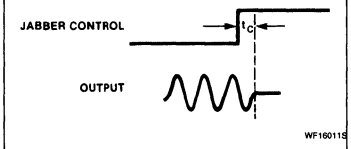

Figure 4. Delay Time, t_C

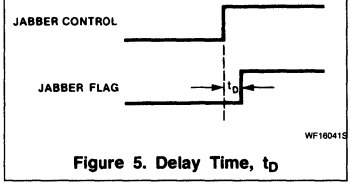

Figure 5. Delay Time, t_D

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Signetics

NE5081
High-Speed FSK Modem Receiver

Preliminary Specification

Linear Products

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies in the 802 standard. However, the receiver will work at other frequencies.

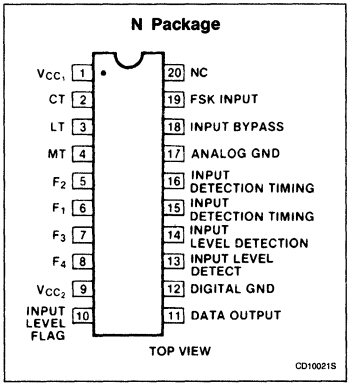
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half- or full-duplex operation**
- **Low bit rate error (10^{-12} typical)**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

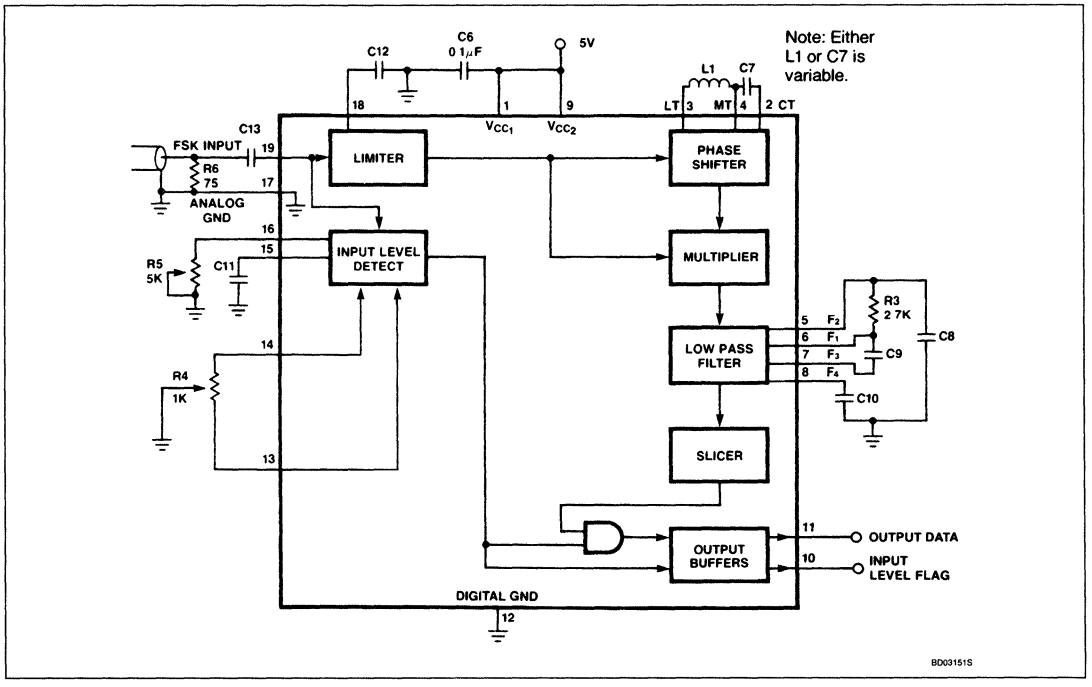
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE5081N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	−0.3 to $+V_{CC}$	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1, 2} = 4.75 - 5.25V$. External LC circuit tuned to 5MHz. Input level detect set at $16mV_{RMS}$, $T_A = 0°C$ +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	$I_{OL} = 4.0mA$ $V_{IN} > 16mV_{RMS}$ Freq = f_0			0.4	V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} > 16mV_{RMS}$ Freq = f_1	2.4			V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} < 5mV_{RMS}$ Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	$I_{OL} = 4.0mA$ $V_{IN} = 0V_{RMS}$			0.4	V
V_{OH}		$I_{OH} = -400\mu A$ $V_{IN} > 16mV$	2.4			V
I_{CC}	Supply Current	$V_{CC} = 5.25V$ (V_{CC1} connected to V_{CC2}) $V_{IN} = 1.0V_{RMS}$ Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > $16mV_{RMS}$ maximum in-band noise = $1.6mV_{RMS}$		10^{-12}	10^{-9}	

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AC ELECTRICAL CHARACTERISTICS (AN195, Figure 5 with a 100KHz 1V_{P-P})

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0 05	1	μs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	μs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	μs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	μs
	Required Delay	Carrier Turn Off	Valid Data End		2			μs

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4 — Token-Passing Single-Channel Phase-Continuous-FSK Bus — (i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from 16mV_{RMS} to 1V_{RMS}. This can be adjusted.[3]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3 75MHz and 6 25MHz See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level This level is adjustable within the range given in the electrical specification section The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV_{RMS}
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change

NE5081 PIN FUNCTION

PIN	FUNCTION
1	**V_{CC1}:** Should be connected to the 5V supply and Pin 9
2	**CT:** One end of an external capacitor that is used to tune the receiver
3	**LT:** One end of an indicator that is used to tune the receiver
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver
5	**F2**
6	**F1** } Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** } harmonics from the data output
8	**F4**
9	**V_{CC2}:** Connect to Pin 1 (see Pin 1 function) close to the device
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level
11	**Data Output:** Supplies T^2L level data that corresponds to the FSK input received
12	**Digital Ground:** Should be connected to digital ground
13 and 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency
17	**Analog Ground:** Connect to analog ground close to the device
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry
19	**Input:** The FSK signal from the cable goes to this pin
20	**No Connection**

TIMING DIAGRAMS

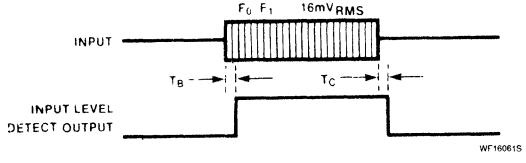

Figure 1. Delay Time, t_B, t_C

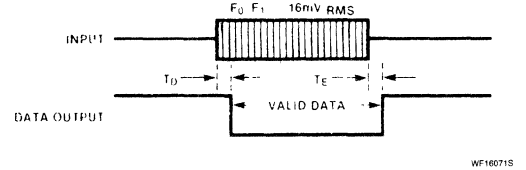

Figure 2. Delay Time, t_D, t_E

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Signetics

AN195
Applications Using the NE5080, NE5081

Application Note

Linear Products

APPLICATIONS

Figure 1 shows a block diagram of the NE5080 and NE5081 in a simple point-to-point communications scheme. Pin 5 of the NE5080 is grounded to permanently enable transmission, grounding Pin 3 disables the jabber function

An example of a communications system block diagram using the NE5080 and the NE5081 (as in a modem) is shown in Figure 2

The jabber function is active in this system. The NE5080 Jabber Flag (Pin 2) goes high when the capacitor at Pin 3 of the NE5080 charges to about 1 4V This fault condition will interrupt the Transmission Controller, which will cease transmitting and write to the proper address for the decoder to put out a signal to discharge the capacitor. The Controller will then pass the token to the next node

The transmission medium can be anything from a twisted pair to a fiber optic link The NE5081 receives the FSK signal and converts it to a digital data stream corresponding to the data sent by the NE5080. Pin 10 of the NE5081 goes high when the signal at its input is above the threshold set by the potentiometer between Pins 13 and 14 of the NE5081.

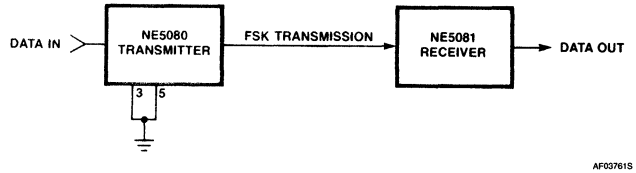


Figure 1. Point-to-Point Communications

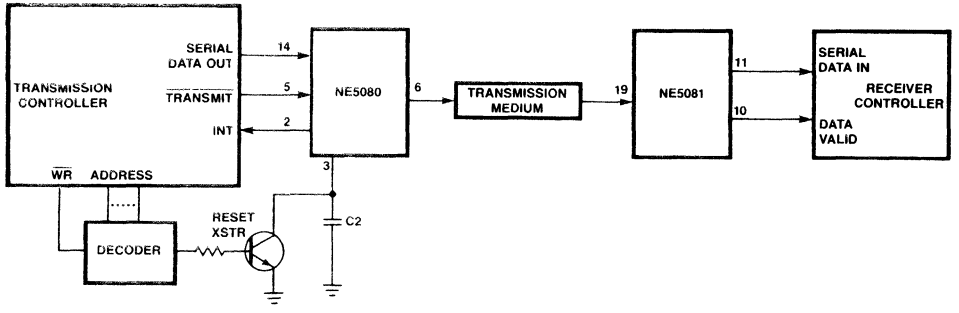
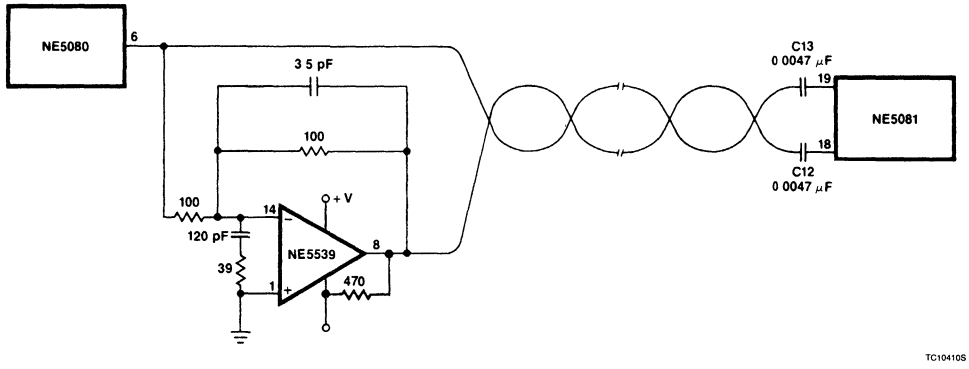


Figure 2. Communications System Block Diagram

Applications Using the NE5080, NE5081 AN195



NOTE:
In applications using twisted-pair lines where noise pick-up may be excessive, it is recommended that the twisted-pair be driven differentially

Figure 3. Modem Using a Twisted-Pair Transmission Line

DC-to-2 Megabaud Modem Using the NE5080 and NE5081

The NE5080 and NE5081 are designed to be used together as an asynchronous modem. They employ FSK modulation at high carrier frequencies, plus filtering to reject EMI and RFI noise that is frequently encountered in industrial and commercial environments. Figures 4 and 5 show full- and half-duplex modems.

The carrier frequency is externally adjustable and can range from 50kHz to over 20MHz.

The modem can be used in a number of ways:

1. Multidrop party line of data transmitting and receiving devices (local area networks).
2. Point-to-point operation connecting just two transmitting/receiving devices.
3. Either of the above operated on one cable in the half-duplex mode.
4. Either 1 or 2 above operated on two cables in the full-duplex mode.

The 30dB dynamic range of modems built using the NE5080 and NE5081 makes it possible to attach them at any point on the cable without any gain adjustment. There is no problem with proximity to other similar modems.

The distance that can be driven varies with the type of cables used, the number of modems attached to the cable, and the carrier frequency.

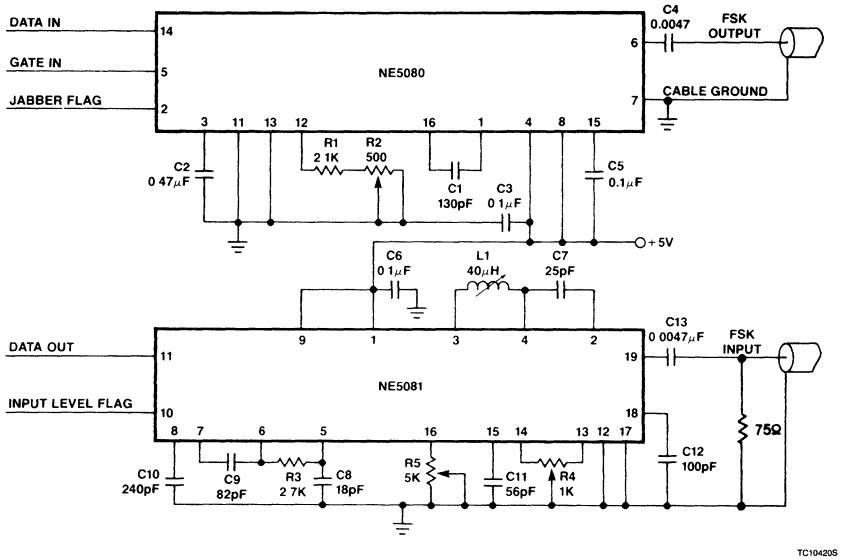
Typical operation can be 100 modems randomly spaced on up to 2000 meters of RG-11 (foam) cable with a center frequency of 5MHz.

In point-to-point operation, one can drive further. Table 1 gives obtainable distances when different carrier frequencies and cables are used.

Table 1. Transmission Distance for a Single Receiver as a Function of Center Frequency and Cable Type

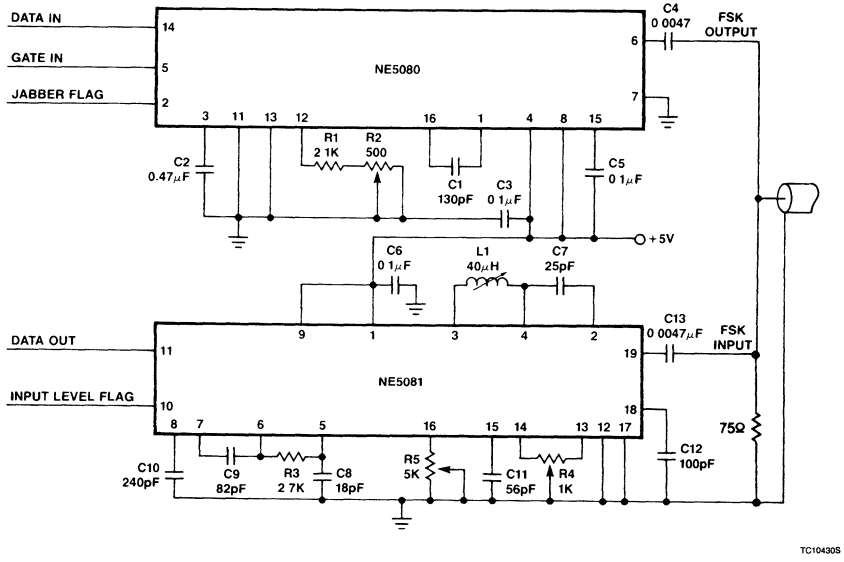
CARRIER FREQUENCY	MAXIMUM DATA RATE	CABLE			
		RG-59	RG-11 (Foam)	T4412J	T4750J
1MHz	0.5 Megabaud	6000 Ft	21000 Ft	33000 Ft	50000 Ft
3MHz	1.0 Megabaud	5000 Ft	12000 Ft	20000 Ft	32000 Ft
5MHz	2.0 Megabaud	4200 Ft	9500 Ft	15000 Ft	25000 Ft

Applications Using the NE5080, NE5081 AN195



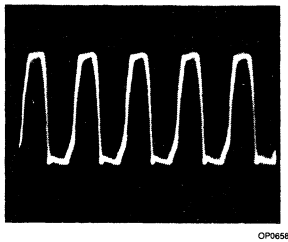
EXTERNAL COMPONENTS SHOWN HERE ARE FOR 5MHz CARRIER

Figure 4. NE5080 and NE5081 Connected as a Full-Duplex Modem



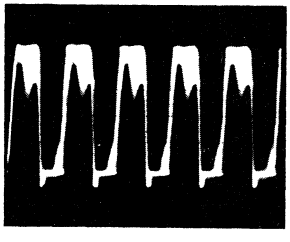
EXTERNAL COMPONENTS SHOWN HERE ARE FOR 5MHz CARRIER

Figure 5. NE5080 and NE5081 Connected as a Half-Duplex Modem



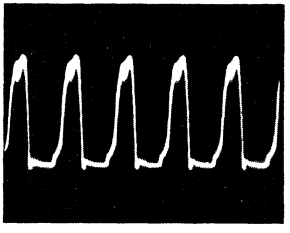
OP06580S

Figure 6. NE5081 Data Output When Correctly Tuned to Incoming 5MHz Carrier



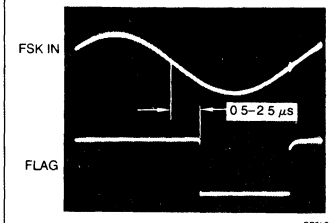
OP06590S

Figure 7. NE5081 Data Output When Tuned Just Below 5MHz Carrier



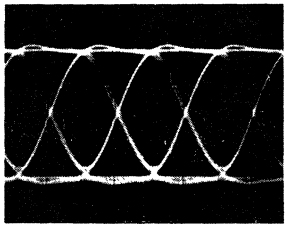
OP06600S

Figure 8. NE5081 Data Output Tuned Just Above 5MHz Carrier



OP06610S

Figure 9. Correct Adjustment of Input Level Detection Timing



OP06620S

Figure 10. 'Eye' Pattern at NE5081 Pin 8

FSK MODEM SETUP PROCEDURES

To set up the modem per IEEE 802.4 specifications, the following sequence should be followed at 25 ±2°C ambient.

TRANSMITTER SETUP:

1. Ground Jabber Control (Pin 3) and the transmit gate (Pin 5) of the NE5080.
2. Turn on the power and allow the circuit to warm up for 3 minutes.
3. Hold the Data Input (Pin 14) of the NE5080 at a logic high.
4. Measure the frequency at the FSK output of the transmitter (cable should be properly terminated) and adjust R2 for a frequency reading of 6.250MHz ±5kHz.
5. Apply a logic low to the Data Input and check the output frequency. If the reading is not 3.750MHz ±40kHz, readjust R1 until the high frequency is 6.250MHz ±25kHz and the low frequency is 3.750MHz ±40kHz.

Transmitter setup is now complete.

RECEIVER SETUP:

6. Set Detection Timing pot R5 and Input Level Detect pot R4 at the NE5081 to mid range.
7. Apply a 5.000MHz $1V_{P-P}$ sine wave to the receiver FSK Input.
8. Attach an oscilloscope probe to the Data Output pin of the NE5081 and adjust L1 or C7 (whichever is adjustable) until the output state alternates between high and low levels. Figure 7 and 8 indicate examples of improper tuning.
9. Set the generator to 3.750MHz, $35mV_{P-P}$.
10. Adjust Input Level Detect pot R4 until the Data Output pin is alternating between high and low levels.
11. Increase the generator output to $45mV_{P-P}$ and verify that the data output is low.
12. Decrease the generator output to $25mV_{P-P}$ and verify that the data output is high.
13. Apply a 100kHz $1V_{P-P}$ signal to the FSK Input and connect a scope probe to the Input Level Flag and another probe to the FSK Input. Adjust Detection Timing pot R5 so that the delay from the time the FSK Input signal goes through 0 volts on the Positive to negative transition, to the time when the Input Level Flag goes from high to low, is between 0.5 and 2.5µs. See Figure 9.
14. For final adjustment to the tuning of L1/C7 use an adjusted transmitter to transmit pseudo random data and tune the receiver L1/C7 tank circuit for minimum jitter and symmetrical eye pattern observed on the receiver Pin 8 (see Figure 10).

This concludes the receiver setup procedure.

DETERMINING COMPONENT VALUES

Power supply pins of both devices should be bypassed with high quality 0.1µF capacitors close to the devices. Additionally, the NE5081 V_{CC2} (Pin 9) should be well-decoupled from the power supply by a small inductor (about 10µH) and another 0.1µF capacitor as the NE5081 exhibits large changes in power supply current during switching.

The coupling capacitors C4 and C13 are needed to maintain input bias when a low DC impedance line is connected to the FSK Input. Too small a value for these capacitors could result in excessive signal attenuation. If these capacitors are too large, the receiver Input Level Flag may remain high for an excessive amount of time after the input signal is removed. Each transmitter and each receiver should have its own coupling capacitor. This is necessary to prevent any DC terminations from altering biases.

The external resistance at the NE5080 Pin 12 should always be about 2.4kΩ, with some adjustment allowable to compensate for the tolerance of C1 and slight differences between individual ICs.

5

C11 and R5 are the Carrier Detect timing components and determine how long after the FSK input signal is discontinued before the Input Level Flag goes low. R5 should not exceed 5kΩ. With C11 set at 56pF, a 5kΩ R5 will allow Carrier Detect Timing adjustment to 2μs. R5 can be a fixed resistor if this timing is not critical (perhaps because of the use of an "end of data" signal). This delay is required to allow the signal to propagate through the receiver. Carrier Detect Timing should be adjusted for different center frequencies by choosing C11 according to the relationship:

$$C11 = \frac{1}{3572\ f_C}$$

The Input Level Detect function can be disabled and the receiver be made to hold the Carrier Detect Flag high by removing R5 and C11 and tying Pins 15 and 16 together and pulling them up to V_{CC} with a 10kΩ resistor

If the Jabber function is not to be used, Jabber control Pin 3 of NE5080 should be grounded. If the Jabber function is to be used, a capacitor, C2, should be connected between Pin 3 and ground. The value of this capacitor is determined as indicated below.

$$C2 = (0.95 \times 10^{-6})t$$

where t is the maximum allowable transmit time in seconds

The resistance R1, together with capacitor C1, set the transmit frequencies The logic high frequency is fixed at about 1.67 times the logic low frequency, meaning that the logic low frequency is 0.75 times the center frequency f_C, and the logic high frequency is 1.25 times the center frequency. Note that this center frequency is never transmitted in normal operation and is sometimes referred to as the "carrier frequency."

C1 is chosen by the relationship for f_C at or below 7MHz:

$$C1 = \frac{6.5 \times 10^4}{f_C}$$

Above 7MHz center frequency, this capacitor is found by modifying this equation to:

$$C1 = \frac{5.5 \times 10^{-4}}{f_C}$$

To get the characteristics that are needed for proper operation of the NE5081, it is important to keep the proper relationship between L1 and C7:

$$C7 = \frac{1}{7885\ f_C}$$

$$L1 = \frac{200}{f_C}$$

Capacitor values of the filter are dependent upon operating frequencies to maintain proper characteristics:

$$C8 = \frac{9.0 \times 10^{-5}}{f_C}$$

$$C9 = \frac{4.1 \times 10^{-4}}{f_C}$$

$$C10 = \frac{1\,2 \times 10^{-3}}{f_C}$$

$$C12 = \frac{5 \times 10^{-4}}{f_C}$$

Coupling capacitor values also depend upon center frequency·

$$C4 = C13 = \frac{2.5 \times 10^{-2}}{f_C}$$

In all of the above equations, capacitances are in Farads, inductances in Henrys, and frequencies in Hertz

SOME COMMON BAUD RATES

Although intended to be used with a center frequency of 5MHz, the NE5080 and NE5081 can be used at other center frequencies. Table 2 gives minimum center frequency (f_C) for some common baud rates, together with external component values for those center frequencies Note that it is not recommended that these devices be operated at center frequencies below 50kHz

USING THE NE5080/NE5081 WITH A FIBER-OPTIC LINK

The NE5080/NE5081 chip set is highly suitable for use in low cost fiber-optic links There are many advantages to fiber links over open-wire or coaxial cable links These advantages include:

1. Cost savings in conductor weight and size.
2. Immunity to EMI/RFI
3. Low crosstalk.
4. High communications security; cannot be tapped by electromagnetic induction or surface conduction.
5. Fiber-optic cable does not radiate electromagnetic energy nor disturb other communications media.
6. Extremely wide bandwidth (high channel per conductor density)
7. Low attenuation
8. No ground loops or shifts caused by common grounds.
9. Complete electrical isolation between transmitter and receiver.
10. Cable breaks cause no shorts, making this technology useful in hazardous environments, e.g., explosive chemical facilities.
11. No damage to equipment is expected due to current surges on adjacent lines.
12. Fiber cable does not act as an antenna to pick up high electromagnetic pulses such as those caused by electrical storms.
13. Low BER (Bit Error Rate).

The circuit of Figure 11 shows a simplex fiber link between the NE5080 transmitter and the NE5081 receiver The components shown are for a center frequency of 5MHz, although this frequency can be increased to 20MHz with proper selection of external component values The NE5539 has a 350MHz unity gain bandwidth which may limit maximum operating frequencies in some systems.

Since the NE5081 can adequately accept signals below 10mV at 5MHz carrier, the gain stage (within the dashed lines of Figure 11) may be eliminated if the attenuation in the link is low If the gain stage is used, be mindful of the bandwidth trade-off at higher gains. Refer to the NE5539 data sheet for details.

The transmitter and receiver are set up as described under FSK Modem Setup Procedure

LAYOUT PRECAUTIONS

As is the case with any components using high frequencies, good layout practice is essential; poor layout can adversely affect performance. All lead lengths should be as short as is practical for all lines which carry RF, including the tuning capacitor and resistors (C1, R1, R2) of the NE5080. Lead length is especially critical with C1, which should be mounted as close to the NE5080 as is possible. A printed circuit board with a good ground plane, both top and bottom, is also recommended (wire-wrap is NOT recommended). The ground plane should extend below tuning capacitor C1 on both top and bottom of the board, with no other trace coming between the leads of this capacitor.

Because of the high speed switching, Pin 9 (V_{CC2}) of the NE5081 can exhibit a large current swing, causing vertical output jitter which may be eliminated by decoupling Pin 9 with a small (10μH) RF choke and a 0.05μF capacitor.

See Figure 12 for an example of a working layout.

Table 2. Recommended Minimum Center Frequency and Component Values for Various Baud Rates

BAUD RATE (kBaud)	f_C (kHz)	C1	L1	C4 C13	C7	C8	C9	C10	C11	C12
9.6	50	13nF	4mH	0.50μF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
19.2	50	13nF	4mH	0.50μF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
38.4	100	6.8nF	2mH	0.27μF	1 3nF	0.9nF	3.9nF	12nF	2.7nF	5nF
50.1	125	5.1nF	1.6mH	0.20μF	1.0nF	750nF	3.3nF	10nF	2.2nF	3.9nF
64.0	160	3.9nF	1.3mH	0.15μF	800pF	560pF	2.5nF	7.5nF	1.8nF	3nF
128	320	2nF	625μH	0.075μF	390pF	270pF	1.3nF	3 9nF	860pF	1.6nF
256	640	1nF	312μH	0.039μF	200pF	150pF	640pF	1.8nF	430pF	750pF
512	1250	510pF	160μH	0 02μF	100pF	75pF	330pF	1.0nF	220pF	390pF
1500	3750	180pF	53μH	6.8nF	33pF	25pF	110pF	330pF	75pF	130pF
1544	4000	160pF	50μH	6.8nF	33pF	22pF	100pF	300pF	68pF	125pF
2000	5k	130pF	40μH	5 0nF	25pF	18pF	82pF	240pF	56pF	100pF
8000	20k	33pF	10μH	1.2nF	6pF	5pF	20pF	62pF	15pF	25pF

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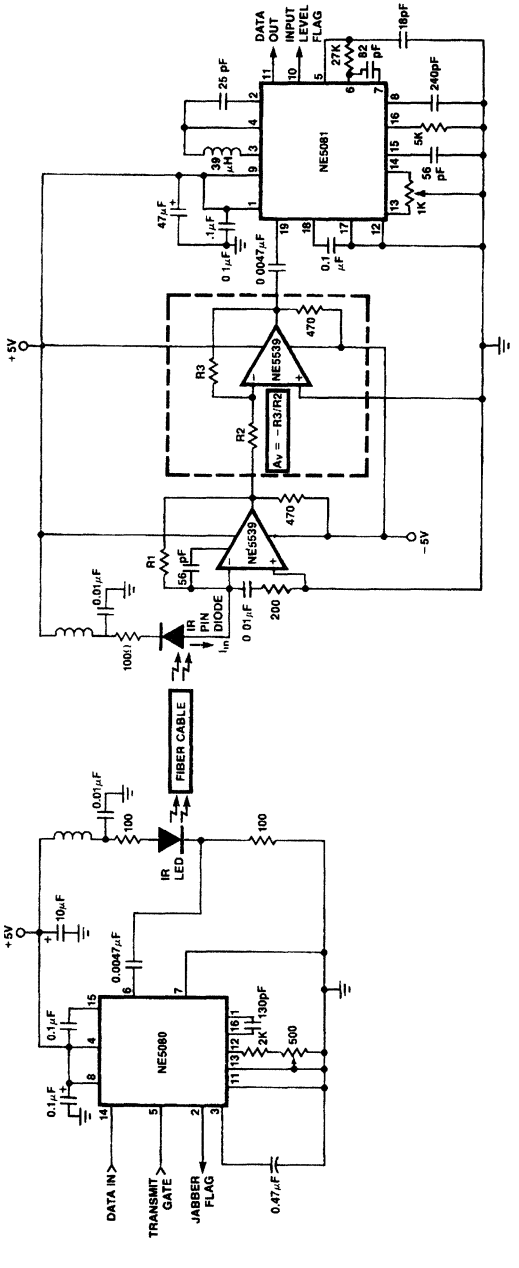
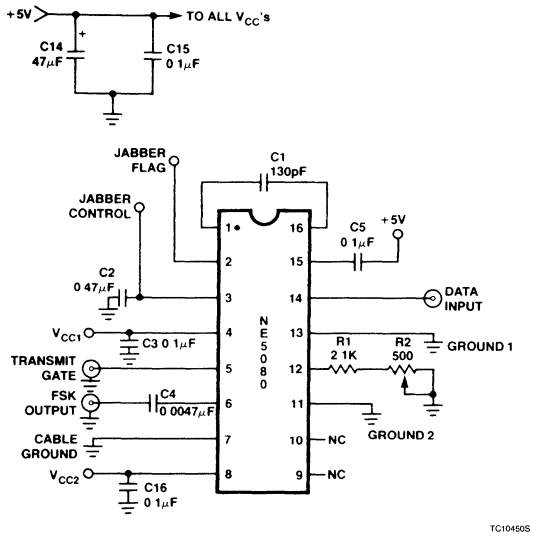
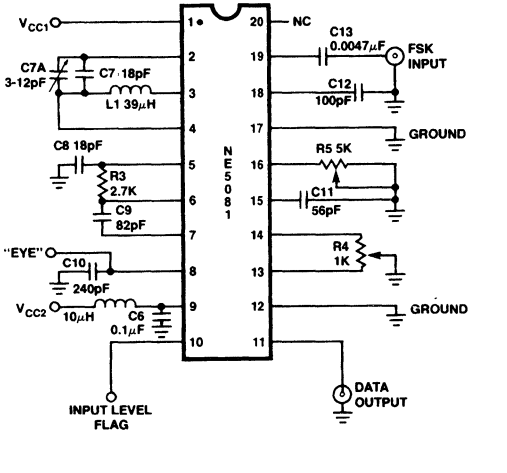


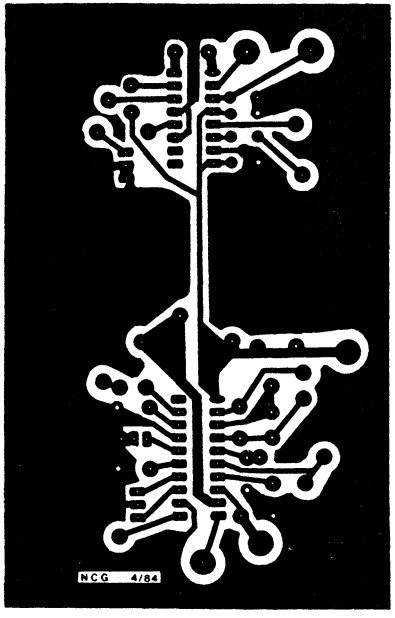
Figure 11. Simplex Fiber-Optic System





NOTE:
See NE5080 and NE5081 Block Diagram(s)

NOTE:
Signetics NE5080/NE5081 Evaluation Board



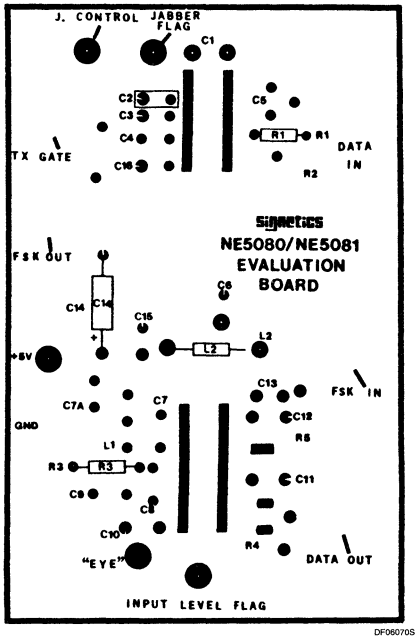


Figure 12. Components and Layout Used for Evaluation Board

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Signetics

AN1950
Application of NE5080 and NE5081 With Frequency Deviation Reduction

Linear Products

Application Note

Author: Prasanna M. Shah

INTRODUCTION

Application note AN195 discusses numerous applications of NE5080 and NE5081 in point-to-point, half-duplex and full-duplex communications using coaxial, twisted-wire pair, and fiber optic cables. It also discusses several aspects about tuning the transmitter and receiver at various center frequencies and board layout precautions. In this application note, the transmitter and receiver chips themselves are discussed. Following the brief circuit description, a few novel application ideas are discussed.

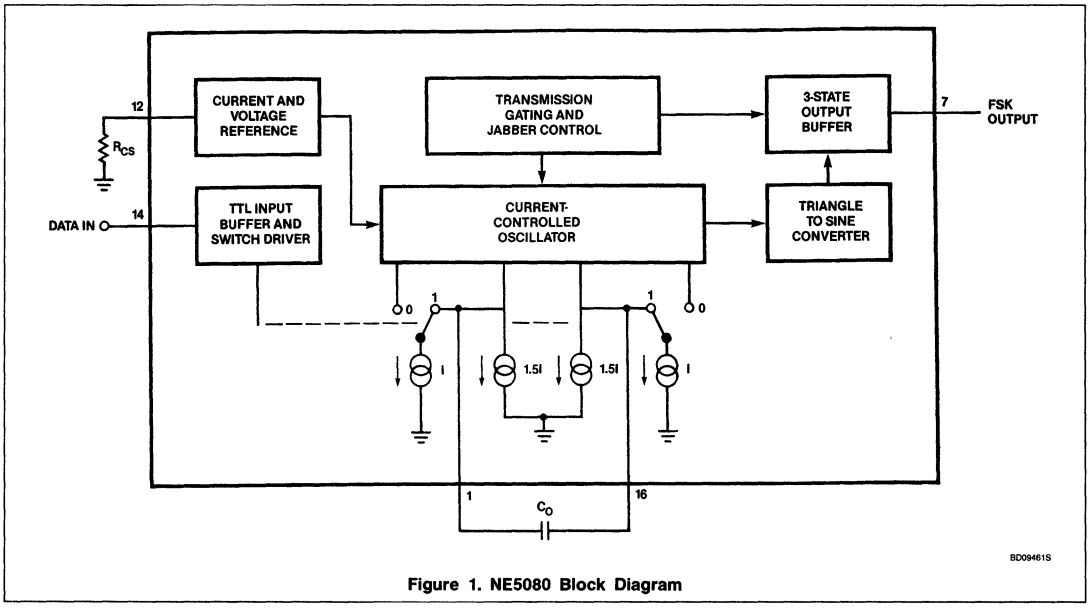

Figure 1. NE5080 Block Diagram

TRANSMITTER

The block diagram of the transmitter NE5080 is shown in Figure 1. The transmitter is composed of the following six major building blocks: a TTL input buffer and switch driver, a current controller oscillator, a triangle-to-sine wave converter, a 3-state output buffer, and transmission gating and jabber control circuitry. It also has an on-chip voltage regulator that provides current and voltage references to the various building blocks of the circuit.

The transmitter center frequency can be adjusted by selecting the values of the tuning capacitor, C_O. The switch driver circuitry switches the current sources I in and out of Pins 1 and 16. This effectively changes the total average charging and discharging current into C_O from 1.5I to 2.5I, which causes the output to shift from one frequency to another. This soft switching action keeps the output phase continuous and eliminates discontinuities. The ratio of the two output frequencies is equal to the ratio of the total average current charging and discharging C_O. Since the values of the internal current sources are fixed, it produces a constant frequency ratio of 1.66. An external modification for changing this ratio through extra components is discussed later.

The triangle-to-sine wave converter circuitry converts the output of the current-controlled oscillator into a sine wave with about 2% distortion. The transmission gating and jabber control circuitry controls the FSK output through the 3-state output buffer. The transmit gate, when held high, will inhibit the transmission by putting the output buffer into the high impedance state. It also turns off the current-controlled oscillator, thus minimizing any feedthrough to the output.

The jabber control function is similar to the transmit gate, but the transmission time can be programmed through an external capacitor. There is a small current sourced to the jabber control pin, which charges up the capacitor. When the voltage on the capacitor reaches a preset threshold level, the transmission is stopped. This is a failsafe feature provided to restrict an errant transmitter or the NE5080 itself from tying up the network. In point-to-point communications, the jabber control can be disabled by connecting the jabber control pin to ground.

Application of NE5080 and NE5081 With Frequency Deviation Reduction

AN1950

RECEIVER

The receiver block diagram shown in Figure 2 is composed of the following seven major building blocks: an input limiter, a phase shifter, an analog multiplier, a low-pass filter, a comparator, an input level detector, and a TTL output buffer. The input limiter limits the FSK input signal eliminating any amplitude variations.

The L and C tank circuit of the phase shifter is tuned to resonate with the incoming carrier center frequency. A quadrature detection scheme is used to demodulate the data. The balanced analog multiplier processes the incoming signal with its phase-shifted carrier frequency and generates signals with baseband data and other higher order harmonics.

The low-pass filter is a simple second-order Butterworth filter which eliminates the carrier frequency and higher-order intermodulation frequencies, and gives the baseband data which is equivalent to the signal modulated by the transmitter. The comparator makes the decision based on the output of the low-pass filter with reference to a threshold voltage. The TTL buffers provide the output data at TTL levels. The input detection level can be adjusted through the external resistor to set the threshold for minimum input level. If the input level falls below the set threshold, the output buffers are disabled, preventing the noise from being interpreted as data.

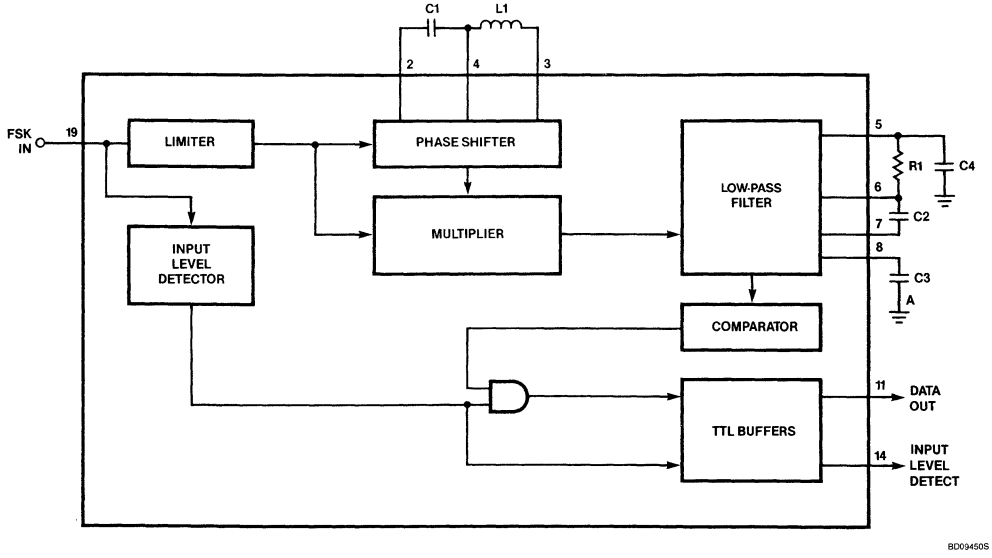

Figure 2

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Application of NE5080 and NE5081 With Frequency Deviation Reduction

AN1950

APPLICATIONS

NE5080 AND NE5081 chip set encompasses a broad spectrum of data rates and facilitates economical modem design for various applications. The transmitter can be tuned to various center frequencies for different data rates. The wide dynamic range of the receiver and the excellent drive capability of the transmitter make it possible to drive long distances without any signal repeaters. The transmitter is not limited to transmitting on coaxial cable only; it can also drive a twisted-wire pair and optical fibers. All these salient features are discussed in greater detail in AN195.

The major focus of this application note is on reducing the frequency deviation. The reduction in frequency ratio can be achieved by bringing the two frequencies f_0 and f_1 closer together. This will reduce the overall bandwidth utilized by the modem because the main lobe in the spectrum becomes narrower. This gain in bandwidth reduction is offset by a slight increase in the probability of a bit error due to poor noise margin. As explained in the transmitter block diagram section of this application note, the frequency of the oscillator is controlled by the charging and discharging current into C_O. The two oscillating frequencies can be brought close together either by lowering the higher frequency f_1 or by raising the lower frequency f_0. Figure 3 shows the technique for raising the lower frequency f_0. When the logic input is a '1', the two diodes are reversed biased. In this situation, the capacitor is charged and discharged by the current from the internal current sources. As the logic input changes to a '0', the two diodes are forward biased. This will increase the available current from the internal current sources that are charging and discharging the capacitor C_O, thus resulting in a higher frequency of oscillation than would be obtained otherwise. The value of resistor R will determine the amount of excess current available, which will affect the ratio of the higher frequency to the lower frequency (f_1/f_0).

Figure 4 gives a graph of the deviation ratio versus the resistor value R for different values of oscillator capacitor C_O. It can be seen from the graph that the deviation ratio remains constant for a fixed value of resistor R over a wide range of capacitor values C_O. It should be noted that the effective data rates will be lower when the frequency deviation is reduced. A similar scheme can also be applied to increase the frequency ratio and thereby increase the data rate, but this will be done at the cost of extra bandwidth. Using appropriate filters for the transmitters and receivers, a frequency division multiplexing (FDM) can be achieved for more efficient usage of the most expensive resource, namely the coaxial cable.

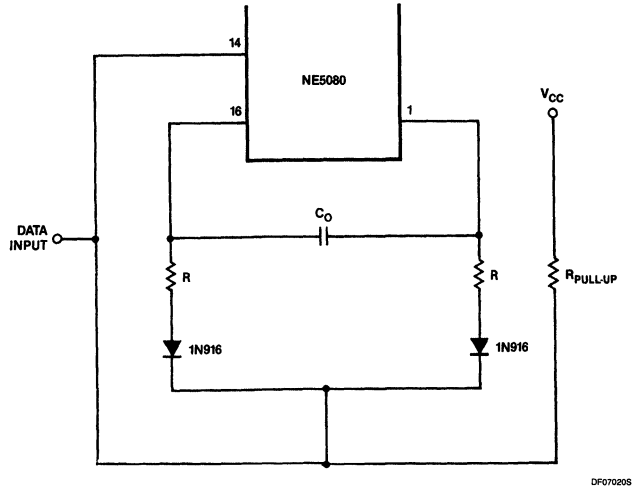


Figure 3

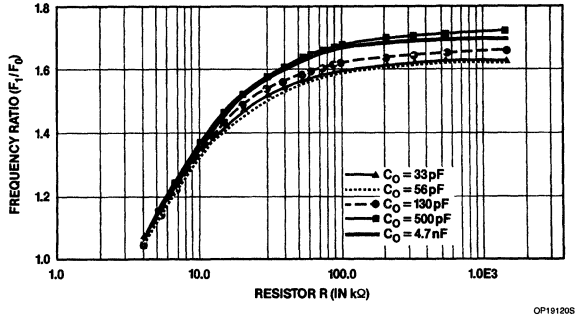


Figure 4

NE5210
Transimpedance Amplifier (280MHz)

Preliminary Specification

Linear Products

DESCRIPTION

The NE5210 is a 7kΩ transimpedance wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

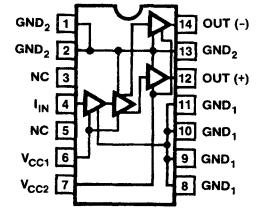
- **Low noise: 3.5pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 280MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **High overload threshold current**
- **Wide dynamic range**
- **7kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wideband gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

D Package



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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5210D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	6	V
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Operating junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Power dissipation T_A = 25°C (still air)[1]	1.0	W
I_{INMAX}	Maximum input current[2]	5	mA

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance. θ_{JA} = 125°C/W.
2. The use of a pull-up resistor to V_{CC} for the PIN diode, is recommended

Transimpedance Amplifier (280MHz) NE5210

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	0 to +90	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC} = 5V, unless otherwise specified. Typical data applies at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	V
V_{OS}	Output offset voltage			0	80	mV
I_{CC}	Supply current		21	26	32	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±120	±160		μA
I_{INMAX}	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±160	±240		μA

NOTE:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current

Transimpedance Amplifier (280MHz) NE5210

AC ELECTRICAL CHARACTERISTICS Typical data and Min/Max limits apply at V_{CC} = 5V and T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 8, Procedure 1	4 9	7	10	kΩ
R_O	Output resistance (differential output)	DC tested	16	30	42	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	2.45	3.5	5	kΩ
R_O	Output resistance (single-ended output)	DC tested	8	15	21	Ω
f_{3dB}	Bandwidth (–3dB)	Test Circuit 1, T_A = 25°C	200	280		MHz
R_{IN}	Input resistance			60		Ω
C_{IN}	Input capacitance			7.5		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5± 0.5V		9.6	20	%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.05	0.1	%/°C
I_N	RMS noise current spectral density (referred to input)	f = 10MHz, T_A = 25°C, Test Circuit 2		3.5	6	pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0$[1]	T_A = 25°C Test Circuit 2				
		Δf = 100MHz		37		nA
		Δf = 200MHz		56		nA
		Δf = 300MHz		71		nA
	C_S = 1	Δf = 100MHz		40		nA
		Δf = 200MHz		66		nA
		Δf = 300MHz		89		nA
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	Dc tested, ΔV_{CC} = 0.1V Equivalent AC test circuit 3	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = 0 1V Equivalent AC test circuit 4	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = 0 1V Equivalent AC test circuit 5		65		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	f = 0.1MHz, Test Circuit 6		23		dB
V_{OMAX}	Maximum output voltage swing differential	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3 2		V_{P-P}
V_{INMAX}	Maximum input amplitude for output duty cycle of 50± 5%[3]	Test Circuit 7	650			mV_{P-P}
t_R	Rise time for 50 mV_{P-P} output signal[4]	Test Circuit 7		0 8	1 2	ns

NOTES:
1 Package parasitic capacitance amounts to about 0 2pF
2 PSRR is output referenced and is circuit board layout dependent at higher frequencies For best performance use RF filter in V_{CC} line
3 Guaranteed by linearity and overload tests
4 t_R defined as 20 – 80% rise time It is guaranteed by a -3dB bandwidth test

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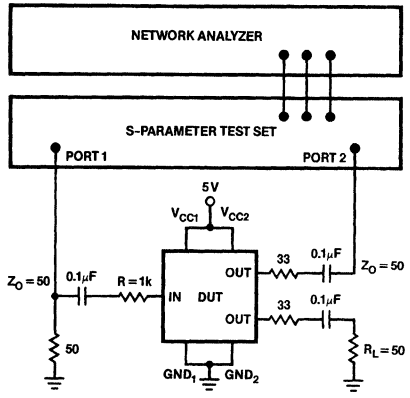
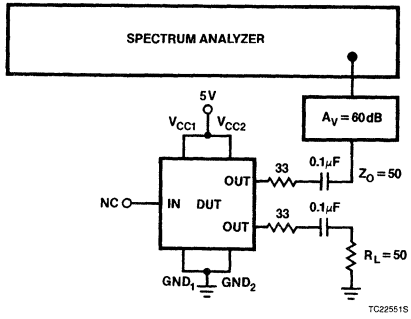
Transimpedance Amplifier (280MHz) NE5210

TEST CIRCUITS



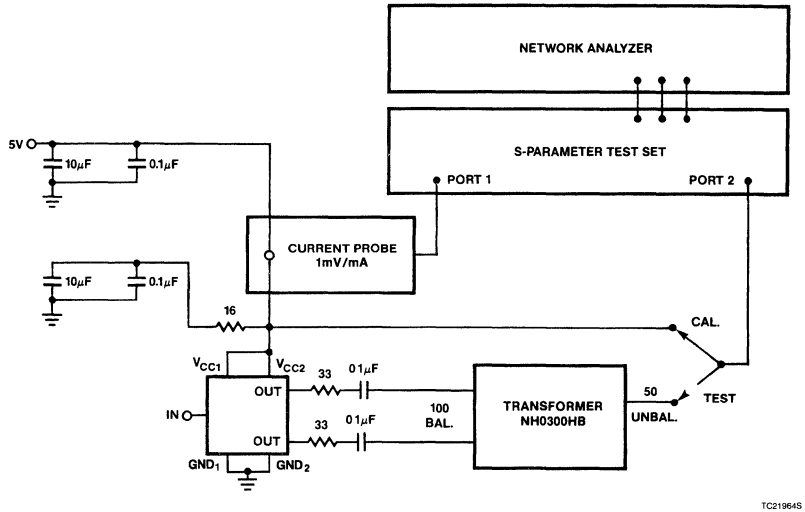
SINGLE-ENDED	DIFFERENTIAL
$R_T \cong \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \times S21 \times R$
$R_O \cong Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 66$

Test Circuit 1

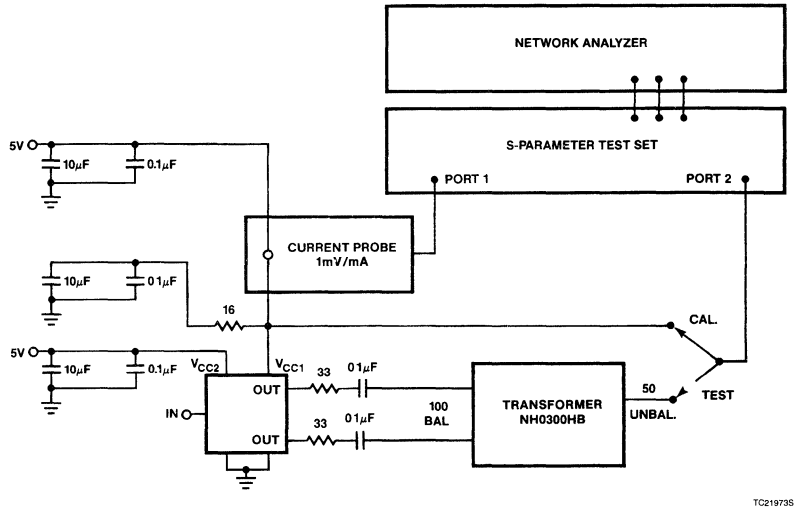


Test Circuit 2

TEST CIRCUITS (Continued)

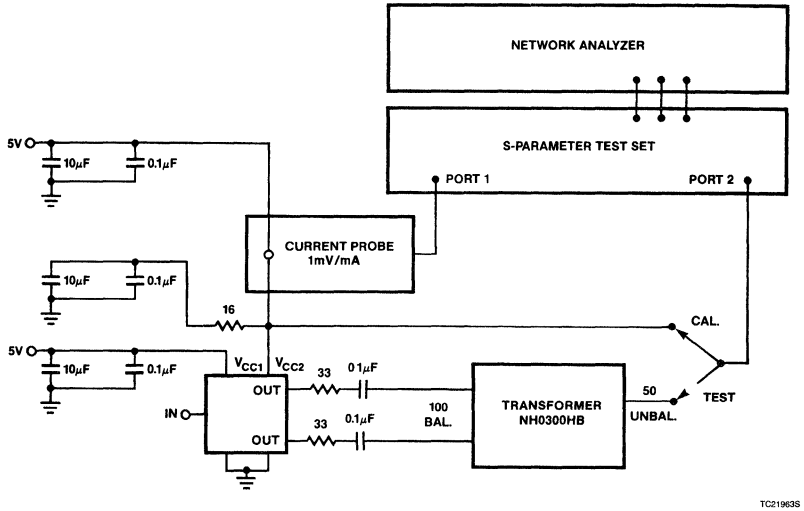


Test Circuit 3

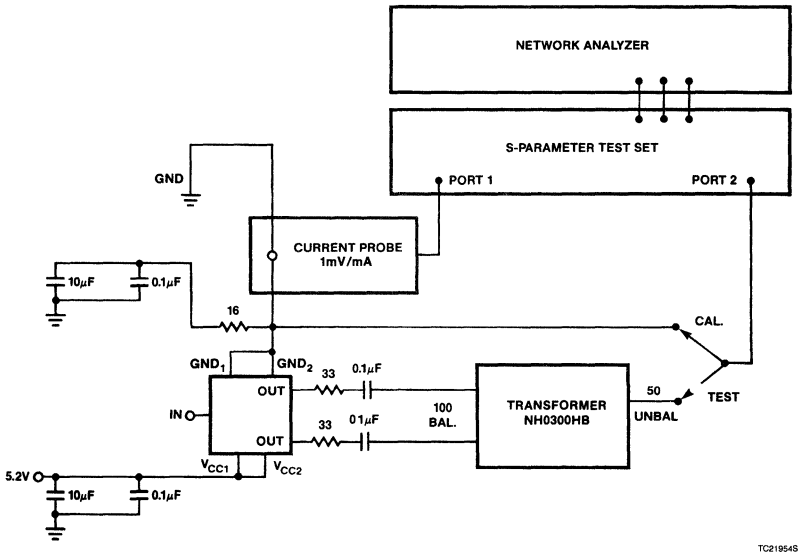


Test Circuit 4

TEST CIRCUITS (Continued)



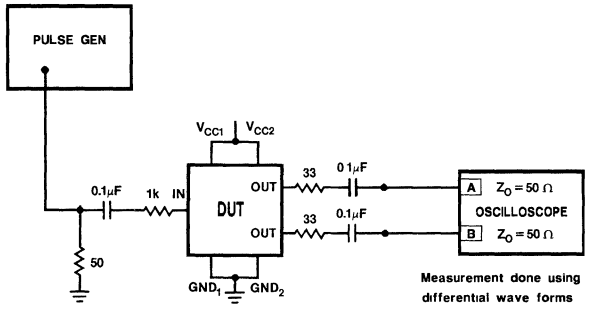
Test Circuit 5



Test Circuit 6

Transimpedance Amplifier (280MHz) NE5210

TEST CIRCUITS (Continued)



Test Circuit 7

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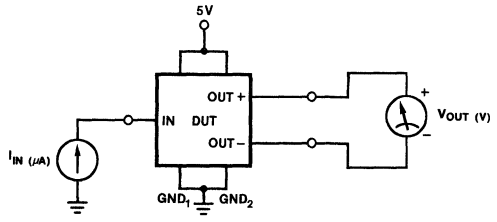
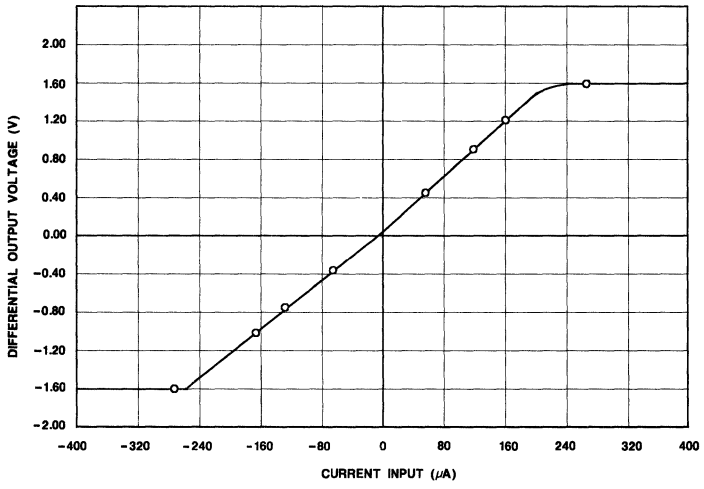
TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input



TC23460S



OP20990S

NE5210 TEST CONDITIONS

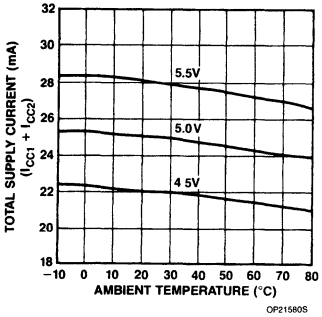
Procedure 1	R_T measured at 60μA $R_T = (V_{O1} - V_{O2})/(+60\mu A - (-60\mu A))$ Where. V_{O1} Measured at $I_{IN} = +60\mu A$ V_{O2} Measured at $I_{IN} = -60\mu A$
Procedure 2	Linearity = 1 – ABS$((V_{OA} - V_{OB})/(V_{O3} - V_{O4}))$ Where: V_{O3} Measured at $I_{IN} = +120\mu A$ V_{O4} Measured at $I_{IN} = -120\mu A$ $V_{OA} = R_T * (+120\mu A) + V_{O8}$ $V_{OB} = R_T * (-120\mu A) + V_{O8}$
Procedure 3	$V_{OMAX} = V_{O7} - V_{O8}$ Where: V_{O7} Measured at $I_{IN} = +260\mu A$ V_{O8} Measured at $I_{IN} = -260\mu A$
Procedure 4	$I_{IN\ MAX}$ Test Pass Conditions: $V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$ Where: V_{O5} Measured at $I_{IN} = +160\mu A$ V_{O6} Measured at $I_{IN} = -160\mu A$ V_{O7} Measured at $I_{IN} = +260\mu A$ V_{O8} Measured at $I_{IN} = -260\mu A$

Test Circuit 8

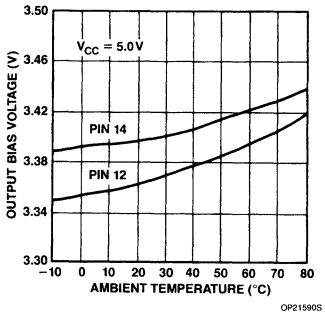
Transimpedance Amplifier (280MHz) NE5210

TYPICAL PERFORMANCE CHARACTERISTICS

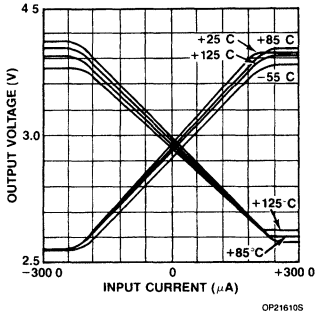
NE5210 Supply Current vs Temperature



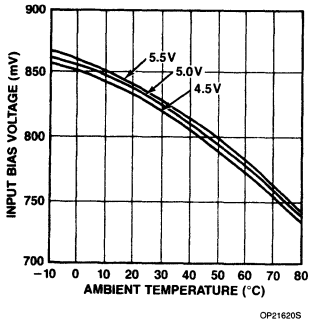
NE5210 Output Bias Voltage vs Temperature



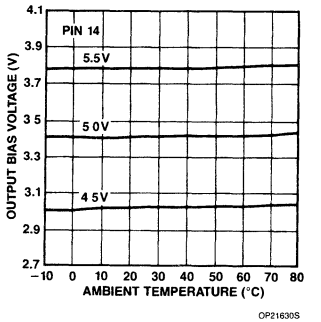
Output Voltage vs Input Current



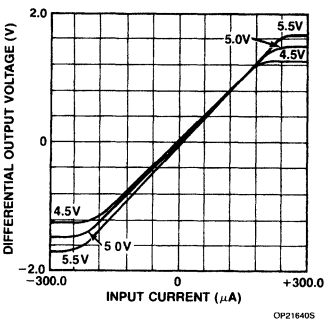
NE5210 Input Bias Voltage vs Temperature



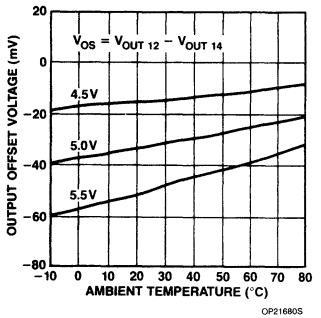
NE5210 Output Bias Voltage vs Temperature



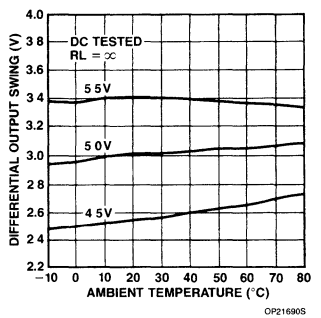
Differential Output Voltage vs Input Current



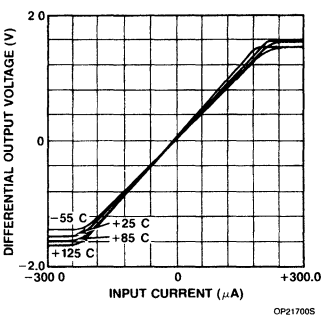
NE5210 Output Offset Voltage vs Temperature



NE5210 Differential Output Swing vs Temperature



Differential Output Voltage vs Input Current



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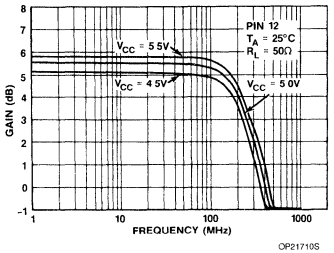
Transimpedance Amplifier (280MHz) NE5210

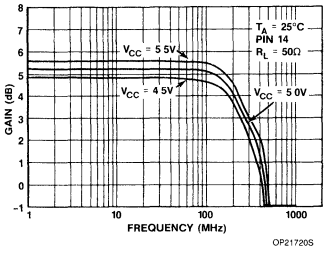
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency



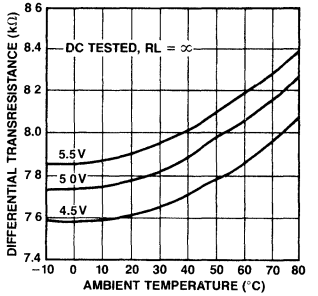
OP21710S

Gain vs Frequency



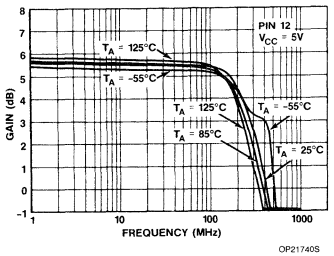
OP21720S

NE5210 Differential Transresistance vs Temperature



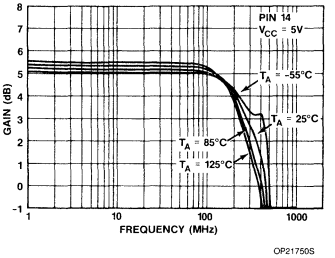
OP21730S

Gain vs Frequency



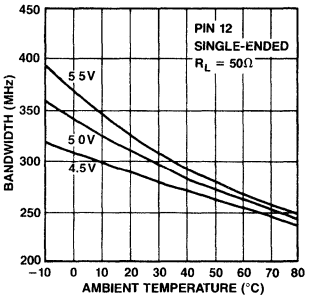
OP21740S

Gain vs Frequency



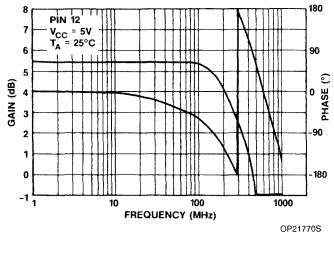
OP21750S

NE5210 Bandwidth vs Temperature



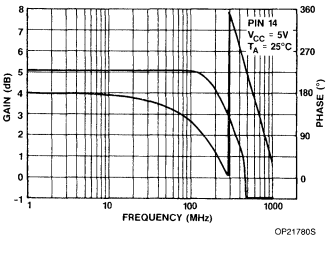
OP21760S

Gain and Phase Shift vs Frequency



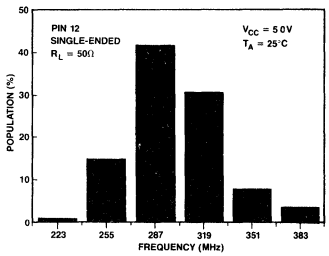
OP21770S

Gain and Phase Shift vs Frequency



OP21780S

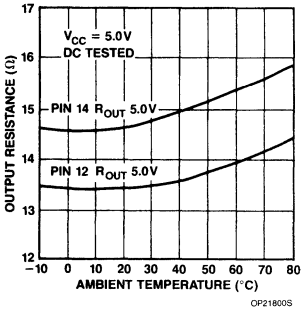
NE5210 Typical Bandwidth Distribution (70 Parts from 4 Wafer Lots)



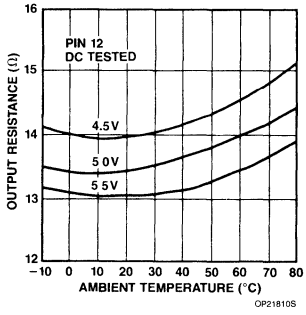
OP21790S

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

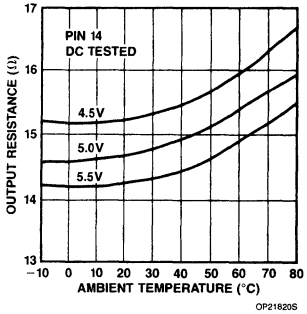
NE5210 Output Resistance vs Temperature



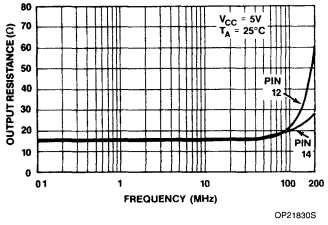
NE5210 Output Resistance vs Temperature



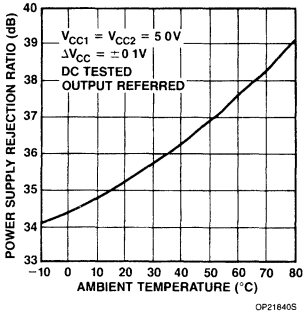
NE5210 Output Resistance vs Temperature



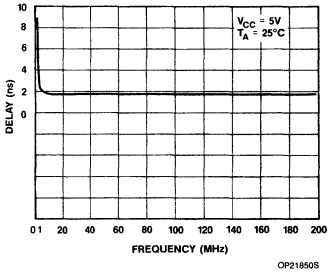
Output Resistance vs Frequency



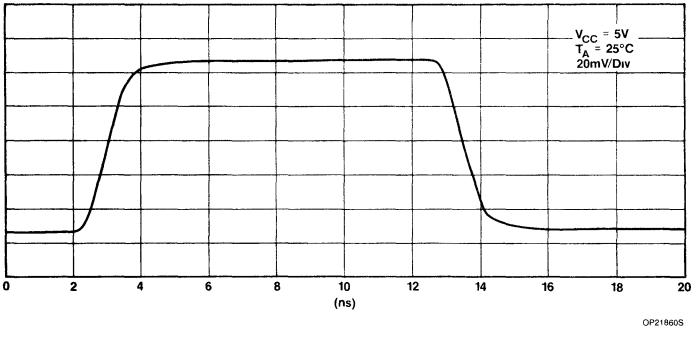
NE5210 Power Supply Rejection Ratio vs Temperature



Group Delay



Output Step Response



5

Transimpedance Amplifier (280MHz) NE5210

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5210 is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5210 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F = 3.6kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(3.6K) = 7.2k\Omega$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage The output impedance is about 17Ω single-ended.

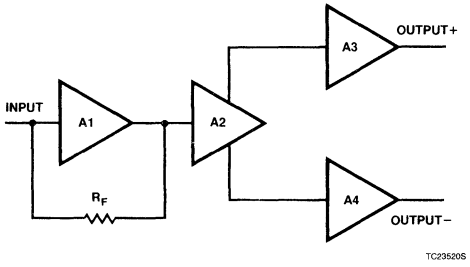


Figure 1. NE5210 – Block Diagram

For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier A simplified analysis can determine the performance of the amplifier The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{3\,6k}{71} = 51\Omega$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier,

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}$$

Assuming typical values for R_F = 3.6kΩ, R_{IN} = 60Ω, C_{IN} = 7 5pF

$$f_{-3dB} = \frac{1}{2\pi\ 7\,5pF\ 60} = 354MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1 + 7 5) pF which will lead to only a 12% bandwidth reduction

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/$\sqrt{Hz}$ The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 240μA and a wideband noise of I_{EQ} = 66nA_{RMS} for an external source capacitance of C_S = 1pF

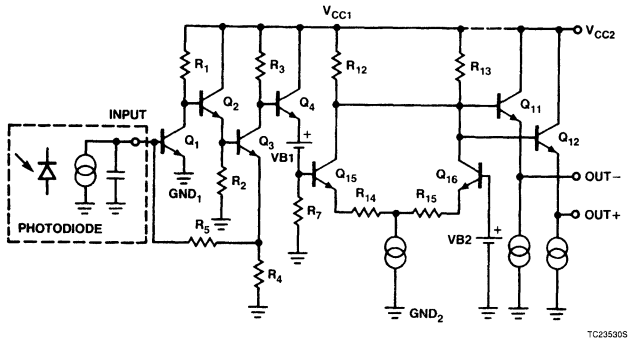


Figure 2. Trans-Impedance Amplifier

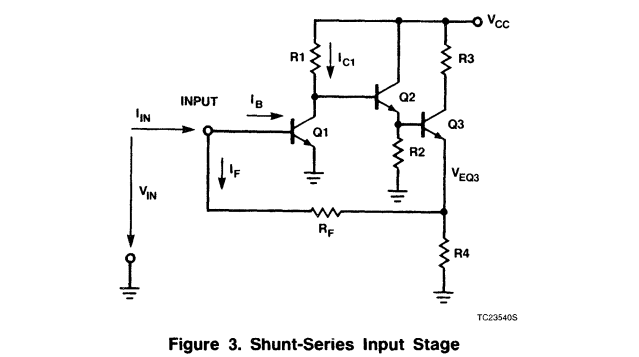


Figure 3. Shunt-Series Input Stage

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$= 20 \log \frac{(240 \times 10^{-6})}{(\sqrt{2}\ 66 \times 10^{-9})}$$

$$= 20 \log \frac{(240\mu A)}{(93nA)} = 68dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

$$\text{Energy of one Photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.
c = speed of light = 3×10^8 mt/sec
c/λ = optical frequency

$$\text{No. of incident photons/sec} = \frac{P}{\frac{hc}{\lambda}} \text{ where P = optical incident power}$$

$$\text{No of generated electrons/sec} = \eta \cdot \frac{P}{\frac{hc}{\lambda}}$$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$I = \eta \cdot \frac{P}{\frac{hc}{\lambda}} \cdot e \text{ Amps (Coulombs/sec)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\eta \cdot e}{\frac{hc}{\lambda}} \text{ Amp/watt}$$

I = P•R

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{66 \times 10^{-9}}{(1.6 \times 10^{-19})(200 \times 10^6)} = 2063$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \frac{hc}{\lambda} B\ Z = 12\ \ 2.3 \times 10^{-19}$$

$$200 \times 10^6\ \ 2063$$

$$= 1139nW = -29.4dBm,$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

$$I_{avMIN} = q P_{avMIN} \frac{\lambda}{hc}$$

$$= \frac{1139 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 792nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 240\mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc\ I_{avMAX}}{\lambda\ q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} 240 \times 10^{-6}$$

$$= 345mW \text{ or } -4.6dBm.$$

Thus the optical dynamic range, D_o is:

$D_o = P_{avMAX} - P_{avMIN} = -4.6 - (-29.4) = 24.8dB.$

This represents the maximum limit attainable with the NE5210 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5210 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near

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Transimpedance Amplifier (280MHz) NE5210

800MHz The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling Some applications may require an RF choke in series with the power supply line Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5210 and the NE5214 post amplifier.

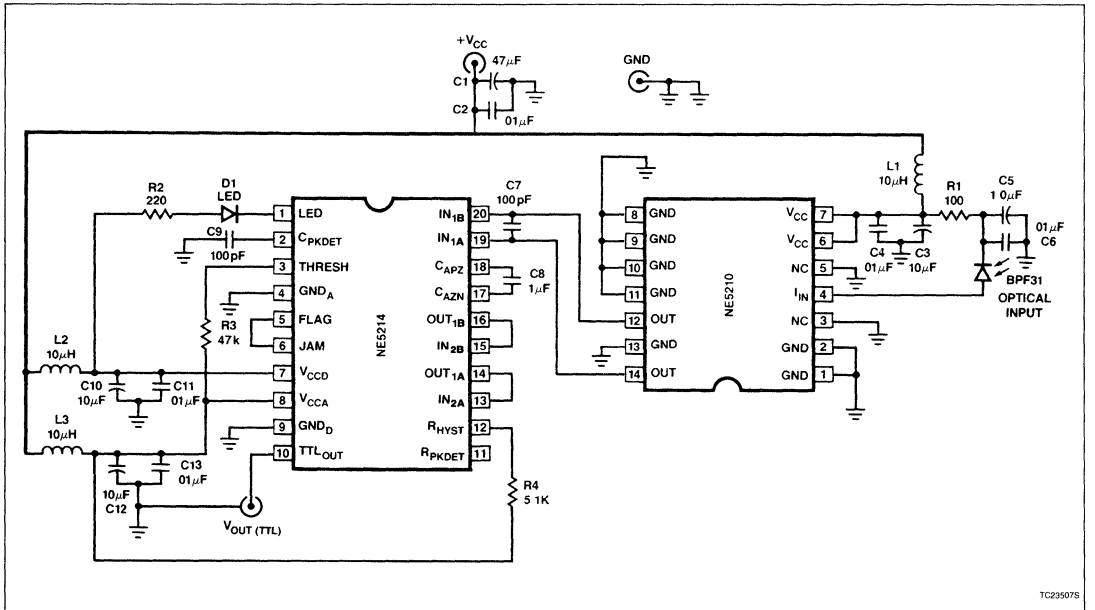


Figure 4. A 50Mb/s TTL Fiber Optic Receiver Using NE5210/NE5214

Signetics

NE/SA5211
Transimpedance Amplifier (180MHz)

Preliminary Specification

Linear Products

DESCRIPTION

The NE/SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

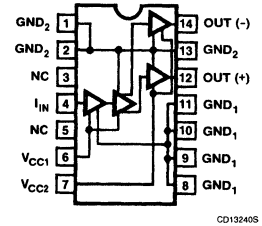
- **Extremely low noise: 1.8pA/√Hz**
- **Single 5V supply**
- **Large bandwidth: 180MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **28kΩ differential transresistance**

APPLICATIONS

- **Fiber optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wide-band gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

D Package



TOP VIEW

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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5211D
14-Pin Plastic SO	−40 to +85°C	SA5211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5211	SA5211	
V_{CC}	Power supply	6	6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
$P_{D\ MAX}$	Power dissipation, T_A = 25°C (still-air)[1]	1.0	1.0	W
$I_{IN\ MAX}$	Maximum input current[2]	5	5	mA

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance θ_{JA} = 125°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range NE Grade SA Grade	 0 to +70 −40 to +85	 °C °C
T_J	Junction temperature range NE Grade SA Grade	 0 to +90 −40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V, unless otherwise specified. Typical data apply at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.00	V
$V_{O\pm}$	Output bias voltage		2.8	3.4	3.7	2.7	3.4	3.7	V
V_{OS}	Output offset voltage			0	120		0	130	mV
I_{CC}	Supply current		21	24	30	20	26	31	mA
I_{OMAX}	Output sink/source current[1]		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±30	±40		±20	±40		μA
$I_{IN\ MAX}$	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±40	±60		±30	±60		μA

NOTE:
1 Test condition output quiescent voltage variation is less than 100mV for 3mA load current.

Transimpedance Amplifier (180MHz) NE/SA5211

AC ELECTRICAL CHARACTERISTICS Typical data and Min and Max limits apply at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested $R_L = \infty$ Test Circuit 8, Procedure 1	22	28	35	21	28	36	kΩ
R_O	Output resistance (differentialoutput)	DC tested		30			30		Ω
R_T	Transresistance (single-ended output)	DC tested $R_L = \infty$	11	14	17.5	10.5	14	18.0	kΩ
R_O	Output resistance (single-ended output)	DC tested		15			15		Ω
f_{3dB}	Bandwidth (-3dB)	T_A = 25°C Test circuit 1		180			180		MHz
R_{IN}	Input resistance			200			200		Ω
C_{IN}	Input capacitance			4			4		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5± 0.5V		3.7			3.7		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.025			0.025		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		1.8			1.8		pA/$\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input)	T_A = 25°C Test Circuit 2							
	$C_S = 0$[1]	Δf = 50MHz Δf = 100MHz Δf = 200MHz		13 20 35			13 20 35		nA nA nA
PSRR	C_S = 1pF Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	Δf = 50MHz Δf = 100MHz Δf = 200MHz DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 3	26	13 21 41 32		23	13 21 41 32		nA nA nA dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 4	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 5	45	65		45	65		dB
PSRR	Power supply rejection ratio (ECL configuration)[2]	f = 0.1MHz Test Circuit 6		23			23		dB
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of 50± 5%[3]	Test Circuit 7	160			160			mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 7		0.8	1.2		0.8	1.8	ns

NOTES:
1. Package parasitic capacitance amounts to about 0 2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20 - 80% rise time. It is guaranteed by - 3dB bandwidth test.

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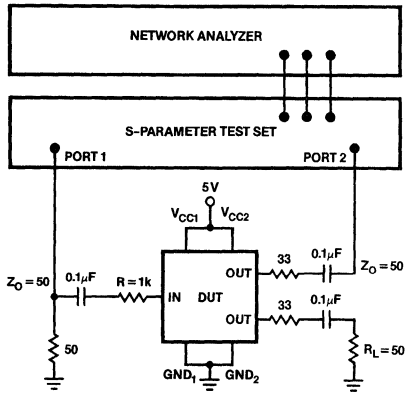
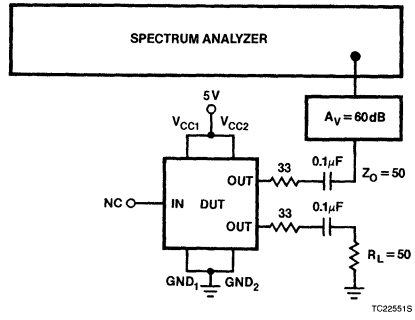
Transimpedance Amplifier (180MHz) NE/SA5211

TEST CIRCUITS



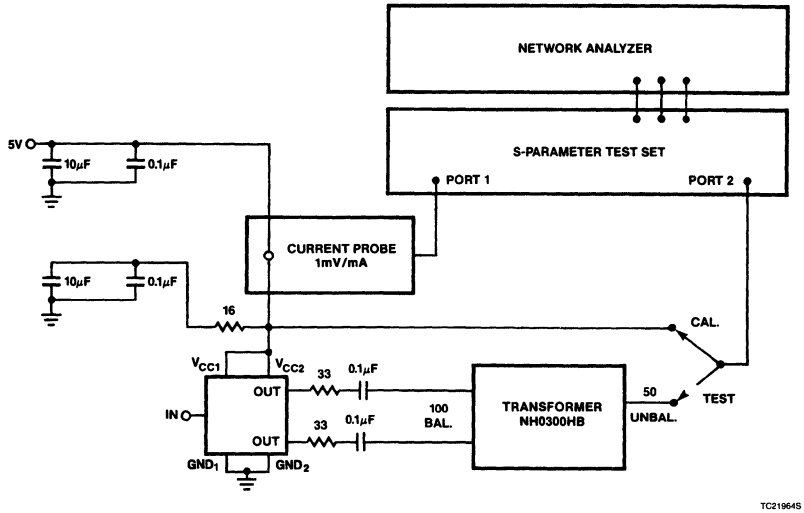
SINGLE-ENDED	DIFFERENTIAL
$R_T \cong \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \times S21 \times R$
$R_O \cong Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1+S22}{1-S22} \right\rvert - 66$

Test Circuit 1

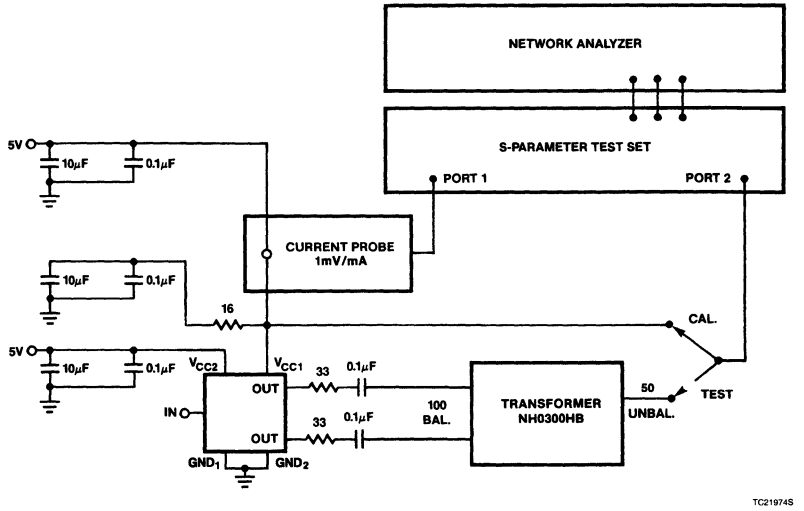


Test Circuit 2

TEST CIRCUITS (Continued)



Test Circuit 3



Test Circuit 4

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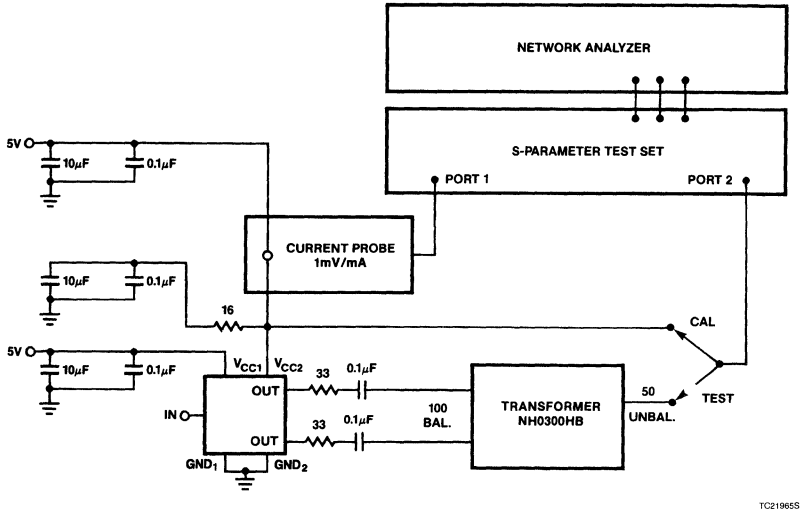
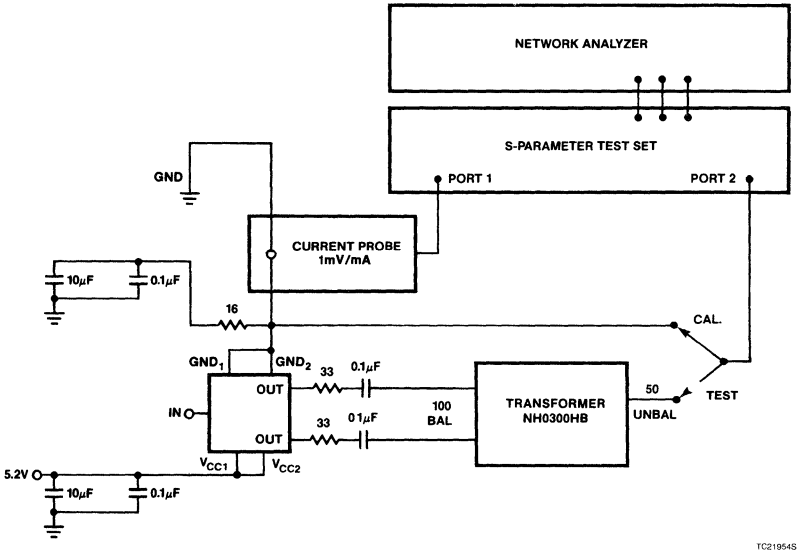
TEST CIRCUITS (Continued)

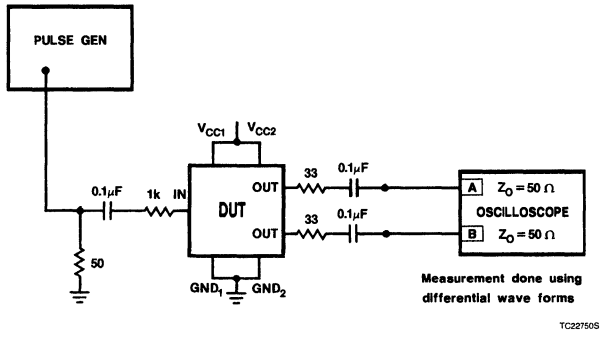


Test Circuit 5



Test Circuit 6

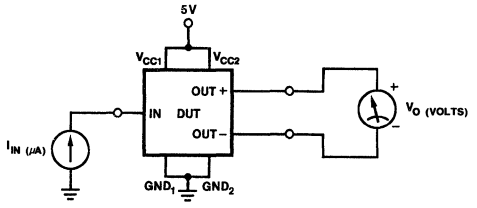
TEST CIRCUITS (Continued)



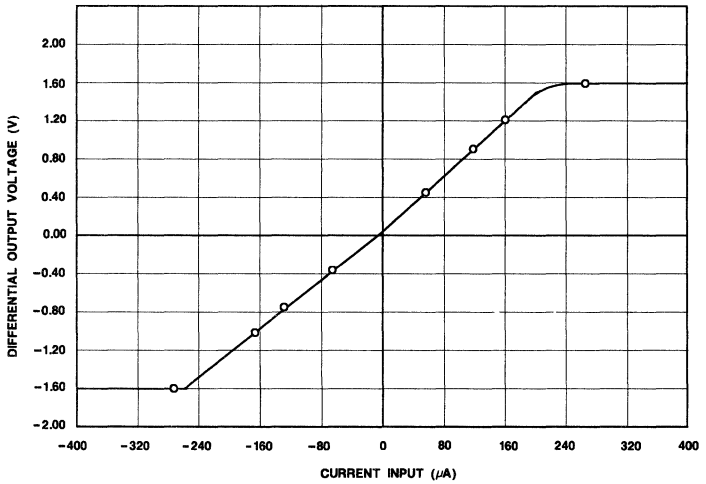
Test Circuit 7

5

TEST CIRCUITS (Continued)



Typical V_O (Differential) vs I_{IN}



NE5211 TEST CONDITIONS

Procedure 1

R_T measured at 15μA
$R_T = (V_{O1} - V_{O2})/(+15\mu A - (-15\mu A))$
Where: V_{O1} Measured at $I_{IN} = +15\mu A$
V_{O2} Measured at $I_{IN} = -15\mu A$

Procedure 2

Linearity = 1 – ABS$((V_{OA} - V_{OB})/(V_{O3} - V_{O4}))$
Where: V_{O3} Measured at $I_{IN} = +30\mu A$
V_{O4} Measured at $I_{IN} = -30\mu A$
$V_{OA} = R_T * (+30\mu A) + V_{O8}$
$V_{OB} = R_T * (-30\mu A) + V_{O8}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +65\mu A$
V_{O8} Measured at $I_{IN} = -65\mu A$

Procedure 4

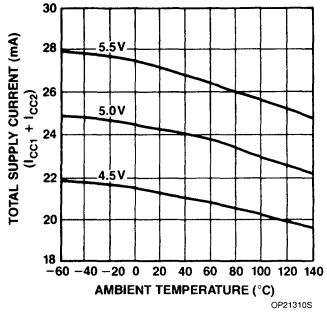
$I_{IN\ MAX}$ Test Pass Conditions:
$V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O5} > 50mV$
Where: V_{O5} Measured at $I_{IN} = +40\mu A$
V_{O6} Measured at $I_{IN} = -40\mu A$
V_{O7} Measured at $I_{IN} = +65\mu A$
V_{O8} Measured at $I_{IN} = -65\mu A$

Test Circuit 8

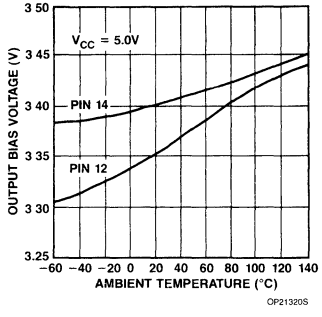
Transimpedance Amplifier (180MHz) NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS

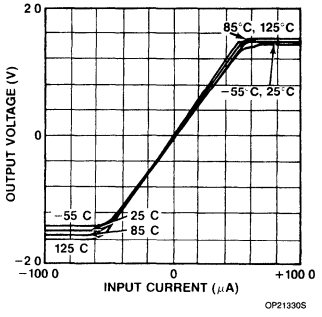
NE5211 Supply Current vs Temperature



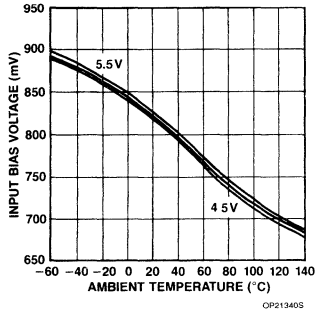
NE5211 Output Bias Voltage vs Temperature



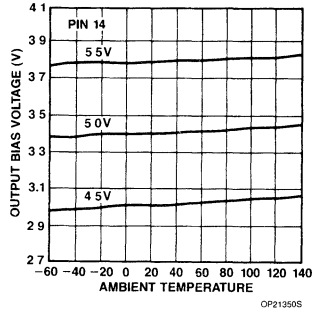
Output Voltage vs Input Current



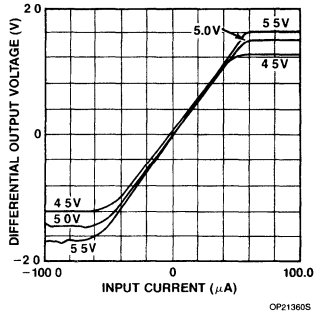
NE5211 Input Bias Voltage vs Temperature



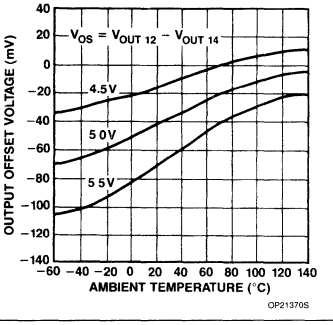
NE5211 Output Bias Voltage vs Temperature



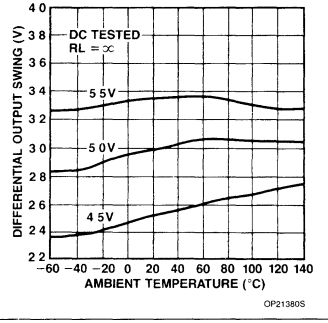
Differential Output Voltage vs Input Current



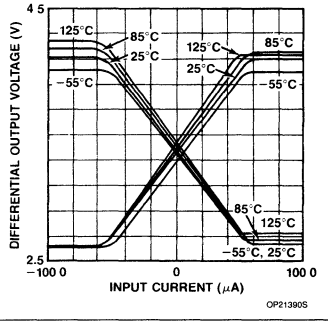
NE5211 Output Offset Voltage vs Temperature



NE5211 Differential Output Swing vs Temperature



Differential Output Voltage vs Input Current



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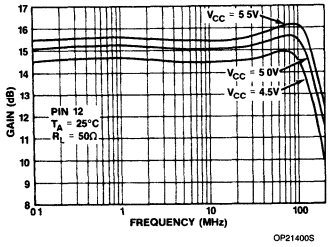
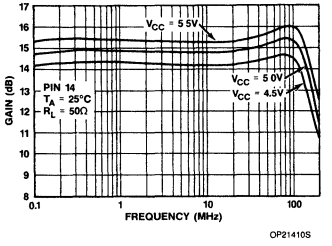
Transimpedance Amplifier (180MHz) NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

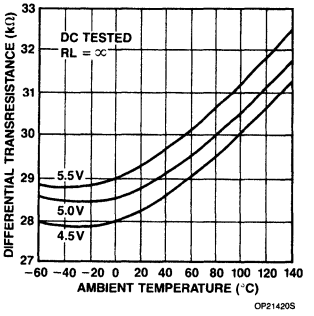
Gain vs Frequency



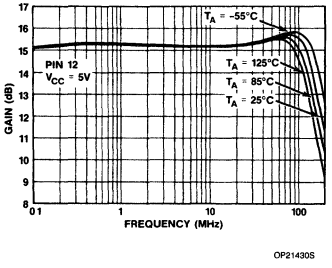
Gain vs Frequency



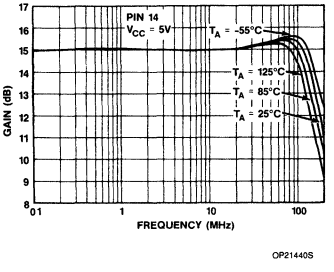
NE5211 Differential Transresistance vs Temperature



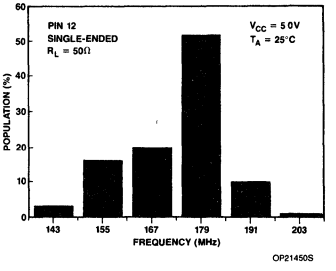
Gain vs Frequency



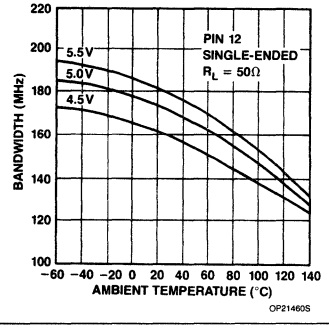
Gain vs Frequency



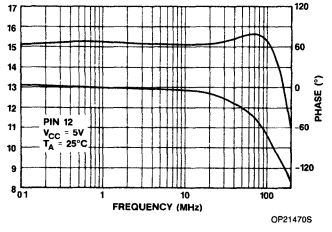
NE5211 Typical Bandwidth Distribution (70 Parts from 3 Wafer Lots)



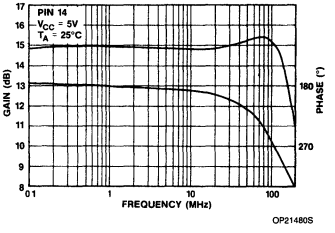
NE5211 Bandwidth vs Temperature



Gain and Phase Shift vs Frequency

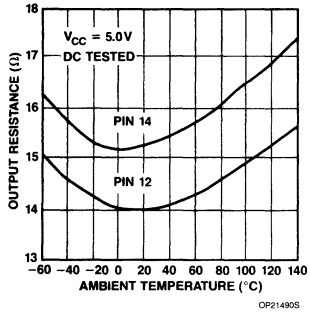


Gain and Phase Shift vs Frequency

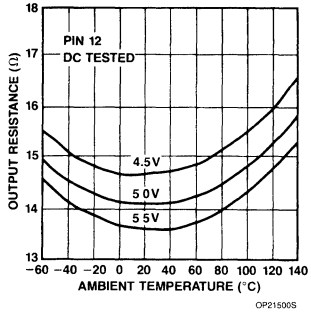


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

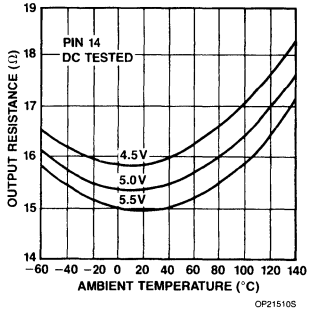
NE5211 Output Resistance vs Temperature



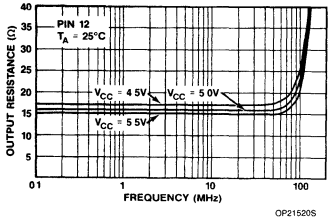
NE5211 Output Resistance vs Temperature



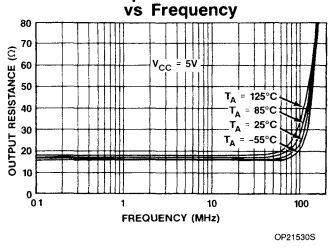
NE5211 Output Resistance vs Temperature



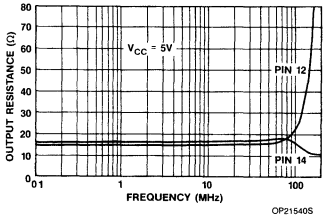
Output Resistance vs Frequency



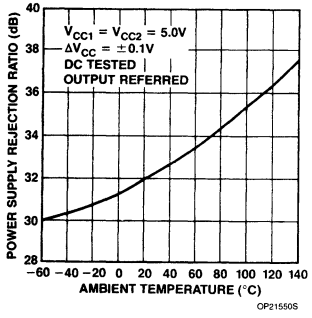
Output Resistance vs Frequency



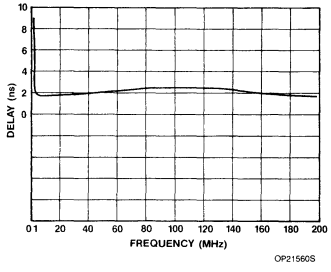
Output Resistance vs Frequency



NE5211 Power Supply Rejection Ratio vs Temperature



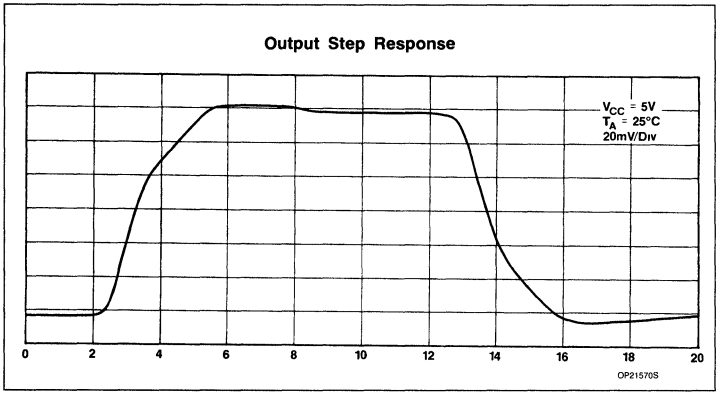
Group Delay vs Frequency



5

Transimpedance Amplifier (180MHz) NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5211 is a wide bandwidth (typically 180MHz) transimpedance amplifier designed primarily for high sensitivity. The maximum input current before output stage clipping occurs at typically 50μA. The NE5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F = 14.4kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT\ (diff)}}{I_{IN}} = 2R_F = 2(14.4k) = 28.8k\Omega.$$

The single-ended transresistance of the amplifier is typically 14.4kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 4pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4k}{71} = 203\Omega.$$

More exact calculations would yield a value of 200Ω

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier,

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}.$$

Assuming typical values for R_F = 14.4kΩ, R_{IN} = 200Ω, C_{IN} = 4pF:

$$f_{-3dB} = \frac{1}{2\pi\ 4pF\ 200} = 200MHz.$$

The operating point of Q1 has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 200Ω then the total input capacitance, C_{IN} = (1 + 4)pF which will lead to only a 20% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 1.8pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 41nA in a 200MHz bandwidth for C_S = 1pF

DYNAMIC RANGE

The electrical dynamic range can be defined as the radio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 60μA and a wideband noise of I_{EQ} = 41nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$= 20\ \log\ \frac{(60 \times 10^{-6})}{(\sqrt{2}\ 41 \times 10^{-9})}$$

$$= 20 \log \frac{(60\mu A)}{(58nA)} = 60dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

$$\text{Energy of one photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h = Planck's Constant = $6\,6 \times 10^{-34}$ Joule sec.

c = speed of light = 3×10^{8} mt/sec

c/λ = optical frequency

$$\text{No. of incident photons/sec} = \frac{\frac{P}{hc}}{\lambda} \text{ where P = optical incident power}$$

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{\frac{P}{hc}}{\lambda}$$

Where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{\frac{P}{hc}}{\lambda} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = $1\,6 \times 10^{-19}$ Coulombs

$$\text{Responsivity } R = \frac{\frac{\eta \cdot e}{hc}}{\lambda} \text{ Amp/watt}$$

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{i_{eq}}{qB} = \frac{41 \times 10^{-9}}{(1.6 \times 10^{-19})\ (200 \times 10^{6})} = 1281$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is·

$$P_{avMIN} = 12 \frac{hc}{\lambda} B\ Z = 12\ 2\,3 \times 10^{-19}$$

200×10^{6} 1281 = 707nW = −31.5dBm,

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

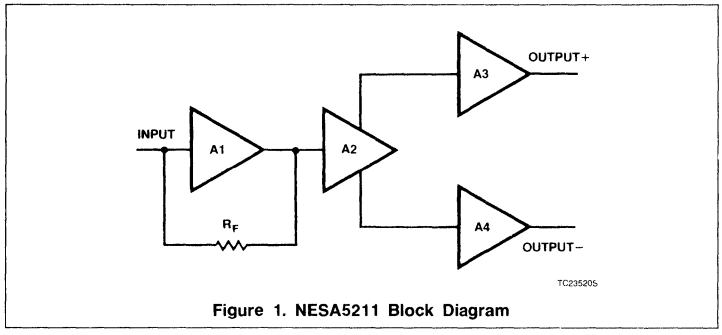


Figure 1. NESA5211 Block Diagram

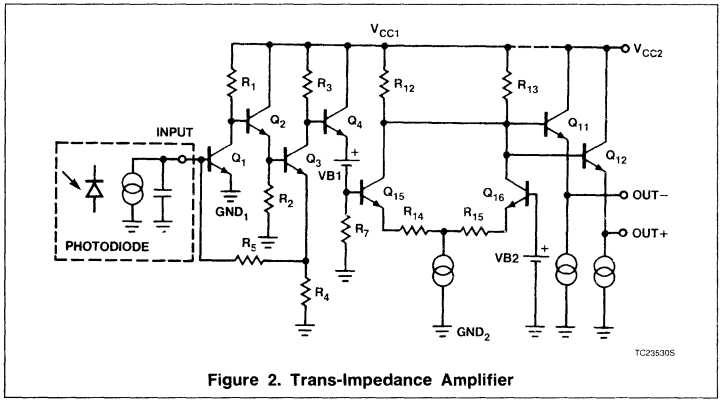


Figure 2. Trans-Impedance Amplifier

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{707 \times 10^{-9} \times 1\,6 \times 10^{-19}}{2\,3 \times 10^{-19}}$$

$$= 492nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 60\mu A$, the maximum mean optical power is·

$$P_{avMAX} = \frac{hc\ I_{avMAX}}{\lambda\ q} = \frac{2\,3 \times 10^{-19}}{1\,6 \times 10^{-19}} 60 \times 10^{-6}$$

$$= 86mW \text{ or } -10\,6dBm$$

Thus the optical dynamic range, D_o is

$$D_o = P_{avMAX} - P_{avMIN} = -31\ 5 - (-10\ 6)$$
$$= 20.8dB$$

This represents the maximum limit attainable with the NE5211 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout such that Ground 1 and Ground 2 have very low impedance paths have produced the best results This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1 Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz The easiest way to realize that the part is not functioning normally is to measure

1 S. D Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3

Transimpedance Amplifier (180MHz) NE/SA5211

the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5211 and the NE5214 post amplifier. For more information on this circuit, please refer to Application Brief AB1432.

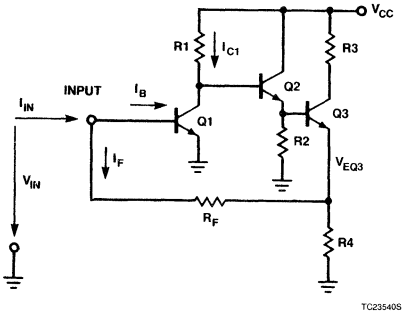


Figure 3. Shunt-Series Input Stage

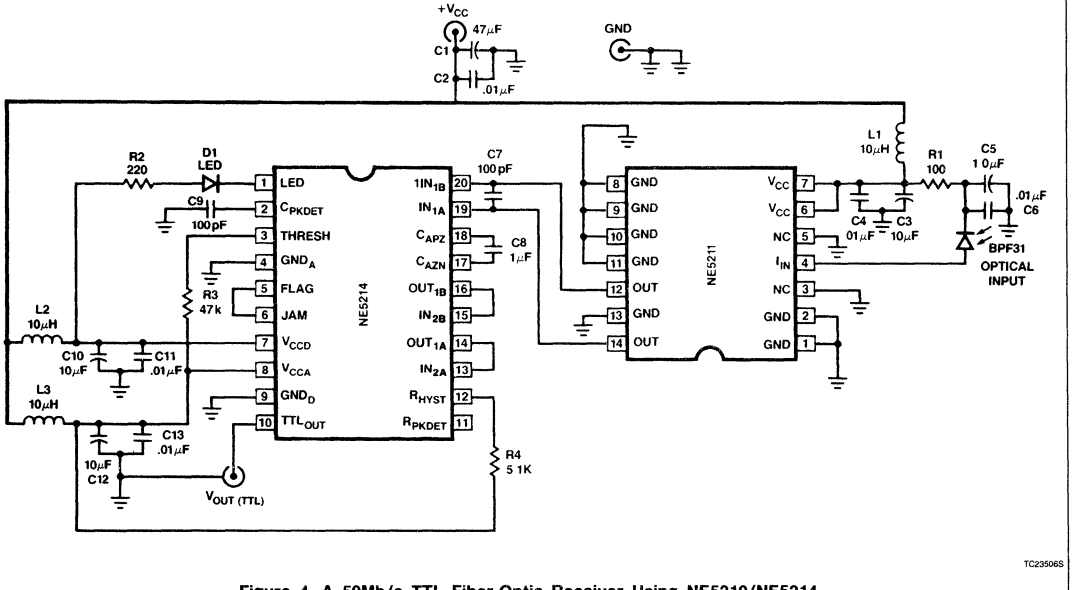


Figure 4. A 50Mb/s TTL Fiber-Optic Receiver Using NE5210/NE5214

Signetics

NE/SA/SE5212
Transimpedance Amplifier (140MHz)

Product Specification

Linear Products

DESCRIPTION

The NE/SA/SE5212 is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

FEATURES

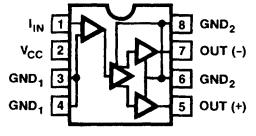
- **Extremely low noise: 2.5pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 140MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High-power supply rejection ratio**
- **14kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wideband gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

N, FE, D Packages



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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5212N
8-Pin Plastic SO	0 to +70°C	NE5212D
8-Pin Ceramic DIP	0 to +70°C	NE5212FE
8-Pin Plastic SO	−40°C to +85°C	SA5212D
8-Pin Plastic DIP	−40°C to +85°C	SA5212N
8-Pin Ceramic DIP	−40°C to +85°C	SA5212FE
8-Pin Plastic DIP	−55°C to +125°C	SE5212N
8-Pin Ceramic DIP	−55°C to +125°C	SE5212FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5212	SA5212	SE5212	
V_{CC}	Power Supply	6	6	6	V
$P_{D\ MAX}$	Power dissipation, $T_A = 25°C$ (still air)[1]				
	8-Pin Plastic DIP	1100	1100	1100	mW
	8-Pin Plastic SO	750	750	750	mW
	8-Pin Cerdip	750	750	750	mw
$I_{IN\ MAX}$	Maximum input current[2]	5	5	5	mA
T_A	Operating ambient temperature range	0 to 70	−40 to 85	−55 to 125	°C
T_J	Operating junction	−55 to 150	−55 to 150	−55 to 150	°C
T_{STG}	Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   8-Pin Plastic DIP: 110°C/W
   8-Pin Plastic SO: 160°C/W
   8-Pin Cerdip: 165°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	4.5 to 5.5	V
T_A	Ambient temperature ranges		
	NE Grade	0 to +70	°C
	SA Grade	−40 to +85	°C
	SE Grade	−55 to +125	°C
T_J	Junction temperature ranges		
	NE Grade	0 to +90	°C
	SA Grade	−40 to +105	°C
	SE Grade	−55 to +145	°C

DC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified. Typical data applies at $V_{CC} = 5V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	2.5	3.3	3.8	V
V_{OS}	Output offset voltage				80			120	mV
I_{CC}	Supply current		21	26	32	20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 6, Procedure 2	±60	±80		±40	±80		μA
$I_{N\ MAX}$	Maximum input current overload threshold	Test Circuit 6, Procedure 4	±80	±120		±60	±120		μA

AC ELECTRICAL CHARACTERISTICS Minimum and Maximum limits apply over operating temperature range at V_{CC} = 5V, unless otherwise specified. Typical data applies at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 6, Procedure 1	9.8	14	18.2	9.0	14	19	kΩ
R_O	Output resistance (differential output)	DC tested	14	30	42	14	30	46	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	4.9	7	9.1	4.5	7	9.5	kΩ
R_O	Output resistance (single-ended output)	DC tested	7	15	21	7	15	23	Ω
f_{3dB}	Bandwidth (–3dB)	Test Circuit 1 D package, T_A = 25°C N, FE packages, T_A = 25°C	100 100	140 120		100 100	140 120		MHz MHz
R_{IN}	Input resistance		75	110	143	70	110	150	Ω
C_{IN}	Input capacitance			10	15		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5 ±0.5V		9 6			9.6		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.05			0.05		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		2.5			2.5		pA/$\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0$[1]	T_A = 25°C Test Circuit 2 Δf = 50MHz Δf = 100MHz Δf = 200MHz		20 27 40			20 27 40		nA nA nA
	C_S = 1pF	Δf = 50MHz Δf = 100MHz Δf = 200MHz		22 32 52			22 32 52		nA nA nA
PSRR	Power supply rejection ratio[2]	Any package DC tested ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	26	33		20	33		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	Any package f = 0 1MHz[1] Test Circuit 4		23			23		dB
$V_{O\ MAX}$	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 6, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of 50 ±5%[3]	Test Circuit 5		325			325		mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 5		2.0			2.0		ns

NOTES:
1 Package parasitic capacitance amounts to about 0 2pF
2 PSRR is output referenced and is circuit board layout dependent at higher frequencies For best performance use RF filter in V_{CC} line
3 Guaranteed by linearity and over load tests
4 t_R defined as 20 – 80% rise time It is guaranteed by –3dB bandwidth test

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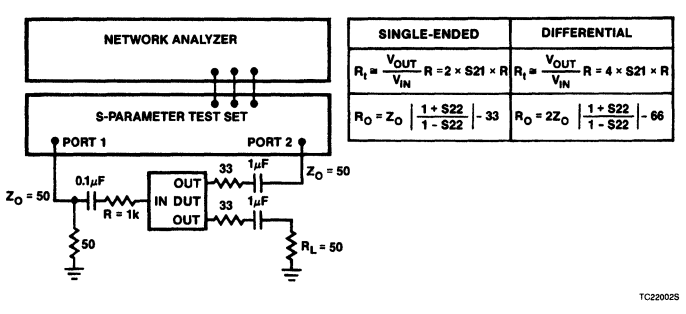
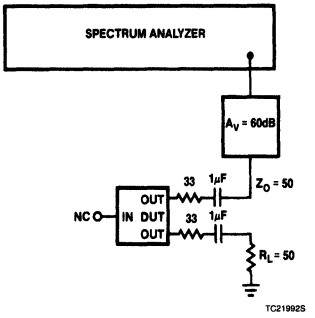
Transimpedance Amplifier (140MHz) NE/SA/SE5212

TEST CIRCUITS

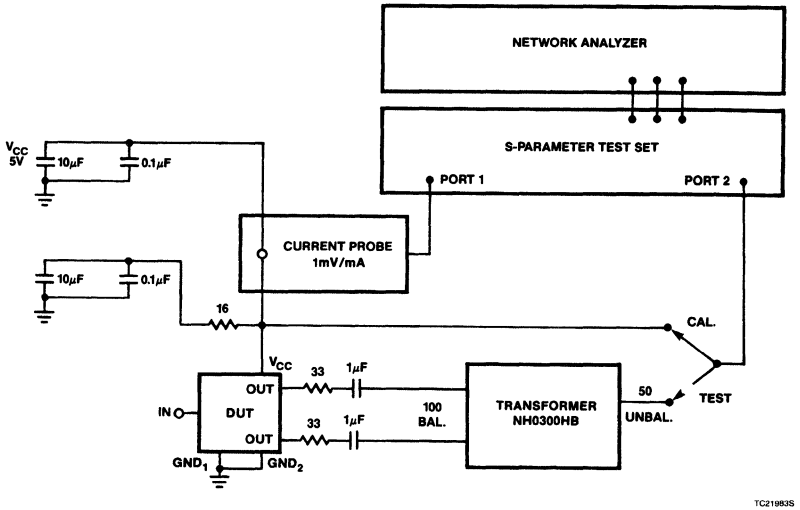


SINGLE-ENDED	DIFFERENTIAL
$R_t \cong \frac{V_{OUT}}{V_{IN}} R = 2 \times S21 \times R$	$R_t \cong \frac{V_{OUT}}{V_{IN}} R = 4 \times S21 \times R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$

Test Circuit 1

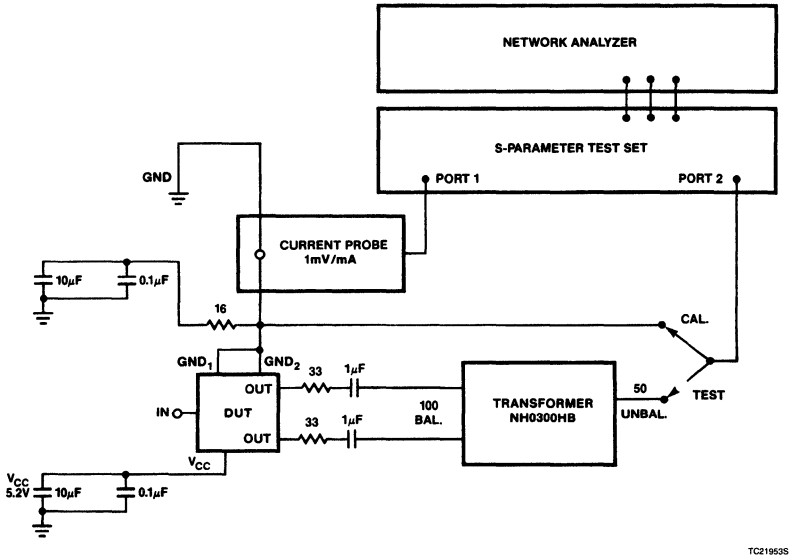


Test Circuit 2

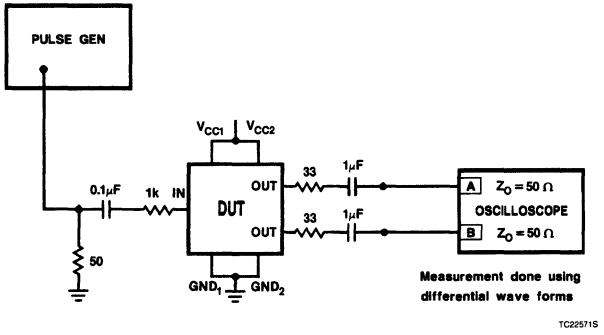


Test Circuit 3

TEST CIRCUITS (Continued)

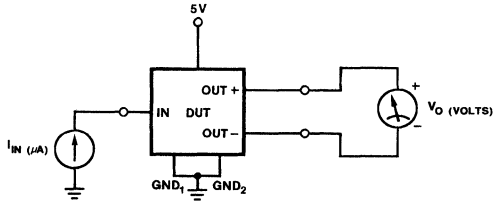


Test Circuit 4



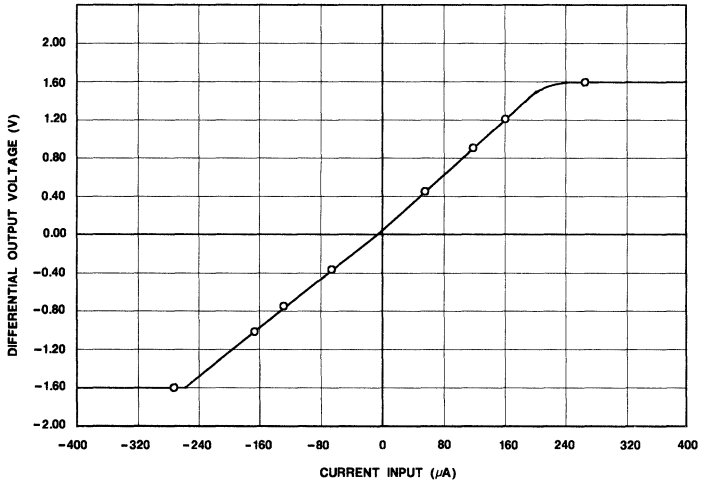
Test Circuit 5

TEST CIRCUITS (Continued)



TC23462S

Typical V_O (Differential) vs I_{IN}



OP20990S

NE5212 TEST CONDITIONS

Procedure 1

R_T measured at 30μA
$R_T = (V_{O1} - V_{O2})/(+30\mu A - (-30\mu A))$
Where: V_{O1} Measured at $I_{IN} = +30\mu A$
V_{O2} Measured at $I_{IN} = -30\mu A$

Procedure 2

Linearity = 1 – ABS(($V_{OA} - V_{OB}$/($V_{O3} - V_{O4}$))
Where: V_{O3} Measured at $I_{IN} = +60\mu A$
V_{O4} Measured at $I_{IN} = -60\mu A$
$V_{OA} = R_T$ * (+60μA) + V_{O8}
$V_{OB} = R_T$ * (–60μA) + V_{O8}

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

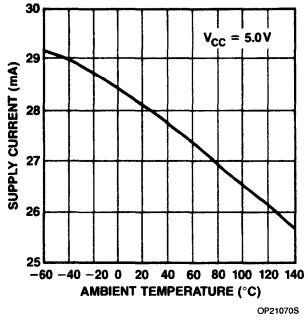
Procedure 4

$I_{IN\ MAX}$ Test Pass Conditions:
$V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O5} > 50mV$
Where. V_{O5} Measured at $I_{IN} = +80\mu A$
V_{O6} Measured at $I_{IN} = -80\mu A$
V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

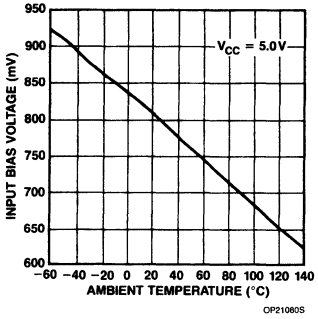
Test Circuit 6

TYPICAL PERFORMANCE CHARACTERISTICS

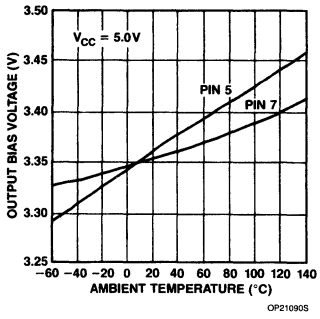
NE5212 Supply Current vs Temperature



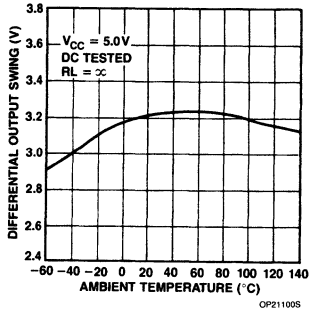
NE5212 Output Bias Voltage vs Temperature



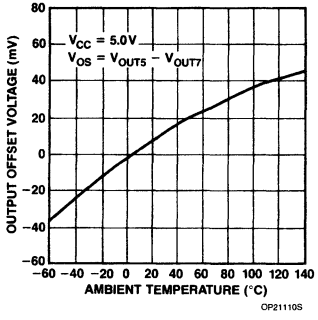
NE5212 Output Bias Voltage vs Temperature



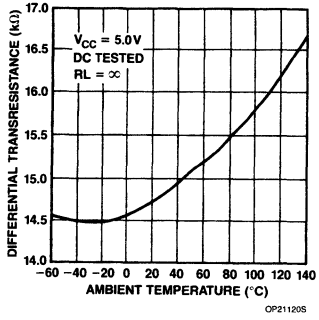
NE5212 Differential Output Swing vs Temperature



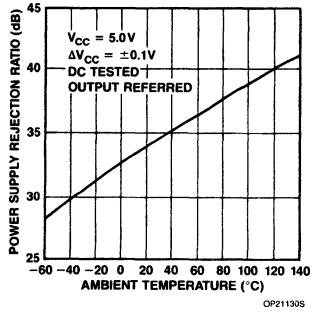
NE5212 Output Offset Voltage vs Temperature



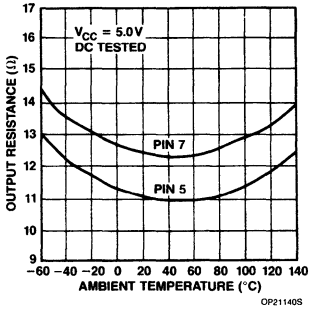
NE5212 Differential Transresistance vs Temperature



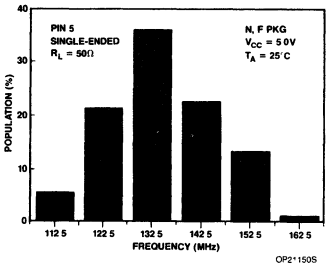
NE5212 Power Supply Rejection Ratio vs Temperature



NE5212 Output Resistance vs Temperature



NE5212 Typical Bandwidth Distribution (75 Parts from 3 Wafer Lots)



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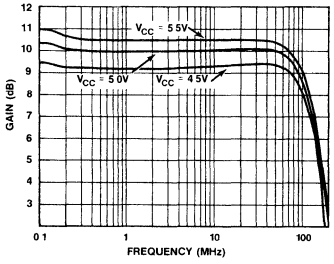
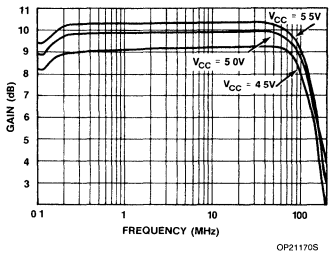
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency



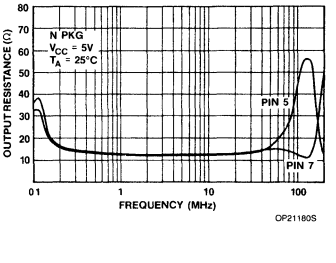
OP21160S

Gain vs Frequency



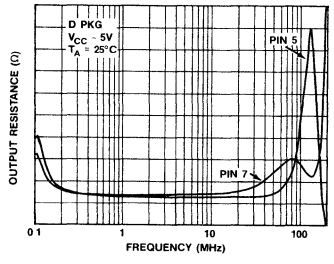
OP21170S

Output Resistance vs Frequency



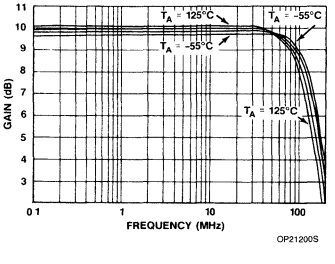
OP21180S

Output Resistance vs Frequency



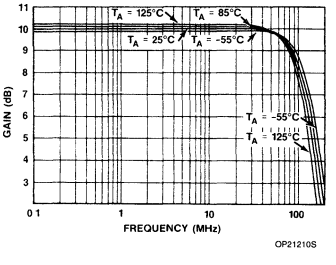
OP21190S

Gain vs Frequency OP21230S



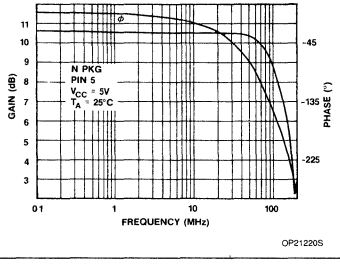
OP21200S

Gain vs Frequency OP21240S



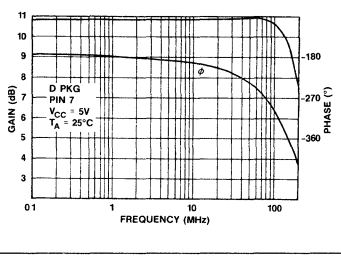
OP21210S

Gain and Phase Shift vs Frequency

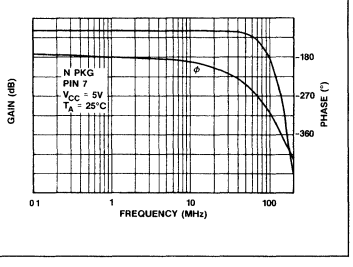


OP21220S

Gain and Phase Shift vs Frequency

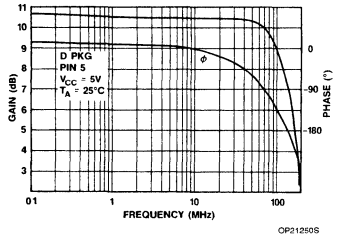


Gain and Phase Shift vs Frequency

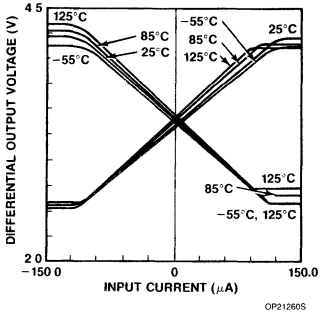


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

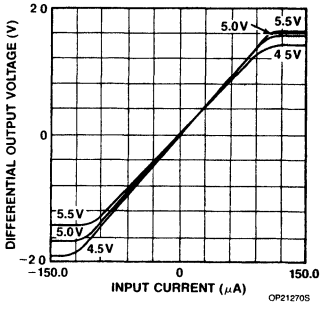
Gain and Phase Shift vs Frequency



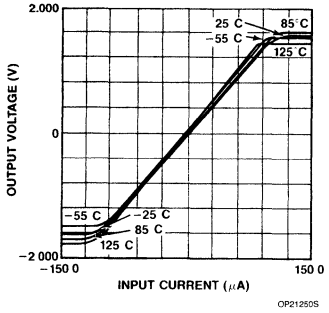
Differential Output Voltage vs Input Current



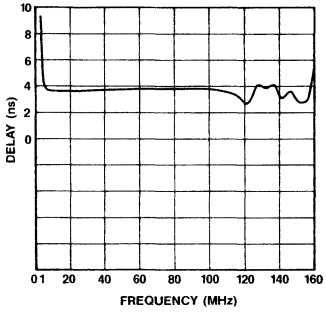
Differential Output Voltage vs Input Current



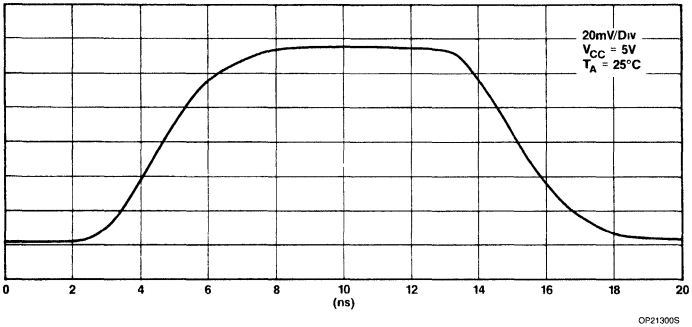
Output Voltage vs Input Current



Group Delay vs Frequency



Output Step Response



Transimpedance Amplifier (140MHz) NE/SA/SE5212

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber optic receivers The NE5212 is a wide bandwidth (typically 130MHz) transimpedance amplifier designed primarily for high sensitivity The maximum input current before output stage clipping occurs at typically 120μA The NE5212 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry A block diagram of the circuit is shown in Figure 1 The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, $R_F = 7.2k\Omega$ The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(7\ 2k) = 14\ 4k\Omega$$

The single-ended transresistance of the amplifier is typically 7 2kΩ

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1 The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2} The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage The output impedance is about 17Ω single-ended For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

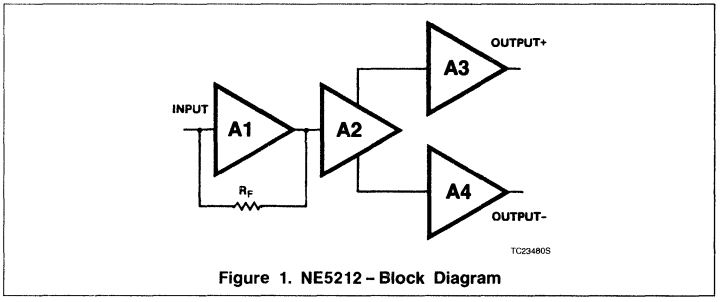


Figure 1. NE5212 – Block Diagram

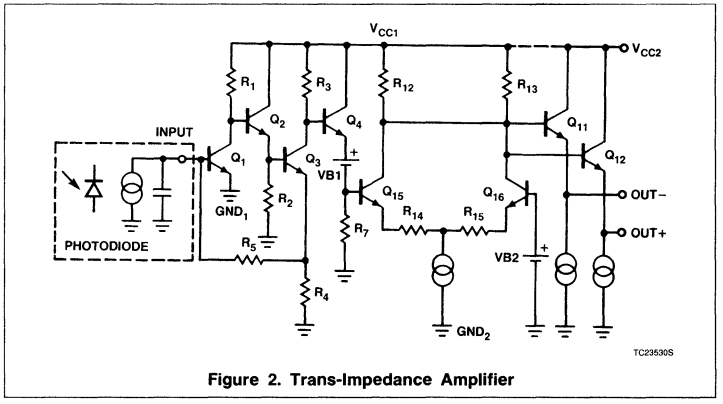


Figure 2. Trans-Impedance Amplifier

BANDWIDTH CALCULATIONS:

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 10pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as.

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{7\ 2k}{70} = 103\Omega.$$

More exact calculations would yield a value of 110Ω

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}.$$

Assuming typical values for $R_F = 7.2k\Omega$, $R_{IN} = 110\Omega$, $C_{IN} = 10pF$:

$$f_{-3dB} = \frac{1}{2\pi\ 110\ 10 \times 10^{-12}} = 145MHz.$$

The operating point of Q1 has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, $R_{IN} = 110\Omega$ then the total input capacitance, $C_{IN} = (1 + 10)$ pF which will lead to only a 9% bandwidth reduction.

NOISE

Most of the currently installed fiber optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very im-

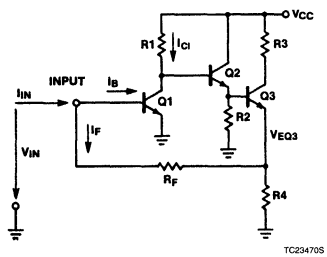


Figure 3. Shunt-Series Input Stage

portant. The input stage achieves a low input referred noise current (spectral density) of 2.5pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input RMS noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 52nA in a 200MHz bandwidth for C_S = 1pF.

DYNAMIC RANGE:

The electrical dynamic range can be defined as the radio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming $I_{INMAX} = 120\mu A$ and a wideband noise of $I_{EQ} = 52nA_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$= 20 \log \frac{(120 \times 10^{-6})}{(\sqrt{2}\ 52 \times 10^{-9})}$$

$$= 20 \log \frac{(120\mu A)}{(73nA)} = 64dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

$$\text{Energy of one photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 mt/sec

c/λ = optical frequency

$$\text{No. of incident photons/sec} = \frac{P}{\frac{hc}{\lambda}} \text{ where}$$

P = optical incident power

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{P}{\frac{hc}{\lambda}}$$

Where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hc}{\lambda}} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\eta \cdot e}{\frac{hc}{\lambda}} \text{ Amp/watt}$$

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:

$$Z = \frac{I_{eq}}{qB} = \frac{52 \times 10^{-9}}{(1.6 \times 10^{-19})\ (200 \times 10^6)} = 1625$$

where Z is the ratio of RMS noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \frac{hc}{\lambda} B\ Z = 12\ 2.3 \times 10^{-19}$$

$200 \times 10^6\ 1625 = 897nW = -30.5dBm$,

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum

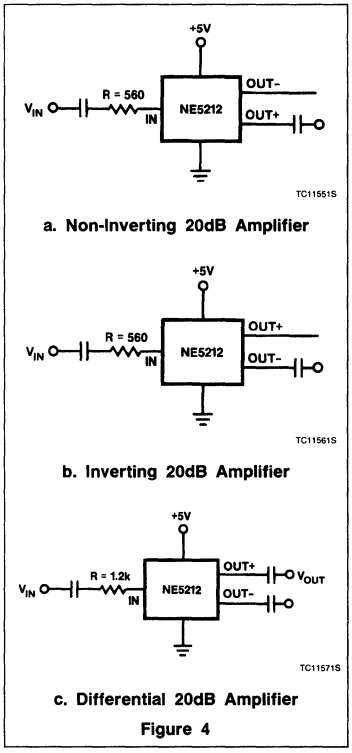


Figure 4

input current to the NE5212, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{897 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 624nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 120\mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc\ I_{avMAX}}{\lambda\ q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} = 120 \times 10^{-6}$$

$$= 86mW \text{ or } -7.6 \text{ dBm.}$$

Thus the optical dynamic range, D_o is:

$$D_o = P_{avMAX} - P_{avMIN} = -30.5 - (-7.6) = 22.8dB.$$

This represents the maximum limit attainable with the NE5212 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

[1] S. D. Personick, *Optical Fiber Transmission Systems,* Plenum Press, NY, 1981, Chapter 3

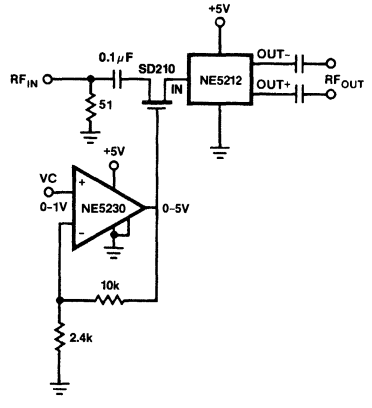


Figure 5. Variable Gain Circuit

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response Since the NE5212 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout such that Ground 1 and Ground 2 have very low impedance paths have produced the best results. This was acomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance The first of these is the use of a well-regulated power supply The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{cc1} and V_{cc2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{cc1} and V_{cc2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible

BASIC CONFIGURATION

A trans resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain The NE5212 has a differential transresistance of 14kΩ typically and a single-ended transresistance of 7kΩ typically The device has two outputs. inverting and non-inverting. The output voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 4 shows some basic configurations.

VARIABLE GAIN

Figure 5 shows a variable gain circuit using the NE5212 and the NE5230 low voltage op amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the NE5212. This circuit has a distortion of less than 1% and a 25dB range, from −42.2dBm to −15.9dBm at 50MHz, and a 45dB range, from −60dBm to −14.9dBm at 10MHz with 0 to 1V of control voltage at V_C.

16MHz CRYSTAL OSCILLATOR

Figure 6 shows a 16MHz crystal oscillator operating in the series resonant mode using the NE5212 The non-inverting input is fed back to the input of the NE5212 in series with a 2pF capacitor. The output is taken from the inverting output.

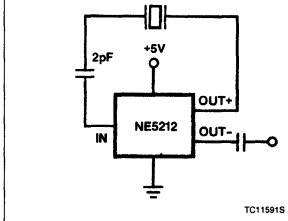


Figure 6. 16MHz Crystal Oscillator

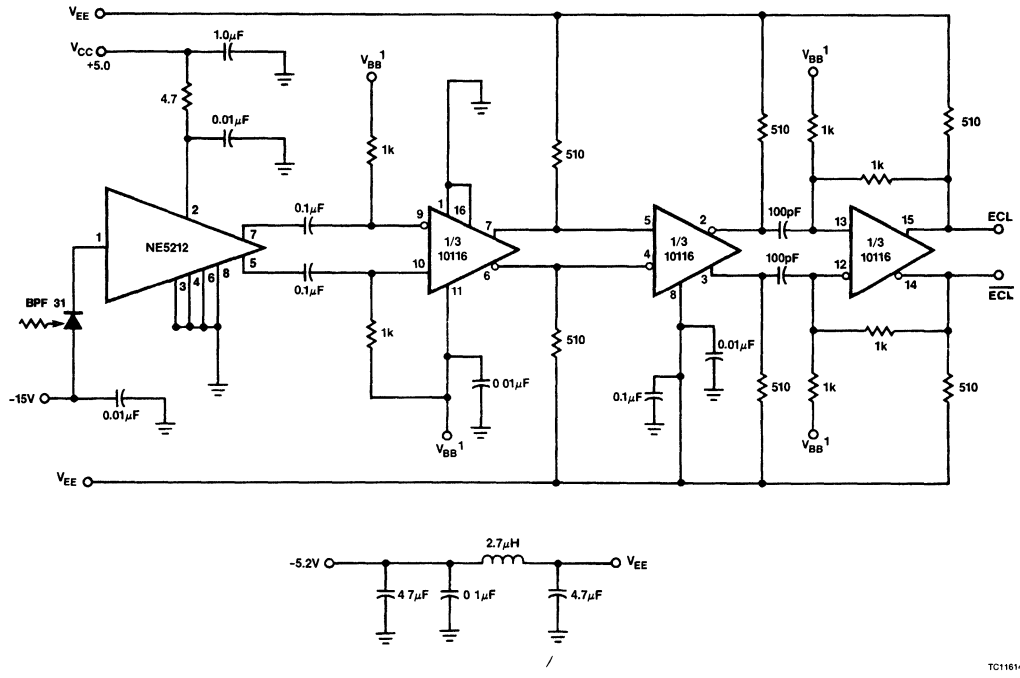
DIGITAL FIBER OPTIC RECEIVER

Figures 7 and 8 show a fiber optic receiver using off-the-shelf components.

The receiver shown in Figure 7 uses the NE5212, the Signetics 10116 ECL line receiver, and Philips/Amperex BPF31 PIN diode. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

Figure 8 depicts a TTL receiver using the NE5212 and the NE5214 fast amplifier system along with the Philips/Amperex PIN diode. The system shown is optimized for 50 Mb/s Non Return to Zero (NRZ) data. A link status indication is provided along with a jamming function when the input level is below a user-programmable threshold level.

Transimpedance Amplifier (140MHz) NE/SA/SE5212



NOTE:
1 Tie all V_{BB} points together

Figure 7. ECL Fiber Optic Receiver

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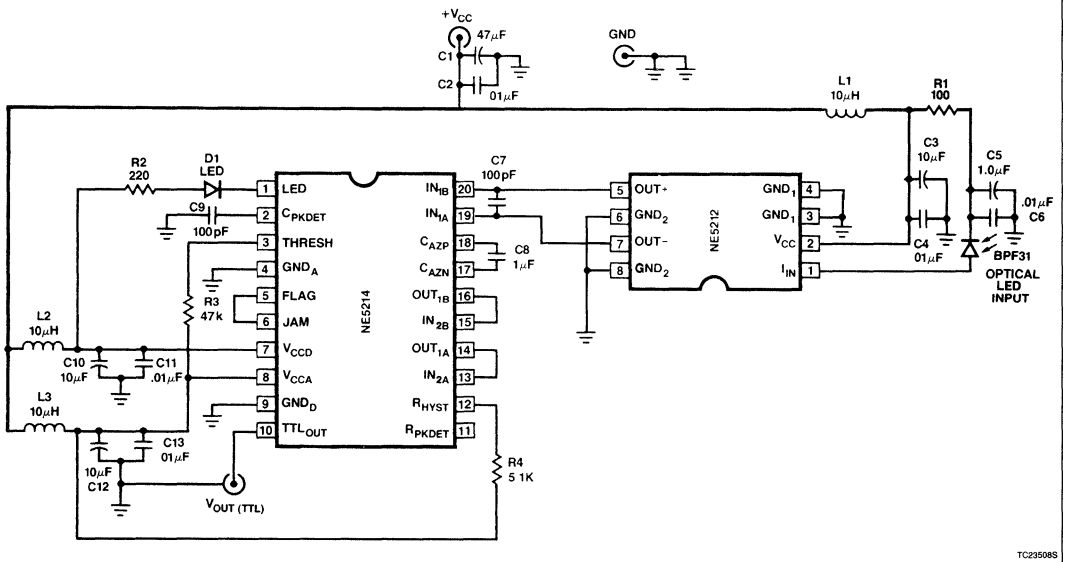


Figure 8. A 50Mb/S TTL Digital Fiber Optic Receiver

Signetics

NE/SA5214
Postamplifier with Link Status Indicator

Preliminary Specification

Linear Products

DESCRIPTION

THE NE/SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5214 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5214 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE/SA5212/5214 or NE/SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/5212 preamplifier family**
- **Wideband operation: typical 75MHz (100MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Low signal output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally ON with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**

APPLICATIONS

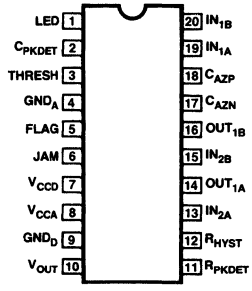
- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Metropolitan Area Networks (MAN)**
- **Synchronous Optical Networks (SONET)**
- **RF limiter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5214D
20-Pin Plastic SOL	-40°C to +85°C	SA5214D

PIN CONFIGURATION

D[1] Package



TOP VIEW

CD15320S

NOTE:
1 SOL — Released in large SO package only

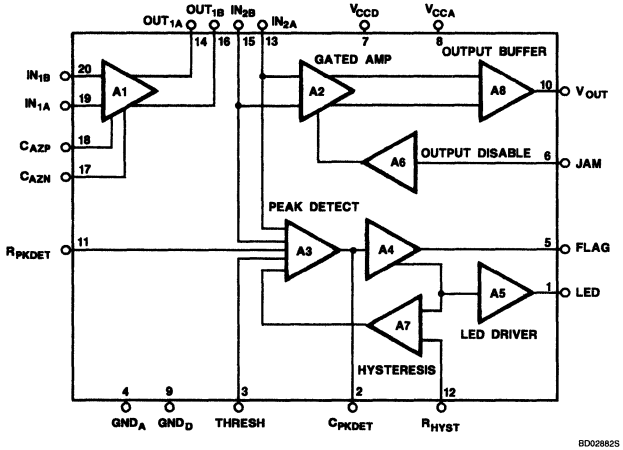
PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver Open collector output transistor with 125Ω series limiting resistor An above threshold signal turns this transistor ON
2	C_{PKDET}	Capacitor for the peak detector The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor
3	THRESH	Peak detector threshold resistor The value of this resistor determines the threshold level of the peak detector
4	GND_A	Device analog ground pin
5	FLAG	Peak detector digital output When this output is LOW, there is data present above the threshold This pin is normally connected to the JAM pin and has a TTL fanout of two
6	JAM	Input to inhibit data flow Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW This pin is normally connected to the FLAG pin and is TTL-compatible
7	V_{CCD}	Power supply pin for the digital portion of the chip
8	V_{CCA}	Power supply pin for the analog portion of the chip
9	GND_D	Device digital ground pin
10	V_{OUT}	TTL output pin with a fanout of five
11	R_{PKDET}	Peak detector current resistor The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}

5

PIN CONFIGURATION (cont.)

PIN NO.	SYMBOL	DESCRIPTION
12	R_{HYST}	Peak detector hysteresis resistor The value of this resistor determines the amount of hysteresis in the peak detector
13	IN_{2A}	Non-inverting input to amplifier A2
14	OUT_{1A}	Non-inverting output of amplifier A1
15	IN_{2B}	Inverting input to amplifier A2
16	OUT_{1B}	Inverting output of amplifier A1
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal) The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal) The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1
20	IN_{1B}	Inverting input of the preamp A1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	−0.5 to 5.5	−0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	0 to +95	−40 to +110	°C
P_D	Power dissipation	250	250	mW

5

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/− inputs)		3.16	3.4	3.63	3.13	3.4	3.65	V
V_{O1}	A1 output bias voltage (+/− outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (V_{CCA}, V_{CCD})	$V_{CCA} = V_{CCD} = 4.75$ to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	$\Delta V_{CM} = 200mV$		60			60		dB
V_{I2}	A2 input bias voltage (+/− inputs)		3.59	3.7	3.85	3.56	3.7	3.86	V
V_{OH}	High-level TTL output voltage	$I_{OH} = -200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	$V_{OUT} = 2.4V$		−40	−26		−40	−24.4	mA
I_{OL}	Low-level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA

DC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{OS}	Short-circuit TTL output current	$V_{OUT} = 0.0V$		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	$V_{IJ} = 2.7V$			20			30	μA
I_{ILJ}	Low-level jam input current	$V_{IJ} = 0.4V$	-450	-240		-485	-240		μA
V_{OHF}	High-level flag output voltage	$I_{OH} = -80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	$V_{OUT} = 2.4V$		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	$V_{OUT} = 0.4V$	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	$V_{OUT} = 0.0V$	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	$V_{LED} = 3.0V$	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single ended)	Test CIrcuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF

AC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage	Test circuit		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH} = 47k		12			12		mV_{P-P}
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	$50mV_{P-P}$, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$	2.5				2.5		%

NOTE:
1 The NE/SA5214 is capable of detecting a much lower input level Operation under $12mV_{P-P}$ cannot be guaranteed by present day automatic testers

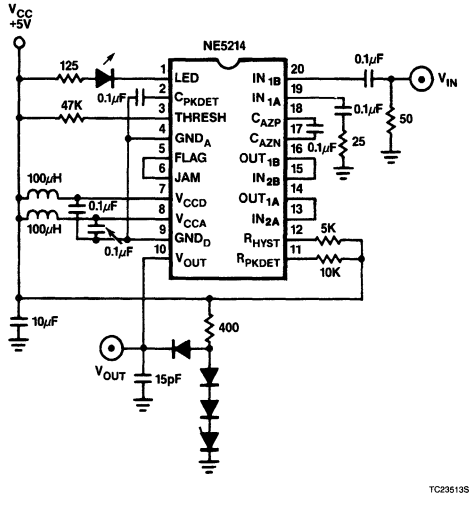
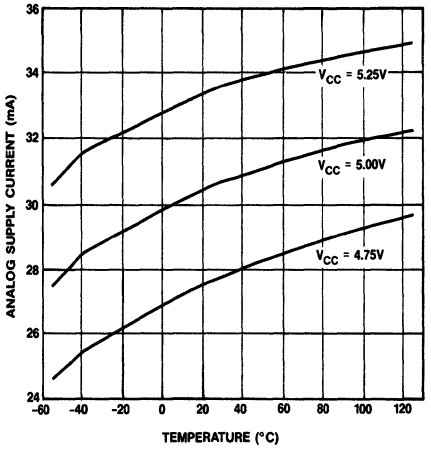


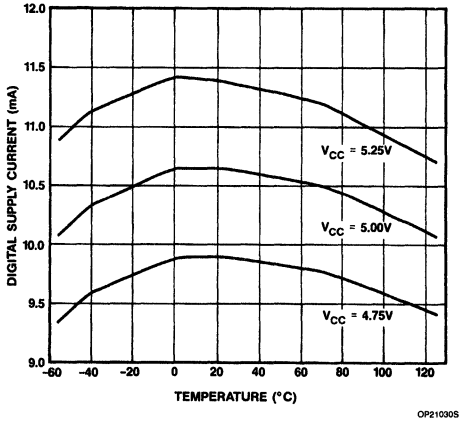
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

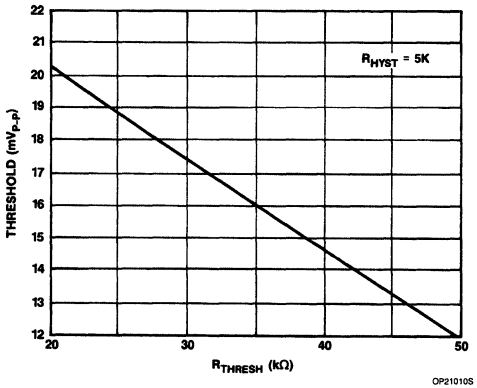
Analog Supply Current vs Temperature



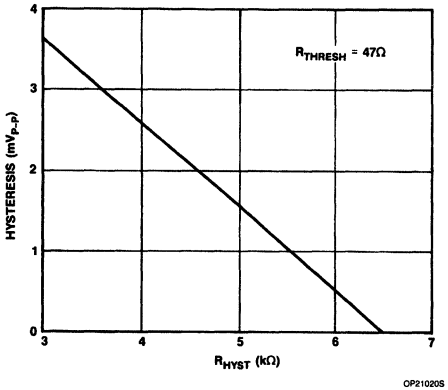
Digital Supply Current vs Temperature



Threshold Voltage vs R_{THRESH}



Hysteresis Voltage vs R_{HYST}



THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5214 postamplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

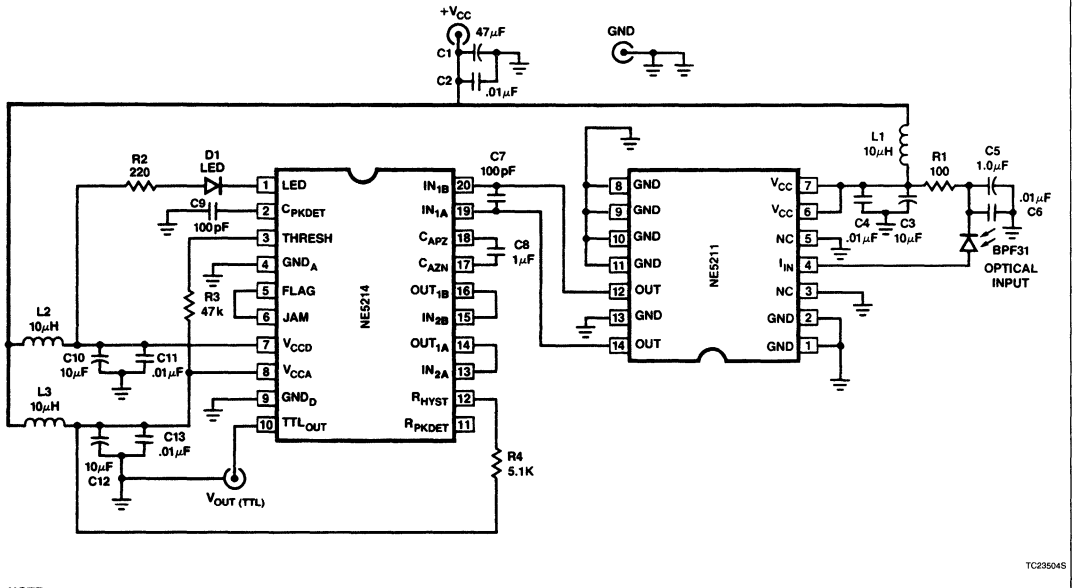
The NE5214 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5214 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5214 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5214 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et al.

A typical application of the NE5214 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to AB 1432.



NOTE:
The NE5211/NE5214 combination can operate at data rates in excess of 100Mb/s NRZ

Figure 2. A 50Mb/s Fiber Optic Receiver

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Signetics

NE/SA5217
Fiber Optic Postamplifier with Link Status Indicator

Objective Specification

Linear Products

DESCRIPTION

THE NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible, instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmidt trigger function by connecting two external capacitors. The result is that a much longer string of 1's and 0's, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5217 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The NE/SA5212/5217 or NE/SA5211/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/5212 preamplifier family**
- **Wideband operation: typical 75MHz (100MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Low signal output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally ON with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**

APPLICATIONS

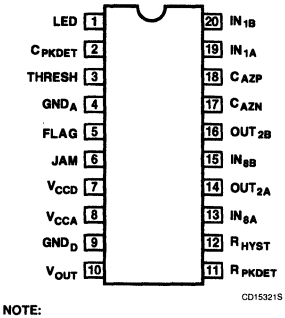
- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Metropolitan Area Networks (MAN)**
- **Synchronous Optical Networks (SONET)**
- **RF limiter**
- **Good for 2^{23}-1 pseudo random number sequence**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5217D
20-Pin Plastic SOL	-40°C to +85°C	SA5217D

PIN CONFIGURATION

D[1] Package



CD15321S

NOTE:
1 SOL — Released in large SO package only

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver Open collector output transistor with 125Ω series limiting resistor An above threshold signal turns this transistor ON
2	C_{PKDET}	Capacitor for the peak detector The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor
3	THRESH	Peak detector threshold resistor The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin
5	FLAG	Peak detector digital output When this output is LOW, there is data present above the threshold This pin is normally connected to the JAM pin and has a fanout of two.
6	JAM	Input to inhibit data flow Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, Low This pin is normally connected to the FLAG pin and is TTL-compatible
7	V_{CCD}	Power supply pin for the digital portion of the chip
8	V_{CCA}	Power supply pin for the analog portion of the chip
9	GND_D	Device digital ground pin
10	V_{OUT}	TTL output pin with a fanout of five
11	R_{PKDET}	Peak detector current resistor The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}

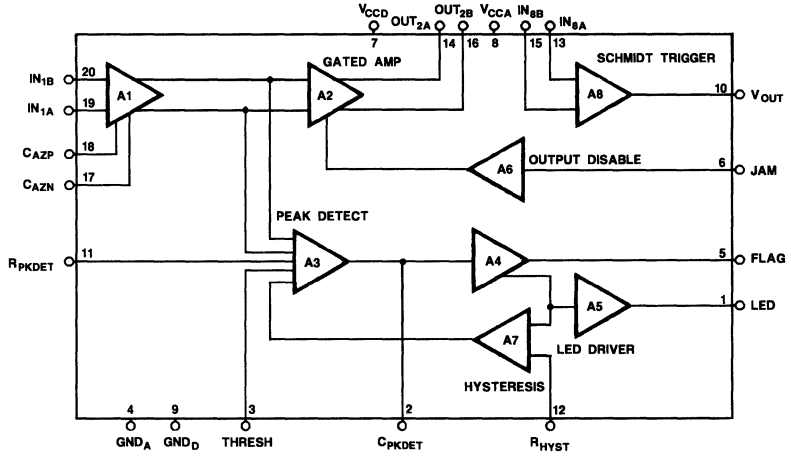
Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

PIN CONFIGURATION (cont.)

PIN NO.	SYMBOL	DESCRIPTION
12	R_{HYST}	Peak detector hysteresis resistor The value of this resistor determines the amount of hysteresis in the peak detector
13	IN_{8A}	Non-inverting input to amplifier A8
14	OUT_{2A}	Non-inverting output of amplifier A2
15	IN_{8B}	Inverting input to amplifier A8
16	OUT_{2B}	Inverting output of amplifier A2
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal) The value of this capacitor determines the low-end frequency response of the preamp A1
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal) The value of this capacitor determines the low-end frequency response of the preamp A1
19	IN_{1A}	Non-inverting input of the preamp A1
20	IN_{1B}	Inverting input of the preamp A1

BLOCK DIAGRAM



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Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	−0.5 to 5.5	−0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	0 to +95	−40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/− inputs)	3.16	3.4	3.63	3.13	3.4	3.65	V	
V_{O1}	A1 output bias voltage (+/− outputs)	3.17	3.8	4.45	3.10	3.8	4.50	V	
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (V_{CCA}, V_{CCD})	$V_{CCA} = V_{CCD} = 4.75$ to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	$\Delta V_{CM} = 200mV$		60			60		dB
V_{I8}	A8 input bias voltage (+/− inputs)	3.59	3.7	3.85	3.7	3.86	V		
V_{OH}	High-level TTL output voltage	$I_{OH} = -200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	$V_{OUT} = 2.4V$		−40	−26		−40	−24.4	μA
I_{OL}	Low-level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	$V_{OUT} = 0.0V$		−95			−95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	$V_{IJ} = 2.7V$			20			30	μA

Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

DC ELECTRICAL CHARACTERISTICS (Continued)

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{ILJ}	Low-level jam input current	$V_{IJ} = 0.4V$	-450	-240		-485	-240		μA
V_{OHF}	High-level flag output voltage	$I_{OH} = -80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	$V_{OUT} = 2.4V$		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	$V_{OUT} = 0.4V$	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	$V_{OUT} = 0.0V$	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	$V_{LED} = 3.0V$	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test Circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test Circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Maximum Functional A1 input signal (single ended)	Test Circuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage range	Test circuit, $T_A = 25°C$		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH} = 47k		12			12	mV_{P-P}	
t_{TLH}	TTL Output Rise Time 20% to 80%	Test circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} \times 10^2$	2.5				2.5		%

NOTE:
1 The NE/SA5217 is capable of detecting a much lower input level Operation under 12mV_{P-P} cannot be guaranteed by present day automatic testers

Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

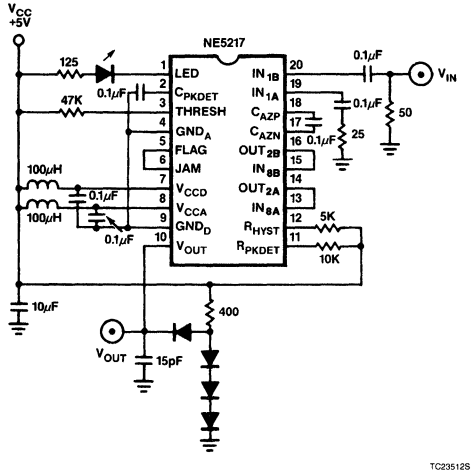
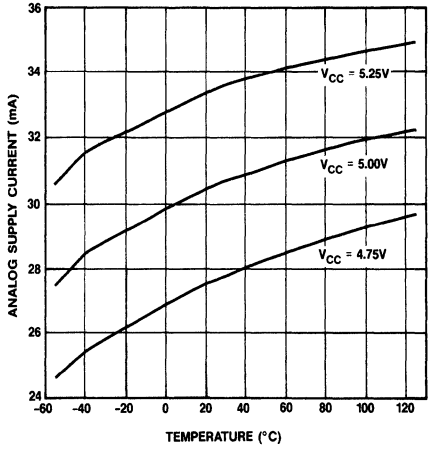


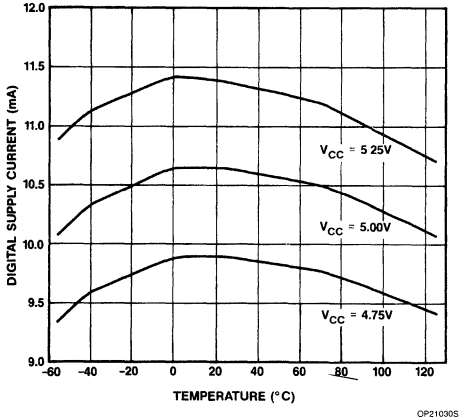
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Analog Supply Current vs Temperature



Digital Supply Current vs Temperature



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Fiber Optic Postamplifier with Link Status Indicator

NE/SA5217

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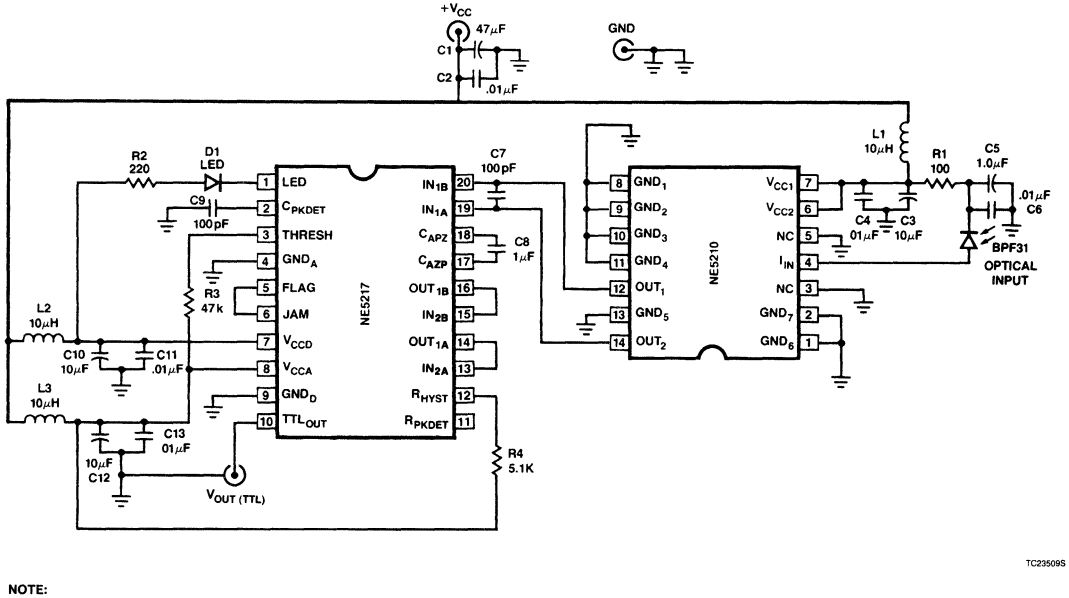
The NE5217 contains eight amplifier blocks (see Block Diagram) The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input, this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors This auto-zero loop cancels the transimpedance amplifiers's DC offset, the NE5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5217 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et a1.

A typical application of the NE5217 post amplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a −3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to Application Brief AB 1432.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

Figure 2. A 50Mb/s Fiber Optic Receiver

Signetics

Linear Products

Section 6
Telecommunications

INDEX

Signetics

NE5900
Call Progress Decoder

Product Specification

Linear Products

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder provides information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ringback, busy signal, or reorder tones.

A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS, and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

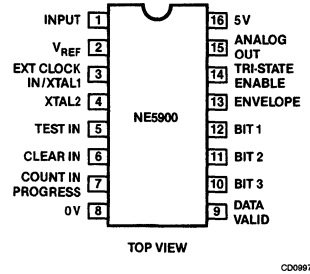
- **Fully decoded tri-state call progress status output**
- **Works with traditional, precision, or PBX call progress tones**
- **Low power consumption**
- **Low cost 3.58MHz crystal or clock**
- **No calibration or adjustment**
- **Interfaces with LSTTL, CMOS, NMOS**
- **Easy application**

APPLICATIONS

- **Modems**
- **PBXs**
- **Security equipment**
- **Auto dialers**
- **Answering machines**
- **Remote diagnostics**
- **Pay telephones**

PIN CONFIGURATION

D[1] and N Packages

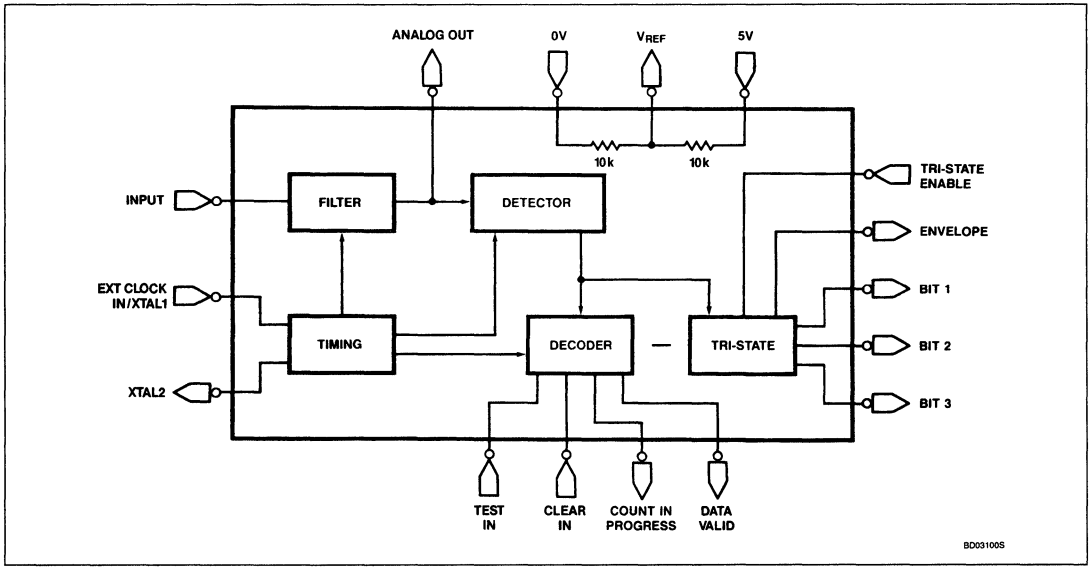


TOP VIEW

CD09970S

NOTE:
1 SOL — Released in large SO package only

BLOCK DIAGRAM CPD



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ORDERING INFORMATION

DESCRIPTION	AMBIENT TEMPERATURE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5900D
16-Pin Plastic DIP	0 to +70°C	NE5900N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Power supply voltage	9	V
V_{IN}	Logic control input voltages	−0.3 to +16	V
V_{IN}	All other input voltages[1]	−0.3 to V_{CC} +0.3	V
V_{OUT}	Output voltages	−0.3 to V_{CC} +0.3	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_J	Junction temperature	+150	°C

NOTE:
1 Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS Unless otherwise stated, V_{DD} = +5.0V; Pin 3 f_{OSC} = 3.58MHz; Ambient Temperature = 0 to +70°C. Pin 5 = 0V, Pin 14 = V_{DD}.

SYMBOL	PARAMETER	TEST CONDITONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pins 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads.		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DC} = V_{REF} Output Pin 13 = V_{DD}		-39	-35	dB[1]
	Signal rejection	Pin 1 level, 300Hz frequency, V_{DC}=V_{REF} Output Pin 13 = 0V			-50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 input voltage	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 input voltage	Pins 6, 14	0		0.8	V
I_{HL}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	-1.0		1.0	μA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	-1.0		1.0	μA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} - 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} - 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13 Pin 14 = 0V	-3.0		3.0	μA
	Filter output gain	Input Pin 1, 460Hz - 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	-1.0		1.0	dBmo
	Input impedance[2]	Pin 1, frequency = 460Hz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz - 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTES:
1. 0dB = 0.775V_{RMS}.
2. By design; not tested.

Call Progress Decoder NE5900

The NE5900 uses the signal in the call progress tone passband and the cadence or interrupt rate of the signal to determine which call progress tone is present.

Figure 1 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from line transients The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of −39dB typical (0dB = $0.775V_{RMS}$). The decoder will not respond to any signals below −50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15 A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3-second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 − 12, can be read.

The output code is as follows:

	PIN 12	PIN 11	PIN 10
DIAL TONE	0	0	0
RINGING SIGNAL	1	0	0
BUSY SIGNAL	0	1	0
REORDER TONE	0	0	1
OVERFLOW	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3-second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval Note that the end of dial tone is interpreted as a valid ringing signal

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2μs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6) When dialing is complete, the device is cleared and ready to respond to the next call progress unit

Enable is held at 5V to enable Pins 10, 11, 12, and 13 When enable is brought low, data valid is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications

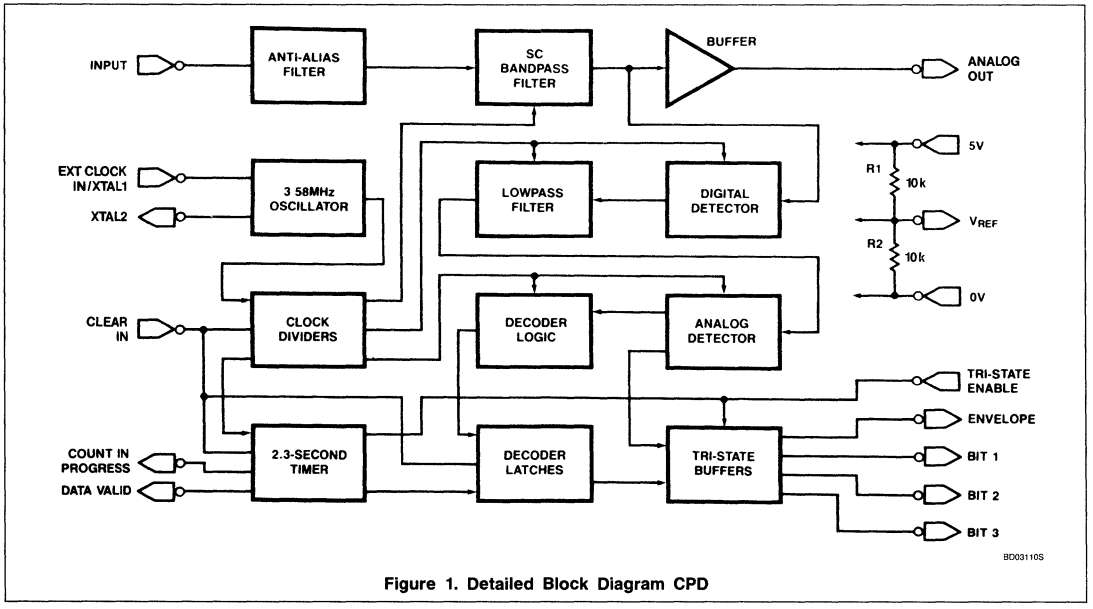


Figure 1. Detailed Block Diagram CPD

Figure 2 shows a typical application of the call progress decoder.

In this application only one external component is needed and no microprocessor activity other than clear is required.

Figure 3 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 4 gives a typical timing diagram for the application of Figures 2 and 3.

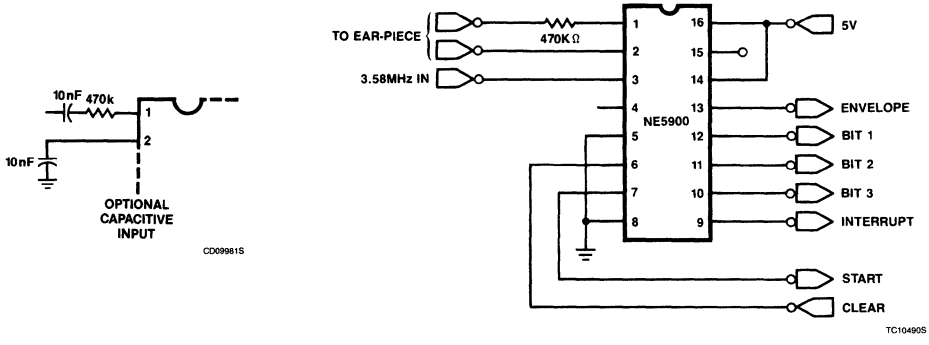


Figure 2. Typical Application

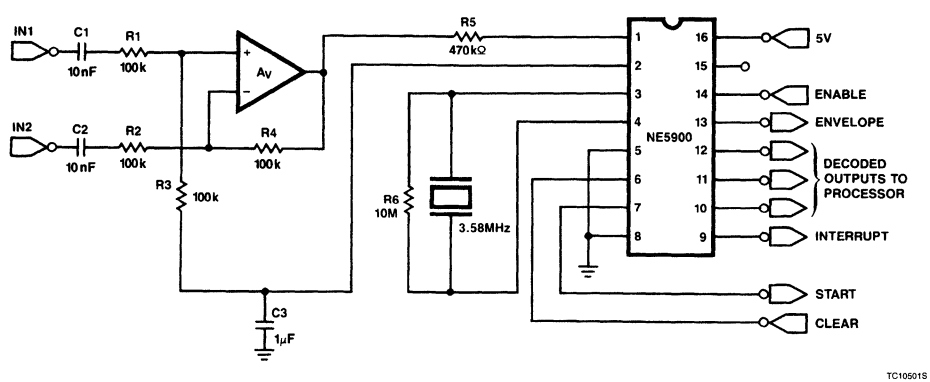


Figure 3. Typical Two-Wire Application

6

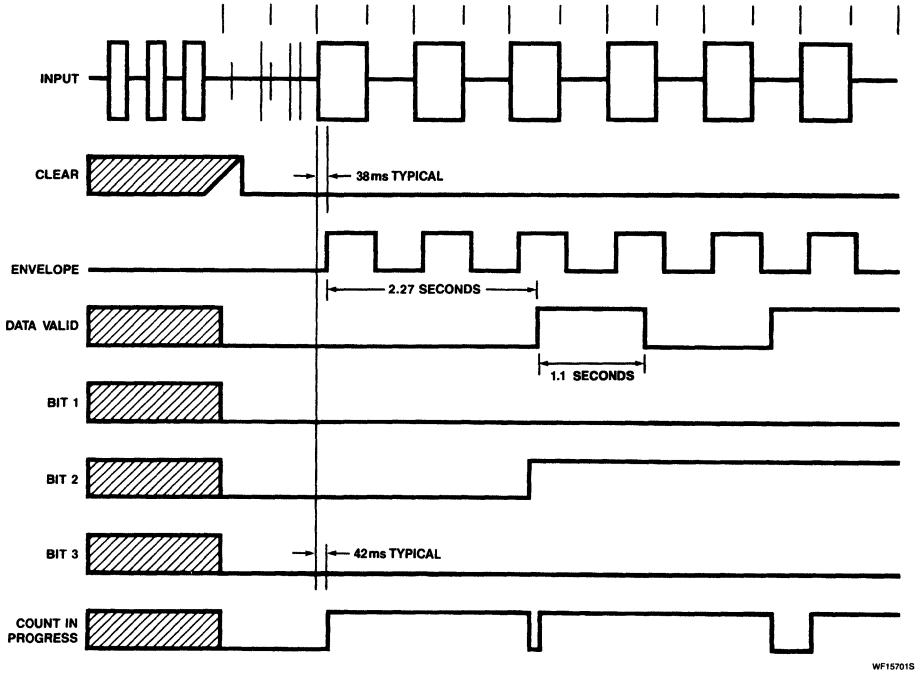
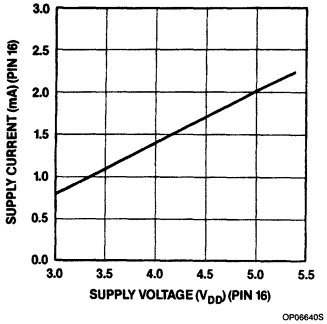

INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
WF15701S

Figure 4

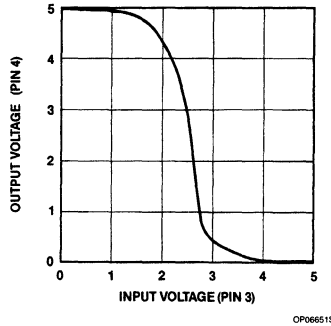
TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Current vs V_{DD}



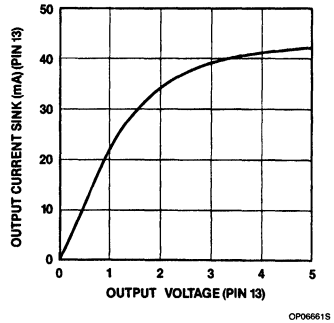
OP06640S

Voltage Transfer Curve



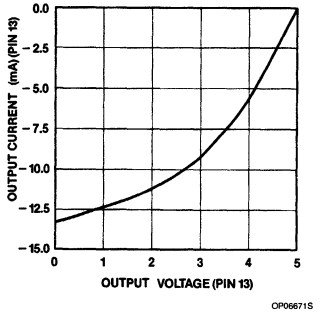
OP06651S

Output Voltage Current Curve Digital Output Low



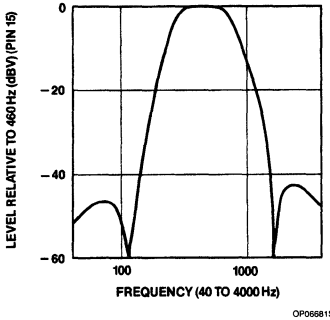
OP06661S

Output Voltage Current Curve Digital Output High



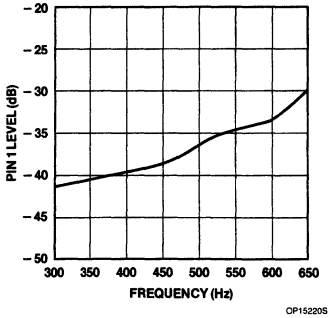
OP06671S

Filter Frequency Response



OP06681S

Typical Threshold



OP15220S

6

Signetics

PCD3310/A
Pulse and DTMF Dialer with Redial

Product Specification

Linear Products

DESCRIPTION

The PCD3310/A is a single-chip silicon-gate CMOS integrated circuit with an on-chip oscillator for a 3.58MHz crystal. It is a dual-standard dialing circuit for either pulse dialing (PD) or dual-tone multi-frequency (DTMF) dialing.

Input data is derived from any standard matrix keypad for dialing in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode, bursts as well as pauses are timed to a minimum in manual dialing, the maximum depending on the key depression time.

FEATURES

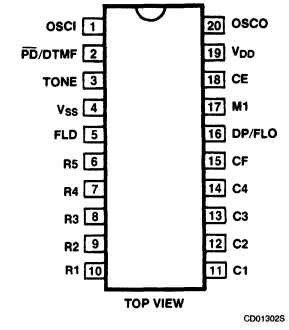
- **PD and DTMF dialing.**
- **23-digit capacity for redial operation (cursor method)**
- **Memory clear and electronic notepad**
- **Mixed mode dialing (start with PD and end with DTMF dialing)**
- **Dual redial buffers for PABX and public calls**
- **Four extra function keys: program, flash, redial and PD-to-DTMF (mixed dialing)**
- **DTMF timing:**
  - **manual dialing-minimum duration for bursts and pauses**
  - **redialing-calibrated timing**
- **On-chip voltage reference for supply, and temperature independent tone output**
- **On-chip filtering for low output distortion (CEPT CS 203 compatible)**
- **On-chip oscillator with low cost 3.58MHz TV color-burst crystal**
- **Uses standard single-contact or double-contact (common left open) keypad**
- **Keyboard entries fully debounced at both edges**
- **Flash (register recall) output**

APPLICATIONS

- **Single standard telephone sets**
- **Dual standard telephone sets**

PIN CONFIGURATIONS

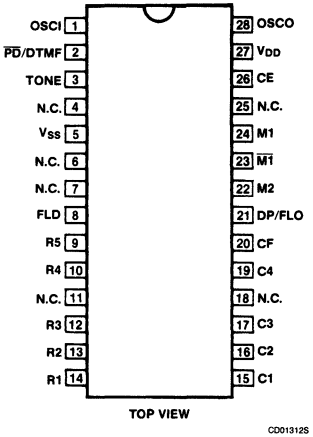
N Package



TOP VIEW

CD01302S

D Package



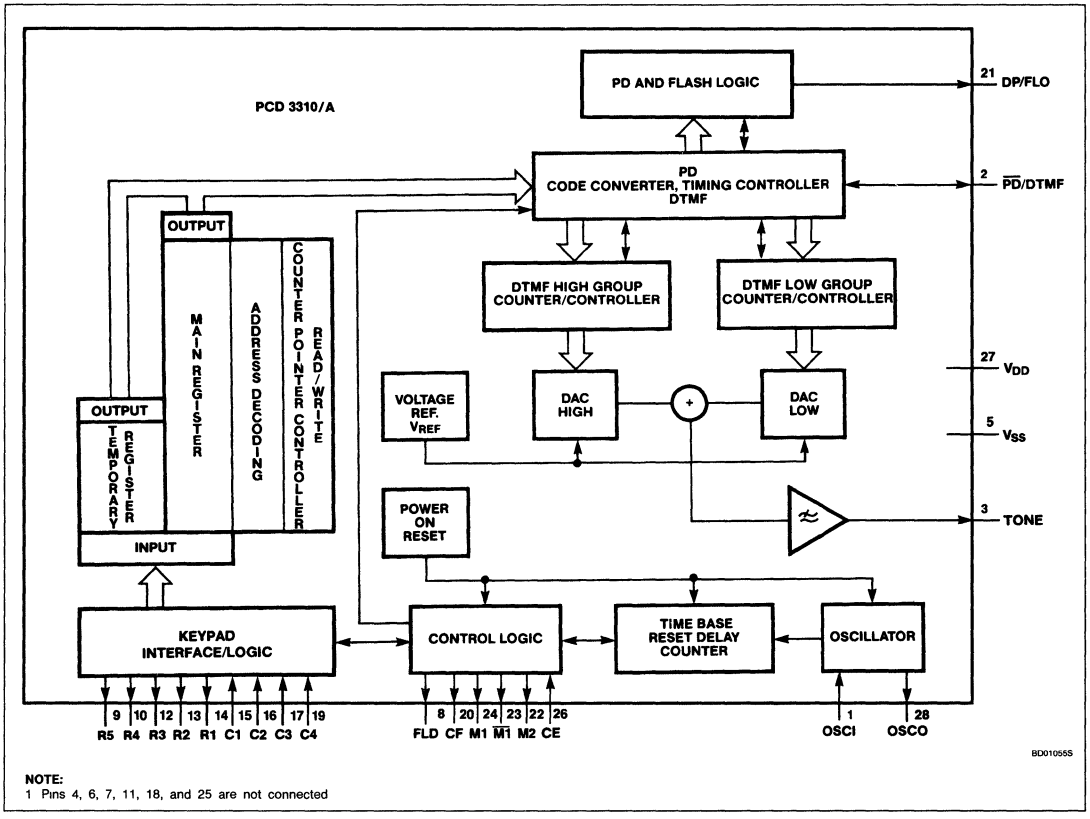
TOP VIEW

CD01312S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP (SOT-146)	−25°C to +70°C	PCD3310PN
28-Pin Plastic SO (SO-28; SOT-136A)	−25°C to +70°C	PCD3310TD
20-Pin Plastic DIP (SOT-146)	−25°C to +70°C	PCD3310APN
28-Pin Plastic SO (SO-28; SOT-136A)	−25°C to +70°C	PCD3310ATD

BLOCK DIAGRAM (D Package)

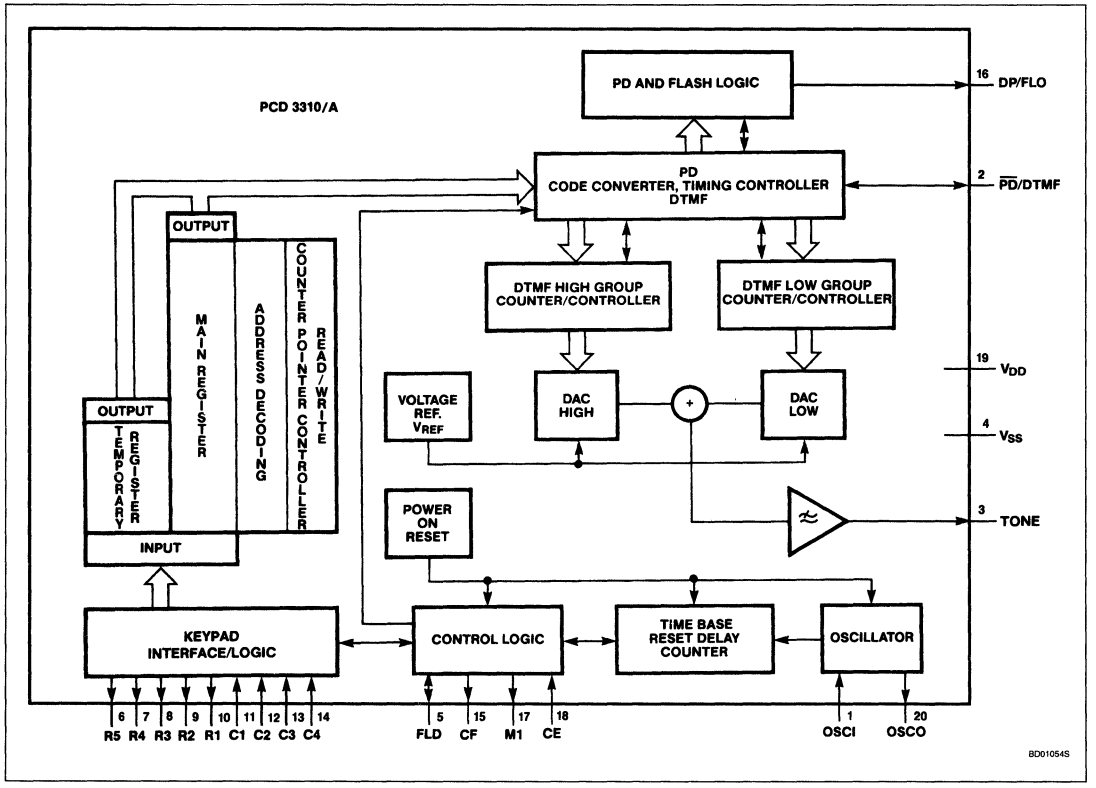


NOTE:
1 Pins 4, 6, 7, 11, 18, and 25 are not connected

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.8 to 8	V
I_{DD}	Supply current	50	mA
$\pm I_I$, $\pm I_O$	DC current into any input or output	10	mA
V_I	All input voltages	−0.8V to V_{DD} +0.8	V
P_{TOT}	Total power dissipation	300	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

BLOCK DIAGRAM (N Package)



DC AND AC ELECTRICAL CHARACTERISTICS V_{DD} = 3V; V_{SS} = 0V; crystal parameters: f_{OSC} = 3.579545MHz; R_S = 50Ω max.; T_A = −25°C to +75°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Operating supply voltage	2.5		6.0	V
V_{DDO}	Standby supply voltage	1.8		6.0	V
	Operating supply current				
I_{DDC}	conversation mode (oscillator ON)			100	μA
I_{DDP}	pulse dialing or flash			200	μA
I_{DDF}	DTMF dialing (tone ON)		0.6	0.9	mA
I_{DDF}	DTMF dialing (tone OFF)			200	μA
I_{DDO}	Standby supply current[1] (oscillator OFF) at V_{DD} = 1.8V; T_A = 25°C			5	μA
INPUTS					
V_{IL}	Input voltage LOW (any pin)	0		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH (any pin)	$0.7V_{DD}$		V_{DD}	V
$\lvert I_{IL} \rvert$	Input leakage current; CE			1	μA
Keyboard inputs					
I_{ON}	Keyboard ON current			45	μA
I_{OFF}	Keyboard OFF current	7.5			μA
OUTPUTS					
	Output sink current at $V_{OL} = V_{SS} + 0.5V$				
I_{OL}	M1, $\overline{M1}$, M2, DP/FLO, CF, FLD	0.7			mA
I_{OL}	$\overline{PD}$/DTMF[2]			1	mA
	Output source current at $V_{OH} = V_{DD} - 0.5V$				
$-I_{OH}$	M1, $\overline{M1}$, M2, DP/FLO, CF	0.6			mA
$-I_{OH}$	$\overline{PD}$/DTMF[2]		1		mA
$-I_{OH}$	FLD[3]		100		nA
TIMING AND FREQUENCY					
t_{ON}	Clock start-up time		4		ms
t_E	Debounce time		12		ms
t_{RD}	Reset delay time		160		ms
f_{CT}	Confidence tone frequency		330		Hz
TONE output (see Figure 9) at V_{DD} = 2.5 to 6V					
	DTMF output voltage levels (RMS value)				
$V_{HG(RMS)}$	HIGH group	158	192	205	mV
$V_{LG(RMS)}$	LOW group	125	150	160	mV
Δf/f	Frequency deviation	−0.6		+0.6	%
V_{DC}	DC voltage level		$\frac{1}{2}V_{DD}$		V
$\lvert Z_O \rvert$	Output impedance		0.1	0.5	kΩ
ΔV_G	Pre-emphasis of group	1.85	2.1	2.35	dB
THD	Total harmonic distortion[4] at T_A = 25°C		−25		dB

6

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{DD} = 3V; V_{SS} = 0V; crystal parameters: f_{OSC} = 3.579545MHz; R_S = 50Ω max.; T_A = −25°C to +75°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Transmission and pause time					
t_T, t_P	Manual dialing	68			ms
t_T, t_P	Redialing	68	70	72	ms
t_{FL}	Flash pulse duration	98	100	102	ms
t_{FLH}	Flash hold-over time	31	33	34	ms
t_H	Hold-over time (muting on M1)	78	80	81	ms
Pulse dialing (PD)					
f_{DP}	Dialing pulse frequency	7.8	10	10.4	Hz
t_{ID}	Inter-digit pause	828	840	844	ms
t_B	Break time[5,6]		67		ms
t_M	Make time[5,6]		33		ms

NOTES:

1 Crystal connected between OSCI and OSCO, CE at V_{SS} and all other pins open-circuit.
2. < |10mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode)
3. Flash inactive, $V_{OH} = V_{SS}$.
4 Related to the level of the LOW group frequency component (CEPT CS 203)
5 Mark-to-space ratio 2 1
6 A version mark-to-space ratio 3 2.

FUNCTIONAL DESCRIPTION

Power Supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.

To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.

If V_{DD} drops below the minimum standby supply voltage of 1.8V the power-on reset circuit inhibits redialing after hook-off.

The power-on reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock Oscillator (OSCI, OSCO)

The time base for the PCD3310 for both PD and DTMF modes is a crystal-controlled on-chip oscillator which is completed by connecting a 3.58MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary Write Address Counter (TWAC) which point to the last entered digit (Figure 3). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(MIN)}$.

The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialing or redialing operation starts. The operating current is I_{DDP} if in the pulse dialing mode, or I_{DDF} if the DTMF dialing mode is selected.

If the CE input is taken to a LOW level for more than time t_{RD} (see Figures 7a, 7b and timing data), an internal reset pulse will be generated at the end of the t_{RD} period. The system changes to the static standby state. Short CE pulses of $< t_{RD}$ will not affect the operation of the circuit, and reset pulses are not produced.

Mode Selection ($\overline{PD}$/DTMF)

PD Mode

If $\overline{PD}$/DTMF = V_{SS}, the pulse mode is selected. Entries of non-numeric keys are neglected; they are not stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD}, the dual tone multi-frequency dialing mode is selected. Each nonfunction pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfill the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_T) or minimum pause time (t_P).

Mixed Mode

When the $\overline{PD}$/DTMF pin is open-circuit, the mixed mode is selected. After activation of CE or FL (flash) the circuit starts as a pulse dialer and remains in this state until a non-numeric (A, B, C, D, *, #) or the " > " key is activated. Then the circuit changes over to DTMF dialing and remains there until FL is activated or, after a static standby condition, CE is re-activated.

A connection between $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialing. Chip enable, FL, or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialing.

Keyboard Inputs/Outputs

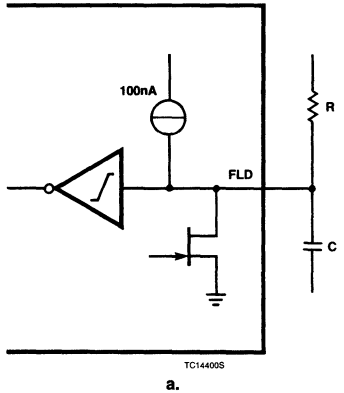
The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the PCD3310 are directly connected to the keyboard as shown in Figure 2.

All keyboard entries are debounced on both the leading and trailing edges for approximately time t_E as shown in Figure 7. Each entry is tested for validity.

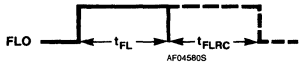
When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall



a.



NOTE:

Where $t_{FLRC} \approx RC$

b.

Figure 1. Flash Pulse Duration Setting

Table 1. Frequency Tolerance of the Output Tones for DTMF Signaling

ROW/ COLUMN	STANDARD FREQUENCY Hz	TONE OUTPUT FREQUENCY Hz[1]	FREQUENCY DEVIATION	
			%	Hz
Row 1	697	697.90	+0.13	+0.90
Row 2	770	770.46	+0.06	+0.46
Row 3	852	850.45	−0.18	−1.55
Row 4	941	943.23	+0.24	+2.23
Col 1	1209	1206.45	−0.21	−2.55
Col 2	1336	1341.66	+0.42	+5.66
Col 3	1477	1482.21	+0.35	+5 21
Col 4	1633	1638.24	+0.32	+5.25

NOTE:
1. Tone output frequency when using a 3 579545MHz crystal

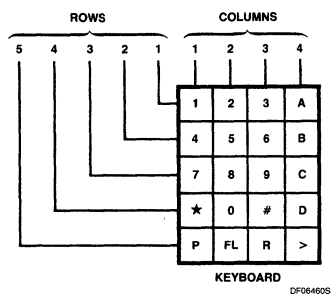


Figure 2. Keyboard Organization

- R redial
- > change of dial mode from PD to DTMF in mixed dialing mode

In pulse dialing mode, the valid keys are the 10 numeric pushbuttons (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialing or the redial storage. Valid function keys are P, FL and R.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In mixed mode all key entries are valid and executed accordingly.

Flash Duration Control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialing mode. Pressing the FL pushbutton will produce a timed line-break of 100ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Figure 1).

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

TONE OUTPUT (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfills the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signaling.

When the DTMF mode is selected, output tones are timed in manual dialing with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single-tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial Pulse and Flash Output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialing or for a calibrated break in both dialing modes (flash or register recall).

Mute Output (M1)

During pulse dialing the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialing the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute Output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Strobe Output (M2)

Active HIGH output during actual dialing; i.e., during break or make time in pulse dialing, or during tone ON/OFF in DTMF dialing. Available only in 28-pin surface mount device.

Confidence Tone Output (CF)

When any of the keys are activated, a square wave is generated and appears at this output to serve as an acoustic feedback for the user.

DIALING PROCEDURES

Dialing

After CE has risen to V_{DD}, the oscillator starts running and the Read Address Counter (RAC) is set to the first address (Figure 3). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated write address counter. After the sixth valid digit is entered, TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered, redial will be inhibited. If not more than 5 digits are entered, only the temporary register and the associated TWAC are affected. All entries are debounced on both the leading and trailing edges for at least time t_E as shown in Figure 7. Each entry is tested for validity before being deposited in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF, or mixed), the entries are transmitted as PD pulse trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialing; they are neither stored nor transmitted.

Redialing

After CE has risen to V_{DD}, the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD3310 is in the conversation mode.

If "R" is the first keyboard entry, the circuit starts redialing the contents of the temporary register. If the overflow flag of the TWAC was

set in the previous dialing, the redialing continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialed until the temporary read and write registers are equal.

Before pressing "R," a dialing sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode, only the first part entered (the pulse dialed part of the stored number) can be redialed.

During redial, keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialing.

No redial activity takes place if one of the following events occurs:

- Power on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode, a number with up to 23 digits can be entered and stored for redialing. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited) Afterwards, by entering and storing any digits, redialing will be possible after flash or hook on and off.

During notepad programming, the numbers entered will neither be transmitted nor is the mute active; only the confidence tone is generated.

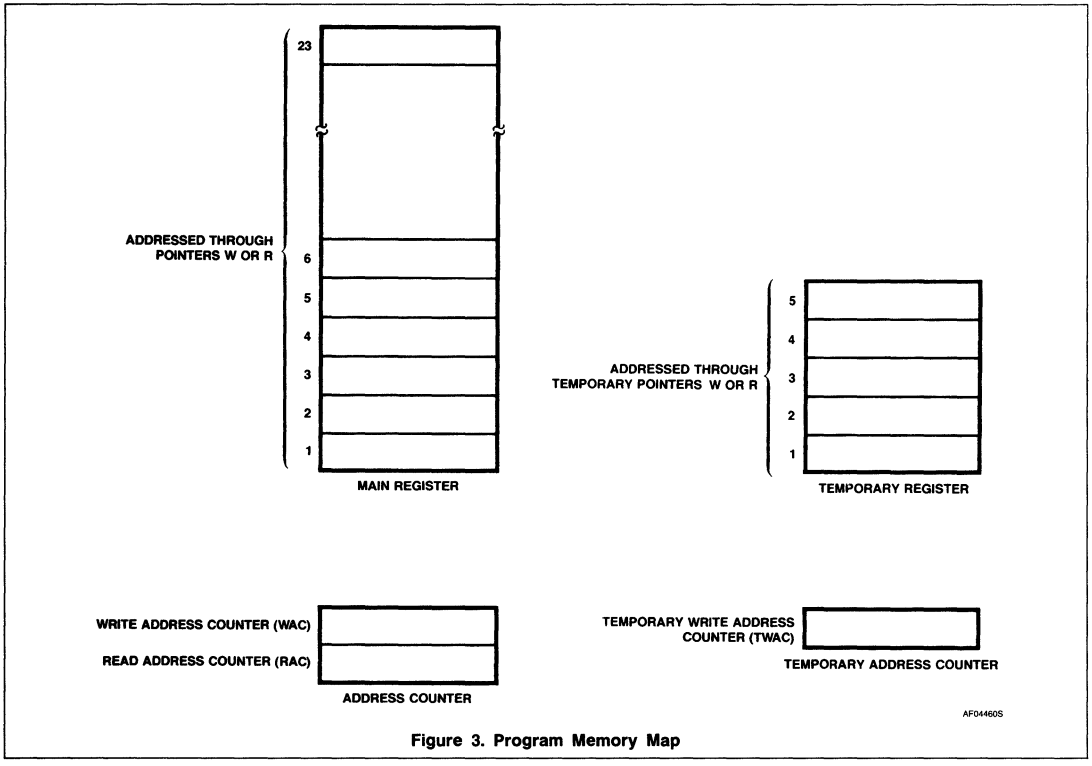


Figure 3. Program Memory Map

6

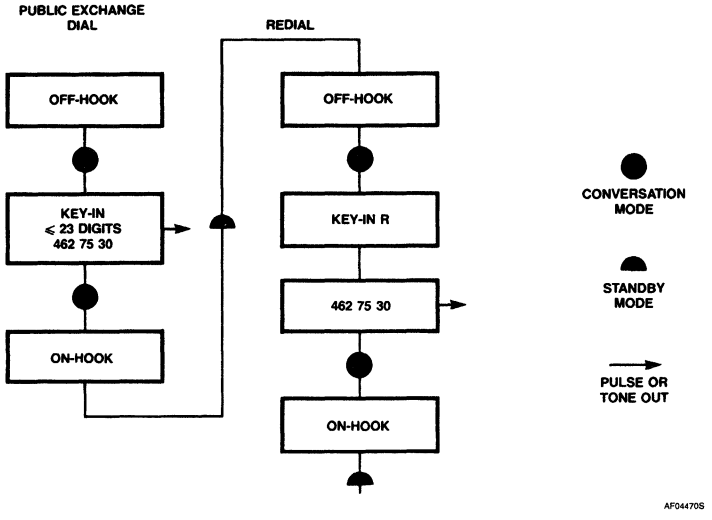
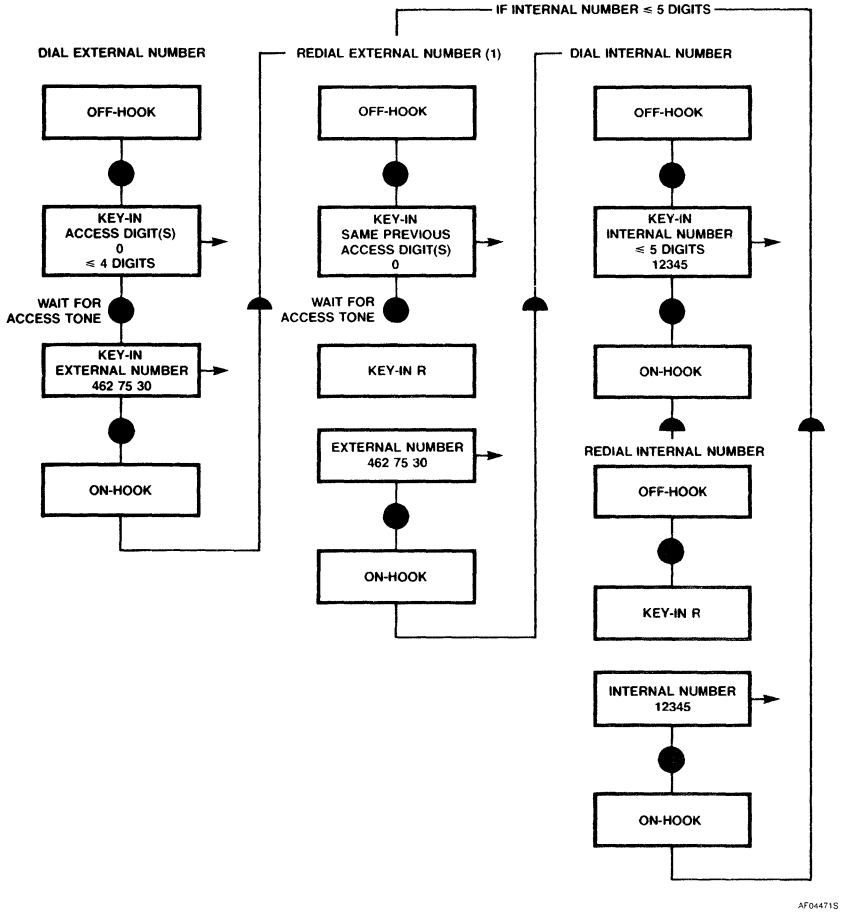


Figure 4a. Public Exchange $\overline{PD}$/DTMF Mode



NOTE:
1 If [access digit(s) + external number] ≤ 23 digits

Figure 4b. PABX $\overline{PD}$/DTMF Mode

6

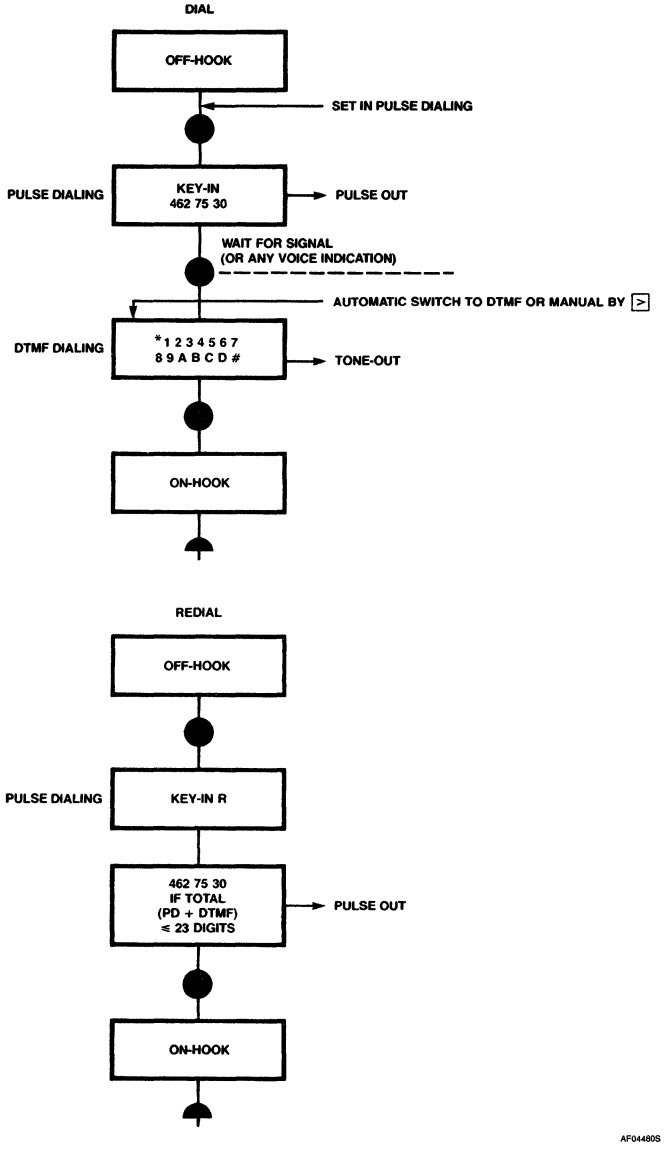


Figure 5. $\overline{PD}$/DTMF Mixed-Mode Dialing

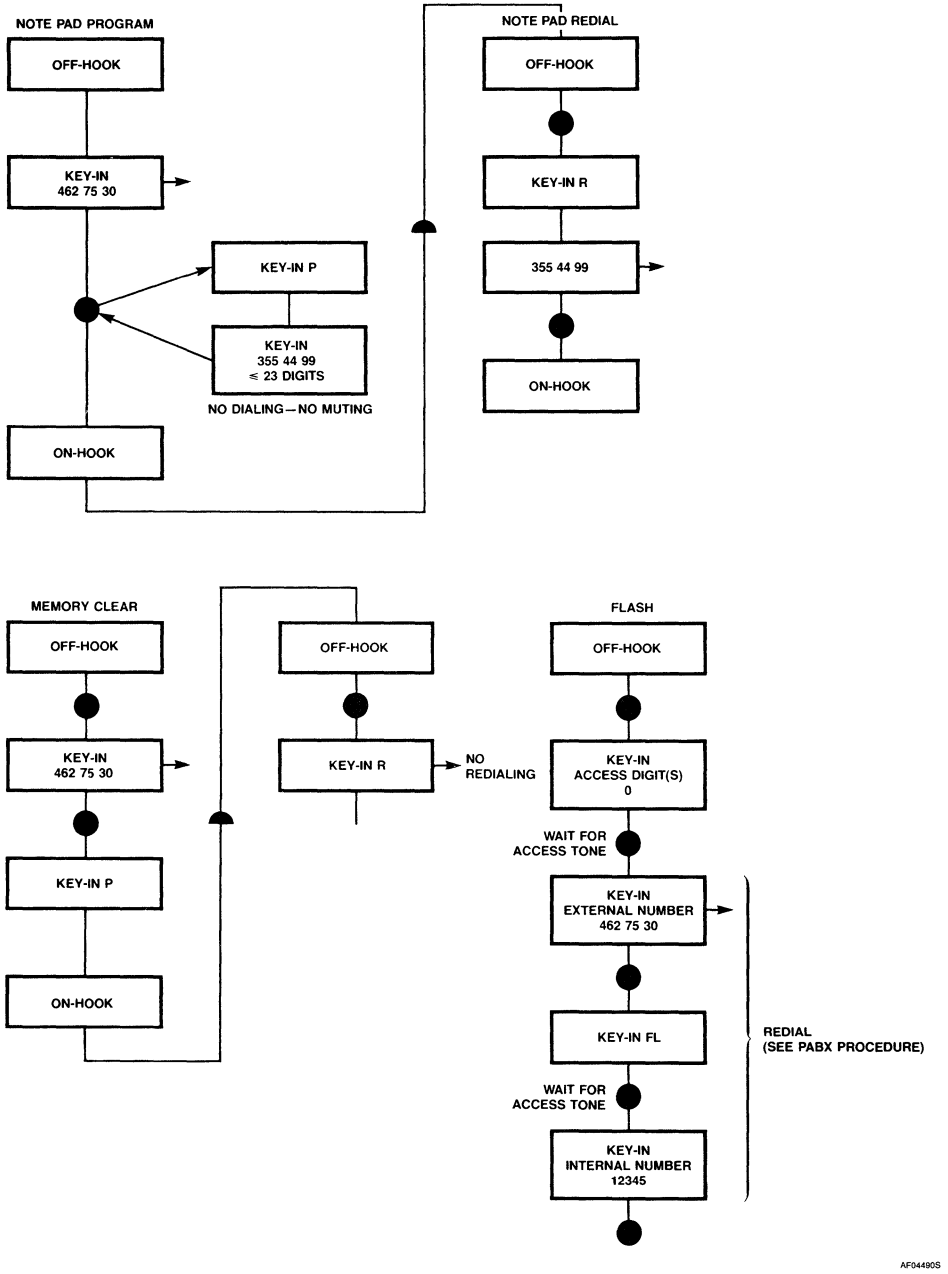


Figure 6. Notepad/Memory Clear, Flash; Independent of Dialing Mode

6

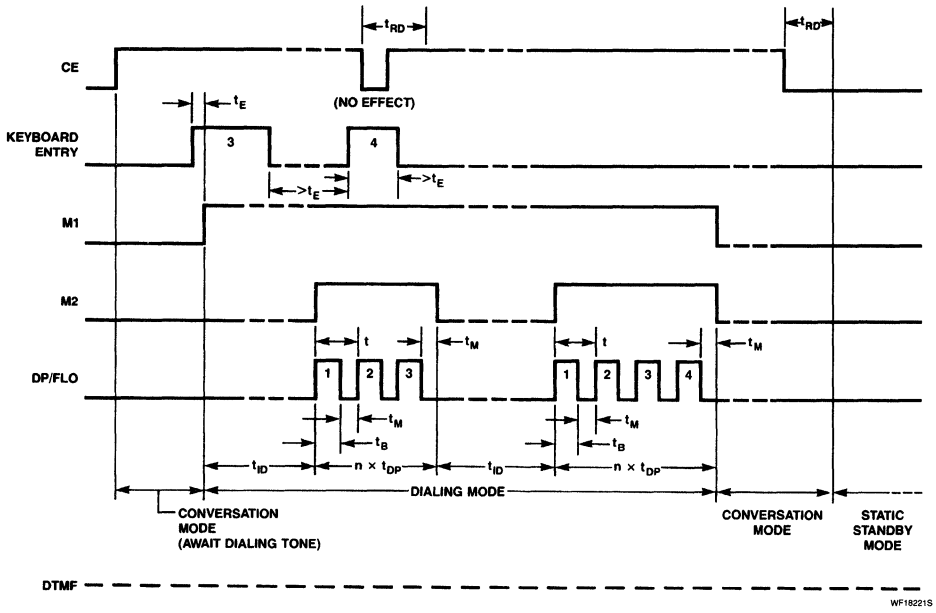


Figure 7a. Timing Diagram for Dialing Mode Defined by $\overline{PD}$/DTMF Selection Pin; Pulse Dialing ($\overline{PD}$/DTMF = V_{SS})

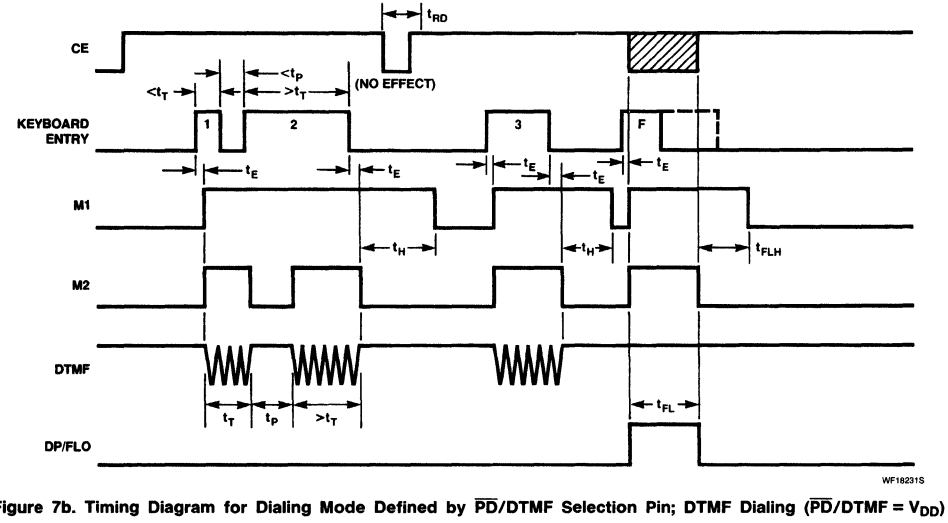


Figure 7b. Timing Diagram for Dialing Mode Defined by $\overline{PD}$/DTMF Selection Pin; DTMF Dialing ($\overline{PD}$/DTMF = V_{DD})

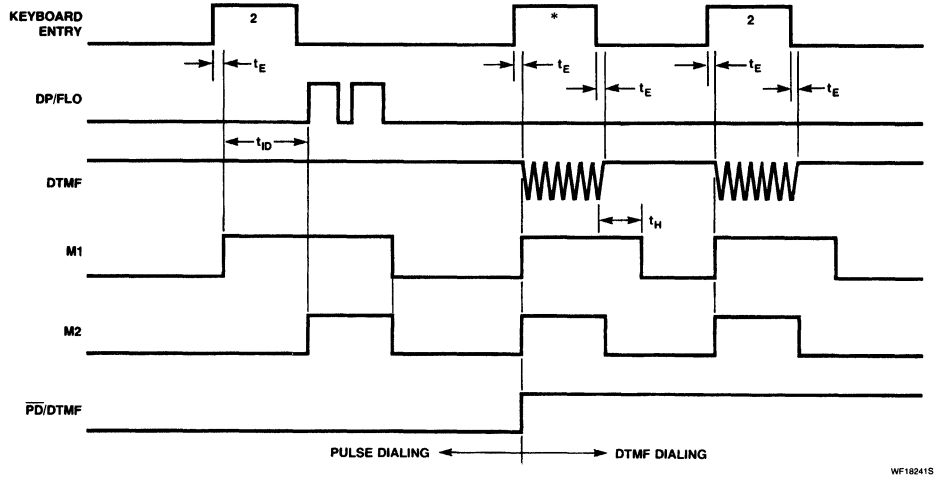


Figure 7c. Timing Diagram for Dialing Mode Defined by $\overline{PD}$/DTMF Selection Pin; Pulse Dialing (Mixed Mode)

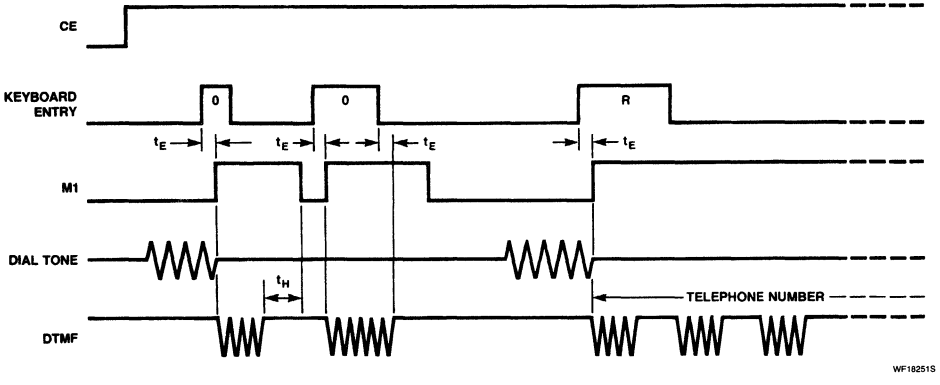


Figure 8. Timing Diagram Showing REDIAL Where PABX Access Digits are the First Keyboard Entries; DTMF Dialing with $\overline{PD}$/DTMF = V_{DD}

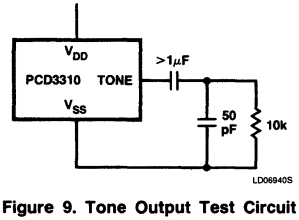
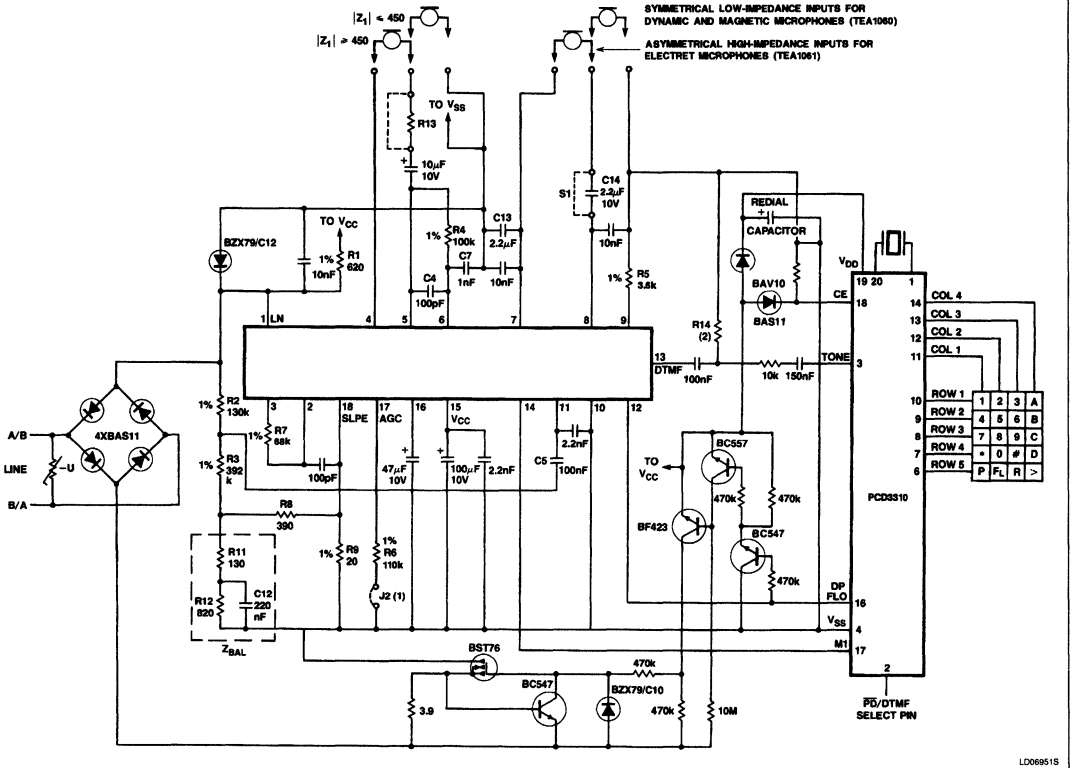


Figure 9. Tone Output Test Circuit



NOTES:
1 Automatic line compenstion obtained by connecting R6 to V_{SS}
2 The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060

Figure 10. Application Diagram of the Full Electronic Basic Telephone Set

Signetics

PCD3311/12
DTMF/Modem/Musical Tone Generators

Product Specification

Linear Products

DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialing systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3.58MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS203 recommendations.

In addition to the standard DTMF frequencies, the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

FEATURES

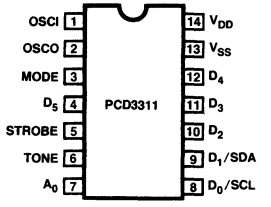
- **Stabilized output voltage level**
- **Low output distortion with on-chip filtering (CEPT CS203 compatible)**
- **Latched inputs for data bus applications**
- **I^2C bus compatible**
- **Mode select input (selection of parallel or serial data input)**
- **MODEM and melody tone generators**

APPLICATION

- **Microcontrolled telephone sets**

PIN CONFIGURATIONS

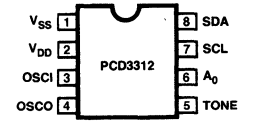
N Package



TOP VIEW

CD12720S

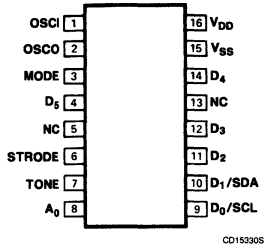
D, N Packages



TOP VIEW

CD12730S

D Package



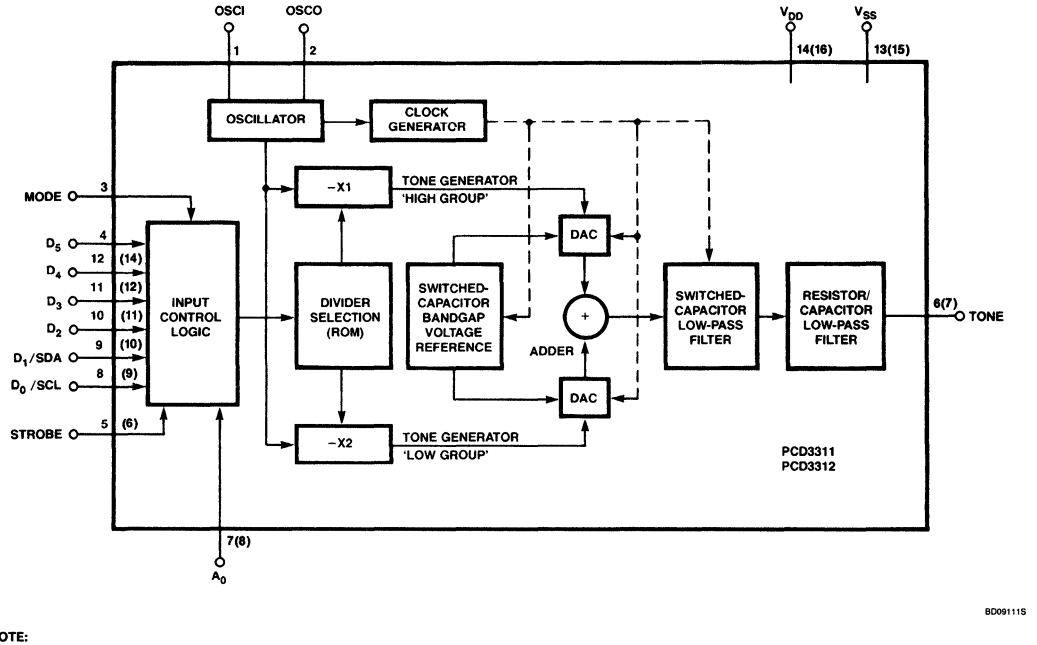
CD15330S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP (SOT-27k, M, T)	−25°C to +70°C	PCD3311PN
16-Pin Plastic SO (SO-16L; SOT-162A)	−25°C to +70°C	PCD3311TD
8-Pin Plastic DIP (SOT-97A)	−25°C to +70°C	PCD3312PN
8-Pin Plastic SO (SO-8L; SOT-176)	−25°C to +70°C	PCD3312TD

6

BLOCK DIAGRAM



NOTE:
The pin numbers in parentheses refer to the PCD3311TD, Pins 5 and 13 are NC

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{DD}	Supply voltage range	−0.8	+8.0	V
V_I	Input voltage range (any input)	−0.8	V_{DD} + 0.8	V
$\pm I_I$	DC input current (any input)		10	mA
$\pm I_O$	DC output current (any output)		10	mA
$\pm I_{DD}$; $\pm I_{SS}$	Supply current		50	mA
P_O	Power dissipation per output		50	mW
P_{TOT}	Total power dissipation per package		300	mW
T_A	Operating ambient temperature range	−25	+70	°C
T_{STG}	Storage temperature range	−65	+150	°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.5 to 6V; V_{SS} = 0V; crystal parameters: f_{OSC} = 3.579 545MHz, R_{SMAX} = 50Ω; T_A = −25°C to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Operating supply voltage	2.5		6.0	V
	Operating supply current[1] oscillator ON; V_{DD} = 3V				
I_{DD}	no output tone		50	100	μA
I_{DD}	single output tone		0.5	1.0	mA
I_{DD}	dual output tone		0.6	1.2	mA
	Static standby current[1]				
I_{DDO}	oscillator OFF			3	μA
Inputs/outputs (SDA)					
	D_0 to D_5; MODE; STROBE				
V_{IL}	Input voltage LOW	0		0.3 × V_{DD}	V
V_{IH}	Input voltage HIGH	0.7 × V_{DD}		V_{DD}	V
	D_2 to D_5; MODE; STROBE; A_0				
$-I_{IL}$	Pull-down input current, V_I = V_{DD}	30	150	300	nA
	SCL (D_0); SDA (D_1)				
I_{OL}	Output current LOW (SDA), V_{OL} = 0.4V	3			mA
f_{SCL}	Clock frequency (see Figure 7)			100	kHz
C_I	Input capacitance; V_I = V_{SS}			7	pF
t_I	Allowable input spike pulse width			100	ns
TONE output (See Figure 11)					
	DTMF output voltage levels (RMS values)				
$V_{HG(RMS)}$	HIGH group	158	192	205	mV
$V_{LG(RMS)}$	LOW group	125	150	160	mV
V_{DC}	DC voltage level		½ V_{DD}		V
ΔV_G	Pre-emphasis of group	1.85	2.10	2.35	dB
	Total harmonic distortion, T_A = 25°C				
THD	dual tone[2]		−25		dB
THD	modem tone[3]		−29		dB
$\|Z_O\|$	Output impedance		0.1	0.5	kΩ
OSCI input					
$V_{OSC(P-P)}$	Maximum allowable amplitude at OSCI			$V_{DD} - V_{SS}$	V
Timing (V_{DD} = 3V)					
$t_{OSC(ON)}$	Oscillator start-up time		3		ms
$t_{TONE(ON)}$	TONE start-up time[4]		0.5		ms
t_{STR}	STROBE pulse width[5]	400			ns
t_{DS}	Data setup time[5]	150			ns
t_{DH}	Data hold time[5]	100			ns

NOTES:

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5.6kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

FUNCTIONAL DESCRIPTION

Clock/Oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3.58MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode Select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data Inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Strobe Input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

Table 1. D_5 and D_4 in Accordance With the Selected Application

D_5	D_4	APPLICATION
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	Melody tones

NOTES:
1 = H = HIGH voltage level
0 = L = LOW voltage level

Serial Clock and Data Inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1, respectively. For the PCD3311, the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see CHARACTERISTICS OF THE I^2C BUS). Both inputs must be pulled-up externally to V_{DD}.

Address Input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case, A_0 must be connected to V_{DD} or V_{SS}.

I^2C Bus Data Configuration (see Figure 2)

The PCD3311 and PCD3312 are always slave receivers in the I^2C bus configuration ($R/\overline{W}$ bit = 0)

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

Tone Output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-On Reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF)

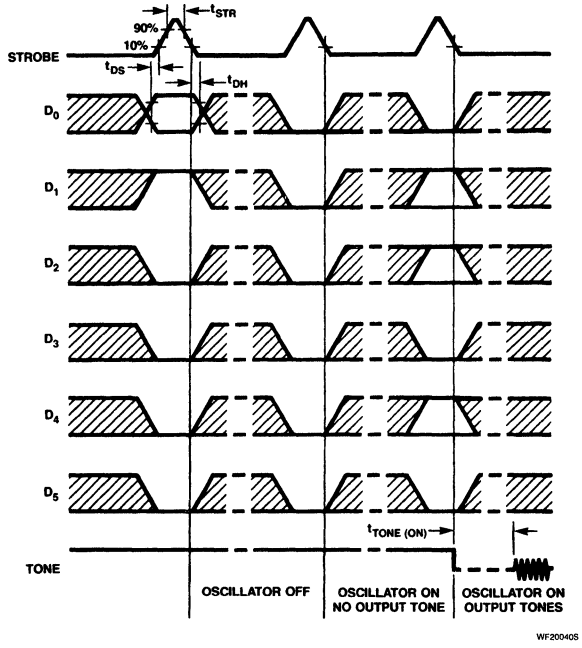


Figure 1. Timing Diagram Showing Control Possibilities of the Oscillator and the TONE Output (e.g., 770Hz + 1477Hz) in the Parallel Mode (MODE = HIGH)

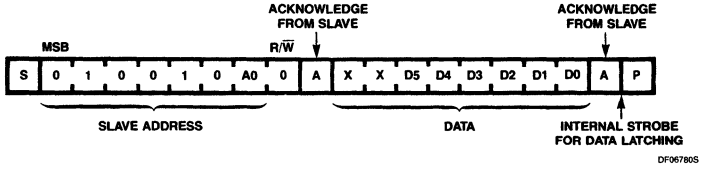


Figure 2. I^2C Bus Data Format

Table 2. Input Data for Control (No Output Tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	OSCILLATOR
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

NOTES:
1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

Table 3. Input Data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	SYMBOL	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQ. (Hz)[1]	FREQUENCY DEVIATION	
										%	Hz
0	0	1	0	0	0	08		697	697.90	+0.13	+0.90
0	0	1	0	0	1	09		770	770.46	+0.06	+0.46
0	0	1	0	1	0	0A		852	850 45	−0.18	−1.55
0	0	1	0	1	1	0B		941	943.23	+0.24	+2.23
0	0	1	1	0	0	0C		1209	1206 45	−0.21	−2.55
0	0	1	1	0	1	0D		1336	1341 66	+0.42	+5.66
0	0	1	1	1	0	0E		1477	1482.21	+0.35	+5.21
0	0	1	1	1	1	0F		1633	1638.24	+0.32	+5.24
0	1	0	0	0	0	10	0	941 + 1336			
0	1	0	0	0	1	11	1	697 + 1209			
0	1	0	0	1	0	12	2	697 + 1336			
0	1	0	0	1	1	13	3	697 + 1477			
0	1	0	1	0	0	14	4	770 + 1209			
0	1	0	1	0	1	15	5	770 + 1336			
0	1	0	1	1	0	16	6	770 + 1477			
0	1	0	1	1	1	17	7	852 + 1209			
0	1	1	0	0	0	18	8	852 + 1336			
0	1	1	0	0	1	19	9	852 + 1477			
0	1	1	0	1	0	1A	A	697 + 1633			
0	1	1	0	1	1	1B	B	770 + 1633			
0	1	1	1	0	0	1C	C	852 + 1633			
0	1	1	1	0	1	1D	D	941 + 1633			
0	1	1	1	1	0	1E	*	941 + 1209			
0	1	1	1	1	1	1F	#	941 + 1477			

Table 4. Input Data for MODEM Frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQ. (Hz)[1]	FREQUENCY DEVIATION		REMARKS
									%	Hz	
1	0	0	1	0	0	24	1300	1296 94	−0 24	−3.06	V.23
1	0	0	1	0	1	25	2100	2103 14	+0 15	+3.14	
1	0	0	1	1	0	26	1200	1197 17	−0.24	−2.83	Bell 202
1	0	0	1	1	1	27	2200	2192.01	−0 36	−7 99	
1	0	1	0	0	0	28	980	978 82	−0.12	−1.18	V.21
1	0	1	0	0	1	29	1180	1179 03	−0 08	−0.97	
1	0	1	0	1	0	2A	1070	1073.33	+0 31	+3.33	Bell 103
1	0	1	0	1	1	2B	1270	1265 30	−0 37	−4 70	
1	0	1	1	0	0	2C	1650	1655 66	+0 34	+5.66	V.21
1	0	1	1	0	1	2D	1850	1852 77	+0 15	+2.77	
1	0	1	1	1	0	2E	2025	2021 20	−0 19	−3 80	Bell 103
1	0	1	1	1	1	2F	2225	2223 32	−0 08	−1.68	

NOTES:
1 Tone output frequency when using a 3 579 545MHz crystal
1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5. Input Data for Melody Tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	NOTE	STANDARD FREQUENCY (Hz)[1]	TONE OUTPUT FREQUENCY (Hz)[2]
1	1	0	0	0	0	30	D#5	622.3	622.5
1	1	0	0	0	1	31	E5	659.3	659.5
1	1	0	0	1	0	32	F5	698.5	697.9
1	1	0	0	1	1	33	F#5	740.0	741.1
1	1	0	1	0	0	34	G5	784.0	782.1
1	1	0	1	0	1	35	G#5	830.6	832.3
1	1	0	1	1	0	36	A5	880.0	879.3
1	1	0	1	1	1	37	A#5	932.3	931.9
1	1	1	0	0	0	38	B5	987.8	985.0
1	1	1	0	0	1	39	C6	1046.5	1044.5
1	1	1	0	1	0	3A	C#6	1108.7	1111.7
1	0	1	0	0	1	29	D6	1174.7	1179.0
1	1	1	0	1	1	3B	D#6	1244.5	1245.1
1	1	1	1	0	0	3C	E6	1318.5	1318.9
1	1	1	1	0	1	3D	F6	1396.9	1402.1
0	0	1	1	1	0	0E	F#6	1480.0	1482.2
1	1	1	1	1	0	3E	G6	1568.0	1572.0
1	0	1	1	0	0	2C	G#6	1661.2	1655.7
1	1	1	1	1	1	3F	A6	1760.0	1768.5
0	0	0	1	0	0	04	A#6	1864.7	1875.1
0	0	0	1	0	1	05	B6	1975.5	1970.0
1	0	0	1	0	1	25	C7	2093.0	2103.1
1	0	1	1	1	1	2F	C#7	2217.5	2223.3
0	0	0	1	1	0	06	D7	2349.3	2358.1
0	0	0	1	1	1	07	D#7	2489.0	2470.4

NOTES:
1. Standard scale based on A4 = 440Hz.
2. Tone output frequency when using a 3.579 545MHz crystal.
   1 = H = HIGH voltage level
   0 = L = LOW voltage level

6

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

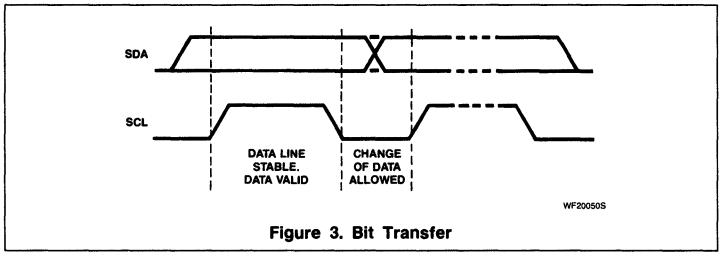


Figure 3. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

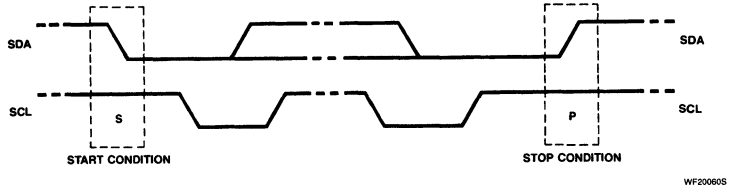


Figure 4. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse; so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate to stop condition.

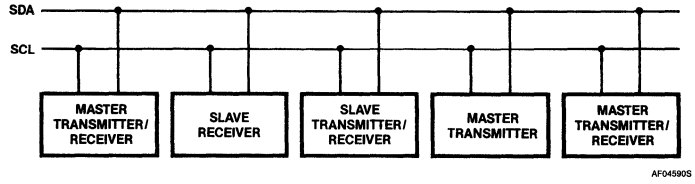


Figure 5. System Configuration

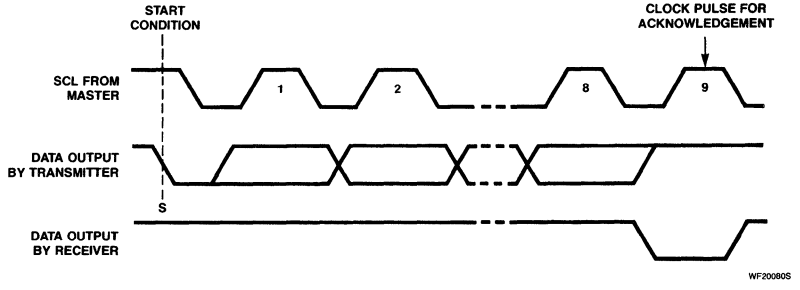
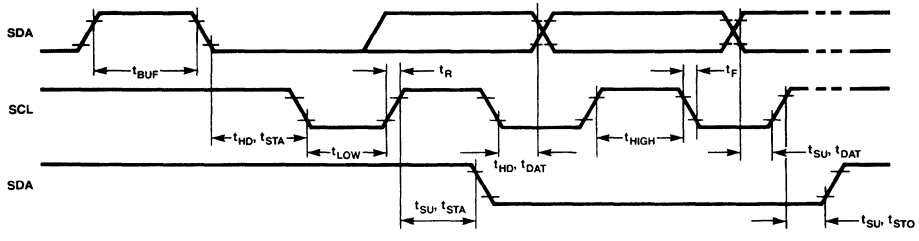


Figure 6. Acknowledgment on the I^2C Bus

Timing Specifications

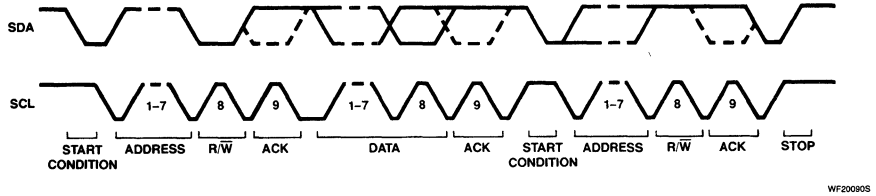
Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 7.



Where		
t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
t_{HD}; t_{STA}	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
t_{SU}; t_{STA}	$t \geq t_{LOWmin}$	Start condition setup time, only valid for repeated start code
t_{HD}; t_{DAT}	$t \geq 0\mu s$	Data hold time
t_{SU}; t_{DAT}	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
t_{SU};t_{STO}	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}

Figure 7. Timing



Where	
Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgment of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Maximum number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Figure 8. Complete Data Transfer

6

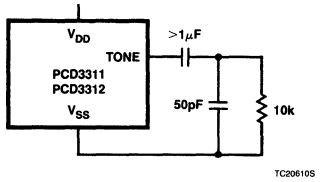


Figure 9. TONE Output Test Circuit

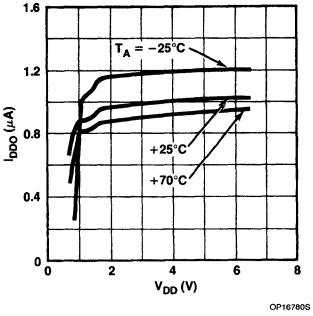


Figure 10. Standby Supply Current as a Function of Supply Voltage; Oscillator OFF

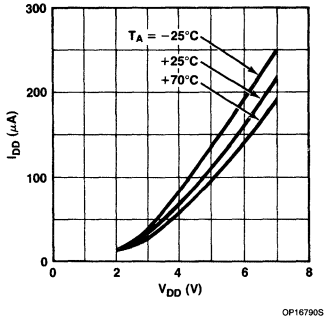


Figure 11. Operating Supply Current as a Function of Supply Voltage; Oscillator ON; No Output at TONE

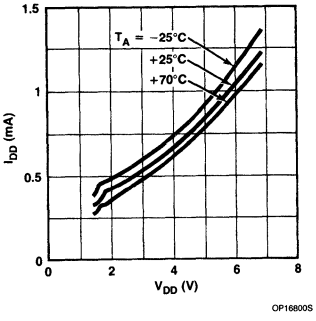


Figure 12. Operating Supply Current as a Function of Supply Voltage; Oscillator ON; Dual-Tone at TONE

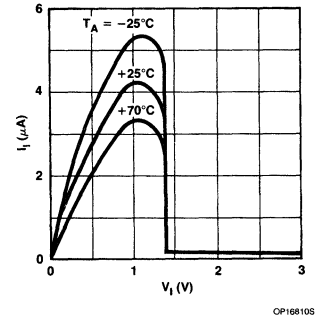


Figure 13. Pull-Down Input Current as a Function of Input Voltage; V_{DD} = 3V

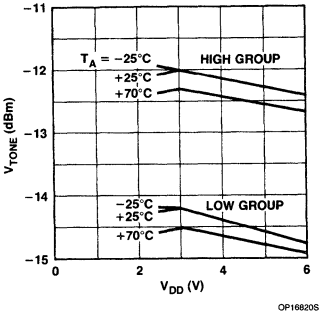


Figure 14. DTMF Output Voltage Levels as a Function of Operating Supply Voltage; R_L = 1MΩ

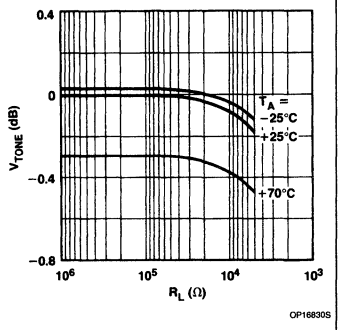


Figure 15. Dual-Tone Output Voltage Level as a Function of Output Load Resistance

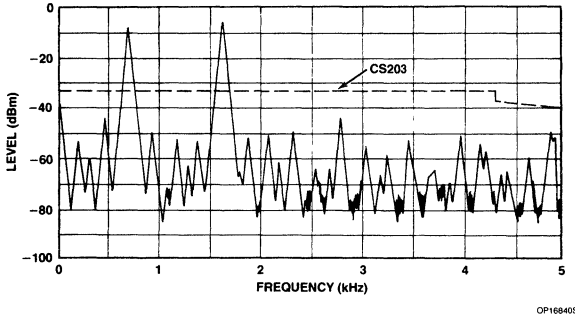


Figure 16. Typical Frequency Spectrum of a Dual-Tone Signal After Flat-Band Amplification of 6dB

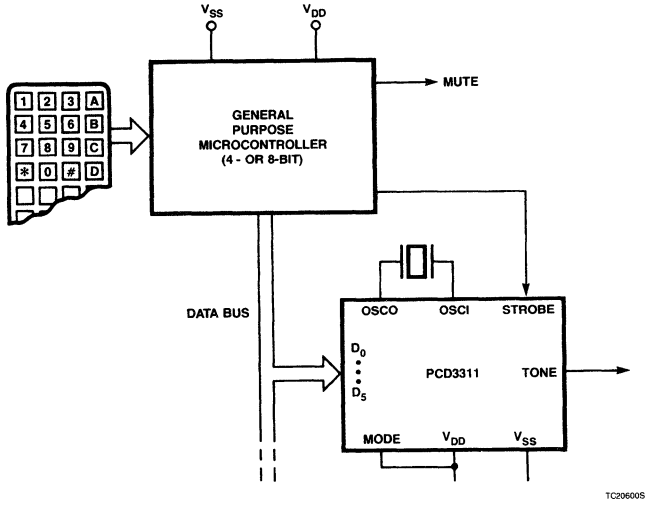


Figure 17. PCD3311 Driven by a Microcontroller with Parallel Data Bus

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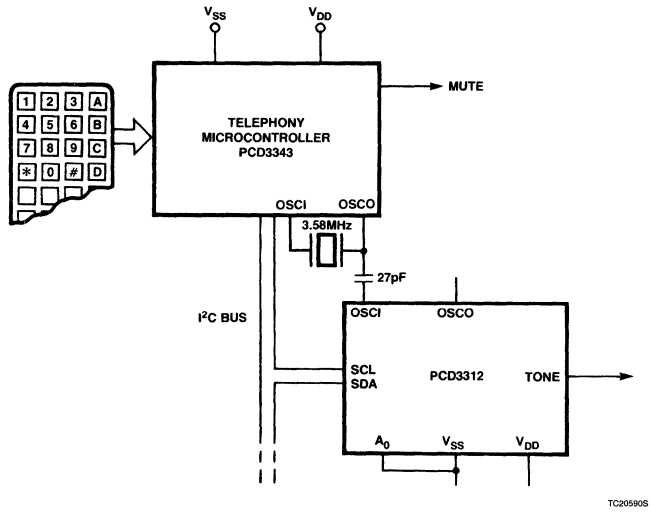


NOTE:
The PCD3343 is a single-chip 8-bit microcontroller with 3k ROM/224 RAM bytes
The same application is possible with the PCD3311 with MODE = V_{SS}

Figure 18. PCD3312 Driven by Telephony Microcontroller PCD3343 with Serial I/O (I^2C Bus)

PCD3315
CMOS Redial and Repertory Dialer

Product Specification

Linear Products

DESCRIPTION

The PCD3315 is a single-chip CMOS dialer IC for telephone sets. It has two dialing modes: pulse dialing (PD), and dual-tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312. In addition to manual dialing, it also features several automatic functions, such as redial, extended redial, note-pad, and repertory dial.

FEATURES

- **Pulse dialing**
- **DTMF dial control of tone generator PCD3312**
- **Redial**
- **Extended redial**
- **Electronic notepad**
- **Ten repertory dial numbers**
- **18-digit capacity for each autodial memory**
- **I^2C compatible**
- **Maximum of 36 digits per call**
- **Flash or register recall**
- **Uses standard 4 × 4 keyboard (single- or double-contact)**
- **Four extra function keys: program/autodial, flash, redial, access pause**
- **Access pause generation and termination**
- **Automatic PABX-digit recognition resulting in an access pause insertion**
- **Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers**
- **Four diode or strap functions: general/German, access pause time, reset delay time, general: mark-space ratio/German: prepulse**
- **Manual reset of autodial RAM**
- **On-chip power-on reset**
- **Programmed for improved noise immunity**

APPLICATION

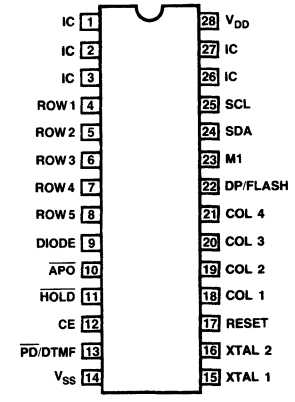
- **Feature phones**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−25°C to +70°C	PCD3315PN
28-Pin Plastic SO package (SO-28; SOT-136A)	−25°C to +70°C	PCD3315TD

PIN CONFIGURATIONS

N, D Packages

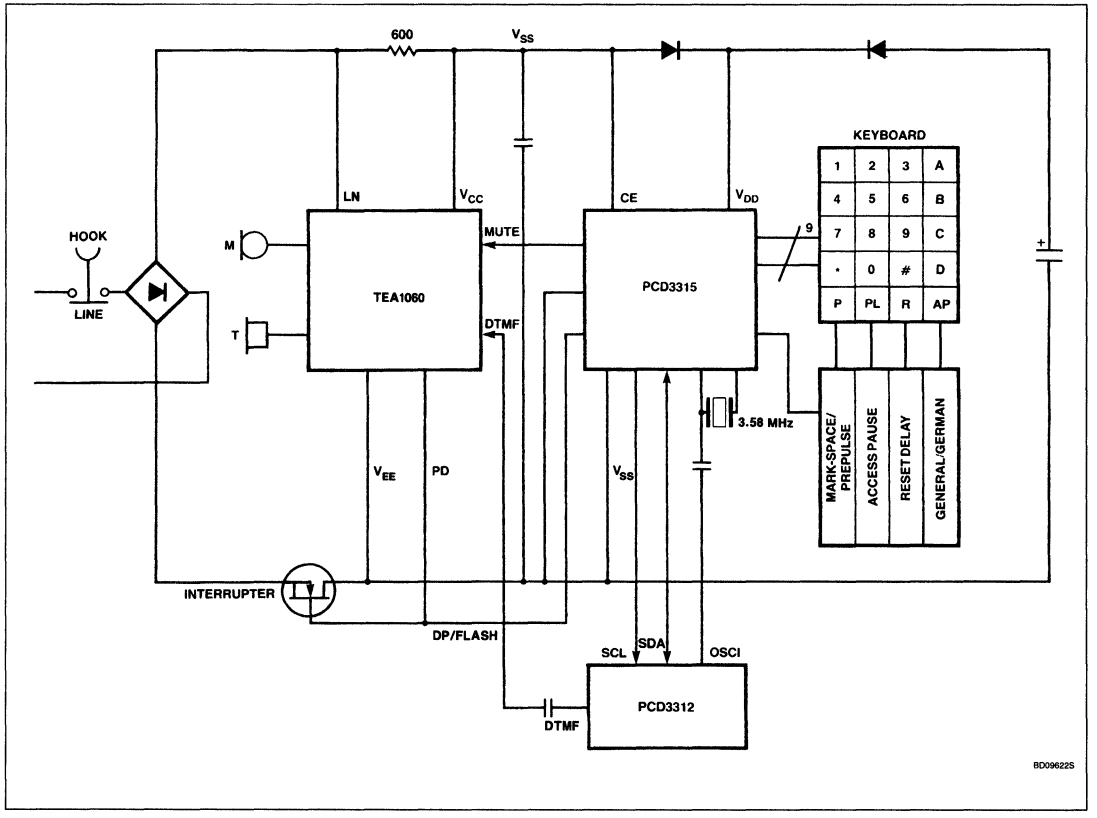


TOP VIEW

CD12950S

PIN NO.	SYMBOL	DESCRIPTION
1	IC	Internally connected
2	IC	Internally connected
3	IC	Internally connected
4	ROW 1	Scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	DIODE	Diode option output
10	$\overline{APO}$	Access-pause output
11	$\overline{HOLD}$	Hold input
12	CE	Chip-enable input
13	$\overline{PD}$/DTMF	Input to select pulse or DTMF dialing
14	V_{SS}	Negative supply
15	XTAL1	Crystal pins
16	XTAL2	
17	RESET	Reset input/output
18	COL 1	Sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	DP/FL	Dialing pulse and flash output
23	M1	Muting output
24	SDA	Serial data
25	SCL	Serial clock
26	IC	Internally connected
27	IC	Internally connected
28	V_{DD}	Positive supply

BLOCK DIAGRAM OF FEATURE PHONE



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage (Pin 28)	−0.8 to +8	V
V_I	All input voltages	0.8 to V_{DD} + 0.8	V
$\pm I_I$, $\pm I_O$	DC current into any input or output	10	mA
P_{TOT}	Total power dissipation	500	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C
T_J	Operating junction temperature	125	°C
θ_{JA}	Thermal resistance (junction-to-ambient) for SOT-117D for SOT-136A	 120 150	 °C/W °C/W

DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 6V, V_{SS} = 0V, T_A = −25 to +70°C; all voltages with respect to V_{SS}; f = 3.58MHz with R_S = 50Ω, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Supply voltage				
V_{DD}	operating	2.5		6	V
V_{DD}	STOP mode for RAM retention[1]	1.0		6	V
	Supply current				
	dialing mode				
I_{DD}	at V_{DD} = 3V		500		μA
	conversation mode				
I_{DD}	at V_{DD} = 3V		270		μA
	STOP mode[2]				
I_{DD}	at V_{DD} = 1.8V; T_A = 25°C		1.2	2.5	μA
I_{DD}	at V_{DD} = 1.8V; T_A = 55°C			5	μA
I_{DD}	at V_{DD} = 1.8V; T_A = 70°C			10	μA
RESET I/O					
V_{RESET}	Switching level		1.2	1.5	V
I_{OL}	Sink current at $V_{DD} > V_{RESET}$		7		μA
Inputs					
V_{IL}	Input voltage LOW	0		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD}	V
$\pm I_{IL}$	Input leakage current at $V_{SS} < V_I < V_{DD}$			1	μA
Outputs					
V_{OL}	Output voltage LOW at $V_I = V_{SS}$ or V_{DD}, $\|I_O\| < 1\mu A$			0.05	V
I_{OL}	Output sink current LOW at V_{DD} = 3V; V_O = 0.4V	0.6	1.5		mA
	Pull-up output source current HIGH (except SDA, SCL)				
$-I_{OH}$	at V_{DD} = 3V; $V_O = 0.9V_{DD}$	10			μA
$-I_{OH}$	at V_{DD} = 3V; $V_O = V_{SS}$			200	μA

NOTES:
1. Because RAM is cleared if POR is activated by software, this value must be max V_{RESET}
2. Crystal connected between XTAL1 and XTAL2, SCL and SDA pulled to V_{DD} via 5.6kΩ resistor, CE and $\overline{PD}$/DTMF at V_{SS}

6

FUNCTIONAL DESCRIPTION

Power Supply (V_{DD}; V_{SS})

The minimum supply voltage and supply current depend on the operating modes:

- Standby
- Conversation
- Dialing

(see Operational Description)

Oscillator (XTAL1; XTAL2)

The timebase for the PCD3315 is a crystal-controlled oscillator with a 3.58MHz quartz crystal connected between XTAL1 and XTAL2. The oscillator will run when the CE = HIGH. The output XTAL2 can drive the oscillator input of the PCD3312 via a capacitor.

Keyboard Inputs/Outputs (COL 1 to 4; ROW 1 to 5)

The sense column COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 4 are directly connected to a 4 × 4 single-contact keyboard matrix. An extra row (ROW 5) is added to address four additional function keys that are required for autodial functions. The keyboard organization is shown in Figure 1. Keyboard entries are valid 20ms (debounce time) after the leading edge and until 20ms after the trailing edge of the keyboard entry.

In pulse dialing mode, the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialing and are ignored.

In DTMF dialing mode, the 10 numeric keys and the 6 non-numeric keys are valid.

Diode Option Output (DIODE)

An extra row is added to the keyboard matrix to provide several selections:

- Access pause duration
- Reset delay time
- Mark/space ratio or prepulse yes/no
- General or German version

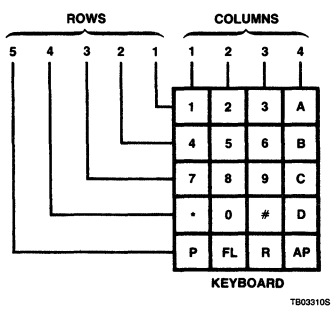


Figure 1. Keyboard Organization

Dialing Pulse and Flash Output (DP/FL)

This output drives the line interrupter circuit. In pulse dialing mode, it controls the timing for the line interrupter. This output also provides a "Flash" pulse which generates a 95ms line break. In the German version, this "Flash" occurs only in the DTMF dialing mode.

Chip Enable Input (CE)

The CE input is used for hook-detection. Hook-off will result in CE = HIGH. This will change the circuit state from standby to operational mode and also initialize the circuit.

When the circuit detects a line break longer than the reset delay time, it will switch the IC to the standby mode. This essentially achieves a low standby current during hook-on. During access pauses, the reset delay time is longer because the telephone line supply is switched over, which may result in longer line drops.

Mute Output (M1)

This output is active

- In pulse dialing mode; Mute = HIGH during interdigit pause plus dialing pulses
- In DTMF dialing mode; Mute = HIGH during DTMF bursts plus hold-over time
- During access pauses; Mute = HIGH during the mute hold-over time
- During flash; Mute = HIGH
- During programming

Hold Input ($\overline{HOLD}$); Access Pause Output ($\overline{APO}$)

The hold input suspends dialing after completion of the current digit, or in pulse dialing during the inter-digit pause.

The hold function facilitates an extra time delay during dialing under the control of external circuitry, i.e., a dialing tone recognizer.

In the hold state ($\overline{HOLD}$ = LOW), the muting output is also LOW, thus the IC is in the conversation mode. The $\overline{HOLD}$ input can be controlled by the access pause output ($\overline{APO}$) directly, or indirectly via a dialing tone recognizer (see Figure 2). The $\overline{APO}$ output will go LOW when an access pause is recognized.

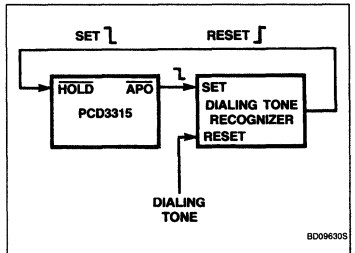


Figure 2. Automatic Variation of Length of an Access Pause Under the Control of a Dialing Tone Recognizer

Serial Data (SDA); Serial Clock (SCL)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialing mode (see Figure 4). Both outputs require external pull-up resistors.

Dialing Mode Selection Input ($\overline{PD}$/DTMF)

This input selects the dialing mode:

- $\overline{PD}$/DTMF = LOW selects pulse dialing
- $\overline{PD}$/DTMF = HIGH selects DTMF dialing

Reset Input/Output (RESET)

When the reset input is active High, it can be used to initialize the IC. In normal application, this is achieved by the CE input. Reset is also an output of the internal power-on reset circuit, which generates a reset pulse if V_{DD} drops below 1.3V (typ.).

OPERATIONAL DESCRIPTION

The PCD3315 has 3 operating modes:

- Standby
- Conversation
- Dialing

Standby Mode

When the chip enable input (CE) is LOW, the IC is in the standby mode. The oscillator is switched off and the IC requires only a standby current (1.2μA typ.) for memory retention.

The circuit will leave the standby mode and enter the conversation mode 0.5ms after CE becomes High.

Conversation Mode

In this mode, the IC is active in order to scan the keyboard entries. Mute and dialing pins are inactive. The current consumption is 270μA (typ.) at V_{DD} = 3V.

Dialing Mode

The IC will be switched to the fully-operational mode in the following circumstances:

- A valid keyboard entry
- Dialing mode
- Programming mode

The current consumption is 500μA (typ.) at V_{DD} = 3V.

The PCD3315 has two dialing modes:

- Pulse dialing direct via DP/FL output
- DTMF dialing via PCD3312 using the serial I/O lines SDA and SCL

Pulse Dialing

The timing sequence for pulse dialing is shown in Figure 3a. Output DP/FL starts with

an inter-digit pause, followed by a sequence of pulses corresponding to the digit for transmission. The dialing frequency is fixed at 10Hz; the break and make times are 60ms and 40ms, respectively.
In the general version with diode option, the user can also select break and make times of 67ms and 33ms, respectively.
The muting pulse will overlap the total dialing sequence. After dialing, the muting output (M1) goes LOW and the circuit is switched to the conversation mode.

DTMF Dialing
The timing sequence for DTMF dialing is shown in Figure 3b. The PCD3312 generates the selected DTMF tones via the serial I/O lines SDA and SCL. These tones are transmitted with minimum tone burst durations of 70.70ms (for the German version 80.80ms). The maximum tone burst duration is equal to the key depression time.
After dialing, the muting output goes LOW after a hold-over time of 80ms, and the circuit is switched to the conversation mode.

Normal Dialing
The IC has a working register with a maximum capacity of 18 positions. Entries in these positions may be:
- 10 numeric digits 0 to 9
- Manually-programmed access pauses
- 6 non-numeric special keys (*, #, A, B, C, D) in DTMF mode

If none of the special keys has been pressed, the contents of the working register will be stored automatically in the Redial Buffer. The number of digits can be extended to a maximum of 36, but this will result in a redial memory clear after hook-on. This is also valid for manual dialing after automatic dialing.

Automatic Dialing
In addition to manual dialing, the IC provides the following automatic functions:
- Redial of the last manually-dialed number (German version) or Redial of the last-dialed number (general version)
- Extended redial
- Electronic notepad
- Maximum of 10 repertory dialing numbers

The maximum capacity of the registers for these numbers is also 18 positions. The 6 non-numeric digits (*, #, A, B, C, D) will not be stored.

To achieve these automatic dialing functions, an extra row of the keyboard is required which contains the following special function keys:
- P programming/automatic dialing
- FL flash or register recall
- R redial
- AP manual access pause entry

Besides the operational procedure for automatic dialing, there are also procedures for programming these numbers into the memory (see Table 1).

Access Pause
During a dialing sequence, it may be necessary to insert a wait time to ensure correct dialing. A dialing sequence can always be interrupted by the $\overline{\text{HOLD}}$ input through an access pause recognition, which results in a fixed time delay.

There are three ways to enter an access pause:
- At manual dialing by pressing the AP key
- At auto dialing by recognition of the AP-code in the memory
- Recognition of PABX digits, after which an automatic access pause will be inserted

There are four ways to terminate an access pause:
- $\overline{\text{HOLD}}$, $\overline{\text{APO}}$ pins directly interconnected; after a fixed time delay of 3 or 5s in pulse dialing; 1 5 or 2.5s in DTMF dialing The fixed time delay is determined by a diode strap
- $\overline{\text{HOLD}}$, $\overline{\text{APO}}$ pins interconnected via an RC network; after a fixed time delay of 3 or 5s in pulse dialing; 1.5 or 2.5s in DTMF dialing — plus an additional time delay determined by the RC values
- $\overline{\text{APO}}$ pin enables a dialing tone recognizer, which controls the $\overline{\text{HOLD}}$ input (see Figure 2)
- $\overline{\text{HOLD}}$ input connected to V_{DD}, no access pause

During the access pause, the muting output remains active during hold-over time. In order to handle longer line drops during access pauses, the PCD3315 automatically switches to the maximum reset delay time of 320ms.

PABX Digits
The PCD3315 will detect pre-programmed PABX digits and insert an access pause in the dialing sequence. The reserved capacity is for two different PABX numbers with a maximum of 2 digits each.

Program procedure: $\overline{P} \cdot R \cdot d_1$, d_2 R d_3 d_4.

Notepad
In the conversation mode, the notepad procedure will overwrite the extended redial buffer, without dialing-out digits. After hook-off, this number can be recalled through the extended redial buffer.

Store procedure : P·P·TN P

Dial · P·R

Flash (see Figure 3b)
Flash or register recall is activated by the flash key which results in a timed line break at output pin DP/FL. This line break is of a fixed 95ms duration in both pulse and DTMF dialing modes. In the German version, it is only applicable to the DTMF mode.

Table 1. Keying Procedures for Dial and Program Operation

MODE	OPERATION	PROGRAM
Redial	R	Automatic
Extended redial	P·R	TN·P
Notepad	P·R	Dial·P·P·TN·P
Repertory dial	P·d	$\overline{P}$·d·TN
PABX digits	Automatic	$\overline{P}$·R·d_1 (d_2) R d_3 (d_4)
Reset autodial	Hook-on	
RAM	$\overline{2, 5, 8, 0}$	
	Hook-off	
	2, 5, 8, 0	

Where:
P = Press and release P-key
$\overline{P}$ = Press and keep P-key pressed
R = Press and release R-key
TN = Telephone number
d = Digit 0 to 9
$\overline{2, 5, 8, 0}$ = Press and keep pressed keys 2, 5, 8, and 0
2, 5, 8, 0 = Release keys 2, 5, 8, and 0

In the dialing procedure, a flash entry will initialize the IC and, thus, the working register which acts like a chip enable procedure.

Memory Clear

A built-in, manual total-memory clear to facilitate resetting of the autodial RAM after servicing, maintenance, or telephone set delivery exists.

Procedure: hook-on, press, and keep depressed keys 2, 5, 8, 0; hook-off, release keys 2, 5, 8, 0.

Program Security

Security measures are incorporated in the IC to avoid incorrect dialing operations and hang-ups.

The program has a built-in RAM check procedure to protect the autodial numbers stored in the RAM. If one or more bits of this RAM are changed during standby, or the battery falls below 1.3V (typ.), this will result in a memory clear to avoid subsequent incorrect dialing.

Diode Options

There are 4 different diode or strap options which are an extension of the keyboard matrix. Addressing is via the 4 columns and diode pins.

There are two possibilities:

- Without diode
- With diode (cathode on row-side)

The built-in selections are shown in Table 2.

Table 2. Diode Option Selections

COLUMN	DESCRIPTION	WITHOUT DIODE	WITH DIODE	REMARKS
4	Version	German	General	
1	Break, make-time	60, 40ms	67, 33ms	General version
1	Prepulse	No	Yes	German version
2	Access pause	3s	5s	Pulse dialing
2	Access pause	1.5s	2.5s	DTMF dialing
3	Reset delay time	160ms	320ms	

Table 3. Timing Date, General Version

SYMBOL	PARAMETER	MIN	TYP		UNIT
			Without Diode	With Diode	
t_{RDS}	Reset delay time		160	320	ms
t_{RDS}	Reset delay time during access pause		320	320	ms
t_{DB}	Keyboard debounce time		20	20	ms
t_{FL}	Flash time		95	95	ms
Pulse dialing					
f_D	Dial frequency		10	10	Hz
$t_{B/M}$	Break/make time		60/40	67/33	ms
t_{IDP}	Interdigit pause		840	840	ms
t_{AP}	Access pause		3	5	s
t_H	Mute hold-over time (only during access pause)		1	1	s
DTMF dialing					
t_T	Tone transmission time		70 or key-down time		ms
t_P	Tone pause time	70			ms
t_H	Mute hold-over time during dialing		150	150	ms
t_H	Mute hold-over time during access pause		1	1	s
t_{AP}	Access pause		1.5	2.5	s

Table 4. Timing Data, German Version

SYMBOL	PARAMETER	MIN	TYP		UNIT
			Without Diode	With Diode	
t_{RDS}	Reset delay time		160	320	ms
t_{RDS}	Reset delay time during access pause		320	320	ms
t_{DB}	Keyboard debounce time		20	20	ms
Pulse dialing					
f_D	Dial frequency		10	10	Hz
$t_{B/M}$	Break/make time		60/40	60/40	ms
t_{IDP}	Interdigit pause		840	840	ms
t_{AP}	Access pause		3	5	s
t_H	Mute hold-over time (only during access pause)		1	3	s
t_{PP}	Prepulse time			20	ms
DTMF dialing					
t_T	Tone transmission time		80 or key-down time		ms
t_P	Tone pause time	80			ms
t_H	Mute hold-over time during dialing		160	160	ms
t_H	Mute hold-over time during access pause		1	1	s
t_{AP}	Access pause		1.5	2.5	s
t_{FL}	Flash time		95	95	ms

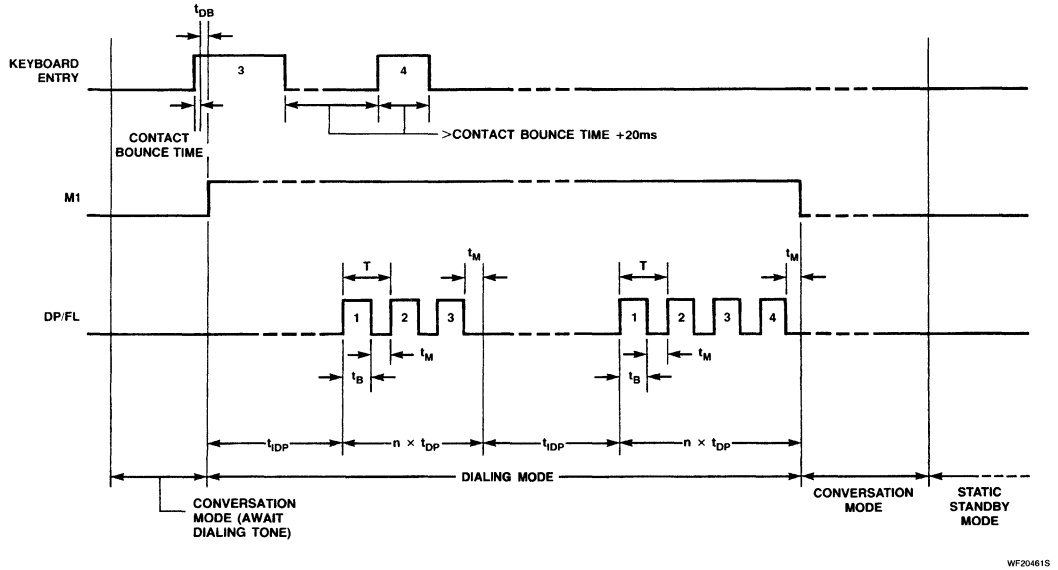


Figure 3a. Timing Diagram for Pulse Dialing Mode, Defined by $\overline{PD}$/DTMF = LOW (V_{SS})

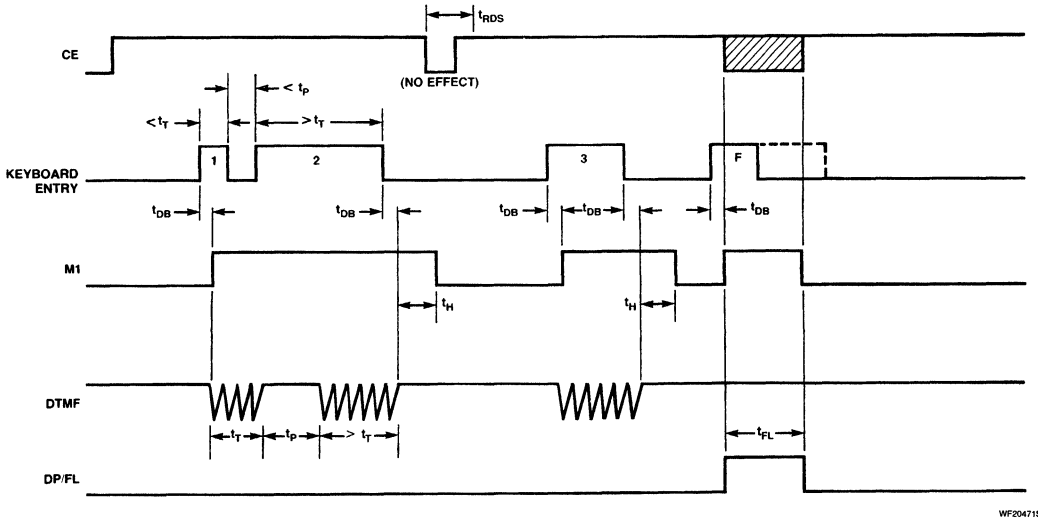


Figure 3b. Timing Diagram for DTMF Dialing Mode, Defined by $\overline{PD}$/DTMF = HIGH (V_{DD})

Signetics

PCD3341
CMOS Repertory Telephone Set Controller

Preliminary Specification

Linear Products

DESCRIPTION

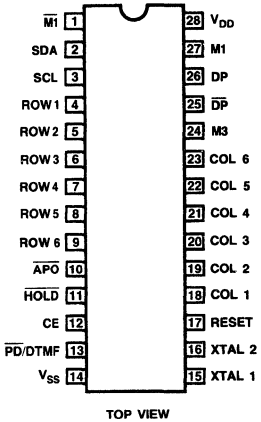
The PCD3341 is a low threshold voltage IC fabricated in CMOS. It is designed to control display, redial and repertory dialing in a telephone set. The IC has two dialing modes: Pulse Dialing (PD) and Dual Tone Multi-Frequency (DTMF). The architecture of the PCD3341 is identical to that of the PCD3343. It comprises an 8-bit CPU, 224 RAM bytes and 3k ROM bytes (the ROM is already programmed). The operating supply voltage is 2.5 to 6.0V with a low current consumption in all operating modes: Standby, conversation and dialing modes. Up to 18 digits and 2 manual access pauses can be stored for redial, extended redial and direct dial purposes together with on-chip storage for 10 repertory numbers.

For expansion of the system, the PCD3341 provides a two-wire serial input/output port, in accordance with the I^2C bus specifications, to control the DTMF tone generator, LCD drivers and additional RAMs for additional repertory numbers.

FEATURES

- **Pulse dialing**
- **DTMF dial control of tone generator PCD3312**
- **Redial/Extended Redial**
- **Electronic notepad**
- **Direct dialing (emergency call)**
- **On-chip storage for 10 repertory dial numbers**
- **18-digit capacity for each autodial memory**
- **Flash or register recall**
- **Manual reset of autodial RAM**
- **On-chip power-on reset**
- **Programmed for improved noise immunity**
- **Extension possible with external RAM for up to 110 repertory dial numbers**
- **Four extra function keys: Program/autodial, flash, redial, access pause**
- **Keyboard expansion possible for 10 separate repertory dialed numbers**
- **Automatic recognition of PABX digits resulting in an access pause insertion**
- **Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers**
- **Six diode or strap functions: Mark-to-space ratio, tone burst time, inter-digit pause time, access pause time, normal or expanded keyboard, normal or direct dialing**

PIN CONFIGURATION



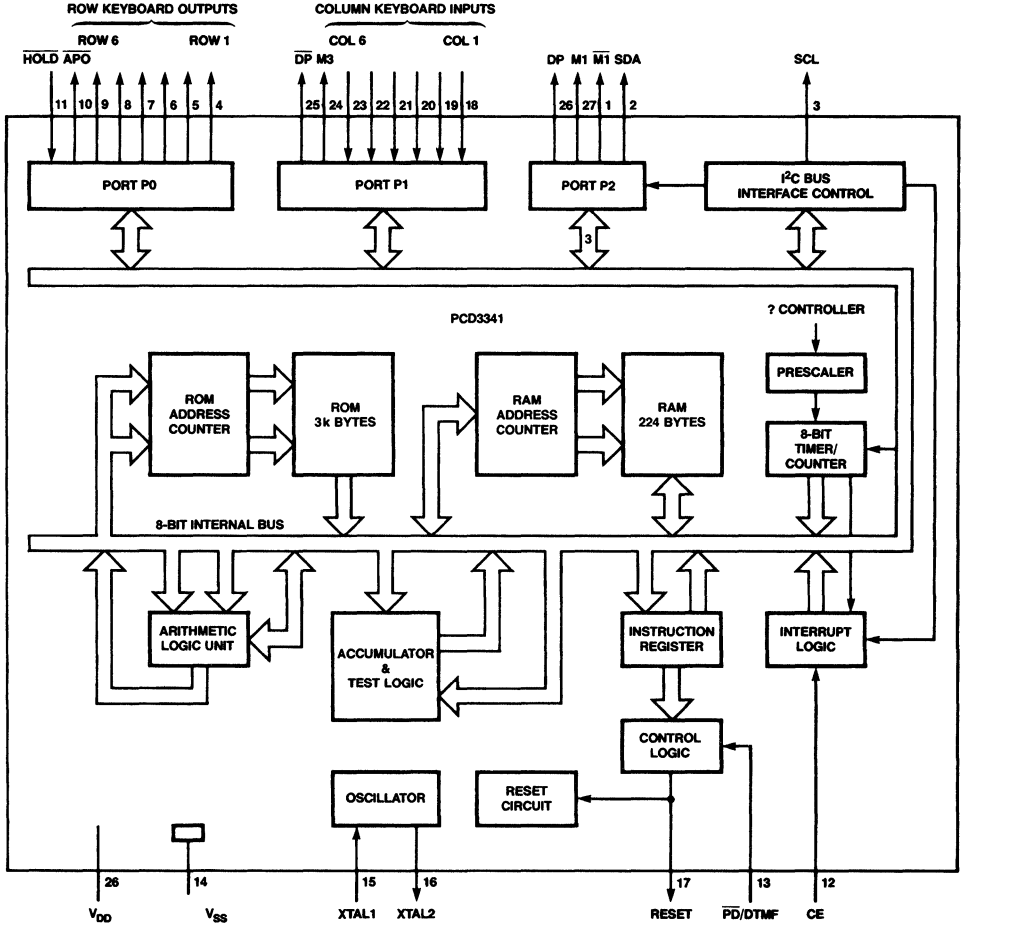
TOP VIEW

CD12951S

PIN NO.	SYMBOL	DESCRIPTION
1	$\overline{M1}$	Inverted output of M1
2	SDA	Serial data
3	SCL	Serial clock
4	ROW 1	Scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	ROW 6	
10	$\overline{APO}$	Access-pause output
11	$\overline{HOLD}$	Hold input
12	CE	Chip-enable input
13	$\overline{PD}$/DTMF	Input to select pulse or DTMF dialing
14	V_{SS}	Negative supply
15	XTAL1	Input to on-chip oscillator
16	XTAL2	Output from on-chip oscillator
17	RESET	Reset input/output
18	COL 1	Sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	COL 5	
23	COL 6	
24	M3	Muting output
25	$\overline{DP}$	Inverted pulse dialing output
26	DP	Pulse dialing output
27	M1	Muting output
28	V_{DD}	Positive supply

6

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic Dip (SOT-117D)	−25°C to +70°C	PCD3341TD
28-Pin Plastic SO (SO-28; SOT-136A)	−25°C to +70°C	PCD3341TD

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 28)	−0.8 to 8	V
$\pm I_I$, $\pm I_O$	DC current into any input or output	10	mA
V_I	All input voltages	V_{SS} − 0.8 to V_{DD} + 0.8	V
P_D	Total power dissipation	500	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3V; V_{SS} = 0V; crystal parameters: f_{OSC} = 3.57954MHz; R_S = 50Ω max.; T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Operating supply voltage Operating supply current	2.5	3	6.0	V
I_{DDC} I_{DDD}	Conversation mode (CE = 1) Dialing mode (CE = 1)		270 600		µA µA
V_{DDO}	Standby supply voltage (CE = 0)	1 8	3	6.0	V
I_{DDO}	Standby supply current (CE = 0)			2.5	µA
Reset I/O					
V_{RESET} I_{OL}	Switching level at $V_{DD} < V_{RESET}$ Sink current at $V_{DD} < V_{RESET}$		1.3 7	1.5	V µA
Inputs					
V_{IL} V_{IH}	Input voltage Low (any pin) Input voltage High (any pin)	0 0 7V_{DD}		0.3V_{DD}	V V
$-I_{IL}$ I_{IL}	Input leakage current; CE at $V_I = V_{SS}$ to V_{DD} at CE = 1			100 1	nA µA
Keyboard contact resistance					
R_{KON} R_{KOFF}	Keyboard ON Keyboard OFF	100		1	kΩ kΩ
Outputs					
I_{OL} $-I_{OH}$	M1, M1, M3, DP, DP Output sink current at V_{OL} = 0.4V Output source current at V_{OH} = 2.6V (push-pull)		1.5 1.5		mA mA
I_{OL} $-I_{OH}$	SDA, SCL Output sink current at V_{OL} = 0.4V at V_{OH} = 0 to V_{DD} (open drain)	1.5		1	mA µA

6

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

Power supply must be retained for data storage.

Clock Oscillator (XTAL1; XTAL2)

The time base for the PCD3341 is a crystal controlled, on-chip oscillator which is completed by connecting a 3.58MHz crystal between XTAL1 and XTAL2. The oscillator starts when V_{DD} reaches the operating voltage level and CE = High. The output XTAL2 can be used to drive the oscillator input of the PCD3312.

Chip Enable (CE)

This active-High input is used to initialize part of the system, to select the operational or standby mode, and to handle line power breaks.

Pulse Dialing Outputs (DP; $\overline{DP}$)

DP output drives an external switching transistor or relay in pulse dialing mode. This output is also used to pulse out a calibrated FLASH pulse (recall register) of 90ms duration as soon as the keyboard input FLASH is activated by depressing the key F. The FLASH function acts like CE with respect to redial.

Muting Outputs (M1; $\overline{M1}$; M3)

M1 output is used for muting during the dialing sequence For pulse dialing, M1 goes High with the first inter-digit pause and remains active for 33 or 40ms (mark-to-space selection) following the last break pulse after the last digit held in store has been transmitted. In DTMF dialing, input PD/DTMF is High. M1 is High as long as two out of the eight frequency signals are sent, then remains High for an additional 80ms (hold-over time). $\overline{M1}$ output is the inverted output of M1.

M3 output is an AND function, with $\overline{DP}$ and M1 as input, used for direct drive of a switching transistor for dialing pulses and muting.

Hold input ($\overline{HOLD}$; Access Pause Output ($\overline{APO}$)

The hold input suspends dialing after completion of the current digit, or in pulse dialing during an inter-digit pause.

The hold function facilitates an extra time delay during dialing under control of external circuits (dialing tone recognized). In the hold state ($\overline{HOLD}$ = Low), the muting output is also Low, thus the IC is in the conversation mode. The $\overline{HOLD}$ input can be controlled by the access pause output (APO) directly or indirectly via a dialing tone recognizer (see Figure 1). The tone recognizer automatically terminates access pauses upon receipt of the access tone, regardless of whether this occurs during or after the access pause time (t_{AP}). The $\overline{APO}$ output will go Low when an access pause is recognized.

Serial Data (SDA); Serial Clock (see Figure 4)

The serial I/O lines, SDA and SCL, are used to control the PCD3312 in the DTMF dialing mode, additional RAMs (PCD8570) for repertory and LCD drivers (PCF8577). Both outputs require external pull-up resistors.

Keyboard Inputs/Outputs (COL 1 to 6; ROW 1 to 6)

The sense column inputs, COL 1 to COL 6 and the scanning row outputs ROW 1 to ROW 6, are directly connected to a 4x4 single contact keyboard matrix. The keyboard organization is shown in Figure 2. In the pulse dialing mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialing. In the DTMF dialing mode, the 10 numeric keys and the 6 non-numeric keys are valid. On-chip repertory dialing uses the 10 numeric numbers (no external RAM).

With extended repertory dialing, 10 extra keys (M1 to M10) are used (on-chip or external RAM). Row 5 of the keyboard contains the following special function keys:

- P Memory clear and programming (notepad)
- FL Flash or register recall
- R Redial
- AP Manual access pause entry

Diode Options (ROW 6)

ROW 6 is added to the keyboard matrix to provide the following selections:

Mark-to-space ratio (M/S)
OFF M/S 3:2
ON M/S 2:1

Tone burst time (t_{TB})
OFF t_{TB} = 70ms
ON t_{TB} = 100ms

Inter-digit pause (IDP)
OFF IDP = 900ms
ON IDP = 500ms

Access pause time (t_{AP})
OFF t_{AP} = 1.5s (DTMF; 3s (PD))
ON t_{AP} = 2.5s (DTMF; 5s (PD))

Keyboard expansion (EKB)
OFF normal keyboard
ON expanded keyboard

Normal/direct call (N/D)
OFF normal call mode
ON direct call (emergency)

Dialing Mode Selection Input ($\overline{PD}$/DTMF)

This input selects the dialing mode:

- $\overline{PD}$/DTMF = Low selects pulse dialing
- $\overline{PD}$/DTMF = High selects DTMF dialing

Reset Input/Output (RESET)

When the reset input is active-High, it can be used to initialize the IC. In normal application this is achieved by the CE input. Reset is also an output of the internal power-on reset circuit, which generates a reset pulse if V_{DD} drops below 1.3V (typ.).

OPERATION

The PCD3341 has 3 operating modes:

- Standby
- Conversation
- Dialing

Standby Mode

When the chip enable input (CE) is Low, the IC is disabled. In the standby mode, the only current drawn is from a back-up supply (battery or line powered) for memory retention, holding up to 13 call numbers for repertory and redialing.

Conversation Mode

After the handset is lifted, CE is activated and V_{DD} rises to the working voltage. M1 muting is inactive and speed or dial tone can be heard. With the oscillator operating, the chip is ready to accept keyboard entries. Current consumption is $< 300\mu A$.

Dialing Mode

The dialing mode starts with first valid keyboard entry when it initiates:

- a normal call of a newly dialed number

or

- a repertory or redialing cycle of previously entered and stored numbers

The current consumption is $< 600\mu A$.

Pulse Dialing ($\overline{PD}$/DTMF = Low)

The keyboard entry initiates a recall from a previously stored number, or is a simultaneous keying-in and pulsing-out activity, with storing for possible later recall. If in the recalled number or at keying-in the keys *, #, A, B, C, D keys are used, these digits will not be transmitted. Normally, keying-in is followed by an inter-digit pause of 900 or 500ms duration (diode option IDP), followed by a sequence of pulses corresponding to the present digit in store. Each pulse starts with a mark (line break) followed by space (line make).

The pulse period is 100ms with a mark-to-space ratio of 3:2 or 2:1 (diode option). After transmission of a digit, the next digit will be

processed again, starting with an inter-digit pause. The pulsing is suspended if $\overline{HOLD}$ goes Low. It will be terminated if the current memory content has been transmitted, or the handset is replaced (CE = Low < t_{RD}). The pulses are available on the DP line. After completion of the number string, M1 goes Low and the circuit changes from the dialing mode to the conversation mode.

Dual Tone Multi Frequency Dialing ($\overline{PD}$/DTMF = HIGH)

The PCD3341 converts keyboard inputs into serial data via the I^2C bus lines SDA and SCL, suitable for control of the PCD3312 DTMF tone generator. These tones are transmitted with minimum tone burst durations of 70.70ms. The maximum tone burst duration is equal to the key depression time. With redial and repertory dialing, tones are automatically fed at a rate of 70.70ms. After dialing, the muting output goes Low after a hold-over time of 80ms, and the circuit is switched to the conversation mode.

SYSTEM EXTENSION

The PCD3341 can control the extensions of a telephone set via its I^2C bus. Both in DTMF dialing and pulse dialing, an extended repertory dialer provides more than 10 stored on-chip numbers, and the indication on an LC display of all keys pressed (programming or dialing procedure).

The following ICs can be used in combination with the PCD3341:

- PCD3312 DTMF generator
- PCD8570 256 x 8 static CMOS RAM
- PCF85772 LCD drivers in LCD module

DTMF Dialing

By using a PCD3312 DTMF generator with I^2C bus interface, the PCD3341 may be extended to Dual Tone Multi Frequency dialing applications. This is selected when the input pin $\overline{PD}$/DTMF = High. DTMF dialing is much faster than pulse dialing. Each keypad digit corresponds to a unique combination of two frequencies: One from a group of 4 high frequencies, and one from a group of 4 low frequencies. Both frequencies are applied simultaneously to the line. The PCD3341 is capable of directly driving the PCD3312 oscillator.

Repertory Dialing

If more than 10 stored numbers are required, repertory dialing can be extended by the I^2C bus lines and external CMOS RAMs (PCD8570) with serial interface. With a RAM capacity of 256 × 8 bits, another 20 stored numbers can be added. A maximum of 5 external RAMs can be served by the PCD3341 directly. This provides a telephone with a total capacity of 110 (100) stored numbers. The number of external RAMs connected on the I^2C bus lines is automatically checked by the PCD3341 at initial turn-on.

To identify each RAM, the PCD8570 has 3 hardware address pins (A2, A1, A0) which allow a maximum of 8 RAMs to be connected

Display

To display the dialed phone number or programmed number, the PCD3341 provides the signals to control an LC Display module using two PCD8577 duplex drivers These signals are fed via the I^2C bus lines. In the dialing and programming modes, the digits are displayed from right to left in the sequence entered by the keyboard. The access pause is indicated by the bar If the number of digits exceeds 16, they drop out on the left side of the display

OPERATING PROCEDURE

Initialization

At the first application of the standby power supply, the PCD3341 will clear the RAM in order to avoid a wrong content By lifting the handset, the buffer capacitor for V_{DD} is charged to the operating voltage. CE will then be activated. Within start-up time, the oscillator starts and the initialization program begins.

Automatic Access Pause Setting

Before the start procedure, the system can also be initialized by setting the access pause system (e.g., for PABX applications) The circuit will automatically insert an access pause after recognition of access of a number within a digit group This (or these) digit(s) must be programmed. Up to a maximum of 3 digits per group can be programmed.

The procedure is as follows.

- Depress and hold pushbutton P
- Press and release pushbutton R
- Enter 1, 2 or 3 digits as access digit for first group
- Release pushbutton P (only if no second group is required)
- Press and release pushbutton R
- Enter 1, 2 or 3 digits for second group
- Release pushbutton P

Apart from the procedure that automatically detects and inserts access pause(s), a telephone number with up to 2 additional manually inserted access pauses can be dialed or programmed by pressing button AP. In DTMF dialing mode, each access pause has a duration of 1.5 or 2.5 seconds. In the PD mode, each access pause has a duration of 3 or 5 seconds.

Data Entry

The debounce keyboard entries are written into the on-chip CMOS RAM in consecutive order.

Dialing

If the first pushbutton pressed is 0 to 9 in pulse dialing, or 0 – 9, A to D, *, # in DTMF dialing, digits are entered into the redial register after initial clearing. During the data entry, the circuit starts with the transmission of the call, and is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed Up to 18 digits can be stored in the redial register. After the main store overflows, a 10 digit First-In/First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register, this position is automatically cleared to provide space for the storage of new data. In this way, the total number that can be transmitted is unlimited, provided the key-in rate is not excessive. However, if the FIFO register overflows (more than 10 digits in store), further input will be ignored.

Redial

If the first digit entered is "REDIAL", R, the stored number in the redial register will be recalled and transmitted. If the current content is less than 18 digits, new digits entered are appended automatically to the redial number. After the 18th digit has been entered, the FIFO register will take over as previously described in the dialing section.

Extended Redial

The dialed number is saved in the extended redial buffer if pushbutton P is the last key pressed before the handset is replaced

Pressing and releasing pushbutton P, followed by pressing and releasing R, will cause the extended redial register to be recalled and transmitted in the same manner as by

Table 1. Repertory Number Organization

PCD8570 ADDRESS			KEYBOARD DIGIT(S)	
A2	A1	A0	Without EKB	With EKB
0	0	0	10 to 29	00 to 19
0	0	1	30 to 49	20 to 39
0	1	0	50 to 69	40 to 59
0	1	1	70 to 89	60 to 79
1	0	0	90 to 99	80 to 99
PCD3341			00 to 09	M1 to M10

redial. If fewer than 18 digits are contained in the extended redial register, digits can be added until the total content is 18. After the 18th digit the FIFO register will take over as before. The original number is not affected by the new digits.

Direct Call/Emergency Call

This is a diode option usually operated by a turn key switch. If set, the programmed number will be dialed by pressing *any* key. In the normal mode, the turn key switch is positioned OFF, with the diode option OFF.

"Programmed" is achieved by lifting the handset, depressing the P pushbutton with the key in the OFF position, then turning the key switch to the ON position (diode option ON). The required telephone number is now entered. Pushbutton P can now be released and the handset replaced.

After programming, the key switch can remain in the ON position (activating emergency call), or be switched off (normal mode). If the key switch is in the ON position, emergency calling is possible by removing the handset and pressing *any* pushbutton.

Repertory Dialing

The PCD3341 has an on-chip CMOS RAM to store up to ten 18 digit numbers, and can be extended up to 100 (110) numbers using CMOS RAMs with 2-line serial interface. The circuit automatically checks the number of external RAMs If no external RAM is connected, the on-chip repertory is limited to 10 numbers. In this application the standard keypad (0 to 9) and one digit address can be used. With the diode option EKB (expanded keyboard) ON, the extended keypad matrix (M1 to M10) can be used to access the on-chip repertory. If external RAMs are connected, the capacity of the repertory can be increased up to 100 (110) numbers. In this application, the standard keypad (0 to 9), and/or the extended keypad (M1 to M10), can be used to access the repertory (see Table 1).

Programming is possible only after the handset is lifted and no pushbutton is operated before P. Programming is achieved by pushbutton P being continually depressed, entering the repertory address of one or two digits, followed by the number (including access digits), then releasing pushbutton P. The designated telephone number, including access digits, is dialed after pressing pushbutton P followed by the address. With the extended keypad, a single address pushbutton is required. After transmission of the repertory sequence, it is possible to manually enter additional digits (see Redial).

Table 2. Display Indications

PROCEDURE	KEY PROCEDURE	DISPLAY INDICATION
Programming automatic access pauses after access digits	$\overline{P}$R00R9	Pr-00-9
Dialing	004627530	00-4627530
Redial	R	r = 00-4627530
Extended redial programming dialing	004627530 PR	00-4627530P Pr = 00-4627530
Emergency redial programming dialing	N/D OFF, $\overline{P}$, N/D ON (+TN) N/D ON any key	PH-00-4627530 H = 00-4627530
Repertory programming dialing	$\overline{P}$12004627530 $\overline{P}$12	P12-00-4627530 P12 = 00-4627530
Repertory with extended keyboard programming dialing	$\overline{P}$M1004627530 M1	PM1-00-4627530 M1 = 00-4627530
Note pad programming	PP0080808P	7530PP00-808080P
Note pad dialing	PR	00-808080
Error	Incorrect key procedure	≡

NOTES:
Where: TN = Telephone number
P = Depress and release pushbutton P
$\overline{P}$ = Depress pushbutton P continually during programming
R = Depress and release pushbutton R

Successive Repertory Dialing During a Call (Chain Dialing)

It is possible to dial more than one repertory number during one single telephone call. The following procedures are possible:

- Redial, extended redial, or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial, followed by one or more repertory numbers

Note Pad

Note pad provides the facility to store a number during the conversation mode without dialing and muting. This number will be stored in the extended redial register and recalled with the extended redial procedure. The programming procedure is as follows:

- Depress and release pushbutton P
- Depress and release pushbutton P
- Enter the telephone number
- Depress and release pushbutton P

If a wrong number is entered, correction is achieved by restarting the programming procedure.

A built-in memory clear facilitates resetting of the autodial RAM after servicing, maintenance or telephone set delivery. The procedure is as follows:

- Hook-on, depress and keep depressed keys 2, 5, 8, and 0
- Hook-off, release keys 2, 5, 8, and 0

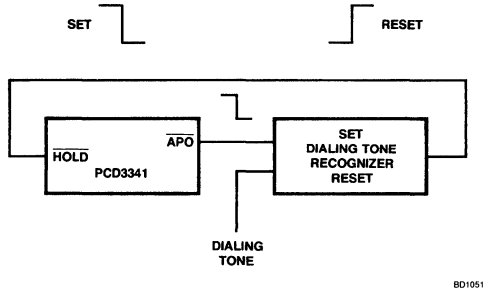


Figure 1. Automatic Variation of Length of an Access Pause Under Control of a Dialing Tone Recognizer

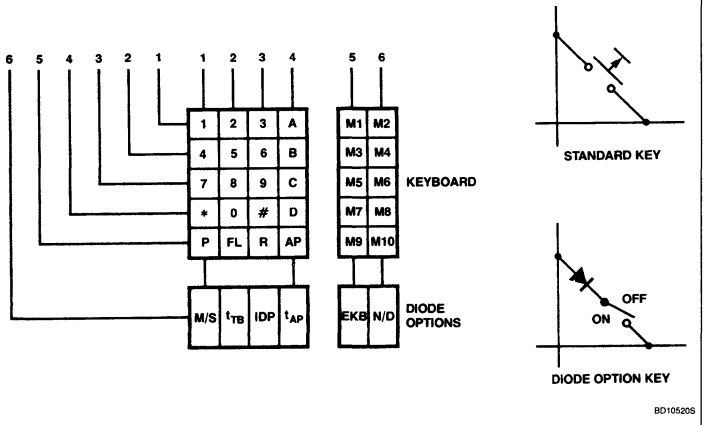


Figure 2. Keyboard Organization

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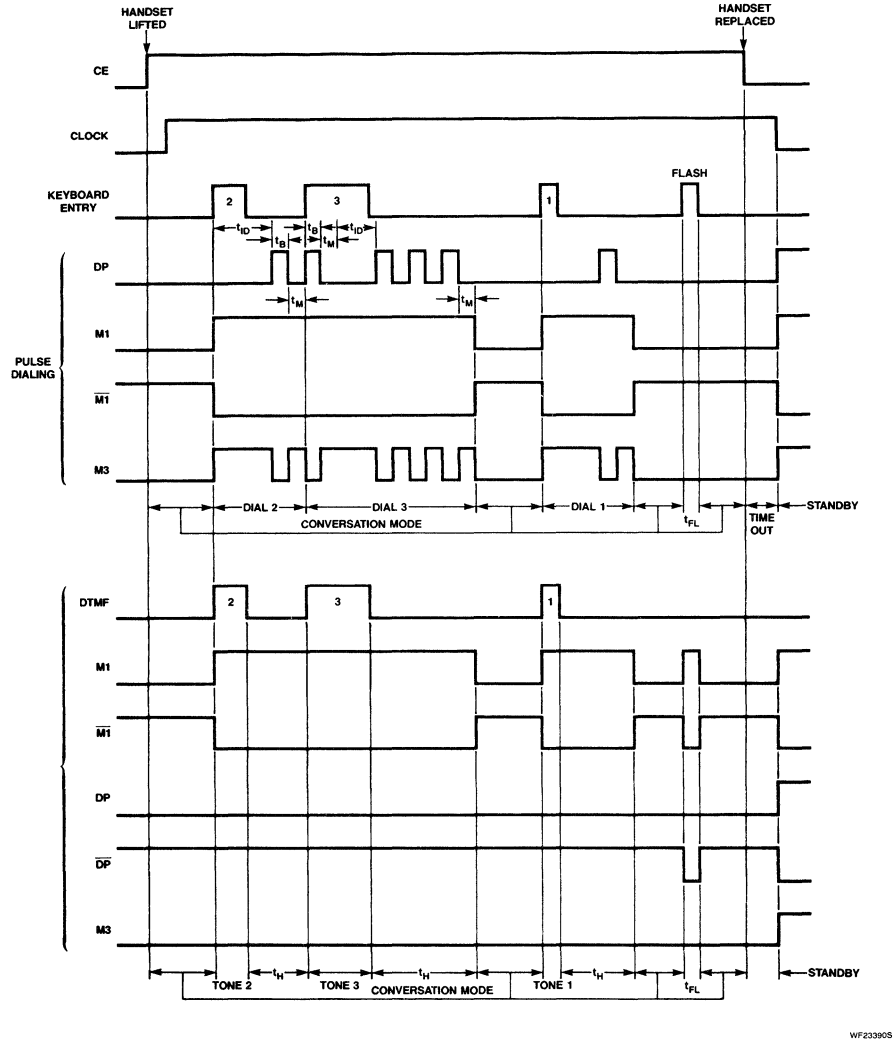

Figure 3. Pulse Dialing; DTMF Dialing

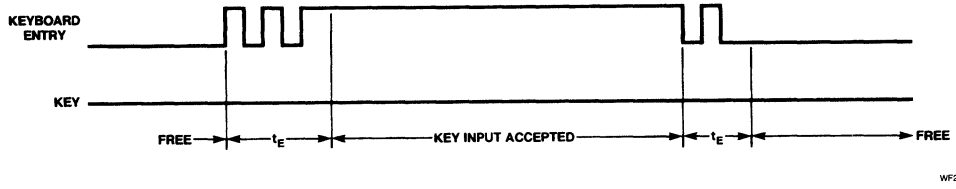

Figure 4. Keyboard Entry With Noise Debounced

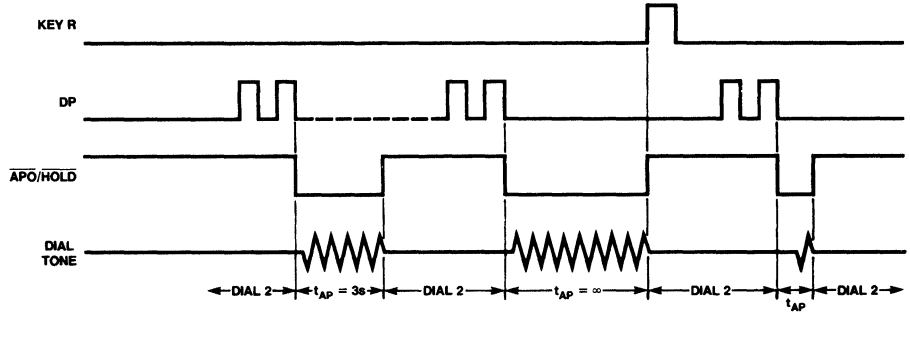

Figure 5. Access Pause With Reset BY, Internal 3s Timer, Key R, Tone Recognizer

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CMOS Repertory Telephone Set Controller PCD3341

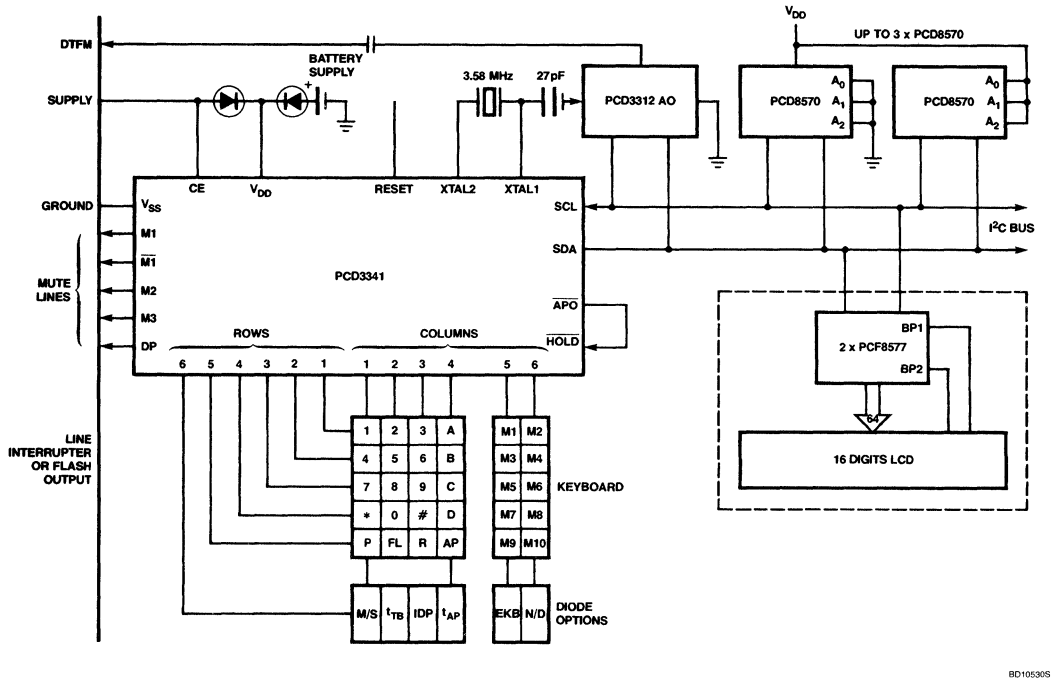


Figure 6. PCD3341 in Combination With PCD3312 (DTMF Dialer), PCD8570 (2k RAM) and PCF (Display Drivers)

Signetics

PCD3343
CMOS Microcontroller for Telephone Sets

Product Specification

Linear Products

DESCRIPTION

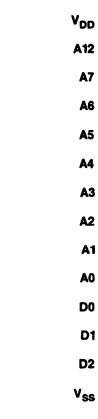
The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS. It has special on-chip features for application in telephone sets. The device is mask-programmable, designed to provide telephone dialing facilities such as redial, repertory dial, emergency call, keyboard scan, and pulse dial and/or DTMF dial via dedicated peripheral.

FEATURES

- **8-bit CPU, ROM, RAM, I/O in a single 28-lead DIP or SO package**
- **3K ROM bytes**
- **224 RAM bytes**
- **20 quasi-bidirectional I/O port lines**
- **Two test inputs: one of which is also the external interrupt input (CE/$\overline{TO}$)**
- **Single-level vectored interrupts: external, timer/event counter, serial I/O**
- **Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)**
- **8-bit programmable timer/event counter**
- **Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)**
- **All instructions 1 or 2 cycles**
- **Clock frequency 100kHz to 10MHz**
- **Single supply voltage from 1.8V to 6V**
- **Low standby voltage and current**
- **STOP and IDLE mode**
- **On-chip oscillator with output drive capability for peripherals (e.g., PCD3312 DTMF generator)**
- **Configuration of all I/O port lines individually selected by mask: pull-up, open-drain or push-pull**
- **Power-on reset circuit and low supply voltage detection**

PIN CONFIGURATION

PCF84C00B "Piggy-back" Version Top Pinning



TOP VIEW

CD11470S

PIN NO.	SYMBOL	DESCRIPTION
14, 22	V_{SS}	Ground
1, 26 – 28	V_{DD}	Power supply
10 – 3, 25, 24, 21, 23, 2	A0 – A12	Address outputs
11 – 13, 15 – 19	D0 – D7	Data
20	$\overline{PSEN}$	Program store enable

NOTES:
1. RAM capacity of PCF8500B is 256 bytes
2. Access time for ROMS/EPROMS to be below $7 \times 1/f_{XTAL}$
3. Pin 12 CE/$\overline{TO}$ is on the PCF84C00B, inverted and labeled $\overline{INT}$/TO

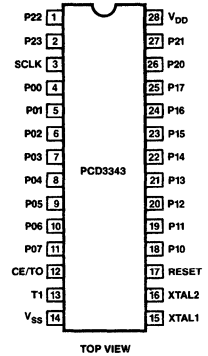
- **Reset state of all ports individually selected by mask**
- **Operating temperature range: –25 to +70°C**

APPLICATIONS

- **Feature phones**
- **Pay telephones**
- **Control application with low voltage/current requirements**

PIN CONFIGURATION

D, N Package



TOP VIEW

CD11480S

PIN NO.	SYMBOL	DESCRIPTION
3	SCLK	**Clock:** Bidirectional clock for serial I/O
4 – 11	P00 – P07	**PORT 0:** 8-bit quasi-bidirectional I/O port
12	CE/$\overline{TO}$	**Interrupt/Test 0:** External interrupt input (sensitive to positive-going edge)/test input pin, when used as a test input directly tested by conditional branch instructions JTO and JNTO
13	T1	**Test 1:** Test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction
14	V_{SS}	**Ground:** Circuit ground potential
15	XTAL1	**Crystal input:** Connection to timing component (crystal) which determines the frequency of the internal oscillator, also the input for an external clock source
16	XTAL2	Connection to the other side of the timing component
17	RESET	**Reset input:** Used to initialize the processor (active High), or output of power-on-reset circuit
18 – 25	P10 – P17	**Port 1:** 8-bit quasi-bidirectional I/O port
26, 27, 1, 2	P20 – P23	**Port 2:** 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode
28	V_{DD}	**Power supply:** 1.8V to 6V

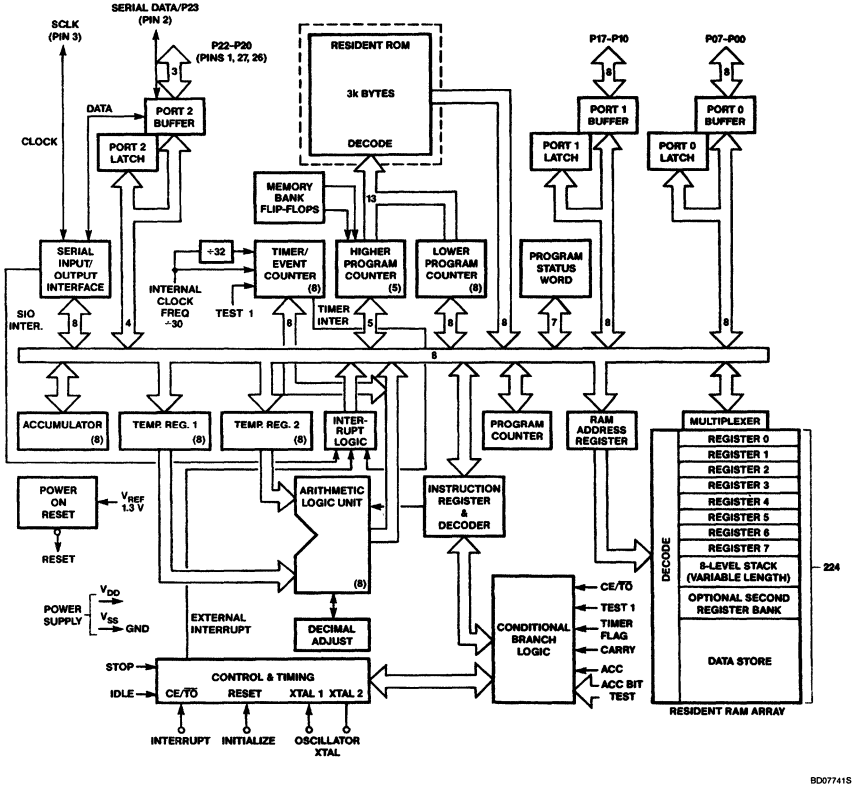
NOTE:
CE/$\overline{TO}$ is labeled $\overline{INT}$/TO on the PCF84C00B and has inverted polarity

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	–25°C to +70°C	PCD3343PN
28-Pin Plastic SO Package (SO-28, SOT-136A)	–25°C to +70°C	PCD3343TD

CMOS Microcontroller for Telephone Sets PCD3343

BLOCK DIAGRAM



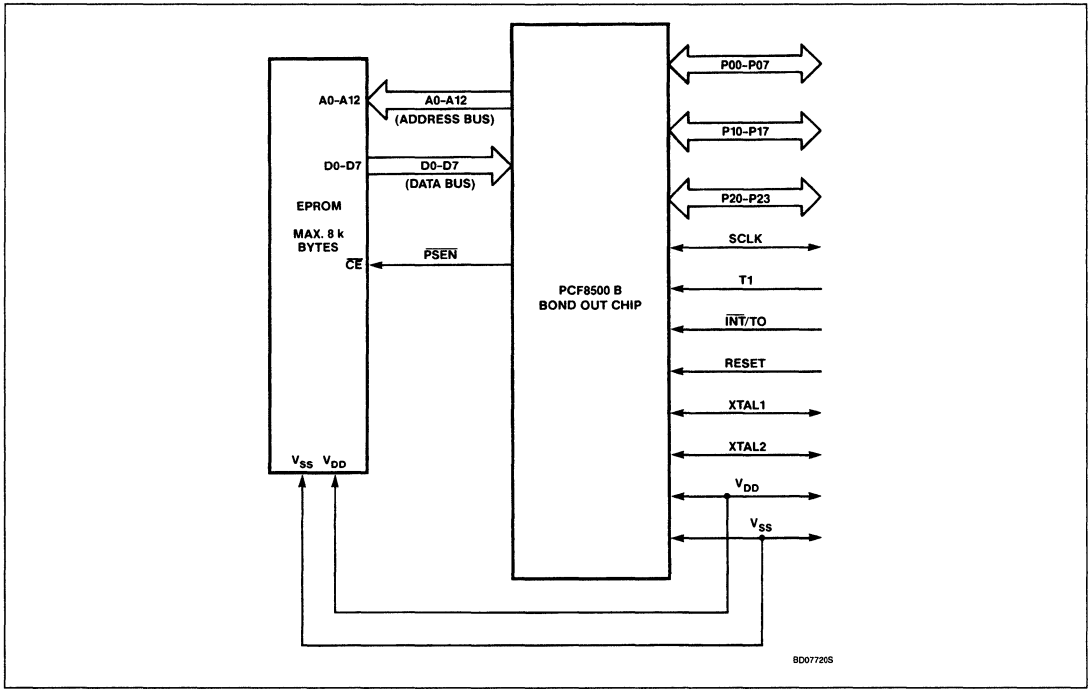
a.

Replacement of Dotted Part in Block Diagram for the PCF84C00T ROM-less Version

b.

Replacement of Dotted Part in Block Diagram for the PCF84C00B "Piggy-back" Version

Connection of EPROM to 'Piggy-back' Package PCF8500B



6

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage (Pin 28)	−0.8 to +8	V
V_I	All input voltages	0.8 to V_{DD} + 0.8	V
$\pm I_I$, $\pm I_O$	DC current into any input or output	10	mA
P_{TOT}	Total power dissipation[1]	500	mW
	Power dissipation per output		
P_O	except P23, SCLK	50	mW
P_O	P23, SCLK	180	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C
T_J	Operating junction temperature	125	°C

NOTES:

1. Thermal resistance (junction to ambient)
   for SOT-117D θ_{JA} max. = 120°C/W
   for SOT-135A θ_{JA} max. = 60°C/W.
   for SOT-136A θ_{JA} max. = 150°C/W

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.75 to 6V; V_{SS} = 0V, T_A = −25°C to +70°C; all voltages with respect to V_{SS}; f = 3.58MHz with R_S = 50Ω, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Supply voltage				
V_{DD}	operating (see Figure 20)	1.8		6	V
V_{DD}	STOP mode for RAM retention	1.0		6	V
	Supply current				
I_{DD}	operating				
	at V_{DD} = 3V (see Figure 21)		600		μA
I_{DD}	IDLE mode				
	at V_{DD} = 3V (see Figure 22)		300		μA
I_{DD}	STOP mode (see Figure 23)[1]				
	at V_{DD} = 1.8V; T_A = 25°C		1.2	2.5	μA
	at V_{DD} = 1.8V; T_A = 55°C			5	μA
	at V_{DD} = 1.8V; T_A = 70°C			10	μA
Reset I/O					
V_{RESET}	Switching level		1.3		V
	Sink current				
I_{OL}	at $V_{DD} > V_{RESET}$		7		μA
Inputs					
V_{IL}	Input voltage Low	0		$0.3V_{DD}$	V
V_{IH}	Input voltage High	$0.7V_{DD}$		V_{DD}	V
	Input leakage current				
$\pm I_{IL}$	at $V_{SS} < V_I < V_{DD}$			1	μA
Outputs					
	Output voltage Low				
V_{OL}	at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1\mu A$			0.05	V
	Output sink current Low				
I_{OL}	at V_{DD} = 3V; V_O = 0.4V except P23/SDA, SCLK (see Figure 24)	0.75	1.5		mA
I_{OL}	P23/SDA, SCLK (see Figure 25)	1.5			mA
	Pull-up output source current High (see Figure 26)				
$-I_{OH}$	at V_{DD} = 3V; $V_O = 0.9V_{DD}$	25			μA
$-I_{OH}$	at V_{DD} = 3V; $V_O = V_{SS}$			200	μA
	Push-pull output source current High				
$-I_{OH}$	at V_{DD} = 3V; $V_O = V_{DD} - 0.4V$	0.75	1.5		mA

NOTE:
1 Crystal connected between XTAL 1 and XTAL 2, SCL and SDA pulled to V_{DD} via 5.6kΩ resistor, CE and T1 at V_{SS}

AC ELECTRICAL CHARACTERISTICS

Rise and fall times between 10 and 90% levels, C_L = 50pF

SYMBOL	PARAMETER	At 70°C Maximum Value			UNIT
V_{DD}	Supply voltage	1.8	3.0	6.0	V
t_F	Fall time	200	100	70	ns
t_R	Rise time	200	100	80	ns

FUNCTIONAL DESCRIPTION

Bond-Out Version PCF84C00B

The PCF84C00B is a microcontroller that contains no on-board ROM, but has all address and data lines brought out to access an external ROM or EPROM. This version has more pins than the PCD3343 with on-board ROM. The RAM has 256 bytes. It can address 8k bytes of ROM.

'Piggy-Back' Version PCF84C00B

The PCF84C00B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIP package. The RAM has 256 bytes and can also address 8k bytes of program memory.

Program Memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 1 shows the program memory map.

Four program memory locations are of special importance:

- Location 0: contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3: contains the first byte of an external interrupt service subroutine,
- Location 5: contains the first byte of a serial I/O interrupt service subroutine,
- Location 7: contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2k bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data Memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 2 shows the data memory map.

Working Registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1 designates locations 24 to 31 as working registers instead of locations 0 to 7, and they are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines, saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0′, and R1′, which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

Program Counter Stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Figure 3) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines

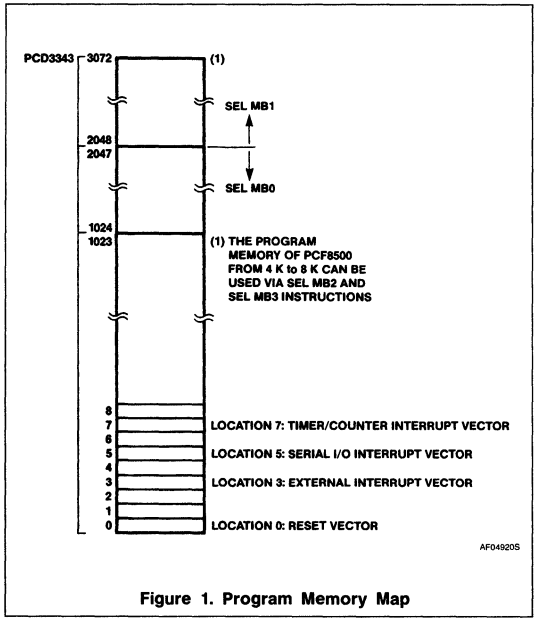


Figure 1. Program Memory Map

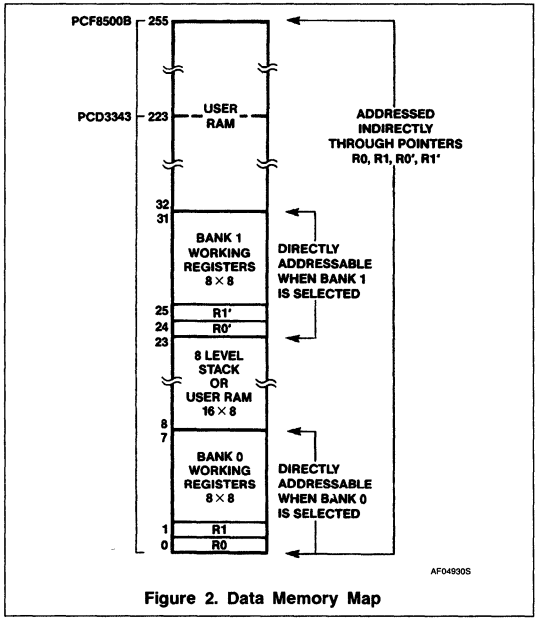


Figure 2. Data Memory Map

which of the eight register pairs of the program counter stack will be loaded with the next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6, and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur, the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

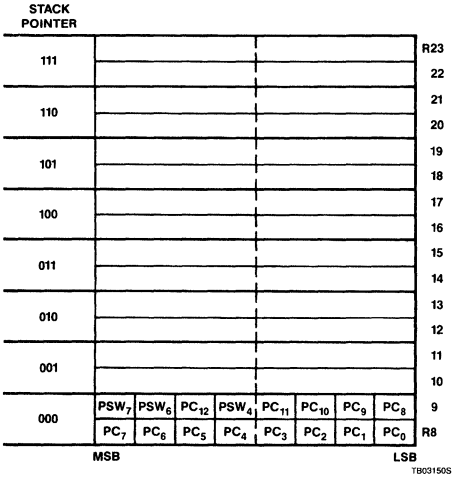


Figure 3. Program Counter Stack

IDLE and STOP Modes

IDLE Mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01'), the oscillator, timer/counter, and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled, or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Figure 4).

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out A Low-to-High transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A High level applied to CE/$\overline{TO}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was High before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Figure 5).

Wake-up from the IDLE mode is ensured when CE/$\overline{TO}$ is Low for 4CP (clock periods) followed by a High for 7CP. After the initial forced CALL H'003' operation (60CP) the program continues with the external interrupt service routine.

STOP Mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents, and the state of I/O ports are not affected. The microcontroller can be brought out of the STOP mode by an

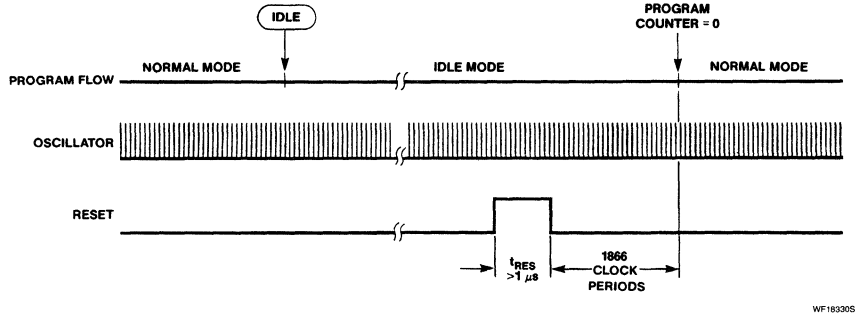


Figure 4. Exit from IDLE Mode via a RESET

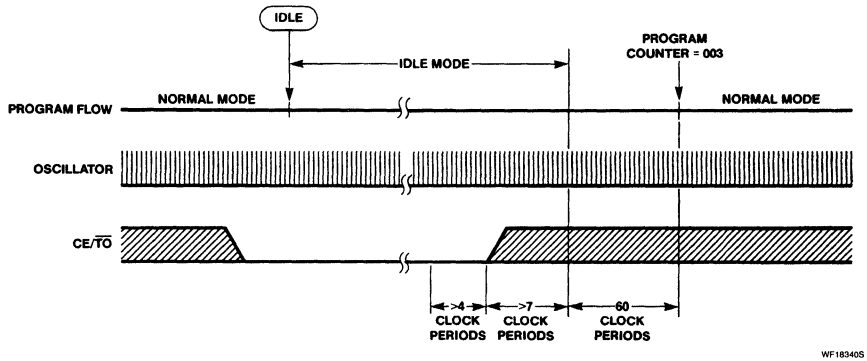


Figure 5. Exit from IDLE via an Interrupt

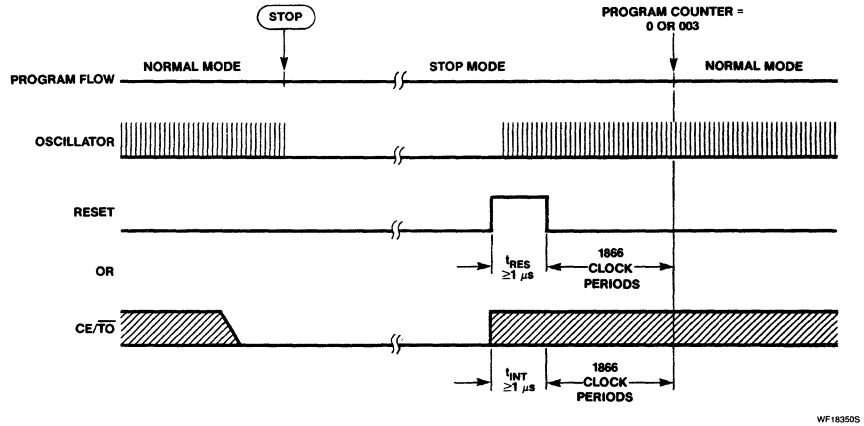


Figure 6. Entering and Exiting the STOP Mode

active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied, an internal delay of 1866CP is provided to ensure that all internal clocks are operating correctly before restart (see Figure 6).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin High, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a High level applied at the CE/$\overline{TO}$ pin, and not by a Low-to-High transition as in a normal interrupt mechanism

When the CE/$\overline{TO}$ level is active during the STOP instruction, no STOP is executed.

A High level on the external interrupt input of at least 1µs will cause the microcontroller to exit the STOP mode

I/O Facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0: Parallel port of 8 lines (P00 to P07).
- Port 1: Parallel port of 8 lines (P10 to P17).
- Port 2: Parallel port of 4 lines (P20 to P23).
- SCLK: Serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK.
- CE/$\overline{TO}$: External interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0.
- T1: Test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

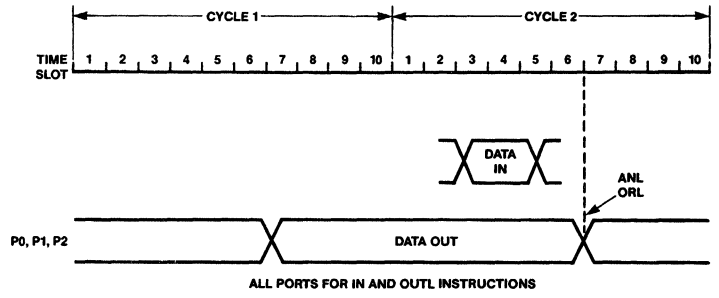


Figure 7 Timing Diagram of all Ports on IN and OUTL Instructions, for ANL and ORL Instructions, the Ports Change on the Time Slot 7 of Cycle 2

Parallel Ports

All parallel ports can be used as outputs or inputs. Their structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible. Output lines can drive one LSTTL or CMOS load. Instructions, for ANL and ORL Instructions, the Ports Change on the Time Slot 7 of Cycle 2.

Figure 8 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.

Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL High level, yet can be pulled Low by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line; otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore, the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1: STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100μA (typ.) and P-channel booster transistor TR2 (1.5mA). TR2 is only active during 1 clock cycle (0.28μs at 3.58MHz).

Option 2: OPEN-DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Figure 9).

Option 3: PUSH-PULL OUTPUT; drive capability of the output will be 1.5mA (typ.) at V_{DD} = 3V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Figure 10).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2, or 3.

Option S-SET: after RESET this pin will be initialized to High.

Option R-RESET: after RESET this pin will be initialized to Low.

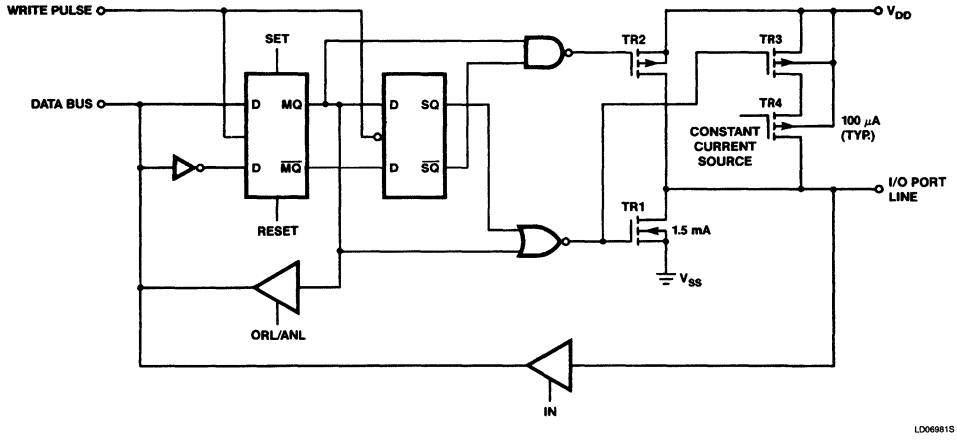


Figure 8. Standard Output with Switched Pull-up Current Source

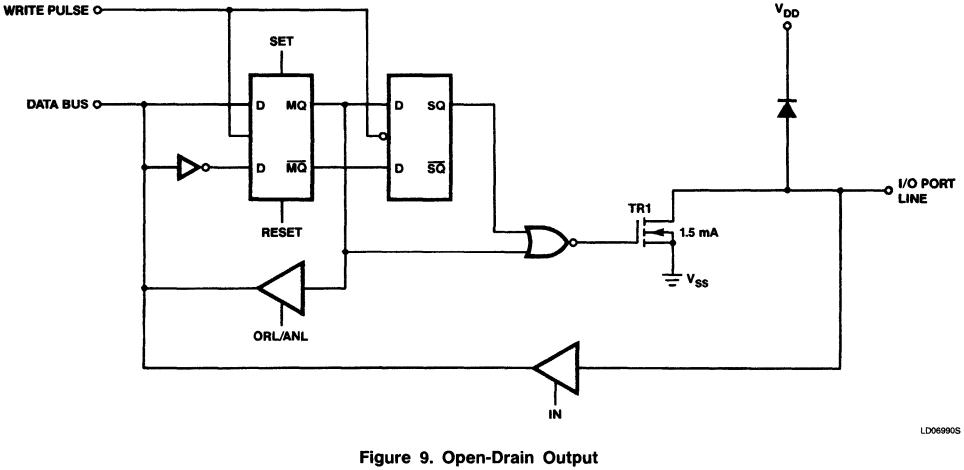


Figure 9. Open-Drain Output

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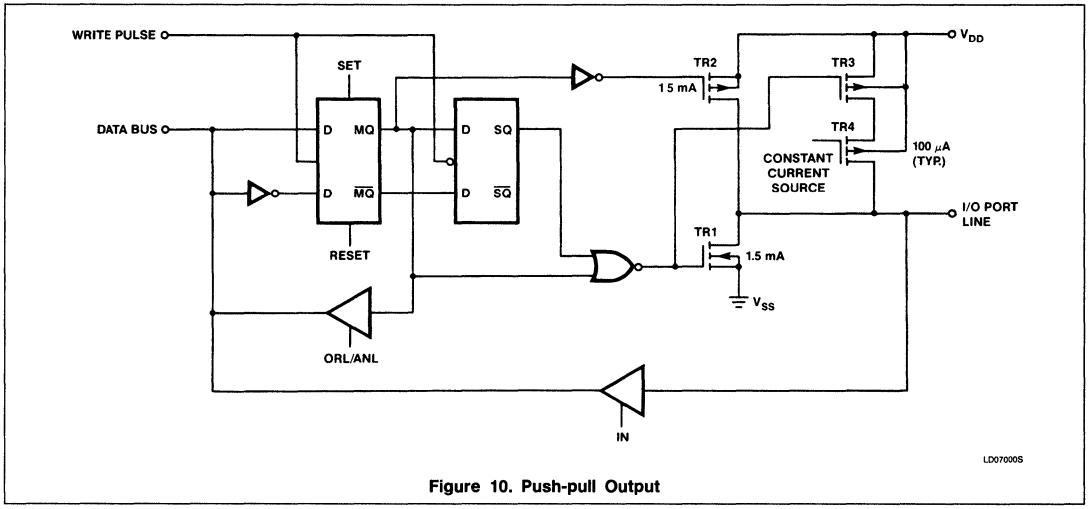

Figure 10. Push-pull Output

Serial I/O (SIO)
The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Figure 30.

In this application the SIO is used to communicate with the different peripherals, such as:
- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing, and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives, and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Similarly, during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance, in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurrence of the STOP instructions. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.

Serial I/O Interface
Figure 11 shows the serial I/O interface. The clock line of the serial bus has exclusive use of Pin 3 (SCLK) while the data line shares Pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:
- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data Shift Register (SO)
Register SO converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address, or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O Interface Status Word (S1)
Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (See Table1)
These bits determine the operating mode of the serial I/O interface.

Table 1. Operating Modes of the Serial I/O Interface

MST	TRX	OPERATING MODE
0	0	Slave receiver
1	0	Master receiver
0	1	Slave transmitter
1	1	Master transmitter

BB: Bus Busy.
This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not
PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial Output
The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1, and BC2
Bits BC0, BC1, and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost
The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave
This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero
This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0, and LRB can only be read by software.

Serial Clock Control Word (S2)
Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3.58MHz crystal is used, the frequency of the serial clock can be varied between 92kHz and 580Hz (see Table 2). An asymmetrical clock with a High-to-Low ratio of 3:1 can be generated using Bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address Register
The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, #data instructions, but only when ESO = '0'.

Serial I/O Interrupt Logic
An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 2. SIO Clock Pulse Frequency Control When Using a 3.58MHz Crystal

HEXADECIMAL S20-S24 CODE	DIVISOR	F_{SCLK} (kHz) (APPROXIMATE)
0	Not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9.2
10	483	7.4
11	579	6.2
12	675	5.3
13	771	4.6
14	963	3.7
15	1155	3.1
16	1347	2.7
17	1539	2.3
18	1923	1.9
19	2307	1.6
1A	2691	1.3
1B	3075	1.2
1C	3843	0.93
1D	4611	0.78
1E	5379	0.67
1F	6147	0.58

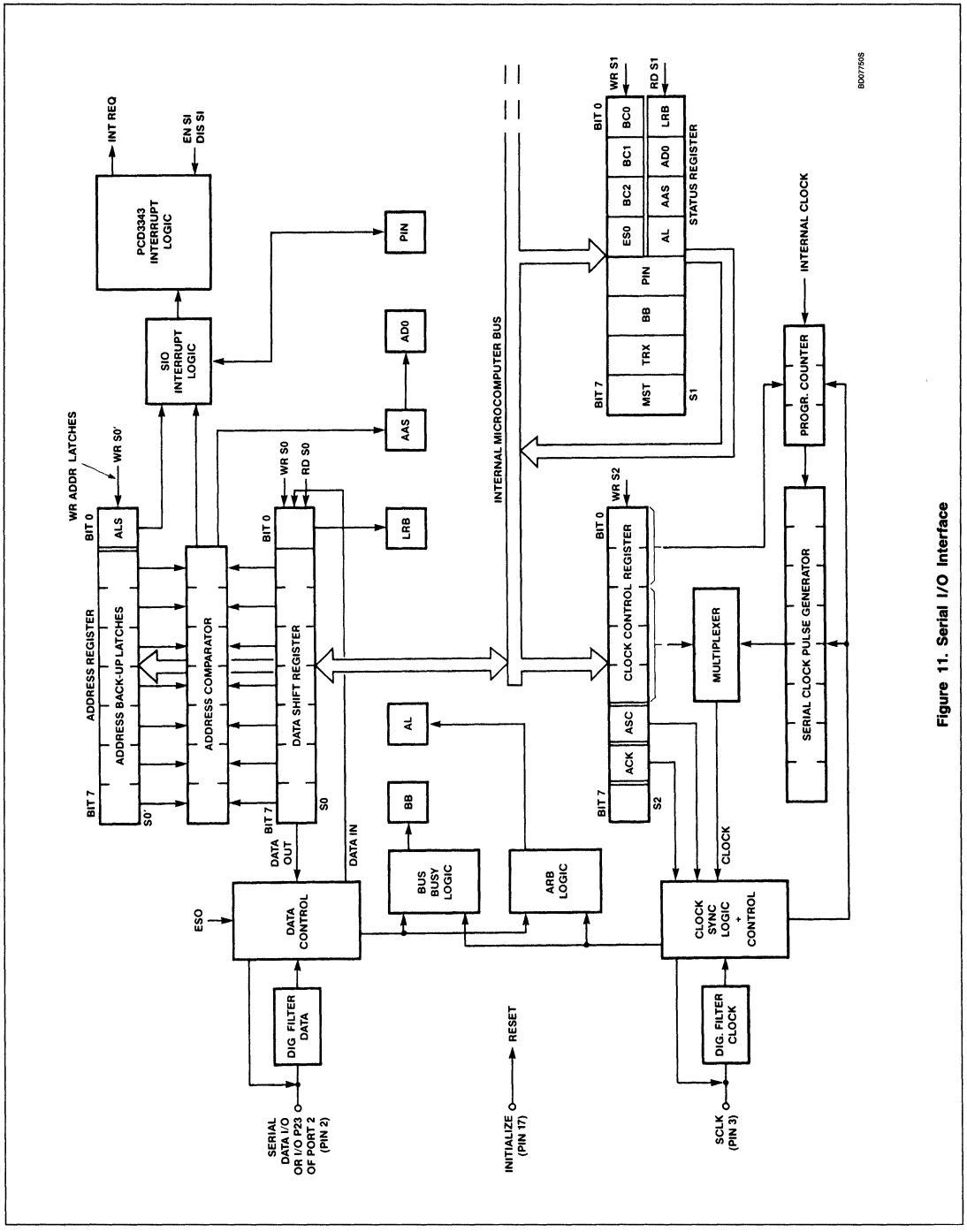

Figure 11. Serial I/O Interface

Table 3. Serial I/O Addresses for Telephony Peripherals

TYPE	ADDRESS								DESCRIPTION
	7	6	5	4	3	2	1	0	
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2k RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1k RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialer
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialer
PCF8566	0	1	1	1	1	1	0/1	0	1 4 LCD driver
PCF8582	1	0	1	0	A2	A1	A0	R/$\overline{W}$	256 × 8 EEPROM
PCF8583	1	0	1	0	0	0	A0	R/$\overline{W}$	256 × 8 RAM with clock calendar
PCF8591	1	0	0	1	A2	A1	A0	R/$\overline{W}$	A/D plus DAC
PCF8200	0	0	1	0	0	0	0	R/W	Speech synthesizer
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	Clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	0/1	0	1 4 LCD driver
PCF8577	0	1	1	1	0	1	0/1	0	1 2 LCD driver

Interrupts (see Figure 12)

When the external interrupt is enabled, a Low-to-High transition on the CE/$\overline{TO}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction The interrupt must remain enabled until the interrupt instruction is completed. Otherwise, the next instruction of the main program will be executed Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6, and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt logic After executing RETR, the program continues in the main part, this is independent of the occurrence of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

(1) external
(2) serial I/O
(3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed A Low-to-High transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (Pin 12) If required, Pin 12 must be externally connected to a resistor ($R \leq 100k\Omega$) When the external interrupt is not used, Pin 12 must be connected to V_{SS}

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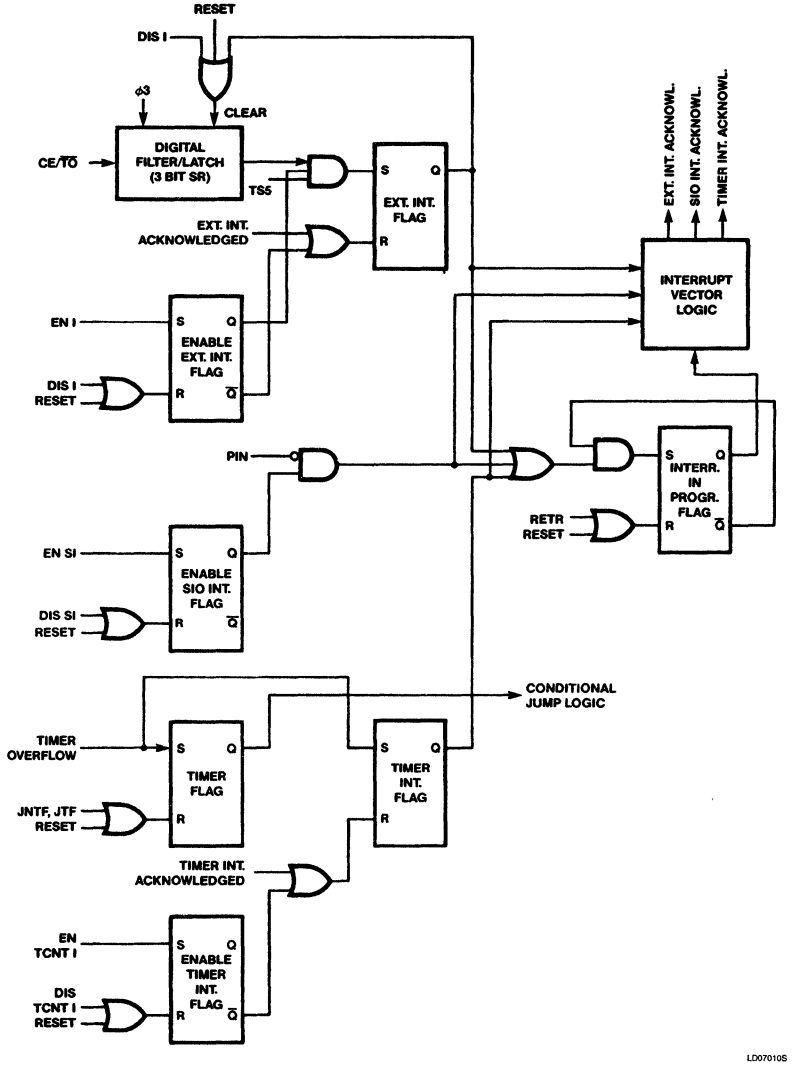


NOTES:
1. CE/$\overline{TO}$ positive edge is always latched in the digital filter/latch
2. Correct interrupt timing is ensured when CE/$\overline{TO}$ is Low for > 4CP followed by High for > 7CP
3. When the interrupt-in-progress flag is set, further interrupts are latched but ignored, until RETR is executed
4. A DIS I instruction always clears a pending external interrupt

Figure 12. Interrupt Logic

Oscillator (see Figure 13)

The 3.58MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a High level at either the CE/$\overline{TO}$ or RESET pin.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via Pin 16 (XTAL 2). An external clock can be applied to Pin 15 (XTAL 1). A machine cycle consists of ten time slots, each time slot being three oscillator periods.

In telephony applications the 3.58MHz crystal provides an 8.4μs machine cycle. The range of the clock frequency is from 100kHz up to a maximum which is a function of the supply voltage (see Figure 20).

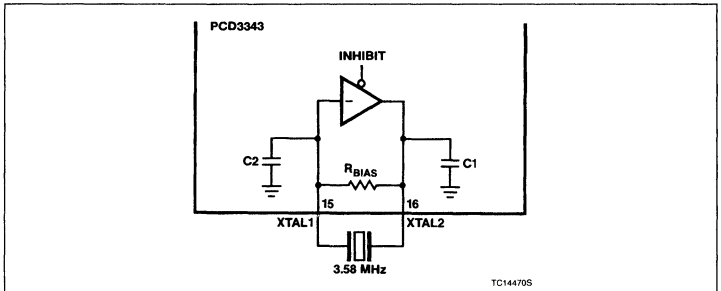


Figure 13. Oscillator with Integrated Elements

Timer/Event Counter (see Figure 14)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, Low-to-High transitions on Pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182.6kHz for an 8.4μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

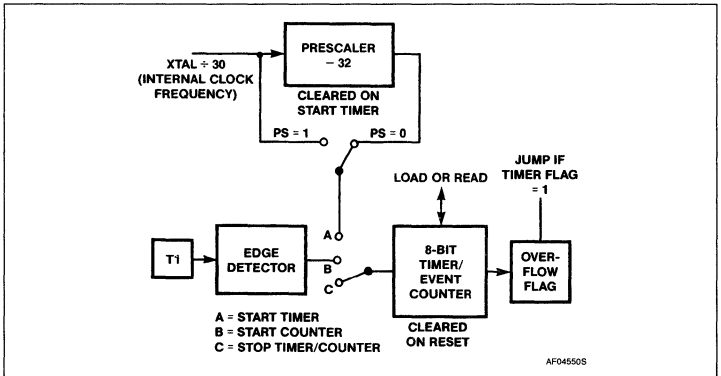


Figure 14. Timer/Event Counter

Table 4. Timer/Event Counter Control

FUNCTION	TIMER MODE MODULO-1, MODULO-32[1]	COUNTER MODE
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ[2]	MOV A,T	MOV A,T

NOTES:
1 With prescaler select, PS = 0, the timer counts modulo-32 machine cycles; with PS = 1, it counts modulo-1 cycles (prescaler not used), prescaler cleared with STRT T, prescaler not readable
2 READ does not disturb the counting process

Program Status Word (see Figure 15)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.

The PSW bits are:

- Bits 0 to 2 Stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 Prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 Working register bank select (RBS); 0 = register bank 1 = register bank 0
- Bit 5 Not used (1)
- Bit 6 Auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 Carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

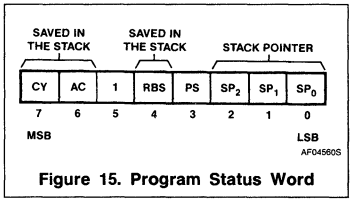


Figure 15. Program Status Word

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, Bit 3 by the MOV PSW, A instruction, and Bits 0, 1, and 2 by the CALL, RET, or RETR instructions, and in the event of an interrupt. Bits 7, 6, and 4 are stored in

6

the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program Counter (see Figure 16)

A 13-bit program counter is used to facilitate 8k bytes of ROM being addressed. The arrangement of the bits is shown in Figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

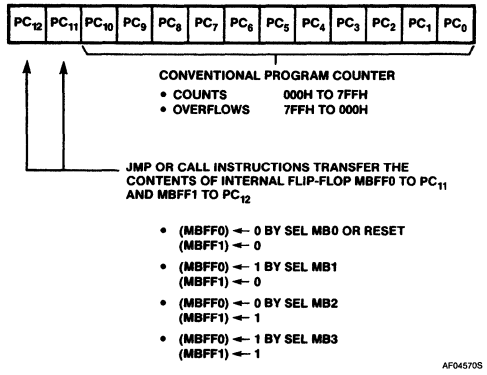


Figure 16. Program Counter

Central Processing Unit

The PCD3343 has arithmetic, logical, and branching capabilities. The DA A, SWAP A, and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional Branch Logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5. Conditional Branches

TEST	JUMP CONDITION	JUMP INSTRUCTION
Accumulator	All bits zero	JZ
	Any bit non-zero	JNZ
Accumulator bit test	1	JB0 to JB7
Carry flag	1	JC
	0	JNC
Timer overflow flag	1	JTF
	0	JNTF
Test input T0	1	JNT0
	0	JT0[1]
Test input T1	1	JT1
	0	JNT1
Register	Non-zero	DJNZ

NOTE:
1. Because of the inverted interrupt input CE/$\overline{T0}$, the conditional jump JT0 is also inverted

Test Input T1 (Pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- **JT1** instruction tests for logic 1 level
- **JNT1** instruction tests for logic 0 level

When used as an input to the event counter, T1 must be Low for > 4CP, followed by a High for > 4CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required, it must be externally connected to a resistor ($R = \leqslant 100k\Omega$). When T1 is not used, Pin 13 must be connected to V_{DD} or V_{SS}.

Reset (Pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer, and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

After the voltage is applied to RESET, an internal delay of 1866CP is introduced before the microcontroller commences operation.

Power-On Reset and Low Voltage Detection (see Figure 17)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by

the addition of an internal power-on reset and low voltage detection circuit.

To allow an external RESET signal being fed into the PCD3343, the reset pin (Pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, Pin 17 is pulled High by TR1 controlled by the reset circuit.

When the reset condition is not present, a pull-down current source (TR2) will be activated. TR2 forces Pin 17 Low, thus removing the RESET signal from the microcontroller.

Since the level at Pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and Pin 17 (see Figure 19).

The signal at Pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1.3V), a reset (High) is applied to Pin 17. This reset is removed (Pin 17 goes Low), after a fixed delay (t_D), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low voltage condition, the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low voltage detection circuit is shown in Figure 18.

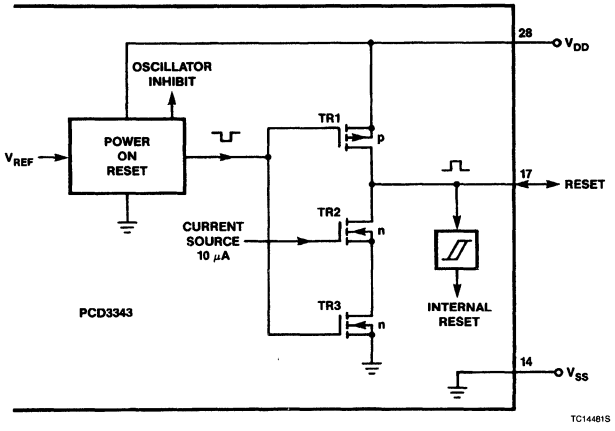
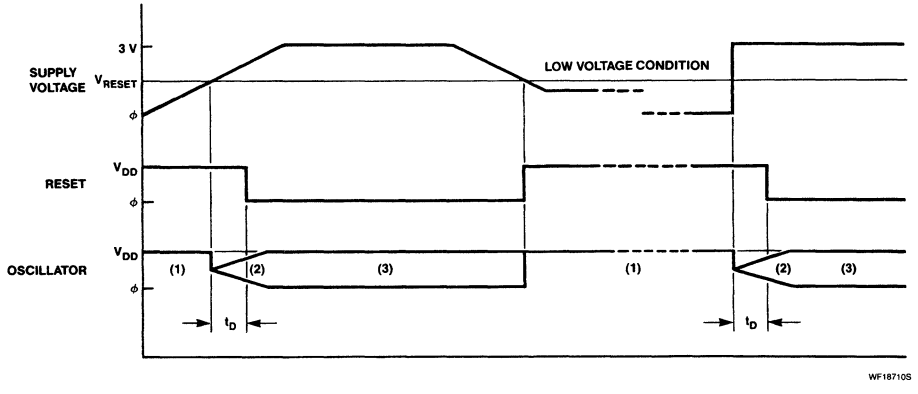


Figure 17. Power-On Reset Configuration



Where:
(1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Figure 18. Timing of Power-On Reset and Low Voltage Detection

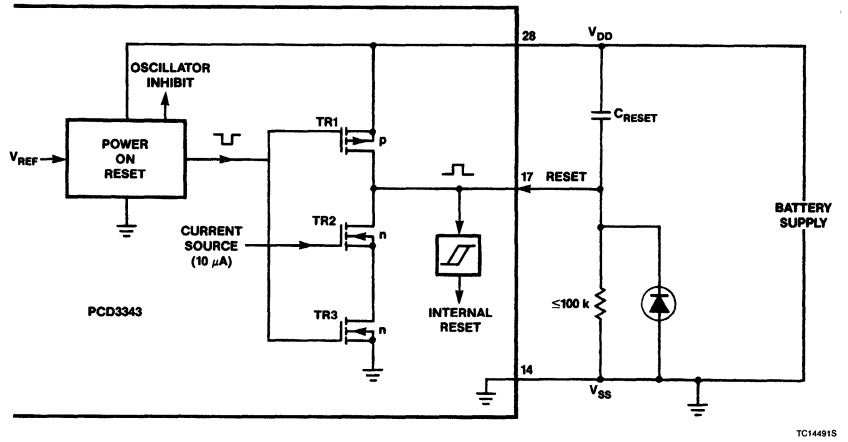


Figure 19. Stretched Power-On Reset with External Capacitor

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one- and two-byte instructions, and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343, Table 7 shows the instruction map, and Table 6 details the symbols and definition descriptions that are used.

Table 6. Symbols and Definitions Used in Table 8

SYMBOL	DEFINITION DESCRIPTION
A	Accumulator
Addr	Program memory address
Bb	Bit designation (b = 0 – 7)
RBS	Register bank select
C	Carry bit (bit CY)
CNT	Event counter
D	Mnemonic for 4-bit digit (nibble)
Data	8-bit number or expression
I	Interrupt
MB	Memory bank
MBFF	Memory bank flip-flop
P	Mnemonic for 'in-page' operation
PC	Program counter
Pp	Port designation (p = 0, 1, or 2)
PSW	Program status word
RB	Register bank
Rr	Register designation (r = 0 – 7)
Sn	Serial I/O register
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Test 0 and 1 inputs
#	Immediate data prefix
@	Indirect address prefix
(X)	Contents of X
((X))	Contents of location addressed by X
←	Is replaced by
↔	Is exchanged with

Table 7. PCD3343 Instruction Map

first hexadecimal character of opcode ↓ / SECOND HEXADECIMAL CHARACTER OF OPCODE →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	IN A, Pp 0	1	2		MOV A, Sn 0	1		
1	INC @Rr 0	1	JB0 addr	ADDC A, #data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A, @Rr 0	1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A, Rr 0	1	2	3	4	5	6	7
3	XCHD A, @Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp, A 0	1	2		MOV Sn, A 0	1	2	
4	ORL A, @Rr 0	1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A, Rr 0	1	2	3	4	5	6	7
5	ANL A, @Rr 0	1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A, Rr 0	1	2	3	4	5	6	7
6	ADD A, @Rr 0	1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A, Rr 0	1	2	3	4	5	6	7
7	ADDC A, @Rr 0	1	JB3 addr		CALL page 3			RR A	ADDC A, Rr 0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp, #data 0	1	2					
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp, #data 0	1	2		MOV Sn, #data 0	1	2	
A	MOV @Rr, A 0	1		MOVP A, @A	JMP page 5	SEL MB2		CPL C	MOV Rr, A 0	1	2	3	4	5	6	7
B	MOV @Rr, #data 0	1	JB5 addr	JMPP A, @A	CALL page 5	SEL MB3			MOV Rr, #data 0	1	2	3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A, @Rr 0	1	JB6 addr	XRL A, #data	CALL page 6	SEL RB1		MOV PSW, A	XRL A, Rr 0	1	2	3	4	5	6	7
E	DJNZ @Rr, addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0	1	2	3	4	5	6	7
F	MOV A, @Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A, Rr 0	1	2	3	4	5	6	7

Table 8. Instruction Set

MNEMONIC	OPCODE (HEX.)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
ACCUMULATOR						
ADD A, Rr	6*	1/1	Add register contents to A	(A) ← (A) + (Rr)	r = 0 – 7	1
ADD A, @Rr	60	1/1	Add RAM data, addressed by Rr, to A	(A) ← (A) + ((R0))		1
	61			(A) ← (A) + ((R1))		
ADD A, #data	03 data	2/2	Add immediate data to A	(A) ← (A) + data		1
ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A) ← (A) + (Rr) + (C)	r = 0 – 7	1
ADDC A, @Rr	70	1/1	Add carry and RAM data, addressed	(A) ← (A) + ((R0)) + (C)		1
	71		by Rr, to A	(A) ← (A) + ((R1)) + (C)		
ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A) ← (A) + data + (C)		1
ANL A, Rr	5*	1/1	'AND' Rr with A	(A) ← (A) AND (Rr)	r = 0 – 7	
ANL A, @Rr	50	1/1	'AND' RAM data, addressed by Rr, with A	(A) ← (A) AND ((R0))		
	51			(A) ← (A) AND ((R1))		
ANL A, #data	53 data	2/2	'AND' immediate data with A	(A) ← (A) AND data		
ORL A, Rr	4*	1/1	'OR' Rr with A	(A) ← (A) OR (Rr)	r = 0 – 7	
ORL A, @Rr	40	1/1	'OR' RAM data, addressed by Rr, with A	(A) ← (A) OR ((R0))		
	41			(A) ← (A) OR ((R1))		
ORL A, #data	43 data	2/2	'OR' immediate data with A	(A) ← (A) OR data		
XRL A, Rr	D*	1/1	'XOR' Rr with A	(A) ← (A) XOR (Rr)	r = 0 – 7	
XRL A, @Rr	D0	1/1	'XOR' RAM, addressed by Rr, with A	(A) ← (A) XOR ((R0))		
	D1			(A) ← (A) XOR ((R1))		
XR LA, #data	D3 data	2/2	'XOR' immediate data with A	(A) ← (A) XOR data		
INC A	17	1/1	Increment A by 1	(A) ← (A) + 1		
DEC A	07	1/1	Decrement A by 1	(A) ← (A) – 1		
CLR A	27	1/1	Clear A to zero	(A) ← 0		
CPL A	37	1/1	One's complement A	(A) ← NOT(A)		
RL A	E7	1/1	Rotate A left	$(A_{n+1}) \leftarrow (A_n)$	n = 0 – 6	
				$(A_0) \leftarrow (A_7)$		
RLC A	F7	1/1	Rotate A left through carry	$(A_{n+1}) \leftarrow A_n$	n = 0 – 6	2
				$(A_0) \leftarrow (C), (C) \leftarrow (A_7)$		
RR A	77	1/1	Rotate A right	$(A_n) \leftarrow (A_{n+1})$	n = 0 – 6	
				$(A_7) \leftarrow (A_0)$		
RRC A	67	1/1	Rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$	n = 0 – 6	2
				$(A_7) \leftarrow (C), (C) \leftarrow (A_0)$		
DA A	57	1/1	Decimal adjust A			2
SWAP A	47	1/1	Swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES						
MOV A, Rr	F*	1/1	Move register contents to A	(A) ← (Rr)	r = 0 – 7	
MOV A, @Rr	F0	1/1	Move RAM data, addressed by Rr, to A	(A) ← ((R0))		
	F1			(A) ← ((R1))		
MOV A, #data	23 data	2/2	Move immediate data to A	(A) ← data		
MOV Rr, A	A*	1/1	Move accumulator contents to register	(Rr) ← (A)	r = 0 – 7	
MOV @Rr, A	A0	1/1	Move accumulator contents to RAM	((R0)) ← (A)		
	A1		Location addressed by Rr	((R1)) ← (A)		
MOV Rr, #data	B* data	2/2	Move immediate data to Rr	(Rr) ← data		
MOV @Rr, #data	B0 data	2/2	Move immediate data to RAM location	((R0)) ← data		
	B1 data		addressed by Rr	((R1)) ← data		
XCH A, Rr	2*	1/1	Exchange accumulator contents with Rr	(A) ↔ (Rr)	r = 0 – 7	
XCH A, @Rr	20	1/1	Exchange accumulator contents with	(A) ↔ ((R0))		
	21		RAM data addressed by Rr	(A) ↔ ((R1))		
XCHD A, @Rr	30	1/1	Exchange lower nibbles of A and RAM	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$		
	31		data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R1_{0-3})$		
MOV A, PSW	C7	1/1	Move PSW contents to accumulator	(A) ← (PSW)		
MOV PSW, A	D7	1/1	Move accumulator Bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
MOVP A, @A	A3	1/2	Move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) = \leftarrow ((PC))$		

Table 8. Instruction Set (Continued)

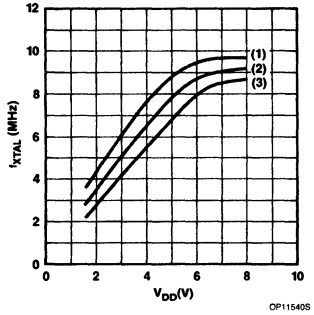
MNEMONIC	OPCODE (HEX.)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
FLAGS					
CLR C	97	1/1	Clear carry bit	(C) ← 0	2
CPL C	A7	1/1	Complement carry bit	(C) ← NOT(C)	2
REGISTER					
INC Rr	1*	1/1	Increment register by 1	(Rr) ← (Rr) + 1 r = 0 – 7	
INC @Rr	10	1/1	Increment RAM data, addressed by Rr, by 1	((R0)) ← ((R0)) + 1	
	11			((R1)) ← ((R1)) + 1	
DEC Rr	C*	1/1	Decrement register by 1	(Rr) ← (Rr) – 1 r = 0 – 7	
DEC @Rr	C0	1/1	Decrement RAM data, addressed by Rr, by 1	((R0)) ← ((R0)) – 1	
	C1			((R1)) ← ((R1)) – 1	
BRANCH					
JMP addr	• 4 address	2/2	Unconditional jump within a 2k bank	(PC_{8-10}) ← $addr_{8-10}$ (PC_{0-7}) ← $addr_{0-7}$ (PC_{11-12}) ← MBFF 0 – 1	
JMPP @A	B3	1/2	Indirect jump within a page	(PC_{0-7}) ← ((A))	
DJNZ Rr, addr	E* address	2/2	Decrement Rr by 1 and jump if not zero to addr	(Rr) ← (Rr) – 1 r = 0 – 7 if (Rr) not zero (PC_{0-7}) ← addr	
DJNZ @Rr, addr	E0	2/2	Decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0)) ← ((R0)) – 1 if ((R0)) not zero (PC_{0-7}) ← addr	
	E1			((R1)) ← ((R1)) – 1 if ((R1)) not zero (PC_{0-7}) ← addr	
JBb addr	▲ 2 address	2/2	Jump to addr if Acc. bit b = 1	If b = 1 : (PC_{0-7}) ← addr b = 0 – 7	
JC addr	F6 address	2/2	Jump to addr if C = 1	If C = 1 : (PC_{0-7}) ← addr	
JNC addr	E6 address	2/2	Jump to addr if C = 0	If C = 0 : (PC_{0-7}) ← addr	
JZ addr	C6 address	2/2	Jump to addr if A = 0	If A = 0 : (PC_{0-7}) ← addr	
JNZ addr	96 address	2/2	Jump to addr if A is NOT zero	If A ≠ 0 : (PC_{0-7}) ← addr	
JT0 addr	36 address	2/2	Jump to addr if T0 = 0	If T0 = 0: (PC_{0-7}) ← addr	
JNT0 addr	26 address	2/2	Jump to addr if T0 = 1	If T0 = 1: (PC_{0-7}) ← addr	
JT1 addr	56 address	2/2	Jump to addr if T1 = 1	If T1 = 1: (PC_{0-7}) ← addr	
JNT1 addr	46 address	2/2	Jump to addr if T1 = 0	If T1 = 0: (PC_{0-7}) ← addr	
JTF addr	16 address	2/2	Jump to addr if Timer Flag = 1	If TF = 1: (PC_{0-7}) ← addr	4
JNTF addr	06 address	2/2	Jump to addr if Timer Flag = 0	If TF = 0: (PC_{0-7}) ← addr	
TIMER/EVENT COUNTER					
MOV A, T	42	1/1	Move timer/event counter contents to accumulator	(A) ← (T)	
MOV T, A	62	1/1	Move accumulator contents to timer/event counter	(T) ← (A)	
STRT CNT	45	1/1	Start event counter		
STRT T	55	1/1	Start timer		
STOP TCNT	65	1/1	Stop timer/event counter		
EN TCNTI	25	1/1	Enable timer/event counter interrupt		
DIS TCNTI	35	1/1	Disable timer/event counter interrupt		
CONTROL					
EN I	05	1/1	Enable external interrupt		
DIS I	15	1/1	Disable external interrupt		
SEL RB0	C5	1/1	Select register bank 0	(RBS) ← 0	5
SEL RB1	D5	1/1	Select register bank 1	(RBS) ← 1	5
SEL MB0	E5	1/1	Select program memory bank 0	(MBFF0) ← 0, (MBFF1) ← 0	
SEL MB1	F5	1/1	Select program memory bank 1	(MBFF0) ← 1, (MBFF1) ← 0	
SEL MB2	A5	1/1	Select program memory bank 2	(MBFF0) ← 0, (MBFF1) ← 1	
SEL MB3	B5	1/1	Select program memory bank 3	(MBFF0) ← 1, (MBFF1) ← 1	
STOP	22	1/1	Enter STOP mode		
IDLE	01	1/1	Enter IDLE mode		

Table 8. Instruction Set (Continued)

MNEMONIC	OPCODE (HEX.)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
SUBROUTINE					
CALL addr	▲ 4 address	2/2	Jump to subroutine	$((SP)) \leftarrow (PC)$, $(PSW_{4,6,7})$ 6 $(SP) \leftarrow (SP) + 1$ $(PC_{8-10}) \leftarrow addr_{8-10}$ $(PC_{0-7}) \leftarrow addr_{0-7}$ $(PC_{11-12}) \leftarrow$ MBFF 0 – 1	6
RET	83	1/2	Return from subroutine	$(SP) \leftarrow (SP) - 1$ $(PC) \leftarrow ((SP))$	6
RETR	93	1/2	Return from interrupt and restore bits 4, 6, 7 of PSW	$(SP) \leftarrow (SP) - 1$ $(PSW_{4,6,7}) + (PC) \leftarrow ((SP))$	6
PARALLEL INPUT/OUTPUT					
IN A, Pp	08	1/2	Input port p data to accumulator	$(A) \leftarrow (P0)$	
	09			$(A) \leftarrow (P1)$	
	0A			$(A) \leftarrow (P2)$	7
OUTL Pp, A	38	1/2	Output accumulator data to port p	$(P0) \leftarrow (A)$	
	39			$(P1) \leftarrow (A)$	
	3A			$(P2) \leftarrow (A)$	
ANL Pp, #data	98	2/2	AND port p data with immediate data	$(P0) \leftarrow (P0)$ AND data	
	99			$(P1) \leftarrow (P1)$ AND data	
	9A			$(P2) \leftarrow (P2)$ AND data	
ORL Pp, #data	88	2/2	OR port p data with immediate data	$(P0) \leftarrow (P0)$ OR data	
	89			$(P1) \leftarrow (P1)$ OR data	
	8A			$(P2) \leftarrow (P2)$ OR data	
SERIAL INPUT/OUTPUT					
MOV A, S_n	0C	1/2	Move serial I/O register contents to	$(A) \leftarrow (S0)$	
	0D		accumulator	$(A) \leftarrow (S1)$	8
MOV S_n, A	3C	1/2	Move accumulator contents to serial	$(S0) \leftarrow (A)$	
	3D		I/O register	$(S1) \leftarrow (A)$	
	3E			$(S2) \leftarrow (A)$	9
MOV S_n, #data	9C	2/2	Move immediate data to serial	$(S0) \leftarrow$ data	
	9D		I/O register	$(S1) \leftarrow$ data	
	9E			$(S2) \leftarrow$ data	
EN SI	85	1/1	Enable serial I/O interrupt		
DIS SI	95	1/1	Disable serial I/O interrupt		
NOP	00	1/1	No operation		

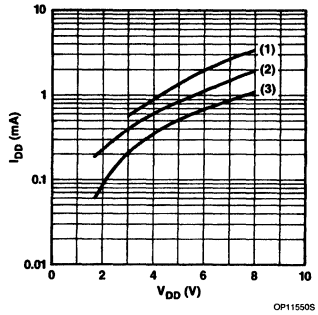
NOTES:
1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF)
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20
8. (S1) has a different meaning for read and write operation, see serial I/O interface
9. (S2) is a write only register Reading S2 will give value FFH.

* . 8, 9, A, B, C, D, E, F
• · 0, 2, 4, 6, 8, A, C, E
▲ 1, 3, 5, 7, 9, B, D, F



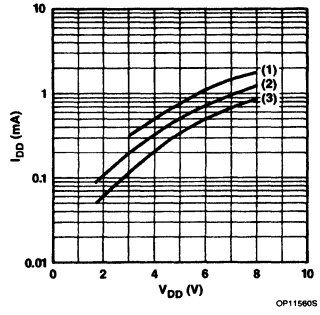
NOTES:
1 $T_A = -25°C$
2 $T_A = 25°C$
3 $T_A = 70°C$

Figure 20. Maximum Clock Frequency (f_{XTAL}) as a Function of the Supply Voltage (V_{DD})



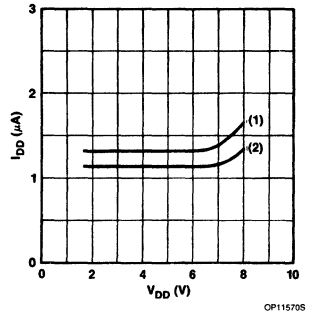
NOTES:
1 Clock frequency = 4MHz
2. Clock frequency = 2MHz
3. Clock frequency = 500kHz
4 $T_A = 25°C$

Figure 21. Typical Supply Current (I_{DD}) in Operating Mode as a Function of the Supply Voltage (V_{DD})



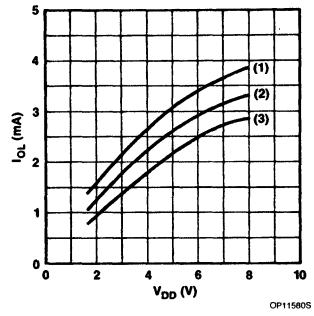
NOTES:
1 Clock frequency = 4MHz
2 Clock frequency = 2MHz
3 Clock frequency = 500kHz
4 $T_A = 25°C$

Figure 22. Typical Supply Current (I_{DD}) in IDLE Mode as a Function of the Supply Voltage (V_{DD})



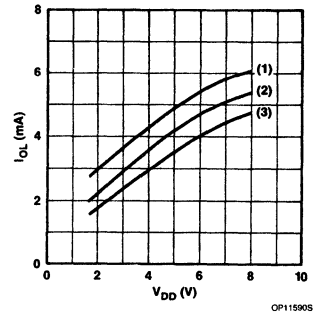
NOTES:
1 $T_A = 70°C$
2 $T_A = 25°C$

Figure 23. Typical Supply Current (I_{DD}) in STOP Mode as a Function of the Supply Voltage (V_{DD})



NOTES:
1 $T_A = -25°C$
2 $T_A = 25°C$
3 $T_A = 70°C$
4 $V_O = 0.4V$

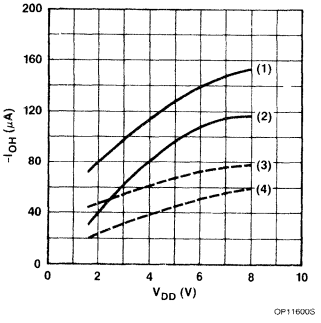
Figure 24. Output Sink Current Low (I_{OL}), Except Outputs P23/SDA and SCLK, as a Function of Supply Voltage (V_{DD})



NOTES:
1 $T_A = -25°C$
2 $T_A = 25°C$
3 $T_A = 70°C$
4 $V_O = 0.4V$

Figure 25. Output Current LOW(I_{OL}), Outputs P23/SDA and SCLK, as a Function of Supply Voltage (V_{DD}

6



NOTES:
1 $T_A = 25°C$, $V_O = V_{SS}$
2 $T_A = 25°C$, $V_O = 0.9V_{DD}$
3 $T_A = 70°C$, $V_O = V_{SS}$
4 $T_A = 70°C$, $V_O = 0.9V_{DD}$

Figure 26. Output Source Current HIGH ($-I_{OH}$) as a Function of Supply Voltage (V_{DD})

Table 9. Input Timing Shown in Figure 27

SYMBOL	TIMING
t_{BUF}	$\geqslant 14t_{XTAL}$
t_{HD}, t_{STA}	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
t_{SY}, t_{STO}	$\geqslant 14t_{XTAL}$
t_{HD}, t_{DAT}	> 0
t_{SU}, t_{DAT}	$\geqslant 250ns$
t_{RD}	$\leqslant 1\mu s$
t_{RC}	$\leqslant 1\mu s$
t_{FD}	$\leqslant 1\mu s$
t_{FC}	$\leqslant 0.3\mu s$

NOTES.
t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280ns for f_{XTAL} = 3.58MHz
These figures apply to all modes

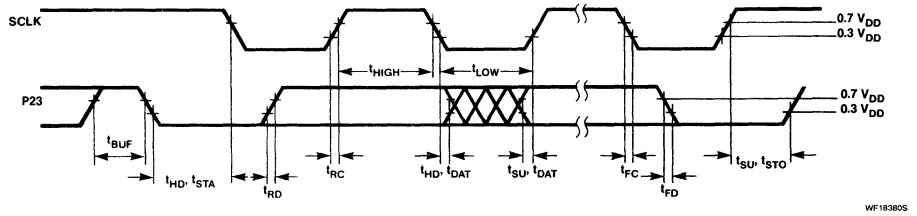


Figure 27. PCD3343 Timing Requirements for the P23 and SCLK Input Signals

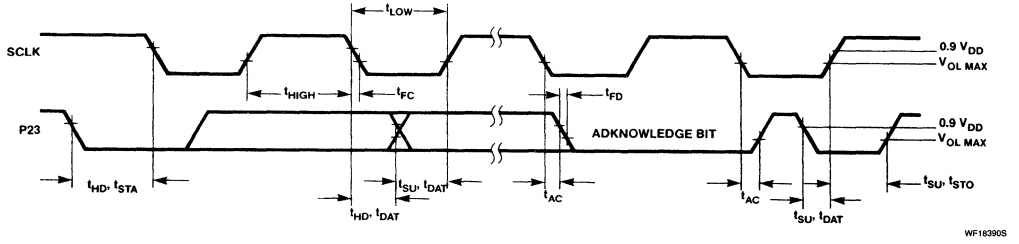


Figure 28. PCD3343 Timing Requirements for the P23 and SCLK Output Signals

Table 10. Output Timing Shown in Figure 28

SYMBOL	TIMING	
	NORMAL MODE (ASC in S2 = 0)	LOW-SPEED MODE (ASC IN S2 = 1)
t_{HD}, t_{STA}	$\frac{1}{2}$ (DF + 9) t_{XTAL}	$\frac{3}{4}$ (DF + 9) t_{XTAL}
t_{HIGH}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{3}{4}$ (DF) t_{XTAL}
t_{LOW}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{1}{4}$ (DF) t_{XTAL}
t_{SU}, t_{STO}	$\frac{1}{2}$ (DF – 3) t_{XTAL}	$\frac{1}{4}$ (DF – 3) t_{XTAL}
t_{HD}, t_{DAT} (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{HD}, t_{DAT} (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	
for DF $\leqslant$ 99		$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{SU}, t_{DAT} (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	
for DF > 99		$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
for DF $\leqslant$ 99		$\geqslant 9t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100ns at C_b = 400pF	$\leqslant$ 100ns at C_b = 400pF

NOTES:

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280ns for f_{XTAL} = 3.58MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

6

APPLICATION INFORMATION

A block diagram of an electric Feature phone built around the PCD3343 is shown in Figure 29. It comprises the following dedicated telephony ICs:

- TEA1060/1061 Transmission circuit for telephony
- PCD3312 DTMF generator with Serial I/O
- PCF8577 LCD driver
- PCD8571 1k RAMs with Serial I/O; the number of RAMs depends on the required amount of stored telephone numbers
- PCD3360 Programmable multi-tone ringer

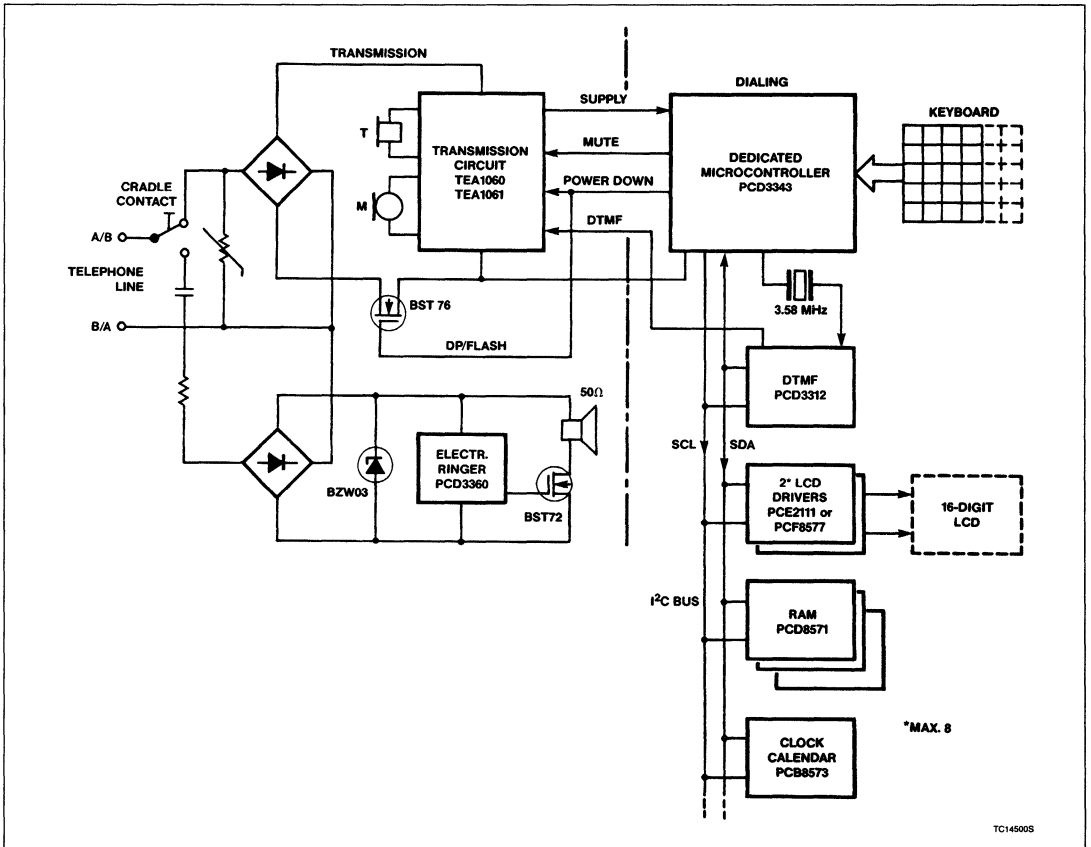


Figure 29. Block Diagram of Electronic Featurephone with Common Line Interface

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM), and two PCE2111 (LCD display drivers) is shown in Figure 30.

Row 5 of the keyboard contains the following special keys.

- **P** Program and autodial
- **FL** Flash or register recall
- **R** Redial or extended redial
- **AP** Access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

Additional Information is available on request for the following:

- Serial I/O
- I^2C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

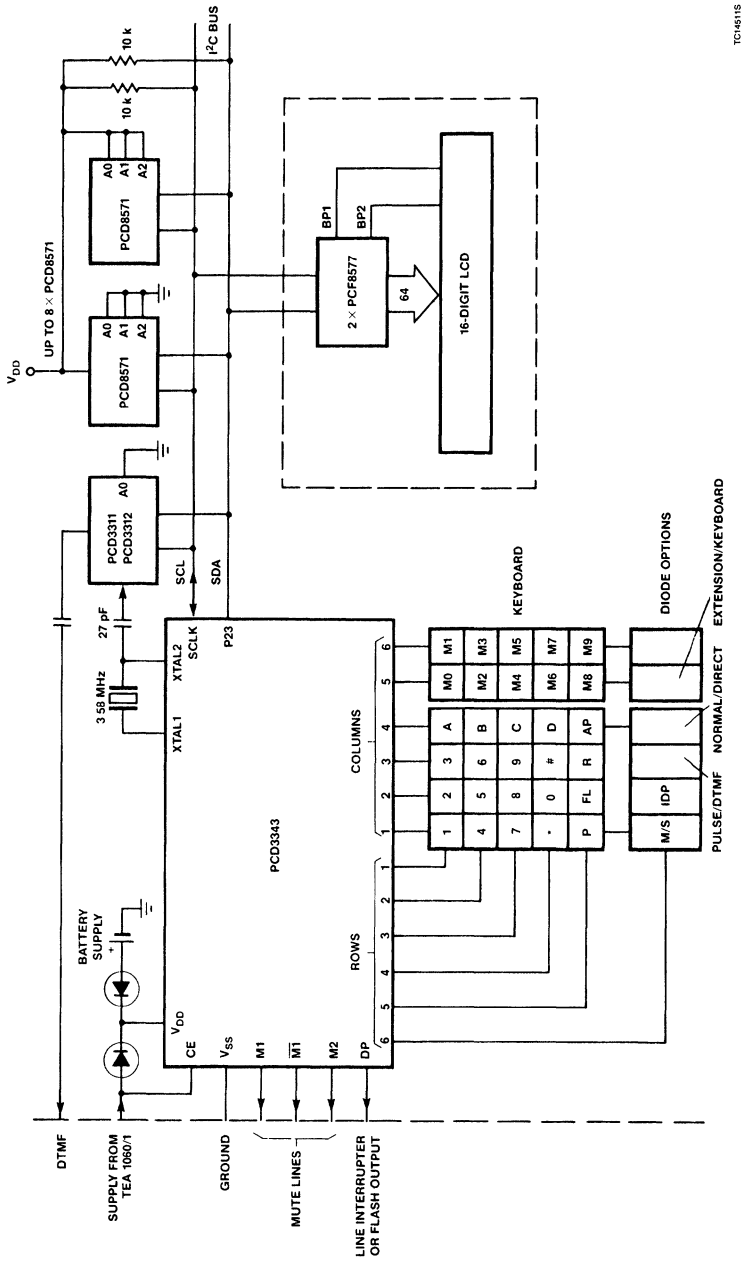


Figure 30. Application Diagram of PCD3343 for Electronic Featurephone with Associated Keyboard

6

Signetics

PCD3360
Programmable Multi-Tone Telephone Ringer

Product Specification

Linear Products

DESCRIPTION

The PCD3360 are CMOS integrated circuits, designed to replace the electromechanical bell in telephone sets. They meet most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezoelectric (PXE) transducer are provided. In the former application, no audio transformer is required since the loudspeaker is driven in class D.

NOTE:
Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

FEATURES

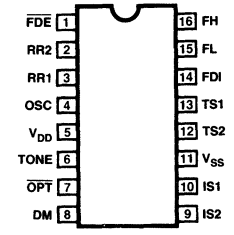
- **Output signals for electrodynamic transducer (loudspeaker) or for piezoelectric transducer (PXE)**
- **7 basic frequencies (tones) and a pause**
- **4 selectable tone sequences**
- **4 selectable repetition rates**
- **3 selectable impedance settings**
- **3-step automatic swell (loudspeaker only)**
- **Delta-modulated output signal that approximates a sinewave (loudspeaker only)**
- **Input frequency discriminator with selectable upper and lower frequency limits**
- **Output for optical signal**

APPLICATION

- **Telephone hand sets**

PIN CONFIGURATION

D, N Packages



TOP VIEW

CD12710S

PIN NO.	SYMBOL	DESCRIPTION
1	$\overline{PDE}$	Frequency discriminator enable
2	RR2	Repetition rate selection
3	RR1	
4	OSC	Oscillator
5	V_{DD}	Positive supply
6	TONE	Tone output
7	$\overline{OPT}$	Optical signal output
8	DM	Drive mode selection
9	IS2	Impedance setting and automatic swell
10	IS1	
11	V_{SS}	Negative supply
12	TS2	Tone sequence selection
13	TS1	
14	FDI	Frequency discriminator input
15	FL	Lower frequency limit selection
16	FH	Upper frequency limit selection

ORDERING INFORMATION

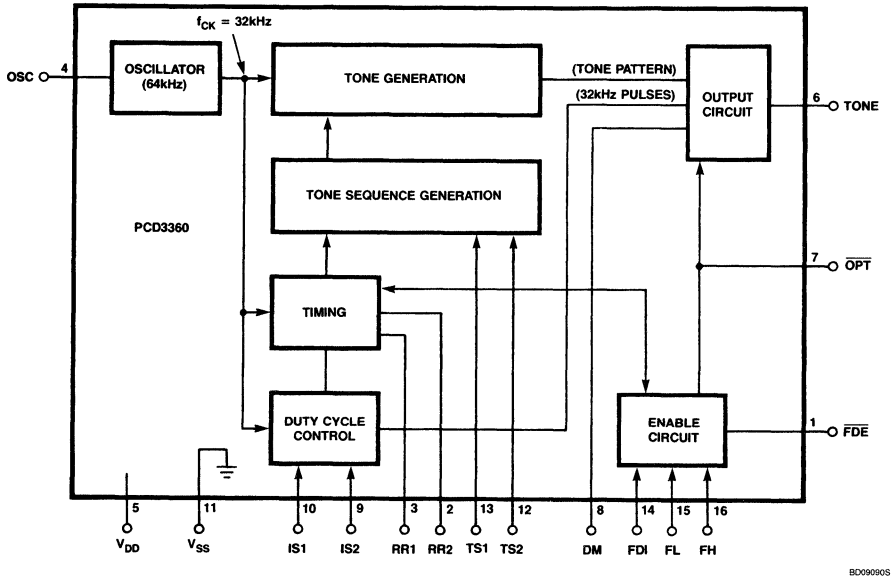
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−25°C to +75°C	PCD3360PN
16-Pin Plastic SO (SO-16L; SOT-162A)	−25°C to +75°C	PCD3360TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.8 to +9	V
I_{DD}	Supply current	50	mA
$\pm I_I$, $\pm I_O$	DC current into any input or output	10	mA
V_I	All input voltages	−0.8V to V_{DD} +0.8	V
P_{TOT}	Total power dissipation	300	mW
P_O	Total dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

Programmable Multi-Tone Telephone Ringer PCD3360

BLOCK DIAGRAM



6

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 6V; V_{SS} = 0; f_{OSC} = 64kHz; T_A = −25°C to +70°C; valid enable conditions at FDI and $\overline{FDE}$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Operating supply voltage	V_{SB} + 0.1		8.0	V
V_{SB}	Standby supply voltage[1]	TBD	4.8	5.7	V
V_{AS}	Supply voltage for automatic swell reset[2]		$0.5V_{SB}$		V
I_{DD}	Operating supply current		100	120	μA
I_{SB}	Standby supply current[3] at $V_{DD} < V_{SB}$		4	8	μA
Inputs					
V_{IL}	Input voltage LOW (any pin)	0		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH (any pin)	$0.7V_{DD}$		V_{DD}	V
	Pull-down circuits of inputs				
R_{IL}	$\overline{FDE}$, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH Pull-down resistance with input at V_{SS}		20		kΩ
I_{IH}	Pull-down current with input at V_{DD}		0.1		μA
	Pull-down circuit of FDI				
I_{SL}	Pull-down current with $V_{FDI} = 0.3V_{DD}$	TBD	20	TBD	μA
I_{SH}	Pull down current with $V_{FDI} = 0.7V_{DD}$		0.1		μA
I_{SX}	Pull-down current with $V_{DD} < V_{SB}$		0.1		μA
$\pm I_{IS}$	Current into input FDI[4]			0.2	mA
Outputs (TONE, $\overline{OPT}$)					
I_{OL}	Output sink current at V_{OL} = 0.5V	1	2		mA
$-I_{OH}$	Output source current at $V_{OH} = V_{DD} - 0.5V$	1	2		mA

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 6V; V_{SS} = 0; f_{OSC} = 64kHz; T_A = −25 to + 70°C; valid enable conditions at FDI and $\overline{FDE}$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$t_{D(on)}$	Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)[5]	1		1.5	ms
$t_{D(off)}$	Switch-off delay (with $\overline{FDE}$ = LOW) at FL = LOW			75	ms
$t_{D(off)}$	at FL = HIGH			112.5	ms
f_{OSC}	Oscillator frequency at R_{OSC} = 365kΩ; C_{OSC} = 56pF[6]	TBD	64	TBD	kHz
Δf_{OSC}	Frequency variation at V_{DD} = 5.7 to 8.0V			1	%

NOTES:

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC
4. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range)
5. The switch-on delay is measured in cycles of incoming ringing frequency
6. Lead lengths of R_{OSC} and C_{OSC} to be kept to a minimum.

FUNCTIONAL DESCRIPTION

Supply Pins (V_{DD} and V_{SS})

If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}) The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs

Oscillator (OSC)

The 64kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32kHz internal system clock

Selection Pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Figure 1). Thus, when the pins are open-circuit, they are defined LOW Therefore, only a single-contact switch is required to connect the pins to V_{DD}, yet the supply current is only marginally increased as I_{IH} is very small.

Frequency Discriminator Circuit (Pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.

The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.

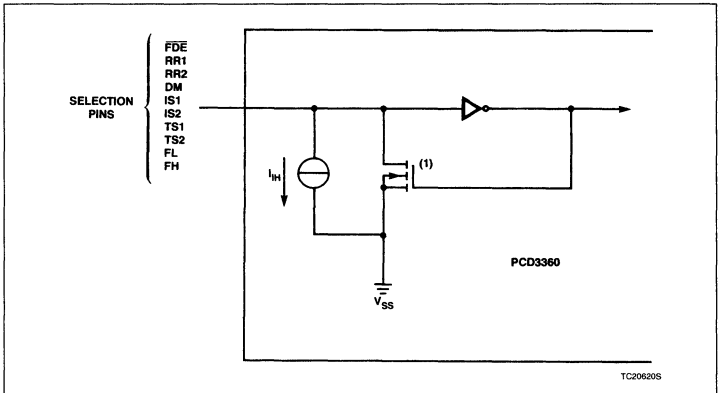
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.

The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfills the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1.5 cycles of the incoming ringing frequency.

FDI has a Schmitt trigger action, the levels are set by an external resistor R2 (see Figure 6) and an internal sink current that is switched from 20μA (typ.) for FDI = LOW to < 0.1μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed to internal diodes clamped to V_{DD} and V_{SS}.



NOTE.
1 Transistor resistance = R_{IL} when switched on

Figure 1. Input Circuit of Selection Pins

Selection of Frequency Discriminator Limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Tables 1 and 2, respectively.

Table 1. Selection of Lower Frequency Discriminator Limits (f_{OSC} = 64kHz)

FL INPUT STATE	LOWER DISCRIMINATOR LIMIT (Hz)
LOW	20
HIGH	13.33

Table 2. Selection of Upper Frequency Discriminator Limits (f_{OSC} = 64kHz)

FH INPUT STATE	UPPER DISCRIMINATOR LIMIT (Hz)
LOW	60
HIGH	30

Selection of Tone Sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Figure 2.

Four tone sequences are programmed in the internal ROM (see Figure 3). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask-programmable with any length up to 16 time intervals

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Figure 3.

Selection of Repetition Rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3. Duration of Time Intervals (f_{OSC} = 64kHz)

INPUT STATE		TIME INTERVAL (ms)
RR1	RR2	
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask-programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

6

Drive Mode Selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezoelectric transducers. An example of both signals, for a tone frequency of 667Hz, is shown in Figure 4.

Loudspeaker Mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE Mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g., the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of Impedance, Sound Pressure Level and Automatic Swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the DC resistance R_{xy} (seen at points x and y in Figure 6) and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

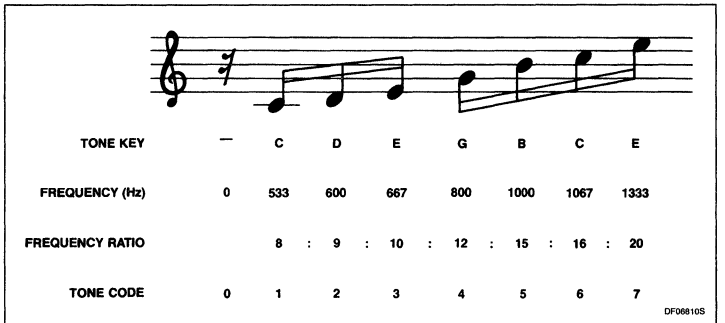


Figure 2. Available Tones and Their Corresponding Internal ROM Tone Code

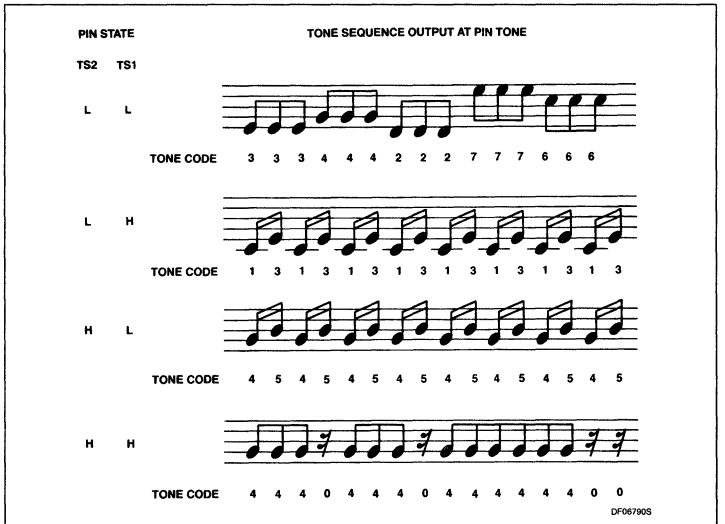


Figure 3. Tone Sequences Mask-Programmed in the PCD3360

Table 4. Setting of Pulse Duration and Automatic Swell (DM = LOW)

INPUT STATE		FUNCTION	RINGING BURST NUMBER (N)	PULSE DURATION (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			Fund	Harm			
L	L	Automatic Swell	1	1.8	1.6	40	TBD	TBD
			2	2.6		20	17.5	−4
			> 2	3.9		5	7	0
L	H	Constant Level		2.6		20	17.5	−4
H	L			3.6		10	10.5	TBD
H	H			5.0		5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{OSC} = 64kHz and f_{CK} = 32kHz.
2. SPL is the relative Sound Pressure Level, and 0dBr is defined as the SPL for IS1 = IS2 = HIGH
3. Values of the DC resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage $V_I = 40V_{RMS}$ in Figure 6.

Setting of Impedance, Sound Pressure Level and Automatic Swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.

Each time V_{DD} drops below V_{AS}, the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).

A buffer capacitor C3 (see Figure 6) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2, the pulse duration has a constant value Thus, the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Figure 5) The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10dB below the fundamental level

The harmonic frequency range is from 2kHz to 3 2kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5. Harmonic Frequency In Relation to Tone Code and Fundamental Frequency

TONE CODE	FREQUENCY (Hz)	
	Fundamental	Harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following.

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical Output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Figure 6

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by

- The logic threshold of input FDI ($0.5V_{DD}$ typ 3 4V for V_{DD} = 6 8V)
- The pull-down current of input FDI ($20\mu A$ typ for FDI < 3 4V)
- The value of R2 (680 kΩ in Figure 6)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH, V_H is the sum of the input threshold and the voltage drop across R2, thus:

$V_H = 3.4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17V$.

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH, the voltage drop across R2 can be discounted, thus $V_L = 3.4V$.

The minimum operating voltage across C3 is 17.7V which is determined by·

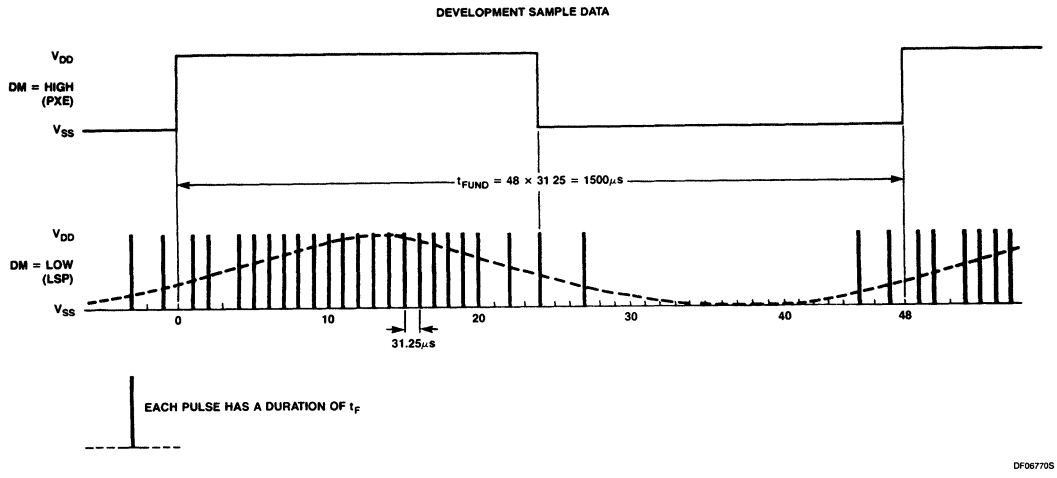
- The minimum operating voltage of the PCD3360 (5.7V)
- The supply current of the PCD3360 ($120\mu A$ maximum)
- The value of R3 (100kΩ in Figure 6)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5kV. During these surges the voltage on the 68V zener diode (BZW03) can rise to 100V; the DMOS transistor BST72 (TR1) has a maximum-drain source voltage of 100V. Up to 220V, 50Hz can be applied to the A/B terminals without damaging the ringer The choke (L1) in series with the 50Ω loudspeaker increases the sound pressure level by approximately 3dB by suppression of the 32kHz carrier frequency and its sidebands The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency

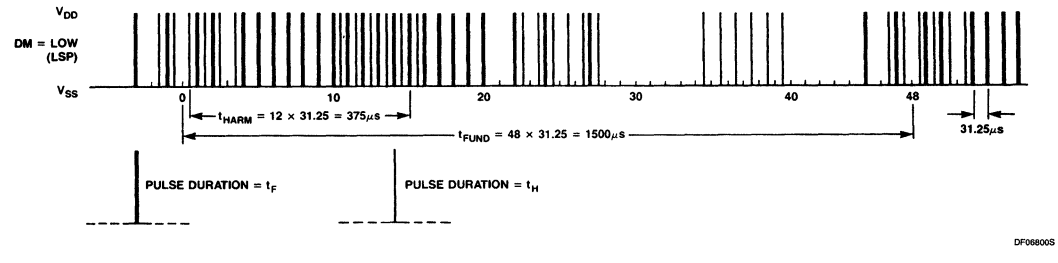
Application of the PCD3360 together with a PXE transducer is shown in Figure 7 The only significant difference between Figure 6 and Figure 7 is the output stage. Two BST72 transistors provide an output voltage swing almost equal to the voltage at C3 Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

6



NOTE:
For f_{OSC} = 64kHz, to provide f_{CK} = 32kHz.

Figure 4. Fundamental Signal (667Hz) at Pin TONE



NOTE:
For f_{OSC} = 64kHz, to provide f_{CK} = 32kHz.

Figure 5. Fundamental Signal (667Hz) + Harmonic Signal (2667Hz) at Pin TONE

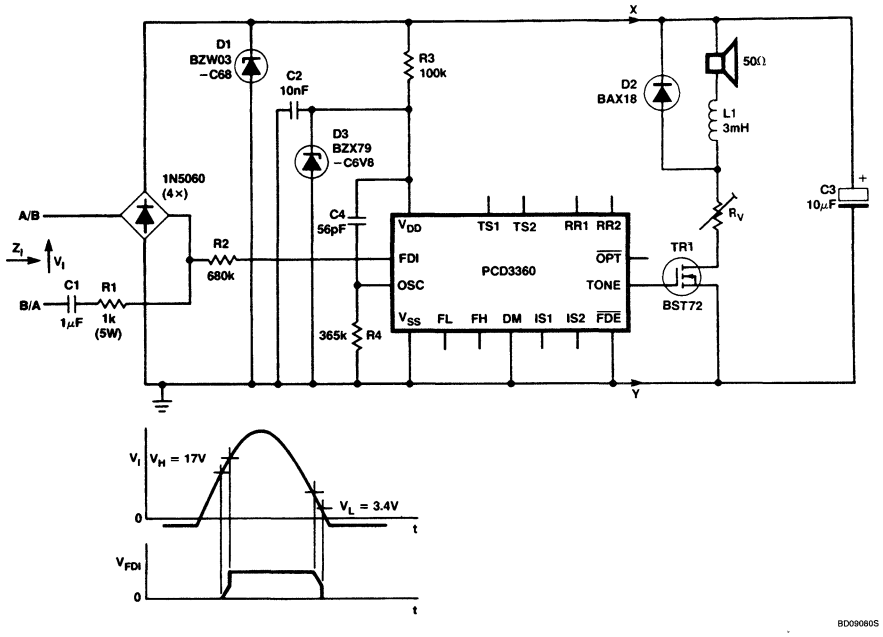


Figure 6. Transformerless Electronic Ringer With PCD3360 and a Loudspeaker

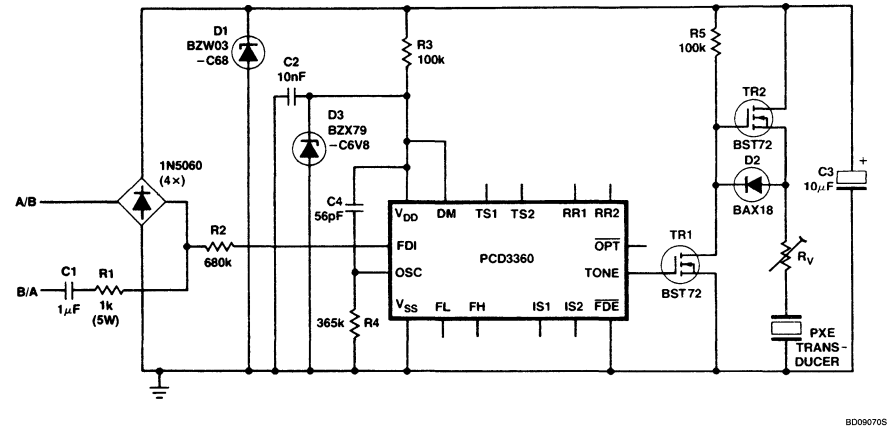


Figure 7. PCD3360 Ringer With PXE Transducer

Signetics

PCD4415/A
Pulse and DTMF Dialer with Redial

Product Specification

Linear Products

DESCRIPTION

The PCD4415/A is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3.58MHz crystal. It is a dual-standard dialing circuit for either pulse dialing (PD) or dual tone multi-frequency (DTMF) dialing.

Input data is derived from any standard matrix keyboard for dialing in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial.

In DTMF, mode bursts as well as pauses are timed to a minimum; in manual dialing the maximum depends on the key depression time.

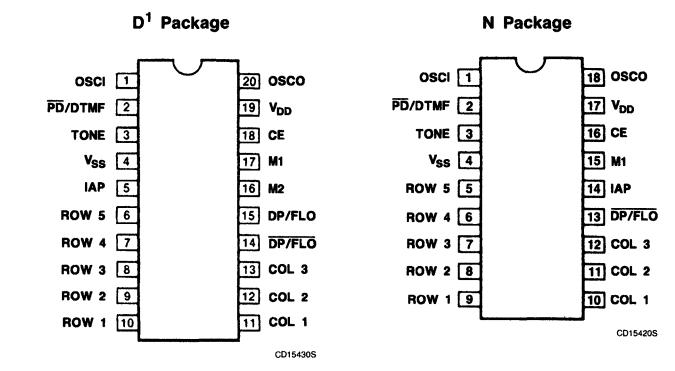
FEATURES

- **Pulse and DTMF dialing**
- **23-digit capacity for redial operation**
- **Three dialing modes: Pulse, DTMF, and data transmission (DTMF)**
- **Redial buffer for PABX and public calls**
- **Three function keys: * or >, # or R/AP, and FL (flash)**
- **DTMF timing: manual dialing - minimum duration for bursts and pauses redialing - calibrated timing**
- **On-chip voltage reference for supply and temperature independent tone output**
- **On-chip filtering for low output distortion (CEPT CS 203 compatible)**
- **Uses standard single-contact or double-contact (common left open) keyboard**
- **Keyboard entries fully debounced**
- **Flash (register recall) output**

APPLICATIONS

- **Telecom terminal equipment**

PIN CONFIGURATIONS



NOTE:
1 Available in large SO package with different pinout.

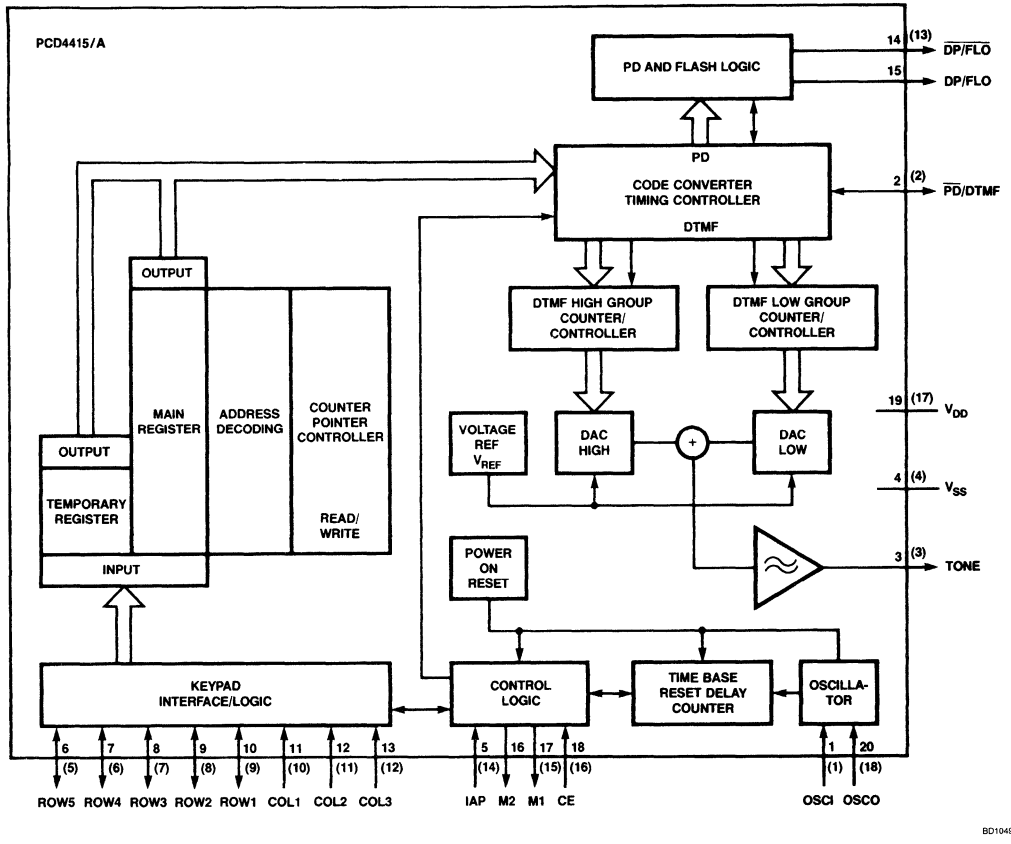
PIN NO. Supply	SYMBOL	DESCRIPTION
1	OSCI	Oscillator input
2	PD/DTMF	Select pin, pulse or DTMF dialing
3	TONE	Single or dual tone frequency output
4	V_{SS}	Negative supply
5	IAP	Input access pause
6	ROW 5	Scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	Sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	$\overline{DP}$/FLO	Dialing pulse and flash output
15	DP/FLO	Dialing pulse and flash output
16	M2	Strobe, active HIGH during transmission
17	M1	Muting output
18	CE	Chip enable input
19	V_{DD}	Positive supply
20	OSCO	Oscillator output

PIN NO. Supply	SYMBOL	DESCRIPTION
1	OSCI	Oscillator input
2	PD/DTMF	Select pin, pulse or DTMF dialing
3	TONE	Single or dual tone frequency output
4	V_{SS}	Negative supply
5	ROW 5	Scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	Sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	Dialing pulse and flash output
14	IAP	Input access pause
15	M1	Muting output
16	CE	Chip enable input
17	V_{DD}	Positive supply
18	OSCO	Oscillator output

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102)	−25°C to +70°C	PCD4415PN
20-Pin Plastic SOL; (SO-20; SOT-163A)	−25°C to +70°C	PCD4415TD
18-Pin Plastic DIP (SOT-102)	−25°C to +70°C	PCD4415APN
20-Pin Plastic SOL; (SO-20; SOT-163A)	−25°C to +70°C	PCD4415ATD

BLOCK DIAGRAM (D Package)



NOTE:
Pin numbers for N package are in parentheses

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0 8 to 8	V
I_{DD}	Supply current	50	mA
$\pm I_I$, $\pm V_O$	DC current into any input or output	10	mA
V_I	All input voltages	−0 8V to V_{DD} +0.8	°C
P_{TOT}	Total power dissipation	300	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

DC ELECTRICAL CHARACTERISTICS V_{DD} = 3V; V_{SS} = 0V; crystal parameters: f_{OSC} = 3.579545MHz; R_S = 100Ω max.; T_A = −25 to +70°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{DD}	Operating supply voltage		2.5		6.0	V
V_{DDO}	Standby supply voltage		1.8		6.0	V
	Operating supply current[2]					
I_{DDC}	conversation mode (oscillator ON)				150	μA
I_{DDP}	pulse dialing or flash				200	μA
I_{DDF}	DTMF dialing (tone ON)				0.9	mA
I_{DDF}	DTMF dialing (tone OFF)				200	μA
I_{DDO}	Standby supply current[1] (oscillator OFF)	V_{DD} = 1.8V T_A = 25°C			5	μA
Inputs						
V_{IL}	Input voltage LOW (any pin)		0		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH (any pin)		$0.7V_{DD}$		V_{DD}	V
$\|I_{IL}\|$	Input leakage current; CE				1	μA
	Keyboard inputs					
R_{KON}	Keyboard ON resistance				2	kΩ
R_{KOFF}	Keyboard OFF resistance		1			MΩ
Outputs						
I_{OL}	Output sink current	$V_{OL} = V_{SS}$ + 0.5V M1, M2, DP/FLO $\overline{DP/FLO}$	0.7			mA
$-I_{OH}$	Output source current	$V_{OH} = V_{DD}$ − 0.5V M1, M2, DP/FLO	0.6			mA
Timing and Frequency						
t_{ON}	Clock start-up time			4		ms
t_E	Debounce time			12		ms
t_{RD}	Reset delay time		152	160	168	ms
Tone output (see Figure 1)						
	DTMF output voltage levels ($_{RMS}$ value)	at V_{DD} = 2.5 to 6V				
$V_{HG(RMS)}$	HIGH group		158	192	205	mV
$V_{LG(RMS)}$	LOW group		125	150	160	mV
Δf/f	Frequency deviation		−0.6		+0.6	%
V_{DC}	DC voltage level			$0.5V_{DD}$		V
$\|Z_O\|$	Output impedance			0.1	0.5	kΩ
R_L	Load resistance		10			kΩ
ΔV_G	Pre-emphasis of group		1.85	2.1	2.35	dB
THD	Total harmonic distortion[2]	at T_A = 25°C		−25		dB

DC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 3V, V_{SS} = 0V; crystal parameters. f_{OSC} = 3 579545MHz, R_S = 100Ω max., T_A = −25 to +70°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Transmission and pause time[3]						
t_T	Manual and data transmission dialing mode		65			ms
t_P	Redialing		65			ms
t_T	Redialing		65	70	75	ms
t_P	Redialing		65	70	75	ms
t_{FL}	Flash pulse duration		95	100	105	ms
t_{FLH}	Flash hold-over time		32	34	36	ms
Pulse dialing (PD)[3]						
f_{DP}	Dialing pulse frequency		9 8	10	10.4	Hz
t_{ID}	Inter-digit pause		800	840	880	ms
t_B	Break time[4, 5]		64	66/60	68	ms
t_M	Make time[4, 5]		32	34/40	36	ms

NOTES:
1 Crystal connected between OSCI and OSCO, CE at V_{SS} and all other pins open-circuit
2. Related to the level of the LOW group frequency component (CEPT CS 203)
3 Other timing is possible on request
4. Mark-to-space ratio 2 1
5. A version mark-to-space ratio 3 2

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

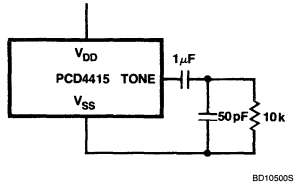


Figure 1. Tone Output Test Circuit

FUNCTIONAL DESCRIPTION

Power Supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.

To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.

If V_{DD} drops below the minimum standby supply voltage of 1.8V, the power-on reset circuit inhibits redialing after hook-off The power-on reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock Oscillator (OSCI, OSCO)

The time base for the PCD4415/A for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3 58MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC

CE = LOW provides the static standby condition In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Figure 3). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.

The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on. CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialing or redialing operation starts. The operating current is I_{DDP} if in the pulse dialing mode, or I_{DDF} if the DTMF dialing mode is selected. If the CE input is taken to a LOW level for more than time t_{RD} (see Figures 7a, 7b and timing data), the system changes to the static standby state and the oscillator stops running. Short CE pulses of t_{RD} will not affect the operation of the circuit and reset pulses are not produced.

Mode Selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse dialing mode is selected.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialing mode is selected. Each numeric push-button activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfill the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_T) or minimum pause time (t_P).

Data transmission mode

Data transmission mode is entered from the dialing mode (PD or DTMF) on first depression of key "*", or key " > ". The "*" tones are not transmitted.

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In the data transmission mode no digits are stored for later redial; "*" and "#" are purely DTMF keys, so are no longer special functions. The digits are temporarily stored in a special register, which has a maximum capacity of eight digits.

There are two ways to lease the data transmission mode:

- Reactivate chip enable (CE), HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard Inputs/Outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4415/A are directly connected to the keyboard as shown in Figure 2.

All keyboard entries are debounced on both the leading and trailing edges for approximately time t_E as shown in Figure 7. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the push-button.

Keys "*" and "#" represent the DTMF tones and also special dialing functions. In ROW 5 the keys ">" and R/AP only are function keys, while key FL offers flash or register recall.

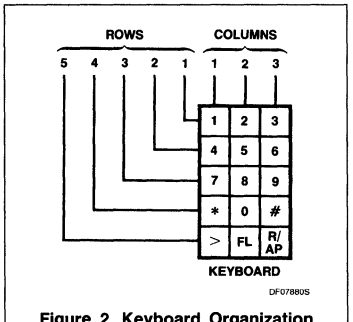

Figure 2. Keyboard Organization

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL push-button will produce a timed line-break of 100ms at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated at 100ms.

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number).

TONE Output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfills the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signaling.

When the DTMF mode is selected, output tones are timed in manual dialing with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Table 1. Frequency Tolerance of the Output Tones for DTMF Signaling

ROW/ COLUMN	STANDARD FREQUENCY HZ	TONE OUTPUT FREQUENCY HZ(1)	FREQUENCY DEVIATION	
			%	Hz
Row 1	697	697.90	+0.13	+0.90
Row 2	770	770.46	+0.06	+0.46
Row 3	852	850.45	−0.18	−1.55
Row 4	941	943.23	+0.24	+2.23
Col 1	1209	1206.45	−0.21	−2.55
Col 2	1336	1341.66	+0.42	+5.66
Col 3	1477	1482.21	+0.35	+5.21

NOTE:
1. Tone output frequency when using a 3.579545MHz crystal.

Dial Pulse and Flash Output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialing or for a calibrated break in both dialing modes (flash or register recall).

Dial Pulse and Flash Output ($\overline{DP/FLO}$)

Inverted output of DP/FLO. In the PCD4415/A it is only available as a bonding option of DP/FLO.

Mute Output (M1)

During pulse dialing the mute output becomes active-HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out. During DTMF dialing the mute output becomes active-HIGH for the period of the tone transmission and pause times. During Flash the mute output is active-HIGH and remains at this level for the period of flash and flash hold-over time

Mute Output ($\overline{M1}$)

Inverted output of M1. In the PCD4415/A it is only available as a bonding option of M1.

Strobe Output (M2)

Active-HIGH output during actual dialing, i.e., during break and make time in pulse dialing, or during tone transmission in DTMF dialing. Only available as a bonding option of IAP.

Input Access Pause (IAP)

This input can be used instead of the "#" (R/AP) key for programming access pause(s) in RAM when dialing and terminating access pause(s) during redial.

Data Transmission Mode

Timing in the data transmission mode is the same as the manual dialing mode.

Dialing Procedures (see also Figures 4, 5 and 6)

Dialing

After CE has risen to V_{DD}, the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Figure 3). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. If more than 23 digits are entered, redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least time t_E as shown in Figure 7. Each entry is tested for validity before being deposited in the redial register.

In manual dialing mode (pulses and DTMF) only the 0 to 9 keys result in dialing operations. "#" and "*" are special function keys:

- If the first key after CE or Flash means: Redial (see redial procedure)
- If not the first key, then it is used to program access pause(s) in the RAM for later redial. If it is the last key it will be omitted before going "on-hook".

"*" key or ">" key

- Used to switch from dialing mode (pulse or DTMF) to data transmission mode. The "*" tones will not be transmitted even if the previous mode was DTMF dialing.

In data transmission mode keys 0 to 9, "*" and "#" result in associated DTMF tones (see Table 1), keys > and R/AP will be ignored.

Redialing

After CE has risen to V_{DD}, the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4415/A is in conversation mode. If "#" or "R/AP" is the first keyboard entry, the circuit starts redialing the contents of the register. Timing in the DTMF mode is calibrated for both tone bursts and pauses. Only the first part entered (the pulse or DTMF dialed part of the stored number) can be redialed. During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialing. The "#" and R/AP keys are active only during access pauses.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory overflow (more than 23 valid data entries)

If an access pause is detected during redial, the circuit is switched back to the conversation mode and stays there until the "#" or R/AP key is depressed. Therefore, when the "#" or R/AP key is depressed, the access pause is ended. After termination of the access pause, the circuit continues dialing the rest of the telephone number.

In addition to the manual use of the # or R/AP key for programming and terminating access pause(s), the input IAP can be used. If during manual dialing and conversation mode IAP becomes HIGH, an access pause will be stored in the memory.

If, after "on-hook" or "flash", the last stored digit is an access pause, then it will be deleted out of the memory. When during redialing an access pause occurs and IAP becomes HIGH, then the access pause will be automatically terminated and redialing continues.

As soon as the conversation mode is entered, depressing the "*" or ">" key will again switch the circuit to the data transmission mode.

Redial takes place in the main register (max. 23 digits). After redial when a numeric key is pressed (first digit of an extension number) the redial number will be cleared. Thus the total capacity of the main register is available for extension number dialing. This extension number is stored in the main register (max 23 digits) and is available later after "on-hook", "off-hook". The main register will also store digits that have been keyed-in at a rate faster than dialed out

Access pause

- The number of access pauses is unlimited.
- Consecutive pauses will be stored as a single pause.

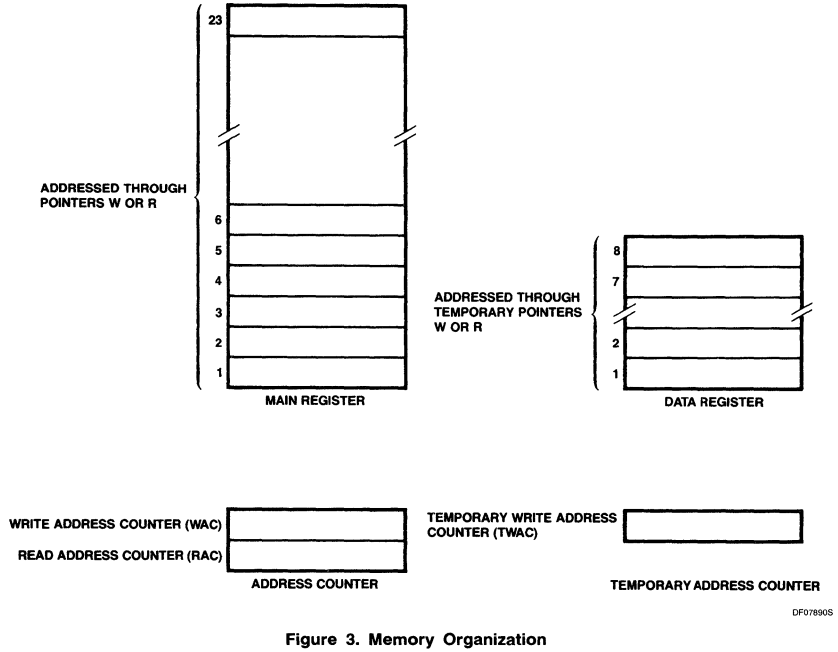

Figure 3. Memory Organization

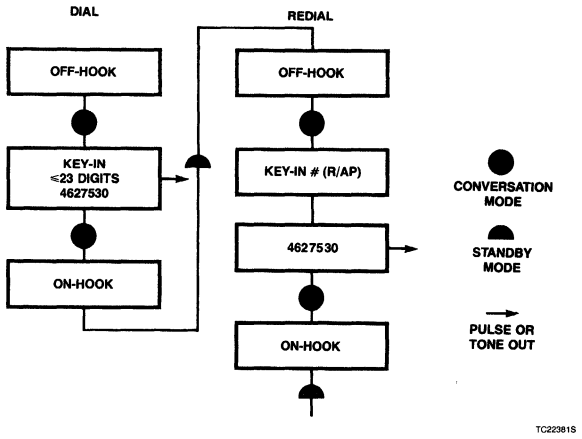

Figure 4. Pulse/DTMF Dialing Mode

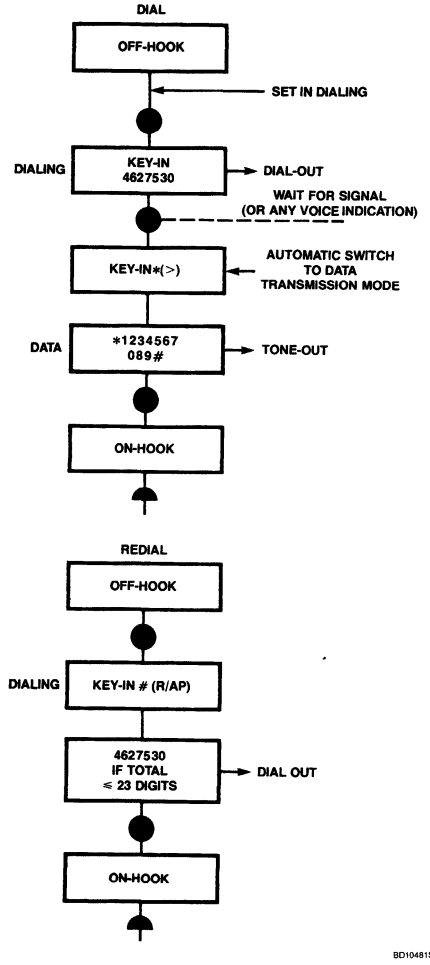

Figure 5. Pulse/DTMF Dialing and Data Transmission Mode

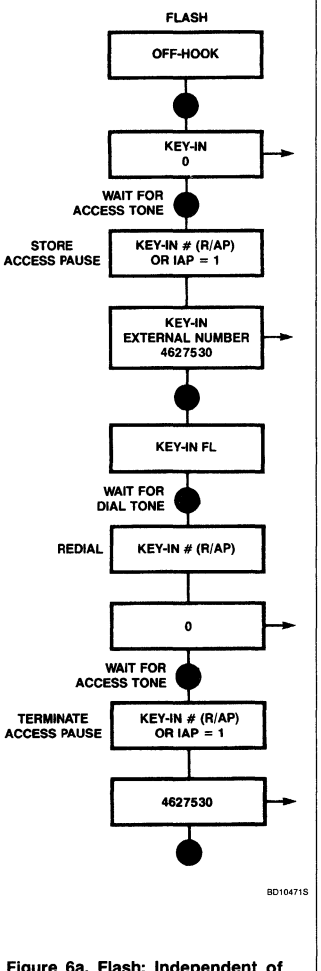

Figure 6a. Flash: Independent of Dialing Mode

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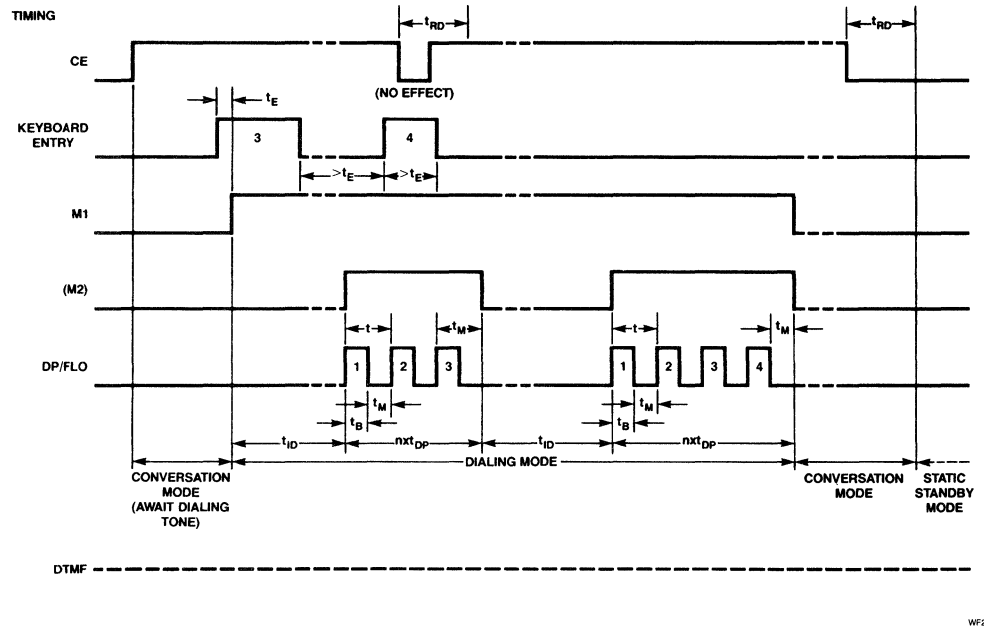

Figure 6b. Timing Diagram for Dialing Mode Defined by $\overline{PD}$/DTMF Selection Pin; Pulse Dialing ($\overline{PD}$/DTMF = V_{SS})

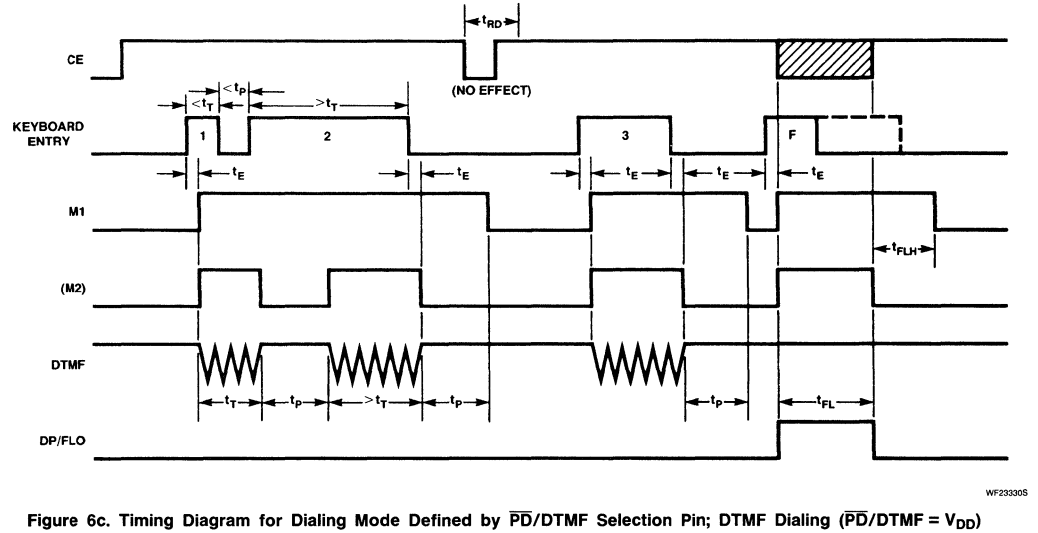

Figure 6c. Timing Diagram for Dialing Mode Defined by $\overline{PD}$/DTMF Selection Pin; DTMF Dialing ($\overline{PD}$/DTMF = V_{DD})

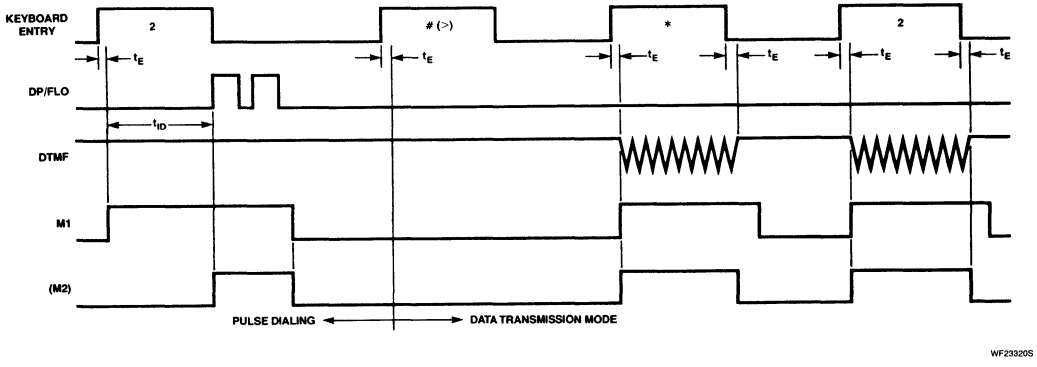

Figure 6d. Timing Diagram for Dialing Mode Defined by $\overline{PD}$/DTMF Selection Pin; Pulse Dialing and Data Transmission Mode

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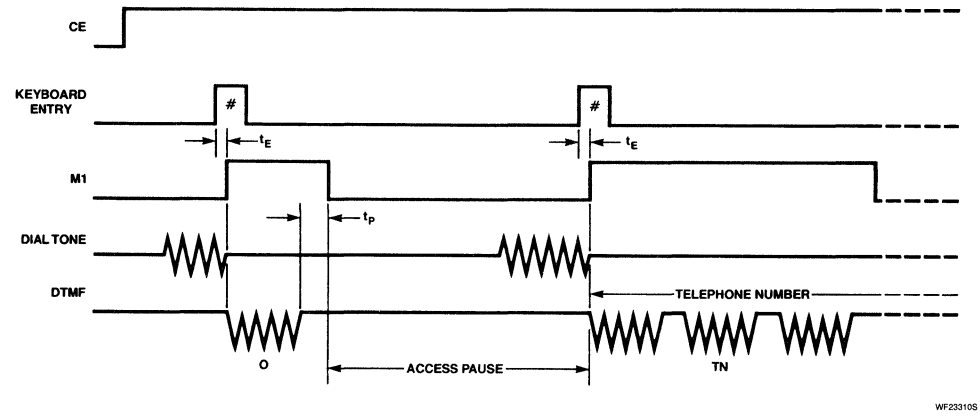


Figure 7a. Timing Diagram Showing REDIAL Where PABX Access Digit(s) are the First Keyboard Entries and Access Pause is Terminated by the # or R/AP Key; DTMF Dialing with $\overline{PD}$/DTMF = V_{DD}

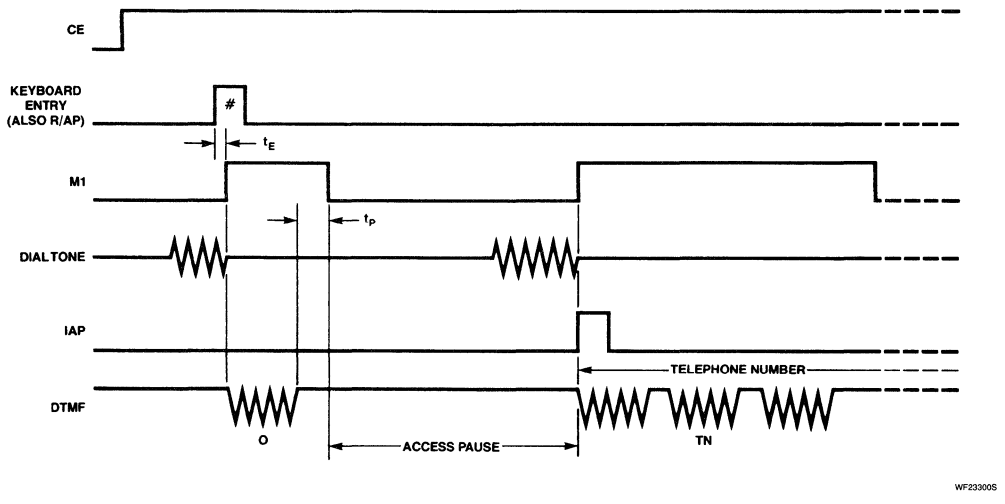
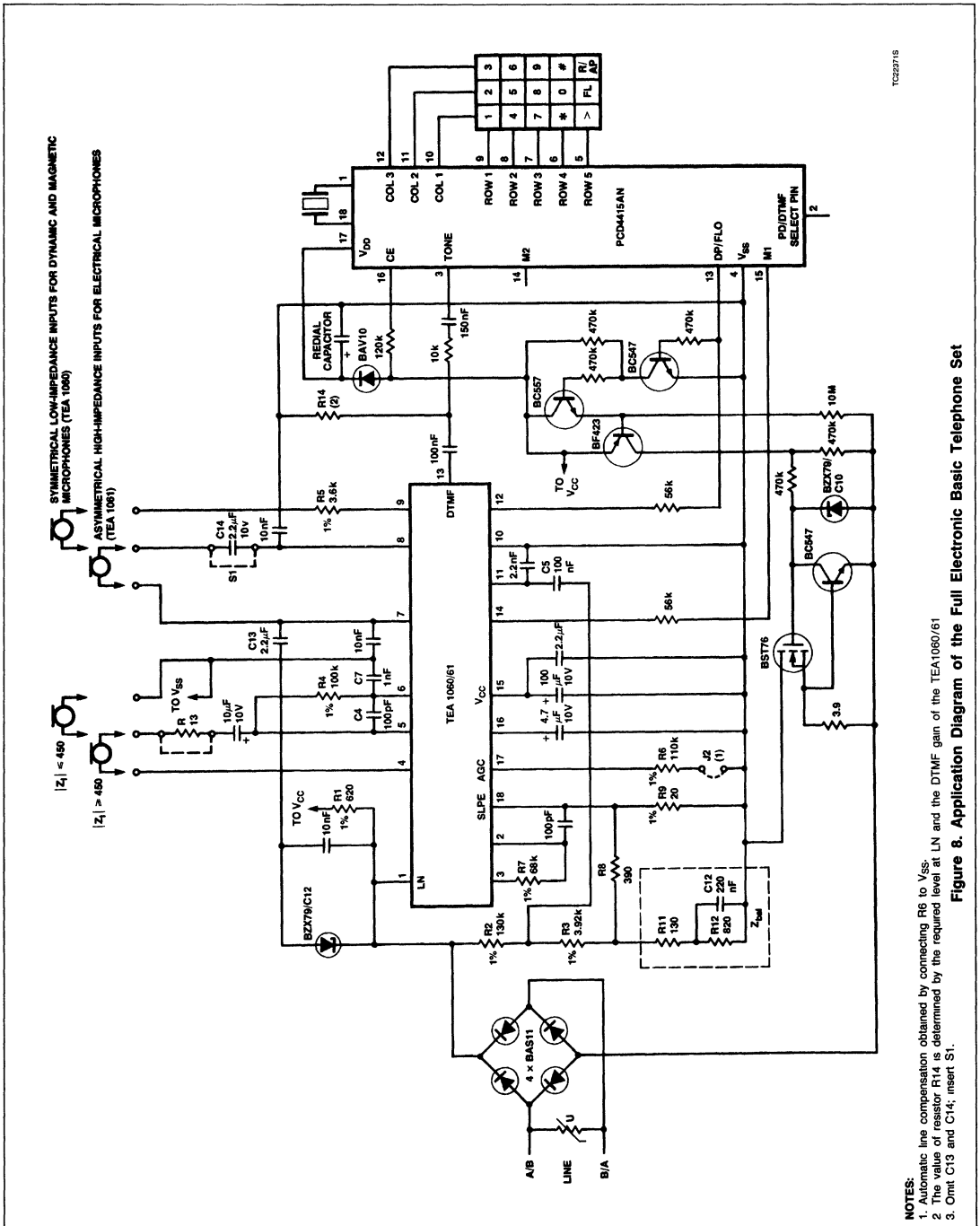


Figure 7b. Timing Diagram Showing REDIAL Where PABX Access Digit(s) Occur and are Terminated by IAP; DTMF Dialing with $\overline{PD}$/DTMF = V_{DD}



NOTES:
1. Automatic line compensation obtained by connecting R6 to V_{SS}.
2. The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61
3. Omit C13 and C14; insert S1.

Figure 8. Application Diagram of the Full Electronic Basic Telephone Set

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Signetics

TEA1060/61
Versatile Telephone Transmission Circuits with Dialer Interface

Linear Products

Product Specification

DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The circuits internally performs electronic switching between dialing and speech.

FEATURES

- **Voltage regulator with adjustable static resistance**
- **Provides supply for external circuitry**
- **Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)**
- **Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)**
- **Asymmetrical high-impedance input for electret microphone (TEA1061)**
- **DTMF signal input**
- **Mute input for pulse or DTMF dialing**
- **Power down input for pulse dial or register recall**
- **Receiving amplifier for magnetic, dynamic or piezoelectric earpieces**
- **Large amplification setting range on all amplifiers**
- **Line loss compensation facility, line current dependent**
- **Gain control adaptable to exchange supply**

APPLICATION

- **Electronic telephone sets**

ORDERING INFORMATION

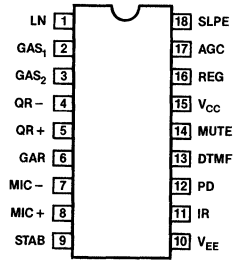
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102A)	−25 to +75°C	TEA1060PN
18-Pin Plastic DIP (SOT-102A)	−25 to +75°C	TEA1061PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{LN}	Positive line voltage	13.2	V
	Line current		
$I_{LINE(AV)}$	average	140	mA
$I_{LINE(S)}$	non-repetitive (t_{MAX} = 100 hours)	250	mA
$I_{LINE(SM)}$	non-repetitive peak (t_{MAX} = 1ms)	1	A
V	Voltage on all other pins	V_{CC} + 0.7	V
−V		0.7	V
P_{TOT}	Total power dissipation	660	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +75	°C

PIN CONFIGURATION

N Package



TOP VIEW

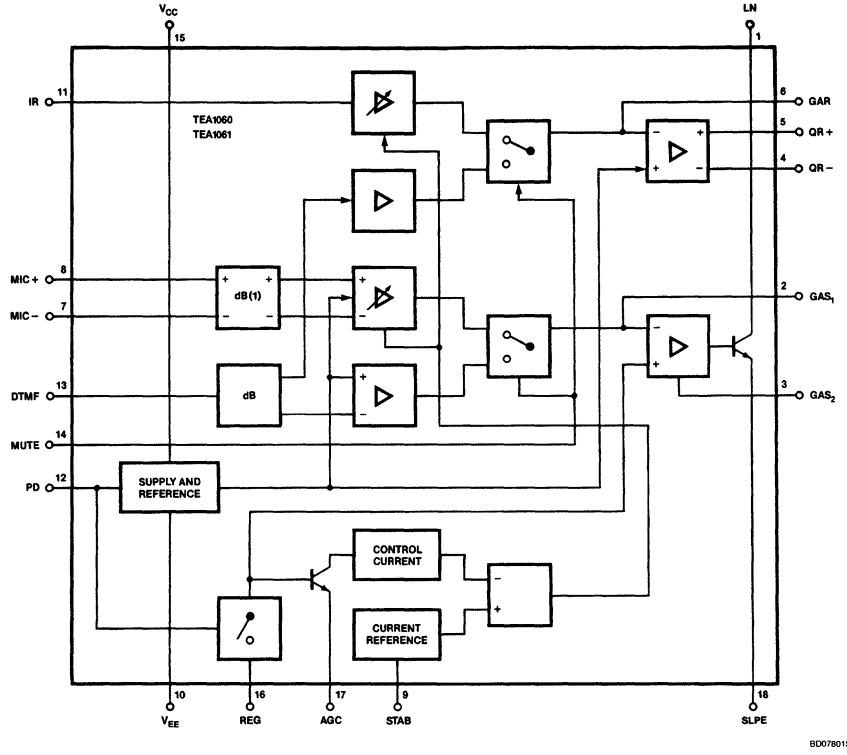
CD11540S

PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line terminal
2	GAS_1	Gain adjustment, transmitting amplifier
3	GAS_2	Gain adjustment, transmitting amplifier
4	QR−	Inverting output, receiving amplifier
5	QR+	Non-inverting output, receiving amplifier
6	GAR	Gain adjustment, receiving amplifier
7	MIC−	Inverting microphone input
8	MIC+	Non-inverting microphone input
9	STAB	Current stabilizer
10	V_{EE}	Negative line terminal
11	IR	Receiving amplifier input
12	PD	Power-down input
13	DTMF	Dual-tone multi-frequency input
14	MUTE	Mute input
15	V_{CC}	Positive supply decoupling
16	REG	Voltage regulator decoupling
17	AGC	Automatic gain control input
18	SLPE	Slope (DC resistance) adjustment

Versatile Telephone Transmission Circuits with Dialer Interface

TEA1060/61

BLOCK DIAGRAM



NOTES:
The blocks marked "dB" are attenuators
The block marked (1) is only present in the TEA1061

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DC ELECTRICAL CHARACTERISTICS I_{LINE} = 10 to 140mA; V_{EE} = 0V; f = 800Hz; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply: LN and V_{CC} (Pins 1 and 15)					
	Voltage drop over circuit				
V_{LN}	at I_{LINE} = 5mA		4.15		V
V_{LN}	at I_{LINE} = 15mA	4.15	4.35	4.55	V
V_{LN}	at I_{LINE} = 100mA	5.4	6.1	6.7	V
V_{LN}	at I_{LINE} = 140mA			7.5	V
$\Delta V_{LN}/\Delta T$	Variation with temperature at I_{LINE} = 15mA	−4	−2	0	mV/°C
	Supply current				
I_{CC}	at V_{CC} = 2.8V; PD = LOW		0.96	1.25	mA
I_{CC}	at V_{CC} = 2.8V; PD = HIGH		50		μA
Microphone inputs MIC+ and MIC−					
	Input impedance				
$\lvert Z_{IS}\rvert$	TEA1060		4		kΩ
$\lvert Z_{IS}\rvert$	TEA1061		20		kΩ
σ	Standard deviation on input impedance		12		%
k_{CMR}	Common-mode rejection ratio; TEA1060		80		dB
	Voltage amplification at I_{LINE} = 15mA; R7 = 68kΩ				
A_{VD}	TEA1060	51	52	53	dB
A_{VD}	TEA1061	37	38	39	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency at f = 300 to 3400Hz		±0.2		dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA; T_A = −25 to +75°C		±0.5		dB
Dual-tone multi-frequency input DTMF					
$\lvert Z_{IS}\rvert$	Input impedance		20		kΩ
σ	Standard deviation on input impedance		12		%
A_{VD}	Voltage amplification at I_{LINE} = 15mA; R7 = 68kΩ	25	26	27	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency at f = 300 to 3400Hz		±0.2		dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA; T_A = −25 to +75°C		±0.5		dB
Gain adjustment (Pins GAS_1 and GAS_2)					
ΔA_{VD}	Amplification variation with R7, transmitting amplifier	−8		+8	dB
Transmitting amplifier output LN					
	Output voltage at I_{LINE} = 15mA;				
$V_{LN(RMS)}$	d_{TOT} = 2%	1.4	2.3		V
$V_{LN(RMS)}$	d_{TOT} = 10%		2.6		V
	Noise output voltage at I_{LINE} = 15mA; R7 = 68kΩ				
$V_{NO(RMS)}$	psophometrically weighted (P53 curve)		−70		dBmp
Receiving amplifier input IR					
$\lvert Z_{IS}\rvert$	Input impedance	17	21	25	kΩ

DC ELECTRICAL CHARACTERISTICS (Continued) I_{LINE} = 10 to 140mA; V_{EE} = 0V; f = 800Hz; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Receiving amplifier outputs QR+ and QR–					
$\|Z_{OS}\|$	Output impedance; single-ended		4		Ω
	Voltage amplification at I_{LINE} = 15mA; R4 = 100kΩ;				
A_{VD}	single-ended; R_L = 300Ω	24	25	26	dB
A_{VD}	differential; R_L = 600Ω	30	31	32	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency, at f = 300 to 3400Hz		±0.2		dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA; T_A = −25 to +75°C		±0.5		dB
	Output voltage at I_{CC} = 0; d_{TOT} = 2%; sine wave drive				
$V_{O(RMS)}$	single-ended; R_L = 150Ω	0.3	0.38		V
$V_{O(RMS)}$	single-ended; R_L = 450Ω	0.4	0.52		V
$V_{O(RMS)}$	differential; C_L = 47nF + R_L = 100Ω; f = 3400Hz	0.8	1.0		V
	Noise output voltage at I_{LINE} = 15mA; R4 = 100kΩ; psophometrically weighted (P53 curve)				
$V_{NO(RMS)}$	single-ended; R_L = 300Ω		50		μV
$V_{NO(RMS)}$	differential; R_L = 600Ω		100		μV
Gain adjustment (Pin GAR)					
ΔA_{VD}	Amplification variation with R4, receiving amplifier	−8		+8	dB
MUTE input					
	Input voltage				
V_{IH}	HIGH	1.5		V_{CC}	V
V_{IL}	LOW			0.3	V
I_{MUTE}	Input current		8	15	μA
$-\Delta A_{VD}$	Reduction of voltage amplification from MIC+ and MIC– to LN at MUTE = HIGH		70		dB
$-\Delta A_{VD}$	Reduction of gain between I_{LINE} = 15mA and I_{LINE} = 35mA	−1.0	−1.5	−2.0	dB
A_{VD}	Voltage amplification from DTMF to QR+ or QR– at MUTE = HIGH; single-ended load; R_L = 300Ω		−18		dB
Power-down input PD					
	Input voltage				
V_{IH}	HIGH	1.5		V_{CC}	V
V_{IL}	LOW			0.3	V
I_{PD}	Input current		5	10	μA
Automatic gain control input AGC					
$-\Delta A_{VD}$	Amplification control range		6		dB
I_{LINE}	Highest line current for maximum amplification at R6 = 110kΩ		22		mA
I_{LINE}	Lowest line current for minimum amplification at R6 = 110kΩ		60		mA
Peripheral supply across Pins 15 and 10					
V_{CCP}	I_P = 0mA	3.5	3.75		V
	I_P = 1.2mA	2.8	3.05		V
	I_P = 1.7mA	2.5			V

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FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e g., dialing and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}, the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage, V_{EXCH}, the feeding bridge resistance R_{EXCH}, the DC resistance of the subscriber line R_{LINE} and the DC voltage on the subscriber set (see Figure 1).

If the line current I_{LINE} exceeds the current I_{CC} + 0 5mA required by the circuit itself ($I_{CC} \approx 1mA$), plus the current I_{CC} required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{REF} + I_{SLPE} \times R9$$
$$= V_{REF} + (I_{LINE} - I_{CC} - 0\ 5\ 10^{-3} - I_{CC}) \times R9$$

V_{REF} being an internally-generated temperature-compensated reference voltage of 4.1V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{SLPE} \geqslant I_{CC}$ + 0.5mA + I_{CC} The static behavior of the circuit then equals a 4.1V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1.

The current I_{CC} available from V_{CC} for supplying peripheral circuits depends on external components, and on the line current. Figure 2 shows this current for V_{CC} = 3V min., this being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW, the available current is further reduced when the receiving amplifier is driven.

Microphone Inputs MIC + and MIC − and Gain Adjustment Pins GAS_1 and GAS_2

The TEA1060 and TEA1061 have symmetrical microphone inputs.

The TEA1060 is intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Its input impedance is 2 × 4kΩ and its voltage amplification is typically 52dB.

The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 × 20kΩ and its voltage amplification is typically 38dB.

The arrangements with the microphone types mentioned are shown in Figure 3.

The amplification of the microphone amplifier in both types can be adjusted over a range of ±8dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS_1 and GAS_2

An external capacitor C6 of 100pF between GAS1 and SLPE is required to ensure stability A larger value may be chosen to obtain a first-order low-pass filter The cut-off frequency corresponds with the time constant R7 × C6.

Mute Input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-Tone Multi-Frequency Input DTMF

When the DTMF input is enabled, dialing tones may be sent onto the line. The voltage amplification from DTMF to LN is typically 26dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier: IR, QR +, QR − and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR + and an inverting output QR −. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Figure 6). Amplification from IR to QR + is typically 25dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6dB. This makes differential drive possible, which is required for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 450Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + 8dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR + .

Two external capacitors C4 = 100pF and C7 = 10 × C4 = 1nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 × C4.

Automatic Gain Control Input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6dB. This corresponds with a line length of 5km for a 0.5mm diameter copper twisted-pair cable with a DC resistance of 176Ω/km and an average attenuation of 1.2dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Figure 5 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-Down Input PD

During pulse dialing or register recall (timed loop break) the telephone line is interrupted; as a consequence, it provides no supply for the transmission circuit. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input, which reduces the supply current from typically 1mA to typically 50μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the circuit's impedance equals a 4.1V voltage regulator diode with an internal resistance equal to R9. This results in rectangular current waveforms in pulse dialing and register recall. When this facility is not required PD may be left open.

Side-Tone Suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{BAL} (see Figure 8). Maximum compensation is obtained when Z_{BAL}/k equals the line impedance Z_{LINE} as seen by the set (scale factor $k = R_8/R_1$).

In practice Z_{LINE} varies strongly with line length and cable type; consequently, an average value has to be chosen for Z_{BAL}. The suppression further depends on the accuracy with which Z_{BAL}/k equals the average line impedance.

The anti-side-tone network attenuates the signal from the line. With R8 = 390Ω and R9 = 20Ω the attenuation is 32dB. The attenuation is nearly flat over the audio-frequency range.

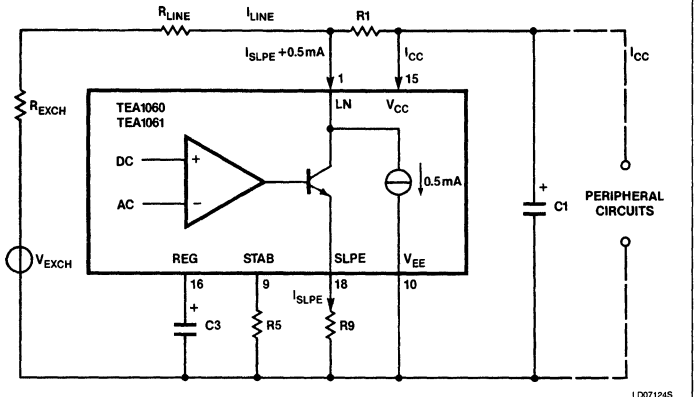
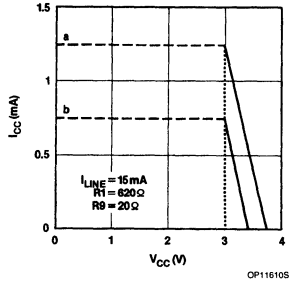
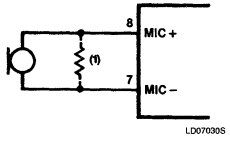


Figure 1. Supply Arrangement



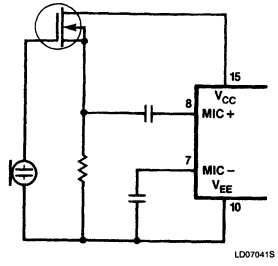
NOTE:
Curve "a" is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve "b" is valid when MUTE = LOW and the receiving amplifier is driven, $V_{O(RMS)}$ = 150mV, R_L = 150Ω

Figure 2. Maximum Current I_{CC} Available from V_{CC} for External (Peripheral) Circuitry with $V_{CC} \geqslant 3V$

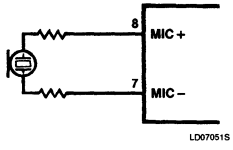


NOTE:
The resistor marked (1) may be connected to lower the terminating impedance

a. Magnetic or Dynamic Microphone, TEA1060

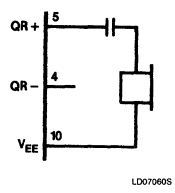


b. Electret Microphone, TEA1061

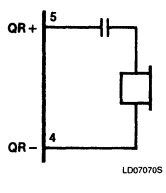


c. Piezoelectric Microphone TEA1061

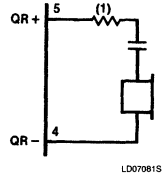
Figure 3. Alternative Microphone Arrangements



a. Dynamic Telephone with Less Than 450Ω Impedance

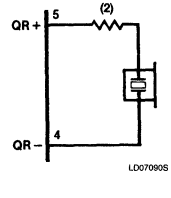


b. Dynamic Telephone with More Than 450Ω Impedance



NOTE:
The resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic

c. Magnetic Telephone with More Than 450Ω Impedance



NOTE:
The resistor marked (2) is required to increase the phase margin

d. Piezoelectric Telephone

Figure 4. Alternative Receiver Arrangements

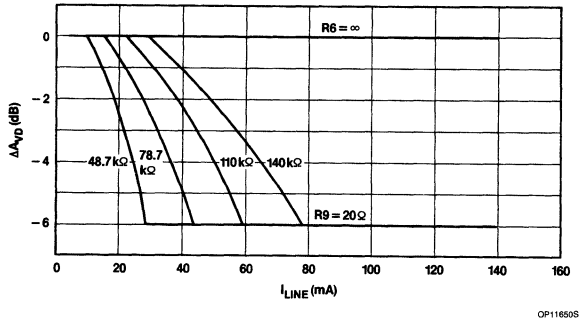
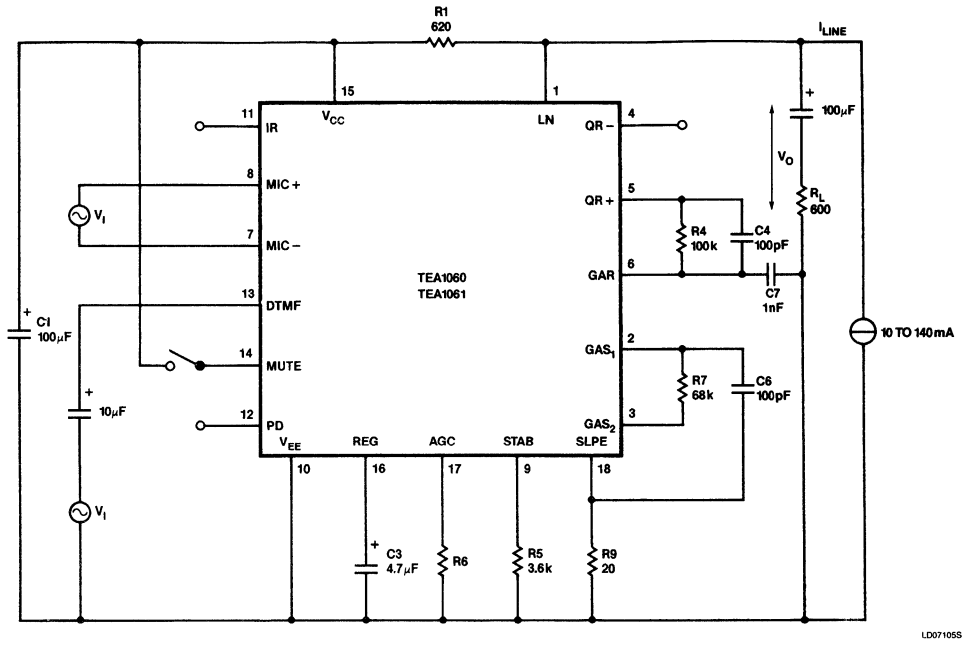


Figure 5. Variation of Amplification with Line Current, with R6 as a Parameter

Table 1. Values of Resistor R6 for optimum Line Loss Compensation, for Various Usual Values of Exchange Supply Voltage V_{EXCH} and Exchange Feeding Bridge Resistance R_{EXCH}

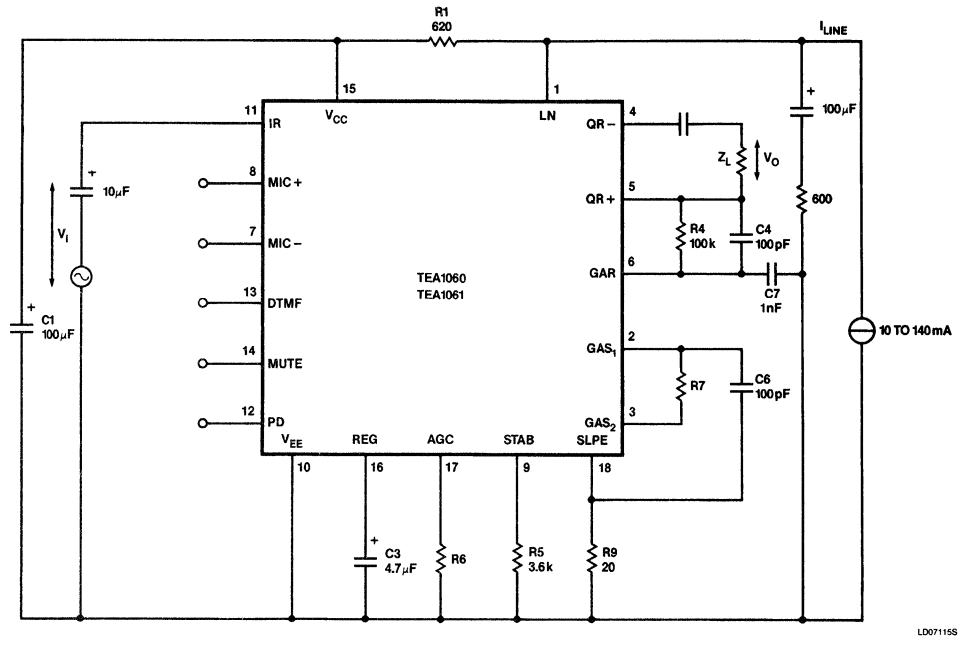
		R_{EXCH} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{EXCH} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102



NOTES:
Voltage amplification is defined as $A_{VD} = 20 \log |V_O/V_I|$
For measuring the amplification from MIC+ and MIC–, the MUTE input should be LOW or open, for measuring the DTMF input, MUTE should be HIGH
Inputs not under test should be open

Figure 6. Test Circuit for Defining Voltage Amplification of MIC+, MIC– and DTMF Inputs

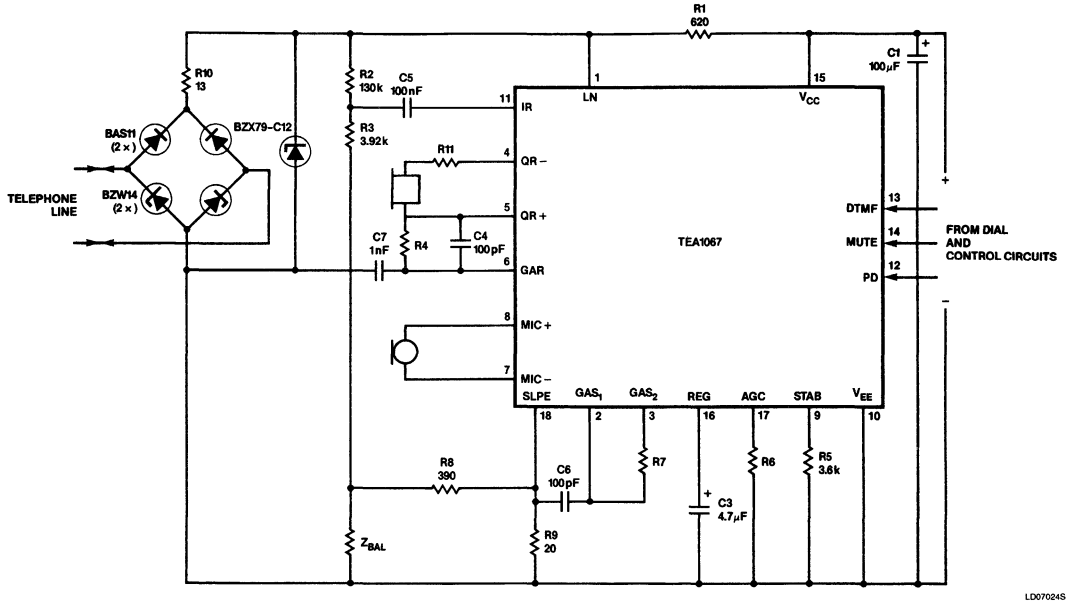
6



NOTE:
Voltage amplifictaion is defined as $A_{VD} = 20 \log |V_O/V_I|$

Figure 7. Test Circuit for Defining Voltage Amplification of the Receiving Amplifier

APPLICATION INFORMATION

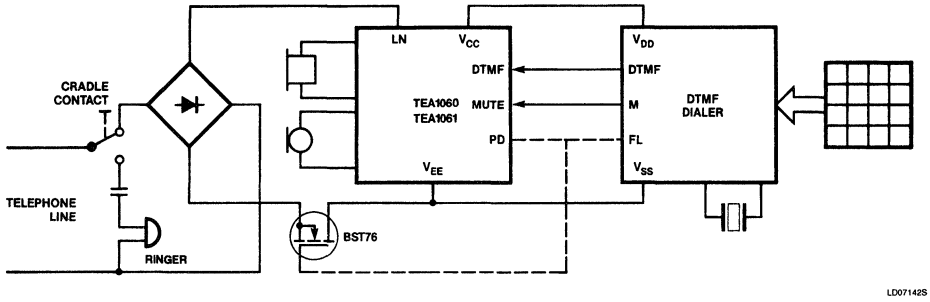


NOTE:
The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialing or register recall require a different protection arrangement.

Figure 8. Typical Application of the TEA1060 or TEA1061, Shown Here with a Piezoelectric Earpiece and DTMF Dialing

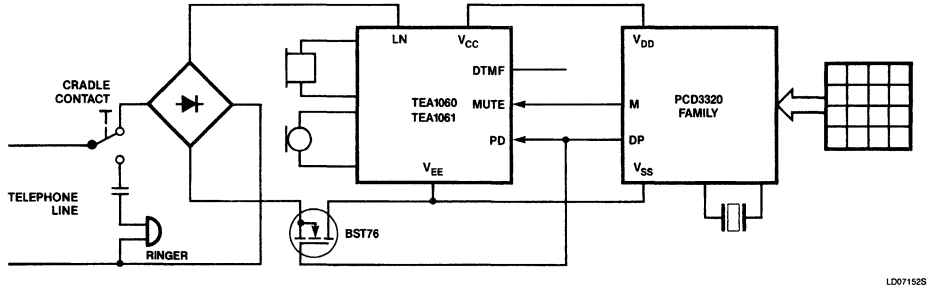
6

APPLICATION INFORMATION (Continued)

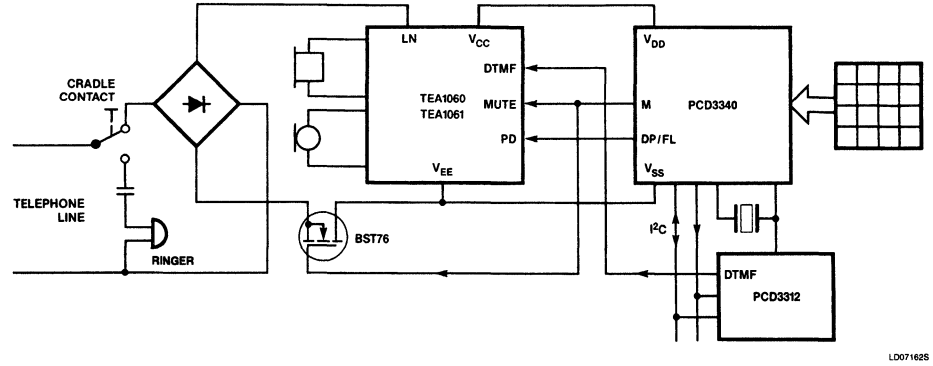


NOTE:
The dashed lines show an optional flash (register recall by timed loop break)

a. DTMF Set with a CMOS DTMF Dialing Circuit



b. Pulse Dial Set with One of the PCD3320 Family of CMOS Interrupted Current-Loop Dialing Circuits



c. Dual-Standard (Pulse and DTMF) Feature Phone with the PCD3340 CMOS Telephone Controller and the PCD3312 CMOS DTMF Generator with I^2C Bus

Figure 9. Typical Applications of the TEA1060 or TEA1061 (Simplified)

Signetics

TEA1067
Low Voltage Transmission IC with Dialer Interface

Product Specification

Linear Products

DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialing and speech. The circuit is able to operate down to DC line voltage of 1.6V (with reduced performance) to facilitate the use of more telephone sets in parallel.

FEATURES

- **Low DC line voltage; operates down to 1.6V (excluding polarity guard)**
- **Voltage regulator with adjustable static resistance**
- **Provides supply with limited current for external circuitry**
- **Symmetrical high-impedance inputs (64kΩ) for dynamic, magnetic or piezoelectric microphones**
- **Asymmetrical high-impedance input (32kΩ) for electret microphone**
- **DTMF signal input with confidence tone**
- **Mute input for pulse or DTMF dialing**
- **Power down input for pulse dial or register recall**
- **Receiving amplifier for magnetic, dynamic or piezoelectric earpieces**
- **Large amplification setting range on microphone and earpiece amplifiers**
- **Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)**
- **Gain control adaptable to exchange supply**
- **Possibility to adjust the DC line voltage**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−25°C to +75°C	TEA1067PN
20-Pin Plastic SOL (SOT-163A)	−25°C to +75°C	TEA1067TD

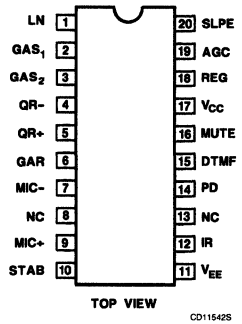
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{LN}	Positive line voltage continuous	12	V
V_{LN}	Repetitive line voltage during switch-on or line interruption	13.2	V
V_{LN}	Repetitive peak line voltage $t_{P/P}$ = 1ms/5s; R10 = 13Ω; R9 = 20Ω (see Figure 8)	28	V
I_{LINE}	Line current	140	mA
V_I $-V_I$	Voltage on all other pins	V_{CC} + 0.7 0.7	V V
P_{TOT}	Total power dissipation	660	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +75	°C

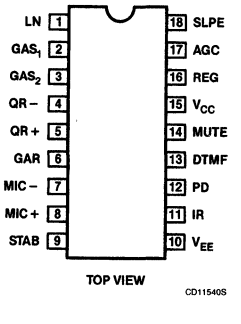
6

PIN CONFIGURATION

D[1] Package



N Package



NOTE:
1. Available only in large SO package (SOL) with different pinout.

PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line terminal
2	GAS_1	Gain adjustment, transmitting amplifier
3	GAS_2	Gain adjustment, transmitting amplifier
4	QR–	Inverting output, receiving amplifier
5	QR+	Non-inverting; receiving amplifier
6	GAR	Gain adjustment, receiving amplifier
7	MIC–	Inverting microphone input
8	NC	Not connected
9	MIC+	Non-inverting microphone input
10	STAB	Current stabilizer
11	V_{EE}	Negative line terminal
12	IR	Receiving amplifier input
13	NC	Not connected
14	PD	Power-down input
15	DTMF	Dual-tone multi-frequency input
16	MUTE	Mute input
17	V_{CC}	Positive supply decoupling
18	REG	Voltage regulator decoupling
19	AGC	Automatic gain control input
20	SLPE	Slope (DC resistance) adjustment

PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line terminal
2	GAS_1	Gain adjustment, transmitting amplifier
3	GAS_2	Gain adjustment, transmitting amplifier
4	QR–	Inverting output, receiving amplifier
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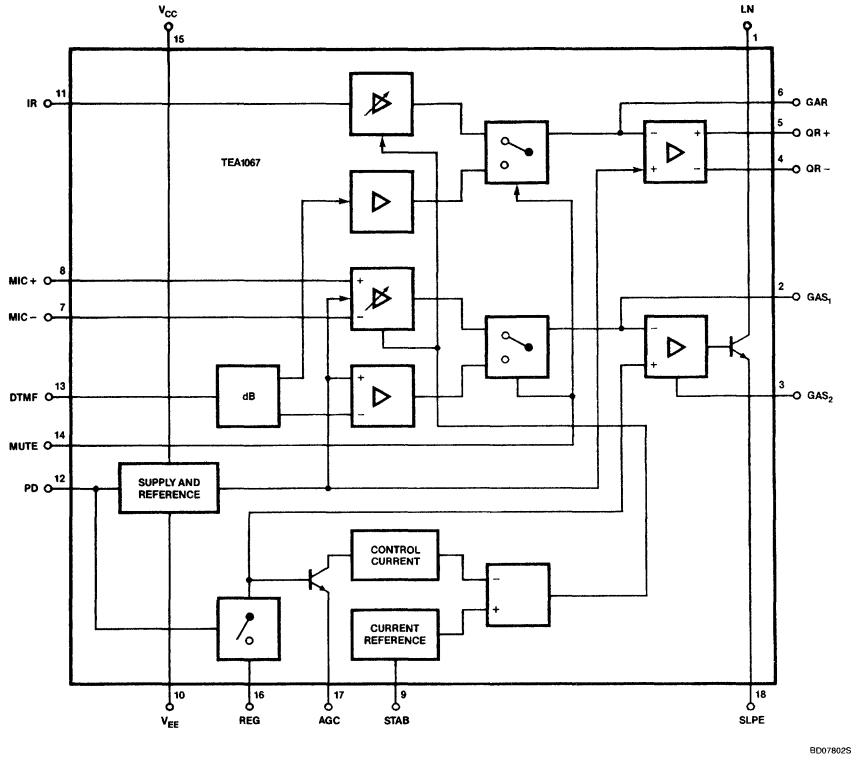
6	GAR	Gain adjustment; receiving amplifier
7	MIC–	Inverting microphone input
8	MIC+	Non-inverting microphone input
9	STAB	Current stabilizer
10	V_{EE}	Negative line terminal
11	IR	Receiving amplifier input
12	PD	Power-down input
13	DTMF	Dual-tone multi-frequency input
14	MUTE	Mute input
15	V_{CC}	Positive supply decoupling
16	REG	Voltage regulator decoupling
17	AGC	Automatic gain control input
18	SLPE	Slope (DC resistance) adjustment

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS I_{LINE} = 11 to 140mA; V_{EE} = 0V; f = 800Hz; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply: LN and V_{CC} (Pins 1 and 15)					
	Voltage drop over circuit; between Pin 1 and Pin 10 = V_{LN}; microphone inputs open				
V_{LN}	at I_{LINE}		1.6		V
V_{LN}	at I_{LINE} = 4mA	1.75	2.0	2.25	V
V_{LN}	at I_{LINE} = 7mA	2.25	2.8	3.35	V
V_{LN}	at I_{LINE} = 11mA	3.55	3.8	4.05	V
V_{LN}	at I_{LINE} = 15mA	3.65	3.90	4.15	V
V_{LN}	at I_{LINE} = 100mA	4.9	5.6	6.5	V
V_{LN}	at I_{LINE} = 140mA			7.5	V
$\Delta V_{LN}/\Delta T$	Variation with temperature at I_{LINE} = 15mA	−3	−1	1	mV/°C
	Voltage drop over circuit with external resistor R_{VA} at I_{LINE} = 15mA				
V_{LN}	R_{VA} (Pin 1 to Pin 16) = 68kΩ	3.1	3.4	3.7	V
V_{LN}	R_{VA} (Pin 16 to Pin 18) = 39kΩ	4.2	4.5	4.8	V
	Supply current I_{CC}; current into Pin 15				
I_{CC}	PD = LOW (Pin 12); V_{CC} = 2.8V		1.0	1.35	mA
I_{CC}	PD = HIGH (Pin 12); V_{CC} = 2.8V		55	82	μA
	Current available from Pin 15 to supply peripheral circuits at I_{LINE} = 15mA				
I_{CC}	$V_{CC} \geq$ 2.2V; Mute = High	1.4	1.8		mA
Microphone inputs MIC+ and MIC− (Pins 7 and 8)					
	Input impedance				
$\lvert Z_{IS} \rvert$	differential (between Pins 7 and 8)	51	64	77	kΩ
$\lvert Z_{IS} \rvert$	single-ended (Pin 7 or WRT V_{EE})	25.5	32	38.5	kΩ
CMRR	Common-mode rejection ratio		82		dB
	Voltage amplification (from Pins 7 − 8 to Pin 1) at				
A_{VD}	I_{LINE} = 15mA; R7 = 68kΩ	51	52	53	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency at f = 300 to 3400Hz	−0.5	±0.2	+0.5	dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA; T_A = −25 to +75°C		TBD		dB
Dual-tone multi-frequency input DTMF (Pin 13)					
$\lvert Z_{IS} \rvert$	Input impedance	TBD	20.7	TBD	kΩ
A_{VD}	Voltage amplification (from Pin 13 to Pin 1) at I_{LINE} = 15mA; R7 = 68kΩ	24.5	25.5	26.5	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency f = 300 to 3400Hz	−0.5	±0.2	+0.5	dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA; T_A = −25 to +75°C		±0.2		dB
Gain adjustment GAS_1 and GAS_2 (Pins 2 and 3)					
ΔA_{VD}	Amplification variation with R7 (connected between Pins 2 and 3) transmitting amplifier	−8		0	dB
Sending amplifier output LN (Pin 1)					
	Output voltage at I_{LINE} = 15mA;				
$V_{LN(RMS)}$	d_{TOT} = 2%		1.9		V
$V_{LN(RMS)}$	d_{TOT} = 10%	1.9	2.2		V
$V_{LN(RMS)}$	at I_{LINE} = 4mA; d_{TOT} = 10%		0.8		V
$V_{LN(RMS)}$	at I_{LINE} = 7mA; d_{TOT} = 10%		1.4		V
$V_{NO(RMS)}$	Noise output voltage, I_{LINE} = 15mA; R7 = 68kΩ; 200Ω between Pins 7 and 8; psophometrically weighted (P53 curve)		−72		dBmp
Receiving amplifier input IR (Pin 11)					
$\lvert Z_{IS} \rvert$	Input impedance	17	21	25	kΩ

DC ELECTRICAL CHARACTERISTICS (Continued) I_{LINE} = 11 to 140mA; V_{EE} = 0V; f = 800Hz; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Receiving amplifier outputs QR+ and QR– (Pins 5 and 4)					
$\|Z_{OS}\|$	Output impedance; single-ended		4		Ω
A_{VD} A_{VD}	Voltage amplification from Pin 11 to Pins 4 – 5 at I_{LINE} = 15mA; R4 = 1/0kΩ; single-ended; R_L = 300Ω (from Pin 11 to Pins 4 – 5) differential; R_L = 600Ω (from Pin 11 to Pins 4 – 5)	30 36	31 37	32 38	dB dB
$A_{VD}/\Delta f$	Variation with frequency, f = 300 to 3400Hz	–0.5	±0.3	+0.5	dB
$\Delta A_{VD}/\Delta T$	Variation with temperature I_{LINE} = 50mA; T_A = –25 to +75°C		±0.2		dB
$V_{O(RMS)}$ $V_{O(RMS)}$ $V_{O(RMS)}$	Output voltage at I_{CC} = 0; d_{TOT} = 2%; sine wave drive; R4 = 100kΩ single-ended; R_L = 150Ω single-ended; R_L = 450Ω differential; C_L = 47nF (100Ω series resistors); f = 3400Hz	0.25 0 45 0.65	0.29 0.55 0.80		V V V
$V_{O(RMS)}$ $V_{O(RMS)}$	Output voltage at I_{CC} = 0; d_{TOT} = 10%; sine wave drive; R4 = 100kΩ; R_L = 150Ω I_{LINE} = 4mA I_{LINE} = 7mA		15 130		mV mV
$V_{NO(RMS)}$ $V_{NO(RMS)}$	Noise output voltage I_{LINE} = 15mA, R4 = 100kΩ; Pin 11 open psophometrically weighted (P53 curve) single-ended; R_L = 300Ω differential; R_L = 600Ω		50 100		μV μV
Gain adjustment GAR (Pin 6)					
ΔA_{VD}	Amplification variation with R4 (connected between Pins 6 and 5), receiving amplifier	–11		+8	dB
MUTE input (Pin 14)					
V_{IH} V_{IL}	Input voltage HIGH LOW	1.5		V_{CC} 0.3	V V
I_{MUTE}	Input current		8	15	μA
ΔA_{VD}	Reduction of voltage amplification from MIC+ (Pin 7) and MIC– (Pin 8) to LN at MUTE = HIGH		70		dB
A_{VD}	Voltage amplification from DTMF (Pin 13) to QR+ (Pin 5) or QR– (Pin 4) at MUTE = HIGH, single-ended load R_L = 300Ω	–21	–19	–17	dB
Power-down input PD (Pin 12)					
V_{IH} V_{IL}	Input voltage HIGH LOW	1.5		V_{CC} 0.3	V V
I_{PD}	Input current (into Pin 12)		5	10	μA
Automatic gain control input AGC (Pin 17)					
A_{VD}	Controlling the gain from Pin 11 to Pins 4 – 5 and the gain from Pins 7 – 8 to Pin 1; R6 = 100kΩ (between Pins 17 and 10) amplification control range	–5.5	–5.9	–6.3	dB
A_{VD}	Reduction of gain between I_{LINE} = 15mA I_{LINE} = 35mA	–1.0	–1.5	–2.0	dB
I_{LINE}	Highest line current for maximum amplification		23		mA
I_{LINE}	Lowest line current for minimum amplification		61		mA
Peripheral supply across Pins 15 and 10					
V_{CCP}	I_P = 0mA I_P = 0.9mA I_P = 1.4mA	3.0 2.5 2.2	3.2 2.4		V V V

6

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g., dialing and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{EXCH}, the feeding bridge resistance R_{EXCH}, the DC resistance of the subscriber line R_{LINE} and the DC voltage on the subscriber set (see Figure 1).

If the line current I_{LINE} exceeds the current I_{CC} + 0.5mA required by the circuit itself ($I_{CC} \simeq 1$mA), plus the current I_{CC} required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{REF} + I_{SLPE} \times R9$$
$$= V_{REF} + (I_{LINE} - I_{CC} - 0.5 \times 10^{-3} - I_{CC}) \times R9.$$

V_{REF} being an internally-generated temperature-compensated reference voltage of 3.6V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone, maximum output swing on LN and on the DC characteristic (especially in the low voltage part). Under normal conditions $I_{SLPE} \geqslant I_{CC}$ + 0.5mA + I_{CC}. The static behavior of the circuit then equals a 3.6V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. R_{VA} (1 – 16) connected between pins LN and REG will decrease the internal reference voltage. R_{VA} (16 – 18) connected between REG and SLPE will increase the internal reference voltage.

At line currents below 9mA the internal reference voltage is automatically adjusted to a lower value (Typ. 1.6V at 1mA). This means that the operation of more telephone sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6V. At line currents below 9mA the circuit has limited sending and receiving levels.

The current I_{CC} available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 4 shows this current for $V_{CC} > 2.2$V minimum. If MUTE is LOW, the available current is further reduced when the receiving amplifier is driven. To increase the supply possibilities, the supply IC TEA1080 can be connected in parallel with R1 (Figure 9c). An alternative is to set the DC line voltage to a higher value by means of an external resistor R_{VA} (16 – 18) connected between REG and SLPE.

Microphone Inputs MIC + and MIC – and Gain Pins: GAS_1 and GAS_2

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64kΩ (2 × 32kΩ) and its voltage amplification is typ. 52dB. Either dynamic, magnetic, piezoelectric microphones or an electret microphone with built-in FET source-follower can be used.

The arrangements with the microphone types mentioned are shown in Figure 3.

The amplification of the microphone amplifier can be adjusted between 44dB to 52dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS_1 and GAS_2. An amplification more than 52dB is possible (up to 60dB); however, in that case, the spread of the DC voltage (V_{LN}) will increase and the minimum voltage at 11mA (V_{LN} = 3.55V) cannot be guaranteed. An external capacitor C6 of 100pF between GAS_1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter.

The cut-off frequency corresponds with the time constant R7 × C6.

Mute Input: MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier input; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line. In case the line current drops below 6mA (parallel operation of more sets) the circuit is always in speech condition independent of the DC level applied to the MUTE input.

Dual-Tone Multi-Frequency Input DTMF

When the DTMF input is enabled, dialing tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 25.5dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signaling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier: IR, QR +, QR – and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR + and an inverting output QR –. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Figure 4). Amplification from IR to QR + is typ. 31dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The amplification of the receiving amplifier can be adjusted between 20 and 39dB with single-ended drive and between 26 and 45dB in case of differential drive to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR + .

Two external capacitors C4 = 100pF and C7 = 10 × C4 = 1nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 × C4.

Automatic Gain Control Input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6dB. This corresponds with a line length of 5km for a 0.5mm diameter copper twisted-pair cable with a DC resistance of 176Ω/km and an average attenuation of 1.2dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Figure 5 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range. If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-Down Input PD

During pulse dialing or register recall (timed loop break) the telephone line is interrupted; as a consequence, it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typically 1mA to typically 55μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialing or register recall. When this facility is not required, PD may be left open.

Side-Tone Suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R1 Z_{LINE}, R2, R3, R8, R9 and Z_{BAL} (see Figure 8). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1(R3 + [R8//Z_{BAL}])$

b) $[Z_{BAL}/(Z_{BAL} + R8)] = [Z_{LINE}/ (Z_{LINE} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{BAL}| \ll R3$.

To obtain optimum side-tone-suppression, condition b) has to be fulfilled resulting in:

$Z_{BAL} = (R8/R1)Z_{LINE} = k.Z_{LINE}$

Where k is a scale factor; k = (R8/R1).

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{BAL}
- $|Z_{BAL}//R8| \ll R3$
- $|Z_{BAL} + R8| \ll R9$

In practice Z_{LINE} varies strongly with the line length and cable type; consequently, an average value has to be chosen for Z_{BAL}. The suppression further depends on the accuracy with which Z_{BAL}/k equals the average line impedance.

The anti-side-tone network as used in the standard application (Figure 8) attenuates the signal from the line with 32dB. The attenuation is nearly flat over the audio-frequency range. Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

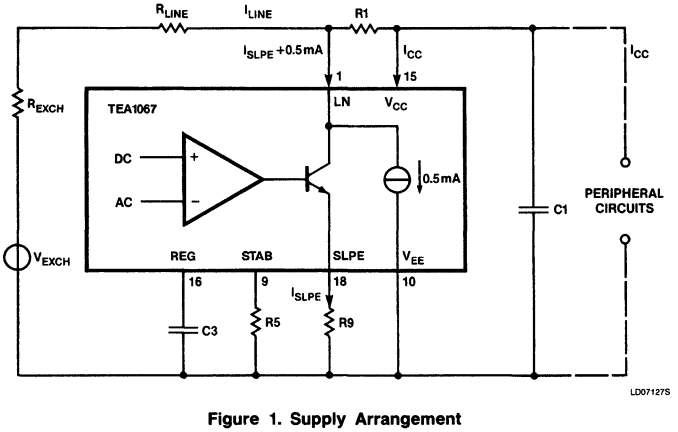
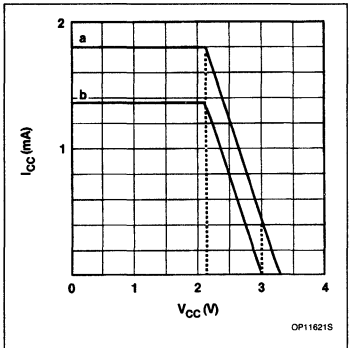


Figure 1. Supply Arrangement



NOTES:
a) = 1 8mA
b) = 1 35mA
I_{LINE} = 15mA at V_{LN} = 3 9V
R1 = 620Ω and R9 = 20Ω

Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH,
Curve (b) is valid when MUTE = LOW and the receiving amplifier is driven, $V_{O(RMS)}$ = 150mV, R_L = 150Ω asymmetrical The supply possibilities can be increased simpy by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} (16 – 18)

Figure 2. Typical Current I_{CC} Available from V_{CC} for Peripheral Circuitry with V_{CC} > = 2.2V

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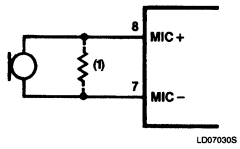
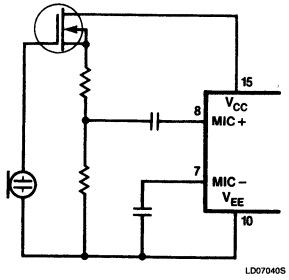
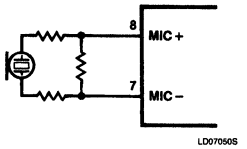


NOTE:
The resistor marked (1) may be connected to lower the terminating impedance In case of sensitive microphone types a resistor attenuator can be used to prevent overloading of the microphone inputs

a. Magnetic or Dynamic Microphone

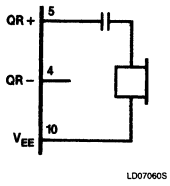


b. Electret Microphone

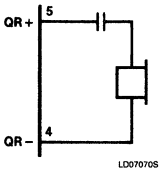


c. Piezoelectric Microphone

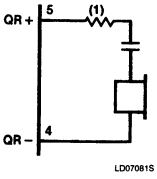
Figure 3. Alternative Microphone Arrangements



a. Dynamic Telephone With Less Than 450Ω Impedance

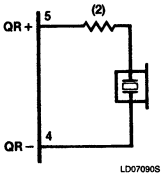


b. Dynamic Telephone With More Than 450Ω Impedance



NOTE:
The resistor marked (1) may be connected to prevent distortion (inductive load)

c. Magnetic Telephone With More Than 450Ω Impedance



NOTE:
The resistor marked (2) is required to increase the phase margin (capacitive load)

d. Piezoelectric Telephone

Figure 4. Alternative Receiver Arrangements

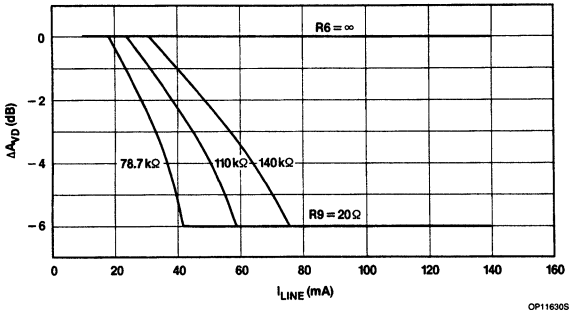
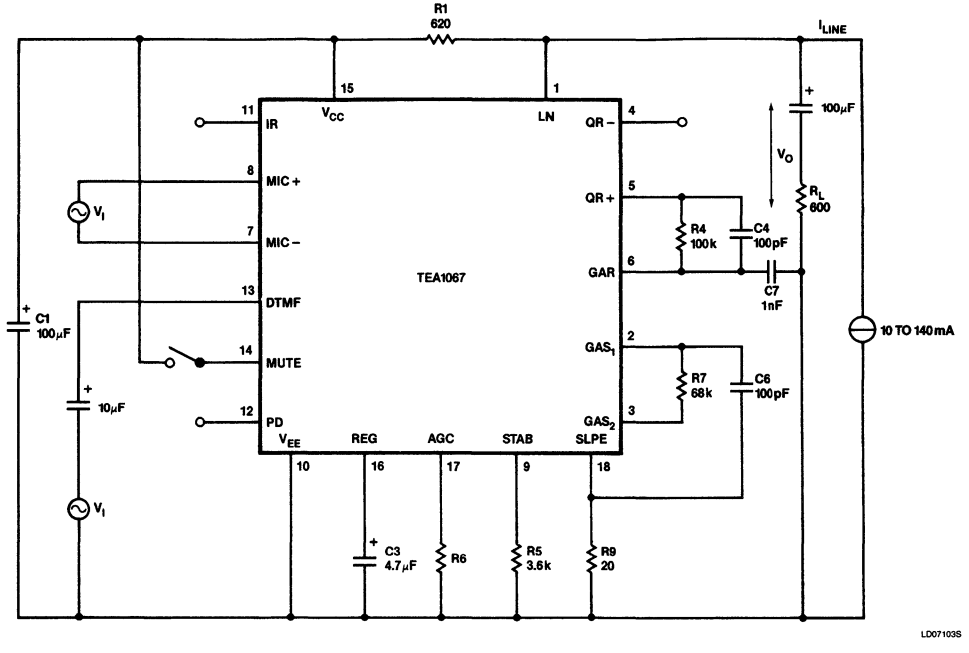


Figure 5. Variation of Amplification with Line Current With R6 as a Parameter

Table 1. Values of Resistor R6 for Optimum Line Loss Compensation, for Various Usual Values of Exchange Supply Voltage V_{EXCH} and Exchange Feeding Bridge Resistance R_{EXCH}.

		R_{EXCH} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{EXCH} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

NOTE:
R9 = 20Ω



NOTE:
Voltage amplification is defined as $A_{VD} = 20\log|V_O/V_I|$ For measuring the amplification from MIC+ and MIC−, the MUTE input should be LOW or open, for measuring the DTMF input, MUTE should be HIGH Inputs not under test should be open

Figure 6. Test Circuit for Defining Voltage Amplification of MIC+, MIC− and DTMF Inputs

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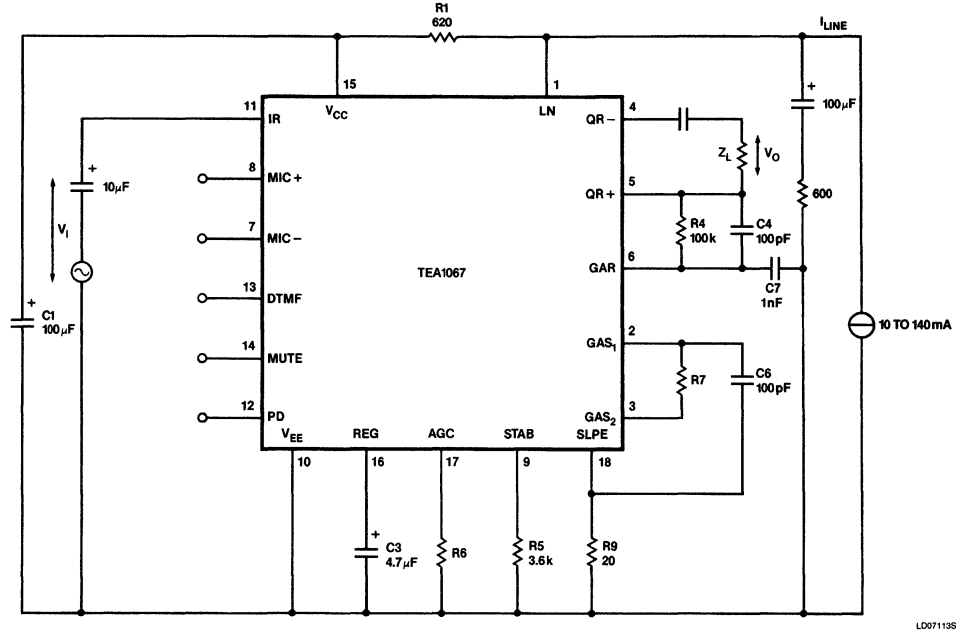
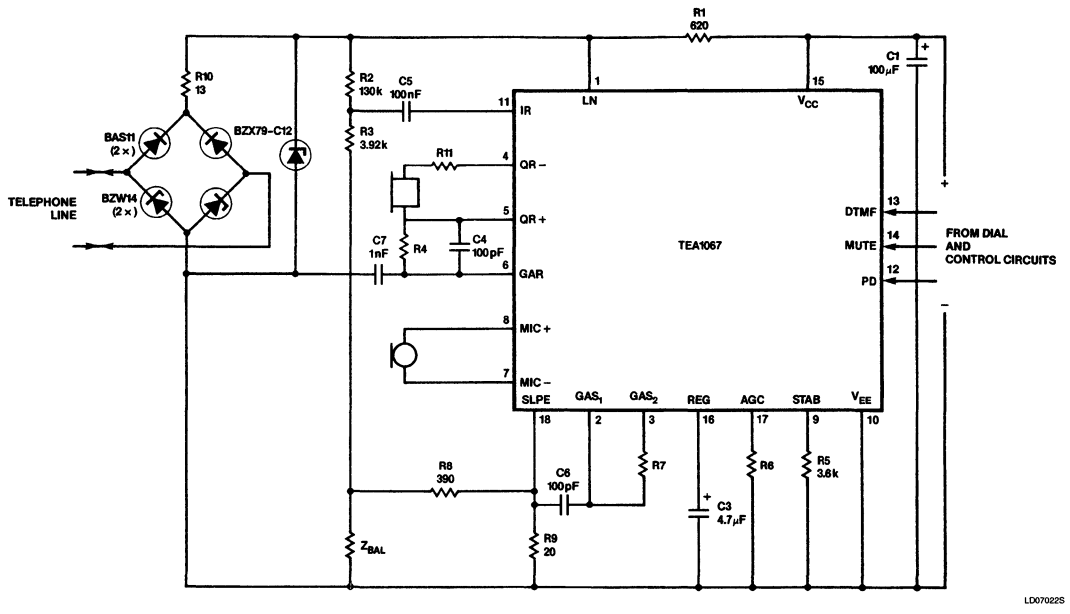


NOTE:
Voltage amplification is defined as $A_{VD} = 20\log |V_O/V_I|$

Figure 7. Test Circuit for Defining Voltage Amplification of the Receiving Amplifier



NOTE:
The bridge to the left, the zener diode and R10 limit the current and the voltage into the circuit during line transients Pulse dialing or register recall require a different protection arrangement By means of resistor (R_{16-18}) the DC line voltage can be set to a higher value.

Figure 8. Typical Application of the TEA1067, Shown Here with a Piezoelectric Earpiece and DTMF Dialing

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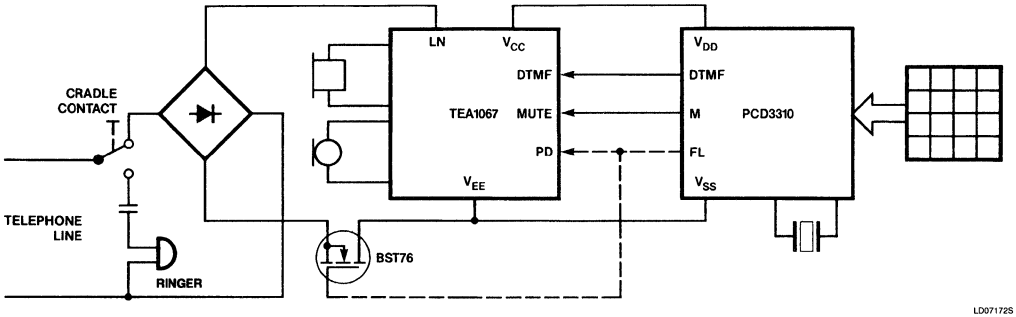
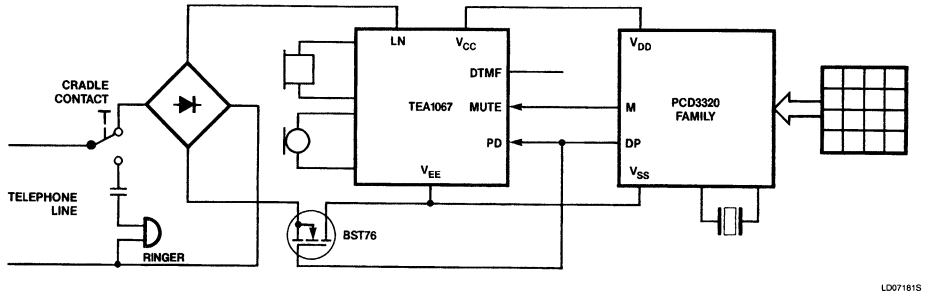
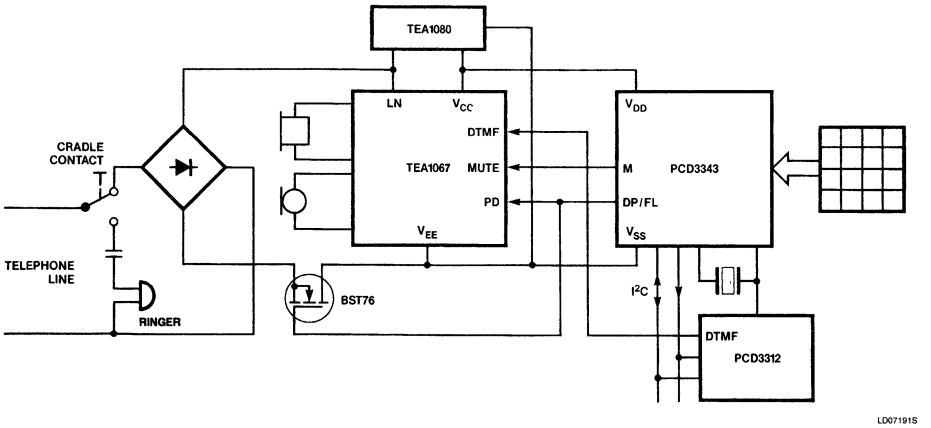


NOTE:
The dashed lines show an optional flash (register recall by timed loop break)

a. DTMF-Pulse Set with CMOS-Bilingual Dialing Circuit PCD3310



b. Pulse Dial Set with One of the PCD3320 Family of CMOS Interrupted Current-Loop Dialing Circuits



NOTE:
Supply is provided by the TEA1080 supply circuit

c. Dual-Standard (Pulse and DTMF) Feature Phone with the PCD3343 CMOS Telephone Controller and the PCD3312 CMOS DTMF with I^2C Bus

Figure 9. Typical Applications of the TEA1067 (Simplified)

AN1942
Application of the Low Voltage Versatile Transmission Circuit

Application Note

INTRODUCTION

The TEA1067 is a speech/transmission circuit for analog telephone sets. It has been developed to fulfill requirements for the North American Telephony specifications. The circuit enables parallel operation with classical telephone sets.

Additional features of the TEA1067 are as follows:

- High-ohmic microphone inputs and high gain microphone amplifier which can be adapted to every type of microphone.
- Improved receiving amplifier (high gain; low noise).
- Lower DC voltage in the normal operating range ($I_{LINE} > 11mA$). Meets USA DC requirement 6V at 20mA (RS470) with a normal diode bridge having 1.4V voltage drop.

The circuit permits fully electronic telephone sets to be designed for virtually any kind of speech transducer and set-impedance. Although the IC has been designed primarily for the increasingly-used common-line interface systems (with internal electronic switching between dialing and speech condition), it is also suitable for systems with separated speech and dialing parts (with a two-wire connection between the dialing part in the base and the speech part in the handset). It can be used with either complex or real set-impedances in either the special anti-sidetone bridge or the Wheatstone bridge configuration. All the interface functions between microphone and earphone transducers, the telephone line, and the dialing circuits are incorporated on-chip.

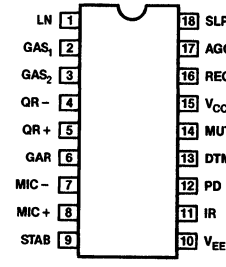
A supply connection with limited current (because of the low voltage drop across the circuit) for peripherals is provided. The supply possibilities can be extended considerably by means of a special supply IC TEA1080, or more simply by setting the line voltage to a higher value by means of an external resistor. Some alternatives to increase the supply possibilities are given. Also, a straight-forward design procedure is given to be able to adjust all necessary parameters in the most convenient order (Appendix 1).

DESCRIPTION OF THE CIRCUIT

Block Diagram

The block diagram of the TEA1067 is shown in Figure 2. The internal functions are as follows:

- Voltage regulator with low voltage drop and adjustable static resistance. The voltage drop can be adjusted externally by approximately plus or minus 0.6V.
- Low DC operating voltage; down to an absolute minimum of typical 1.6V excluding the polarity guard.
- Supply connection for driving peripheral circuits. The capabilities of the supply depend on the DC voltage setting of the voltage regulator, on external components, and on the available line current.
- Microphone amplifier with adjustable gain, and frequency roll-off with adjustable cut-off frequency.
- High-impedance symmetrical microphone inputs suitable for dynamic, magnetic, and piezoelectric microphones. Electret microphones with a source-follower or preamplifier can be connected in asymmetrical mode.
- DTMF input
- Confidence tone in the earpiece during DTMF dialing.
- Earpiece amplifier with two complementary outputs suitable for magnetic, dynamic, or piezoelectric earpieces. It has a large gain setting range and adjustable cut-off frequency.
- Line loss compensation facility dependent on line current for microphone and earpiece amplifiers. The DTMF amplifier is not affected by this facility. The control curve has been optimized for 600Ω feeding bridge and is adaptable for various exchange supply voltages.
- Mute input to inhibit the microphone and earpiece amplifier during dialing and to enable the DTMF input and confidence-tone.



PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line terminal
2	GAS1	Gain adjustment, transmitting amplifier
3	GAS2	Gain adjustment, transmitting amplifier
4	QR–	Inverting output, receiving amplifier
5	QR+	Non-inverting output; receiving amplifier
6	GAR	Gain adjustment, receiving amplifier
7	MIC–	Inverting microphone input
8	MIC+	Non-inverting microphone input
9	STAB	Current stabilizer
10	V_{EE}	Negative line terminal
11	IR	Receiving amplifier input
12	PD	Power-down input
13	DTMF	Dual-tone multi-frequency input
14	MUTE	Mute input
15	V_{CC}	Positive supply decoupling
16	REG	Voltage regulator decoupling
17	AGC	Automatic gain control input
18	SLPE	Slope (DC resistance) adjustment

Figure 1. Pin Configuration

- Power-down input to minimize the internal supply current of the IC during line interrupts, for example: during pulse dialing or register recall (flash). The voltage regulator capacitor is disconnected to prevent start-up delays after line interruptions so as to minimize the contribution of the IC to the shape of the current pulses during pulse dialing.

The anti-sidetone circuit is implemented outside the IC by means of discrete components and allows maximum flexibility of circuit design.

The pinning is shown in Figure 1 together with a list of the pin functions. These abbreviations are used throughout the chapters that follow. Figure 3 shows the basic application diagram.

Application of the Low Voltage Versatile Transmission Circuit AN1942

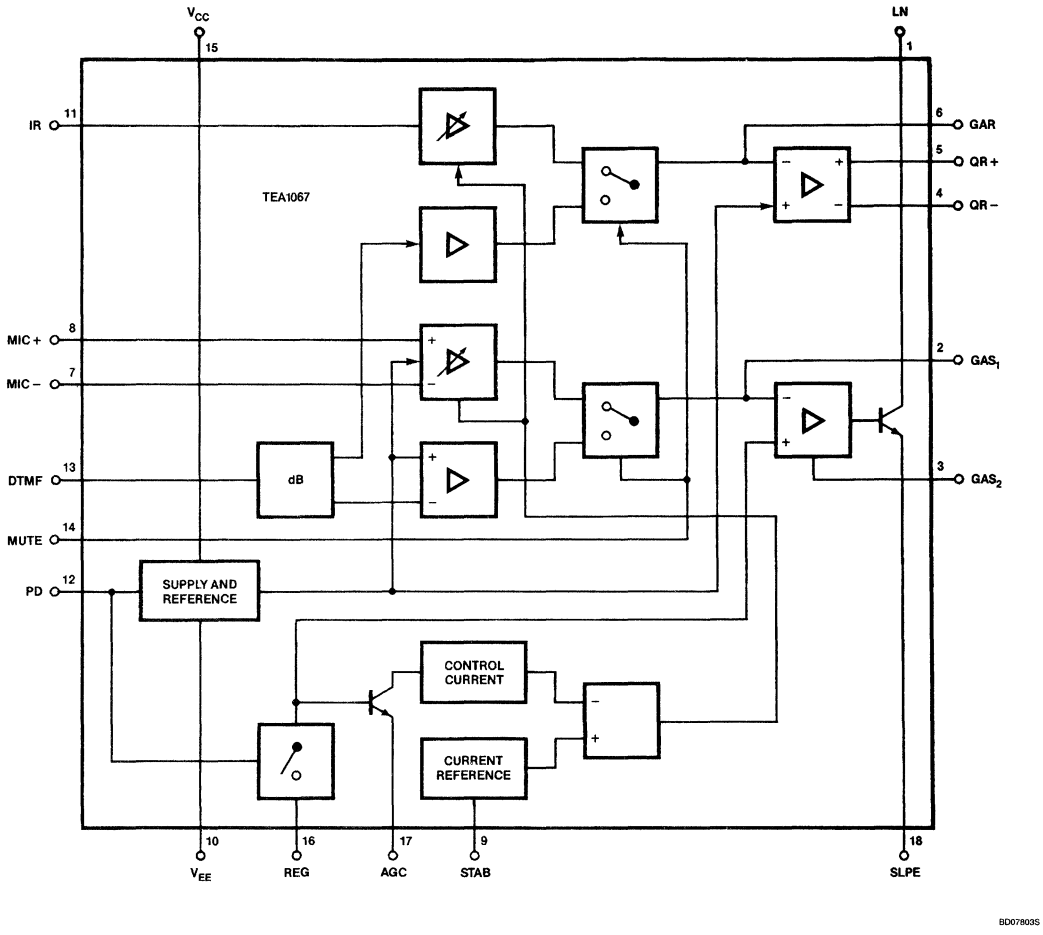
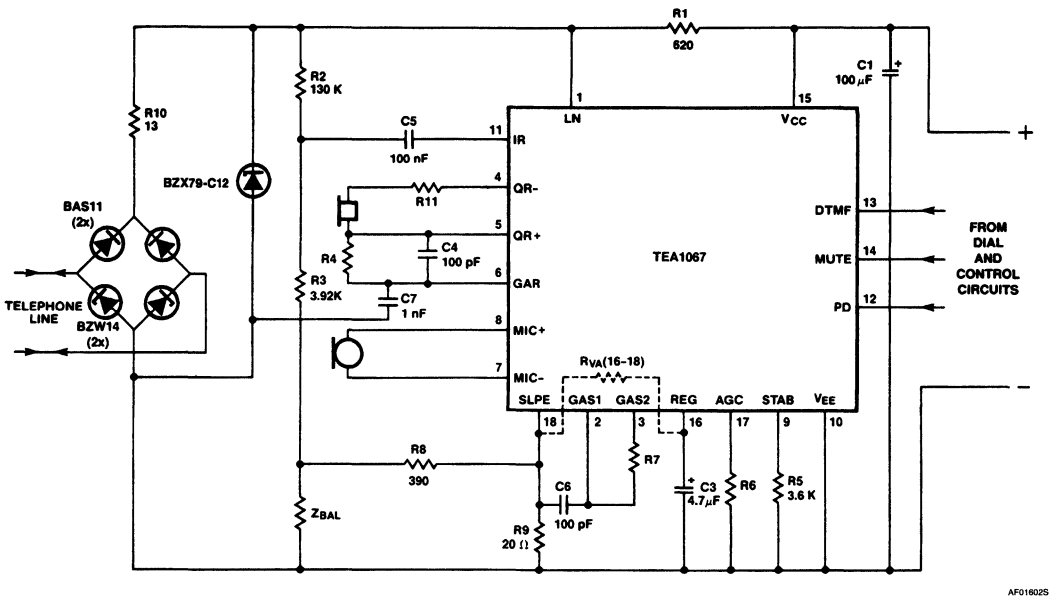


Figure 2. Block Diagram

Application of the Low Voltage Versatile Transmission Circuit AN1942



NOTE:
The Zener between Pin 1 and Pin 18 is optional and can be used to obtain symmectrical clipping of the sending signal.

Figure 3. Basic Application Diagram

Supply Considerations

Supply and Set Impedance

The IC is supplied with current from the telephone line; the general supply arrangement is shown in Figure 4. The equivalent impedance of the circuit is shown in Figure 5. The artificial inductor $L_{EQ} = R_P \cdot R_9 \cdot C_3$

With $R_9 = 20\Omega$

$C_3 = 4.7\mu F$

$R_P = 16.2k\Omega$ (internal resistor; tolerance ±20%)

This results in a typical $L_{EQ} = 1.52H$.

C_3 not only influences the value of L_{EQ}, but also determines start-up time of the DC voltage regulator. The value of C_3 has been chosen to give optimum start up time of the circuit. This means that the voltage regulator starts up after the smoothing capacitor at V_{CC} has been charged.

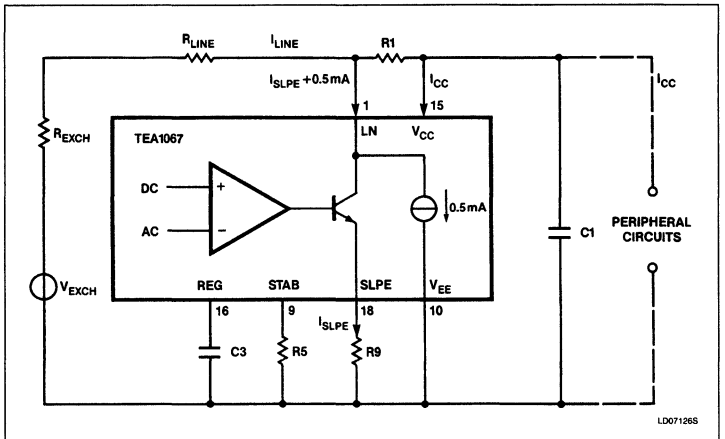


Figure 4. Supply Arrangement

Application of the Low Voltage Versatile Transmission Circuit AN1942

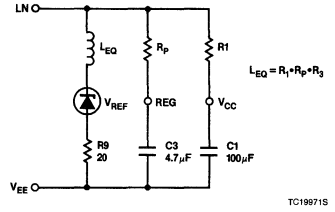
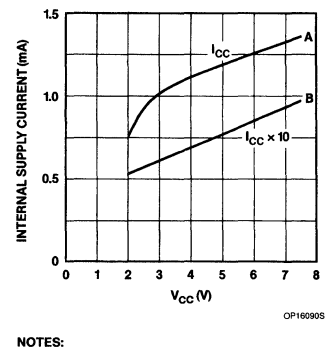


Figure 5. Equivalent Impedance

A different value for L_{EQ} can be obtained either by changing C_3 (taking into account a different start-up time) or, although not recommended, by changing the value of R_9. The latter has influence on several parameters; this will be discussed later.

In the audio frequency range, the impedance of the whole circuit is determined by R_1, or, more exactly, by the value of $R_1 \parallel R_P$.

The network R_1C_1 provides a smoothed voltage V_{CC} both for the IC itself (typical I_{CC} = 1mA at V_{CC} = 2.8V) and also for the peripheral circuits (I_P). Typical I_{CC} versus V_{CC} is shown in Figure 6; normal operating condition and power down condition are shown.



NOTES:
A Normal operating condition, PD = Low
B Power down condition, PD = High

Figure 6. Internal Supply Current $I_{CC} = f(V_{CC})$

Supply of the Integrated Circuit

The direct current which flows into the set is determined by the exchange supply voltage (V_{EXCH}), the resistance of the feeding bridge (R_{EXCH}), the DC resistance of the subscriber line (R_{LINE}) and the DC voltage across the subscriber set including the polarity guard.

If the line current exceeds the value given by (I_{CC} + 0.5mA + I_P), then the voltage regulator diverts the excess current through LN (see Figure 4).

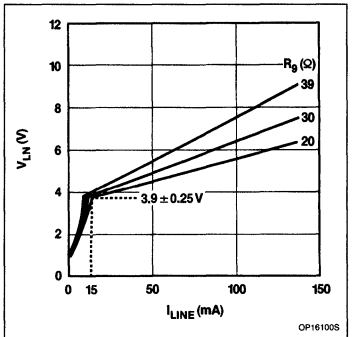


Figure 7. DC Characteristics

With line currents in excess of I_{TH}, the voltage drop across the integrated circuit is V_{LN}, where

$$V_{LN} = V_{REF} + (I_{SLPE} \cdot R_9)$$

in which V_{REF} = internal reference voltage of 3.6V
$I_{SLPE} = I_{LINE} - I_{CC} - 0.5mA - I_P$
I_{TH} = threshold current low voltage part (typ. 9mA)

The internal reference voltage is temperature-compensated, giving a low temperature coefficient of the line voltage V_{LN}; typically about −1mV/k at I_{LINE} = 15mA.

Normally $I_{SLPE} \gg I_{CC} + 0.5mA + I_P$, which means that the equivalent circuit for DC conditions, where I_{LINE} exceeds the threshold current I_{TH}, equals that of a 3.6V regulator diode in series with a resistor R_9 (see Figure 5).

The typical DC voltage V_{LN} is shown in Figure 7 as a function of line current. The slope of the graph is determined by R_9.

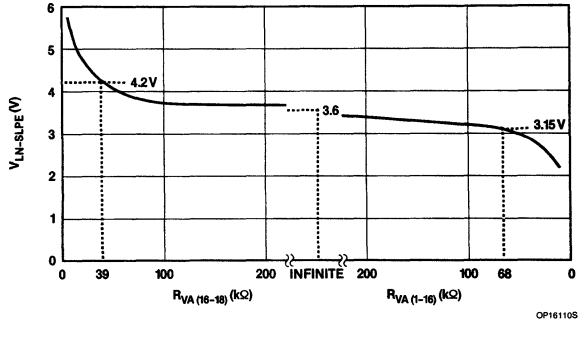
Changing R_9 — Note that R_9 also shifts the low-voltage threshold current I_{TH}. Furthermore, R_9 determines microphone gain and DTMF gain, shifts the gain-control characteristic and, in case its value exceeds 30Ω, it decreases the maximum output swing on LN (especially at high line currents and high ambient temperature). Also, the sidetone will be affected because R_9 is a branch of the anti-sidetone bridge; the bridge must be rebalanced if its value is changed. The preferred value of R_9 is 20Ω and this value is used in the basic application circuit as described in this report. However, choosing another value for R_9 can sometimes be necessary, e.g., to rebalance the anti-sidetone circuit when a set impedance different from 600Ω is chosen.

Increasing DC Slope

Increasing the slope of the DC characteristic can be done by inserting a resistor between Pin 1 (LN) and node [R_1, R_2, R_{10}] (Figure 3). This resistor does not have influence on the set impedance. However, the maximum output swing on the line is decreased slightly. Another alternative is simply increasing the protection resistor R_{10} (Figure 3).

Adjusting the DC Voltage Drop

If necessary, the voltage drop across the circuit (V_{LN}) can be increased by means of an external resistor ($R_{VA[16-18]}$) connected between Pin 16 (REG) and Pin 18 (SLPE). In fact, the external resistor R_{VA} sets the internal reference voltage $V_{REF} = V_{LN\text{-}SLPE}$ of the voltage stabilizer. This resistor causes a slightly increased spread in the voltage drop and a slightly different temperature coefficient. With $R_{VA[16-18]}$ = 39kΩ, Figure 8



NOTE:
With line currents between 11 and 140mA
DC Voltage $V_{LN} = V_{LN\text{-}SLPE} + (I_{LINE} - 1.5mA)R_9$

Figure 8. Internal Reference Voltage $V_{LN\text{-}SLPE}$ vs Resistor R_{VA}

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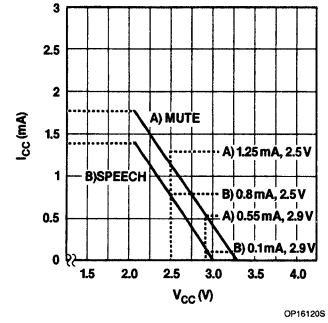
shows that $V_{REF} = 4.2V$, resulting in $V_{LN} = 4.5V \pm 0.3V$ at $I_{LINE} = 15mA$.

A decrease in the voltage drop V_{LN} can be obtained by means of an external resistor $R_{VA[1-16]}$ connected between Pin 1 (LN) and Pin 16 (REG). Figure 8 shows that with $R_{VA[1-16]} = 68k\Omega$, $V_{REF} = 3.15V$, a voltage drop $V_{LN} = 3.4V \pm 0.3V$ at $I_{LINE} = 15mA$ is obtained.

Of course, choosing a modified voltage drop across the circuit will have influence on several parameters: maximum output swing of sending and receiving amplifiers and supply current available for peripherals. Decreasing the voltage drop by means of $R_{VA[1-16]}$ will lower the set impedance slightly.

Parallel Operation

At line currents below the low-voltage threshold current I_{TH} (typically 9mA), the internal reference voltage is automatically adjusted to a lower value. At 1mA a typical voltage drop of 1.6V is obtained. This means that the operation of the circuit with more telephone sets in parallel is possible with line voltages down to an absolute minimum of typically 1.6V. Of course, the sending and receiving amplifiers have reduced gain and output swing in the low-voltage range. Furthermore, the supply point for peripherals is degraded.



NOTES:
—Speech Condition $V_{LN} = 1.4V_{RMS}$ ($d < 2\%$)
$V_{OR+} = 150mV$ across 150Ω single ended load ($d < 2\%$)
—Mute Condition $V_{LN} = 1V_{RMS}$

Figure 9. Typical Current I_{CC} Available From V_{CC} at $I_{LINE} = 15mA$; $V_{LN} = 3.9V$; $T_A = 25°C$

Supply to Peripheral Circuits

The voltage available at Pin 15 (V_{CC}) can be used to supply peripheral circuits such as pulse dialer, DTMF dialer, or a microcomputer with its own peripherals; an electret microphone with a source-follower or preamplifier can also be powered from V_{CC}.

However, the current I_{CC} and the voltage V_{CC} which are available from the circuit in the basic application (Figure 3) are limited and are dependent on the values of external components of the IC and on the actually available line current. Figure 9 shows the typical available current I_{CC} versus V_{CC} at a line current of 15mA. The typical available current and the corresponding voltage V_{CC} as a function of line current are shown in Figure 10 for the speech condition and in Figure 11 for the mute condition; parameters are the same as in Figure 9.

It is shown clearly that the lowest power is available at minimum line current. At higher values of line current, the typical values of available I_{CC} and V_{CC} are both increased. The limit on I_{CC} is then imposed by the requirement to maintain at least the minimum permitted voltage between Pin 15 (V_{CC}) and Pin 18 (SLPE) (minimum instantaneous voltage: $V_{CC} - V_{SLPE} \geq 1.5V$). In case this condition is not met, the maximum possible sending level on LN will be limited.

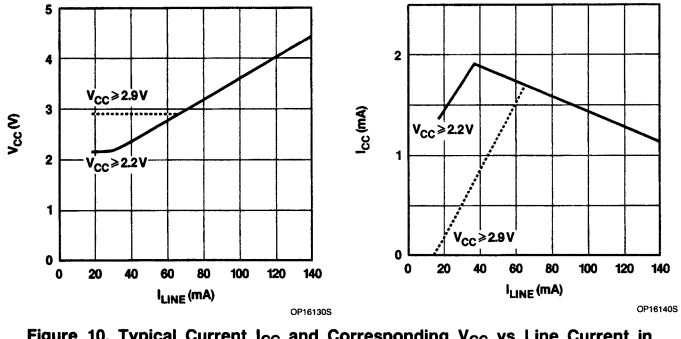


Figure 10. Typical Current I_{CC} and Corresponding V_{CC} vs Line Current in Speech Condition. Signal Conditions as in Figure 9

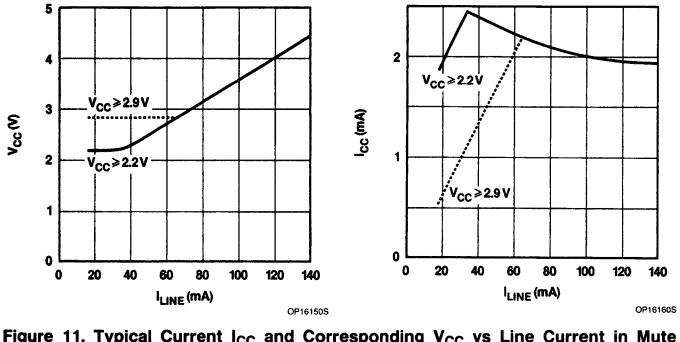


Figure 11. Typical Current I_{CC} and Corresponding V_{CC} vs Line Current in Mute Condition; Signal Conditions as in Figure 9

If the assumption is made that 15mA is the minimum line current under normal operating conditions, some figures can be given. The available current I_{CC} is determined by the minimum supply voltage required for the peripheral circuits. For most CMOS circuits the minimum supply voltage will be 2.5V. The typical available current $I_{CC} = 1.25mA$ at $V_{CC} = 2.5V$; worst-case $I_{CC} > 0.9mA$. In speech condition, the available current depends strongly on the received signal level because of the class-B receiving amplifier output stage; with an extremely high and continuous drive of the receiving amplifier, the available current will be typically 0.8mA. In practice, however, the receiving amplifier will not be driven continuously and the available supply current will be higher under normal speech conditions. This means that the power available from the supply point in the standard application is sufficient for low-power circuits such as pulse dialers and preamplifiers for electret microphones. Most CMOS DTMF dialers can be powered under typical conditions; however, under worst-case conditions of both TEA1067 and tone dialer, the available power may not be sufficient.

In cases where a battery is used for memory retaining, an enable diode will become necessary between V_{CC} and the power pin of the

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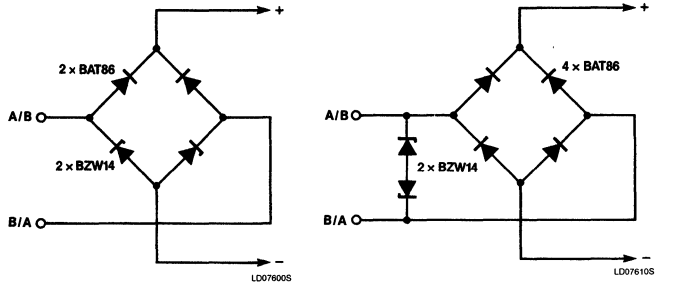
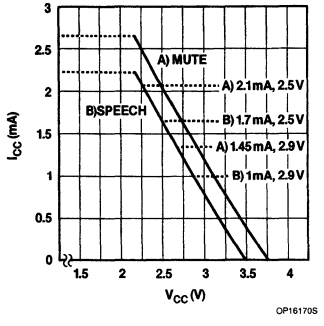


NOTES:
a 4-Diode Solution typ 0.5V Less Drop
b 6-Diode Solution typ 1V Less Drop

Figure 12. Schottky Diode Polarity Guard With Protection Giving Less Voltage Drop Than a Normal 1.4V Polarity Guard



NOTE:
Signal conditions as in Figure 9

Figure 13. Typical Current I_{CC} Available From V_{CC} at I_{LINE} = 15mA With Increased Line Voltage by Means of $R_{VA[16-18]}$ = 39kΩ

peripheral circuit to prevent discharge of the battery. Taking into account a voltage drop for a Schottky enable diode (BAT85· $V_F < 0.32V$ at 25°C and 1mA), the minimum value of V_{CC} we need is about 2.9V. This results in a typical available current of 0.55mA in mute condition (worst case I_P = 0.2mA). This is not sufficient to power a microcontroller and a DTMF dialer (e.g., PCD3315 and PCD3312) simultaneously. Several possibilities to improve the supply of the TEA1067 are given in the following paragraph. In AN1943 a separate overview is given to solve the supply problem of TEA1067 and still meet the RS470 requirements at the same time.

Extending the Supply Possibilities
Several methods exist to extend the supply possibilities. All of them have advantages and also disadvantages. These methods are discussed below.

Increasing the Line Voltage — In cases where this is allowed, the supply problems can be overcome simply by setting the voltage drop across the circuit to a higher value. Of course, the line voltage is also increased then. If a higher line voltage is not allowed (e.g., requirement RS470), this can be corrected in sets with DTMF dialing only (without flash) by using a polarity guard with Schottky diodes resulting in a lower voltage drop across the polarity guard. This is shown in Figure 12. More information can be found in AN1943.

Increasing the voltage drop across the circuit can be obtained by means of an external resistor $R_{VA[16-18]}$. With $R_{VA[16-18]}$ = 39kΩ the typical available I_{CC} and V_{CC} are shown in Figure 13 with V_{LN} = 4.45V and I_{LINE} = 15mA. Taking into account the spread on the voltage drop V_{LN}, it can be calculated that the minimum available power is I_{CC} = 1.1mA at V_{CC} = 2.9V and 1.75mA at V_{CC} = 2.5V in mute condition.

An alternative way to meet the requirements of RS470 is to increase the line voltage into the conditionally acceptable region at the moments when this is allowed. The voltage is switched back into the acceptable region in those cases where this is required; e.g., during pulse-dialing and during the hook-on to hook-off transition. This is described extensively in AN1943.

Compromise Between Set Impedance and Supply — The TEA1067 gives a very good balance return loss (BRL) with respect to a 600Ω reference impedance. In cases where the margin with respect to the requirements for BRL is rather high, it is possible to reduce the AC set impedance to such a value that the BRL requirement still is fulfilled safely. In this way a considerable increase of the supply possibilities is obtained.

Figure 14 shows the typical available supply current with V_{CC} = 2.9V and V_{CC} = 2.5V as a function of R_1 in mute condition with I_{LINE} = 15mA and V_{LN} = 3.9V. Furthermore, Figure 15 shows the measured BRL-figures at

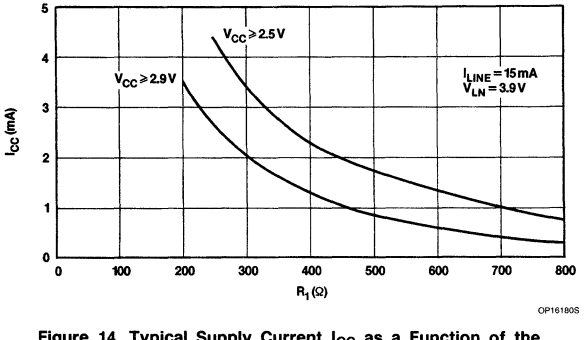


Figure 14. Typical Supply Current I_{CC} as a Function of the Supply Resistor R_1 (in Mute Condition)

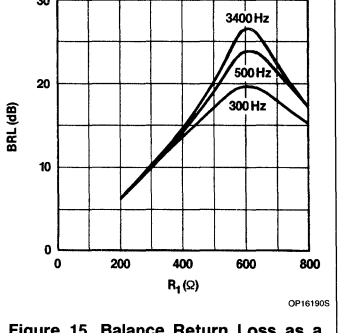


Figure 15. Balance Return Loss as a Function of R_1

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300Hz, at 500Hz, and at 3400Hz as a function of R_1.

Note that lowering of R_1 will have influence also on sending gain (microphone and DTMF), on the maximum possible sending signal on the line at low line currents, and on the balancing of the anti-sidetone bridge. The sending gain normally can be corrected easily. The following section on Anti-Sidetone Circuits shows how the anti-sidetone bridge can be rebalanced by decreasing R_9 or R_2.

RC Smoothing Filter Between LN and SLPE — For relatively small supply currents, an RC filter between Pin 1 (LN) and Pin 18 (SLPE) can be used to power peripherals. An advantage of this method is that the internally-generated reference voltage is used, which is rather constant (temperature compensated) and has a relatively low spread. Furthermore, no influence is to be expected on set-impedance (BRL), sending gain, and on the gain control characteristics.

This configuration is shown in Figure 16. With $R_{L1} = 300\Omega$, $C_{R_L} = 220\mu F$ and $I_{R_L} = 2mA$, the supply voltage across the peripheral load R_{L_2} measures about 3V ±0.25V.

A disadvantage is that a higher line current is necessary for the same output swing of the transmit output stage on the line, because of the dissipation of the AC signal in R_{L_1}.

Furthermore, a problem is that the TEA1067 and the peripherals do not have a common reference. The reference used for the peripherals is SLPE; the TEA1067 reference is V_{EE}. This means that level shifters are necessary between the logical inputs Pin 14 (MUTE) and Pin 12 (PD) of the TEA1067, and the logical outputs of the peripheral IC's. Furthermore, a small correction factor (normally around 1dB) for the total DTMF gain is introduced.

Inductor in Parallel With R_1 — If the above described methods cannot be used, a supply arrangement as shown in Figure 17 is possible. An inductor in parallel with R_1 extends the supply possibilities. The value of this inductor must be more than 2.5H in order not to influence the BRL-figures much. In practice a BRL ≥ 20dB at f = 500Hz can be realized. The maximum series resistance of the inductor depends on the maximum current I_P and the minimum required voltage V_{CC}. For example, with $V_{CC} \geq 3.5V$ and $I_P \geq 3mA$, the maximum series resistance of the inductor is $R_L = 180\Omega$. However, to avoid the need for an excessively large and expensive inductor, an electronic solution is more favourable for currents I_P in excess of about 3mA. Also, for currents less than 3mA an electronic solution can be used in case a discrete inductor is not desirable.

Electronic Inductor — The TEA1080 special supply circuit comprising an artificial inductor (about 10H) can be used in combination with the TEA1067 to extend the supply possibilities to very high values, depending on the available line current and line voltage. This combination is very suitable for listen-in and handsfree applications where a relatively large power is needed.

In this report two possible combinations of TEA1060 and TEA1080 are described: the TEA1080 is either connected between LN and the common reference V_{EE} or between LN and a different reference SLPE Both methods have their own merits.

An electronic inductor can also be realized by means of off-the-shelf components (e.g., op amp TCA520 + 3 resistors + 2 capacitors + 2 transistors + 1 diode); this is shown in Figure 18.

Parallel Operation With a Classical Set — In case a classical telephone set is connected in parallel with the TEA1060/61/66T/68 on a loop with low line current, the line voltage will drop below the zener voltage of the voltage stabilizer of the transmission circuit For example, with a 200Ω classical set on a 20mA loop the line voltage will drop to about 3.8V; this means that the voltage inside the polarity guard will be about 2 6V. The TEA1067, however, automatically decreases its zener voltage in case the current coming from the line drops below the threshold current I_{TH} (typ. 9mA) This means that the transmit output stage will operate down to very low voltages. For example, with the 200Ω classical set connected in parallel to a TEA1067 with 20mA available line current, the line voltage will drop to 3.2V leaving 4mA of line current for the TEA1067 at a voltage of 2V at the power pin of the TEA1067 inside the polarity guard. We assumed that the current used for the peripherals can be neglected at such a low voltage (V_{CC} has a value around 1.6V); this means that in sets containing a microcontroller and battery, the controller will run on the battery; in basic tone dial sets the DTMF dialer will be in an unspecified condition and normally this is a low-power stand-by condition as long as no key is pressed. In case a key is pressed, normally distorted dial tones are generated.

In sets where peripherals are connected to V_{CC} that also consume current under low-voltage conditions, this will cause worse performance of the TEA1067 during parallel operation under minimum conditions, unless the peripherals are switched into a low-power condition in case the line voltage drops below a predetermined value.

Microphone Amplifier

The TEA1067 has symmetrical high impedance microphone inputs. The input impedance is typically 64kΩ (2 × 32kΩ) with tolerances of ±20%. With this high input impedance it is possible to determine the matching of several microphone types very accurately by means of external components. The circuit is suitable for dynamic, magnetic, or piezo-electric microphones with symmetrical drive; electret microphones with built-in source follower or preamplifier can be used in asymmetrical mode.

To obtain optimum noise performance, the microphone inputs must be loaded. The equivalent noise-voltage (psophometrically weighted; P53-curve) at the microphone input is typically $0.65\mu V_{(RMS)P}$ with 8.2kΩ across the microphone inputs. With 200Ω across the

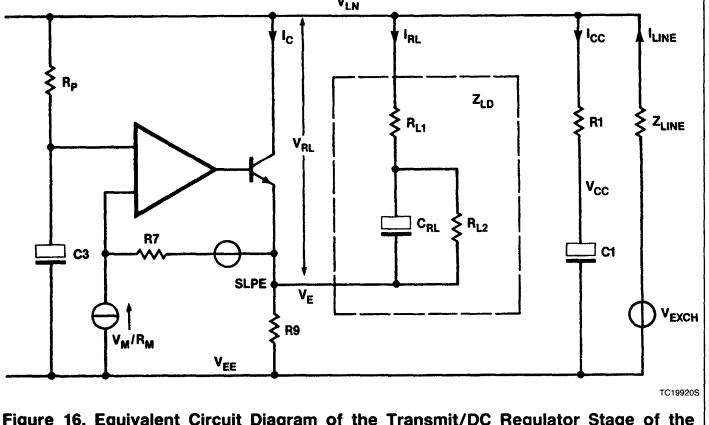

Figure 16. Equivalent Circuit Diagram of the Transmit/DC Regulator Stage of the TEA1067 With Supply Part Connected Between LN

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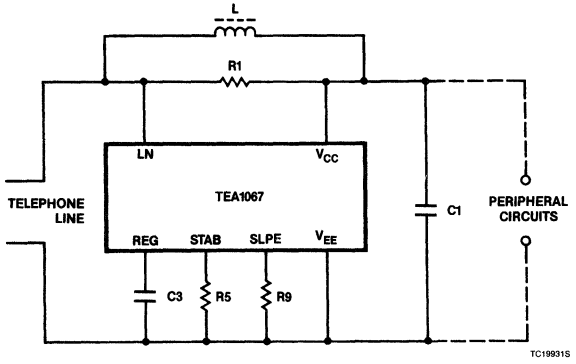


Figure 17. Increased Supply Capability by Means of an Inductor in Parallel With R_1

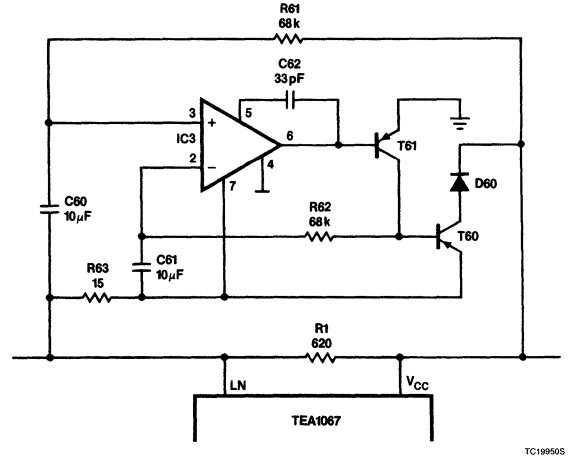


Figure 18. Circuit Diagram of an Electronic Inductor Realized With Off-the-Shelf Components

inputs, the equivalent noise at the input measures typically $0.45\mu V_{(RMS)P}$.

The internal microphone preamplifier accepts signals up to $17mV_{RMS}$ for a 2% level of total harmonic distortion (d_{TOT} = 2%) because of the internal soft limiting. This means that the minimum possible gain of the microphone amplifier measured between the inputs and the line is 44dB with clipping of the line signal being determined fully by the transmit output stage. In case a lower gain is necessary, the input signal must be attenuated before entering the preamplifier; otherwise, the input stage will be overloaded and cause extra distortion (soft clipping) of the line signal. The arrangements with several microphone types are shown in Figure 19.

In case asymmetrical drive of the microphone inputs is used, care should be taken that both inputs MIC+ and MIC− see equal impedances to the common, otherwise, residual line signals present on the supply point (V_{CC}) will cause inaccuracy in gain, and sometimes (with a large DC-blocking capacitor connected to MIC−) even low-frequency hicking (motorboating) may occur.

The gain of the microphone amplifier is given by the following equation (see Figure 3):

$$A_m = 1.356 \times \frac{R_7 + r_D}{R_5\, R_9} \times \frac{R_I\, R_L}{R_I + R_L}$$

where,

$R_I = R_1 \| 16.2k\Omega$, the dynamic impedance of the circuit R_L = load resistance at LN during the measurement; normally 600Ω.

r_D = dynamic resistance of the internal circuitry (3.47kΩ)

R_5 = 3.65kΩ, fixed external resistor determining the current in an internal current stabilizer

If, for a practical circuit such as shown in Figure 3, we insert in the above equation the following realistic values: R_7 = 68.1kΩ, R_5 = 3 65kΩ, R_9 = 20Ω, R_1 = 620Ω, and R_L = 600Ω, then: $20\log A_m$ = 52 ± 1dB.

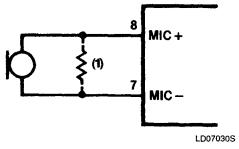
For various microphone sensitivities, the gain can be set between 44dB and 52dB by means of R_7; this takes values between 25kΩ and 68.1kΩ . The microphone gain is shown as a function of R_7 in Figure 20. An amplification of more than 52dB is possible (up to a maximum of 60dB); however, in that case the minimum specified DC voltage of V_{LN} at 11mA ($V_{LN} \geqslant 3.55V$) cannot be guaranteed any more. Also, the specified DC voltages at 7mA and 4mA will show more spread. This is caused by the internal offset voltage of the microphone input stage, which causes an offset onto the low-voltage threshold current of the DC characteristic. The effect of this offset depends on the microphone gain that has been set by means of R_7. With a microphone gain of 52dB (R_7 = 68.1kΩ) and a standard deviation (sigma) of the offset voltage of the input stage of ± 0 5mV, it can be calculated that the threshold current I_{TH} is between about 7 and 11mA (3*sigma). The DC voltage at 11mA is specified to guarantee that the DC voltage in the normal operating range (I_{LINE} > 11mA) is not influenced by this spread with a microphone gain of 52dB.

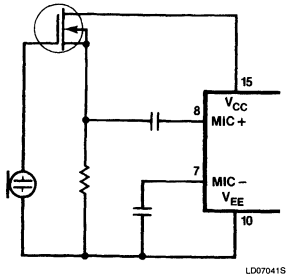
It will be clear that any different choice of R_9 (static resistance of the DC characteristic) will directly influence the gain of the transmitting channel. The value of R_9 also has influence on the DC characteristic (slope, I_{TH}), the gain control characteristic, and on the maximum output swing on the output pin LN. Also, the balancing of the anti-sidetone circuit will be affected, necessitating rebalancing of the bridge.

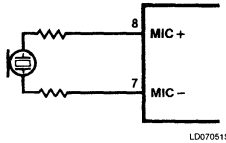
The value used in the basic application diagram is 20Ω If this value is to be changed, the consequences should be considered carefully and the design procedure as given in Appendix 1 must be followed

In case the line current is sufficient, clipping of the output signal at Pin 1 (LN) normally happens when the internal output transistor saturates

($V_{LN} - V_{SLPE}$ = 0 9V)







NOTE:
The resister marked (1) may be connected to lower the terminating impedance

a. Magnetic or Dynamic Microphone **b. Electret Microphone** **c. Piezoelectric Microphone**

Figure 19. Alternative Microphone Arrangements

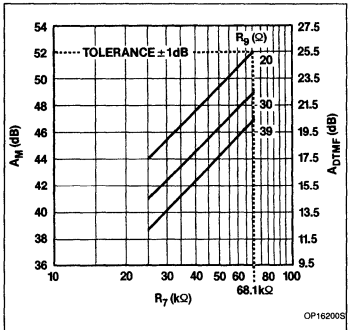


Figure 20. Microphone Gain and DTMF Gain as Function of R_7

This means that the sine wave clips at the bottom. The top of the sine wave can only be clipped by the zener diode at Pin 1 (LN) or by lack of collector current in the output transistor (low line current).

At low line currents, the top part of the output sine wave is clipped because the output stage runs out of current.

In case of sufficient line current, symmetrical clipping at the line output LN can be obtained by using a 6.8V zener diode between LN (Pin 1) and SLPE (Pin 18) of the TEA1067 (Figure 3).

In Figure 21 the maximum output swing of the transmit output stage is shown as a function of the DC line voltage V_{LN} at I_{LINE} = 15mA.

Stability and Frequency Roll-off.
The 100pF external capacitor C_6 connected between GAS1 and SLPE is necessary for ensuring the stability of the transmitting amplifier. Larger values can be applied, and these will then operate as a first-order low-pass filter, for which the cut-off frequency is determined by the time constant R_7C_6. This gives f_{3dB} = 23kHz with R_7 = 68.1kΩ and C_6 = 100pF.

Parallel Operation
In case of parallel operation of sets, the operating voltage of the TEA1067 can drop below the internal reference voltage and the circuit automatically adjusts this voltage to a lower value. Of course, this will have influence on the performance of the microphone amplifier.

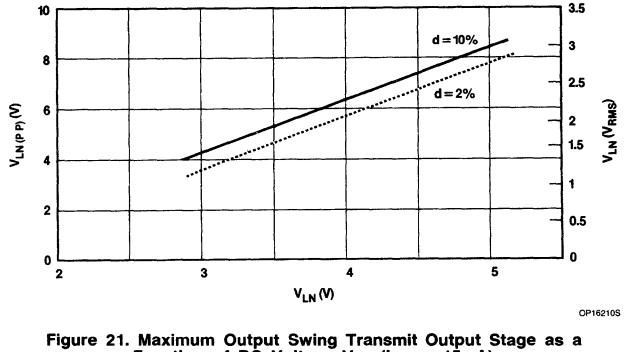


Figure 21. Maximum Output Swing Transmit Output Stage as a Function of DC Voltage V_{LN} (I_{LINE} = 15mA)

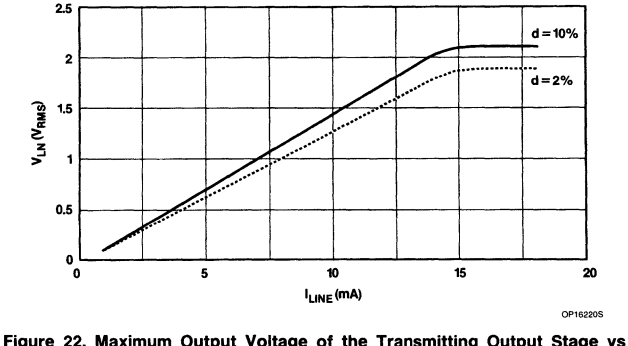


Figure 22. Maximum Output Voltage of the Transmitting Output Stage vs I_{LINE} in Low Line Current Range

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In Figure 22 the maximum output voltage at Pin 1 (LN) is shown with a 300Ω AC load (the resistor determining the set impedance R_1 = 600Ω is in parallel with the 300Ω) as a function of line current that is actually flowing into the TEA1067. This represents one telephone set with a 600Ω AC impedance being connected in parallel with the TEA1067 (600Ω load representing the telephone line being already present). Transmit gain is 52dB in case of a normal 600Ω load; however, with a 600Ω set in parallel, gain decreases with about 3.5dB. The maximum output swing is not determined by the DC voltage at Pin 1, but by the available current in the output stage of the TEA1067.

In Figure 23, the transmit gain versus the DC voltage at Pin 1 (LN) is shown. Gain decrease starts at V_{LN} = 2.2V. At V_{LN} = 2V, the decrease is about 2-3dB and about 12dB at V_{LN} = 1.6V.

The results given are valid for a typical sample in the basic application circuit of Figure 3. Changing component values will influence the results.

DTMF Amplifier

A dual-tone multi-frequency dialing signal can be applied to the IC through the DTMF input at Pin 13. Input impedance is typically about 20kΩ. The voltage gain measured between the DTMF input and the transmitter output at LN is 26.5dB less than that of the microphone amplifier. Thus:

$$20 \log A_{DTMF} = 20 \log A_m = 26.5dB$$

The DTMF gain depends on the values of R_1, R_5, R_7, R_9, and R_L in the same way as the microphone gain (see Figure 20). Thus, the choice of gain to suit one particular microphone capsule will also predetermine the DTMF gain. The dialing tones must, therefore, be adjusted to the appropriate level before they are applied; the DTMF input accepts

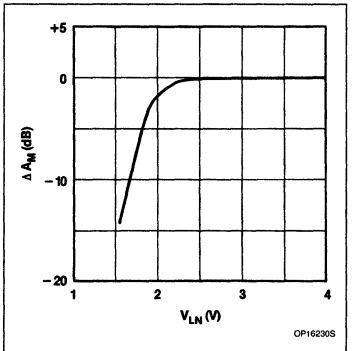

Figure 23. Typical Transmit Gain vs DC Voltage V_{LN} in Low Voltage Range

signals up to 170mV$_{RMS}$ for d_{TOT} = 2% with internal soft limiting of the input stage.

The coupling network between the DTMF generator PCD3311/12 and the transmission circuit is very simple. For further information on this application, contact factory.

Temperature Dependency

The DTMF amplifier is internally temperature compensated. However, because of the asymmetrical input structure (single-ended drive), some influence can be expected from the residual AC line voltage being present on the supply pin V_{CC}. The low-pass filter R_1C_1 provides a smoothed supply voltage V_{CC}. The small residual line voltage being present on V_{CC} depends on the performance of the components of the low-pass, especially the electrolytic capacitor C_1. This means that the temperature dependency of the capacitor C_1 has some influence on the DTMF gain via an internal feedback mechanism; therefore, an electrolytic capacitor with low temperature coefficient should be chosen.

The temperature dependency of DTMF gain was measured in the basic application circuit of Figure 3 with a 100μF, 25V capacitor. The following typical values with respect to 25°C were found:

−0.5dB at −25°C
+0.2dB at +70°C

Receiving Amplifier

The input of the receiving amplifier is Pin 11 (IR). Input impedance is approximately 20kΩ. The amplifier has two complementary Class B outputs — the non-inverting output QR+ at Pin 5, and the inverting output QR− at Pin 4. The outputs can be used either for single-ended drive or for symmetrical drive, depending on the impedance, sensitivity, and type of earpiece used.

It can drive either dynamic, magnetic, or piezoelectric earpieces as shown in Figure 24. Earpieces with an impedance up to 450Ω must be driven in single-ended mode (low-impedance dynamic or magnetic capsules). This is shown in Figure 24a. For impedances above 450Ω, with a high-impedance dynamic, magnetic, or piezoelectric capsule, differential drive is possible, as shown in Figure 24b, c, d. The additional series resistor (1) shown in Figure 24c in case of a magnetic capsule can be used to prevent distortion of the output signal when the output stage is deficient in available current (causing a dI/dt in an inductive load). To preserve stability with a piezoelectric earpiece, the series resistor (2) is required as shown in Figure 24d, as this type of transducer represents a capacitive load.

Capacitive loading of the receiving output stage is permitted up to a maximum of 100nF between QR+ and QR−. However, the decrease of phase margin (could give lead to instabilities) must be restored by means of the series resistor $R_{(2)}$ (for example, with C_L = 100nF, $R_{(2)}$ = 50Ω).

With an asymmetric load, the gain A_{TA} of the receiving amplifier, measured between the input IR and the output QR+, is given by (see Figure 3):

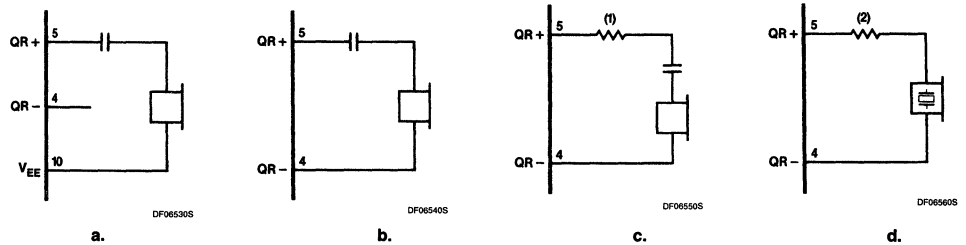

Figure 24. Alternative Earphone Arrangements

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$$A_{TA} = 0\,657 \times \frac{R_4}{R_5} \times \frac{Z_T}{Z_T + r_O}$$

Where, Z_T = earpiece impedance
r_O = output impedance of the receiving amplifier (typically 4Ω).

If we insert the values $R_4 = 100k\Omega$, $R_5 = 3.65k\Omega$, and $Z_T = 450\Omega$, the following results:

$20\log A_{TA} = 31dB \pm 1dB$.

With both outputs QR+ and QR– being used in symmetrical mode, the gain A_{TS} is increased by 6dB and is given by:

$$A_{TS} = 1.314 \times \frac{R_4}{R_5} \times \frac{Z_T}{Z_T + r_O}$$

This results with the values for R_4, R_5, and Z_T which were used above in:

$20\log A_{TS} = 37dB \pm 1dB$.

The gain of the receiving amplifier can be adjusted by means of R_4 between 20dB and 39dB with single-ended drive, and between 26dB and 45dB in case of differential drive This takes values of R_4 between 28kΩ and 250kΩ. The gains A_{TA} and A_{TS} together with the confidence tone as a function of R_4 are shown in Figure 25.

The maximum output swing of the receiving output stage(s) versus DC line voltage V_{LN} is shown in Figure 26 at $I_{LINE} = 15mA$.

The signal received on the line is attenuated by the anti-sidetone network before it enters the input IR of the receiving amplifier. In the basic application circuit (Figure 3) this attenuation is about 32dB. Frequency response between the line and the input IR is almost flat in the audio frequency range when using the special TEA1060 family bridge configuration.

The signal at the input IR of the amplifier is internally limited by symmetrical soft limiting to $17mV_{RMS}$ for $d_{TOT} = 2\%$ and to $53mV_{RMS}$ for $d_{TOT} = 10\%$.

The equivalent noise at the input IR of the receiving amplifier (psophometrically weighted; P53-curve) is typically $1.25\mu V_{(RMS)P}$. With the anti-sidetone circuit connected to the input, the noise generated at the line pin LN will add via the anti-sidetone circuit to the equivalent input noise of the receiving amplifier. The total noise generated at the earpiece output depends on microphone gain that has been set and on the actual sidetone suppression; furthermore, extra circuitry connected to pin LN (for example, an artificial inductor to extend supply possibilities) can give a noise contribution.

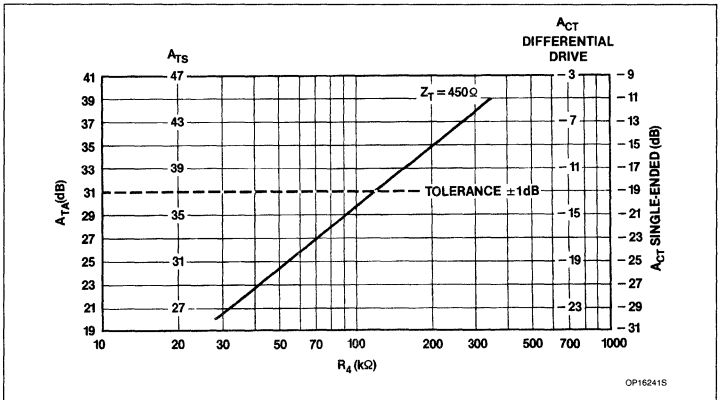

Figure 25. Gain of Receiving Amplifiers A_{TA} and A_{TS} and Confidence Tone A_{CT} Against the Value of R_4

Stability and Frequency Roll-off

Stability is ensured by the use of two discrete capacitors C_4 and C_7 in Figure 3. Capacitor C_4 is connected between QR+ and GAR, and capacitor C_7 is connected between GAR and V_{EE} The value of C_7 is recommended to be ten times greater than that of C_4, and the values are generally $C_4 = 100pF$ and $C_7 = 1nF$ A larger value of C_4 may be chosen so as to obtain a first-order low-pass frequency characteristic, the cut-off frequency being determined by the time-constant R_4C_4. In this case, the ratio of 10·1 for $C_7.C_4$ must be preserved. With $C_4 = 100pF$ and with $R_4 = 100k\Omega$, the cut-off frequency $f_{3dB} = 16kHz$

Parallel Operation

Similar to the microphone amplifier, the possibilities of the receiving amplifier will be decreased under low voltage conditions occuring during parallel operation of sets. Figure 27 shows the maximum output swing of the receiving amplifier ($d_{TOT} = 10\%$) versus the line voltage V_{LN} with different loads in the low voltage part The maximum output swing naturally decreases with the DC voltage at LN. At $V_{LN} = 2V$, typically an output swing of $15mV_{RMS}$ with a 150Ω load can be obtained At about 1.6V, the receiving amplifier is totally cut off.

Figure 28 shows the receive gain as a function of the DC line voltage V_{LN}. Gain decrease starts at about $V_{LN} = 3V$; at $V_{LN} = 2V$, the gain has been decreased by about 13dB

The results are valid for a typical sample in the basic application circuit of Figure 3. Changing components will have influence on the results.

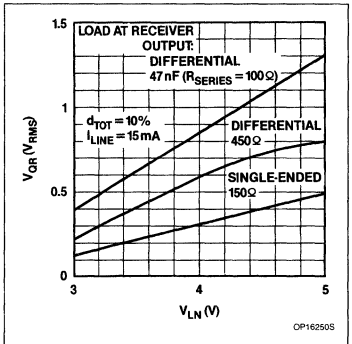

Figure 26. Maximum Output Swing Receiving Amplifier vs DC Voltage V_{LN}

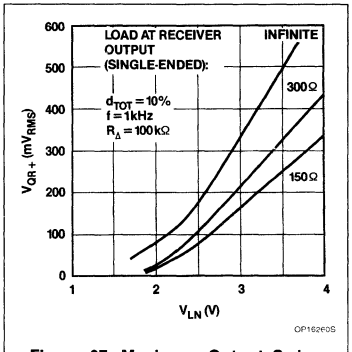

Figure 27. Maximum Output Swing Receiving Amplifier vs V_{LN} in Low Voltage Range

Confidence Tone

During DTMF dialing, the dialing tones can be heard at a low level in the earpiece The level of the tones at the receiving output depends on the gain that has been set for the receiving

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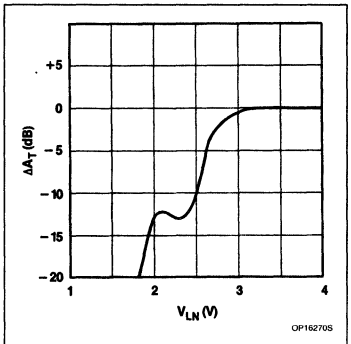

Figure 28. Typical Receive Gain vs V_{LN} in Low Voltage Range

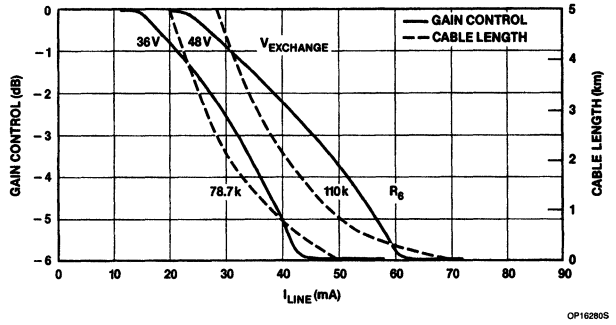

Figure 29. Gain Control Characteristics; 600Ω Feeding Bridge

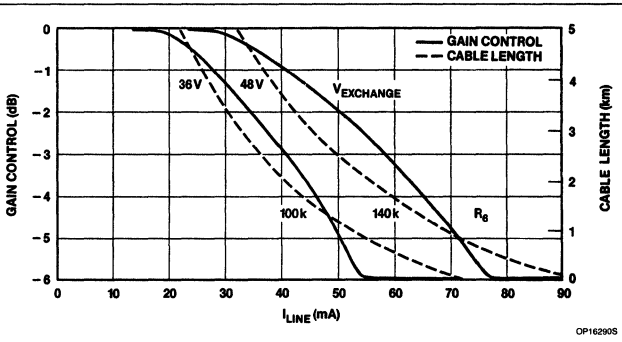

Figure 30. Gain Control Characteristics; 400Ω Feeding Bridge

amplifier, and on the tone level applied to the DTMF input.

The gain A_{CT} between the DTMF input and the receiving output is given by:

$$20 \log A_{CT} = 20 \log A_T - 50dB$$

in which A_T is a general term for telephone gain and this can be replaced by either A_{TA} (single-ended drive) or A_{TS} (symmetrical drive). This is shown in Figure 24.

Line Current-Dependent Gain Control

The gain figures of the microphone amplifier and the receiving amplifier which was derived in the preceding chapters are applicable only when the AGC is inoperative: that is, with Pin 17 (AGC) not connected (open circuit).

When the resistor R_6 is connected between AGC and V_{EE}, line current-dependent gain control of both the microphone amplifier and the receiving amplifier becomes operative; the DTMF amplifier is not affected.

Below a specific value of line current, $I_{LINE\text{-}START}$, the gain is equal to the values calculated with the formulas given before. If the current $I_{LINE\text{-}START}$ is exceeded, the gain of both of the controlled amplifiers decreases as a function of increasing DC line current. Gain control stops when another value of line current ($I_{LINE\text{-}STOP}$) is exceeded. The gain control range of both amplifiers is typically 6dB. This corresponds with a line length of 5km of 0.5mm diameter copper twisted-pair cable with a DC resistance of 176Ω/km and an average AC attenuation of 1.2dB/km. The slope of the gain control characteristic has been chosen to give an optimum tracking between the line attenuation and the required amplifier gain (typical error ⩽ 0.8dB) for a system with a 2 × 300Ω feeding bridge. In case lines with different parameters are used, a small additional tracking error will be introduced.

Correction for Exchange Supply Voltage

The value of resistor R_6 must be chosen in accordance with the supply voltage in the exchange. In Figure 29 the control curves are shown for V_{EXCH} = 36V and 48V with a feeding bridge resistance of 2 × 300Ω.

Also, the calculated relationship between line length and line current is shown in Figure 29. These ideal curves have been calculated with the assumption that an increased voltage drop across the circuit has been set (V_{LN} = 4.45V at 15mA; $R_{VA[16-18]}$ = 39kΩ) and assuming a polarity guard with 1.4V voltage drop. Other parameters will give slightly different results, giving slightly different optimum values for R_6.

Correction for Feeding Bridge Resistance

If the feeding bridge in the exchange has a resistance other than 600Ω, R_6 must be adjusted. This will introduce a minor increase in tracking error because the slope of the gain control curve has been optimized for a 600Ω feeding bridge. With a 1000Ω feeding bridge, the typical tracking error that can be expected is ⩽ 1.2dB.

Figure 30 shows the control curves for a 400Ω feeding bridge with exchange supply voltages of 36V and 48V. Figure 31 shows the characteristics for an 800Ω bridge of 48V and 60V. In Figure 32, the results for a 1kΩ bridge are shown at the same voltages.

The optimum values of R_6 for the various values of exchange supply voltage and exchange feeding bridge resistance, with a 1.4V diode bridge, R_9 = 20Ω, and increased line voltage V_{LN} = 4.45V at 15mA ($R_{VA[16-18]}$ = 39kΩ) are given in Table 1.

In case a value for R_9 is used different from 20Ω, the value for R_6 must be adapted.

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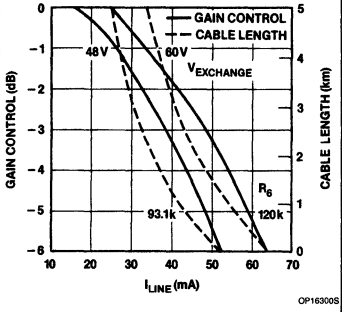

Figure 31. Gain Control Characteristics; 800Ω Feeding Bridge

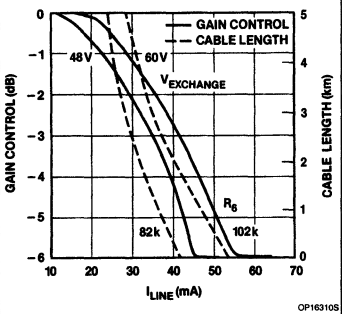

Figure 32. Gain Control Characteristics; 1000Ω Feeding Bridge

Anti-Sidetone Circuit

The anti-sidetone circuit takes care that the microphone signals available on the line output LN are suppressed sufficiently before they enter the receiving amplifier input IR. This is necessary because otherwise these signals would be reproduced as sidetone with an unacceptable high level in the telephone transducer. The anti-sidetone circuit takes the signal which is available at Pin 18 (SLPE) and uses it to compensate the microphone signal at the input IR (Pin 11) of the receiving amplifier.

The design of the anti-sidetone circuit initially depends on whether the special TEA1060-family bridge or the more conventional Wheatstone bridge is to be used. Both structures are shown in Figure 33. For the TEA1060-family bridge in Figure 33a, the bridge components are $R_1 \parallel Z_{LINE}$, R_2, R_3, R_8, R_9, and Z_{BAL}. For the Wheatstone bridge in Figure 33b, the comparable bridge components are $R_1 \parallel Z_{LINE}$, R_8, R_9, R_A, and Z_{BAL}.

Both types can be used either with a resistive set impedance or with a complex set impedance. A brief comparison of both bridge structures and the two types of set impedance is given in the next paragraphs.

Table 1

	R_{EXCH}			
	400	600	800	1000
V_{EXCH}(V)	R_6 (kΩ) with R_9 = 20Ω			
36	100	78.7		
48	140	110	93.1	82
60			120	102

NOTES:
1. V_{LN} = 4.45V at I_{LINE} = 15mA; $R_{VA[16\text{-}18]}$ = 39k
2. In case a value for R_9 is used different from 20Ω the value for R_6 must be adapted

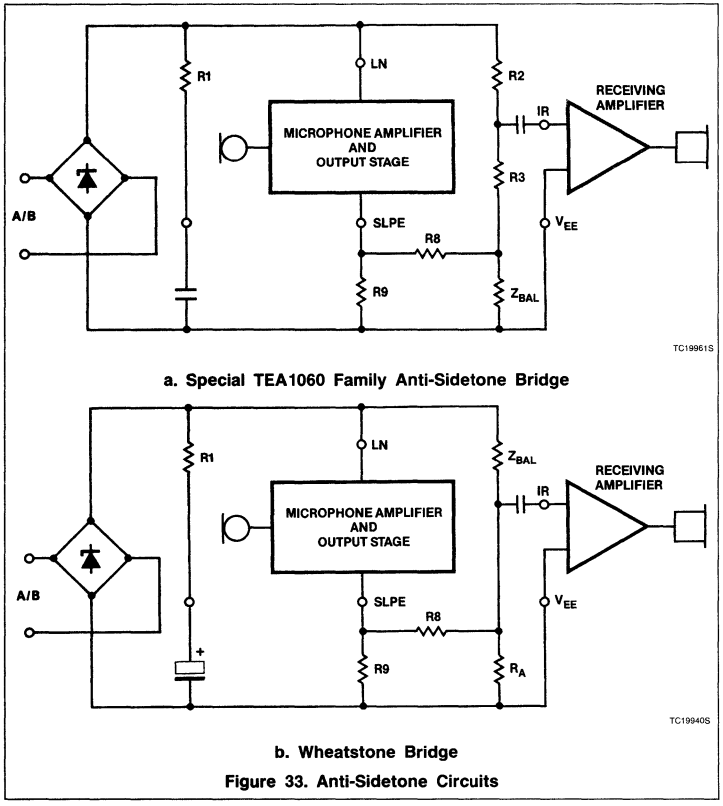

Figure 33. Anti-Sidetone Circuits

TEA1060-Family Bridge

The equivalent circuit of the TEA1060-family bridge is shown in Figure 34. Optimum suppression of the sidetone signal is obtained when the following conditions are fulfilled:

a. $R_9R_2 = R_1 (R_3 + [R_8 \parallel Z_{BAL}])$

b. $[Z_{BAL}/(Z_{BAL} + R_8)] = [Z_{LINE}/(Z_{LINE} + R_1)]$

If fixed values are chosen for R_1, R_2, R_3, and R_9, condition 'a' will always be fulfilled provided that $|R_8 \parallel Z_{BAL}| \ll R_3$.

To obtain optimum sidetone suppression, condition b has to be fulfilled, resulting in.

$Z_{BAL} = (R_8/R_1) \cdot Z_{LINE} = k \cdot Z_{LINE}$

where k is a scale factor: $k = (R_8/R_1)$

Scale factor k (in fact the value of R_8) must be chosen to meet the following criteria:

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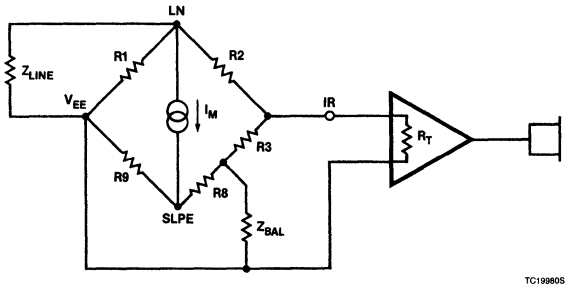

Figure 34. Equivalent Circuit of TEA1060 Family Anti-Sidetone Bridge

- compatibility with a standard capacitor from the $E_6(\mu F)$ or $E_{12}(pF)$ range for Z_{BAL}
- $|Z_{BAL} \parallel R_8| \ll R_3$ necessary to fulfill condition a to ensure correct operation of the anti-sidetone circuit
- $|Z_{BAL} + R_8| \gg R_9$ to avoid influence on microphone gain

In practice Z_{LINE} varies strongly with the line length and line type. Consequently, a value for Z_{BAL} has to be chosen that corresponds to an average line length giving satisfactory sidetone suppression with short and long lines. The suppression further depends on the accuracy with which Z_{BAL} equals this average line impedance.

In the basic application of Figure 3, Z_{BAL} has been optimized for a line length of 5km 0.5mm diameter copper twisted pair with an average attenuation of 1.2dB/km, a DC resistance of 176Ω/km and a capacitance of 38nF/km. The corresponding impedance can be approximated by:

Scale factor k has been chosen according to the criteria mentioned before, resulting in $k = 0.636$. So Z_{BAL} and R_8 can be calculated resulting in the following practical values: $R_{11} = 130\Omega$, $R_{12} = 820\Omega$, $C_{12} = 220nF$, and $R_8 = 390\Omega$.

This results in a roughly equal sidetone level (acoustically measured) at 0km line and with a 10km line with the line current-dependent gain control activated. In case no AGC is used, the sidetone has to be optimized for a shorter line length in order to obtain equal (acoustical) sidetone levels at 0km and at 10km line length. Of course, overall sidetone suppression is worse in that case compared to the situation where AGC is activated. In practice, normally a compromise is chosen between loudness of the set and sidetone level; this means that sending and receiving gain will be reduced somewhat.

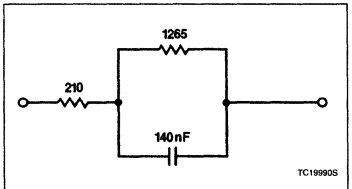

Figure 35. Equivalent Line Impedance for Optimum Sidetone Suppression

The attenuation of the received line signal between LN and IR can be derived from:

$$\frac{V_{IR}}{V_{LN}} = \frac{R_T \parallel R_3}{R_2 + (R_T \parallel R_3)}$$

where R_T is the input impedance of the receiving amplifier (typically 20kΩ). This attenuation is about 32dB with the basic application as shown in Figure 3. Frequency dependence of the input attenuation is negligible in the audio frequency range. However, a frequency roll-off can be obtained by means of a capacitor connected between IR and V_{EE} to prevent high frequency components from entering the receiving amplifier.

Complex Set Impedance

Complex set impedances can be realized by using a complex network instead of R_1, and normally the bridge can be rebalanced by readjusting the values of R_8 and Z_{BAL}, and either R_2 or R_9. Changing R_9 also has consequences on other parameters and the range of possible values is limited. Therefore, the design procedure as given in Appendix 1 should be considered. Changing R_2 has influence on the attenuation of the received signal between LN and IR; this necessitates a readjustment of the receiving gain. Note that changing R_1 also has influence on the capabilities of the supply for peripherals.

The TEA1060 family bridge configuration has the advantage of an almost flat transfer function in the audio frequency range between LN and the receiving amplifier input IR, either with a resistive set impedance or with a complex set impedance.

Furthermore, the attenuation of the bridge for the received signal is independent of the value that has been chosen for Z_{BAL} once the set impedance has been fixed and condition 'a' is fulfilled. Thus, readjustment of receive gain is not necessary in many cases.

Disadvantages include the need for a relatively large capacitor (about 200nF) in Z_{BAL}, and the need for an extra resistor on top of those required by the Wheatstone bridge. Calculation of new values is also sometimes considered to be more difficult, particularly in case of complex set impedances.

In some cases, calculating the optimum condition is not very useful because a compromise must be chosen to meet sidetone requirements in several conditions. In those cases a more practical and probably faster method is using an empirical method: doing acoustical measurements and hustling components Z_{BAL} and R_8 until the requirements are met.

Wheatstone Bridge

The conditions in the Wheatstone bridge (equivalent circuit in Figure 36) for optimum sidetone suppression are given by:

$$Z_{BAL} = \frac{R_8}{R_9} \times \frac{R_1 Z_{LINE}}{R_1 + Z_{LINE}}$$

provided that $R_8/R_9 >> 1$.

Also, for this bridge type a value for Z_{BAL} has to be chosen that corresponds with an average line length.

The attenuation of the received line signal between LN and IR is given by:

$$\frac{V_{IR}}{V_{LN}} = \frac{R_8 \parallel R_T \parallel R_A}{Z_{BAL} + (R_8 \parallel R_T \parallel R_A)}$$

Where R_T = input impedance of the receiving amplifier at IR, typically 20kΩ.

A practical circuit could have the following values: $R_8 = 820\Omega$, $R_1 = 620\Omega$, and Z_{BAL} optimized for the line impedance as shown in Figure 35. With R_A = infinite and a 600Ω load at the line, the attenuation varies typically from about 24dB to 27.5dB over the normal audio frequency range; the lower attenuation occurs at the upper frequencies. R_A is used to adjust the bridge attenuation; its value does not have influence on the balancing of the bridge.

Complex Set Impedance

If complex set impedances are used with the Wheatstone bridge, it can be rebalanced by adapting the values of Z_{BAL}. However, the frequency dependence of the transfer function between LN and IR will increase.

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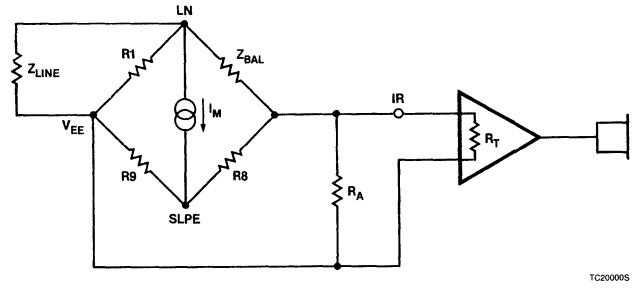

Figure 36. Equivalent Circuit of Wheatstone Bridge Anti-Sidestone Circuit

The Wheatstone bridge offers the advantages of needing one less resistor compared to the special TEA1060-family bridge, and only a small capacitor (about 10nF) is needed in Z_{BAL}. Furthermore, the values are calculated rather easily with either resistive set impedances or complex set impedances.

Disadvantages are the dependence of the attenuation of the bridge on the value chosen for Z_{BAL}, and also the frequency-dependence of that attenuation. This necessitates a readjustment of the receive gain.

Mute Input

Electronic switching between dialing and speech can be obtained by controlling the MUTE input at Pin 14. If a high level ($\geq$ 1.5V, $\leq$ 15μA) is applied to the MUTE input, then both the microphone and receiving amplifier inputs are inhibited, and the DTMF input is simultaneously enabled. The converse situation, with DTMF inhibited and the microphone and earpiece amplifier both enabled, is obtained by either applying a low-level input ($\leq$ 0.3V) to MUTE, or by leaving the MUTE input open. The internal switching takes place with negligible clicking at the earpiece outputs and on the line.

If the supply voltage at V_{CC} drops below V_{CC} = 2V (in the case of no external load at V_{CC}. V_{LN} < 2.5V and I_{LINE} < 6mA), the mute function becomes inoperative and the circuit will be in a condition where signals applied to either the microphone inputs or the DTMF input will be sent onto the line. However, under these low voltage conditions, only occurring during parallel operation of sets under worst case conditions, dialing normally will not take place.

Power-Down Input

The power-down input PD at Pin 12 is available for use in pulse dialing and in register recall applications, in which the telephone line is interrupted. During these interrupts, the telephone set is without continuous power and the transmission IC and the peripheral circuits must be supplied by the charge available in the smoothing capacitor C_1 connected to V_{CC} (Pin 15) in Figure 3. The discharge time of this capacitor will be longer in case the power-down function is used; this results in less ripple on V_{CC}.

When a high-level input ($\geq$ 1.5V, $\leq$ 10μA) is applied to the PD pin, the internal supply current is reduced from about 1mA to typically 55μA at V_{CC} = 2.8V. Furthermore, the voltage regulator capacitor C_3 at REG (Pin 16) is internally disconnected to prevent it from being discharged during line interrupts. This means that after each line interrupt, the voltage regulator is able to start without delay at the same DC line voltage as before the interrupt. This minimizes the contribution of the IC to the shape of the current pulses during pulse dialing. Of course, in case of a highly inductive character of the exchange feeding bridge, the inductors mainly determine current waveform. Under these conditions, the voltage regulator may show some switch-on delay because of the active character of the transmission circuit (the exchange inductors determine the current resulting in voltage overshoot at the line connection (LN) of the IC).

In case the voltage drop across the circuit is increased by means of $R_{VA(16-18)}$, the power-down function will be affected. This results in a different shape of the current pulses.

Immunity to RF Signals

In a strong radio frequency electromagnetic field, it is possible for common-mode amplitude modulated RF signals to be present on the a/b lines. These common-mode signals can sometimes become differential-mode signals as a result of asymmetrical parasitic capacitances to ground; this may occur, for example, through the hand of the subscriber holding the handset. Steps have to be taken to avoid the possibility of these signals being detected and the low-frequency modulation appearing as unwanted signal at the earpiece or on the line. Small discrete capacitors are necessary to suppress the unwanted RF signals before they can enter the circuit. Capacitor types suitable for high frequencies must be used, such as ceramic types. In Figure A1 they have been added to the basic application circuit. C_8 and C_9 at the microphone inputs, C_{10} at the receiving input IR, C_{13} at the supply point V_{CC}, and C_{11} at the transmitter output LN. All of the capacitors are connected to the common V_{EE}.

Furthermore, the layout of the printed circuit board may have influence on RF immunity. The copper ground area should be kept as large as possible. Ground loops must be avoided and traces must be kept as short as possible. RFI-capacitors must be mounted as close as possible to the IC pins.

In practice, it has been shown that two inductors (chokes with a value between 200μH and 1mH) in series with the a/b lines improve RF immunity considerably. It has been shown also in practice that a so-called "guard ring" (closed copper ring) around the circuit gives a considerable improvement against radiated magnetic fields.

Because the TEA1067 has a very high microphone input impedance, it is possible to use low-pass filtering in series with both microphone inputs, without affecting gain accuracy.

The RC filter should be positioned as close as possible to Pins 7 (MIC−) and 8 (MIC+). A low-ohmic termination across the microphone inputs will reduce pick-up of unwanted RF signals via the handset cord.

Polarity Guard and Transient Suppression

There is a possibility that the transmission IC is destroyed by excessive current surges on the telephone lines if no proper measures are taken. The type of protection differs for sets with only DTMF dialing or sets with either pulse-dialing or DTMF dialing with "flash" (register recall by means of a timed line interrupt).

With DTMF dialing only, the bridge rectifier, which normally acts as a polarity guard, can also incorporate two voltage reference diodes (such as BZW14). Under normal operating conditions, one of the two voltage reference diodes conducts while the other is non-conducting. If the voltage across the set temporarily exceeds the reference voltage of the previously mentioned non-conducting diode, it will conduct and limit the voltage across the set. The maximum permissible voltage across the transmission circuit is 12V continuously and is determined by the collector-emitter breakdown voltage of the IC process used. During switch-on and line interrupts, the maximum permissible voltage is 13.2V allowing the use of a 12V voltage reference diode in the polarity guard.

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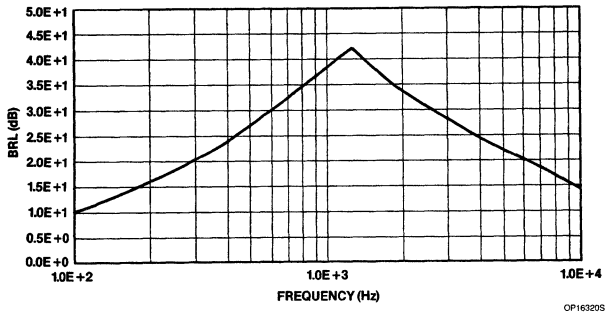

NOTE: $BRL = \frac{Z - Z_0}{Z + Z_0}$ with $Z_0 = 600\Omega$

Figure 37. Balance Return Loss (BRL) as a Function of Frequency

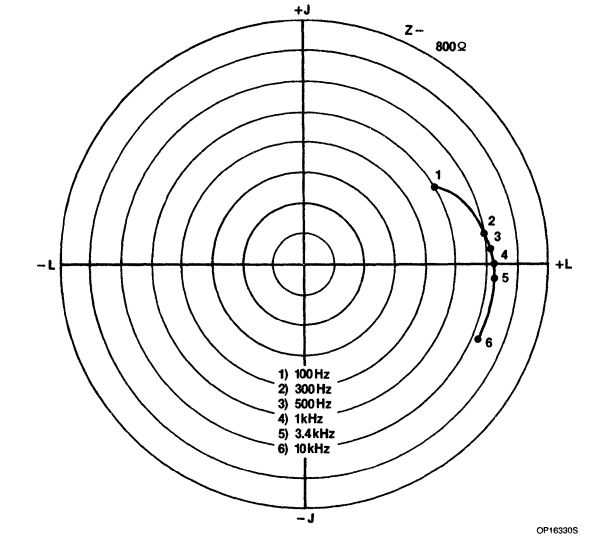

Figure 38. Polar Plot of Impedance Between A/B Connections

Further protection is offered by the resistor R_{10} in series with the bridge rectifier, which limits the current that can be drawn by the IC. The maximum allowed transient voltage on the circuit, including the protection resistor R_{10} being 13Ω and with $R_9 = 20\Omega$, is 28V during 1ms with a repetition time of 5sec. This corresponds with a 50A surge onto the BZW14 zener diodes used in the polarity guard.

For DTMF dialing with flash, or for pulse dialing, a different protection arrangement is necessary because, during line interruption, the line current must be zero. This means that the bridge rectifier must be able to withstand a relatively high voltage, on the order of 200V. A polarity guard using four diodes with type number BAS11 is appropriate for this purpose. Protection against line current surges can then be obtained by means of a suitable VDR connected between the a/b lines in front of the polarity guard. The speech circuit is protected against overvoltages that may occur, for example, during switching-in, by means of a 12V regulator diode connected between LN and V_{EE}, or in case a current limiter is used (e.g., combined with the interrupter), by a 6.8V voltage regulator diode connected between LN and SLPE. The latter method also provides symmetrical clipping of the sending signal. Figure A2 shows an application of the TEA1067 with an interrupter circuit.

Hints for Printed Circuit Board Layout

Care must be taken to avoid having the large line current flowing into common ground traces to which sensitive points are connected.

For this reason, resistors R_9 (connected between STAB and V_{EE}) and R_6 (connected between AGC and V_{EE}) must be situated on the PCB close to Pin 10 (V_{EE}).

Also, the ground connection of the earpiece should preferably be realized at a point where no large line current is flowing.

The copper tracks connecting R_7 and R_4 to the corresponding IC pins should be kept as short as possible.

The ground connection of all RFI capacitors should be made by means of the largest possible copper planes. RFI capacitors must be connected as close as possible to the pins that have to be decoupled.

The ground plane on the circuit board must be kept as large as possible.

PERFORMANCE

Some measurements have been done with the basic application circuit, including RFI capacitors as shown in Figure A1. This gives an indication of the performance of the TEA1067.

Balance Return Loss

The result of the balance return loss measurement (BRL) is shown in Figure 37. The impedance of the circuit is shown in Figure 38.

Different values chosen for C_3 and for R_9 will have influence on the impedance and the BRL of the circuit. Remember that C_3 and R_9 also determine some other parameters.

Frequency Characteristics

Figure 39 shows the frequency characteristic of the sending channel measured between microphone inputs and the transmitter output LN with a 600Ω load. The microphone gain is set by means of R_7 to 52dB ($R_7 = 68.1k\Omega$). The upper cut-off frequency is about 24kHz (mainly determined by the time constant R_7C_6).

Note that if a complex set impedance has been chosen, it will have influence on the frequency characteristic.

Figure 40 shows the frequency characteristic of the receiving channel measured between LN and the QR+ output loaded with 150Ω (single-ended drive; 10μF DC-blocking capacitor). With $R_4 = 100k\Omega$, the transfer ratio

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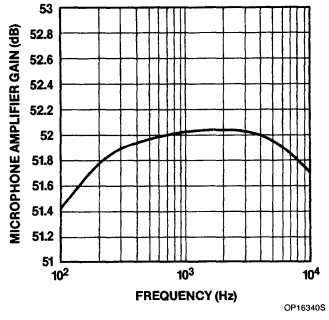

Figure 39. Frequency Characteristic of Microphone Amplifier

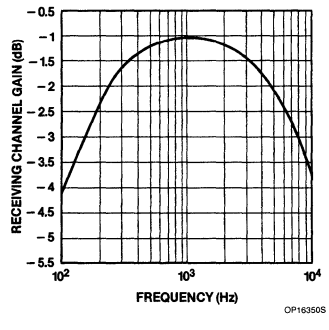

Figure 40. Frequency Characteristic of the Receiving Channel

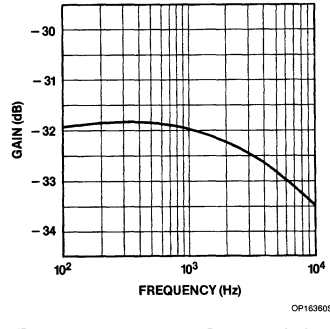

Figure 41. Frequency Characteristic of the Anti-Sidetone Circuit Between LN and IR

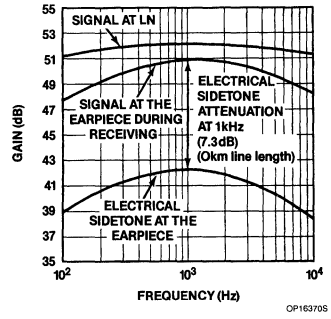

Figure 42. Frequency Characteristic of the Electrical Sidetone at 0km Line Length

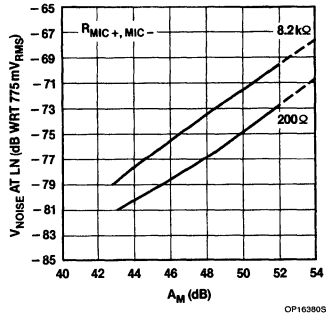

Figure 43. Psophometrically-Weighted Noise on the Line LN vs Microphone Gain

is −1dB at 1kHz. The lower cut-off frequency is 120Hz and is determined in this case by the time constant R_LC_2 of the load resistor R_L and the DC-blocking capacitor C_2. The upper cut-off frequency is about 9.5kHz and is determined partly by R_4C_4 (15kHz) and partly by the cut-off frequency of the anti-sidetone circuit (18kHz).

The frequency response of the anti-sidetone circuit (LN to IR) is given in Figure 41. The cut-off frequency is about 18kHz. This is mainly obtained by the 2.2nF capacitor connected between IR and V_{EE} (necessary for RF immunity)

The transfer ratio as a function of frequency measured from the microphone inputs to a 150Ω asymmetrical load at the receive output QR+ (10μF DC blocking capacitor) is shown in Figure 42. This represents the electrical sidetone at 0km of telephone line (600Ω load at LN) The measured sending signal at LN is shown also The signal at the receive output with the same line signal in receiving condition is shown also in Figure 42.

The difference between wanted receive signal and principally unwanted sidetone at the receive output is in fact the electrical sidetone suppression. This means that for this application the electrical sidetone suppression at 0km of line length is about 7.3dB at 1kHz. The result depends strongly on the balancing of the anti-sidetone circuit. In this case, the balance impedance Z_{BAL} has been optimized for 5km line length with 0.5mm diameter, 176Ω/km and 38nF/km

Electrical sidetone suppression is not dependent on whether gain control is used or not, because both amplifiers (microphone and receive) are affected by the gain control function.

Noise

Typical noise psophometrically (P53 curve) measured on the line LN with a 600Ω load is given as a function of microphone gain in Figure 43. The microphone input is loaded with a 200Ω resistor or 8.2kΩ.

Psophometrical noise at the receive output (single-ended 300Ω load) as a function of microphone gain is shown in Figure 44. Parameters are the receive gain and the resistor across the microphone inputs.

NOTE:
For information on discrete semiconductors used in this application note, contact Amperex Electronic Corp., Smithfield, RI, (401) 232-0500

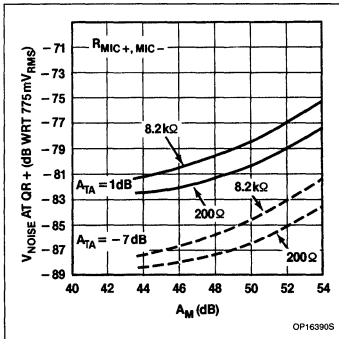

Figure 44. Psophometrically Weighted Noise at the Receiver Output vs Microphone Gain

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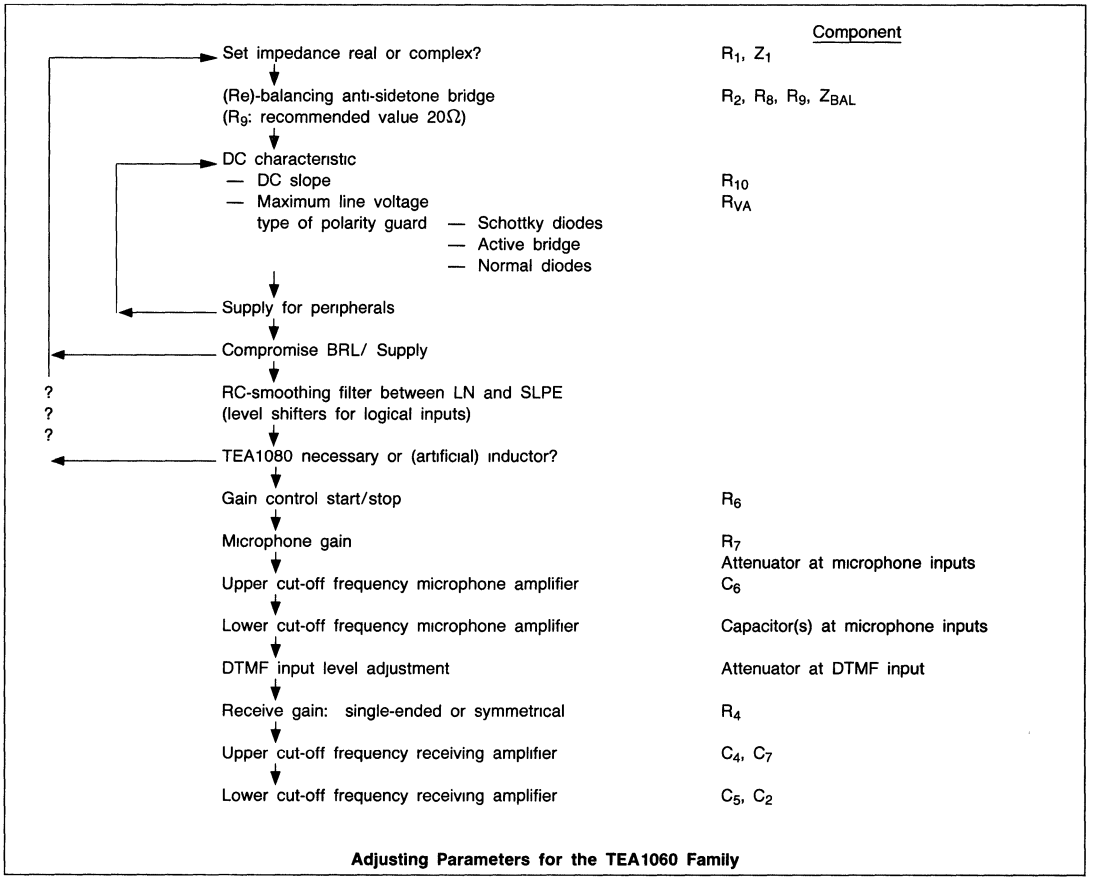
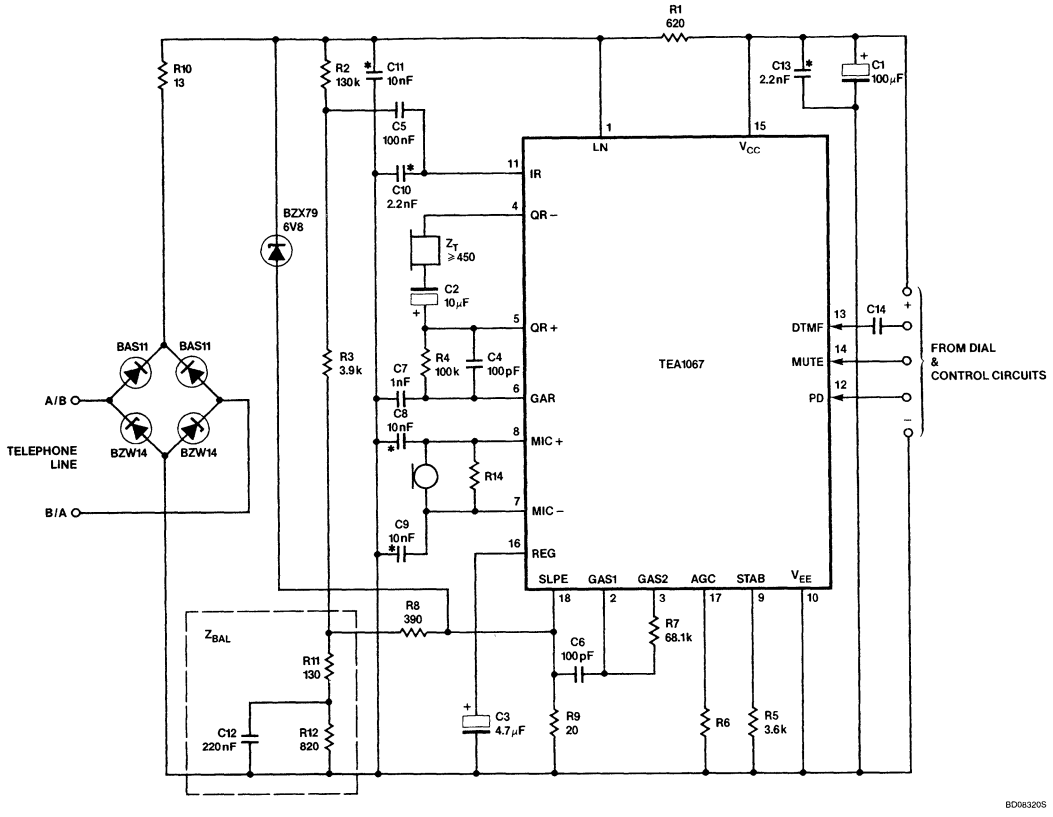
APPENDIX I



Adjusting Parameters for the TEA1060 Family

Application of the Low Voltage Versatile Transmission Circuit AN1942



NOTE:
RFI capacitors are marked with an asterisk

Figure A1. Basic Application Diagram of TEA1067 in Sets With DTMF Dialing

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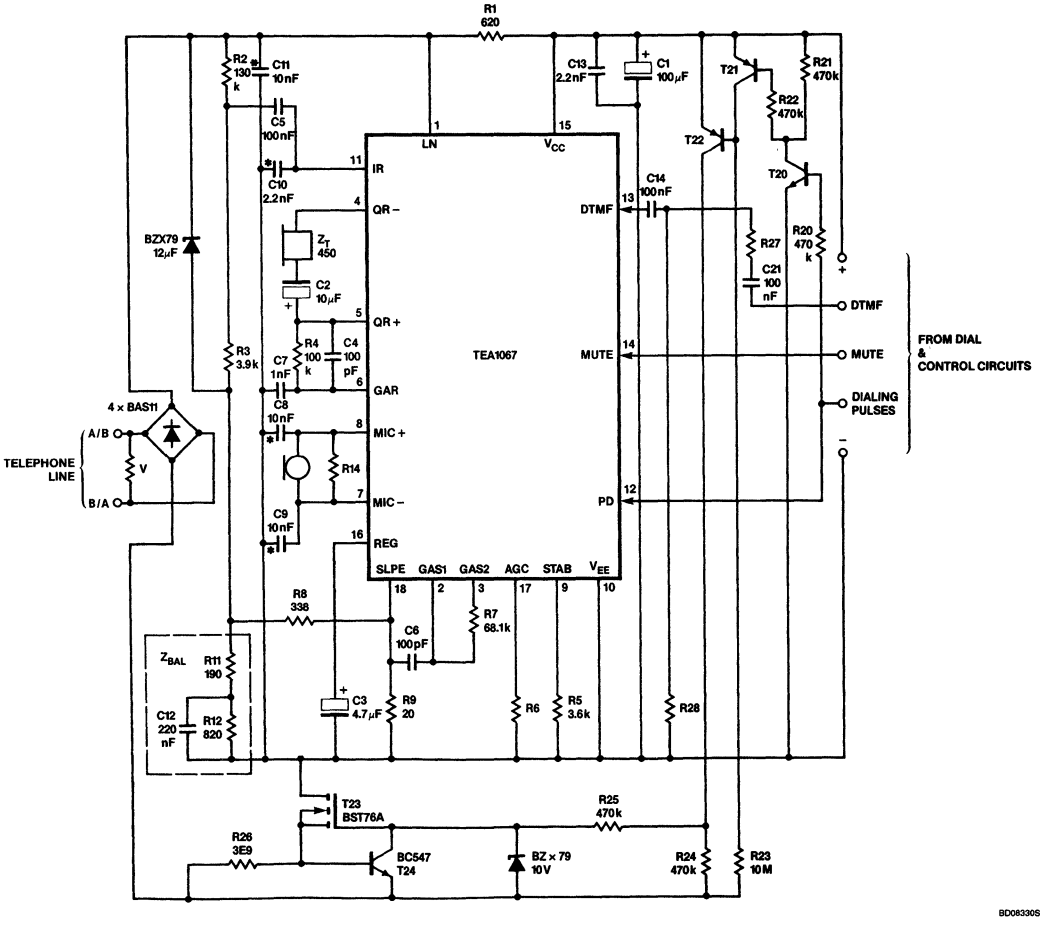
Application of the Low Voltage Versatile Transmission Circuit AN1942



NOTE:
RFI capacitors are marked with an asterisk

Figure A2. Basic Application Diagram of TEA1067 in Sets With Combined Pulse and Tone Dialing Including Interrupter With Interface

Signetics

Linear Products

AN1943

Supply of Peripheral Circuits With the TEA1067 Speech Circuit

Application Note

INTRODUCTION

The telephony line interface and speech transmission circuits TEA1060/1 have been in use for several years now. They contain all interface circuitry required to connect transducers and dialers to a telephone line.

A lot of components such as dialers and computers have been developed which can be interfaced to the TEA1060/1 easily. These components are powered by the supply point of the TEA1060/1.

To meet the North American Telephony requirements RS-470, the new speech circuit TEA1067 has been developed. TEA1067 operates at a lower line voltage, which enables it to operate in parallel with the conventional telephone sets (unlike the TEA1060/1).

However, a lower line voltage and the possibility of connecting conventional telephone sets in parallel have potentially severe effects on the supply capabilities of the speech circuit.

This application report contains some proposals to realize optimal connection of peripherals to the TEA1067 speech circuit.

NORTH AMERICAN TELEPHONY REQUIREMENTS RS-470 FOR TELEPHONE SETS IN USA

Telephone sets used in the USA (and also in some Far East countries) have to fulfill some special demands which are described in the RS-470 requirements. The points of importance for Philips speech circuits are:

- It is allowed to connect more telephone sets in parallel. RS-470 doesn't specify details, but it seems to be that electronic speech circuits must remain operative (at least at a reduced performance) if a conventional (carbon microphone) telephone set is connected in parallel on a subscriber loop, having the minimum line current of 20mA. For measurements, a reasonable replacement for such a conventional telephone set seems to be a 200Ω resistor.
- The off-hook tip-to-ring DC voltage versus current characteristics must be in the acceptable region of Figure 1 during the on-hook to off-hook transition, and during the make-interval of rotary dial pulses on outgoing calls, and for at least one second after answer of an incoming call. The upper limit of this region is determined by the ability of the telephone set to draw adequate current for proper pull-up of central office relays.

After this one-second period for incoming calls, and during DTMF-dialing, and after called-party answer on outgoing calls (where the relays are required only to hold their energized state), operation may fall within the conditionally acceptable region of Figure 1.

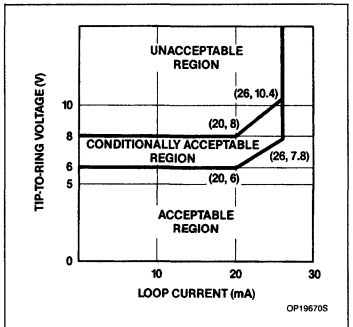


Figure 1. DC Voltage vs Current Characteristics

It is desired that the off-hook tip-to-ring impedance of the telephone set be 600Ω across the 200 – 3200Hz band. More specifically, the balance return loss (measured against 600Ω) shall be greater than 3.5dB for the 200 – 3200Hz band and greater than 7.0dB for the 500 – 2500Hz band.

EFFECTS OF RS-470 ON PHILIPS SPEECH CIRCUITS

Under normal operation, the minimum line current which can occur according to the RS-470 requirements is 20mA. The minimum supply capabilities of the supply point of the TEA1060/1 are according to Figure 2a.

Most Philips CMOS peripherals require a minimum supply voltage of 2.5V. Taking into account 0.4V as the forward voltage drop of a Schottky enable diode (BAT85: $V_F < 320mV$ at 25°C and 1mA), the minimum allowable voltage of the supply point of the TEA1060/1 is 2.9V. At this voltage the minimum available supply current is 1.2mA, according to Figure 2a, which is enough to power a CMOS microcontroller (e.g., PCD3315) and a DTMF generator (PCD3312).

However, there are two problems with the TEA1060/1 with respect to the RS-470 requirements.

The first problem concerns the parallel connection of conventional telephone sets and TEA1060/1 sets at low line currents. Taking a resistance of 200Ω for the parallel set, the line voltage at 20mA line current will drop to about 3.8V (assuming 1mA remaining current for the TEA1060/1) or 2.3V after the polarity guard. The transmitting stage of the TEA1060/1 doesn't function at such low voltages. In order to keep the transmitting amplifier operating at such low line voltages (with a reduced performance), the TEA1067 has been designed.

Second, the maximum line voltage of the TEA1060/1, excluding the interrupter circuit, measures 6.35V at 20mA [maximum line voltage at 20mA (4.75V), plus temperature effects (assume 0.1V), plus polarity guard voltage drop (assume 1.5V)], which is 0.35V too much (see Figure 1). Therefore, the line voltage of the TEA1067 has been decreased by 0.55V with respect to the TEA1060/1.

However, both measures have severe implications for the architecture advised by Philips/Signetics hitherto.

If a 200Ω telephone set is connected in parallel with a TEA1067 set on a 20mA loop, the supply voltage for peripherals will decrease to less than 2V. In applications with the TEA1060/1, Philips/Signetics advises their customers to use a MOSFET of the type BST76A as an interrupter switch. Since the gate-source threshold voltage of this type of FET can be as high as 2 7V, problems can be expected when used in a TEA1067 set with a 200Ω parallel set — it can't be guaranteed that the interrupter switch remains conducting. Therefore, a bipolar interrupter will be described which doesn't have this problem. The problems that occur with the supply of peripherals in this case will be illustrated later.

Furthermore, due to the reduced line voltage of the TEA1067, the supply capabilities of its supply point are considerably reduced with respect to the TEA1060/1 (see Figure 2b). At 2.9V, a minimum supply current of only 300μA can be guaranteed. This is not enough to power a microcontroller and a DTMF dialer (e.g., PCD3315 + PCD3312) simultaneously. Some suggestions to overcome this problem will be given later.

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Supply of Peripheral Circuits With the TEA1067 Speech Circuit AN1943

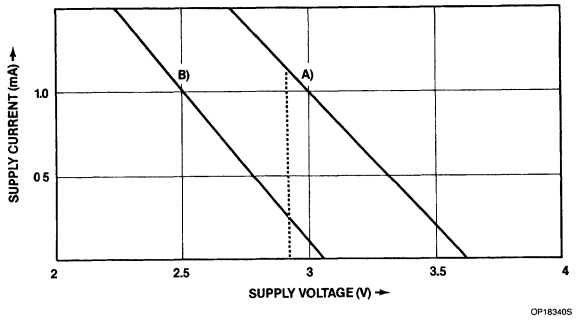


Figure 2. Minimum Supply Current Available for Peripherals as a Function of Supply Voltage of TEA1060/1 (A) and TEA1067 (B) at 20mA Line Current

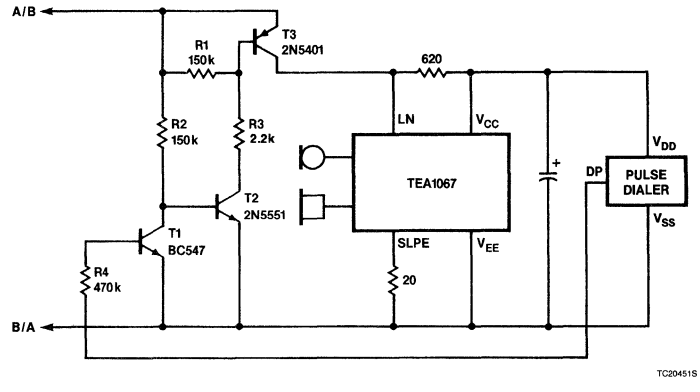


Figure 3. Circuit Diagram of Low-Voltage Interrupter

A LOW-VOLTAGE INTERRUPTER

In Figure 3 the circuit diagram of an interrupter is given which operates at input voltages down to 1V

The circuitry around T2 and T3 is commonly used already in telephony applications and needs no further explanation The interface function between this interrupter and the pulse dialer is performed by transistor T1 and resistor R4 Using transistors of the type 2N5401 and 2N5551 allows operation up to 150V In case higher voltages occur, a voltage limiting device (e.g., a VDR) has to be used in front of the circuitry. No current limiting function is accomplished in this circuit.

In Figure 4 the typical voltage drop over the interrupter (V_{EC} of T3) is given as a function of loop current using a 2 2kΩ resistor for R3 A lower resistance lowers the voltage drop at high line currents, but also reduces the current which is left for the TEA1067.

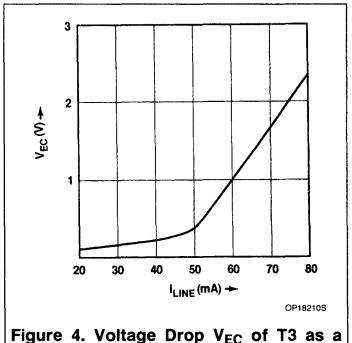


Figure 4. Voltage Drop V_{EC} of T3 as a Function of Line Current

Since R3 is connected in parallel with the 600Ω impedance of the TEA1067 circuitry, the total set impedance is now lower than 600Ω. Using 2 2kΩ for R3, the TEA1067 impedance must be increased to approximately 850Ω in order to compensate for this effect. In the next section it will be shown that this measure adversely affects the supply capabilities of the TEA1067.

INCREASING THE SUPPLY CAPABILITIES OF THE TEA1067

Use of an Inductor

The bottleneck in the supply problems of the TEA1067 is in the 620Ω resistor connected between the pins LN and VCC of the TEA1067 (Figure 3). It determines the supply capabilities of the TEA1067 as well as the AC impedance of the circuit. A reduction of the resistance therefore results in improved supply capabilities, but also in poorer BRL figures.

If this DC resistance can be reduced while maintaining the 600Ω impedance for AC, the supply problem can be solved. This can be realized by means of an inductor connected in parallel with the 620Ω.

There are two possibilities to realize a practical inductor:

- Use of a coil (Figure 5a)
- Use of an electronic inductor (e.g., TEA1080 supply IC (Figure 5b), (discrete) gyrator circuit)

Use of a Schottky Diode Polarity Guard

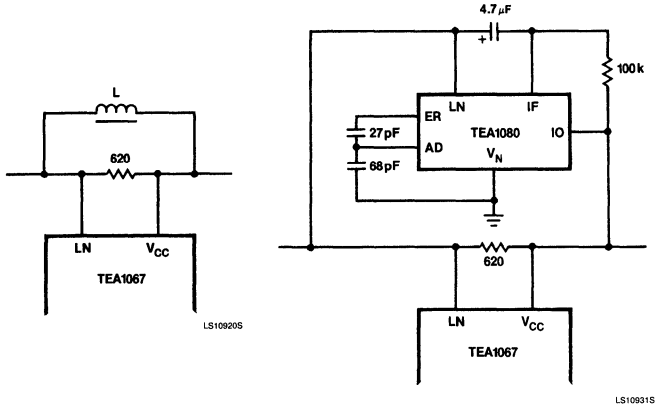
In case only DTMF dialing is used (without FLASH), no interrupter circuit is required and, therefore, no transients due to line current interruptions can occur. This makes it possible to realize protection with rugged low-voltage zener diodes (e.g., Philips BZW14 with a maximum voltage during transients of 28V). At such low voltages, the high voltage diodes required in the polarity guard (e.g., BAS11 which can stand 300V) normally can be replaced by low-voltage Schottky diodes (e.g., BAT86 which can stand 50V) resulting in a lower voltage drop over the polarity guard. In Figure 6, two possible configurations are given.

In Figure 6a the voltage gain (due to a lower voltage drop) is about 0.5V; in Figure 6b it is about 1.0V.

It is possible now to increase the line voltage of the TEA1067 by 0.5 or 1.0V, thus increasing the supply capabilities of the TEA1067. (The increase will measure 0.5V/ 620Ω = 0.8mA in Figure 6a or 1.6mA in Figure 6b.

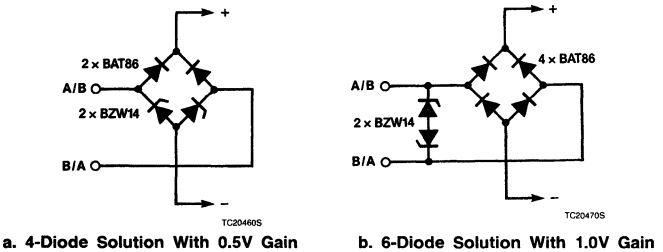
Increase of the line voltage of the TEA1067 can be achieved by means of an external resistor between the pins REG and SLPE. In Figure 7 the relation between this resistance and the resulting typical line voltage for a line current of 20mA is given.

Supply of Peripheral Circuits With the TEA1067 Speech Circuit AN1943



a. Coil b. TEA1080

Figure 5. Examples of Increasing the Supply Capabilities of the TEA1067



a. 4-Diode Solution With 0.5V Gain (Due to a Lower Voltage Drop)

b. 6-Diode Solution With 1.0V Gain (Due to a Lower Voltage Drop)

Figure 6. Schottky Diode Polarity Guard With Protection

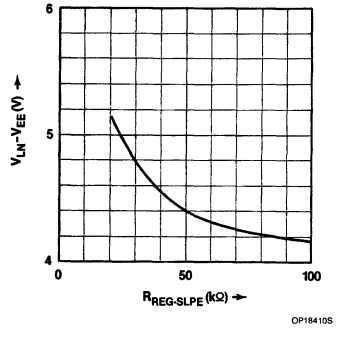


Figure 7. Typical Line Voltage ($V_{LN}-V_{EE}$) as a Function of $R_{REG-SLPE}$ at a Line Current of 20mA

However, this resistor causes a slightly increased spread in the voltage drop and a slightly modified temperature coefficient of the TEA1067. Besides, it has a minor influence on the power-down function of the TEA1067.

Two Other Methods

In principle, the RS-470 requirements give two alternative ways to come out of the supply problems of the TEA1067:

1) The TEA1067 itself fulfills the balance return loss figures required with a large margin. Accepting a smaller margin by means of decreasing the AC impedance will result in an increase of the supply capabilities.
2) The most severe supply problem occurs when a DTMF dialer must be operative. But in that case, operation in the conditionally acceptable region of Figure 1 is allowed! This lightens the supply problems considerably.

In Figure 8, the minimum supply capabilities of the TEA1067 are given as a function of the supply resistor of the TEA1067. A subscriber line having the minimum line current of 20mA

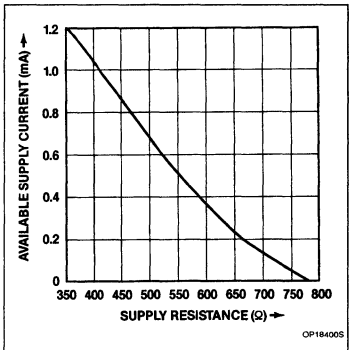


Figure 8. Calculated Minimum Supply Current Available at the Supply Point of the TEA1067, at a Voltage of 2.9V, Assuming a Subscriber Line of 20mA, as a Function of the Supply Resistance

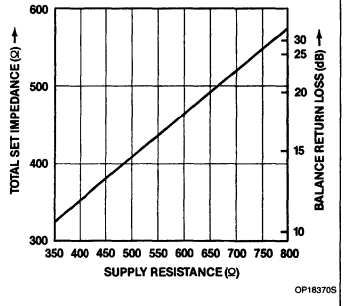


Figure 9. Calculated Total Set Impedance and BRL as a Function of the Supply Resistor of the TEA1067 (Including Influence of 2.2kΩ Interrupter)

is assumed here. Assuming the use of a bipolar interrupter having a resistance of 2.2kΩ (which is connected in parallel to the TEA1067), the resulting set impedance and BRL are given in Figure 9.

As can be seen in Figure 8, the supply capabilities of the TEA1067 equal those of the TEA1060/1 if a supply resistor of 380Ω (instead of the 620Ω used for the TEA1060/1) is used. The resulting total set impedance will be 320Ω, resulting in a BRL of about 10dB (see Figure 9). This still fulfills the RS-470 requirements (> 7dB between 500 and 2000Hz) with a safe margin.

However, change of the 620Ω resistor of the TEA1067 results not only in a change of AC impedance and an improvement of the supply point, but also in a change of microphone gain (which depends linearly on the load

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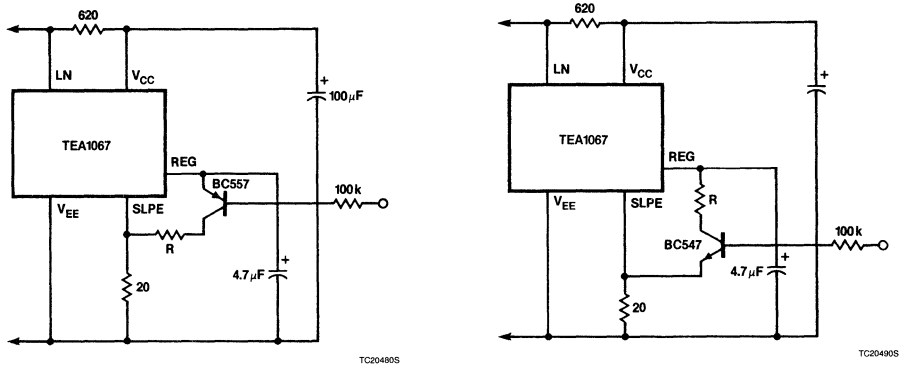
Supply of Peripheral Circuits With the TEA1067 Speech Circuit AN1943



a. HIGH = Normal Voltage, LOW = Increased Voltage

b. HIGH = Increased Voltage, LOW = Normal Voltage

Figure 10. Circuit to Increase the Line Voltage Temporarily

impedance) and in a change of the driving range of the transmitting stage. Besides, rebalancing the anti-sidetone bridge will become necessary.

If a better BRL is required, it is possible to use one of the circuits given in Figure 10. In these circuits the supply resistor is increased again, resulting in better BRL figures, but also in reduced supply capabilities.

However, if maximum supply current is required (i.e., during DTMF dialing), the line voltage can be increased by activating the transistor, thus giving a higher maximum supply current. Resistor R increases the line voltage according to the principle described previously and in Figure 7.

The switching transistor can be driven directly by a mute signal generated by a DTMF generator, resulting in the nominal line voltage except for the time DTMF tones are generated. This approach makes it possible to dimension the supply resistor in such a way that it can power all peripherals excluding the DTMF dialer. In case of DTMF dialing, the line voltage will be increased, resulting in enough supply current for the DTMF dialer, too.

It is also possible to drive the transistor automatically, according to the circuit given in Figure 11. Immediately after going off-hook, T1 is switched off until C1 is charged to V_{CC} ($V_{REG} - 0.6V$) via R2. Until then, the line voltage will fall into the acceptable region of Figure 1. After this period, the line voltage will be increased and will fall into the conditionally acceptable region of Figure 1.

If a dial pulse or a flash signal is applied to D1, C1 is discharged rapidly via D1, thus bringing back the line voltage into the acceptable region of Figure 1.

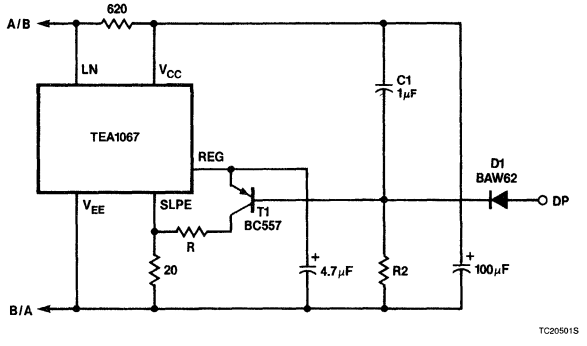
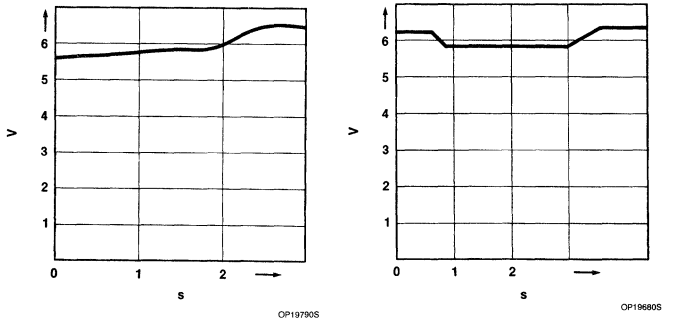


Figure 11. Circuit Which Increases Line Voltage if This is Allowed According to RS-470



a. After Initial Switch-On

b. During and After Pulse Dialing

Figure 12. Line Voltage as a Function of Time

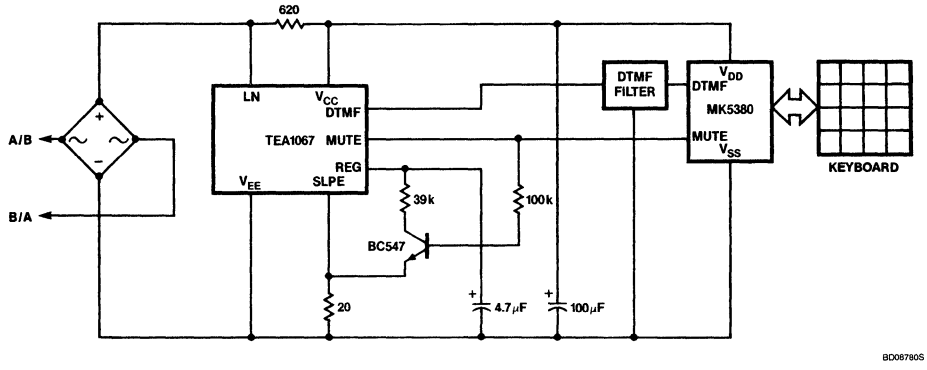


Figure 13. TEA1067 Used in Combination With a 5380 DTMF Dialer

Notice that the power-down function of the TEA1067 remains fully operative in this case, since the connection between the pins REG and SLPE is now removed.

In Figure 12, the line voltage after initial switch-on and during and after pulse dialing is shown.

TWO PRACTICAL EXAMPLES

In the preceding text we have considered several possibilities to increase the supply capabilities of the TEA1067. Now we will look at two practical examples.

The use of a TEA1067 with a CMOS DTMF dialer (5380 in this case) will be considered. Later, the use of a TEA1067 with the PCD3315 repertory dialer and PCD3312 DTMF dialer will be discussed.

TEA1067 Plus MK5380 CMOS DTMF Dialer

The schematic circuit of this combination is shown in Figure 13.

Since an MK5380 in standby mode consumes only 150μA maximally at 2.5V, it can be powered directly from the TEA1067 supply point using the standard supply resistor of 620Ω when the telephone set is in its speech mode.

However, in the dial mode, the supply current of an MK5380 can be as high as 2mA at 2.5V, while the TEA1067 can deliver only 1mA at this voltage (Figure 2). Therefore, in the dial mode an increase of the line voltage of 1mA × 620Ω is required. This will result in a voltage over the telephone set that falls in the conditionally acceptable region of Figure 1 which is allowed during DTMF dialing. This increase of voltage can be achieved according to the circuit given in Figure 10b using a resistor of 39kΩ (Figure 7) between pin REG of the TEA1067 and the collector of the BC547. The transistor can be controlled directly by the MUTE signal of the 5380.

As an alternative, the 39kΩ resistor can be connected directly between the pins REG and SLPE of the TEA1067 in combination with the Schottky diode bridge of Figure 6b. This will also result in a line voltage which is in the acceptable region of Figure 1.

If a conventional telephone set is connected in parallel to the circuit of Figure 13, the supply voltage for the 5380 dialer can drop to below 2V. Since its minimum supply voltage is 2.5V, proper DTMF tones generation can't be guaranteed under these circumstances.

TEA1067 Plus PCD3315 and PCD3312

Since it is not allowed to have a line voltage which falls into the conditionally acceptable region of Figure 1 during pulse dialing, it is not possible to use the approach described previously here. Therefore, the principle of Figure 11 has been chosen for this example. In Figure 14, the schematic diagram of the circuitry used is shown.

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Supply of Peripheral Circuits With the TEA1067 Speech Circuit AN1943

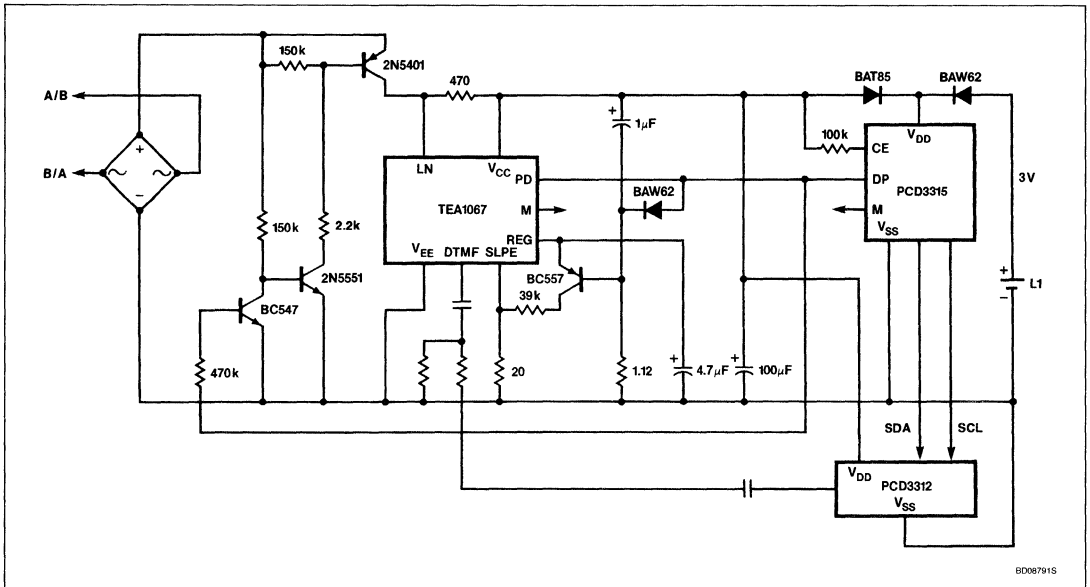

Figure 14. TEA1067 Used With PCD3315 and PCD3312

The minimum supply voltage of the PCD3315 and the PCD3312 is 2 5V Since the PCD3315 has to be powered via a series (Schottky) diode, the minimum supply point voltage of the TEA1067 allowed is 2 9V. At this voltage the TEA1067 can deliver only 300µA (Figure 2) Although the maximum supply current of the PCD3315 during pulse dialing is not specified yet, 700µA seems to be a reasonable value According to Figure 8, this can be reached by using a supply resistor of 470Ω instead of 602Ω. Using a bipolar interrupter with an impedance of 2.2kΩ, this will result in a balance return loss of still 13dB according to Figure 9.

In the case of DTMF dialing, the PCD3312 must also be powered. This can be achieved by increasing the line voltage of the TEA1067. The maximum operating current of the PCD3312 is specified as 1 2mA at 3.0V Using a supply resistor of 470Ω, an extra 1.2mA can be gained by increasing the line voltage with 1.2mA × 470Ω = 0.6V. This results in a resistor of 39kΩ between pins REG and SLPE of the TEA1067.

Since the supply resistor in Figure 14 has been reduced from 620Ω to 470Ω, a lot of components around the TEA1067 have to be adapted to the new situation. The sending gains and the sidetone are especially influenced by this measure.

If a conventional telephone set is connected in parallel with the circuit of Figure 14, the supply point voltage might drop to below 2V As a result, the PCD3312 receives a too-low supply voltage, and improper generation of DTMF tones might occur. For the PCD3315, however, there won't be a problem. If the supply point voltage drops too far, it simply continues to operate on battery power (unless the CE voltage becomes too low) Of course, the lifetime of the battery will be decreased considerably in this way

NOTE:

For information on discrete semiconductors used in this application note, contact Amperex Electronic Corp Smithfield, RI (401) 232-0500

This application note was originally published as Laboratory Report ETT8602, in April 1986 The report was written by J V Tiggelen at C A B -ELCOMA, The Netherlands

Signetics

TEA1068
Versatile Telephone Transmission Circuit

Product Specification

Linear Products

DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully-electronic telephone sets. The circuit internally performs electronic switching between dialing and speech.

FEATURES

- **Voltage regulator with adjustable static resistance**
- **Provides supply for external circuitry**
- **Symmetrical high-impedance inputs (64kΩ) for dynamic, magnetic or piezoelectric microphones**
- **Asymmetrical high-impedance input (32kΩ) for electret microphone**
- **DTMF signal input with confidence tone**
- **Mute input for pulse or DTMF dialing**
- **Power-down input for pulse dial or register recall**
- **Receiving amplifier for magnetic, dynamic or piezoelectric earpieces**
- **Large amplification setting range on microphone and earpiece amplifiers**
- **Line loss compensation facility, line current dependent for microphone and receiving amplifiers**
- **Gain control adaptable to exchange supply**
- **Possibility to adjust the DC line voltage**

APPLICATION

- **Electronic telephone sets**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−25°C to +75°C	TEA1068PN
20-Pin SOL (SOT-163)	−25°C to +75°C	TEA1068TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{LN}	Positive line voltage (DC)	12	V
V_{LN}	Repetitive line voltage during switch-on or line interruption	13.2	V
V_{LNRM}	Repetitive peak line voltage t_P/P = 1ms/5s; R_{10} = 13Ω; R_9 = 20Ω (see Figure 8)	28	V
I_{LINE}	Line current	140	mA
V_I $-V_I$	Voltage on all other pins	V_{CC} +0.7 0.7	V V
P_{TOT}	Total power dissipation	640	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +75	°C

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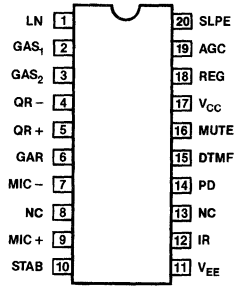
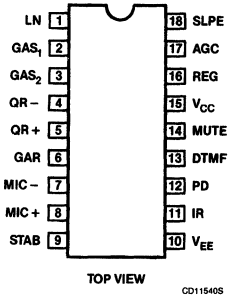
Versatile Telephone Transmission Circuit | TEA1068

PIN CONFIGURATION

D[1] Package



N Package

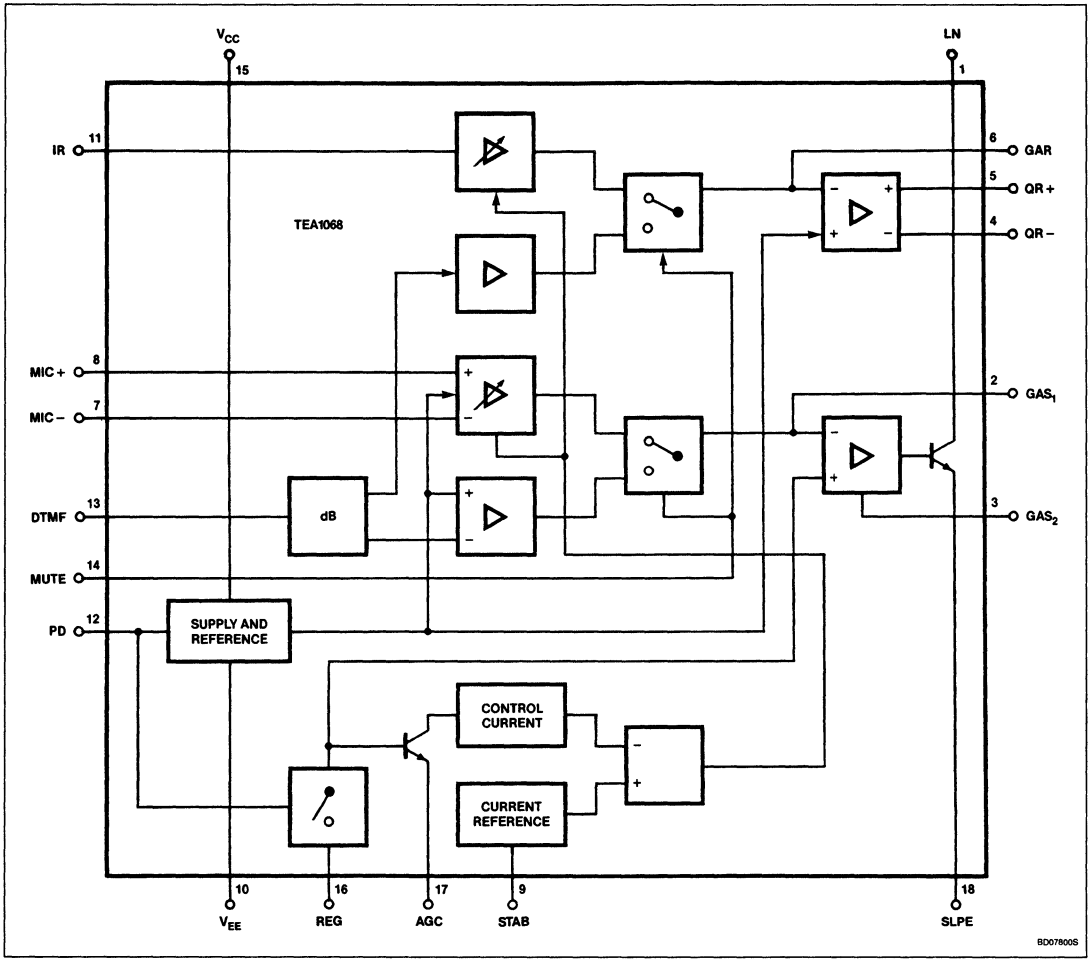


NOTE:
1 Available only in large SO package (SOL) with different pinout

PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line terminal
2	GAS_1	Gain adjustment, transmitting amplifier
3	GAS_2	Gain adjustment, transmitting amplifier
4	QR–	Inverting output, receiving amplifier
5	QR+	Non-inverting output, receiving amplifier
6	GAR	Gain adjustment, receiving amplifier
7	MIC–	Inverting microphone input
8	NC	Not connected
9	MIC+	Non-inverting microphone input
10	STAB	Current stabilizer
11	V_{EE}	Negative line terminal
12	IR	Receiving amplifier input
13	NC	Not connected
14	PD	Power-down input
15	DTMF	Dual-tone multi-frequency input
16	MUTE	Mute input
17	V_{CC}	Positive supply decoupling
18	REG	Voltage regulator decoupling
19	AGC	Automatic gain control input
20	SLPE	Slope (DC resistance) adjustment

PIN NO.	SYMBOL	DESCRIPTION
1	LN	Positive line connection
2	GAS_1	Gain adjustment connection, sending amplifier
3	GAS_2	Gain adjustment connection, sending amplifier
4	QR–	Inverting output, receiving amplifier
5	QR+	Non-inverting output, receiving amplifier
6	GAR	Gain adjustment connection, receiving amplifier
7	MIC+	Non-inverting microphone input
8	MIC–	Inverting microphone input
9	STAB	Current stabilizer connection
10	V_{EE}	Negative line connection
11	IR	Receiving amplifier input
12	PD	Power-down input
13	DTMF	Dual-tone multi-frequency input
14	MUTE	Mute input
15	V_{CC}	Positive supply decoupling connection
16	REG	Voltage regulator decoupling connection
17	AGC	Automatic gain control input
18	SLPE	Slope (DC resistance) adjustment connection

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS $I_{LINE} = I_1 = 10$ to 140mA; $V_{EE} = V10 = 0V$; f = 800Hz; R9 = 20Ω; $T_A = 25°C$, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply: LN and V_{CC} (Pins 1 and 15)					
	Voltage drop over circuit V_{1-10} microphone inputs open				
V_{LN}	at I_{LINE} = 5mA	3.95	4.25	4.55	V
V_{LN}	at I_{LINE} = 15mA	4.20	4.45	4.70	V
V_{LN}	at I_{LINE} = 100mA	5.4	6.1	7	V
V_{LN}	at I_{LINE} = 140mA			8	V
$\Delta V_{LN}/\Delta T$	Variation with temperature I_{LINE} = 15mA	−4	−2	0	mV/°C
	Voltage drop over circuit at I_{LINE} = 15mA				
V_{LN}	$R_{VA} = R_{1-16} = 68k\Omega$	3.45	3.80	4.10	V
V_{LN}	$R_{VA} = R_{16-18} = 39k\Omega$	4.65	5.0	5.35	V
	Supply current				
I_{CC}	PD (Pin 12) = LOW, V_{CC} = 2.8V		0 96	1.30	mA
I_{CC}	PD (Pin 12) = HIGH; V_{CC} = 2 8V		55	82	μA
Microphone inputs MIC+ and MIC− (Pins 8 and 7)					
	Input impedance				
$\lvert Z_{IS} \rvert$	differential (between Pins 7 and 8)	51	64	77	kΩ
$\lvert Z_{IS} \rvert$	single-ended (Pins 7 − 10 or Pins 8 − 10)	25.5	32	38.5	kΩ
CMRR	Common-mode rejection ratio		82		dB
A_{VD}	Voltage amplification (Pins 7, 8-1) at I_{LINE} = 15mA, R7 = 68kΩ	51	52	53	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency at f = 300 to 3400Hz	−0.5	±0.2	+0.5	dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA, $T_A = -25°C$ to +75°C		±0.2		dB
Dual-tone multi-frequency input DTMF (Pin 13)					
$\lvert Z_{IS} \rvert$	Input impedance	16 8	20.7	24.6	kΩ
A_{VD}	Voltage amplification at I_{LINE} = 15mA, R7 = 68kΩ	24.5	25.5	26.5	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency at f = 300 to 3400Hz	−0.5	±0.2	+0.5	dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA, $T_A = -25°C$ to +75°C		±0.2		dB
Gain adjustment GAS1 and GAS2 (Pins 2 and 3)					
ΔA_{VD}	Amplification variation with R7 transmitting amplifier	−8		+8	dB
Transmitting amplifier output LN (Pin 1)					
	Output voltage at I_{LINE} = 15mA,				
$V_{LN(RMS)}$	d_{TOT} = 2%	1.9	2.3		V
$V_{LN(RMS)}$	d_{TOT} = 10%		2.6		V
$V_{NO(RMS)}$	Noise output voltage I_{LINE} = 15mA; R7 = 68kΩ, R_{7-8} = 200Ω psophometrically weighted (P53 curve)		−72		dBmp

DC ELECTRICAL CHARACTERISTICS (Continued) $I_{LINE} = I_1 = 10$ to 140mA; $V_{EE} = V10 = 0V$; f = 800Hz; R9 = 20Ω; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Receiving amplifier input IR (Pin 11)					
$\|Z_{IS}\|$	Input impedance	16.5	20.4	24.3	kΩ
Receiving amplifier outputs QR+ and QR– (Pins 5 and 4)					
$\|Z_{OS}\|$	Output impedance; single-ended		4		Ω
	Voltage amplification from Pin 11 to Pins 4 or 5 I_{LINE} = 15mA; R4 = 100kΩ;				
A_{VD}	single-ended; R_L = 300Ω	24	25	26	dB
A_{VD}	differential; R_L = 600Ω	30	31	32	dB
$\Delta A_{VD}/\Delta f$	Variation with frequency, f = 300 to 3400Hz	–0.5	±0.2	+0.5	dB
$\Delta A_{VD}/\Delta T$	Variation with temperature at I_{LINE} = 50mA; T_A = –25 to +75°C		±0.2		dB
	Output voltage at $I_{CC} = 0$; d_{TOT} = 2%; R4 = 100kΩ; sine-wave drive	0.3	0.38		V
$V_{O(RMS)}$	single-ended; R_L = 150Ω				
$V_{O(RMS)}$	single-ended; R_L = 450Ω	0.4	0.52		V
$V_{O(RMS)}$	differential; C_L = 47nF; (100Ω series resistor); f = 3400Hz	0.8	1.0		V
	Noise output voltage at I_{LINE} = 15mA; R4 = 100kΩ; Pin 11 = IR = open Psophometrically weighted (P53 curve)				
$V_{NO(RMS)}$	single-ended; R_L = 300Ω		50		μV
$V_{NO(RMS)}$	differential; R_L = 600Ω		100		μV
Gain adjustment GAR (Pin 6)					
ΔA_{VD}	Amplification variation with R4 between Pins 6 and 5 receiving amplifier	–8		+8	dB
MUTE input (Pin 14)					
V_{IH}	Input voltage HIGH	1.5		V_{CC}	V
V_{IL}	LOW			0.3	V
I_{MUTE}	Input current		8	15	μA
A_{VD}'	Reduction of voltage amplification MIC+ and MIC– to LN at MUTE = HIGH		70		dB
A_{VD}	Voltage amplification from DTMF to QR+ or QR– to LN at MUTE = HIGH R4 = 100kΩ; R_L single-ended = 300Ω	–21	–19	–17	dB
Power-down input PD (Pin 12)					
V_{IH}	Input voltage HIGH	1.5		V_{CC}	V
V_{IL}	LOW			0.3	V
I_{PD}	Input current		5	10	μA
Automatic gain control AGC (Pin 17)					
$-\Delta A_{VD}$	Controlling the gain from Pin 11 to Pins 4 and 5 and the gain from Pins 7 and 8 to Pin 1 R6 = 110kΩ; connected between Pins 17 and 10		6		dB
	Amplification control range				
I_{LINE}	Highest line current for A_{MAX}		22		mA
I_{LINE}	Lowest line current for A_{MIN}		60		mA

6

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g., dialing and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{EXCH}, the feeding bridge resistance R_{EXCH}, the DC resistance of the subscriber line R_{LINE} and the DC voltage on the subscriber set (see Figure 1).

If the line current I_{LINE} exceeds the current I_{CC} + 0.5mA required by the circuit itself, (I_{CC} ca. 1mA), plus the current I_P required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{REF} + I_{SLPE} \times R9$$
$$= V_{REF} + (I_{LINE} - I_{CC} - 0.5 \times 10^{-3} - I_{CC}) \times R9$$

V_{REF} being an internally-generated temperature-compensated reference voltage of 4.2V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.

Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0.5mA + I_{CC}. The static behavior of the circuit then equals a 4.2V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1.

The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor connected between LN (Pin 1) and REG (Pin 16) will decrease the internal reference voltage. R_{VA} connected between REG (Pin 16) and SLPE (Pin 18) will increase the internal reference voltage. The current I_{CC} available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 2 shows this current for $V_{CC} > 2.2V$ and for $V_{CC} > 3V$. Of which 3V being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone Inputs MIC+ and MIC− and Gain Adjustment Pins GAS_1 and GAS_2

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64kΩ (2 × 32kΩ) and its voltage amplification is typical 52dB. Either dynamic, magnetic, piezoelectric microphones or an electret microphone with built-in FET source-follower can be used.

The arrangements with the microphone types mentioned are shown in Figure 3.

The amplification of the microphone amplifier can be adjusted over a range of + or −8dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS_1 and GAS_2.

An external capacitor C6 of 100pF between GAS_1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 × C6.

Mute Input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier input; a LOW level or an open-circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-Tone Multi-Frequency Input DTMF

When the DTMF input is enabled, dialing tones may be sent onto the line. The voltage amplification from DTMF to LN is typically. 25.5dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signaling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Figure 4). Amplification from IR to QR+ is typ. 25dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6dB and this makes differential drive possible. This feature can be used in case the earpiece impedance exceeds 450Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The amplification of the receiving amplifier can be adjusted over a range of + and −8dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 (100pF) and C7 (10 × C4 = 1nF) are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 × C4.

Automatic Gain Control Input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6dB. This corresponds with a line length of 5km for a 0.5mm diameter copper twisted-pair cable with a DC resistance of 176Ω/km and an average attenuation of 1.2dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Figure 5 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-Down Input PD

During pulse dialing or register recall (timed loop break), the telephone line is interrupted; as a consequence, it provides no supply for the transmission circuit and the peripherals connected to V_{CC} These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typically 1mA to typically 55μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialing or register recall. When this facility is not required PD may be left open.

Side-Tone Suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R1 // Z_{LINE}, R2, R3, R8, R9 and Z_{BAL} (see Figure 8). Maximum compensation is obtained when the following conditions are fulfilled.

a) R9.R2 = R1(R3 + [R8//Z_{BAL}])

b) [Z_{BAL}/(Z_{BAL} + R8)] = [Z_{LINE}/(Z_{LINE} + R1)].

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that | R8//Z_{BAL}| ≪ R3.

To obtain optimum side tone suppression, condition b) has to be fulfilled resulting in.

$Z_{BAL} = (R8/R1)Z_{LINE} = k.Z_{LINE}$

where k is a scale factor k = (R8/R1).

Scale factor k (value of R8) must be chosen to meet the following criteria.

- compatibility with a standard capacitor from the E6 or E12 range for Z_{BAL}
- $|Z_{BAL}//R8| \ll R3$
- $|Z_{BAL} + R8| \gg R9$

In practice, Z_{LINE} varies strongly with line length and cable type; consequently, an average value has to be chosen for Z_{BAL}. The suppression further depends on the accuracy with which Z_{BAL}/k equals the average line impedance.

The anti-side-tone network as used in the standard application (Figure 8) attenuates the signal from the line with 32dB. The attenuation is nearly flat over the audio frequency range.

Instead of the above described special TEA1068 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

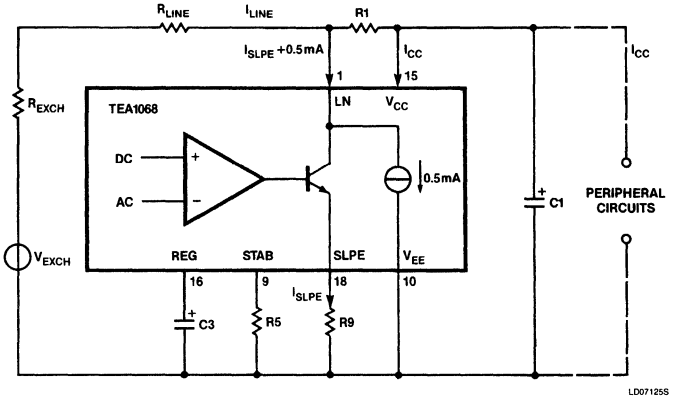
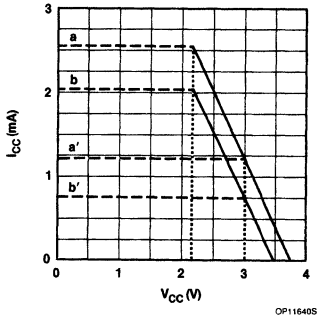


Figure 1. Supply Arrangement



NOTES:
Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE is HIGH, curves (b) and (b') are valid when MUTE is LOW and the receiving amplifier is driven at $V_{O(RMS)}$ = 150mV and R_L = 150Ω asymmetrical
I_{LINE} = 15mA at V_{LN} = 4 45V, R1 = 620Ω and R9 = 20Ω
a) = 2 55mA, b) = 2 1mA, a') = 1 2mA and b') = 0 75mA

Figure 2. Maximum Current I_{CC} Available from V_{CC} for Peripheral Circuitry with V_{CC} > 2.2V and V_{CC} > 3V

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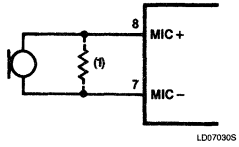
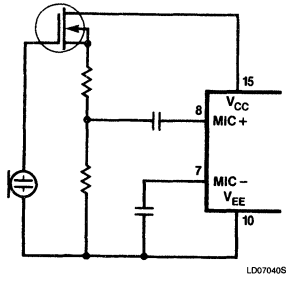
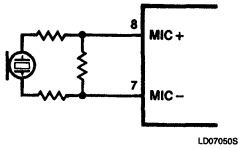


NOTE:
The resistor marked (1) may be connected to lower the terminating impedance In case of sensitive microphone types, a resistor attenuator can be used to prevent overloading of the microphone inputs

a. Magnetic or Dynamic Microphone

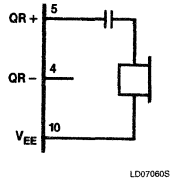


b. Electret Microphone

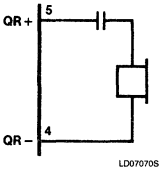


c. Piezoelectric Microphone

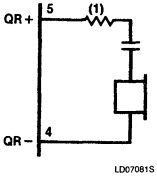
Figure 3. Alternative Microphone Arrangements



a. Dynamic Telephone with Less Than 450Ω Impedance

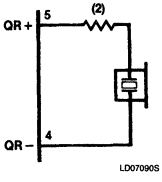


b. Dynamic Telephone with More Than 450Ω Impedance



NOTE:
The resistor marked (1) may be connected to prevent distortion (inductive load)

c. Magnetic Telephone with More Than 450Ω Impedance



NOTE:
The resistor marked (2) is required to increase the phase margin (capacitive load)

d. Piezoelectric Telephone

Figure 4. Alternative Receiver Arrangements

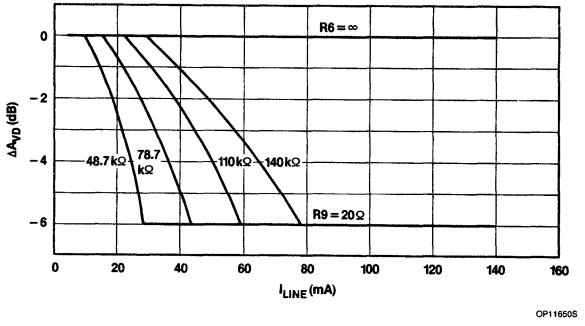
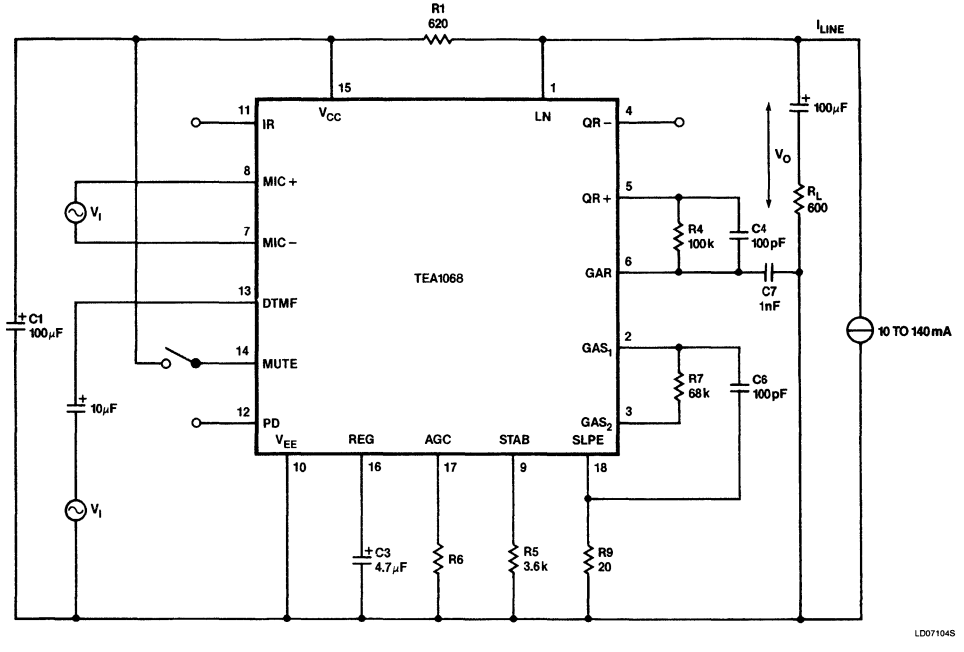


Figure 5. Variation of Amplification with Line Current, with R6 as a Parameter

Table 1. Values of Resistor R6 for Optimum Line Loss Compensation, for Various Usual Values of Exchange Supply Voltage V_{EXCH} and Exchange Feeding Bridge Resistance R_{EXCH}.

		R_{EXCH} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{EXCH} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

NOTE:
R9 = 20Ω



NOTES:
Voltage amplification is defined as $A_{VD} = 20 \log|V_O/V_I|$
For measuring the amplification from MIC+ and MIC–, the MUTE input should be LOW or open, for measuring the DTMF input, MUTE should be HIGH
Inputs not under test should be open

Figure 6. Test Circuit for Defining Voltage Amplification of MIC+, MIC– and DTMF Inputs

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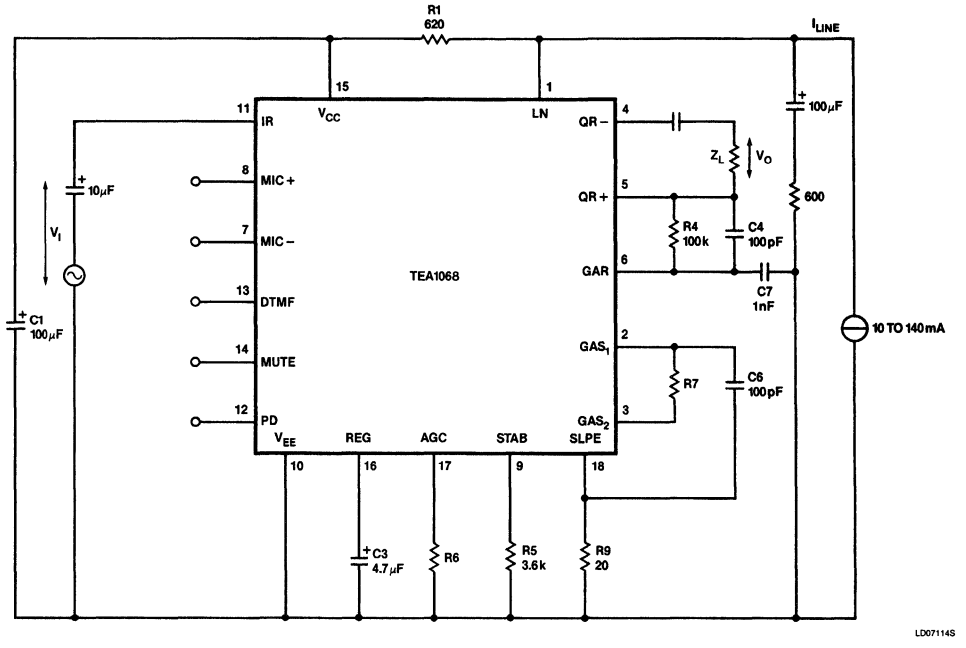
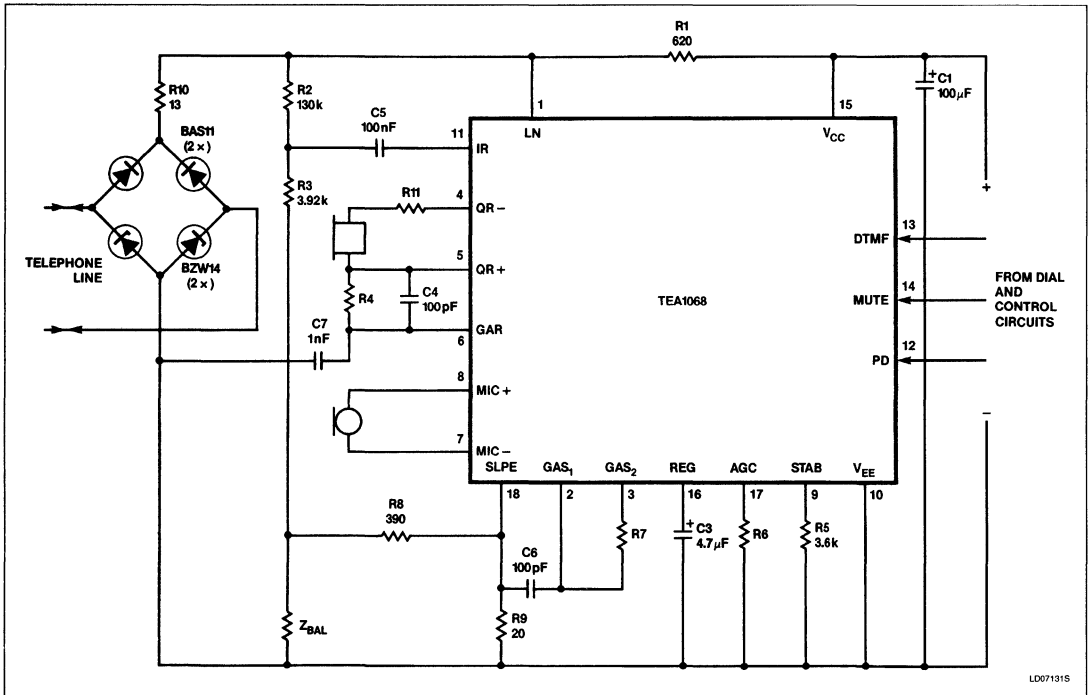
Versatile Telephone Transmission Circuit TEA1068



NOTE:
Voltage amplification is defined as $A_{VD} = 20\log|V_O/V_I|$.

Figure 7. Test Circuit for Defining Voltage Amplification of the Receiving Amplifier

APPLICATION INFORMATION



NOTES:
The bridge to the left, the zener diode and R10 limit the current and the voltage into the circuit during the transients
Pulse dialing or register recall require a different protection arangement

Figure 8. Typical Application of the TEA1068, Shown Here with a Piezoelectric Earpiece and DTMF Dialing

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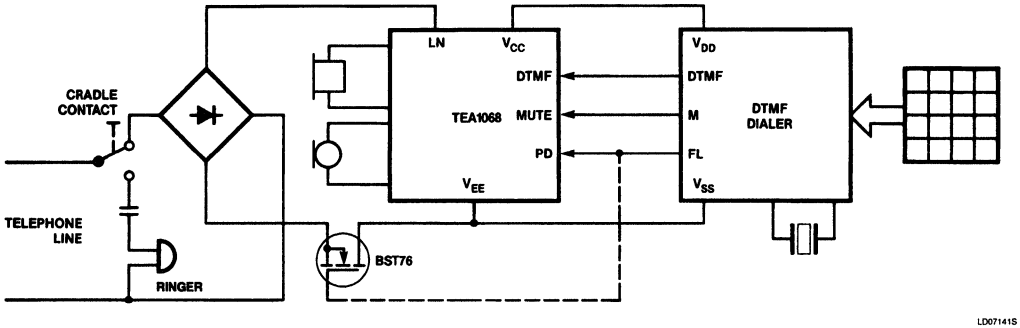
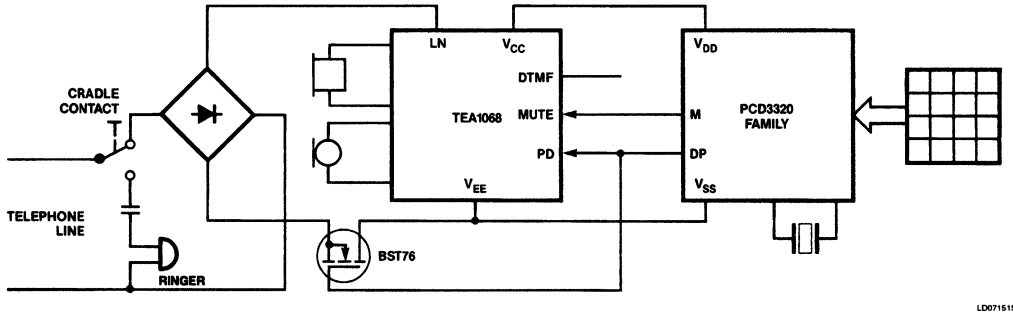
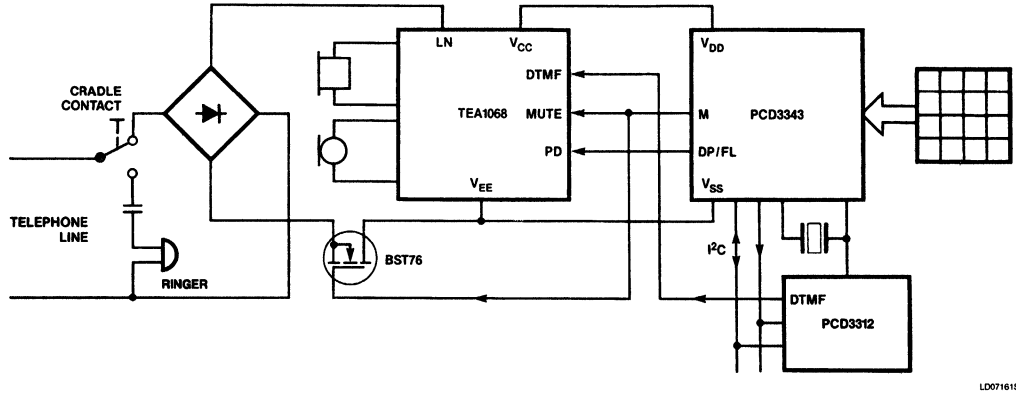


NOTE:
The dashed lines show an optional flash (register recall by times loop back)

a. DTMF Set with a CMOS DTMF Dialing Circuit



b. Pulse Dial Set with One of the PCD3320 Family of CMOS Interupted Current Loop Dialing Circuits



c. Dual-Standard (Pulse and DTMF) Feature Phone with the PCD3343 CMOS Telephone Controller and the PCD3312 CMOS DTMF Generator with I^2C Bus

Figure 9. Typical Applications of the TEA1068 (Simplified)

Signetics

Linear Products

Section 7
Radio/Audio

INDEX

Signetics

TDA1072A
AM Receiver Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA1072A integrated AM receiver circuit performs the active function and part of the filtering function of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50MHz and can handle RF signals up to 500mV. RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

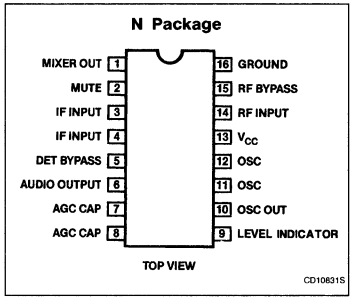
FEATURES

- **Inputs protected against damage by static discharge**
- **Gain-controlled RF stage**
- **Double-balanced mixer**
- **Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils**
- **Gain-controlled IF stage with wide AGC range**
- **Full-wave, balanced envelope detector**
- **Internal generation of AGC voltage with possibility of second-order filtering**
- **Buffered field-strength indicator driver with short-circuit protection**
- **AF preamplifier with possibilities for simple AF filtering**
- **Electronic standby switch**

APPLICATIONS

- **AM receiver**
- **Communications receiver**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	TDA1072AN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{13-16}$	Supply voltage	20	V
P_{TOT}	Total power dissipation	875	mW
V_{14-15}	Input voltage	12	V
V_{14-16}, V_{15-16}		V_{CC}	V
$\|I_{14}\|$, $\|I_{15}\|$	Input current	200	mA
T_A	Operating ambient temperature range	−40 to +80	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	+125	°C
θ_{JA}	Thermal resistance from junction to ambient	80	°C/W

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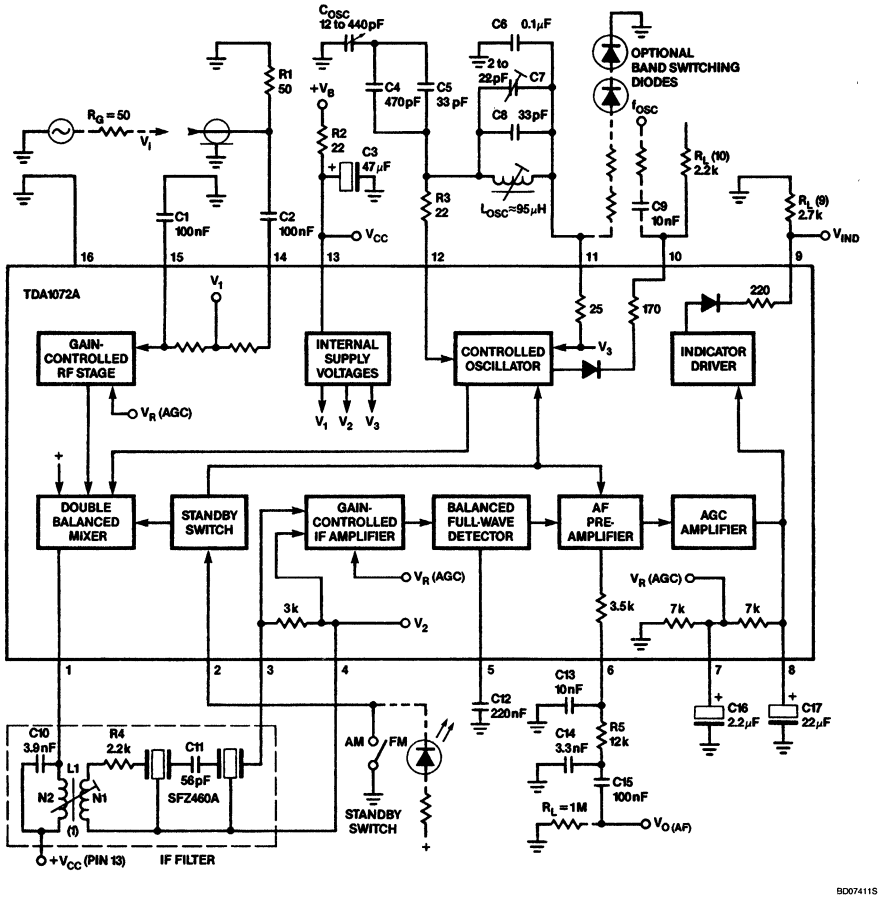
AM Receiver Circuit | TDA1072A

BLOCK DIAGRAM



NOTES:
1. Coil Data TOKO sample no 7XNS-A7523DY, L1 N1/N2 = 12/32, Q_O = 65, Q_B = 57
2. Filter Data Z_F = 700Ω at R_{3-4} = 3kΩ, Z_I = 4.8kΩ

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{13-16} = 8.5V$; $T_A = 25°C$; $f_I = 1MHz$; $f_M = 400Hz$; $m = 30\%$; $f_{IF} = 460kHz$; measured in Block Diagram and Test Circuit, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
$V_{CC} = V_{13-16}$	Supply voltage	7.5	8.5	18	V
$I_{CC} = I_{13}$	Supply current	15	23	30	mA
RF stage and mixer					
V_{14-16}, V_{15-16}	Input voltage (DC value)		$V_{CC}/2$		V
R_{14-16}, R_{15-16}	RF input impedance at $V_I < 300\mu V$		5.5		kΩ
C_{14-16}, C_{15-16}			25		pF
R_{14-16}, R_{15-16}	RF input impedance at $V_I > 10mV$		8		kΩ
C_{14-16}, C_{15-16}			22		pF
R_{1-16}	IF output impedance	500			kΩ
C_{1-16}			6		pF
I_1/V_I	Conversion transconductance before start of AGC		6.5		mA/V
$V_{1-13(P-P)}$	Maximum IF output voltage, inductive coupling to Pin 1		5		V
I_1	DC value of output current (Pin 1) at $V_I = 0V$		1.2		mA
	AGC range of input stage		30		dB
$V_{I(RMS)}$	RF signal handling capability: input voltage for THD = 3% at m = 80%		500		mV
Oscillator					
f_{OSC}	Frequency range	0.6		60	MHz
V_{11-12}	Oscillator amplitude (Pins 11 to 12)		130	150	mV
$R_{12-11\ (EXT)}$	External load impedance	0.5		200	kΩ
$R_{12-11\ (EXT)}$	External load impedance for no oscillation			60	Ω
RR	Ripple rejection at $V_{CC(RMS)} = 100mV$; $f_p = 100Hz$ ($RR = 20 \log [V_{13-16}/V_{11-16}]$)		55		dB
V_{11-16}	Source voltage for switching diodes ($6 \times V_{BE}$)		4.2		V
$-I_{11}$	DC output current (for switching diodes)	0		20	mA
ΔV_{11-16}	Change of output voltage at $\Delta I_{11} = 20mA$ (switch to maximum load)		0.5		V
Buffered oscillator output					
V_{10-16}	DC output voltage		0.7		V
$V_{10-16(P-P)}$	Output signal amplitude		320		mV
R_{10}	Output impedance		170		Ω
$-I_{10(PEAK)}$	Output current			3	mA

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DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{13-16} = 8.5V$; $T_A = 25°C$; $f_I = 1MHz$; $f_M = 400Hz$; $m = 30\%$; $f_{IF} = 460kHz$; measured in Block Diagram and Test Circuit, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
IF, AGC, and AF stages					
V_{3-16}, V_{4-16}	DC input voltage		2.0		V
R_{3-4}	IF input impedance	2.4	3	3.9	kΩ
C_{3-4}	IF input impedance		7		pF
V_{3-4}	IF input voltage for THD = 3% at m = 80%		90		mV
V_{3-4}/V_{6-16}	Voltage gain before start of AGC		68		dB
ΔV_{3-4}	AGC range of IF stages; change of V_{3-4} for 1dB change of $V_{O(AF)}$; $V_{3-4\ (REF)} = 75mV$		55		dB
$V_{O(AF)}$	AF output voltage at $V_{3-4(IF)} = 50\mu V$		130		mV
$V_{O(AF)}$	AF output voltage at $V_{3-4(IF)} = 1mV$		310		mV
$\lvert Z_O \rvert$	AF output impedance (Pin 6)		3.5		kΩ
Indicator driver					
V_{9-16}	Output voltage at $V_I = 0mV$; $R_{L(9)} = 2.7k\Omega$		20	150	mV
V_{9-16}	Output voltage at $V_I = 500mV$; $R_{L(9)} = 2.7k\Omega$	2.5	2.8	3.1	V
$R_{L(9)}$	Load resistance	1.5			kΩ
Standby switch					
	Switching threshold at $V_{CC} = 7.5$ to 18V; $T_A = -40$ to $+80°C$				
$V_2 - 16$	on – voltage	0		2.0	V
$V_2 - 16$	off – voltage	3.5		20	V
$-I_2$	on – current at $V_{2-16} = 0V$			200	μA
$\lvert I_2 \rvert$	off – current at $V_{2-16} = 20V$			10	μA

OPERATING CHARACTERISTICS V_{CC} = 8.5V; f_I = 1MHz; m = 30%; f_M = 400Hz; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
RF sensitivity					
V_I	RF input required for S + N/N = 6dB		1.5		μV
V_I	RF input required for S + N/N = 26dB		15		μV
V_I	RF input required for S + N/N = 46dB		150		μV
V_I	RF input at start of AGC		30		μV
RF large signal handling					
V_I	RF input at THD = 3%; m = 80%		500		mV
V_I	RF input at THD = 3%; m = 30%		700		mV
V_I	RF input at THD = 10%; m = 30%		900		mV
AGC range					
ΔV_I	Change of V_I for 1dB change of $V_{O(AF)}$; $V_{I(REF)}$ = 500mV		86		dB
ΔV_I	Change of V_I for 6dB change of $V_{O(AF)}$; $V_{I(REF)}$ = 500mV		91		dB
Output signal					
$V_{O(AF)}$	AF output voltage at V_I = 4μV; m = 80%		130		mV
$V_{O(AF)}$	AF output voltage at V_I = 1mV	240	310	390	mV
d_{TOT}	THD at V_I = 1mV; m = 80%		0.5		%
d_{TOT}	THD at V_I = 500mV; m = 30%		1		%
(S + N)/N	Signal-to-noise ratio at V_I = 100mV		58		dB
RR	Ripple rejection at V_I = 2mV; $V_{CC(RMS)}$ = 100mV; fp = 100Hz (RR = 20 log [$V_{CC}/V_{O(AF)}$])		38		dB
Unwanted signals					
	Suppression of IF whistles at V_I = 15μV; m = 0% related to AF signal of m = 30%				
α_{2IF}	at $f_J \approx 2 \times f_{IF}$		37		dB
α_{3IF}	at $f_J \approx 3 \times f_{IF}$		44		dB
	IF suppression at RF input				
α_{IF}	for symmetrical input		40		dB
α_{IF}	for asymmetrical input		40		dB
	Residual oscillator signal at mixer output				
$I_{1(OSC)}$	at f_{OSC}		1		μA
$I_{1(2OSC)}$	at 2 × f_{OSC}		1.1		μA

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FUNCTIONAL DESCRIPTION

Gain-Controlled RF Stage and Mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behavior is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the signal-to-noise ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double-balanced mixer provides the IF output signal to Pin 1.

Oscillator

The differential amplifier oscillator is temperature-compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage V_{11-16}. An extra buffered oscillator output (Pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-Controlled IF Amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF Preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter-follower with a series resistor which, together with an external capacitor, yields the required low-pass for AF filtering.

AGC Amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at Pin 7 can be omitted for low-cost applications.

Field Strength Indicator Output

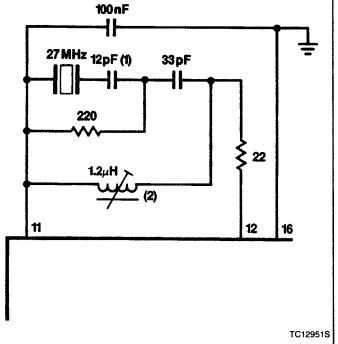
A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

Standby Switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer, and AF preamplifier are switched off.

Short-Circuit Protection

All pins have short-circuit protection to ground.



NOTES:
1. Capacitor values depend on crystal type
2. Coil Data: 9 windings of 0.1mm dia laminated Cu wire on TOKO coil set 7K 199CN, $Q_O = 80$

Figure 1. Oscillator Circuit Using Quartz Crystal; Center Frequency = 27MHz

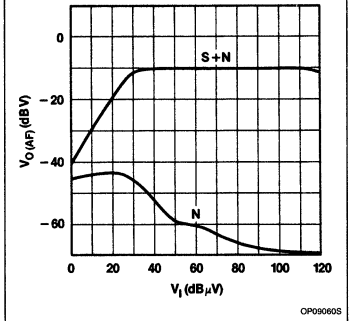


Figure 2. AF Output as a Function of RF Input in the Test Circuit; f_I = 1MHz; f_M = 400Hz; m = 30%

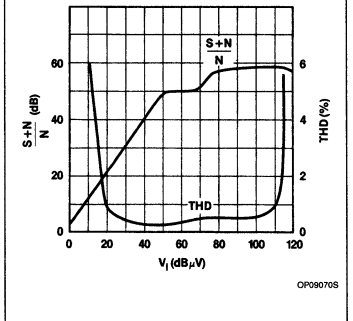


Figure 3. Total Harmonic Distortion and (S + N)/N as Functions of RF Input in the Test Circuit; m = 30% for (S + N)/N Curve and m = 80% for THD Curve

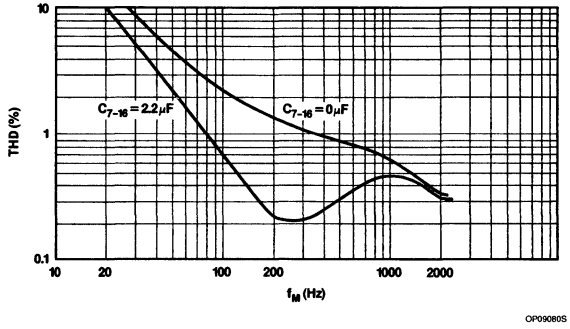


Figure 4. Total Harmonic Distortion as a Function of Modulation Frequency at V_I = 5mV; m = 80%; Measured in the Test Circuit With $C_{7-16(EXT)} = 0\mu F$ and $2.2\mu F$

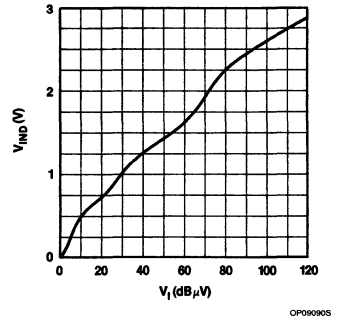
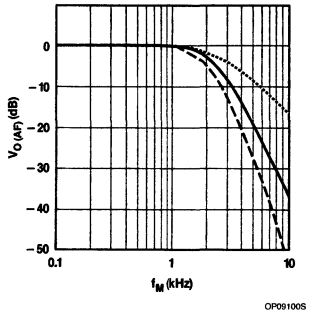


Figure 5. Indicator Driver Voltage as a Function of RF Input in the Test Circuit



NOTES:
——— With IF filter
····· With AF filter
- - - - With IF and AF filters

Figure 6. Typical Frequency Response Curves From Test Circuits Showing the Effect of Filtering

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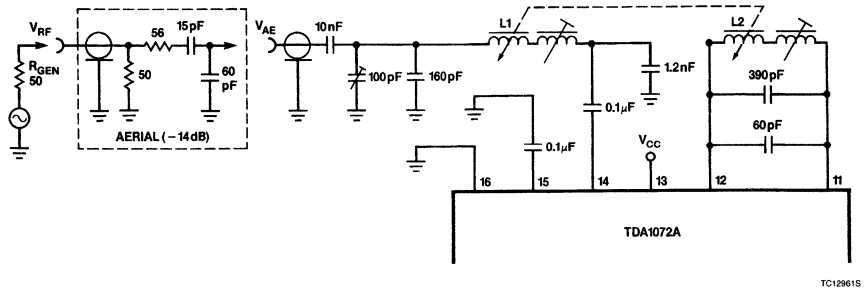


Figure 7. Car Radio Application With Inductive Tuning

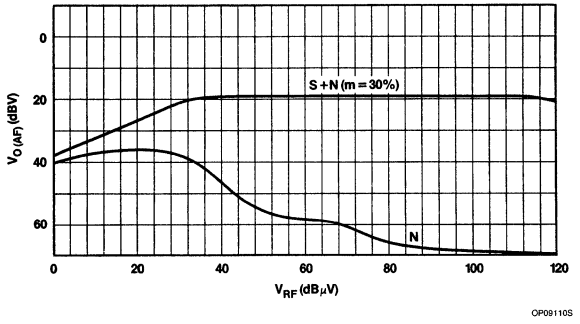
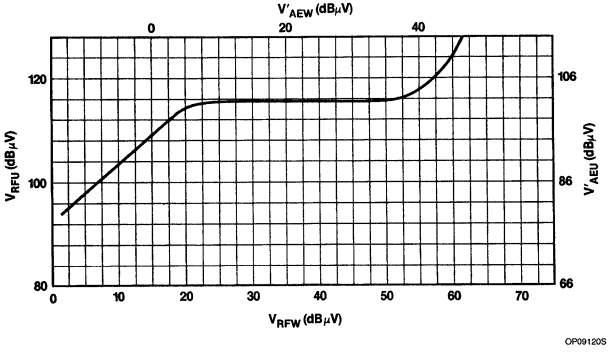


Figure 8. AF Output as a Function of RF Input Using the Circuit of Figure 7 With That of the Test Circuit



NOTES:
1 Wanted signal (V'_{AEW}, V_{RFW}) f_I = 1MHz, f_M = 400Hz, m = 30%
2 Unwanted signal (V'_{AEU}, V_{RFU} f_I = 900kHz, f_M = 400Hz, m = 30%
3 Effective selectivity of input tuned circuit = 21dB
4 Curve is for wanted $V_{o(AF)}$/unwanted $V_{o(AF)}$ = 20dB V_{RFW}, V_{RFU} are signals at the aerial input, V'_{AEW}, V'_{AEU} are signals at the unloaded output of the aerial

Figure 9. Suppression of Cross-Modulation as a Function of Input Signal, Measured in the Circuit of Figure 7 With the Input Circuit as Shown in Figure 11

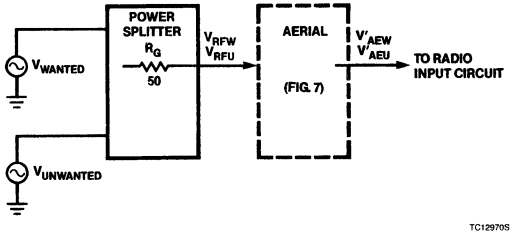


Figure 10. Input Circuit to Show Cross-Modulation Suppression (see Figure 9)

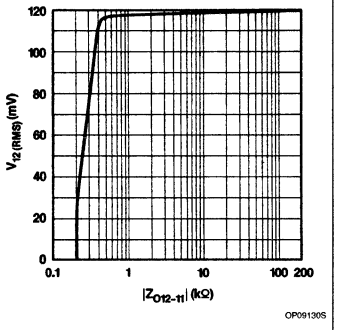


Figure 11. Oscillator Amplitude as a Function of Pins 11, 12 Impedance in the Circuit of Figure 7

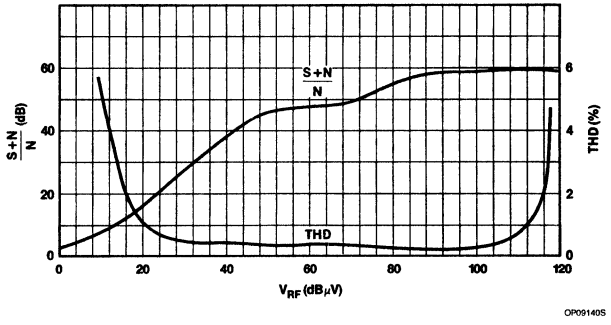


Figure 12. Total Harmonic Distortion and (S + N)/N as Functions of RF Input Using the Circuit of Figure 7 With That of Test Circuit

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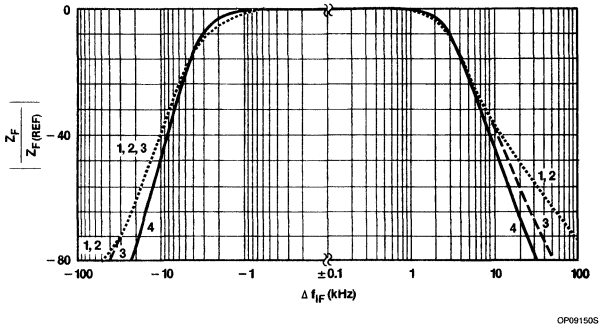
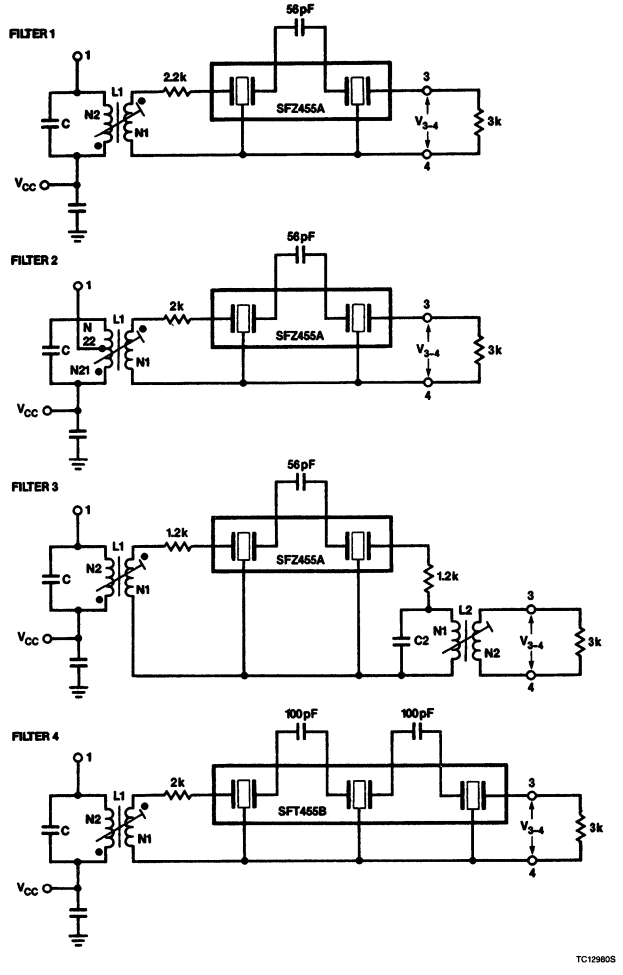


Figure 13. Forward Transfer Impedance as a Function of Intermediate Frequency for Filters 1 to 4 Shown in Figure 14, Center Frequency = 455kHz

Table 1. Data for IF Filters Shown in Figure 14

FILTER NO.	1	2	3		4	UNIT
Coil data	**L1**	**L1**	**L1**	**L2**	**L1**	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12:32	13:(33 + 66)	15.31	29:29	13:31	
Diameter of Cu laminated wire	0.09	0.08	0.09	0.08	0.09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic[1]	● ●	● ● 66	● ●	● ● 29	● ●	
of	12 ●32	13	15 ●31	29	13 ●31	
windings	● ●	● ● 33	● ●	● ●	● ●	
				(N1) (N2)		
Toko order no.	7XNS – A7523DY	L7PES – A0060BTG	7XNS – A7518DY	7XNS – A7521AIH	7XNS – A7519DY	
Resonators						
Murata Type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3dB)	4.2	4.2	4.2		4.5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4.8	3.8	4.2		4.8	kΩ
Q_B	57	40	52(L1)	18(L2)	55	
Z_F	0.70	0.67	0.68		0.68	kΩ
Bandwidth (−3dB)	3.6	3.8	3.6		4.0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

NOTE:
1 The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding
2 Criterium for adjustment is Z_F = maximum (Optimum Selectivity curve at center frequency f_o = 455kHz). See also figure 13



NOTE:
For filter data, refer to Table 1

Figure 14. IF Filter Variants Applied to the Test Circuit

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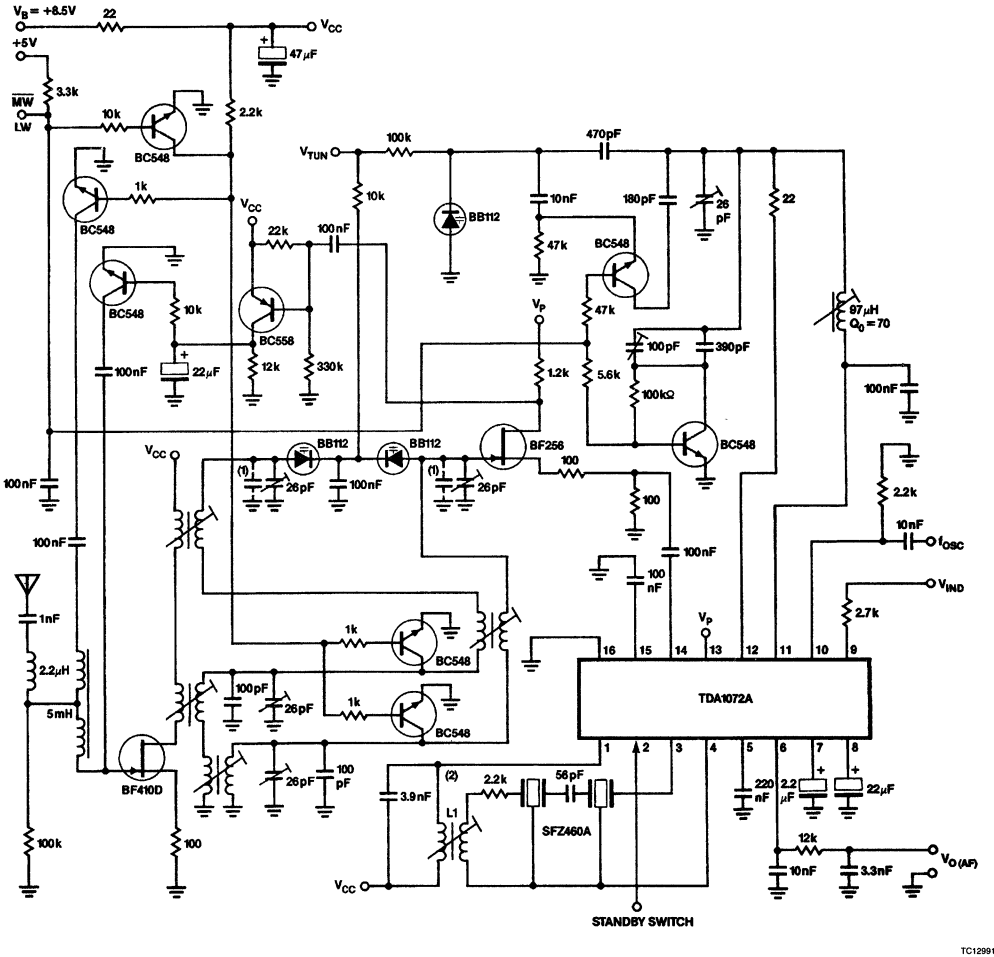


NOTES:
1 Values of capacitors depend on the selected group of capacitive diodes BB112
2 For IF filter and coil data refer to Block Diagram
3 The circuit includes pre-stage AGC optimized for good large-signal handling

Figure 15. Car Radio Application With Capacitive Diode Tuning and Electronic MW/LW Switching

Signetics

AN1961
Integrated AM TDA1072A Receiver

Application Note

Linear Products

Successor to the well-known TDA1072, the TDA1072A is an inexpensive integrated AM radio circuit that performs all the active functions between the aerial and the audio power amplifier. Its ability to handle a wide dynamic range of input signals and its low distortion make the TDA1072A suitable for use in a wide range of car radios, domestic radios, and tuners. The TDA1072A brings the TDA1072 right up-to-date to meet present trends in the design of the AM section of a radio, such as varicap diode tuning, AM stereo facility, and electronic search tuning. Performance improvements include a 6dB increase in sensitivity over most of the input signal operating range, and 55dB ripple rejection between the supply voltage and the oscillator output.

With the TDA1072A, designers have complete freedom of choice in tuning method, gain and selectivity, since none of the aerial circuit has been integrated. And the TDA1072A is ideal for use with low-cost hybrid IF filters.

Semi-professional and professional applications outside the AM broadcast bands using local oscillator frequencies up to 60MHz and down to ultrasound frequencies are also possible.

The main features of the TDA1072A are:

- High sensitivity: 15μV aerial input for 26dB signal-to-noise ratio, m = 0.3
- Large signal handling capability, low distortion and high signal-to-noise ratio
- Particularly suitable for use with varicap diode tuning owing to a constant low-level output voltage (typ. 130mV$_{RMS}$) from the local oscillator
- Separate buffered local oscillator output (320mV$_{P-P}$, Pin 10) for digital frequency synthesizers
- Internal AGC circuit with fast settling time — essential in electronic search tuning — and low distortion at low modulation frequencies
- Logarithmic field strength output for simple generation of stop pulses and for driving a signal strength indicator or meter
- Internal standby switch operated by logic levels
- Requires very few peripheral components
- Operates from supply voltages between 7.5 and 18V
- Ambient operating temperature: −40°C to +80°C.

CIRCUIT AND PERFORMANCE

Figure 1 shows the block diagram of the TDA1072A. Although basically similar to its predecessor, the TDA1072A offers:

- 6dB improvement in signal-to-noise ratio owing to redesigned input circuitry
- 55dB improvement in ripple rejection owing to redesigned oscillator circuitry
- New field strength curve optimized for LED bar indicators and easy stop pulse generation with selectable level.

The main differences in performance between the two circuits are given in Table 1.

RF Input

A redesigned input circuit gives a 6dB improvement in signal-to-noise over most of the operating range (see Figures 2 and 3). To obtain the full improvement, the source impedance of the RF input circuit should be reduced from 1.6kΩ (TDA1072) to 1kΩ (f_I = 1MHz), the latter value being a compromise between large signal capability (low cross modulation) of permeability-tuned circuits and sensitivity.

In addition, this value allows low-impedance electronically-tuned RF input stages with FETs (especially those used as source-followers) to be used. Moreover, it allows a home radio frame antenna to be connected to the TDA1072A without using a FET. The antenna forms part of the RF input circuit coil, which is a transformer directly connected to the RF input of the TDA1072A.

The input impedance at 1MHz (Pins 14 and 15, both surge-protected) is 5.5kΩ ‖ 22pF for an RF input < 300μV; 8kΩ ‖ 22pF for an input > 10mV.

Tuning behavior of the TDA1072 and TDA1072A is different owing to the former's proportional AGC and the latter's more integrating AGC. With the TDA1072, the optimal tuning position could be identified by the rapid increase of noise with detuning. With the TDA1072A, the noise only increases slowly with detuning. This is advantageous in mechanically-tuned radios since slight detuning (due to vibration, temperature) produces only a small increase in noise and distortion.

For optimal tuning and sensitivity at very low RF input signals, a 220nF metal foil capacitor should be connected between Pin 5 and ground. This replaces the 470nF electrolytic capacitor needed with the TDA1072.

Local Oscillator

The voltage-controlled oscillator provides signals of low distortion and high spectral purity even when tuned with varicap diodes. It delivers an almost constant output of typically 130mV for impedances from 500Ω to 200kΩ. Internal temperature compensation circuitry ensures ultra stable signals even on short waves. Only a few external components are required to complete the oscillator.

An additional buffered oscillator output is provided (Pin 10, 320mV$_{P-P}$; 200mV TDA1072) for use in synthesizer-tuned radios.

The oscillator of the TDA1072A is DC referenced to ground (V_{11} = 4.2V, i.e., 6V_{BE}) unlike the TDA1072 which was DC-referenced to the supply ($V_{11} = V_{13} - 1.4V$). This new arrangement has improved the ripple rejection between the supply voltage and the DC oscillator voltage by 55dB. Hence, frequency modulation of the oscillator signal due to supply voltage ripple is minimized.

NOTE:
There should always be a DC connection between Pins 11 and 12 (usually a coil or resistor) owing to internal biasing. For stability, a 100nF capacitor should be connected between Pin 11 and ground

In order to use band-switching diodes as well as transistors with the TDA1072A, Pin 11 can switch up to 20mA.

Mixer

A double-balanced mixer is used to generate the IF signal. The mixer output (Pin 1) is the collector of a transistor pair which requires a positive DC voltage. Since a resistive load would reduce the maximum IF output signal, an inductor should be used in the coupling circuit to the IF amplifier.

High IF gain allows the IF selectivity to be provided by an external hybrid or ceramic filter. Hybrid IF filters are recommended for reasons of cost. These should have a transfer impedance of

$$Z_{21} = V_{34}/I_1 = 700\Omega,$$

and an input impedance between 3kΩ and 5kΩ to prevent overloading the mixer.

7

Integrated AM TDA1072A Receiver AN1961

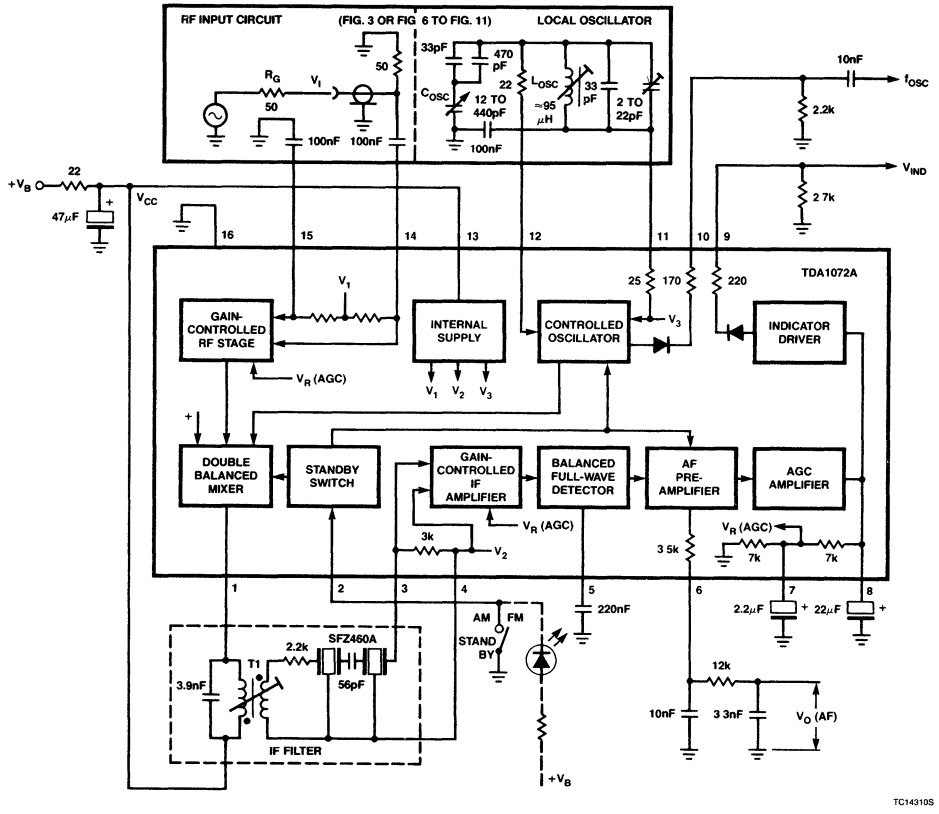


Figure 1. TDA1072A and Test Circuit

IF Amplifier and Detector

The IF amplifier comprises two cascaded differential amplifier stages with independent gain control.

The low noise full-wave balanced envelope detector provides a linear low distortion output over a wide dynamic range Residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF Preamplifier

The emitter-follower output with an internal series resistor enables external low-pass filtering of the AF signal to be designed as required.

NOTE:

In applications with ferrite rod aerials, the external capacitors should be close to the IC to minimize IF interference

AGC Amplifier

This amplifier provides a control voltage proportional to the carrier amplitude. Second-order filtering of the AGC voltage gives low distortion over the whole range of amplitudes (even at low modulation frequencies) in addition to fast settling time of the AGC — essential when this signal is used to derive stop pulses in electronic search tuning. The values of the capacitors (Pins 7 and 8) in the external filter shown in Figure 1 provide a compromise between short settling time and low distortion. Both capacitors should be positioned close to the IC and should be connected to a main ground to avoid coupling ground currents. In low cost sets, the capacitor at Pin 7 can be omitted.

An 86dB AGC control range holds the level of the AM, IF signal constant (within 1dB) over a broad range of RF input levels. In AM stereo systems, this simplifies the matrixing of the stereo difference signal.

Field Strength Indicator Output/ Stop Pulse Generation

A buffered DC output which is a logarithmic function of aerial input voltage over the full dynamic range is available for driving a field strength indicator or for generating stop pulses in search-tuning systems (Figure 4). The field strength curve of the TDA1072A (Figure 5) has been optimized for LED indicator drivers, but can still be used with meters. Up to 2mA may be drawn (Pin 9); and with an input of 500mV between Pins 14 and 15, the typical field strength output is 2.8V.

A diode is incorporated in the output stage so that a common indicator can be used to display FM and AM field strengths without the need for a switch.

Table 1. Performance of the TDA1072A and TDA1072

SYMBOL	PARAMETER	TDA1072A	TDA1072	UNIT
	Sensitivity (see also Figure 3):			
	RF input voltage[1] for			
V_I	(S + N)/N = 6dB	1.5	2.2	μV
V_I	(S + N)/N = 26dB	15	30	μV
V_I	(S + N)/N = 46dB	150	550	μV
V_I	start of AGC	30	14	μV
	Large signal handling:			
	maximum RF input voltage (Pins 14 and 15)			
V_I	d_{TOT} = 3%, m = 0.8	500	600	mV
V_I	d_{TOT} = 3%, m = 0.3	700	800	mV
V_I	d_{TOT} = 10%, m = 0.3	900	1200	mV
	AGC control range			
dV_I	for a 6dB change of V_O	91	91	dB
dV_I	1dB change of V_O	86		dB
$V_{O(AF)}$	AF output voltage at V_I = 1mV, f_I = 1MHz, m = 0.3 and f_M = 400Hz THD of AF output voltage (see Figure 3)	310	300	mV
d_{TOT}	V_I = 500mV; m = 0.3	1% (m = 0.3)	1.8% (m = 0.8)	
f_{OSC}	Oscillator frequency range	0.6 – 60[2]	0.6 – 60	MHz
$-I_{11}$ max.	Oscillator output current	20	15	mA
dV_{11}/dV_{13}	Ripple rejection	55	0	dB
	Field strength indication range	114	114	dB

NOTES:
All values are typical and measured in the circuit of Figure 1 unless otherwise specified.
1. V_{CC} = 8.5V (TDA1072A), 15V (TDA1072); f_I = 1MHz, f_M = 400Hz; m = 0.3.
2. Operation at < 0.6MHz possible.

7

Integrated AM TDA1072A Receiver AN1961

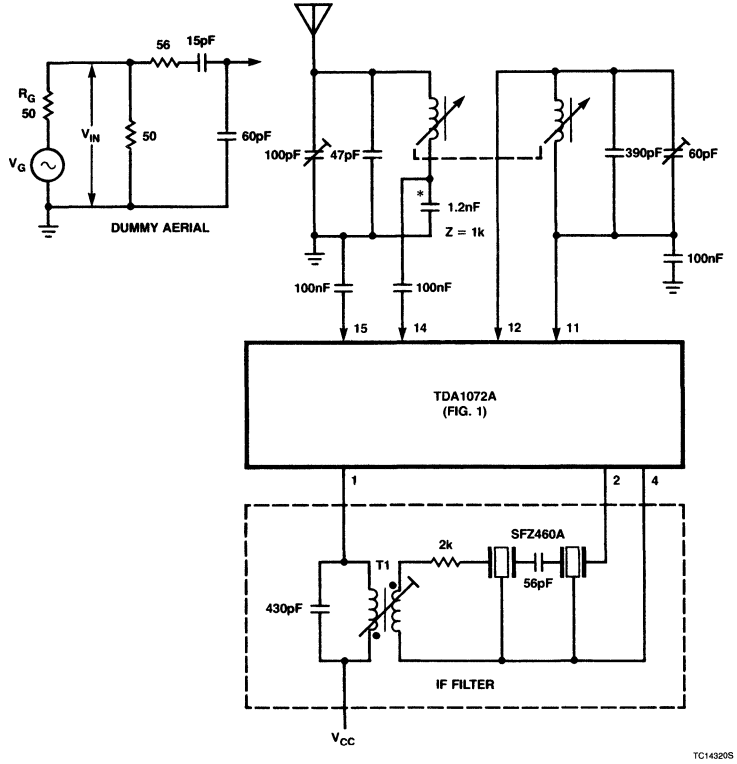


Figure 2. Aerial Local Oscillator Circuits for a Permeability-Tuned Medium-Wave Car Radio Whose Performance is Shown in Figure 3

Internal Supply Voltage

An internal hum filter is completed by connecting a 47μF electrolytic capacitor to Pin 13. The connections from the capacitor to Pin 13 and to the IF filter should be short.

APPLICATIONS

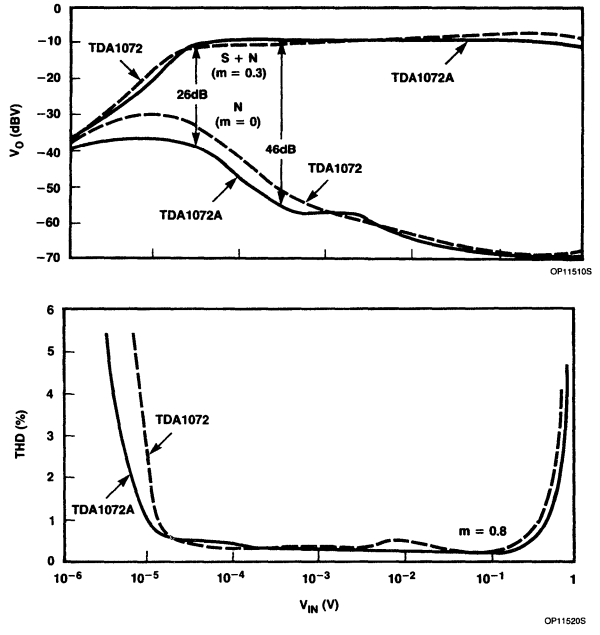
Existing designs using the TDA1072 can usually be upgraded using the TDA1072A. However, some circuits may have to be modified owing to different DC levels (Table 2) and the new field strength curve.

Figures 6 to 11 give an indication of the applications possible with the TDA1072A.

Table 2. Difference in DC Voltages Between the TDA1072A and TDA1072, Supply 8.5V

PIN	TDA1072A	TDA1072
10	10.7	4.5
11 & 12	4.2	7.2
14 & 15	4.2	2.7

NOTE:
All other voltages remain unaltered



NOTE:
f_M = 400Hz, V_{CC} = 8.5V

Figure 3. Performance of the AM Section of the Car Radio Circuitry Shown in Figure 2

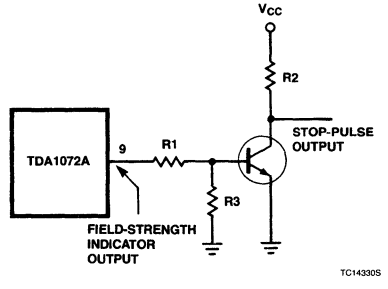


Figure 4. Simple Stop Pulse Generation Circuit

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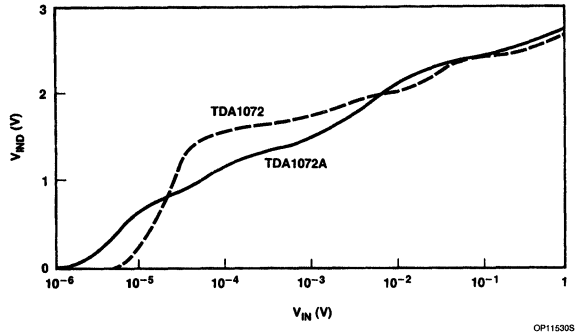
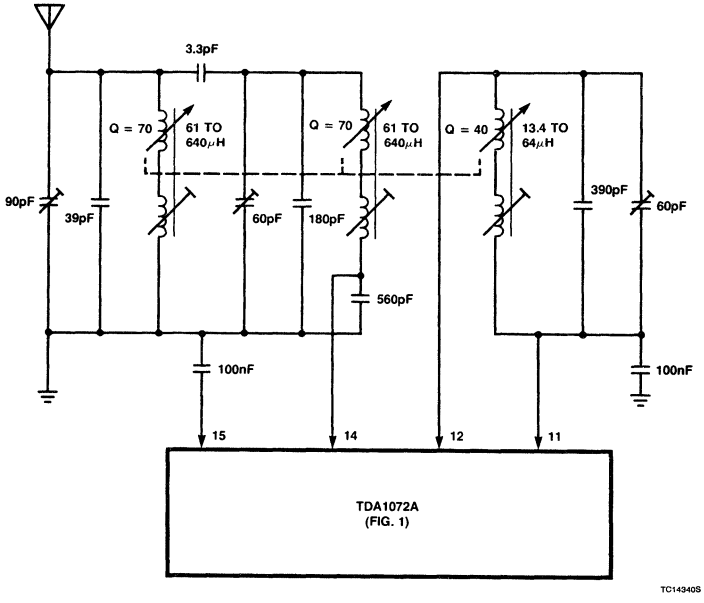


NOTE:
f_i = 1MHz, f_M = 0, m = 0, V_{CC} = 8.5V.

Figure 5. Field Strength Indication Voltage Characteristic for the Circuit of Figure 3



NOTE:
Permeability tuning coil. Hopf VM BC2.4.2A.

Figure 6. Aerial and Local Oscillator Circuits for a Permeability-Tuned Car Radio With Input Band-Pass Filter

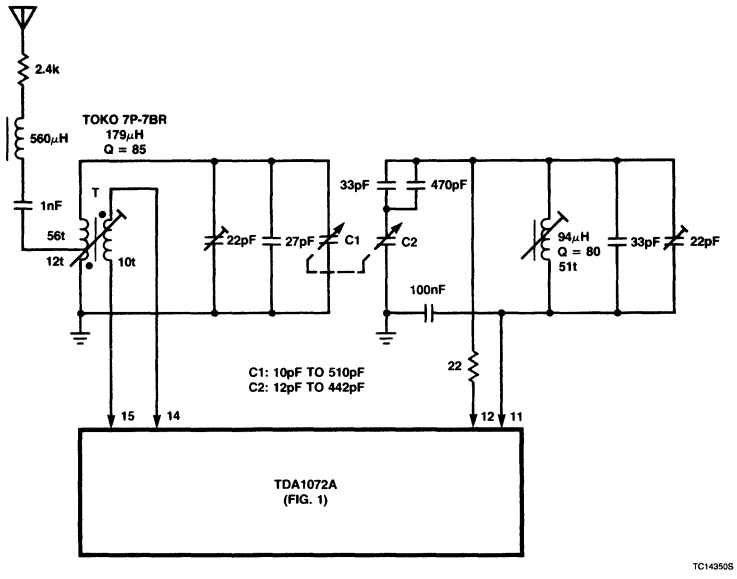
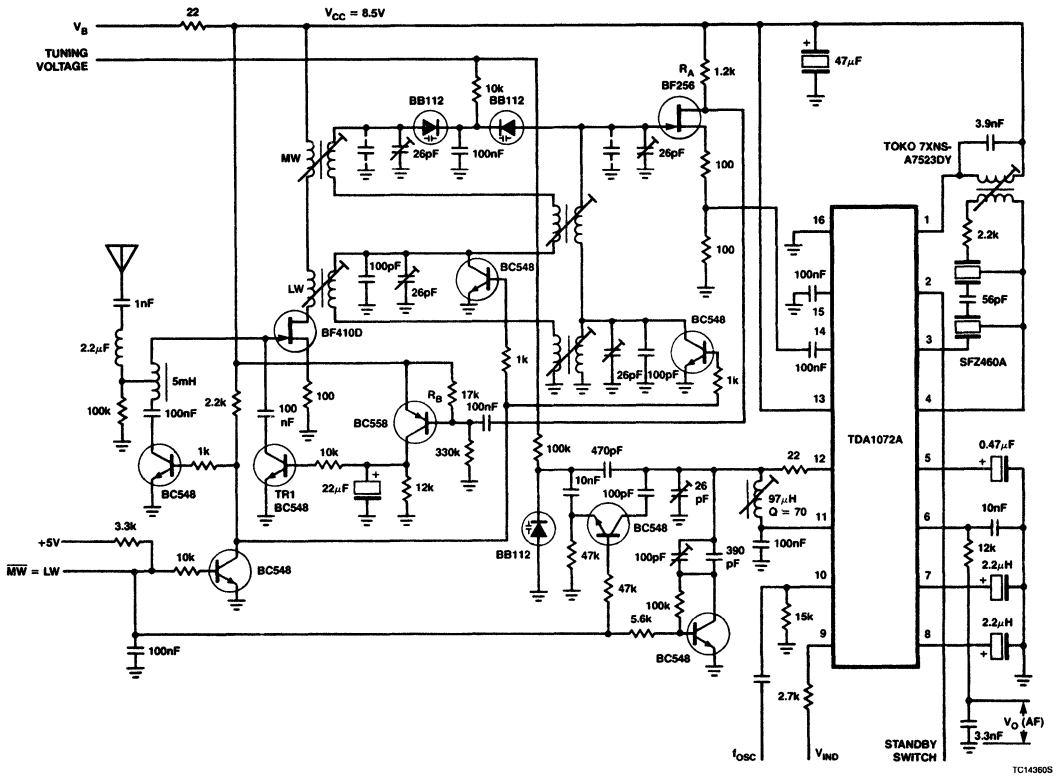


Figure 7. Aerial and Local Oscillator Circuits for a Variable-Capacitor Tuned Medium-Wave Domestic Radio

7

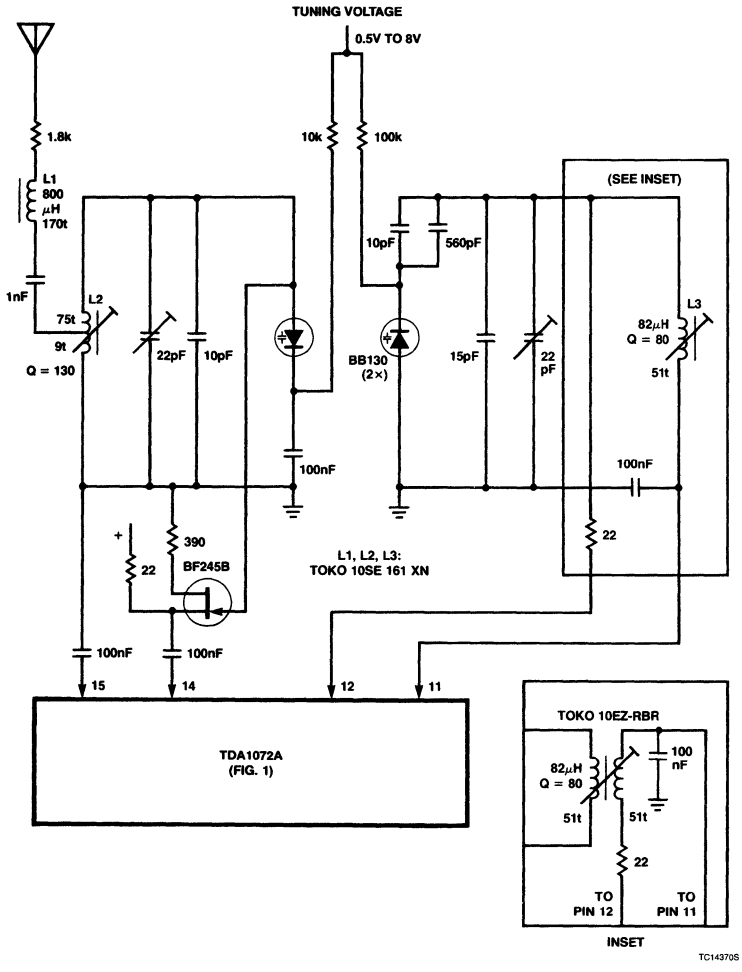
Integrated AM TDA1072A Receiver AN1961



NOTE:
The diode-tuned RF preamplifier provides large signal handling capability. For strong aerial signals, TR1 loads the antenna, keeping the gate voltage of the BF410D and the AC voltage across the varicap diodes low (130mV for RF input signals exceeding 5V). The slope of the AGC is set by R_a and the onset of gain control by R_b. Because the RF gain control is derived from the output of the tuned RF preamplifier, there is no masking of desired weak signals situated close to strong ones.

Figure 8. A Varicap Diode-Tuned Long-/Medium-Wave Car Radio With AGC for Large Signal Handling Capability

Integrated AM TDA1072A Receiver AN1961

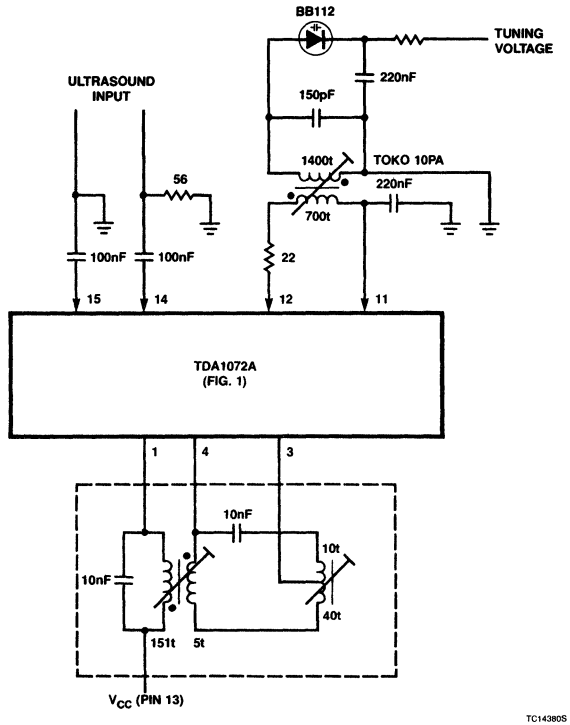


NOTE:
For high Q and aerial decoupling, a BF245B FET is used

Figure 9. Aerial and Local Oscillator Circuits for a Varicap Diode-Tuned Medium-Wave Domestic Radio

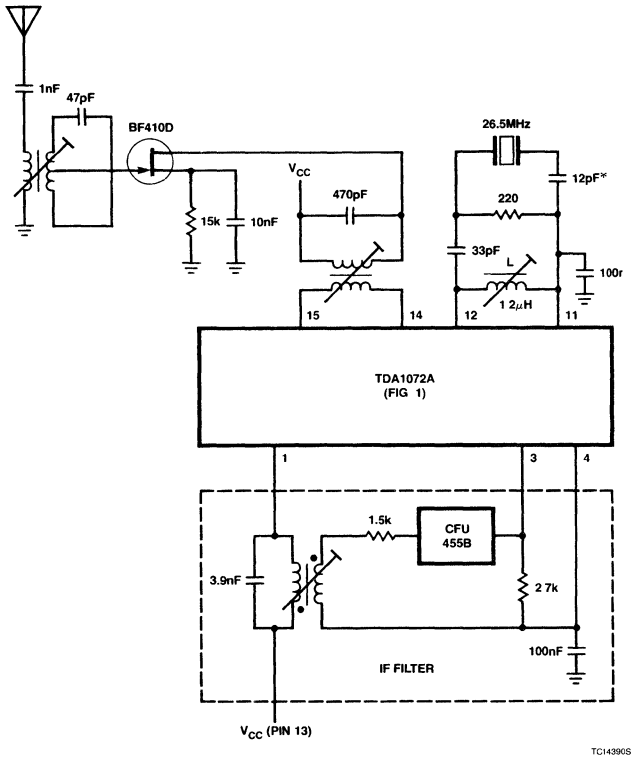
7

Integrated AM TDA1072A Receiver AN1961



NOTE:
The IF filter is tuned to 60kHz The IC oscillator is tuned by a varicap diode to between 25 and 35kHz.

Figure 10. Receiver for 25kHz to 35kHz Transmissions Such as Those Used in Doppler Rangefinders



NOTE:
A crystal Oscillator is used so that a narrow-band hybrid IF filter can be used

Figure 11. Aerial and Local Oscillator Circuits for a 27MHz Receiver for Remote for Remote Control of Garage Doors, Projectors, Curtains, etc.

7

REFERENCES

1. "Integrated AM Radio TDA1072," Philips Elcoma Technical Note 148, ordering code 9398 014 80011.
2. JANSEN, W. and KANOW, W., "AM Stereo — A New Dimension for Car Radios," *Electronic Components and Applications*, Vol. 3, No 4, Aug. 1981, also available as an offprint: Philips Elcoma Technical Publication 034, ordering code 9398 020 40011.
3. BAHNSEN, B.P. and GARSKAMP, A., "Integrated Circuits for Car Radios," *Electronic Components and Applications*, Vol. 3, No 2, Feb. 1981, also available as an offprint. Philips Elcoma Technical Publication 002, ordering code 9398 017 00011.
4. KANOW, W. and SIEWERT, I., "Integrated Circuits for Hi-Fi Radios and Tuners," *Electronic Components and Applications*, Vol. 4, No. 1, Nov. 1981, also available as an offprint: Philips Elcoma Technical Publication 040, ordering code 9398 021 10011.
5. "Single variable capacitance diode for AM Car Radios," *Electronic Components and Applications*, Vol. 4, No. 4, Aug. 1982, also available as an offprint: Philips Elcoma Technical Publication 076, ordering code 9398 038 20011.
6. BAHNSEN, B.P., "Voltage-controlled tuning of AM radios," *Electronic Components and Applications*, Vol. 2, No. 2, Feb. 1980.

Previously published as Technical Publication 152, Elcoma, February 5, 1985, The Netherlands

Signetics

TEA5570
AM/FM Radio Receiver Circuit

Product Specification

Linear Products

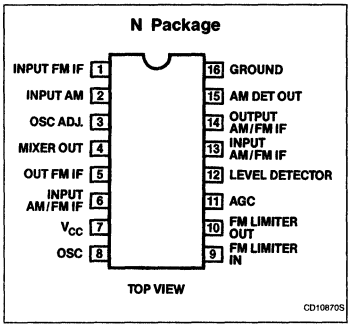
DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function, the IC incorporates for AM a double-balanced mixer, 'one-pin' oscillator, IF amplifier with AGC and detector, and a level detector for tuning indication. The FM circuitry comprises IF stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication completes the FM part.

FEATURES

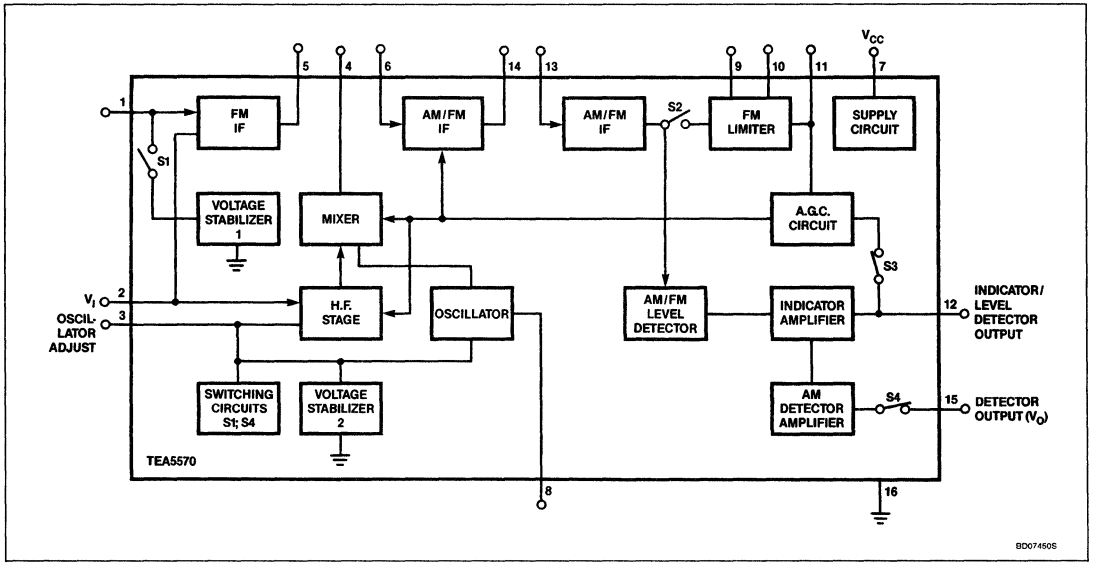
- **Simple DC switching for AM to FM by only one DC contact to ground (no switch contacts in the IF channel, AF or level detector outputs)**
- **AM and FM gain control**
- **Low current consumption (I_{TOT} = 6mA)**
- **Low voltage operation (V_{CC} = 2.7 to 9V)**
- **Ability to handle large AM signals; good IF suppression**
- **Applicable for inductive, capacitive and diode tuning**
- **Double smoothing of AGC line**
- **Short-wave range up to 30MHz**
- **Lumped or distributed IF selectivity with coil and/or ceramic filters**

PIN CONFIGURATION



- **AM and AGC output voltage control**
- **Distribution of PCB wiring provides good frequency stability**
- **Economic design for 'AM only' receivers**

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−30°C to +85°C	TEA5570N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC} = V_{7-16}$	Supply voltage (Pin 7)	12	V
V_{n-16}	Voltage at Pins 4, 5, 9, and 10 to Pin 16 (ground)	12	V
V_{8-16}	Voltage range at Pin 8	$V_{CC} \pm 0.5$	V
I_5	Current into Pin 5	3	mA
P_{TOT}	Total power dissipation	see Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +85	°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 6V$, $T_A = 25°C$, measured in Figure 9, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 7)					
$V_{CC} = V_{7-16}$	Supply voltage	2.4	5.4	9.0	V
Voltages					
V_{1-16}	at Pin 1 (FM)		1.42		V
V_{1-16}	at Pin 1; $-I_1 = 50\mu A$ (FM)		1.28		V
$V_{2,3-16}$	at Pins 2 and 3 (AM)		1.42		V
V_{6-16}	at Pin 6		0.7		V
V_{11-16}	at Pin 11		1.4		V
V_{13-16}	at Pin 13		0.7		V
V_{14-16}	at Pin 14		4.3		V
Currents					
I_7	Supply current	4.2	6.2	8.2	mA
$-I_1$	Current supplied from Pin 1 (FM)			50	μA
$-I_{12}$	Current supplied from Pin 12			20	μA
$-I_{15}$	Current supplied from Pin 15		30		μA
I_4	Current into Pin 4 (AM)		0.6		mA
I_5	Current into Pin 5 (FM)[4]		0.35		mA
I_8	Current into Pin 8 (AM)		0.3		mA
$I_{9,10}$	Current into Pins 9, 10 (FM)		0.65		mA
I_{14}	Current into Pin 14		0.4		mA
P	Power consumption		40		mW

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AC ELECTRICAL CHARACTERISTICS V_{CC} = 6V; T_A = 25°C; RF condition: f_I = 1MHz, m = 0.3, f_M = 1kHz; transfer impedance of the IF filter $|Z_{TR}| = v_6/I_4$ = 2.7k; measured in Figure 9, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	RF sensitivity (Pin 2)				
V_I	at V_O = 30mV	3.5	5.0	7.0	μV
V_I	at S + N/N = 6dB		1.3		μV
V_I	at S + N/N = 26dB		16	20	μV
V_I	at S + N/N = 50dB		1		mV
V_I	Signal handling (THD ⩽ 10% at m = 0.8)	200			mV
V_O	AF output voltage at V_I = 1mV	80	100	125	mV
	Total harmonic distortion				
THD	at V_I = 100μV to 100mV (m = 0.3)		0.5		%
	at V_I = 2mV (m = 0.8)		1.0	2.5	%
	at V_I = 200mV (m = 0.8)		4.0	10	%
α	IF suppression at V_O = 30mV[2]	26	35		dB
	Oscillator voltage (Pin 8)[3]				
V_{8-16}	at f_{OSC} = 1455kHz	120	160	200	mV
I_{12}	Indicator current (Pin 12) at V_I = 1mV		200	230	μA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 6V; T_A = 25°C; IF condition: f_I = 10.7MHz, Δf = ± 22.5kHz, f_M = 1kHz; transfer impedance of the IF filter $|Z_{TR}| = v_6/I_5$ = 275Ω; measured in Figure 9, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
IF part					
	IF sensitivity (adjustable)[4]				
	Input voltage				
V_I	at −3dB before limiting	90	110	130	μV
V_I	at S + N/N = 26dB		6		μV
V_I	at S + N/N = 65dB		1		mV
V_O	AF output voltage at V_I = 1mV	80	100	125	mV
THD	Total harmonic distortion at V_I = 1mV		0.3		%
AMS	AM suppression[5]		50		dB
Indicator/level detector (Pin 12)					
I_{12}	Indicator current		250	325	μA
	DC output voltage				
V_{12-16}	at V_I = 300μV		0.25		V
V_{12-16}	at V_I = 2mV		1.0		V
AM to FM switch					
$-I_3$	Switching current at V_{3-16} < 1V			400	μA

NOTES:

1. Oscillator operates at $V_{7-16} > 2.25V$
2. IF suppression is defined as the ratio $\alpha = 20 \log \frac{V_{I1}}{V_{I2}}$ where V_{I1} is the input voltage at f = 455kHz and V_{I2} is the input voltage at f = 1MHz.
3. Oscillator voltage at Pin 8 can be preset by R_{OSC} (see Figure 9)
4. Maximum current into Pin 5 can be adjusted by R1 (see Figure 9).

$$I_5 = \frac{V_{3-16}}{R1} - I_3 \text{ when } V_{3-16} = 800mV,\ I_3 = 400\mu A$$

5 AM suppression is measured with f_M = 1kHz, m = 0 3 for AM; f_M = 400Hz, Δf = ± 22.5kHz for FM.

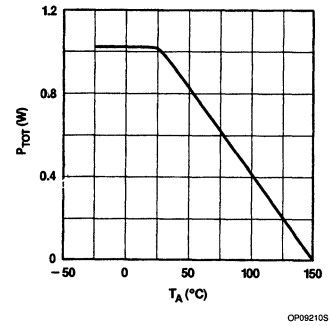
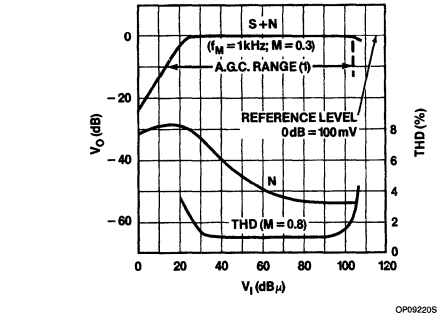


Figure 1. Power Derating Curve

FACILITY ADAPTATION

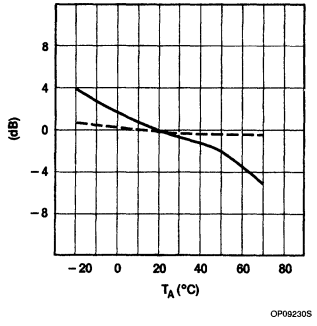
Facility adaptation is achieved as follows (see Figure 9):

Facility	Component
FM sensitivity	R1 fixes the current at Pin 5 ($I_5 = \frac{V_{3-16}}{R_1} - 400\mu A$) (gain adjustable ± 10dB)[4]
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{OSC}
AM output voltage	R7, R11
AM AGC setting	R7



NOTES:
1 AGC range (figure of merit, FOM)
2 Measured at f_i = 1MHz in Test Circuit Figure 9

Figure 2. Signal, Noise, and Distortion as a Function of Input Voltage (V_I)



NOTES:
——— Sensitivity (V_I) at V_O = 30mV, m = 0.3
– – – – Output voltage (V_O) at V_I = 2mV, m = 0.3
Measured at f_i = 1MHz in Test Circuit Figure 9

Figure 3. Sensitivity (V_I), Output Voltage (V_O), as a Function of Temperature Behavior T_A

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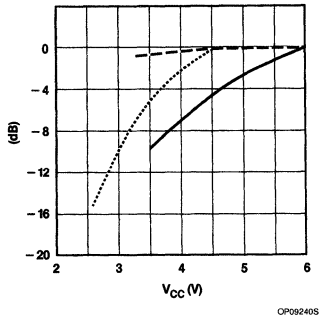
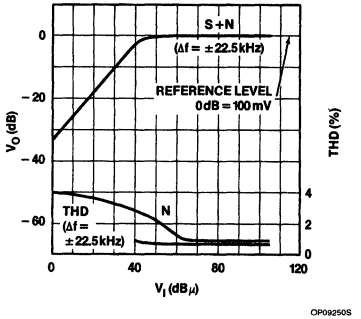


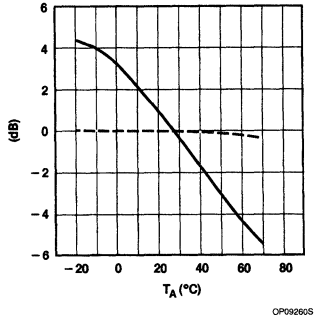
NOTES:
——— Sensitivity (V_I) at V_O = 30V, m = 0 3 6V application
····· Sensitivity (V_I) at V_O = 30mV, m = 0 3 4 5V application
– – – – Output voltage (V_O) at V_I = 0 2mV, m = 0 3
Measured at f_I = 1MHz in Test Circuit Figure 9, for application V_{CC} = 6V
Also shown is the sensitivity for V_{CC} = 4 5V application (Figure 15)

Figure 4. Sensitivity (V_I) and Output Voltage (V_O) as a Function of Supply Voltage (V_{CC})



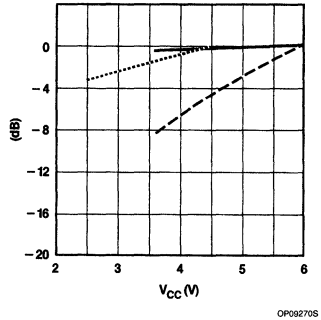
NOTE:
Measured at f_I = 10 7MHz in Test Circuit Figure 9

Figure 5. Signal, Noise, and Distortion as a Function of Input Voltage (V_I)



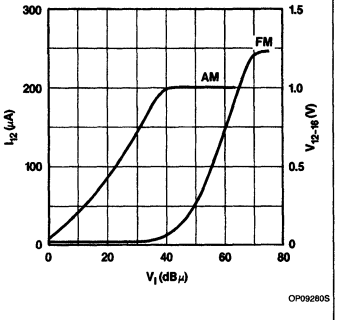
NOTES:
——— Sensitivity at −3dB limiting
– – – – Output voltage (V_O) at V_I = 1mV, Δf = ± 22kHz
Measured at f_I = 10 7MHz in Test Circuit Figure 9

Figure 6. Sensitivity (V_I) Output Voltage (V_O) as a Function of Temperature Behavior (T_A)



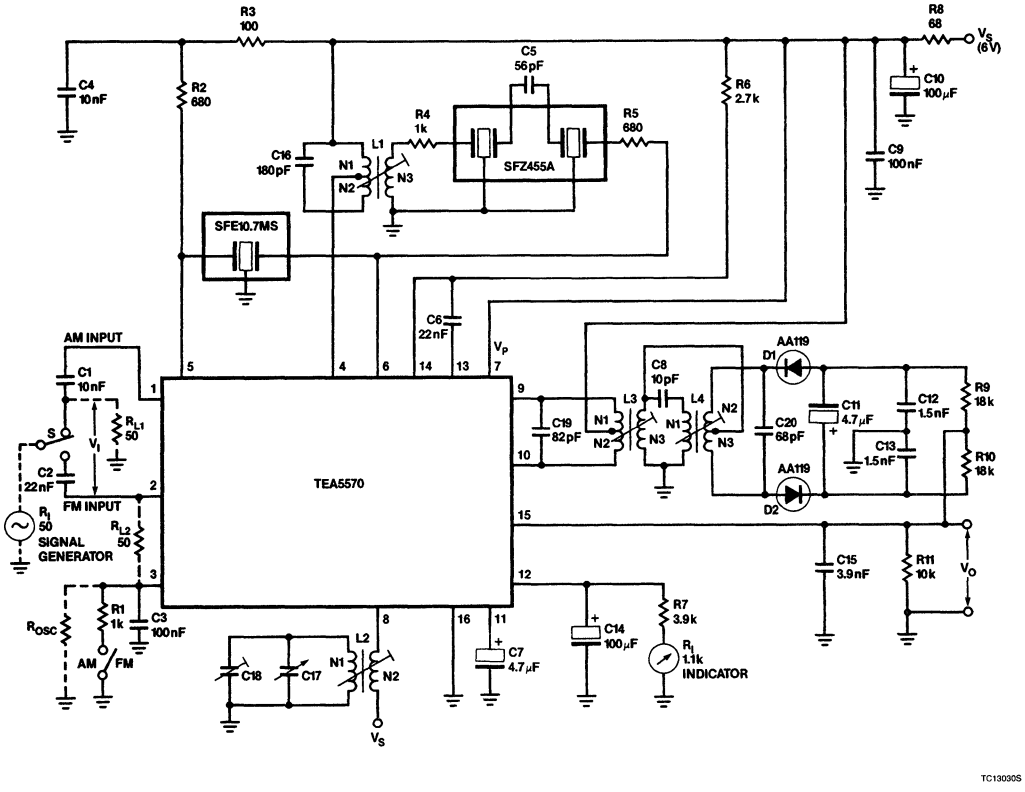
NOTES:
——— Sensitivity at −3dB limiting V_{CC} = 6V application
····· Sensitivity at −3dB limiting V_{CC} = 4 5V application
– – – – Output voltage (V_O) at V_I = 1mV, Δf = ± 22 5kHz
(V_O) as a function of supply voltage (V_{CC})
Measured at f_I = 10 7MHz in Test Circuit Figure 9

Figure 7. Sensitivity (V_I) and Output Voltage



NOTES:
AM f_I = 1MHz, (V_I) Measured in Figure 9, V_{CC} = 6V, R_{12-16} = 5k

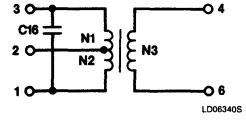
Figure 8. Indicator Output Current (I_{12}) and DC Output Voltage (V_{12-16})



NOTES:
Coil Data
The transfer impedance of the IF filter is
AM $|Z_{TR}| = v_6/I_4 = 2.7k\Omega$ (SFZ 455A)
FM $|Z_{TR}| = v_6/I_5 = 275\Omega$ (SFE 10.7 MS)
See also Figures 10, 11, 12, and 13

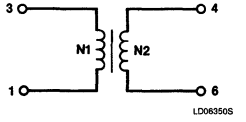
Figure 9. Test Circuit

AM IF Coils (Figure 9)



NOTES:
N1 = 73
N2 = 73
N3 = 9
C16 = 180pF (internal)
Wire = 0.07mm dia
TOKO sample no 7 MC-7P

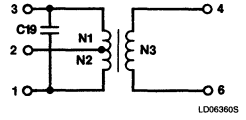
Figure 10. IF Bandpass Filter (L1)



NOTES:
N1 = 90
N2 = 7
Wire = 0.07mm dia
TOKO sample no 7 BR-7P

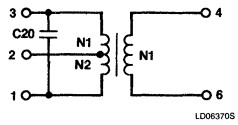
Figure 11. Oscillator Coil (L2)

FM IF Coils (Figure 9)



NOTES:
N1 = 5
N2 = 5
N3 = 4
C19 = 82pF (internal)
Wire = 0.1mm dia
TOKO sample no 119 AN-7P

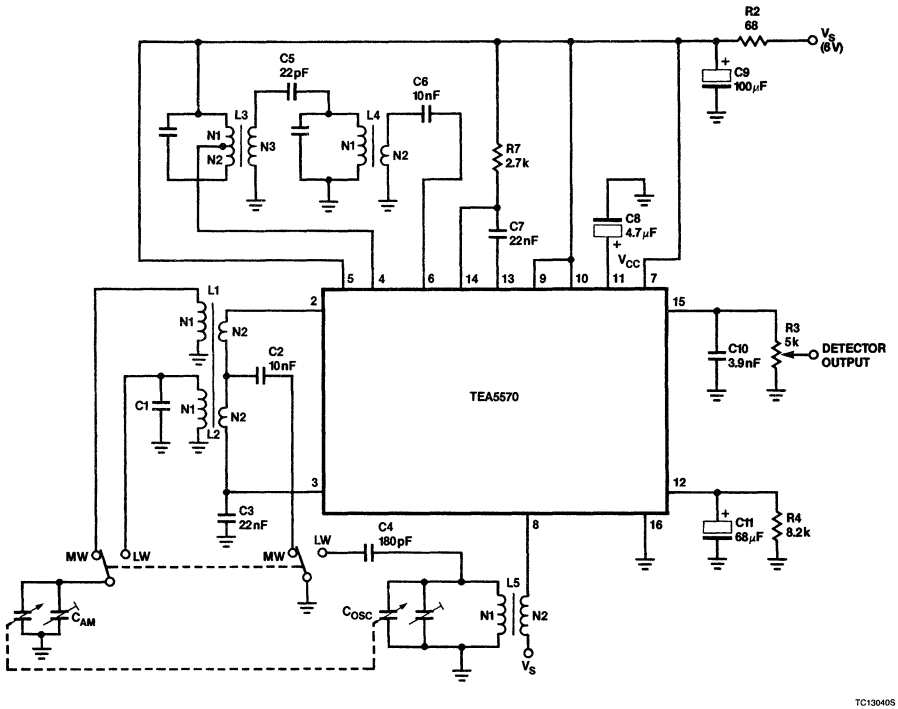
Figure 12. Primary Ratio Detector Coil (L3)



NOTES:
N1 = 2
N2 = 6
N3 = 6
C20 = 68pF (internal)
Wire = 0 1mm dia
TOKO sample no 119 AN-7P

Figure 13. Secondary Ratio Detector Coil (L4)

APPLICATION INFORMATION Figures 14 and 16 show the circuit diagrams for the application of 6V AM MW/LW, and 4.5V AM/FM channels, respectively, using the TEA5570. Figure 15 shows the circuitry for the TEA5570.



Coil Data

L3	N1	= 73
	N2	= 73
	N3	= 9
	C	= 180pF
L4	N1	= 146
	N2	= 9
	C	= 180pF
L5	N1	= 90
	N2	= 6

Figure 14. Typical Application Circuit for 6V AM MW/LW Reception Using the TEA5570

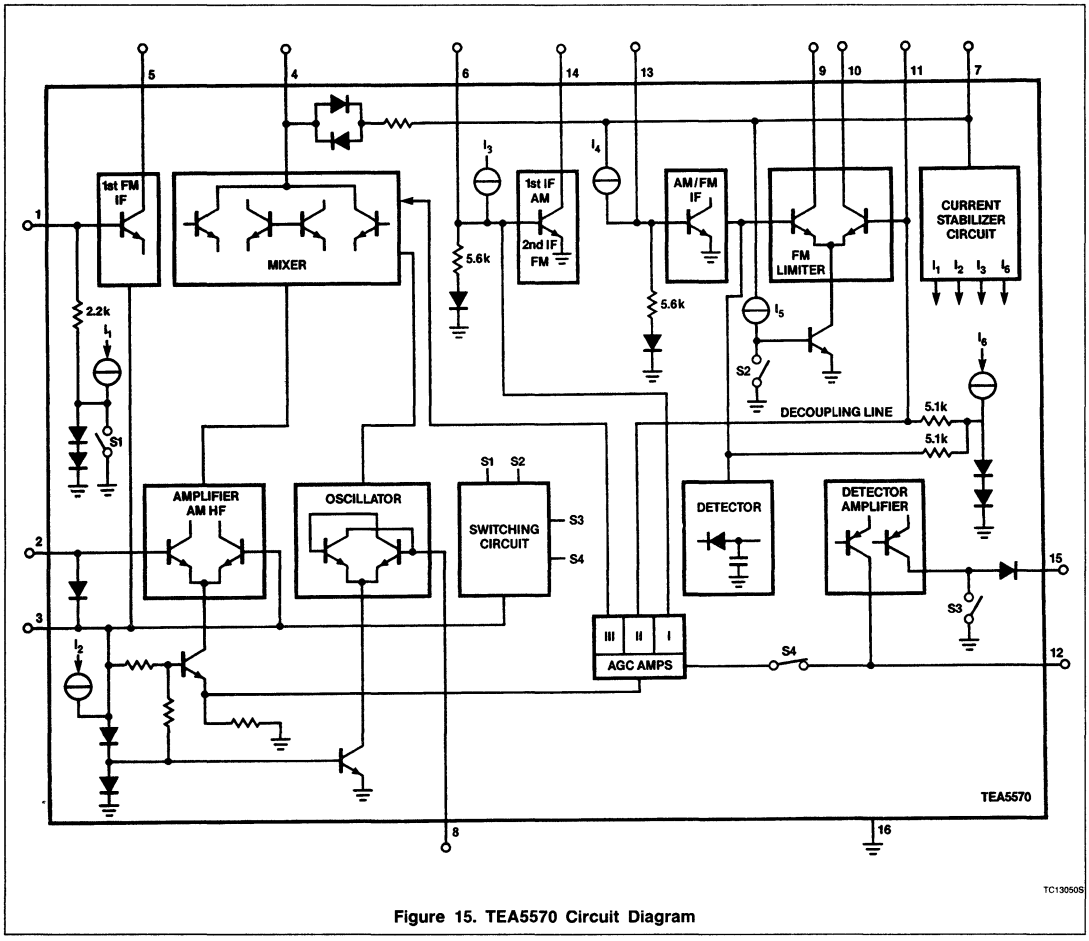


Figure 15. TEA5570 Circuit Diagram

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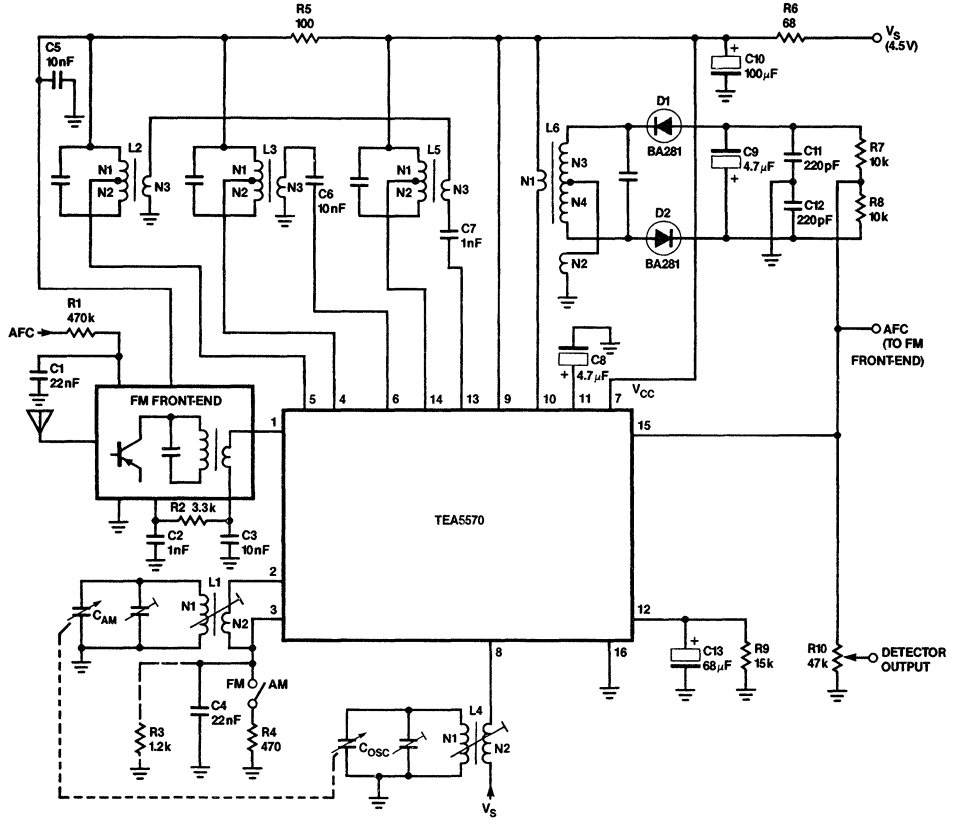


Coil Data

L2	N1	= 3
	N2	= 8
	N3	= 1
	C	= 82pF
L3	N1	= 33
	N2	= 113
	N3	= 9
	C	= 180pF
L4	N1	= 90
	N2	= 6
L5	N1	= 33
	N2	= 113
	N3	= 9
L6	N1	= 50
	N2	= 50
	N3	= 4 5
	N4	= 6 5
	C	= 82pF

Figure 16. Typical Application Circuit for 4.5V AM/FM Reception Using the TEA5570 With Coils and Single-tuned Ratio Detector (With Silicon Diodes)

TDA1001B
Interference Suppressor

Product Specification

Linear Products

DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

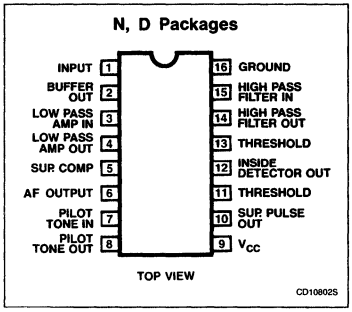
FEATURES

- **Active low-pass and high-pass filters**
- **Interference pulse detector with adjustable and controllable response sensitivity**
- **Noise detector designed for FM IF amplifiers with ratio detectors or quadrature detectors**
- **Schmitt trigger for generating an interference suppression pulse**
- **Active pilot tone generation (19kHz)**
- **Internal voltage stabilization**

APPLICATIONS

- **FM mono and stereo receivers**
- **Noise suppression**

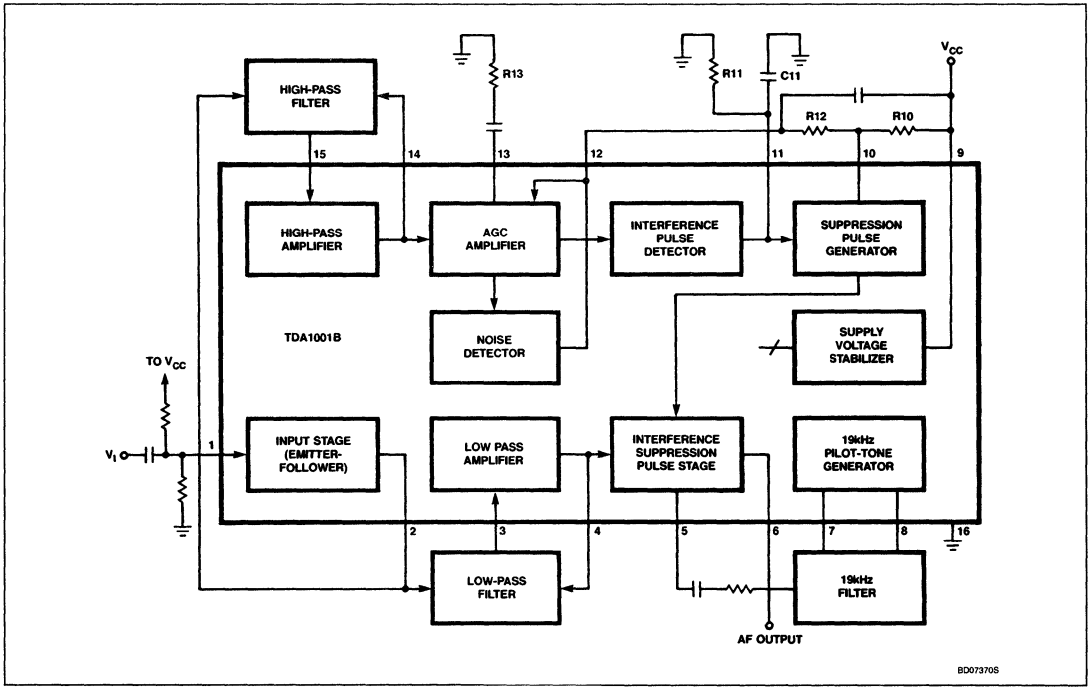
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to 70°C	TDA1001BN
16-Pin Plastic SO (SO-16; SOT-109A)	0 to 70°C	TDA1001BTD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 9)	18	V
V_{IN}	Input voltage (Pin 1)	V_{CC}	V
I_{OUT} $-I_{OUT}$	Output current (Pin 6)	1 15	mA mA
P_D	Total power dissipation	see derating curves Figure 3	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; T_A = 25°C, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Input stage					
$\|Z_{I1}\|$	Input impedance (Pin 1) f = 40kHz		45		kΩ
R_{I1}	Input resistance (Pin 1) with pin 2 not connected		600		kΩ
I_{I1}	Input bias current (Pin 1) V_{1-16} = 4.8V		6	15	μA
R_{O2}	Output resistance (Pin 2) unloaded		low-ohmic		
R_{2-16}	Internal emitter resistance		5.6		kΩ
Low-pass amplifier					
R_{I3}	Input resistance (Pin 3)	10			MΩ
I_{I3}	Input bias current (Pin 3)			7	μA
R_{O4}	Output resistance (Pin 4)			5	Ω
A_V	Voltage gain (V_4/V_3)		1.1		V
Suppression pulse stage					
I_{OS5}	Input offset current at Pin 5 during the suppression time t_S		50	200	nA
Output stage					
R_{O6}	Output resistance (Pin 6)		low-ohmic		
R_{6-16}	Internal emitter resistance		6		kΩ
$G_{I5/6}$	Current gain (I_5/I_6)		85		dB
Pilot tone generation (19kHz)					
$\|Z_{I8}\|$	Input impedance (Pin 8)			1	Ω
$\|Z_{O7}\|$	Output impedance (Pin 7) Pin 8 open	150			kΩ
I_{O7}	Output bias current (Pin 7)	0.7	1	1.3	mA
$G_{I7/8}$	Current gain (I_7/I_8)		3		mA
High-pass amplifier					
R_{I15}	Input resistance (Pin 15)	10			MΩ
I_{BIAS15}	Input bias current (Pin 15)			7	μA
R_{O14}	Output resistance (Pin 14)			5	Ω
$A_{V14/15}$	Voltage gain ($V_{14/15}$)		14		V

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
AGC amplifier; interference and noise detectors					
R_{13-14}	Internal resistance (Pins 13 and 14)	1.5	2.0	2.5	kΩ
$\pm V_{14int\ m}$ $\pm V_{14n\ m}$	Operational threshold voltage (uncontrolled); peak value (Pin 14) of the interference pulse detector of the noise detector		 15 6.5		 mV mV
V_{11-16M}	Output voltage (peak value; Pin 11)	5.2	5.8	6.4	V
I_{12M}	Output control current (Pin 12) (peak value)	150	200	250	μA
I_{O12}	Output bias current (Pin 12)		2.5	6	μA
V_{12-9} or:	Input threshold voltage for onset of control (Pin 12) ($V_{I(tr)O}$ + 3dB)	360	425 $0.66V_{BE}$	500	mV mV
Suppression pulse generation (Schmitt trigger)					
 V_{11-16} V_{11-16}	Switching threshold (Pin 11) 1: gate disabled 2: gate enabled		 3.2 2.0		 V V
ΔV_{11-16}	Switching hysteresis		1.2		V
I_{OS11}	Input offset current (Pin 11)			100	nA
I_{O10M}	Output current (Pin 10) gate disabled; peak value	0.6	1	1.4	mA
I_{R10}	Reverse output current (Pin 10)			2	μA
V_{10-16}	Sensitivity (Pin 10)	2.5			V

APPLICATION INFORMATION V_{CC} = 12V; T_A = 25°C; f = 1kHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range (Pin 9)	7.5	12	16	V
I_{CC}	Quiescent supply current (Pin 9)	10	14	18	mA
Signal path					
V_{1-16}	DC input voltage (Pin 1)		4.5		V
$\lvert Z_{I1} \rvert$	Input impedance (Pin 1); f = 40kHz	35			kΩ
V_{6-16}	DC output voltage (Pin 6)	2.4	2.8		V
R_{O6}	Output resistance (Pin 6)		low-ohmic		
$A_V6/1$	Voltage gain (V_6/V_1)	0	0.5	1	dB
$f_{(-3dB)}$	−3dB point of low-pass filter		70		kHz
$V_{I(P-P)}$	Sensitivity for THD < 0.5% (peak-to-peak value)	1.2	1.8		V
$V_{6-16(P-P)}$	Residual interference pulse after suppression (see Figure 4); Pin 7 to ground; $V_{I(TR)M}$ = 100mV; (peak-to-peak value)			3	mV
α_{int}	Interference suppression at R13 = 0;[5, 6] $V_{I(RMS)}$ = 30mV; f = 19kHz (sine wave); $V_{I(TR)M}$ = 60mV; f_r = 400Hz	20	30		dB

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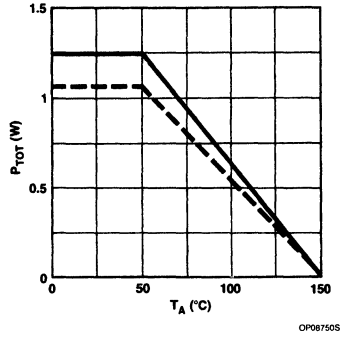
APPLICATION INFORMATION (Continued) V_{CC} = 12V; T_A = 25°C; f = 1kHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Interference processing					
	Input signal at Pin 1; output signal at Pin 10				
	Suppression pulse threshold voltage; control function OFF (Pin 9 connected to Pin 12); RMS value[1] measured with sinewave input signal f = 120kHz; $-V_{10-9} > 1V$				
$V_{I(TR)RMS}$	at R13 = 0Ω	8	11	14	mV
$V_{I(TR)RMS}$	at R13 = 2.7kΩ	18	28.5	40	mV
$\Delta V_{I(RMS)}$	voltage difference for safe triggering/non-triggering (RMS value) measured with interference pulses f = 400Hz (see Figure 4); peak value		1		mV
$V_{I(TR)M}$	at R13 = 0Ω		19		mV
$V_{I(TR)M}$	at R13 = 2.7kΩ		45		mV
t_S	Suppression pulse duration[2]	24	27	30	µs
Noise threshold feedback control[1, 3]					
	Noise input voltage (RMS value) f = 120kHz sinewave for V_{12-9} = 300mV				
$V_{NI(RMS)}$	at R13 = 0Ω	2.3	3.3	4.3	mV
$V_{NI(RMS)}$	at R13 = 2.7kΩ		8.2		mV
	for V_{12-9} = 425mV ($V_{I(TR)O}$ + 3dB)				
$V_{NI(RMS)}$	at R13 = 0Ω		7.3		mV
$V_{NI(RMS)}$	at R13 = 2.7kΩ		16.5		mV
	for V_{12-9} = 560mV ($V_{I(TR)O}$ + 20dB)				
$V_{NI(RMS)}$	at R13 = 0Ω	33	45	57	mV
$V_{NI(RMS)}$	at R13 = 2.7kΩ		107		mV
	Amplification control voltage by interference intensity[4] $V_{I(RMS)}$ = 50mV; f = 19kHz; $V_{I(TR)M}$ = 300mV; RMS value				
$V_{O6(RMS)}$	at repetition frequency f_R = 1kHz	49		56	mV
$V_{O6(RMS)}$	at repetition frequency f_R = 16kHz	45		65	mV

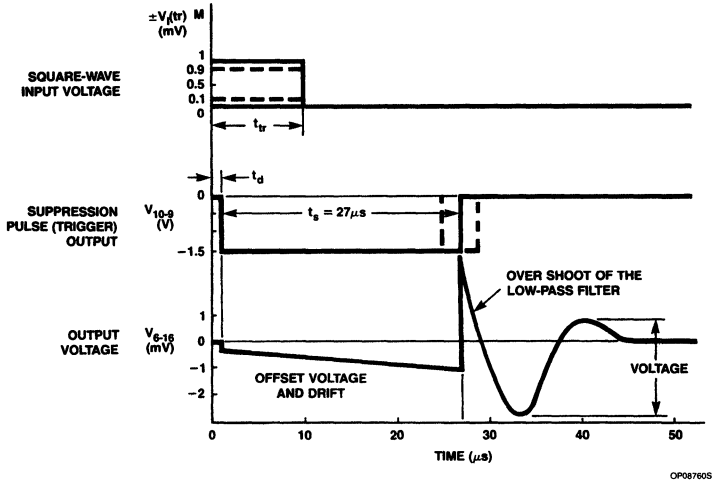
NOTES:

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{I(TR)} = (1 + R13/R_S \times V_{I(TR)O}$ in which R_S = 2kΩ;
   $V_{NI} = (1 + R13/R_S \times V_{NIO}$ in which R_S = 2kΩ.
2. The suppression pulse duration is determined by C11 = 2.2nF and R11 = 6.8kΩ.
3. The characteristics of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interfence suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19kHz generator can be adjusted with R_{7-16} (and R_{7-8}). Adjustable is not required if components with small tolerances are used, e.g., $\Delta R < 1\%$ and $\Delta < 2\%$.
6. Measuring conditions.
   The peak output noise voltage (V_{NO}, CCITT filter) shall be measured at the output with a deemphasizing time t = 50µs (R = 5kΩ, C = 10nF); the reference value of 0dB is $V_{O\ INT}$ with the 19kHz generator short-circuited (Pin 7 grounded).



NOTES:
——— In plastic DIP package (TDA1001B)
– – – In plastic SO package (TDA1001BT), mounted on a ceramic substrate of 50 × 15 × 0.7mm

Figure 1. Power Derating Curves



NOTE:
At the input (Pin 1) a square wave is applied with a duration of $t_{TR} = 10\mu s$ and with rise and fall times $t_R = t_F = 10ns$

Figure 2. Measuring Signal for Interference Suppression

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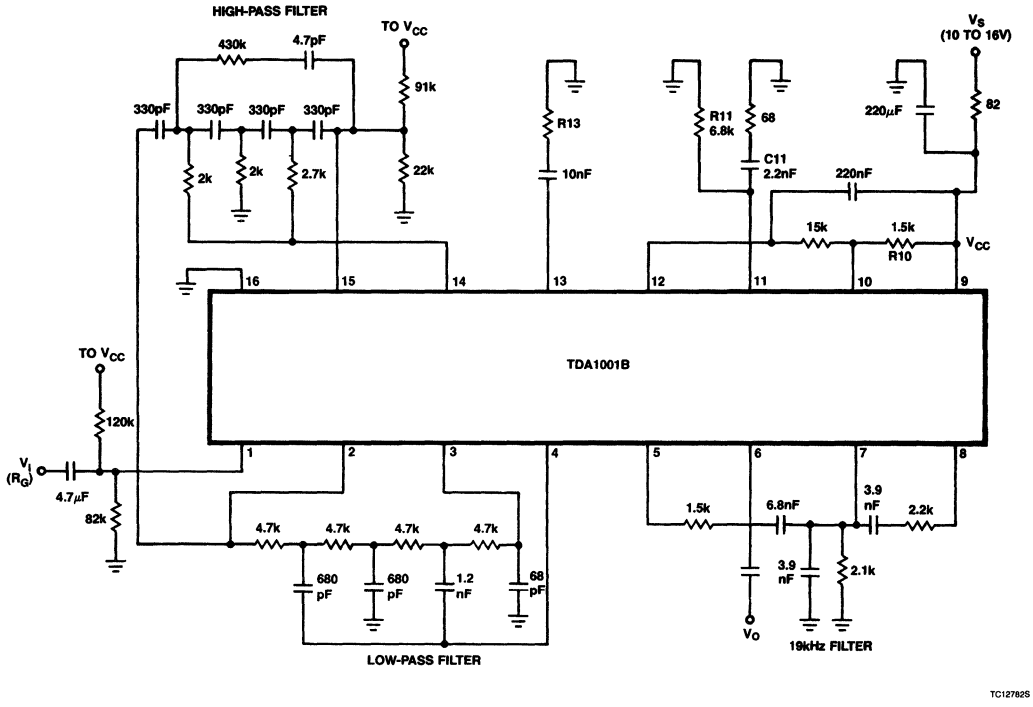


Figure 3. Application Circuit Diagram

Signetics

TDA7000
Single-Chip FM Radio Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked Loop) system with an intermediate frequency of 70kHz. The IF selectivity is obtained by active RC filters. The only function which needs tuning is the resonant circuit for the oscillator which selects the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates weak, noisy input signals. Special precautions are taken to meet the radiation requirements.

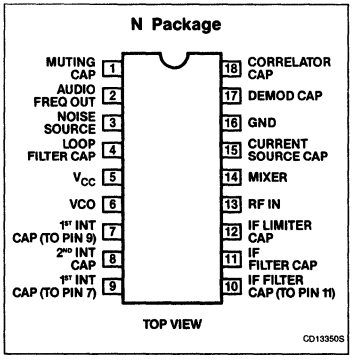
FEATURES

- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

APPLICATIONS

- **Mono FM Portable Radios**
- **LAN**
- **Data Receivers**
- **SCA Receiver**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	0 to +70°C	TDA7000N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 5)	12	V
V_{6-5}	Oscillator voltage (Pin 6)	V_{CC} − 0.5 to V_{CC} + 0.5	V
P_{TOT}	Total power dissipation	See derating curve Figure 1	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

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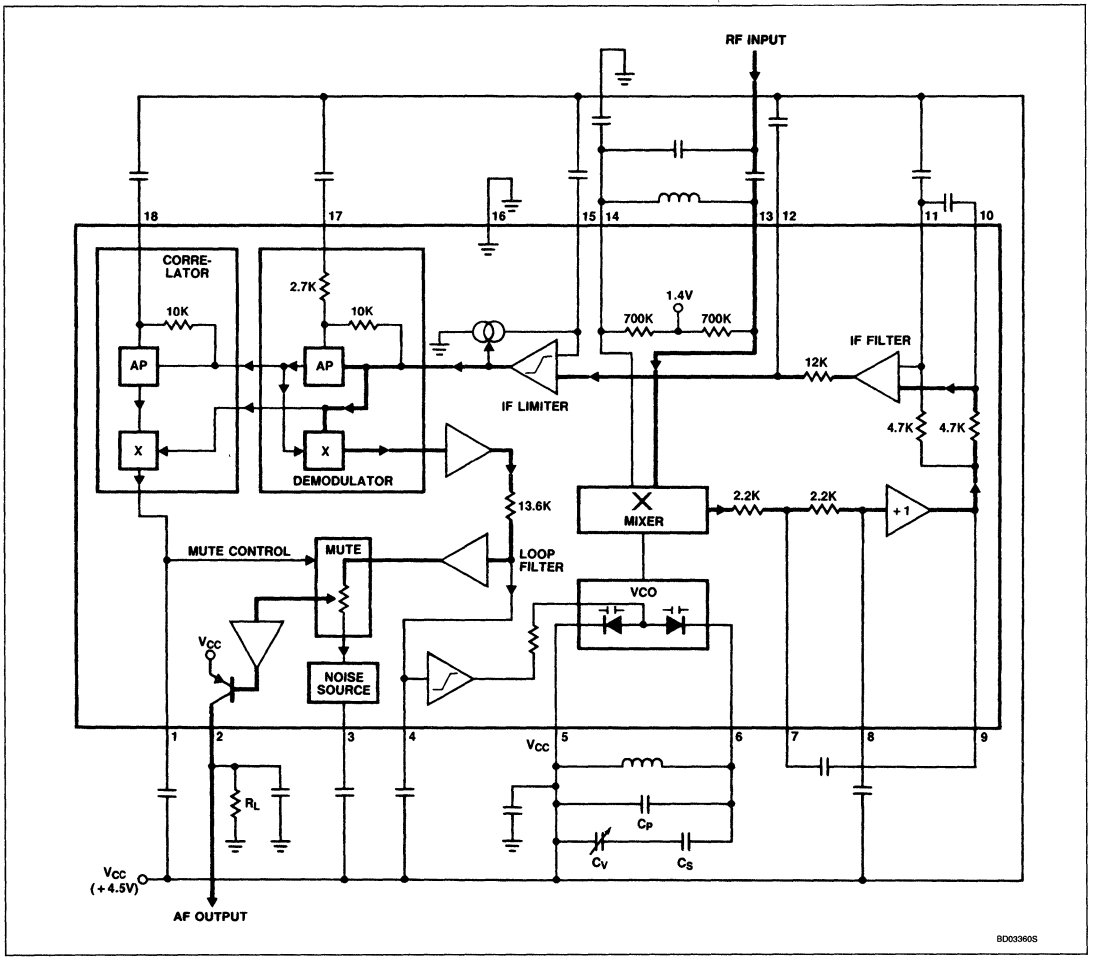
Single-Chip FM Radio Circuit TDA7000

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C; measured in Figure 3, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 5)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_6	Oscillator current	(Pin 6)		280		μA
V_{14-16}	Voltage	(Pin 14)		1.35		V
I_2	Output current	(Pin 2)		60		μA
V_{2-16}	Output voltage	(Pin 2) R_L = 22kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C; measured in Figure 3 (mute switch open, enabled); f_{RF} = 96MHz (tuned to max. signal at 5μV EMF) modulated with Δf = ± 22.5kHz; f_M = 1kHz; EMF = 0 2mV (EMF voltage at a source impedance of 75Ω); RMS noise voltage measured unweighted (f = 300Hz to 20kHz), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (EMF voltage)	-3dB limiting, muting disabled		1 5		μV
		-3dB muting		6		
		S/N = 26dB		5.5		
EMF	Signal handling (EMF voltage)	THD < 10%; Δf = ± 75kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ± 22.5kHz		0.7		%
		Δf = ± 75kHz		2.3		
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_M = 1kHz; Δf = ± 75kHz AM signal: f_M = 1kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100mV; f = 1kHz)		10		dB
$V_{6-5(RMS)}$	Oscillator voltage (RMS value)	(Pin 6)		250		mV
Δf_{OSC}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		60		kHz/V
S_{+300}	Selectivity			45		dB
S_{-300}				35		
Δf_{RF}	AFC range			± 300		kHz
BW	Audio bandwidth	ΔV_O = 3dB measured with pre-emphasis (t = 50μs)		10		kHz
$V_{O\ RMS}$	AF output voltage (RMS value)	R_L = 22kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

NOTES:

1. The muting system can be disabled by feeding a current of about 20μA into Pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at Pin 3. Silent tuning can be achieved by omitting this capacitor

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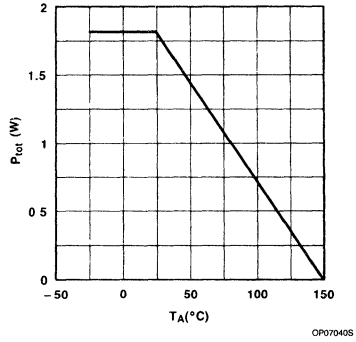
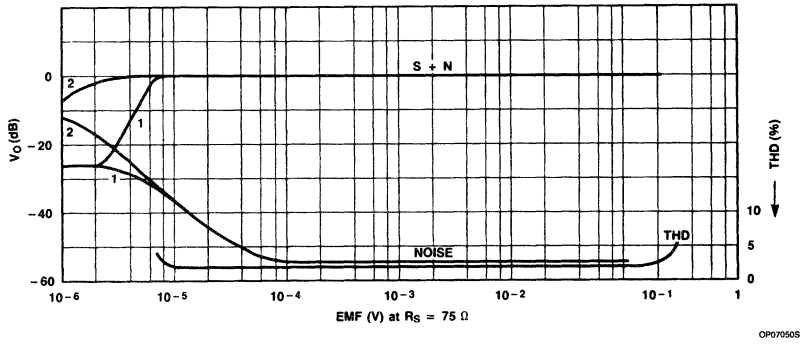


Figure 1. Power Derating Curve



NOTES:
1 The muting system can be disabled by feeding a current of about 20μA into Pin 1
2 The interstation noise level can be decreased by choosing a low-value capacitor at Pin 3 Silent tuning can be achieved by omitting this capacitor

Conditions 0dB = 75mV, f_{RF} = 96MHz
for S + N curve $\Delta f = \pm 22.5$kHz f_M = 1kHz
for THD curve $\Delta f = \pm 75$kHz f_M = 1kHz

Figure 2. AF Output Voltage (V_O) and Total Harmonic Distortion (THD) as a Function of the EMF Input Voltage (EMF) With a Source Impedance (R_S) of 75Ω: (1) Muting System Enabled; (2) Muting System Disabled

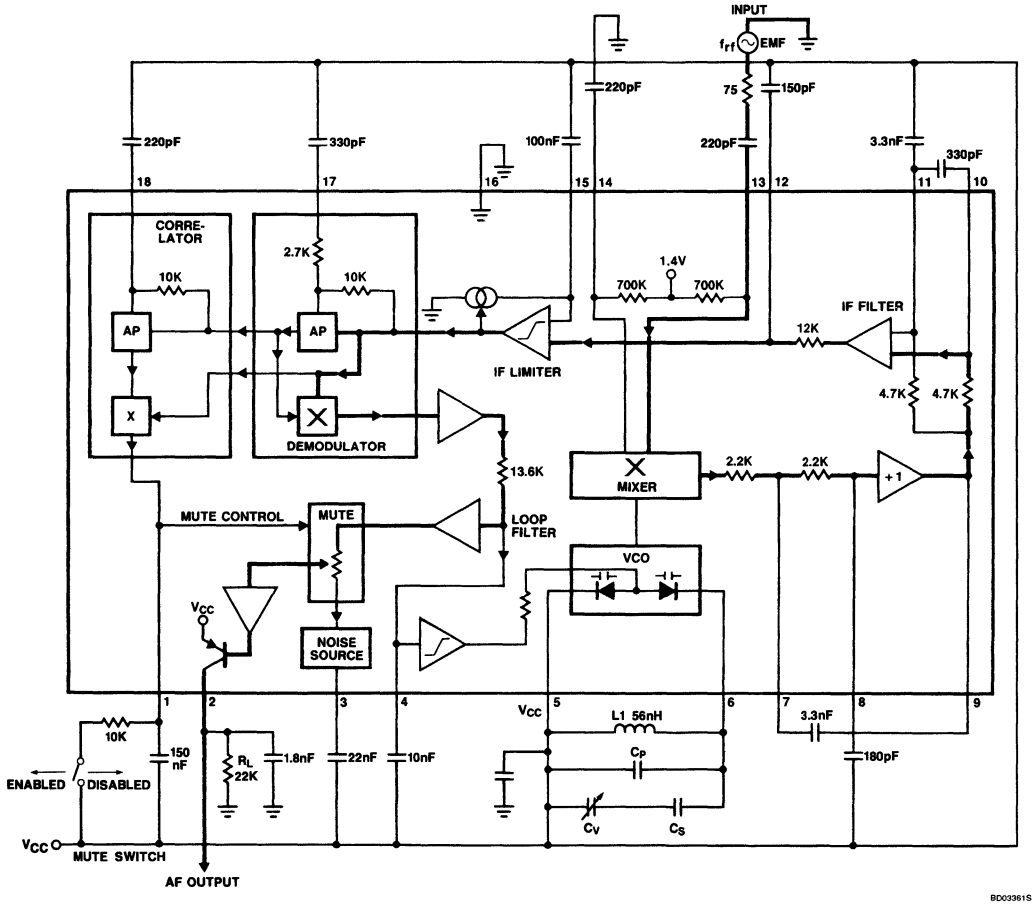


Figure 3. Test Circuit

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Signetics

AN192
A Complete FM Radio on a Chip

Application Note

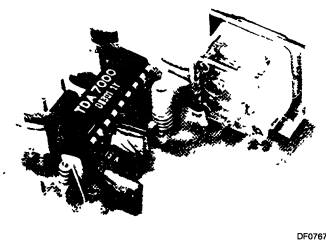
Linear Products

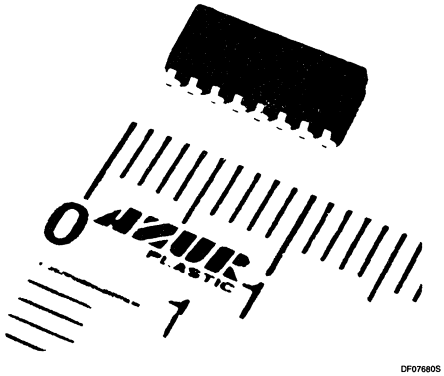
Authors: W.H.A. Van Dooremolen and
M. Hufschmidt

Until now, the almost total integration of an FM radio has been prevented by the need for LC tuned circuits in the RF, IF, local oscillator and demodulator stages. An obvious way to eliminate the coils in the IF and demodulator stages is to reduce the normally used intermediate frequency of 10.7MHz to a frequency that can be tuned by active RC filters, the op amps and resistors of which can be integrated. An IF of zero deems to be ideal because it eliminates spurious signals such as repeat spots and image response, but it would not allow the IF signal to be limited prior to demodulation, resulting in poor signal-to-noise ratio and no AM suppression. With an IF of 70kHz, these problems are overcome and the image frequency occurs about halfway between the desired signal and the center of the adjacent channel. However, the IF image signal must be suppressed and, in common with conventional FM radios, there is also a need to suppress interstation noise and noise when tuned to a weak signal. Spurious responses above and below the center frequency of the desired station (side tunings), and harmonic distortion in the event of very inaccurate tuning must also be eliminated.

We have now developed a mono FM reception system which is suitable for almost total integration. It uses an active 70kHz IF filter and a unique correlation muting circuit for suppressing spurious signals such as side responses caused by the flanks of the demodulator S-curve. With such a low IF, distortion would occur with the ±75kHz IF swing due to received signals with maximum modulation. The maximum IF swing is therefore compressed to ±15kHz by controlling the local oscillator in a frequency-locked loop (FLL). The combined action of the muting circuit and the FLL also suppresses image response.

The new circuit is the TDA7000 which integrates a mono FM radio all the way from the aerial input to the audio output. External to the IC are only one tunable LC circuit for the local oscillator, a few inexpensive ceramic plate capacitors and one resistor. The TDA7000 dramatically reduces assembly and post-production alignment costs because only the oscillator circuit needs adjustment during manufacture to set the limits of the tuned frequency band. The complete FM radio can be made small enough to fit inside a calculator, cigarette lighter, key-ring fob or even a slim watch. The TDA7000 can also be used as receiver in equipment such as cordless telephones, CB radios, radio-controlled models, paging systems, the sound channel of a TV set or other FM demodulating systems.





A Laboratory Model of the TDA7000 in a Complete FM Radio. Also Shown is the TDA7010T in the SO Package Against a CM Scale

A Complete FM Radio on a Chip AN192

Using the TDA7000 results in significant improvements for all classes of FM radio. For simpler portables, the small size, lack of IF coils, easy assembly and low power consumption are not the only attractive features. The unique correlation muting system and the FLL make it very easy to tune, even when using a tiny tuning knob. For higher-performance portables and clock radios, variable-capacitance diode tuning and station presetting facilities are often required. These are easily provided with the TDA7000 because there are no variable tuned circuits in the RF signal path. Only the local oscillator needs to be tuned, so tracking and distortion problems are eliminated.

The TDA7000 is available in either an 18-lead plastic DIP package (TDA7000), or in a 16-pin SO package (TDA7010T). Future developments will include reducing the present supply voltage (4.5V typ.), and the introduction of FM stereo and AM/FM versions.

BRIEF DATA

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{CC}	Typical supply voltage		4.5		V
I_{CC}	Typical supply current		8		mA
f_{RF}	RF input frequency range	1.5		110	MHz
V_{RF-3dB}	sensitivity for –3dB limiting EMF with $Z_S = 75\Omega$, mute disabled		1.5		μV
V_{RF}	Maximum signal input for THD < 10%, $\Delta f = \pm 75$kHz EMF with $Z_S = 75\Omega$		200		mV
V_O	Audio output (RMS) with $R_L = 22k\Omega$, $\Delta f = \pm 22.5$kHz		75		mV

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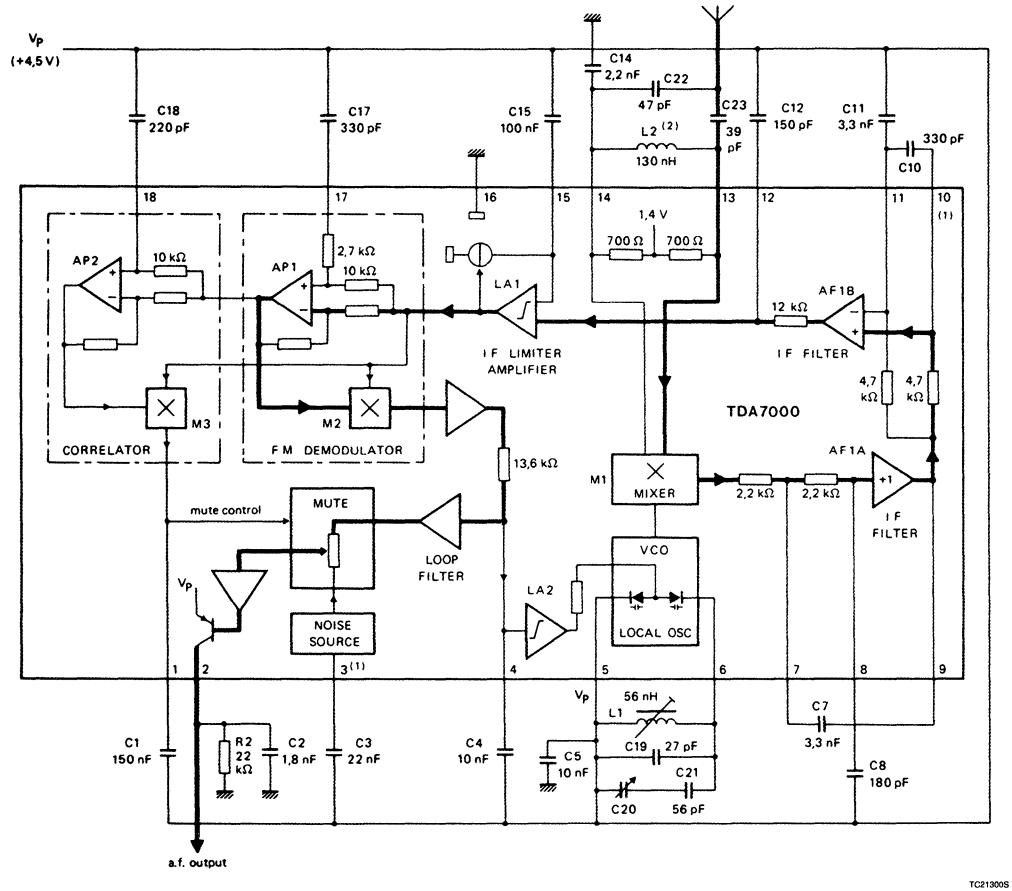
A Complete FM Radio on a Chip AN192



NOTES:
1 These pins are not used in the SO package version (TDA7010T) AP = All-Pass filter
2 L_2 is printed on the experimental PCB (Figure 12)
L_1 = Toko MC108 No 514 HNE 150013S13
C_{20} = Toko No 2A-15BT-R01

Figure 1. The TDA7000 as a Variable Capacitor-Tuned FM Broadcast Receiver

A Complete FM Radio on a Chip AN192

CIRCUIT DESCRIPTION

As shown in Figure 1, the TDA7000 consists of a local oscillator and a mixer, a two-stage active IF filter followed by an IF limiter/amplifier, a quadrature FM demodulator, and an audio muting circuit controlled by an IF waveform correlator. The conversion gain of the mixer, together with the high gain of the IF limiter/amplifier, provides AVC action and effective suppression of AM signals. The RF input to the TDA7000 for −3dB limiting is 1.5μV. In a conventional portable radio, limiting at such a low RF input level would cause instability because higher harmonics of the clipped IF signal would be radiated to the aerial. With the low IF used with the TDA7000, the radiation is negligible

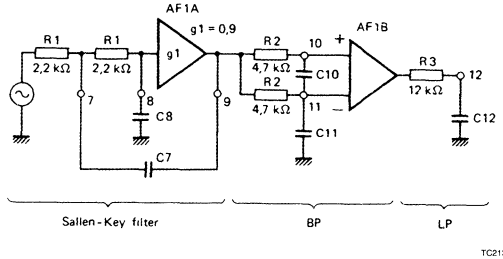
To prevent distortion with the low IF used with the TDA7000, it is necessary to restrict the IF deviation due to heavily modulated RF signals to ±15kHz. This is achieved with a frequency-locked loop (FLL) in which the output from the FM demodulator shifts the local oscillator frequency in inverse proportion to the IF deviation due to modulation

Active IF Filter

The first section of the IF filter (AF1A) is a second-order low-pass Sallen-Key circuit with its cut-off frequency determined by internal 2.2kΩ resistors and external capacitors C_7 and C_8. The second section (AF1B) consists of a first-order bandpass filter with the lower limit of the passband determined by an internal 4.7kΩ resistor and external capacitor C_{11}. The upper limit of the passband is determined by an internal 4.7kΩ resistor and external capacitor C_{10}. The final section of the IF filter consists of a first-order low-pass network comprising an internal 12kΩ resistor and external capacitor C_{12}. The overall IF filter therefore consists of a fourth-order low-pass section and a first-order high-pass section Design equations for the filter are given in Figure 2. Figure 3 shows the measured response for the filter.

FM Demodulator

The quadrature FM demodulator M2 converts the IF variations due to modulation into an audio frequency voltage. It has a conversion gain of −3.6V/MHz and requires phase quadrature inputs from the IF limiter/amplifier. As shown in Figure 4, the 90° phase shift is provided by an active all-pass filter which has about unity gain at all frequencies but can provide a variable phase shift, dependent on the value of external capacitor C_{17}



Sallen-Key circuit

$$A_{SK} = \frac{g}{1 + j\omega a - \omega^2 b} \quad \text{with } a = 2R_1C_8 \quad b = R_1{}^2C_7C_8$$

$$\text{With } f_O = \frac{1}{2\pi R_1\sqrt{(C_7C_8)}} \text{ and } Q = \frac{\sqrt{b}}{a} = 0.5\sqrt{\frac{C_7}{C_8}}$$

$$A_{SK} = \frac{g}{1 + \left(j\frac{\omega}{\omega_0} \times \frac{1}{Q}\right) - \frac{\omega^2}{\omega^2_0}}$$

For C_7 = 3.3nF, C_8 = 180pF, Q = 2.1 and f_O = 94kHz

Bandpass circuit

$$A_{BP} = \frac{1}{1 + j\omega C_{10}R_2} \times \frac{j\omega C_{11}R_2}{1 + j\omega C_{11}R_2 + \frac{j\omega C_{10}R_2}{1 + j\omega C_{10}R_2}}$$

$$\text{for } f_{LP} = \frac{1}{2\pi R_2 C_{10}} \text{ and } f_{HP} = \frac{1}{2\pi R_2 C_{11}}$$

$$A_{BP} = \frac{f_{LP}}{f_{HP}} \times \frac{1}{\left(1 + j\frac{f}{f_{HP}}\right)\left(1 - j\frac{f_{LP}}{f}\right) + 1}$$

For C_{10} = 330pF, C_{11} = 3.3nF, f_{LP} = 103kHz, f_{HP} = 10.3kHz

Low-Pass circuit

$$A_{LP} = \frac{1}{1 + j\omega C_{12}R_3}$$

$$\text{for } f_{LP} = \frac{1}{2\pi C_{12}R_3}$$

$$A_{LP} = \frac{1}{1 + j\frac{\omega}{\omega_{LP}}}$$

For C_{12} = 150pF, f_{LP} = 88.4kHz

Figure 2. IF Filter of the TDA7000

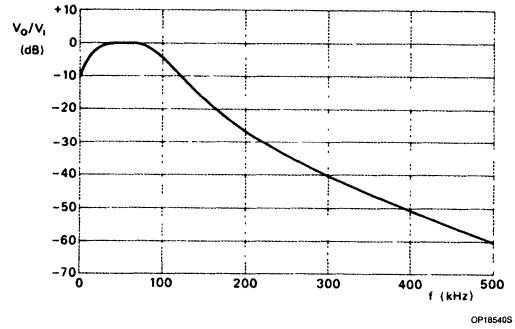
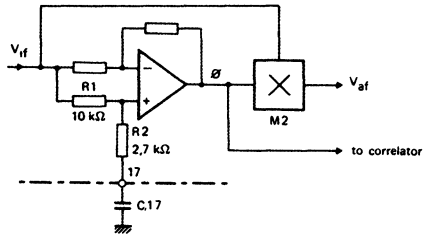


Figure 3. Measured Response of the IF Filter



With $R_2 = 0$
$\phi = -2\tan^{-1}\omega R_1 C_{17}$

for $\phi = -90°$, $C_{17} = \frac{1}{\omega R_1} = 227pF$

for $f_L = 70kHz$
To improve the performanace of the all-pass filter with the amplitude-limited IF waveform, R_2 has been added.
Since this influences the phase angle, the value of C_{17} must be increased by 45%, i.e., to 330pF for $f_{IF} = 70kHz$

Figure 4. FM Demodulator Phase Shift Circuit (All-Pass Filter)

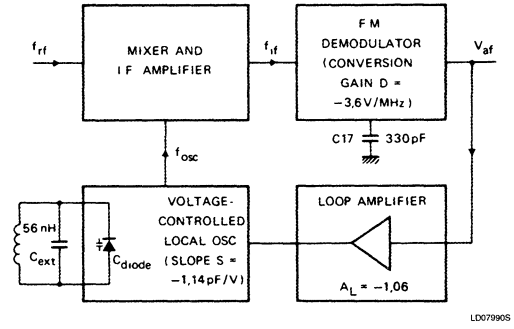
IF Swing Compression With the FLL

With a nominal IF as low as 70kHz, severe harmonic distortion of the audio output would occur with an IF deviation of ± 75kHz due to full modulation of a received FM broadcast signal. The FLL of the TDA7000 is therefore used to compress the IF swing by using the audio output from the FM demodulator to shift the local oscillator frequency in opposition to the IF deviation. The principle is illustrated in Figure 5, which shows how an IF deviation of 75kHz is compressed to about 15kHz. The THD is thus limited to 0.7% with ± 22.5kHz modulation, and to 2.3% with ± 75kHz modulation.

Correlation Muting System With Open FLL

A well-known difference between FM and AM is that, for FM, each station is received in at least three tuning positions. Figure 6 shows the frequency spectrum of the output from the demodulator of a typical portable FM radio receiving an RF carrier frequency-modulated with a tone of constant frequency and amplitude. In addition to the audio response at the correct tuning point in the center of Figure 6, there are two side responses due to the flanks of the demodulator S-curve. Because the flanks of the S-curve are nonlinear, the side responses have increased harmonic distortion. In Figure 6, the frequency and intensity of the side responses are functions of the signal strength, and they are separated from the correct tuning point by amplitude minima. However, in practice, the amplitude minima are not well defined because the modulation frequency and index are not constant and, moreover, the side response of adjacent channels often overlap.

High performance FM radios incorporate squelch systems such as signal strength-dependent muting and tuning deviation-dependent muting to suppress side responses. They also have a tuning meter to facilitate correct tuning. Although the TDA7000 is mainly intended for use in portables and clock radios, it incorporates a very effective new correlation muting system which suppresses interstation noise and spurious responses due to detuning to the flanks of the demodulator S-curve. The muting system is controlled by a circuit which determines the correlation between the waveform of the IF signal and an inverted version of it which is delayed (phase-shifted) by half the period of the nominal IF (180°). A noise generator works in conjunction with the muting system to give an audible indication of incorrect tuning.



$C_O = C_{EXT} + C_{STRAY} + C_{DIODE}$ with open loop = 49pF at f_O = 96MHz

Feedback factor $\beta = \frac{A_L S f_O}{2C_O}$

Open-loop conversion gain = D = −3 6V/MHz

Closed-loop conversion gain = $\frac{D}{1 + D\beta}$ = 0 68V/MHz for f_O = 96MHz

Modulation compression factor K = $\frac{\text{open-loop gain}}{\text{closed-loop gain}} = \frac{3\ 6V/MHz}{0\ 684V/MHz} \approx 5$

$\Delta f_{OSC} = \Delta f_{RF}\left(1 - \frac{1}{K}\right)$

$\Delta f_{IF} = \frac{\Delta f_{RF}}{K}$

for Δf_{RF} = 75kHz, $\Delta f_{OSC} \approx$ 60kHz, $\Delta f_{IF} \approx$ 15kHz

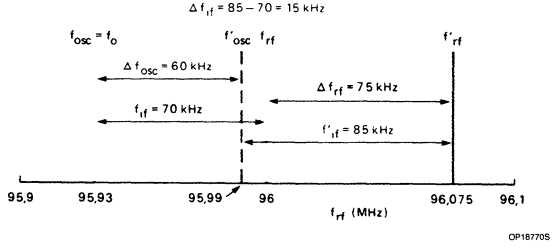


Figure 5. IF Swing Compression with the FLL

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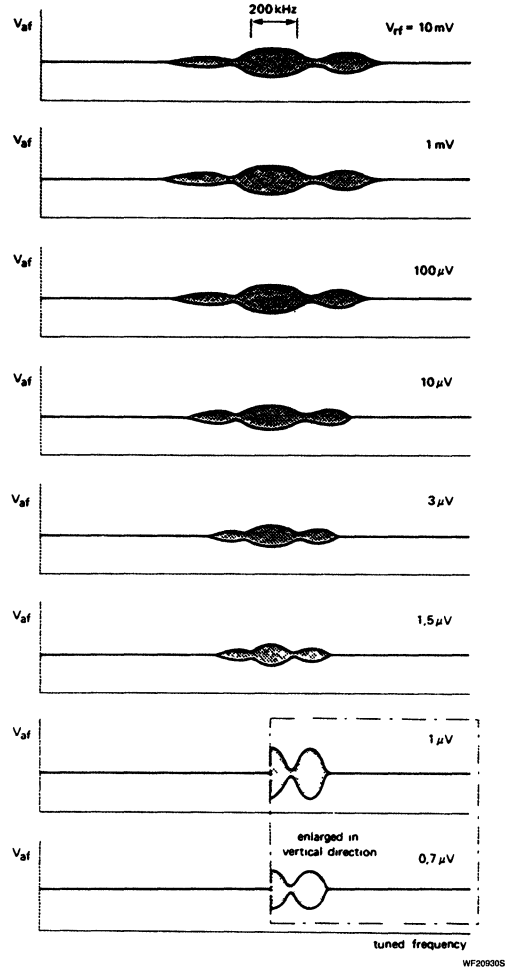


Figure 6. Audio Signal of a Typical Portable Radio as a Function of Tuned Frequency With RF Input as a Parameter. The Modulation and Amplitude are Both Constant

Figure 7 illustrates the function of the muting system. Signal IF' is derived by delaying the IF signal by half the period of the nominal IF and inverting it. With correct tuning as shown in Figure 7a, the waveforms of the two signals are identical, resulting in large correlation. In this situation, the audio signal is not muted. With detuning as shown in Figure 7b, signal IF' is phase-shifted with respect to the IF signal. The correlation between the two waveforms is therefore small and the audio output is muted. Figure 7c shows that, because of the low Q of the IF filter, noise causes considerable fluctuations of the period of the IF signal waveform. There is then small correlation between the two waveforms and the audio is muted. The correlation muting system thus suppresses noise and side responses due to detuning to the flanks of the demodulator S-curve. Since the mute threshold is much lower than that obtained with most other currently-used muting systems, this muting system is ideal for portable radios which must often receive signals with a level only slightly above the input noise.

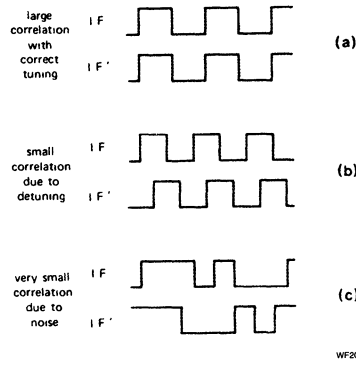
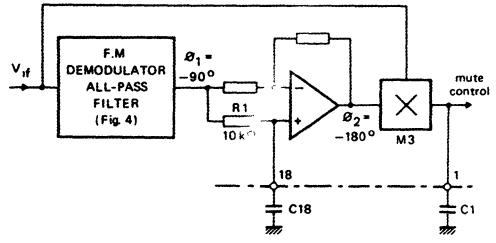


Figure 7. Function of the Correlation Muting System

As shown in Figure 8, the correlation muting circuit consists of all-pass filter AP2 connected in series with FM demodulator all-pass filter AP1 and adjusted by an external capacitor to provide a total phase shift of 180°. The output from AP2 is applied to mixer M3 which determines the correlation between the undelayed limited IF signal at one of its inputs and the delayed and inverted version of it at its other input. The output from mixer M3 controls a muting circuit which feeds the demodulated audio signal to the output when the correlation is high, or feeds the output from a noise source to the output to give an audible indication of incorrect tuning when the correlation is low. The switching of the muting circuit is progressive (soft muting) to prevent the generation of annoying audio transients. The output from mixer M3 is available externally at Pin 1 and can also used to drive a detuning indicator.



$$\phi_2 = -2 \tan^{-1} \omega R_1 C_{18} - \phi_1$$

$$\text{for } \phi_2 = -180^\circ \; C_{18} = \frac{1}{\omega R_1}$$

$$\text{for } f_{if} = 70 \text{ kHz}, \; C_{18} = 227 \text{ pF}$$

TC21310S

Figure 8. Correlator of the TDA7000

Figure 9 shows that there are two regions where the demodulated audio signal is fed to the output because the muting is inactive. One region is centered on the correct tuning point f_L. The other is centered on the image frequency $-f_L$. The image response is therefore not suppressed by the muting system when the frequency-locked loop is open. When the loop is closed, the time constant of the muting system, which is determined by external capacitor C_1, prevents the image response being passed to the audio output. This is described under the next heading.

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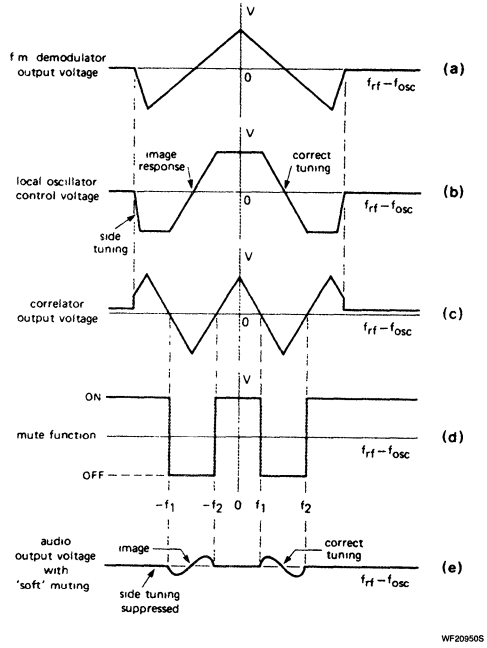
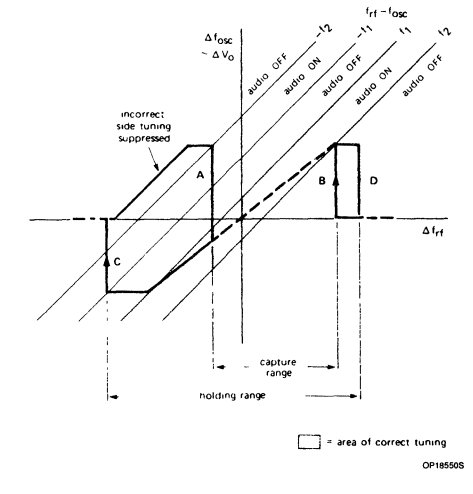


Figure 9. Operation of the Correlation Muting System With Open-Loop FLL



NOTE:
The slope of the correct tuning line is such that a 75kHz deviation of f_{RF} causes a 15kHz deviation of $f_{RF}-f_{OSC}$

Figure 10. Closed-Loop Response of the FLL

Correlation Muting System With Closed FLL

The closed-loop response of the FLL is shown in Figure 10, in which the point of origin is the nominal IF ($f_{RF}-f_{OSC}=f_L$). With correct tuning, the muting is inactive and the audio signal is fed to the output. Spurious responses due to the flanks of the demodulator S-curve which occur outside the IF band $-f_2$ to f_2 are suppressed because the muting is active. Fast transients of the audio signal due to locking of the loop (A and B), and to loss of lock (C and D) are suppressed in two ways.

Lock and loss of lock transients B and D occur when the IF is greater than f_2 and are therefore suppressed because the muting is active. The situation is different during loss of lock transient C because the muting is only active for the last part of the transient. To completely suppress this transient, capacitor C_1 in Figure 1 holds the muting control line positive (muting active) during the short interval while the IF traverses from $-f_1$ to $-f_2$. The same applies for lock transient A during the short interval while the IF traverses from $-f_2$ to $-f_1$. Since the image response occurs halfway between $-f_1$ and $-f_2$, it is also suppressed.

Figure 11 shows the audio output from the TDA7000 radio as a function of tuned frequency with aerial signal level as a parameter. Compared with the similar diagram for a typical conventional portable radio (Figure 6), there are three important improvements:

1. There are no side responses due to the flanks of the demodulator S-curve. This is due to the action of the correlation muting system (soft mute) which combines the function of a detuning-dependent muting system with that of a signal strength-dependent muting system.

2. The correct tuning frequency band is wide, even with weak aerial signals. This is due to the AFC action of the FLL which reduces a large variation of aerial input frequency (equivalent to detuning) to a small variation of the IF. There is no audio distortion when the radio is slightly detuned.

3. Although the soft muting system remains operative with low level aerial signals, there is no degradation of the audio signal under these conditions. This is due to the high gain of the IF limiter/amplifier which provides −3dB limiting of the IF signal with an aerial input level of 1.5μV. However, the soft muting action does reduce the audio output level with low level aerial signals.

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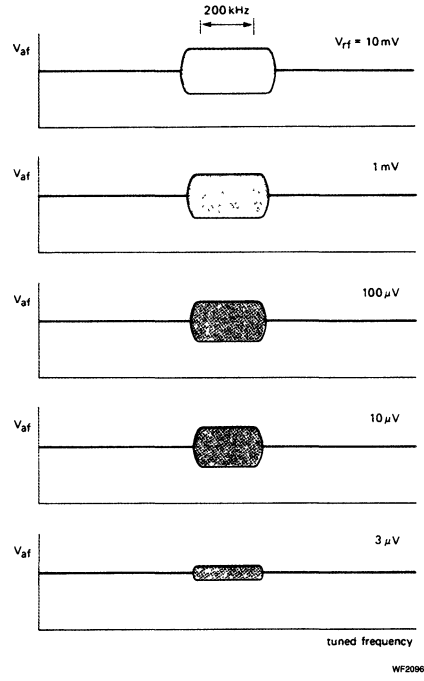

NOTE:
The modulation frequency and amplitude are both constant.

Figure 11. Audio Signal of the TDA7000 as a Function of the Tuned Frequency With RF Input as a Parameter

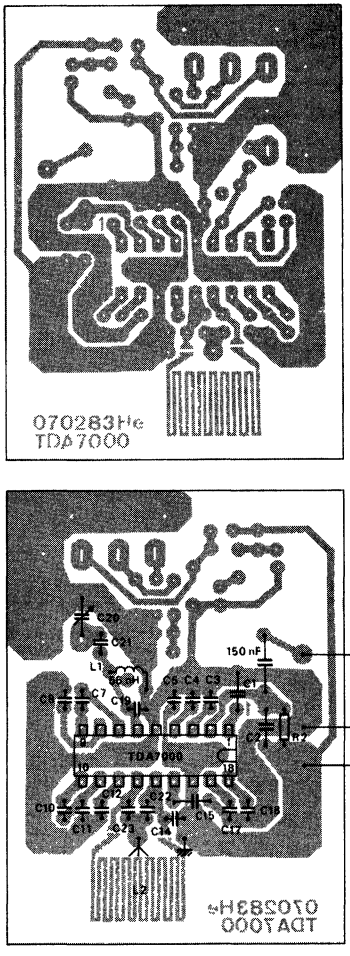

Figure 12. Experimental Printed Wiring Board for the Circuit of Figure 1

RECEIVER CIRCUITS

Circuits With Variable Capacitor Tuning

The circuit diagram of the complete mono FM radio is given in Figure 1. An experimental printed-wiring board layout is given in Figure 12. Special attention has been paid to supply lines and the positioning of large-signal decoupling capacitors.

The functions of the peripheral components of Figure 1 not already described are as follows:

C_1 — Determines the time constant required to ensure muting of audio transients due to the operation of the FLL.

C_2 — Together with R_2 determines the time constant for audio de-emphasis (e.g., $R_2C_2 = 40\mu s$).

C_3 — The output level from the noise generator during muting increases with increasing value of C_3. If silent mute is required, C_3 can be omitted.

C_4 — Capacitor for the FLL filter. It eliminates IF harmonics at the output of the FM demodulator. It also determines the time constant for locking the FLL and influences the frequency response.

C_5 — Supply decoupling capacitor which must be connected as close as possible to Pin 5 of the TDA7000.

C_7 to C_{12}, C_{17} and C_{18} — Filter and demodulator capacitors. The values shown are for an IF of 70kHz. For other intermediate frequencies, the values of these capacitors must be changed in inverse proportion to the IF change.

C14 — Decouples the reverse RF input. It must be connected to the common return via

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A Complete FM Radio on a Chip AN192

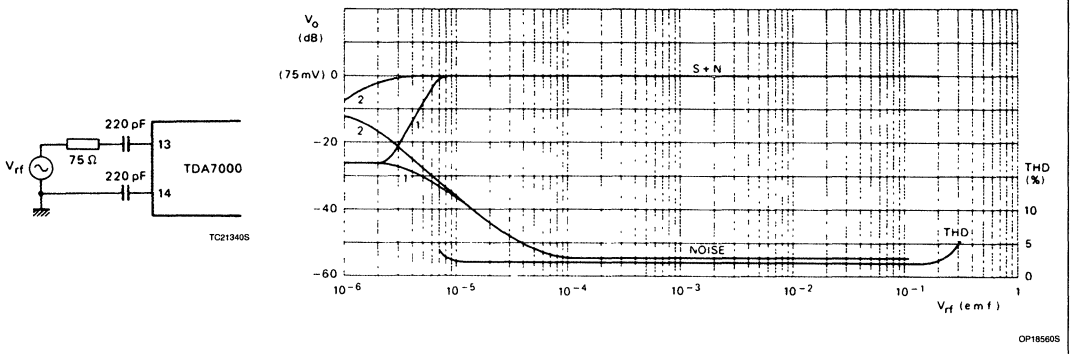
a good quality short connection to ensure a low-impedance path. Inductive or capacitive coupling between C_{14} and the local oscillator circuit or IF output components must be avoided.

C_{15} — Decouples the DC feedback for IF limiter/amplifier LA_1.

C_{19} and C_{21} — Local oscillator tuning capacitors. Their values depend on the required tuning range and on the value of tuning capacitor C_{20}.

C_{22}, C_{23}, L_1, L_2 — The values given are for an RF bandpass filter with Q = 4 for the European and U.S.A. domestic FM broadcast band (87.5MHz to 108MHz). For reception of the Japanese FM broadcast band (76MHz to 91MHz), L_1 must be increased to 78nH and L_2 must be increased to 150nH. If stopband attenuation for high level AM or TV signals is not required, L_2 and C_{22} can be omitted and C_{23} changed to 220pF.

R_2 — The load for the audio output current source. It determines the audio output level, but its value must not exceed 22kΩ for V_{CC} = 4.5V, or 47kΩ for V_{CC} = 9V.



NOTES:
The curves numbered 1 were measured with the muting system active The curves numbered 2 were measured with the muting system disabled by injecting about 20μA into Pin 1 of the TDA7000 The input frequency was 96MHz modulated with 1kHz with a deviation of ±22 5kHz for the output level curves, and ±75kHz for the distortion curve

Figure 13. Audio Output as a Function of Input EMF

Performance of the Circuit V_{CC} = 4.5V, T_A = 25°C, f_{RF} = 96MHz, V_{RF} = 0.2mV EMF from a 75Ω source, modulated with $\Delta f = \pm 22.5$kHz, f_M = 1kHz. Noise voltage measured unweighted over the bandwidth 300Hz to 20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TYP	MAX	UNIT
	Sensitivity (EMF voltage) for −3dB limiting:			
EMF	muting disabled	1.5		μV
EMF	for −3dB muting	6		μV
EMF	for (S + N)/N = 26dB	5.5		μV
	Signal handling (EMF voltage)			
EMF	for THD < 10%; $\Delta f = \pm 75$kHz	200		mV
(S + N)/N	Signal-to-noise ratio (see Figure 13)	60		dB
	Total harmonic distortion (see Figure 13)			
THD	at $\Delta f = \pm 22.5$kHz	0.7		%
THD	at $\Delta f = \pm 75$kHz	2.3		%
	AM suppression (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1kHz; $\Delta f = \pm 75$kHz			
AMS	AM signal: f_m = 1kHz; m = 80%	50		dB
RR	Ripple rejection (ΔV_{CC} = 100 mV; f = 1kHz)	10		dB
$V_{6-5\ RMS}$	Oscillator voltage (RMS value) at Pin 6	250		mV
Δf_{OSC}	Variation of oscillator frequency with supply voltage (ΔV_{CC} = 1V)	60		kHz/V
S_{+300}	Selectivity	45		dB
S_{-300}		35		dB
Δf_{RF}	AFC range	±300		kHz
B	Audio bandwidth at ΔV_O = 3dB measured with pre-emphasis (t = 50μs)	10		kHz
$V_{O(RMS)}$	AF output voltage (RMS value) at R_L = 22kΩ	75		mV
	Load resistance for audio output current source			
R_L	at V_{CC} = 4.5V		22	kΩ
R_L	at V_{CC} = 9.0V		47	kΩ

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A Complete FM Radio on a Chip AN192

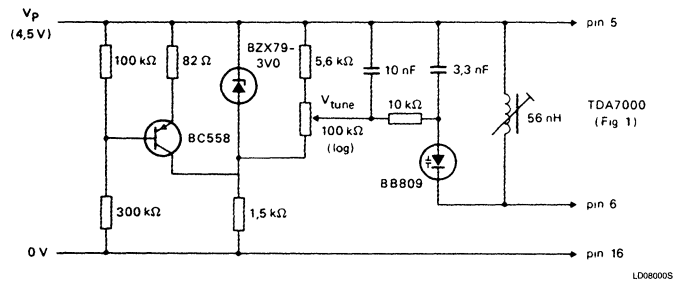


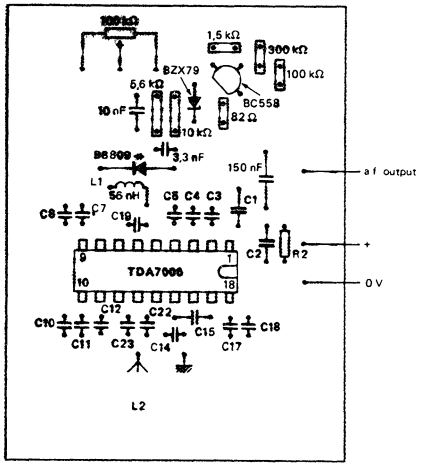
Figure 14. Variable-Capacitance Diode Tuning for the Local Oscillator. Additional Measures Must be Taken to Ensure Temperature Stability

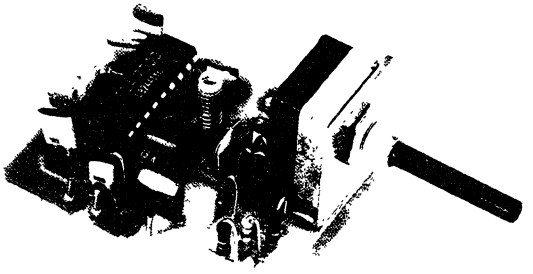
Circuit With Variable-Capacitance Diode Tuning

Since it is only necessary to tune the local oscillator coil, it is very simple to modify the circuit of Figure 1 for variable-capacitance diode tuning. The modifications are shown in Figure 14. A circuit board layout for the modified receiver and a photograph of a complete laboratory model are shown in Figure 15.

Narrow-Band FM Receiver

The TDA7000 can also be used for reception of narrowband FM signals. In this case, the local oscillator is crystal-controlled (as shown in Figure 16) and there is therefore hardly any compression of the IF swing by the FLL. The deviation of the transmitted carrier frequency due to modulation must therefore be limited to prevent severe distortion of the demodulated audio signal.





NOTE:
This is the same PC Board as shown in Figure 12

Figure 15. Circuit Board Layout and Complete Model of a TDA7000 Radio With Variable-Capacitance Diode Tuning

A Complete FM Radio on a Chip AN192

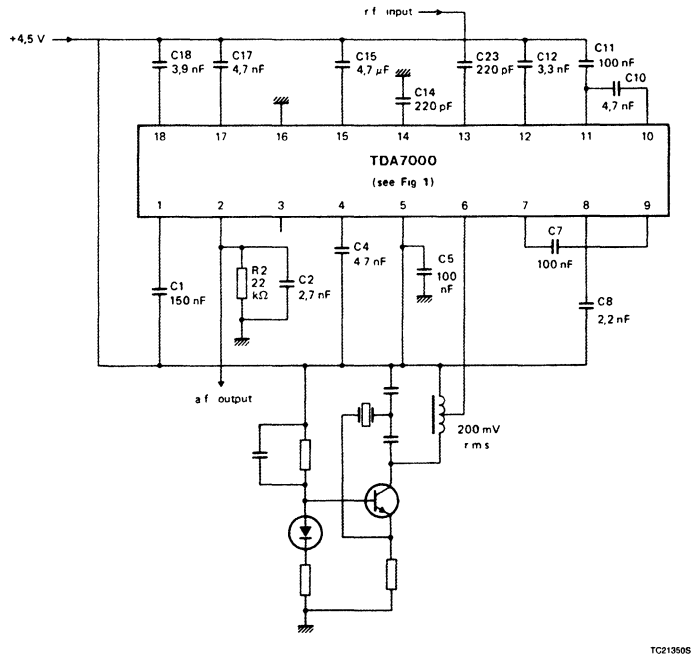


Figure 16. A Narrow-Band FM Receiver With a Crystal-Controlled Local Oscillator

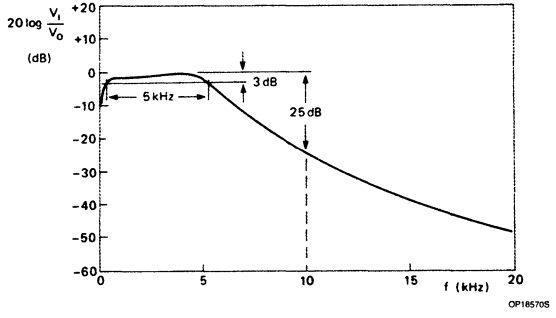


Figure 17. IF Selectivity for the Narrow-Band FM Receiver

The component values in Figure 16 result in an IF of 4.5kHz and an IF bandwidth of 5kHz (Figure 17). If the IF is multiplied by N, the values of capacitors C_{17} and C_{18} in the all-pass filters and the values of filter capacitors C_7, C_8, C_{10}, C_{11}, and C_{12} must be multiplied by 1/N. For improved IF selectivity to achieve greater adjacent channel attenuation, second-order networks can be used in place of C_{10} and C_{11}.

In this circuit the detuning noise generator is not used. Since the circuit is mainly for reception of audio signals, the audio output must be passed through a low-pass Chebyshev filter to suppress IF harmonics.

AUDIO AMPLIFIER AND DETUNING INDICATOR CIRCUITS

Audio output stages suitable for use with the TDA7000 are shown in Figures 18 and 19. Figure 20 shows how the muting signal can be used to operate an LED to give an indication of detuning.

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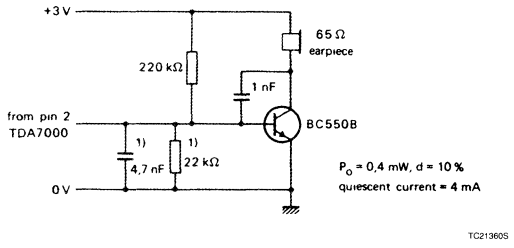
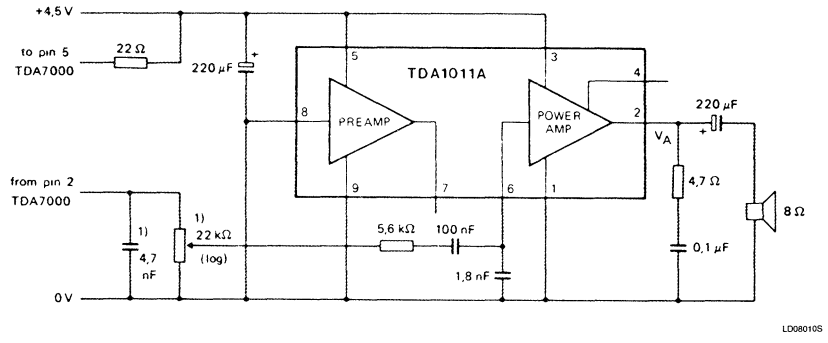


NOTE.
1 These components replace R2 and C2 in Figure 1

Figure 18. A 0.4mW Transistor Audio Output Stage Without Volume Control for Driving an Earpiece



NOTE:
1 These components replace C2 and R2 in Figure 1 P_o = 250mW, d = 10% quiescent current = 8mA

Figure 19. An Integrated 250mW Audio Output Stage

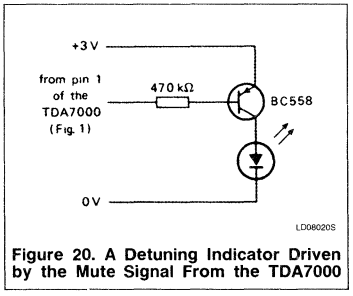


Figure 20. A Detuning Indicator Driven by the Mute Signal From the TDA7000

ACKNOWLEDGEMENTS

The authors wish to acknowledge the information provided by D Kasperkovitz and H.v Rumpt for incorporation in this article

REFERENCE

KANOW, W. and SIEWERT, I., 'Integrated circuits for hi-fi radios and tuners', *Electronic Components and Applications,* Vol. 4, No 1, November 1981, pp 11 to 27.

Signetics

AN193
TDA7000 for Narrow-Band FM Reception

Application Note

Linear Products

Author: W. V. Dooremolen

INTRODUCTION

Today's cordless telephone sets make use of duplex communication with carrier frequencies of about 1.7MHz and 49MHz.

- In the base unit incoming telephone information is frequency-modulated on a 1.7MHz carrier.
- This 1.7MHz signal is radiated via the AC mains line of the base unit.
- The remote unit receives this signal via a ferrite bar antenna.
- The remote unit transmits the call signals and speech information from the user at 49MHz via a telescopic antenna.
- The base unit receives this 49MHz FM-modulated signal via a telescopic aerial.

Today's Remote Unit Receivers

In cordless telephone sets, a normal superheterodyne receiver is used for the 1.7MHz handset. The suppression of the adjacent channel at, e.g., 30kHz, must be 50dB, and the bandwidth of the channel must be 6 – 10kHz for good reception. Therefore, an IF frequency of 455kHz is chosen. Since at this frequency there are ceramic filters with a bandwidth of 9kHz (AM filters), the 1.7MHz is mixed down to 455kHz with an oscillator frequency of 2.155MHz. Now there is an image reception at 2.61MHz. To suppress this image sufficiently, there must be at least two RF filter sections at the input of the receiver.

The ceramic IF filter with its subharmonics is bad for far-off selectivity, so there must be an extra LC filter added between the mixer output and the ceramic filter.

After the selectivity there is a hard limiter for AGC function and suppression of AM.

Next, there is an FM detector which must be accurate because it must detect a swing of ±2.5kHz at 455kHz; therefore, it must be tuned.

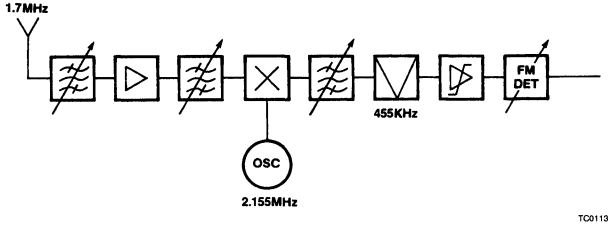


Figure 1. Remote-unit Receiver: 1.7MHz

Figure 1 shows the block diagram which fulfills this principal. The total number of alignment points of this receiver is then 5:

2 RF filters
1 Oscillator
1 IF filter
1 FM detector

5 Alignments

A Remote Unit Receiver With TDA7000

The remote unit receiver (see Figure 2) has as its main component the IC TDA7000, which contains mixer, oscillator, IF amplifiers, a demodulator, and squelch functions.

To avoid expensive filtering (and expensive filter-adjustments) in RF, IF, and demodulator stages, the TDA7000 mixes the incoming signal to such a low IF frequency that filtering can be realized by active RC filters, in which the active part and the Rs are integrated.

To select the incoming frequency, only one tuned circuit is necessary: the oscillator tank circuit. The frequency of this circuit can be set by a crystal.

IMAGE RECEPTION

For today's concept, a number of expensive components are necessary to suppress the image sufficiently. The suppression of the image is very important because the signal at the image can be much larger than the wanted signal and there is no correlation between the image and the wanted signal.

In a concept with 455kHz IF frequency, the 1.7MHz receiver has image reception at 2.155MHz. In the TDA7000 receiver, the IF frequency is set at 5kHz. Then the 1.7MHz receiver (with 1.695MHz oscillator frequency) has image reception at 1.69MHz, which is at 10kHz from the required frequency (see Figure 3).

An IF frequency of 5kHz has been chosen because:

- this frequency is so low, there will be no neighboring channel reception at the image frequency.
- this frequency is not so low that at maximum deviation (maximum modulation) distortion could occur (folding distortion, caused by the higher-order bessel functions)
- this frequency gives the opportunity to obtain the required neighboring channel suppression with minimum components in the IF selectivity.

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TDA7000 for Narrow-Band FM Reception AN193

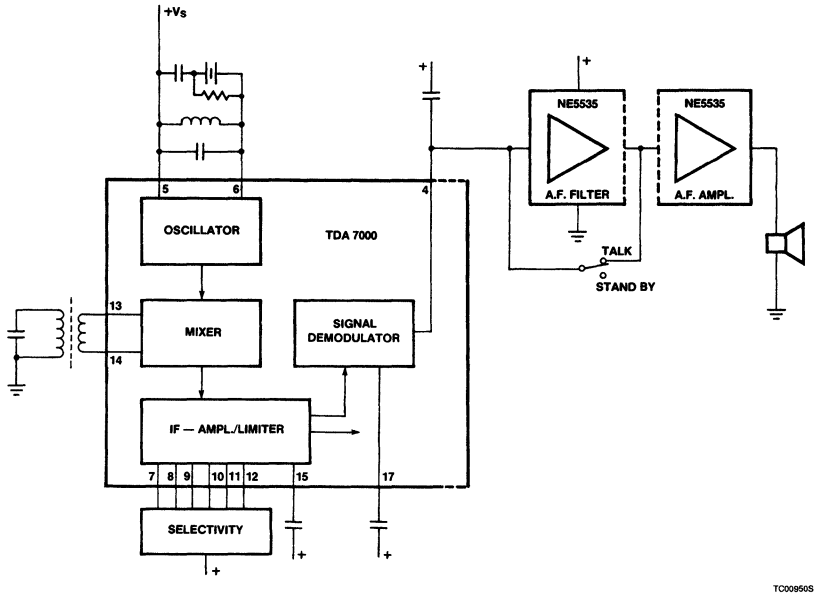

Figure 2

CIRCUIT DESCRIPTION (see Figure 2)

When a remote unit is at "power-on" in the "standby" position, it is ready to receive a "bell signal". A bell signal coming through the telephone line will set the base unit in the mode of transmitting a 1.7MHz signal, modulated with, e.g., 0.75kHz with ±3kHz deviation.

The ferrite antenna of the remote unit receives this signal and feeds it to the mixer, where it is converted into a 5kHz IF signal.

Before the RF signal enters the mixer (at Pins 13 and 14) it passes RF selectivity, taking care of good suppression of unwanted signals from, e.g., TV or radio broadcast frequencies. The IF signal from the mixer output passes IF selectivity (Pins 7 to 12) and the IF amplifier/limiter (Pin 15), from which the output is supplied to a quadrature demodulator (Pin 17). Due to the low IF frequency, cheap capacitors can be used for both IF selectivity and the phase shift for the quadrature demodulator.

The AF output of the demodulator (Pin 4) is fed to the AF filter and AF amplifier NE5535.

The RF Input Circuit

As the image reception is an in-channel problem, solved by the choice of IF frequency and IF selectivity, the RF input filter is only required for stopband selectivity (a far-off selectivity to suppress unwanted large signals from, e.g., radio broadcast transmitters).

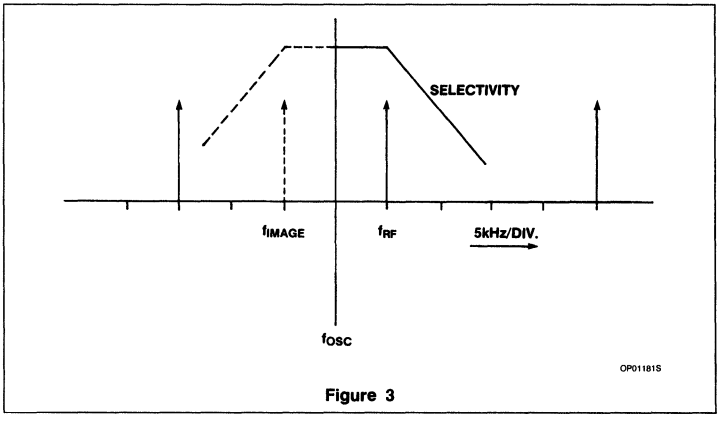

Figure 3

In a remote unit receiver at 1.7MHz, this filter is at the ferrite rod. Figure 4 shows the bandpass behavior of such a filter at 1.7MHz.

The Mixer

The mixer conversion gain depends on the level of the oscillator voltage as shown in Figure 5, so the required oscillator voltage at Pin 6 is 200mV$_{RMS}$.

The Oscillator

To obtain the required frequency stability in a cordless telephone set, where adjacent channels are at 20 or 30kHz, crystal oscillators are commonly used.

The crystal oscillator circuits usable for this kind of application always need an LC-tuned resonant circuit to suppress the other modes of the crystal. In this type of oscillator (see Figure 6 as an example) the crystal is in the feedback line of the oscillator amplifier. Inte-

TDA7000 for Narrow-Band FM Reception AN193

gration of such an amplifier should give a 2-pin oscillator.

The TDA7000 contains a 1-pin oscillator. An amplifier with current output develops a voltage across the load impedance.

Voltage feedback is internal to the IC.

To obtain a crystal oscillator with the TDA7000 1-pin concept, a parallel circuit configuration as shown in Figure 7 has to be used.

Explanation of this circuit:

a. Without the parallel resistor R_P —
Figure 8 shows the relevant part of the equivalent circuit. There are three frequencies where the circuit is in resonance (see Figure 9, and the frequency response for "impedance" and "phase", shown in Figure 10). The real part of the highest possible oscillation frequency dominates, and, as there is also a zero-crossing of the imaginary part, this highest frequency will be the oscillator frequency. However, this frequency (f_{PAR}) is not crystal-controlled; it is the LC oscillation, in which the parasitic capacitance of the crystal contributes.

b. With parallel resistor R_P —
The frequency response (in "amplitude" and "phase") of the oscillator circuit of Figure 7 *with* R_P is given in Figure 11. As the resistor value of R_P is large related to the value of the crystal series resistance R_1 or R_3, the influence of R_P at crystal resonances is negligible. So, at crystal resonance (see Figure 9b), R_3 causes a circuit damping

$$R = \frac{1}{W^2} \cdot R_3 \cdot C_1^2 + R_3 \left(1 + \frac{C_2}{C_1}\right)^2.$$

However, at the higher LC-oscillation frequency f_{PAR} (see Figure 9c), R_P reduces the circuit impedance R_O to

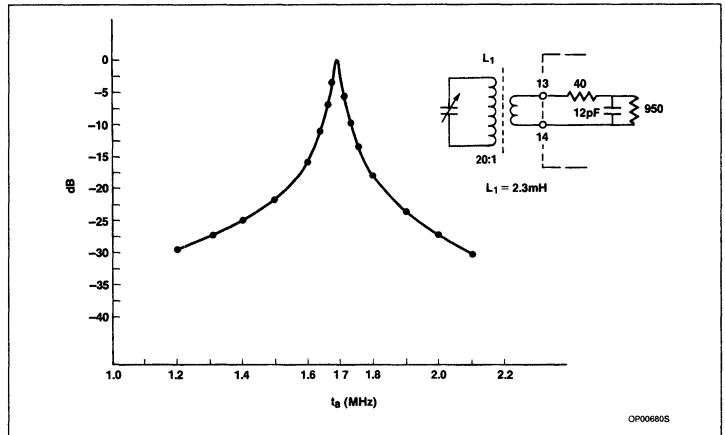

Figure 4

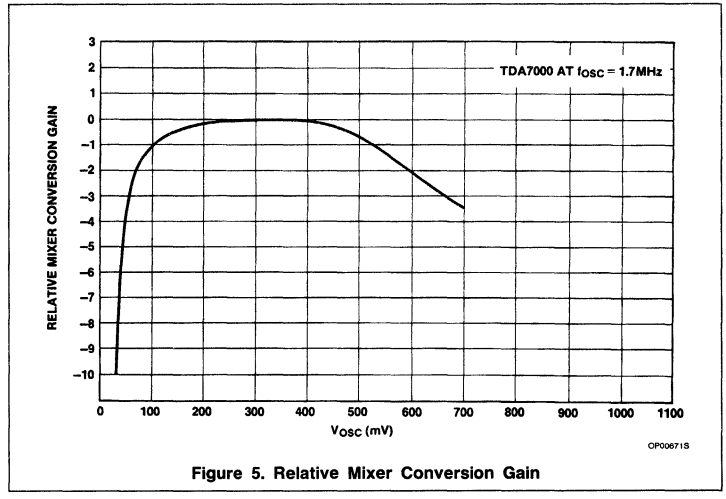

Figure 5. Relative Mixer Conversion Gain

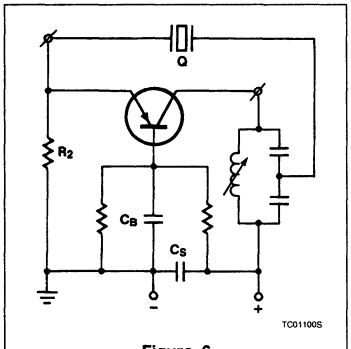

Figure 6

$$\frac{R_O \cdot R_{DAMPING}}{R_O + R_{DAMPING}} = R_C$$

where

$$R_{DAMPING} = \frac{1}{W_2} \cdot R_P \cdot C_1^2 \cdot R_P \left(1 + \frac{C_2}{C_1}\right)^2.$$

Thus a damping resistor parallel to the crystal (Figure 7) damps the parasitic LC oscillation at the highest frequency. (Moreover, the imaginary part of the impedance at this frequency shows incorrect zero-crossing.)

Taking care that $R_P \gg R_{SERIES}$, the resistor is too large to have influence on the crystal resonances. Then with the impedance R_C at the parasitic resonance lower than R at crystal resonance, oscillation will only take place at the required crystal frequency, where impedance is maximum and phase is correct (in this example, at third-overtone resonance).

Remarks:

a. It is advised to avoid inductive or capacitive coupling of the oscillator tank circuit with the RF input circuit by careful positioning of the components for these circuits and by avoiding common supply or ground connections.

The IF Amplifier

Selectivity

Normal selectivity in the TDA7000 is a fourth-order low-pass and a first-order high-pass

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filter. This selectivity can be split up in a Sallen and Key section (Pins 7, 8, 9), a bandpass filter (Pins 10, 11), and a first-order low-pass filter (Pin 12).

Some possibilities for obtaining required selectivity are given:

a. In the basic application circuit, Figure 12a, the total filter has a bandwidth of 7kHz and gives a selectivity at 25kHz IF frequency of 42dB.

   In this filter the lower limit of the passband is determined by the value of C4 at Pin 11, where C3 at Pin 10 determines the upper limit of the bandpass filter section.

b. To obtain a higher selectivity, there is the possibility of adding a coil in series with the capacitor between Pin 11 and ground. The so-obtained fifth-order filter has a selectivity at 25kHz of 57dB (see Figure 12b).

c. If this selectivity is still too small, there is a possibility of increasing the 25kHz selectivity to 65dB by adding a coil in series with the capacitor at Pin 11 to ground. In this application, where at 5kHz IF frequency an adjacent channel at −30kHz will cause a (30−5) = 25kHz interfering IF frequency, the pole of the last-mentioned LC filter (trap function) is at 25kHz (see Figure 12c).

For cordless telephone sets with channels at 15kHz distance, the filter characteristics are optimum as shown in the curves in Figure 13, in which case the filters are dimensioned for 5kHz IF bandwidth (instead of 7kHz). So for this narrow channel spacing application, the required selectivity is obtained by reducing the IF bandwidth; this at the cost of up to 2dB loss in sensitivity.

NOTE:
At 5kHz IF frequency adjacent channels at ± 15kHz give undesired IF frequencies of 20kHz and 10kHz, respectively

Limiter/Amplifier

The high gain of the limiter/amplifier provides AVC action and effective suppression of AM modulation. DC feedback of the limiter is decoupled at Pin 15.

The Signal Demodulator

The signal demodulator is a quadrature demodulator driven by the IF signal from the limiter and by a phase-shifted IF signal derived from an all-pass filter (see Figure 14).

This filter has a capacitor connected at Pin 17 which fixes the IF frequency. The IF frequency is where a 90 degree phase shift takes care of the center position in the demodulator output characteristics (see Figure 15, showing the demodulator output (at Pin 4) as a function of the frequency, at 1mV input signal).

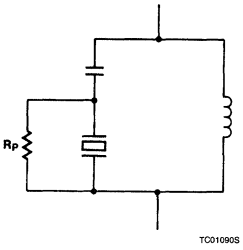

Figure 7

The AF Output Stage

The signal demodulator output is available at Pin 4, where a capacitor, C, serves for elimination of IF harmonics. This capacitor also influences the audio frequency response. The output from this stage, available at Pin 2, has an audio frequency response as shown in Figure 16, curve a. The output at Pin 2 can be muted.

Output Signal Filtering

Output signal filtering is required to suppress the IF harmonics and interference products of these harmonics with the higher-order bessel components of the modulation. Active filtering with operational amplifiers has been used (see Figure 17). The frequency response of such a filter is given in Figure 16, Curve b, for an active second-order filter with an additional passive RC filter.

Output Amplification

The dimensioning of the operational amplifier of Figure 17a results in no amplification of the AF signal. In case amplification of this op amp is required, a feedback resistor and an RC filter at the reverse input can be added (see Figure 17b, for about 30dB amplification).

MEASUREMENTS

For sensitivity, signal handling, and noise behavior information in a standard application as shown in Figure 18, the signal and noise output as a function of input signal has been measured at 1.7MHz, at 400Hz modulation where the deviation is ± 2.5kHz (see Figure 19). As a result the S+N/N ratio is as given in Figure 19, Curve 3.

APPENDIX

RF-Tuned Input Circuit at 46MHz

In Figure 20 a filter is given which matches at 46MHz a 75Ω aerial to the input of the TDA7000. Extra suppression of RF frequencies outside the passband has been obtained by a trap function.

RF Pre-Stage at 46MHz

For better quality receivers at 46MHz, an RF pre-stage can be added (see Figure 21) to improve the noise figure. Without this transistor, a noise figure F = 11dB was found. With a transistor (BFY 90) with RC coupling at 3mA, F = 7dB or at 6mA F = 6dB.

With a transistor stage having an LC-tuned circuit, one can obtain F = 7dB at I = 0.3mA.

NOTE:
The noise figure includes image-noise

An LC Oscillator at 1.7MHz

An LC oscillator can be designed with or without AFC. If for better stability external AFC is required, one can make use of the DC output of the signal demodulator, which delivers 80mV/kHz at a DC level of 0.65V to +supply. An LC oscillator as shown in Figure 22a, using a capacitor with a temperature coefficient of −150ppm, gives an oscillator signal of 190mV, with a temperature stability of 1kHz/50°.

With the use of AFC, as shown in Figure 22b, one can further improve the stability, as AFC reduces the influence of frequency changes in the transmitter (due to temperature influence or aging). The given circuit gives a factor 2 reduction. Note that the temperature behavior of the AFC diode has to be compensated. In Figure 22b, with BB405B having a capacitance of 18pF at the reverse voltage V4 = 0.7V, the temperature coefficient of the capacitor C has to be −200ppm.

AF Output Possibilities

The AF output from the signal demodulator, available at Pin 4, depends on the slope of the demodulator as shown in Figure 15. The TDA7000 AF output is also available at Pin 2 (see Figure 23). The important difference between the output at Pin 2 and the output at Pin 4 is that the Pin 4 output is amplified and limited before it is led to Pin 2 (see Figure 24). Moreover, the Pin 2 output is controlled by the mute function, a mute which operates in case the received signal is bad as far as noise and distortion are concerned.

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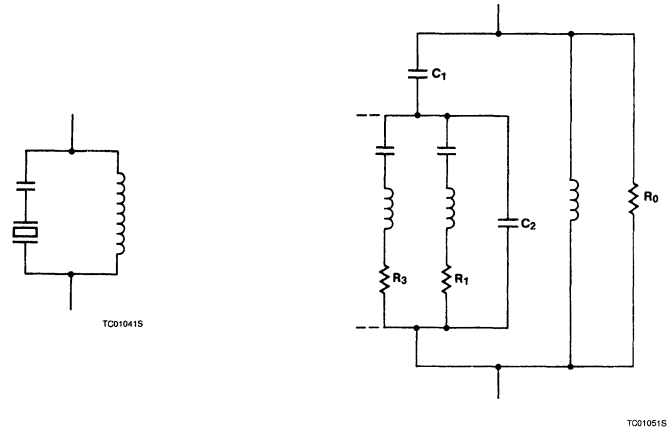
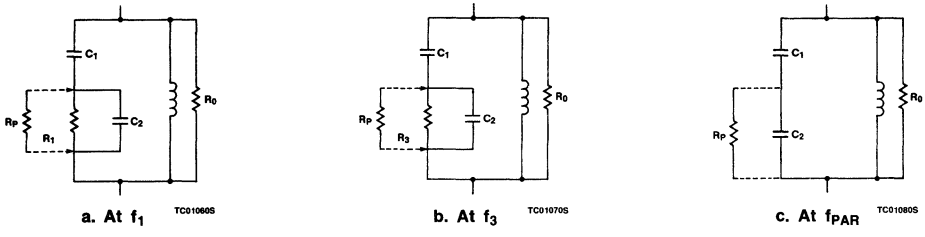


a. b.

Figure 8



a. At f_1 b. At f_3 c. At f_{PAR}

Figure 9

The Pin 2 output delivers a higher AF signal; however, the AF output spectrum shows more mixing products between IF harmonics and modulation frequency harmonics. This is due to the "limited output situation" at Pin 2. In narrow-band application with relatively large deviation these products are so high that extra AF output filtering is required and, moreover, the IF center frequency has to be higher compared to the concept, using AF output at Pin 4.

So for those sets where the mute/squelch function of the TDA7000 is not used, and the higher AF output is not required, the use of the AF output at Pin 4 is advised, giving less interfering products and simplified AF output filtering.

Squelch and Squelch Indication

The TDA7000 contains a mute function, controlled by a "waveform correlator", based on the exactness of the IF frequency.

The correlation circuit uses the IF frequency and an inverted version of it, which is delayed (phase-shifted) by half the period of nominal IF. The phase shift depends on the value of the capacitor at Pin 18 (see Figure 23).

This mute also operates at low field strength levels, where the noise in the IF signal indicates bad signal definition. (The correlation between IF signal and the inverted phase-shifted version is small due to fluctuations caused by noise; see Figure 25.) This field strength-dependent mute behavior is shown in Figure 26, Curve 2, measured at full mute operation. The AF output is not "fast-switched" by the mute function, but there is a "progressive (soft muting) switch". This soft muting reduces the audio output signal at low field strength levels, without degradation of the audio output signal under these conditions.

The capacitor, C_1, at Pin 1 (see Figure 23) determines the time constant for the mute action.

Part operation of the mute is also a possibility (as shown by Figure 26, Curve 3) by circuiting a resistor in parallel with the mute capacitor at Pin 1.

In Figure 26 the small signal behavior with the mute disabled has been given also (see Curve 1).

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One can make use of the mute output signal, available at Pin 1, to indicate squelch situation by an LED (see Figure 27). Operation of the mute by means of an external DC voltage (see Figure 28) is also possible.

Bell Signal Operation

To avoid tone decoder filters and tone decoder rectifiers for bell signal transmission, use can be made of the mute information in the TDA7000 to obtain a bell signal without the transmission of a bell pilot signal.

With a handset receiver as shown in Figure 23 in the "standby" position, the high mute output level turns amplifier 1 off via transistor T1 until a correct IF frequency is obtained. This situation appears at the moment that a bell signal switches the base unit in transmission mode If the transmitted field strength is high enough to be received above a certain noise level, the mute level output goes down; T1 will be closed and amplifier 1 starts operating. However, due to feedback, this amplifier starts oscillating at a low frequency (a frequency dependent on the filter concept). This low-frequency signal serves for bell signal information at the loudspeaker.

Switching the handset to "talk" position will stop oscillation. Then amplifier 1 serves to amplify normal speech information.

Mute at Dialing

During dial operation, the key-pulser IC delivers a mute voltage. This voltage can be used to mute the AF amplifier, e.g., via T1 of the bell signal circuit/amplifier (see Figure 23)

CONCLUSIONS

The application of the TDA7000 in the remote unit (handset) as narrow-band FM receiver is very attractive, as the TDA7000 reduces assembly and post-production alignment costs. The only tunable circuit is the oscillator circuit, which can be a simple crystal-controlled tank circuit.

A TDA7000 with:

- fifth-order IF filter
- third-order AF output filter
- matched input circuit
- crystal oscillator tank circuit
- disabled mute circuit

gives a sensitivity of 2.5μV for 20dB signal-to-noise ratio, at adjacent channel selectivity of 40dB (at 15kHz) in cordless telephone application at 1.7MHz.

The TDA7000 circuit is:

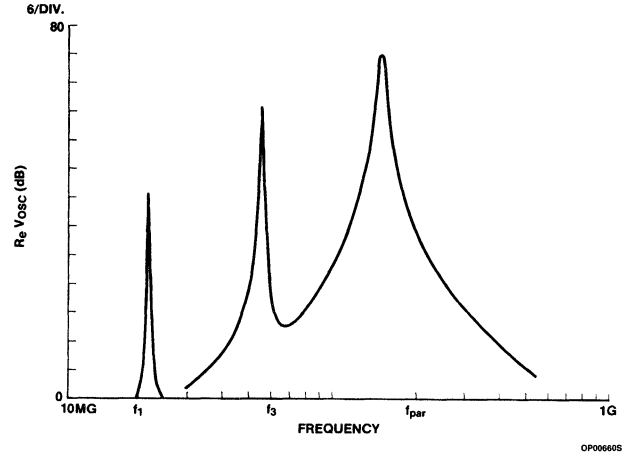
- without an RF pre-stage
- without RF-tuned circuits
- without oscillator transistor (and its components)
- without LC or ceramic filters in IF and demodulator

For improved performance, the TDA7000 circuit can be expanded:

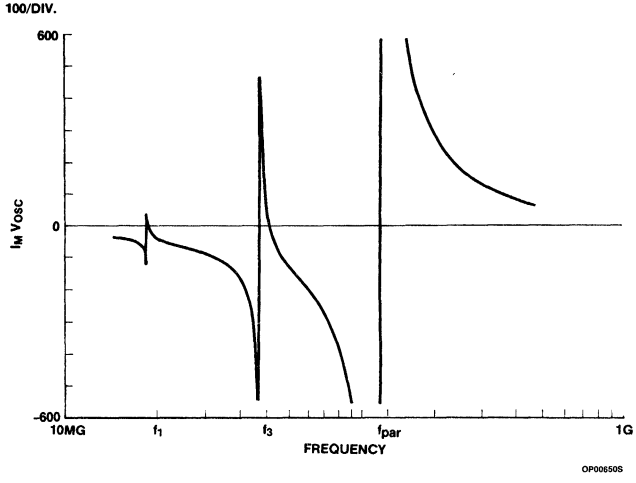
- with an RF pre-stage and RF selectivity
- with higher-order IF filtering
- with mute/squelch function.

For reduced performance the TDA7000 circuit can be simplified.

- to LC-tuned oscillator
- to lower-order IF filter
- to bell signal operation without pilot transmission

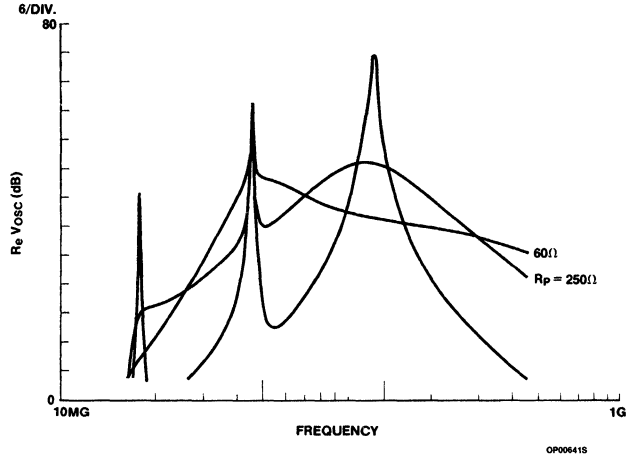


a. 1-Pin Crystal Oscillator

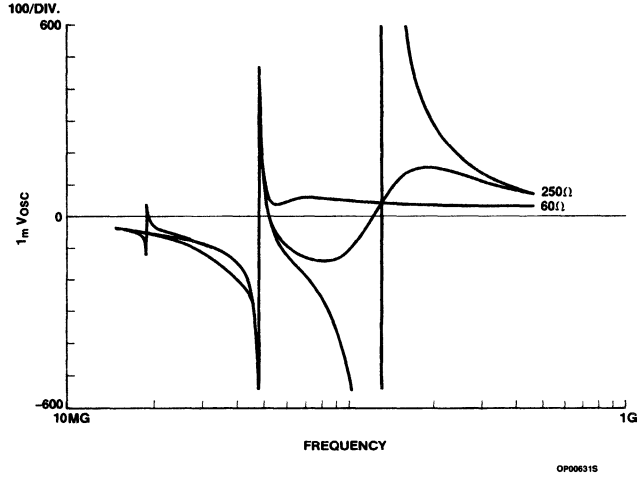


b. 1-Pin Crystal Oscillator

Figure 10



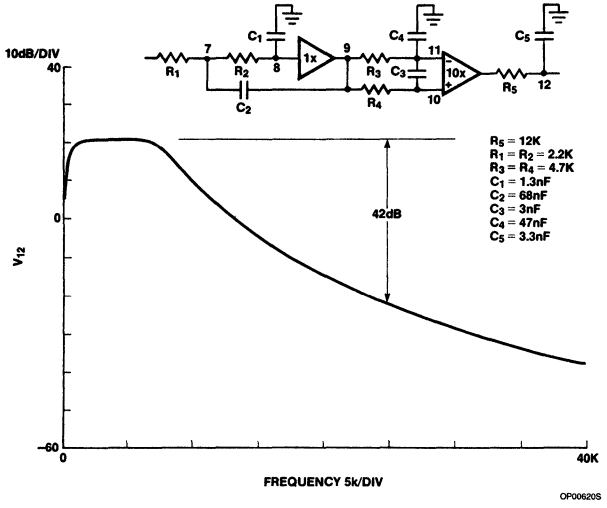
a. 1-Pin Crystal Oscillator
(R = ∞, 250, 60)



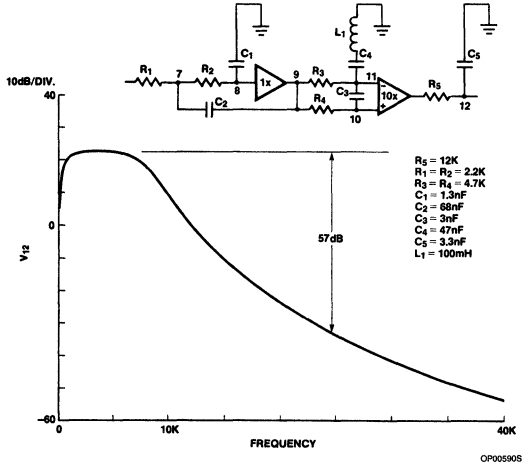
b. 1-Pin Crystal Oscillator
(R = ∞, 250, 60)

Figure 11

TDA7000 for Narrow-Band FM Reception AN193

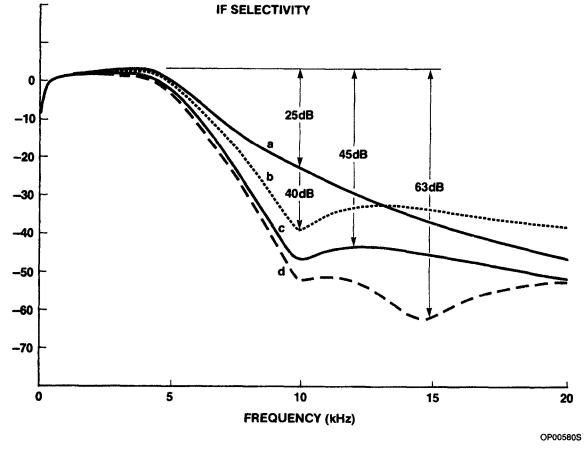


a.



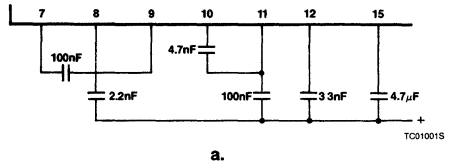
b.

Figure 12

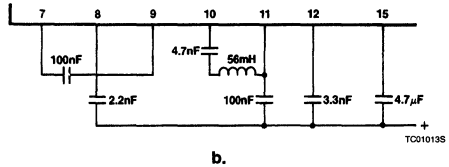


c.

Figure 12 (Continued)



a.



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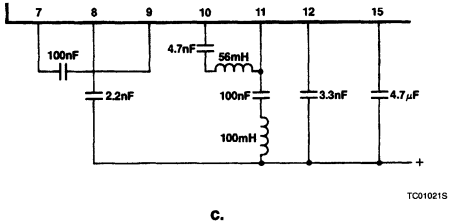
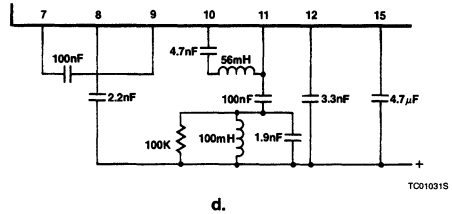


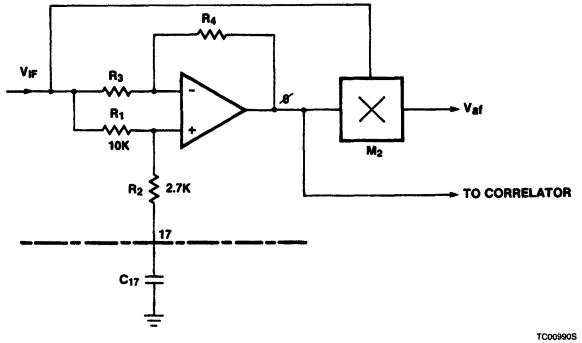
c.



d.

Figure 13

7



NOTES:
With $R_2 = 0$

$\phi = -2 \tan_1 wR_1C_{17}$

for $\phi = -90°C$, $C_{17} = \frac{1}{wR1\sqrt{\frac{R_4}{R_3}}} = 4\,1nF$ for $f_{IF} = 5kHz$

To improve the performance of the all-pass filter with the amplitude limted IF waveform, R_2 has been added. Since this influences the phase angle, the value of C_{17} must be increased by 13%, i.e., to 4.7nF

Figure 14. FM Demodulator Phase-Shift Circuit (All-Pass Filter)

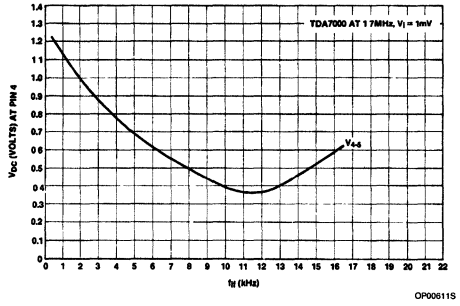


Figure 15

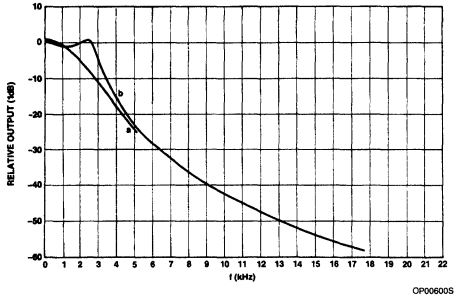
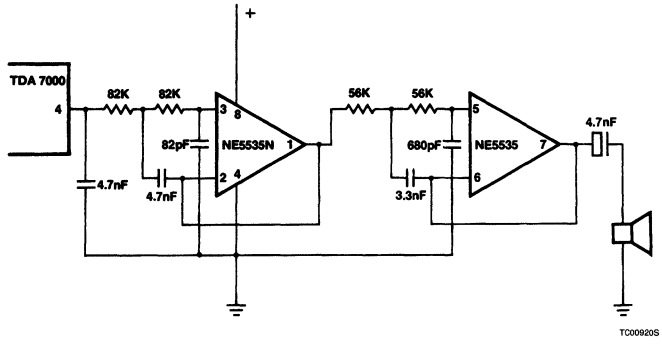


Figure 16



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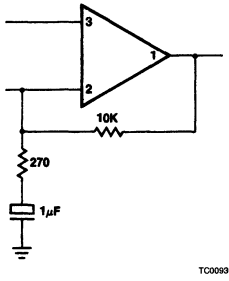


b.

Figure 17

TDA7000 for Narrow-Band FM Reception AN193

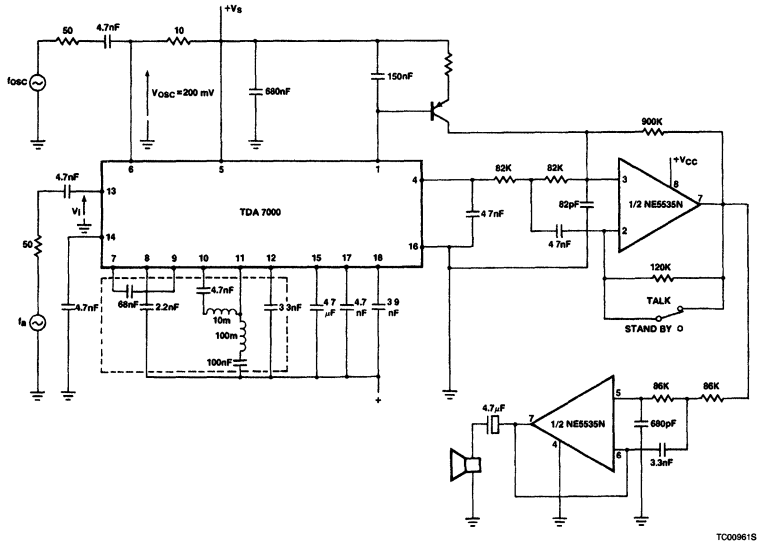


Figure 18

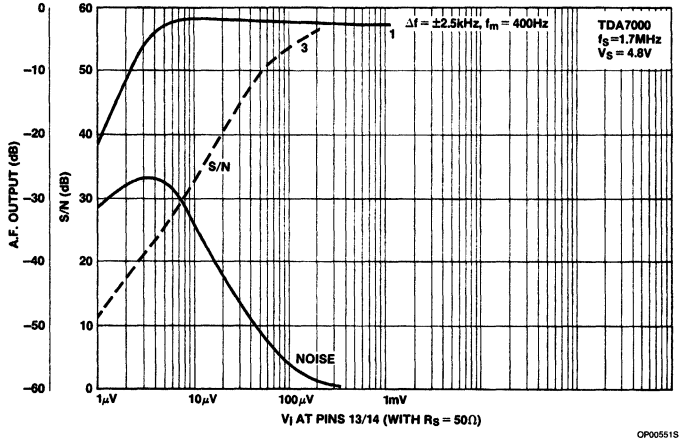


Figure 19

TDA7000 for Narrow-Band FM Reception AN193

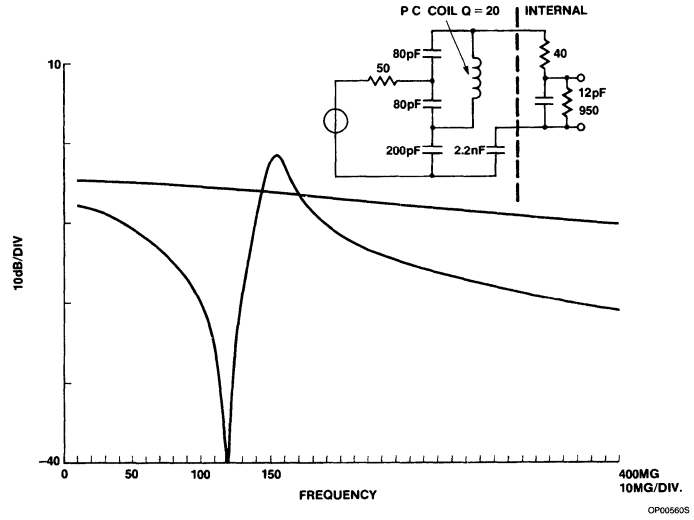


Figure 20

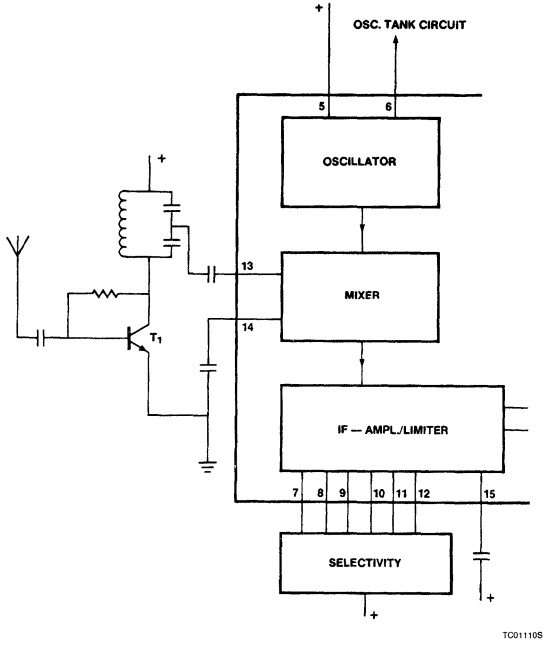


Figure 21

TDA7000 for Narrow-Band FM Reception AN193

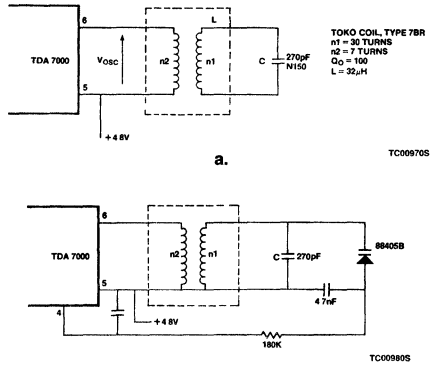


Figure 22

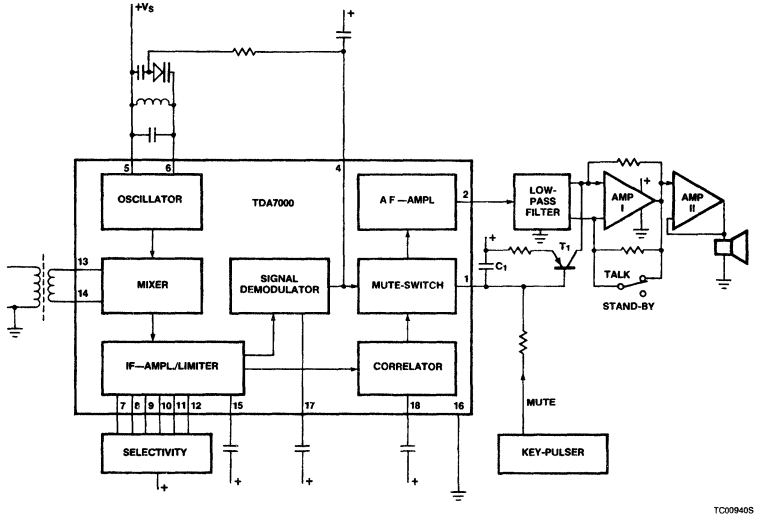


Figure 23. Remote Unit Receiver: 1.7MHz

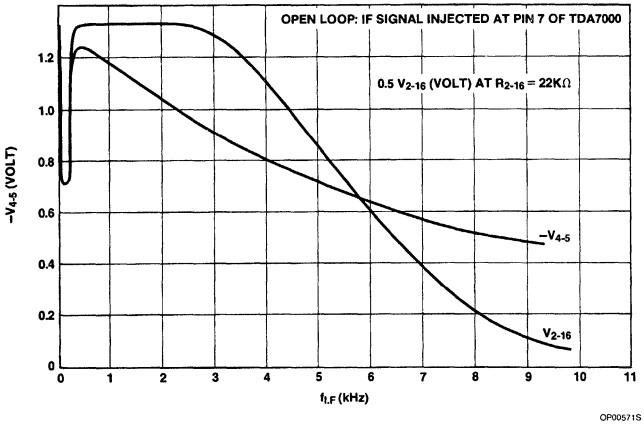


Figure 24. Demodulator Characteristics

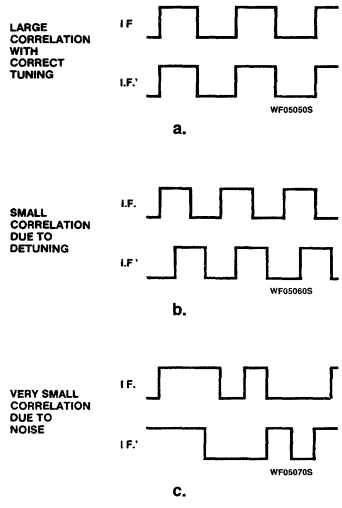


Figure 25. Function of the Correlation Muting System

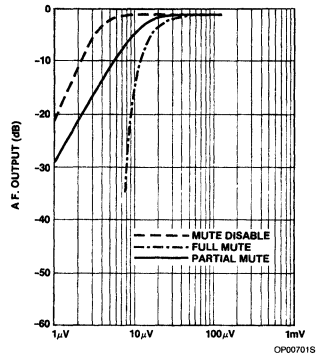


Figure 26

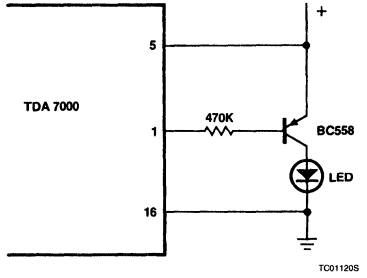


Figure 27

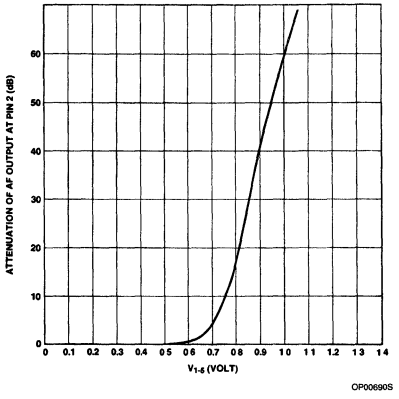


Figure 28

Previously published as "BAE83135," Eindhoven, The Netherlands, December 20, 1983.

TDA7010
FM Radio Circuit (SO Package)

Product Specification

Linear Products

DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked Loop) system with an intermediate frequency of 70kHz. The IF selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

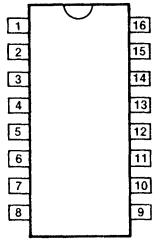
- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

APPLICATIONS

- **Mono FM Portable Radios**
- **LAN**
- **Data Receivers**
- **SCA Receivers**

PIN CONFIGURATION

D Package



TOP VIEW

CD10160S

PIN NO.	DESCRIPTION
1	Muting capacitor
2	Audio frequency output
3	Loop filter capacitor
4	Supply Voltage
5	VCO
6	1st integrator capacitor (to Pin 8)
7	2nd integrator capacitor
8	1st integrator capacitor (to Pin 6)
9	IF filter capacitor
10	IF limiter capacitor
11	RF input
12	Mixer
13	Current source capacitor
14	Ground
15	Demodulator capacitor
16	Correlator capacitor

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO DIP (SOT 109 A)	0 to +70°C	TDA7010TD

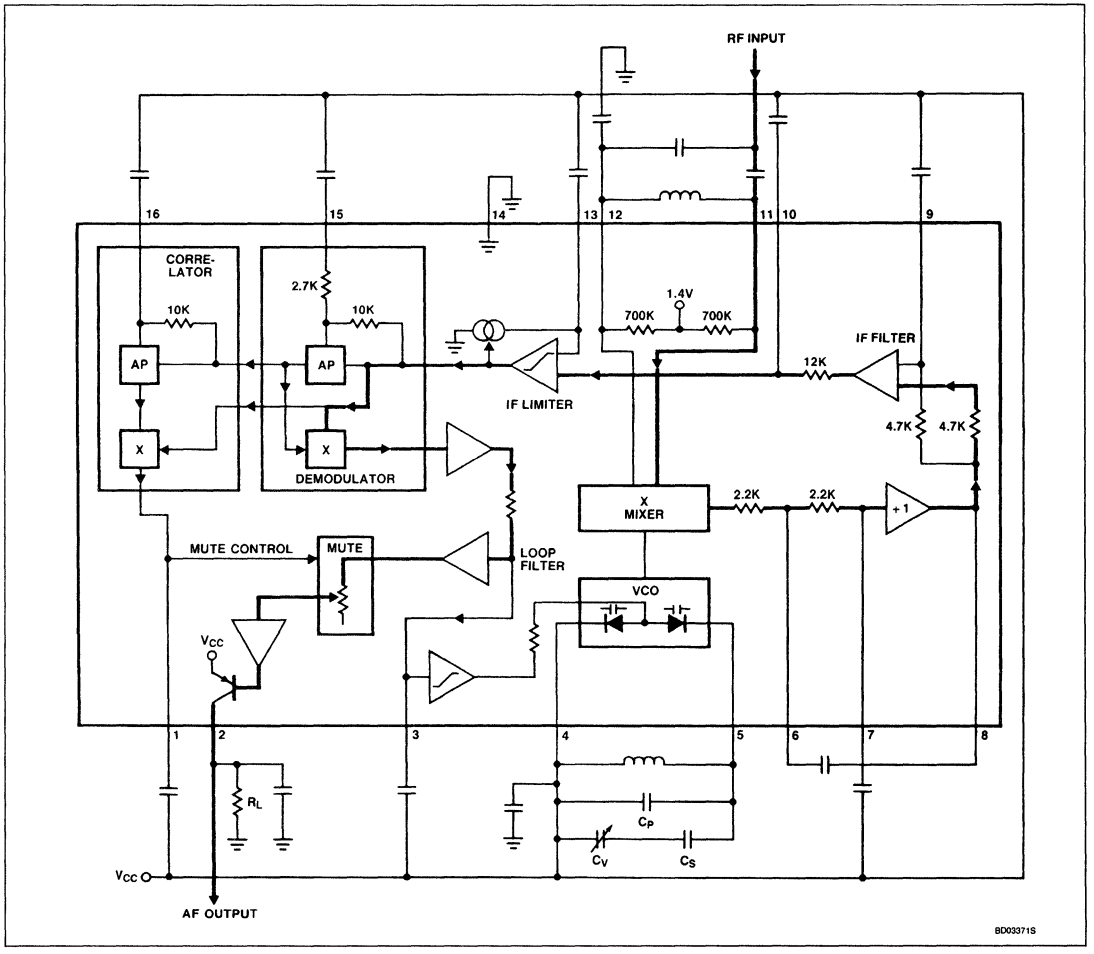
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 4)	12	V
V_{6-5}	Oscillator voltage (Pin 5)	V_{CC} – 0.5 to V_{CC} + 0.5	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	–55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

7

FM Radio Circuit (SO Package) TDA7010

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.5V; T_A = 25°C: measured in Figure 3, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 4)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_5	Oscillator current	(Pin 5)		280		μA
V_{12-14}	Voltage	(Pin 12)		1.35		V
I_2	Output current	(Pin 2)		60		μA
V_{2-14}	Output voltage	(Pin 2) R_L = 22kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS V_{CC} = 4.5V; T_A = 25°C; measured in Figure 3 (mute switch open, enabled); f_{RF} = 96MHz (tuned to max. signal at 5μV EMF) modulated with Δf = ±22.5kHz; f_M = 1kHz; EMF = 0.2mV (EMF voltage at a source impedance of 75Ω); RMS noise voltage measured unweighted (f = 300Hz to 20kHz), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (EMF voltage)	-3dB limiting; muting disabled		1.5		μV
		-3dB muting		6		
		S/N = 26dB		5.5		
EMF	Signal handling (EMF voltage)	THD < 10%; Δf = ± 75kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ± 22.5kHz Δf = ± 75kHz		0.7 2.3		% %
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_M = 1kHz; Δf = ± 75kHz AM signal: f_M = 1kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100mV; f = 1kHz)		10		dB
V_{5-4RMS}	Oscillator voltage (RMS value)	(Pin 5)		250		mV
Δf_{OSC}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		60		kHz/V
S_{+300}	Selectivity			43		dB
S_{-300}				28		
Δf_{RF}	AFC range			± 300		kHz
B	Audio bandwidth	ΔV_O = 3dB Measured with pre-emphasis (t = 50μs)		10		kHz
$V_{O\ RMS}$	AF output voltage (RMS value)	R_L = 2kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

7

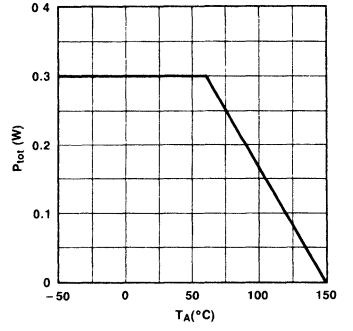
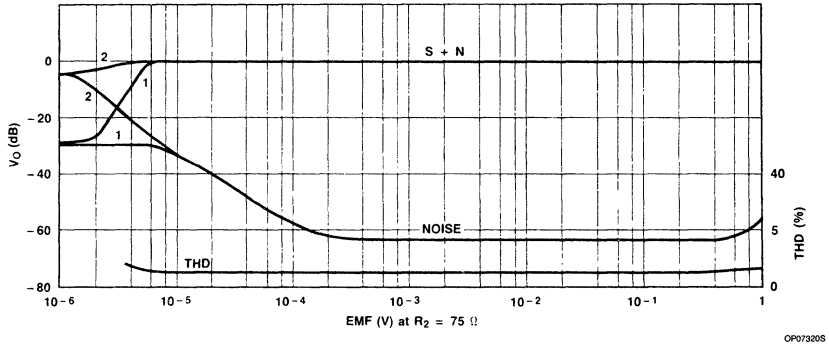


Figure 1. Power Derating Curve



NOTE:
1. The muting system can be disabled by feeding a current of about 20μA into Pin 1.

Conditions: 0 dB = 75mV; f_{RF} = 96MHz
for S + N curve: Δf = ± 22.5kHz: f_M = 1kHz
for THD curve: Δf = ± 75kHz: f_M = 1kHz

Figure 2. AF Output Voltage (V_O) and Total Harmonic Distortion (THD) as a Function of the EMF Input Voltage (EMF) With a Source Impedance (R_S) of 75Ω: (1) Muting System Enabled; (2) Muting nystem Disabled

FM Radio Circuit (SO Package) TDA7010

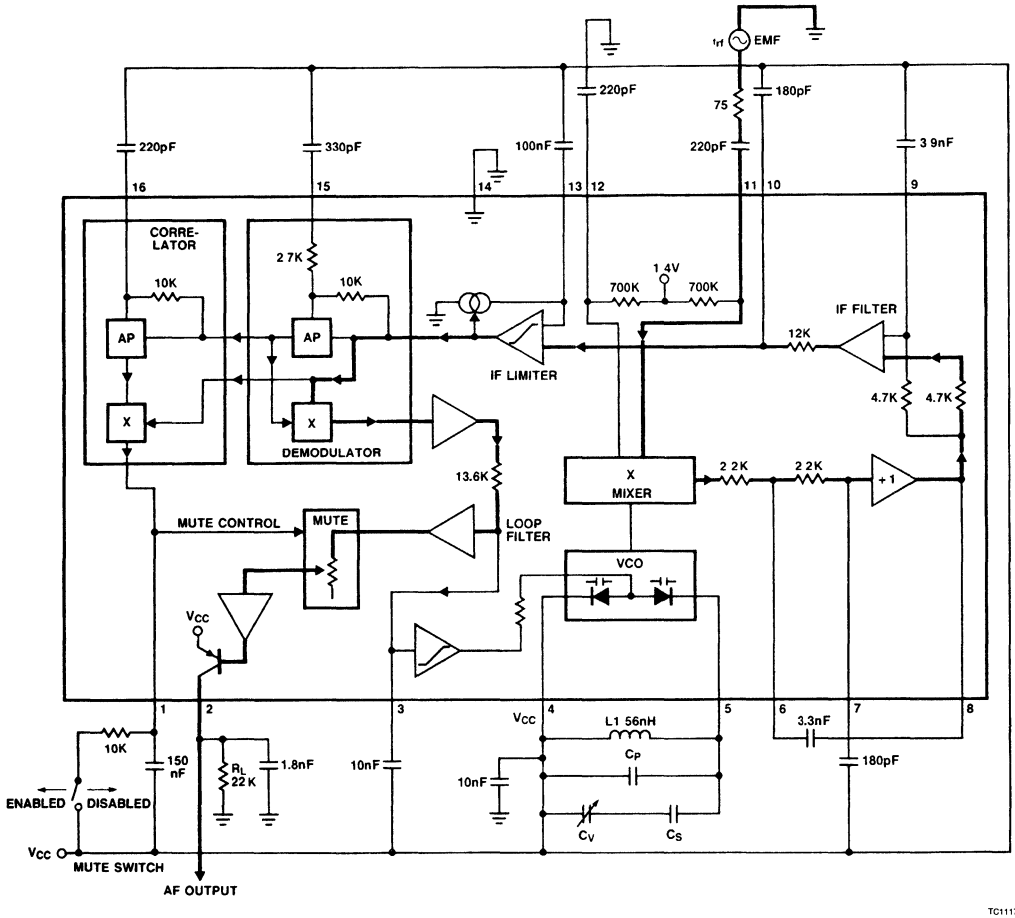


Figure 3. Test Circuit

7

Signetics

TDA7021
Single-Chip FM Radio Circuit

Preliminary Specification

Linear Products

DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system IC (MTS). The IC has a frequency-locked loop (FLL) system with an intermediate frequency of 76kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field strength detector enables field strength-dependent channel separation control.

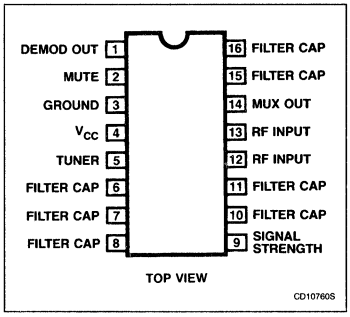
FEATURES

- **RF input stage**
- **Mixer**
- **Local oscillator**
- **IF amplifier/limiter**
- **Frequency detector**
- **Mute circuit**
- **MTS compatible**
- **Loop amplifier**
- **Internal reference circuit**
- **LF amplifier for**
  - **mono earphone amplifier or**
  - **MUX filter**
- **Field strength-dependent channel separation control facility**

APPLICATIONS

- **FM radios**
- **Stereo**
- **Mono**

PIN CONFIGURATION



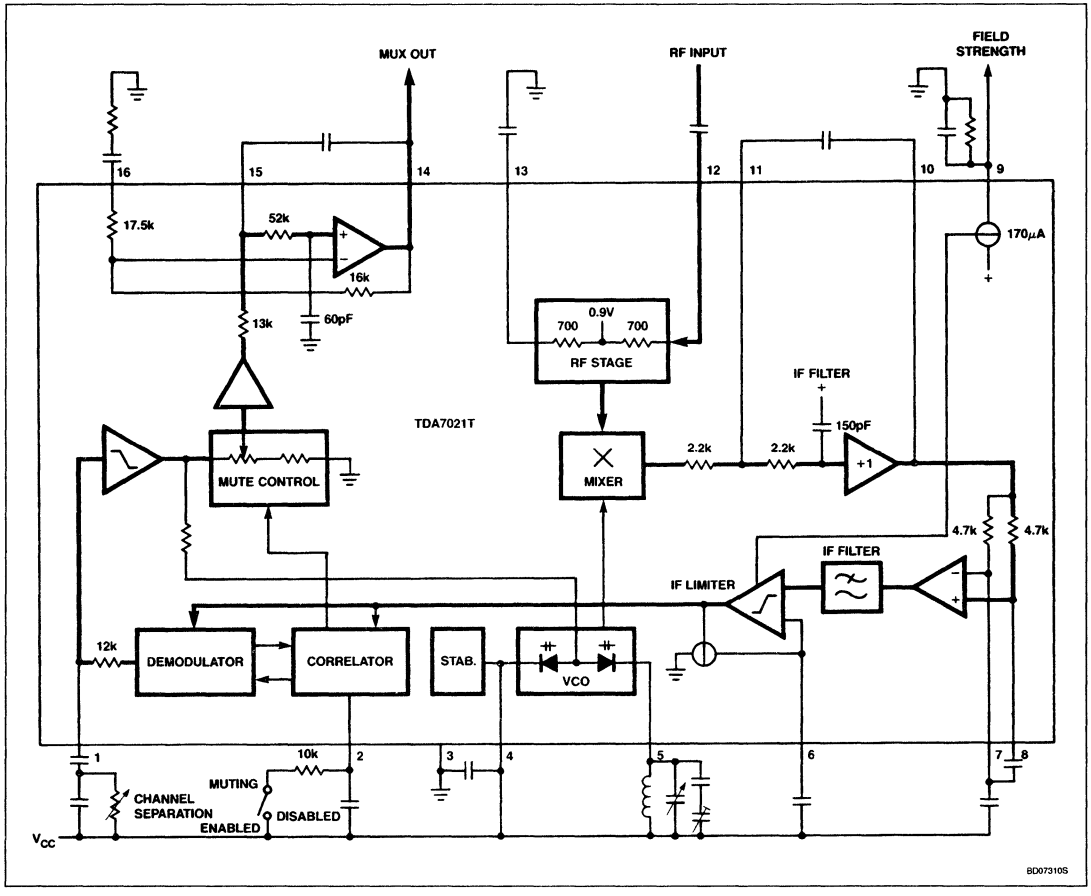
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	TDA7021TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 4)	7	V
V_{6-5}	Oscillator voltage (Pin 5)	V_{CC} - 0.5 to V_{CC} + 0.5	V
T_{stg}	Storage temperature range	-55 to +150	°C
T_A	Operating ambient temperature range	-10 to +70	°C
θ_{JA}	Thermal resistance From junction to ambient	300	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{CC} = 3V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage (Pin 4)	1.8	3.0	6	V
I_{CC}	Supply current at V_{CC} = 3V		6 3		mA
I_5	Oscillator current (Pin 5)		250		µA
V_{13-3}	Voltage at Pin 13		0.9		V
V_{14-3}	Output voltage (Pin 14)		1.3		V

7

AC ELECTRICAL CHARACTERISTICS (MONO OPERATION)

V_{CC} = 3V, T_A = 25°C; measured in Figure 5; f_{RF} = 96MHz modulated with $\Delta f = \pm 22.5$kHz; f_M = 1kHz; EMF = 300μV (EMF voltage at a source impedance of 75Ω); RMS noise voltage measured unweighted (f = 300Hz to 20kHz), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (EMF voltage) for −3dB limiting; muting disabled for −3dB muting for S/N = 26dB		 4.0 5.0 7		 μV μV μV
EMF	Signal handling (EMF voltage) for THD < 10%; $\Delta f = \pm 75$kHz		200 60		mV
S/N	Signal-to-noise ratio		60		dB
THD	Total harmonic distortion at $\Delta f = \pm 22.5$kHz at $\Delta f = \pm 75$kHz		 0.7 2.3		 % %
AMS	AM suppression of output voltage (ratio of AM signal: f_M = 1kHz; m = 80% to FM signal: f_M = 1kHz; at $\Delta f = \pm 75$kHz)		50		dB
RR	Ripple rejection (ΔV_{CC} = 100mV; f = 1kHz)		30		dB
$V_{5-3(RMS)}$	Oscillator voltage (Pin 5) RMS value Variation of oscillator frequency		250		mV
$\Delta f_{OSC}/\Delta C_P$ $\Delta f_{OSC}/\Delta T$	with supply voltage (ΔV_{CC} = 1V) with temperature		5 0.2		kHz/V kHz/°C
S_{+300} S_{-300}	Selectivity (without modulation; Test Circuit, Figure 7)		30 46		dB dB
$\pm \Delta f_{RF}$	AFC range		160		kHz
$\pm \Delta f_{RF}$	Mute range		120		kHz
BW	Audio bandwidth at ΔV_O = 3dB measured with pre-emphasis (t = 50μs)		10		kHz
$V_{O(RMS)}$	AF output voltage (RMS value) at R_L (Pin 14) = 100Ω; Pin 16 open		90		mV
$I_{O(DC)}$ $I_{O(AC)}$	AF output current MAX. DC load MAX. AC load for THD = 10%; peak value	−100	 3	+100	 μA mA

AC ELECTRICAL CHARACTERISTICS (STEREO OPERATION)

V_{CC} = 3V, T_A = 25°C; measured in Figure 6, f_{RF} = 96MHz modulated with pilot $\Delta f = \pm 6.75$kHz and AF signal $\Delta f = \pm 22.5$kHz; f_M = 1kHz; EMF = 1mV (EMF voltage at a source impedance of 75Ω); RMS noise voltage measured unweighted (f = 300Hz to 20kHz), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
EMF	Sensitivity (Figure 2) (EMF voltage) for S/N = 46dB		300		μV
S/N	Signal-to-noise ratio		53		dB
α	Channel separation		20		dB
V_{PILOT}	Pilot voltage level at Pin 14		13 5		mV
$V_{AF(RMS)}$	AF level at output		80		mV
S_{+300} S_{-300}	Selectivity without modulation (test circuit Figure 6)		22 40		dB dB

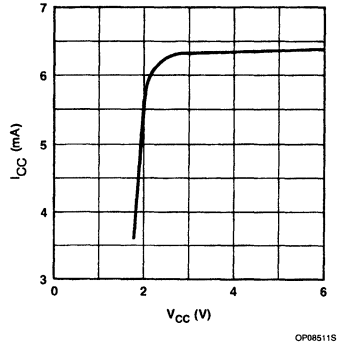


Figure 1. Supply Current as a Function of the Supply Voltage

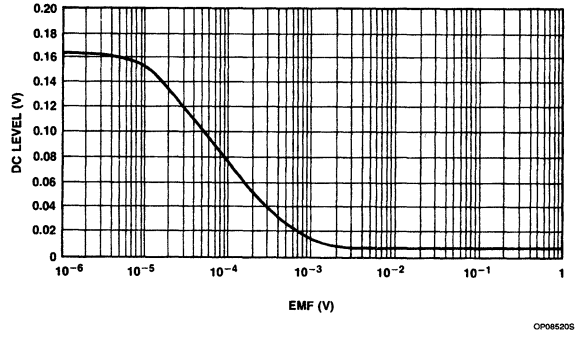
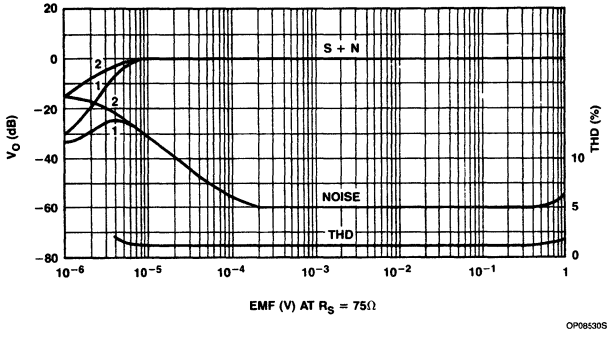
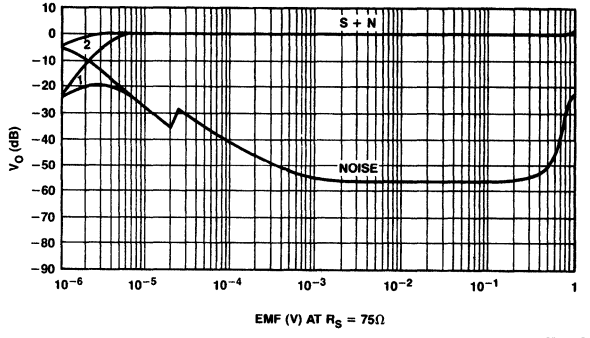


Figure 2. Field Strength Voltage (V_{9-3}) at $R_S = 1k\Omega$; f = 96.75MHz and Supply Voltage is 3V



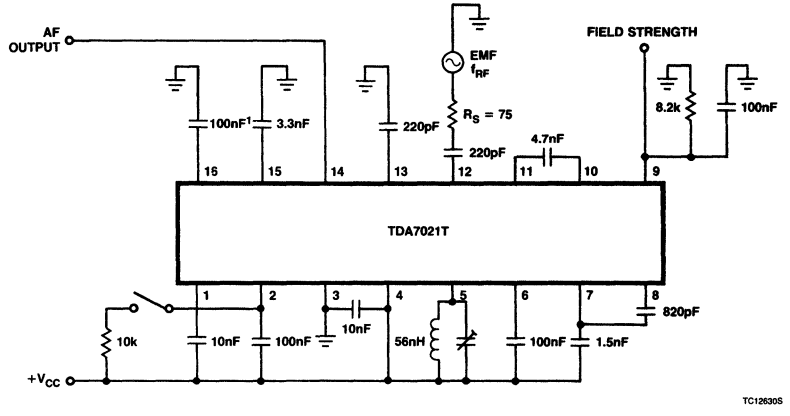
NOTES:
Conditions: 0 dB – 100mV, f_{RF} = 96MHz,
for S + N curve $\Delta f = \pm 22.5$kHz, f_M = 1kHz
for THD curve $\Delta f = \pm 75$kHz, f_M = 1kHz
AF output voltage (V_O) and total harmonic distortion (THD) as a function of the EMF input voltage (EMF) with a source impedance (R_S) of 75Ω (1) Muting system enabled, (2) Muting system disabled

Figure 3. MONO Operation



NOTE:
AF output Voltage (V_O) as a function of the EMF input voltage (EMF) (1) Muting system enabled; (2) muting system disabled

Figure 4. STEREO Operation



NOTE:
1 The AF output can be decreased by 5dB by disconnection of the 100nF capacitor of Pin 16

Figure 5. Test Circuit for MONO Operation

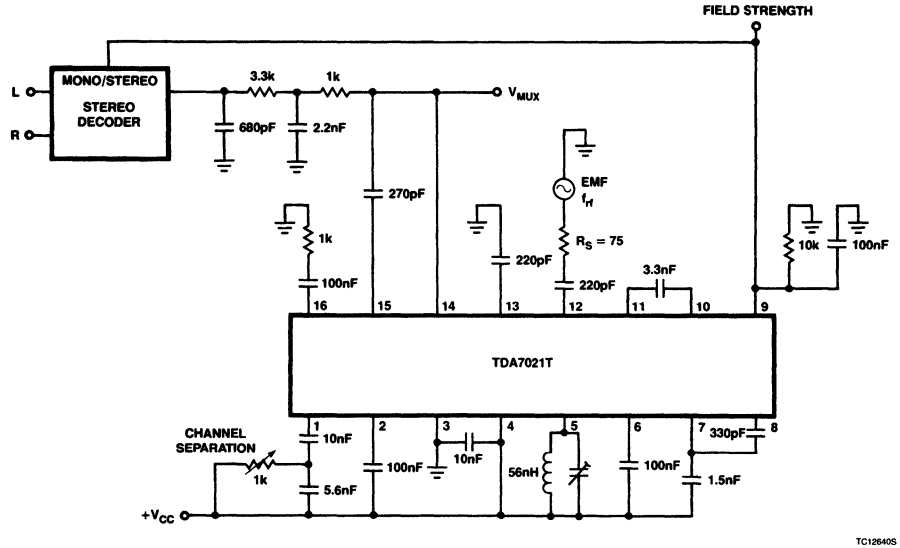
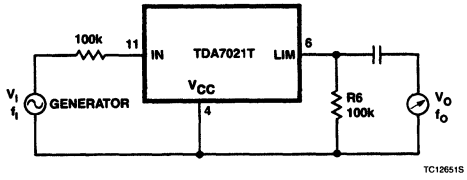


Figure 6. Test Circuit for STEREO Operation



NOTES:
Setup with circuitry as Figure 5 or Figure 6
C_6 (100nF) deleted and replaced by R6 = 100kΩ, V_i = 30mV; f_i = 76kHz.
Output: selective voltmeter; $R_I \geq 1M\Omega$; $C_I \leq 8pF$; $f_O = f_i$

$$S_{+300} = 20_{Log}\frac{V_O\,|\,(300kHz - f_i)}{V_O\,|\,f_i} \qquad S_{-300} = 20_{Log}\frac{V_O\,|\,(300kHz + f_i)}{V_O\,|\,f_i}$$

Figure 7. Test Circuit

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Signetics

TEA5560
FM/IF System

Product Specification

Linear Products

DESCRIPTION

The TEA5560 is a monolithic integrated FM/IF system circuit, intended for car radios and home receivers equipped with a ratio detector.

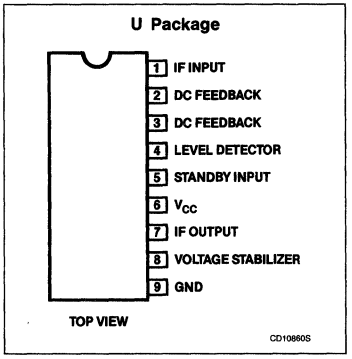
FEATURES

- **A three-stage IF limiting amplifier**
- **A 15dB field strength-dependent muting circuit**
- **A field strength-dependent DC voltage, for:**
  - **mono/stereo switching**
  - **channel separation control of a stereo decoder**
  - **an indicator ($I_{MAX} \leqslant 1mA$)**
- **Standby ON/OFF switching circuit**
- **A voltage stabilizer for the internal circuit current and an external current up to 15mA**
- **Adjustable gain ($\Delta G = 15dB$)**

APPLICATIONS

- **Home receivers**
- **Car radios**

PIN CONFIGURATION



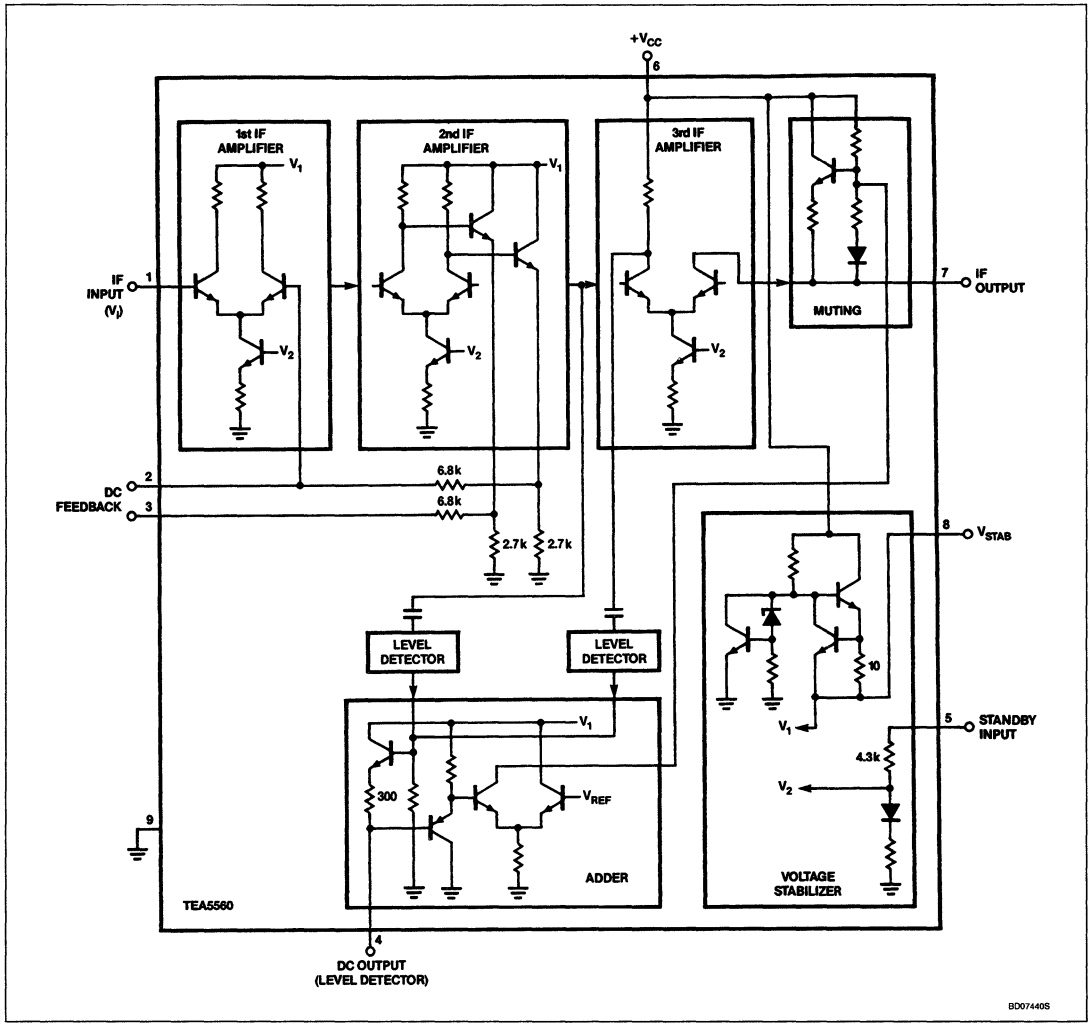
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-142)	−30°C to +85°C	TEA5560U

ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNITS
	Supply voltages		
$V_{CC} = V_{6-9}$	Pin 6	24	V
V_{7-9}	Pin 7	24	V
V_{4-9}	Voltage at Pin 4	6	V
V_{5-9}	Voltage at Pin 5	9	V
$-I_{8SM}$	Non-repetitive peak output current (Pin 8)	100	mA
P_{TOT}	Total power dissipation	1000	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +85	°C
θ_{JA}	Thermal resistance from junction to ambient (in free-air)	75	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{CC} = 14.4V; T_A = 25°C; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 6)					
$V_{CC} = V_{6-9}$	Supply voltage[1]	10.2	14.4	18.0	V
Voltages					
V_{8-9}	at Pin 8; $-I_8 = 0$[2]	7.5	8.0	8.5	V
	at Pin 8 when $-I_8$ increases from 0 to 15mA		200	300	mV
ΔV_{8-9}	at Pin 8 when V_{CC} reduces from 14.4V to 10.2V			1.0	V
ΔV_{8-9}	at Pin 8 when V_{CC} increases from 14.4V to 18.0V			200	mV
V_{4-9}	at Pin 4 (level detector)			100	mV
$V_{1,\ 2,\ 3-9}$	at Pins 1, 2 and 3		2.4		V
Currents					
I_{TOT}	Total supply current; $-I_8 = 0$	15	20	30	mA
$-I_8$	Current supplied from Pin 8			15	mA
I_{SB}	Stand-by current; $V_{5-9} = 0$	8	11	14	mA
I_5	Current into Pin 5	1.0	1.5	2.0	mA
I_7	Current into Pin 7		3.0		mA
Power consumption					
P_C	$-I_8 = 0$		300		mW

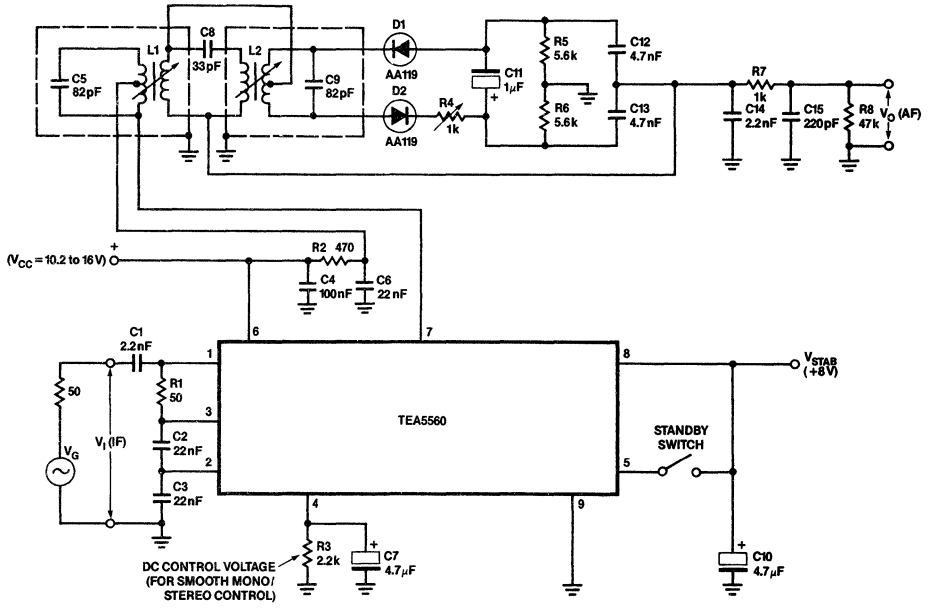
NOTES:
1. A stabilized supply voltage of 7 to 9V can also be applied at Pins 5 and 6 (linked); for this application Pin 8 must not be connected.
2. The temperature coefficient of the stabilized voltage at Pin 8 is typically – 2.3mV/°C.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 14.4V; T_A = 25°C; V_I = 1mV; f_O = 10.7MHz; $\Delta f = \pm 22.5$kHz; f_M = 1kHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
IF part and ratio detector					
	Sensitivity at – 3dB before limiting (Pin 1); (without muting)[1]	105	150	210	μV
	Signal-to-noise S+N/S measured in a bandwidth of 60Hz to 15kHz				
S/N	at V_I = 20μV	40	45		dB
S/N	at V_I = 150μV		65		dB
S/N	at V_I = 1mV		78		dB
S/N	at V_I = 10mV		80		dB
	AF output voltage				
V_O	$\Delta f = \pm 22.5$kHz		200		mV
V_O	$\Delta f = \pm 75$kHz		600		mV
	Total harmonic distortion				
THD	$\Delta f = \pm 22.5$kHz		0.3		%
THD	$\Delta f = \pm 75$kHz		2.0		%
	AM suppression f_M = 1kHz; m = 0.3 (for AM) f_M = 70kHz; $\Delta f = \pm 22.5$kHz (for FM)				
AMS	at V_I = 150μV		40		dB
AMS	at V_I = 1mV		50		dB
AMS	at V_I = 10mV		55		dB
Level detector circuit					
	DC output voltage (Pin 4)				
V_{4-9}	at V_I = 200μV		1.9		V
V_{4-9}	at V_I = 500μV		2.8		V
V_{4-9}	at V_I = 1mV		3.5		V
V_{4-9}	at V_I = 3mV		5.0		V
V_{4-9}	at V_I = 10mV		5.7		V
Muting circuit (see also Figure 4)					
α_{VO}	Change in output voltage at V_I = 3μV (with and without muting)[1]	10	15		dB
V_{IN}	Input voltage at a change in output voltage of $\leqslant$ 1 dB[1] (V_I at $\alpha_{VO} \leqslant$ 1 dB)			250	μV

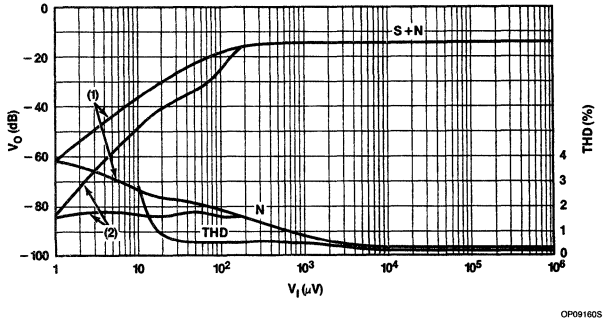
NOTE:
1 With muting $V_{4-9} < 0.3$V, without muting V_{4-9} = 1.2 to 6V

7



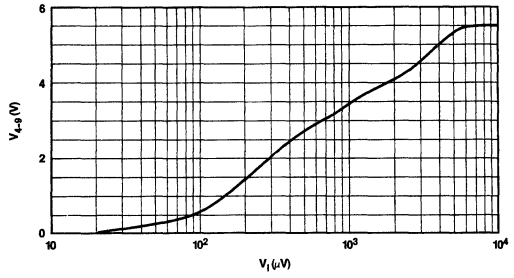
NOTES:
Catalog number of detector coils
L1 3122 138 20211
(TOKO 85ACS-4238A)
L2 3122 138 20212
(TOKO 85ACS-4260SEJ)

Figure 1. FM Test Circuit



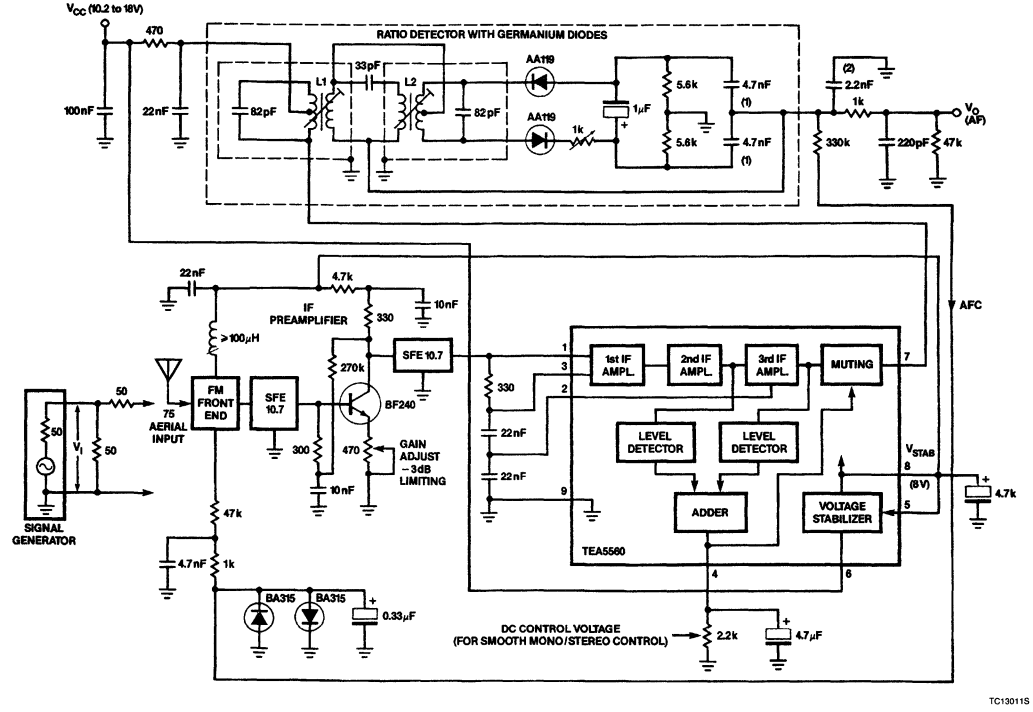
NOTES:
1. Without muting
2. With muting
3. Reference level 0dB = 1V, and the total harmonic distortion (THD) as a function of the IF input voltage (V_I) Measured in the Test Circuit Figure 1 at $\Delta f = \pm 22.5$kHz, $f_m = 1$kHz

Figure 2. AF Output Voltage (V_O)



NOTE:
Measured in Test Circuit Figure 1

Figure 3. Level Detector DC Output Voltage (Pin 4) as a Function of the IF Input Voltage



Catalog number of detector coils
L1 3122 138 20211 (TOKO 85ACS-4238A)
L2 3122 138 20212 (TOKO 85ACS-4260SEJ)
F M Front-end ALPS MMK11E11

NOTES:
1 Stereo application 220pF
2 Stereo application 390pF

Figure 4. FM Channel for (Car) Radios Using the TEA5560 and a Ratio Detector With AA119 Germanium Diodes

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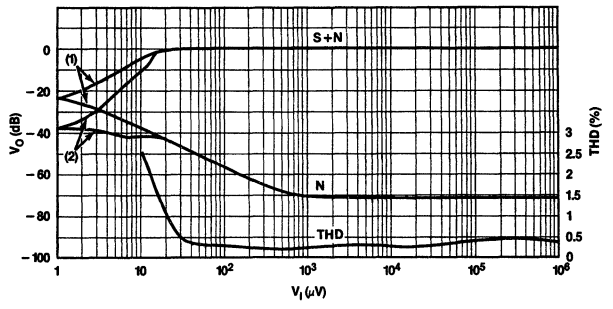
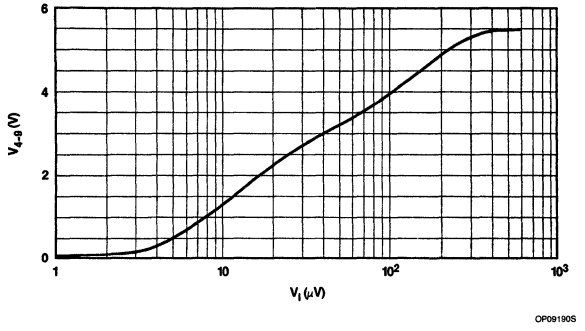


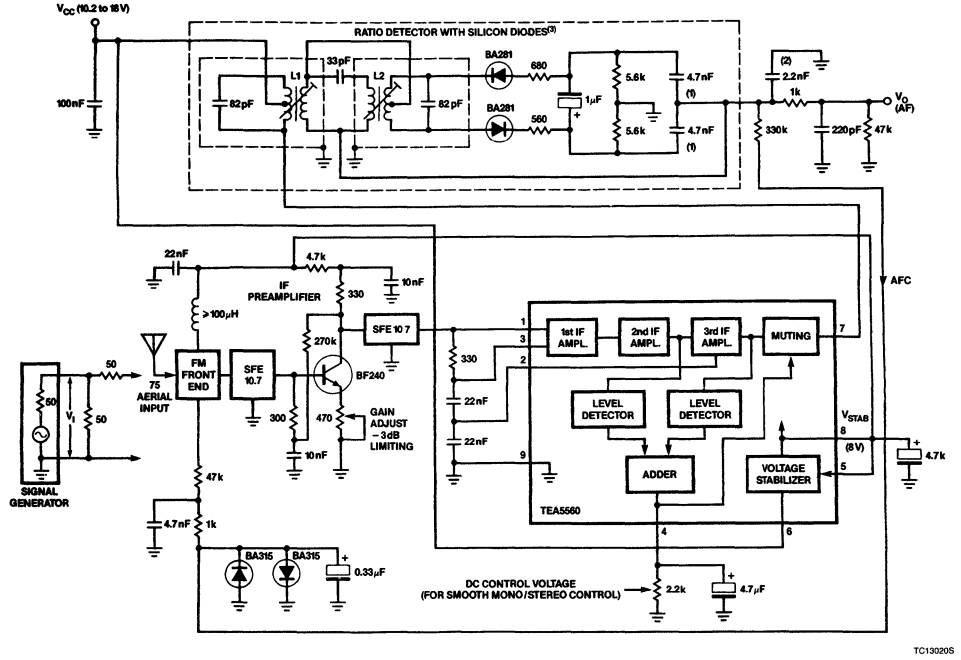
NOTES:
1. Without muting
2. With muting.
3. Reference level 0dB = 200mV, and the total harmonic distortion (THD) as a function of the aerial input voltage (V_I). Measured in Application Circuit Figure 6 at $\Delta f = \pm 22.5$kHz, $f_M = 1$kHz

Figure 5. Signal and Noise (S + N) and Noise (N)



NOTE:
Measured in Application Circuit Figure 4

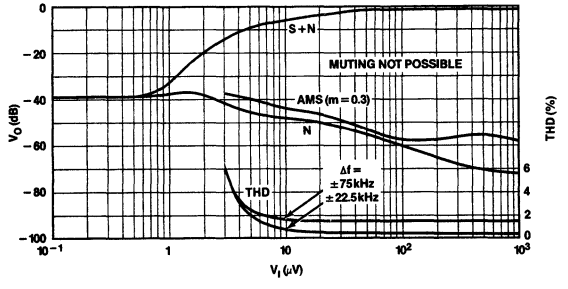
Figure 6. Level Detector DC Output Voltage (Pin 4) as a Function of the Aerial Input Voltage



Catalog number of detector coils
L1 3122 138 20211 (TOKO 85ACS-4238A)
L2. 3122 138 20212 (TOKO 85ACS-4260SEJ)
F M. Front-end· ALPS MMK11E11

NOTES:
1 Stereo application 220pF.
2. Stereo application 390pF
3 Further detailed information on the use of silicon diodes is available on request

Figure 7. FM Channel for (Car) Radios Using the TEA5560 and a Ratio Detector With BA281 Silicon Diodes



NOTE:
Reference level 0dB = 245mV, AM Suppression (AMS) and Total Harmonic Distortion (THD) as a function of the aerial input voltage (V_I). Measured in Application Circuit Figure 7
at $\Delta f = \pm 22.5$kHz, f_M = 1kHz, for AM suppression m = 0 3, $\Delta f = \pm 22$ 5kHz

Figure 8. Signal and Noise (S + N) and Noise (N)

Signetics

TDA1578A
PLL Stereo Decoder

Product Specification

Linear Products

DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

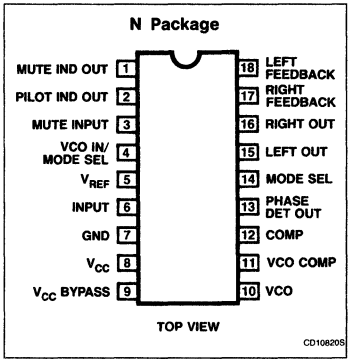
FEATURES

- **Adjustable input and output voltage levels**
- **Automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level**
- **Analog control of mono/stereo changeover**
- **Pilot indicator driver**
- **Analog muting control**
- **Muting indicator driver**
- **Oscillator with decoupled frequency measurement output**
- **Electronic smoothing of the supply voltage**

APPLICATION

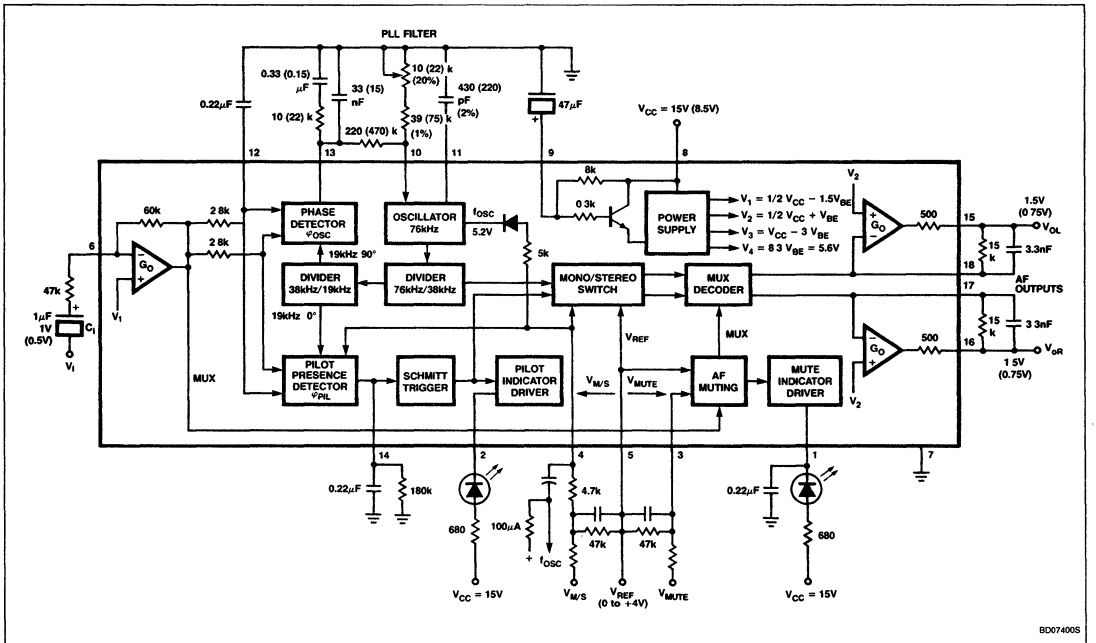
- **PLL decoder**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	0 to +70°C	TDA1578AN



NOTE:
Values given in parentheses are for V_{CC} = 8.5V

Block Diagram With External Components; Used as Test Circuit

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage (Pin 8)	20	V
V_{IN}	Input voltages (Pins 3, 4 and 5)	0 to 12	V
V_{OUT}	Indicator driver output voltage	24	V
I_{OUT}	Indicator driver output current	30	mA
P_D	Total power dissipation at $T_A = 25°C$	1 2	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C
θ_{CA}	Thermal resistance from crystal to ambient	80	°C/W

DC ELECTRICAL CHARACTERISTICS

Input signal m = 100% ($\Delta f = \pm 75$kHz), pilot signal m = 9% ($\Delta f = \pm 6$ 75kHz), Modulation frequency 1kHz, $V_{3-5} = V_{4-5} = 0V$, De-emphasizing time t = 50μs, oscillator adjusted to f_{OSC} at a pilot voltage $V_I = 0V$, $T_A = 25°C$, unless otherwise specified

SYMBOL	PARAMETER	V_{CC} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range (Pin 8)		7 5	8.5	18	V
I_{CC}	Supply current (except	8.5		21		mA
I_{CC}	output and indicator) Pin 8	15		30	40	mA
	Nominal multiplex input					
$V_{MUX(P-P)}$	voltage (peak-to-peak value)	8 5		0 5		V
$V_{MUX(P-P)}$	$R_I = 47k\Omega$	15		1.0		V
	Overdrive reserve of input					
	at THD = 1%	8.5	3	6		dB
	at THD = 0 3%	15	3	6		dB
	AF output voltage (RMS value; mono without pilot)					
$V_{O(RMS)}$	$R_{15-18} = R_{16-17} = 15k\Omega$	8 5		0 75		V
$V_{O(RMS)}$		15		1 5		V
$V_{O(RMS)}$	$R_{15-18} = R_{16-17} = 24k\Omega$	8.5		1.2		V
$V_{O(RMS)}$		15		2 4		V
	Overdrive reserve of output[1]					
	$R_{15-18} = R_{16-17} = 24k\Omega$		3			dB
$\pm \Delta V_O/V_O$	Spread in output voltage levels[1]				1	dB
$\pm \Delta V_{15-16}/V_O$	Difference of output voltage levels[1]				1	dB
R_O	Output resistance[1]			low-ohmic		
$\pm I_O$	Available output current Pins 15 and 16[1]					mA
$V_{15,16-7}$	Modulation range at output (unloaded)[1]			1 to $V_{9-7}-1$		V
I_O	Internal current limiting[1]			15		mA
$V_{15,16-7}$	DC output voltage	8 5	3 6	4 1	4 6	V
$V_{15,16-7}$	$R_{15-18} = R_{16-17} = 24k\Omega$	15	7.0	7.7	8.4	V
$-I_{17,18}$	DC current	8 5		33		μA
$-I_{17,18}$	(Pins 17 and 18)	15		23		μA
α	Channel separation	8.5	32	50		dB
α	at $V_{4-5} = 0V$	15	39	50		dB
THD	Total harmonic distortion	8.5		0.1	0 3	%
THD		15		0 04	0 1	%
S/N	Signal-to-noise ratio	8.5		87		dB
S/N	f = 20Hz to 16kHz	15		90		dB

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DC ELECTRICAL CHARACTERISTICS (Continued) Input signal: m = 100% ($\Delta f = \pm 75$kHz); pilot signal: m = 9% ($\Delta f = \pm 6.75$kHz); Modulation frequency: 1kHz; $V_{3-5} = V_{4-5} = 0$V; De-emphasizing time: t = 50μs; oscillator adjusted to f_{OSC} at a pilot voltage $V_I = 0$V; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	V_{CC} (V)	LIMITS			UNIT
			Min	Typ	Max	
	Carrier and harmonic suppression at the output					
α_{19}	pilot signal; f = 19kHz[1]			32		dB
α_{38}	subcarrier; f = 38kHz[1]		40	50		dB
α_{57}	f = 57kHz[1]			46		dB
α_{76}	f = 76kHz[1]			60		dB
	intermodulation[1]					
	f_M = 10kHz;					
	spurious signal f_S = 1kHz					
α_2	PLL-filter Figure 1[1]			50		dB
α_2	PLL-filter Figure 2[1]			70		dB
	f_M = 13kHz;					
α_3	spurious signal f_S = 1kHz[1]			75		dB
	traffic radio (VWF)[2];					
$\alpha_{57(VWF)}$	f = 57kHz[1]			70		dB
	SCA (Subsidiary Communications Authorization);					
α_{67}	f = 67kHz[4,1]			70		dB
	ACI (Adjacent Channel Interference)[3]					
α_{114}	f = 114kHz[1]			80		dB
α_{190}	f = 190kHz[1]			52		dB
	Ripple rejection at the output; f = 100Hz;					
RR_{100}	$V_{CC(RMS)}$ = 100mV (Pin 8)[1]		40	43		dB
V_{9-7}	Voltage on filter capacitor without external load[1]			$V_{CC} - 0.25$		V
R_{9-8}	Source resistance[1]		6	8	10	kΩ
Mono/stereo control						
	Pilot threshold voltages (peak-to-peak values)					
$V_{I(P-P)}$	for stereo 'ON'	8.5		21	30	mV
$V_{I(P-P)}$		15		43	61	mV
$V_{I(P-P)}$	for mono 'ON'	8.5	6	15		mV
$V_{I(P-P)}$		15	12	30		mV
	Switch hysteresis					
ΔV_I	V_{ION}/V_{IOFF}[1]			3		dB
	Switching time at $C_{14-7} = 0.22\mu$F					
t_{STON}	for stereo 'ON'[1]			15		ms
t_{MON}	for mono 'ON'[1]			27		ms
External mono/stereo control[5] (see Figure 12)						
V_{14-7}	Switching voltage for	8.5			0.7	V
V_{14-7}	external mono control	15			1.4	V
or: $-V_{4-5}$[1]			315			mV
$-V_{4-5}$	Control voltage for channel separation: α = 6dB	8.5		120		mV
$-V_{4-5}$		15		130		mV
ΔV_{4-5}[1]					± 20	mV
$-V_{4-5}$	α = 26dB	8.5		70		mV
$-V_{4-5}$		15		80		mV
	Control voltage					
$-V_{4-5}$	for mono 'ON'	8.5		240		mV
$-V_{4-5}$		15		270		mV
$-V_{4-5}$	for stereo 'ON'	8.5		220		mV
$-V_{4-5}$		15		250		mV
ΔV_{4-7}	Control voltage difference for α = 6dB; stereo 'ON'	8.5	80	100	120	mV

DC ELECTRICAL CHARACTERISTICS (Continued)

Input signal: m = 100% ($\Delta f = \pm 75$kHz); pilot signal: m = 9% ($\Delta f = \pm 6.75$kHz); Modulation frequency: 1kHz; $V_{3-5} = V_{4-5} = 0V$; De-emphasizing time. t = 50μs; oscillator adjusted to f_{OSC} at a pilot voltage $V_I = 0V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	V_{CC} (V)	LIMITS			UNIT
			Min	Typ	Max	
Muting circuit[5] (see Figure 13)						
$-V_{3-5}$	Control voltage for an attenuation: α = 3dB	8.5		140		mV
$-V_{3-5}$		15		145		mV
ΔV_{3-5}[1]				±20		mV
$-V_{3-5}$	α = 26dB	8.5		255		mV
$-V_{3-5}$		15		270		mV
α	Attenuation with $V_{3-5} = 0V$[1]				0.2	dB
α	with $-V_{3-5} = 450mV$[1]			80		dB
I_1	LED driver output current at an attenuation: α = 3dB[1]		1.2	1.7	2.2	mA
$-V_{3-5}$	Control voltage	8.5		150		mV
$-V_{3-5}$	for $I_1 = 200\mu A$	15		160		mV
Control inputs						
$V_{3,4,5-7}$	Recommended voltage range[1]		0		4	V
$I_{3,4,5}$	Input bias current[1]			10	100	nA
Indicator driver						
V_{1-7SAT}	Output saturation voltages at $I_1 = 20mA$; $V_{3-5} = 0V$[1]			1.2	1.8	V
V_{2-7SAT}	at $I_2 = 20mA$[1]			0.5	1	V
$I_{1,2}$	Output leakage current at $V_{1,2-7} = 24V$[1]			20		μA
VCO						
f_{OSC}	Oscillator frequency adjustable with R_{10-7}[1]			76		kHz
f_{OSC}	Spread of free-running frequency at nominal external circuitry[1]		71		82	kHz
TC	Free-running frequency[6] dependency with temperature[1]			1×10^{-4}	400	$°C^{-1}$
$\Delta f_{OSC}/\Delta V_{CC}$	with supply voltage[1]					Hz/V
$\Delta f/f$	Capture and holding range for a pilot input voltage $V_{PIL} = 0.5 \times V_{PIL\ NOM}$[1]		±2			%
S_{TOT}	PLL control slope (total)[1]			4.5		kHz/μs
V_{10-7}	DC voltage at Pin 10[1]			2.1		V
or:				$3.2V_{BE}$		V
V_{4-7}	Frequency measuring point; internal switching threshold[1]			6		V
or:				$9V_{BE}$		V
$V_{4-7(P-P)}$	Output voltage (peak-to-peak value) at Pin 4; R = 4.7kΩ[1]			350		mV
R_{4-7}	Output resistance[1]			5		kΩ

NOTES:

1 V_{CC} = 8.5 or 15V

2 Intermodulation suppression (BFC Beat-Frequency Components)

$$\alpha_2 = \frac{V_O(\text{signal}) \text{ (at 1kHz)}}{V_O(\text{spurious}) \text{ (at 1kHz)}};\ f_S = (2 \times 10\text{kHz}) - 19\text{kHz}$$

$$\alpha_3 = \frac{V_O(\text{signal}) \text{ (at 1kHz)}}{V_O(\text{spurious}) \text{ (at 1kHz)}},\ f_S = (3 \times 13\text{kHz}) - 38\text{kHz}$$

measured with 91% mono signal, f_M = 10 or 13kHz, 9% pilot signal

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3. Traffic radio (VWF) suppression

$$\alpha_{57(VWF)} = \frac{V_O(\text{signal}) \text{ (at 1kHz)}}{V_O(\text{spurious}) \text{ (at 1kHz } \pm 23\text{kHz)}}$$

measured with: 91% stereo signal; f_M = 1kHz; 9% pilot signal; 5% traffic subcarrier (f = 57Hz, f_M = 23Hz AM, m = 60%).

4. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_O(\text{signal}) \text{ (at 1kHz)}}{V_O(\text{spurious}) \text{ (at 4kHz)}}; \; f_S = 110\text{kHz} - (3 \times 38\text{kHz})$$

$$\alpha_{190} = \frac{V_O(\text{signal}) \text{ (at 1kHz)}}{V_O(\text{spurious}) \text{ (at 4kHz)}}; \; f_S = 186\text{kHz} - (5 \times 38\text{kHz})$$

measured with: 90% mono signal; f_M = 1kHz; 9% pilot signal; 1% spurious signal (f_S = 110 or 186kHz, unmodulated).

5. SCA (Subsidiary Communication Authorization)

$$\alpha_{67} = \frac{V_O(\text{signal}) \text{ (at 1kHz)}}{V_O(\text{spurious}) \text{ (at 9kHz)}}; \; f_S = (2 \times 38\text{kHz}) - 67\text{kHz})$$

measured with: 81% mono signal; f_M = 1kHz; 9% pilot signal; 10% SCA-subcarrier (f_S = 67kHz, unmodulated).

6. Assuming $V_T = \frac{k \times T}{q}$ = 28.6mV at T_J = 330°C

7. The effects of external components are not taken into account.

APPLICATION NOTES

1. When mono/stereo control and muting control are not used, Pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   a. A capacitor at Pin 12 (C_{12-7}): phasing 19/38kHz
   b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (α_2); see Figure 2.
4. External mono 'ON' switch; see Figure 3.
5. Switching 'OFF' the oscillator; see Figure 4.

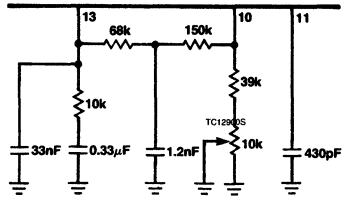
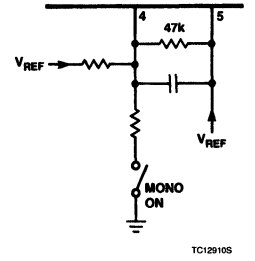
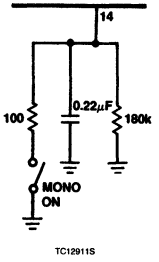


Figure 1. PLL-filter for α_2 = 70dB at V_{CC} = 15V

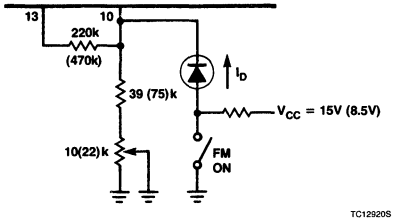


a. At Pin 4; $-V_{4-5}$ 300mV



b. At Pin 14

Figure 2



NOTE:
The oscillator is switched off when
I_D100μA (> 50μA for V_{CC} = 8.5V) and I_D < 1mA

Figure 3

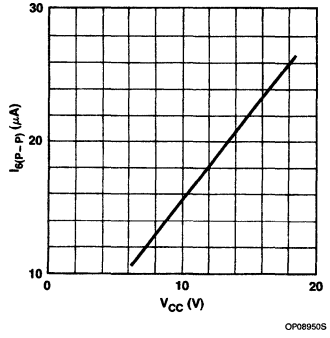


Figure 4. Signal Handling Range at the Input for I_{6NOM} (± 75kHz); $V_{9-7} = V_{CC}$

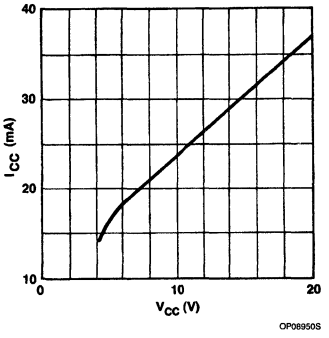


Figure 5. Supply Current Consumption at $V_{9-7} = V_{CC}$

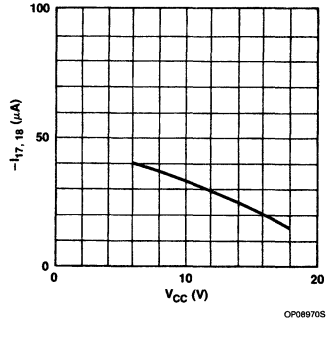


Figure 6. DC Current in the Feedback Loop of the Output Amplifier

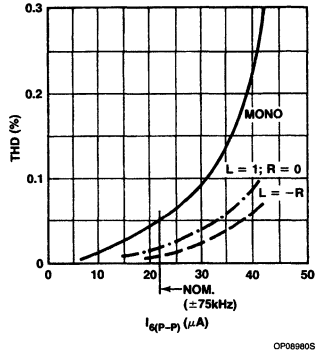


Figure 7. Total Harmonic Distortion (THD) as a Function of the Peak-to-Peak Input Current at Pin 6; V_{CC} = 15V; f_M = 1kHz; $V_{3-5} = V_{4-5}$ = 0V

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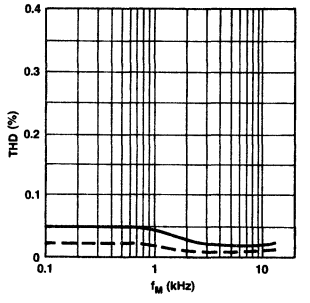


NOTES:
——— Mono
– – – Stereo; L = –R, 91% +9% pilot signal
V_{CC} = 15V
$I_{6(P-P)}$ = 21.5μA

Figure 8. Total Harmonic Distortion (THD) as a function of the Modulation Frequency (f_M)

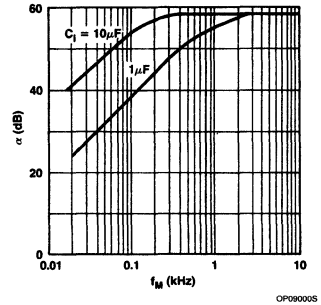


Figure 9. Channel Separation (α) as a Function of the Modulation Frequency (f_M); V_{CC} = 15V; R_I = 47kΩ; V_{4-5} = 0V

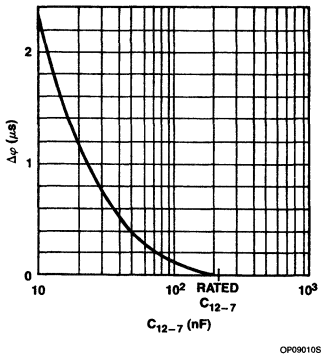
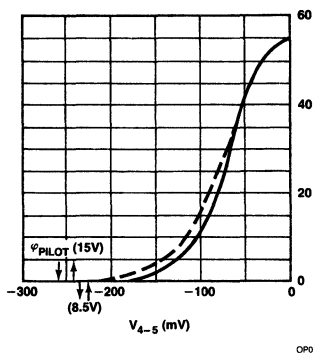
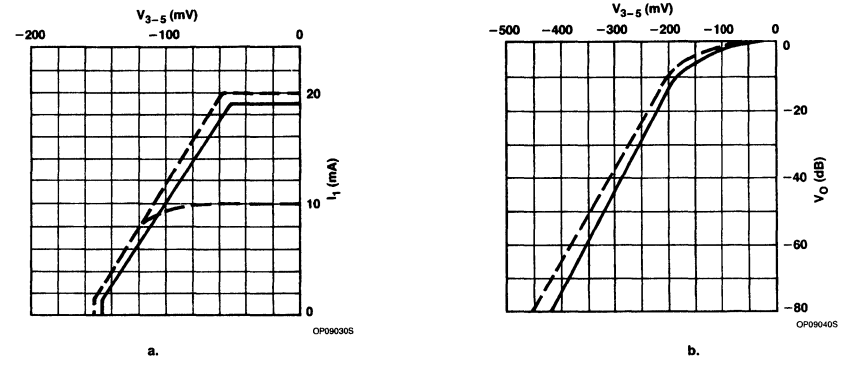


Figure 10. Phase Shift Between Pilot Signal at the Input and the Internal Carrier Processing as a Function of C_{12-7}



NOTES:
——— V_{CC} = 8.5V
– – – – V_{CC} = 15V

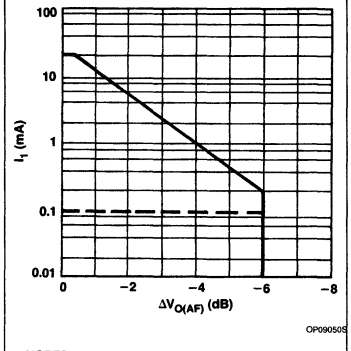
Figure 11. Mono/Stereo Control at f_M = kHz; α is the Channel Separation



NOTES:
I_1 in mA curves for V_{PL}/R_{BIAS1}(Pin 1), - - - - 22V/1kΩ
——— 14V/680Ω
— — — 10V/680Ω

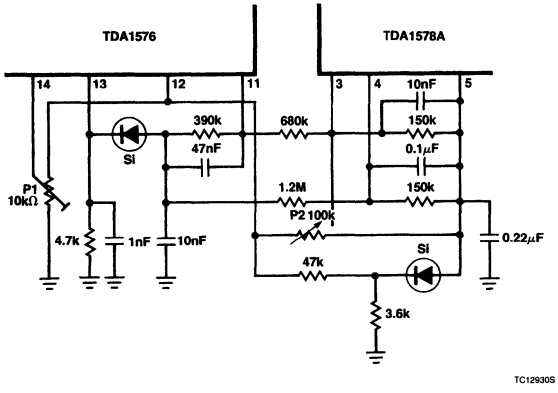
NOTE:
V_O in dB curves, ——— V_{CC} = 8.5V
— — — V_{CC} = 15V

Figure 12. Muting (V_O) and Muting Indicator Current (I_1) as a Function of V_{3-5}



NOTES:
——— R_{BIAS1} = 680Ω.
- - - - R_{BIAS1} = matched

Figure 13. Muting Indicator Current; V_{CC} = 8.5 to 15V; V_{PL} = 14V



NOTES:
1 At $V_{I(HF)}$ = 100μV with P1 to α = 6dB (channel separation)
2 At $V_{I(HF)}$ = 15μV with P2 to $V_{O(AF)}$ = −3dB

Figure 14. Application Information for External Circuitry to Provide External Mono/Stereo and Muting Control

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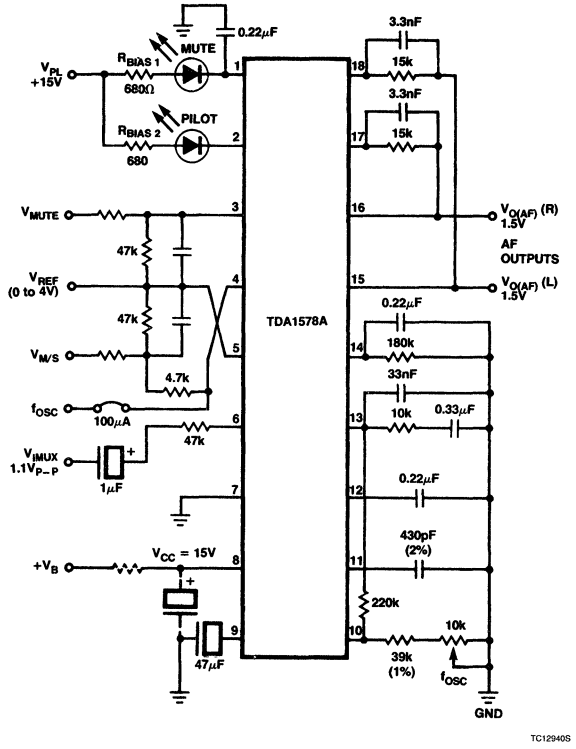


Figure 15. Typical Application Circuit Using TDA1578A for V_{CC} = 15V

Signetics

TDA7040
Low Voltage PLL Stereo Decoder

Preliminary Specification

Linear Products

DESCRIPTION

The TDA7040T is a low voltage PLL stereo decoder designed for low power portable FM stereo radios.

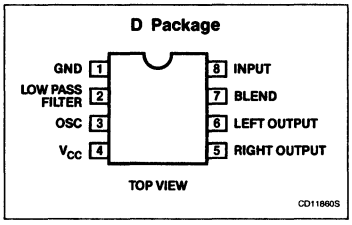
FEATURES

- **4-Pole LP filter with a 70kHz corner frequency to suppress unwanted out-of-band input signals**
- **Integrated 228kHz oscillator**
- **Pilot presence detector and soft mono/stereo blend**
- **Built-in interference suppression**
- **External stereo lamp driver**
- **Chooseable gain**

APPLICATIONS

- **Portable radio**
- **PLL**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (SO-8; SOT-96A)	−25°C to +85°C	TDA7040TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−10 to +70	°C

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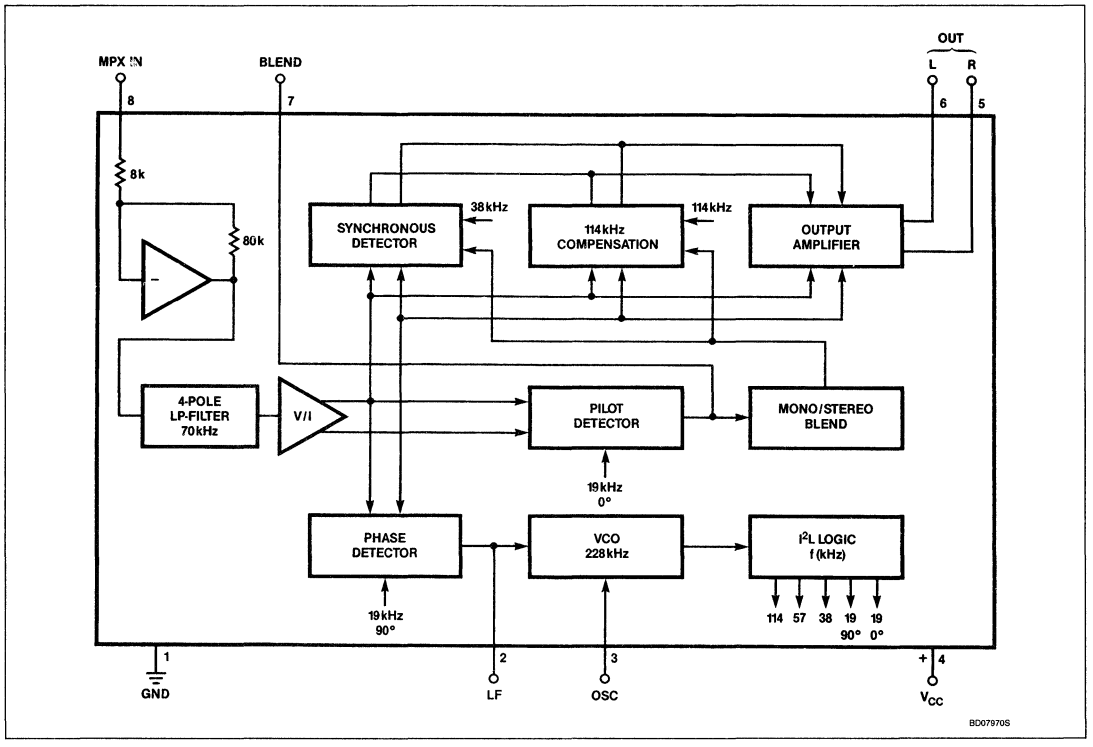
Low Voltage PLL Stereo Decoder TDA7040

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{CC} = 3V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		1.8	3.0	6.0	V
I_{CC}	Supply current	Without input signal		3	4	mA
V_{OUT}	Output voltage	V_{IN} (L + R) = 120mV$_{(RMS)}$ f = 1kHz		240		mV$_{(RMS)}$
	Channel balance	V_{IN} (L + R) = 40mV$_{RMS}$ f = 1kHz		0	1	dB
R_{OUT}	Output resistance			5		kΩ
THD	Total harmonic distortion	V_{IN} (L + R) = 40mV$_{RMS}$ f = 1kHz		0.1	TBD	%
THD	Total harmonic distortion	V_{IN} (L + R) = 40mV$_{(RMS)}$ f = 1kHz V_{CC} = 12mV$_{RMS}$		0.3	TBD	%
S/N	Signal-to-noise ratio	V_{IN} (L + R) = 120mV$_{RMS}$ f = 1kHz		70		dB
S/N	Signal-to-noise ratio	V_{IN} (L + R) = 120mV$_{RMS}$ f = 1kHz V_{CC} = 12mV$_{RMS}$		70		dB
SEP	Channel separation	V_{IN} (L + R) 40mV$_{RMS}$ f = 1kHz V_{CC} = 12mV$_{RMS}$	TBD	40		dB
	Capture range	V_{CC} = 12mV$_{RMS}$		±3		%
	Carrier leak 19kHz	V_{IN} (L + R) = 120mV$_{RMS}$ f = 1kHz V_{CC} = 12mV$_{RMS}$		30		dB
	Carrier leak 38kHz	V_{IN} (L + R) 120mV$_{RMS}$ f = 1kHz V_{CC} 12mV$_{RMS}$		50		dB
	SCA rejection	V_{IN} (L + R) 120mV$_{RMS}$ f = 1kHz; V_{CC} = 12mV$_{RMS}$ V_{SCA} = 12mV$_{RMS}$; f = 67kHz		70		dB
	ACI suppression 114kHz	V_{IN} (L + R) = 120mV$_{RMS}$ f = 1kHz V_{CC} = 12mV$_{RMS}$ V_{ACI} = 1.3mV$_{RMS}$		90		dB
	ACI suppression 190kHz			85		dB
α57	Traffic radio (VWF) suppression[1]			75		

NOTE:

1. Traffic radio (VWF) suppression

$$\alpha 57\ (VWF) = \frac{V_{O(signal)}\ (at\ 1kHz)}{V_{O(spurious)}\ (at\ 1kHz \pm 23Hz)}$$

measured with 91% stereo signal; f_M = 1kHz; 9% pilot signal; 5% traffic sub-carrier (f = 57Hz, f_M = 23Hz AM, m = 60%).

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TDA7040T and TDA7021T RADIO SPECIFICATION[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
THD	Total harmonic distortion	V_{IN} = (L + R) Signal f_{MOD} = 1kHz Pilot On		0.5		%
THD	Total harmonic distortion	V_{IN} = L – Signal f_{MOD} = 1kHz Pilot On		1.0		%
S/N	Signal-to-noise ratio	V_{IN} = (L + R) Signal f_{MOD} = 1kHz Pilot Off		56		dB
S/N	Signal-to-noise ratio	V_{IN} = L – Signal f_{MOD} = 1kHz Pilot On		50		dB
SEP	Channel separation	V_{IN} = L – Signal f_{MOD} = 1kHz Pilot On		26		dB
SEP	Channel separation end of RF-band	V_{IN} = L – Signal f_{MOD} = 1kHz Pilot On f_{RF} = 87MHz		14		dB
V_{OUT}	Output voltage	V_{IN} = (L + R) Signal f_{MOD} = 1kHz Pilot Off		80		mV_{RMS}

NOTES:
1 Noise measured unweighted 400Hz to 15kHz
2 Conditions unless otherwise specified VHF = $1mV_{RMS}$, f_{HF} = 97MHz, f_{DEV} = 22 5kHz, $f_{DEV\ PILOT}$ = 6 75kHz

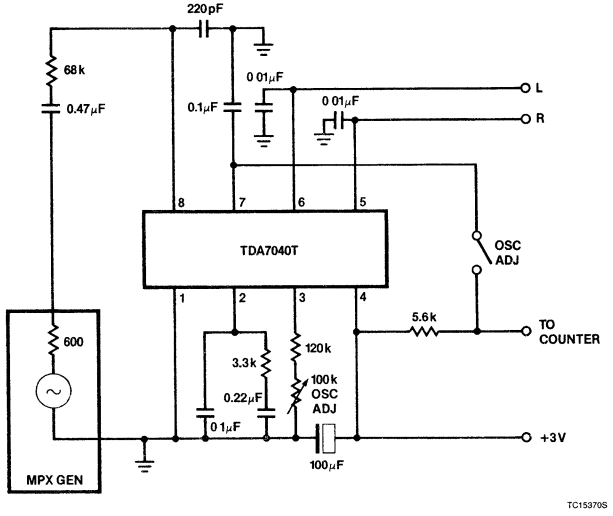

Figure 1. Test Circuit

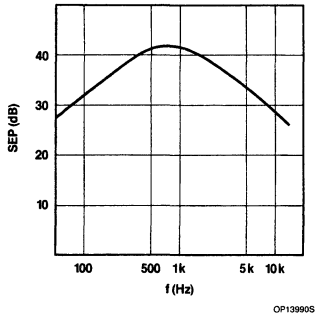

Figure 2. Channel Separation vs Frequency

APPLICATION NOTES

The combination of TDA7040T and TDA7021T will make a low cost FM stereo receiver with an absolute minimum of peripheral components and simple layout.

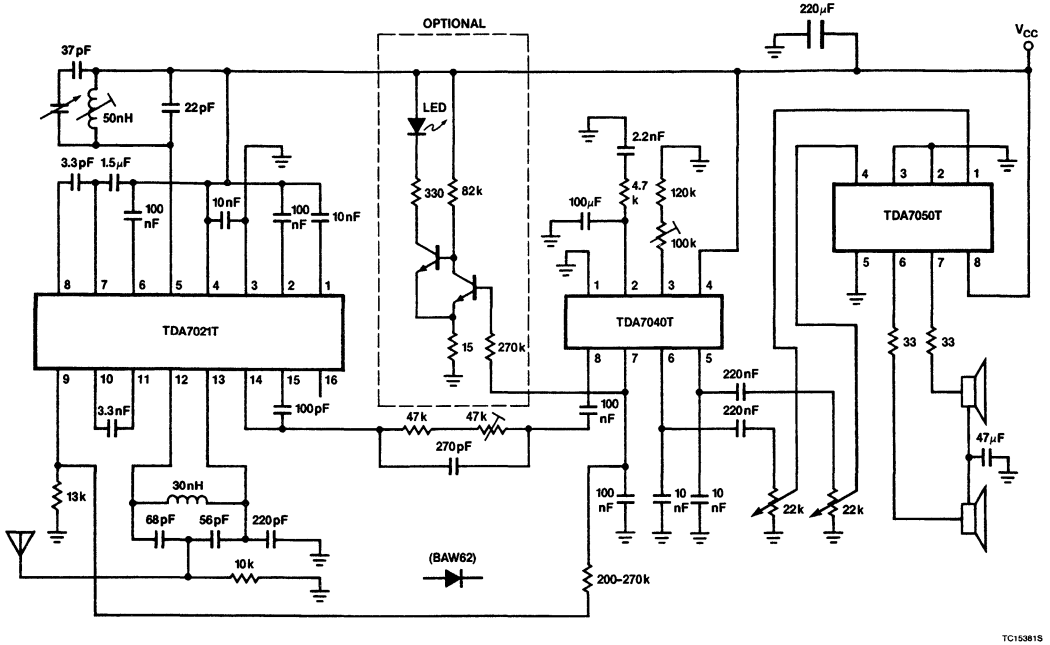

Figure 3. Application Diagram

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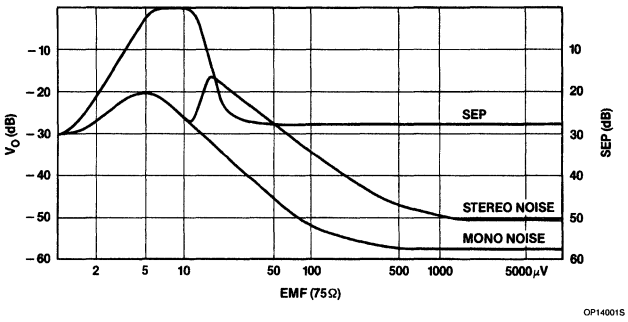


Figure 4. Signal-to-Noise and Separation Behavior of Application in Figure 3

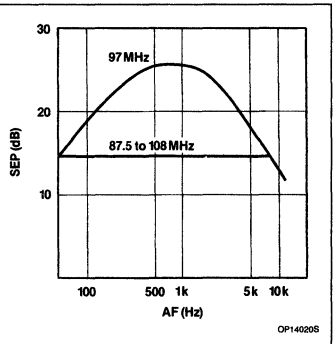


Figure 5. Channel Separation vs AF

Signetics

TEA5581
PLL Stereo Decoder

Preliminary Specification

Linear Products

DESCRIPTION

The TEA5581 is a PLL stereo decoder with cassette head amplifiers especially for car radios. It has SDS circuitry where fluctuating signal strength can cause demodulation noise and distortion. The stereo decoder is compensated for a typical IF filter with a roll-off frequency of 50kHz (2dB down at 38kHz).

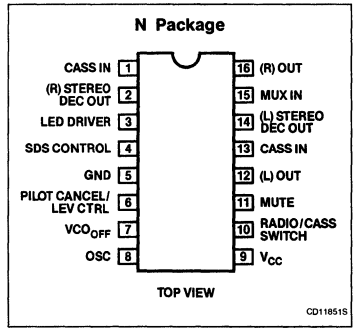
FEATURES

- **A voltage-controlled oscillator**
- **A pilot presence detector and an automatic mono/stereo switch**
- **A matrix and two amplifiers for the left and right output signal**
- **Two output buffers with 10dB gain and low output impedance**
- **Mute circuit**
- **A source selector for radio or cassette**
- **An input amplifier of which the gain can be adjusted by means of an external input resistor**
- **A pilot cancelling circuit for an extra suppression of the pilot signal of 15dB**
- **An SDS circuit (Signal Dependent Stereo) for a smooth change over from stereo to mono at weak tuner input signals**

APPLICATIONS

- **Auto radios**
- **Stereo receivers**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−30°C to +80°C	TEA5581N

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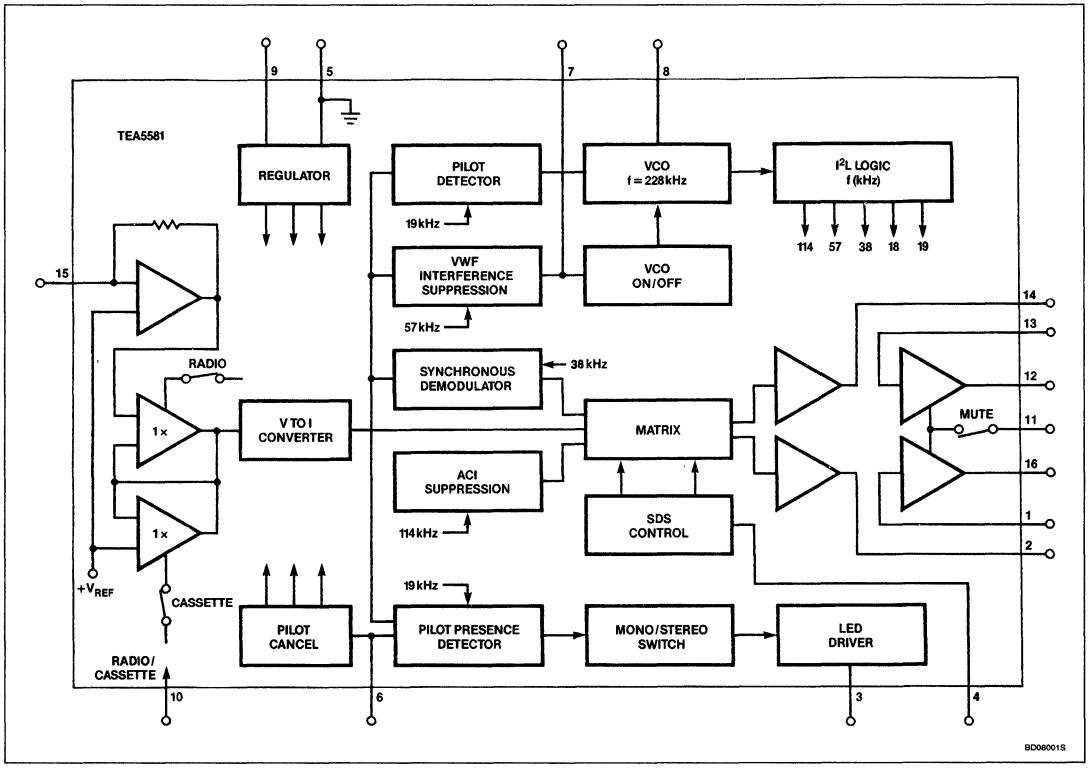
PLL Stereo Decoder TEA5581

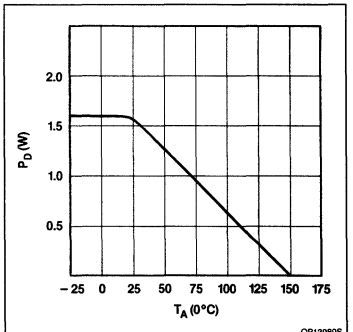
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C
P_{TOT}	Total power dissipation	see derating curve	
V_{3-5}, V_{9-5}	Supply voltage (Pin 3 and Pin 9)	18	V
I_3	LED driver (peak current)	75	mA

DERATING CURVE



NOTE:
Thermal resistance of SOT-38 is θ_{JA} = 75°C/W

ELECTRICAL SPECIFICATION AND OPERATING CHARACTERISTICS

All voltages with reference to Pin 5.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Operating supply voltage	7.0	8.5	16	V

DC ELECTRICAL CHARACTERISTICS Measured in test set-up at $V_{CC} = 8.5V$ and $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_{TOT}	Current consumption (without LED driver)		15		mA
P_D	Power dissipation		125		mW
V_{15-5} $V_{16-5,\ 12-5}$	Voltage on Pin 15 Pins 16, 12		2.0 3.5		V V
$-I_{14}$ $-I_2$	DC current Pin 14 Pin 2	195 195	275 275	390 390	µA µA
$-I_3$	Output current Pin 3			20	mA
V_7	Switch "VCO-OFF" voltage (Pin 7)		2.2		V
I_7	Current (Pin 7)			50	µA

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AF CONDITIONS

Input MUX signal is $1V_{P-P}$ = 1kHz; V_{PILOT} = 32mV (9%), oscillator adjusted to f_{OSC} = 228kHz at V_I=0V, unless otherwise specified. (All figures are measured with a roll-off network of 50kHz (2dB down at 38kHz) at the input.

AC ELECTRICAL CHARACTERISTICS

All parameters are measured in the circuit at nominal supply voltage (V_{CC} = 8.5V) and T_A = 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
A_V	Gain input amplifier			20	dB
Z_I	Input impedance (external)		47		kΩ
V_I	Maximum input voltage			TBD	V_{P-P}
A_V	Gain output buffers		10		dB
V_O 12, 16	Maximum output voltage (THD ⩽ 1%)			TBD	V_0
Z_O	Output impedance (Pin 12, Pin 16)			500	Ω
Z_L	Maximum load impedance	5.0			kΩ
∝muting	Muting level		90		dB
∝	Source selector		90		dB
Overall performance					
V_{OUT}/V_{IN}	Overall gain (mono)	10	11	12	dB
V12 = V16	AF output voltage (RMS) mono	1.1	1.25		V
THD	Total harmonic distortionat $V_{OUT} = 1.2V_{RMS}$[1]			0.5	%
V_{OUT} 12, 16	Output voltage for THD = 1%			TBD	V
$\frac{V_{OUT}\ 12}{V_{OUT}\ 16}$	Output channel unbalance		0.2	1	dB
∝	Channel separation (L = 1; R = 0)	26	40		dB
S/N S/N	Signal-to-noise ratio Bandwidth 20Hz to 16kHz Bandwidth DINA		76 82		dB dB
SDS control					
V4	10dB channel separation		1.0		V
V4	Full stereo (channel separation ⩾ 26dB)		1.2		V
V4	Full mono (channel separation ⩽ 1dB)		0.8		V
Stereo/mono switch (R6 – 5 = 180k)[2]					
V_I	For switching to stereo		14	20	mV
V_I	For switching to mono	4			mV
ΔV_I	Hysteresis		4		mV

AC ELECTRICAL CHARACTERISTICS (Continued) All parameters are measured in the circuit at nominal supply voltage (V_{CC} = 8.5V) and T_A = 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Carrier and harmonic suppression at the output[3]					
α19	Pilot signal; f = 19kHz (R6-5 = 180kΩ)[2]	32	40		dB
α38	Subcarrier; f = 38kHz		45		dB
α57	f = 57kHz		50		dB
α228	f = 228kHz		75		dB
	Intermodulation[4]				
	f_M = 10kHz, spurious signal				
α2	f_S = 1kHz		50		dB
	f_M = 13kHz; spurious signal				
α3	f_S = 1kHz		50		dB
α57(VWF)	Traffic radio (VWF) suppression f = 57kHz[5]		80		dB
α67	SCA (subsidiary communications authorization) f = 67kHz[6]		70		dB
	ACI (adjacent channel interference)[7]				
α114	f = 114kHz		90		dB
α190	f = 190kHz		60		dB
	Ripple rejection				
	(f = 100Hz; V_{RIPPLE} = 100mV)				
RR100	at V9 = 8 5V		46		dB
RR100	at V9 = 7.0V		TBD		dB
VCO (voltage-controlled oscillator)					
f_{OSC}	Oscillator frequency adjustable with R8		228		kHz
Δf/f	Capture range (deviation from 228kHz center frequency) V_{PILOT} = 32mV		4		%
T_C	Temperature drift (uncompensated)		+200		ppm/°C
Muting circuit (Pin 11)					
V_{Dlow}	Input voltage (mute "on")			0.8	V
$-I_{Dlow}$	current (mute "on")	25	10		μA
V_{Dhigh}	Input voltage (mute "off")	2 0		8.0	V
I_{Dhigh}	current (mute "off")			TBD	μA

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AC ELECTRICAL CHARACTERISTICS (Continued) All parameters are measured in the circuit at nominal supply voltage (V_{CC} = 8.5V) and T_A = 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Source selector (Pin 10) switching level					
V_{Clow} $-I_{Clow}$	Cassette-to-Radio	 25	 10	0.8	V μA
V_{Chigh} I_{Chigh}	Radio-to-Cassette	2.0		8.0 TBD	V μA

NOTES:

1. Guaranteed for mono, mono + pilot, stereo.
2. Also adjustable.
3. Reference output voltage at 1kHz (measured channel R (Pin 2)).
4. Intermodulation suppression (BFC: Beat-Frequency Components):

$$\alpha 2 = \frac{V_O \text{ (signal) at 1kHz}}{V_O \text{(spurious) a t 1kHz}}; \; f_S = (2 \times 10kHz) - 19kHz$$

$$\alpha 3 = \frac{V_O \text{ (signal) at 1kHz}}{V_O \text{(spurious) at 1kHz}}; \; f_S = (3 \times 13kHz) - 38kHz$$

measured with: 91% mono signal; f_M = 10 or 13kHz; 9% pilot signal.

5. Traffic radio (VWF) suppression.

$$\alpha 57 \text{ (VWF)} = \frac{V_O \text{ (signal) at1kHz}}{V_O \text{ (spurious) at 1kHz} \pm 23Hz}$$

measured with. 91% stereo signal; f_M = 1kHz; 9% pilot signal; 5% traffic subcarrier (f = 57kHz; 60% AM modulated with f mod. 23Hz).

6. SCA (Subsidiary Communications Authorization):

$$\alpha 67 = \frac{V_O \text{ (signal) at1kHz}}{V_O \text{ (spurious) at 9kHz}}; \; f_S = (2 \times 38kHz) - 67kHz$$

measured with: 81% mono signal; f_M = 1kHz; 9% pilot signal; 10% SCA-subcarrier (f_S = 67kHz, unmodulated).

7. ACI (Adjacent Channel Interference):

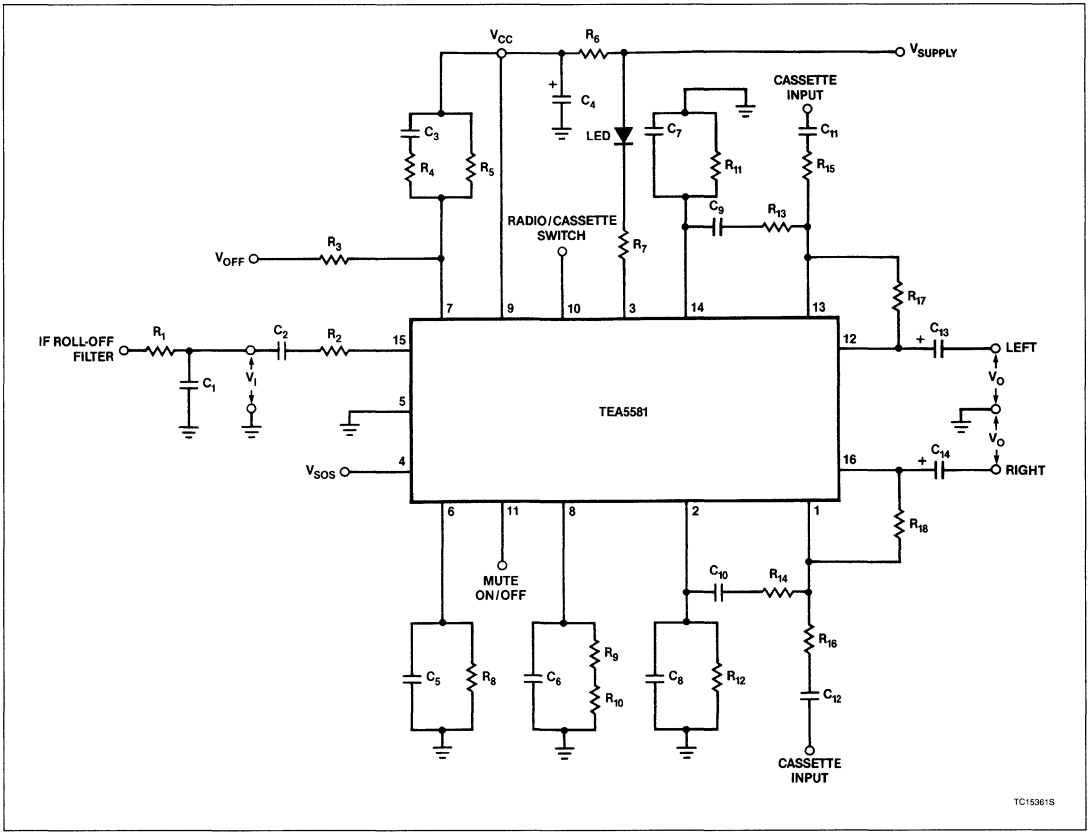
$$\alpha 114 = \frac{V_O \text{ (signal) at 1kHz}}{V_O \text{ (spurious) at 4kHz}}; \; f_S = 110kHz - (3 \times 38kHz)$$

$$\alpha 190 = \frac{V_O \text{ (signal) at 1kHz}}{V_O \text{ (spurious) at 4kHz}}; \; f_S = 186kHz - (3 \times 38kHz)$$

measured with 90% mono signal; f_S = 1kHz; 9% pilot signal; 1% spurious signal (f_S = 110 or 186kHz, unmodulated).

PLL Stereo Decoder TEA5581

APPLICATION DIAGRAM



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Signetics

μA758
FM Stereo Multiplex Decoder, Phase-Locked Loop

Product Specification

Linear Products

DESCRIPTION

The μA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

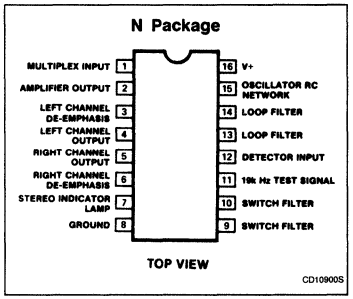
FEATURES

- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input — low impedance output**

APPLICATIONS

- **Stereo decoder for radios**

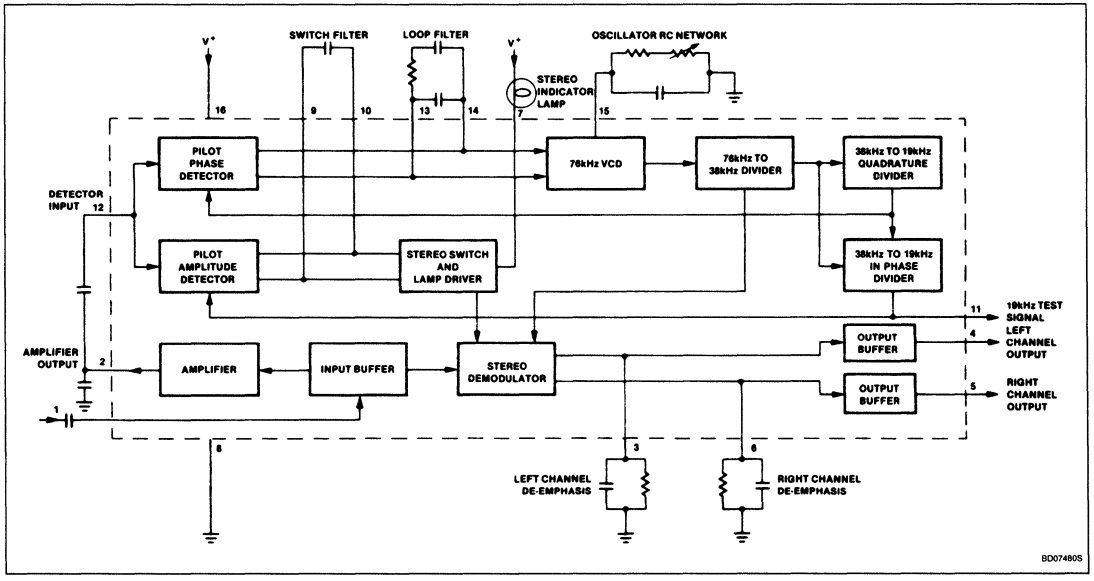
PIN CONFIGURATION



ORDERING INFORMATION

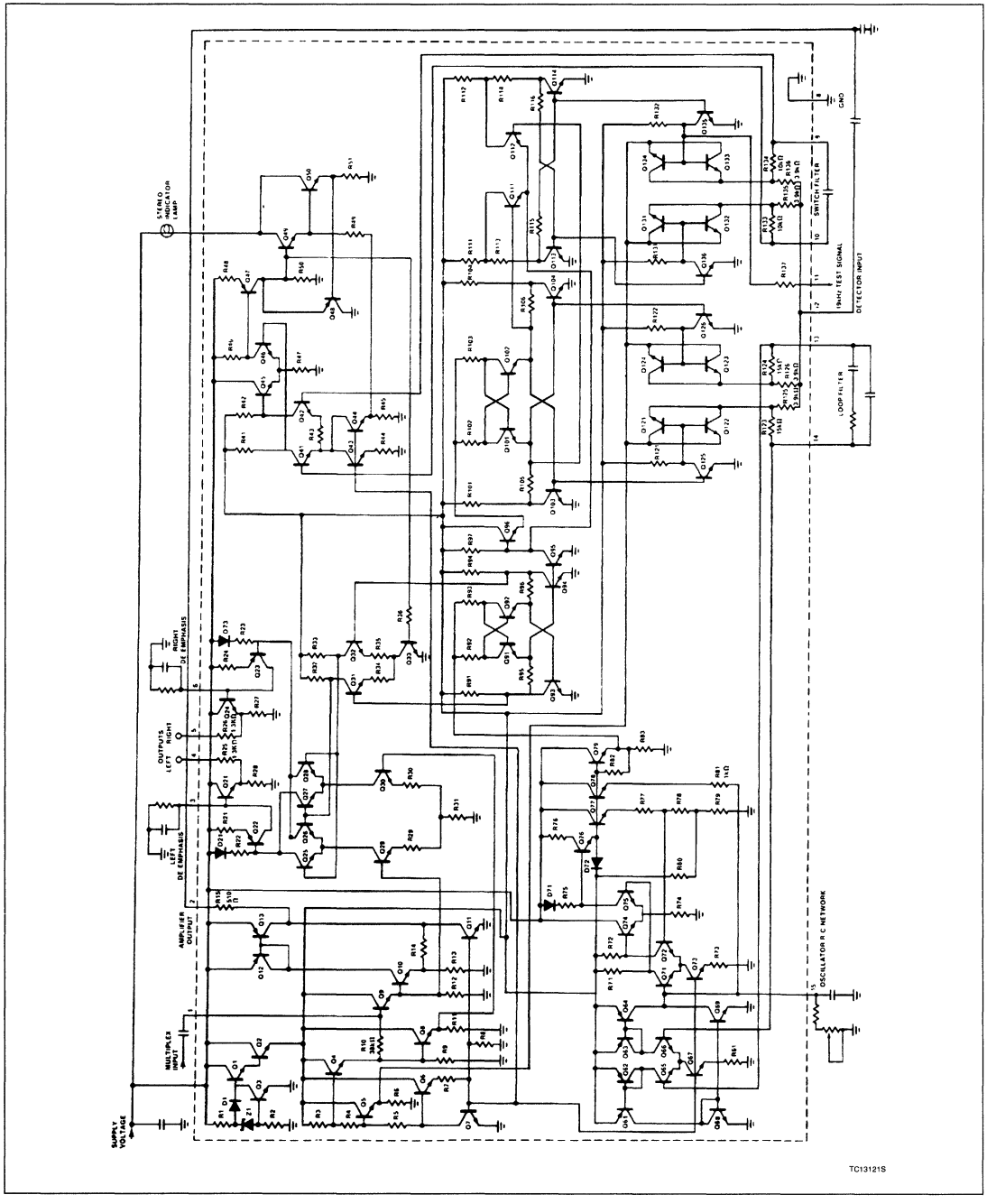
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	μA758N

BLOCK DIAGRAM



FM Stereo Multiplex Decoder, Phase-Locked Loop — μA758

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+18	V
V_{CC}	Supply voltage ($\leq$ 15 seconds)	+22	V
	Voltage at lamp driver terminal (Lamp OFF)	+22	V
P_D	Internal power dissipation	730	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +125	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+ = +12V, 19kHz pilot level = 30mV$_{RMS}$, multiplex signal (L = R, pilot OFF) = 300V$_{RMS}$, modulation frequency = 400Hz or 1Hz, Test Circuit 1, unless otherwise specified .

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{CC} I_L	Supply current Maximum available lamp current	Lamp OFF	 75	31 150	38	mA mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
R_{IN}	Input resistance		20	35		kΩ
R_{OUT}	Output resistance		0.9	1.3	2.0	kΩ

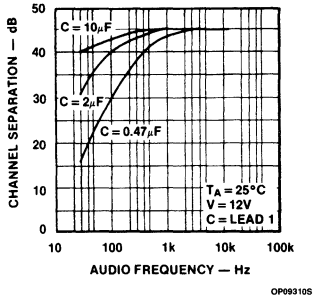
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$\Delta(V_4\&V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
PSRR	Power supply ripple rejection	200Hz, 200mV$_{RMS}$	35			dB
SEP	Channel separation	100Hz 400Hz 10kHz	30	40 45 45		dB dB dB
BAL	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on Lamp turn-off	 2.0	18 7.0	25	mV$_{RMS}$ mV$_{RMS}$
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
THD	Capture range Total harmonic distortion	Multiplex level = 600mV$_{RMS}$ pilot OFF	2.0	4.0 0.4	6.0 1.0	% %
	19kHz rejection 38kHz rejection SCA rejection[1]		25 25	35 45 70		dB dB dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	0°C $\leq T_A \leq$ 25°C 25°C $\leq T_A \leq$ 70°C		+0.1 −0.4	±2 ±2	% %

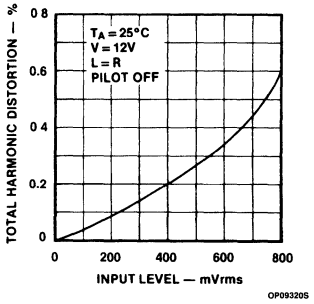
NOTES:
1. Measured with a stereo composite consistency of 80% stereo. 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from Pin 15 to ground, in Test Circuit, required to set reference frequency at Pin 11 to 19kHz ±10Hz.

TYPICAL PERFORMANCE CHARACTERISTICS

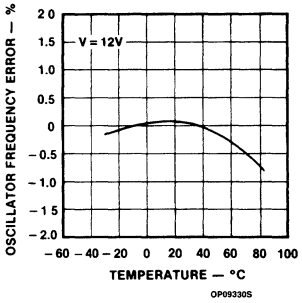
Channel Separation vs Audio Frequency



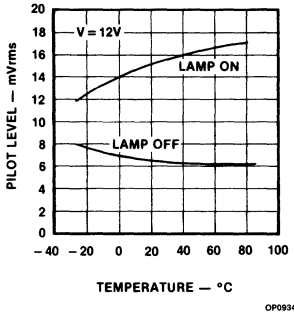
Harmonic Distortion vs Input Level



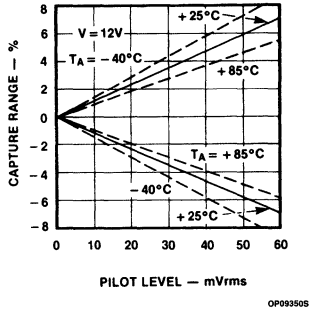
Oscillator Free-Running Frequency Error vs Ambient Temperature



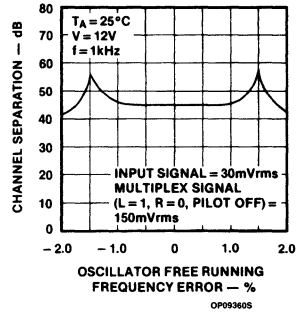
Lamp Turn-On & Turn-Off Sensitivity vs Ambient Temperature



Capture Ranges vs Pilot Level



Channel Separation vs Oscillator Free-Running Frequency Error



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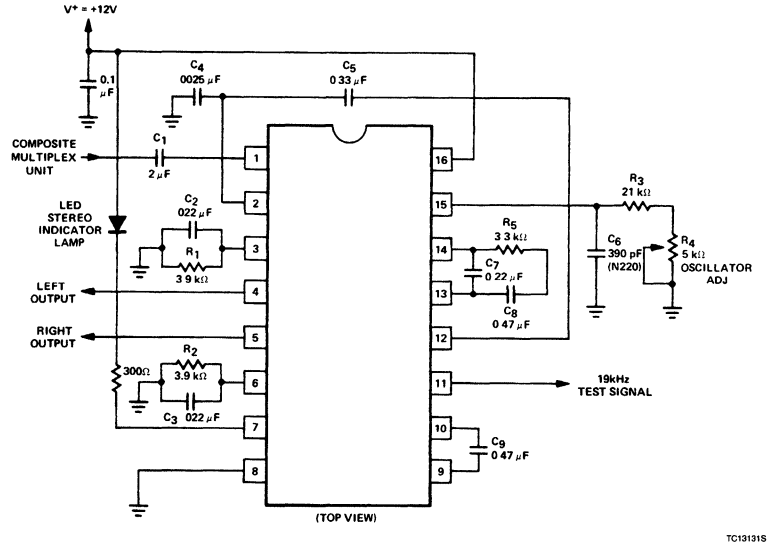
FM Stereo Multiplex Decoder, Phase-Locked Loop μA758

TEST CIRCUIT AND TYPICAL APPLICATION



NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20%, unless otherwise specified C_1 tolerance = +100%, −20%, C_6 tolerance = ±1% in test circuit and ±5% in typical applications R_3 tolerance = ±1%, R_4 tolerance = ±10%, R_1 and R_2 tolerance = ±1% in Test Circuit and ±5% in Typical Application

Signetics

Linear Products

AN191
Stereo Decoder Applications Using the μA758

Application Note

INTRODUCTION

The phase-locked loop (PLL) has been used for many years in consumer equipment Due to the nature of FM Stereo Multiplex Systems, where prime importance is the channel separation, discrete systems lacked the tracking ability over wide temperature and voltage ranges to be done economically.

The development of the monolithic PLL and improvements in IC processing have made the Phase-Locked Loop FM Stereo Multiplexer Decoder a reality

MAJOR ADVANTAGES

The economic advantages in using the PLL multiplex decoding system are not only cost reduction, by eliminating peripheral components, but the man-hour cost reduction by eliminating turning coils, thereby eliminating tedious alignment procedures

The cost advantages are extremely significant and are in addition to the following.

- 45dB channel separation
- Automatic stereo/mono switching
- Stereo indicator lamp driver with current limiting
- High impedance input — low impedance outputs
- 70dB SCA rejection (subsidiary carrier authorization)
- One adjustment for complete alignment
- 10V to 16V supply voltage range

FM STEREO MULTIPLEX SUBCARRIER AND PILOT

The two (2) basic signals differentiating an FM stereo multiplex signal from an FM monaural signal are the 19kHz pilot and the 38kHz subcarrier. The frequency and phase relationship of these signals is well defined.

Earlier systems had to reconstruct the 38kHz subcarrier by using the 19kHz pilot. This system required frequency multipliers and selective filters (coils). Since maximum channel separation is directly related to proper phasing, alignment procedures were extremely critical and therefore expensive In addition, long-term stability and performance were degraded due to component aging, and temperature

Use of the PLL as the multiplex decoder eliminated these shortcomings since the phase accuracy of the 38kHz signal is limited only by the loop gain of the system and the free-running oscillator stability. Both of these parameters are easily controlled, providing easy, rapid adjustment and excellent long-term stability

GENERAL DESCRIPTION

The μA758 is a monolithic Phase-Locked Loop FM Stereo Multiplex decoder using the 16-lead DIP N package This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

REFERENCING THE BLOCK DIAGRAM

The upper row of blocks comprises the PLL which regenerates the 38kHz subcarrier, necessary for multiplex signal demodulation. The basic 76kHz generator is voltage-controlled, and is divided by two to insure a 50% duty cycle 38kHz internally-generated signal. This symmetry is necessary for maximum left/right channel separation and SCA rejection (band-centered at 67kHz). Dividing the 38kHz by two generates the 19kHz signal necessary to lock on to the incoming pilot signal. A second 19kHz signal is generated which is in quadrature to the first internally-generated 19kHz signal and in phase with the pilot. This second 19kHz is mixed in a quadrature (synchronous) phase detector to operate the stereo switch and lamp driver circuitry.

When a stereo signal is present, the stereo switch enables the stereo demodulator, and when a stereo signal is not present, the demodulator is disabled, allowing the system to reach optimum noise performance.

FUNCTIONAL OPERATION

To aid in understanding the system operation, the μA758 equivalent circuit has been broken down into subsections as follows (see Figure 2):

I Buffer Amplifier and Bias Supplies
II Demodulator
III Stereo Switch and Lamp Driver
IV Voltage-Controlled Oscillator
V Frequency Dividers
VI Pilot Phase and Amplitude Detectors

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Stereo Decoder Applications Using the μA758 AN191

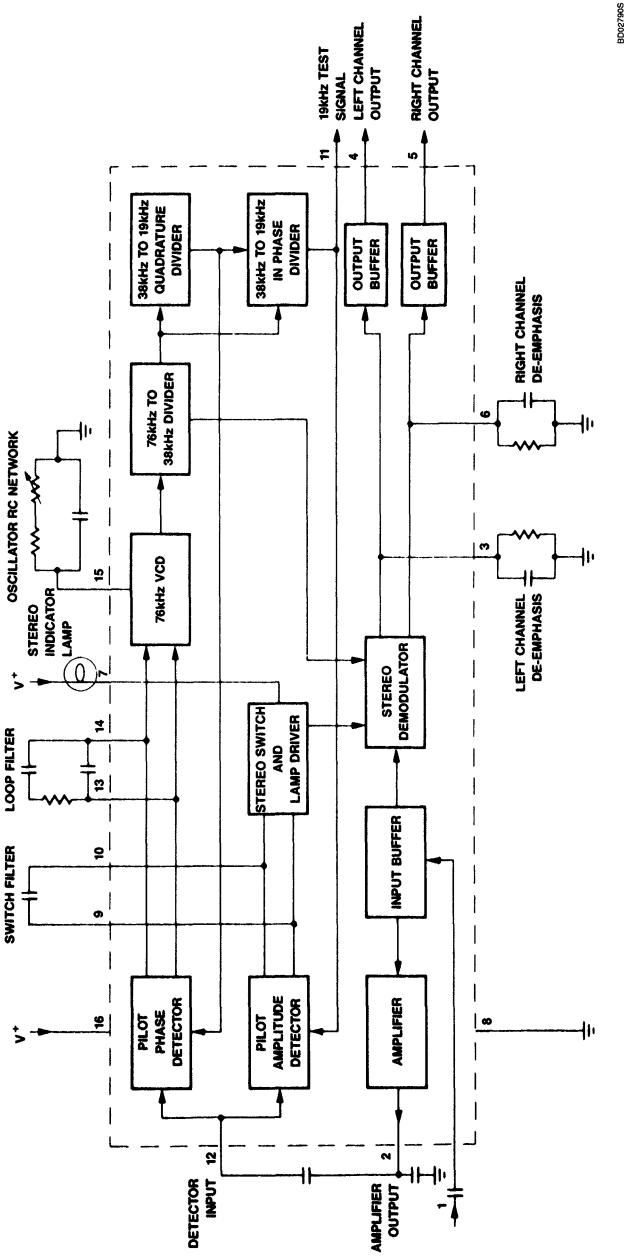

Figure 1. Block Diagram

Stereo Decoder Applications Using the μA758

AN191

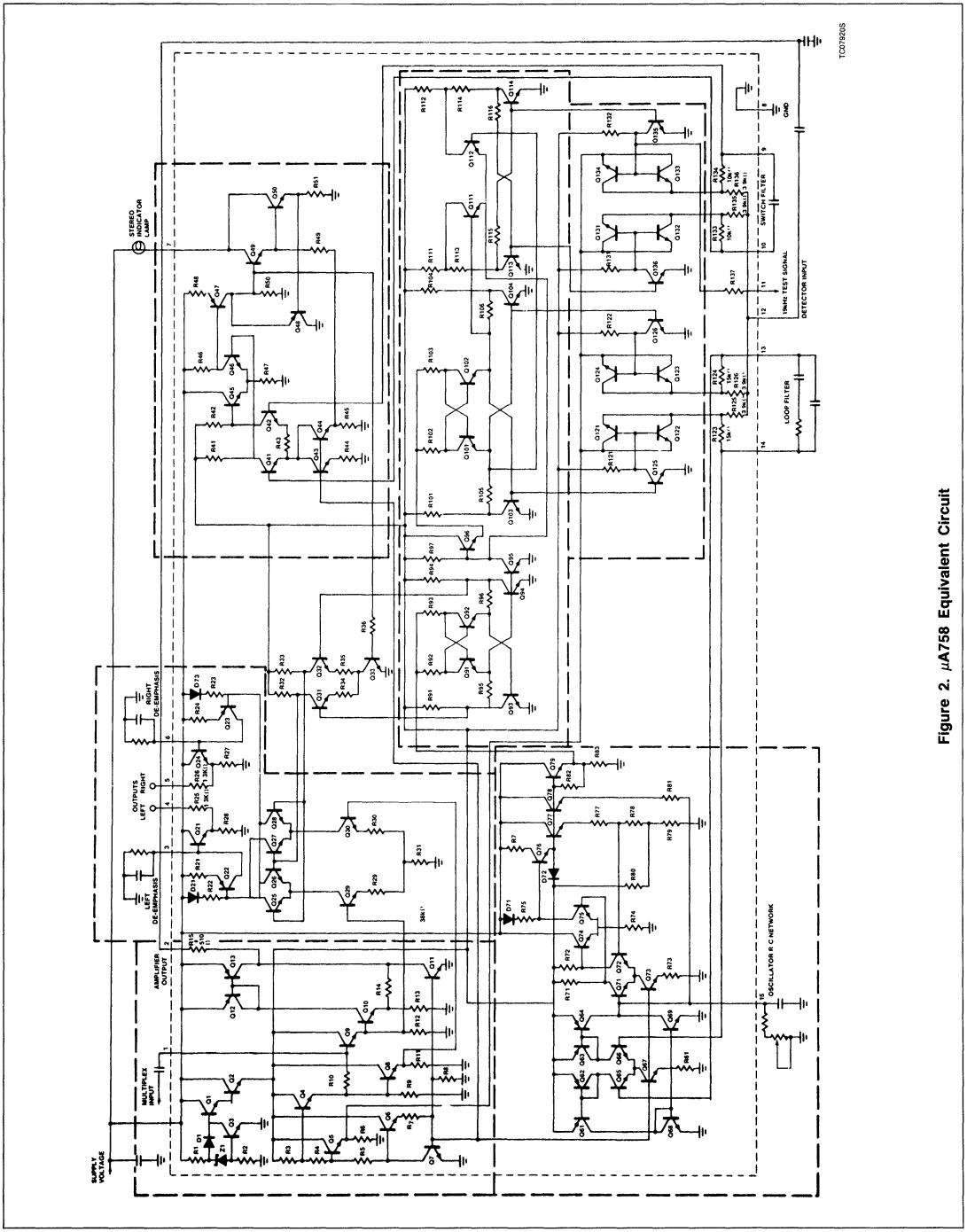

Figure 2. μA758 Equivalent Circuit

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Stereo Decoder Applications Using the μA758 AN191

I. Buffer Amplifier and Bias Supplies (Figure 3)

The zener diode, Z, and its associated transistors generate a 6V internal voltage reference source. From this 6V reference, additional bias levels are established via resistors R3, R4, and R5. In addition, transistor Q7 acts as the control source for several current mirrors; Q11 in the Buffer Amplifier, Q43 and Q44 in the Stereo Switch and Lamp Driver (III) and Q67 and Q73 in the Voltage Controlled Oscillator (IV).

The input Buffer Amplifier (Q8, Q9) level shifts the composite multiplex input signal to 2 levels each in phase with each other.

Transistors Q10 – Q13 amplify this same signal by the ratio of:

$$A = \frac{R14}{R13}$$

This amplified signal, the gain of which is independent of supply voltage variation, is fed to the Pilot Phase and Amplitude Detectors (VI).

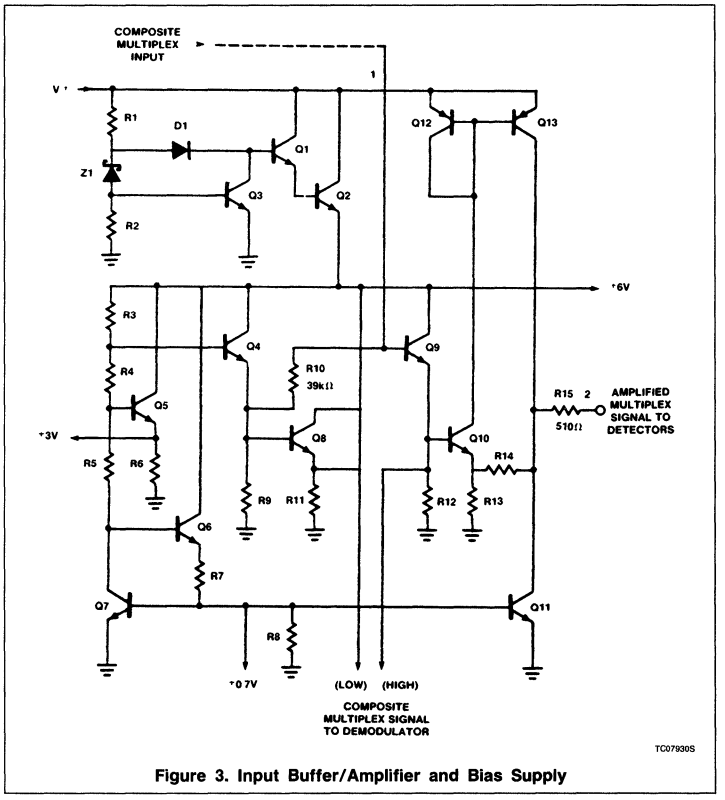

Figure 3. Input Buffer/Amplifier and Bias Supply

II. Demodulator (Figure 4)

The basic demodulator, Q25 – Q30, is a fully-balanced detector similar to standard phase-locked loop types. The addition of resistors R29, R30, and R31 introduces a small offset to allow a small multiplex signal in the collector of Q30. This signal compensates the crosstalk components inherent to the synchronous switching demodulation process.

Switching to the left and right channels is accomplished through Q25 and Q26 when the 38kHz drive is present at their bases. This occurs when Q33 is "on." When Q33 is off, a DC bias is placed at the bases of Q25 and Q26 through resistors R32 and R33, this automatically converts the system to monophonic operation.

Supply voltage rejection is accomplished at the demodulator outputs by converting the audio to current supplies in Q23 and Q24. The voltage developed across PNP transistors is

$$V_e = (V^+ + V_{MOD}) - (V_{BE} + V_{D1} + [R22\ I_{AC}] + V_{MOD})$$

where V_{BE} = base-emitter voltage across Q22 and Q23

V_{MOD} = modulation on the power line

V_{D1} = diode drop in D21

$(R22)I_{AC}$ = voltage drop due to current in the demodulator

Simplifying the above reduces to

$$V_e = V+ - (V_{BE} + V_{D1} + R22\ I_{AC}) \quad (1)$$

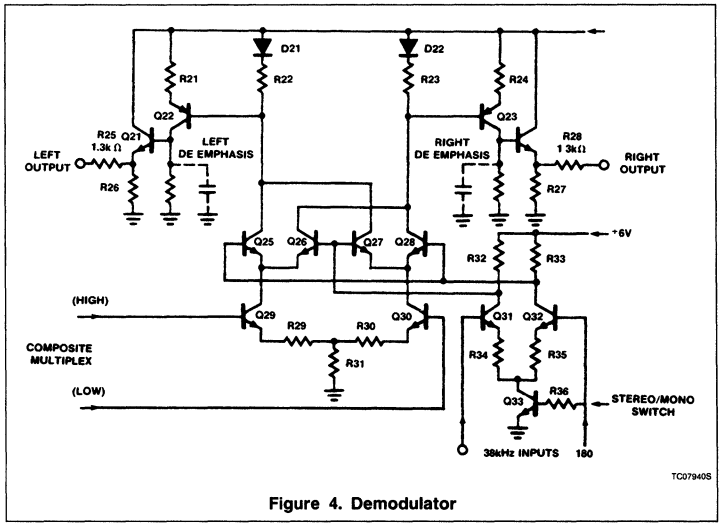

Figure 4. Demodulator

The output voltage developed is

$$V_{OUT} = \left(\frac{V_e}{R21}\right) R_{EXT} \quad (2)$$

where R_{EXT} = external resistor

The output voltage at Pins 4 and 5 are provided through 1.3k resistors driven by emitter-followers Q21 and Q24.

III. Stereo Switch and Lamp Driver (Figure 5)

The pilot amplitude detector differential voltage is sensed by the differential amplifier Q41 and Q42. This pair, in conjunction with their load resistors (R41, R42), controls amplifiers Q45, Q46. Positive feedback action is achieved through Q47, R50, Q50 and R46 (which turns off Q44).

The turn-on threshold is the differential input voltage required to overcome the offset voltage required to overcome the offset voltage in R43 times the current summation of I_{R44} and I_{R45}. When the lamp is on, Q44 is off and the differential voltage across R43 is reduced by the amount ($I_{R45} \times I_{R43}$), which means a lower turn-off voltage is required. This voltage difference is referred to as the switch hysteresis.

Transistors Q48 senses the current across R51 which therefore controls the maximum current in the Stereo Indicator Lamp.

$$I_{MAX} = \frac{V_{BE}Q48}{R151} \quad (3)$$

IV. Voltage-Controlled Oscillator (Figure 6)

The basic oscillator Q71 – Q79 is an RC relaxation type which generates a positive low duty cycle, 76kHz output. The frequency is established by Equations 4 and 5.

The control voltage from the phase detector into the transconductance amplifier Q61 – Q69 converts the differential error to a bidirectional single-ended current drive to the oscillator.

Voltage on the capacitor is compared with the set voltages by the differential input stage Q71, Q72. This feeds Q74, Q75. The output of Q75 drives a PNP inverter, Q76, (whose action eliminates power supply modulation as described in the demodulator section of this note), when these set limits are reached the direction of charge reverses.

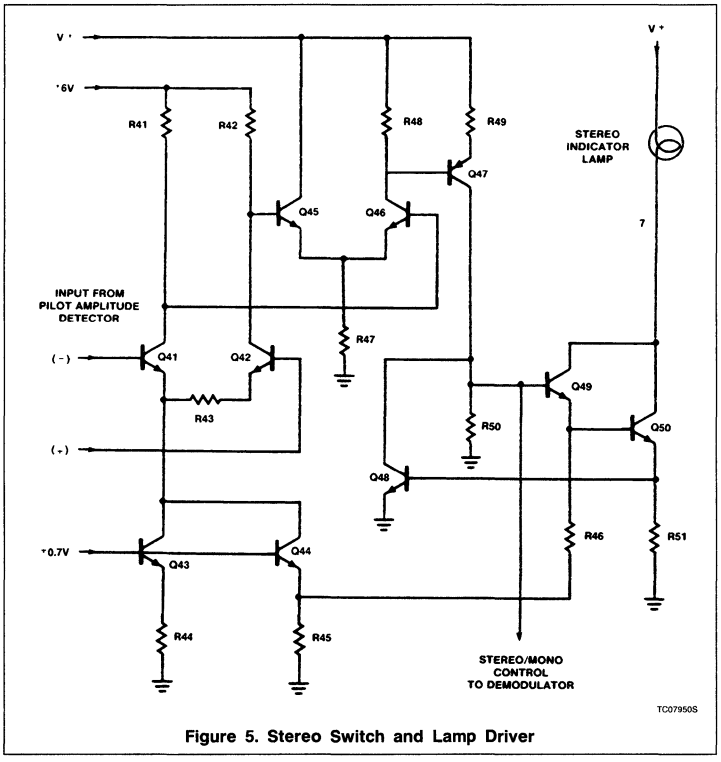

Figure 5. Stereo Switch and Lamp Driver

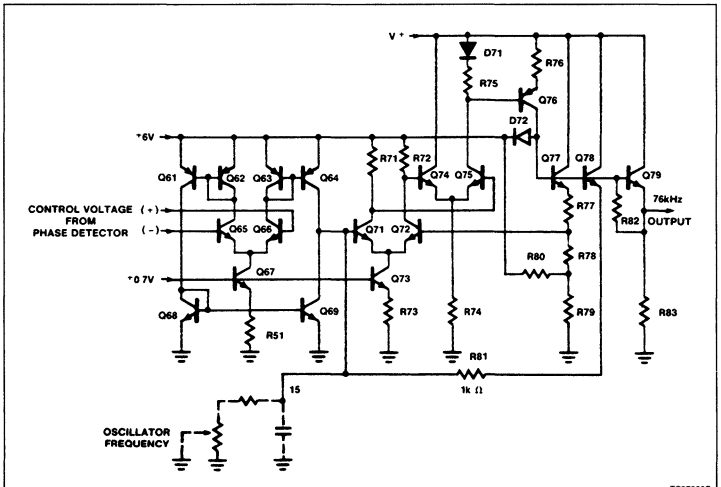

Figure 6. Voltage-Controlled Oscillator (VCO)

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Lower set voltage is set by R79, R80, and the regulated 6V supply. The upper set voltage (V_H) involves two (2) additional resistors R77 and R78 and is established when Q76 turns on Q77. Both set levels are referenced to the regulated 6V supply and are therefore dependent only on resistor ratios. (Proper design layout should also eliminate temperature variations.)

Capacitor charging is through Q78 and R8 and discharging through the external fixed resistor

Equations 4 and 5 of Figure 7 are first-order expressions for the change and discharge periods.

Q79 supplies a positive output pulse necessary to operate the 38kHz dividers.

V. Frequency Dividers (Figure 8)

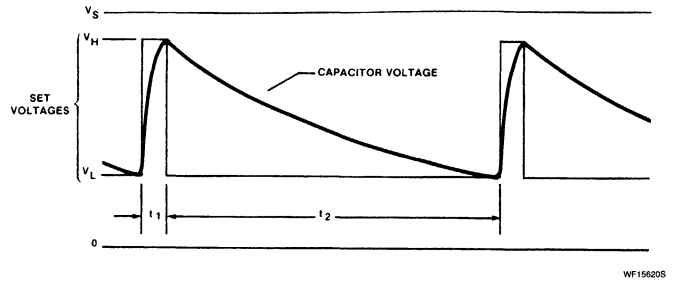
Transistors Q91 through Q94 form a simple divide-by-two circuit which converts the pulse output from the 76kHz oscillator to a 38kHz square wave.

The divider changes state during the positive excursion of the input pulse supplied from the emitter of Q79 in the oscillator. Initially, when the input is low, Q91 and Q92 are OFF and we may arbitrarily assume Q93 is ON and Q94 is OFF

As the potential on the input rises, Q91 starts conduction before Q92 because the emitter of Q91 is at a lower potential than the emitter of Q92. (The emitter of Q91 is connected through R95 to the collector of Q93 which is in saturation, whereas the emitter of Q92 is at the V_{BE}(ON) potential of Q93). Since Q91 is ON, the current from both R92 and R93 flows through the emitter of Q91 into R95. As this current increases, the rising voltage at the emitter of Q91 turns Q94 ON which removes base drive to Q93 and turns it OFF, thus producing a change-of-state in the divider Even though the relative potentials at the emitters of Q91 and Q92 are now reversed, current continues to flow in Q91 for the duration of the positive input because Q92 is held OFF by Q91 When the input returns to a low potential, Q91 turns OFF. The divider remains in its present state until driven by the next positive-going input.

Oppositely phased 38kHz outputs to the demodulator are taken from the collectors of Q93 and Q94. Transistors Q95 and Q96 are used to drive the two 38kHz dividers.

The 38kHz Quadrature Divider has an identical configuration to the 76kHz divider. A change-of-state occurs with each positive excursion of the 38kHz input signal from the emitter of Q96



NOTES:
Basic timing equations

$$t1 = R81\ C\ 1n\frac{V_S - V_L}{V_S - V_H} \quad \text{(Equation 4)}$$

$$t2 = RC\ 1n\frac{V_H}{V_L} \quad \text{(Equation 5)}$$

where R and C are external components on Lead 15, R81 is on the chip, and V_H and V_L are set voltages which are a fixed percentage of V_S, the internally-regulated 6V supply

Figure 7. Oscillator Waveforms

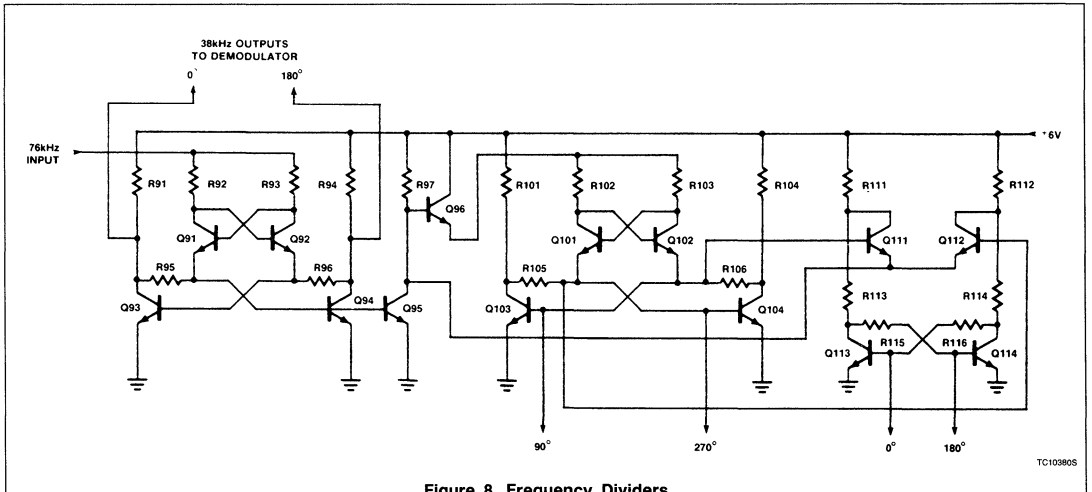


Figure 8. Frequency Dividers

Stereo Decoder Applications Using the μA758 AN191

The 38kHz in-phase divider contains a bistable pair, Q113 and Q114, steered by inputs into Q111 and Q112, (a 38kHz input from the collector of Q95, and 19kHz inputs from the bases of Q103 and Q104). If the 19kHz input to the base of Q111 is high when the 76kHz divider turns Q95 ON, Q111 conducts and removes drive to Q114, changing the state of the bistable pair, Q113 and Q114. The bistable remains in this state until the next 38kHz turn on of Q95 which, this time, turns Q112 ON, removes drive to Q113 and resets the bistable pair. The resulting 19kHz output from Q113 and Q114 is at 90° to the quadrature divider output with no ambiguity in phasing.

VI. Pilot Phase and Amplitude Detectors

The pilot phase detector and pilot amplitude detector, as shown in Figure 9, are synchronous, balanced chopper types which develop differential output signals across external filters. Back-to-back NPN transistor pairs are used for each switch to insure minimum drop regardless of signal polarity without reliance on inverse NPN beta characteristics.

The chopper transistors (Q121 through Q124) in the phase detector are driven from the 38kHz Quadrature Divider through transistors Q125 and Q126. The input signal is supplied from lead 12 through resistors R125 and R126. A differential output is developed across the loop filter, comprised of resistors R123 and R124 and the external RC network between leads 13 and 14.

The pilot amplitude detector (Q131 through Q136), has an identical configuration to the phase detector. Since it operates with drive which is in phase with the pilot signal (90° from the drive to the phase detector), its output is proportional to the amplitude of the pilot component of the multiplex signal. The differential output at leads 9 and 10 is filtered by the external capacitor on these two leads.

A reference 19kHz square wave signal is taken from the collector of drive transistor Q136 through resistor R137 to lead 11. It has the same phasing as the pilot contained in the multiplex input signal.

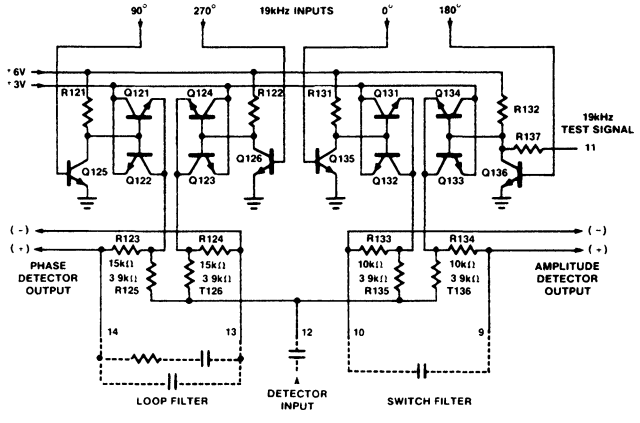
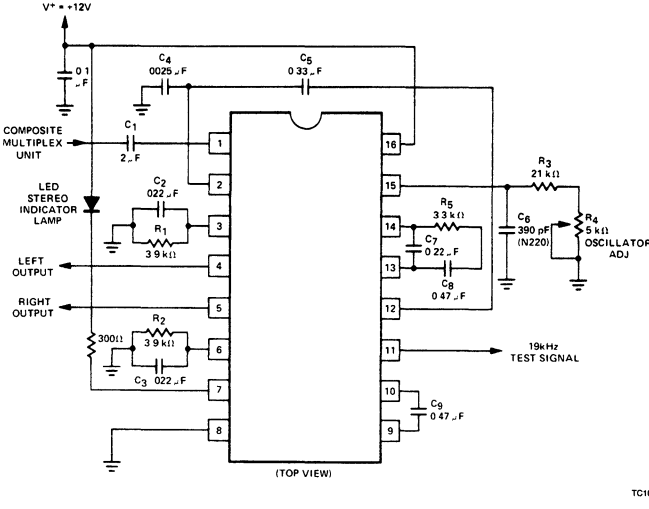


Figure 9. Pilot Phase and Amplitude Detectors



NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified
C1 Tolerance = +100%, −20%
C6 Tolerance = ±1% in test circuit and ±5% in typical application
R3 Tolerance = ±1%
R4 Tolerance = ±10%
R1 and R2 Tolerances = ±1% in test circuit and ±5% in typical application

Figure 10. Test Circuit 1 and Typical Application

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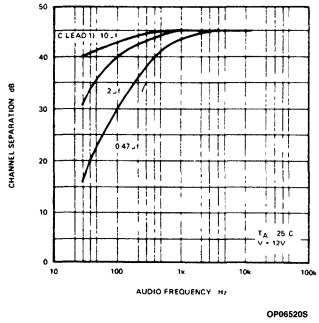
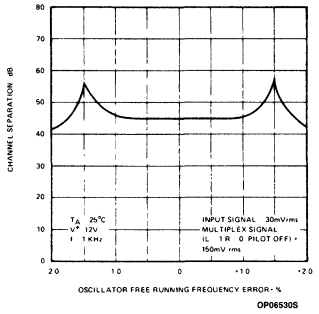
Stereo Decoder Applications Using the μA758 AN191

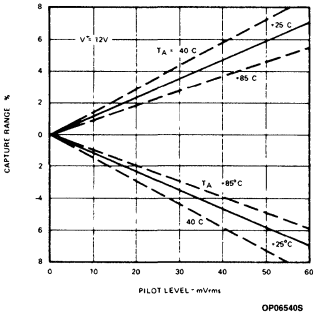
Channel Separation as a Function of Audio Frequency



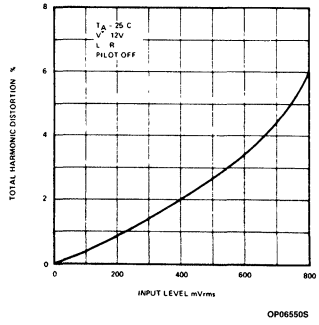
Channel Separation as a Function of Oscillator Free-Running Frequency Error



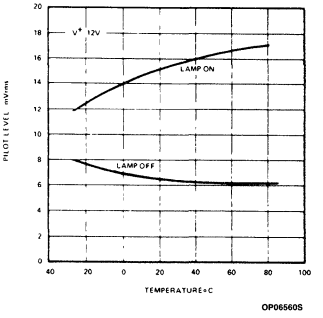
Capture Range as a Function of Pilot Level



Total Harmonic Distortion as a Function of Input Level



Lamp Turn-On and Turn-Off Sensitivity as a Function of Ambient Temperature



Oscillator Free-Running Frequency Error as a Function of Ambient Temperature

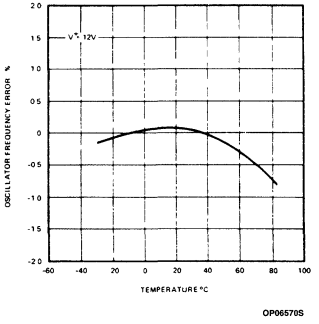


Figure 11. Typical Performance Curves for the μA758 (Test Circuit 1 Unless Otherwise Specified)

Signetics

NE542
Dual Low-Noise Preamplifier

Product Specification

Linear Products

DESCRIPTION

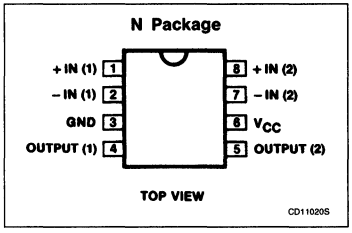
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC}–$2V_{P-P}$), and internal compensation to 10dB. The NE542 operates from a single supply across a range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

FEATURES

- **Low noise — 0.7μV total input noise**
- **High gain — 104dB open-loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC}–$2V_{P-P}$)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz ($15V_{P-P}$)**
- **Internally-compensated (stable at 10dB)**
- **Short-circuit protected**
- **High slew rate 5V/μs**

PIN CONFIGURATION



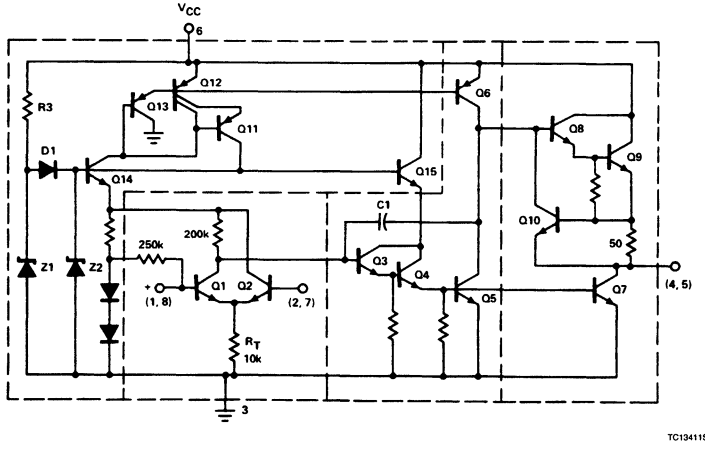
APPLICATIONS

- **Tape preamplifier**
- **Phono preamplifier**
- **Microphone preamplifier**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE542N

EQUIVALENT CIRCUIT



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Dual Low-Noise Preamplifier — NE542

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+24	V
P_D	Power dissipation	500	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	= dc

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

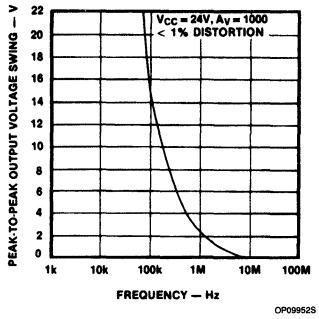
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		9		24	V
I_{CC}	Supply current	$V_{CC} = 9$ to 18V, $R_L = \infty$		9	15	mA
R_{IN}	Input resistance Positive input Negative input			 100 200		 kΩ kΩ
R_{OUT}	Output resistance	Open-loop		150		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

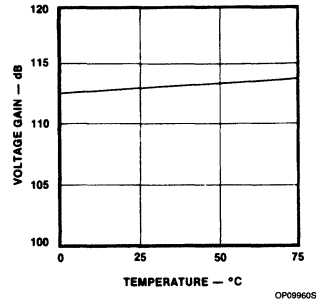
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
A_V	Voltage gain	Open-loop		160,000		V/V
I_{IN}	Negative input current				0.5	
I_{OUT}	Output current	Source Sink (linear operation)	8 2	14 3		mA mA
V_{OUT}	Output voltage swing		V_{CC} −2.5	V_{CC} −2		V
SR	Small signal bandwidth Slew rate			15 5		MHz V/μs
P_{BW}	Power bandwidth	$15V_{P-P}$		100		kHz
V_{IN}	Maximum input voltage	Linear operation, < 2.5% distortion			300	mV_{RMS}
PSRR	Power supply rejection ratio	f = 60, 120Hz f = 1kHz		100 110		dB dB
	Channel separation	f = 1kHz	40	70		dB
THD	Total harmonic distortion	40dB gain, f = 1kHz		0.1	0.3	%
	Total equivalent input noise	$R_S = 600Ω$, 100 − 10,000Hz		0.7	1.2	$μV_{RMS}$
	Noise figure	$R_S = 50kΩ$, 10 − 10,000Hz $R_S = 20kΩ$, 10 − 10,000Hz $R_S = 10kΩ$, 10 − 10,000Hz $R_S = 5kΩ$, 10 − 10,000Hz		1.2 1.2 1.5 2 4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

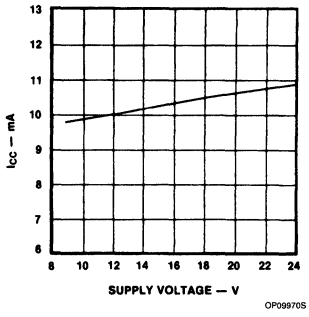
Large-Signal Frequency Response



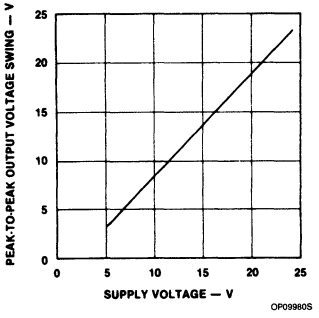
Gain vs Temperature



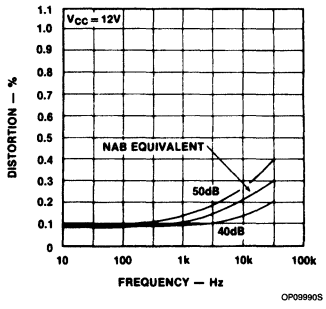
V_{CC} vs I_{CC}



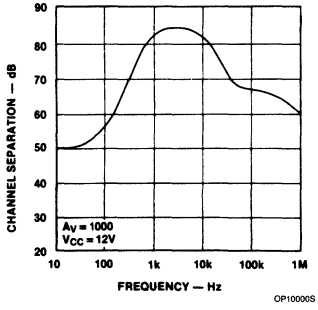
Peak-to-Peak Output Voltage Swing vs V_{CC}



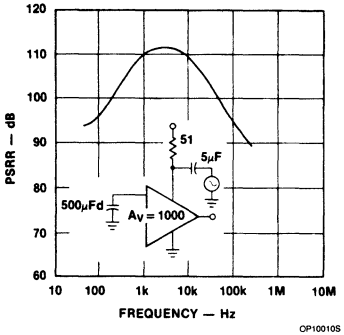
% Distortion



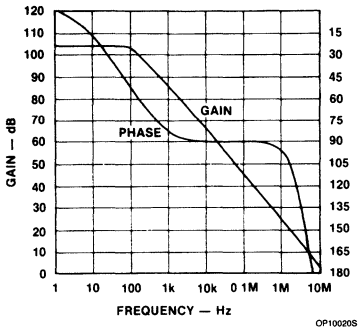
Channel Separation



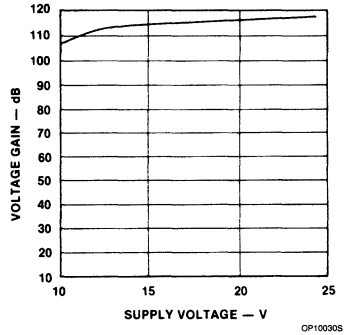
PSRR vs Frequency



Gain and Phase Response



Voltage Gain vs Supply Voltage



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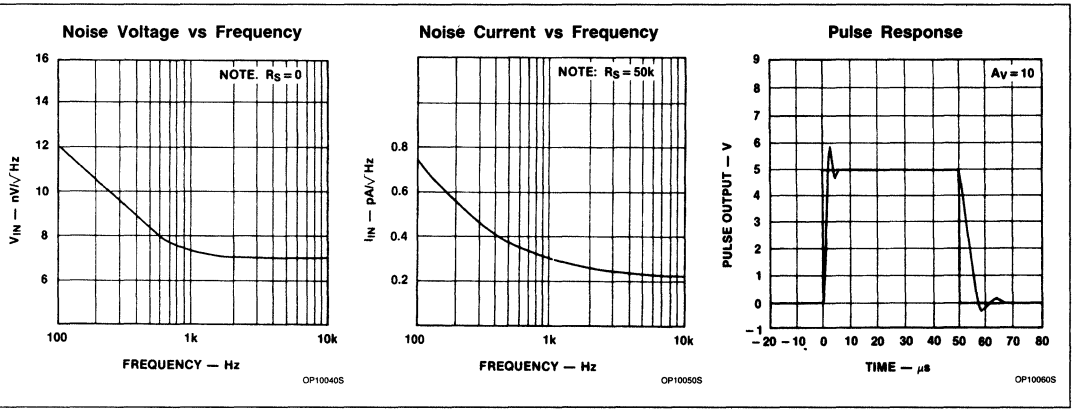
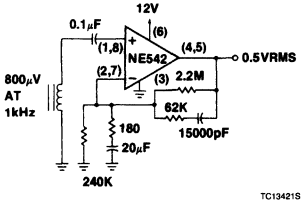
Dual Low-Noise Preamplifier NE542

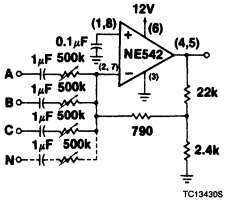
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



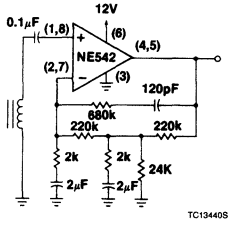
TYPICAL APPLICATIONS



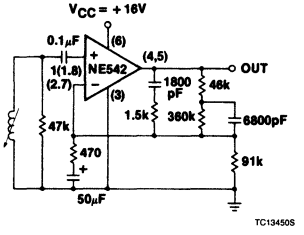
Typical Tape Playback Amplifier



Audio Mixer



Two-Pole Fast Turn-On NAB Tape Preamp



RIAA Magnetic Phono Preamp

NOTE:
All resistor values are typical and in ohms

AN190
Applications of Low Noise Stereo Amplifiers: NE542

Application Note

Linear Products

Introduction

Stereo preamplifiers have come into greater and greater demand with the increased usage of tape recorders. With stereophonic recording systems, the need increased to have multiple devices in the same package to insure greater thermal tracking and packing density, without sacrificing performance.

The NE542 qualifies as a low noise dual preamplifier. The NE542 is an 8-pin dual in-line device.

This device has greater than 100dB open-loop gain and (15 – 20) MHz gain bandwidth product. In selecting the proper "low noise" preamplifier, several factors must be considered.

1. Frequency shaping characteristic required.
2. Closed-loop response with respect to a system reference level.
3. Response of the record/playback head.
4. System distortion requirements.
5. Response of the tape used.

The following will deal with Items 1, 2, and 4.

When approaching the design criteria of Item 2, the designer should be concerned with the open-loop device characteristics. These characteristics will aid in determining the maximum boost available, knowing that a specific loop gain (open-loop gain minus closed-loop gain) will be necessary to keep the system distortion low and maintain the output impedance of the "low noise" preamplifier constant over the required operating frequency range.

RIAA standards call for a maximum recording velocity of 21cm/sec for stereo discs. This worst-case velocity describes a limit for the preamplifier gain because the input signal at this velocity is maximum.

NAB TAPE EQUALIZATION

Recording and playback characteristics of magnetic tape and record/playback heads are not flat but exhibit a loss at high frequencies and a boost at lower frequencies. To obtain an overall flat frequency response and improved signal-to-noise ratio, the audio signals are equalized by boosting the higher frequencies in amplitude before recording. Playback amplifiers must exhibit bass boost to remove the effects of pre-emphasis for an overall flat response.

Known as the NAB equalization curve, the standard deemphasis employs attenuation from the turnover frequency of 50Hz to the turnover frequency of 3180Hz for 7.5ips recording. The slower recording speed of 3.75ips employs turnover frequencies of 50Hz and 1326Hz. These curves are shown in Figure 1. A reference level of 800μV head sensitivity at 1kHz is also used by the NAB.

STEREO PREAMPLIFICATION

The voltage level appearing at the output of tape playback heads and some phono cartridges are too small to be useful without a large amount of low noise preamplification. In addition to providing low noise amplification, the preamplifier should possess enough open-loop gain so that the RIAA and NAB equalization curves can be produced in the feedback networks of the amplifier. The following paragraphs describe the characteristics and applications of the 542. This device provides a matched pair of amplifiers which have been specifically designed to minimize amplifier noise and maximize signal-to-noise ratio.

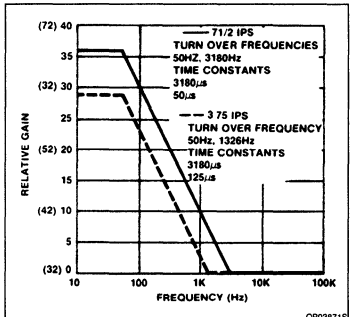


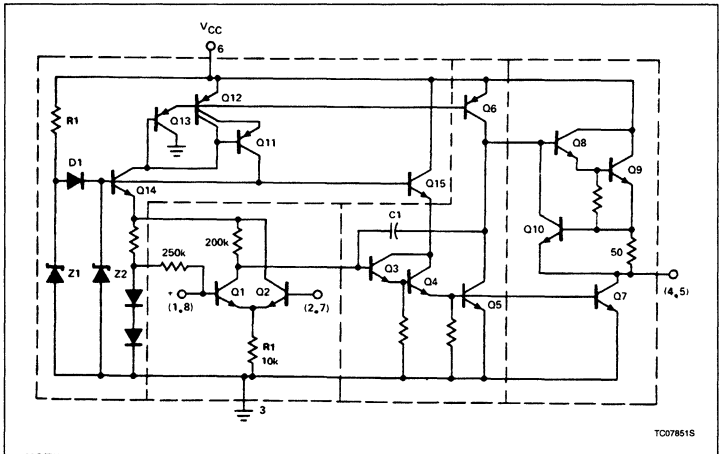
Figure 1. Tape Equalization Curves

NE542 DEVICE DESCRIPTION

The NE542 is a dual low noise amplifier with 104dB open-loop gain produced by two stages of voltage gain followed by one stage of current gain.

In the design of low noise devices, special attention must be focused on the input stage. If differential topography is used, the stage should be designed so that one of the differential transistors is turned off. This reduces the noise contribution by a factor of 1.4 since only one transistor is producing noise. Current sources and mirrors cannot be used for biasing loads because active elements will contribute more noise.

Implementing these observations, the first gain stage of the NE542 is pictured with the complete schematic in Figure 2.



NOTE:
All resistor values are in Ω

Figure 2. Equivalent Schematic NE542

Applications of Low Noise Stereo Amplifiers: NE542 AN190

Although the differential input configuration degrades the noise performance slightly, using differential inputs has the advantage of higher input impedance, allowing smaller capacitors and larger resistors to be used to achieve the RIAA and NAB curves.

The second stage is a common-emitter amplifier (Q_5) with a current source load (Q_6). The Darlington emitter-follower $Q_3 - Q_4$ provides level shifting and current gain to the common-emitter stage (Q_5) and the output current sink (Q_7). The voltage gain of the second stage is approximately 2000, making the total gain of the amplifier typically 160,000 in the differential input configuration

The preamplifier is internally-compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed-loop gain of 10.

BIASING

The non-inverting input has been internally-biased from a 1 4V internal voltage source Following the zero differential rule of amplifiers, the output voltage will be set by the resistor feedback network (R4 and R5) of Figure 3.

The base of Q2 requires 0.5μA bias current. Hence R5 should pass 5μA minimum for stability, for an output DC voltage of $\frac{V_{CC}}{2}$ the values of R4 and R5 are:

$$R5 = \frac{2V_{BE}}{10\ I_B} = 240k\Omega \text{ Max.} \quad (1)$$

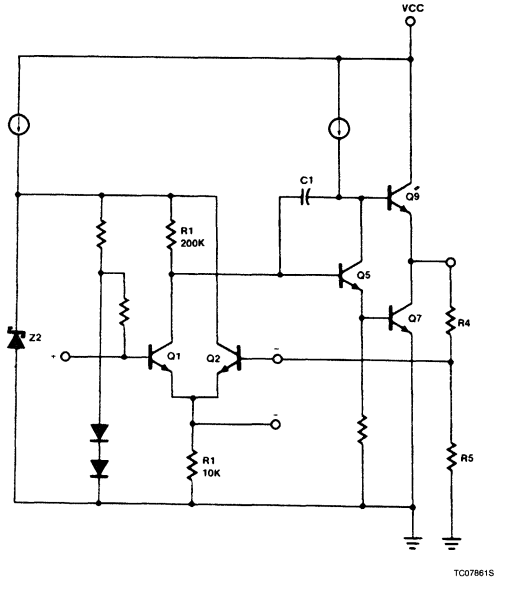
$$R4 = \left(\frac{V_{CC}}{28-1} \right) \times R5 \quad (2)$$

DC amplifier gain is defined by the ratio of R4 and R5. Open-loop AC gain can be regained by adding a shunt capacitor across R5. The low frequency 3dB corner is then defined by the capacitor-resistor break point.

NAB Tape Preamplifier

Design of a preamplifier begins by determining the gain and output signal amplitudes in reference to the standard 800μV input signal level. For the following design example, we will use the 542 to achieve a 100mV output level at 1kHz following the 7.5Ips NAB equalization curve. The graph of Figure 1 has been calibrated both in absolute gain for this example and relative gain for general use.

From the given parameters, the closed-loop gain becomes 32dB at the highest frequency of interest. The NAB response is achieved by adding frequency-selective AC feedback as depicted by Figure 4. Resistors R4 and R5 select the DC gain as defined by Equations 1 and 2. Placing a value of 200k upon R5, Equation 2 yields a value of 680kΩ.



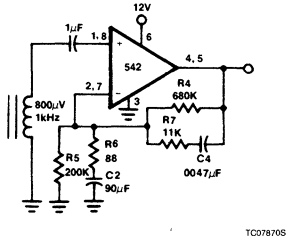
NOTE:
All resistor values are in Ω

Figure 3. Differential Input Biasing NE542

The lower corner frequency is determined next by the reactance of C4 and R4 such that:

$$f_1 = \frac{0.159}{C4\ R4} \quad (3)$$

Solving for C4 yields a value of 0 0047μF.



NOTE:
All resistor values are in Ω

Figure 4. NAB Response Amplifier

The upper corner frequency, f_2, is similarly fixed by the reactance of C4 and R7.

$$f_2 = \frac{0.159}{C4\ R7} \quad (4)$$

Then solving Equation 4 for R7 defines a value of 11kΩ.

Midband gain is now fixed by the relationship.

$$A = \frac{R6 + R7}{R6} \quad (5)$$

Solving for the 1kHz gain of 42dB using 11k for R7 yields a value of 88Ω for R6. The final calculation of the low frequency cut-off of the preamp determines the size of C2.

$$C2 = \frac{0.159}{f_{CUTOFF}\,R6} \quad (6)$$

Typical Applications

In addition to the previous detailed design examples, the following general amplifier configurations (see Figures 5 through 8) are presented. The choice of design and the device used is a function of the desired complexity and overall performance.

Applications of Low Noise Stereo Amplifiers: NE542 AN190

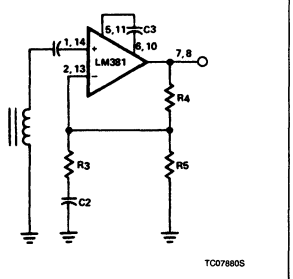


Figure 5. Flat Response Tape Amplifier

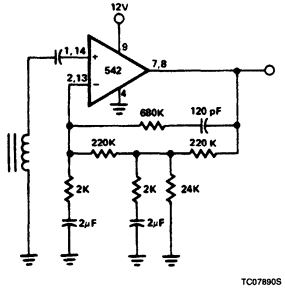
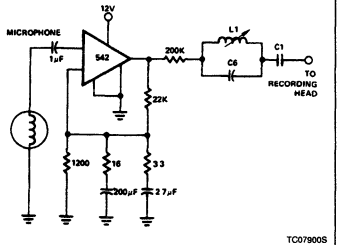


Figure 6. Two-Pole Fast Turn-On NAB Type Preamp



NOTE:
All resistor values are in Ω

Figure 7. Typical NAB Record Preamplifier

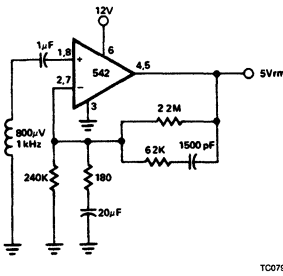


Figure 8. Typical Tape Playback Amplifier

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Signetics

TDA1029
Stereo Audio Switch

Product Specification

Linear Products

DESCRIPTION

The TDA1029 is a dual operational amplifier (connected as an impedance converter); each amplifier has four mutually-switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in AF amplifiers.

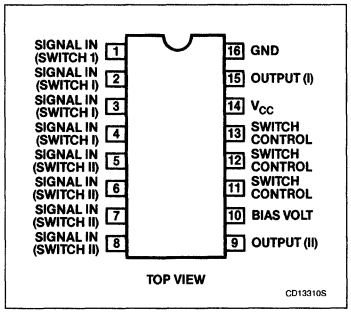
FEATURES

- **Four input source/channel**
- **Clamp diode input protected**
- **Two channel signal-source switch**

APPLICATIONS

- **Audio amplifiers**
- **Preamplifiers**
- **Graphic equalizers**

PIN CONFIGURATION



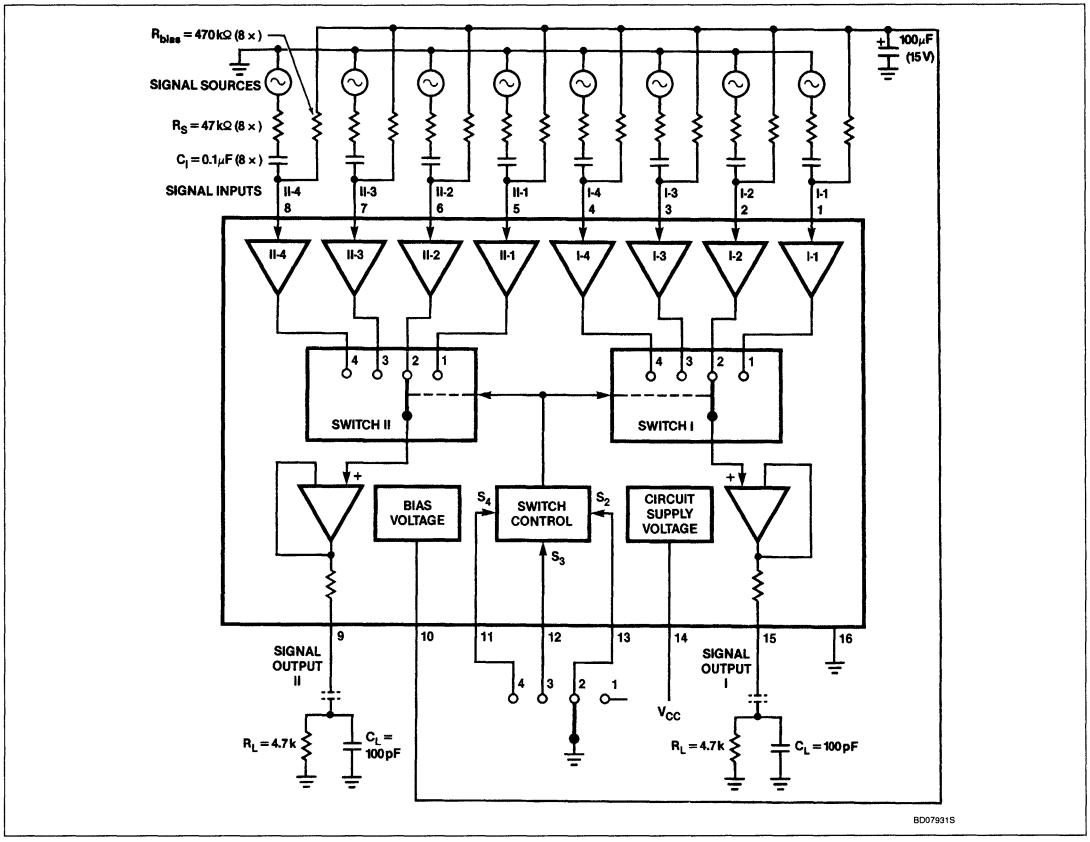
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−30°C to +80°C	TDA1029N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 14)	23	V
V_I $-V_I$	Input voltage (Pins 1 to 8)	V_{CC} 0.5	V
V_S	Switch control voltage (Pins 11, 12 and 13)	0 to 23	V
$\pm I_I$	Input current	20	mA
$-I_S$	Switch control current	50	mA
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C

BLOCK DIAGRAM



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DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 20V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_{14}	Current consumption without load; $I_9 = I_{15} = 0$	2	3.5	5	mA
V_{CC}	Supply voltage range (Pin 14)	6		23	V
Signal inputs					
V_{IO}	Input offset voltage of switched-on inputs $R_S \leqslant 1k\Omega$		2	10	mV
I_{IO}	Input offset current of switched-on inputs		20	200	nA
I_{IO}	Input offset current of a switched-on input with respect to a non-switched-on input of a channel		20	200	nA
I_{BIAS}	Input bias current independent of switch position		250	950	nA
C	Capacitance between adjacent inputs		0.5		pF
V_I	DC input voltage range	3		19	V
SVRR	Supply voltage rejection ratio; $R_S \leqslant 10k\Omega$		100		μV/V
$V_{N(RMS)}$	Equivalent input noise voltage $R_S = 0$, f = 20Hz to 20kHz (RMS value)		3.5		μV
$I_{N(RMS)}$	Equivalent input noise current f = 20Hz to 20kHz (RMS value)		0.05		nA
α	Crosstalk between a switched-on input and a non-switched-on input; measured at the outputat $R_S = 1k\Omega$; f = 1kHz		100		dB
Signal amplifier					
A_V	Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$		1		dB
A_I	Current gain of a switched-on amplifier		10^5		
Signal outputs					
R_O	Output resistance (Pins 9 and 15)		400		Ω
$\pm I_9$; $\pm I_{15}$	Output current capability at V_{CC} = 6 to 23V		5		mA
f	Frequency limit of the output voltage $V_{I(P-P)} = 1V$; $R_S = 1k\Omega$; $R_L = 10M\Omega$; $C_L = 10pF$		1.3		MHz
SR	Slew rate (unity gain); $\Delta V_{9-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$ $R_L = 10M\Omega$; $C_L = 10pF$		2		V/μs
Bias voltage					
V_{10-16}	DC output voltage[1]	10.2	11	11.8	V
R_{10-16}	Output resistance		8.2		kΩ
Control inputs (Pins 11, 12 and 13)					
V_{SH} V_{SL}	Required voltage HIGH[2] LOW	3.3		 2.1	V V
I_{SH} $-I_{SL}$	Input current HIGH (leakage current) LOW (control current)	1 250			μA μA

NOTES:
1. V_{10-16} is typically $0.5 \cdot V_{14-16} + 1.5 \cdot V_{BE}$.
2. Or control inputs open ($R_{11, 12, 13-16} > 33M\Omega$)

SWITCH CONTROL

SWITCHED-ON INPUTS	INTERCONNECTED PINS	CONTROL VOLTAGES		
		V_{11-16}	V_{12-16}	V_{13-16}
I-1, II-1	1 – 15, 5 – 9	H	H	H
I-2, II-2	2 – 15, 6 – 9	H	H	L
I-3, II-3	3 – 15, 7 – 9	H	L	H
I-4, II-4	4 – 15, 8 – 9	L	H	H
I-4, II-4	4 – 15, 8 – 9	L	L	H
I-4, II-4	4 – 15, 8 – 9	L	H	L
I-4, II-4	4 – 15, 8 – 9	L	L	L
I-3, II-3	3 – 15, 7 – 9	H	L	L

NOTE:
In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time In that case safe switching-through is obtained at $V_{SL} \leqslant 1.5V$.

APPLICATION INFORMATION

$V_{CC} = 20V$; $T_A = 25°C$; $R_S = 47k\Omega$; $C_I = 0.1\mu F$; $R_{BIAS} = 470k\Omega$; $R_L = 4.7k\Omega$; $C_L = 100pF$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
A_V	Voltage gain		–15		dB
ΔV_{9-16}; ΔV_{15-16}	Output voltage variation when switching the inputs		10	100	mV
d_{TOT} d_{TOT} d_{TOT}	Total harmonic distortion over most of signal range (see Figure 4) $V_I = 5V$, f = 1kHz $V_I = 5V$, f = 20Hz to 20kHz		 0.01 0.02 0.03		 % % %
$V_{O(RMS)}$	Output signal handling $d_{TOT} = 0.1\%$; f = 1kHz (RMS value)		5.0	5.3	V
$V_{N(RMS)}$	Noise output voltage (unweighted) f = 20Hz to 20kHz (RMS value)		5		μV
V_N	Noise output voltage (weighted) f = 20Hz to 20kHz (in accordance with DIN 45405)		12		μV
ΔV_{9-16}; ΔV_{15-16}	Amplitude response[1] $V_I = 5V$; f = 20Hz to 20kHz, $C_I = 0.22\mu F$			0.1	dB
α	Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1kHz[2]		75		dB
α	Crosstalk between switched-on inputs and the outputs of the other channels[2]		90		dB

NOTES:
1. The lower cut-off frequency depends on values of R_{BIAS} and C_I
2 Depends on external circuitry and R_S The value will be fixed mostly by capacitive crosstalk of the external components

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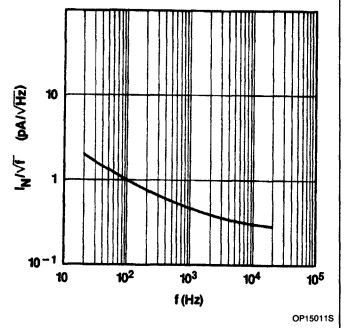


Figure 1. Equivalent Input Noise Current

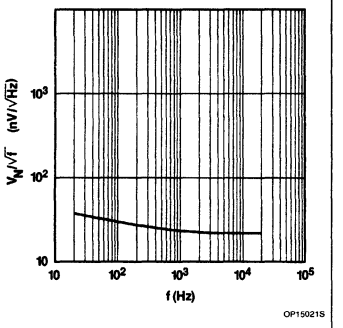
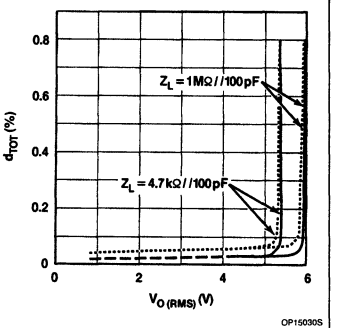


Figure 2. Equivalent Input Noise Voltage



NOTES:
——— f = 1kHz
····· f = 20kHz

Figure 3. Total Harmonic Distortion as a Function of RMS Output Voltage

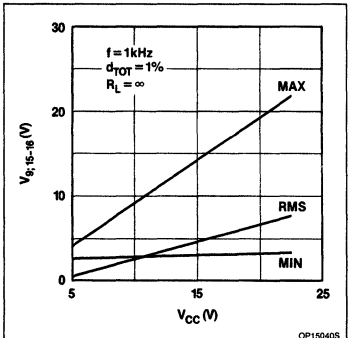
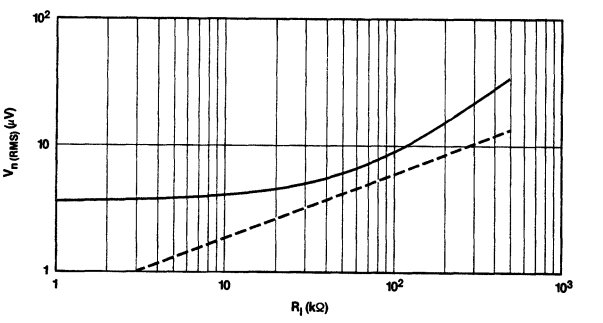


Figure 4. Output Voltage as a Function of Supply Voltage



NOTES:
A_V = 1dB, f = 20Hz to 20kHz
——— V_N (output)
– – – – V_N (R_S)

Figure 5. Noise Output Voltage as a Function of Input Resistance

Input Protection Circuit and Indication

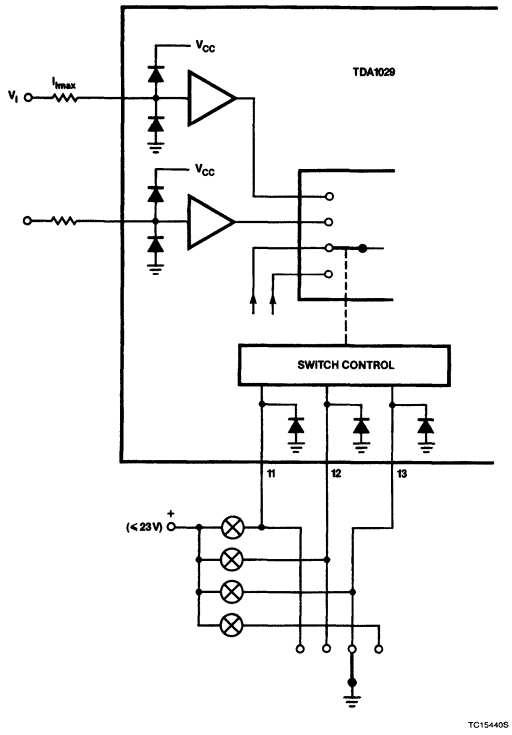


Figure 6. Circuit Diagram Showing Input Protection and Indication

Unused Signal Inputs

Any unused inputs must be connected to a DC (bias) voltage, which is within the DC input voltage range; e.g., unused inputs can be connected directly to Pin 10

Circuits With Standby Operation

The control inputs (Pins 11, 12 and 13) are high-ohmic at $V_{SH} \leq 20V (I_{SH} \leq 1\mu A$, as well as when the supply voltage (Pin 14) is switched off

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Stereo Audio Switch TDA1029

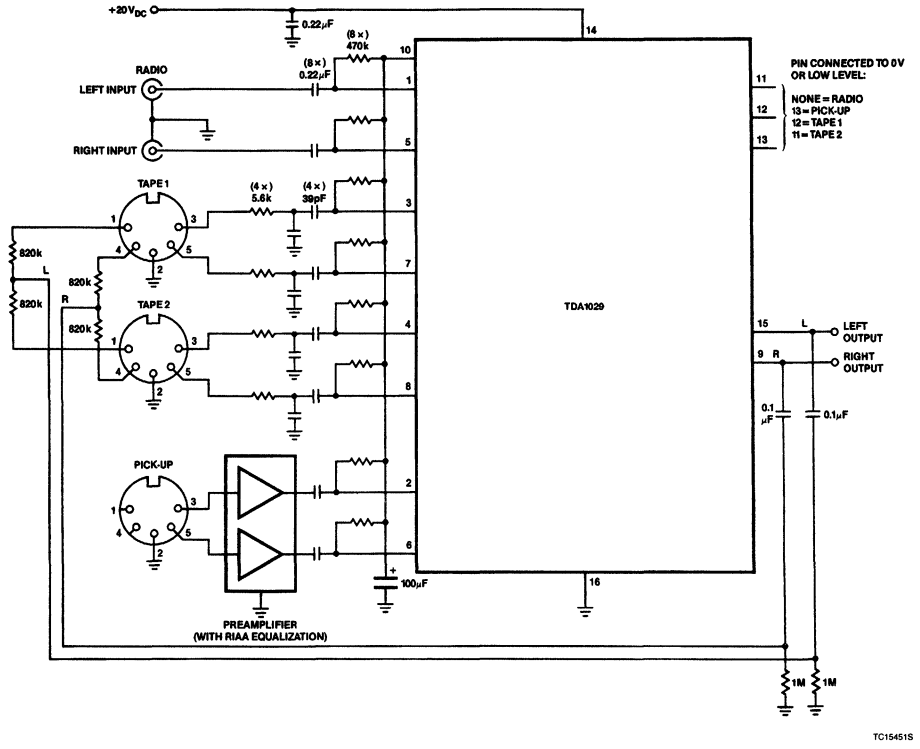


Figure 7. TDA1029 Connected as a 4-Input Stereo Source Selector

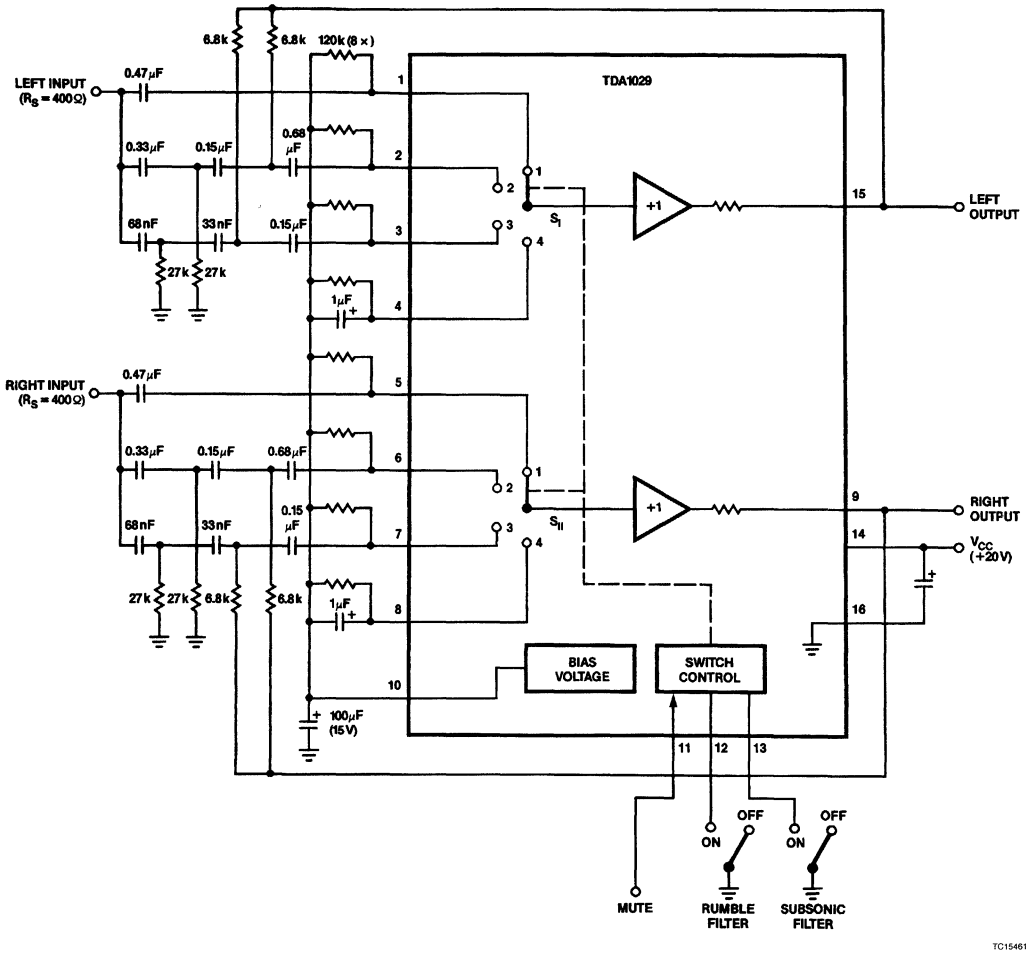


Figure 8. TDA1029 Connected as a Third-Order Active High-Pass Filter With Butterworth Response and Component Values Chosen According to the Method Proposed by Fjällbrant. It is a Four-Function Circuit Which can Select Mute, Rumble Filter, Subsonic Filter and Linear Response

SWITCH CONTROL

FUNCTION	V_{11-16}	V_{12-16}	V_{13-16}
Linear	H	H	H
Subsonic filter 'on'	H	H	L
Rumble filter 'on'	H	L	X
Mute 'on'	L	X	X

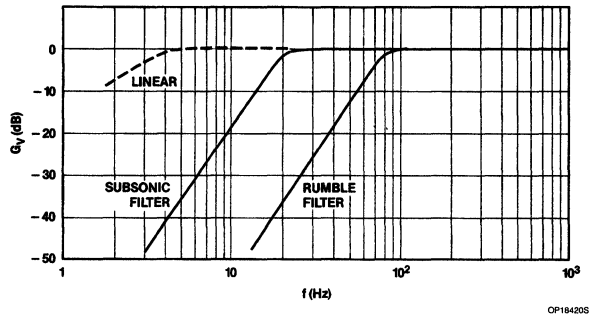


Figure 9. Frequency Response Curves for the Circuit of Figure 8

Signetics

TDA1074A
DC-Controlled Dual Potentiometer Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual DC control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the DC control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a DC control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can perform bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

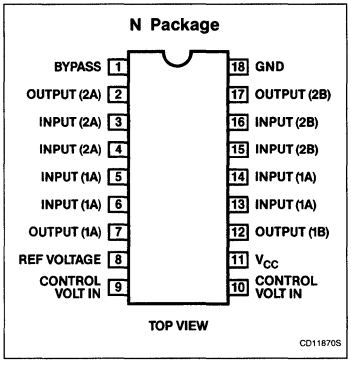
FEATURES

- **High impedance inputs to both 'ends' of each electronic potentiometer**
- **Ganged potentiometers track within 0.5dB**
- **Electronic rejection of supply ripple**
- **Internally-generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0V level**
- **The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption**
- **The operational amplifier outputs are current limited to provide output short-circuit protection**
- **Although designed to operate from a 20V supply (giving a maximum input and output signal level of 6V), the TDA1074A can work from a supply as low as 7.5V with reduced input and output signal levels**

APPLICATIONS

- **Volume control**
- **Tone control**
- **Low level fader**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102CS)	−30°C to +80°C	TDA1074AN

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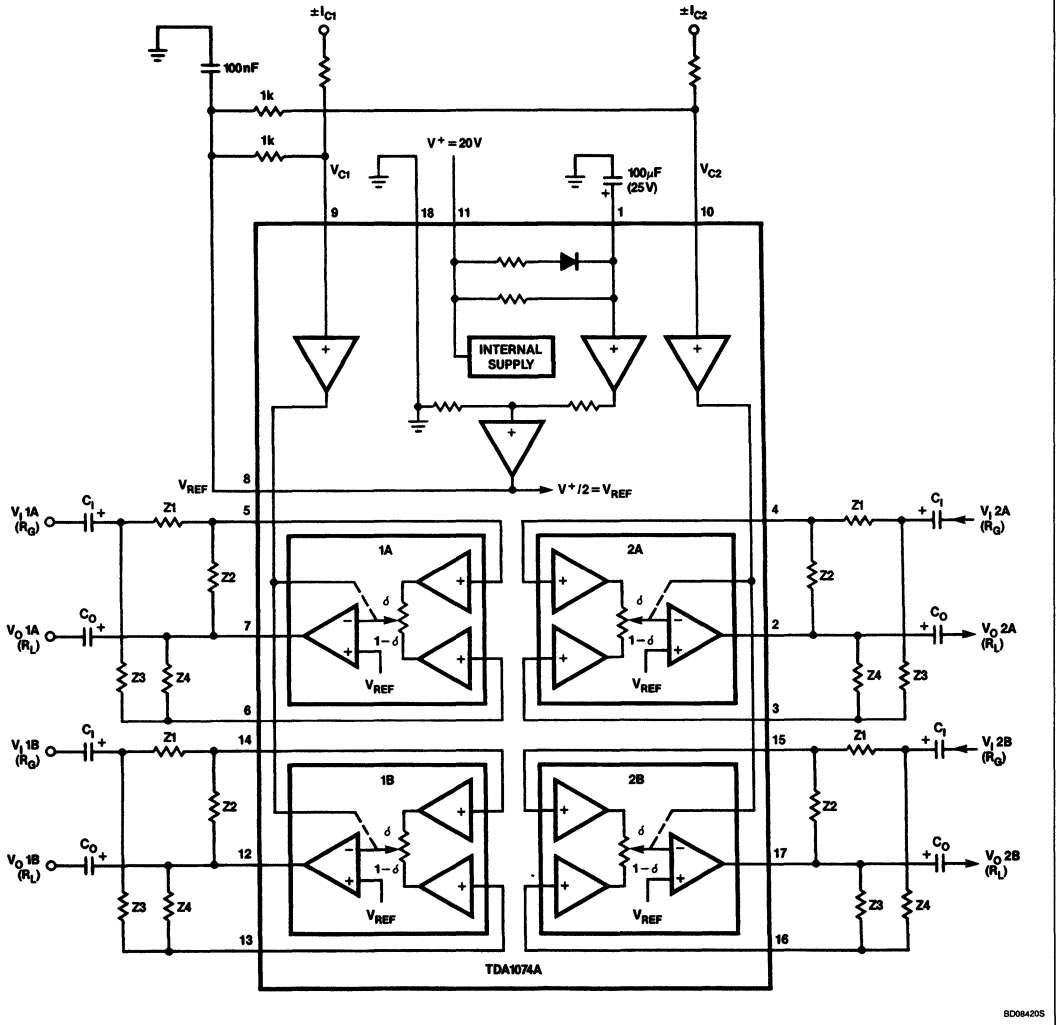
DC-Controlled Dual Potentiometer Circuit | TDA1074A

BLOCK DIAGRAM



NOTES:
I_{C1} (at Pin 9) and I_{C2} (at Pin 10) are control input currents, V_{C1} (at Pin 9) and V_{C2} (at Pin 10) are control input voltages with respect to $V_{REF} = V_{CC/2}$ at Pin 8; Z1 = Z2 = Z3 = Z4 = 22kΩ, the input generator resistance $R_G = 60\Omega$, the output load resistance $R_L = 4.7k\Omega$, the coupling capacitors at the inputs and outputs are $C_I = 2.2\mu F$ and $C_O = 10\mu F$, respectively

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 11)	23	V
	Control voltages (Pins 9 and 10)	1	V
V_I	Input voltage ranges (with respect to Pin 18) at Pins 3, 4, 5, 6, 13, 14, 15, 16	0 to V_{CC}	V
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C
θ_{CRA}	Thermal resistance from crystal to ambient	80	°C/W

APPLICATION INFORMATION

Treble and Bass Control Circuit

V_{CC} = 20V; T_A = 25°C; measured in Figure 1; R_G = 60Ω; R_L > 4.7kΩ; C_L < 30pF; f = 1kHz; with a linear frequency response (V_{C1} = V_{C2} = 0V), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_{CC}	Supply current (without load)	14	22	30	mA
f	Frequency response (−1dB) V_{C1} = V_{C2} = 0V	10		20,000	Hz
A_V*	Voltage gain at linear frequency response (V_{C1} = V_{C2} = 0V)		0		dB
ΔA_V*	Gain variation at f = 1kHz at maximum bass/treble boost or cut at $\pm V_{C1}$ = $\pm V_{C2}$ = 120mV		±1		dB
	Bass boost at 40Hz (ref. 1kHz) V_{C2} = 120mV		17.5		dB
	Bass cut at 40Hz (ref. 1kHz) $-V_{C2}$ = 120mV		17.5		dB
	Treble boost at 16kHz (ref. 1kHz) V_{C1} = 120mV		16		dB
	Treble cut at 16kHz (ref. 1kHz) $-V_{C1}$ = 120mV		16		dB
	Total harmonic distortion at $V_{O(RMS)}$ = 300mV				
THD	f = 1kHz (measured selectively)		0.002		%
THD	f = 20Hz to 20kHz		0.005		%
	at $V_{O(RMS)}$ = 5V				
THD	f = 1kHz		0 015	0.1	%
THD	f = 20Hz to 20kHz		0.05	0.1	%
V_I, $V_{O(RMS)}$	Signal level at THD = 0.7% (input and output)	5.5	6.2		V
BW	Power bandwidth at reference level $V_{O(RMS)}$ = 5V (−3dB); THD = 0.1%		40		kHz
	Output noise voltages				
$V_{NO(RMS)}$	(signal plus noise (RMS value); f = 20Hz to 20kHz		75		μV
$V_{NO(M)}$	noise (peak value); weighted to DIN 45405; CCITT filter		160	230	μV
	Crosstalk attenuation (stereo)				
αCT	f = 1kHz		86		dB
αCT	f = 20Hz to 20kHz		80		dB
	Control voltage cross-talk to the outputs at f = 1kHz;				
−αCT	$V_{C1(RMS)}$ = $V_{C2(RMS)}$ = 1mV		20		dB
α100	Ripple rejection at f = 100Hz; $V_{CC(RMS)}$ < 200mV		46		dB

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DC-Controlled Dual Potentiometer Circuit TDA1074A

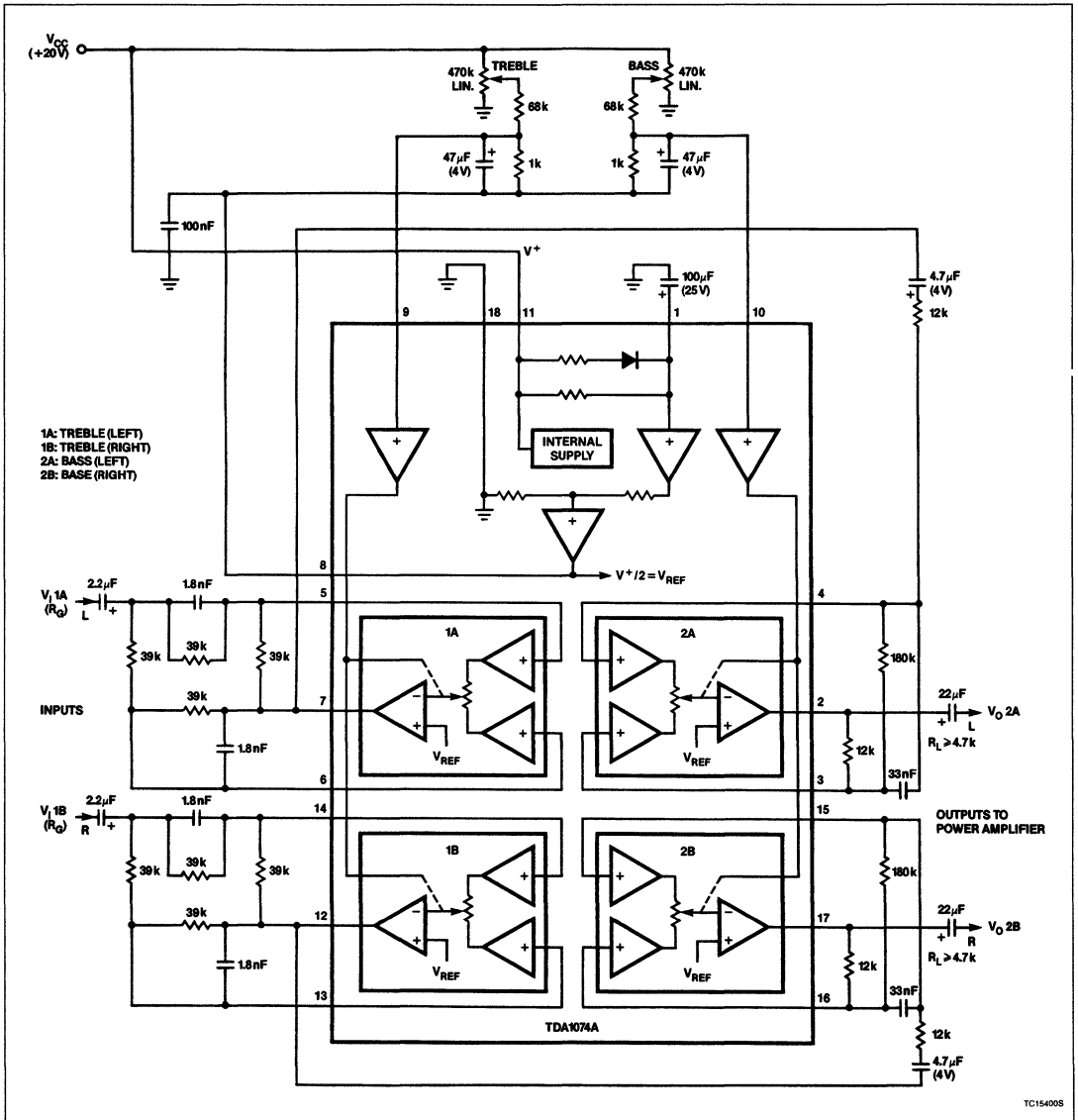


Figure 1. Application Diagram for Treble and Bass Control

APPLICATION INFORMATION (Continued)

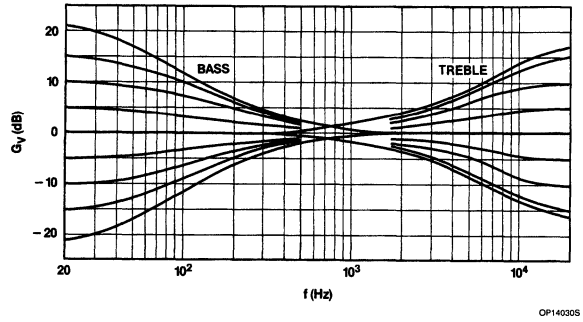


Figure 2. Frequency Response Curves; Voltage Gain (Treble and Bass) as a Function of Frequency

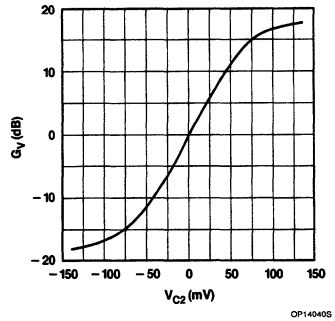


Figure 3. Control Curve; Voltage Gain (Bass) as a Function of the Control Voltage (V_{C2}); f = 40Hz

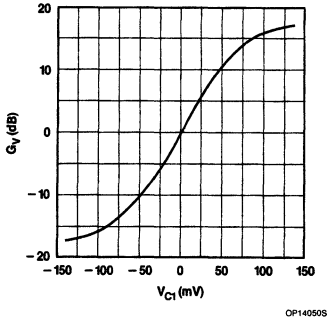
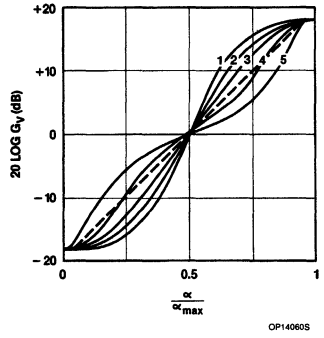


Figure 4. Control Curve; Voltage Gain (Treble) as a Function of the Control Voltage (V_{C1}); f = 16kHz



Curve No.	Value of R
1	10kΩ
2	100kΩ
3	220kΩ
4	470kΩ
5	1MΩ

Figure 5. Voltage Gain ($A_V = V_O/V_I$) Control Curves as a Function of the Angle of Rotation (α) of a Linear Potentiometer (R); (for Curve Numbers see Table Above); f = 40Hz to 16kHz

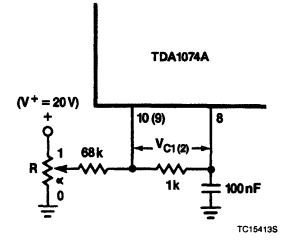


Figure 6. Circuit Diagram for Measuring Curves in Figure 5

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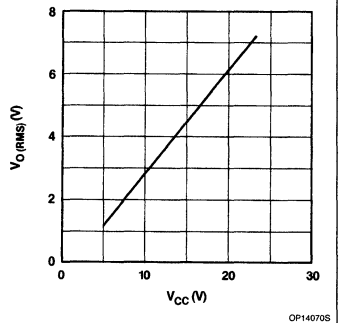
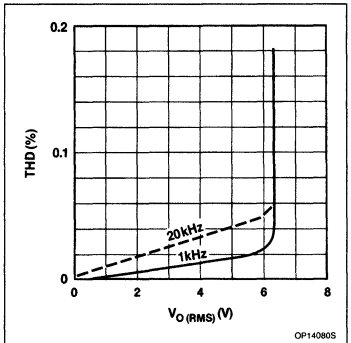
APPLICATION INFORMATION (Continued)



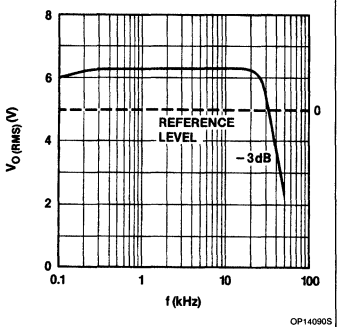
NOTES:
THD = 0 7%,
f = 1kHz, $V_{C1} = V_{C2} = 0V$

Figure 7. Output Signal Level as a Function of V_{CC}



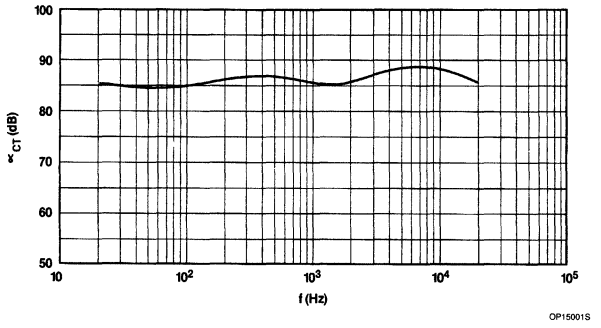
NOTES:
——— f = 1kHz
-------- f = 20kHz
V_{CC} = 20V, R_L = 4 7kΩ, $V_{C1} = V_{C2}$ = 0V
(Linear A_{VTOT} = 1)

Figure 8. Total Harmonic Distortions as a Function of the Output Level



NOTES:
Reference Level is 5V (RMS)

Figure 9. Power Bandwidth at THD = 0.1%



NOTE:
Linear treble/bass setting ($V_{C1} = V_{C2}$ = 0V), V_I = 5V, R_G = 60Ω, R_L = 4 7kΩ

Figure 10. Crosstalk as a Function of Frequency

Application Recommendations

1. If one or more electronic potentiometers in an IC are not used, the following is recommended:

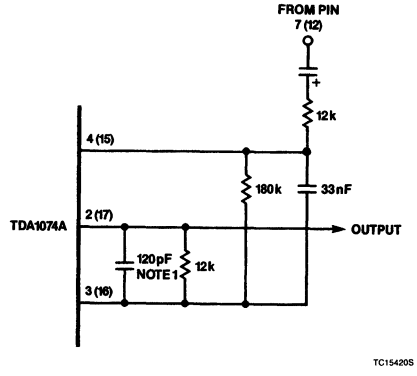
a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g., Pins 3 and 4 to Pin 2.

b. Unused control voltage inputs should be connected directly to Pin 8 (V_{REF}).

2. Where more than one TDA1074A IC are used in an application, Pins 1 can be connected together; however, Pins 8 (V_{REF}) may not be connected together directly.

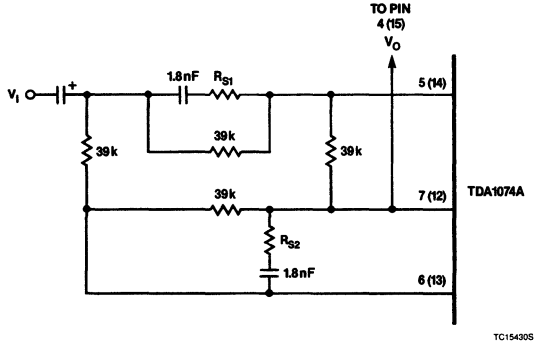
3. Additional circuitry for limiting the frequency response in the ultrasonic range is shown in Figure 11.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range is shown in Figure 12.



NOTE:
1 f_{-3db} = 110kHz at linear setting

Figure 11. Circuit Diagram for Frequency Response Limiting



NOTES:
For $R_{S1} = R_{S2} = 3.3k\Omega$, $f_{-3dB} \cong 1MHz$ at linear setting
For $R_{S1} = R_{S2} = 0\Omega$; $f_{-3dB} \cong 100kHz$ at linear setting

Figure 12. Circuit Diagram for Limiting Gain of Treble Control Circuit

7

Signetics

TDA1524A
Stereo Audio Control

Product Specification

Linear Products

DESCRIPTION

The device is designed as an active stereo tone/volume control for car radios, TV receivers and audio equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers. The bass and treble responses are defined by a single capacitor per control per channel.

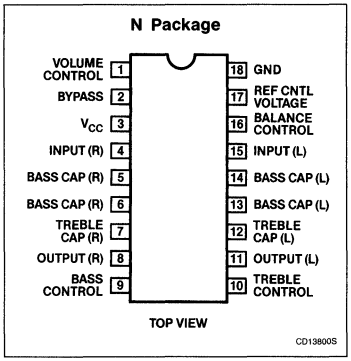
FEATURES

- **Few external components necessary**
- **Low noise due to internal gain**
- **Bass emphasis can be increased by a double-pole low-pass filter**
- **Wide power supply voltage range**

APPLICATIONS

- **Hi-Fi radio**
- **Auto radio**
- **TV**
- **Audio systems**

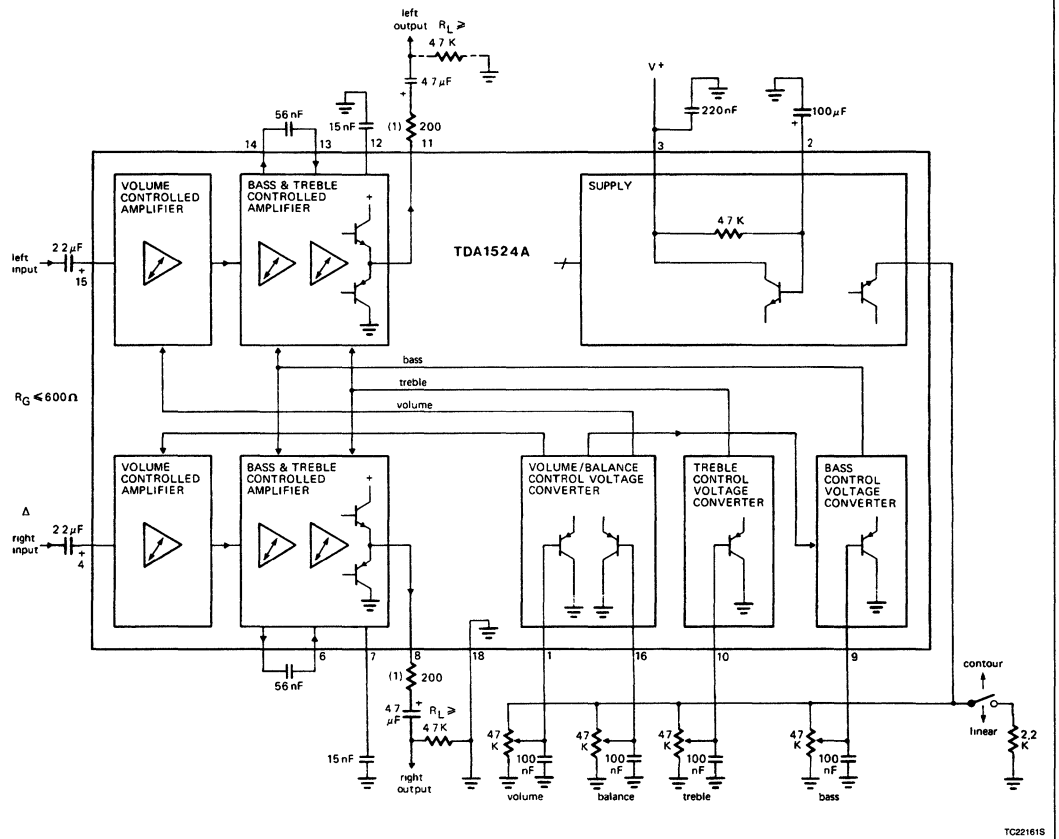
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDERING CODE
18-Pin Plastic DIP (SOT-102HE)	−30°C to +80°C	TDA1524AN

BLOCK DIAGRAM AND APPLICATION CIRCUIT WITH SINGLE-POLE FILTER



NOTE:
Series resistor is recommended in the event of the capacitive loads exceeding 200 pF

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{3-18}$	Supply voltage	20	V
P_{TOT}	Total power dissipation	1200	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−30 to +80	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V; T_A = 25°C, measured in Block Diagram; $R_G \leq 600\Omega$; $R_L \geq 4.7k\Omega$; $C_L \leq 200pF$, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 3)					
$V_{CC} = V_{3-18}$	Supply voltage	7.5		16.5	V
	Supply current				
$I_{CC} = I_3$	at V_{CC} = 8.5V	19	27	36	mA
$I_{CC} = I_3$	at V_{CC} = 12V	25	35	45	mA
$I_{CC} = I_3$	at V_{CC} = 15V	30	43	56	mA
	DC input levels (Pins 4 and 15)				
$V_{4, 15-18}$	at V_{CC} = 8 5V	3.8	4.25	4.7	V
$V_{4, 15-18}$	at V_{CC} = 12V	5.3	5.9	6.6	V
$V_{4, 15-18}$	at V_{CC} = 15V	6.5	7.3	8 2	V
	DC output levels (Pins 8 and 11) under all control voltage conditions with DC feedback (Figure 2)				
$V_{8, 11-18}$	at V_{CC} = 8 5V	3.3	4.25	5.2	V
$V_{8, 11-18}$	at V_{CC} = 12V	4.6	6.0	7.4	V
$V_{8, 11-18}$	at V_{CC} = 15V	5.7	7.5	9.3	V
Pin 17					
V_{17-18}	Internal potentiometer supply voltage at V_{CC} = 8.5V	3.5	3.75	4.0	V
	Contour on/off switch (control by I_{17})				
$-I_{17}$	contour (switch open)			0.5	mA
$-I_{17}$	linear (switch open)	1.5		10	mA
	Application without internal potentiometer supply voltage at $V_{CC} \geq 10.8V$ (contour cannot be switched off)				
V_{17-18}	Voltage range forced to Pin 17	4.5		$V_{CC}/2 - V_{BE}$	V
	DC control voltage range for volume, bass, treble and balance (Pins 1, 9, 10 and 16, respectively)				
$V_{1, 9, 10, 16}$	at V_{17-18} = 5V	1 0		4.25	V
$V_{1, 9, 10, 16}$	using internal supply	0.25		3.8	V
$-I_{1, 9, 10, 16}$	Input current of control inputs (Pins 1, 9, 10 and 16)			5	μA

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{3-18} = 8.5V$; $T_A = 25°C$; measured in Block Diagram; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leq 600\Omega$; $R_L \geq 4.7k\Omega$; $C_L \leq 200pF$; f = 1kHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Control range					
$A_{V\ MAX}$	Maximum gain of volume (Figure 4)	20.5	21.5	23	dB
ΔA_V	Volume control range; $A_{V\ MAX}/A_{V\ MIN}$	90	100		dB
ΔA_V	Balance control range; A_V = 0dB (Figure 5)		−40		dB
ΔA_V	Bass control range at 40Hz (Figure 6)		−19 to +17±3		dB
ΔA_V	Treble control range at 16kHz (Figure 7)		±15±3		dB
	Contour characteristics	see Figures 8 and 9			
Signal inputs, outputs					
$R_{I4,\ 15}$ $R_{I4,\ 15}$	Input resistance; Pins 4 and 15[1] at gain of volume control: A_V = 20dB A_V = −40dB	10	 160		kΩ kΩ
$R_{O8,\ 11}$	Output resistance (Pins 8 and 11)			300	Ω
Signal processing					
PSRR	Power supply ripple rejection at $V_{CC(RMS)} \leq 200$ mV; f = 100Hz; A_V = 0dB	35	50		dB
α_{CS}	Channel separation (250Hz to 10kHz) at A_V = −20 to +21.5dB	46	60		dB
ΔA_V	Spread of volume control with constant control voltage $V_{1-18} = 0.5\ V_{17-18}$			±3	dB
$\Delta A_{V,\ L\text{-}R}$	Gain tolerance between left and right channel $V_{16-18} = V_{1-18} = 0.5\ V_{17-18}$			1.5	dB
ΔA_V	Tracking between channels for A_V = 21.5 to −26dB f = 250Hz to 6.3kHz; balance adjusted at A_V = 10dB			2.5	dB
Signal handling with DC feedback (Figure 2)					
$V_{I(RMS)}$	Input signal handling at V_{CC} = 8.5V; THD = 0.5%; f = 1kHz (RMS value)	1.4			V
$V_{I(RMS)}$	at V_{CC} = 8.5V; THD = 0.7%; f = 1kHz (RMS value)	1.8	2.4		V
$V_{I(RMS)}$	at V_{CC} = 12V; THD = 0.5%; f = 40Hz to 16kHz (RMS value)	1.4			V
$V_{I(RMS)}$	at V_{CC} = 12V; THD = 0.7%; f = 40Hz to 16kHz (RMS value)	2.0	3.2		V
$V_{I(RMS)}$	at V_{CC} = 15V; THD = 0.5%; f = 40Hz to 16kHz (RMS value)	1.4			V
$V_{I(RMS)}$	at V_{CC} = 15V; THD = 0.7%; f = 40Hz to 16kHz (RMS value)	2.0	3.2		V
$V_{O(RMS)}$	Output signal handling[2,3] at V_{CC} = 8.5V; THD = 0.5%; f = 1kHz (RMS value)	1.8	2.0		V
$V_{O(RMS)}$	at V_{CC} = 8.5V; THD = 10%; f = 1kHz (RMS value)		2.2		V

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AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{3-18} = 8.5V$; $T_A = 25°C$; measured in Block Diagram; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leq 600\Omega$; $R_L \geq 4.7k\Omega$; $C_L \leq 200pF$; f = 1kHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_{O(RMS)}$	at V_{CC} = 12V; THD = 0.5%; f = 40Hz to 16kHz (RMS value)	2.5	3.0		V
$V_{O(RMS)}$	at V_{CC} = 15V; THD = 0.5%; f = 40Hz to 16kHz (RMS value)		3.5		V
Noise performance (V_{CC} = 8.5V)					
	Output noise voltage (unweighted; Figure 14) at f = 20Hz to 20kHz (RMS value)				
$V_{NO(RMS)}$	for maximum voltage gain[4]		260		μV
$V_{NO(RMS)}$	for A_V = −3dB[4]		70	140	μV
	Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)				
$V_{NO(M)}$	for maximum voltage gain[4]		890		μV
$V_{NO(M)}$	for maximum emphasis of bass and treble (contour off; A_V = −40dB)		360		μV
Noise performance (V_{CC} = 12V)					
	Output noise voltage (unweighted; Figure 14) at f = 20Hz to 20kHz (RMS value)[5]				
$V_{NO(RMS)}$	for maximum voltage gain[4]		310		μV
$V_{NO(RMS)}$	for A_V = −16dB[4]		100	200	μV
	Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)				
$V_{NO(M)}$	for maximum voltage gain[4]		940		μV
$V_{NO(M)}$	for maximum emphasis of bass and treble (contour off; A_V = −40dB)		400		μV
Noise performance (V_{CC} = 15V)					
	Output noise voltage (unweighted; Figure 14) at f = 20Hz to 20kHz (RMS value)[5]				
$V_{NO(RMS)}$	for maximum voltage gain[4]		350		μV
$V_{NO(RMS)}$	for A_V = −16dB[4]		110	220	μV
	Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)				
$V_{NO(M)}$	for maximum voltage gain[4]		980		μV
$V_{NO(M)}$	for maximum emphasis of bass and treble (contour off, A_V = −40dB)		420		μV

NOTES:

1 Equation for input resistance (see also Figure 3)

$$R_I = \frac{160k\Omega}{1+A_V}, \quad A_{V\,MAX} = 12$$

2 Frequencies below 200Hz and above 5kHz have reduced voltage swing. The reduction at 40Hz and at 16kHz is 30%

3 In the event of bass boosting the output signal handling is reduced The reduction is 1dB for maximum bass boost

4 Linear frequency response

5 For peak values add 4 5dB to RMS values

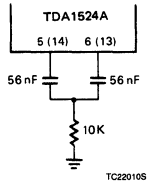


Figure 1. Double-Pole Low-Pass Filter for Improved Bass Boost

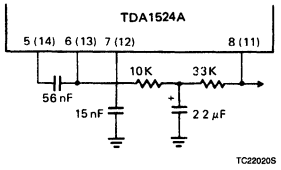


Figure 2. DC Feedback With Filter Network for Improved Signal Handling

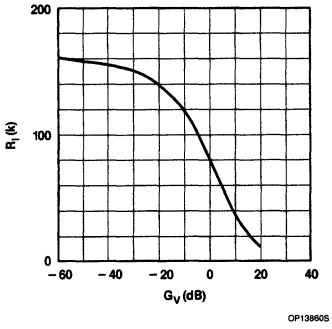
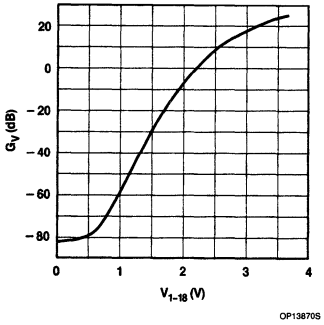
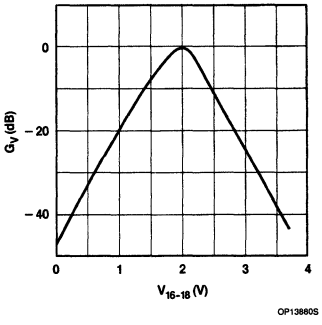


Figure 3. Input Resistance (R_I) as a Function of Gain of Volume Control (A_V)



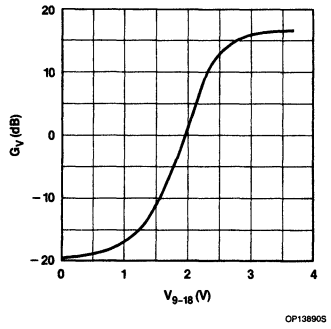
NOTES:
Internal potentiometer supply from Pin 17 used,
V_{CC} = 8.5V, f = 1kHz
See Block Diagram

Figure 4. Volume Control Curve; Voltage Gain (A_V) as a Function of Control Voltage (V_{1-18})



NOTES:
Internal potentiometer supply from Pin 17 used,
V_{CC} = 8.5V
See Block Diagram

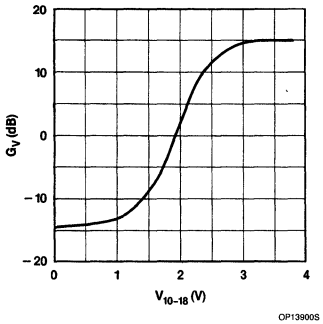
Figure 5. Balance Control Curve; Voltage Gain (A_V) as a Function of Control Voltage (V_{16-18})



NOTES:
With single-pole filter, Internal potentiometer supply from Pin 17 used, V_{CC} = 8.5V, f = 40Hz
See Block Diagram.

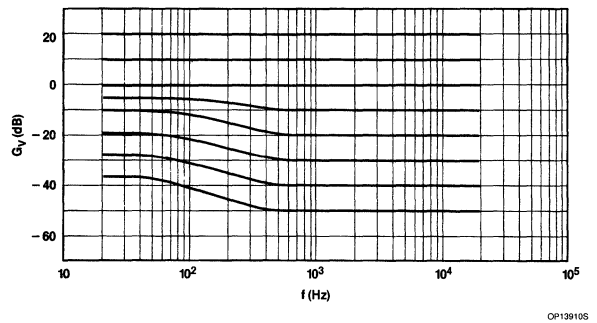
Figure 6. Bass Control Curve; Voltage Gain (A_V) as a Function of Control Voltage (V_{9-18})

7



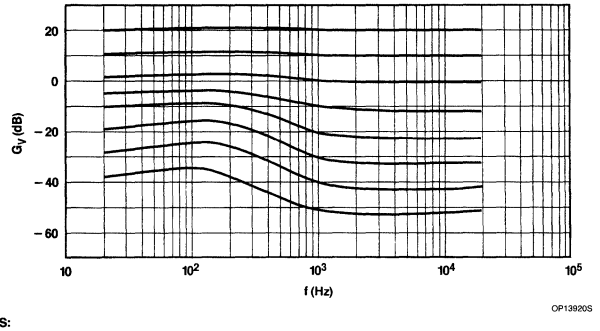
NOTES:
Internal potentiometer supply from Pin 17 used,
V_{CC} = 8.5V, f = 16kHz
See Block Diagram

Figure 7. Treble Control Curve; Voltage Gain (A_V) as a Function of Control Voltage (V_{10-18})



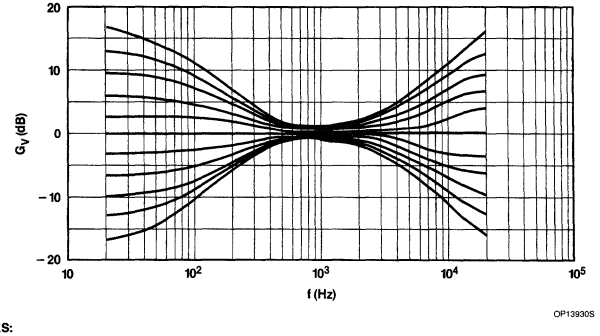
NOTES:
With single-pole filter, V_{CC} = 8.5V
See Block Diagram

Figure 8. Contour Frequency Response Curves; Voltage Gain (A_V) as a Function of Audio Input Frequency



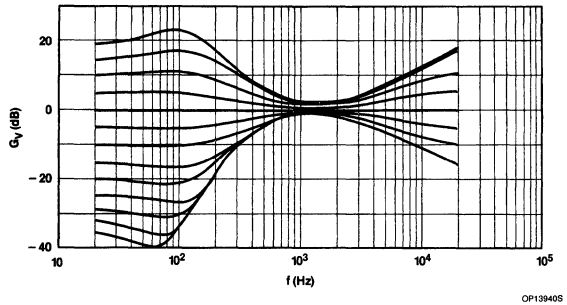
NOTES:
With double-pole filter, V_{CC} = 8.5V
See Block Diagram

Figure 9. Contour Frequency Response Curves; Voltage Gain (A_V) as a Function of Audio Input Frequency



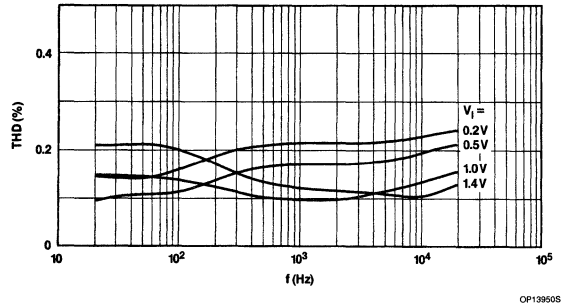
NOTES:
With single-pole filter, V_{CC} = 8.5V
See Block Diagram

Figure 10. Tone Control Frequency Response Curves; Voltage Gain (A_V) as a Function of Audio Input Frequency



NOTES:
With double-pole filter, V_{CC} = 8 5V
See Block Diagram

Figure 11. Tone Control Frequency Response Curves; Voltage Gain (A_V) as a Function of Audio Input Frequency

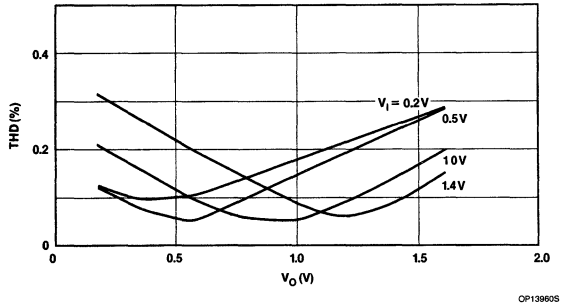


NOTES:
V_{CC} = 8 5V volume control voltage gain at

$A_V = 20 \log \frac{V_O}{V_I} = 0dB$

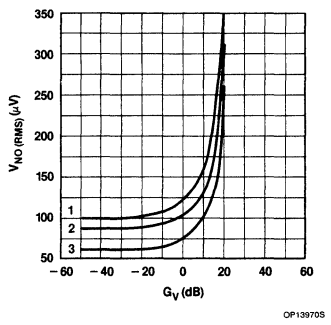
See Block Diagram

Figure 12. Total Harmonic Distortion (THD); as a Function of Audio Input Frequency



NOTES:
V_{CC} = 8 5V; f_I = 1kHz
See Block Diagram

Figure 13. Total Harmonic Distortion (THD) as a Function of Output Voltage (V_O)



NOTES:
1 V_{CC} = 15V
2 V_{CC} = 12V
3 V_{CC} = 8 5V
f = 20Hz to 20kHz
See Block Diagram

Figure 14. Noise Output Voltage ($V_{NO(RMS)}$; Unweighted); as a Function of Voltage Gain (A_V)

7

Signetics

TDA8440
Video and Audio Switch IC

Product Specification

Linear Products

DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in applications equipped with video/audio inputs.

It provides two 3-State switches for audio channels and one 3-State switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be controlled via a bidirectional I^2C bus or it can be controlled directly by DC switching signals. Sufficient sub-addressing is provided for the I^2C bus mode.

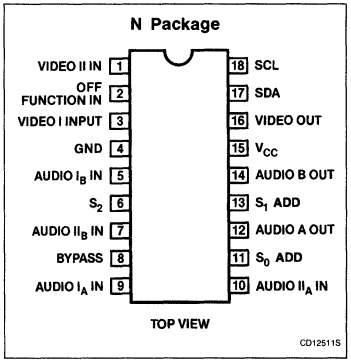
FEATURES

- **Combined analog and digital circuitry gives maximum flexibility in channel switching**
- **3-State switches for all channels**
- **Selectable gain for the video channels**
- **Sub-addressing facility**
- **I^2C bus or non-I^2C bus mode (controlled by DC voltages)**
- **Slave receiver in the I^2C bus mode**
- **External OFF command**
- **System expansion possible up to 7 devices (14 sources)**
- **Static short-circuit proof outputs**

APPLICATIONS

- **TVRO**
- **Video and audio switching**
- **Television**
- **CATV**

PIN CONFIGURATION



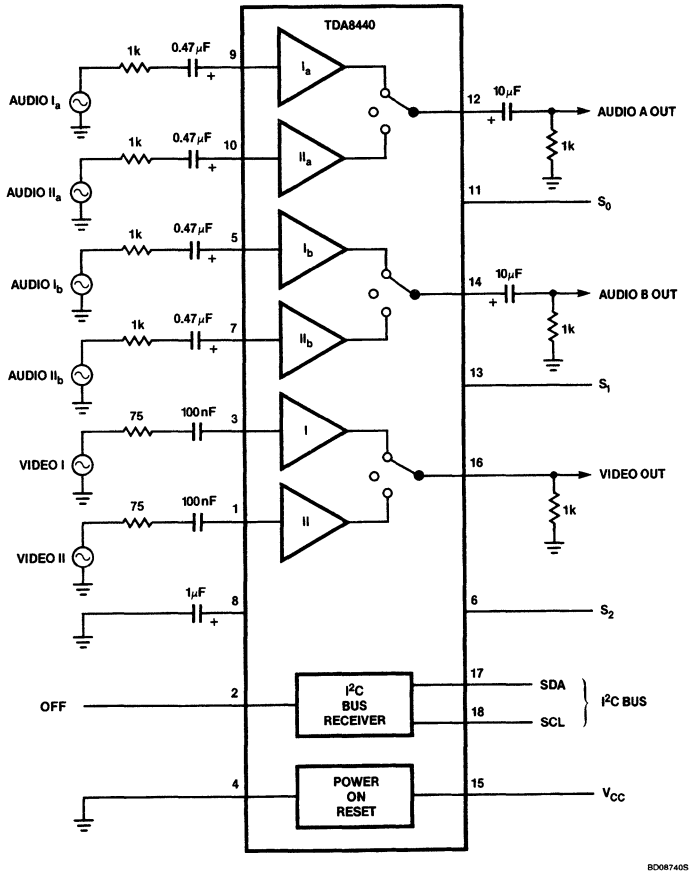
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102)	0 to 70°C	TDA8440N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage Pin 15	14	V
	Input voltage		
V_{SDA}	Pin 17	−0.3 to V_{CC} +0.3	V
V_{SCL}	Pin 18	−0.3 to V_{CC} +0.3	V
V_{OFF}	Pin 2	−0.3 to V_{CC} +0.3	V
V_{S0}	Pin 11	−0.3 to V_{CC} +0.3	V
V_{S1}	Pin 13	−0.3 to V_{CC} +0.3	V
V_{S2}	Pin 6	−0.3 to V_{CC} +0.3	V
$-I_{16}$	Video output current Pin 16	50	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
θ_{JA}	Thermal resistance from junction to ambient in free-air	50	°C/W

BLOCK DIAGRAM AND TEST CIRCUIT



NOTE:
S0, S1, S2, and OFF (Pins 11, 13, 6, and 2) connected to V_{CC} or GND If more than 1 device is used, the outputs and Pin 8 (bias decoupling of the audio inputs) may be connected in parallel

7

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{15-4}	Supply voltage	10		13.2	V
I_{15}	Supply current (without load)		37	50	mA
Video switch					
C_1C_3	Input coupling capacitor	100			nF
A_{3-16} A_{3-16}	Voltage gain (times 1; SCL = L) (times 2; SCL = H)	−1 +5	0 +6	+1 +7	dB dB
A_{1-16} A_{1-16}	Voltage gain (times 1; SCL = L) (times 2; SCL = H)	−1 +5	0 +6	+1 +7	dB dB
V_{3-4}	Input video signal amplitude (gain times 1)			4.5	V
V_{1-4}	Input video signal amplitude (gain times 1)			4.5	V
Z_{16-4}	Output impedance		7		Ω
Z_{16-4}	Output impedance in 'OFF' state	100			kΩ
	Isolation (off-state) (f_O = 5MHz)	60			dB
S/S + N	Signal-to-noise ratio[2]	60			dB
V_{16-4}	Output top-sync level	2.4	2.8	3.2	V
G	Differential gain			3	%
V_{16-4}	Minimum crosstalk attenuation[1]	60			dB
RR	Supply voltage rejection[3]	36			dB
BW	Bandwidth (1dB)	10			MHz
α	Crosstalk attenuation for interference caused by bus signals (source impedance 75Ω)	60			db
Audio switch "A" and "B"					
$V_{9-4\ (RMS)}$ $V_{10-4\ (RMS)}$ $V_{5-4\ (RMS)}$ $V_{7-4\ (RMS)}$	Input signal level			2 2 2 2	V V V V
Z_{9-4} Z_{10-4} Z_{5-4} Z_{7-4}	Input impedance	50 50 50 50	100 100 100 100		kΩ kΩ kΩ kΩ
Z_{12-4} Z_{14-4}	Output impedance			10 10	Ω Ω
Z_{14-4}	Output impedance (off-state)	100			kΩ
V_{9-12} V_{10-12} V_{5-14} V_{7-14}	Voltage gain	−1 −1 −1 −1	0 0 0 0	+1 +1 +1 +1	dB dB dB dB
	Isolation (off-state) (f = 20kHz)	90			dB
S/S + N	Signal-to-noise ratio[4]	90			dB
THD	Total harmonic distortion[6]			0.1	%

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Crosstalk attenuation for interferences caused by video signals[5]				
α	Weighted	80			dB
α	Unweighted	80			dB
α	Crosstalk attenuation for interferences caused by sinusoidal sound signals[5]	80			dB
	Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1kΩ)	80			dB
RR	Supply voltage rejection	50			dB
BW	Bandwidth (−1dB)	50			kHz
I²C bus inputs/outputs SDA (Pin 17) and SCL (Pin 18)					
V_{IH}	Input voltage HIGH	3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+1.5	V
I_{IH}	Input current HIGH[7]			10	μA
I_{IL}	Input current LOW[7]			10	μA
V_{OL}	Output voltage LOW at $I_{OL} = 3mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
C_I	Capacitance of SDA and SCL inputs, Pins 17 and 18			10	pF
Sub-address inputs S_0 (Pin 11), S_1 (Pin 13), S_2 (Pin 6)					
V_{IH}	Input voltage HIGH	3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+0.4	V
I_{IH}	Input current HIGH			10	μA
I_{IL}	Input current LOW	−50		0	μA
OFF input (Pin 2)					
V_{IH}	Input voltage HIGH	+3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+0.4	V
I_{IH}	Input current HIGH			20	μA
I_{IL}	Input current LOW	−10		2	μA

NOTES:

1. Caused by drive on any other input at maximum level, measured in B = 5MHz, source impedance for the used input 75Ω,

   $$\text{crosstalk} = 20\log \frac{V_{OUT}}{V_{IN}\ \text{max}}$$

2. $$S/N = 20\log \frac{V_O\ \text{video noise}\ (P-P)\ (2V)}{V_O\ \text{noise}\ _{RMS}\ B = 5MHz}$$

3. Supply voltage ripple rejection $= 20\log \frac{V_R\ \text{supply}}{V_R\ \text{on output}}$ at f = max 100kHz

4. $$S/N = 20\log \frac{V_O\ \text{nominal (0 5V)}}{V_O\ \text{noise}\ B = 20kHz}.$$

5. Caused by drive of any other input at maximum level, measured in B = 20kHz, source impedance of the used input = 1kΩ,

   $\text{crosstalk} = 20\log \frac{V_{OUT}}{V_{IN}\ \text{max}}$ according to DIN 45405 (CCIR 468)

6. f = 20Hz to 20kHz.
7. Also if the supply is switched off.

AC ELECTRICAL CHARACTERISTICS I^2C bus load conditions are as follows: 4kΩ pull-up resistor to +5V; 200pF to GND. All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			μs
$t_{S\ (STA)}$	Start condition setup time	4			μs
$t_{H\ (STA)}$	Start condition hold time	4			μs
t_{LOW}	SCL, SDA LOW period	4			μs
t_{HIGH}	SCL, HIGH period	4			μs
t_R	SCL, SDA rise time			1	μs
t_F	SCL, SDA fall time			0.3	μs
$t_{S\ (DAT)}$	Data setup time (write)	1			μs
$t_{H\ (DAT)}$	Data hold time (write)	1			μs
$t_{S\ (CAC)}$	Acknowledge (from TDA8440) setup time			2	μs
$t_{H\ (CAC)}$	Acknowledge (from TDA8440) hold time	0			μs
$t_{S\ (STO)}$	Stop condition setup time	4			μs

Table 1. Sub-Addressing

S_2	S_1	S_0	SUB-ADDRESS		
			A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an auxiliary video/audio plug. The IC incorporates 3-State switches which comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) with an auxiliary input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the auxiliary video/audio plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to DC switching voltages. Inputs S_0 (Pin 11), S_1 (Pin 13), and S_2 (Pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1, and S_2 can be connected to the supply voltage (H) or to ground (L). In this way, no peripheral components are required for selection.

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the auxiliary video/audio plug, inputs S_2, S_1, and S_0 must be connected to the supply line (12V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the auxiliary video/audio plug:

- Sources I are selected if SDA = 12V (external source)
- Sources II are selected if SDA = 0V (TV mode)
- Video amplifier gain is 2 × if SCL = 12V (external source)
- Video amplifier gain is 1 × if SCL = 0V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12V switching voltage on the plug.

- All switches are in the OFF position if OFF = H (12V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0V)

I^2C BUS CONTROL

Detailed information on the I^2C bus is available on request.

Table 2. TDA8440 I²C Bus Protocol

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio I_a is selected to audio output a
D_7 = 0 audio I_a is not selected
D_6 = 1 audio II_a is selected to audio output a
D_6 = 0 audio II_a is not selected
D_5 = 1 audio I_b is selected to audio output b
D_5 = 0 audio I_b output is not selected
D_4 = 1 audio II_b is selected to audio output b
D_4 = 0 audio II_b is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

D_0/OFF Gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	In accordance with last defined $D_7 - D_1$ (may be entered while OFF = HIGH)
1 (off input inactive)	H	In accordance with $D_7 - D_1$
1	L	In accordance with $D_7 - D_1$

OFF FUNCTION

With the OFF input all outputs can be switched off (high-ohmic mode), depending on the value of D_0.

Power-on Reset

The circuit is provided with a power-on reset function.

When the power supply is switched on, an internal pulse will be generated that will reset the internal memory S_0. In the initial state all the switches will be in the off position and the OFF input is active ($D_7 - D_0 = 0$), (I^2C mode). In the non-I^2C mode, positions are defined via SDA and SCL input voltages.

When the power supply decreases below 5V, a pulse will be generated and the internal memory will be reset. The behavior of the switches will be the same as described above.

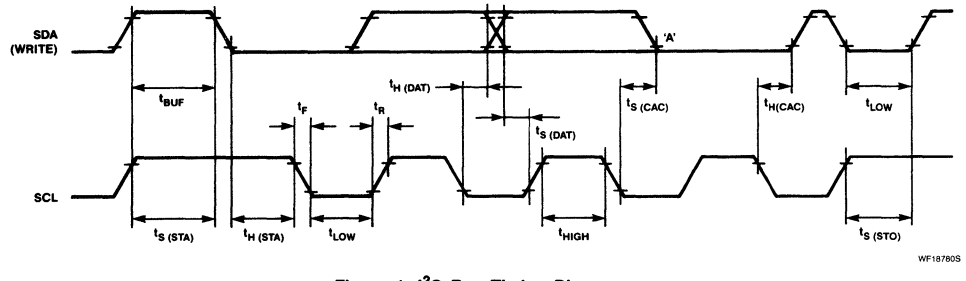


Figure 1. I²C Bus Timing Diagram

Signetics

TEA6300

Digitally-Controlled Tone, Volume, and Fader Control Circuit

Linear Products

Preliminary Specification

DESCRIPTION

The TEA6300 is a single-chip I^2C bus-controlled tone, volume, loudness, and fader control circuit ideal for audio signal processing in an automotive entertainment environment. The TEA6300 provides three stereo source input selector switching, volume, loudness, tone, and fader (front/rear) controls. The active tone control functions are determined by two capacitors along with on-chip op amps which keep external component counts to a minimum.

FEATURES

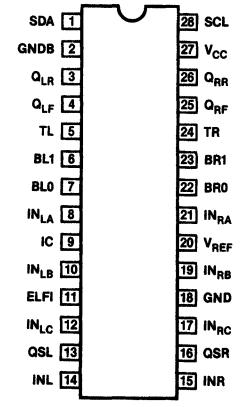
- **Source selector for three stereo inputs**
- **Low noise and distortion**
- **Volume and balance control; Control range of 86dB in 2dB steps**
- **Bass and treble control from +15dB (treble +12dB) to -12dB in 3dB steps**
- **Fader control from 0dB to -30dB in 2dB steps**
- **Fast muting**
- **Low noise suitable for DOLBY® NR**
- **Signal handling suitable for compact disc**
- **Pop-free on/off switching**
- **28-pin package**

APPLICATIONS

- **Auto radio**
- **Audio systems**
- **TV**
- **Remote control audio systems**

PIN CONFIGURATION

N Package



TOP VIEW

CD13340S

PIN NO.	SYMBOL	DESCRIPTION
1	SDA	Data input/output
2	GNDB	Ground for BUS terminals
3	Q_{LR}	Output left rear
4	Q_{LF}	Output left front
5	TL	Termination for treble control capacitor left channel
6	BL1	Termination for bass control capacitor left channel
7	BL0	Termination for bass control capacitor left channel
8	IN_{LA}	Input left source A
9	IC	Internal connected
10	IN_{LB}	Input left source B
11	ELFI	Electronic filtering for supply
12	IN_{LC}	Input left source C
13	QSL	Output source selector left
14	INL	Input left control part
15	INR	Input right control part
16	QSR	Output source selector right
17	IN_{RC}	Input right source C
18	GND	Ground
19	IN_{RB}	Input right source B
20	V_{REF}	Reference voltage (½ V_{CC})
21	IN_{RA}	Input right source A
22	BR0	Termination for bass control capacitor right channel
23	BR1	Termination for bass control capacitor right channel
24	TR	Termination for treble control capacitor right channel
25	Q_{RF}	Output right front
26	Q_{RR}	Output right rear
27	V_{CC}	Supply voltage
28	SCL	Clock input

ORDERING INFORMATION

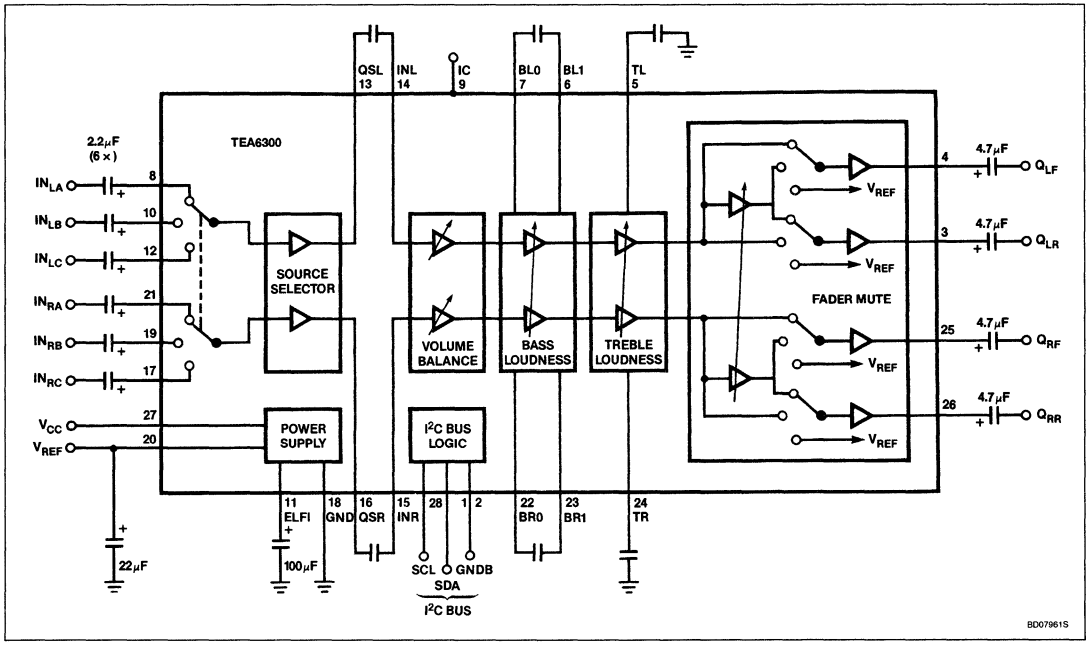
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117BE)	-40°C to +85°C	TEA6300N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pins 27 - 18)	16	V
P_{TOT}	Maximum power dissipation	2	W
T_{STG}	Storage temperature range	-55 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

Digitally-Controlled Tone, Volume, and Fader Control Circuit TEA6300

BLOCK DIAGRAM



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Digitally-Controlled Tone, Volume, and Fader Control Circuit TEA6300

FUNCTIONAL DESCRIPTION

The input selector selects three stereo channels, e.g., RF part (AM/FM), recorder and compact disk. As the outputs of the source selector as well as the inputs of the main control part are available, additional circuits like compander- and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion, and a high dynamic range for the circuit.

The separated volume controls of the left and the right channel make the balance control possible. The range and the characteristic of the balance is software-programmable by setting an extra bass (and optional treble) control, depending on the actual volume position, the loudness function, performed by software in a microcomputer controlling both the switching points and the ranges. Because the TEA6300 has four outputs, a low-level fader is included. The fader control is independent of the volume control and an extra mute position for the front or the rear or for all channels is built in. The last function may be used for muting during preset selection. For pop-free switching, on and off, an extra pop suppression circuitry is built in. As all switching and control functions are controllable via the two-wire I^2C bus, no external interface between the microcomputer and the TEA6300 is required. The on-chip power-on reset sets the TEA6300 into the general mute mode.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 8.5V; R_S = 600Ω; R_L = 10kΩ; f = 1kHz; T_A = 25°C (Figure 6), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	7.0	8.5	13.2	V
I_{CC}	Supply current		26		mA
V_{REF}	Internal reference voltage (Pin 20) $V_{REF} = 0.5\ V_{CC}$		4.25		V
A_V	Maximum gain bass and treble linear, fader off		20		dB
	Output level				
$V_{O(RMS)}$	for P_{MAX} at the output stage		500		mV
$V_{O(RMS)}$	for start of clipping		1000		mV
$V_{I(RMS)}$	Input sensitivity at V_O = 500mV		50		mV
	Frequency response				
f_R	bass and treble linear; roll-off frequency −1dB	35		20000	Hz
αCS	Channel separation G = 0dB; bass and treble linear; frequency range 250Hz to 10kHz	45	70		dB
	Total harmonic distortion frequency range 20Hz to 12.5kHz				
THD	V_{IN} = 50mV; G = 20dB		0.1	0.3	%
THD	V_{IN} = 500mV; G = 0dB		0.05	0.2	%
THD	V_{IN} = 1.6V; G = −10dB		0.2	0.5	%
	Ripple rejection				
	$V_{R(RMS)}$ < 200mV; G = 0dB; bass and treble linear;				
RR_{100}	at f = 100Hz		70		dB
RR_{RANGE}	at f = 40Hz to 12.5kHz		tbf		dB
	Signal-to-noise ratio bass and treble linear;[1, 2]				
	CCIR 468-2 weighted; quasi-peak				
S/N	V_I = 50mV; V_O = 46mV; P_O = 50mW		65		dB
S/N	V_I = 500mV; V_O = 45mV; P_O = 50mW		67		dB
S/N	V_I = 50mV; V_O = 200mV; P_O = 1W		70		dB
S/N	V_I = 500mV; V_O = 200mV; P_O = 1W		78		dB
S/N	V_I = 50mV; V_O = 500mV; P_O = 6W		70		dB
S/N	V_I = 500mV; V_O = 500mV; P_O = 6W		85		dB
P_N	Noise power mute position, only contribution of TEA6300, power amplifier for 25W			10	nW
	Crosstalk (20 log $V_{BUS(P-P)}/V_{O(RMS)}$)				
	between BUS inputs and signal outputs				
αB	G = 0Db; bass and treble linear		110		dB

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 8.5V; R_S = 600Ω; R_L = 10kΩ; f = 1kHz; T_A = 25°C (Figure 6), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Source selector					
Z_I	Input impedance	20	30	40	kΩ
Z_O	Output impedance			100	Ω
R_L	Admissible output load resistance	10			kΩ
C_L	Admissible output load capacity	0		200	pF
αS	Input isolation not selected source; frequency range 40Hz to 12 5kHz		80		dB
G	Gain $R_L > 10k\Omega$		0		dB
$V_{B\ INT}/V_{REF}$	Internal bias voltage		1		
$V_{I(RMS)}$ $V_{I(RMS)}$	Maximum input level THD < 0.5% THD < 0.5%; V_{CC} = 7.5V		1.65 1.5		V V
THD	Total harmonic distortion V_I = 500mV, R_L = 10kΩ			0.1	%
N_W	Noise voltage weighted CCIR 468-2, quasi peak		9	20	μV
V_O	DC offset voltage between any inputs			10	mV
Control part					
	(Source selector disconnected, source resistance 600Ω)				
Z_I	Input impedance	35	50	65	kΩ
Z_O	Output impedance		100	150	Ω
R_L	Admissible output load resistance	10			kΩ
C_L	Admissible output load capacity	0		1000	pF
$V_{I(RMS)}$	Maximum input voltage THD < 0 5%; G = −10dB; bass and treble linear		2.0		V
	Noise voltage weighted acc CCIR 468-2, quasi peak, bass and treble linear, fader off				
N_W	gain 20dB		110	220	μV
N_W	gain 0dB		25	50	μV
N_W	gain −66dB		19	38	μV
N_W	mute position		11	22	μV
Volume control					
G_C	Continuous control range		86		dB
	Step resolution		2		dB
ΔG_a	Attenuator set error (G = +20 to −50dB)			2	dB
ΔG_a	Attenuator set error (G = +20 to −66dB)			3	dB
ΔG_t	Gain tracking error balance in mid position, bass and treble linear			2	dB
αM	Mute attenuation		80		dB

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DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 8.5V; R_S = 600Ω; R_L = 10kΩ; f = 1kHz; T_A = 25°C (Figure 6), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Bass control					
	Bass control range				
G_b	f = 40Hz; maximum boost	14	15	16	dB
$-G_b$	f = 40Hz; maximum attenuation	11	12	13	dB
	Step resolution		3		dB
	Step error			0.5	dB
Treble control					
	Treble control range				
G_t	f = 15kHz; maximum boost	11	12	13	dB
$-G_t$	f = 15kHz; maximum attenuation	11	12	13	dB
G_t	f > 15kHz; maximum boost			15	dB
	Step resolution		3		dB
	Step error			0.5	dB
Fader control					
G_f	Continuous attenuation fader control range		30		dB
	Step resolution		2		dB
	Attenuator set error			1.5	dB
αM	Mute attenuation		80		dB
Digital part					
	Bus terminals Input voltage				
V_{IH}	HIGH	3		12	V
V_{IL}	LOW	−0.3		1.5	V
	Input current				
I_{IH}	HIGH	−10		10	μA
I_{IL}	LOW	−10		10	μA
	Output voltage LOW				
V_{OL}	I_L = 3mA			0.4	V
AC Characteristics according to the I^2C Bus specification					
	Power-on Reset When RESET is active the GMU (general mute) bit is set and the BUS receiver is in RESET position				
	Increasing supply voltage				
V_{CC}	start of reset			2.5	V
V_{CC}	end of reset	5.2	6.0	6.8	V
	Decreasing supply voltage				
V_{CC}	start of reset	4.2	5.0	5.8	V

NOTES:

1. The indicated values for output power assume a 6W power amp, with 20dB gain, connected to the output of the circuit Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. Signal-to-noise ratios on a CCIR 468-2 average reading meter are 4.5dB better than on CCIR 468-2 quasi peak

Digitally-Controlled Tone, Volume, and Fader Control Circuit TEA6300

I²C BUS FORMAT

S	SLAVE ADDRESS	A	SUB-ADDRESS	A	DATA	A	P

S = start condition
SLAVE ADDRESS = 1000 0000
A = acknowledge, generated by the slave
SUB-ADDRESS = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte DATA is transmitted, then auto-increment of the sub-address is performed

Table 1

FUNCTION	SUB-ADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
Volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
Bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
Treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
Fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
Switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

NOTES:
Function of the bits:

VL0 to VL5	Volume control left
VR0 to VR5	Volume control right
BA0 to BA3	Bass control
TR0 to TR3	Treble control
FA0 to FA3	Fader control
FCH	Select fader channel (front or rear)
MFN	Mute control of the selected fader channel (front or rear)
SCA to SCC	Source selector control
GMU	Mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	Do not care bits (1 during testing)

Table 2. Bass Setting

G (dB)	DATA			
	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
- 3	0	1	1	0
- 6	0	1	0	1
- 9	0	1	0	0
-12	0	0	1	1
-12	0	0	1	0
-12	0	0	0	1
-12	0	0	0	0

Table 3. Treble Setting

G (dB)	DATA			
	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
- 3	0	1	1	0
- 6	0	1	0	1
- 9	0	1	0	0
-12	0	0	1	1
-12	0	0	1	0
-12	0	0	0	1
-12	0	0	0	0

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Table 4. Volume Setting LEFT

G (dB)	DATA					
	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
- 2	1	1	0	1	0	0
- 4	1	1	0	0	1	1
- 6	1	1	0	0	1	0
- 8	1	1	0	0	0	1
-10	1	1	0	0	0	0
-12	1	0	1	1	1	1
-14	1	0	1	1	1	0
-16	1	0	1	1	0	1
-18	1	0	1	1	0	0
-20	1	0	1	0	1	1
-22	1	0	1	0	1	0
-24	1	0	1	0	0	1
-26	1	0	1	0	0	0
-28	1	0	0	1	1	1
-30	1	0	0	1	1	0
-32	1	0	0	1	0	1
-34	1	0	0	1	0	0
-36	1	0	0	0	1	1
-38	1	0	0	0	1	0
-40	1	0	0	0	0	1
-42	1	0	0	0	0	0
-44	0	1	1	1	1	1
-46	0	1	1	1	1	0
-48	0	1	1	1	0	1
-50	0	1	1	1	0	0
-52	0	1	1	0	1	1
-54	0	1	1	0	1	0
-56	0	1	1	0	0	1
-58	0	1	1	0	0	0
-60	0	1	0	1	1	1
-62	0	1	0	1	1	0
-64	0	1	0	1	0	1
-66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5. Volume Setting RIGHT

G (dB)	DATA					
	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
- 2	1	1	0	1	0	0
- 4	1	1	0	0	1	1
- 6	1	1	0	0	1	0
- 8	1	1	0	0	0	1
-10	1	1	0	0	0	0
-12	1	0	1	1	1	1
-14	1	0	1	1	1	0
-16	1	0	1	1	0	1
-18	1	0	1	1	0	0
-20	1	0	1	0	1	1
-22	1	0	1	0	1	0
-24	1	0	1	0	0	1
-26	1	0	1	0	0	0
-28	1	0	0	1	1	1
-30	1	0	0	1	1	0
-32	1	0	0	1	0	1
-34	1	0	0	1	0	0
-36	1	0	0	0	1	1
-38	1	0	0	0	1	0
-40	1	0	0	0	0	1
-42	1	0	0	0	0	0
-44	0	1	1	1	1	1
-46	0	1	1	1	1	0
-48	0	1	1	1	0	1
-50	0	1	1	1	0	0
-52	0	1	1	0	1	1
-54	0	1	1	0	1	0
-56	0	1	1	0	0	1
-58	0	1	1	0	0	0
-60	0	1	0	1	1	1
-62	0	1	0	1	1	0
-64	0	1	0	1	0	1
-66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6. Fader Function

SETTING		DATA					
Front/Rear dB	dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
- 2	0	1	1	1	1	1	0
- 4	0	1	1	1	1	0	1
- 6	0	1	1	1	1	0	0
- 8	0	1	1	1	0	1	1
-10	0	1	1	1	0	1	0
-12	0	1	1	1	0	0	1
-14	0	1	1	1	0	0	0
-16	0	1	1	0	1	1	1
-18	0	1	1	0	1	1	0
-20	0	1	1	0	1	0	1
-22	0	1	1	0	1	0	0
-24	0	1	1	0	0	1	1
-26	0	1	1	0	0	1	0
-28	0	1	1	0	0	0	1
-30	0	1	1	0	0	0	0
		mute front					
-80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
-80	0	0	1	0	0	0	0

SETTING		DATA					
Front/Rear dB	dB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	- 2	1	0	1	1	1	0
0	- 4	1	0	1	1	0	1
0	- 6	1	0	1	1	0	0
0	- 8	1	0	1	0	1	1
0	-10	1	0	1	0	1	0
0	-12	1	0	1	0	0	1
0	-14	1	0	1	0	0	0
0	-16	1	0	0	1	1	1
0	-18	1	0	0	1	1	0
0	-20	1	0	0	1	0	1
0	-22	1	0	0	1	0	0
0	-24	1	0	0	0	1	1
0	-26	1	0	0	0	1	0
0	-28	1	0	0	0	0	1
0	-30	1	0	0	0	0	0
		mute rear					
0	-80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	-80	0	0	0	0	0	0

Table 7

SELECTED INPUTS	DATA SCC	SCB	SCA
Data not admissible	1	1	1
Data not admissible	1	1	0
Data not admissible	1	0	1
IN_{LC}, IN_{RC}	1	0	0
Data not admissible	0	1	1
IN_{LB}, IN_{RB}	0	1	0
IN_{LA}, IN_{RA}	0	0	1
Data not admissible	0	0	0

MUTE CONTROL	DATA GMU	REMARKS
Active	1	Outputs Q_{LF}, Q_{LR}, Q_{RF} and Q_{RR} are muted
Passive	0	No general mute

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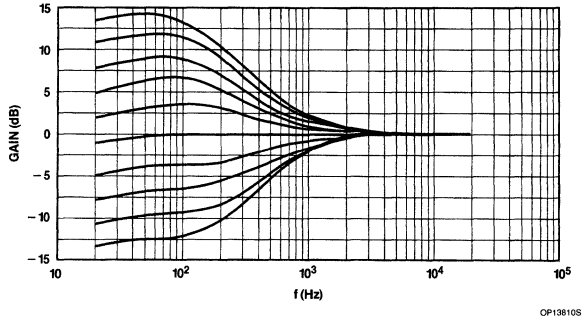


Figure 1. Bass Control

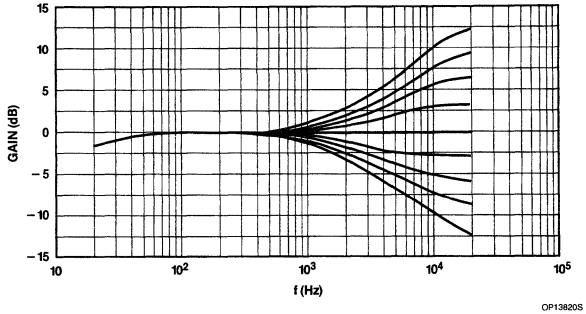


Figure 2. Treble Control

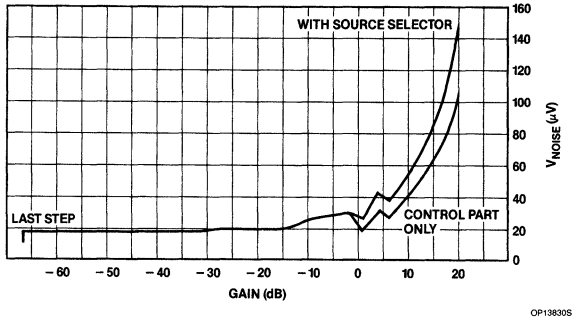


Figure 3. Output Noise Voltage (CCIR 468-2 Weighted; Quasi Peak)

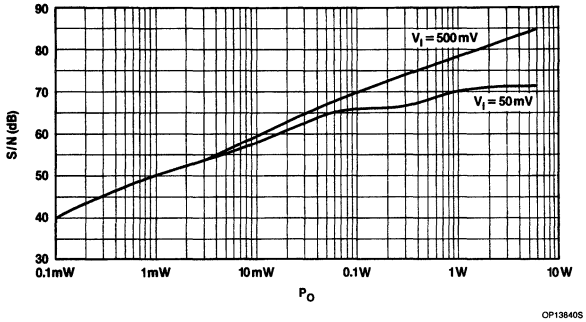
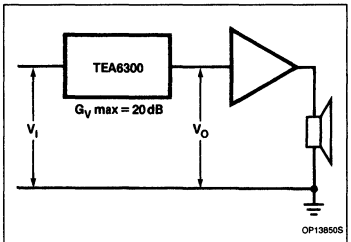


Figure 4. Signal-to-Noise Ratio (CCIR 468-2 Weighted; Quasi Peak) With a 6W Power Amplifier (Gain 20dB) Without Noise Contribution of the Power Amplifier (See Figure 6)



NOTE:
$V_{I\ MIN}$ = 50mV, V_O = 500mV for P_{MAX}

Figure 5. Recommended Level Diagram

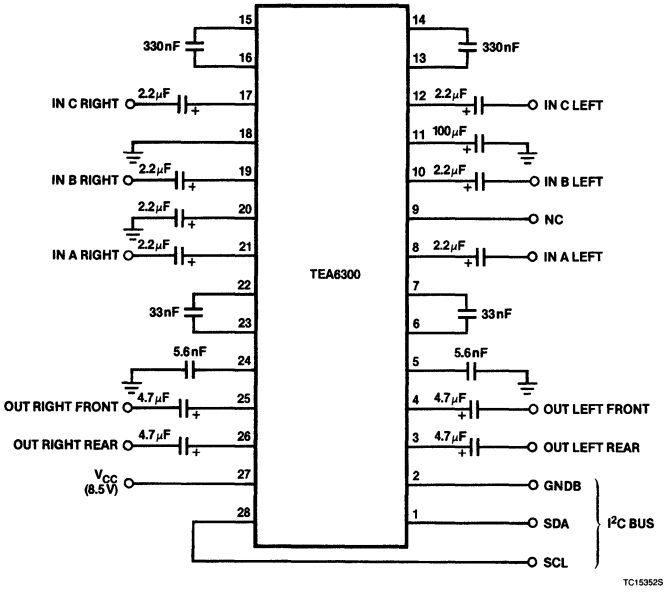


Figure 6. Test and Application Circuit

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Signetics

NE5240
Dolby Digital Audio Decoder

Preliminary Specification

Linear Products

DESCRIPTION

The NE5240 is a two channel decoder for the Dolby Digital Audio System. *The IC includes input latches to separate two channels of audio and control data, a precision internal voltage reference, and digital/analog signal processing circuitry for each channel. The IC design is implemented in a bipolar process to achieve low noise, low distortion, and wide dynamic range.

NOTE:

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and applications information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California

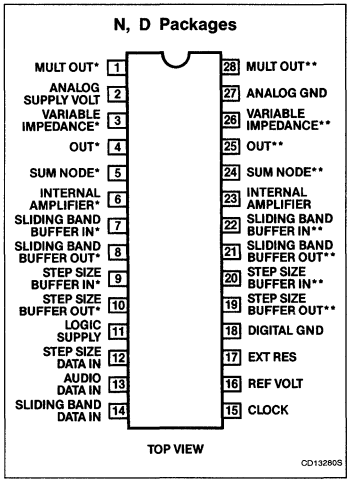
FEATURES

- **Wide dynamic range — 85dB**
- **Low distortion 0.05% @ 1kHz, −10dB**
- **TTL and CMOS compatible logic inputs**
- **Audio bandwidth — 30Hz to 15kHz**

APPLICATIONS

- **High quality digital transmission of audio data**
- **Satellite reception**
- **Cable TV**
- **Microwave distribution systems**

PIN CONFIGURATION

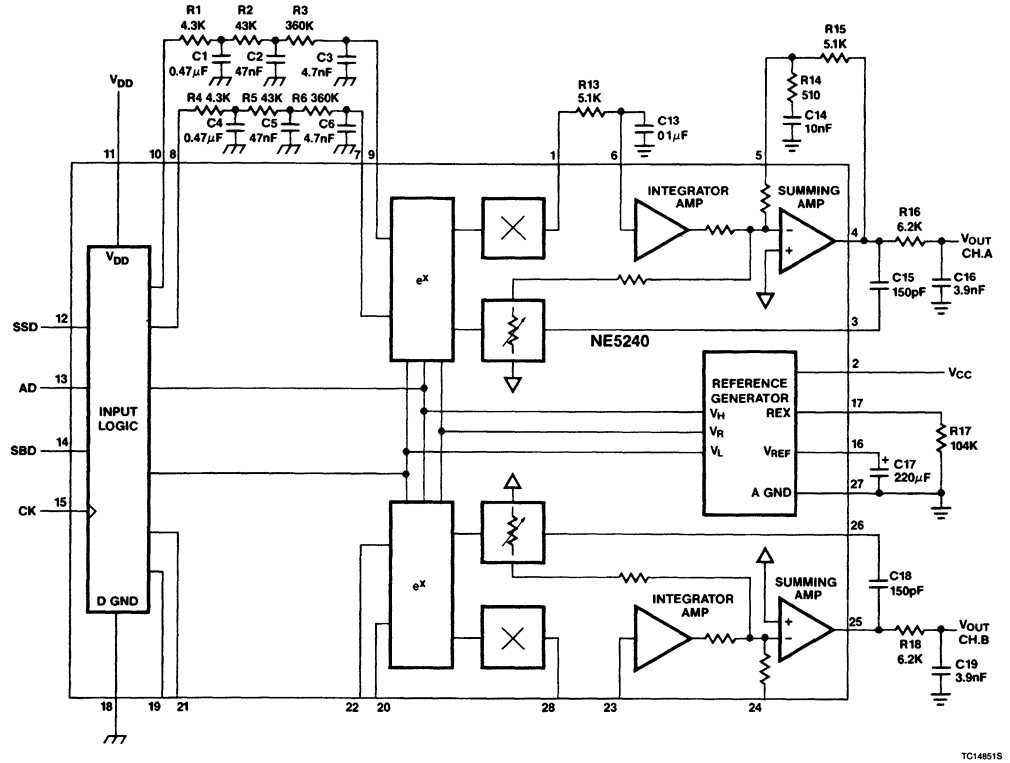


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin SO	0 to +70°C	NE5240D
28-Pin Plastic DIP	0 to +70°C	NE5240N

Dolby Digital Audio Decoder NE5240

BLOCK DIAGRAM



NOTE:
One channel of the application shown with external components

7

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Analog supply voltage	+15	V
V_{DD}	Logic supply voltage	+7	V
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

All specifications are at $T_A = 25°C$, $V_{CC} = 12V$, $V_{DD} = 5V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Analog voltage supply range		10	12	14	V
V_{DD}	Logic voltage supply range		4.5	5	5.5	V
I_{CC}	Supply current	$V_{CC} = 12V$	10	24	35	mA
I_{DD}	Supply current	$V_{DD} = 5V$	5	12	18	mA
V_{IH}	Input voltage high		2		5	V
V_{IL}	Input voltage low		0		0.8	V
I_{IL}	Input current low	$V_{DD} = 4.5V$		10	100	μA
I_{IH}	Input current high			1	100	μA
t_S	Setup time		150			ns
t_H	Hold time		150			ns
I_B	Input buffers, Pins 7, 9, 20, 22	$V_{IN} = 2.0V$			100	nA
R_L	Summing amp output load		5			kΩ
V_{OS}	Output offset voltage			0.1	0.6	V
V_{OS}	Output offset change	10%-SBD-70%		±5	±20	mV
V_{REF}	Reference voltage		5.5	$0.5V_{CC}$	6.5	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS			UNIT
			Min	Typ	Max	
V_O	Full-Scale output, 0dB	f = 100Hz		1.8		V_{RMS}
	Absolute output level	f = 1kHz, SSD = 40%	93	118	150	mV_{RMS}
	Channel balance	f = 1kHz, 20%-SSD-70%	-1.5		1.5	dB
	Step-Size linearity	f = 1kHz, 20%-SSD-70%	-1.5		1.5	dB
	Step-Size linearity	f = 100Hz, SSD = 90%	-2.5		1.0	dB
f_R	Frequency response	f = 2kHz, SBD = 10%	-1.0		1.0	dB
f_R	Frequency response	f = 5kHz, SBD = 20%	-1.0		1.0	dB
f_R	Frequency response	f = 7kHz, SBD = 30%	-1.0		1.0	dB
f_R	Frequency response	f = 8kHz, SBD = 40%	-1 0		1.0	dB
f_R	Frequency response	f = 10kHz, SBD = 50%	-1.0		1.0	dB
f_R	Frequency response (all WRT 100Hz)	f = 12kHz, SBD = 60% f = 14kHz, SBD = 70%	-1.0 -1.5		1.0 1.5	dB dB
S/N	Dynamic range	SSD = 70%, CCIR/ARM	80	85		dB
THD	Harmonic distortion	f = 1kHz, -3dB		0.1	0.5	%
THD Channel separation	Harmonic distortion	f = 1kHz, -10dB f = 1kHz, 0dB	 60	0.05 75	0.2	% dB
PSRR	Power supply rejection ratio[1]	f = 1kHz		60		dB

NOTES:
1. PSRR depends on value of capacitor on Pin 16.
2. The duty cycle of SSD and SBD control data is 10%, unless otherwise noted.

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Signetics

NE645/646
Dolby Noise Reduction Circuit

Product Specification

Linear Products

DESCRIPTION

The NE645/646 is a monolithic audio noise reduction circuit designed as a direct replacement device for the NE645B/NE646B in Dolby* B-Type noise reduction systems. The NE645/646 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, California.

NOTE:
*T M Dolby Laboratories Licensing Corporation

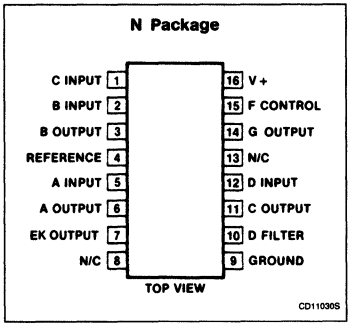
FEATURES

- **Accurate record mode frequency response**
- **Excellent frequency response tracking with temperature and $V_{CC} \pm 0.4$ dB typical**
- **Excellent back-to-back dynamic response — DC shift less than 20mV typical**
- **Improved stability of all op amps**
- **High reliability packaging**

APPLICATIONS

- **Tape decks**
- **Dolby surround sound system**

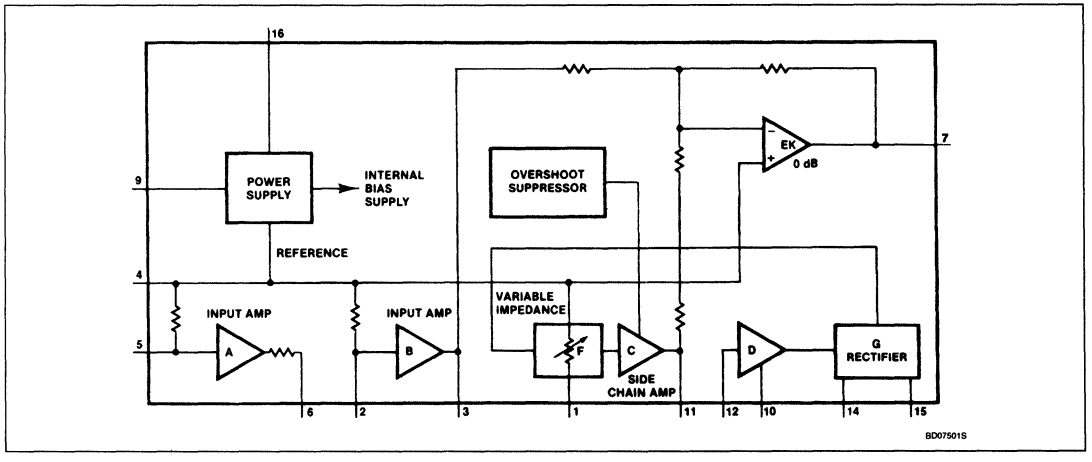
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE645N
16-Pin Plastic DIP	0 to +70°C	NE646N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	24	V
	Temperature range		
T_A	Operating ambient	0 to +70	°C
T_{STG}	Storage	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, f = 20Hz to 20kHz. All levels referenced to 580mV_{RMS} (0dB) at Pin 3, T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE645			NE646			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage Range		8		20	8		20	V
I_{CC}	Supply Current	V_{CC} = 12V		16	24		16	24	mA
A_V	Voltage gain (Pins 5 – 3)	f = 1kHz (Pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
A_V	Voltage gain (Pins 3 – 7)	f = 1kHz, 0 dB at Pin 3, noise reduction out	−0.5	0	+0.5	−0.5	0	+0.5	dB
	Distortion THD, 2nd and 3rd harmonic	f = 20Hz – 10 kHz, 0dB		0.05	0.1		0.05	0.2	%
		f = 20Hz – 10 kHz, +10dB		0.15	0.3		0.2	0.5	%
	Signal handling[1] (V_{CC} = 12V)	1% dist at 1kHz	+12	+15		+12	+15		dB
S/N	Signal-to-noise ratio[2]	Record mode	67	72		64	72		dB
		Playback mode	77	82		74	82		dB
	Record mode Frequency response (at Pin 7) referenced to encode monitor point (Pin 3)	f = 1.4kHz							
		0dB	−1	0	+1	−1.5	0	+1.5	dB
		−20dB	−16.6	−15.6	−14.6	−17.1	−15.6	−14.1	dB
		−30dB	−23.5	−22.5	−21.5	−24.0	−22.5	−21.0	dB
		f = 5kHz							
		0dB	−0.7	+0.3	+1.3	−1.2	+0.3	+1.8	dB
		−20dB	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
		−30dB	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
		−40dB	−30.2	−29.7	−28.7	−30.2	−29.7	−28.2	dB
		f = 20kHz							
		0dB	−0.3	+0.7	+1.7	−0.8	+0.7	+2.2	dB
		−20dB	−18.3	−17.3	−16.3	−18.8	−17.3	−15.8	dB
		−30dB	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
	Back-to-back frequency response	Using typical record mode .5 frequency response test points	−1	0	+1	−1.5	0	+1.5	dB
R_{IN}	Input resistance	Pin 5	35	50	65	35	50	65	kΩ
		Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	kΩ
R_{OUT}	Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	kΩ
		Pin 3		80	120		80	120	Ω
		Pin 7		80	120		80	120	Ω
	Back-to-back frequency response shift								
	vs temperature	0°C to +70°C		±0.4			±0.4		dB
	vs supply voltage	8 – 20V		±0.4			±0.4		dB

NOTES:

1. See maximum signal handling versus supply voltage characteristics
2. All noise levels are measured CCIR/ARM weighted using a 10k source with respect to Dolby level See Dolby Laboratories Bulletin 19.

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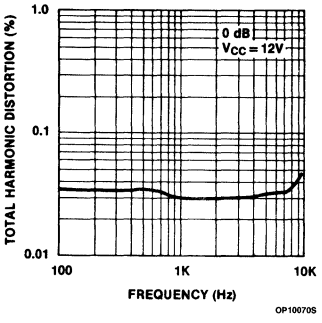
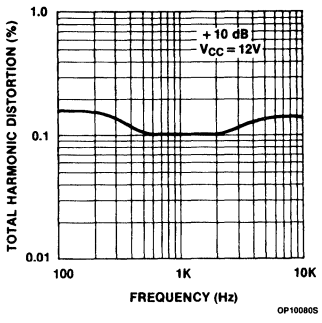
TYPICAL PERFORMANCE CHARACTERISTICS

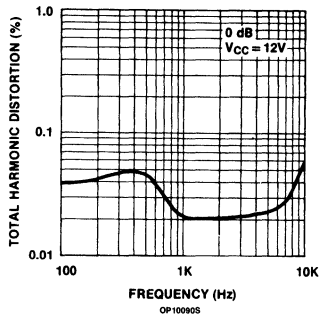
THD vs Frequency Record Mode



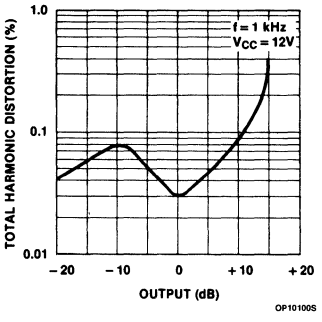
THD vs Frequency Record Mode



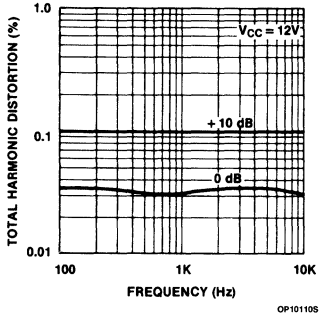
THD vs Frequency Play Mode



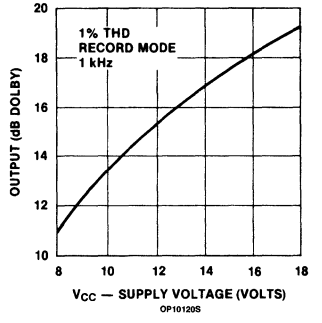
THD vs Output Record Mode



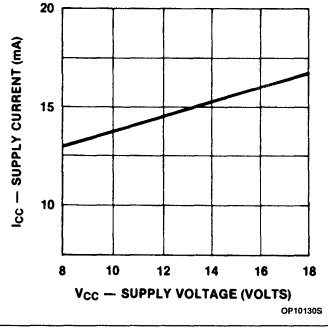
THD vs Frequency
Noise Reduction (NR) Off



Maximum Signal Handling
vs Supply Voltage



Supply Current vs
Supply Voltage



APPLICATION INFORMATION

The NE645/646 is a direct replacement for the NE645B/646B. The NE645/646 incorporates improved design techniques to insure excellent performance required in Dolby B and C Type Audio Noise Reduction Systems. Critical component values are unchanged except for C309 on Pin 1 which is now an optional component in specific applications defined by Dolby Laboratories. All circuit parameters are guaranteed at 12V V_{CC}.

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE:
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

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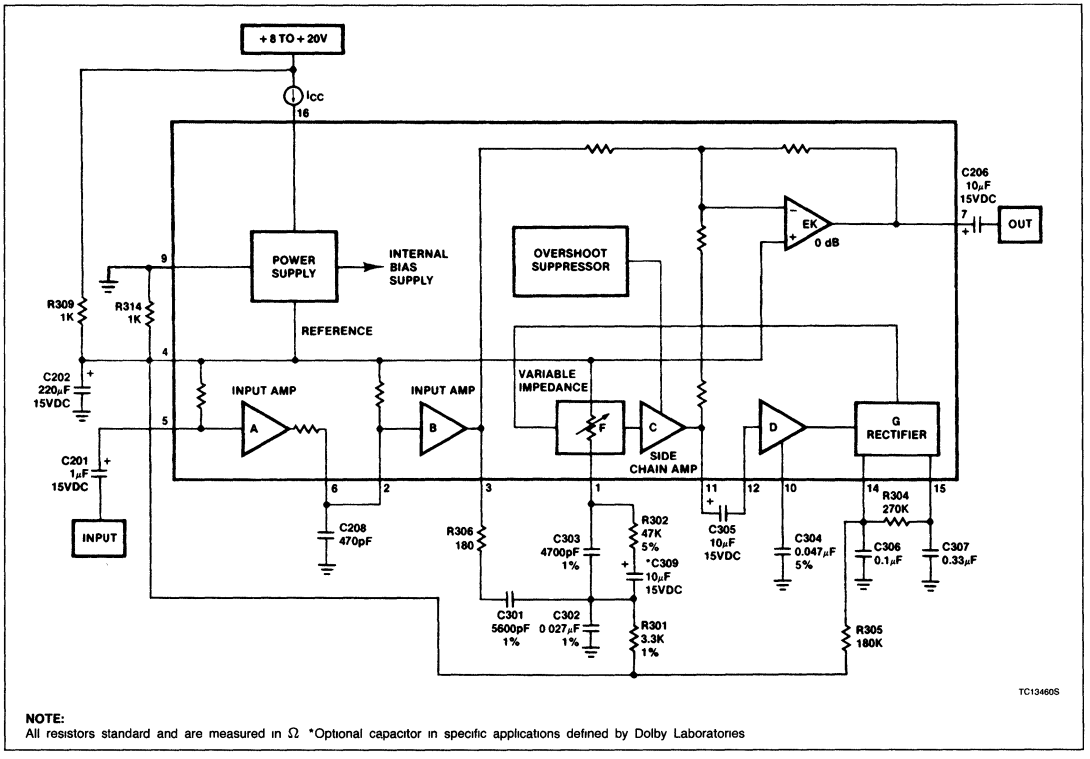
Dolby Noise Reduction Circuit | NE645/646

TEST CIRCUIT



NOTE:
All resistors standard and are measured in Ω *Optional capacitor in specific applications defined by Dolby Laboratories

Signetics

NE649
Low Voltage Dolby Noise Reduction Circuit

Product Specification

Linear Products

DESCRIPTION

The NE649 is an audio noise reduction circuit designed for use in low voltage entertainment systems. The circuit is used to reduce the level of background noise introduced during the recording and playback of audio signals on magnetic tape and improve the noise level in FM broadcast reception. The circuit is intended for use in automotive and portable cassette Dolby™ B-Type noise reduction systems. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

Dolby is a trademark of Dolby Laboratories Licensing Corporation

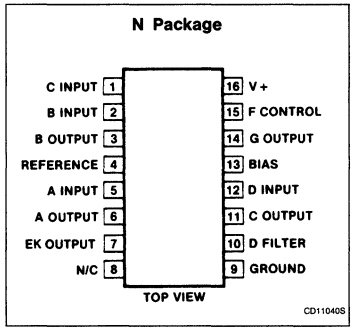
FEATURE

- **Low voltage operation**

APPLICATION

- **Tape decks**

PIN CONFIGURATION



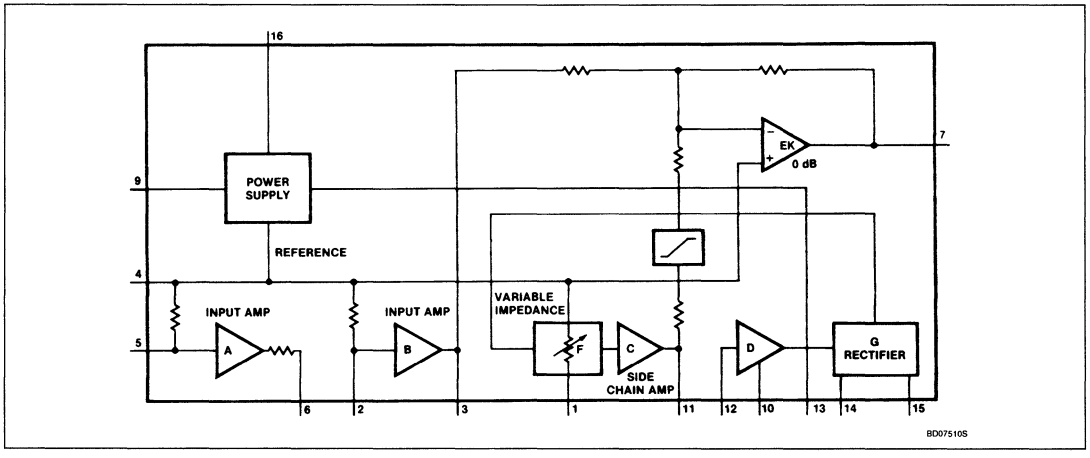
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE649N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	16	V
T_A	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature 10sec max	+300	°C

BLOCK DIAGRAM



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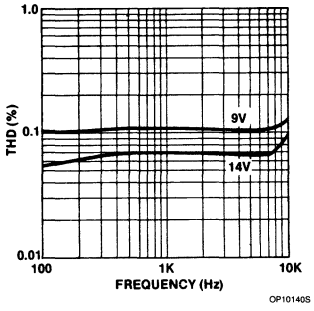
DC ELECTRICAL CHARACTERISTICS V_{CC} = 9V, f = 20Hz to 20kHz. All levels referenced to 580mV_{RMS} (0dB) at Pin 3, T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE649			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range[3]		6	9	14	V
	Minimum voltage supply for 8dB headroom 10dB headroom	 f = 1.4kHz THD < 1%	 6.5 7.5			 V V
I_{CC}	Supply Current			11	18	mA
I_{CC}	Supply Current[1]				20	mA
A_V	Voltage gain (Pins 5 - 3)	f = 1kHz (Pins 6 and 2 connected)	24.5	26	27.5	dB
A_V	Voltage gain (Pins 3 - 7)	f = 1kHz, 0dB at Pin 3, noise reduction out	-0.5	0	+0.5	dB
	Distortion	f = 20kHz to 10kHz, 0dB f = 20Hz to 10kHz, +10dB		0.05 0.2	0.2 0.5	% %
	Signal Handling (See Performance Characteristics)					
S/N	Signal-to-noise ratio[2]	Record (Pins 6 and 2 connected) Playback (Pins 6 and 2 connected)	64 74	72 82		dB dB
	Record mode frequency response (at Pin 7) referenced to encode monitor point (Pin 3)	If = 1.4kHz 0dB -20dB -30dB	 -1.5 -17.1 -24.0	 0 -15.6 -22.5	 +1.5 -14.1 -21.0	 dB dB dB
		f = 5kHz 0dB -20dB -30dB -40dB	 -1.2 -18.3 -23.3 -30.2	 +0.3 -16.8 -21.8 -29.7	 +1.8 -15.3 -20.3 -28.2	 dB dB dB dB
		f = 20kHz 0dB -20dB -30dB	 -0.8 -18.8 -25.0	 +0.7 -17.3 -23.5	 +2.2 -15.8 -22.0	 dB dB dB
	Back-to-back frequency response	Using typical record mode response		±1.5		db
R_{IN}	Input resistance	Pin 5 Pin 2	35 3.1	50 4.2	65 5.3	kΩ kΩ
R_{OUT}	Output resistance	Pin 6 Pin 3 Pin 7	1.9	2.4 80 80	3.1 120 120	kΩ Ω Ω
	Record mode frequency response shift vs temperature vs V_{CC}	 0 to 70°C -40 to 85°C 6 to 14V				 dB dB dB/V

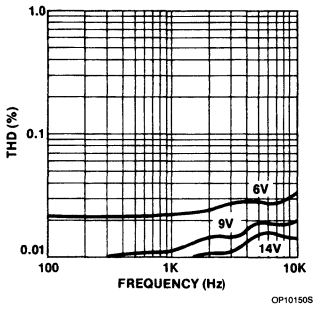
NOTES:
1. With electronic switching
2. All noise levels are measured CCIR/ARM weighted using a 10k source with respect to Dolby level See Dolby Laboratories Bulletin 19.
3 The circuit will function as low as V_{CC} = 4 5V (i.e , output signal present) See graphs of I_{CC} and signal handling vs V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

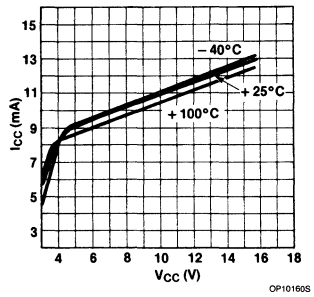
(+10dB) THD vs Frequency



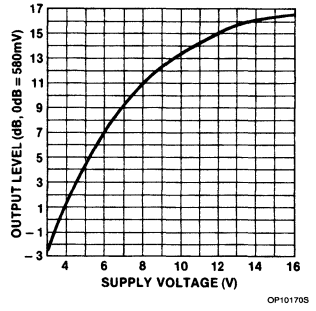
(0dB) THD vs Frequency



Current vs Supply Voltage



Maximum Signal Handling vs Supply Voltage for 1%THD (Record)



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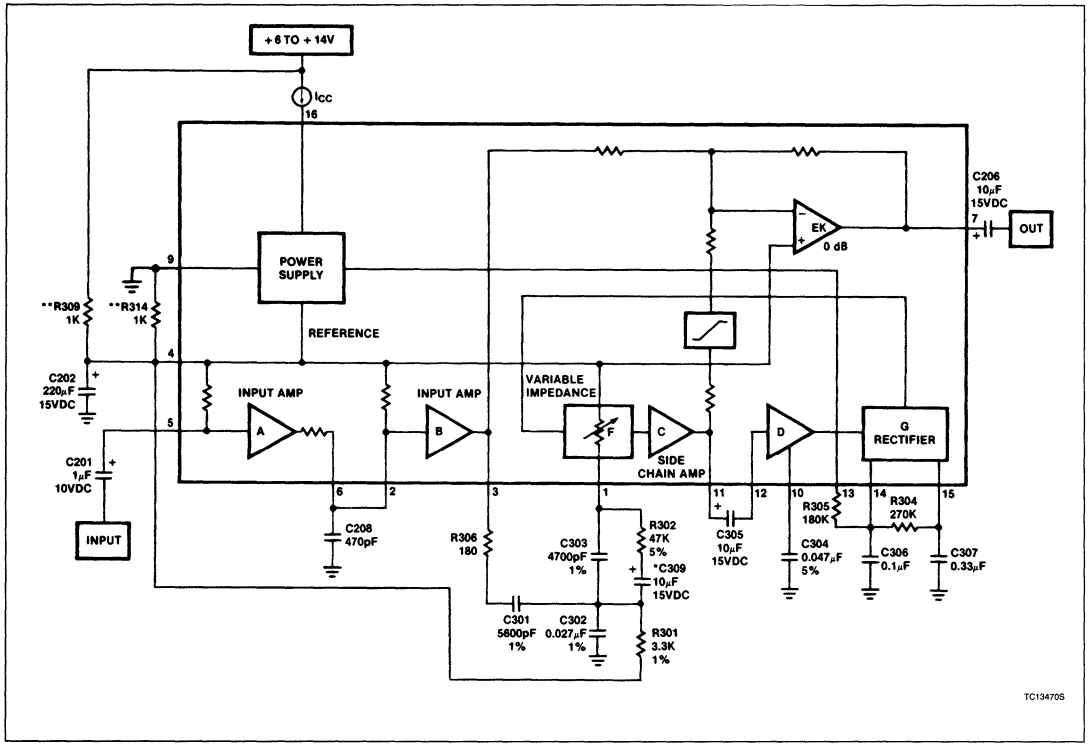
DOLBY ENCODER Output for constant level input (single tone frequency response)

FREQUENCY (kHz)	INPUT LEVEL (dB)								
	0 (DOLBY LEVEL)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE:
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerance which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

Low Voltage Dolby Noise Reduction Circuit NE649

TEST CIRCUIT



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Signetics

NE650
Dolby B-Type Noise Reduction Circuit

Product Specification

Linear Products

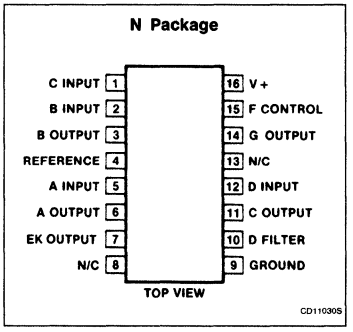
DESCRIPTION

The NE650 is a monolithic audio noise reduction circuit designed for use in Dolby™B-Type noise reduction systems. The NE650 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape.

The NE650 features excellent dynamic characteristics over a wide range of operating conditions and is pin-compatible with NE645/646. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

Dolby is a trademark of Dolby Laboratories Licensing Corporation.

PIN CONFIGURATION



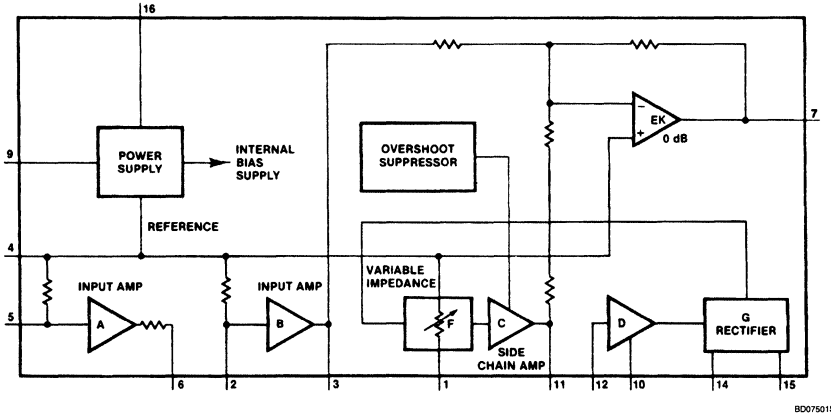
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE650N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	24	V
	Temperature range		
T_A	Operating ambient	0 to +70	°C
T_{STG}	Storage	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	+300	°C

BLOCK DIAGRAM



Dolby B-Type Noise Reduction Circuit | NE650

DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V, f = 20Hz to 20kHz. All levels referenced to 580mV_{RMS}(0db) at Pin 3, T_A = +25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	NE650			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		8		20	V
I_{CC}	Supply current	Electronic switching on		16	24	mA
A_V	Voltage gain (Pins 5 – 3)	f = 1kHz (Pins 6 and 2 connected)	25.5	26	26.5	dB
A_V	Voltage gain (Pins 3 – 7)	f = kHz, 0dB at Pin 3, noise reduction out	−0.5	0	+0.5	dB
A_V	Voltage gain (Pins 2 – 3)	f = 1kHz		13		dB
	Distortion THD: 2nd and 3rd harmonic	f=20Hz to 10kHz, 0dB f=20Hz to 10kHz, +10dB		0.05 0.15	0.1 0.3	% %
	Signal handling	1% distortion at 1kHz	+12	+15		dB
S/N	Signal-to-noise ratio*	Record mode Playback mode	68 78	72 82		dB dB
	Back-to-back frequency response	Using typical record mode response		±0 5		dB
	Record mode frequency response (at Pin 7) referenced to encode monitor point (Pin 3)	f = 1.4kHz 0dB −20dB −30dB	 −0.5 −16.1 −23.5	 0 −15.6 −22.5	 +0.5 −15.1 −21.5	 dB dB dB
		f = 5kHz 0dB −20dB −30dB −40dB	 −0.7 −17.3 −22.3 −30.2	 +0.3 −16.8 −21.8 −29.7	 +1.3 −16.3 −21.3 −29.2	 dB dB dB dB
		f = 20kHz 0dB −20dB −30dB	 −0.3 −18.3 −24.5	 +0.7 −17.3 −23.5	 +1.7 −16 3 −22 5	 dB dB dB
R_{IN}	Input resistance	Pin 5 Pin 2	35 3.1	50 4.2	65 5.3	kΩ kΩ
R_{OUT}	Output resistance	Pin 6 Pin 3 Pin 7	1.9	2.4 80 80	3.1 120 120	kΩ Ω Ω
	Back-to-back frequency response shift vs T_A vs V_{CC}	 0°C to −70°C 8 to 20V		 ±0.4 ±0.4		 dB dB

NOTE:
*All noise levels are measured CCIR/ARM weighted using a 10k source with respect to Dolby level See Dolby Laboratories Bulletin 19

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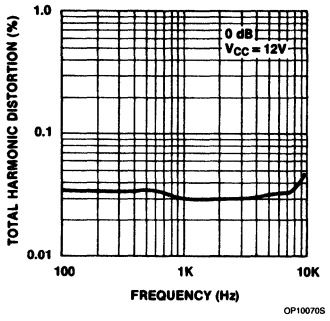
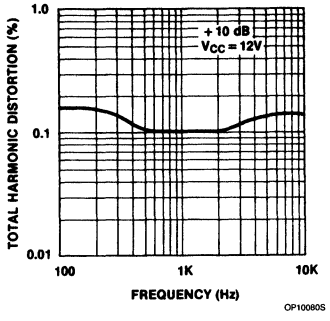
PERFORMANCE CHARACTERISTICS

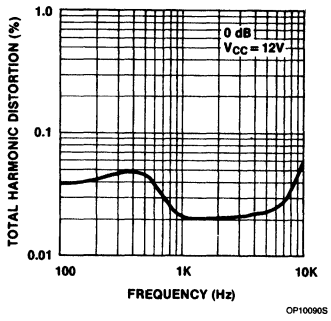
THD vs Frequency Record Mode



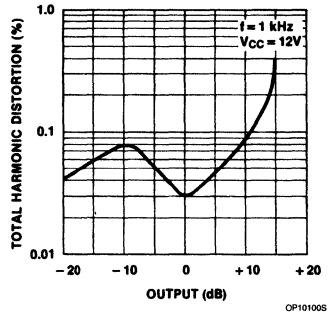
THD vs Frequency Record Mode



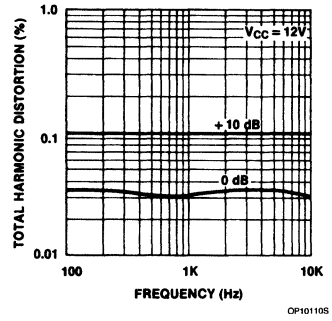
THD vs Frequency Play Mode



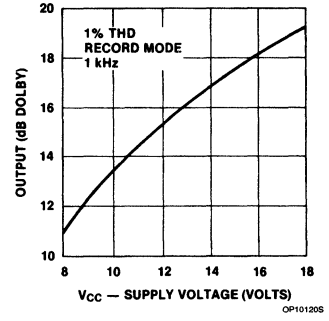
THD vs Output Record Mode



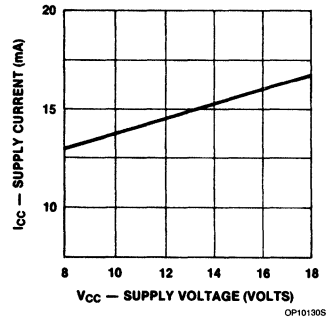
THD vs Frequency
Noise Reduction (NR) Off



Maximum Signal Handling vs
Supply Voltage



Supply Current vs
Supply Voltage



DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0 3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0 5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6 1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0 9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0 2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1 7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1 1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE:
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics Thus, no inference should be drawn on the tolerance which licensees must retain in consumer equipment The figures can, however, be used to plot typical characteristics

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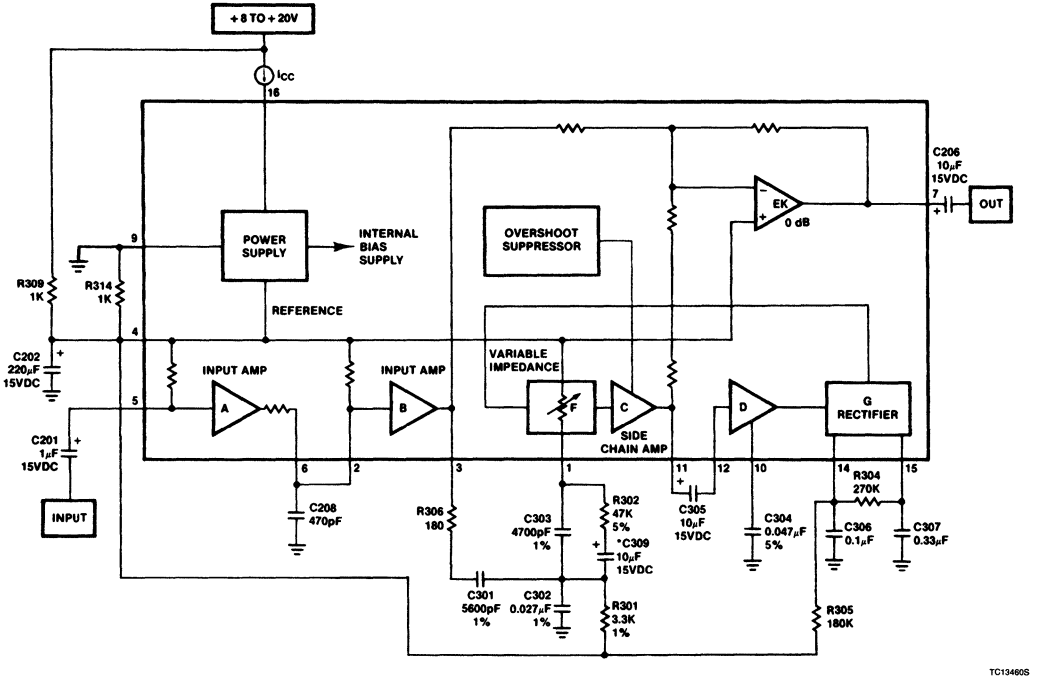
Dolby B-Type Noise Reduction Circuit NE650

TEST CIRCUIT



NOTES:
All resistors standard and are measured in Ω
*Optional capacitor in specific applications defined by Dolby Laboratories

Symbols and Definitions for Audio Power Amplifiers

Bridge-Tied Load (BTL)
An application where the outputs of two amplifiers are tied to opposite ends of a load (speaker) thereby increasing the output power level to the load.

Channel Separation
The measure of the electrical isolation between two or more independent monolithic circuits.

Input Sensitivity
The minimum signal magnitude required to drive the output to a given output power level.

Noise Output Voltage ($V_{N(RMS)}$)
The output noise voltage for a given set of conditions.

Output Power
The power available to the load for a given set of conditions.

Peak Output Current
The maximum instantaneous current available from the amplifier output.

Repetitive Peak Output Current
The maximum operating current available from the amplifier output.

Ripple Rejection (RR)
The measure of the amplifier's ability to reject influences of power supply voltage variations (ripple).

Signal-to-Noise Ratio (S/N)
The ratio of recoverable signal level to the noise level generated by the amplifier.

Standby Current (I_{SB})
The supply current drawn by the device when operated with no load.

Total Harmonic Distortion (THD)
The measure of the amplifier's ability to amplify only the input signal without introducing any harmonic interference.

Signetics

TDA1010A
6W Audio Amplifier with Preamplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIP) plastic package. The device is primarily developed as a 6W car radio amplifier for use with 4Ω and 2Ω load impedances.

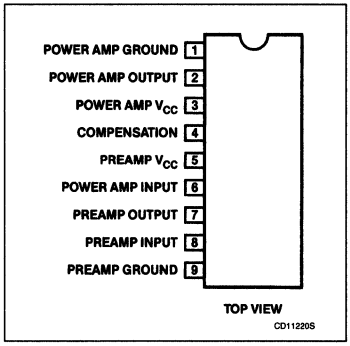
FEATURES

- **Single in-line (SIP) construction for easy mounting**
- **Separated preamplifier and power amplifier**
- **High output power**
- **Low cost external components**
- **Good ripple rejection**
- **Thermal protection**

APPLICATIONS

- **Stereo power amplifier**
- **Television**
- **Radios**
- **Intercom**
- **Alarms**
- **Modems**

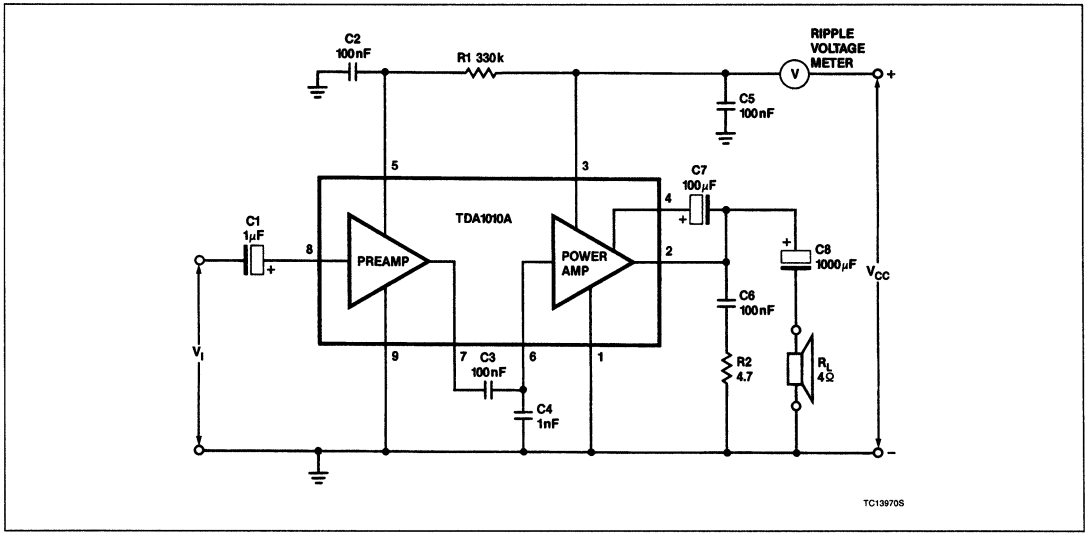
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-110B)	−25°C to +150°C	TDA1010AU

TEST CIRCUIT



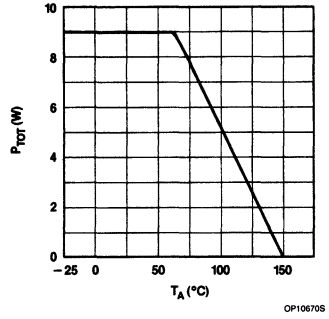


Figure 1. Power Derating Curve

HEATSINK DESIGN

Assume V_{CC} = 14.4V; R_L = 2Ω; T_A = 60°C maximum; thermal shutdown starts at T_J = 150°C. The maximum sinewave dissipation in a 2Ω load is about 5.2W. The maximum dissipation for music drive will be about 75% of the worst-case sinewave dissipation, so this will be 3.9W. Consequently, the total resistance from junction to ambient

$$\theta_{JA} = \theta_{JTAB} + \theta_{TABH} + \theta_{HA}$$

$$= \frac{150 - 60}{3.9} = 23°C/W.$$

Since θ_{JTAB} = 10°C/W and θ_{TABH} = 1°C/W,

θ_{HA} = 23 − (10 + 1) = 12°C/W.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} (MAX)	Supply voltage	24	V
I_{CC}	Peak output current	5	A
I_{CC} (Rep)	Repetitive peak output current	3	A
P_{TOT}	Total power dissipation	see derating curve in Figure 1	
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature	−25 to +150	°C
t_{SC}	AC short-circuit duration of load during sinewave drive; without heatsink at V_{CC} = 14.4V	max. 100	hours

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	6		24	V
I_{ORM}	Repetitive peak output current			3	A
I_{TOT}	Total quiescent current at V_{CC} = 14.4V		31		mA

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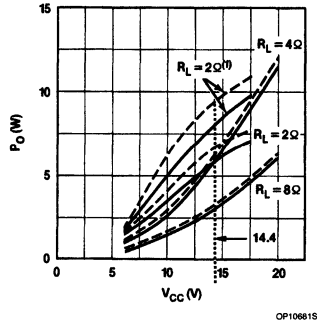
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14.4V$; $R_L = 4\Omega$; f = 1kHz, unless otherwise specified.

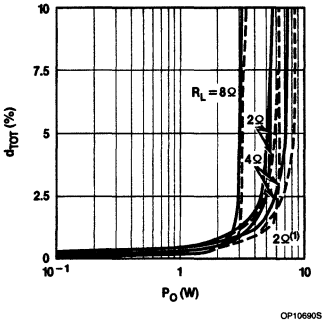
SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
P_O	$V_{CC} = 14.4V$; $R_L = 2\Omega$[1]		6.4		W
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$[1, 2]	5.9	6.2		W
P_O	$V_{CC} = 14.4V$; $R_L = 8\Omega$[1]		3.4		W
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$; without bootstrap		5.7		W
P_O	$V_{CC} = 14.4V$; $R_L = 2\Omega$; with additional bootstrap resistor of 220Ω between Pins 3 and 4		9		W
	Voltage gain				
A_{V1}	preamplifier[3]	21	24	27	dB
A_{V2}	power amplifier	27	30	33	dB
$A_{V\ TOT}$	total amplifier	51	54	57	dB
d_{TOT}	Total harmonic distortion at $P_O = 1W$		0.2		%
η	Efficiency at $P_O = 6W$		75		%
B	Frequency response (−3dB)	80Hz		15	kHz
	Input impedance				
$\|Z_I\|$	preamplifier[4]	20	30	40	kΩ
$\|Z_I\|$	power amplifier[5]	14	20	26	kΩ
$\|Z_O\|$	Output impedance of preamplifier; Pin 7[5]	14	20	26	kΩ
	Output voltage preamplifier (RMS value)				
$V_{O(RMS)}$	$d_{TOT} < 1\%$ (Pin 7)[3]	0.7			V
	Noise output voltage (RMS value)[6]				
$V_{N(RMS)}$	$R_S = 0\Omega$		0.3		mV
$V_{N(RMS)}$	$R_S = 8.2k\Omega$		0.7		mV
RR	Ripple rejection at f = 1kHz to 10kHz[7]	42			dB
RR	at f = 100Hz; C2 = 1μF	37			dB
V_I	Sensitivity for $P_O = 5.8W$		10		mV
$I_{4(RMS)}$	Bootstrap current at onset of clipping; Pin 4 (RMS value)		30		mA

NOTES:
1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_O \leqslant 3W$: $d_{TOT} \leqslant 1\%$
3. Measured with a load impedance of 20kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_O|$) is correlated (within 10%) with the input impedance ($|Z_I|$) of the power amplifier.
6. Unweighted RMS noise voltage measured at a bandwidth of 60Hz to 15kHz (12dB/octave)
7. Ripple rejection measured with a source impedance between 0 and 2kΩ (maximum ripple amplitude: 2V).
8. The tab must be electrically floating or connected to the substrate (Pin 9)



NOTES:
Solid lines indicate the power across the load, dashed lines that available at Pin 2 of the TDA1010 $R_L = 2\Omega$(1) has been measured with an additional 220Ω bootstrap resistor between Pins 3 and 4 Measurements were made at f = 1kHz, $d_{TOT} = 10\%$, $T_A = 25°C$

Figure 2. Output Power of the Test Circuit as a Function of the Supply Voltage with the Load Impedance as a Parameter; Typical Values



NOTES:
Solid lines indicate the power across the load, dashed lines that available at Pin 2 of the TDA1010. $R_L = 2\Omega$(1) has been measured with an additional 220Ω bootstrap resistor between Pins 3 and 4 Measurements were made at f = 1kHz, $V_{CC} = 14.4V$

Figure 3. Total Harmonic Distortion in the Test Circuit as a Function of the Output Power with the Load Impedance as a Parameter; Typical Values

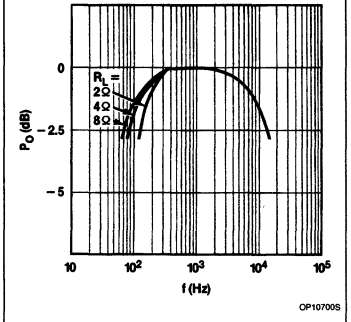
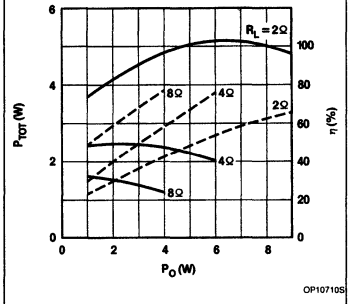


Figure 4. Frequency Characteristics of the Test Circuit for Three Values of Load Impedance. P_O Relative to 0dB = 1W; $V_{CC} = 14.4V$



NOTE:
For $R_L = 2\Omega$ an external bootstrap resistor of 220Ω has been used; typical values $V_{CC} = 14.4V$, f = 1kHz

Figure 5. Total Power Dissipation (Solid Lines) and the Efficiency (Dashed Lines) of the Test Circuit; a Function of the Output Power With the Load Impedance as a Parameter

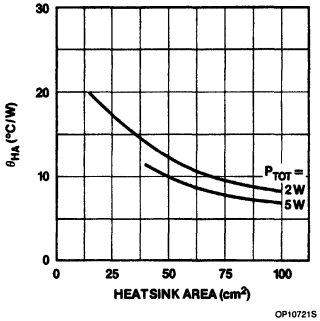


Figure 6. Thermal Resistance from Heatsink to Ambient of a 1.5mm Thick Bright Aluminum Heatsink as a Function of the Single-sided Area of the Heatsink With the Total Power Dissipation as a Parameter

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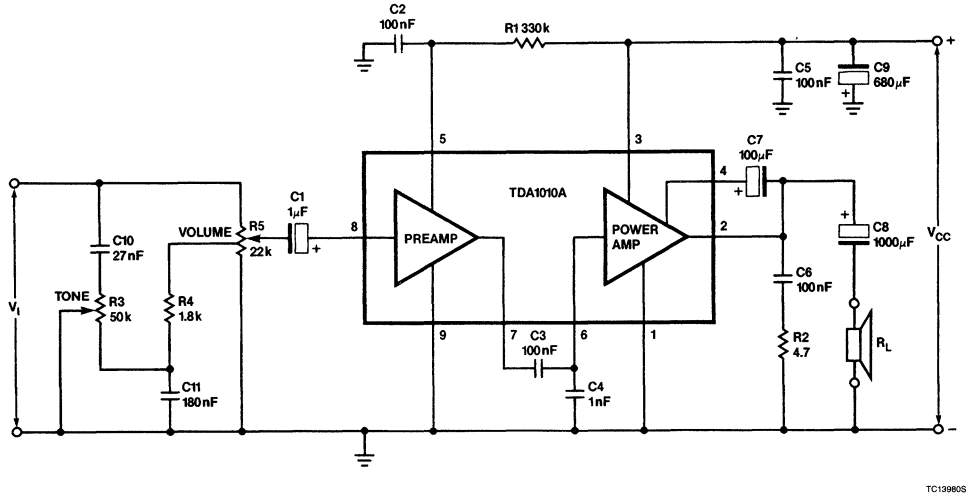


Figure 7. Complete Mono Audio Amplifier of a Radio

Signetics

TDA1011

2 to 6W Audio Power Amplifier with Preamplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIP) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4W in a 4Ω load impedance. The device can deliver up to 6W into 4Ω at 16V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24V makes this circuit very suitable for DC and AC apparatus, while the low applicable supply voltage of 3.6V permits 6V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo.

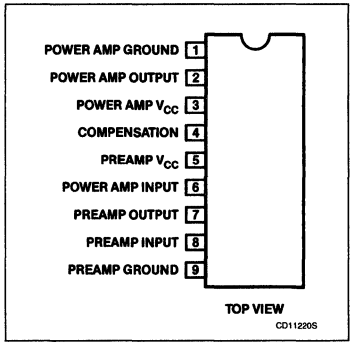
FEATURES

- **Single in-line (SIP) construction, for easy mounting**
- **Separated preamplifier and power amplifier**
- **High output power**
- **Thermal protection**
- **High input impedance**
- **Low current drain**
- **Limited noise behavior at radio frequencies**

APPLICATIONS

- **Radios**
- **Television**
- **Intercom**
- **Modems**
- **Alarms**

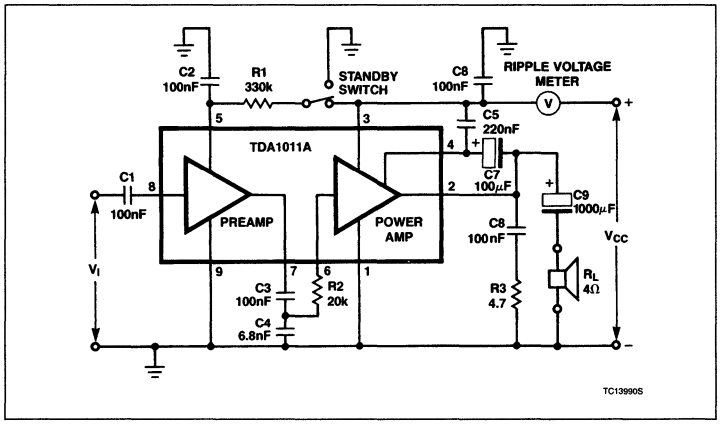
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-110B)	−25°C to +150°C	TDA1011U

TEST CIRCUIT



7

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	24	V
I_{OM}	Peak output current	3	A
P_{TOT}	Total power dissipation	see derating curve Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +150	°C
t_{SC}	AC short-circuit duration of load during sine wave drive; V_{CC} = 12V	100	hours drive; V_{CC} = 12V

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	3.6		20	V
I_{ORM}	Repetitive peak output current			2	A
I_{TOT}	Total quiescent current at V_{CC} = 12V		14	22	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 12V$; $R_L = 4\Omega$; f = 1kHz, unless otherwise specified; see also Test Circuit.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	AF output power $d_{TOT} = 10\%$ with bootstrap:				
P_O	$V_{CC} = 16V$; $R_L = 4\Omega$	3.6	6.5		W
P_O	$V_{CC} = 12V$; $R_L = 4\Omega$		4.2		W
P_O	$V_{CC} = 9V$; $R_L = 4\Omega$		2.3		W
P_O	$V_{CC} = 6V$; $R_L = 4\Omega$ without bootstrap:		1.0		W
P_O	$V_{CC} = 12V$; $R_L = 4\Omega$		3.0		W
	Voltage gain:				
A_{V1}	preamplifier[2]	21	23	25	dB
A_{V2}	power amplifier[3]	27	29	31	dB
$A_{V\ TOT}$	total amplifier[3]	50	52	54	dB
d_{TOT}	Total harmonic distortion at $P_O = 1.5W$		0.3	1	%
B	Frequency response; -3dB[4]	60Hz		15kHz	
$\|Z_{I1}\|$	Input impedance preamplifier[5]	100	200		kΩ
$\|Z_{O1}\|$	Output impedance preamplifier		1		kΩ
	Output voltage preamplifier (RMS value)				
$V_{O(RMS)}$	$d_{TOT} < 1\%$[2]	0.7			V
	Noise output voltage (RMS value)[6]				
$V_{N(RMS)}$	$R_S = 0\Omega$		0.2		mV
$V_{N(RMS)}$	$R_S = 10k\Omega$		0.6	1.4	mV
	Noise output voltage at f = 500kHz (RMS value)				
$V_{N(RMS)}$	B = 5kHz; $R_S = 0\Omega$		8		μV
	Ripple rejection[6]				
RR	f = 1 to 10kHz		42		dB
RR	f = 100Hz; C2 = 1μF	35			dB
$I_{4(RMS)}$	Bootstrap current at onset of clipping; Pin 4 (RMS value)		35		mA

NOTES:
1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20kΩ.
3. Measured with R2 = 20kΩ.
4. Measured at $P_O = 1W$; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted RMS noise voltage measured at a bandwidth of 60Hz to 15kHz (12dB/octave).

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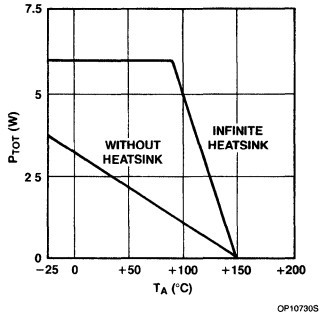


Figure 1. Power Derating Curve

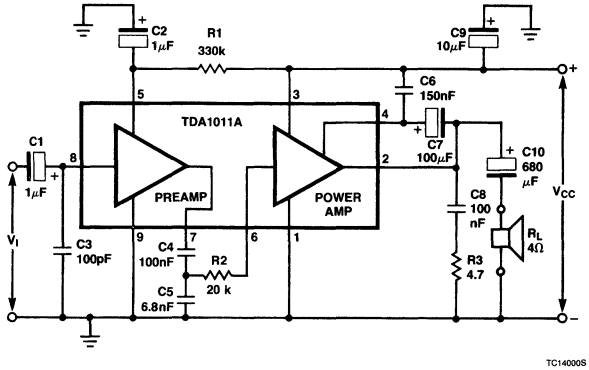


Figure 2. Circuit Diagram of a 4W Amplifier

HEATSINK DESIGN

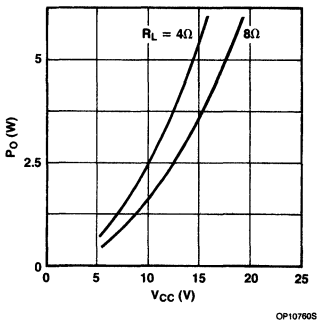
Assume V_{CC} = 12V; R_L = 4Ω; T_M = 60°C maximum; P_O = 3.8W.

The maximum sinewave dissipation is 1.8W.

The derating of 10°C/W of the package requires the following external heatsink (for sinewave drive):

$$\theta_{JA} = \theta_{JTAB} + \theta_{TABH} + \theta_{HA}$$
$$= \frac{150 - 60}{1.8} = 50°C/W.$$

Since θ_{JTAB} = 10°C/W and θ_{TABH} = 1°C/W, θ_{HA} = 50 − (10 + 1) = 39°C/W.



NOTES:
d_{TOT} = 10%, typical values The available output power is 5% higher when measured at Pin 2 (due to series resistance of C1). *

Figure 5. Output Power Across R_L as a Function of Supply Voltage with Bootstrap

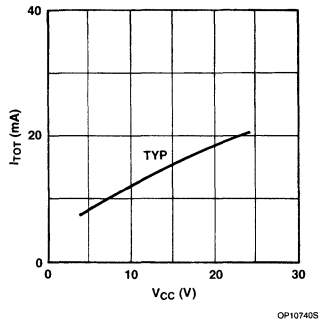
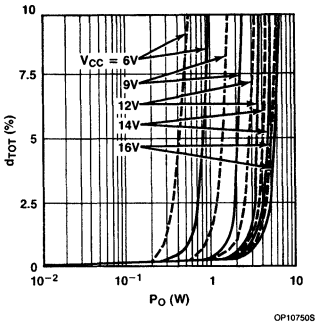
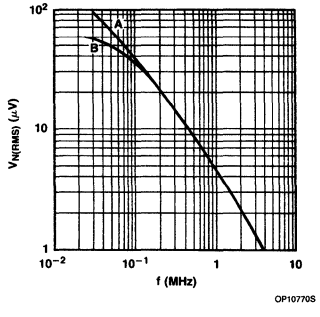


Figure 3. Total Quiescent Current as a Function of Supply Voltage



NOTES:
— with bootstrap, - - - without bootstrap, f = 1kHz, typical values The available output power is 5% higher when measured at Pin 2 (due to series resistance of C10)

Figure 4. Total Harmonic Distortion as a Function of Output Power Across R_L



NOTES:
Curve A. total amplifier, curve B power amplifier, B = 5kHz. R_S = 0, typical values

Figure 6. Noise Output Voltage as a Function of Frequency

Signetics

TDA1013A

4W Audio Amplifier with DC Volume Control

Product Specification

Linear Products

DESCRIPTION

The TDA1013A is a monolithic integrated 4W audio amplifier circuit with DC volume control in a 9-pin single in-line (SIP) plastic package. The wide supply voltage range makes this circuit very suitable for applications such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80dB. Control can be obtained by means of a variable DC voltage between 3.5 and 8V.

The audio amplifier has a well-defined open-loop gain and a fixed integrated closed-loop gain. This offers an optimum in number of external components, performance and stability.

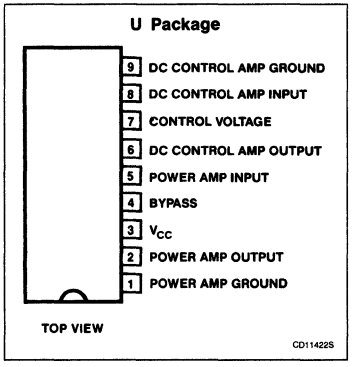
FEATURES

- **DC volume control**
- **SIP package**
- **Low distortion**
- **Logarithmic control**

APPLICATIONS

- **Computers**
- **Intercom**
- **AM/FM Radio**
- **Television**
- **Modems**

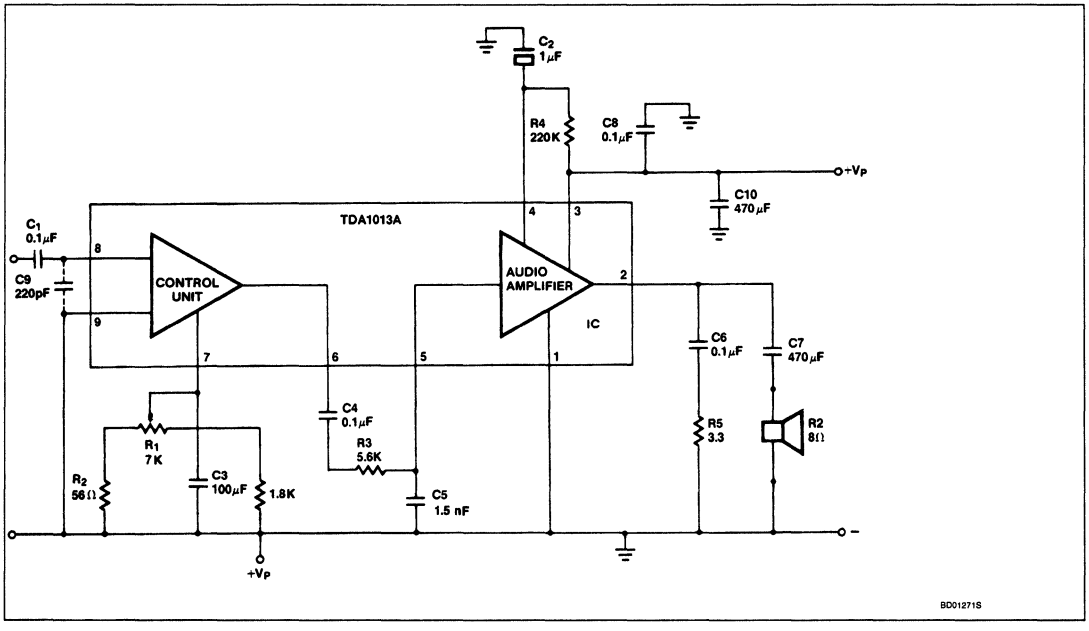
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-110B)	−25°C to +150°C	TDA1013AU

BLOCK DIAGRAM



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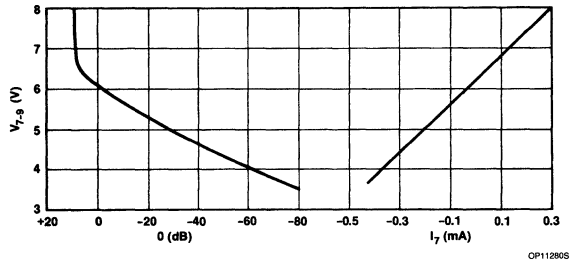
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	35	V
I_{OSM}	Non-repetitive peak output current	3	A
I_{ORM}	Repetitive peak output current	1.5	A
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature range	−25 to +150	°C
P_{TOT}	Total power dissipation	see derating curve, Figure 2	

DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 18V; R_L = 8Ω; f = 1kHz, T_A = 25°C, unless otherwise specified.

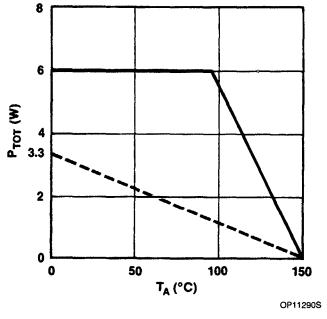
SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	15		35	V
I_{TOT}	Total quiescent current		35		mA
V_n	Noise output voltage (see note)			1.4	mV
V_I	Total sensitivity (DC control at maximum gain) for P_O = 2.5W	38	55	69	mV
f	Frequency response (−3dB)	35Hz		20	kHz
Audio amplifier					
I_{ORM}	Repetitive peak output current			1.5	A
P_O	Output power at d_{TOT} = 10%	4	4.5		W
d_{TOT}	Total harmonic distortion at P_O = 2.5W		0.5	1	%
A_V	Voltage gain		30		dB
V_I	Sensitivity for P_O = 2.5W		125		mV
$\lvert Z_I \rvert$	Input impedance (Pin 5)	100	250		kΩ
DC volume control unit					
ϕ	Gain control range (see Figure 1)	80			dB
V_I V_I	Signal handling at d_{TOT} < 1% (DC control at 0dB) sensitivity for V_O = 125mV at maximum voltage gain	1.2	 55		V mV
$\lvert Z_I \rvert$	Input impedance (Pin 8)	100	250		kΩ
$\lvert Z_O \rvert$	Output impedance (Pin 6)	100	200	400	Ω

NOTE:
Measured in a bandwidth according to IEC 179 curve 'A', R_S = 5kΩ and DC control at minimum gain



NOTE:
V_I at Pin 7

Figure 1. Typical Values Gain Control



NOTE:
——— Infinite heatsink
- - - - Without heatsink

Figure 2. Power Derating Curve

HEATSINK DESIGN

Assume V_{CC} = 18V; R_L = 8Ω; T_A = 60°C (maximum); T_J = 150°C (maximum); for a 4W application into an 8Ω load, the maximum dissipation is about 2.5W. The thermal resistance from junction to ambient can be expressed as:

$$\theta_{JA} = \theta_{JTAB} + \theta_{TABH} + \theta_{HA}$$

$$= \frac{T_{J\ MAX} - T_{A\ MAX}}{P_{MAX}} = \frac{150 - 60}{2.5} = 36°C/W.$$

Since θ_{JTAB} = 9°C/W and θ_{TABH} = 1°C/W, θ_{HA} = 36 – (9 + 1) = 26°C/W.

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Signetics

AN148
Audio Amplifier with TDA1013A

Application Note

Linear Products

Author: D. Udo

ABSTRACT

The 9-pin SOT-110B-encapsulated TDA1013A is an audio power amplifier that has a DC volume control on-board. The device is designed for audio amplifier applications in TV sound channels.

At a supply voltage of 18V, the output power is about 4.4W into an 8Ω loudspeaker.

The gain control range is > 80dB with a DC control voltage from 8 to 3.5V.

Some basic information of the TDA1013A is dealt with in this application note. Detailed performance properties are given for an 18V into 8Ω application.

INTRODUCTION

The TDA1013A has two functions: a DC volume control and audio power amplifier.

Some performance characteristics are:

- Supply voltage range 15 – 35V
- Max. repetitive peak current 1.5A
- Max. non-repetitive peak current 3A
- θ_{JTAB} 9°C
- θ_{JA} 45°C
- Input impedance (Pins 5 and 8) 100kΩ
- Output impedance (Pin 6) 200Ω (typ.)
- Voltage gain DC control part (Pins 8 to 6) 7dB
- Voltage gain power amplifier (Pins 5 to 2) 30dB

APPLICATION CIRCUIT

The complete application circuit is given in Figure 1. With high input impedance, C_9 is necessary to filter-out RF input interferences. R_3 in combination with C_5 is used to limit the AF frequency bandwidth. The 470μF power supply decoupling capacitor is C_{10}.

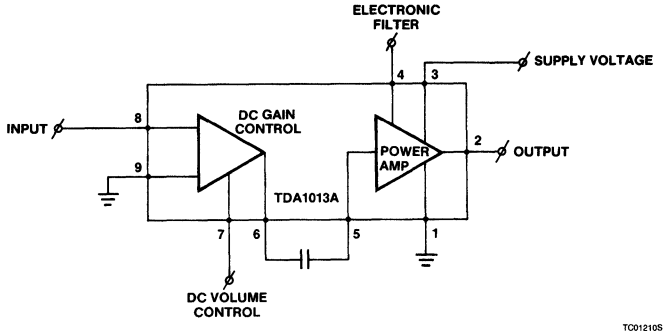

Figure 1

Audio Amplifier with TDA1013A AN148

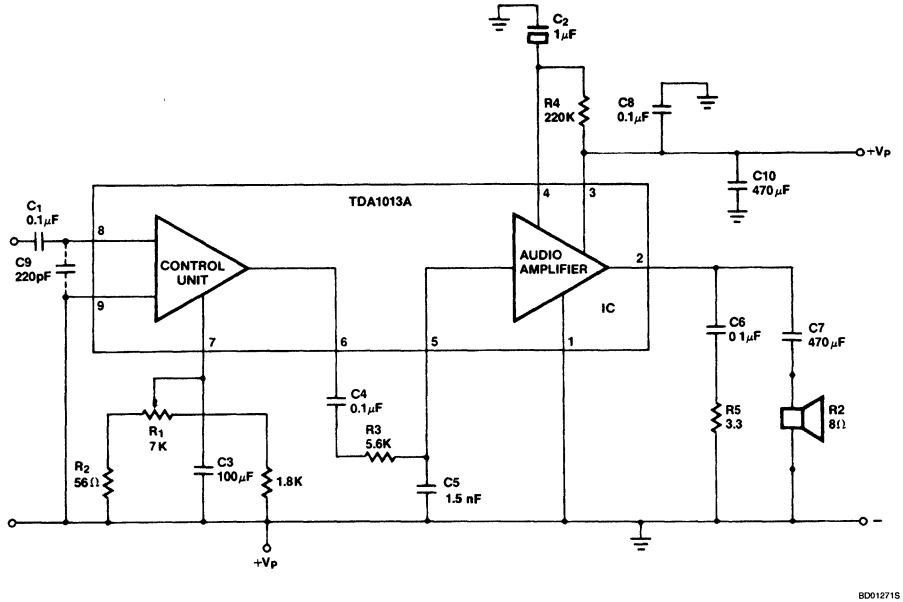

Figure 2. Block Diagram and External Components

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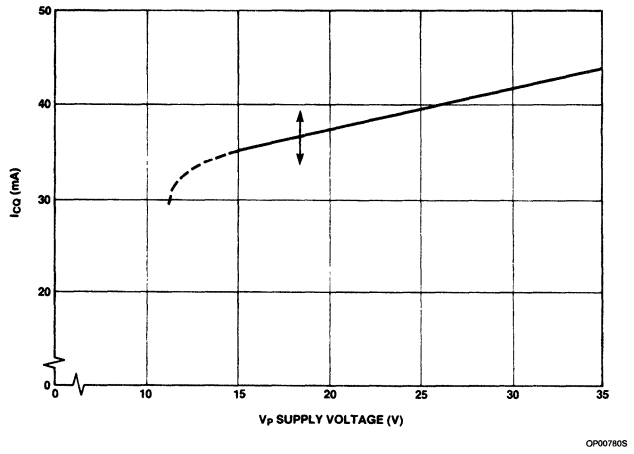

Figure 3. Quiescent Current vs V_{CC}

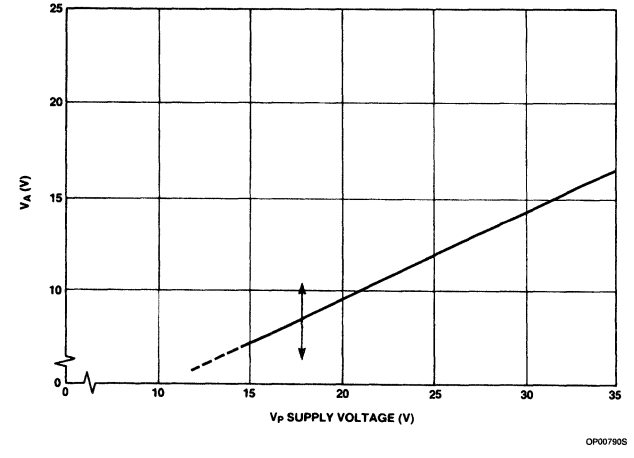

Figure 4. Midtap Voltage vs V_{CC}

MEASUREMENTS

Various measurements made in the circuit of Figure 1 are given. If not otherwise stated, the measurements are done at V_{CC} = 18V, R_L = 8Ω, f = 1kHz and T_A = 25°C.

Quiescent Current Consumption

The quiescent current as a function of V_{CC} is given in Figure 3. At V_{CC} = 18V the maximum spread on 20 samples is indicated by arrows.

Midtap Voltage

The midtap voltage V_A versus V_{CC} at output Pin 2 is shown in Figure 4.

Output Power and Dissipation

The output power for d = 10% as a function of V_{CC} at Pin 2 and across the 8Ω loudspeaker load is given in Figure 5. The upper curve gives the worst-case sinewave dissipation. The dissipation versus output power for V_{CC} = 18V is given in Figure 6.

Distortion

The total harmonic distortion as a function of P_O is shown in Figure 7 for signal frequencies of 1 and 10kHz (DC control voltage at Pin 7 is constant 8V). In Figure 8 the same curve is given for f = 1kHz but now the output power is reduced by the DC control voltage (at d = 10% V_{DC} Pin 7 = 8V). The distortion for 2.5W output power versus frequency is given in Figure 11. In Figure 9, the distortion of the DC gain-controlled preamplifier as a function of the signal excursion at Pin 6 is shown for a DC control voltage (V_{DC} Pin 7) of 8V.

Audio Amplifier with TDA1013A AN148

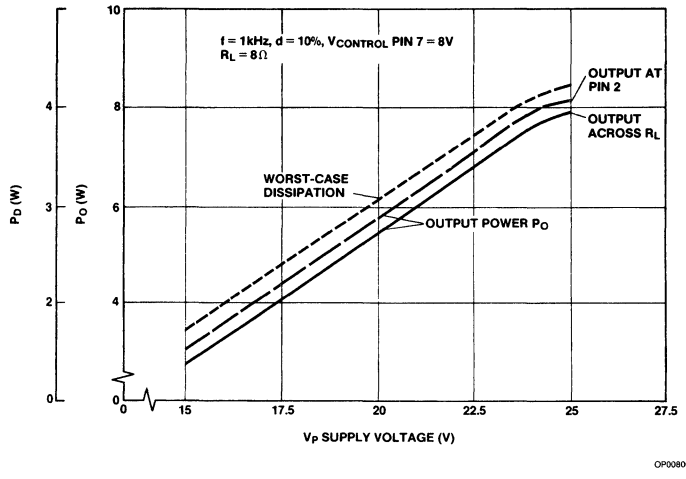

Figure 5. Output Power and Dissipation vs V_{CC}

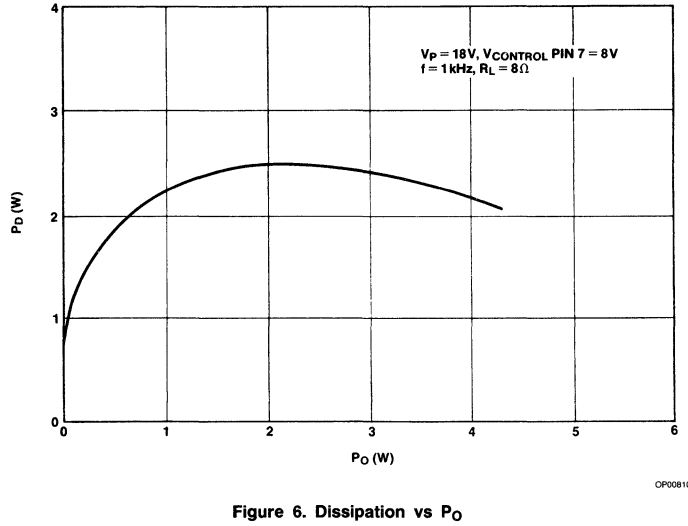

Figure 6. Dissipation vs P_O

Gain Control

The typical overall voltage gain (V_{DC} Pin 7 = 8V) is 38dB. The gain control curve versus the DC control voltage on Pin 7 is shown in Figure 10.

Frequency Characteristic

The frequency characteristic is presented in Figure 12. The – 3dB bandwidth is from 32Hz to 20kHz.

Power Bandwidth

The power bandwidth (d = 10%) is given in Figure 13. The low frequency behavior is determined by the value of the output electrolytic C_7.

Supply Voltage Ripple Rejection

The supply voltage ripple rejection versus frequency is shown in Figure 14 for $R_S = 0$ and 10kΩ. Ripple voltage on Pin 3 is 500mV_{RMS}.

Noise Behavior

The A-weighted, IEC 179 standard, signal-to-noise ratio at maximum gain (V_{DC} Pin 7 = 8V) is 68dB at $R_S = 0\Omega$ and related to P_O = 2.5W. Increasing R_S has hardly any influence on this noise level. Typical S/N is 74dB.

CONCLUSION

The TDA1013A is a suitable IC as an audio amplifier in TV receivers. It delivers an output power of about 4.4W in $R_L = 8\Omega$ at V_{CC} = 18V. An 80dB DC gain control is incorporated.

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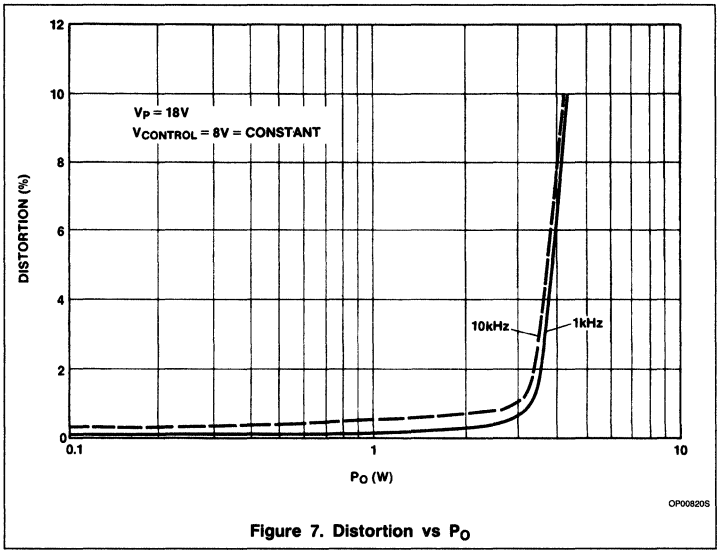

Figure 7. Distortion vs P_O

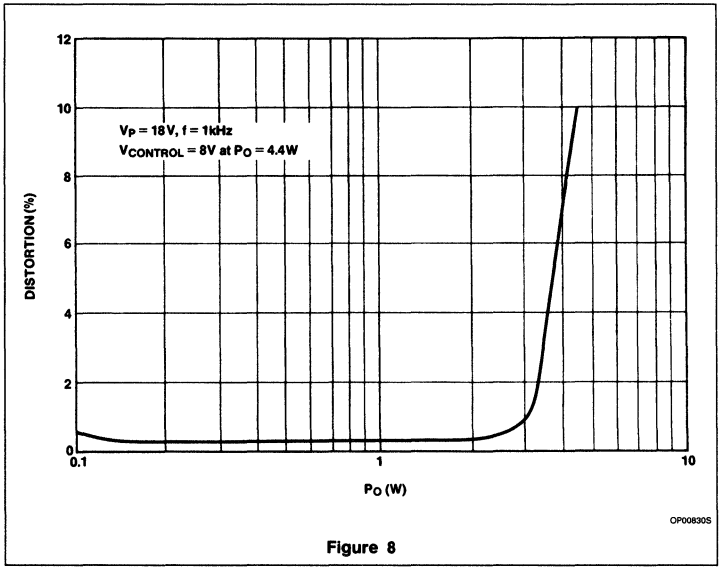

Figure 8

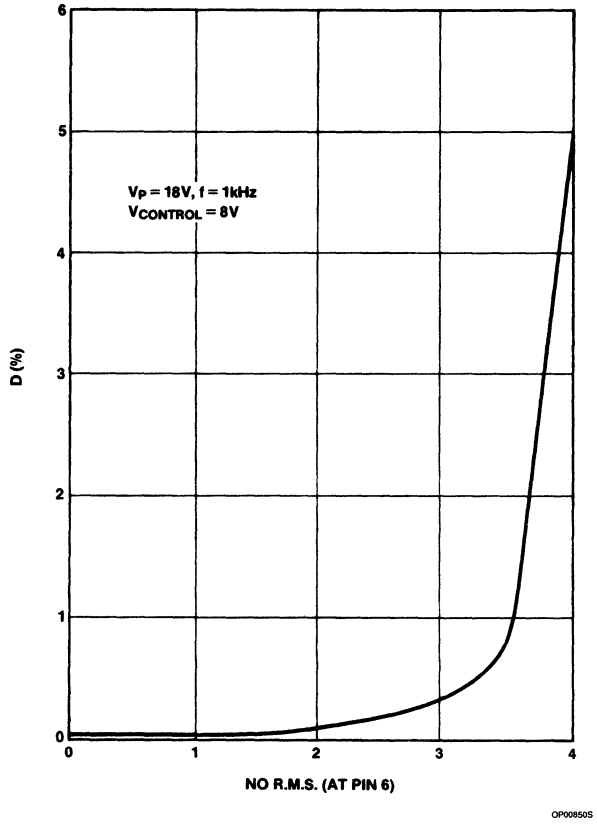

Figure 9. Distortion of Control Amplifier at Pin 6

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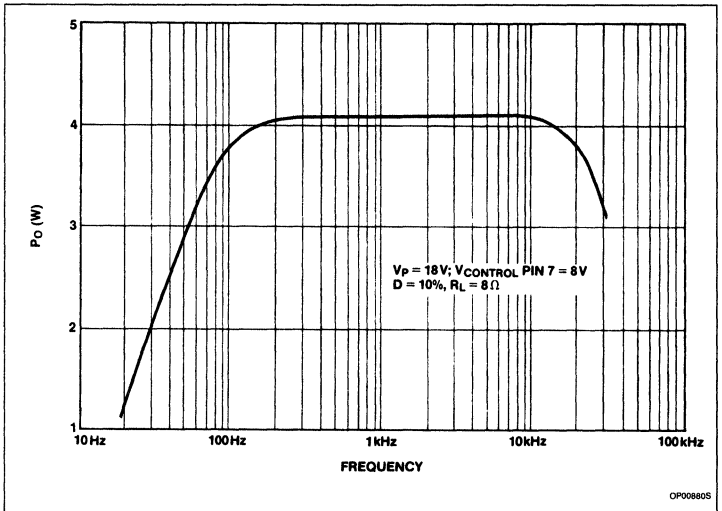

Figure 10. Typical Control Curve DC Control Voltage at Pin 7

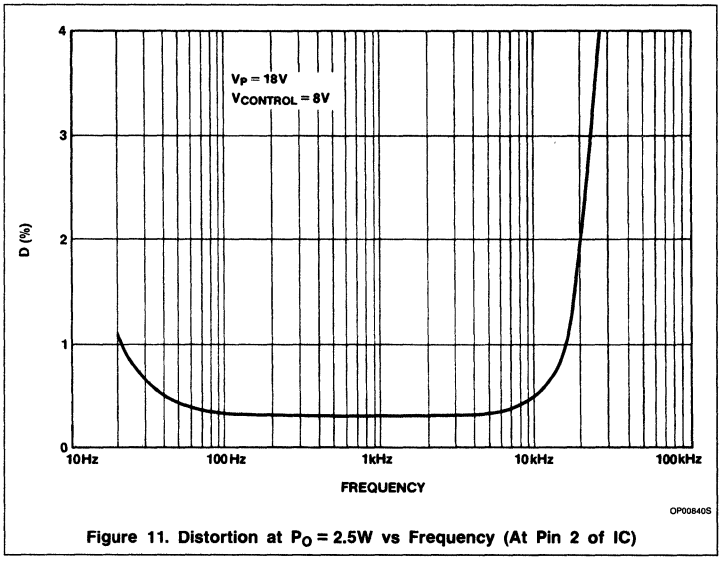

Figure 11. Distortion at P_O = 2.5W vs Frequency (At Pin 2 of IC)

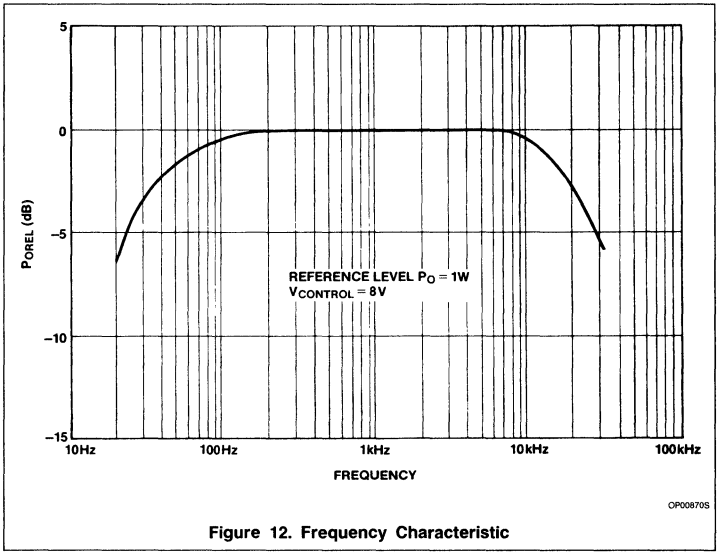

Figure 12. Frequency Characteristic

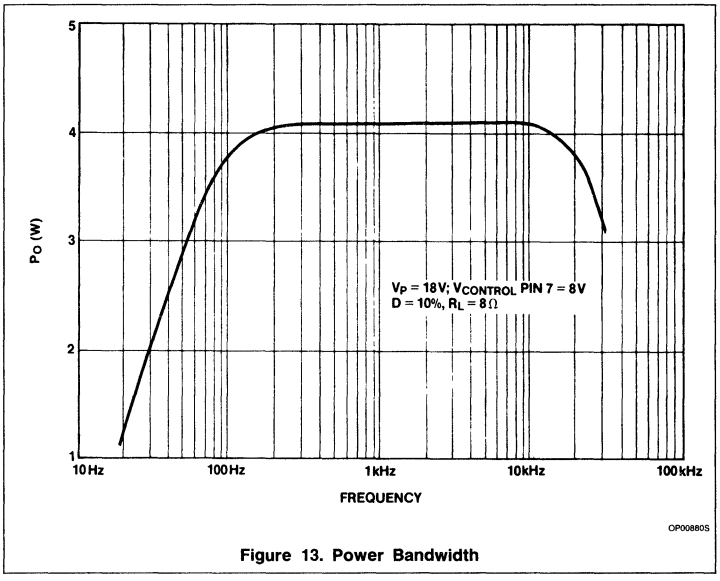

Figure 13. Power Bandwidth

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Audio Amplifier with TDA1013A AN148

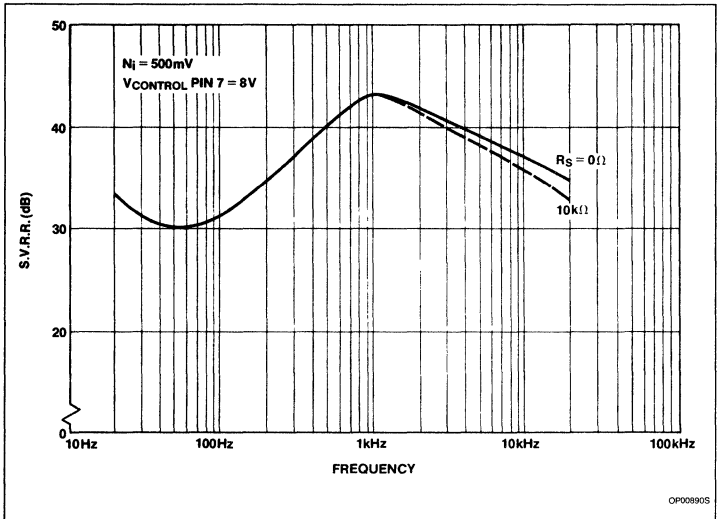


Figure 14. Ripple Rejection vs Frequency

Signetics

TDA1015
1 to 4W Audio Amplifier with Preamplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1015 is a monolithic integrated 1 to 4W audio amplifier with preamplifier circuit in a 9-pin single in-line (SIP) plastic package. The device is especially designed for low voltage applications and delivers up to 4W in a 4Ω load impedance.

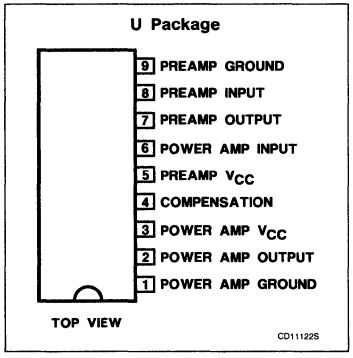
FEATURES

- **Single in-line (SIP) construction for easy mounting**
- **Separated preamplifier and power amplifier**
- **High output power**
- **Thermal protection**
- **High input impedance**
- **Low current drain**
- **Limited noise behavior at radio frequencies**

APPLICATIONS

- **Intercoms**
- **Tape recorders and players**
- **AM/FM radio**
- **Alarms**
- **Speech synthesizer output**
- **Telephone amplifier**

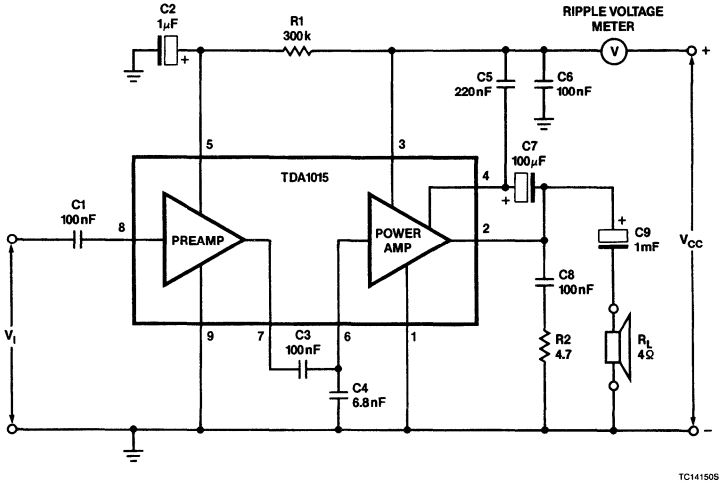
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-110B)	−25°C to +150°C	TDA1015U

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{OM}	Peak output current	2.5	A
P_{TOT}	Total power dissipation	see derating curve, Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +150	°C
t_{SC}	AC short-circuit duration of load during sine-wave drive; V_{CC} = 12V	100	hours

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	3.6		18	V
I_{ORM}	Repetitive peak output current			2	A
I_{TOT}	Total quiescent current at V_{CC} = 12V		14	25	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C; V_{CC} = 12V; R_L = 4Ω; f = 1kHz, unless otherwise specified; see also Figure 2.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	AF output power at d_{TOT} = 10%[1] with bootstrap:				
P_O	V_{CC} = 12V; R_L = 4Ω		4.2		W
P_O	V_{CC} = 9V; R_L = 4Ω		2.3		W
P_O	V_{CC} = 6V; R_L = 4Ω		1.0		W
P_O	V_{CC} = 12V; R_L = 4Ω without booststrap		3.0		W
	Voltage gain:				
A_{V1}	Preamplifier[2]		23		dB
A_{V2}	Power amplifier		29		dB
$A_{V\ TOT}$	Total amplifier	49	52	55	dB
d_{TOT}	Total harmonic distortion at P_O = 1.5W		0.3	1.0	%
B	Frequency response −3dB[3]	60Hz		15	kHz
	Input impedance				
$\lvert Z_{I1}\rvert$	Preamplifier[4]	100	200		kΩ
$\lvert Z_{I2}\rvert$	Power amplifier		20		kΩ
$\lvert Z_{O1}\rvert$	Output impedance preamplifier		1		kΩ
$V_{O(RMS)}$	Output voltage preamplifier (RMS value) d_{TOT} < 1%[2]		0.8		V
	Noise output voltage (RMS value)[5]				
$V_{n(RMS)}$	R_S = 0Ω		0.2		mV
$V_{n(RMS)}$	R_S = 10kΩ		0.5		mV
	Noise output voltage at f = 500kHz (RMS value)				
$V_{n(RMS)}$	B = 5kHz; R_S = 0Ω		8		μV
RR	Ripple rejection[6] f = 100Hz		38		dB

NOTES:
1. Measured with an ideal coupling capacitor to the speaker load
2. Measured with a load resistor of 20kΩ.
3. Measured at P_O = 1W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier
5. Unweighted RMS noise voltage measured at a bandwidth of 60Hz to 15kHz (12dB/octave)
6. Ripple rejection measured with a source impedance between 0 and 2kΩ (maximum ripple amplitude. 2V)
7. The tab must be electrically floating or connected to the substrate (Pin 9)

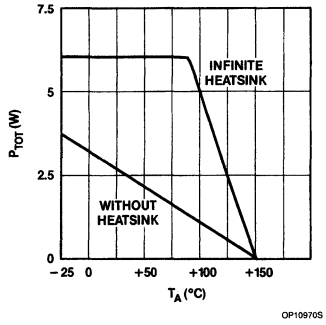


Figure 1. Power Derating Curve

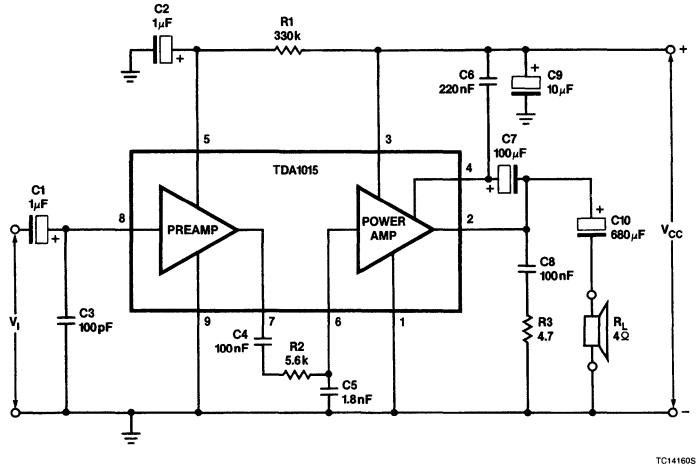


Figure 2. Circuit Diagram of a 1 to 4W Amplifier

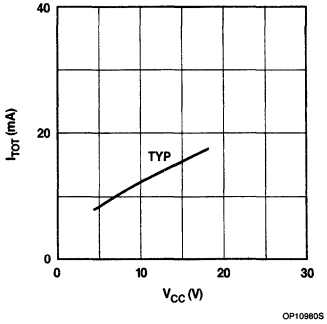


Figure 3. Total Quiescent Current as a Function of Supply Voltage

HEATSINK DESIGN

Assume $V_{CC} = 12V$, $R_L = 4\Omega$, $T_A = 45°C$ maximum.

The maximum sine-wave dissipation is 1.8W.

$$\theta_{JA} = \theta_{JTAB} + \theta_{TABH} + \theta_{HA} = \frac{150 - 45}{1.8} = 58°C/W$$

Where θ_{JA} of the package is 45°C/W, no external heatsink is required

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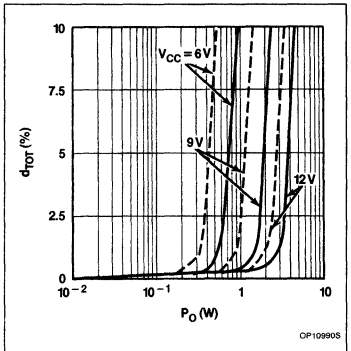
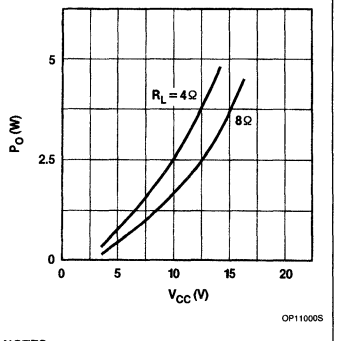


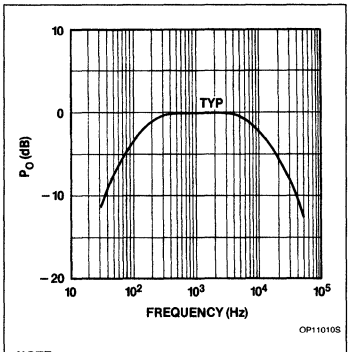
NOTES:
——— With Bootstrap,
- - - - Without Bootstrap,
f = 1kHz, typical values
The available output power is 5% higher when measured at Pin 2 (due to series resistance of C10)

Figure 4. Total Harmonic Distortion as a Function of Output Power Across R_L



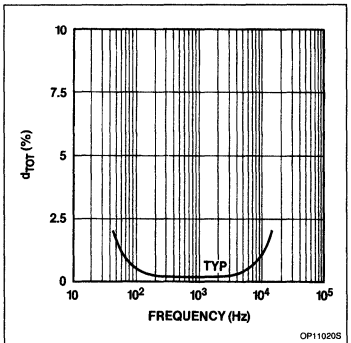
NOTES:
1 d_{TOT} = 10%, Typical Values
2 The available output power is 5% higher when measured at Pin 2 (due to series resistance of C10)

Figure 5. Output Power Across R_L as a Function of Supply Voltage with Bootstrap



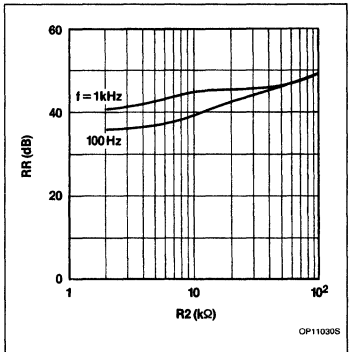
NOTE:
P_O Relative to 0dB = 1W, V_{CC} = 12V, R_L = 4Ω

Figure 6. Voltage Gain as a Function of Frequency



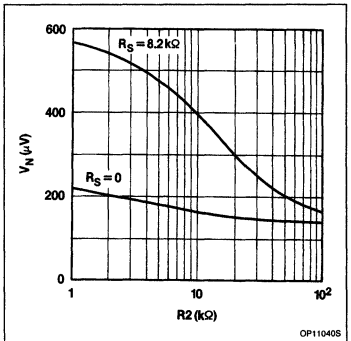
NOTE:
P_O = 1W, V_{CC} = 12V, R_L = 4Ω

Figure 7. Total Harmonic Distortion as a Function of Frequency



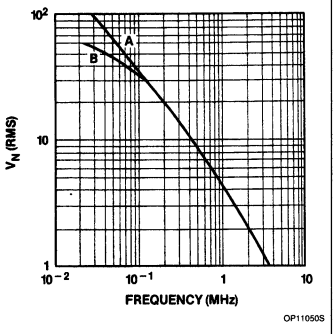
NOTE:
R_S = 0, Typical Values

Figure 8. Ripple Rejection as a Function of R2 (see Figure 2)



NOTE:
Measured according to A-Curve, capacitor C5 is adapted for obtaining a constant bandwidth

Figure 9. Noise Output Voltage as a Function of R2 (see Figure 2)



NOTE:
Curve a total amplifier, curve b, power amplifier, B = 5kHz, R_S = 0, typical values

Figure 10. Noise Output Voltage as a Function of Frequency

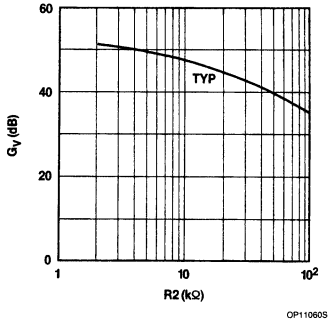


Figure 11. Voltage Gain as a Function of R2 (see Figure 2)

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Signetics

TDA1020
12W Audio Amplifier with Preamplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1020 is a monolithic integrated 12W audio amplifier in a 9-lead single in-line (SIP) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_{CC} = 14.4V, an output power of 7W can be delivered into a 4Ω load and 12W into 2Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18V also makes the IC suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18V (< 45V), the device will not be damaged (load dump protected). Also, a short-circuiting of the output to ground (AC) will not destroy the device. Thermal protection is built in.

As a special feature, the circuit has a low standby current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

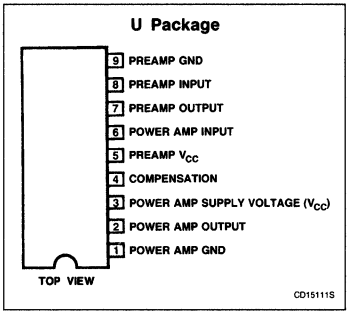
FEATURES

- **Load dump protected**
- **Short-circuit protected**
- **Standby mode**
- **High output power**
- **Single in-line (SIP) package**

APPLICATIONS

- **Auto radio**
- **Modems**
- **Television**
- **Intercom**
- **Telephone amplifier**
- **Alarms**

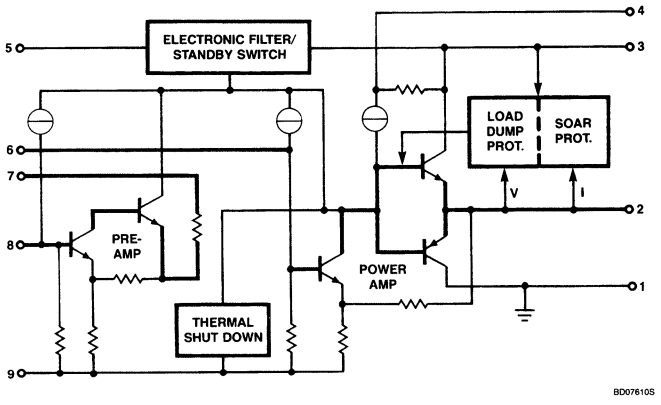
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-110B)	−25°C to +150°C	TDA1020U

BLOCK DIAGRAM



NOTE:
The heavy lines indicate the signal paths

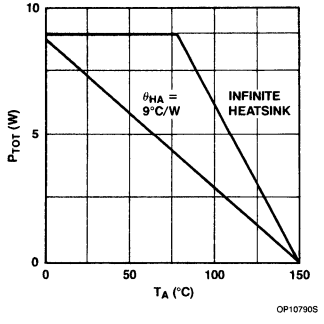


Figure 1. Power Derating Curves

HEATSINK DESIGN EXAMPLE

The derating of 8°C/W of the encapsulation requires the following external heatsink (for sine wave drive):

10W in 2Ω at V_{CC} = 14.4V

Maximum sine wave dissipation: 5.2W

T_A = 60°C maximum

$$\theta_{JA} = \theta_{JTAB} + \theta_{TABH} + \theta_{HA} = \frac{150 - 60}{5.2}$$

$$= 17.3°C/W$$

Since $\theta_{JTAB} + \theta_{TABH} = 8°C/W$,

$\theta_{HA} = 17.3 - 8 \approx 9°C/W$.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage; operating (Pin 3)	18	V
V_{CC}	Supply voltage; non-operating	28	V
V_{CC}	Supply voltage; load dump	45	V
I_{OSM}	Non-repetitive peak output current	6	A
P_{TOT}	Total power dissipation	See derating curves, Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_C	Crystal temperature	150	°C
t_{SC}	Short-circuit duration of load behind output electrolytic capacitor at 1kHz sine-wave overdrive (10dB); V_{CC} = 14.4V	100	hours

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DC ELECTRICAL CHARACTERISTICS

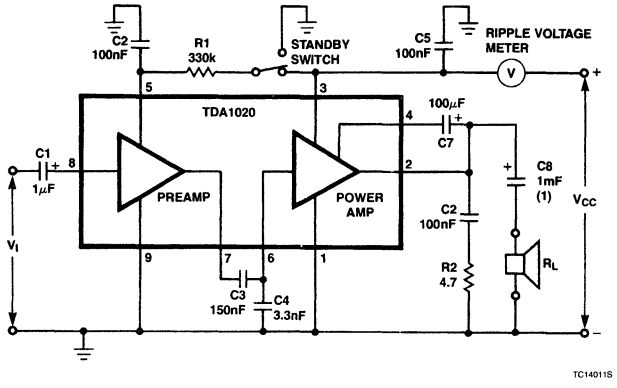
SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range (Pin 3)	6		18	V
I_{ORM}	Repetitive peak output current			4	A
	Total quiescent current				
I_{TOT}	at V_{CC} = 14.4V		30		mA
I_{TOT}	at V_{CC} = 18V		40		mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = 14.4V; R_L = 4Ω; f = 1kHz, unless otherwise specified; see also Figure 2.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Output power at d_{TOT} = 10%; with bootstrap[1]				
P_O	V_{CC} = 14.4V; R_L = 2Ω	10	12		W
P_O	V_{CC} = 14.4V; R_L = 4Ω	6	7		W
P_O	V_{CC} = 14.4V; R_L = 8Ω		3 5		W
	Output power at d_{TOT} = 1%; with bootstrap[1]				
P_O	V_{CC} = 14.4V; R_L = 2Ω				W
P_O	V_{CC} = 14.4V; R_L = 4Ω				W
P_O	V_{CC} = 14.4V; R_L = 8Ω				W
	Output voltage (RMS value)				
$V_{O(RMS)}$	R_L = 1kΩ; d_{TOT} = 0.5%		5		V
P_O	Output power at d_{TOT} = 10%; without bootstrap	4.5			W
	Voltage gain				
A_V[1]	Preamplifier[2]	16.7	17.7	18.7	dB
A_V[2]	Power amplifier	28.5	29.5	30.5	dB
$A_{V\ TOT}$	Total amplifier	46.2	47	48.2	dB
	Input impedance				
$\|Z_I\|$	Preamplifier	28	40	52	kΩ
$\|Z_I\|$	Power amplifier	28	40	52	kΩ
	Output impedance				
$\|Z_O\|$	Preamplifier	1.4	2.0	2.6	kΩ
$\|Z_O\|$	Power amplifier		50		mΩ
	Output voltage (RMS value) at d_{TOT} = 1%				
$V_{O(RMS)}$	Preamplifier[2]	1 0	1.5		V
B	Frequency response	50Hz		25	kHz
	Noise output voltage (RMS value)[3]				
$V_{N(RMS)}$	R_S = 0Ω		0.3	0.5	mV
$V_{N(RMS)}$	R_S = 8.2kΩ		0.5	1.0	mV
	Ripple rejection[4]				
RR	At f = 100Hz; C2 = 1μF		44		dB
RR	At f = 1kHz to 10kHz	48	54		dB
	Bootstrap current at onset of clipping (Pin 4)				
I_4	R_L = 4Ω and 2Ω		40		mA
I_{SB}	Standby current[5]			1	mA
T_C	Crystal temperature for −3dB gain	150			°C

NOTES:
1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40kΩ
3. Measured according to IEC curve A
4. Maximum ripple amplitude is 2V, input is short-circuited
5. Total current when disconnecting Pin 5 or short-circuited to ground (Pin 9).
6. The tab must be electrically floating or connected to the substrate (Pin 9)



NOTE:
With $R_L = 2\Omega$, preferred value of C8 = 2200μF

Figure 2. Test Circuit

7

Signetics

TDA1510
2 × 12W Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1510 is a monolithic integrated class B output amplifier in a 13-pin single in-line (SIP) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage V_{CC} = 14.4V, an output power of 24W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as stereo amplifier, it delivers 2 × 12W into 2Ω or 2 × 7W into 4Ω.

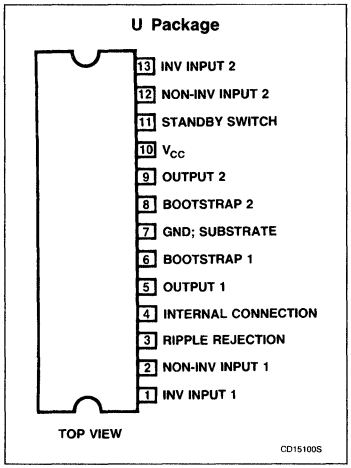
FEATURES

- **Flexibility in use — stereo as well as mono BTL**
- **High output power**
- **Low offset voltage at the output (important for BTL)**
- **Large useable gain variation**
- **Very good ripple rejection**
- **Load dump protection**
- **AC short-circuit safe to ground**
- **Thermal protection**
- **Internal limited bandwidth for high frequencies**
- **Low standby current possibility, to simplify required switches**
- **Low number and small sized external components**
- **High reliability**

APPLICATIONS

- **Car radios**
- **Low-impedance loads**
- **Stereo amplifiers**

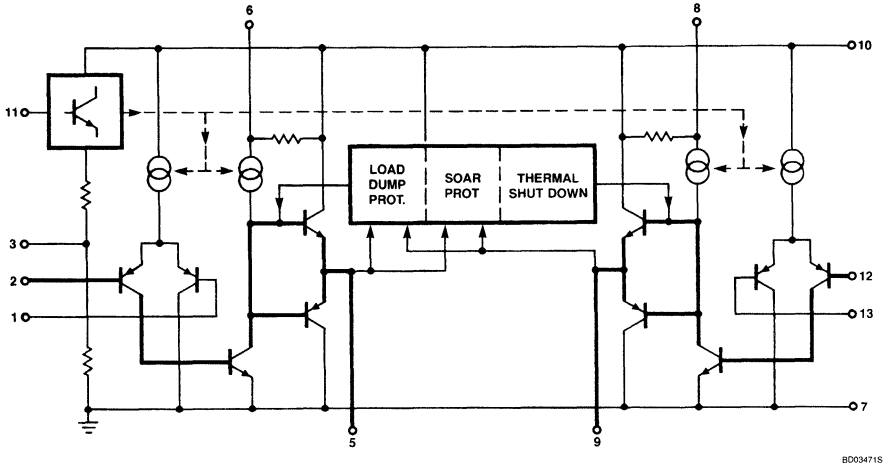
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
13-Pin Plastic SIP (SOT-141B)	0 to +70°C	TDA1510U

BLOCK DIAGRAM



NOTE:
Internal Block Diagram, the heavy lines indicate the signal paths Pin 4 is internally connected

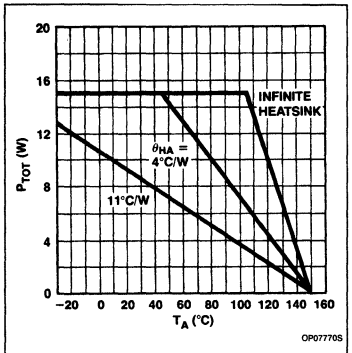


Figure 1. Power Derating Curves

HEATSINK DESIGN EXAMPLE

The derating of 3°C/W of the encapsulation requires the following external heatsink (for sine wave drive):

24W BTL (4Ω) or 2 × 12W stereo (2Ω)

maximum sine wave dissipation: 12W

T_A = 65°C maximum

$$\theta_{HA} = \frac{150 - 65}{12} - 3 = 4°C/W.$$

2 × 7W stereo (4Ω)

maximum sine wave dissipation: 6 W

T_A = 65°C maximum

$$\theta_{HA} = \frac{150 - 65}{6} - 3 = 11°C/W.$$

ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage, operating (Pin 10)	18	V
V_{CC}	Supply voltage, non-operating	28	V
V_{CC}	Supply voltage during 50ms (load dump protection)	45	V
I_{OM}	Peak output current	6	A
P_D	Total power dissipation	(see derating curve Figure 1)	
T_{STG}	Storage temperature range	−65 to +150	°C
T_C	Crystal temperature	150	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range (Pin 10)	6		18	V
I_{ORM}	Repetitive peak output current			4	A
I_{TOT}	Total quiescent current		75	120	mA
I_{SB}	Standby current			2	mA
I_{SO}	Switch-on current (Pin 11) at $V_{11} \leqslant V_{10}$[1]		0.35	0.8	mA

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AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14.4V$; f = 1kHz, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Bridge-tied load application (BTL) (see Figure 2)					
	Output power at $R_L = 4\Omega$ (with bootstrap)				
P_O	$V_{CC} = 14.4V$; $d_{TOT} = 0.5\%$	15.5	18.0		W
P_O	$V_{CC} = 14.4V$; $d_{TOT} = 10\%$	20	24		W
P_O	$V_{CC} = 13.2V$; $d_{TOT} = 0.5\%$		15		W
P_O	$V_{CC} = 13.2V$; $d_{TOT} = 10\%$		20		W
G_O	Open-loop voltage gain		75		dB
G_C	Closed-loop voltage gain[2]	39.5	40	40.5	dB
B	Frequency response at −3dB[3]	20	20,000		Hz
$\|Z_i\|$	Input impedance[4]	1			MΩ
	Noise input voltage (RMS value) at f = 20Hz to 20kHz				
$V_{n(RMS)}$	$R_S = 0\Omega$		0.2		mV
$V_{n(RMS)}$	$R_S = 10k\Omega$		0.35	0.8	mV
V_n	$R_S = 10k\Omega$; according to IEC179 curve A		0.25		mV
	Supply voltage ripple rejection[5]				
RR	f = 100Hz	42	50		dB
$\|\Delta V_{5-9}\|$	DC output offset voltage between the outputs		2	50	mV
	Loudspeaker protection (if one of the 2 outputs is short-circuited to ground)				
$\|\Delta V_{5-9}\|$	Maximum DC voltage (across the load)			1	V
B	Power bandwidth; −1dB; $d_{TOT} = 0.5\%$	30	40,000		Hz
Stereo application (see Figure 4)					
	Output power at $d_{TOT} = 10\%$; with bootstrap[6]				
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$	6	7		W
P_O	$V_{CC} = 14.4V$; $R_L = 2\Omega$	6	12		W
P_O	$V_{CC} = 13.2V$; $R_L = 4\Omega$		6		W
P_O	$V_{CC} = 13.2V$; $R_L = 2\Omega$		10		W
	Output power at $d_{TOT} = 0.5\%$; with bootstrap[6]				
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$		5.5		W
P_O	$V_{CC} = 14.4V$; $R_L = 2\Omega$		9.0		W
P_O	$V_{CC} = 13.2V$; $R_L = 4\Omega$		4.5		W
P_O	$V_{CC} = 13.2V$; $R_L = 2\Omega$		7.5		W
	Output power at $d_{TOT} = 10\%$; without bootstrap				
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$[6, 8, 9]		6		W
B	Frequency response; −3dB[3]	40	20,000		Hz
RR	Supply voltage ripple rejection[5] f = 1kHz		50		dB
α	Channel separation; $R_S = 10k\Omega$; f = 1kHz	40	50		dB
G_C	Closed-loop voltage gain[7]		40	40.5	dB
	Noise output voltage (RMS value) at f = 20Hz to 20kHz				
$V_{n(RMS)}$	$R_S = 0\Omega$		0.15		mV
$V_{n(RMS)}$	$R_S = 10k\Omega$		0.25		mV
V_n	$R_S = 10k\Omega$; according to IEC179 curve A		0.2		mV

NOTES:

1. If $V_{11} > V_{10}$, then I_{11} must be $\leq 10mA$.
2. Closed-loop voltage gain can be chosen between 32 and 56dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Figure 3) is typically 100kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0Ω (maximum ripple amplitude: 2V).
6. Output power is measured directly at the output pins of the IC.
7. Closed-loop voltage gain can be chosen between 26 and 50dB (stereo), and is determined by external components.
8. A resistor of 56kΩ between Pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100μF capacitor between Pins 5 and 6 (or 8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

2 × 12W Audio Amplifier TDA1510

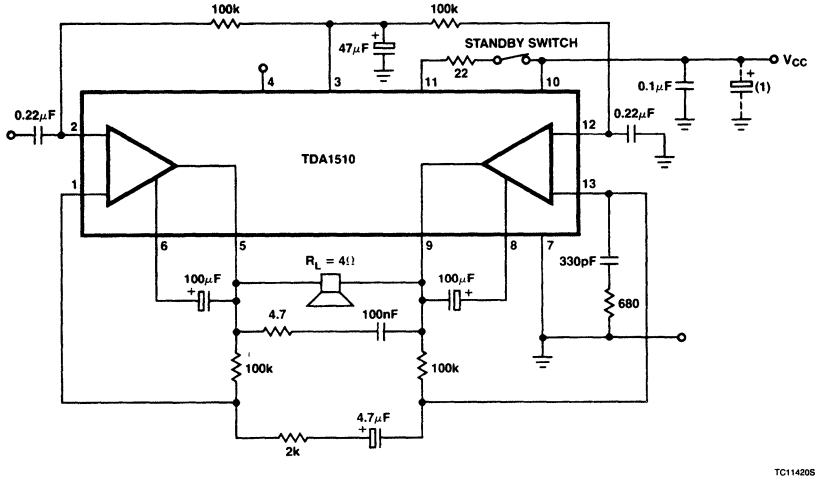

Figure 2. Test and Application Circuit Bridge-Tied Load (BTL)

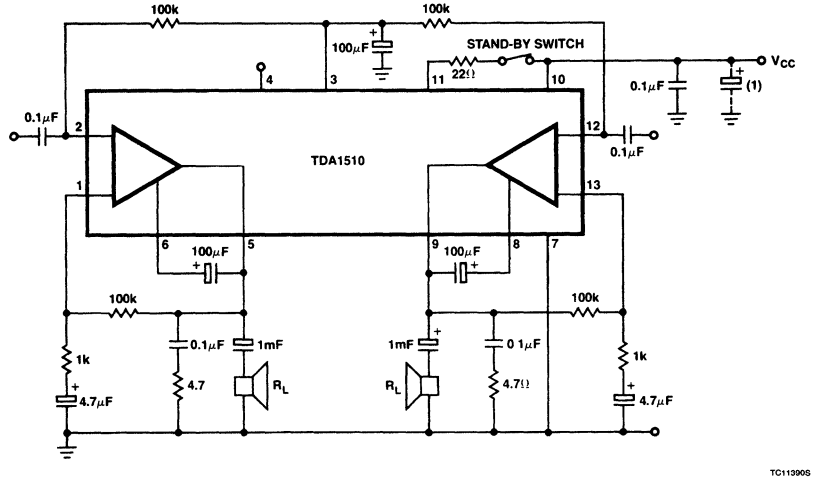

Figure 3. Test and Application Circuit Stereo Mode

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Signetics

AN1491
Car Radio Audio Power Amplifier up to 24W with the TDA1510

Linear Products

Author: F. A. Pelser

The TDA1510 is a power amplifier for car radio applications. It contains two identical amplifiers which can be used for stereo or BTL applications. The circuit consists of a 13-lead SIP-to-DIP plastic power package (SOT-141B) with a $\theta_{JC} \leqslant 3°C/W$.

Car radio ICs require protection from hostile environmental conditions. Therefore, several protection circuits are built-in:

- AC short-circuit to ground
- Power supply overvoltage protection
- Thermal shutdown
- Low offset voltage between the two outputs (important in BTL)
- Large open-loop gain
- Good ripple rejection
- Low standby current

CIRCUIT DESCRIPTION

General

The TDA1510 contains two identical amplifiers with differential input stages. It can be used for stereo or bridge applications.

Signal Path

The collectors of the non-inverting PNP input transistors are coupled to the Class A driver stages which drive the Class B output stages. The Class A driver transistors are frequency-limited by a Miller capacitor. This improves the stability and overall noise behavior.

Protection Circuits

SOAR Protection

To improve the reliability during overdrive conditions and short-circuiting, both amplifiers have a Safe Operating Area Region (SOAR) protection circuit for the upper output stage. The base current of the output transistor is limited, based on the voltage and current applied to the output transistor. The protection area lies between 5A/0V and 0A/20V, thus limiting the signal excursion of these stages to its allowable boundaries including AC short-circuiting to ground. When a continuous short-circuit condition exists, the chip temperature can rise above 150°C. At that point, the thermal shutdown circuit becomes operative.

Special attention has been paid to the layout of the output transistors to avoid current crowding.

Power Supply Overvoltage Protection

The power supply overvoltage protection circuit is activated when the difference between output voltage and V_{CC} is about 18V. Then, a low impedance is switched across the base and emitter of the upper Darlington output transistor. This offers a low impedance between base and emitter. The upper Darlington transistor breakdown voltage is thereby increased to $V_{CER} \approx 50V$.

Thermal Shutdown

To safeguard the circuit against high temperatures, a thermal shutdown protection circuit has been built into both amplifiers. When the die temperature exceeds 150°C, a transistor begins to turn on and thereby decreases the drive current to the power transistors.

Special Features

A special feature of the TDA1510 is the low current ($\leqslant$2mA) standby switch option. Because of the low switching current ($\leqslant$0.8mA), an inexpensive switch can be used.

This switch must be connected between Pin 11 and the positive supply line. It can also be used as a mute facility by disconnecting Pin 11 from the supply voltage.

Both amplifiers have bootstrap facilities at Pins 6 and 8. When these pins are not used, the internal bootstrap resistors have to be short-circuited by connecting Pins 6 and 8 to V_{CC}.

To optimize the output voltage for maximum output power without bootstrap, a resistor of 56kΩ must be connected between Pin 3 and common ground.

The supply ripple voltage can be smoothed by decoupling Pin 3 to ground.

Car Radio Audio Power Amplifier up to 24W with the TDA1510

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BOOSTER APPLICATION

Principle of BTL

The output power of an amplifier is determined by the supply voltage, the loudspeaker impedance, and the voltage losses in the output stage. Higher output power in car radios can be obtained by:

a) decreasing the loudspeaker impedance: (two speakers in parallel)

b) a bridge-tied load (BTL) circuit.

Decreasing the loudspeaker impedance far below 2Ω is impractical because of high losses in the loudspeaker wires and the high capacitance values of the output electrolytics. The only practical car radio circuit solution for higher output powers is BTL operation.

The basic principle of the BTL circuit is shown in Figure 1. This figure shows only the output stages. Both channels are antiphase driven. During the first half-period of the sine wave excursion T_1 and T_4 are conducting, and in the second half-period T_2 and T_3 are conducting.

The output swing across the load resistor has a peak-to-peak amplitude of two times V_{CC}.

The ideal average output power when clipping equals $\frac{(V_{CC})^2}{2}$

$$P_{O_{IDEAL}} = \frac{(V_{CC})^2}{R_L} \quad (1)$$

At V_{CC} = 14.4V and $R_L = 4\Omega$ $P_{O_{IDEAL}}$ = 26W

Because of voltage losses in the output stage of the TDA1510, the practical measured output power is 24W at d = 10% and 18W at d = 0.5%.

Amplification

The series drive principle of the BTL amplifier can be seen from the circuit that follows.

Assuming point A as virtual ground, the non-inverting amplifier 1 multiplies the input signal V_I by a factor $\left(\frac{R3 + R5}{R5}\right)$

A part of the output signal, V_{O1}–,i.e., $\frac{V_{O1} \cdot R_5}{R_3 + R_5}$,

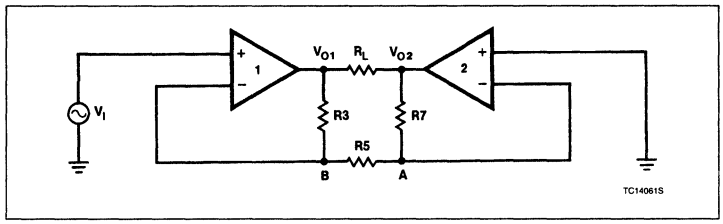
is amplified by inverting amplifier 2 with a factor R7/R5.* For maximum output voltage, R3 and R7 must have equal values.

In this case $V_{O1} = \frac{R3 + R5}{R5} \cdot V_I$ and because R3 = R7, (2)

$$V_{O2} = -\left(\frac{R7}{R5}\right) \cdot \left(\frac{R5}{R3 + R5}\right) \cdot \left(\frac{R3 + R5}{R5}\right) V_I$$

$$= -\left(\frac{R7}{R5}\right) \cdot V_I \quad (3)$$

NOTE:
* Since point 'B' is a virtual input for amplifier 2



The AC sine wave V_O across the load is $|V_{O1}| + |V_{O2}|$.

The overall voltage gain becomes:

$$A_V = \frac{V_O}{V_I} = \frac{|V_{O1}| + |V_{O2}|}{V_I}$$

$$= \frac{R7 + R5}{R5} + \frac{R7}{R5} = 2 \cdot \frac{R7}{R5} + 1 \quad (4)$$

In practice, $2 \cdot \frac{R7}{R5} \gg 1$, so $A_V = 2 \cdot \frac{R7}{R5}$ (5)

Design Criteria

The basic application circuit diagram is given in Figure 2.

Important design criteria of the printed circuit board:

1. The Boucherot filters $C_4 - R_4$ and $C_5 - R_6$ must be mounted as close as possible to the output Pins 5 and 9 and ground (Pin 7).
2. Filter $C_9 - R_8$ must be as close as possible to Pin 13 and the input ground. The specific filter is necessary to improve the overall stability.
3. The supply decoupling capacitors $C_{10} - C_{11}$ must be mounted as close as possible to Pins 10 and 7.
4. The supply ripple smoothing capacitor C2 and capacitor C8 must be connected to the input ground.
5. To avoid ground loops, the input and output ground must be kept separate.
6. For stability, it is recommended that a 22Ω resistor with short leads be placed in series with Pin 11.
7. The inputs are very sensitive to interferences and must be shielded from the rest of the circuit.

Performance Measurements

In the application circuit of Figure 2, several measurements are made. Unless otherwise specified, the measurements are made at V_{CC} = 14.4V; $R_L = 4\Omega$; f = 1kHz and T_A = 25°C. The supply wires to the DC voltage source are a twisted-pair.

Quiescent current consumption — In Figure 3 the total quiescent current consumption is given as a function of the supply voltage V_{CC}. The maximum guaranteed value at V_{CC} = 14.4V is 150mA.

Output voltage — The output voltage, V_A, measured between Pins 5-7 and 9-7 as a function of V_{CC}, is given in Figure 4. The offset voltage between Pins 5 and 9 is typically 2mV (maximum limit: 50mV).

Output power — The output power as a function of V_{CC} for d = 0.5% and d = 10% is given in Figure 5.

Harmonic distortion — The distortion as a function of the output power at f = 1kHz and f = 20kHz is given in Figure 6. In Figure 7 the distortion as a function of frequency is given at P_O = 10W.

Input impedance — The input impedance is mainly determined by resistor R_1 (see Figure 2) In this application, $R_1 = 100k\Omega$. To minimize offset voltage, it is necessary that $R_1 = R_3$ and $R_2 = R_7$. For resistor values higher than 100kΩs, the offset voltage can increase due to differences in base currents.

Voltage gain — Previously it was derived that the closed-loop amplification in BTL equals:

$$A_V \approx 2 \cdot \frac{R7}{R5}$$

In this application $A_V \approx 100 \times$ = 40dB.

The open-loop gain of the TDA1510 is 80dB. It is possible to reduce the voltage gain *down to 32dB* (without instability) by increasing R5.

Frequency characteristic — In Figure 8 the relative voltage gain, A_V, is given as a function of the frequency (reference level P_O = 2.4W).

Power bandwidth — The relative output power as a function of the frequency for d = 0.5% and d = 10% is given in Figure 9.

Power dissipation — The power dissipation as a function of the output power is given in Figure 10.

For a worst-case sine wave dissipation of 11.8W, the external heatsink must have a

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Car Radio Audio Power Amplifier up to 24W with the TDA1510

thermal resistance of 4.4°C/W (for derivation see Appendix I).

Supply voltage ripple rejection (SVRR) — The SVRR as a function of the frequency is given in Figure 11.

Noise — The noise output voltage with $R_S = 10k\Omega$, and measured according to the IEC 179 A-curve, is 250μV.

Stability — The TDA1510 is stable for each kind of load, *down to 32dB.*

STEREO

The Stereo Application

The basic stereo application circuit diagram is given in Figure 12.

Important design criteria for the layout of the stereo print are the same as those for the BTL print regarding Boucherot filters, supply decoupling capacitor and the capacitor for the supply voltage ripple rejection.

Performance Measurements

In the application circuit of Figure 12 several measurements are made. If not otherwise specified, the measurements are made at $V_{CC} = 14.4V$; $R_1 = 4\Omega$; f = 1kHz and $T_A = 25°C$.

Quiescent current and output voltage — The quiescent current consumption is identical to that given for the BTL circuit (see Figure 3). The same holds for the output voltages at Pins 5 and 9 (see Figure 4).

Output power — The output power versus the supply voltage is given in Figure 13 for $R_L = 1.6\Omega$, 2Ω, 3.2Ω and 4Ω for a constant distortion level of 10%.

In Figure 14 the same characteristics are given for 0.5% distortion.

Using the circuit without bootstrap capacitors C_3 and C_7, the output voltage must be corrected to have symmetrical clipping. To do this a 56kΩ resistor has to be connected between Pin 3 and the input ground; Pins 5 and 8 must be connected to $+V_{CC}$.

The output power at the output pins is now 5.7W (4Ω load) and 10.5W (2Ω load).

Distortion — In Figure 15 the distortion as a function of the output power is given for $R_L = 4\Omega$ at 1 and 20kHz.

The same characteristics are given in Figure 16 for $R_L = 2\Omega$.

Input impedance — The input impedances are mainly determined by resistors R1 and R5.

In this application $R_1 = 100k\Omega$ (see Figure 12).

Voltage gain — The closed-loop voltage gain is determined by the feedback resistors R2 and R3 and R7 and R8, in this case: 40dB. It is possible to reduce the voltage gain down to 26dB (without instabilities) by increasing R2 and R8.

Frequency characteristics — The voltage gain A_V as a function of the frequency at $P_O = 1W$ is given in Figure 17.

Power bandwidth — In Figure 18 the output power is given as a function of the frequency for d = 0.5% and 10%.

Power dissipation — The total power dissipation of the two channels as a function of the output power per channel is given in Figure 19 for $R_L = 2\Omega$ and 4Ω.

The worst-case power dissipation in stereo is the same as in the BTL circuit.

The external heatsink must also have a thermal resistance of 4.4°C/W.

Supply voltage ripple rejection (SVRR) — The SVRR of both channels is 55dB from 100Hz to 20kHz.

Noise — The noise output voltages, measured according to IEC 179 A-curve are 90μV and 170μV at $R_S = 0$ and 10kΩ, respectively.

Channel separation — The channel separation at $P_O = 1W$ and $R_S = 10k\Omega$ is 60dB.

Stability — The TDA1510 is stable for each kind of complex load *down to 26dB* of gain.

APPENDIX

Heatsink Design

The TDA1510 has a θ_{JC} of 3°C/W.

Assume: $V_{CC} = 14.4V$, $R_L = 4\Omega$ and $T_{AMAX} = 60°C$.

From Figure 10 it can be seen that the maximum sine wave power dissipation with a 4Ω load is $\approx$ 11.8W in BTL.

The total required thermal resistance becomes:

$$\theta_{JA} = \frac{150-60}{11.8} = 7.6°C/W$$

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

When using a thermal compound, θ_{CH} is approximately 0.2°C/W,

it follows:

$$\theta_{HA} = 7.6 - (3 + 0.2) = 4.4°C/W$$

From these measurements it appears that the maximum power dissipation with music drive is about 75% of the worst-case sine wave power dissipation. Then the maximum practical power dissipation becomes 8.8°C/W with a 4Ω load in BTL.
This gives:

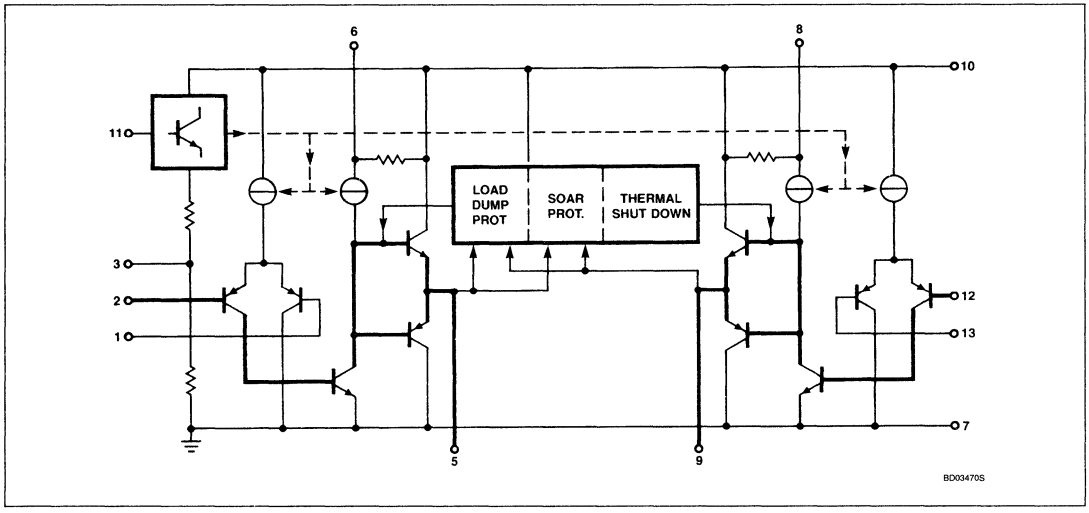
$$\theta_{JA} = \frac{150-60}{8.8} = 10.2°C/W$$

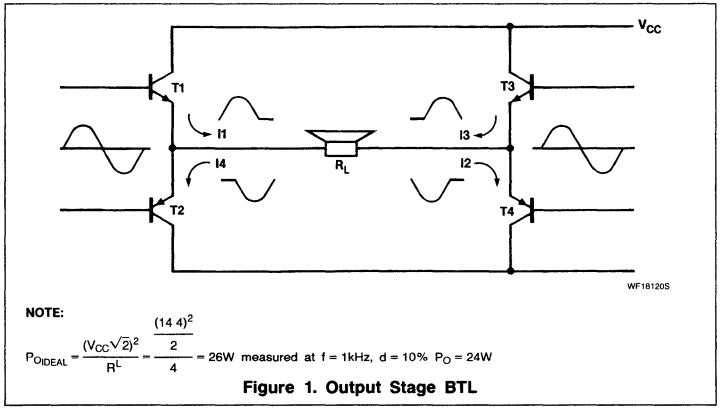
and the heatsink thermal resistance:

$$\theta_{HA} = 10.2 - (3 + 0.2) \approx 7°C/W$$

Car Radio Audio Power Amplifier up to 24W with the TDA1510

INTERNAL CIRCUIT BLOCK DIAGRAM





NOTE:

$$P_{O_{IDEAL}} = \frac{(V_{CC}\sqrt{2})^2}{R^L} = \frac{\frac{(14.4)^2}{2}}{4} = 26W \text{ measured at } f = 1kHz,\ d = 10\%\ P_O = 24W$$

Figure 1. Output Stage BTL

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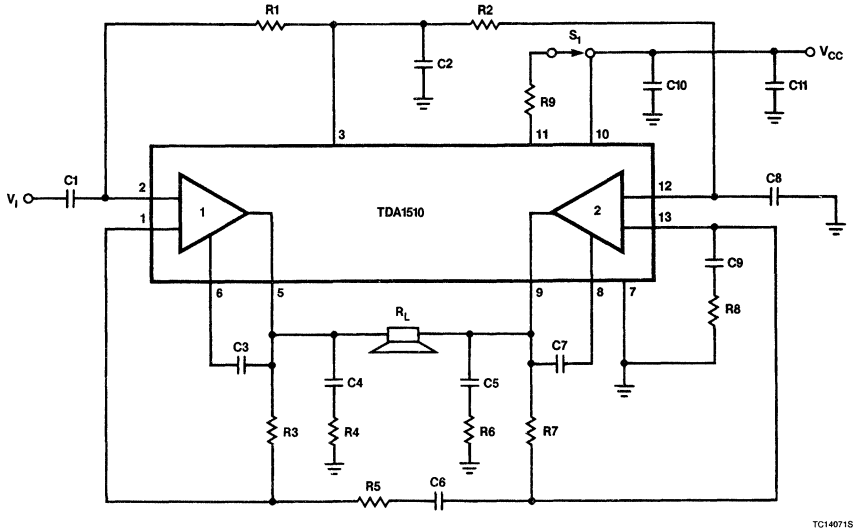

Figure 2. TDA1510 Bridge Application

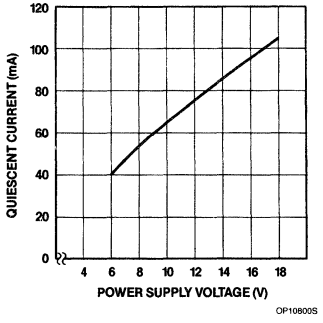

Figure 3. Total Quiescent Current Consumption vs Supply Voltage

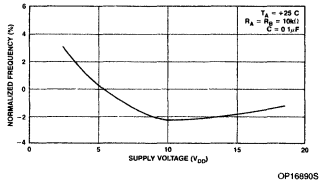

Figure 4. Output Voltage vs Supply Voltage

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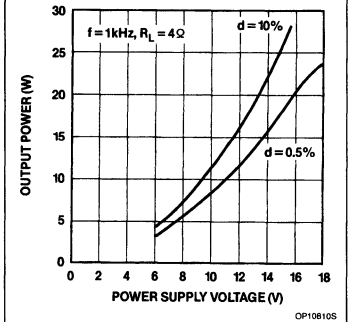

Figure 5. Output Power vs Supply Voltage

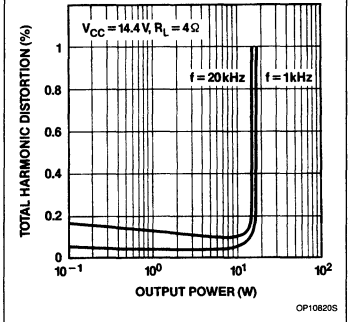

Figure 6. Total Harmonic Distortion vs Output Power

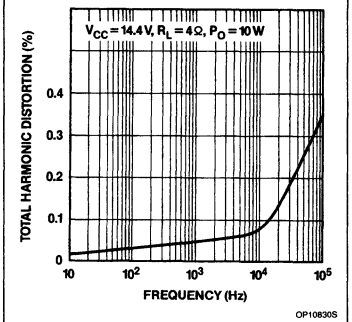

Figure 7. Total Harmonic Distortion vs Frequency

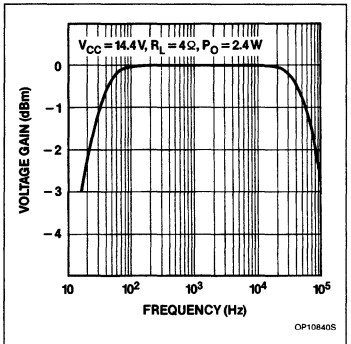

Figure 8. Frequency Characteristic

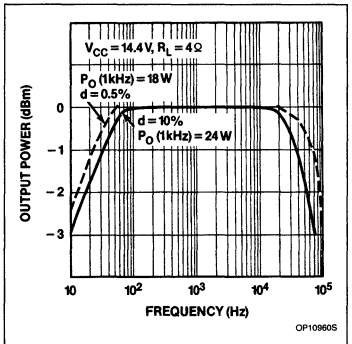

Figure 9. Power Bandwidth

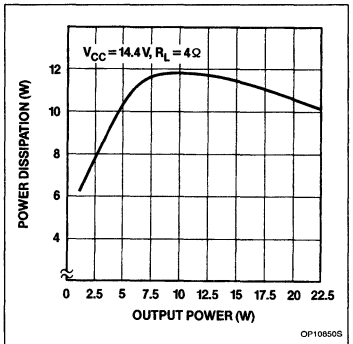

Figure 10. Power Dissipation vs Output Power

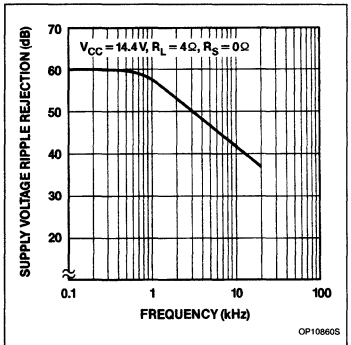

Figure 11. Supply Voltage Ripple Rejection vs Frequency

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Car Radio Audio Power Amplifier up to 24W with the TDA1510

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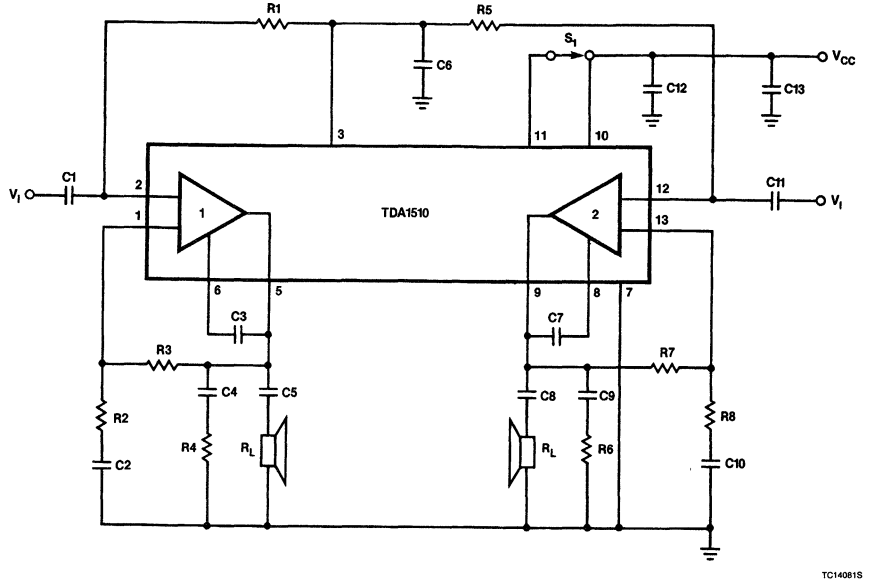


Figure 12. TDA1510 Stereo Application

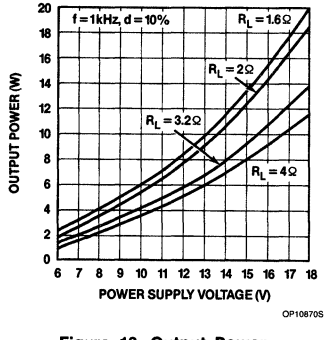


Figure 13. Output Power vs Supply Voltage

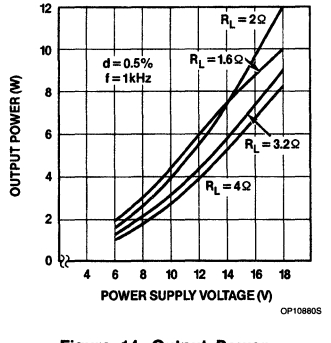


Figure 14. Output Power vs Supply Voltage

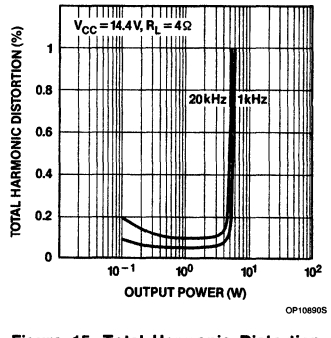


Figure 15. Total Harmonic Distortion vs Output Power

Car Radio Audio Power Amplifier up to 24W with the TDA1510

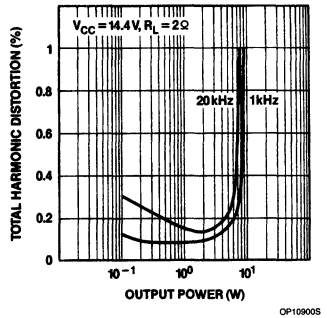


Figure 16. Total Harmonic Distortion vs Output Power

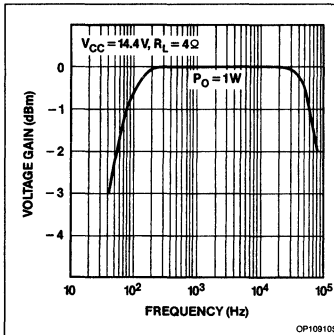


Figure 17. Frequency Characteristic

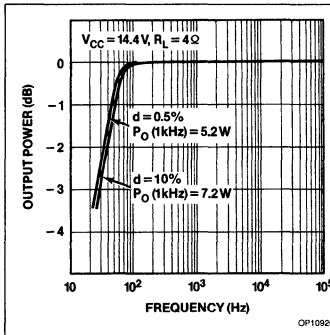


Figure 18. Power Bandwidth

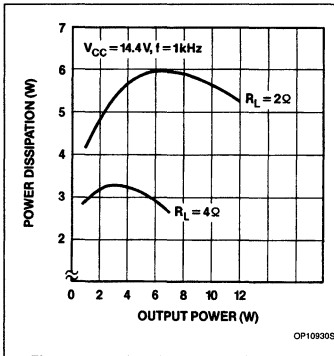


Figure 19. Total Power Dissipation vs Output Power Per Channel

NOTE:
Originally published as Report No. NBA8107, N.V. Philips Application Laboratory, December 17, 1981, Nijmegen, The Netherlands.

7

Signetics

TDA1512
12 to 20W Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies.

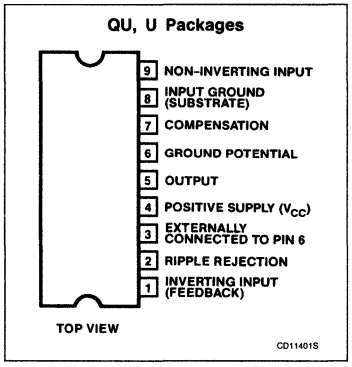
FEATURES

- **Thermal protection**
- **Low intermodulation distortion**
- **Low transient intermodulation distortion**
- **Built-in output current limiter**
- **Low input offset voltage**
- **Output stage with low cross-over distortion**
- **Single in-line (SIP) power package**

APPLICATIONS

- **Television**
- **Radio receivers**
- **Hi-fi power amp**

PIN CONFIGURATION

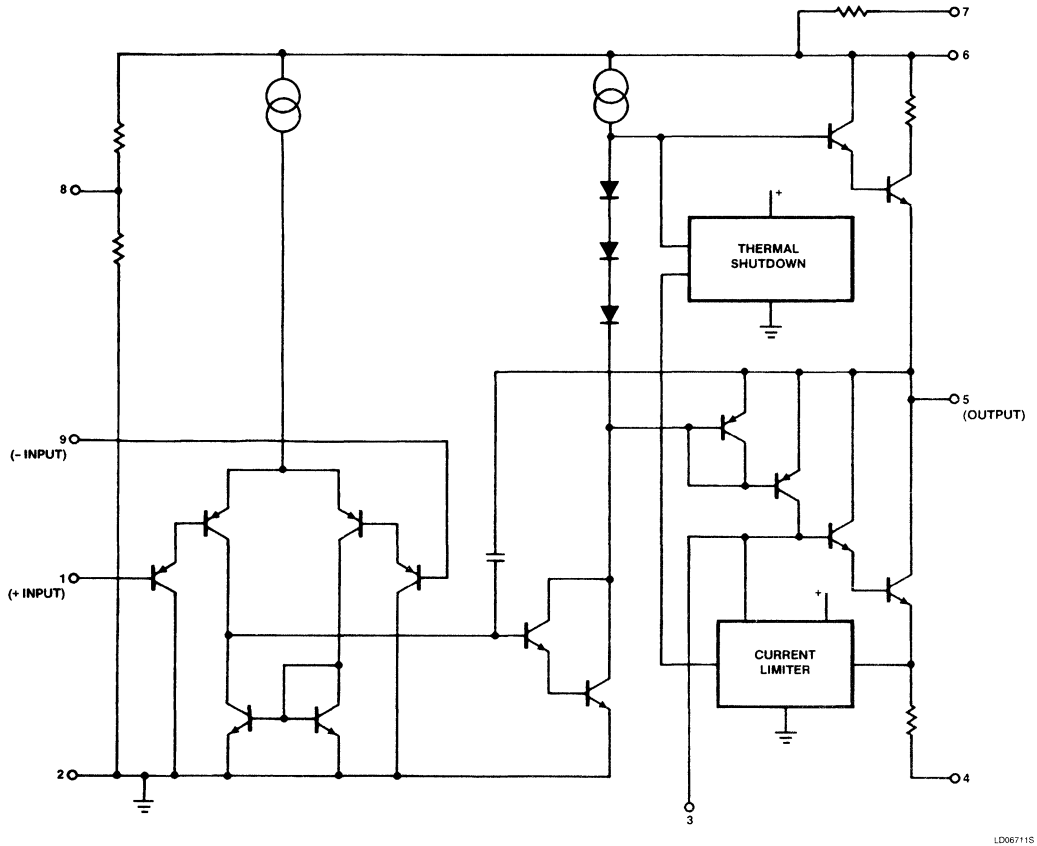


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131B)	−25°C to +150°C	TDA1512U
9-Pin Plastic SIP-bent-to-DIP Plastic Power (SOT-157B)	−25°C to +150°C	TDA1512QU

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	35	V
I_{ORM}	Repetitive peak output current	3.2	A
I_{OSM}	Non-repetitive peak output current	5	A
P_{TOT}	Total power dissipation	See derating curve Figure 1	
T_{STG}	Storage temperature	−55 to +150	°C
T_A	Operating ambient temperature	−25 to +150	°C
t_{SC}	AC short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_{CC} = 30V$ with $R_I = 4\Omega$	100	hours
θ_{JMB}	Thermal resistance from junction to mounting base	typ. 3 $\leqslant 4$	°C/W °C/W



Simplified Internal Circuit Diagram

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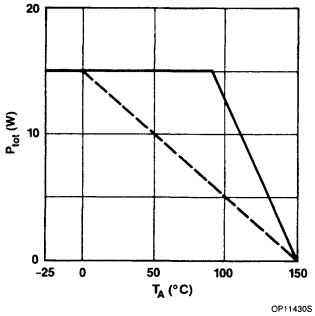
DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	15		35	V
I_{TOT}	Total quiescent current at V_{CC} = 25V		65		mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 25V; R_L = 4Ω; f = 1kHz; T_A = 25°C; measured in Test Circuit of Figure 2, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Output power				
	sine-wave power at d_{TOT} = 0.7%				
	R_L = 4Ω		13		W
	R_L = 8Ω		7		W
	music power at V_{CC} = 32V				
P_O	R_L = 4Ω; d_{TOT} = 0.7%		21		W
	R_L = 4Ω; d_{TOT} = 10%		25		W
	R_L = 8Ω; d_{TOT} = 0.7%		12		W
	R_L = 8Ω; d_{TOT} = 10%		15		W
B	Power bandwidth; −1.5dB; d_{TOT} = 0.7%	40Hz		16	kHz
	Voltage gain				
A_{VO}	open-loop		74		dB
A_{VC}	closed-loop		30		dB
	Input resistance (Pin 1)	100			kΩ
R_{IN}	Input resistance of Test Circuit (Figure 2)		20		kΩ
	Input sensitivity				
V_{IN}	for P_O = 50mW		16		mV
	for P_O = 10W		210		mV
	Signal-to-noise ratio				
	at P_O = 50mW; R_S = 2kΩ;				
S/N	f = 20Hz to 20kHz; unweighted	68			dB
	weighted; measured according to IEC 173 (A-curve)		76		dB
RR	Ripple rejection at f = 100Hz		50		dB
d_{TOT}	Total harmonic distortion at P_O = 10W		0.1	0.3	%
R_O	Output resistance (Pin 5)		0.1		Ω



NOTES:
——— mounted on infinite heatsink
- - - - mounted on heatsink of 6°C/W

Figure 1. Power Derating Curves

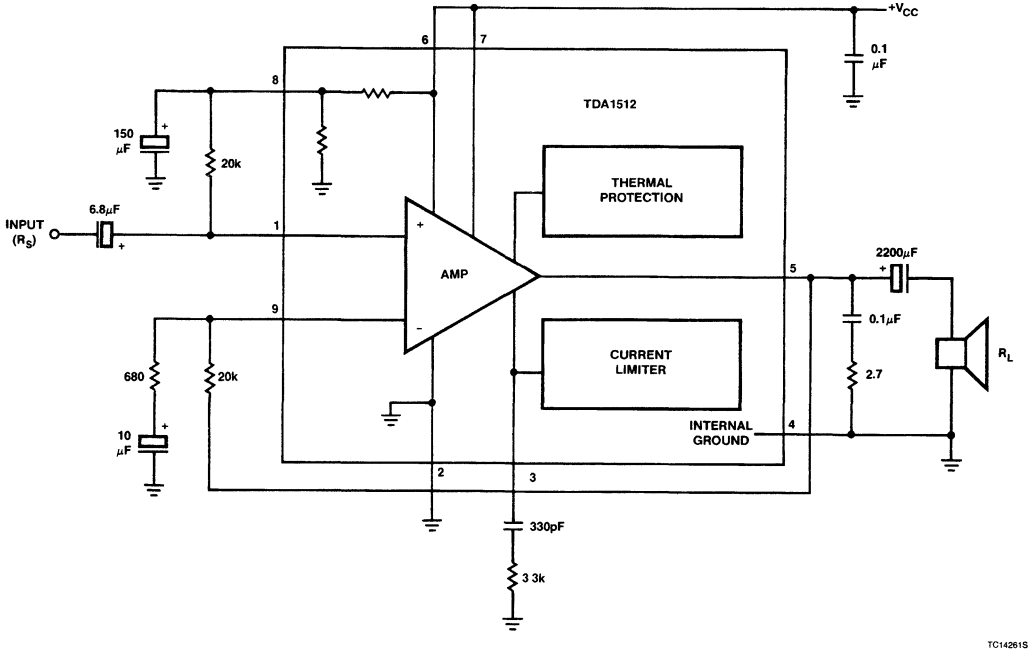


Figure 2. Test Circuit

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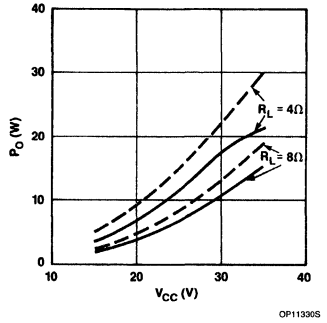


NOTES:
——— d_{TOT} = 0.7%.
- - - - d_{TOT} = 10%

Figure 3. Ouput Power as a Function of the Supply Voltage; f = 1kHz

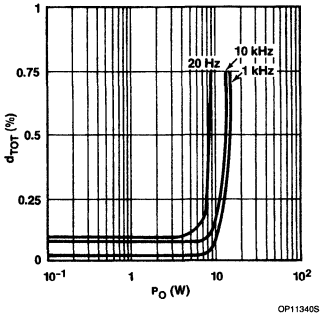


Figure 4. Total Harmonic Distortion as a Function of Output Power

Signetics

TDA1514
40W High-Performance Hi-Fi Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1514 integrated circuit is a hi-fi power amplifier for use as a building block in radio, TV and audio recorder applications. The high performance of the IC meets the requirements of digital sources (e.g. compact disc equipment).

The circuit is totally protected, the two output transistors both having thermal and SOA protection. The circuit also has a mute function that can be arranged to operate for a period after power-on with a delay time fixed by external components.

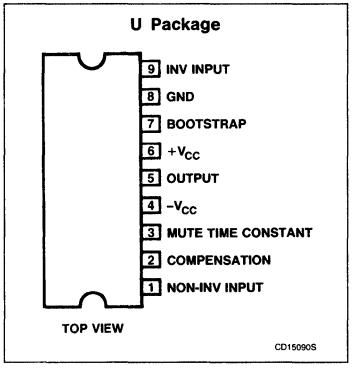
The device is intended for symmetrical power supplies, but an asymmetrical supply may also be used.

The theoretical maximum power dissipation with a stabilized power supply is $(V_{CC} - V_N)^2/2\pi^2 R_L = 19W$, where $V_{CC} = +27.5V$, $V_N = -27.5V$ and $R_L = 8\Omega$. Considering, for example, a maximum ambient temperature of 50°C and a maximum junction temperature of 150°C, the total thermal resistance θ_{JA} is $(150 - 50)/19 = 5.3°C/W$. Since the thermal resistance of the SOT-131A encapsulation is $< 1.5°C/W$, the thermal resistance required of the heatsink is $< 3.8°C/W$. Thus the maximum output power, and therefore the music power output, is limited only by the supply voltage and not by the heatsink.

FEATURES

- **Thermal protection**
- **Low THD**
- **SOA protection**
- **Mute time delay**
- **Short-circuit protected**
- **High power output**

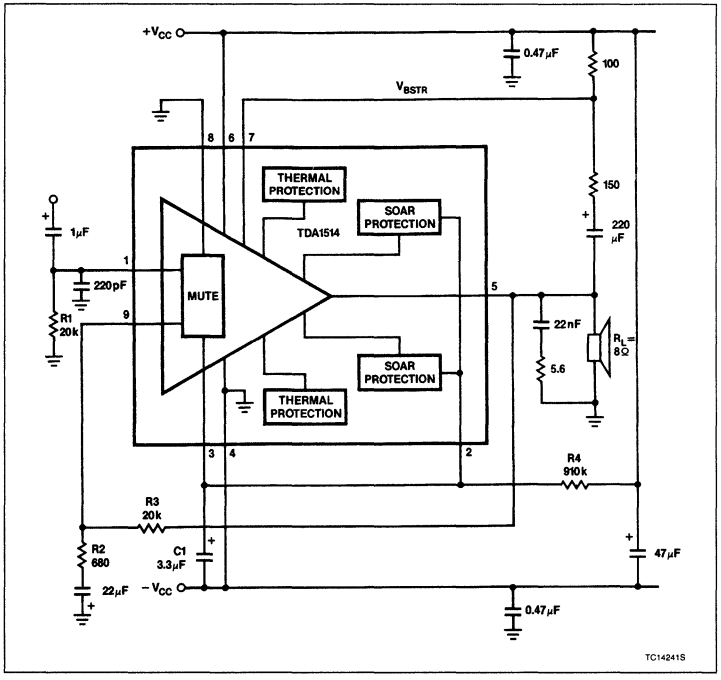
PIN CONFIGURATION



APPLICATIONS

- **Hi-Fi amplifier**
- **Radio**
- **Television**
- **Motor driver**

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131A)	−25°C to +150°C	TDA1514U

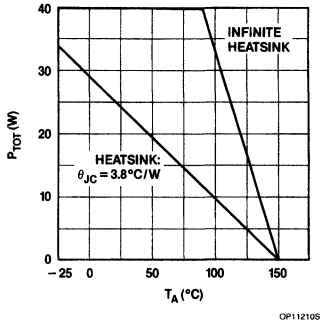


Figure 1. Power Derating Curve

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$+V_{CC}$ to $-V_{CC}$	Supply voltage (Pin 6 to Pin 4)	60	V
V_{BSTR}	Bootstrap voltage (Pin 7 to Pin 4)	70	V
I_O	Output current (repetitive peak)	4.0	A
T_A	Operating ambient temperature range	−25 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	See Figure 1	
t_{PR}	Thermal shut-down protection time	1	hour
t_{SC}	Short-circuit protection time[1]	10	min
V_M	Mute voltage (Pin 3 to Pin 4)	7	V

NOTE:

1. Driven by a pink-noise voltage
   Symmetrical power supply: AC and DC short-circuit protected
   Asymmetrical power supply. AC short-circuit protected

DC ELECTRICAL CHARACTERISTICS

$+V_{CC} = +27.5V$; $-V_{CC} = -27.5V$; $R_L = 8\Omega$; $f = 1kHz$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$+V_{CC}$ to $-V_{CC}$	Supply voltage range (Pin 6 to Pin 4)	15		60	V
I_{OMmax}	Maximum output current (peak value)	3.2			A
I_{TOT}	Total quiescent current	30	60	90	mA
	Output power with THD = −60dB:				
P_O	at $V_{CC} - V_N = 55V$	37	40		W
P_O	at $V_{CC} - V_N = 44V$		25		W
P_O	at $V_{CC} - V_N = 32V$			12.5	W
THD	Total harmonic distortion at $P_O = 32W$		−90	−80	dB
d_{IM}	Intermodulation distortion at $P_O = 32W$[1]		−80		dB
B	Power bandwidth (−3dB) at THD = −60dB		20 to 25k		Hz
dV/dt	Slew rate		15		V/μs
A_{VC}	Closed-loop voltage gain[2]	29.2	29.7	30.2	dB
A_{VO}	Open-loop voltage gain		85		dB
Z_I	Input impedance[3]	1			MΩ
(S + N)/N	S/N related to $P_O = 4mW$[4]	80			dB
V_{OS}	Input offset voltage		3		mV
$\pm I_{IO(B)}$	Input offset bias current		0.2	1	μA
$B+ I_B$	Input bias current		1	5	μA
Z_O	Output impedance			0.1	Ω
RR	Supply voltage ripple rejection at ripple frequency = 100Hz; ripple voltage (RMS value) = 500mV; source resistance = 2kΩ	70			dB
t_M	Mute time[5]		1.25		s
$V_{M(on)}$	Mute on voltage (Pin 3 to Pin 4)	0		5	V
$V_{M(off)}$	Mute off voltage (Pin 3 to Pin 4)	6		7	V
I_{2TOT}	Quiescent current into Pin 2[6]		20		μA

NOTES:

1. Measured with two superimposed signals of 50Hz and 7kHz with an amplitude relationship of 4:1.
2. The closed-loop gain is determined by external resistors and is variable between 20 and 46dB.
3. The input impedance in the test circuit is determined by the bias resistor R1
4. The noise voltage at the output is measured in the band 20Hz to 20kHz and source resistance $R_S = 2k\Omega$
5. Determined by R4 and C1.
6. The quiescent current into Pin 2 determines (with the value of R4) the minimum power supply voltage at which the mute function remains in operation. $+V_{CC} - V_N = I_{2TOT} \times R4 + V_{M(ON)max}$

7

Signetics

TDA1515A
24W BTL Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1515 is a monolithic integrated class-B output amplifier in a 13-pin single in-line (SIP) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage V_{CC} = 14.4V, an output power of 21W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as stereo amplifier, it delivers 2 × 11W into 2Ω or 2 × 6.5W into 4Ω.

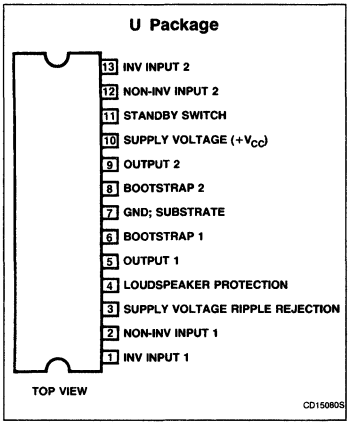
FEATURES

- **Flexibility in use — mono BTL as well as stereo**
- **High output power**
- **Low offset voltage at the output (important for BTL)**
- **Large usable gain variation**
- **Very good ripple rejection**
- **Internal limited bandwidth for high frequencies**
- **Low standby current possibility (typ. 1μA), to simplify required switches; TTL drive possible**
- **Low number and small-sized external components**
- **High reliability**
- **Load dump protection**
- **AC and DC short-circuit safe to ground up to V_{CC} = 18V**
- **Thermal protection**
- **Speaker protection in bridge configuration**
- **SOAR protection**
- **Outputs short-circuit safe to ground in BTL**
- **Reverse-polarity safe**

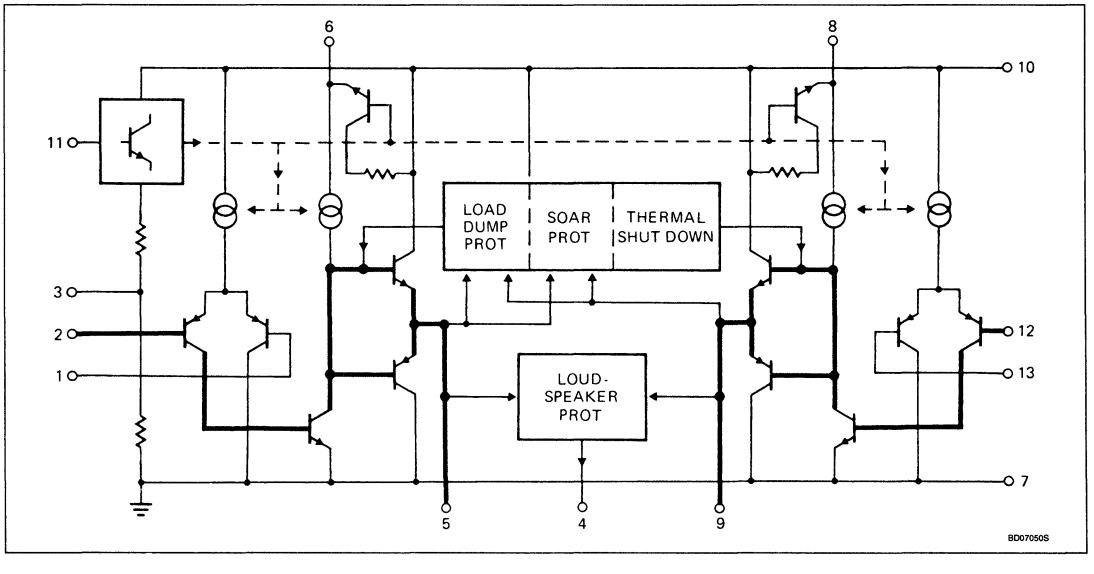
APPLICATIONS

- **Car radio applications**
- **Drive low impedance loads**
- **Stereo amplifier**

PIN CONFIGURATION



BLOCK DIAGRAM



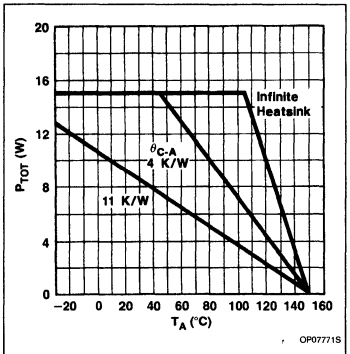


Figure 1. Power Derating Curves

HEATSINK DESIGN EXAMPLE

The derating of 3°C/W of the encapsulation requires the following external heatsink (for sine-wave drive):

21W BTL (4Ω) or 2 × 11W stereo (2Ω) maximum sine wave dissipation: 12W

T_A = 65°C maximum

$$\theta_{HA} = \frac{150 - 65}{12} - 3 = 4°C/W.$$

2 × 6.5W stereo (4Ω) maximum sine wave dissipation: 6W

T_A = 65°C maximum

$$\theta_{HA} = \frac{150 - 65}{6} - 3 = 11°C/W.$$

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
13-Pin Plastic SIP (SOT-141B)	0 to +70°C	TDA1515AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage; operating (Pin 10)	18	V
V_{CC}	Supply voltage; non-operating	28	V
V_{CC}	Supply voltage; during 50ms (load dump protection)	45	V
I_{OM}	Peak output current	6	A
P_{TOT}	Total power dissipation	see derating curve Fig. 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_C	Crystal temperature	150	°C
	AC and DC short-circuit safe voltage	18	V
	Reverse polarity	10	V

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range (Pin 10)	6		18	V
I_{ORM}	Repetitive peak output current			4	A
I_{TOT}	Total quiescent current		75	75	mA
V_{11} V_{11}	Switching level 11: OFF ON	 3		1.8	V V
$\lvert Z_{OFF}\rvert$	Impedance between Pins 10 and 6; 10 and 8 (standby position V_{11} < 1.8V)	100			kΩ
I_{SB}	Standby current at V_{11} = 0 to 0.8V		1	100	μA
I_{SO}	Switch-on current (Pin 11) at $V_{11} \leqslant V_{10}$		10	100	μA

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AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14.4V$; $f = 1kHz$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Bridge-tied load application (BTL) (see Figure 2)					
	Output power at $R_L = 4\Omega$ (with bootstrap)				
P_O	$V_{CC} = 14.4V$; $d_{TOT} = 0.5\%$	15 5	18		W
P_O	$V_{CC} = 14.4V$; $d_{TOT} = 10\%$	20	24		W
P_O	$V_{CC} = 13.2V$; $d_{TOT} = 0.5\%$		15		W
P_O	$V_{CC} = 13.2V$; $d_{TOT} = 10\%$		20		W
G_O	Open-loop voltage gain		75		dB
G_C	Closed-loop voltage gain[2]		40		dB
	Output power without bootstrap[9]				
P_O	$V_{CC} = 14.4V$; $d_{TOT} = 10\%$		15	15	W
P_O	$V_{CC} = 14.4V$; $d_{TOT} = 0.5\%$		12	12	W
P_O	$V_{CC} = 13.2V$, $d_{TOT} = 10\%$		12	12	W
P_O	$V_{CC} = 13.2V$, $d_{TOT} = 0.5\%$		9	9	W
B	Frequency response at $-3dB$[3]	20		20	Hz
$\|Z_I\|$	Input impedance[4]	1			MΩ
	Noise input voltage (RMS value) at $f = 20Hz$ to $20kHz$				
$V_{N(RMS)}$	$R_S = 0\Omega$		0 2	0.2	mV
$V_{N(RMS)}$	$R_S = 10k\Omega$		0.35	0.35	mV
V_N	$R_S = 10k\Omega$		0.25	0.8	mV
	Supply voltage ripple rejection				
RR	$f = 100Hz$	42	50	50	dB
$\|\Delta V_{5-9}\|$	DC output offset voltage between the outputs		2	50	mV
	Loudspeaker protection (all conditions)				
$\|\Delta V_{5-9}\|$	maximum DC voltage (across the load)			1	V
B	Power bandwidth; $-1dB$; $d_{TOT} = 0.5\%$	30		40	kHz
Stereo application (see Figure 3)					
	Output power at $d_{TOT} = 10\%$; with bootstrap[6]				
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$	6	7		W
P_O	$V_{CC} = 14.4V$; $R_L = 2\Omega$	10	12		W
P_O	$V_{CC} = 13.2V$; $R_L = 4\Omega$		6		W
P_O	$V_{CC} = 13.2V$; $R_L = 2\Omega$		10		W
	Output power at $d_{TOT} = 0.5\%$; with bootstrap[6]				
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$		5.5		W
P_O	$V_{CC} = 14.4V$; $R_L = 2\Omega$		9		W
P_O	$V_{CC} = 13.2V$; $R_L = 4\Omega$		4.5		W
P_O	$V_{CC} = 13.2V$; $R_L = 2\Omega$		7.5		W
	Output power at $d_{TOT} = 10\%$; without bootstrap				
P_O	$V_{CC} = 14.4V$; $R_L = 4\Omega$[6, 8, 9]		6		W
B	Frequency response at $-3dB$[3]	40		20	kHz
RR	Supply voltage ripple rejection[5]		50		dB
α	Channel separation; $R_S = 10k\Omega$; $f = 1kHz$	40	50		dB
G_C	Closed-loop voltage gain[7]		40		dB
Noise output voltage (RMS value) at f = 20Hz to 20kHz					
$V_{n(RMS)}$	$R_S = 0\Omega$		0.15		mV
$V_{n(RMS)}$	$R_S = 10k\Omega$		0.25		mV
V_n	$R_S = 10k\Omega$		0.2		mV

NOTES:
1 The internal circuit impedance at Pin 11 is $> 5k\Omega$ if $V_{11} > V_{10}$
2. Closed-loop voltage gain can be chosen between 32 and 56dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4 The input impedance in the test circuit (Figure 3) is typically $100k\Omega$
5. Supply voltage ripple rejection measured with a source impedance of 0Ω (maximum ripple amplitude 2V)
6. Output power is measured directly at the output pins of the IC
7. Closed-loop voltage gain can be chosen between 26 and 50dB (stereo), and is determined by external components.
8. A resistor of $56k\Omega$ between Pins 3 and 7 to reach symmetrical clipping
9. Without bootstrap the $100\mu F$ capacitor between Pins 5 and 6 (8 and 9) can be omitted Pins 6, 8 and 10 have to be interconnected

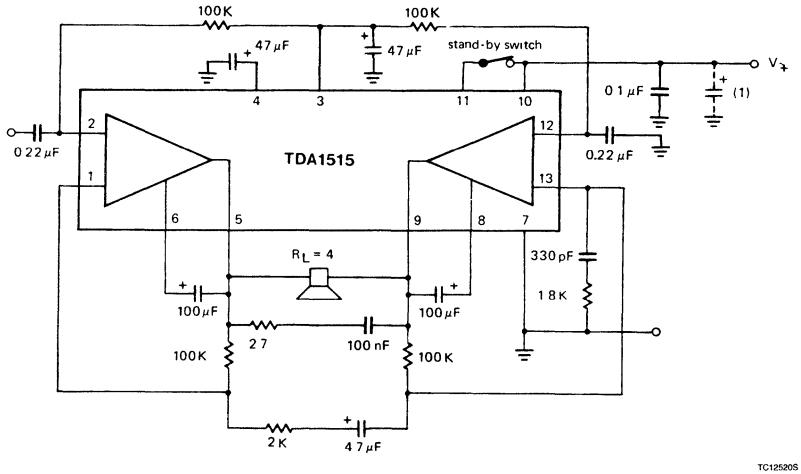

Figure 2. Test/Application Circuit Bridge-Tied Load (BTL)

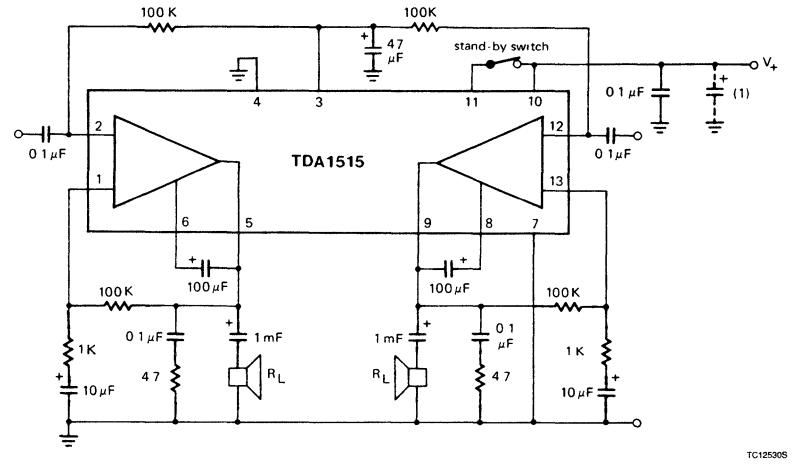

Figure 3. Test/Application Circuit Stereo

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Signetics

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Car Radio Audio Power Amplifiers up to 20W with the TDA1515

Linear Products

Application Note

Authors F Pelser
J Sips

The TDA1515 is a power amplifier for car radio applications It contains two identical amplifiers which can be utilized for BTL or stereo applications The TDA1515 is available in a 13-lead single in-line plastic power package with θ_{JC} of $\leqslant$ 3°C/W

Car radios require protection from hostile automotive environmental conditions, therefore, several protection circuits are built into the TDA1515

- AC and DC short-circuit to ground
- Power supply over voltage
- Thermal shutdown
- Speaker protection in bridge configuration

Other features of the TDA1515 include

- Low offset voltage
- Large gain selection range
- Good ripple protection
- Low standby current
- Standby control with TTL levels

CIRCUIT DESCRIPTION

The TDA1515 contains two identical amplifiers with differential input stages It can be used for stereo or bridge applications

Signal Path

The collectors of the non-inverting PNP input transistors are coupled to the Class A driver stages which drive the Class B output stages The Class A driver transistors are frequency-limited by a Miller capacitor This improves the stability and overall noise behavior

Protection Circuits

To improve the reliability where the overdrive condition exists and when short circuiting, both amplifiers have a Safe Operating Area Region (SOAR) protection circuit for the upper output stage The base current of the output transistor is limited, based on the voltage and current applied to the output transistor The SOAR lies between 5A/0V and 0A/20V Due to the SOAR protection circuit, it is possible to limit the signal excursion of these stages to their allowable boundaries. Therefore, AC and DC short-circuiting to ground will not damage the device

With continuous short circuit, the chip temperature can rise above 150°C At that point, the thermal shutdown circuits become operative Special attention has been paid to the layout of the output transistors to avoid current crowding

Power Supply Over Voltage Protection

The power supply over voltage protection circuit is activated when the difference between output voltage and V_{CC} is about 18V Then, a low impedance is switched between the base and emitter of the upper Darlington output transistor The upper Darlington transistor breakdown voltage is thereby increased to $V_{CER} \approx 50V$

Thermal Shutdown

To safeguard the IC against high temperatures, thermal shutdown protection circuits have been built into both amplifiers. When the die temperature exceeds 150°C, a transistor begins to turn on and thereby decreases the drive current to the power transistor. A second thermal shutdown protection circuit protects the output transistors against hot spot temperatures

Loudspeaker Protection in BTL

The loudspeaker protection in BTL starts operating when the DC offset voltage between the output Pins 5 and 9 exceeds 1V An internal comparator circuit controls the deviating DC output voltage. The maximum DC current through the loudspeaker is therefore limited to a safe value for the speaker ($\simeq$250mA for a 4Ω speaker)

Due to the RC time (about 1 second with 47μF) at Pin 4, the DC current-limiting protection circuit is inoperative during switching on and short-circuiting for one second

Special Features

A special feature of the TDA1515 is a mute function When Pin 11 is taken below 1.8V, mute is on. When it is taken above 3V, mute is off.

Both amplifiers have bootstrapping capabilities at Pins 6 and 8 When these pins are not used, the internal bootstrap resistors must be short-circuited by connecting Pins 6 and 8 to V_{CC} To avoid poor ripple rejection in the standby mode, the bootstrap resistor is internally switched off To optimize the output voltage for maximum output power without bootstrap, a resistor of 56kΩ must be connected between Pin 3 and common ground The supply ripple voltage can be smoothed by decoupling Pin 3 to ground

BOOSTER APPLICATION

Principle of BTL

The principle of the BTL circuit is shown in Figure 1. This figure shows only the output stages Both channels are antiphase driven During the first half-period of the sine wave excursion, T_1 and T_4 are conducting, and in the second half-period T_2 and T_3 are conducting. The output swing across the load resistor has a peak-to-peak amplitude of two times V_{CC}

The ideal average output power at clipping equals

$$P_O \text{ ideal} = \frac{\frac{V_{CC}{}^2}{2}}{R_L} \quad (1)$$

At $V_{CC} = 14.4V$ and $R_L = 4\Omega$ P_O ideal = 26W. Because of voltage losses in the output stage of the TDA1515 and due to wiring of the board, the practical measured output power on the board is 20.5W

Measured on the pins of the IC, the output power becomes 21W.

Amplification

The overall voltage gain in the amplification circuit becomes.

$$A_V = \frac{V_0}{V_I} = \frac{|V_{OI}| + |V_{OII}|}{V_I} = \frac{R6 + R5}{R5} > +$$

$$\frac{R6}{R5} = 2 \cdot \frac{R6}{R5} + 1$$

(assuming R3 = R6) (2)

In practice $2 \cdot \frac{R6}{R5} >> 1$,

therefore $A_V = 2 \cdot \frac{R6}{R5}$. (3)

Design Criteria

The basic application circuit diagram is given in Figure 2

Car Radio Audio Power Amplifiers up to 20W with the TDA1515

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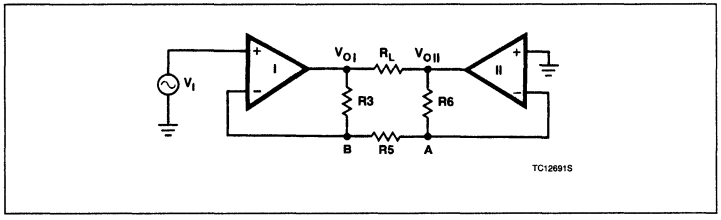
AMPLIFICATION CIRCUIT



Important design criteria of the PC board:

1. The Boucherotfilter $C_4 - R_4$ must be mounted as close as possible between the output Pins 5 and 9.

2. Filter $C_9 - R_7$ must be as close as possible between Pin 13 and the input ground. The specific filter is necessary to improve overall stability.

3. The supply decoupling capacitors $C_{10} - C_{11}$ must be mounted as close as possible between Pins 10 and 7.

4. The supply ripple smoothing capacitor C_2 and capacitor C_8 must be connected to the input ground.

5. Separate input and output grounds must be maintained.

6. With the high input impedance at Pin 11, it is recommended to decouple Pin 11 with a 100nF capacitor to ground to guarantee a good standby switching behavior.

Performance Measurements

In the application circuit of Figure 2, several measurements are done. If not otherwise stated, the measurements are given at $V_{CC} = 14.4V$ on the PC board connections; $R_L = 4\Omega$; f = 1kHz and $T_A = 25°C$.

The power supply wires are a twisted-pair.

a) Quiescent current consumption
In Figure 3 the total quiescent current consumption is given as a function of the supply voltage V_{CC}. The maximum guaranteed value at $V_{CC} = 14.4V$ is 125mA. In standby position of S the quiescent current is $\approx 1\mu A$ ($\leq 0.2mA$).

b) Output voltage
The output voltage measured between Pins 5 – 7 and 9 – 7 as a function of V_{CC} is given in Figure 4. The offset voltage between Pins 5 and 9 is typically 2mV (maximum limit: 50mV).

c) Output power
The output power as a function of V_{CC} for d = 0.5% and d = 10% is given in Figure 5 (Power losses across the PC board are $\approx 0.5W$ at d = 10% and $\approx 0.25W$ at d = 0.5% level and $V_{CC} = 14.4V$).

d) Harmonic distortion
The distortion as a function of the output power at f = 1kHz and f = 20kHz is given in Figure 6. In Figure 7, the distortion as a function of frequency is given at $P_O = 1W$.

e) Input impedance
The input impedance is mainly determined by resistor R_1 (see Figure 2). In our application: 100kΩ. To minimize offset voltage, it is necessary that $R_1 = R_3$ and $R_2 = R_6$. For resistor values higher than some 100kΩs the offset voltage can increase due to differences in base currents.

f) Voltage gain
In the Applications section it is derived that the closed-loop amplification in BTL equals:

$$A_V \approx 2 \cdot \frac{R6}{R5}$$

In our application $A_V = 100 \times (40dB)$. The open-loop gain of the TDA1515 is 75dB. It is possible to reduce the voltage gain down to 32dB (without instability) by increasing R5.

g) Frequency characteristics
In Figure 8 the relative voltage gain A_V is given as a function of the frequency (reference level P_O 10dB below 20W).

h) Power bandwidth
The relative output power as a function of the frequency for d = 0.5% and d = 10% is given in Figure 9.

i) Power dissipation
The power dissipation as a function of the output power is given in Figure 10. For a worst-case sine wave dissipation of $\approx 11.5W$, the external heatsink must have a thermal resistance of 4.6°C/W.

j) Supply Voltage Ripple Rejection (SVRR)
The SVRR as a function of the frequency is given in Figure 11.

k) Noise
The noise output voltage with $R_S = 10k\Omega$ and measured according to the IEC 179 A-curve is $250\mu V$.

STEREO

The Stereo Application

The basic stereo application circuit diagram is given in Figure 12.

Design criteria for the layout of the stereo application are the same as those given in the Design Criteria Section. Component leads are as short as possible for the power supply decoupling capacitor, and the capacitor for the supply voltage ripple rejection.

Performance Measurements

In the application circuit of Figure 12, several measurements are done. If not otherwise stated, the results of the measurements are given at $V_{CC} = 14.4V$; $R_1 = 4\Omega$; f = 1kHz and $T_A = 25°C$. (V_{CC} measured on the PC board connections).

a) The quiescent current consumption and output voltage are identical to those given for the BTL circuit above.

b) Output power
The output power versus the supply voltage is given in Figure 13 for $R_L = 1.6$, 2, 3.2, and 4Ω, respectively, for a constant distortion level of 10%. (The power losses due to the output electrolytic are about 0.3W, while the losses across the PC board traces are $\approx 0.25W$ at $V_{CC} = 14.4V$ and $R_L = 2\Omega$). In Figure 14, the same characteristics are given for 0.5% distortion.
Using the circuit without bootstrap capacitors C_3 and C_7, the output voltage must be corrected to have symmetrical clipping. Therefore a 56kΩ resistor has to be connected between Pin 3 and the input ground; Pins 5 and 8 must be interconnected to $+V_{CC}$.
The output power at the output pins is now 5.3W (4Ω load) and 6.5W (2Ω load).

c) Distortion
In Figure 15 the distortion as a function of the output power is given for $R_L = 4\Omega$ at 1 and 20kHz, while in Figure 16 it is shown for $R_L = 2\Omega$. The total harmonic distortion versus frequency for $R_L = 2$ and 4Ω is given in Figure 17.

d) Input impedance
The input impedances are mainly determined by resistor R1 and R5 (100kΩ).

e) Voltage gain
The closed-loop voltage gain is determined by the feedback resistors $R_2 - R_3$ and $R_7 - R_8$, in this case 40dB. It is possible to reduce the voltage gain down to 26dB (without instabilities) by increasing R_2 and R_8.

f) Frequency characteristics
The relative voltage gain as a function of

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Car Radio Audio Power Amplifiers up to 20W with the TDA1515

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the frequency at P_O = 1W is given in Figure 18.

g) Power bandwidth
In Figure 19 the relative output power is given as a function of the frequency for d = 1% and 10%.

h) Power dissipation
The total power dissipation of the two channels as a function of the output power per channel is given in Figure 20 for R_L = 2 and 4Ω. The worst-case power dissipation in stereo is the same as in the BTL circuit. The external heatsink must also have a thermal resistance of 4.6°C/W.

i) Supply Voltage Ripple Rejection (SVRR)
The SVRR as a function of the frequency is given in Figure 21.

j) Noise
The noise output voltages, measured according to IEC 179 A-curve are 90 and 170μV at R_S = 0 and 10kΩ, respectively.

k) Channel separation
The channel separation at P_O = 1W, f = 1kHz and R_S = 10kΩ is 60dB.

APPENDIX I

Heatsink Design

The TDA1515 has a θ_{JC} of 3°C/W

Assume: V_{CC} = 14.4V, R_L = 4Ω, T_A = 60°C.

From Figure 10 it follows that the maximum sine wave power dissipation with a 4Ω load is ≈11.5W in BTL.

The total required thermal resistance becomes:

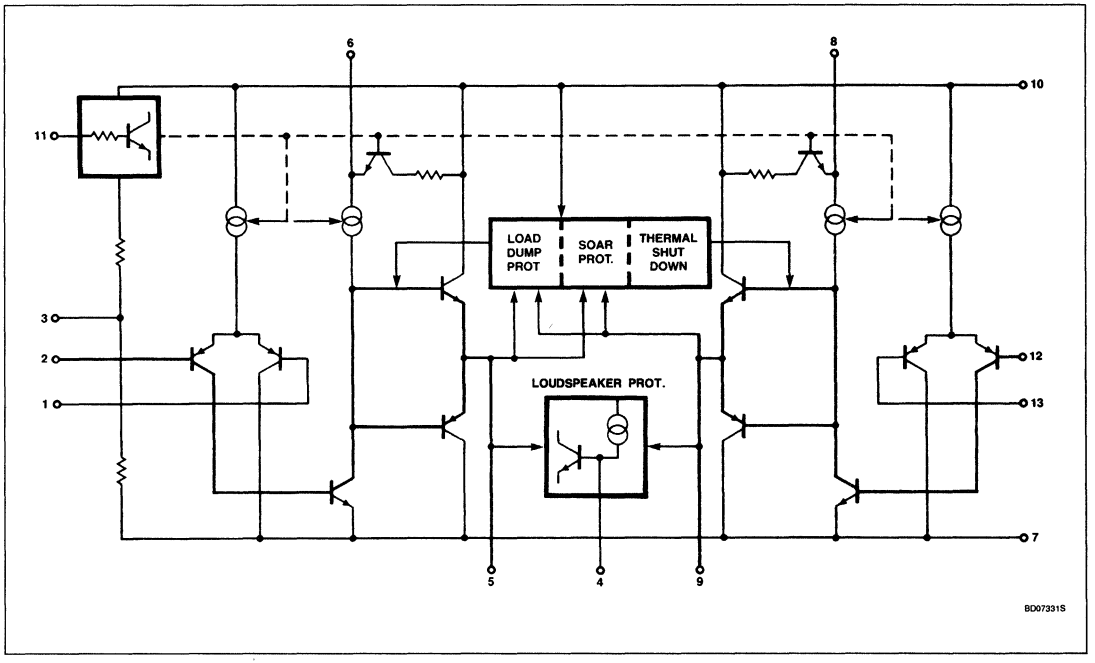
$$\theta_{JA} = \frac{150 - 60}{11.5} = 7.8°C/W$$

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

When using thermal compound θ_{CH} is about 0.2°C/W it follows:

$$\theta_{HA} = 7.8 - (3 + 0.2) = 4.6°C/W$$

INTERNAL CIRCUIT BLOCK DIAGRAM



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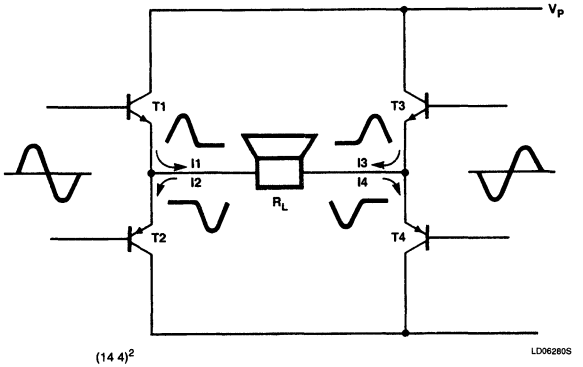

NOTE: P_O ideal $= \frac{(V_{CC}/\sqrt{2})^2}{R_L} = \frac{\frac{(14.4)^2}{2}}{4} = 26W$ (measured at f = 1kHz, d = 10%, P_O = 20.5W)

Figure 1. Output Stage BTL

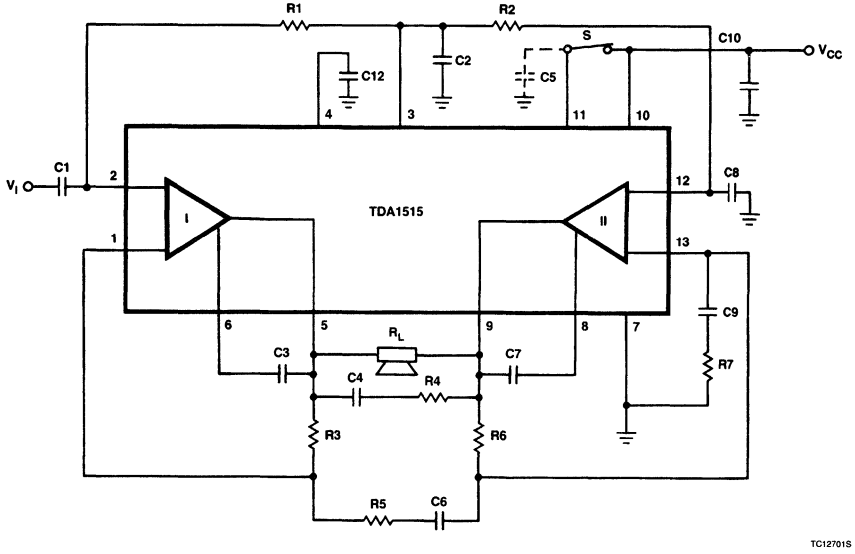

Figure 2. TDA1515 Bridge Application

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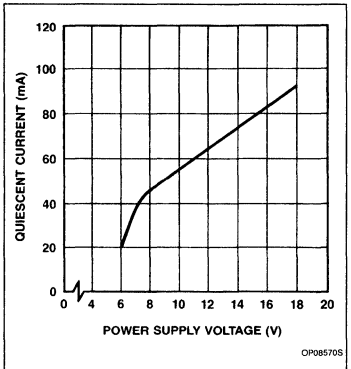

Figure 3. Quiescent Current vs Power Supply Voltage

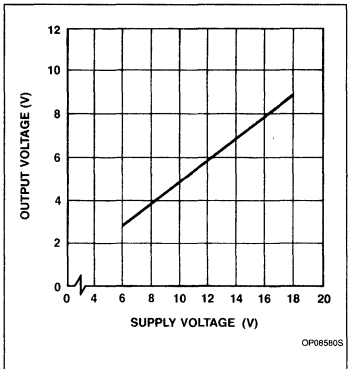

Figure 4. Output Voltage vs Supply Voltage

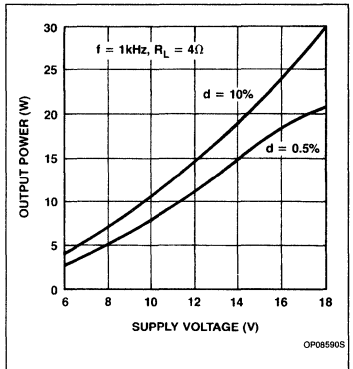

Figure 5. Output Power vs Supply Voltage

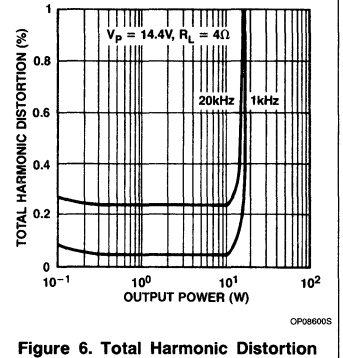

Figure 6. Total Harmonic Distortion vs Output Power

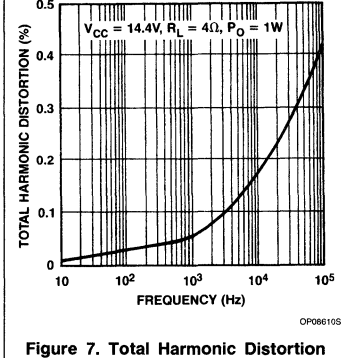

Figure 7. Total Harmonic Distortion vs Frequency

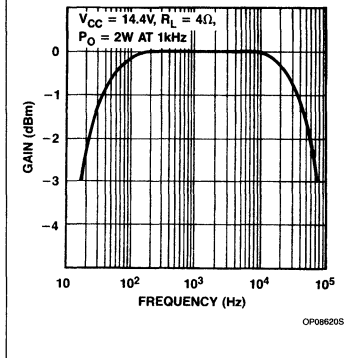

Figure 8. Frequency Characteristic

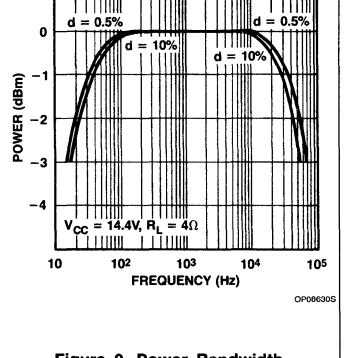

Figure 9. Power Bandwidth

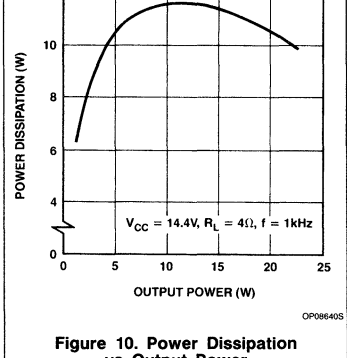

Figure 10. Power Dissipation vs Output Power

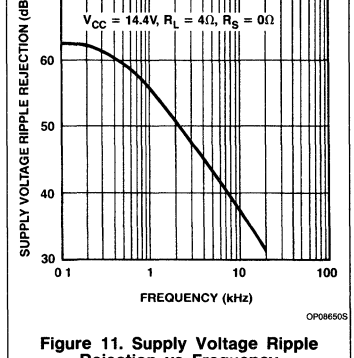

Figure 11. Supply Voltage Ripple Rejection vs Frequency

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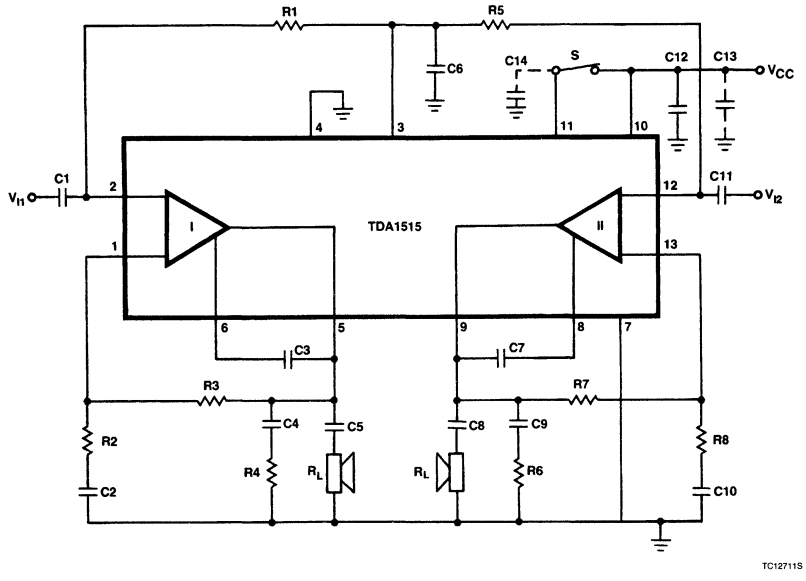

Figure 12. TDA1515 Stereo Application

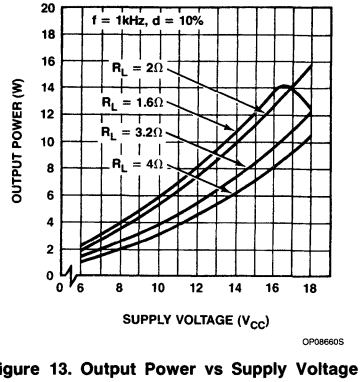

Figure 13. Output Power vs Supply Voltage

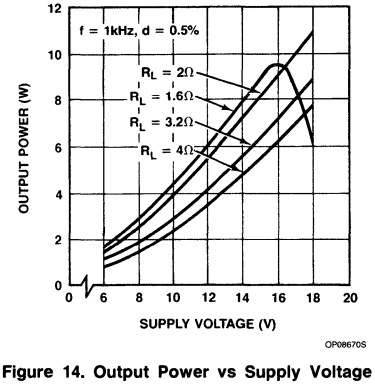

Figure 14. Output Power vs Supply Voltage

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Car Radio Audio Power Amplifiers up to 20W with the TDA1515

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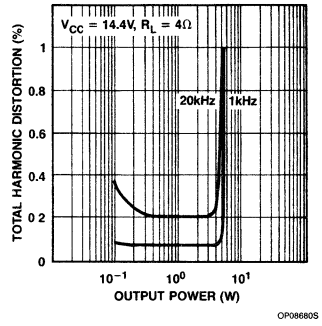


Figure 15. Total Harmonic Distortion vs Output Power

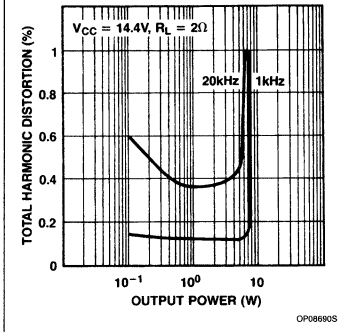


Figure 16. Total Harmonic Distortion vs Output Power

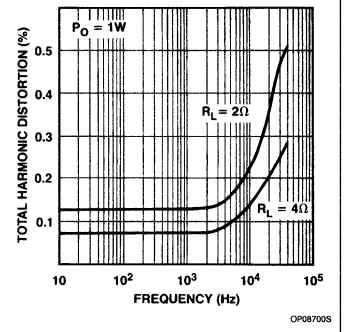


Figure 17. Total Harmonic Distortion vs Frequency

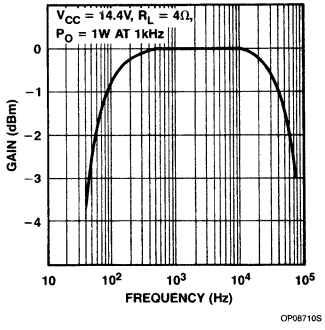


Figure 18. Frequency Characteristic

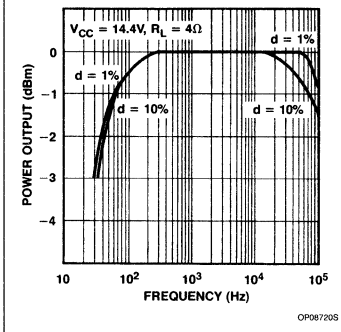


Figure 19. Power Bandwidth

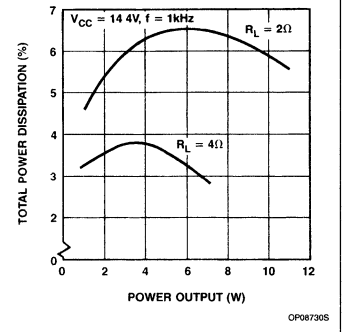


Figure 20. Total Power Dissipation vs Output Power per Channel

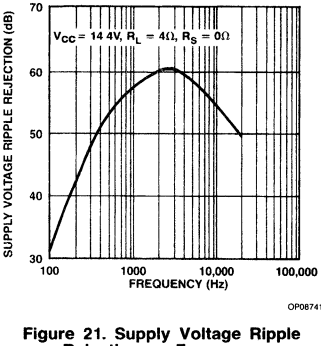


Figure 21. Supply Voltage Ripple Rejection vs Frequency

Signetics

TDA1520B
20W Hi-Fi Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1520B is a 20W hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies.

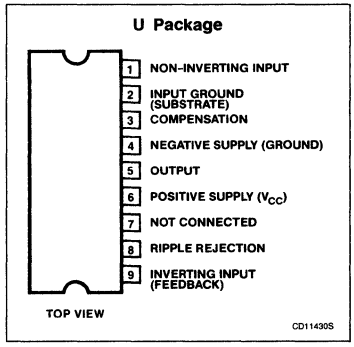
FEATURES

- **Low input offset voltage**
- **Output stage with low cross-over distortion**
- **Single in-line (SIP) power package**
- **AC short-circuit protected**
- **Very low internal thermal resistance**
- **Thermal protection**
- **Very low intermodulation distortion**
- **Very low transient intermodulation distortion**
- **Complete SOA protection**

APPLICATIONS

- **Hi-fi audio power amplifier**
- **Motor driver**
- **Power op amp**

PIN CONFIGURATION



ORDERING INFORMATION

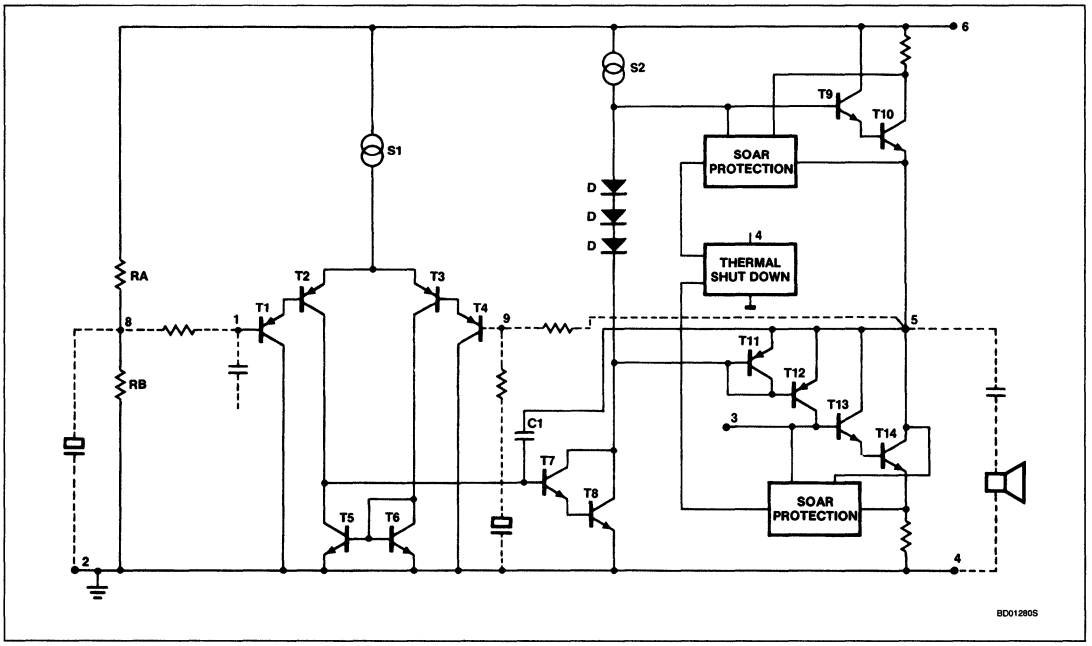
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131A)	−25°C to +150°C	TDA1520BU
9-Pin Plastic SIP (SOT-157A)	−25°C to +150°C	TDA1520BQU

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	50	V
I_{ORM}	Repetitive peak output current	4	A
I_{OSM}	Non-repetitive peak output current	5	A
P_{TOT}	Total power dissipation	see derating curve Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +150	°C

7

SIMPLIFIED INTERNAL CIRCUIT DIAGRAM



DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	15		50	V
I_{TOT}	Total quiescent current at V_{CC} = 33V	22	60	105	mA mA
I_{ORM}	Minimum guaranteed output current (peak value)			3.2	A

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 33V; R_L = 4Ω; f = 1kHz, T_A = 25°C; measured in Test Circuit of Figure 2, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
P_O	Output power sine-wave power at d_{TOT} = 0.5% R_L = 4Ω (Figure 4)	20	22		W
B	Power bandwidth at d_{TOT} = 0.5% from P_O = 50mW to 10W	20Hz			kHz
	Voltage gain				
A_{VO}	open-loop		74		dB
A_{VC}	closed-loop		30		dB
R_{IN}	Internal resistance of Pin 1 (at R_{1-8} = ∞)	1			MΩ
R_{IN}	Input resistance of Test Circuit at Pin 1 (Figure 2)		20		kΩ
V_{IN}	Input sensitivity for P_O = 16W		260		mV
	Signal-to-noise ratio at P_O = 50mW; R_{SOURCE} = 2kΩ				
S/N	f = 20Hz to 20kHz, unweighted;		76		dB
	weighted, measured according to IEC 179 (A-curve)		80		dB
RR	Ripple rejection at f = 100Hz; R_S = 0Ω	45	60		dB
d_{TOT}	Total harmonic distortion at P_O = 16W		0.01		%
R_O	Output resistance (Pin 5)		0.01		Ω
V_O	Input offset voltage		1	100	mV
d_{TIM}	Transient intermodulation distortion at P_O = 10W		0.01		%
d_{IM}	Intermodulation distortion at P_O = 10W		0.02		%
SR	Slew rate		6		V/μs

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POWER DISSIPATION AND HEATSINK INFORMATION

The maximum theoretical power dissipation with a stabilized power supply is (V_{CC} = 33V and R_L = 4Ω):

$$\frac{V_{CC}^2}{2\pi^2 R_L} = 13.8W.$$

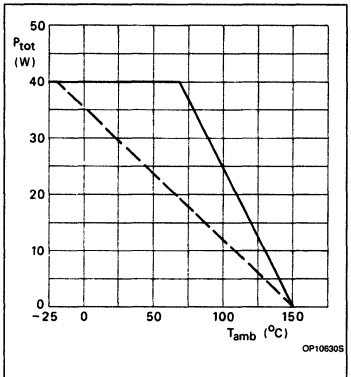
Worst case power dissipation with a non-stabilized power supply is (regulation factor of 15%; over voltage of 10% and R_L min. = 0.8× R_L typ.; V_{CC} is the loaded supply voltage):

$$\frac{(1.1 \times V_{CC})^2}{2\pi^2 R_L \text{ min.}} = 23.4W.$$

With a maximum ambient temperature of 50°C and a maximum crystal temperature of 150°C, the required thermal resistance is:

$$\theta_{JA} = \frac{150 - 50}{23.4} = 4.3°C/W.$$

The thermal resistance of the encapsulation is < 2.5°C/W; therefore, the thermal resistance of the heatsink must be < 1.8°C/W.



NOTES:
—— Mounted on infinite heatsink
- - - Mounted on heatsink of 1.8°C/W

Figure 1. Power Derating Curves

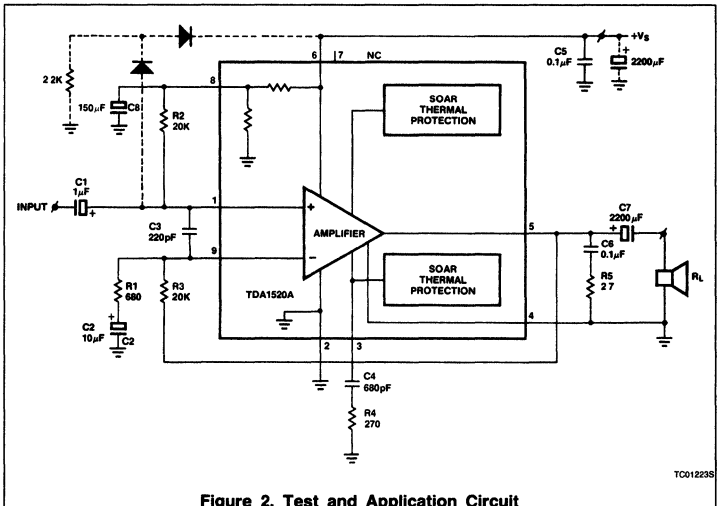


Figure 2. Test and Application Circuit

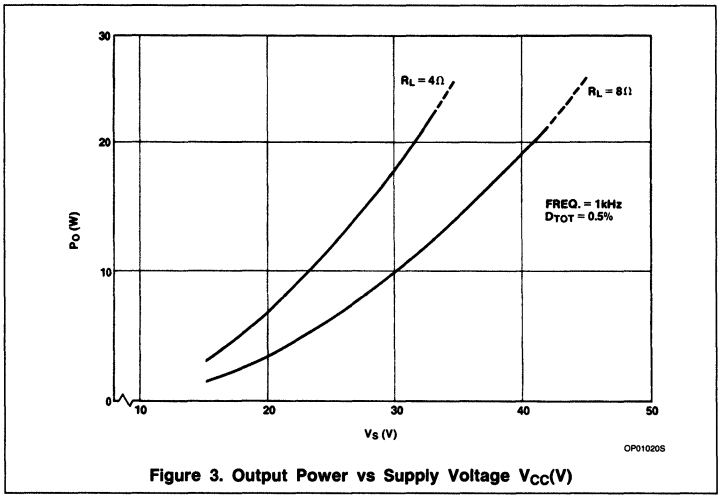


Figure 3. Output Power vs Supply Voltage V_{CC}(V)

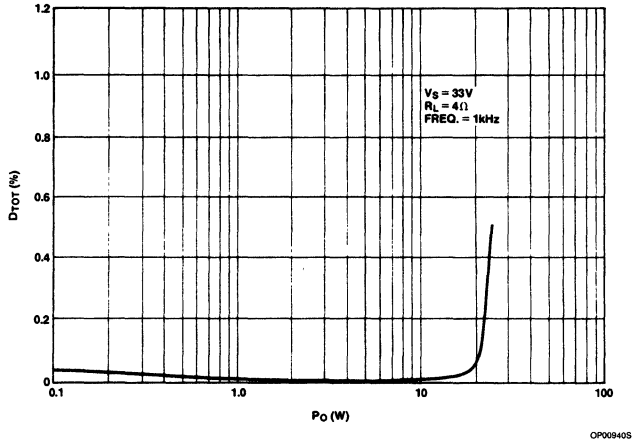


Figure 4. Total Harmonic Distortion (d_{tot})

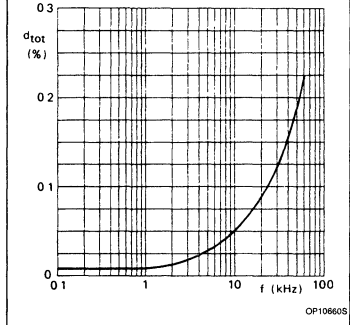


Figure 5. Total Harmonic Distortion (d_{tot}) vs Operating Frequency (f) at V_{CC} = 33V, R_L = 4Ω, P_O = 10W (Constant)

7

Signetics

AN149
20W Hi-Fi Power Amplifier with the TDA1520A

Application Note

Linear Products

Author: D. Udo

ABSTRACT

The TDA1520A single operational hi-fi power amplifier is intended for audio and television applications.

The circuit can deliver output power up to 20W into 4Ω and 8Ω loudspeakers operating either from symmetrical or asymmetrical power supplies.

The 9-lead SOT 131A power encapsulation combines good thermal behavior ($\theta_{JMB} \leqslant 2°C/W$) with a reliable simple mounting to external heatsinks (screw or clip mounting).

The IC has several internal protection circuits to allow misloading conditions.

INTRODUCTION

The TDA1520A integrated operational amplifier in the 9-lead single-in-line plastic power package SOT 131A is intended for use as class-B hi-fi power amplifier.

Some performance specifications are shown below.

– Supply voltage range	15 – 50V
– Minimum guaranteed output current	3.2A
– Maximum non-repetitive output peak current	5A
– Maximum operating ambient temperature	150°C
– Thermal resistance θ_{JC}	$\leqslant 2°C/W$
Input impedance at Pin 1	$> 1 M\Omega$

The TDA1520A can be powered with symmetrical and asymmetrical power supplies. This application note shows applications with asymmetrical power supplies.

INTERNAL CIRCUIT DESCRIPTION

The internal circuit block diagram of the TDA1520A is shown in Figure 1.

The input amplifier is a Darlington-coupled PNP differential stage (T1 – T4) having an 800μA current source S1. DC biasing for T1 can be derived from the internal voltage bleeder RA – RB.

In our application with asymmetrical power supply, the DC biasing is made with an external resistor between Pin 1 and Pin 8. The external resistance between Pin 1 and Pin 8 must be limited to 100 kΩ for offset voltage reasons. The current drive to the class-A driver stage (T7 – T8) is obtained from the current mirror circuit of T5 – T6.

The DC current source S2 (5mA), for the class-A stage T7 – T8 flows through the three series diodes D, to adjust and stabilize the quiescent current of the output stage.

Each branch of the quasi-complementary output stage consists of two Darlington-coupled NPN transistors (T9 – T10 and T13 – T14).

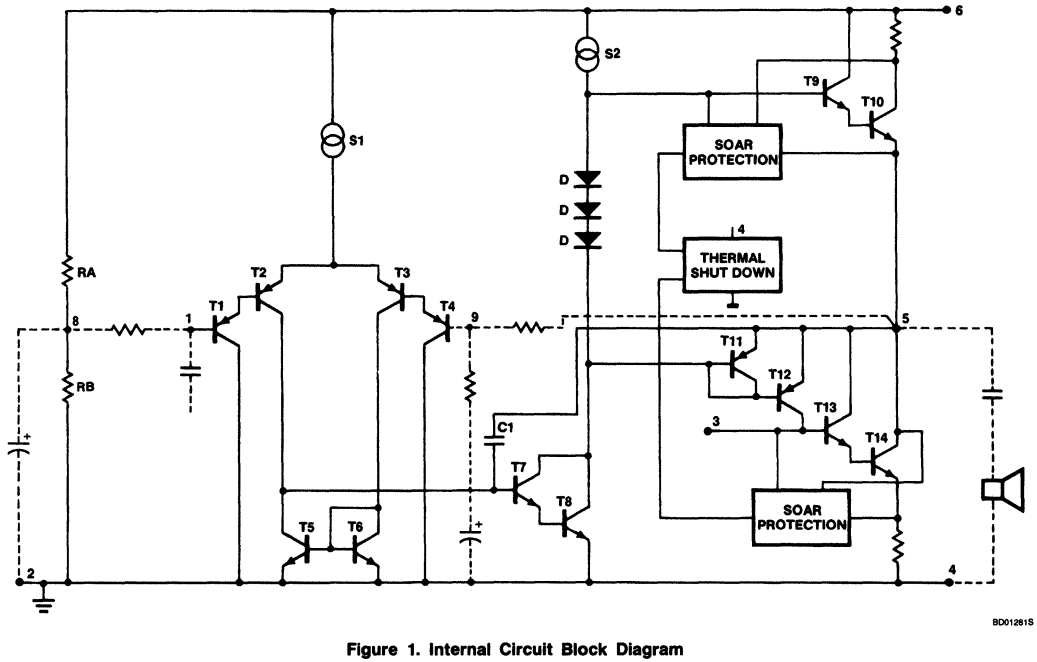


Figure 1. Internal Circuit Block Diagram

20W Hi-Fi Power Amplifier with the TDA1520A AN149

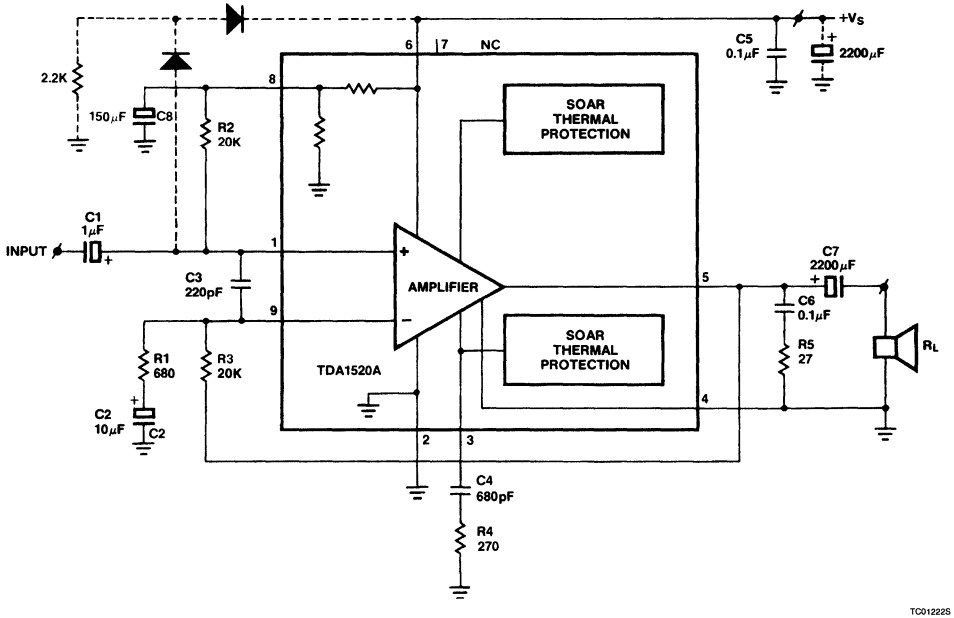


Figure 2. Circuit Diagram

The unity gain PNP class-B driver (T11 – T12) offers the 180° phase-shift for the lower output stage.

The open-loop frequency cut-off is determined by the integrated capacitor C1. Open-loop gain is typical 74dB.

The amplifier has a number of internal circuit blocks to protect the device against short-circuiting of the loudspeaker, misloading conditions (SOAR and thermal protection)

The thermal shut-down circuit starts operating for chip temperatures *higher* than 150°C.

AMPLIFIER APPLICATION CIRCUIT

The circuit diagram of the TDA1520A amplifier operating from an asymmetrical power supply is shown in Figure 2.

The closed-loop gain of 30dB is fixed by the resistors R1 and R3 while the input resistor R2 has the same value as R3 to keep the offset voltage as small as possible

Also to keep the offset voltage low, it is advised to limit the value of R2 to about 100kΩ.

To improve the turn-off behavior, some external components are added These components, a resistor of 2.2kΩ and two diodes, are dashed in Figure 2.

It is recommended to have the power supply electrolytic as close as possible to the amplifier PC board.

With the asymmetrical power supply of 33V, the worst-case power dissipation is 15.5W (see also Figure 18).

Calculation of the heatsink:

$$\theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{P_{TOT}}$$

$$= \frac{(150 - 45)°C}{15.5W} = 6.7\ °C/W$$

The thermal resistance of the heatsink becomes:

$$\theta_{HA} = \theta_{JA} - \theta_{JC} - \theta_{CH}$$
$$= (6.7 - 2 - 0.2)°C/W = 4.5°C/W.$$

In the proposed appliance a 3.5cm extruded heatsink is used (type KL-134 of Seifert).

MEASUREMENTS

Several measurements are done on the application circuit of Figure 2.

Quiescent Current Consumption.

The quiescent current consumption versus supply voltage is given in Figure 3.

Midtap Voltage

The midtap voltage versus supply voltage is given in Figure 4.

Harmonic Distortion

The harmonic distortion versus frequency at P_O = 10W is given in Figure 5 for V_S = 33V and R_L = 4Ω and in Figure 6 for V_S = 42V and R_L = 8Ω.

The harmonic distortion versus output power at f = 1kHz is given in Figure 7 for V_S = 33V and R_L = 4Ω and in Figure 8 for V_S = 42V and R_L = 8Ω.

Power Bandwidth

The power bandwidth for d_{TOT} = 0.5% is given in Figure 9 for V_S = 33V and R_L = 4Ω and in Figure 10 for V_S = 42V and R_L = 8Ω.

Intermodulation Distortion

IM distortion versus output power is given in Figure 11 for V_S = 33V and R_L = 4Ω and in Figure 12 for V_S = 42V and R_L = 8Ω.

Frequency Response

In Figure 13 the frequency response is given for V_S = 33V and R_L = 4Ω and in Figure 14 for V_S = 42V and R_L = 8Ω.

The reference level (0dB) is at 10dB below $P_{O\ MAX}$ (= 2.2W) at f = 1kHz.

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20W Hi-Fi Power Amplifier with the TDA1520A AN149

Output Power
The output power versus supply voltage is given in Figure 15 for $R_L = 4\Omega$ and 8Ω, measured at $d_{TOT} = 0.5\%$ and f = 1kHz.

Power Dissipation
The power dissipation of the TDA1520A as a function of the output power, measured at $V_S = 33V$, f = 1kHz and $R_L = 4\Omega$ is given in Figure 16 and with $V_S = 42V$, f = 1kHz and $R_L = 8\Omega$ in Figure 17.

The worst-case power dissipation versus supply voltage is shown in Figure 18.

Input And Output Impedance
The input impedance of the TDA1520A at Pin 1 is > 1 mΩ. The input impedance of the application circuit of Figure 2 is 20kΩ, determined by the external resistor R2.

The output impedance at Pin 5 is 10 mΩ at f = 1kHz.

Gain
The input sensitivity for $P_O = 10W$ is 210mV. The closed-loop gain measured at f = 1kHz is 30dB. The closed-loop gain can be varied by resistors R1 and R3.

Noise
The weighted signal-to-noise ratio at $P_O = 50mW$ and $R_S = 2\ k\Omega$ is 80dB measured according to IEC 179 (A-curve).

The unweighted noise (f = 20Hz – 20kHz) is 76dB.

Measured according to CCIR 468 peak value (also new DIN 45405 standard) this signal-to-noise ratio is 66dB.

Slew Rate
The slew rate of the amplifier is 6V/μs.

Supply Voltage Ripple Rejection
The supply voltage ripple rejection at f = 100Hz, is 58dB ($R_S = 0$).

Short-Circuit Behavior
AC short-circuiting is possible during 60 sec, measured with sine wave drive f ⩾ 40Hz into clipping at a supply voltage of 30V and with a supply series resistance of 4Ω.

Measuring under the same conditions but with pink noise drive, according to IEC 268-1C, AC short-circuiting is allowed up to 15 minutes.

Turn-on and -off Behavior
With the extra network the turn-off behavior of the TDA1520A can be improved.

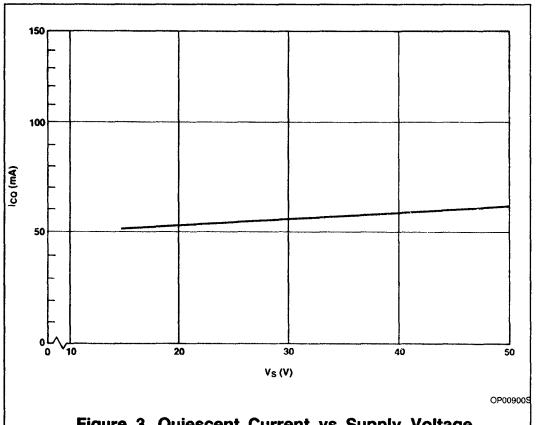

Figure 3. Quiescent Current vs Supply Voltage

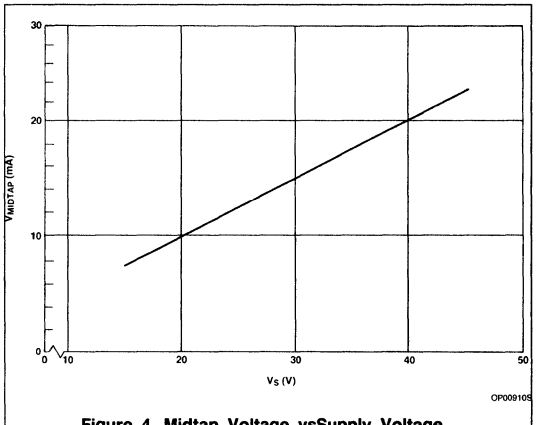

Figure 4. Midtap Voltage vsSupply Voltage

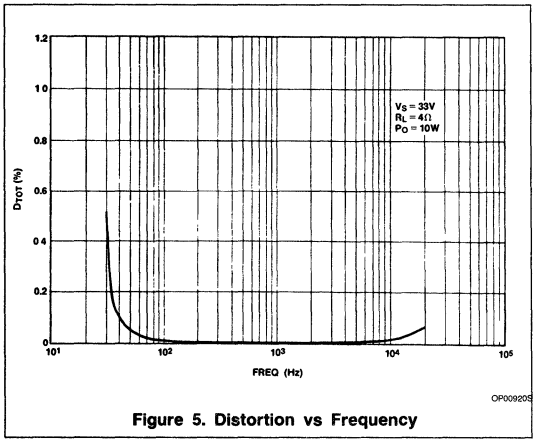

Figure 5. Distortion vs Frequency

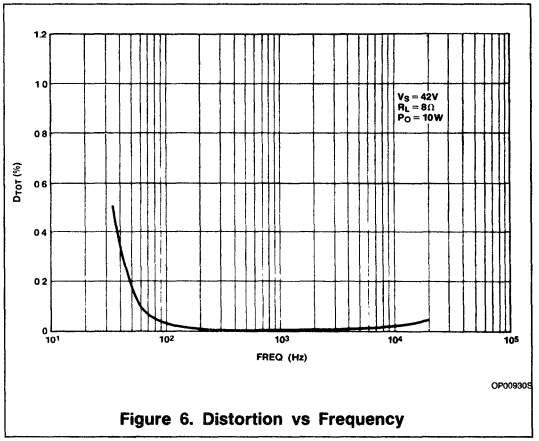

Figure 6. Distortion vs Frequency

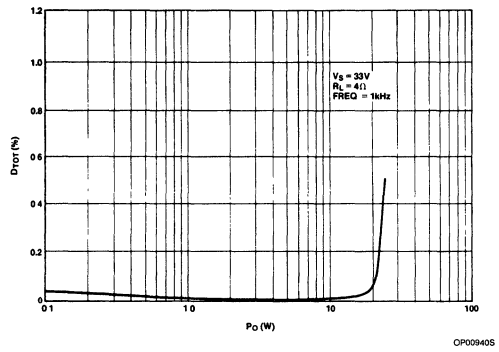

Figure 7. Distortion vs Output Power

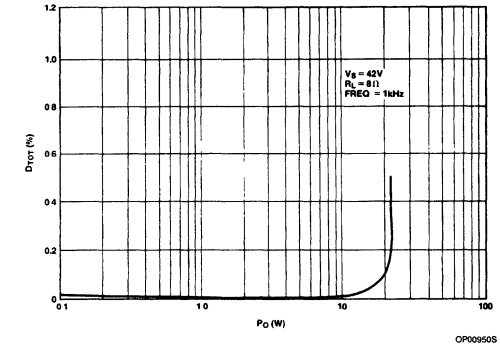

Figure 8. Distortion vs Output Power

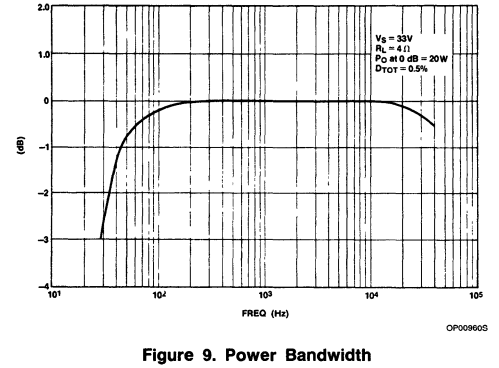

Figure 9. Power Bandwidth

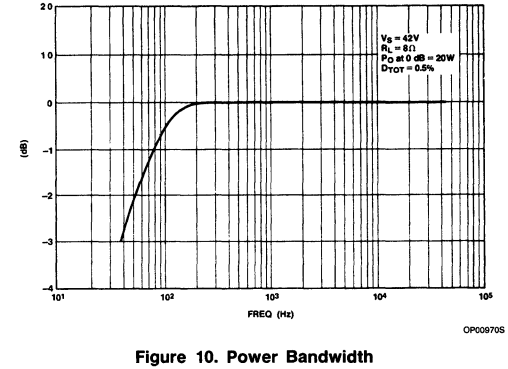

Figure 10. Power Bandwidth

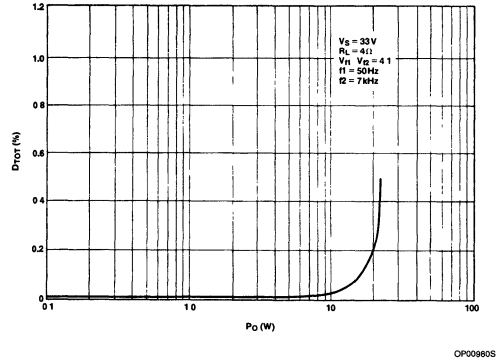

Figure 11. IM Distortion vs Output Power

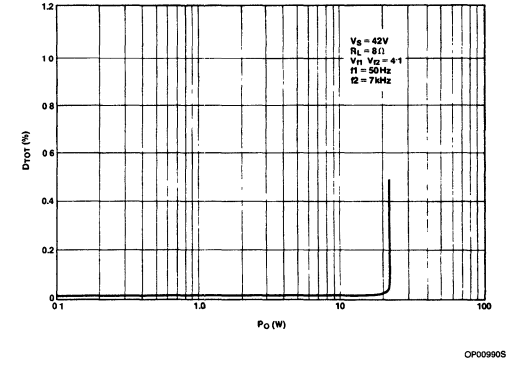

Figure 12. IM Distortion vs Output Power

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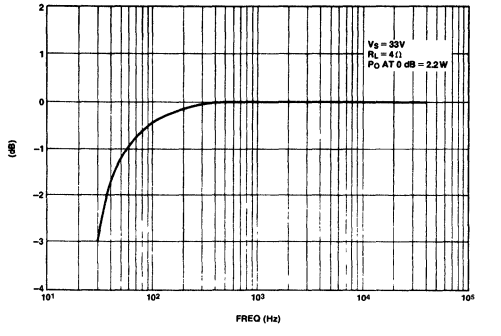


Figure 13. Frequency Response at P_O = 2.2W

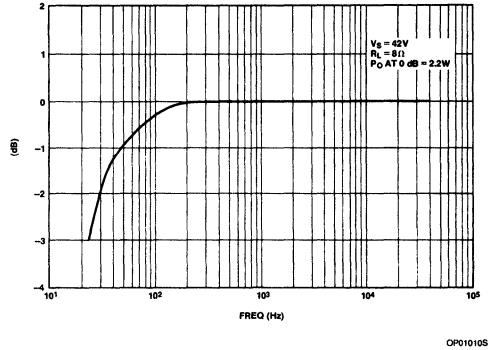


Figure 14. Frequency Response at P_O = 2.2W

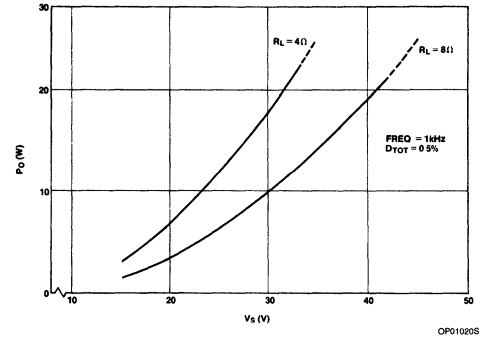


Figure 15. Output Power vs Supply Voltage

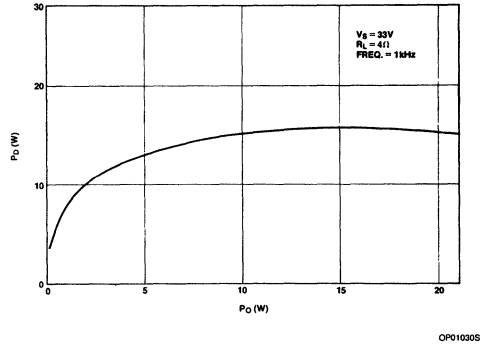


Figure 16. Power Dissipation vs Output Power

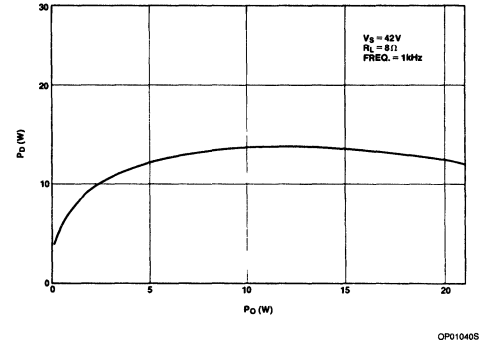


Figure 17. Power Dissipation vs Output Power

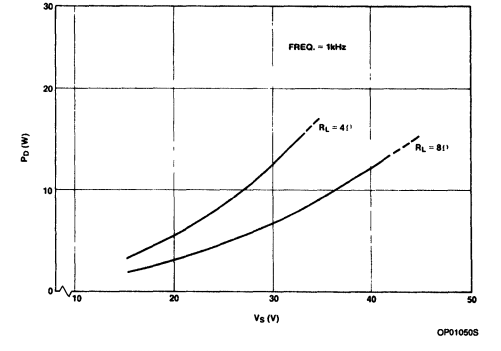


Figure 18. Worst-Case Power Dissipation vs Supply Voltage

TDA1521
2 × 12 Hi-Fi Audio Power Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA1521 is a dual hi-fi audio power amplifier in a 9-lead single in-line (SIL-9) plastic power package. The device is especially designed for mains-fed applications (e.g., stereo TV sound and stereo radio).

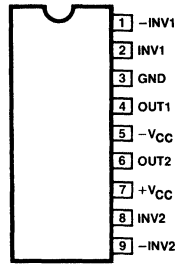
FEATURES

- **Requires very few external components**
- **Input muted during power-on and -off (no switch-on or switch-off sounds)**
- **Low offset voltage between output and ground**
- **Excellent gain balance between channels**
- **Hi-fi according to IEC 268 and DIN 45500**
- **Short-circuit-proof**
- **Thermally protected**

APPLICATIONS

- **Stereo**
- **TV sound**
- **Radio**

PIN CONFIGURATION



TOP VIEW

CD10361S

PIN NO.	SYMBOL	DESCRIPTION
1	-INV1	Non-inverting input 1
2	INV1	Inverting input 1
3	GND	Ground
4	OUT1	Output 1
5	$-V_{CC}$	Negative supply
6	OUT2	Output 2
7	$+V_{CC}$	Positive supply
8	INV2	Inverting input 2
9	-INV2	Non-inverting input 2

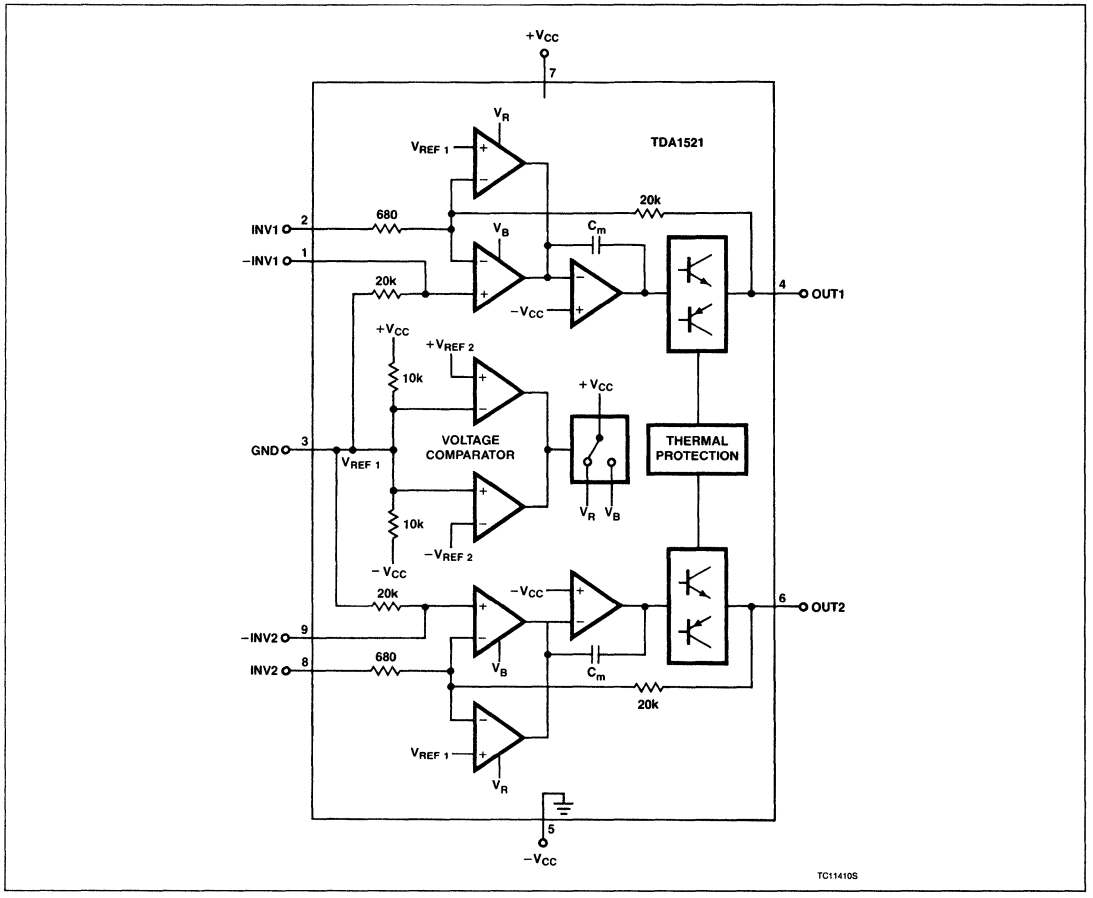
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131B)	0 to +70°C	TDA1521U

7

2 × 12 Hi-Fi Audio Power Amplifier TDA1521

BLOCK DIAGRAM



2 × 12 Hi-Fi Audio Power Amplifier | TDA1521

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains-fed applications. The circuit is optimal for symmetrical power supplies but it is also well suited to asymmetrical power supply systems. An output power of 2 × 12W (THD = 0.5%) can be delivered into an 8Ω load with a symmetrical power supply of ±16V.

The gain is fixed internally at 30dB, but can be changed externally if required. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0.2dB).

A special feature is an input mute circuit which provides suppression of unwanted signals at the inputs during switching on and off. This circuit disconnects the non-inverting inputs when the supply voltage is below ±6V, while allowing the amplifiers to remain in their DC operating condition.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150°C, allowing safe operation to a maximum junction temperature of 150°C without added distortion.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{5,\ 7-3}$	Supply voltage (Pins 5 and 7)	+20	V
I_{OSM}	Non-repetitive peak output current (Pins 4 and 6)	4	A
P_{TOT}	Total power dissipation	see Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_j	Junction temperature	+150	°C
t_{SC}	Short-circuit time: outputs short-circuited to ground Symmetrical power supply	1	hour
t_{SC}	Asymmetrical power supply; V_{CC} < *V (unloaded); $R_l \geqslant$ *Ω	1	hour
θ_{JC}	Thermal resistance from junction to case	25	°C/W

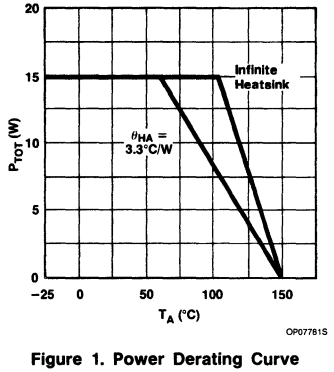


Figure 1. Power Derating Curve

HEATSINK DESIGN EXAMPLE

With derating of 2.5°C/W, the value of heatsink thermal resistance is calculated as follows: given $R_L = 8\Omega$ and $V_{CC} = \pm 16V$, the measured maximum dissipation is 14.6 W; then, for a maximum ambient temperature of 65°C, the required thermal resistance of the heatsink is

$$\theta_{HA} = \frac{150 - 65}{14.6} - 2.5 = 3.3°C/W$$

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			±16	±20	V
I_{ORM}	Repetitive peak output current				2.2	A
Operating mode: symmetrical power supply; test circuit as per Figure 2; V_{CC} = ±16V; R_L = 8Ω; T_A = 25°C; f = 1kHz						
V_{CC}	Supply voltage range		±7.5	±16	±20	V
I_{TOT}	Total quiescent current	without R_L		50	*	mA
P_O P_O	Output power	THD = 0.5% THD = 10%	10	12 15		W W
THD	Total harmonic distortion	P_O = 6W		*	0.2	%
B	Power bandwidth[1]	THD = 0.5%	20Hz to 20kHz			
G_V	Voltage gain		29	30	31	dB
ΔG_V	Gain balance			0.2		dB
$V_{NO(RMS)}$	Noise output voltage (RMS value); unweighted (20Hz to 20kHz)	R_S = 2kΩ		70	140	μV
$\|Z_i\|$	Input impedance		14	20	26	kΩ
RR	Ripple rejection[2]		40	60		dB
∞	Channel separation	R_S = 0Ω	46	70		dB
I_{IB}	Input bias current			0.3		μA
V_{OFF}	DC output offset voltage	WRT GND		20	200	mV
Input mute mode: symmetrical power supply; test circuit as per Figure 2; V_{CC} = ±4V; R_L = 8Ω; T_A = 25°C; f = 1kHz						
V_{CC}	Supply voltage		±2		±5.8	V
I_{TOT}	Total quiescent current	without R_L		30	*	mA
V_{OUT}	Output voltage	V_I = 600mV			1.8	mV
$V_{NO(RMS)}$	Noise output voltage (RMS value); unweighted (20Hz to 20kHz)	R_S = 2kΩ		70	140	μV
RR	Ripple rejection[2]		35			dB
V_{OFF}	DC output offset voltage	WRT GND		20	200	mV
Operating mode: asymmetrical power supply; test circuit as per Figure 3; V_{CC} = ±4V; R_L = 8Ω; T_A = 25°C; f = 1kHz						
I_{TOT}	Total quiescent current			50	*	mA
P_O P_O	Output power	THD = 0.5% THD = 10%	5	6 8.5		W W
THD	Total harmonic distortion	P_O = 4W		*	0.2	%
B	Power bandwidth	THD = 0.5%[1]	40Hz		20	kHz
G_V	Voltage gain		29	30	31	dB
ΔG_V	Gain balance			0.2		dB
$V_{NO(RMS)}$	Noise output voltage (RMS value); unweighted (20Hz to 20kHz)	R_S = 2kΩ		70	140	μV
$\|Z_i\|$	Input impedance		14	20	26	kΩ
RR	Ripple rejection[2]		40	50		dB
∞	Channel separation	R_S = 0Ω	40			dB

NOTES:
1 Power bandwidth at $P_{O\ MAX}$ −3dB
2 Ripple rejection at R_S = 0Ω, f = 100Hz to 20kHz; ripple voltage = 200mV (RMS value) applied to positive or negative supply rail.

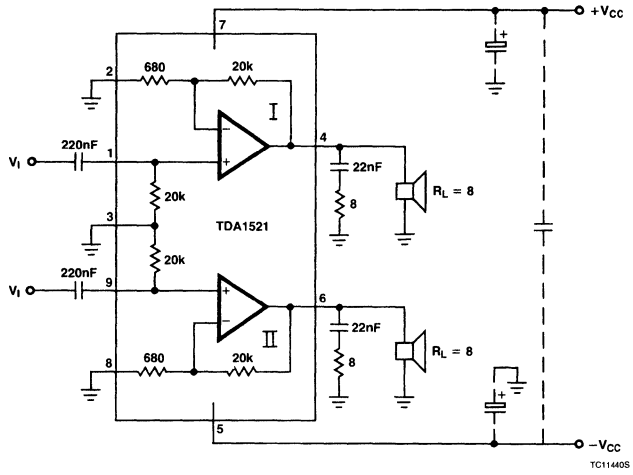

Figure 2. Test and Application Circuit; Symmetrical Power Supply

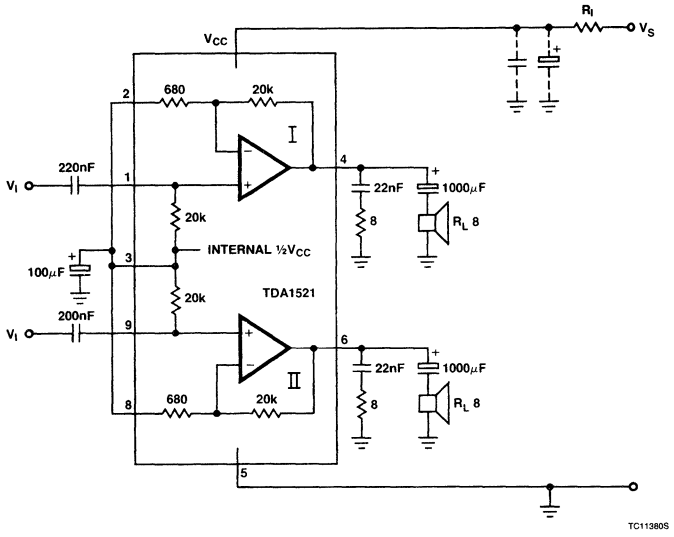

Figure 3. Test and Application Circuit; Asymmetrical Power Supply

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Signetics

TDA2611A
5W Audio Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA2611A is a 5W audio amplifier in a 9-pin single in-line (SIP) plastic package.

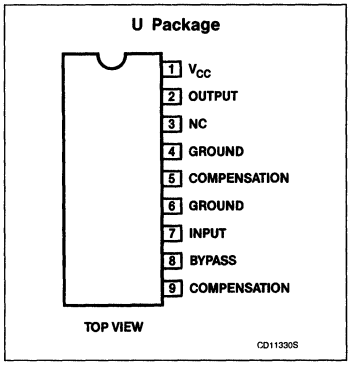
FEATURES

- **Possibility for increasing the input impedance**
- **Single in-line (SIP) construction for easy mounting**
- **Extremely low number of external components**
- **Thermal protection**
- **Well-defined open-loop gain circuitry with simple quiescent current setting and fixed integrated closed-loop gain**

APPLICATIONS

- **TV**
- **Radio**
- **Record player**
- **Communication receiver**
- **Alarms**

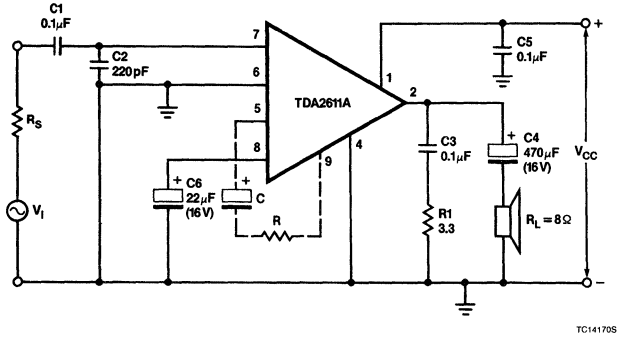
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-110B)	−25°C to +150°C	TDA2611AU

TEST CIRCUIT



NOTES:
Pin 3 not connected
Input impedance can be increased by applying C and R between Pins 5 and 9 (see also Figures 4 and 5)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	35	V
I_{OSM}	Non-repetitive peak output current	3	A
I_{ORM}	Repetitive peak output current	1.5	A
P_{TOT}	Total power dissipation	see derating curves Figure 1	
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +150	°C

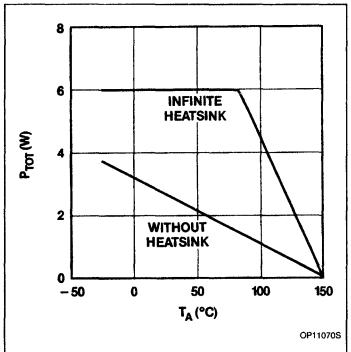


Figure 1. Power Derating Curves

HEATSINK EXAMPLE

Assume V_{CC} = 18V; R_L = 8Ω; T_A = 60°C maximum; T_J = 150°C (max. for a 4W application into an 8Ω load, the maximum dissipation is about 2.2W). The thermal resistance from junction to ambient can be expressed as:

$$\theta_{JA} = \theta_{JTAB} + \theta_{TABH} +$$

$$\theta_{HA} = \frac{150 - 60}{2.2} = 41°C/W.$$

Since θ_{JTAB} = 11°C/W and
θ_{TABH} = 1°C/W,
θ_{HA} = 41 − (11 + 1) = 29°C/W.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	6		35	V
I_{ORM}	Repetitive peak output current			1.5	A
I_{TOT}	Total quiescent current at V_{CC} = 18V		25	25	mA

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AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = 18V$; $R_L = 8\Omega$; f = 1kHz, unless otherwise specified, see also Figure 2.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
P_O	AF output power at $d_{TOT} = 10\%$ $V_{CC} = 18V$; $R_L = 8\Omega$ $V_{CC} = 12V$; $R_L = 8\Omega$ $V_{CC} = 8.3V$; $R_L = 8\Omega$ $V_{CC} = 20V$, $R_L = 8\Omega$ $V_{CC} = 25V$; $R_L = 15\Omega$		4	 4.5 1 7 0.65 6 5		W W W W W W
d_{TOT}	Total harmonic distortion at $P_O = 2W$		1	0 3		%
	Frequency response		15			kHz
$\|Z_I\|$	Input impedance			45		kΩ[1]
V_N	Noise output voltage at $R_S = 5k\Omega$; B = 60Hz to 15kH z			0.2	0.5	mV mV
V_I	Sensitivity for $P_O = 2.5W$		44	55	66	mV mV

NOTE:

1. Input impedance can be increased by applying C and R between Pins 5 and 9 (see also Figures 4 and 5).

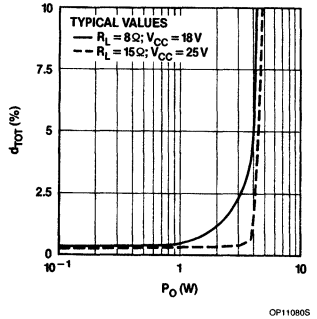


Figure 2. Total Harmonic Distortion as a Function of Output Power

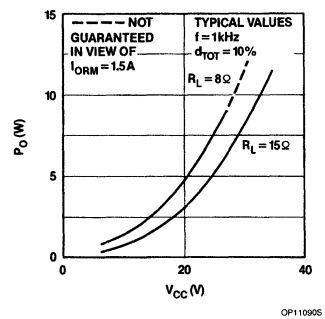
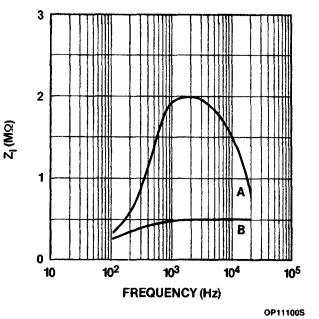
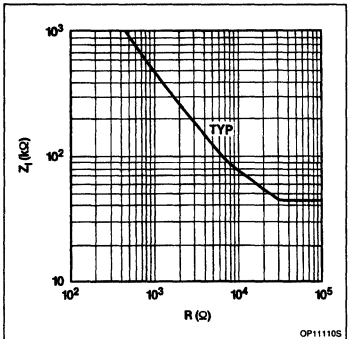


Figure 3. Output Power as a Function of Supply Voltage



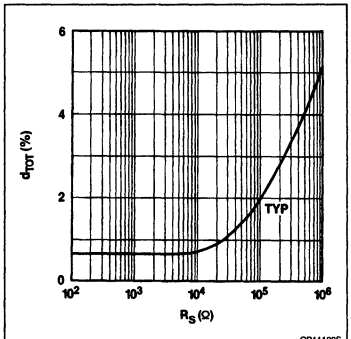
NOTES:
Curve a for C = 1μF, R = 0Ω,
Curve b for C = 1μF, R = 1kΩ,
C2 = 10pF, typical values

Figure 4. Input Impedance as a Function of Frequency



NOTE:
C = 1μF, f = 1kHz.

Figure 5. Input Impedance as a Function of R(Ω) in Test Circuit



NOTE:
P_O = 3.5W; f = 1kHz.

Figure 6. Total Harmonic Distortion as a Function of R_S(Ω) in the Test Circuit

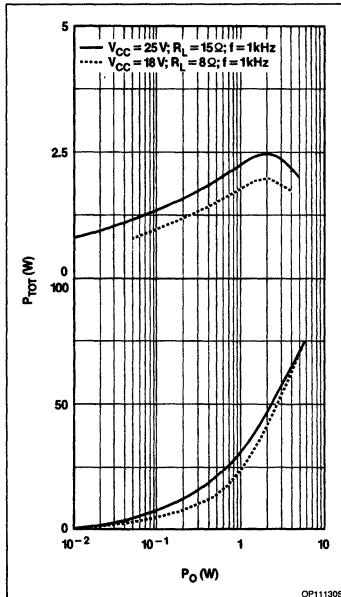


Figure 7. Total Power Dissipation and Efficiency as a Function of Output Power

APPLICATION INFORMATION

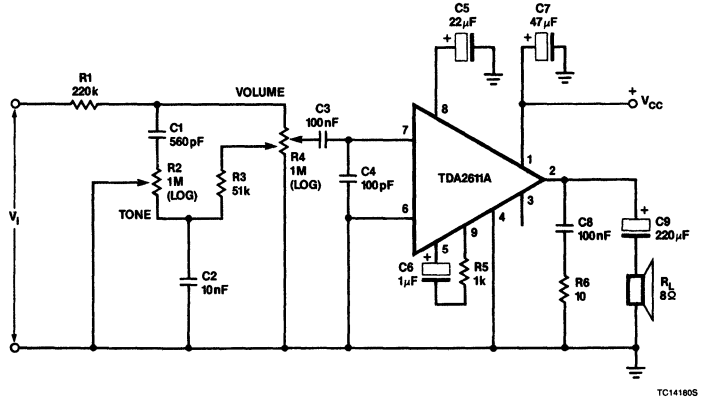
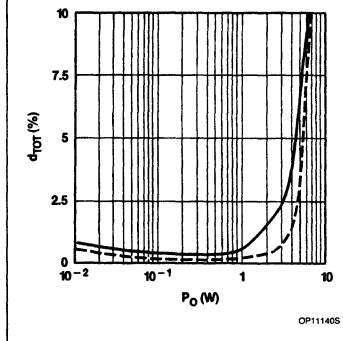


Figure 8. Ceramic Pick-Up Amplifier Circuit



NOTES:
—— with tone control
- - - without tone control, in circuit of Figure 8, typical values

Figure 9. Total Harmonic Distortion as a Function of Output Power

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Signetics

TDA7050
Low Voltage Mono/Stereo Power Amplifier

Product Specification

Linear Products

DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

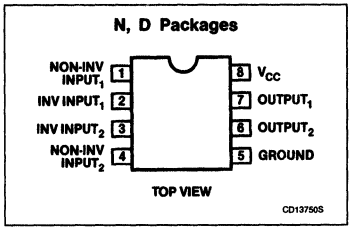
FEATURES

- **Limited to battery supply application only (Typ. 3 and 4V)**
- **Operates with supply voltage down to 1.6V**
- **No external components required**
- **Very low quiescent current**
- **Fixed integrated gain of 26dB, floating differential input**
- **Flexibility in use — mono BTL as well as stereo**
- **Small dimension of encapsulation**

APPLICATIONS

- **Portable radio**
- **Personal computer**
- **Speech synthesis**
- **Telephone**
- **Modem**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO Package (SOT-96A; SO-8)	0 to +70°C	TDA7050TD
8-Pin Plastic DIP (SOT-97A)	0 to +70°C	TDA7050TN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
I_{OM}	Peak output current	150	mA
P_{TOT}	Total power dissipation	see derating curve, Figure 1	
T_{STG}	Storage temperature range	−55 to +150	°C
T_C	Crystal temperature	100	°C
t_{SC}	AC and DC short-circuit duration at V_{CC} = 3.0V (during mishandling)	5	s

DC ELECTRICAL CHARACTERISTICS V_{CC} = 3V; f = 1kHz; R_L = 32Ω; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Supply					
V_{CC}	Supply voltage	1.6		6.0	V
I_{TOT}	Total quiescent current		3.2	4	mA
Bridge-tied load application (BTL); see Figure 4					
P_O	Output power[1] V_{CC} = 3.0V; d_{tot} = 10%		140		mW
P_O	V_{CC} = 4.5V; d_{tot} = 10% (R_L = 64Ω)		150		mW
G_V	Voltage gain		32		dB
$V_{NO(RMS)}$	Noise output voltage (RMS value) R_S = 5kΩ; f = 1kHz		140		μV
$\|\Delta V\|$	DC output offset voltage (at R_S = 5 kΩ)			70	mV
$\|Z_I\|$	Input impedance (at R_S = ∞)	1			MΩ
I_I	Input bias current		40		nA
Stereo application; see Figure 5					
P_O	Output power[1] V_{CC} = 3.0V; d_{tot} = 10%		35		mW
P_O	V_{CC} = 4.5V; d_{tot} = 10%		75		mW
G_V	Voltage gain		26		dB
$V_{NO(RMS)}$	Noise output voltage (RMS value) R_S = 5kΩ; f = 1kHz		100		μV
α	Channel separation R_S = 0Ω; f = 1kHz	30	40		dB
$\|Z_I\|$	Input impedance (at R_S = ∞)	2			MΩ
I_I	Input bias current		20		nA

NOTE:

1. Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Figure 2 (BTL Application) and in Figure 3 (Stereo Application).

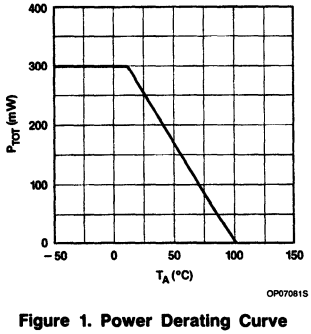


Figure 1. Power Derating Curve

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{J\ MAX} - T_A}{\theta_{JA}} = \frac{100 - 60}{300} = 0.1\ W$$

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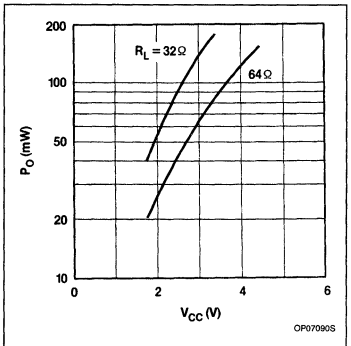


Figure 2. Output Power Across the Load Impedance (R_L) as a Function of Supply Voltage (V_{CC}) in BTL Application. Measurements Were Made at f = 1kHz; d_{tot} = 10%; T_A = 25°C

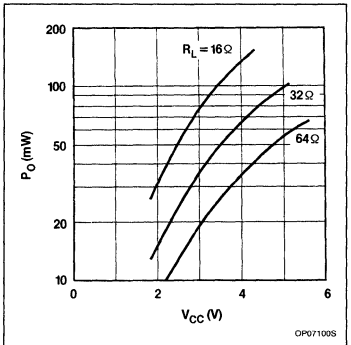


Figure 3. Output Power Across the Load Impedance (R_L) as a Function of Supply Voltage (V_{CC}) in Stereo Application. Measurements Were Made at f = 1kHz; d_{tot} = 10%; T_A = 25°C

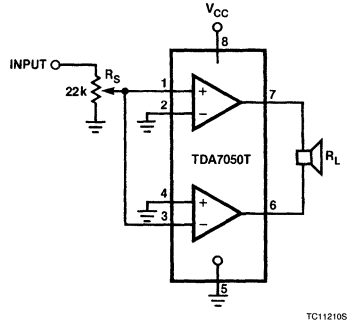


Figure 4. Application Diagram (BTL); Also Used as Test Circuit

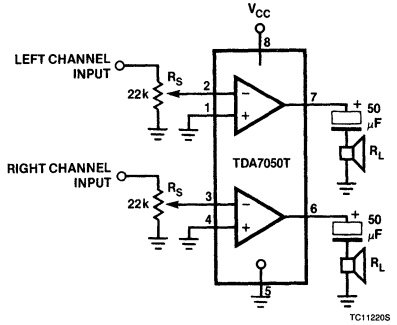


Figure 5. Application Diagram (Stereo); Also Used as Test Circuit

Signetics

TDA7052
1 Watt Low Voltage Audio Power Amplifier

Preliminary Specification

Linear Products

DESCRIPTION

The TDA7052 is a 1 Watt power amplifier in an 8-pin DIP plastic package. The device is designed for audio applications. It can be used for motor driver applications. It operates from a supply voltage of 3 to 15V. It has a proprietary circuit design making use of the Bridge-Tied Load (BTL) principle. The TDA7052 makes use of no external passive components.

FEATURES

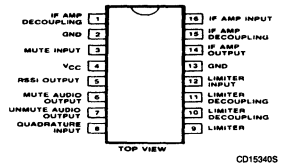
- **No external components**
- **No switch-on or switch-off clicks**
- **Good overall stability**
- **Low power consumption**
- **No external heatsink required**
- **Short-circuit proof**

APPLICATIONS

- **Communications equipment**
- **Speech synthesis output**
- **Portable equipment**
- **Motor drivers**
- **Audio amplifiers**
- **Personal computers**
- **Radio/TV**

PIN CONFIGURATION

N Package



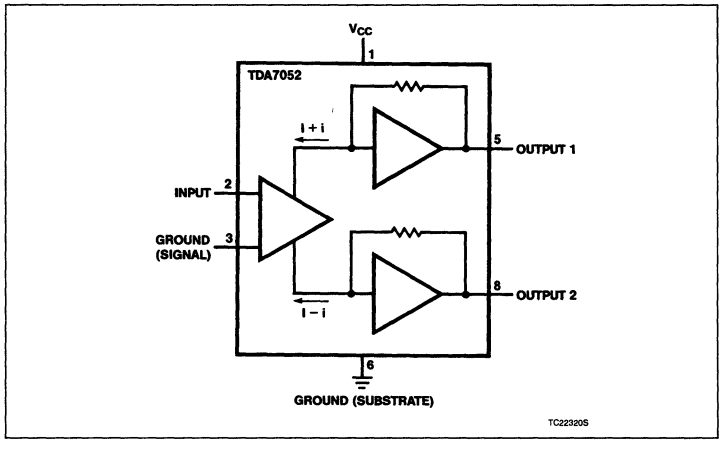
CD15340S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{CC}	Supply voltage.
2	IN	Input
3	GND_1	Ground (signal)
4	NC	Not connected.
5	OUT_1	Output 1
6	GND_2	Output 2.
7	NC	Not connected.
8	OUT_2	Output 2

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic package (SOT-97)	0°C to +70°C	TDA7052PN

BLOCK DIAGRAM



TC22320S

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1 Watt Low Voltage Audio Power Amplifier TDA7052

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{OSM}	Non-repetitive peak output current	1.5	A
P_{TOT}	Operating ambient temperature range	See Figure 1	mW
T_C	Operating junction	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CCA} = 6V; R_L = 8Ω; f = 1kHZ; T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		3	6	15	V
I_{TOT}	Total quiescent current	R_L = ∞	—	4	8	mA
G_V	Voltage gain		39	40	41	dB
P_O	Output power	THD = 10%	1.0	1.2	—	W
	Noise output voltage[1,2] (RMS value)					
$V_{NO(RMS)}$			—	150	300	μV
$V_{NO(RMS)}$			—	60	—	dB
f_R	Frequency response		20		20k	Hz
SVRR	Supply voltage ripple rejection		40	50	—	dB
ΔV_{5-8}	DC output offset voltage Pin 5 – 8	R_S = 5kΩ	—	—	100	mV
THD	Total harmonic distortion	PO = 0.1W	—	0.2	1.0	%
$\|Z_I\|$	Input impedance		—	100	—	kΩ
I_{BIAS}	Input bias current		—	100	300	nA

NOTES:

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60kHz with a source impedance (R_S) of 5kΩ.
2. The RMS output voltage is measured at a bandwidth of 5kHz with a source impedance of 0Ω and a frequency of 500kHz. With a practical load (R = 8Ω; L = 200μH), the noise output current is only 100nA.
3. Ripple rejection is measured at the output with a source impedance of 0Ω and a frequency between 100Hz and 10kHz The ripple voltage = 200mV (RMS value) is applied to the positive supply rail.

1 Watt Low Voltage Audio Power Amplifier | TDA7052

FUNCTIONAL DESCRIPTION

The TDA7052 is an output amplifier designed for battery-powered portable audio applications, such as portable and industrial equipment. The TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1.2W (THD = 10%) into an 8Ω load with a power supply of 6V. The load can be short-circuited at each signal output. The gain is fixed internally at 40dB.

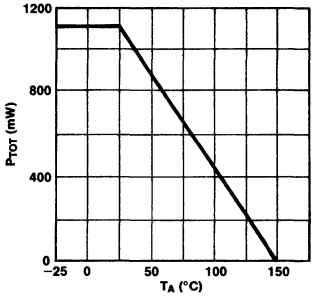

Figure 1. Power Derating Curve.

POWER DISSIPATION

Assume V_{CC} = 6V; R_L = 8Ω; T_A = 50°C maximum.

The maximum sinewave dissipation is 0.9W.

θ_{JA} = (150-50)/0.9 ≈ 110°C/W.

Where θ_{JA} of the package is 110°C/W, so no external heatsink is required.

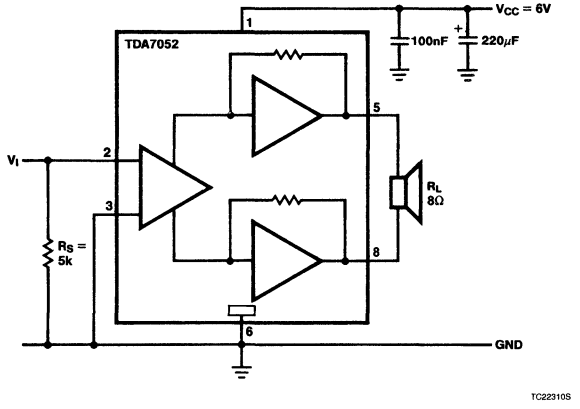

Figure 2. TDA7052 Application Diagram.

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Signetics

SAA7210
Decoder for Compact Disc Digital Audio System

Product Specification

Linear Products

DESCRIPTION

The SAA7210 incorporates the functions of demodulator, subcoding processor, error corrector, and concealment in one chip. The device accepts data from the disc and outputs serial data directly to a dual 16-bit digital-to-analog converter TDA1541 (DAC) via the Inter-IC signal bus (I^2S). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus oversampling digital filtering. For descriptive purposes, the SAA7210 is referred to as the A-chip and the SAA7220 as the B-chip.

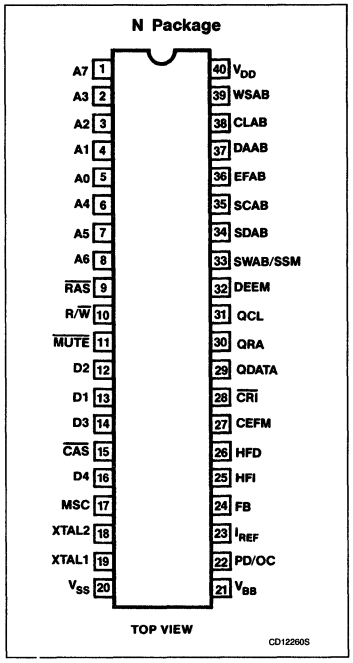
FEATURES

- **Adaptive slicer with high-frequency level detector for input data**
- **Built-in drop-out detector to prevent error propagation in adaptive slicer**
- **Fully protected timing synchronization to incoming data**
- **Eight-to-Fourteen Modulation (EFM) decoding**
- **Cross-Interleaved Reed-Solomon Code (CIRC) used for error correction system**
- **Subcoding microprocessor handshaking protocol**
- **Motor speed control logic which stabilizes the input data rate**
- **Error flag processing to identify unreliable data**
- **Concealment to replace uncorrectable data**
- **I^2S bus for data exchange between A-chip, B-chip, and DAC**
- **Bidirectional data bus to external RAM (16k × 4 bits)**

APPLICATION

- **Compact disc digital audio system**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	−20°C to +70°C	SAA7210N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 40)	−0.5 to +7.0	V
V_I	Maximum input voltage range	−0.5 to V_{DD} + 0.5	V
I_I	Input current (Pin 23)	5	mA
V_O	Maximum output voltage range (Pin 17, 33)	−0.5 to +7.0	V
I_O	Output current (each output)	10	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
V_{ES}	Electrostatic handling*	−1000 to +1000	V

NOTE:
*Equivalent to discharging a 100pF capacitor through a 1.5kΩ series resistor with a rise time of 15ns.

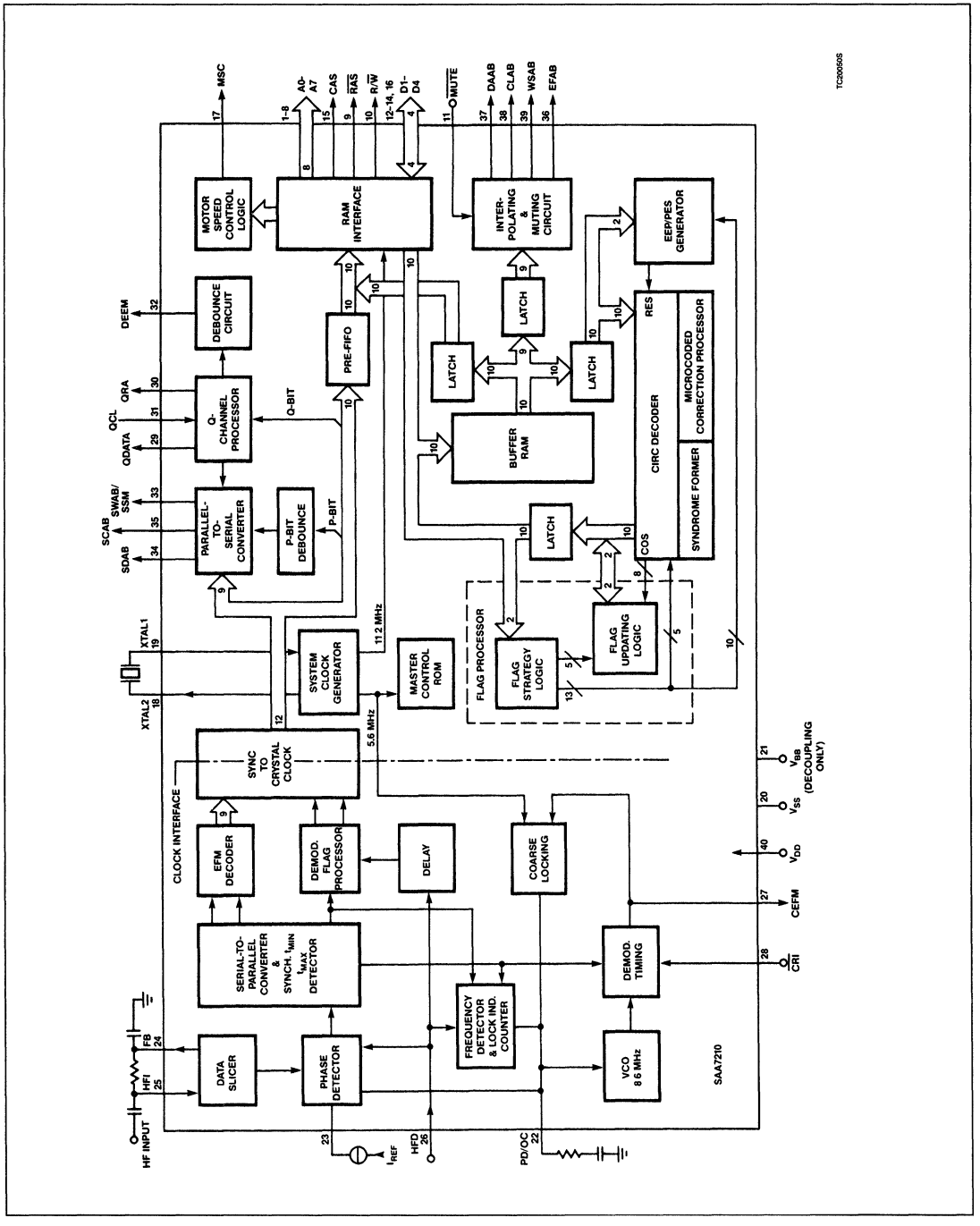
PIN DESCRIPTION

PIN NO.	MNEMONIC	DESCRIPTION
1 – 8	A0 – A7	**Address:** address outputs to external RAM.
9	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs
10	R/$\overline{W}$	**Read/Write:** output signal to external RAM
11	$\overline{MUTE}$	**Mute:** input from the microprocessor When mute is LOW, the data output DAAB (Pin 37) is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute, the data output is incremented to the first "good" value in 2 steps This input has an internal pull-up of 50kΩ (typ)
12 – 14	D1 – D3	**Data:** data inputs/outputs to external RAM
15	$\overline{CAS}$	**Column Address Select:** output signal to external RAM
16	D4	**Data:** data input/output to external RAM
17	MSC	**Motor Speed Control:** open-drain output which provides a pulse width modulated signal with a pulse rate of 88kHz to control the rate of data entry. The duty factor varies from 1 6% to 98.4% in 62 steps When a motor-start signal is detected via Pin 33 (SWAB/SSM) the duty factor is forced to 98.4% for 0 2 seconds followed by a normal calculated signal After a motor-stop signal is detected, the duty factor is forced to 1 6% for 0.2 seconds, followed by a continuous 50% duty factor
18	XTAL2	**Crystal Oscillator Output:** drive output to clock crystal (11 2896MHz typ.)
19	XTAL1	**Crystal Oscillator Input:** input from crystal oscillator or slave clock
20	V_{SS}	**Ground:** circuit ground potential
21	V_{BB}	**Back Bias Supply Voltage:** back bias output voltage (–2.5V ± 20%) The internal back bias generator can be decoupled at this pin
22	PD/OC	**Phase Detector Output/Oscillator Control Input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO
23	I_{REF}	**Current Reference:** external reference input to the phase detector This input is required to minimize the spread in the charge pump output of the phase detector An internal clamp prevents the voltage on this pin from rising above 3 5V
24	FB	**Feedback:** output from the input data slicer This output is a current source of 100μA (typ) which changes polarity when the level detector input at Pin 25 (HFI) rises above the threshold voltage of 2V (typical). When a data run length violation is detected (e g , during drop-out), or when HFD (Pin 26) is LOW, this output goes to high impedance state
25	HFI	**High-Frequency Input:** level detector input to the data slicer A differential signal of between 0 25 and 2 5V (peak-to-peak value) is required to drive the data slicer correctly When a T_{MAX} violation is detected or when HFD is LOW, this input is biased directly to its threshold voltage
26	HFD	**High-Frequency Detector:** when HIGH, this input signal enables the frequency and phase detector inputs, also the feedback output (FB) from the data slicer An internal voltage clamp of 3V (typical) requires the HFD input to be fed via a high impedance This input has an internal pull-up of 50kΩ (typical)
27	CEFM	**Clock Eight-to-Fourteen Modulation:** demodulator clock output 4 3218MHz (typcal)
28	$\overline{CRI}$	**Counter Reset Inhibit:** when LOW, this input signal allows the divide-by-588 master counter in the DEMOD timing to run free This input has an internal pull-up of 50kΩ (typical).
29	QDATA	**Q-Channel Data:** this subcoding output is parity checked and changes in response to the Q-channel clock input (see subcoding microprocessor handshaking protocol)
30	QRA	**Q-Channel Request Input/Acknowledge Output:** the output has an internal pull-up of nominally 10kΩ (See subcoding microprocessor handshaking protocol)
31	QCL	**Q-Channel Clock:** clock input generated by the microprocessor when it detects a QRA LOW signal.
32	DEEM	**De-emphasis:** signal derived from one bit of the parity-checked Q-channel and fed out via the debounce circuit.
33	SWAB/SSM	**Subcoding Word Clock Output and Start/Stop Motor Input:** open-drain output which is sensed during each HIGH period, and if externally forced LOW, a motor-stop condition will be decoded and fed to the motor control logic circuit
34	SDAB	**Subcoding Data:** a 10-bit burst of data, including flags and sync bits, is output serially to the B-chip once per frame clocked by burst clock output SCAB (see Figure 2)
35	SCAB	**Subcoding Clock:** a 10-bit burst clock 2 8224MHz (typ) output which is used to synchronize the subcoding data.
36	EFAB	**Error Flag:** output from interpolation and mute circuit to B-chip indicating unreliable data
37	DAAB	**Data:** this output which is fed to the B-chip or DAC, together with its clock (CLAB) and word select (WSAB) outputs, conforms to the I^2S bus format (see Figure 3)
38	CLAB	**Clock:** output to B-chip or DAC
39	WSAB	**Word Select:** output to B-chip or DAC
40	V_{DD}	**Power Supply:** positive supply voltage (+ 5V)

NOTE:
The pin sequence of the address outputs (A0 – A7) and the data outputs (D1 – D4) has been selected to be compatible with various dynamic 16K × 4-bit RAMs including the 4416

Decoder for Compact Disc Digital Audio System — SAA7210

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 to 5.5V; V_{SS} = 0V; T_A = −20°C to + 70°C, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pin 40)	4.5	5.0	5.5	V
I_{DD}	Supply current (Pin 40)		200	TBF	mA
Inputs					
D1 – D4, QCL					
V_{IL}	Input voltage LOW	−0.3		+0.8	V
V_{IH}	Input voltage HIGH	2.0		V_{DD} + 0.5	V
$\pm I_{LI}$	Input leakage current			10	μA
C_I	Input capacitance			7	pF
$\overline{\text{MUTE}}$, $\overline{\text{CRI}}$					
V_{IL}	Input voltage LOW	−0.3		+0.8	V
V_{IH}	Input voltage HIGH	2.0		V_{DD} + 0.5	V
$\lvert Z_I \rvert$	Internal pull-up impedance at V_I = 0V	TBF	50	TBF	kΩ
C_I	Input capacitance			7	pF
QRA, SWAB					
V_{IL}	Input voltage LOW	−0.3		+0.8	V
V_{IH}	Input voltage HIGH	2.0		V_{DD} + 0.5	V
C_I	Input capacitance			7	pF
$\lvert Z_I \rvert$	Internal pull-up impedance at V_I = 0V	5	10		kΩ
HFD					
V_{IL}	Input voltage LOW	−0.3		+0.8	V
V_{IH}	Input voltage HIGH	2.0		clamped	V
V_{CL}	Input clamping voltage at I_I = 100μA		3		V
$\pm I_S$	Input source current			100	μA
C_I	Input capacitance			7	pF
$\lvert Z_I \rvert$	Internal pull-up impedance at V_I = 0V		50		kΩ
Outputs					
A1 – A8, R/$\overline{\text{W}}$, D1 – D4, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, CEFM, QDATA, DEEM, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB					
V_{OL}	Output voltage LOW at $-I_{OL}$ = 1.6mA	0		0.4	V
V_{OH}	Output voltage HIGH at I_{OH} = 0.2mA	2.4		V_{DD}	V
C_L	Load capacitance			50	pF
MSC (open-drain)					
V_{OL}	Output voltage LOW at $-I_{OL}$ = 1mA	0		0.2	V
C_L	Load capacitance			50	pF
SWAB, QRA (open drain)					
V_{OL}	Output voltage LOW at $-I_{OL}$ = 1.6mA	0		0.4	V
C_L	Load capacitance			50	pF
R_L	Internal load resistance	5			kΩ

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 4.5 to 5.5V; V_{SS} = 0V; T_A = −20°C to + 70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Analog circuits					
Data slicer input HFI					
$V_{I(P-P)}$	AC input voltage range (peak-to-peak value)	0.25		2.5	V
	Input impedance				
$\|Z_I\|$	normal (HFD HIGH)	TBF		TBF	kΩ
$\|Z_I\|$	disabled (HFD LOW)	TBF		TBF	kΩ
C_I	Input capacitance			7	pF
Output FB					
I_O	Output current at V_{FB} = 2V	TBF	100	TBF	μA
Phase detector					
Output PD/OC					
$\|Z_O\|$	Output impedance		TBF		kΩ
α	Control range[1]	± 2.1			rad
G	Gain factor		TBF		mA/rad
Input I_{REF}					
I_{REF}	Input reference current		500	TBF	μA
Fine frequency detector					
Output PD/OC					
$\|Z_O\|$	Output impedance		2		kΩ
Coarse frequency detector					
Output PD/OC[2]					
$\|Z_O\|$	Output impedance		1		kΩ
Voltage-controlled oscillator					
Input PD/OC					
K_{OSC}	Oscillator constant		TBF		MHz/V
Crystal oscillator					
Input XTAL1/Output XTAL2					
G_M	Mutual conductance at 100kHz	1.5			ms
G_V	Small-signal voltage gain ($G_V = G_M \times R_O$)	3.5			V/V
C_I	Input capacitance			10	pF
C_{FB}	Feedback capacitance			5	pF
C_O	Output capacitance			10	pF
$\pm I_{LI}$	Input leakage current			10	μA
Slave clock mode					
V_{IL}	Input voltage LOW	−0.3		0.8	V
V_{IH}	Input voltage HIGH	2.4		V_{DD} + 0.5	V
t_R	Input rise time[3]			20	ns
t_F	Input fall time[3]			20	ns
t_{HIGH}	Input High time at 1.5V (relative to clock period)	45		55	%

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 4 5 to 5 5V, V_{SS} = 0V, T_A = −20°C to + 70°C, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing characteristics					
f_{XTAL}	Operating frequency (XTAL)	10 16	11.2896	12.42	MHz
f_{VCO1} f_{VCO2}	Operating frequency (VCO) coarse frequency detector inactive no input Pin 25 (HFI)	$f_{XTAL}/2$ 4	8.6436	f_{XTAL} 15	MHz MHz
Outputs (see Figures 6 and 7)					
CEFM[4]					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
t_{HIGH}	Output High time	50			ns
DAAB, CLAB, WSAB, EFAB[4] **(data to B-chip; I²S format)**					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
DAAB, WSAB, EFAB to CLAB					
t_{SU}, t_{DAT}	Data setup time	100			ns
CLAB to DAAB, WSAB, EFAB					
t_{HD}, t_{DAT}	Data hold time	100			ns
SDAB, SCAB, DEEM[4] **(subcoding outputs)**					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
SDAB to SCAB					
$t_{SU;}$ t_{SDAT}	Subcoding data setup time	100			ns
SCAB to SDAB					
$t_{HD;}$ t_{SDAT}	Subcoding data hold time	100			ns
SWAB[4]					
t_R	Output rise time			1	μs
t_F	Output fall time			100	ns
	Output duty factor		50		%

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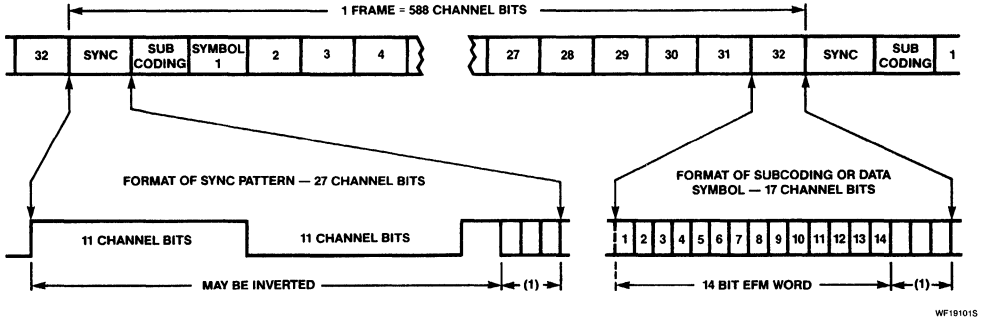
DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 4.5 to 5.5V; V_{SS} = 0V; T_A = −20°C to + 70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Q-channel I/O (see Figures 10 and 11)					
QRA, QCL, QDATA					
	Access time[5]				
$t_{ACC, N}$	normal mode	0		13.3 + n × 13.3	ms
$t_{ACC, F}$	refresh mode	13.3		n × 13.3	ms
t_{DACK}	QCL to QRA acknowledge delay			500	ns
$t_{HD, R}$	QCL to QRA request hold time	500			ns
$t_{CK; LOW}$	QCL clock input LOW time	500			ns
$t_{CK, HIGH}$	QCL clock input HIGH time	500			ns
t_{DD}	QCL to QDATA delay time			500	ns
$t_{HD; ACC}$	Data hold time before new frame is accessed	2.3			ms
t_{ACK}	Acknowledge time			10.8	ms

NOTES:

1. 1 rad = $\frac{180°}{(3.14)}$.
2. Coarse frequency detector output PD/OC active for VCO frequencies $> f_{XTAL}$ and $< \frac{f_{XTAL}}{2}$.
3. Reference levels = 0.5V and 2.5V.
4. Output rise and fall times measured with load capacitance (C_L) = 50pF.
5. Q-channel access times dependent on cyclic redundancy check (CRC).



NOTE:
(1) = merging and low frequency suppression bits

Figure 1. Data Input Signal

FUNCTIONAL DESCRIPTION

Demodulation

Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector, and a voltage-controlled oscillator (VCO) form an internal phase-locked loop (PLL) system. The voltage-controlled oscillator (VCO) runs at twice the input data rate (typically at 8.6436MHz), its frequency being dependent on the voltage at Pin 22 (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked, the frequency detector output stage is disabled via a lock indication signal. The VCO output is divided by two to provide the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at Pin 22 (PD/OC), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source connected to Pin 23 (I_{REF}).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs, the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input (Pin 28) Low to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal, together with a data strobe and two error flags, is also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output to B-chip

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC-checked Q-channel. The DEEM output (Pin 32) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at Pin 34. The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output to the B-chip consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q-channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst, this output delivers the debounced P-bit signal which can be read externally on the rising edge of SWAB at Pin 33 (see Figure 2).

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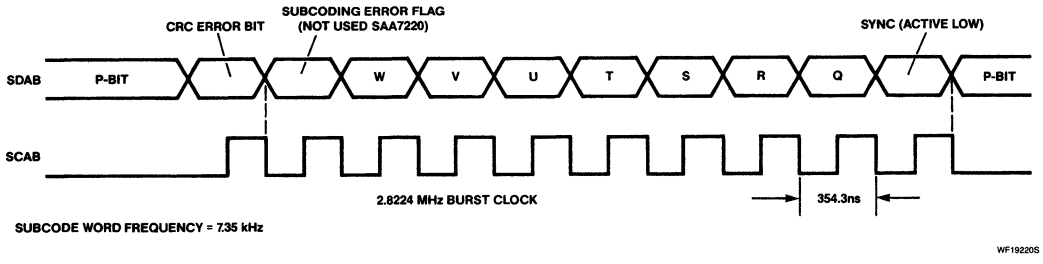


Figure 2. Typical Subcoding Waveform Outputs

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid

(2) Whether the new data symbol is the first symbol of a frame.

The pre-FIFO stores up to 4 symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency (e.g., pitch control).

Data Control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11.2MHz to determine the RAM access waveforms (the main clock for the system is 5.6MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1μs. The timing (see Figure 4) is based upon the specification for the dynamic 16k × 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address ($\overline{RAS}$ Pin 9) is set up first and then three 4-bit nibbles are accessed using sequential column addresses ($\overline{CAS}$ Pin 15). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The deinterleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag Processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus "good" data (flags = 00) and three levels of error can be indicated.

The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

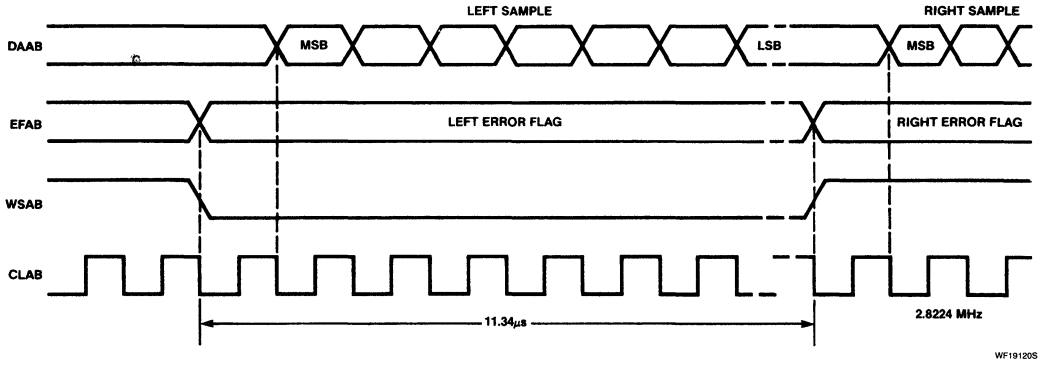


Figure 3. Typical Waveform Outputs to B-Chip or DAC

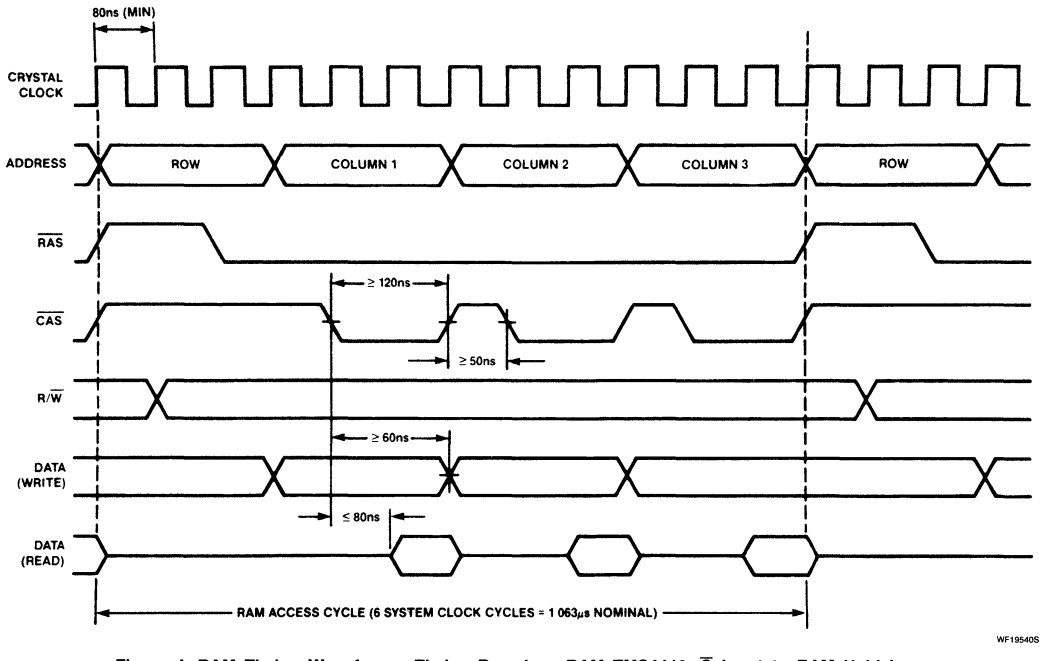


Figure 4. RAM Timing Waveforms: Timing Based on RAM TMS4416; $\overline{G}$ Input to RAM Held Low

7

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles, and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$2t + e = 4$

where:

e = the number of erasures (erroneous symbols whose position is known).

t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections: Syndrome formation and micro-coded correction processing.

Syndrome Formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded Correction Processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample-and-hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period, the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the B-chip where it receives additional and more efficient concealment.

Motor Speed Control (see Figure 5)

The motor speed control (MSC) output from Pin 17 is a pulse width modulated signal. The duty factor of the pulse width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88.2kHz.

The duty factor of MSC varies in 62 steps from 1.6% (FIFO full) to 98.4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98.4% for 0.2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected, the duty factor is forced to 1.6% for 0.2 seconds followed by a continuous 50% duty factor. A change in motor-start/-stop status occurring within the 0.2 second periods overrides the previous condition and resets the data control timer.

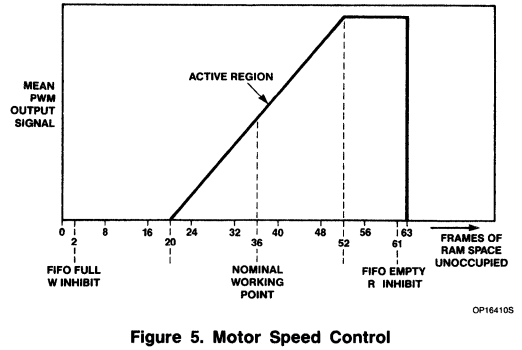
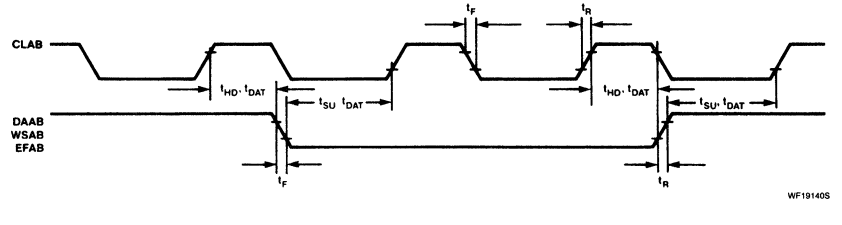
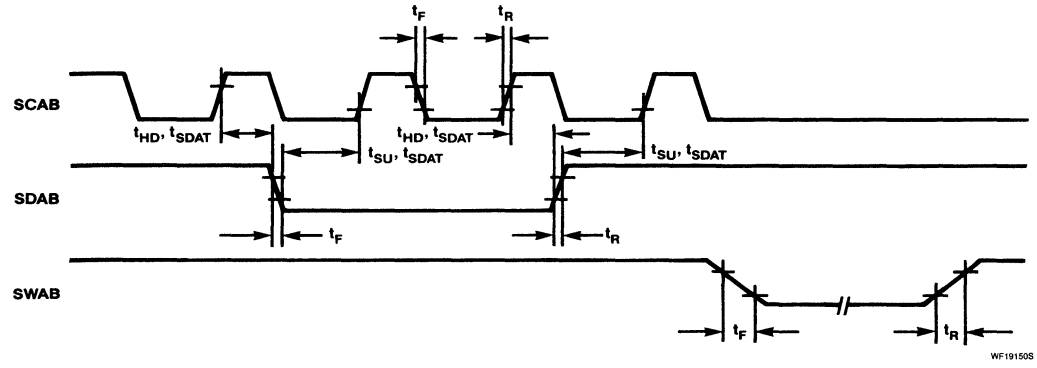


Figure 5. Motor Speed Control



NOTE:
Reference Levels = 0 8V and 2 0V

Figure 6. Typical Data Output Waveforms to B-Chip or DAC



NOTES:
1. Reference levels for SCAB and SDAB = 0.8V and 2.0V
2. Reference levels for SWAB = 0.8V and 4.0V

Figure 7. Typical Subcoding Data Output Waveforms

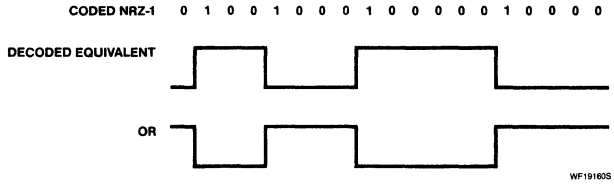


Figure 8. Non-Return to Zero (NRZ) Representation

Table 1. Codes Used to Define Subcoding Frame Sync

8-BIT NRZ DATA SYMBOL								14-BIT EQUIVALENT CODE WORD													
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
x	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
x	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

NOTE:
Where: X = don't care state.

APPLICATION INFORMATION

EFM Encoding System

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a DC free signal to the demodulator. In this modulation system, the data run length between transitions is ≥ 3 clock periods and ≤ 11 clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the DC content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Figure 8).

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{MAX}, T_{MIN}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

When a subcoding frame sync is detected, the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

Table 2. EFM Code Conversion

NO.	DNZ DATA SYMBOL D1 D8	EQUIVALENT CODE WORD C1 C14	NO.	DNZ DATA SYMBOL D1 D8	EQUIVALENT CODE WORD C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11 to 119			139 to 247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 0 1 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 0 1 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 0 1 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 0 1 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

Subcoding Microprocessor Handshaking Protocol (see Figures 9, 10, and 11)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7210.

The SAA7210 is continuously collecting Q-channel data, and when it detects that QRA is HIGH, it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7210 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal, it generates a clock signal (QCL) to shift the data out from the SAA7210 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowledge signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits), it pulls the QRA line LOW again. The SAA7210 now disables the QDATA output and resumes collecting new Q-channel data.

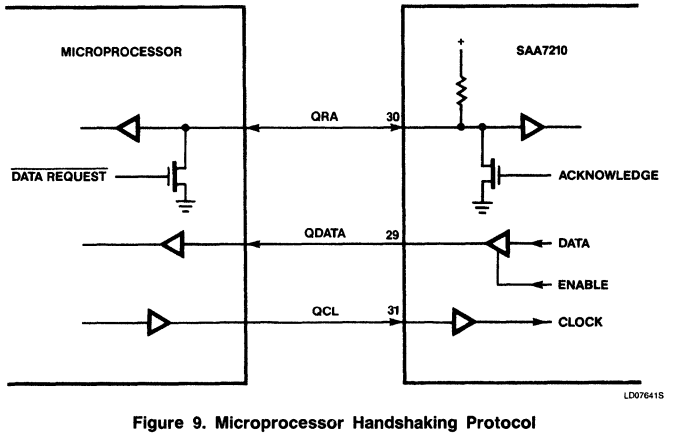


Figure 9. Microprocessor Handshaking Protocol

If the microprocessor does not generate a QCL signal within 10.8ms from the start of the acknowledge (QRA LOW), the SAA7210 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2.3ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13.33ms the SAA7210 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

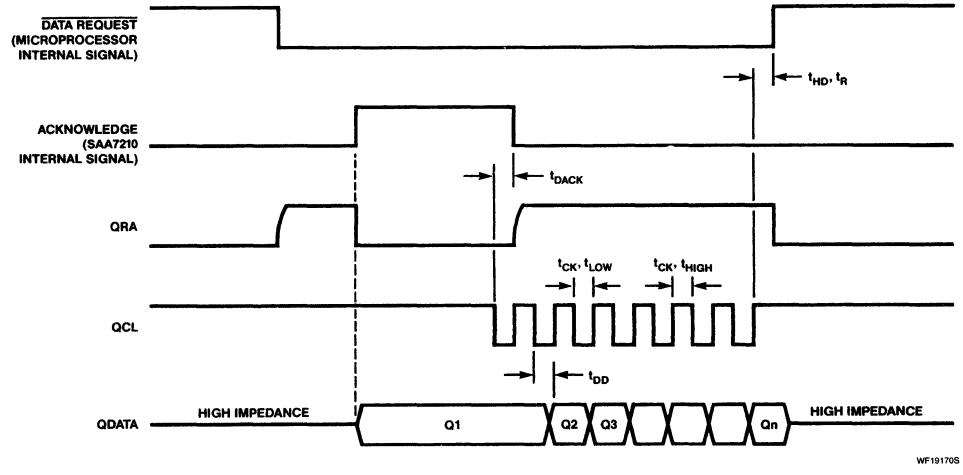


Figure 10. Q-Channel Timing Waveforms (Normal Mode)

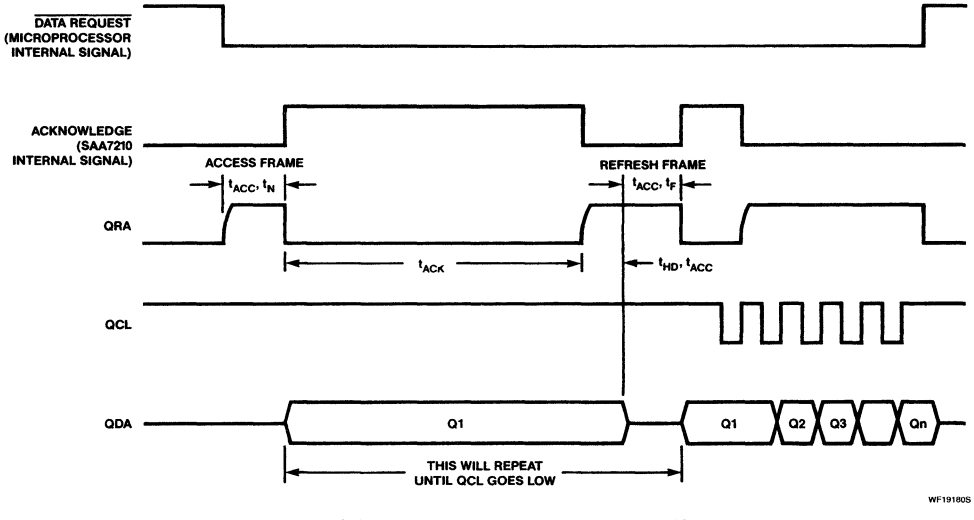


Figure 11. Q-Channel Timing Waveforms (Refresh Mode)

7

Signetics

SAA7220
Digital Filter for Compact Disc Digital Audio System

Product Specification

Linear Products

DESCRIPTION

The SAA7220 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. For descriptive purposes, the SAA7220 is referred to as the B-chip and the SAA7210 as the A-chip.

FEATURES

- **16-bit serial data input (two's complement)**
- **Interpolated data replaces erroneous data samples**
- **−12dB attenuation via the active Low attenuation input control (ATSB)**
- **Smoothed transitions before and after muting**
- **Two identical finite impulse response transversal filters each with a sampling rate of four times that of the normal digital audio data**
- **Digital audio output of 32-bit words transmitted in biphase-mark code**
- **I^2S data transfer between SAA7210 and 16-bit dual DAC (TDA1541)**

APPLICATIONS

- **Compact disc digital audio system**
- **Digital filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	−20°C to +70°C	SAA7220N

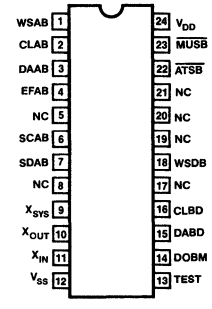
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 24)	−0.5 to +7.0	V
V_I	Maximum input voltage range	−0.5 to V_{DD} + 0.5	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
V_{ES}	Electrostatic handling[1]	−1000 to +1000	V

NOTES:
All outputs are short-circuit protected except the crystal oscillator output
1. Equivalent to discharging a 100pF capacitor through a 1.5Ω series resistor with a rise time of 15ns

PIN CONFIGURATION

N Package

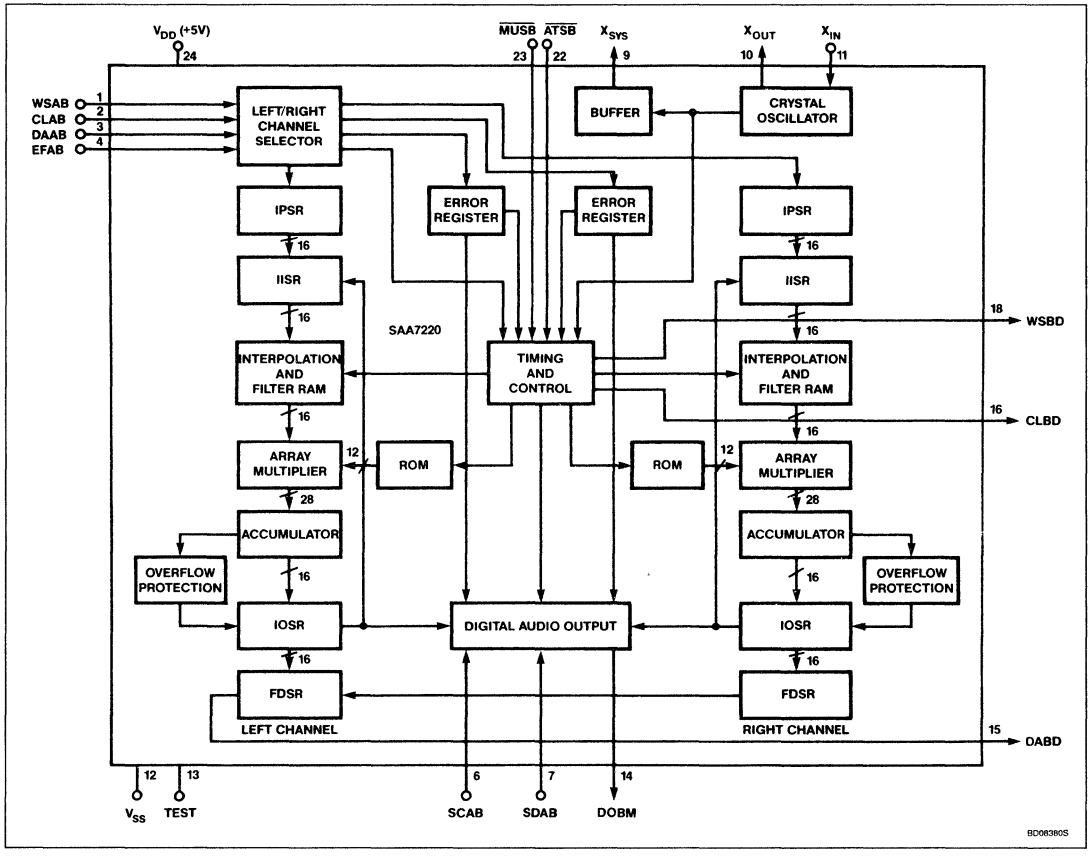


TOP VIEW

CD12270S

PIN NO.	SYMBOL	DESCRIPTION
1	WSAB	**Word select:** input from A-chip
2	CLAB	**Clock:** input from A-chip, has an internal pull-up
3	DAAB	**Data:** input from A-chip
4	EFAB	**Error flag:** Active-High input from A-chip indicating unreliable data. This input has an internal pull-down
5	NC	Not connected
6	SCAB	**Subcode clock:** a 10-bit burst clock 2.82 24MHz (typical) input which synchronizes the subcode data. This input has an internal pull-up
7	SDAB	**Subcode Data:** a 10-bit burst of data, including flags and sync bits serially input from the A-chip once per frame clocked by burst clock input SCAB (see Figure 6). This input has an internal pull-down
8	NC	Not connected
9	XSYS	**System clock output:** 11.2896MHz (typical) output to DAC and to A-chip as slave clock input
10	XOUT	**Crystal oscillator output:** drive output to clock crystal (11.2896MHz typical)
11	XIN	**Crystal oscillator input:** input from crystal oscillator or slave clock
12	V_{SS}	**Ground:** circuit ground potential
13	TEST	**Test input:** this input has an internal pull-down. In normal operation Pin 13 should be open circuit or connected to V_{SS}
14	DOBM	**Digital audio output:** this output contains digital audio samples which have received interpolation, attenuation, and muting, plus subcode data. Transmission is by biphase-mark code
15	DABD	**Data:** this output which is fed to the DAC, together with its clock (CLBD) and word select (WSBD) outputs, conforms to the I^2S format (see Figure 5)
16	CLBD	**Clock:** output to DAC
17	NC	Not connected
18	WSBD	**Word select:** output to DAC
19	NC	Not connected
20	NC	Not connected
21	NC	Not connected
22	$\overline{ATSB}$	**Attenuation:** when Active-Low, this control input provides −12dB attenuation. This input has an internal pull-up
23	$\overline{MUSB}$	**Mute:** Active-Low control input with internal pull-up
24	V_{DD}	**Power supply:** positive supply voltage (+5V)

BLOCK DIAGRAM



7

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 to 5.5V; V_{SS} = 0V; T_A = −20°C to +70°C, unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pin 24)	4 5	5 0	5.5	V
I_{DD}	Supply current (Pin 24)		180		mA
Inputs					
WSAB, DAAB					
V_{IL}	Input voltage Low	−0.3		+0.8	V
V_{IH}	Input voltage High	2 0		V_{DD} + 0.5	V
I_{LI}	Input leakage current	−10	0	+10	μA
C_I	Input capacitance			7	pF
EFAB, SDAB[1]					
V_{IL}	Input voltage Low	−0.3		+0.8	V
V_{IH}	Input voltage High	2.0		V_{DD} + 0.5	V
I_{LI} I_{LI}	Input leakage current at V_I = 0V at V_I = V_{DD}	−10		 +50	 μA μA
C_I	Input capacitance			7	pF
CLAB, SCAB, $\overline{\text{ATSB}}$, $\overline{\text{MUSB}}$[2]					
V_{IL}	Input voltage Low	−0.3		+0.8	V
V_{IH}	Input voltage High	2.0		V_{DD} + 0.5	V
I_{LI} I_{LI}	Input leakage current at V_I = 0V at V_I = V_{DD}	−30		 +10	 μA μA
C_I	Input capacitance			7	pF
Crystal oscillator (see Figure 7)					
Input XIN					
Output XOUT					
G_M	Mutual conductance at 100kHz	1.5			mA/V
A_V	Small-signal voltage gain ($A_V = G_M \times R_O$)	3.5			V/V
C_I	Input capacitance			10	pF
C_{FB}	Feedback capacitance			5	pF
C_O	Output capacitance			10	pF
I_{LI}	Input leakage current	−10	0	+10	μA
Slave clock mode					
$V_{I(P-P)}$	Input voltage[3] (peak-to-peak value)	3.0		V_{DD} + 0.5	V
V_{IL}	Input voltage Low[3]	0		1	V
V_{IH}	Input voltage High[3]	3.0		V_{DD} + 0.5	V
t_R	Input rise time[4]			20	ns
t_F	Input fall time[4]			20	ns
t_{HIGH}	Input High time at 2V (relative to clock period)	35		65	%

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 4.5 to 5.5V; V_{SS} = 0V; T_A = −20°C to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Outputs					
DABD, CLBD, WSBD					
V_{OL}	Output voltage Low at I_{OL} = 1.6mA	0		0.4	V
V_{OH}	Output voltage High at $-I_{OH}$ = 0.2mA	2.4		V_{DD}	V
C_L	Load capacitance			50	pF
XSYS[5]					
V_{OL}	Output voltage Low	0		0.4	V
V_{OH}	Output voltage High	2.4		V_{DD}	V
C_L	Load capacitance			50	pF
DOBM					
$V_{L(P-P)}$	Voltage across a 75Ω load via attenuator; see Figure 8 (peak-to-peak value)	0.4		0.6	V

NOTES:

1. Inputs EFAB and SDAB both have internal pull-downs.
2. Inputs CLAB, SCAB, $\overline{ATSB}$, and $\overline{MUSB}$ have internal pull-ups.
3. The minimum peak-to-peak voltage can be reduced to 2V if the output XSYS is not being used. Similarly V_{IH} can be reduced to 2.4V (min.). All other levels remain the same.
4. Reference levels = 10% and 90%.
5. The output current conditions are dependent on the drive conditions. When a crystal oscillator is being used, the output current capability is I_{OL} = +1.6mA; I_{OH} = −0.2mA. But if a slave input is being used, the output currents are reduced to I_{OL} = +0 2mA; I_{OH} = −0.2mA.
6. Reference levels = 0.8V and 2.0V.
7. The signal CLAB can run at either 2.8MHz (¼ system clock) or 1.4MHz (⅛ system clock) under typical conditions. It does not have a minimum or maximum frequency, but is limited to being ¼ or ⅛ of the system clock frequency.
8. Input setup and hold times measured with respect to clock input from A-chip (CLAB). Reference levels = 0.8V and 2.0V.
9. Input setup and hold times measured with respect to subcode burst clock input from A-chip (SCAB). Reference levels = 0.8V and 2.0V.
10. Output setup and hold times measured with respect to system clock output (XSYS).
11. Output setup and hold times measured with respect to clock output (CLBD).
12. Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level.

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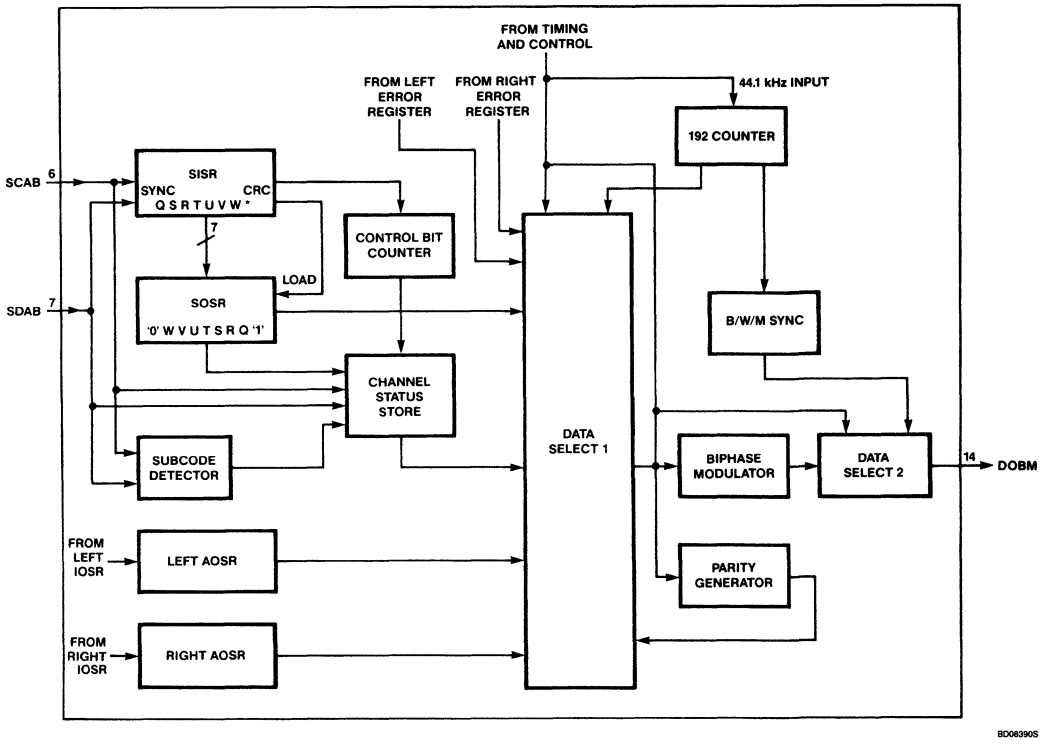

Where:

SISR = Subcode input shift register
SOSR = Subcode output shift register
IOSR = Intermediate output shift register
AOSR = Audio output shift register
* = Subcode word error flag

Figure 1. Digital Audio Output Block Diagram

FUNCTIONAL DESCRIPTION

General

The SAA7220 incorporates the following functions:

- Interpolation of data in error
- Attenuation
- Muting
- Finite impulse response transversal filtering with a four times increased sampling rate
- A digital audio output

Serial data formatted in two's complement (DAAB; Pin 3) is clocked in by its bit clock (CLAB; Pin 2) together with word select (WSAB; Pin 1) and error flag (EFAB; Pin 4). After resynchronization with the internal clocks, the data is separated into left and right channels and fed to two identical Input Shift Registers (IPSR). Internal timing and control loads the data into the interpolation RAM via the Intermediate Input Shift Register (IISR).

After interpolation, attenuation, and muting, the data is fed serially from the Intermediate Output Shift Register (IOSR) to the Audio Output Shift Register (AOSR) and to the IISR. From the IISR, it is loaded into the filter RAM.

After filtering, the data is passed to the Filter Data Shift Register (FDSR). From the FDSR it is transmitted serially to the data output (DABD; Pin 15) together with the appropriate word select (WSBD; Pin 18) and bit clock (CLBD; Pin 16), in accordance with the I^2S bus specification. Data is again formatted in two's complement. Outputs DABD, WSBD, and CLBD are strobed to maintain the correct timing relationship with the system clock output (XSYS) at Pin 9 (see Figure 10).

The subcode data (SDAB; Pin 7) and 10-bit burst clock (SCAB; Pin 6) are resynchronized to the internal clocks within the digital audio output block. SCAB clocks the data into the Subcode Input Shift Register (SISR; Figure 2). Data is transferred to the Subcode Output Shift Register (SOSR) on receipt of all of the 10-bit burst clocks. The subcode data is then mixed with the data from the AOSR and the error flag to provide the output DOBM at Pin 14. SISR is reset when no clocks are detected on the SCAB input.

Interpolation

When, for either left or right channel, unreliable samples are flagged between two correct samples, linear interpolation is used to replace the erroneous samples (up to a maximum of 8 consecutive errors).

When the error flag is set, the sample is replaced by a value calculated by the following formula:

$$S(n) = \frac{x}{x+1} \cdot S(n-1) + \frac{1}{x+1} \cdot S(n+x)$$

Where: $S(n)$ = new sample value
x = number of successive erroneous samples following $S(n-1)$
$S(n-1)$ = the preceding sample
$S(n+x)$ = the first following correct sample

The value of x is detected (1 to 8) to determine the coefficients for the multiplications. Eight coefficient pairs are stored in the ROM. If $x = 0$ or ≥ 9, then S(n) will remain unchanged.

Attenuation

Attenuation is controlled by the ATSB input at Pin 22. When the input is Active-Low, the sample is multiplied by a coefficient that provides −12dB attenuation. If the input is High, the multiplication factor is 1.

Mute

Mute is controlled by the MUSB input at Pin 23. When the input is Active-Low, the value of the samples is decreased smoothly to zero following a cosine curve. 32 coefficients are used to step down the value of the data, each one being used 31 times before stepping onto the next. When MUSB is released (Pin 23 High), the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order.

Filtering

The SAA7220 incorporates two identical finite impulse response transversal filters with the equivalent of 120 taps, one filter for each stereo channel. The corresponding 120 coefficients are structured as 4 sections of 30 coefficients.

(Each ROM contains only 60 filter coefficients, the same 60 being used a second time, but in the reverse order, to make a total of 120.)

Data is stored in a 480-bit RAM (30 words × 16 bits). The 30 words are sequentially addressed 4 times to generate the 4 output samples.

When a new word is moved from the interpolation RAM to the filter RAM, the oldest word is discarded and all other words moved one position with respect to the ROM coefficients. The data storage effectively forms a 30-sample wide moving window on the input data. The samples move within this window at 5.6448MHz, and the window moves one sample every 22.6μs.

An output word is formed by multiplying 30 samples from the filter RAM with 30 coefficients from the ROM, using a 16 × 12 array multiplier. The result is added in an accumulator. At the end of the 30 multiplications, the 16 MSBs are passed from the accumulator via the IOSR to the FDSR, and the accumulator is reset. Overflow protection is incorporated so that the output always limits cleanly in the event of accumulator overflow. Also, to simplify the design of the digital-to-analog converter, a DC offset of +5% is added to the accumulator.

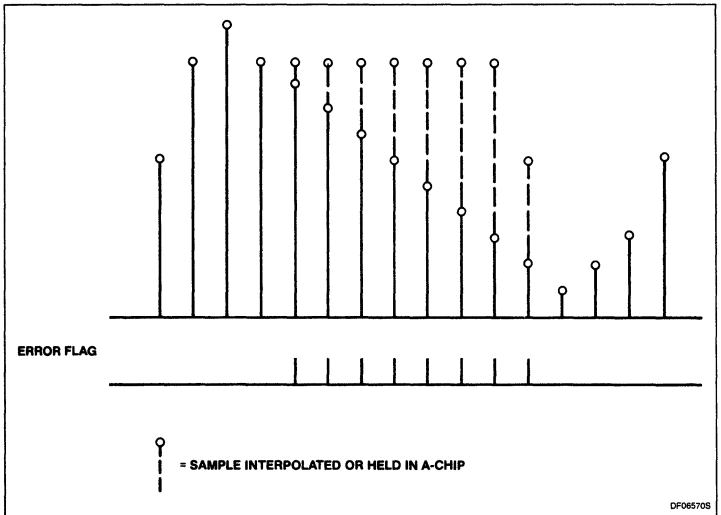

Figure 2. Example of an Eight-Sample Linear Interpolation

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Table 1. Composition of the 32-Bit Digital Audio Output Word

BIT NUMBER	DESCRIPTION	INFORMATION
1 to 4	Sync	
5 to 8	Auxiliary	Not used (always zero)
9 to 28	Audio sample	Bits 9 to 12 not used (always zero) Bits 13 (LSB) to 28 (MSB) two's complement
29	Audio valid	Copy of the error flag
30	User data	Used for subcode data
31	Channel status	Indication of control bits and category code
32	Parity bit	Even parity for all word bits excluding sync pattern

The filtered data is output in the I^2S format at a 5.6448MHz bit rate and a sample rate of 176kHz.

Digital Audio Output

The digital audio output (DOBM; Pin 14) consists of 32-bit words transmitted in bi-phase-mark code. That is, two transitions for a logic 1 and one transition for a logic 0. The 32-bit words are transmitted in blocks of 384 words. Table 1 shows the information contained in each word.

The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns (B, M, and W) indicate the following situations:

- Sync B; start of a block of 384 words, contains left sample (11101000)
- Sync M; word contains left sample, but is not a block start (11100010)
- Sync W; word contains right sample (11100100)

In the SAA7220, sync words are always preceded by 0. Left and right samples are transmitted alternately. Audio samples are available for digital audio output after interpolation, attenuation, and muting, but before filtering. Data held in the Subcode Output Shift Register (SOSR) is transmitted via the user data bit and is asynchronous with the block rate.

Channel Status

The channel status bit is the same for both left and right words. Therefore, a block of 384 words contains 192 channel status bits as shown in Table 2.

When there is no subcode, the channel status will switch over to the general format. 'No subcode' is identified by the subcode detector when SCAB is a continuous High or Low.

If a subcode clock is provided, but there is no subcode data (SDAB is a continuous High or Low), the control bits will be zero and the category code will be CD.

The SYNC bit and the cyclic redundancy check bit (CRC) in the subcode data from the A-chip to the B-chip have the format shown by Figure 3. Typical subcode data output waveforms are shown by Figure 6.

Table 2. Channel Status Bit Assignment

BIT NUMBER	DESCRIPTION	SUBCODE PROVIDED	NO SUBCODE PROVIDED
1 to 4	Control	Copy of Q channel	Bits 1 and 2 zero Bit 3 image of SCAB Bit 4 image of SDAB
5 to 8	Reserved	Always zero	Always zero
9 to 16	Category code	CD category	General category
		Bit 9 logic 1	All bits zero
17 to 192		Always zero	Always zero

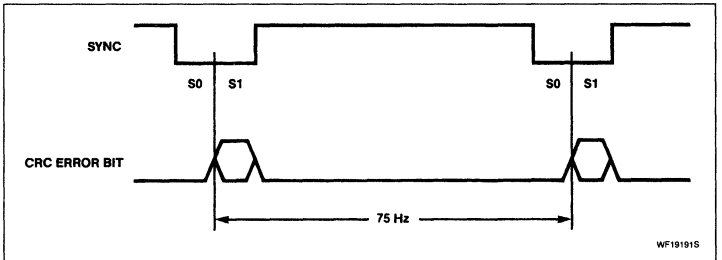

Figure 3. Subcode Data Format for SYNC and CRC Bits

SYNC is active Low and indicates the start of a subcode block, which contains 98 words including 2 sync words, S0 and S1. CRC is always Low except during SYNC S1 when:

- CRC = logic 1; previous Q block was true
- CRC = logic 0; previous Q block was false

Two 32-bit words are transmitted at the sample frequency of 44.1kHz ($2 \times 32 \times 44.1\text{kHz} = 2.8224\text{Mbits/s}$ data rate). An internal 5.6448MHz clock (XSYS/2) is used in the biphase modulator.

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{XTAL}	Operating frequency (XTAL)	10.16	11.2896	12.42	MHz
Inputs (see Figure 9)					
SCAB, CLAB[6]					
f_{SCAB}	SCAB clock frequency (burst clock)		2.8224		MHz
f_{CLAB} f_{CLAB}	CLAB clock frequency[7]		2.8224 1.4112		MHz MHz
t_{CKL}	Clock Low time	110			ns
t_{CKH}	Clock High time	110			ns
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns
DAAB, WSAB, EFAB[8]					
t_{SU}, t_{DAT}	Data setup time	40			ns
t_{HD}, t_{DAT}	Data hold time	0			ns
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns
SDAB[9]					
t_{SU}, t_{SDAT}	Subcode data setup time	40			ns
t_{HD}, t_{SDAT}	Subcode data hold time	0			ns
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns
Outputs (see Figure 10)					
WSBD[6, 10]					
t_{SU}, t_{WS}	Word select setup time	40			ns
t_{HD}, t_{WS}	Word select hold time	0			ns
WSBD[6]					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
DABD[6, 10]					
t_{SU}, t_{DATD}	Data setup time	40			ns
t_{HD}, t_{DATD}	Data hold time	0			ns
DABD[6]					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
CLBD[6, 10]					
t_{CK}	Clock period	161	177	197	ns
t_{CKL}	Clock Low time	65			ns
t_{CKH}	Clock High time	65			ns
t_{SU}, t_{CLD}	Clock setup time	40			ns
t_{HD}, t_{CLD}	Clock hold time	0			ns

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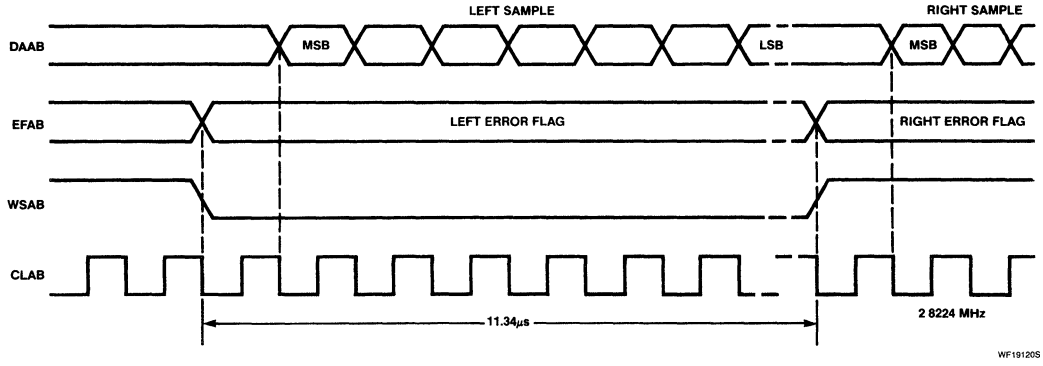
TIMING CHARACTERISTICS (Continued)

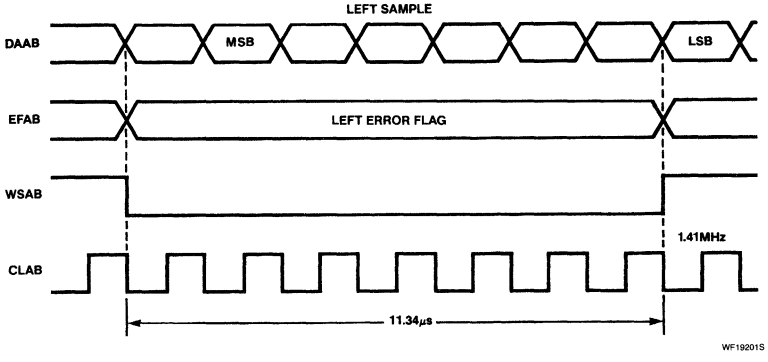
SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
CLBD[6]					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
DABD[6, 11]					
$t_{SU, DATBD}$	Data setup time	40			ns
$t_{HD, DATBD}$	Data hold time	60			ns
WSBD[6, 11]					
$t_{SU, DATWSD}$	Word select setup time	40			ns
$t_{HD, DATWSD}$	Word select hold time	60			ns
DOBM[12]					
t_R	Output rise time			20	ns
t_F	Output fall time			20	ns
	Data Bit 0				
$t_{HIGH(0)}$	pulse width High		354		ns
$t_{LOW(0)}$	pulse width Low		354		ns
	Data Bit 1				
$t_{HIGH(1)}$	pulse width High		177		ns
$t_{LOW(1)}$	pulse width Low		177		ns
XSYS					
t_R	Output rise time[6]			20	ns
t_F	Output fall time[6]			20	ns
t_{HIGH}	Output High time at 2V (relative to clock period)	35		65	%

NOTES:

1 Inputs EFAB and SDAB both have internal pull-downs.
2 Inputs CLAB, SCAB, $\overline{ATSB}$, and $\overline{MUSB}$ have internal pull-ups.
3 The minimum peak-to-peak voltage can be reduced to 2V if the output XSYS is not being used Similarly, V_{IH} can be reduced to 2.4V (min.). All other levels remain the same
4. Reference levels = 10% and 90%.
5. The output current conditions are dependent on the drive conditions When a crystal oscillator is being used, the output current capability is $I_{OL} = +1.6mA$; $I_{OH} = -0.2mA$. But if a slave input is being used, the output currents are reduced to $I_{OL} = +0.2mA$, $I_{OH} = -0.2mA$.
6 Reference levels = 0.8V and 2.0V.
7 The signal CLAB can run at either 2.8MHz (1/4 system clock) or 1.4MHz (1/8 system clock) under typical conditions It does not have a minimum or maximum frequency, but is limited to being 1/4 or 1/8 of the system clock frequency.
8. Input setup and hold times measured with respect to clock input from A-chip (CLAB) Reference levels = 0.8V and 2.0V
9 Input setup and hold times measured with respect to subcode burst clock input from A-chip (SCAB). Reference levels = 0.8V and 2.0V.
10 Output setup and hold times measured with respect to system clock output (XSYS).
11. Output setup and hold times measured with respect to clock output (CLBD)
12 Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level



a. Typical Sample Data Input Waveforms From A-Chip (2.8MHz)



b. Typical Sample Data Input Waveforms From A-Chip (1.4MHz)

Figure 4

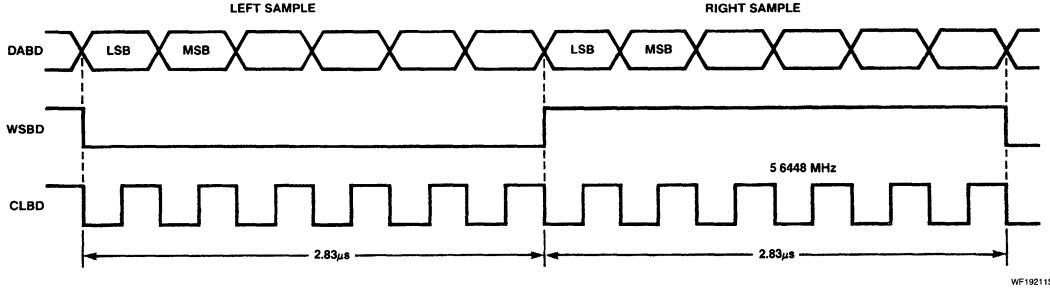
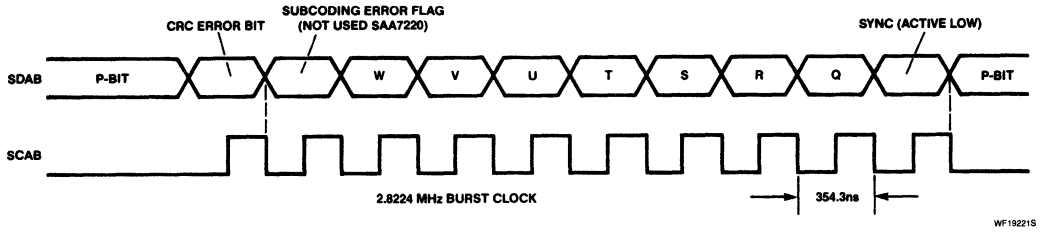


Figure 5. Typical Sample Data Output Waveforms to DAC



NOTE:
Subcode word frequency = 7.35kHZ

Figure 6. Typical Subcode Data Input Waveforms

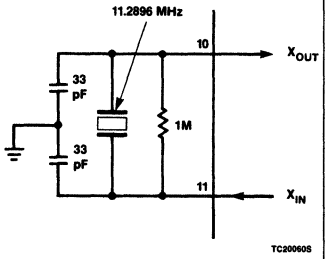


Figure 7. Crystal Oscillator Circuit

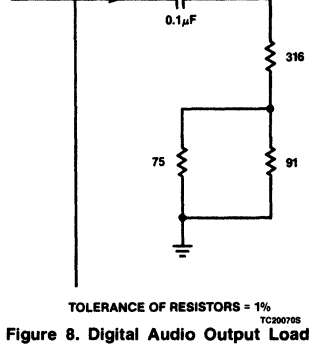
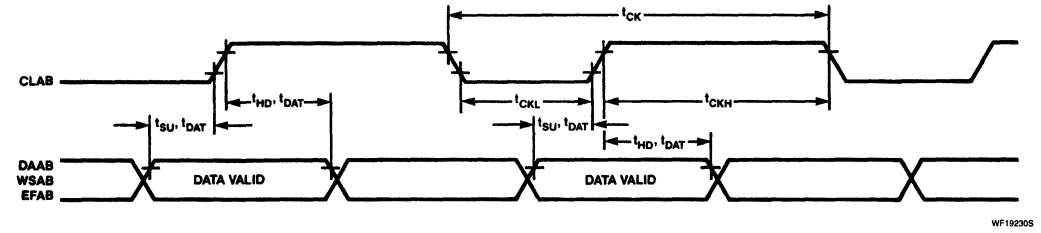


Figure 8. Digital Audio Output Load



NOTES:
1. Reference levels = 0.8V and 2.0V.
2. Applicable to subcode data input (t_{SU}, T_{SDAT} and t_{HD}, t_{SDAT}).

Figure 9. Data Input Timings

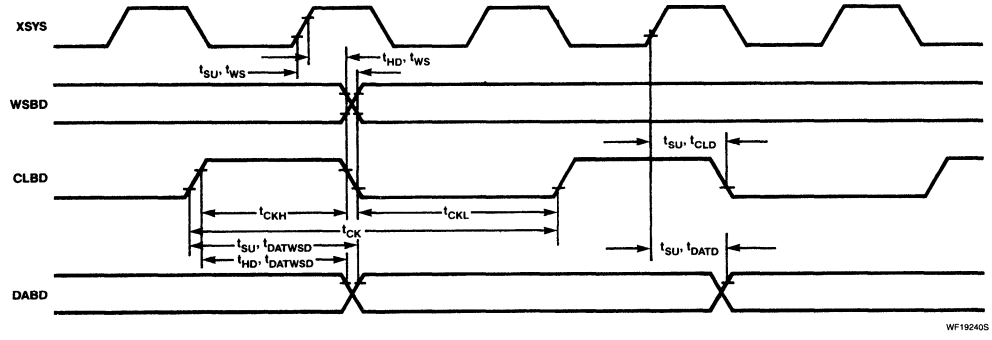


Figure 10. Data Output Timings; Reference Levels = 0.8V and 2.0V

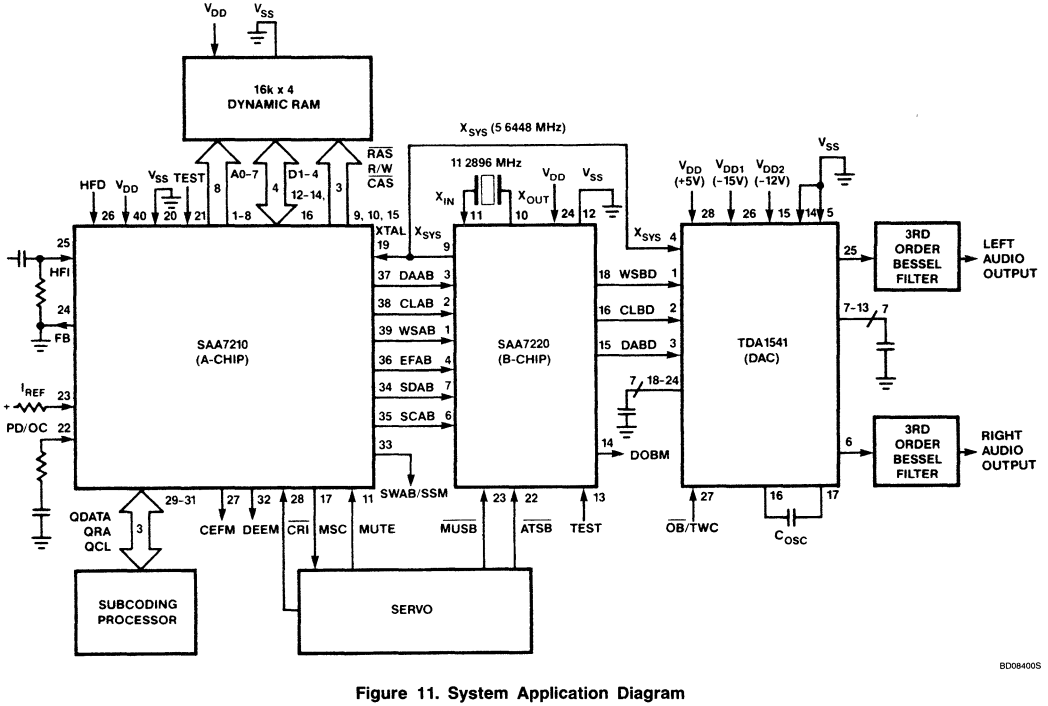


Figure 11. System Application Diagram

Signetics

TDA1541A
Dual 16-Bit Digital-to-Analog Converter

Product Specification

Linear Products

DESCRIPTION

The TDA1541A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed for use in hi-fi digital audio equipment such as compact disc players, digital tape, or cassette recorders.

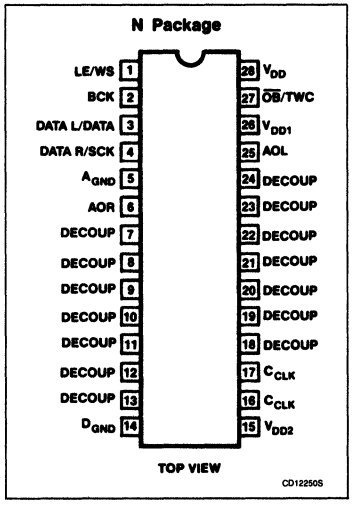
FEATURES

- **Selectable input format: offset binary or two's complement**
- **Internal timing and control circuit**
- **TTL-compatible digital inputs**
- **High maximum input bit rate and fast settling time**
- **6Mbits/s data rate**
- **Low linearity error (½ LSB typ.)**
- **Fast settling (1μs typ.)**

APPLICATIONS

- **Compact disc players**
- **Digital audio tape, and cassette recorders and players**
- **Waveform generation**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	−20°C to +70°C	TDA1541AN

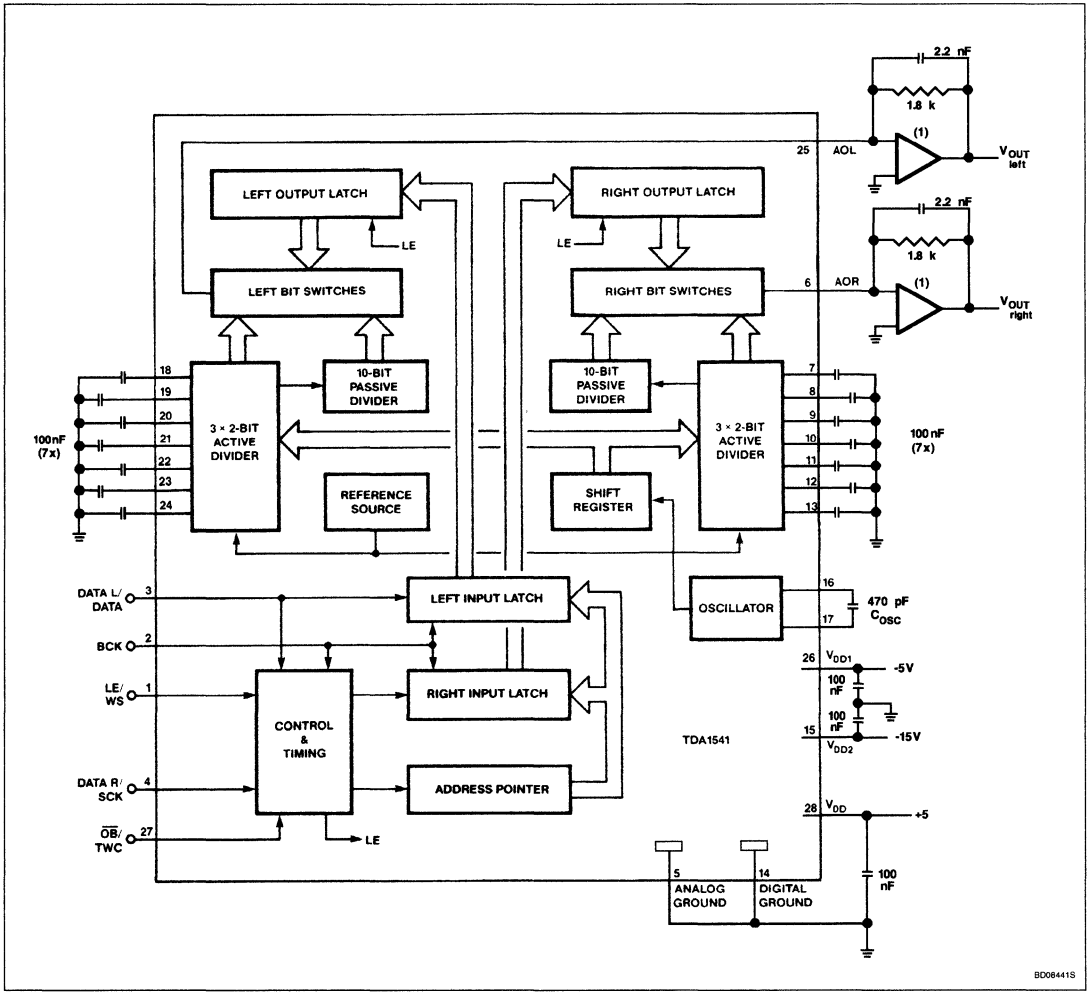
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges		
V_{DD}	Pin 28	+7	V
V_{DD1}	Pin 26	−7	V
V_{DD2}	Pin 15	−17	V
T_J	Junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C
V_{ES}	Electrostatic handling[1]	−1000 to +1000	V

NOTE:
1. Discharging a 250pF capacitor through a 1kΩ series resistor.

Dual 16-Bit Digital-to-Analog Converter TDA1541A

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{DD} = +5V$; $V_{DD1} = -5V$; $V_{DD2} = -15V$; $T_A = +25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
	Supply voltage ranges				
V_{DD}	Pin 28	4.5	5.0	5.5	V
$-V_{DD1}$	Pin 26	4.5	5.0	5.5	V
$-V_{DD2}$	Pin 15	14	15	16	V
	Supply currents				
I_{DD}	Pin 28		27	40	mA
$-I_{DD1}$	Pin 26		37	50	mA
$-I_{DD2}$	Pin 15		25	35	mA
	Resolution		16		bits
	Voltage difference between analog and digital ground	−0.3		+0.3	V
Inputs					
	Input current (Pins 1, 2, 3 and 4)				
I_{IL}	digital inputs LOW (< 0.8V)			0.4	mA
I_{IH}	digital inputs HIGH (> 2.0V)			20	μA
	Digital input current (Pin 27)				
$\|\overline{OB}/TWC\|$	+5V			1	μA
$\|\overline{OB}/TWC\|$	0V			20	μA
$\|\overline{OB}/TWC\|$	−5V			40	μA
	Input frequency				
f_{BCK}	at clock input (Pin 2)			0.4	MHz
f_{DAT}	at data inputs (Pin 3 and Pin 4)			0.4	MHz
f_{WS}	at word select input (Pin 1)			200	kHz
f_{LE}	at latch enable Pin 1			200	kHz
C_I	Input capacitance of digital inputs		12		pF
Oscillator					
f_{OSC}	Oscillator frequency $C_{OSC} = 470pF$	150	200	275	kHz
Analog outputs (AOL; AOR)					
V_{OC}	Output voltage compliance				mV
I_{FS}	Full-scale current	3.4	4.0	4.6	mA
$\pm I_{ZS}$	Zero-scale current		25	50	mA
TC_{FS}	Full-scale temperature coefficient $T_A = -20$ to $+85°C$		$\pm 200 \times 10^{-6}$		ppm/°C
	Linearity error integral				
E_L	at $T_A = 25°C$		0.5	1.0	LSB
E_L	at $T_A = -20$ to $+85°C$			1.0	LSB
	Linearity error differential				
E_{DL}	at $T_A = 25°C$		0.5	1.0	LSB
E_{DL}	at $T_A = -20$ to $+85°C$			1.0	LSB
THD	Total harmonic distortion		−100		dB
S/N	Signal-to-noise ratio + THD^2	90	95		dB
t_{CS}	Settling time to ±1 LSB		0.5		μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{DD} = +5V$; $V_{DD1} = -5V$; $V_{DD2} = -15V$; $T_A = +25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
α	Channel separation	80	98		dB
ΔI_{FS}	Unbalance between outputs		0.1	0.3	dB
t_D	Time delay between outputs			0.2	μs
	Supply voltage ripple rejection[3]				
SVRR	$V_{DD} = +5V$		-76		dB
SVRR	$V_{DD1} = -5V$		-84		dB
SVRR	$V_{DD2} = -15V$		-58		dB
	Signal-to-noise ratio				
S/N	at bipolar zero		110		dB
	at full scale	98	104		dB
Timing (see Figures 2, 3, and 4)					
t_R	Rise time			32	ns
t_F	Fall time			32	ns
t_{CY}	Bit clock cycle time	156			ns
t_{HB}	Bit clock High time	46			ns
t_{LB}	Bit clock Low time	46			ns
t_{FBRL}	Bit clock fall time to latch rise time	0			ns
t_{RBFL}	Bit clock rise time to latch fall time	0			ns
t_{SDB}	Data setup time to bit clock	32			ns
t_{HDB}	Data hold time to bit clock	0			ns
t_{SDS}	Data setup time to system clock	32			ns
t_{HWS}	Word select hold time to system clock	0			ns
t_{SWS}	Word select setup time to system clock	32			ns

NOTES:
1. To ensure no performance losses, permitted output voltage compliance is ±25mV maximum.
2. Signal-to-noise ratio + THD with 1kHz full-scale sine wave generated at a sampling rate of 176.4kHz.
3. $V_{RIPPLE} = 100mV$ and $f_{RIPPLE} = 100Hz$.

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit rate and fast settling time facilitates application in 4× oversampling systems (44.1kHz to 176.4kHz or 48kHz to 192kHz) with the associated simple analog filtering function (low-order, linear phase filter).

Input Data Selection

(See also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analog outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD}, the mode is the same, but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied by BCK and a latch-enable input (LE). With this mode selected, the data must be in offset binary.

The format of data input signals is shown in Figures 2, 3, and 4.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL-compatible.

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Table 1. Input Data Selection

$\overline{OB}$/TWC	MODE	PIN 1	PIN 2	PIN 3	PIN 4
−5V	Simultaneous	LE	BCK	DATA L	DATA R
0V	Time MUX OB	WS	BCK	DATA OB	NOT USED
+5V	Time MUX TWC	WS	BCK	DATA TWC	NOT USED

Where
LE = Latch enable
WS = Word select
BCK = Bit clock
DATA L = Data left
DATA R = Data right
DATA OB = Data offset binary
DATA TWC = Data two's complement
MUX OB = Multiplexed offset binary
MUX TWC = Multiplexed two's complement

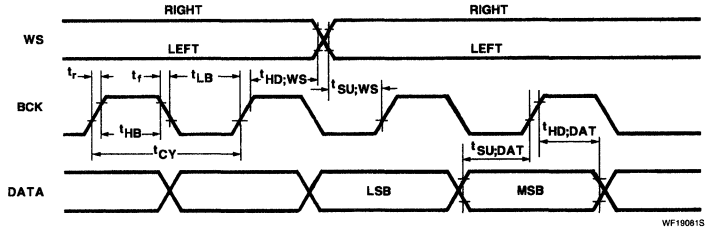


Figure 1. Format of Input Signals; Time Multiplexed at $f_{SCK} = f_{CK}$ (I^2S Format)

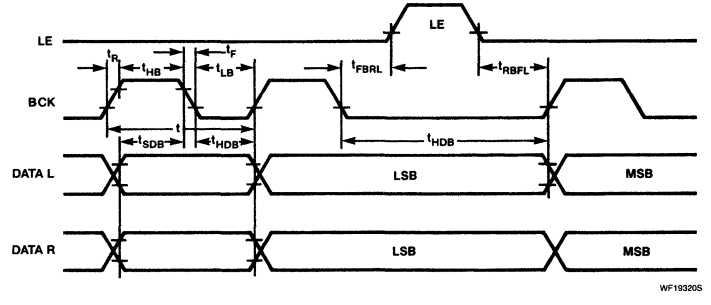


Figure 2. Format of Input Signals; Simultaneous Data

Signetics

Linear Products

Section 8
Speech/Audio Synthesis

INDEX

Signetics

OM8210
Speech Encoding And Editing System

Product Specification

Linear Products

DESCRIPTION

The OM8210 is a speech encoding and editing system and is comprised of a speech adaptor box and associated software. The software is available for use with either the Hewlett-Packard 9816S or IBM AT or XT. The OM8210 and the personal computer function together to produce speech coding for the PCF8200 Speech Synthesizer Chip. The system's human engineering is such that many of the available commands are single-key operations.

FEATURES

- **Input sampling of analog speech signal**
- **Speech analysis using formant algorithms**
- **Graphic representation of speech parameters**
- **On-screen parameter editing**
- **Conversion of parameters to PCF8200 synthesizer**
- **ROM programming**
- **Parameter storage on floppy disc**
- **Speech output via PCF8200 voice synthesizer**

HARDWARE DESCRIPTION

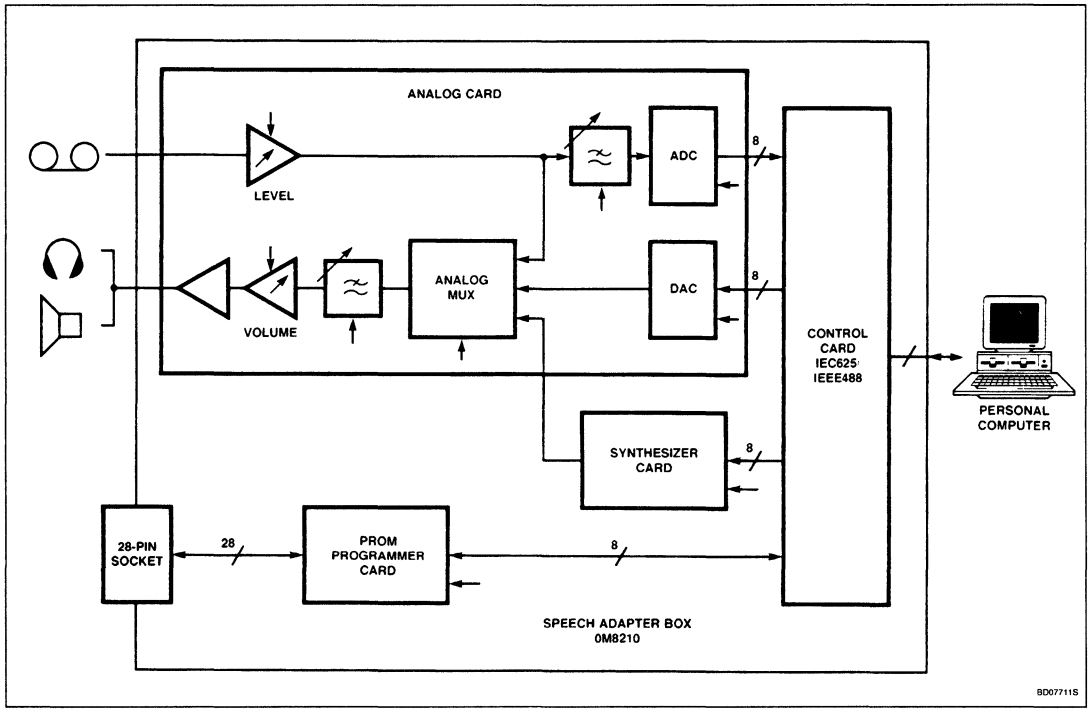
The hardware for the OM8210 is contained in a box allowing access to all interconnections (IEE488, interface loudspeaker, headphones, tape input, and ROM socket) from the front panel. There are four single Eurocards and a power supply forming the speed adaptor box. These cards are:

- Analog card
- Synthesizer card
- ROM card
- Control card

Analog Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analog-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analog converter (DAC) on the analog card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analog multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

BLOCK DIAGRAM



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The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

Synthesizer Card

This card accommodates the PCF8200 voice synthesizer chip and peripheral components to allow voice output.

PROM Programmer Card

This card allows four different types of PROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

Control Card

This card performs three functions:

- IEEE488 interface
- Control sequencer
- Clock generator

*The IEEE interface is a simple talker/listener implementation with an HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEEE interface and the chip enable signals for the rest of the system (the ADC, DAC, synthesizer and control circuits).

The filter sampling frequency is generated with a software-programmable PLL frequency synthesizer The speech sampling frequency is derived from the filter sampling frequency by frequency division Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available

Each mode and each command in the mode is selected by single-key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are as follows:

Sample Mode — Samples and digitizes the recorded speech. The amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible

Analysis Mode — Generates speech parameters from samples. The analysis selects the voiced/unvoiced sections, extracts the formants, amplitude, and the pitch, and quantizes the speech parameters.

Parameter Edit Mode — Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours or amplitudes, concatenate sounds and optimize data rate by editing the frame duration

Code Mode — Generates PCF8200 code and permits the arrangement of utterances in the optimum order of application. This mode also generates the address map at the head of the EPROM.

EPROM Mode — Used to program/read EPROM with data for the code memory. Also possible is a blank check, bit check and verification commands.

File Mode — Stores speech parameters or codes on disc. Can also assemble code speech segment from an already existing library.

Media Mode — For diskette initialization and making back-up copies.

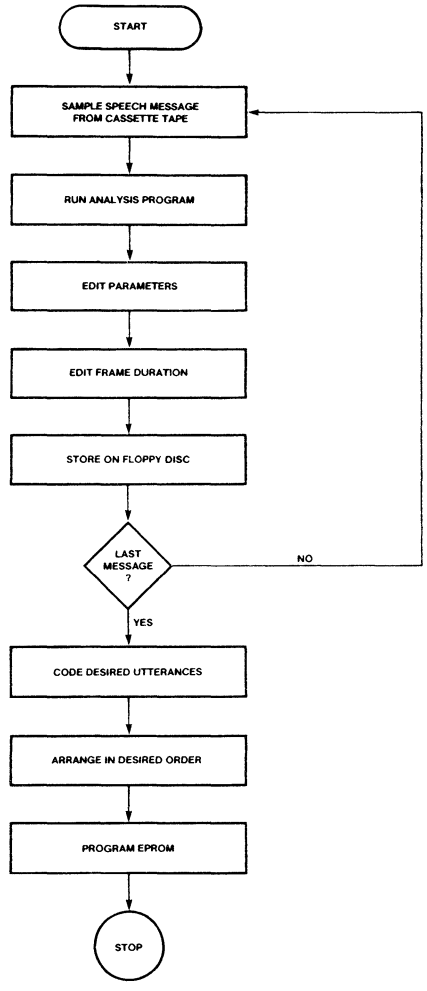
Option Mode — Allows the system configuration to be read or changed. The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

Computer System

The following equipment is required to make a complete editing system·

- HP9816S-630 or IBM AT or XT
- Dual floppy disc drive
- 512k bytes of memory

SPEECH CODING PROCESS FLOWCHART



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Signetics

PCF8200
CMOS Male/Female Speech Synthesizer

Objective Specification

Linear Products

DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.

FEATURES

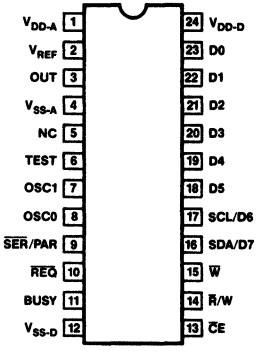
- **Male and female speech with good quality**
- **Speech-band from 0 to 5kHz**
- **Bit rate between 455 bits/second and 4545 bits/second**
- **Programmable frame duration**
- **Programmable speaking speed**
- **CMOS technology**
- **Operating temperature range −40 to +85°C**
- **Single 5V supply with low power consumption and power-down stand-by mode**
- **Interfaces easily with most popular microcomputers and microprocessors through 8-bit parallel bus or I^2C bus**
- **Software readable status word (parallel bus or I^2C bus)**
- **BUSY-signal and REQN-signal hardware readable**
- **Internal low-pass filter and 11-bit D/A converter**

APPLICATIONS

- **Telecommunications**
- **Video games**
- **Aids for the handicapped**
- **Industrial control equipment**
- **Automotive**
- **Irrigation systems**

PIN CONFIGURATION

N Package



TOP VIEW

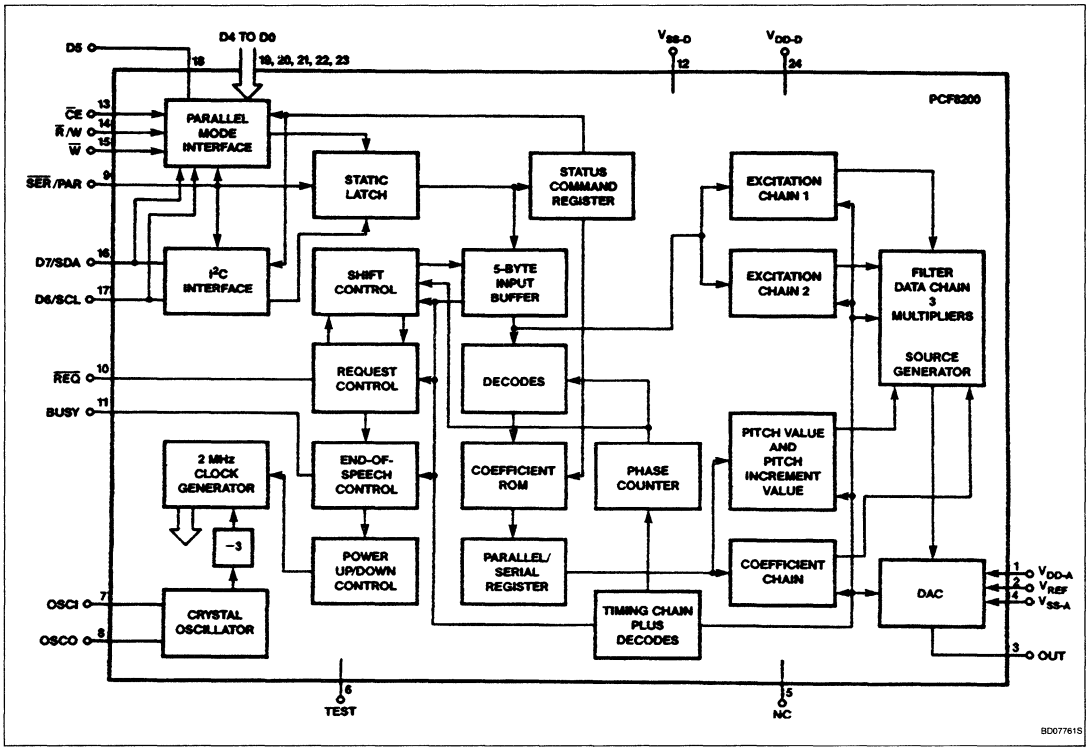
CD11511S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{DD-A}	Positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	Speech output
4	V_{SS-A}	Negative supply voltage for DAC stage
5	NC	Not connected
6	TEST	For normal operation this pin must be grounded (V_{SS})
7	OSCI	Oscillator input
8	OSCO	Oscillator output
9	$\overline{SER}$/PAR	For parallel data bus operation, this pin is hard-wired to V_{DD}, or to V_{SS}, to enable the I^2C bus
10	$\overline{REQ}$	Status bit indicating request for data
11	BUSY	Status indicating synthesizer busy
12	V_{SS-D}	Negative supply voltage for digital circuits
13	$\overline{CE}$	Chip-enable input
14	R/$\overline{W}$	Read/write control input
15	$\overline{W}$	Write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	Parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	Positive supply voltage for digital circuits

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−40°C to +85°C	PCF8200PN

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage[1]	−0 3 to 7 5	V
V_I	Input voltage[1]	−0.3 to 7.5	V
V_O	Output voltage[1]	−0 3 to 7 5	V
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−55 to +125	°C

NOTE:
1 Any pin with respect to V_{SS}

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DC AND AC ELECTRICAL CHARACTERISTICS

$T_A = -45°C$ to $+85°C$; supply voltage (V_{DD} to V_{SS}) = 4.5V to 5.5V with respect to V_{SS}, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage	4.5	5.0	5.5	V
I_{DD}	Supply current		10		mA
$I_{DD(SB)}$	Standby current		200		μA
Inputs $\overline{CE}$, R/$\overline{W}$, $\overline{W}$, OSCI					
V_{IH}	Input voltage High	2.0		V_{DD}	V
V_{IL}	Input voltage Low	0		0.8	V
I_{IR}	Input leakage current V_{IN} = 0 to 5.5V	−10		10	μA
t_{RF}	Rise and fall times[1]			50	ns
C_I	Input capacitance			7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
V_{IH}	Input voltage High	2.0		V_{DD}	V
V_{IL}	Input voltage Low	0		0.8	V
I_{IR}	Input leakage current (V_{IN} = 0 to 5.5V, output off)	−10		10	μA
C_I	Input capacitance			7	pF
Output Characteristics (D5 to D7 only)					
V_{OH}	Output voltage High (I_{OH} = −100μA)	3.5		V_{DD}	V
V_{OL}	Output voltage Low (I_{OL} = 3.2mA)	0		0.4	V
C_L	Load capacitance			80	pF
t_{RF}	Rise and fall times[2]			50	ns
SERIAL MODE					
Input Characteristics (SDA and SDL)					
V_{IH}	Input voltage High	3.0		V_{DD}	V
V_{IL}	Input voltage Low	0		1.5	V
I_{IR}	Input leakage current (V_{IN} = 0 to 5.5V, output off)	−10		10	μA
C_I	Input capacitance			10	pF
Output Characteristics (SDA only, open-drain)					
V_{OL}	Output voltage Low (I_{OL} = 3mA)	0		0.4	V
OSCILLATOR					
f_{XTAL}	Crystal frequency		6	6.1	MHz
V_{REF}					
V_{REF}	Reference voltage	1.9		$\frac{V_{DD} - 1.5}{1.25}$	V
I_{IR}	Input leakage current		5		μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

$T_A = -45°C$ to $+85°C$, supply voltage (V_{DD} to V_{SS}) = 4.5V to 5.5V with respect to V_{SS}, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Outputs $\overline{REQ}$, BUSY					
V_{OH}	Output voltage High ($I_{OH} = 100\mu A$)	3 5		V_{DD}	V
V_{OL}	Output voltage Low ($I_{QL} = 3.2mA$)	0		0 4	V
C_L	Load capacitance			80	pF
t_{RF}	Rise and fall times[2]			50	ns
OUT					
V_{OUT}	Output voltage	$0.66 \times V_{REF}$		$1\ 34 \times V_{REF}$	V
	Minimum external load	600			Ω
Timing characteristics[3]					
t_{WR}	Write enable	200			ns
t_{DS}	Data setup for write	150			ns
t_{DH}	Data hold for write	30			ns
t_{RD}	Read enable	200			ns
t_{DD}	Data delay for read[1]			150	ns
t_{DF}	Data floating for read[1]			150	ns
t_{CS}	Control setup	0			ns
t_{CH}	Control hold	0			ns
t_{RN}	REQ new (new byte of the same speech frame)		3		μs
t_{RV}	REQ Valid	0			ns
t_{RH}	REQ Hold		250	TBD	ns

NOTES:
1 Levels greater than 2V for a '1' or less than 0 8V for a '0' are reached with a load of one TTL input and 50pF
2 Rise and fall times between 0 6V and 2 2V levels
3 Timing reference level is 1 5V, supply 5V ± 10%, temperature range of −40°C to 85°C

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CMOS Male/Female Speech Synthesizer — PCF8200

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly; therefore, the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8.8, 10.4, 12.8 or 17.6 milliseconds with the speed option, speaking speed, in the command register.

The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard frame duration.

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation. A block diagram of the formant synthesizer is shown in Figure 1.

The filter output is upsampled to 80kHz and filtered with a digital low-pass filter. Before the signal is digital to analog converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

Table 1. Frame Duration as a Function of Speed-Option (FS1, FS0) and Frame-Duration (FD1, FD0).

	10	01	00	11	FS1, FS0
00	8.8	10.4	12.8	17.6	ms
01	17.6	20.8	25.6	35.2	ms
10	26.4	31.2	38.4	52.8	ms
11	44.0	52.0	64.0	88.0	ms
FD1, FD0					

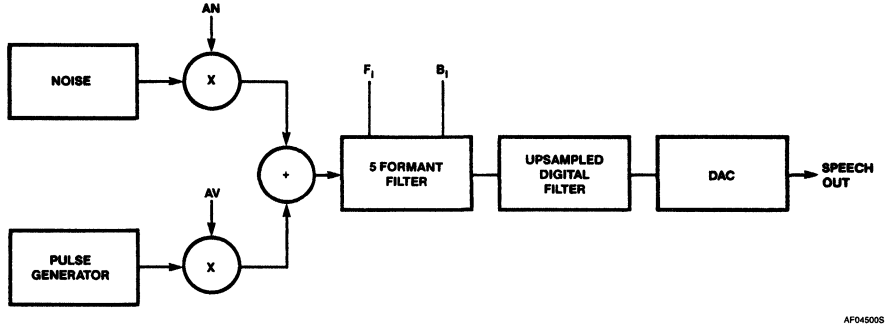


Figure 1. Block Diagram of Formant Synthesizer

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC Amplitude Factor

The DAC amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

Start Pitch

The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one-byte start value for the on-chip pitch-period generator.

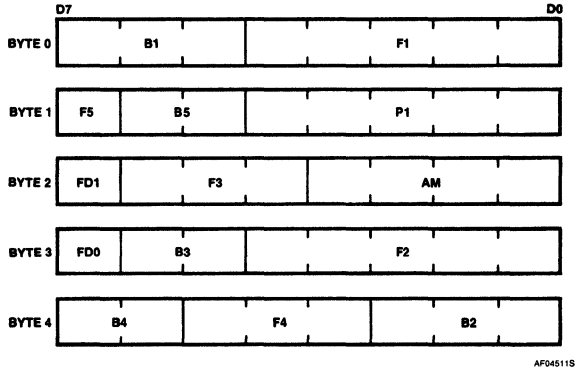
The frame data is a five-byte block which contains the filter and source information. The frame data bits are organized as shown in Figure 2.

Table 2. DAC Amplitude Factor

BYTE	FACTOR	dB
01110000	3.5	10.88
10110000	3.25	10.24
00110000	3.0	9.54
11010000	2.75	8.97
01010000	2.5	7.96
10010000	2.25	7.04
00010000	2.0	6.02
11100000	1.75	4.86
01100000	1.5	3.52
10100000	1.25	1.94
00100000	1.0	0.00
11000000	0.75	−2.50
01000000	0.5	−6.02
10000000	0.25	−12.04
00000000	0.0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Frame Data

Pitch increment/decrement value	5 bits
Amplitude	4 bits
Frame duration	2 bits
Frequency of 1st formant	5 bits
Frequency of 2nd formant	5 bits
Frequency of 3rd formant	3 bits
Frequency of 4th formant	3 bits
Frequency of 5th formant	1 bit
Bandwidth of 1st formant	3 bits
Bandwidth of 2nd formant	3 bits
Bandwidth of 3rd formant	2 bits
Bandwidth of 4th formant	2 bits
Bandwidth of 5th formant	2 bits
	40 bits = 5 bytes



NOTE:
It is not allowed to set byte 0 to the hexidecimal value E0.

Figure 2. Format of Frame-Data

8

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Figure 3

FS0, FS1 Speed Option

FS1	FS0	SPEECH SPEED	STANDARD FRAME DURATION
0	0	100%	12 8ms
0	1	123%	10.4ms
1	0	145%	8.8ms
1	1	73%	17 6ms

$\overline{M}$/F, Male/Female Option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop, repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP·

1. $\overline{REQ}$ = 1, STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (E0) This is shown in Figure 4

$\overline{REQ}$ = 1 No data required
= 0 Synthesizer requesting new data

BUSY = 1 Busy (an utterance is pronounced)
= 0 Idle, REQN will set to 1; (the synthesizer is in STOP or BADSTOP mode)

STOP The STOP bit is the same as the stop bit written to the synthesizer during a command write.
STOP = 1, BUSY = 0 (stopped by the user).
STOP = 0, BUSY = 0 (BADSTOP because the data was not sent in time).

After initial power-up the status/command register is set to the following status·

FS0, FS1 = 0 Standard-frame duration of 12.8ms

$\overline{M}$/F = 0 Male quantization table

STOP = 1

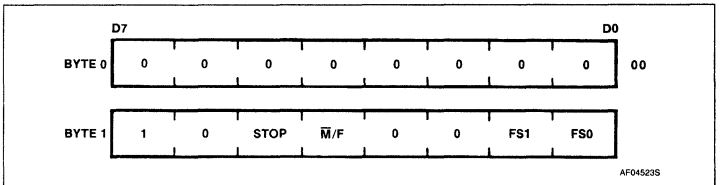


Figure 3. Control Write: First Byte Fixed, Second Byte Control

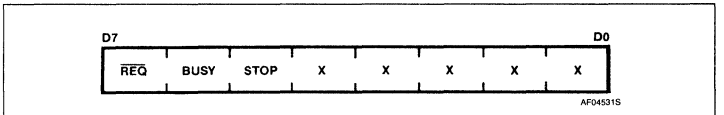


Figure 4. Status Read

BUSY = 0 Idle

$\overline{REQ}$ = 1 No data required

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0, or when $\overline{REQ}$ = 1 and BUSY = 0. Figure 5 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up

The I^2C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs, the byte must be provided within the duration of a half standard frame. If the byte is not provided in time, a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1' Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I^2C ADDRESS

On chip there is an I^2C slave receiver/transmitter with the address

7 6 5 4 3 2 1 0

0 0 1 0 0 0 0 R/W

POWER-UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR mode: The input latches are active so they can receive the first byte

SER mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer, a parallel write sequence (Figure 7) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W}$ = 0 and $\overline{R}$/W = 1.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE}$ = 0, $\overline{R}$/W = 1, $\overline{W}$ = 0).

POWER-DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down In the power-down mode the status/command register will be retained.

In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

$\overline{SER}$/PAR

$\overline{SER}$/PAR is hard-wired to V_{DD} or V_{SS}.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

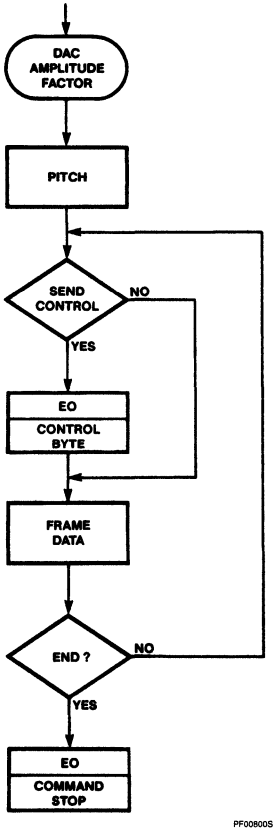
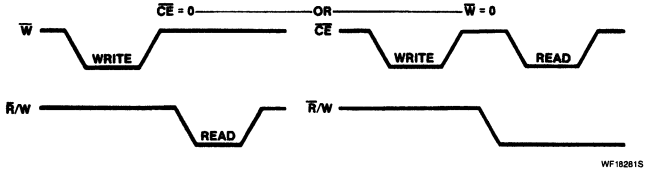


Figure 5. Interface Protocol

Timing Diagrams

The control signals CE, R/W and W have been specified to enable easy interface to most microprocessors and microcomputers. For instance, with connection to an MAB8048 microcomputer, the R/W and W inputs can be used as the RD and WR strobe inputs.

TYPICAL CONNECTION OF CONTROL SIGNALS



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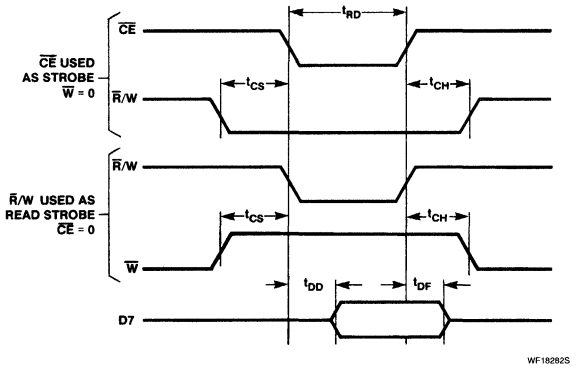

Figure 6. Read Timing

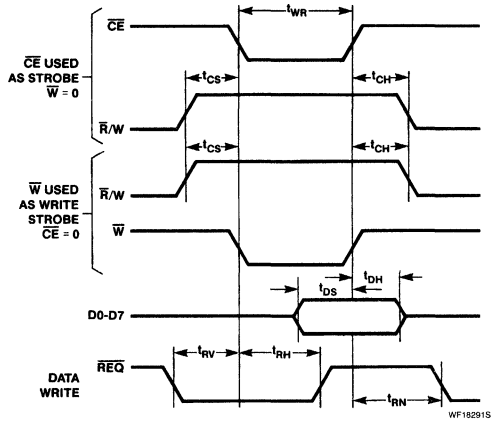

Figure 7. Write Timing

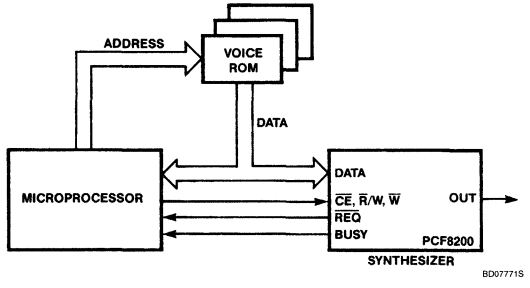

Figure 8. Typical Application Configuration with Parallel Interface

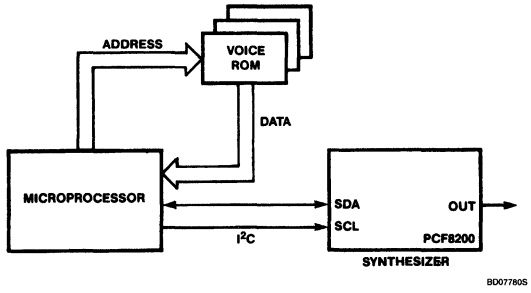

Figure 9. Typical Application Configuration with Series Interface

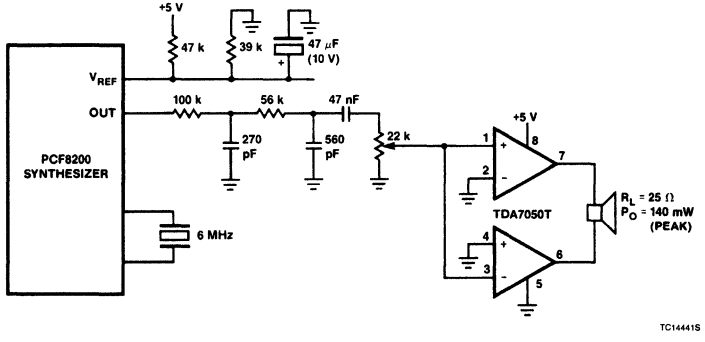

Figure 10. An Example of an Output Configuration

Figure 11. Oscillator Clock Configurations

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Signetics

Linear Products

SAA1099

Stereo Sound Generator for Sound Effects and Music Synthesis

Product Specification

DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

FEATURES

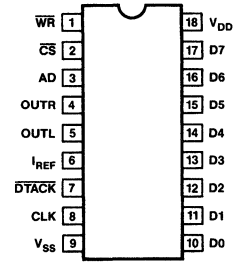
- **Six frequency generators — eight octaves per generator; 256 tones per octave**
- **Two noise generators**
- **Six noise/frequency mixers**
- **Twelve amplitude controllers**
- **Two envelope controllers**
- **Two 6-channel mixers/current sink analog output stages**
- **TTL input compatible**
- **Readily interfaces to 8-bit microcontroller**
- **Minimal peripheral components**
- **Simple output filtering**

APPLICATIONS

- **Consumer games systems**
- **Home computers**
- **Electronic organs**
- **Arcade games**
- **Toys**
- **Chimes/alarm clocks**

PIN CONFIGURATION

N Package



TOP VIEW

CD11500S

PIN NO.	SYMBOL	DESCRIPTION
1	$\overline{WR}$	**Write Enable:** Active-LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers
2	$\overline{CS}$	**Chip Select:** Active-LOW input to identify valid $\overline{WR}$ inputs to the chip This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers
3	A0	**Control/Address select:** input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1)
4	OUTR	**Right channel output:** a 7-level current sink analog output for the 'right' component This pin requires an external load resistor
5	OUTL	**Left channel output:** a 7-level current sink analog output for the 'left' component This pin requires an external load resistor
6	I_{REF}	**Reference current supply:** used to bias the current sink outputs
7	$\overline{DTACK}$	**Data Transfer Acknowledge:** open-drain output, Active-LOW to acknowledge successful data transfer On completion of the cycle $\overline{DTACK}$ is set to inactive
8	CLK	**Clock:** input for an externally-generated clock at a nominal frequency of 8MHz
9	V_{SS}	**Ground:** 0V
10 – 17	D0 – D7	**Data:** Data bus input
18	V_{DD}	**Power supply:** +5V typical

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102CS)	0 to +70°C	SAA1099PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage (Pin 18)	−0 3 to +7.5	V
V_I V_I	Maximum input voltage at V_{DD} = 4.5 to 5.5V	−0.3 to +7 5 −0.5 to 7.5	V V
I_O	Maximum output current	10	mA
P_{TOT}	Total power dissipation	450	mW
T_{STG}	Storage temperature range	−65 to +125	°C
T_A	Operating ambient temperature range	0 to +70	°C
V_{ES}	Electrostatic handling[1]	−1000 to +1000	V

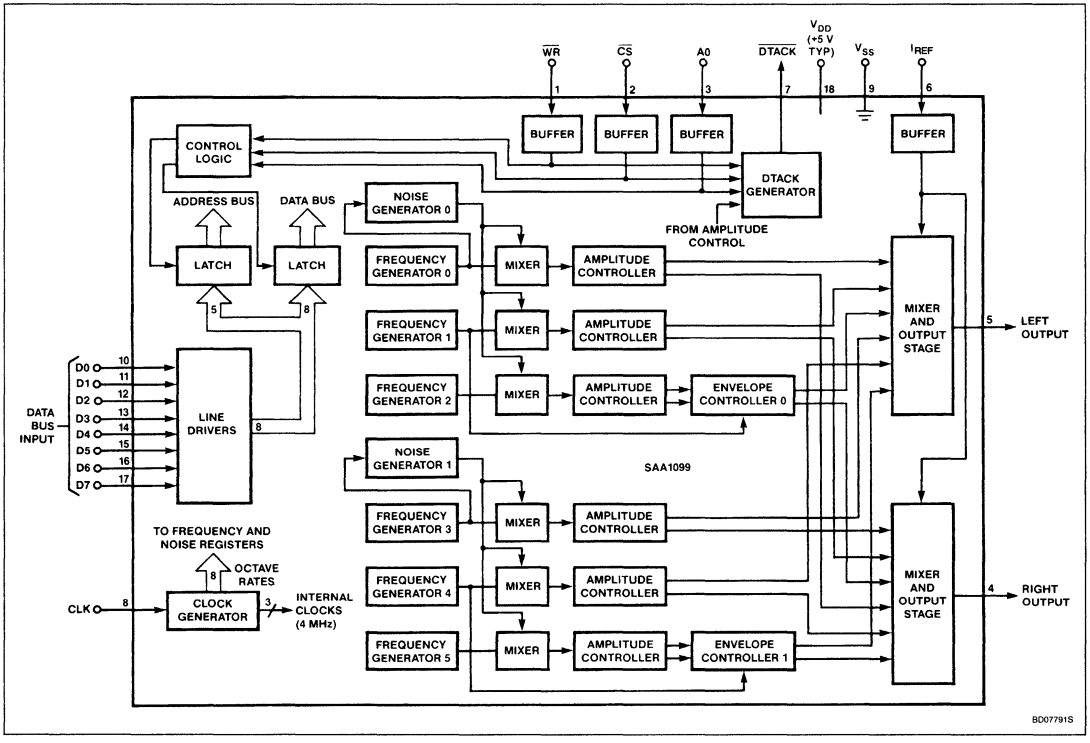
NOTE:

1 Equivalent to discharging a 250pF capacitor through a 1kΩ series resistor

Stereo Sound Generator for Sound Effects and Music Synthesis

SAA1099

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{DD} = 5V; T_A = 0 to 70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage	4.5	5.0	5.5	V
I_{DD}	Supply current		55	90	mA
I_{REF}	Reference current[1]	100	250	400	μA
Inputs					
V_{IH}	Input voltage HIGH	2.0		6.0	V
V_{IL}	Input voltage LOW	−0.5		0.8	V
$\pm I_{LI}$	Input leakage current			10	μA
C_I	Input capacitance			10	pF
Outputs					
	$\overline{DTACK}$ (open-drain)[2]				
V_{OL}	Output voltage LOW at I_{OL} = 3.2mA	0		0.4	V
V_{7-9}	Voltage on Pin 7 (OFF state)	−0.3		6.0	V
C_O	Output capacitance (OFF state)			10	pF
C_L	Load capacitance			150	pF
$-I_{LO}$	Output leakage current (OFF state)			10	μA
Audio outputs (Pins 4 and 5)					
	With fixed I_{REF}[3]				
$I_{01}I_{REF}$	One channel on	90		125	%
$I_{06}/6 \times I_{REF}$	Six channels on	85		120	%
	With I_{REF} = 250μA; R_L = 1.1kΩ (±5%)				
I_{01}/I_{REF}	One channel on	95		115	%
$I_{06}/6 \times I_{REF}$	Six channels on	90		110	%
I_{01}	Output current one channel on	238		288	μA
I_{06}	Output current six channels on	1.38		1.65	mA
	With resistor supplying I_{REF}[4]				
I_{01}	Output current one channel on	155		270	μA
I_{06}	Output current six channels on	0.94		1.65	mA
R_L	Load resistance	600			Ω
$-I_{LO}$	DC leakage current all channels off			10	μA
$\pm I_{OMAX}$	Maximum current difference between left and right current sinks[5]			15	%
S/N	Signal-to-noise ratio[6]		TBD		dB

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V; T_A = 0 to 70°C; timing measurements taken at 2.0V for a logic 1 and 0.8V for a logic 0, unless otherwise specified (see waveforms Figures 1 and 2)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Bus interface timing (see Figure 1)					
t_{ASC}	A0 setup time to $\overline{CS}$ fall	0			ns
t_{CSW}	$\overline{CS}$ LOW to $\overline{WR}$ fall	30			ns
t_{ASW}	A0 setup time to $\overline{WR}$ fall	50			ns
t_{WL}	$\overline{WR}$ LOW time	100			ns
t_{BSW}	Data bus valid to $\overline{WR}$ rise	100			ns
t_{DFW}	$\overline{DTACK}$ fall delay from $\overline{WR}$ fall[7]	0		85	ns
t_{AHW}	A0 hold time from $\overline{WR}$ HIGH	0			ns
t_{CHW}	$\overline{CS}$ hold time from $\overline{WR}$ HIGH	0			ns
t_{DHW}	Data bus hold time from $\overline{WR}$ HIGH	0			ns
t_{DRW}	$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	0		100	ns
t_{CY}	Bus cycle time[8]	2CP			
t_{CY}	Bus cycle time[9]	8CP			
Clock input timing (see Figure 2)					
t_{CLK}	Clock period	120	125	255	ns
t_{HIGH}	Clock LOW time	55			ns
t_{LOW}	Clock HIGH time	55			ns

NOTES:

1 Using an external constant current generator to provide a nominal I_{REF} or external resistor connected to V_{DD}

2 This output is short-circuit protected to V_{DD} and V_{SS}

3 Measured with I_{REF} a constant value between 100 and 400μA, load resistance (R_L) allowed to match E24 (5%) in all applications via

$$R_L = \frac{0\ 27775 \pm 0\ 03611}{I_{REF}}$$

4 Measured with R_{REF} = 10kΩ (±5%) connected between I_{REF} and V_{DD}, R_L = 820Ω (±5%), OUTR and OUTL short-circuit protected to V_{SS}

5 Left and right outputs must be driven with identical configuration

6 Sample tested value only

7 This timing parameter only applies when no wait states are required, otherwise, parameter is invalid

8 The minimum bus cycle time of two clock periods is for loading all registers except the amplitude registers

9 The minimum bus cycle time of eight clock periods is for loading the amplitude registers In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500ns Without $\overline{DTACK}$ the parameter given must be used

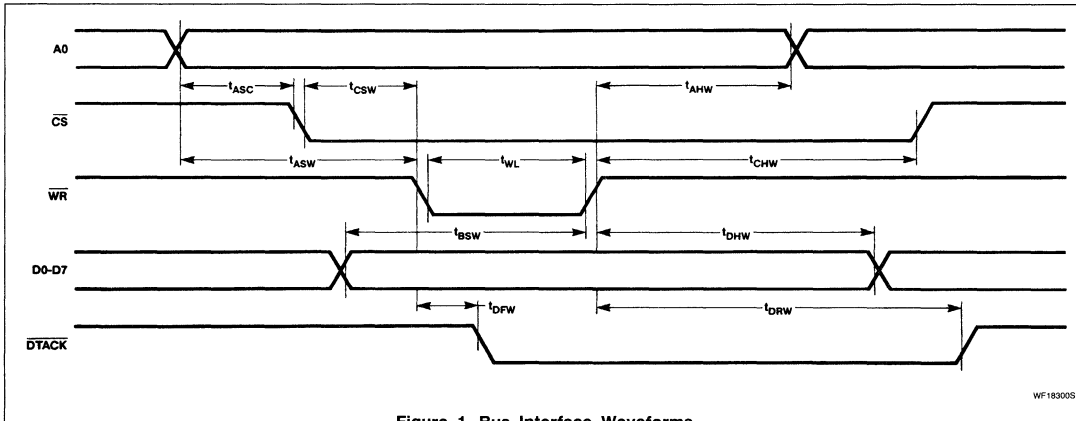


Figure 1. Bus Interface Waveforms

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FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram.

Frequency Generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 30Hz to 7.74kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone and to make it inaudible when required.

The frequency ranges per octave are:

Octave	Frequency range
0	30Hz to 60Hz
1	60Hz to 122Hz
2	122Hz to 244Hz
3	244Hz to 488Hz
4	489Hz to 976Hz
5	978Hz to 1.95kHz
6	1.95kHz to 3.90kHz
7	3.91kHz to 7.81kHz

Noise Generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three predefined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e., a range of 61Hz to 15.6kHz. In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4, and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three predefined noises are based on a clock frequency of 7.8kHz, 15.6kHz or 31.25kHz.

Noise/Frequency Mixers

There are six noise/frequency mixers, each with four selections:

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it. Three channels use noise generator 0 and the other three use noise generator 1.

Amplitude Controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope Controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.

The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Block Diagram). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.

There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Block Diagram), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event, the frequency will be the envelope rate which, provided the rate is from the frequency channel, will be a maximum of 1kHz. Higher frequencies of up to 2kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of an 8MHz clock.

Six-Channel Mixers/Current Sink Analog Output Stages

Six channels are mixed together by the two mixers, allowing each one to control one of six equally weighted current sinks to provide a seven level analog output.

Command/Control Select

In order to simplify the microprocessor interface, the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc., the command register has to be loaded. The contents of this register determine to which register the data is written in the next control cycle. If a continuous update of the control register is necessary, only the control information has to be written (the command information does not change).

If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to Microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data transfer acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

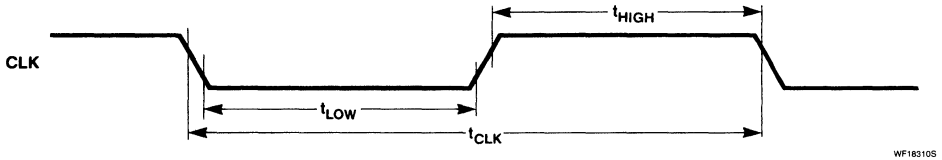

Figure 2. Clock Input Waveform

APPLICATION INFORMATION

Device Operation

The SAA1099 uses pulse-width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analog format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62.5kHz, compared with the highest tone output of 7.74kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of an 8MHz clock.

A data bus-based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded, multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors. A $\overline{DTACK}$ output is included to optimize the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately. This applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register Description (See Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel-by-channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zeroes. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3, etc). The frequency and noise enables are grouped together for ease of programming The controls for noise 'color' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls: direct acting controls and buffered controls The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Figure 3 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1. External Memory Map

SELECT A0	DATA BUS INPUTS								OPERATIONS
	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	Data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	Internal register address

NOTE:
Where X = don't care state.

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Table 2. Internal Register Map

REGISTER ADDRESS	DATA BUS INPUTS								OPERATIONS
	D7	D6	D5	D4	D3	D2	D1	D0	
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	Amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	Amplitude 1 right/left
02	2	2	2	2	2	2	2	2	Amplitude 2 right/left
03	3	3	3	3	3	3	3	3	Amplitude 3 right/left
04	4	4	4	4	4	4	4	4	Amplitude 4 right/left
05	5	5	5	5	5	5	5	5	Amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	Frequency of tone 0
09	1	1	1	1	1	1	1	1	Frequency of tone 1
0A	2	2	2	2	2	2	2	2	Frequency of tone 2
0B	3	3	3	3	3	3	3	3	Frequency of tone 3
0C	4	4	4	4	4	4	4	4	Frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	Frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	Octave 1; octave 0
11	X	032	031	030	X	022	021	020	Octave 3; octave 2
12	X	052	051	050	X	042	041	040	Octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	Frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	Noise enable
16	X	X	N11	N10	X	X	N01	N00	Noise generator 1; Noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	Envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	Envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	X	SE	Sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

NOTE:
Where:
All don't cares (X) should be written as zeroes.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

Table 3. Register Description

BIT	DESCRIPTION
ARn3; ARn2; ARn1; ARn0 (n = 0.5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1, ALn0 (n = 0.5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0.5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0.5)	3 bits for octave control 0 0 0 lowest octave (30Hz to 60Hz) 0 0 1 (60Hz to 122Hz) 0 1 0 (122Hz to 244Hz) 0 1 1 (244Hz to 488Hz) 0 1 1 (244Hz to 488Hz) 1 0 0 (489Hz to 976Hz) 1 0 1 (978Hz to 1.95kHz) 1 1 0 (1.95kHz to 3.90kHz) 1 1 1 highest octave (3.91kHz to 7.81kHz)
FEn (n = 0.5)	Frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0.5)	Noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0.1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'color') Nn1 Nn0 Clock frequency (kHz) 0 0 31.3 0 1 15.6 1 0 7.6 1 1 61 to 15.6 (frequency generator 0/2)

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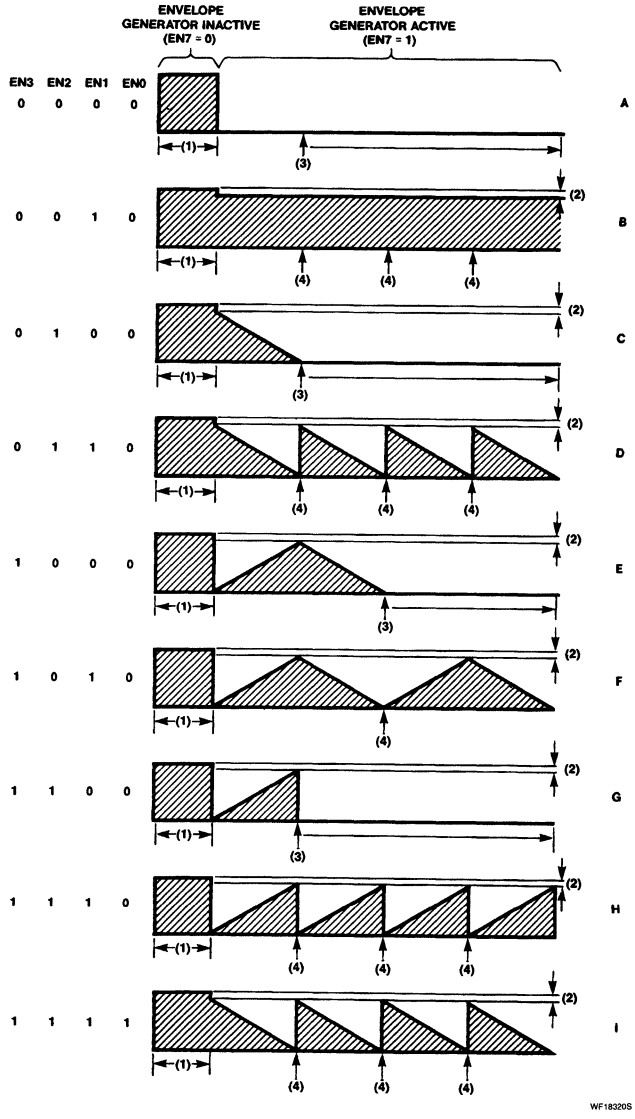
Table 3. Register Description (Continued)

BIT	DESCRIPTION
En7; En5 to En0 (n = 0.1)	7 bits for envelope control En0 0 Left and right component have the same envelope 1 Right component has inverse of envelope that is applied to left component En3 En2 En2 0 0 0 Zero amplitude 0 0 1 Maximum amplitude 0 1 0 Single decay 0 1 1 Repetitive decay 1 0 0 Single triangular 1 0 1 Repetitive triangular 1 1 0 Single attack 1 1 1 Repetitive attack En4 0 4 bits for envelope control (maximum frequency = 976Hz) 1 3 bits for envelope control (maximum frequency = 1.95kHz) En5 0 Internal envelope clock (frequency generator 1 or 4) 1 External envelope clock (address write pulse) En7 0 Reset (no envelope control) 1 Envelope control enable
SE	SE sound enable for all channels (reset on power-up to 0) 0 All channels disabled 1 All channels enabled

NOTE:
All rates given are based on the input of an 8MHz clock



NOTES:
1 The level at this time is under amplitude control only (En7 = 0, no envelope)
2 When the generator is active (En7 = 1) the maximum level possible is $^{15}/_{16}$ of the amplitude level, rounded down to the nearest eight When the generator is inactive (En = 0) the level will be $^{15}/_{16}$ of the amplitude level
3 After position (3) the buffered controls will be acted upon when loaded
4 At position (4) the buffered controls will be acted upon if already loaded
5 Waveforms 'a' to 'h' show the left channel (En0 = 0, left and right components have the same envelope)
Waveform 'i' shows the right channel (En0 = 1, right component inverse of envelope applied to left)

Figure 3. Envelope Waveforms

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Stereo Sound Generator for Sound Effects and Music Synthesis

SAA1099

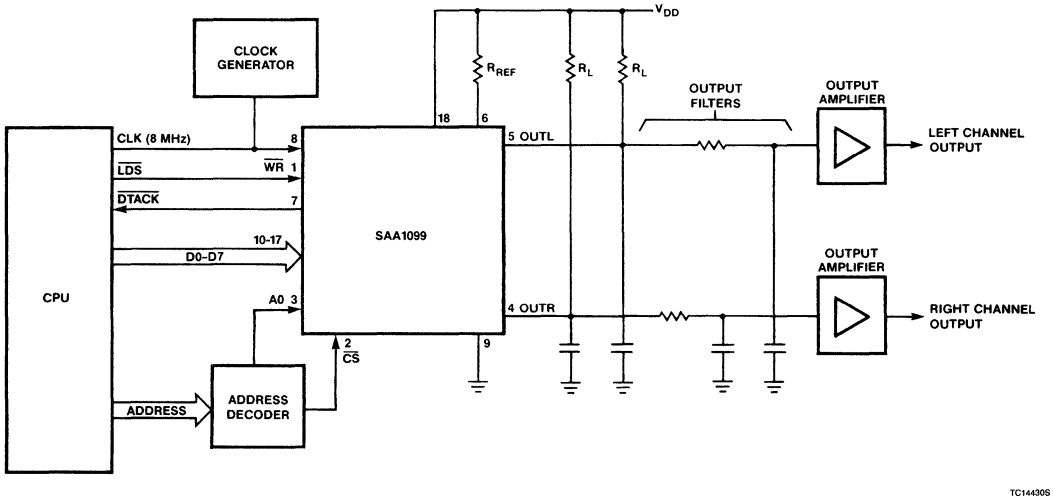


Figure 4. Typical Application Circuit Diagram

Signetics

Linear Products

Section 9
Packaging Information

INDEX

Substrate Design Guidelines for Surface-Mounted Devices

INTRODUCTION

SMD technology embodies a totally new automated circuit assembly process using a new generation of electronic components: surface-mounted devices (SMDs). Smaller than conventional components, SMDs are placed onto the surface of the substrate, not through it like leaded components. And from this, the fundamental difference between SMD assembly and conventional through-hole component assembly arises; SMD component positioning is relative, not absolute.

When a through-hole (leaded) component is inserted into a PCB, either the leads go through the holes, or they don't. An SMD, however, is placed onto the substrate surface, its position only relative to the solderlands, and placement accuracy is therefore influenced by variations in the substrate track pattern, component size, and placement machine accuracy.

Other factors influence the layout of SMD substrates. For example, will the board be a mixed-print (a combination of through-hole components and SMDs) or an all-SMD design? Will SMDs be on one side of the substrate or both? And there are process considerations, such as: what type of machine will place the components and how will they be soldered?

Using our expertise in the world of SMD technology, this section draws upon applied research in the area of substrate design and manufacture, and presents the basic guidelines to assist the designer in making the transition from conventional through-hole PCB assembly to SMD substrate manufacture.

Designing With SMD

SMD technology is penetrating rapidly into all areas of modern electronic equipment manufacture — in professional, industrial, and consumer applications. Boards are made with conventional print-and-etch PCBs, multilayer boards with thick film ceramic substrates, and with a host of new materials specially developed for SMD assembly.

However, before substrate layout can be attempted, footprints for all components must be defined. Such a footprint will include the combination of patterns for the copper solderlands, the solder resist, and, possibly, the solder paste. So the design of a substrate breaks down into two distinct areas: the SMD footprint definition, and the layout and track routing for SMDs on the substrate.

Each of these areas is treated individually; first, the general aspects of SMD technology, including substrate configurations, placement machines, and soldering techniques, are discussed.

Substrate Configurations

SMD substrate assembly configurations are classified as:

Type I — Total surface mount (all-SMD); substrates with no through-hole components at all. SMDs of all types (SM integrated circuits, discrete semiconductors, and passive devices) can be mounted either on one side, or both sides, of the substrate. See Figure 1a.

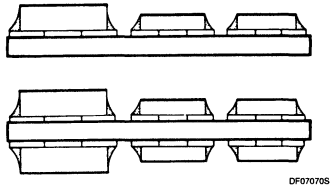
Type IIA — Double-sided mixed-print; substrates with both through-hole components and SMDs of all types on the top, and smaller SMDs (transistors and passives) on the bottom. See Figure 1b.

Type IIB — Underside attachment mixed-print; the top of the substrate is dedicated exclusively to through-hole components, with smaller SMDs (transistor and passives) on the bottom. See Figure 1c.

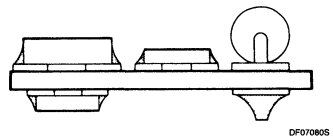
Although the all-SMD substrate will ultimately be the cheapest and smallest variation as there are no through-hole components, it's the mixed-print substrate that many manufacturers will be looking to in the immediate future, for this technique enjoys most of the advantages of SMD assembly and overcomes the problem of non-availability of some components in surface-mounted form.

The underside attachment variation of the mixed-print (type IIB — which can be thought of as a conventional through-hole assembly with SMDs on the solder side) has the added advantages of only requiring a single-sided, print-and-etch PCB and of using the established wave soldering technique. The all-SMD and mixed-print assembly with SMDs on both sides require reflow or combination wave/reflow soldering, and, in most cases, a double-sided or multilayer substrate.

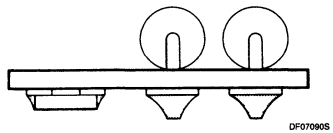
The relatively small size of most SMD assemblies compared with equivalent through-hole designs means that circuits can often be repeated several times on a single substrate. This multiple-circuit substrate technique (shown in Figure 2) further increases production efficiency.



a. Type I — Total Surface-Mount (all-SMD) Substrates



b. Type IIA — Mixed-Print (Double-Sided) Substrate



c. Type IIB — Mixed-Print (Underside Attachment) Substrate

Figure 1

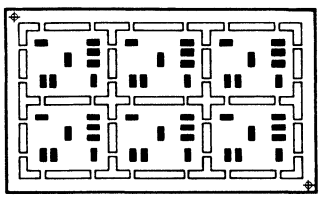


Figure 2. Multiple-Circuit Substrate

Mixed Prints

The possibility of using a partitioned design should be investigated when considering the mixed-print substrate option. For this, part of the circuit would be an all-SMD substrate, and the remainder a conventional through-hole

Substrate Design Guidelines for Surface-Mounted Devices

PCB or mixed-print substrate. This allows the circuit to be broken down into, for example, high and low power sections, or high and low frequency sections.

Automated SMD Placement Machines

The selection of automated SMD placement machines for manufacturing requirements is an issue reaching far beyond the scope of this section. However, as a guide, the four main placement techniques are outlined. They are·

In-Line Placement — a system with a series of dedicated pick-and-place units, each placing a single SMD in a preset position on the substrate. Generally used for small circuits with few components. See Figure 3a.

Sequential Placement — a single pick-and-place unit sequentially places SMDs onto the substrate. The substrate is positioned below the pick-and-place unit using a computer-controlled X-Y moving table (a "software programmable" machine). See Figure 3b.

Simultaneous Placement — places all SMDs in a single operation. A placement module (or station), with a number of pick-and-place units, takes an array of SMDs from the packaging medium and simultaneously places them on the substrate. The pick and place units are guided to their substrate location by a program plate (a "hardware programmable" machine), or by software-controlled X-Y movement of substrate and/or pick-and-place units. See Figure 3c.

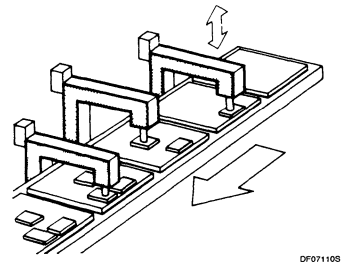
Sequential/Simultaneous Placement — a complete array of SMDs is transferred in a single operation, but the pick-and-place units within each placement module can place all devices simultaneously, or individually (sequentially). Positioning of the SMDs is software-controlled by moving the substrate on an X-Y moving table, by X-Y movement of the pick-and-place units, or by a combination of both. See Figure 3d.

All four techniques, although differing in detail, use the same two basic steps: picking the SMD from the packaging medium (tape, magazine, or hopper) and placing it on the substrate. In all cases, the exact location of each SMD must be programmed into the automated placement machine.

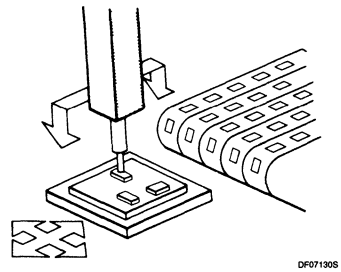
Soldering Techniques

The SMD-populated substrate is soldered by conventional wave soldering, reflow soldering, or a combination of both wave and reflow soldering. These techniques are covered at length in another publication entitled *SMD Soldering Techniques*, but, briefly, they can be described as follows:

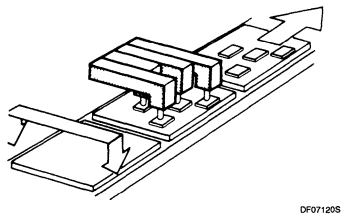
Wave Soldering — the conventional method of soldering through-hole component assemblies where the substrate passes over a wave (or more often, two waves) of molten solder. This technique is favored for mixed-print assemblies with through-hole components on the top of the substrate, and SMDs on the bottom.



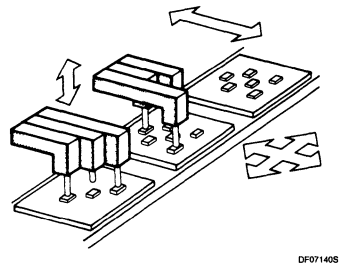
a. In-line Placement



b. Sequential Placement



c. Simultaneous Placement



d. Sequential/Simultaneous Placement

Figure 3

Reflow Soldering — a technique originally developed for thick-film hybrid circuits using a solder paste or cream (a suspension of fine solder particles in a sticky resin-flux base) applied to the substrate which, after component placement, is heated and causes the solder to melt and coalesce. This method is predominantly used for Type I (all-SMD) assemblies.

Combination Wave/Reflow Soldering — a sequential process using both the foregoing techniques to overcome the problems of soldering a double-sided mixed-print substrate with SMDs and through-hole components on the top, and SMDs only on the bottom. (Type IIB).

Footprint Definition

An SMD footprint, as shown in Figure 4, consists of:

- A pattern for the (copper) solderlands
- A pattern for the solder resist
- If applicable, a pattern for the solder cream.

The design for the footprint can be represented as a set of nominal coordinates and dimensions. In practice, the actual coordinates of each pattern will be distributed around these nominal values due to positioning and processing tolerances. Therefore, the coordinates are stochastic; the actual values form a probability distribution, with a mean value (the nominal value) and a standard deviation.

The coordinates of the SMD are also stochastic. This is due to the tolerances of the actual component dimensions and the positional errors of the automated placement machine.

The relative positions of solderland, solder resist pattern, and SMD, are not arbitrary. A number of requirements may be formulated concerning clearances and overlaps. These include:

- Limiting factors in the production of the patterns (for example, the spacing between solderlands or tracks has a minimum value)

Substrate Design Guidelines for Surface-Mounted Devices

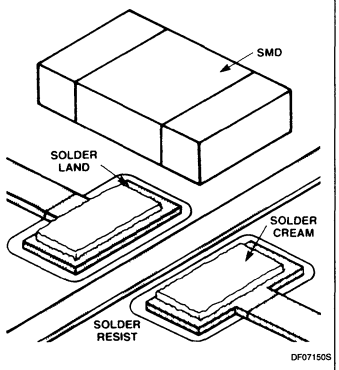


Figure 4. Component Lead, Solder Land, Solder Resist, and Solder Cream "Footprint"

- Requirements concerning the soldering process (for example, the solderlands must be free of solder resist)
- Requirements concerning the quality of the solder joint (for example, the solderland must protrude from the SMD metallization to allow an appropriate solder meniscus)

Mathematical elaboration of these requirements and substitution of values for all tolerances and other parameters lead to a set of inequalities that have to be solved simultaneously. To do this manually using worst-case design is not considered realistic. A better approach is to use a statistical analysis; although this requires a complex computer program, it can be done.

Such an approach may deliver more than one solution, and, if this is so, then the optimal solution must be determined. Optimization is achieved by setting the following objective — find the solution that:

- Minimizes the area occupied by the footprint
- Maximizes the number of tracks between adjacent solderlands.

The final SMD footprint design also depends on the soldering process to be used. The requirements for a wave-soldered substrate differ from those for a reflow-soldered substrate, so each is discussed individually.

Footprints for Wave Soldering

To determine the footprint of an SMD for a wave-soldered substrate, consider four main interactive factors:

- The component dimensions plus tolerances — determined by the component manufacturer
- The substrate metallization — positional tolerance of the solderland with respect to a reference point on the substrate
- The solder resist — positional tolerance of the solder resist pattern with respect to the same reference point
- The placement tolerance — the ability of an automated placement machine to accurately position the SMD on the substrate.

The coordinates of patterns and SMDs have to meet a number of requirements. Some of these have a general validity (the minimum overlap of SMD metallization and solderland) and available space for solder meniscus. Others are specifically required to allow successful wave soldering. One has to take into account factors like the "shadow effect" (missing of joints due to high component bodies), the risk of solder bridging, and the available space for a dot of adhesive.

The "Shadow Effect"

In wave soldering, the way in which the substrate addresses the wave is important. Unlike wave soldering of conventional printed boards where there are no component bodies to restrict the wave's freedom to traverse across the whole surface, wave soldering of SMD substrates is inhibited by the presence of SMDs on the solder-side of the board. The solder is forced around and over the SMDs as shown in Figure 5a, and the surface tension of the molten solder prevents its reaching the far end of the component, resulting in a dry-joint downstream of the solder flow. This is known as the "shadow effect."

The shadow effect becomes critical with high component bodies. However, wetting of the solderlands during wave soldering can be improved by enlarging each land as shown in Figure 5b. The extended substrate metallization makes contact with the solder and allows it to flow back and around the component metallization to form the joint.

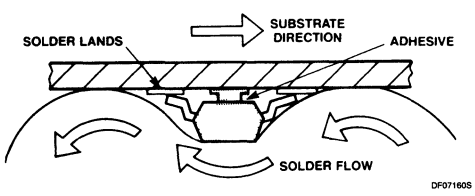
The use of the dual-wave soldering technique also partially alleviates this problem because the first, turbulent wave has sufficient upward pressure to force solder onto the component metallization, and the second, smooth wave "washes" the substrate to form good fillets of solder. Similarly, oil on the surface of the solder wave lowers the surface tension, (which lessens the shadow effect), but this technique introduces problems of contaminants in the solder when the oil decomposes.

Footprint Orientation

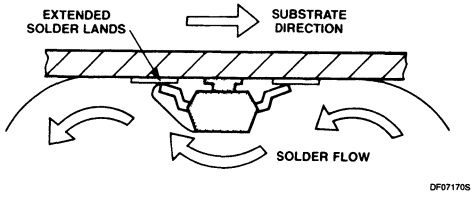
The orientation of SO (small outline) and VSO (very small outline) ICs is critical on wave-soldered substrates for the prevention of solder bridge formation. Optimum solder penetration is achieved when the central axis of the IC is parallel to the flow of solder as shown in Figure 6a. The SO package may also be transversely oriented, as shown in Figure 6b, but this is totally unacceptable for the VSO package.

Solder Thieves

Even with parallel mounted SO and VSO packages, solder bridges have a tendency to form on the leads downstream of the solder flow. The use of solder thieves (small squares of substrate metallization), shown in Figure 7 for a 40-pin VSO, further reduces the likelihood of solder-bridge formation.



a. Surface Tension Can Prevent the Molten Solder From Reaching the Downstream End of the SMD, Known as the "Shadow Effect"

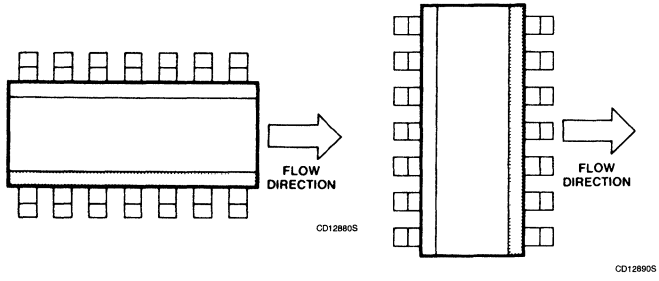


b. Extending the Solder Lands to Overcome the Shadow Effect

Figure 5

9

Substrate Design Guidelines for Surface-Mounted Devices



a. Parallel Orientation for SO and VSO Packages

b. Transverse Orientation for SO Packages Only

Figure 6

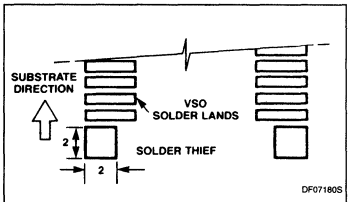


Figure 7. Example of Solder Thieves for VSO-40 Footprints (Dims in mm)

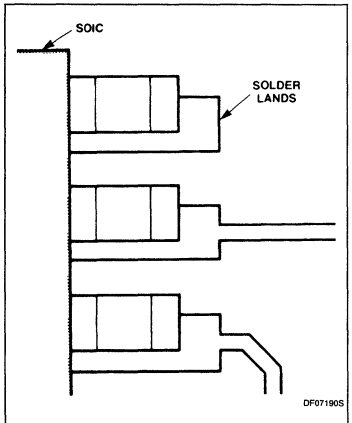


Figure 8. Misaligned Placement of SO Package Increases the Possibility of Solder Bridging

Placement Inaccuracy

Another major cause of solder bridges on SO ICs and plastic leaded chip carriers (PLCCs) is a slight misalignment as shown in Figure 8. The close spacing of the leads on these devices means that any inaccuracy in placement drastically reduces the space between adjacent pins and solderlands, thus increasing the chance of solder bridges forming.

Dummy Tracks for Adhesive Application

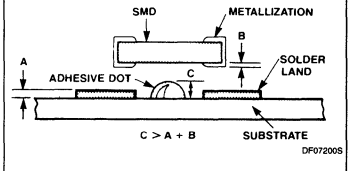
For wave soldering, an adhesive to affix components to the substrate is required. This is necessary to hold the SMDs in place between the placement operation and the soldering process (this technique is covered at length in another publication entitled *Adhesive Application and Curing*).

The amount of adhesive applied is critical for two reasons: first, the adhesive dot must be high enough to reach the SMD, and, second, there mustn't be too much adhesive which could foul the solderland and prevent the formation of a solder joint. The three parameters governing the height of the adhesive dot are shown in Figure 9. Although this diagram illustrates that the minimum requirement is $C > A + B$, in practice, $C > 2(A + B)$ is more realistic for the formation of a good strong bond.

Taking these parameters in turn, the substrate metallization height (A) can range from about 35μm for a normal print-and-etch PCB to 135μm for a plated through-hole board. And the component metallization height (B) (on 1206-size passive devices, for example) may differ by several tens of microns. Therefore, A + B can vary considerably, but it is desirable to keep the dot height (C) constant for any one substrate.

The solution to this apparent problem is to route a track under the device as shown in Figure 10. This will eliminate the substrate metallization height (A) from the adhesive dot-height criteria. Quite often, the high component density of SMD substrates necessitates the routing of tracks between solderlands, and, where it does not, a short dummy track should be introduced.

For bonding small outline (SO) ICs to the substrate, two dots of adhesive are sufficient for SO-8, -14, and -16 packages, but the SOL-20, -24, -28, and VSO-40 packages need three dots. The through-tracks (or dummy tracks) must be positioned beneath the IC accordingly to support the adhesive dots.



NOTES:
A = Substrate metallization height
B = SMD metallization height
C = Height of adhesive dot

Figure 9. Adhesive Dot Height Criteria

Footprints for Reflow Soldering

To determine the footprint of an SMD for a reflow-soldered substrate, there are now five interactive factors to consider: the four that affect the wave solder footprints (although the solder resist may be omitted), plus an additional factor relating to the solder cream application (the positional tolerance of the screen-printed solder cream with respect to the solderlands).

Solder Cream Application

In reflow soldering, the solder cream (or paste) is applied by pressure syringe dispensing or by screen printing. For industrial purposes, screen printing is the favored technique because it is much faster than dispensing.

Screen Printing

A stainless steel mesh coated with emulsion (except for the solderland pattern where cream is required) is placed over the substrate. A squeegee passes across the screen and forces solder cream through the uncoated areas of the mesh and onto the solderland. As a result, dots of solder cream of a given height and density (in mg/mm^2) are produced.

There is an optimum amount of solder cream for each joint. For example, the solder cream requirements for the C1206 SM capacitor are around 1.5mg per end; the SO IC requires between 0.5 and 0.75mg per lead.

The solder cream density, combined with the required amount of solder, makes a demand upon the area of the solderland (in mm^2). The footprint dimensions for the solder cream pattern are typically identical to those for the solderlands.

Substrate Design Guidelines for Surface-Mounted Devices

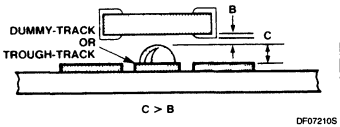


Figure 10. Through-Track or Dummy Track to Modify Dot Height Criteria

Floating

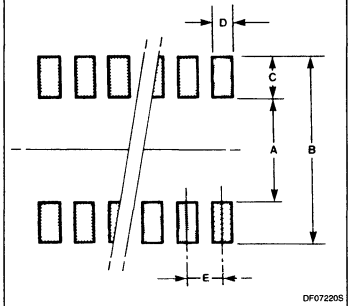
One phenomenon sometimes observed on reflow-soldered substrates is that known as "floating" (or "swimming"). This occurs when the solder paste reflows, and the force exerted by the surface tension of the now molten solder "pulls" the SMD to the center of the solderland.

When the solder reflows at both ends simultaneously, the swimming phenomenon results in the SMD self-centering on the footprint as the forces of surface tension fight for equilibrium. Although this effect can remove minor positional errors, it's not a dependable feature and cannot be relied upon. Components must always be positioned as accurately as possible.

Footprint Dimensions

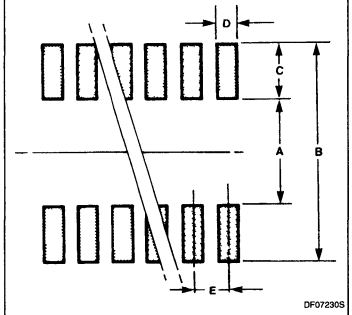
The following diagrams (Fig. 11 to 19) show footprint dimensions for SO ICs, the VSO-40 package, PLCC packages, and the range of surface-mounted transistors, diodes, resistors, and capacitors. All dimensions given are based on the criteria discussed in these guidelines.

Please note — these footprints are based on our experience with both experimental and actual production substrates and are reproduced for guidance only. Research is constantly going on to cover all SMDs currently available and those planned for in the future, and data will be published when in it becomes available.



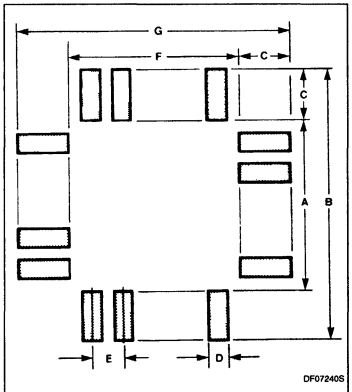
PACKAGE OUTLINE	A	B	C	D	E
	INCHES				
SO-8, 14, 16	155	275	060	024	050
SOL-16, 20, 24, 28	310	450	070	024	050
	METRIC (mm)				
SO SMALL	4 0	7 0	1 5	6	1 27
SO LARGE	7 8	11 4	1 8	6	1 27
	METRIC (mm)				
SOL-8	9 0	13 2	2 1	.6	1 27
	INCHES				
SOL-8	36	528	084	024	050

Figure 11. Footprints for SO ICs



PACKAGE OUTLINE	A	B	C	D	E
	INCHES				
VSO-40	32	536	108	02	030
VSO-56	46	676	108	02	030
	METRIC (mm)				
VSO-40	8 0	13 4	2 7	5	762
VSO-56	11 5	16 9	2 7	5	75

Figure 12. Footprints for VSO ICs



PACKAGE OUTLINE	A	B	C	D	E	F	G
	INCHES						
PLCC-20	260	.440	.090	024	050	.260	440
PLCC-28	360	540	090	024	050	.360	.540
PLCC-44	560	.740	.090	.024	.050	560	.740
PLCC-52	660	.840	090	024	.050	660	.840
PLCC-68	.8601	040	.090	.024	050	.860	1 040
PLCC-84	1 0601	.240	090	024	.050	1.060	1 240
PLCC-32	.360	540	090	024	.050	.460	.640

Figure 13. Footprints for PLCCs

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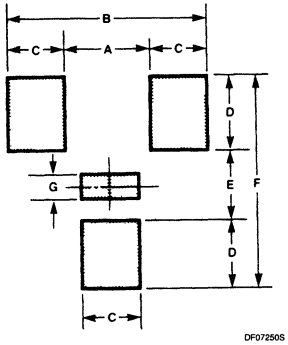
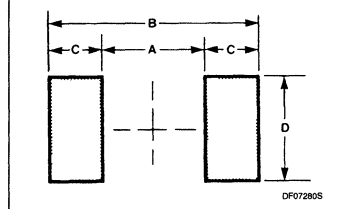
Substrate Design Guidelines for Surface-Mounted Devices



	INCHES					
SOT-23	A	B	C	D	E	F
Reflow	0 048	0 104	0 028	0 044	0 104	—
Wave	0 032	0 136	0 052	0 052	0 048	0 152

	METRIC (mm)					
SOT-23	A	B	C	D	E	F
Reflow	1 2	2 6	0.7	1 1	2 6	—
Wave	0.8	3 4	1 3	1 3	1 2	3 8

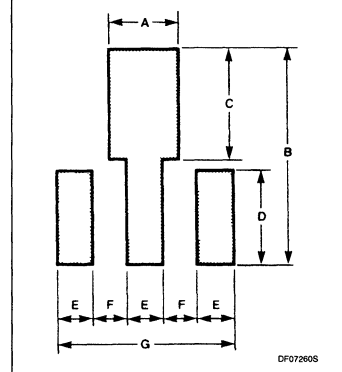
Figure 14. Footprints for SOT-23 Transistors



	INCHES			
SOD-80	A	B	C	D
Reflow	0 096	0 208	0 056	0 056
Wave	0 10	0 2	0 05	0 08

	METRIC (mm)			
SOD-80	A	B	C	D
Reflow	2 4	5 2	1 4	1 4
Wave	2 5	5 0	1 25	2 0

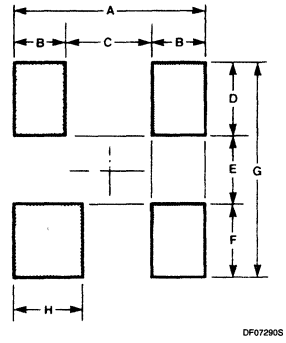
Figure 15. Footprints for SOD-80 Diodes



PACKAGE OUTLINE	INCHES						
	A	B	C	D	E	F	G
SOT-89	0 08	0 184	0 104	0 048	0 032	0 028	0 152

PACKAGE OUTLINE	METRIC (mm)						
	A	B	C	D	E	F	G
SOT-89	2 0	4 6	2 6	1 2	0 8	0 7	3 8

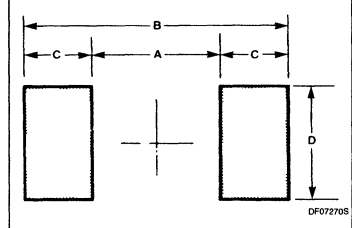
Figure 16. Footprints for Reflow-Soldered SOT-89 Transistors



PACKAGE OUTLINE	INCHES							
	A	B	C	D	E	F	G	H
SOT-143	0 104	0 028	0 048	0 036	0.044	0 036	0 116	0 044

PACKAGE OUTLINE	METRIC (mm)							
	A	B	C	D	E	F	G	H
SOT-143	2.6	0 7	1.2	0 9	1 1	0 9	2 0	1 1

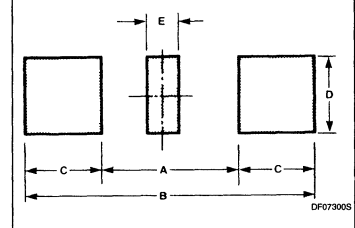
Figure 17. Footprints for Reflow-Soldered SOT-143 Transistors



		INCHES			
CODE	SIZE	A	B	C	D
C0805	0 08 × 0 05	0.032	0 136	0 052	0 056
R/C1206	0 128 × 0 064	0 072	0 184	0 056	0 068
C1210	0 128 × 0 1	0 072	0 184	0 056	0 104
C1808	0 18 × 0 08	0 112	0 248	0 068	0 084
C1812	0 18 × 0 128	0 112	0.248	0 068	0 132
C2220	0 228 × 0 2	0 16	0 296	0 068	0 204

		METRIC (mm)			
CODE	SIZE	A	B	C	D
C0805	2 0 × 1 25	0 8	3 4	1 3	1 4
R/C1206	3 2 × 1 6	1 8	4 6	1.4	1 7
C1210	3 2 × 2 5	1 8	4 6	1 4	2 6
C1808	4 5 × 2 0	2 8	6 2	1 7	2 1
C1812	4 5 × 3 2	2 8	6 2	1 7	3 3
C2220	5 7 × 5 0	4 0	7 4	1 7	5 1

Figure 18. Footprints for Reflow-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors



		INCHES				
	SIZE	A	B	C	D	E
C0805	0 08 × 1 05	0 048	0 144	0 048	0 048	0 016
R/C1206	0 128 × 0640 08		0 192	0 056	0 056	0 020

		METRIC (mm)				
CODE	SIZE	A	B	C	D	E
C0805	2.0 × 1 25	1 2	3 6	1 2	1 2	0 4
R/C1206	3 2 × 6	2 0	4 8	1 4	1 4	0 5

Figure 19. Footprints for Wave-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors

Substrate Design Guidelines for Surface-Mounted Devices

Layout Considerations

Component orientation plays an important role in obtaining consistent solder-joint quality. The substrate layout shown in Figure 20 will result in significantly better solder joints than a substrate with SMD resistors and capacitors positioned parallel to the solder flow.

Component Pitch

The minimum component pitch is governed by the maximum width of the component and the minimum distance between adjacent components. When defining the maximum component width, the rotational accuracy of the placement machine must also be considered. Figure 21 shows how the effective width of the SMD is increased when the component is rotated with respect to the footprint by angle $\phi°$. (For clarity, the rotation is exaggerated in the illustration.)

The minimum permissible distance between adjacent SMDs is a figure based upon the gap required to avoid solder-bridging during the wave soldering process. Figure 22 shows how this distance and the maximum component width are combined to derive the basic expression for calculating the minimum pitch (F_{MIN}).

As a guide, the recommended minimum pitches for various combinations of two sizes of SMDs, the R/C1206 and C0805 (R or C designating resistor or capacitor respectively; the number referring to the component size), are given in Table 1. These figures are statistically derived under certain assumed boundary conditions as follows:

- Positioning error (Δp)± 0.3mm; (± 0.012")
- Pattern accuracy (Δq)± 0.3mm; (± 0.012")
- Rotational accuracy (ϕ)± 3°
- Component metallization/solderland overlap (M_{MIN}) 0.1mm (0.004") (Note this figure is only valid for wave soldering)
- The figure for the minimum permissible gap between adjacent components (G_{MIN}) is taken to be 0.5mm (0.020").

As these calculations are not based on worst-case conditions, but on a statistical analysis of all boundary conditions, there is a certain flexibility in the given data.

For example, it is possible to position R/C1206 SMDs on a 2.5mm pitch, but the probability of component placements occurring with G_{MIN} smaller than 0.5mm will increase; hence, the likelihood of solder-bridging also increases. Each application must be assessed on individual merit with regard to acceptable levels of rework, and so on.

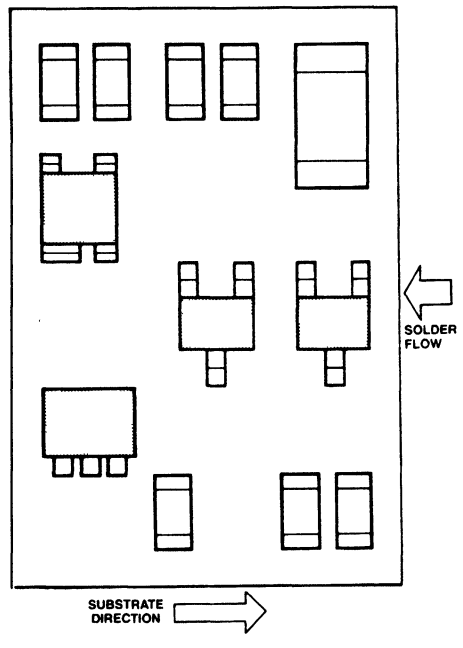
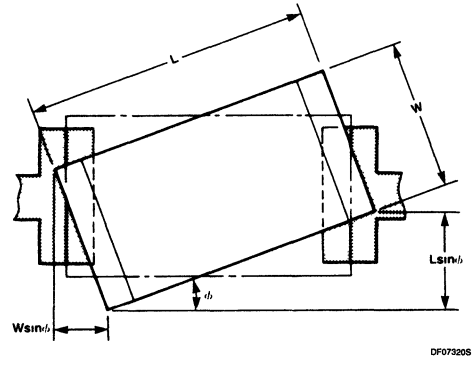


Figure 20. Recommended Component Orientation for Wave-Soldered Substrates



NOTES:
ϕ = Component rotation with respect to footprint
L sin ϕ = Effective increase in width
W sin ϕ = Effective increase in length

Figure 21. The Influence of Rotation of the SMD With Respect to the Footprint

Solderland/Via Hole Relationship

With reflow-soldered multilayer and double-sided, plated through-hole substrates, there must be sufficient separation between the via holes and the solderlands to prevent a solder well from forming. If too close to a solder joint, the via hole may suck the molten solder away from the component by capillary action; this results in insufficient wetting of the joint.

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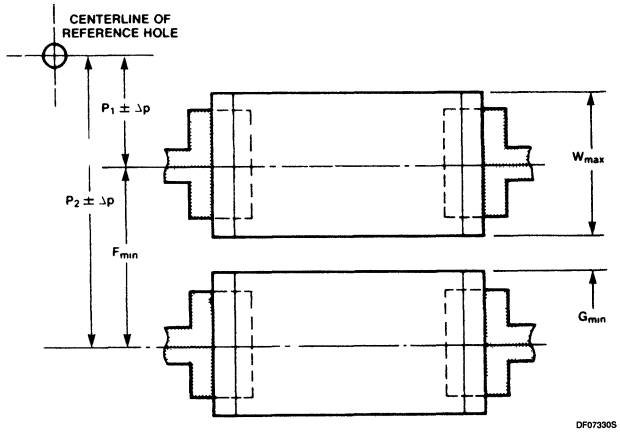
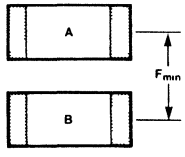
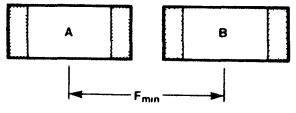
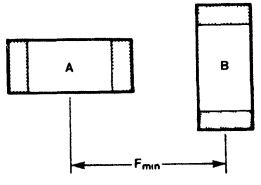
Substrate Design Guidelines for Surface-Mounted Devices



NOTES:
W_{MAX} = Maximum width of component
G_{MIN} = Minimum permissible gap
F_{MIN} = Minimum pitch
P_1 = Nominal position of component 1 (tolerance Δp)
P_2 = Nominal position of component 2 (tolerance Δp)
$F_{MIN} = W_{MAX} + 2\Delta p + G_{MIN}$

Figure 22. Criteria for Determining the Minimum Pitch of SMDs

Table 1. Recommended Pitch For R/C1206 and C0805 SMDs

Combination	Component A	Component B	
		R/C1206	C0805
	R/C1206 C0805	3.0(0.12") 2.8(0.112")	2.8(0.112") 2.6(0.0104")
	R/C1206 C0805	5.8(0.232") 5.3(0.212")	5.3(0.212") 4.8(0.192")
	R/C1206 C0805	4.1(0.164") 3.6(0.144")	3.7(0.148") 3.0(0.12")

Solderland/Component Lead Relationship

Of special consideration for mixed-print substrate layout is the location of leaded components with respect to the SMD footprints and the minimum distance between a protruding clinched lead and a conductor or SMD. Figure 23 shows typical configurations for R/C1206 SMDs mounted on the underside of a substrate with respect to the clinched leads of a leaded component. Minimum distances between the clinched lead ends and the SMDs or substrate conductors are 1mm (0.04") and 0.5 (0.02") respectively.

Placement Machine Restrictions

There are two ways of looking at the distribution of SMDs on the substrate: uniform SMD placement and non-uniform SMD placement. With nonuniform placement, center-to-center dimensions of SMDs are not exact multiples of a predetermined dimension as shown in Figure 24a, so the location of each is difficult to program into the machine.

Uniform placement uses a modular grid system with devices placed on a uniform center-to-center spacing. (For example, 2.5 (0.1") or 5mm (0.2") as shown in Figure 24b.) This placement has the distinct advantage of establishing a standard and enables the use of other automated placement machines for future production requirements without having to redesign boards.

Substrate Population

Population density of SMDs over the total area of the substrate must also be carefully considered, as placement machine limitations can create a "lane" or "zone" that restricts the total number of components which can be placed within that area on the substrate.

For example, on a hardware-programmable simultaneous placement machine (see Figure 3c), each pick-and-place unit within the placement module can only place a component on the substrate in a restricted lane (owing to

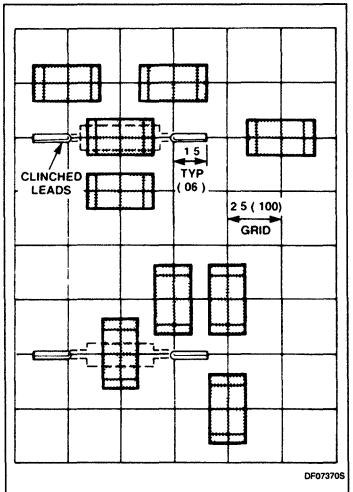
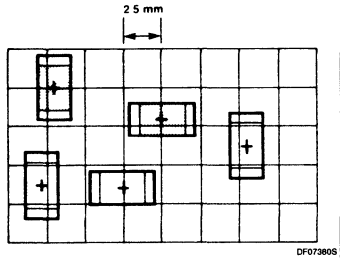
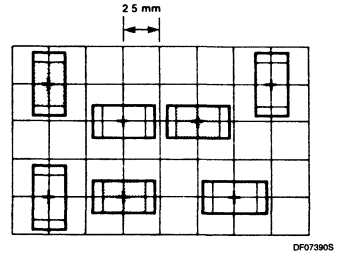


Figure 23. Location of R/C1206 SMDs on the Underside of a Mixed-Print Substrate with Respect to the Clinched Leads of Through-Hole Components (Dimensions in mm)

Substrate Design Guidelines for Surface-Mounted Devices



a. Non-Uniform Component Placement



b. Uniform Component Placement

Figure 24

adjacent pick-and-place units), typically 10 to 12mm (0.4" to 0.48") wide, as shown in Figure 25.

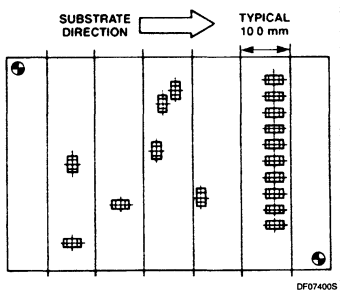


Figure 25. Substrate "Lanes" From Use of a Simultaneous Placement Machine

Placement of the 10 components in the lane on the right of the substrate shown will require a machine with 10 placement modules (or ten passes beneath a single placement module), an inefficient process considering that there are no more than three SMDs in any other lane.

Test Points

Siting of test points for in-circuit testing of SMD substrates presents problems owing to the fewer via holes, higher component densities, and components on both sides of SMD substrates. On conventional double-sided PCBs, the via holes and plated-through component lead-holes mean that most test-points are accessible from one side of the board. However, on SMD substrates, extra provision for test-points may have to be made on both sides of the substrate.

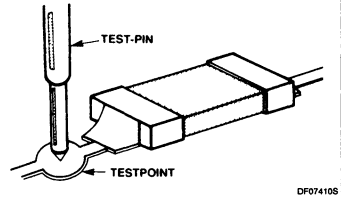
Figure 26a shows the recommended approach for positioning test-points in tracks close to components, and Figure 26b shows an acceptable (though not recommended) alternative where the solderland is extended to accommodate the test pin. This latter method avoids sacrificing too much board space, thus maintaining a high-density layout, but can introduce the problem of components moving ("floating") when reflow-soldered. The approach shown in Figure 26c is totally unacceptable since the pressure applied by the test pin can make an open-circuit soldered joint appear to be good, and, more importantly, the test pin can damage the metallization on the component, particularly with small SMDs.

CAD Systems for SMD Substrate Layout

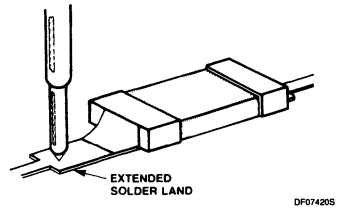
At present, about half of all PCBs are laid out using computer-aided design (CAD) techniques, and this proportion is expected to rise to over 90% by 1988. Of the many current CAD systems available for designing PCB layouts for conventional through-hole components and ICs in DIL packages, few are SMD-compatible, and systems dedicated exclusively to SMD substrate layout are still comparatively rare. There are two main reasons for this: some CAD suppliers are waiting for SMD technology to fully mature before updating their systems to cater to SMD-loaded substrates, and others are holding back until standard package outlines are fully defined.

However, updating CAD systems used for through-hole printed boards is not simply a case of substituting SMD footprints for conventional component footprints, since SMD-populated substrates impose far tougher restraints on PCB layout and require a total rethink of the layout programs. For example, systems must deal with higher component densities, finer track widths, devices on both sides of the substrate (possibly occupying corresponding positions on opposite sides), and even SMDs under conventional DILs on the same side of the substrate.

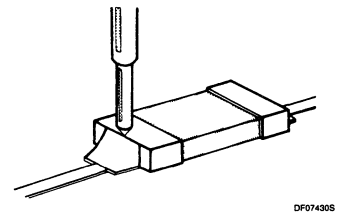
The amount of reworking that a program requires depends on whether it's an interactive (manual) system, or one with fully automatic routing and placement capabilities. For



a. RECOMMENDED Test Point Location Close to an SMD



b. Acceptable Test Point Location



c. UNACCEPTABLE Test Point Location

Figure 26

interactive systems, where the user positions the components and routes the tracks manually on-screen, program modifications will be minimal. Automatic systems, however, must contend with the stricter design rules for SMD substrate layout. For example, many autorouting programs assume that every solderland is a plated through-hole and, therefore, can be used as a via hole. This is not applicable for SMD-populated substrates.

CAD programs base the substrate layout on a regular grid. This method, analogous to drawing the layout on graph paper, must have the grid lines on a pitch that is no larger than the smallest component or feature (track width, pitch, and so on). For conventional DIL boards, this is typically 0.635mm (0.025"), but with the much smaller SMDs, a grid spacing of 0.0254mm (0.001") is required. Consequently, for the same area of substrate, a CAD system based on this finer grid requires

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a resolution more than 600 times greater than that required for conventional-layout CAD systems.

To handle this, extra memory capacity can be added, or the allowable substrate area can be limited In fact, the small size of SMDs, and the high-density layouts possible, generally result in a smaller substrate. However, high-density layout gives rise to additional complications not directly related to the SMD substrate design guidelines. Most CAD systems, for instance, cannot always completely route all interconnects, and some traces have to be routed manually. This can be particularly difficult with the fewer via holes and smaller component spacing of SMD boards.

Ideally, the CAD program should have a "tear-up and start again" algorithm that allows it to restart autorouting if a previous attempt reaches a position where no further traces can be routed before an acceptable percentage of interconnects (and this percentage must first be determined) have been made. This minimizes the manual reworking required.

CAE/CAD/CAM Interaction

Computer-aided production of printed boards has evolved from what was initially only a computer-aided manufacturing process (CAM — digitizing a manually-generated layout and using a photoplotter to produce the artwork) to fully-interactive computer-aided engineering, design, and manufacture using a common database. Figure 27 illustrates how this multi-dimensional interaction is particularly well-suited to SMD-populated substrate manufacture in its highly-automated environment of pick-and-place assembly machines and test equipment.

Using a fully-integrated system, linked by local area network to a central database, will make it possible to use the initial computer-aided engineering (CAE — schematic design, logic verification, and fault simulation) in the generation of the final test patterns at the end of the development process. These test patterns can then be used with the automatic test equipment (ATE) for functional testing of the finished substrates.

Such a system is particularly useful for testing SMD-populated substrates, as their high component density and fewer via-holes make in-circuit testing ("bed of nails" approach) difficult Consequently, manufacturers are turning to functional testing as an alternative. These aspects are covered in another publication entitled *Functional Testing and Repair.*

Substrate Design Guidelines for Surface-Mounted Devices

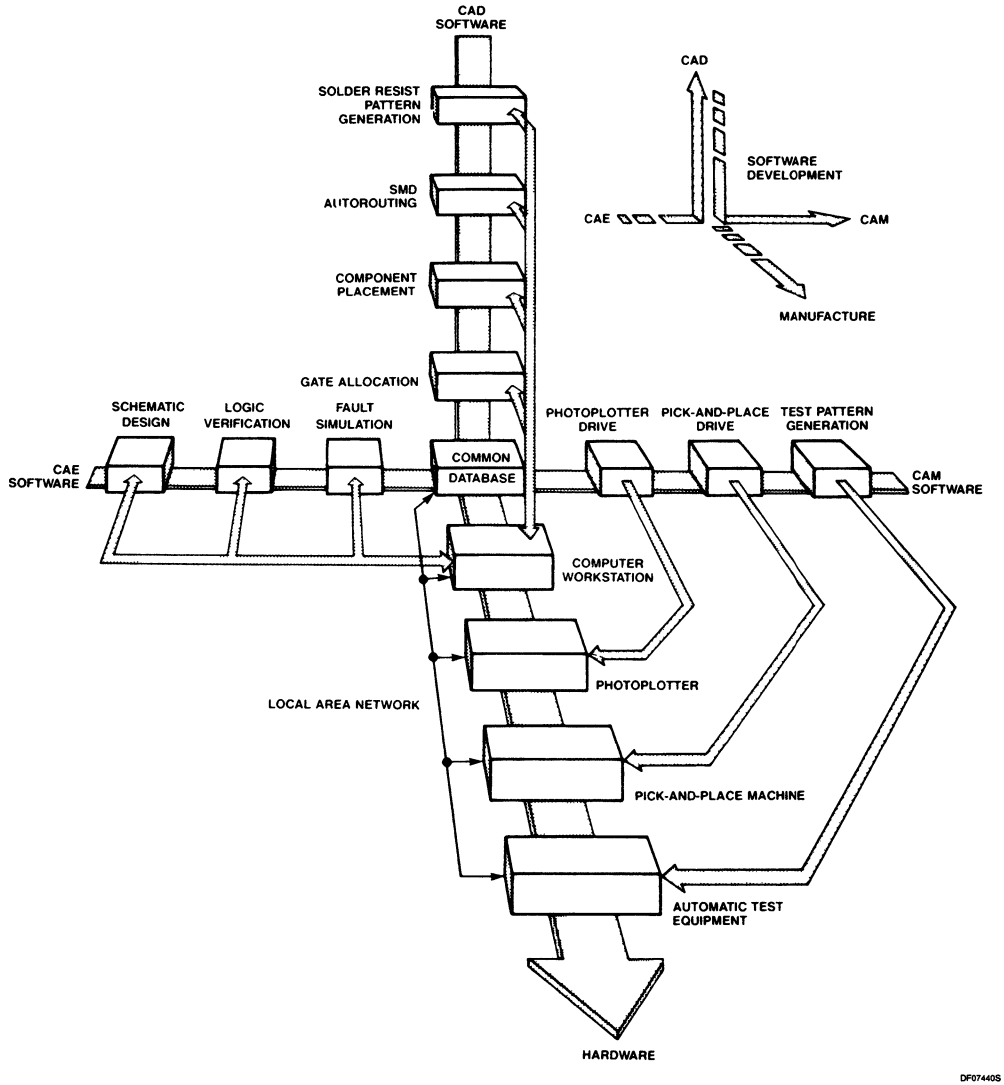

Figure 27. The Software-Hardware Interaction for the Computer-Aided Engineering, Design, and Manufacture of SMD Substrates

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AN INTRODUCTION

The key questions that must be asked of any electronic circuit are "does it work, and will it continue to do so over a specified period of time?" Until zero-defect soldering is achieved, and all components are guaranteed serviceable by the vendors, manufacturers can only answer these questions by carrying out some form of test on the finished product.

The types of tests, and the depth to which they are carried out, are determined by the complexity of the circuit and the customer's requirements. The amount of rework to be performed on the circuit will depend on the results of these tests and the degree of reliability demanded. The criteria are true of all electronic assemblies, and the test engineer must formulate test schedules accordingly.

Substrates loaded with surface mounted devices (SMDs), however, pose additional problems to the test engineer. The devices are much smaller, and substrate population density is greater, leading to difficulty in accessing all circuit nodes and test points. Also SMD substrate layout designs often have fewer via and component lead holes, so test points may not all be on one side of the substrate and double-sided test fixtures become necessary.

To achieve the high throughput rates made possible by using highly automated SMD placement machines and volume soldering techniques, automatic testing becomes a necessity. Visual inspection of the finished substrate by trained inspectors can normally detect about 90% of defects. With the correct combination of automatic test equipment, the remainder can be eliminated. In this publication, we hope to provide the manufacturer with information to enable him to evaluate and select the best combination of test equipment and the most effective test methods for his product.

BARE-BOARD TESTING

Although SMD substrates will undoubtedly be smaller than conventional through-hole substrates and have less space between conductors, the principles of bare-board testing remain the same. Many of the testers already in use can, with little or no modification, be used for SMD substrates. As this is already a well-established and well-documented practice, it will not be discussed further in this publication, but it is recommended that bare-board testing always be used as the first step in assuring board integrity.

POST-ASSEMBLY TESTING

Testing densely populated substrates is no easy task, as the components may occupy both sides of the board and cover many of the circuit nodes (see Figure 1 for the three main types of SMD-populated substrates). Unlike conventional substrates, on which all test points are usually accessible from the bottom, SMD assemblies must be designed from the start with the siting of test points in mind. Probing SMD substrates is particularly difficult owing to the very close spacing of components and conductors.

Mixed print or all-SMD assemblies with components on both sides further aggravate the testing problems, as not all test points are present on the same side of the board. Although two-sided test fixtures are feasible, they are expensive and require considerable time to build.

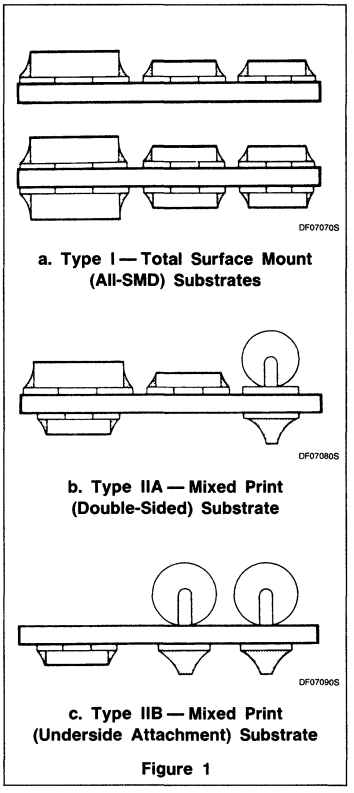
The application of a test probe to the top of an SMD termination could damage it, and probe pressure on a poor or open solder joint can force contact and thus allow a defective joint to be assessed as good. Figure 2a illustrates the recommended siting of test points close to SMD terminations, and Figure 2b shows an alternative, though not recommended, option. Here, problems could arise from reflow soldering (solder migrating from the joint) unless the test point area is separated from the solder land area with a stripe of solder resist. Excessive mechanical pressure caused by too many probes concentrated in a small area may also result in substrate damage.

It is good practice for substrates to have test points on a regular grid so that conventional, rather than custom, testers may be used. If the substrate has tall components or heat-sinks, the test points must be located far enough away to allow the probes to make good contact. All test points should be solder coated to provide good electrical contact. Via holes may also be used as test points, but the holes must be filled with solder to prevent the probe from sticking.

AUTOMATIC TEST EQUIPMENT (ATE)

As manufacturers strive to increase production, the question becomes not whether to use automatic test engineering (ATE), but which ATE system to use and how much to spend on it. Because of the rapid fall in price of computers, memories, and peripherals, today's low-cost ATE equals the performance of the high-cost equipment of just two or three years ago. For factory automation, manufacturers must consider many factors, such as production volume, product complexity, and availability of skilled personnel.

One question is whether the ATE system can be used not only for production testing but also for service and repair to reduce the high cost of keeping a substrate inventory in the field. Another is whether assembly and process-induced faults represent a significant percentage of production defects, rather than out-of-tolerance components. These questions need to be answered before deciding on the type of ATE system required.

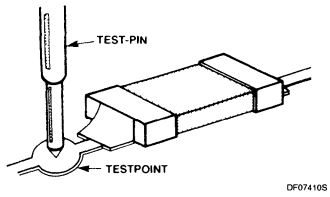


a. Type I — Total Surface Mount (All-SMD) Substrates

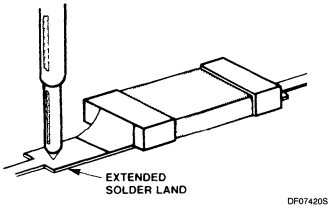
b. Type IIA — Mixed Print (Double-Sided) Substrate

c. Type IIB — Mixed Print (Underside Attachment) Substrate

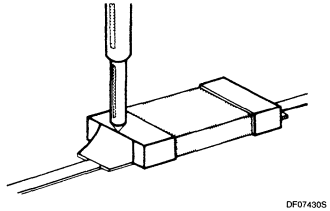
Figure 1



a. Recommended Location of Test Points Close to SMDs



b. Acceptable, Though Not Recommended, Location of Test Points Close to SMDs



c. Unacceptable Location of Test Points Close to SMDs

Figure 2

Several systems are currently available to the manufacturer, including short-circuit testers, in-circuit testers, in-circuit analyzers, and functional testers. Figure 3 shows a bar-chart giving a comparison of percent fault detection and programming time for various ATE systems.

A loaded-board, short-circuit tester takes from two to six hours to program and its effective fault coverage is between 35% and 65%. It has the advantage of being operationally fast and comparatively inexpensive. On the negative side, however, it is limited to the detection of short-circuits and may require a double-sided, bed-of-nails test fixture (see Figure 4), which for SMD substrates may be expensive and take time to produce. Careful

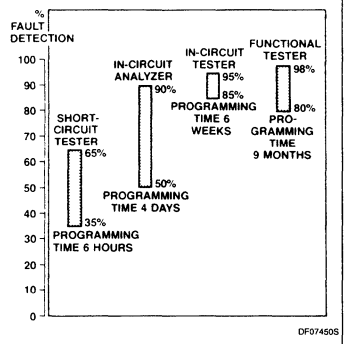


Figure 3. Bar Chart Showing a Comparison of Percent Fault Detection and Programming Time for Various ATE Systems

design can, however, often eliminate the need for double-sided test probe fixtures.

In-circuit testers power the assembly and check for open or short-circuits, circuit parameters, and can pinpoint defective components They can provide around 90% fault coverage, but are more expensive than short-circuit testers and programming can take more than six weeks.

In-circuit analyzers are relatively simple to program and can detect manufacturing-induced faults in one third of the time required by an in-circuit tester Fault coverage is between 50% and 90%. Because they do not power the assembly, they cannot detect digital logic faults, unlike an in-circuit tester or functional tester.

Functional testers, on the other hand, check the assembly's performance and simply make a go or no-go decision. Either the assembly performs its required function or it does not. They are much more expensive, but their fault coverage is between 80% and 98%. Their major disadvantages, apart from cost, are that they cannot locate defective components, and programming for a high-capacity system can take as long as nine months.

ATE Systems

An analysis of defects on a finished substrate will determine which combination of ATE will best meet the test requirements with regard to fault coverage and throughput rate.

If most defects are short-circuits, a loaded-board short-circuit tester, in tandem with an in-circuit tester, will pre-screen the substrate for short-circuits twice as fast as the in-circuit tester. This allows more time for the in-circuit tester to handle the more complex test requirements. This combination of ATE, instead of an in-circuit tester alone, improves the throughput rate.

Combining a short-circuit tester with a functional tester produces even more dramatic results. If most defects are manufacturing-produced shorts, the use of a short-circuit tester to relieve the functional tester of this task can increase throughput five-fold while maintaining a fault coverage of up to 98%.

If manufacturing faults and analog component defects are responsible for the majority of failures, a relatively low-cost, in-circuit analyzer can be used in tandem with an in-circuit tester or functional tester to reduce testing costs and improve throughput. The in-circuit analyzer is three times faster than an in-circuit tester in detecting manufacturing-induced faults, offers test and diagnostics usually within 10 seconds each, and is relatively simple to program. But because it is unpowered, an in-circuit analyzer cannot test digital logic faults, either an in-circuit tester or functional tester following the in-circuit analyzer must be used to locate this type of defect.

POLLUTED POWER SUPPLIES

Today's electronic components and the equipment used to test them are susceptible to electrical noise. Erroneous measurements on pass-or-fail tests could lower test throughput or, even more seriously, allow defective products to pass inspection. Semiconductor chips under test can also be damaged or destroyed as high-energy pulses or line-voltage surges stress the fine-line geometrics separating individual cells.

Noise pulses can be either in the normal (line-to-line) mode or common (line-to-ground) mode. Common-mode electrical noise poses a special threat to modern electronic circuitry since the safety ground line to which common-mode noise is referenced is often used as the system's logic reference point. Since parasitic capacitance exists between safety ground and the reference point, at high frequencies these points are essentially tied together, allowing noise to directly enter the system's logic.

MANUAL REPAIR

The repair of SMD-populated substrates will entail either the resoldering of individual joints and the removal of shorts or the replacement of defective components.

The reworking of defective joints will invariably involve the use of a manual soldering iron. Bits are commercially available in a variety of shapes, including special hollow bits used for desoldering and for the removal of solder bridges. The criteria for the inspec-

Test and Repair

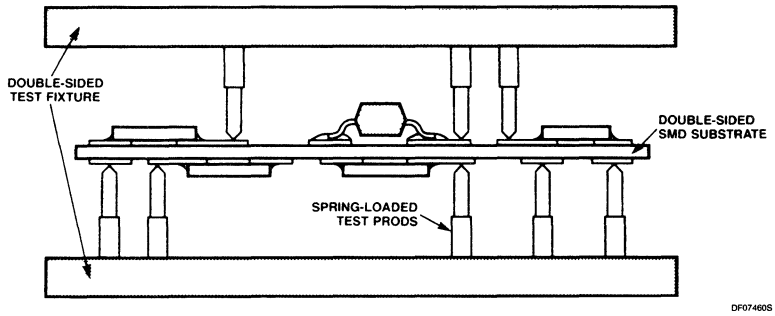


Figure 4. Double-Sided, Bed-of-Nails Test Fixture

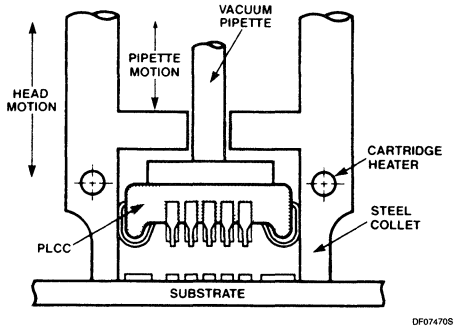


Figure 5. Heated Collet for the Removal and Replacement of Multi-Leaded SMDs (a PLCC is Shown Here)

tion of reworked soldered joints are the same as those for machine soldering.

Special care must be taken when reworking or replacing electrostatic sensitive devices. Soldering irons should be well grounded via a safety resistor of minimum 100kΩ. The ground connection to the soldering iron should be welded rather than clamped. This is because oxidation occurs beneath the clamp, thus isolating the ground connection. Voltage spikes caused by the switching of the iron can be avoided by using either continuously-powered irons, or irons that switch only at zero voltage on the AC sine curve.

To remove defective leadless SMDs, a variety of soldering iron bits are available that will apply the correct amount of heat to both ends of the component simultaneously and allow it to be removed from the substrate. If the substrate has been wave soldered, an adhesive will have been used, and the bond can be broken by twisting the bit. Any adhesive residue must then be removed. The same tool is then used to place and solder the new component, using either solder cream or resin-cored solder.

When a multi-leaded component, such as a plastic leaded chip carrier (PLCC), has to be removed, a heated collet can be used (see Figure 5). The collet is positioned over the PLCC, heat is applied to the leads and solder lands automatically until the solder reflows. The collet, complete with the PLCC, is then raised by vacuum. Solder cream is then re-applied to the solder lands by hand. No adhesive is required in this operation.

The collet is positioned over the replacement PLCC, which is held in place by the slight spring pressure of the PLCC leads against the walls of the collet. The collet, complete with PLCC, is then raised pneumatically and positioned over the solder lands.

Using air pressure, the center pin of the collet then pushes the PLCC into contact with the substrate where it is maintained with the correct amount of force. Heat is then applied through the walls of the collet to reflow the solder paste. The center pin maintains pressure on the PLCC until the solder has solidified, then the center pin is raised and the replacement is complete.

Another method, well-suited to densely populated SMD substrates, uses a stream of heated air, directed onto the SMD terminations. Once the solder has been reflowed, the component can be removed with the aid of tweezers. While the hot air is being directed onto the component, cooler air is played onto the bottom of the substrate to protect it from heat damage. During removal, the component should be twisted sideways slightly in order to break the surface tension of the solder and any adhesive bond between the component and the substrate. This prevents damage to the substrate when the component is lifted.

To fit a new component, the solder lands are first retinned and fluxed, the new component accurately placed, and the solder reflowed with hot air. Substituting superheated argon, nitrogen, or a mixture of nitrogen and hydrogen for the hot air stream removes any risk of contaminating or oxidizing the solder.

Focused infrared light has also been used successfully to reflow the solder on densely populated substrates.

In general, the equipment and procedures used for the replacement of PLCCs can be used for leadless ceramic chip carriers (LCCCs) and small-outline packages (SO ICs). SO ICs are somewhat easier to replace, as the leads are more accessible and only on two sides of the component.

Fluxing and Cleaning

INTRODUCTION

The adoption of mass soldering techniques by the electronics industry was prompted not only by economics, and a requirement for high throughput levels, but also by the need for a consistent standard of quality and reliability in the finished product unattainable by using manual methods. With surface-mounted device (SMD) assembly, this need is even greater.

The quality of the end-product depends on the measures taken during the design and manufacturing stages. The foundations of a high-quality electronic circuit are laid with good design, and with correct choice of components and substrate configuration. It is, however, at the manufacturing stage where the greatest number of variables, both with respect to materials and techniques, have to be optimized to produce high-quality soldering, a prerequisite for reliability.

Of the two most commonly-used soldering techniques, wave and reflow, wave soldering is by far the most widely used and understood. Many factors influence the outcome of the soldering operation, some relating to the soldering process itself, and others to the condition of components and substrate to which they are to be attached. These must be collectively assessed to ensure high-quality soldering.

One of the most important, most neglected, and least understood of these processes is the choice and application of flux. This section outlines the fluxing options available, and discusses the various cleaning techniques that may be required, for SMD substrate assembly.

FLUXES

Populating a substrate involves the soldering of a variety of terminations simultaneously. In one operation, a mixture of tinned copper, tin/lead-or gold-plated nickel-iron, palladium-silver, tin/lead-plated nickel-barrier, and even materials like Kovar, each possessing varying degrees of solderability, must be attached to a common substrate using a single solder alloy.

It is for this reason that the choice of the flux is so important. The correct flux will remove surface oxides, prevent reoxidization, help to transfer heat from source to joint area, and leave non-corrosive, or easily removable corrosive residues on the substrate. It will also improve wettability of the solder joint surfaces.

The wettability of a metal surface is its ability to promote the formation of an alloy at its interface with the solder to ensure a strong, low-resistance joint.

However, the use of flux does not eliminate the need for adequate surface preparation. This is very important in the soldering of SMD substrates, where any temptation to use a highly-active flux in order to promote rapid wetting of ill-prepared surfaces should be avoided because it can cause serious problems later when the corrosive flux residues have to be removed. Consequently, optimum solderability is an essential factor for SMD substrate assembly.

Flux is applied before the wave soldering process, and during the reflow soldering process (where flux and solder are combined in a solder cream). By coating both bare metal and solder, flux retards atmospheric oxidization which would otherwise be intensified at soldering temperature. In the areas where the oxide film has been removed, a direct metal-to-metal contact is established with one low-energy interface. It is from this point of contact that the solder will flow

Types of Flux

There are two main characteristics of flux. The first is efficacy—its ability to promote wetting of surfaces by solder within a specified time. Closely related to this is the activity of the flux, that is, its ability to chemically clean the surfaces.

The second is the corrosivity of the flux, or rather the corrosivity of its residues remaining on the substrate after soldering. This is again linked to the activity; the more active the flux, the more corrosive are its residues.

Although there are many different fluxes available, and many more being developed, they fall into two basic categories; those with residues soluble in organic liquids, and those with residues soluble in water.

Organic Soluble Fluxes

Most of the fluxes soluble in organic liquids are based on colophony or rosin (a natural product obtained from pine sap that has been distilled to remove the turpentine content). Solid colophony is difficult to apply to a substrate during machine soldering, so it is dissolved in a thinning agent, usually an alcohol. It has a very low efficacy, and hence limited cleaning power, so activators are added in varying quantities to increase it. These take the form of either organic acids, or organic salts that are chemically active at soldering temperatures. It is therefore convenient to classify the colophony-based fluxes by their activator content.

Non-Activated Rosin (R) Flux

These fluxes are formed from pure colophony in a suitable solvent, usually isopropanol or ethyl alcohol. Efficacy is low and cleaning action is weak. Their uses in electronic soldering are limited to easily-wettable materials with a high level of solderability. They are used mainly on circuits where no risk of corrosion can be tolerated, even after prolonged use (implanted cardiac pacemakers, for example). Their flux residues are noncorrosive and can remain on the substrate, where they will provide good insulation.

Rosin, Mildly-Activated (RMA) Flux

These fluxes are also composed of colophony in a solvent, but with the addition of activators, either in the form of di-basic organic acids (such as succinc acid), or organic salts (such as dimethylammonium chloride or diethylammonium chloride). It is customary to express

the amount of added activator as mass percent of the chlorine ion on the colophony content, as the activator-to-colophony ratio determines the activity, and, hence, the corrosivity. In the case of RMA activated with organic salts, this is only some tenths of one percent.

When organic acids are used, a higher percentage of activator must be added to produce the same efficacy as organic salts, so frequently both salts and acids are added. The cleaning action of RMA fluxes is stronger than that of the R type, although the corrosivity of the residues is usually acceptable. These residues may be left on the substrate as they form a useful insulating layer on the metal surfaces. This layer can, however, impede the penetration of test probes at a later stage.

Rosin, Activated (RA) Flux

The RA fluxes are similar to the RMA fluxes, but contain a higher proportion of activators. They are used mainly when component or substrate solderability is poor and corrosion-risk requirements are less stringent. However, as good solderability is considered essential for SMD assembly, highly-activated rosin fluxes should not be necessary. The removal of

Fluxing and Cleaning

flux residues is optional and usually dependent upon the working environment of the finished product and the customer's requirements.

Water-Soluble Fluxes

The water-soluble fluxes are generally used to provide high fluxing activity. Their residues are more corrosive and more conductive than the rosin-based fluxes, and, consequently, must always be removed from the finished substrate. Although termed water soluble, this does not necessarily imply that they contain water; they may also contain alcohols or glycols. It is the flux residues that are water soluble. The usual composition of a water-soluble flux is shown below.

1. A chemically-active component for cleaning the surfaces.
2. A wetting agent to promote the spreading of flux constituents.
3. A solvent to provide even distribution.
4. Substances such as glycols or water-soluble polymers to keep the activator in close contact with the metal surfaces.

Although these substances can be dissolved in water, other solvents are generally used, as water has a tendency to spatter during soldering. Solvents with higher boiling points, such as ethylene glycol or polyethylene glycol are preferred.

Water-Soluble Fluxes With Inorganic Salts

These are based on inorganic salts such as zinc chloride, or ammonium chloride, or inorganic acids such as hydrochloric. Those with zinc or ammonium chloride must be followed by very stringent cleaning procedures as any halide salts remaining on the substrate will cause severe corrosion. These fluxes are generally used for non-electrical soldering. Although the hydrazine halides are among the best active fluxing agents known, they are highly suspect from a health point of view and are therefore no longer used by flux manufacturers.

Water-Soluble Fluxes With Organic Salts

These fluxes are based on organic hydrohalides such as dimethylammonium chloride, cyclo hexalamine hydrochloride, and aniline hydrochloride, and also on the hydrohalides of organic acids. Fluxes with organic halides usually contain vehicles such as glycerol or polyethylene glycol, and non-ionic surface-active agents such as nonylphenol polyoxyethylene. Some of the vehicles, such as the polyethylene glycols, can degrade the insulation resistance of epoxy substrate material and, by rendering the substrate hydrophilic, make it susceptible to electrical leakage in high-humidity environments.

Water-Soluble Fluxes With Organic Acids

Based on acids such as lactic, melonic, or citric, these fluxes are used when the presence of any halide is prohibited. However, their fluxing action is weak, and high acid concentrations have to be used. On the other hand, they have the advantage that the flux residues can be left on the substrate for some time before washing without the risk of severe corrosion.

Solder Creams

For reflow soldering, both the solder and the flux are applied to the substrate before soldering and can be in the form of solder creams (or pastes), preforms, electro-deposit, or a layer of solder applied to the conductors by dipping. For SMD reflow soldering, solder cream is generally used.

Solder cream is a suspension of solder particles in flux to which special compounds have been added to improve the rheological properties. The shape of the particles is important and normally spherical particles are used, although non-spherical particles are now being added, particularly in very fine-line soldering.

In principle, the same fluxes are used in solder creams as for wave soldering. However, due to the relatively large surface area of the solder particles (which can oxidize), more effective fluxing is required and, in general, solder creams contain a higher percentage of activators than the liquid fluxes. The drying of the solder paste during preheating (after component placement) is an important stage as it reduces any tendency for components to become displaced during soldering.

Flux Selection

Choosing an appropriate flux is of prime importance to the soldering system for the production of high-quality, reliable joints. When solderability is good, a mildly-activated flux will be adequate, but when solderability is poorer, a more effective, more active flux will be required. The choice of flux, moreover, will be influenced by the cleaning facilities available, and if, in fact, cleaning is even feasible.

With water-soluble fluxes, aqueous cleaning of the substrate after soldering is mandatory. If thorough cleaning is not carried out, severe problems may arise in the field, due to corrosion or short circuits caused by too low a surface resistance of the conductive residues.

For rosin-based fluxes, the need for cleaning will depend on the activity of the flux. Mildly-activated rosin residues can, in most cases, remain on the substrate where they will afford protection and insulation. In practice, for the great majority of electronic circuits, the choice will be between an RA or an RMA rosin-based flux.

Application of Flux

Three basic factors determine the method of applying flux: the soldering process (wave or reflow), the type of substrate being processed (all-SMD or mixed print), and the type of flux.

For wave soldering, the flux must be applied in liquid form before soldering. While it is possible to apply the flux at a separate fluxing station, with the high throughput rates demanded to maximize the benefits of SMD technology, today's wave-soldering machines incorporate an integral fluxing station prior to the preheat stage. This enables the preheat stage to be used to dry the flux as well as preheat the substrate to minimize thermal shock.

The most commonly-used methods of applying flux for wave soldering are by foam, wave, or spray.

Foam Fluxing

Foam flux is generated by forcing low-pressure clean air through an aerator immersed in liquid flux (see Figure 1). The fine bubbles produced by the aerator are guided to the surface by a chimney-shaped nozzle. The substrates are passed across the top of the nozzle so that the solder side comes in contact with the foam and an even layer of flux is applied. As the bubbles burst, flux penetrates any plated-through holes in the substrate.

Wave Fluxing

A double-sided wave can also be used to apply flux, where the washing action of the wave deposits a layer of flux on the solder side of the substrate (see Figure 2). Wave-height control is essential and a soft, wipe-off brush should be incorporated on the exit side of the fluxing station to remove excess flux from the substrate.

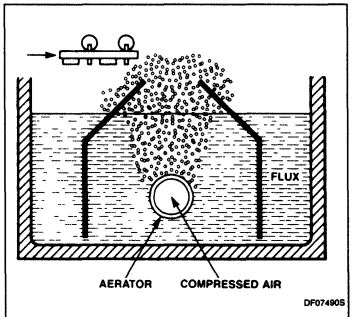


Figure 1. Schematic Diagram of Foam Fluxer

Fluxing and Cleaning

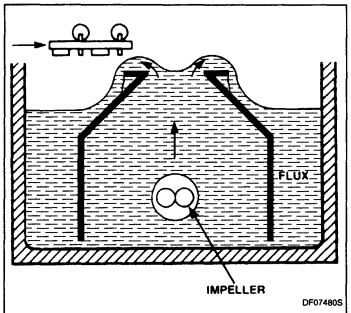


Figure 2. Schematic Diagram of Wave Fluxer

Spray Fluxing

Several methods of spray fluxing exist; the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate (see Figure 3). Four parameters affect the amount of flux deposited: conveyor speed, drum rotation, air pressure, and flux density. The thickness of the flux layer can be controlled using these parameters, and can vary between 1 and 10μm.

The advantages and disadvantages of these three flux application techniques are outlined in Table 1.

Flux Density

One of the main control factors for fluxes used in machine soldering is the flux density. This provides an indication of the solids content of the flux, and is dependent on the nature of the solvents used. Automatic control systems, which monitor flux density and inject more solvent as required, are commercially available, and it is relatively simple to incorporate them into the fluxing system.

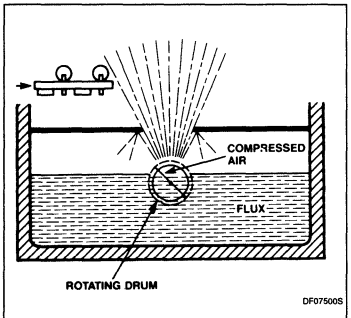


Figure 3. Schematic Diagram of Spray Fluxer

PREHEATING

Preheating the substrate before soldering serves several purposes. It dries the flux to evaporate most of the solvent, thus increasing the viscosity. If the viscosity is too low, the flux may be prematurely expelled from the substrate by the molten solder. This can result in poor wetting of the surfaces, and solder spatter.

Drying the flux also accelerates the chemical action of the flux on the surfaces, and so speeds up the soldering process. During the preheating stage, substrate and components are heated to between 80°C and 90°C (solvent-based fluxes) or to between 100°C and 110°C (water-based systems). This reduces the thermal shock when the substrate makes contact with the molten solder, and minimizes any likelihood of the substrate warping.

The most common methods of preheating are: convection heating with forced air, radiation heating using coils, infrared quartz lamps or heated panels, or a combination of both convection and radiation. The use of forced air has the added advantage of being more effective for the removal of evaporated solvent. Optimum preheat temperature and duration will depend on the nature and design of the substrate and the composition of the flux.

Figure 4 shows a typical method of preheat temperature control. The desired temperature is set on the control panel, and the microprocessor regulates preheater No. 1 to provide approximately 60% of the required heat. The IR detector scans the substrate immediately following No. 1 heater and reads the surface temperature. By taking into account the surface temperature, conveyor speed, and the thermal characteristics of the substrate, the microprocessor then calculates the amount of additional heat required to be provided by heater No. 2 in order to attain the preset temperature. In this way, each substrate will have the same surface temperature on reaching the solder bath.

POSTSOLDERING CLEANING

Now that worldwide efforts in both commercial and industrial electronics are converting old designs from conventional assembly to surface mounting, or a combination of both, it can also be expected that high-volume cleaning systems will convert from in-line aqueous cleaners to in-line solvent cleaners or in-line saponification systems (a technique that uses an alkaline material in water to react with the rosin so that it becomes water soluble). These systems may, however, become subject to environmental objections, and new governmental restrictions on the use of halogenated hydrocarbons.

The major reason for this is that the water-soluble flux residues, containing a higher concentration of activators, or showing hygroscopic behavior, are much more difficult to remove from SMD-populated substrates than rosin-based flux residues. This is primarily because the higher surface tension of water, compared to solvents, makes it difficult for the cleaning agents to penetrate beneath SMDs, especially the larger ones, with their greatly reduced off-contact distance (the distance between component and substrate).

Postsoldering cleaning removes any contamination, such as surface deposits, inclusions, occlusions, or absorbed matter which may degrade to an unacceptable level the chemical, physical, or electrical properties of the assembly. The types of contaminant on substrates that can produce either electrical or mechanical failure over short or prolonged periods are shown in Table 2.

All these contaminants, regardless of their origin, fall into one of two groups: polar and non-polar.

Polar Contaminants

Polar contaminants are compounds that dissociate into free ions which are very good conductors in water, quite capable of causing circuit failures. They are also very reactive with metals and produce corrosive reactions. It is essential that polar contaminants be removed from the substrates.

Non-Polar Contaminants

Non-polar contaminants are compounds that do not dissociate into free ions or carry an electrical current and are generally good insulators. Rosin is a typical example of a non-polar contaminant. In most cases, non-polar contamination does not contribute to corrosion or electrical failure and may be left on the substrate. It may, however, impede functional testing by probes and prevent good conformal coat adhesion.

Solvents

The solvents currently used for the post-soldering cleaning of substrates are normally organic based and are covered by three classifications: hydrophobic, hydrophilic, and azeotropes of hydrophobic/hydrophilic blends.

Azeotropic solvents are mixtures of two or more different solvents which behave like a single liquid insomuch that the vapor produced by evaporation has the same composition as the liquid, which has a constant boiling point between the boiling points of the two solvents that form the azeotrope. The basic ingredients of the azeotropic solvents are combined with alcohols and stabilizers. These stabilizers, such as nitromethane, are included to prevent corrosive reaction be-

Fluxing and Cleaning

Table 1. Advantages and Disadvantages of Flux Application Methods

Method	Advantages	Disadvantages
Foam Fluxing	• Compatible with continuous soldering process • Foam crest height not critical • Suitable for mixed-print substrates	• Not all fluxes have good foaming capabilities • Losses throught evaporation may be appreciable • Prolonged preheating because of high boiling point of solvents
Wave Fluxing	• Can be used with any liquid flux • Compatible with continuous soldering process • Suitable for densely-populated mixed print	• Wave crest height is critical to ensure good contact with bottom of substrate without contaminating the top
Spray fluxing	• Can be used with most liquid fluxes • Short preheat time if appropriate alcohol solvents are used • Layer thickness is controllable	• High flux losses due to non-recoverable spray • System requires frequent cleaning

tween the metallization of the substrate and the basic solvents.

Hydrophobic solvents do not mix with water at concentrations exceeding 0.2%, and consequently have little effect on ionic contamination. They can be used to remove non-polar contaminants such as rosin, oils, and greases.

Hydrophillic solvents do mix with water and can dissolve both polar and non-polar contamination, but at different rates. To overcome these differences, azeotropes of the various solvents are formulated to maximize the dissolving action for all types of contamination.

Solvent Cleaning

Two types of solvent cleaning systems are in use today: batch and conveyorized systems, either of which can be used for high-volume production. In both systems, the contaminated substrates are immersed in the boiling solvents, and ultrasonic baths or brushes may also be used to further improve the cleaning capabilities.

The washing of rosin-based fluxes offers advantages and disadvantages. Washed substrates can usually be inserted into racks easier, as there will be no residues on their edges; test probes can make better contact without a rosin layer on the test points, and the removal of the residues makes it easier to visually examine the soldered joints. On the other hand, washing equipment is expensive, and so are the solvents, and some solvents present a health or environmental hazard if not correctly dealt with.

Aqueous Cleaning

For high-volume production, special machines have been developed in which the substrates are conveyor-fed through the various stages of spraying, washing, rinsing, and drying. The final rinse water is blown from the substrates to prevent any deposits from the water being left on the substrate.

Where water-soluble fluxes have been used in the soldering process, substrate cleaning is mandatory. For the rosin-based fluxes, it is optional, and is often at the discretion of the customer.

Conformal Coatings

A conformal, or protective coating on the substrate, applied at the end of processing, prevents or minimizes the effects of humidity and protects the substrate from contamination by airborne dust particles. Substrates that are to be provided with a conformal coating (dependent on the environmental conditions to which the substrate will be subjected) must first be washed.

Environmental and Ecological Aspects of Fluxes and Solvents

Fumes and vapors produced during soldering processes, or during cleaning, will not, under normal circumstances, present a health hazard, if relevant health and safety regulations are observed.

Fumes originating from colophony can cause respiratory problems, so an efficient fume-extraction system is essential. The extraction system must cover the fluxing, preheating, and soldering stations, remain operational for at least one hour after machine shutdown, and conform to local regulations. Today, the problem of noxious fumes is unlikely to concern the cleaning station, as all commercial systems are equipped to condense the vapors back into the system. In the future, however, it can be expected that a much lower degree of escape of noxious fumes from any system will be allowed, and all systems may have to be reviewed.

Certain fluxes, particularly some water-soluble ones, contain highly aggressive substances, and must not be allowed to come into contact with the skin or eyes. Any contamination should immediately be removed with plenty of clean, fresh water. Deionized water should also be readily available as an eye-wash. Should contamination occur, a qualified medical practitioner should be consulted. Protective clothing should be worn during cleaning or maintenance of the fluxing station.

Conclusion

SMD technology imposes tougher restraints on fluxing and cleaning of substrate assemblies. Traditionally, rosin-based fluxes have been used in electronic soldering where residues were considered "safe" and could be left on the board. However, increased SMD packing density, fine-line tracks, and more rigid specifications have resulted in changes to this basic philosophy.

There is now a demand for surfaces free from residues; test probes are more efficient when they do not have to penetrate rosin flux residues, and conformal coating and board inspection benefit from the absence of such residues.

Cleaning also poses problems for SMD substrates. The close proximity of component and substrate means that solvents cannot effectively clean beneath devices. Components must also be compatible with the cleaning process. They must, for example, be resistant to the solvents used and to the temperatures of the cleaning process. They must also be sealed to prevent cleaning fluids from entering the devices and degrading performance.

So, eliminating the need for cleaning is better than poor or incomplete cleaning. And in a well-balanced system, mildly-activated rosin-based fluxes, leaving only non-corrosive residues, can be successfully used for SMD substrate soldering without subsequent cleaning.

Much research into fluxes and solder creams is presently being done — for example, the production of synthetic resin, with qualities superior to colophony at a lower cost. Another area of research is that of solder creams with non-melting additives, such as lead or ceramic spheres, that increase the distance

Fluxing and Cleaning

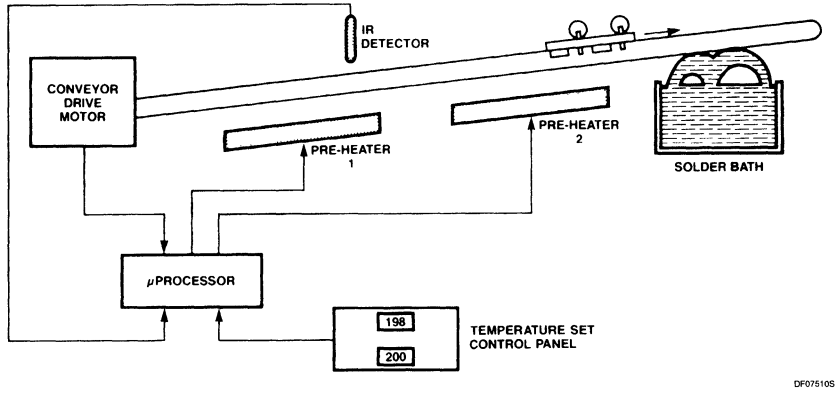


Figure 4. Schematic Diagram of a Typical Controlled Preheat System

Table 2. Substrate Contaminants

Contaminant	Origin
Organic compounds	Fluxes, solder mask
Inorganic insoluble compounds	Photo-resists, substrate processing
Organo-metallic compounds	Fluxes, substrate processing
Inorganic soluble compounds	Fluxes
Particle matter	Dust, fingerprints

between component and substrate, thus making it easier for cleaning fluids to penetrate beneath the component. It also increases the joint's ability to withstand thermal cycling.

Rosin-free and halide-free fluxes are also being developed with similar activities to conventional rosin-based fluxes. These new types will combine the "safety" of rosin fluxes with easier removal in conventional solvents. Using non-polar materials, ionizable or corrosive residues are eliminated, and the need for cleaning immediately after soldering is avoided.

Thermal Considerations for Surface-Mounted Devices

Linear Products

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long-term operating life of an IC. As will be shown in this section, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. **Some of the VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface-Mount Device (SMD) technology, management of thermal characteristics remains a valid concern, not only because the SMD packages are much smaller, but also because the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface-mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

POWER DISSIPATION

Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

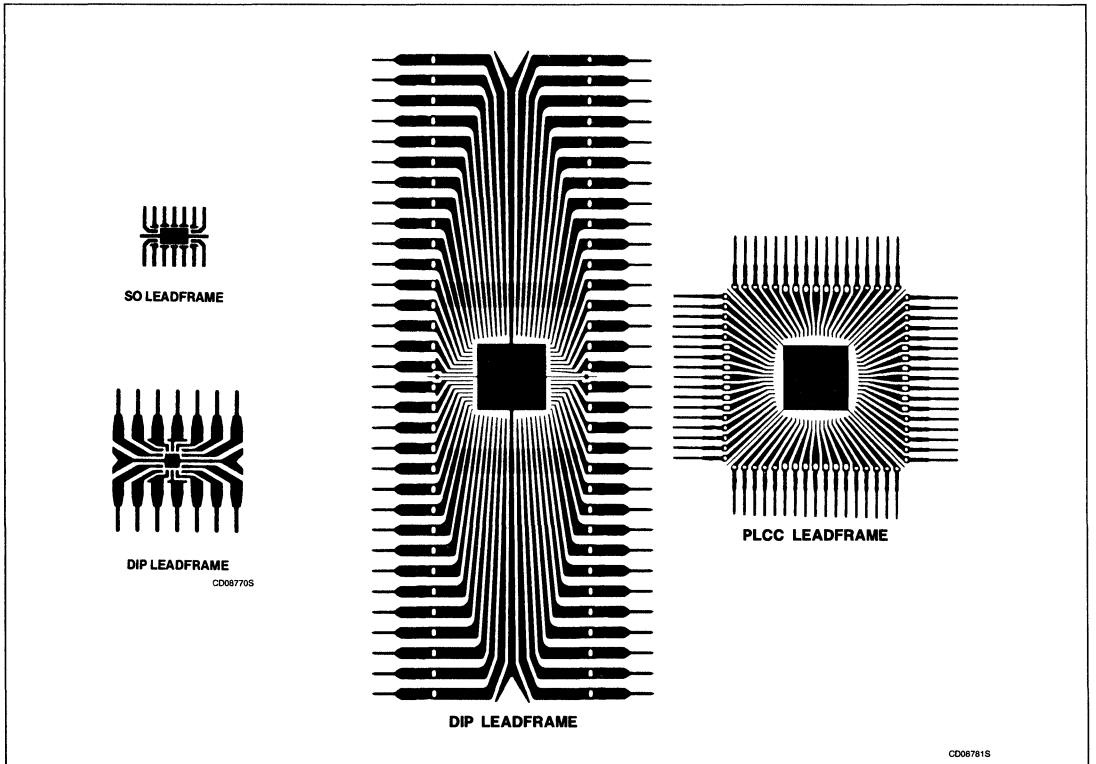
THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the



a. SO-14 Leadframe Compared to a 14-Pin DIP Leadframe

b. PLCC-68 Leadframe Compared to a 64-Pin DIP Leadframe

Figure 1

Thermal Considerations for Surface-Mounted Devices

substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and, to a lesser extent, other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally-conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years, the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However, three to five years ago the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package.

Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die-size, die-attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small it makes the difference insignificant.

Gold-wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller than in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards. It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts, or compositions may give different results from this data. Each SMD user should compare his system to the Signetics test system and determine if the data is appropriate or needs adjustment for his application.

Test Method

Signetics uses what is commonly called the TSP (temperature-sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant-temperature oil bath and constant-current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating; data given here used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}} \Bigg|\ I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

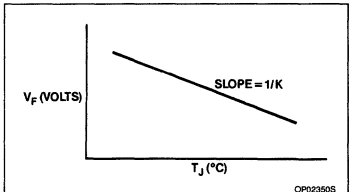


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

9

Thermal Considerations for Surface-Mounted Devices

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K(V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)

V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)

V_H = Heating Voltage (V)

I_H = Heating Current (A)

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size — SO Small
1.12″ × 0.75″ × 0.059″
— SO Large:
1.58″ × 0.75″ × 0.059″
— PLCC:
2.24″ × 2.24″ × 0.062″

Board Material — Glass epoxy, FR-4 type with 1oz. sq.ft. copper solder coated

Board Trace Configuration — See Figure 3.

SO devices are set at 8 – 9mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 – 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board, and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still-air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air-flow tests were run in a 4″ × 4″ cross-section by 26″ long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16″ stand-off. Figure 6 shows the air-flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water-cooled block approximately 4″ × 7″ × 0.75″) to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040″ diameter sheath, grounded junction type K) mounted flush with heat-sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook-up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

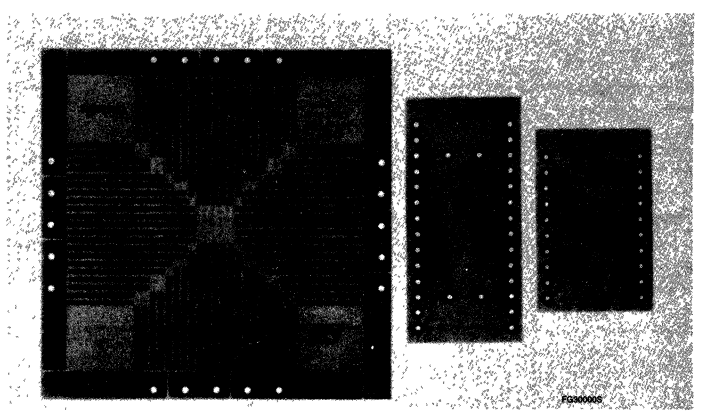


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

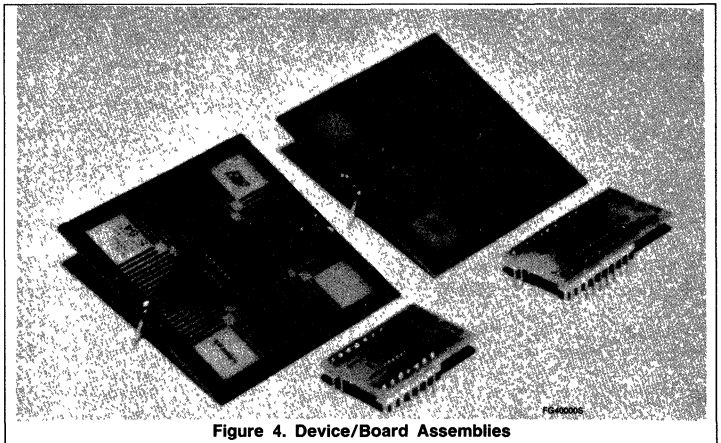


Figure 4. Device/Board Assemblies

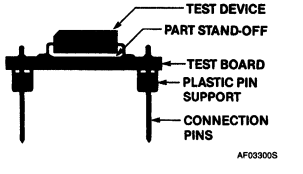
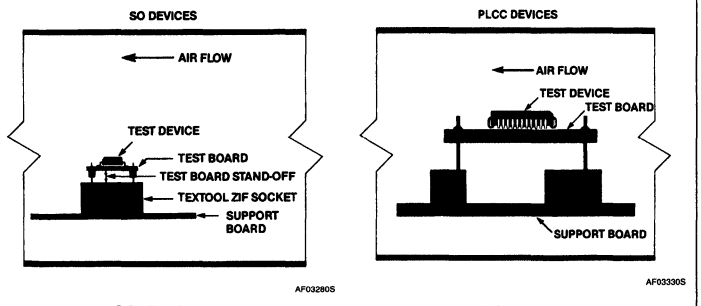


Figure 5. Cross-Section of Test Device Soldered to Test Board

Thermal Considerations for Surface-Mounted Devices



SO Devices PLCC Devices

Figure 6. Air-Flow Test Setup

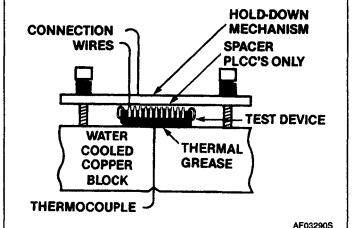


Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)

θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)

P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)

T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air-flow ambients. Given $T_A = 30°C$,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data — SOL-20 graph.

   Answer: 88°C/W @ 0.7W

2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.

   Percent change in Power

   $$= \frac{0.5W - 0.7W}{0.7W} \times 100$$

   $$= -28.6\%$$

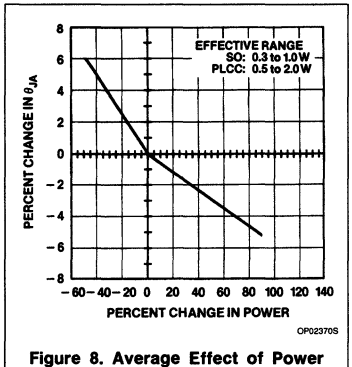


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

From Figure 8:
28.6% change in power gives
3.5% increase in θ_{JA}

Answer:
88°C/W + (88 × 0.035)
= 91°C/W @ 0.5W

3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.

From Figure 9: 200 LFPM air flow gives 14% decrease in θ_{JA}

Answer:
91°C/W - (91 × 0.14) = 78°C/W

4. Calculate approximate junction temperature

Answer:
T_J (still-air)
= (91°C/W × 0.5W) + 30
= 76°C
T_J (200 LFPM)
= (78°C/W × 0.5W) + 30
= 69°C

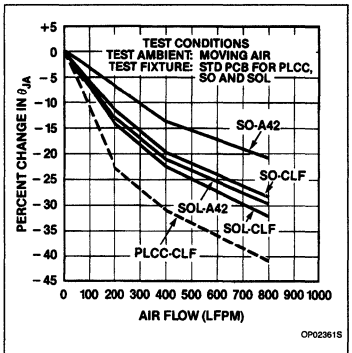
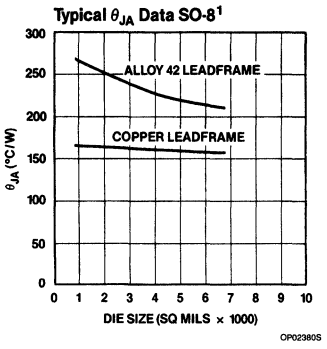
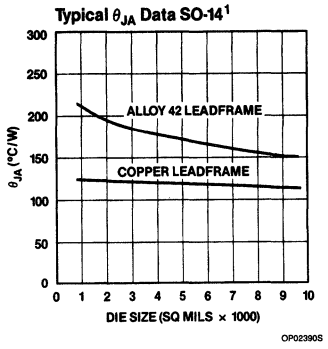
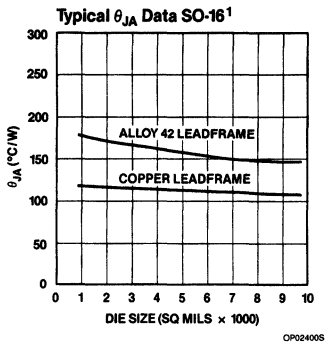


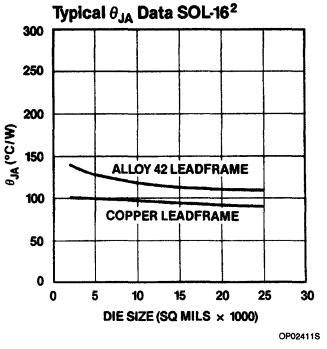
Figure 9. Average Effect of Air Flow on SMD θ_{JA}

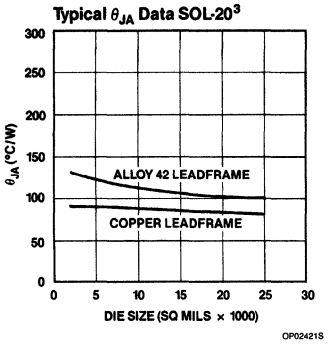
Thermal Considerations for Surface-Mounted Devices

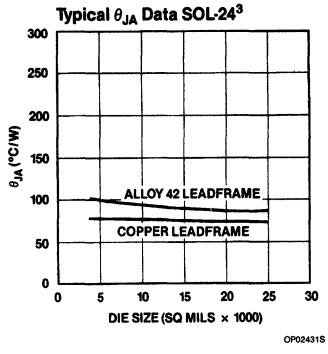


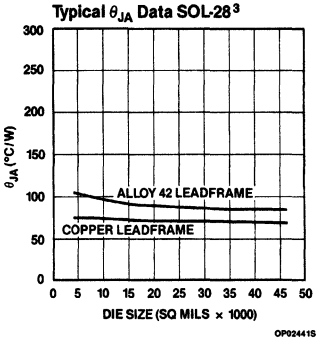












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation·	0.5W
Test fixture·	Philips PCB (1 12″ × 0 75″ × 0 059″)
Accuracy	±15%

2. TEST CONDITIONS:

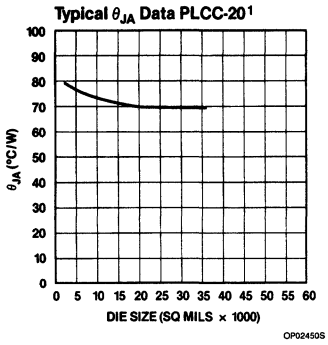
Test ambient.	Still air
Power dissipation:	0 5W
Test fixture.	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy.	±15%

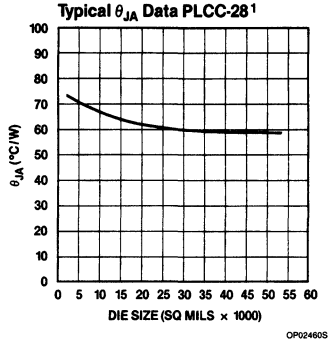
3. TEST CONDITIONS:

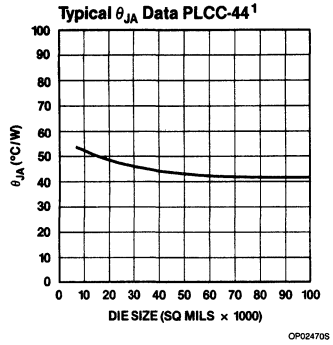
Test ambient.	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0 059″)
Accuracy	±15%

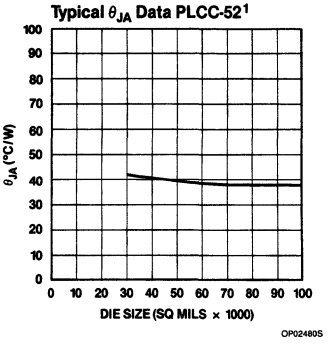
Figure 10. Typical SMD Thermal (θ_{JA}) Characteristics

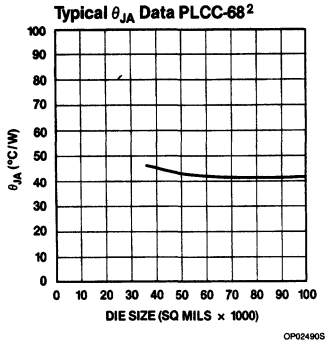
Thermal Considerations for Surface-Mounted Devices

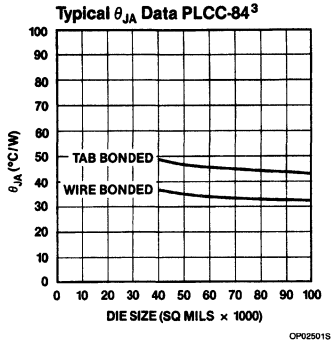












NOTES:

1. TEST CONDITIONS:

Test ambient·	Still air
Power dissipation·	0 75W
Test fixture·	Signetics PCB (2 24″ × 2 24″ × 0 062″)
Accuracy·	±15%

2. TEST CONDITIONS:

Test ambient	Still air
Power dissipation	1 0W
Test fixture	Signetics PCB (2 24″ × 2.24″ × 0 062″)
Accuracy.	±15%

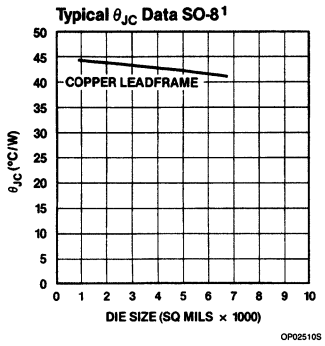
3. TEST CONDITIONS:

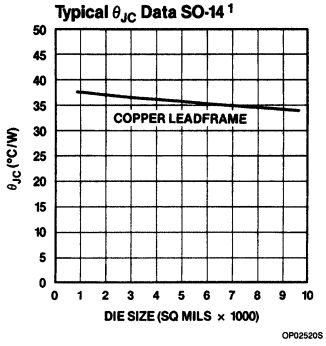
Test ambient	Still air
Power dissipation	1 5W
Test fixture	Signetics PCB (2 24″ × 2 24″ × 0 062″)
Accuracy.	±15%

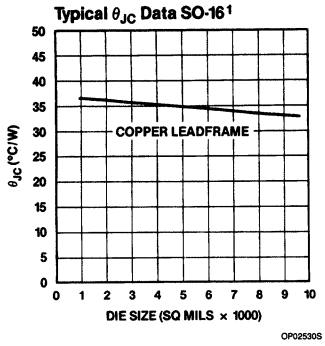
Figure 11. Typical SMD Thermal (θ_{JA}) Characteristics

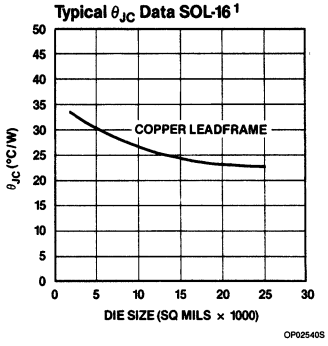
9

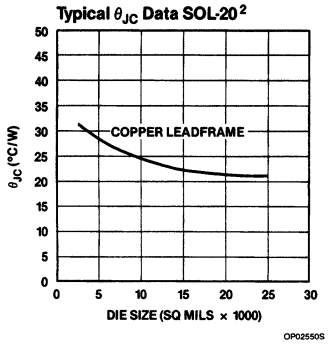
Thermal Considerations for Surface-Mounted Devices

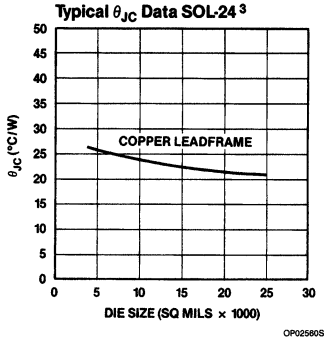


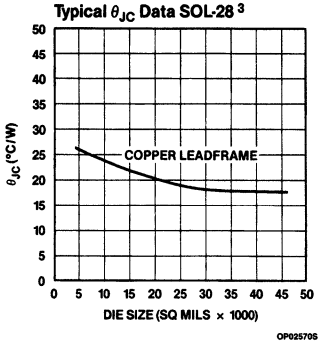












NOTES:

1. TEST CONDITIONS:

Power dissipation	0 5W
Test fixture.	"Infinite" heat sink
Accuracy·	± 15%

2. TEST CONDITIONS:

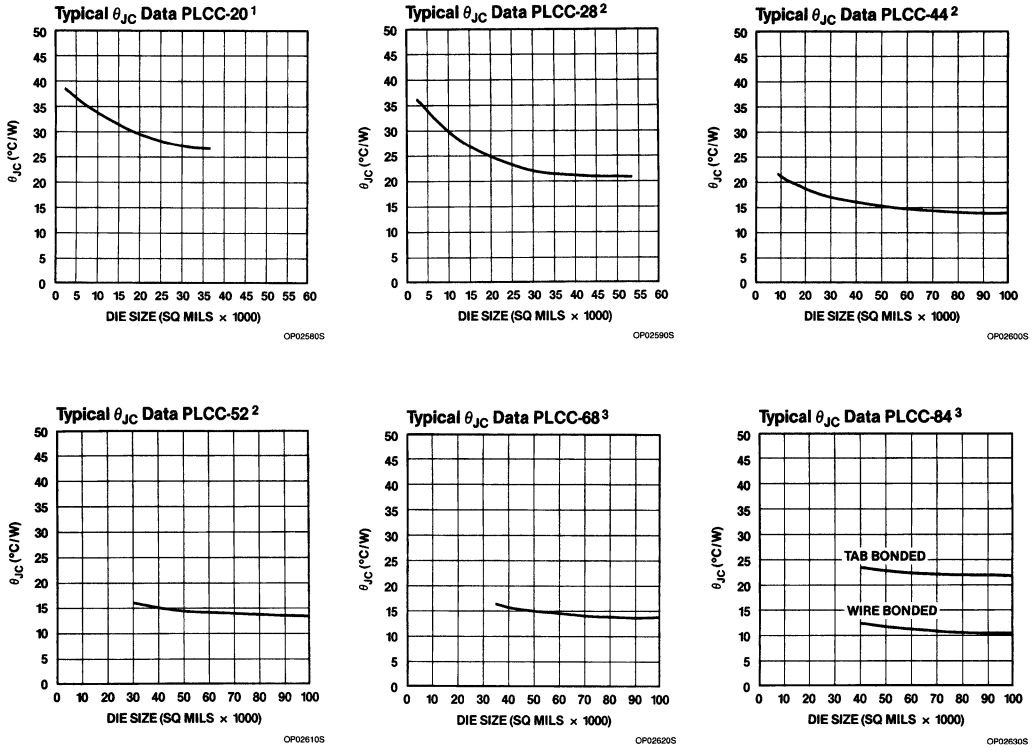
Power dissipation·	0 7W
Test fixture	"Infinite" heat sink
Accuracy	± 15%

3. TEST CONDITIONS:

Power dissipation.	1 0W
Test fixture	"Infinite" heat sink
Accuracy	± 15%

Figure 12. Typical SMD Thermal (θ_{JC}) Characteristics

Thermal Considerations for Surface-Mounted Devices



NOTES:

1. TEST CONDITIONS:

Power dissipation	0 75W
Test fixture	"Infinite" heat sink
Accuracy	±15%

2. TEST CONDITIONS:

Power dissipation	1 0W
Test fixture	"infinite" heat sink
Accuracy	±15%

3. TEST CONDITIONS:

Power dissipation	2 0W
Test fixture	"Infinite" heat sink
Accuracy	±15%

Figure 13. Typical SMD Thermal (θ_{JC}) Characteristics

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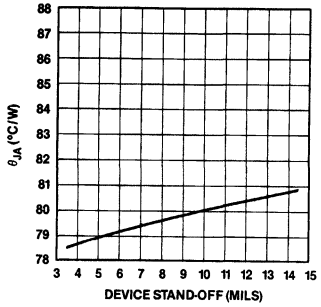
Thermal Considerations for Surface-Mounted Devices

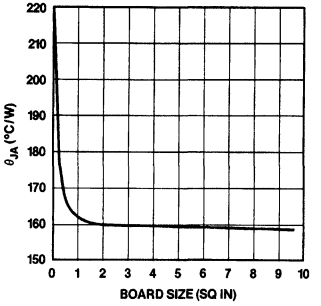
Effect of Device Stand-Off on SO θ_{JA} [1]



NOTES:
1. TEST CONDITIONS

Package type	SOL-20 CLF
Die size	11,322sq mils
Test Ambient	Still-air
Power dissipation	0 75W
Test fixture	Phillips PCB (1 58" × 0 75" × 0 059")

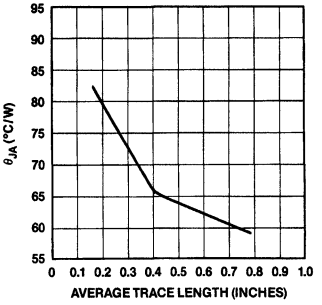
Effect of Board Size on SO θ_{JA} [2]



NOTES:
2. TEST CONDITIONS

Package type	SOL-14 CLF
Die size	5,040sq mils
Test Ambient	Still-air
Power dissipation	0 6W
Test fixture	0 062" thick PCB with "no traces" 8 – 9mil stand-off

Effect of Trace Length on 28-Lead PLCC θ_{JA} [3]



NOTES:
3. TEST CONDITIONS

Package type	PLCC-28 CLF
Die size	10,445sq mils
Test Ambient	Still-air
Power dissipation.	1 0W
Test fixture	Signetics PCB (2 24" × 2 24" × 0 062") trace 27mil-wide 1oz sq ft copper

Figure 14

Thermal Considerations for Surface-Mounted Devices

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations, and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection-molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a surface-mounted assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduce the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

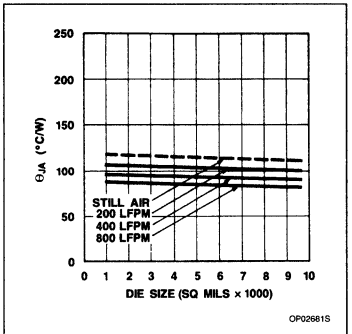


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

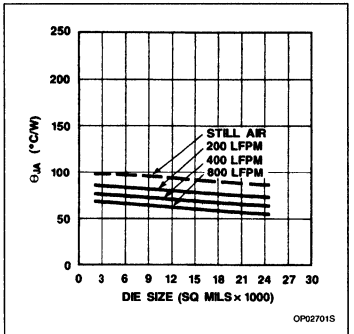


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

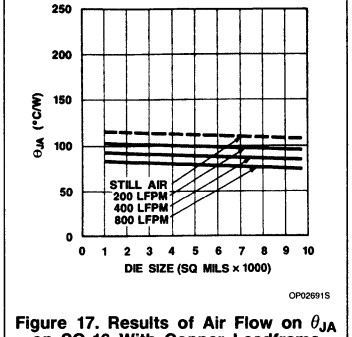


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

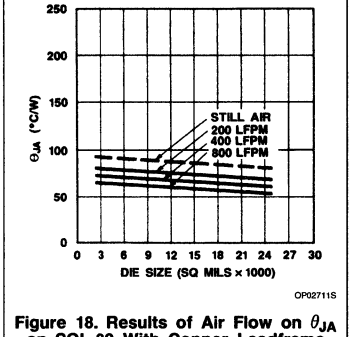


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be set up in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/°C soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/°C. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

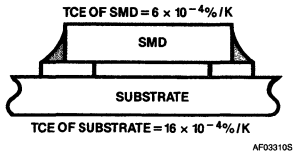
The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, is normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses set up in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its

Thermal Considerations for Surface-Mounted Devices

most critical in applications requiring large LCCCs with high pin counts.



NOTE:
Data provided by N V. Philips

Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL, and PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e., SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO, can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metallic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate, can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar®or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed, in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability, and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates, however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates, traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely-used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 $\times$ 10^{-6}/°C. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill, and is prone to resin microcracking and water absorption.

Polyimide quartz substrates have a TCE between 6 and 12, making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

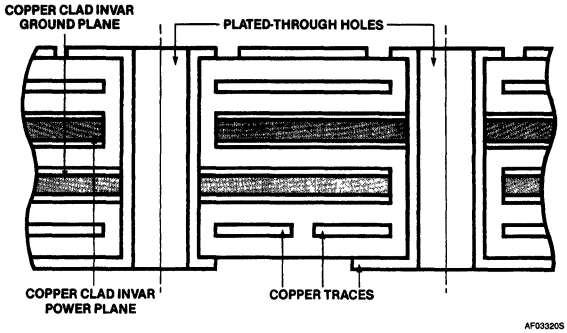
Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate,

Thermal Considerations for Surface-Mounted Devices

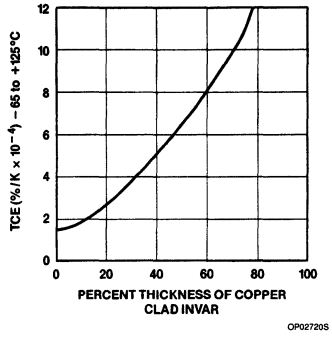
making it possible to mount LCCCs with confidence.

Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness and shows the TCE range of each of several other materials to which the clad material can be matched. For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.



NOTE:
Data provided by N.V Philips

Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-Clad Invar Ground and Power Planes, Interconnected via Plated-Through Holes



NOTE:
Data provided by N V Philips

Figure 21. The TCE Range of Copper-Clad Invar as a Function of Copper Thickness

9

Thermal Considerations for Surface-Mounted Devices

Table 1. Substrate Material Properties

SUBSTRATE MATERIAL	TCE (10^{-6}/°C)	THERMAL CONDUCTIVITY (W/m^{3}K)
Glass-epoxy (FR-4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper-clad Invar	6.4 (typical)	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material
Data provided by N V Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS

CONCLUSION

Thermal management remains a major concern of producers and users of ICs The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart . . . even with copper leadframes. That is the major trade-off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

Package Outlines
For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC

INTRODUCTION
The following information applies to all packages unless otherwise specified on individual package outline drawings.

GENERAL
1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120mils square die for plastic packages and a 90mils square die in the smallest available cavity for hermetic packages. All units were solder-mounted to PC boards, with standard stand-off, for measurement.

PLASTIC ONLY
5. Lead material: Alloy 42 (Nickel/Iron Alloy), Olin 194 (Copper Alloy), or equivalents, solder-dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO packages/microminiature packages:
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

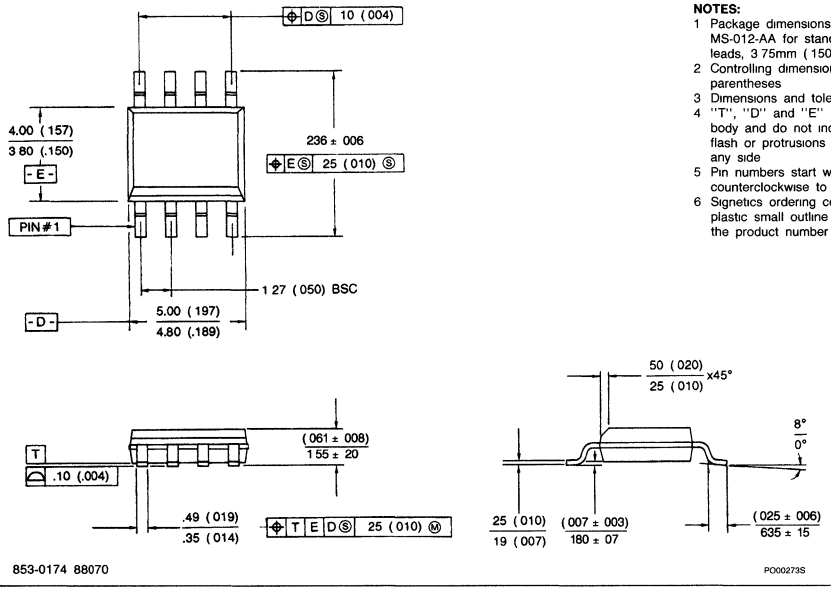
HERMETIC ONLY
10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated, tin-plated, or solder-dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent — tin-plated, gold-plated or solder-dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent — gold- or tin-plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel- or tin-plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold-plated, alloy seal.
    d. BeO ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb 0.010 inches.
16. Maximum glass climb or lid skew is 0.010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

PLASTIC PACKAGES

DESCRIPTION	PACKAGE CODE	θ_{JA}/θ_{JC} (°C/W)	PACKAGE TYPE
Standard Dual-in-Line Packages			
8-Pin	N	110/49	
14-Pin	N	90/46	TO-116/MO-001
16-Pin	N	90/46	MO-001
18-Pin	N	79/36	
20-Pin	N	79/35	
22-Pin	N	56/23	
24-Pin	N	58/30	MO-015
28-Pin	N	56/30	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO-5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	162/26	Dual-in-Line Ceramic
14-Pin	F	109/26	Dual-in-Line Ceramic
16-Pin	F	105/26	Dual-in-Line Ceramic
18-Pin	F	88/22	Dual-in-Line Ceramic
20-Pin	F	85/22	Dual-in-Line Ceramic
22-Pin	F	75/13	Dual-in-Line Ceramic
24-Pin	F	65/16	Dual-in-Line Ceramic
28-Pin	F	62/16	Dual-in-Line Ceramic
Laminated Ceramic, Side-Brazed Lead			
16-Pin	I	90/25	DIP Laminate

8-PIN PLASTIC SO (D PACKAGE)

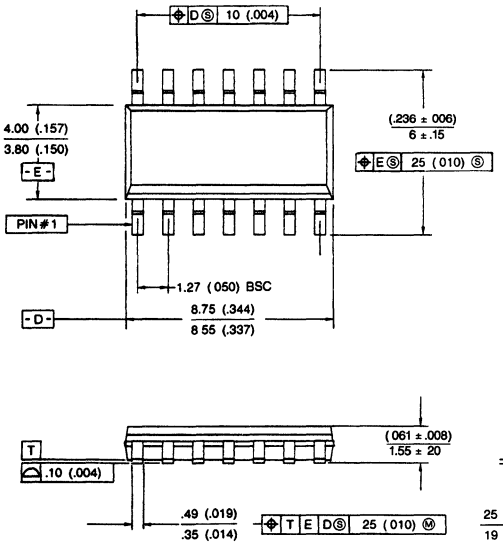


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

853-0174 88070

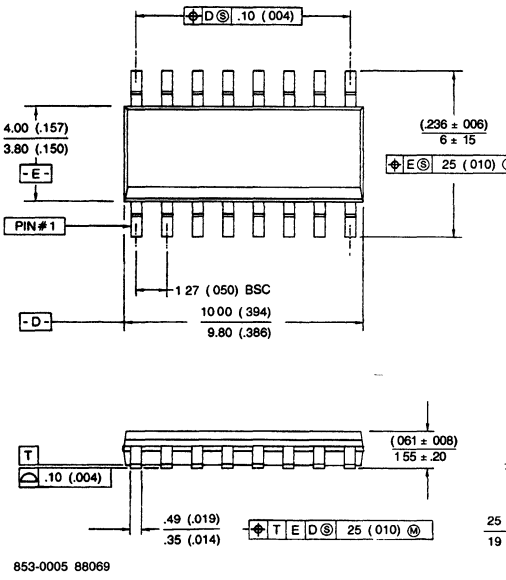
PO00273S

14-PIN PLASTIC SO (D PACKAGE)



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3 75mm (.150") body width (issue A, June 1985)
2. Controlling dimensions are in mm Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14 5M- 1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

16-PIN PLASTIC SO (D PACKAGE)

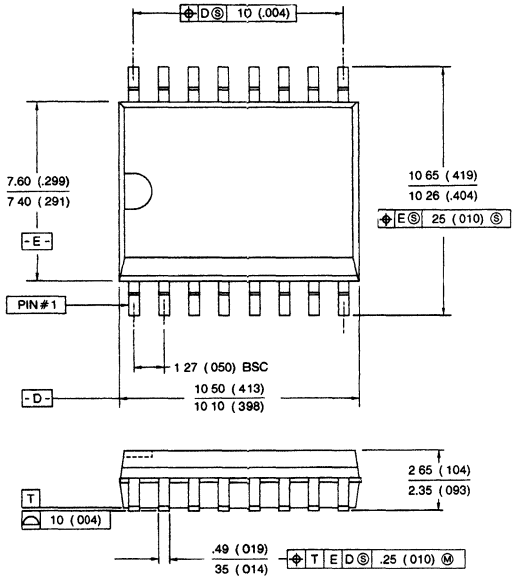


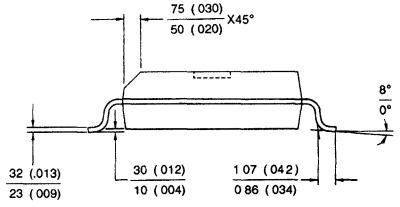
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3 75mm (.150") body width (issue A, June 1985)
2. Controlling dimensions are in mm Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14 5M- 1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

9

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

16-PIN PLASTIC SOL (D PACKAGE)



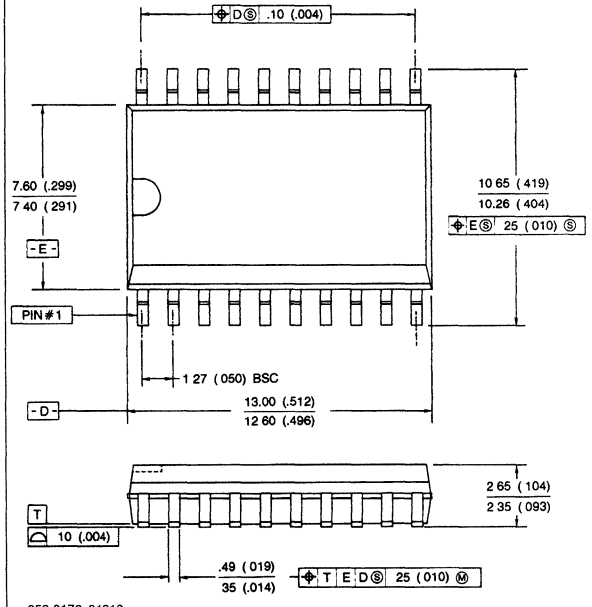


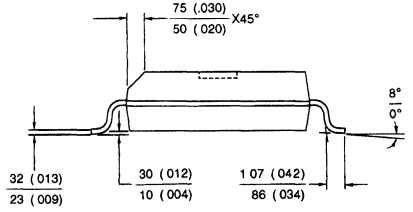
853-0171 81218

PO00241S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (Issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

20-PIN PLASTIC SOL (D PACKAGE)





853-0172 81219

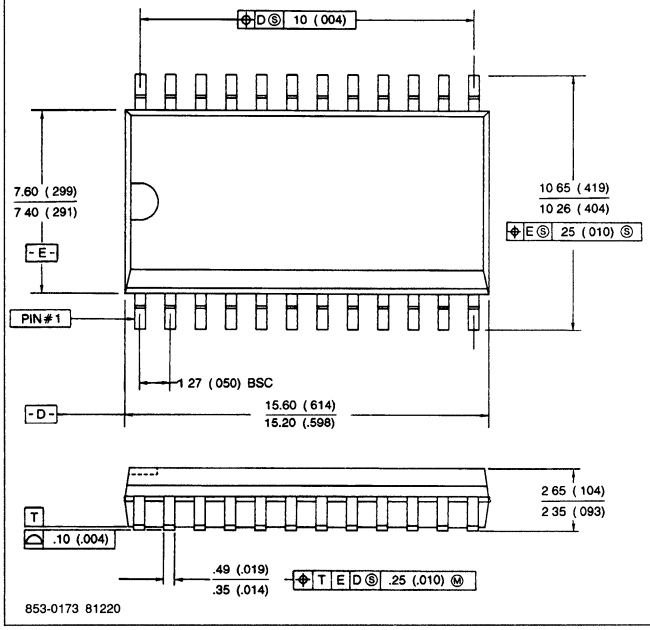
PO00231S

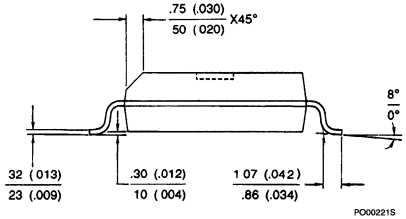
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (Issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC

Package Outlines

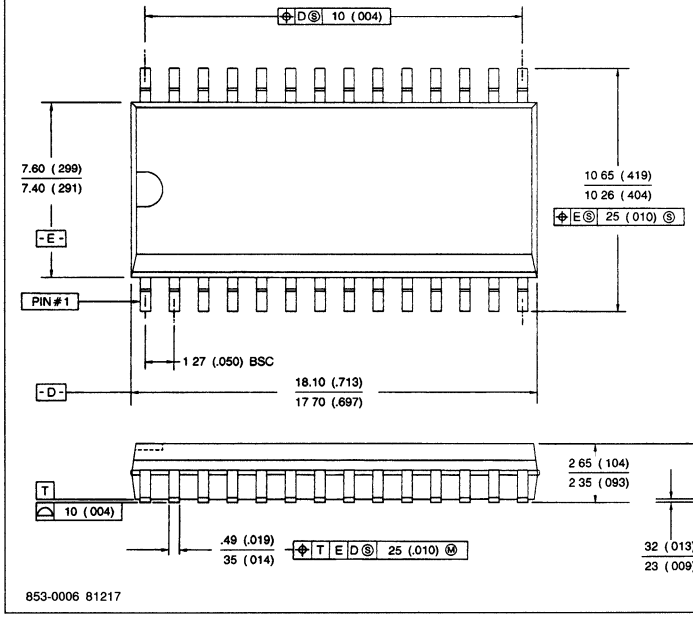
24-PIN PLASTIC SOL (D PACKAGE)

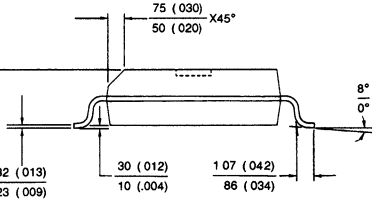




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

28-PIN PLASTIC SOL (D PACKAGE)

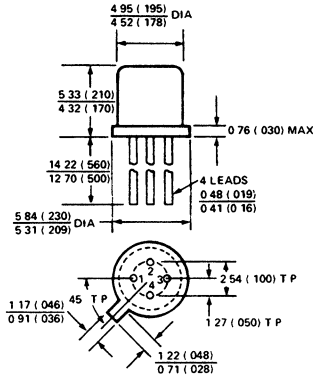




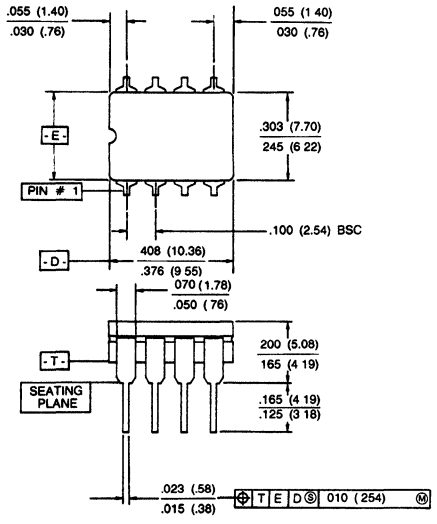
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

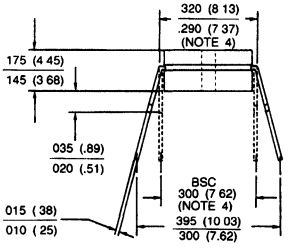
4-PIN HERMETIC TO-72 HEADER (E PACKAGE)



8-PIN CERDIP (FE PACKAGE)



NOTES:
1. Controlling dimension inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.



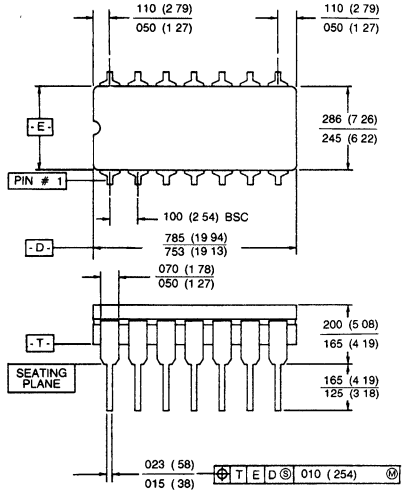
853-0580 81594

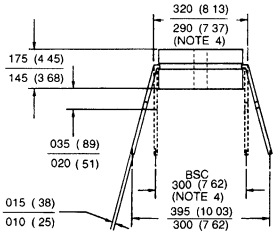
PO00480S

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC

Package Outlines

14-PIN CERDIP (F PACKAGE)



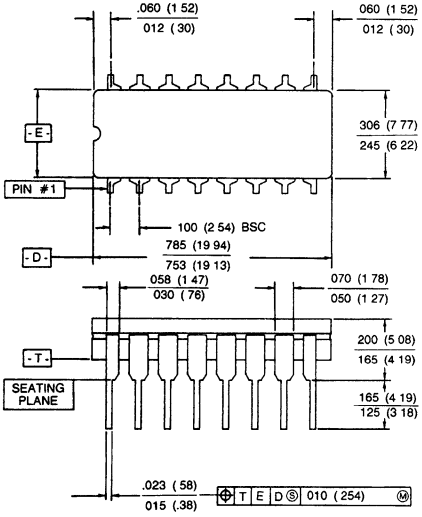


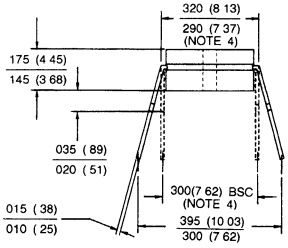
NOTES:
1. Controlling dimension inches Millimeters are shown in parentheses
2. Dimensions and tolerancing per ANSI Y14 5M – 1982
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch
4. These dimensions measured with the leads constrained to be perpendicular to plane T
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top

853-0581 81594

PO00440S

16-PIN CERDIP (F PACKAGE)





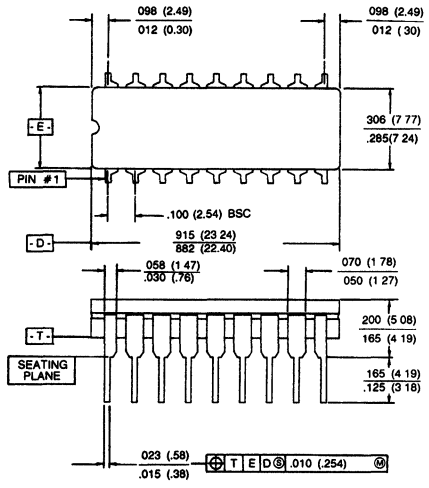
NOTES:
1. Controlling dimension inches Millimeters are shown in parentheses
2. Dimensions and tolerancing per ANSI Y14 5M – 1982
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch
4. These dimensions measured with the leads constrained to be perpendicular to plane T
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top

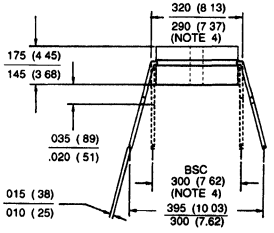
853-0582 81594

PO00490S

9

18-PIN CERDIP (F PACKAGE)



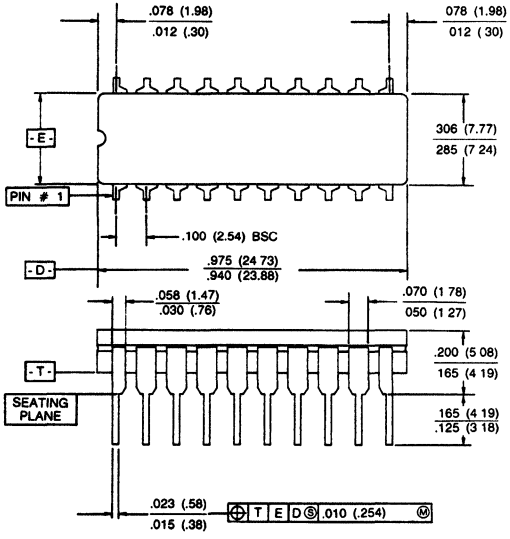


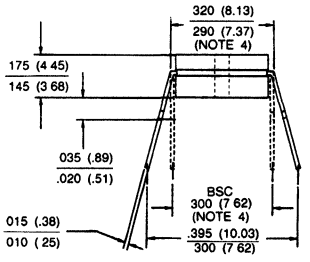
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

853-0583 81594

PO00470S

20-PIN CERDIP (F PACKAGE)



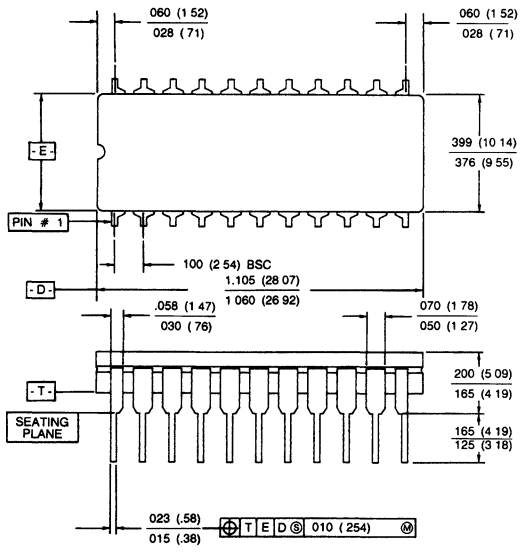


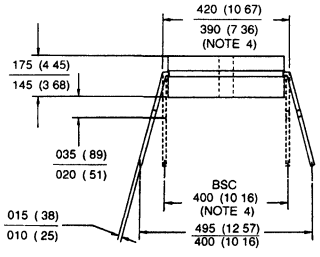
NOTES:
1 Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3 "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4 These dimensions measured with the leads constrained to be perpendicular to plane T.
5 Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0584 81594

PO00430S

22-PIN CERDIP (F PACKAGE)



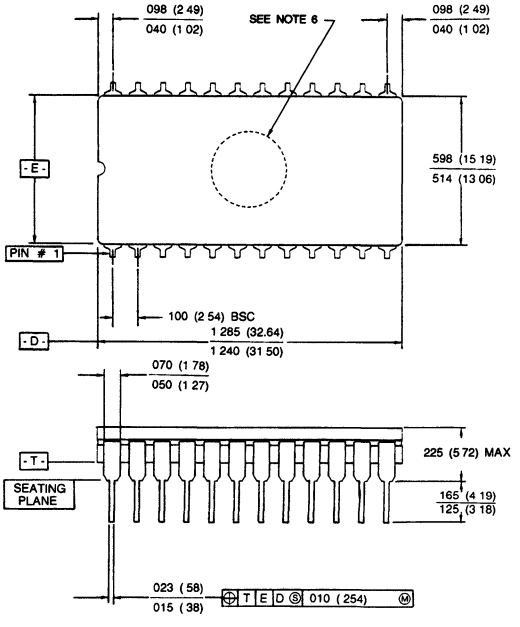


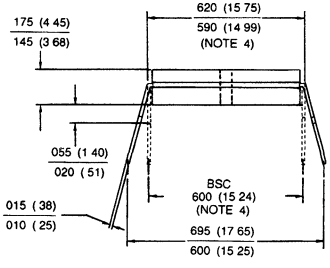
NOTES:
1. Controlling dimension inches Millimeters are shown in parentheses
2. Dimensions and tolerancing per ANSI Y14 5M – 1982
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch
4. These dimensions measured with the leads constrained to be perpendicular to plane T
5. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top

853-0585 81594

PO00420S

24-PIN CERDIP (F PACKAGE)





NOTES:
1 Controlling dimension inches Millimeters are shown in parentheses
2 Dimensions and tolerancing per ANSI Y14 5M – 1982
3 "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch
4 These dimensions measured with the leads constrained to be perpendicular to plane T
5 Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top

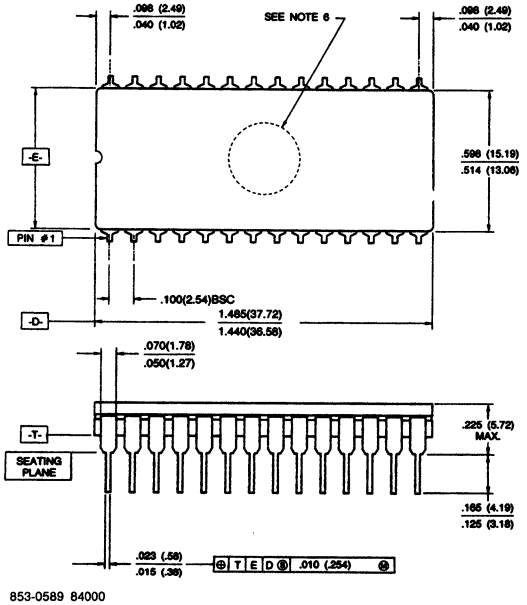
853-0588 84221

PO00464S

9

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

28-PIN CERDIP (F PACKAGE)

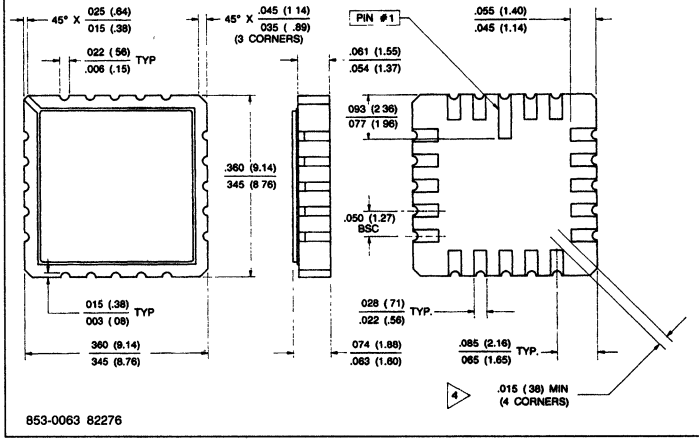


853-0589 84000

PO00660S

NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14 5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch
4 These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM Products.

20-PIN PGA (G PACKAGE)

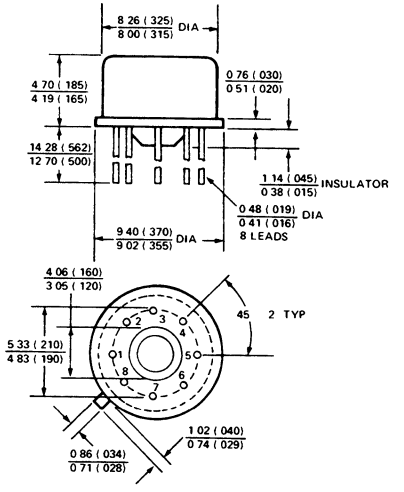


853-0063 82276

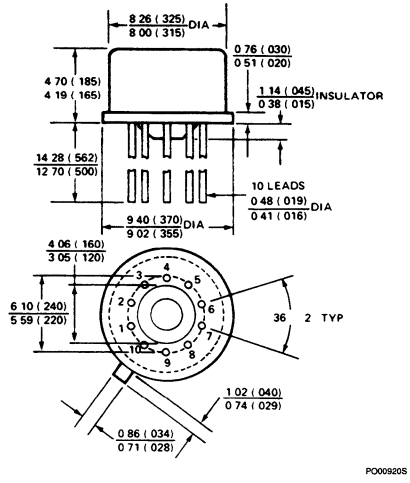
PO00870S

NOTES:
1 Package dimensions conform to Mil-M-38510, outline NO. C - 2, 20 leads, square ceramic leadless chip carrier.
2. Controlling dimension. inches, millimeters are shown in parenthesis.
3. Dimension and tolerancing per ANSI Y14 5M - 1982.
4. This dimension represents the minimum spacing between the corner contact pads These corner pads may have a .020 inch by 45 degree maximum chamfer to accomplish the 015 minimum spacing
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top
6 Signetics order code for product packaged in a CCCL is the suffix "G" after the product number.

8-PIN HERMETIC TO-5 HEADER (H PACKAGE)

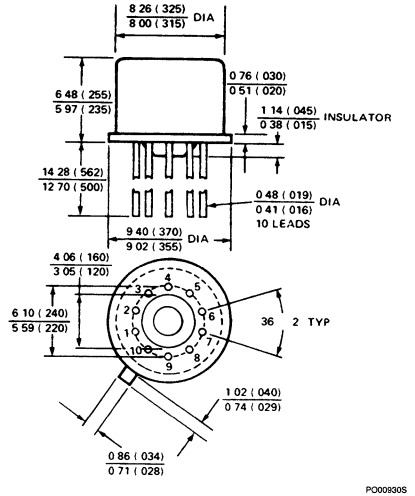


10-PIN HERMETIC TO-5/100 HEADER SHORT CAN (H PACKAGE)

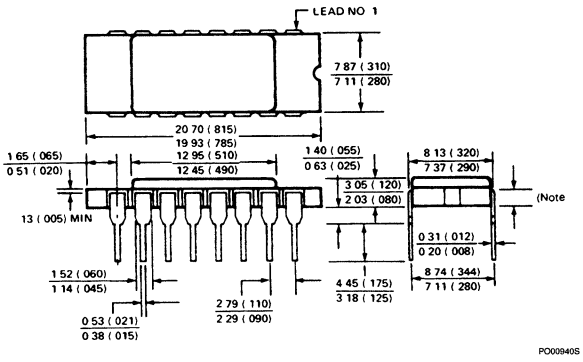


9

10-PIN HERMETIC TO-5/100 HEADER TALL CAN (H PACKAGE)

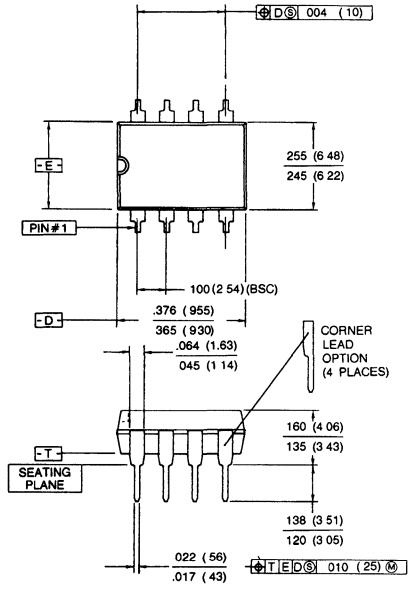


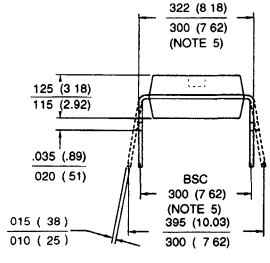
16-PIN HERMETIC SDIP (I PACKAGE)



For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

8-PIN PLASTIC PDIP (N PACKAGE)



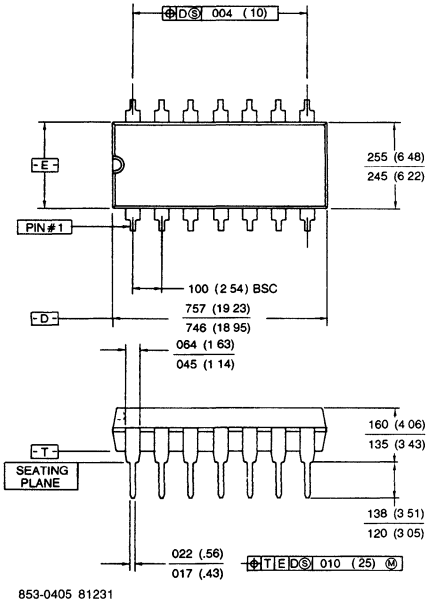


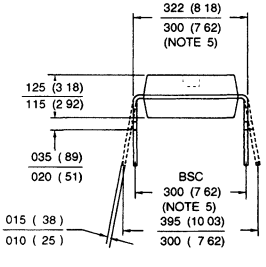
NOTES:
1. Controlling dimension inches Metric are shown in parentheses
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package 300 inch row spacing (PLASTIC) 8 leads (issue B 7/85)
3. Dimensions and tolerancing per ANSI Y14 5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 010 inch (25mm) on any side
5. These dimensions measured with the leads constrained to be perpendicular to plane T
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top

853-0404 81230

PO00312S

14-PIN PLASTIC DIP (N PACKAGE)





NOTES:
1. Controlling dimension inches Metric are shown in parentheses
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package 300 inch row spacing (PLASTIC) 14 leads (issue B 7/85)
3. Dimensions and tolerancing per ANSI Y14 5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 010 inch (25mm) on any side
5. These dimensions measured with the leads constrained to be perpendicular to plane T
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top

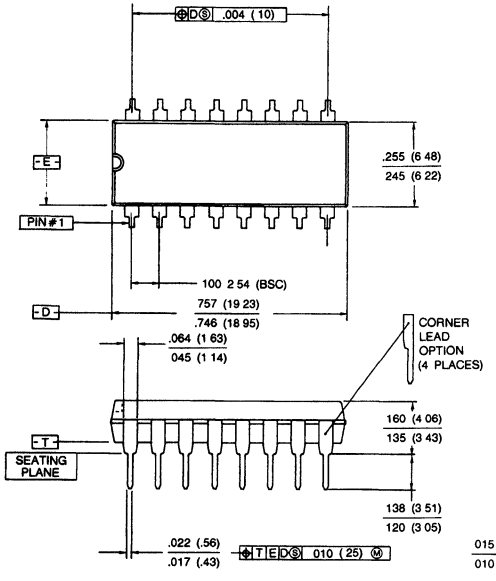
853-0405 81231

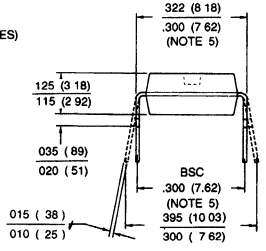
PO00330S

9

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

16-PIN PLASTIC DIP (N PACKAGE)

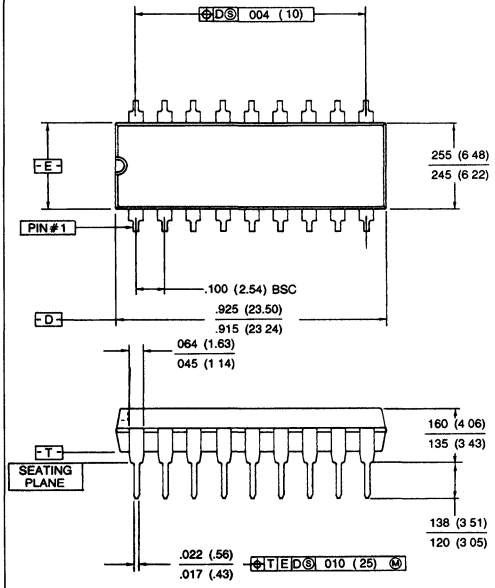


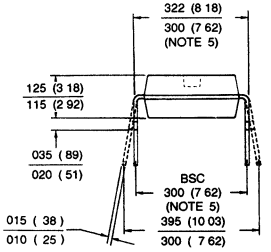


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B, 7/85)
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side
5. These dimensions measured with the leads constrained to be perpendicular to plane T
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top

853-0406 81232 PO00280S

18-PIN PLASTIC DIP (N PACKAGE)



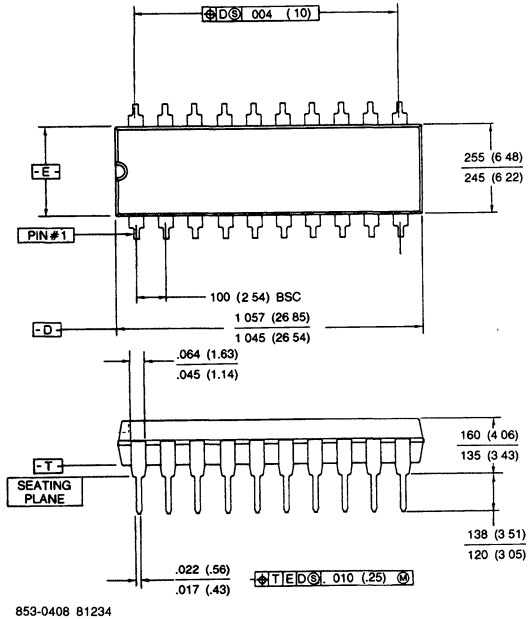


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses
2. Package dimensions conform to JEDEC specification MS-001-AD for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B, 7/85)
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side
5. These dimensions measured with the leads constrained to be perpendicular to plane T
6. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top

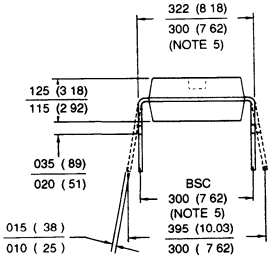
853-0407 81233 PO00300S

For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

20-PIN PLASTIC DIP (N PACKAGE)



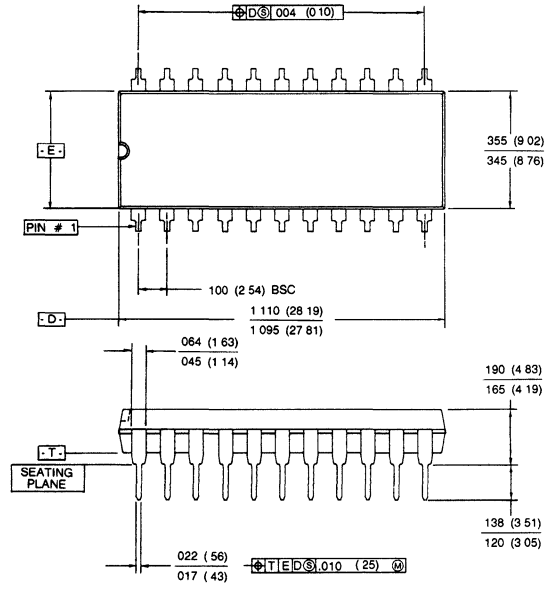
NOTES:
1 Controlling dimension inches Metric are shown in parentheses
2 Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package 300 inch row spacing (PLASTIC) 20 leads (issue B 7/85)
3 Dimensions and tolerancing per ANSI Y14 5M-1982
4 "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 010 inch (25mm) on any side
5 These dimensions measured with the leads constrained to be perpendicular to plane T
6 Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top



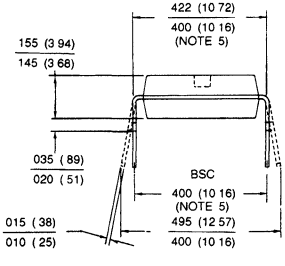
853-0408 81234

PO00290S

22-PIN PLASTIC DIP (N PACKAGE)



NOTES:
1 Controlling dimension inches Metric are shown in parentheses
2 Package dimensions conform to JEDEC specification MS-010-AA for standard dual in-line (DIP) package 400 inch row spacing (PLASTIC) 22 leads (issue A 7/85)
3 Dimensions and tolerancing per ANSI Y14 5M-1982
4 "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 010 inch (25mm) on any side
5 These dimensions measured with the leads constrained to be perpendicular to plane T
6 Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top



853-0409 81235

PO00341S

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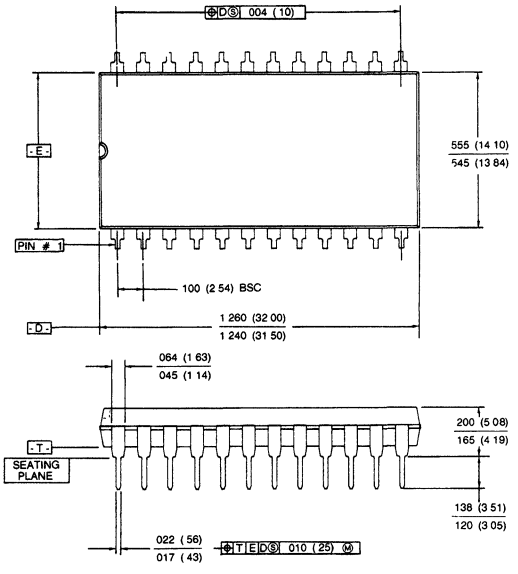
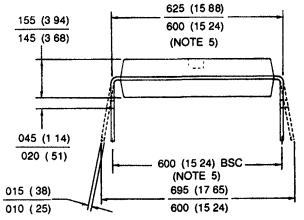
For Prefixes ADC, AM, AU, CA, DAC, ICM, LF, LM, MC, NE, SA, SE, SG, μA, UC — Package Outlines

24-PIN PLASTIC DIP (N PACKAGE)



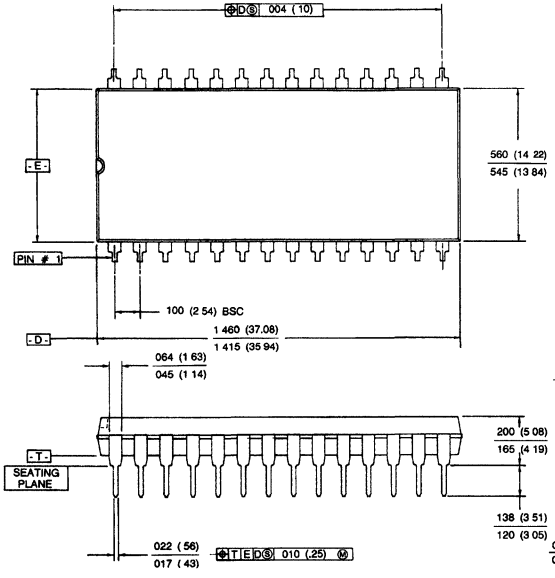


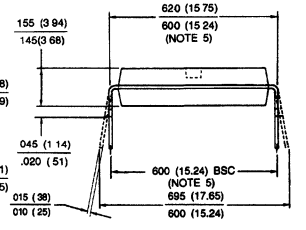
NOTES:
1. Controlling dimension· inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package 600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 010 inch (.25mm) on any side
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top

853-0412 81238

PO00361S

28-PIN PLASTIC DIP (N PACKAGE)





NOTES:
1. Controlling dimension inches Metric are shown in parentheses
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package 600 inch row spacing (PLASTIC) 28 leads (issue B 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 010 inch (.25mm) on any side
5. These dimensions measured with the leads constrained to be perpendicular to plane T
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top

853-0413 84099

PO00372S

Package Outlines
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

INTRODUCTION

Soldering

1. By hand
Apply the soldering iron below the seating plane (or not more than 2mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C, for not more than 5 seconds.

2. By dip or wave
The maximum permissible temperature of the solder is 260°C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints
The same precautions and limits apply as in (1) above.

SMALL OUTLINE (SO) PACKAGES

The Reflow Solder Technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230°C when a mild flux is used.

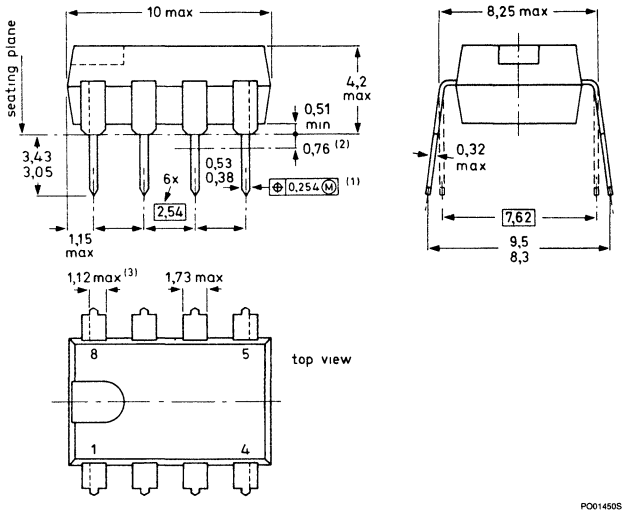
For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105μm is used for which the emulsion thickness should be about 50μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.

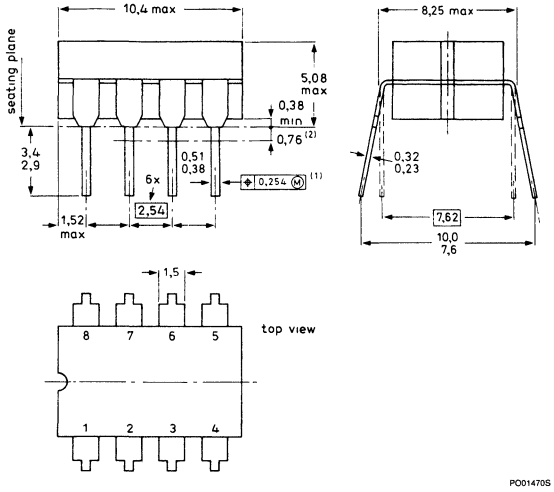
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

8-PIN PLASTIC (SOT-97A)



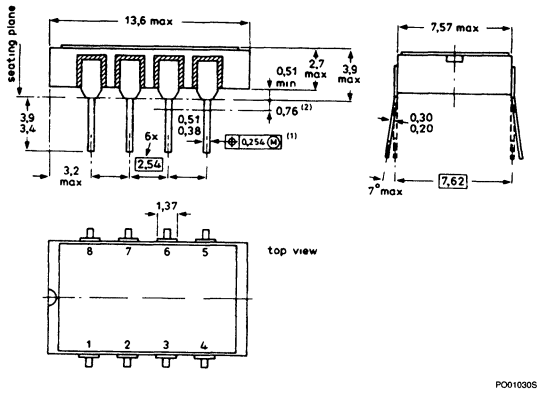
8-PIN CERDIP (SOT-151A)



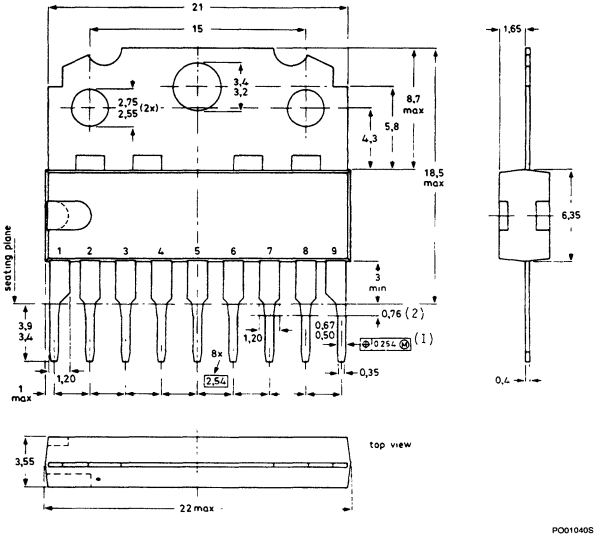
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

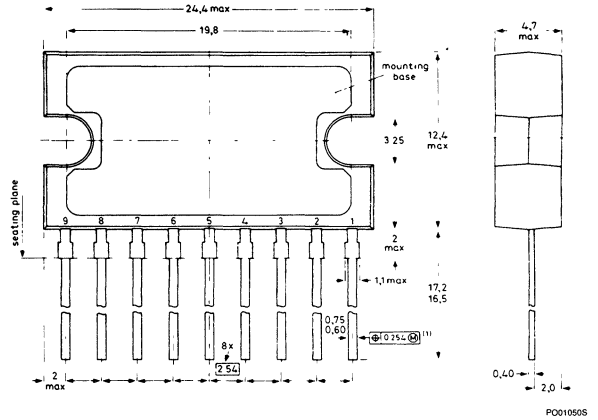
8-PIN METAL CERDIP (SOT-153B)



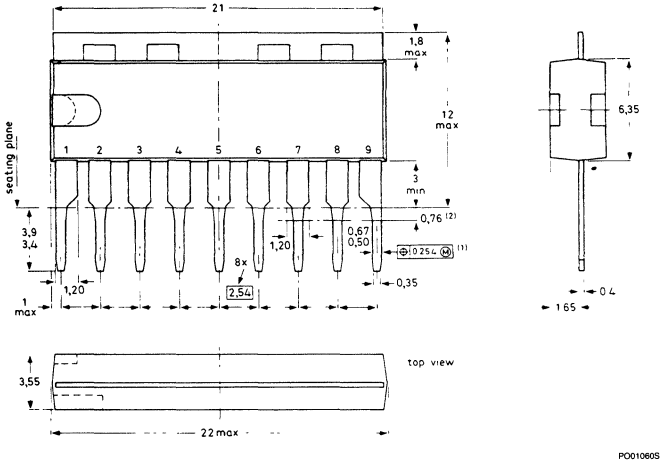
9-PIN PLASTIC SIP (SOT-110B)



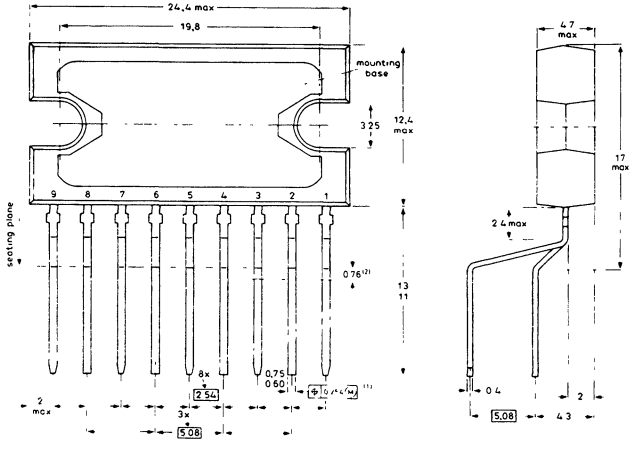
9-PIN PLASTIC POWER SIP (SOT-131A, B)



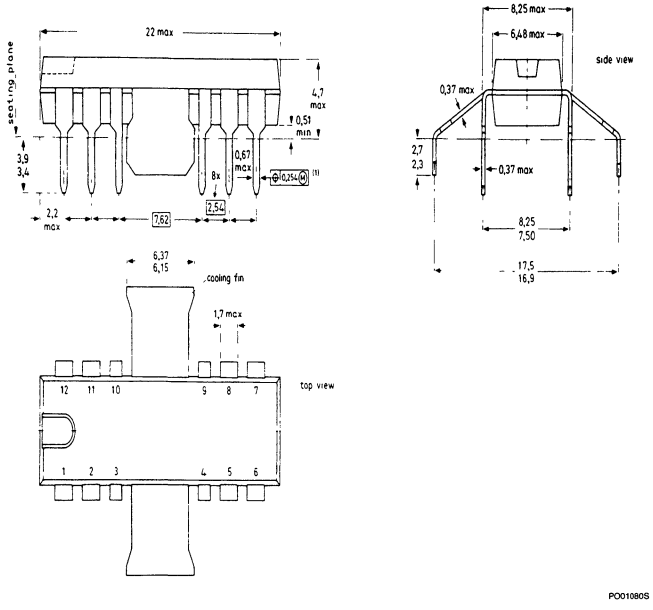
9-PIN PLASTIC SIP (SOT-142)



9-PIN PLASTIC POWER SIP-BENT-TO-DIP (SOT-157B)

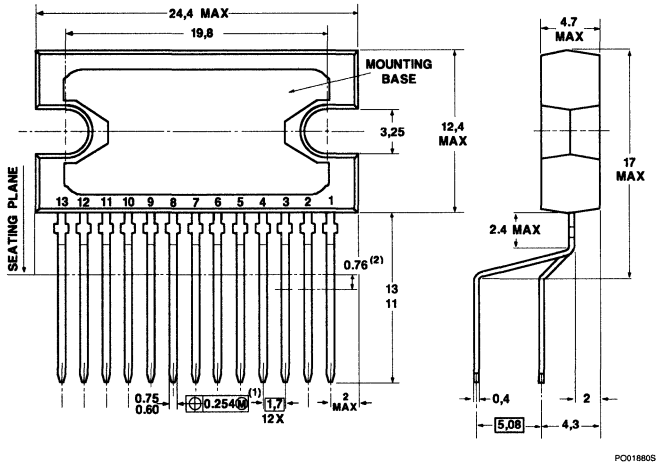


12-PIN PLASTIC DIP WITH METAL COOLING FIN (SOT-150)

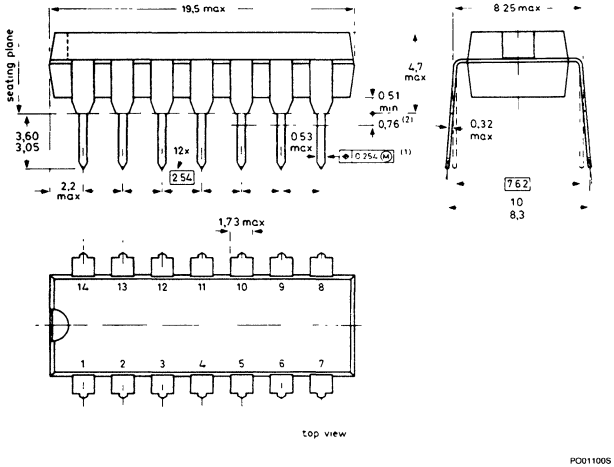


9

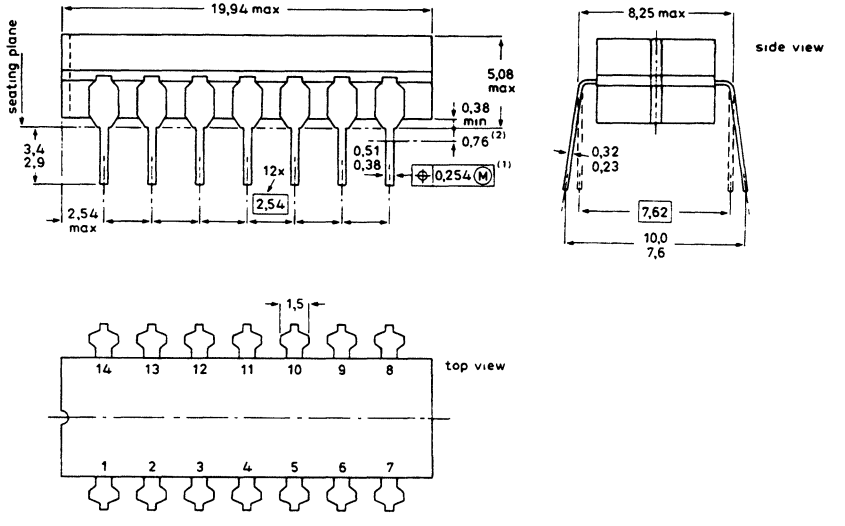
13-PIN PLASTIC POWER SIP-BENT-TO-DIP (SOT-141BA)



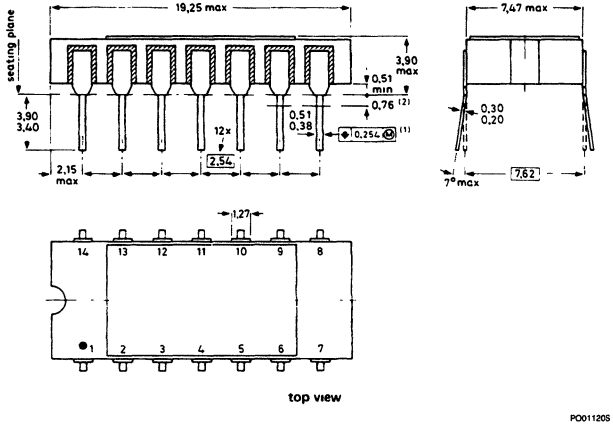
14-PIN PLASTIC DIP (SOT-27K, M, T)



14-PIN CERDIP (SOT-73A, B, C)



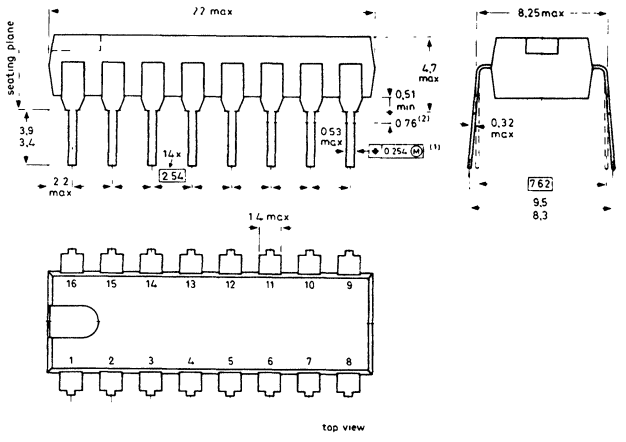
14-PIN METAL CERDIP (SOT-83B)



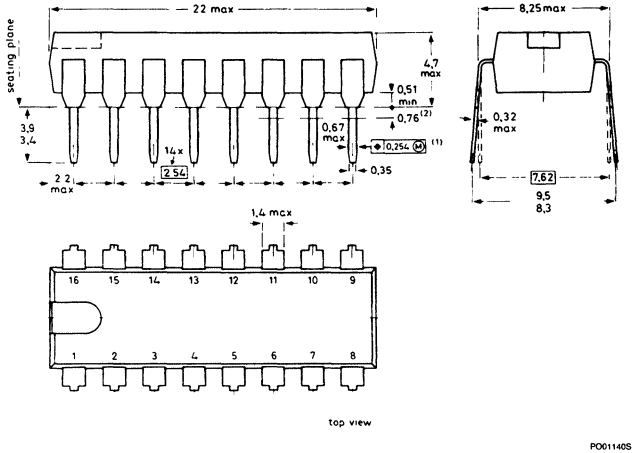
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

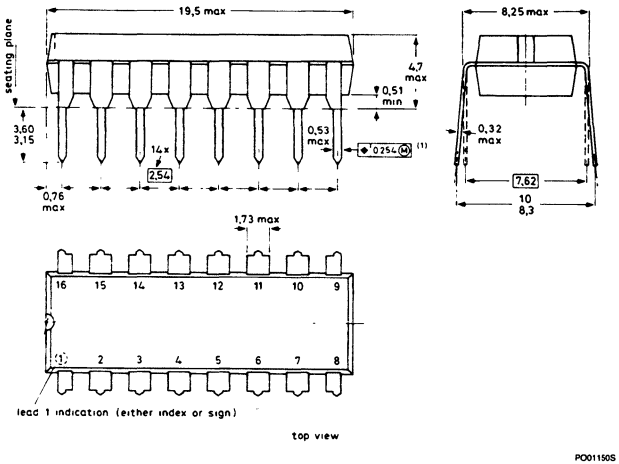
16-PIN PLASTIC DIP (SOT-38)



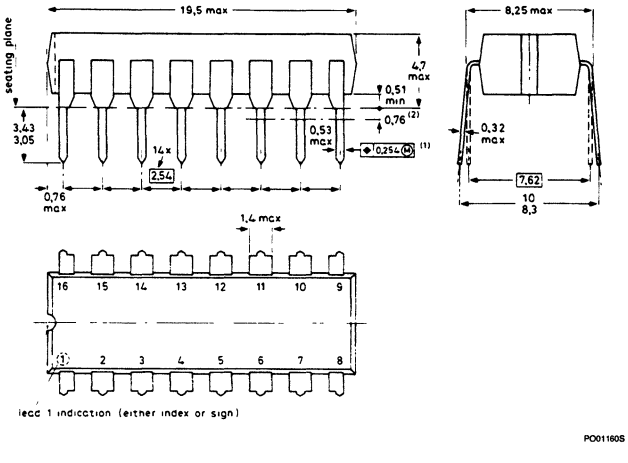
16-PIN PLASTIC DIP (SOT-38A)



16-PIN PLASTIC DIP (SOT-38D, DE)

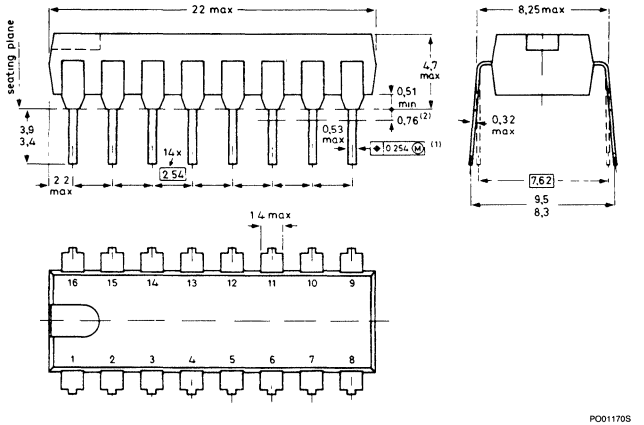


16-PIN PLASTIC DIP (SOT-38Z)

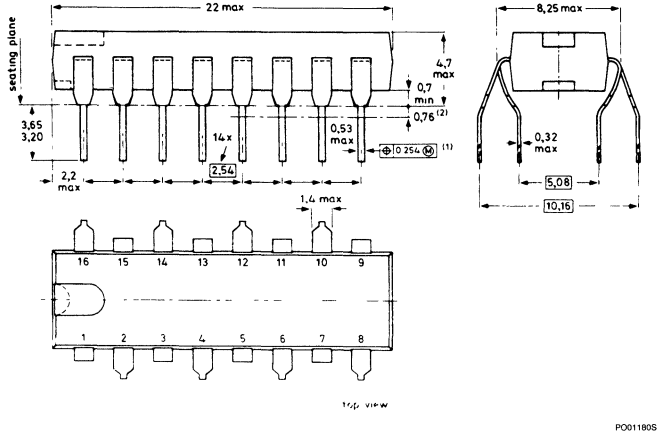


9

16-PIN PLASTIC DIP WITH INTERNAL HEAT SPREADER (SOT-38WE-2)



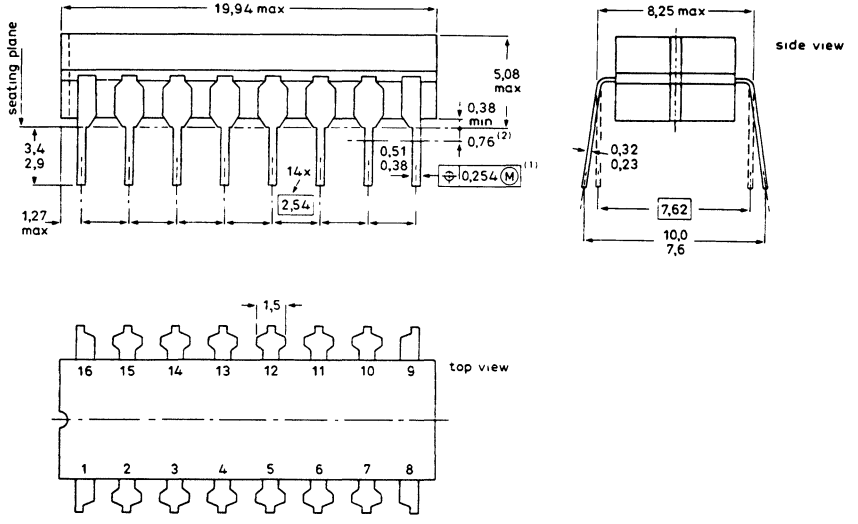
16-PIN PLASTIC QIP (SOT-58)



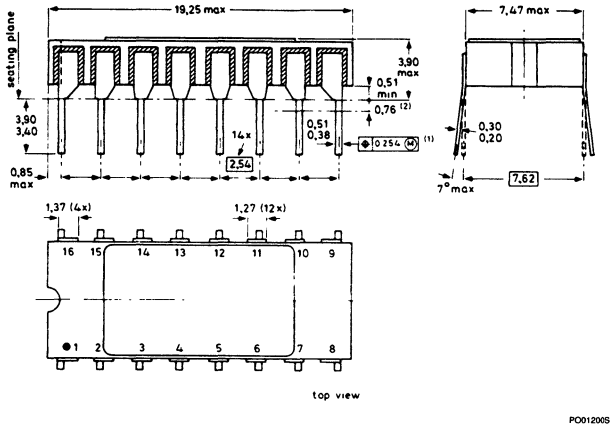
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

16-PIN CERDIP (SOT-74A, B, C)



16-PIN METAL CERDIP (SOT-84B)

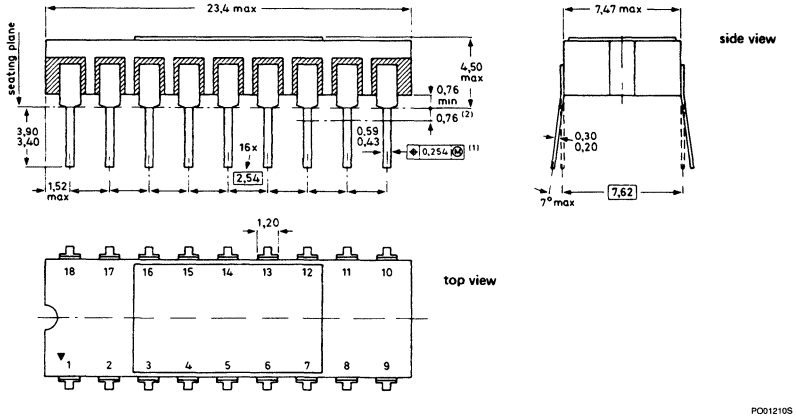


9

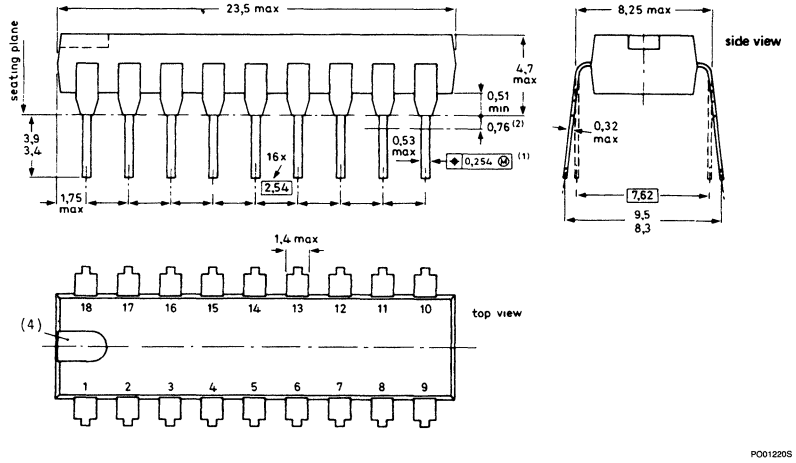
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

18-PIN METAL CERDIP (SOT-85B)



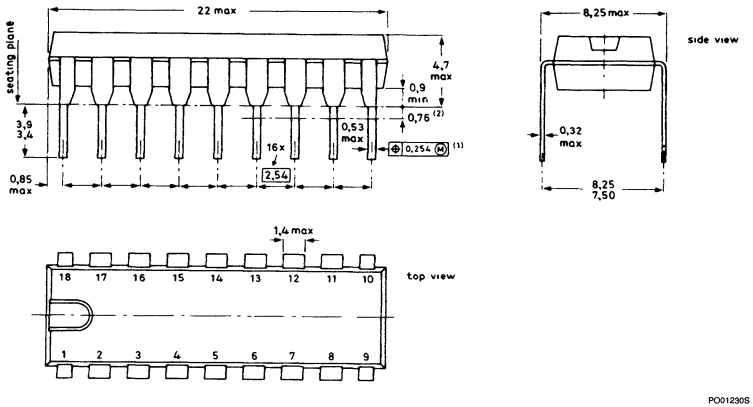
18-PIN PLASTIC DIP (SOT-102A)



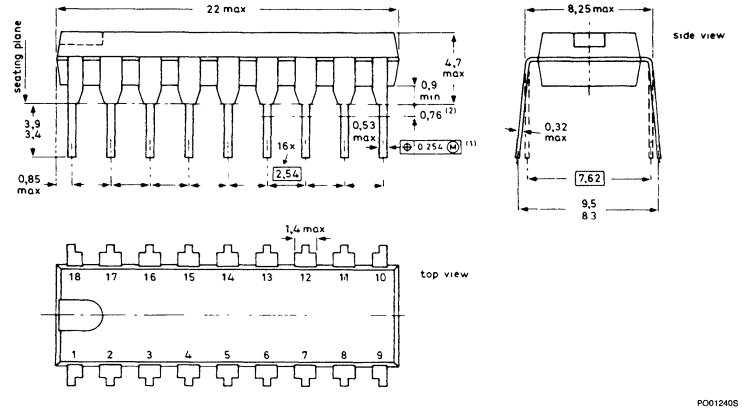
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

18-PIN PLASTIC DIP (SOT-102C)



18-PIN PLASTIC DIP (SOT-102CS)

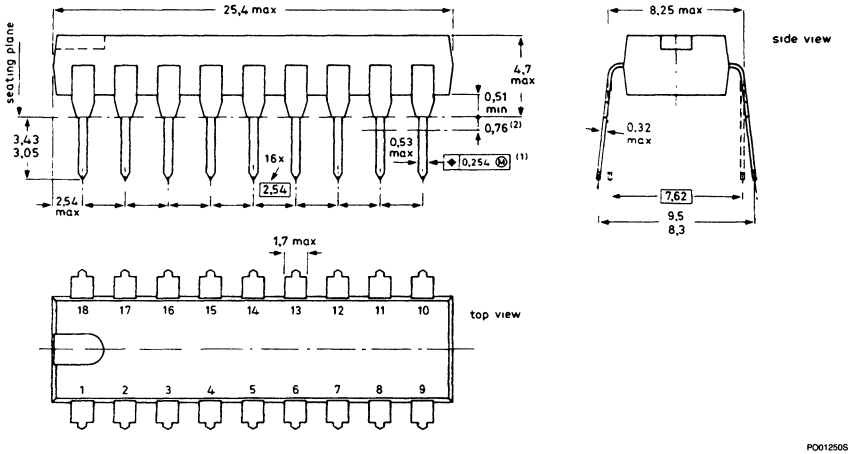


9

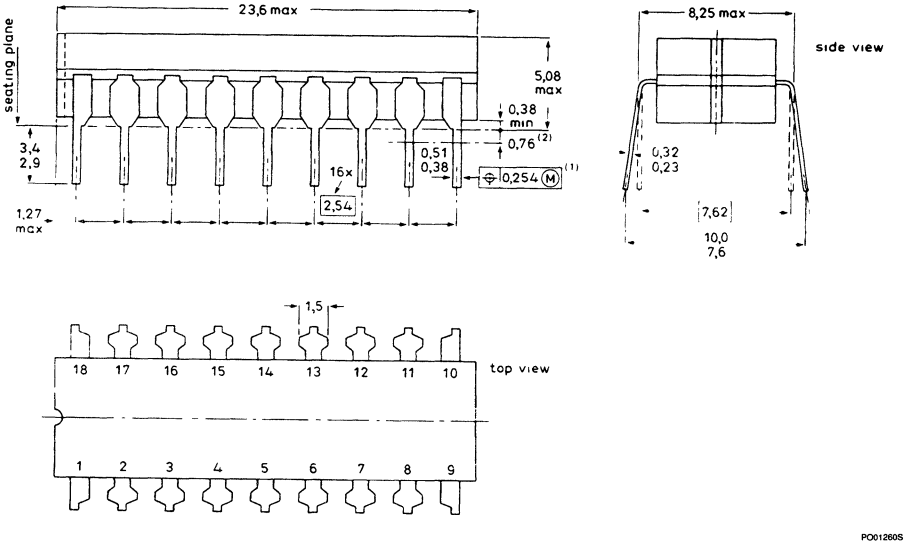
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

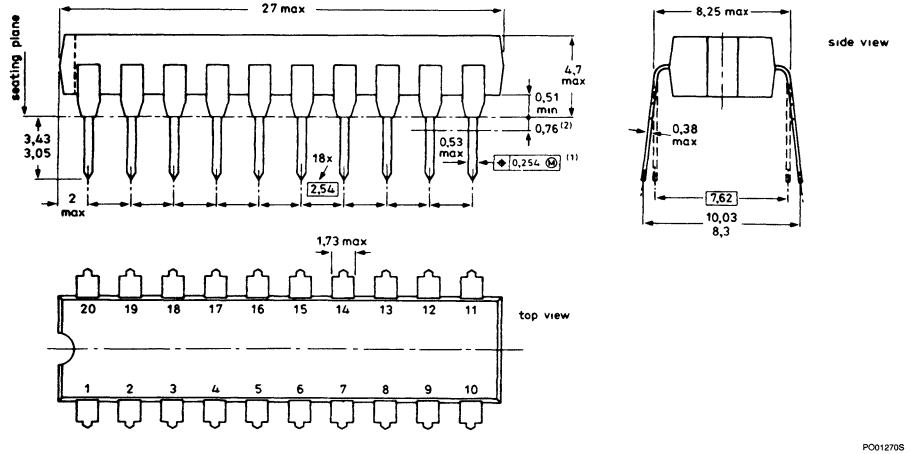
18-PIN PLASTIC DIP (SOT-102G)



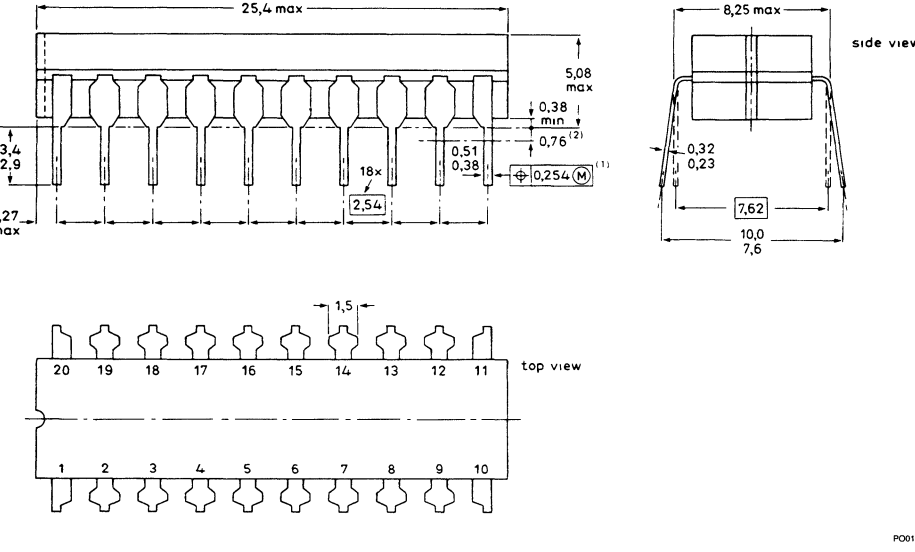
18-PIN CERDIP (SOT-133A, B)



20-PIN PLASTIC DIP (SOT-146)



20-PIN CERDIP (SOT-152B, C)

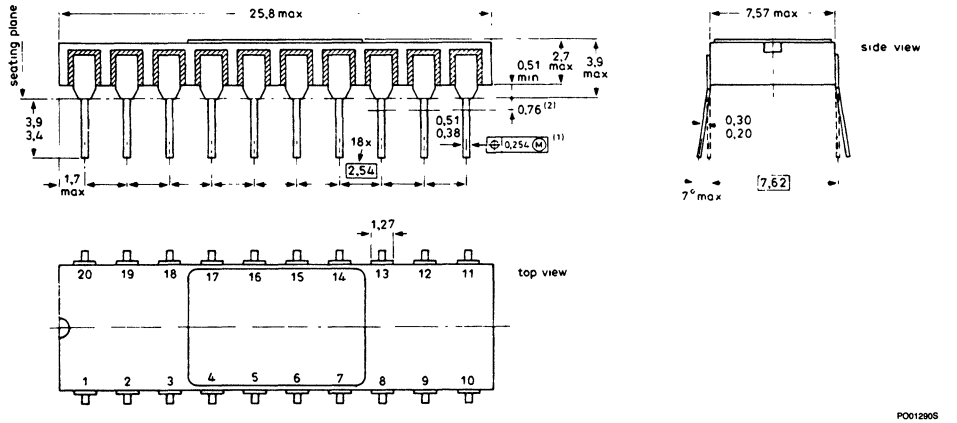


9

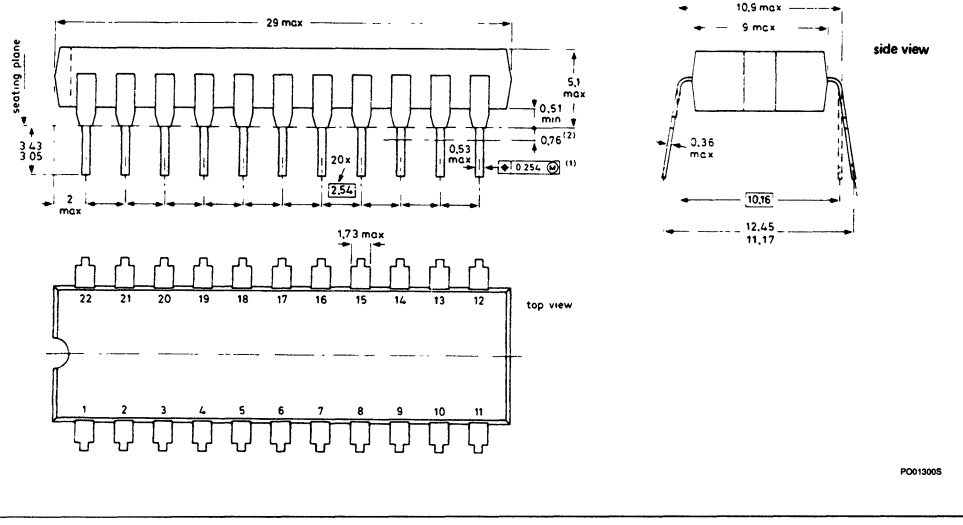
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

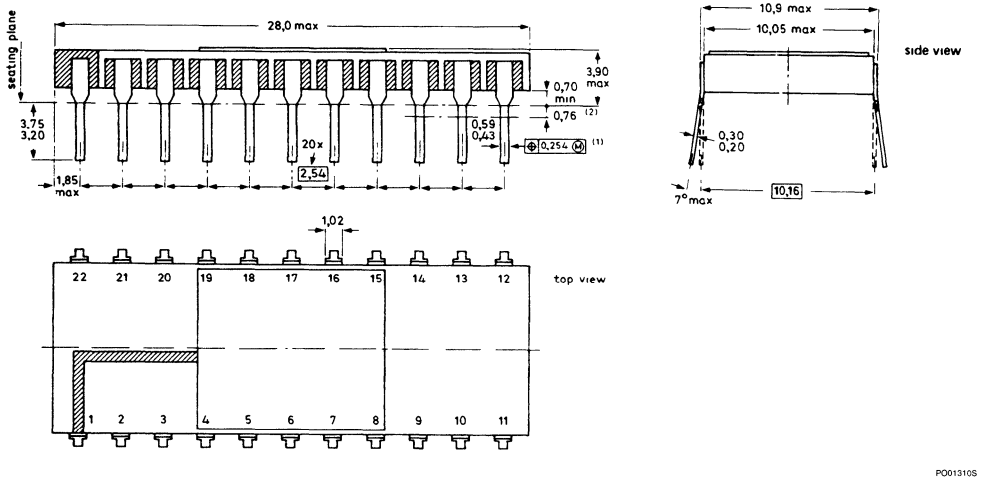
20-PIN METAL CERDIP (SOT-154B)



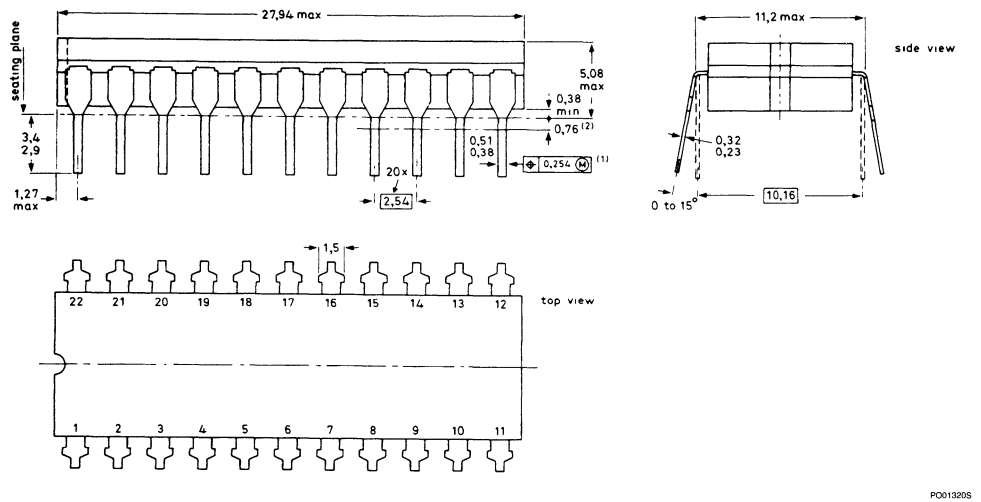
20-PIN PLASTIC DIP (SOT-116)



22-PIN METAL CERDIP (SOT-118B)



22-PIN CERDIP (SOT-134A)

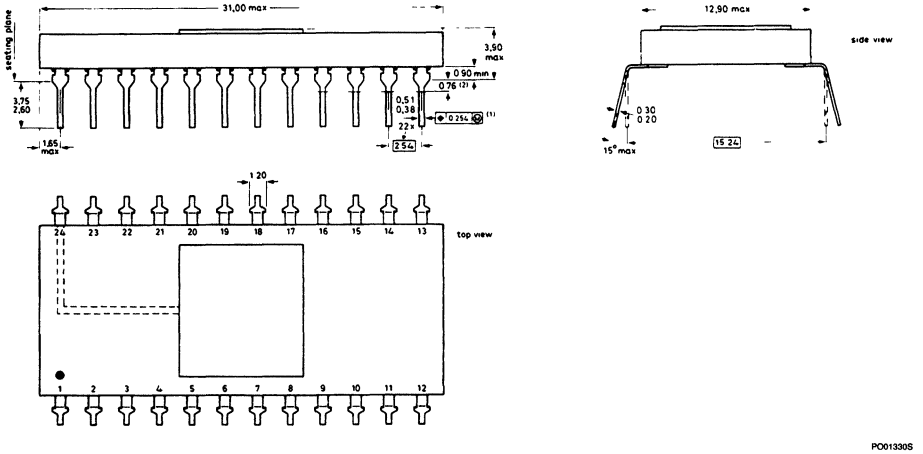


9

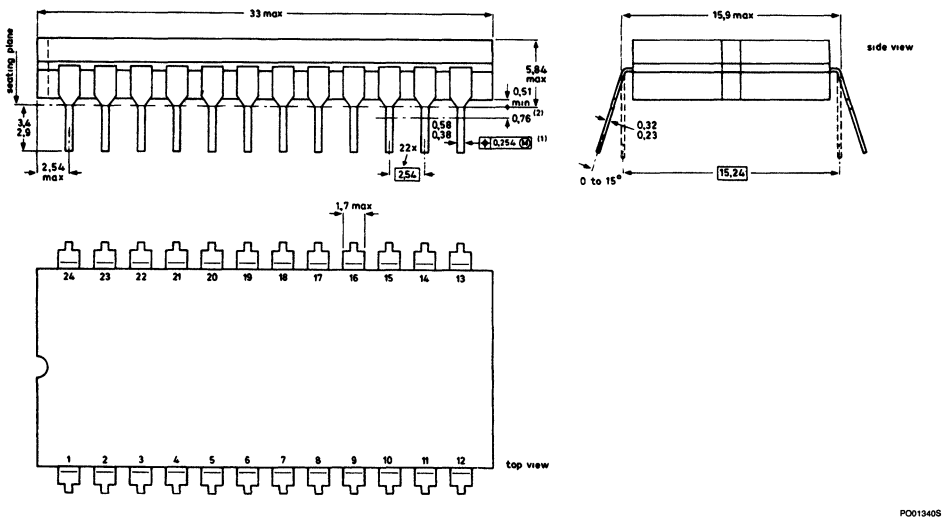
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

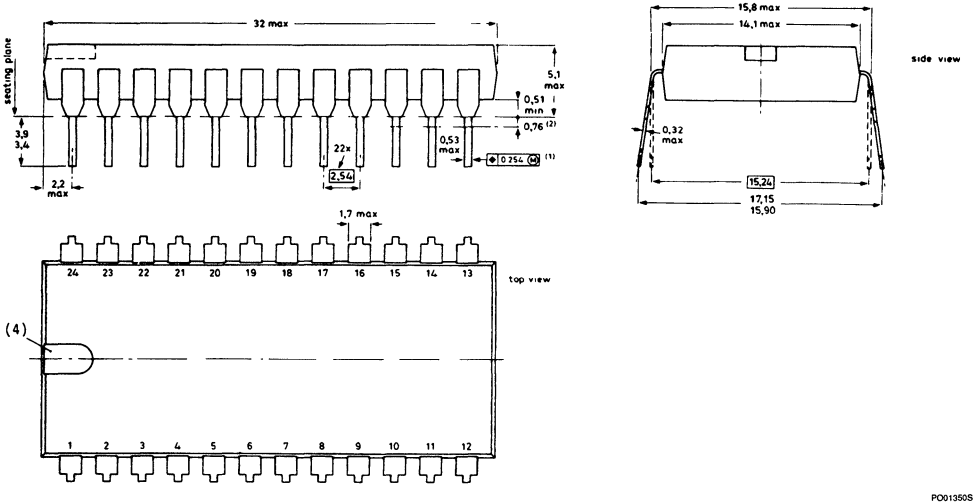
24-PIN METAL CERDIP (SOT-86A)



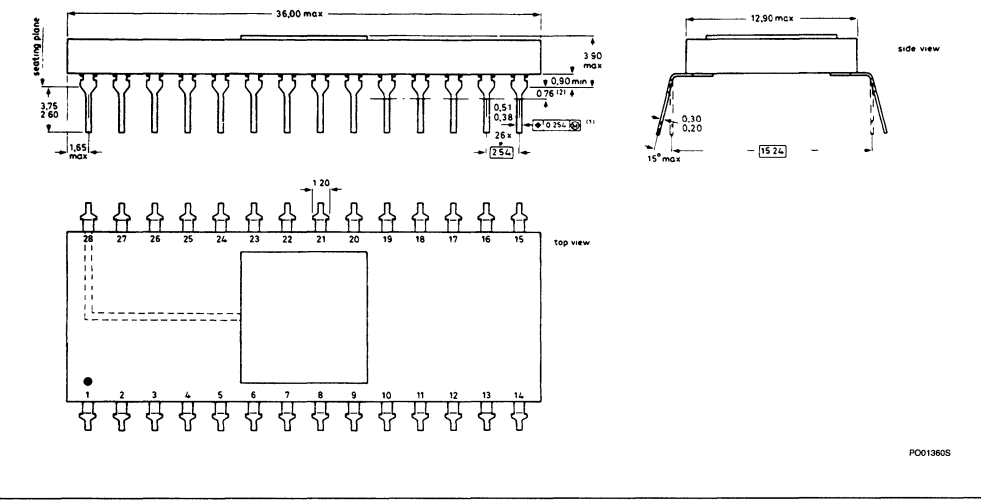
24-PIN CERDIP (SOT-94)



24-PIN PLASTIC DIP WITH INTERNAL HEAT SPREADER (SOT-101A, B)

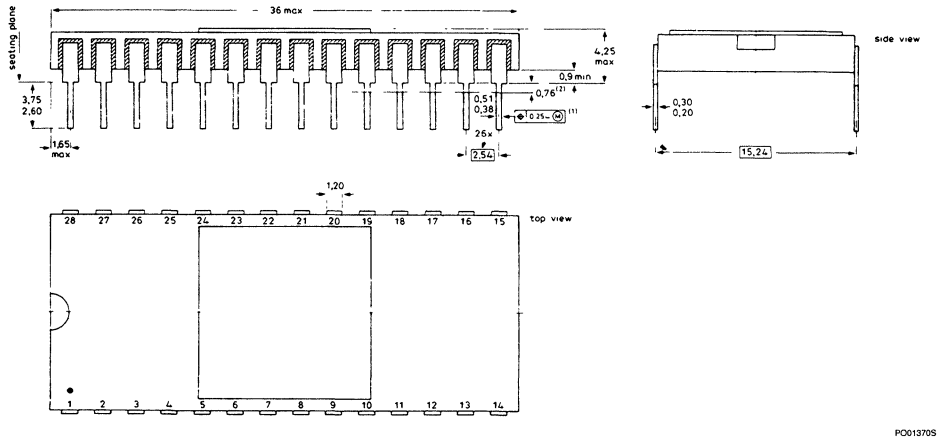


28-PIN METAL CERDIP (SOT-87A)

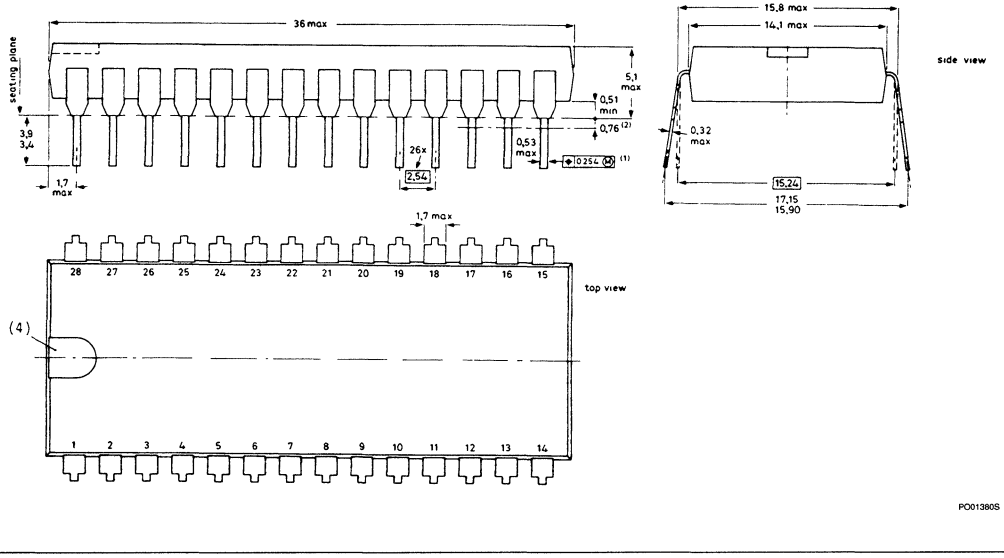


9

28-PIN METAL CERDIP (SOT-87B)



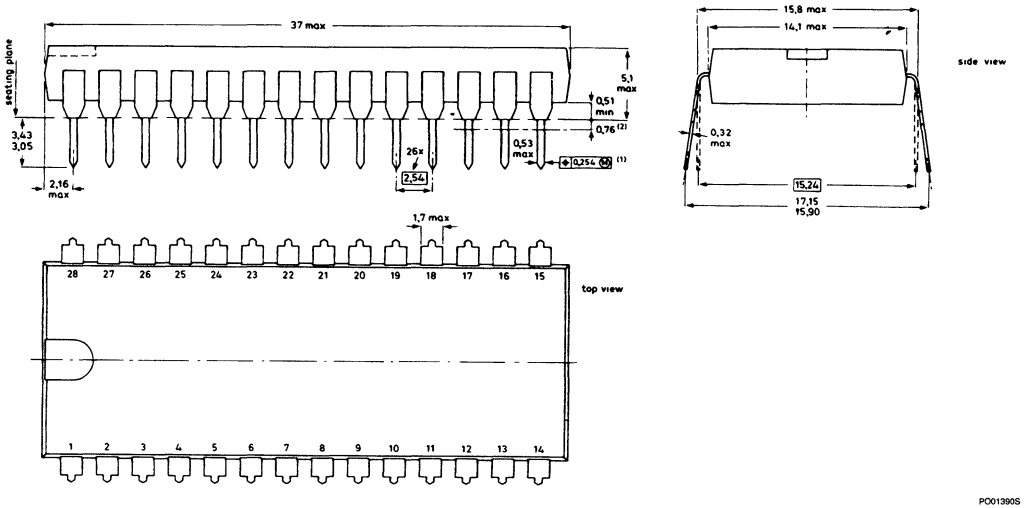
28-PIN PLASTIC DIP (SOT-117)



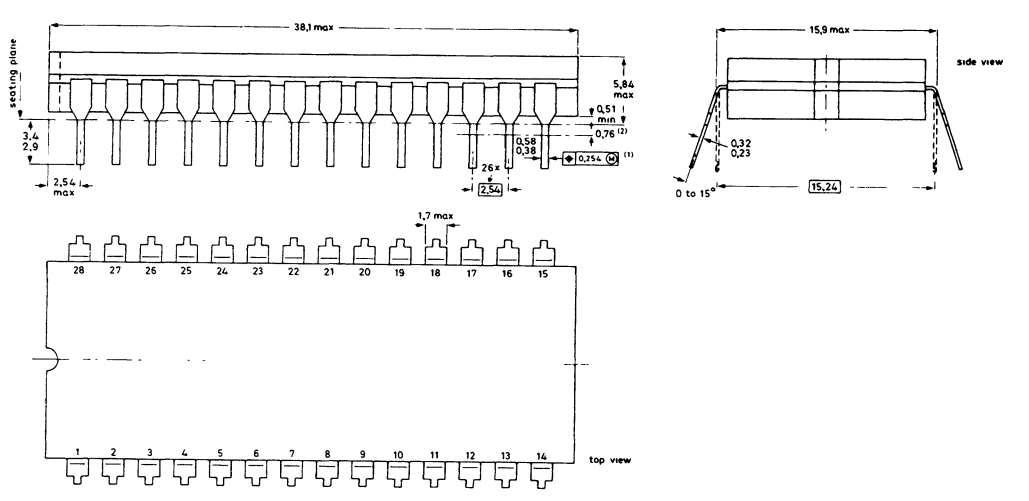
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

28-PIN PLASTIC DIP (SOT-117D)



28-PIN CERDIP (SOT-135A)

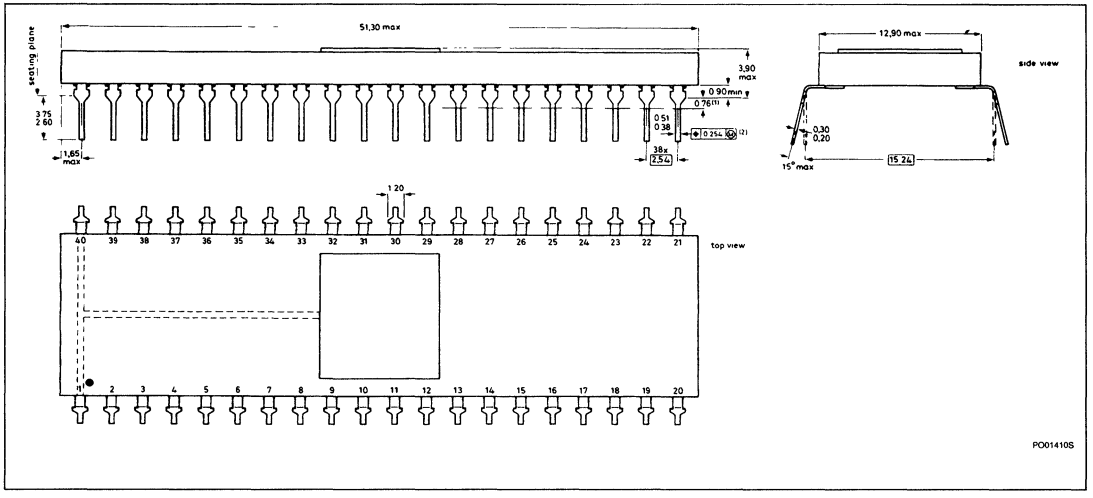


9

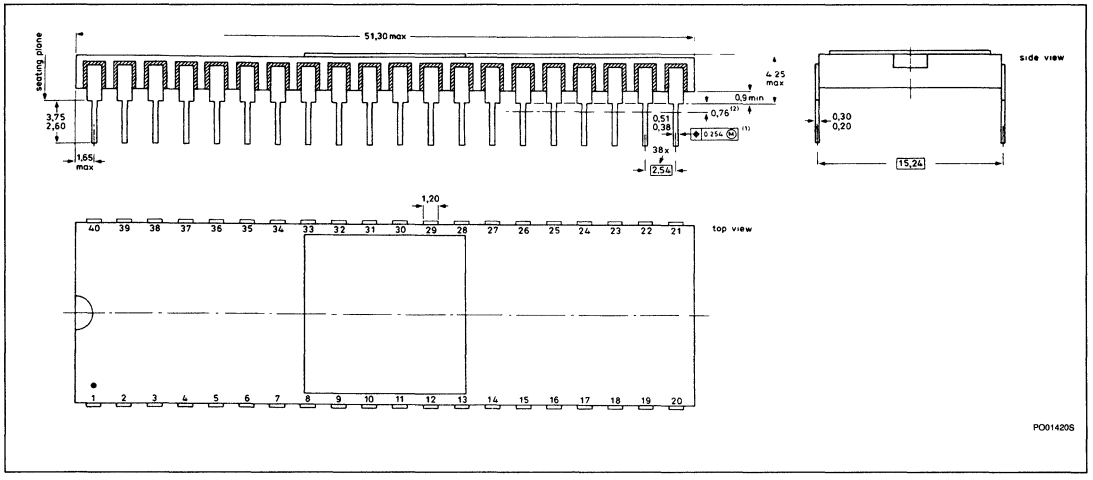
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

40-PIN METAL CERDIP (SOT-88)



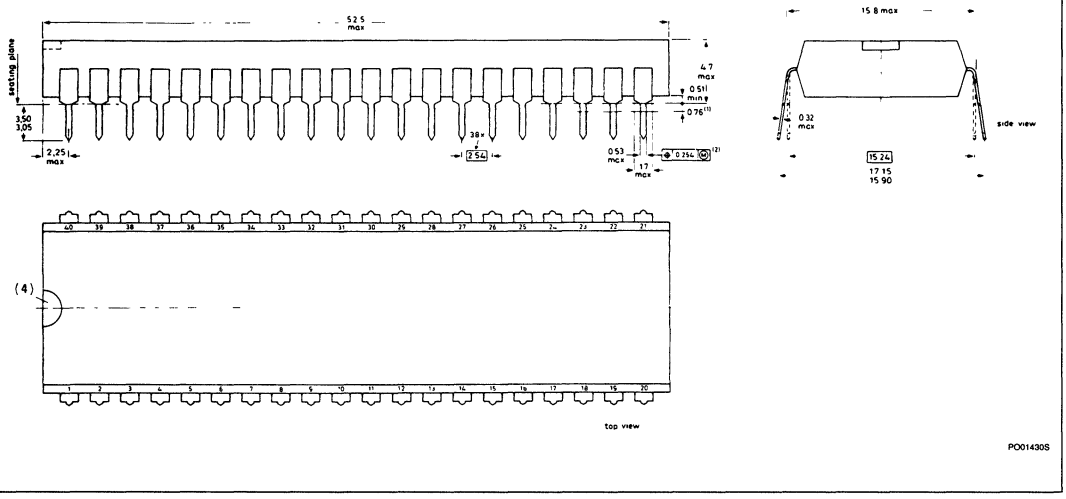
40-PIN METAL CERDIP (SOT-88B)



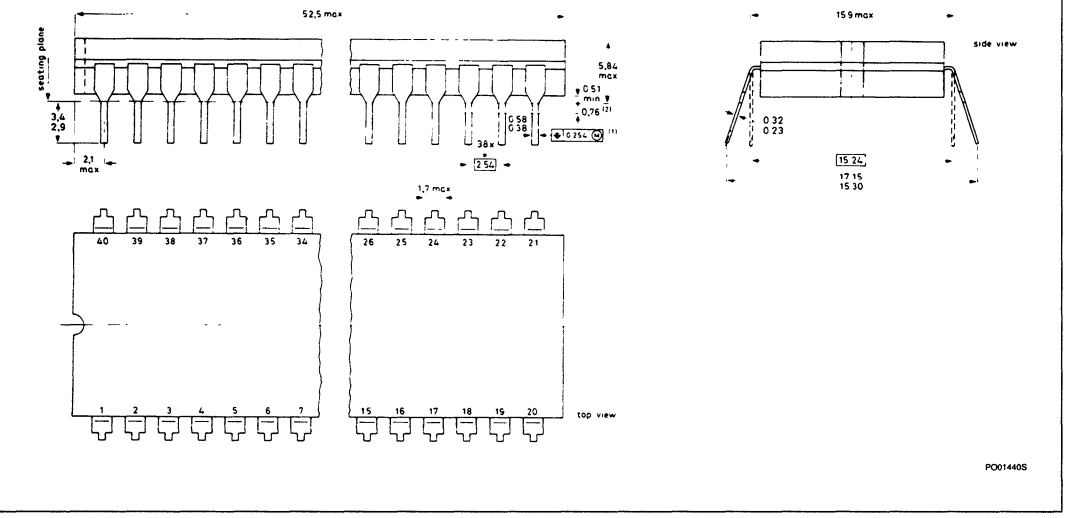
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

40-PIN PLASTIC DIP (SOT-129)



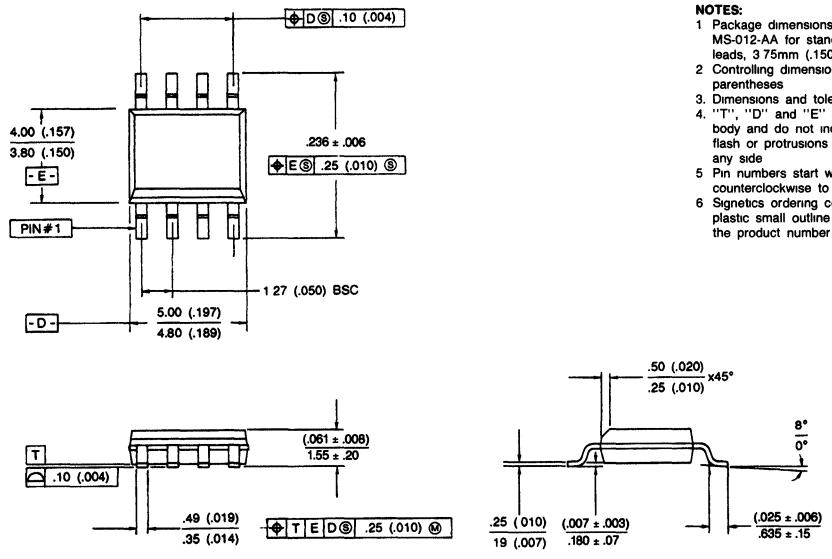
40-PIN CERDIP (SOT-145)



For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

8-PIN PLASTIC SO (D PACKAGE) (SO-8, SOT-96A)

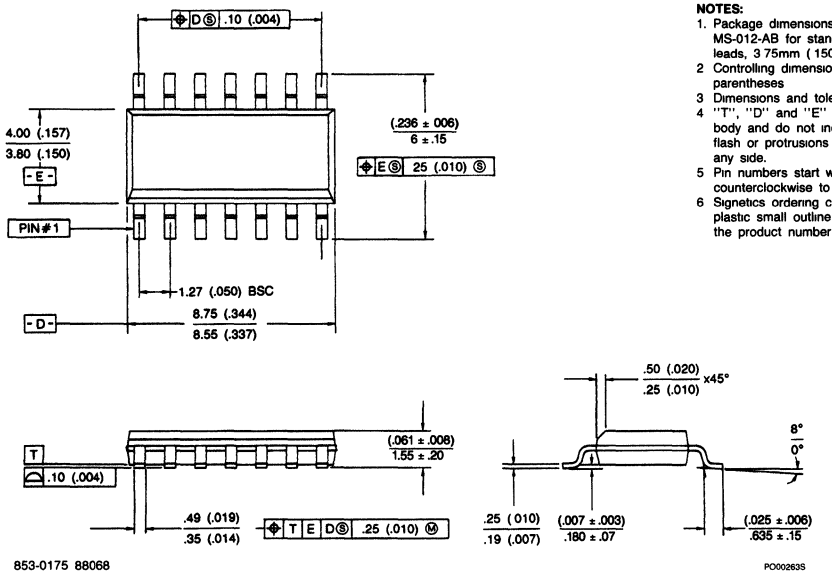


853-0174 88070

PO0027S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3 75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14 5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

14-PIN PLASTIC SO (D PACKAGE) (SO-14, SOT-108A)

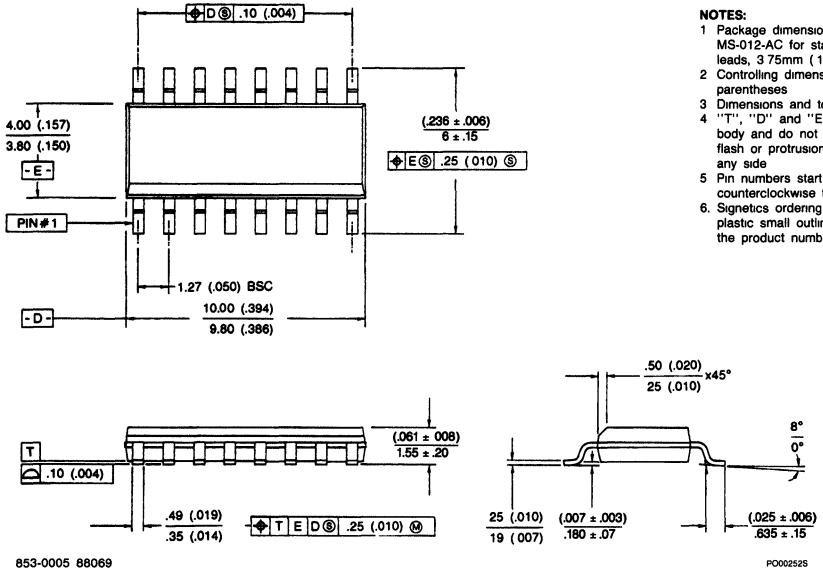


853-0175 88068

PO0026S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3 75mm (150") body width (issue A, June 1985)
2. Controlling dimensions are in mm Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M- 1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

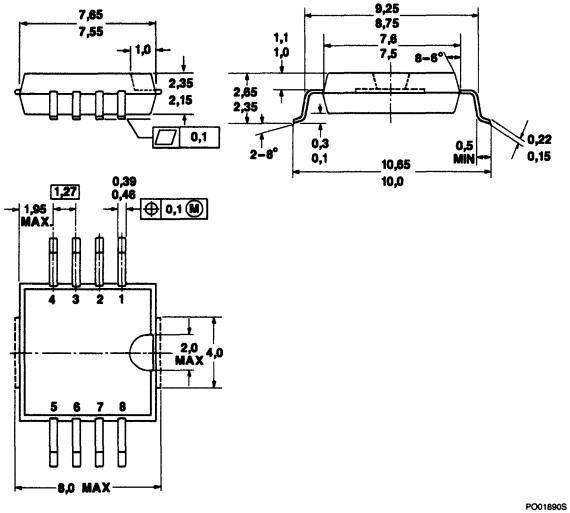
16-PIN PLASTIC SO (D PACKAGE) (SO-16, SOT-109A)



NOTES:

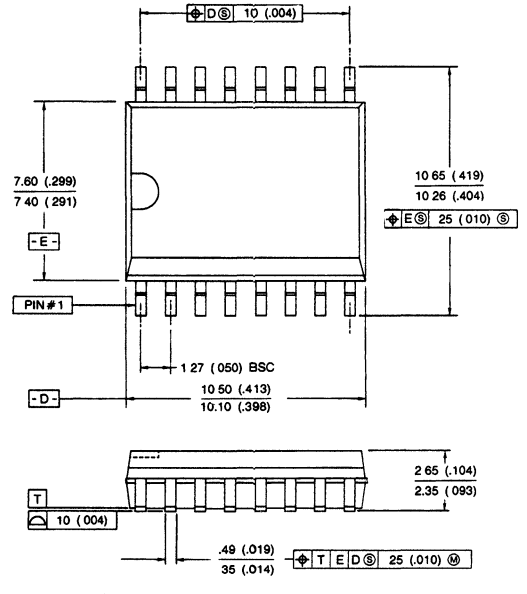
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3 75mm (.150") body width (issue A, June 1985)
2. Controlling dimensions are in mm Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14 5M- 1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions Mold flash or protrusions shall not exceed 15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

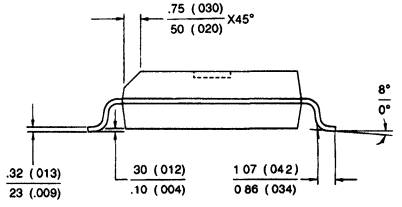
8-PIN PLASTIC SOL (D Package) (SOL-8, SOT-176)



9

16-PIN PLASTIC SOL (D PACKAGE) (SOL-16, SOT-162A)



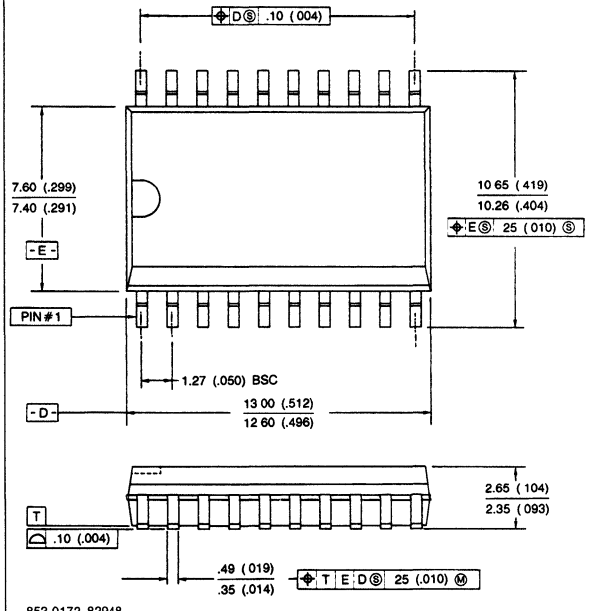


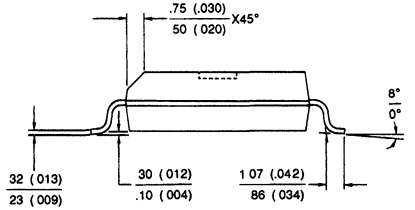
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

853-0171 81218

PO00241S

20-PIN PLASTIC SOL (D PACKAGE) (SOL-20, SOT-163A)



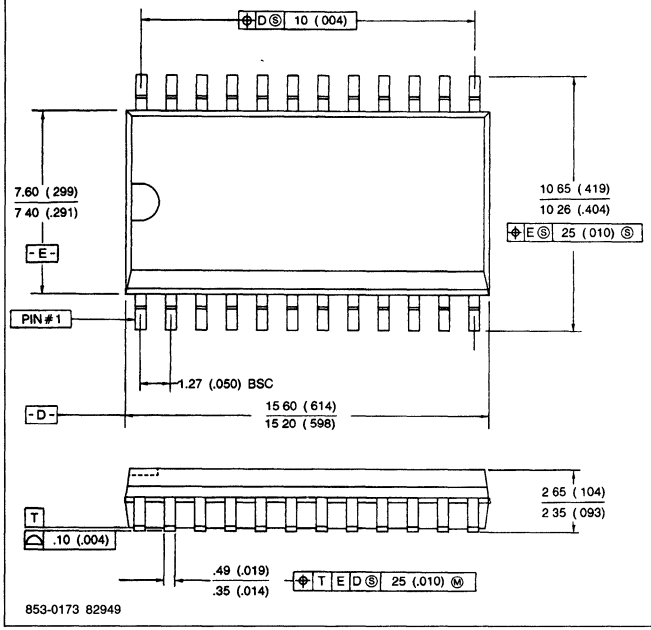


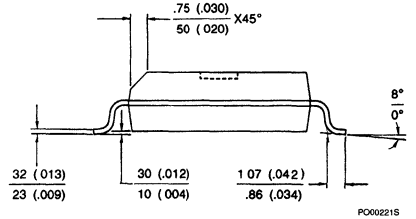
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0172 82948

PO00231S

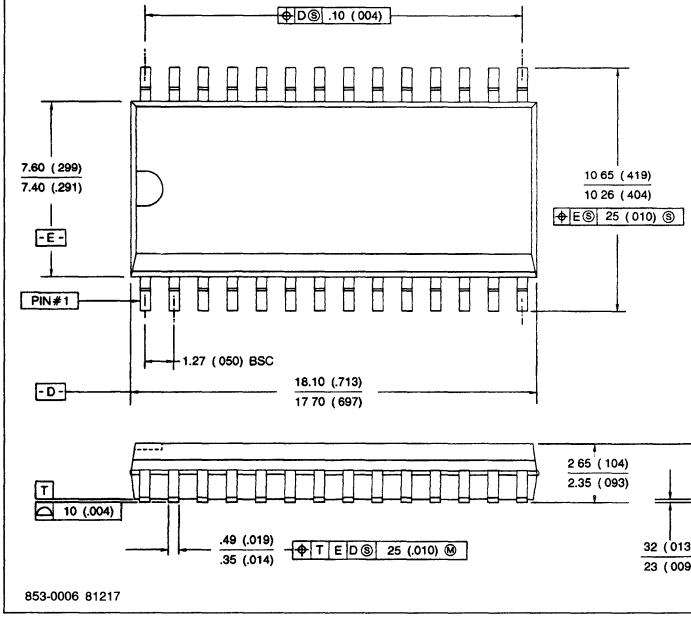
24-PIN PLASTIC SOL (D PACKAGE) (SOL-24, SOT-137A)

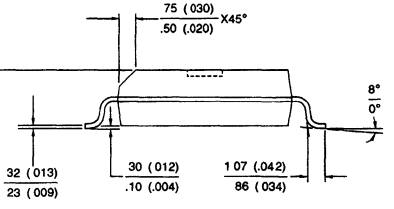




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

28-PIN PLASTIC SOL (D PACKAGE) (SOL-28, SOT-136A)



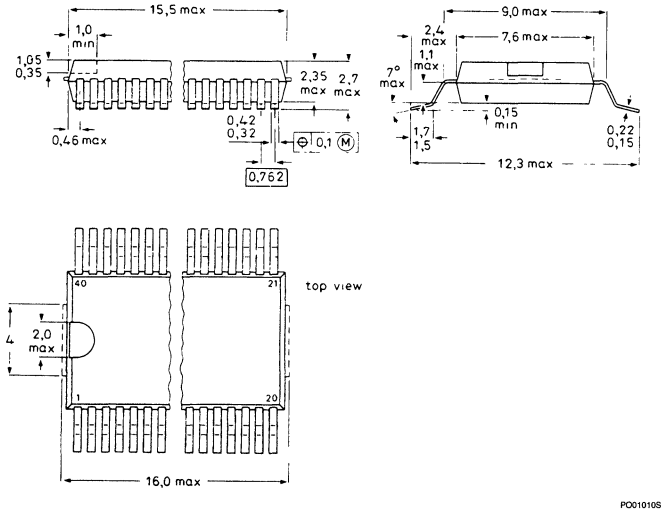


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985)
2. Controlling dimensions are in mm. Inch dimensions in parentheses
3. Dimensions and tolerancing per ANSI Y14.5M-1982
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number

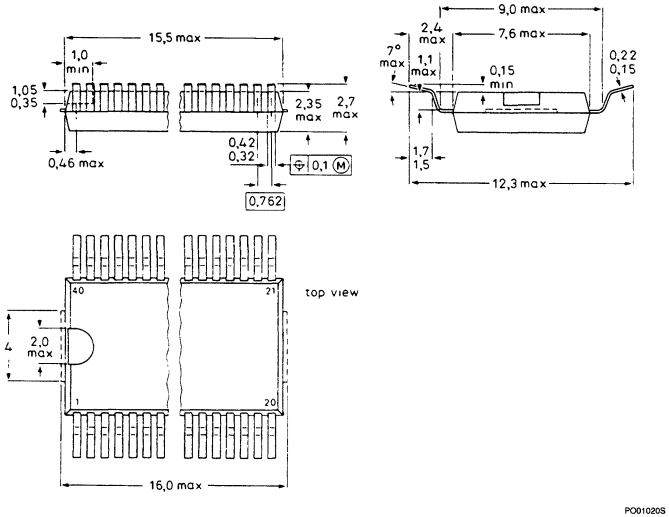
For Prefixes HEF, OM, PCD, PCF, PNA, SAA, SAB, TDA, TDD, TEA

Package Outlines

40-PIN PLASTIC SO (VSO-40, SOT-158A)



40-PIN PLASTIC SO (OPPOSITE BENT LEADS) (VSO-40, SOT-158B)



Signetics

Linear Products

Section 10
Sales Offices

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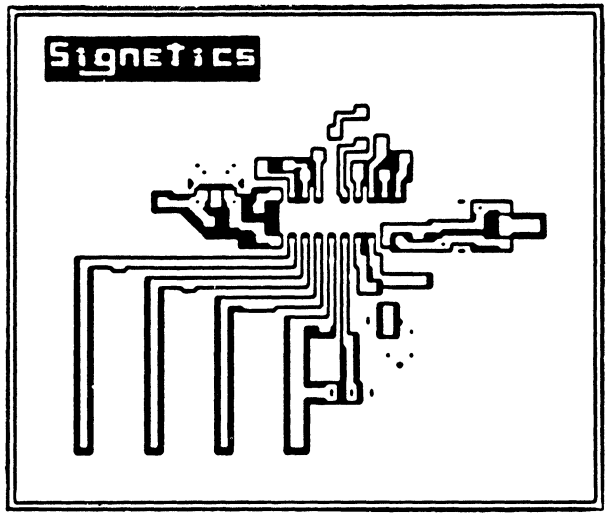
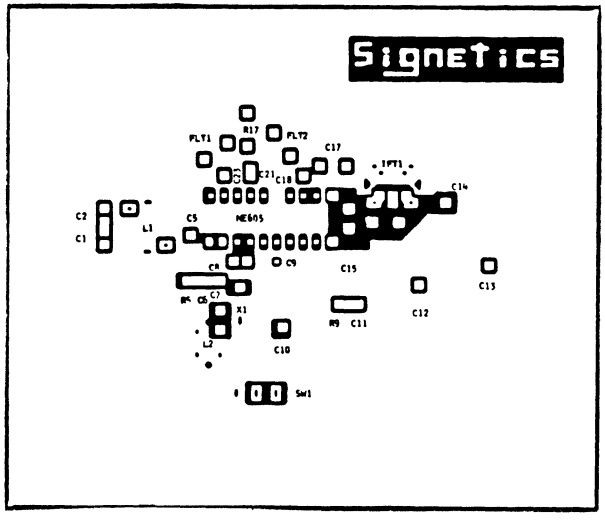
Effective October 1988

Additional Drawings for the NE/SA605





Additional Drawings for the NE/SA605

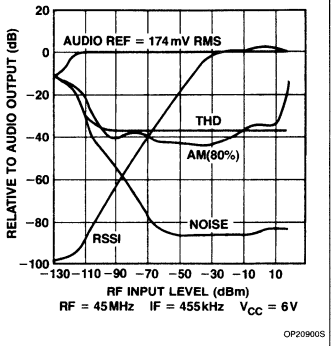


Figure 3. NE/SA605 Application Board at 25°C

Additional Drawings for the NE/SA575

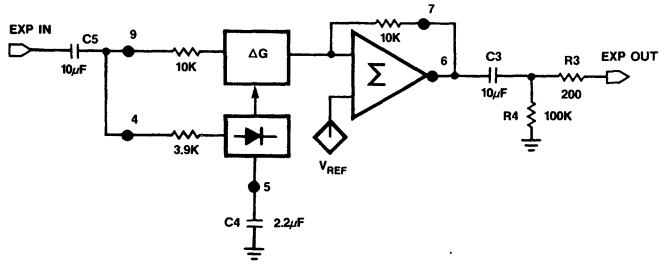


Figure 1. Typical Expandor Configuration

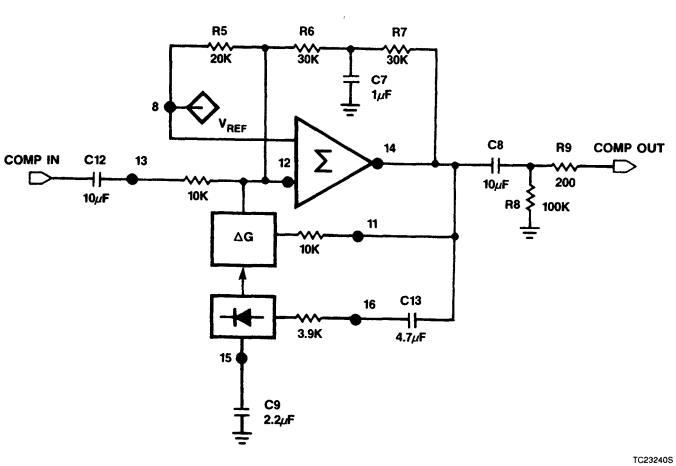


Figure 2. Typical Expandor Configuration

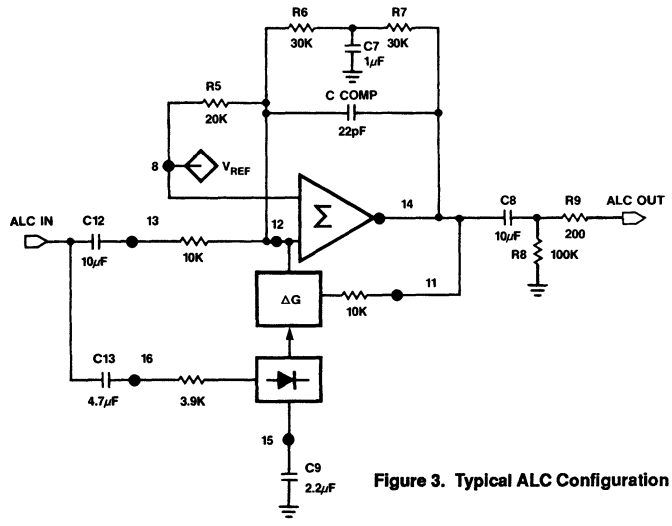


Figure 3. Typical ALC Configuration

Additional Drawings for the NE/SA575

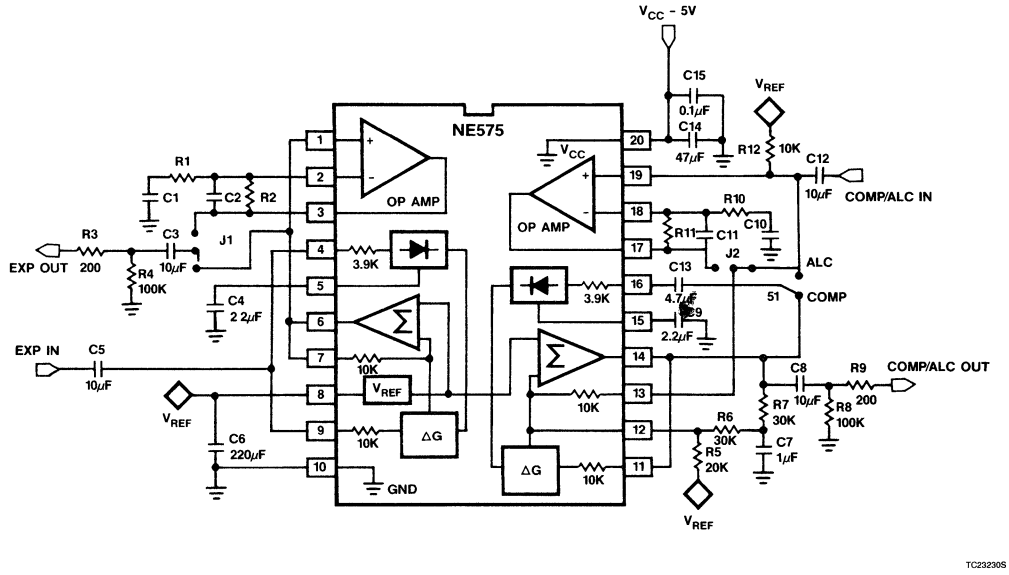


Figure 4. Signetics NE575 Low Voltage Expandor/Compressor/ALC Demo Board

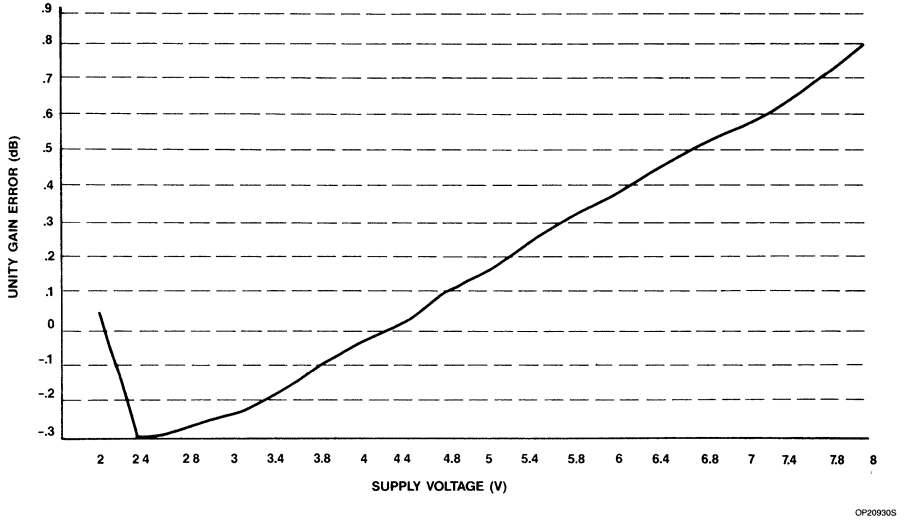


Figure 5. Unity Gain Error vs Supply Voltage

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