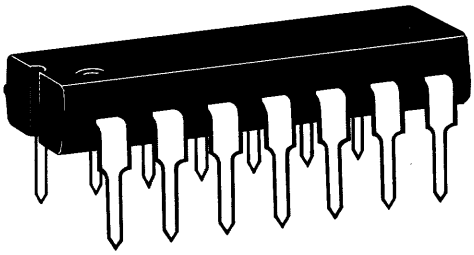
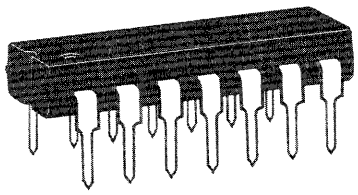


UTILOGIC® II HANDBOOK

SPECIFICATIONS
USAGE RULES
APPLICATIONS

MAY 1968



UTILOGIC® II HANDBOOK

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UTILOGIC II

SP300A SERIES (0°C to +75°C)
LU300A SERIES (+10°C to +55°C)

- DUAL IN-LINE PACKAGING
- GREATER THAN 1-VOLT DC NOISE MARGINS

INTRODUCTION

UTILOGIC II is a newly engineered version of Signetics original UTILOGIC family which was introduced in 1964. New features and devices in UTILOGIC II include dual in-line plug-in packaging, two new dual J-K flip-flops, three new multiple NOR gates (dual, triple, and quad), a new expandable dual OR gate and a new dual buffer. The proven performance of the earlier UTILOGIC family, including greater than 1-volt noise margins and high capacitive drive capability has been retained. The simplicity of the silicone package provides inherently low cost in both manufacturing and subsequent handling by the user, as well as very reliable performance under severe environmental conditions. Extensive reliability data based on nearly three years of testing this package is available on request to Signetics Technical Information Center.

UTILOGIC II elements are available in two temperature ranges: those with SP prefixes are for applications in the 0°C to 75°C range, and those with LU prefixes in the +10°C to +55°C range.

The suffix A signifies the 14-pin dual in-line package; the suffix B signifies the 16-pin dual in-line package.

At the time of the writing of this handbook (March 1968), the UTILOGIC II family consists of the following elements:

SP/LU300A – Dual 3-Input Expander
SP/LU305A – Single 6-Input AND Gate
SP/LU306A – Dual 3-Input AND Gate
SP/LU314A – Single 7-Input NOR Gate
SP/LU317A – Dual 4-Input Expandable NOR Gate
SP/LU321A – Dual J-K Binary
SP/LU322B – Dual J-K Binary
SP/LU333A – Dual 3-Input Expandable OR Gate
SP/LU356A – Dual 4-Input Expandable Line Driver
SP/LU370A – Triple 3-Input NOR Gate
SP/LU380A – Quad 2-Input NOR Gate

LOADING DEFINITIONS

UTILOGIC II loads are classified as "sink loads," or current out of the load inputs, and as "source loads," or current into the load inputs. The standard sink load is the input of a UTILOGIC II AND gate. The standard source load is the input of a UTILOGIC II NOR gate. See loading chart for specific values.

NOISE MARGINS

Signetics specifies noise immunity on UTILOGIC II NOR gates in terms of DC margins determined under worst conditions for both the "0" and "1" levels. The margin for a "1" input applies to negative-going noise on the high level or on the power supply line. The margin for a "0" input applies to positive-going noise on the low logic level or the ground line.

The DC margin is defined as the difference between the worst case output level and the worst case input threshold. Output levels for the NOR are 3.8 volts or greater for the "1" level and 0.6 volts or less for the "0" level. The corresponding input thresholds are 2.7 volts for "1" and 1.4 volts for "0". Thus, the minimum DC margins are specified as 1100 mV for "1" and 800 mV for "0" levels.

Current margins, which Signetics specifies in addition to the familiar voltage margins, are quite useful to the designer because current margins provide a measure of the amount of coupling necessary to cause an erroneous output. Specifications state that the UTILOGIC II NOR's can supply 2 mA at the "1" level and sink 12.5 mA at the "0" level. The maximum specified fan-out of these elements is 11 source loads (requiring 1.98 mA) and 5 sink loads (requiring 12.5 mA).

For AND gates, maximum offset voltages, which are more appropriate to non-saturating gates, are specified. These offset voltages ensure maintenance of high DC margins in cascaded logic configurations.

OPERATING VOLTAGE FOR ALL UTILOGIC II ELEMENTS: 5V ±5%

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

VOLTAGE APPLIED (All Terminals)	±5.5V (Note 4)
CURRENT RATING (All Input Terminals)	±10 mA (Note 4)
CURRENT RATING (All Other Terminals)	±50 mA (Note 4)
OPERATING TEMPERATURE (SP300)	0°C to +75°C
OPERATING TEMPERATURE (LU300)	+10°C to +55°C

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 — Standard Conditions: V_{CC} = +5.0V, T = +25°C)

300

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
EXPANSION FORWARD VOLTAGE	V_{OUT}	1.85			V	V_{IN} = +2.7V, R_{OUT} = 590Ω ±1% to 0V
AVERAGE GATE DELAY	t_{pd}		5.0		ns	Measured at 50% points
FAN-IN EXPANSION OF 317				33		See text under "NOR GATES"

321, 322

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
"1" OUTPUT VOLTAGE	V_{OUT}	3.8			V	I_{OUT} = −1.6 mA
"0" OUTPUT VOLTAGE	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA
"0" INPUT CURRENT: CLOCK, S_D, R_D INPUTS						
(321) CLOCK, R_D	I_{IN}			−6.2	mA	V_{IN} = 0.6V
(322) CLOCK, R_D	I_{IN}			−3.1	mA	V_{IN} = 0.6V
(321, 322) S_D	I_{IN}			−3.1	mA	V_{IN} = 0.6V
(321, 322) J-K	I_{IN}			−1.6	mA	V_{IN} = 0.6V
"1" INPUT CURRENT (321, 322) J-K	I_{IN}			50*	μA	V_{IN} = 4.5V
AVERAGE POWER CONSUMPTION			90		mW	Each binary
AVERAGE PROPAGATION DELAY	t_{pd}		25		ns	R_L = 1.6K to Gnd, C_L = 50 pF, P.W. = 200 ns
AVERAGE PROPAGATION DELAY	t_{pd}		35		ns	R_L = 1.6K to Gnd, C_L = 130 pF, P.W. = 200 ns
FAN-OUT						
To sink loads				5		Notes 6, 7
To source loads				8		Notes 6, 7

*Proportionally higher on Clock, R_D and S_D inputs.

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 — Standard Conditions: V_{CC} = +5.0V, T = +25°C)

305, 306

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
"1" OFFSET VOLTAGE	$V_{IN} - V_{OUT}$	0.15			V	I_{OUT} = –1.8 mA, V_{IN} = +3.8V
"0" OFFSET VOLTAGE	$V_{IN} - V_{OUT}$			–0.3	V	V_{IN} = +0.6V
"0" INPUT CURRENT	I_{IN}			–2.5	mA	V_{IN} = +0.6V
AVERAGE POWER CONSUMPTION			6.0		mW	Each gate; 50% duty cycle
AVERAGE GATE DELAY (Measured at 50% points)	t_{pd}		15		ns	R_L = 16K to Gnd; C_L = 8 pF to Gnd; F.O. = 1
	t_{pd}		35		ns	R_L = 1.6K to Gnd; C_L = 75 pF to Gnd; F.O. = 10
FAN-OUT (To source loads)				10		Note 6

333, 314, 317, 370 and 380

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"		800	1200		mV	Note 8
NOISE IMMUNITY FOR "1"		1100	1700		mV	Note 8
"1" OUTPUT VOLTAGE						
(314, 317, 370, 380)	V_{OUT}	3.8			V	I_{OUT} = –2 mA, V_{IN} = +1.4V
(333 only))	V_{OUT}	3.8			V	I_{OUT} = –2 mA, V_{IN} = +2.7V
"0" OUTPUT VOLTAGE						
(314, 317, 370, 380)	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA, V_{IN} = +2.7V
(333 only)	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA, V_{IN} = +1.4V
"1" INPUT CURRENT	I_{IN}			180	μA	V_{IN} = +2.7V
EXPANDER NODE VOLTAGE (317, 333)	V_N	1.85			V	V_{IN} = +2.7V
AVERAGE POWER CONSUMPTION (314, 317, 370, 380)			22		mW	Each gate; 50% duty cycle
(333 only)			44		mW	Each gate; 50% duty cycle
AVERAGE PROPAGATION DELAY	t_{pd}		20		ns	7-stage ring oscillator
(314, 317, 370, 380)	t_{pd}		30		ns	7-stage ring oscillator, C_L = 130 pF/gate
AVERAGE GATE DELAY	t_d		20		ns	R_L = 16K to Gnd; C_L = 8 pF to Gnd; F.O. = 1
(333 at 50% points)	t_d		35		ns	R_L = 1.6K to Gnd; C_L = 130 pF to Gnd; F.O. = 12
FAN-OUT						
To sink loads				5		Note 6, 7
To source loads				11		Note 6, 7

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 – Standard Conditions: V_{CC} = +5.0V, T = +25°C)

356

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"			800		mV	Note 8
NOISE IMMUNITY FOR "1"			1500		mV	Note 8
"1" OUTPUT VOLTAGE	V_{OUT}	3.5			V	I_{OUT} = –2 mA, V_{IN} = +1.0V
"0" OUTPUT VOLTAGE	V_{OUT}			0.6	V	I_{OUT} = 44 mA, V_{IN} = +2.7V
"0" INPUT CURRENT	I_{IN}			–2.5	mA	V_{IN} = +0.6V
AVERAGE POWER CONSUMPTION			37		mW	Each gate, 50% duty cycle
AVERAGE PROPAGATION DELAY	t_{pd}		55		ns	
FAN-OUT						
To sink loads				17		Note 6, 7
To source loads				11		Note 6, 7

Notes:

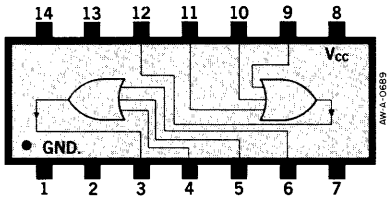
1. Pins not specifically referenced are left electrically open.
2. All voltage measurements are referenced to the ground pin. Positive current flow is defined as into the terminal indicated.
3. Maximum ratings are values above which serviceability may be impaired.
4. Precautionary measures should be taken to ensure current limiting per the maximum ratings should the isolation diodes become forward biased.
5. Positive Logic Definition: "UP" Level = "1"; "DOWN" Level = "0".
6. Sink load is defined as a 306 Input, source load is defined as a 317 Input.
7. This device is capable of accommodating the maximum specified sink and source loads concurrently.
8. This characteristic guaranteed by output voltage measurements.
9. Manufacturer reserves right to make design and process improvements.

NORMALIZED LOADING CHART (Notes 2 and 3)

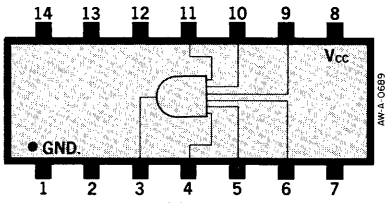
ELEMENT	INPUT LOAD		FAN-OUT		ELEMENT	INPUT LOAD		FAN-OUT	
	SINK	SOURCE	SINK	SOURCE		SINK	SOURCE	SINK	SOURCE
300		1.0	Note 1	Note 1	321, 322	N/A	N/A	5	8
305, 306	1.0			10	J,K INPUTS	0.7	0.5	N/A	N/A
314, 317		1.0	5	11	CLOCK, R_D (321)	2.5	1.0	N/A	N/A
370, 380		1.0	5	11	CLOCK' R_D (322)	1.3	0.5	N/A	N/A
333		1.0	5	11	S_D (321, 322)	1.3	0.5	N/A	N/A
356	1.0		17	11					

Loading Chart Notes:

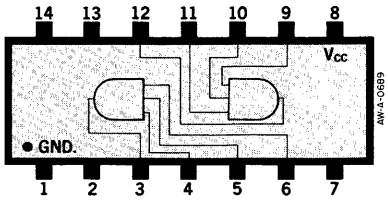
1. Output to connect to 317 or 333 expansion node only.
2. Normalized sink load is 306 maximum input current = -2.5 mA.
3. Normalized source load is 317 maximum input current = 180 μA.



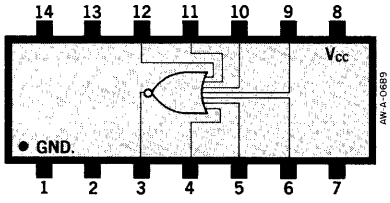
300A
DUAL 3-INPUT EXPANDER



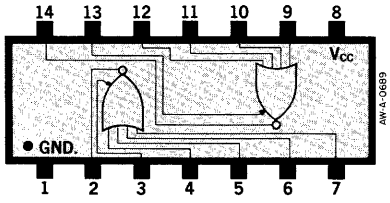
305A
6-INPUT AND GATE



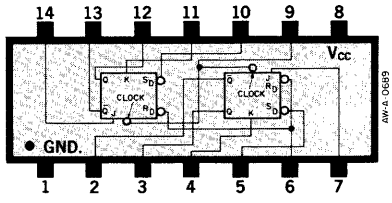
306A
DUAL 3-INPUT AND GATE



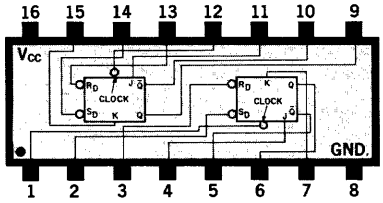
314A
7-INPUT NOR GATE



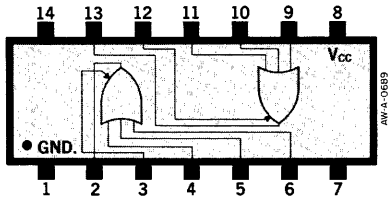
317A
DUAL 4-INPUT EXPANDABLE NOR GATE



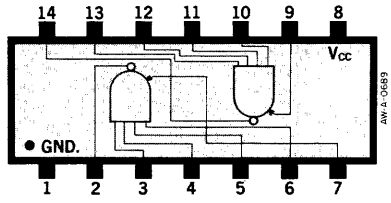
321A
DUAL J-K BINARY



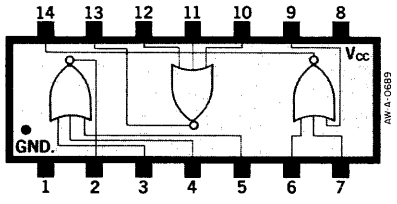
322B
DUAL J-K BINARY



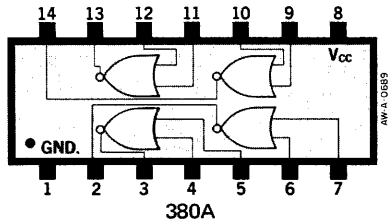
333A
DUAL 3-INPUT EXPANDABLE OR GATE



356A
DUAL 4-INPUT EXPANDABLE LINE DRIVER

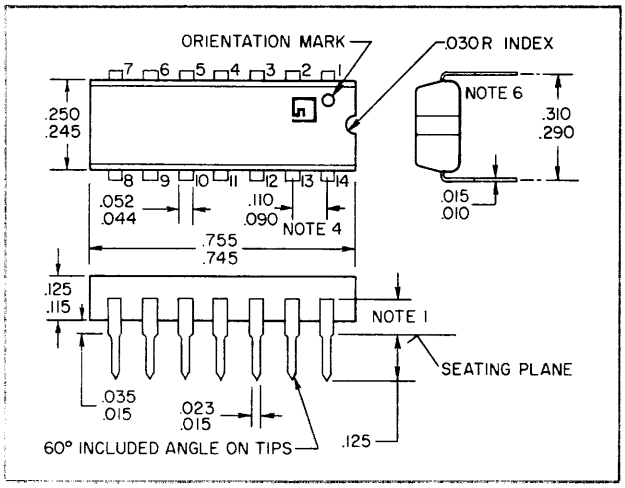


370A
TRIPLE 3-INPUT NOR GATE

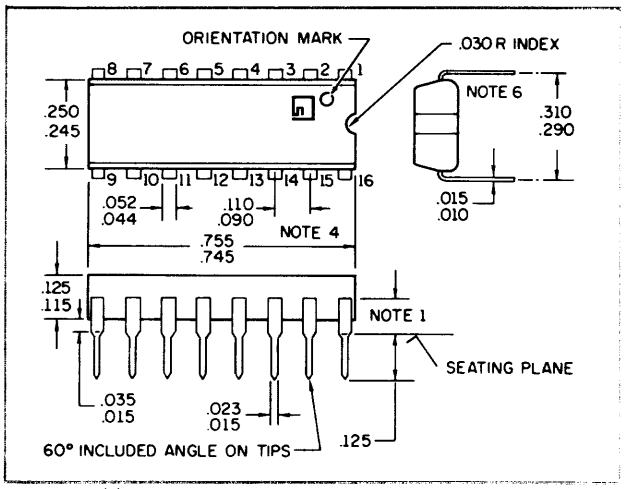


380A
QUAD 2-INPUT NOR GATE

A-PACKAGE



B-PACKAGE



NOTES:
(1) Lead spacing shall be measured within this zone.
(2) Molded Plastic Body.
(3) Kovar Leads.
(4) Lead spacing tolerances are non-cumulative.
(5) Thermal resistance from junction to still air, $\Theta_{J\text{-}A}$ = 0.16°C/mW.
(6) Leads shown as positioned by Signetics dual in-line package carrier.
(7) All dimensions of plastic package exclude molding-caused flash.

UTILOGIC II CIRCUITS

UTILOGIC II inputs are classified as sink loads and source loads by the direction of current flow required to activate the input. The input of the OR and NOR gates are called source loads because they must be driven by a source of current, e.g., the output of a UTILOGIC II element in the "1" state or a connection to the positive supply. The inputs of the AND gates and the Binary are called sink loads because they must be driven from a current sink; for example, the output of a UTILOGIC II element in the "0" state or a connection to ground.

In this publication, and all other UTILOGIC II literature, the convention of positive logic, i.e., the positive level is "1", has been assumed. If the negative logic notation is assumed (most negative level is "1"), the AND, OR, and NOR gates become OR, AND, and NAND respectively.

The characteristic curves presented in the various sections are designed to allow the system designer to predict system performance characteristics for various operating conditions. In general, characteristics are normalized to the conditions of the specification sheets. The use of the normalized characteristic is a definite design aid in that it is usually the change in the characteristic as a result of a change in the parameter that is of interest.

As long as the effects, e.g., $\frac{\partial V_{sat}}{\partial Temp.}$, are small, the total effect may be predicted by taking the product of the individual effects.

Throughout the discussion that follows, V_{CC} is assumed to be 5.0V unless otherwise specified.

UTILOGIC II AND Gates

The UTILOGIC II AND gates 305 and 306 are fabricated from the same basic chip, and therefore have identical electrical characteristics. The internal connection pattern is varied to produce a single 6-input AND gate in the 305, and the dual 3-input AND gates in the 306.

CIRCUIT DESCRIPTION

Schematic diagrams of the UTILOGIC II AND gates are shown in Figures 1 and 2. The multiple-emitter input structure provides the same function as a Diode AND gate. The output-emitter follower provides the current gain necessary for high fan-out, and also reduces the offset voltage associated with Diode AND gates. The emitter follower provides a low output impedance to effect fast response on "0" to "1" transitions and the current gain necessary for source current fan-out. The input transistor and connecting diode provide a low impedance circuit to maintain good response on "1" to "0" transitions.

Input Characteristics

The input of the AND is defined as a standard UTILOGIC II sink load. The standard sink load may be simulated by 2 kohm resistor with a series diode to the supply voltage. The input impedance of UTILOGIC II AND gates

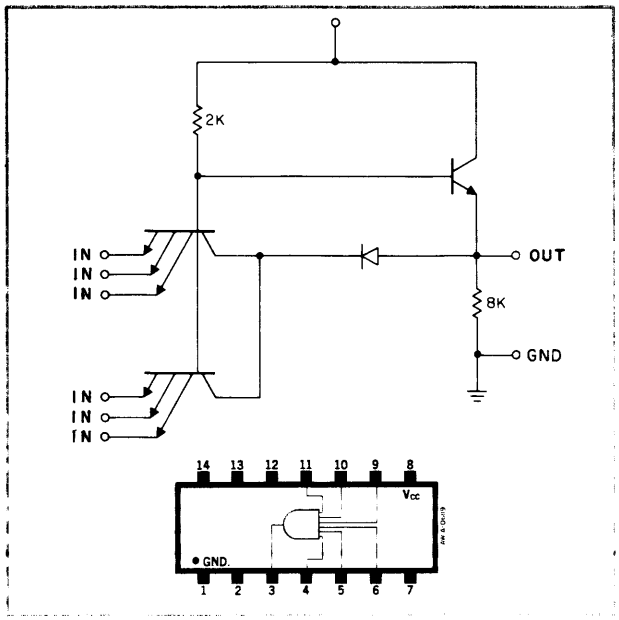


Figure 1 305 6-Input AND Gate

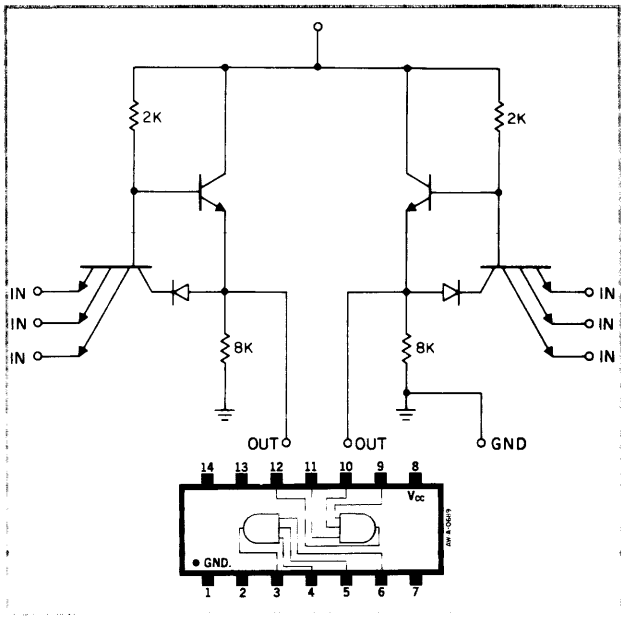


Figure 2 306 Dual 3-Input AND Gate

is low enough so that unused inputs may be left open without degrading circuit performance (open inputs are logical "1") however; it is recommended that unused inputs be connected to the used inputs of the circuit. Connecting the unused inputs to used inputs of the same circuit will not increase the circuit loading. The effect of the added capacitance will be negligible.

Output Characteristics

The fan-out of the UTILOGIC II AND gate is 10 to standard UTILOGIC II source loads. The AND gate does not have output current sinking capability; therefore, it cannot drive sink loads. The AND gate can drive any of the UTILOGIC II source loads. The AND gate outputs should not be paralleled with the outputs of any other circuits as in collector logic configurations. However, outputs of AND gates may be connected to increase fan-out if the inputs of the two circuits are in common.

Characteristic Curves

The following characteristic curves are normalized, when applicable, to the standard data sheet conditions.

Figure 3 shows the test circuit and definition of T_1 and T_2. The switching times (T_1 and T_2) of the UTILOGIC II AND gates are shown as a function of load capacitance, fan-out, supply voltage, temperature, and load resistance.

The input current versus input voltage relationship shown in Figure 4 is vital at interfaces and also allows computation of margins at non-standard conditions of fan-out.

Offset voltage, which is defined as the input voltage minus the output voltage, is shown in Figure 4F as a function of temperature. Full rated load current is applied to the outputs. Input voltages correspond to worst case UTILOGIC II or Binary Element "1" and "0" output voltage levels.

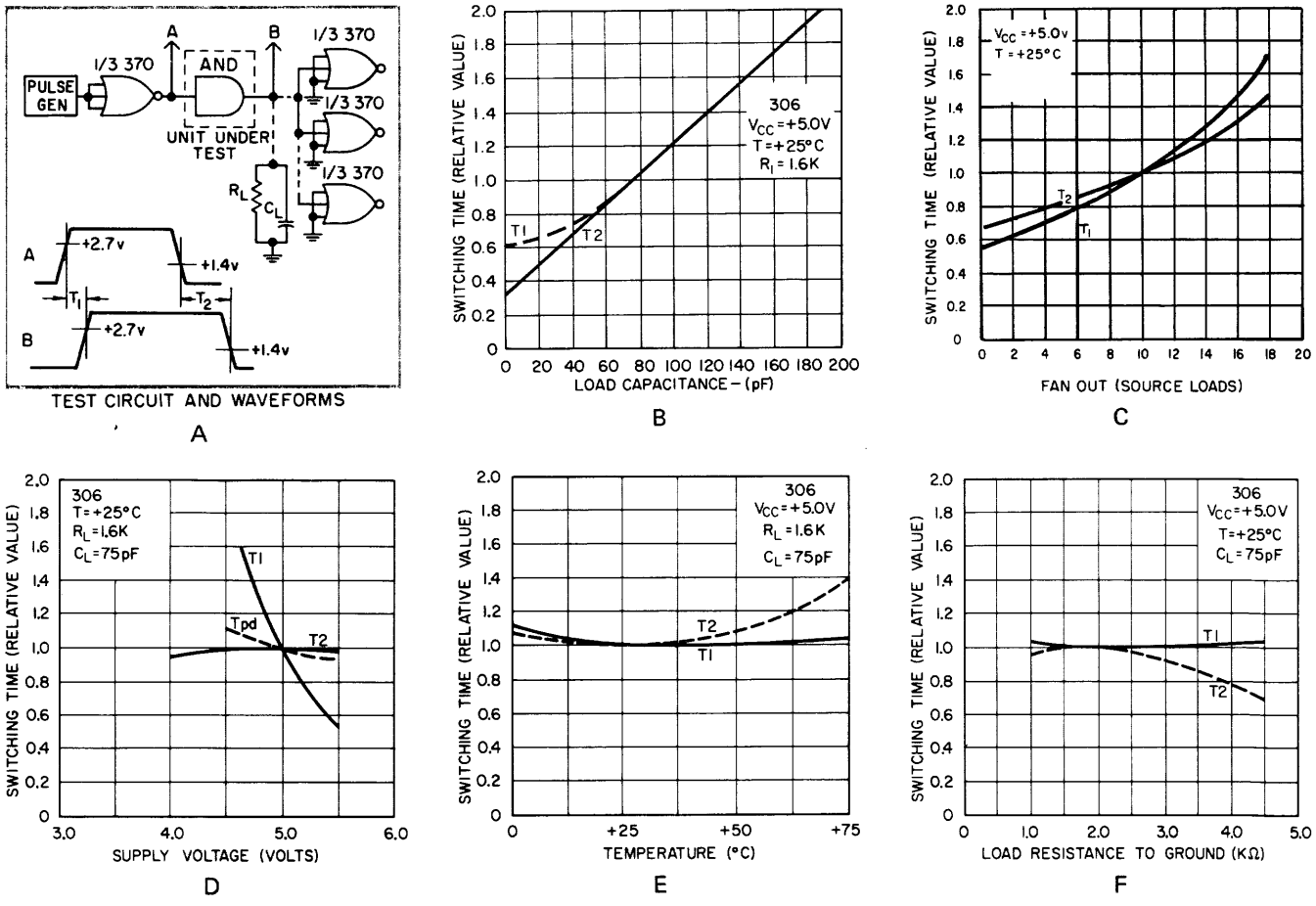


Figure 3 AND Gate Switching Characteristics

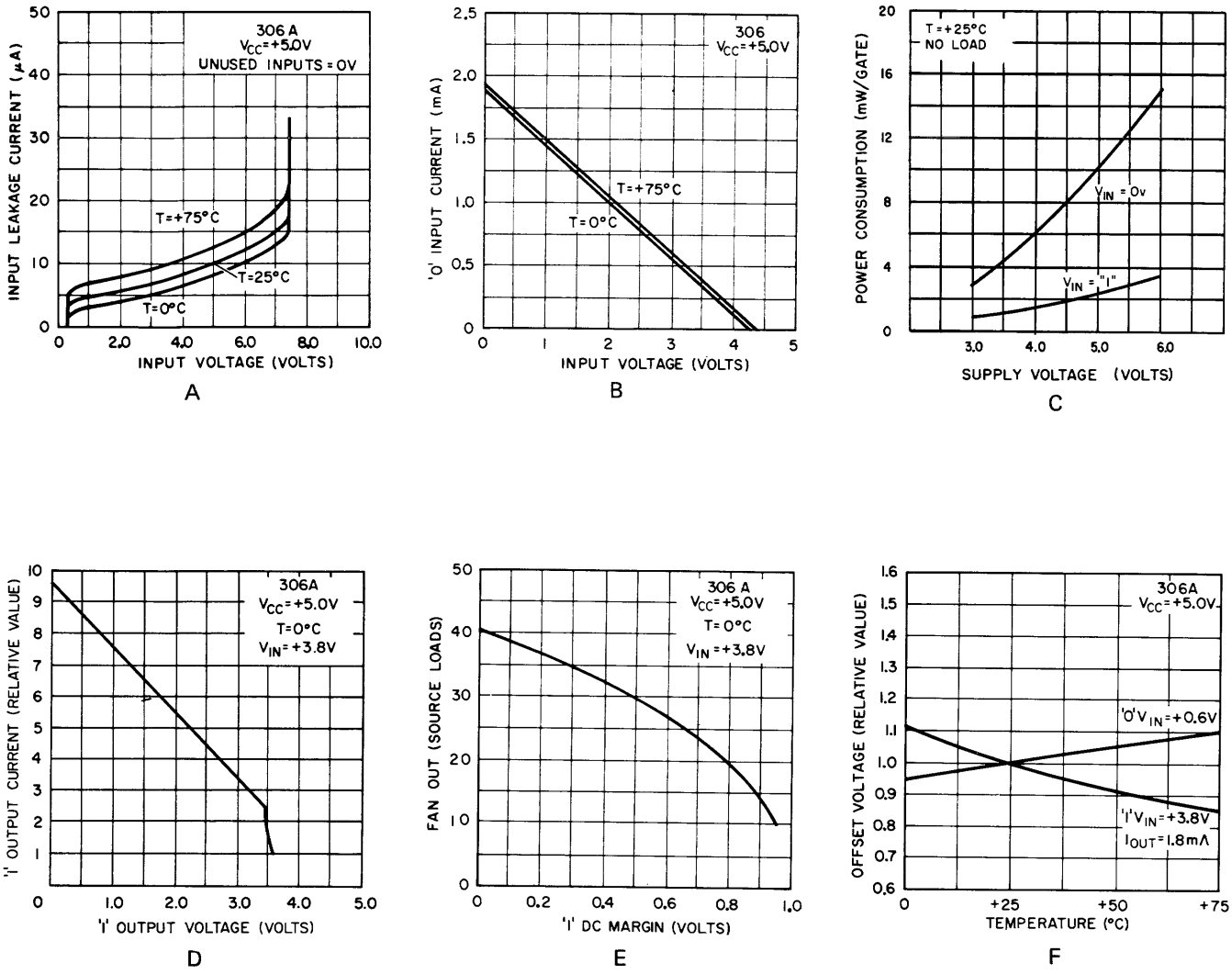


Figure 4 AND Gate DC Characteristics

UTILOGIC II NOR Gates and Expander

The UTILOGIC II NOR gates (314, 370, and 380), Expandable NOR gate (317) and Expander (300), are all derived from the same basic circuit chip to ensure full compatibility of the Expandable Gates and Expander, and to give all the circuits identical electrical characteristics. However, the 300 and 317 will have longer turn-off delay times (T_2) because of the additional capacitive loading on the expansion input. Turn-on delays (T_1) are not sensitive to this capacitance because the source impedance is low during turn-on.

The 300 Expander circuit is characterized in terms of its operation in conjunction with the 317 Expandable NOR and 333 Expandable OR. The ways in which 300 and 317 (as well as 300 and 333) compatibility is guaranteed are of interest. The expansion forward voltage for the 300 and the expansion input voltage of the 317 are measured under the same conditions, and the same limits are guaranteed. In addition, the 300 input leakage current and the 317 "0" input current specifications guarantee reverse current compatibility. These specifications assure the user that the 300 and 317 or the 300 and 333 combination will have the same DC characteristics as when the 317 or 333 is used alone. AC characteristics are shown later (with the 317 and 333 curves) as a function of the capacitance on the expansion input.

CIRCUIT DESCRIPTION

The UTILOGIC II NOR gate (Figures 5, 6, 7, and 8) may be considered as a derivation of the DTL NOR gate. The input diodes of the DTL NOR were replaced with

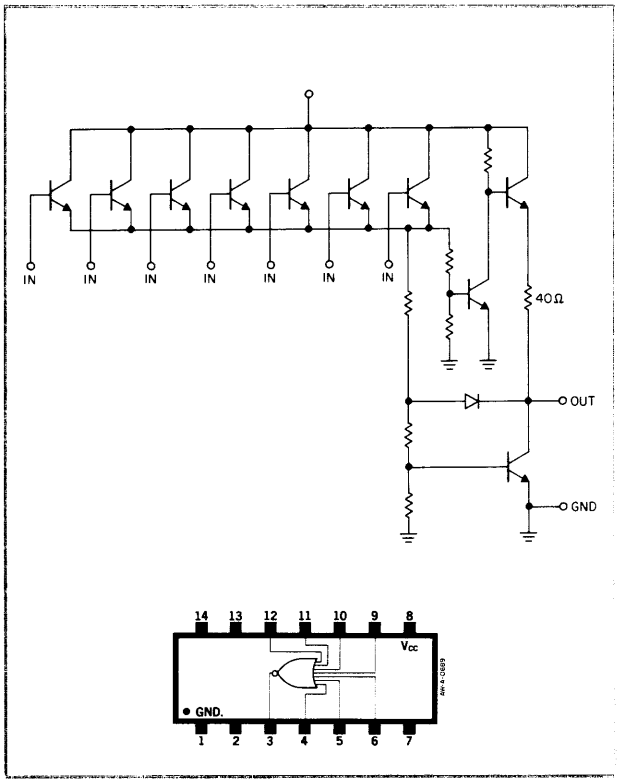


Figure 5 314 7-Input NOR Gate

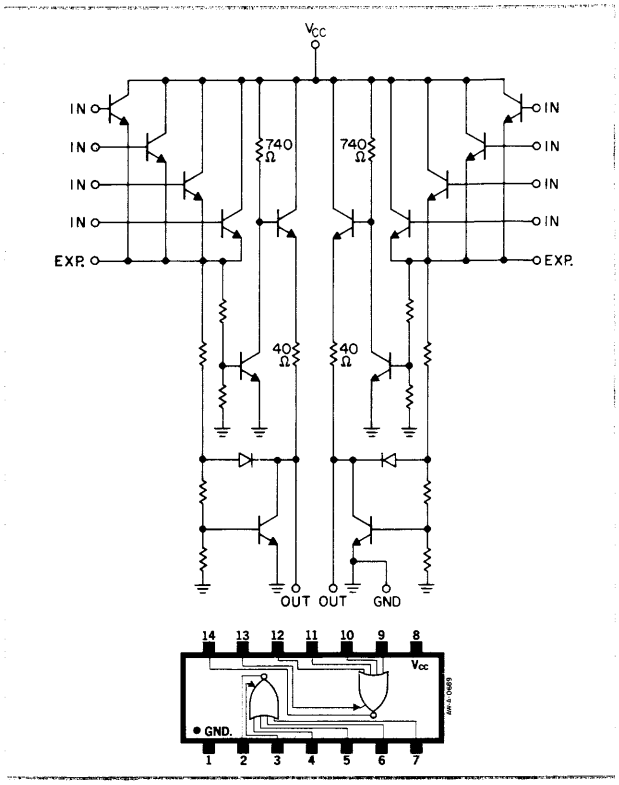


Figure 6 317 Dual 4-Input Expandable NOR Gate

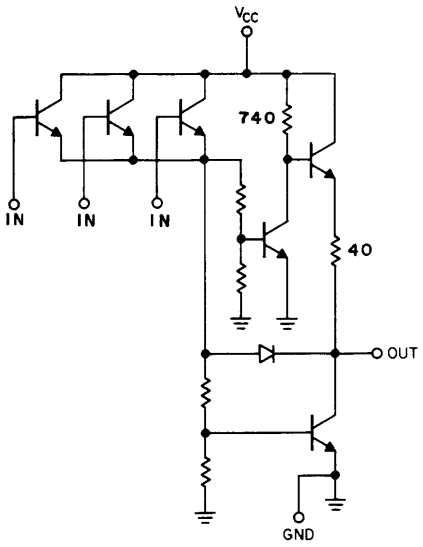
transistors to decrease the input current to allow larger source fan-out capabilities from the NOR and other circuits in the family. The NOR employs a totem-pole output to obtain low output impedance in both the "1" and "0" states. The switching thresholds are determined by the ratio of the coupling resistance to the pull-down resistance at the base of each switching transistor. The series resistor at the output provides current-limiting should the output become accidentally shorted to ground. The Expandable NOR is implemented by connecting the common emitters of the input transistors to an expansion input. The Expander (Figure 9) is a dual array of input transistors; thus, the effect of connecting the Expander output to an expansion input is the same as connecting more input transistors in parallel.

Input Characteristics

The Standard UTILOGIC II Source Load is the NOR input. The Standard Source Load may be simulated by a 10 kΩ resistor and 2 series diodes to ground. An unused NOR input should be tied to ground through a resistance of 60 kΩ (or less) or connected in common with a used input on the same circuit. The capacitance of an open input may become charged during prolonged "1" levels at a driven input. When the driven input goes from "1" to "0", the charged capacitance discharges into the input and gives the effect of a slow circuit. Two or more common inputs represent the same DC load as a single input since the "1" input current is determined by the voltage across the coupling resistors and the gain of the input transistors. Neither of these values changes appreciably when inputs are connected in common. The additional capacitance of a commoned input has no measurable effect on switching times. Input voltages should not exceed the supply voltage unless precautions are taken to limit the resulting current in the collector-base junction of the input transistor to 30 mA.

Output Characteristics

A UTILOGIC II NOR gate has a fan-out of 5 sink loads and 11 source loads. All 16 loads may be connected simultaneously because they do not interact. Because the NOR gates employ transistors for both pull-up and pull-down, their outputs cannot be connected in parallel with the output of any other independent circuit (collector logic). Parallel operation of an active device with another device may result in ambiguous output voltages and/or excessively high currents if one device should attempt to reach a "1" level while the other is attempting to reach a level "0". However, two NORs in the same package may be connected with common inputs and common outputs. In this case, fan-out is doubled and the input loading is two Standard Source Loads.



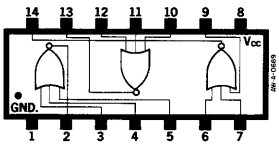
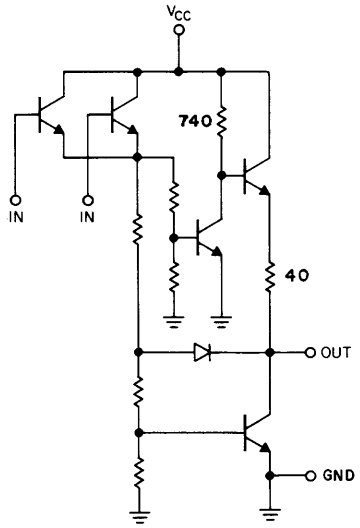


Figure 7 370 Triple 3-Input NOR Gate



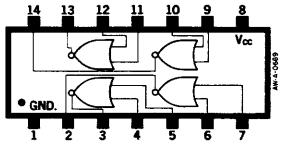
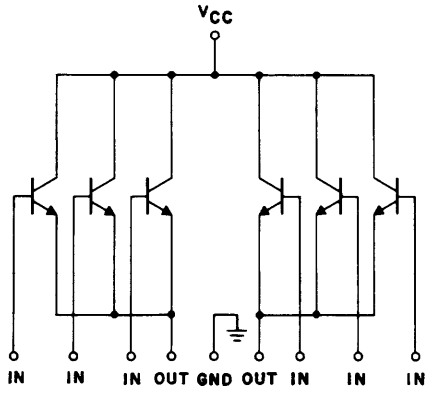


Figure 8 380 Quad 2-Input NOR Gate



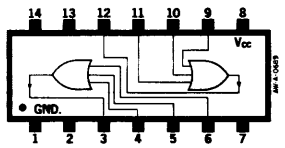
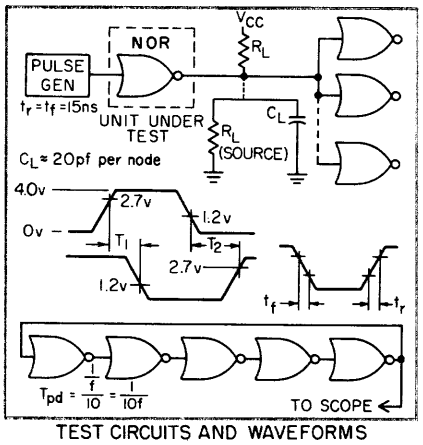
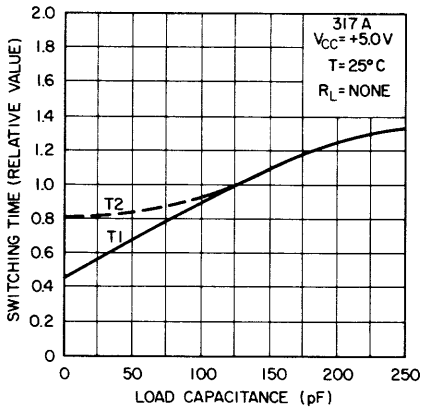


Figure 9 300 Dual 3-Input EXPANDER

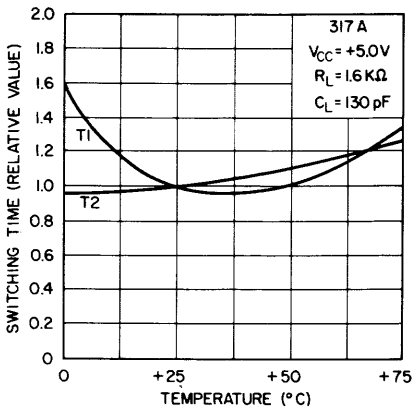


TEST CIRCUITS AND WAVEFORMS

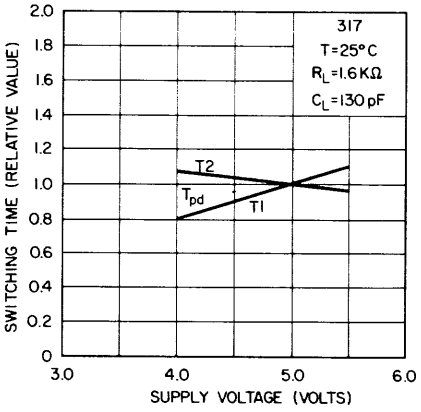
A



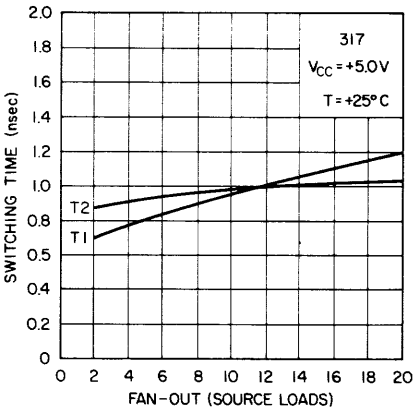
B



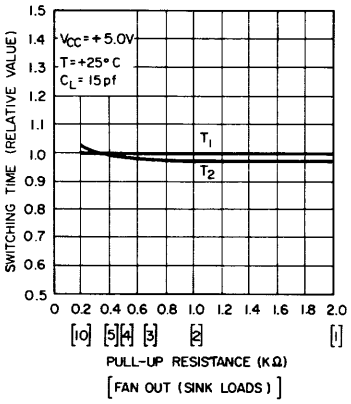
C



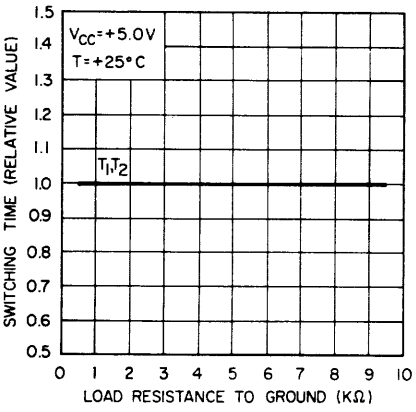
D



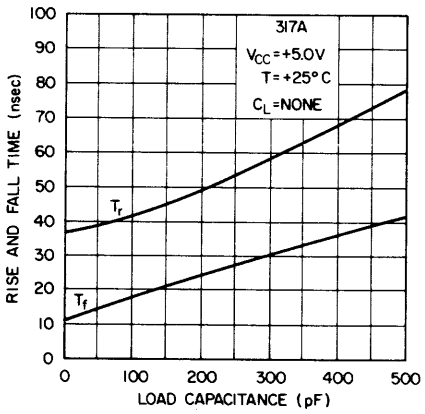
E



F



G



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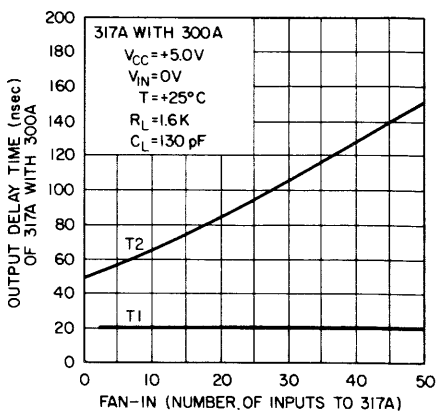


I

Figure 10 NOR Gate Switching Characteristics

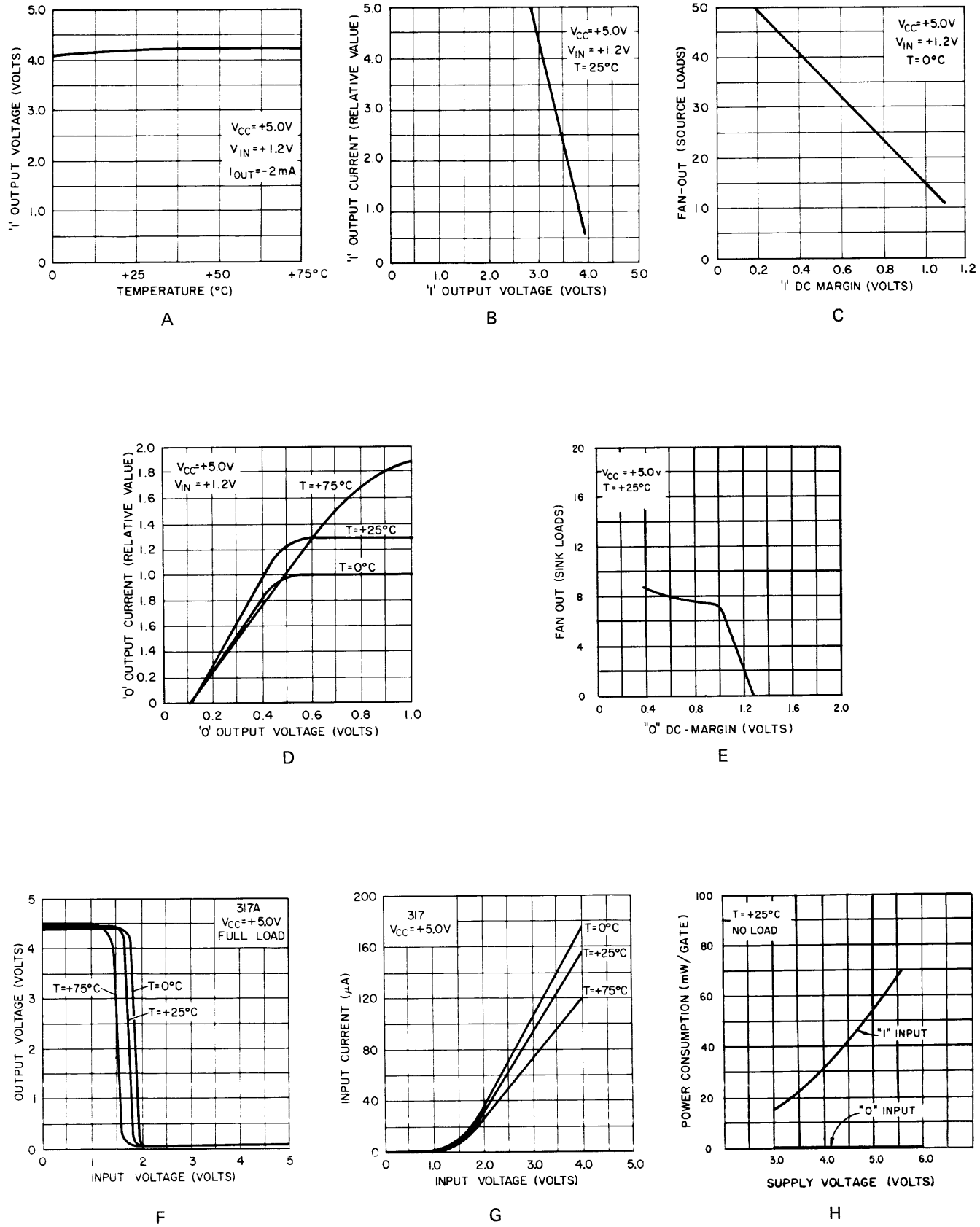


Figure 11 NOR Gate DC Characteristics

UTILOGIC II OR Gates

The UTILOGIC II Expandable OR gate is compatible pin-for-pin with the UTILOGIC II NOR gates and Expandable NOR gate respectively, and therefore simplifies system design, layout and checkout.

Comparison of the schematics of the UTILOGIC II OR gate (Figure 12) and the UTILOGIC II NOR gate (Figures 5, 6, 7, and 8) shows that both types of gates have essentially identical input and output structures; however, the OR gate uses one more transistor to obtain the additional inversion required to produce an OR gate from the basic UTILOGIC II NOR configuration.

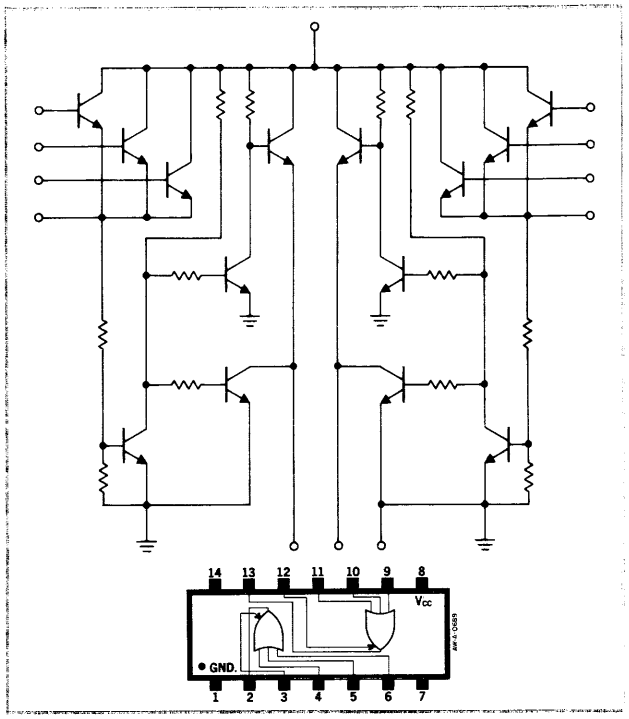


Figure 12 333 Dual 3-Input Expandable OR Gate

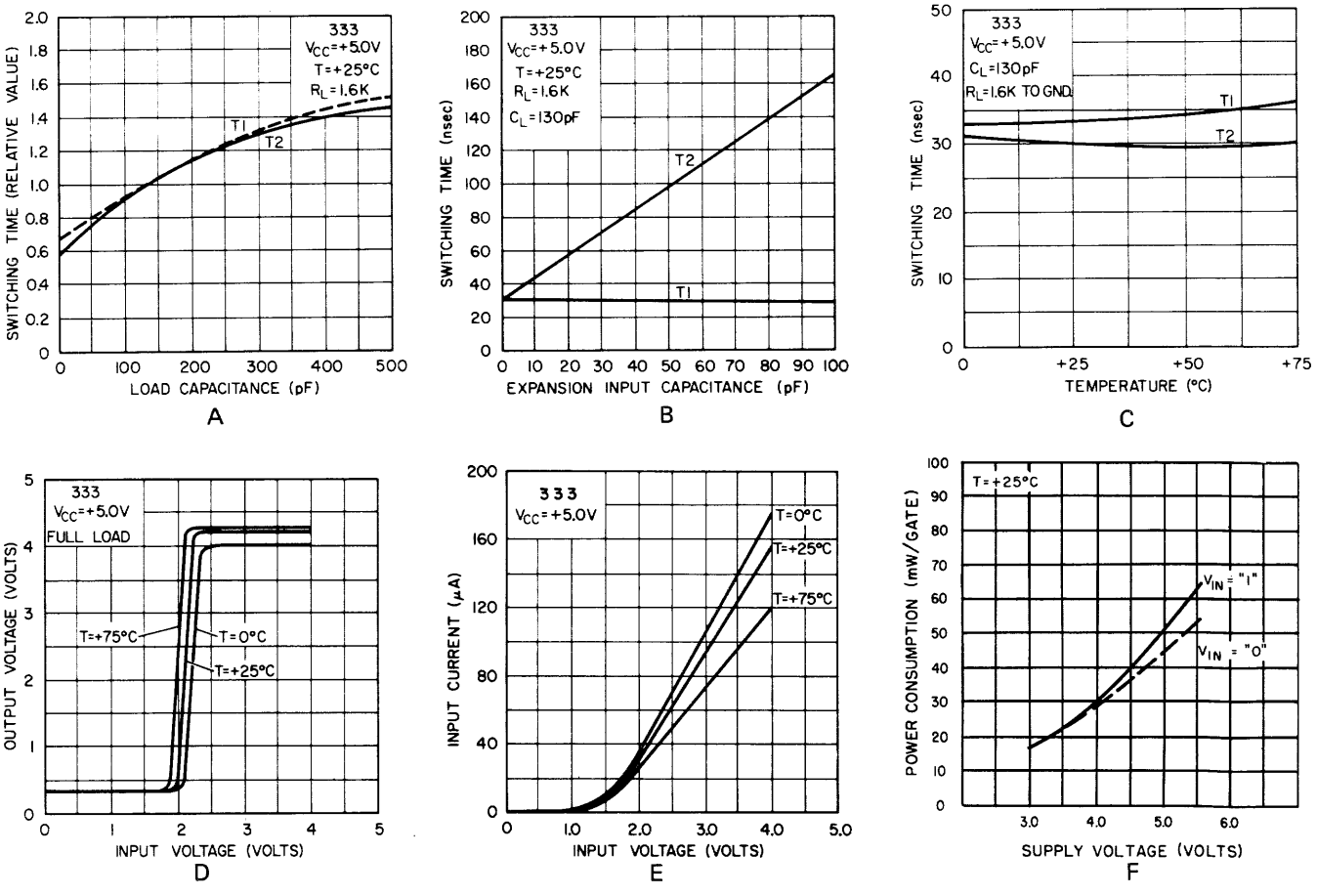


Figure 13 OR Gate Characteristics

UTILOGIC II J-K Binaries

The UTILOGIC II 321 and 322 are dual J-K general purpose binaries with both synchronous and asynchronous inputs. They employ DC level triggering with clocking effected on the negative-going edge of the clock pulse waveform.

CIRCUIT OPERATION

The 321 and 322 have the following output sequence:

1. With clock pulse low, the logical inputs are disabled and the slave is connected to the master.

2. At the rise of the clock pulse the slave is disconnected from the master and the logical inputs are enabled. Data now enters the master setting it to the state determined by the logical inputs.

3. At the fall of the clock pulse the logical inputs are disabled to prevent entry of further information and the slave is connected to the master. The slave now takes the state of the master and state of the slave appears at the outputs. The J and K inputs of the 321 and 322 are non-inverting, that is the flip-flop will be set at "1" when the J input is high and the K input is low. The asynchronous inputs are inverting, that is actuated by logical "0". The effect of the asynchronous inputs is independent of the state of the clock line.

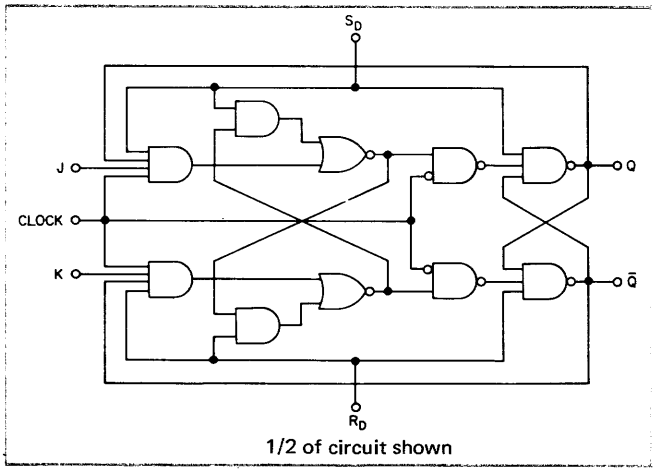


Figure 14 321 and 322 Logic Diagram

Note that mounting of the 322 package can be facilitated by turning the package 180° so that the ground pin is on the ground buss side, and the V_{CC} pin is on the V_{CC} buss side.

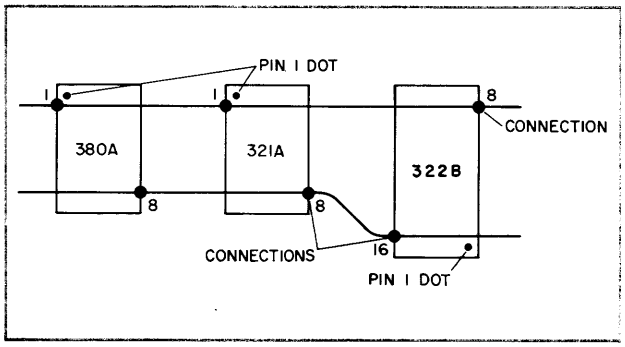


Figure 15 322 Package Mounting

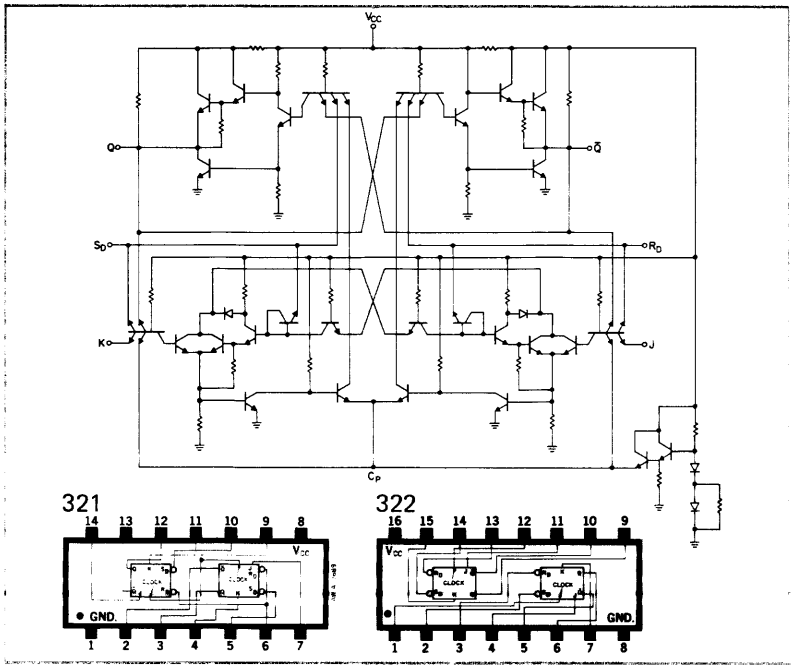


Figure 16 321, 322 Schematic Diagram

J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

S_D	R_D	Q
0	0	*
1	0	0
0	1	1
1	1	No change

*Both Q and $\bar{Q}$ in "1" state.

Figure 17 321 and 322 Truth Tables

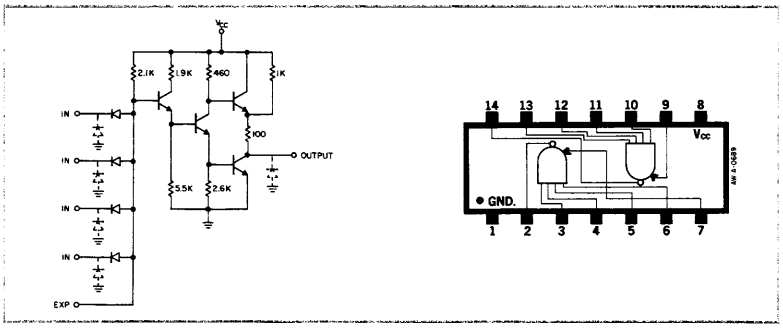
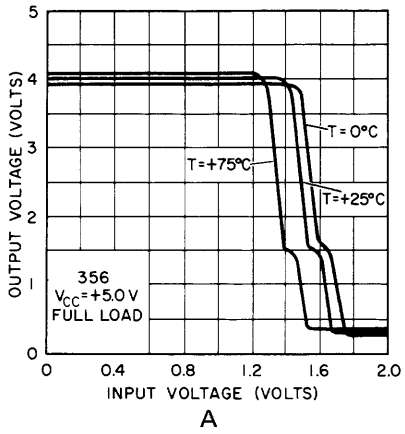
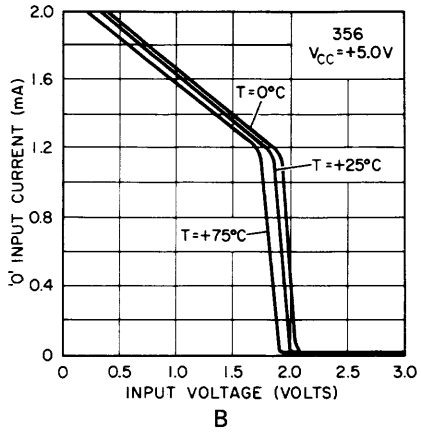
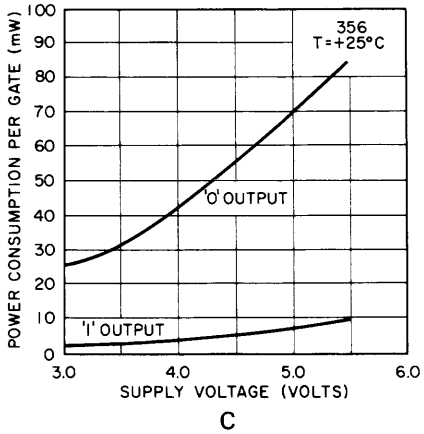
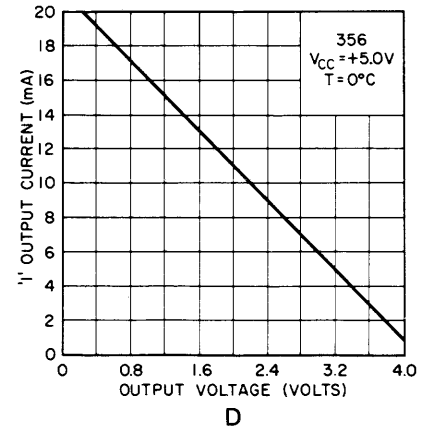


Figure 18 356 Dual 4-Input Expandable Line Driver









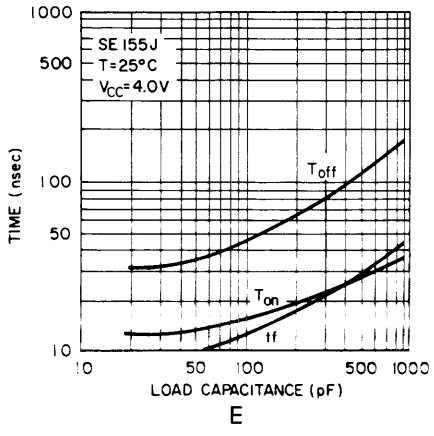


Figure 19 356 Line Driver DC Characteristics

UTILOGIC II Line Driver

The UTILOGIC II 356 Line Driver is shown in Figure 18. It is intended for driving the clock and RESET lines of the 321 and 322 J-K binaries. The "1" level output impedance of the driver is approximately 150 ohms for output voltages less than one diode drop below V_{CC}. It should also be noted that the use of active outputs for both the "1" and "0" states means that the output of these drivers cannot be connected in parallel with any other element. However, for those cases where high fan-out is required, but absolutely no clock skew can be allowed, the two line drivers in one package may be tied in parallel if the inputs also are made common. DC and switching characteristics for the 356 are shown in Figures 19A through 19E.

HOW TO DESIGN WITH UTILOGIC II

Information in this section gives examples of efficient system design with UTILOGIC II integrated circuits. The use of the characterization curves presented earlier for each UTILOGIC II circuit will be demonstrated here.

Interfacing is discussed, including the interconnecting of UTILOGIC II and other circuit types. Typical interfacing techniques are illustrated.

Some of the features of UTILOGIC II that make the family especially interesting to the systems engineer are:

1. High noise immunity, a major design consideration where application may be in high ambient noise environments that are encountered in industrial control equipment, computer peripherals, etc.

2. Low output impedance, essential for good noise immunity, also provides high DC fan-out capabilities. Switching times are relatively unaffected by the increased load capacitance associated with high fan-outs or long inter-connecting lines.

3. Single power supply to provide economy in power supply costs. Tolerance to voltage variations (±5 percent) permit the use of simply regulated supplies for further economy.

All members of the UTILOGIC II family have built-in protection against damage produced by momentary short circuit conditions, valuable during debugging or trouble-shooting procedures. Any input or output connection of any UTILOGIC II element may be connected to the input, output, supply voltage, or ground connection of any other UTILOGIC II element momentarily, without producing damage to either circuit. It is not recommended that UTILOGIC II elements be connected so that they produce conditions designated as abnormal for periods of time that can be measured in seconds. If the devices are required to operate for extended periods of time under other than recommended conditions, precautions should be taken to limit the current to safe values within the device's dissipation capabilities.

General Design Considerations

The normal good design practices that are commonly used in layout of networks of any digital circuit family should also be applied to UTILOGIC II networks. Although all of the UTILOGIC II elements have excellent noise margins, any circuit, discrete or integrated, will produce erroneous results if the noise levels become high enough. As in any system, ground, DC distribution, and noise problems should be considered from the very beginning of the design.

A major consideration with integrated circuits is the higher packaging density, as compared to discrete devices. For example, a printed circuit board that held 3 or 4 discrete flip-flops can now hold 30 to 40 integrated flip-flops; the design of the DC and ground distribution systems must allow for the corresponding current increases. DC and ground lines should be kept as short as possible and of adequate cross-section, and the use of tantalum or other high-frequency type by-pass capacitors is recommended.

The effect of the high circuit density on system cooling requirements and the increased possibility of localized hot spots must also be considered.

Signal leads should be kept as short as possible to minimize cross-talk, noise pick-up, and propagation time down the wire.

Generally, it becomes important to terminate signal lines when the signal propagation time down the wire becomes appreciable as compared to the signal transition times. Since UTILOGIC II rise and fall times are on the order of 10 ns, lead lengths of 2 to 3 feet should not require any special termination. The simple termination network shown in Figure 20 has been found effective at any UTILOGIC II input with lines up to 12 feet in length, and with coaxial cable as well as open wire.

When using a clock distribution system which has several branches, all flip-flops should be driven from the same relative position on the branches. In addition, the clock drivers should be as close as possible to the flip-flops that they will trigger so that the driving lines are short and uniform in length.

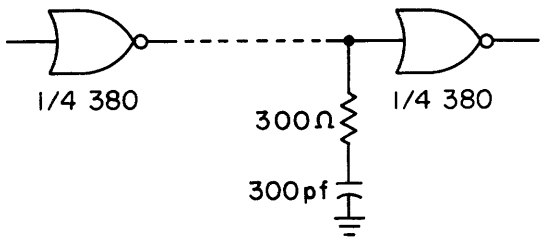


Figure 20 Termination Network

Interfacing Considerations

GENERAL CONSIDERATIONS

The need to interface UTILOGIC II integrated circuits with discrete component circuitry or with integrated circuits of another family may arise when a UTILOGIC II system or subsystem is added to or must operate with existing hardware. General rules when interfacing are:

1. Inputs to UTILOGIC II source loads must be capable of supplying 180 μA input current at the "1" input threshold voltage of at least 2.7 volts.

2. Inputs to sink loads must be capable of sinking 2.5 mA at the "0" voltage (0.6V).

3. A UTILOGIC II output will supply 2 mA at 3.8 volts for NOR and OR gates; it will supply 1.6 mA at 3.8 volts for binaries; and 1.8 mA at 3.8 volts for ANDs.

4. The approximate equivalent circuit for any UTILOGIC II output at "1" is 100 ohms to 4.0 volts. A NOR, OR and binary output will sink 12.5 mA at 0.6 volts or less.

UTILOGIC II AND DTL

A UTILOGIC II-to-Signetics 100 or 600 series DTL (DTL in general) interface requires, at most, modification of load definitions. The input resistor of the DTL NAND gate and the UTILOGIC II AND are approximately the same value so that the DTL load is equal to a UTILOGIC II sink load. The "1" and "0" levels at UTILOGIC II outputs are fully compatible with DTL input requirements and vice versa.

DTL elements that have resistively loaded outputs generally have fan-outs of 2 to UTILOGIC II source loads. Higher source load fan-out can be obtained by providing 8 k of pull-up resistance (1/4 DTL load) for each additional source fan-out required. A UTILOGIC II AND gate may be used as a high-fan-out buffer.

Mixed UTILOGIC II – DTL systems should operate with a 5.0 volt power supply; the rules above assume a common power supply.

UTILOGIC II TO RTL

The Resistor-Transistor (grounded-emitter transistor amplifier) logic stage, Figure 21, is often employed as a level translator or general purpose buffer stage since all that is required generally is one transistor and one or two resistors. At these interfaces, the output of a UTILOGIC II element may be treated as a voltage source of 4.0V (less than 100 ohms source impedance). For a typical input current requirement of 0.5 mA, R_{IN} in Figure 21 will be 5 kΩ.

MISCELLANEOUS INTERFACES

For applications where input "1" levels are higher than UTILOGIC II "1" levels ("0" voltages about equal), several interfacing possibilities exist. A UTILOGIC II AND gate may be used as a buffer by using a series diode (d) to improve the input breakdown voltage (see Figure 22). The external resistor, (R), may be used to improve the "0" offset voltage, thereby compensating for the voltage rise across the diode (each 20 kΩ load reduces fan-out by 1). High conductance diodes are recommended to keep the input voltage as low as possible.

Interfacing high "1" voltage outputs to UTILOGIC II source load inputs may be accomplished by techniques such as those in the following four examples. In Figure 23, the forward voltage of one or more diodes is the voltage dropping medium. In Figure 24, a zener diode is used when voltage drops of 5 volts or more must be obtained. The resistor, R, may be used to increase the zener current to improve its regulation. Using a zener as shown in Figure 25, may be especially desirable if the "1" level of the driving source has large variations. In Figure 26, a simple resistive voltage divider provides the necessary voltage reduction, and may be used when minor modifications to the logic levels are required and when high speeds are not necessary.

When the "1" level output of another logic circuit will not reach the required UTILOGIC II input level of 2.7 volts, the 317 or 333 Expandable gates will often provide an acceptable buffer, shown in Figure 27. Because the voltage required to switch an Expandable Gate is a "diode drop" lower at the Expansion Input than at the regular inputs, "1" levels of 2.0 volts and "0" levels of 0.8 volts are sufficient. Maximum "1" input current is 3 mA. This Expansion Input interface scheme also may be used at interfaces with Diode Logic, shown in Figure 28.

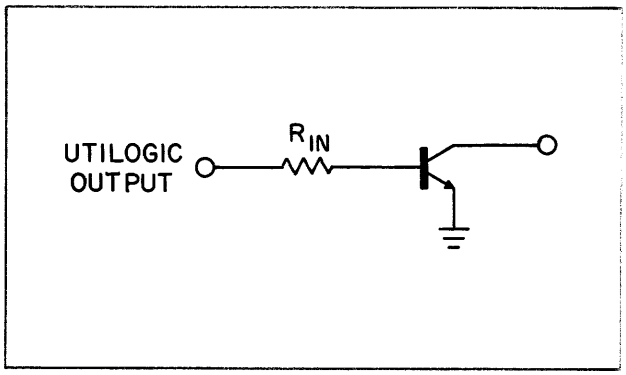


Figure 21 UTILOGIC II to RTL Interface

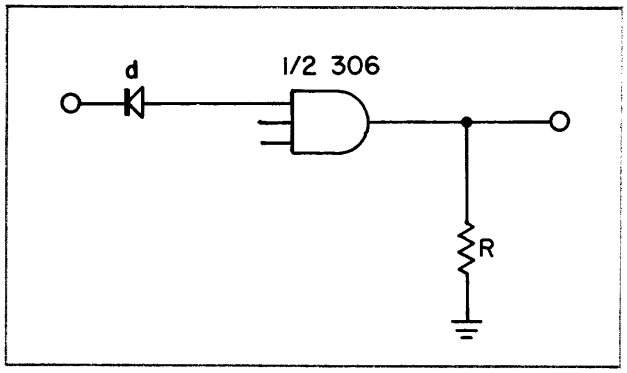


Figure 22 High Level to AND Interface

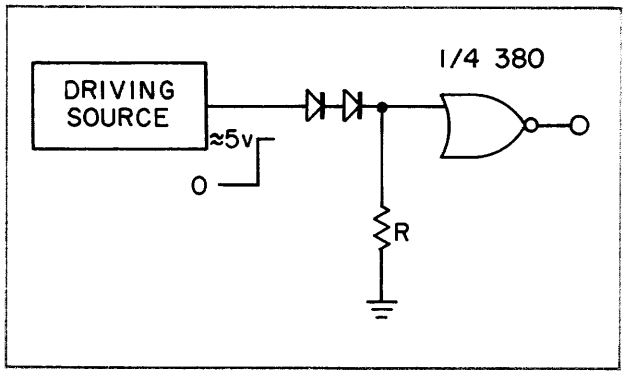


Figure 23 5 Volt to Source Input Interface

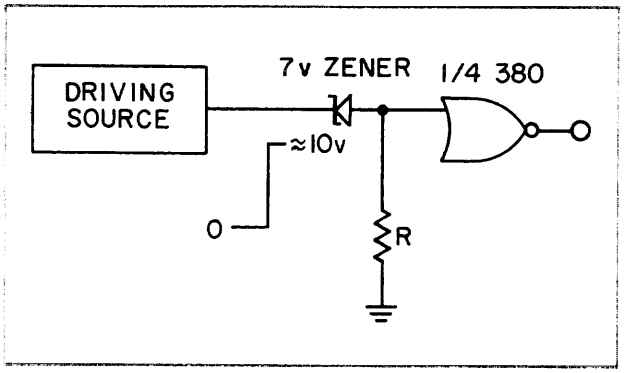


Figure 24 10 Volt to Source Input Interface

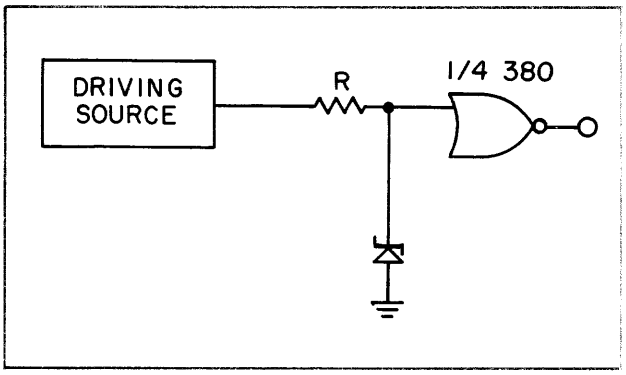


Figure 25 Interfacing with Variable Input Levels

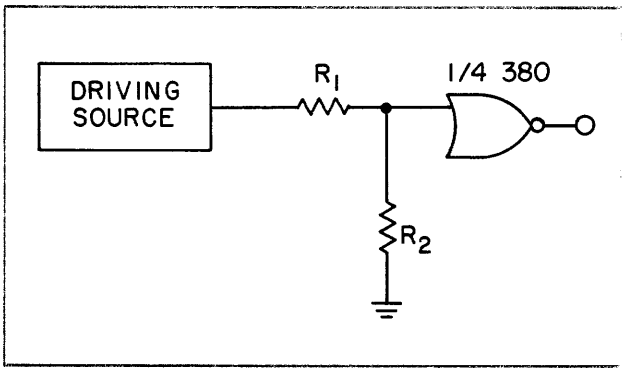


Figure 26 Resistive Interface

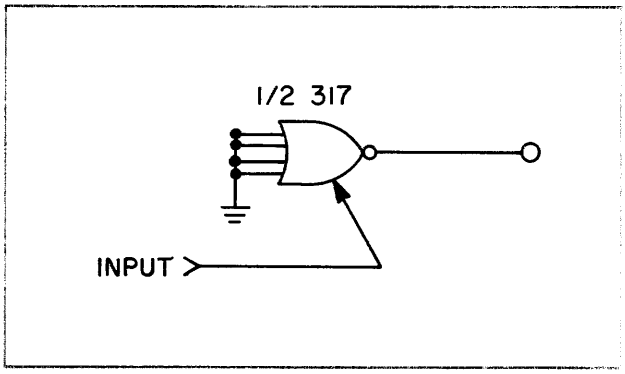


Figure 27 Low Level to UTILOGIC II Interface

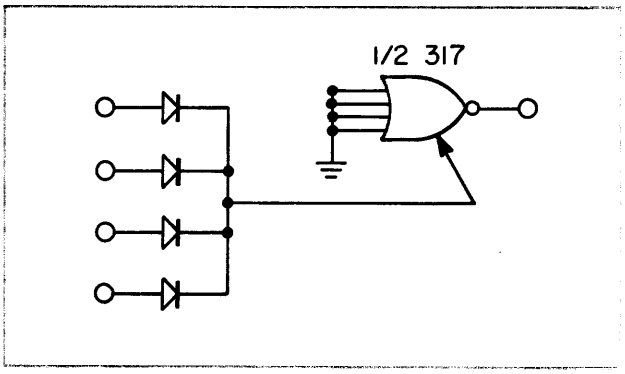


Figure 28 Diode Logic to UTILOGIC II Interface

TYPICAL APPLICATIONS OF UTILOGIC II

The examples in Figures 29 through 56 illustrate the versatility of the basic UTILOGIC II gates in the implementation of some simple logic configurations.

The Exclusive-OR (X ⊕ Y) function, shown in Figure 33 is equivalent to the statement, "f equals X or Y, but not both, or X is not equal to Y." The Digital Comparator output, Figure 34, is the complement of the Exclusive-OR output and is used to implement the function, X equals Y.

Arithmetic Functions

This subsection describes three basic arithmetic functions (Half-Adder, Full-Adder, and Full Subtractor) and illustrates their implementation with UTILOGIC II circuits.

HALF-ADDER

The Half-Adder (Figure 35) is a functional circuit for obtaining the binary sum of X plus Y. The circuit has two outputs, Sum and Carry (S and C). The Sum output is the same as the output of the Exclusive-OR circuit; the C output indicates a binary carry. A Half-Adder may be used at the lowest order position of a Parallel Adder (all bits added simultaneously) since there is no carry input to this position. Two Half-Adders may be combined to obtain a Full-Adder.

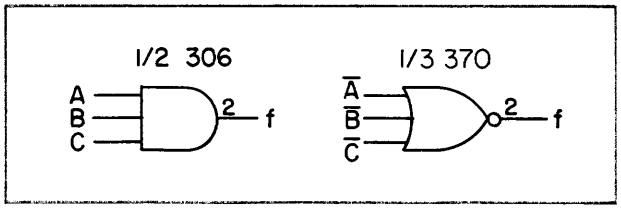


Figure 29 f = ABC

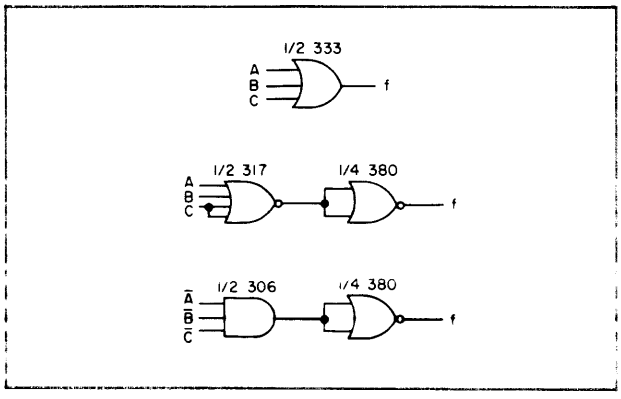


Figure 30 f = A + B + C

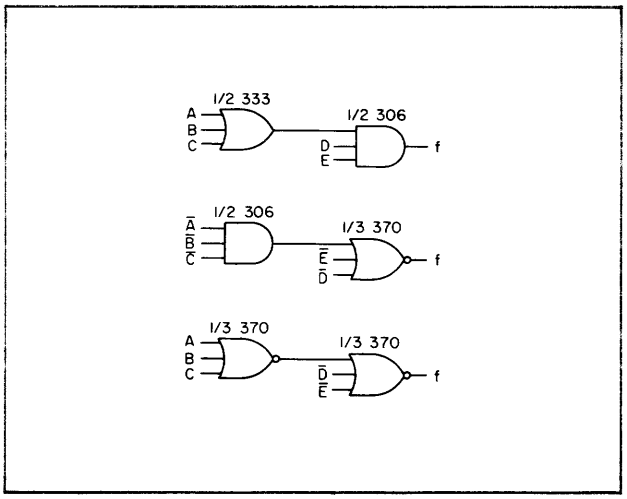


Figure 31 f = (A + B + C) DE

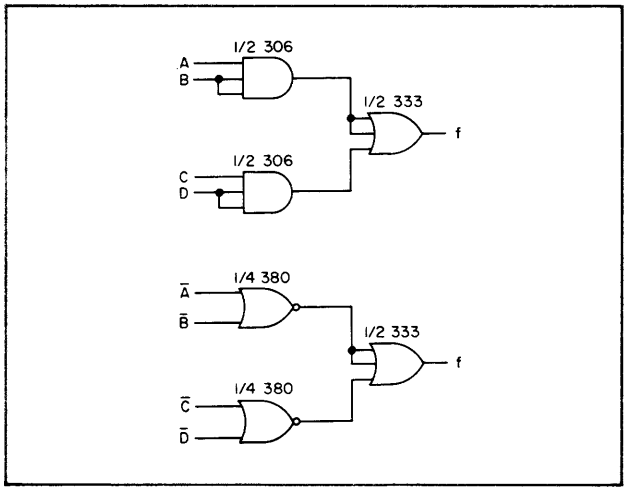


Figure 32 f = AB + CD

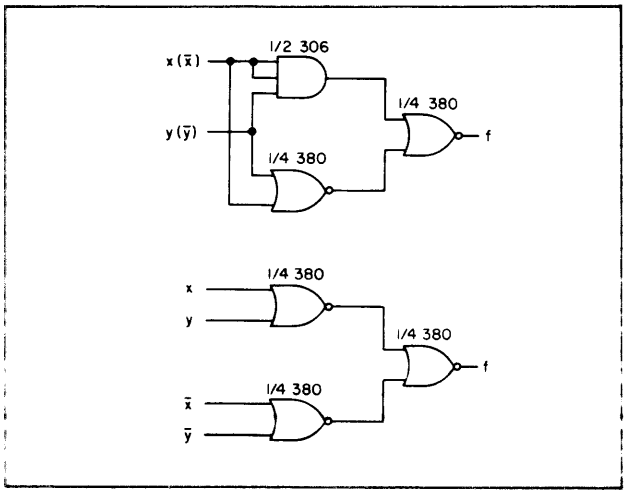


Figure 33 Exclusive-OR

FULL-ADDER

A Full-Adder (Figure 36) is a circuit for obtaining the binary sum of three binary digits, X, Y, and C (carry). The circuit has two outputs: S to indicate the sum of the three inputs and C′ to indicate the value of the resulting carry.

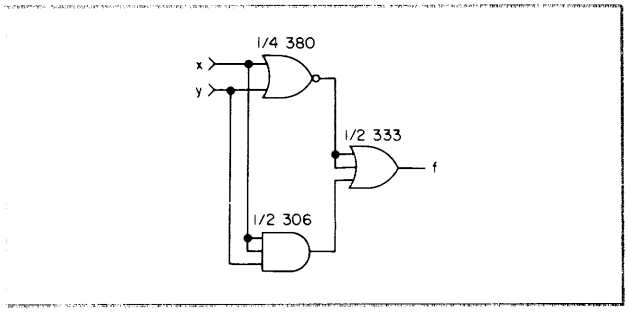


Figure 34 Digital Comparator

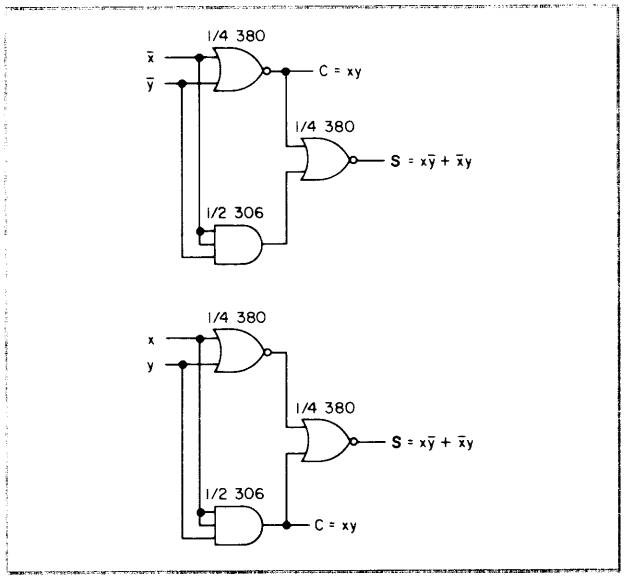


Figure 35 Half Adder

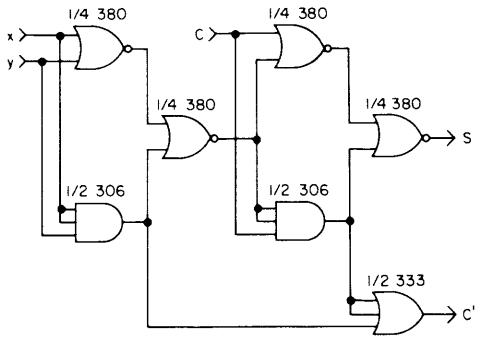
FULL-SUBTRACTOR

The circuitry to obtain the binary Difference, (D equals X minus Y minus Borrow), and B′ (new Borrow), is identical to the above Full-Adder, except that a false input and a change of output notation are required. The UTILOGIC II Full-Subtractor implementation is shown in Figure 37.

Shift Registers

A Shift Register is a circuit for storing and shifting a number of binary or decimal digits. Shift Registers frequently are used in arithmetic operations to accomplish multiplication or division; they also are used to present information in serial form for use in displays, adders, magnetic tapes, and magnetic drums. The Shift Register, shown in Figure 38, shifts its contents one position to the right upon each occurrence of the clock pulse. The input lines allow entry of new information to the first stage; the clear line will preset all of the stages to "0". A configuration is shown in Figure 39 in which information stored at $X_1, X_2 \ldots X_N$ (another shift register) is entered in parallel to register Y ($Y_1, Y_2 \ldots Y_N$) upon the command ENTER. Upon each command to SHIFT, the information stored in register Y is shifted one stage to the right. Although the parallel entry utilizes the asynchronous inputs, the entire operation is under the direct control of the clock pulse so that the operation is synchronous.

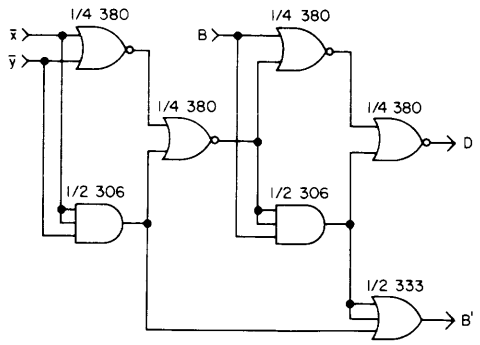
X	Y	C	S	C′
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1



$$S = C(XY + \overline{X}\,\overline{Y}) + \overline{C}(X\overline{Y} + \overline{X}Y) \qquad C' = XY + C(X\overline{Y} + \overline{X}Y)$$

Figure 36 Full Adder

X	Y	B	D	B′
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
0	1	1	0	1
1	1	1	1	1



$$D = B(XY + \overline{X}\,\overline{Y}) + \overline{B}(X\overline{Y} + \overline{X}Y)$$

$$B' = \overline{X}Y + B(XY + \overline{X}\,\overline{Y})$$

Figure 37 Full Subtractor

Counting Functions

Since many computing functions, such as indexing and program control, are essentially counting functions, a large variety of counters is used in computing equipment. Some of the more common counter types discussed in this section showing the flexibility of the UTILOGIC II family are: asynchronous ripple counters, useful for frequency division; simple synchronous counters for high-speed logic operations; reversible counters for specialized control; and feedback shift registers which are especially suited for commutation and very high-speed counting.

BINARY RIPPLE COUNTERS

In ripple counters, the flip-flop normally operates in the simple toggle mode (change with each clock pulse) with the output of each element driving the clock input of the following stage. Ripple counters operating in this manner are able to operate at higher input frequencies than most other types of counters, require no gating and few interconnections, and present only one clock input to the input line. The asynchronous Set/Reset characteristics of the 321 and 322 binaries allow the binary sequence of the simple ripple counter to be modified to arbitrary sequence lengths, many of which can be obtained without gating. A limitation of all ripple counters is that a change of state may be required to ripple through the entire length of the counter. The propagation time of this change may determine the maximum operating frequency of the modified types and will be determined when any decoding networks may be sampled. A simple Binary Ripple Counter that counts up is shown in Figure 40. Since each stage changes state (complements) on each "1" to "0" transition of the previous stage, the counter is implemented by connecting the clock input of each stage to the "Q" output of the previous stage.

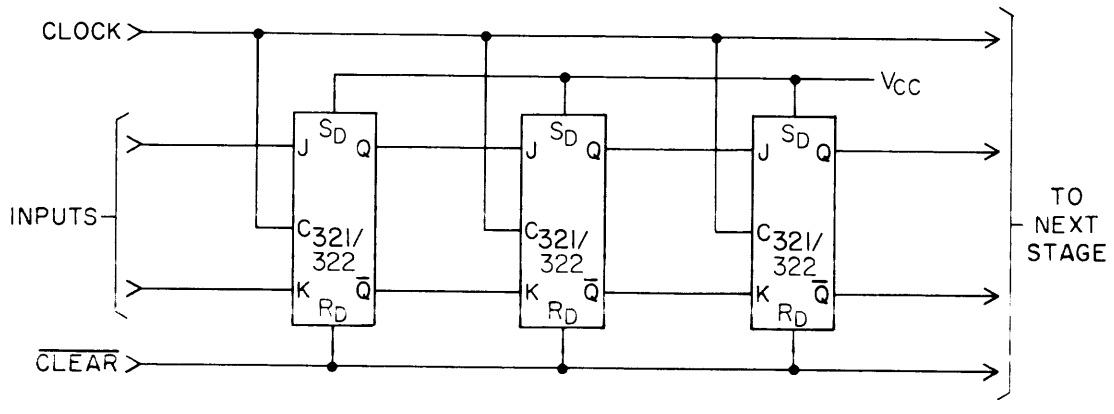


Figure 38 Serial Entry Shift Register

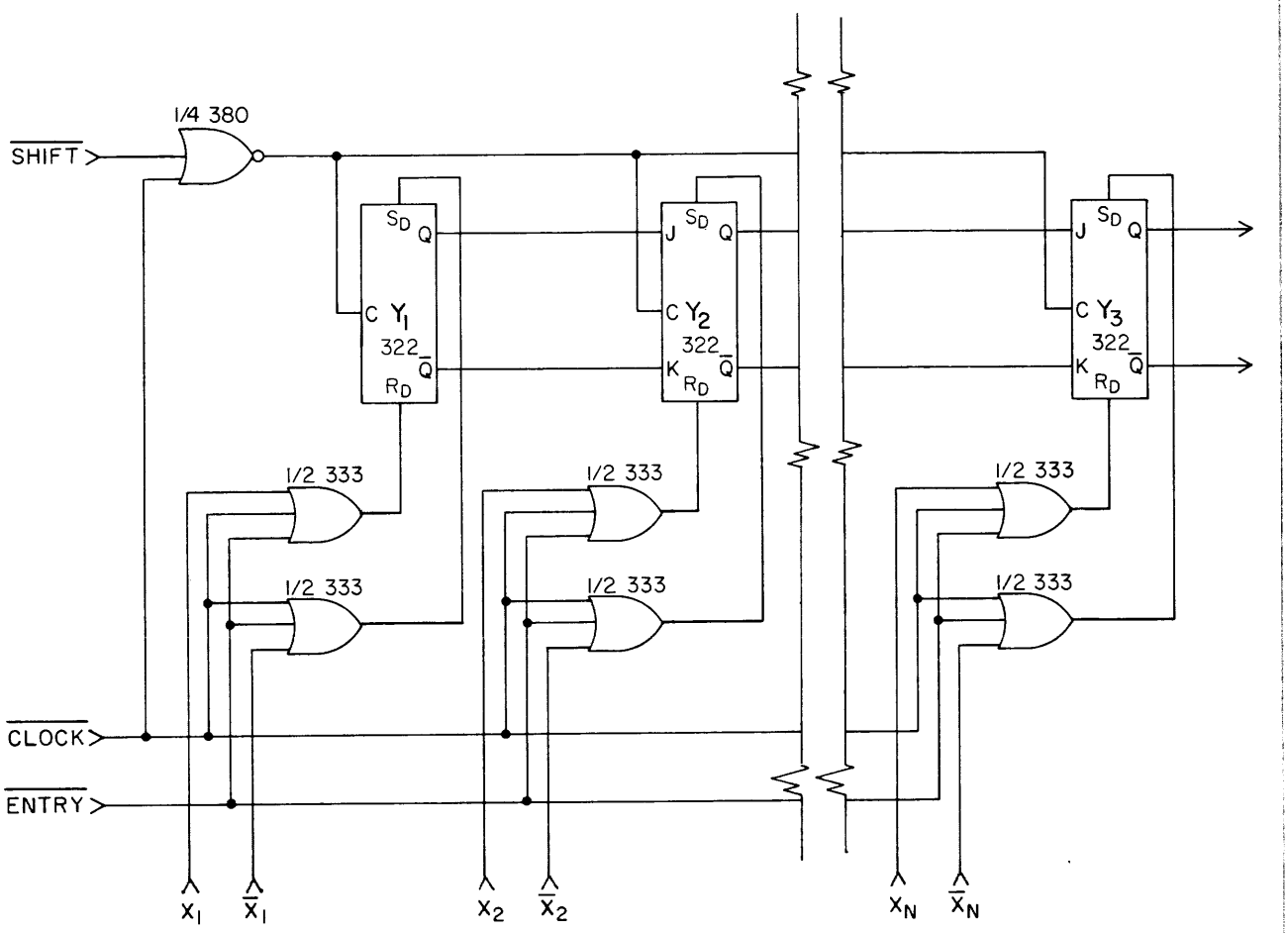
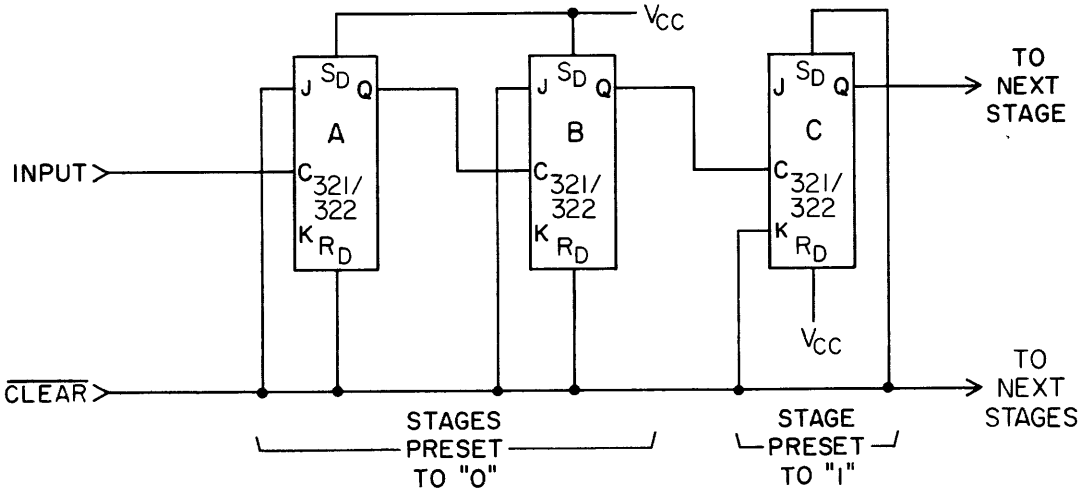


Figure 39 Parallel Entry Shift Register

A	B	C
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
0	0	0



NOTE: Tie all unused J and K inputs to V_{CC}.

Figure 40 Binary Ripple Counter

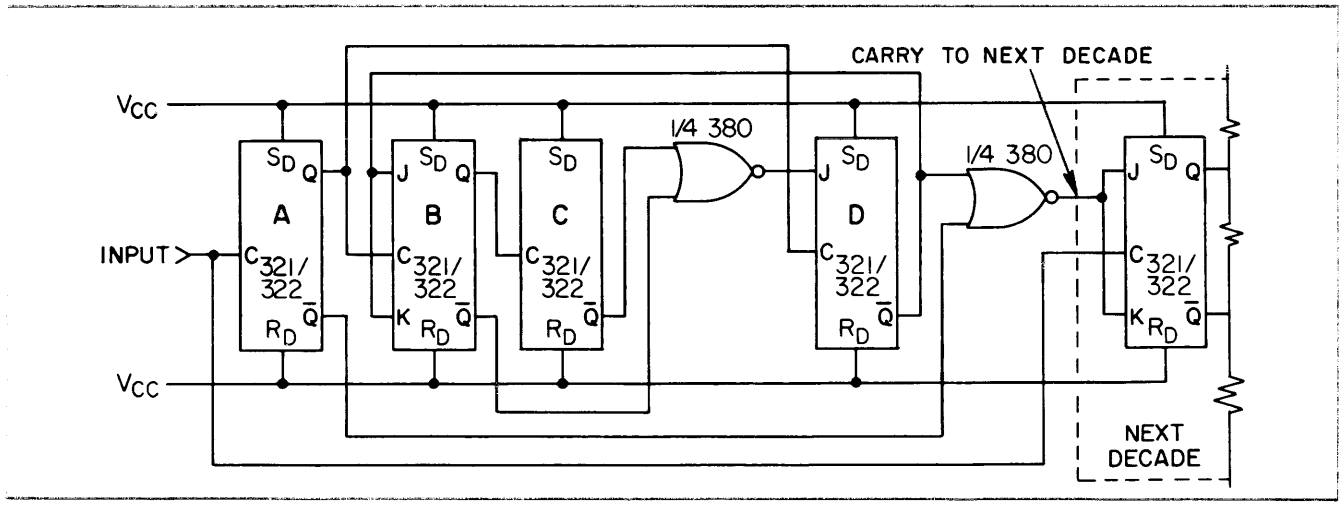


Figure 41 BCD Counter with Gated Carry

Presetting to "0" is illustrated in the first two stages in Figure 40; presetting to "1" is shown in the third stage.

MODIFIED RIPPLE COUNTERS

Many popular counters are modifications of the basic Binary Ripple Counter previously described. The decimal counter modifications, shown in Figure 41, illustrate the versatility obtained by combining the ripple counting technique with logical feedback. In Figure 41, the carry provides resynchronization to the clock pulse. This technique may be applied to other similar ripple counters. It provides most of the speed advantage of ripple propagation while allowing synchronous operation between decades.

8-4-2-1 DECIMAL COUNTERS

The 8-4-2-1 Decimal Counter, shown in Figure 42 requires one gate. The maximum propagation delay occurs either at the transition from state number 3 to state number 4 ($2\ T_1 + T_2$) or at the transition from state number 7 to state number 8 ($3\ T_1$), depending upon operating conditions. The above example illustrates the flexibility that the 321/322 Binary Elements offer the designer. For stages A, B, and C, the design utilizes the J-K characteristic and generates a "change logic" common to both the J and K input. At stage D, it is more economical to treat the 321/322 as an R-S flip-flop and to generate independent "set" and "reset" logic.

SYNCHRONOUS COUNTERS

Synchronous counters are used in applications where all flip-flop outputs must change simultaneously, as in most high-speed logic systems and in counters that must be decoded during counting. Synchronous counters may be used to stop an event on a specific count or may be used for timing events as a function of specific intervals in a clock pulse sequence.

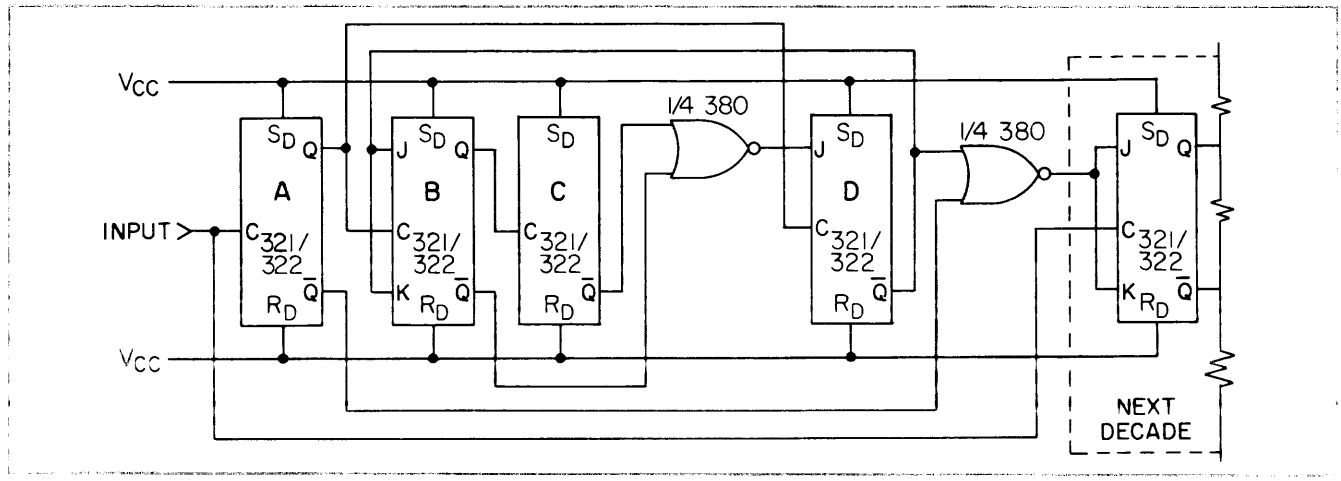


Figure 42 BCD Counter with Gated Carry

Also, these counters are useful for special computer applications that involve reversing, special codes, and start/stop operations. Some limitations of a synchronous counter as compared to a ripple counter are:

1. Higher flip-flop fan-outs and gate fan-ins are required.

2. The clock line represents a relatively high load.

Figure 44 shows the effect on clock frequency of an increasing number of gates between binaries in any synchronous system; the two curves show the difference between the use of all-NOR gating and the maximum utilization of AND gates (alternate levels).

BINARY COUNTER

The large fan-in capability of UTILOGIC II NOR gates allows a simple Synchronous Binary Counter to be implemented easily, as shown by the ten sample stages in Figure 43. The large fan-out capability of the 321/322 binaries allows this counter to be extended to 14 stages (16, 384 states) without buffering. The alternate implementation shown reduces:

1. The fan-out requirements of the 321/322 binaries.

2. The fan-in requirements of the NOR gates.

3. The number of circuit elements when gate fan-in requirements exceed 7.

However, the operating speed is lowered because of the introduction of additional propagation delays. The counter sequence is the same for both implementations.

MODULAR BINARY COUNTER

This type of counter, as shown in Figure 45, requires lower fan-out and fan-in than required in the previous example but at the expense of propagation delay. The maximum signal delay is through N-2 gates for a counter of N stages. Stages may be added in a modular fashion because the logic is repetitive for each stage.

8–4–2–1 DECADE COUNTER WITH DECIMAL DECODING

Feedback and the J-K characteristics of the UTILOGIC II 321/322 are employed to produce the 8–4–2–1 decade counter shown in Figure 46. UTILOGIC II AND gates may be substituted for the NOR gates illustrated in

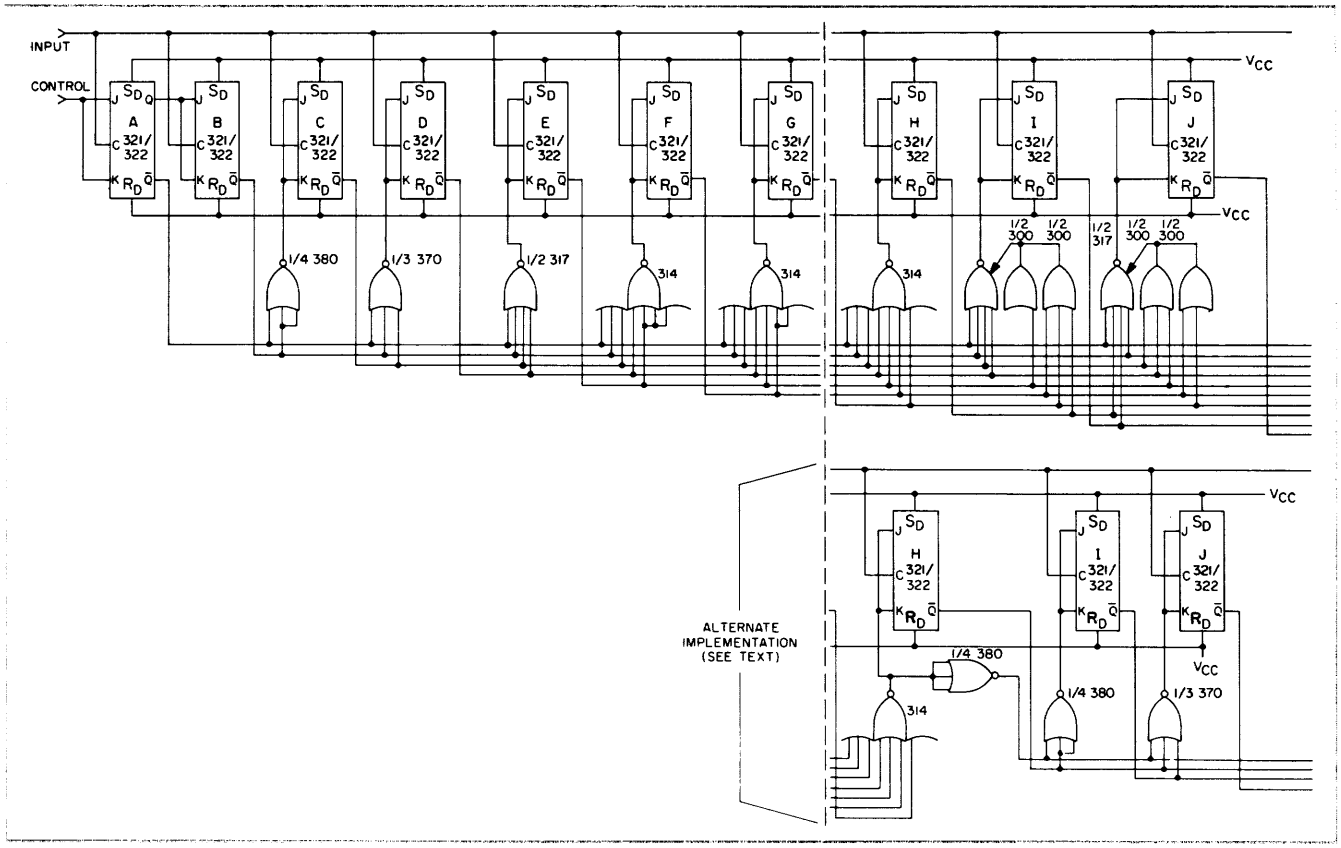


Figure 43 Synchronous Binary Counter

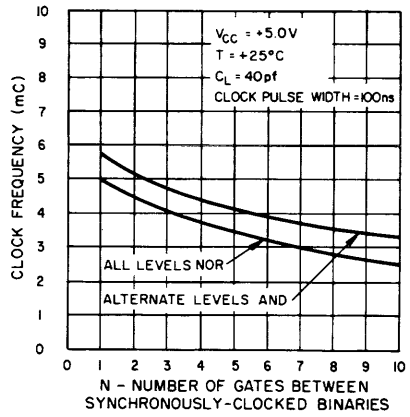


Figure 44 Effect of Logic Depth on Clock Frequency

FEEDBACK SHIFT REGISTERS

Feedback Shift Registers or Ring Counters, like the ripple-carry counters, are capable of operating at the maximum frequency of the flip-flops; they have the additional feature of being able to shift as well as count. This characteristic is very valuable when the information in the counter is to be presented as a serial word to a display or memory device. When connected as a Ring Counter, a Feedback Shift Register will have a sequence length of 2N; other connections may give sequence lengths to the maximum of 2^N-1.

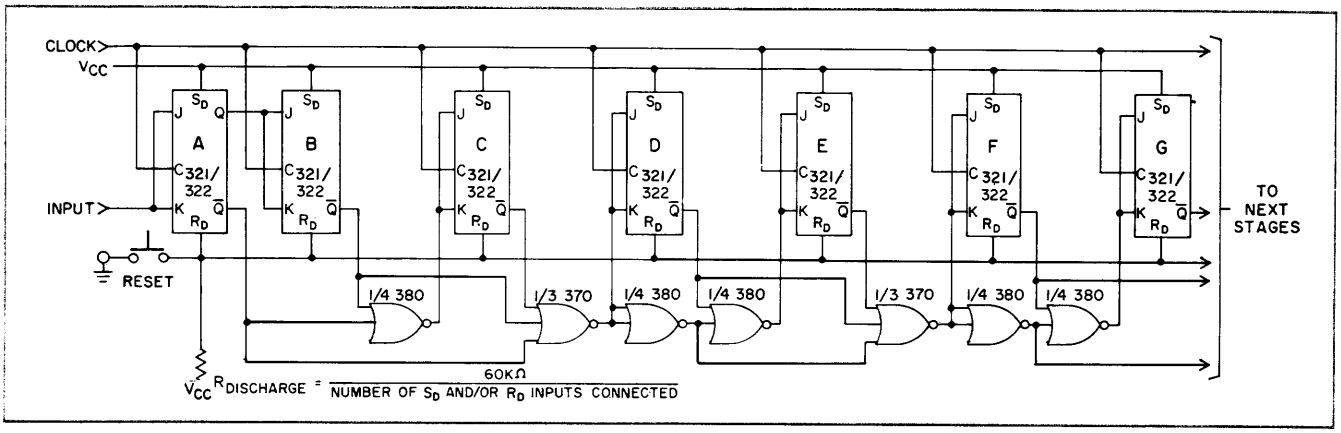


Figure 45 Modular Binary Counter

the decoding matrix when sink fan-out from the decoding gates is not required and decreased propagation delays are desired.

4–2–2–1 DECADE COUNTER

The count sequence of the counter shown in Figure 47 is not as popular as the previously shown 8–4–2–1 sequence but is frequently used since its decimal decoding matrix requires only 3-input gates.

REVERSIBLE BINARY COUNTER

The counter shown in Figure 48 will count every input pulse. The counter will count up when the UP input is low; it will count down when the DOWN input line is low.

REVERSIBLE DECADE COUNTER

The counter shown in Figure 49 uses feedback to produce an 8–4–2–1 decade sequence. The counter will count only when the appropriate command is present.

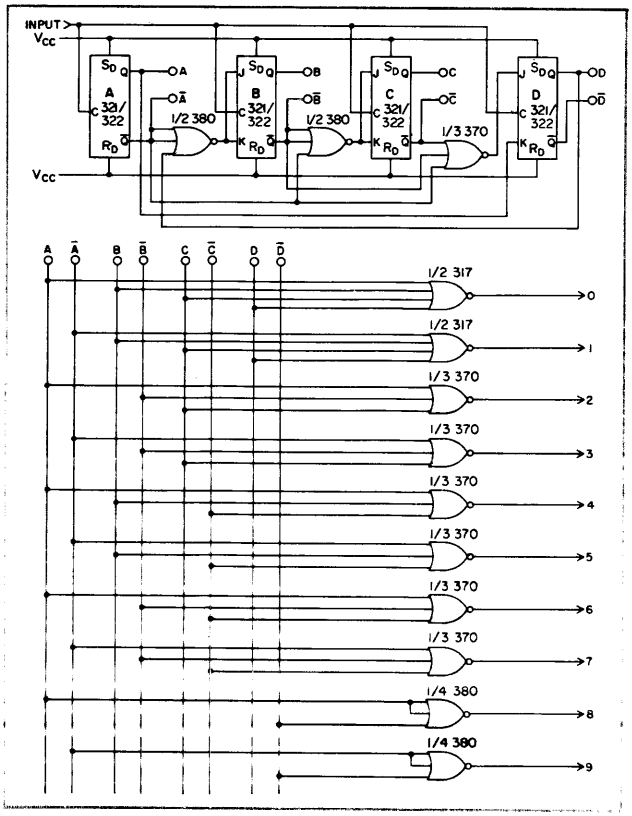


Figure 46 BCD Counter with Decimal Decoding

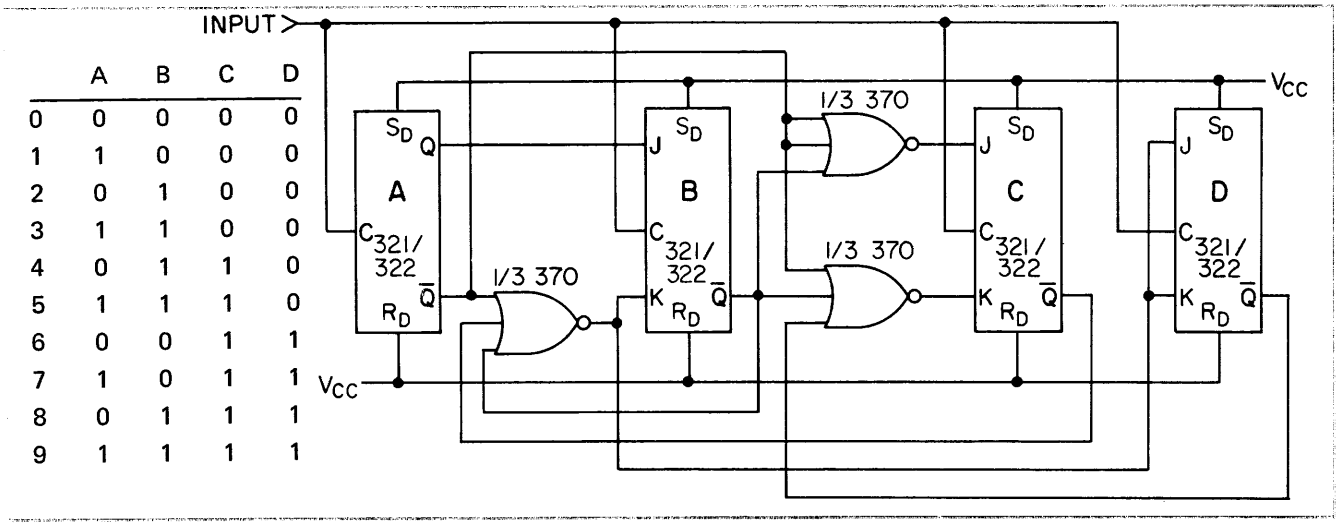


Figure 47 4–2–2–1 Decade Counter

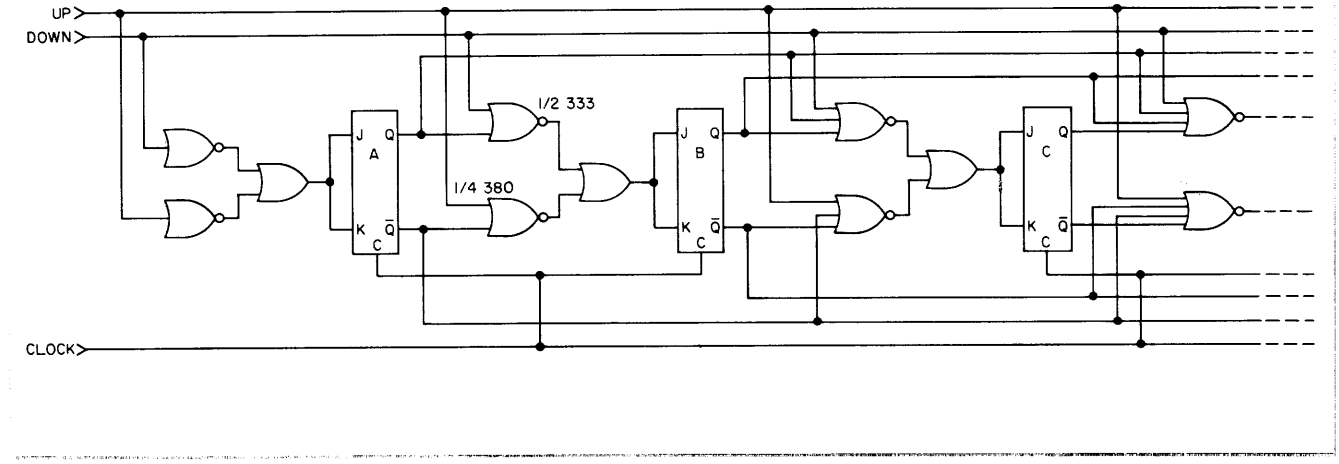


Figure 48 Reversible Binary Counter

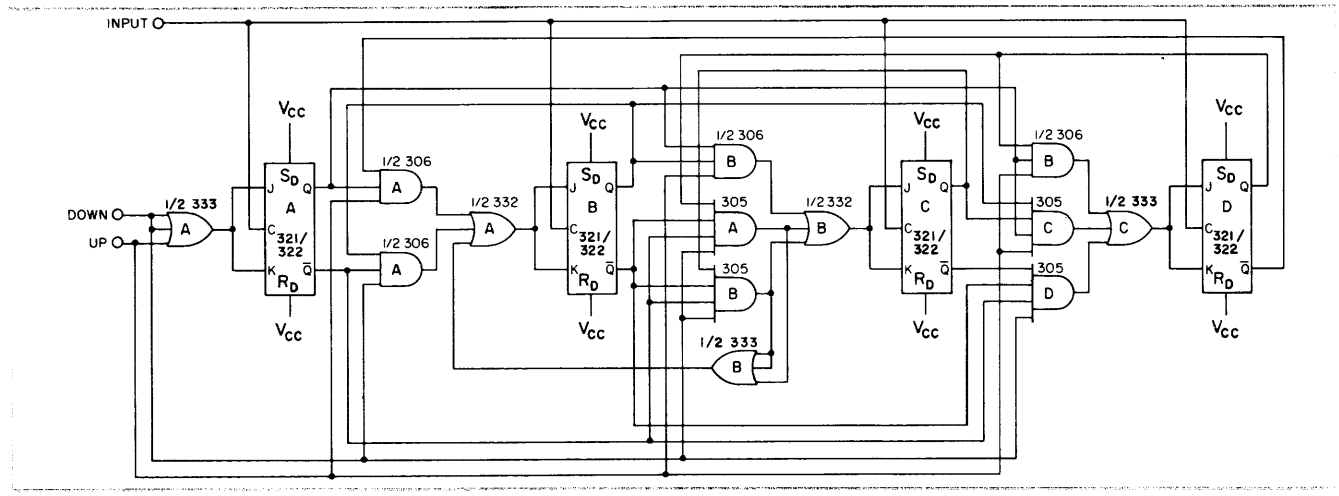
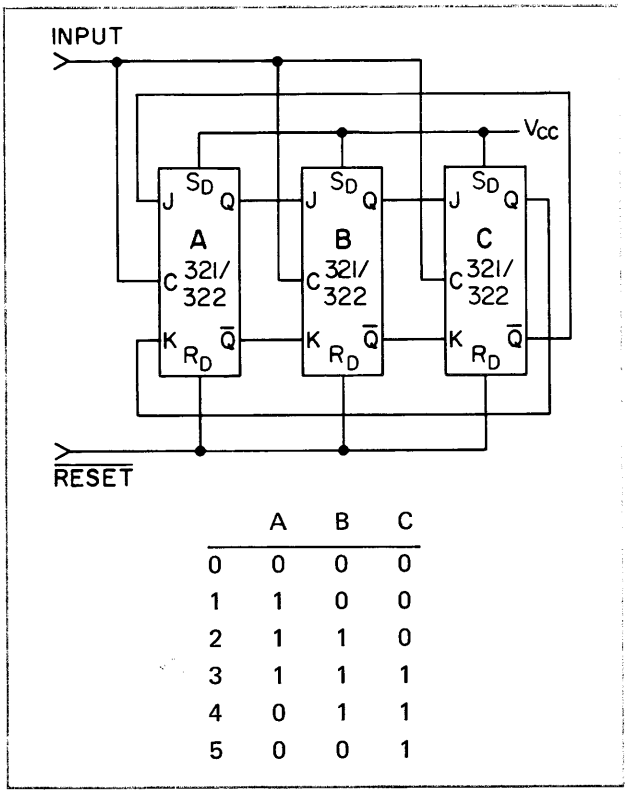


Figure 49 Reversible Decade Counter

Simple Ring Counter

A very simple Ring Counter with sequence of 6 (N equals 3) that requires no gating is shown in Figure 50. Presetting is required to ensure that the proper sequence is entered.



	A	B	C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

Figure 50 Simple Ring Counter

Decimal Ring Counter With Decoding and Self-Sequencing

The counter in Figure 51 is essentially the above counter except that N equals 5, and a gate has been added to provide self-sequencing. Readout gating is shown to illustrate its simplicity. UTILOGIC II AND gates may be substituted for the NOR decoding gates when sink fan-out from the decoding gates is not required, and decreased propagation times are desired.

Johnson Counter

The Johnson Counter (Feedback Shift Register) has a sequence length, 2^N-1, for most small N (N equals the number of stages). However, for some N, the sequence lengths may be different. For example, when N equals 5, one initial state (00000) gives 21 states; another (11000) gives 7; a third initial state (00100) gives 3 states. The Johnson Counter can be designed to produce sequence lengths not easily obtainable with other high-speed counter designs; however, this type of counter is hard to decode and debug since there is no common pattern to the sequence. The Johnson Counter shown in Figure 52 has a sequence length of 15 (initial state "0000") as shown in the Truth Table.

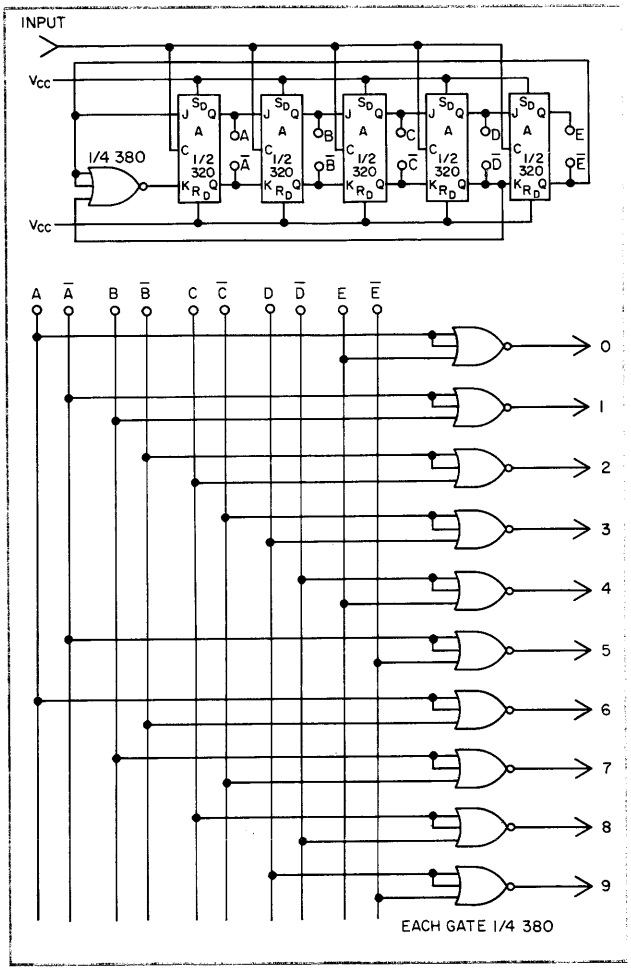


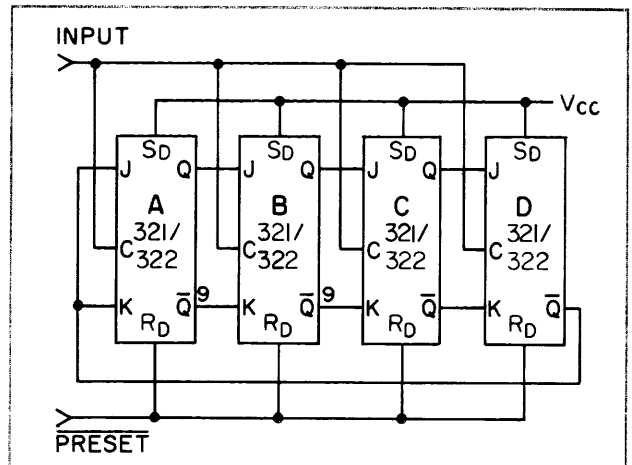
Figure 51 Decimal Ring Counter

ASYNCHRONOUS CONTROL CONFIGURATIONS

In the following asynchronous examples, the timing of the operations is controlled by internally generated signals instead of by an external clock source as in synchronous operations. The logic required to generate the timing signals may require a great deal of hardware, but the operation may be considerably faster than in an equivalent synchronous operation where the clock period must allow for the maximum circuit delays.

SIMPLE ASYNCHRONOUS ADD SEQUENCE

The simple system shown in Figure 53 illustrates typical asynchronous techniques. In this figure, the Asynchronous Sequencer is cleared and started by the START ADD signal. The Asynchronous Sequencer immediately enables the Transfer operation, which proceeds to com-



	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	0	1	0	1
5	0	0	1	0
6	1	0	0	1
7	1	1	0	0
8	0	1	1	0
9	1	0	1	1
10	1	1	0	1
11	1	1	1	0
12	0	1	1	1
13	0	0	1	1
14	0	0	0	1
0	0	0	0	0

Figure 52 Johnson Counter

pletion and signals the Sequencer that it is completed. The Sequencer then enables each succeeding operation in sequence, but only after receiving a completion signal from each signal from each previous operation. After all operations under the control of the Sequencer have been completed, an ADD COMPLETE signal is sent to the master control circuits.

ASYNCHRONOUS SEQUENCER

The circuit shown in Figure 54 will generate the enable signals for "N" asynchronous operations. The Sequencer may be expanded where shown in order to accommodate any number of operations. Typically, the Asynchronous Sequencer will be used in combination with a similar asynchronous circuit, such as the following Shift Register with Asynchronous Transfer.

ASYNCHRONOUS TRANSFER REGISTER

Figure 55 shows a logic configuration to asynchronously transfer information stored at locations X_A, X_B . . . X_N (a register) to register Y. Upon receipt of the command TRANSFER, the input NOR gates, which are serving as ANDs, will connect X to Y to allow Y to assume the state of X. The Digital Comparators compare the state of each Y position to the state at each X position. When all of the positions agree, TRANSFER COMPLETE signals completion to a control circuit such as the Asynchronous Sequencer above.

Miscellaneous Circuits

This simple 2-gate RS flip-flop circuit, shown in Figure 56, is frequently called a latch to distinguish it from a more complex flip-flop, such as the 321 or 322.

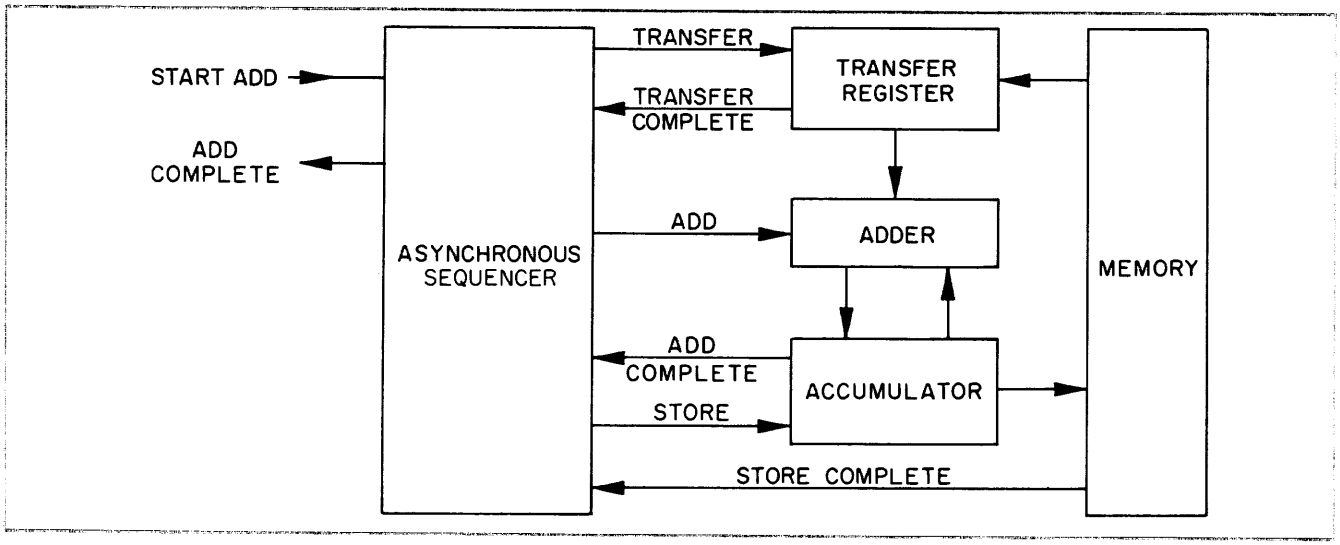


Figure 53 Asynchronous System

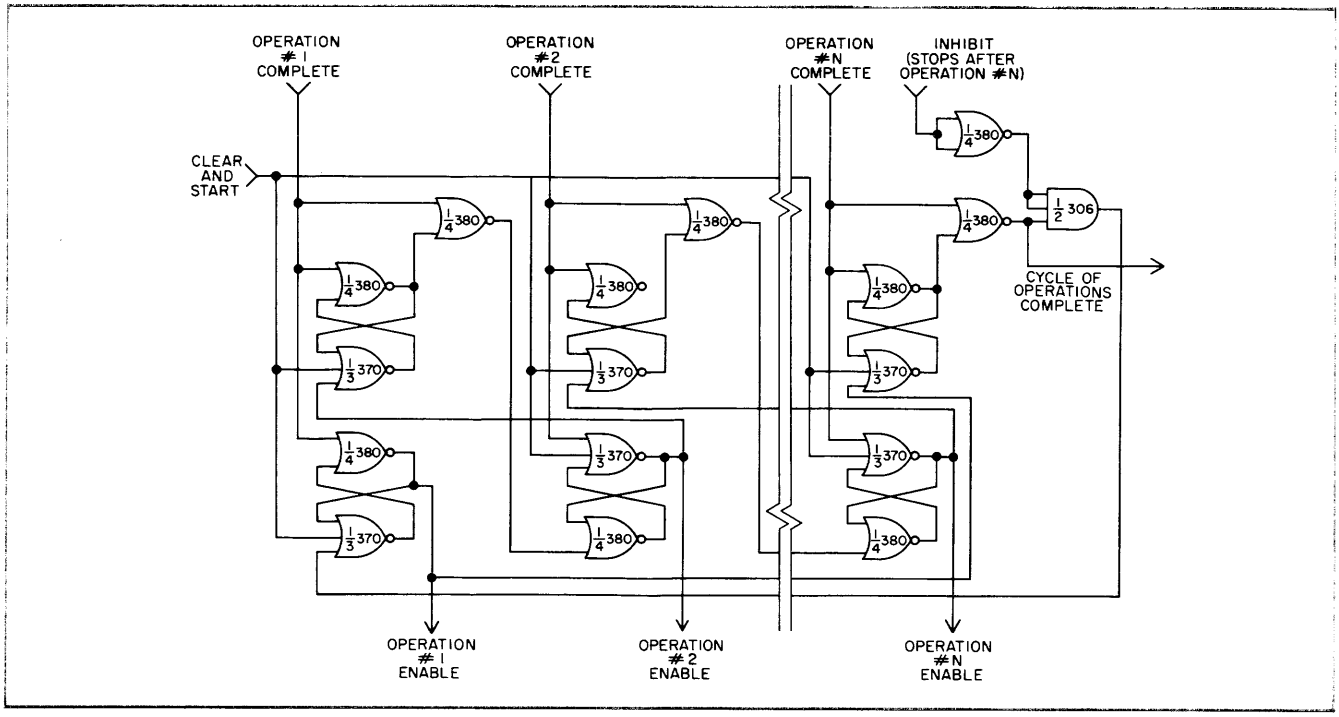


Figure 54 Asynchronous Sequencer

The high input impedance of the UTILOGIC II source inputs makes them ideally suited for use with integrating circuits to form a great variety of pulse-shaping circuits. When connected as in Figure 57, a Pulse-Width Discriminator is formed with a pulse-width threshold of about C_T where time is ns and C_T pF. By reversing the polarity of the diodes as in Figure 58, a simple Pulse Stretcher is formed. This circuit will widen positive pulses by about 8 C_T.

Figure 59 shows 321 implementation of a simple one-shot using only one additional NOR gate.

Figure 60 shows a simple Schmitt trigger circuit implemented with 1/2 333 OR gate. This circuit provides sharp switching with less than 150 mV hysteresis at 25°C, as shown on V_{IN} versus V_{OUT} graph, Figure 61.

The oscillator circuit (see Figures 62 and 63) is based on the fact that an odd number of gates in a ring is unstable. The period is adjusted by connecting capacitance to the expander terminal. This oscillator has good temperature stability. Waveform deterioration limits the lower usable frequencies to 250 kHz.

One-shots also may be obtained from the UTILOGIC II NOR gates and OR gates as in Figures 64 and 65. For the circuit of Figure 64, the period is 0.7 R_TC_T. R_T must be 8K or less, and C_T 100 pF or greater. Maximum period is 5 milliseconds; minimum period is 200 ns.

When only one output is required, the circuit of Figure 65 may be used. The period is 1.1 R_TC_T ±35 percent. R_T includes the input impedance of the OR gate (≈20K). External resistors will reduce the pulse width tolerance to about 15 percent at 2K. The diode will lessen the effect on pulse widths when the duty cycle exceeds 25 percent. These two circuits should not be used when the one-shot requirement is for stable operation and/or wide pulse widths.

The NOR gates also are useful as inexpensive, low performance linear amplifiers for certain applications. When used, as in Figure 66, a UTILOGIC II NOR gate will have a gain of about 10, and bandwidth of 3 MHz.

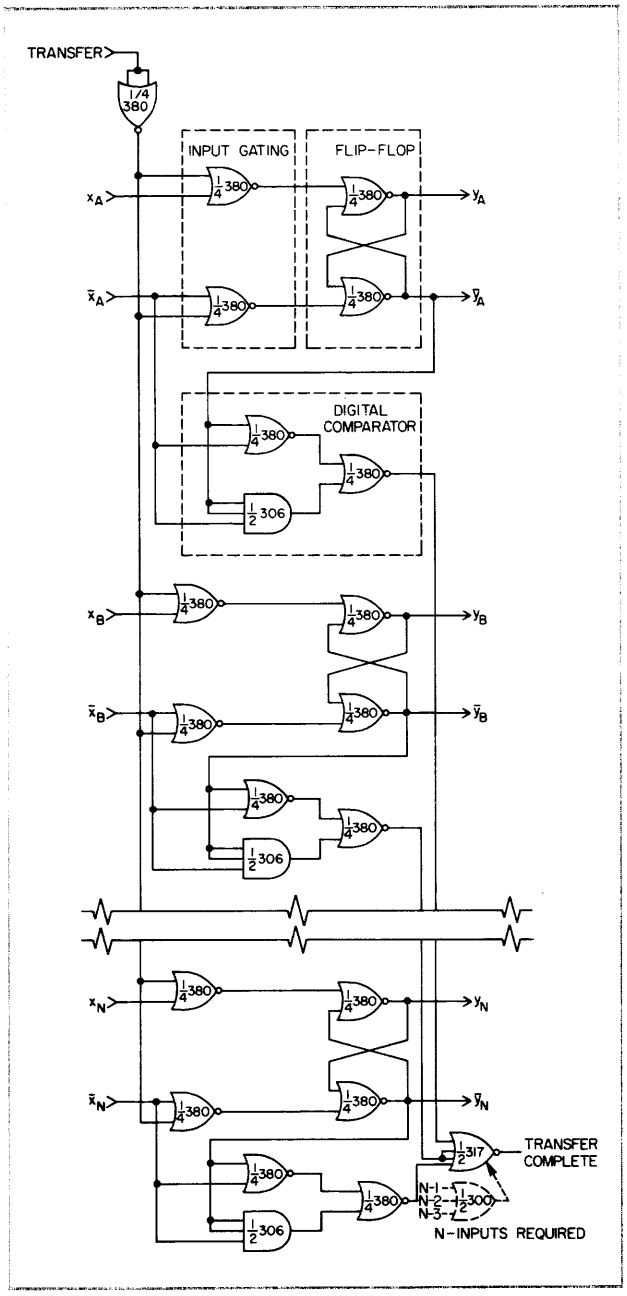


Figure 55 Asynchronous Transfer

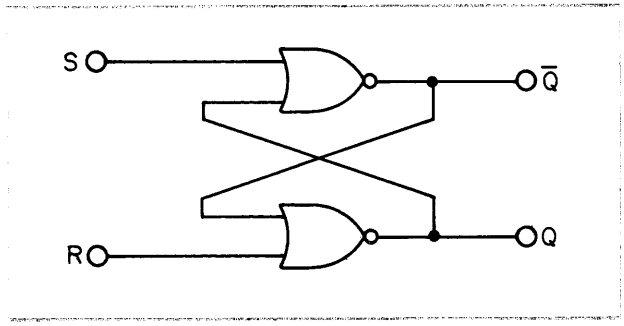


Figure 56 Latch

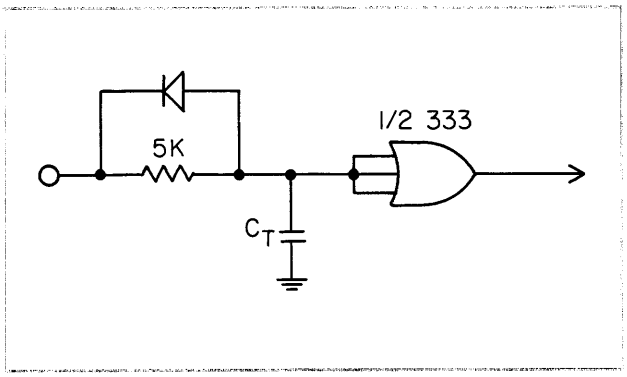


Figure 57 Pulse Width Discriminator

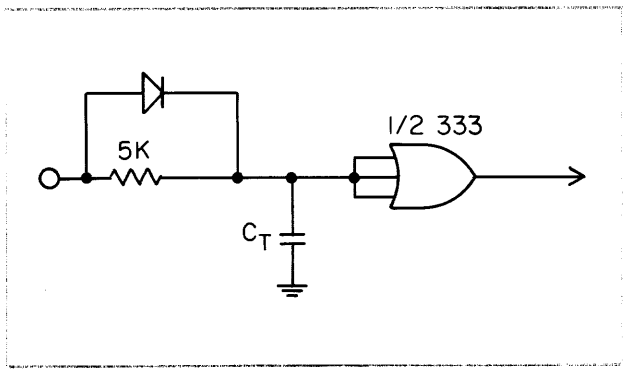


Figure 58 Pulse Stretcher

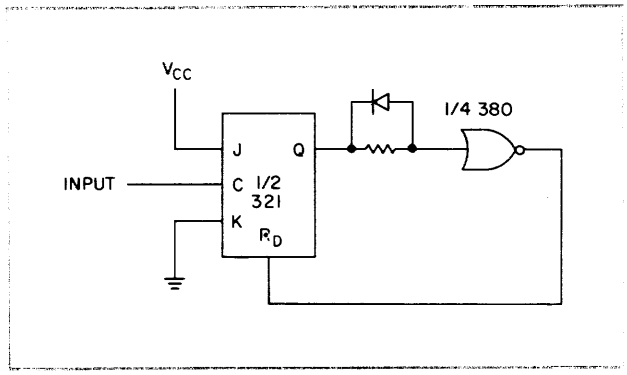


Figure 59 One-Shot

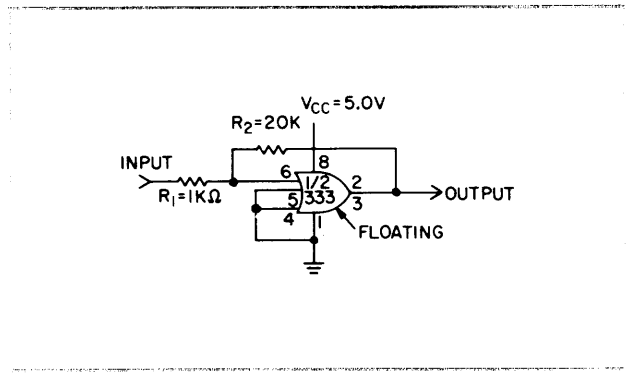


Figure 60 Schmitt Trigger

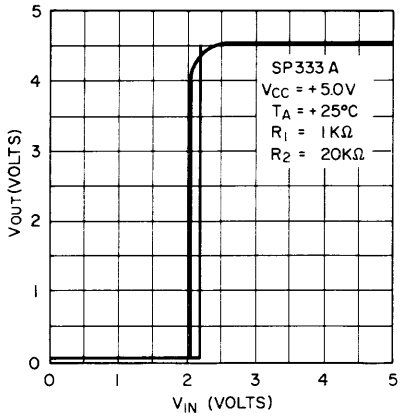


Figure 61 Schmitt Trigger V_{IN} vs V_{OUT}

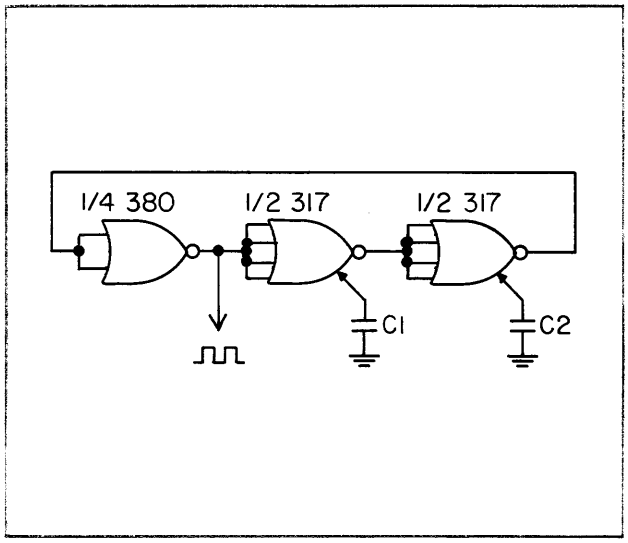


Figure 62 Oscillator

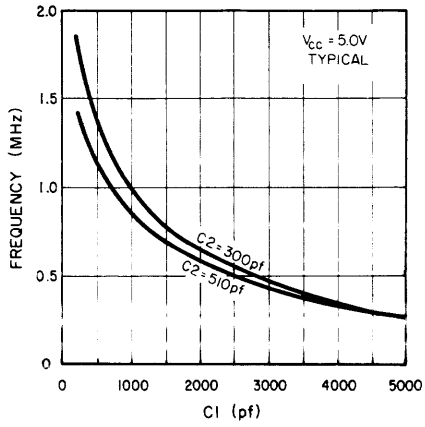


Figure 63 Oscillation Frequency

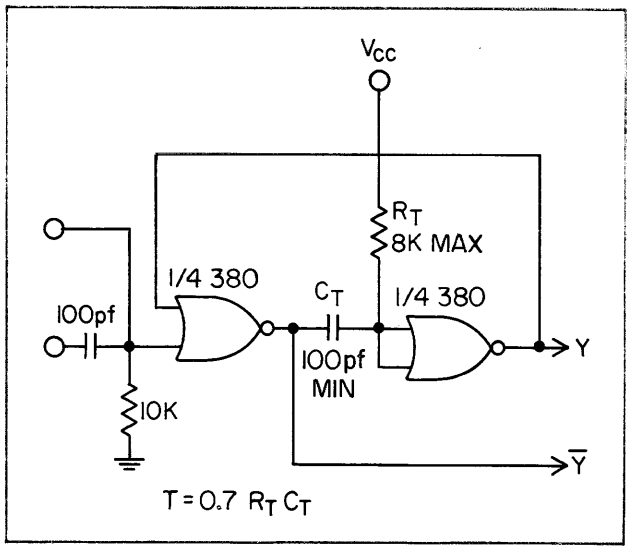


Figure 64 One-Shot with Complementary Outputs

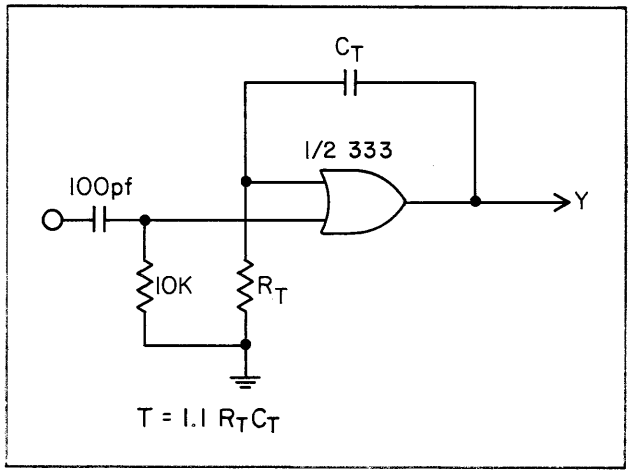


Figure 65 One-Shot

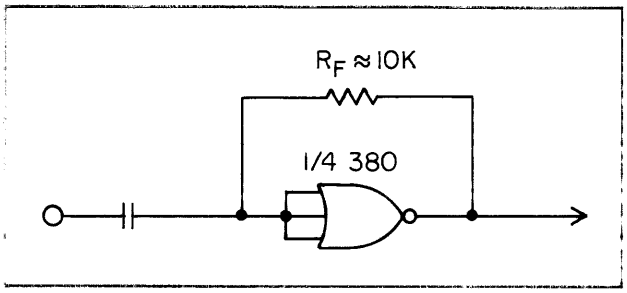


Figure 66 Linear Amplifier

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