Xerox Extended Performance RAD Storage System

Models 7231/7232

Reference Manual

90 15 57C

RAD ORDER CODES

Code (Hexadecimal)	Function
01	Write
02	Read (Report any transmission error at "count done")
03	Seek
04	Sense
05	Check-write
12	Read (Terminate data transfer and report any transmission error at end of current sector if error is encountered)
13	Test (for diagnostic purposes)

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REVISION

This publication 90 15 57C, is a revision of the Xerox Extended Performance RAD Storage System Reference Manual, 90 15 57B, dated January, 1970. The major change is the description of the diagnostic features provided by the Model 7231A02 Controller. A change in text from that of the previous manual is indicated by a vertical line in the margin of the page.

RELATED PUBLICATIONS

Title	Publication No.
Xerox Sigma 2 Computer/Reference Manual	90 09 64
Xerox Sigma 3 Computer/Reference Manual	90 15 92
Xerox Sigma 5 Computer/Reference Manual	90 09 59
Xerox Sigma 6 Computer/Reference Manual	90 17 13
Xerox Sigma 7 Computer/Reference Manual	90 09 50
Xerox Sigma 8 Computer/Reference Manual	90 17 49
Xerox Sigma 9 Computer/Reference Manual	90 17 53
Xerox Symbol/LN, OPS Reference Manual (Sigma 5-9)	90 17 90
Xerox Symbol/LN, OPS Reference Manual (Sigma 2/3)	90 10 51
Xerox Extended Symbol/LN, OPS Reference Manual (Sigma 2/3)	90 10 52
Xerox Meta-Symbol/LN, OPS Reference Manual	90 09 52
Xerox Macro-Symbol/LN, OPS Reference Manual	90 15 78

Manual Content Codes: BP – batch processing, LN – language, OPS – operations, RBP – remote batch processing, RT – real-time, SM – system management, TS – time-sharing, UT – utilities.

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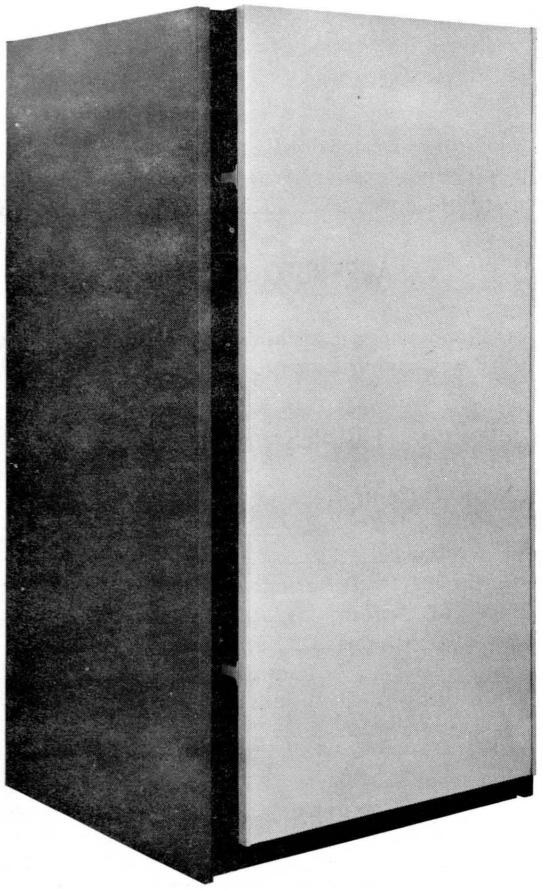
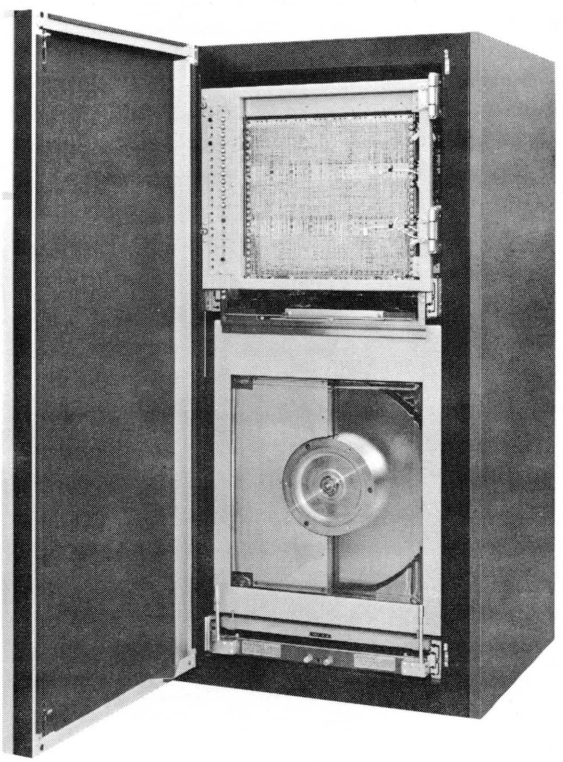


Model 7231 RAD Controller and 7232 Storage Unit



RAD Interior View

1. GENERAL DESCRIPTION

INTRODUCTION

The Extended Performance RAD (Rapid Access Data) Storage System provides fast, high capacity, random-access memory for Xerox Sigma computers. RAD units may be used for system, scratch pad, or working storage for processing programs. In a time-sharing system, they may serve as permanent file storage, "swap" storage, and as a medium for storing real-time programs.

A RAD system consists of one Model 7231 Controller[†] and one to four storage units, Model 7232. The controller and one storage unit are in the same cabinet. Additional storage units are in separate cabinets.

The basic addressable unit of information is a sector of 1024 data bytes. There are 12 sectors to each track. A 7232 RAD unit has 512 tracks (see Table 1). Data is presented in 8-bit bytes to the RAD by the controlling system, and each byte is written serially on the selected sector. Access time is minimal because each track has a separate read/write head (average access time is 17 milliseconds).

Rotational delay may be reduced by sensing the unit's current position before initiating an input or output operation and then transferring data beginning immediately at the next sector to be accessed. If desired, a data record can overlap from sector to sector or from track to track; the RAD controller automatically performs sector and track incrementing.

The contents of RAD storage units are permanently protected against primary power failure. Also, "write-protect" switches prevent inadvertent destruction of recorded information due to programming error. Each switch inhibits writing on 32 adjacent tracks.

The term "RAD" in this manual indicates a device controller and storage unit. Any separate reference is specified by "controller" or "storage unit".

[†]Unless specified by Model 7231A02 Controller, the information in this manual applies to all Model 7231 Controllers. Model 7231A02 has the additional diagnostic features.

To use this manual effectively, the reader should be familiar with the Sigma Computer Reference Manual (see Related Publications) applicable to his installation (particularly the input/output instructions and input/output operations sections).

Table 1. Characteristics

Operating Characteristics	
RAD file rotational speed	1774 rpm
Total time per revolution	33.8 milliseconds
Inter-sector gap time	140 microseconds
Sector-to-sector time	2.81 milliseconds
Effective read/write bit rate	3,072,000 bits/second
Byte transfer rate	
Single sector	384,000 bytes/second
Multiple sectors	364,000 bytes/second
Byte capacity	6,290,000 bytes (512 tracks)
Write protection	Each switch protects 32 tracks.
Physical Dimensions	
Height	63 in.
Width	32 in.
Depth	31 in.
Weight (7231/7232)	1200 lb (approx.)
Environmental Characteristics	
Power requirements	
Service	208 vac ± 10%, 60 ± 0.5 Hz, three-phase
Start	20 kva
Run	2000 watts
Ambient temperature	50° to 105°F.
Relative humidity	10% to 90%

2. FUNCTIONAL DESCRIPTION

DATA REPRESENTATION

Data is presented to a RAD one byte at a time, and is written bit-serially on the designated sector. Similarly, data is read serially from a RAD and assembled in its buffer register for presentation to the controlling system, a byte at a time. (See "RAD Orders" and "Addressing Format".)

RAD STATES

The RAD's initial operational state depends on its power status. If all power is off, it is removed from the line ("not operational" state). Any attempt to access it results in a response of "No I/O address recognition" to the I/O instruction. The status response, if requested, is unpredictable under these conditions.

OPERATIONAL STATES

When required power is on, the RAD enters the "automatic" mode and the "ready" condition. The exact RAD condition may be determined by examining the status response to one of the instructions, START INPUT/OUTPUT (SIO), HALT INPUT/OUTPUT (HIO), or TEST INPUT/OUTPUT (TIO). Other I/O instructions, TEST DEVICE (TDV) and ACKNOWLEDGE INPUT/OUTPUT INTERRUPT (AIO), provide additional specific status indications (see "RAD Status Response").

A brief explanation of RAD conditions and mode follows.

CONDITIONS

Ready. The "ready" condition is entered when required power is initially turned on. In this condition, an SIO instruction can be accepted by the RAD controller and executed, provided that no interrupt is pending.

Busy. In this condition, the RAD controller has already accepted an SIO instruction. A new SIO will not be accepted until the current operation is completed and no device interrupt is pending.

MODE

Automatic. The RAD is in the "automatic" mode as long as required power is on ("ready-automatic" or "busy-automatic").

TRANSITIONS BETWEEN STATES

Table 2 summarizes the allowable state transitions and the conditions required to cause them.

Table 2. RAD Controller State Transitions

Present State \ Next State	Not Operational	Ready Automatic	Busy Automatic
Not Operational	———	Power is turned on	Not possible
Ready Automatic	Power is turned off	———	SIO has been accepted
Busy Automatic	Power is turned off	Operation completed, or HIO, or I/O reset signal received	———

DATA TRANSFER

A RAD operation is initiated by the controlling system with a START INPUT/OUTPUT OPERATION (SIO) instruction if all the following conditions are satisfied:

1. Input/output address recognition exists.
2. The RAD is in the "ready" condition.
3. No RAD interrupt is pending.

If these are satisfied, the RAD enters the "busy" condition. The RAD controller now initiates the transfer of data to or from the RAD storage unit as specified by the order (Write or Read) until the required number of bytes have been transferred. The operation then terminates, and the RAD returns to the "ready-automatic" state. The operation may also be terminated by:

1. An Input/Output Processor (IOP) Halt[†], generated by the IOP[†] on certain error conditions (in which case all data may not have been transferred).
2. A HALT I/O (HIO) instruction (in which case all data may not have been transferred).

Following an HIO or IOP Halt[†], the RAD is in a "ready-automatic" state.

[†]Not applicable to Sigma 2

3. PROGRAM INTERFACE

RAD ORDERS

The RAD contains an address register that selects the track and sector to be accessed. This register is initially loaded by executing a Seek order. During a data transfer, if more bytes are transferred than can be contained in one sector (1024 bytes) the address register is automatically incremented so that the next sector is addressed. The address register is cleared by means of the I/O RESET switch (Sigma 5/7) or RESET position of the INITIALIZE switch (Sigma 2/3). An error results, however, if the address register is incremented when addressing the last available sector. This error condition also occurs if a programmer tries to use a Seek order to load the address register with a nonexistent disc address.

Upon completion of a data transfer, the address register is incremented so that it addresses the sector following the last one involved in the data transfer.

During a write operation, each byte received is summed to form a parity checksum. This sum is always written in the last 2 byte positions of the sector, even if less than 1024 bytes are transmitted. During a read operation, the data is summed as it is read and the result is compared with the parity checksum. Failure to compare results in an error condition.

The seven valid orders are:

Order	Action
X'01' Write	The Write order causes the RAD unit to record the number of bytes specified in the command doubleword, starting at the track and sector address currently selected by the RAD controller address register (this address is specified by the previous Seek order or the last sector involved in the data transfer incremented by one). Transmission continues until the computer indicates to the storage unit that the entire record has been transferred. If the transmitted information does not completely fill the last sector, zeros are written into the remainder of the sector. If a write operation is attempted in a protected area, the operation is not performed and the condition is immediately reported to the controlling system (see "Addressing Format" and "RAD Status Response" in this section).
X'02' Read	This Read order causes the RAD to read the bytes specified in the command doubleword, starting at the track and sector address currently selected by the RAD controller address register (this address is specified by the previous Seek order or the last sector involved in the data transfer incremented by one). The data is stored in core memory beginning at the location specified by the command doubleword. Parity check errors are signalled at the end of the logical record.
X'12' Read	This Read order reads the number of bytes specified in the command doubleword from the track and sector currently selected by the RAD controller address register (this address is specified by the previous Seek order or the last sector involved in the data transfer incremented by one). The data is stored in core memory starting at the location specified by the command doubleword. Parity check errors are signalled at the end of the sector in which they occur.
X'03' Seek	The Seek order causes two bytes to be sent to the RAD where they are loaded into the RAD controller address register. The controller then directs any subsequent read/write operation to begin at this address. An "incorrect length" indication is generated if a byte count other than 2 is specified in the I/O doubleword associated with the Seek order.
X'04' Sense	The Sense order causes the storage unit to transmit three bytes of position and status information into core memory. The first two bytes are the contents of the RAD address register currently stored in the controller. The first bit of the first byte indicates whether the track associated with the current track address is "write-protected". The third byte indicates the current rotational position. Incorrect length indication is generated if a byte count other than 3 is specified in the I/O doubleword associated with the Sense order. The Sense order also causes a sector unavailable error if the address register has incremented beyond the last available sector.
X'05' Check-write	The Check-write order is used to verify recorded data. It causes data to be sent to the RAD controller by the controlling system where it is compared with that being read from the RAD. In the event that a byte does not compare, a "transmission error" signal is transmitted to the controlling system, and the data transfer is terminated. Data on the RAD and in core storage are not recorded or modified, but only compared.
X'13' Test (for diagnostic purposes)	The 7231A02 controller requests one byte of data from the controlling system. The byte determines the test mode to be entered or resets the test mode indicators (see Table 3). The program signals "count done" after this data transfer. Succeeding orders are

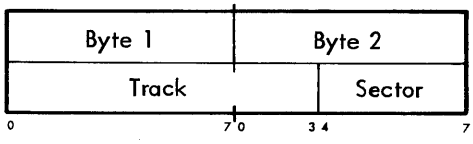
Order	Action	
X'13' Test (cont.)	decoded as described above with the following test mode modifications:	
	Test Mode 1	Data is transferred to or from the Fast Access Memory (FAM), as determined by bit 7 of the above orders.
	Test Mode 2 (Check-write)	The controller simulates a check-write operation by comparing the contents of the byte register with data received from the controlling system.
	Test Mode 2 (Read)	The controller simulates a Read order by reading the contents of the byte register. If the modifier bit is set, the controller forces a parity error.

Table 3. Test Mode Selection (7231A02 Controller)

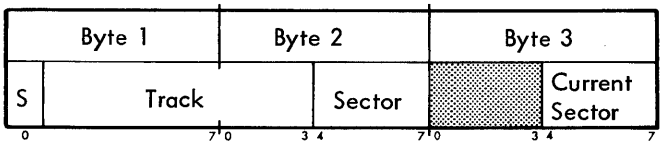
Bit Position	Function	State	Meaning
3,4	Reserved	0	These bits are currently zero; however, they may be used in future enhancements.
5,6,7	Select Test Mode	001	Test Mode 1 is selected.
		010	Test Mode 2 is selected.
		100	The test mode modifier bit is set.
		000	The test mode indicators are reset.

ADDRESSING FORMAT

The format of the two bytes sent to the RAD by a Seek order is:



The format of the three bytes received on a Sense order is:



where

S is the setting of the write-protect switch for the indicated track (0=not write-protected; 1=write-protected).

Track is the track number currently contained in the RAD controller address register.

Sector is the sector number currently contained in the RAD controller address register.

Current sector is the current sector position of the RAD.

KEY EVENTS

The key events that occur during a RAD operation are described in the following paragraphs. No chronological order of occurrence should be assumed from the order of presentation.

START INPUT/OUTPUT

A RAD operation is initiated with the execution of an SIO instruction by the controlling system. If I/O address recognition exists and the RAD is in the "ready" condition with no interrupt pending, the controlling system sets its "I/O address recognition" and "SIO accepted" indicators. The RAD then advances from the "ready" to the "busy" condition. It then requests an order byte from the controlling system and proceeds with the operation defined by the order byte.

UNUSUAL END CONDITIONS

After receiving an order, the RAD returns an "unusual end" indication to the controlling system when any of the following conditions occurs:

1. Invalid order code.
2. Not operational.
3. Incrementing the RAD controller address register beyond the last available sector in the current RAD unit.
4. Nonexistent "Seek" address.
5. Attempting to write on a write-protected track.
6. Transmission data error.

CHANNEL END CONDITIONS

After receiving an order from the controlling system, the RAD signals "channel end" to the controlling system when

all data has been transferred or when an "unusual end" condition occurs while a data transfer is in process.

NOT OPERATIONAL CONDITIONS

Conditions that cause the RAD to become "not operational" are

1. Absence or failure of ac or dc power.
2. RAD unit off-line for testing purposes.

TRANSMISSION ERROR CONDITIONS

The RAD can detect and report transmission errors to the controlling system. Conditions causing this error are

1. Failure of the end of sector parity check during a Read or Check-write operation.
2. Failure of a data comparison on a Check-write operation (the parity byte is also automatically compared).
3. A data overrun; the controlling system has failed to maintain the data transfer rate required by the RAD during the execution of the previous Read, Write, or Check-write order.
4. Failure to recognize a "sync" pattern on a Read or Check-write order.

INCORRECT LENGTH CONDITIONS

The RAD can detect and report incorrect length errors to the controlling system. Conditions causing this error are

1. A byte count other than 2 has been specified in the I/O doubleword associated with a Seek order.
2. A byte count other than 3 has been specified in the I/O doubleword associated with a Sense order.
3. The last Read, Write, or Check-write order did not specify a byte count that was an integral multiple of 1024 bytes.

RAD STATUS RESPONSE

The RAD system returns various status flags in response to computer-executed I/O instructions. A detailed explanation of the I/O instructions and their status information is contained in the reference manuals for Sigma computers.

I/O INSTRUCTION STATUS BITS

The execution of an I/O instruction by the controlling system provides two bits of information (condition codes) pertaining to the general status of the addressed I/O device and its controller. Table 4 lists the possible status bit settings provided by the execution of each I/O instruction and the significance of each setting.

DEVICE STATUS BYTE

Eight bits of status information are made available to the controlling system in response to the execution of an I/O instruction. Tables 5,6, and 7 show the significance of each status flag returned to the controlling system by the RAD.

OPERATIONAL STATUS BYTE

The Operational Status Byte generated at the end of each I/O operation also provides indicators to the controlling system. See Table 8.

PROGRAMMING CONSIDERATIONS

This RAD system is designed to permit track switching and order modification (read to write and vice-versa on Sigma 5-9) during the gap between sectors. The command chaining feature of the I/O system must be used.[†]

Frequent data chaining (small byte counts) or frequent use of test instruction loops (TIOs and TDVs) cause a reduction of the available I/O system transfer rate due to the additional communication between the I/O section and the central processor and/or memory required for either kind of task. This can result in a reduction of as much as 50 percent and, therefore, can cause frequent data overruns.

When "immediate" mode transfer techniques are used (data transmission at the next available sector) the programmer must add 1 to the sector number received as a result of the Sense order. This procedure ensures one sector time (2.81 milliseconds) for the programmer to prepare the command list for the subsequent data transfer. Command chaining should be used between the ensuing Seek order and the related data operation, i.e., Read, Write or Check-write. If command chaining is not used, 2 must be added to the sector number received from the Sense order, or the time of one revolution of the RAD will be lost before data transfer is initiated.

INFORMATION PROTECTION

The contents of RAD storage units are protected in case of primary power failure; recorded information is not lost or altered.

"Write-protect" switches prevent inadvertent destruction of recorded data due to programming error. These toggle switches are located on a panel inside the cabinet. Writing is inhibited with the switch in the "up" position. Each switch protects 32 tracks. The first switch inhibits writing on tracks 0 through 31; the second inhibits writing on tracks 32 through 63, etc.

[†]Command chaining not available on the Sigma 2/3 I/O system.

Table 4. RAD I/O Instruction Execution Response

Instruction	Code[t] CC1 or O	Code[t] CC2 or C	Significance
SIO	0	0	I/O address recognized and SIO accepted.
	0	1	I/O address recognized, but SIO not accepted (i.e., RAD was already "busy" or an interrupt is pending).
	1	0	RAD attached to a "busy" selector IOP (not applicable to Sigma 2/3 computers).
	1	1	I/O address not recognized.
HIO	0	0	I/O address recognized and RAD was not "busy" when halt occurred.
	0	1	I/O address recognized and RAD was "busy" when halt occurred.
	1	0	Invalid code.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can be accepted.
	0	1	I/O address recognized, but SIO cannot be accepted.
	1	0	RAD attached to a "busy" selector IOP (not applicable to Sigma 2/3 computers).
	1	1	I/O address not recognized.
TDV	0	0	I/O address recognized and previous operation not terminated because of a "not operational" condition.
	0	1	I/O address recognized, but previous operation terminated because of a "not operational" condition.
	1	0	RAD attached to a "busy" selector IOP (not applicable to Sigma 2/3 computers).
	1	1	I/O address not recognized.
AIO	0	0	Normal interrupt condition present (no "unusual end").
	0	1	Unusual interrupt condition present ("unusual end").
	1	0	Invalid code.
	1	1	No interrupt condition present.

[t]"CC1" and "CC2" refer to condition code bits in Sigma 5-9 computers; "O" represents the Overflow bit and "C" represents the Carry bit in Sigma 2/3 computers.

Table 5. Status Response for SIO, TIO, and HIO

Bit Position	Function	State	Meaning
0	Interrupt Pending	1	Interrupt pending (issued but not yet acknowledged by an AIO instruction). The RAD continues transmitting data (if specified) until current operation completed (all data transferred or operation terminated due to error condition). Does not accept new SIO until this interrupt has been acknowledged; new order can be accepted, however, if command chaining specified, even though interrupt may be pending. Interrupt cleared by executing an AIO or HIO.
1,2	Device Condition	00	RAD "ready".
		01	RAD "not operational".
		10	RAD unavailable – not applicable.
		11	RAD "busy".
3	Mode – Automatic or Manual	1	Always in "automatic" mode.
4	Device Unusual End	1	Execution of previous order terminated due to "unusual end" condition.
5,6	RAD Controller Condition	00	RAD controller "ready".
		01	RAD controller "not operational" – not applicable.
		10	RAD controller unavailable – not applicable.
		11	RAD controller "busy".
7	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.

Table 6. Status Response for TDV and AIO

Bit Position	Function	State	Meaning
0	Data Overrun	1	A data overrun has occurred during execution of the previous order.
1	Reserved	0	This bit is currently zero; however, it may be used in future enhancements.
2	Sector Unavailable	1	RAD controller address register was incremented beyond last available sector during previous order, or Seek order loaded RAD controller address register with value greater than last available sector, or Sense order was issued after data transfer that accessed the last available sector on the RAD.
3	Write-protect Violation	1	Previous Write order attempted to write on a track that was write-protected.
4	Missed "Sync" Pattern	1	This bit is for diagnostic use only.
5-7	Reserved	0	These bits are currently zeros; however, they may be used in future enhancements.

Table 7. Status Response for TDV in Test Mode Operation (7231A02 Controller)

Bit Position	Function	State	Meaning
0,1,2	Test Mode Responses[t]	000	Normal TDV response (see Table 4).
		001	Parity register returned for controlling system.
		010	Track register bits 0 through 4 returned to controlling system.
		100	Track register bits 5 through 8 and sector register returned to controlling system.
3-7	See Table 3.		

[t]TDV response during test mode operations are determined by the above three bits of the first data byte following the execution of an X'13' order.

Table 8. Operational Status Byte[t]

Function	State	Meaning
Transmission Error	1	One of the conditions specified under "Transmission Error Conditions" has occurred since previous order received by RAD.
Incorrect Length	1	An incorrect length condition has occurred since previous order received by RAD.
Chaining Modifier		Not applicable.
Channel End	1	RAD has terminated its operation for any of the reasons listed under "Channel End Conditions".
Unusual End	1	RAD has terminated its operation for any of the reasons listed under "Unusual End Conditions".
Reserved	0	The other bits are currently zeros; however, they may be used in future enhancements.

[t]For the bit positions of these functions in the Operational Status Byte, see the applicable Sigma Computer Reference Manual.

SEQUENCE OF ACTIVITY

Figures 1 through 6 illustrate the sequential relationship of the key events that occur during RAD operations.

RAD FAULTS AND RECOVERY PROCEDURES

The following information, unless otherwise noted, is applicable for a RAD I/O system operating with a Xerox Sigma 2, 3, 5, 6, 7, 8, or 9 computer.

This information describes how to evaluate the status response and condition code bits associated with specific I/O instructions to determine whether a RAD I/O operation has been completed successfully or terminated due to a fault condition. Detailed information is also provided for evaluating failing I/O operations in a prescribed sequence and taking appropriate corrective action.

It is assumed that RAD operations are performed in an I/O interrupt environment and that the status response and condition code bits of ACKNOWLEDGE INPUT/OUTPUT INTERRUPT (AIO) and TEST DEVICE (TDV) instructions after an I/O interrupt provide sufficient information to determine if the RAD operation was successful. For failing RAD operations, additional information is obtained from the status response and condition code bits of a TEST INPUT/OUTPUT (TIO) instruction. Note that before the status of any I/O instruction may be used for testing purposes, the condition codes returned with the I/O instruction must be tested to verify that the I/O instruction has been successfully executed and that the status information is available in the register.

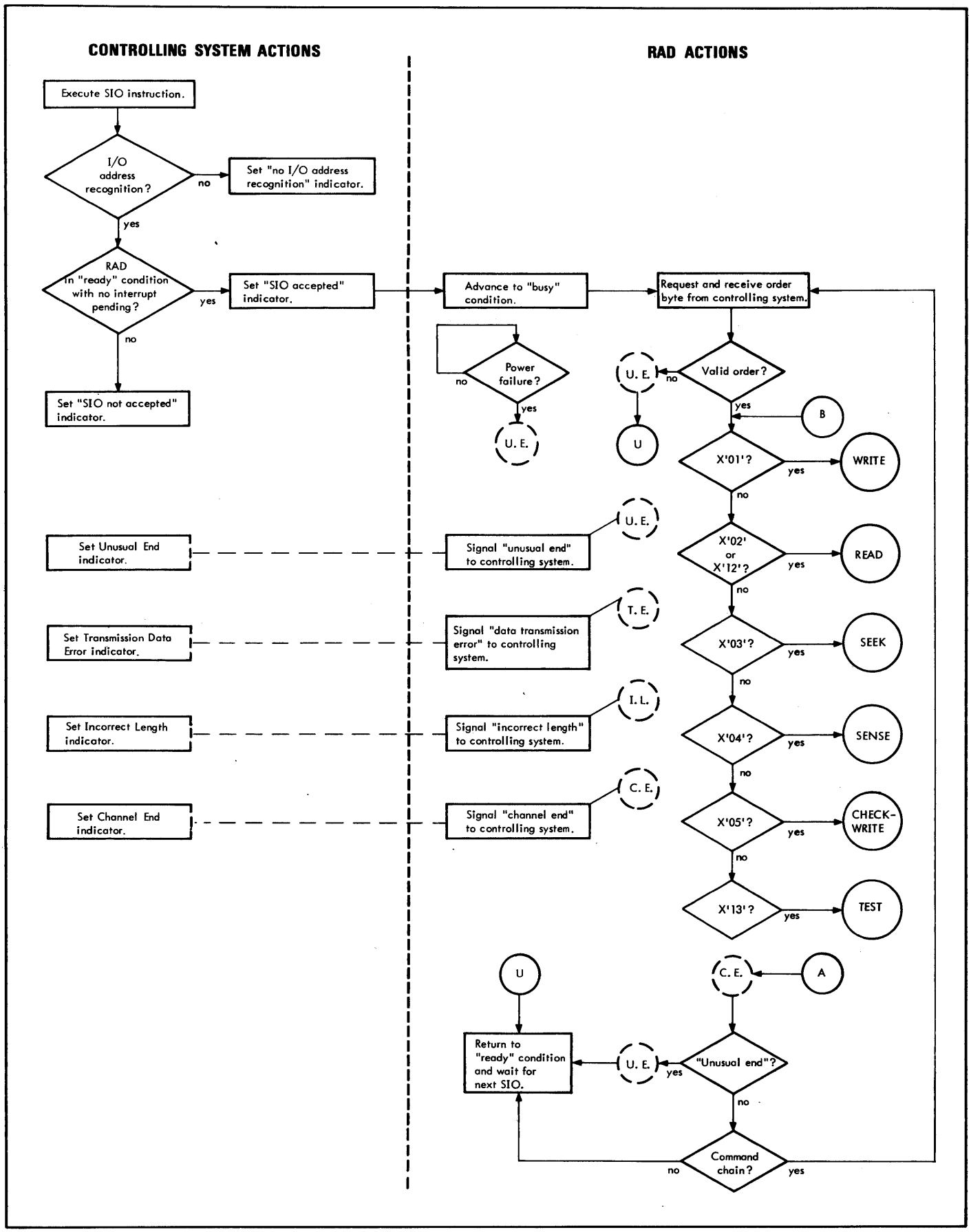


Figure 1. Controlling System/RAD Actions

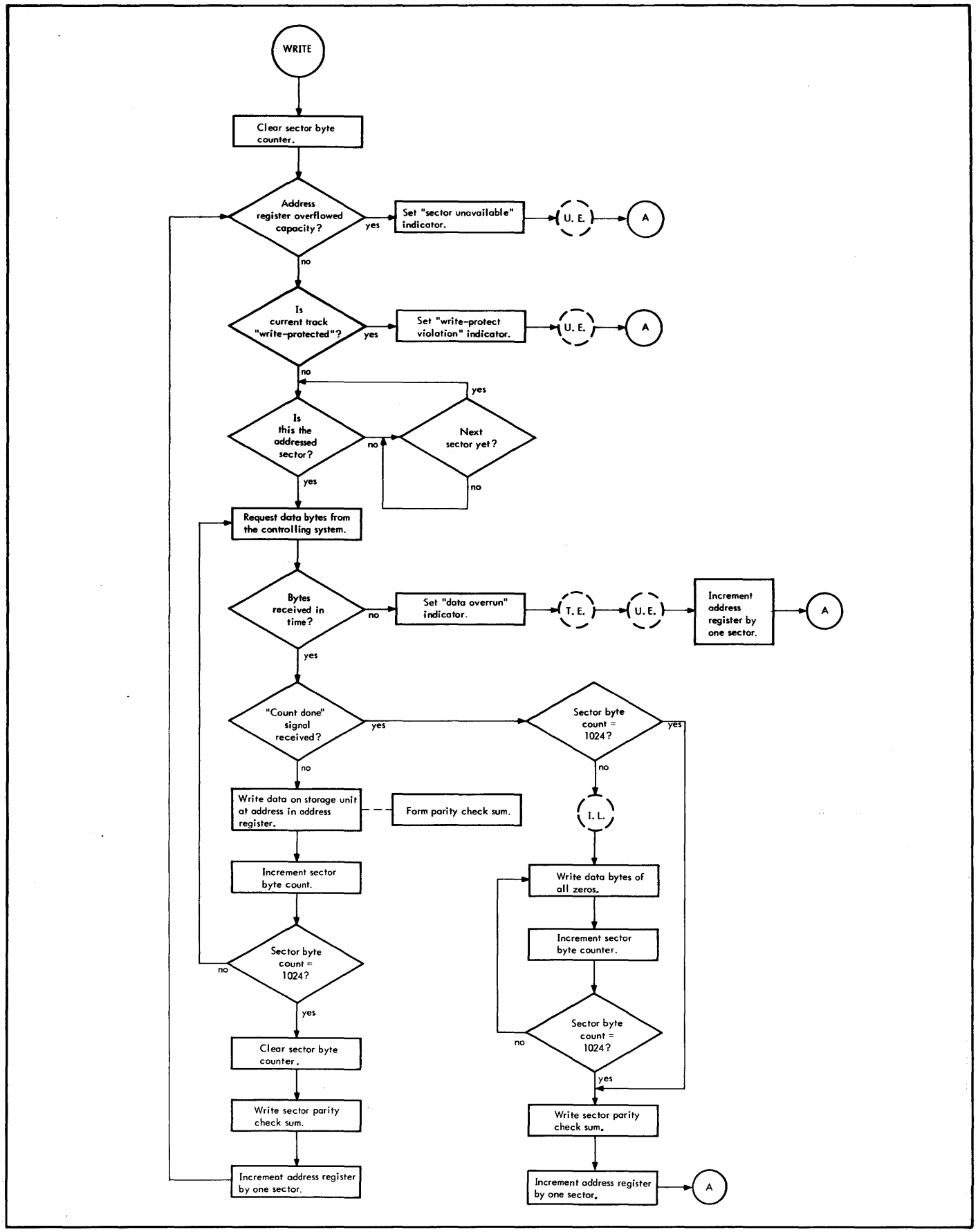


Figure 2. Write Order RAD Actions

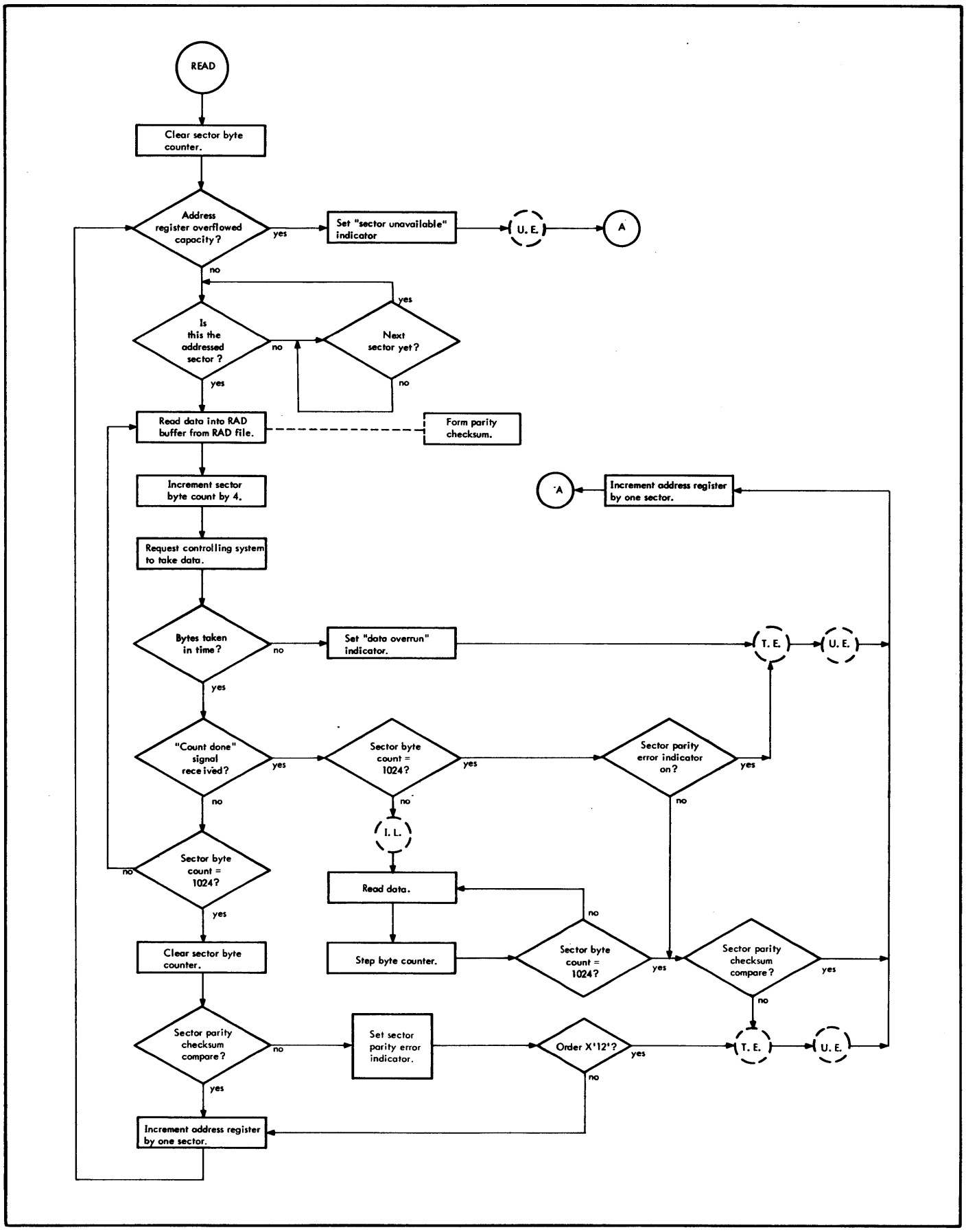


Figure 3. Read Order RAD Actions

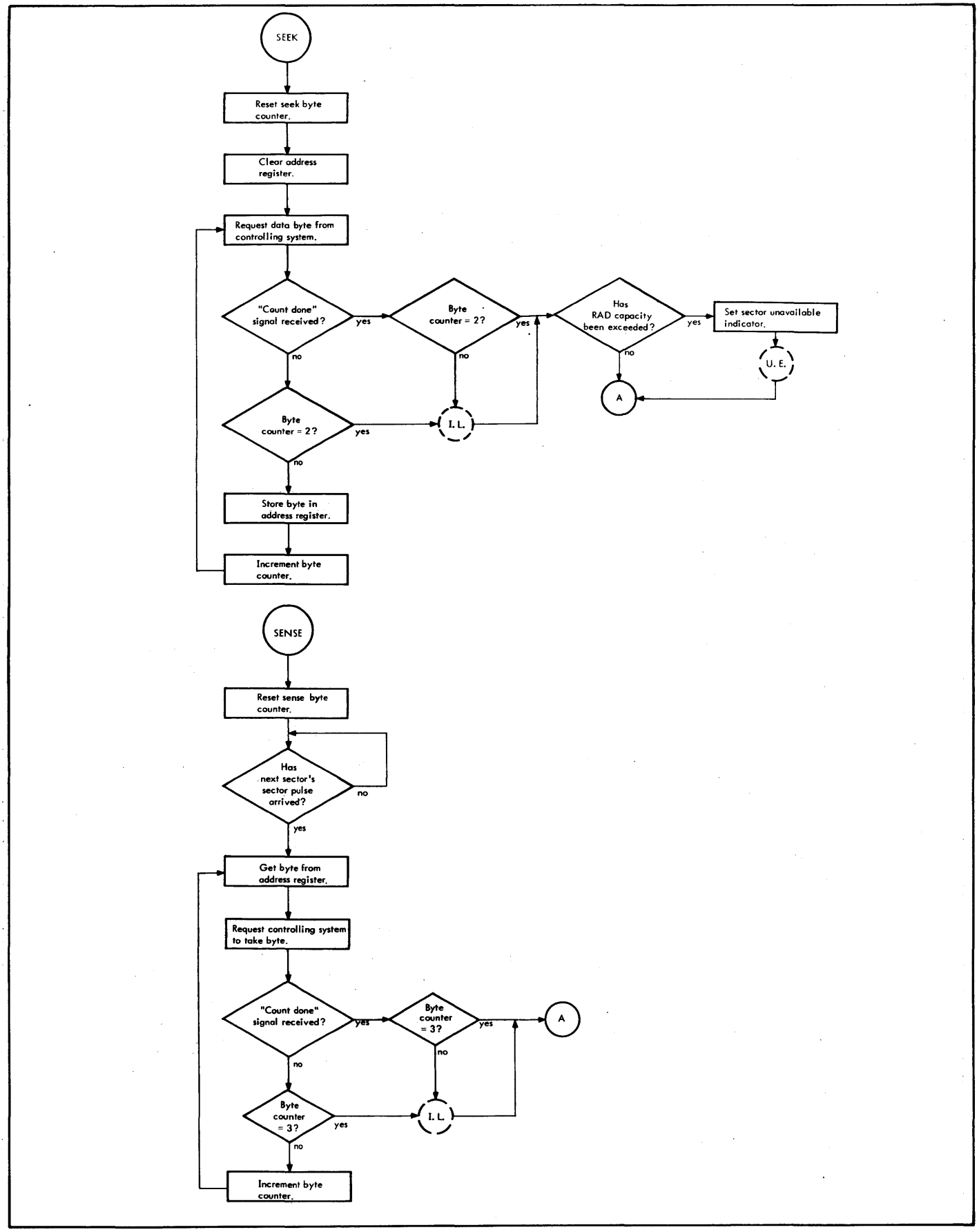


Figure 4. Seek/Sense Order RAD Actions

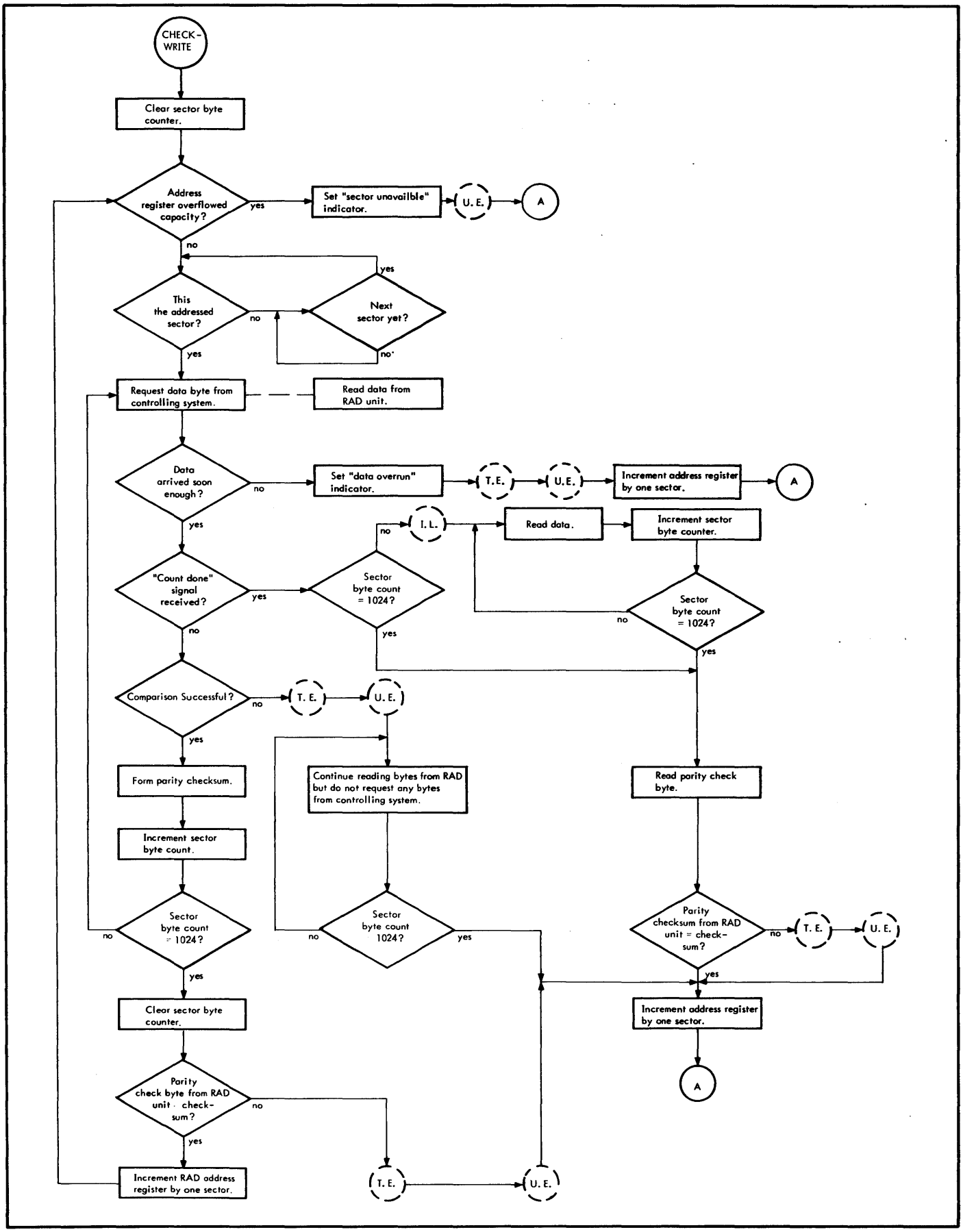


Figure 5. Check-Write Order RAD Actions

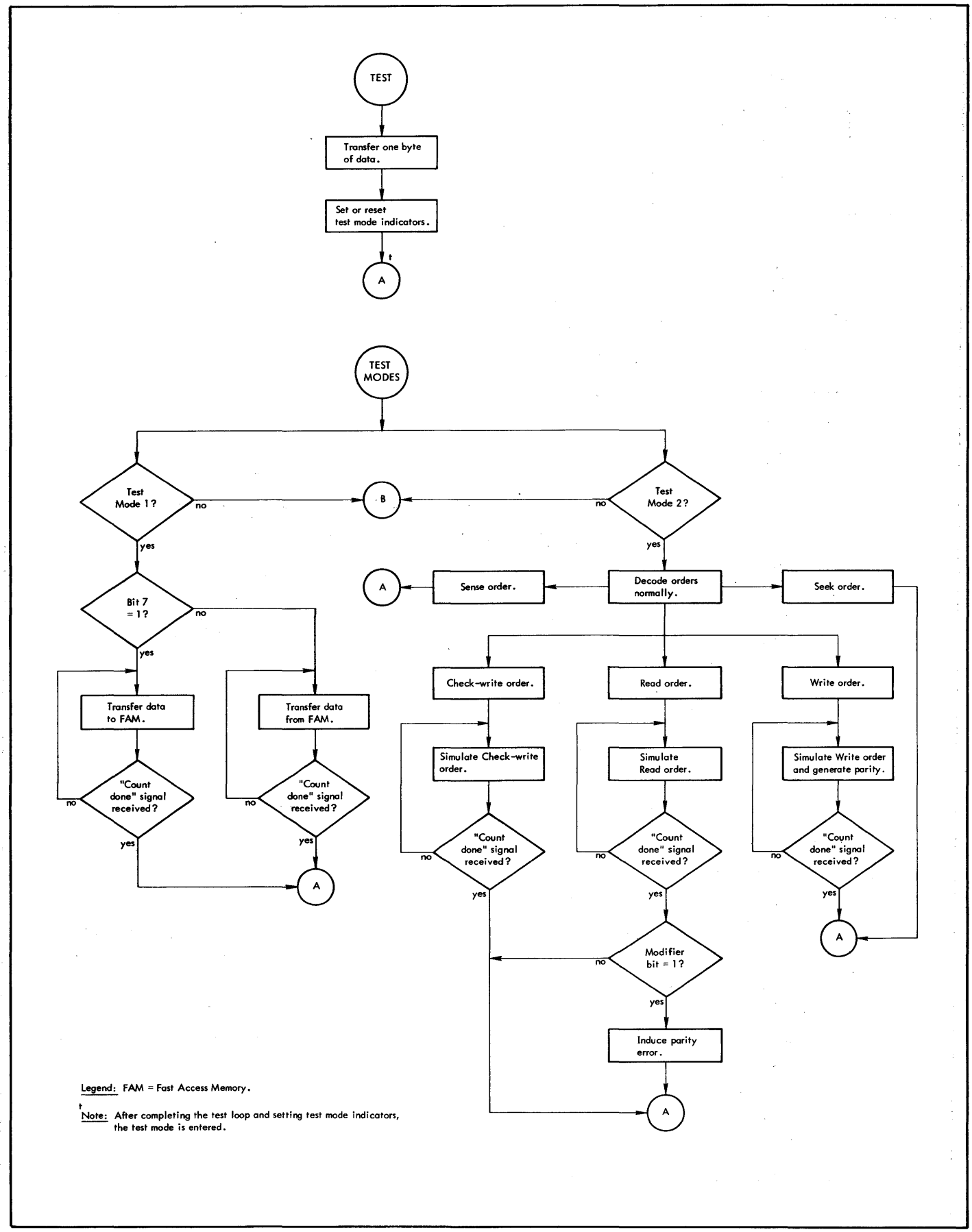


Figure 6. Test Order RAD Actions

Additional assumptions are that a fault can be attributed to a specific RAD order (i.e., Seek, Sense, etc.) and for multisector operations, the failing sector can be determined.

In the case of command lists, a sequence of operations may be performed before the I/O interrupt occurs and status information is available. When an error occurs, the command list sequence is terminated and the failing order (operation) can be determined from the TIO current command address. The programming system then has its choice of repeating the entire command list or rebuilding the command list (bypassing all nonfailing surface operations) to repeat the operation which failed.

I/O INTERRUPT ENVIRONMENT

The I/O interrupt environment is established by setting flags within the Input/Output Command Doublewords (IOCDs) of the command lists and by using specified time-out delays within software time-out routines.

SOFTWARE TIME-OUT VALUES

The recommended software time-out delay for RAD operations is a minimum of one second.

IOCD FLAGS

The setting of the IOCD flags depends on the type of computer system.

Sigma 2/3 IOCD Flag. The Interrupt flag (I) is set to a 1 in every IOCD. This permits an I/O interrupt to be requested whenever a "channel end" or "unusual end" condition occurs. If data chaining is specified, the Interrupt flag should be set to a 1 only in the last IOCD of the command list.

Sigma 5-9 IOCD Flags. When the RAD is operating with a Sigma 5, 6, 7, 8, or 9 computer, the following flags must be set:

ICE (Interrupt at Channel End). This flag is set to a 1 only in the last IOCD of a command list.

IUE (Interrupt at Unusual End). This flag is set to a 1 in all IOCDs.

HTE (Halt on Transmission Error). This flag is set to a 1 in all IOCDs.

SIL (Suppress Incorrect Length). This flag is set to a 1 whenever an incorrect length indication is to be inhibited from causing an IOP Halt and subsequent unusual end I/O interrupt. An incorrect length indication is generated whenever any of the following conditions occurs:

1. During a Read, Write, or Check-write operation when the number of data bytes is not an integral multiple of 1024 bytes.
2. During a Seek operation when a byte count other than 2 is specified.
3. During a Sense operation when a byte count other than 3 is specified.

I/O OPERATION EVALUATION

By evaluating the status response and condition code bits obtained by executing AIO and TDV instructions after an I/O interrupt, a decision may be made as to whether the I/O operation was completed successfully or terminated due to a fault condition.

For Sigma 2/3 Computer Systems Only. A RAD I/O operation may be considered successful if all the status response and condition code bits are as described below:

1. After an AIO instruction, the Overflow and Carry indicators are both 0.
2. After a TDV instruction, the Overflow and Carry indicators are both 0.
3. The Error flag in the odd I/O channel register (assigned to RAD) is 0.
4. Bits 0, 1, and 4 in the even I/O channel register (assigned to RAD) are all 0.

For Sigma 5-9 Computer Systems Only. A RAD I/O operation may be considered successful if all the status response and condition code bits are as described below:

1. After an AIO instruction, condition code bits CC1 and CC2 are both 0.
2. After an AIO instruction, Operational Status Byte bits 8-15 are all 0.
3. After a TDV instruction, condition code bits CC1 and CC2 are both 0.
4. After a TDV instruction, Operational Status Byte bits 8-15 are all 0.

In either case (Sigma 2/3 or Sigma 5-9 computer systems), if one or more of the specified bits are not 0, a TIO instruction must be issued to obtain the state of the RAD.

I/O FAULTS AND RECOVERY PROCEDURES

Status information that is obtained by executing AIO, TDV, and TIO instructions after an I/O interrupt is evaluated in a prescribed manner as listed in Table 9. Column 1 provides a summary description of the fault when the specified bits are not 0 (indicating generally that a fault condition has occurred). Column 2 shows specific bit configurations and a detailed description of a fault condition. Thus, the first 2 columns of Table 9 permit a fault condition to be defined as a function of the status response and condition code bits.

Table 9. Fault Testing Sequence

Sequence and Summary Description	Configuration and Significance of Status Bits	Failing Order: Seek	Sense	Read X'02'	Read X'12'	Write	Check-write	Recommended Corrective Action (see Table 10)
Step 1. Performed only if TIO 5,6 ≠ 00 indicating that controller is not ready (applicable to all computer systems).	TIO 5,6 = 01 or TIO 5,6 = 10 Not defined. The controller is not ready immediately after an I/O interrupt.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
	TIO 5,6 = 11 Busy. The controller failed to return to the ready state immediately after the I/O interrupt due to a hardware malfunction or because the command list is coded with multiple interrupts.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
Step 2. Performed only if TIO 1,2 ≠ 00 indicating that device is not ready (applicable to all computer systems).	TIO 1,2 = 01 Not Operational. The device is not operational due to a power failure or because the device has been placed in the off-line state. Both conditions are considered to be hardware malfunctions.	X	X	X	X	X	X	Recovery Procedure 1 for all failing orders.
	TIO 1,2 = 10 Not defined. The device is not ready immediately after an I/O interrupt.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
	TIO 1,2 = 11 Busy. The device failed to return to the ready state due to a hardware malfunction or the command list is coded with multiple interrupts.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
Step 3A. Performed only if Error flag ≠ 0 indicating a parity error (applicable to Sigma 2/3 computer systems only).	Error flag = 1 The Error flag in the odd channel register indicates that a parity error has been detected on bytes received during an input operation, or a memory parity error was detected during an output operation.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
	For Sigma 3 only. The following errors generate an IOP Halt to the device controller: 1. Detecting the memory parity error while fetching an order code from memory on order out. 2. Detecting a memory parity error while fetching a new IOCD from memory during a later chaining operation.							
Step 3B. Performed only if TDV 10, 11, 12, and 13 ≠ 0000 indicating an IOP operational error (applicable to Sigma 5-9 computer systems only).	TDV 11 = 1 Memory Address Error. This error may be due to a hardware malfunction or programming error.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
	TDV 12 = 1 IOP Memory Error. This error is due to a hardware malfunction.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
	TDV 13 = 1 IOP Control Error. This error is due to a hardware malfunction or programming error.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
	TDV 10 = 1 Transmission Memory Error. This error is due to a hardware malfunction.	X	X					Recovery Procedure 2.
				X	X	X	X	Recovery Procedure 3.
Step 4. Performed only if TDV 2 ≠ 0 indicating that a sector is unavailable (applicable to all computer systems).	TDV 2 = 1 Sector Unavailable. The surface address of the Seek operation is outside the range of available sectors, or the current surface operation has been aborted because the previous surface operation has incremented the surface address beyond the last available sector.	X						Recovery Procedure 2.
			X					Recovery Procedure 4.
				X	X	X	X	Recovery Procedure 3.

Table 9. Fault Testing Sequence (cont.)

Sequence and Summary Description	Configuration and Significance of Status Bits	Failing Order						Recommended Corrective Action (see Table 10)
		Seek	Sense	Read X'02'	Read X'12'	Write	Check-write	
Step 5. Performed only if TDV 3≠0 indicating a Write Protect violation (applicable to all computer systems).	TDV 3 = 1 Write Protect Violation. The addressed sector is write protected by manual hardware switches. The Write operation has been aborted.					X		Recovery Procedure 4.
Step 6. Performed for Sigma 2/3 computer systems only if OSB 0 ≠ 0. Performed for Sigma 5-9 computer systems if TDV 9 ≠ 0. Note: OSB = Operational Status Byte. OSB = Operational Status Byte	OSB 0 = 1 or TDV 9 = 1 Transmission Data Error. This error may be caused by any of the following: 1. Data Overrun. When the system fails to maintain data transfer rate required during Read, Write, or Check-write operations (TDV 0 will be set to a 1). 2. Check-write Error. When a data or parity error is detected during a Check-write operation. 3. Sync Pattern Error. The controller failed to synchronize with the device's data at the beginning of a surface (Read or Write) operation. 4. Sector Parity Error. The sector data parity failed to compare to the expected parity during a Read operation. 5. Interface Parity Error (Model 7231A02 only). A controller-device communication parity error has been detected.	X	X	X	X	X	X	Recovery Procedure 2. Recovery Procedure 3.
Step 7. Performed only if TIO 4≠0 indicating an unusual end (applicable to all computer systems).	TIO 4 = 1 Unusual End. If none of the above error indications are present, then the current operation was terminated with an unusual end due to any of the following: 1. Invalid order. 2. Power failure. 3. Incorrect Seek byte count (other than 2). 4. Incorrect Sense byte count (other than 3).	X	X	X	X	X	X	Recovery Procedure 2. Recovery Procedure 3.
Step 8. Performed only if the condition codes for a TDV instruction are CC1, CC2 ≠ 00 (Sigma 5-9) or if the Overflow and Carry indicators are O, C ≠ 00 (Sigma 2/3).	TDV CC1, CC2 = 01 or TDV O, C = 01 Operational Fault. The previous operation was terminated with a fault condition attributable to a hardware malfunction.	X	X	X	X	X	X	Recovery Procedure 2. Recovery Procedure 3.
Step 9. Performed only if TDV 8 ≠ 0 indicating an incorrect length error (Sigma 5-9) or if OSB 1 ≠ 0 (Sigma 2/3) (applicable to all computer systems).	TDV 8 = 1 or OSB 1 = 1 Incorrect Length. This bit is set whenever an incorrect length has been detected. Except for the Seek operation, this indication would not be considered an error (see SIL flag).	X	X	X	X	X	X	Recovery Procedure 2. Recovery Procedure 4.
Step 10.	Inconsistent Status Error. Whenever the device-dependent status has failed to indicate the specific failure for which the device-dependent status checking was invoked, it is considered a hardware malfunction.	X	X	X	X	X	X	Recovery Procedure 2. Recovery Procedure 3.

The recommended corrective action (column 9) for a specific fault depends on the failing order (columns 3-8). Generally, for failing Seek and Sense orders, a reference is made to Recovery Procedure 2, Table 10; for failing Read, Write, and Check-write orders, a reference is made to Recovery Procedure 3, Table 10.

Symbols used in the tables have the following meanings:

Symbol	Meaning
TIO "n"	nth bit of the status response received for a TIO instruction.
TDV "n"	nth bit of the status response received for a TDV instruction.
OSB 0 and OSB 1	Bits 0 and 1, respectively, of the Operational Status Byte returned to the even I/O channel register assigned to the RAD (Sigma 2/3 computers only).
Error Flag	Bit 0 of the odd I/O channel register assigned to the RAD (Sigma 2/3 computers only).

The status of a particular bit is shown by equating the symbol to a 1 or a 0 (e.g., TDV = 1). The simultaneous status of more than one bit is shown by equating a series of symbols (each representing a status response bit) to a binary number. The binary digit for a particular symbol occupies the same relative position within the binary number as the symbol does within the series. For example, "TIO 1,2 = 10" signifies that TIO 1 is set to a 1 while at the same time TIO 2 is set to a 0.

IRRECOVERABLE ERRORS

If a particular fault condition persists after performing the recommended recovery procedure, the fault is irrecoverable. Specific action to be taken after an irrecoverable fault will vary with the order and with the user's application. For example, in the case of Sense failures, the system may tolerate such faults, whereas Read failures may require a range of action such as job abortion to shutting the system down. On the other hand, an irrecoverable Write failure may require the choosing of another surface area (sector and/or track) and disallowing further operations on the failing surface area.

Table 10. Recommended Recovery Procedures

Recovery Procedure Number	Description
1	Abort – Operator Intervention. All operations on the device must be aborted and operator notification given that the device is not operational.
2	Order Retry – Program Recovery. An HIO instruction should be issued (in the case of controller and/or device not ready) and the operation retried. This recovery sequence should be retried ten times before considering the operation irrecoverable.
3	Order Retry After Seek – Program Recovery. An HIO instruction is issued (in the case of controller and/or device not ready) and a Seek operation is performed to readdress the sector, followed by the operation that failed. This sequence should be retried ten times before considering the operation irrecoverable. In the case of Check-write operations, it may be necessary to rewrite the failing sector.
4	Program Notification. The program is notified that a Write Protect violation has occurred, an incorrect length was reported, or a Sense operation resulted in a sector unavailable condition.

APPENDIX

SIGMA 5-9 PROGRAMMING EXAMPLE

The following example is a subroutine for reading or writing data on the RAD in Sigma 5-9 computer systems. The subroutine assumes that the RAD is the only I/O device currently being used and that the main program sets up locations indicating the storage unit address, track and sector address, address of the I/O area in main core memory, and the number of bytes to be transferred.

The subroutine is called with the instruction BAL,15 RADREAD or BAL,15 RADWRITE. There are three possible returns that the subroutine can make to the main program:

1. If the operation is completed normally, return to calling location + 1.
2. If the operation cannot be started ("no I/O address recognition" or "SIO not accepted") return to calling location + 2.
3. If an error occurs during or upon completion of the operation, return to calling location + 3.

Label	Command	Argument	Comments
RADREAD	LD,R8	RDSORDER	Load R8 and R9 with read command pair.
	LI,R10	-1	Set read-write indicator for read.
	B	$ + 3	
RADWRITE	LD,R8	WRTORDER	Load R8 and R9 with write command pair.
	LI,R10	0	Set read-write indicator for write.
	OR,R8	BFRADDRS	Set up memory byte address (the main program stores an address in "BFRADDRS" before branching here).
	OR,R9	BYTCOUNT	Set up byte count (the main program sets this location before branching here).
	STD,R8	COMMLIST + 2	Save assembled command pair in command list.
	MTW,0	R10	
	BCS,1	IOINTSUP	Is this a write operation?
	LD,R8	COMMLIST + 6	Yes – set up check-write command pair.
	AND,R8	FLAGMASK	Save order field.
	AND,R9	FLAGMASK	Save flag field.
	OR,R8	BFRADDRS	Set up memory byte address.
	OR,R9	BYTCOUNT	Set up byte count.
	STD,R8	COMMLIST + 6	Store check-write command pair in command list.
IOINTSUP	LW,R8 STW,R8	DSCIOINT X'5C'	Get and store an "XPSD DSCINTPT" instruction into location 5C.
	LI,R8	X'20'	Set I/O interrupt arming bit.
	WD,R8	X'1200'	Arm and enable the I/O interrupt.
	LI,R0	DA(COMMLIST)	Load register 0 with the doubleword address of the first command pair in the command list.
	SIO,R10	*DISCADDR	Start disc operation ("DISCADDR" is set up by the main program and is the disc "unit address").
	STCF	DSCCSAVE	Save the condition code for the SIO.
	BCR,12	$ + 3	Was SIO accepted?
	MTW,1 B	R15 *R15	No – step return address once and return to the main program.

Label	Command	Argument	Comments
	WAIT		Yes – wait for the I/O interrupt.
DISCDONE	AIO,R10	0	Acknowledge the interrupt.
	STCF	DSCCSAVE	Save the AIO condition code
	LCF	DSCCSAVE	Get saved condition code.
	BCR,4	$ + 2	Did operation finish successfully?
	MTW,2	R15	No – add 2 to return address.
DISCEXIT	LI,R8	X'20'	Yes – disable and disarm the I/O interrupt.
	WD,R8	X'1100'	
	B	*R15	Return to the main program.
	:		
	BOUND	8	This is an assembler directive insuring that the following constants are on a doubleword boundary
RDSORDER	DATA	X'02000000'	Read command pair-flags = interrupt on channel end or
	DATA	X'1E000000'	unusual end, halt on transmission error, and suppress incorrect length.
WRTORDER	DATA	X'01000000'	Write command pair-flags = command chain, interrupt
	DATA	X'2E000000'	on unusual end, halt on error, and suppress incorrect length.
COMMLIST	DATA	X'03000800'	Seek command pair – the address 800 is the byte address
+1	DATA	X'2E000002'	of a location (200) where the main program stores the track and sector address for the read or write operation, the byte count is 2, and the flags are the same as the write flags above.
+2	DATA	0	The read or write command pair are stored here.
+3	DATA	0	
+4	DATA	X'03000800'	Seek command pair – this command is used on a write
+5	DATA	X'2E000002'	operation and is identical to the one above.
+6	DATA	X'05000000'	Checkwrite command pair – this command pair is exe-
+7	DATA	X'1E000000'	cuted on a write operation to verify data on the disc from the write just executed.
FLAGMASK	DATA	X'FF000000'	"Order" and "flag" field mask.
DSCIOINT	XPSD	DSCINPT	This instruction is stored in X'5C'.
DSCINTPT	DATA	0	When the I/O interrupt occurs, the program status double-
	DATA	0	word is saved in "DSCINTPT" and "DSCINTPT + 1" and
	DATA	DISCDONE	the program branches to "DISCDONE".
	DATA	0	
DSCCSAVE	DATA	0	Temporary storage for condition code.
	:		
	MAIN PROGRAM		
BFRADDRS	DATA	---	This location contains the address of the I/O buffer area.
BYTCOUNT	DATA	---	This location contains the byte count.
DISCADDR	DATA	---	This location will contain the unit address.
	:		

Label	Command	Argument	Comments
	BAL,15	RADREAD	Call (branch to) RAD read routine; save return address in general register 15.
	B	RDONE or $ + 3	Normal return.
	B	RABNORM	Abnormal return (no I/O address recognition or RAD not operational).
	B	RERROR	Error return.
	:		
	BAL,15	RADWRITE	Call RAD write routine; save return address in general register 15.
	B	WDONE	Normal return.
	B	WABNORM	Abnormal return.
	B	WERROR	Error return.

SIGMA 2/3 PROGRAMMING EXAMPLE

The following example is a subroutine showing one way in which the RAD in a Sigma 2 or 3 computer system could be programmed. It assumes that no other I/O devices are in operation and certain locations have been set up by the main program before the subroutine is called. The subroutine is called with the instruction sequence:

```
RCPYI 1,2                    RCPYI 1,2
B     RADWRITE     or        B     RADREAD
```

There are three possible returns to the main program:

1. If the operation is completed normally, return to calling location + 1 in the main program.
2. If the operation cannot be started, return to calling location + 2.
3. If an error is encountered during or after the operation, return to calling location + 3.

The maximum record length that can be written or read in this routine is 8191 bytes. The data will be stored in a block of core memory, labeled "IOBUFFER", during a read operation. For a write operation, the data should be in this same area of main core memory prior to branching to this routine.

Label	Command	Argument	Comments
RADWRITE	LDA	WRITE	Get Write order.
	B	$ + 2	
RADREAD	LDA	READ	Get Read order.
	STA	ORDER	Save specified order.
	RCPY STA	2,7 RADRETN	Save the return address to the main program in location "RADRETN".
	LDA TIO	RADADDRS	Execute a TIO instruction to the unit addressed in location "RADADDRS" which is the unit address of the RAD.
	STA	TIOSTAT	Save TIO status response.
	RD	X'C0'	Save overflow and carry bits.
	AND	= 3	
	STA	TIOSTAT + 1	Save O and C indicators.
	BAZ	$ + 2	Overflow or carry set?
	B	EXIT - 1	Yes – Return to branch address + 2.
	LDA SCRS AND ADD STA RCPYI STA	RADADDRS 3 =X'E' =8 ECHANNEL 7,7 OCHANNEL	No – Generate the addresses of the even and odd channel registers for the unit addressed by "RADADDRS" (I/O channel x 2 + 8 = E; I/O channel x 2 + 9 = O). Save these addresses in locations "ECHANNEL" and "OCHANNEL", respectively.
	LDA WD	=SEEK *ECHANNEL	Set the word address of the Seek I/O table in the even channel register.
	LDA WD	=3 *OCHANNEL	Set the byte count for the Seek operation in the odd channel register (Order byte + 2 data bytes.)
	LDA	RADADDRS	Load accumulator with device address.
	SIO		Issue SIO to the addressed device.
	TIO		
	BNO	$ + 2	New SIO possible?
	B	$ - 2	No – Execute TIO again.

Label	Command	Argument	Comments
	RD	*ECHANNEL	Yes – Get operational status byte.
	AND	=X'C800'	Save TE, IL, and UE bits.
	RCPY	7,6	Save these bits in the extended accumulator.
	LDA	RADADDRS	Get the device status and combine with the opearional status byte indicators.
	TDV		
	ROR	6,7	
	BAZ	$ + 2	Did an error occur during the Seek?
	B	EXIT - 2	Yes – Return to branch address + 3.
	LDA	=RADINTPT	No – Store the interrupt processor starting address in the I/O in-
	STA	X'106'	terrupt location.
	LDA	=X'200'	Set I/O interrupt bit in accumulator.
	WD	*INTCNTL	Arm and enable the I/O interrupt.
	LDA	=ORDER	Set even I/O channel to the address of the specified order.
	WD	*ECHANNEL	
	LDA	=X'6001'	Set odd I/O channel for 1 byte (order) and set the data chaining
	WD	*OCHANNEL	and interrupt bits.
	LDA	COUNT	Set interrupt flag in odd channel word with byte count.
	OR	=X'2000'	
	STA	ORDER + 2	Save odd channel word.
	LDA	RADADDRS	Execute the specified order.
	SIO		
WAIT	WAIT		Wait for interrupt at channel end time.
RADINTPT	DATA	0	These two locations are to hold the Program Status Doubleword at
	DATA	0	the time the interrupt occurs.
	LDA	=X'200'	Disarm the I/O interrupt.
	WD	*INTCNTL1	
	AIO		Execute an AIO and save the status and address response. Save
	STA	AIOSTAT	the overflow and carry indicators.
	RD	X'C0'	
	AND	=3	
	STA	AIOSTAT+1	
	LDA	RADADDRS	Get device address.
	TIO		Get I/O status.
	AND	=X'6000'	Save device status bits.
	CP	=X'6000'	Check for "busy".
	BNC	$ + 5	Is device "busy"?
	LDA	=X'200'	Yes – arm and enable the I/O interrupt.
	WD	*INTCNTL	
	WD	X'D8'	Go back to WAIT until a "channel end" occurs.
	LDX	INTCNTL1	
	RD	*ECHANNEL	Get Operational Status Byte.
	AND	=X'C800'	Save TE, IL, and UE bits.
	STA	ERRSAVE	
	OR	AIOSTAT	Add AIO error bits.
	BAZ	$+3	Did an error occur on this operation?

Label	Command	Argument	Comments
	WD	X'D8'	Yes – Clear interrupt and return to branch address + 3.
	LDX	ERREXIT	
	WD	X'D8'	No – Clear interrupt and return to branch address + 1.
	LDX	NOERXIT	
	IM	RADRETN	Return to calling location + 3.
	IM	RADRETN	Return to calling location + 2.
EXIT	B	*RADRETN	Return to calling location + 1.
	CONSTANTS		
WRITE	DATA	X'01'	Write order.
READ	DATA	X'02'	Read order.
ORDER	DATA	0	Specified order.
	DATA	IOBUFFER	Starting address of I/O buffer area.
	DATA	0	Byte count + interrupt bit are stored here.
RADRETN	DATA	0	Return address to main program.
RADADDRS	DATA	X'F0'	Unit address of RAD.
ECHANNEL	DATA	X'16'	Even channel address.
OCHANNEL	DATA	X'17'	Odd channel address.
COUNT	DATA	0	Byte count.
ERRSAVE	DATA	0	Temporary storage for error bits.
INTCNTL	DATA	X'1200'	Arm and enable selected interrupts.
INTCNTLI	DATA	X'1100'	Disarm selected interrupts.
NOERXIT	DATA	WAIT	Interrupt WAIT.
ERREXIT	DATA	EXIT	
	DATA	EXIT - 2	
AIOSTAT	RES	2	AIO status storage registers.
TIOSTAT	RES	2	TIO status storage registers.
SEEK	DATA	X'03'	Seek order.
TRAKSECT	DATA	0	Track and sector address for specified operation.
	MAIN PROGRAM		
	•		
	•		
	•		
	RCPYI	1,2	
	B	RADWRITE	Calling instruction for write operation.
	B	WDONE	Normal return.
	B	WABNORM	Abnormal return.
	B	WERROR	Error return.
	•		
	•		
	•		
	RCPYI	1,2	
	B	RADREAD	Calling instruction for read operation.
	B	RDONE	Normal return.
	B	RABNORM	Abnormal return.
	B	RERROR	Error return.

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