900973E
INTERFACE DESIGN MANUAL

XEROX

SIGMA COMPUTER SYSTEMS

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SECTION I
GENERAL INFORMATION

INTRODUCTION

The Interface Design Manual (IDM) was prepared to assist engineers in connecting external equipment to Xerox Sigma computers. It describes compatible interfaces for all configurations of Sigma series equipment.

For information on the use of Xerox T-Series integrated circuit modules, see Xerox T-Series Integrated Circuit Logic Modules Description and Specifications Bulletin 64-51-03R, which can be obtained from the local Xerox representative or directly from corporate headquarters.

Note

Timing information, signal nomenclature, and systems cabling descriptions included in the IDM are not authorized for use as maintenance data.

The Sigma interface line-up consists of:

1. Direct Input/Output (DIO), also called Read Direct/Write Direct Interface
2. Input/Output Processor (IOP) Interface
3. Sigma 2 16-Bit Memory Interface
4. Sigma 3 16-Bit Memory Interface
5. 32-Bit Memory Interface
6. Interrupt and External Real-Time Clock Interface

DIO INTERFACE

The DIO interface provides input or output paths for central processing unit (CPU) communication with external devices to transmit or to receive data and control information.

The DIO interface is controlled by the Read Direct (RD) or by the Write Direct (WD) instructions. Each RD or WD instruction presents the 16 least significant bits of the effective address at the interface together with a control signal. The external unit addressed must then acknowledge the call to enable instruction execution. Direct input/output is the simplest means of transferring data or control information between the CPU and any unit. A unit requires less control logic to connect to the DIO interface than to connect to an IOP or directly to memory.

However, a CPU instruction is necessary for every word transferred. Therefore a unit on the DIO interface generally requires more CPU time than when other methods are used. Also, a unit on the DIO interface may need an interrupt level to call in the CPU.

The DIO interface consists of data lines, address lines, RD/WD selection line, function strobe line, function strobe acknowledge line, status lines, I/O reset line, and 1.024-MHz clock line.

Most Xerox equipment designed to operate on the DIO interface will function satisfactorily with the Sigma 2, 3, 5, or 7 computer. For specific information, refer to the applicable computer reference manual.

IOP INTERFACE

The IOP interface provides lines through which peripheral units are controlled by a Sigma CPU and lines for data exchange between peripherals and core memories. The IOP interface is characterized by automatic operation. Following program initiation, data transfers occur automatically and without further direct program intervention.

The IOP interface consists of data lines, function lines, status lines, control lines (strobes, acknowledgments, and so forth), priority determination lines, service request lines, miscellaneous lines.

16-BIT AND 32-BIT MEMORY INTERFACES

The 16-bit memory interfaces in Sigma 2 and Sigma 3 and the 32-bit Sigma 5 and 7 memory interfaces provide direct data interchange between external devices and the Sigma memories. The Sigma 2 and 3 memory systems store 64K words maximum; Sigma 5 and 7 each store 128K words maximum. The memory interfaces are characterized by simplicity, a high data transfer rate, and a maximum flexibility of control.

The memory interfaces consist of data lines, address lines, control lines (request, acknowledge, and so on) and miscellaneous lines.

Each standard device, CPU, IOP, or special device which requires a direct connection to memory communicates with memory on its own bus. Although seldom necessary, special external devices can share a memory bus if related logic is included to resolve access conflicts.

INTERRUPT AND CLOCK INTERFACE

The external interrupt interface provides peripheral devices with the means of notifying the CPU of the need for service. The several external interrupt chassis can be located in the CPU or elsewhere. The real-time clock interface is located at the CPU and enables users to run real-time programs at desired rates.

Sigma 5 and 7 computers accept a maximum of 14 interrupt chassis with each chassis providing up to 16 interrupt levels. In Sigma 2, one group of four integral levels and eight external chassis of 16 levels are available. In Sigma 3, one group of four integral levels and six internal chassis of 16 levels each are available. Three cables are

used to interface a priority (external) interrupt control chassis and user equipment.

The interrupt and clock interface consists of:

Interrupt request lines
Interrupt acknowledge lines
I/O reset line
External real-time clock input lines

CABLING

SELECTION OF COMPONENTS

The use of Xerox cabling, cable drivers, and cable receivers as tie-ins to power supplies is essential for the following reasons:

1. Design, fit, and function of Xerox cables, cable drivers, and cable receivers are matched to the usage.

2. Xerox components provide verified efficiency and reliability.

3. No effort need be expended in converting data in the interface design manual (IDM).

4. A monetary loss would result if substitute components failed to perform all required functions or fell short of Xerox performance criteria.

5. Xerox must disclaim a responsible supplier interest in interface installations where substitute cabling, cable drivers, or cable receivers have been employed.

CABLE LAYOUT

All interfaces described in this manual, except the Sigma 3 memory interface, use the same cable driver- receiver scheme and the same means of interunit cabling (figures 1-1 through 1-3). Interunit cabling consists of several cables, with each cable consisting of 14 shielded wires (for characteristics refer to section VIII). Each shielded wire used as a transmission line is terminated with a 33-ohm characteristic impedance at each end (figure 1-4). Connection to this line is made by tapping the line without unduly affecting the characteristic impedance. A number of cables are used to handle all signals associated with each interface. These are:

DIO interface	Three cables for Sigma 2 or 3
	Four cables for Sigma 5 or 7
IOP interface to device controller — one-byte interface	Four cables for all (three signal cables plus a single priority-determination cable)
IOP interface to device controller — four-byte interface	Six cables for all (five signal cables plus priority determination cable)
Memory interface	Three cables for Sigma 2
	Two ribbon cables for Sigma 3
	Five cables for Sigma 5
	Five cables for Sigma 7
Interrupt interface	One, two, or three cables for all (depending on the number of interrupts)

For all signals on 33-ohm cables (except device controller priority determination signals), each unit may tap any line with both a cable driver and a cable receiver. The following conventions are used:

Logical one, +2 volts — Driver output = low impedance

Logical zero, 0 volts — Driver output = high impedance

DRIVER-RECEIVER CIRCUITS

The quiescent state of any time-shared line is high impedance from the driver (logical zero). A unit whose driver is active on a given line may bring that line to the logical one state using the driver circuit shown in figure 1-5. Receiver circuits similarly tap the common line for each signal. Receivers incorporate high-noise-rejection discriminator circuits. No inversion exists in either drivers or receivers. If the input to a driver is a logical one (+4 volts), the line driven goes to logical one (+2 volts). If a line is at logical one (+2 volts), the receiver output is at logical one (+4 volts).

Priority determination signals are similar except that only one driver and one receiver are normally connected to each line. Signals are received by each unit through standard logic elements and then may or may not be routed to the next unit.

CABLE-TO-MODULE CONNECTIONS

Except for length and the special offset cable described in section VII, all interunit cabling is physically identical. The cables do not include special components or circuits and are directly connected to edge contacts on the various cable driver-receiver modules. The cable driver-receiver modules can be inserted in any slot (except adjacent slots) in a standard Sigma chassis. Standard slots are provided for standard interfaces. The modules should be wired into these slots for ease of identification by customer servicemen. Cable driver-receiver modules cannot be located in adjacent module slots because of space limitations. At least one module of some other type or an unused connector slot must be provided between cable driver-receiver modules.

Each driver-receiver module can accept two cables mechanically sandwiched to the module (figure 1-6). Thus, interunit cabling comprises one long transmission line with drivers and receivers connected at each unit. The last unit on the transmission line at each end must have a terminator attached to the line in place of the cable that would otherwise start from that point (as shown in figure 1-7).

TESTING EXTERNAL SIGNALS

Either RD or WD instructions can be used to select and to test an external condition and to transmit the results of that test on two sense lines at the interface. Test results are stored in condition code bits 3 and 4 in Sigma 5 or 7, or in the overflow and carry bits in Sigma 2 or 3. Program instructions permit these flags to be tested with branching based on their state.

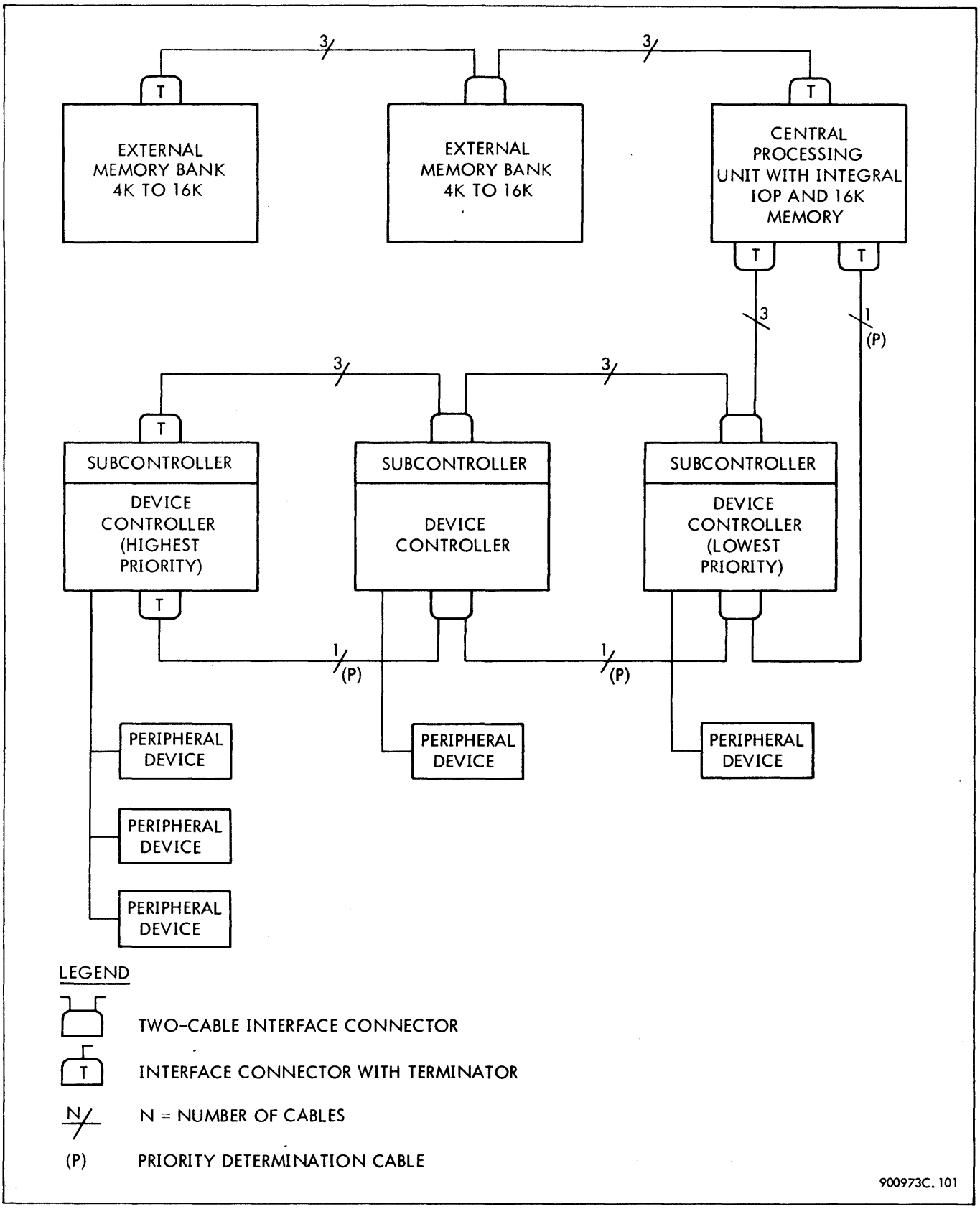


Figure 1-1. Typical Sigma 2 Cabling Scheme

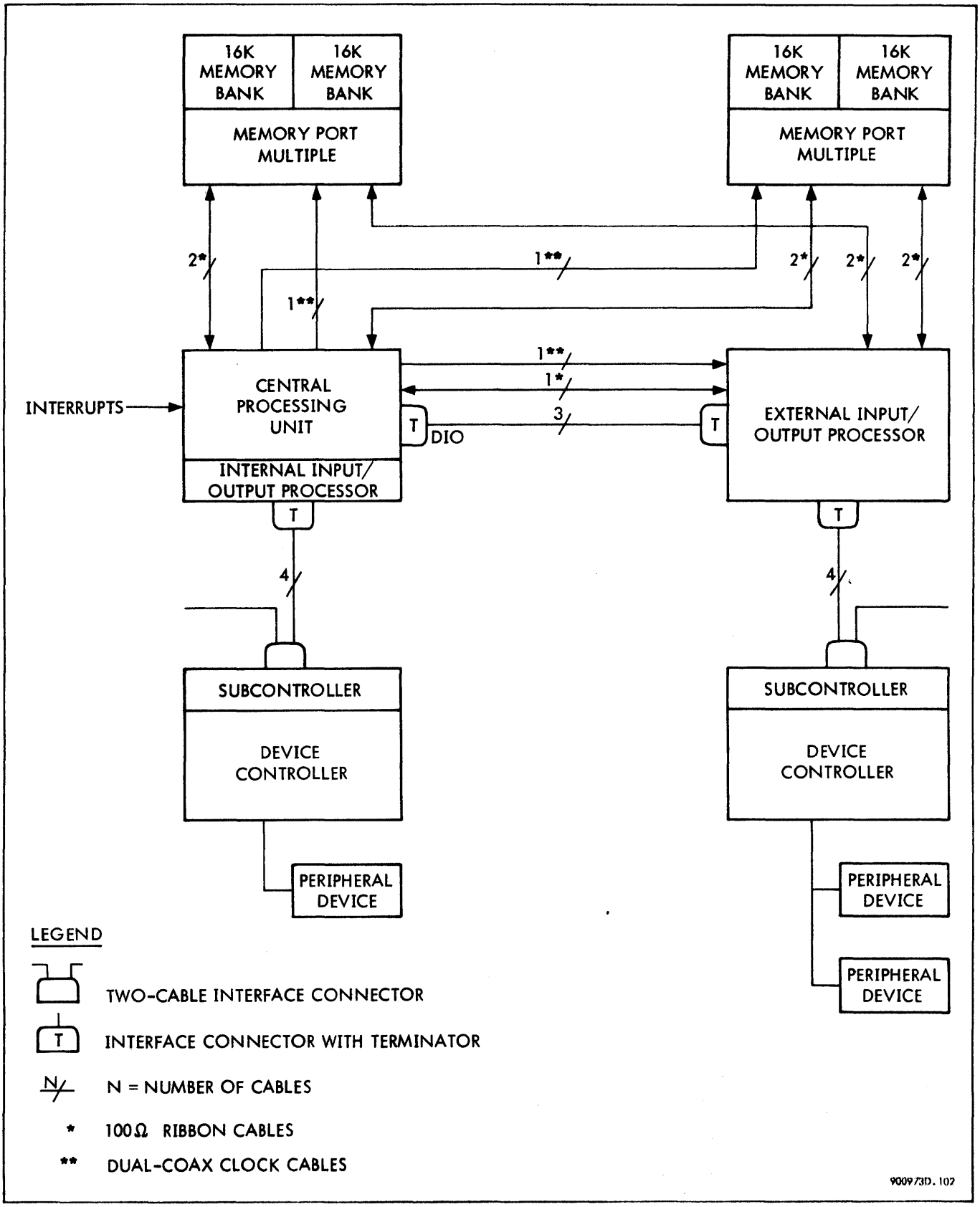


Figure 1-2. Typical Sigma 3 Cabling Scheme

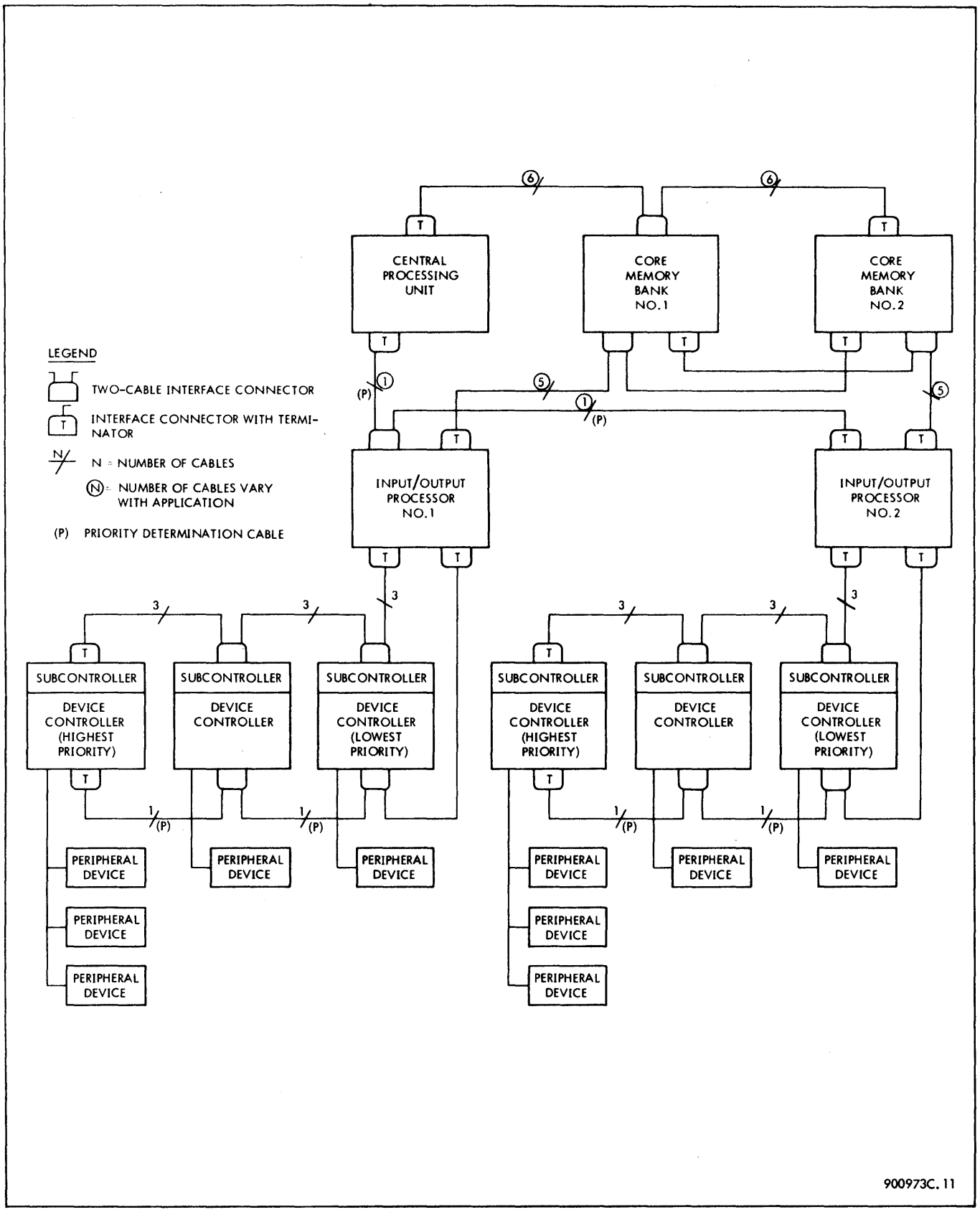


Figure 1-3. Typical Sigma 5 and 7 Cabling Scheme

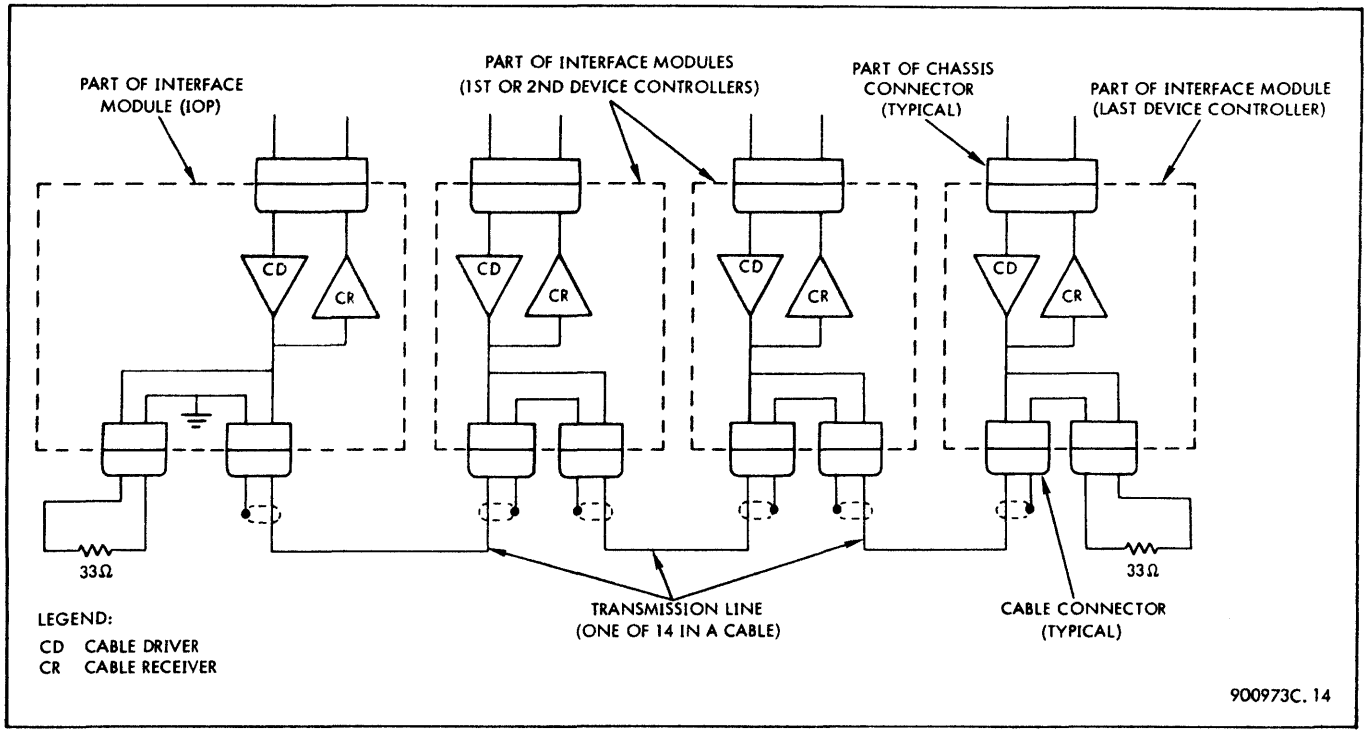


Figure 1-4. Typical Transmission Line Connections

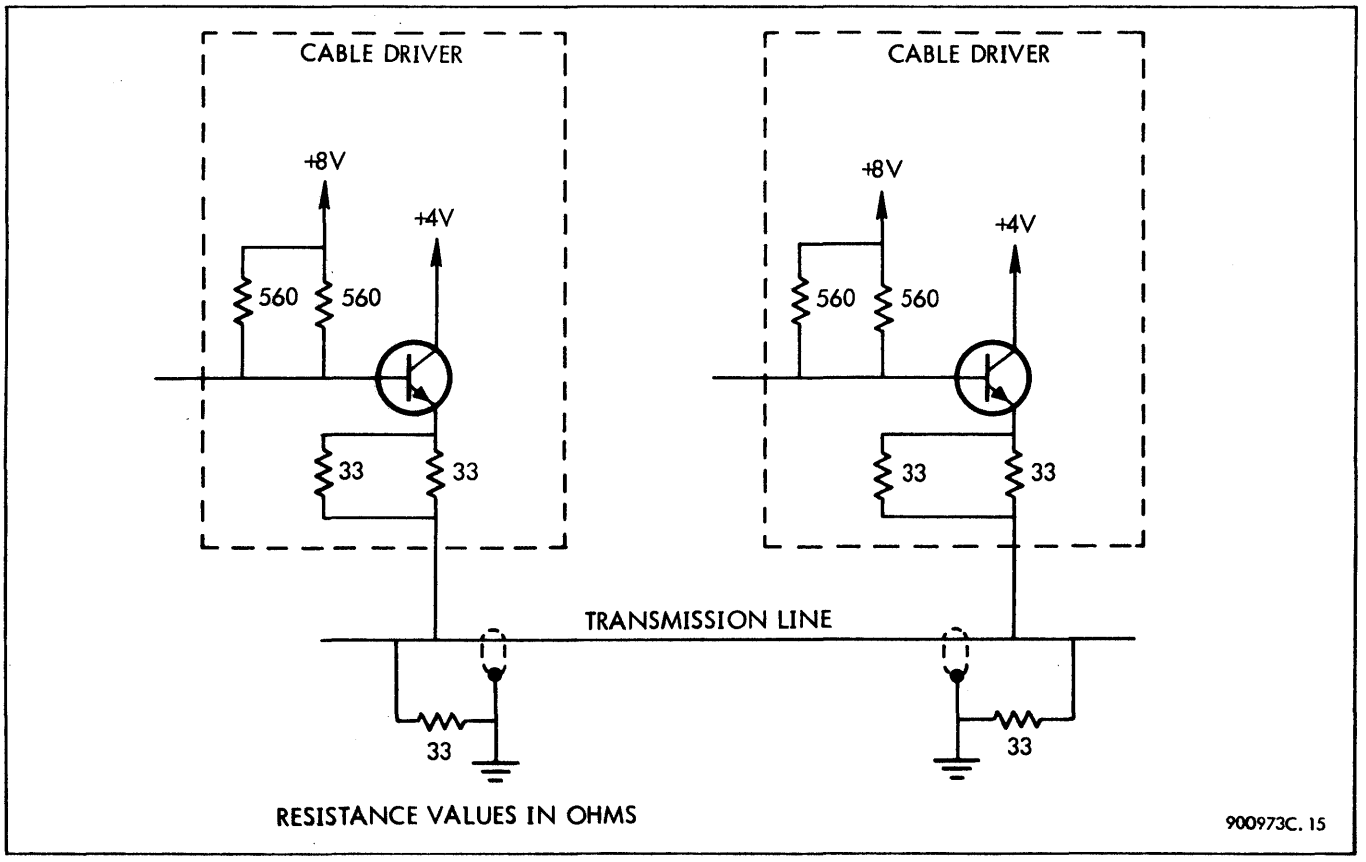


Figure 1-5. Cable Driver Circuit, Simplified Schematic Diagram

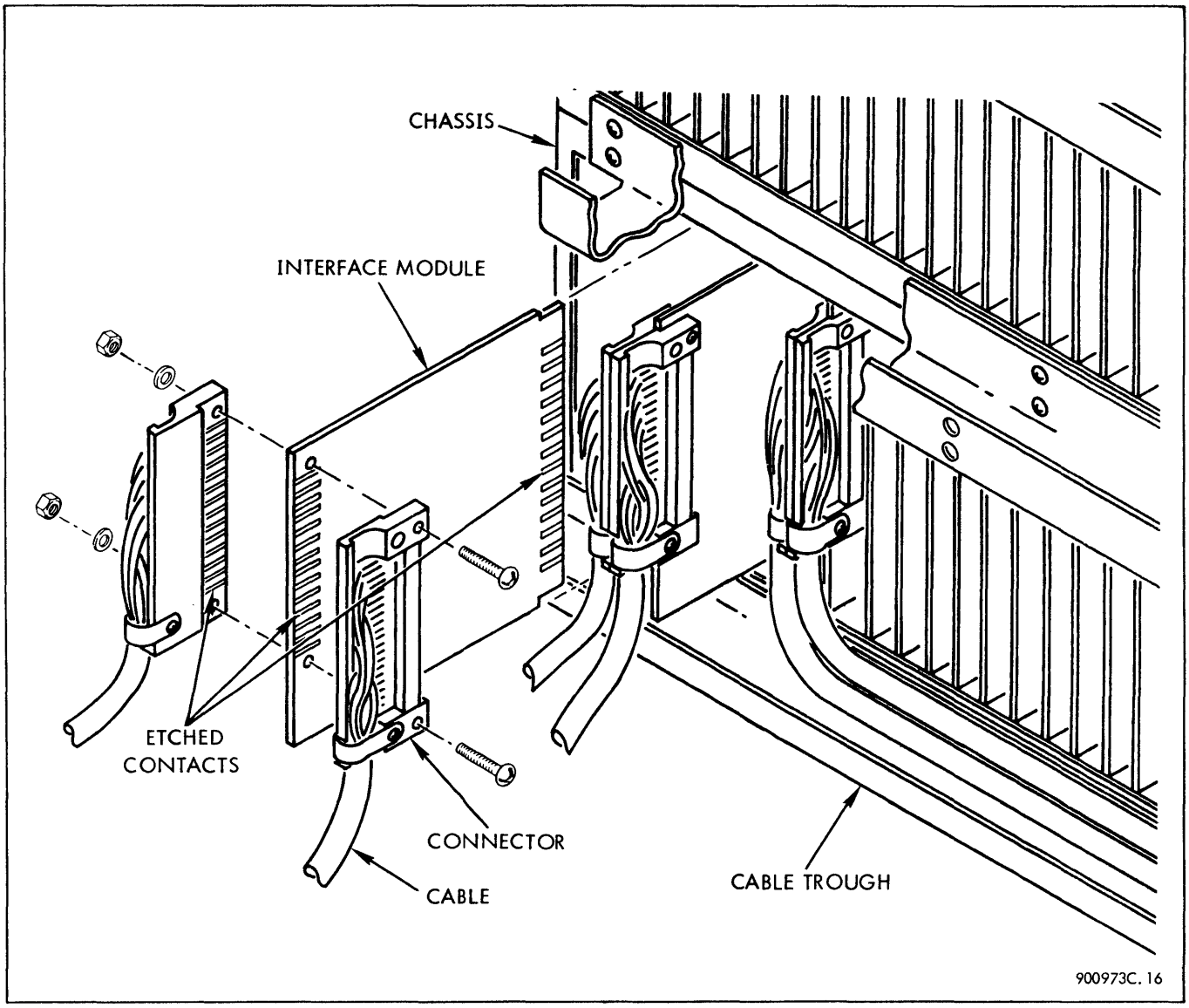


Figure 1-6. Interface Cable Connectors

DESIGN AIDS

The Sigma input/output system design concept emphasizes ease of component connection and separation. The interface design engineer should therefore ascertain that he has followed the following basic considerations:

1. All cables (except the special offset cable described in section VI) should be identical except for length.

2. Cable receptacles should be located in the same place in each chassis assembly.

3. Similar assemblies should be connected in similar manner.

4. Cables should be connected in a trunk-to-tail manner.

5. Cable length restrictions (as stated in the IDM) should not be exceeded.

6. No more than 25 receivers or 25 drivers should be connected to one line.

7. No more than one transmitter should drive a given line to its positive level at a given time.

8. The end of each line is terminated by a 33-ohm resistor to ground.

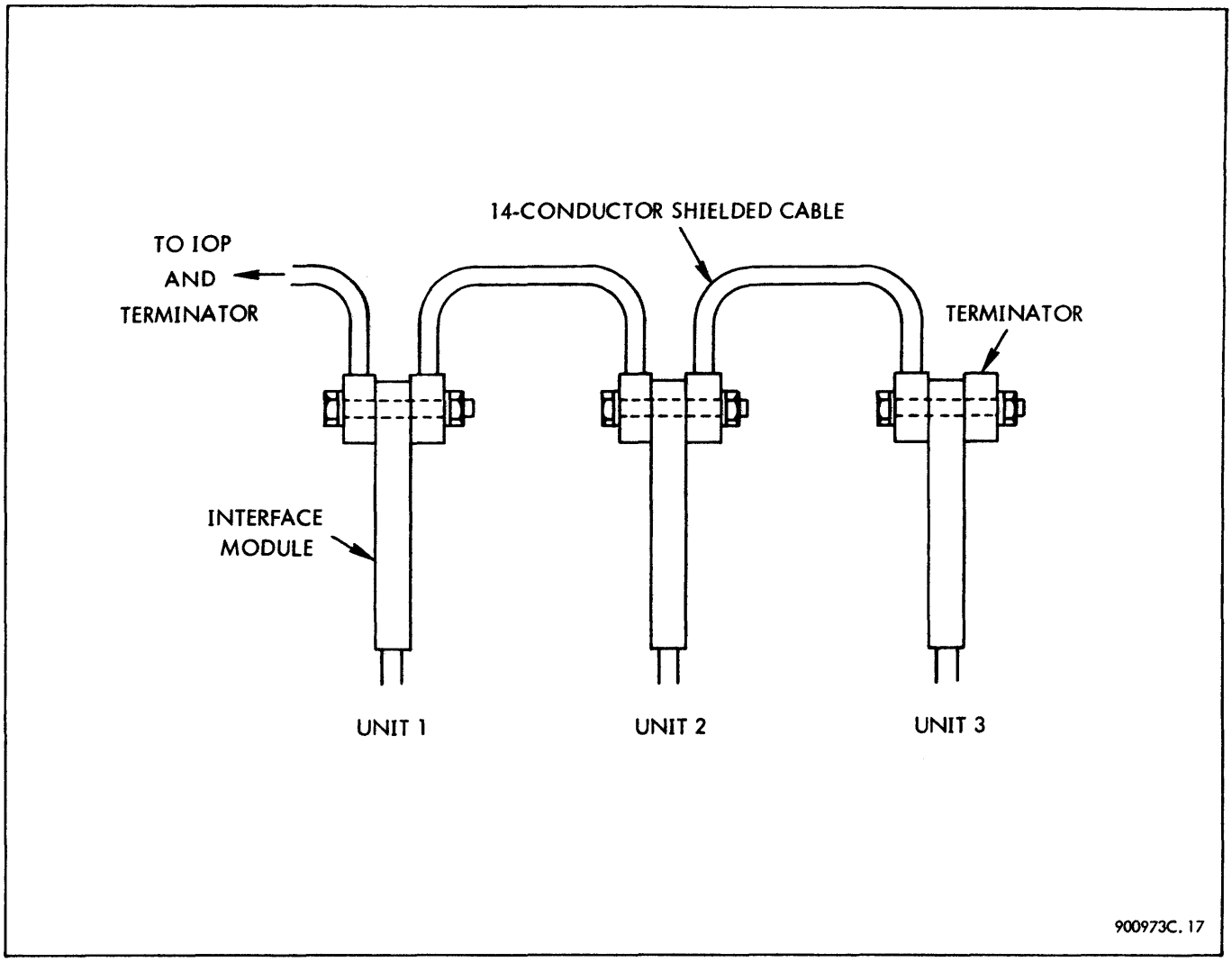


Figure 1-7. Cable and Terminator Connections

SECTION II

DIO INTERFACE

INTRODUCTION

The Direct Input/Output (DIO) interface (figure 2-1) is controlled by the Read Direct (RD) and the Write Direct (WD) instructions. Each RD or WD instruction presents the 16 least significant bits of the effective address at the interface together with an FS (function strobe) control signal. The external unit must provide a function strobe acknowledge (FSA) signal to enable complete execution of the RD or the WD instruction.

During the RD instruction, the external unit may provide data (32 bits in Sigma 5 or 7 and 16 bits in Sigma 2 or 3) for storage in a computer register. This data is provided in conjunction with signal FSA. During the WD instruction, Sigma 5 or 7 presents 32 bits and Sigma 2 or 3 presents 16 bits of data to the external unit with signal FS. WD is transmitted on the same lines used to transmit input data during the RD instruction. The data lines are thus bidirectional and are time-shared for the two instructions.

Additional signals provided at the DIO interface are:

1. A signal that differentiates between RD and WD instructions for the external user (since RD and WD appear identical in all other respects).

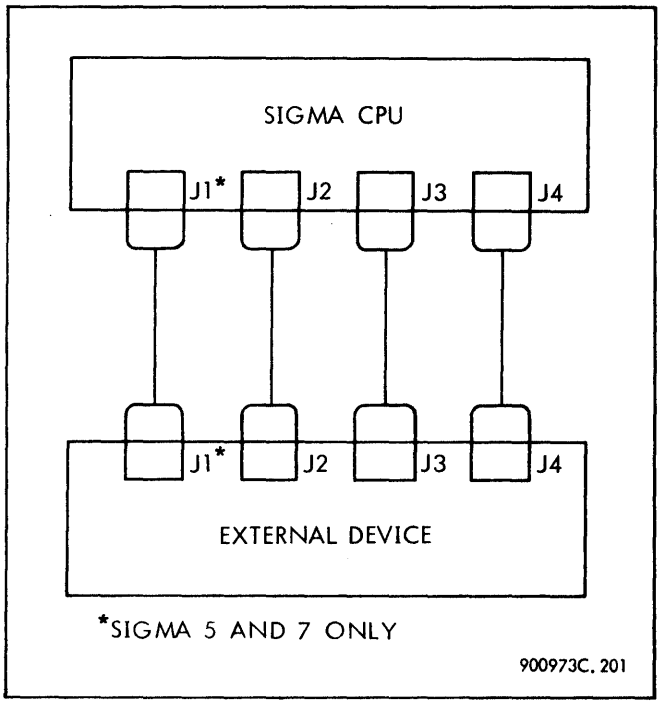


Figure 2-1. DIO Interface Diagram

2. Two input status lines. During either RD or WD instructions, these data lines set condition code bits 3 and 4 (CC3 and CC4) in Sigma 5 or 7 or set the overflow and carry bits in Sigma 2 or 3 (O and C).

3. An input/output reset signal.

4. A 1.024-MHz clock signal (not synchronized with instruction execution).

For a listing of DIO interface signals, refer to table 8-2.

INTERFACE DESCRIPTION

DATA LINES

Thirty-two bidirectional data lines are available on Sigma 5 or 7 and 16 lines on Sigma 2 or 3. When an RD or a WD instruction is not being executed, these data lines are in an undefined state, that is, the lines may be high, low, or changing.

During execution of a WD instruction, the CPU puts data on the lines to obtain stability for at least 360 nanoseconds (ns) before the function strobe is raised. The date lines remain stable for at least 200 ns after the CPU lowers the function strobe. (The times given are at the CPU driver outputs.)

During execution of an RD instruction, the addressed external unit places data on the lines with the FSA response signal. Data must be steady at the CPU receiver input no later than 160 ns after FSA reaches the CPU receiver input. The external device must continue to hold the data lines stable until the falling edge of the function strobe has been detected.

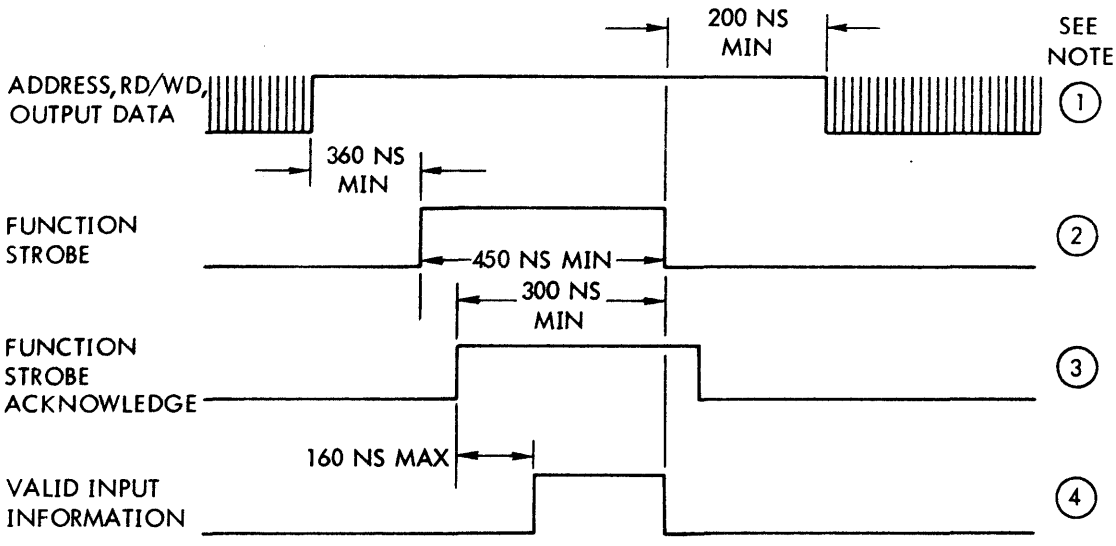
All timing is measured at the output of the CPU cable drivers for signals arriving from the CPU. All timing is measured at the input to the CPU cable receiver for signals being sent to the CPU. When measuring delays between signals, all measurements are made at the 50-percent point of the voltage waveforms. Figure 2-2 is a diagram of RD/WD timing.

ADDRESS LINES (A00R-A15R)

The 16 address lines are driven only by the CPU. Timing is identical to that of the data lines during a WD instruction (figure 2-2). Address line information consists of the effective address (16 least significant bits) of the WD or RD instruction.

READ DIRECT/WRITE DIRECT SELECTION LINE (RWDR)

The CPU drives one line to enable external devices to distinguish between a WD (output) and an RD (input) instruction. Timing is the same as for the address lines and the data lines during output. The selection line is driven high for WD and low for RD.



NOTES :

(1) THESE LINES MAY REMAIN HIGH, LOW, OR MAY BE CHANGING UNTIL SUCCEEDING USAGE

(2) THE CPU HOLDS THIS LINE HIGH UNTIL THE FUNCTION STROBE ACKNOWLEDGE SIGNAL IS RECEIVED FROM THE DEVICE. HOWEVER, IF THE SIGMA 3 INTERFACE TIMER IS IN USE, THE SIGMA 3 CPU WILL ABORT THE RD/WD INSTRUCTION AND DROP FS IF FSA IS NOT RECEIVED WITHIN 40 μS

(3) THE DEVICE MUST LOWER THIS LINE WHEN LOWERING OF THE FUNCTION STROBE HAS BEEN DETECTED. IF NOT LOWERED, SOME PROCESSORS MAY FAIL TO EXECUTE THE SUCCEEDING INSTRUCTION

(4) TIME PERIOD DURING WHICH EXTERNAL UNIT MUST GUARANTEE STABILITY OF INPUT DATA TO STATUS LINES AND TO DATA LINES FOR RD

(5) TIMES SHOWN ARE AT THE OUTPUT OF THE CPU CABLE DRIVERS OR THE INPUT TO CPU CABLE RECEIVERS

(6) WHERE MINIMUM AND MAXIMUM DELAY TIMES ARE NOT CLEARLY SPECIFIED, FULL RANGES ARE IMPLIED. FOR EXAMPLE, THE ADDRESS FALLING EDGE RELATIVE TO THE FUNCTION STROBE FALLING EDGE IS SHOWN TO BE 200 NS MINIMUM. THIS IMPLIES THAT THE MAXIMUM DELAY TIME MAY BE INFINITE OR UNTIL THE NEXT USAGE

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Figure 2-2. RD/WD (External Mode), Timing Diagram

FUNCTION STROBE AND ACKNOWLEDGMENT LINES (RFSR AND RFSAD)

The DIO interface is alerted and synchronization is obtained by means of the FSS and the FSA signals. Upon executing a WD or a RD instruction, the CPU sets address lines, the RD/WD selection line, data lines (for a WD instruction) and then raises FS after a minimum delay of 360 ns at the driver output. The external device which recognizes the address responds by raising FSA. Upon detecting FSA, the CPU lowers FS after a minimum delay of 300 ns. The external device should then respond to the falling edge of FS by removing all signals from the interface without delay.

STATUS LINES (CC3D AND CC4D)

Two lines allow the external device to send two status bits to the CPU for either WD or RD instructions. The timing requirement for these two signals is the same as for input data during an RD instruction. Only the device addressed may raise these lines.

I/O RESET LINE (RSTR)

The I/O reset line is raised in response to manual setting of the applicable control panel switches or during a power-on or a power-off sequence. The applicable control panel switches are the I/O RESET and SYS RESET on Sigma 5 and 7, the INITIALIZE switch on Sigma 2, and the RESET switch on Sigma 3.

1.024-MHz CLOCK (CL1R)

A 1.024-MHz clock signal is available for use by devices connected to the DIO interface. The line is continuously driven by the CPU regardless of the CPU function in progress. The signal is a square wave of approximately 50 percent duty cycle with a crystal-controlled frequency of 1.024 MHz (±0.02 percent long-term stability).

BASIS INSTRUCTIONS

DATA INPUT

The RD instruction presents the 16 low-order effective address on the DIO interface address lines together with a signal that indicates execution of the RD instruction. The selected external device generates an acknowledge signal and presents data on the DIO interface data lines, as well as two bits of status information on the two status lines. In Sigma 5 or 7, if the R-field (the register-specifying field in the instruction) is not equal to zero, the 32 data bits are stored in the specified register. If the R-field equals zero, the 32 data lines are disregarded, but bits CC3 and CC4 are still set as specified by the external device. In Sigma 2 or 3, the RD instruction is the same as in Sigma 5 or 7 except that only 16 bits of data are accepted and are stored in the accumulator. The status input lines are stored in the Sigma 2 or 3 overflow and carry indicators.

DATA OUTPUT

In Sigma 5 and 7, the WD instruction presents the 16 low-order bits of effective address on the DIO interface address lines together with a signal that indicates execution of the WD instruction. The selected external device generates an acknowledge signal and may accept 32 bits of data from the DIO interface data lines. The computer simultaneously accepts two bits of status information on two other lines to set bits CC3 and CC4. If the R-field is not equal to zero, the 32 bits of the specified register are transmitted on the 32 data lines. If the R-field equals zero, the 32 data lines are set at logical zero regardless of the contents of any register, but bits CC3 and CC4 are still set as specified by the external device.

On Sigma 2 or 3, the WD instruction is the same as Sigma 5 and 7 except that only 16 bits of data are transmitted from the accumulator. The status input lines are stored in the overflow and carry indicators.

EFFECTIVE ADDRESS ASSIGNMENTS

The general area controlled by an RD or WD instruction is specified by the four high-order bits of the address which appear on the I/O bus. These bits designate the control mode. Control mode assignments are as follows:

Hexadecimal	Definition
0	Internal computer control
1	Interrupt control (WD instruction only)
2	Xerox testers
3 through E	Reserved for assignment by Xerox for use in standard products
F	Systems special units (for customer use with specially designed equipment)

A list of effective address assignments for control modes 0 through E is maintained by the Xerox Product Planning Department. For detailed coverage of effective address assignments, refer to the applicable Sigma reference manual. For all standard product effective address assignments, the reservation of a particular code applies to all Sigma computers.

DESIGN AIDS

CABLE DRIVERS

Cable drivers may be driven by any standard Xerox logic circuit, including flip-flop outputs. However, the following considerations should be noted:

1. The cable driver circuit takes nine unit loads (one unit load equals 3.8 MA).

2. The nominal output of standard Sigma logic elements is 16 unit loads.

3. Pull-up resistors draw two unit loads.

4. Terminating resistors draw five unit loads.

5. Terminating resistors should not be used on circuits that feed cable driver inputs (any circuit can feed one cable driver and five other loads).

6. The driving source should use no pull-up resistors for a cable driver input.

7. Insofar as possible, circuits feeding cable drivers should not be used to drive other points.

CIRCUITRY FOR FUNCTION STROBE ACKNOWLEDGE

Figure 2-3 shows a circuit for obtaining the FSA signal.

EXTERNAL DEVICE INPUTS

An external unit should utilize the DIO interface for the shortest possible period needed for information transfer. This guideline may be modified for an engineering or an economic tradeoff. During the period that an external unit employs the DIO interface, the CPU cannot execute additional instructions. Also, a watchdog timer trap may occur on some processors.

The designer of external equipment must ground inputs to drivers for the function strobe, RD/WD, I/O reset, the 1.024-MHz clock, address lines 0-15, unused data lines, and CC3 and CC4 if not used (refer to table 2-1).

Failure to release FSA may delay completion of instruction execution. Good design practice therefore is that the external unit release FSA as soon as the CPU has released FS.

Note that RD/WD is true for the WD instruction.

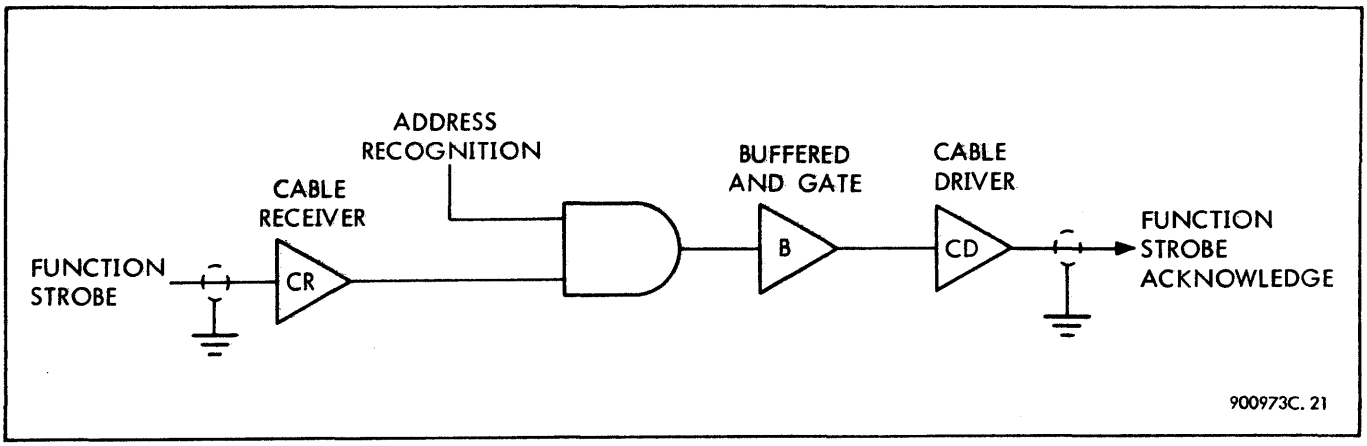


Figure 2-3. Function Strobe Acknowledge, Logic Diagram

Table 2-1. DIO Interface Signals

CABLE CONNECTOR PIN	BACKPANEL CONNECTOR PIN	SIGNAL NAME			
		Cable J1	Cable J2	Cable J3	Cable J4
1, A	2 6	DB1D DB1R	DB15D DB15R	DB29D DB29R	* A03R
2, B	1 4	DB0D DB0R	DB14D DB14R	DB28D DB28R	* A02R
3, C	9 10	DB3D DB3R	DB17D DB17R	DB31D DB31R	Unassigned
4, D	3 8	DB2D DB2R	DB16D DB16R	DB30D DB30R	* A04R
5, E	12 13	DB4D DB4R	DB18D DB18R	* FSR	* A00R
6, F	15 18	DB5D DB5R	DB19D DB19R	FSAD – –	* A01R
7, G	19 20	DB6D DB6R	DB20D DB20R	* RWDR	* A08R
8, H	23 22	DB7D DB7R	DB21D DB21R	* A05R	* A09R
9, K	25 27	DB8D DB8R	DB22D DB22R	* A06R	* A10R
10, L	33 34	DB9D DB9R	DB23D DB23R	* A07R	* A11R
11, M	35 36	DB10D DB10R	DB24D DB24R	* A12R	CC3D – –
12, N	37 38	DB11D DB11R	DB25D DB25R	* A13R	CC4D – –
13, P	39 40	DB12D DB12R	DB26D DB26R	* A14R	* RESR
14, R	45 42	DB13D DB13R	DB27D DB27R	* A15R	* 1MHZR
		Cable J1	Cable J2	Cable J3	Cable J4
MODULE LOCATOR	Sigma 2	– –	28A	30A	32A
	Sigma 3	– –	24A	26A	28A
	Sigma 5	09M	22Q	26Q	29Q
	Sigma 7	23S	27Q	30P	29N

*Must be hard-wired to ground

Notes

Data lines 0 through 15 not available on Sigma 2 and 3

Table listing is in relation to an AT11 type module

SECTION III

IOP INTERFACE

INTRODUCTION

Peripheral devices connect to Sigma series hardware through the following Input/Output Processor (IOP) interfaces:

Sigma 2 integral IOP

Sigma 3 integral IOP

Sigma 3 external IOP (EIOP)

Sigma 5 integral IOP

Sigma 5 or 7 multiplexer IOP (MIOP)

Sigma 5 or 7 selector IOP (SIOP)

The IOP interface provides lines through which peripherals are controlled by a CPU and provides lines for data exchange between peripherals and Sigma core memories. As shown in figure 3-1, a peripheral can be connected to the IOP interface with four, five, or six cables for the one byte, two byte or four byte data path, respectively. Table 3-1 is a listing of IOP interface cable signals at the device controller.

DEVICE CONTROLLERS

With the exceptions listed under Input/Output Processors in this section, all IOP's present the same interface and general signal interaction to a device controller (DC). Any peripheral device designed to operate on the eight-bit (one-byte) IOP interface described in this manual can connect to any type of IOP (subject to rate capabilities).

The IOP-DC interface uses an 8, 16 or 32-bit data path, which corresponds to one, two and four bytes, respectively. One data path is associated with each IOP in a system. Each data path is logically and electrically independent of other paths. If more than one DC is used, the additional DC's are interconnected to the first DC in a trunk-tail manner (see figure 3-2). All DC's time-share the single data path. Each peripheral device connects to the IOP through a device controller.

I/O SEQUENCE

A typical DC operational state flow diagram is shown in figure 9-1. Once a peripheral device has been started by the main computer program, the general I/O sequence is as follows:

1. All DC's in the busy state may request service simultaneously from the IOP. In an SIOP installation, only one DC can be busy per given instant.

2. The IOP brings up signals to activate a hard-wired priority chain between DC's. The highest priority DC that has requested service puts its device address on return lines together with an acknowledge signal and is then connected to the IOP.

3. A DC makes one of the following requests while connected to the IOP:

   a. Data out (DOUT) — data transfer from memory to the DC

   b. Data in (DIN) — data transfer from the DC to memory

   c. Order out (OOUT) — control information transfer from the IOP to the DC

   d. Order in (OIN) — control information transfer from the DC to the IOP

4. While connected to an IOP, a DC can transmit or receive up to four bytes of data (a record if it is connected to an SIOP) or one byte of control information and, in some cases, an additional byte for the terminal order. Each device is serviced in sequence by the IOP based on the hard-wired priority chain.

IOP INTERFACE LINE DESCRIPTION

Figure 3-1 shows IOP interface lines.

DATA LINES

The data lines (DA0-DA7, DB0-DB7, DC0-DC7, DD0-DD7) are multipurpose lines driven by either the IOP or the DC. The data lines transmit information during the following operations:

1. During execution of Start Input/Output (SIO), Halt Input/Output (HIO), Test Input/Output (TIO), and Test Device (TDV) instructions when the IOP sends a DC address (DA0-DA7 only)

2. Execution of Acknowledge Interrupt (AIO) instructions when a DC sends status to the IOP (DA0-DA7 only)

3. An order-out sequence when the IOP sends an order to a DC (DA0-DA7 only)

4. An order-in sequence when a DC sends an operational status byte to the IOP (DA0-DA7 only)

5. Data-out sequences when the IOP sends data to the DC (DA0-DA7, DB0-DB7, DC0-DC7, DD0-DD7)

6. Data-in sequences when a DC sends data to the IOP (DA0-DA7, DB0-DB7, DC0-DC7, DD0-DD7)

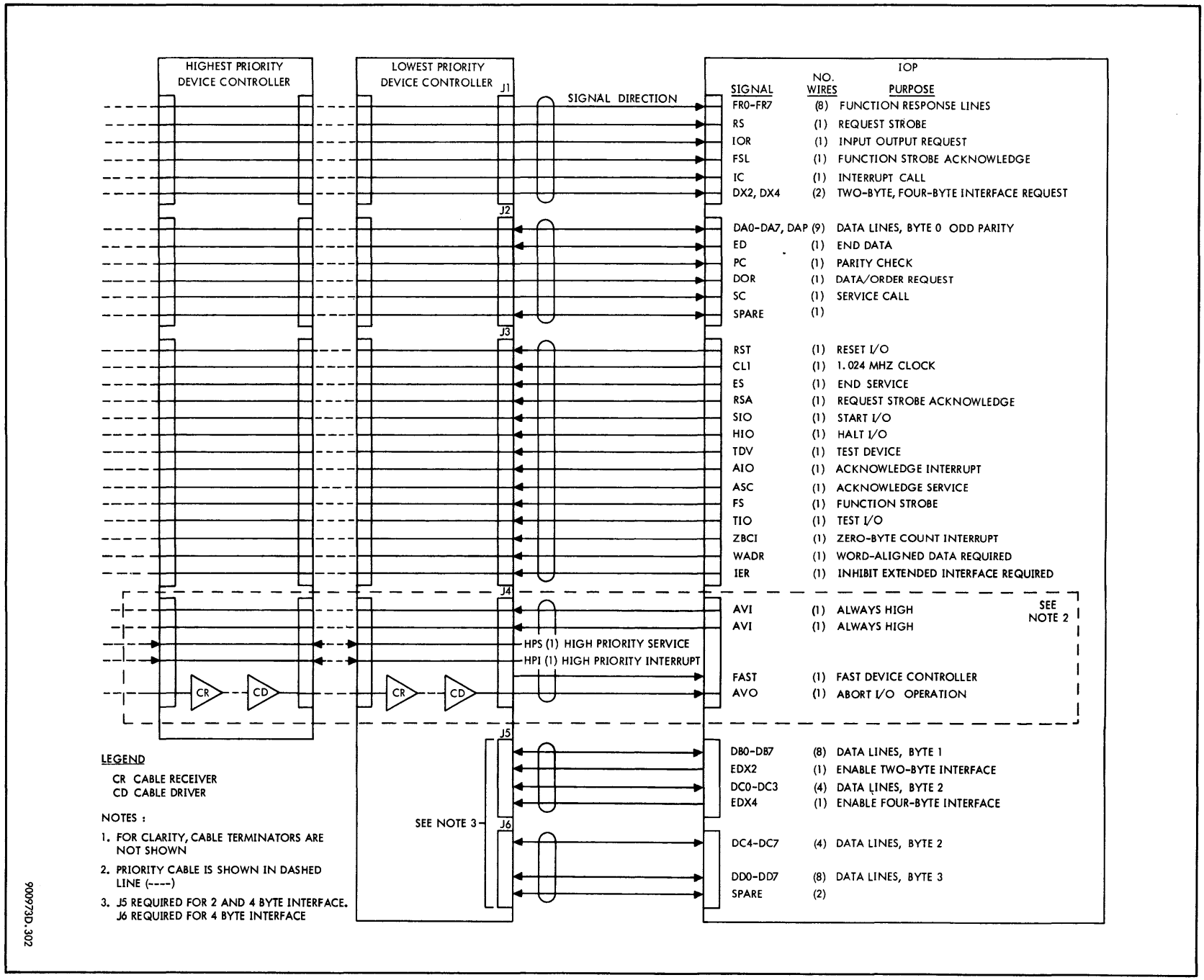


Figure 3-1. IOP Interface Signal Lines Diagram

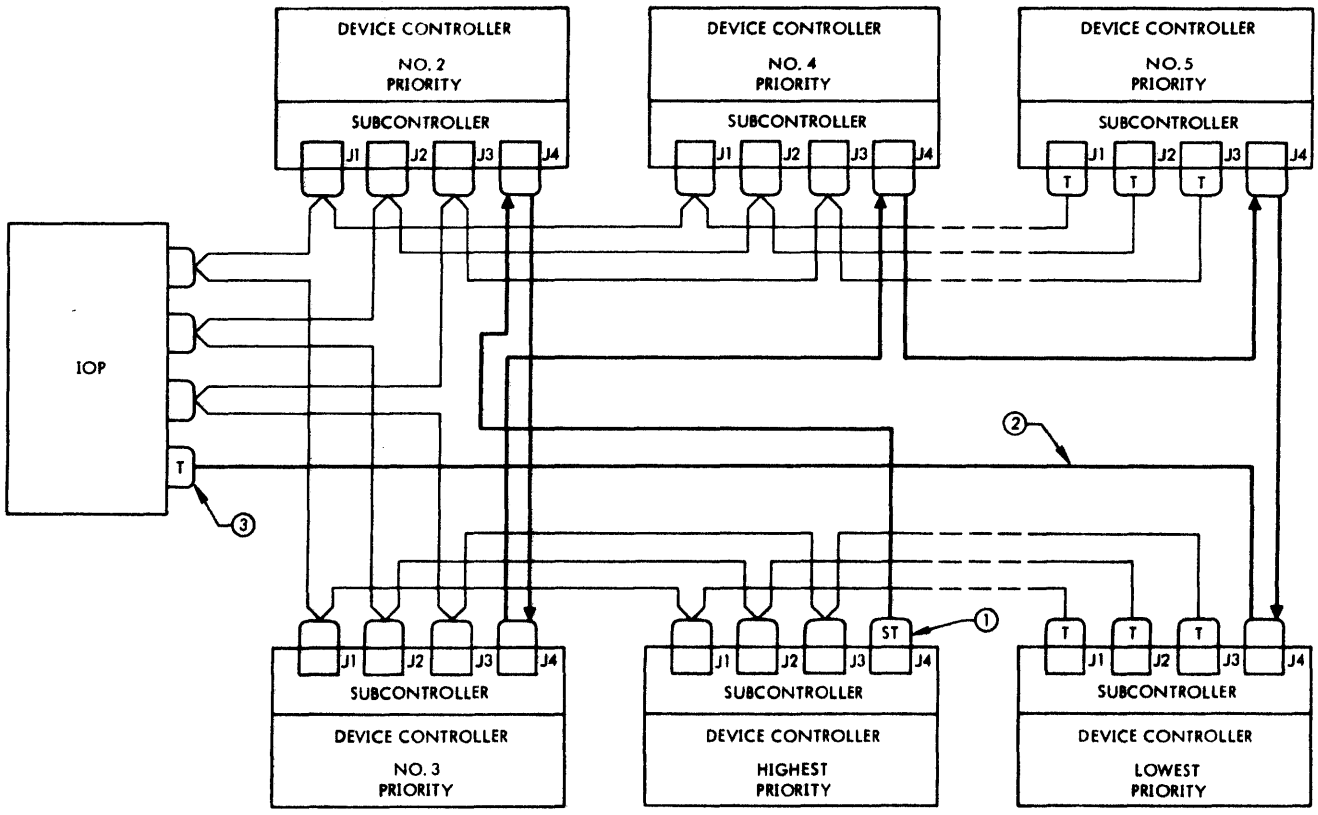
Table 3-1. IOP Interface Cable Signals at Device Controller

CABLE CONNECTOR PIN	BACKPANEL CONNECTOR PIN	SIGNAL NAME AT BACKPANEL					
		J1 AT12 Module	J2 AT11 Module	J3 AT10 Module	J4* AT17 Module	J5 AT11 Module	J6 AT11 Module
A, 1	2	FR7D	DA7D		(35) HPID	DB0D	DC4D
	6		DA7R	RESTR	(06) HPIR	DB0R	DC4R
B, 2	1	FR6D	DA6D		(33) HPSD	DB1D	DC5D
	4		DA6R	CL1R	(04) HPSR	DB1R	DC5R
C, 3	9	FR5D	DA5D		(31) FASTD	DB2D	DC6D
	10		DA5R	ESR		DB2R	DC6R
D, 4	3	FR4D	DA4D		(29) AVOD	DB3D	DC7D
	8		DA4R	RSAR	(08) AVIR	DB3R	DC7R
E, 5	12	FR3D	DA3D		**	DB4D	†
	13		DA3R	SIOR		DB4R	†
F, 6	15	FR2D	DA2D		**	DB5D	DD0D
	18		DA2R	HIOR		DB5R	DD1R
G, 7	19	FR1D	DA1D		**	DB6D	DD1D
	20		DA1R	TIOR		DB6R	DD1R
H, 8	23	FR0D	DA0D		**	DB7D	DD2D
	22		DA0R	TDVR		DB7R	DD2R
K, 9	25	RSD	DAPD		**		DD3D
	27		DAPR	AIOR		EDX2R	DD3R
L, 10	33	IORD	EDD		**	DC0D	DD4D
	34		EDR	ASCR		DC0R	DD4R
M, 11	35	FSLD	PCD		**	DC1D	DD5D
	36			FSR		DC1R	DD5R
N, 12	37	DX2D	DORD		**	DC2D	DD6D
	38			ZBCIR		DC2R	DD6R
P, 13	39	ICD	SCD		**	DC3D	DD7D
	40		SCR	WADRR		DC3R	DD7R
R, 14	45	DX4D	†		**		†
	42		†	IERR		EDX4R	†

*Backpanel connector pin for AT17 only

†Spare

**No cable driver-receiver available



NOTES: UNLESS OTHERWISE SPECIFIED

1. HIGHEST PRIORITY CONTROLLER TERMINATES THE PRIORITY CABLE WITH SPECIAL TERMINATOR XDS 128047
2. LOWEST PRIORITY CONTROLLER IS CONNECTED TO THE IOP J4
3. [T] DESIGNATES STANDARD TERMINATOR XDS 127315
4. ALL CABLE ASSEMBLIES ARE XDS 127314
5. CABLING BETWEEN CONNECTORS J1, J2, AND J3 FOLLOWS THE SHORTEST ROUTE
6. CABLING BETWEEN J4 CONNECTORS IS ROUTED IN RESPECT TO PRIORITY; THE CONTROLLER CLOSEST TO THE IOP HAS LOWEST PRIORITY

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Figure 3-2. Typical I/O Interconnections

7. When the IOP sends a terminal order to the DC in response to a DC request (DA0-DA7 only)

During data-in or data-out operations the data path may be one, two or four bytes wide depending on the IOP in use and the state of the EDX-DX control lines. Table 3-2 includes a summary of bit codes used on the data lines.

FUNCTION INDICATOR LINES

Function indicator lines SIO, HIO, TIO, TDV, AIO, and ASC are controlled by the IOP. These lines let the device know which I/O instruction the CPU is currently executing (SIO, HIO, TIO, TDV, or AIO), or that its service call (SC) is being acknowledged by an Acknowledge Service Call (ASC). Only one of the function indicator lines may be true at one time. These lines are driven for SIO, HIO, TIO, TDV, and AIO based on the instruction executed by the computer. The ASC function indicator is generated by the IOP in response to a service call from a device and is not controlled directly by the CPU or by CPU instruction. Generation of the function indicators is also controlled by the internal IOP address selection logic and timing signals from the phase flip-flops and delay lines.

FUNCTION STROBE, FUNCTION STROBE ACKNOWLEDGE, AVI/AVO LINES

When logic power is on, the IOP provides a continuous available input (AVI) signal input to the highest priority DC connected to the IOP. The IOP raises a function indicator line and the function strobe (FS) line in response to a CPU request to perform I/O instructions or in response to a DC service request. The DC's respond to FS by raising either the function strobe acknowledge (FSL) line or the available output (AVO) line at the IOP interface.

The addressed DC answers an FS (accompanied by an SIO, HIO, TIO, or TDV function indicator) by raising the FSL line if the DC is connected. If DC is not connected, the DC raises AVO.

In response to an FS accompanied by an AIO function indicator, the highest priority DC with an interrupt call pending responds by raising the FSL line. If no interrupt call is pending, the AVO line is raised. In response to an FS accompanied by an ASC function indicator, the highest priority DC with a service call pending responds by raising the FSL line. If no service call is pending, the AVO line is raised.

FUNCTION RESPONSE LINES

The multipurpose function response lines (FR0-FR7) are DC controlled. When responding to an FS accompanied by an SIO, HIO, TIO, or TDV function indicator, the DC places status information on the function response lines. The DC places its address on the FR lines when responding to an FS accompanied by an AIO or ASC function indicator. Table 3-2 includes a summary of bit codes used on the function response lines.

DATA/ORDER AND INPUT/OUTPUT REQUEST LINES

The multipurpose data/order (DOR) and input/output request (IOR) lines are DC controlled. When responding to an FS accompanied by an SIO, HIO, TIO, TDV, or AIO function indicator, the DC places condition code data on the DOR and the IOR lines. When responding to an FS accompanied by the ASC function indicator, the DC codes the DOR and the IOR lines to inform the IOP whether an order out/order in or data out/data in operation is to be performed. A summary of bit codes used in conjunction with DOR and IOR is included in table 3-2. The bit code responses (IOR, DOR) to FS accompanied by ASC are shown under Service Cycles in this section.

SERVICE CALL AND HIGH PRIORITY SERVICE LINES

The service call (SC) and the high priority service (HPS) lines are DC controlled. Only the IOP responds to the SC line. Only DC's respond to the HPS line. Device controllers raise the SC line to request order out-order in data out-data in operation by the IOP.

The IOP responds to an SC by raising the ASC function indicator and FS. The subsequent response of a device controller to FS depends on whether or not the particular DC has an SC pending.

A DC which does not have an SC pending raises the AVO line when AVI goes true. The DC takes no action if the AVI line does not go true (indicating that a higher priority DC has an SC pending).

A DC with an SC pending determines the status of the AVI and the HPS lines. The DC raises the FSL line if AVI is true and HPS false (or if the DC is driving HPS). Otherwise, the DC raises the AVO line to the next lower priority DC. If the AVI line does not go true, the DC takes no action in response to FS and ASC.

INTERRUPT CALL AND HIGH PRIORITY INTERRUPT LINES

The interrupt call (IC) and the high priority interrupt (HPI) lines are DC controlled. Only the IOP responds to the IC line. Only DC's respond to the HPI line. DC's raise the IC line to generate an input/output interrupt call to the CPU.

The IOP responds to an IC during execution of an AIO instruction by raising the AIO function indicator and FS. The subsequent response of a device controller to FS depends on whether or not the particular DC has an IC pending.

A DC which does not have an IC pending raises the AVO line when AVI goes true. The DC takes no action if the AVI line does not go true (indicating that a higher priority DC has an IC pending).

A DC with an IC pending determines the status of the AVI and the HPI lines. The DC raises the FSL line if AVI is true and if HPI false (or if the DC is driving HPI). Otherwise, the DC raises the AVO line to the next lower priority DC. If the AVI line does not go true, the DC takes no action in response to FS and AIO.

REQUEST STROBE AND REQUEST STROBE ACKNOWLEDGE LINES

The request strobe (RS) line is DC controlled and the request strobe acknowledge (RSA) line is IOP controlled in response to an RS signal from the DC. These lines operate in a closed-loop mode; that is, upon sensing that the DC has driven the RS line, the IOP delays and then drives the RSA line. Upon sensing that the RS line has dropped, the IOP immediately drops the RSA line. After connecting for service, the DC sends a succession of RS signals to the IOP until the IOP signals RSA and end service.

END DATA AND END SERVICE LINES

The end data (ED) line is driven by either the DC or the IOP. The end service (ES) line is driven by the IOP only. The ED line is

Function	Lines*	0	1	2	3	4	5	6	7	DOR (NCC1)	IOR (NCC2)
SIO, HIO, TIO, TDV	DA	Device controller address									
SIO, HIO, TIO	FR	Interrupt pending	00 = D ready 01 = D not operational 10 = D unavailable 11 = D busy		Device automatic	Device unusual end (last operation)	00 = DC ready 01 = DC not operational 10 = DC unavailable 11 = DC busy		0	Address recognition	SIO: SIO successful HIO: DC was not busy when HIO occurred TIO: SIO can be accepted
TDV	FR	Rate error								Address recognition	Abnormal condition does not exist
AIO	DA		Device end							AIO acknowledged	DC error or fault does not exist
AIO, ASC	FR	Device controller address									
Order in	DA	Trans. error	Incorrect length	Chaining modifier	Channel end	Unusual end				1	0
Terminal order	DA	Interrupt	Count done	Command chain	IOP halt						
Order out (even command word bits 0-7) Control	DA	M	M	M	M	M	M	1	1		
Write		M	M	M	M	M	M	0	1		
Read		M	M	M	M	M	M	1	0		
Read back		M	M	M	M	1	1	0	0	1	1
Sense		M	M	M	M	0	1	0	0		
Stop		1	0	0	0	0	0	0	0		

*DA = data lines; FR = function response lines. Status supplied by the device controller on the function response lines and data lines must remain stable while function strobe acknowledge is true.

Table 3-2. Summary of Bit Codings for Data Exchanges

always driven by the DC with the initial RS of an order out-order in sequence. During a data out-data in sequence, either the DC or the IOP may raise the ED line to signify that no additional data is to be exchanged.

The IOP drives the ES line together with the RSA line to signify that the service sequence is to terminate. If the ES line is held false when the ED line is initially driven, the DC must request a terminal order from the IOP before termination. Otherwise, the DC concludes the sequence with the last data exchange.

DATA PARITY AND PARITY CHECK LINES

The data parity (DAP) line is driven by either the IOP or the DC. The parity check (PC) line is driven only by the DC. The IOP generates an odd parity bit for the data byte on data lines DA0 through DA7 for all data-out exchanges. A device controller (such as a magnetic tape controller) may record this bit.

On data input exchanges, the DC may send the DAP bit to the IOP together with the data byte on lines DA0 through DA7. The DC can also request the IOP to check the odd parity by raising the PC line. (The IOP does not check odd parity if EDX4 and DX4 are true.)

ENABLE EXTENDED INTERFACE AND EXTENDED INTERFACE REQUEST LINES

The enable four-byte (EDX4) and the enable two-byte (EDX2) interface lines are IOP controlled. The four-byte request (DX4) and the two-byte request (DX2) lines are DC controlled.

An IOP that is capable of exchanging data during data in-data out sequences over an extended data path drives the EDX4 or EDX2 line true.

A DC connected to an IOP that is signaling extended data path capability (EDX4 or EDX2) may request extended data path exchanges by raising DX4 or DX2, whichever corresponds to the signaled capability of the IOP.

WORD-ALIGNED DATA REQUIRED LINE

The word-aligned data required (WADR) line is IOP controlled. This line is always false in IOP's with only a one-byte data path. A true signal on the WADR line indicates that each data word on the expanded width data path must correspond to a full word and must be aligned on a word boundary for exchanges between an IOP and memory. The WADR line normally does not generate additional DC functions. In a specialized DC application (such as a data systems design integration), the WADR line could be made available to the program through routing to an unused TDV status bit.

INHIBIT EXTENDED INTERFACE REQUEST

The inhibit extended interface request (IER) line is driven by the IOP with the same timing as ES to signal to the DC that the next I/O service call sequence must be in the one-byte mode.

The DC monitors IER only at ES with the last RSA. If IER is false, the DC may enter an extended mode of operation when again connected for service. If IER is true at ES with the last RSA, the DC is forced to operate in the one-byte data path mode when reconnected for service.

FAST DEVICE CONTROLLER AND ZERO-BYTE COUNT INTERRUPT LINES

The fast device controller (FAST) line is DC controlled, and the zero-byte count interrupt (ZBCI) line is IOP controlled. If a DC drives the FAST line during service sequences, the IOP does not terminate to send ZBCI to the DC during data chaining. However, certain IOP's drive the DC ZBCI line to signify that the DC should request a ZBCI.

I/O RESET AND 1.024-MHz CLOCK LINES

The I/O reset (RST) and the 1.024-MHz clock (CL1) lines are IOP controlled. The RST signal is generally used for initializing a DC. The CL1 line is driven continuously at a 1.024 MHz rate and may be used by DC's as a flip-flop clock.

IOP INTERFACE FUNCTIONS

PRIORITY DETERMINATION

Data Transmission and Priority Cables (See figure 3-2)

Three cables (or five cables for a four-byte interface not shown in figure 3-2) run from the IOP to the first DC. Three or five cables run from the first DC to the second DC. In addition, a priority cable runs from DC to DC with the lowest priority DC connected to the IOP. The physical routing of the priority cables (which determines the priority order of units in the event of simultaneous interrupts or service calls) is independent of the routing of the data transmission cables. The data transmission cables are normally run in minimum lengths in relation to the location of DC's. Although the maximum permissible cable length from the IOP is 100 feet, a twin 100-foot setup can be installed as shown in figure 3-3. The priority cable run is limited to 200 feet and is routed according to the desired response sequence for DC's with simultaneous service calls or interrupt calls. In establishing priority order, the designer should consider the frequency of service requests from each DC, in addition to the ability of the system to recover from a data overrun condition in such devices as card readers or card punches.

Priority Cable Function

When two or more DC's make simultaneous service requests, only one may be connected for service. When the IOP acknowledges the service call, the highest priority requesting DC responds. Lower priority DC's wait for a subsequent service call acknowledgement from the IOP.

When two or more DC's make an interrupt request and when AIO is executed by the CPU and the IOP, only the highest priority DC may respond. Lower priority DC's wait until the CPU executes a subsequent AIO instruction.

If the addressed DC is not connected to the IOP channel during SIO, HIO, TIO and TDV instructions, an AVO priority chain signal is sent to the IOP. The operation is then aborted. The condition is signaled by the IOP on the status response lines to the CPU.

Priority Signals

Four signals are carried on the priority cable:

- HPI High priority interrupt
- HPS High priority service
- AVI Available input
- AVO Available output

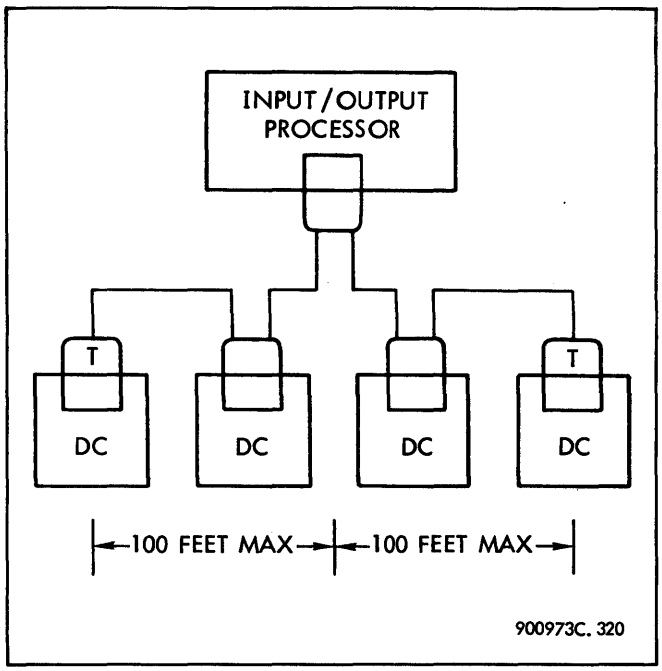

Figure 3-3. Data Transmission Cable Twin Installation

HPI and HPS each constitute a bus which is tapped and is driven by each unit as the other signals on the data transmission cables. Signals AVI and AVO are unique because they are not carried on buses. Signal AVO is an output from each DC sent to the next DC down the line. AVO is a logical function of signal AVI, signals HPI, HPS, no address recognition during SIO, TIO, TDV, or HIO, and the internal state and design specification of the DC. A DC which does not sense its own address during execution of an SIO, TIO, TDV, or HIO instruction passes on signal AVO when it senses AVI.

Signal HPI has the same relationship to IC (interrupt call) that HPS has to SC (service call). A device that uses HPI must also use IC. In responding to signal AIO, any device with HPI set takes precedence over one with only IC set. A DC with only IC set has its interrupt request acknowledged only if no DC's have set HPI, and then only if it is the highest priority DC with IC set.

When one or more DC's initiate a service request, the IOP responds with the function strobe signal to all DC's together with the ASC function indicator. A unit which does not pass on AVO is connected to the IOP for service and may engage in data exchanges. All other units wait their turn.

The same priority chain is used for response to the AIO instruction, except that function indicator AIO is used instead of ASC, and signal HPI is used instead of HPS in the logic. Figure 3-4 shows the logic for a typical unit which is generally included as part of the subcontroller.

STROBE ACKNOWLEDGEMENT

The two strobe signals generated by the I/O system are the request strobe (RS) and the function strobe (FS).

These strobe signals are acknowledged in a closed-loop manner where the strobe signal is applied until an acknowledge signal is received. The acknowledge signal only remains applied until the strobe signal is removed. The I/O data transfer rate is dependent on the rapidity of response to strobe signals. DC's must acknowledge strobe signals with a maximum delay period of 100 ns to permit maximum IOP rates. (Delay in raising strobes or responding to strobes may cause watchdog timer runout in the CPU during I/O instruction execution.)

The IOP receives a response to signal FS (accompanied by a function indicator) either as signal FSL or as signal AVO from the lowest priority DC, but never both. The AVI/AVO and FS/FSL signal flow is shown in figure 3-5.

The DC response according to the function indicator is:

1. ASC or AIO. The highest priority service-calling DC responds to signal FS by raising signal FSL and by inhibiting AVO. If a service-calling device has become non-operational after requesting service and before the IOP response, all DC's respond by sending AVO to the next lower priority DC.

2. SIO, TIO, TDV, HIO. An addressed operational DC responds by raising signal FSL. If not operational, all DC's respond by sending AVO to the next lower priority DC.

DC's respond to the dropping of signal FS by dropping either FSL or AVO. The IOP receives only one response.

During SIO, HIO, AIO and ASC, any clocking required is accomplished at the trailing edge of function strobe FS. During service connection, all signals generated by the IOP are strobed by the DC at the trailing edge of request strobe RS.

INSTRUCTION EXECUTION

SIO, HIO, TIO and TDV Instructions

The primary characteristics of the SIO, HIO, TIO, and TDV instructions follow. (Figure 9-2 is a flow diagram of these instructions.)

1. SIO causes the addressed DC to go to the busy state or the instruction may be rejected for certain reasons.

2. HIO causes an unconditional halt of the DC, the peripheral device, and also resets any waiting interrupts.

3. TIO and TDV differ only in that the status information returned to the CPU during TIO is general and is independent of the particular DC or device, while the status information returned during TDV is specific for each device (defined in the individual specifications for each DC).

SIO, HIO, TIO, and TDV cause the following signal interactions on the IOP bus:

1. One of four function indicator lines is driven according to the particular instruction being executed and a device address is placed on the data lines.

2. The IOP delays 100 ns minimum and signals FS to the DC's.

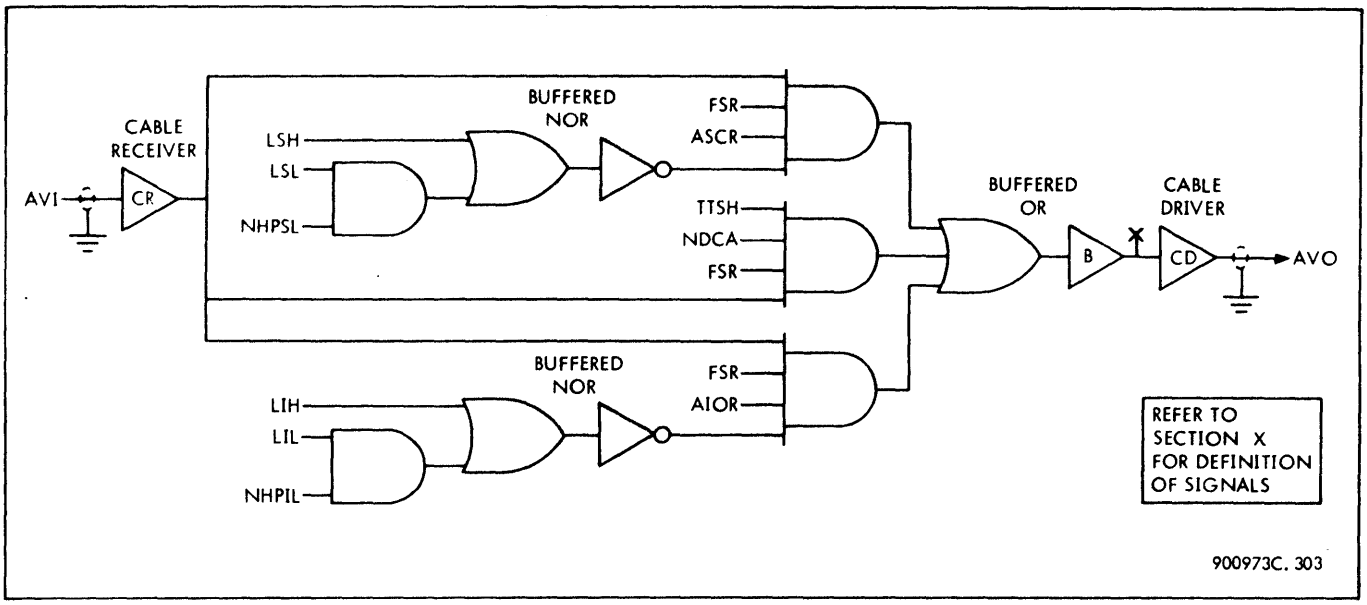

Figure 3-4. Priority Chain, Logic Diagram

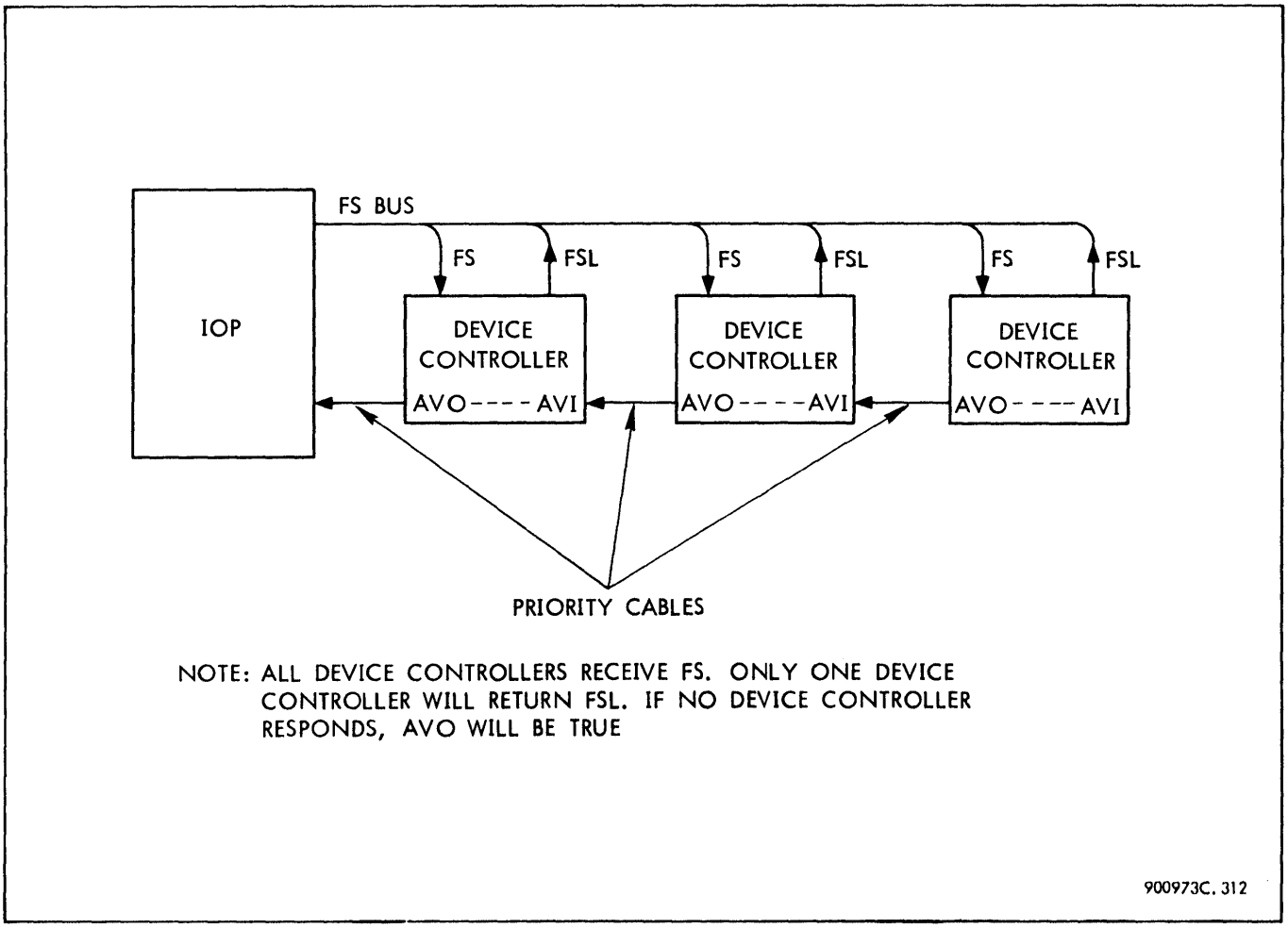

Figure 3-5. Strobe Acknowledge, Interface Diagram

3. All nonaddressed DC's that receive the AVI priority signal must respond by passing on AVO and by remaining off all other lines.

4. The addressed DC must place status information on function response lines FR0 through FR7, on IOR and DOR, and must drive FSL.

5. The IOP responds to the driven FSL by releasing FS.

6. The addressed DC must respond to the released FS by releasing FSL.

Information returned on the FR lines by the addressed DC is defined in table 3-3 for SIO, HIO, and TIO instructions (TDV is unique for each DC).

Table 3-3. SIO, HIO, and TIO Status Response

Function Response Line		Description
FR0		Interrupt pending
FR1, FR2	00	Device ready
	01	Device not operational
	10	Device unavailable
	11	Device busy
FR3		Device auto
FR4		Device unusual end
FR5, FR6	00	Device controller ready
	01	Device controller not operational
	10	Device controller unavailable
	11	Device controller busy
FR7		Not assigned (but always 0)

Notes

1. For single-device DC's when responding to SIO, HIO or TIO, the device and DC status information must be identical (that is, bit 1 and bit 5 must be alike, and bit 2 and bit 6 must be alike)

2. The interrupt pending response to SIO, HIO or TIO (bit 0) should be set only if the addressed device has a device interrupt pending or if a DC interrupt is pending

3. Devices not having AUTO-MANUAL states should report AUTO

AIO Instruction

A DC can activate the interrupt call (IC) line to the IOP except during the interval when another interrupt is being acknowledged by an AIO instruction. The reasons for generating an IC could be internal to the DC, the actuation of a pushbutton on a device, or a command from the IOP (via bit 0 of any terminal order) to generate an interrupt. The status information generally indicates the reason for the IC. The DC is usually unable to report the reason for interrupts initiated by a TO from the IOP but completes the interrupt-reporting sequence regardless.

The CPU uses the AIO instruction to determine which of many possible DC's or peripheral devices has an interrupt request pending. The timing and signal interaction for AIO are identical to SIO, HIO, TIO, and TDV. Figure 9-3 is an AIO flow diagram.

Priority determination and acknowledgement of signal FS are identical to that for other instructions, but information placed on the data and function response lines by the DC is different. During AIO, the highest priority DC must put its own address on function response lines FR0 through FR7 and must also put status information on the data lines. The status information is unique to each device and is thus described in the individual specifications for each device.

The same condition reported for both AIO and TDV in a status response must be reported in the same bit position in the respective response bytes even though signaled on different sets of lines. Rate error (data overrun) if reportable must be in bit position 0 for both AIO and TDV.

Where applicable, bit 7 of the AIO status reponse is reserved for reporting an interrupt generated by bit zero in a stop order. Bit 1 of the AIO status response is reserved for the first device-generated interrupt. The reserved bits (0, 1, and 7) should be assigned to other status responses only as an unavoidable alternative when no other bits are available.

SERVICE CALLS AND ACKNOWLEDGEMENT

An ASC flow diagram is shown in figure 9-4. When the IOP senses that the service call (SC) line is high (denoting service requests by one or more DC's), the following sequence of signal interactions occur on the IOP bus:

1. Function indicator line ASC is driven true (figure 3-6).

2. The IOP delays 100 ns and signals FS to all DC's.

3. The single DC to be serviced (based on examination of the priority determination signals) must put its own address on the FR lines and drive FSL.

4. The IOP responds to the driven FSL by releasing FS.

5. The DC to be serviced responds by releasing FSL.

6. The DC to be serviced may begin issuing request strobes.

The ASC function can then overlap the previous service cycle to some other connected device, thus increasing IOP throughout.

If the DC is driving SC and AVI is true and if HPS is false (or the DC is driving HPS), the DC connects for service.

SERVICE CYCLES

Once legally connected to the IOP for service, a DC may issue request strobe (RS) signals. The lines used in the IOP-DC communication during a service cycle are listed in table 3-4.

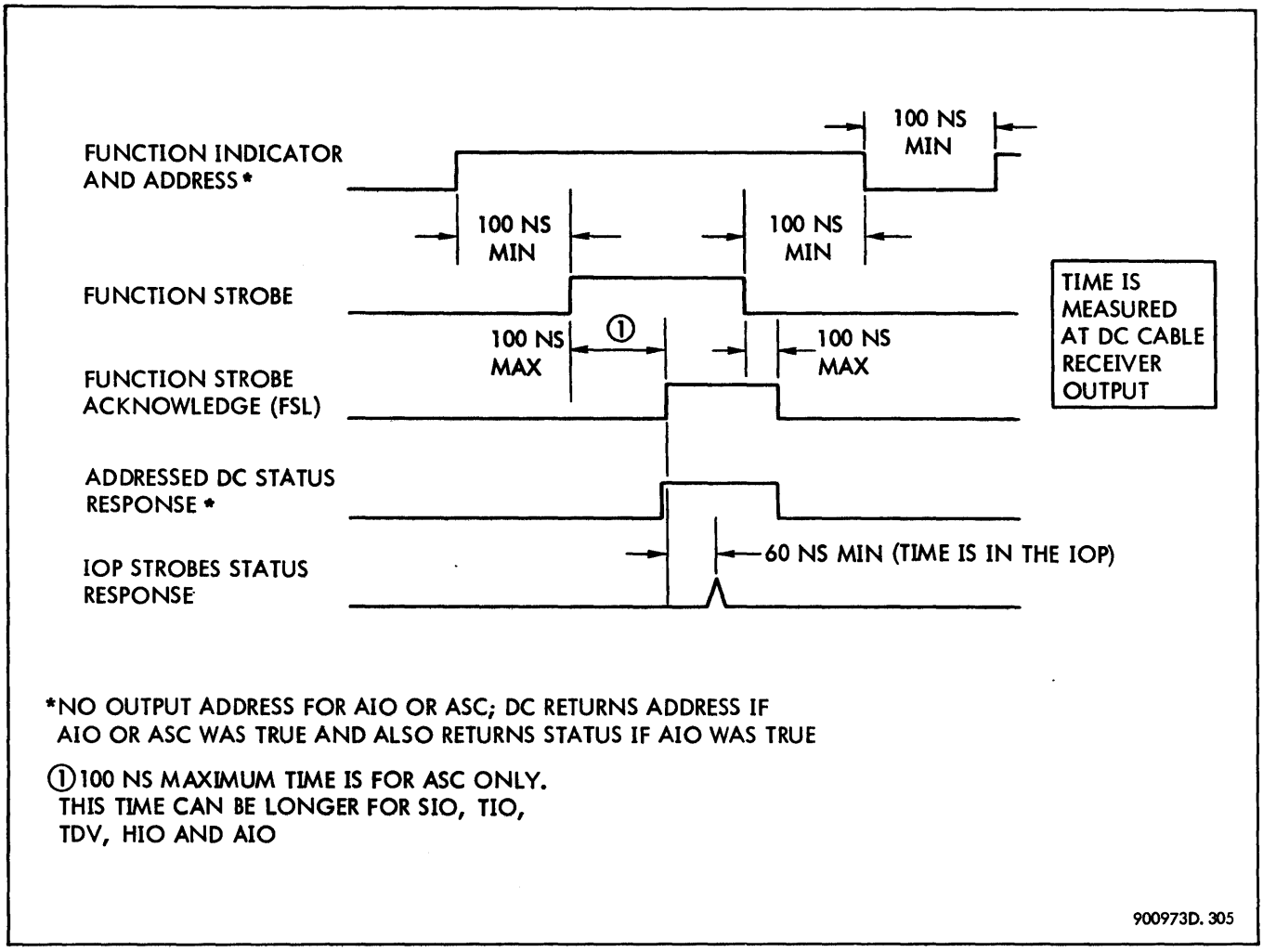

Figure 3-6. Instruction Execution and Service Call Acknowledgement, Timing Diagram

Figure 3-7 shows service cycle timing with a correlation to the ASC timing. The sequence of interaction between the IOP and a DC during a service cycle follows.

1. The DC brings up signal RS and simultaneously controls DOR and IOR to specify the type of information to be exchanged.

DOR	IOR	Service Cycle
0	0	Data input (DIN)
0	1	Data output (DOUT)
1	0	Order input (OIN)
1	1	Order output (OOUT)

2. If an input operation is specified (IOR = 0), the DC concurrently puts data (and perhaps data parity) on the data lines and may drive signal PC if parity checking is needed in the IOP.

3. The IOP responds to signal RS by generating RSA. If an output operation was specified, the output data is first put on the lines (after a 100-ns delay), followed by signal RSA after an additional 100-ns delay.

4. When signal RSA is sensed, the DC must release RS. Output data should be strobed at this point if an output operation was specified.

5. Upon sensing that signal RS has been released, the IOP releases RSA. The DC may then generate another RS (subject to the state of signals ED and ES as described subsequently).

6. Upon generating signal RS, the DC may also drive ED if the current data exchange is to be the last one. The DC can discontinue issuing RS signals only upon sensing that ES is true.

7. The IOP may also drive ED true (with or without ES) to terminate the data exchange portion of the service cycle.

8. Under certain circumstances, the IOP may have to transmit control information to the DC (other than OOUT). This is accomplished by a TO (terminal order). The DC upon sensing that

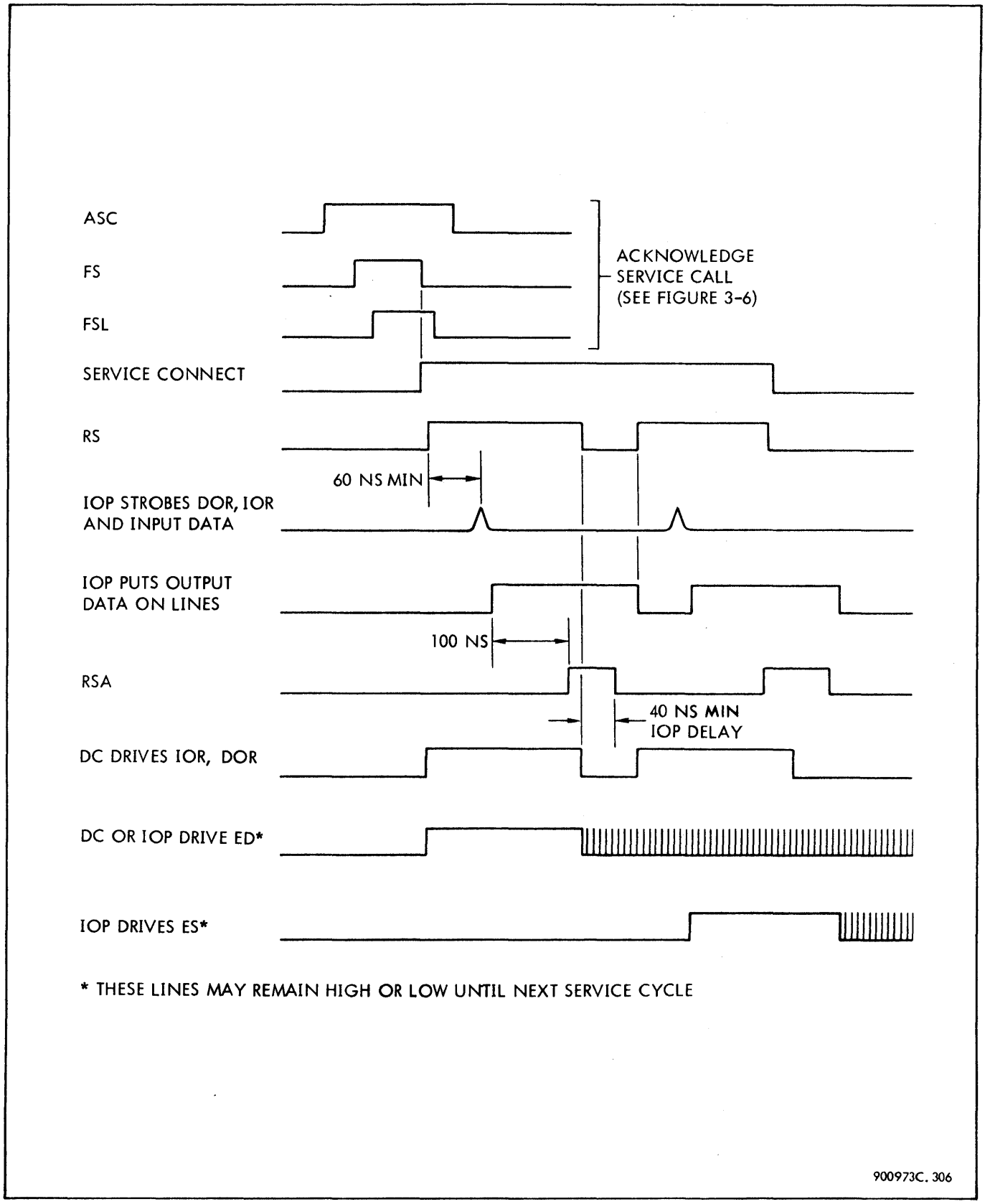

Figure 3-7. Service Cycle, Timing Diagram

Table 3-4. IOP Service Cycle Lines Description

Line	Description	Application
RS	Request strobe	
RSA	Request strobe acknowledgement	
DOR	Data order request	
IOR	Input/output request	
ED	End data	
ES	End service	
DA0 through DA7	Data lines	
DB0 through DD7	Data lines	32-bit data path only
DAP	Data parity	8-bit data path only
PC	Parity check	8-bit data path only
FAST/ZBCI	Fast device controller/zero byte count interrupt	32-bit data path only
EDX2/DX2	Enable 2-byte interface/2-byte interface request	16-bit data path
EDX4/DX4	Enable 4-byte interface/4-byte interface request	32-bit data path only
IER	Inhibit extended interface request	
WADR	Word-aligned data required	32-bit data path only

ED is true and that ES is false must generate one more RS signal to receive the TO.

9. The timing for the additional TO subcycle is identical to all others. The TO data timing resembles OOUT or DOUT. During the TO subcycles, ES is caused to go true by the IOP. Service is always complete after a TO.

Data In Service Cycle

In response to a data in (DIN) service request from the DC, the IOP delays after receiving RS, then strobes the data lines. The IOP delays again and raises the RSA line. Request RS and response RSA continue until ED has been signaled by either the IOP or the DC. Data received by the IOP is transferred to core memory. If ES is false when the DC receives ED from the IOP, the DC raises RS for the TO. If ES is true when the DC receives ED from the IOP, the DC terminates service immediately. The data path is one, two or four bytes wide depending on the state of EDX4/DX4 and EDX2/DX2. During DIN service, the IOP also checks odd parity if the data path is one byte wide. Figure 9-5 is a DIN flow diagram.

Data Out Service Cycle

In response to a data out (DOUT) service request from the DC, the IOP accesses core memory to obtain the data, raises the data lines, delays, and raises RSA. The DC then strobes the data lines and drops RS. This cycle continues until the ED line is raised by either the IOP or the DC. If ES is not raised when ED is raised, the DC raises RS for the TO. If ED and ES are raised together with RSA, the DC terminates service without requesting a TO. The data path is one, two or four bytes wide depending on the state of EDX4/DX4 and EDX2/DX2. During DOUT service, the IOP generates an odd parity bit for the one byte data path. Figure 9-6 is a DOUT flow diagram.

Order Output Service Cycle

Figure 9-7 is an order output flow diagram.

The two reasons a DC may request OOUT are:

1. The device has just gone to the busy state as result of SIO; the first OOUT instructs the DC as to the type of operation to be performed by subsequent service calls.

2. Command chaining is required.

The sequence which allows a DC to ask for OOUT during command chaining is as follows (Sigma 2 and 3 do not perform command chaining):

1. When the last data byte (in or out) is processed, the IOP issues a TO that specifies count done if data chaining is not called for. If data chaining is required, the DC is not informed nor is the DC made aware that the byte count has gone to zero and has then been set to some new nonzero value by means of data chaining.

2. The DC must perform an OIN specifying channel end (CHEND), which is universally required following a TO which specifies count done.

3. If a TO follows OIN, a bit designates whether or not command chaining is to be performed. The CC bit may be present during every TO, but should be inspected by the DC only after the OIN that specifies CHEND. If the command chaining bit is not set, the DC should return to the ready condition, thus requiring another SIO instruction to return to the busy state. If the command chaining bit is set, the DC should request OOUT on the next service cycle and begin another operational sequence.

The significance of the data lines during order out is:

MMMMMM11	Control
MMMMMM01	Write
MMMMMM10	Read
MMMM1 100	Read backward
MMMM0 100	Sense
I 0 0 00 0 00	Stop

where M denotes control bits whose significance is unique to each DC; I denotes that the DC should issue interrupt request if I = 1. Stop code should produce an immediate CHEND

The orders decoded by a DC apply solely to the function of the DC. A DC designed to perform only one duty need not decode any orders at all and functions regardless of the order received.

Order Input Service Cycle

Figure 9-8 is an order input flow diagram. The OIN function is to allow the DC to communicate control information to the IOP. This information is placed on the data lines by the DC concurrent with raising signal RS. The DC should also drive line ED, and the IOP might hold ES low, thus producing the conditions for a TO. The significance of control information placed on the data lines by the DC during OIN is described in table 3-5. A DC enters the OIN service cycle for the following reasons:

1. A TO was received which indicated count done. CHEND is reported.

2. A stop order was received via an OOUT. CHEND is reported.

3. A condition requiring UEND has been detected.

Service Cycle Signal Interaction

In reviewing the signal interaction that takes place during service cycles, the following points should be carefully noted:

1. Either the IOP or the DC may drive ED, thus signaling the last valid byte of data exchange (as opposed to control information). Only the IOP may drive ES, thus terminating service.

2. Signals ED and ES may be interpreted as follows:

ED	ES	Significance
0	0	More data to follow. DC must generate at least one more RS.
1	0	Last data byte. DC must generate one more RS to get the TO.
x	1	Either the last data byte with no TO to follow, or the TO itself. Either completes service.

3. The MIOP is so designed that, at most, four bytes of data may be exchanged in one service cycle, while the SIOP can exchange a record in one service cycle. The MIOP may generate ED after any or every byte, thus allowing only one byte of data to be exchanged per service cycle, but must generate ED at least once every four bytes, thus ending the service cycle.

4. During a service cycle, the DOR and IOR lines are scanned by the IOP only during the first RS of the particular service cycle. All data exchanges during the particular service cycle are of the same type (data or order) and in the same direction (input or output) as the first byte except the TO, which is unique. However, the DC should continue to drive the DOR and IOR lines through the entire service cycle to facilitate testing.

5. The input or output specification is made by the DC, and the IOP responds as requested. In the Sigma 2 and 5 integral IOP and MIOP, where each service cycle is independent, a DC can be designed to alternate input and output service cycles. The IOP then reads or writes in memory as directed, interleaving these operations as required. Each service cycle can be either a read or a write but not both.

6. A DC cannot issue an OIN until it has taken an OOUT after an SIO or following CHEND when command chaining was specified.

7. A DC cannot request more than one OIN for each OOUT taken. The DC must execute the OIN for each OOUT to report CHEND or UEND (unless terminated by an HIO, I/O reset, loss of power, and so forth).

TERMINAL ORDERS

A TO is a data transmission from the IOP to a DC. Figure 9-9 is a TO flow diagram. The TO may conclude certain other data exchanges. A service cycle may not consist solely of a TO, but must first include either DOUT, DIN, OOUT, or OIN.

The DOUT and DIN cycles may consist of one or more bytes. Since both the IOP and the DC control line ED, either may determine the number of bytes exchanged in a service cycle. Although a DC may ask for four bytes in a service cycle, the IOP can abort operations sooner, if necessary, to transmit a TO immediately. The IOP may issue a TO for the following reasons:

1. To request the DC to generate an interrupt request

2. To signal count done to the DC

3. To define command chaining

Table 3-5. Order Input Bit Significance

Bit	Signal	Significance
0	TE	Transmission error detected by the DC
1	IL	Incorrect length. The length of a record was incorrect, usually in regard to a device physical characteristic (for example, other than 120 bytes transmitted to a card punch in binary mode from the IOP)
2*	CM	Chaining modifier. If this bit has been set, the next OOUT execution causes the IOP to skip one command doubleword (two locations) in the IOP program (command list)
3	CHEND	Channel end. Indicates completed transmission and checking of data for the last record. If command chaining is not called for in the TO, the device returns to the ready state following this OIN. If the TO specifies command chaining, the DC must remain busy and subsequently request another OOUT. The DC must accept an SIO (if called for) immediately following OIN if not busy. The DC should delay signaling CHEND until such time as none of the stated conditions would be violated. Following CHEND execution, the I/O channel is open (assuming no command chaining) and can be used by another device on the same channel
4	UEND	Unusual end. Signifies unusual conditions in the DC that require the DC to terminate. UEND is interpreted as a special CHEND. Note however that UEND (unlike CHEND) must be signaled by all DC's via an OIN as part of normal operation. Following the UEND signal, a DC must return immediately to either ready (preferred condition) or not operational (if unavoidable) using the trailing edge of the TO RS as a clock. The DC must then be receptive to an SIO. If IOP halt is signaled in a TO in an OIN cycle, the DC returns to ready without generating or regenerating UEND and without further I/O signals. If the TO calls for an interrupt, the interrupt request must still be issued and the CC bit disregarded. Examples of conditions which would generate a UEND are a device or DC fault (such as data parity error); actuation of the RESET switch on a busy device when the responsible DC is busy with respect to the device; and an order received via an OOUT which is not recognized by the DC. UEND should be reported as quickly as possible – if a delay is required data exchange is not permissible in the interim. For UEND, the state of the CHEND bit is irrelevant but should be set true for consistency
5 6 7		No assigned significance. Should always be set to zero
*Sigma 2 and 3 do not respond to bit 2		

4. To signal IOP halt

5. For internal IOP logic reasons (in this case, data is not generated and the TO is considered a dummy)

The bits in a TO have the following significance:

Bit 0 Interrupt. The DC must respond by generating an interrupt request. No other DC or IOP operations are affected by this bit alone.

Bit 1 Count done. Signaled when required data transmission is complete. The DC must respond to this condition with another service cycle specifying OIN, in which CHEND is signaled.

Bit 2[1,2] Command chain (CC). If the CC bit in IOP fast memory is set, the CC bit may be true in every TO. The DC should inspect this bit only during the TO following the OIN in which CHEND was reported to the IOP. At that time, if this bit is reset, the DC should return to ready and should not issue further service calls until a subsequent SIO instruction is issued. If bit 0 is also true, the DC should issue an interrupt request, wait for acknowledgement and not accept SIO's until an AIO has been issued. If the CC bit is set, command chaining is called for and the DC should request another service cycle. During the service cycle, OOUT should be called for to get the next command (this should be done in parallel with the interrupt request if bit 0 is also set).

Bit 3[2] IOP halt. Signifies that the IOP has detected one of a variety of conditions inhibiting successful completion of the required operations for the channel. The DC must indicate UEND via an OIN without further DOUT or DIN service cycles.

The remaining bits in a TO have no assigned significance.

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[1] Sigma 3 does not signal

[2] Sigma 2 does not signal

INPUT/OUTPUT PROCESSORS

SIGMA 2 INTEGRAL IOP

The Sigma 2 integral IOP uses only the eight-bit data path. Input/output operations are defined and controlled by the CPU through input/output instructions SIO, HIO, TIO, TDV, and AIO, by input/output control word pairs in fast memory, and by input/output tables in core memory. A group of internal read direct instructions can start (SIO), halt (HIO), and test (TIO, TDV) peripheral devices or acknowledge interrupts (AIO) originating from peripherals. For each I/O channel (four basic, 20 maximum) a pair of 16-bit words in fast memory defines the location and the size of an I/O table in core memory and the flags associated with the channel operation. During device service, the CPU is prevented from executing instructions.

SIGMA 3 INTEGRAL IOP

The Sigma 3 integral IOP (IIOP) uses only the eight-bit data path. Input/output operations are defined and controlled by the CPU through input/output instructions SIO, HIO, TIO, TDV, and AIO, by input/output control word pairs in fast memory, and by input/output tables in core memory. A group of internal read direct instructions can start (SIO), halt (HIO), and test (TIO, TDV) peripheral devices or acknowledge interrupts (AIO) originating from peripherals. For each I/O channel (four basic, 12 maximum), a pair of 16-bit words in fast memory define the location and size of an I/O table in core memory and flags associated with the channel operation. During device service, the CPU is prevented from executing instructions.

SIGMA 3 EXTERNAL IOP

The external IOP (EIOP) operates as a multiplexer IOP and is connected only to a Sigma 3 CPU. The EIOP operates on either the eight-bit data path or (optionally) on the 16-bit data path.

Input/output operations are defined and controlled by the CPU through input/output instructions, SIO, HIO, TIO, TDV and AIO (transmitted to the EIOP on the DIO interface), by input/output control words in fast memory, private to the EIOP, and by I/O tables in core memory.

This same group of internal read direct instructions can start (SIO), halt (HIO), and test (TIO, TDV) peripheral devices or acknowledge interrupts (AIO) originating from peripherals.

For each I/O channel (eight basic, 16 maximum), a pair of 16-bit words of EIOP fast memory defines the location and the size of an I/O table in core memory and the flags associated with the channel operations.

SIGMA 2 AND 3 DIFFERENCES

The differences between the IOP interface for Sigma 2 and 3 and other IOP's relate primarily to the method of command chaining and not to the appearance or timing of interface signals. The differences do not affect the external equipment designer. For command chaining in other IOP's, a TO is delivered to the DC specifying count done. The DC replies with an OIN for CHEND. In the TO that follows CHEND, the IOP requests command chaining (if applicable) and the DC either asks for OOUT and the new order or returns to ready, depending on whether the command chaining bit is true in the TO following OIN.

In Sigma 2 and 3 command chaining is never specified to the DC. Since the command chaining bit is false, the DC must return to ready. Another SIO is required to reinitiate operations. Command chaining can be simulated with a sequence of SIO's (the DC returning to ready after each SIO operation).

SIGMA 5 INTEGRAL IOP

The Sigma 5 integral IOP uses only the eight-bit data path. The Sigma 5 integral IOP is similar in performance to the multiplexer IOP that can be connected to either a Sigma 5 or 7. The integral multiplexer IOP shares the registers and the control logic of the CPU and thus communicates with core memory through the CPU memory port. During device service, the CPU is prevented from executing instructions. Upon completion of service to a device, the IOP attends other devices requesting service before returning control to the CPU.

EIGHT-BIT MULTIPLEXER IOP

The eight-bit multiplexer IOP (MIOP) is connected to either Sigma 5 or Sigma 7. This MIOP operates on the eight-bit data path only and may service up to 32 DC's on a time-sharing basis. A maximum of 32 DC's connected to an IOP can be in the busy state simultaneously. Multiple-channel DC's may be serviced on eight of the 32 subchannels.

THIRTY-TWO BIT MULTIPLEXER IOP

The 32-bit MIOP is connected to either Sigma 5 or Sigma 7. This IOP operates on either an eight-bit or 32-bit data path and may service up to 24 DC's on a time-sharing basis. A maximum of 24 DC's connected to an IOP can be in the busy state simultaneously. Multiple channel DC's may be serviced on eight of the 24 subchannels.

SELECTOR IOP

The selector IOP (SIOP) is connected to either a Sigma 5 or 7. The SIOP operates devices on either a one byte or a four byte data path. It is designed to service only one device at a time. Only one DC can be in the busy state at one time.

DEVICE OPERATIONAL STATES AND CONTROLS

STATES AND MODES

The use of uniform controls and nomenclature for all peripheral device states is recommended. A description of the generalized modes and states for all devices and the controls necessary to change them follows.

The two modes in which devices can operate are manual and automatic.

Four states are possible for a device:

1. Ready
2. Busy
3. Not operational
4. Not available

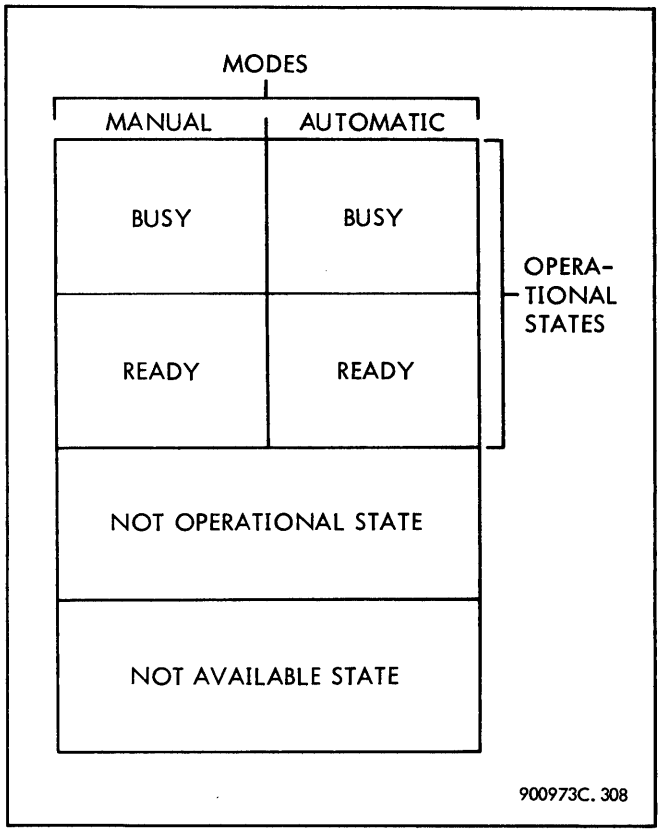


Figure 3-8. Device Mode and State Diagram

The not available state is reserved for devices accessible to more than one controller. The relationship of the modes and states is diagrammed in figure 3-8. Upon receiving an I/O instruction, a device generates a response indicating both mode and state. The four operational substates are:

1. Ready – manual
2. Ready – automatic
3. Busy – manual
4. Busy – automatic

In the not operational and not available states, a manual or automatic mode indication is not pertinent. The not operational state generally exists whenever an interlock is not closed, power is not applied, or device operation is prevented. This would occur if the operator opened the door on a magnetic tape unit or if a card jam occurred on a card reader or punch. The device then returns to the not operational state causing the DC to generate UEND to the IOP. Operator intervention is normally required to clear the not operational state.

Control is generally effected by operator intervention for changeover between modes and by computer intervention for operational state transitions. When the operator has cleared all interlocks, the device becomes operational normally by entering the ready-manual state. Operational transitions are controlled as follows:

1. Ready to Busy. If in the ready state, the unit can accept an SIO instruction and advance to the busy state provided no interrupt is pending. The program tests the device in the ready state and is notified of both the state and the mode. The fact that the device is in the manual mode is no deterrent to becoming busy. While ready, the device accepts the SIO instruction and is subsequently busy.

2. Manual to Automatic. All conditions for running the device must be satisfied before progression from manual to automatic can occur. After these conditions have been met, the operator presses the START switch (if installed) to advance the device from manual to automatic. Transition can be made from either the ready or busy state. Both an SIO instruction and a START switch actuation (in either order) must occur before a device can run.

3. Busy to Ready. In normal operation, the device moves from the busy to the ready state in automatic mode at the end of command chaining or after receiving an HIO instruction. Also, if the operator presses the RESET switch or if an interlock fails, a busy to ready change occurs. When the transition is not initiated by the computer, a UEND signal is generated by the DC for the IOP.

4. Automatic to Manual. The operator can usually shift the device from automatic to manual by actuating the STOP switch. If a condition such as running out of cards in a card reader or a low-paper signal in a line printer occurs during device operation, the device returns to manual. These conditions are not considered unusual or abnormal but require operator intervention. The computer or the program need not be aware of the occurrence of such conditions. When the condition has been corrected, the operator presses the START switch to return the device to the automatic mode. On some devices, the computer can switch the device from the automatic to the manual mode (for example, with a magnetic tape unit rewind in manual order).

Note

The automatic or manual mode status of a device must not be changed by I/O reset (RST) or by an HIO instruction.

CONTROLS AND INDICATORS

Where applicable, the controls and indicators shown in figure 3-9 are used in Sigma series peripheral devices.

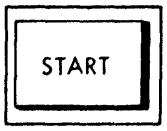
Note

Devices not equipped with START/STOP control switches must remain in the automatic mode and must signal automatic in response to an SIO, HIO, or TIO.

DC READY CONDITION

A DC enters the ready condition under the following circumstances:

1. Power is initially applied.
2. I/O reset signal is received.
3. CPU performs an HIO instruction.
4. After reporting UEND.
5. After reporting CHEND if command chaining is not required.



START Switch. Transfers the device to the automatic mode if all conditions for transfer have been fulfilled. Turns off the MANUAL indicator (if installed) and turns on the AUTOMATIC indicator.

AUTOMATIC Indicator. Lighted by the START switch if all conditions for automatic mode have been fulfilled. Remains lighted while the device is in the automatic mode. Can be the back light for the START switch

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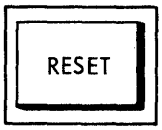

RESET Switch. Used in unusual situations to halt the device immediately. The device must return to the manual mode. If the device is busy, operations discontinue abruptly. The DC generates a UEND signal and requests an OIN to signal the UEND to the IOP. Following the UEND report, the device goes to the manual mode in either the ready or the not-operational state. RESET switch actuation must not reset the UEND status bit, the interrupt-pending status bit, or the AIO status response bits. A special case applies to one of several peripherals under one DC. If RESET is pressed on the peripheral when the DC is either ready or busy with another peripheral, the affected unit should terminate motion and return to ready without notifying the DC or the IOP. If not busy when RESET is actuated, the responsible DC goes to the manual mode

READY Indicator. Should be lighted when the device is in the ready state and should remain lighted for the busy state unless a separate indicator is furnished

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MANUAL Indicator. Lighted when the device is in the manual mode. Can be the back light for the STOP switch

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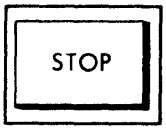

STOP Switch. Returns the device to the manual mode and turns off the AUTOMATIC indicator. If the device is busy, operations must be terminated promptly, without causing errors, loss of data, or change of status (other than automatic to manual mode).
The IOP is not notified except via specific status response to SIO/HIO/TIO. Normal, error-free operation must resume when the START button is pressed. Unit-record devices (such as card equipment, a line printer, or mag tape) must not terminate until the end of the current record. The device must enter the manual mode no later than the time when operations were terminated. If not busy, the DC merely goes to the manual mode

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Figure 3-9. Peripheral Device Controls and Indicators

The HIO instruction performs a function similar to I/O reset except that status bits or registers associated with the device (and not with the I/O system) may remain unaltered if needed subsequently for identification of the prehalt processing point. A DC should enter the ready condition immediately following HIO using FSR HIOR DCA (refer to section X) as a clock. The ready condition ends with an SIO (provided no interrupt is pending).

DEVICE SUBCONTROLLER

SUBCONTROLLER DESCRIPTION

Although each DC contains a device subcontroller, the device subcontroller is available as a separate unit (Model 7900). The device subcontroller consists of a single chassis with module positions 23 through 32 wired to accept the subcontroller modules. The subcontroller can be fixed-position mounted in a standard 5.25 x 19-inch rack or vertically hinged to swing either right or left. The terms device subcontroller and subcontroller are synonymous. The subcontroller is a group of nine modules that serve functions common to all device controllers. Table 3-6 identifies and describes the nine subcontroller modules and lists connector locations. The subcontroller provides the following:

1. All cable drivers and cable receivers required to connect the eight-bit data path interface.

Note

The additional cable driver/receiver modules necessary for the 32-bit data path are not included in the Device Subcontroller Model 7900.

2. Logic to determine priority during ASC and AIO.

3. Eight address selection switches and logic for comparing switch outputs against the device number presented by the IOP during SIO, HIO, TIO, and TDV.

4. Service-connect flip-flop.

5. Relay logic (under remote control) for connecting and disconnecting the subcontroller to the IOP-DC interface during power on-power off.

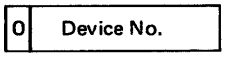
SUBCONTROLLER SIGNALS

When the IOP raises the SIO, HIO, TIO or TDV function indicator, the peripheral device number is also supplied on the data lines. The device number is in the following form:

1. Subcontroller with one device

Data line

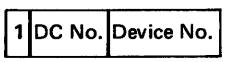
0 1 2 3 4 5 6 7



2. Subcontroller with multiple devices

Data Line

0 1 2 3 4 5 6 7



Interface signals between the subcontroller and the DC are:

SWA0 through SWA7	Switch outputs. Used for manual channel address selection
DCA	Device controller address. True when switch settings SWA0 through SWA7 equal data line receivers DA0R through DA7R (NDCA also provided)
TTSH	Derived from function indicators for SIO, HIO, TIO and TDV TTSH = (SIOR + HIOR + TIOR + TDVR)
TSH	Derived from function indicators for SIO, HIO, and TIO, with DCA true. TSH = (SIOR + HIOR + TIOR) DCA

The subcontroller supplies signal FSL to the line and also supplies gating on function response line buffers for TDV (one set of eight points) and SIO, HIO, and TIO (a second set of eight points). Subcontroller latch circuits receive service and interrupt requests from the DC and pass the requests on to the IOP. The DC signals must be held up until properly acknowledged by the IOP since the subcontroller latch applies only during the acknowledgement. These requests are:

CIL	Interrupt request from DC to subcontroller
CIH	High priority interrupt request from DC to subcontroller (CIL must also be issued when CIH is issued)
CSL	Service request from DC to subcontroller
CSH	High priority service request from DC to subcontroller (CSL must also be issued when CSH is issued)

The subcontroller handles all priority determination internally. Each subcontroller also sets service-connect flip-flop (FSC) at the trailing edge of signal ASC (gated with FS). FSC remains set until ES is sensed. Thus each DC may issue RS only while its FSC is true.

Receiving circuit outputs from the cable receivers are all available to the DC, as are all input driving points to the cable drivers. A signal cannot be fed directly to a cable driver input also fed by a subcontroller signal (a condition which should never arise if the subcontroller is properly utilized). The subcontroller provides the entire power on-power off logic, allowing power to any DC to be removed without affecting the IOP bus adversely. All data lines are inverted for carrying subcontroller outputs. Table 3-7 lists various SDS documents pertaining to the device subcontroller.

INTERFACE CONNECT/DISCONNECT DESCRIPTION

The subcontroller connects and disconnects the DC from the IOP interface without transients when power is applied or removed from the DC. Although the subcontroller provides connect and disconnect sequencing, the controller actually provides the stimulus to start the operation.

Table 3-6. Subcontroller Connector/Cable/Module Relationship

Connector Location	Module Type	Cable Designation	Module Function
23	LT25		Special logic module containing service call latch circuits, data line (received) inverters, a toggle switch (to indicate online or offline) and other subcontroller functions
24	LT26		Special logic module containing eight toggle switches for device controller address selection and two four-bit comparators to compare selected address with IOP output address during SIO, HIO, and TDV instructions
25	Reserved; AT17 takes two slots		
26	AT17	J4	Cable driver-receiver and power on-power off relay to which input and output priority determination cable connects (occupies two module positions)
27	LT24		Special logic module containing function response line buffers with three-way OR gates and other subcontroller functions
28	AT10	J3	Cable receiver to which one cable from IOP connects
29	LT41		Special logic module containing some priority determination logic, service-connect flip-flop (FSC), TSH, and TTSH
30	AT11	J2	Cable driver-receiver to which one cable from IOP connects
31	LT43		Special logic module containing some priority determination logic and various subcontroller functions
32	AT12	J1	Cable driver to which one cable from IOP connects

Table 3-7. Device Subcontroller Model 7900, Reference Documents

Dwg. or Pub. Number	Title
133021	Assembly, Device Subcontroller
133022	Specification, Design
133023	Installation Drawing
127040	Chart, Module Location
127042	Pin List
127043	Equations Logic

Connect Principles of Operation (See figure 3-10.)

When the subcontroller is to be connected to the IOP interface, the ON-OFF switch on the subcontroller must be set to ON and a ground applied to the connect-disconnect circuit. The ground should be applied after all voltages have reached the nominal operating level. When a ground is applied to the connect-disconnect circuit, the following sequence occurs (times are approximate):

1. A set of relay contacts close and signal NINI is grounded 4.5 milliseconds after the ground is applied.

2. Signal INI is allowed to go true 0.5 milliseconds later. A short circuit between lines AVI and AVO is removed at this time.

3. Signal INC goes true and signal NINC is grounded 120 microseconds after INI goes true.

4. When signals INI and INC have reached the true state, the controller is connected to the IOP interface and the service call, the interrupt call, and the cable driver lines become active.

Disconnect Principles of Operation (See figure 3-10.)

The subcontroller is disconnected from the IOP interface when the ON-OFF switch on module LT25 is OFF, or the controller removes the ground from the connect-disconnect circuit. The ON-OFF switch on the subcontroller is connected in series with ground to the connect-disconnect circuit. When the ground to the connect-disconnect circuit is removed, the following sequence occurs (times are approximate):

1. All service and interrupt calls to the IOP are inhibited by grounding signal INC 1.6 milliseconds after the ground is removed. This lets NINC go true through relay and transistor logic.

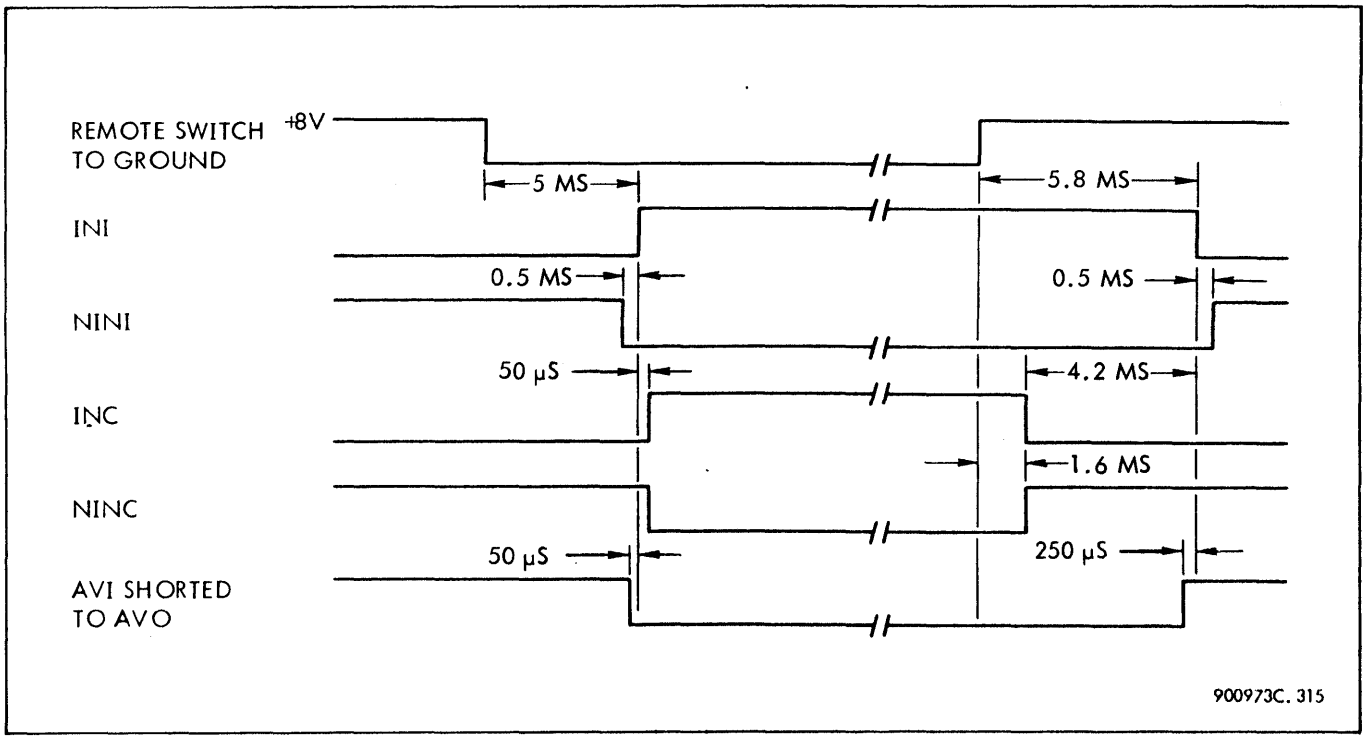


Figure 3-10. Connect-Disconnect, Timing Diagram

2. Signal INI becomes grounded through a set of relay contacts 4.2 milliseconds after signal INC is grounded. Line AVI is also shorted to AVO through a second set of relay contacts at this time. The timing of the two sets of contacts can vary by as much as 250 microseconds.

3. Signal NINI is allowed to go true 0.5 milliseconds after signal INI is grounded.

4. When INI is grounded, the subcontroller is effectively disconnected from the IOP interface because INI grounds all inputs to the subcontroller cable drivers. Line AVI is short-circuited to AVO so that the subcontroller remains connected to the priority cable of the IOP interface without interfering with priority cable operation.

SWITCH COMPARATOR MODULE

The subcontroller includes an LT26 module for comparing the device number with eight toggle switch settings. The eight-switch layout is illustrated in figure 3-11.

POWER REQUIREMENTS

The basic subcontroller requires the following dc power:

+8V at 1.6A

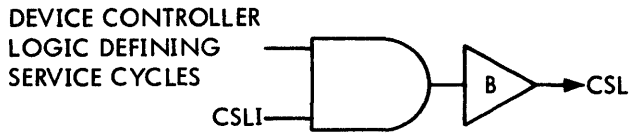
-8V at 0.3A

+4V at 2.0A

DESIGN AIDS

IOP-DC SERVICE CYCLES

The four service cycles are OOUT, OIN, DOUT, AND DIN. Upon entering these cycles, the service call line to the IOP must be raised. The actual raising of the line is controlled by the subcontroller after the DC raises service request signal CSL. Signal CSL is obtained as follows:



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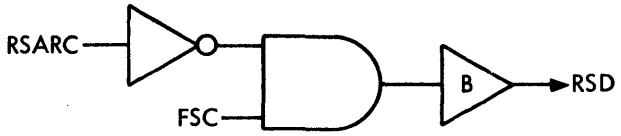
Signal CSLI prohibits DC logic switching transients from appearing on the SC line. The DC waits until the subcontroller service-connect flip-flop FSC goes true, at which time the DC raises request strobe signal RSD. Signal RSD is obtained as follows:



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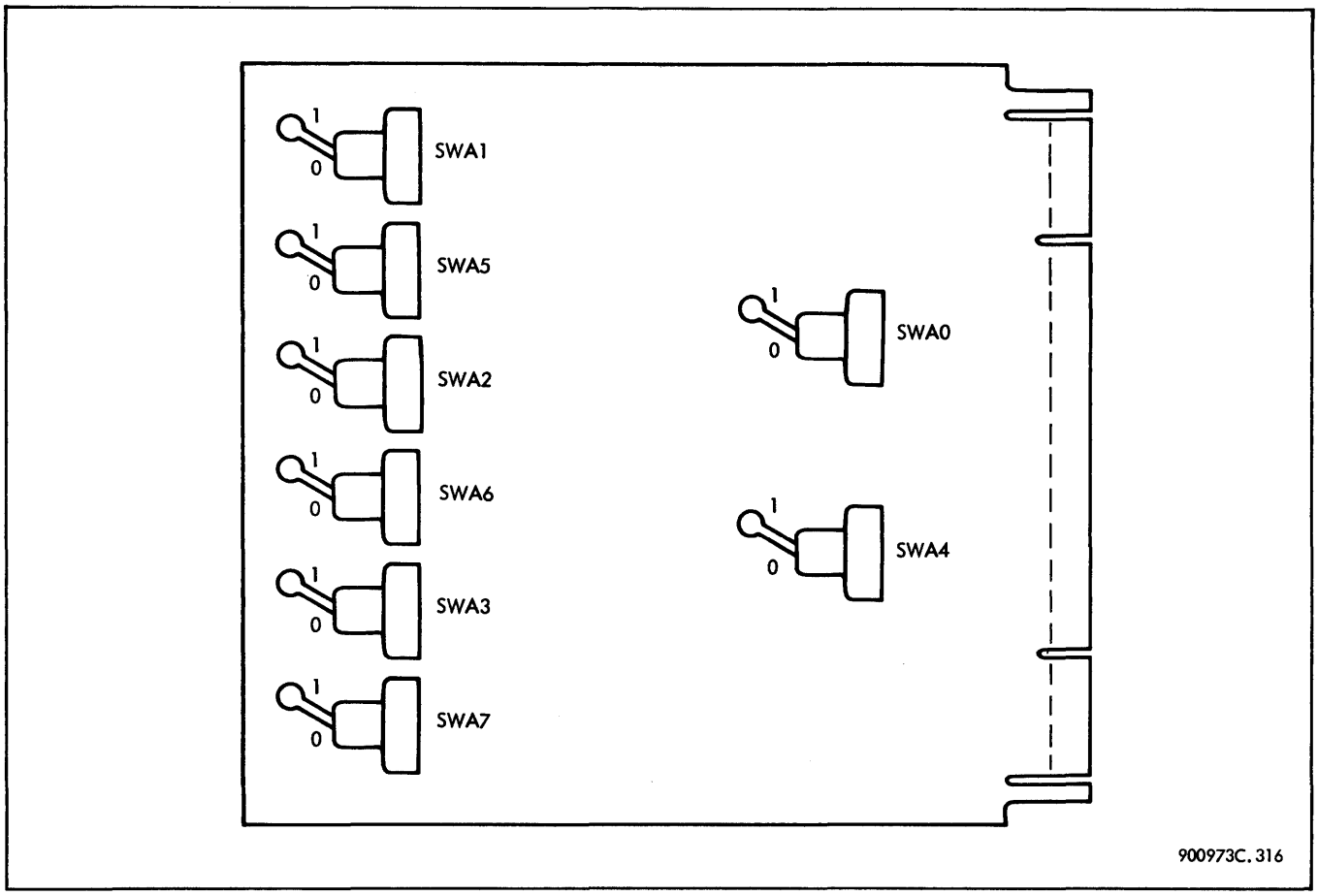


Figure 3-11. Switch Comparator Module

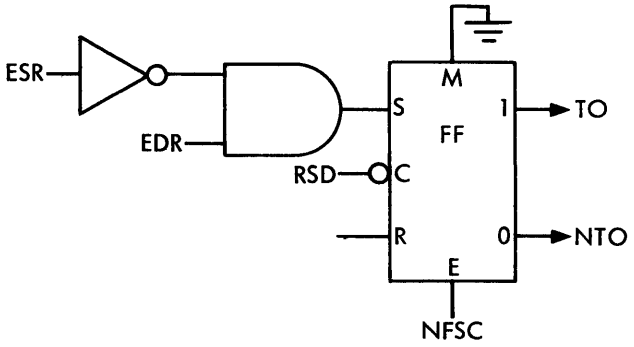
The associated signal lines connected to the IOP interface bus at this time are DA0 through DA7, ED, ES, DOR, and IOR.

Signal RSARC is derived from signal RSAR raised by the IOP. When signal RSARC goes true, signal RSD goes false. The falling edge of signal RSD is used to strobe the applicable interface lines, such as DA0 through DA7, ED, and ES.

When signal RSD goes false, the IOP drops signal RSAR, permitting RSD to go true. This action continues until FSC is reset at the falling edge of RSD when signal ESR is true. The service cycle is now complete.

TERMINAL ORDER

A flip-flop is generally used to mechanize the TO and is clocked by the falling edge of request strobe signal RSD. The set input of the flip-flop is NESR EDR. The logic diagram is shown here by using a standard flip-flop.



At the falling edge of the following request strobe, the TO control logic is based partially on the contents of data lines DA0 through DA7.

CONTINUOUS SERVICE CALL DC

A DC that would make continuous service calls (except when in its

own service cycle) would necessitate assigning that DC the lowest priority in the determination chain; otherwise no other DC could use the IOP simultaneously. Priority cable length limitations might make this operation impractical. Another method of making continuous service calls without dominating the IOP is to inhibit the continuous DC from issuing a service call while any other device has a service call pending. An issued service call should be held up until it has been answered and service has been received.

This method could be used by a DC that needed to communicate with the IOP as often and as rapidly as possible without monopolizing IOP time required by other standard peripheral devices. An example of this application would be a computer-to-computer coupler. This mode of operation would be feasible with an MIOP, and SIOP, but not with the Sigma 2, 3, or 5 integral IOPs since a continuous service call would inhibit the CPU from executing instructions.

SPECIAL CONSIDERATIONS FOR MULTIDEVICE CONTROLLERS

The DC should remain busy as long as the last device remains busy with a channel-dependent operation. Magnetic tape rewind is not channel dependent; the DC should therefore go to the ready condition during rewind (see device end condition description following).

Regardless of whether a DC is busy or ready, I/O instructions addressed to a nonactive device should affect that device only. The DC should be affected only by an I/O instruction addressed to an active device. Only one device can be active for each controller; the active device is defined as the one currently (or last) engaged in a channel-controlled operation.

A DC interrupt in the last transmission should be reset only if an HIO is addressed to the active device. An HIO should affect only the device addressed unless the device is active, in which case the DC should be reset also.

A device end (DE) condition occurs in multidevice controllers during nondata transfer modes. DE occurs typically where a DC-independent operation (such as rewind) can take place after the channel is free without interfering with DC direction of another device. If appropriate, DE can be flagged for interrupt via an order modifier bit. DE is not identified for single-device controllers but is considered coincident with CHEND.

OPTIONAL UEND GENERATORS

The following conditions are optional sources of a UEND signal depending on the requirements of a DC:

1. Detection of an illegal configuration of bits in an order. To minimize the cost factor, however, this irregularity should be mapped into a legal function to avoid triggering UEND.

2. Detection of a data error, data format error, or incorrect length when it would be impractical to permit I/O system control by signaling these irregularities in an OIN.

3. A DC designed to remain on during normal operations (such as a character-oriented communications controller) could generate UEND if count done is signaled.

DC-GENERATED INTERRUPT

A DC creates an interrupt request (CIL) because of:

1. A TO with data line DA0R true

2. A device-generated interrupt

The interrupt request is generated through a flip-flop which once set can be reset only by an HIO or AIO instruction.

Status information supplied by the DC when an interrupt request is acknowledged must indicate the reason for a device-generated interrupt.

A DC directed to generate an interrupt by a TO is not inhibited from making state transitions or from performing other functions except that a busy DC will not accept an SIO with an interrupt pending. The interrupt pending does not inhibit command chaining or the request for and execution of an order out.

SECTION IV

SIGMA 2 16-BIT MEMORY INTERFACE

INTRODUCTION

The Sigma 2 external memory varies in size to a maximum of 64K words (K equals 1024). Each word consists of 16 bits plus parity. Parity is generated and checked by the CPU or the external unit. Modes of memory operation are: read-restore, clear-write, and suspended. Read-restore is used to read from memory. Clear-write is used to write into memory. The suspended mode allows an interval of up to one microsecond to be inserted between the first half of the memory operation (read or clear) and the second half (restore or write). Use of the suspended mode enables a CPU or an external unit to cause the memory to perform a partial-write operation. The Sigma 2 extended memory is made up of one to four memory banks. Each bank consists of External Memory Adapter Model 8054 and Sigma 2 Basic Memory Model 8051. Each bank is functionally independent and provides storage of 4K, 8K, 12K, or 16K words. See figure 4-1 for a block diagram of the Sigma 2 memory system.

MEMORY COMMUNICATION

SIGMA 2 EXTERNAL MEMORY PORTS

Each memory bank in the external memory can include up to two ports, each with identical characteristics. One port is used for connection to the Sigma 2 CPU bus. The other port may be connected to the bus for a special unit requiring direct access to memory or to another Sigma 2 CPU bus. The memory cycle is divided into selection and active intervals. Memory requests are processed on an as-received basis. If memory requests are continuously present on both ports, service alternates between ports.

ADDRESS RANGE AND STARTING ADDRESS SWITCHES

The address range and the starting address are separately switch-selected for each port as listed in table 4-1. The address range can be 4K, 8K, 12K, or 16K. Only ranges equal to or less than the actual memory size should be selected. The starting address must be a multiple of the address range (including zero) for 4K, 8K, and 16K ranges. The starting address for the 12K range must be a multiple of 16K.

DATA SIGNALS

Data signals D00 through D16 require 17 lines and are bidirectional. Data signals are transmitted by the external unit if information is to be written into memory. Data signals are transmitted by memory when information is to be read by the CPU or the external unit. Address signals S00 through S15 require 16 lines and are transmitted only by the external unit.

CONTROL SIGNALS

Essential control signals transmitted by the CPU or the external unit are memory request MQ, data to memory DM, and write-byte signals W0 and W1 (refer to table 4-2). These signals are interpreted by memory as follows: Signal MQ means that the address signals are settled and that a CPU or an external unit is requesting service. Signal DM means that data to be written is on the data lines and is stable. Signals W0 and W1 are interpreted as follows:

W0	W1	Meaning
0	0	Read-restore full word and parity
0	1	Write new right byte and parity and restore old left byte when DM goes true (suspended mode)
1	0	Write new left byte and parity and restore old right byte when DM goes true (suspended mode)
1	1	Write full word and parity

W0 or W1 must be raised simultaneously with memory address. The byte which is to be written in a partial-write operation cannot be read.

Essential control signals transmitted by the memory to the CPU or external unit are address release REL and data to source DS. Signal REL informs the CPU or external unit that the memory cycle requested by signal MQ has been initiated and that MQ may be dropped, after which address signals may be changed. Signal DS informs the CPU or external unit that data is being transmitted by memory if the requested operation was read or partial write. The leading edge of signal REL means that signals MQ, W0, and W1 may then be changed for the next request. Signals REL and DS are both pulses. The cable pin assignments for all signals on a memory bus are included in table 4-3. Table 4-4 indicates the location of 16-bit memory interface connectors.

SIGNAL LINES AND TIMING

ADDRESS, DATA, CONTROL SIGNAL SEQUENCE

The sequence of events involving address, data, and essential control signals is as follows:

1. Address and W0-W1 are transmitted by the CPU or the external unit.

2. Signal MQ is transmitted by the CPU or the external unit. If both W0 and W1 are true, signal DM should be transmitted now and data put on the data bus.

3. Address release REL is transmitted by memory.

4. Signal MQ is removed by the CPU or the external unit.

5. Address and W0-W1 may be changed by the CPU or the external unit.

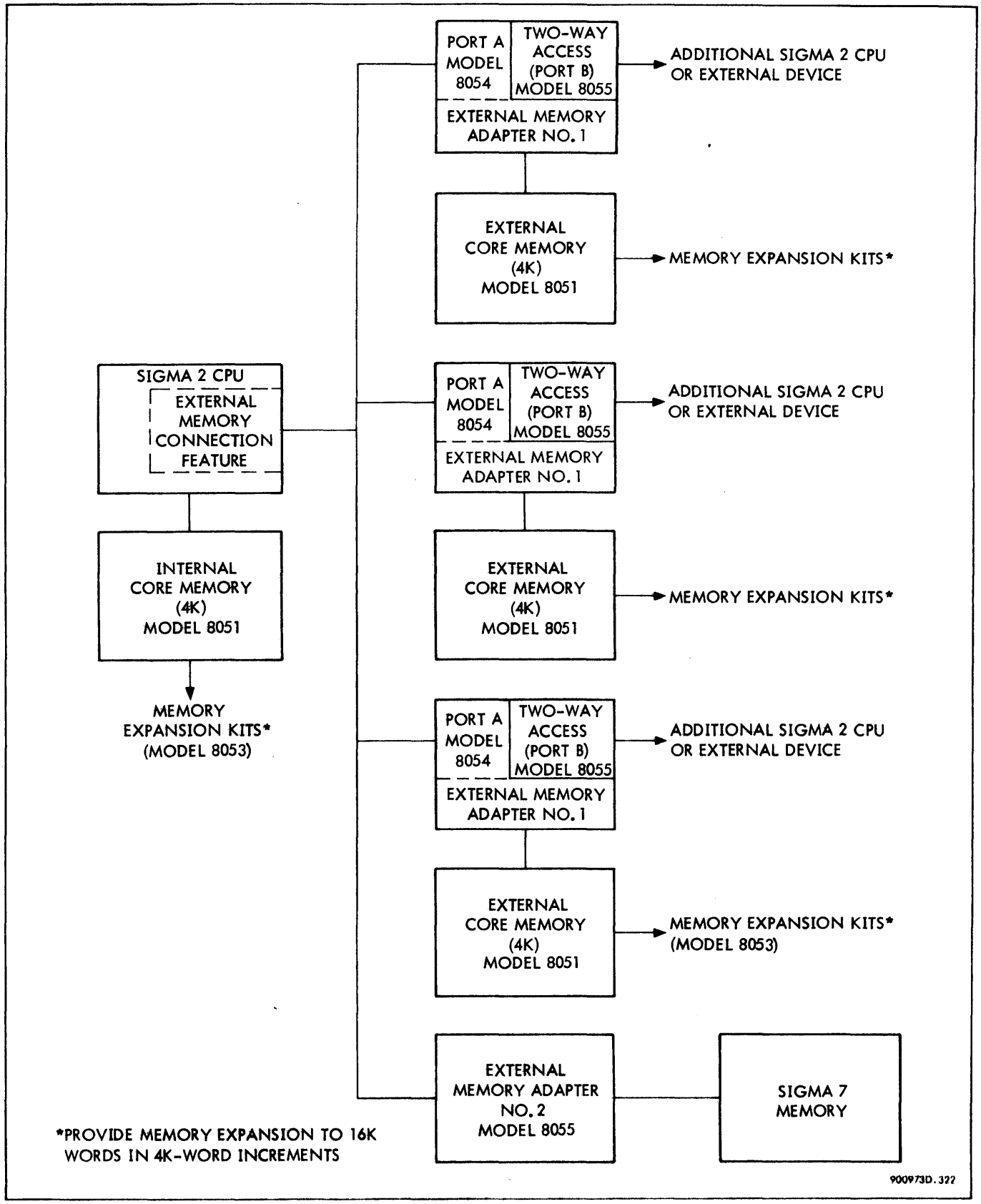


Figure 4-1. Sigma 2 Memory System, Block Diagram

Table 4-1. Sigma 2 External Memory Switch Settings

STARTING ADDRESS SWITCHES				
Port	Switch			
A	1	2	3	4
B	8	9	10	11
Address bit	0	1	2	3
Bit weight	32K	16K	8K	4K

ADDRESS RANGE SWITCHES			
Port	Switch		
A	5	6	7
B	12	13	14
Address range			
4K	0	0	0
8K	0	1	0
12K	1	1	1
16K	1	1	0

Notes

All switches are on ST14 module in location 20A

If port B is missing, set all port B switches to 0

Table 4-2. Interface Signals for 16-Bit Memory

Signal	Description	No. of Lines	Direction	Notes
AH	Address here	1	From memory	Memory recognizes address
D00-D15	Data bits 00-15	16	From/to memory	
D16	Data parity bit	1	From/to memory	Odd parity
DM	Data to memory	1	To memory	Data to memory stable; proceed with partial write cycle
DS	Data to source	1	From memory	Data from memory stable
MQ	Memory request	1	To memory	Address, W0-W1 stable; start memory cycle
REL	Release	1	From memory	Requested memory cycle has started
RES	Reset	1	To memory	Resets memory timing and control logic
S00-S15	Address bits 00-15	16	To memory	
W0	Write byte 0	1	To memory	Left byte; bits 00-07
W1	Write byte 1	1	To memory	Right byte; bits 08-15

Table 4-3. Cable and Connector Pin Assignment for Sigma 2 Port Cables

CABLE CONNECTOR PIN	BACKPANEL CONNECTOR PIN		SIGNAL NAME		
	Cable Driver Input	Cable Receiver Output	Cable 1 AT12 Module	Cable 2 AT11Module	Cable 3 AT11 Module
1, A	2	6	S02D	D00 D D00 R	D14 D D14 R
2, B	1	4	S03D	D01 D D01 R	D15 D D15 R
3, C	9	10	S04D	D02 D D02 R	D16 D D16 R
4, D	3	8	S05D	D03 D D03 R	* DSR
5, E	12	13	S06D	D04 D D04 R	WOD
6, F	15	18	S07D	D05 D D05 R	WID
7, G	19	20	S08D	D06 D D06 R	* RELR
8, H	23	22	S09D	D07 D D07 R	DMD
9, K	25	27	S10D	D08 D D08 R	MQD
10, L	33	34	S11D	D09 D D09 R	S00 D
11, M	35	36	S12D	D10 D D10 R	S01 D
12, N	37	38	S13D	D11 D D11 R	* AHR
13, P	39	40	S14D	D12 D D12 R	RESD
14, R	45	42	S15D	D13 D D13 R	

*Must be grounded

Table 4-4. Connector Locations for 16-Bit Memory Interface

Unit	Cable 1	Cable 2	Cable 3
Sigma 2 CPU	30B	32B	28B
Sigma 2 external memory adapter (Model 8054)			
Port A	7A	5A	3A
Port B*	14A	12A	10A
Sigma 2 external memory adapter 32-bit (Model 8050)	11A	15A	13A

*Cables connecting port B to the CPU, external device, or port A of another memory must be attached to the cable driver/receiver modules of port B upside down (cable leading upward)

6. If either W0-W1 were false during MQ, data and signal DS are transmitted by memory.

7. If both W0 and W1 were false, the operation is complete. If one was true and one was false, parity on the entire word should be computed by the external unit, data and parity put on the bus, and signal DM raised within one microsecond to complete the suspended memory cycle.

TIMING

All times are defined at the cable receiver outputs or cable driver inputs in the Memory Adapter Model 8054. For data on cable timing, refer to section VIII. Figure 4-2 is a Sigma 2 external memory timing diagram.

Signal AH follows address signals S00-S03 continuously with a delay of 70 ns maximum signal. AH indicates that the current address falls within the range of this memory bank. Address signals S00-S15 and byte-write signals W0 and W1 must be stable for 40 ns minimum before MQ is raised and must remain stable while MQ is high.

If the memory is ready to respond to MQ, memory cycle timing starts 65 to 120 ns after the rise of MQ. All subsequent timing is shown in figure 4-2 in reference to this time designated t_0. REL indicates that the cycle has started for this request. REL occurs 10 to 45 ns after t_0 and is a pulse of 80 ns width minimum. MQ must stay high for a minimum of 145 ns after t_0 and must be dropped 600 ns maximum after t_0 to preclude recycling for the same request. Byte data not to be written in this cycle rises between 280 to 410 ns and falls between 540 to 625 ns after t_0.

Signal DS indicates that data from memory is stable. DS occurs 350 to 385 ns after t_0 and is a pulse of 80 ns width minimum.

Signal DM controls (with W0 and W1) gating of data into the memory data register and, in the event of a partial (byte) write cycle, controls continuation of the memory cycle out of the suspended state.

In the simplest case, if the byte-write function is not used DM may be high continuously. Data to memory must then be stable 75 ns maximum and must remain stable until 480 ns minimum after t_0. If DM is not high continuously, data must be stable while DM is high, except for an early DM, where data must be stable only by 75 ns maximum after t_0.

For a full write cycle (W0 and W1 true) DM must not drop before 170 ns and must rise no later than 310 ns after t_0. DM must be 80 ns wide minimum. For a byte-write cycle (either W0 or W1 true, but not both) DM must not drop before 475 ns and must rise no later than 1300 ns after t_0. Normally DM would occur after DS, delayed sufficiently to generate a new parity bit for the word consisting of the byte that is to be preserved and the new byte to be written.

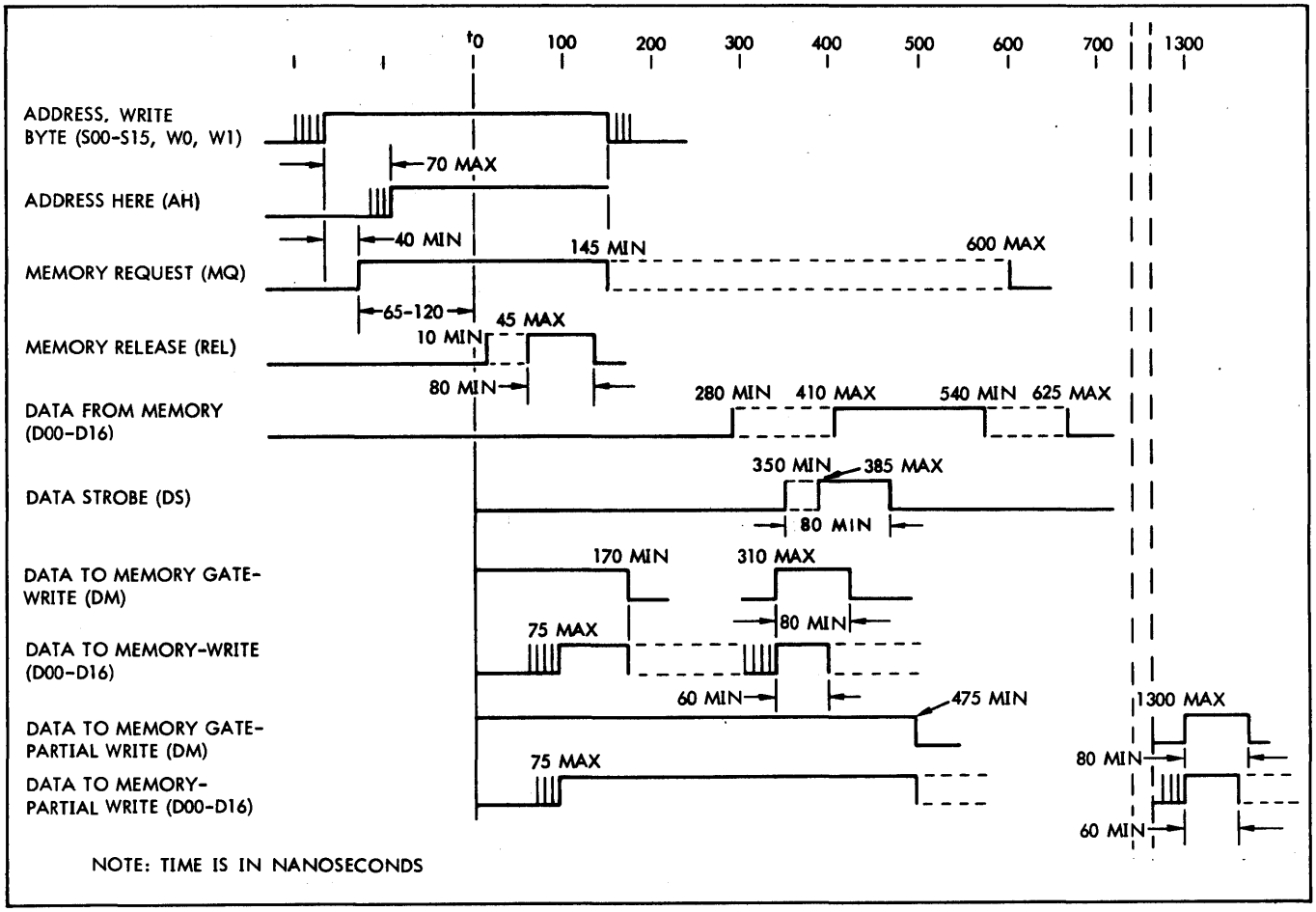


Figure 4-2. Sigma 2 External Memory, Timing Diagram

SECTION V

SIGMA 3 16-BIT MEMORY INTERFACE

INTRODUCTION

A Sigma 3 memory system ranges in size from 8K to 64K words (K equals 1024) and has from one to four memory ports which are direct access paths to memory. Either the amount of memory or the number of ports may be expanded independently. The basic Model 8101 comes with 8K of memory and one port. The basic Model 8102 comes with 8K of memory and two ports (one for the CPU and one for the external IOP). The assembly which interconnects memory and port users is the memory port multiple (MPM). Figure 5-1 shows a block diagram of a large Sigma 3 memory system. For clarity, only one set of port connections are shown. All ports and bank drives of the MPM's are independent so that for any one MPM, two memory accesses may occur simultaneously. For example, port 2 may be accessing a location in bank A at the same time that port 3 is accessing a location in bank B. When two MPM's are considered, it is possible for four separate memory accesses to be taking place simultaneously if all four ports are in use. However, there is no interleave or overlap capability through a single port.

The Sigma 3 memory port interface is not compatible with the Sigma 2 memory port interface. The Sigma 3 memory system is a clocked, synchronous system that requires the port user to use clock signals from the CPU in order to generate properly certain key control signals.

The bank A drive of an MPM may be replaced with the External Memory Adaptor Model 8150. The external memory adaptor allows a Sigma 3 memory system to communicate directly with a Sigma 5 or 7 memory.

MEMORY COMMUNICATION

CLOCKING

The Sigma 3 system is a clocked, synchronous system in which a 975 ns memory cycle is divided into three 325 ns clock periods. The 325 ns clock period is further subdivided by two phase clock signals CLA and CLB (see figure 5-2). The vertical reference line marked t_0 in figure 5-2 represents the start of the memory cycle. The start of the cycle is actually timed with the rising edge of CLB, but the rest of the cycle proceeds asynchronously after the start of the cycle. Therefore, all times must be referenced to a memory cycle time (t_0).

The memory request signal (MQ) must be so timed to overlap cleanly CLB as shown in figure 5-2. This requires that the port user make use of clock signals provided by the Sigma 3 CPU when generating MQ. The method of bringing CLA and CLB to the backwiring board of a port user is for the port user to install an AT59 module in his equipment. This module is interconnected to the clock oscillator in the Sigma 3 CPU by a special, dual-coax, 15-foot cable which minimizes clock skew throughout the system.

The use of this module to generate many of the required signals is covered in Design Aids in this section. The port user is not permitted to connect to the Sigma 3 clock system in any other manner.

PORT CABLING

The cable interface between a port user and a single MPM consists of two ribbon cables whose data formats are given in tables 5-1 and 5-2. If the memory system requires more than one MPM (which usually implies more than 32K of memory), the port user must have a second set of two ribbon cables for the second MPM. In addition, the drive requirements of signals going from the port user to the MPM's are doubled. (Refer to table 5-3.)

All signals coming from the MPM to the port user can drive 14 unit loads. However, all of these signals must be terminated with a 220-ohm resistor to +4V whether or not they are used.

Several different cable lengths are available. Maximum cable length is 140 inches (Xerox Assembly No. 137482-143). When using standard Xerox frames and cabinets, part of the cable length is required for the swinging of frames and the routing to the cable brackets. The practical effect of this is that if the port user uses the 140-inch cables and positions the port ribbon cables in the top chassis of a swing frame, the cables can be expected to reach an MPM in the adjacent cabinet and the cabinet next to the adjacent cabinet but no further.

Any pins not assigned a signal name in tables 5-1 and 5-2 must be left unused. They may not be used as if they were blank pins.

ADDRESSING

An MPM contains a set of starting address switches for each port with respect to each bank. (See table 5-4.) The address range of Sigma 3 is 0-64K. The starting address switches are coded in increments of 8K. This means that a memory system may be composed of four banks of 8K each, four banks of 16K each, or any combination with the restriction that the starting address of any 16K bank of memory must be on a 16K address boundary. The total address field must start at zero and must have no gaps in the address field.

PARITY

The Sigma 3 memory system uses odd parity. When writing into memory, the parity bit must be generated by the port user and sent along with the write data as if it were a 17th data bit. The memory contains 17 cores for each word of data in order to store the 16 bits of data plus the parity bit. When reading from memory, the parity bit is read out as if it were a 17th data bit. The check for odd parity must be performed by the port user during read operations.

Table 5-1. Format of Memory Port Cable No. 1

PIN NO.	SIGNAL	DESCRIPTION	PIN NO.	SIGNAL	DESCRIPTION
01	MR01	Read data	25	GROUND	(At memory end of cable)
02	MR02	↓	26	NL00	ADDRESS
03	MR03		27	NL01	↓
04	MR04		28	NL02	
05	MR05		29	L00	
06	MR06		30	L01	
07	MR07		31	L02	
08	MR08		33	L03	
09	MR09		34	L04	
10	MR10		35	L05	
11	MR11		36	L06	
12	MR12		37	L07	
13	MR13		38	L08	
14	MR14		39	L09	
15	MR15		40	L10	
17	MR00		41	L11	
18	MR16	Read Parity	42	L12	
19			43	L13	
20			44	L14	
21	MQ	Memory Request	45	L15	
22	NMAH	Not Address Here	46	NL06	
23	MRR	Result Release	47	NL07	
24	NMRR	Not Result Release	50	NL09	

Table 5-2. Format of Memory Port Cable No. 2

PIN NO.	SIGNAL	DESCRIPTION	PIN NO.	SIGNAL	DESCRIPTION
01	MW01	Write Data	25		These pins are not used
02	MW02	↓	26		↓
03	MW03		27		
04	MW04		28		
05	MW05		29		
06	MW06		30		
07	MW07		31		
08	MW08		33		
09	MW09		34		
10	MW10		35		
11	MW11		36		
12	MW12		37		
13	MW13		38		
14	MW14		39		
15	MW15		40		
17	MW00		41		
18	NMW16	Write Parity	42		
19			43		
20	RST	Reset	44		
21	RSTE	Reset Early	45		
22	GROUND*		46		
23			47		
24	MREAD	Read Operation	50		

*Must be wired to ground at the port user's end of the port ribbon cable

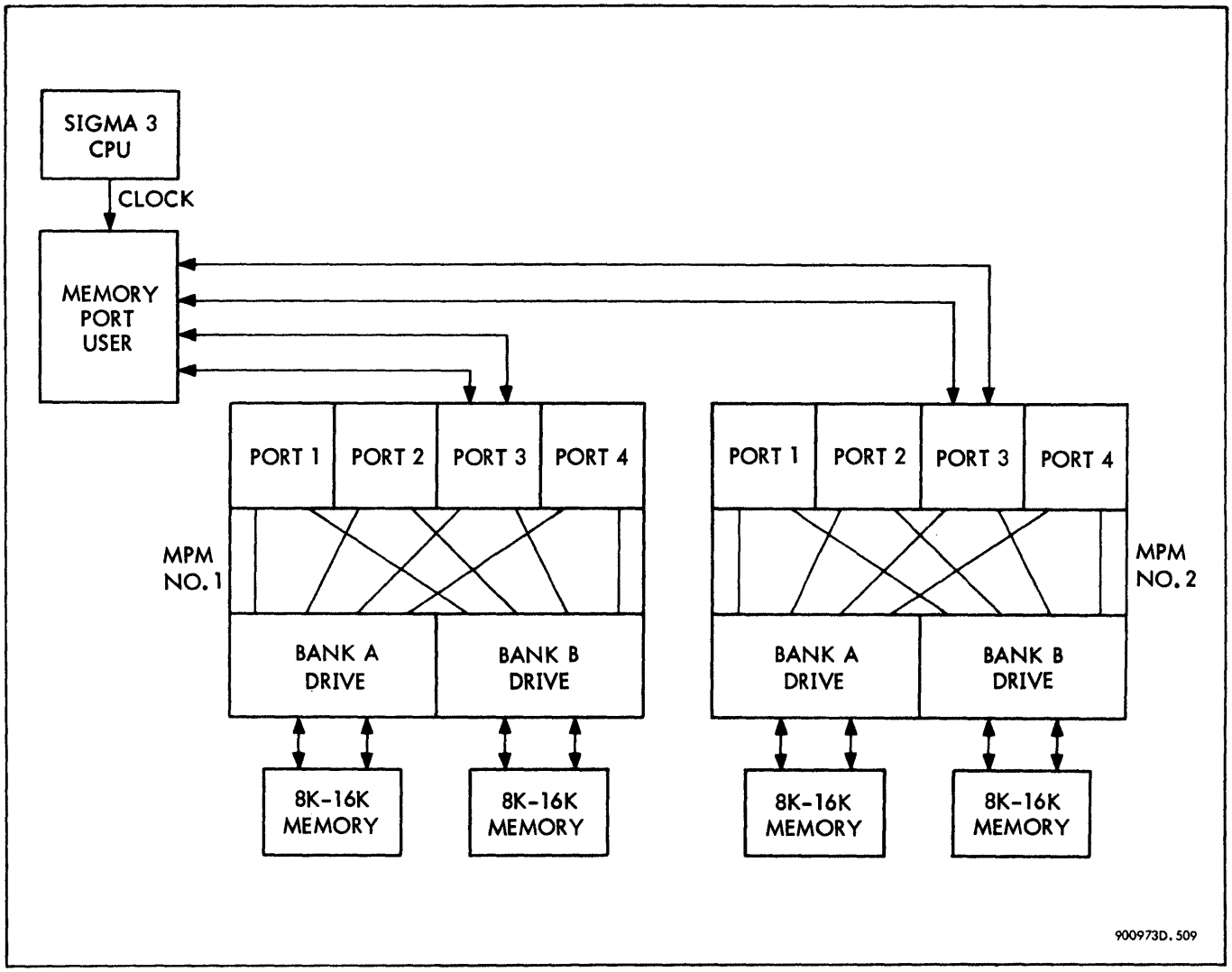


Figure 5-1. Sigma 3 Memory Configuration (Large), Block Diagram

Table 5-3. Drive Requirements for Signals to an MPM

Signal	Unit Loads		Signal	Unit Loads
MREAD	12		L00	8
MQ	7		L01	8
MW00-MW15	6		L02	9
NMW16	9		L03-L05	7
NL00	11		L06	8
NL01	11		L07	8
NL02	11		L08	7
NL06	6		L09	8
NL07	6		L10-L15	7
NL09	6			

Notes

1. One unit load equals 3.7 MA
2. These are drive requirements to a single MPM. If two MPM's are used, twice the amount of drive is required

Table 5-4. MPM Switch Settings

PRIORITY SWITCHES*

Bank	Switch	Switch Module Location
A	2	08C
B	14	08C

PORT DISABLE SWITCHES†

Port	Switch	Switch Module Location
1	15	08C
2	1	08C
3	2	02C
4	15	02C

STARTING ADDRESS SWITCHES

MPM Bank	Port	Starting Address 0	Starting Address 1	Starting Address 2	Switch Module Location
A	1	5	4	3	08C
	2	9	8	6	08C
	3	5	4	3	02C
	4	9	8	6	02C
B	1	5	4	3	04C
	2	9	8	6	04C
	3	2	1	11	04C
	4	15	14	12	04C
Bit Weight		32K	16K	8K	

*Down means all old requests serviced before new requests admitted

†Down means enable

There is no provision for a direct partial write. For example, if it is desired to modify only one of the two bytes of a word, the whole word must read out, read parity must be checked by the port user, the desired byte must be modified, write parity must be regenerated for the whole word by the port user, and the whole word is then rewritten into memory. Thus, two complete memory cycles (a read and a write operation) are required to modify the byte.

PORT PRIORITY

The MPM has two modes of priority determination between ports. The mode is selected by a toggle switch. When in the normal mode, if two or more memory requests are received at the same time, the higher priority is processed first but all of those requests are processed before any new requests are processed. This prevents high data rate devices from locking out other devices.

The other mode of priority determination between ports is the straight priority scheme where the higher priority port may use every memory access to the exclusion of the other ports. Refer to table 5-4 for switch settings.

PORT DISABLE

Each MPM contains a toggle switch for each port to disable that port if necessary. When the switch is in the disable position, all memory requests from that port are ignored by that MPM. (See table 5-4 for switch settings.)

SIGNAL DESCRIPTION

TYPICAL READ SEQUENCE

The typical sequence of events during a read operation is as follows:

1. Reset read data register
2. Set to correct values MREAD, L00-L15, NMW16
3. Use the leading edge of CLA to set MQ latch
4. Abort operation if the address here signal is not returned when expected
5. If the address here instruction is returned when expected, wait for MRR. If the MPM is not busy with a request from another port when MQ is received, MRR is returned as shown in figure 5-2. If the MPM is busy, MRR is returned during a later clock period.
6. When MRR is received, reset MQ
7. Delay, then change address
8. Read data into data register
9. Check parity

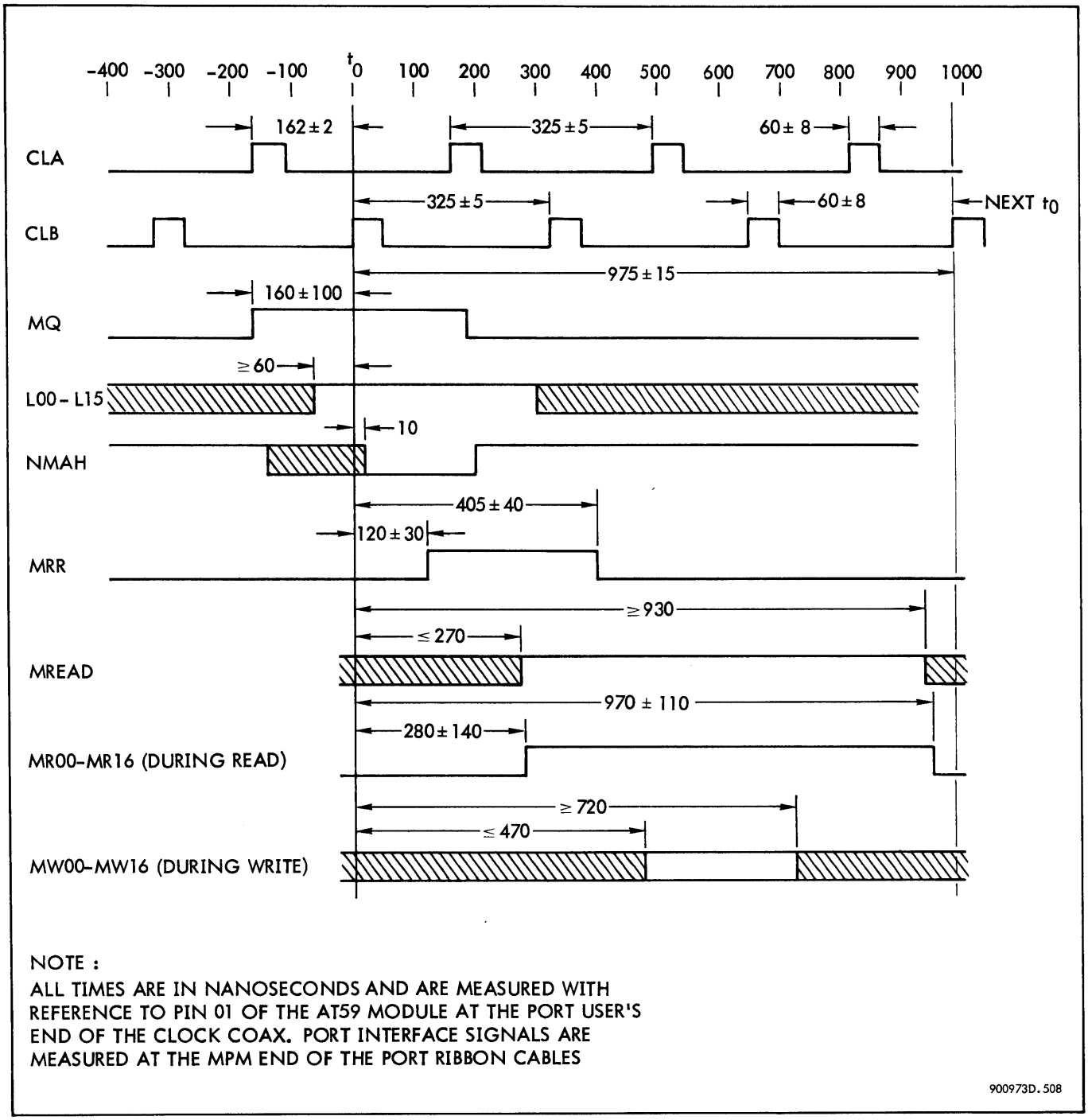


Figure 5-2. Memory Port, Timing Diagram

DETAILED SIGNAL DESCRIPTION

A general timing diagram is shown in figure 5-2. A detailed signal description follows (all times measured at the memory port):

MQ — Memory Request. Memory cycles are initiated by MQ. The timing requirements of the leading edge of MQ are specified in figure 5-2.

Usually, the port user should turn off MQ with MRR. MQ must be turned off within 300 ns after the leading edge of MRR. MQ must stay down for at least 300 ns and must not be turned on again any sooner than 600 ns after the leading edge of the previous MRR.

L00-L15 — Address Signals. The timing of the leading edge of the address signals is shown in figure 5-2. The address must not be changed until 100 ns after the leading edge of MRR.

MW00-MW16 Memory Write Data. Sixteen data bits plus parity. Figure 5-2 shows the timing if MRR is received as shown. If not, MW00-MW16 must be held valid by the port user for the same amount of time after MRR shown in figure 5-2. MW00-MW15 may be allowed to do anything during a read operation. However, NMW16 must be driven true during a read operation during the same time interval defined in Figure 5-2 for MREAD.

MREAD Read. Differentiates between a memory read operation and a memory write operation. See figure 5-2 for timing. If MRR is not received as shown in figure 5-2, MREAD must be held valid by the port user for the amount of time after MRR shown in figure 5-2.

MAH Memory Address Here. This signal is derived from MQ, L00-L02, and the starting address switches and means that an existent memory has been addressed. If the address here signal does not occur after MQ with the timing shown in figure 5-2, nonexistent memory has been addressed and no MRR signal will be forthcoming. The port user should provide logic to escape this condition, which hangs up operations. MAH is gated with MQ; therefore, it cannot come true until after MQ, and it goes false within 70 ns after MQ goes false. Even when MQ is true, MAH is indeterminate anytime that address lines are changing. The timing of the leading edge is shown in figure 5-2. The inverse polarity of the signal is sent out by the MPM.

MRR Memory Request Release. When this signal comes true, the port user should drop MQ and may change the address lines 100 ns later.

The MPM may be busy when MQ is received. MRR is returned only when the memory is able to process that particular request. When MRR is returned, it has the timing relationship to clock shown in figure 5-2. MRR is a pulse whose nominal width is 260 ns. MRR is generated only if there was a previous MAH.

MR00-MR16 Memory Read Data. Sixteen data bits plus parity. The timing of these signals is shown in figure 5-2. These lines are indeterminate during a write operation. This register is reset at the end of each memory cycle.

RST, RSTE The system reset signal (RST) and early system reset (RSTE) are provided for the port user. The rising edges of both RST and RSTE are asynchronous and occur at approximately the same time. The falling edge of RST occurs at least 100 ns after the falling edge of RSTE. These two signals are generated when:

1. The RESET button on the Sigma 3 processor control panel (PCP) is pressed
2. During a power-on sequence
3. During a power-off sequence

EXTERNAL MEMORY ADAPTOR

The function of the bank Model A drive of an MPM may be changed from driving 16K of core to providing an External Memory Adaptor Model 8150 interface. This adaptor allows a Sigma 3 memory system to be partly composed of Sigma 5 and 7 memory which is accomplished by plugging in optional modules. The two Model 8150 cables are inserted in the positions where the memory cables normally go.

The timing on the memory port interface is affected when Sigma 5 and 7 memory is accessed through an external memory adaptor. The following signals are affected:

MR16 Read Parity Bit. Instead of having the timing relationship shown in figure 5-2, MR16 may come true as late as 600 ns after the leading edge of MRR.

MAH Memory Address Here. The MAH response comes true with the timing shown in Figure 5-2, but its meaning is altered. MAH means that the present memory address is equal to or greater than the switch setting in the MPM. This requires that memory starting addresses always be chosen so that the Model 8150 is the highest address bank of memory. If, after having passed the initial MAH address criteria, it is discovered that the address truly does not exist in Sigma 5 and 7 memory, the indication seen by the port user is read data of all zeros. This pattern should be recognized by the port user as a parity error.

MRR Request Release. MRR is delayed from three to five clock periods for a read operation and two clock periods for a write operation. (In the absence of memory interference in the Sigma 5 and 7 memory.)

DESIGN AIDS

GENERAL

In order to meet the timing requirements shown in figure 5-2, the port user must use clock signals from the Sigma 3 CPU. The port user is therefore required to make use of a Xerox AT59 module and a special coax cable (Assembly No. 152035-152) which interconnects the AT59 module with the clock oscillator in the Sigma 3 CPU.

MODULE AT59

The AT59 Clock Receiver/Driver module receives two clock signals from the Sigma 3 CPU and generates two-phase clocks with a large amount of drive capability. The actual signals on the cable are 6MHZ and 3MHZ signals, and the two-phase 3MHZ clock is derived from these signals through the use of enabling flip-flop CLAEN. (See figures 5-3 and 5-4 and table 5-5.)

MECHANIZATION EXAMPLE

Figure 5-5 shows an example of how the AT59 module may be used to synchronize the MQ signal with the Sigma 3 clock. There are

many ways that the interface logic can be mechanized. However, in general, it is found more practical if the entire logic unit which interfaces the Sigma 3 memory port is clocked from the AT59 module.

The oscillator in the Sigma 3 CPU may be switched to an adjustable mode for clock period margining. A typical test would be to reduce the clock period by 5 percent. A port user's design should allow for this procedure to avoid damage to his equipment.

Table 5-5. AT59 Module Signal Characteristics

PIN	SIGNAL CHARACTERISTICS
01, 45, 46	These pins may drive one additional unit load. Wire length must be $\leqslant$ 4 inches
02	Port user not permitted to wire to this pin
23	May drive 12 additional unit loads
27	May drive 8 additional unit loads
34, 31	May drive 46 unit loads
08, 09, 10, 11, 12	Total load on all five pins may be 82 unit loads
03, 04, 06, 07	Total load on all four pins may be 82 unit loads (The delay through this circuit is the same as the circuit with outputs on 08, 09, 10, 11, 12)
39	May drive 12 additional unit loads. Maximum delay from inputs is 25 ns
37, 40, 42	May drive 14 additional unit loads. Maximum delay from inputs is 25 ns.
00, 05, 16, 24, 32, 41, 48	Grounds. Must be hardwired together by port user
50	-8V. Must be hardwired to -8V by port user
25, 26, 29, 30, 33	Terminating resistors. Five unit loads each. All input pins require one unit load

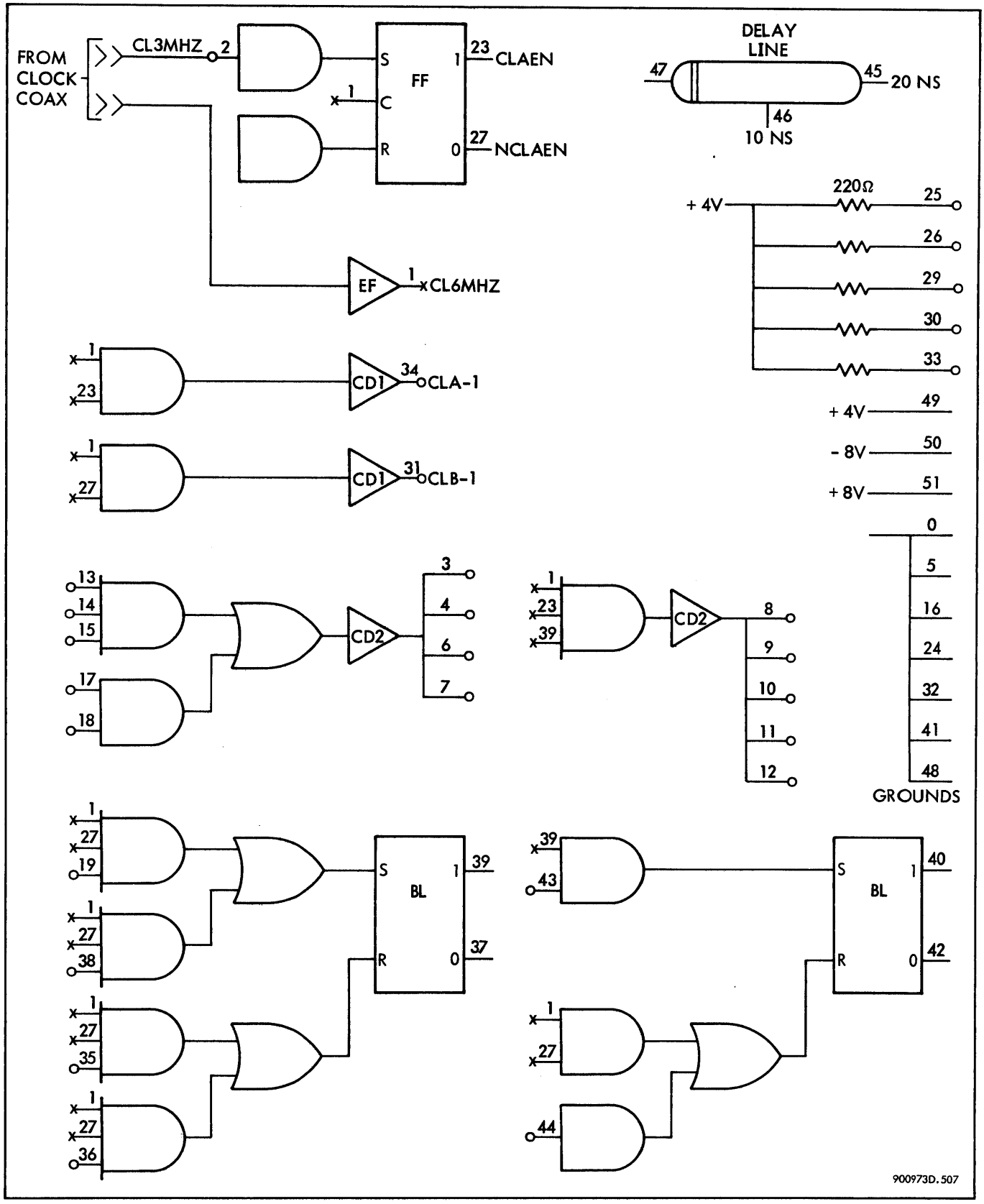


Figure 5-3. AT59 Module, Logic Diagram

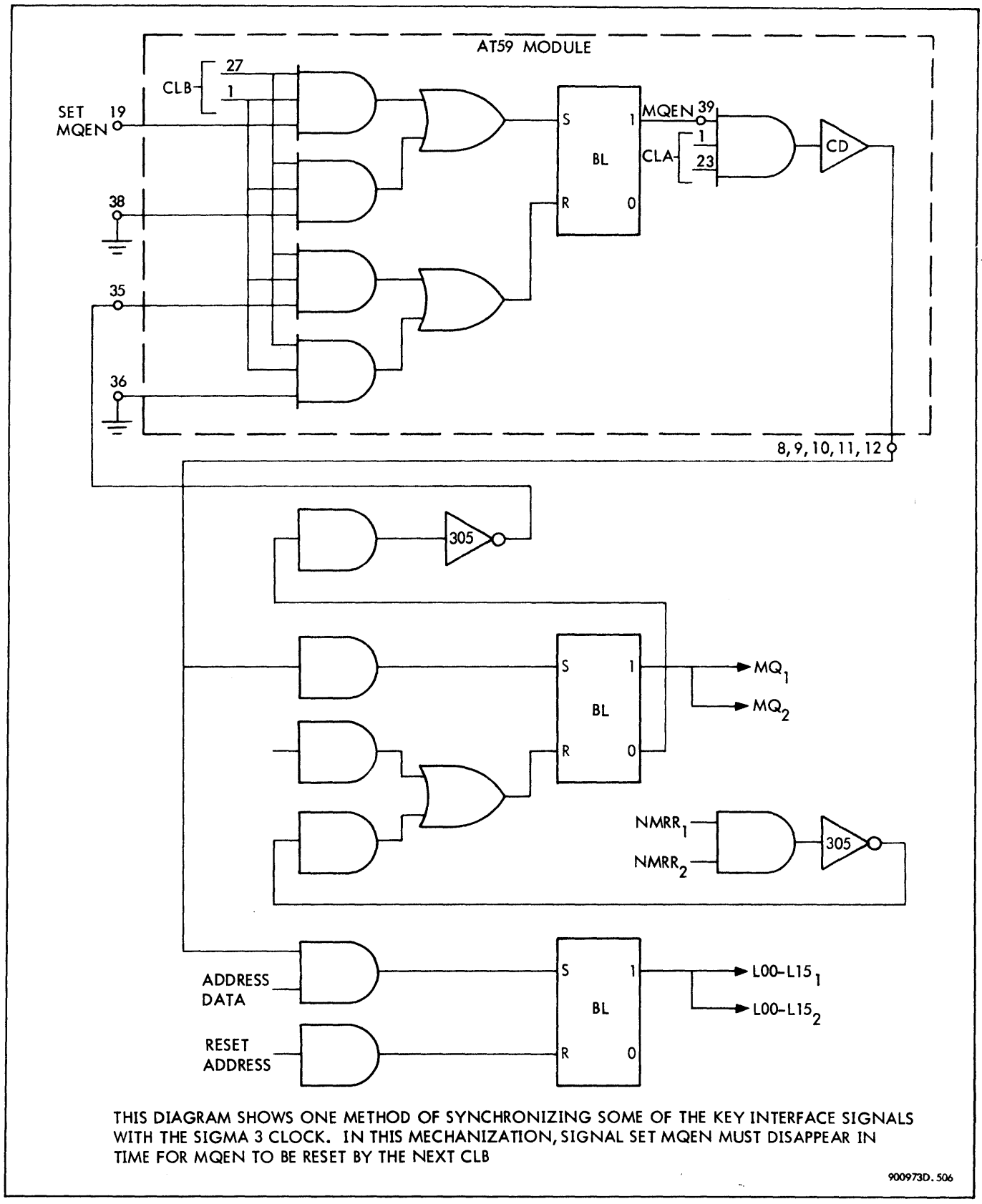


Figure 5-4. AT59 Module, Timing Diagram

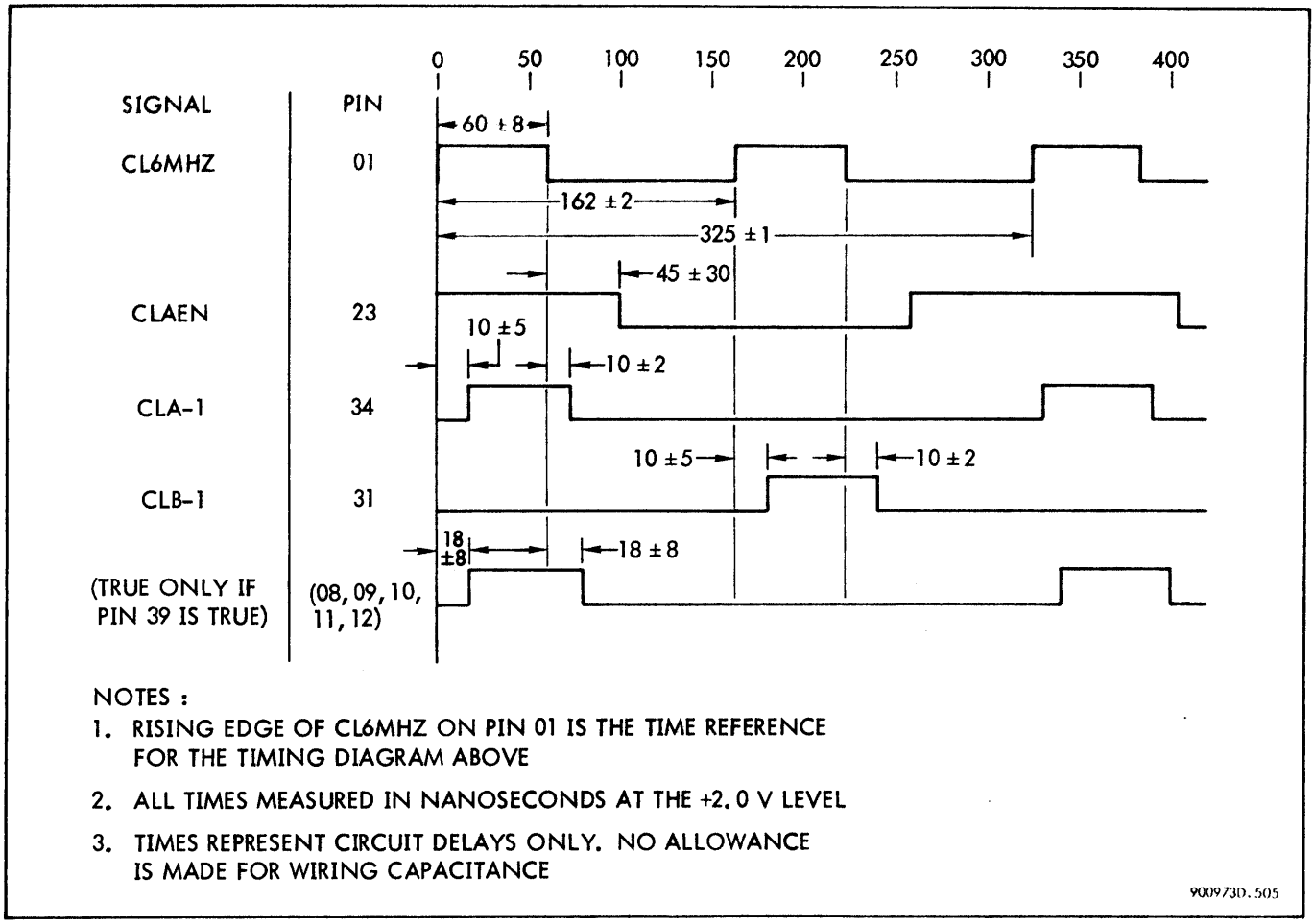


Figure 5-5. Control Logic Mechanization, Logic Diagram

Table 5-6. Sigma 3 Memory Port Cable Locations

	MPM LOCATION	
	CABLE 1	CABLE 2
PORT 1	31D	32D
PORT 2	31C	32C
PORT 3	29C	30C
PORT 4	27C	28C

SECTION VI

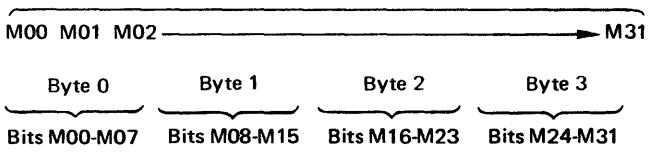
SIGMA 5 AND 7 32-BIT MEMORY INTERFACE

INTRODUCTION

The Sigma 5 and 7 memories can vary in size from 4K to 128K words (K equals 1024). Each word consists of 32 bits plus parity. Parity is generated and checked internally in the memory system. Modes of memory operation are:

1. Full read
2. Full write
3. Partial write

The term full refers to a full word of 32 bits, which consists of four bytes of eight bits each, as illustrated below.



The most significant bit and byte are M00 and byte 0, respectively. The partial write mode allows writing of one or more bytes within a word without altering the remaining byte or bytes within the word. The Sigma 5 and 7 memories consist of one to eight memory banks. Each bank is functionally independent and provides storage for 4K, 8K, 12K, or 16K words.

MEMORY COMMUNICATION

PORT CONCEPT

Each CPU, IOP, or special unit requiring direct connection to Sigma 5 and 7 memory communicates with memory on its own bus. Connection of a bus to each memory bank is made through a port. Memory banks may have one to six ports. Synchronism is not required between banks or between external units. Memory starting address switch settings for each port are listed in table 6-1.

The memory cycle is divided into two intervals, selection and active. During the selection interval, one port is selected for service by the memory bank during the active interval which will follow. The selection interval is initiated by a memory request if no memory cycle is in process. If a memory request (MQ) is received during a memory cycle, initiation of the selection interval is deferred to a point near the end of the active interval. The active interval is initiated by completion of the selection interval. Requests for service are processed as received. If two or more requests are present at the memory ports at the beginning of the selection interval, the request on the port of the highest priority is serviced first. A fixed priority is assigned as follows:

1. Two-port memory bank

Port	Priority
B	1 (highest)
C	2

2. Three-port memory bank

Port	Priority
A	1
B	2
C	3

3. Six-port memory bank (A-expanded)

	Port	Priority
Expansion of port A on three-port bank	1	1
	2	2
	3	3
	4	4
	B	5
	C	6

4. Six-port memory bank (B-expanded)

	Port	Priority
	A	1
Expansion of port B on three-port bank	1	2
	2	3
	3	4
	4	5
	C	6

Either port A or port B may be expanded (figure 6-1 is a port expander installation block diagram). Ports are identical in signals required, connector pin assignments, and in timing required by attaching devices. The selection interval is shortest for port C and identical for all other ports. The shorter selection interval for port C is obtained by allowing a memory bank to preselect port C when no memory cycle is in progress. Virtually no selection time is required in this case to respond to a request for service on port C. Typically, the CPU memory bus is assigned to port C.

MEMORY PORT SEQUENCE

A typical sequence of events is:

1. Memory port user sends address to memory.

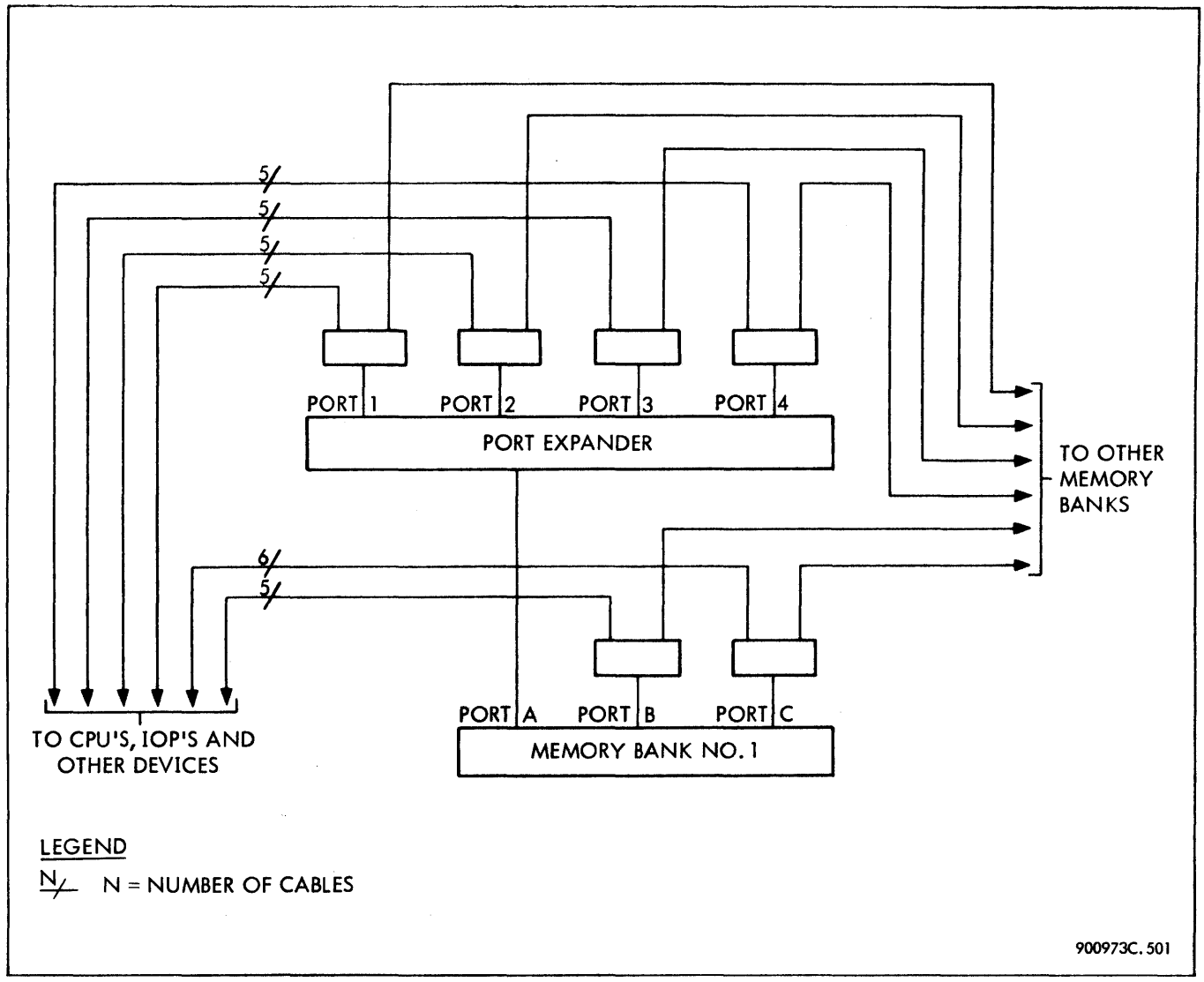


Figure 6-1. Memory Port Expander, Installation Block Diagram

2. Port user sends memory request, write byte signals, and write data (if necessary) to memory.

3. Memory sends address release.

4. Port user drops memory request on receipt of address release.

5. Port user may change address and write byte signals.

6. If operation is read, memory sends read data together with control signals.

7. If operation is write, memory sends data release. Upon receipt of data release signal the port user may change the data lines.

8. If operation is a read or partial write, memory sends parity signals.

9. The sequence repeats as required by the user.

SIGNAL DESCRIPTION

For signals sent to memory, all delays are calculated at the output of the cable receiver in the memory port. For signals sent from memory, all delays are calculated at the input to the cable drivers in the memory port. The port user must therefore make allowances for all additional delays resulting from the following: cable drivers and receivers in the transmission system, cable delays, and cable dispersion. Cable dispersion is the difference in delay of two signals traveling through the same length of cable (for example, a typical 20 ns difference for 40 feet of Xerox standard memory cable). Additional cable information is included in section VIII.

In figures 6-2 and 6-3, many signals are referenced to an internal time (expressed as t_0) in the memory cycle. This time is considered the beginning of the active interval. All times given are in nanoseconds. All signals from memory are pulses and must be handled accordingly. Refer to cable pin assignments in table 6-2 and cable locations in table 6-3.

Table 6-1. Sigma 5 or 7 Memory Starting Address, Toggle Switch Settings

UNIT	PORT	STARTING ADDRESS BIT					SWITCH MODULE LOCATION
		15	16	17	18	19	
Sigma 5 or 7 Memory	A	11	12	13	14	15	20C
	B	6	7	8	9	10	20C
	C	11	12	13	14	15	21C
Port Expander F	1	1	2	3	4	5	24D
	2	6	7	8	9	10	24D
	3	1	2	3	4	5	25D
	4	6	7	8	9	10	25D
Port Expander S	1	1	2	3	4	5	21E
	2	6	7	8	9	10	21E
	3	1	2	3	4	5	22E
	4	6	7	8	9	10	22E
		64K*	32K*	16K*	8K*	4K*	

*Bit weight

MEMORY REQUEST (MQ)

The memory request signal initiates a request for a memory cycle in memory. The memory request signal must occur no sooner than 35 ns after the address lines have settled and must remain true until the address release signal is present on the port. The memory request signal must be dropped on receipt of the address release signal prior to changing the address lines.

ADDRESS (L15-L31)

Signals on the address lines must be present at least 40 ns before the memory request MQ signal is given and must remain stable until the address release signal is received from memory. The address signals must remain stable until after MQ is dropped at the memory.

ADDRESS HERE (AH)

The address here signal is generated by the port if the address represented by the signals on the address lines specifies a location in the memory bank. This is a function of the settings of the starting address switches, the memory module size, and the interleave pattern. The AH signal tracks the address line signals with a 110 ns maximum delay.

DATA TO MEMORY (M00-M31)

Signals on the data lines must be stable within 100 ns after t_0 and must not change until the data release signal is present on the port.

DATA FROM MEMORY (M00-M31)

See figures 6-2 and 6-3 for timing.

WRITE BYTE (MW0-MW3)

Write byte signals MW0 through MW3 indicate which of the four bytes are to be written into memory. If all four write byte lines are ones, a write full operation is performed. If no write byte lines are ones, a read operation is performed. A write partial operation is performed otherwise. The write byte signals must be stable on the line at the memory port no later than 25 ns after t_0 and must not change until address release.

ABORT (ABO)

The abort signal overrides a write operation (specified by write byte signals) and prevents changing the contents of the memory location. The abort signal must occur within 100 ns after t_0 and must remain until data release. This signal is reserved for CPU use only.

MEMORY REQUEST RELEASE (MQR)

The address release signal is a pulse signifying the following:

1. Memory request signal can be dropped.
2. Address lines can now be dropped.
3. Write byte lines can be dropped.

For address release timing see figures 6-2 and 6-3.

DATA RELEASE (DR)

The data release signal is a pulse signifying that the data lines may be dropped during a write operation. For a read operation, DR may be used as a timing signal if needed. For timing see figures 6-2 and 6-3.

EARLY DATA RELEASE (EDR)

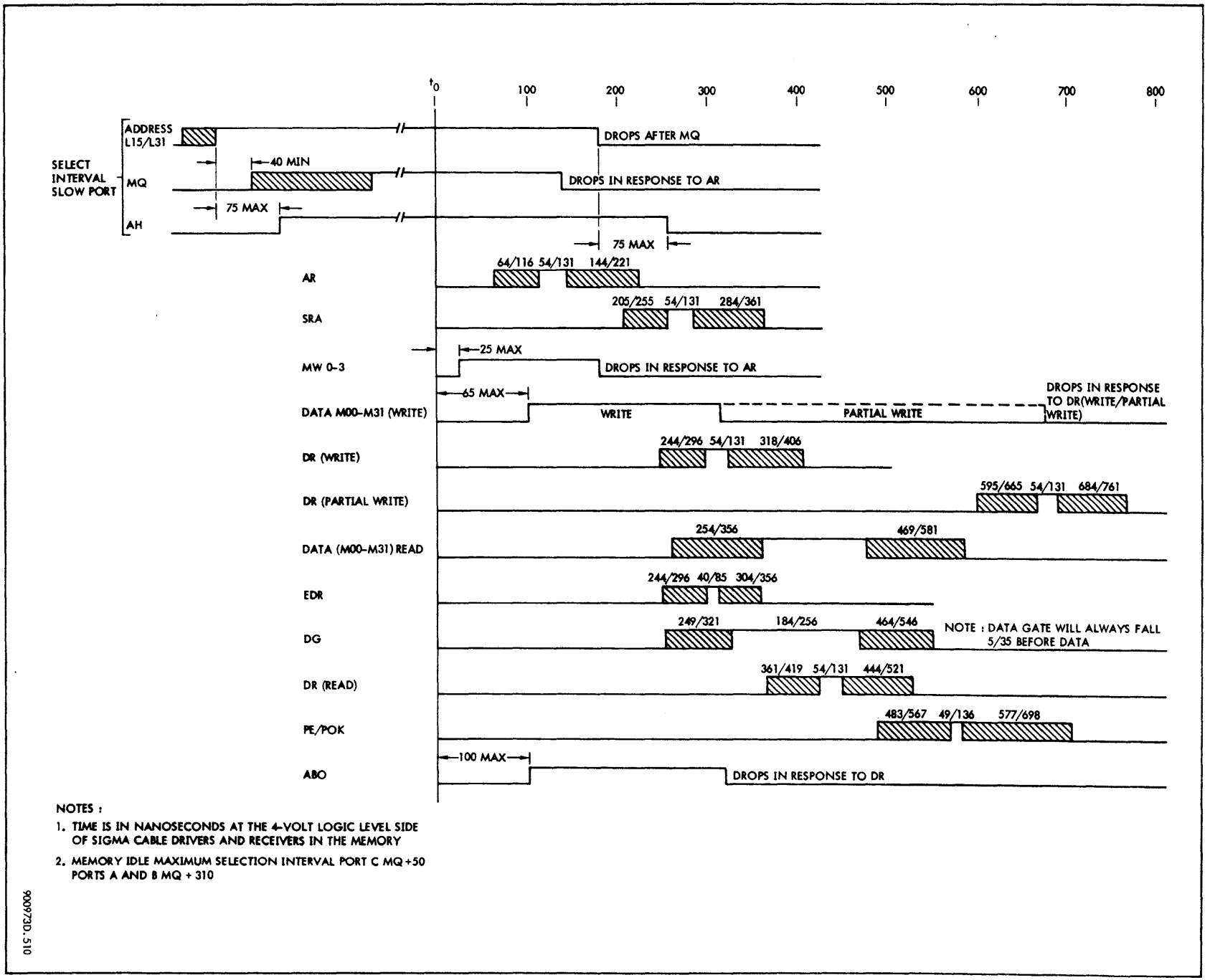
The early data release signal is a pulse used only during the read mode to clear the receiving register. For timing see figures 6-2 and 6-3. This signal is reserved for CPU use only.

DATA GATE (DG)

The data gate signal gates data into the receiving register for a read operation. For timing see figures 6-2 and 6-3.

SECOND REQUEST ALLOWED (SRA)

The second request allowed signal indicates that it is permissible to initiate a subsequent memory request on a bus. When using more than one memory bank, the port user must not send a memory request until 50 ns after SRA.

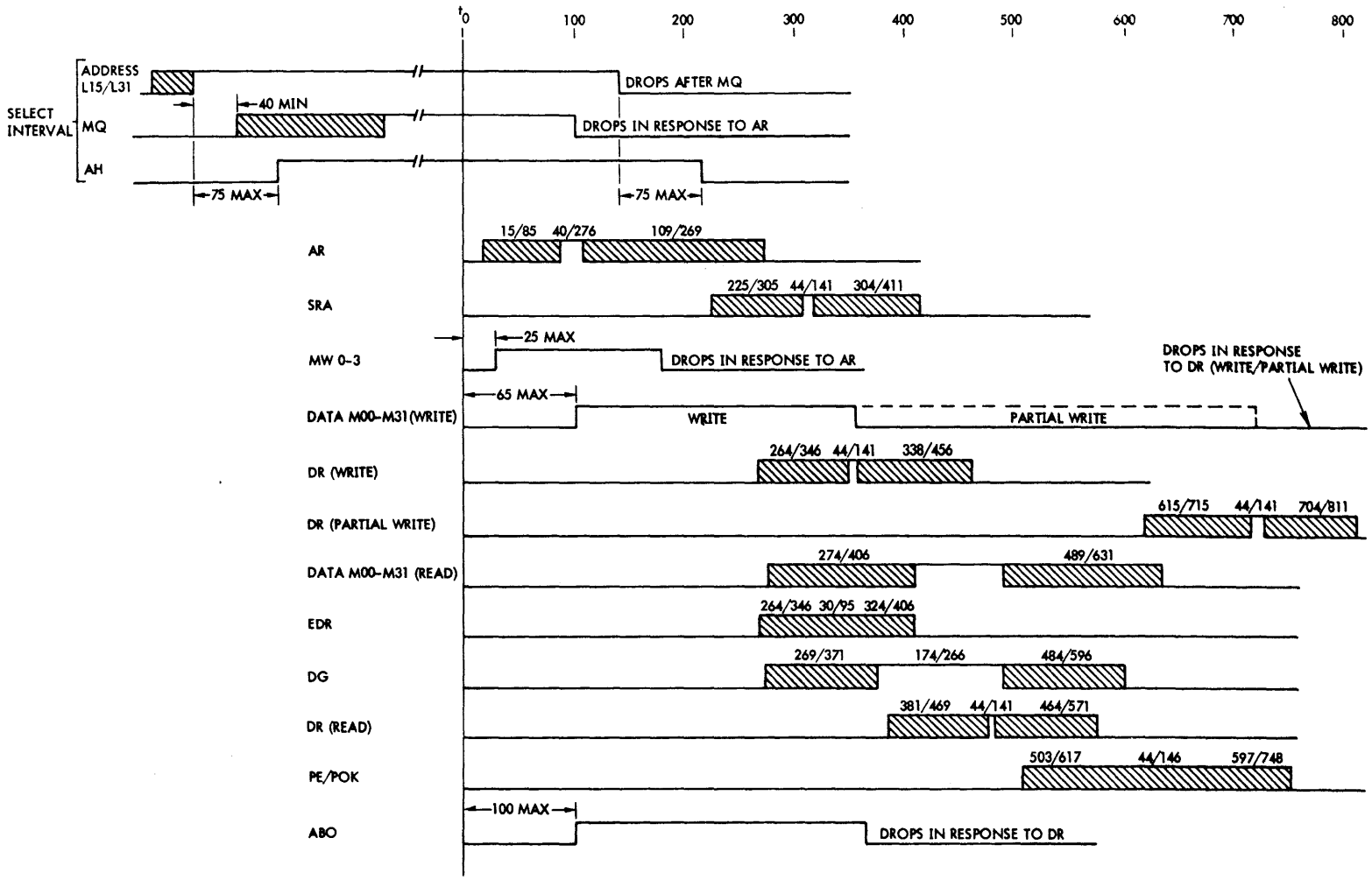


NOTES :

1. TIME IS IN NANOSECONDS AT THE 4-VOLT LOGIC LEVEL SIDE OF SIGMA CABLE DRIVERS AND RECEIVERS IN THE MEMORY
2. MEMORY IDLE MAXIMUM SELECTION INTERVAL PORT C MQ+50 PORTS A AND B MQ + 310

900973D.510

Figure 6-2. Ports A, B, and C, Timing Diagram



NOTES :

1. TIME IS IN NANOSECONDS AT THE 4-VOLT LOGIC LEVEL SIDE OF SIGMA CABLE DRIVERS AND RECEIVERS IN THE MEMORY
2. MEMORY IDLE MAXIMUM SELECTION INTERVAL THROUGH PORT EXPANDER IS : MQ + 350

9009730.511

Figure 6-3. Ports 1, 2, 3, and 4, Timing Diagram

Table 6-2. Sigma 5 or 7 Memory Cables for Signals

CABLE CONNECTOR PIN	BACKPANEL CONNECTOR PIN	SIGNAL NAME				
		Cable 1 Module AT11	Cable 2 Module AT11	Cable 3 Module AT11	Cable 4 Module AT12	Cable 5 Module AT11
2	1 4	M00D M00R	M14D M14R	M28D M28R	L15D	MQD
1	2 6	M01D M01R	M15D M15R	M29D M29R	L16D	* AHR
4	3 8	M02D M02R	M16D M16R	M30D M30R	L17D	* ARR
3	9 10	M03D M03R	M17D M17R	M31D M31R	L18D	* DRR
5	12 13	M04D M04R	M18D M18R	L29D	L19D	* PER
6	15 18	M05D M05R	M19D M19R	L30D	L20D	* SRAR
7	19 20	M06D M06R	M20D M20R	L31D	L21D	*
8	23 22	M07D M07R	M21D M21R	MW0D	L22D	ABOD
9	25 27	M08D M08R	M22D M22R	MW1D	L23D	* POKR
10	33 34	M09D M09R	M23D M23R	MW2D	L24D	*
11	35 36	M10D M10R	M24D M24R	MW3D	L25D	*
12	37 38	M11D M11R	M25D M25R	* DGR	L26D	*
13	39 40	M12D M12R	M26D M26R	* EDRR	L27D	*
14	45 42	M13D M13R	M27D M27R	*	L28D	*

*Must be hard wired to ground by port user.

Note

Signals described are from point of view of user of a memory port. Backpanel connector pins are for standard XDS cable drivers and receivers. Signals ending in D are cable driver inputs. Signals ending in R are cable receiver outputs. Unused driver inputs must be grounded

Table 6-3. Sigma 5 or 7 Memory Cable Location Chart

PORT	CHASSIS CONNECTOR LOCATIONS					UNIT
	Cable 1	Cable 2	Cable 3	Cable 4	Cable 5	
A	A2	B2	A4	C4	C6	Memory bank
B	A6	B6	B4	D2	D4	Memory bank
C	A8	B8	C8	D6	D8	Memory bank
1*	B2	D2	B10	B18	B26	Port expander
2*	B4	D4	B12	B20	B28	Port expander
3*	B6	D6	B14	B22	B30	Port expander
4*	B8	D8	B16	B24	B32	Port expander

*Presence of ports 1, 2, 3, 4 requires deletion of either port A or port B

PARITY ERROR AND PARITY OK (PE AND POK)

The parity error (PE) and parity OK (POK) signal pulses indicate the result of the parity check. One or the other of these signals occurs on a port for every read or partial write operation made through that port. For timing see figures 6-2 and 6-3.

HIGH SPEED OPERATION

For high speed operation, all times given herein assume no interference from other ports.

DESIGN AIDS

ACCESSING DATA FROM ONE MEMORY MODULE

When accessing successive data from the same memory module, the nominal cycle time of a memory bank is 850 ns, with a range of 770 to 870 ns. This rate can be obtained only if successive memory requests are received sufficiently early in the cycle. To operate at this rate, the next MR must be received by memory within 360 ns after the prior AR for ports A, B, 1, 2, 3, and 4. If this parameter is not met, the effective cycle time may be as long as 1200 ns.

ACCESSING DATA FROM MULTIPLE MEMORY MODULES

When accessing successive data from different memory modules the most important consideration is that discussed under SRA for port C. If a read operation is followed by a write, another limiting factor is the clearing of the data bus. The data bus carries read information late into the read cycle yet must pick up write data early in the write cycle. The absolute minimum effective cycle time is 560 ns. A typical method of reading and holding memory data is shown in figure 6-4.

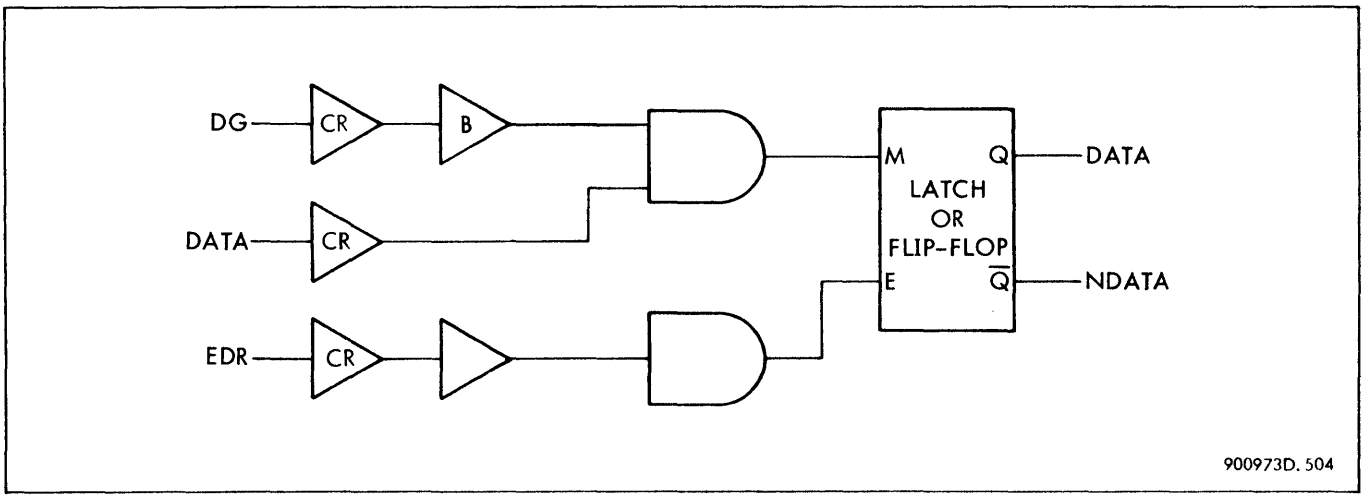


Figure 6-4. Read and Hold Memory Data, Logic Diagram

SECTION VII

INTERRUPT AND CLOCK INTERFACE

INTRODUCTION

For priority interrupts, Sigma 5 and 7 can accommodate up to 14 groups (or chassis) with each chassis furnishing a maximum of 16 interrupt levels. In Sigma 2, one group of four integral levels and eight external groups of 16 levels are available. In Sigma 3, one group of four integral levels and six external groups of 16 are available. The priority of each chassis is determined by the arrangement of cabling.

EXTERNAL PRIORITY INTERRUPTS

Three cables are used to interface a priority (external) interrupt control chassis and user equipment. Design considerations for interrupt chassis interfaces are identical for all Sigma computers. Interrupt Chassis Model 8021 is used for Sigma 2; Model 8121 for Sigma 3; Model 8221 for Sigma 5; and Model 8421 for Sigma 7. Each interrupt chassis contains three AT11 cable connector modules. Receiver and driver networks are used at the external interrupt interface. Refer to section I for a description of the cable driver-receiver scheme employed. The user may drive a given transmission line from more than one source and may receive a given transmission line at more than one destination. Three types of signals are transmitted across the interface as listed in table 7-1. Signals IN00 through IN15 are interrupts from external equipment with IN00 holding highest priority within the given chassis and IN15 the lowest. Signals RE00 through RE15 are response (feedback) lines with RE00 corresponding to the highest priority interrupt requests and RE15 the lowest. Figure 7-1 is a diagram of the external priority interrupt chassis interface.

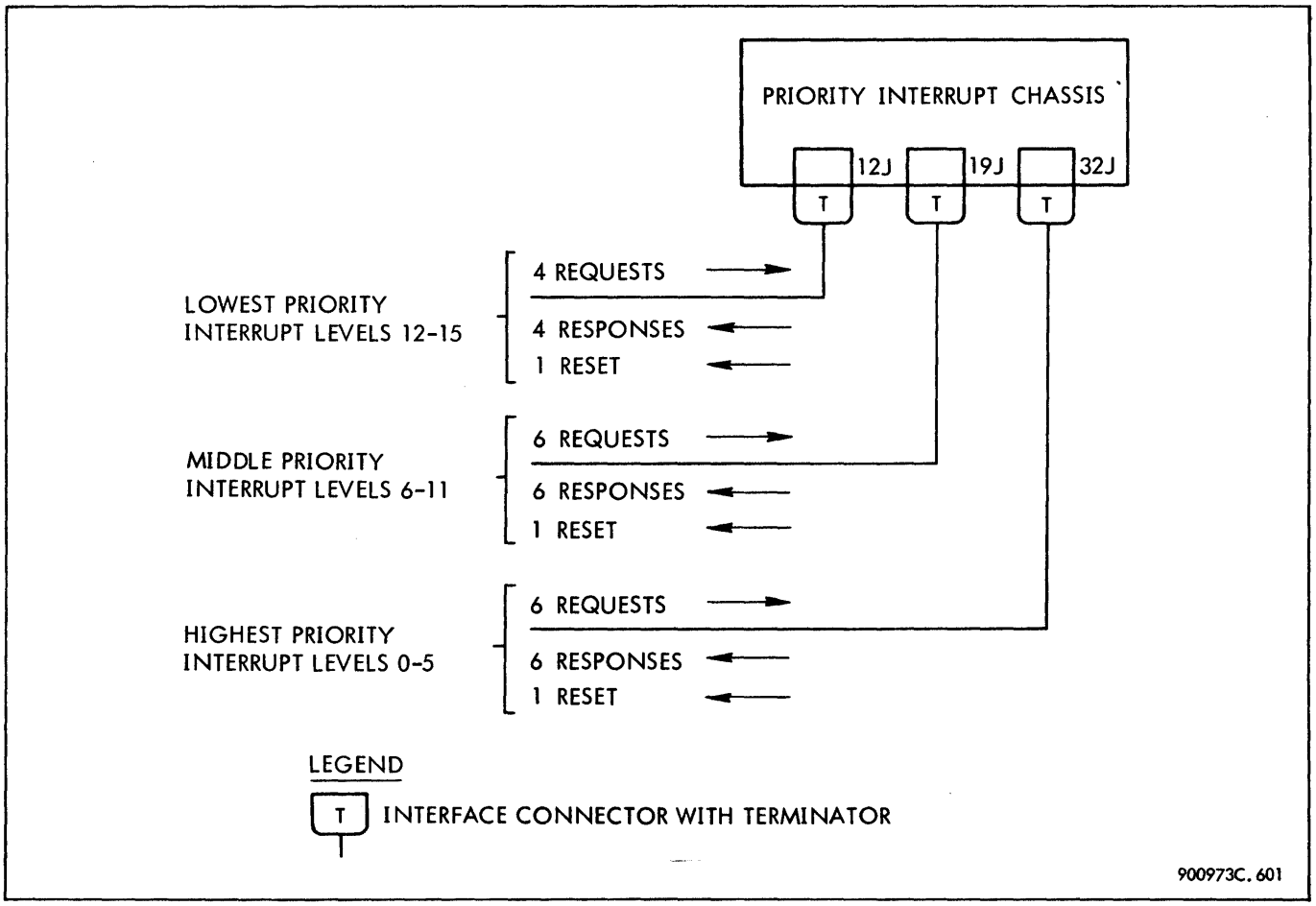


Figure 7-1. External Priority Interrupt Chassis, Interface Diagram

General reset signal RSTI is equivalent to the reset signal provided by the CPU for the IOP and the DIO interfaces. This signal may be utilized by the user to initialize his logic when the CPU logic is initialized.

Table 7-1. Interrupt Interface Signals

Function	Signal
General reset signal	RST
User requests for service	IN00-IN15*
Responses for user requests for service	RE00-RE15†

*IN00-IN15 implies requests to interrupt levels 0-15

†RE00-RE15 implies responses (acknowledgments to requests made to interrupt levels 0-15

A user request (INXX) is remembered by the external interrupt logic if the requested level was armed before the service request was made. If the requested level was not previously armed, the user request for service is disregarded.

The interrupt logic works on a request-response basis or on a request-only basis. If the system is used on a request-only basis, the minimum acceptable pulsewidth of the service request is 1.25 μs for Sigma 7, 2.5 μs for Sigma 5, 1.15 μs for Sigma 2, and 1.8 μs for Sigma 3.

The external interrupt logic generates a positive response to the user as soon as a user request for service has been accepted. The response remains true from the time the service request is accepted until the interrupt routine has been completely processed. The response (REXX) can therefore be used to control the repetition rate of the service request. Since a service request is accepted only by an armed interrupt level, the fact that the interrupt level is armed implies that it is not presently busy. The time sequencing of the external interrupt request and response is shown in figure 7-2. Note that in figure 7-2 the second INXX cannot go true until the REXX for the first INXX has gone false.

If the user exceeds the allowable request repetition rate (for example, by issuing a new request before REXX from the previous request has terminated), requests will be made which will not be acknowledged. The end result is that the user is not served each time he makes a request for service. If the maximum pulsewidth is exceeded, the CPU may process a given routine more than once for a single request.

SIGMA 2 OR 3 INTEGRAL PRIORITY INTERRUPTS

All logic characteristics of Sigma 2 or 3 integral interrupts are identical to external priority interrupts except that internal interrupt signal connections are made directly to a reserved area within the CPU rather than to an external chassis.

One cable provides communication for 12 signals to interface the integral interrupts and user equipment. Four signals are inputs for four external real-time clocks: CP1, CP2, CP3, and CP4. When these signals are used to make requests to the real-time clock interrupt levels, a request is made each time that the clock makes a negative transition. The duration of the pulse is not critical. The time between pulses must be at least long enough to permit the interrupt level to service the request. Upon reaching an interrupt point, the Sigma 2 CPU requires 2.5 μs to service a real-time clock interrupt. The Sigma 3 CPU requires 3.6 μs.

Four signals are input requests for the four integral priority interrupt levels: ER1, ER2, ER3, and ER4. Four signals are responses to these requests: ERS1, ERS2, ERS3, and ERS4.

When an internal request is made, the user raises the appropriate ER line. When the request has been sensed, the system responds by raising the corresponding ERS line. The ERS line remains true until the user is allowed to make another interrupt service request.

INTERRUPT INTERFACE SERVICE MODULES

MODULE AT11

The AT11 incorporates 14 cable driver-receiver circuits each of which corresponds to the schematic shown in figure 7-3. In the schematic, P1 is the regular backwiring connector and P2 and P3 represent both sides of the cable connector at the front edge of the module. Each circuit is usable as a cable driver or cable receiver. The AT11 can be used by the external equipment as an interrupt signal driver and response receiver for up to six interrupt levels. Inputs of unused drivers must be grounded in the external equipment.

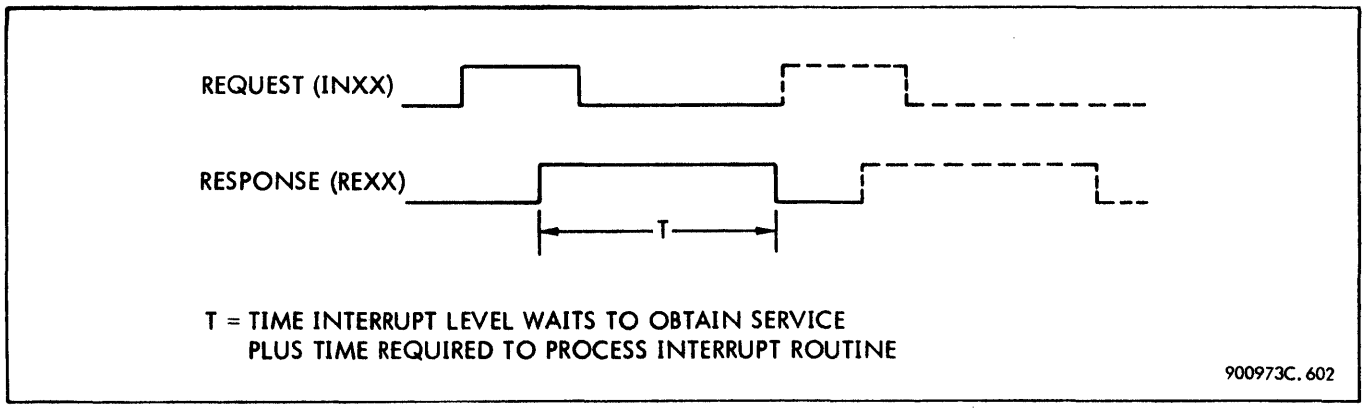


Figure 7-2. External Interrupt Request and Response, Timing Diagram

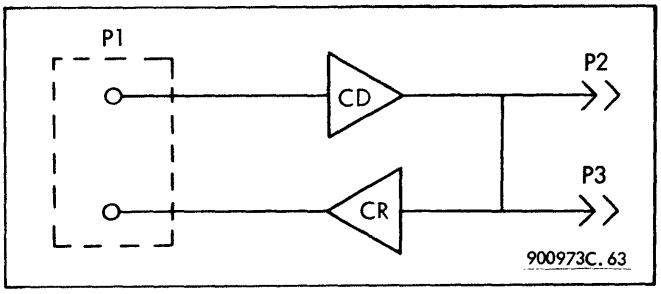


Figure 7-3. AT11 Cable Driver-Cable Receiver Circuit, Schematic Diagram

MODULE AT39

The AT39 cable plug module has four drivers and receivers in the four highest priority positions. The cable pin connectors for the four circuits are similar to those for AT11. The AT39 is a more economical module than the AT11 when four or fewer interrupt levels are used per connector.

MODULE LT55

The LT55 module is indicated for one- or two-level interrupt installations. The highest priority cable connector pins are used for transmission and reception of interrupt and acknowledgment signals, respectively. The module also includes two independent sets of decoders for unrelated functions.

MODULE ST29

The ST29 cable connection module consists of four cable receivers and four cable drivers. The ST29 is installed in the Sigma 2 CPU at location 7B for the four-level interrupt system. Unlike the AT11, AT39, and LT55, the ST29 does not have both sides of the cable connector tied together. A termination block therefore cannot be installed on one side of the cable. The receivers on the ST29 have 33-ohm termination resistors mounted on the module. The drivers are not terminated on the board and can drive only one external 33-ohm resistor compared to two such loads for the AT11, AT39, and LT55. The standard procedure is to terminate the cable on both ends with a 33-ohm resistor. For an external cable chain, only a single terminator is necessary at the remote end of the chain.

CHAIN INTERCONNECTION OF USER REQUESTS TO PRIORITY INTERRUPT INTERFACE

Various methods can be used to interconnect external interrupt signals to the Sigma 2, 3, 5 or 7 priority interrupt chassis or to the Sigma 2 or 3 integral system. The means of interconnection is by two types of 14-conductor, 33-ohm shielded cable.

ET10 DIRECT CABLE

The ET10 cable is a standard coupling device with one-to-one wiring between corresponding pins of the connectors. The ET10 carries subassembly number 127314 with a three-digit-length code appended.

ET15 OFFSET CABLE

The ET15 is a cable specially designed to overcome level coincidence confusion. In the ET15, wiring to corresponding pins is offset by two. The scheme is such that, when all cables are chained, all signals are properly routed by completed functional rotation. Use of the ET15 obviates wiring changes in an external unit regardless of the desired priority levels. The ET15 carries assembly number 139241 with a three-digit length code applied. Figure 7-4 is a diagram of the offset ET15 interconnections.

EXAMPLES OF CHAIN INTERCONNECTION METHODS

In figure 7-5 (sheet 1), the two highest priority interrupt levels are routed directly through standard ET10 cable to the six-level 8X21 interrupt chassis. The drivers are connected to P3-R and P2-14 on the AT11 module. The receivers are connected to P3-H and P2-8. All other drivers on the AT11 should be grounded. The AT39 has four drivers connected to R, P, N, and M of P3. Since the ET15 cable which connects the AT39 to the AT11 is offset, these signals are routed via the pins on the external AT11 to the lower four levels.

In figure 7-5 (sheet 2), the inverse of the previous illustration shows four levels from the AT39 with the highest priority. To use additional equipment, the ET15 cable must be reversed. The AT11 can then supply fifth and sixth level interrupts to the interrupt chassis which is connected in the middle of the chain.

In figure 7-5 (sheet 3), three controllers (each with two interrupts) are shown connected with two ET15 cables in a manner to obtain correct priority.

In figure 7-5 (sheet 4), virtually any combination of priority interrupt level is shown to be feasible using the direct and offset cables.

DESIGN AIDS

REAL-TIME CLOCK INPUTS

1. A Xerox cable driver module should be incorporated at the user's end of the cable.

2. A cable should be terminated at the user's end only. Terminations are not permissible at the interface.

3. Real-time clock requests are made with the falling edge of the user's request.

4. For cable pin information refer to tables 7-2 and 7-3.

5. Pulse duration is not critical. The time between falling edges must be sufficiently long to allow the CPU to process a single instruction interrupt. The minimum pulse width required at the interface is 50 ns.

PRIORITY INTERRUPTS

1. Xerox driver-receiver modules should be used when connecting to the interface.

2. Cables should be terminated at the interface and at the user's end. The terminator designation is ET13.

3. For cable pin information refer to tables 7-4 and 7-2.

4. The minimum pulsewidth of the user's request is 2.5 times the period of the priority interrupt logic clock. The maximum pulsewidth is determined by the time required to complete the interrupt subroutine.

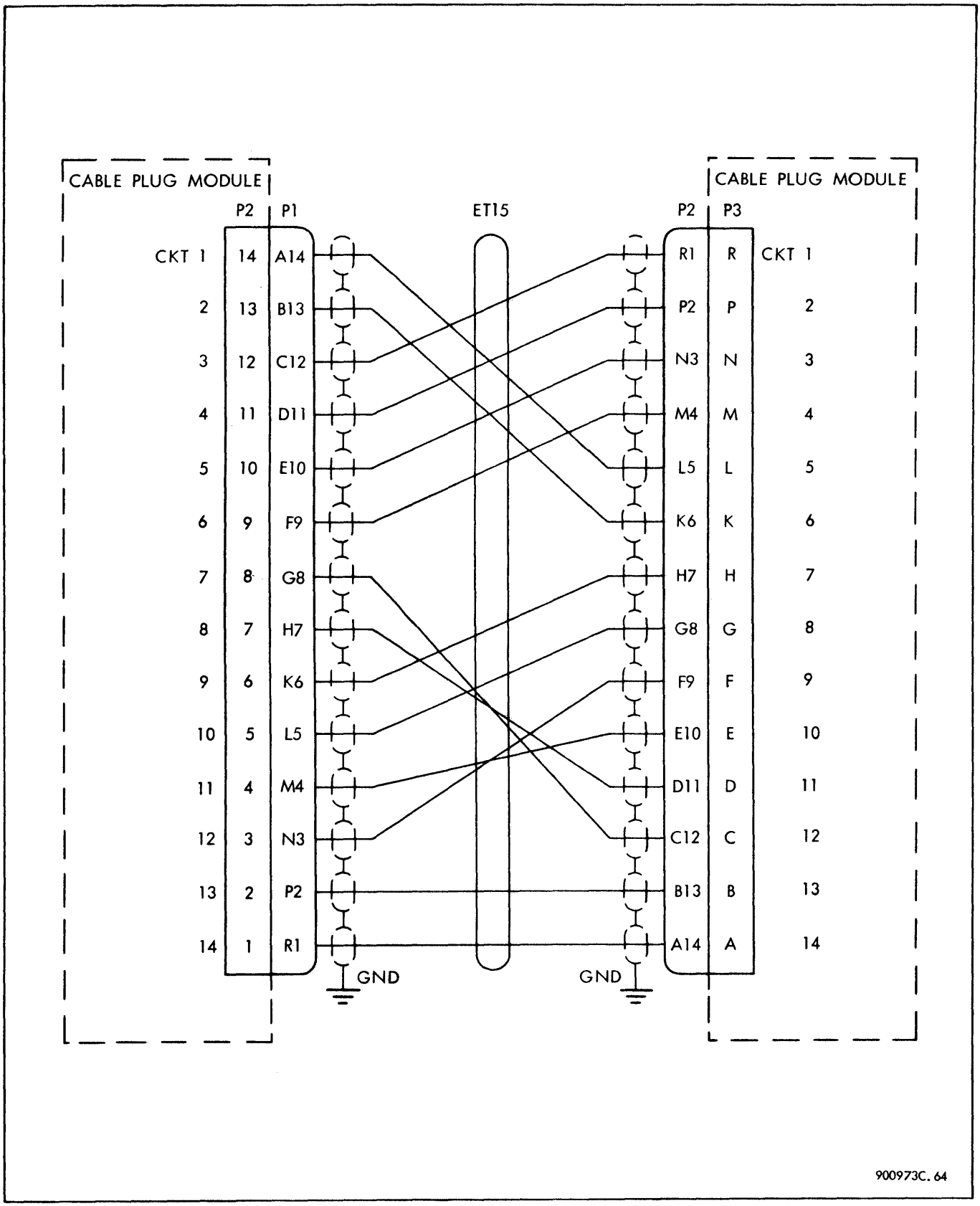


Figure 7-4. ET15 Priority Interrupt, Cable Diagram

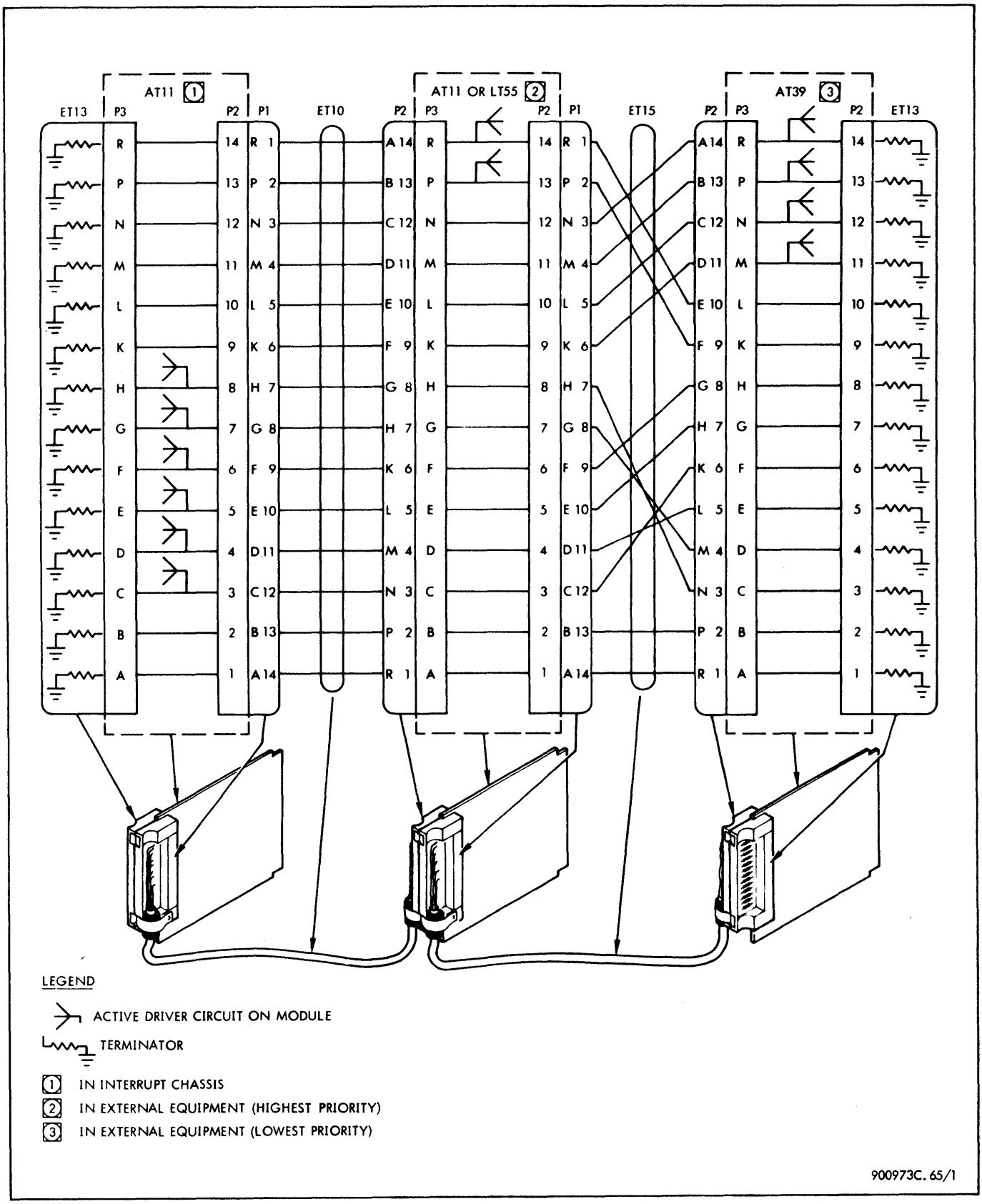


Figure 7-5. Priority Interrupt Interface Connections (Sheet 1 of 4)

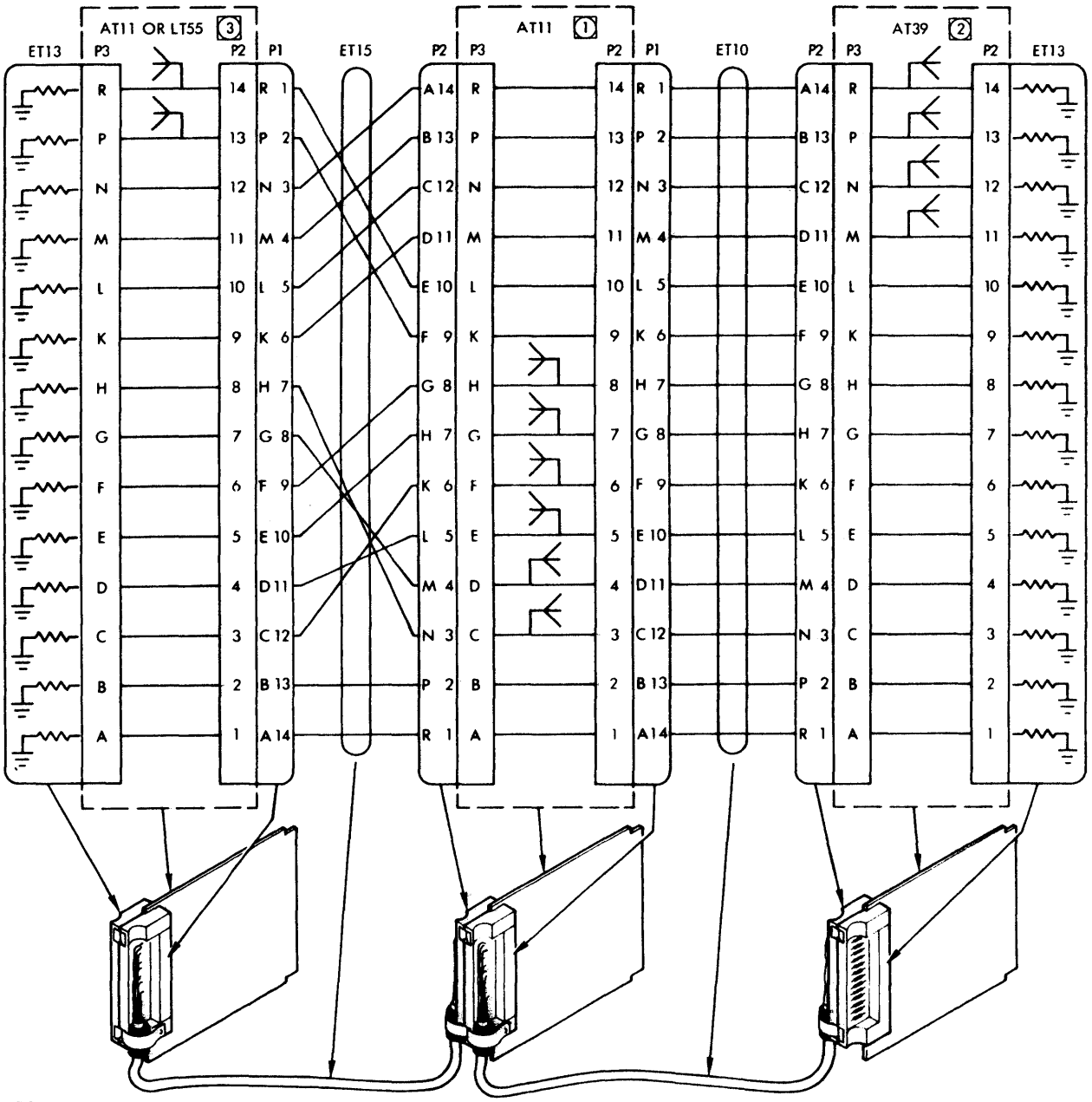


Figure 7-5. Priority Interrupt Interface Connections (Sheet 2 of 4)

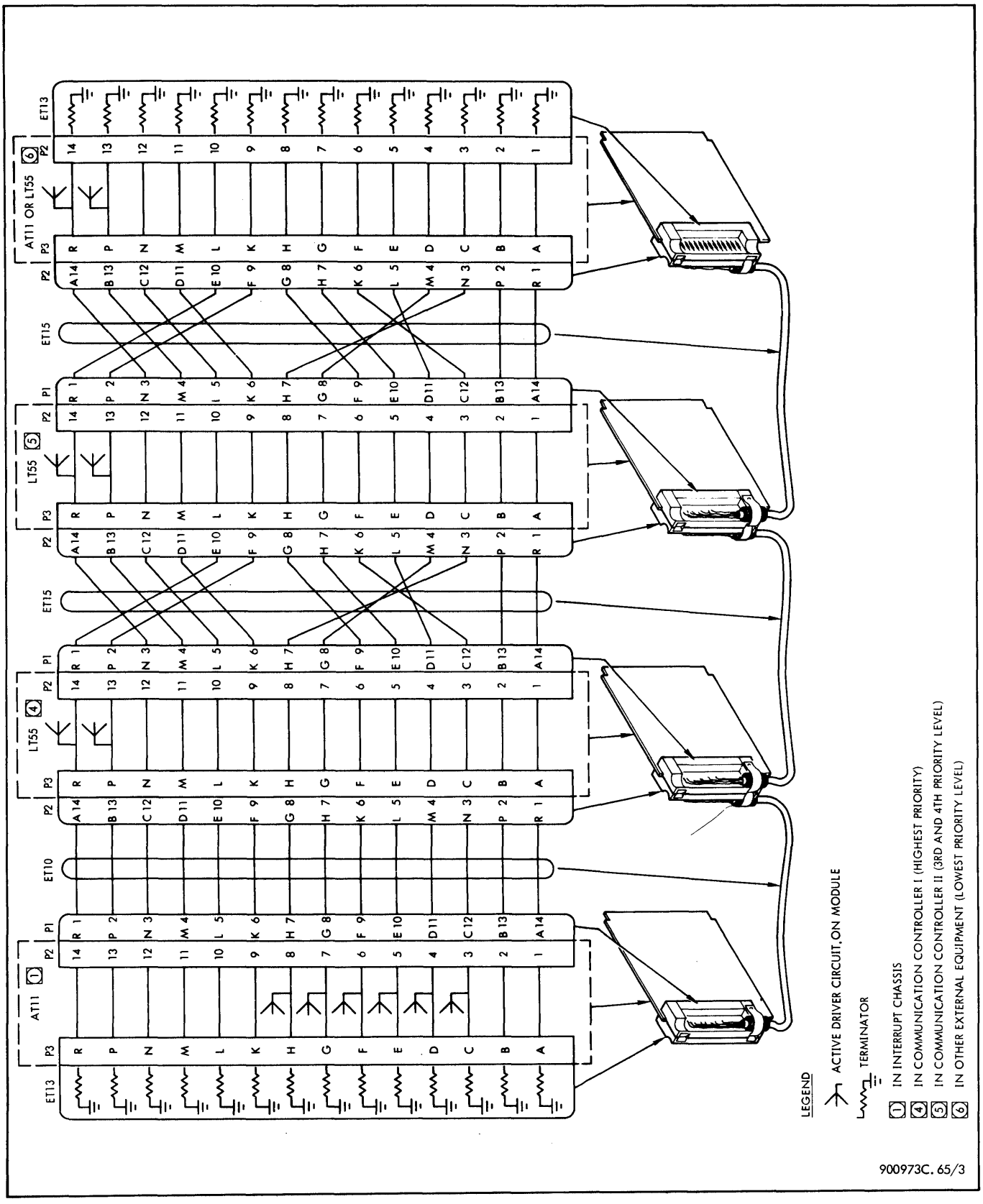


Figure 7-5. Priority Interrupt Interface Connections (Sheet 3 of 4)

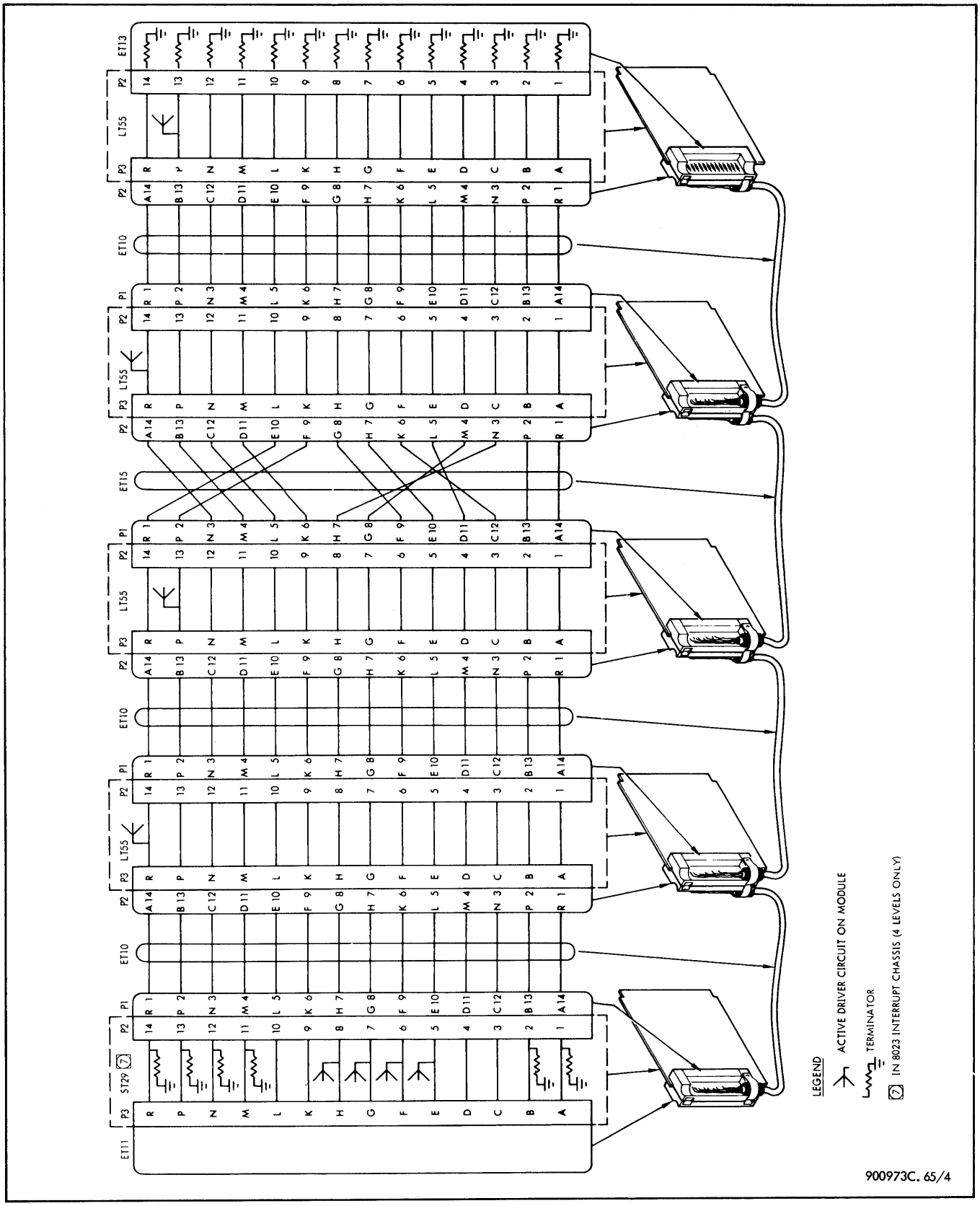


Figure 7-5. Priority Interrupt Interface Connections (Sheet 4 of 4)

Table 7-2. Sigma 2 or 3 Integral Priority Interrupt and Clock Cable Signals

Cable Connector Pin	Backpanel Connector Pin	Signal Name		Cable Connector Pin	Backpanel Connector Pin	Signal Name	
		Sigma 3	Sigma 2			Sigma 3	Sigma 2
2	6	/INT:CP2/	/CP2/	8			
					30	/INT:ERS1/=I16S	/IS16/
1	7	/INT:CP1/	/CP1/	9		NOT USED	
4	11	/INT:CP4/	/CP4/	10		NOT USED	
3	9	/INT:CP3/	/CP3/	11	34	/INT:ER4/	/ER4/
5				12	36	/INT:ER3/	/ER3/
	10	/INT:ERS4/=I19S	/IS19/				
6				13	38	/INT:ER2/	/ER2/
	12	/INT:ERS3/=I18S	/IS18/				
7				14	40	/INT:ER1/	/ER1/
	39	/INT:ERS2/=I17S	/IS17/				

NOTES: 1. Module ST29, location 7B (Sigma 2 CPU), 23C (Sigma 3 CPU).

2. Numbered side is not connected (Not plated through) on ST29 cable connector contacts.

Table 7-3. Sigma 5 or 7 Clock Cable Signals

USER REQUEST TO REAL-TIME CLOCKS		CABLE PIN DESIGNATION	CONNECTOR LOCATION	
Interface Designation	Legend		Sigma 5	Sigma 7
ECPUL1	Request Clock Counter No. 1 (Interrupt level 2)	G	2K	30W
ECPUL2	Request Clock Counter No. 2 (Interrupt level 3)	H		
ECPUL3	Request Clock Counter No. 3 (Interrupt level 4)	K		

Note

All signals are received by the CPU. No external acknowledgement is provided. Interrupt level 2 is associated with memory location X'52', level 3 with X'53', and level 4 with X'54'

Table 7-4. Sigma 2 or 3 External Priority Interrupt Cable Signals

CABLE CONNECTOR PIN	BACKPANEL CONNECTOR PIN	SIGNAL NAME CONNECTOR LOCATION		
		J12	J19	J32
2	1 4			
1	2 6	* RST	* RST	* RST
4	3 8		* RE11	* RE05
3	9 10		* RE10	* RE04
5	12 13	RE15	* RE09	* RE03
6	15 18	* RE14	* RE08	* RE02
7	19 20	* RE13	* RE07	* RE01
8	23 22	* RE12	* RE06	* RE00
9	25 27		IN11	IN05
10	33 34		IN10	IN04
11	35 36	IN15	IN09	IN03
12	37 38	IN14	IN08	IN02
13	39 40	IN13	IN07	IN01
14	45 42	IN12	IN06	IN00

*Must be grounded

Note

REXX signals imply response to or acknowledgment of user requests to interrupt level XX. INXX signals are received at Models 8021, 8221, and 8421 interfaces and imply user requests to interrupt level XX

SECTION VIII

CABLE AND SIGNAL DATA

PERIPHERAL EQUIPMENT TESTER MODEL 7901

Peripheral Equipment Tester Model 7901 is an offline or online monitor unit for device controller operations. Model 7901 is a general-purpose, self-powered, portable unit with two cables for tie-in to the controller by means of module connectors. The tester requires about 5 percent of the total module count of a DC (not including the two tester connector positions) used in the system:

Model 7901 includes the following features:

1. Parity generator
2. Voltage monitor
3. Indicator lamps
4. Nine-bit comparator logic
5. Twelve-stage binary counter
6. Clock signals
7. Unique overlay panels for each device controller

The best location for connecting the tester to a DC is at a point where IOP signals are most closely simulated. The most economical location for tester integration is at the controller-subcontroller interface where the bulk of the controller logic can be tested.

The tester switches can be used to check controller operations such as SIO, HIO, OOUT, DIN, and DOUT at a single-step or running rate. In addition, state counter outputs and unusual condition outputs can be monitored. The tester binary counter can be used to generate a sequentially increasing pattern to output devices. When used with the comparator logic, the binary counter can be used for checking the operation of all input devices.

Figure 8-1 is a representation of the control panel for a peripheral equipment tester.

Refer to Xerox technical manual publication No. 901004 for additional information.

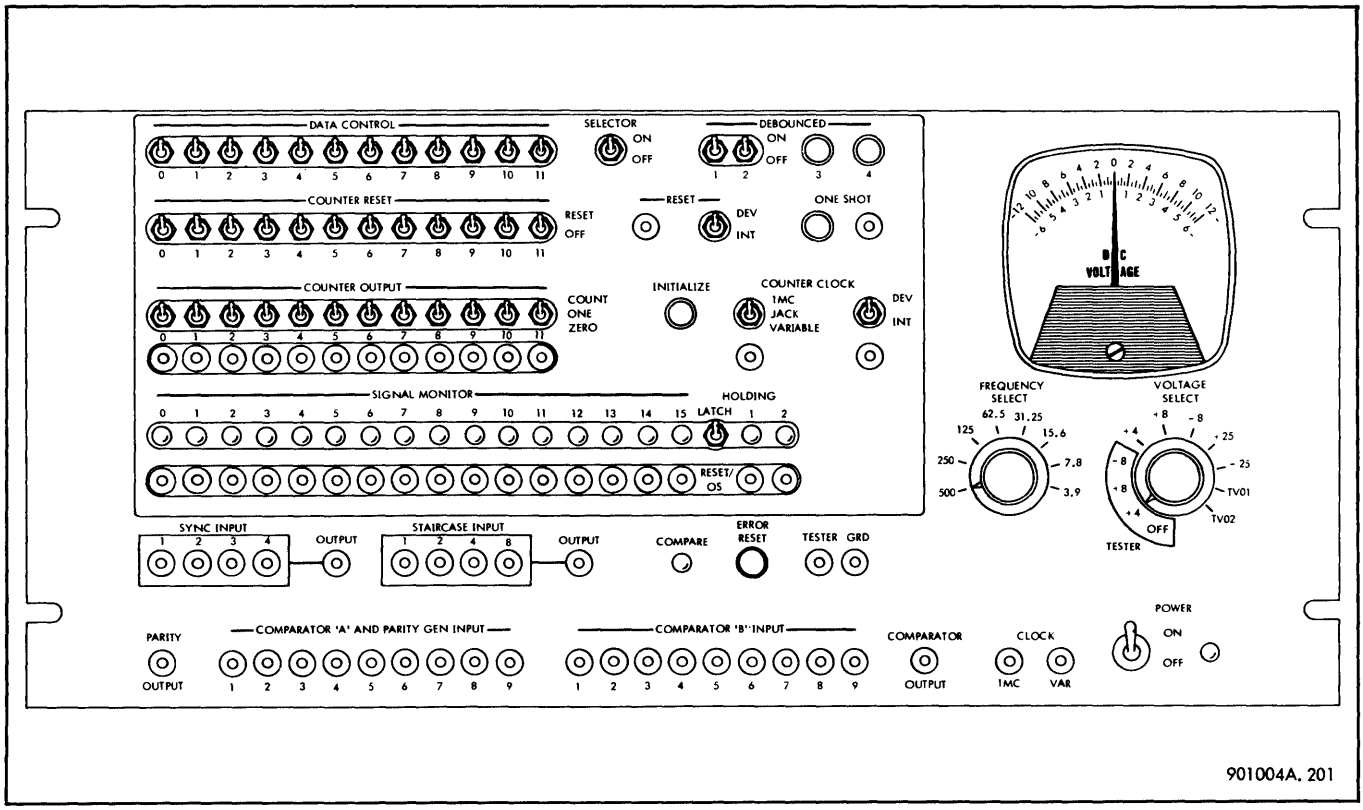


Figure 8-1. Peripheral Equipment Tester Control Panel

CABLE DELAYS

POSITIVE RESPONSE METHOD

I/O transfers between Sigma channels and Sigma peripherals are through a positive response method which eliminates precompensation for cable dispersion. Positive response also increases the reliability of signal timing between subsystems. Transfer periods are subject to two factors:

1. Cable length between the IOP and the connected peripheral.

2. Number of discrete signals of either direction in a given sequence according to the nature of the transfer as listed in table 8-1.

Table 8-1. Byte and Cable Signal Relationship

Data Transfer Quantity in Bytes	Cable Signals per Service Call
1	2
2	6
3	10
4	14

Notes

1. Tabulation is for signals on eight-bit data path cables only. Signals between IOP and CPU, IOP and memory, or priority determination signals are partially or totally overlapped by other logic events causing delay to be configuration-dependent.

2. Other IOP functions such as I/O instructions, order transfers, data chaining, and command chaining involve eight-bit data path signals. These signals appear infrequently in the majority of applications and are therefore not considered here. Xerox provides this data on request.

CABLE DELAY COMPUTATION

In expressing cable delays, cable driver and receiver circuits are considered add-ons to the cable value. Transfer delay and signal dispersion occur once for each discrete signal transmitted from the IOP to the device controller (or inversely). As an example, in a four-byte service call, total cable delay is the sum of 14 cable driver delays, 14 cable receiver delays, and 14 cable transmission delays.

Maximum-minimum delays for a driver are 45 and 10 ns; maximum-minimum delays for a receiver are 10 and 1 ns, respectively.

Figure 8-2 shows maximum and minimum delays in relation to cable length. Total delay for a discrete signal transfer can be expressed as:

$$D = \text{circuit delay} + \text{cable delay}$$
$$= 33 \pm 22 + (1.75 \pm 0.18)L$$

or

$$D = \text{average delay} + \text{dispersion}$$
$$= 33 + 1.75L \pm (22 + 0.18L)$$

where D is in nanoseconds; L is in feet.

Because of the way D is defined, it is not permissible to multiply the cable length (for example, 30 feet) by the number of individual signal trips in a sequence (for example, six for a two-byte service call) to obtain the total cable delay for the applicable service call. Following through, the example would show 180 feet of cable (which is correct) and a delay of 345 (±55) ns (which is incorrect). Determined properly, the delay for a single signal transfer through a 30-foot cable plus the cable circuits must be first ascertained. This value (86 ±29 ns) is then multiplied by six to obtain the correct delay of 516 (±174) ns.

MAXIMUM AND MINIMUM DELAY DEFINITIONS

Maximum delay includes the time needed to obtain a 300-millivolt noise immunity in the cable receiver. Minimum delay excludes noise immunity. Expressed in other terms, maximum delay is the time required to get the signal completely in at the receiving device with cable driver input rise expressed as a function of time. Minimum delay is the time during which a receiving device is safe from the earliest effect of a signal.

CABLE CHARACTERISTICS

Xerox cable characteristics are as follows:

Characteristic impedance:	33 ohms
DC resistance (center conductor):	23 milliohms per foot
DC resistance (shield):	10 milliohms per foot
Inductance:	50 nanohenries per foot
Capacitance:	50 picofarads per foot
Signal delay:	1.4 ns per foot

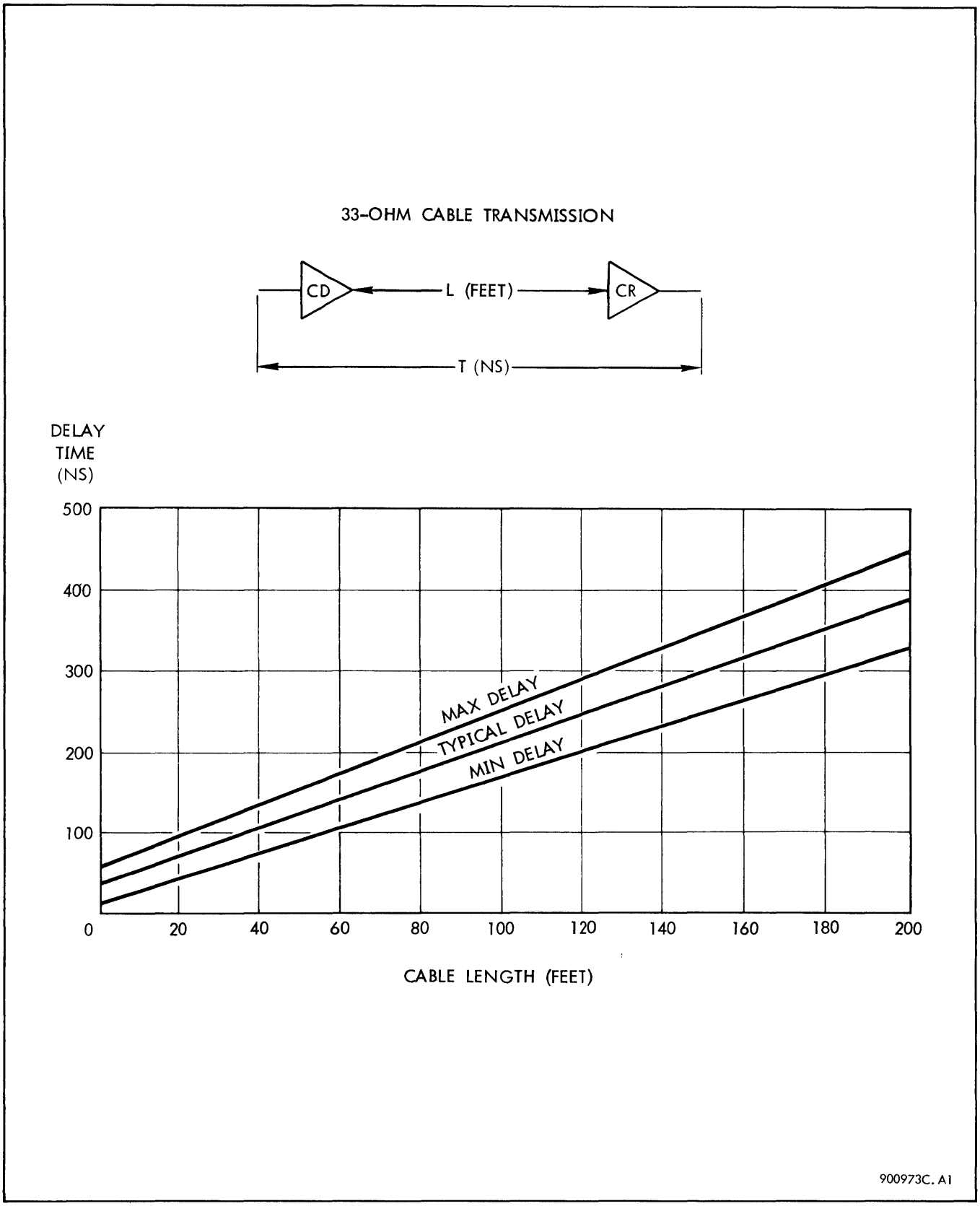


Figure 8-2. Delay as a Function of Cable Length

SECTION IX

FLOW DIAGRAMS

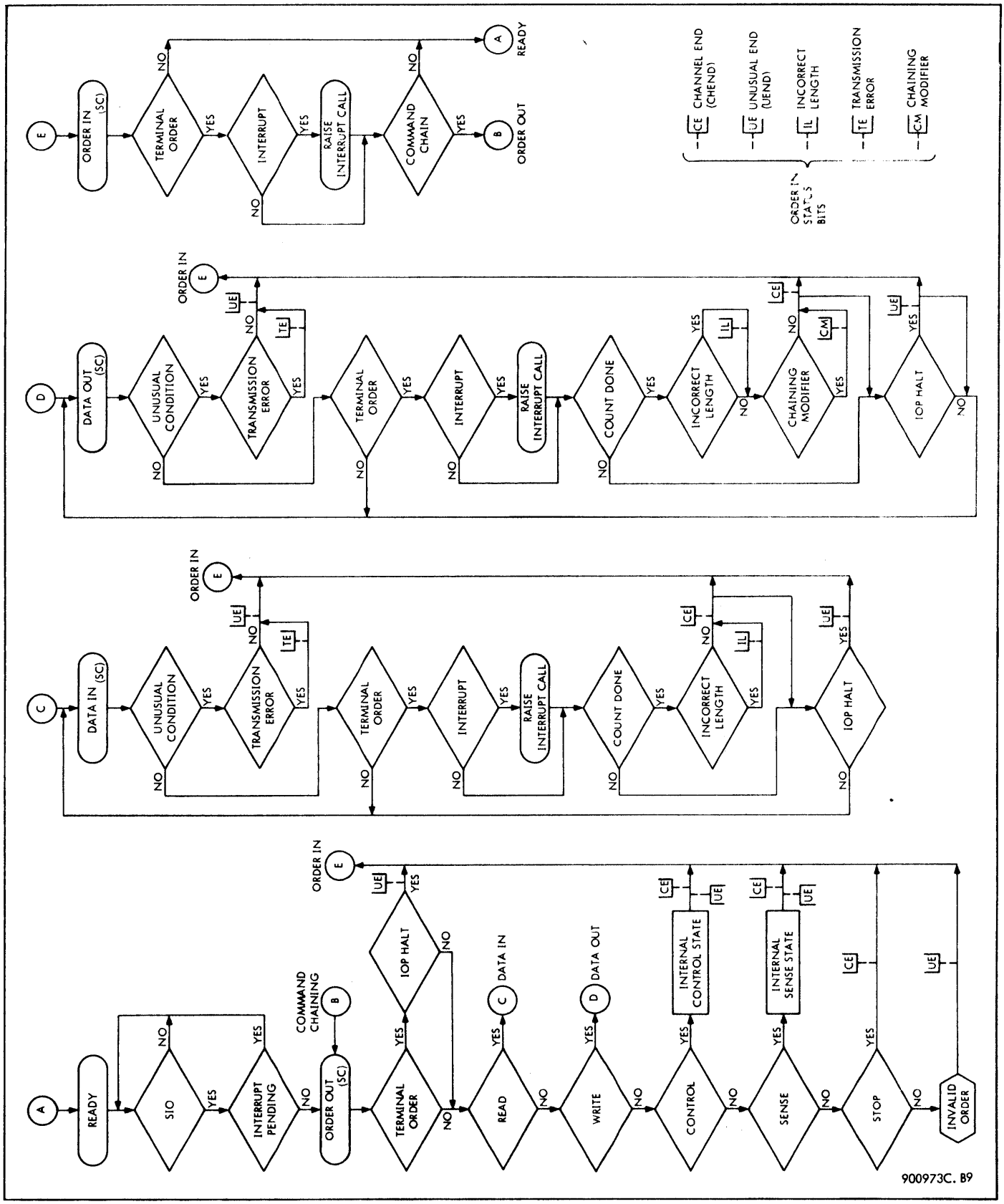
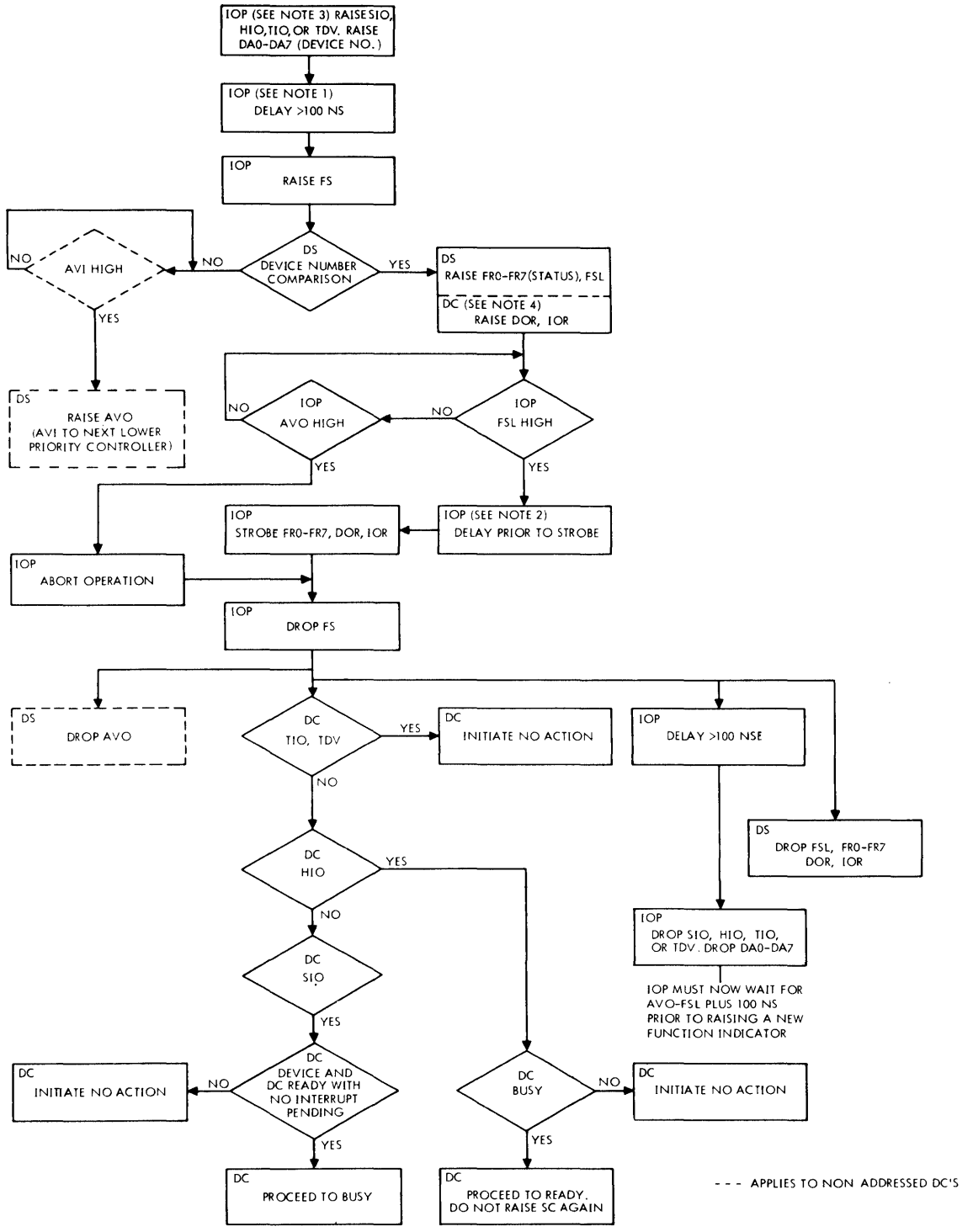


Figure 9-1. Eight-Bit I/O Operational State, Flow Diagram



NOTES:

1. FOR SIGNALS ARRIVING FROM IOP, ALL TIMING IS MEASURED AT OUTPUT OF DEVICE CONTROLLER CABLE RECEIVER
2. BEFORE STROBING INPUT SIGNAL LINES AFTER RECEIVING FSL OR RS SIGNAL, IOP MUST COMPENSATE FOR WORST-CASE SIGNAL DISPERSION CAUSED BY CABLES, IOP RECEIVERS, IOP LOGIC, PLUS 60 NS
3. ONLY ONE FUNCTION INDICATOR (SIO, HIO, TIO, TDV, AIO, OR ASC) CAN BE HIGH AT ANY TIME.
4. DOR AND IOR REPRESENT CONDITION CODES NCC1 AND NCC2, RESPECTIVELY, AT THIS TIME. RAISE IOR (NCC2) ONLY IF APPLICABLE
5. AVI TO THE HIGHEST PRIORITY DEVICE CONTROLLER IS ALWAYS HIGH

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Figure 9-2. SIO, HIO, TIO, and TDV, Flow Diagram

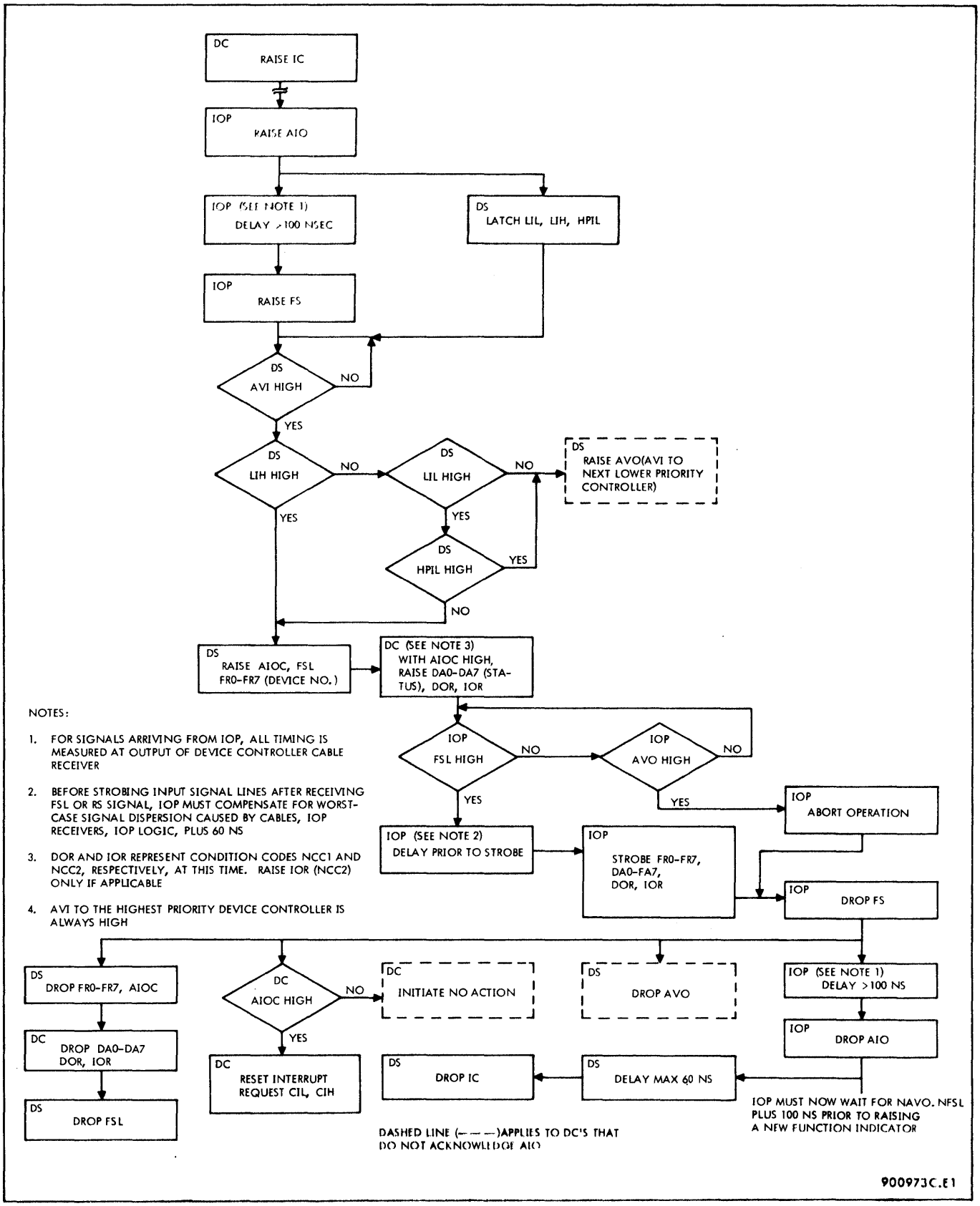


Figure 9-3. AIO, Flow Diagram

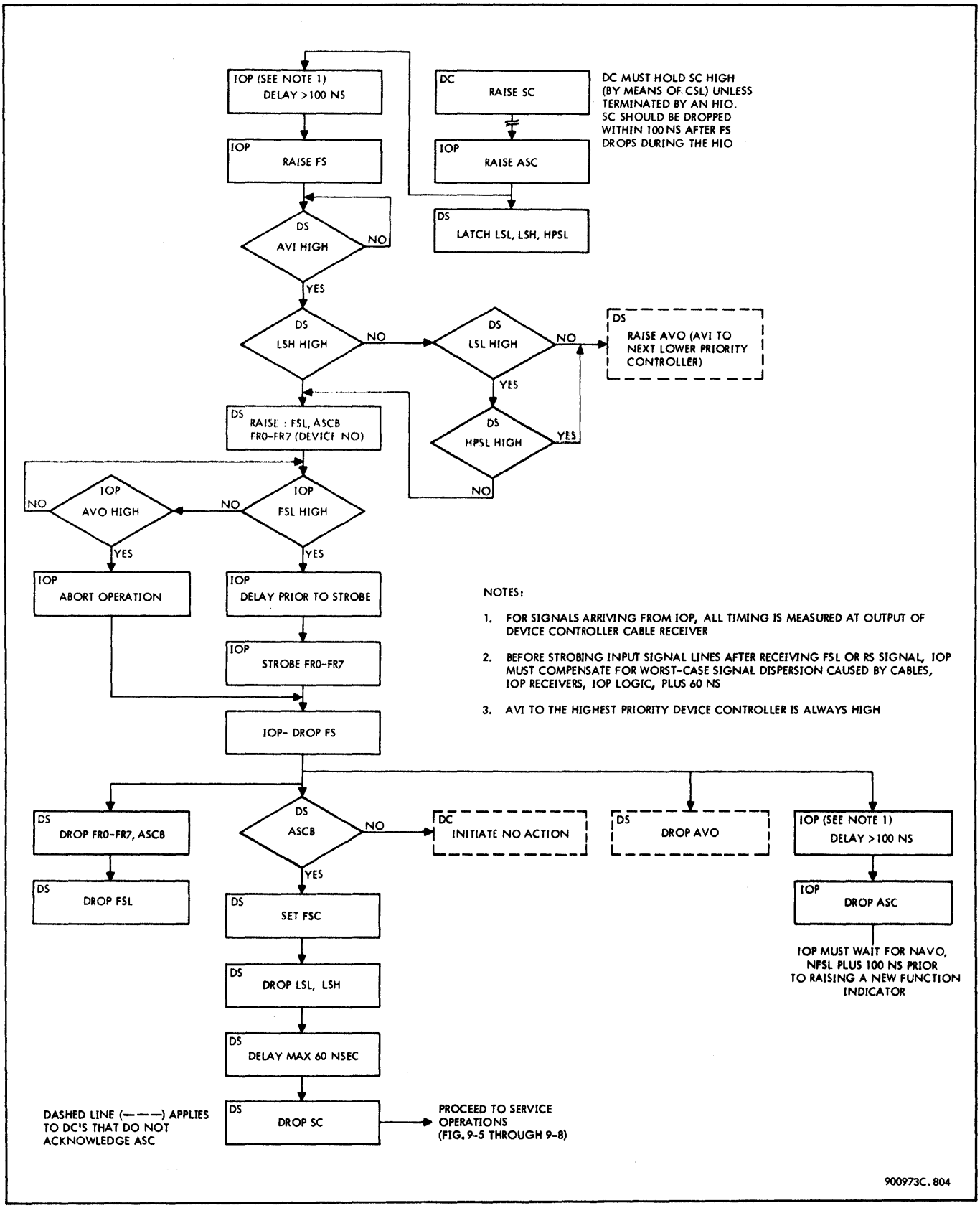


Figure 9-4. ASC (Prior to Service Connection), Flow Diagram

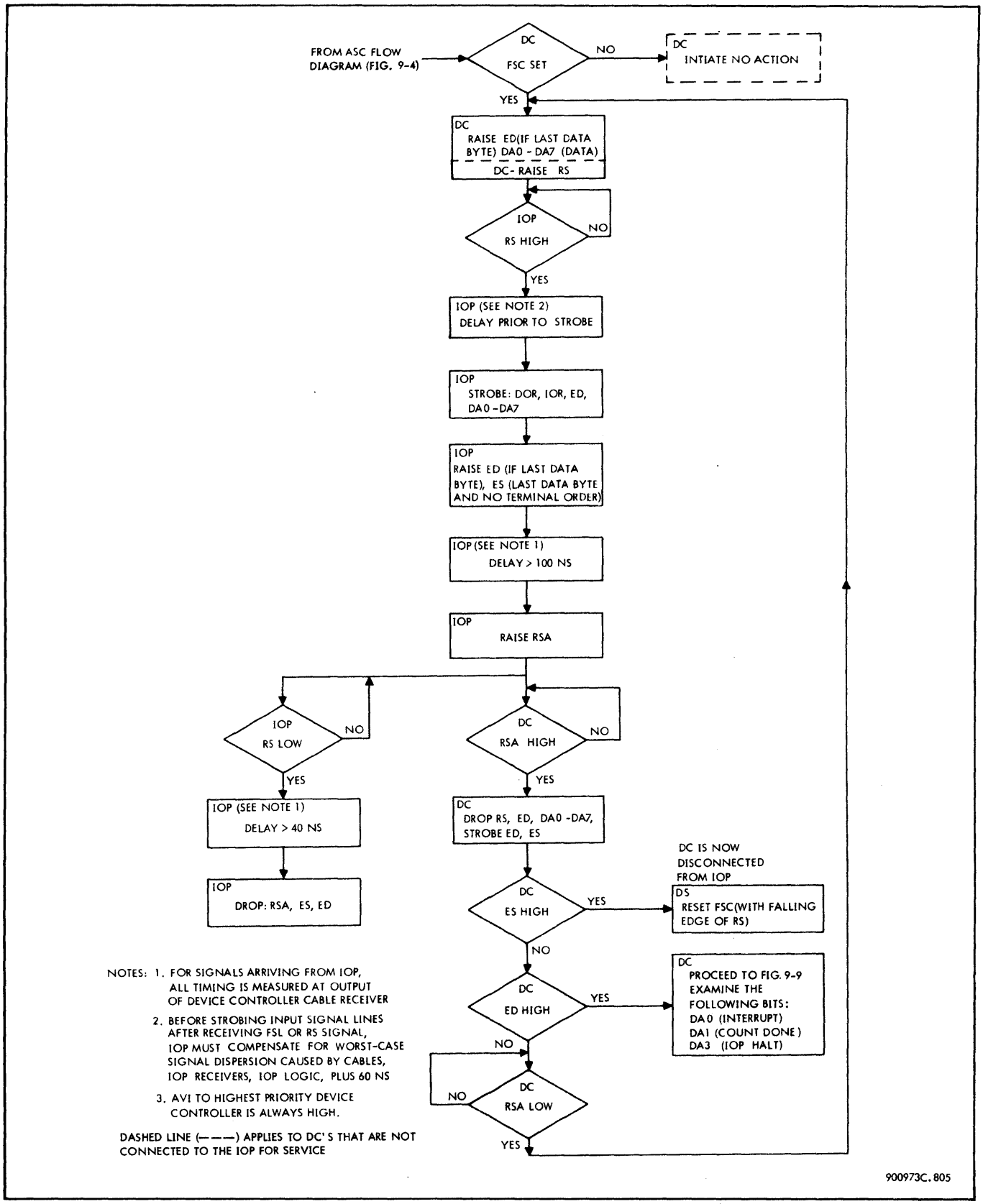


Figure 9-5. Service – Data Input, Flow Diagram

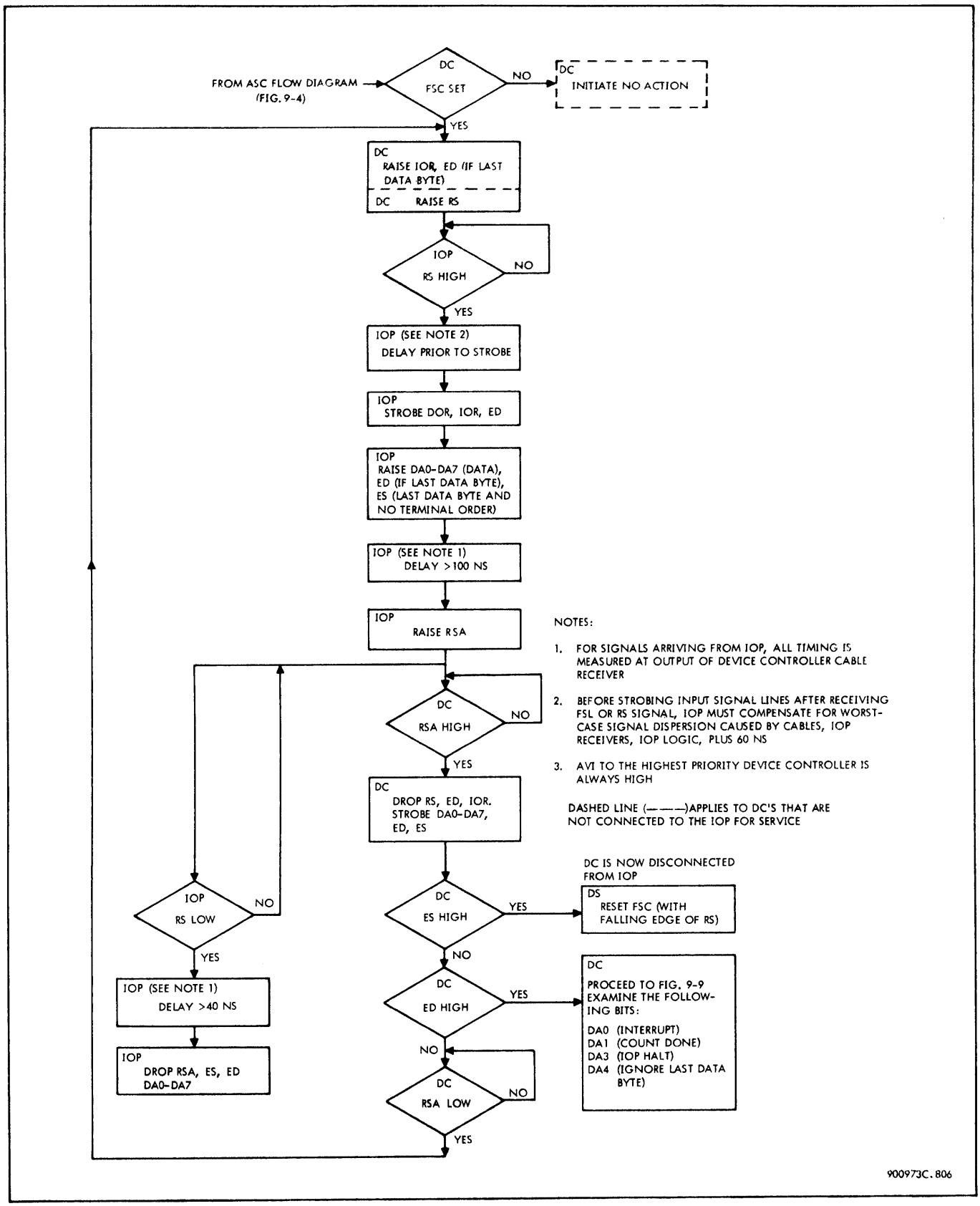


Figure 9-6. Service – Data Output, Flow Diagram

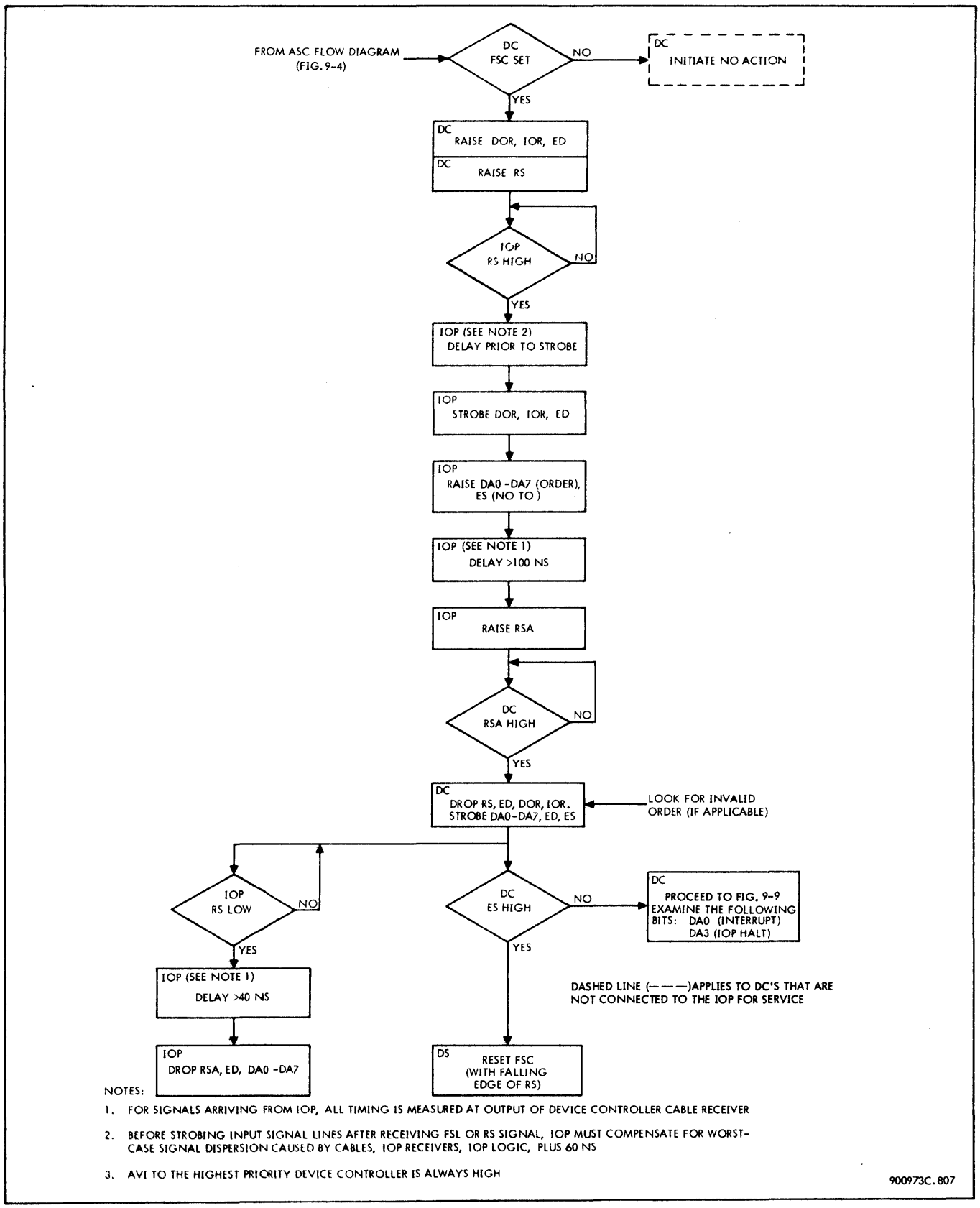


Figure 9-7. Service – Order Output, Flow Diagram

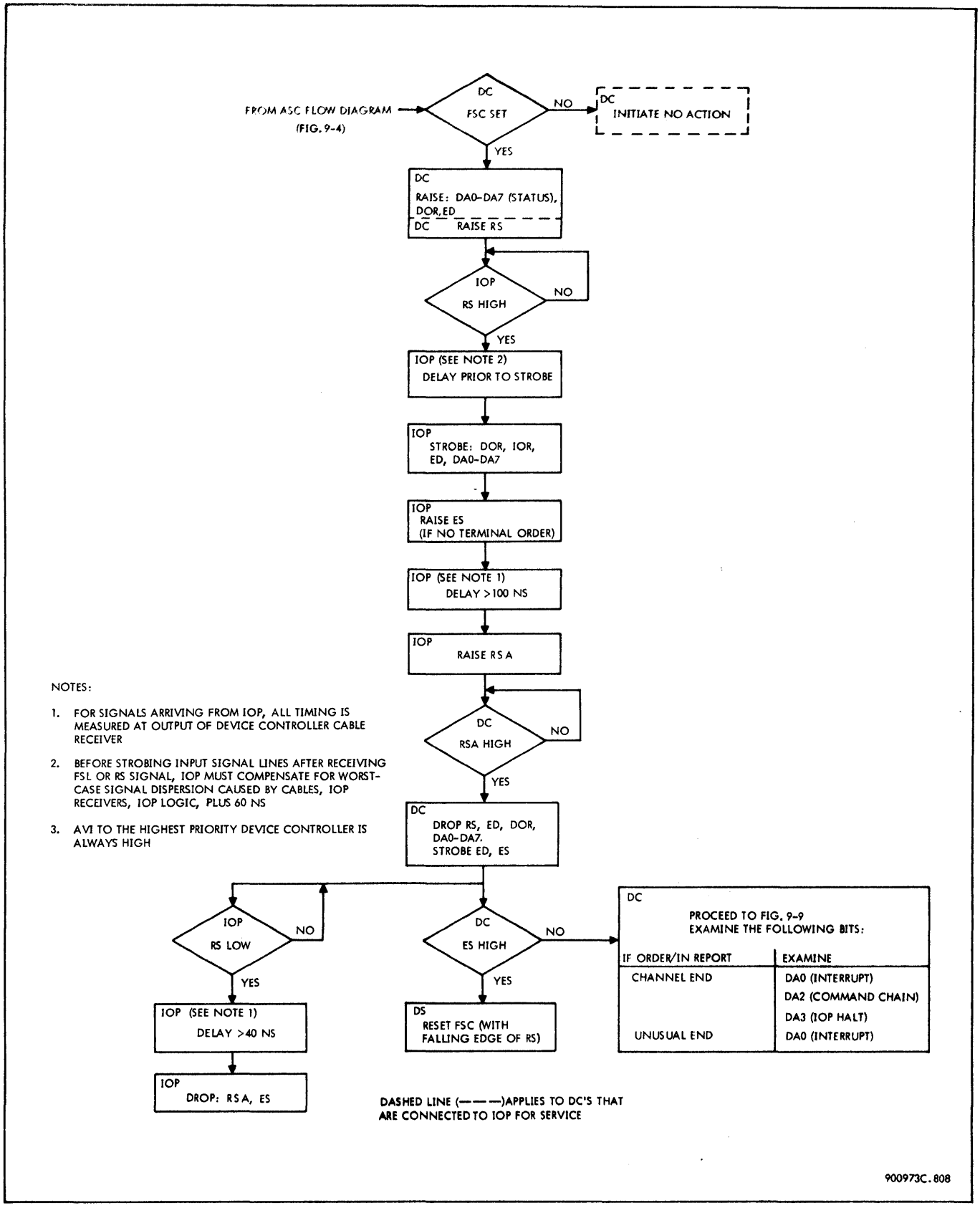
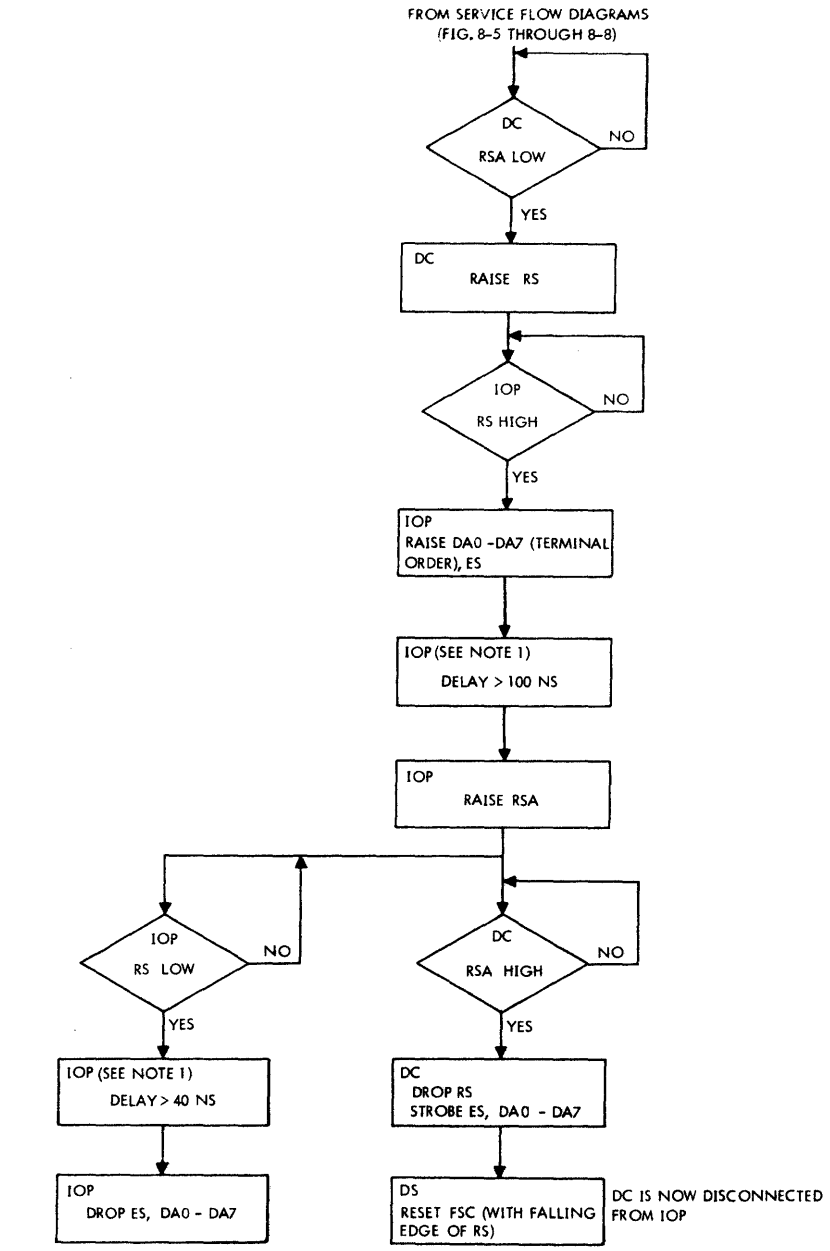


Figure 9-8. Service – Order Input, Flow Diagram



NOTES: 1. FOR SIGNALS ARRIVING FROM IOP, ALL TIMING IS MEASURED AT OUTPUT OF DEVICE CONTOLLER CABLE RECEIVER

2. AVI TO THE HIGHEST PRIORITY DEVICE CONTROLLER IS ALWAYS HIGH

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Figure 9-9. Terminal Order, Flow Diagram

SECTION X

SIGNAL DICTIONARY

Section X includes an alphabetically arranged listing of signals included in the IDM. (Refer to table 10-1.) When the letter N preceding a signal is used in this IDM, it represents an inverse or false condition. The letters D and R appended to a signal indicate a driver input and a receiver output, respectively.

DS loads, where stated, indicate the number of unit loads that the device subcontroller requires from the signal. One unit load equals 3.8 milliamperes. To determine how many loads may be used by the DC logic, subtract DS loads from 16. (The letters DS indicate device subcontroller.)

Table 10-1. Signal Logic Dictionary

Signal	Interface	Definition
A		
A00-A15	DIO	CPU-driven address lines
ABO	32-bit memory	Abort. Signal that overrides write operation and prevents changing of memory location contents
AH	16-bit and 32-bit memory	Address here. Signal from memory indicating that current address falls within range of a particular memory block
AIO	IOP	Acknowledge interrupts. IOP function indicator line
AIOC	IOP	Defines period when device controller (DC) supplies interrupt status, condition codes, and device number to IOP. Can be used at FSR trailing edge to reset CIL and CIH. Four device subcontroller (DS) loads
AIOM	IOP	Indication that an AIO will be accepted when AVIR is received. Four DS loads
AR	32-bit memory	Address release. Indication that address, memory request, and write byte lines can be dropped
ASC	IOP	Acknowledge service call. An IOP function indicator line
ASCB	IOP	Indication that service-connect flip-flop FSC will set when FSR is dropped. Four DS loads
AVI	IOP	Available input priority signal
AVO	IOP	Available output priority signal
B		
BSYC	IOP	Subcontroller logic signal indicating that a given device has highest priority and is acknowledging either service or an interrupt. Indication that either AIO or ASC is accepted. Twelve DS loads
C		
CC	IOP	Command chaining flag
CC1-CC4	IOP	Condition code bits 1 through 4
CC3D-CC4D	DIO	Lines used by addressed external device to send status
CHEND	IOP	Channel end. Bit 3 in an OIN indicating completed data transmission
CIH	IOP	High priority interrupt request from DC to DS (must be accompanied by CIL)

(Continued)

Table 10-1. Signal Logic Dictionary (Cont.)

Signal	Interface	Definition
CIL	IOP	Interrupt request from DC to DS. Two DS loads
CL1	DIO	1.024 MHz-clock line (500 ns high, 500 ns low)
CM	IOP	Chaining modifier. Bit 2 in OIN service cycle specification
CP1-CP4	Interrupt	Sigma 2 or 3 input lines for external real-time clocks
CSH	IOP	High priority service request from DC to DS (must be accompanied by CSL)
CSL	IOP	Service request from DC to DS. Two DS loads
CSL1	IOP	Input to signal CSL; prevents DC logic switching transients from appearing on SC line. Two DS loads
D		
D00-D15	16-bit memory	Data bits 00-15 from OR to memory
D16	16-bit memory	Odd parity bit from OR to memory
DA0-DA7	IOP	Bidirectional data lines
DAP	IOP	Data parity line
DB00-DB31	DIO	Data lines for Sigma 5 or 7
DB16-DB31	DIO	Data lines for Sigma 2 or 3
DCA	IOP	Device controller address. Nine DS loads
DE	IOP	Device end. A DC-independent operation (such as rewind) by a device when the responsible DC may be busy with another device
DG	32-bit memory	Data gate. Signal for gating data into receiving register for read
DIN	IOP	Data in. A service cycle for data transfer from DC to memory
DM	16-bit memory	Data to memory. Signal that controls (with W0 and W1) gating of data into memory data register
DOR	IOP	Data order line. If DOR is true, information being transferred is an order. If DOR is false, information being transferred is data. DOR is part of condition code during an instruction
DOUT	IOP	Data out. A service cycle for data transfer from memory to DC
DR	32-bit memory	Data release signal generated by memory. Pulse signifies that data lines can be dropped for a write operation
DS	16-bit memory	Data to source signal. Indication that data from memory is stable
DX4	IOP	Four-byte interface request line
E		
ED	IOP	Bidirectional end data line that indicates transmission of last data or order byte
EDR	32-bit memory	Early data release. Pulse in read mode that clears receiving register

(Continued)

Table 10-1. Signal Logic Dictionary (Cont.)

Signal	Interface	Definition
EDX4	IOP	Signal that enables four-byte interface
ER1-ER4	Interrupt	Sigma 2 or 3 input request lines for the four integral priority interrupt levels
ERS1-ERS4	Interrupt	Sigma 2 or 3 response lines for the four integral priority interrupt levels
ES	IOP	End service line that indicates transmission of last byte of service
F		
FAST	IOP	Fast device controller line
FR0-FR7	IOP	Function response lines
FS	IOP	Function strobe. Indication that function indicator lines are stable
FSA	DIO	Function strobe acknowledge. Response of external unit to an FS from the CPU
FSC	IOP	Service-connect flip-flop set by DS. When true, indicates that DC is connected for service. Eight unit loads
FSD	IOP	Function strobe delayed (as required by controller). DC must return this signal to DS when FSR occurs. Five DS loads
FSL	IOP	Function strobe leading acknowledge. Indication that FR lines, condition code lines, and so forth, can be strobed by IOP
H		
HIO	IOP	Halt input/output. IOP function indicator line
HPI	IOP	High priority interrupt line
HPIL	IOP	Latch circuit that holds HPI condition during AIO. Three unit loads
HPS	IOP	High priority service line
HPSL	IOP	Latch circuit that holds HPSL condition during ASC. Three unit loads
HTE	IOP	Halt on transmission error flag
I		
IC	IOP	Interrupt call line
IL	IOP	Incorrect length. Bit 1 in an OIN; indication that error is in record length
IN00-IN15	Interrupt	User request for service lines. IN00 is highest priority interrupt level
INC	IOP	Signal that inhibits new service or interrupts during power on-power off
INI	IOP	Signal to initialize after power failure and clamp inputs to cable drivers during power on-power off sequencing (relay contact). Also, indication to bypass AVI signal when power is removed from DC (relay contact)
IOR	IOP	Input/output request. Input/output line during service (where high equals output) and condition code during function acknowledgements. If true, information transfer is from memory to device. If false, information transfer is from device to memory
IR	Interrupt	Interrupt request

(Continued)

Table 10-1. Signal Logic Dictionary (Cont.)

Signal	Interface	Definition
L		
L15-L31	32-bit memory	Address signals
LIH	IOP	Latch interrupt high. Latch circuit that holds CIH condition during AIO
LIL	IOP	Latch interrupt low. Latch circuit that holds CIL condition during AIO
LSH	IOP	Latch service high. Latch circuit that holds CSH condition during ASC
LSL	IOP	Latch service low. Latch circuit that holds CSL condition during ASC. Six unit loads each for LIH, LIL, LSH, and LSL
M		
M00-M31	32-bit memory	Data lines to or from memory
MQ	16-bit and 32-bit memory	Memory request. Signal that initiates request for memory cycle
MW0-MW3	32-bit memory	Write byte signals indicating which of four bytes are to be written in memory
O		
OIN	IOP	Order in. A service cycle for control information transfer from DC to IOP
OOUT	IOP	Order out. A service cycle for control information transfer from IOP to DC
P		
PC	IOP	Parity check line
PE	32-bit memory	Parity error. Signal to indicate result of parity check
POK	32-bit memory	Parity OK. Signal to indicate result of parity check
PT18	IOP	Signal from DC to open a ground return line prior to any voltages decaying below a safe limit
R		
RE00-RE15	Interrupt	Response to user request for service lines. (See IN00-IN15)
REL	16-bit memory	Release signal from memory that indicates cycle has started for current request
RES	16-bit memory	Reset signal to memory timing and control logic
RS	IOP	Request strobe line signal indicating stable lines
RSA	IOP	Request strobe acknowledge line; indicates RS can be dropped
RSAR	IOP	RSA receiver output. Four unit loads
RSARC	IOP	Signal that repeats RSAR except at end service when RSARC latches until FSC resets. Two unit loads
RST	DIO	Input/output reset line. DC must initialize all circuits when RST is high

(Continued)

Table 10-1. Signal Logic Dictionary (Cont.)

Signal	Interface	Definition
RST	Interrupt	General reset signal
RWD	DIO	Selection line driven by CPU to enable external devices to distinguish between a WD and an RD instruction. Write when true
S		
S00-S15	16-bit memory	Address bits 00-15 to memory
SC	IOP	Service call line
SIO	IOP	Start input/output. IOP function indicator line
SRA	32-bit memory	Second request allowed. Pulse to initiate next memory request
SWA4C-SWA7C	IOP	Least significant device number bits supplied by DC during AIO and ASC
SWA0-SWA7	IOP	Toggle switch outputs for channel address manual selection
T		
TDV	IOP	Test device. IOP function indicator line
TE	IOP	Transmission error. Bit 0 in an OIN
TIO	IOP	Test input/output. IOP function indicator line
TO	IOP	Terminal order. A data transmission from an IOP to a DC that concludes data exchanges
TSH	IOP	Signal that defines DCA (TIOR + SIOR + HIOR). Ten unit loads
TTSH	IOP	Signal derived from function indicators for SIO, HIO, TIO, and TDV. Four unit loads
U		
UEND	IOP	Unusual end. DC unusual terminal signal. Bit 4 in an OIN
W		
W0	16-bit memory	Write byte 0. Write left byte in memory
W1	16-bit memory	Write byte 1. Write right byte in memory
WADR	IOP	Word-aligned data-required line
Z		
ZBC1	IOP	Zero-byte count interrupt lines

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