APPLICATION	
NEXT ASSY	USED ON
FINAL	GRAPHIC 7

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
-	RELEASED FOR DEVELOPMENT	11/15/77	O.OT
A	REV PER ENG	1/22/92	CMP

REVISION STATUS OF SHEETS																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
REVISION	A	-	-	A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
.XX DECIMAL ± .XXX DECIMAL ±
ANGLES ± SURFACE QUALITY √ MAX
INTERPRET DWG PER 815002

DEVELOPMENT
CHANGE BY REV.

MFG N. Koch 8-2-78

CONT NO.

DRFTG: DR M. DELIZZA DATE 10NOV 77; APPD; CHK

ENGRG: DEV J. O'Toole 15 Nov. 77; E/M R Batchelder 8/2/78; PROJ J Keller 8/7/78

SANDERS ASSOCIATES, INC NASHUA, NEW HAMPSHIRE

INTERFACE CONTROL DOCUMENT
SEL HSD-9132/GRAPHIC 7
PARALLEL INTERFACE (MODEL 5716)

SIZE	CODE IDENT NO.	DWG NO.
A	94117	1089717

SCALE

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OP—330 REV H

DO NOT SCALE PRINT

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1.0 INTRODUCTION

1.1 General

This Interface Control Document describes the interface signals, protocol, and cabling which is utilized as the communications link between a Systems Engineering Labs (SEL) Series - 32 computer HSD 9132 Interface and a Sanders Associates, Inc. (S/A) GRAPHIC 7 Display System

The system allows two-way, high speed, parallel communication between the display system and the host computer.

2.0 REFERENCE DOCUMENTS

2.1 Sanders Associates, Inc. Documents

1. Logic Diagram, S/A Parallel Interface, SEL-HSD9132/ GRAPHIC 7 Drawing No. 1089703.
2. Graphic 7 Technical Description - GA-76-165 (Rev. B)
3. Software Test Requirement Specification - 1088693

2.2 SEL Documents

1. Systems Engineering Labs, Inc. Technical Manuals, Volumes 1, 2, and 3. HSD 9132
   Publication No. 325-329132-000 1977

3.0 HARDWARE INTERFACE CHARACTERISTICS

3.1 Interface Signal Definition

The following is a list of the signals, and their definitions which will provide the interface communications between the SEL/HSD-9132 and the GRAPHIC 7 parallel interface board.

It may be noted that only 16 bits, of the 32 bit data bus, will be utilized, (namely: DATØØ-15).

1. Bidirectional Data Bus (DATØØ-15)

   This 16-bit bidirectional bus carries data, command, status, and address information.

2. Input Data Ready (IDR)

   This signal is generated by the GRAPHIC 7 interface, and indicates that the input data is stable. This signal remains true until the Input Acknowledge signal is returned by the HSD-9132.

3. Input Acknowledge (IA)

   This signal, generated by the HSD-9132, is used to acknowledge the receipt of the input data. This signal remains true until the IDR signal goes false.

4. Output Data Ready (ODR)

   This signal is generated by the HSD-9132, in conjunction with output data information. This signal remains true until the Output Acknowledge signal is returned by the GRAPHIC 7 interface.

5. Output Acknowledge (OA)

This signal is generated by the GRAPHIC 7 interface, and is used to acknowledge the receipt of the output data. This signal remains true until the ODR signal goes false.

6. External Function (EF)

This signal is generated by the HSD-9132; and, when true, indicates that the associated host computer (SEL-32/55) has placed a command (e.g. Initialize, request status, or input/output) onto the data lines.

7. External Function Acknowledge (EFA)

This signal is generated by the GRAPHIC 7 interface, and is used to acknowledge the receipt of the EF signal. The EFA signal remains true until the EF signal goes false.

8. Device Present (DP)

This signal is a level which is generated by the GRAPHIC 7 interface. This signal is normally true, so as to enable communication with the host computer.

As described in Section 3.2 (Interface Operation) the Device Present signal goes false only when a computer request for interface control is being denied. In this case, the Device Present signal remains false until the EF signal goes false.

9. Input Status Ready (ISR)

This signal is generated by the GRAPHIC 7 interface and, when true, indicates that the GRAPHIC 7 system has data which should be read by the host computer. That is, the host computer should initiate an Input command sequence. It should be noted that the host (SEL) computer must first issue a "Device Status Request" command in order for the GRAPHIC 7 interface to generate the ISR signal.

The ISR signal remains true until the receipt of either the ISA signal or the IOR signal.

10. Input Status Acknowledge (ISA)

This signal is generated by the HSD 9132, and is used to acknowledge the receipt of the ISR signal. The ISA signal remains true until the ISR signal goes false.

11. Last Word Flag (LWF)

This signal accompanies the last ODR signal in the output mode or the last IA signal in the input mode. This is a flag from the HSD 9132 to the GRAPHIC 7 interface signifying End of Block.

Receipt of the LWF signal will cause the GRAPHIC 7 interface to terminate the transfer.

12. I/O Reset (IOR)

This signal is generated by the HSD9132, and is used by the GRAPHIC 7 interface to reset a previously received "Device Status Request" command.

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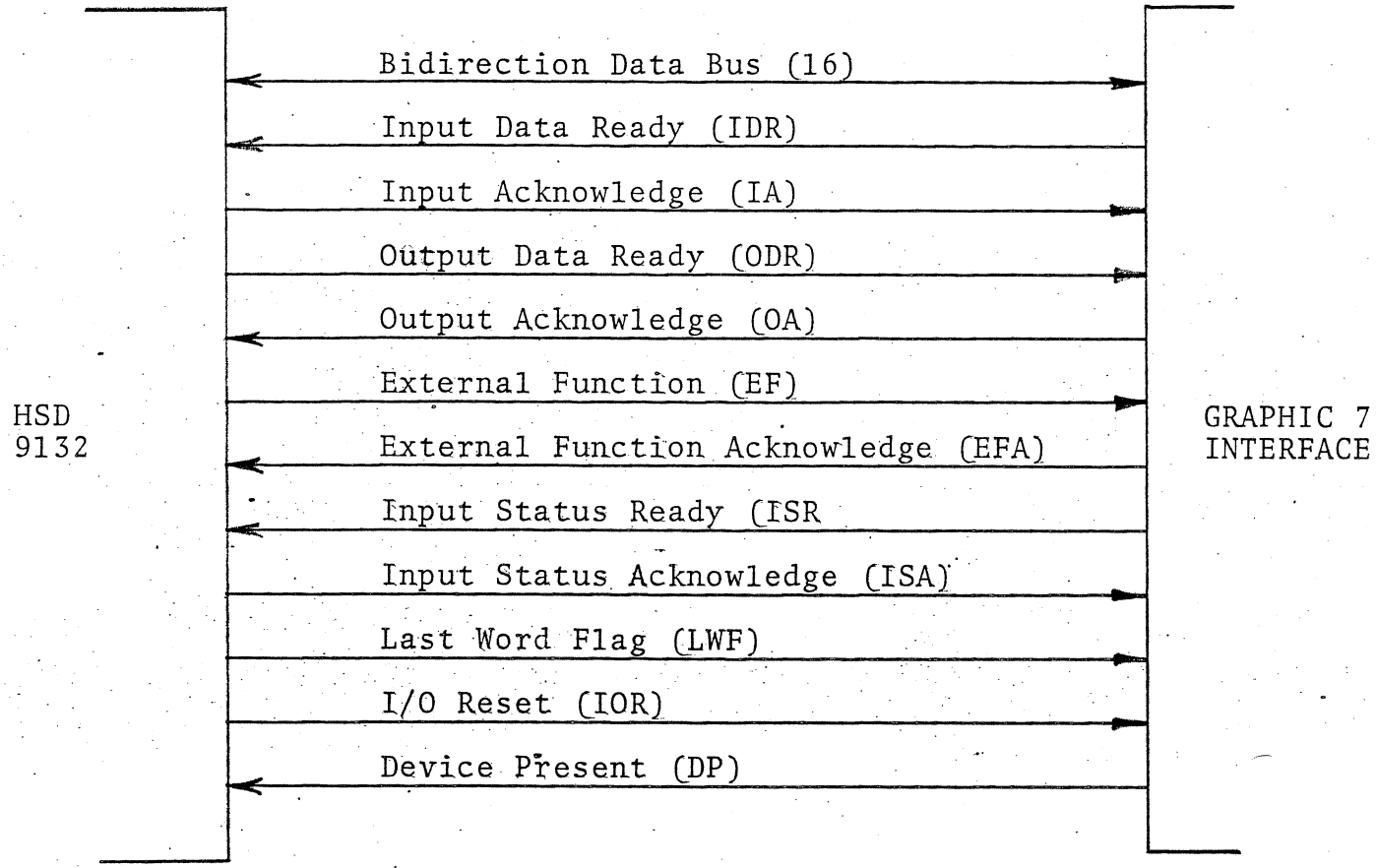

HSD-9132/GRAPHIC 7

INTERFACE SIGNALS

FIGURE I

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3.2 Interface Operation

3.2.1 General

In order to request interface control, the requesting computer must issue an I/O command to the GRAPHIC 7; and, except for the "Device Status Request" command and the "Initialize" command, all commands are considered (by the GRAPHIC 7 interface) to be I/O commands. Upon receipt of the EF signal, which accompanies each I/O command, the GRAPHIC 7 interface will respond with the EFA signal.

The following three (3) modes of operation (Modes A thru C) describe in more detail the sequences of events:

3.2.2 Mode A, Host to GRAPHIC 7 (G-7) Outputting Data

1. Host sets up for sending data; and is enabled for interrupt in case of an error (and maybe an EOB).
2. The above causes an External Function (EF) to be generated; and the G-7 acknowledges the EF and also, acknowledges each data word.
3. When the Last Word Flag (LWF) is received, the G-7 terminates the transfer.

3.2.3 Mode B, G-7 to Host

Device Status Request Command

1. Host sets up for requesting Device Status, and enabled for interrupting on EOB.
2. The G-7 gets an EF with the Device Status bit set in the data word (bit #2).
3. The G-7 acknowledges the EF.
4. If the G-7 has data to be sent, it will raise the ISR signal. If not, the G-7 will wait until input data is available.
5. Host will acknowledge the ISR, and application program gets an interrupt.
6. Last Word Flag will be generated.

3.2.4 Mode C, G-7 to Host

Inputting Data

1. Host sets up for receiving data; and is enabled for interrupt in case of an error (and maybe an EOB).
2. That generates an EF to the G-7; and the G-7 acknowledges the EF and issues an IDR.
3. When LWF is received, the G-7 terminates the transfer.

3.3 Electrical Characteristics

3.3.1 Signal Levels

At the interface, a logic ONE is defined as being between zero volts and +1.5 volts; and a logic ZERO is defined as being +3.2 volts and +5.0 volts.

These seemingly pseudo TTL levels exist because of the driver-receiver circuit (SN75138, open-collector quad bus transceivers).

3.3.2 Interface Connectors

1. The SEL-HSD9132 end of the interface cable assembly utilized two (2) connectors of the following type:
   AMP Mod-4, Body: 2-86177-1 Contacts: 86016-1
   These two (2) connectors are referred to as "P1" and "P4" in Figure 2.
2. The GRAPHIC 7 end of the interface cable assembly utilizes two (2) connectors of one of the following types:
   Berg: 65043-012 or DDMA-50S.
   Referred to as "P2" and "P3" in Figure 2.

3.3.3 Interface Cabling

The interface cable assembly is 30 feet in length, and is made up of 24 gauge twisted-pair wire.

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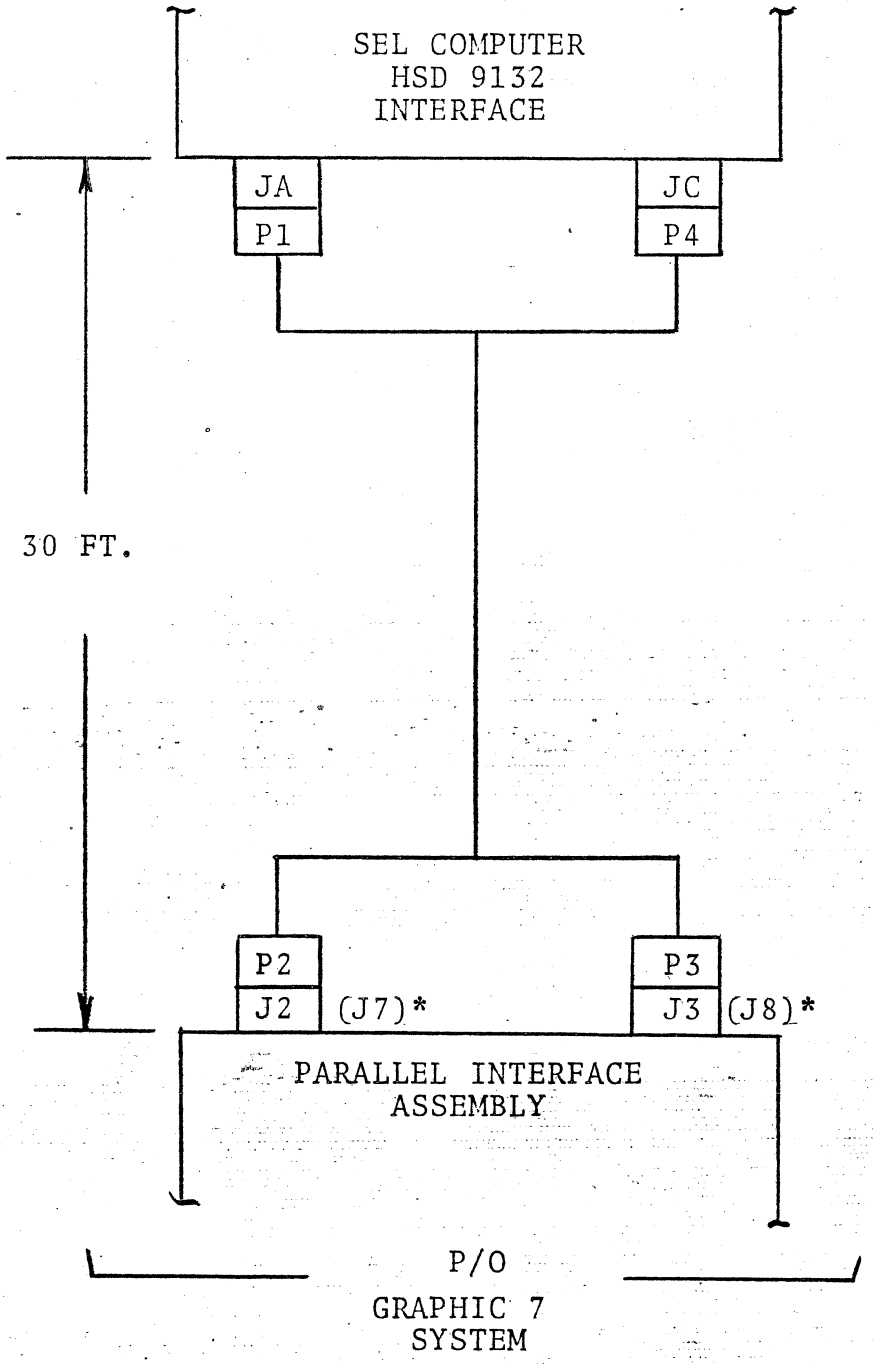

FIGURE 2 - INTERFACE CABLING

*If System Interconnect Panel is installed.

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4.0 SOFTWARE CHARACTERISTICS

4.1 Host/Graphic 7 Communications

All communications between the host computer and the Graphic 7 can be handled by GCP (Graphics Control Program) or by down-loaded user-generated software. Transmissions in either direction are referred to as messages. Each message begins with a command header that contains two ASCII characters to define the message type. The header is then followed by as many 16-bit words as are required to transmit the associated data. No translation of the data words is necessary and no end-of-message indicator is required.

GCP supports nineteen (19) different types of message across the interface that are divided into two groups - fundamental and additional messages. Table 4-1 summarizes the interface messages of the Graphic 7, both fundamental and additional types.

However, as noted above, additional messages forming the user's own communications software can be written and used as per the interface protocol described herein.

4.2 GCP Fundamental Messages

These messages, which represent a nucleus of standard GRAPHIC 7 functions allow the user to achieve an interactive graphic capability. These messages provide a means to display a graphic image, and allow (1) the image to be rapidly transformed and (2) system identification of particular items within the image in response to operator actions.

The format for these messages is as shown by the example on the following page.

Each message consists of a command word followed by a number of argument words. The 16-bit command word is always formed from two 7-bit ASCII letters.

Example: Command Word: MU

	15	14 ... 8	7	6 ... 0	
MSB	0	ASCII M	0	ASCII U	LSB

The argument words contain either auxiliary data for the command word or display data.

4.3 GCP Additional Messages

Additional GCP GRAPHIC 7 messages give the user detailed control and access to all of the display terminal registers and parameters. These messages are available, ready for use, in the basic GRAPHIC 7 terminal controller. See Table 4-1.

The additional message format is as per Section 4.2. Additional detail concerning all standard Host/Graphic 7 messages may be found in the Programmer's Reference Manual.

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TABLE 4-1

HOST/GRAPHIC 7 MESSAGE SUMMARY

Fundamental Messages			
Host-to-GRAPHIC 7		GRAPHIC 7-to-Host	
Initialize	(IZ)	Keyboard	(KY)
Memory Update	(MU)	Lightpen	(PN)
Start Picture	(SP)	Function Key	(RK)
Halt Picture	(HP)		
Additional Messages			
Host-to-GRAPHIC 7		GRAPHIC 7-to-Host	
Continue Picture	(KP)	Keyboard #2	(KT)*
Selective Update	(SU)	Lightpen #2	(PT)*
Give Image	(GI)	Return Image	(RI)
Give Register	(GR)	Return Register	(RR)
Selective Interrupt Cont	(IK)	Scratchpad Ready	(XR)(XT)*
Light Function Keys	(LK(IT)*	Return PED	(RP)(RW)*
Initialize PED ①	(IP)(IT)*	Lightpen Switch	(SW)(ST)*
Give PED	(GP)(GT)*	Display Halt Interrupt	(HI)
Initialize Scratchpad	(ZR)(ZT)*	Display X-Y Overflow	(XI)
Transfer Control	(TK)	Error Condition	(XX)
No Operation	(NO)	Variable Length Block	(VL)
		Function Key #2	(RL)*

*These messages pertain to the second device of each type.

① PED - Positional Entry Device (i.e., trackball, joystick)

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APPENDIX A
Parallel Interface Register Descriptions

A-1 General

Tables A-1 and A-2 list register and interrupt trap addresses in the Parallel Interface. In the Address listings, the 2nd, 3rd and 4th card columns list the preassigned addresses of the registers if additional optional Interface Cards are used.

Tables A-3 through A-7 list and describe the significance of individual bits in the Parallel Interface registers.

TABLE A-1
PARALLEL INTERFACE REGISTER ADDRESSES

	Address			
Register	1st Card	2nd Card	3rd Card	4th Card
Word Count (WCR)	172410	172430	172450	172470
Memory address (MAR)	172412	172432	172452	172472
Status (STR)	172414	172434	172454	172474
Data (IDR & ODR)	172416	172436	172456	172476

TABLE A-2

PARALLEL INTERFACE INTERRUPT TRAP ADDRESSES

	Trap Address			
Interrupt	1st Card	2nd Card	3rd Card	4th Card
Input	120	400	420	440
Output	124	404	424	444
Attention	130	410	430	450

TABLE A-3

WORD COUNT REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Word Count	Program read/write, cleared by bus reset. To initiate a DMA mode, the program writes the two's complement of the number of words to be transferred between memory and the Host. Each time the Interface completes a DMA word transfer, the word count is incremented by +1. The Interface continues the DMA mode until the word count = 0 and then sets DMA Complete (status register, bit 04) and generates an interrupt.

TABLE A-4

MEMORY ADDRESS REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Memory Address	Program read/write, cleared by bus reset. Before entering a DMA mode, the program writes the starting memory byte address of the transfer. After each word is transferred, during the DMA mode, the Interface increments the address by +2 bytes.

TABLE A-5

STATUS REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00	Spare Input #1	Program read/write, cleared by bus reset. This bit is directly presented to the Host and can be programmed as required.
01, 02	Address Bits 16, 17	Program read/write, cleared by bus reset. These bits are used in conjunction with the memory address register to expand the DMA addressing capability to 256K bytes.
03	DMA I/O Mode	Program read/write, cleared by bus reset. The program writes this bit prior to a DMA mode as follows: 1 = DMA input, 0 = DMA output. This bit must not be changed until the DMA operation is complete.
04	DMA Complete	Program read only, cleared by bus reset or by starting a DMA mode. The Interface sets this bit at the completion of a DMA mode.
05	Output Word Received	Program read/write (set only), cleared by bus reset. This bit, which is sent to the Host to indicate data taken, is set by the program either when a data ready interrupt occurs or when Output Control (bit 07) is sensed. During an output DMA, this bit is set by the Interface. It is cleared whenever Output Control is not present.

TABLE A-5

STATUS REGISTER BIT DESCRIPTIONS (Cont)

Bit #	Name	Description
06	Output Interrupt Enable	Program read/write, cleared by bus reset. This bit when set allows the Interface to generate an interrupt to indicate either a data ready or an output DMA complete.
07	Output Control	Program read only. This bit reflects the state of the Output Control signal from the Host and is raised to indicate that output data is available.
08	Count ≠ Ø	Program read only, cleared by bus reset. This bit when set indicates that the word count register contains a non-zero value.
09, 10	Attention #1, #2	Program read only. These bits reflect the state of the Attention signals from the Host. If bit 11 is high, a low to high transition on either bit causes an optional interrupt to be generated.
11	Attention Interrupt Enable	Program read/write, cleared by bus reset. This bit when set allows the interface to generate an Attention (optional) interrupt if either Attention #1 (bit 09) or Attention #2 (bit 10) goes high.
12	Spare Input #2	Program read/write, cleared by bus reset. This bit is directly presented to the Host and can be programmed as required.

TABLE A-5

STATUS REGISTER BIT DESCRIPTIONS (Cont)

Bit #	Name	Description
13	Input Word Request	Program read/write (set only), cleared by bus reset. If a single word input transfer is desired, the program loads the input data register and then sets this bit to indicate to the Host that data is available. Either a data taken interrupt or sensing Input Ready (bit 15) indicates that the single transfer is complete. During an input DMA mode, the Interface reads data from memory, loads the input data register and then sets this bit. This bit is cleared whenever a new data ready pulse (NDRY) occurs. (Note: The Interface generates an NDRY pulse, for the Host, whenever Input Control, from the Host, goes high.
14	Input Interrupt Enable	Program read/write, cleared by bus reset. This bit, when set, allows the Interface to generate an interrupt to indicate either a data taken or an input DMA complete.
15	Input Not Ready	Program read only. This bit is reset if both the Input Word Request (bit 13) and the Input Control signal, from the Host, are clear. When set, this bit indicates that an input data transfer is in process.

TABLE A-6

OUTPUT DATA REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Output Data	Program Read only. These bits reflect the state of the data lines from the Host. The program reads these bits either when a Data Ready interrupt occurs or after sensing output control (status bit 07). During output DMA, the Interface loads this data into memory. Note: The Interface will accept either high true or low true output data from the Host.

TABLE A-7

INPUT DATA REGISTER BIT DESCRIPTIONS

Bit #	Name	Description
00-15	Input Data	Program write only, cleared by bus reset. These bits are directly presented to the Host. (Note: The Interface will provide either high true or low true data to the Host.) During an input DMA, the Interface loads this register with memory data. During single data transfers, the program loads this data prior to raising Input Word Request (status bit 13).