Microelectronics Divisions
Rockwell International

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January 10, 1975

In response to your request, we are pleased to enclose information on our family of PPS Microprocessor devices. We are presently delivering large production quantities of PPS-4 devices.

Our Microprocessor system is unique in that we have several standard I/O devices (General Purpose I/O, General Purpose Keyboard and Display, Printer Controller and 1200 bps Modem), which interface directly between the internal bus structure and various peripherals without additional circuits.

If your application is presently in the development stage, you may find one or more of our Evaluation and Development modules useful. These popular prototyping "tools" are described in the enclosed document, No. 29003N11. The modules are moderately priced and can be furnished 30 days after receipt of your order.

An alternate prototyping approach, which you may prefer, would be to purchase a PPS-4MP Assemulator described in the enclosed literature. Because of a special arrangement with the supplier, the price has been reduced to $2,495, if purchased directly from Rockwell. Delivery is 60 days after receipt of order. Assemulator options are also available at nominal costs.

Start today by sending your purchase order to the above address.

Very truly yours,

Ronald F. Voigt

Ronald F. Voigt
Director
Customer Services

Enclosure

SAMPLE PRICES

PPS MICROPROCESSOR CIRCUITS

FOR MICROCOMPUTERS

Part Number		Prices Each
	Quantities: 1-24 *	
10660	CPU	$ 92
10432	RAM (256 x 4)	$ 70
10706	CLOCK	$ 29
10788	KEYBOARD/DISPLAY I/O	$ 95
10789	PRINTER CONTROLLER I/O	$ 90
10696	GP I/O	$ 41
10371	1200 BPS MODEM - UART (TDI)	$180
10738	BUS INTERFACE	$ 45
A05	ROM (1K x 8)	$ 22 **
A52	ROM 2K (2K x 8)	$ 23.50 **
A08	ROM/RAM (704 x 8/116 x 4)	$ 22.**
A07	ROM/RAM (1K x 8/116 x 4)	$ 23.50 **

*Higher quantities - quote.
**Available only in minimum quantities of 1,000 as part of a PPS set.

PROTOTYPING HARDWARE

PPS EVALUATION BOARD (Includes CPU, 2 RAM, 2 I/O, Clock), PN 20102 D02	$500 Each ($550 outside U.S.A.)
PPS INTERFACE KITS (Includes 2 bus interface devices, PN 10738)	
1. TTL Bus Interface Module, PN 20102 D27	$140 Each
2. SOS/ROM Interface Module, PN 20102 D30	$175 Each
3. PROM Interface Module, PN 20102 D33	$180 Each
GP I/O MODULE, PN 20102 D36	$375 Each
RAM ASSEMBLY BOARD (INCLUDES 8 RAMs, PN 10432), PN 20102 D17	$600 Each
ROM ASSEMBLY BOARD (ROMs NOT INCLUDED), PN 20102 D19	$ 45 Each

All prices f.o.b. Anaheim, California.
Prices and specifications subject to change without notice.
1 Sept. 1974

Rev. 3. June, 1974

DATA SHEET

PARALLEL PROCESSING SYSTEM (PPS-4) MICROCOMPUTER

A 4-BIT DATA WORD/8-BIT INSTRUCTION WORD MICROCOMPUTER

PPS-4 BASIC DEVICES:

CENTRAL PROCESSOR (CPU)	P/N 10660
RANDOM ACCESS MEMORY (RAM)	P/N 10432
READ ONLY MEMORY (ROM)	P/N A05---
READ ONLY MEMORY (ROM)	P/N A52---
READ ONLY/RANDOM ACCESS MEMORY (ROM/RAM)	P/N A07---
READ ONLY/RANDOM ACCESS MEMORY (ROM/RAM)	P/N A08---
GENERAL PURPOSE INPUT/OUTPUT (GPI/O)	P/N 10696
CLOCK	P/N 10706

Microelectronic Device Division
Rockwell International

Document No. 29003 N11

CONTENTS

NOTICE

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Microelectronic Device Division
Rockwell International

Microelectronic Device Division

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INTRODUCTION

SCOPE

This data sheet describes the basic circuits of the Rockwell 4-bit word Parallel Processing System (PPS-4) microcomputer. These basic circuits, and associated special purpose input/output circuits and memory devices are listed in Table I. This data sheet also describes system characteristics, timing and interface requirements, and the design software and hardware aids offered by Rockwell.

GENERAL

The PPS-4 system is a set of modular MOS/LSI circuits which provides equipment designers with a low cost means of developing a range of versatile, powerful, custom programmed microcomputer systems.

A minimum PPS-4 system can be made from only two MOS/LSI circuits and a clock circuit. The modular design of the PPS-4 circuits allows designers to create very powerful systems by simply adding additional Rockwell memory and/or I/O circuits. The typical system shown in Figure 1 delineates these expansion parameters. The many different types of available I/O and memory circuits enhances the economics and versatility of the PPS-4.

The PPS-4 has a high throughput and fast execution speed which enables the PPS-4 to economically implement many functions normally thought to require 8-bit or larger processors. High throughput is demonstrated by the PPS-4 strobing and transferring data from the I/O to RAM at a rate of 36 μsec per 8-bit byte, and fast execution is demonstrated by the addition of two 8-bit decimal numbers in 240 μsec.

Other design advantages include simpler programming with less program steps, quicker turn-around in system prototyping, the use of fewer components to implement systems, and the capability of Rockwell to design and produce custom I/O devices to suit a user's unique requirements.

FEATURES

Functional Power:

- 50 Instructions, which include—
  - Arithmetic and Logic Operations
  - Conditional and Unconditional Transfers
  - Direct and Indirect Subroutine Calls
  - Direct and Indirect RAM Addressing
  - Input/Output Commands
- 4-bit data words/8-bit instruction words
- Hardware/software subroutine stacking – unlimited nesting.
- Implementable Interrupt

Performance Power:

- 21-line parallel bus structure.
- Fast execution time – adds two 8-digit decimal numbers in 240 μsec.
- High throughout – parallel data transfer RAM to I/O or I/O to RAM:
  - 4-bit byte/28 μsec
  - 8-bit byte/36 μsec
  - 12-bit byte/56 μsec
- Decimal and binary arithmetic modes.
- Directly addressable up to 16 1Kx8 ROMs or 16 2Kx8 ROMs, and 32 256x4 RAMs (294,912-bit memory capacity).
- Directly addresses up to 16 I/O circuits.
- Advanced MOS/LSI Non-Volatile RAM and Electrically Alterable ROM circuits.

Design/Production Economics:

- No external interface circuitry required between CPU, memories, and I/O circuits.
- Eight LSI interface/control circuits – including a direct bus-to-TTL memory circuit, direct Keyboard and Display control circuit, and a MODEM/UART circuit on a single chip.
- Custom designed I/O devices for special applications.
- All I/O circuits are TTL compatible
- Single power supply
- ROM/RAM (one chip) for production of two chip (plus clock) minimum systems.
- Four-phase dynamic operation for low power and high speed
- No memory refresh circuitry required
- Complete software and hardware development support

Table 1. PPS Circuit Devices

Devices	Function	Availability
BASIC DEVICES		
Central Processor Unit (CPU), P/N 10660	Provides the arithmetic and control circuitry. Functions as 4-bit parallel data processor, and when combined with other devices forms the control center of the PPS-4 microcomputer.	Now
Clock Generator, P/N 10706	Generates the basic 4-phase clock signals A and $\overline{B}$.	Now
General Purpose Input/Output, P/N 10696 (GPI/O)	Connects the PPS-4 instruction data bus lines to external MOS or TTL circuits. Provides 12 discrete inputs and 12 discrete static outputs.	Now
1K Read Only Memory (ROM), P/N A05——	Stores the custom programs. Provides 8192 bits in an 8 x 1024 bit configuration.	Now
2K Read Only Memory (ROM), P/N A52——	Functionally the same as the 1K ROM, but provides twice the storage capacity on a single chip, (16,384 bits).	Now
Random Access Memory (RAM), P/N 10432	General working and memory register for data storage. Provides 1024 bits in a 4 x 256 configuration.	Now
ROM/RAM, P/N A08——	Provides both the ROM and the RAM function on one chip for systems requiring limited memory with minimum cost (704 x 8/76 x 4).	Now
ROM/RAM, P/N A07——	Same function as the A08—— except the A07—— offers more memory (1024 x 8/116 x 4).	Now
OTHER MEMORY DEVICES		
Electrically Programmable ROM (EPAROM), P/N 10443	Provides block-eraseable, non-volatile program storage for 256 8-bit words.	1st Qtr 1975
Non-Volatile RAM (NV RAM), P/N 10439	Provides word-eraseable, non-volatile data storage for 256 4-bit words.	1st Qtr 1975
SPECIAL PURPOSE INPUT/OUTPUT DEVICES		
General Purpose Keyboard and Display Control, (GPKD) P/N 10788	Provides 64 key strobing, key debounce, 2 key rollover protection, 9 key buffering, and two 16 4-bit character display buffers with automatic refresh.	Now
Printer Controller, (PC), P/N 10789	Provides 21 4-bit character print buffer and automatic control and timing for the Seiko 101, 102, and 104 printers.	Now
Telecommunications Data Interface, (TDI), P/N 10371	1200 BPS data transmission. Full duplex operation including two 8-bit transmit buffers and two 8-bit receive buffers for complete UART functions. Compatible with either the Bell 202 or CCITT systems	Now
Keyboard/Printer Controller, (KPC), P/N 10815	Provides complete control of the Seiko 320 printer and the capability of reading a 64-key keyboard.	4th Qtr 1974
Display Controller, (DC) P/N 10814	Provides control of a 16 digit display. Uses internal buffer, decode logic and output strobes.	4th Qtr 1974
Bus Interface Circuit, (BI) P/N 10738	Permits core, static memories, and TTL I/O access to the PPS Bus.	Now
Serial Data Controller (SDC) P/N 10930	Full duplex, 0 thru 12 KBPS, asynchronous data transmission. Provides odd/even parity and one or two stop bits selection. EIA RS-232-C compatible.	2nd Qtr 1975

DESCRIPTION

GENERAL DESCRIPTION

Each of the PPS-4 circuits (except for the clock) are packaged in 42-pin flat packs to provide maximum interfacing capability. A complete system can consist of only two 42-pin packages (the CPU and a ROM or combination ROM/RAM) plus the 4-phase clock generator. The PPS-4 circuits have been designed as a compatible group and each has been configured to maximize circuit density and processing speed, and to minimize power consumption. The CPU with its 12-bit parallel address bus and 8-bit parallel instruction/data bus directly addresses 4K of 8-bit instruction (ROM) words and 4K of 4-bit data (RAM) words while simultaneously the ROM outputs instruction words to the CPU in the form of 8-bit parallel information and the RAM transmits and receives 4 bits of data in parallel during the same one cycle time. It is this parallel organization, along with a sophisticated time sharing technique, which results in an unusually high data rate.

The implementation of a broad class of digital equipment is possible because of the one chip central processing unit (CPU) which receives and decodes an 8-bit instruction word to perform all required arithmetic and logic operations. The large number of instruction words to which the CPU responds gives it the capability of a 4-bit parallel minicomputer. These instruction words (referred to as micro instructions) are stored in ROMs for rapid accessing while RAMs are used to provide register files and storage of working data. An input/output buffer and multiphase clock generator complete the basic circuits required to configure a total system. Figure 1 illustrates a typical PPS-4 organization.

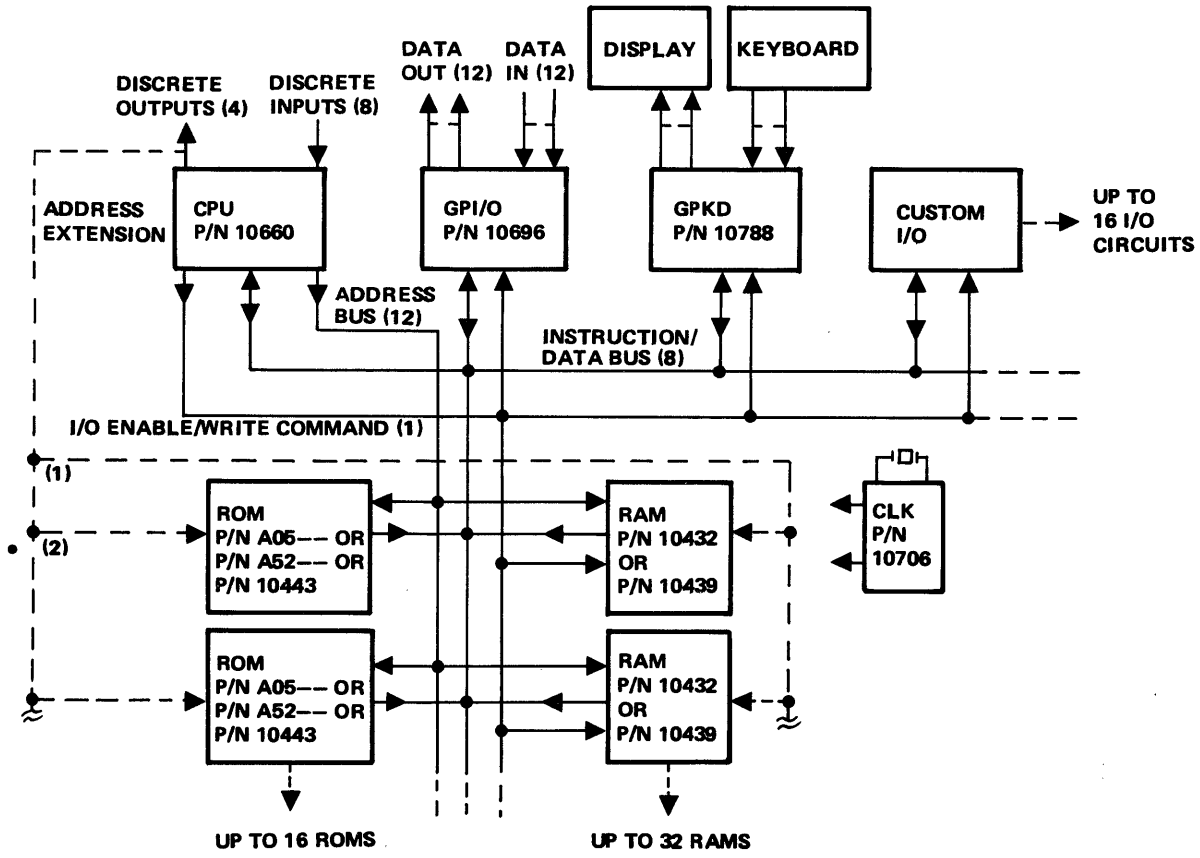


Figure 1. Typical System Block Diagram.

DESCRIPTION – CENTRAL PROCESSING UNIT (CPU), P/N 10660

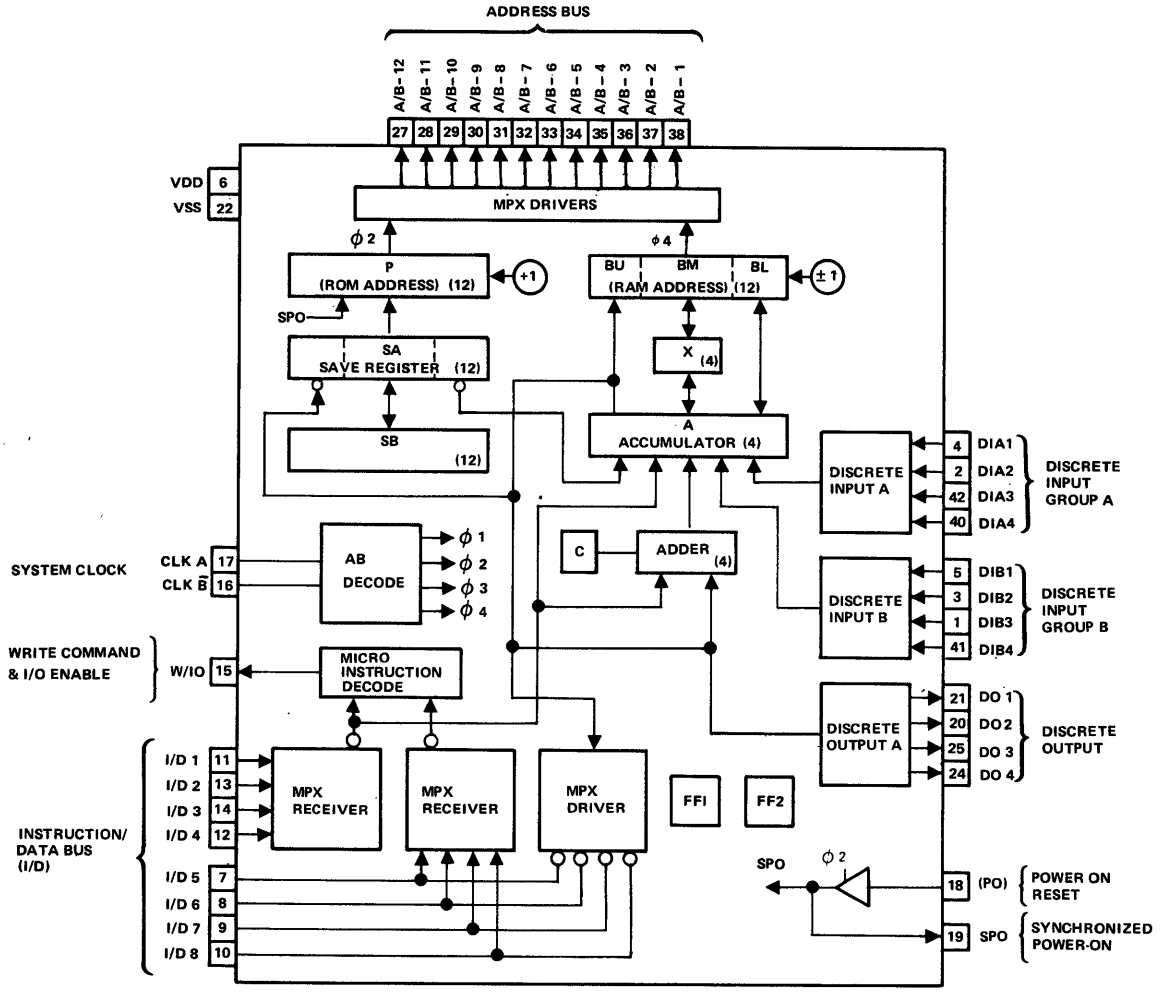


Figure 2. Central Processing Unit Block Diagram.

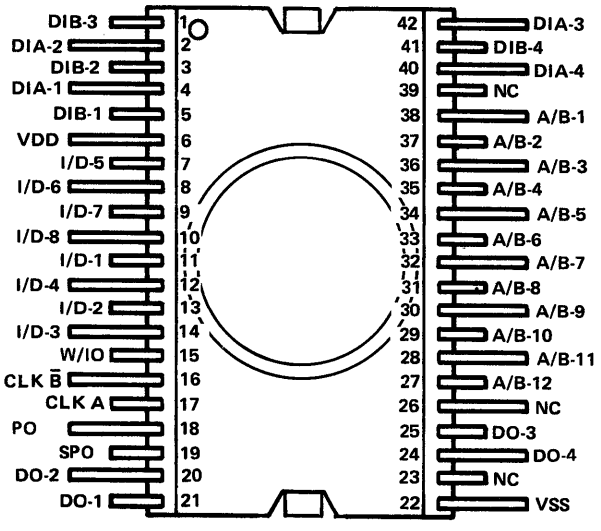


Figure 3. Central Processing Unit (CPU) Pin Configuration.

The Central Processing Unit (CPU) shown in Figure 2 is a 4-bit parallel processor. The CPU, through time sharing, utilizes an 8-bit parallel I/D bus to transfer 8-bit word instructions from ROM to CPU and I/O and also as a dual bidirectional 4-bit parallel data bus to transfer data between the CPU and RAMs and I/Os.

For memory expansion, software interrupt, or direct access with peripheral equipment, the CPU includes 8 discrete input and 4 discrete output lines.

The CPU contains: (a) microinstruction decoding necessary to receive and decode 50 basic instructions, (b) 4-bit parallel adder-accumulator for arithmetic and logic operations, (c) 12-bit (B) register for creating and storing addresses for RAM, (d) 12-bit (P) register and two 12-bit "Save" registers for creating and storing addresses for ROM, (e) 8 discrete input synchronizers, (f) 4 discrete output static drivers, (g) two individual control flip-flops and (h) multiplexed receivers and drivers for interfacing with the 12-bit parallel address bus and the 8-bit parallel data/instruction bus, and W/IO control line.

(a) Micro-Instruction Decode

The decode portion of the chip interprets the instructions to control data transfers, arithmetic operations, and set up logical sequences. Instructions are coded in one byte (8 bits) and grouped as arithmetic, logical, data transfer, control transfer, input/output and special instructions. Direct subroutine calls, unconditional transfers, direct RAM address modifications, and the Input/Output command are considered long instructions because they require two bytes of ROM storage. However, the indirect subroutine call and indirect RAM address modification require only one byte of ROM storage. All instructions are executed in one cycle time of the "A" clock except long and indirect instructions and the I/O instruction which are executed in two cycle times. The instructions to which the CPU responds are listed on Pages 17 through 21.

(b) Adder-Accumulator

The adder is a 4-bit parallel binary adder with an internally connected carry FF for implementing precision arithmetic operations. The adder together with the 4-bit accumulator form the Arithmetic Logic Unit (ALU) secion of the CPU. Functionally, the CPU has ten microinstructions dedicated to arithmetic and logical operations. All are one-cycle instructions and enable direct arithmetic operation between the accumulator and the data stored in RAM or ROM memory.

In addition to its arithmetic functions, the accumulator is the primary working register in the CPU and is the central data interchange point for almost all data transfer operations occurring in the Parallel Processing System.

During internal data transfer the accumulator is the interfacing data register for both RAM and ROM. For external data exchanges (Input/Output) the accumulator is the source of the output data and the receiver register for the input data.

Because of the high usage of the accumulator, a secondary (extra) X-register has been included in the CPU. The X-register is a 4-bit register and is used in conjunction with the accumulator for temporary storage of data.

(c) RAM Address Register

This 12-bit B register, consists of three 4-bit registers (BU, BM and BL), which contain the address location to be accessed in RAM. Register BL is a counter and can be incremented or decremented by 1 through program control providing the ability to sequence through RAM registers serially by 4-bit character. The upper 8-bits (BU and BM) of RAM address can be set to special values by program control during a transfer operation of data to or from a distant RAM location into the working storage area indicated by the 4-bits of BL. During RAM address modification operations it is also possible to use accumulator A and register X for temporary storage of the upper 8 bits of the new address retrieval from RAM without destroying the current RAM address pointer.

(d) Program Counter and Save Register

The 12-bit P-register and counter contains the address of the next program instruction. The lower 6-bits is a counter which is automatically incremented each cycle time during normal operation. The most significant 6-bits give the ROM number and page location. These six bits are only modified by the unconditional transfer (TL) or subroutine call (TML and TM) instructions. The SA and SB registers are two "Save" registers which provide a two level stack for holding instruction addresses during branching. This gives a direct two level nesting capability for storing program subroutine addresses in hardware; however, unlimited nesting is available via instruction CYS. This instruction recirculates register SA and accumulator A and, therefore, provides for saving ROM program addresses in RAM. Since RAM can be used for storing program addresses, subroutine nesting becomes limited only by the amount of dedicated storage allocated for this purpose.

(e) Control Flip-Flop (FF) and Discrete Input/Output (I/O)

There are two control flip-flops, FF1 and FF2, which can be set, reset, and tested by program control. There are also 8 discrete inputs which can be copied directly into the accumulator as two separate 4-bit groups. These groups are identified as discrete inputs group A (DIA) and discrete inputs group B (DIB). These inputs are intended to be used for inputting special signals, switch positions flags or interrupt line from circuitry external to the PPS. The contents of the accumulator can be outputted directly to circuits external to the PPS via a special 4-bit parallel output register (DOA) with individual output drivers. These outputs can be used to extend the ROM and RAM addressing beyond 4K. See special interface considerations on page 12 for more information on discrete inputs and outputs.

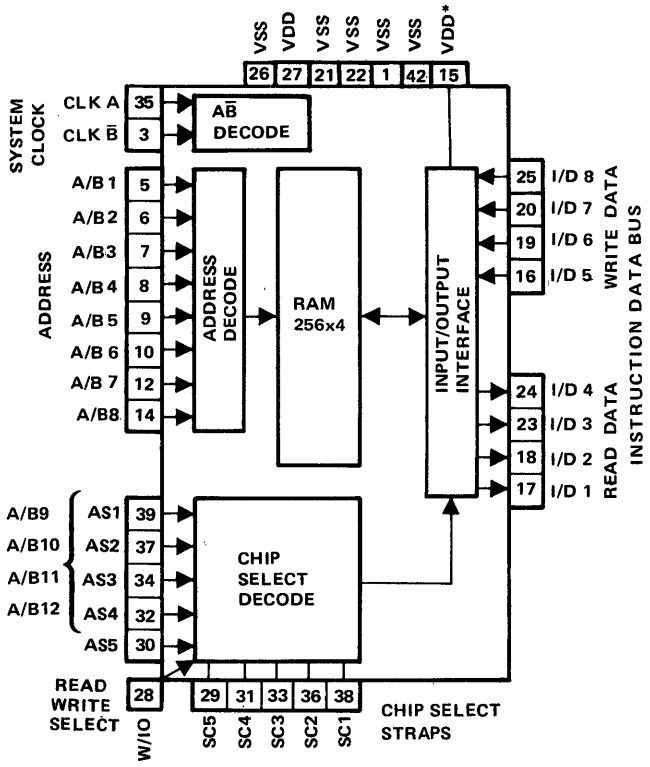
(f) Multiplex Drivers and Receivers

The multiplex driver and receiver circuits in the CPU provide direct interfacing with the system address and instruction data bus. The bus is time multiplexed and uses a unique precharge technique to achieve an unusually high system fan out. Systems containing up to 30 circuits can be mechanized without the need for external drivers.

(g) Power-On Reset

During power turn-on it is necessary to initialize the CPU P-counter to a known state such that the proper sequence of events can occur. This initialization is accomplished by inputting a negative pulse for a time duration of 10 msec or greater. This pulse is generated external to the PPS and as long as the pulse is a logic 1, the P-counter is held reset. The CPU, at the same time, generates a synchronized Power-on output signal which can be used to initialize other circuits.

DESCRIPTION – RANDOM ACCESS MEMORY (RAM) , P/N 10432



* THIS INPUT IS A SEPARATE VDD SOURCE FOR THE OUTPUT DRIVERS. THIS IS USEFUL FOR ISOLATING INDIVIDUAL CIRCUITS DURING DEVICE TESTING AND FOR FAULT ISOLATION WHEN MULTIPLE CIRCUITS ARE CONNECTED TO THE DATA BUS.

Figure 4. Random Access Memory (RAM), Block Diagram.

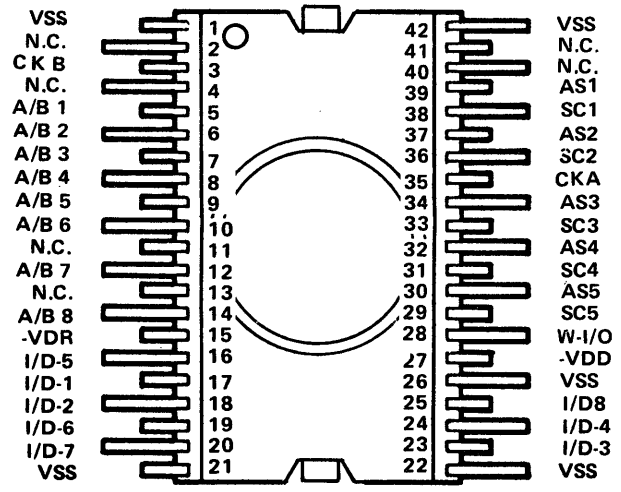


Figure 5. 256 x 4 Random Access Memory Pin Configuration.

The Random Access Memory (RAM) P/N 10432, shown in Figure 4, is a 1024-bit Random Access Memory organized in a 256 x 4-bit configuration. It has been designed as a dynamic memory with automatic refresh logic for use as a general working and memory register storage of data within a PPS set.

The Central Processing Unit (CPU), with its 12-bit parallel address outputs can directly address up to 16 RAM chips or 4096 words of 4-bit data. The RAM, with its 8 parallel address and 5 chip select inputs, provides for direct selection of up to 32 RAM chips or 8192 words of data. The one additional chip select input on the RAM chip (which cannot be addressed by the 12 bit address bus) can be used for memory expansion greater than 4096 word locations. For large systems the AS5 chip select input can be addressed by an output from an I/O circuit or a discrete output from the CPU. For systems with RAM memory capacity of 4096 words or smaller, the AS5 chip select input must be terminated at VSS.

The unique time sharing design of the PPS address and data buses is such that the contents of a given location in RAM can be exchanged with the contents of the accumulator in the CPU during one clock phase time. This is possible because when the RAM is addressed, it shifts the 4-bit data contents of the addressed location to the RAM output registers which place the data on one of the 4-bit parallel data buses. At the same time, if the write/RAM select input to the RAM is enabled, the RAM captures the data on the other 4-bit parallel data bus and copies it into memory location being addressed. In order for this to work, the CPU has placed the contents of the accumulator into its output register (which is the data being written into the RAM) and copies the data output from the RAM into the accumulator. This timing and data exchange capability is a major key to the high data rate and predictable performance of the PPS.

RAM CHIP ADDRESS SELECTION

CHIP NO. \ CHIP SELECT STRAP	SC 5	SC 4	SC 3	SC 2	SC 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
•					
•					
•					
31	1	1	1	1	1

WHERE 1 = VDD, 0 = VSS

Figure 6. RAM Chip Address Selection Format.

DESCRIPTION – READ ONLY MEMORY (ROM), P/N A05-–

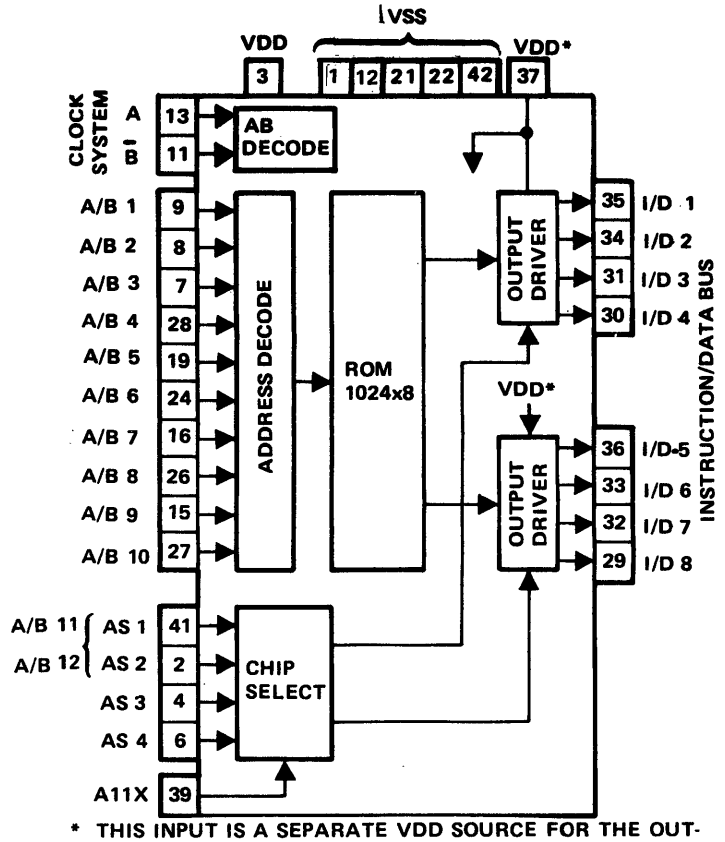


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Figure 7. Read Only Memory (ROM) Block Diagram, P/N A05-–

The Read Only Memory P/N A05--, shown in Figure 7, is a 8192-bit Read Only Memory organized in a 1024 x 8-bit configuration. It has been designed with dynamic address decode logic for interface compatibility with the PPS CPU. The ROM is programmed with a custom mask and is primarily intended to be used to store 8-bit micro-instruction routines for control and sequencing of data within a PPS set. The Central Processing Unit with its 12-bit parallel address outputs, can directly address up to 4 ROM chips or 4096 words of microinstruction. The ROM, with its 10 address and 4 chip select inputs, provides the direct selection of up to 16 ROM chips or 16,384 words of microinstruction. The two additional chip select inputs on the ROM chip (which cannot be addressed by the 12-bit address bus) can be used for memory expansion greater than 4096. A detailed discussion of the ROM system expansion can be found in the programers manual. If not used, the extra inputs (AS3 and AS4) should be tied to VSS.

In addition to its primary function of storing microprograms, the ROM is designed such that it can be encoded, during the mask operation, to respond to Read Out during the RAM time interval. This means that a selected ROM can be used as a Read Only RAM for code conversion or a table look-up operation. When used in this application, the selected ROM responds to the RAM address and transmits 4-bits of data to the data bus. The 8 parallel outputs from the ROM are externally connected together to form a 4-bit parallel output. The A11X address term is used to select the upper or lower 4 bits of the 8-bit output. This has the effect of creating a 2048 x 4-bit organization for the storage of permanent data which is easily addressed and accessed by the RAM data transfer instructions. For example A11X=0 selects I/D5–I/D8 and A11X=1 selects I/D4–I/D1.

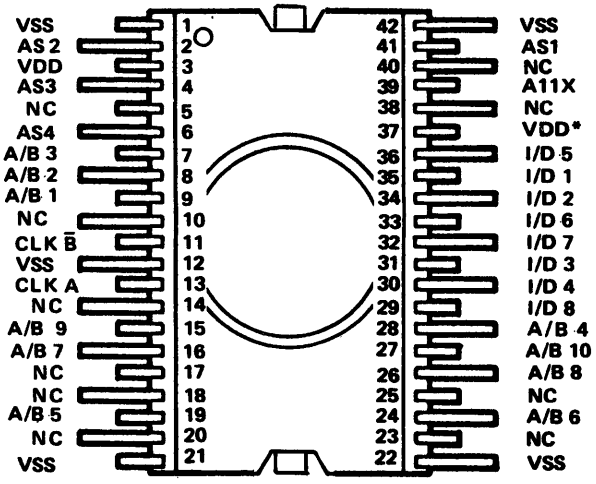

Figure 8. Read Only Memory Pin Configuration, P/N A05-–

DESCRIPTION – READ ONLY MEMORY (ROM), P/N A52--

The Read Only Memory P/N A52--, shown in Figure 9 is a 16,384-bit read only memory organized in a 2048 x 8-bit configuration. Functionally, the A52-- ROM is identical to the A05-- ROM except that the A52-- ROM provides twice as much storage capacity. The pin-outs and internal circuitry is similar except that addressing inputs A/B11 on pin 41 goes to the Address Decode circuits instead of the Chip Select circuits and input A11X becomes AS5. These addressing input changes provide for addressing the additional memory.

It has been designed with dynamic address decode logic for interface compatibility with the PPS CPU. The ROM is programmed with a custom mask and is primarily intended to be used to store 8-bit microinstruction routines for control and sequencing of data within a PPS set. The Central Processing Unit with its 12-bit parallel address outputs, can directly address up to 2 ROM chips or 4096 words of microinstruction. The ROM, with its 11 address and 4 chip select inputs, provides for direct selection of up to 16 ROM chips or 32,768 words of microinstruction. The three additional chip select inputs on the ROM chip (which cannot be addressed by the 12-bit address bus) can be used for memory expansion greater than 4096. A detailed discussion of the ROM system expansion can be found in the programers manual. If not used, the extra inputs (AS3, AS4 and AS5) should be tied to VSS.

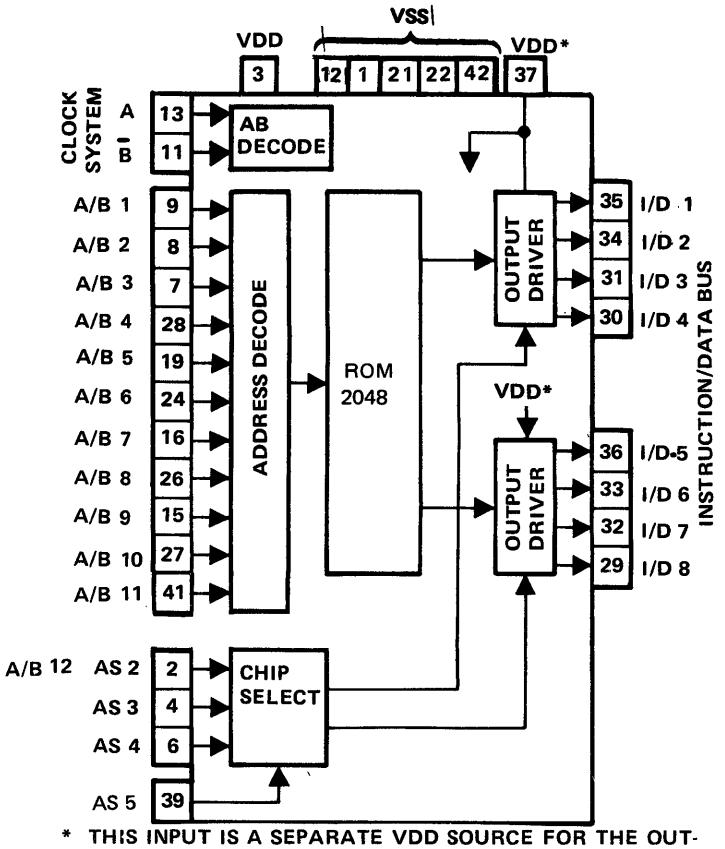

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Figure 9. Read Only Memory (ROM) Block Diagram.

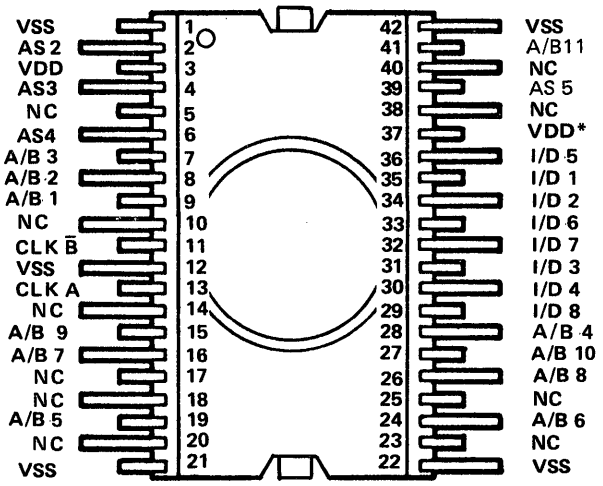


Figure 10. Read Only Memory Pin Configuration.

DESCRIPTION – READ ONLY MEMORY/RANDOM ACCESS MEMORY (ROM/RAM), P/N A07--

Read Only Memory/Random Access Memory (ROM/RAM) P/N A07-- is similar to ROM/RAM P/N A08-- except that the A07-- provides 8192 bits of ROM storage and 464 bits of RAM storage which is considerably greater than the storage in the A08--. Like the A08--, the A07-- is uniquely designed for use with the PPS-4, and is especially adaptable for production of low cost microcomputer systems since both the ROM and RAM are a single circuit. Application of this device is common in controllers, small cash registers, electronic weighing scales, fast food service terminals, etc.

The ROM section is organized as 1024 x 8 words and the RAM section is organized as 116 x 4 words. The block diagram shown in Figure 11 is valid for ROM/RAM A07--, and the pin configurations and address formats in Figures 12 and 13 are also valid for the A07--.

Two A07-- ROM/RAM's may be used in a single system, or one A07-- may be combined with one A08-- in a single system. The ROM function is selected by A/B11, and the RAM function is selected by A/B7. Both A/B7 and A/B11 can be masked so that either is activated by a logic one or zero. During the RAM function time A/B9 and A/B10 must be at "0",

DESCRIPTION – READ ONLY MEMORY/RANDOM ACCESS MEMORY (ROM/RAM), P/N A08 ––

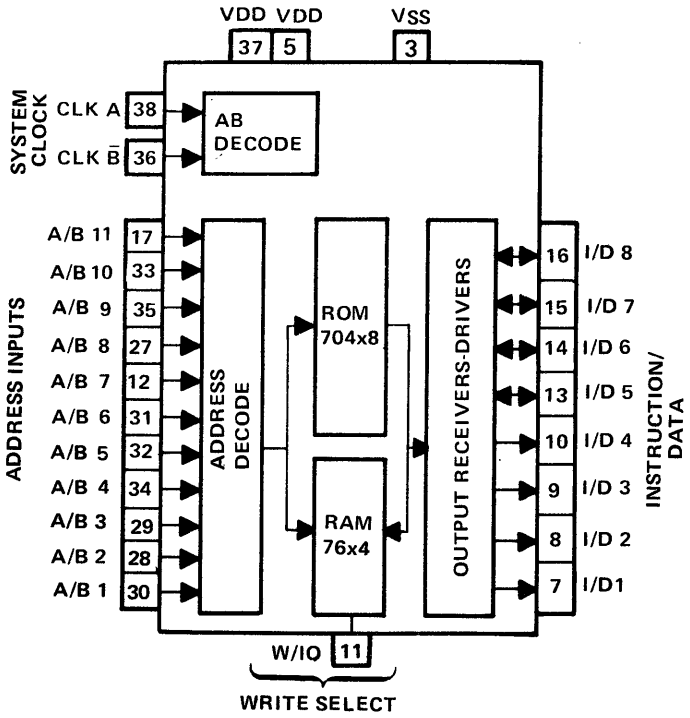


Figure 11. ROM/RAM Block Diagram P/N A08–– and P/N A07––

The Read Only Memory/Random Access Memory P/N A08--, shown in Figure 11, is a circuit containing a mask programmable MOS ROM as well as a RAM. It is uniquely designed to interface with the PPS CPU address and data bus and, as such, is useful in equipments requiring only a relatively small amount of ROM and RAM. The ROM section is organized as 704 x 8 words (5,632 bits) while the RAM section is organized as 76 x 4 words (304 bits). The chip interfaces with the common address bus and contains a single address decoder section. Internal clock timing is generated such that the decoded address is routed to the RAM section or the ROM section as a function of "A" and "B" clock inputs. In a like manner, the outputs drive or receive data from the 8-bit instruction/data bus in the PPS as a function of clock timing and control signals. From the users' point of view, this single chip provides the same functions as the ROM chip, P/N A05-- and the RAM chip, P/N 10432, except for the smaller amount of ROM and RAM.

The addressing mask option provides for up to two A08-- ROM/RAM's in a single system. Specifically, the ROM function is selected by A/B11, and the RAM function selected by A/B7. Both A/B7 and A/B11 can be masked so that either is activated by a logic one or zero. During the RAM function time A/B9 and A/B10 must be at "0".

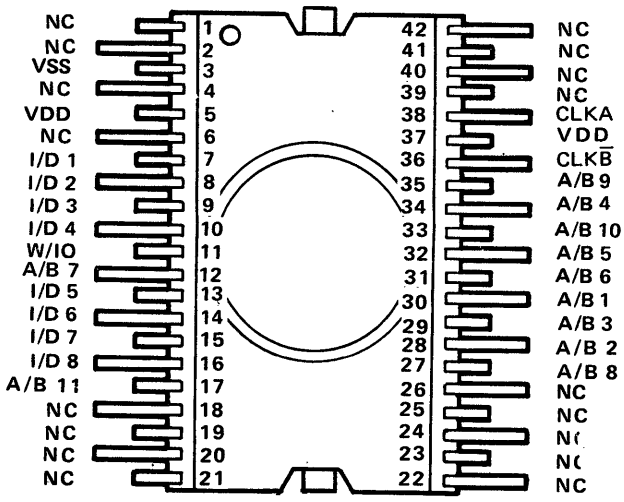
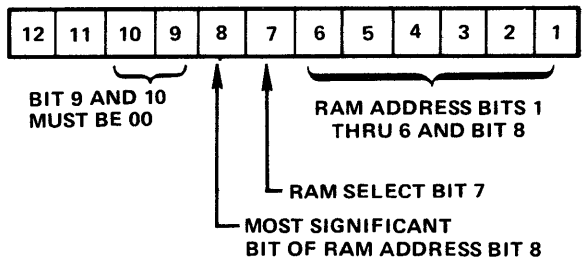


Figure 12. ROM/RAM Configuration.

RAM ADDRESS FORMAT (B REGISTER)



ROM ADDRESS FORMAT (P REGISTER)

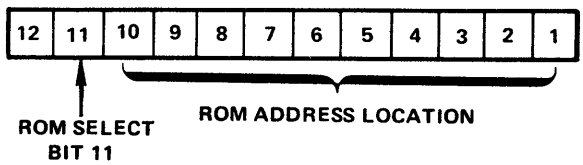


Figure 13. RAM Address Format.

DESCRIPTION – GENERAL PURPOSE INPUT/OUTPUT (I/O), P/N 10696

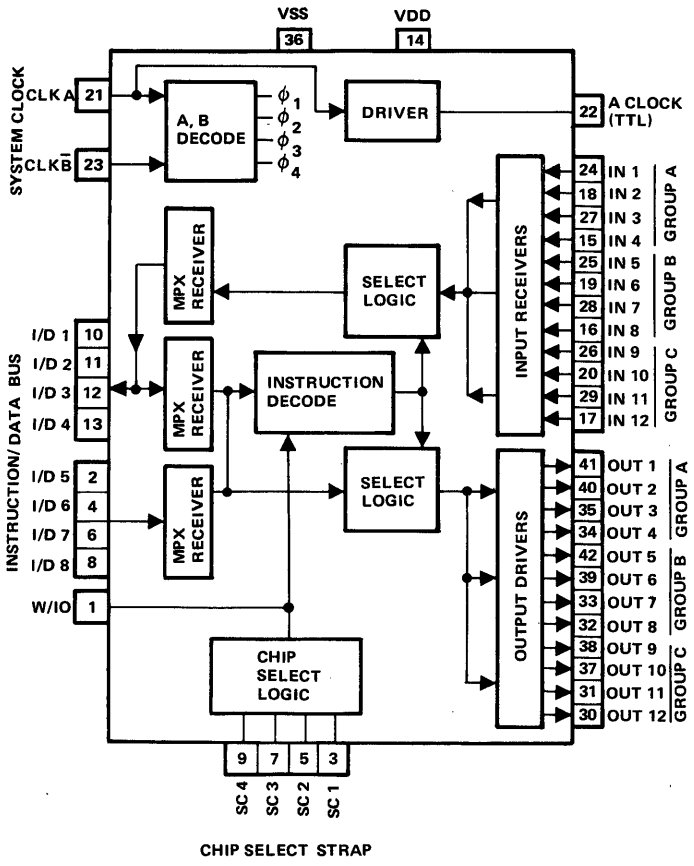


Figure 14. General Purpose Input/Output Device Block Diagram.

The General Purpose Input/Output device P/N 10696, shown in Figure 14. provides 12 discrete inputs and 12 discrete static outputs. This device is used for direct data exchange or status and control functions with an external peripheral device. The GPI/O circuit uses special interface circuitry to directly interface with TTL circuitry. A schematic of the recommended TTL interface is shown on page 12, Special Interface Considerations. Direct addressing for up to sixteen of these circuits is possible by the use of 4 chip address straps that can be terminated, by the user, to create each chip address. The I/O is accessed with an I/O enable signal from the CPU and a simultaneous 8-bit instruction from ROM. Four bits of the instruction are used to address the particular I/O chip; the other four bits define the I/O operation.

The 4-bit operation code is interpreted by the I/O to either copy the contents of the accumulator into one of the three 4-bit parallel output registers (A, B or C) or transfer data from one of the 4-bit parallel input receivers (A, B or C) into the accumulator of the CPU. The output drivers are static outputs and data remains in the output registers until altered. Bits 1 through 4 of the instruction word are commands to the I/O while bits 5 through 8 are used to address 1 of 16 possible I/O chips. The four I/O select inputs terminated by the user, create the addresses for each I/O circuit. The I/O coding is shown below.

Data is transferred through the GPI/O from input groups A, B or C to I/D 1-4 and output groups A, B or C to I/D 5-8 most significant to most significant and least significant to least significant. For Signal Polarity see special interface considerations Page 12.

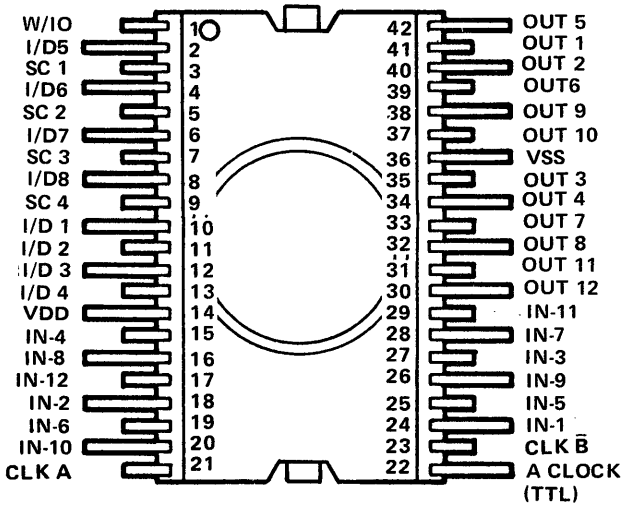
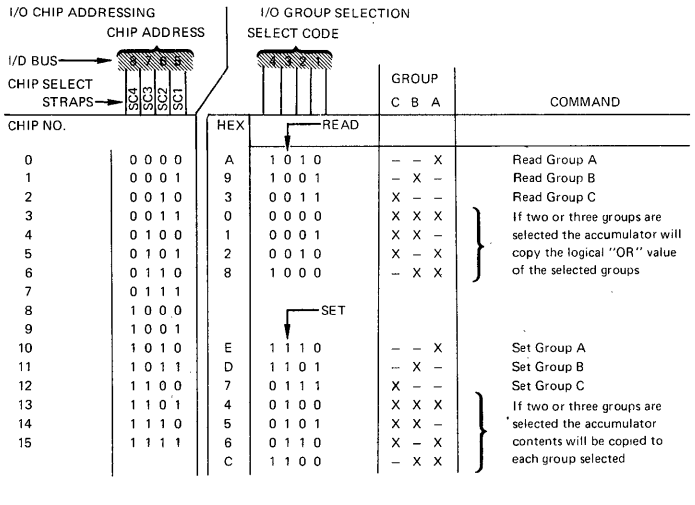


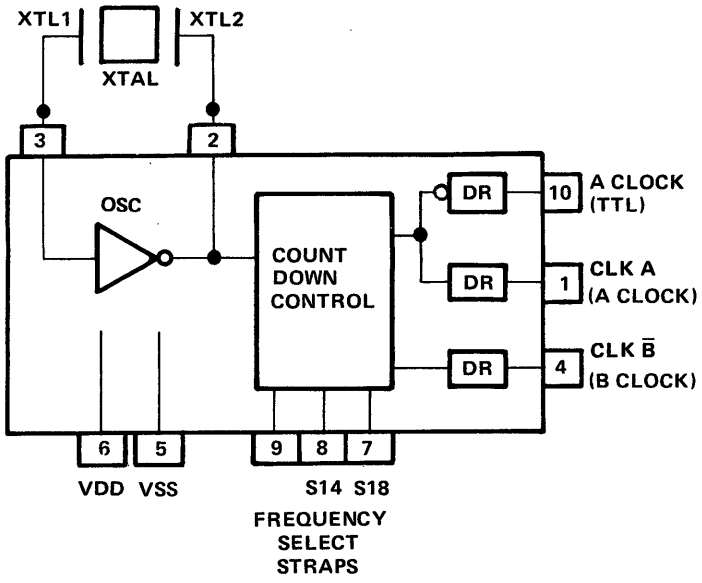
Figure 15. General Purpose Input/Output Pin Configuration.



NOTE: Any one of the I/O chips may be used to read or set any group (A, B, or C) or combination of groups.

Figure 16. GPI/O Instruction Format.

DESCRIPTION – CLOCK GENERATOR, P/N 10706



NOTE: PIN 5 IS INTERNALLY TIED TO THE CASE

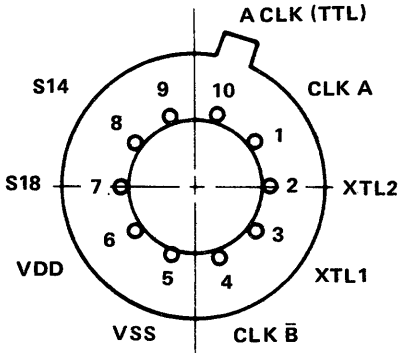
Figure 17. Clock Generator Block Diagram

The Clock Generator circuit P/N 10760, shown in Figure 17, generates the "A" and "$\overline{B}$" clock waveforms required by circuits in the PPS. The combined A and $\overline{B}$ clocks provide the unique 4-phase dynamic timing shown in Figure 23 and described in the associated text on page 14. The Clock Generator has an internal oscillator which is stabilized by connecting a quartz crystal to the appropriate inputs. The crystal is a 3.579545 MHz color TV crystal which is low in cost and readily available. The "A" clock output is a square wave and considered the primary clock. Output "$\overline{B}$" is a pulse output occurring during each phase of the "A" clock and has unique timing features required by the circuits within the PPS set. The "A" clock is also provided through an output which drives to ground such that TTL levels can be easily achieved for synchronizing equipment external to the PPS.

The input straps provide a countdown of the oscillator frequency equal to the number associated with the strap: i.e., S14 divides by 14 and S18 input results in a countdown by 18. Thus, with a crystal frequency of approximately 3.58 MHz and input S18 terminated to V_{DD}, the "A" clock output frequency will be 358 ÷ 18 = 199 kHz. This is the recommended mode of operation when used in the PPS set.

Crystal Specifications (3.57954 MHz)

Max Series Resistance	150 Ω
Excitation Level	10 ± 1 Mw
Shunt Capacity	7 Pf Max
Load Capacity	16 Pf ± 0.5 Pf



BOTTOM VIEW

Figure 18. Clock Generator Pin Configuration, P/N 10706NB.

FREQUENCY SELECTION

SELECT STRAPS / DIVISION	S14	S18	CLOCK FREQ
÷ 18	0	1	199 kHz
÷ 14	1	0	256 kHz

WHERE 1= VDD, 0 = VSS

Figure 19. Frequency Selection Format.

SPECIAL INTERFACE CONSIDERATION

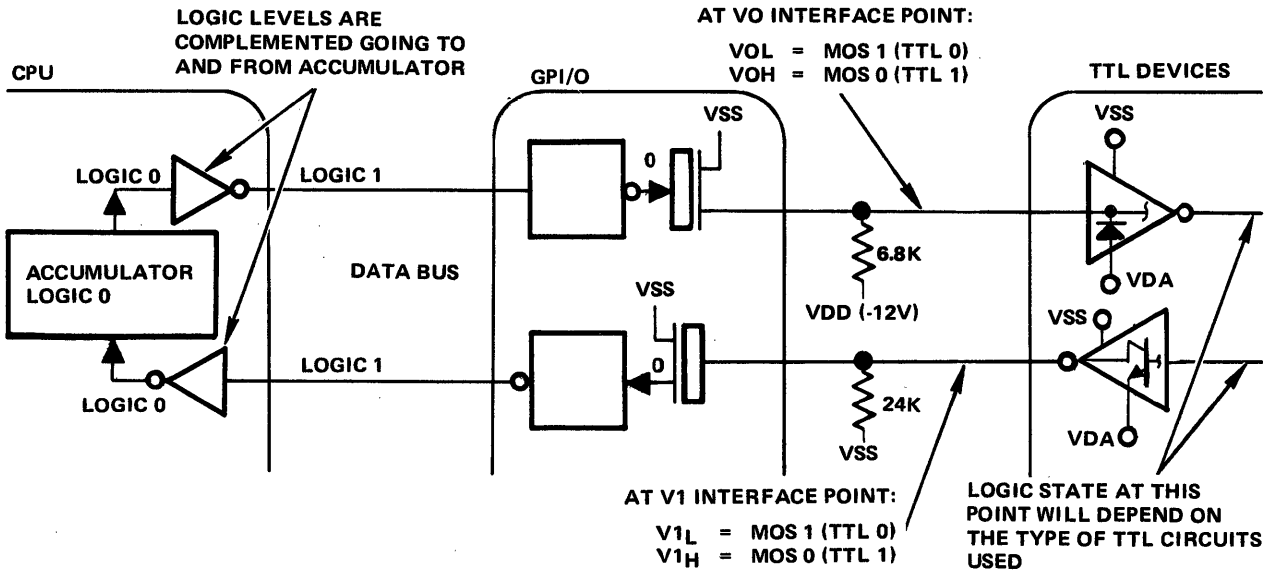
GPI/O Outputs and "A Clock TTL Output"

The GPI/O outputs are open drain buffers which when turned on will drive the GPI/O output to VSS with a maximum resistance of 1K ohms and a maximum current capacity of 2.7 mA. When turned off the GPI/O output will float, hence a pull down resistor to VDD is required. A logic 1 on a data bus will turn the corresponding driver off and a logic 0 will turn the driver on. These circuits can be used for either TTL or MOS levels. Shown is the circuit termination for a TTL interface. The diode, which is internal to the TTL device, prevents a reverse breakdown of the TTL gate. The transfer of data through the GPI/O is done without any signal inversions. However, data bus signals are inverted from the I/D bus to the CPU accumulator and from the CPU accumulator to the I/D bus.

GPI/O Inputs

The GPI/O inputs are a low threshold design which will respond to the TTL voltage levels. A recommended circuit for TTL to MOS interface is shown in Figure 20. For optimum performance, the TTL device should have an open collector output. The window of voltage values with respect to VSS where the device will change state internally is between -1.5V and -4.2V.

The transfer of data through the GPI/O is done without signal inversions. However, data bus signals are inverted from the I/D bus to the CPU accumulator and from the CPU accumulator to the I/D bus.



NOTE: VSS, VDA, AND VDD VOLTAGE RELATIONS ARE AS FOLLOWS:

NAME	MOS GND REFERENCE	TTL GND REFERENCE
VSS	0V	+5V
VDA	-5V	0V
VDD	-17V	-12V

Figure 20. Typical GPI/O Interface Logic.

SPECIAL INTERFACE CONSIDERATION (CONT)

CPU Discrete Outputs (See Figure 21)

These outputs are designed to work with circuitry external to the MOS circuitry. This type of output is an open drain MOS transistor to VSS. In the "ON" state, the output is driven to VSS with a maximum resistance of 1.25K and a maximum current capacity of 1.25 mA. In the off state, the output is floating.

The term float means a minimum of 5 megohms to any source.

CPU Discrete Inputs (See Figure 22)

The inputs are internally synchronized to the clock so that regardless of the timing or speed of the input signal, all of the internal logic connected to this signal will accept the signal as a good true or a good false at the same bit time. The window of voltage values with respect to VSS where the device will change states internally will be between -2.5V and -7.5V.

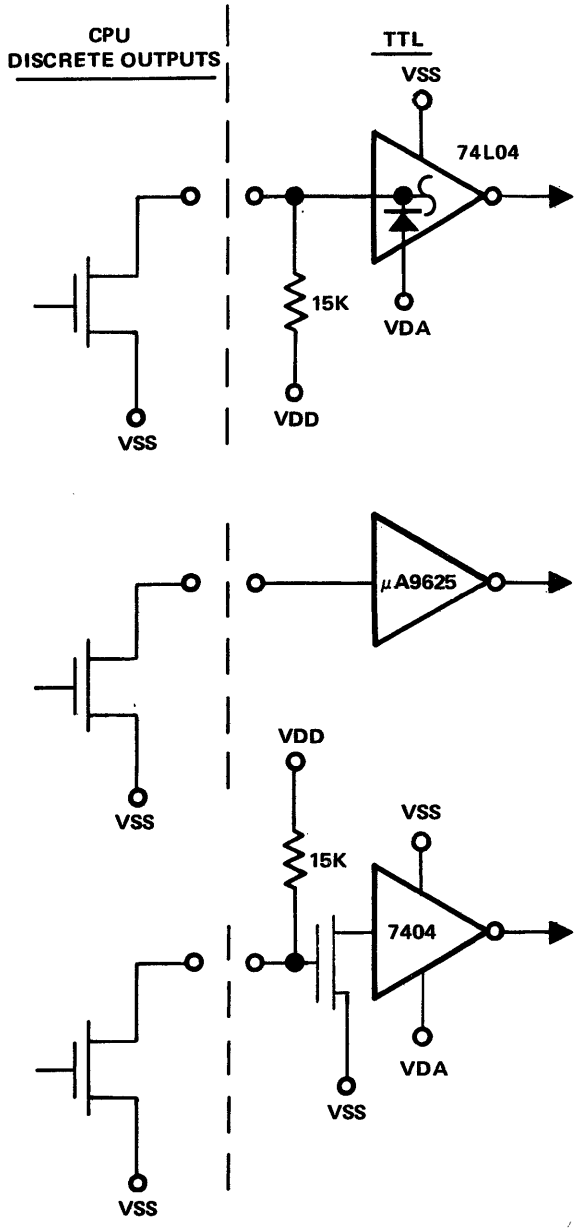


Figure 21. Typical CPU Discrete Output Circuits.

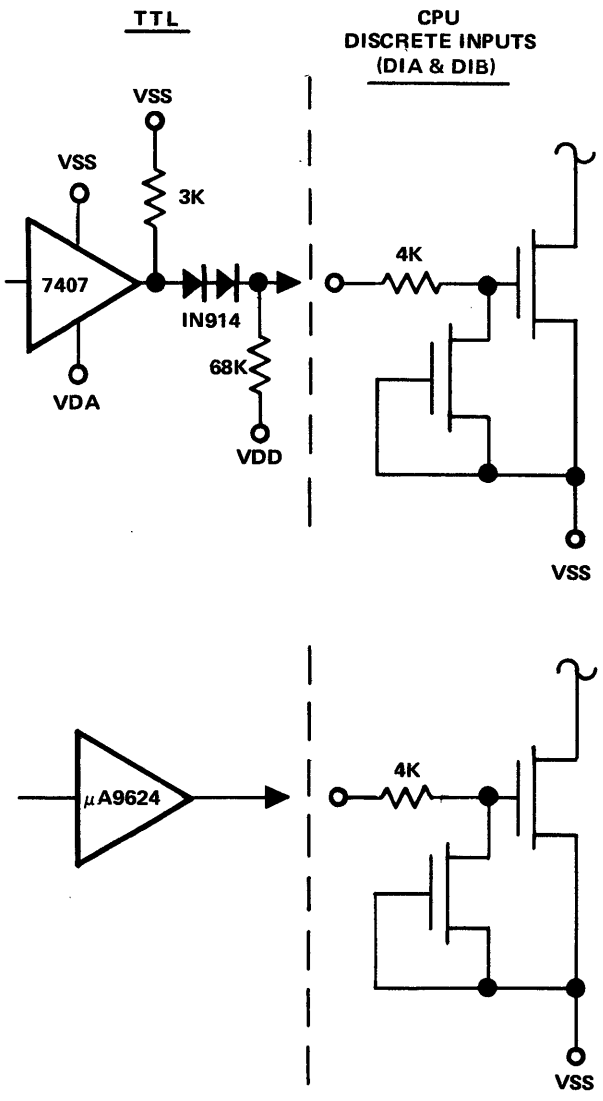


Figure 22. Typical Discrete Input Circuits.

The Parallel Processing System has a repertoire of 50 basic CPU instructions and 16 instructions for each I/O circuit. These instructions control the operation of the PPS microcomputer, and are the key to the versatility of the systems.

During each program counter bit time the CPU will address the ROM, read and decode the instruction, execute the instruction, increment the ROM program counter, and load the RAM program counter in preparation for the next instruction. This bit time or single cycle instruction fetch and execution time is 5 μsec. The proprietary architecture and multiphase clock timing techniques of the PPS result in this unusually high data handling rate from a relatively slow external clocking system.

(a) System Timing

The PPS circuits are controlled from a crystal controlled clock generator which provides two synchronized and phased clock signals. These signals, designated as A and $\overline{B}$, are received by the CPU and logically divided into four phases, such that the internal signals are being manipulated at four times the frequency of the A clock. For example, if the A clock is 200 kHz, logic signal flow within the CPU is occurring at 800 kHz. The basic clock timing is shown in Figure 23.

The PPS parallel bus transfer lines are synchronized by A and $\overline{B}$ clock signals so that data and address transfer occurs only at $\phi 2$ and $\phi 4$ time as shown in Figures 23 and 24. During the alternate phase times, $\phi 1$ and $\phi 3$, the address and data bus lines are automatically cleared to zero. This unique interface timing enables the system to drive high capacitive loads normally associated only with larger and more complex systems. In fact, systems with up to 30 PPS devices can reliably share the PPS bus without the need for additional buffering or drive circuitry.

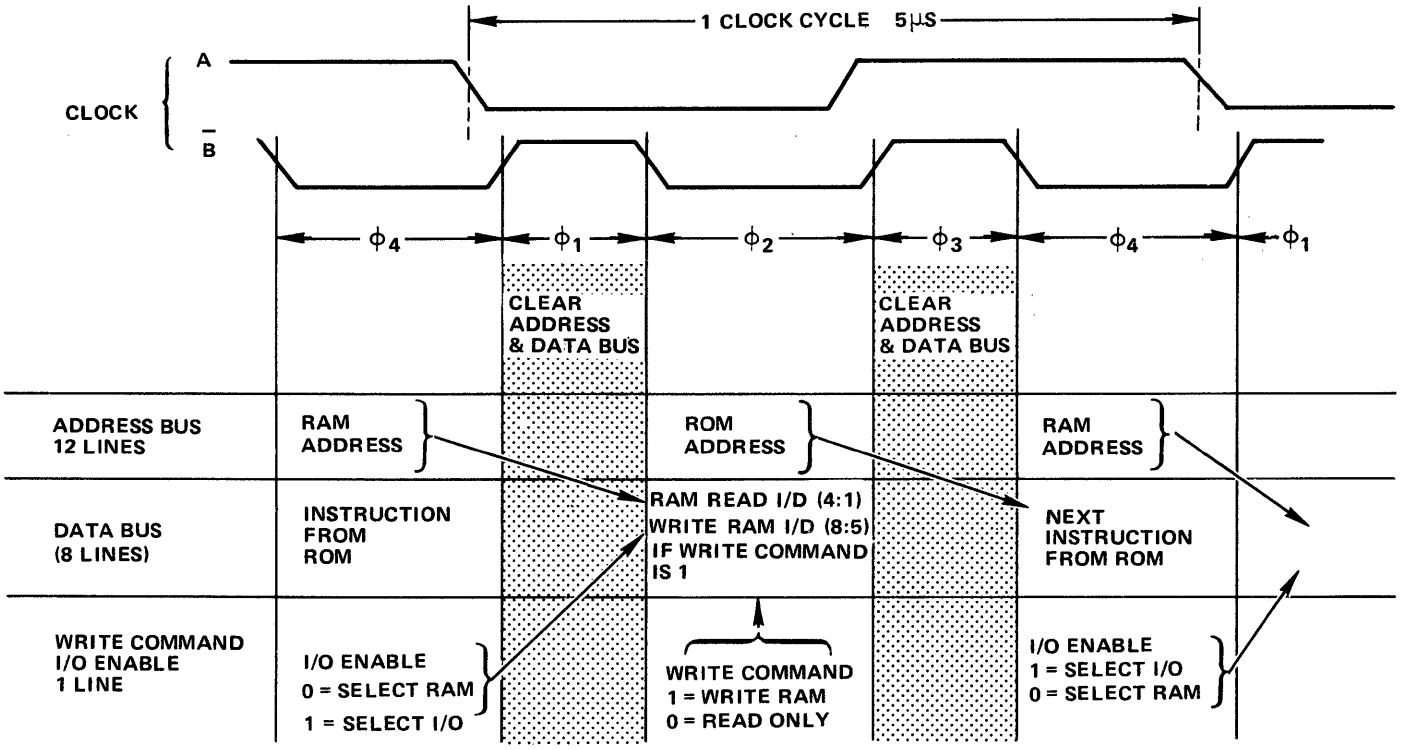


Figure 23. Parallel Processing System Basic Bus Timing

(b) Logic Levels

A negative logic notation is used in the PPS system. That is, a logic one (1) is defined as the most negative voltage, while a logic zero (0) is defined as the most positive voltage. For example, assuming a −17 volt power supply where $V_{DD} = -17$ volts and $V_{SS} = 0$ volts; a logic 0 is defined as ≥ -1.9 volts while a logic 1 is defined as ≤ -7.5 volts.

(c) Multiplex System Data Transfer

In addition to the power and clock signals there are 21 multiplexed lines interconnecting the CPU with ROM, RAM and I/O circuits. These lines are functionally grouped as follows:

12 parallel address lines
8 parallel data lines
1 write command and I/O enable line

The twelve address lines originate at the CPU and are time multiplexed within the CPU to provide direct addressing capability for up to 4096 locations on both the ROM and RAM. In addition to the twelve direct address lines, the ROM, P/N A05––, circuit has two chip select inputs and the RAM, P/N 10432, circuit has one chip select input. These chip select lines may be directly controlled by discrete outputs from CPU or I/O circuits for memory expansion without the need for auxiliary circuitry. Memory expansion is more fully explained in the description of the ROM and RAM. Like the address lines the eight data bus lines are time-shared lines from the CPU. During $\phi 2$ a logical "one" on the write enable line is interpreted by the RAM's as a write enable command and data on the bus will be written into RAM. The RAM is a non-destructive read-out device and, therfore, is always programmed to read; however, it must be instructed to "write." Because the 8 data lines are functioning as a dual 4-bit bidirection data bus during $\phi 2$, it is possible for RAM to read 4 bits from the designated address out to the data bus and, during the same cycle time, write 4 bits from the data bus into the designated RAM address location.

The same line providing the write command to RAM during $\phi 2$ time serves as an I/O enable signal during $\phi 4$ time of the input/output instruction (IOL). If the I/O enable is on (logical 1) at $\phi 4$ the RAM will be disabled during the next $\phi 2$ time, and the data bus will be used to transfer information between accumulator in the CPU and I/O circuits.

The input/output instruction (IOL) is a special application of the bus timing and requires two clock cycles and two successive ROM memory locations. During the first clock cycle the "IOL" instruction is received from ROM and decoded in the CPU. During the second clock cycle the I/O enable line will alert all the I/O circuits and at the same time an I/O address and command is transmitted from ROM turning on the selected I/O circuit. Data transfer between the selected I/O circuit and accumulator in the CPU will occur during $\phi 2$ of the next clock cycle.

A timing diagram of the IOL instruction is shown in Figure 24.

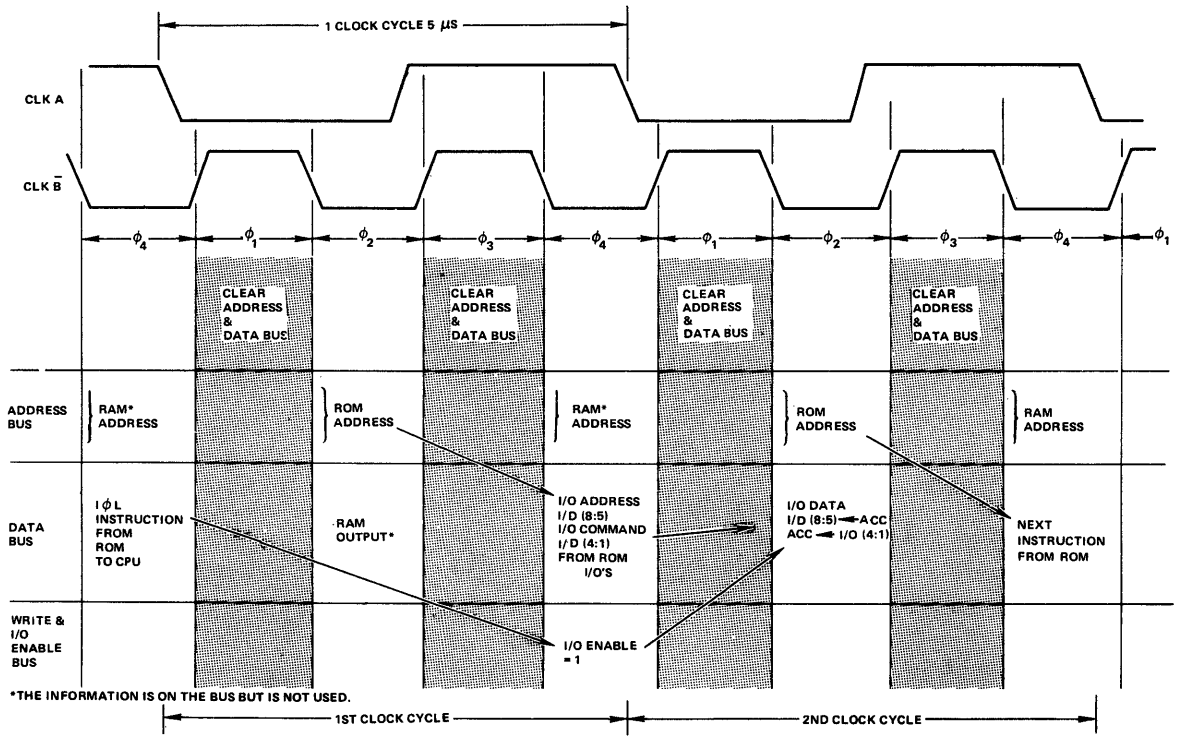


Figure 24. I/O Instruction PPS Timing.

INSTRUCTION LIST

The following pages provide a listing of the 50 instructions which can be used to control generation of ROM and RAM address as well as manipulation and transfer of data between the CPU and RAM and I/O. Definitions of symbology used in the instruction list is also provided such that a programmer can easily understand the instruction list and begin to visualize how the PPS may be used for a given application.

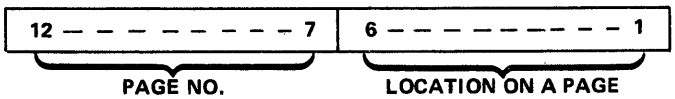
DEFINITIONS OF SYMBOLIC NOTATION

Symbols

A	Accumulator Register, A(4:1)
A/Bn	Line n of Address Bus
B	RAM Address Register, B(12:1)
C	Carry Link Flip-Flop
FF_1, FF_2	General Flip-Flop 1, General Flip-Flop 2
I	Instruction (Typically 8-bit Field)
I/Dn	Line n of Instruction/Data Bus
In	Byte n of Long Instruction (i.e. I_1 = 1st byte, I_2 = 2nd byte)
M	RAM Memory Contents Designated by Register B
m	General Numeric Designator, m = 1, 2, 3, . . .
n	General Numeric Designator, n = 1, 2, 3, . . .
P	ROM Program Counter Register, P (12:1)
BL	Lower Field of Register B (4:1)
BM	Middle Field of B Register B (8:5)
BU	Upper Field of B Register, B (12:9)
R(n)	Bit n of General Register R
R(m:n)	Bits m thru n of General Register R inclusive [e.g., R(12:7)]
SA	Upper Stack of Save Registers, SA(12:1)
SB	Lower Stack of Save Registers, SB(12:1)
W/IO	Write Command and I/O Enable Line
X	Secondary Accumulator Register, X(4:1)
Digit	Four Bit Field (sometimes referred to as Data or Character)
Byte	Eight Bit Field
Page	ROM Block of 64 Bytes (*)
← →	Replaces
⟷	Exchange
—	1's Complement (e.g., $\overline{A}$ is 1's complement of A)
V	Logical Inclusive OR
⊻	Logical Exclusive OR
Λ	Logical and
+	Algebraic Add
-	Algebraic Subtract

*A page is defined in the PPS as 64 ROM address locations. The page number is specified by the six (6) most significant bits of the 12-bit P register. The locations within a page are defined by the six (6) least significant bits.

P REGISTER



ARITHMETIC INSTRUCTIONS

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
AD	OB 0000 1011	Add (1 cycle)	The result of binary addition of contents of accumulator and 4-bit contents of the RAM currently addressed by B register, replaces the contents of accumulator. The resulting carry-out is loaded into C flip-flop.	C, A ← A+M
ADC	OA 0000 1010	Add with carry-in (1 cycle)	Same as AD except the C flip-flop serves as a carry-in to the adder.	C,A ← A+M+C
ADSK	O9 0000 1001	Add and skip on carry-out (1 cycle)	Same as AD except the next ROM word will be skipped (ignored) if a carry-out is generated.	C, A ← A+M Skip if C = 1
ADCSK	O8 0000 1000	Add with carry-in and skip on carry-out (1 cycle)	Same as ADSK except the C flip-flop serves as a carry-in to the adder.	C, A ← A+M+C Skip if C = 1
ADI	60-6E *0110 xxxx Except 65	Add immediate and skip on carry-out (1 cycle)	The result of binary addition of contents of accumulator and 4-bit immediate field of instruction word replaces the contents of accumulator. The next ROM word will be skipped (ignored) if a carry-out is generated. This instruction does not use or change the C flip-flop. The immediate field I(4:1) of this instruction may not be equal to binary 0000 or 1010 (See CYS and DC)	A ← A+[I(4:1)] Skip if carry-out = one I(4:1) ≠ '0000 I(4:1) ≠ 1010 See Note 3
DC	65 0110 0101	Decimal Correction (1 cycle)	Binary 1010 is added to contents of accumulator. Result is stored in accumulator. Instruction does not use or change carry flip-flop or skip.	A ← A+1010
		LOGICAL INSTRUCTIONS		
AND	OD 0000 1101	Logical AND (1 cycle)	The result of logical AND of accumulator and 4-bit contents of RAM currently addressed by B register replaces contents of accumulator.	A ← A∧M
OR	OF 0000 1111	Logical OR (1 cycle)	The result of logic OR of accumulator and 4-bit contents of RAM currently addressed by B register replaces contents of accumulator.	A ← A∨M
EOR	OC 0000 1100	Logical Exclusive-OR (1 cycle)	The result of logic exclusive-OR of accumulator and 4-bit contents of RAM currently addressed by B register replaces contents of accumulator.	A ← A∀M
COMP	OE 0000 1110	Complement (1 cycle)	Each bit of the accumulator is logically complemented and placed in accumulator.	A ← $\bar{A}$

*xxxx Indicates restrictions on bit patterns allowable in immediate field as specified in the symbolic equation description.

DATA TRANSFER INSTRUCTIONS

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
SC	20 0010 0000	Set Carry flip-flop (1 cycle)	The C flip-flop is set to 1.	C ← 1
RC	24 0010 0100	Reset Carry flip-flop (1 cycle)	The C flip-flop is set to 0.	C ← 0
SF1	22 0010 0010	Set FF1 (1 cycle)	Flip-flop 1 is set to 1.	FF1 ← 1
RF1	26 0010 0110	Reset FF1 (1 cycle)	Flip-flop 1 is set to 0.	FF1 ← 0
SF2	21 0010 0001	Set FF2 (1 cycle)	Flip-flop 2 is set to 1.	FF2 ← 1
RF2	25 0010 0101	Reset FF2 (1 cycle)	Flip-flop 2 is set to 0.	FF2 ← 0
LD	30-37 0011 0 _ _ _	Load Accumulator from Memory (1 cycle)	The 4-bit contents of RAM currently addressed by B register are placed in the accumulator. The RAM address in the B register is then modified by the result of an exclusive-OR of the 3-bit immediate field I(3:1) and B(7:5).	A ← M; B(7:5)←B(7:5)∀ [I(3:1)] See Note 3
EX	38-3F 0011 1 _ _ _	Exchange Accumulator and Memory (1 cycle)	Same as LD except the contents of accumulator are also placed in currently addressed RAM location.	A ↔ M B(7:5) ← B(7:5)∀ [I(3:1)] See Note 3
EXD	28-2F 0010 1 _ _ _	Exchange Accumulator and Memory and decrement BL (1 cycle) See Note 3	Same as EX except RAM address in B register is further modified by decrementing BL by 1. If the new contents of BL is 1111, the next ROM word will be ignored.	A ↔ M B(7:5) ← B(7:5)∀ [I(3:1)]; BL ← BL-1 Skip on BL=1111
LDI	70-7F 0111 _ _ _ _	Load Accumulator Immediate (1 cycle)	The 4-bit contents, immediate field I(4:1), of the instruction are placed in accumulator. (See Note below)	A ← [I(4:1)] See Note 3
LAX	12 0001 0010	Load Accumulator from X register (1 cycle)	The 4-bit contents of the X register are placed in the accumulator.	A ← X
LXA	1B 0001 1011	Load X Register from Accumulator (1 cycle)	The contents of the accumulator are transferred to the X register.	X ← A
LABL	11 0001 0001	Load Accumulator with BL (1 cycle)	The contents of BL register are transferred to the accumulator.	A ← BL
LBMX	10 0001 0000	Load BM with X (1 cycle)	The contents of X register are transferred to BM register.	BM ← X
LBUA	04 0000 0100	Load BU with A (1 cycle)	The contents of accumulator are transferred to BU register. Also, the contents of currently addressed RAM are transferred to accumulator.	BU ← A, A ← M

NOTE
Only the first occurrence of an LDI in a consecutive string of LDI's will be executed. The program will ignore the remaining LDI's and execute next valid instruction.

DATA TRANSFER INSTRUCTIONS (CONT)

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
XABL	19 0001 1001	Exchange Accumulator and BL (1 cycle)	The contents of accumulator and BL register are exchanged.	A ↔ BL
XBMX	18 0001 1000	Exchange BM and X (1 cycle)	The contents of BM register and X register are exchanged.	X ↔ BM
XAX	1A 0001 1010	Exchange Accumulator and X (1 cycle)	The contents of accumulator and X register are exchanged.	A ↔ X
XS	06 0000 0110	Exchange SA and SB (1 cycle)	The 12-bit contents of SA register and SB register are exchanged.	SA ↔ SB
CYS	6F 0110 1111	Cycle SA register and accumulator. (1 cycle)	A 4-bit right shift of the SA register takes place with the four bits which are shifted off the end of SA being transferred into the accumulator. The contents of the accumulator are placed in the left end of SA register.	A ← SA(4:1) SA(4:1) ← SA(8:5) SA(8:5) ← SA(12:9) SA(12:9) ← A
LB **	CO-CF 1st word 1100 ---- 2nd word from page 3 ---- ----	Load B Indirect (2 cycles)	Sixteen consecutive locations on ROM page 3 (I_2) contain data which can be loaded into the eight least significant bits of the B register by use of any LB instruction. The four most significant bits of B register will be loaded with zeros. The contents of the SB register will be destroyed. This instruction takes two cycles to execute but occupies only one ROM word. (Automatic return) (See Note below.)	SB ← SA, SA ← P P(12:5) ← 0000 1100 P(4:1) ← I1(4:1) BU ← 0000 B(8:1) ← [I2(8:1)] P ← SA, SA ↔ SB See Notes 3 and 4
LBL	00 1st word 0000 0000 2nd word ---- ----	Load B Long (2 cycles)	This instruction occupies two ROM words, the second of which will be loaded into the eight least significant bits of the B register. The four most significant bits of B (BU) will be loaded with zeros. (See Note below)	BU ← 0000 B(8:1) ← [I2(8:1)] See Note 3
INCB	17 0001 0111	Increment BL (1 cycle)	BL register (least significant four bits of B register) is incremented by 1. If the new contents of BL is 0000, then the next ROM word will be ignored.	BL ← BL+1 Skip on BL=0000
DECB	1F 0001 1111	Decrement BL (1 cycle)	BL register is decremented by 1. If the new contents of BL is 1111, then the next ROM word will be ignored.	BL ← BL-1 Skip on BL = 1111

NOTE

Only the first occurrence of an LB or LBL instruction in a consecutive string of LB or LBL will be executed. The program will ignore the remaining LB or LBL and execute the next valid instruction. Within subroutines the LB instruction must be used with caution because the contents of SB have been modified.

CONTROL TRANSFER INSTRUCTIONS

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
T *	80-BF 10-- ----	Transfer (1 cycle)	An unconditional transfer to a ROM word on the current page takes place. The least significant 6-bits of P register P(6:1) are replaced by six bit immediate field I(6:1).	P(6:1) ← I(6:1)
TM**	DO-FF * 1st word 11xx ---- 2nd word from page 3 ---- ----	Transfer and Mark Indirect (2 cycles)	48 Consecutive locations on ROM page 3 contains pointer data which identify subroutine entry addresses. These subroutine entry addresses are limited to pages 4 through 7. This TM instruction will save the address of the next ROM word in the SA register after loading the original contents of SA into SB. A transfer then occurs to one of the subroutine entry addresses. This instruction occupies one ROM word but takes two cycles for execution.	SB ← SA, SA ← P P(12:7) ← 000011 P(6:1) ← I1(6:1) P(12:9) ← 0001 P(8:1) ← I2(8:1) See Note 4 Note: I1(6:5)≠00
TL	50-5F 1st word 0101 ---- 2nd word ---- ----	Transfer Long (2 cycles)	This instruction executes a transfer to any ROM word on any page. It occupies two ROM words and requires two cycles for execution. The first byte loads P(12:9) with field I1(4:1) and then the second byte I2(8:1) is placed in P(8:1).	P(12:9) ← I1(4:1); P(8:1) ← I2(8:1)
TML	01-03 * 1st word 0000 00xx 2nd word ---- ----	Transfer and Mark Long (2 cycles)	This instruction executes a transfer and mark to any location on ROM pages 4 through 15. It occupies two ROM words and requires two cycle times for execution.	See Note 4 SB ← SA, SA ← P P(12:9) ← I1(4:1) P(8:1) ← I2(8:1) Note I1(2:1)≠00
SKC	15 0001 0101	Skip on Carry flip-flop (1 cycle)	The next ROM word will be ignored if C flip-flop is 1.	Skip if C = 1
SKZ	1E 0001 1110	Skip on Accumulator Zero (1 cycle)	The next ROM word will be ignored if accumulator is zero.	Skip if A = 0
SKBI	40-4F 0100 ----	Skip if BL Equal to Immediate (cycle)	The next ROM word will be ignored if the least significant four bits of B register (BL) is equal to the 4-bit immediate field I(4:1) of instruction.	Skip if BL = I(4:1)
SKF1	16 0001 0110	Skip if FF1 Equals 1 (1 cycle)	The next ROM word will be ignored if FF2 is 1.	Skip if FF1 = 1
SKF2	14 0001 0100	Skip if FF2 Equals 1 (1 cycle)	The next ROM word will be ignored if FF1 is 1.	Skip if FF2 = 1
RTN **	05 0000 0101	Return (1 cycle)	This instruction executes a return from subroutine by loading contents of SA register into P register and interchanges the SB and SA registers.	P ← SA, SA ↔ SB

*xx Indicates restrictions on bit patterns allowable in the designated bit positions in the instruction field as specified in the symbolic equation description.

** These instructions, with the exception of T * +1, cannot be used in ROM location 0000.

CONTROL TRANSFER INSTRUCTIONS (CONT)

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
RTNSK **	07 0000 0111	Return and Skip (1 cycle)	Same as RTN except the first ROM word encountered after the return from subroutine is skipped.	P ← SA , SA↔SB P ← P+1

INPUT/OUTPUT INSTRUCTIONS

Mnemonics	I/D Bus OP Code Hex & Binary	Name	Description	Symbolic Equation
IOL	1C 1st word 0001 1100 2nd word ---- ----	Input/Output Long (2 cycles)	This instruction occupies two ROM words and requires two cycles for execution. The first ROM word is received by the CPU and sets up the I/O Enable signal. The second ROM word is then received by the I/O devices and decoded for address and command. The contents of the accumulator inverted are placed on the data lines for acceptance by the I/O. At the same time, input data received by the I/O device is transferred to the accumulator inverted.	$\overline{A}$ → Data Bus A ← $\overline{\text{Data Bus}}$ I2 → I/O Device
DIA	27 0010 0111	Discrete Input Group A (1 cycle)	Data at the inputs to discrete. Group A is transferred to the accumulator.	A ← DIA
DIB	23 0010 0011	Discrete Input Group B (1 cycle)	Data at the inputs to discrete. Group B is transferred to the accumulator.	A ← DIB
DOA	1D 0001 1101	Discrete Output (1 cycle)	The contents of the accumulator are transferred to the discrete output register.	D O A ← A

SPECIAL INSTRUCTION

SAG	13 0001 0011	Special Address Generation (1 cycle)	This instruction causes the eight most significant bits of the RAM address output to be zeroed during the next cycle only. Note that this instruction does not alter the contents of the B register.	A/B Bus (12:5) ← 0000 0000 A/B Bus (4:1) ← BL(4:1) Contents of "B" remain unchanged

GENERAL NOTES

(1) The word "skip" or "ignore" as used in this instruction set means the instruction will be read from memory but not executed. Each skipped or ignored word will require one clock cycle time.

(2) The reference to ROM pages and locations are defined as the ROM address appearing on the A/B bus. During initial Power On the starting address is Page 0 Location 0 and is automatically incremented each clock cycle.

(3) Instruction ADI, LD, EX, EXD, LDI, LB and LBL have a numeric value coded as part of the instruction in the immediate field. This numeric value must be in complementary form on the bus. All of these immediate fields which are inverted are shown in brackets.

For example: ADI 1, as written by the programmer who wishes to add one to the value in the accumulator, is converted to $6E_{(16)}$=0110 [1110]; the bracketed binary value is the value as seen on the data bus.

If the programmer is using the Rockwell Assembler he does not have to manually determine the proper inverted value as the assembler does this for him.

(4) On all instructions which transfer the contents of P into SA, the P register has already been advanced to the next instruction location.

ELECTRICAL SPECIFICATIONS

OPERATING LIMITATIONS AND CHARACTERISTICS

Supply Voltage:

VDD = -17 Volts ± 5% (Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.) (Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies: 199 kHz or 256 kHz.

Operating Temperature (TA): 0°C to 70°C. (TA = 25°C unless otherwise specified.)

Storage Temperature: -55°C to 120°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . | VDD – VSS | = 27 Volts Maximum.

Input Voltage with Respect to VSS . . . . . -27 Volts Maximum.

Maximum Positive Voltage on any Pin . . . . . +0.3 Volts.

Product	Function	Symbol	Parameter	Limits Min	Limits Typ	Limits Max.	Unit	Test Conditions
Supply Current								VDD = -17.0V VSS = 0V
CPU		I_{DD}	Supply Current		13	14	mA	
ROM		I_{DD}	Supply Current		8	9	mA	OUTPUT LOAD
RAM		I_{DD}	Supply Current		9	10	mA	350 pF at 199 KHz
ROM/RAM		I_{DD}	Supply Current		8	9	mA	100 pF at 256 KHz
Clock		I_{DD}	Supply Current		19	21	mA	
GPI/O		I_{DD}	Supply Current		8	9	mA	
Input and Output Characteristics – System Bus								VDD = -17.0V± 5% VSS = 0V
CPU ROM RAM ROM/RAM GPI/O	Instruction/ Data Bus $I/D_1 - I/D_4$ $I/D_5 - I/D_8$ Address Bus $A/B_1 - A/B_{12}$ W/IO	V_{IH}	Input High Level	-1.5			V	
		V_{IL}	Input Low Level			1	V	
		V_{OH}	Output High Level	-1.0			V	
		V_{OL}	Output Low Level			2	V	
		CL	Load Capacitance			350	pf	199 kHz clock
						100	pf	256 kHz clock
Input and Output Characteristics – System External Interface and Strapping								VDD = -17.0V ± 5% VSS = 0V
CPU (Discrete Inputs)	DI-1 – DI-8	V_{IH}	V_{IN} High Level	-2.5			V	
		V_{IL}	V_{IN} Low Level			4	V	
CPU (Discrete Outputs)	DO-1 – DO-4	V_{OH}	V_{OUT} High Level	-1.6			V	I_L = 1.25 mA
		V_{OL}	V_{OUT} Low Level				V	Floating
RAM and GPI/O Straps	$SC_M - SC_N$	V_{OH}		-1.5			V	
		V_{OL}				-13	V	
GPI/O Inputs and Outputs	$IN_1 - IN_{12}$	V_{IH}	Input High Level	-1.5			V	
		V_{IL}	Input Low Level			-4.2	V	
	$OUT_1 - OUT_{12}$	V_{OH}	V_{OUT} High Level	-2.7			V	I_L = 2.7 mA,
		V_{OL}	V_{OUT} Low Level				V	Floating

DC AND OPERATING CHARACTERISTICS

Product	Function	Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
Input and Output Characteristics – Clock and Power On								VDD = -17.0V ± 5%
Clock	A, $\overline{B}$	V_{OH}	V_{OUT} High Level	-0.5			V	
		V_{OL}	V_{OUT} Low Level			-10		
	A (TTL)	V_{OH}	V_{OUT} High Level	-1.6V			V	With Recommended TTL Interface Can Drive 1 TTL Load
		V_{OL}	V_{OUT} Low Level	-5.6		–	V	
CPU	PO Power On	V_{IH}	Input High Level	-1.9				
		V_{IL}	Input Low Level			▷3		
	SPO Syncronized Power On	V_{OH}	Output High Level	-0.5				
		V_{OL}	Output Low Level			-9		
Capacitance								
CPU ROM RAM ROM/RAM GPI/O Clock	All Logic Inputs and Outputs	C_{IN}	Input Capacitance			6	pF	
		C_{OUT}	Output Capacitance			6	pF	
Off Input Resistance and Leakage Current								
ROM RAM ROM/RAM GPI/O Clock	All Logic Inputs and Outputs	R_{OFF}	Off Resistance	1 Meg.			Ω	
		I_R	Input Leakage Current			10	μA	
Interface on Resistances Outputs								
Clock	A (TTL)	R_{ON}	On Resistance			1,000	Ω	
CPU	Outputs $DO_1 - DO_4$	R_{ON}	On Resistance			1,250	Ω	
GPI/O	$OUT_1 - OUT_{12}$	R_{ON}	On Resistance			1,000	Ω	
Load Conditions								
Clock	A, $\overline{B}$	CL	Load Capacitance	50		400	pf	199 kHz
				50		100	pf	256 kHz
	A (TTL)	IOH	Output Current			2.7	mA	
CPU	Outputs $DO_1 - DO_4$	IOH	Output Current			1.25	mA	
GPI/O	$OUT_1 - OUT_{12}$	IOH	Output Current			2.7	mA	

NOTE: Input and output voltage levels indicated by the ▷ symbols vary as a function of | VDD | in accordance with the following equations. (The equations are applicable over the entire operating temperature range.)

▷1 V_{IL} = -(0.66 | VDD | - 4.16) Example: If VDD = -17.0V, V_{IL} = -7.06V

▷2 V_{OL} = -(0.66 | VDD | - 3.16) Example: If VDD = -17.0V, V_{OL} = -8.06V

▷3 V_{IL} = -(0.29 | VDD | + 8.32) Example: If VDD = -17.0V, V_{IL} = -13.25V

▷4 V_{IL} = -(0.29 | VDD | + 2.32) Example: If VDD = -17.0V, V_{IL} = 7.25V

SYSTEM INPUT AND OUTPUT TIMING

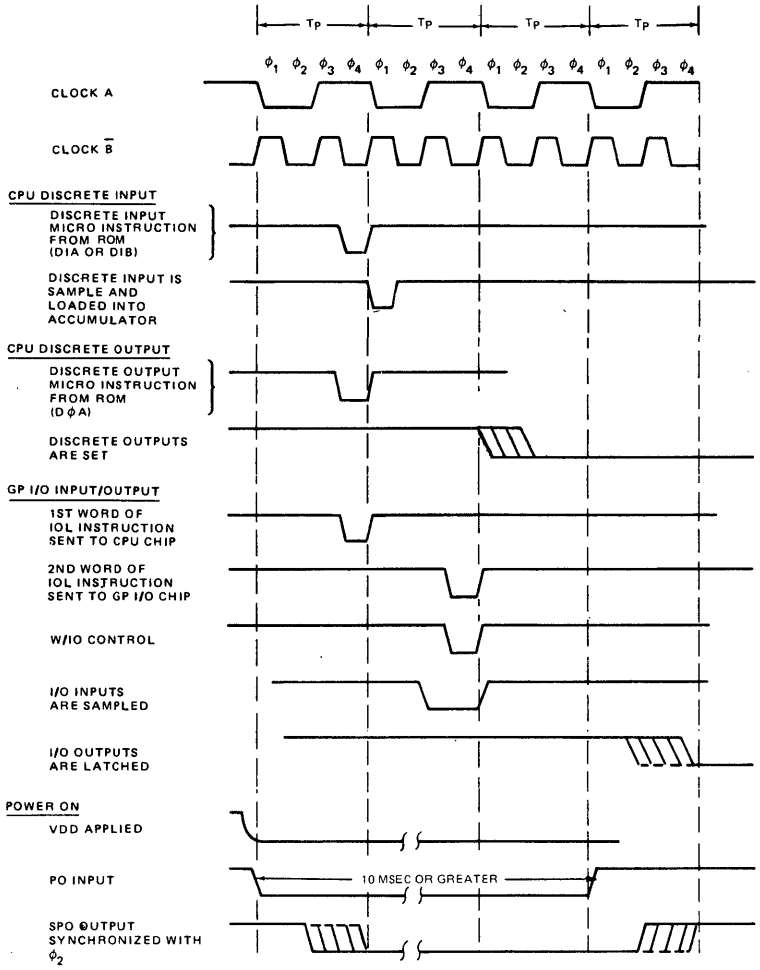


Figure 25. System Input and Output Timing.

AC CHARACTERISTICS

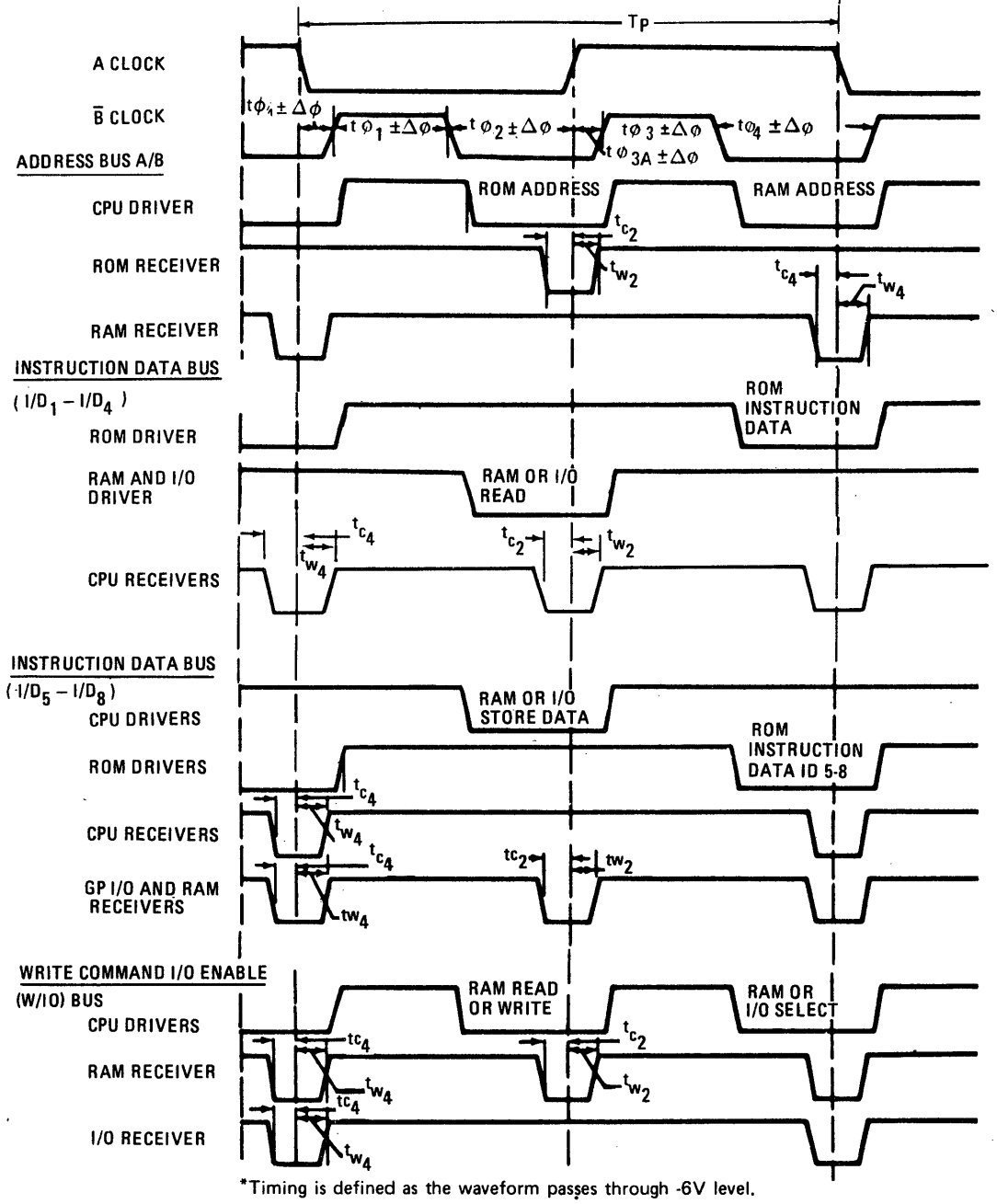
$T_A = 0^oC$ to $+70^oC$; $V_{DD} = -17V + 5\%$; $V_{SS} = 0V$

Symbol	Test	Min	Typ	Max	Units	Conditions and Comments
T_P	Timing period of clock		5.03		μsec	Clock select ÷ 18
			3.91		μsec	Clock select ÷ 14
$\Delta\phi$	Time variations of phase intervals		20	40	nsec	
	Time duration of phases 1, 2, 3, 4		1.26		μsec	Clock select ÷ 18
			978		nsec	Clock select ÷ 14
$t\phi_{1A} = t\phi_{3A}$	Time duration of phases 1A and 3A		279		nsec	Clock select ÷ 18
			279		nsec	Clock select ÷ 14
t_{c_2}	Phase 2 input charge time	150	200		nsec	Data must be stable
t_{c_4}	Phase 4 input charge time	150			nsec	Data must be stable
t_{w_2}	Window time phase 2	350			nsec	Data must be stable
t_{w_4}	Window time phase 4	350			nsec	Data must be stable
$t_{f_c} = t_{r_c}$	Clock fall and rise time	10		120	nsec	Load A = Load $\overline{B}$, which are between 50 and 100 pF

TIMING DIAGRAM *

A.C. CHARACTERISTICS
SYSTEM CLOCK PHASE

		φ4	φ1A	φ1	φ2	φ3A	φ3	φ4	φ1A	φ1
CLOCK TIMING RATIO	S18 = 1 (÷18)	1/18	4/18	4/18	4/18	1/18	4/18	4/18	1/18	4/18
	S14 = 1 (÷14)	1/14	3/14	3/14	3/14	1/14	3/14	3/14	1/14	3/14
	S12 = 1 (÷12)	1/12	2/12	3/12	3/12	1/12	2/12	3/12	1/12	2/12



*Timing is defined as the waveform passes through -6V level.

Figure 26. Timing Diagram.

System Bus Load vs Clock Frequency

The PPS is designed to operate with a recommended clock frequency of about 199 kHz (3.58 MHz ÷ 18). Operating at this frequency the multiplex bus interface circuitry is designed to drive a system with capacity load of up to 350 pf.

For clock frequencies above 199 kHz, the multiplex bus drive capability must be derated. At 256 kHz (3.58 MHz ÷ 14) the maximum allowable system bus load must not exceed 100 pf.

CUSTOMER SUPPORT – GENERAL

GENERAL

Rockwell provides complete support for customers in the form of technical assistance, training seminars, complete documentation, programming software, and development and testing hardware. The related documentation, software, and supporting hardware are described in the following paragraphs.

CUSTOMER SUPPORT – SOFTWARE

SUPPORT SOFTWARE

Standard programs are available to minimize program development time. Complete programs for program development using timeshared computer facilities from either General Electric or Tymshare Corp. are also available. There is an Assembler Program which allows you to write programs directly from mnemonic codes. There is a Simulator Program which is a model of the PPS-4 CPU that enables you to verify the operation of the program before it is committed to firmware. And, there is an Output Program that provides you with output format options that include both punch cards and punch paper tape, and code formats allow direct compatibility with mask programmable ROMs, laser encodable SOS ROMs, and PROMs, or the new Applied Computer Technology Company's PPS Assemulator. (The Assemulator is a new PPS development tool that functions as both a software assembler and hardware emulator.) Various software items are described in the following listing.

Product	Description	Language	Availability
PPS-Cross Assemblers	Programs to convert PPS-4 assembly language to microprocessor machine code. Assembly language is fully symbolic and symbol cross referencing is provided together with diagnostics of programming errors. Special assembler features are provided to enable efficient use of unique architectural features of the PPS microprocessors.	Fortran IV	Now
PPS Simulators	Programs to simulate execution of PPS-4 programs. Simulators are interpretive and provide bit-for-bit duplication of microprocessor instruction executing timing, register contents, etc. Direct user control over execution conditions; RAM/register contents, interrupts, I/O data, etc., is provided.	Fortran IV	Now
PPS Output Formatter	Program to produce punched card/tape versions of assembled PPS-4 programs in formats compatible with any of the following microprogram storage media: (1) PPS mask encodable ROM's, (2) laser and mask encodable SOS ROM's, (3) PROMs, (4) PPS-4 MP Assemulator*, (5) PPS-4ME Emulator, (6) Rockwell's EAROM loader/ROM Emulator, and (7) Scientific Micro System's 1000A ROM Emulator.	Fortran IV	Now
PPS Macro/ Subroutine Libraries	Extensive library of PPS-4 Macros/subroutines which can be assessed directly from the timesharing systems and included in user programs. The libraries include decimal arithmetic functions, as well as bit manipulation routines and allow the PPS programmer to efficiently program at a higher language level.	PPS-4 Assembly Language	PPS-4 Now PPS-8 1975

*These products are manufactured by Applied Computer Technology, Inc., the term "Assemulator" is a trademark of this company.

NOTE: The above support software is available for use via the following computer timesharing systems:

1. General Electric Information Service Mark III System
2. Tymshare Incorporated TYMCOM-X System

The Fortran source decks for the above systems and for the IBM 360 TSO System are available for purchase. The Fortran source deck of the assembler program for several popular minicomputers is also available.

CUSTOMER SUPPORT – PPS-4 DOCUMENTATION

PPS-4 DOCUMENTATION

The PPS is supported by a complete and comprehensive set of documents. These documents are continually updated to incorporate additional data and/or reflect new capabilities or techniques. The supporting documents are listed below:

TITLE	DOCUMENT NO.
PPS-4 Basic Devices, Data Sheet	29003N11
Installation of 42-Lead Plastic Package	29000N32
MOS/ROM Card Format, Procedure	29000N31
Bus Interface, Data Sheet	10738N11
GPKD, Data Sheet	10788N11
Printer Controller, Data Sheet	10789N11
MNOS Non-Volatile RAM, Data Sheet	10439PN10
EAROM, Data Sheet	10443N10
GPI/O, Application Notes	10696N22
Evaluation Modules, Product Description	29004N41
Programmer's Reference Manual	29001N20
Programmer's Ref. Manual, Supp. No. 1	29001N21
Tymshare Timeshare Operating Manual	20992N20
GE Timeshare Operating Manual	29004N20
ROM Emulation for Microprogram Development, Application Notes	29003N22
1200 BPS TDI, Data Sheet	20371N10
PPS-4 Applied to Electronic Weighing Scale, Application Notes	2518-D-23

CUSTOMER SUPPORT – HARDWARE

SUPPORT HARDWARE

The user may select a complete set of breadboarding (PPS Evaluation Modules) and support equipment from a wide variety of support equipment described in the following paragraphs. The various support equipment and methods of using the equipment are under continuous development at Rockwell and associated equipment companies in order to minimize costs, further reduce development time, and to simplify processes.

PPS Support Systems Produced by Rockwell

ITEM	FUNCTION	IN USE
PPS EAROM Programmer/ ROM Emulator	Provides for programming a single EAROM or an EAROM module from paper tape or from an integral Hex keyboard and display. EAROMs are electrically eraseable and, therefore, need not be removed from the module or socket to be erased and reprogrammed. Contains integral RAM buffer for one EAROM to permit editing of of any EAROM. May also be used as a ROM emulator. Optional expansion capability to interface with modem and cassette will be available at a later date.	1st QTR 1975
PPS-4 Device Tester and Adapters	Tests all the MOS/LSI devices used in the PPS-4. A functional (not mockup) test is performed on each circuit. The tester provides fast, thorough, automatic testing of the devices in the dynamic mode.	4th QTR 1974

Design Aid Equipment/Systems Produced by Other Companies – For Rockwell Microcomputers

The following are complete PPS-4 debug equipment available from Applied Computing Technology, Incorporated, 17961-F Sky Park Circle, Irvine, California, 92707.

ITEM	FUNCTION	IN USE
PPS-4 MP Assemulator	A self-contained PPS-4 microcomputer system with resident assembler and utility program, together with a debug console and direct interface with an ASR-33 TTY. The user's program is stored in PPS-4 RAM and can be modified directly by the user from the ASR-33. Debug features include trap, single instruction step, halt, and address and instruction/ data monitoring/snapshot. Provides 24 fully buffered I/O channels for connecting to external system. A PROM programmer option is available.	Now
PPS-4ME Emulator	A complete PPS-4 microcomputer system with resident utility program and programmer console (keyboard, tape reader, display and controls) for complete PPS-4 system debug. The user's program is stored in PPS-4 RAM and can be modified directly by the user from the console keyboard. Debug features include trap, halt, address and instruction/ data monitoring/snapshot, and single step.	Now

EVALUATION MODULES

The PPS Evaluation Modules provide an efficient and fast method of assembling a breadboard utilizing Rockwell's Parallel Processing System. There are seven different PPS Evaluation Modules of which the Processor Module is the basic or key module. The Processor Module is a printed circuit card containing all the necessary components of a PPS set including a crystal controlled clock generator circuit, power-on initialization circuit, one 10660 CPU, two 10432 RAMs, and two 10696 I/Os. That is, it contains everything except the ROM. The content of the ROM is the system program, is developed by the customer, and is, therefore, unique to each product and application

A typical PPS evaluation system is shown in Figure 28. All pertinent signal, control, address, data, and I/O lines connect to each board. Note that either a customer furnished ROM Emulator or a PROM Evaluation Module can be used for program development. If a ROM Emulator is used, then the address and data bus go to the PPS Bus/TTL Interface Module for converting the PPS MOS dynamic signals to TTL static signals. This output signal conversion allows the user to implement the ROM Emulator with an in-house minicomputer memory or memory system specifically designed to be used for microprogram development. Details of using the PROM Evaluation Module for developing a program are covered in Rockwell International Publication No. 29004N41. The following PPS Evaluation Modules are available and are described in publication 29004N41.

Evaluation Modules	Part No.
PPS-4 Processor Module	20102D02
PPS Bus to TTL Interface Module	20102D27
PROM Module	20102D33
RAM Module	20102D17
SOS/ROM Module	20102D30
MOS ROM Module	20102D19
General Purpose I/O Module	20102D36
PPS EAROM Module *	

The development of a microcomputer program is much like the development of a general purpose computer program. That is, the machine language mnemonics must be understood, the problem must then be defined, an initial program listing is compiled, and then – with the aid of a computer – the program is tested, debugged and finally released for running.

Thus, a user of PPS must first define the product program problem; compile a listing with the aid of Rockwell's PPS assembler and simulation computer program (available through General Electric Co. or Tymshare, Inc. international timesharing networks); test the program with the aid of a ROM emulator and Rockwell's PPS Evaluation Modules; and finally, when the microprogram has been proven and demonstrated, submit the ROM patterns to Rockwell for conversion to a MOS ROM such as the A05--. This sequence is necessary since each individual ROM is unique to, and maintains the integrity of, a specific application.

Rockwell's PPS Processor Evaluation Module and associated software, as defined below, is available at $500 each ($550 outside of U.S.A.). Send P.O. to PPS Product Marketing, RC01, D/724 Manager, Rockwell Microelectronics, P.O. Box 3669 (3430 Miraloma Ave.), Anaheim, CA 92803.

*Available 1st Qtr 1975

BASIC PPS EVALUATION KIT

PPS-4 Processor Module

Part Number: 20102D02

Board Size – – 5" x 7"

System Components on Board

1	10660 CPU
2 ea	10432 RAM
2 ea	10696 General Purpose I/O
1	10706 Clock and Crystal Automatic Power Reset

System Clock

199 kHz	Crystal Controlled
5 sec	Instruction Cycle

Power Requirements

17 volts + 5%

0.060 Amps Typical

Board Mating Connector

Sylvania, PN 6AC AO-X7-120-0
Winchester, PN HW 50D0-111
Viking PN 3VH50/1CND

Supporting Software

Programmer's Reference Manual Pub No. 29001-N20 and N21

Provides program aids

ROM Emulator Interface

Provides schematics for interfacing to ROM emulator

PPS Applications Notes Pub No. 29003-N21

Provides general systems information

PPS-4 Microprogram Development Pub No. 29002-N20 and 29004-N20

Operation Manuals for Assembler and Simulator Programs using General Electric or Tymshare Timesharing Computer Services.

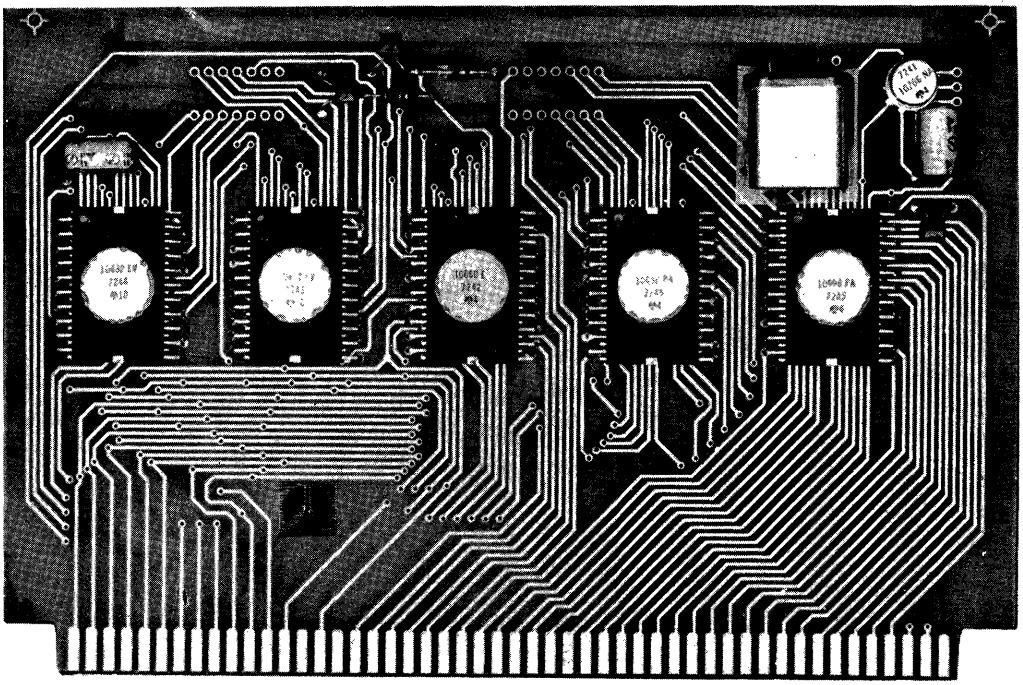


Figure 29. PPS-4 Processor Evaluation Module.

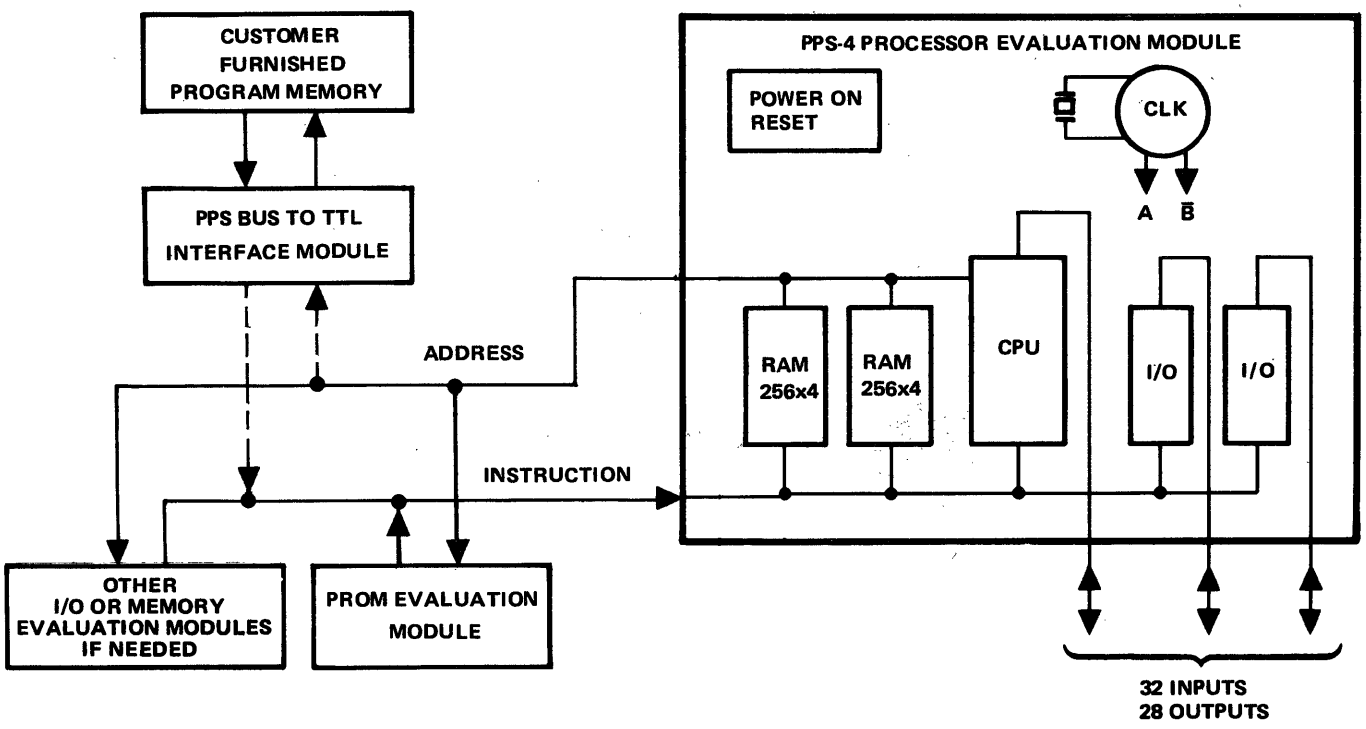
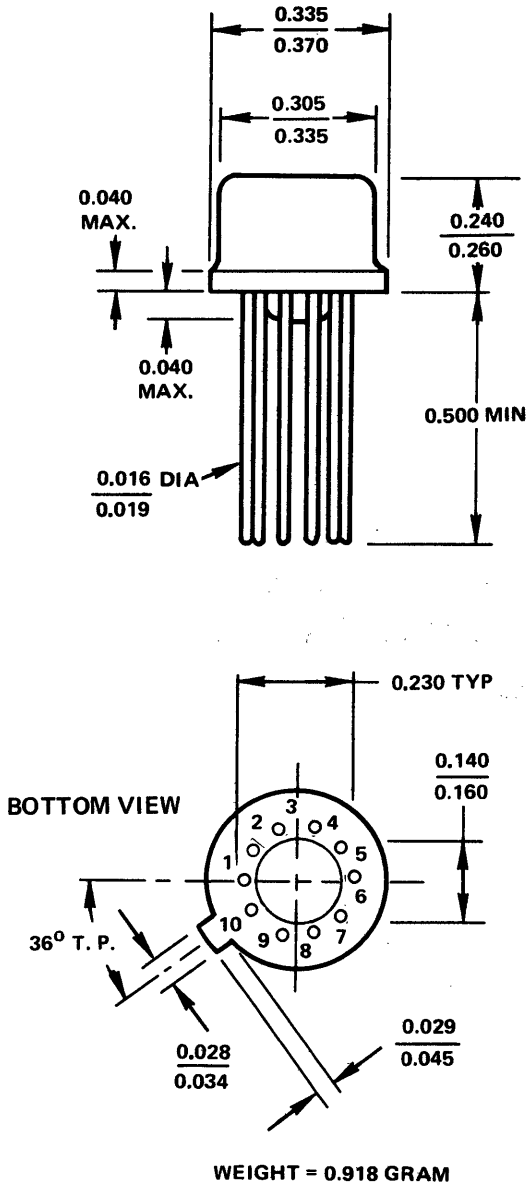


Figure 28. PPS Evaluation System.

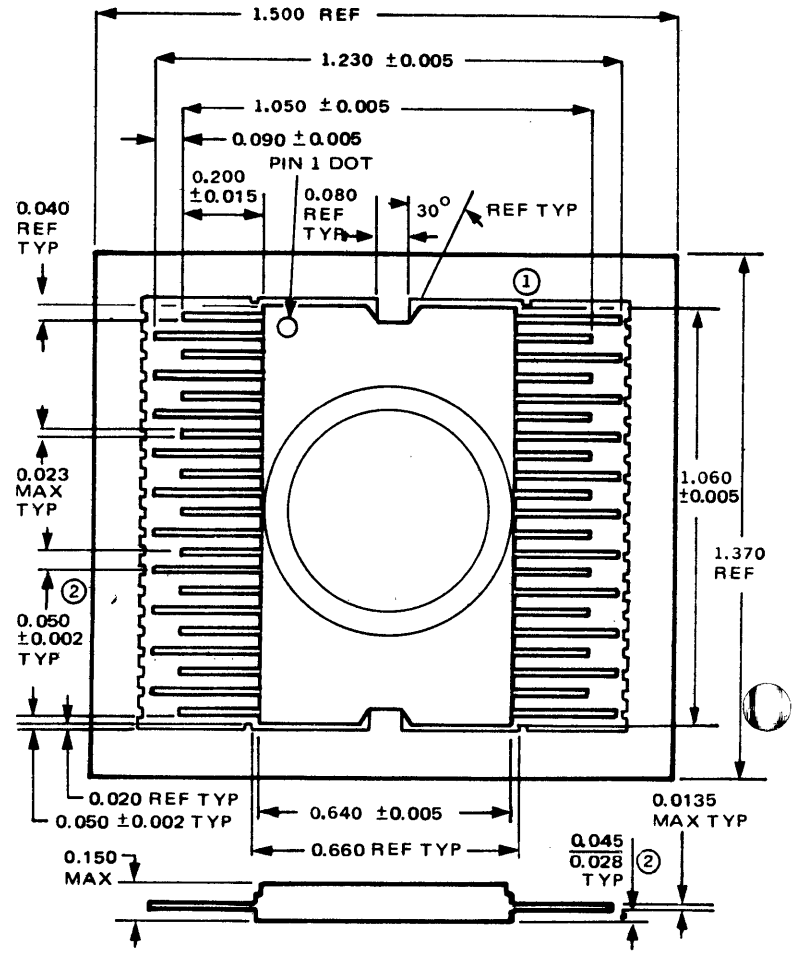
STANDARD PACKAGES

TO 100 PACKAGE



WEIGHT = 0.918 GRAM

STANDARD 42 LEAD PACKAGE



1. BURRS UP TO 0.005" MAY OCCUR ON LEAD ENDS
2. TOOL HOLES IN LEAD FRAMES MAY BE FILLED WITH SOLDER
(1) 3. STUBS ON LEAD FRAME OPTIONAL (TYPICAL 4 PLACES)
(2) 4. DIMENSIONS ONLY APPLY WHERE LEADS LEAVE BODY

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Rockwell International

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July 1974

DATA SHEET

PARALLEL PROCESSING SYSTEM (PPS-4) MICROCOMPUTER

PPS-4 BASIC DEVICES' SUPPLEMENT

EVALUATION AND DEVELOPMENT MODULES

INTRODUCTION

This document is a supplement to PPS-4 Basic Devices Data Sheet, Document No. 2519-D-13. This supplement provides a detailed description of each of the seven PPS-4 Evaluation and Development modules. These modules have been designed to provide a family of PPS circuits which may be quickly and efficiently combined into various configurations to simulate or duplicate proposed microcomputer systems. Using these modules, an equipment designer can develop a real microcomputer; interface it with the equipment in development; and readily make any changes required in the equipment, microcomputer, interfacing, or programming.

Any or all of Evaluation and Development modules described in this supplement may be purchased at a nominal cost by contacting the nearest Rockwell International Device Division office as indicated below.

Information contained in this supplement is extracted from the PPS-4 Evaluation and Development Modules Data Sheet, Document No. 29004 N41. Data Sheet 29004 N41 is provided with purchase of Evaluation and Development modules or the Data Sheet may be purchased separately for $3.00

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PPS PROCESSOR MODULE (P/N 20102 D02)

INTRODUCTION

The PPS Processor Module (P/N 20102 D02) is the primary module in a series of modules developed by Microelectronic Device Division for new product development utilizing the Parallel Processing System (PPS).

The PPS Processor Module contains the basic components of a PPS system, i.e. clock generator, power-on initialization circuit, central processor, random access memory, and general purpose input/output. The designer has only to select an appropriate SOS-ROM Module (P/N 20102 D30), ROM Module (P/N 20102 D19), PROM Module (P/N 20102 D33), or other writable control store for program storage in order to be ready to configure a unique product. In addition, by adding RAM Modules (P/N 20102 D17), General Purpose I/O Modules (P/N 20102 D36), power source, and keyboard/display, the designer can greatly increase the flexibility of the prototype product.

DESCRIPTION

The PPS Processor Module consists of a 5 X 7 inch plug-in circuit card with all parts interconnected and ready for use. Figure 1 is a block diagram of the PPS Processor Module and shows the PPS circuits and main data flow paths. These include a power-on initialization circuit, a Clock Generator (P/N 10706) and 3.579545 MHz crystal, a Central Processing Unit (CPU) (P/N 10660), two Random Access Memories (RAM) (P/N 10432), and two General Purpose Input/Outputs (GPI/O) (P/N 10696).

Any of the other evaluation modules may be bused to the PPS Processor Module, term-to-term. To facilitate this interconnection, the PPS Processor Module power initialization signals (SPO and PO), clock A and B signals, address bus (A/B) lines, instruction/data bus (I/D) lines, write input/output line (W/IO), power inputs, and ground lines are accessible on card edge pins. These pin connections are common on all evaluation modules.

Additional lines consist of eight discrete CPU inputs (DIA1-DIA4 and DIB1-DIB4), four discrete CPU outputs DO1-DO4, twenty-four general purpose inputs, and twenty-four general purpose outputs (GPI/O). These lines are all connected to PPS Processor module printed circuit card edge pins.

The PPS Processor Module functions at either of two clock frequencies, 199 kHz or 256 kHz; however, 199 kHz is the recommended operating clock frequency when used with PPS circuits. The clock frequency is selected by making appropriate strap connections on the module. For the recommended clock frequency of 199 kHz, place straps S12 and S14 at VSS and strap S18 at VDD (the processor module circuit board is printed in this configuration). For 256 kHz output, place straps S12 and S18 at VSS and S14 at VDD.

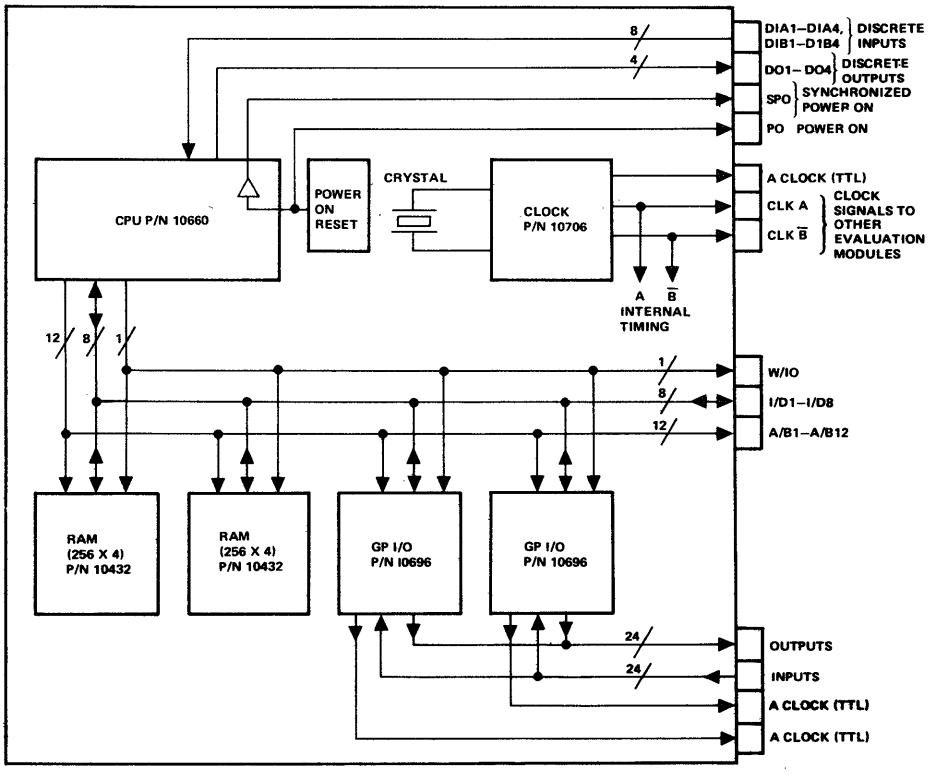


Figure 1. PPS Processor Module Block Diagram

PPS BUS TO TTL INTERFACE MODULE (P/N 20102 D27)

INTRODUCTION

When designing a new product around the PPS, the wide range of applications to which the PPS can be adapted may make it necessary to interface special memory circuits directly to the PPS Processor Module address and data buses. This is easily accomplished with the PPS Bus to TTL Interface Module (P/N 20102 D27) without developing additional external discrete logic. The PPS Bus to TTL Interface Module incorporates two bus interface circuits (P/N 10738) and TTL drivers which provide timing, impedance matching, and logic level interfacing between the PPS bus functions and TTL static memories, core, or other special type circuits. Each of the 12 TTL drivers provides a fan-out capability of up to 30 standard TTL loads.

DESCRIPTION

The PPS Bus to TTL Interface Module consists of a 5 x 7-inch plug-in circuit card with all parts interconnected and ready for use. Figure 2 is a block diagram of the PPS Bus to TTL Interface Module and shows the circuits and main data flow paths. The main circuits include two Bus Interface Circuits, 12 TTL Drivers, and 8 TTL Data Bus Buffers. In addition to the availability of the TTL address and instruction data lines on the card edge pins, a 24-pin socket is located on the card which provides access to these same points.

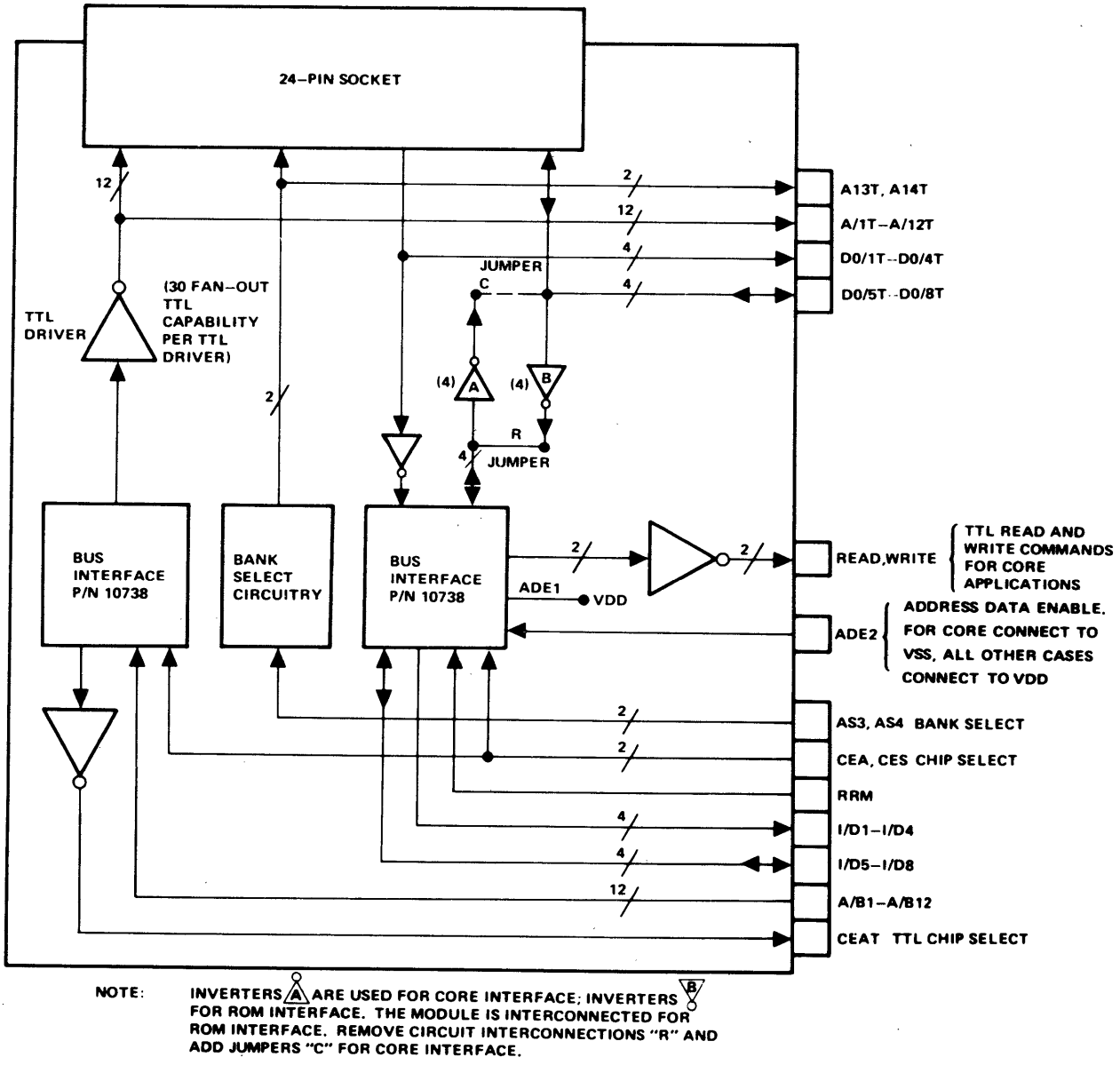


Figure 2. PPS Bus to TTL Interface Module Block Diagram

PPS PROM MODULE (P/N 20102 D33)

INTRODUCTION

The design of a custom PPS application for a new product may require the use of a Programmable Read Only Memory (PROM). Microelectronic Device Division has developed a PROM Module (P/N 20102 D33) for use with the PPS Processor Module that accepts up to 16 PROM (256 x 8) chips. With 16 PROMs installed, 4096 X 8-bit words of storage are provided on one module. The user can determine the amount of programmable read only memory required, and then install either the National MM5203 or Intel 1702 erasable PROMs. In addition, a maximum of four PROM Modules may be implemented into a system using external control of module select lines AS3 and AS4 for a total of 16K words of program storage. The PROMs that are selected for use must have an access time less than 1 microsecond. Address and data interface to the PPS are provided by two bus interface circuits. A 4-to-16 line decoder translates the four MSBs of the address to select one of the 16 PROMs. The eight LSBs of the address are used to select one of the 256 words on the addressed PROM.

A further advantage of the PROM Module is that it may be utilized as a RAM look-up table by appropriate strapping. This strapping results in the PROM Module responding to the RAM read phase of the clock. Therefore, fixed data may be stored, eliminating the need to reload constants and table information after power cycling. In this mode, only half of the PROM storage is utilized, for a total of 4096 X 4-bit words.

NOTE

Any PROM device used with the PPS-4 must have an access time of less than 1 microsecond.

DESCRIPTION

The PROM Module consists of a 5 x 7-inch plug-in circuit card with all parts interconnected and ready for use. Figure 3 is a block diagram of the PROM Module and shows the circuits and main data flow paths. The main circuits include two bus interface circuits (P/N 10738), a 4-to-16 line decoder, and 16 sockets for PROM installation.

The address bus (A/B1 through A/B12) and instruction/data bus (I/D1 through I/D8) are common to the pin locations of the address and instruction/data buses of the PPS Processor Module, facilitating simple interconnection of the modules for product development.

The expansion of the PPS system PROM memory capacity to up to 16K words in 4K steps is accomplished by adding PROM Modules, making appropriate strap connections, and then selecting the appropriate address logic. The PROM Module is prewired for logical "0" for the AS3 and AS4 address selecting the first 4K of PROM. For a logical "1" selection of AS3 or AS4, the etched circuit marked "0" is cut and then jumpered in the logical "1" position.

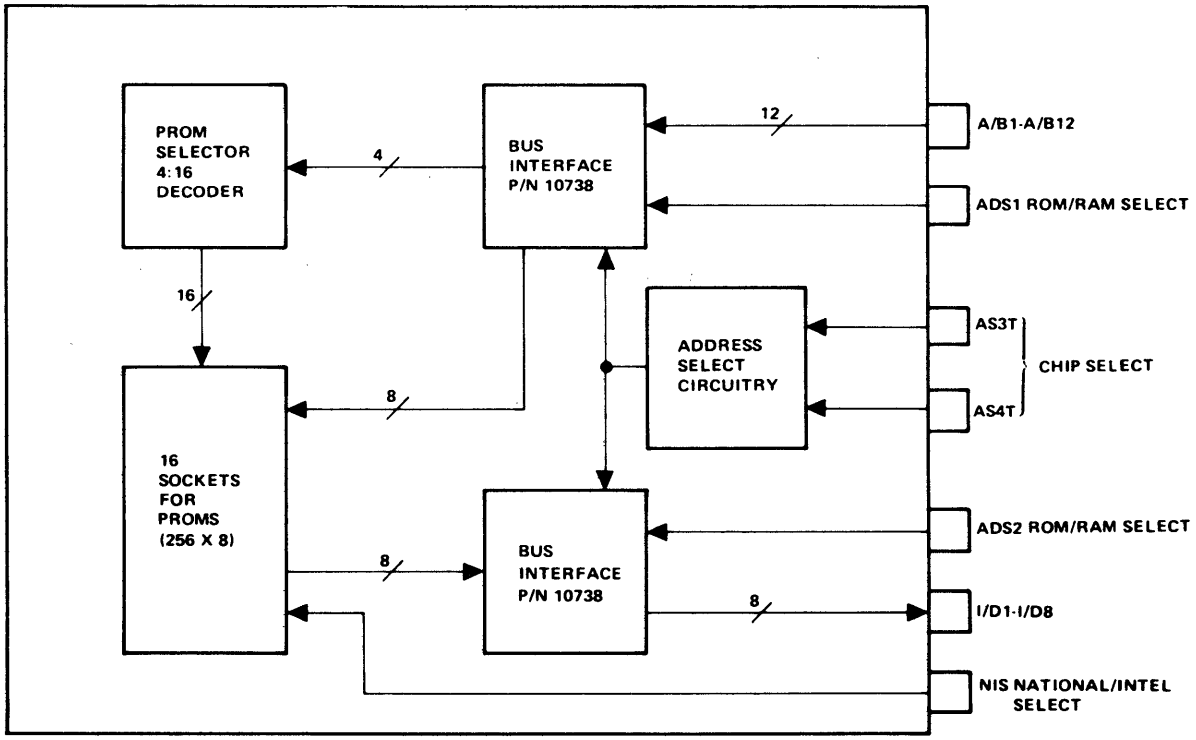


Figure 3. PPS PROM Module Block Diagram

PPS MOS - ROM MODULE (P/N 20102 D19)

INTRODUCTION

The Microelectronic Device Division PPS MOS-ROM Module (P/N 20102 D19) is designed to provide the user with a method of prototyping with or testing MOS-ROMs which have been encoded by the Microelectronic Device Division to the customer's specifications.

All necessary interconnection circuitry for mounting and interfacing up to eight ROM chips (P/N A05——) to the PPS Processor Module or other PPS Modules is included on the MOS-ROM Module. Eight ROM chips provide 8K 8-bit words of ROM memory. Addressing in banks of 4K words is possible using the CPU or GPI/O outputs to control bank select lines AS3 and AS4.

When a read only RAM configuration is required to allow read-out of constants and code conversions, the ROM may be encoded to read out during RAM time 02. Input line A11X is connected to a discrete output and is used as part of the address for the read only RAM configuration to select the upper or lower 4-bit word storage sections of the ROM.

DESCRIPTION

The MOS-ROM Module consists of a 5 x 7-inch plug-in circuit card with all parts interconnected and ready for use. Figure 5 is a block diagram of the MOS-ROM Module and shows the circuits and main data flow paths.

The address bus (lines A/B1 through A/B12) and instruction/data bus (lines I/D1 through I/D8) are common to the pin locations of the address and instruction data buses of the PPS Processor Module to facilitate simple interconnection of the modules during product development. For further information on the MOS-ROM chips refer to the PPS-4 data sheet, Pub. No. 2519-D-13-(311).

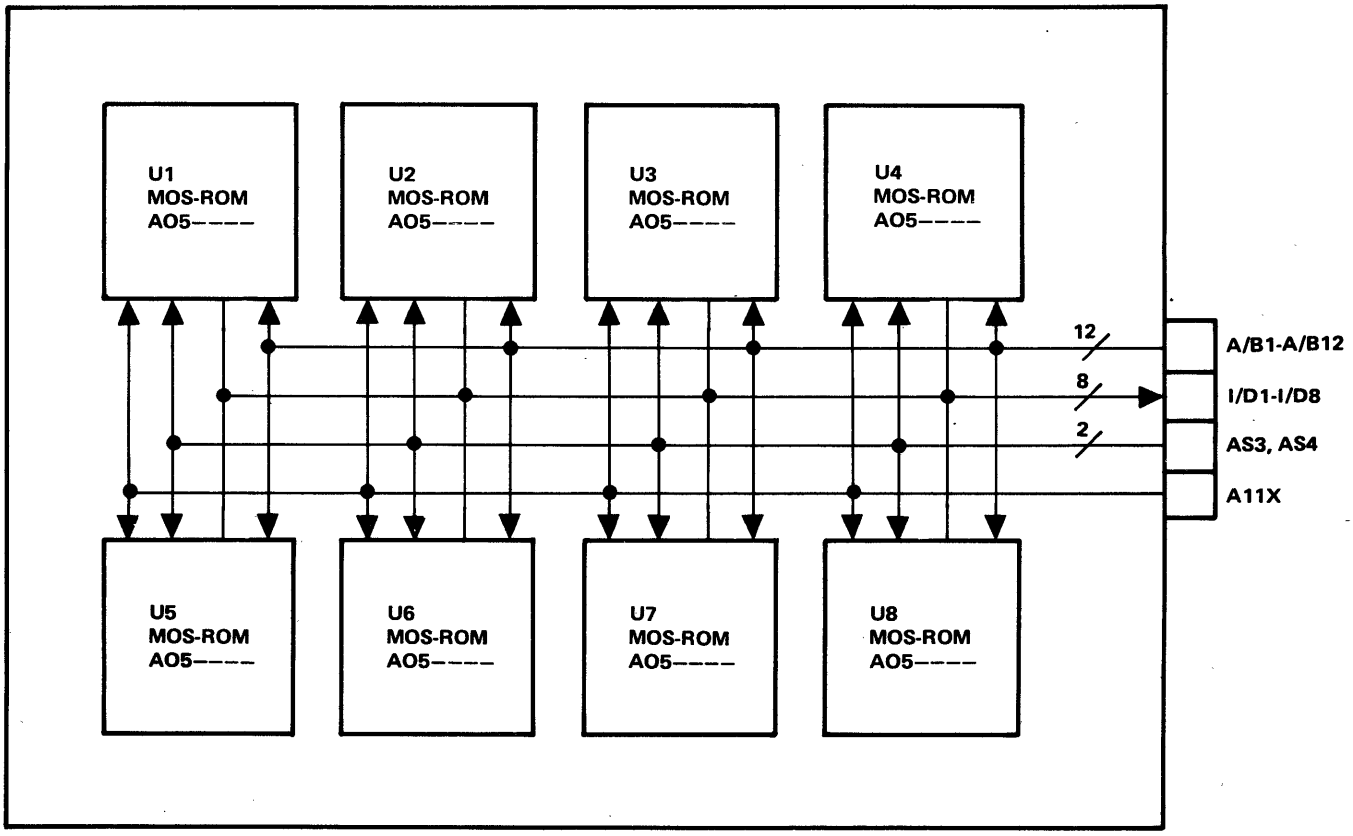


Figure 5. PPS MOS-ROM Module Block Daigram

PPS SOS - ROM MODULE (P/N 20102 D30)

INTRODUCTION

The Microelectronic Device Division SOS-ROM Module (P/N 20102 D30) is a 5 x 7-inch plug-in board providing mounting and interface connections for implementing up to 2048 X 8 bits of read only memory in the PPS system. The SOS-ROM's (P/N 15900 NB) may be configured as a 1024 X 8-bit memory by installing two SOS-ROMs on the SOS-ROM Module. In addition, strapping pins are available to configure the SOS-ROM Module so that it will respond during the RAM read phase, providing either 1024 X 4-bit or 2048 X 4-bit read only RAM for table look-up.

All interfacing circuits are provided on the SOS-ROM Module. The user purchases only the number of SOS-ROM chips required. One, two or four chips may be utilized, depending upon the designer's program requirements. The SOS-ROMs can be Laser encoded to specifications within five* days of receipt by Microelectronic Device Division of a deck of punched cards containing the desired codes. Laser encoding provides reliable devices, fast and inexpensive prototype work in low volume production. The SOS-ROM may also be mask encoded for low cost quantity production runs.

DESCRIPTION

The functional parts of the SOS-ROM Module are shown in the block diagram in Figure 4. All common signal lines, such as the address bus A/B1 through A/B12 and instruction/data bus I/D1 through I/D8, are pin compatible with the PPS Processor Module, which results in simple interconnection of the PPS system. The AS3 and AS4 straps allow the PPS system to be developed with up to 16K words (eight SOS-ROM Modules) or ROM using bank selection. If only one SOS-ROM Module is used, no additional strapping is required.

To utilize the Microelectronic Device Division SOS-ROM Module as either a ROM or a read only RAM make either of the following connections:

1. For ROM operation, connect ADS1 and JI-4 (RRM) to VSS, and connect ADS2 to VDD.

2. For read only RAM operation, connect ADS1 to VDD, ADS2 to VSS, and J1-4 (RRM) to PPS Processor Module J1-2 (W/IO bus).

Refer to Data Sheet Number 15900 N11 for a detailed description of the SOS-ROM chip and encoding procedures.

* Delivery is subject to change without notice.

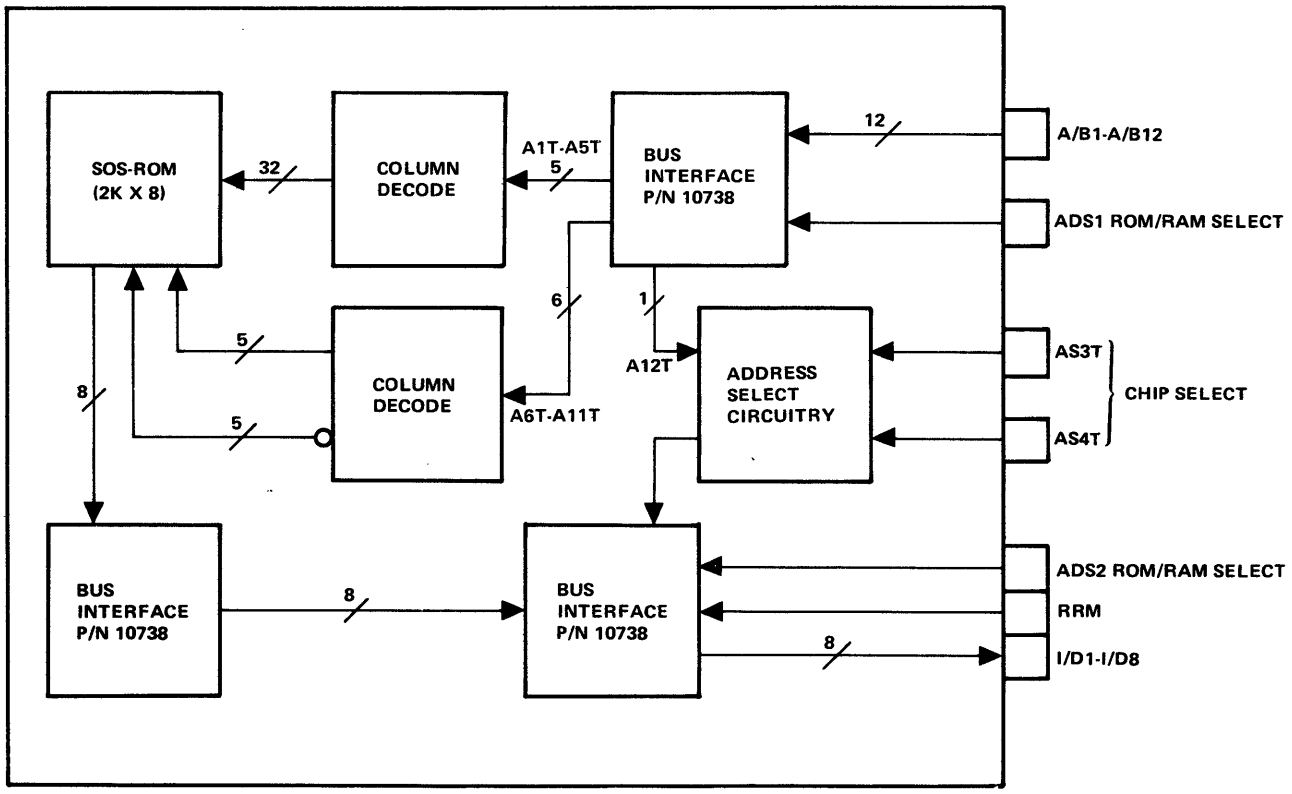


Figure 4. PPS SOS-ROM Module (2K x 8) Block Diagram

PPS RAM MODULE (P/N 20102 D17)

INTRODUCTION

The Microelectronic Device Division PPS RAM Module (P/N 20102 D17) is a 5 x 7-inch plug-in board providing the user with mounting and interface connections for up to eight RAM chips (P/N 10432). Each RAM chip provides 256 X 4-bit words of memory, providing up to 2048 X 4-bit words per each RAM module. By proper termination (bank select), up to four Ram modules may be incorporated into each PPS system for a total of 8K X 4-bit words of RAM.

With external clock switching logic, the RAM may be configured for use as a writable control store. In this mode, the RAM is read during the ROM cycle. A ROM word is 8 bits; therefore, the capacity of each RAM Module with eight RAM chips is reduced to 1024 X 8-bit words of memory. For further information regarding this option, contact Microelectronic Device Division of Rockwell International.

DESCRIPTION

The RAM Module is functionally divided into an upper RAM bank consisting of four RAM chips and a lower RAM bank consisting of four RAM chips as shown in the block diagram, Figure 6. The address bus (A/B1 through A/B12) and the RAM write half of the instruction/data bus (I/D5 through I/D8) are common to both banks; however, the read half of the instruction/data bus is divided into two groups, I/D1 through I/D4 for the upper bank and I/D1X through I/D4X for the lower bank.

When used as a RAM Module, these two groups of lines are bused together, (I/D1 through I/D4 to I/D1X through I/D4X). When the RAM Module is used as a writable control store, the module is connected to the 8-line I/D bus, (RAM Module I/DI through I/D4 to bus I/D1 through I/D4, and I/D1X through I/D4X to I/D5 through I/D8). It should be noted that I/D1X through I/D4X must be switched when loading the RAM. (For further information regarding this application, contact Microelectronic Device Division of Rockwell International.) Separate lines are provided for upper and lower chip select (SC3, SC4) to enable versatile address selection. Bank select is provided by connecting AS5 to CPU discrete outputs or GPI/O outputs.

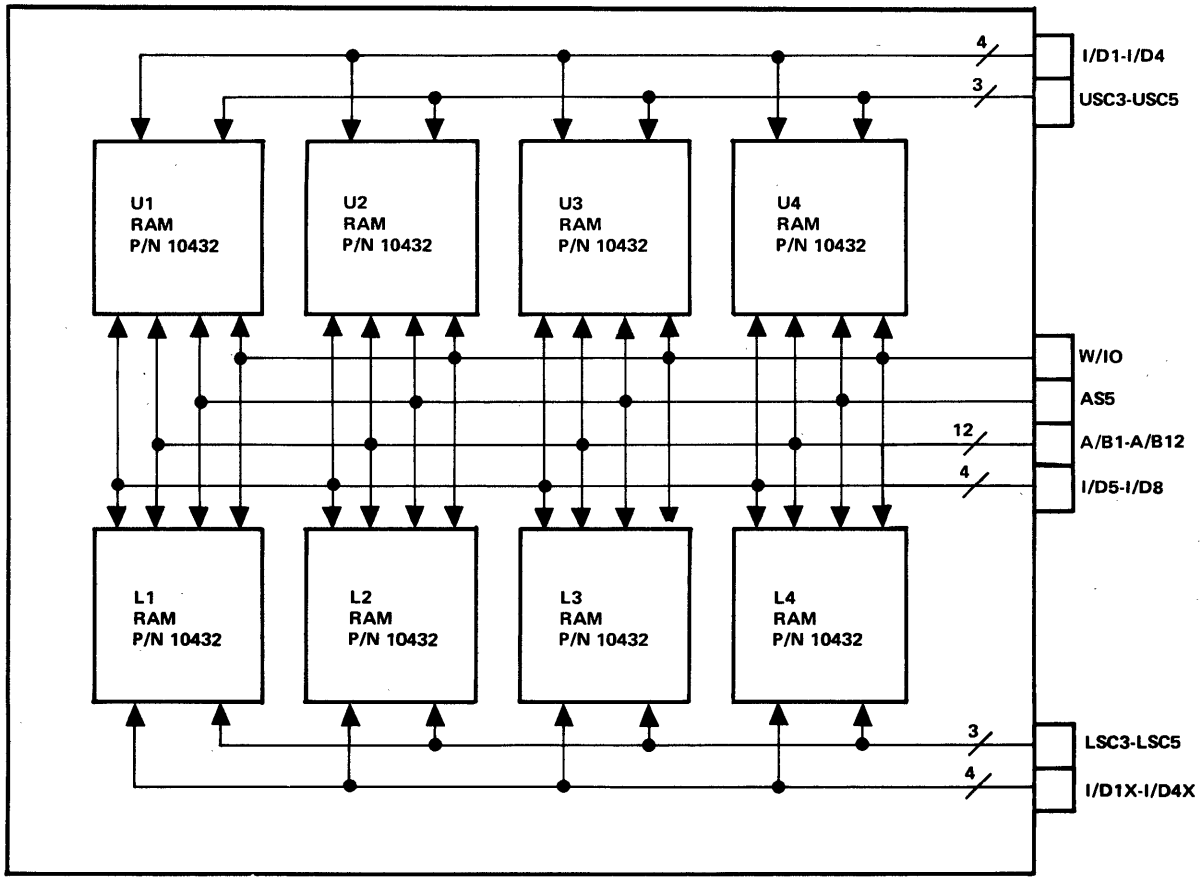


Figure 6. PPS RAM Module Block Diagram

PPS GENERAL PURPOSE INPUT OUTPUT (GPI/O) MODULE (P/N 20102 D36)

INTRODUCTION

The Microelectronic Device Division GPI/O Module (P/N 20102 D36) is designed to provide additional input/output capability for PPS product development. The GPI/O Module provides four general purpose input/output circuits with associated TTL buffers. Four 24-pin sockets are provided for interfacing TTL signals to external circuits.

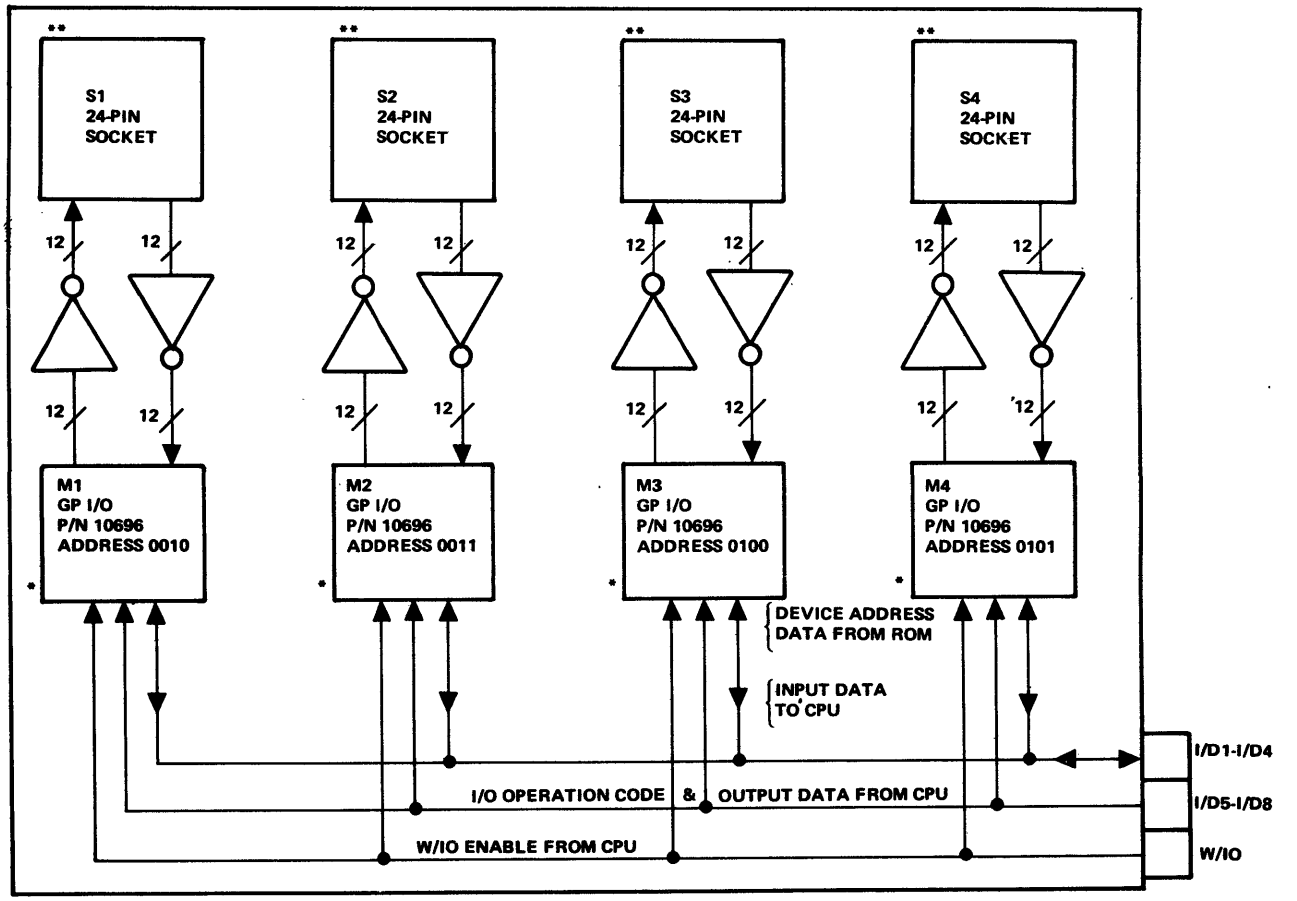
DESCRIPTION

The GPI/O Module consists of a 5 x 7-inch plug-in circuit card with all parts interconnected and ready for use. These circuits include four GPI/O circuits (P/N 10696) with 24 TTL buffers in each GPI/O circuit. (Refer to Figure 7 for the block diagram.)

The address bus (lines A/B1 through A/B12) and instruction/data bus (lines I/D1 through I/D8) are common to the pin locations of the address and instruction data buses of the PPS Processor Module, facilitating simple interconnection of the modules for product development.

The W/IO line controls the operation of any GPI/O chip. Addressing of the four GPI/O chips is accomplished during the second cycle of the IOL instruction. By proper strap termination, up to four GPI/O Modules may be used (16 GPI/O chips). With each execution of an IOL instruction, one group (A, B, or C) of four bits in, or four bits out, is addressed. Data transfer in or data transfer out then occurs in accordance with the executed IOL instruction.

The 12 input and 12 output lines from each of the four GPI/O chips are connected in parallel to four identical 24-pin sockets through buffer circuits. The sockets provide an easy method of connecting the GPI/Os to external devices, and the buffers provide the electronics required to convert the MOS logic levels to external TTL logic levels. Each of the 48 output buffers can drive up to 10 TTL circuits. All 48 input buffers accept TTL logic inputs, providing buffered interface to the GPI/O. The four 24-pin sockets attached to the GPI/O Module are identical and have similar mnemonics assigned to the pins.



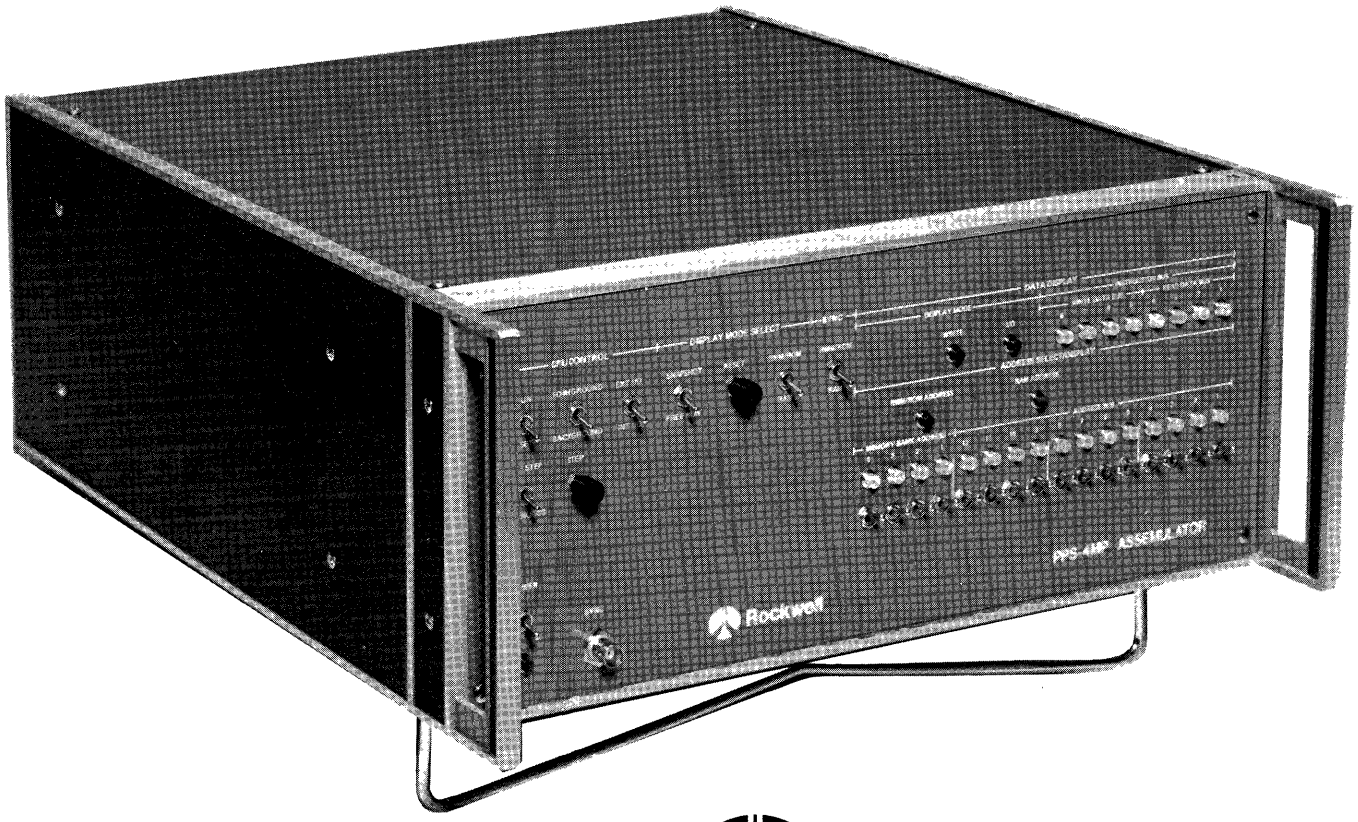
* MODULE IS SHOWN STRAPPED (ADDRESSED) AS A CONTINUATION OF THE PPS PROCESSOR GP I/O. PROCESSOR GP I/Os ARE NORMALLY STRAPPED TO RESPOND TO ADDRESSES 0000 AND 0001.

** THE 24-PIN SOCKETS PROVIDE 12 INPUT AND 12 OUTPUT CONNECTIONS FOR EXTERNAL TTL DEVICE INTERFACE TO THE PPS SYSTEM.

Figure 7. PPS GP/IO Module Block Diagram

PPS-4MP ASSEMULATOR

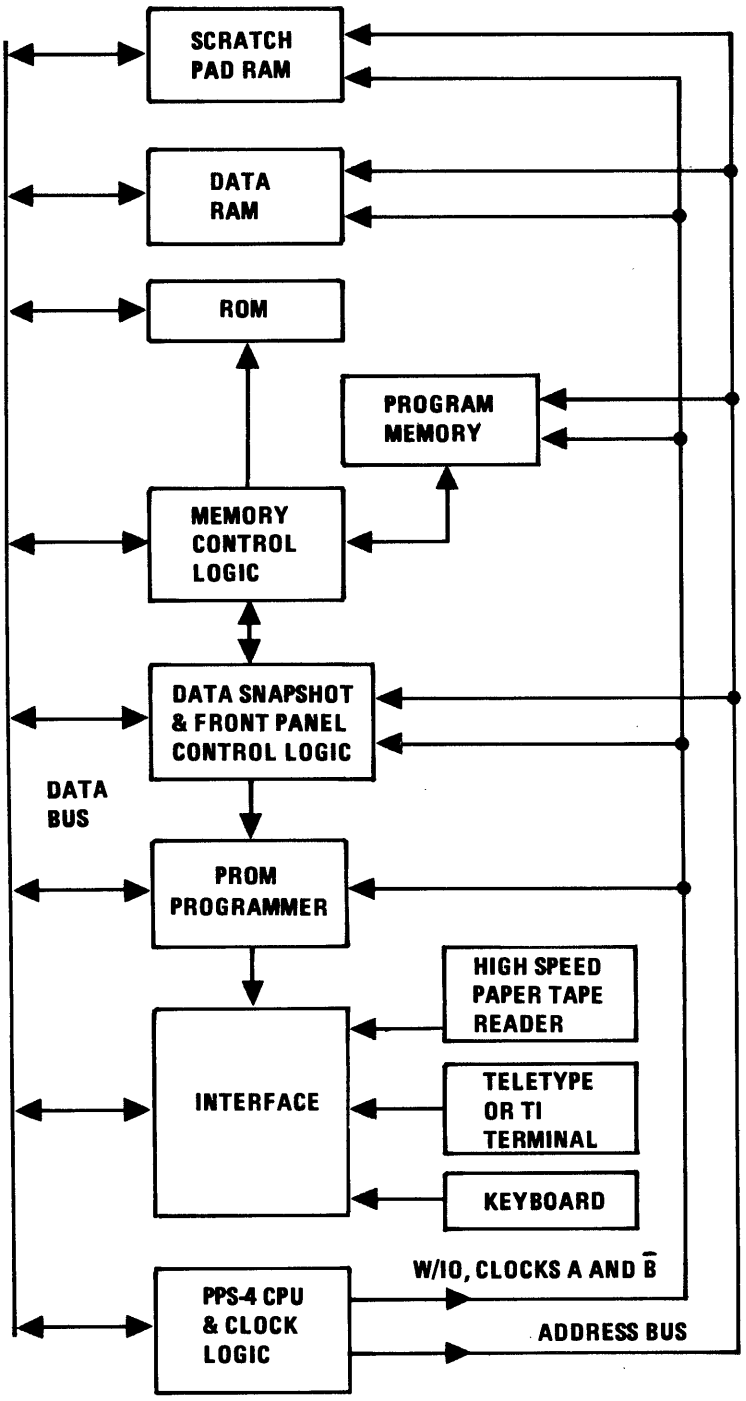
FOR MICROCOMPUTER: **PROGRAM ASSEMBLY--- PROGRAM DEBUGGING & REASSEMBLY--- ROM EMULATION--- PROTOTYPE TESTING--- SYSTEM TESTING---**



Rockwell International

FUNCTIONAL DESCRIPTION

Functionally, the PPS-4MP Assemulator basic configuration consists of the following:



1. Scratch Pad RAM (256 X 4). Provides internal assembler-utility data storage. (Not accessible to the user.)
2. Data RAM (256 X 4). Provides data storage. (Up to 4K X 4 data storage available.)
3. Resident ROM provides control program for assembler, tape edit and utility modes.
4. Program Memory. Stores the assembled program and is utilized by the CPU as ROM during the foreground mode. Used as RAM in the background mode. (Up to 10K words of program storage available.)
5. Memory Control Logic. Controls loading of the Program Memory in the utility load modes (background) and switches the Program Memory to act as ROM in the real time emulation (foreground) mode.
6. Data Snapshot Logic and Front Panel Logic. Provides monitoring of the PPS address bus and data bus. Continuous and single step modes are provided. Free run provides for display of all addresses and data. Continuous mode provides detection of address during execution of program and displays the detected ROM/RAM address and data. Single step mode displays present ROM address and data and executes single instructions.
7. Optional PROM Programmer provided to program erasable PROMs from the Program Memory and compare PROM and the Program Memory. (PROM contents can be dumped via utilities.)
8. Interface provided to control a Teletype ASR-33 and TI 733-ASR terminal. Reads tape into Program Memory and writes Program Memory onto tape.
9. Optional High Speed Paper Tape Reader to read paper tape at 120 ch/sec. Can be used in conjunction with TTY to speed up assembly.
10. Optional Hex Data and Control Keyboard allows the Assemulator to be controlled and change Program Memory without a need for a terminal.
11. CPU (PPS-4 Central Processor) controls the system during assembly-utility use and during actual real time emulation. PPS clock circuit provides timing for the system.

The PPS-4MP ASSEMULATOR provides program and product development support for the Rockwell MOS/LSI 4-bit Parallel Processing System (PPS-4).

The Assemulator allows designers and programmers to efficiently perform the following functions:

- Assemble programs by simply typing the PPS mnemonic code on TTY ASR-33 or TI 733-ASR terminal connected to the Assembler.
- Edit program source tapes.
- Emulate programs assembled by the Assembler or Rockwell's PPS Assembly/Simulation program which can be accessed via the General Electric or Tymshare computer services.
- Edit, reassemble, debug, test and operate assembled programs in real time.
- Set program traps for individual program step analysis.
- Execute the program in single instruction steps when desired.
- Prototype-Test complete product equipment models interconnected with keyboards, printers, displays, or as a system interconnected with a modem or other peripherals in real time.
- Program erasable PROMs.
- Input from optional High Speed Paper Tape Reader.
- Input from optional Hex Data and Control Keyboard for operation without a terminal.

A secondary but highly valuable use for the PPS-4MP is that of a powerful micrcomputer which can be programmed for a variety of dedicated functions.

FUNCTIONAL DETAILS

Program Assembly: Using an interconnected terminal, the equipment designer types in the mnemonic of the instructions which he wants the PPS to execute. Through its control program in ROM, the CPU in the PPS Accumulator is used to assemble and edit the program which is stored in the Program Memory (RWM).

The equipment designer can also use Rockwell's assembly and simulation program which is available through the Tymshare, or General Electric, timesharing computer network. The assembled program is output on punched tape or cassette tape at the terminal which is connected to the computer. The program can then be loaded, via the terminal or high speed paper tape reader, into the RWM of the Assemulator for prototype testing.

Program Editing: When the PPS Assemulator is used as an assembler, the equipment designer can edit the assembled listing which is printed out on the terminal and then output onto tape at the terminal for debugging and reassembling.

The equipment designer can use the terminal to set up traps during program execution or single step program execution with single step selection. Additionally, an oscilloscope can be synchronized with the address and/or data bus lines to obtain displays of actual data as specific signals through a connector on the front panel so that execution of programs can be verified visually.

Prototype Testing: With the assembled program in the RWM, the equipment designer can switch to an operate mode in which the stored program is used as a ROM emulator. In this mode, the CPU accesses the program in the RWM as if it were the ROM in an operational system. The terminal now functions as a peripheral input/output device. Or, other peripherals – keyboards, displays, printers, etc. – can be connected and operated in **REAL TIME**. The optional Hex Data and Control Keyboard can also be used for this purpose in place of the terminal.

The PPS Assemulator is packaged in a 7-inch high, 19-inch wide standard rack mount chassis which is also suitable for desk top use. Entry and control of data into the unit is made via Teletype ASR-33 or TI 733-ASR, which also provides printed output. Entry and control without printout capability is also provided by the optional Hex Data and Control Keyboard.

Detailed information and all necessary parts are provided for connecting the unit to a Teletype ASR-33 with paper tape loader or TI 733-ASR with twin cassettes. When purchased with the high speed paper tape reader and Hex Data and Control Keyboard, the Assemulator can function as a self-contained ROM Emulator requiring no terminal. All functions can be performed in this configuration except assembly and tape edit.

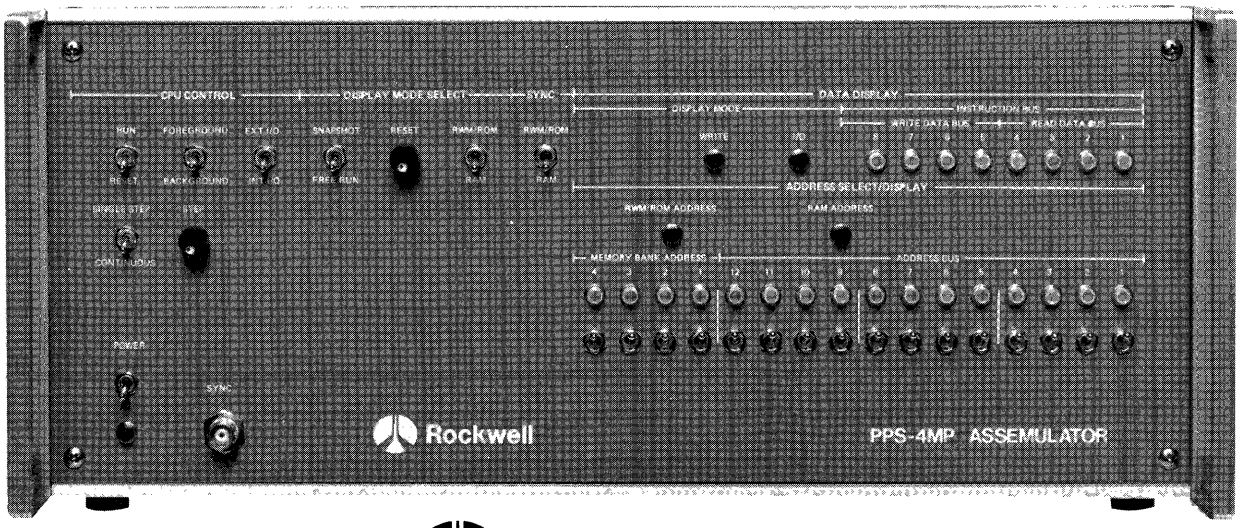
PPS-4MP ASSEMULATOR FEATURES

BASIC UNIT

- Single Step Instruction Execution for Debug
- Resident Tape Editor
- Data Snapshot
- Resident ROM Assembler
- Resident ROM Utility and Debug
- Real Time Program Execution and Program Modification
- CPU and CPU Control Logic
- Chassis
- Power Supply
- 1K X 8 Program Memory Expandable to 10K X 8
- Scratch Pad RAM
- Input/Output Ports With Interconnecting Cables
- 256 X 4 Data RAM Expandable to 4K X 4
- Interfaces With Teletype ASR-33 and/or Texas Instruments 733-ASR Terminals

OPTIONS

- Bus Extender Module
- High Speed Paper Tape Reader
- Hex Data And Control Keyboard
- I/O Control Modules (GPI/O, GPKD, PC)
- Memory Modules — Program Memory and Data Memory
- PROM Programmer Module



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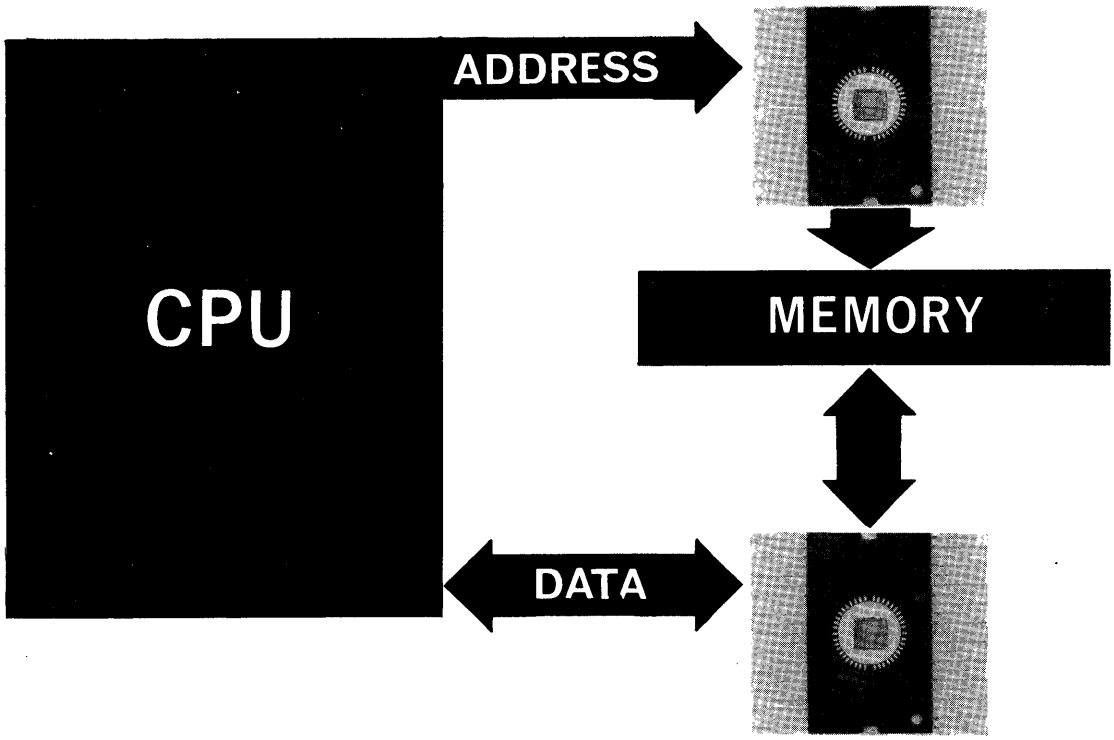
NOV. 1974 DOCUMENT NO. 29400 N40

DATA SHEET

PARALLEL PROCESSING SYSTEM
(PPS-4)
BUS INTERFACE CIRCUIT
Part No. 10738



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Document No. 10738 N11
Rev. 2. Sept. 1974

RELATED PUBLICATIONS

Parallel Processing System (PPS-4) Basic Devices, Data Sheet. Document No. 29003 N11

PPS-8 Parallel Processing System Pretest Description. Document No. 20164 N40

NOTICE

Information provided in this Data Sheet is for reference purposes only and is subject to change without notice.

For specific detail information on this device or any of our other advanced microelectronic devices please contact the nearest Rockwell International Microelectronic Device Division Office.

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INTRODUCTION

INTRODUCTION

This data describes the Bus Interface (B/I) Circuit, P/N 10738, manufactured by the Microelectronic Device Division of Rockwell International. The B/I is a MOS/LSI (Metal-Oxide-Semiconductor/Large Scale Integrated) circuit used for interfacing the Parallel Processing System (PPS) Address Bus (A/B) or the PPS Instruction/Data Bus (I/D) with static MOS or TTL logic circuits. The B/I provides a time, impedance, and logic level interface between the PPS bus and SOS ROM, PROM, and core-type static memories.

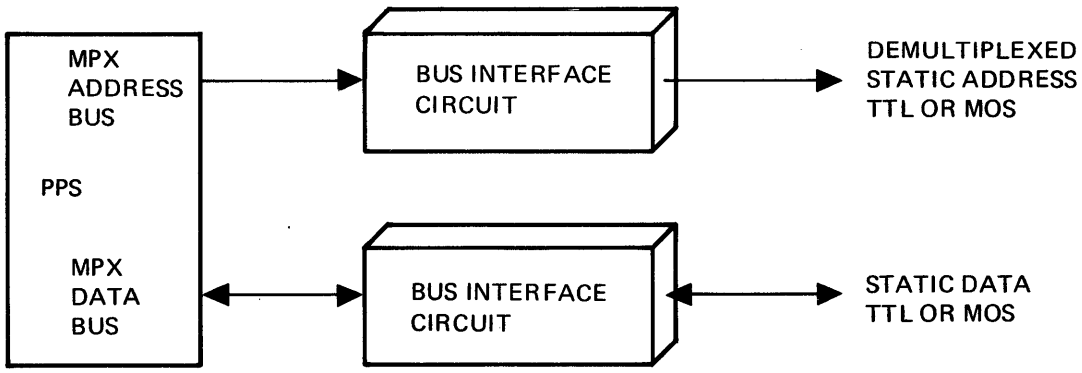
FEATURES

- Identical circuits for both PPS Instruction/Data Bus and Address Bus Interface
- Direct Interface — no external components needed
- MOS Compatible Interface
- TTL Compatible Interface
- Static Outputs

The Bus Interface is a multipurpose circuit designed to serve as an interface between the dynamic MOS levels of PPS address and data bus signals and the static commercially available MOS or TTL memory products. The circuit is multipurpose in that it can be appropriately strapped by four input pins to act as an interface for the 12-bit parallel ROM/RAM address bus as well as the 8-bit parallel instruction/data bus. This single, multipurpose circuit simplifies purchasing, inventory, and product assembly.

This circuit can be used to interface with a variety of TTL compatible ROMs, such as Rockwell SOS ROM or other semiconductor manufacturers' programmable and electrically alterable ROMs. Programmable ROMs (PROMs) are useful when building a small quantity of prototype systems, performing ROM emulation functions or providing an alteratle ROM as a customizing feature of the overall ROM section of a PPS system. This bus interface circuit can also be used to interface with other manufacturers' core memories in those systems which must have a non-volatile memory.

Information on the PPS-4 can be found in the PPS-4 Basic Device Data Sheet, Document No. 29003 N11.



GENERAL APPLICATION OF BUS INTERFACE CIRCUIT

BUS INTERFACE CIRCUIT (BI), P/N 10738

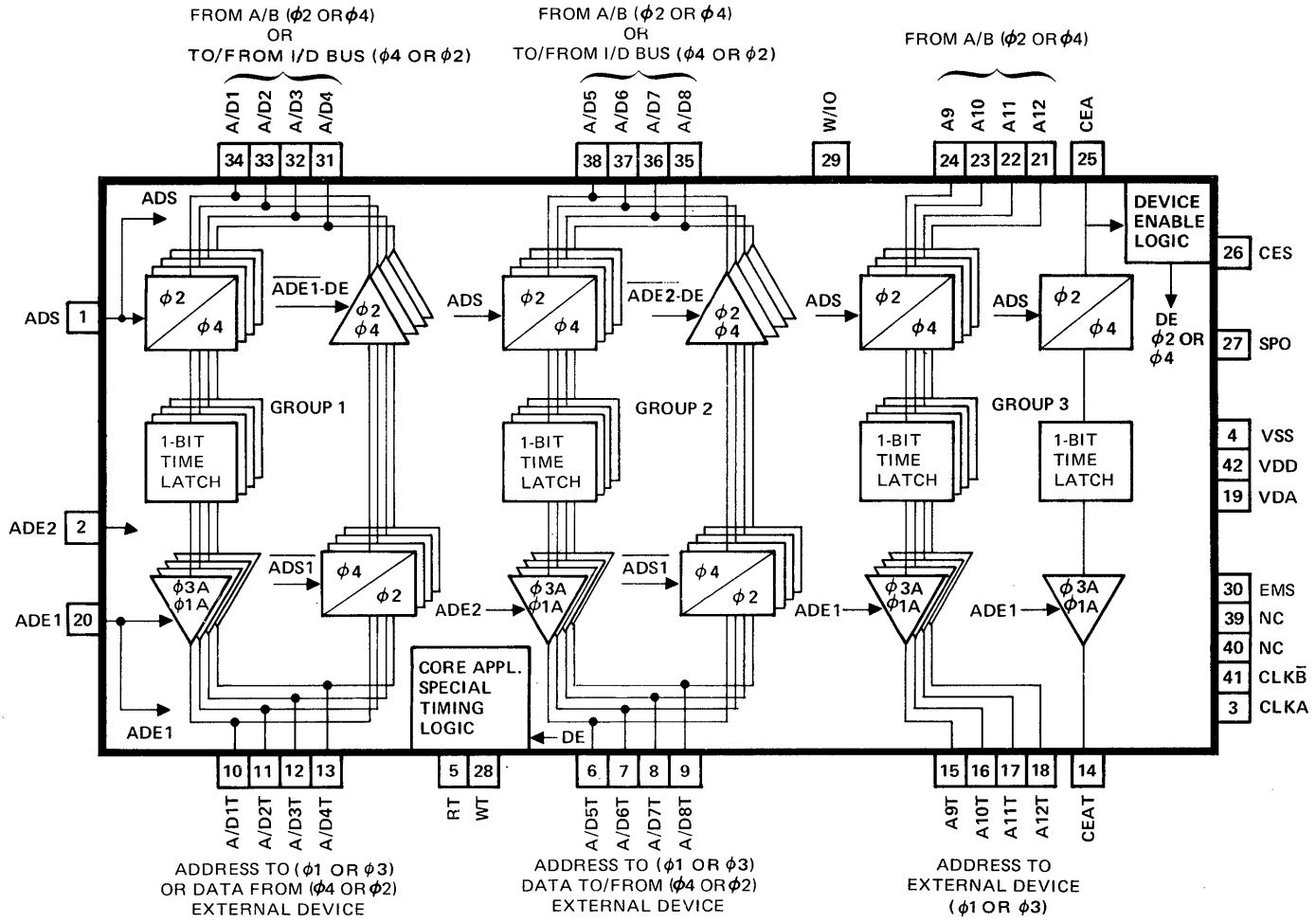


FIGURE 1. BUS INTERFACE CHIP BLOCK DIAGRAM

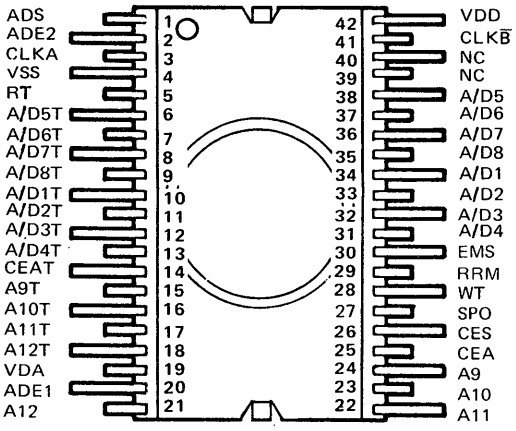


FIGURE 2. BUS INTERFACE PIN CONFIGURATION, P/N 10738

DEFINING EQUATIONS

1. CORE APPLICATION
   - RT = CLKA
   - WT = $W/IO_{\phi 2} \cdot (CEA_{\phi 4} \oplus CES)$
   - $DE_{\phi 2} = W/IO_{\phi 4} \cdot (CEA_{\phi 4} \oplus CES)$
   - Signal $DE_{\phi 2}$ enables the BI data drivers during Phase 2. (DE Means Device Enable Data Mode)
   - RRM Input connects to W/IO
2. PROM APPLICATION
   - $DE_{\phi 4} = CEA_{\phi 2} \oplus CES$
   - Signal $DE_{\phi 4}$ enables the BI PPS ϕ_4 drivers during Phase 4.
   - The RPM input is strapped to Logic Zero (GND).
3. RPM (ROM RAM MEMORY SELECT)
   - RPM connects to WI/O when B/I is used as RAM look-up table. RRM connects to VSS when B/I is used as ROM.

BUS INTERFACE CIRCUIT DESCRIPTION

DESCRIPTION

The Block Diagram of the Bus Interface circuit, Figure 1, shows the BI circuit divided into three functional groups. Groups 1 and 2 consist of four identical circuits each. The only difference between groups 1 and 2 is the separate Address Data Enable lines; ADE 1 for group 1 and ADE 2 for group 2. Group 3 differs from groups 1 and 2 in that it is not bi-directional. The left hand path of group 3 has four identical circuits and is identical to the left hand path of group 1. The right hand path of group 3 is similar to the left hand path of groups 1 and 3 except it is a single path.

The left hand paths of all groups have four 1-bit latches and the right hand path of group 3 has a single 1-bit latch. The user, by strapping, selects when these latches are enabled either at $\emptyset_2$ or $\emptyset_4$ time. These latches capture the dynamic PPS bus data or address. Thus, captured logic levels appear as static logic levels at the corresponding TTL compatible outputs, when the output drivers are enabled. The right hand path of groups 1 and 2 are enabled at appropriate times for the transmission of TTL static logic levels to the PPS I/D bus at selected $\emptyset$ times. Refer to page 2 (Defining Equations) and Table 1 (Mode Select Control) for further details.

The pin designations, Figure 2, have the following meanings: A/D1 – A/D8 are address or data lines numbers 1 through 8; A9 – A12 are address lines 9 – 12. These same labels followed by a T represent TTL interface lines; the CLKA and CLK$\overline{B}$ are the clock input lines, and the EMS is a TTL compatible clock signal available for synchronization; VSS and VDD are power pins and VDA is an alternate VDD source for the output driver circuits. Proper VDA termination provides compatible output logic levels (VDA = -5V for TTL interface and -17V for MOS interface (or alternatively, VDA = 0V for TTL interface and -12V for MOS interface)); RT and WT are synchronizing memory read and write signal outputs; SPO is a synchronized power-on signal input obtained from the CPU; W/IO is the PPS CPU Write Command and Input/Output Enable Signal. The meaning and use of ADS, ADE1, ADE2, CES and CEA signals is explained in the following paragraphs.

The BI circuit is enabled by placing on the Chip Enable Address input (CEA), the logic state opposite to that which appears on the Chip Enable Strap (CES). Reference Table 2. CEAT provides the TTL equivalent of CEA.

The Address Data Selector Strap (ADS) is connected to logic one to capture input data during phase 4 and to a logic zero to capture data during phase 2.

ADE1 and ADE2 are enabled by logic zero levels and disabled by logic one levels. When ADE1 or ADE2 enable the left hand paths, the right hand paths are disabled by ADE1•DE, ADE2•DE logic signal. The term DE corresponds to DE $\emptyset_2$ or DE $\emptyset_4$, as defined by the Defining Equations, page 2.

Defining Equations

These equations define the logic functions performed in the Core and PROM Application Special Timing Logic block and the Device Enable Logic block of Figure 1 (Bus Interface Chip Block Diagram).

The Device Enable Logic activates selected B/1 drivers for communication on the PPS bus. When not selected, the driver outputs float. Read Time (RT) and Write Time (WT) are two additional outputs provided for memory commands. Output RT is an inverted CLKA output for synchronizing memory read. The WT signal is defined in the Defining Equations, page 2.

RT & WT Signal Polarity

The BI circuit inverts voltage levels from the PPS bus to the static outputs for RT and WT signals.

External Memory Strobe (EMS) Signal

The EMS signal serves as a strobe for external memory device address and data lines. The EMS signal is synchronized by the $\overline{B}$ clock signal and occurs between 70 and 300 msec after $\overline{B}$ as shown in Figure 7.

Bus Interface Operation

When used to interface ROM or RAM components with the 12-bit address bus, address data flows from top to bottom through the left hand branches of groups 1, 2 and 3, Figure 1. When used to interface components with the 8-bit instruction bus, instruction data flows from bottom to top through the right-hand branches of groups 1 and 2. When used to interface core memory systems to the data bus, 4-bit data is transferred from core to data bus via the right hand path of group 1, and 4-bit data is transferred to core from data bus via the left hand path of group 2. The BI provides "read enable" and "write enable" signals for the core memory systems. Note in Figure 1 that interface with PPS bus signals is shown at the top while interface with TTL circuitry is at the bottom. These signal interfaces are shown in Figures 4 and 5. Figure 4 shows signal flow when used as an interface with PROM memory circuits. Figure 5 identifies signal flow when used as an interface with CORE-type memories.

The three input straps designated as ADS, ADE1, and ADE2 are used to instruct the BI circuit as to the mode of operation it is expected to perform. ADS in conjunction with ADE1 and ADE2 are used to designate between ROM and RAM-type memory operation. ADE1 and ADE2 select either address or data bus modes of operation for interface circuits groups 1 and 2, respectively. These inputs and related codes are further defined in Table 1 (Mode Select).

The SPO signal from the CPU is used to inhibit write control signal (WT) output until power is synchronized.

BUS INTERFACE CIRCUIT APPLICATIONS

APPLICATIONS

Tables 1 and 2 show how the BI circuit strap terminations (see Figures 4 and 5) are connected for various applications.

Table 1, Mode Select, is divided into two main classes of application for the BI circuit. These main classifications are Read Only Memory (ROM), and Random Access Memory (RAM), applications. Each of these applications has two modes of operation for the BI circuit: address and data modes. These modes are designated in the first two columns. The last two columns indicate the phase times that addresses and data are available for the specific application. The remainder of the columns show the proper termination of all mode selecting pins.

A typical method of interfacing the PPS-4 with PROMs using the BI circuits is shown in Figure 3. The interfacing circuits and PROM circuits shown are those used on the Rockwell PROM Evaluation and Development module, P/N 20102 D17. Each of these modules provides a 4K x 8 memory complete with two Bus Interfacing circuits. Up to four of these PROM modules may be used in a PPS-4 system.

Figure 4 shows the PROM application of the BI circuit. For clarity, only the pertinent circuits and phase times are shown. Table 3 shows the interface connections for ROM applications.

The use of BI circuits for interfacing with core memory is shown in Figure 5. Only the utilized portions of the circuit groups are shown. For example the BI circuit uses only the left hand path of groups 1, 2 and 3 for address interface. Also indicated are the phase times during which the receiver and driver circuits are enabled, Ø4 and Ø3A, respectively. The same type of information is shown for the BI circuit used for data bus interface. Table 4 shows the interface connections for RAM (mainly core) applications.

TABLE 1 – MODE SELECT

FUNCTION	BI APPLICATION	RRM	ADDRESS/ DATA SELECTOR ADS	ADDRESS/ DATA ENABLE 1 ADE 1	ADDRESS/ DATA ENABLE 2 ADE 2	CHIP ENABLE ADDRESS CEA	READ TIME RT Ø(1&2)	WRITE TIME WT Ø(3&4)	ADDRESS A/D1 - A/D12	DATA A/D1 - A/D4	DATA A/D5 - A/D8
READ ONLY MEMORY (PROM) INTERFACE	ROM ADDRESS	0	0	0	0	*	NA	NA	Ø2		
	ROM INSTRUCTIONS	0	1	1	1	*	NA	NA		Ø4	Ø4
READ ALTERABLE MEMORY (RAM) INTERFACE. (PRIMARILY CORE)	RAM ADDRESS	W/IO	1	0	0	*	Ø(1+2)	Ø(3+4)	Ø4		
	RAM DATA	W/IO	0	1	0	*				Ø2	Ø2
			STRAP TERMINATION			* SEE TABLE 2	LOGIC LEVEL AT Ø TIMES		NON-INVERTING SIGNAL PATHS		

TABLE 2 – CHIP ENABLE ADDRESS (CEA)

CEA ACTIVATION LOGIC LEVEL	(CES) CHIP ENABLE STRAP TERMINATION
1	0
0	1

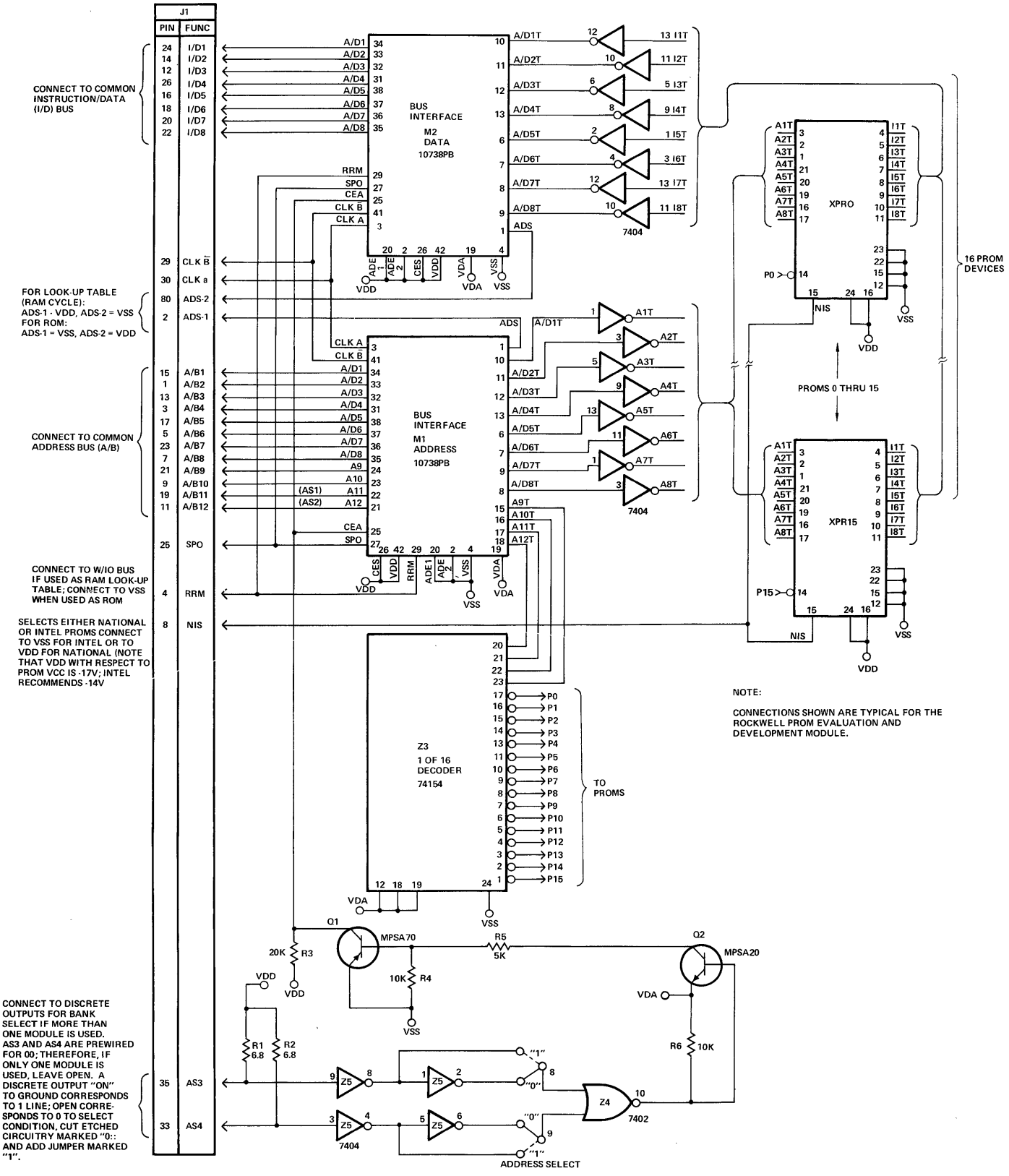
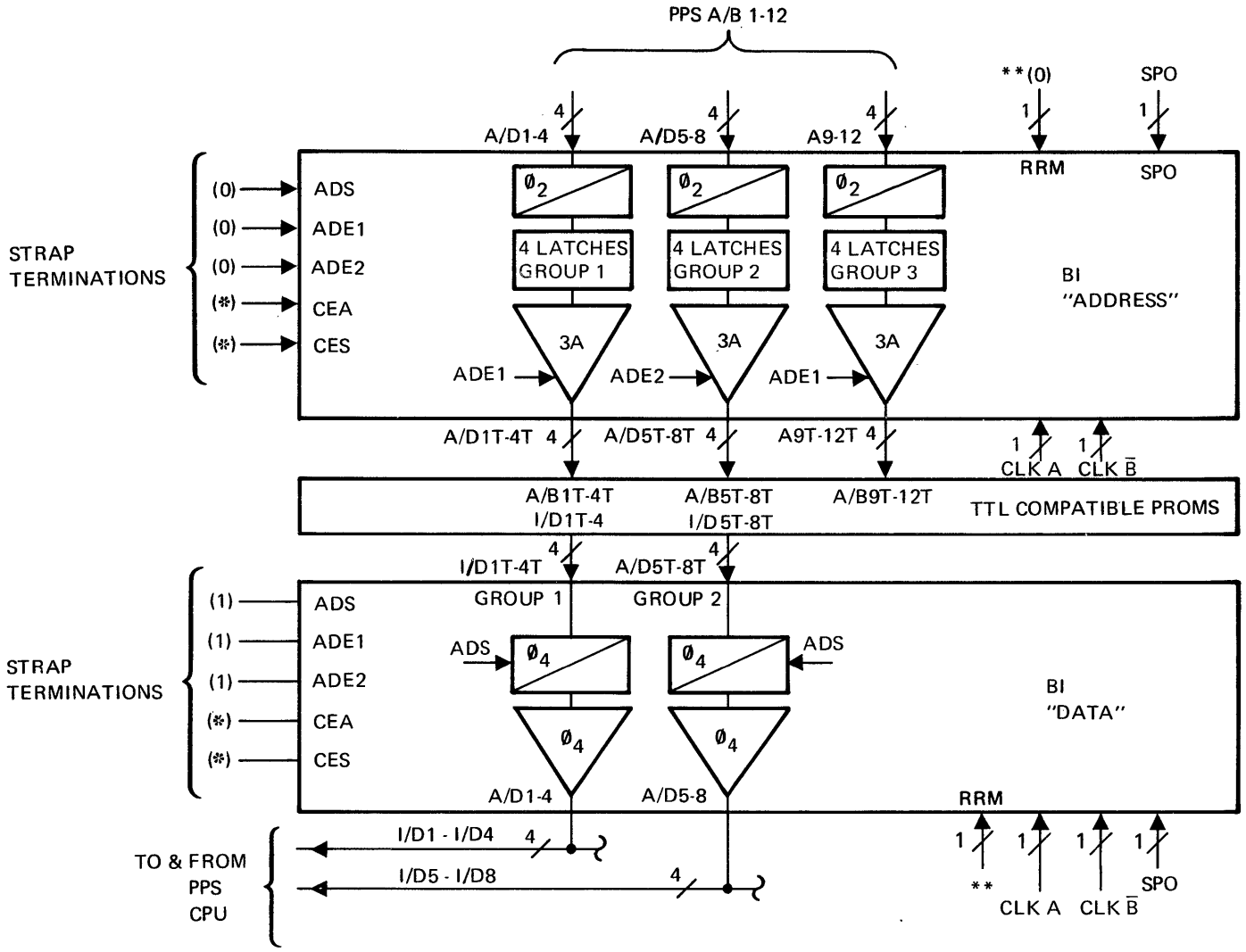


FIGURE 3. TYPICAL PROM INTERFACE

TABLE 3. PPS/ROM INTERFACE THRU BUS INTERFACES CIRCUIT

PPS	B1 (ADDRESS) PIN	B1 (ADDRESS) TERM	PROM/ROM		B1 (DATA) PIN	B1 (DATA) TERM	PPS
A/B1	34	A/D1			34	A/D1	I/D1
A/B2	33	A/D2			33	A/D2	I/D2
A/B3	32	A/D3			32	A/D3	I/D3
A/B4	31	A/D4			31	A/D4	I/D4
A/B5	38	A/D5			38	A/D5	I/D5
A/B6	37	A/D6			37	A/D6	I/D6
A/B7	36	A/D7			36	A/D7	I/D7
A/B8	35	A/D8			35	A/D8	I/D8
A/B9	24	A9			24	A9	
A/B10	23	A10			23	A10	
A/B11	22	A11			22	A11	
A/B12	21	A12			21	A12	
	10	A/D1T	A/B1T	I/D1T	10	A/D1T	
	11	A/D2T	A/B2T	I/D2T	11	A/D2T	
	12	A/D3T	A/B3T	I/D3T	12	A/D3T	
	13	A/D4T	A/B4T	I/D4T	13	A/D4T	
	6	A/D5T	A/B5T	I/D5T	6	A/D5T	
	7	A/D6T	A/B6T	I/D6T	7	A/D6T	
	8	A/D7T	A/B7T	I/D7T	8	A/D7T	
	9	A/D8T	A/B8T	I/D8T	9	A/D8T	
	15	A9T	A/B9T		15	A9T	
	16	A10T	A/B10T		16	A10T	
	17	A11T	A/B11T		17	A11T	
	18	A12T	A/B12T		18	A12T	
	5	RT			5	RT	
	28	WT			28	WT	
VDA	19	VDA	TTL GND		19	VDA	
VSS	29	RRM			29	RRM	VSS
SPO	27	SPO			27	SPO	
VSS	4	VSS			4	VSS	
VDD	42	VDD			42	VDD	
CLK$\overline{B}$	41	CLK$\overline{B}$			41	CLK$\overline{B}$	
CLKA	3	CLKA			3	CLKA	
	30	EMS			30	EMS	
VSS	1	ADS (STRAP)			1	ADS (STRAP)	VDD
VSS	20	ADE1 (STRAP)			20	ADE1 (STRAP)	VDD
VSS	2	ADE2 (STRAP)			2	ADE2 (STRAP)	VDD
VDD or VSS	26	CES (STRAP)			26	CES (STRAP)	VDD or VSS
VSS or VDD	25	CEA			25	CEA	VSS or VDD

BUS INTERFACE CIRCUIT APPLICATIONS



*SEE TABLE 2. V_{DD} = (1)
V_{SS} = (0)

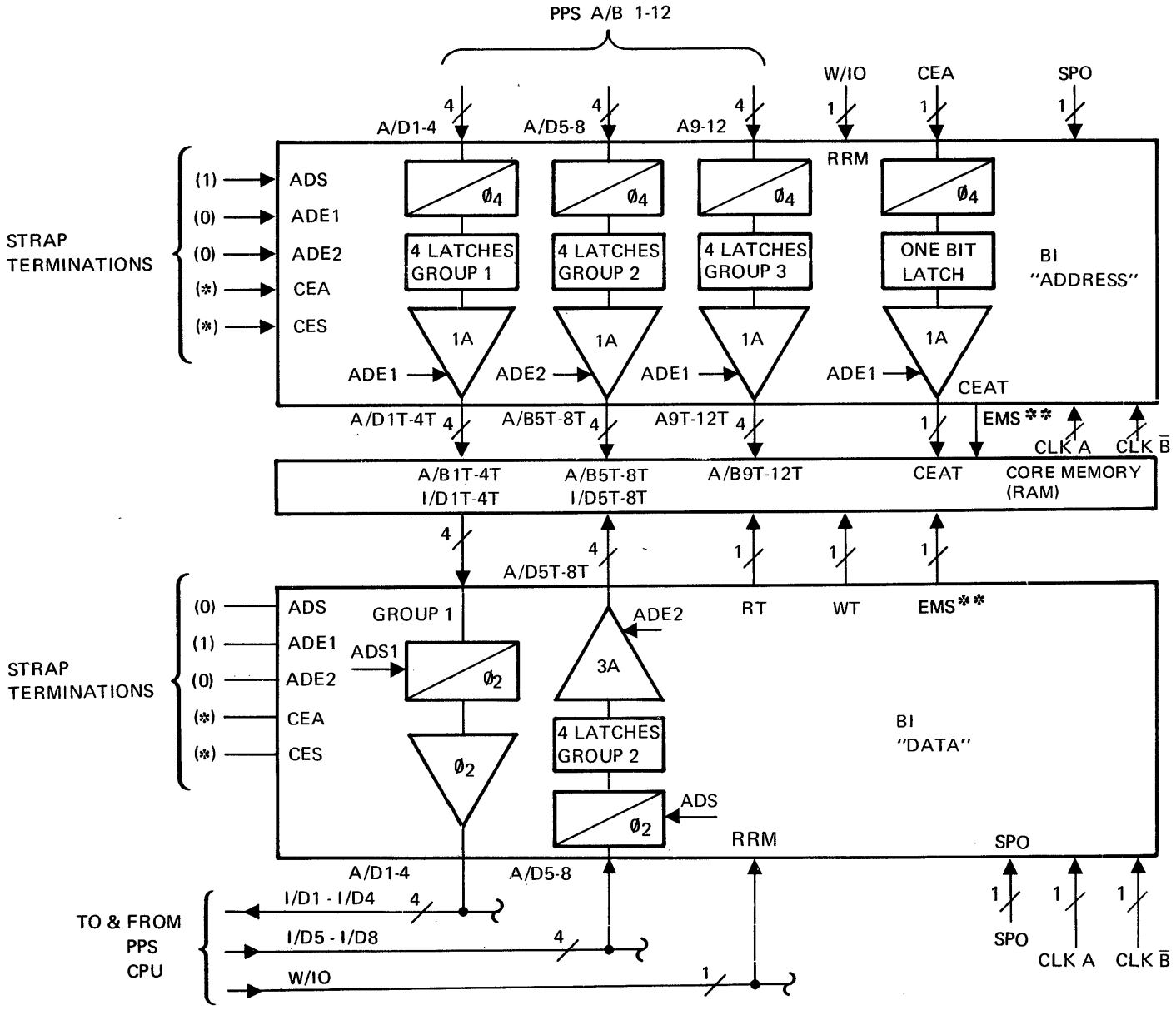
**RRM = VSS FOR ROM
RRM = W/IO FOR TABLE LOOK UP

FIGURE 5. CORE MEMORY APPLICATION BLOCK DIAGRAM

TABLE 4. PPS/RAM INTERFACE THRU BUS INTERFACES CIRCUIT

PPS	B1 (ADDRESS)		RAM (CORE)			B1 (DATA)		PPS
	PIN	TERM				PIN	TERM	
A/B1	34	A/D1				34	A/D1	I/D1
A/B2	33	A/D2				33	A/D2	I/D2
A/B3	32	A/D3				32	A/D3	I/D3
A/B4	31	A/D4				31	A/D4	I/D4
A/B5	38	A/D5				38	A/D5	I/D5
A/B6	37	A/D6				37	A/D6	I/D6
A/B7	36	A/D7				36	A/D7	I/D7
A/B8	35	A/D8				35	A/D8	I/D8
A/B9	24	A9				24	A9	
A/B10	23	A10				23	A10	
A/B11	22	A11				22	A11	
A/B12	21	A12				21	A12	
	10	A/D1T	A/B1T	I/D1T		10	A/D1T	
	11	A/D2T	A/B2T	I/D2T		11	A/D2T	
	12	A/D3T	A/B3T	I/D3T		12	A/D3T	
	13	A/D4T	A/B4T	I/D4T		13	A/D4T	
	6	A/D5T	A/B5T	I/D5T		6	A/D5T	
	7	A/D6T	A/B6T	I/D6T		7	A/D6T	
	8	A/D7T	A/B7T	I/D7T		8	A/D7T	
	9	A/D8T	A/B8T	I/D8T		9	A/D8T	
	15	A9T	A/B9T			15	A9T	
	16	A10T	A/B10T			16	A10T	
	17	A11T	A/B11T			17	A11T	
	18	A12T	A/B12T			18	A12T	
	5	RT	READ ENABLE			5	RT	
	28	WT	WRITE ENABLE			28	WT	
VDA	19	VDA				19	VDA (TTL GND)	VDA
W/IO	29	RRM				29	RRM	W/IO
SPO	27	SPO				27	SPO	SPO
VSS	4	VSS				4	VSS	VSS
VDD	42	VDD				42	VDD	VDD
CLKB	41	CLK$\overline{B}$				41	CLK$\overline{B}$	CLK$\overline{B}$
CLKA	3	CLKA				3	CLKA	CLKA
	30	EMS				30	CLK $\overline{BT}$	
VDD	1	ADS (STRAP)				1	ADS (STRAP)	VSS
VSS	20	ADE1 (STRAP)				20	ADE1 (STRAP)	VDD
VSS	2	ADE2 (STRAP)				2	ADE2 (STRAP)	VSS
*	26	CES (STRAP)				26	CES (STRAP)	*
*	23	CEA				25	CEA	*
	14	CEAT	EX ADDRESS BIT			14	CEAT	

*SEE TABLE 2



*SEE TABLE 2 VDD = (1)
VSS = (0)

**ONLY ONE EMS INPUT TO CORE IS REQUIRED

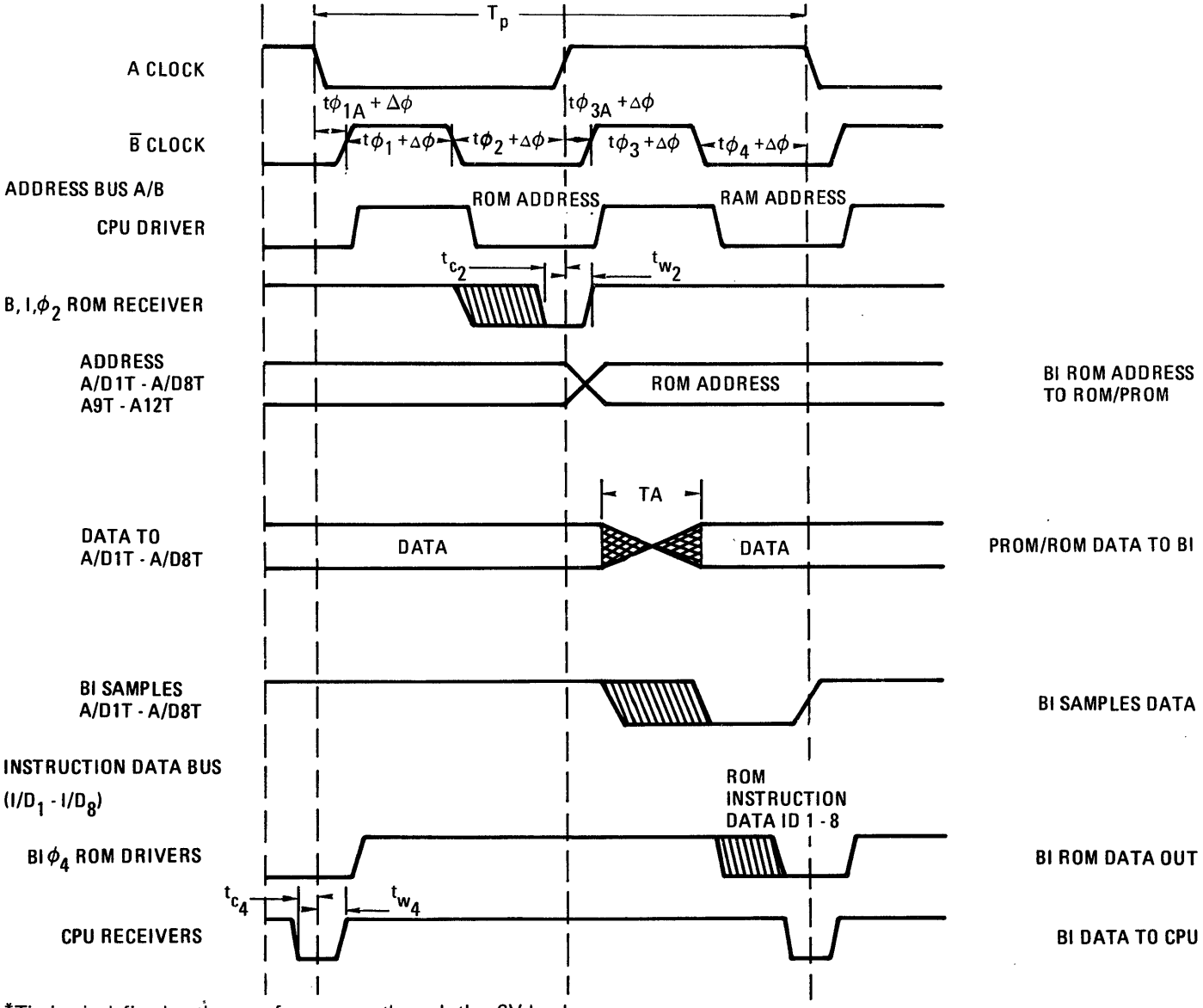
FIGURE 5. CORE MEMORY APPLICATION BLOCK DIAGRAM

TIMING DIAGRAM* ROM

A.C. CHARACTERISTICS (See Table of AC Characteristics for Additional Details)

SYSTEM CLOCK PHASE

		$\phi 4$	$\phi 1A$	$\phi 1$	$\phi 2$	$\phi 3A$	$\phi 3$	$\phi 4$	$\phi 1A$	$\phi 1$
CLOCK TIMING RATIO	S18 = 1 (÷18)	1/18	4/18	4/18	1/18	4/18	4/18	1/18	4/18
	S14 = 1 (÷14)	3/14	3/14	3/14	1/14	3/14	3/14	1/14	3/14
	S12 = 1 (÷12)	2/12	2/12	3/12	1/12	2/12	3/12	1/12	2/12



*Timing is defined as the waveform passes through the -6V level.

FIGURE 6. ROM TIMING DIAGRAM

System Bus Load vs Clock Frequency

The PPS is designed to operate with a recommended clock frequency of about 199 kHz (3.58 MHz ÷ 18). Operating at this frequency, the multiplex bus interface circuitry is designed to drive a system with capacity load of up to 350 pF.

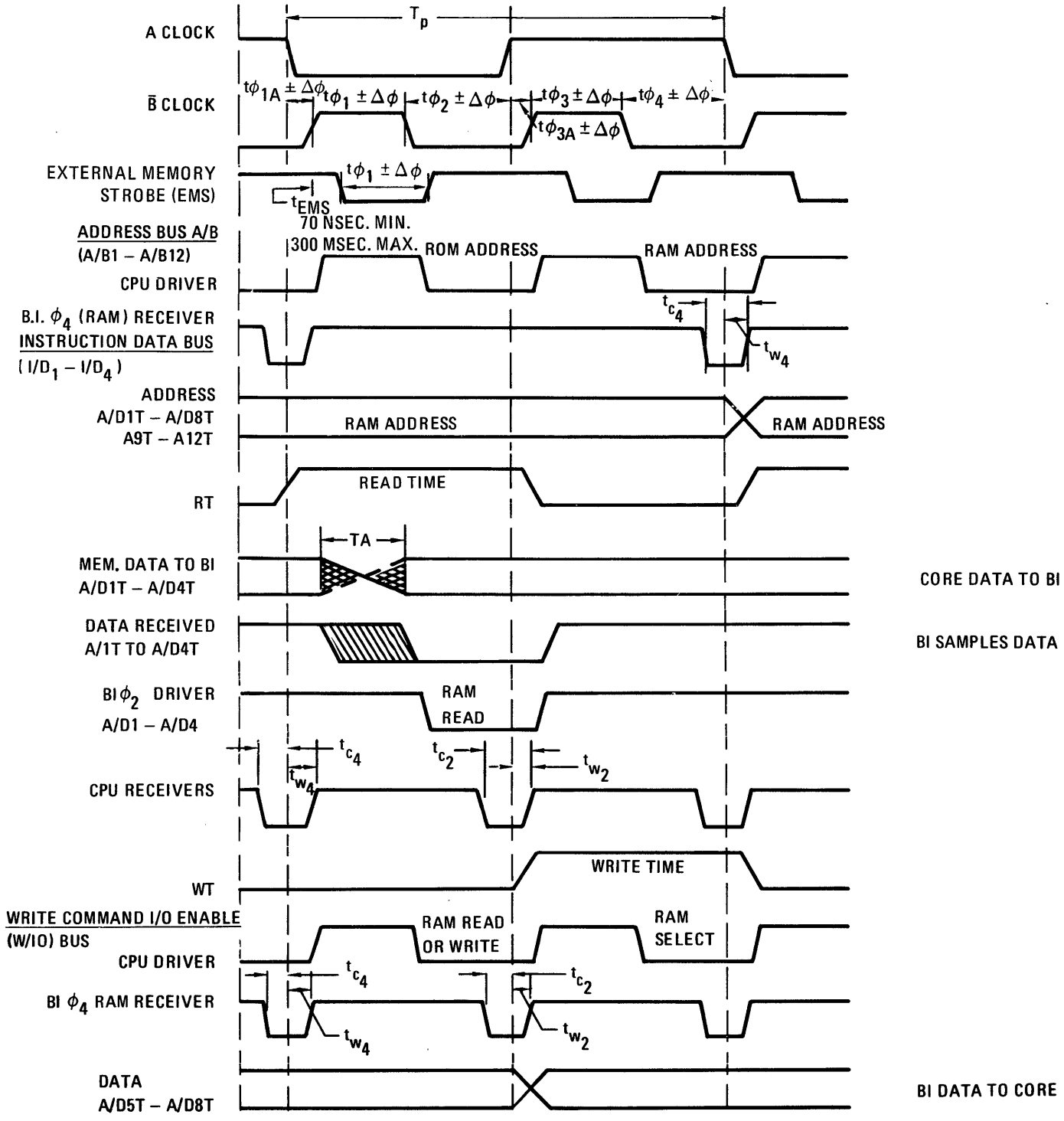
For clock frequencies above 199 kHz, the multiplex bus interface capacitive drive must be derated. For example, at 256 kHz (3.58 MHz ÷ 14), the maximum allowable system bus load must not exceed 100 pF.

TIMING DIAGRAM* RAM

A.C. CHARACTERISTICS
SYSTEM CLOCK PHASE

(See Table of AC Characteristics for Additional Details)

		ϕ4	ϕ1A	ϕ1	ϕ2	ϕ3A	ϕ3	ϕ4	ϕ1A	ϕ1
CLOCK TIMING RATIO	S18 = 1 (÷18)	1/18	4/18	4/18	1/18	4/18	4/18	1/18	4/18
	S14 = 1 (÷14)	3/14	3/14	3/14	1/14	3/14	3/14	1/14	3/14
	S12 = 1 (÷12)	2/12	2/12	3/12	1/12	2/12	3/12	1/12	2/12



*Timing is defined as the waveform passes through the -6V level.

FIGURE 7. RAM TIMING DIAGRAM

AC CHARACTERISTICS

(See Figures 6 and 7 for Timing Diagrams)

Symbol	Test	Min	Typ (1)	Max	Units	Conditions and Comments
T_P	Timing period of clock		5.01		μsec	Clock select ÷ 18 (199 KHz)
			3.91		μsec	Clock select ÷ 14 (256 KHz)
$\Delta\phi$	Time variations of phase intervals		20	.40	nsec	
$t\phi_n$	Time duration of phases 1, 2, 3, 4		1.11		μsec	Clock select ÷ 18 (199 KHz)
			0.836		μsec	Clock select ÷ 14 (256 KHz)
$t\phi_{1A} = t\phi_{3A}$	Time duration of phases 1A and 3A		279		nsec	Clock select ÷ 18 (199 KHz)
			279		nsec	Clock select ÷ 14 (256 KHz)
t_c2	Phase 2 input charge time	150	200		nsec	Data must be stable
t_c4	Phase 4 input charge time	150			nsec	Data must be stable
t_w2	Window time phase 2	350			nsec	Data must be stable
t_w4	Window time phase 4	350			nsec	Data must be stable
$t_{fc} = t_{rc}$	Clock fall and rise time	10		120	nsec	Load A = Load B, which is between 50 and 100 pF
T_A	Access time			1	μsec	Using 5.01 sec clock
				836	nsec	Using 3.91 sec clock
t_{EMS}	Time delay between $\overline{B}$ clock and EMS	70		300	nsec	Load = 30 pF

$T_A = 0^oC$ to $+70^oC$; $V_{DD} = -17V \pm 5\%$; $V_{SS} = 0V$

(1) Typical values are at $T_A = 25^oC$.

BUS INTERFACE ELECTRICAL SPECIFICATIONS

OPERATING LIMITATIONS AND CHARACTERISTICS

Supply Voltage:

VDD = -17 Volts ± 5% . . . . . (Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.) . . . . . (Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies: . . . . . 199 kHz or 256 kHz.

Operating Temperature (TA): . . . . . $0^{o}C$ to $70^{o}C$. (TA = $25^{o}C$ unless otherwise specified.)

Storage Temperature: . . . . . $-55^{o}C$ to $120^{o}C$.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . $|VDD - VSS|$ = 27 Volts Maximum.

Input Voltage with Respect to VSS . . . . . -27 Volts Maximum.

Maximum Positive Voltage on any Pin . . . . . +0.3 Volts.

Function	Symbol	Parameter	Limits Min	Limits Typ (1)	Limits Max	Unit	Test Conditions
Supply Current Average							VDD = -17.9V VSS = 0V
Supply Current	I_{DD}	Avg Supply Current			32	mA	199 KHz 350 pF
					35	mA	256 KHz 100 pF
Input and Output Characteristics — System Bus							VDD = -17.0V ± 5% VDA = -17.0V ± 5% VSS = 0V
Address Bus/	V_{IH}	Input High Level	-1.5		0.3	V	
Data Bus	V_{IL}	Input Low Level			▷1	V	
A/D_1 A/D_8	V_{OH}	V_{OUT} High Level	-1.0			V	
A9 - A12 CEA W/IO	V_{OL}	V_{OUT} Low Level			▷2	V	
Input and Output Characteristics — External Interface and Strapping — MOS							VDD = -17.0V ± 5% VDA = -17.0V ± 5% VSS = 0V
Address Bus/	V_{IH}	V_{IN} High Level	-1.5			V	
Data Bus Outputs	V_{IL}	V_{IN} Low Level			▷1	V	
A/D1T - A/D8T	V_{OH}	V_{OUT} High Level	-1.0			V	
A9T - A12T, EW15 CEAT, RT, WT	V_{OL}	V_{OUT} Low Level			▷2	V	
ADS, ADE1,	V_{IH}	Input High Level				V	
ADE2, CEA,* CES	V_{IL}	Input Low Level				V	
SPO	V_{IH}	V_{IN} High Level			0.3	V	VDD = -17.0V ± 5%
	V_{IL}	V_{IN} Low Level			▷1	V	
Input Clock Characteristics							VDD = -17.0V ± 5%
A, $\overline{B}$	V_{IH}	V_{IN} High Level				V	
	V_{IL}	V_{IN} Low Level				V	

BUS INTERFACE ELECTRICAL SPECIFICATIONS

Function	Symbol	Parameter	Limits Min	Limits Typ (1)	Limits Max	Unit	Test Conditions
Input and Output Characteristics – External Interface and Strapping – TTL VDA = -5V							VDD = -17.0V ± 5% VDA = -5.0V
Address Bus/ Data Bus TTL Outputs A/D1T - A/D8T A9T - A12T CEAT	V_{IH}	V_{IN} High Level	-1.0		0.3	V	
	V_{IL}	V_{IN} Low Level	-4.5		-4.2	V	
	V_{OH}	V_{OUT} High Level	-1.0			V	
	V_{OL}	V_{OUT} Low Level	-4.5		-4.8	V	
RT, WT, EMS	V_{OH}		-1.0			V	
	V_{OL}		-4.5		-4.8	V	
ADS, ADE1, ADE2, CEA,* CES	V_{IH}	Input High Level				V	
	V_{IL}	Input Low Level				V	
Capacitance							
All Logic Inputs and Outputs	C_{IN}	Input Capacitance			6	pF	
	C_{OUT}	Output Capacitance					
RT, WT, A/D1T - A/D8T, A9T-A12T	C_L	Load Capacitance			30	pF	
Off Input Resistance and Leakage Current							
All Logic Inputs and Outputs	R_{OFF}	Off Resistance	1 Meg			Ω	
	I_R	Input Leakage Current			10	μA	
Interface on Resistances Outputs							
TTL Outputs	R_{ON}	On Resistance			400	Ω	VDA =-5.0V I =-1.7 ma
TTL Outputs	R_{ON}	On Resistance			1000	Ω	VDA = -17.0V ±-5%
TTL Outputs	PUR	Pull Up Resistance	2K		4K	Ω	VDA =-5.0V

*All are straps except CEA (Chip Enable Address).

Note: 1. A V_{IH} translates to a corresponding V_{OH} and a V_{IL} translates to a corresponding V_{OL} which represents NO voltage inversion. However, when going from positive TTL logic to negative MOS logic, or vice versa, an inversion in the logic sense is seen.

2. Typical vales are at $T_A = 25^oC$.

3. Input and output voltage levels indicated by the ▷ symbols vary as a function of $|VDD|$ in accordance with the following equations. (The equations are applicable over the entire operating temperature range.)

(1) $V_{IL} = -(0.66\,|VDD| - 4.16)$ Example: If VDD = -17.0V, V_{IL} = -7.06V

(2) $V_{OL} = -(0.66\,|VDD| - 3.16)$ Example: If VDD = -17.0V, V_{OL} = -8.06V

SPECIAL INTERFACE CONSIDERATION

ADDRESS/DATA SIGNAL POLARITY

The BI circuit does not invert voltage levels from the PPS bus to the BI static outputs or from the BI static inputs to the PPS bus. That is, a most positive signal voltage into the BI is output as a most positive signal voltage no matter what the application or direction of signal flow. However, this does represent a logic inversion when going from negative PPS bus logic to positive TTL logic, or vice versa.

TTL DRIVERS

The 16 BI circuit outputs that have TTL drivers are WT, RT, CEAT, CLK$\overline{BT}$, A/D1T - A/D8T and A9T - A12T. Figure 8 shows a single TTL driver circuit which has a complementary MOS output Q_1 and Q_2.

For a TTL logic 1 output, Q_1 is on and has a 4KΩ maximum impedance to VSS. For a TTL logic 0 output, Q_2 is on and has a 400Ω maximum impedance to VDA.

BUS INTERFACE TTL RECEIVERS

The 8 BI circuit inputs that have TTL receivers are A/D1T - A/D8T. Figure 9 shows a single TTL receiver circuit. FET Q_1 is always on and functions as a load resistor for the TTL input, which allows the use of "Open Collectors" TTL drivers as well as regular TTL drivers.

The maximum impedance of Q_1 to VSS is 4KΩ.

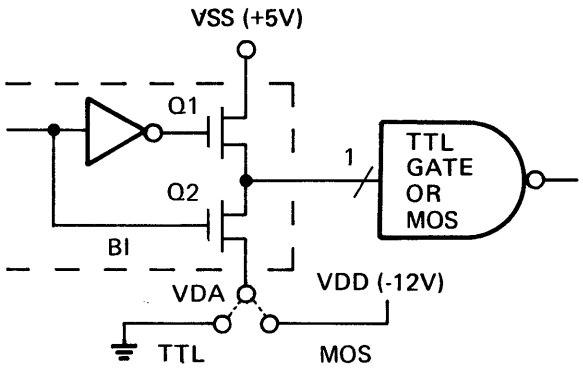


FIGURE 8. OUTPUT DRIVER SCHEMATIC

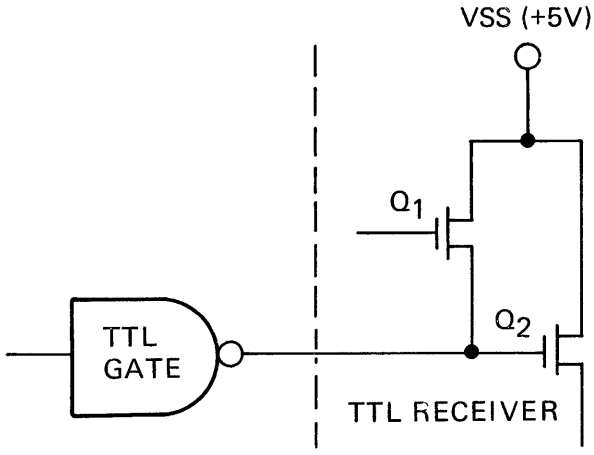


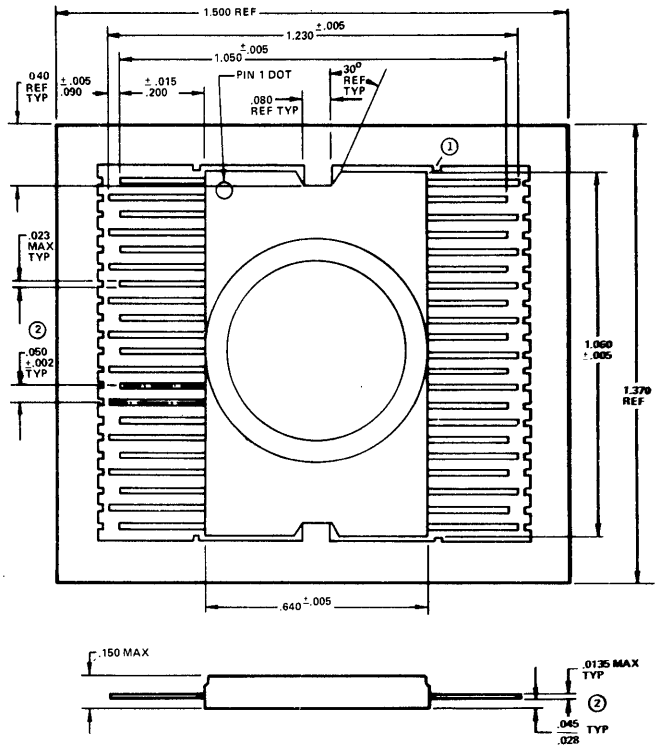
FIGURE 9. TTL RECEIVER SCHEMATIC

EVALUATION AND DEVELOPMENT BOARDS

The following printed circuit board assemblies are available from Rockwell to expedite fabrication of breadboard product prototypes which utilize the PPS family of circuits. All printed circuit boards are approximately 5" x 7" and have common address, data, and power pins which mate to a 100 pin card edge connector.

1. PPS Evaluation Board (P/N 20102D02):
   Contains one CPU (P/N 10660); two RAM's (P/N 10432); two GP I/O's (P/N 10696); one Clock (P/N 10706); and one crystal.
2. RAM Assembly (P/N 20102D17):
   Available with 0 to 8 RAM's (P/N 10432).
3. MOS ROM Assembly (P/N 20102D19):
   Contains circuitry for mounting up to eight MOS ROM's (P/N A05XX).
4. PPS Bus to TTL Interface Assembly (P/N 20102D27):
   Contains two BI's (P/N 10738) which provide demultiplexing, at either Ø2 or Ø4 times of the PPS address and data bus, to static TTL outputs and inputs. The TTL address outputs are buffered to provide a 30 TTL load fan-out capability. These outputs are available via the 100-pin connector and the 24-pin socket mounted on the printed circuit board.
5. PPS SOS/ROM Assembly (P/N 20102D30):
   Contains two BI's (P/N 10738) Selection Logic which provide interface from PPS Bus to SOS/ROM's and circuitry for mounting SOS/ROM's. The SOS/ROM can be used in the following configurations: 1K X 8 or 2K X 8 for ROM applications and 1K X 4 or 2K X 4 for ROM responding to RAM addresses for table look-up applications.
6. PPS PROM Assembly (P/N 20102D33):
   Contains two BI's (P/N 10738) and selection logic which provide interface from sockets for up to 16 National MM5203 or Intel 1702 erasable and programmable ROM's.
7. PPS GP I/O Assembly (P/N 20102D36):
   Contains four GPI/O's with TTL buffering and 24 pin sockets for connecting the GP I/O discrete inputs and outputs to external equipment.

STANDARD PACKAGE



1. BURRS UP TO 0.005" MAY OCCUR ON LEAD ENDS
2. TOOL HOLES IN LEAD FRAMES MAY BE FILLED WITH SOLDER
③ 3. STUBS ON LEAD FRAME OPTIONAL (TYPICAL 4 PLACES)
④ 4. DIMENSIONS ONLY APPLY WHERE LEADS LEAVE BODY

Rockwell International

Microelectronic Device Division
3310 Miraloma Avenue
P. O. Box 3669
Anaheim, California 92803

Document No. 10696 N22
January 5, 1974

APPLICATION NOTES

PRELIMINARY

PARALLEL PROCESSING SYSTEM (PPS-4)

PPS-4 GENERAL PURPOSE INPUT/OUTPUT (GP I/O) DEVICE PART NO. 10696

Prepared by K. H. HARLAN

NOTICE

Information provided in this Application Note is for reference purposes only and is subject to change without notice.

For specific detail information on this device or any of our other advanced microelectronic devices please contact the nearest Rockwell International Microelectronic Device Division Office.

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INTRODUCTION

General Purpose Input/Output device Part No. 10696 is manufactured by Rockwell Microelectronic Device Division using advanced MOS technology. The General Purpose Input/Output device (GP I/O) is used to interface external input systems and output devices to the Rockwell Parallel Processing System (PPS-4).

This document provides applications oriented data for the GP I/O. Additional data on the GP I/O, the overall PPS-4 system, and the related programming requirements can be found in the following documents.

PPS-4 Basic Devices Data Sheet
Pub. No. 2519-D-13 (311), Document No. 29003 N11

Parallel Processing System Application Notes
No. 2518-D-17

Operating Manual for PPS-4 Microprogram Development Using the TYMCOM-X System
Doc. No. 29002 N20

Operating Manual for PPS-4 Microprogram Development Using the General Electric MARK III System
Doc. No. 29004 N20

PPS-4 Evaluation and Development Modules Data Sheet
Pub. No. 2519-D-20, Doc. No. 29004 N41

DESCRIPTION

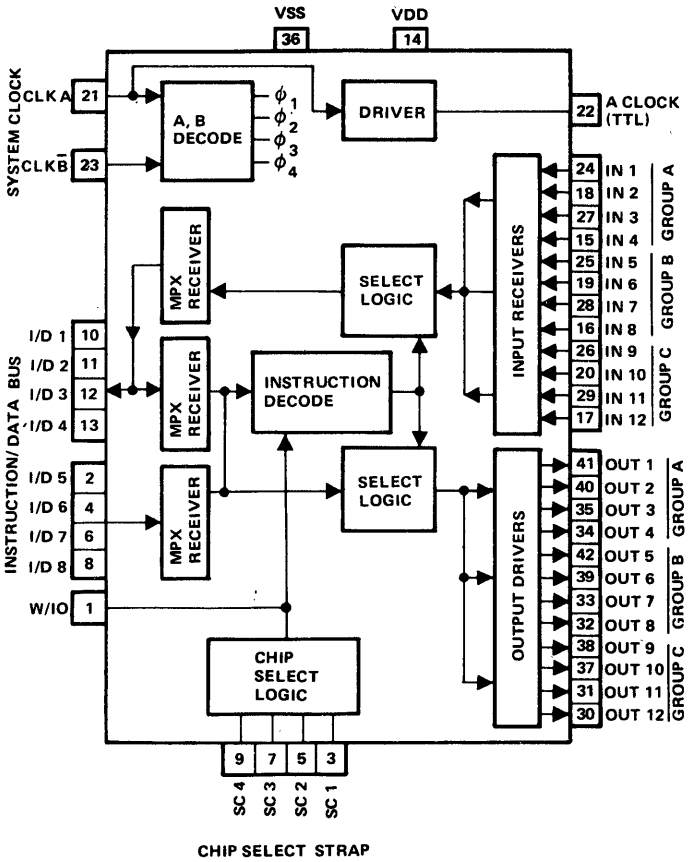


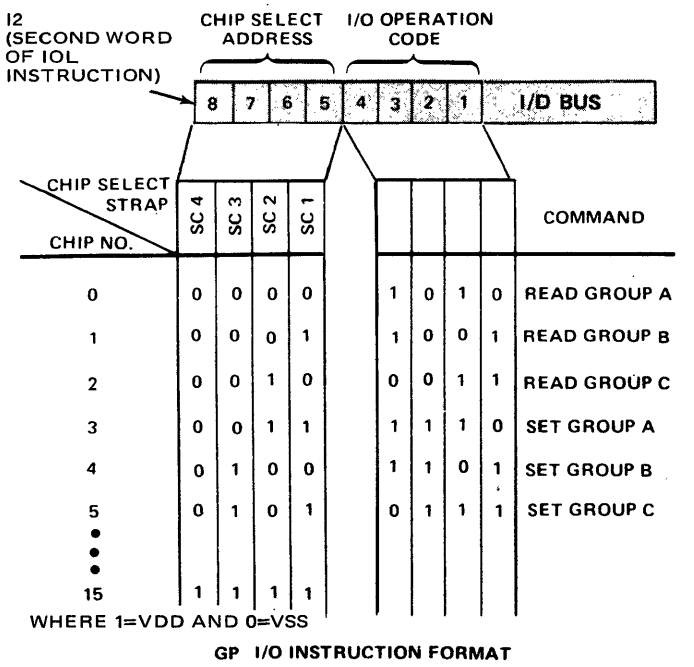
Figure 1. General Purpose Input/Output Block Diagram, P/N 10696

The General Purpose Input/Output device (GP I/O) is used to interface external devices to the PPS-4 system through TTL compatible interconnections. As shown in Figure 1, there are 12 inputs and 12 outputs which are arranged in six groups of four lines each. Direct addressing of up to sixteen GP I/O devices is possible by use of chip address straps. All of the GP I/Os are enabled with an I/O enable signal from the CPU, and one specific GP I/O is then accessed and commanded by a simultaneous 8-bit word from ROM. The I/O enable signal from the CPU is the result of the first word (I1) of the IOL instruction, and the second 8-bit word (I2) is the GP I/O address and instruction. Four bits of the second word are used to address the particular GP I/O chip and the other four bits are the operation code used to define which of the three input groups or three output groups will be used.

The 4-bit operation code is interpreted by the GP I/O to either copy the contents of the CPU accumulator into one of the three 4-bit parallel output drivers (registers) A, B, or C or transfer data from one of the 4-bit parallel input receivers A, B, or C into the accumulator of the CPU. The output drivers are static outputs and data remains in the output registers until altered by another IOL command. Bits 1 through 4 of the instruction word are commands to the GP I/O while bits 5 through 8 are used to address 1 of 16 possible GP I/O chips. The four GP I/O select inputs (straps) terminated by the user, create the addresses for each GP I/O circuit. The codes required in I2 (bits 1 through 4) of the IOL instruction for the normal operation are shown in Table 1. Six codes of the 16 possible codes are shown, three for input and three for output. The codes shown allow selection of only one group at a time. These are the only codes shown in the Data Sheet (Pub. No. 2519-D-13-308) and in the Programming Manual (Pub. No. 2520-D-26-305R).

DESCRIPTION

Table 1. GP I/O Instruction Format



However, the GP I/O chip is implemented using minimum decoding of the I2 bits 1 through 4, which means that all 16 possible combinations are valid.

Table 2 provides a complete tabulation of the I2 decode and the result. Note that when two or more groups are selected for read, the accumulator will copy the logical OR of the groups selected. When in the set mode each group selected will be set to the accumulator value. For operation code "B" no group is selected and the accumulator will copy all zeros from the data bus. A read example and a set example are shown following Table 2.

The GP I/O can execute an I/O read instruction using several different techniques. The following text describes two techniques, or methods, of executing the I/O instruction. The first technique, designated method A, is a typical program while the second technique, designated method B, is a more efficient program for special applications. In the example shown in Figure 2, 12 input lines are tested for bit status. Typically, the programmer first desires to know if any one of the 12 inputs is set.

Programming method A reads each of the three groups (A, B, and C) individually and tests for zero. If the first group is zero, the next group is read and tested. If the second group is zero, the third group is read and tested. If all three groups are zero a return and skip is executed which will initiate re-entry to the main program. If any group is not zero, a return is executed and transfer to a subroutine (TM CHECK) is made to determine which bit was set.

Table 2. GP I/O Operation Coding

I/O OPERATION CODE I2(4:1) BIT

GROUP SELECTED { X = selected, – = not selected

HEX	4	3	2	1		C	B	A	
					READ				
0	0	0	0	0		X	X	X	If two or three groups are selected the accumulator will copy the logical "OR" value of the selected groups.
1	0	0	0	1		X	X	–	
2	0	0	1	0		X	–	X	
3	0	0	1	1		X	–	–	
8	1	0	0	0		–	X	X	
9	1	0	0	1		–	X	–	
A	1	0	1	0		–	–	X	
B	1	0	1	1		–	–	–	
					SET				
4	0	1	0	0		X	X	X	If two or three groups are selected the accumulator contents will be copied to each selected group.
5	0	1	0	1		X	X	–	
6	0	1	1	0		X	–	X	
7	0	1	1	1		X	–	–	
C	1	1	0	0		–	X	X	
D	1	1	0	1		–	X	–	
E	1	1	1	0		–	–	X	
F	1	1	1	1		–	–	–	

Shading indicates the six codes shown in Table 1.

READ EXAMPLE:

If the operation code = 8

	Data
Group A – Selected	= 1 0 1 1
Group B – Selected	= 0 1 1 0
Group C – Not Selected	
Copy to Accum	= 1 1 1 1

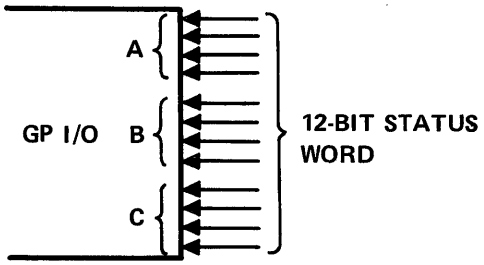
SET EXAMPLE:

If the Operation code = 5

Accumulator = 1 0 1 0

Group A – Not Selected, Output = No Change
Group B – Selected, Output = 1 0 1 0
Group C – Selected, Output = 1 0 1 0

DESCRIPTION




```
METHOD A                    METHOD B

    TM      STAT                TM      STAT
    TM      CHECK               TM      CHECK

STAT IOL     0A          STAT IOL     00
     SKZ                         SKZ
     RTN                         RTN
     IOL     09                  RTNSK
     SKZ
     RTN
     IOL     03          IOL 00; READS ALL GROUPS.
     SKZ                         IF ALL INPUTS ARE
     RTN                         ZERO A RTN TO MAIN
     RTNSK                       LINE PROGRAM IS
                                 EXECUTED, IF NOT TM
                                 TO GSTAT SUBROU-
                                 TINE IS EXECUTED
                                 WHICH WILL READ
                                 EACH GROUP AND
                                 STORE STATUS.
```

Figure 2. Simultaneous Scan of Input Groups

```
METHOD A                    METHOD B

    TL      CLEAR               TL      CLEAR

CLEAR LDI    0
      IOL    0E          CLEAR LDI    0
      LDI    0                 IOL    04
      IOL    0D
      LDI    0
      IOL    07
```

Figure 3. Set All Output Groups to Zero

Method B takes advantage of the IOL instruction to read all three groups simultaneously to determine if any of the 12 inputs is set. The IOL instruction 00 will read the ORed inputs of groups A, B, and C, (See Table 2). If any one or more than one bit is set the ORed result will not be zero and a return will be executed and a transfer to a subroutine (TM CHECK) is made to determine which bit(s) were set. If all 12 bits are zero the ORed inputs will be zero and a skip will result, and a return and skip will be executed causing the re-entry to the main program.

Note that method B requires only 5 instructions and method A requires 13 instructions to execute the I/O test instruction.

Another use of the multiple group selection codes is to initialize all outputs to zero at power turn-on. As shown in Figure 3, two programming methods are available to zero all outputs. Method A, which clears each group separately, is currently in common usage. Method B, which is introduced in this document, uses a new technique explained in the following text which reduces the time required substantially.

For Method A, the programmer generates a subroutine similar to the one shown in Figure 3 Method A, using only the operation codes in Table 1. The sequence requires an LDI and IOL instruction for each of the three groups of outputs. The accumulator must be reinitialized after each IOL due to the nature of the IOL instruction which always copies the I/D bus into the the accumulator during $\phi 2$ of the instruction. Method A requires nine instruction words to execute.

Method B represents a more efficient method of setting all outputs to zero. As shown in Figure 3, the subroutine for Method B first loads the accumulator with zeroes, and via the IOL instruction using an operation code equal to 4, (See Table 2) sets all 12 outputs to zero within one IOL instruction time. Method B requires only three instruction words to execute which reduces both ROM requirements and operation time. Note that in all examples, the address of the GP I/O is 0000. For a GP I/O address of 1111 (F_{16}) then the instruction in, for example, method B above would be IOL F4 instead of IOL 04.

Document No. 10788 N11
Rev 2. Sept 1974

DATA SHEET

PARALLEL PROCESSING SYSTEM (PPS)

GENERAL PURPOSE KEYBOARD AND DISPLAY (GPKD) CIRCUIT

PART NO. 10788

Rockwell International
Microelectronic Device Division

NOTICE

Information provided in this Data Sheet is for reference purposes only, and is subject to change without notice.

For specific detail information on this device or for information on any of our other advanced microelectronic devices, please contact the nearest Rockwell International Microelectronic Device Division office.

RELATED PUBLICATIONS

1. PPS-4 Basic Devices, Data Sheet, Document No. 29003 N11
2. MOS/LSI PPS Programmer's Reference Manual.
   Pub. No. 2520-D-26 305R, Document No. 29001 N40
3. PPS-4 Microprogram Development Using the General Electric MARK III System. Document No. 29004 N20.
4. PPS-4 Microprogram Development Using the TYMCOM-X System. Document No. 29002 N20.
5. PPS-4 Evaluation and Development Modules.
   Document No. 29004-41.

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INTRODUCTION

This data sheet describes General Purpose Keyboard and Display circuit P/N 10788, manufactured by the Microelectronic Device Division of Rockwell International. This versatile circuit provides the optimum method of interfacing the Rockwell Parallel Processing System (PPS) to a wide variety of keyboards and display devices. The General Purpose Keyboard and Display (GPKD) circuit interfaces the functional circuits in the PPS with the majority of business machine, Point-of-Sale (POS), and calculator keyboards and displays as shown in Figure 1.

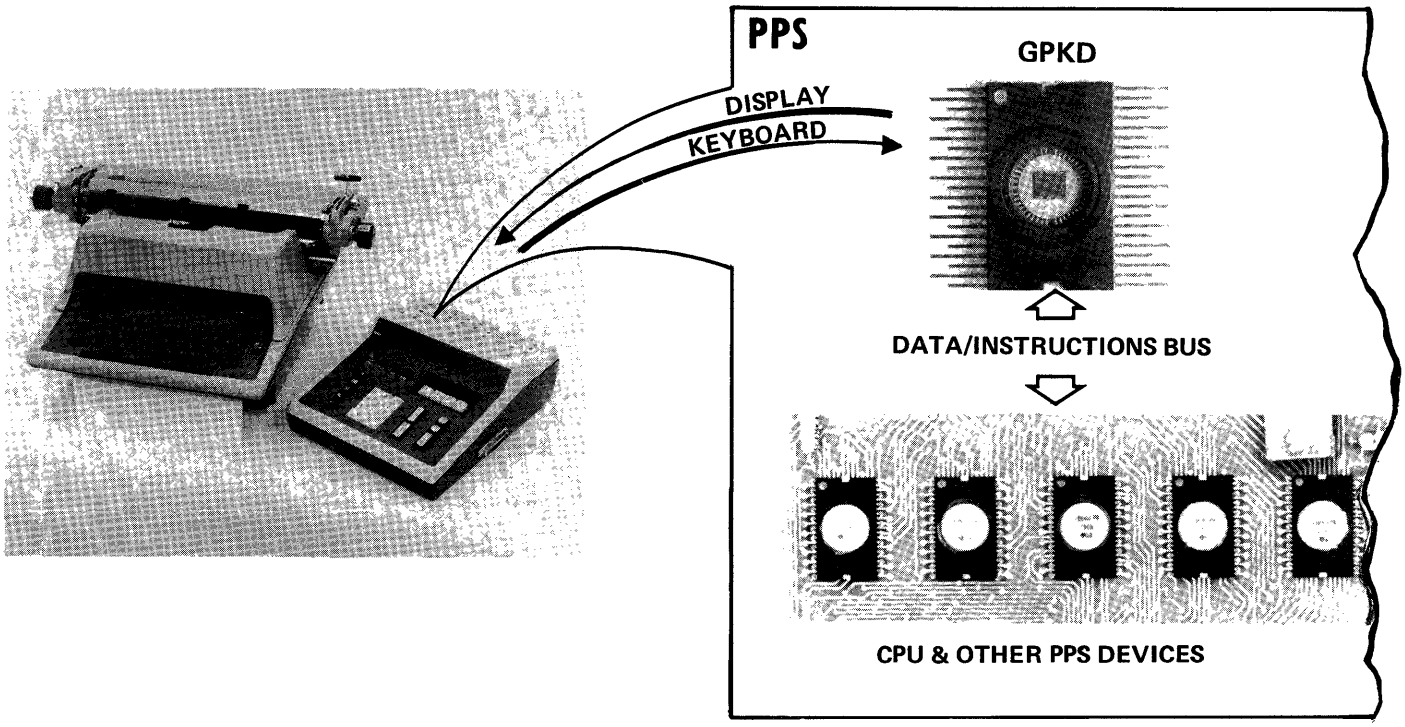


Figure 1. Typical Keyboard and Display Application

FEATURES

Keyboard

- Nine-Key Buffering
- Two-Key Rollover
- 7.68 msec Key Debounce Delay
- Handle up to 64 keys on 8 x 8 matrix
- Chip Address Strap Encoded
- Initialized at Power On (SPO)

Display

- Display up to 16 characters
- 32 Digits of Display Possible
- Two 16-Digit Display Buffers
- Two Sets of Hexadecimal Code Outputs for Display
- TTL Compatible Interface
- 5% Duty Cycle

PPS INTERFACE FEATURES

The General Purpose Keyboard and Display circuit (GPKD) connects directly with the PPS data bus. The GPKD is initialized by the Synchronized Power-On (SPO) signal from the CPU.

KEYBOARD FEATURES

The GPKD strobes up to 64 single-pole, single-throw momentary switches on an 8 x 8 matrix and provides a 7.68 msec debounce delay for these switches. A 9-level, 8-bit key buffer allows up to nine key inputs to be stored until the PPS processes them. Inputs can be entered at an operating speed of 7.68 msec/character.

DISPLAY FEATURES

The GPKD synchronizes and strobes up to 16 characters of display data which are outputted in two hexadecimal groups. The two hexadecimal groups of data, designated as Group A and Group B, may be used as one group of 8-bit data or several groups of data composed of less than 8 bits. A typical application of the data display is to use 4 bits of data for numeric display, 2 bits for decimal point and comma, and the remaining 2 bits for display up to 32 status indicators. It is also possible to display 32 consecutive digits of numeric data and some symbols when two 16-digit hexadecimal groups are treated as one 32-digit hexadecimal code.

FUNCTIONAL DESCRIPTION

The GPKD block diagram (Figure 2) shows the various functional circuits in the GPKD. The functional circuits are as follows:

- Chip Select Decode
- Command Decoding
- Bit Time Counter
- Scan Counter
- Display Register Control
- Display Register A
- Display Register B
- Display Bank Select
- Strobe Select
- Return Sampling
- Key Buffer Register Control
- Key Buffer Registers
- Key Code Transfer Control

The following paragraphs discuss the functional elements.

Chip Select Decode

The chip select decode circuit compares the chip address data on data bus lines I/D5, I/D6, and I/D7 to the data on chip select straps SC5, SC6, and SC7. If the result is the same and the W/IO and I/D8 lines are true, the GPKD is selected.

Command Decoding

The command decoding circuit determines which of the eight GPKD commands listed in Table 1 will be executed. The chip select decode logic enables the command decoding, which decodes the command inputs I/D1, I/D2, I/D3 and I/D4.

Bit Time Counter

The bit time counter divides the PPS clock frequency by 8 to provide increment timing of the scan counter. One bit time equals one basic PPS cycle time, (typically 5 usec).

Scan Counter

The scan counter provides timing signals for the display register control, display bank select, return sampling, key buffer register control, and strobe select functions. The scan counter updates its count once every 8 bit times by using the bit time counter output.

The 8-bit codes generated by the scan counter represent corresponding keys on the key matrix. (See Table 2 for key codes.) Upon a detection of a key depression, the scan counter content at that moment represents the depressed key and is transferred to the first key buffer register.

Display Register Control

The display register control logic controls load, shift, hold, turn on, and turn off of display registers A and B. The scan counter provides the synchronizing signal to the display register control, and the command decoding function provides the signal that controls the modes of the display registers.

Display Registers A and B

Display registers A and B are used to store display data. Each display register consists of four 16-bit storage registers. The contents of the storage registers can be changed only by I/O commands and, therefore, are independent of the system operations controlled by other than I/O commands. The display registers take the data from the data bus ID/5, ID/6, ID/7 and ID/8. Loading time and outputting of the display registers are controlled by display register control logic, which is governed by microprogrammed commands and the scan counter.

Each of the two display registers has four parallel open drain outputs each of which is capable of driving one TTL load. (See special interface considerations, page 11.) These outputs are synchronized with the strobe select lines and display bank select line. The outputs of display register A are designated DA1, DA2, DA3 and DA4, and the outputs of display register B are designated DB1, DB2, DB3 and DB4.

Display Bank Select

The display bank select combined with the eight strobe lines provides scanning for up to 16 characters of display. The display bank select output is designated as DBS. A VSS level on the DBS line selects the lower eight strobes and the VDD level on DBS selects the upper eight strobes, thus yielding a total of 16 strobes.

Strobe Select

The strobe select circuit sequentially outputs eight strobe signals designated X0 through X7, each on a separate output line. The first strobe occurs on X0, the second strobe occurs on X1, and strobes continue in sequence through X7, after which the strobes restart at X0. The strobes are used in forming an 8 by 8 XY keyboard matrix in which X corresponds to the strobe select lines and Y to the keyboard return lines. The strobe select, in conjunction with the display bank select, is also used for multiplexing up to 16 characters of display, (see Figure 8).

Return Sampling

The return sampling circuit tests the states of key matrix return lines from the keyboard. The results of the tests are used in the key buffer register control logic to determine the key status. The eight return lines from the keyboard XY matrix are designated Y0 through Y7.

Key Buffer Register Control

The key buffer register control performs the following two functions: (1) loads the key code generated by the scan counter into the first buffer register when the return sampling logic detects a key closure, and (2) controls the "first in, first out" operation of the key buffer registers.

Key Buffer Registers

The GPKD has nine 8-bit key buffer registers to store key codes (keyboard entries) until transferred out by PPS request. Upon a key closure detection, the corresponding code generated by the scan counter is loaded into the first key buffer register, then transferred to the next key buffer register if it is empty. If all nine buffer registers are full and another key is depressed the MSB of the ninth key code goes from 0 to 1, (See Table 2). A "1" in the MSB indicates to the CPU that the key buffer register storage capacity has been exceeded, and that one or more key entries may have been lost. The CPU will reset this error condition using the KER instruction, (See Table 1). The data in the first eight buffer registers will be accepted by the CPU as valid data.

Key Code Transfer Control

The key code transfer control outputs data from the last key buffer register to the I/D bus upon request by the PPS CPU. The output of data is handled on a "first in, first out" basis.

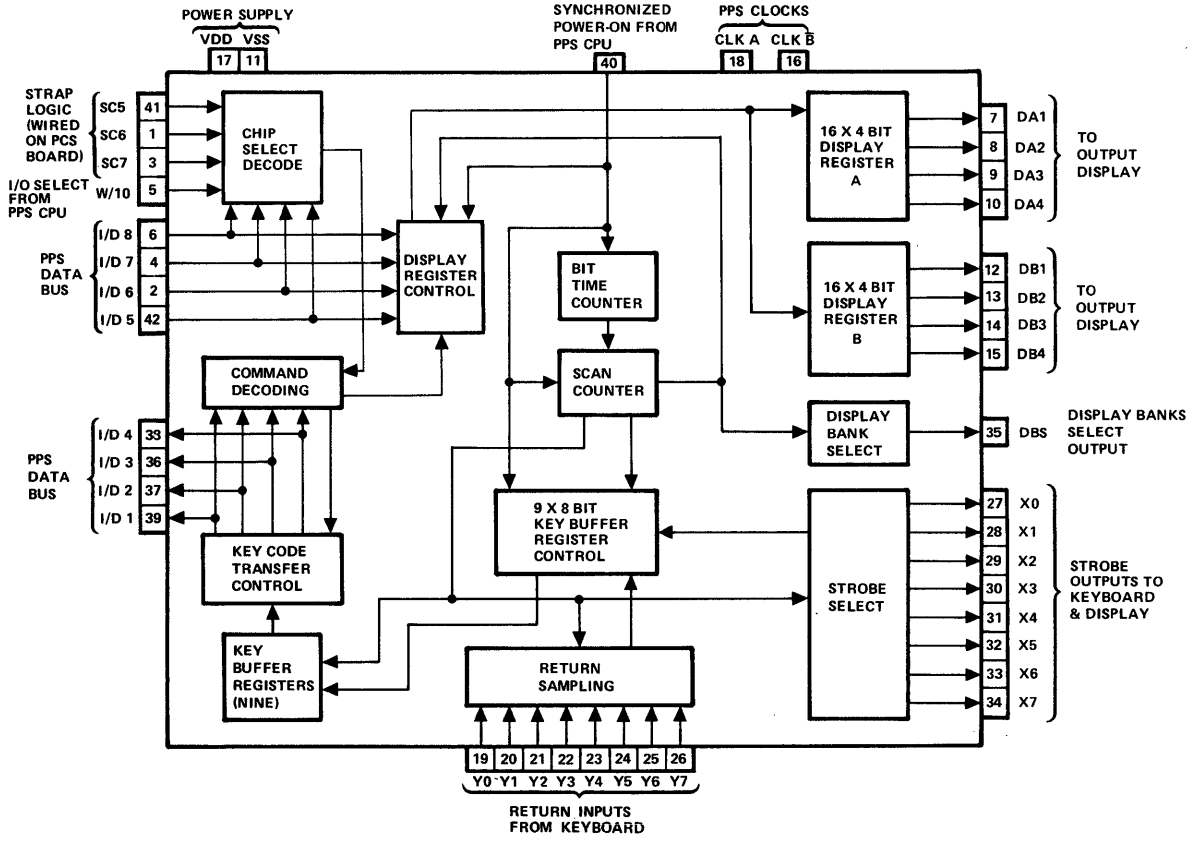


Figure 2. General Purpose Keyboard and Display (GPKD) Block Diagram

OPERATION (CPU GPKD INTERFACE)

GENERAL

The operation of the GPKD is divided into three functions for explanation purposes. These functions are as follows:

1. PPS CPU Interface to GPKD
2. Keyboard Interface to GPKD
3. Display Interface to GPKD

A simplified schematic diagram showing the GPKD Interface with a Panaplex display is given in Figure 10. A similar schematic showing the GPKD Interface with Light Emitting Diodes (LED) displays is shown in Figure 11. Table 1 lists the PPS IOL instructions which are used with the GPKD chip.

PPS CPU INTERFACE TO THE GPKD

Physical interconnection of the CPU to the GPKD is accomplished by connecting CPU lines to GPKD circuit pins of the same designation. The interface is shown in Figure 3. The CPU lines connected to the GPKD are I/D1 - I/D8, SPO, and W/IO.

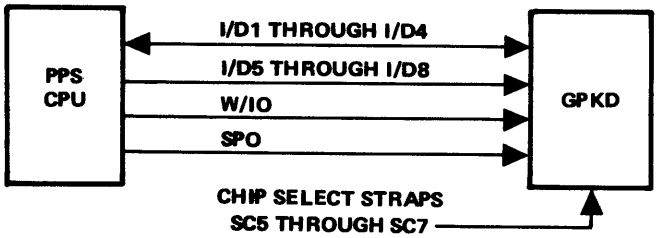


Figure 3. CPU to GPKD Interface

Electrically, chip selection requires that strap lines SC5, SC6, and SC7 on the GPKD be terminated at logic levels which correspond with the desired address coding on I/D bus lines I/D5, I/D6, and I/D7 and that I/D8 be at the VDD level. For example, a GPKD with all straps terminated to VDD (the most-negative voltage) is addressed when bits I/D5 through I/D8 are all logic ones (the most-negative voltage). Activation of the GPKD requires both the proper address on the I/D bus and the W/IO line to be a logic one at Ø4 of the second cycle of a two-cycle microinstruction. Refer to the paragraph on PPS GPKD SYSTEM TIMING for details on interface timing.

Functionally, the PPS system requires an IOL instruction when it needs to control one of the system's I/O chips. Each IOL instruction consists of two words. The first word automatically initiates generation of a chip select enable signal (W/IO) by the CPU. The most significant half of the second word (on data bus I/D5 through I/D8) designates an address of an I/O chip. This address, with W/IO signal true, selects only one I/O chip at a time. The least significant half of the second word (on data bus I/D1 through I/D4) is the real command which instructs the I/O chip what to do with the data.

Table 1. GPKD Instructions

Instruction MNEMONIC	W/IO	OP Codes, 2nd Word of Two Word IOL								Names	Descriptions
		Chip Select I/D				Command I/D					
		8	7	6	5	4	3	2	1		
KTR	1	1	X	X	X	1	1	0	0	Transfer Keyboard Return	Key Return → Data Bus I/D1, I/D2, I/D3, I/D4
KTS	1	1	X	X	X	1	0	1	0	Transfer Keyboard Strobe	Key Strobe → Data Bus I/D1, I/D2, I/D3, I/D4
KLA	1	1	X	X	X	1	1	1	0	Load Display Register A	Data Bus I/D5, I/D6, I/D7, I/D8 → Data Reg. A
KLB	1	1	X	X	X	1	1	0	1	Load Display Register B	Data Bus I/D5, I/D6, I/D7, I/D8 → Data Reg. B
KDN	1	1	X	X	X	0	0	1	1	Turn on Display	Turn on Display
KAF	1	1	X	X	X	1	0	1	1	Turn Off A	Blank the Display of DA1, DA2, DA3, DA4, DB1 and DB2
KBF	1	1	X	X	X	0	1	1	1	Turn Off B	Blank the Display of DB3 and DB4
KER	1	1	X	X	X	0	1	1	0	Reset Keyboard Error	0 → Keyboard Error Flip-Flop and Key Buffer Registers

NOTES:
1. W/IO is generated by the first word of the PPS IOL instruction.
2. Polarities of I/D7, I/D6 and I/D5 must be same as the polarities of chip select straps SC7, SC6 and SC5, respectively.
3. KLA resets DA1-DA4 and DB1 and DB2 to VSS level. KLB resets DB3 and DB4 to VSS level.
4. KAF or KBF is used to blank the display without changing the contents of display data registers.
5. KAF resets output line DA1, DA2, DA3, DA4, DB1 and DB2 to VSS level. KBF resets output lines DB3 and DB4 to VSS level.
6. KAF stops the circulation of the display register A, and KBF stops the circulation of display register B.
7. KER takes a maximum of 10-bit times to complete. Therefore, there must be at least 10-bit times between KER and the next KTS instruction.

PPS GPKD System Timing

All GPKD instructions are two-cycle microinstructions; Figure 4 shows the timing for a single GPKD instruction. The illustration also shows the manipulation of address and data, and the relationship of this address and data-bus information to the W/IO enable line information and phase-timing.

The PPS IOL microinstructions used to command the GPKD are listed in Table 1. Each IOL microinstruction command occupies two words in ROM and requires two clock cycle times to execute. The first word of an IOL instruction causes the CPU to generate the IOL enable signal W/IO. The second word of the IOL instruction contains the chip select address and defines the particular IOL command to be executed. (See Table 1.)

The sequence of events is as follows: As shown in Figure 4 the first word of an IOL instruction in ROM is addressed during phase 2 of the first clock cycle. This first word is transferred from ROM to the CPU during phase 4 of the first clock cycle to initiate generation of the W/IO enable signal in the CPU. During phase 2 of the second clock cycle the second word of the IOL instruction in ROM is addressed. During phase 4 of the second clock cycle the second word is transferred from ROM to the I/O. At the same time the W/IO enable signal is transferred from the CPU to the I/O. The second word contains one of the GPKD commands listed in Table 1 and is decoded as follows:

1. I/D5 through I/D8 designate GPKD address.
2. I/D1 through I/D4 designate GPKD functions.

During the two clock cycle times just described the desired IOL instruction (GPKD command) has been transferred from ROM and placed in I/O, and the CPU has generated the data enable signal W/IO. During phase 2 of the next cycle time the W/IO signal commands the RAM to stay off the data bus and the data transfer between the GPKD and the CPU takes place. That is, I/D5 through I/D8 transfer data from the CPU accumulator to the GPKD and I/D1 through I/D4 transfer data from the GPKD to the CPU accumulator. Data transferring from the CPU accumulator to the data bus is inverted, and data on the data bus is inverted before entering the CPU accumulator.

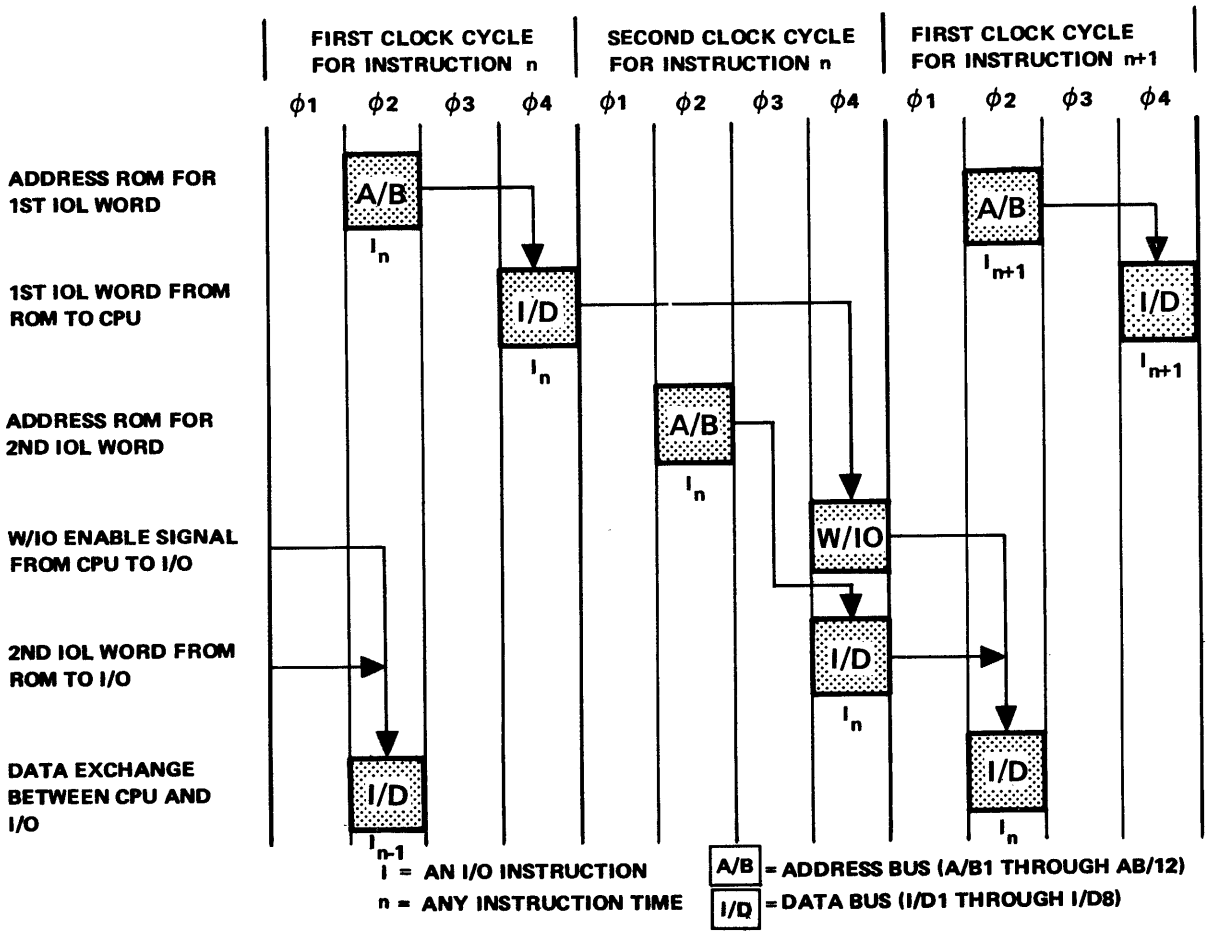


Figure 4. IOL (GPKD) Instruction Timing

KEYBOARD INTERFACE TO GPKD

The GPKD has 16 lines which form a keyboard matrix. Eight of the lines are strobe lines designated X0 through X7 and the other eight lines are return lines designated Y0 through Y7. Two IOL instructions are required to read in a designated key location, one instruction for strobe line data and the other instruction for return line data. Table 2 lists the strobe and return codes and Figure 5 shows the strobe and return lines timing. A typical connection between the keyboard matrix and GPKD is shown in Figure 6. An example of the keyboard read routine is provided in the flow diagram in Figure 7.

Table 2. Strobe and Return Codes

Strobes	I/D Bus Code				Returns	I/D Bus Code			
	I/D4	I/D3	I/D2	I/D1		I/D4	I/D3	I/D2	I/D1
No Key	0	0	0	0	–	–	–	–	–
X0	1	0	0	0	Y0	X	0	0	0
X1	1	0	0	1	Y1	X	0	0	1
X2	1	0	1	0	Y2	X	0	1	0
X3	1	0	1	1	Y3	X	0	1	1
X4	1	1	0	0	Y4	X	1	0	0
X5	1	1	0	1	Y5	X	1	0	1
X6	1	1	1	0	Y6	X	1	1	0
X7	1	1	1	1	Y7	X	1	1	1

NOTES:
1. The polarities shown in this table represent the polarities on the I/D data bus lines (1 = VDD, 0 = VSS).
2. For a strobe code a "1" on I/D4 indicates the presence of a key strobe.
3. For a return code I/D4 can be either polarity (X). A "0" means the capacity of the key buffer register is not exceeded; a "1" means the capacity is exceeded.

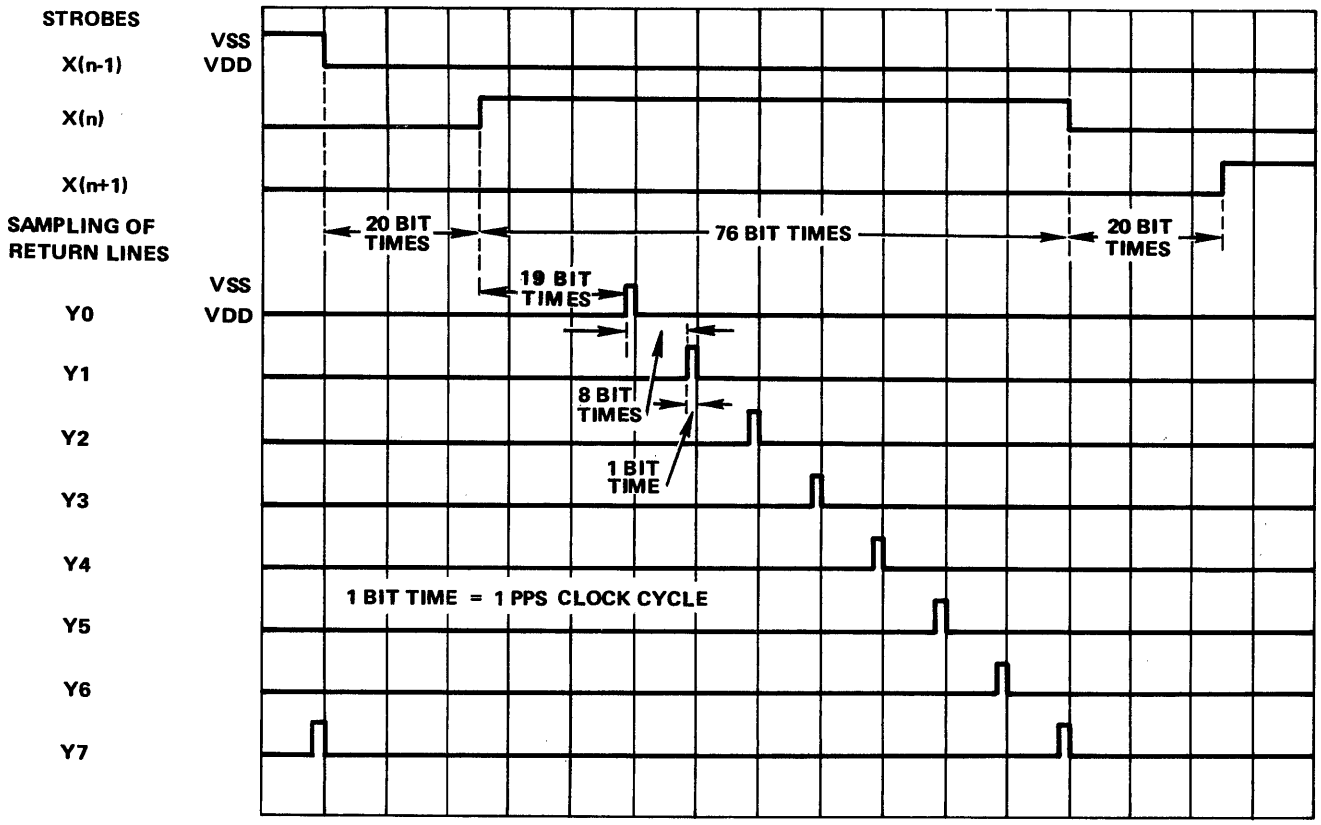


Figure 5. Timing of Strobe and Return Lines

Key Actuation Detection

Three possible conditions can result during keyboard operations. These conditions and the associated functions are described as follows:

1. Single Key Depression

   When a key is depressed, the corresponding key code is loaded into the first key buffer register and held there for one keyboard scan cycle (1536 bit times). If no other key is depressed during that period, the key code is defined as a single key depression and the key code is shifted to the next key buffer register, if the next key buffer register is available.

2. Simultaneous Key Depressions

   Depression of two or more keys within one keyboard scan cycle is defined as a simultaneous key depression. If this condition occurs, the GPKD ignores all keys depressed until only one key remains closed and all of the others are released. Then, the remaining key is treated as a single key depression.

3. Key Rollover

   If two keys are depressed with at least one keyboard scan cycle interval between them, the first depressed key is always detected first. If the second key is depressed with the first key down, the second key will be accepted when the first key is released. If the second key is released before the first key, the second key will be ignored. This action provides a two-key rollover feature if the first key depressed is always released first.

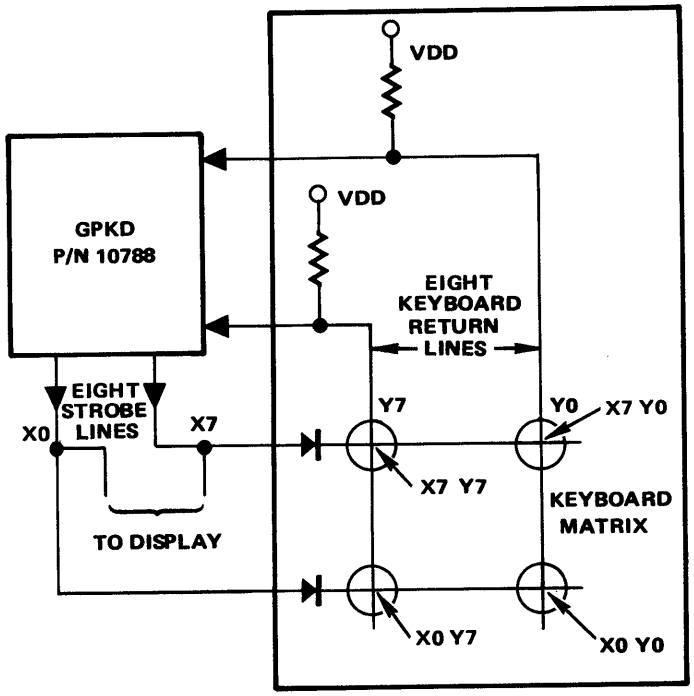
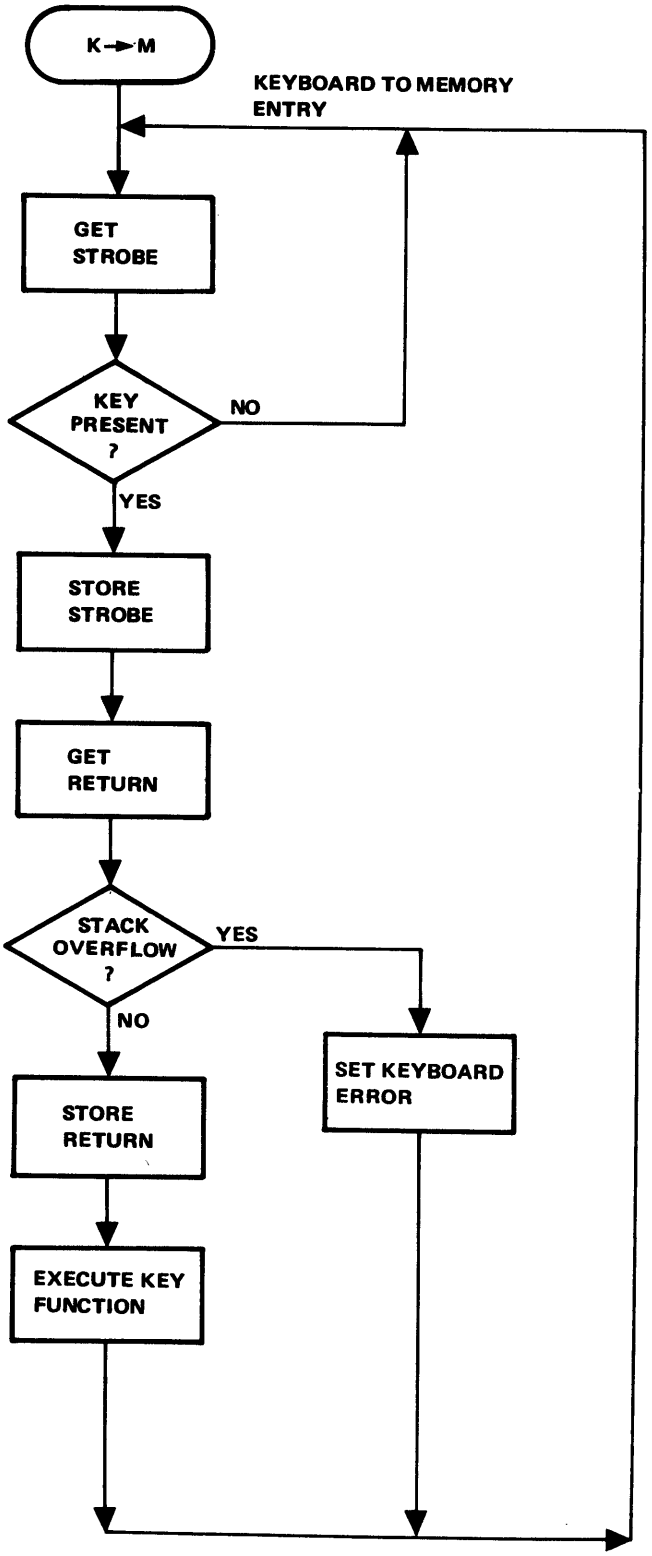


Figure 6. Keyboard to GPKD Interface



	TM	KEYIN	
ZKEYIN	IOL COMP	KTS	Get Strobe value
	ADI	8	Key present?
	T	ZKEYIN	No
	LBL EXD	STR	Yes Save Strobe value in RAM
	IOL COMP	KTR	Get Return value
	ADI	8	Keyboard stack overflow?
	ADI	8	No, restore value, skip
	TM	KBERROR	Yes, go to error processing routine
	EX		Save Return value in RAM
	TL	DECODE	Go to key decoder

AUXILIARY INFORMATION

KBERROR	PTR	ERROR
KEYIN	PTR	ZKEYIN
KTS	EQX	8A
KTR	EQX	8C
STR	EQX	IF

Figure 7. Keyboard to Memory Routine

DISPLAY INTERFACE TO GPKD

Two groups of four 16-bit registers are used to store display data. Each of these two register groups has four outputs and each output is capable of driving one TTL load. The GPKD is designed to use TTL logic to interface to the many different commercial displays. An example of an interface arrangement for a gas discharge display is shown in Figure 10. The required timing for extinguishing segments between strobes is provided within the device. Phosphorescent and L.E.D. displays can also be easily driven with appropriate TTL interface circuits. The select logic, segment decoder and driver, and the number of status lamps, latches, and drivers are determined by the particular product's requirements. The eight GPKD display register outputs can also be decoded to 256 different output lamps.

When the complete display is blanked by an IOL instruction or disabled between adjacent strobes, the data outputs (DA1 through DA4 and DB1 through DB4) are at the VSS level. When only specific display characters are to be blanked the data outputs to be decoded by external circuits must be at the VSS level. When any one or more of the DA or DB data outputs are used individually, the VSS level must be used as the off-level.

It should be noted that there is one level inversion between the data outputs of GPKD and the CPU accumulator.

Table 1 lists the five instructions related to display functions. These are KLA, KLB, KDN, KAF and KBF, and are in the second word of the IOL instruction. The digit selection is achieved by using the eight strobe select lines, X0 through X7, and the display bank select line, DBS. The DBS output is used to multiplex the eight strobes to give 16 separate strobes for up to 16 digits of display. The timing diagram in Figure 8 shows the display timing.

Flow Diagram, Figure 9, shows the sequence of events needed for displaying data. The first block shows that data may be formatted before display registers A and B are loaded via two IOL type instructions (KLA and KLB). Once the A and B registers are loaded, the display is turned on by the KDM instruction and the program returns to the main line program.

Data are loaded from the addressed RAM into display registers A and B through the CPU accumulator four bits (one digit) at a time. The sequence of loading is to read the least significant digit (LSD) out of RAM and load it into the most significant digit (MSD) position of the display register. During the next cycle the display register will shift its contents one digit position toward the LSD position and the next digit in the addressed RAM is loaded into the MSD position of the display register. This process is repeated until all 16 digit positions of the display register have been loaded. At the completion of the load cycle the MSD of the RAM will be in the MSD position of display register A and the LSD of the RAM will be in the LSD position of display register B. The data in the display register will be in the same format that it was in RAM. All 16 digits must be loaded each time a change in the display is desired.

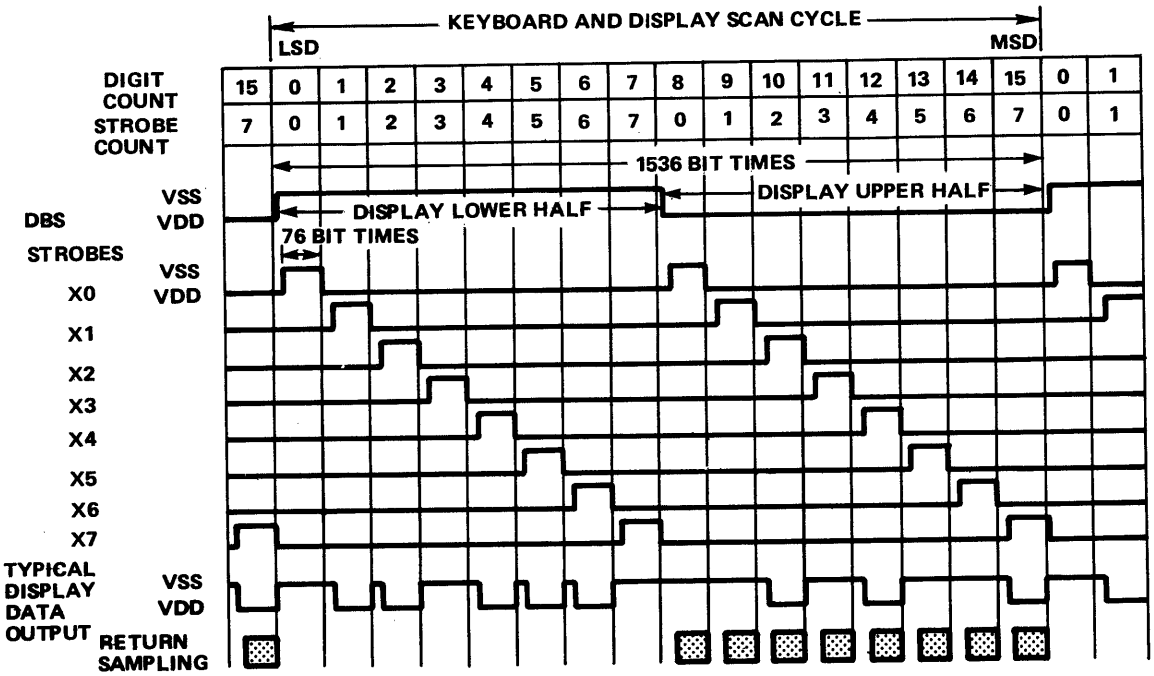
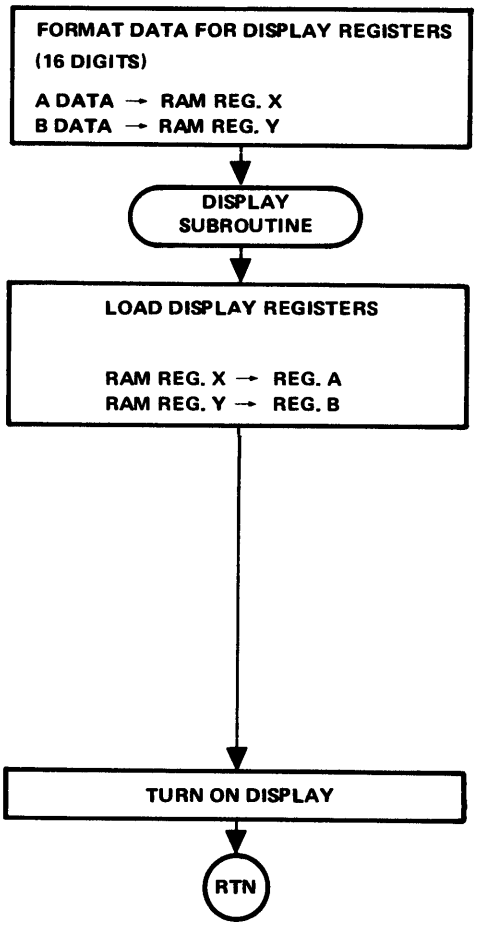


Figure 8. Display and Key Scan Timing

OPERATION (DISPLAY GPKD INTERFACE Continued)




```
                    TM      DISPL
                    |       |
                    ≈       ≈
                    |       |
ZDISPL              LBL     DBUF    Load RAM register A address
D1                  LD      1       Get digit from RAM register A
                                    and change RAM address to
                                    register B
                    IOL     KLA     Load display register A
                    LD      1       Get digit from RAM register B
                                    and change RAM address to
                                    register A
                    IOL     KLB     Load display register B
                    DECB            Last digit pair?
                    T       D1      No, do next digit pair
                    IOL     KDN     Turn on display
                    RTN
```

AUXILIARY INFORMATION

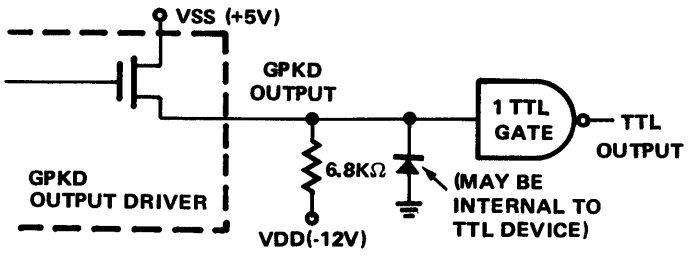
DISPL	PTR	ZDISPL
DBUF	EQX	EF
KLA	EQX	8E
KLB	EQX	8D
KDN	EQX	83

Figure 9. Memory to Display Routine

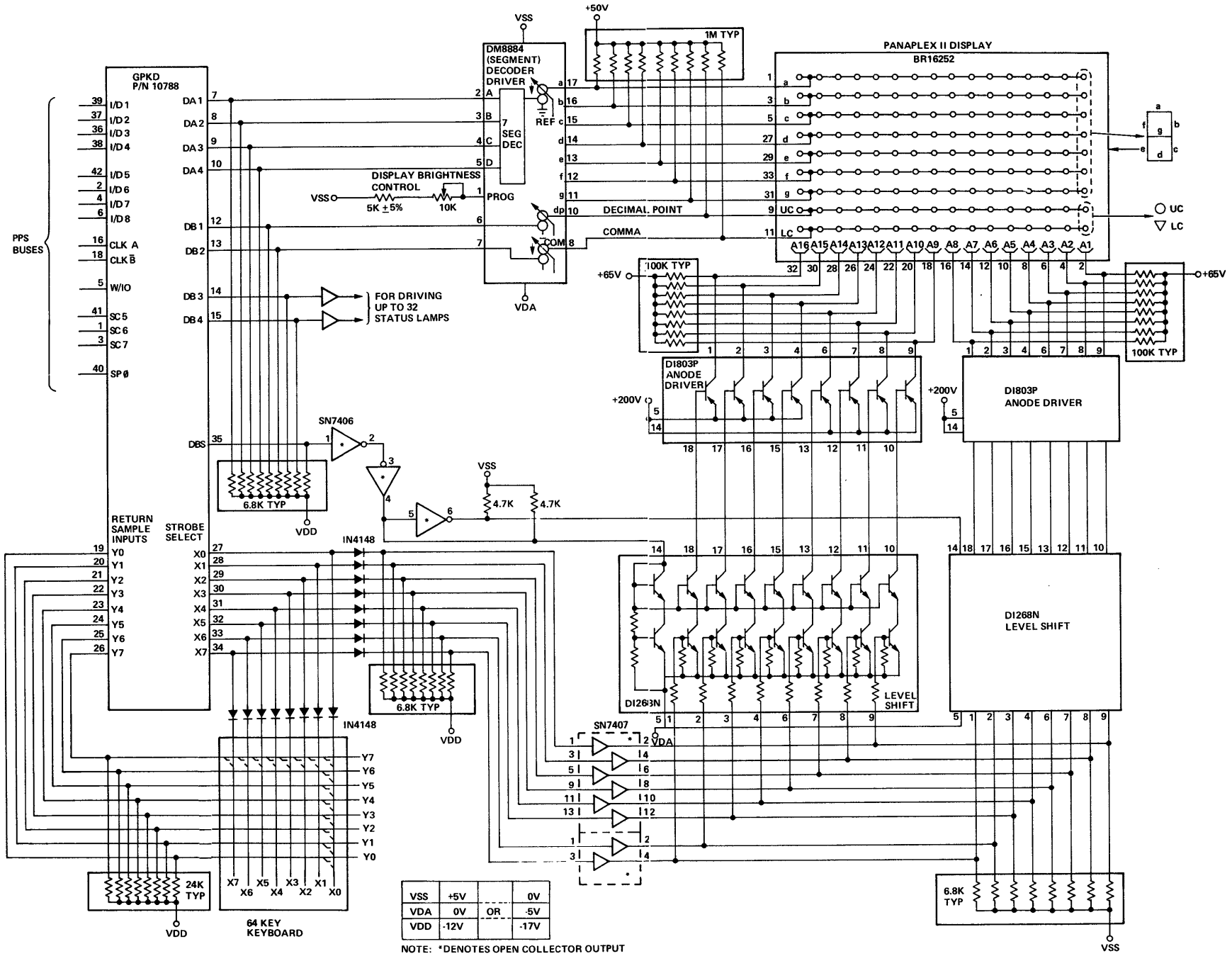
SPECIAL INTERFACE CONSIDERATION

DA, DB, X, and DBS Outputs

The GPKD output drivers are open drain buffers which when turned on will drive the GPKD output to VSS. When turned off the GPKD output will pull down toward VDD. A logic 1 on a data bus line will turn the corresponding driver off and a logic 0 will turn the driver on for a display data output. These circuits can be used for either TTL or MOS levels. Shown is the circuit termination for a TTL interface. The diode prevents a reverse breakdown of the TTL gate. This diode may be included in the input circuit of many TTL gates.



Circuit Termination for TTL Interface



VSS	+5V		0V
VDA	0V	OR	-5V
VDD	-12V		-17V

NOTE: *DENOTES OPEN COLLECTOR OUTPUT

Figure 10. GPKD Interface Diagram for Panaplex Display

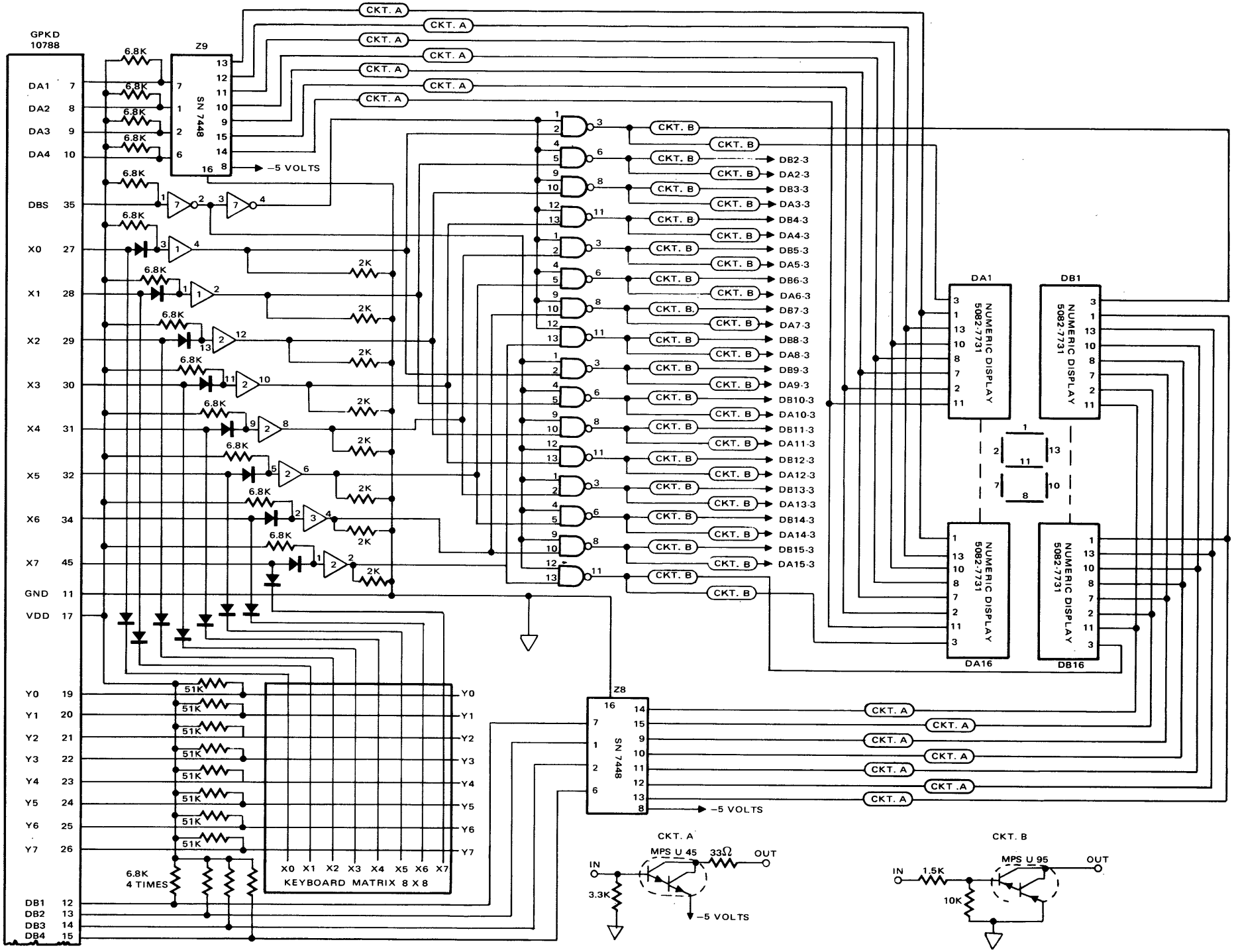


Figure 11. GPKD Interface Diagram for LED Display

ELECTRICAL SPECIFICATIONS

OPERATING LIMITATIONS AND CHARACTERISTICS

VDD = -17V ±5%
VSS = 0V
Logic "1" = Most negative voltage (V_{IL}, V_{OL})
Logic "0" = Most positive voltage (V_{IH}, V_{OH})

Operating Temperature, Case (T_A) 0° to 70°C
Storage Temperature -55° to 120°C
Frequency, Clock: (PPS-4 System Clock 199 kHz or 256 kHz)
Limit Values Determined at T_A of 25°C Unless Otherwise Noted

ABSOLUTE MAXIMUM RATINGS

Supply Voltage | VDD to VSS | 27 Volts Maximum
Input Voltage With Respect to VSS -27 Volts Maximum

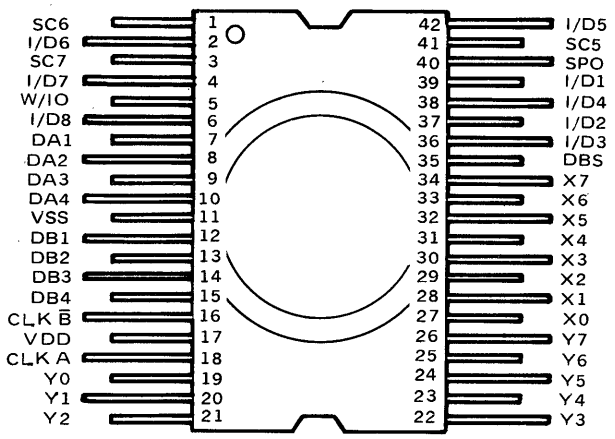
Function	Symbol	Parameter	Limits Min	Limits Typ	Limits Max.	Unit	Test Conditions
Power Requirement		Power Dissipation			200	mW	
Supply Current	I_{DD}	Avg Supply Current		4	6	mA	
Input and Output Characteristics							
1. System Bus Instruction/Data Bus (I/D1 - I/D4 and I/D5 - I/D8) and W/IO	V_{IH}	Input High Level	-1.5		0.3	V	
	V_{IL}	Input Low Level			▷1	V	
	V_{OH}	Output High Level	-1.0			V	
	V_{OL}	Output Low Level			▷2	V	
2. Interface and Strapping Return Sampling (Y0 - Y7)	V_{IH}	V_{IN} High Level	-4		0	V	VDD = 17.0V
	V_{IL}	V_{IN} Low Level	-17		-13		
Strobe Select X0 - X7 Display Interface, DBS, DB1 - DB4, DA1 - DA4	V_{OH}	V_{OUT} High Level	-2.7			V	I_L = 2.7 mA max
	V_{OL}	V_{OUT} Low Level	(Determined by external load)		-27	V	Floating
Straps SC5 - SC7	V_{IH}		-1.5		0.3	V	
	V_{IL}		-13		VDD	V	
Synchronize with Power on (SPO)	V_{OH}	V_{OUT} High Level	-1.0		0.3	V	
	V_{OL}	V_{OUT} Low Level	-7			V	
3. Clock	V_{IH}	Input High Level	-0.5		0.3		VDD = 17.0V
	V_{IL}	Input Low Level	-10.0		VDD		
4. Capacitance All Logic Inputs and Outputs	C_{IN}	Input Capacitance		5		pF	
	C_{IL}	Load Capacitance		100		pF	
5. Off Input Resistance and Leakage Current All Logic Inputs and Outputs	R_{OFF}	Off Resistance	1 Meg			Ohms	
	I_R	Input Leakage Current			10	μA	
6. Output Impedance (Interface Drivers "ON") DA's, DB's, and DBS	R_{ON}	On Resistance			1000	Ohms	
X0 - X7	R_{ON}	On Resistance			700	Ohms	

NOTE: Inputs and output voltage levels indicated by the ▷ symbols vary as a function of | VDD | in accordance with the following equations. (The equations are applicable over the entire operating temperature range.)

▷1 V_{IL} = -(0.66 |VDD| - 4.16)V (Example: If VDD = -16.15V, V_{IL} = -6.5V)

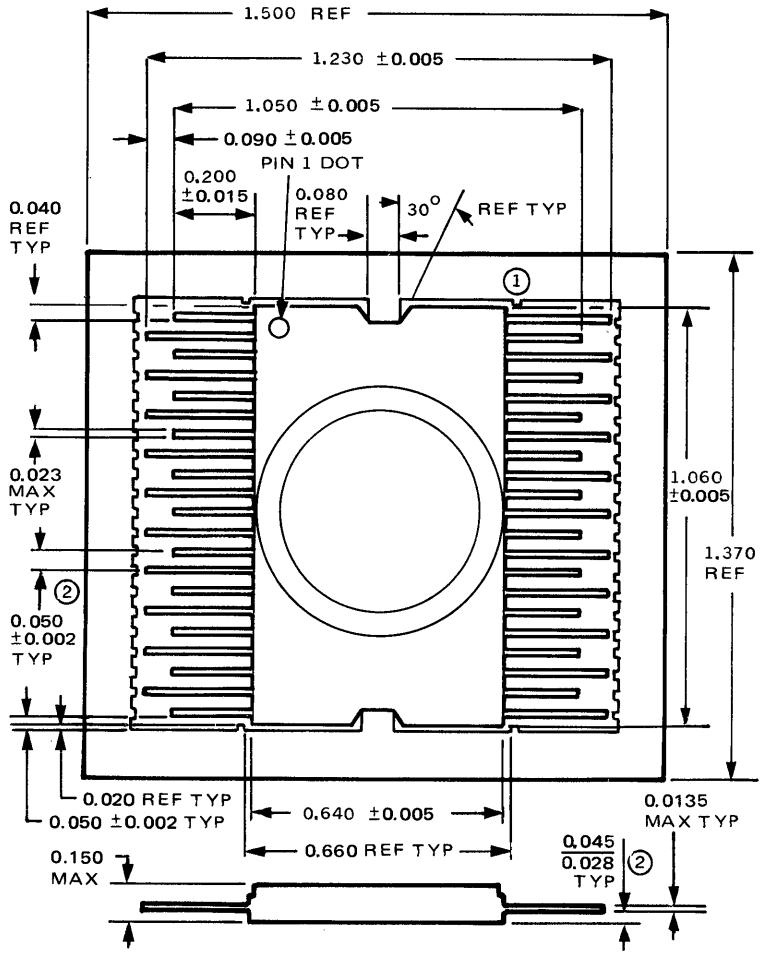
▷2 V_{OL} = -(0.66 |VDD| - 3.16)V (Example: If VDD = -16.15V, V_{OL} = -7.5V)

PIN ASSIGNMENTS



Input/Output Pin Configuration

STANDARD PLASTIC PACKAGE DIMENSIONS



1. BURRS UP TO 0.005" MAY OCCUR ON LEAD ENDS
2. TOOL HOLES IN LEAD FRAMES MAY BE FILLED WITH SOLDER
(1) 3. STUBS ON LEAD FRAME OPTIONAL (TYPICAL 4 PLACES)
(2) 4. DIMENSIONS ONLY APPLY WHERE LEADS LEAVE BODY

Standard 42-Lead Package Dimensions

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DATA SHEET

PRELIMINARY

PARALLEL PROCESSING SYSTEM (PPS-4)

PRINTER CONTROLLER CIRCUIT

Part No. 10789

RELATED PUBLICATIONS

1. MOS/LSI PPS Programmer's Reference Manual. Pub. No. 2520-D-26 Document No. 29001 N20.

2. PPS-4 Microprogram Development Using General Electric Information Services. Pub. No. 2520-D-44, Document No. 29004 N20.

3. PPS-4 Microprogram Development Using The TYMCOM-X System. Pub. No. 2520-D-43, Document No. 29002 N20.

4. PPS 4 Evaluation and Development Modules. Pub. No. 2519-D-20, Document No. 29004-41.

5. PPS-4 Data Sheet, Pub. No. 2519-D-13

NOTICE

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INTRODUCTION

This data sheet describes the Printer Controller circuit P/N 10789, manufactured by the Microelectronic Device Division of Rockwell International. This advanced microelectronic MOS device provides control between the Rockwell Parallel Processing System (PPS) and a number of commercially available printers such as Seiko Models EP101S, EP101, CR101T, Model 102, and Model 104. This Printer Controller circuit (PCC) provides a wide range of printer control functions, and two circuits may be used to control two separate printer mechanisms simultaneously as shown in Figure 1.

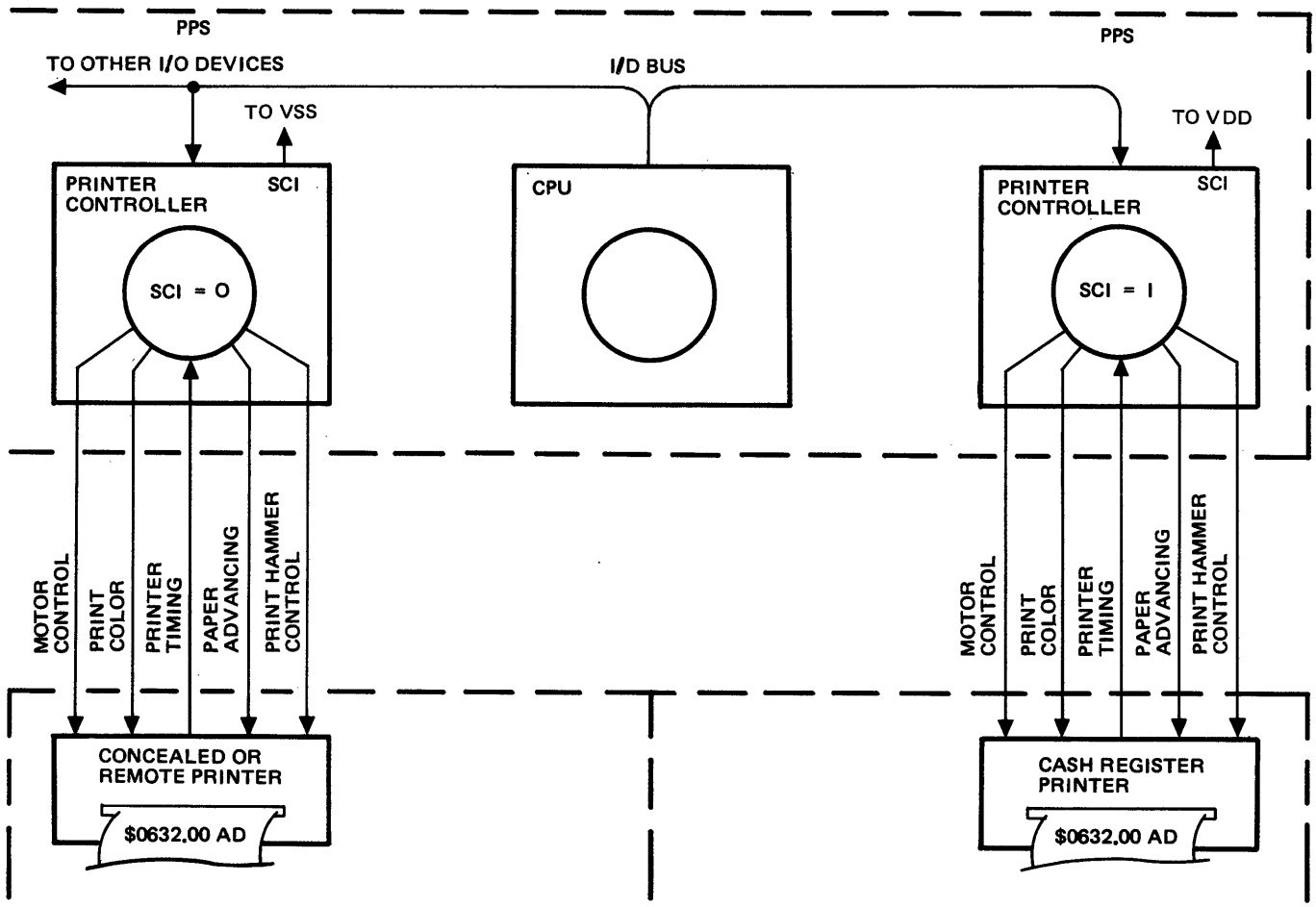


Figure 1. Typical Printer Controller Application Using Two Printer Controller Chips

FEATURES

- PPS Compatible
- Compatible With Seiko Printers
- One Discrete Input
- Automatic Initialization
- Chip Address Strap Encoded
- Two Printer Controller Circuits May Be Used For Two-Printer Operation
- Selective Motor On/Off Control
- Red/Black Print Color Select
- Automatic Multiple Paper Feeds
- Variable Number Of Print Columns
  Up To 21; Or
  Up To 13 Print Columns Plus
  Up To 8 Discrete Outputs
- Each Output Is Capable Of Driving One Standard TTL Device

PPS INTERFACE FEATURE

Interface between the Printer Controller circuit and the PPS is made directly without additional circuitry. Interface between the Printer Controller circuit and the Seiko printers requires additional circuits as shown in Figures 10 and 11. Two Printer Controller circuits may be used with one PPS by selecting the state of the SC1 strap.

PRINTER CONTROLLER OPERATIONAL FEATURES

Control of the printer by the Printer Controller circuit is accomplished independently of the PPS once the print data and Print command have been loaded. While the Printer Controller circuit is sequencing the printer through a print cycle, a busy signal is being generated by the busy inquiry control in the Printer Controller circuit. The PPS microprogram waits until the busy signal is no longer being generated before initiating the next print cycle.

Twenty-one columns of print characters on a print drum similar to that shown in Figure 2 may be controlled by the Printer Controller circuit. If less than this number is needed, up to eight of the unused print column drivers may be used as discrete outputs.

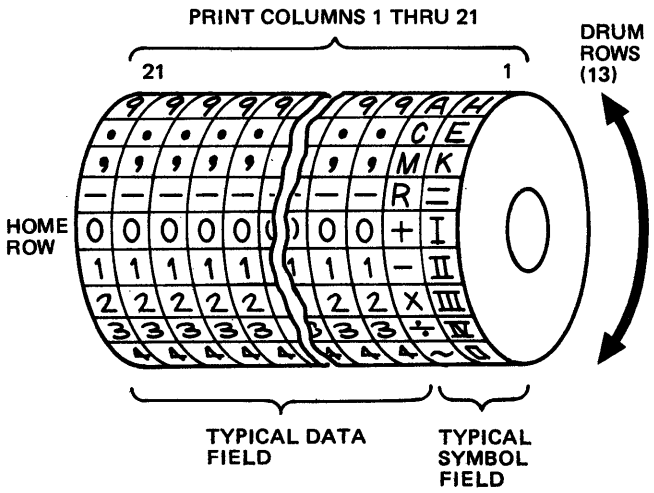


Figure 2. Typical 13 Row Print Drum

These eight discrete outputs are loaded by the PPS microprogram in a manner similar to that used to load discrete outputs on the General Purpose I/O circuit (P/N 10696).

The Printer Controller circuit contains a buffer memory that retains print data loaded by the PPS microprogram until the print cycle is completed. At print cycle completion, the buffer is automatically cleared to the all blank state as at power-on. When loading print data, the PPS microprogram need only load the significant characters, with the left-most (most significant) character loaded first and the right-most (least significant) character loaded last; leading blanks need not be loaded. The last character loaded prints in the right-most column.

The microprogrammed red print signal and paper advance signal are automatically generated by the Printer Controller circuit at the appropriate time. When the buffer memory has been loaded with all of the print data, the PPS microprogram causes a Print command to be issued to the Printer Controller circuit. The data transmitted with the Print command indicates the print color (red or black) and the quantity of paper feeds that must follow the print. One to eight paper feeds may be programmed. Paper feeds may also be ordered without any associated printing by issuing a Print command without loading any print data.

A special output is provided in the Printer Controller circuit to provide on-off control of the printer motor. If desired, the printer motor can be de-energized when the printer is not required by programming a Stop Motor command. The Stop Motor command causes the motor control output to switch to the floating state. When the printer motor must be energized, the Start Motor command is programmed. If the motor control output is already set to the active state, indicating that the printer motor has been commanded on, the command is ignored by the logic. If the motor control is in the non-active state, indicating that the printer motor was last commanded off, the motor control driver is switched to the active state. The active state can be sensed by switching circuitry which causes power to be transferred to the printer motor. The busy inquiry control in the Printer Controller circuit responds as busy to the PPS microprogram interrogation until the motor control has counted three revolutions of the print drum, indicating that the printer motor has reached operating speed. This feature prevents the PPS microprogram from initiating a print cycle before the printer motor is at sufficient speed for proper printer operation.

One TTL compatible discrete input is accepted by the Printer Controller circuit. This signal may be used as a printer fail input, or any other status input signal desired and will be passed on to the CPU when requested. When the PPS microprogram issues a Read Discrete Input command to the Printer Controller circuit, the discrete input is read and transferred into the most significant position of the CPU accumulator register for program control.

The following listing summarizes the operational feature of the Printer Controller circuit as executed in the normal sequence of events. A more detailed explanation of each of these functions is provided under Functional Description.

INTRODUCTION (CONT.)

OPERATIONAL FEATURES SUMMARY

INITIAL OPERATIONS	THEN
• Starts printer motor when system is energized or at predetermined time in programmed sequence	• Starts print cycle
• When queried, informs CPU when printer motor is up to speed and the chip is ready to accept new data	• Sets printer for red or black print color
• Stores data to be printed from CPU	• Prints up to 21 columns, or up to 13 columns plus up to eight discrete outputs
• Accepts print command and stores color of print and number of paper feeds	• Performs up to eight paper advances
	• Turns off printer motor, if instructed by CPU
	• When queried, informs CPU when printer motor is up to speed and the chip is ready for new data

FUNCTIONAL DESCRIPTION (CONT.)

GENERAL

The Printer Controller circuit block diagram (Figure 3) shows the various functional circuits in the Printer Controller circuit. A discussion of each of the following listed functional elements is provided in subsequent paragraphs.

Clock Decoder Driver
Chip Select Decode
Command Decode
Data Receivers
Print Control
Red Print Control
Paper Advance Control
Print Data Buffer
Drum Timing Generator
Drum Row Counter
Comparator
Motor Control
Busy Inquiry Control
Print Hammer Drivers
Discrete Outputs
Sweep Counter
Data Driver

CLOCK DECODER DRIVER

The clock decoder driver generates an internal four-phase clock system which is derived from the system clock signals, CLK A and CLK $\overline{B}$, received from the PPS. The four-phase clock system is utilized for synchronization of all operations performed by the Printer Controller circuit.

CHIP SELECT DECODE

The chip select decode compares the data on chip address data bus line I/D5 to the data on chip select strap SC1. If the result is the same and the logic levels on W/IO, I/D6, I/D7, and I/D8 are true, an output is sent to the command decode circuit which enables the command decode circuit to accept the PPS CPU commands.

COMMAND DECODE

Decoding of command inputs I/D4, I/D3, I/D2, and I/D1 is performed by the command decode circuit. This circuit, enabled by the chip select decode logic, determines which of the eight Printer Controller circuit commands listed in Table 1 is to be executed.

DATA RECEIVERS

Data is transmitted from the CPU accumulator register on data bus lines I/D5 through I/D8 to the data receivers. The four bits of information received are loaded as follows, according to the command received on I/D1 through I/D4 by the command decode:

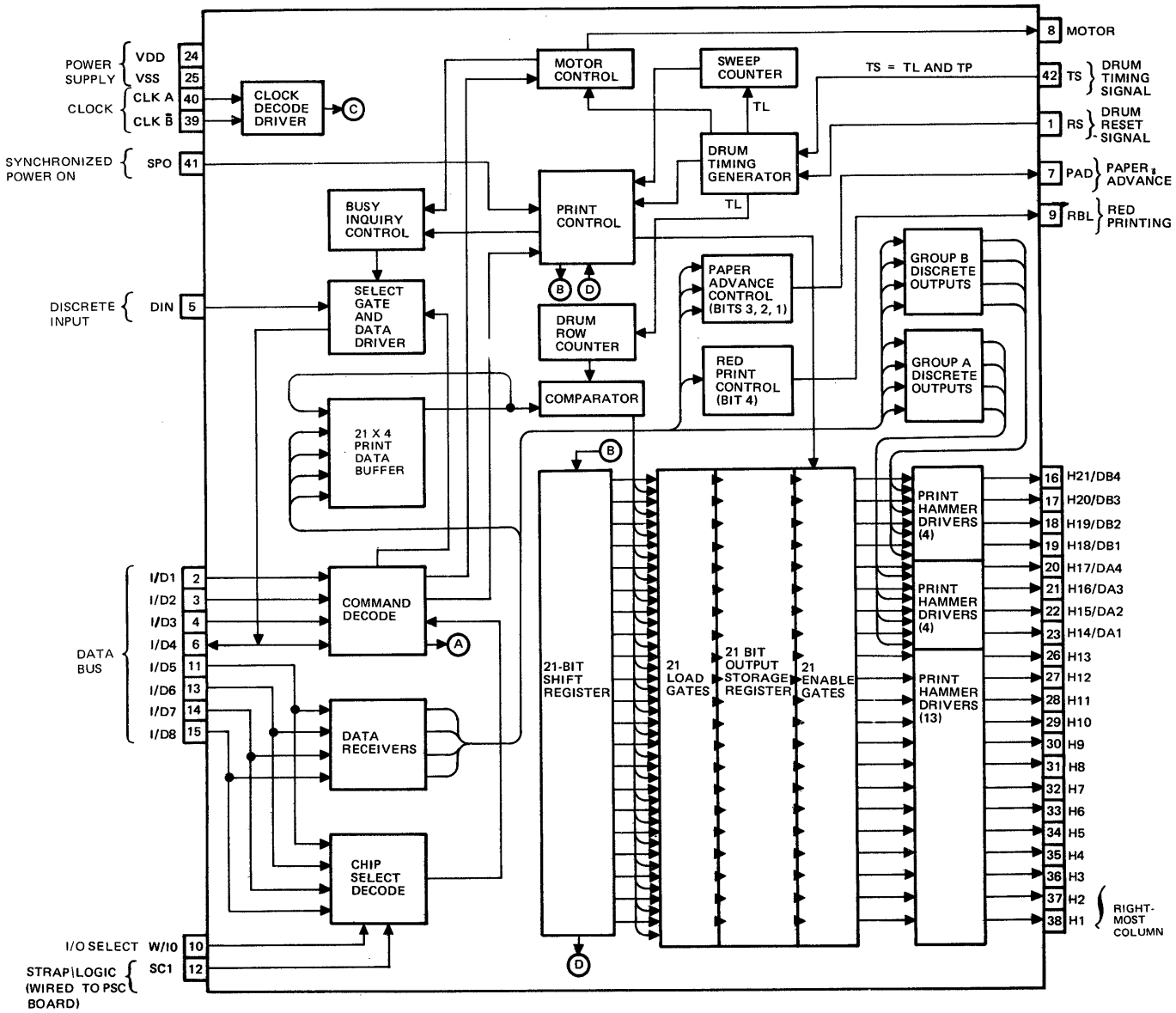
Load Print Data command causes data received to load into print data buffer.

Print command causes data received on line I/D8 to load into red print control and data received on lines I/D7, I/D6, and I/D5 to load into paper advance control.

Load Discrete Output Group A command causes data received to load into the Group A discrete output flip-flop register which drives output signals H14 through H17.

Load Discrete Output Group B command causes data received to load into the Group B discrete output flip-flop register which drives output signals H18 through H21.

FUNCTIONAL DESCRIPTION



NOTES:
- A = COMMAND LOGIC TO ALL APPLICABLE FUNCTIONS
- B = CONTROL LOGIC TO ALL APPLICABLE FUNCTIONS
- C = FOUR PHASE INTERNAL CLOCK TO APPLICABLE FUNCTIONS
- D = PRINT CONTROL RETURN FROM 21 BIT SERIAL REGISTER

Figure 3. Printer Controller Circuit Block Diagram

PRINT CONTROL

Proper timing of all Printer Controller circuit signals is controlled by the print control. The print control receives the drum timing generator outputs, sweep counter output, synchronized power on signal, and command decode output. These inputs and the command logic input cause the print control to generate (1) the signal necessary for the operation of the busy inquiry control, and (2) the control logic for the execution of each of the Printer Controller circuit operations.

RED PRINT CONTROL

When a red print is required, the red print control is loaded with data bit four from the data receiver when the PPS issues the Print command. The red print control generates the ribbon lift (RBL) signal, causing the printer to shift to red when the appropriate control logic is received from the print control.

PAPER ADVANCE CONTROL

The paper advance control is loaded with data from data receiver bits 3, 2, and 1 when the print command is issued. At the end of the print cycle, the paper advance control generates a signal which actuates the printer for the appropriate number of paper feeds.

PRINT DATA BUFFER

The print data buffer is a shift and hold register capable of holding 21 characters of four bits each. When a Load Print Data command is received, the print data buffer shifts one character position and accepts the data received into the vacated character position. This shift and load cycle is repeated until all characters to be printed have been entered. There is no inversion between the accumulator and the print data buffer, i.e., a hex number in the accumulator goes to the same hex number in the print data buffer. During printout, each character is sequenced to the comparator and also recirculated to the print data buffer input so that, at the end of each character comparison cycle, the data has been restored to the print data buffer. This cycle is repeated for each drum row. (Each drum row prints one character value.)

DRUM TIMING GENERATION

The printer generates a timing signal pulse (TS) and a reset signal pulse (RS), which are utilized by the drum timing generator to determine the immediate position of the print drum. The TS and RS pulses provide the information necessary to (1) determine the angular position of the print drum, (2) generate the timing of the print hammer signals H1 through H21, and (3) provide the print control circuits with the timing necessary to control the red print, motor, and paper advance signal. The TS signal consists of a pair of pulses of which TL is the first pulse and TP is the second pulse (Figure 5). Print hammer activation occurs from the TP pulse to the following TL pulse. The TL pulse marks off each row on the drum as the row passes. The RS pulse is generated once for each revolution of the drum, indicating that row 0 is passing in front of the print hammers.

DRUM ROW COUNTER

The drum row counter indicates to the comparator the row location of the drum at any instant. The RS pulse initializes the drum row counter to zero (row 0) at each drum revolution. Each row is then identified to the comparator as the drum row counter counts TL pulses. If the row counter has reached a value denoting row 15 when the RS pulse occurs, the Printer Controller logic determines that the printer is a Model 101 and causes the circuits to function accordingly.

COMPARATOR AND ASSOCIATED CIRCUITRY

The comparator determines the numeric value of each of the 21 character positions in the print data buffer and provides an output to the printer output circuits. During each drum row time, all 21 characters in the print data buffer are fed character-serial, 4-bit parallel through the comparator in synchronization with a single control bit passing through the 21-bit shift register. The comparator sequentially checks each of the 21 characters to determine if the character matches the current drum row value. When coincidence occurs, the comparator generates an output signal which is transmitted to one input of each of the 21 output storage register load gates. Coincidence between the output from the comparator appearing at a gate and the control bit moving through the 21-bit shift register enables that gate which in turn sets a flip-flop in the 21-bit output storage register. (see following example.) Within one drum row time after all 21 characters have passed through the comparator and the 21-bit output storage register is loaded, the transfer gates corresponding to the set flip-flops in the 21-bit output storage register are enabled by the print control. The output of the enabled transfer gates causes the corresponding print hammer drivers to assume the active state. This cycle is repeated for each of the rows on the printer drum (either 13 or 16 rows) until all the characters have passed through the Printer Controller circuit.

Example: (See Figures 2 and 5)

While the drum row counter is at a position corresponding with character 6, all 21 characters in the print data buffer are sequentially checked in the comparator to locate any sixes. If the third character is a six, the comparator provides an output to all 21 gates at column time 3. However, only the third gate accepts this output because it is the only gate enabled by the control-bit then

FUNCTIONAL DESCRIPTION (CONT.)

W/IO	CHIP SELECT I/D 8	7	6	5	COMMAND I/D 4	3	2	1	ASSEMBLER EQX* VALUE SC1=0	SC1=1	NAME	COMMENT
1	1	1	1	X	0	1	1	0	E6	F6	Load Print Data	A(4:1)→Print Data Buffer
1	1	1	1	X	0	1	0	1	E5	F5	Load Discrete Output Group A	A(4:1)→H17, H16, H15, H14
1	1	1	1	X	0	0	1	1	E3	F3	Load Discrete Output Group B	A(4:1)→H21, H20, H19, H18
1	1	1	1	X	1	1	0	0	EC	FC	Start Motor	If motor on, ignored; if motor off, motor is turned on and circuit indicates busy until drum is up to speed (three revolutions of drum).
1	1	1	1	X	1	0	1	0	EA	FA	Stop Motor	Motor is turned off
1	1	1	1	X	1	0	0	1	E9	F9	Print**	A4→red print control, A(3:1)→paper advance control, print cycle begins
1	1	1	1	X	1	1	1	0	EE	FE	Busy Inquiry***	If busy, 0→A4; if not busy, 1→A4
1	1	1	1	X	1	1	0	1	ED	FD	Read DIN***	$\overline{DIN}$→A4(If DIN is negative, 0→A4; if DIN is at VSS, 1→A4.)

1. Polarity of I/D5 must be the same as chip select strap SC1.
2. W/IO is generated by first word of PPS IOL instruction.
3. All IOL instructions cause the previous data in the CPU accumulator to be lost.

* EQX = Equivalent statement as defined in Operating Manual for PPS-4 Microprogram Development Using the Tymshare TYMCOM-X System, Pub. No. 2520-D-43, or the General Electric Information Services Manual, Pub. No. 29004 N20 as applicable.

** PRINT command data:

Color	Accumulator 4 3 2 1	Paper Advance Spaces
Black	0 0 0 0	8
Red	1 0 0 1	1
	0 1 0	2
	0 1 1	3
	.	.
	.	.
	.	.
	1 1 1	7

*** A3, A2, and A1 will be indeterminate at this time.

in the third position of the 21-bit shift register. The resulting output of the third gate sets the third flip-flop in the 21-bit output storage register. Later in the cycle, if the fifteenth character is a six, the comparator again provides an output to all the gates. However, the control-bit in the 21-bit shift register has now advanced to the fifteenth position and the coincidence of these signals enables the fifteenth gate, setting the fifteenth flip-flop in the 21-bit output storage register. After all 21 positions have been compared for the character 6, the cycle is complete and every print column position that should print a 6 (3 and 15 in this example) is ready to do so. This character search and print cycle is completed before the drum row counter advances to the next value (7 in this example). The comparison cycle is then repeated for the new value.

The comparison is started immediately following receipt of a Print command. The logic does not wait for the RS signal to be received.

MOTOR CONTROL

The motor control contains a flip-flop which is set by a Start Motor command or by power-on and is reset by a Stop Motor command. In addition, the motor control contains a counter which counts drum revolutions. When the motor control flip-flop has been set to the motor-on state from the motor-off state (or at power-on), the motor control instructs the busy inquiry control to respond as busy until three drum revolutions have passed. If the motor control is in the motor-on state, a Start Motor command will not cause the Printer Controller circuit to enter this busy mode.

BUSY INQUIRY CONTROL

The busy inquiry control provides a signal to the PPS microprogram to indicate if the printer is in a print cycle or if the print cycle is complete so that a new print cycle can be initiated. This allows the PPS microprogram to detect "motor-up-to speed" at power-on and motor turn-on, and to detect that the printing cycle is in process. The busy signal is transmitted from the busy inquiry control through the data driver to CPU accumulator bit 4 upon receipt of a Busy Inquiry command.

PRINT HAMMER DRIVERS

Enabling of the print hammer drivers is accomplished by the comparator between the occurrence of a TP pulse and the next TL pulse. The print hammer drivers are the open-drain type which drive to the VSS logic level or float. Print hammer drivers 14 through 21 can be used for discrete outputs only if they are not required for print columns. If these drivers are used for print columns, the discrete outputs do not interfere with the print hammer signals because the discrete outputs are cleared to the float state at power-on and remain in this state unless a Load Discrete Output command is issued. Output H1 is normally used for the right-most print column.

DISCRETE OUTPUTS

Any number of the eight available discrete outputs of discrete output groups A or B may be utilized for discrete outputs, with the remainder being used for print hammers. Because of the open-drain type print hammer drivers, a logic 1 in a discrete output register does not interfere with the print hammer signal. As an example, if two discrete outputs and 19 columns of print are required, two discrete output values can be loaded into bits 4 and 3 of the accumulator and a logic 1 loaded into bits 2 and 1. When the Load Discrete Output Group B command is issued, the two discrete output values appear on H21 and H20 and there is no interference with the print hammer information on H19 and H18.

Two discrete output commands are available for loading the discrete output groups A and B. The discrete outputs are loaded non-inverted from the CPU accumulator so that a logic 1 in the accumulator results in a logic 1 (float) at the print hammer drive output. The Load Discrete Output Group A command loads the accumulator bits 1 through 4 into discrete outputs which drive output signals H14 and H17. The Load Discrete Output Group B command loads the accumulator bits 1 through 4 into the discrete outputs which drive output signals H18 through H21.

SWEEP COUNTER

Termination of the print cycle is controlled by the sweep counter, which counts TL pulses until the number accumulated indicates a completed print cycle. The sweep counter then signals the print control to terminate the print cycle.

DATA DRIVER

The data driver transmits either the value of the discrete input or the busy status from the Printer Controller circuit to the most significant position of the PPS CPU accumulator register. The information transmitted depends, respectively, whether the Read Discrete Input (Read DIN) command or the Busy Inquiry command is decoded. There is an inversion between the discrete input and the accumulator. Therefore, a positive voltage (VSS) input at DIN is transferred to the data bus as a "0" and then into the accumulator as a "1". The foregoing discussion assumes MOS engative logic convention.

OPERATION

GENERAL

The operation of the Printer Controller circuit is divided into two functions for purposes of explanation: (1) Printer Controller circuit interface to the PPS CPU circuit and (2) PPS microprogramming techniques relative to the print cycle. A sample program of a typical printout subroutine is shown at the end of this section. Table 1 in the front of this document, lists the PPS IOL commands used with the Printer Controller circuit.

PRINTER CONTROLLER CIRCUIT INTERFACE TO THE PPS CPU

Physical interconnection of the Printer Controller circuit to the CPU is accomplished by connecting Printer Controller lines to the PPS CPU circuit pins of the same designation. The interface is shown in Figure 4. The CPU lines connecting to the Printer Controller circuit are the Instruction Data Command Bus (I/D1 through I/D8), Synchronized Power-on (SPO), and Write Command I/O enable (W/IO).

Two addresses are available for the Printer Controller circuit, which allows two Printer Controller circuits to be utilized with one PPS. In both instances, SC1 is strapped to either VDD or VSS to provide unique addressing. To address a Printer Controller circuit, line I/D5 must be at the same logic state as SC1, and I/D6, I/D7, and I/D8 must be at VDD (logic 1).

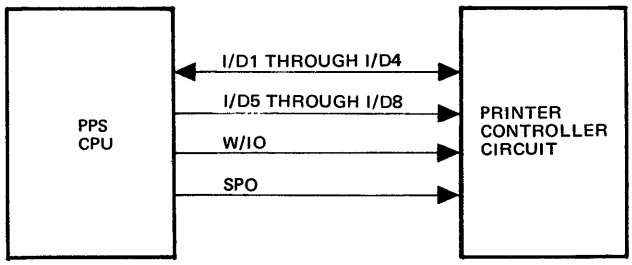


Figure 4. CPU to Printer Controller Circuit Interface

Functionally, the PPS system requires a two-word IOL instruction when control of one of the system's I/O circuits is required. The first IOL word automatically initiates generation of a chip select enable signal (W/IO) by the CPU. The most significant half of the second word (on data bus lines I/D5 through I/D8) designates the address of an I/O chip. This address, with W/IO signal true, selects one I/O chip at a time. The least significant half of the second word (on data bus lines I/D1 through I/D4) contains a command for the addressed I/O chip. Some commands require transfer of data or status between the CPU and the I/O chip. Data can be transferred from the CPU to the I/O chip over lines I/D5 through I/D8. Data or status can be transferred from the I/O chip to the CPU over lines I/D1 through I/D4. Data transfer takes place during the next half cycle following receipt by the I/O chip of the command from ROM.

PRINT CYCLE/PPS MICROPROGRAMMING TECHNIQUES

A brief, general discussion of several aspects of printer operations as related to PPS microprogramming techniques is presented in the following paragraphs. (See Figure 5 for timing relationships.) More detailed information will be provided in future changes to this publication.

Print Cycle Phases

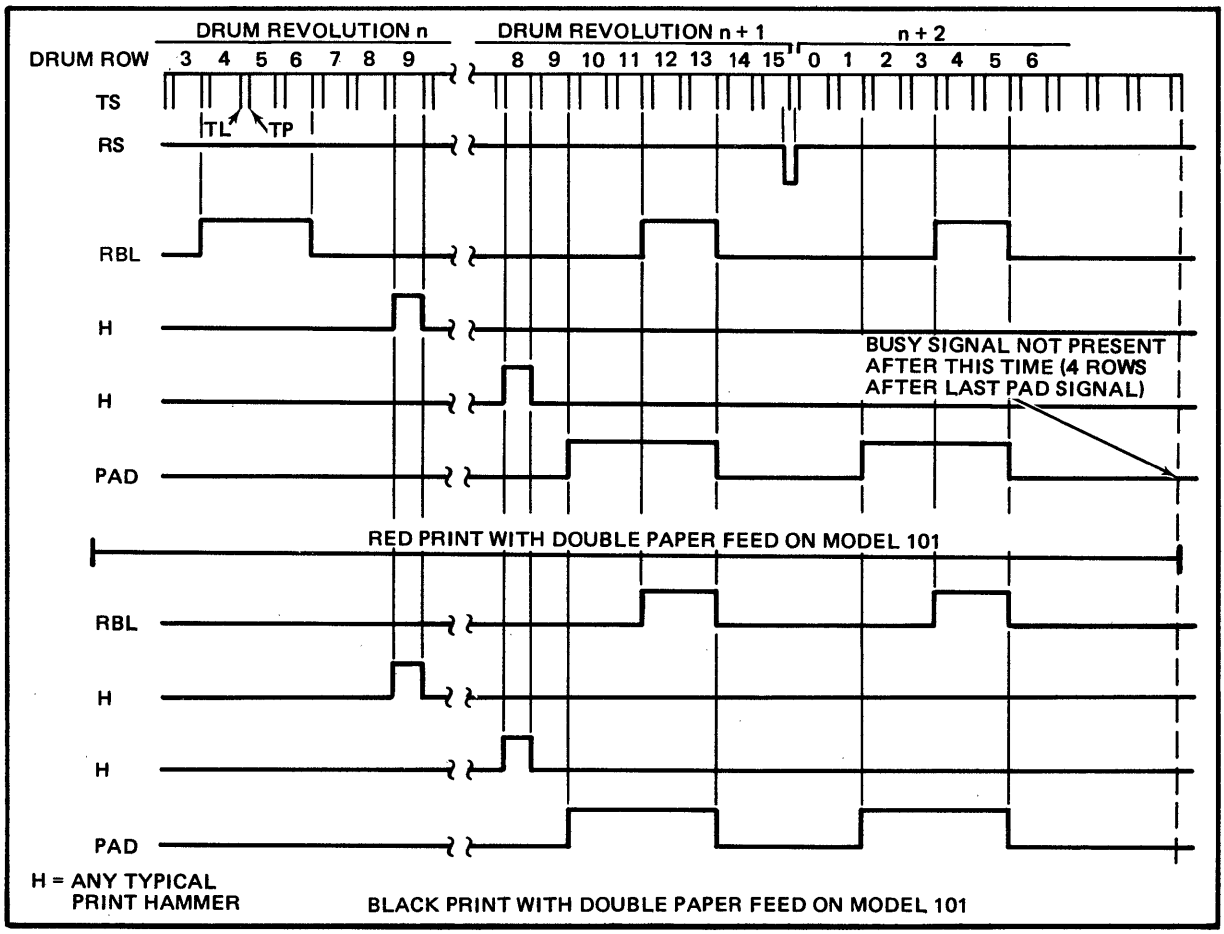
An individual print cycle consists of three phases: (1) the red print phase, (2) the print phase, and (3) the paper advance phase. The red print phase begins when a Print command is received and ends with a TL pulse corresponding to the first row for which hammers may be activated. The print phase begins with the previously mentioned TL pulse and ends after 13 drum rows for the Model 102 and 104 Seiko printers or 16 drum rows for the Model 101 series Seiko printers. The paper advance phase begins at the end of the print phase and ends when all paper feeds have been accomplished.

Drum Row Characters

As shown in Figure 2 a typical printer drum will have the 0 character in all print columns of the home row in the data field. The characters corresponding to consecutive integers 1 through 9 are provided on the next nine drum rows for print columns in this field. The remaining rows may contain various other symbols, such as decimal point or comma. For example, row 10 could contain the symbol, row 11 the , symbol, and row 12 the - symbol.

To cause printing of any particular character, the PPS microprogram loads the CPU accumulator register with a value equal to the row number corresponding to that character. Then the PPS microprogram executes a Load Print Data command. For example, on some drums the data field characters 3. - would be printed by the PPS microprogram executing Load Print Data commands with decimal values of 3, 10, and 12, respectively, (3 = 3, 10 =., and 12 = -)

The drum on the Models 102 and 104 SEIKO Printers contains only 13 rows. Therefore, a decimal value of 13, 14, or 15 in the CPU accumulator corresponds to blank columns on the printed page. The Model 101 series Seiko printers have 16 rows on the drum, except Model AN101F which has 42 rows. Therefore, decimal values 13 and 14 may not be used for blanks with Model 101 series printers.



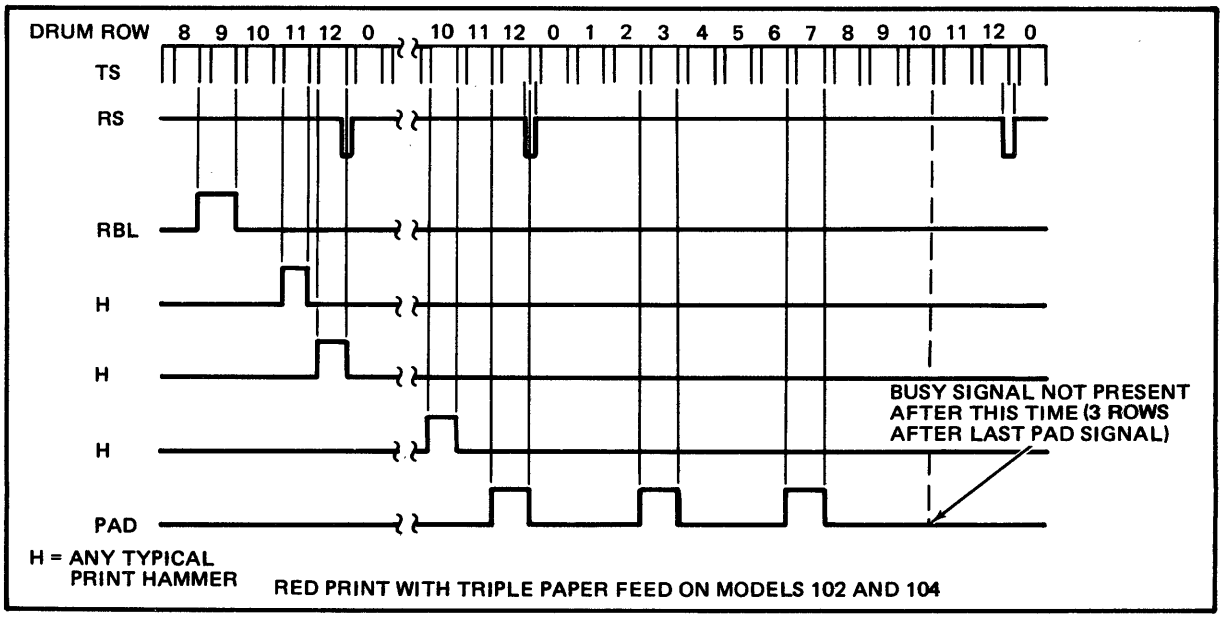


Figure 5. Print Color and Paper Feed Timing for Seiko Printers

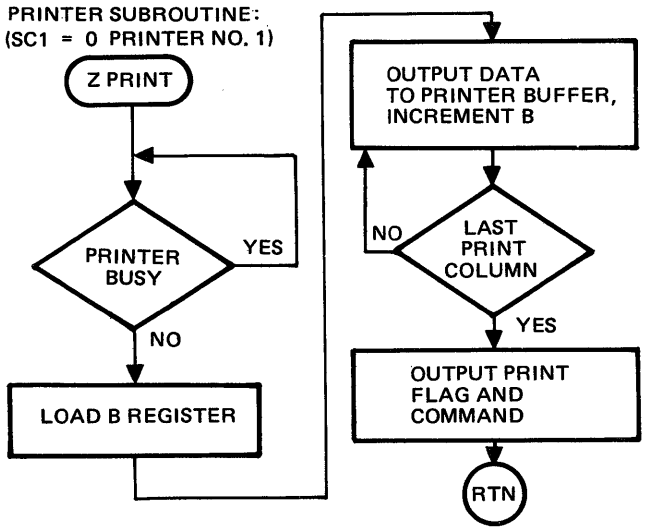
The Printer Controller contains special logic which prohibits print hammer activation on row 15. Therefore a decimal value of 15 in the CPU accumulator corresponds to a blank column on any printer, and no printable characters can occupy row 15 of the drum.

A reset (RS) pulse generated by the printer signifies that row 0 is passing in front of the print hammers.

SAMPLE PRINTOUT SUBROUTINE

The sample subroutine shown in Figure 6 is a typical printout operation which provides for printing eight columns of data from RAM 0, register 1, beginning with word 3 through word 10. This subroutine assumes that print driver H1 is connected to the right-most print column, and that H8 is connected to the left-most print column. Upon entry into the subroutine, printer status is checked by reading operand PBUSY. Operand PBUSY indicates printer busy. If the printer is not busy the CPU B register is loaded with the beginning address of the print data. Data is loaded into the CPU accumulator then output to the printer by operand PLPD. The CPU B register (BL) is incremented and a check for word 11 is made. If word 11 has not been reached, a transfer to LOADPB (next word) is executed and the output continues. If word 11 is reached, a skip is executed and the address of the print command data word is loaded into the B register. (The print command data could be in word 11 eliminating the need for loading the B register.) The print flag word is output at IOL PRNT and a RTN is executed. The printer will at this time go busy and print the previously output data.

This sample subroutine is based on the assumption that all formatting of print data has been done previous to the subroutine call. It is possible to achieve a net decrease in required ROM words by combining certain formatting functions such as leading zero suppression and insertion of commas and decimal points within the program loop which does the actual outputting of print data.




```
                TM      PRINT
                :       :
Z PRINT         IOL     P BUSY      PRINTER BUSY?
                ADI     8
                T       Z PRINT     YES, WAIT
                LBL     PRBUF       LOAD B WITH PRINTER
                                    BUFFER ADDRESS
LOAD PB         LD
                IOL     PLPD        LOAD PRINTER BUFFER
                INCB
                SKBI    11          PRINT COMPLETE ?
                T       LOAD PB     NO, GO BACK
                LBL     PRFLG       LOAD B WITH PRINT
                                    FLAG ADDRESS
                LD                  GET PRINT COMMAND DATA
                IOL     PRNT        PRINT LINE
                RTN

AUXILIARY INFORMATION
PRINT   PTR  ZPRINT     SUBROUTINE ENTRY POINTER
PBUSY   EQX  EE    }
PLPD    EQX  E6    }    SEE TABLE 1
PRNT    EQX  E9    }
PRBUF   EQX  13         RAMO, REGISTER 1, WORD 3
PRFLG   EQX  12         RAMO, REGISTER 1, WORD 2
```

Figure 6. Typical Printout Subroutine Flow Chart

ELECTRICAL SPECIFICATIONS

OPERATING LIMITATIONS AND CHARACTERISTICS

VDD = -17V ±5%
VSS = OV
Logic "1" = Most negative voltage (V_{IL}, V_{OL})
Logic "0" = Most positive voltage (V_{IH}, V_{OH})

Operating Temperature, Case (T_A) 0° to 70°C
Storage Temperature -55° to 120°C
Frequency, Clock: (PPS-4 System Clock 199 kHz or 256 kHz)
Limit values determined at T_A of 25°C unless otherwise noted

ABSOLUTE MAXIMUM RATINGS

Supply Voltage |VDD to VSS| 27 Volts Maximum
Input Voltage With Respect to VSS -27 Volts Maximum

INPUT/OUTPUT CHARACTERISTICS

Refer to Electrical Specifications in PPS-4 Basic Devices Data Sheet Doc. No. 29003-N11 for additional information on signals.

Function	Symbol	Parameter	Limits Min	Limits Typ	Limits Max.	Unit	Test Conditions
Power Requirement		Power Dissipation			200	mW	
Supply Current	I_{DD}	Avg Supply Current				mA	
Input and Output Characteristics							
1. System Bus Instruction/Data Bus (I/D1 - I/D4 and I/D5 - I/D8) and W/IO	V_{IH}	Input High Level	-1.5		0.3	V	
	V_{IL}	Input Low Level			▷1	V	
	V_{OH}	Output High Level	-1.0			V	
	V_{OL}	Output Low Level			▷2	V	
2. Interface and Strapping Printer Inputs TS, RS	V_{IH}	V_{IN} High Level	-4		0	V	VDD = 17.0V
	V_{IL}	V_{IN} Low Level	-17		-13		
DIN	V_{IH}	V_{IN} High Level	-1.5			V	
	V_{IL}	V_{IN} Low Level			-4.2	V	
Print Hammer Drivers H1–H21	V_{OH}	V_{OUT} High Level	-2.7			V	I_L = 2.7 mA max
	V_{OL}	V_{OUT} Low Level	(Determined by external load)		-27	V	Floating
Strap SC1	V_{IH}		-1.5		0.3	V	
	V_{IL}		-13		VDD	V	
Synchronized Power on (SPO)	V_{OH}	V_{OUT} High Level	-1.0		0.3	V	
	V_{OL}	V_{OUT} Low Level	-7			V	
3. Clock CLK A, CLK $\overline{B}$	V_{IH}	Input High Level	-0.5		0.3		VDD = 17.0V
	V_{IL}	Input Low Level	-10.0		VDD		
4. Capacitance All Logic Inputs and Outputs	C_{IN}	Input Capacitance			5	pF	
	C_{IL}	Load Capacitance		100		pF	
5. Off Input Resistance and Leakage Current All Logic Inputs and Outputs	R_{OFF}	Off Resistance	1 Meg			Ohms	
	I_R	Input Leakage Current			10	μA	
6. Output Impedance Print Hammer Drivers "ON" H1–H21	R_{ON}	On Resistance			1000	Ohms	

NOTE: Inputs and output voltage levels indicated by the ▷ symbols vary as a function of |VDD| in accordance with the following equations. (The equations are applicable over the entire operating temperature range.)

▷1 V_{IL} = -(0.66 |VDD| - 4.16)V (Example: If VDD = -16.15V, V_{IL} = -6.5V)

▷2 V_{OL} = -(0.66 |VDD| - 3.16)V (Example: If VDD = -16.15V, V_{OL} = -7.5V)

PIN ASSIGNMENTS

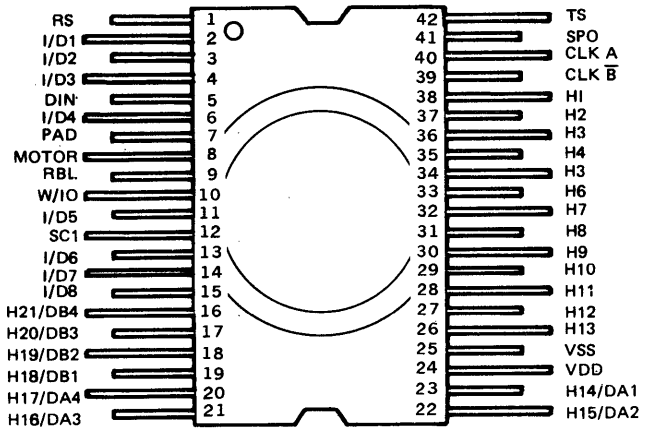


Figure 7. Input/Output Pin Configuration

STANDARD PLASTIC PACKAGES DIMENSIONS

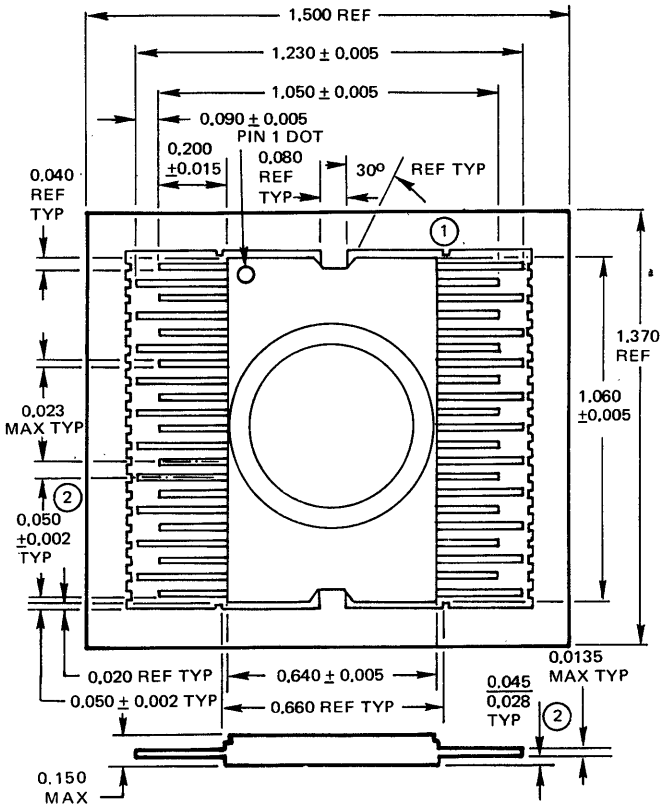


Figure 8. Standard 42-Lead Package Dimensions

SPECIAL INTERFACE CONSIDERATION

Printer Controller Outputs (Except I/D4)

The output drivers are open drain buffers which when turned on will drive the output to VSS. When turned off the output will pull down toward VDD. A logic 1 at the data output will turn the corresponding driver off and a logic 0 will turn the driver on to VSS.

These circuits can be used for either TTL or MOS levels. Shown is the circuit termination for a TTL interface. The diode prevents a reverse breakdown of the TTL gate. This diode may be included in the input circuit of many TTL gates. In this system VSS and VDD have been shifted from 0V and -17V to +5V and -12V

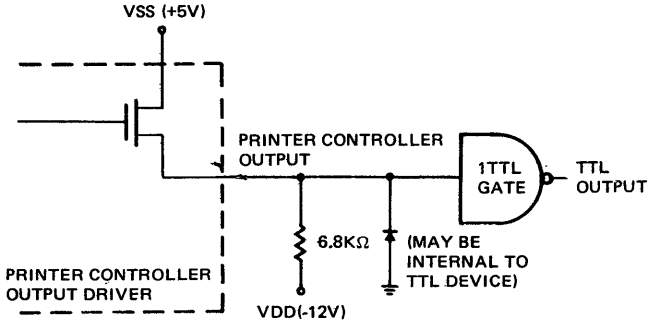


Figure 9. Circuit Termination for TTL Interface

Figures 10 and 11 show typical interface connections between the Printer Controller and the printers.

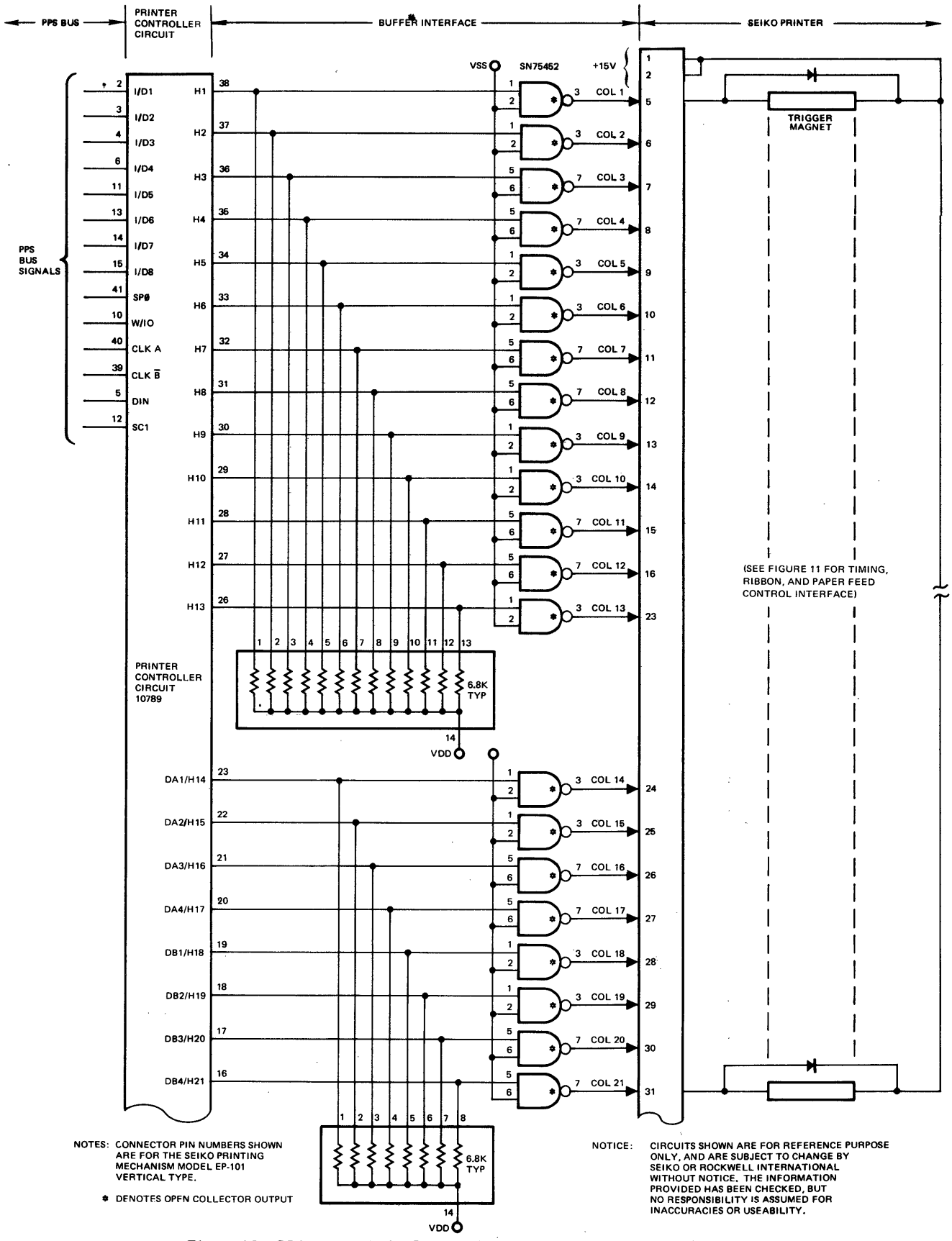


Figure 10. PPS Bus to Sieko Printer Hammer Drivers Interface Schematic

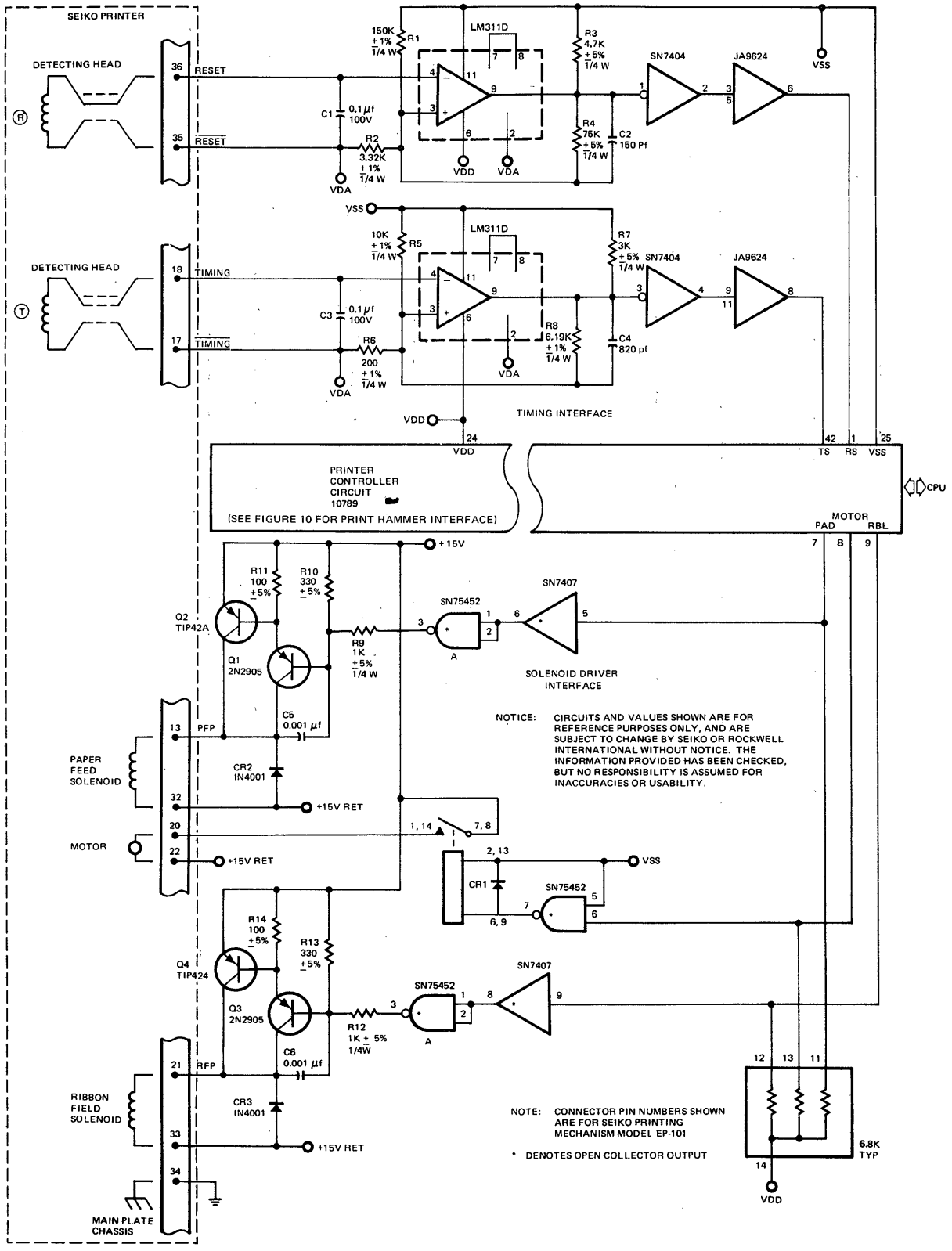


Figure 11. Printer Controller to Sieko Printer Timing and Control Circuit Interface Schematic

Rockwell

KEYBOARD/PRINTER CONTROLLER CIRCUIT

Preliminary Data Sheet
Document No. 10815 N10

Part No. 10815

INTRODUCTION

This data sheet describes the Keyboard/Printer Controller circuit, P/N 10815, manufactured by the Microelectronic Device Division of Rockwell International. This versatile and advanced microelectronic MOS device provides interfacing between the Rockwell Parallel Processing System (PPS) and both a Seiko Model 320 printer and a 16 x 4 keyboard.

The Keyboard/Printer Controller circuit (KPC) provides a broad range of control functions. The keyboard portion of the KPC scans the keyboard matrix, determines the validity of a key depression, stores the keys in a first-in first-out stack, and transmits the keyboard data to the PPS system on request. In addition the printer controller portion accepts formatted data to be printed, and then drives the printer without further direction from the PPS system.

FEATURES: Printer Controller

- PPS Compatible
- Controls SEIKO Model 320 Printer
- Automatic Initialization
- Red/Black Color Select
- 22 Column Control
- Double Line Feeds
- Direct Memory Transfer

FEATURES: Keyboard Interface

- Ten-Key Stack
- Accepts up to 64 Keys on a 16 x 4 Keyboard Matrix
- Key Debounce Delay of 8 msec
- Function Access
- Initialized at Power On (SPO)
- Two-Key Rollover

DESCRIPTION

This versatile and advanced LSI/MOS device provides control and interfacing between the Rockwell Parallel Processing System (PPS) microcomputer, the Seiko Model 320 printer, and any keyboard with up to 64 keys in a 16 x 4 matrix.

The Keyboard/Printer Controller circuit (KPC) provides a broad range of control functions. The keyboard portion of the KPC scans the keyboard matrix, determines the validity of a key depression, stores the keys in a first-in first-out stack, and transmits the keyboard data to the PPS on request. In addition the printer controller portion accepts formatted data to be printed, and then drives the printer without further direction from the PPS.

KEYBOARD CONTROL DESCRIPTION

Up to 64 single pole, single throw, momentary switches arranged in a 16 x 4 matrix are strobed by the keyboard control section of the KPC circuit. The replies are stored without the necessity of PPS CPU supervision in a 10-level stack until the CPU calls for them.

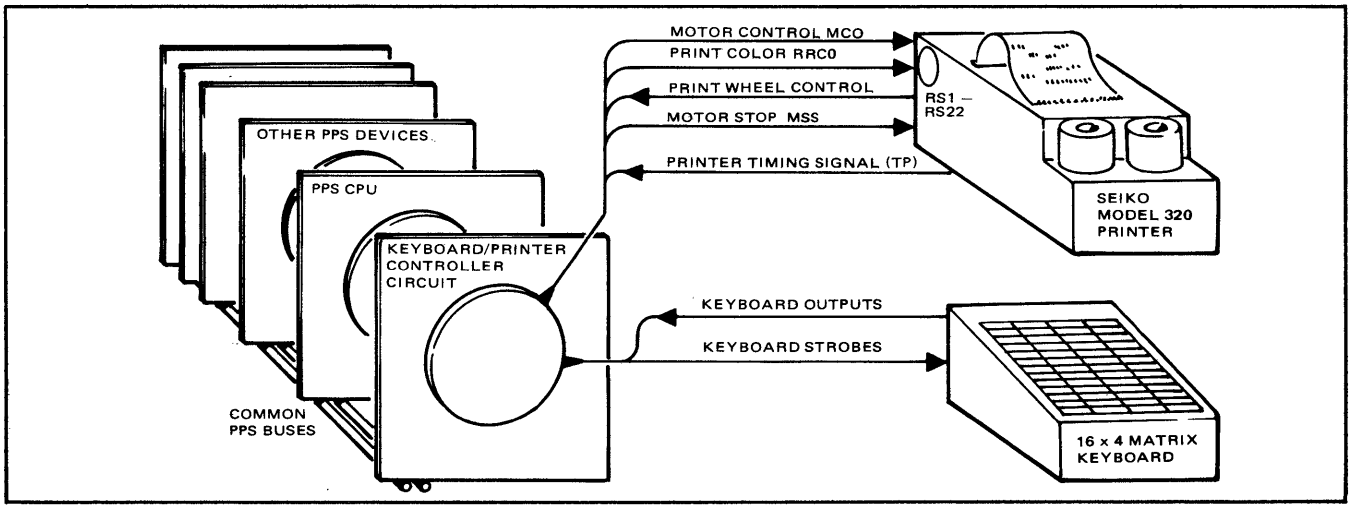


Figure 1. TYPICAL KEYBOARD/PRINTER CONTROLLER CIRCUIT APPLICATION

INTRODUCTION (CONT)

Sixteen of the 22 lines which energize the character select solenoids are time-shared for keyboard strobing. The pulse width of each strobe signal is of such a short duration that the solenoid sharing the line cannot respond to any strobe signal.

The KPC circuit strobing functions in two modes: the print mode and the non-print mode. In the non-print mode, keyboard scanning occurs every 8 msec. A depressed key will be detected and stored on the first strobe cycle after depression, and verified and accepted as a valid key on the next cycle. This results in a minimum key depression time of 16 msec. In the print mode, the keyboard section operates the same, except that the strobe cycle is initiated upon receipt of the timing pulse from the printer.

When the PPS program is ready to process a new key, the CPU issues a command requesting a keyboard reply. If the key has been accepted the KPC circuit transmits the reply in coded binary on the PPS data bus and a command requesting the corresponding strobe is issued from ROM. Upon transmitting the strobe, the KPC circuit shifts the next key into the output area of the keyboard stack.

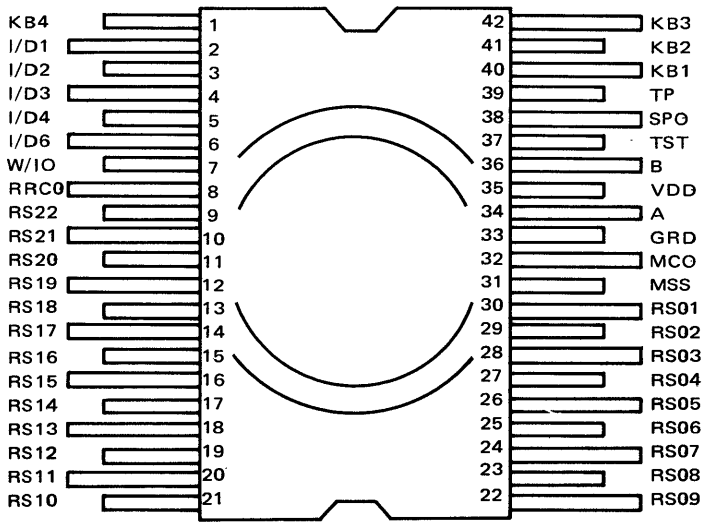
PRINTER CONTROL DESCRIPTION

The printer controller portion of the KPC circuit operates in a stand-alone manner. That is, when the printer controller has been loaded with print data and has been issued a print command, it will initiate and supply all necessary control signals to the printer and accomplish the print cycle without further attention from the PPS system. The printer controller generates a busy-inquiry signal which allows the PPS program to determine when the completion of each print cycle occurs so that a new print cycle can be initiated.

A print output buffer is utilized to hold print data loaded by the program until the print cycle is completed. Clearing of the print output buffer is accomplished at each initial power-on and at the completion of each print cycle. Data may be loaded in any order. If the right most column is to be loaded first, the solenoid driver lines are connected with the number 1 line connected to the right most column. If the programmer decides it is more convenient to load the left most data first, the solenoid driver lines are reversed. In this reverse configuration, leading zeros may be suppressed by transmitting only the data to the right which are actually to be printed, since the print output buffer was previously blanked.

When the PPS program causes the CPU to issue a print command, the instructions for a red or black printout, and, if required, an extra line feed are also issued. Then the KPC circuit issues the proper command to the printer when required. If more than one extra line feed is required, the programmer has only to add additional print commands. Each time a print command is ordered without corresponding data inputs, a line feed is accomplished if the busy inquiry signal is false.

I/D1 – 4	CONTROL FROM PPS CPU
I/D5	KPC ADDRESS
RS01 – 22	KPC OUTPUT TO PRINTER AND KEYBOARD
KB1 – 4	KEYBOARD OUTPUTS TO KPC



PIN CONFIGURATION

FUNCTIONAL DESCRIPTION

The KPC block diagram (Figure 2) shows the various functional circuits in the KPC circuit. A discussion of each of the following listed functional elements is provided in subsequent paragraphs.

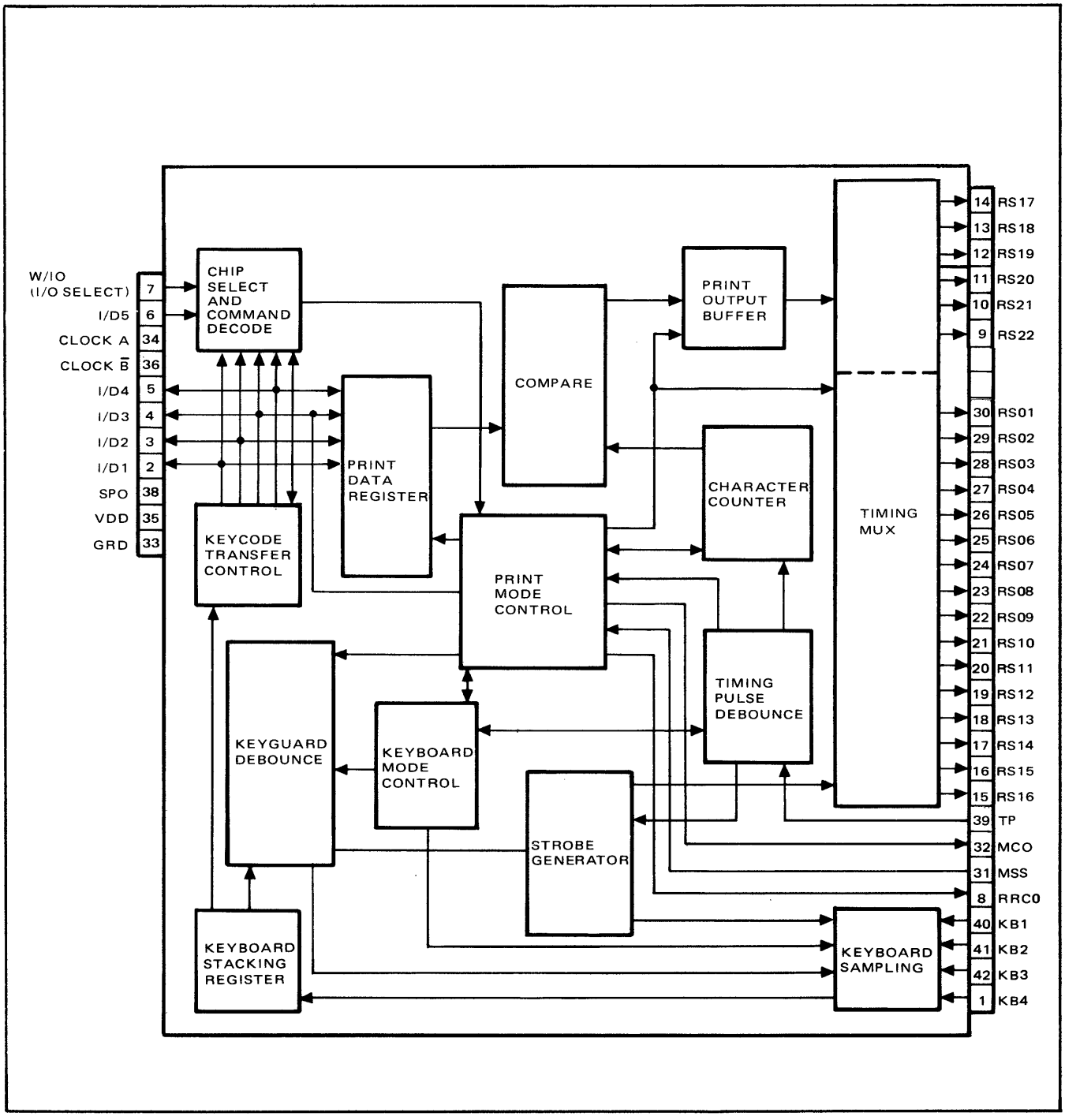


Figure 2. KEYBOARD/PRINTER CONTROLLER (KPC) BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT)

Command Code

The KPC circuit command decode examines the I/O select signal (W/IO) and the I/D5 line. If both are true, the command decode initiates one of the five commands to be executed. These commands are discussed later where applicable. Only I/D5 is examined, therefore, the KPC will respond to all odd addresses limiting the number of I/O devices to nine. However, these can be expanded by gating the I/D5 going into the KPC with a discrete output.

Print Data Register

The KPC circuit print data register consists of a 22 four-bit word serial shift and hold register. When the "load print data" command is received from the command code section, the existing data is shifted to the next word and the four bits of data are loaded into the print data register. The data is received directly (the data is not loaded into the Accumulator) from the RAM at clock time phase-two, two bit times after the "load print data" command. The print mode control provides the proper shift and hold signals.

Printer Timing Pulse (TP) Debounce

The KPC circuit timing pulse debounce minimizes the possibility that a noise pulse on the timing line might cause an incorrect print cycle. The debounce counter checks the timing pulse 21 bit times. To be accepted as a correct timing pulse, it must be true 21 times. This test is also performed on the transition of the timing pulse from a true to false state.

Print Mode Control

The necessary logic to control the printing of a line of characters is provided by the KPC circuit print mode control. When a "print" command is decoded, the data received in lines I/D4 and I/D1 are copied into the print mode control red print and double line feed sections respectively. The print mode controller then goes into the print mode and energizes the motor control output.

When a correct signal is received from the timing pulse debounce, the print mode control signals the keyboard mode control to sample the keyboard one time. The print mode control then causes the print data register to be circulated while the data is being compared to the character counter. The output of the compare is shifted into the print output buffer and on completion of the compare, the selected outputs to the printer solenoids are energized. These outputs remain energized until the timing pulse has gone from the true state to the false state and back to the true state.

After 13 timing pulses have been received, the print mode control waits for the motor stop signal and for the timing pulse to remain false for 24 msec. When this occurs, it sets the printer busy control false provided a double line feed is not required. The KPC circuit is now ready to accept another line of data for printing. Upon decoding a "printer ready inquiry" command, the print mode control will cause the transmission of a binary four to the PPS CPU accumulator which indicates that the printer is not busy.

Character Counter

The timing pulses (TP's) are counted by the character counter to determine which character on the print wheels is in position for solenoid activation.

Comparator

In preparation for energizing the appropriate solenoids, the print data register is circulated and the word in the output position is compared to the state of the character counter. If all four bits of data agree, a true output is fed to the print output buffer.

Print Output Buffer

The print output buffer consists of a 22-bit shift and hold register. The output of the comparator is shifted into the print output buffer and held until the next comparator cycle is started. The outputs of the print output buffer are time multiplexed onto the solenoid select outputs.

Time Multiplexer

Of the 22 solenoid select outputs, 16 are time shared with the strobes to the keyboard. In the print mode, the strobes are outputted sequentially by the time multiplexer for 15 bit times each, and then the selected solenoids are energized.

Keyboard Mode Control

The keyboard mode control generates the logic to generate strobes and sample keyboard replies. The keycodes are also stored by the keyboard mode control until called for by the PPS.

Keyboard Debounce

The keyboard debounce consists of a counter which provides a pulse approximately every eight milliseconds to initiate the keyboard scan cycle when the KPC circuit is in the non-print mode.

FUNCTIONAL DESCRIPTION (CONT)

Strobe Generator

The strobe generator performs several functions. It determines which strobe is to be output, how long the strobe will be held, and provides a signal to initiate keyboard sampling. Strobe cycles are initiated by the keyboard debounce counter when in a non-print mode and by the timing pulse debounce logic when in the print mode.

The KPC outputs the strobes sequentially once each scan cycle until a reply is received from the keyboard. When a reply is received the current strobe count is held until the key is verified and stored and the key is released.

Keyboard Sampling

The keyboard sampling portion of the KPC circuit tests the states of the keyboard reply lines (the keyboard 4-key matrix lines). When a reply is transmitted, the keyboard sampling holds the key code and the key is verified on the next strobe cycle. When the key is verified, the keyboard sampling is then directed to transfer a binary key code into the key stack. A new key cannot be recognized until the previous key has been released.

Keyboard Stacking Register

The keyboard stacking register consists of a 10-key buffer register that stores key codes until transferred out at the request of the PPS microinstruction. The keyboard reply data is stored in three bits, and the active strobe in four bits. When a key is verified, the code is loaded into the first key buffer and then transferred to the next register is empty. This transfer continues until the key code is in the output position. It is then held until requested by the PPS microinstruction.

Key Code Transfer Control

When a command requesting the next keyboard reply is decoded, the keyboard transfer control transmits the three bits of reply data to the PPS CPU. Upon request for the corresponding strobe, the data is transmitted and the next key code is shifted into the keycode transfer control output position.

OPERATION

GENERAL

The operation of the KPC circuit is divided into two functions for purposes of explanation. (1) PPS CPU interface to KPC circuit, and (2) Keyboard and Printer to KPC circuit. Table 1 lists the PPS IOL instructions which are used with the KPC and Figure 10 provides a simplified functional schematic diagram with detailed interface information.

PPS CPU INTERFACE TO KPC

Physical interconnection of the KPC to the CPU is accomplished by connecting the KPC circuit pins to the CPU pins of the same designation. The functional interface is shown in Figure 3. The CPU lines connecting to the KPC circuit are the Instruction Data Command Bus (I/D1 through I/D5), Synchronized Power-on (SPO), and Write Command I/O Select (W/IO).

NOTE: The KPC responds to all odd I/O addresses, therefore only one KPC is allowed per system and all other I/O's must be on even addresses unless a discrete output is used to deselect the KPC.

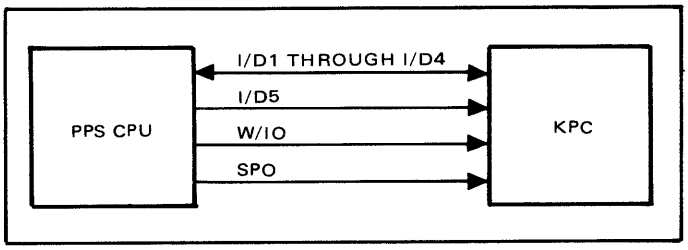


Figure 3. CPU TO KPC INTERFACE

PPS KPC System Timing

All KPC instructions are two-cycle instructions; Figure 4 shows the timing for one KPC instruction. The illustration also shows the manipulation of address and data, and the relationship of this address and data-bus information to the W/IO enable line information and phase-timing.

The PPS IOL instructions used to command the KPC are listed in Table 1. Each IOL instruction command occupies two words in ROM and requires two clock cycle times to execute. The first word of an IOL instruction causes the CPU to generate the enable signal W/IO. The second word of the IOL instruction contains the chip select address and defines the particular IOL command to be executed. (See Table 1).

OPERATION (CONT)

Table 1. KPC CIRCUIT INSTRUCTIONS

INSTRUCTION MNEMONIC	CHIP SELECT		COMMAND I/D				COMMAND NAME	DESCRIPTION
	W/IO	I/D5	4	3	2	1		
TRT	1	1	1	1	0	X	TRANSFER KEYBOARD REPLY	KEY REPLY → DATA BUS I/D1, I/D2, I/D3
TST	1	1	1	0	1	X	TRANSFER KEYBOARD STROBE	KEY STROBE → DATA BUS I/D1, I/D2, I/D3, I/D4
TPB	1	1	1	1	1	X	BUSY INQUIRY	IF BUSY THEN 0 I/D3; IF NOT BUSY THEN 1 → I/D3
LDP	1	1	0	1	1	X	LOAD PRINT DATA	DATA BUS I/D4, I/D3, I/D2, I/D1 → DATA REQUIRED
PRT	1	1	1	0	0	1	PRINT	STARTS PRINT CYCLE, I/D4 RED PRINT CONTROL, I/D1 DOUBLE LINE FEED

NOTE: 1) W/IO IS GENERATED BY THE FIRST WORD OF THE PPS IOL INSTRUCTION.

2) LOGIC 1 IN THE COMMAND CODE INDICATES A VDD VOLTAGE LEVEL ON THE I/D BUS; LOGIC 0 INDICATES A VSS VOLTAGE LEVEL.

3) LOGIC X INDICATES THAT A LOGICAL 1 OR 0 MAY OCCUR AND HAS NO EFFECT ON SELECTION OR COMMANDS.

The sequence of events is as follows: As shown in Figure 4 the first word of an IOL instruction in ROM is addressed during phase 2 of the first clock cycle. This first word is transferred from ROM to the CPU during phase 4 of the first clock cycle to initiate generation of the W/IO enable signal in the CPU. During phase 2 of the second clock cycle the second word of the IOL instruction in ROM is addressed. During phase 4 of the second clock cycle the second word is transferred from ROM to the I/O. At the same time the W/IO enable signal generated by the CPU is accepted by the I/O. The second word contains one of the KPC commands listed in Table 1 and is decoded as follows:

1. I/D5 and I/O designate KPC address.

2. I/D1 through I/D4 designated KPC functions.

During the two clock cycle times just described the desired IOL instruction (KPC command) has been transferred from ROM and placed in I/O, and the CPU has generated the enable signal W/IO. During phase 2 of the next (third) cycle time the W/IO signal commands the RAM to stay off the data bus and the data transfer between the KPC and the CPU takes placed. At phase 2 of the fourth cycle after a LDP, command, data from the RAM will be transferred to the KPC. The KPC will continue to accept data after each LDP command until a PRT command is executed. Note that the RAM address register cannot be modified until two cycles after the LDP command, (See program example, Figure 5).

KEYBOARD AND PRINTER INTERFACE TO KPC

The KPC has 20 lines that form a keyboard matrix. Sixteen lines are strobe lines designated RS01 through RS16. These

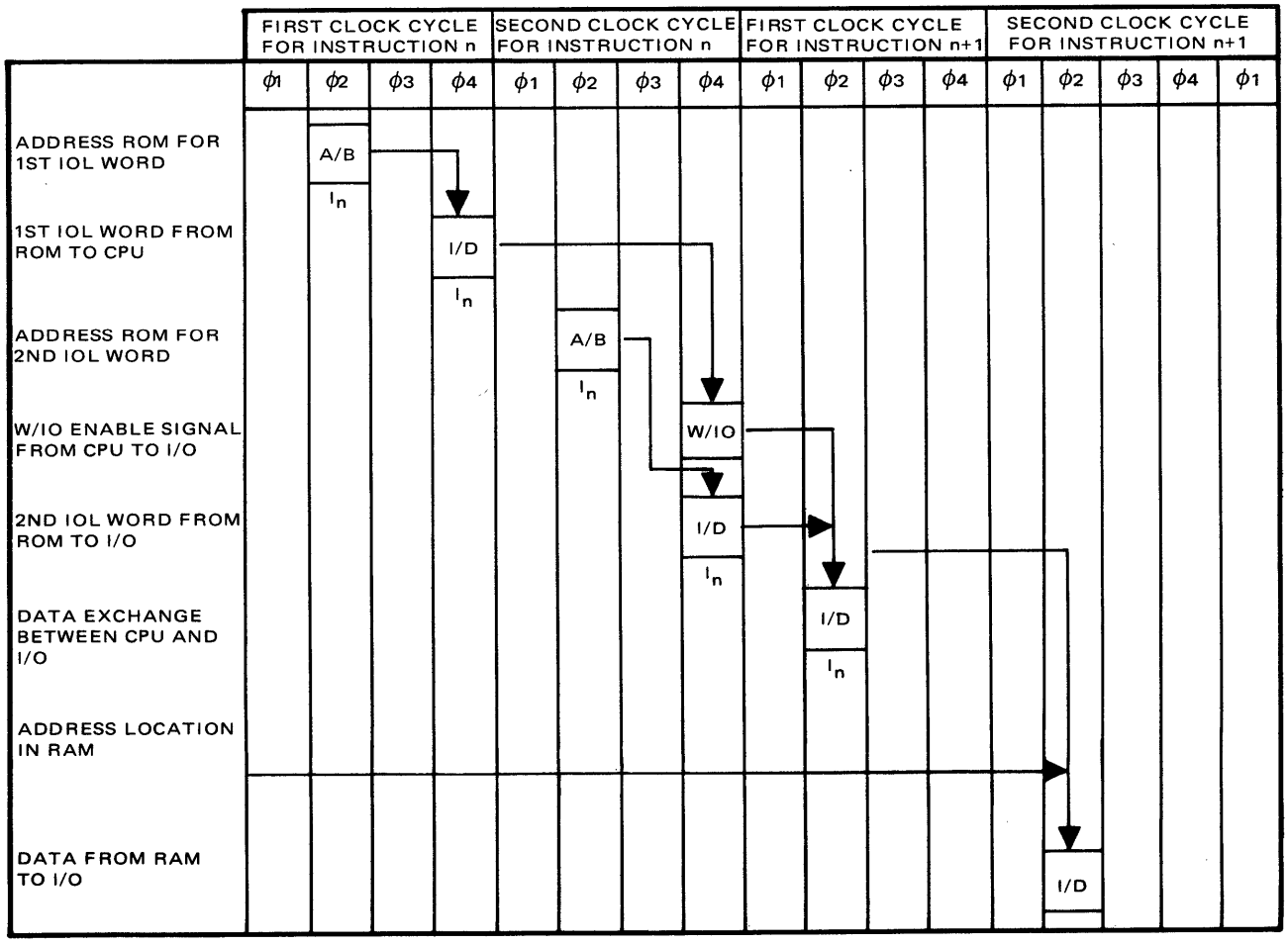
sixteen lines are time-shared with 16 of the 22 printer solenoid lines designated RS01 through RS22. Four lines are reply lines designated KB1 through KB4. Table 2 lists the strobe and reply codes and Figure 6 shows the printer/keyboard timing. Figure 7 illustrates the keyboard strobe timing and Figure 8 the keyboard reply sampling timing. Figure 9 shows a typical KPC keyboard matrix and printer interface application. An example of the keyboard read routine is provided in the flow diagram in Figure 10. A typical KPC to printer and keyboard interface diagram is shown in Figure 11.

Key Actuation Detection

Three possible conditions can result during keyboard operations. These conditions and the associated functions are described as follows:

1. Single Key Depression

   When a key is depressed, the corresponding key code is loaded into the first key buffer register and held there for one keyboard scan cycle (2047 bit times).



NOTES: I = AN I/O INSTRUCTION
n = ANY INSTRUCTION TIME
A/B = ADDRESS BUS (A/B1 THROUGH A/B12)
I/D = DATA BUS (I/D1 THROUGH I/D5)

Figure 4. IOL (KPC) INSTRUCTION TIMING

OPERATION (CONT)

If the key is verified during the next keyboard scan and if no other key is depressed during that period, the key code is defined as a single key depression. Then, the key code is shifted to the next key buffer register if the next key buffer register is available.

2. Simultaneous Key Depressions

Depression of two or more keys within one keyboard scan cycle is defined as a simultaneous key depression. If this condition occurs, the KPC accepts either key and ignores all other keys depressed until only one key remains closed and all of the others are released. Then, the remaining key is treated as a second key depression.

3. Key Rollover

If two keys are depressed with at least one keyboard scan cycle interval between then, the first depressed key is always detected first. If the second key is depressed with the first key down, the second key will be accepted when the first key is released. If the second key is released before the first key, the second key will be ignored. This action provides a two-key rollover feature if the first key depressed is always released first.

Table 2. STROBE AND REPLY CODES

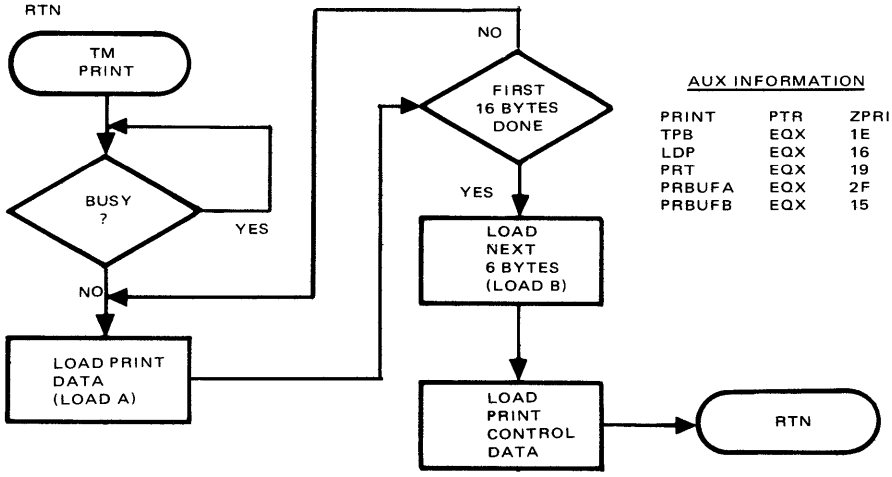
	I/D BUS CODE					I/D BUS CODE			
STROBES	I/D4	I/D3	I/D2	I/D1	REPLY	I/D4	I/D3	I/D2	I/D1
RS01	1	1	1	1	NO KEY	1	1	1	1
RS02	1	1	1	0	KB1	1	1	1	0
RS03	1	1	0	1	KB2	1	1	0	1
RS04	1	1	0	0	KB3	1	1	0	0
RS05	1	0	1	1	KB4	1	0	1	1
RS06	1	0	1	0					
RS07	1	0	0	1					
RS08	1	0	0	0					
RS09	0	1	1	1					
RS10	0	1	1	0					
RS11	0	1	0	1					
RS12	0	1	0	0					
RS13	0	0	1	1					
RS14	0	0	1	0					
RS15	0	0	0	1					
RS16	0	0	0	0					

NOTES: 1) THE LOGIC CONDITIONS SHOWN REPRESENT THE LOGIC LEVELS ON THE I/D BUS LINES (1 = VDD, 0 = VSS).

2) A "0" ON ANY REPLY LINE INDICATES THE PRESENCE OF A KEY.

OPERATION (CONT)

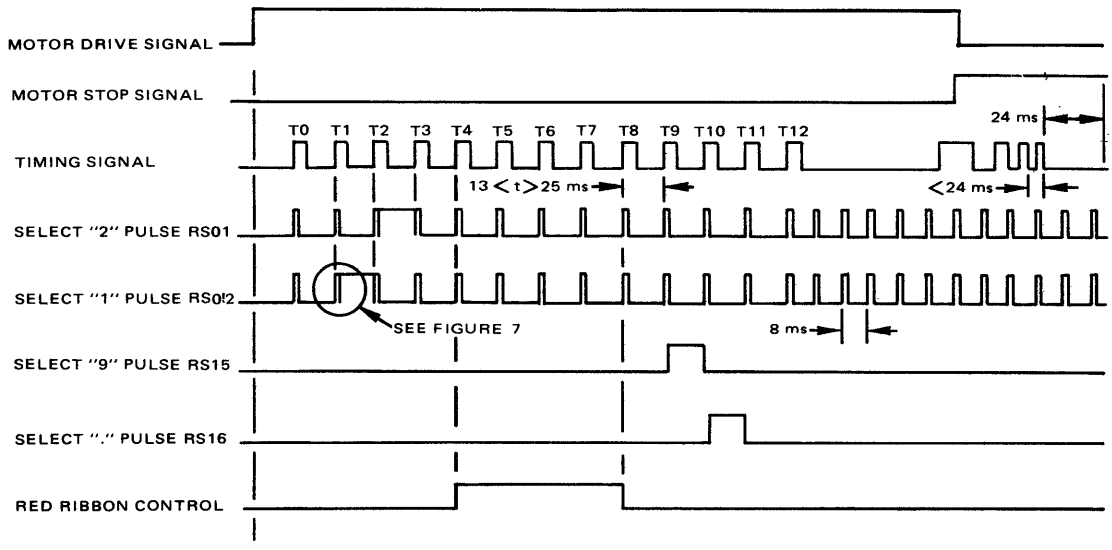
```
          TM      PRINT
          •       •
          •       •
ZPRINT    LBL     PRBUFA    LOAD PRINT DATA BUFFER 'A' ADDRESS
STATUS    IOL     TPB       READ STATUS          (FIRST 16 DATA WORDS)
          ADI     15        BUSY?
          T       STATUS    YES, WAIT.
LOADA     IOL     LDP       LOAD PRINT DATA, FIRST 16 WORDS
          DECB              ADDRESS NEXT WORD, 16 COL LOADED?
          T       LOADA     NO, LOAD NEXT WORD
          LBL     PRBUFB    YES, LOAD PRINT BUFFER 'B', LAST 6 WORDS
LOADB     IOL     LDP       LOAD PRINT DATA, LAST 6 WORDS
          DECB              ADDRESS NEXT WORD, 6 COL LOADED?
          T       LOADB     NO, LOAD NEXT WORD
          LDI     1         YES, LOAD CONTROL, BLACK PRINT, TWO LINE FEEDS
          IOL     PRT       PRINT
          RTN
```



AUX INFORMATION

PRINT	PTR	ZPRINT
TPB	EQX	1E
LDP	EQX	16
PRT	EQX	19
PRBUFA	EQX	2F
PRBUFB	EQX	15

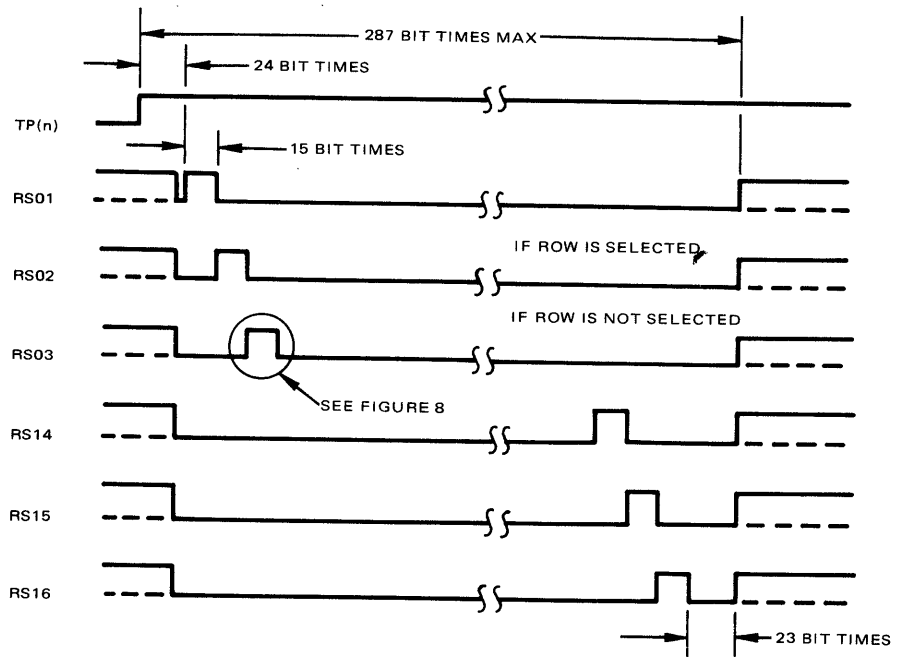
Figure 5. PROGRAM EXAMPLE



NOTE: INTERNALLY GENERATED TIMING IS DEPENDENT ON CLOCK FREQUENCY

Figure 6. KPC PRINTER/KEYBOARD TIMING

OPERATION (CONT)



NOTE:
1. DURING PRINTING, THE STROBE CYCLE IS INITIATED BY TP. WHEN NOT PRINTING, THE CYCLE OCCURS EVERY 8 msec.
2. WHEN SEARCHING FOR A NEW KEY, 16 STROBES ARE OUTPUTTED. WHEN OPERATING ON A KEY, ONLY ONE STROBE IS OUTPUTTED.

Figure 7. KPC KEYBOARD/STROBE TIMING

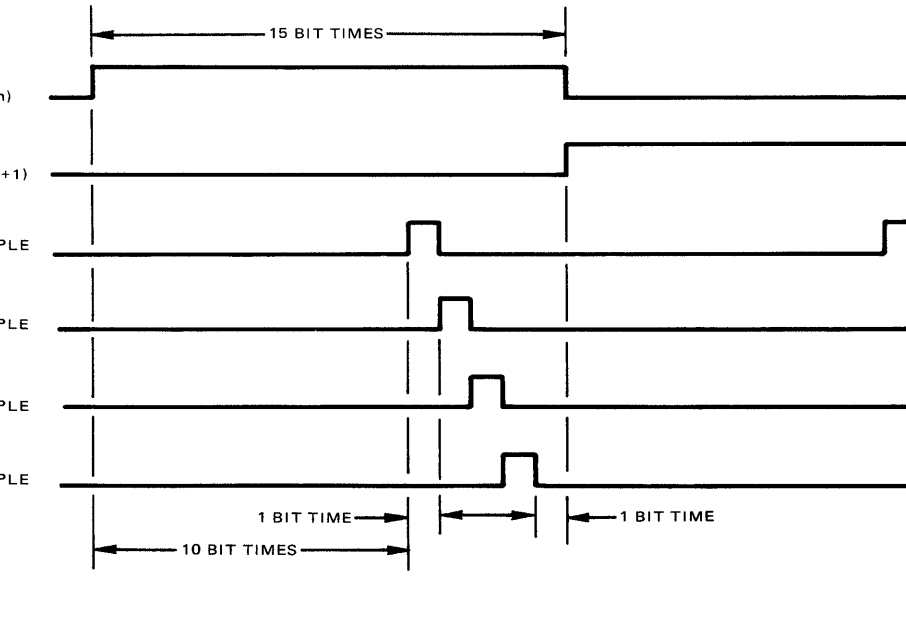


Figure 8. KPC KEYBOARD REPLY SAMPLING TIMING

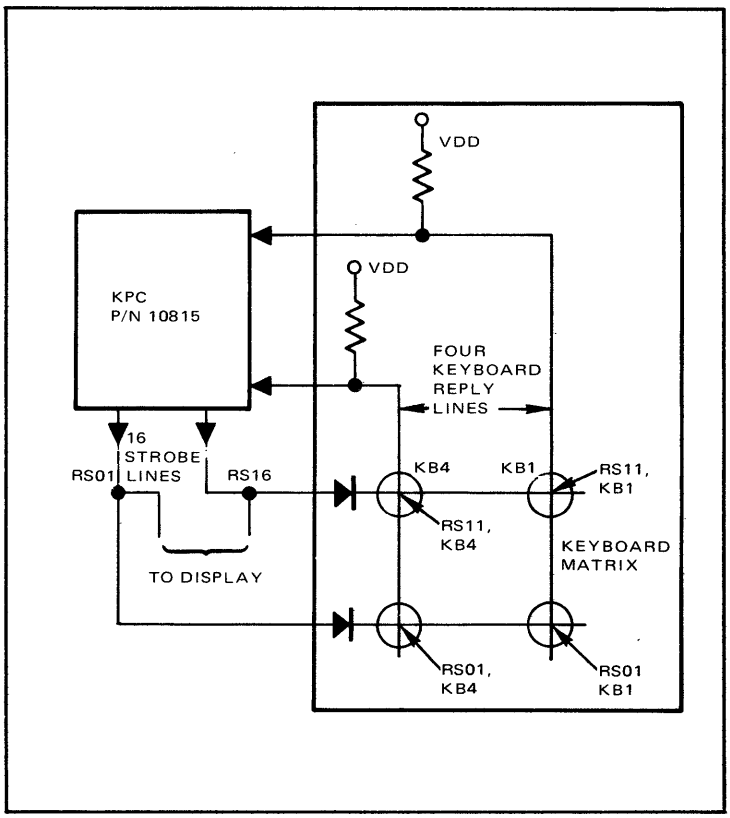


Figure 9. KEYBOARD TO KPC INTERFACE

```
                TM      KEYB
                 •       •
                 •       •
ZKEYB           IOL     TRT     GET REPLY
                SKZ             KEY PRESENT?
                T       *+2     YES, GO STORE
                T       ZKEYB   NO, LOOP
                LBL     KEY     GET KEY STORE
                                ADDRESS
                EXD             STORE REPLY
                IOL     TST     GET STROBE
                EX              STORE STROBE
                RTN             GO TO KEY
                                FUNCTION
                                ROUTINE
```

AUXILIARY INFORMATION

KEYB	PTR	ZKEYB
TRT	EQX	1C
TST	EQX	1A
STR	EQX	1F

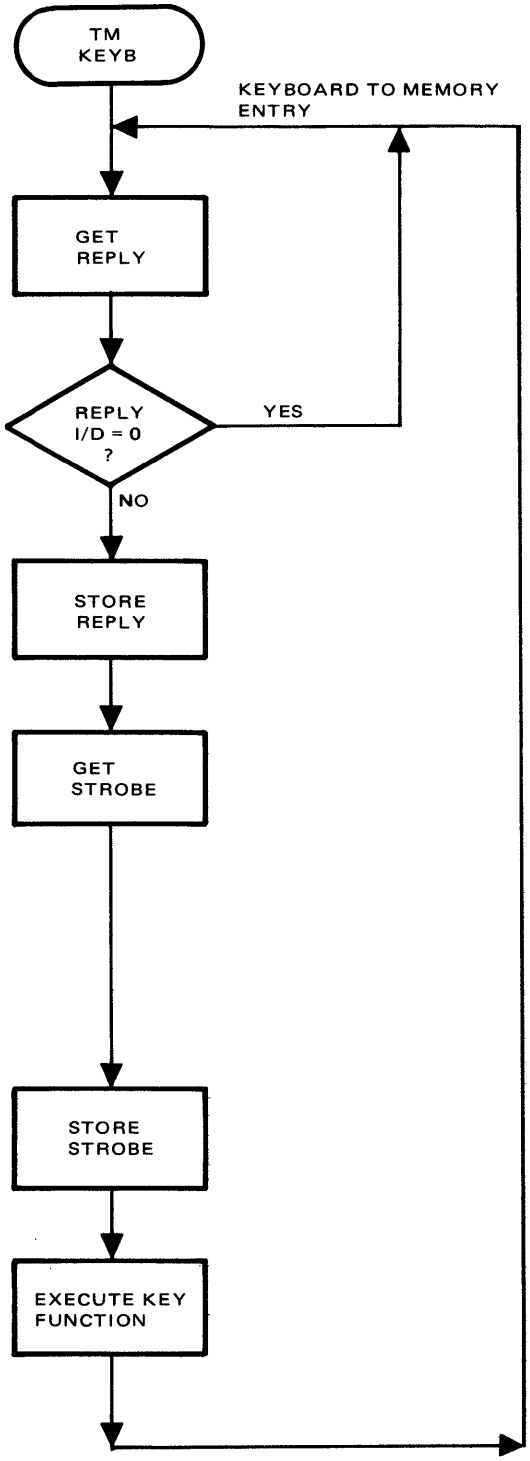
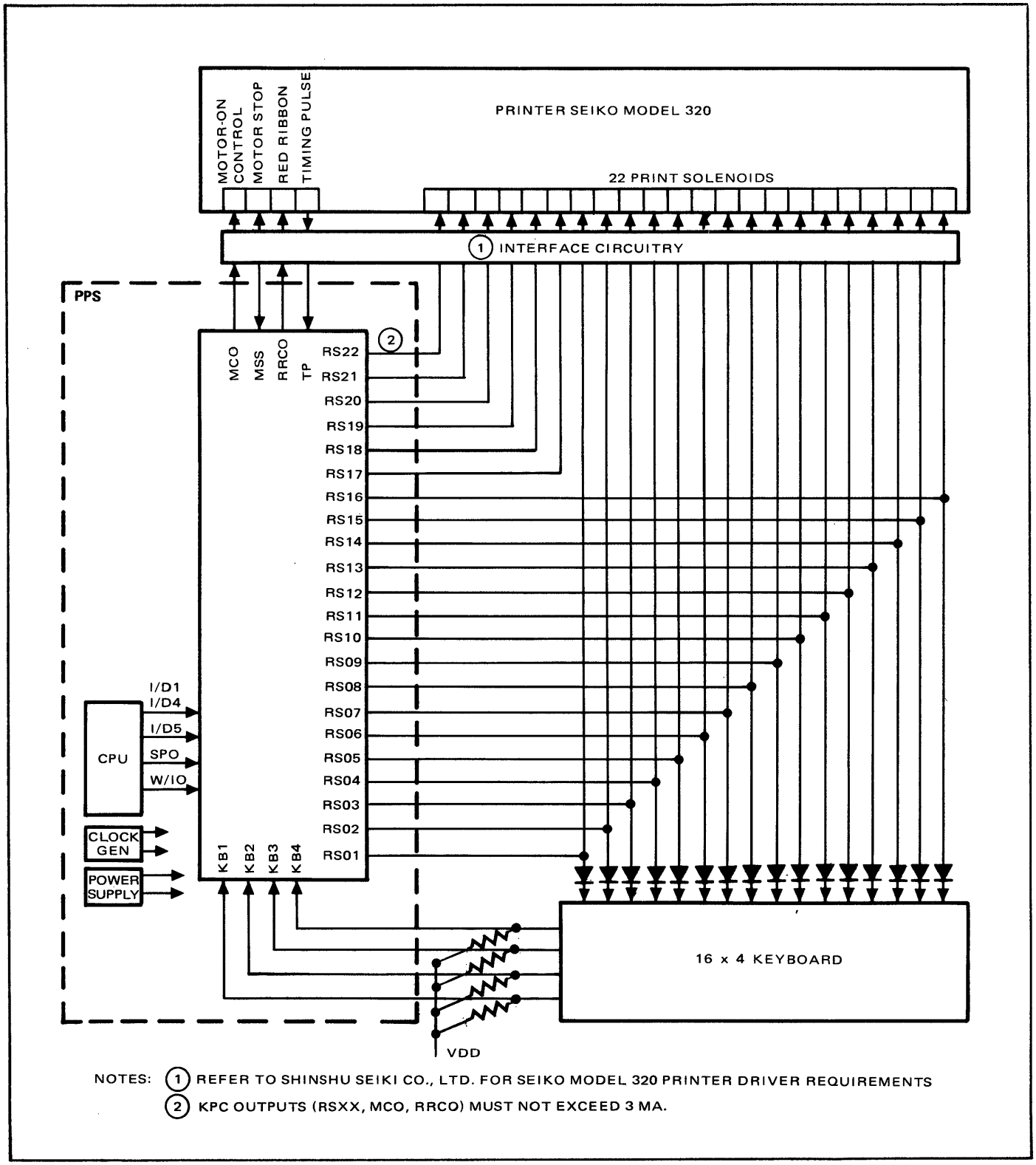


Figure 10. KEYBOARD TO MEMORY, (K→M) FLOW DIAGRAM

OPERATION (CONT)



NOTES: (1) REFER TO SHINSHU SEIKI CO., LTD. FOR SEIKO MODEL 320 PRINTER DRIVER REQUIREMENTS
(2) KPC OUTPUTS (RSXX, MCO, RRCO) MUST NOT EXCEED 3 MA.

Figure 11. KPC TYPICAL INTERFACE DIAGRAM

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage | VDD to VSS |	27 Volts Maximum
Input Voltage With Respect to VSS	-27 Volts Maximum

OPERATING LIMITATIONS AND CHARACTERISTICS

VDD = -17V ± 5%
VSS = 0V
Logic "1" = Most negative voltage (V_{IL}, V_{OL})
Logic "0" = Most positive voltage (V_{IH}, V_{OH})

Operating Temperature, Case (T_A) 0^o to 70^oC
Storage Temperature -55^o to 120^oC
Frequency, Clock: (PPS-4 System Clock 119 kHz or 256 kHz)
Limit Values Determined at T_A of 25^oC Unless Otherwise Noted

Function	Symbol	Parameter	Limits Min	Limits Typ	Max.	Unit	Test Conditions
Power Requirement		Power Dissipation			200	mW	
Supply Current	I_{DD}	Avg Supply Current				mA	
Input and Output, Characteristics							
1. System Bus Instruction/Data Bus (I/D1 I/D5 and W/IO	V_{IH}	Input High Level	-1.5		0.3	V	
	V_{IL}	Input Low Level			▷1	V	
	V_{OH}	Output High Level	-1.0			V	
	V_{OL}	Output Low Level			▷2	V	
2. Keyboard & Printer Interface Return Sampling KB1 – KB4	V_{IH}	V_{IN} High Level	-4		0	V	VDD = 17.0V
	V_{IL}	V_{IN} Low Level	-17		-13	V	
Row/Strobe Select RS01 – RS22 MCO	V_{OH}	V_{OUT} High Level	-3.0			V	I_L = 3.0 mA max
	V_{OL}	V_{OUT} Low Level	(Determined by external load)		-27	V	Floating
MSS, TP	V_{IH}	V_{IN} High Level	-2.5		0.3	V	
	V_{IL}	V_{IN} Low Level	-13		VDD	V	
MCO Motor On	V_{OH}	Output High Level	-4.5			V	3 mA max
RRC0 Red Ribbon Control	V_{OL}	Output Low Level	(Determined by external load)			V	
RS Output Lines MCO, and RRC0	I_O	Output Current			3	mA	
3. Synchronize with Power on (SPO)	V_{OH}	V_{OUT} High Level	-1.0		0.3	V	
	V_{OL}	V_{OUT} Low Level	-7			V	
4. Clock	V_{IH}	Input Low Level	-0.5		0.3		VDD = 17.0V
	V_{IL}	Input Low Level	-10.0		VDD		
5. Capacitance All Logic Inputs and Outputs	C_{IN}	Input Capacitance		5		pF	
	C_{IL}	Load Capacitance		100		pF	
6. Off Input Resistance and Leakage Current All Logic Inputs and Outputs	R_{OFF}	Off Resistance	1 Meg			Ohms	
	I_R	Input Leakage Current			10	μA	
7. Output Impedance (Interface Drivers "ON")	R_{ON}	On Resistance			1000	Ohms	

NOTE: Inputs and output voltage levels indicated by the ▷ symbols vary as a function of | VDD | in accordance with the following equations. (The equations are applicable over the entire operating temperature range.)

▷1 $V_{IL} = -(0.66 \mid VDD \mid - 4.16)V$ (Example: If VDD = -16.15V, V_{IL} = -6.5V)

▷2 $V_{OL} = -(0.66 \mid VDD \mid - 3.16)V$ (Example: If VDD = -16.15V, V_{OL} = -7.5V)

SPECIAL INTERFACE CONSIDERATIONS

RS, MCO, and RCCO Outputs

As shown in Figure 12, the output drivers are open drain buffers which when turned on will connect the KPC output to VSS to energize the corresponding solenoid.

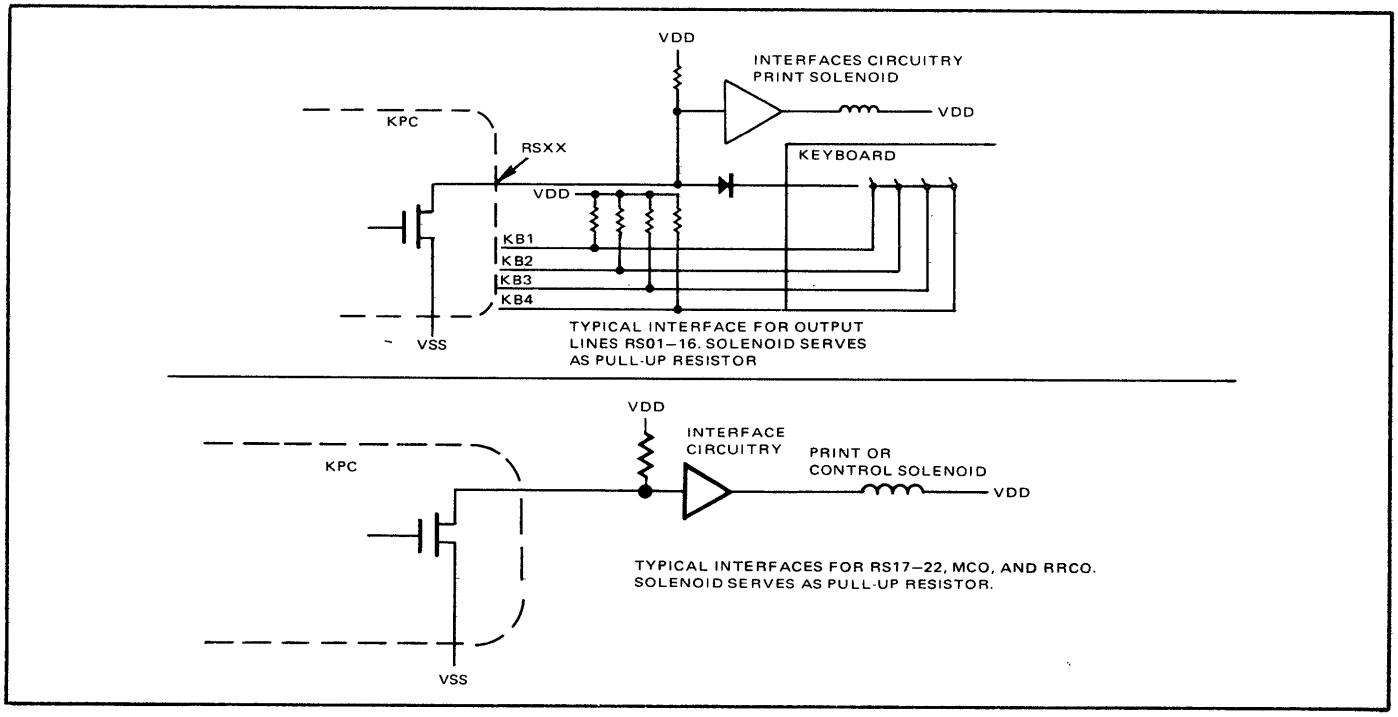


Figure 12. TYPICAL INTERFACE CIRCUITS

NOTICE

Information provided in this Data Sheet is for reference purposes only, and is subject to change without notice.

For specific detail information on this device or for information on any of our other advanced microelectronic devices, please contact the nearest Rockwell International Microelectronic Device Division office.

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Pub. No. 2519-D-22
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MOS/LSI

DATA SHEET

PRELIMINARY

1200 BPS TELECOMMUNICATIONS DATA INTERFACE

MOS/LSI CIRCUIT

Part No. 10371

Microelectronic Device Division
Rockwell International

Document No. 10371 N10

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INTRODUCTION

This data sheet describes the MOS/LSI 1200 BPS Telecommunications Data Interface (TDI) circuit, Part Number 10371, manufactured by the Microelectronics Device Division of Rockwell International. The TDI is intended to operate with external filters, gain circuitry and an approved telephone network access arrangement. The TDI is an advanced type of modem with UART (Universal Asynchronous Receiver Transmitter) capabilities which provides both full-duplex and half-duplex, switched carrier, asynchronous data transmission at 1200 bits per second (bps) over non-conditioned voice-grade telephone lines.

Two basic modes of operation are provided: the serial mode and the PPS mode. In the serial mode, the TDI operates as a universal modem and is assumed to be connected to a serial processor or data terminal which performs all data formatting, decoding and check-bit generation/detection. In the PPS mode, the TDI operates as an integral part of the Rockwell Parallel Processing System (PPS)* and is controlled by microinstructions from the PPS CPU or ROMS. When in the PPS mode, the TDI can be programmed to provide either non-formatted individual bits (similar to the serial mode) or character-formatted words, (see Figure 1). When using character-formatted data, the TDI provides parity generation and detection as well as data buffering. Characters are formatted as eight-bit characters (with or without parity) for asynchronous communication using a start/stop code to delimit the beginning and end of message. The PPS mode also provides variable message-length transmission. From one to eight characters may be transmitted or received within a single pair of start and stop bits, thereby increasing the effective data transmission rate by as much as 17 percent. When operating as part of a PPS-8 system, data transfers between the CPU/ROM and the TDI are initiated on demand by an interrupt system.

*Details of the PPS are covered in Rockwell International Publications 2519-D-13(311) and 2920-D2.

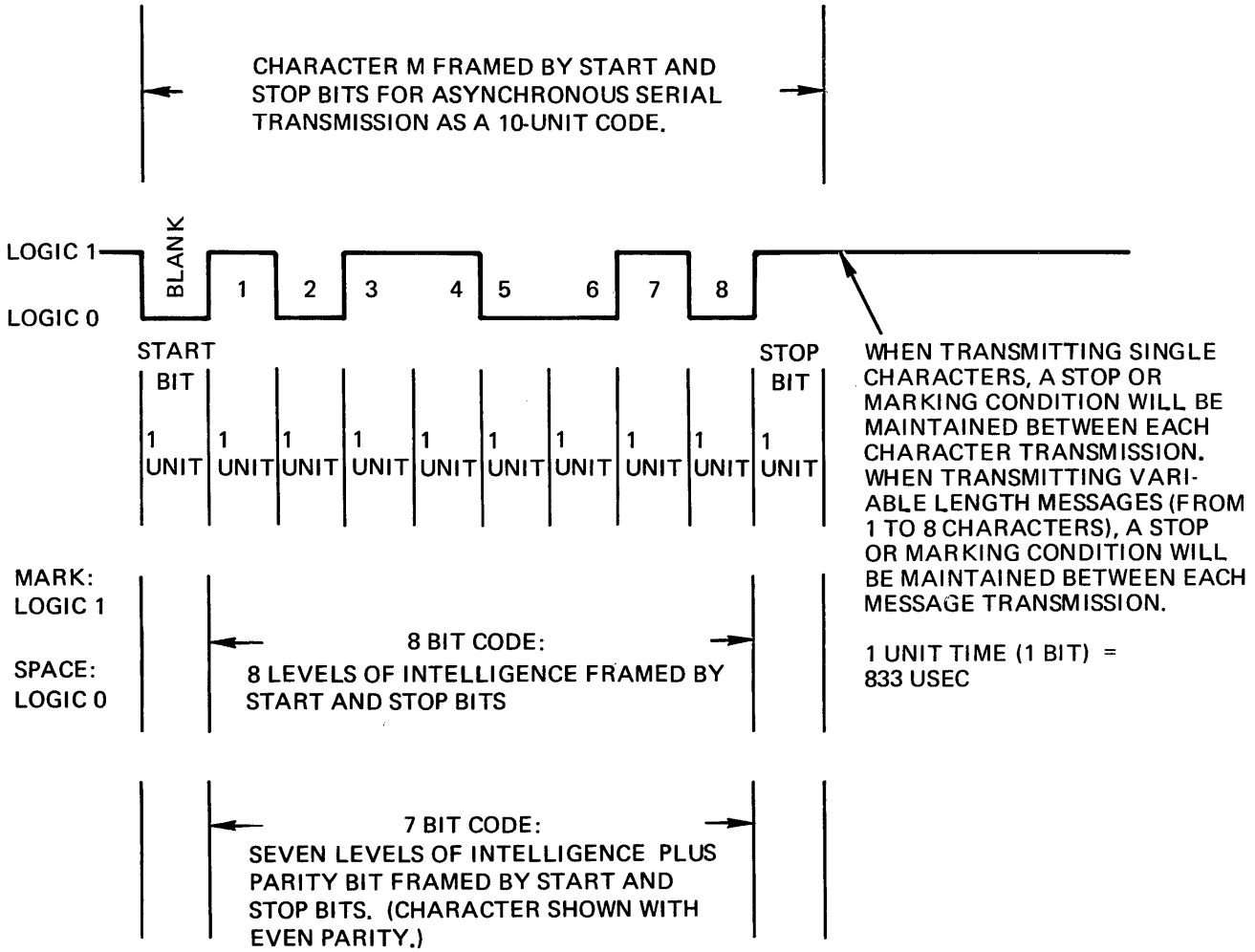


Figure 1. Character Data Format

INTRODUCTION (CONTINUED)

FEATURES

- **Full-duplex or Half-duplex Operation**
- **0 to 1200 BPS Transmission Rate**
- **Strap Selectable Modulating Frequencies (CCITT or Bell 202)**
- **TTL Compatible Interface**
- **Variable Word-Length Transmission**
- **Strap Selectable Chip Address**
- **Automatic Initialization at Power On**
- **Interrupt-Initiated Transfers Between CPU and TDI**

The modulated output of the TDI is provided on four output lines which are intended to be connected to an external four-resistor summing network and amplifier to form the stepped analog waveform (see Figure 2). The values and accuracies of the resistors will be specified by Rockwell on request. The stepped analog waveform is expected to have the following characteristics:

- The second through eighth harmonics should be 35 db below the fundamental.
- The ninth harmonic has the highest energy level and should be 12 db below the fundamental.

The TDI uses frequency modulation in both the serial mode and the PPS mode. In either mode, a choice of two sets of characteristic frequencies is provided:

	F_Z Mark (1)	F_A Space (0)
Set 1 (CCITT):	1300 Hz	2100 Hz
Set 2 (Bell 202):	1200 Hz	2200 Hz

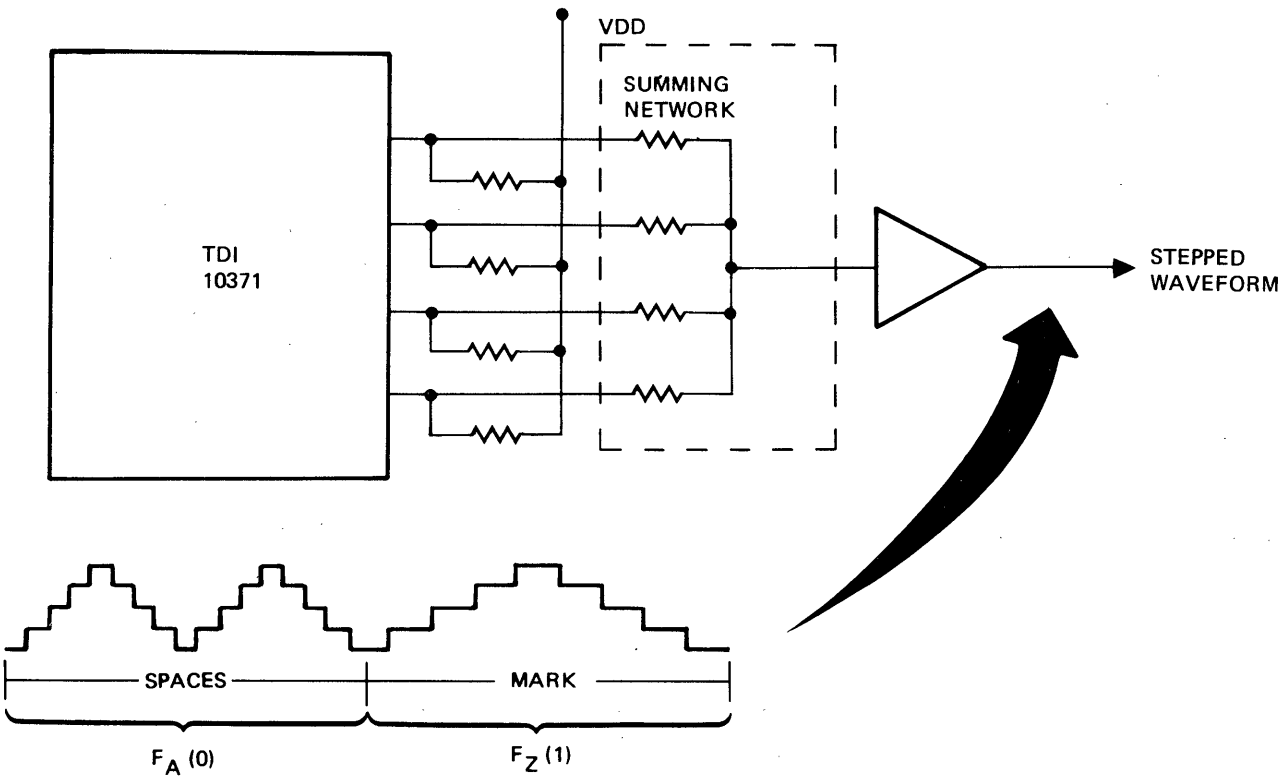


Figure 2. External Summing Network

FUNCTIONAL DESCRIPTION

Figure 3 shows the functional circuits in the TDI; each circuit is briefly described in the following paragraphs.

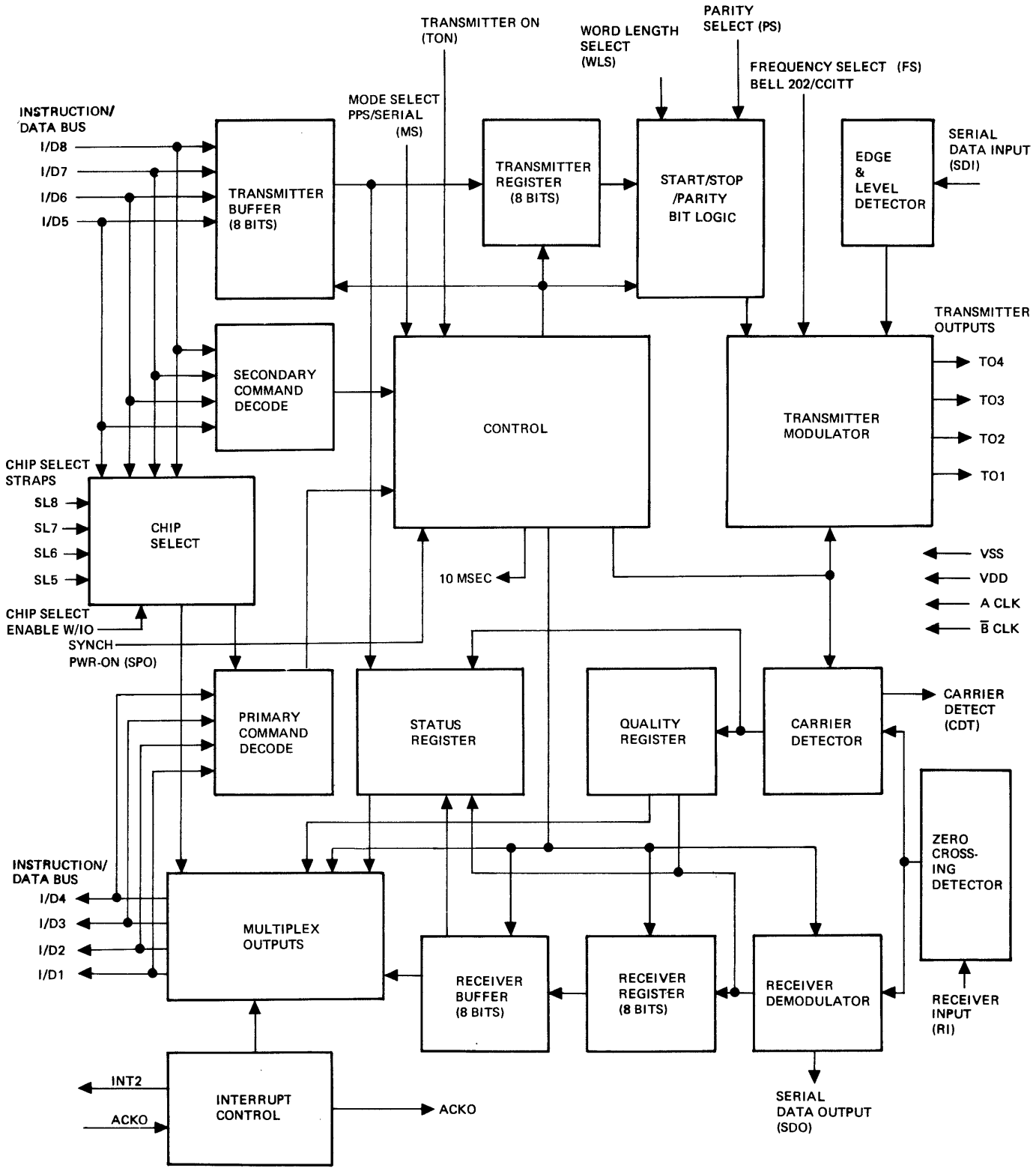


Figure 3. TDI Block Diagram

PPS CPU INTERFACE TO THE TDI

Physical interconnection of the CPU to the TDI is accomplished by connecting CPU lines to TDI circuit pins of the same designation. The interface is shown in Figure 4. The PPS controls the various I/O chips through execution of IOL microinstructions. The PPS IOL microinstructions used to command the TDI are listed in Table 1. Each IOL microinstruction occupies two words in ROM and requires two clock cycle times to execute. The first word of an IOL instruction causes the CPU to generate the IOL enable signal W/IO. The second word of the IOL instruction contains the chip select address and defines the particular IOL command to be executed. (See Table 1.)

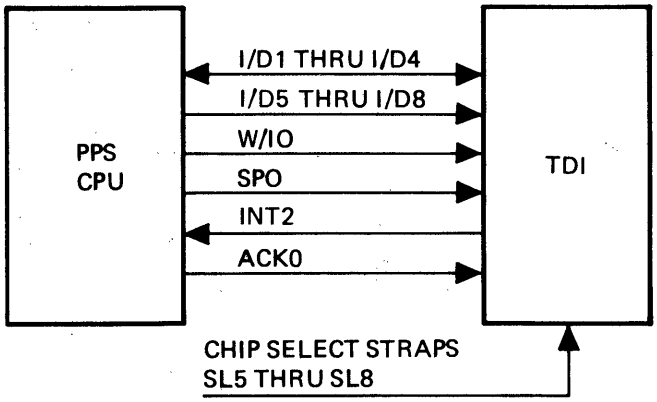


Figure 4. CPU to TDI Interface

Figure 5 shows the timing for a single IOL instruction. The illustration also shows the manipulation of address and data, and the relationship of this address and data-bus information to the W/IO enable line information and phase-timing. The sequence of events is as follows: As shown in Figure 5, the first word of an IOL instruction in ROM is addressed during phase 2 of the first clock cycle. This first word is transferred from ROM to the CPU during phase 4 of the first clock cycle to initiate generation of the W/IO enable signal in the CPU.

During phase 2 of the second clock cycle, the second word of the IOL instruction in ROM is addressed. During phase 4 of the second clock cycle, the second word is transferred from ROM to the I/O. At the same time the W/IO enable signal is transferred from the CPU to the I/O. The second

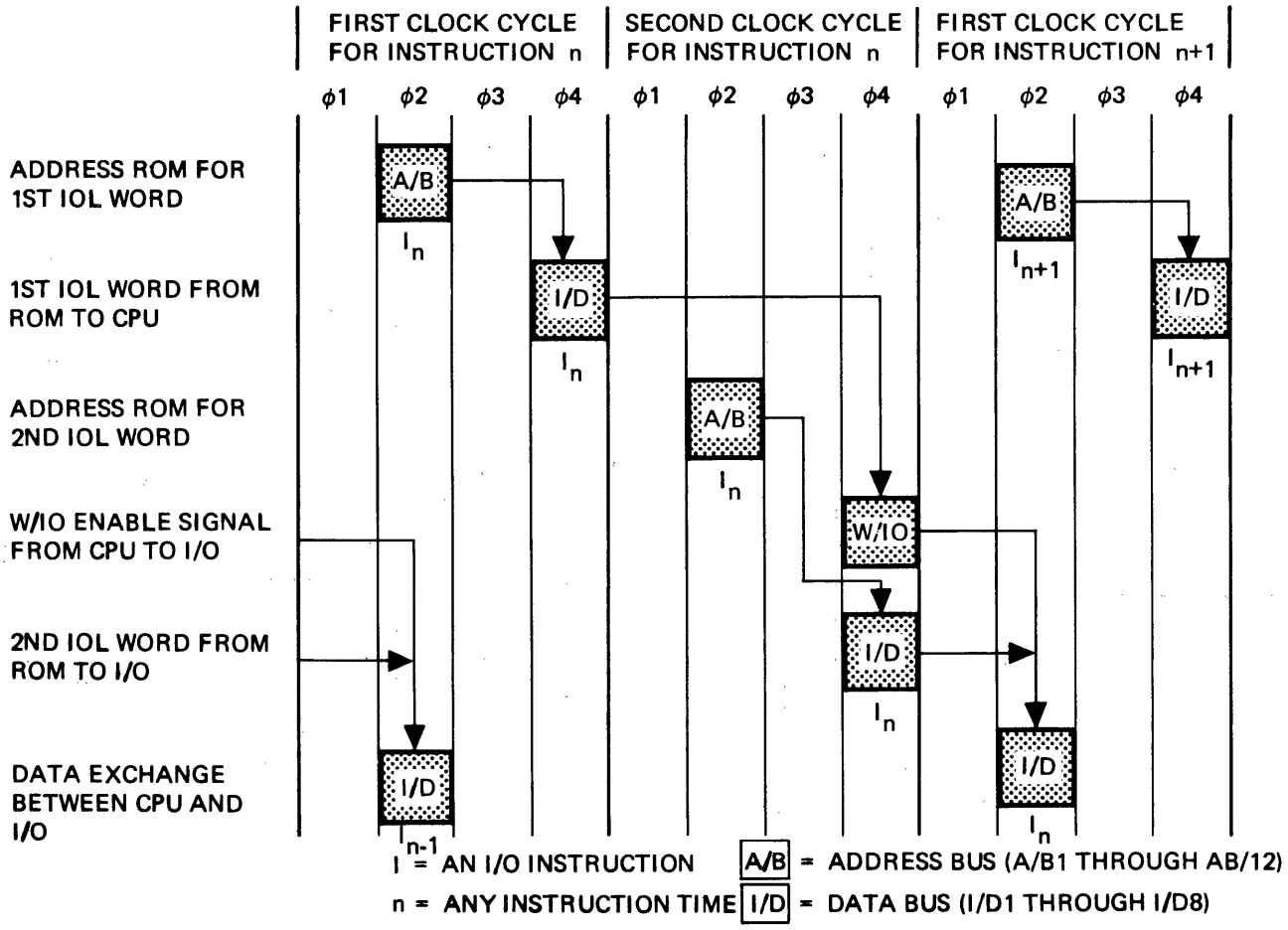


Figure 5. IOL Instruction Timing

word contains one of the TDI commands listed in Table and is decoded as follows:

1. I/D5 through I/D8 designate TDI address.
2. I/D1 through I/D4 designate TDI functions.

During the two clock cycle times just described the desired IOL instruction (TDI command) has been transferred from ROM and placed in I/O, and the CPU has generated the data enable signal W/IO. During phase 2 of the next cycle time the W/IO signal commands the RAM to stay off the data bus and the data transfer between the TDI the CPU takes place. That is, I/D5 through I/D8 transfer data from the CPU accumulator to the TDI and I/D1 through I/D4 transfer data from the TDI to the CPU accumulator. Data transferring from the CPU accumulator to the data bus is inverted, and data on the data bus is inverted before entering the CPU accumulator.

CHIP SELECT DECODE

The chip select decode circuit operates in the PPS mode only. In this mode, the chip select decode circuit compares the chip address on instruction/Data Bus lines I/D5 through I/D8 with the address encoded on chip select straps SL5 through SL8. If agreement exists, and if W/IO is true, the TDI is selected and enabled. Chip select addresses are limited to the range of 01 to 15; address 00 is a special control code used for the PPS-8 interrupt system.

PRIMARY COMMAND DECODE

The primary command decode circuit operates in the PPS mode only. In this mode, the primary command decode circuit determines which of the eight TDI primary commands listed in Table 1 is to be executed. When the TDI is addressed and W/IO is true, the chip select decode circuit enables the primary command decode circuit to receive, store and decode the primary command on Instruction/ Data Bus lines I/D1 through I/D4.

SECONDARY COMMAND DECODE

The secondary command decode circuit operates in the PPS mode only. In this mode, the secondary command decode circuit determines which of the secondary commands is to be executed when the primary command is either RQS or RQR (see Table 1).

CONTROL

The control circuit establishes the basic operating mode (serial mode or PPS mode) based on the state of the mode select (MS) signal as follows. When MS = VDD, the serial mode is selected; when MS = VSS, the PPS mode is selected.

Serial Mode

When the serial mode is selected, the control circuit inhibits all circuits other than those listed below:

Edge and Level Detector

Transmitter Modulator

Zero Crossing Detector

Receiver Demodulator

Carrier Detector

In the serial mode, the control circuit enables the serial data input (SDI) path (via the edge and level detector) to the transmitter modulator and inhibits the transmitter modulator input from the start/stop/parity bit logic. The control circuit operates the transmitter modulator in accordance with the state of the transmitter on (TON) signal as follows. When TON = 1, the transmitter modulator is enabled; when TON = 0, the transmitter modulator is inhibited.

PPS Mode

When the PPS mode is selected, the TDI operating configuration is determined by whether PPS nonformatted mode or PPS character mode operation is programmed. PPS nonformatted mode and PPS character mode operation is selected by specific secondary commands used with RQS and RQR primary commands (see Table 1).

When operating in the PPS nonformatted mode, transmission and reception of individual bits is accomplished by execution of RQS and RQR commands, respectively, and the following circuits are inhibited:

a. Transmit circuits. Transmitter buffer, transmitter register, start/stop/parity bit logic, and edge and level detector.
b. Receive circuits. Receiver buffer, receiver register and error register.

When operating in the PPS character mode, the control circuit enables all other circuits, inhibits the SDI input to the transmitter modulator and enables the transmitter modulator input from the start/stop/parity bit logic. In the PPS character mode, the control circuit provides additional control in response to decoded TDI commands from the primary and secondary command decode circuits to establish data flow paths and provide timing and enabling signals to control register loading, transfers, etc.

TRANSMITTER BUFFER

The transmitter buffer operates in the PPS character mode only. In this mode, the transmitter buffer loads a 4-bit word from the CPU upon execution of an LMT or LLT command (see Table 1). The LMT is executed first and loads the most-significant half of the transmitter buffer. Next, an LLT is executed to load the least-significant half of the transmitter buffer and signal the control circuit that the transmitter buffer is full.

TRANSMITTER REGISTER

The transmitter register operates in the PSS character mode only. In this mode, if the transmitter buffer is full and the transmitter register is not busy, the control circuit initiates an 8-bit parallel transfer from the transmitter buffer to the transmitter register. The contents of the transmitter register are then serially shifted into the start/stop/parity bit logic, least significant bit first.

Table 1. TDI IOL Instructions (Sheet 1 of 5)

Instruction Name and Mnemonic	Ø4 Instruction/Data Bus 2nd Word of IOL		Ø2 Instruction/Data Bus		Description
	Chip Addr	Command	From CPU Accumulator*	To CPU Accumulator*	
	8 7 6 5	4 3 2 1	8 7 6 5	4 3 2 1	
Request To Send (RQS)	X X X X	1 1 0 0	0 0 0 1	– – – –	Transmitter modulator is turned on and continuous spaces are transmitted.
	X X X X	1 1 0 0	0 0 1 0	– – – –	Transmitter modulator is turned on and continuous marks are transmitted.
	X X X X	1 1 0 0	0 1 0 0	– – – –	Transmitter modulator is turned off (no carrier).
				No. of Bits Transmitted	The TDI is set to the asynchronous character transmission mode. The transmitter modulator is turned on and begins sending a stop code. A character transmission will be initiated by the indication of a full transmitter buffer (i.e., execution of an LLT command). Serial transmission will continue for the number of bit times specified by the secondary command. If the transmitter buffer is not reloaded and the secondary command calls for transmission of more than eight bits, the character residing in the transmitter buffer will be retransmitted as many times as necessary to complete transmission of the total number of bits called for by the secondary command. Start and stop codes will frame the number of bits to be transmitted as specified by the secondary command. When the specified number of bits have been transmitted, the transmitter modulator will be held in a stop/mark condition until execution of another RQS.
	X X X X	1 1 0 0	1 0 0 0	– – – –	8
	X X X X	1 1 0 0	1 0 0 1	– – – –	16
	X X X X	1 1 0 0	1 0 1 0	– – – –	24
	X X X X	1 1 0 0	1 0 1 1	– – – –	32
	X X X X	1 1 0 0	1 1 0 0	– – – –	40
	X X X X	1 1 0 0	1 1 0 1	– – – –	48
	X X X X	1 1 0 0	1 1 1 0	– – – –	56
	X X X X	1 1 0 0	1 1 1 1	– – – –	64
		Primary Command	Secondary Command		

Table 1. TDI IOL Instructions (Sheet 2 of 5)

Instruction Name and Mnemonic	Ø4 Instruction/Data Bus 2nd Word of IOL		Ø 2 Instruction/Data Bus		Description
	Chip Addr	Command	From CPU Accumulator*	To CPU Accumulator*	
	8 7 6 5	4 3 2 1	8 7 6 5	4 3 2 1	
Load Most Significant Half of Word (LMT)	X X X X	0 0 1 1	Ø Ø Ø Ø	Ø Ø Ø Ø TDI Status	Transfer Instruction/Data Bus at Ø2 to the most-significant half of transmitter buffer. Simultaneously, transfer contents of TDI status register to data bus. For status word format see TMS instruction. → To transmitter buffer bit 5. → To transmitter buffer bit 6. → To transmitter buffer bit 7. → To transmitter buffer bit 8.
Load Least Significant Half of Word (LLT)	X X X X	1 0 0 1	Ø Ø Ø Ø	Ø Ø Ø Ø TDI Quality	Transfer Instruction/Data Bus at Ø2 to the least-significant half of transmitter buffer. Simultaneously, transfer contents of TDI quality register to data bus. For quality word format, see TMQ instruction. The LLT instruction will set transmitter buffer to full status. → To transmitter buffer bit 1 . → To transmitter buffer bit 2. → To transmitter buffer bit 3. → To transmitter buffer bit 4.

Table 1. TDI IOL Instructions (Sheet 3 of 5)

Instruction Name and Mnemonic	Ø4 Instruction/Data Bus 2nd Word of IOL		Ø2 Instruction/Data Bus		Description
	Chip Addr	Command	From CPU Accumulator*	To CPU Accumulator*	
	8 7 6 5	4 3 2 1	8 7 6 5	4 3 2 1	
Request to Receive (RQR)	X X X X	0 1 1 0	0 0 0 0	– – – –	The TDI is set to receive non-formatted serial bits. The input buffer, start bit detection, and parity logic is inhibited. Received information is handled as individual data bits.
					No. of Bits Received — The TDI is set to receive a synchronous 8-bit characters. Start and stop codes will frame the number of bits to be received as specified by the secondary command. The start and stop bits are removed, parity bits, if present, are replaced by zero's, and each 8-bit character is stored in the receiver buffer. Execution of an RQR instruction will reset the quality register.
	X X X X	0 1 1 0	1 0 0 0	– – – –	8
	X X X X	0 1 1 0	1 0 0 1	– – – –	16
	X X X X	0 1 1 0	1 0 1 0	– – – –	24
	X X X X	0 1 1 0	1 0 1 1	– – – –	32
	X X X X	0 1 1 0	1 1 0 0	– – – –	40
	X X X X	0 1 1 0	1 1 0 1	– – – –	48
	X X X X	0 1 1 0	1 1 1 0	– – – –	56
	X X X X	0 1 1 0	1 1 1 1	– – – –	64
		Primary Command	Secondary Command		
Transfer Most Significant Half of Receiver Buffer (TMR)	X X X X	1 1 1 0	– – – –	Ø Ø Ø Ø	Transfer the most significant half of the receiver buffer to the Instruction/Data Bus at Ø2. From receiver buffer bit 5. From receiver buffer bit 6. From receiver buffer bit 7. From receiver buffer bit 8. (1 = space, 0 = mark)

Table 1. TDI IOL Instructions (Sheet 4 of 5)

Instruction Name and Mnemonic	Ø4 Instruction/Data Bus 2nd Word of IOL		Ø2 Instruction/Data Bus		Description
	Chip Addr	Command	From CPU Accumulator*	To CPU Accumulator*	
	8 7 6 5	4 3 2 1	8 7 6 5	4 3 2 1	
Transfer Least Significant Half of Receiver Buffer (TLR)	X X X X	1 0 1 1	– – – –	Ø Ø Ø Ø	Transfer the least significant half of the receiver buffer to the Instruction/Data Bus at Ø2. From receiver buffer bit 1 From receiver buffer bit 2 From receiver buffer bit 3 From receiver buffer bit 4
Transfer TDI Status (TMS)	X X X X	1 1 0 1	– – – –	Ø Ø Ø Ø	Transfer contents of TDI status register to the Instruction/Data Bus at Ø2. 1 = Currently receiving a Mark 0 = Currently receiving a Space 1 = Presence of carrier on line 0 = Absence of carrier on line 1 = Transmitter buffer full 0 = Transmitter buffer empty 1 = Receiver buffer full 0 = Receiver buffer empty

Table 1. TDI IOL Instructions (Sheet 5 of 5)

Instruction Name and Mnemonic	ϕ4 Instruction/Data Bus 2nd Word of IOL		ϕ2 Instruction/Data Bus		Description
	Chip Addr	Command	From CPU Accumulator*	To CPU Accumulator*	
	8 7 6 5	4 3 2 1	8 7 6 5	4 3 2 1	
Transfer TDI Quality (TMQ)	X X X X	0 1 1 1	– – – –	ϕ ϕ ϕ ϕ	Transfer contents of TDI quality register to the Instruction/Data Bus at ϕ2. Execution of TMQ resets the quality register. 1 = Receiver register overflow (new input data received before receiver register contents transferred to receiver buffer). 0 = No receiver register overflow. 1 = Parity error detected 0 = No parity error detected 1 = Stop bit missing on a character 0 = Stop bit not missing on a character 1 = Carrier was dropped during carrier reception 0 = Carrier was not dropped during character reception

*Notes:

(1) The data and secondary commands are defined as they appear on the Instruction/Data Bus. These must be inverted when referred to the CPU accumulator.

(2) The logic levels as seen on the Instruction/Data Bus are defined as follows:

Logic 1 = VDD (-12V), Logic 0 = VSS (+5V)

START/STOP/PARITY BIT LOGIC

The start/stop/parity bit logic operates in the PPS character mode only. Operation of the start/stop/parity big logic is controlled by the state of the word length select (WLS) signal, the parity select (PS) signal and signals from the control circuit.

The word length select signal (WLS) determines whether the transmitted 8-bit character will or will not include a parity bit. When WSL = VDD, the transmitted character contains eight intelligence bits (no parity bit); when WLS = VSS, the transmitted character contains seven intelligence bits and one parity bit (see Figure 1).

The parity select (PS) signal determines whether odd or even parity shall be provided. When PS = VDD, odd parity is provided; When PS = VSS, even parity is provided. (If WLS = VDD, no parity bit is generated, regardless of the state of PS.)

The control circuit signals the start/stop/parity bit logic as to when to insert start and stop bits as well as parity bits. Variable message-length transmission can range from 8 bits (excluding start and stop bits) to 64 bits, in multiples of 8. Regardless of the number of bits transmitted, only one start bit and one stop bit are transmitted. Thus, a given number of data bits can be

transmitted in less time when using the variable message-length feature. When WLS = VSS (7 bit character), a parity bit is inserted after every seventh data bit.

EDGE AND LEVEL DETECTOR

The edge and level detector operates in the serial mode only. The edge and level detector monitors the serial data input (SDI) signal for leading edge transitions and appropriate levels. SDI is the serial data from the external processor or data terminal.

TRANSMITTER MODULATOR

The transmitter modulator operates in both the serial mode and the PPS mode. In the serial mode, data input to the transmitter modulator is from SDI via the edge and level detector; in the PPS character mode, data input is from the start/stop/parity bit logic. In either case, the transmitter modulator output is provided on four lines (T01 through T04). These four outputs, together with the required external circuitry, form a stepped waveform which represents the modulated output (see Figure 1). The stepped waveform will have the marking frequency (F_Z) as its fundamental component if the data bit being transferred is a one, and the spacing frequency (F_A) as its fundamental component if the data bit is a zero. The characteristic frequencies used for F_A and F_Z are selected by the frequency select (FS) signal:

When FS = VSS, set 1 (CCITT) is used:

F_Z = Mark (1) = 1300 Hz

F_A = Space (0) = 2100 Hz

When FS = VDD, Set 2 (Bell 202) is used:

F_Z = Mark (1) = 1200 Hz

F_A = Space (0) = 2200 Hz

The transmitter modulator is inhibited when in the serial mode and TON = 0 or when in the PPS character mode and the transmitter register is empty. When inhibited, the transmitter modulator outputs are floating.

When operating in the PPS non-formatted mode, the transmitter modulator is turned on and off by a series of RQS commands to produce individual bits (see Table 1).

ZERO CROSSING DETECTOR

The zero crossing detector operates in both the serial mode and the PPS mode. The zero crossing detector monitors the receiver input (RI) signal (from the telephone line interface circuit) for leading edge transitions and appropriate levels.

RECEIVER DEMODULATOR

The receiver demodulator operates in both the PPS mode and the serial mode. In either mode, the receiver demodulator converts the incoming frequency coded data to digital form for subsequent processing. In the serial mode, the serial data output (SDO) of the receiver demodulator is available for use by the external processor or data terminal.

RECEIVER REGISTER

The receiver register operates in the PPS character mode only. In this mode, the receiver register accumulates eight bits of data as it is received serially from the receiver demodulator. When the control circuit detects that the receiver register is full, it initiates an 8-bit parallel transfer from the receiver register to the receiver buffer.

RECEIVER BUFFER

The receiver buffer operates in the PPS character mode only. In this mode, the receiver buffer provides intermediate storage of the incoming data, thereby allowing the receiver register to accumulate additional data without waiting for PPS sampling.

CARRIER DETECT

The carrier detect circuit operates in both the PPS mode and the serial mode. In either mode the carrier detect circuit provides outputs indicating the presence or absence of a carrier on the incoming line. In the serial mode, the output (CDT) is applied to the external processor or data terminal. In the PPS mode, CDT is inhibited and a similar output is provided to the quality register and the status register.

QUALITY REGISTER

The quality register operates in the PPS character mode only. The quality register monitors inputs from the receiver demodulator and the carrier detect circuit. The contents of the quality register have the following meaning:

Bit 1 = 1: Receiver register overflow (new input data received before receiver register contents transferred to receiver buffer)
Bit 1 = 0: No receiver register overflow

Bit 2 = 1: Parity error detected
Bit 2 = 0: No parity error detected

Bit 3 = 1: Stop bit missing on a character
Bit 3 = 0: Stop bit not missing on a character

Bit 4 = 1: Carrier dropped during character reception
Bit 4 = 0: Carrier not dropped during character reception

STATUS REGISTER

The status register operates in the PPS mode only. The status register monitors inputs from the receiver demodulator,

carrier detector, receiver buffer and transmitter buffer. The contents of the status register have the following meaning:

Bit 1 = 1: Currently receiving a mark (1)
Bit 1 = 0: Currently receiving a space (0)

Bit 2 = 1: Presence of carrier on line
Bit 2 = 0: Absence of carrier on line

Bit 3 = 1: Transmitter buffer is full
Bit 3 = 0: Transmitter buffer is empty

Bit 4 = 1: Receiver buffer is full
Bit 4 = 0: Receiver buffer is empty

MULTIPLEX OUTPUTS

The multiplex outputs circuit operates in the PPS mode only. The multiplex outputs circuit provides a time-shared interface with the PPS CPU Instruction/Data Bus lines I/D1 through I/D4. Under program control, the CPU can accept the contents of the receiver buffer, quality register and status register via the multiplex outputs circuit. In PPS-8 systems, the CPU can also accept the strap encoded chip select address via the multiplex outputs circuit (see the following description of the interrupt control).

INTERRUPT CONTROL

The interrupt control operates in the PPS character mode only, and only in PPS-8 systems. The interrupt control allows the CPU to service the TDI on a demand basis. The interrupt control monitors the status register contents (bits 3 and 4) to determine whether the transmitter buffer is empty or the receiver buffer is full. If either condition exists, the interrupt control generates a data interrupt request (INT2). The CPU, in response to INT2 generates an interrupt acknowledge signal (ACKO). If the TDI interrupt is the highest priority interrupt present, ACKO is allowed to propagate through on various I/O devices to the TDI. After a time delay sufficient to allow ACKO to propagate through the I/O device chain, the CPU execute a Device Address Request Instruction. The requesting device which has received the acknowledge pulse then transmits its device address (1 to 15) over the Instruction/Data Bus to the CPU. This address is decoded under CPU software control and used to identify the proper interrupt processing routine. (The Device Address Request is also used by the I/O device to reset its INT2 output).

The interrupt response subroutine must include tests to determine whether the interrupt was generated as a result of the transmitter buffer being empty or the receiver buffer being full. This information is available in the status register and may be sampled by the TMS command (see Table 1). After determining the desired direction of data flow (CPU output to empty transmitter buffer or CPU input from full receiver buffer), the appropriate data transfer commands (LMT and LLT or TMR and TLR) are executed.

It should be noted that when operating in the PPS non-formatted mode, the transmitter buffer and the receiver buffer are inhibited and, consequently, the interrupt control is also inhibited. Thus, when there is no data to transmit, a RQS primary command with a transmitter off secondary command will prevent the empty transmitter buffer from initiating interrupts.

OPERATIONAL INFORMATION

TDI COMMANDS

The TDI has eight primary commands specified by the least-significant half of the second word of the IOL instruction. Functionally, these commands are divided into three groups:

Receiver Commands

RQR	Request to receive
TMR	Transfer most-significant 4 bits of receive buffer
TLR	Transfer least-significant 4 bits of receive buffer

Transmitter Commands

RQS	Request to send
LMT	Load most-significant 4 bits of transmitter buffer
LLT	Load least-significant 4 bits of transmitter buffer

Status Commands

TMS	Transfer modem status
TMQ	Transfer modem quality

Two of these commands (RQR and RQS) are further defined by secondary commands. The secondary command must reside in the CPU accumulator prior to execution of the RQR or RQS command. The secondary command appears on the Instruction/Data Bus at Ø2 of the second half of the IOL instruction.

The codes and functions of the TDI primary and secondary commands are defined in Table 1. The signal polarity is specified as seen on the Instruction/Data Bus. There is signal inversion between the CPU accumulator and the Instruction/Data Bus; therefore, care should be taken to use the compliment of the Ø2 signals when they are referenced to the CPU accumulator.

INTERFACE

The TDI has the following three types of signal interfaces: a TTL digital interface with the serial processor or data terminal, a multiplex interface that is compatible with the PPS Instruction/Data Bus, and an analog interface with the telephone line via its associated interface circuitry. Figure 6 and Table 2 provide summaries of the data terminal, PPS and analog line interfaces. Figure 7 defines signal polarities as they appear at the TDI interface.

ELECTRICAL SPECIFICATIONS

ELECTRICAL REQUIREMENTS

Power Supplies

TTL	VSS	+5 VDC ±0.5 VDC @ 50 ma referenced from ground including line and loading. Ripple shall be no more than 100 mv peak-to-peak within one clock period.
	VDA	0 VDC (GND)
	VDD	−12 VDC ±0.6 VDC @ 50 ma referenced from ground including line and loading. Ripple shall be no more than 100 mv peak-to-peak within one clock period.
or		
MOS	VSS	0 VDC (GND)
	VDD	−17 VDC

Clocks

A Clock — Clock A is a signal having a nominal duty cycle of 50%, a 0 level more positive than −0.5 volts and a 1 level more negative than −10.0 volts. The frequency is derived from a 3.579545 MHz crystal frequency referenced and is typically 256 KHz. This signal is further described in Rockwell Microelectronics Device Specification 10706P11, Rev. B.

$\overline{B}$ Clock — Clock $\overline{B}$ is a signal having a nominal duty cycle of 30%, a 0 level more positive than −0.5 volts and a 1 level more negative than −10.0 volts. The frequency is also crystal derived and is typically twice the A clock frequency. This signal is further described in Rockwell Microelectronics Device Specification 10706P11, Rev. B.

ENVIRONMENTAL REQUIREMENTS

The TDI satisfies the requirements of this data sheet over the following range of environmental conditions:

Temperature

Operating	$0^{o}C$ to $70^{o}C$
Storage	$-55^{o}C$ to $120^{o}C$

Humidity

The TDI is designed to operate functionally in a RH of 0 to 90% for a minimum of 240 hours.

TYPICAL INTERFACE DIAGRAM

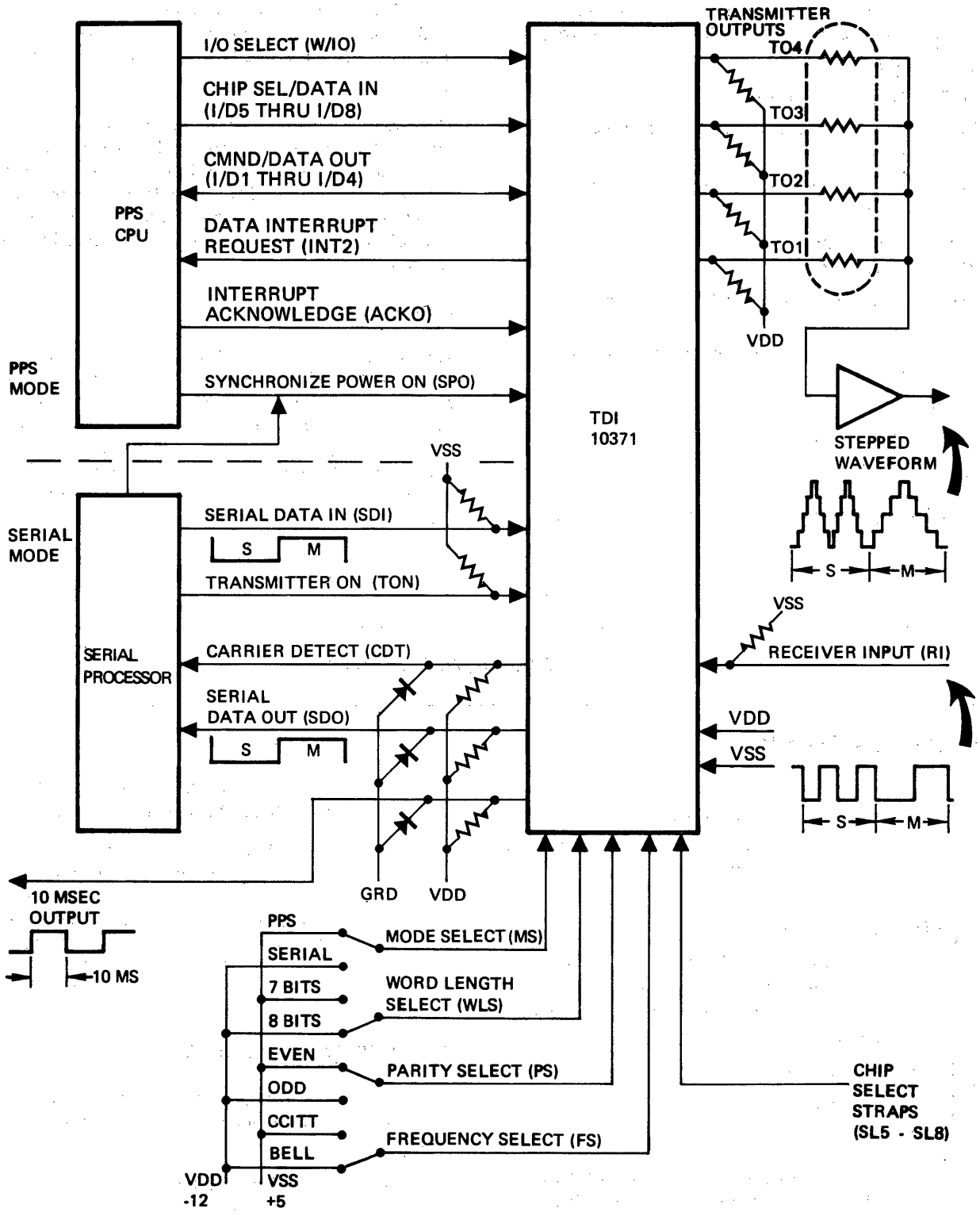


Figure 6. Typical Interface Diagram

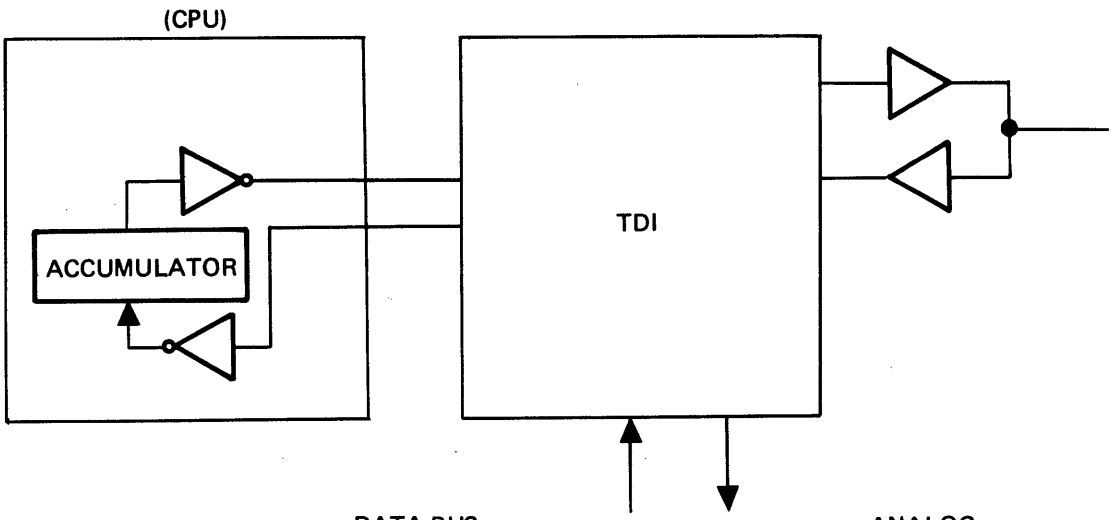
Table 2. Interface Signals (Sheet 1 of 2)

Interface Type	Signal Direction	Signal Name	Description
TTL to Serial Processor or Data Terminal	TDI Inputs	SDI	Serial Data Input. SDI is the serial mode data input to the TDI. It provides data to be transmitted after modulation. See Figure 8 for required interface circuitry. Logic 1 (Mark) = (VSS + 0.3) to (V_{SS} – 0.5) Logic 0 (Space) = OV (Grd) to +0.4V
		TON	Transmitter On. TON is the serial mode control for the transmitter modulator. See Figure 8 for required interface circuitry. Logic 1 (Enable Transmitter) = (V_{SS} + 0.3) to (V_{SS} – 0.5) Logic 0 (Inhibit Transmitter) = OV (Grd) to +0.4V
	TDI Outputs	SDO	Serial Data Output. SDO is the output decision resulting from demodulating the receiver input (RI) signal. See Figure 9 for required interface circuitry. Logic 1 (Mark) = 1KΩ (max) to V_{SS}; max current capability = 2.7 MA Logic 0 (Space) = Output Floating
		CDT	Carrier Detect. The CDT signal indicates the presence or absence of a carrier at the receiver input (RI). See Figure 9 for required interface circuitry. Logic 1 (Carrier Present) = 1KΩ (max) to V_{SS}; max current capability = 2.7 MA Logic 0 (Carrier Absent) = Output floating
PPS	TDI Inputs	SPO W/IO I/D5 thru I/D8 ACKO	Sync Power On Chip Select Enable Instruction/Data Bus Lines 5 thru 8 Interrupt Acknowledge Refer to the general device specification for standard parallel processing system devices, No. 20101P11, for signal definition.

Table 2. Interface Signals (Sheet 2 of 2)

Interface Type	Signal Direction	Signal Name	Description
PPS	TDI Inputs/Outputs	I/D1 thru I/D4	Instruction/Data Bus Lines 1 thru 4. Refer to the general device specification for standard Parallel Processing System devices, No. 20101P11, for signal definition
	TDI Output	DIR INT2	Data Interrupt Request. Refer to the general device specification for standard Parallel Processing System Devices, No. 20101P11, for signal definition.
	TDI Strap Inputs	SL5 thru SL8	Chip Select — Refer to the general device specification for standard Parallel Processing System Devices, No. 20101P11, for signal definition
		MS	Mode Select
		WLS	Word Length Select
		PS	Parity Select
		FS	Frequency Select
Analog TTL to Telephone Interface Circuitry	TDI Input	RI	Receiver Input. RI is the signal from the telephone line interface circuit after external band-pass filtering, compromise equalization and hard limiting. See Figure 8 for required interface circuitry. Logic 1 (Mark) = (V_{SS} + 0.3) to (V_{SS} −0.5) Logic 0 (Space) = OV (Grd) to + 0.4V
	TDI Outputs	TO1 thru TO4	Transmitter Modulator Outputs. These four outputs, together with the required external circuitry (see Figure 1) from a stepped waveform which represents the output of the transmitter modulator. See Figure 10 for required signal interface circuitry. Logic 1 = 1KΩ (max) to V_{SS}; max current capability = 2.7 MA Logic 0 = Output floating
		10 MSEC	10 Millisecond real time reference signal. This signal is generated from a countdown of the PPS clock and appears as a symetrical square wave of 50 Hz. The counter is reset with SPO and the first transition occurs 10 milliseconds following SPO.

DEFINITION OF SIGNAL POLARITY



DATA BUS

	PPS ACCUMULATOR	DATA & COMMAND	SERIAL MODE TTL	ANALOG TELEPHONE INTERFACE
MARK/STOP CONDITION	LOGIC 1	LOGIC 0*	LOGIC 1	LOGIC 1
	———	VSS (+5)	VSS (+5V)	———
	MARK/STOP	MARK/STOP	MARK/STOP	MARK/STOP
	———	———	———	LOWER FREQUENCY
SPACE/STR. CONDITION	LOGIC 0	LOGIC 1	LOGIC 0	LOGIC 0
	———	VDD (-12)	GND (0 V)	———
	SPACE/START	SPACE/START	SPACE/START	SPACE/START
	———	———	———	HIGHER FREQUENCY

*NOTE: THE COMMAND CODES OF TABLE 1 REFERENCE THE LOGIC NOTATION ON THE DATA BUS. THE DATA AND SECONDARY COMMANDS MUST BE INVERTED WHEN REFERRED TO THE CPU ACCUMULATOR.

Figure 7. Definition of Signal Polarity

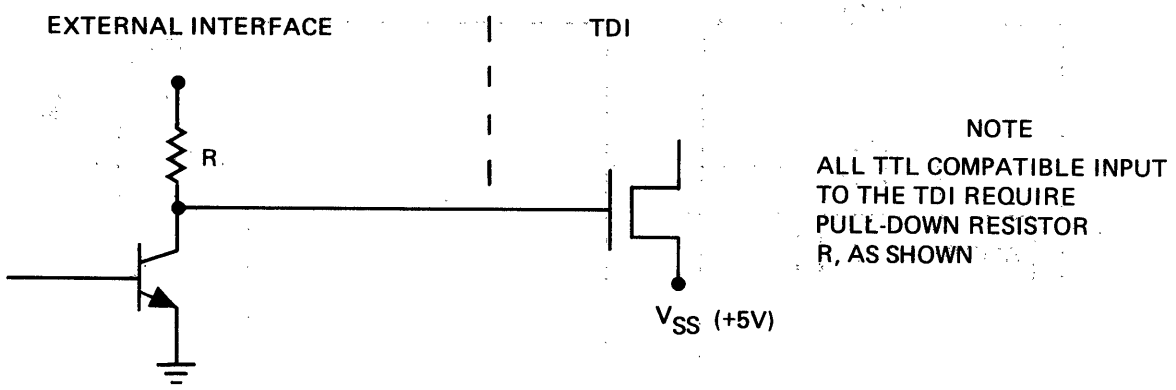


Figure 8. TTL Compatible Interface for SDI, TON and RI

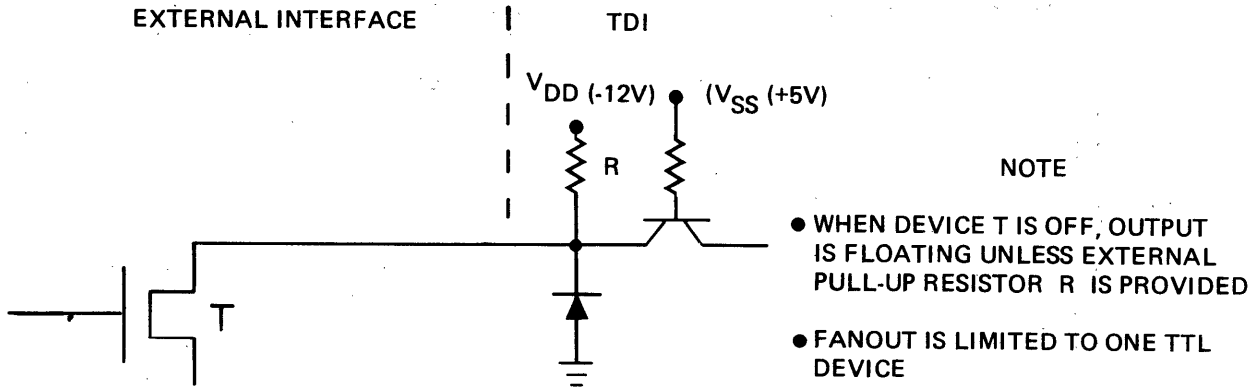


Figure 9. TTL Compatible Interface for SDO and CDT.

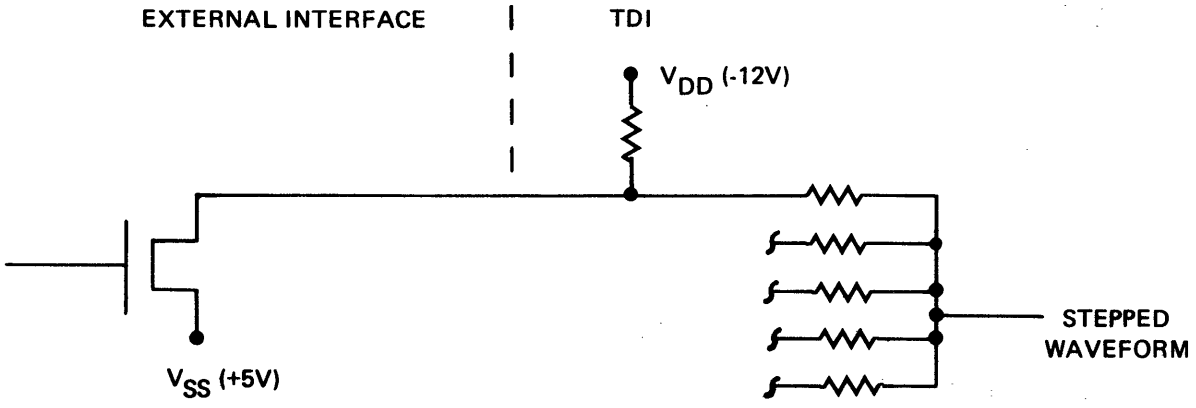


Figure 10. TTL Compatible Interface for TO1 through TO4