704 IC SYSTEMS COMPUTER

TECHNICAL MANUAL

OPERATION AND MAINTENANCE

BASIC COMPUTER

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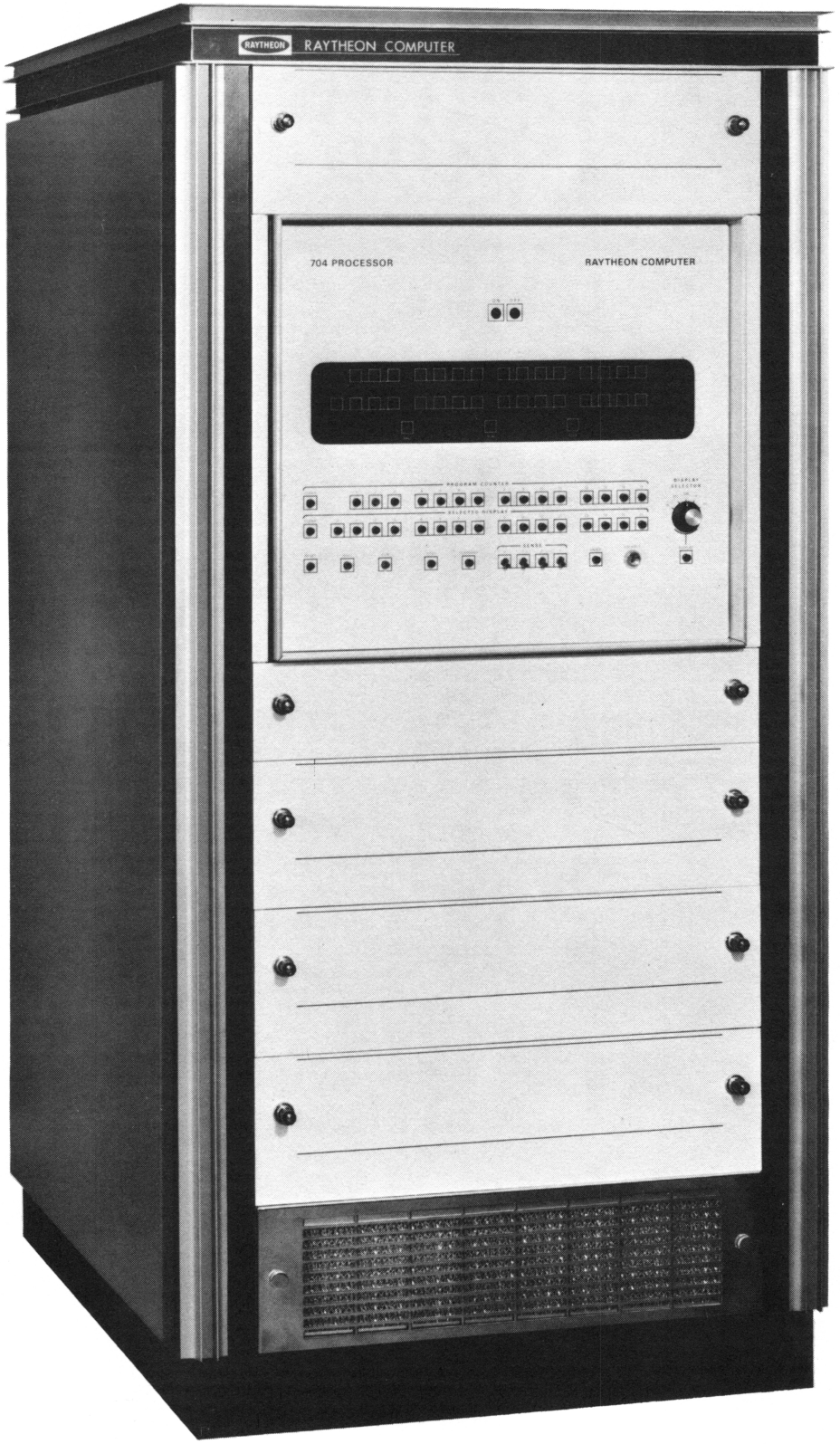

Raytheon 704 Basic Computer System

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Section I

GENERAL DESCRIPTION

1-1. INTRODUCTION

1-2. This manual contains operation and maintenance information for the basic Raytheon 704 Processor and all circuit additions that can be supplied as standard options manufactured by Raytheon Computer, Santa Ana, California.

1-3. The instructions contained in this manual are primarily intended for operators and maintenance personnel and include installation and operation instructions, theory of operation, and maintenance instructions. Detailed logic diagrams, schematic diagrams, and wiring diagrams are grouped at the back of the manual for reference convenience.

1-4. To avoid unnecessary duplication, the computer word formats and the machine instructions are described in the *Raytheon 704 Processor User's Manual*, Bulletin SP-351. The same manual also provides much in the way of system software information. It is assumed that the user of this manual is either familiar with this information or that it is readily available to him, so it is not repeated here.

1-5. Operation and maintenance instructions for standard peripheral equipment that is compatible with the 704 Processor are provided in individual manuals covering the separate devices and their controllers. These related publications are listed under paragraph 1-40.

1-6. DESCRIPTION

1-7. The 704 Processor is a 16-bit general purpose computer with a memory access and machine cycle time of 1 microsecond. Data is handled as binary numbers and is processed in parallel according to the rules of 2's complement arithmetic. The processor may be used as the control element for data acquisition, data processing, and system control.

1-8. The basic 704 Processor consists of a central processor unit (CPU), 4096 words of magnetic core memory, a device controller for a Model ASR 33 or ASR 35 Teletypewriter Set (TTY set not included), and the necessary dc power supplies, all housed in a single equipment cabinet. The teletypewriter set is a separate free-standing unit and contains a low-speed paper tape reader and punch as well as the typewriter keyboard and printer. It is the basic input-output device for the processor.

1-9. All circuits of the basic 704 Processor (excluding the dc power supplies) are mounted on plug-in type printed circuit cards that reduce maintenance down time and increase processor configuration flexibility. For in addition to the basic complement of circuit cards, the 704 Processor cabinet is prewired for plug-in installation of most of the standard option functions and up to 16,384 words of internal memory. The standard options (paragraph 1-15) may be specified at the time of purchase or added later to adapt the CPU to particular applications.

1-10. All operating controls and indicators for the 704 Processor are located on the front panel of the main cabinet. These control and indicators govern the operating mode of the processor and permit display of CPU register and memory location contents as well as manual data entry into CPU registers and memory locations. The functions of all CPU controls and indicators and instructions for their use are given in Section III of this manual.

1-11. The CPU communicates with peripheral devices over a data input-output (DIO) bus. Data is transferred into and out of the CPU accumulator register in 16-bit, parallel words. The number of bits of the data word actually used by a peripheral device depends on the particular device. Addressing permits up to 16 devices to be connected to the DIO bus and controlled, using up to 16 function codes to control each device. Command words and status responses are also transmitted over the DIO bus lines.

1-12. MEMORY EXPANSION OPTIONS

1-13. The magnetic core memory used in the 704 Processor is of modular construction; each module consists of two printed circuit boards installed as a single plug-in assembly that provides 4096 18-bit word storage locations. The basic processor is wired for four of these memory modules (16,384 word locations) within the processor cabinet and is delivered with one memory module installed. Expansion of the memory in 4096-word increments is simply a matter of plugging in one or more additional memory modules.

1-14. Because of space limitations, memories larger than 16,384 words require a separate memory expansion cabinet that contains its own power supplies and the additional 4096-word memory modules over the four in the main cabinet. The memory may be expanded in this way until the address limit of 32,768 word locations is reached. All memory module assemblies are identical and fully interchangeable.

1-15. CENTRAL PROCESSOR UNIT OPTIONS

1-16. The 704 Processor is prewired so that the inclusion or addition of standard CPU options, like memory expansion, can be accomplished simply by plugging in printed circuit card assemblies. In a few cases, minor wiring changes may be necessary. Each standard option fits on a single printed circuit card and can be installed directly within the main cabinet of the processor.

1-17. The standard CPU options available are described briefly below. A detailed discussion of the functions they perform and the theory of operation of their logic is given in Section IV of this manual.

1-18. Hardware Multiply-Divide

1-19. Installation of this option adds two machine instructions, MPY and DIV, to the CPU command repertoire. By using these instructions instead of the lengthy multiply and divide subroutines, the time required for multiplication is reduced from 105 μs to 8 μs and for division from 193 μs to 10 μs. These are special two-word instructions with the second word used to specify the location in memory of the multiplicand or the divisor. The use of a full word to address the multiplicand or divisor allows any location in memory to be addressed without reference to the index register, which is only available to the MPY instruction for address formation.

1-20. Execution of the MPY instruction forms the 31-bit product of two 16-bit numbers, and the DIV instruction forms a 16-bit quotient and 16-bit remainder from dividing a 16-bit divisor into a 31-bit dividend. All operands must be signed, and either positive numbers or 2's complement negative numbers may be used in these operations. The hardware multiply-divide logic computes the correct signs of all resultants and delivers negative resultants in 2's complement form automatically.

1-21. Priority Interrupt Expansion

1-22. The basic 704 Processor is equipped with one level of interrupt service for recognition of devices connected to the DIO bus. All devices share a common interrupt line in the one-level system, so the status of the individual devices must be checked in the interrupt service routine to determine which of the devices is interrupting. This system may be expanded to 8 levels or to 16 levels by installing one or two priority interrupt option circuit cards, respectively.

1-23. In a multi-level priority interrupt system, the peripheral devices are assigned recognition priorities, and where interrupts from two or more devices occur simultaneously (or are waiting to be serviced), the device interrupting on the higher priority level will be serviced first. Interrupts from

specific devices may also be selectively enabled or disabled under program control in expanded interrupt systems. The teletypewriter set, being the slowest I/O device, is normally assigned to the lowest priority level (level 00).

1-24. Manual Interrupt

1-25. The manual interrupt option allows the operator to interrupt data processing by pressing a MANUAL INTERRUPT switch located on the teletypewriter set. At least eight levels of interrupt must be installed to use this option, and the option comes preassigned to priority level 01 (although it is reassignable to any priority level by a simple jumper change). The actual function performed by a manual interrupt is programmable and is written into the interrupt service routine for priority level 01 (or any other level assigned).

1-26. Direct Memory Access

1-27. A direct memory access (DMA) option provides direct communication between high-speed I/O devices (magnetic tape, disc memory, etc) and the memory via a special DMA bus that bypasses the CPU. Up to six devices may share the DMA bus on an assigned priority basis, but only one device has access to the memory for the reading or writing of data at one time. Normal program execution by the CPU is not affected by data transfer on the DMA bus unless both require access to memory at the same time. In this case, the device on the DMA bus is serviced first.

1-28. Those devices connected to the DMA bus must also communicate with the CPU via the DIO bus. They are controlled by function codes supplied over the DIO bus and receive starting location addresses from the same source. Requests for status and status responses from the device controllers are handled much the same way as those from DIO communicating devices.

1-29. Memory Parity Check

1-30. The basic 704 Processor does not check data read from memory for errors. However, a memory parity check option may be installed which generates a parity check bit for each 8-bit byte stored into memory. The state of this bit is such as to maintain odd parity between the byte and its check bit. The two parity bits per word are appended to the data word and are stored with it into memory, accounting for the 18-bit word length of the memory module locations. No overall parity is established for the entire data word.

1-31. When a word is read from memory, whether by the CPU or by a device on the DMA bus, each byte is checked against its parity check bit for odd parity. If a parity error is detected, the processor halts and a machine status indicator lights to show why data processing has stopped.

1-32. Automatic Bootstrap

1-33. (Information not available at this time.)

1-34. Power Failsafe Option

1-35. An optional power failsafe unit may be installed in the processor to protect the contents of memory and to bring program execution to an orderly halt in the event of power failure. If power fails abruptly or the line voltage drops below a preset limit, a one-millisecond power failure interrupt causes the contents of registers and machine status to be stored, the CPU to be halted, and the system to be reset before the dc voltage decreases significantly. Memory access is disabled at the end of the interrupt period to protect the contents of the memory during the time the dc voltages are decaying. When power is restored, computer operation is automatically restarted.

1-36. PERIPHERAL EQUIPMENT

1-37. It is not practical to include here a list of all peripheral equipment available for use with the 704 processor; devices such as card readers, line printers, magnetic tape units, disc memories, etc. The current list is impressive and expanding rapidly as new items are developed. Your Raytheon Computer Sales Representative can supply you with the latest information on this equipment.

1-38. BASIC PROCESSOR CHARACTERISTICS

1-39. Table 1-1 provides the basic design and electrical characteristics of the 704 Processor.

1-40. RELATED PUBLICATIONS

1-41. Operation and maintenance information for peripheral equipment is not covered in this manual. Where a device is manufactured by another firm, the true manufacturer's technical manual is sent with the equipment. Raytheon Computer has prepared additional manuals which describe any modifications to the device made by us and the particulars of its controller. These Raytheon Computer publications are listed below.

Publication No.	Manual Part No.	Title
RC2022	391344	Paper Tape Reader and Punch
RC2023	391345	Magnetic Tape System (DMA, 9-track) 17.5/35, 36, 75 ips — 8 bpi
RC2024	391346	Disc Memory (Mod. 1 Revised)
RC2025	391347	Card Reader and Punch
RC2026	391348	Line Printer
RC2029	393682	Magnetic Tape System (DIO 7- or 9-track) Sync or incremental, density and format options
RC2041	392435	Multiverter Interface
RC2032	392436	Miniverter Interface
RC2033	392437	Buffered Digital Output Channel
RC2034	392438	Buffered Digital Input Channel
RC2035	392804	Time-of-Day Clock
RC2036	392805	Digital-to-Analog Converter
RC2037	392806	Buffered Digital Input/Output Channel
RC2038	392807	Buffered Digital Output Channel
RC2054	394178	Teletype Multiplexer
RC2055	393683	Digital Plotter Controller
RC2070	393877	Magnetic Tape System (DMA, 7-track) 75 ips, 8 bpi

Table 1-1. 704 Processor Characteristics

General	
Number of instructions	74 plus 2 optional
Machine cycle time	1.0 microsecond
Instruction word length	16 bits
Data word length	16 bits (or two 8-bit bytes)
Data number system	Signed fixed-point binary
Arithmetic method	2's complement
Registers	Four addressable registers and one index register
Addressing modes	Direct; indexed local; indexed global
Maximum addressing capacility	32,768 words (15 bits)
Main Memory	
Storage type	Random-access, DRO, magnetic core
Basic memory size	4096 words (one module)
Word length	18 bits (16-bit data word plus 1 byte parity check bits)
Read/restore cycle time	1.0 microsecond
Parity error check	Not standard; byte parity logic available as an option
Expansion capability	
Within CPU cabinet	Two, three, or four modules (to 16,384 words, in 4096-word increments)
Outside CPU cabinet	Up to four additional 4096-word modules (to 32,868-word address limit)
Data Input-Output (DIO) Interface	
Device addressing	Up to 16 different devices and 16 different functions for each device over eight address lines.
Data transfer	Separate, full-word (16-bit parallel) data input and output lines
Basic interrupt system	One level automatic interrupt
Interrupt expansion capability	Eight or 16 levels of priority interrupt
Direct memory access (DMA) interface	
Device channels	Up to 6 different devices serviced on an assignable priority basis
Data Transfer	Separate, full-word (16-bit parallel) data input and output lines

Table 1-1. 704 Processor Characteristics (Cont)

Direct memory access (DMA) interface (Cont)	
Memory addressing	From device DMA controller over 15 parallel address lines
Environmental limits	
Operating temperature range	0 to 40 degrees C.
Storage temperature range	-20 to 65 degrees C.
Maximum humidity	90 percent, relative, without condensation
Physical Properties	
Overall dimensions	15-3/4 inches high by 17-1/2 inches wide by 23-1/2 inches deep (allow 4 inches additional depth for rear panel connectors)
Total weight	75 pounds, approximately
Method of cooling	Two exhaust fans
Power requirements	110 — 120 volts ac, 50 — 60 Hz, 9 amperes maximum

Section II
INSTALLATION

2-1. GENERAL

2-2. This section contains instructions for unpacking, installation, and initial checkout of the 704 Processor.

2-3. UNPACKING AND INSPECTION

2-4. The 704 Processor is shippped fully assembled in a single shipping container. Ancillary and peripheral equipment, such as expansion cabinets and the teletypewriter set, are shipped in their own separate containers. Proceed as follows:

> **Note**
>
> If shipping damage is uncovered while unpacking the equipment, proceed no further and save all packing material. Notify the transportation agent and your Raytheon Computer sales representative immediately.

a. Open top of shipping container carefully. Do not use any tools or procedures that might damage the contents.

b. Remove upper foam cushion and lift out unit. Do not discard any packing material until all items listed on packing slip are accounted for and have been inspected.

c. Open hinged front panel by inserting lip of door opening tool (part no. 545241) behind left-hand edge of panel about 2 inches from bottom and pulling straight forward to release latch.

d. Remove top access cover by pressing with the fingers of both hands, palms upward, along the front edge of panel from inside cabinet to release front snap-latch strips. Grasp front edge of panel from outside and slowly lift up and to the rear, being careful not to bend cover while removing it.

e. Remove all packing material (foam padding, tape, etc) found inside unit. Also remove shipping clamp (aluminum bar with two hooked rods that keep circuit card guide rails from springing) by loosening two nuts, disengaging rods, and withdrawing from the top. Inspect interior for loose or damaged circuit cards. Also check that connectors attached to front of some circuit cards are firmly seated, wiring is undamaged, and printed wiring board behind front panel is screwed down tightly.

f. Check for a shipping rod (piece of loose welding rod) running horizontally through holes in lower rear corners of all plug-in circuit cards. If rod is present, perform steps that follow. Otherwise, close door and proceed to installation instructions, paragraph 2-5.

g. Remove left-hand side access cover (as viewed from front) by pressing out with the fingers from inside until several of nylon snap-latches have been separated. Panel can now be lifted off with a careful prying motion from outside.

> **Note**
>
> As a point of interest, right-hand side access cover also comes off in the same manner for access to the power supply.

h. Remove shipping rod by pulling it straight out from the left-hand side. It is of no further use and may be discarded.

j. Replace side and top access covers (align and engage snap-latch strips at one edge first and work across face of panel to opposite edge, pressing firmly over each fastener to engage it).

Note

Two side access panels are not interchangeable. When both covers have been removed, replace them so that the louvers are nearer the front of the cabinet.

k. Close front panel door, pressing lower left-hand corner to engage snap fastener.

2-5. INSTALLATION

2-6. There are no special requirements in selecting a suitable location for the 704 Processor other than the usual installation site considerations (ambient temperature and humidity, availability of power, protection of interconnecting cables, etc). Where possible, the unit should be located well away from any major bulkhead that might restrict airflow through the unit. Cooling air is drawn into the unit through the side louvers and forced directly out the back. Figure 2-1 gives pertinent installation dimensions and other data.

a. Locate 704 Processor so that 80-inch power cable will reach a suitable primary power outlet (115 volts, 60 Hz, single phase, 9 amperes). Do not plug in power cable yet.

b. If applicable, locate Teletype model ASR 33 or ASR 35 teletypewriter set adjacent to processor and interconnect the two units using cable assembly 545218. Cable plugs into processor rear panel TTY connector. Also plug in teletypewriter set power cord, but leave set turned off.

c. Install DIO terminator plug (part no. 279767) into DIO connector (either one if there are two) on processor rear panel.

d. If applicable, connect other DIO bus device controllers to one another and to vacant DIO connector on processor rear panel. Use DIO cable assemblies (part no. 279558) of the required lengths. Total cable run from processor to furthest controller must not exceed 50 feet under any condition and should be as short as possible. See figure 2-2 for DIO bus interconnections.

Note

All ends of the DIO bus must be terminated by inserting a DIO terminator plug 279767 into vacant DIO connectors. See figure 2-2.

e. Check all DIO controllers for device address number and priority interrupt level assignments. Change if necessary (instructions given in each device controller manual). Assignments must be compatible with number of interrupt levels in system (one, level 00, unless noted otherwise on options nameplate) and with interrupt service software.

f. If processor has DMA logic installed (check options listed on nameplate), install DMA terminator plug (part no. 279768) into either DMA connector.

g. If applicable, connect DMA bus device controllers to one another, to the DIO bus controllers (they share the DIO bus for selection, control, and status), and to vacant DMA connector on processor rear panel. Use DMA cable assemblies (part no. 279557) of the required lengths. Total length of cable run must not exceed 24 feet. See figure 2-3 for DMA bus interconnection scheme.

Note

A DMA terminator plug 279768 must be installed in the unused DMA connector on the far-end DMA controller. See figure 2-3.

h. Check all DMA controllers for request/acknowledge channel assignment. Change if necessary (instructions given in each device controller manual).

j. If system includes memory- or logic-expansion

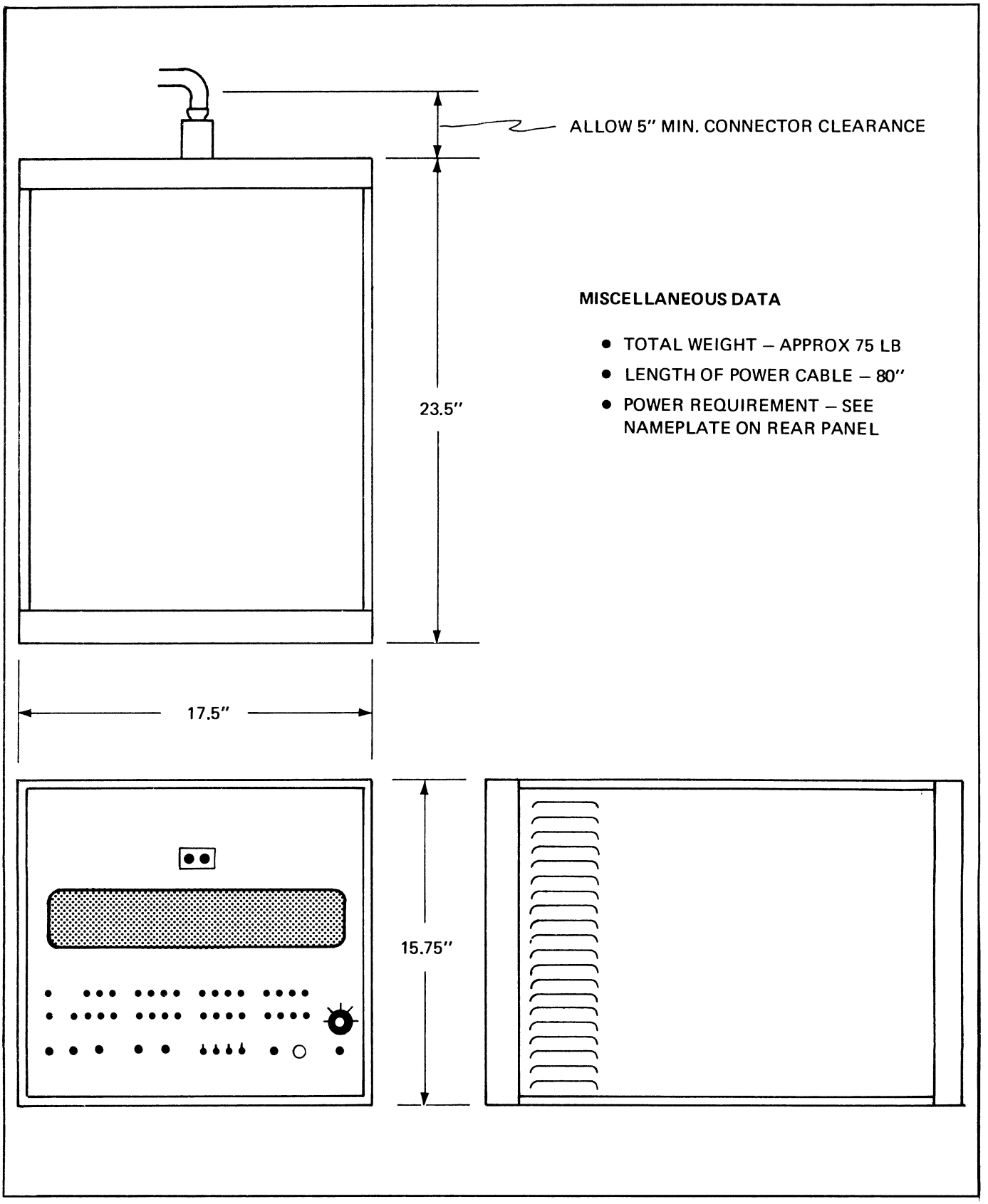


Figure 2-1. 704 Processor Installation Dimensions

cabinet, make necessary cable connections. Refer to technical manual for memory expansion unit or to special system documentation for inter-unit cabling required.

k. Plug in processor power cable. Processor should remain off (blowers not operating and all front panel lights out).

Note

If processor RUN or HALT indicator lights when power plug is connected, the unit probably has power failsafe logic (see list of options on nameplate) or the power supply is connected for power ON-OFF switch override. To disable this override, refer to instructions in Section V.

2-7. CHECKOUT

2-8. Before operating the 704 Processor as an operational system, the equipment and the installation should be checked out as follows:

a. Turn on processor by pressing front panel ON switch. Check that both blowers are delivering air rearward. Also check for automatic power-on reset (i.e., only HALT indicator should be lit). Press RESET switch if this is not the case.

b. Run a general check of unit by manually entering and displaying data to and from all accessible registers and a few memory locations. See Section III for manual operating instructions.

c. Manually enter bootstrap load routine (refer to Section III) and load 704 Sensor diagnostic programs or some other acceptance test program. All peripheral devices used in these tests must, of course, be plugged in and turned on. Run test programs until satisfied that entire system is operating trouble free.

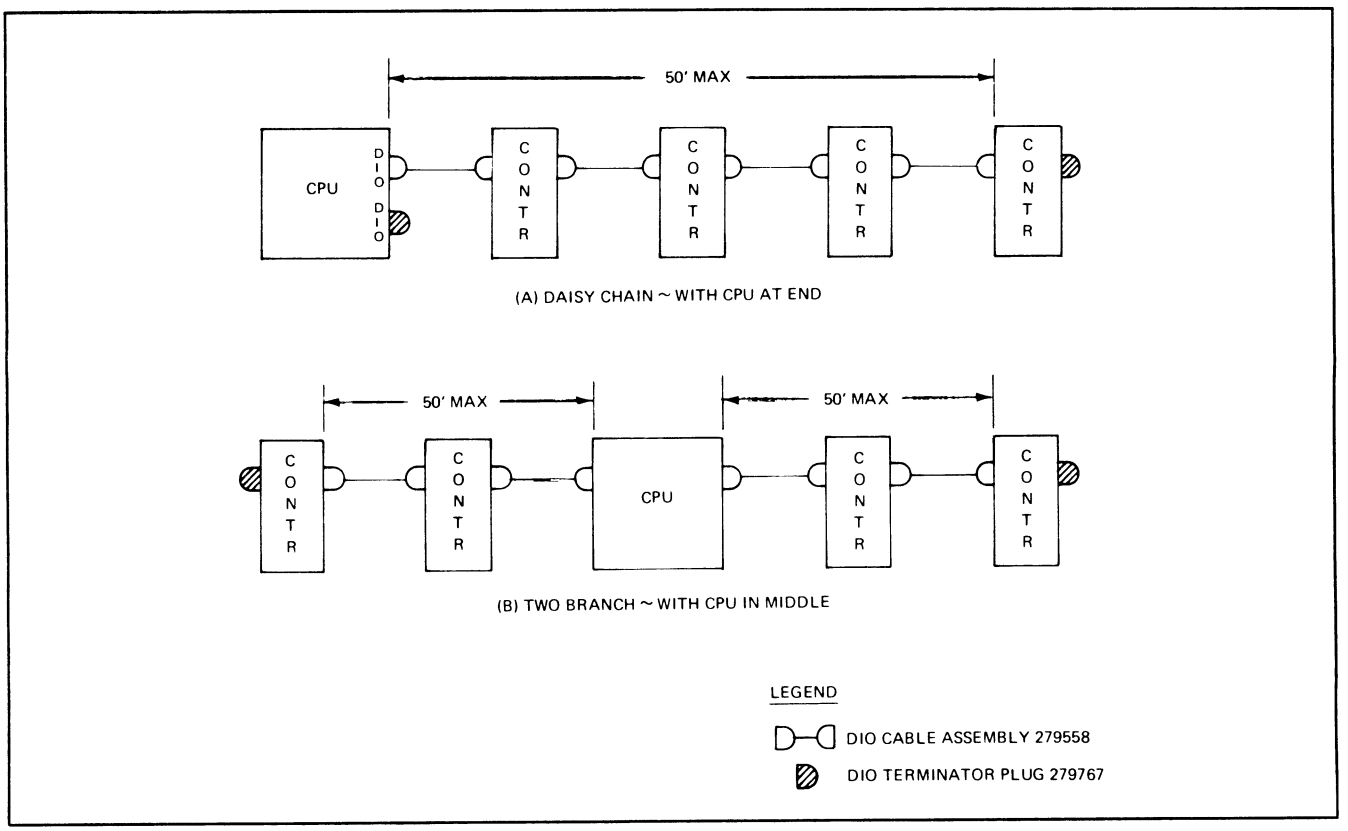


Figure 2-2. DIO Bus Interconnection Schemes

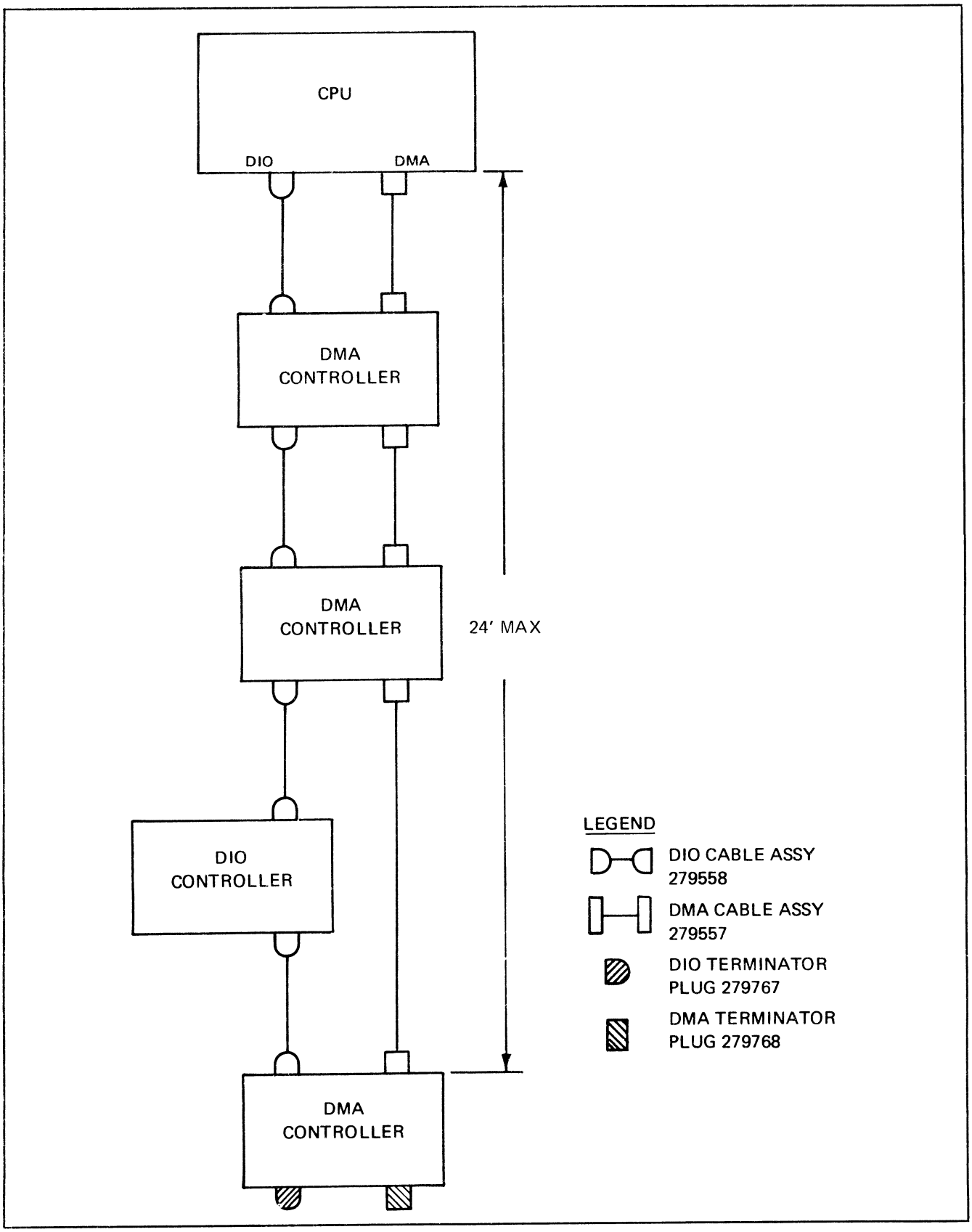


Figure 2-3. DMA Bus Interconnection Scheme

Section III

OPERATING INSTRUCTIONS

3-1. GENERAL

3-2. This section contains a functional description of the 704 Processor operating controls and indicators and instructions for loading and executing computer programs manually. Instructions for use of the 704 Programming Systems are contained in the system software manuals. Instructions for operating various peripheral devices which may be included in the system will be found in the operation and maintenance manuals for the equipment, if standard; or in your system manual, if the equipment is of special design.

3-3. CONTROLS AND INDICATORS

3-4. All central processor unit (CPU) controls and indicators are located on the front panel of the main chassis. Their locations are shown in figure 3-1 and the function of each is described in table 3-1.

3-5. The teletypewriter set (Model ASR 33 or ASR 35) supplied with the 704 Processor is modified for use in this application. The normal teletypewriter set controls and indicators are described in the manual supplied with the set. The modifications to the sets are described in Section IV of this manual.

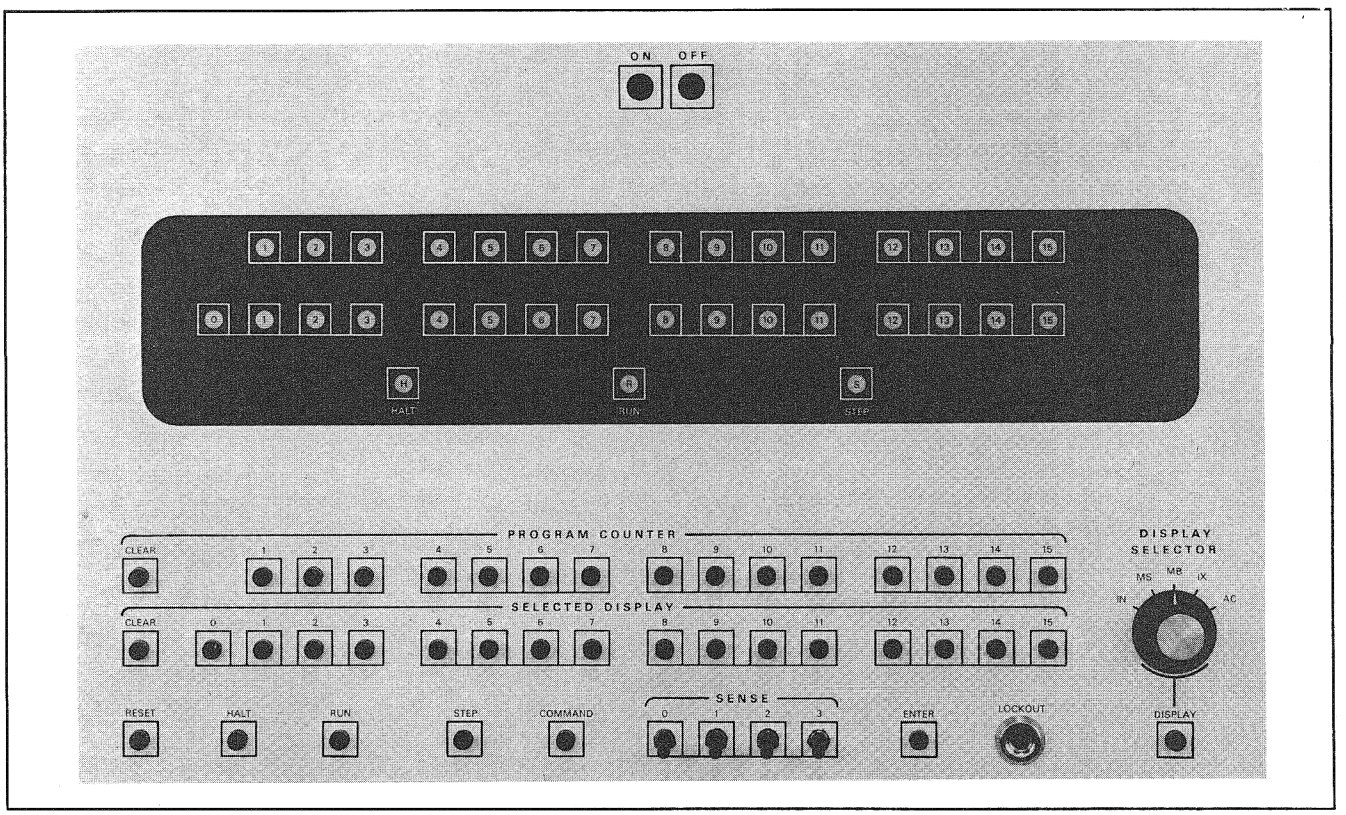


Figure 3-1. 704 Processor Control Panel

Table 3-1. 704 Processor Controls and Indicators

Name	Function
ON-OFF Switches	Turn the processor power supply on and off and reset the processor system. (**Note:** The only indication that the processor is turned on is that at least one control panel indicator will be lit and the blowers will be running.)
Indicators 1 thru 15 (top row)	Display the contents of the program counter register whenever the processor is halted or in the single-step mode. Ones occupy those bit positions that are lit.
Indicators 0 thru 15 (bottom row)	Display the contents of any one of four registers or machine status, depending upon the position of the DISPLAY SELECTOR switch. Machine status bit assignments (displayed when the switch is in the MS position) are: Bits 00 — 04 Extension register contents Bit 05 ADFNEG flip-flop state Bit 06 ADFEQL flip-flop state Bit 07 ADFOVF flip-flop state Bit 08 CCFGLB flip-flop state Bit 13 Memory Parity Error
HALT-RUN-STEP Indicators	One of these lamps will be lit at all times that the processor is turned on, indicating whether it is currently halted, running, or in the single-step mode.
PROGRAM COUNTER Section	
CLEAR Switch	Clears all bits of the program counter register to the 0 state.
Bit Switches 1 thru 15	Each switch sets its corresponding bit in the program counter register to the 1 state. Used to enter a location address for manual access to memory.
SELECTED DISPLAY Section	
CLEAR Switch	Clears all bits of the register selected by the DISPLAY SELECTOR switch (operative in positions MB, IX, and AC only).
Bit Switches 0 thru 15	Each switch sets its corresponding bit in the register selected for display by the DISPLAY SELECTOR switch (operative in positions MB, IX, and AC only). Used for manual entry of data into the register.

Table 3-1. 704 Processor Controls and Indicators (Cont)

Name	Function
DISPLAY SELECTOR Switch	Selects machine status or a register for display or manual entry via the SELECTED DISPLAY indicators and switches, as follows: **IN position** — Display instruction register contents (bits 0 thru 7) and the state of the sequence counter in hexadecimal form (bits 12 thru 15). **MS position** — Display machine status (See functional description of indicators 0 thru 15 for bit assignments.) **MB position** — Display the contents of the memory buffer register, enable the SELECTED DISPLAY switches for entry into the register, and enable the ENTER and DISPLAY switches for manual access to memory. **IX position** — Display the contents of the index register and enable the switches for manual entry into the index register. **AC position** — Display the contents of the accumulator register and enable the switches for manual entry into the accumulator register.
RESET Switch	Resets the processor registers, control logic, and peripheral device controllers in the system. Pressing this switch also returns the processor to the halted state from the single-step mode.
HALT Switch	Stops data processing, if the processor is running, or terminates single-step operations.
RUN Switch	Starts data processing.
Single STEP Switch	First actuation of this switch places halted processor into the single step mode. Subsequent actuations cause the processor to execute one machine cycle of the program each time the switch is pressed. (**Note:** The HALT or RESET switch must be pressed to leave the single-step mode.)
Single COMMAND Switch	Causes the halted processor to execute one complete machine instruction and halt again each time the switch is pressed.
SENSE Switches 0 thru 3	Permit conditional skip program modification by testing the state of any one of these presettable toggle switches. The skip function is enabled when a switch is down (false).

Table 3-1. 704 Processor Controls and Indicators (Cont)

Name	Function
ENTER Switch	Writes the contents of the memory buffer register into the memory location addressed by the program count and increments the program count by one. (Operative only when the DISPLAY SELECTOR switch is in the MB position.)
LOCKOUT Switch	Disables all control panel switches except the four SENSE switches, preventing them from affecting the current state of the processor. The front panel switches are "unlocked" when the key is turned to the counterclockwise position.
DISPLAY Switch	Reads the contents of the memory location addressed by the program count, loads it into the memory buffer register for display, and increments the program count by one. (Operative only when the DISPLAY SELECTOR switch is in the MB position.)

3-6. Two indicators are added to both the Model 33 and Model 35 sets. These indicators indicate the input mode selected in the teletypewriter set controller. The KBD indicator lights when the keyboard mode is selected, and the PTR indicator lights when the paper tape reader mode is selected. Both indicators are out when the disconnect or print/punch modes are selected.

3-7. When the manual interrupt option is installed in the processor system, a MANUAL INTERRUPT switch is also added to the teletypewriter set keyboard. Pressing this switch sends an interrupt to the CPU priority interrupt system.

3-8. The MODE switch on the Model 35 set is altered mechanically to reduce the number of switch positions from five to three, and the wiring of the switch is changed so that it no longer functions as it did in the unmodified set. The three switch positions used are reidentified as PRINT, PRINT & PUNCH, and PUNCH. Data sent to the set will be printed only, printed and punched simultaneously, or punched only, depending on the setting of the MODE switch.

3-9. Power On and Off Procedure

3-10. The 704 Processor is turned on and off by operating the front panel ON and OFF switches. Neither of these switches is disabled by the key-operated LOCKOUT switch. Pressing the ON switch turns on the processor by activating the dc power supply. The equipment blowers should begin operating and at least one front panel indicator (the HALT indicator) should light, indicating that the processor is turned on. But if power failsafe circuits are installed, a run command will be sent to the CPU at the end of the power-on sequence to start processing immediately (RUN indicator will be lit) from memory word location zero. Quite often this location will contain a halt instruction.

3-11. If the power failsafe circuits are not installed, make sure that the processor is halted before turning off power, otherwise processing errors may occur. The power failsafe circuits send a power interrupt to the CPU when power is turned off to ensure that the processor is halted before the dc voltages start to decrease. Power is turned off by pressing the OFF switch.

3-12. Failure of the processor to turn off when the OFF switch is pressed means that the power supply has been internally jumpered to bypass the switch. This is the most common method of protecting the processing operation. If the processor is being operated in this way, it is turned on and off directly at the power line plug.

3-13. MANUAL DATA DISPLAY AND ENTRY

3-14. Quite often, it is desirable to be able to observe the contents of a register or memory location or to "go in" and change the data during manual operations such as program debugging or machine troubleshooting. Within certain limits, this is possible, using the front panel controls of the 704 Processor.

3-15. The contents of the program counter register and one of four switch-selectable CPU registers (or machine status) are displayed on the front panel continuously, but usually they can only be read whenever the processor is halted or in the single-step mode. The two rows of indicators correspond positionally to the two rows of pushbutton switches below them; that is, the top row of indicators (1 thru 15) are for the PROGRAM COUNTER register, as are the top row of switches, while the bottom row of indicators (0 thru 15) are for the SELECTED DISPLAY data, the same as the bottom row of switches. Indicators are arranged in groups of four to aid the operator in translating the binary display into its hexadecimal equivalent, where this is appropriate.

3-16. A bit display indicator is lit when the corresponding register flip-flop output is a 1 (or set). If it is out, the flip-flop contains a 0 (or is reset). The pushbutton switches may be used to enter data into the program counter register, the memory buffer register, the index register, and the accumulator register, as described in the paragraphs that follow.

3-17. Program Counter Register

3-18. The top row of indicators display the contents of the program counter register at all times. Reading this display when the processor is halted will indicate the location of the next instruction that will be fetched for execution when run or single-step operation is resumed. If it is desirable to jump to an instruction other than the next instruction in sequence, this can be done by manually entering in the address of the desired instruction. Also, the addresses for manual memory access (display or enter) operations must be entered in the same way. The procedure for entering data into the program counter register is as follows:

a. Unlock the control panel by inserting key into LOCKOUT switch and turning counterclockwise, if necessary.

b. If HALT indicator is not lit, press HALT switch. HALT indicator should light.

c. To change any program counter bit from a 1 to a 0, press PROGRAM COUNTER section CLEAR switch, resetting the entire register. All top row indicators should go out.

d. After clearing the register, or if no bits need changing from a 1 to a 0, enter the necessary 1's in the appropriate bit positions by pressing the corresponding PROGRAM COUNTER switches. Top row indicators should light accordingly.

3-19. Selected Display

3-20. The bottom row of indicators display various bits of machine status data or the contents of a selectable register, as determined by the setting of the DISPLAY SELECTOR switch. This data is displayed continuously, but it cannot be read unless the processor is halted or in single-step mode. The DISPLAY SELECTOR switch may be changed from one position to another at any time. No other action is required to initiate the display.

3-21. The machine status word (data displayed when the DISPLAY SELECTOR switch is set to MS) consists of the data in the extension register displayed as bits 0 through 4; the states of the adder negative flip-flop ADFNEG, the adder equal flip-flop ADFEQL, and the adder overflow flip-flop ADFOVF displayed as bits 5, 6, and 7, respectively; the state of the global control

flip-flop CCFGLB displayed as bit 8; and the "halt due to memory parity error" condition indicated whenever the bit 13 indicator is lit.

3-22. The other four positions of the DISPLAY SELECTOR switch (IN, MB, IX, and AC) permit the display of the contents of the instruction register, the memory buffer register, the index register, and the accumulator, respectively. In the case of instruction register display (IN position of the switch), the content of the instruction register will be seen displayed by indicators 0 through 7 and the state of the sequence counter will be displayed in binary form by indicators 12 through 15. For example, phase 7 will be displayed as 0111, phase B as 1011, phase D as 1101, etc.

3-23. Entering of data manually into a register is permitted only into the memory buffer register, the index register, and the accumulator register. Consequently, the SELECTED DISPLAY push-button switches are enabled only when the DISPLAY SELECTOR switch is in the MB, IX, or AC position. These switches may be used for entering data only when the processor is halted. The procedure is as follows:

a. Unlock the control panel by inserting key into LOCKOUT switch and turning counterclockwise, if necessary.

b. If HALT indicator is not lit, press HALT switch. HALT indicator should light.

c. Set DISPLAY SELECTOR switch to select register to be entered (MB, IX, or AC positions only).

d. To change any register bit displayed from a 1 to a 0, press SELECTED DISPLAY section CLEAR switch, resetting the entire register. All bottom row indicators should go out.

e. After clearing the register, or if no bits need changing from a 1 to a 0, enter the necessary 1's in the appropriate bit positions by pressing the corresponding SELECTED DISPLAY switches. Bottom row indicators should light accordingly.

3-24. Memory Display and Entry

3-25. The operator can read and display the contents of any memory location or enter and write new data into any memory location by using the DISPLAY and ENTER switches at the lower right-hand corner of the control panel. The DISPLAY switch is used to read a word from the memory location given in the program counter register and load it into the memory buffer register for display by the bottom row of indicators. The ENTER switch is used to write a word from the memory buffer register into the memory location given in the program counter register. Pressing either switch automatically increments the program count by one so that a sequence of memory locations can be accessed merely by repeatedly pressing the switch. The DISPLAY SELECTOR switch must be set to the MB position and the processor must be halted before the DISPLAY and ENTER switches are enabled.

3-26. The procedure for displaying the contents of a memory location or series of memory locations is as follows:

a. Unlock the control panel, if necessary. If HALT indicator is not lit, press HALT switch. HALT indicator should light.

b. Set DISPLAY SELECTOR switch to MB.

c. Manually enter memory location address (or first address of a series) into program counter register. See paragraph 3-17 for procedure.

d. Press DISPLAY switch once and release. The data displayed by the bottom row of indicators is the content of the memory location addressed. If the contents of a series of memory locations are to be read, press DISPLAY switch again and read the data displayed by the bottom row indicators for each location.

3-27. The procedure for entering data into a memory location or series of memory locations is as follows:

a. Unlock the control panel, if necessary. If HALT indicator is not lit, press HALT switch. HALT indicator should light.

b. Set DISPLAY SELECTOR switch to MB.

c. Manually enter memory location address (or first address of a series) into program counter register. See paragraph 3-17 for procedure.

d. Using SELECTED DISPLAY pushbutton switches, manually enter data word to be written into the memory buffer register.

e. Press ENTER switch once. Data word in memory buffer register will be written into memory location addressed, and program count will be incremented by one, addressing ext location in sequence.

f. If a number of data words are to be written into sequential memory locations, enter next data word into memory buffer register and press ENTER switch once. Repeat until all words have been entered.

3-28. PROGRAM LOADING

3-29. Initial program loading into the 704 Processor can be initiated in any one of five ways: (1) if short, it can be entered manually via the front panel switches for execution; (2) it can be entered via the DIO bus, using a manually entered bootstrap loader; (3) it can be entered via the DIO bus, using an optional hardware bootstrap loader; it can be entered via the DMA or DIO bus, using a DMA magnetic tape or DMA disc memory controller entered loader; or (5) it can be entered from a number of sources under control of a resident X-RAY executive program.

3-30. Absolute or relocatable object programs may be loaded under control of the X-RAY executive program. This program is covered in the system software manuals. Absolute programs may also be loaded manually, by paper tape bootstrap, by automatic bootstrap hardware, or via the direct memory access bus, as previously noted. These operations are covered in paragraphs 3-35 through 3-43.

3-31. Manual Program Entry

3-32. The front panel controls may be used to load programs manually into memory. These are generally used only to load simple programs, such as the bootstrap programs given in paragraph 3-35, because of the slowness of the process. However, they may be used to load programs of any length desired. Use of the front panel switches and indicators to display and enter data is described in paragraph 3-13.

3-33. The procedure for manually loading a program is as follows:

a. Press computer RESET switch.

b. Set program counter register to starting location of program, if other than location 0.

c. Set DISPLAY SELECTOR switch to MB position.

d. Enter first word of program into memory buffer register.

e. Press ENTER switch. Word will be entered into memory location addressed by program counter register and program count will be incremented by one.

f. Clear memory buffer register, enter next word into register, and press ENTER switch. Repeat until entire program is loaded.

g. Reenter program starting location into program counter register.

3-34. After the program is loaded, accuracy can be verified by pressing the DISPLAY switch and comparing the display contents of the location with the program listing. The program counter register is incremented to the next location each time the DISPLAY switch is pressed, and each entry will be displayed in turn.

3-35. Paper Tape Bootstrap Program Loading

3-36. Absolute programs on punched paper tape may be loaded by means of a simple, manually

entered bootstrap program. The program may be loaded from the paper tape reader of the teletypewriter set or from a high-speed paper tape reader if one is included in the system.

3-37. The SENSOR diagnostic programs must be loaded with a paper tape bootstrap program; the X-RAY executive program cannot be used for this purpose. However, a special SENSOR bootstrap program, which in itself is a diagnostic program, is used to load the SENSOR diagnostic programs. This bootstrap program and its use are described in the 704 Sensor Diagnostic Manual.

3-38. The bootstrap programs for the two paper tape readers are similar, but the device addresses of the readers are different. This requires only a change in the F1 field of two instructions: the second (DOT) and the fourth (DIN). However, the teletypewriter set is always assigned to interrupt level 0, while the high-speed reader may be assigned to level 0 or a different level in systems with more than one interrupt level. If the high-speed reader is not assigned to level 0, the locations where the bootstrap program is entered will be different, and several instructions must be altered to reflect the correct interrupt level.

3-39. The specific bootstrap program for the teletypewriter set paper tape reader is given in table 3-2. A more general bootstrap program for the high-speed paper tape reader that applies to any interrupt level is given in table 3-3. In this program, the interrupt level is represented by the letter "n" and it is necessary to evaluate the expressions for the particular value of n and to insert the result into the locations and instruction fields. (If n = 0, the resulting program is the same as the program given in table 3-2, except for the differences in device addresses.)

3-40. Use of the bootstrap programs to load programs from paper tape is the same for both readers with one exception. The DOT instruction starts the high-speed reader but only selects the paper tape reader mode in the teletypewriter set controller. The teletypewriter set reader must be started manually after the processor RUN switch is pressed.

3-41. The procedure for loading a program by means of the paper tape bootstrap program is as follows:

a. Press processor RESET switch.

b. Enter applicable paper tape bootstrap program (table 3-2 or 3-3) manually (paragraph 3-31).

c. Press processor RESET switch.

d. Set index register (paragraph 3-19) to the byte origin of the program minus 12 (C_{16}) bytes. The byte origin is twice the word origin.

> **Note**
>
> The first 12 characters on standard program tapes contain information that is used by the X-RAY executive program, but not by the bootstrap program. Setting the index register to 12 bytes less the program origin compensates for these leading characters and places the first character of the program into the correct byte location.

e. Load tape into paper tape reader.

f. Press processor RUN switch. If the high-speed reader is being used, the reader will be started, and the program counter will be incremented as the program is loaded. If the teletypewriter set paper tape reader is being used, it is necessary to move the reader control lever to the START position (after pressing the processor RUN switch) to start the reader.

g. When the program has been loaded, press the processor HALT and RESET switches.

h. If the teletypewriter set paper tape reader was used, move control lever to STOP position.

3-42. Hardware Bootstrap Program Loading

3-43. (Information is not available at this time.)

Table 3-2. Teletypewriter Set Paper Tape Reader Bootstrap Program

Location	Contents	Label	Symbolic	Comments
0	0020		ENB 0	Enable interrupt 0
1	8004		LDW SERV	Interrupt service address
2	03E9		DOT E, 9	Select PTR mode
3	1003		JMP $	Wait for interrupt
4	02ED	SERV	DIN E,D	Input frame
5	0800	TEST	SAZ	Not all 0's
6	0401		IXS 1	Yes, increment IXR
7	0010		INR 0	No, restore interrupt 0
8	0638		LLB X'38'	Load STB*0 code
9	300A		STB/TEST	Change TEST to STB*0
A	0010		INR 0	Restore interrupt 0

Table 3-3. High-Speed Paper Tape Reader Bootstrap Program

Location	Contents	Label	Symbolic	Comments
4n +0	002n		ENB n	Enable interrupt n
4n + 1	800(4n + 4)		LDW SERV	Interrupt service address
4n + 2	03D9		DOT D, 9	Start tape
4n + 3	100(4n + 3)		JMP $	Wait for interrupt
4n + 4	02DD	SERV	DIN D,D	Input frame
4n + 5	0800	TEST	SAZ	Not all 0's
4n + 6	0401		IXS 1	Yes, increment IXR
4n + 7	001n		INR n	No, restore interrupt n
4n + 8	0638		LLB X'38'	Load STB*0 code
4n + 9	300(8n + A)		STB/TEST	Change TEST to STB*0
4n + A	001n		INR n	Restore interrupt n

Note: n = interrupt level (0 — 15) of high-speed paper tape reader.

3-44. Direct Program Loading

3-45. Programs may be loaded directly into memory from magnetic tape or disc storage via the direct memory access (DMA) bus. The word origin of the program is set into the device controller, and program loading is initiated by pressing a LOAD switch.

3-46. The program is loaded automatically and, except for using the memory access logic, is completely independent of the CPU. No commands or status are exchanged on the data input-output (DIO) bus, and no interrupts are involved.

3-47. Operating instructions for direct program loading via the DMA bus are contained in the manuals covering the controllers that can perform this operation.

3-48. PROGRAM EXECUTION

3-49. Programs can be executed in any one of three modes: run, single command, and single step. Further, the program can be modified by testing any of four SENSE switches on the front control panel or an external sense line (EXSENS-) which is part of the DIO bus. Use of the SENSE switches and the external sense line is a function of the individual program and is covered in the program description and operating procedures. The three operating modes are discussed in the paragraphs that follow.

3-50. Run Mode

3-51. In the run mode, the program is executed at normal processing rates until a program halt occurs or the HALT switch is pressed. Execution of the program may be interrupted by devices on the DIO and DMA buses but will be resumed when the interrupt or direct memory access operation is completed. The initial conditions that must be set up before the program is executed are given in the program description. The procedure for executing a program in the run mode is as follows:

a. After program is loaded (paragraph 3-28), press processor HALT and RESET switches.

b. Enter data input index and accumulator registers (paragraph 3-19) if called for in program description.

c. Enter data into memory locations (paragraph 3-24) if called for in program description.

d. Enter address of first program instruction into program counter register (paragraph 3-17).

e. Set SENSE switches as specified in program description.

f. Prepare peripheral equipment as specified in program description.

g. Press processor RUN switch.

3-52. Single-Command Mode

3-53. In the single-command mode, one complete program instruction is executed and the machine halts each time the COMMAND switch is pressed, regardless of the number of machine cycles required to execute the instruction. This mode is normally used for program debugging and as a maintenance aid when it is desired to observe the execution of complete instructions individually.

3-54. The processor enters the single-command mode from the halt state each time the COMMAND switch is pressed and returns to the halt state after fetching and executing one instruction. Normal program execution can be resumed at any time by simply pressing the RUN switch.

3-55. Single-Step Mode

3-56. In the single-step mode, one instruction phase is executed each time the STEP switch is pressed. This mode is normally used as a maintenance aid when it is desired to observe the progression from phase to phase of instructions and the execution of each phase.

3-57. The single-step mode must be entered from the halt state. The first time the STEP switch is pressed a single-step flip-flop is set and the

processor advances from the halt state to the instruction fetch phase (instruction phases are discussed in Section IV.) The instruction is fetched from memory but is not executed. The next operation of the switch causes the operations performed by the instruction during the fetch phase to be executed after which the processor advances to the next phase of the instruction and stops before executing it. Pressing the switch again executes this next phase. After the last phase of the instruction is executed, execution of the next instruction is started the next time that the STEP switch is pressed. The processor does not return to the halt state at the end of each instruction.

3-58. The single-step mode can only be terminated by pressing the processor HALT switch (or by a system reset). This resets the single-step mode flip-flop and allows complete instructions to be executed in the single-command mode or normal program execution in the run mode. If the processor is not in the halt state when the HALT switch is pressed, the remaining phases of the instruction being executed are completed without stopping, and the computer returns to the halt state.

Section IV
THEORY OF OPERATION

4-1. GENERAL

4-2. This section contains a discussion of the theory of operation of the 704 Processor at the block diagram and logic diagram levels. The logic diagrams referred to in text are grouped in Section VI for convenience of reference.

4-3. Insofar as possible, the text is arranged so that subjects are discussed before a knowledge of one subject is required to understand another subject. However, this logical progression from subject to subject cannot always be maintained because of the complex interrelationships between the elements of any digital computer. Where it is necessary to introduce into the discussion a subject that has not previously been covered, cross-references to the paragraphs where the subject is discussed are given. Cross-references are also used to refer to subjects previously discussed to avoid repetition.

4-4. References to the logic diagrams are by drawing number. In order to identify the specific logic elements that are being discussed on the diagrams, the inputs that perform a particular function are identified in parenthesis in the discussion. For example, several gates may be OR'ed to produce a given signal. When discussing a given operation, one of these gates is used to generate the output signal. The inputs to that gate, which represent the conditions that must be true for this particular operation, are included in parenthesis in the description.

4-5. The central processor unit (CPU) of the 704 Processor may contain a multiply-divide option that permits the direct multiplication or division of two numbers by executing a single instruction rather than a multi-instruction multiply or divide routine. The logic for this option is contained on a separate printed wiring board assembly installed in the main cabinet with the CPU logic. In most cases, the multiply-divide logic represent additions to the instruction decoder, additions to the sequence counter, additions to the index register input gates, etc. All of the multiply-divide logic and its effect on other functions of the CPU is discussed separately in the description of the multiply-divide option (paragraph 4-280).

4-6. Word formats, instruction formats and definitions, etc. applicable to the 704 Processor are covered in the *704 User's Manual*, Bulletin SP-351; and a knowledge of the contents of this manual is assumed. Information given in the reference manual is not repeated here except as necessary for clarity or completeness of an explanation.

4-7. BASIC COMPUTER CONFIGURATION (Figure 4-1)

4-8. A basic 704 Processor is defined as the CPU without logic for the direct multiply-divide function; timing and control logic with one channel of priority interrupt control; a teletypewriter set controller; and a 4096- to 16,384-word core memory without parity check or the direct memory access (DMA) feature. By definition, the CPU consists of a 16-bit two's-complement adder and the following data registers:

16-bit Accumulator (ACR)
5-bit Memory Address Extension Register (EXR)
8-bit Instruction Register (INR)
16-bit Index Register (IXR)
15-bit Memory Address Register (MAR)
16-bit Memory Buffer Register (MBR)
15-bit Program Counter Register (PCR)

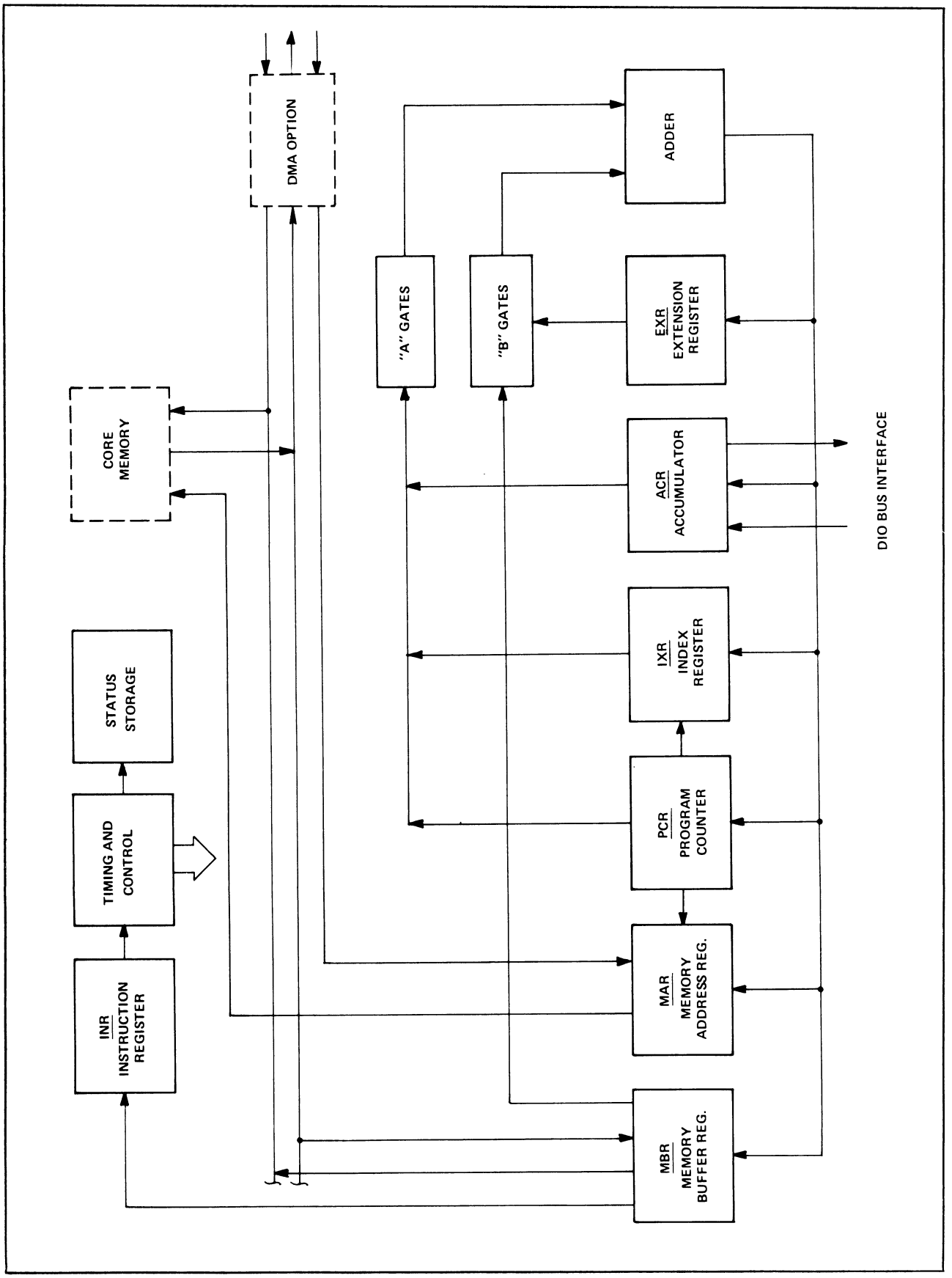


Figure 4-1. Basic Central Processor Data Flow Diagram

A 4-bit iteration counter (ICR) and five 1-bit status storage registers (not shown in the block diagram) complete the CPU. The status storage registers include a right-left byte select register (CCFBYTE), a local-global mode register (CCFGLB), two adder comparator registers (ADFEQL and ADFNEG), and an adder overflow register (ADFOVF).

4-9. By way of initial orientation to the processor, the block diagram shows the major data transfer paths over which the various elements of the processor communicate with one another. A thorough study of this diagram shows many particulars about data flow within the 704 Processor. For example, memory location addresses must come from the memory address register, even when the DMA option is employed. Also, instructions fetched from memory are loaded into the instruction register through the memory buffer register. Further, the program counter register is the only register that transfers data directly rather than through the adder. And finally, only the accumulator register is accessible through the DIO bus interface.

4-10. The adder inputs, gates A and B, are the only means by which data can be applied to the adder. Both gates are used simultaneously for arithmetic and logical operations. During load-from-memory operations, data is transferred from the memory buffer register to the accumulator through the B-gates. Conversely, data is transferred from the accumulator to the memory buffer register through the A-gates during store-into-memory operations. The A-gates are also used for copy, invert, complement, and increment program counter register operations.

4-11. CPU TIMING (Figure 4-2)

4-12. The basic timing interval in the CPU is the "machine cycle". The time required to complete one machine cycle in the 704 Processor is 1.0 μs, and the cycle consists of five clock periods of 200 μs each. Intervals between clocks within a machine cycle are designated time periods T0 through T4, in the order of their occurrence.

4-13. No particular significance can be assigned to the individual time periods that applies generally in all cases. The same action may be performed in one time period in one instruction and in a different time period in another instruction. Also, the actions performed during one machine cycle (enabling, loading, decision making, shifting, etc) may be completely different from those performed in the next machine cycle. Therefore, the significance of the time periods must be related to the particular operations being performed.

4-14. See timing diagrams, figure 4-3. The time periods are defined as the interval from the trailing edge of one clock to the trailing edge of the following clock pulse. Signals are gated during the time period and are clocked by the clock pulse that occurs at the end of the period. Each clock pulse is 75 ns wide, ideally. Type D flip-flops used in all seven major registers of the CPU are positive-edge triggered. These receive inverted clock signals; consequently, transition occurs in these flip-flops coincident with clock pulse trailing edges at the end of the period, as prescribed. The type J-K flip-flops used for other CPU functions are negative-edge triggered. Clock leading edges, which occur 75 ns prior to the end of the time period, enable the clocked inputs to these flip-flops, and the trailing edges trigger transition.

4-15. The direct set and reset inputs to flip-flops of both types are not clocked, and the flip-flops may be set or reset asynchronously by signals applied to these inputs. They respond to negative-true (0 V) level signals.

4-16. Clock Logic

4-17. The clock logic (Drawing 394562, Sht 10) is contained on the Memory Control card. A 20-mHz, crystal-controlled oscillator supplies the primary time standard for the processor. It runs at all times when power is applied to the CPU, and its KK20MCF signal output is used to clock a six-stage frequency divider continuously.

4-18. Flip-flops C0 through C5 are arranged as a ring counter and perform divide-by-four frequency division. A three input AND gate delivers a 1 to the first flip-flop, C3, when the first three flip-flops are in the 0 state. This 1 is propagated down the ring by each KK20MC clock pulse followed by 0's until

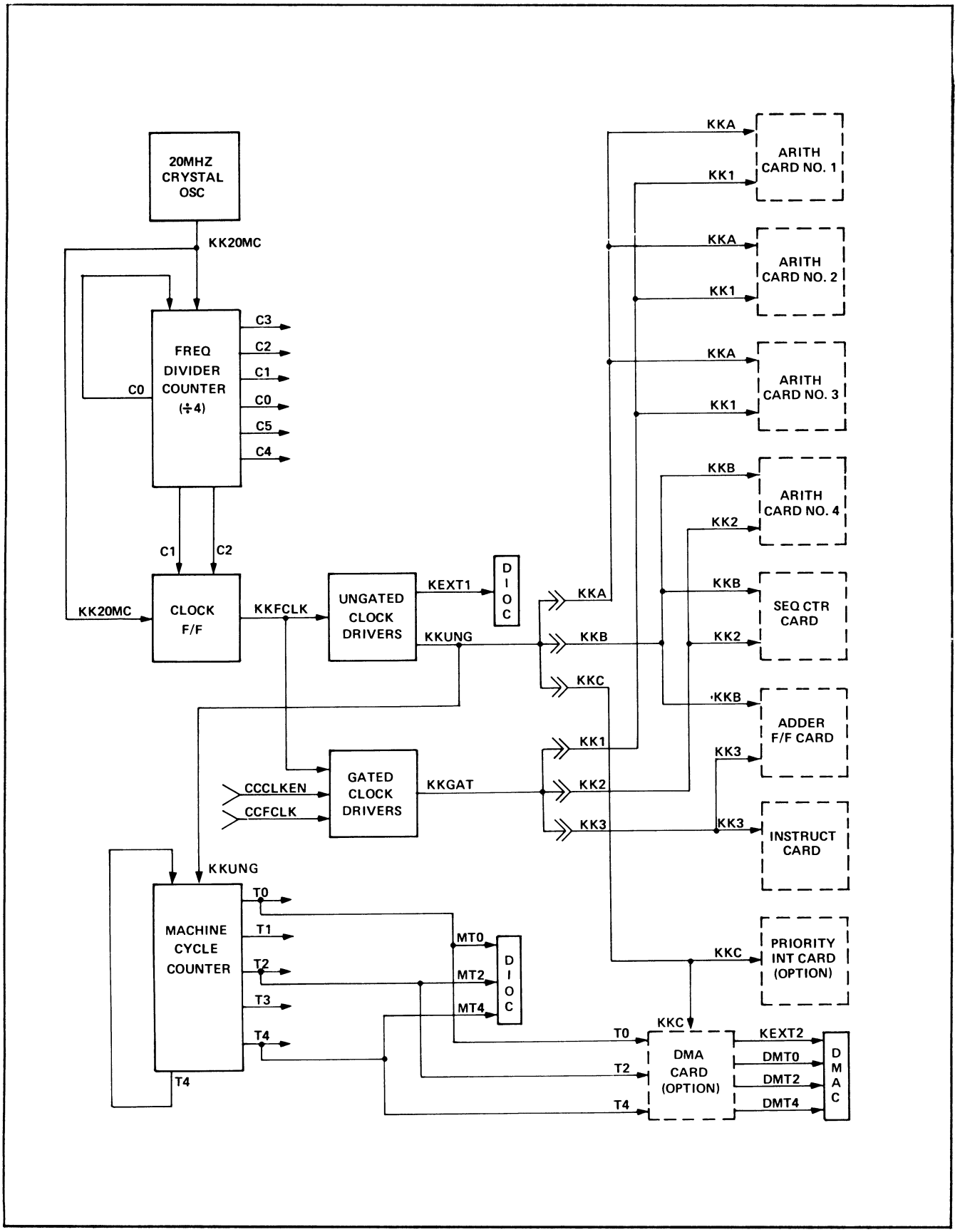


Figure 4-2. Clock Logic and Distribution Block Diagram

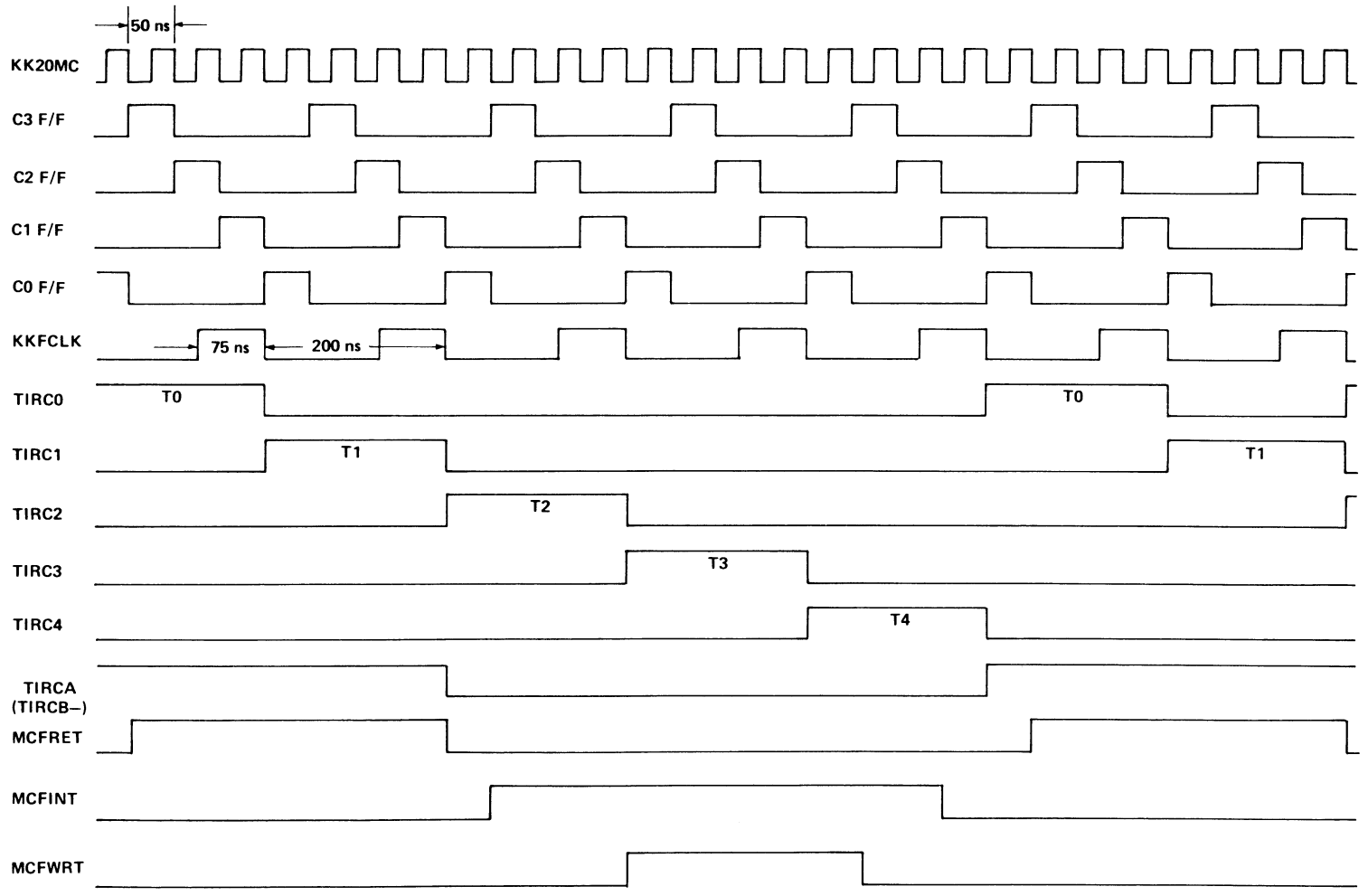


Figure 4-3. Idealized Clock and 1.0 μs Machine Cycle Timing Diagram

it reaches flip-flop C0, at which time another 1 is delivered to the counter. The states of flip-flops C5 and C4 "follow" those of flip-flops C3 and C2, respectively.

4-19. The basic clock, KKFCLK, is generated by a type J-K flip-flop that is directly set by the first positive-going edge of KK20MC that occurs in the time interval when divider flip-flop C2 is set. The flip-flop is toggled reset approximately 75 ns later by the negative edge of KKCLKDLY. This occurs on the negative edge of the KK20MC pulse when flip-flop C1 is set. KKFCLK generated clock pulses are delivered to two ungated clock drivers in parallel and two gated clock drivers in parallel for distribution to the rest of the computer system (paragraph 4-23).

4-20. A five stage ring counter, consisting of flip-flops TIRC0 through TIRC4, counts the basic clock pulses and divides the machine cycle interval into its five constituent time periods. Type J-K flip-flops are used, clocked by ungated clock driver output KKUNG. When the first four flip-flops are in the reset state (TIRC0- TIRC1- TIRC2- TIRC3-), the set input of TIRC0 is enabled to set the flip-flop on the trailing edge of the next clock. The setting of TIRC0 disables the set input, and succeeding clocks cause TIRC1, TIRC2, TIRC3, and TIRC4 to be set in turn, while the preceding flip-flop in the ring is reset. Each circulation through the ring, from TIRC0 being set to TIRC4 being reset, constitutes one machine cycle.

4-21. Timing signals T0, T2, and T4 are supplied to devices on the data input-output (DIO) bus and optional direct memory access (DMA) bus to synchronize their operation with the operation of the CPU. These signals are inverted and transmitted as negative-true signals on the DIO bus (MT0-, MT2-, and MT4-) and by the optional DMA card, when used (DMT0-, DMT2-, and DMT4-).

4-22. A TIRCA/TIRCB flip-flop provides a further subdivision of the machine cycle into two components. This flip-flop is set by the clock that resets TIRC4, producing the TIRCA phase output during time periods T0 and T1. The flip-flop is reset by the same clock that resets TIRC1, producing the TIRCB (TIRCA-) phase output during time periods T2, T3, and T4. This two state cycle is repeated every machine cycle, and the outputs TIRCA and TIRCB are used as a convenience in mechanizing the CPU timing logic (paragraph 4-222).

4-23. Clock Distribution

4-24. A continuous train of KKFCLK clock pulses is provided by the ungated clock drivers as long as power is applied to the CPU. These outputs include an inverted, negative-true KEXT1- output to the DIO bus for external clocking of device controllers connected to the bus. The basic ungated clock has the generic name KKUNG but is renamed KKA, KKB, and KKC for distribution. These "letter" names merely identify clock lines from a common (KKUNG) source. Thus, clock line KKA distributes KKUNG clock pulses to Arithmetic cards 1, 2, and 3; clock line KKB distributes KKUNG clock pulses to Arithmetic card 4, the Sequence Counter card, and the Adder Flip-Flop card; and line KKC distributes KKUNG clock pulses to the option cards in use. Notice (figure 4-2) that the optional DMA card provides an inverter for negative-true clock output KEXT2- that is used to externally clock device controllers connected to the DMA bus.

4-25. The gated clock drivers provide KKFCLK clock pulses under the on-off control of gating signals CCCLKEN from the Sequence Counter card and CCFCLK from the optional DMA card. Both of these signals must be true to output KKGAT gated clock pulses for distribution. CCCLKEN is made false to halt CPU operation and momentarily true to pass clocks in the single step mode of operation. The logic for this clock control term is discussed in paragraph 4-46.

4-26. Signal CCFCLK is made false to suspend CPU operation while a device controller on the DMA bus has direct access to memory. This signal will always be in the true state when the DMA option is not installed. The logic for this clock control term is discussed in paragraph 4-545.

4-27. The generic name KKGAT identifies the output of the gated clock drivers but changes to KK1, KK2, and KK3 for distribution. These "number" names merely identify gated clock lines

from a common (KKGAT) source. Thus, clock line KK1 distributes KKGAT clock pulses to Arithmetic cards 1, 2 and 3; clock line KK2 distributes KKGAT clock pulses to Arithmetic card 4 and to the Sequence Counter card; and clock line KK3 distributes KKGAT clock pulses to the Adder Flip-Flop and Instruction cards.

4-28. CPU CONTROL

4-29. The CPU control logic (Drawing 394557, Sht 10) includes the operating controls and indicators on the front control panel and their associated logic on the Sequence Counter card, two synchronizing flip-flops, and five control flip-flops. The switches and indicators used for manual display or entry of data are not included in the CPU control logic. The display-enter logic is covered in paragraph 4-73, and the program counter controls and indicators are included in the program counter logic (paragraph 4-131).

4-30. System Reset

4-31. The 704 processing system may be reset manually any time power is on and the lockout switch is in the "unlocked" position by pressing the RESET switch on the front control panel. This action applies a ground to the CPSWRST- input of flip-flop CCFRST. The rising edge of clock KKSYN sets the CCFRST flip-flop at the end of a machine cycle (T4 KKB) and it remains set until the same time in the cycle following the release of the switch. The flip-flop will automatically be set by a momentary ground applied to power failsafe reset line PFRST- when the system power ON or OFF switch is pressed, when the optional Power Failsafe card is not installed. (Paragraph 4-751 discusses system reset when the power failsafe option is in use.)

4-32. During the time CCFRST is true, a ground level is applied to lines ACRDR-, MBRDR-, IXRDR-, and PCRDR- which causes direct reset of the accumulator, memory buffer register, index register, and the program counter, respectively. Signal CCFRST also enables power gates for external reset lines REXT1- and REXT2- that go to DIO and DMA peripheral device controllers. These lines are held to ground whenever the power on-off switches are pressed or the power failsafe option applies a reset signal. Finally, master reset line MRESET- goes to ground when CCFRST is true, causing the sequence counter, instruction register, extension register, iteration counter register and other control flip-flops to be reset to system initializing states.

4-33. Certain registers may be cleared selectively. Pressing the PROGRAM COUNTER CLEAR switch grounds line CPSWPCLR- and the PCRDR- direct reset line to the program counter register. Setting the DISPLAY SELECTOR switch to the AC position grounds reset logic input line CPSWDSAC-, making CPDSAC true to enable the ACRDR- gate. When the SELECTED DISPLAY CLEAR switch is pressed, line CPSWDCLR- is grounded, causing CPDCLR to go true which causes the accumulator register to receive an activating ground on direct line ACRDR-. In similar manner, setting the DISPLAY SELECTOR switch to the MB or IX positions grounds lines CPSWDSMB- or CPSWDSIX-, respectively, to enable either the MBRDR- gate to the memory buffer register or the IXRDR- gate to the index register. Pressing the CLEAR switch then activates the enabled gate and resets the selected register.

4-34. Control Switch Operation

4-35. With the exception of data entry, RESET, and CLEAR switches, all operating control switches are followed by latching circuits, consisting of two cross-connected NAND gates. These circuits eliminate the effects of contact bounce and the ambiguity that exists when the common contact of these single-pole, double-throw switches is transferring between the normally-open and the normally-closed contacts. No latch is required on the RESET, CLEAR, and data switches because these are used as single-pole, single-throw type (no ambiguity), and contact bounce has no effect upon this operation.

4-36. All control switch latches (CPHALT, CPRUN, etc) operate in the same manner. Each has two inputs, one connected to the normally-closed and one to the normally-open contacts of the associated control panel switch. The common (switching) contacts of all switches are connected

to ground through a key operated LOCKOUT switch, and toggling of a latch occurs when the ground level makes contact with one of the two latch inputs. Turning the LOCKOUT key switch to the "locked" position deactivates the switches by removing the ground from their common contacts and applying it to the CPSWMLCK- line. This keeps the outputs of all protected latches at the last level assumed. The four SENSE switch latches (CPSENS0 through CPSENS3) are not protected in this manner.

4-37. Auxiliary CPSWDSMB- input gates to the activated side of the DISPLAY and ENTER switch latches (CPDIS and CPENT) prevent these outputs from becoming true unless the DISPLAY SELECT switch is in the MB position (ground on CPSWDSMB- line). In effect, the DISPLAY and ENTER switches will be locked out and inoperative unless access to the memory buffer register is selected.

4-38. Control Switch Synchronization

4-39. Two flip-flops, CCFSYN1 and CCFSYN2, synchronize the asynchronous activity of the control switch latch output signals to the machine cycle. Both flip-flops are initially in the reset state. As long as the direct memory access option is not active (CCFCLK true), the set input gate of the type-D CCFSYN1 flip-flop is enabled. Set input signal CCFSYN11, mechanized in the form [CPHALT-(CPDIAEN + SCDC1F0-]-, is equivalent to the expression CPHALT + CPDIS + CPENT + CPRUN + CPSCM + CPSSTP. In other words, activation of any one of the primary control switch latches will make the set input CCFSYN1S true.

4-40. The operation of the synchronization flip-flops is shown in a timing diagram, figure 4-4. KKSYN and KKSYNA clock pulses consist of ungated KKB clocks that occur at the end of each T4 time period. When a switch latch goes true, the

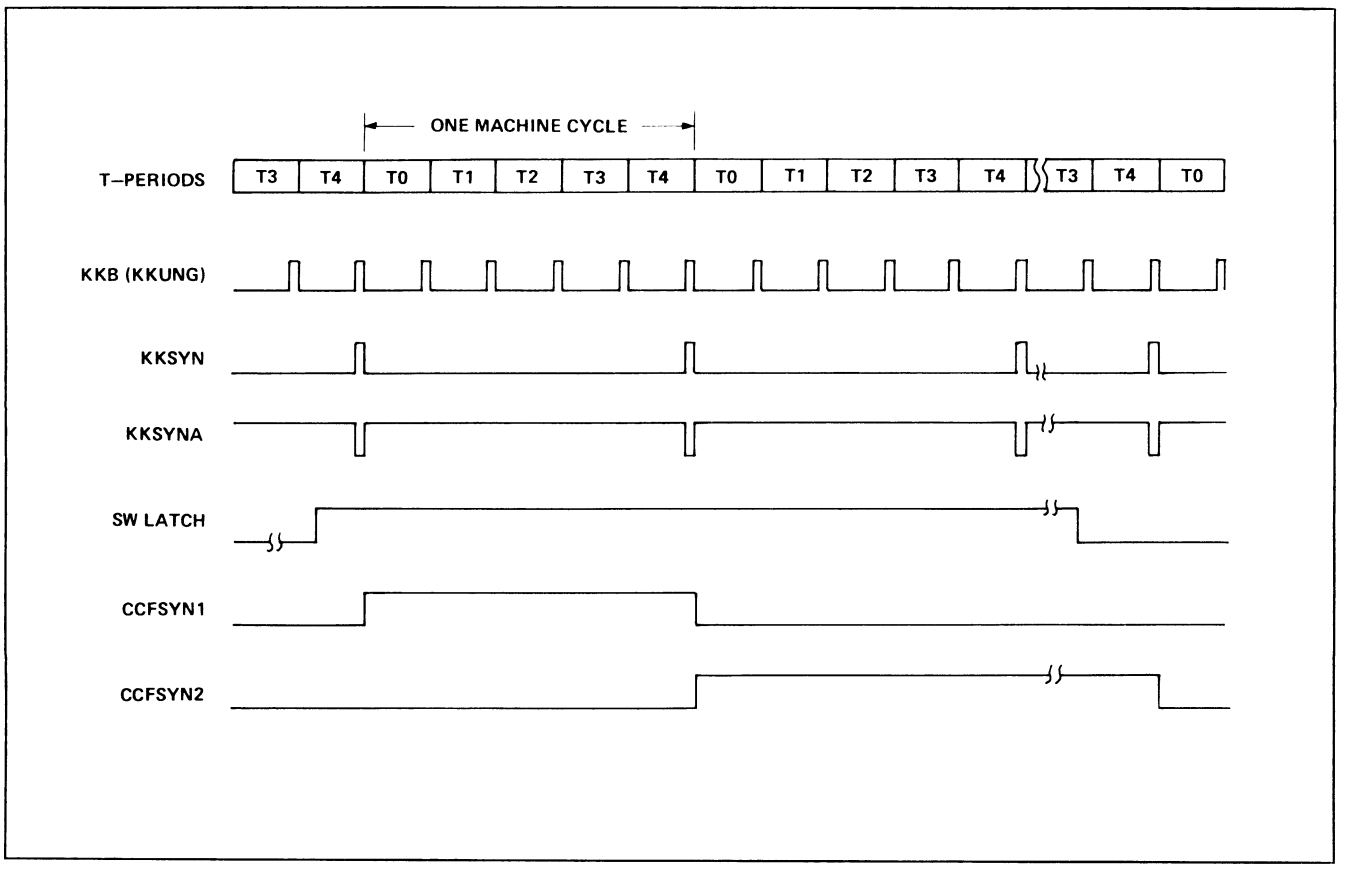


Figure 4-4. SYNC Flip-Flop Timing Diagram

rising edge of the next KKSYNA clock sets CCFSYN1. This enables the set input of flip-flop CCFSYN2, which is set by the falling edge of the next KKSYN clock one machine cycle later. The setting of CCFSYN1 disables the CCFSYN1 input gate, making CCFSYN1S false. Consequently, CCFSYN1 will be reset by the rising edge of the next KKSYNA clock, which occurs when CCFSYN2 is set and cannot be set again until CCFSYN2 has been reset. To reset CCFSYN2, the control switch must be released to deactivate the switch latch which is making signal CCFSYN11 true. The falling edge of the KKSYN clock following release of the switch resets CCFSYN2 and restores the synchronization flip-flops to their initial inactive state. Execution of switch selected control functions occurs during the machine cycle that flip-flop CCFSYN1 is set. The CCFSYN2 flip-flop is used only to lock out subsequent setting of CCFSYN1 while the switch remains activated.

4-41. Run Control

4-42. Pressing the RUN switch starts the CPU. How this is effected is shown in a timing diagram, figure 4-5. Flip-flop CCFRUN is the controlling element. Its set input can only be activated by the true state of RUN switch latch output CPRUN synchronized by the setting of CCFSYN1. The KKMCENMA clock pulses used by the CCFRUN flip-flop are similar to KKSYN clock pulses in timing (T4 KKB), but are inhibited during single step operations, when signal CCCLKEN is false.

Note

In order to obtain a direct reset input for the CCFRUN flip-flop, it was necessary to invert its logical states; that is, the K-input is used as the set input and the $\overline{Q}$-output is used as the true output.

4-43. Once run control flip-flop CCFRUN is set, the sequence counter that controls CPU operation can advance from its idle state. Operation of the sequence counter is discussed in paragraph 4-98. With signal CCFRUN true, a CPRUNL- driver applies a ground to the return side of the front panel RUN indicator lamp to light it.

4-44. The CCFRUN flip-flop will remain set and the CPU will continue to operate in the run mode

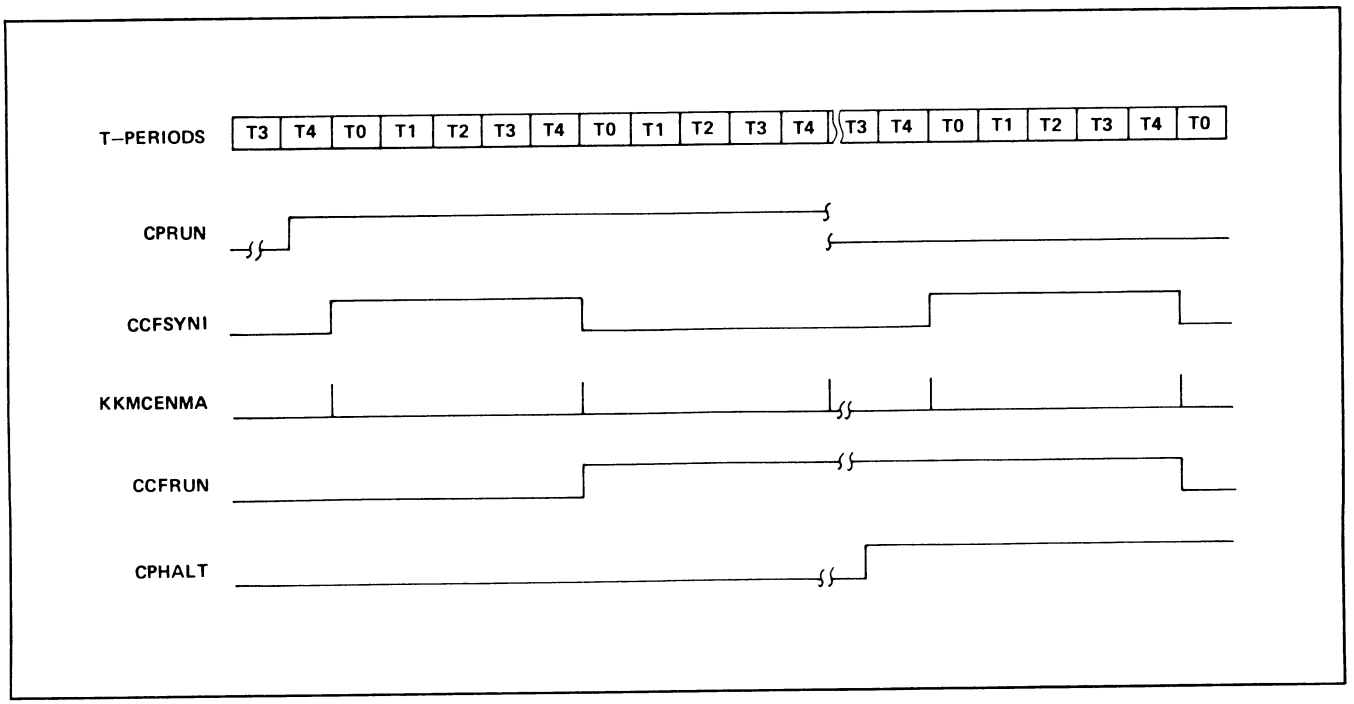


Figure 4-5. RUN Flip-Flop Timing Diagram

until a HLT instruction is executed (SCDC1A INDC000) or the HALT switch is pressed (CPHALT CCFSYN1). Either condition will cause the trailing edge of the next KKMCENMA clock to reset CCFRUN at the end of the machine cycle. With signal CCFRUN- true, a CPHLTL- driver applies a ground to the return side of the front panel HALT indicator lamp to light it. At the same time, the RUN indicator lamp will go out.

4-45. Use of the RESET switch to halt the CPU will directly reset flip-flop CCFRUN (applies CPSWRST- to CCFRUNDS- input) without regard to time period or instruction execution phase. This is an incorrect operating procedure and must not be used because of the danger of introducing errors into the program, the contents of memory, and data transmission over the DIO and DMA busses. If the optional DMA card is installed, detected memory parity errors will also halt the CPU by resetting the CCFRUN flip-flop (PARER- signal applied to negative-true CCFRUNDS OR-gate).

4-46. Single-Step Operation

4-47. In single-step operation, the program is executed one machine cycle at a time. Each time that the SINGLE STEP switch is pressed, the CPU operates for one machine cycle then pauses until the switch is pressed again. The term "pause" is used rather than "halt" because the sequence counter does not return to the halt state after each step but remains in the appropriate instruction execution phase.

4-48. The pauses between steps are effected by inhibiting the distribution of gated clock signals throughout the CPU. When the SINGLE STEP switch is pressed for the first time at the start of the single-step operation, single-step control flip-flop CCFSTP is synchronously set (CPSSTP CCFSYN1), and distribution of gated clock pulses is inhibited, starting at the end of the machine cycle during which signal CCFSYN1 is true (CCFSSTP- and CCFSSTPS are both false, making clock gate enable signal CCCLKEN false). The setting of flip-flop CCFSSTP causes driver CPSSTPL to provide a ground return for the SINGLE STEP indicator lamp, lighting it.

4-49. The CPU must be halted before operating in single-step mode, so the sequence counter will advance from the halt state to the instruction fetch phase (discussed in paragraph 4-98) at the same time that distribution of gated clock pulses is inhibited. The instruction fetch operation is not executed until the SINGLE STEP switch is pressed again.

4-50. Pressing the SINGLE STEP switch the second time again makes signals CCFSSTPS and CCCLKEN true for one machine cycle, during which one instruction phase is executed. The sequence counter enters the next instruction phase, and clock distribution is inhibited once again at the end of the cycle. This sequence of operations is repeated each time the SINGLE STEP switch is pressed.

4-51. Single-step operation is terminated by pressing the HALT switch. This action synchronously resets the CCFRUN and CCFSSTP flip-flops at the end of the current machine cycle (CPHALT CCFSYN1 KKSYN). The resetting of CCFSSTP makes the SINGLE STEP lamp go out and enables the distribution of gated clock pulses once again (CCCLKEN true). If the sequence counter is not in the halt state when the flip-flop is reset, the instruction execution cycle or interrupt service cycle in progress will be completed, the sequence counter will enter the halt state, and CPU operation will stop because the run control flip-flop CCFRUN is in the reset state.

4-52. Single Command Operation

4-53. In single command operation, the program is executed one instruction at a time, irrespective of the number of machine cycles required to execute an instruction. The CPU must be halted when the SINGLE COMMAND switch is pressed to operate in this mode. No control flip-flop is associated with the SINGLE COMMAND switch; the single-command operation being entirely controlled by the sequence counter logic (discussed in detail in paragraph 4-111).

4-54. When the CPU is halted and not set for single-step operation (CCFRUN- CCFSSTP- true),

sequence counter "steering" signals CCSCM will be true and CCSCM- will be false. Pressing of the SINGLE COMMAND switch causes switch latch output CPSCM, synchronized by CCFSYN1, to advance the sequence counter from the halt state into the instruction fetch phase at the beginning of a machine cycle. Normally, after the end of command execution is detected, the sequence counter will return to the instruction fetch phase to continue program processing, unless the run control flip-flop has been reset. However, with steering signal CCSCM true, the sequence counter returns to the halt state at the end of the instruction execution cycle. Repeated pressing of the SINGLE COMMAND switch will cause the CPU to fetch and execute one instruction and return to halt each time the switch is pressed.

4-55. Manual Memory Display and Entry

4-56. The DISPLAY and ENTER switches are used to display or enter manually a word in memory while the CPU is halted. The word is displayed or entered via the memory buffer register, and the SELECTED DISPLAY switch must be set to MB. The word in the memory buffer register is displayed and entered through the SELECTED DISPLAY switches and indicators (discussed in paragraph 4-470).

4-57. The initial memory location address to be accessed is placed into the program counter register by first clearing the register and then entering the address by means of the PROGRAM COUNTER switches. When either the DISPLAY or ENTER switch is pressed, by signal CPDIAEN is true (CPDIS- CPENT-)-. This signal, synchronized by the setting of CCFSYN1, makes memory control term MCENB2 true, and MCENB2 gated with time period T1 (PCLDAD logic) and KK1 (KKPC logic) increments the program count by one. During the same machine cycle, a memory read/write operation is executed (MCRW- logic) to load the memory buffer register with the contents of the address memory location for display or to store the manually entered contents of the memory buffer register into the memory location addressed. Incrementing of the program count is discussed in paragraph 4-241, memory addressing is discussed in paragraph 4-387, and data transfer to and from the memory buffer register is discussed in paragraph 4-444.

4-58. Sense Switches

4-59. The SENSE switches (Dwg 394557, Sht 11) are used to modify the execution of programs. Instructions SS0 through SS3 are used to test ("sense") the positions of the switches and to direct the execution of the program accordingly. Instruction SSE may be used to test an external sense line (DIO input EXSENS-) for the same purpose.

4-60. The normal outputs of the SENSE switch latches (CPSENS0 through CPSENS3) and the negative-true (inverted) EXSENS- signal are used in the skip condition logic (Dwg 394562, Sht 11), and a program skip occurs if the switch being tested is off (down) or the external sense line is false (+3 V) when tested. Program skips are discussed in paragraph 4-139.

4-61. Byte Control Flip-Flop

4-62. The byte control flip-flop CCFBYTE (Dwg 394567, Sht 6) controls the selection of the left or right byte of a word in the CPU during the execution of a byte instruction (CMB, LDB, or STB).

4-63. During the first machine cycle of a byte instruction, the least significant bit of the byte memory address is stored in the byte control flip-flop when the memory address of the word containing the byte is formed (paragraph 4-416). The flip-flop will be set (CCFBYTE) if a right, or odd numbered, byte is addressed (T4SCDC1C INDCBYTE ADSUM15) and is reset (CCFBYTE-) if a left, or even numbered, byte is address (T4SCDC1C INDCBYTE ADSUM15-). The use of the flip-flop outputs to control the selection of the left or right byte is discussed in paragraph 4-457.

4-64. Global Control Flip-Flop

4-65. The global control flip-flop CCFGLB (Dwg 394567, Sht 6) selects the memory addressing mode when the index bit (bit 04) of the instruction word is 1. The indexed global mode is selected if the flip-flop is set, and the indexed local mode is

selected if the flip-flop is reset. Memory addressing is discussed in paragraph 4-375.

4-66. Two instructions, SGM and SLM, are used for program control of the CCFGLB flip-flop. The SGM instruction sets the flip-flop at the end of the instruction execution cycle (T4SCDC1 INDC005). The SLM instruction resets the flip-flop at the end of the instruction execution cycle (T4SCDC1 INDC004).

4-67. Execution of a JSX instruction causes the memory address to be formed in the indexed global mode, regardless of the state of the CCFGLB flip-flop, then sets the flip-flop at the end of the instruction execution cycle (INDC2 T4SCDC1). The flip-flop is also set automatically for global indexing at the end of an interrupt service cycle (SCDCD T4) load link phase (Phase D). This cycle is discussed in paragraph 4-110.

4-68. During an interrupt service routine, the prior state of flip-flop CCFGLB is stored in bit 08 of the machine status word (paragraph 4-612). At the end of the interrupt service routine, the machine status is restored during the execution of the concluding interrupt return INR instruction. When the CPU enters phase 9 as the result of the INR instruction, the CCFGLB flip-flop is unconditionally reset (SCDC9). At the end of the same machine cycle, if bit 08 of the machine status word is a 1, the flip-flop will be set (SCDC9 T4 MBR08) by toggle action. Otherwise, it will remain reset.

4-69. Interrupt Inhibit Flip-Flop

4-70. Interrupt inhibit flip-flop ITFINH enables or disables the priority interrupt system under program control. It has no effect on the receiving or storage of interrupts on the individual interrupt levels, but only controls the interrupt output from the system to the remainder of the CPU. Operation of the interrupt system is discussed in paragraph 4-576.

4-71. Two instructions are used to set or reset the ITFINH flip-flop. The MSK instruction sets the flip-flop at the end of time period T3 of the machine cycle in which it is executed (SCDC1 INDC00A). As long as ITFINH is set, waiting interrupts will not be serviced. Execution of the UNM instruction will reset flip-flop ITFINH at the end of time period T3 of the machine cycle in which it is executed (SCDC1 INDC00B), allowing service of interrupts to commence on the next machine cycle. A power failsafe reset input, PFSINT-, used with the power failsafe option, enables the ITFINH flip-flop to be reset whenever a power failure occurs to ensure that the power failsafe interrupt will be serviced before dc power goes down.

4-72. The interrupt-enable side of the flip-flop (ITFINH-) is gated as interrupt service cycle control signal CCITCY, when an interrupt is waiting (ITWAIT + IT00RQ), except during the service cycle itself (phases 7, B, and D). Interrupt service cycle operation is discussed in paragraph 4-607.

4-73. MANUAL REGISTER DISPLAY AND ENTRY

4-74. Data may be displayed from or entered manually into certain registers by means of the DISPLAY SELECTOR switch and the SELECTED DISPLAY switches and indicators on the front control panel. The DISPLAY and ENTER switches are not used for this purpose; they control the display or entry of a word in memory. Operation of these switches is discussed in paragraph 4-55.

4-75. Data Display

4-76. The DISPLAY SELECTOR switch enables register output lamp drivers from one of five data sources for display by the SELECTED DISPLAY indicators. When the switch is in the IN position, signal DISPIN (CPSWDSIN- inverted) enables gated lamp drivers connected to the outputs of the instruction register (INR0 through INR7), and those drivers whose inputs are 1's supply a ground on return lines DISP00- through DISP07- to light the respective SELECTED DISPLAY indicator lamps 0 through 7. Also, special encoding logic associated with DISPIN enabled lamp drivers DISP12- through DISP15- provides the state of the sequence counter, displayed in hexadecimal-to-binary form by indicators 12 through 15. Thus, phase 1 will be displayed as 0001, phase 9 as 1001, phase C as 1100, etc.

4-77. A machine status word will be displayed when the DISPLAY SELECTOR switch is in the MS position. Signal DISPMS (CPSWDSMS- inverted) enables the appropriate lamp drivers for this display. Data displayed includes the contents of the extension register (EXR00 through EXR04) on lamps 0 through 4; the states of adder flip-flops ADFNEG, ADFEQL, and ADFOVF on indicators 5, 6, and 7, respectively; and the state of global control flip-flop CCFGLB on indicator 8.

4-78. In the MB position of the switch, signal DISPMB gates the contents of the memory buffer register (MBR00 through MBR15) into lamp drivers for SELECTED DISPLAY indicators 0 through 15.

4-79. In the IX and AC positions, signals DISPIX and DISPAC gate the contents of the index register (IXR00 through IXR15) and the accumulator register (ACR00 through ACR15), respectively, and the contents of the register selected are displayed by indicators 0 through 15.

4-80. Data Entry

4-81. Only three positions of the DISPLAY SELECTOR switch may be used for entering data: MB, IX, and AC. In addition to enabling lamp drivers for content display, signals DISPMB, DISPIX, and DISPAC produced by these three switch positions also enable gates to the direct-set inputs of the memory buffer register, the index register, and the accumulator, respectively, connecting them to the SELECTED DISPLAY data entry switches (buffered by DISPENB gates).

4-82. To change the contents of one of the three registers having manual data entry capability, the DISPLAY SELECTOR switch is first set to the appropriate position. This displays the contents of the register selected and enables the direct-set gates to the register. Individual flip-flops in the register cannot be reset manually. If it is necessary to change the state of some bit from a 1 to a 0, the entire register must be reset, and the required 1's are then reentered manually. The register is reset by pressing the SELECTED DISPLAY CLEAR switch, as discussed previously (paragraph 4-33).

4-83. SELECTED DISPLAY switches 0 through 15 correspond directly with the 16 bit positions of the data word. When one of these switches is pressed, the direct-set input of the corresponding bit position flip-flop in the selected register is grounded, setting the flip-flop. Changes in the contents of the register can be seen in the data displayed by the indicator lamps.

4-84. INSTRUCTION EXECUTION

4-85. The 704 Processor program instructions are stored in memory and are brought into the CPU for execution under the control of the program counter. The instructions are fetched and executed in the sequence of their memory locations except when program skips, jumps, or interrupts occur.

4-86. The operation codes and the functions performed by all 704 machine-level instructions are described in the *704 User's Manual.* Reader familiarity with the operational functions of the instructions is assumed. The discussion here is limited to machine-level execution of the instructions.

4-87. The term "instruction code" is used in this manual rather than "operation code" because the former term is used throughout the CPU logic to identify the instruction code register, the instruction decoding logic, and the resulting control signals used by the CPU. A block diagram, figure 4-6, shows the primary functions in the instruction decoding and sequence control logic and the sources and destinations of major control signals.

4-88. Instruction Code Register

4-89. The code for a 704 instruction may consist of one, two, or three hexadecimal characters (4, 8, or 12 bits), depending upon the nature of the instruction. The first two characters of the instruction word (bits 00 through 07) are copied from the memory buffer register into the instruction register (Dwg 394552, Sht 8). One or both of these characters is decoded into intermediate control signals. The third character, if required by the nature of the instruction, is decoded from corresponding output bits (bits 08 through 11) from the memory buffer register.

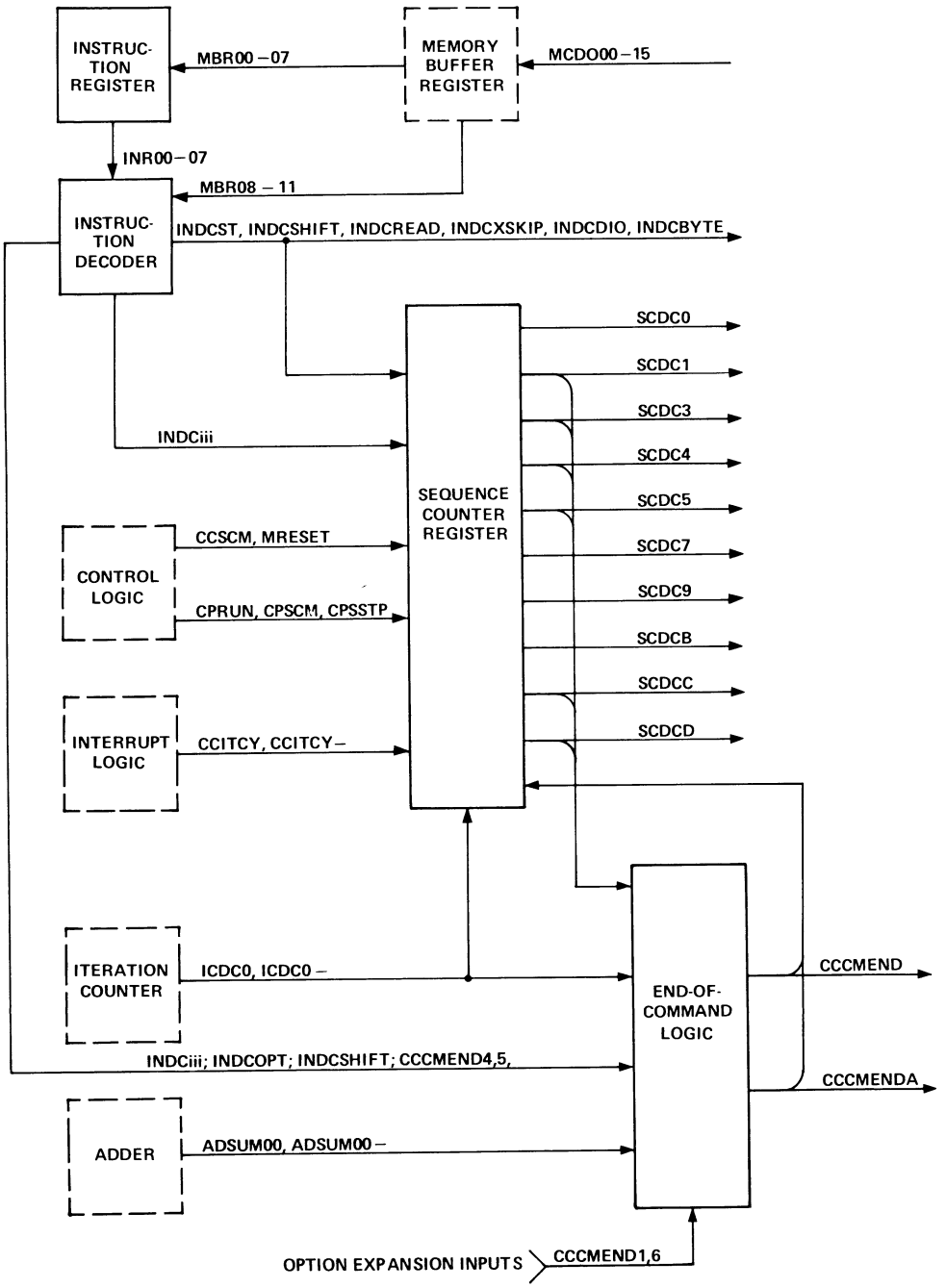


Figure 4-6. Instruction Decoder and Sequencer Block Diagram

4-90. The instruction code register consists of eight type-D flip-flops (INR0 through INR7) whose inputs are connected to applicable outputs of the memory buffer register (MBR00- through MBR07-). The clocks for this register (identical signals KKINA and KKINB) are so gated that a positive-going clocking edge only occurs at the end of time period T1 of the sequencer fetch phase (SCDC1). This timing is contingent upon the instruction word having been read into the memory buffer register within the first 400 ns of the fetch machine cycle.

4-91. The first eight bits of the instruction word remain in the instruction code register until the fetch phase of the next instruction. However, the contents of the memory buffer register may be altered during succeeding phases of the instruction execution cycle, if any, and the last two characters of the instruction word will no longer be available in the register. This makes no difference, with two exceptions which will be discussed later, because these characters are not required after the fetch phase.

4-92. Instruction Decoding

4-93. The transformation of instruction code characters held by the instruction register into functioning control signals for the CPU is accomplished in a minimum of two stages. First, each 4-bit character is converted into hexadecimal form. Secondly, the hexadecimal character signals representing various instructions are combined by gating where there is commonality of function. This common function gating itself may be done in one and in some cases two stages before the final control signal is fully formed. Examples of this will be discussed shortly.

4-94. The first stage of instruction decoding, binary-to-hexidecimal conversion, is performed by four binary-to-octonary converters (Dwg 394552, Sht 9); two for the more-significant character (inputs INR0 through INR3) and two for the less-significant character (inputs INR4 through INR7). These converters are ungated and unclocked and always provide outputs that are equivalent to their inputs from the instruction code register. Moreover, they employ negative-true logic; hence inputs are applied and outputs are received in their inverted form.

4-95. Consider the operation of the converter for the more-significant character (outputs INDC0- through INDCF-). If the most-significant bit INR0 is a 0, one of the outputs INDC0- through INDC7- will be low (negative true) according to the states of bits INR1 through INR3. If INR0 is a 1, the second binary-to-octonary converter comes into play, and one of the outputs INDC8- through INDCF- will be low according to the states of bits INR1 through INR3. Those outputs not activated by the detected code state will be high (negative false).

4-96. The binary-to-hexadecimal converter for the less-significant character (outputs INDC00- through INDC0F-) functions in an identical manner but operates with bits INR4 through INR7. However, the enabling signals for the first and second halves of the converter are INR00ENB- and INR08ENB-, respectively. If INR00ENB- is low (positive-true INR4- INDC0), one of the outputs INDC00- through INDC07- will be low, according to the states of bits INR5 through INR7. Conversely, if INR08ENB- is low (positive-true INR4 INDC0), one of the outputs INDC08- through INDC0F- will be low according to the states of bits INR5 through INR7. Notice that term INDC0 is common to both enabling signals. This is logically consistent with the structure of 704 instructions, since the second digit is meaningless except in generic instructions (most significant digit is zero).

4-97. The second level of instruction decoding, that of combining converter outputs by function, can only be discussed superficially by giving a few examples, since this type of gating is extensive in the logic and involves use of AND-, OR-, NAND-, and NOR-gating, as is most expedient. For example, signal INDCDIO identifies the DIN and DOT instructions (INDC02 + INDC03) and is implemented by a NAND gate. Signal INDCST (equal to INDC3 + INDC6 + INDC7) will be true during execution of store instructions STB, STX, and STW. More of this control signal logic will be described in conjunction with the functions they control.

4-98. Instruction Phase Sequencing

4-99. Most instructions are executed in one machine cycle, but several of them require two or more machine cycles to complete. The time required to execute each instruction is listed in the *704 User's Manual.* These variations in the time required, in increments of machine cycles, make it necessary to execute instructions under the control of a sequencer that directs the progression from one phase of the instruction execution cycle to the next, according to the instruction being executed.

4-100. The basic 704 sequence counter has 10 discrete states. These states and the conditions or instructions that cause the sequence counter to progress from one state to another are diagrammed in figure 4-7. Each state, other than "Halt", represents one phase of an instruction execution cycle and lasts for one machine cycle.

Note

Two additional sequence counter states and additional instruction sequencing logic are needed when the multiply-divide option is installed. These are discussed later, starting at paragraph 4-280.

4-101. The term sequence "counter" is a misnomer. The sequence counter does not "count" at all, but advances directly from one phase of an instruction execution cycle to the next, according to the conditions and instruction being executed.

4-102. The instruction fetch phase (phase 1) is the first phase of the execution cycle for all instructions. During this phase, a memory read operation loads the instruction word into the memory buffer register and the instruction register, where it is decoded into appropriate control signals. Many of the 704 instructions, called one-cycle instructions, can be completed during the fetch phase and produce a CCCMEND end-of-command signal throughout the fetching machine cycle.

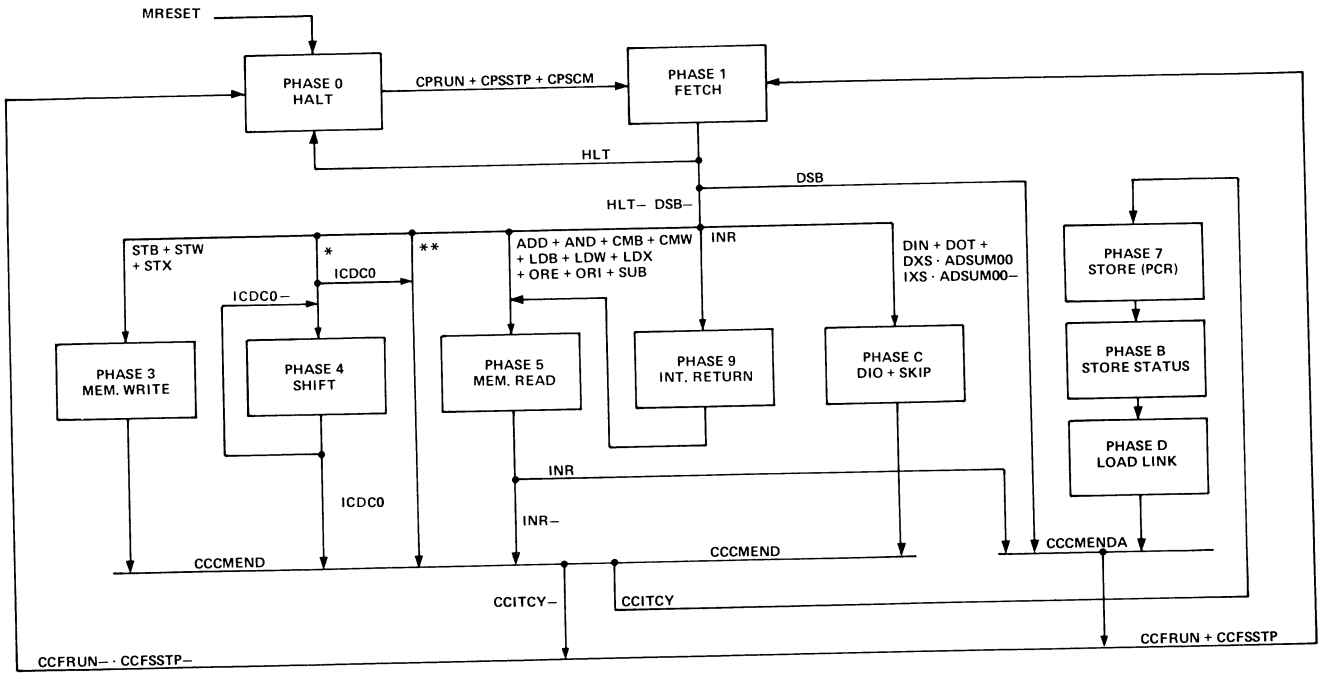
4-103. Whenever CCCMEND is true, a check is made of the interrupt logic status to determine if an interrupt is waiting for service (CCITCY true). If CCITCY is true, the sequencer immediately advances to the start of an interrupt service sequence (phases 7, B, and D), which will be discussed shortly.

4-104. Usually, an interrupt will not be waiting for service (CCITCY- true), and the sequencer will reenter (actually remain in) the fetch phase to fetch the next instruction for execution. This is true only if the CPU is operating in the run or single step modes (CCFRUN + CCFSSTP). If it happens to be operating in the single command mode (CCFRUN- CCFSSTP-), the sequencer will change to the halt phase (phase 0), and CPU operation will cease.

4-105. The halt phase may be entered in any one of five ways: (1) by turning on primary power, (2) by pressing the RESET switch while the CPU is operating (not a recommended procedure), (3) by pressing the HALT switch, (4) by executing a HLT instruction, and (5) by completing a single command mode operation. Once the halt phase is entered, CPU operation ceases and cannot be restarted except by actively causing the sequencer to leave the halt phase. This is done by pressing the RUN, SINGLE STEP, or SINGLE COMMAND switch (CPRUN + CPSSTP + CPSCM). In all cases, the sequencer will advance to phase 1, the fetch phase, causing the CPU to bring an instruction from memory for execution.

4-106. Those instructions requiring more than one machine cycle can be placed into one of six functional categories: memory write instructions, shift instructions, memory read instructions, interrupt return instruction, DIO instructions, and conditional skip instructions. An instruction falling into one of these categories causes the sequencer to advance from the fetch phase to one of five other phases without the CCCMEND signal being generated. Unless some conditional situation specifically prohibits it, the phase entered will last for one machine cycle.

4-107. Memory write instructions STB, STW, and STX cause the sequencer to advance to phase 3, during which the data is loaded into the memory buffer register to be written into memory. CCCMEND is produced during this phase to signal the end of command execution. The shift



*SHIFT INSTRUCTIONS

SLA	SLC	SLL	SRC	SRL
SLA D	SLC D	SLL D	SRC D	SRL D
SRA	SLC R	SLL R	SRC R	SRL R
SRA D	SLC L	SLL L	SRC L	SRL L

**ONE CYCLE INSTRUCTIONS

CAX	CXA	JSX	SAP	SLE	SNE	SS2	DXS · ADSUM00–
CEX	CXE	LLB	SAZ	SLM	SNO	SS3	IXS · ADSUM00
CLB	ENB	MSK	SEQ	SLS	SSE	SXE	
CLR	INV	SAM	SGM	SML	SS0	UNM	
CMP	JMP	SAO	SGR	SMU	SS1		

Figure 4-7. Instruction Phase Sequencing Diagram

instructions listed in the diagram are under control of an iteration count and cause the sequencer to advance from the fetch phase (during which the iteration count is loaded from the instruction word) to phase 4, but only if the iteration count is not zero (ICDC0 false). If an iteration count was not entered or was entered as zero (ICDC0 true) CCCMEND will be generated immediately, without shifting, to end the instruction. Otherwise, the sequencer will remain in phase 4 for the integral number of machine cycles required to reduce the iteration count to zero before CCCMEND is generated to end the instruction and advance the sequencer.

4-108. Those instructions that require the reading of an operand from memory (ADD, AND, CMB, CMW, etc) cause the sequencer to enter phase 5, during which the operand is read from memory and the operation is completed. The execution of an INR interrupt return instruction involves two memory read operations, one to retrieve the stored PCR count and one to retrieve the stored machine status word. Consequently, execution of an INR instruction causes the sequencer to enter an interposing memory read phase (phase 9) for one read operation before advancing to phase 5 for the second read operation. Notice that all memory read instructions except INR generate CCCMEND during the phase 5 machine cycle. INR generates CCCMENDA instead. The significance of this will be explained shortly.

4-109. Phase C is a "catch all" phase for two memory cycle instructions that don't fit into any of the other categories. These include the direct input-output instructions DIN and DOT and the conditional skip instructions DXS and IXS, where a skip operation is required (DXS ADSUM00 or IXS ADSUM00-). When execution of DXS or IXS does not demand a skip operation, they are treated as one-cycle instructions (DXS ADSUM00- or IXS ADSUM00).

4-110. Whenever the condition CCCMEND CCITCY is true, indicating that an instruction is about to be completed and an acknowledged interrupt is waiting for service, the sequencer advances to the start of an interrupt service sequence (phase 7) rather than returning to phase 1 or to phase 0. Each phase of this sequence lasts for one machine cycle. During phase 7, the count in the program counter is stored into memory. During phase B, a machine status word is assembled and stored into memory. And during phase D, the linking address to the start of the appropriate interrupt service routine is loaded from memory into the program counter and end-of-command signal CCCMENDA is generated. CCCMENDA differs from CCCMEND only in the fact that the waiting interrupt status is ignored. Consequently, after completing an interrupt service cycle (phase D), after completing an interrupt return (INR), or after disabling the interrupt system (DSB), the sequencer will return to the fetch phase (or to halt). This prevents the interrupt system from "capturing" the CPU by allowing at least one programmed instruction to be executed between interrupts. Interrupt servicing is more completely discussed in paragraph 4-576.

4-111. Sequence Counter Logic

4-112. The sequence counter consists of ten type-D flip-flops (Dwg 394557, Sht 4), one for each of the sequencer states. Clocks for these flip-flops (identical signals KKSC1 and KKSC2) are generated as the logical NAND combination of time period T4 and gated clock KK2 pulses. Consequently, the clock inputs will be high during all but the last 75 ns of a machine cycle (rising edge of KK2) when the inputs become low and rise again to provide the positive-going clock edge at the end of the machine cycle.

4-113. Sequence counter flip-flop outputs are identifiable by their SCDC names. SCDC0 is true during phase 0, SCDC1 is true during phase 1, etc. Notice that a ground on the MRESET- line will directly reset all sequence counter flip-flops except SCDC0, which will be directly set.

4-114. Disregarding direct set, there are three conditions that will cause the phase 0 flip-flop SCDC0 to be set. First, it will be set at the end of a non-interrupt service command, if an interrupt is not waiting and the CPU is operating in the single command mode (CCCMEND CCITCY- CCSCM). Secondly, it will be set at the end of any interrupt service command, if the CPU is operating in the

single command mode, regardless of interrupt status (CCCMENDA CCSCM). Finally, it will be set whenever a HLT instruction is fetched (SCDC1 INDC000). The gated condition SCDC0 SCDC1R for setting SCDC0 is a maintenance latch that keeps the type-D flip-flop set until some condition arises for setting the phase 1 flip-flop SCDC1.

4-115. There are three possible conditions under which phase 1 flip-flop SCDC1 will be set. First, it will be set synchronously whenever the RUN, SINGLE STEP, or SINGLE COMMAND switch is pressed and the sequencer is in the halt phase [(CPRUN + CPSSTP + CPSCM) SCDC0 CCFSYN1]. Secondly, it will be set at the end of a non-interrupt service command, if an interrupt is not waiting and the CPU is operating in either the run or single step mode (CCCMEND CCITCY-CCSCM-). And finally, it will be set at the end of any interrupt service instruction or cycle, if the CPU is operating in the run or single step mode, regardless of the interrupt system status (CCCMENDA CCSCM-).

4-116. The phase 3 flip-flop SCDC3 is preconditioned for setting by phase 1 and will be set at the end of the cycle if a store instruction is fetched (SCDC1 INDCST). Phase 4 flip-flop SCDC4 is for iterative shifting and will be set by any generic shift instruction if the iteration count is not zero and will remain set for as many whole machine cycles as it requires for the iteration count to reach zero (INDCSHIFT ICDC0-). Term INDCSHIFT is true for all instructions that satisfy the instruction decode condition INDC09 + INDC0A. This includes SLA (091), SLA D (093), SLC (0A5), etc.

4-117. The phase 5 flip-flop SCDC5 controls memory read activities to obtain operands and has two set conditions. First, it will be set if an instruction requiring operand reading is fetched in the fetch phase (INDCREAD SCDC1). Term INDCREAD is true for all instructions that satisfy the instruction decode condition INDC4 + INDC5 + INR0. This includes CMB (4), LDB (5), LDW (8), LDX (9), ADD (A), SUB (B), etc. The other condition for setting SCDC5 is phase 9 (SCDC9), which occurs only when executing an INR instruction. Consequently, the only set condition for the phase 9 flip-flop SCDC9 is SCDC1 INDC001.

4-118. Phase C flip-flop SCDCC has two setting conditions; one for direct input-output instructions and one for conditional skip instructions. The first condition is straightforward; if a DIN or DOT instruction is fetched in phase 1, SCDCC will be set (INDCDIO SCDC1). The conditions for generating term INDCDI0 were discussed in paragraph 4-97. The other SCDCC set condition is when a DXS or IXS instruction is fetched and executed in phase 1 and results in a program skip (INDCXSKIP SCDC1 CCCMEND1-). Expanded to its fullest form, this set logic becomes (INDC04 + INDC05) (SCDC1) (SCDC1 INDC04 ADSUM00)- (SCDC1 INDC05 ADSUM00-)-.

4-119. The sequence counter flip-flops SCDC7, SCDCB, and SCDCD are associated with the interrupt service sequencing. The phase 7 flip-flop SCDC7 can be set only at the end of an instruction execution if an interrupt is waiting service (CCCMEND CCITCY). The phase B flip-flop SCDCB will be set on the next machine cycle preconditioned only by the sequencer having previously entered phase 7 (SCDC7). And finally, the phase D flip-flop SCDCD will be set on the next machine cycle, with entry into phase B being the only set condition (SCDCB0).

4-120. End-of-Command Detector Logic

4-121. The purpose of CCCMEND logic (Dwg 394557, Sht 6) is to detect the last machine cycle of all 704 instructions except HLT, DSB, and INR. In concept, the function is quite simple; in mechanization, the logic becomes obscure. It is most easily seen by starting at the CCCMEND output and working backwards. The first level of gating resolves to SCDC3 + SCDCC + (SCDC1 INDC10R2) + CCCMEND1, which indicates that any time the sequencer enters phase 3 or phase C (these are unconditionally one machine cycle long), CCCMEND will be generated. Also, non-generic instructions JMP and JSX, since they are only one machine cycle long, will generate CCCMEND in phase 1 (SCDC1 INDC10R2). Term INDC10R2 stands for instruction codes INDC1 + INDC2. This leaves only term CCCMEND1 to detect the end points of all the other instructions not covered so far.

4-122. CCCMEND1 logic consists of eight NAND gates, the outputs of which are logically ORed so that any zero will make CCCMEND1- false and, consequently, CCCMEND true. The uppermost gate, CCCMEND5 SCDC1, detects generic instructions that satisfy the condition INDC01 + INDC06 + INDC07 + INDC08, which would include CLR (010), CMP (011), INV (012), etc. All of these instructions can be executed unconditionally in one machine cycle. The second and third gates down perform a similar function, ultimately detecting all one cycle instructions.

4-123. The fourth CCCMEND1 gate down, SCDC4 ICDC0, detects the end condition of phase 4 shift instructions when the iteration count reaches zero. The fifth and sixth gates detect the non-skip conditions of instructions IXS and DXS whereby they end in phase 1 without advancing to phase C. The next gate, SCDC1 INDCSHIFT ICDC0, detects the phase 1 end-of-shift instructions when the iteration count is zero. (Some 704 software uses zero-shift instructions as "no operation" instructions, in which case one machine cycle will be required for execution, but nothing will happen.)

4-124. The final CCCMEND1 gate, SCDC5 INDC0-, detects the end points of all phase 5 memory read instructions except the generic INR instruction. INR is expressly excluded because it is an interrupt service type instruction, and therefore is properly part of CCCMENDA logic rather than CCCMEND logic.

4-125. CCCMENDA logic (Dwg 394557, Sht 6) detects the end of the interrupt service sequence and interrupt servicing instructions INR and DSB. The logic resolves to the condition that CCCMENDA will be true if SCDCD + (SCDC5 INDC00) + (SCDC1 INDC003) is true. Consequently, CCCMENDA will be true whenever the sequencer enters phase D, the INR instruction execution enters phase 5, or whenever one machine cycle instruction DSB is fetched and executed.

4-126. PROGRAM EXECUTION

4-127. The sequential execution of program instructions is controlled by the program counter. The program counter stores the memory address of the next program instruction to be executed, and it is incremented automatically each time that an instruction is executed.

4-128. When instructions are being executed sequentially, the address of the next instruction to be executed is transferred from the program counter register to the memory address register at the same time that the sequence counter enters the instruction fetch phase. Simultaneously, the program count is gated into the adder and incremented by one. The incremented program count is loaded back into the program counter register at the same time that the current instruction is read in from memory and will be used to address the next instruction in sequence.

4-129. The program count is incremented automatically before the current instruction is decoded, but may not necessarily be used to address the next instruction. If the program sequence of instructions is broken by a skip, jump, or interrupt service operation, the program count will be modified or ignored in forming the address of the next instruction.

4-130. The program counter is also used during manual display and entry of memory data by sequentially addressing the memory locations each time a DISPLAY or ENTER switch is pressed. This application is discussed in paragraph 4-55.

4-131. Program Counter Register

4-132. The program counter register (Dwg 545497 — 500, Sht 5) is a 15-bit register, consisting of type-D flip-flops PCR01 through PCR15, with clocked inputs from the CPU adder and direct inputs from the PROGRAM COUNTER switches on the front control panel. The control panel switches are used to clear the program counter register or to preset the program count manually to a selected address. This register is contained on the four arithmetic cards with the three most-significant flip-flops on Arithmetic card 1 (PCR00 is not used and is disabled at its connector input) and four flip-flops on each of the other Arithmetic cards 2, 3, and 4.

4-133. Lamp drivers PCR01L- through PCR15L-

continuously display the register contents on the PROGRAM COUNTER indicator lamps. The drivers supply ground returns to light the lamps when their corresponding flip-flops are set.

4-134. During execution of a program, all inputs to the program counter register come from the adder (ADSUM01- through ADSUM15-), clocked by KKPC positive-going edges. These edges are formed by the logical combination of (PCLDAD KKn). The logic for clock enabling signal PCLDAD is discussed in the paragraphs that follow.

4-135. Sequential Program Execution

4-136. The program count is incremented automatically by the adder at the end of time period T1 of each instruction fetch phase. When the CPU enters the fetch phase, the program count is the same as the contents of the memory address register, which is being used to address the memory location of the instruction being fetched. While the memory read operation is taking place, signal ADENPC (term SCDC1 TIRCA) gates the contents of the program counter register into adder input gate A (Dwgs 545497 — 500, Sht 8) during time periods T0 and T1 of the fetch phase machine cycle. Since the adder uses inverted (1's complement) inputs and the output of the disabled adder input gate B represents -1 (adder gate B inputs are all 0's), the output of the adder will be the 1's complement of the program counter register content incremented by one. Operation of the adder is discussed more fully in paragraph 4-241.

4-137. Program counter register clock enable term PCLDAD is true during time period T1 of the fetch phase (SCDC1 TIRC1), and the rising edge of gated clock KKn causes KKPCn to go low 75 ns prior to the end of T1. The falling edge of KKn causes the KKPCn gate to produce a clocking positive-going edge at the end of time period T1, loading the program counter register with the incremented count from the adder. This count will be used to fetch the next instruction, if the current instruction does not cause a program skip or jump.

4-138. If the current instruction does not alter the program count, and a program interrupt does not occur, the incremented program count is loaded into the memory address register from the program counter register at the end of time period T4 of the last machine cycle of current instruction execution and is used to address the next instruction in sequence.

4-139. Program Skips

4-140. Two types of instructions can cause program skips: all skip generic instructions of the form INDC08n, and literal generic instructions DXS and IXS. The effect of either type of skip instruction is the same. If some condition tested by the instruction is true, the next instruction in sequence will be skipped, and the instruction that follows will be fetched and executed instead. However, the manner in which the program skip is accomplished depends upon the type of skip instruction being executed.

4-141. All skip generic instructions are executed in one machine cycle. The program count is automatically incremented once during time periods T0 and T1 of the fetch cycle (paragraph 4-241) as a normal event. However, during time periods T2, T3, and T4 of a machine cycle that fetches one of the skip generic instructions, the program count is again gated to the adder input gate A by ADENPC (term INDC08 SCDC1 TIRCA-). This twice-incremented program count at the adder output may or may not be loaded into the program counter register, depending upon the outcome of skip testing by the instruction.

4-142. Skip condition testing for skip generic instructions is performed by skip control logic (Dwg 394562, Sht 11) during time period T3. If the skip condition tested by an instruction is not satisfied, flip-flop CCFSKP will remain reset, and the twice-incremented program count at the adder output will not be used. Instead, the once-incremented program count in the program counter register will be loaded into the memory address register at the end of time period T4, and the next instruction in sequence will be fetched for execution.

4-143. If the skip condition is satisfied, signal CCFSKPS1 will be true, causing the skip flip-flop CCFSKP to be set at the end of fetch phase time

period T3 (INDC08 CCFSKPS1 SCDC1 TIRC3). When CCFSKP is set, the twice-incremented program count at the adder outputs will be simultaneously loaded into the program counter register by PCLDAD and into the memory address register by MALDAD at the end of time period T4. This will cause the next instruction in the program sequence to be skipped and the instruction following to be fetched and executed.

4-144. The skip control logic uses only the third decoded digit (INDCXX0 through INDCXXF) from memory buffer register output decoding logic to gate appropriate conditions to be tested. These 17 positive-OR gates (two are used for the SLE instruction identified by code INDCXX9) perform a negative-AND gate function; consequently, their inputs and outputs are inverted. Qualifying signal INDC08 prevents random occurrences of the CCFSKPS1 signal during the execution of other than skip generic instructions from setting the CCFSKP flip-flop.

4-145. Literal generic instructions DXS and IXS required two machine cycles to effect a program skip, but only one machine cycle is required for execution if the skip does not occur. In either case, the program count is incremented once during time periods T0 and T1 of the instruction fetch phase, as usual. During time periods T2, T3, and T4, the contents of the index register are incremented (IXS) or decremented (DXS) by the amount of the literal contained in bits 08 through 15 of the instruction word.

4-146. Both instructions gate the contents of the index register (IXR00 through IXR15) into adder input gate A (term INDCXSKIP SCDC1 TIRCA- of ADENIX). The IXS instruction generates ADENMBR to gate memory buffer register bits 08 through 15 into adder input gate B and ADINCRY to add a carry into the least significant digit of the adder. On the other hand, instruction DXS generates ADENMBC to gate the 1's complements of the memory buffer register contents into adder input gate B. At the same time, the instruction generates signal ADONES that forces adder gate B bits 05 and 07 to the 1 state. In effect, the adder will "see" all 1's in the first eight bits and the normal states of MBR08 through MBR15 outputs in the last eight bits, a necessary condition for performing a right literal subtraction using a 1's complement adder.

4-147. The incremented or decremented index quantity is loaded back into the index register at the end of time period T4. The sign of the index quantity at this time determines whether the sequence counter will reenter phase 1 to fetch the next instruction in sequence or will enter phase C to increment the program count and, consequently, skip the next instruction.

4-148. Entry into phase C automatically generates ADENPC to gate the program count into adder input gate A, and PCLDAD enables the program counter register clock during time period T1 of the skip phase (INDCXSKIP SCDCC T1). Once the incremented count is loaded back into the program counter register at the end of T1, no other action takes place during the skip phase. Signal MALDPC enables loading of the memory address register from the program counter register, and this occurs with the occurrence of the next memory address register clock at the end of time period T4.

4-149. Program Jumps

4-150. Two jump instructions alter the sequential execution of program instructions. Unconditional jump instruction JMP replaces the incremented program count with a literal address for the next instruction to be executed. Execution of a JSX instruction replaces the incremented program count with an address for the next instruction to be executed, but also stores the incremented program count into the index register to permit a return to the next instruction in sequence after performing some action at the jump location.

4-151. Both instructions are executed in one machine cycle. The program count is incremented as usual during time periods T0 and T1 of the cycle (paragraph 4-241). During the last portion of the cycle (time periods T2, T3, and T4), an effective word address is formed in the adder. The manner in which the address is formed depends upon whether a JMP or JSX instruction is being executed and is discussed in paragraph 4-406.

4-152. At the end of time period T4, the effective word address is loaded into the program counter register (term INDC10R2 T4SCDC1 of PCLDAD logic) and into the memory address register (SCDC7R SCDC1 INDC0- INDCBYTE- CCFCLK of MALDAD logic) from the adder. If a JSX instruction is being executed, the incremented program count is also stored in the index register at this time by a true IXLDPC signal (INDC2 T4SCDC1). The incremented program count is lost if a JMP instruction is being executed.

4-153. The effective word address specifies the next instruction to be executed, and the program jump to this location takes place in the next machine cycle.

4-154. Program Interrupts

4-155. A program interrupt causes the normal execution of program instructions to be suspended while the interrupt is serviced. At the end of the interrupt service routine, program execution will resume for at least one more instruction and continue until another program interrupt is encountered. The interrupt system itself is discussed in paragraph 4-576. The initiation and sequencing of interrupt service and interrupt return cycles by the sequence counter have been discussed in paragraph 4-119. Formation of memory addresses in the interrupt service and interrupt return cycles is discussed in paragraph 4-420. Only the operation of the program counter in these cycles is discussed here.

4-156. When the sequence counter enters an interrupt service cycle (phase 7), the program counter already contains the address of the next program instruction, to be executed. This address was placed into the register during the execution of the previous instruction, but was not loaded into the memory address register at the end of the instruction execution cycle because an interrupt was waiting for service (CCCMEND CCITCY) causing MALDIT to be true and MCENMAS to be false. Instead, a memory address assigned to a given level of interrupt is forced into the memory address register (MALDIT).

4-157. The forced memory address is used during the first interrupt service phase (phase 7) to store the program count into one of the first 64 locations in memory. To do this, the contents of the program counter register are gated into adder input gate A. When the sequence counter enters this phase (SCDC7), a carry is added to it to obtain straight transfer (ADINCRY), and the program count is loaded from the adder into the memory buffer register at the end of time period T1 by MBLDADLB and MBLDADRB. During the remainder of the machine cycle, the program count held in the memory buffer register is stored into memory. The forced address held by the memory address register is incremented by 2 automatically at the end of the store phase.

4-158. Entry into the store status phase of the interrupt service cycle (phase B) assembles a machine status word, consisting of the contents of the extension register (EXR00 through EXR04) and states of flip-flops ADFNEG, ADFEQL, ADGOVF, and CCFGLB, by gating these onto adder input gate B. A carry is gated to the adder (ADINCRY) to effect proper transfer, and the adder output is clocked into the memory buffer register at the end of time period T1. During the remainder of the machine cycle, the machine status word in the memory address register is then decremented by 1 automatically at the end of the machine cycle.

4-159. The last phase of the interrupt service cycle (phase D) initiates a memory read operation from the forced address location to load the memory buffer register with the initial, or linking, address of the first instruction of an interrupt level service routine. When the sequence counter enters phase D, the output of the memory buffer register is gated to adder input gate B (ADENMBL and ADENMBR), a carry is gated to the adder (ADINCRY) for proper transfer, and the adder output is gated into the inputs of the program counter register and the memory address register. The linking address is loaded into the memory buffer register from memory during time period T1 and is clocked into the program counter register (PCLDAD KKn-) and the memory address register (MALDAD T4 KKn-) at the end of time period T4. At this point, the sequence counter leaves the interrupt service cycle and enters phase 1 to fetch

and execute the first instruction of the interrupt service routine.

4-160. The last instruction in every interrupt level service routine is always an INR instruction, which allows the CPU to return to normal program execution. Detection of the INR instruction prepares the sequence counter to advance to phase 9 and preconditions a forced address at the memory address register inputs, in accordance with the interrupt level being serviced. At the end of time period T4, the sequence counter enters phase 9, and the forced address is loaded into the memory address register instead of the program count.

4-161. During phase 9, a memory read operation is performed to retrieve the machine status word stored during phase B of the preceding interrupt service cycle. By the end of time period T1, the status word is received into the memory buffer register. Signals ADENMBA and ADINCRY are true during phase 9 and gate the contents of the memory buffer register into adder input gate B and transfer the status word through the adder to reload the extension register (EXLDAD). Machine status flip-flops are reset at the end of time period T3, and all are set in accordance with the machine status word at the end of time period T4. Simultaneously, the forced address, decremented by two, is clocked into the memory address register to retrieve the initial program count from memory during the next machine cycle, and the sequence counter advances to phase 5.

4-162. Phase 5 is used to retrieve the program count stored during phase 7 of the interrupt service cycle. At the beginning of the machine cycle, a memory read operation is initiated which brings the program count into the memory buffer register. As in phase 9, signals ADENMBA and ADINCRY gate memory buffer register outputs into adder input gate B and activate the adder for direct transfer to the program counter and memory address register. At the end of the machine cycle, the program count is simultaneously loaded from the adder outputs into the program counter register (term SCDC5 INDC0 of PCLDAD) and into the memory address register term (CCFCLK CCCMENDA SCDC1- of MALDAD). The CPU is now essentially in the state it was prior to interrupt servicing, and processing will continue from that point.

4-163. Memory Manual Display and Entry.

4-164. During manual display or entry of memory, the CPU is halted, and the address of the next location in memory that will be accessed is contained in the program counter register and displayed by the PROGRAM COUNTER indicators. Note that this is not the address of the data presently displayed by the SELECTED DISPLAY indicators but the address of the next memory location that will be displayed or entered when the DISPLAY or ENTER switch is pressed.

4-165. Pressing either the DISPLAY or ENTER switch causes signal CPDIAEN to become true, making ADENPC true for one machine cycle. During this machine cycle, the memory location is accessed and the program counter is incremented to the next address in sequence.

4-166. Signal ADENPC gates the contents of the program counter register into adder input gate A, and the all 1's input of the disabled gate B cause the program count to be incremented by one (paragraph 4-241). At the end of time period T1, the adder output is clocked into the program counter register, and the incremented program count is loaded from the program counter register to the memory address register at the end of time period T4. This occurs before a new display or enter command can be produced in the control logic and ensures that the same memory location will not be addressed twice in succession.

4-167. CENTRAL PROCESSOR UNIT DATA FLOW

4-168. The details of data flow within the CPU are shown in figure 4-8. Control, sequencing, and timing signals used to control the flow of data within the CPU are omitted from the diagram for clarity. The diagram also shows the data paths between the CPU and other elements of the system: devices connected to the data input-output bus connector (DIOC), and devices connected to the direct memory access bus connector (DMAC), as well as core memory, the optional teletypewriter controller, etc.

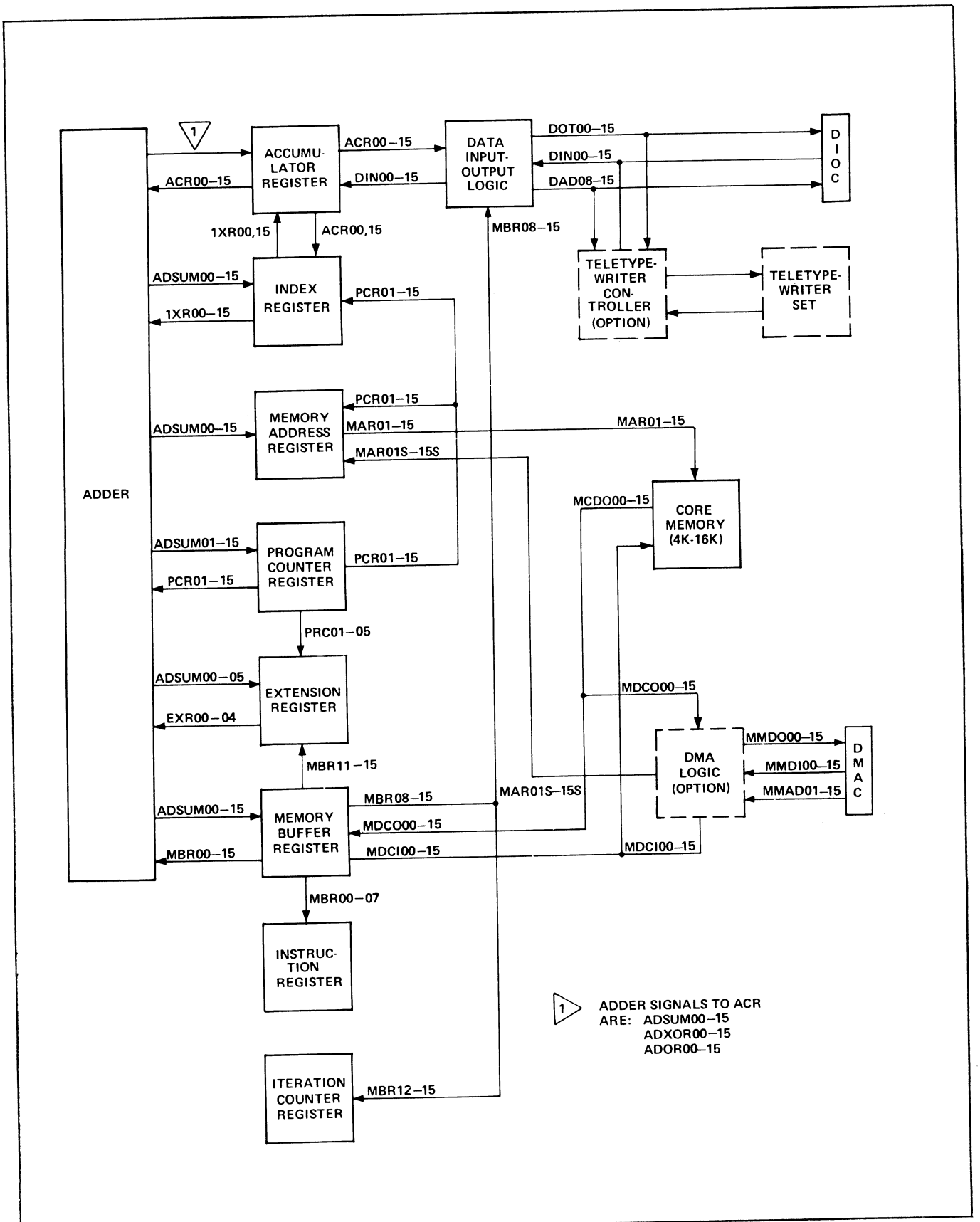


Figure 4-8. Central Processor Unit Data Flow Diagram

4-169. The teletypewriter set controller, while it may be physically housed with the CPU, is connected to the DIO bus and communicates with the CPU in the same manner as external devices on that bus. Operational theory of the teletypewriter set controller is discussed in paragraph 4-620.

4-170. Devices on the direct memory access bus communicate directly with the memory modules over the same lines that are used for communication between the CPU and the memory modules, if the DMA logic card is installed. Memory addressing and data transfer are discussed in paragraph 4-370. These discussions include the descriptions of the CPU elements primarily concerned with memory addressing and data transfer: the memory address register, memory module address logic, the extension register, the memory buffer register, memory data input-output logic, etc.

4-171. The instruction register and the program counter register are concerned with instruction and program execution and were discussed in paragraphs 4-88 and 4-131. The adder is used both as a central routing point in the transfer of data within the CPU and to perform the arithmetic and logical operations of the CPU. This unit is discussed in paragraph 4-220.

4-172. Data Input and Output

4-173. Two program instructions, DIN and DOT, control data transfer over the data input-output bus. Bits 08 through 15 of these instructions identify the device address and the function to be performed by the device selected by the address. Four bits each are used for the device address and for the function code, permitting up to 16 devices to be connected to the DIO bus and up to 16 different functions to be specified per device. Specific device addresses and function codes for external devices are discussed in the manuals covering the individual controllers. The teletypewriter set controller address and function codes are discussed in paragraph 4-655.

4-174. All signals on the DIO bus are negative-true (inverted). Eight inverting line drivers (Dwg 394562, Sht 9 and Dwg 394567, Sht 10) place the device address and function codes onto data address lines DAD08- through DAD15- from the memory buffer register (MBR08 through MBR15). Sixteen drivers place the contents of the accumulator register (ACR00 through ACR15) onto data output lines DOT00- through DOT15-. The inputs to these drivers are not gated, and the contents of the accumulator register and bits 08 through 15 of the memory buffer register are on the output lines at all times, regardless of whether or not a DIN or DOT operation is being performed. Random data on these lines is ignored by the device controllers.

4-175. Two machine cycles are required to execute either a DIN or DOT instruction. During the instruction fetch phase, the instruction is brought in from memory and is decoded. The instruction word is placed into the memory buffer register, and the device address and function code are placed on lines DAD08 through DAD15-. No other action takes place during the fetch phase.

4-176. The sequence counter enters the DIO phase (phase C) from the fetch phase, and data input strobe signal DISB- (SCDCC INDC02) or data output strobe signal DOSB- (SCDCC INDC03) is generated, depending upon the instruction being executed. The strobe command gates the device address and function code into the inputs of the device controller, and the addressed controller is actuated according to the function code.

4-177. If a DIN instruction is being executed, input strobe signal DISB- gates data from the addressed controller onto data input lines DIN00- through DIN15- (ACLDDI). The data signals are inverted to provide positive-true inputs (ACR00S through ACR15S) to the accumulator register. During time period T4 of the DIO phase, the accumulator register clock gates are enabled by ACCLKENBL and ACCLKENBR signals (SCDCC INDC02 T4), and data is loaded into the register as input strobe signal DISB- is terminated, at the end of DIO phase cycle.

4-178. Output data must be in the accumulator register before a DOT instruction is executed so that the data will be present on lines DOT00- through DOT15- when output strobe signal DOSB- is generated. The output data is gated into the addressed controller by the output strobe signal,

and the strobe signal is terminated at the end of time period T4 of the phase C cycle. The contents of the accumulator register are not affected by executing a DOT instruction.

4-179. Accumulator Register

4-180. The accumulator register contains 16 type-D flip-flops (ACR00 through ACR15) that operate in conjunction with the adder to form a conventional arithmetic accumulator. It is also used as a shift register, either alone in single-length shifts or in conjunction with the index register in double-length shifts. Input data from external devices is received by the accumulator register, and output data is transmitted from the accumulator register to external devices.

4-181. This register is contained on the four arithmetic cards with the four most-significant flip-flops on Arithmetic card 1 and four flip-flops on each of the other Arithmetic cards 2, 3, and 4 (Dwg 545497 — 500, Shts 8 and 9). Input gate and clock enabling signals are generated by logic contained primarily on the Instruction card (Dwg 394552, Sht 4).

4-182. The contents of the accumulator register are displayed on the SELECTED DISPLAY indicators when the DISPLAY SELECTOR switch is set to AC, and the SELECTED DISPLAY switches may be used to clear the register or alter its contents. Display-enter logic is discussed in paragraphs 4-75 and 4-80.

4-183. Signal ACRDR- is used to clear the accumulator register when the DISPLAY SELECTOR switch is set to AC and the CLEAR switch is pressed or system reset signal CCFRST is true. This signal is applied to the direct reset inputs of all register flip-flops, and the entire register is reset when the signal goes to ground. Signals ACR00DS- through ACR15DS- are for manual data entry and are applied to the direct set inputs of the register flip-flops, setting the flip-flops individually when the corresponding signal goes to ground.

4-184. The normal flow of data to the accumulator register is from the adder, and all data from other areas of the CPU (except data shifted in from the index register) must be routed through the adder to reach the accumulator register. Either full words (16 bits) or bytes (8 bits) may be transferred, but byte transfers are restricted to the right-hand byte (bits 08 through 15).

4-185. The accumulator receives three types of data from the adder: sum or transfer data (ADSUMn), logical-OR data (ADORn), and exclusive-OR data (ADXORn). These inputs are gated by enabling signals ACLDAD, ACLDOR, and ACLDXOR, respectively. With one exception (the AND instruction), these gating signals are mutually exclusive. When executing an AND instruction, the logical-AND function is obtained by gating logical-OR and exclusive-OR data into the accumulator simultaneously. This peculiarity is described in the adder logic discussion (paragraph 4-261).

4-186. Signal ACLDAD is true for load instructions LLB and LDB (T4SCDC1 INDC06 + T4SCDC5 IN5SC5); instructions LDW, ADD, and SUB [SCDC5 (INDC8 + INDCA + INDCB)]; and the data generic instructions CLR, CMP, INV, and CXA [T4SCDC1 INDC01 (INDCXX0 + INDCXX1 + INDCXX2 + INDCXX4)]; causing full word gating of adder sum outputs (ADSUM00- through ADSUM15-) to the accumulator register inputs. Signal ACLDOR is true for instructions ORI and AND only [SCDC5 (INDCC + INDCE)] and gates adder logical-OR outputs (ADOR00- through ADOR15-) to the accumulator register inputs. And signal ACLDXOR is true for instructions ORE and AND [SCDC5 (INDCD + INDCE)] and gates adder exclusive-OR outputs (ADXOR00- through ADXOR15-) to the accumulator register inputs.

4-187. None of the accumulator gated inputs is effective unless one or both of the clock enabling signals ACCLKENBL and ACCLKENBR is also true to gate the accumulator clock. These signals are byte oriented, with ACCLKENBL controlling the left-byte positions (bits 00 through 07) and ACCLKENBR controlling the right-byte positions (bits 08 through 15). Byte instructions LDB and LLB generate signal ACCLKENBR only. Consequently, only the right-hand byte of the full word presented to the adder will be loaded during these instructions. All other instructions mentioned generate both signals to permit both bytes to be

loaded. In all cases, clocking occurs at the end of time period T4 of the last (CCCMEND) cycle of the instruction.

4-188. Signal ACSHFT- of the accumulator clock logic (Dwg 394552, Sht 4) is false during the shift phase of all shift instructions, so long as the iteration count is not zero (SCDC4 ICDC0-), but the particular clock enable and input gating signals that are generated depend on the shift instruction being executed. Shift operations involve the index register, iteration counter, and other CPU elements as well as the accumulator register and are discussed separately in paragraph 4-207. The enabling of the accumulator register input gates and the shift control logic are covered in that discussion.

4-189. Data from the data input lines (DIN00- through DIN15-) is applied to the accumulator through gates controlled by signal ACLDDI, which is generated during the DIO phase of DIN instruction execution. This has been discussed previously in paragraph 4-177.

4-190. Index Register

4-191. The index register (Dwgs 545497 — 500, Sht 7) consists of 16 type-D flip-flops (IXR00 through IXR15) that serve a number of purposes. Its primary function is that of holding an address modifying operand used in the formation of an effective address when operating in indexed addressing modes. This use of the index register is discussed more thoroughly in paragraph 4-406.

4-192. This register is contained on the four Arithmetic cards with the four most-significant flip-flops located on Arithmetic card 1 and four flip-flops located on each of the other Arithmetic cards 2, 3, and 4. Input gating and clock enabling signals are generated by control logic contained primarily on the Adder Flip-Flop card (Dwg 394567, Sht 11).

4-193. The contents of the index register are displayed on the SELECTED DISPLAY indicators when the DISPLAY SELECTOR switch is set to IX, and the SELECTED DISPLAY switches may be used to clear the register or to alter its contents. Display-enter logic is discussed in paragraph 4-73.

4-194. Signal IXRDR- is used to clear the index register when the DISPLAY SELECTOR switch is set to IX and the CLEAR switch is pressed or system reset signal CCFRST is true. This signal is applied to the direct reset inputs of all register flip-flops, and the entire register is reset when the signal goes low. Signals IXR00DS- through IXR15DS- are for manual data and are applied to the direct set inputs of the register flip-flops, setting the flip-flops individually when the corresponding signal goes to ground.

4-195. The index register is loaded from the memory buffer register, from the accumulator, and from the extension register via the adder. The adder outputs (ADSUM00- through ADSUM15-) are also gated as index register inputs when the contents of the register are incremented or decremented by the literal generic instructions IXS and DXS.

4-196. Signals IXLDADL and IXLDADR control the gating of adder sum outputs to the index register, with the IXLDADL signal gating bits 00 through 04 and IXLDADR gating bits 05 through 15. Both adder sum gating signals are true during time period T4 of the fetch phase of copy accumulator instruction CAX, increment instruction IXS, and decrement instruction DXS [T4SCDC1 (INDC013 + INDC04 + INDC05)] and also during time period T4 of the read phase of the LDX memory load instruction (T4SCDC5 INDC9).

4-197. The only time signals IXLDADL and IXLDADR are not true simultaneously is during time period T4 of the fetch phase for the CEX copy extension register instruction (T4SCDC1 INDC006). In this case, only IXLDADL is true, gating the contents of the extension register from the adder into bits 00 through 04. Other bits of the index register remain unchanged.

4-198. Signal IXLDPC gates the contents of the program counter register directly into index register inputs during the T4 time period of the fetch phase for JSX jump instructions (T4 SCDC1 INDC2).

4-199. Shift control signals IXSL and IXSR enable data within the index register to be shifted left or

right during the execution of double-length shift operations, when the index register is effectively coupled to the accumulator register. Signal IXSL is true during the entire shift phase of all single- and double-length left shift instructions (SCDC4 MBR11 + IXSLOPT). Term IXSLOPT is for left-shift control by the hardware multiply-divide option and will normally be false unless this option is installed and active. Signal IXSR is true during the shift phase of all right-shift instructions (SCDC4 MBR11- + IXSROPT). Operational restraints by the index register clock enable signals prevent shifting during the execution of single-length shift instructions.

4-200. Clock enable signal IXCLKENBL controls the clock to bit 00 through 04 flip-flops, and signal IXCLKENBR controls the clock to the flip-flops for bits 05 through 15. Both signals are true to enable index register clocks during time period T4 of the fetch phase of CAX, IXS, DXS, and JSX instructions; during time period T4 of the read phase of the LDX instruction; and for the entire shift phase of double-length shift instructions SRA D, SLA D, SRL D, SLL D, SRC D, and SLC D. In addition, signal IXCLKENBL is true during time period T4 of the fetch phase of CEX instructions to copy extension register data into the first five bits of the index register.

4-201. Since all non-shift instructions cause the clock to be enabled only during time period T4 of the last (CCCMEND) phase of the instruction, the contents of the index register will only change once, at the end of time period T4 when the positive-going clocking edge occurs. However, clocks are enabled during the entire shift phase of double-length shift instructions until the iteration count reaches zero (SCDC4 MBR08- MBR10 ICDC0-). Consequently, shifting occurs at the end of each time period at a rate of five shifts per machine cycle. The details of double-length shifting are discussed more fully in paragraph 4-207.

4-202. Iteration Counter

4-203. The iteration counter is a 4-bit binary counter (Dwg 394562, Sht 8), consisting of four type J-K flip-flops (ICR0 through ICR3) located on the memory control card. Its primary function is to count the number of shift operations performed during the execution of a shift instruction and to generate a signal which will halt shifting after a prescribed number of shifts has taken place. It does this by copying an initial iteration count from the F2 field (bits 12 through 15) of the shift instruction during the fetch phase and counting down to zero during the shift phase. The 4-bit register length permits up to 15 shift iterations to be performed by any one shift instruction.

4-204. The counter is directly reset whenever the RESET switch is pressed and at the start of every fetch phase by a low level on reset line ICRST- (MRESET + SCDC1 T0 C1). The F2 field of every instruction fetched is copied from the memory buffer register (MBR12- through MBR15-) into the iteration counter at the end of time period T2 of the fetch phase (SCDC1 T2 C1), using direct set gates ICR0DS through ICR3DS enabled by ICLDMB-. The fact that the F2 field of all instructions fetched is copied into the iteration counter is taken advantage of during the execution of INR instructions, where the F2 field specifies the interrupt level when forcing memory addresses (paragraph 4-420). The contents of the memory buffer register is altered during the interrupt return phase, but the F2 field is still available in the iteration counter register for use in forming a second memory address during the phase.

4-205. If the instruction fetched happens to be a shift instruction, the sequence counter advances to the shift phase (phase 4), enabling the iteration counter clock gating signal ICDEC, unless the iteration count loaded was zero (SCDC4 ICDC0- + ICDECOPT). Term ICDECOPT is for control of the counter by options hardware multiply-divide logic.

4-206. KKIC iteration counter clocks occur at the end of each time period at a rate of five clocks per machine cycle. Each negative-going clocking edge decrements the iteration count by one. The algorithm for down counting is quite simple: the least-significant digit changes state every clock (flip-flop ICR3 toggles because of its open J-K inputs); higher order digits change state only if all lesser significant digits are zeros. When the count reaches zero (ICR0- ICR1- ICR2- ICR3-), signal

ICDC0 becomes true, stopping the iteration counter and register shifting. The true ICDC0 signal also conditions the sequence counter to leave the shift phase at the end of the next T4 time period.

4-207. Data Shifting

4-208. The 704 Processor has 30 shift instructions of the instruction code form 09 and 0A. These instructions are defined in the *704 User's Manual.* All single-length and byte shift instructions are performed in the accumulator register. For double-length shift instructions, the index register is coupled to the right, or least-significant, end of the accumulator register, and shifting occurs as though the two registers were one 32-bit register. Shifting may be done in either direction in circular or open-ended fashion, depending upon the type of shift instruction executed.

4-209. The number of shifts that will take place is governed by a number loaded into the iteration counter from the shift instruction word (paragraph 4-204) during the instruction fetch phase. The data is shifted one position and the iteration counter is decremented by one for each clock pulse. When the count reaches zero, shifting stops.

4-210. Shift instructions are of two types: arithmetic and logical. Arithmetic shifts may only be performed on the entire contents of the accumulator register (SLA and SRA instructions) or on the combined contents of the coupled accumulator and index registers (SLA D and SRA D instructions). Data flow during arithmetic shifts is shown in figure 4-9.

4-211. When a left-shift arithmetic instruction (SLA or SLA D) is fetched, adder overflow flip-flop ADFOVF (Dwg 394567, Sht 4) is reset at the end of time period T3 of the fetch phase (TIRC3 SCDC1 INDC09 MBR11) to act as a storage register for any changes in the sign bit (ACR00) that occur during the shift phase. During the shift operation, signal ADFOVFSD is true (SCDC4 ICDC0- INDC09 MBR11), enabling an ACR00, ACR01 bit comparator. Whenever these two bits differ (ACR00- ACR01 + ACR00 ACR01-), it is apparent that the next left shift will change the state of the sign bit. This condition makes ADFOVFS true, and the ADFOVF flip-flop is set by the next clock.

4-212. Setting flip-flop ADFOVF when the sign bit changes permits program testing for overflow, but has no other effect upon CPU operation or instruction execution. The sign bit cannot be altered in arithmetic right shifts, so no overflow detection is necessary for this case.

4-213. Execution of an arithmetic shift instruction causes certain shift control signals to be activated, as listed in table 4-1. These signals enable data transfer gates and register clock gates appropriate to the execution of the instruction. For example, instruction SLA activates signal ACSLENB which enables left-shift gates of the accumulator register (Dwg 545498, Sht 8), signal AC07SL which couples the high order of the accumulator right byte (ACR08) to the low order of the accumulator left byte (ACR07), and both clock enable signals (ACCLKENBL and ACCLKENBR). Signal ACSHFT- is false and active any time the sequence counter is in the shift phase (phase 4) and the iteration count is not zero (SCDC4 ICDC0-), disabling the clocks when it goes false.

4-214. When double-length instruction SLA D is executed, signals IXSL, IXSLZRO, IXCLKENBL, and IXCLKENBR for index register control are activated in addition to those accumulator control signals activated by an SLA instruction. Signal IXSL enables the index register left-shift gates, signal IXSLZRO applies a constant zero to least-significant bit flip-flop IXR15 for shifting into vacated positions, and signals IXCLKENBL and IXCLKENBR enable the index register clocks for shifting. Arithmetic right shift instructions are executed similarly except that signals ACSRENB, AC08SR, and IXSR are generated instead of ACSLENB, AC07SL, and IXSL, respectively, to enable right-shift gating.

4-215. Logical shifts may be performed on either byte content of the accumulator register, on the entire content of the accumulator register, or on the combined content of the coupled accumulator and index registers. Data flow during right, left, and circular logical shifts is shown in figure 4-10.

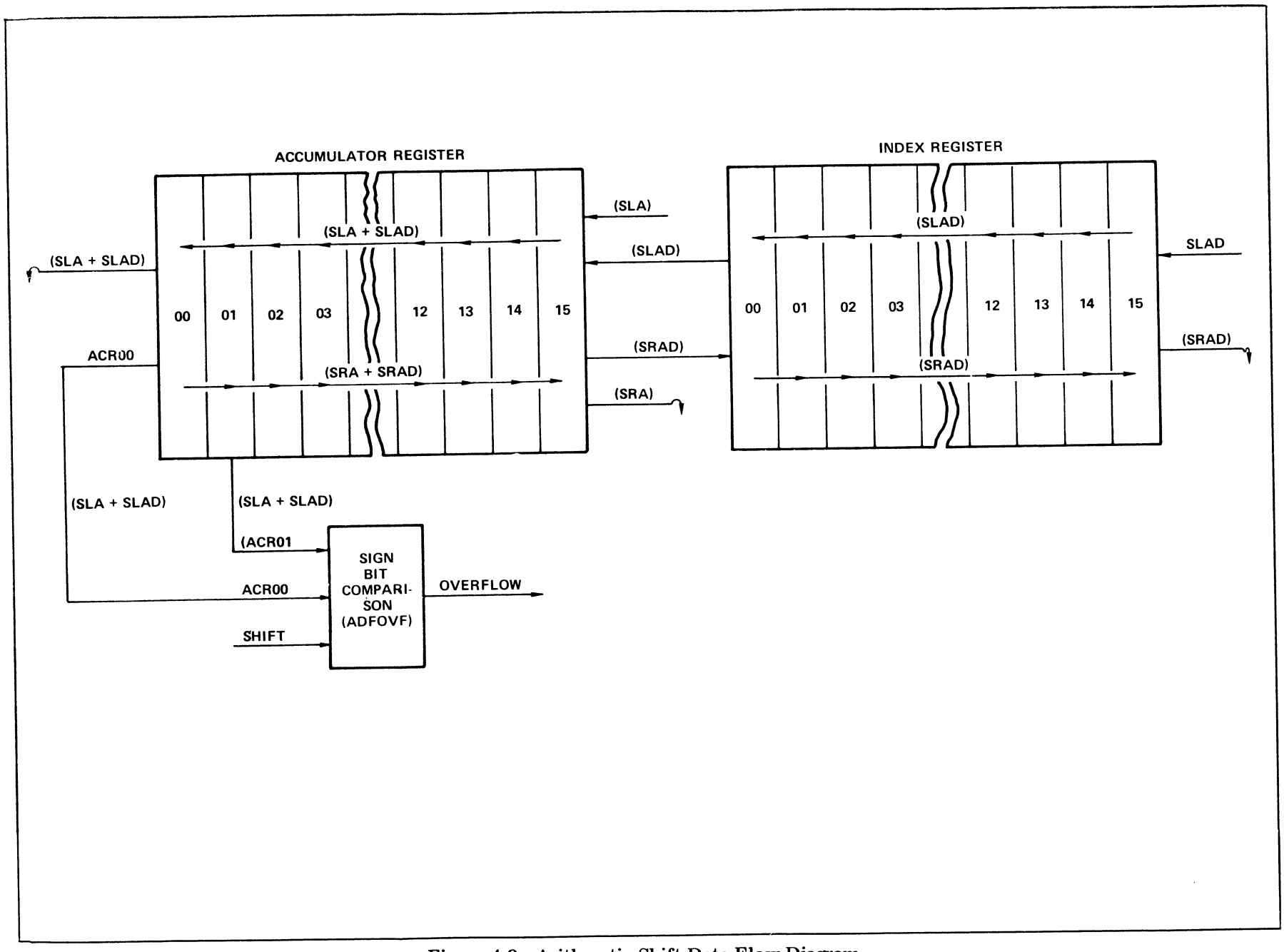


Figure 4-9. Arithmetic Shift Data Flow Diagram

Table 4-1. Shift Control Signals Activated by Shift Instructions

Shift Control Signal	Shift Instruction																			
	SLA	SLA D	SLL	SLL D	SLL L	SLL R	SLC	SLC D	SLC L	SLC R	SRA	SRA D	SRL	SRL D	SRL L	SRL R	SRC	SRC D	SRC L	SRC R
ACSLENB	1	1	1	1	1	1	1	1	1	1										
ACSRENB											1	1	1	1	1	1	1	1	1	1
AC07SL	1	1	1	1			1	1												
AC08SR											1	1	1	1			1	1		
AC00SRCD																		1		
ACSHFT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ACCLKENBL	1	1	1	1	1		1	1	1		1	1	1	1	1		1	1	1	
ACCLKENBR	1	1	1	1		1	1	1		1	1	1	1	1		1	1	1		1
IXSL	X	1	X	1	X	X	X	1	X	X										
IXSR											X	1	X	1	X	X	X	1	X	X
IXSLCDA								1												
IXSLZRO		1		1																
IXCLKENBL		1		1				1				1		1				1		
IXCLKENBR		1		1				1				1		1				1		

1 = Signal is True and Active During Shift Instruction

X = Signal is True but not Effective During Shift Instruction

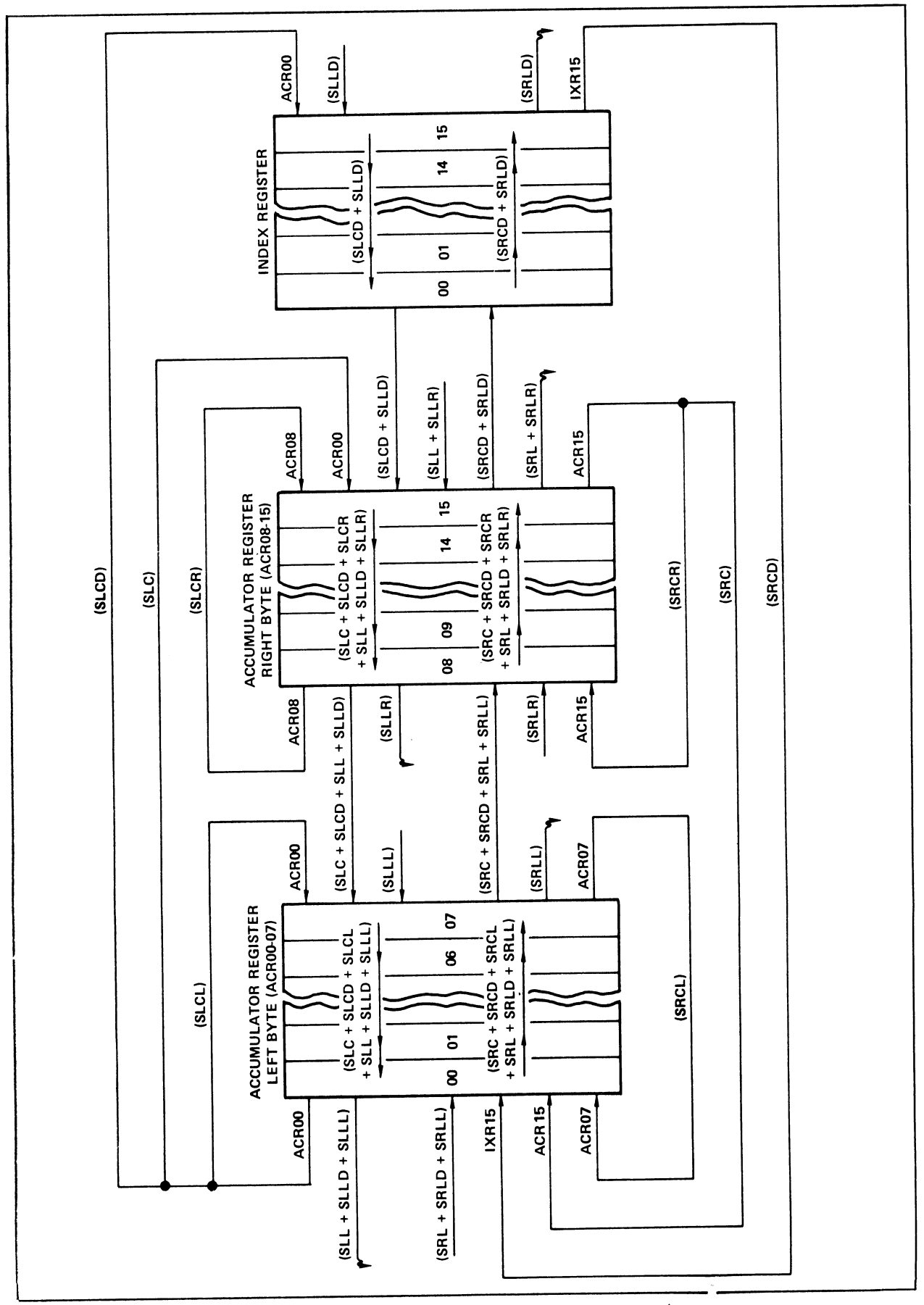


Figure 4-10. Logical Shift Data Flow Diagram

4-217. As in arithmetic shifting, signal ACSHFT- is false during the shift phase of logical shift instruction execution so long as the count in the iteration counter is not zero. This tends to enable the entire accumulator register clock system, but is modified, depending on the specific shift instruction being executed. Signals AC07SL, AC08SR, and ACCLKENBL are inhibited if a right-byte shift instruction SRL R, SLL R, SRC R, or SLC R is being executed. Similarly, signals AC07SL, AC08SR, and ACCLKENBR are inhibited if a left-byte shift instruction SRL L, SLL L, SRC L, or SLC L is being executed.

4-218. Index register right-shift gate control signal IXSR is activated by all arithmetic and logical right-shift instructions (SCDC4 MBR11-), regardless of the single- or double-length nature of the instruction being executed. The same is true of left-shift gate control signal IXSL; it is activated by all left-shift instructions. This enabling of index register shift gates during the execution of single-length shift instructions is redundant, but the clock enable signals IXCLKENBR and IXCLKENBL are both inactive at this time, so no change occurs in the index register content.

4-219. The shift control signals actuated by each logical shift instruction are also given in table 4-1. Shift control logic for the accumulator register is shown in Dwg 394552 and in Dwg 394567 for the index register.

4-220. ARITHMETIC AND LOGICAL OPERATIONS

4-221. All arithmetic and logical operations are performed by the CPU adder, which also serves as a central routing point for the transfer of data within the CPU. All CPU registers except the instruction and iteration counter registers communicate with the adder. In only a few cases is data transferred directly between registers without using the adder. Data flow in the CPU is discussed in paragraph 4-167, and the CPU data flow paths are shown in figure 4-8. The adder is also used to assemble memory addresses, which may or may not also involve an arithmetic operation. This function is discussed in detail in paragraph 4-406. Data flow to, within, and from the adder is shown in figure 4-11. The adder control logic is omitted from the diagram for clarity.

4-222. Adder Input Logic

4-223. The adder input gate A and gate B control logic (Dwg 394552) controls the selection and timing of inputs to adder input gates A and B (Dwgs 545497 — 500). Adder gates are contained on the four Arithmetic cards with the four most-significant-bit gates located on Arithmetic card 1 and four bit gates located on each of the other Arithmetic cards 2, 3, and 4. Adder input gate control logic is located on the Instruction card.

4-224. Time periods T0 and T1 (TIRCA true) of each instruction fetch phase preempt the use of the adder to increment the program count. Those instructions fetched that require access to the adder during their fetch phase are limited to its use only during time periods T2, T3, and T4 (condition SCDC1 TIRCA- true), when signal TBDC1 is active. This signal is seen repeatedly in the logic for adder input gate A and B control signals (Dwg 394532, Sht 6).

4-225. Still other functions that require the use of the adder may be performed during phases other than the fetch phase of an instruction's execution cycle. In some cases, adder input gate control signals will be activated by the sequence counter entering a particular phase, without regard to the instruction that caused the transition. In others, control signal activation is in response to specific instructions, and even these may be dependent upon some prior condition being true. Instead of a lengthy discussion of the functional significance of each term, the adder input control signals are listed in table 4-2 with the conditions and instructions that activate them. These functions are described in detail in the discussions of program execution, memory address formation, and the execution of specific instructions.

4-226. The adder input gate A logic (ADA00- through ADA15-) provides inverted (negative-true) data from the normal accumulator register outputs (ACR00 through ACR15, controlled by signal ADENAC), from the inverted accumulator register

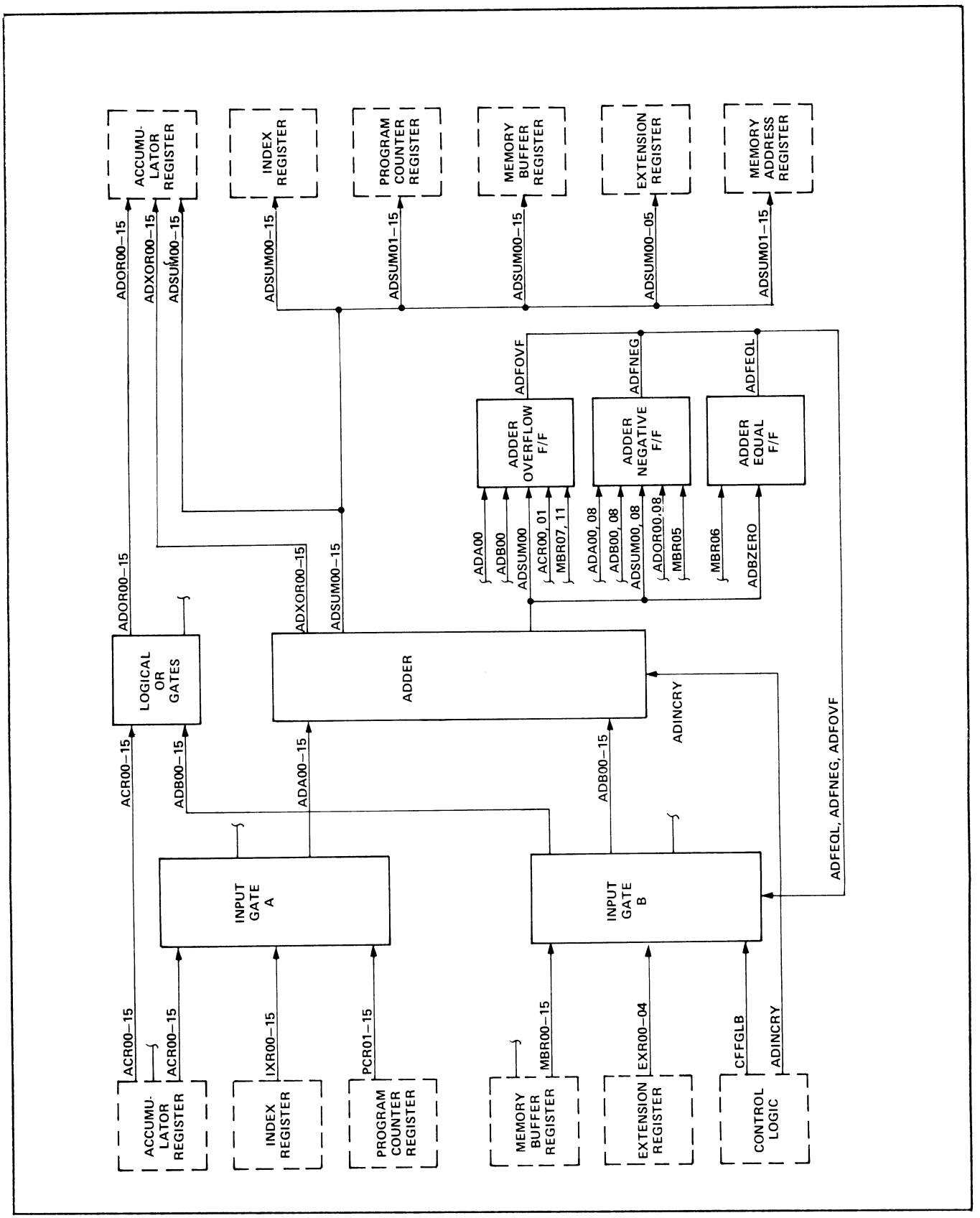


Figure 4-11. Adder Data Flow Diagram

Table 4-2. Adder Input Gate Control Signal Activating Conditions

A-Gate Control Signal	Conditions and Instructions
ADENAC	*Fetch Phase Transfer (SCDC1 TIRCA-):* CAX, CLB *Write Phase Store (SCDC3):* STB (CCFBYTE), STW *Read Phase Transfer (SCDC5):* ADD, AND, CMB, CMW, SUB
ADENACC	*Fetch Phase Complement (SCDC1 TIRCA-):* CMP, INV *Read Phase Complement (SCDC5):* ORE
ADENIX	*Fetch Phase Transfer (SCDC1 TIRCA-):* CXA, CXE, DXS, IXS *Index Operand (SCDC1 TIRCA- MBR04):* ADD, AND, CMB, CMW, JMP, JSX, LDB, LDW, LDX, ORE, ORI, STB, STW, STX, SUB *Write Phase Store (SCDC3):* STX
ADENPC	*Automatic PCR Increment:* SCDC1 TIRCA *Conditional Skip Increment (SCDC1 TIRCA-):* SAM, SAP, SAO, SAZ, SEQ, SGR, SLE, SLS, SNE, SNO, SS0, SS1, SS2, SS3, SSE, SXE *Interrupt PCR Store:* SCDC7 *Manual PCR Increment:* CPDIAEN CCFSYN1 *DXS or IXS Skip Increment:* SCDCC
ADENACRB	*Write Phase Store (SCDC3):* STB (CCFBYTE-)
B-Gate Control Signal	**Conditions and Instructions**
ADENMBL	*Fetch Phase Transfer (SCDC1 TIRCA-):* LLB *Read Phase Transfer (SCDC5):* ADD, AND, INR, LDB (CCFBYTE), LDW, LDX, ORE, ORI *Interrupt Return Transfer (SCDC9):* INR *Interrupt Load Link:* SCDCD

Table 4-2. Adder Input Gate Control Signal Activating Conditions (Cont)

B-Gate Control Signal	Conditions and Instructions
ADENMBR	*All Word Transfers:* ADENMBL *Fetch Phase Transfer (SCDC1 TIRCA-):* ADD, AND, CMB, CMW, IXS, JMP, JSX, LDB, LDW, LDX, ORE, ORI, STB, STW, STX, SUB
ADENMBC	*Fetch Phase Complement (SCDC1 TIRCA-):* CLB, DXS *Read Phase Complement (SCDC5):* CMB (CCFBYTE), CMW, SUB
ADENEXB	*Fetch Phase Transfer (SCDC1 TIRCA-):* CEX *Byte Addressing (SCDC1 TIRCA- (CCFGLB- + MBR04-)):* CMB, LDB, STB *Interrupt Store Status Address:* SCDCB
ADENEXW	*Word Addressing (SCDC1 TIRCA- (CCFGLB- + MBR04-)):* ADD, AND, CMW, JMP, JSX (MBR04-), LDW, LDX, ORE, ORI, STW, STX, SUB
ADENMBB	*Read Phase Transfer (SCDC5):* LDB (CCFBYTE-)
ADENMBBC	*Read Phase Complement (SCDC5):* CMB (CCFBYTE-)
ADONES	*Forced Ones (SCDC1 TIRCA-):* DXS
Adder Control Signal	**Conditions and Instructions**
ADINCRY	*Fetch Phase Carry (SCDC1 TIRCA-):* ADD, AND, CAX, CEX, CLR, CMB, CMW, CXA, CXE, INV, IXS, JMP, JSX, LDB, LDW, LDX, LLB, ORE, ORI, STB, STW, STX, SUB *Write Phase Carry (SCDC3):* STB, STW, STX *Read Phase Carry (SCDC5):* ADD, INR, LDB, LDW, LDX *Interrupt PCR Store:* SCDC7 *Interrupt Return (SCDC9):* INR *Interrupt Status Store:* SCDCB *Interrupt Load Link:* SCDCD

outputs (ACR00- through ACR15-, controlled by signal ADENACC), from the index register outputs (IXR00 through IXR15, controlled by signal ADENIX), and from the program counter register outputs (PCR01 through PCR15, controlled by ADENPC). In addition, the left byte input gates (ADA00- through ADA07-) have the capability of transferring accumulator register right-byte data (ACR08 through ACR15, controlled by ADENACRB).

4-227. The adder input gate B logic (ADB00- through ADB15-) provides inverted (negative-true) data from the left and/or right byte memory buffer register normal outputs (MBR00 through MBR07, controlled by ADENMBL; MBR08 through MBR15, controlled by ADENMBR), from the memory buffer register inverted outputs (MBR00- through MBR15-, controlled by ADENMBC), from the extension register outputs (EXR00 through EXR04, controlled by signals ADENEXB and ADENEXW), and from the various control and adder status flip-flops (ADFEQL, ADFNEG, ADFOVF, and CFFGLB, controlled by SCDCB). In addition, the right byte input gates (ADB08- through ADB15-) have the capability of transferring memory buffer register left-byte data (MBR00 through MBR07, controlled by signal ADENMBB) and inverted left-byte data (MBR00- through MBR07-, controlled by signal ADENMBBC).

4-228. The Adder

4-229. The adder employed in the 704 Processor (Dwgs 545497 — 500, Sht 10) consists of eight 2-bit, full-adder integrated circuits — two on each of the four Arithmetic cards. These operate with the negative-true outputs of adder input gate A (ADA00- through ADA15-) and adder input gate B (ADB00- through ADB15-) and provide negative-true summation outputs (ADSUM00- through ADSUM15-), negative-true exclusive-OR outputs (ADXOR00- through ADXOR15-), and positive-true carry outputs for "external" interconnection (ADC00, ADC02, ADC04, etc). Using rules appropriate to 1's complement arithmetic and logic, this adder is capable of performing normal addition, subtraction, increment-by-one, transfer, 2's-complement, inversion, exclusive-OR, inclusive-OR, and logical-AND operations.

4-230. This adder propagates carrys sequentially from the less-significant end, in the simplest manner possible. Under worst-case conditions, where a carry must be propagated from the least-significant bit to the most-significant bit position, total delay will not exceed 400 ns (or two 1-μs memory time periods).

4-231. Addition

4-232. Execution of the ADD instruction, and any other operation that brings two numerical quantities together for summation, causes one quantity (usually the contents of the accumulator register) to be applied to the adder through input gate A and the other quantity (usually the contents of the memory buffer register) to be applied to the adder through input gate B. Since both of these input gates invert data passing through them, the adder can be thought of as operating with 1's-complement numbers rather than with negative-true numbers. The problem then resolves to obtaining the correct summation at the adder sum outputs in 1's complement form.

4-233. Whenever two 1's-complement numbers are added together, the sum is always excess one, in terms of 1's-complement numbers. For example, if the 1's complement of 9 (0110) is added to the 1's complement of 3 (1100), the binary sum is 0010 with an extraneous carry. This is the 1's complement of 13. It is necessary somehow to subtract 1 from (or add -1 to) the simple sum of A and B. In complementary arithmetic, this can be done by adding 1 to the least-significant digit of the sum. Signal ADINCRY, a carry into the least-significant bit adder, will do this and is always true when addition is being performed. Making the ADINCRY signal true is equivalent to adding -1 to the 1's complement summation, regardless of the function being performed by the adder.

4-234. Adder sum outputs (ADSUM00- through ADSUM15-) are gated to their destination (usually the input of the accumulator register) during time period T4 of the last machine cycle of instruction execution and is clocked in at the end of the time period. Since stable data should be available to the adder inputs no later than the middle of time period T2, the adder outputs will have settled long before clocking of the adder output occurs.

4-235. Operands are treated as signed 16-bit binary numbers, and the algebraic sum of the numbers is formed when they are added. If two numbers of like sign are added, the magnitude of their sum may become too large for the register length (greater than 2^{15}-1 or less than -2^{15}). If this occurs, the overflow from the most-significant magnitude bit (ADSUM01) will cause the sign bit (ADSUM00) to be different from the sign bits of the two numbers (ADA00 and ADB00).

4-236. Adder overflow is detected by overflow flip-flop ADFOVF control logic (Dwg 394567, Sht 4). The flip-flop is reset at the end of time period T3 of the read memory phase for ADD and SUB instructions (SCDC5 INDCAORB TIRC3). Overflow is detected when two positively-signed numbers generate a negatively-signed sum (ADA00 ADB00 ADSUM00-) or when two negatively-signed numbers generate a positively-signed sum (ADA00- ADB00- ADSUM00). In either case, overflow set signal ADFOVFS will be true, and flip-flop ADFOVF is set by the next clock at the end of time period T4.

4-237. Subtraction

4-238. Execution of the SUB instruction, and any other decrementing operation that brings two numerical quantities together for subtraction, causes the minuend (usually from the accumulator register) to be applied to the adder through input gate A and the subtrahend (usually from the memory buffer register) to be applied to the adder through input gate B. Furthermore, the inverse outputs of the subtrahend source are gated so that the adder "sees" the subtrahend in normal (non-inverted) form.

4-239. Whenever the 1's complement of one number is added to the normal form of another number, the sum is always the 1's complement of their difference. For example, if the 1's complement of 9 (0110) is added to the normal form of 3 (0011), the binary sum is 1001 with an extraneous carry. This is the 1's complement of 6. The ADINCRY signal is not required to effect 1's-complement subtraction and will be false during all decrementing operations.

4-240. Adder sum outputs are gated and clocked into their destination register in the same manner as the addition operation. When a SUB instruction is executed, the overflow logic will be enabled and flip-flop ADFOVF will be set if a sign change is detected, according to the rules previously mentioned. It is necessary to remember, however, that it is the signs of the 1's complement minuend and the normal form subtrahend that are being compared to detect overflow. Overflow occurs when a negative number is subtracted from a positive number and the result is greater than 2^{15} -1 (ADA00- ADB00- ADSUM00) or when a positive number is subtracted from a negative number and the result is less than -2^{15} (ADA00 ADB00 ADSUM00-).

4-241. Increment By One

4-242. The program counter uses the adder to increment the program count by one during time period T0 and T1 of each fetch phase and conditionally to increment it for program skips. This has been discussed in paragraph 4-126. Any time a 1 is to be added to the program count, signal ADENPC gates the contents of the program counter register to adder input gate A. No operand is applied to adder input gate B, making its input, in effect, zero. Since the adder input gates invert, the 1's complement of the program count will be added to the 1's complement of 0 (all 1's).

4-243. According to the rules of 1's complement addition given in paragraph 4-231, the sum is always excess one. For example, assume that the program count is 14. If the 1's complement of 14 (0001) is added to the 1's complement of 0 (1111), the binary sum is 0000 with an extraneous carry. This is the 1's complement of 15. The ADINCRY signal serves no purpose in the increment-by-one function and will be false during this operation. Also, the overflow detector is not enabled, since overflow is meaningless.

4-244. Data Transfer

4-245. Memory load and store operations require data to be transferred from the memory buffer register to the accumulator register, or the other

way around, using the adder as a vehicle for transfer. The adder input gate A is used as the data input when the accumulator register is the source, and gate B is used when the memory buffer register is the source. Only one adder input gate will be used at a time, and the adder will see all 1's from the unused gate (1's complement of zero).

4-246. The same type of data transfer operation is performed during copy instructions, where the adder is involved. In all cases, data transfer is similar to an increment-by-one operation (paragraph 4-241), inasmuch as the 1's complement of the transferred data is received by the adder from one input gate and the 1's complement of zero is received from the other input gate. However, since an unincremented output is needed, signal ADINCRY is made true during data transfer operations to add -1 to the 1's complement sum.

4-247. As an example, assume a CAX instruction is being executed wherein the number 5 in the accumulator is to be copied into the index register. The output of the accumulator (0101) is gated to adder input gate A, which inverts it (1010) and applies it to the adder. The binary sum of all data applied by the adder input gates and by the ADINCRY signal activated carry (1010 + 1111 + 0001) is 1010, with an extraneous carry. This 1's complement ADSUM- output is inverted by the activated index register input gates (0101), so that the data copied by the register is the same as the original accumulator register output.

4-248. Complementing

4-249. Execution of a CMP instruction causes the 2's complement of the accumulator register content to be formed and placed back into the accumulator register. Complements are also formed during subtraction, comparison, and decrementing operations and are performed similarly. The 2's complement of any number is formed by adding 1 to the 1's complement of the number.

4-250. As an example of the complement operation, assume that a CMP instruction is being executed wherein the number 6 is the original content of the accumulator. Signal ADENACC generated by this instruction gates the inverted outputs of the accumulator register (1001) to adder input gate A, where they are inverted once again (0110). The inactive adder input gate B provides the 1's complement of zero (1111) to the adder. Since the excess-one rule for 1's complement adder operation applies, the addition of 1 to the sum is automatic, and the ADSUM- output (0101) is the 2's complement of 1001 inverted. Restoration occurs at the accumulator register input, where the activated gates invert the data received from the adder when it is copied by the register.

4-251. During the execution of a CMP instruction, overflow is detected by flip-flop ADFOVF. The flip-flop is reset at the end of time period T3 of the instruction (INDC011 SCDC1 TIRC3). If the 2's complement of -2^{15} is formed, the flip-flop is set at the end of time period T4 (INDC011 T4SCDC1 ADOVFSD). No overflow is possible when the 2's complement of any number greater than -2^{15} is formed.

4-252. Inverting

4-253. Execution of an INV instruction causes the 1's complement of the accumulator register content to be formed and placed back into the accumulator register. The 1's complement of any number is obtained when a straight bit-by-bit inversion is performed upon the number.

4-254. As an example, assume that an INV instruction is executed wherein the number 5 is in the accumulator register. Signal ADENACC generated by this instruction gates the inverted outputs of the accumulator register (1010) to adder input gate A, where they are inverted once again (0101). The inactive adder input gate B provides the 1's complement of zero (1111) to the adder. Since the excess-one rule for 1's complement addition applies, the ADINCRY signal is made true to effectively add -1 to the output sum. Binary addition of the data at the input gates plus the carry applied by signal ADINCRY (0101 + 1111 + 0001) provides an ADSUM- output of 0101, with an extraneous carry. Inversion at the accumulator register input gates causes the accumulator register to copy 1010, the 1's complement of the binary number 5. Overflow flip-flop activity is disabled during the execution of this instruction.

4-255. Exclusive OR

4-256. The adder circuits are used to make exclusive-OR comparisons between like bits of the contents of the accumulator and memory buffer registers, during the execution of the ORE instruction. Signal ADENACC gates the inverted outputs of the accumulator register to adder input gate A, and signals ADENMBL and ADENMBR gate the normal outputs of the memory buffer register to adder input B. The 1's complement of the results appear at the ADXOR- outputs of the adder and are copied back into the accumulator at the end of the machine cycle after being inverted by the accumulator register input gates.

4-257. Assume that the accumulator register holds the number 0101, the memory buffer register holds the number 0011, and the sequence counter advances to the read phase of an ORE instruction. Inverted data from the accumulator register (1010) appears in normal form at the output of adder gate A (0101), and normal data from the memory buffer register (0011) appears in inverted form at the output of adder gate B (1100). The exclusive-OR logical output at the adder ADXOR- outputs will be 1001 (that is, 0101 $\oplus$ 1100), which is the inverse of the normal exclusive-OR logical resultants 0110 (which is 0101 $\oplus$ 0011).

4-258. Inclusive OR

4-259. The inclusive, or common logical-OR function cannot be performed using the 1's complement adder circuits. Instead, 16 positive-true AND gates used as negative-true OR gates (ADOR00- through ADOR15-; Dwgs 545497 — 500) perform this function. These gates receive the inverted outputs of the accumulator register (ACR00- through ACR15-) and the outputs of the adder input B gates (ADB00- through ADB15-) at all times, even though the outputs produced by the gates are used only during the execution of ORI and AND instructions.

4-260. When logical-OR instruction ORI is executed, signals ADENMBL and ADENMBR gate the normal outputs of the memory buffer register to adder input gate B. OR logic gates ADOR00- through ADOR15- then produce a bit-by-bit resultant in inverted form. For example, if the accumulator holds the number 0101 (applying 1010 to the logical-OR gates) and the memory buffer register holds the number 0011 (applying 1100 to the logical-OR gates), the resultant gate output will be 1000 (logical-AND of 1010 and 1100). The inverse of this (011, which is the logical-OR of 0101 and 0011) is copied back into the accumulator at the end of the machine cycle.

4-261. Logical AND

4-262. Execution of the AND instruction causes the logical product of the accumulator register and memory buffer register contents to replace the content of the accumulator. To do this, signal ADENAC gates the normal outputs of the accumulator register to adder input gate A, and signals ADENMBL and ADENMBR gate the normal outputs of the memory buffer register to adder input gate B. By simultaneously gating ADXOR data from the adder and ADOR data from the logical-OR gates into the accumulator, the logical-AND function will result.

4-263. Without going into the various inversions of the gating actually used, it can be shown through Boolean manipulation that the logical product of two classes, A and B, is equivalent to the intersection of their mutually inclusive class and the class that is not exclusively A or B. That is to say, $AB = (A + B)\ \overline{(A \oplus B)}$. The proof that this is a Boolean identity follows:

$$
\begin{aligned}
AB &= (A + B)\ \overline{(A \oplus B)} \\
&= (A + B)\ \overline{(A + B)\ \overline{AB}} \\
&= (A + B)\ \overline{(\overline{A + B} + AB)} \\
&= (A + B)\ AB \\
AB &\equiv AB
\end{aligned}
$$

4-264. Now consider a typical case of logical-AND processing where the content of the accumulator is 0101 and the content of the memory buffer register is 0011. Clearly the logical product (AND intersection) of these two is 0001. Let's follow the operands from their sources through the ADOR and ADXOR logic back to the accumulator to see how this resultant is produced.

4-265. Normal data from the accumulator register

(0101) is inverted by adder input gate A (ADA- output is 1010), and normal data from the memory buffer register (0011) is inverted by adder input gate B (ADB- output is 1100). The adder takes these two inverted operands and provides an exclusive-OR resultant at its ADXOR- outputs (0110). This 0110 output is one of the resultants gated back into the accumulator.

4-266. Simultaneously, the ADOR- gates are monitoring inverted data from the accumulator register (1010) and the outputs of the adder input B gates (1100). In positive-true logic terms, the ADOR- gates are AND gates, and their outputs will be the logical product of their inputs (1000). This 1000 output is the other resultant gated back into the accumulator.

4-267. During the memory read phase of AND instruction execution, both ACLDOR and ACLDXOR accumulator input gate control signals are made true to transfer ADOR- and ADXOR- resultants to the accumulator set inputs simultaneously. The inverting nature of these positive-true NAND gates is such that a logical 1 will be applied to any given accumulator register flip-flop only if its corresponding ADOR- and ADXOR- inputs are both logical 0. So the 1000 and 0110 simultaneous inputs establish a resultant 0001 pattern that is clocked into the accumulator at the end of the read phase machine cycle. This is the logical product of the initial operands 0101 and 0011.

4-268. Comparisons

4-269. Comparisons are performed by subtracting a word or byte from a word or byte stored in the accumulator register and noting whether the difference is positive, zero, or negative. The result indicates whether the quantity subtracted is less than, equal to, or greater than the quantity stored in the accumulator register.

4-270. Three instructions are used for comparisons. The CLB instruction compares a literal contained in bits 08 through 15 of the instruction with the contents of bits 08 through 15 of the accumulator register. The CMB instruction compares a byte from memory to the contents of bits 08 through 15 of the accumulator register, and the CMW instruction compares a word from memory with the entire contents of the accumulator register.

4-271. The CLB instruction is executed in one machine cycle. During the last half (time periods T2, T3, and T4) of the instruction fetch phase, signal ADENAC gates the contents of the accumulator register (ACR00 through ACR15) into adder input gate A, and signal ADENMBC gates the inverse outputs of the memory buffer register (MBR00- through MBR15-) into adder input gate B. This subtracts the entire instruction word from the contents of the entire accumulator register, but only bits 08 through 15 are used in the comparison logic.

4-272. The CMB and CMW instructions require two machine cycles. During the instruction fetch phase, a byte or word address is formed using the memory address field of the instruction (paragraph 4-406). This address is used in the read phase which follows to read in a byte or word from memory for comparison with the accumulator register contents.

4-273. During the read phase, signal ADENAC gates the content of the accumulator register into adder input gate A. The CMB instruction reads in the entire word containing the addressed byte, and the state of byte control flip-flop CCFBYTE determines which of the bytes will be used. If the left byte is addressed (CCFBYTE-), signal ADENMBBC gates the inverse outputs of the memory buffer register left byte (MBR00- through MBR07-) into adder input gate B. If the right byte is addressed (CCFBYTE) or a CMW instruction is being executed, signal ADENMBC gates the inverse outputs of the entire memory buffer register into adder input gate B.

4-274. For comparison, bytes are treated as signed 8-bit binary numbers (bit 08 is sign bit), and words are treated as signed 16-bit binary numbers (bit 00 is sign bit). When the algebraic difference between the quantities is obtained, the comparison logic (Dwg 394567, Sht 5) examines the difference at the adder output for a value of zero (equality) and also the byte or word sign bits, as applicable, for the direction of inequality.

4-275. The results of the comparison are stored in adder-equal flip-flop ADFEQL and in adder-negative flip-flop ADFNEG. Both flip-flops are reset at the end of time period T3 of the fetch phase for CLB instructions and of the read phase for CMB and CMW instructions. If both flip-flops ADFEQL and ADFNEG remain reset at the end of time period T4, when the comparison is made, the difference is not zero and is positive. This indicates that the quantity in the accumulator register is greater than the quantity in the memory buffer register.

4-276. Flip-flop ADFEQL is set at the end of time period T4, if the subtrahend and minuend are equal, making the adder sum outputs zero. Signal ADRBZERO is true if adder sum outputs ADSUM08- through ADSUM15- are all true and will cause the ADFEQL flip-flop to be set during CLB instructions (IN07SC1 ADRBZERO TIRC4) and CMB instructions (IN4SC5 ADRBZERO TIRC4). Signal ADBZERO0 is true if adder sum outputs ADSUM00- through ADSUM03- are true, and signal ADBZERO4 is true if adder sum outputs ADSUM04- through ADSUM07- are true. The signals, combined with ADRBZERO for bits 08 through 15, must be true to set the ADFEQL flip-flop when executing a CMW instruction (INFSC5 ADBZERO0 ADBZER04 ADRBZERO TIRC4).

4-277. Flip-flop ADFNEG is set at the end of time period T4, if the subtrahend (memory buffer register content) has a more positive algebraic value than the minuend (accumulator register content). Clearly this is the case whenever the sign of the subtrahend is negative and the sign of the minuend is positive. This condition is detected by comparing the sign bits at the adder inputs (ADA00 with ADB00 for CMW instructions and ADA08 with ADB08 for CLB and CMB instructions). Because of subtrahend inversion, if both bits are 1's, the minuend is negative and the subtrahend is positive, and the remainder is always negative.

4-278. Whenever the signs of both minuend and subtrahend are the same, the sign of their difference must be determined by the results of actual subtractive comparison. If both signs are positive, the resultant is negative when the magnitude of the accumulator register content is less than the memory buffer register content. Conversely, if both signs are negative, the resultant is negative when the magnitude of the accumulator register content is greater than the memory buffer register content. This condition is detected by comparing adder output sign bit resultants (ADSUM00 with ADOR00 for CMW instructions and ADSUM08 with ADOR08 for CLB and CMB instructions). If both bits are 1's, the minuend is negative with respect to the subtrahend, and the ADFNEG flip-flop is set to reflect this state.

4-279. The results of a comparison may be tested by program instructions SEQ, SGR, SLE, SLS, and SNE. A program skip will occur if the tested condition is true (paragraph 4-139).

4-280. HARDWARE MULTIPLY-DIVIDE OPTION

4-281. The multiply-divide option, in machines so equipped, permits the direct multiplication or division of two numbers by executing single instructions rather than multi-instruction multiply or divide subroutines. This results in a substantial reduction in the time required to perform these basic operations. For example, with the multiply-divide option installed, multiplication of two signed 15-bit numbers is reduced from 105 machine cycles to 8 machine cycles, and division of a 31-bit signed number is reduced from 193 machine cycles to 10 machine cycles.

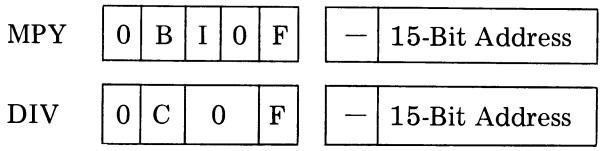
4-282. All of the additional logic for hardware multiplication and division is contained on a single Multiply-Divide option card accommodated inside the basic 704 Processor, which has a prewired connector for this plug-in option card. Dwg 394572 shows all logic functions included on the card.

4-283. Multiply-divide option logic, for the most part, represents extensions of existing basic CPU logic functions. The design philosophy has been to supply those elements needed only for executing multiply and divide instructions on the option card. For instance, MPY and DIV instruction decoding logic, extensions to the sequence counter logic, additional command-end logic, shifted adder output gates to the index register, etc required to

execute multiply and divide instructions only are located on the option card. All of the multiply-divide logic and its effect on other areas of the CPU is covered in the discussions of multiply and divide instruction sequencing and execution (paragraphs 4-296, 4-320, and 4-346).

4-284. Multiply and Divide Instructions

4-285. The multiply (MPY) and divide (DIV) instructions differ from other 704 Processor instructions in that they consist of two 16-bit instruction words each. The formats of the instruction words are shown below:



4-286. The first word of each instruction is a conventional instruction word with a two-character instruction code (0B and 0C, respectively), 0 in the F1 field, and a character in the F2 field to be copied into the iteration counter. This character is always the number 15 (F_{16}) in the MPY and DIV instruction word.

4-287. The second word of the MPY instruction contains a 15-bit direct address for the multiplicand, and the second word of the DIV instruction contains a 15-bit direct address for the divisor. Both of these are effective word addresses for loading these operands from any location in memory.

4-288. Indexing is permitted when executing an MPY instruction, and is specified by a 1 in the bit-8 position of the instruction first word (8_{16} in the F1 field). In this case, the 15-bit address contained in the second word of the MPY instruction is treated as a base address to which the contents of the index register are added to obtain the effective word address for the multiplicand. The state of the global flip-flop and the contents of the extension register are both ignored in this case.

Note

Nothing in the multiply-divide logic precludes indexing of the DIV instruction by specifying an 8_{16} character in its F1 field. However, it is impractical, since the index register must be loaded with the more-significant half of the dividend prior to executing the instruction.

4-289. The following prior conditions are assumed when executing a MPY instruction:

a. The 16-bit multiplier (sign and 15 magnitude bits) is located in the accumulator register. If negative, the multiplier must be expressed in 2's complement form.

b. The 16-bit multiplicand (sign and 15 magnitude bits) is located in the memory location specified by the second word address (direct addressing) or by the sum of the second word address and the index number (indexed addressing). The 2's complement of negative multiplicands must be used.

c. Significant data in the index register has been stored, since it will be lost as the product is accumulated. Also, the index register must contain the proper index number, if operating in the indexed addressing mode.

4-290. After execution of the MPY instruction, the product of the multiplicand and multiplier factors will reside in the coupled index and accumulator registers as a signed 31-bit number (sign and 30 magnitude bits). The state of the product sign bit (IXR00 and ACR00) is determined from the signs of its two factors, according to the rules for algebraic multiplication. If negative, the product will be in 2's complement form.

4-291. Overflow during multiplication can only occur if both factors happen to be -2^{15}. In this case, the overflowing step will be performed, but the adder overflow flip-flop will be set and can be tested by the program.

4-292. The following prior conditions are assumed when executing a DIV instruction:

a. The dividend is represented as a 31-bit signed number and resides in the coupled index and accumulator registers, with the 16 most-significant bits (sign and 15 higher-order magnitude bits) in the index register and the 15 lower-order magnitude bits in the 15 least-significant bit positions of the accumulator. The state of accumulator register bit 0 (ACR00) is immaterial to the proper execution of the instruction. If negative, the dividend must be expressed in its 2's complement form.

b. The 16-bit divisor (sign and 15 magnitude bits) is located in the memory location specified by the second word address. A negative divisor must be expressed in its 2's complement form.

4-293. If the DIV instruction is successfully executed, the quotient will reside in the accumulator register, and the remainder will reside in the index register. Both of these are signed 16-bit numbers. The sign of the quotient is determined by the signs of the dividend and the divisor, according to the rules for algebraic division. The sign of the remainder is the same as the sign of the original dividend. If negative, the quotient and the remainder are expressed in their 2's complement form.

4-294. The DIV instruction cannot be successfully executed if the dividend is so large or the divisor so small that the quotient will overflow the 16-bit accumulator register. In this case, the overflow flip-flop will be set, and the instruction will be terminated without execution. Normally, the dividend contents of the coupled index and accumulator registers will remain unaltered, but bit 0 of the accumulator register (ACR00) may or may not be the same as it was prior to instruction execution.

4-295. DIV instruction execution time is 10 or 11 machine cycles, if the division is completed successfully, and 4 or 5 machine cycles, if an overflow is detected. The shorter times apply when the dividend is positive, with the extra machine cycle being required when the dividend is negative.

4-296. Multiply-Divide Fetch Phase Sequencing

4-297. With slight exception, the sequencing of both MPY and DIV instructions is the same up to the point where each begins to be processed through the cyclic, iterative portion of its algorithm. This common sequencing includes the operations necessary to read both words of the instruction from memory, indexing of the operand address contained in the second word (only if specified), and loading of the effective word address for the multiplicand or divisor into the memory address register. The operations just described represent a compound, two machine cycle instruction fetch phase. Thereafter, MPY and DIV instruction operations enter their respective iterative algorithms for execution (paragraphs 4-309 and 4-339).

4-298. Figure 4-12 is a flow diagram of the fetch phase sequencing common to MPY and DIV instructions. The first word of a MPY or DIV instruction is fetched during time period TA (T0 and T1) of CPU sequencer state SCDC1, like all other 704 Processor instructions. Normal CPU logic performs the following operations during this time period: reads and loads the instruction first word into the memory buffer register, copies the first eight bits (instruction code) into the instruction register, copies the last four bits (F2-field iteration count, which should be F_{16}) into the iteration counter, copies the program count into the memory address register, and increments the program count by one.

4-299. Sometime near the start of time period T2, the output signals from the CPU instruction decoder will indicate that a MPY or DIV instruction has been fetched (INDC0B + INDC0C), and the multiply-divide logic will become active (SC1MD true). The first function performed by the MD logic is to reset all flip-flops to be used which may have remained set after the last multiply or divide instruction was executed. This occurs during time period T3 (SC1MD T3MD), when low signals on ADFOVFR1- and MDRST- lines directly reset CPU adder overflow flip-flop ADFOVF and all of the MD logic flip-flops.

4-300. Because of the nature of the divide algorithm (paragraph 4-339), a negative dividend must be recomplemented before iterative subtractions are performed. This is a two-step process, since the dividend resides in a double-length register. To save

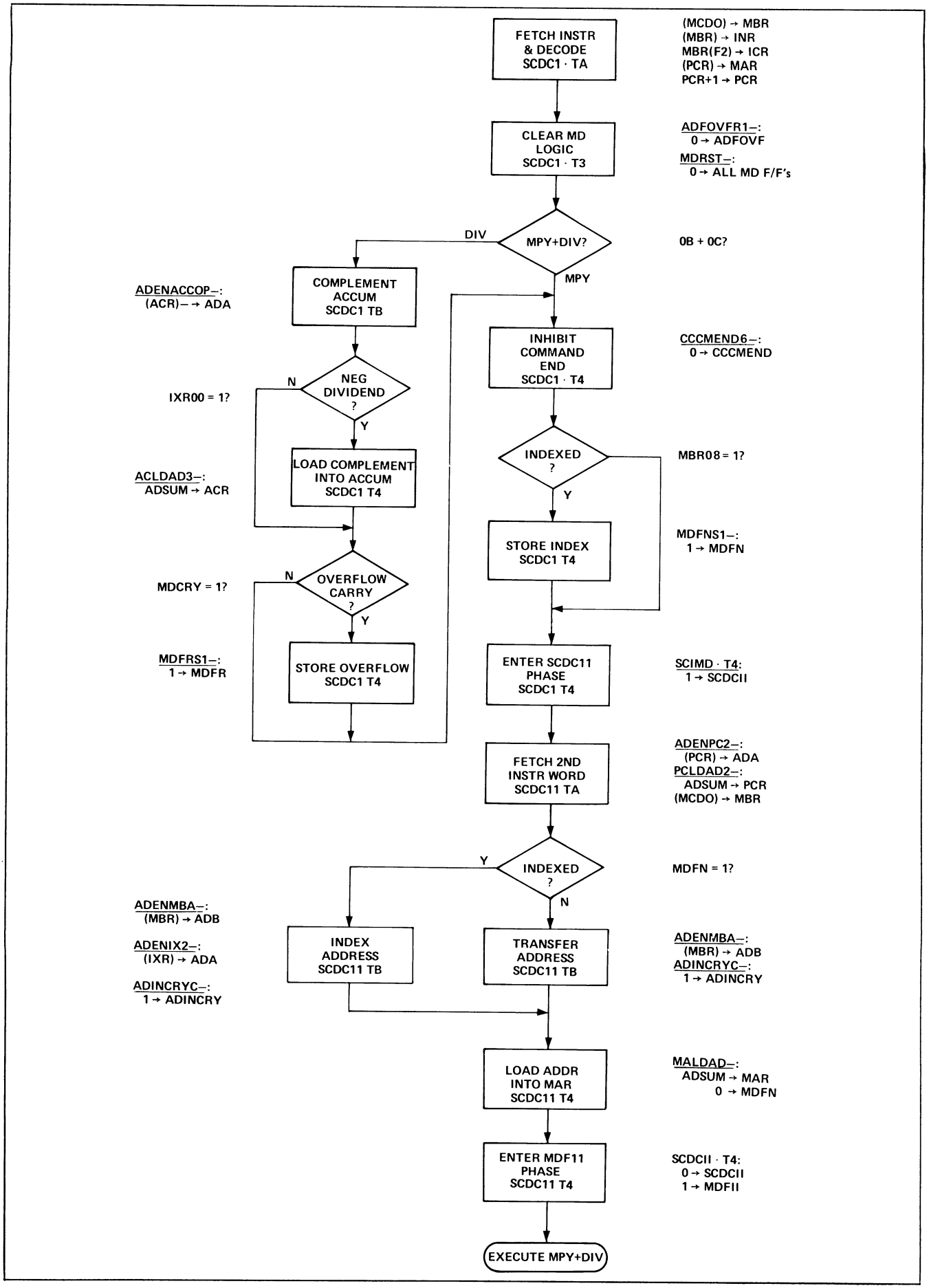


Figure 4-12. Multiply-Divide Instruction Fetch Flow Diagram

time later, and since the adder is available during the second half of the instruction fetch phase (time period TB of phase SCDC1), the accumulator half of negative dividends is recomplemented at this time.

4-301. Signal SC1DIV will be true during the fetch phase of DIV instructions (INDC0C SCDC1). During time periods T2, T3, and T4 (TBMD true), signal ADENACCOP- becomes false to gate inverted outputs of the accumulator register (ACR00- through ACR15-) into the adder input A gates (ADA00- through ADA15-). If the sign bit of the dividend is negative (IXR00MD true), signal ACLDAD3- becomes false during time period T4 (T4MD true), causing the adder outputs (ADSUM00- through ADSUM15-) to be loaded into the accumulator register (ACR00 through ACR15). Since signal ADINCRY was not activated by this operation, the adder output loaded back into the accumulator register will be the 2's complement of the original contents.

4-302. Simultaneously, the adder is checked for carry overflow from this operation which would affect the more-significant half of the dividend when the contents of the index register are inverted later. If overflow occurs (ADA01 ADC02), signal MDCRY will be true and the false state of signal MDFRS1- during time period T4 will cause MD logic flip-flop MDFR to be set at the end of the time period. In this way, the carry over into the index register is now stored for later use.

4-303. The remaining sequence of events for fetch phase processing apply to both MPY and DIV instructions. During time period T4 of the SCDC1 phase (SC1MD T4MD), signal CCCMEND6- is false to inhibit CPU command-end logic and prevent the sequencer from cycling back into the SCDC1 fetch phase. As this is occurring, the state of the instruction word index bit (MBR08) is gated to another MD flip-flop, MDFN, over set line MDFNS1-. The flip-flop will be set at the end of time period T4, if bit MBR08 is a 1. Storage of the index bit is necessary because the contents of the memory buffer register will be lost when the second instruction word is read from memory, during the next fetch phase machine cycle.

4-304. The second machine cycle of the multiply-divide fetching operation begins at the end of T4, when CPU sequencer flip-flop SCDC1 is reset and MD sequencer flip-flop SCDC11 is set (SC1MD KKMDT4). From this point on, the CPU sequencer no longer controls CPU operations (all CPU sequencer flip-flops are reset), and it cannot take over control again until the MD logic generates its own CCCMEND signal. Consequently, there is no case where full execution of a MPY or DIV instruction can be interrupted.

4-305. Reading of the second word from memory and loading it into the memory buffer register during time period TA of phase SCDC11 is automatic, since MCRW- logic regularly causes a memory access operation to occur at this time during every machine cycle, except when specifically inhibited from doing so (paragraph 4-433). However, the automatic incrementing of the program count, which normally occurs at the same time in the SCDC1 phase, must be done by MD logic. The reading in of the second instruction word does not disturb the iteration count, since loading of the iteration counter is a function of SCDC1 being set.

4-306. The program count is incremented during time periods T0 and T1 of the SCDC11 phase (SCDC11 TIRCA). During these two time periods, signal ADENPC2- is false, causing the program counter outputs to be gated to the adder input A gates. During time period T1, signal PCLDAD2- will be false (SCDC11 TIRC1) so that the adder outputs will be gated back to the program counter register and loaded at the end of T1. This adder output will be the original program count plus one, since signal ADINCRY was not generated.

4-307. The remaining three time periods of the machine cycle (SCDC11 TBMD true) are used to index the second word address (only if specified) and to load the memory address register with the effective word address for the stored operand. If flip-flop MDFN was set in the previous phase, indicating address indexing is to be performed, signal ADENIX2- will be false and cause the contents of the index register to be gated to adder input A gates. As noted before, this is only a valid

operation for the MPY instruction, since in the DIV instruction, the index register contains part of the dividend. Signal MD01- is false regardless of the state of the MDFN flip-flop and activates signal lines ADENMBA- and ADINCRYC- to gate the contents of the memory buffer register into adder input B gates and ADINCRY into the adder, respectively. Consequently, by time period T4, the adder outputs will be the sum of the contents of the memory buffer and index registers or just the contents of the memory buffer register, depending upon whether or not the MDFN flip-flop was set. This is the effective word address to be loaded into the memory address register.

4-308. Signal MALDAD- becomes false during time period T4 (SCDC11 T4MD), gating the adder outputs (ADSUM00- through ADSUM15-) into the memory address register (MAR00 through MAR15). At the end of time period T4, the memory address register will be loaded, the MDFN flip-flop will be reset (MALDAD KKMD), the SCDC11 phase flip-flop will be toggled reset, and phase MDF11 flip-flop will be set (SCDC11 KKMDT4). This constitutes the end of the two cycle fetch phase operation, and the MPY and DIV instructions advance to their respective execution sequences.

4-309. Multiply Algorithm

4-310. Multiplication is carried out by accumulating the sum of the partial products formed by multiplying the multiplicand by each digit of the multiplier in turn. The partial sum is accumulated in the index register and is shifted right one place before adding the next partial product. The multiplier contained in the accumulator register is shifted right at the same time, and the lower order bits of the partial sum are shifted into the positions vacated by the multiplier.

4-311. The least-significant bit of the multiplier (ACR15) controls the formation of the partial products. After it has been used, this bit is of no further use, and it is allowed to be lost as the multiplier is shifted right. The next-least-significant bit of the multiplier then becomes the least-significant bit and determines the next partial product. After all 15 iterative shifts have been completed, the entire multiplier is gone and the less-significant half of the final product resides in the accumulator.

4-312. The rules for accumulating partial products during the execution of MPY instructions are as follows:

a. If the least-significant multiplier bit (ACR15) is a 0, shift the accumulated sum (and the multiplier) one place to the right without adding anything to the sum.

b. If the least-significant multiplier bit is a 1, add the multiplicand to the 16 most-significant bits of the accumulated sum and shift the new sum (and the multiplier) one place to the right.

4-313. Since signed numbers are used, with negative numbers expressed in 2's complement form, the partial products and their accumulated sum may be positive or negative, depending on the sign of the multiplicand. (The individual multiplier bits which determine the partial products are positive digits, so the sign of the multiplicand determines the sign of the partial products.) The following rules governing signs apply:

a. If the present multiplier bit is 0 and all previous multiplier bits were 0, the accumulated sum is zero (positive), and a 0 must be supplied in the sign position when the sum is shifted right.

b. If the present multiplier bit is 1, or any previous multiplier bit was 1, the accumulated sum is not zero, and the sign of the multiplicand must be supplied in the sign position when the sum is shifted right.

4-314. The preceding rules ensure that the correct product will be obtained regardless of the sign of the multiplicand, so long as the multiplier is positive. Negative products will be expressed in 1's complement form. But negative multipliers require an additional step to obtain the correct product because the multiplier was in 2's complement form. If the multiplier has a magnitude X, its 2's complement is 2^{16}-X. When partial products are formed and accumulated for all 16 bits of the multiplier, including the sign bit, the product of a

multiplicand of magnitude Y and a 2's complement multiplier will be $(2^{16}\text{-X})Y$ or $(2^{16}Y - XY)$. This is $2^{16}Y$ greater than the correct product -XY, and the quantity $2^{16}Y$ must be subtracted to obtain the correct product.

4-315. The correction for negative multipliers can be simplified because the partial product of the sign bit (1) and the multiplicand is always $2^{15}Y$ because of its notational position. Therefore, the accumulated sum after the partial product of the most-significant magnitude bit is added is $(2^{16}Y - XY) - 2^{15}Y$ (or $2^{15}Y - XY$). At this point it is only necessary to subtract Y, the multiplicand, from the most significant bits of the accumulated sum instead of adding it to obtain the correct product. Because Y is subtracted from the most-significant 16 bits of the 31-bit uncorrected product, it has a weight of $2^{15}Y$, the required correction.

4-316. Since the quantity added to the accumulated sum by the partial product by positive multiplier sign bits is always zero, and the partial product of negative multiplier sign bits is not added to the accumulated sum, partial product accumulation is terminated after the most significant magnitude bit is reached (15 iterations). Thereafter, if the multiplier sign is positive, the correction step is skipped. And if the multiplier sign is negative, the required correction factor (the multiplicand) is subtracted from the sum.

4-317. The foregoing algorithm gives the correct product for any combination of positive and negative multipliers and multiplicands, with negative products expressed in 2's complement form. The procedure is shown in figure 4-13 for representative combinations of positive and negative multipliers and multiplicands (using 6-bit numbers for simplicity).

4-318. After the complete product is formed, it contains 31 bits (sign and 30 magnitude bits) and occupies the index register and the 15 most-significant positions of the accumulator register. The sign bit of the multiplier still occupies the least-significant position of the accumulator register. The last step of the multiplication process is to split the product into two 16-bit numbers by shifting the 15 least-significant bits in the accumulator right one place and copying the sign of the product into the sign position of the accumulator register. This step also disposes of the sign bit of the multiplier by shifting it off.

4-319. Overflow is possible during multiplication only under one condition: when -2^{15} is multiplied by -2^{15}. The product in this case is $+2^{30}$, which is greater than the largest number $(2^{30} - 1)$ that can be expressed by the 31 bits of the product. The test for the overflow condition is made during the correction step, since overflow is not possible if the multiplier is positive. If the sign bits of the multiplier, the multiplicand, and the corrected product are all three negative, overflow has occurred, and the overflow flip-flop will be set.

4-320. Multiply Execute Sequencing

4-321. MPY instruction fetch phase sequencing, which loads both instruction words and loads the memory address register with an indexed or unindexed effective word address for the stored multiplicand, has been discussed previously in paragraph 4-296. The following is a description of the multiply-divide logic and sequence of operations that execute the multiply algorithm. Figure 4-14 is a flow diagram of multiply instruction execution.

4-322. MPY instruction execution begins with the setting of MD logic flip-flop MDF11. This makes signal MDF11MUL true (MDF11 INDC0B) for one machine cycle, during the first part of which the multiplicand is read from memory and loaded into the memory buffer register. Again, this memory-read operation is automatic during time periods T0 and T1 of all machine cycles, unless expressly inhibited. In fact, this is done right away, since fetching of the multiplicand is the last memory access operation required until the end of MPY instruction execution.

4-323. The first clock after MDF11 is set causes MD logic read-write control flip-flop MDFRDWR to be set. The function of the MDFRDWR flip-flop is to hold signal OPTRDWR- false until the command-end condition (MDEND true) occurs. This signal is an inhibit input to the memory control MCRW- logic of the CPU (Dwg 394562,

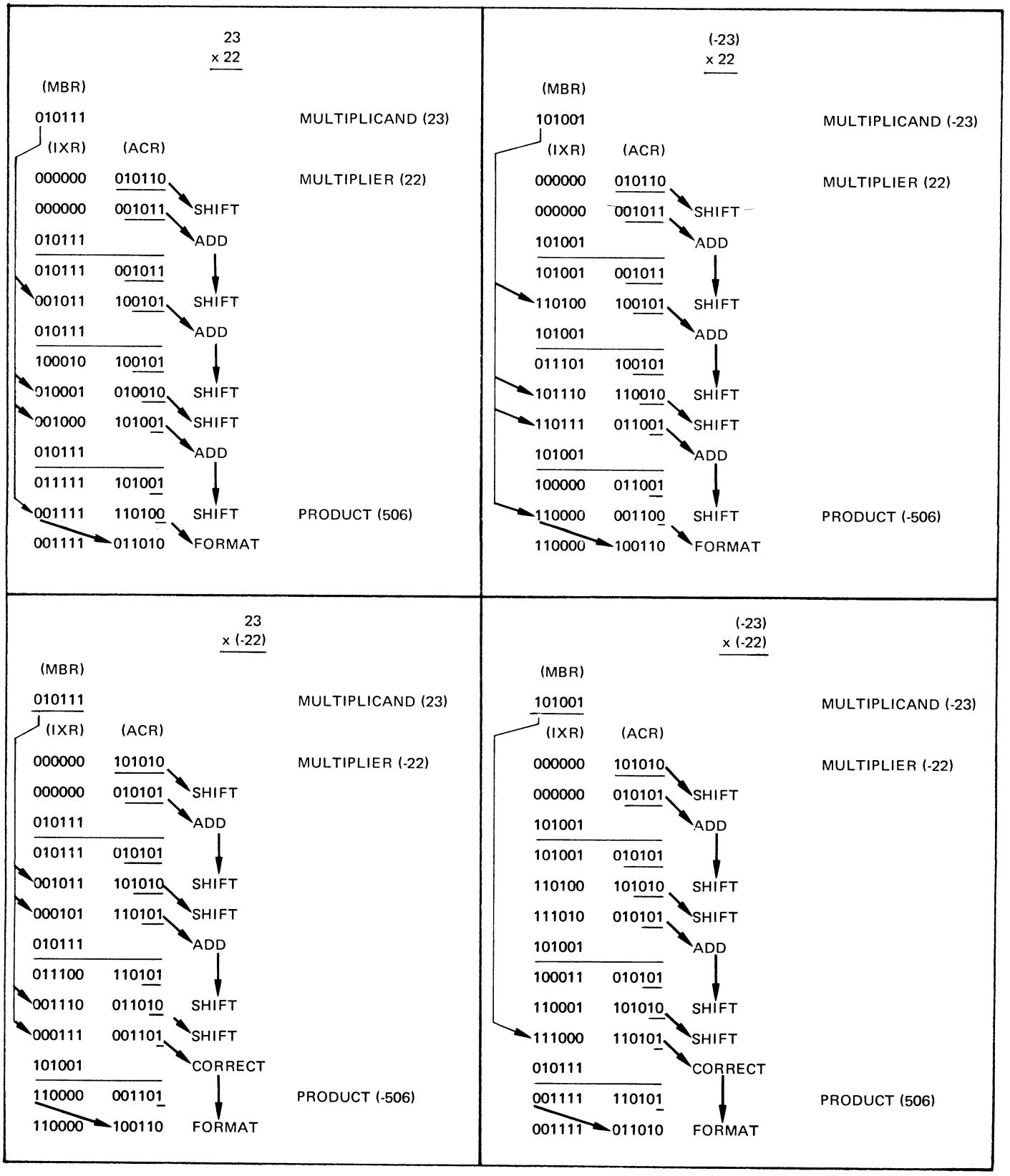


Figure 4-13. Multiplication Examples for Positive and Negative Multipliers and Multiplicands

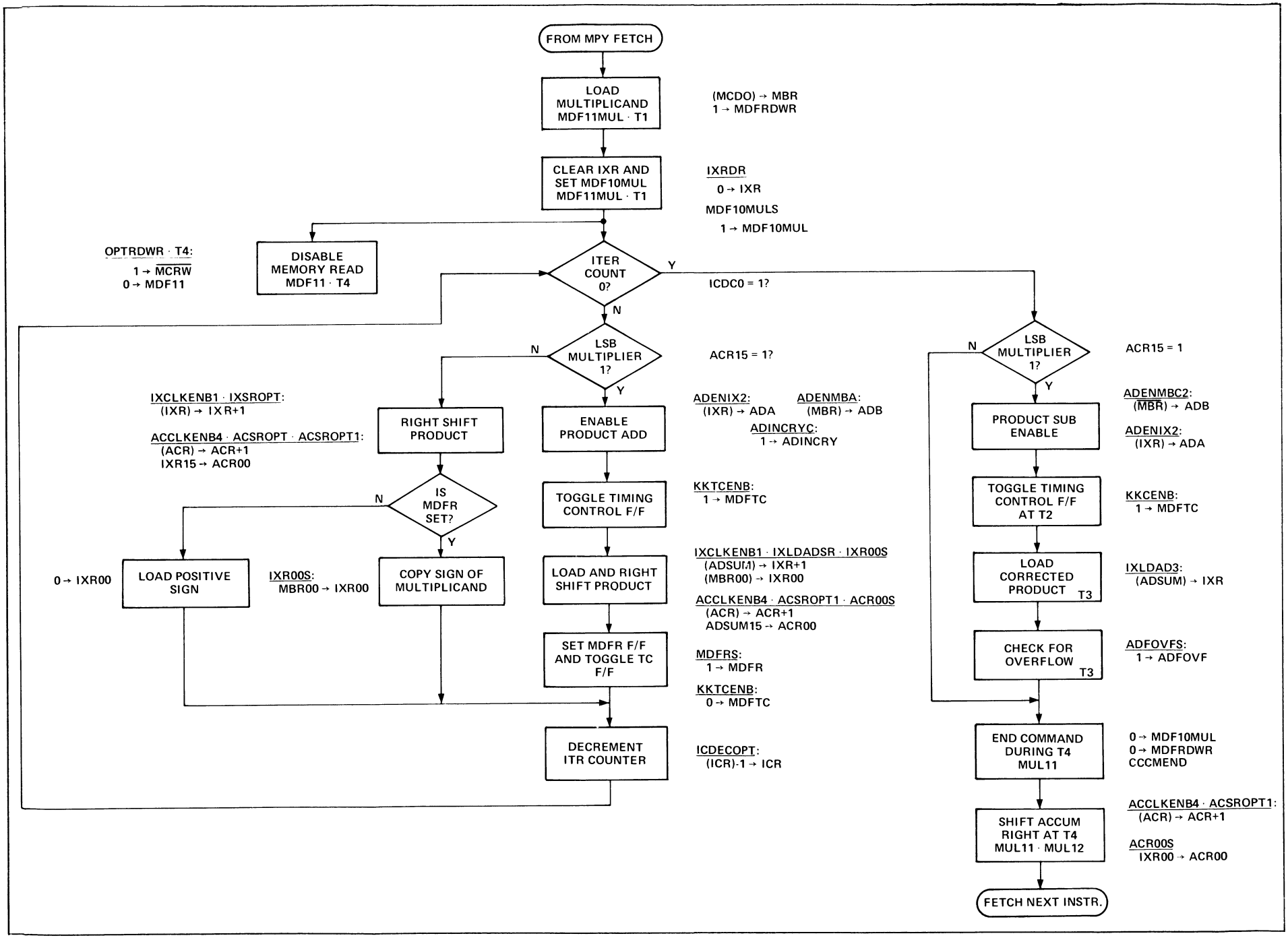


Figure 4-14. Multiply Instruction Execution Flow Diagram

Sht 4). It will not be effective until the following T4 time period when CPU logic flip-flop MCFRDWR is reset to disable the MCRW- line; that is, until the current read-restore memory cycle that loads the multiplicand is completed.

4-324. During time period T1, while the memory-read operation is occurring, signal IXRDR- becomes false (MDF11MUL TIRC1) and directly resets all index register flip-flops preparatory to product accumulation. At the end of time period T1, the ground is removed from the index register direct reset inputs, and phase control flip-flop MDF10MUL is set (MDF10MULS true). Once the MDF10MUL flip-flop is set, iterative execution of the multiply algorithm is enabled. Flip-flop MDF11 is not reset until the end of the following T4 time period (SCDC11- KKMDT4), just as the memory access inhibit condition becomes effective.

4-325. Cyclic operations which occur while flip-flop MDF10MUL is set are under control of the iteration count and the state of the least-significant multiplier bit ACR15. Assuming that the iteration counter received a correct initial loading of 1111_2 (F_{16}) when the instruction first word was fetched, signal ICDC0 will be false (iteration count not zero) for 15 repetitions of the partial product accumulation cycle; that is, until the count has been decremented down to zero. During this time, multiplier bit ACR15 alone determines the path sequencing will take.

4-326. Suppose that the first multiplier bit examined is a zero (signal MUL0N15N true). According to the algorithm, this condition requires shifting the sum of the partial products right one place without adding anything to it. This right shift can be accomplished in one clock period; that is, at a rate of five times per machine cycle. State MUL0N15N true enables index register right shifting for one clock time (generates IXCLKENB1 and IXSROPT signals), and also right shifting of the accumulator register (generates ACCLKENB4, ACSROPT, and ACSROPT1 signals). Signal ACSROPT couples the two registers together by enabling accumulator bit 0 to copy index register bit 15.

4-327. A decision is made simultaneously with the right-shift operation which determines the sign placed into the vacated sign bit position of the index register. If flip-flop MDFR is not set; indicating that no previous multiplier bit examined was a one, and the partial sum is still zero and, therefore, positive; a zero is copied into the IXR00 bit register. This is automatic, occurring whenever the register is clocked and no input has been enabled. But if the MDFR flip-flop is set, the shifted sum of the partial products contains significant data (is not zero), and should have the same sign as the multiplicand. Signal IXR00S accomplishes this by causing sign bit register IXR00 to copy the state of the sign bit register MBR00 of the memory buffer register.

4-328. Now suppose that the multiplier bit examined is a one (signal MUL0N15 true). By the algorithm, the value of the multiplicand must be added once to the accumulating sum of partial products followed by the shifting of the resultant one place to the right. This operation requires two time periods; one to enable the adder inputs and allow the outputs to settle, and another to load the sum into the index register but offset one bit position while direct shifting the accumulator register.

4-329. When signal MUL0N15- becomes false (MDF10MUL ICDC0- ACR15), signal ADENIX2- goes false to gate index register outputs to the adder input A gates, signal ADENMBA- goes false to gate memory buffer register outputs to adder input B gates, and signal ADINCRY- is made false to cause the ADINCRY input to be a 1. Also, MUL0N15- false enables the clock gate (KKTCENB) for flip-flop MDFTC, and the flip-flop is set by the next clock, ending the first phase of the add-and-shift operation.

4-330. The setting of timing control flip-flop MDFTC activates signal MUL02- and several other second-phase control signals. This state causes the clock-enable gates for the index and accumulator registers to be enabled (false states of signals IXCLKENB1- and ACCLKENB4-). Simultaneously, it makes signal IXLDADSR true, activating the auxiliary right-shift input gates (IXR01S

through IXR15S) provided by the MD logic for the loading of adder outputs ADSUM00- through ADSUM14- into index bits IXR01 through IXR15. The state of the multiplicand sign bit MBR00 is copied into the index register sign bit position IXR00 through gates MULIX00S1-, MUL04-, and IXR00S. All of this occurs to the index register on the next clock.

4-331. At the same time, the false state of signal ACSROPT1- activates the direct right-shift gates of the accumulator register, and adder output bit ADSUM15- is copied by the ACR00 bit register through gates MUL03- and ACR00S. This occurs at the same time the index register is shift loaded with the sum output, so the net effect is that of adding the value of the multiplicand to the most-significant half of the partial product and shifting the product and multiplier held in the coupled double-length register one bit to the right.

4-332. The first time a one is detected in bit ACR15 (that is, the first time MUL02- becomes false), flip-flop MDFR will be set and remain set for the rest of MPY instruction execution. This represents the detection of the first significant digit of the multiplier, and infers that the sum of partial products is no longer zero and must assume the sign of the multiplicand.

4-333. Since signal KKTCENB is still true during the second phase, and the state of output MDFTC- is false, timing control flip-flop MDFTC will be reset at the same time that the product and multiplier are shifted. Also, MUL02- false makes signal ICDECOPT- false, and the iteration counter is decremented by one count at the same clock time. These cycles repeat until 15 iterative shifts have occurred and the iteration count has reached zero; that is, until the ICDC0 flip-flop has been set.

4-334. If the MPY instruction has been performed correctly up to this point, the only vestige of the multiplier will be its sign bit, now in ACR15. A subtractive correction is necessary only when the multiplier is negative (ACR15 is a 1). This makes signal MULO15- false (MDF10MUL ACR15 ICDC0), causing the inverse memory buffer register outputs to be applied to the adder input A gates (signal ADENMBC2- false), and the index register outputs to be applied to the adder input B gates (signal ADENIX2- false). Nothing can happen to the adder sum outputs until after the next T2 time period, when timing control flip-flop MDFTC is toggled set again by the false state of MUL05-.

4-335. Once the MDFTC flip-flop is set, signal MUL06- becomes false, causing the sum output of the adder to be gated back into the index register (signal IXLDAD3- false) and loaded by the next clock after time period T3. The false state of signal MUL06- also causes the output of overflow check gates to be checked. A false output at MUL07- indicates that overflow has occurred (ADA00 ADB00 ADSUM00- + ADA00- ADB00- ADSUM00). Signal ADFOVFS- becomes false whenever MUL08- is false, causing the adder overflow flip-flop to be set.

4-336. The remaining steps generate an MD logic CCCMEND signal to reactivate the CPU sequencer and also perform an accumulator right-shift operation to format the final product correctly. These things occur after time period T3 of the correction cycle (MUL06- false) for negative multipliers and immediately after the iteration count has reached zero for positive multipliers (MDF10MUL ICDC0 ACR15-).

4-337. During time period T4, signal MUL11- is false (MUL10 T4MD). This causes command-end gate output MDEND- to go false, re-enabling memory access inhibit line OPTRDWR- and command-end line CCCMEND1-. The MDFRDWR flip-flop receives an MDEND reset input so that it will be reset by the clock at the end of T4. This prevents the memory access inhibit line OPTRDWR- from going false again after MDEND- goes true.

4-338. The MUL11- signal also enables the MDF10MUL flip-flop clock so that the flip-flop can be toggled reset at the end of time period T4. Signals ACSROPT1- and ACCLKENB4- are both false because of the MUL11- state, causing the contents of the accumulator to be shifted right one bit position. The output of the MUL12- gate (MUL10 T4MD IXR00MD) provides an output to the accumulator sign bit gate ACR00S. Thus, the clock at the end of the T4 time period will spread

the product so that the lesser half will reside in ACR01 through ACR15, and the sign in ACR00 will be the same as that in IXR00. Once the MDF10MUL flip-flop is reset, CCCMEND1- becomes true again, and the MD logic is both deactivated and decoupled from the CPU.

4-339. Divide Algorithm

4-340. Division is performed as a succession of trial subtractions of the divisor from the dividend, keeping track of the number of times subtraction was successful without producing a negative remainder. This number of successful subtractions is the quotient. Sixteen trial subtractions are required to form the complete, 16-bit quotient (sign and 15 magnitude bits), the value of each digit being determined by a separate subtraction step.

4-341. The rules for forming a quotient and a declining remainder during the execution of DIV instructions are as follows:

a. A trial subtraction of the divisor from the 16 most-significant bits of the dividend (or the remainder of the dividend) will precede each quotient bit determining iteration.

b. If any trial subtraction (except the last iteration) results in a positive remainder, the subtraction is executed, the remainder of the dividend and any previously determined digits of the quotient are shifted left one bit position, and a one is appended to the less-significant end of the quotient (ACR15).

c. If the first trial subtraction results in a negative remainder, the overflow flip-flop is set immediately, the subtraction is not executed, and the instruction is terminated without forming a quotient. The division overflow criteria is explained in paragraph 4-345.

d. If any subsequent trial subtraction (except the last iteration) results in a negative remainder, the subtraction is not executed, the remainder of the dividend and any previously determined digits of the quotient are shifted left one bit position, and a zero is appended to the less-significant end of the quotient.

e. If the last iteration trial subtraction results in a positive remainder, the subtraction is executed, the quotient only is shifted left one bit position, and a one is appended as the least-significant bit of the final quotient.

f. If the last iteration trial subtraction results in a negative remainder, the subtraction is not executed, the quotient only is shifted left one bit position, and a zero is appended as the least-significant bit of the final quotient.

4-342. The division algorithm can be executed only with positive numbers. If either the dividend or the divisor is signed as a negative number, it is assumed that it was expressed in 2's complement form. Any negative operand is automatically recomplemented prior to iterative subtraction. The original signs of the dividend and divisor are saved for use in determining the signs of the quotient and the remainder after division has been completed, according to the rules which follow:

a. The sign of the final remainder will always be the same as that of the original dividend. If negative, it will be a one, and the magnitude will be expressed in 2's complement form.

b. The sign of the final quotient will be positive when the original signs of the dividend and divisor were both the same (both positive or both negative).

c. The sign of the final quotient will be negative only when the signs of the original dividend and divisor differed. In such cases, the quotient will be expressed in 2's complement form.

4-343. After the division process is completed, the 16-bit (sign and 15 magnitude bits) quotient will be located in the accumulator. The final remainder is the content of the index register and is composed of sign and 15 magnitude bits. The signs of these two resultants are consistent with the signs of the original dividend and divisor and the rules for sign determination just described. Negative resultants are always given in 2's complement form.

4-344. The foregoing algorithm gives the correct quotient and remainder for any combination of positive and negative dividends and divisors, unless

overflow is detected, of course. The division process is illustrated in figure 4-15, using 6-bit numbers to simplify the example. Notice that in each step, the divisor is subtracted from the 16 most-significant bits of the dividend or the subsequent remainder of the dividend, and the sign of the difference determines its disposition as well as the value of one bit of the quotient. The dividend or remainder is shifted left one place for each step, and the quotient bits are shifted into the places vacated on the right.

4-345. A check for overflow is made only once during the execution of a DIV instruction. The very first trial subtraction iteration is a test for overflow. Since the magnitude limit of the accumulator register is $2^{15} - 1$, overflow will occur if the dividend is so large, or the divisor so small that the quotient is greater than $2^{15} - 1$. Therefore, the first step of the division process checks these relative magnitudes. This also determines the sign bit of the quotient, which must be zero (positive) for positive dividends to be successfully divided by positive divisors. The quotient of two positive numbers is negative only when an overflow condition exists.

4-346. Divide Execute Sequencing

4-347. DIV instruction fetch phase sequencing, which loads both instruction words and loads the memory address register with an indexed or unindexed effective word address for the stored divisor, has been discussed previously in paragraph 4-296. The following is a description of the multiply-divide logic and the sequence of operations that execute the divide algorithm just discussed. Figure 4-16 is a flow diagram of divide instruction execution.

4-348. DIV instruction execution begins with the setting of MD logic flip-flop MDF11. This makes signal MDF11DIV true (MDF11 INDC0C) for one machine cycle, during the first part of which the divisor is read from memory and loaded into the memory buffer register. This memory-read operation is automatic during time periods T0 and T1 of all machine cycles, unless expressly inhibited. This is done right away, since fetching of the divisor is the last memory access operation required until the end of the DIV instruction execution.

4-349. The first clock after MDF11 is set causes read-write control flip-flop MDFRDWR to be set. The function of the MDFRDWR flip-flop is to hold signal OPTRDWR- false until the command-end condition (MDEND true) occurs. This signal is an inhibit input to the memory control MCRW- logic of the CPU (Dwg 394562, Sht 4). It will not be effective until the following T4 time period, when CPU logic flip-flop MCFRDWR is reset to disable the MCRW- line; that is, until the current read-restore memory cycle that loads the dividend is completed.

4-350. While the memory-read operation for the divisor is occurring, the adder logic is used to recomplement the second half of negative dividends. It will be recalled (paragraph 4-300) that the accumulator register portion of negative dividends is recomplemented during the DIV instruction second-word fetch cycle. So during time period TA of this cycle, signal ADENIXC is generated unconditionally and gates inverted outputs of the index register to the adder input A gates. The adder will also receive a true ADINCRY signal if no overflow carry occurred when the accumulator register was recomplemented (MDFR flip-flop remained reset). This will cause inversion only (1's complement) to occur to the index register contents, since it is the more-significant half of the dividend, and complementing of the less-significant half in the accumulator did not generate and store a carry. But if a carry was generated (MDFR flip-flop is set), signal ADINCRY will not be true, and the 2's complement of the index register contents will be seen at the adder sum outputs.

4-351. It is not until the end of T1 that the sign of the dividend is actually checked to determine a control action. If the sign is negative, signal DIV01 is true (MDF11DIV TIRC1 IXR00), causing signal MDFNS to store the sign in the MDFN flip-flop and signal IXLDAD3 to gate the ADSUM outputs of the adder to the index register inputs. The same clock at the end of time period T1 also resets the MDFR flip-flop for possible use later. If the sign of the dividend happens to be positive (IXR00 is zero), naturally the contents of the index register will not be changed, and there is no need to store its sign in the MDFN flip-flop, since that flip-flop is

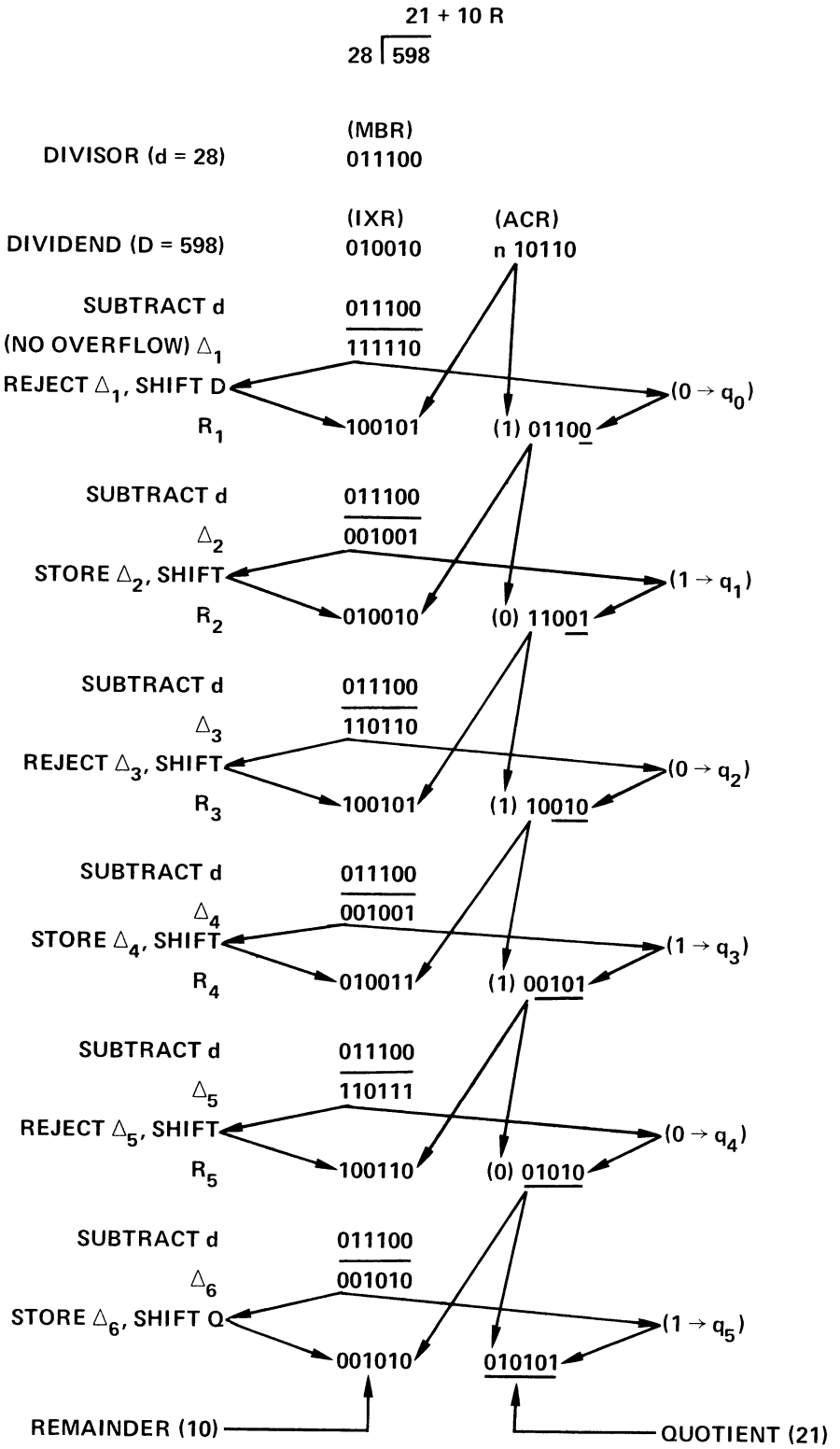


Figure 4-15. Division Example

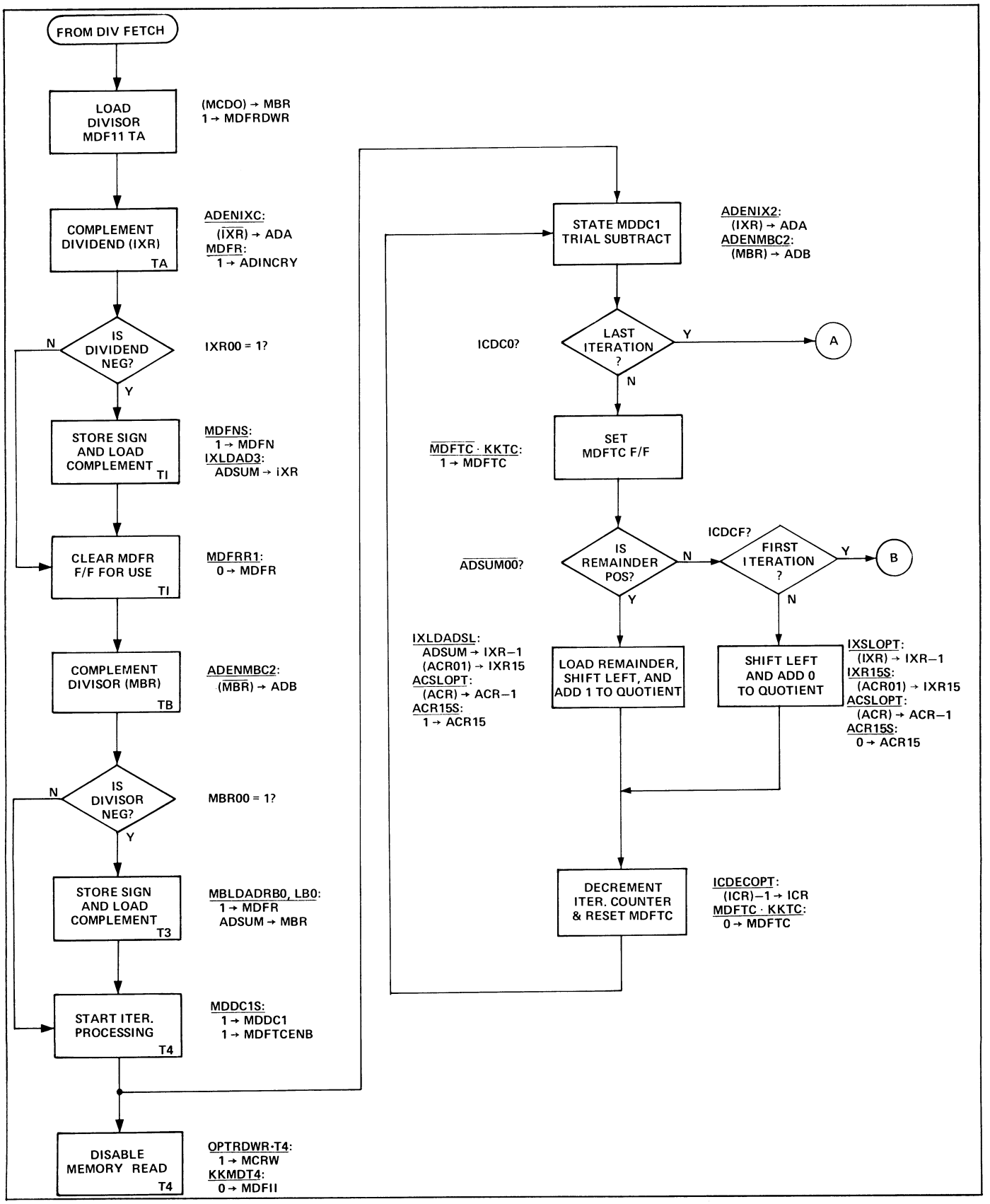


Figure 4-16. Divide Instruction Execution Flow Diagram (Sheet 1 of 2)

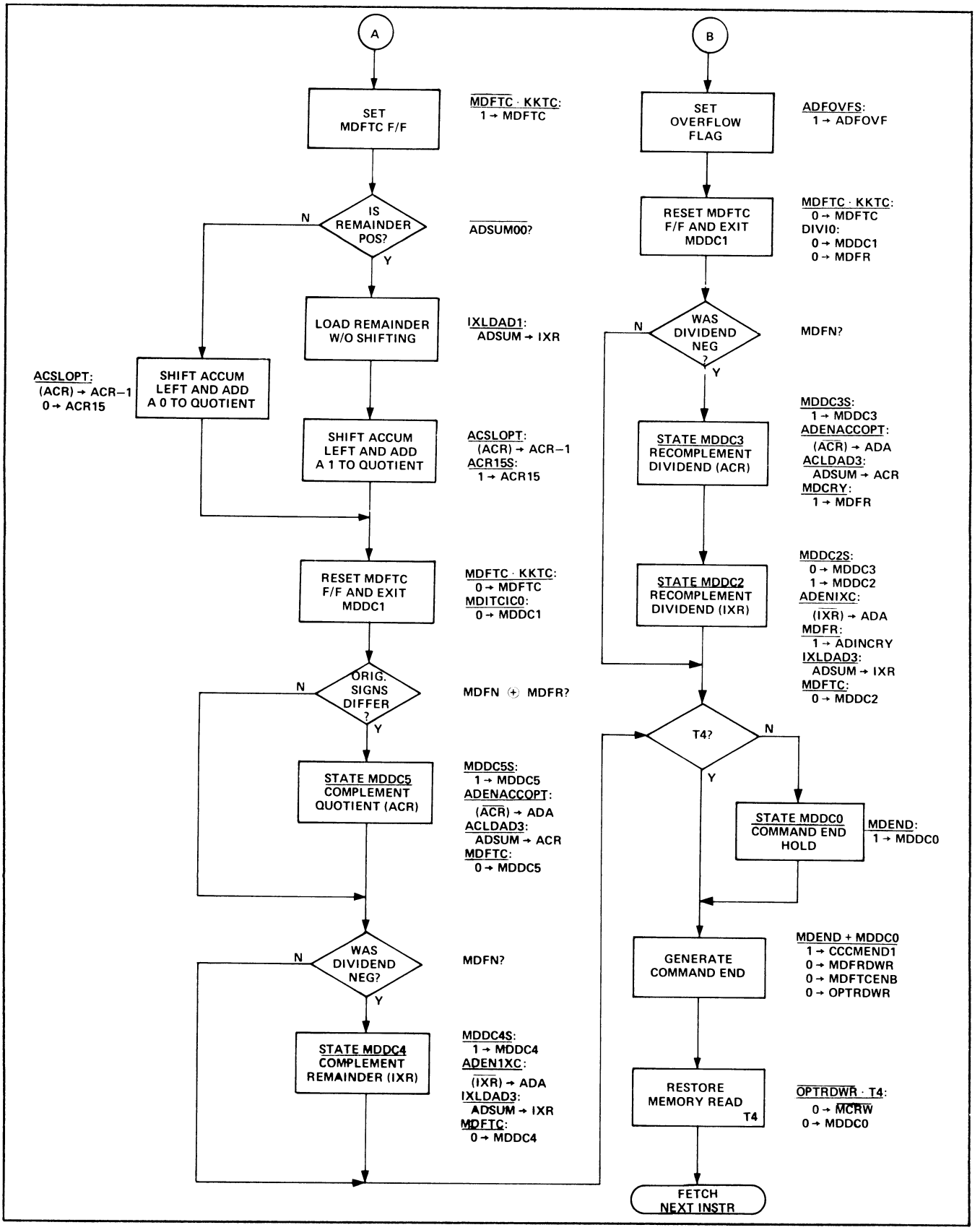


Figure 4-16. Divide Instruction Execution Flow Diagram (Sheet 2 of 2)

already reset. The MDFR flip-flop is cleared for reuse, however, in either case.

4-352. During time period TB of the machine cycle, the adder is used to complement the divisor read in during time period TA, if its sign is negative. State DIV04 is true (MDF11DIV TBMD), which makes signal ADENMBC2 true also and gates the inverted outputs of the memory buffer register into the adder input B gates. Without signal ADINCRY being true, the adder provides the 2's complement of the divisor at its sum outputs. Now if the sign of the original divisor is negative, signals MBLDADRB0- and MBLDADLB0- will go false during time period T3 (MDF11DIV MBR00 T3MD), setting flip-flop MDFR to store the negative sign of the divisor and gating the ADSUM outputs of the adder back to the memory buffer register inputs.

4-353. Once both the dividend and the divisor are positive numbers, the process of iterative subtractions can begin. Iterative processing starts immediately after the MDDC1 flip-flop is set, which occurs at the end of the next T4 time period. Memory access is disabled by placing an inhibiting high level on the MCRW- line at time period T4 and thereafter until the command-end state is reached.

4-354. The setting of flip-flop MDFTCENB enables the clock for timing control flip-flop MDFTC, allowing it to toggle at the time period clock rate; that is, at 5 times per machine cycle. Before proceeding, the function of this flip-flop should be clearly understood. Each repetition of an iteration cycle in the MDDC1 state requires two time periods. The first time period is defined by the MDFTC flip-flop being in the reset state, always. It is at this time that the inputs to the adder are first enabled so that the carry propagation of subtraction (complement addition) can be completed before the adder outputs are copied. The next clock toggles the MDFTC flip-flop set, beginning the second time period. During this period the actual conditional subtraction does or does not take place, depending upon whether or not the adder sum outputs are gated back to the inputs of the index register. The other MDDC states through which the instruction sequencing may pass also require two time periods each and make use of the toggling of the MDFTC flip-flop to distinguish the first time period (MDFTC-) from the second (MDFTC). A new cycle or state is started each time the MDFTC flip-flop toggles reset.

4-355. State MDDC1 is the basic algorithm state, during which the iterative loop repeats until the count in the iteration counter is reduced to zero. It requires 15 two-period cycles to do this, unless the sequence is interrupted by detection of overflow during the first iteration. In the first time period, a trial subtraction is performed. Signal ADENIX2 gates the contents of the index register to the adder input A gates, and signal ADENMBC2 gates the inverted outputs of the memory buffer register to the adder input B gates. Both of these control signals are functions of MDDC1 being set; consequently, these same two sources of adder input data are constantly enabled during the entire iterative portion of the instruction.

4-356. Three general iteration conditions are recognized by the state MDDC1 logic: the first iteration, when the count is F_{16} (ICDCF true); the last iteration, when the count is 0 (ICDC0 true), and the intermediate iterations, when the count is smaller than F but larger than 0 (ICDC0NFN true). Each has its own function and conditional sequencing.

4-357. After the MDFTC flip-flop is set, the sign of the remainder (state of ADSUM00) is checked. When the remainder is positive (ADSUM00 is 0), it means that the absolute value of the divisor is smaller than the absolute value of the 16 most-significant bits of the dividend or dividend remainder and that subtraction is permissible. Signal IXLDADSL gates the adder sum outputs back to the index register through MD logic shift-left gates so that they arrive shifted one bit position toward the more significant end. The same signal also gates the content of the accumulator register most-significant magnitude bit ACR01 to index register least-significant bit position IXR15 input. Simultaneously, signal ACSLOPT sets up the accumulator register for a direct left-shift operation, and a one is shifted into the ACR15 bit position as a significant quotient bit.

4-358. If the remainder from the trial addition is negative (ADSUM00 is 1), it means the subtraction is not permissible. If this occurs on the first iteration, overflow is indicated, and the MD logic immediately leaves the MDDC1 state and goes into an instruction termination sequence which will be discussed shortly. At any other time, however, the dividend remainder and quotient are merely shifted left one bit position without the subtraction being completed. This is accomplished by signals IXSLOPT, IXSR15S, ACSLOPT and ACR15S-. The IXSLOPT signal enables index register direct left-shift gates, and signal IXR15S gates the output of accumulator bit register ACR01 into index register least-significant bit register IXR15. Signal ACSLOPT enables the direct left-shifting of the accumulator register, as before, while signal ACR15S- causes a zero to be shifted into the ACR15 accumulator bit register as a significant bit of the quotient.

4-359. At the same time that the coupled index and accumulator registers are being set up to perform a load and/or shift operation, signal ICDECOPT enables the iteration counter to down count. When the second time period clock occurs, the index and accumulator registers are reloaded, the iteration count is decremented by one, and the MDFTC flip-flop is reset, beginning the first time period of the next MDDC1 cycle.

4-360. After the fifteenth iteration, the accumulator register contains only one bit of the original dividend in bit register ACR00, and the iteration count is zero (ICDC0 true). During the second time period of the last cycle, after the MDFTC flip-flop has been set, the sign of the trial final trial subtraction is looked at. If the remainder is still positive, signal IXLDAD1- is made false to complete the subtraction by loading the remainder back into the index register, but this time without the displacement one bit position to the left. Left-shifting of the accumulator register is enabled by signal ACSLOPT, as usual, and a 1 is shifted into the least-significant bit position by making signal ACR15S true. But if the remainder is negative, the contents of the index register are not changed, signal ACSLOPT left shifts the accumulator register, and signal ACR15S is made false to shift in a zero as the last bit of the quotient. The second period clock that performs these final operations on the index and accumulator registers also causes the MDFTC flip-flop to toggle reset and resets the MDDC1 flip-flop.

4-361. The next procedure, after division has been completed, is to determine the signs of the final quotient and remainder and to complement any negative resultants. It will be recalled that the original sign of the dividend was stored in the MDFN flip-flop and the original sign of the divisor was stored in the MDFR flip-flop prior to the recomplementing of negative operands. If these two original signs differ (MDFN $\oplus$ MDFR), it means that the final quotient is negative and the contents of the accumulator register must be complemented. This is done by advancing to state MDDC5. If the original signs are the same and negative (that is, the dividend was negative and MDFN is set), the remainder of the negative dividend must also be negative, and the contents of the index register must be complemented. This is done by advancing to state MDDC4, either directly from state MDDC1 or two time periods later from state MDDC5. Now if both original signs were positive to begin with, states MDDC5 and MDDC4 are bypassed, advancing directly from MDDC1 to state MDDC0, the command-end state.

4-362. State MDDC5 is a two time-period state entered into if flip-flop MDDC5 set enable signal MDDC5S is true when the clock resets flip-flop MDDC1. This signal can only be true if the stored operand signs differ and it is the last time period of the last iteration ((MDFN MDFR- + MDFN- MDFR) MD1TCIC0). As soon as the MDDC5 flip-flop is set, signal ADENACCOPT becomes true, gating the inverted outputs of the accumulator register into the adder input A gates. After the MDFTC flip-flop is set by the next clock, signal ACLDAD3 gates the ADSUM outputs of the adder (complement of the quotient, since the ADINCRY signal is not active) back to the accumulator register inputs. The next clock loads the register and resets flip-flops MDFTC and MDDC5.

4-363. State MDDC4 is also a two time-period state entered by the setting of the MDDC4 flip-flop. Signal MDDC4S will be true during the last time period of the MDDC1 state, if both stored

signs are negative (MDFN MDFR MD1TCIC0) or during the last time period of state MDDC5, if the stored sign of the dividend is negative (MDDC5 MDFTC MDFN). As soon as the MDDC4 flip-flop is set, signal ADENIXC gates the inverted outputs of the index register into adder input A gates. After the MDFTC flip-flop is set by the next clock, signal IXLDAD3 gates the ADSUM outputs of the adder (complement of the remainder, since the ADINCRY signal is not active) back to the inputs of the index register. The next clock loads the register and resets flip-flops MDFTC and MDDC4, preparatory to ending the instruction.

4-364. Before analyzing DIV instruction command-end logic, consider the sequence of events for instruction termination when overflow is detected in the first iterative cycle. This happens when the remainder of the first trial subtraction is negative (MD1TC ICDCF ADSUM00) and is indicated by the false state of signal DIV10-. As soon as DIV10- becomes false, signal ADFOVFS- becomes false and the next clock sets overflow flip-flop ADFOVF. If the original dividend held in the coupled index and accumulator registers was negative, as indicated by the MDFN flip-flop being set, it must be recomplemented back to its original form, one register at a time, before terminating the instruction. In this case, the clock that resets the MDDC1 flip-flop to end the MDDC1 phase also sets flip-flop MDDC3 and resets flip-flop MDFR, entering state MDDC3.

4-365. The purpose of state MDDC3 is to recomplement the less-significant half of the dividend held by the accumulator register, when the instruction is terminated by detecting overflow. As soon as the MDDC3 flip-flop is set, signal ADENACCOPT gates the inverted outputs of the accumulator register to adder input A gates. Signal ACLDAD3 gates the adder ADSUM outputs back to the accumulator register inputs during the second time period of the state. The next clock reloads the accumulator with the 2's complement of its content and sets the MDFR flip-flop previously cleared, if complementing causes overflow (MDCRY true). This represents a carry into the more-significant half of the dividend and is stored until that half is recomplemented.

4-366. The logic advances unconditionally from state MDDC3 to state MDDC2. State MDDC2 is a two time-period phase during which the index register portion of a negative dividend is restored. The MDDC3 flip-flop is reset and the MDDC2 flip-flop is set by the same clock. With the MDDC2 flip-flop set, signal ADENIXC gates the index register inverted outputs into the adder input A gates. Also, signal ADINCRY will be generated if the MDFR flip-flop remains reset. This will cause the more-significant half of the dividend complement to be a 1's complement. The ADINCRY signal will not be generated if a carry was stored from the preceding state MDDC3, however (MDFR set). In this case, the 2's complement will be formed to account for the carry from the less-significant half of the dividend. Signal IXLDAD3 gates the adder ADSUM outputs back to the index register inputs during the second time period of the state, and the next clock reloads the index register and resets flip-flop MDDC2.

4-367. The command-end signal, MDEND, becomes true just as soon as no further processing of the final quotient and remainder (or dividend in overflow terminated operations) is required. During the DIV instruction execution, this is indicated by signal DIV13-, DIV14-, or MDDC0S4- being false. The DIV13- signal is false unconditionally during the second time period of state MDDC2, after completing the dividend recomplementation. The DIV14- signal is false unconditionally during the second time period of state MDDC4, after complementing the remainder. Finally, signal MDDC0S4- is false when advancing directly from state MDDC1 or state MDDC5 to the end-of-command phase.

4-368. As soon as signal MDEND is generated, the CCCMEND1- line to the CPU command-end logic goes false to terminate the instruction. If the CPU machine cycle is not in the T4 time period, the next clock sets flip-flop MDDC0. This is a command-end holding state and keeps MDEND true until the end of the next T4 time period, when the flip-flop will be reset. Since signal MDEND- is no longer true, signal OPTRDWR- is no longer active, removing the inhibit level from the memory access control logic. Also, the reset inputs of flip-flops

MDFRDWR and MDFTCENB are activated by MDEND, and the next clock resets them, disabling the memory access inhibit latch and MDFTC flip-flop toggle action.

4-369. Memory read-write access is fully restored at the end of time period T4. The clock at the end of this time period advances the CPU sequence counter to the fetch phase, and the false level on memory control signal MCRW- line enables the next instruction to be fetched.

4-370. MEMORY SYSTEM

4-371. The minimal configuration of the 704 Processor is provided with an internal main memory having a capacity of 4096 18-bit words (16 data bits plus right- and left-byte parity check bits). Destructive readout (DRO) magnetic core arrays with integral X- and Y-line drivers, Z-inhibit drivers, and Z-sense amplifiers for 4096 words mounted on a single memory module assembly provide the building blocks which allow easy plug-in expansion of the memory system up to a full internal capacity of 16,384 words. Memory data and address buffer registers and the logic which generates memory timing and control signals are a part of the basic CPU and are shared by all memory module assemblies (up to four) in the memory system.

4-372. The DRO core memory operates in a conventional manner, going through read and restore phases when data is retrieved and through clear and write phases when data is stored. Total memory cycle time for either operation is one machine cycle.

4-373. Primary access to the memory system is through the CPU. However, a direct memory access option, made operational by plugging in a DMA card, gives memory access to external devices connected to the direct memory access bus connector (DMAC) without disturbing the CPU. When the DMA option is operational, DMA requests for memory access take precedence over similar CPU requests by merely suspending CPU operation temporarily until the direct memory access operation is completed. The direct memory access option is discussed more fully, starting at paragraph 4-535.

4-374. Figure 4-17 is a block diagram of CPU and DMA card functional elements that take part in memory system addressing, data transfer and storage, and in memory system read-write control. In it, data word transfer paths to and from the memory modules are shown by heavy lines. The memory module block on the right represents from one up to four memory modules receiving inputs and supplying outputs in parallel, except as noted. However, only one memory module may be addressed for access at any given time.

4-375. Memory Addresses

4-376. The memory address word is 15 bits in length. This word length permits addressing of up to 32,768 discrete locations; however, as presently configured, the 704 Processor memory system provides a maximum of only 16,384 discrete locations. The first bit of the address word is not used (must be zero), and the second and third bits of the address specify the memory module (0 through 3) to be enabled (must be 00 to address module 0 in 4096-word memory systems). The remaining 12 bits of the address specify the word location (0000 through 4095) within the memory module enabled.

4-377. The three most significant bits of the address are gated from the memory address register inputs for bits 0 through 3 (MAR01S through MAR03S), decoded, and made to set one of four module enable flip-flops (MCFEN0 to MCFEN3), the outputs of which are sent to the memory modules, enabling one of them. The 12 least significant bits of the address come directly from the memory address register outputs (MAR04 through MAR15) and are applied, in parallel, to all memory modules, where the enabled memory module decodes them to select appropriate X- and Y-line drivers. Memory module logic is discussed in paragraph 4-477.

4-378. Module enable flip-flops MCFEN0 through MCFEN3 (Dwg 394562, Sht 5) supply the memory module enabling signal (ground on one of the MCFEN0- through MCFEN3- lines). Each flip-flop serves one memory module card of 4096-word locations. Ungated clock KKMCEN causes the flip-flops to copy the outputs of a four state decoder for memory address register inputs

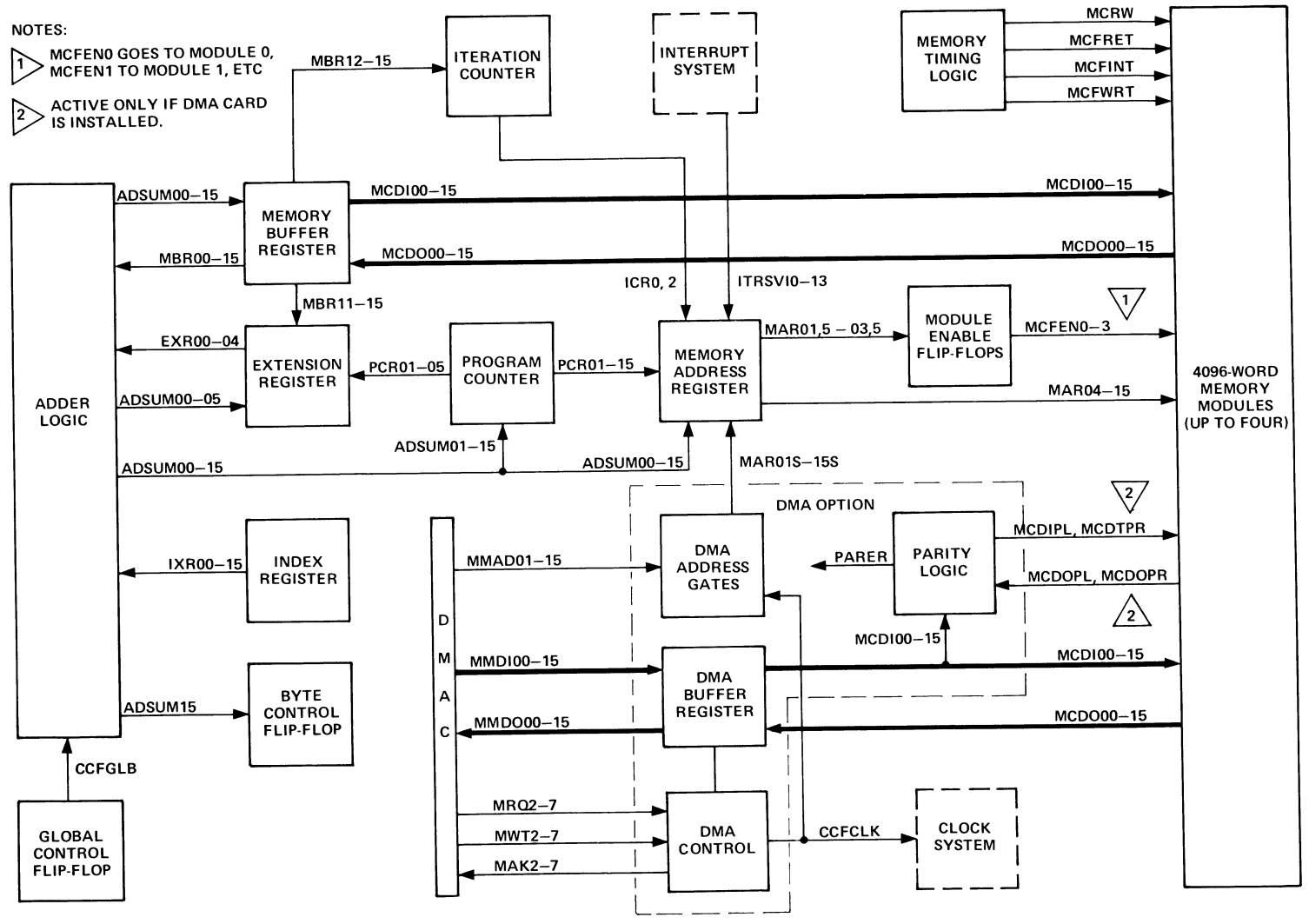


Figure 4-17. Memory Addressing and Data Transfer Block Diagram

MAR01S through MAR03S at the end of each T4 time period. For example, if all three input bits are 0's, detector gate MCFEN0R output will be false, causing flip-flop MCFEN0 to be set, and any previously set flip-flop to be reset.

Note

To make the D-input of a D-type flip-flop function as a $\overline{D}$-input, the logical functions of outputs Q and $\overline{Q}$ are reversed (that is, $\overline{Q}$ true is considered the set state).

In the same manner, detected bit states 001, 010, or 011 will set flip-flop MCFEN1, MCFEN2, or MCFEN3, respectively.

4-379. Automatic addressing of memory module 0 occurs whenever the CPU sequences to the start of an interrupt service cycle or to the start of interrupt return (MALDIT + MALDIC). Signal MARDRL- becomes false (ground) at this time for two 20-mc clock intervals, directly setting MCFEN0 and directly resetting MCFEN1, MCFEN2, and MCFEN3 flip-flops. The same signal also directly resets memory address register flip-flops MAR04 through MAR09, effectively forcing an address restricted to the first 64 memory locations. The operational significance of this is discussed in paragraph 4-420.

4-380. A module enable flip-flop is set in accordance with bits MAR01S through MAR03S at the beginning of each machine cycle, enabling a memory module. Likewise, the memory address register supplies positive-true outputs for the remaining 12 address bits to the memory modules, whether memory access will be performed or not. Memory access is independent of the addressing function; operationally, memory access is under complete control of memory timing logic (paragraph 4-433).

4-381. The memory address field of non-generic instruction words is used to form the address of operands or the address of the next instruction in program jumps. This field contains only 11 bits; the other four bits of the address must be added to it before it can be used to address a memory location. This formation of operand addresses is discussed in paragraph 4-406.

4-382. Since the 11-bit memory address field can address only 2048 words, this field gives rise to the concept of *word pages*. In this concept, the most-significant bit of the 12-bit word is grouped with the 2-bit module number to form a 3-bit word page number (0 through 8). The remaining 11 bits of the address specify one of the 2048 words in the page (0000 to 2047). Once the memory address word is formed, the concept of pages has no further significance in the CPU logic or the memory module logic, and the address is treated as a 3-bit module address followed by a 12-bit word address.

4-383. It is also possible to address either the left or right byte of a memory word, and this leads to further subdivision of the memory into *byte pages* of 2048 bytes each. Since there are twice as many bytes as words in memory, 16 bits are required to address all byte locations of a 32,768 word memory. In this case, a 5-bit *byte page number* is added to the 11-bit memory address field to form the 16-bit address.

4-384. Individual bytes cannot be accessed in memory, and the 15 most-significant bits of the byte address are used to address the word containing the byte. The 16th bit is used in the CPU to select the left or right byte of the word. In practice, the 16-bit byte address is formed and is then divided by two by shifting it one place to the right. The quotient is used as the word address, and the remainder (least-significant bit shifted off) is stored in byte control flip-flop CCFBYTE in the CPU control logic (paragraph 4-61). If the remainder is a 0, the left (even) byte of the word from memory is copied; the right (odd) byte is selectively copied if the remainder is a 1.

4-385. The concept of breaking down the memory locations into word pages of 2048 words each and into byte pages of 2048 bytes each is illustrated in figure 4-18 for a 16,384-word memory. The module number plus the most-significant bit of the word number define the 8 word page addresses. In effect, this is simply addressing the first 2048 locations (0000 through 2047) of a module when

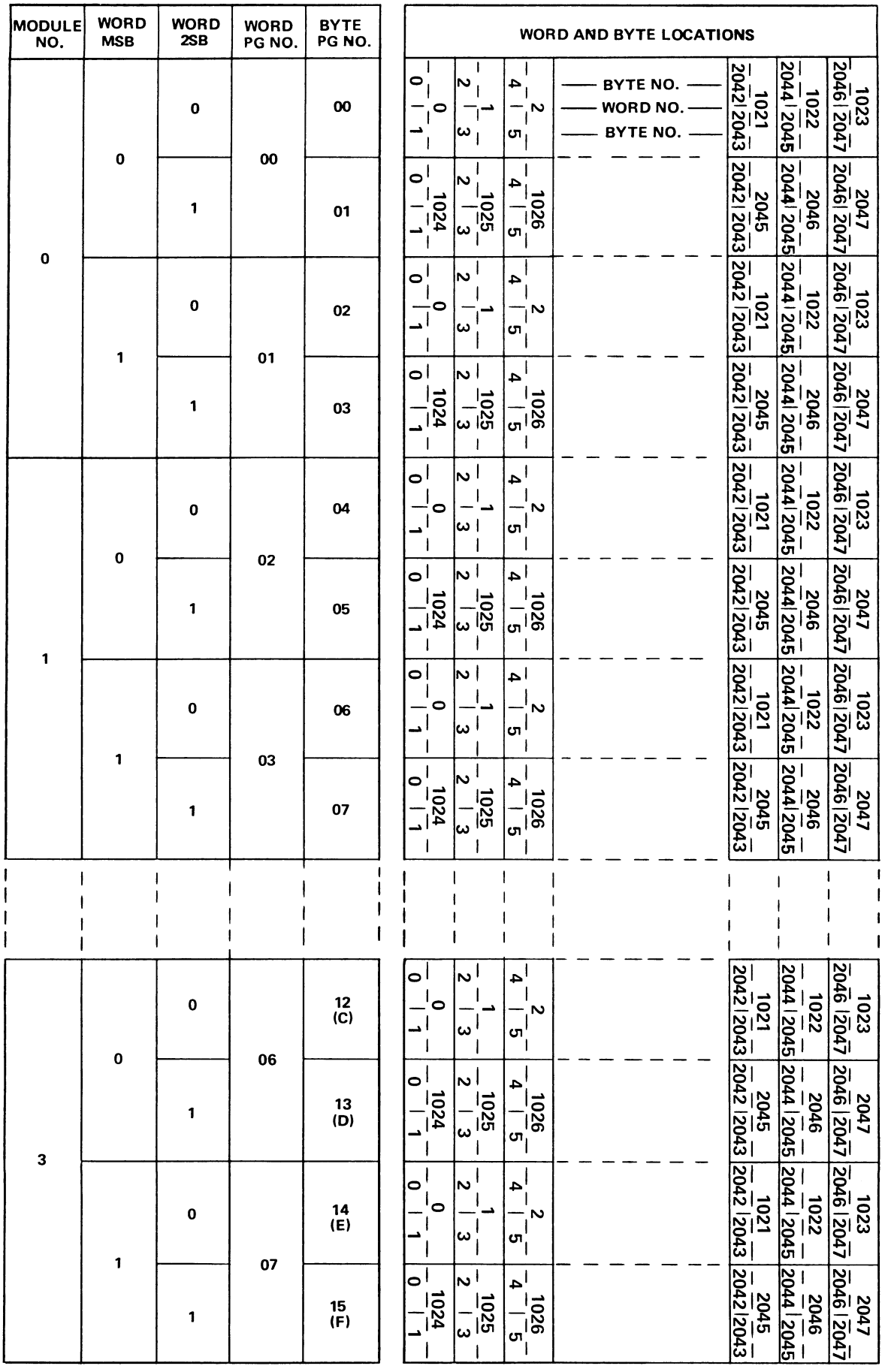


Figure 4-18. Memory Word Page and Byte Page Addressing (4096-Word Modules)

the most-significant bit is 0 and the last 2048 locations (2048 through 4095) when the most-significant bit is 1.

4-386. The module number plus the two most-significant bits of the word number define the 16 byte page numbers. This breaks the word locations of a module into four blocks of 1024 words each (0000-1023, 1024-2047, 2048-3071, and 3072-4095), and the remaining 10 bits of the memory address specify one of the 1024 words in the selected block. The 1024 words are broken down into 2048 bytes in the CPU, as described above.

4-387. Memory Address Register

4-388. The memory address register is a 16-bit register, consisting of type-D flip-flops MAR00 through MAR15 (Dwgs 545497 — 500, Sht 6) which supply the 15-bit memory address word to the memory enable flip-flops and to the memory modules. Flip-flops MAR00 through MAR03 are logically redundant, since bit 0 is never used, and bits 1, 2, and 3 are taken directly from the set input gates and applied to the memory enable flip-flops. This register is contained on the four Arithmetic cards with the four most-significant flip-flops on Arithmetic card 1 and four flip-flops on each of the other Arithmetic cards 2, 3, and 4.

4-389. The source of the address may be the adder, the program counter, or "forced" addresses generated in the memory address register control logic, depending on the operation being performed.

4-390. The contents of the program counter (PCR01 through PCR15) are gated into the inputs of the memory address register (MAR01S through MAR15S) by signal MALDPC (Dwg 394557, Sht 7) whenever an adder output address is not to be used, an address is not being forced, and the CPU clock has not been inhibited for direct memory access (MALDAD- MALDADSR- MALDPC1 CCFCLK). Addresses are forced only during an interrupt service cycle or an interrupt return cycle. At times other than these, the address is either the address of the next instruction to be executed, the address of an operand, or an externally supplied address for direct memory access.

4-391. The address of the next instruction to be executed is the same as the program count in the program counter, but is not necessarily loaded into the memory address register from the program counter register. In some cases, the incremented program count is not loaded into the program counter register from the adder until the moment when one instruction execution cycle is completed and the next is started. In these cases, the adder output must be loaded into the program counter and the memory address registers simultaneously in order for the address of the next instruction to be in the memory address register in time to address the next instruction.

4-392. The program count is gated into the memory address register inputs from the adder (ADSUM01 through ADSUM15) by signal MALDAD, if a program skip occurs during the execution of a skip generic instruction (SCDC1 SCDC7R CCFSKP CCFCLK); during the execution of JMP or JXS instructions (SCDC1 SCDC7R INDCBYTE- INDC0- CCFCLK); during the read memory phase of INR instructions, and during the load link phase of interrupt service cycles (SCDC1-CCCMENDA CCFCLK). These cases are discussed in detail in the discussion of program execution (paragraph 4-126).

4-393. Operand addresses are gated into the memory address register inputs from the adder during the fetch phase of all non-generic instructions. If the instruction is a word instruction (SCDC1 INDCBYTE- INDC0- CCFCLK), the operand address is gated into the memory address register by signal MALDAD. Bits 01 through 15 of the operand address are gated into the corresponding memory address positions.

4-394. During the fetch phase of byte instructions CMB, LDB, and STB; signal MALDADSR is generated (SCDC1 SCDC7R INDCBYTE CCFCLK), which gates bits 00 through 14 of the operand address into memory address bit positions 01 through 15. In effect, the operand address is divided by 2 by the one position right shift, and bit 15 of the byte address is gated into byte control flip-flop CCFBYTE (paragraph 4-61). The manner in which the operand addresses are formed is discussed in paragraph 4-406.

4-395. The memory address register clock is enabled during time period T4 of each machine cycle (MACLKEN). At the end of the time period, the address at the register inputs are loaded into the register by ungated clock KKA or KKB.

4-396. Extension Register

4-397. The extension register (Dwg 394567) is used in conjunction with the memory address field of memory access instructions to form the direct memory address for operands. It consists of five flip-flops (EXR00 through EXR04) located on the Adder Flip-Flop card. Operational use of the extension register in the formation of operand addresses is discussed in paragraph 4-413.

4-398. The extension register receives its inputs from the program counter register (PCR01 through PCR05), the memory buffer register (MBR11 through MBR15), and from the adder (ADSUM00 through ADSUM05). It is clocked at the end of time period T4 of each machine cycle during which an input is gated to the register (EXLDAD + EXLDADSR + EXLDMB + EXLDPC).

4-399. The inputs from bits 01 through 05 of the program counter are gated into the flip-flop inputs by signal EXLDPC during the fetch phase of all non-generic instructions except JMP and JSX (SCDC1 INDC0- INDC1- INDC2-), copying the local page number of the instruction being executed into the extension register. The local page number may or may not be used in forming an operand address in the next instruction phase, depending on the addressing mode of the instruction (paragraph 4-419).

4-400. Execution of a JMP or JSX instruction causes the local page number of the next instruction to be copied into the extension register from the adder at the same time that the address of the next instruction is loaded into the program counter register from the adder. Signal EXLDADSR (SCDC1 INDC1OR2) gates adder outputs ADSUM01 through ADSUM05 to the register flip-flop inputs, and the page number is loaded into the register at the end of fetch phase time period T4.

4-401. Signal EXLDADSR also copies the local page number of the first instruction of an interrupt service routine into the extension register at the end of the interrupt service cycle load-link phase (SCDCD). The address of the instruction is copied into the program counter register from the adder at the same time.

4-402. Three control generic instructions enable the contents of the extension register to be altered under program control. The CXE instruction copies the contents of bits 00 through 04 of the index register into the extension register. The SML or SMU instructions copy a literal number contained in the F2 field (bits 12 through 15) plus the last digit of the instruction code (bit 11) into the extension register. Consequently, the SML instruction resets flip-flop EXR00 and the SMU instruction sets flip-flop EXR00 as the contents of their F2 field are copied into flip-flops EXR01 through EXR04.

4-403. When a CXE instruction is executed, signal ADENIX gates the contents of the index register into adder input gate A during the last half of the instruction fetch phase. Adder outputs ADSUM00 through ADSUM04 are gated to the extension register inputs by signal EXLDAD, whenever this instruction is detected (SCDC1 INDC007), so that index register bits IXR00 through IXR04 are effectively copied into EXR00 through EXR04 at the end of fetch phase time period T4.

4-404. When an SML or SMU instruction is executed, signal EXLDMB gates bits MBR11 through MBR15 from the memory buffer register, which contains the last bit of the instruction code (1 for SMU code 009 and 0 for SML code 008) plus the F2 field of the instruction, to the inputs of flip-flops EXR00 through EXR04 (SCDC1 INDCXX8 + SCDC1 INDCXX9). This data is loaded into the register at the end of the instruction fetch phase time period T4.

4-405. During an interrupt service cycle, the contents of the extension register are stored in memory as part of the machine status word. When machine status is restored at the end of the interrupt service routine by an INR instruction,

signal EXLDAD gates bits ADSUM00 through ADSUM04 from the adder into the register inputs during the interrupt return phase of INR instruction execution (SCDC9). The register clock is enabled during time period T4, and the contents of the extension register are restored at the end of the time period.

4-406. Operand Addressing

4-407. The manner in which an operand address is formed depends upon the addressing mode in effect (direct, indexed local, or indexed global) and whether it is a word address or a byte address. The memory addressing logic is the same as for instruction addressing, but the address that is placed into the memory address register is assembled in the adder after the instruction is needed. The use of the memory address field of the instruction in forming word or byte addresses and the concepts of word and byte "pages" has been discussed in paragraph 4-375.

4-408. Operand addresses are formed during the last half (time periods T2, T3, and T4) of the fetch phase of all non-generic instructions. The addresses formed during the execution of jump instructions JMP or JSX are not the addresses of operands, but the addresses of the next instruction, and cannot properly be called operand addresses. However, these addresses are formed in the same manner and by the same logic as the true operand addresses and are included in this discussion for convenience.

4-409. Since the operand address is formed from the 11-bit word or byte address contained in the memory address field of the instruction word and a word or byte page number, and may be modified by the contents of the index register, the final address send to the memory address register is called the effective word address. Effective byte addresses may be divided into an effective word address and a byte location (left or right), as explained in paragraph 4-383, but only the effective word address is sent to the memory address register.

4-410. The addressing mode of all non-generic instructions, except JSX, is determined by the states of bit 04 of the instruction and by the state of global control flip-flop CCFGLB. Bit 04 of the instruction word determines whether direct (INR04 is a 0) or indexed (INR04 is a 1) addressing will be used. The JSX instruction ignores the state of the global control flip-flop during indexed addressing and forces the addressing to be in the indexed global mode.

4-411. The terms "local" and "global" refer to the word page number that will form part of the effective address and only have significance during indexed addressing. The "local" page is the memory word page containing the instruction being executed, and the effective word address is indexed relative to an address in this word page, in indexed local mode. In indexed global mode, the local page number is ignored, and the effective word address is indexed relative to an address in word or byte page zero.

4-412. Direct addressing may be used to address any word or byte in memory. If the word or byte lies outside the local word or byte page, it is necessary to place the word or byte page number of the location into the extension register by means of an SML or SMU instruction before executing the instruction that will address the location.

4-413. The method of forming word and byte addresses in the direct mode is shown in figure 4-19. The direct mode is specified in the instruction word when the index bit (INR04) is 0. When the instruction code is for any non-generic instruction except byte instructions CMB, LDB, or STB, the word page number is gated into adder input gate B bits ADB01 through ADB04 by signal ADENEXW (Dwg 394552, Sht 6) during the last half of the instruction fetch phase [SCDC1 TIRCA- (CCFGLB + MBR04-)]. At the same time, the memory address field of the instruction word is gated into ADB05 through ADB15 by signal ADENMBR to complete the direct word address.

4-414. Adder input gate A is inhibited in direct addressing, and the effective word address at the adder output is the same as the direct word address. Bits ADSUM01 through ADSUM15 from the adder are gated into the memory address register inputs by signal MALDAD, and the

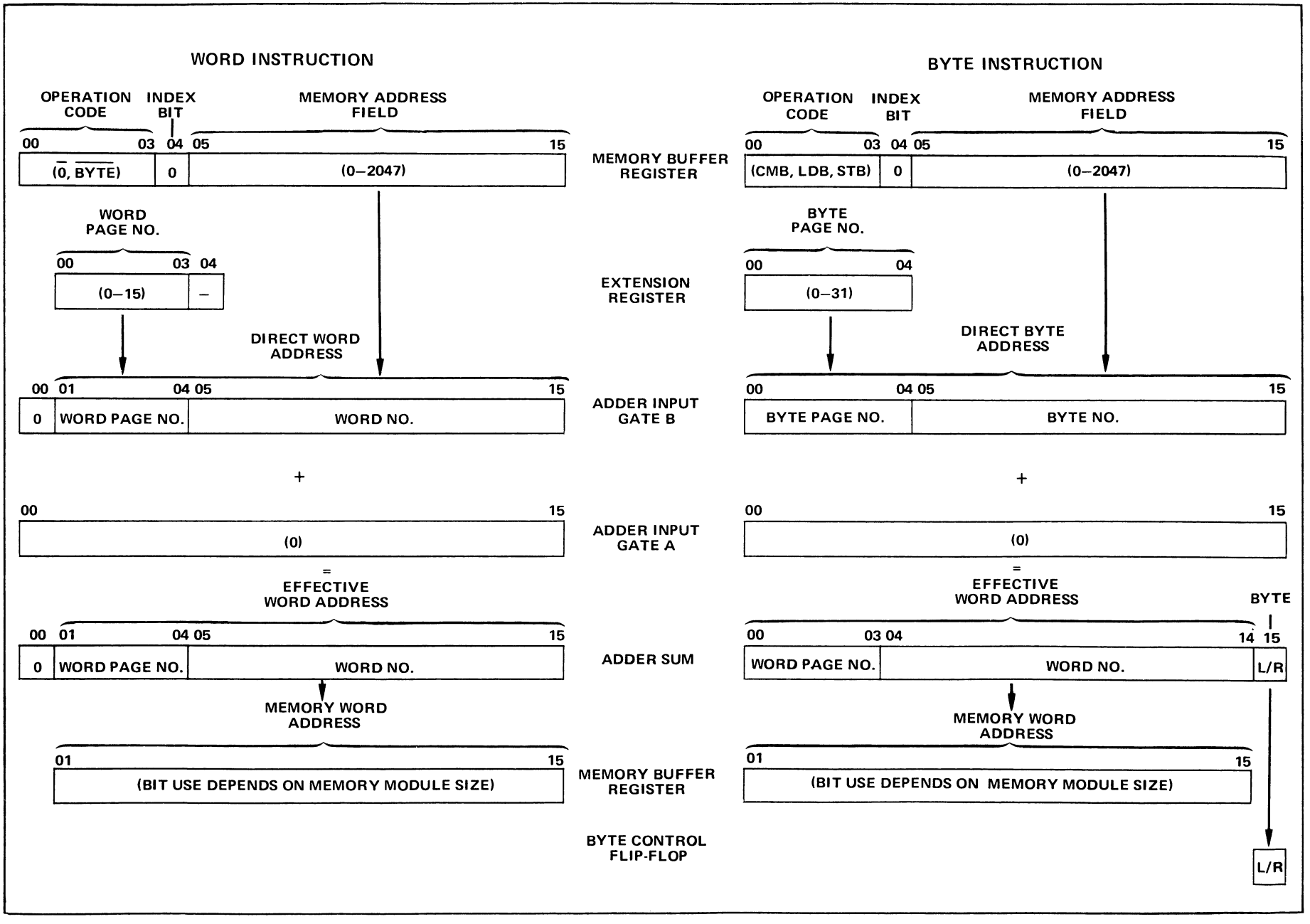


Figure 4-19. Operand Address Formation in Direct Mode

effective word address is loaded into the register at the end of time period T4 to address the operand in the next machine cycle.

4-415. When a byte instruction is executed (CMB, LDB, or STB), the direct byte address is formed in adder input gate B the same as a direct word address, except that the byte page number is gated into ADB00 through ADB04 from the extension register by signal ADENEXB [SCDC1 TIRCA-(CCFGLB + MBR04-)]. The adder output is the same as the direct byte address, but the output is separated into an effective word address and a byte designator bit.

4-416. The effective word address (ADSUM00 through ADSUM14) is gated into the memory address register by signal MALDADSR and is loaded into the register at the end of time period T4 to address the word containing the byte during the next machine cycle. The byte designator bit (ADSUM15) is stored in byte control flip-flop CCFBYTE (Dwg 394567, Sht 6) at the end of time period T4 (T4SCDC1 INDCBYTE) to control the selection of the left (CCFBYTE-) or right (CCFBYTE) byte of the word after it is brought into the CPU.

4-417. Address formation in the indexed local mode (figure 4-20) is the same as direct addressing except that the JSX instruction cannot be executed in this mode, and the address modifier is gated into adder input gate A from the index register by signal ADENIX (Dwg 394552, Sht 6) when the index bit (INR04) is 1 (SCDC1 TIRCA- MBR04). The effective word or byte address at the adder output is the sum of the direct word or byte address and the address modifier word, so that it is indexed relative to an address in the word or byte page number contained in the extension register.

4-418. The JSX instruction inhibits signal ADENEXW when indexing is specified in the instruction word and forces the instruction to be executed in the indexed global mode, regardless of the state of global control flip-flop CCFGLB. The CCFGLB flip-flop (Dwg 394567, Sht 6) is set to the global mode at the end of time period T4 of the fetch phase of executed JSX instructions (T4SCDC1 INDC2).

4-419. In the indexed global mode, signals ADENEXB and ADENEXW are inhibited by both CCFGLB and MBR04 signals being true, and the extension register is not used in the formation of the direct word or byte address (figure 4-21). This places all 0's in the word or byte page number of the direct address, and the effective address is indexed relative to a word or byte in word or byte page zero.

4-420. Forced Memory Addresses

4-421. Forced addressing is used to address interrupt storage locations during CPU interrupt service and interrupt return cycles. The forced address logic, shown in Drawing 394557, Sheet 8, can handle up to 16 levels of interrupt, although the 704 Processor may be equipped with no more than one or perhaps eight interrupt levels.

4-422. The first 64 locations in memory are reserved (unprotected) for use as interrupt storage locations. Four memory locations are allocated to each interrupt level, so that interrupt storage can be thought of as 16 blocks containing four word locations each. The words making up each block have the following storage functions.

Word 0 (00) — Program Count
Word 1 (01) — Service Routine Link Address
Word 2 (10) — Machine Status Word
Word 3 (11) — Not Used

Memory address bits 10 through 13 provide the block address, and bits 14 and 15 provide the word location address within each block.

4-423. In practice, interrupt storage locations are addressed by forcing memory address bits 01 through 09 to the all-zero state (first 64 locations), bits 10 through 13 to copy the interrupt level number from some register (block address), and bits 14 and 15 to change in a manner appropriate to the interrupt sequences. Address forcing is initiated whenever signal MALDIT or MALDIC becomes true, activating signal MARDRL-.

4-424. The MALDIT signal is generated when the CPU is about to enter an instruction fetch phase

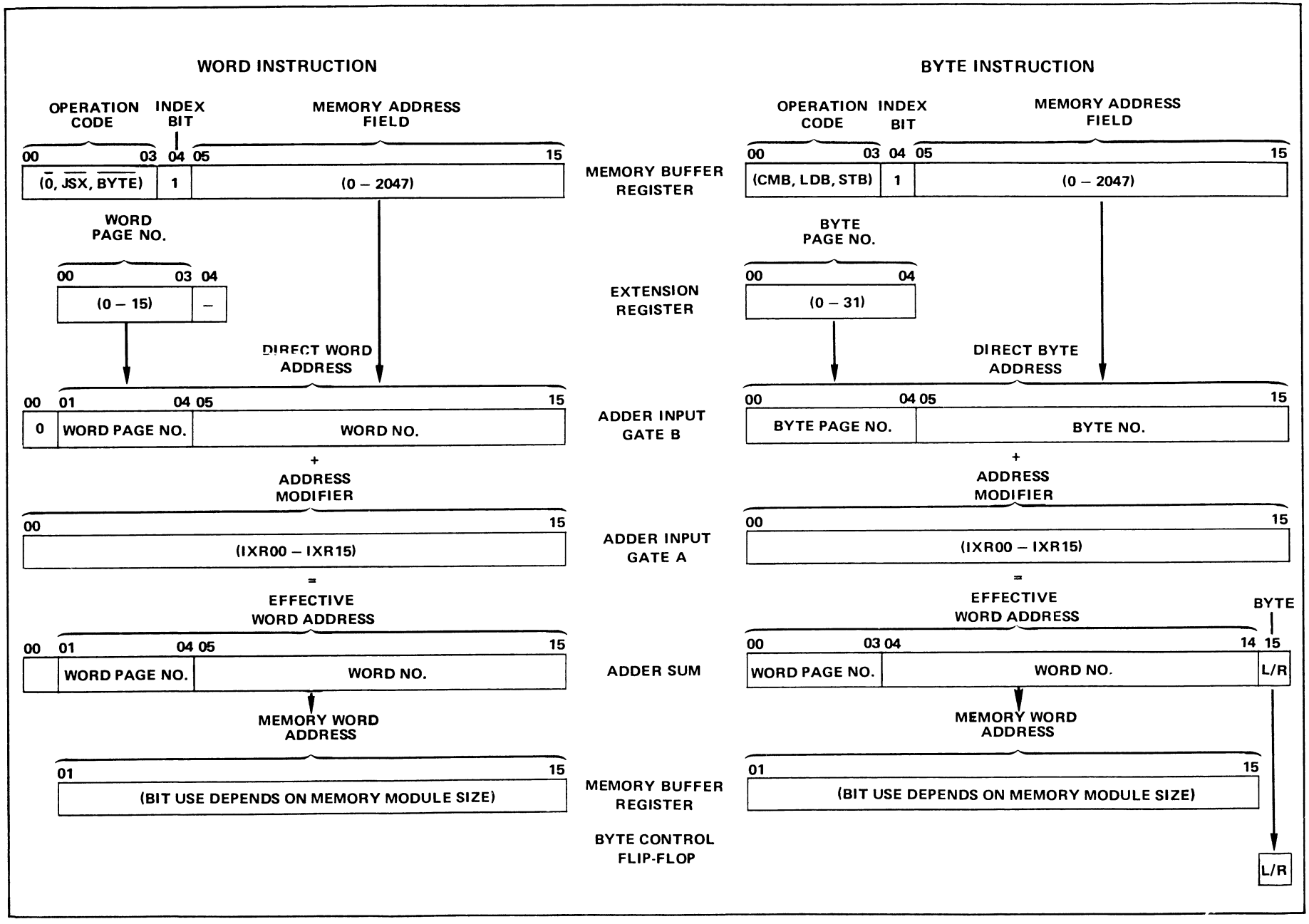


Figure 4-20. Operand Address Formation in Indexed Local Mode

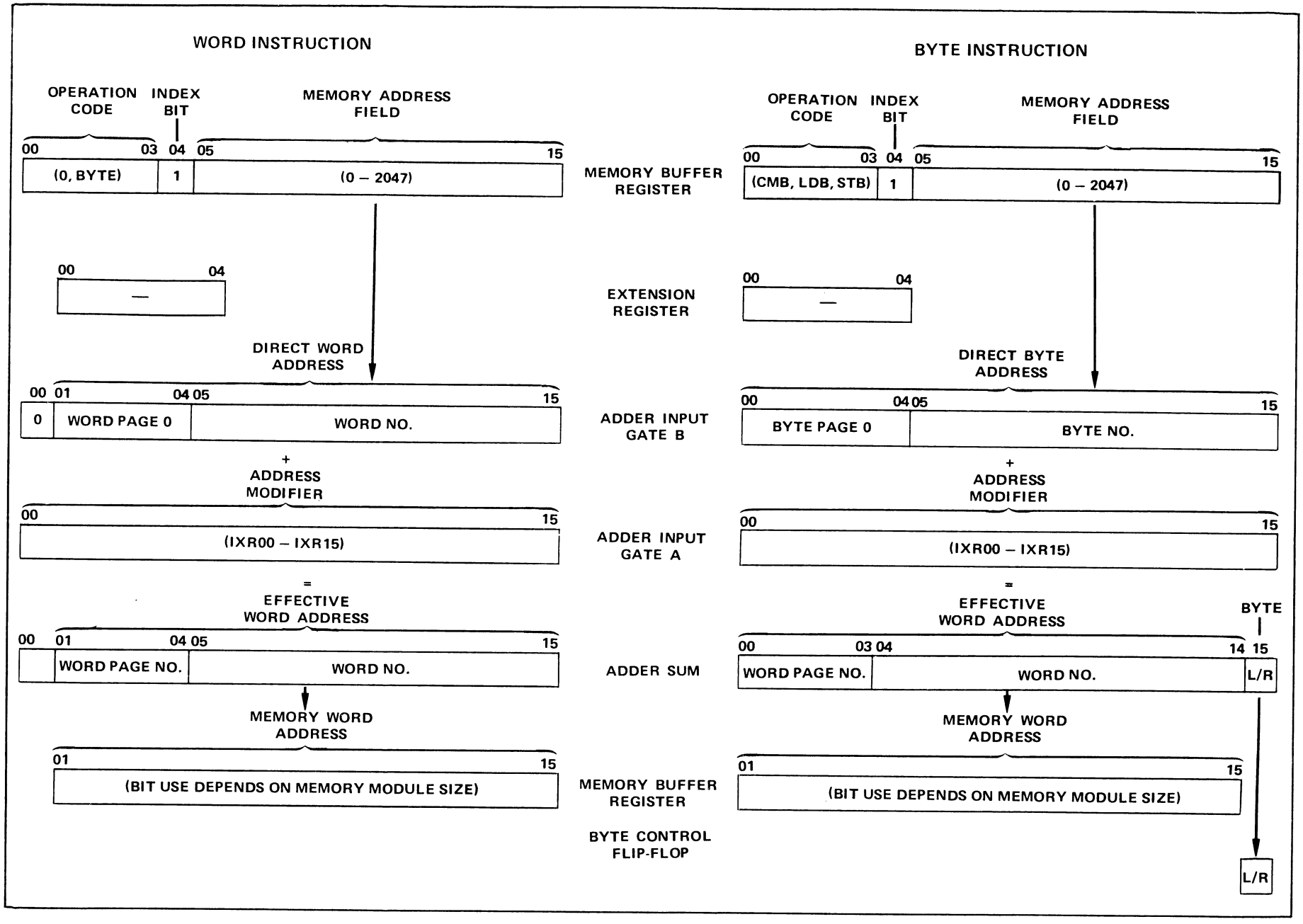


Figure 4-21. Operand Address Formation in Indexed Global Mode

and an interrupt service cycle is called for (SCDC7R-) and during the first two phases of the interrupt service cycle (SCDC7ORB). Signal MALDIT is detected prior to entry into phase 7 so that the address MCENMAS goes false, which inhibits program count load signal MALDPC and MCENMAS goes false, which inhibits program count load signal MALDPC and triggers flip-flop MARDRL.

4-425. The MARDRL flip-flop performs as a synchronous one-shot and when triggered, signal MARDRL- goes false (ground) for 100 ns in the middle of the next T4 time period. This signal automatically resets the memory enable flip-flops to activate memory module 0 and directly resets memory address register flip-flops MAR00 through MAR09, forcing the upcoming address to the first 64 locations in memory.

4-426. Signal MALDIT gates the contents of interrupt service flip-flops ITRSV10 through ITRSV13 to memory address register inputs MAR10S through MAR13S to address the block appropriate to the level of interrupt. And since the sequencer has not entered the interrupt service cycle yet (SCDC7- SCDCB- true), bits MAR14S and MAR15S are at state 00 when the next clock loads the inputs into the memory address register and the cycle enters phase 7. It is during this phase that the program count is stored into word 0 of the appropriate interrupt storage block.

4-427. The memory address to be used during phase B is forced at the inputs of the memory address register during phase 7. Since the condition SCDC7 SCDCB- is now true, bits MAR14S and MAR15S are at state 10 as the sequencer leaves phase 7 and enters phase B. It is during this phase that the machine status word is stored into interrupt block word 2.

4-428. Entry into phase B sets up the conditions for forcing the forced address for memory access during the next phase, phase D. Now the condition SCDC7- SCDCB is true, making bits MAR14S and MAR15S assume the state 01, which is clocked into the memory address register as the sequencer enters phase D. It is during this phase that the linking address to start the interrupt service routine is loaded from interrupt block word 1 into both the program counter and the memory address register. Since the MALDIT signal is not true during phase D, the processing of memory access addresses returns to normal.

4-429. Encountering the INR instruction at the end of the interrupt service routine generates the precondition SCDC9R- true, activating signal MALDIC. This signal initiates the forcing of interrupt return memory addresses by making MCENMAS false, which inhibits MALDPC and triggers flip-flop MARDRL, as before. Once again, memory module 0 is enabled and memory address register flip-flops MAR00 through MAR09 are directly reset.

4-430. The block location address appropriate to the service routine interrupt level is contained in the F2 field of the INR instruction. By happy circumstance, this field is copied by the iteration counter during the fetch phase of all instructions, even though it is only used operationally to control iterative shifting. So bits 12 through 15 of the INR instruction are transferred to memory address register inputs MAR10S through MAR13S via the iteration counter (ICR0 through ICR3-), as long as MALDIC remains true.

4-431. Phase 9 of the interrupt return cycle is used to retrieve the machine status word from block storage word 2 location. To do this, bits MAR14S and MAR15S are forced to the 10 state by the condition MALDIC SCDC1 prior to entering phase 9. Entry into phase 9 loads the forced memory address into the memory address register and sets up the conditions for forcing the next address to be used during phase 5.

4-432. Phase 5 of the interrupt return cycle is used to retrieve the program count from the word 0 storage location. During phase 9, bits MAR14S and MAR15S assume the 00 state, since condition MALDIC SCDC1- is now true. This word address is loaded into the memory address register at the end of phase 9 so that the word 0 storage location of the block will be accessed during phase 5. Once the sequencer leaves phase 9, signal MALDIC becomes false, disabling the forced address logic so that normal data processing can resume.

4-433. Memory Control Logic

4-434. Every read or write memory access operation requires one complete machine cycle to execute. During any one machine cycle, only one memory location can be addressed. That is, it is not possible to load in data from one memory location and store it in another memory location without performing separate memory-read and memory-write operations, requiring two machine cycles. However, because of destructive readout each time a memory location is activated, each cycle consists of a read phase followed by a write phase. This is true regardless of the external read or write demands of the operation performed.

4-435. When instruction or operand data is read from memory, all cores of the memory location addressed are switched to the "zero" state, causing those which were in the "one" state to induce a signal on bit oriented sense lines. These are picked up by sense amplifiers and placed on the memory data output lines (MCDO00 through MCDO15, MCDOPL and MCDOPR) during machine cycle time period T0 or T1. This data is loaded into the memory buffer register when it occurs.

4-436. Since the content of the memory location addressed was destroyed in the readout process, it must be restored by writing the content of the memory buffer register back into the memory location cores. This occurs during machine cycle time periods T2, T3, and T4 when all cores are switched back to the "one" state. Data from the memory buffer register on memory data input lines (MCDI00 through MCDI15, MCDIPL and MCDIPR) activates inhibit drivers in the memory which supply a bucking current to all cores which should remain in the zero state, in order to duplicate the data on the input lines. So a memory-read operation actually consists of sequential read and restore operations performed on the same memory location during one machine cycle.

4-437. When a memory-write operation is performed, the same sequence of events takes place within the memory. The cores of the memory location addressed are switched to the "zero" state, but the data detected by the sense amplifiers is not loaded into the memory buffer register — this being merely a clearing operation. Then during the write phase of the machine cycle, the data in the memory buffer register is made to activate the inhibit drivers so that it is stored in the memory location correctly, as in the restore phase of memory-read operations. Thus, a memory-write operation consists of clear and write operations performed on the same memory location during one machine cycle.

4-438. Signals that enable and time data entering and leaving the memory buffer register are functionally part of the memory buffer register control logic (paragraph 4-444). Memory control logic (Dwg 394562) is involved with the generation of four signals which actually activate the memory module electronics and consequently control memory timing. These include memory access enable signal MCRW-, memory read timing control signal MCFRET-, memory inhibit timing control signal MCFINT-, and memory write timing control signal MCFWRT-.

4-439. The false state of signal MCRW- enables activation of the memory modules. This signal is under control of flip-flop MCFRDWR. The MCFRDWR flip-flop is clocked at the end of each T4 time period (TIRC4 KKGAT) and copies the state of its D-input gate signal MCOPRDS. The MCOPRDS signal will be true at the start of each non-memory access phase of the sequencer (SCDC0R- + SCDC4R- + SCDCCR- + OPTRDWR). Term OPTRDWR comes from the multiply-divide option sequencer.

4-440. Because inverted outputs of the flip-flop are used (that is, true signal MCFRDWR comes from the $\overline{Q}$ output), the MCFRDWR signal will be true during each memory access machine cycle. If the CPU is not in the single-step mode (CCFSSTP-), signal MCRW- will be false for the entire machine cycle, enabling the memory modules to respond to the other three memory timing control signals. If the CPU happens to be in single step mode, pressing the SINGLE STEP switch at the beginning of a memory access phase causes MCRW- to become false for the one machine cycle duration of the sync flip-flop set state (CPSSTP MCFRDWR CCFSYN1), enabling memory access to occur. The CPDIAEN CCFSYN1

gate of the MCRW- logic is for memory access during manual display or entry of memory data (paragraph 4-470).

4-441. Memory timing control signals MCFRET-, MCFINT-, and MCFWRT- are generated during each machine cycle, critically timed by basic clock pulses, so long as the CPU power is on. Naturally, they cannot activate the various operating functions of the memory modules unless the MCRW- signal has enabled them. Each is generated by a separate J-K flip-flop clocked by the negative-going edges of KK20MC clock pulses. The false state of each output is the memory activating state.

4-442. The first KK20MC negative clock transition after the start of time period T0 (TIRC0) sets the MCFRET flip-flop, making MCFRET- false and activating the memory-read function (assuming memory access is enabled). The flip-flop is reset at the end of time period T1 (TIRC1 C1), making MCFRET- true and terminating the memory-read operation. Next, the MCFINT flip-flop is set by the first KK20MC negative clock transition after the start of time period T2 (TIRC2), making MCFINT- false and activating the memory write inhibit drivers. Before the MCFINT flip-flop is reset, flip-flop MCFWRT is set. This occurs at the end of time period T2 (TIRC2 C1), making MCFWRT- false, which activates the memory-write function. The memory-write operation is terminated by resetting flip-flop MCFWRT shortly after the start of time period T4 (first negative KK20MC clock transition that occurs during TIRC4). Finally, the write inhibit drivers are deactivated by resetting the MCFINT flip-flop shortly before the end of time period T4 (TIRC4 C4). The "run out" C4 interval corresponds to the C2 interval.

4-443. Memory control signal timing is shown in idealized form by figure 4-3. The actual timing of these signals, relative to the basic timing intervals of the CPU and the availability of memory address and data signals (and also considering practical circuit delay tolerance limits) can be seen in figure 5-3.

4-444. Memory Buffer Register

4-445. The memory buffer register is used to hold data being stored into or loaded from the memory modules. It consists of 16 type-D flip-flops located on the four Arithmetic cards (MBR00 through MBR15; Dwgs 545497 — 500, Sht 4).

4-446. The flow of data to and from the memory buffer register is shown in figure 4-8. Inputs to the register come from the memory module data output lines (MCDO00 through MDCO15) during memory-read operations and from the CPU adder (ADSUM00 through ADSUM15) during memory-write operations. Outputs from the register go to the memory module data input lines (MCDI00 through MCDI15) during all memory access operations and to several data and control elements of the CPU during memory-read operations, depending upon the specific operation being performed or instruction being executed.

4-447. When a memory access phase is entered by the CPU sequencer, signal MCENB3 becomes true (SCDC1 + SCDC3 + SCDC5 + SCDC7 + SCDC9 + SCDCB + SCDCD + CPDIS CCFSYN1). This signal enables the gate which generates signal MBRDR-, and MBRDR- goes to ground for 50 ns before the end of time period T0 (MCENB3 TIRC0 C1 CCFCLK), directly resetting all flip-flops in the memory buffer register. Consequently, whenever a memory access machine cycle occurs, the memory buffer register will be in the cleared state by the start of time period T1, provided memory access has not been relinquished to the optional direct memory access logic (CCFCLK-).

4-448. The memory buffer register clocks (KKMB) control the loading of data from the adder (ADSUM00- through ADSUM15-) prior to storing it into memory. The clocks are byte selectable; that is, the KKMB clocks which clock data into registers MBR00 through MBR07 are under the control of left-byte clock enable signal MBLDADLB, and the KKMB clocks which clock data into registers MBR08 through MBR15 are controlled by right-byte clock enable signal MBLDADRB.

4-449. During the write phase of store left-byte STB instruction execution (SCDC3 CCFBYTE-), signal MBLDADLB2 only will be true, and MBLDADLB will be enabled during time period T1

(MBLDADLB2 TIRC1). Clocking of left-byte-only data into the memory buffer register occurs at the end of that time period.

4-450. Similarly, during the write phase of store right-byte STB instruction execution (SCDC3 CCFBYTE), only signal MBLDADRB2 will be true, enabling MBLDADRB during the T1 time period (MBLDADRB2 TIRC1). Clocking of right-byte-only data into the memory buffer register occurs at the end of the time period.

4-451. At all other times when data is to be stored into memory, signals MBLDADLB2 and MBLDADRB2 will both be true simultaneously to load full words from the adder. This occurs during the write phase of STW and STX instruction execution (SCDC3 INDCBYTE-), during interrupt cycle storage of the program count (SCDC7), and during interrupt cycle storage of the machine status word (SCDCB). As before, the clock gates are enabled during time period T1, and loading occurs at the end of that time period. The data loaded into the memory buffer register is immediately available on the memory data input lines MCDI00 through MCDI15, provided the MBR00- through MBR15- output gating signal MCENMB is true. This signal comes from the direct memory access logic, when installed, and is false only during the time that the DMA logic option is accessing memory.

4-452. Data read from memory comes via memory data output lines MCDO00 through MCDO15 and is loaded asynchronously into the memory buffer register through its direct set inputs. Asynchronous loading is used because the data signals come directly from the memory sense amplifiers as nominal 50 ns pulses which can occur within a 100 ns region of time period T1.

4-453. The load-from-memory input gates are controlled by byte selectable enable signals MBLDMCLB and MBLDMCRB. Signal MBLDMCLB is the left-byte enable signal and controls the transfer of memory data outputs to direct set inputs MBR00DS- through MBR07DS-, and signal MBLDMCRB is the right-byte enable signal that controls the transfer of right-byte memory data outputs to direct set inputs MBR08DS- through MBR15DS-.

4-454. During the execution of full-word store-into-memory operations, both MBLDMCLB and MBLDMCRB signals are disabled (MBLDADLB2 and MBLDADRB2 true). This inhibits memory data coming in during the read phase of the memory access machine cycle from being loaded on top of the adder output data which is to be stored during the machine cycle write phase. Also, both signals will be inactive whenever the DMA option has memory access control (ACDLY- false) or when manually entering data into memory (MCWRENT- false).

4-455. When the write phase of a store left-byte STB instruction occurs, signal MBLDMCLB is inactive and signal MBLDMCRB is active (MBLDADLB2 true, MBLDADRB2 false), so that the left byte of the assembled word written back into memory will consist of adder data and the right byte will consist of memory data. The converse is true during the write phase of a store right-byte STB instruction (MBLDADLB2 false, MBLDADRB2 true). At all other times except those mentioned above, both direct set enable signals will be active, permitting full-word memory output data to be loaded into the memory buffer register.

4-456. Data may be loaded manually into the memory buffer register when the CPU is halted by means of the switches on the front control panel (paragraph 4-470). These inputs are applied to the direct set inputs of the register flip-flops (MBR00DS- through MBR15DS-). Any time that the DISPLAY SELECTOR switch is in the MB position, signal DISPMB will be true, causing the memory buffer register outputs to be displayed by the SELECTED DISPLAY indicators and the SELECTED DISPLAY switch inputs (DISPENB00 through DISPENB15) to be enabled. Normally, the register will first be cleared, and then the 1's will be entered, as required, by pressing the appropriate front panel switches. These set corresponding bit flip-flops in the memory buffer register.

4-457. Load and Store Instructions

4-458. Six instructions are used specifically to load or store memory data words or bytes. These instructions are LDB, LDW, LDX, STB, STW, and STX. The arithmetic and logical instructions also

load words from memory and are discussed in paragraph 4-220. Also, memory words are loaded and stored during interrupt service and return cycles; these operations are discussed in paragraphs 4-607 and 4-614.

4-459. When a load-from-memory instruction is executed, an operand address is formed during the instruction fetch phase (paragraph 4-406) and loaded into the memory address register at the end of the phase. The sequence counter enters the memory read phase from the instruction fetch phase, and a memory access cycle is initiated at the beginning of the machine cycle. The memory buffer register is cleared at the start of time period T0, and the word from the addressed memory location is loaded into the memory buffer register during time period T1.

4-460. The addressed word or byte is then transferred from the memory buffer register to the accumulator register or to the index register (word only) via the adder. Signals ADENMBL and ADENMBR (Dwg 394552, Sht 6) gate the contents of the memory buffer register into adder input gate B during the memory read phase of LDW and LDX instructions.

4-461. Signal ACLDAD (Dwg 394552, Sht 4) gates the adder outputs into the accumulator register inputs during the memory read phase of LDW instructions. The register right- and left-byte clock enable signals ACCLKENBL and ACCLKENBR are both activated during time period T4 of the phase, and the word from memory is loaded into the register at the end of the phase.

4-462. Signals IXLDADL and IXLDADR (Dwg 394567, Sht 11) gate the adder outputs into the index register inputs during the memory read phase of LDX instructions. Clock enable signals IXCLKENBL and IXCLKENBR are both activated during time period T4 of the phase, and the word from memory is loaded into the index register at the end of the phase.

4-463. The LDB instruction reads the entire memory word containing the addressed byte into the memory buffer register. Byte control flip-flop CCFBYTE contains the least-significant bit of the byte address (paragraph 4-394) and determines whether the left or right byte is loaded into the accumulator. The addressed byte is always loaded into the right-byte half of the accumulator register (ACR08 through ACR15).

4-464. During the memory read phase of LDB instructions, signal ADENMBB (Dwg 394552, Sht 6) gates the outputs of the left-half of the memory buffer register (MBR00 through MBR07) into the right half of adder input gate B (ADB08 through ADB15), if the CCFBYTE flip-flop contains a 0. If it contains a 1, signal ADENBR gates the outputs of the right half of the memory buffer register (MBR08 through MBR15) into the right half of the adder input gate B (ADB08 through ADB15). Signal ACLDAD gates the full-word output of the adder into the accumulator register inputs, but only the right half of the register (ACR08 through ACR15) is enabled for loading, during time period T4 (ACCLKENBL false, ACCLKENBR true). When the clock occurs at the end of the time period, the selected memory byte is loaded into the right-byte position of the register.

4-465. When a store-into-memory instruction is executed, an operand address is formed during the instruction fetch phase and loaded into the memory address register at the end of the phase. The sequence counter then enters the memory write phase, and the memory buffer register is cleared for loading.

4-466. Instructions STW and STX store full words. Words are gated into adder input gate A from the accumulator register or from the index register by signals ADENAC and ADENIX, respectively. The output of the adder (ADSUM00- through ADSUM15-) is clocked into the memory buffer register at the end of time period T1 (MBLDADLB and MBLDADRB true). Thereafter, it is written into the addressed memory location during time period T3 of the memory write phase.

4-467. If an STB instruction is being executed, a "mixed" word must be assembled in the memory buffer register, consisting of accumulator register right-byte data placed in either the left- or right-byte location plus the unaffected byte data from the memory location addressed. The assembled word is then written back into the same memory

location. All of this occurs during the memory write phase of the instruction.

4-468. Byte control flip-flop CCFBYTE contains the least-significant bit of the byte address and determines whether the byte from the accumulator register replaces the left or right byte of the word in the memory buffer register. If the flip-flop is in the 0 state, signal ADENACRB gates the accumulator register right byte (ACR08 through ACR15) into the left-byte position of the adder input gate A (ADA00 through ADA07), and the adder left-byte output will be clocked into the left-byte position of the memory buffer register at the end of time period T1 (MBLDADLB true). During the same time period, the data read from memory will be loaded into the right-byte position only of the memory buffer register (MBLDMCRB true). The word thus assembled in the memory buffer register is written back into the addressed memory location during time period T3 of the memory write phase.

4-469. When the CCFBYTE flip-flop is in the 1 state, signal ADENAC gates the full word from the accumulator register into the adder input gate A. However, only the right-byte output of the adder (ADSUM08 through ADSUM15) will be clocked into the right-byte position of the memory buffer register at the end of time period T1 (MBLDADRB true). During the same time period, the data read from memory will be loaded into the left-byte position only of the memory buffer register (MBLDMCLB true). The word thus assembled in the memory buffer register is written back into the addressed memory location during time period T3 of the memory write phase.

4-470. Manual Display and Entry

4-471. The contents of memory locations may be displayed or words may be entered by means of the indicators and controls on the CPU front control panel. Manual display or entry of memory locations is enabled when the CPU is halted and the DISPLAY SELECTOR switch is set to MB. This causes the contents of the memory buffer register to be displayed automatically by the SELECTED DISPLAY indicators and the SELECTED DISPLAY switch inputs to the memory buffer register to be enabled.

4-472. The address of the memory location, or the starting address of a sequence of memory locations, to be accessed must be manually entered into the program counter register by means of the PROGRAM COUNTER switches (paragraph 4-57) before initiating the memory access operation manually. If it is desired to display the contents of the memory location addressed by the program counter, as seen on the PROGRAM COUNTER indicators, the DISPLAY switch is pressed. This initiates one memory read cycle to load the memory buffer register with the data contained in the memory location so that it can be seen on the SELECTED DISPLAY indicators. The program counter is automatically incremented by one during the process.

4-473. If it is desired to enter data into the memory location addressed by the program counter, the data must first be entered manually into the memory buffer register (paragraph 4-73) The ENTER switch is then pressed, initiating one memory write cycle which stores the contents of the memory buffer register into the memory location. Again, the program counter is automatically incremented by one during the process.

4-474. When the CPU is halted, the content of the program counter register is copied by the memory address register at the end of each machine cycle (MALDPC true). Consequently, the address placed into the program counter register will also be in the memory address register when the display or entry is executed.

4-475. When either the DISPLAY or ENTER switch is pressed, signal CPDIAEN is true (CPDIS + CPENT, Dwg 394557). This signal triggers the one cycle synchronizing flip-flop CCFSYN1 at the start of the next machine cycle. During the one cycle that flip-flop CCFSYN1 is set, the condition CPDIAEN CCFSYN1 activates MCRW- to initiate a memory access operating (paragraph 4-439), makes signal ADENPC true to transfer the program count into the adder for incrementing, and also makes PCLDAD true to load the program counter register with the adder output resultant (paragraph 4-135).

4-476. When the DISPLAY switch is pressed, the true condition CPDIS CCFSYN1 enables memory

buffer register direct reset signal MBRDR- to be generated at the beginning of time period T0, clearing the register to receive the data read out of memory. When the ENTER switch is pressed, the true condition CPENT CCFSYN1 makes memory buffer register input enable signals MBLDMCLB and MBLDMCRB false, preventing memory output data generated while the memory location is being cleared from ruining the data in the memory buffer register which is to be stored (paragraph 4-454).

4-477. CORE MEMORY MODULES

4-478. Core memory modules for the 704 Processor consist of two printed circuit board assemblies connected to form a larger assembly. Each module provides the magnetic core arrays and attendant read-write electronic circuits for 4096 18-bit words of storage. The modules use standard coincident current 3-wire techniques for location addressing, destructive readout data retrieval, and data restoration. Module selection and most read-write timing control signals are generated externally and are provided by the CPU.

4-479. Each 4096-word core memory module consists of two interconnected printed circuit boards, as mentioned. One of the boards mounts most of the electronic components and the other mounts primarily the magnetic components. The board upon which all matrices of the magnetic core array are mounted (with their X-drive, Y-drive, and sense-inhibit lines) is called the stack assembly.

4-480. Stack Assembly

4-481. The stack assembly (Drawing 394690) contains 73,728 magnetic core elements, one for each bit of the 4096 18-bit words (4096 x 18). These elements are grouped as eighteen squares with 64 elements on a side. Each square (64 by 64 matrix) represents storage for a particular bit in all 4096-word storage locations. That is to say, the 18 matrices are bit position oriented and the cores within the matrices are word location oriented.

Note

The detailed structure of the magnetic core array is discussed here only to aid understanding of the addressing and line drive schemes used. This must not be taken as license to attempt core replacement or other repairs to the array.

4-482. Drawing 394696 shows the general layout of the magnetic core array and the scheme employed for threading the X- and Y-drive lines through the cores. Notice that the X-drive lines are threaded along the axis of the array. A particular X-drive line starts at one of the four corner matrices, passes through all cores aligned within a particular row of matrices in one direction, passes through another string of cores within the middle row of matrices in the opposite direction, and then passes through the same line of cores in the third row of matrices to end at the diagonally opposite corner of the array. The opposite end of a line is indicated by an overbar on the line name (opposite end of line X0 is $\overline{X0}$, etc).

4-483. Y-drive lines are threaded through the cores along the short axis of the array. By following the Y0 line from the bottom left-hand corner of the diagram to the bottom right-hand corner, it can be seen that the scheme is similar to the X-drive line scheme. Notice that the Y0 line (as a typical example) is threaded up through the left-hand column of cores in matrices 0, 11, and 12, and is threaded down through the right-hand column of cores in matrices 13, 10, and 1. The only significance which should be ascribed to this is that it keeps line crossovers around the periphery of the array to a minimum. It is certainly unnecessary to be so familiar with the array wiring that one can easily locate the core element for a specific word within any bit position matrix.

4-484. The sense-inhibit (Z-) lines are completely matrix oriented; that is to say, each bit position matrix has its own independent sense-inhibit line which threads all 4096 cores in the matrix. Drawing 394696 shows the threading pattern for this line used in all 18 matrices. It is difficult and unnecessary to understand why this pattern was chosen except that it provides the correct polarity for the inhibit driver bucking current and consistent polarity of a sense amplifier input induced on the line by the read switching of any core in the matrix. What is important about this line is that it

is "doubled" and has three "ends." The three "ends" include the two actual wire ends (designated S and $\overline{S}$ followed by the bit matrix number) connected to the sense amplifiers and a center-tapped end (designated I and followed by the bit matrix number) connected to the inhibit driver. Consequently, the sense amplifiers "see" the cores of its matrix strung serially along a single line, while the inhibit driver "sees" the cores of the matrix equally divided between two parallel driven lines. The significance of this will be seen shortly.

4-485. Functional Organization

4-486. The electronic circuits which provide the location-addressing coincident currents on the X- and Y-drive lines, the detection of core switching produced by read currents, and the write-one bucking currents on the Z-drive (inhibit) lines are assembled on the main circuit board assembly of the memory. Figure 4-22 is a block diagram of the memory and shows its general organization. The functions include: (1) address decoder, (2) Y-line read and write current sources, (3) Y-line current drivers, (4) Y-line current sinks, (5) X-line read and write current sources, (6) X-line current drivers, (7) X-line current sinks, (8) Z-line bit sense amplifiers, (9) Z-line bit inhibit drivers, and (10) module enable and read-write timing control.

4-487. Core memory modules receive memory address register output signals on lines MAR04 through MAR15 whenever power is on. These signals are grouped by threes (MAR04, 5, 6; MAR07, 8, 9; etc) and decoded into X- and Y-line addressing signals by four binary-to-octonary decoders. Thus each full 12-bit address produces four true signals, one from each decoder. These select one of eight X-line drivers, one of eight X-line sink switches, one of eight Y-line drivers, and one of eight Y-line sink switches.

4-488. By a process which will be explained shortly (paragraph 4-490), the activation of one of eight X-line drivers and one of eight X-line sink switches will cause current flow in one of 64 X-axis location addressing lines of the magnetic core array. The same is true for the Y-line circuits. Since any one of 64 X-lines and any one of 64 Y-lines can be activated, any one of 4096 memory word locations (64 x 64) is accessible, the location addressed being determined by where the two intersecting coincident currents can effect core switching.

4-489. As mentioned earlier, the Z-lines that pass through all cores of a given bit matrix do double duty. They serve as sense lines during the read switching phase of memory access, during which they transmit induced signals to the data readout sense amplifiers which drive the MCDO data output lines. They also serve as inhibit lines during the write switching phase of memory access. At this time, those data bits on the MCDI data input lines which are zeroes cause corresponding bit inhibit drivers to provide a bucking current which nullifies (at least in their bit locations) what would otherwise be a write-all-ones operation. This is common core memory technique and will not be discussed further.

4-490. X - Y Address Lines

4-491. Figure 4-23 shows in three-dimensional diagrammatic form how the selection of one X-line driver and one X-line sink can select one of the 64 X-lines of the array. This function is what is labeled X-Line Select Matrix (8 x 8) in Figure 4-22. As can be seen, it has more to do with the manner of driver, array, and sink interconnection than with circuitry. Naturally, this whole function and discussion apply to the Y-line drivers and sinks as well.

4-492. First, notice that the drivers and sinks are connected to opposite ends of the X-drive lines in such a manner that each services eight lines. Further, no driver has more than one line in common with any sink. So by addressing one driver and one sink, a specific X-line will be addressed. Drivers and sinks are called by their input line names: X-line driver 0 (XRD0) through X-line driver 7 (XDR7), X-line sink 0 (XSO0) through X-line sink 7 (XSO7), Y-line driver 0 (YDR0) through Y-line driver 7 (YDR7), and Y-line sink 0 (YSO0) through Y-line sink 7 (YSO7). Table 4-3 lists the combinations of X-line drivers and sinks which address the X-lines. By substituting the letter Y for the letter X in the table, it becomes valid for Y-line addressing as well.

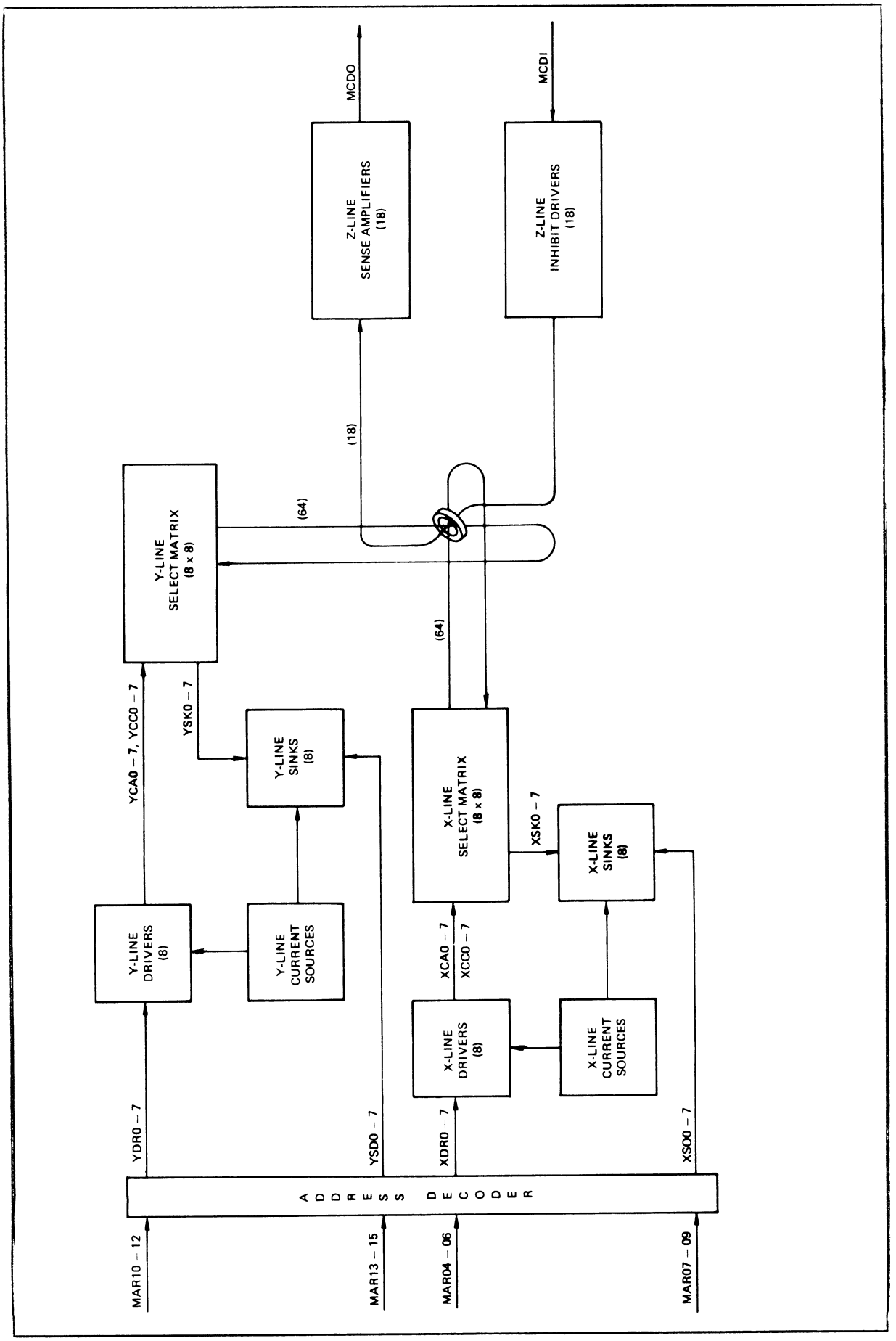


Figure 4-22. Core Memory Module Block Diagram

4-493. The need for changing the current direction within a line for read and write operations further complicates the circuitry of the line drivers and sink switches. This is shown in figure 4-24, a block diagram for a typical X-line driver, X-line, and X-line sink switch. Each line driver is actually two current drivers: a write driver for positive write current and a read driver for negative read current. All write drivers share a constant current source operating from +24 volts. Similarly, all read drivers share a constant current source operating into 0 volts.

4-494. Read and write drivers are coupled to their lines through current-steering diodes named for their common elements. For instance, eight diodes have their cathodes connected in common to the XDR0 read driver and their anodes connected to eight separate lines. Collectively, these diodes are known as XCC0 diodes (CC for common cathode). Those associated with the XDR1 read driver are named XCC1, etc. Likewise, the write drivers each have eight diodes whose cathodes are connected separately to eight different lines (the same lines as the write driver diodes) and the anodes connected in common to the write driver input. For the XDR0 write driver, these diodes are known as XCA0 diodes (CA for common anode). Those associated with the XDR1 write driver are named XCA1, etc.

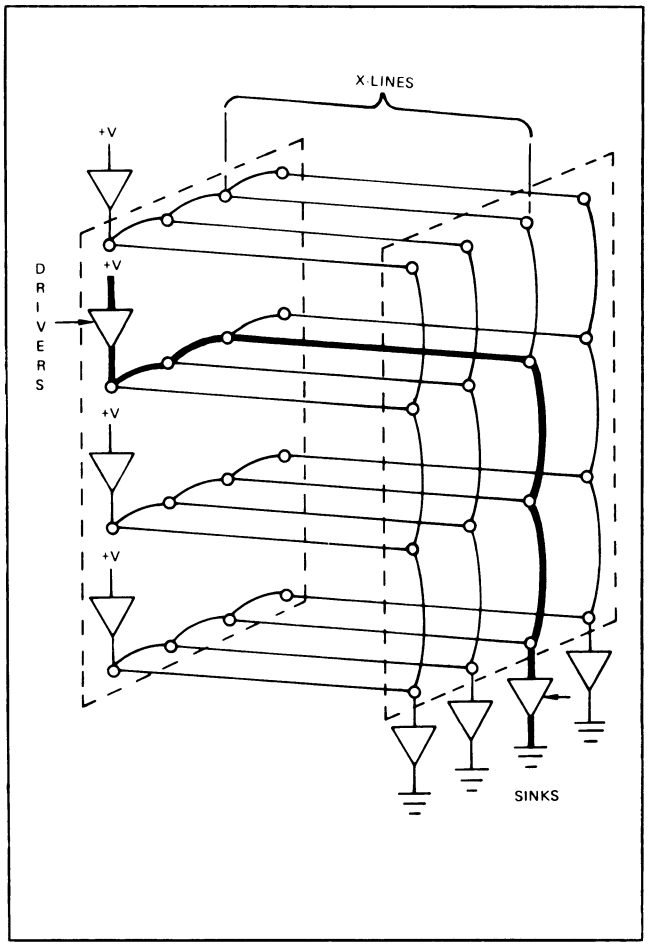


Figure 4-23. Address Line Selection

Table 4-3. X-Line Select Matrix

DRIVERS									
	XDR0	X0	X4	X8	X12	X16	X20	X24	X28
	XDR1	X1	X5	X9	X13	X17	X21	X25	X29
	XDR2	X2	X6	X10	X14	X18	X22	X26	X30
	XDR3	X3	X7	X11	X15	X19	X23	X27	X31
	XDR4	X60	X56	X52	X48	X44	X40	X36	X32
	XDR5	X61	X57	X53	X49	X45	X41	X37	X33
	XDR6	X62	X58	X54	X50	X46	X42	X38	X34
	XDR7	X63	X59	X55	X51	X47	X43	X39	X35
		XSO0	XSO1	XSO2	XSO3	XSO4	XSO5	XSO6	XSO7
		SINKS							

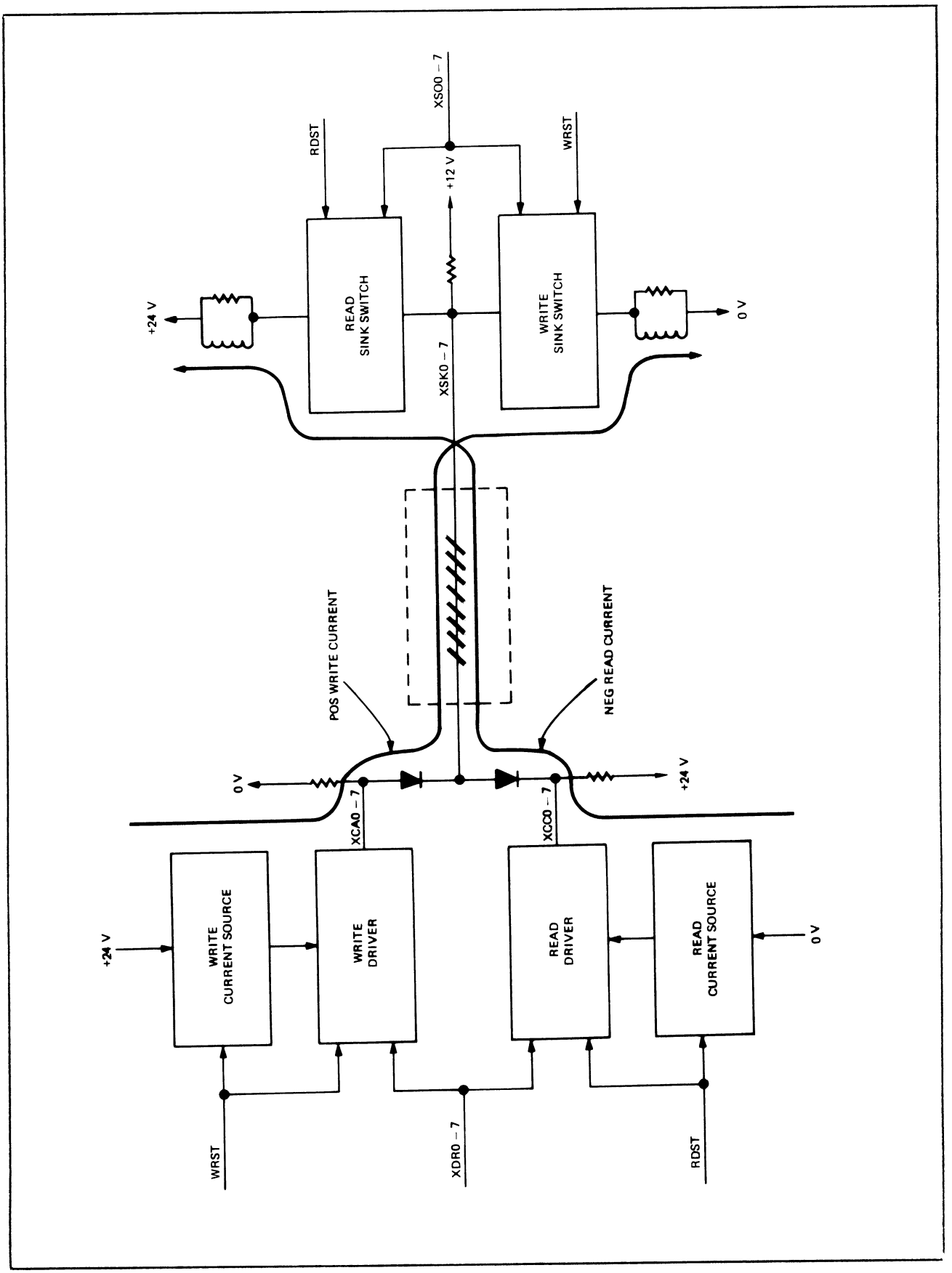


Figure 4-24. Read-Write Current Flow Diagram

4-495. Each sink switch is divided into two separate sections: one for read current returning to +24 volts and one for write current returning to 0 volts.

Note

To simplify the naming of circuits, a convention has been adopted here that write current is positive and read current is negative. As a consequence, it is permissible to speak of a 0-volt read current source and a +24-volt read current sink, which is done.

A given pair of read and write sink switches service eight lines. Each group of lines is named for the sink switches to which it connects. Lines XSK0 go to X-line sink switch pair XSO0, lines XSK1 go to X-line sink switch pair XS01, etc. A terminating resistor to 12 volts is connected to each set of lines.

4-496. To access a particular word location, the X-line for its intersection must be addressed. This is done by enabling one current driver (XDR0 through XDR7) and one sink switch (XSO0 through XSO7). Next, a timed read control signal (RDST true) activates the read current source, the enabled read driver, and the enabled read sink switch, causing negative read current to flow through the forward biased common-anode diode, through the addressed X-line and the read sink switch to the 24-volt supply. The current continues for the duration of the RDST signal, stabilized at a constant value by the read current source.

4-497. A timed write control signal (WRST) activates the write current source, the enabled write driver, and the enabled write sink switch, causing positive write current to flow through the forward biased common-cathode diode, through the addressed X-line, and through the write sink switch to the 0-volt return. Write current continues for the duration of the WRST signal, stablized at a constant value by the write current source. When neither signal RDST or WRST is active, both the common-anode and common-cathode diodes are back biased, decoupling the line from the current drivers and making current flow in the line impossible.

4-498. Memory Access Control Circuits

4-499. The circuits that control access to the memory module are shown in Drawing 394693, Sheet 1. A memory module cannot be activated unless its module addressing enable signal (MCFEN0- through MCFEN7-) and the read-write memory access signal (MCRW-) are both low. This causes their OR-gate (negative AND- gate) output to be low, enabling input gates for read, write, and inhibit timing signal gates.

4-500. To cause the memory module to perform read addressing and core switching, the module must be addressed, memory access must be enabled, and read timing signal MCFRET- must be low. A low level on the RDST line activates the X- and Y- read current sources (discussed in paragraph 4-503) and turns on transistor Q1 of the read current driver and sink control circuit. The positive pulse induced in the secondary of transformer T1 turns on transistor Q2 to provide a positive voltage to enable the selected X-read driver (XRSW), Y-read driver (YRSW), X-read sink (XRSK), and Y-read sink (YRSK). Notice that this positive voltage also forward biases diode CR1, and the +5 volts disables the gating for write timing control signal WRST. This is not an operational necessity, since MCFRET- and MCFWRT- signals usually cannot occur coincidentally. It does provide a contingency safety factor, however. After transistor Q2 is turned off, diode CR2 is forward biased and provides a 0-volt level to enable WRST gating.

4-501. Write addressing and core switching within the memory module requires that the module must be addressed, memory access must be enabled, the read timing signal must be absent, and write timing signal MCFWRT- must be low. If these conditions are met, signal WRST will be low, activating the X- and Y-write current sources (discussed in paragraph 4-512) and turning on transistor Q3 of the write current driver and sink control circuit. This circuit operates essentially in the same way as the one above it to enable the X- and Y-write drivers and sinks by applying 12 volts to them through resistors R15 through R18. Notice, however, that there is no lockout of the RDST gate when transistor Q4 is turned on.

4-502. Inhibit timing control signal MCFINT- is applied to the memory module through a negative AND-gate which transfers the signal only if the module has been addressed and memory access has been enabled (MCFENx- MCRW-). In such a case, a low MCFINT- signal will produce low outputs on the INHG1 and INHG2 output lines and activate the inhibit drivers (paragraph 4-530).

4-503. Current Source Circuits

4-504. Four similar circuits operate at constant current sources; two for negative read current and two for positive write current. Read current source circuits (Drawing 394693, Sheet 1) will be discussed first.

4-505. X- and Y-line read current sources are controlled by read timing signal RDST and provide negative current from a 0-volt supply at 380 milliamperes to the X- and Y-line read drivers. These circuits also perform the ancillary function of generating a sense amplifier strobe signal (SAST) that is critically timed to the rise of read currents in the magnetic array.

4-506. Consider the initial conditions that prevail when the read current sources are turned off. Read control signal RDST is high, causing its input gate to hold capacitor C6 in the discharged condition (0 volts at the junction capacitor C6 and resistor R28). This low state holds transistors Q6, Q10, and Q13 turned off. Because their collectors are high, transistors Q10 and Q13 will keep their respective regulator transistors turned off, and the X- and Y-line read drivers will see a non-current producing +24 volts through 100 ohms (IRDC lines). Also because transistor Q6 is turned off, sense amplifier strobe transistor Q132 will be turned off, strobe delay transistor Q8 will be turned on, and strobe pulse transistor Q9 will also be conducting. So in the quiescent state, signal lines SAST1 and SAST2 will be low.

4-507. Capacitor C6, transistor Q6, and resistor R30 form an integrator for constant current delivered by transistor Q7. When signal RDST goes low, the collector of its input gate is no longer grounded (open) and allows capacitor C6 to charge through transistor Q7. Because of the constant 6.3-volt emitter-to-base differential provided by reference diode CR4, the charging current will be linear. As soon as the charge reaches the base voltage of transistor Q6, the transistor conducts and prevents the voltage from building higher. The total rise time is approximately 100 nanoseconds from the time the circuit is first turned on until the current-governing threshold is reached. Transistor Q5, capacitor C5, and resistor R27 provide the reference threshold for transistor Q6. Sensistor R406 provides temperature compensation for rising emitter currents by reducing the threshold voltage as the temperature rises. It has a positive temperature coefficient.

4-508. The rising voltage at the base of transistor Q10 causes it to increase conduction linearly. Transistors Q11, Q12, and Q133 follow, allowing negative current to flow from the 0-volt supply to the +24-volt negative current sink through resistor R34 and balun transformer T23A. These three parallel current regulators are held conducting at a point where 380 milliamperes flow through the transformer and X-line connected to it. This half-current value is ultimately controlled by base bias components C5 and R27 for transistor Q6, as trimmed by resistor R415.

4-509. Balun transformers in each X- and Y-line current source circuit help to damp out switching overshoot and ringing in the driven lines by offering a transient sensitive load. The primary of this transformer (pins 13 and 14 of transformer T23A) is connected to the line on the driver side. Any change in current induces a change-bucking voltage in the secondary of the transformer, which is connected to the line at the sink end. Specifically, as seen on the schematic diagram, the X READ (IRDC) line goes to the read side of all X-line drivers and the XREAD SINK BUS line comes from the read side of all X-line sink switches.

4-510. The moment the read control ramp voltage reaches its maximum value and transistor Q6 conducts, the base of Q132 goes positive and the transistor is turned on. The negative-going collector voltage is differentiated by capacitor C10 and resistor R410, causing a momentary negative spike which turns off transistor Q8 during a brief delay

interval. When transistor Q8 is turned on again, the edge differentiated by capacitor C8 and resistor R32 turns off transistor Q9 momentarily. The 50-nanosecond wide positive pulse produced by transistor Q9 is distributed to the sense amplifiers as activating strobe signals by power drivers feeding lines SAST1 and SAST2.

4-511. The Y-line read current source, consisting of transistor Q13 controlling current regulators Q14, Q15, and Q134, also operates from the voltage developed across capacitor C6. Operation is identical with the X-line current source.

4-512. Write current source circuits (Drawing 394693, Sheet 2) are controlled by signal WRST and are activated by a low level to the WRST input. Transistor Q25, which is normally turned on, is switched off by this level and causes transistor Q21 to cease conducting also. With transistor Q21 cut off, a voltage is allowed to be integrated across capacitor C11 until it reaches a threshold level established at the base of transistor Q17 and the transistor conducts. Thereafter, the operation is much the same as that described for the read current sources. Transistor Q18 is the control amplifier for series current regulators Q19, Q20, and Q135. These feed positive current to the X-line write drivers through transformer T23C.

4-513. The Y-line write current source, consisting of transistor Q22 controlling series regulators Q23, Q24, and Q136, also operates from the voltage developed across capacitor C11. Operation is identical with the X-line current source.

4-514. Memory Protect Circuits

4-515. These circuits prevent memory access by inhibiting operation of the memory read and write current sources during power-on or power-off transitions. The controlling signal is PFRST from the power failsafe option. Normally, this input is an open line so that Schmitt trigger transistors Q26 and Q27 (Drawing 394693, Sheet 2) will be turned off and turned on, respectively. A 1.5-volt IR drop across forward biased diodes CR6 and CR7 provides the trigger level for the circuit. In this state, transistor Q28 will be conducting, and transistors Q29, Q30, and Q31 will be off.

4-516. To activate the memory protect circuits, the PFRST input line must be grounded. This is done through a relay closure, and since the base of transistor Q26 is now more negative than the 1.5-volt threshold at the base of transistor Q27, the circuit is triggered (Q26 on; Q27 off). As the base of transistor Q28 is no longer forward biased, the transistor is turned off, turning on transistors Q29, Q30, and Q31. With transistor Q30 conducting, point A is essentially at +24 volts. This prevents capacitor C11 from developing a charge (no differential between its two terminals) and disables both X- and Y-line write current sources. Similarly, the conduction of transistor Q31 applies essentially 0 volts to capacitor C6 (point B) so that it cannot develop an activating charge. This disables the X- and Y-line read current sources.

4-517. Address Decoder Circuits

4-518. Four binary-to-octonary (3-to-8 line) decoders convert the states of the 12 memory address bits MAR04 through MAR15 into four appropriate X- and Y-line source and sink select signals. These decoders (Drawing 394693, Sheet 1) operate with positive-true input logic levels, but negative-true output levels. Thus, if memory address bits MAR07 through MAR09, for example, are all zeros (0 volts on all three input lines), X-sink select signal XSO0 will be true (0 volts). And if all three bits are ones (+5 volts on all inputs), X-sink select signal XSO7 will be true (0 volts). It is important to notice that the activating condition for the source or sink circuit being selected is the low, or ground, condition. All other output lines will be high (+12 volts through collector load resistors). Table 4-4 is a positive-true truth table for the address decoder. Also observe in the truth table that the decoders "see" the input bits in reverse order of significance (LSB of group is seen as MSB, etc).

4-519. Drive Line Source and Sink Circuits

4-520. X-line source drive and sink circuits (Drawing 394693, Sheet 3) and Y-line source drive and sink circuits (Drawing 394693, Sheet 4) are identical to one another and consist of 64 switching transistors controlled by 16 current steering pulse transformers. X-line drivers and sinks will be

Table 4-4. Memory Address Decoder Truth Table

Inputs			Outputs							
C (LSB)	B (2SB)	A (MSB)	0	1	2	3	4	5	6	7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

discussed. However, the discussion applies equally well to the Y-line drivers and sinks.

4-521. Transistors Q48 through Q63 belong to the X-line driver circuits. They are grouped in pairs, one for read current and one for write current. A particular pair share a pulse transformer, which has a center-tapped primary and split secondaries that allow one transistor or the other to be pulsed into conduction. A pair is enabled by a low level on its addressing input (XDR0 through XDR7). This low level acts as a return for the +12-volt read and write activating signals XRSW and XWSW.

4-522. Consider a typical memory access operation during which X-line driver XDR7 is addressed. During the entire memory access operation, signal XDR7 will be low (0 volt) and the others will be high (+12 volts). To select the correct polarity for read current, signal XRSW goes high, and primary current flows through diode CR24 and the top half of transformer T6A. The pulse induced in the secondary causes transistor Q48 to be turned on, allowing positive current to flow from the X-read current source (IRDC) to common-cathode diode group 7 (XCC7) and through the line connected to the similarly activated X-read sink switch.

4-523. Read current is followed by write current for which the drive polarity must be reversed. This is done by signal XWSW going high and causing primary current to flow through diode CR25 and the lower half of transformer T6A. Transistor Q49 is turned on by the pulse induced in the secondary and allows negative current to flow from the X-write current source (IWRC) to common-anode diode group 7 (XCA7) and through the line connected to the similarly activated X-write sink switch.

4-524. The X-line sink switches are comprised of transistors Q32 through Q47. These, too, are grouped in pairs, one for read current and one for write current, and are controlled by center-tapped primary/split secondary pulse transformers identical to those used in the driver circuits. A given pair of sink switches is enabled by placing a low level on its addressing input (XSO0 through XSO7) and activated by making read polarity selecting signal XRSK or write polarity selecting signal XWSK high.

4-525. Consider an operation where sink switches XS07 are addressed. Signal XS07 will be low for the duration of the memory access, supplying a

ground return through the primary center tape of transformer T2A. The read current sink switch is activated by a high-level pulse on the XRSK line, which causes a current to flow through diode CR8 and the top half of the transformer. This turns on transistor Q32 and provides a path from the ends of eight X lines in group 7 (XS7) to the balun transformer secondary for the X-read sink bus, a +24-volt sink for negative current.

4-526. Signal XWSK goes high at the same time signal XWSW goes high, causing primary current to flow through diode CR9 and the lower half of transformer T2A. Transistor Q33 is turned on by the pulse induced by the action and allows the negative write current to flow from the X-line connected to the X-write current source to the balun transformer secondary for the X-write sink bus, a 0-volt sink for positive current. How the addressing of one source driver and one sink switch causes a particular line to be selected has been discussed in paragraph 4-490.

4-527. Z-Axis Data Lines

4-528. Incoming data to be written into memory is received as 18 parallel bits over input data lines MCDI00 through MDCI15, MCDIPL and MCDIPR. Data on these lines goes to 18 inhibit drivers. Similarly, outgoing data read from memory is sent as 18 parallel bits over data lines MCDO00 through MCDO15, MCDDOPL and MCDOPR. Data on these lines comes from 18 sense amplifiers. One inhibit driver, one data line, and one sense amplifier are associated with each bit position matrix of the core array. Figure 4-25 shows a typical example of the relationship of these three elements for data bit 0, in simplified form.

4-529. A single data line threads through all 4096 cores of any given bit position matrix. This line serves the dual purpose of collecting voltages induced by the switching of cores for input to the sense amplifier and also for routing inhibit current through the cores to prevent switching. Notice in the figure that the inhibit driver is connected to the center of the line (10) and delivers a positive current through both legs of the line to a pair of decoupling diodes at the sense amplifier ends of the line (S0 and $\overline{S0}$).

4-530. Inhibit Drive Circuits

4-531. All 18 inhibit drivers (Drawing 394693, Sheets 5 thru 10) are identical and consist of a negative-true AND input gate followed by a two stage current switch. Transistor stages Q96 and Q97 of the bit 00 inhibit driver are typical. Since it is desired to produce an inhibit current only if the data bit being written is a zero, transistor Q96 will be turned on only if the level on the MCDI00 line is low (a zero) and a low-level inhibit gate signal

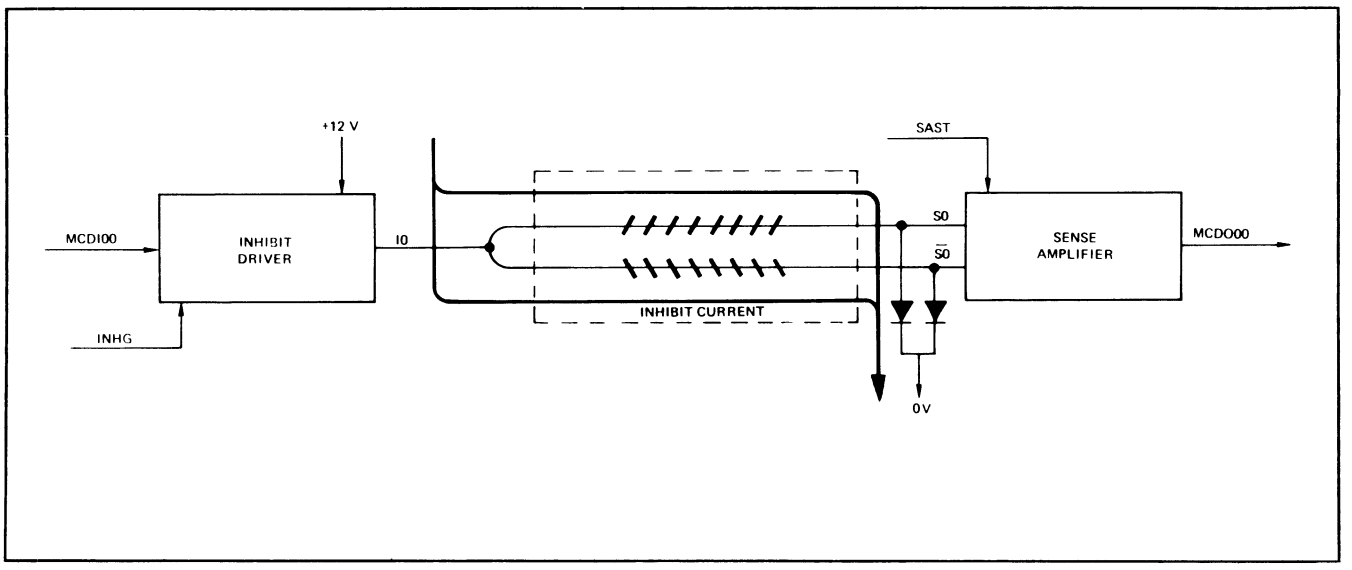


Figure 4-25. Data Line Current Flow Diagram

INHG1 is present. When switch Q96 is turned on, emitter follower Q97 is also turned on through coupling transformer T18A. Within 100 nanoseconds, 750 milliamperes of current flow through resistor R165, out through terminal I00 to terminals S00 and $\overline{S00}$ at the opposite ends of the line, through diodes CR72 and CR73 to the 0-volt return. Since the current splits, the bucking inhibit current is approximately 375 milliamperes in each leg; considerably less than the current required for switching.

4-532. Sense Amplifier Circuits

4-533. Dual differential comparator integrated circuits are used for the memory-read sense amplifiers. These detect sense line signals of core switching amplitude without regard for their polarity, since half of the cores on a sense line produce negative-going signals and half produce positive-going signals with respect to one end of the line. The sense amplifiers for all 18-bit sense lines are identical and all operate in the same way. Operation of the bit 00 sense amplifier connected to the S00 line (Dwg 394693, Sht 5) is typical.

4-534. An input voltage divider; consisting of resistors R156, R158, and R160, between +12 volts and ground; makes the pin 3 input of one differential amplifier approximately 20 millivolts more positive than its pin 4 input. Likewise, the pin 7 input of the second differential amplifier is 20 millivolts more positive than its pin 6 input because of another, similar divider. Both of these voltages represent a backward, or cutoff, bias to their respective amplifiers. If a voltage differential between the S00 and S00- inputs is induced which exceeds this 20-millivolt threshold, one or the other amplifier will detect it and turn on, since they work in opposition to one another. Normally, the common output of the amplifier pair will be 0 volts (open line to 1000-ohm load clamped negatively to ground) when the amplifiers are turned off. A sense amplifier strobe signal greater than +3 volts is required on the SAST1 line to enable output transfer. If one of the differential amplifiers is turned on at the time that the strobe pulse occurs, a positive pulse of approximately 50-nanosecond duration (width of the strobe) and approaching the logical-true level in amplitude will be seen at output MCDO00.

4-535. DIRECT MEMORY ACCESS OPTION

4-536. The direct memory access (DMA) option permits up to six external devices to communicate directly with the memory modules on a fixed priority basis without going through the data input-output (DIO) channels of the CPU. Consequently, direct memory accessing does not interfere with normal data processing unless both the CPU and the DMA option require memory access during the same machine cycle. All 704 Processors are wired to receive this option, which is contained on a single circuit card. Logic for generating memory parity check bits during memory write operations and for detecting memory parity errors during memory read operations may also be included on this card. Installation of the appropriate card is all that is required to implement either or both the six-level DMA and memory parity check functions.

4-537. The direct memory access logic on the DMA option card acts as a universal interface between DMA device controllers connected to the DMA bus and the CPU memory system. It consists of request and acknowledge registers for processing device controller requests for recognition, DMA priority and read-write control logic which translate requests into CPU compatible modes of operation, a DMA memory buffer register for storage of data words being transferred to and from the memory modules, memory address gates which couple memory location addresses from the device controllers to the CPU memory address register, and the independent memory parity check logic mentioned earlier. Figure 4-26 is a block diagram of the DMA option card, showing all of these functions, DMA data transfer paths, and the major control signals involved.

4-538. When the direct memory access function is installed and operational, CPU program execution and direct memory accessing proceed simultaneously until both require access to memory at the same time. At this point, the direct memory access logic is given precedence over the CPU logic, and

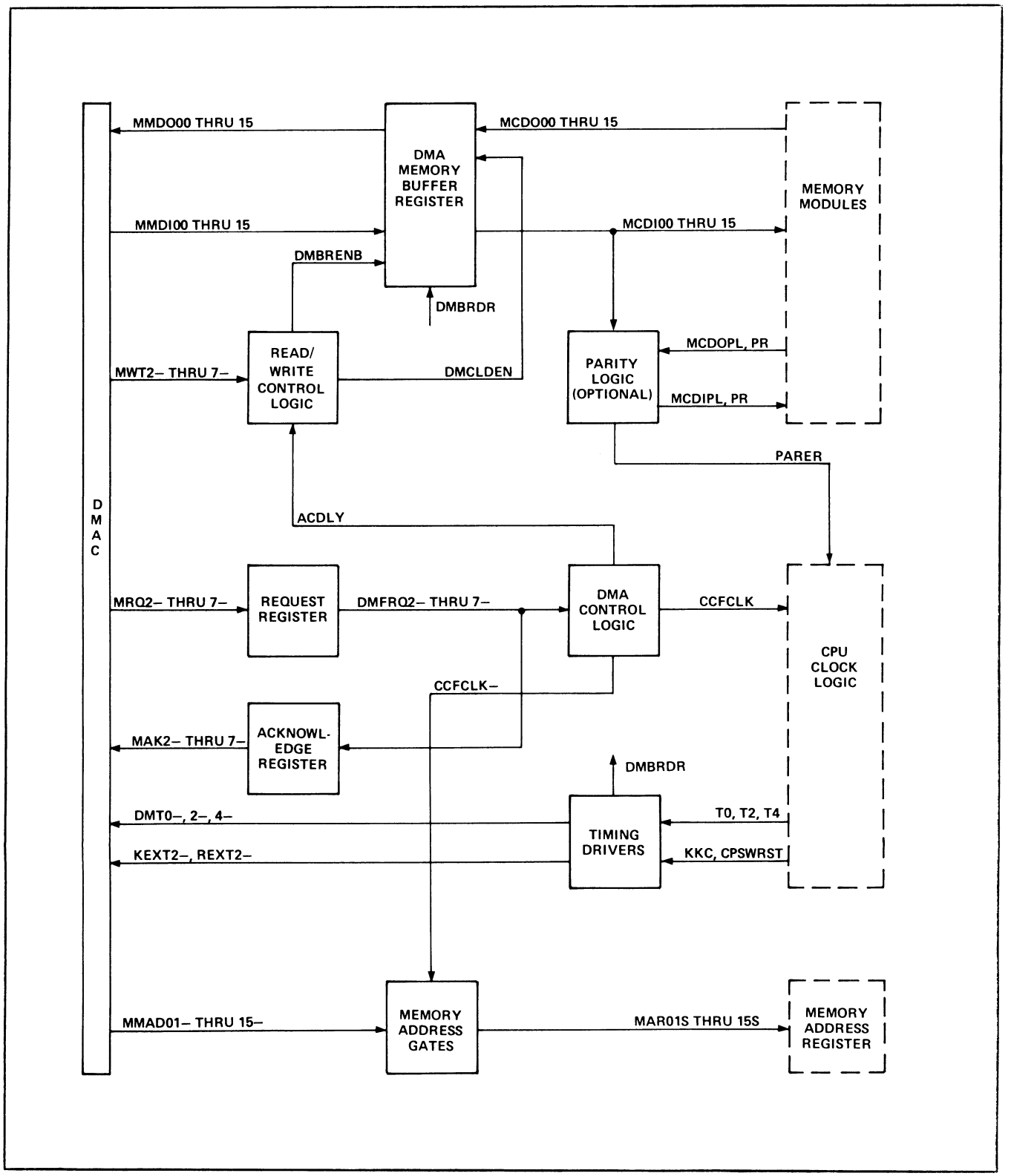


Figure 4-26. Direct Memory Access Option Block Diagram

program execution is suspended until a machine cycle is available for CPU access to memory. Simultaneous operation then resumes until both require concurrent access to memory again. Program execution is suspended by suppressing the distribution of clock pulses in the CPU. This subject is discussed in paragraph 4-23.

4-539. All signals except memory data transmitted to or from direct memory access device controllers are negative-true (logically inverted) signals. The "true" or "1" level is 0 V (low), and the "false" or "0" level is +3.0 (high). Direct memory access data input and output lines (MMDI00- through MMDI15- and MMDO00- through MMDO15-) transfer full 16-bit parallel words and communicate with the memory modules through the DMA memory buffer register. This register performs a function similar to that of the CPU memory buffer register. In fact, its data input and output lines to the memory modules (MCDI00 through MCDI15 and MCDO00 through MCDO15) are logically compatible with similar lines from the CPU memory buffer register and are connected in parallel (logically ORed) with those lines.

4-540. Memory location addresses for direct memory access must be supplied by the external device controllers and come in as normal, 15-bit parallel address words (MMAD01- through MMAD15-). These are transferred by the memory address gates to the inputs of the CPU memory address register (MAR01S through MAR15S) only during those machine cycles that direct memory access is active. Bits 01 through 03 address a memory module and set a corresponding module enable flip-flop at the beginning of the machine cycle. All bits of the address are loaded into the memory address register at the same time, so that bits 04 through 15 will be stored for location addressing within the module enabled during the entire machine cycle.

4-541. Operation of device controllers on the direct memory access bus is synchronized with operation of the CPU by external clock signal KEXT2- (a function of ungated clock signal KKC) and timing signals DMT0-, DMT2-, and DMT4- (functions of time periods T0, T2, and T4). External reset signal REXT2- (a function of system RESET switch signal CPSWRST or power failsafe reset signal PFRST-) is also supplied to the device controllers.

4-542. The devices on the direct memory access bus operate on a priority basis (all have priority over the CPU, which may be considered as operating at priority level 1). Priority levels 2 through 7 are assigned to the various device controllers through jumper connections made during installation, with each numbered level having priority over all lower-numbered levels under it. According to its priority level assignment, requests for direct memory access are made over one of six request lines (MRQ2- through MRQ7-) by a device controller and stored in the request register. If no higher level request has been received, an acknowledgement will be sent back to the device controller over the assigned level acknowledge line (MAD2- through MAK7-), and the direct memory access operation takes place in the next machine cycle. If no direct memory access requests are present, the memory may be accessed by the CPU during the next machine cycle.

4-543. During the direct memory access machine cycle, a read or write mode control signal must be supplied by the device controller over its assigned level read-write control line (MWT2- through MWT7-). If the signal is true (low), the DMA logic operates in the memory write mode.

4-544. In addition to the direct memory access signals described above, direct memory access device controllers communicate with the CPU via the DIO bus as well. It is over this bus that the controller receives function codes which control modes of operation, receives the initial (or starting) memory location address for direct memory access addressing, and transmits status reports under program control. The functional description and theory of operation for direct memory access device controllers are contained in separate manuals covering each controller.

4-545. Memory Access Control

4-546. The priority of devices connected to the direct memory access bus is determined by the memory priority control logic (Dwg 394577, Shts

4 — 6). This logic also gives all direct memory access requests priority over memory access by the CPU. The first 11 signals shown in DMA read and write timing diagrams (figures 4-27 and 4-28) are the same and represent the preliminary operations that capture the memory system for direct memory access.

4-547. The states of the six direct memory access request lines (MRQ2- through MRQ7-) will be false (high) unless an active request is being made. Each line is monitored by a separate type-D flip-flop (DMFRQ2 through DMFRQ7) with inverted outputs ($\overline{Q}$ used as the set output), so that the D-input operates as a $\overline{D}$-input. These request storage flip-flops are clocked by signal KKRQ, a negative-going clock derived from ungated clock pulse signal KKC during each T2 time period.

4-548. At the end of each time period T2, when the positive-going edge of clock signal KKRQ occurs, those flip-flops whose inputs are true (low), indicating direct memory access requests at the active priority levels, will be set. Unless the request is still present when the next clock pulse occurs at the end of the following T2 time period, the flip-flop will be reset. Normally, the DMA device controllers are designed to hold the request on the line until they have been acknowledged and serviced.

4-549. Six acknowledge register flip-flops (DMFACK2 through DMFACK7) monitor request register outputs in such a manner that only one can be set at a time. Their input gates perform the function of determining the highest level priority of all requests during any given machine cycle. For example, if DMFRQ7 is true, acknowledge flip-flop DMFACK7 will be set when the KKACKA clock occurs at the end of T3. Acknowledge flip-flop DMFACK6 can only be set if DMFRQ7- DMFRQ6 is true, flip-flop DMFACK5 can only be set if DMFRQ7- DMFRQ6- DMFRQ5 is true, and so on down the line.

4-550. Acknowledge register clock signals KKACKA and KKACKB are identical, negative-going clocks derived from ungated clock pulse signal, KKC, during each time period T3. The positive-going clocking edge occurs at the end of that time period, setting the acknowledge flip-flop for the highest priority request stored in the request register. An inverting driver (MAK2- through MAK7-) on the output of each acknowledge flip-flop provides the true (low) signal back to the device controller which indicates that the request has been acknowledged. Normally, DMA device controllers are designed to "turn off" their request signal when the acknowledge signal is received. However, they must do so no later than time period T2 of the next cycle. The acknowledge flip-flop set at the end of time period T3 of one cycle will be reset at the end of time period T3 of the following cycle, making the MAK signal false (high) once again, provided that the request signal is no longer present.

4-551. At the same time that the highest level priority requesting acknowledge flip-flop is set, clock control flip-flop CCFCLK is reset (CCFCLK- true). Its D-input gates detect the no-request condition (DMFRQ2- through DMFRQ7- false) and will keep the flip-flop set, as long as a request has not been received. The CCFCLK output is an enabling signal for many CPU functions, including the distribution of gated clock pulses, triggering of the manual control sync flip-flops, resetting of the memory buffer register, and CPU loading of the memory address register. All of these functions are disabled when signal CCFCLK is false, denying memory access to the CPU until the signal returns to the true state.

4-552. An acknowledge delay flip-flop, ACDLY, monitors the reset output CCFCLK- of the clock control flip-flop. Since it is triggered by the positive-going edge of inverted KKC ungated clock pulses (KKCA), it will be set one time period later, at the start of time period T0, than the resetting of the CCFCLK flip-flop. It remains set for one full machine cycle, and its output delineates the time during which the direct memory access read or write operation will take place.

4-553. During the direct memory access machine cycle that flip-flop ACDLY is set, the false state of output ACDLY- disables CPU memory buffer register control signals MBLDMCLB and MBLDMCRB, preventing the contents of that register from being changed by memory data read

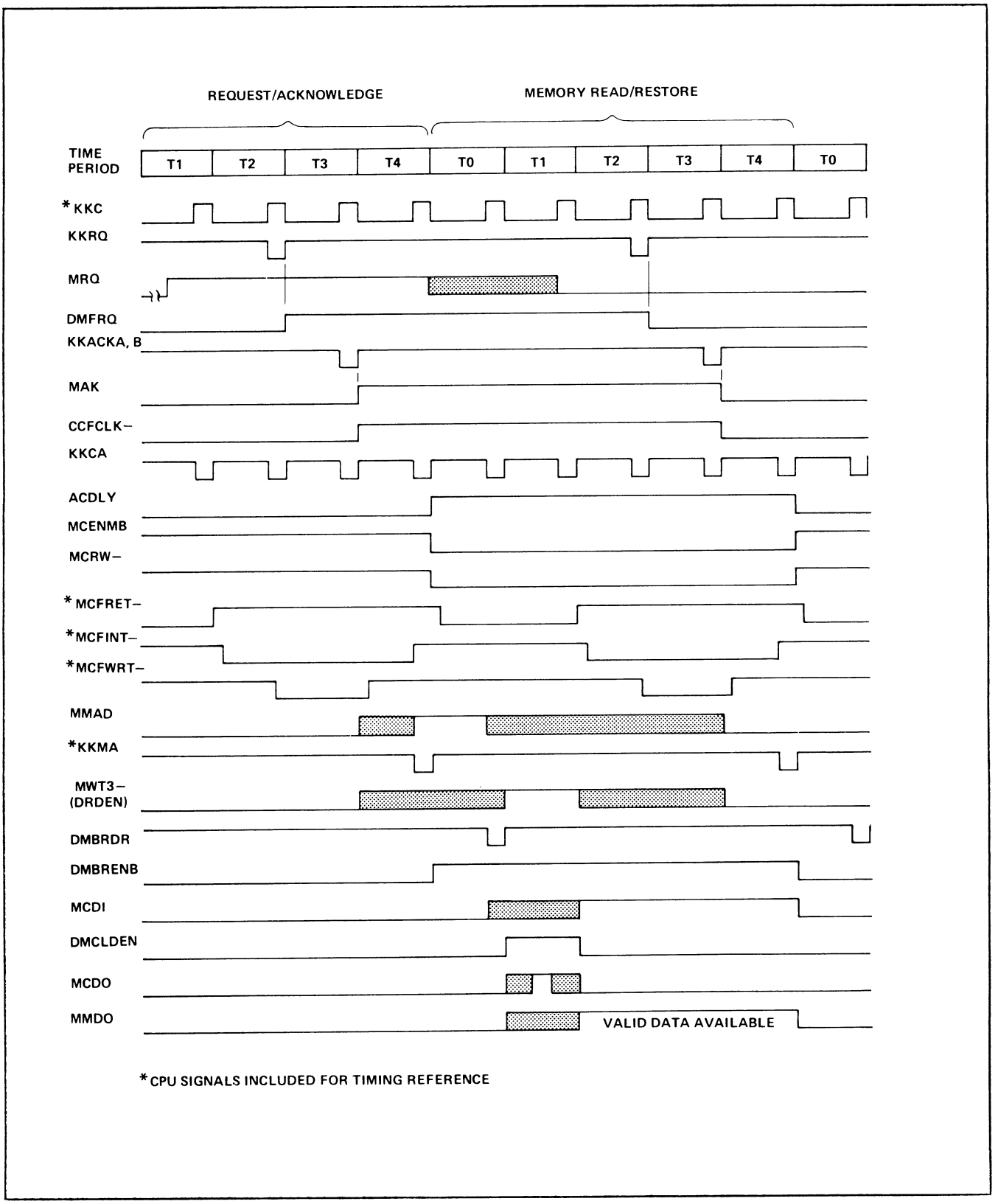
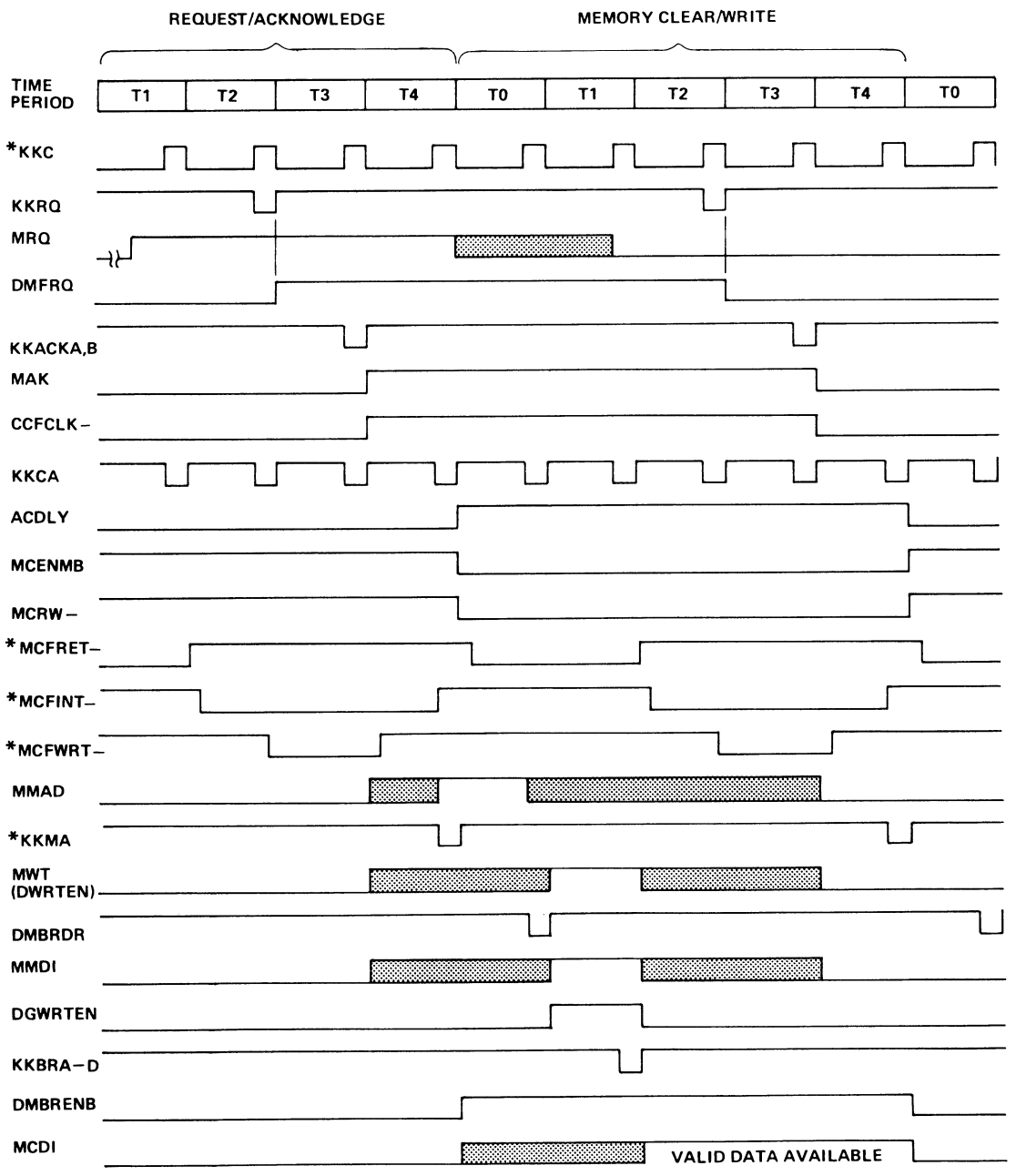


Figure 4-27. DMA Read Timing Diagram



* CPU SIGNALS INCLUDED FOR TIMING REFERENCE.

Figure 4-28. DMA Write Timing Diagram

during the direct memory access. Signal MCENMB is also false during DMA machine cycles, forcing the CPU memory buffer register output gates to the memory modules (MCDI00 through MDCI15) to produce an all 1's output. This is necessary because the DMA memory buffer register outputs to the memory modules are connected to the same lines, and functional OR gating of ground levels will occur otherwise. Finally, the setting of ACDLY makes MCRW- false to enable the memory modules for access.

Direct Memory Address Gates

4-555. Fifteen direct memory address gates (MAR01S through MAR15S) handle the memory location address word to be used for the DMA read or write operation. Signal DMADEN enables these gates during the time that the CPU gated clocks are inhibited (CCFCLK- true). The acknowledged DMA device controller must supply the memory address in logically inverted form over lines MMAD01- through MMAD15-. Normally, the supplying of a memory location address is made a function of the presence of the enabling MAK signal, so that the address will be present at the inputs of the address gates from the beginning of T4 of the request-acknowledge memory cycle to the beginning of T4 of the memory access machine cycle. In any event, it must be available somewhat before the end of time period T4 preceding memory access and removed prior to the end of time period T4 of the following machine cycle.

4-556. During all memory access operations, the memory modules receive memory location addresses from the memory enable flip-flops and from the memory address register in the CPU. Consequently, the outputs of the DMA address gates are connected in parallel with the other set inputs of the memory address register and clocked into the register by KKMA clocks at the end of time period T4 in a normal manner (paragraph 4-395). Since all other memory address register input sources are inhibited during the time period preceding direct memory access, the memory address register will copy the outputs of these gates. Likewise, these gates must be disabled one time period (T4) following direct memory access so that any memory address required during the next machine cycle, when CPU data processing resumes, can be loaded into the memory address register correctly. Since the DMA memory location address is stored in the CPU memory address register for the full direct memory access machine cycle, it can be removed by the device controller from the MMAD lines any time after the beginning of time period T0.

4-557. Direct Memory Buffer Register

4-558. The direct memory access buffer register (Dwg 394577, Shts 8 — 11) consists of 16 type-D flip-flops (DMBR00 through DMBR15) whose D-inputs are made to respond as $\overline{D}$-inputs by using the $\overline{Q}$-output as the set output. Data received from the memory modules (MCDO00- through MCDO15-) is loaded through direct set inputs under the control of enabling signal DMCLDEN. Data received from the device controller (MMDI00- through MMDI15-) is applied through the D-inputs, clocked by identical signals KKBRA,B,C, and D.

4-559. As in CPU memory accessing, a DMA read operation consists of sequential read-restore phases, and a DMA write operation consists of sequential clear-write phases. Both phases of an operation are executed in one machine cycle. Execution of a read or write operation primarily affects how data is loaded into the memory buffer register, whether data loaded during the first half of the memory access machine cycle comes from the memory modules (read operation) or from the device controller data input lines (write operation).

4-560. To execute a DMA read operation, the acknowledged device controller supplies a false level (high) on its assigned MWT- line, along with the memory location address to be read. All six MWT- lines are monitored by a large, negative-true NOR-gate (Dwg 394577, Sht 7). Since all inputs are high, signal DRDEN will be true. This, and all other signals associated with the DMA read operation are shown as the last seven entries in the read timing diagram, figure 4-27.

4-561. Signal DMBRDR goes to ground unconditionally at the end of each T0 time period, directly resetting all flip-flops of the DMA memory buffer register at the start of each machine cycle. Signal

DMBRENB is a function of the set state of the ACDLY flip-flop and will be true during the entire memory read-restore cycle. It enables the DMA memory buffer register output gates which supply data to the MCDI memory module data input lines.

4-562. With signals ACDLY and DRDEN true, signal DMCLDEN goes true during time period T1, enabling the direct-set input NAND gates of the DMA memory buffer register which load readout data from the MCDO memory module data output lines. This data is seen in the form of positive-going pulses of approximately 50-ns duration for all 1's in the data word, which can occur at any time during the last 100 ns of the time period. Once loaded, the DMA memory buffer register supplies valid readout data on its MMDO data output lines after time period T1. This data must be stored by the device controller prior to the next T0 time period, when the DMA memory buffer register will be reset by signal DMBRDR. The content of the register are written back into the same memory location during time period T3, as a normal restore operation.

4-563. To execute a DMA write operation, the acknowledged device controller supplies a true level (low) on its assigned MWT- line, along with the memory location address and the data to be stored. Since one input to the negative-true NOR gate is low, signal DWRTEN will be true. This, and all other signals associated with the DMA write operation are shown as the last seven entries in the write timing diagram, figure 4-28.

4-564. The DMA memory buffer register is directly reset at the end of time period T0 by signal DMBRDR, and its MCDI output gates are enabled by signal DMBRENB, as before. In device controllers of standard design, the gating of write word data is normally made a function of the MAK acknowledge signal being present. That is, data will be available for loading into the DMA memory buffer register from the preceding T4 time period to the following T3 time period. In any event, it must be present during time period T1 of the memory clear-write machine cycle.

4-565. With signals ACDLY and DWRTEN true, signal DGWRTEN is true during time period T1. The DGWRTEN signal enables the DMA memory buffer register clock gates KKBRA,B,C, and D, and the trailing edge of the next KKC clock pulse loads the register through its D-inputs with the data word supplied by the device controller on the MMDI data input lines. The content of the register is written into the addressed memory location during time period T3, as a normal write operation.

4-566. MEMORY PARITY CHECK OPTION

4-567. The memory parity check logic (Dwg 394577, Shts 13, 14) is associated physically with DMA logic, but performs the entirely separate function of generating odd-parity check bits stored during memory write operations and checking for parity error during memory read operations. The parity check system of the 704 Processor is byte oriented; that is, a separate odd parity check bit is provided for each byte of a data word. All words in memory are treated as two 8-bit bytes with their own parity check bit, requiring the use of memory modules with 18-bit word storage capability.

4-568. Figure 4-29 is a block diagram of the memory parity logic, showing the primary interconnections between its various functions. The logic contains an 8-bit Exclusive NOR parity tree for each memory data byte output, a parity bit storage register for each memory byte parity bit, a parity error detector, read-write control logic, and a pair of byte parity bit input gates.

4-569. The left-byte parity tree monitors memory data input lines MCDI00 through MCDI07 continuously, and the right-byte parity tree does the same for lines MCDI08 through MCDI15. The nature of the parity tree is such that the output at the apex (MCDIPL1 for the left-byte tree and MCDIPR1 for the right-byte tree) will be a 1 if the number of 1's at the input is even and 0 if the number of 1's at the input is odd. Each output is then compared with its respective parity check bit (stored as LBP for left byte and as RBP for right byte) by a final Exclusive NOR gate error detector. When the parity of a byte is even, its check bit should be a 1, and the output of the comparator will be true. Likewise, if byte parity is odd, its check bit should be a 0, and the output of the comparator will be true. Any time comparator

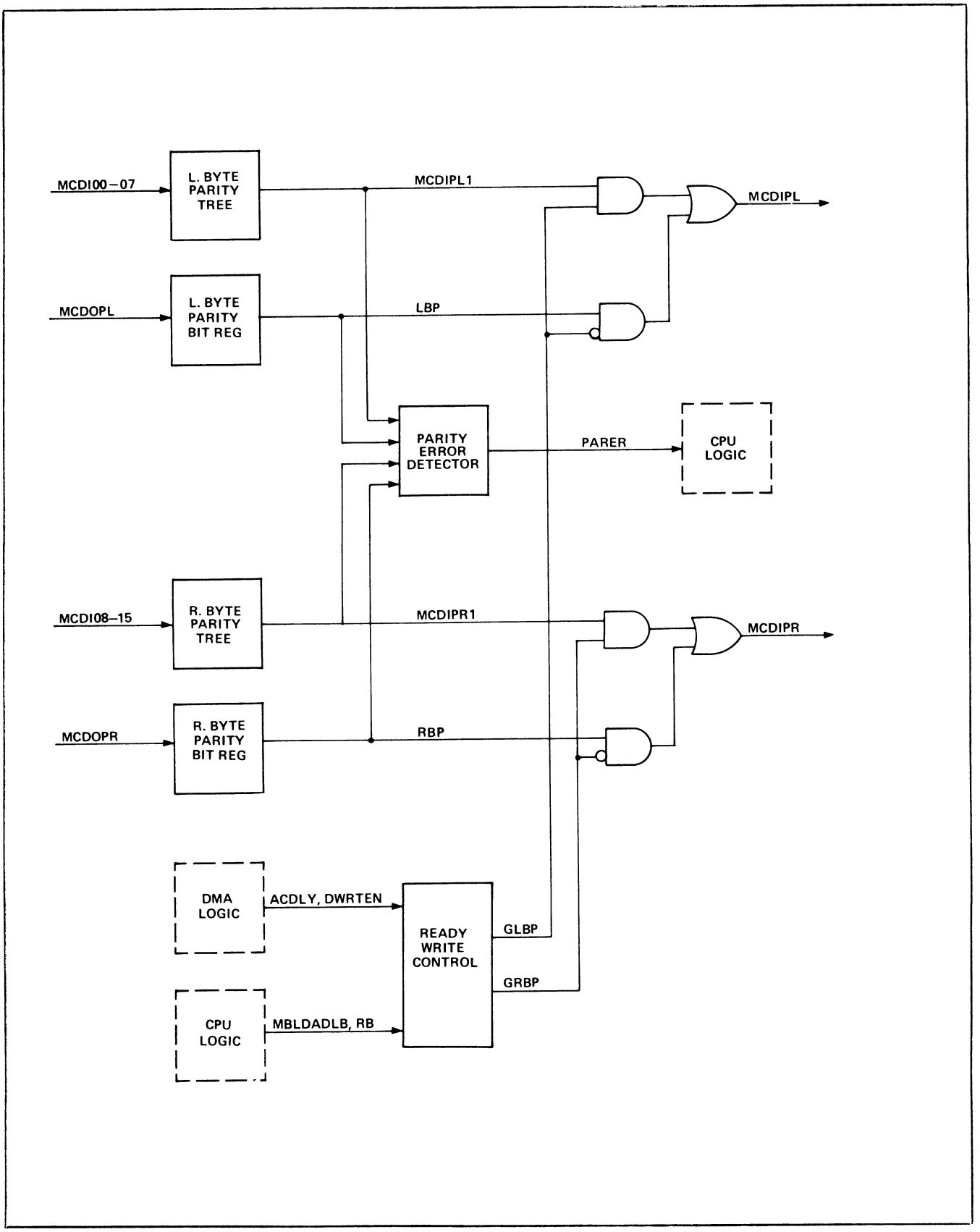


Figure 4-29. Memory Parity Logic Block Diagram

output LBPE- or RBPE- is false, a parity error is indicated. This indication is not always valid, and it is only sampled during those times and conditions when it is valid. This will be discussed shortly in connection with the sequence of events which occur during memory read and write operations.

4-570. Byte parity bit storage flip-flops LBP and RBP are reset during time period T0 of each machine cycle by the low level of signal DT0-. Their direct set inputs are enabled during every T1 time period by signal TIRC1, and the flip-flops copy the states of the parity bits presented on the MCDOPL and MCDOPR lines caused by reading or clearing a memory storage location. Any one pulse on a line will set the corresponding flip-flop, and the flip-flop will remain set until the start of the next T0 time period.

4-571. Read-write gate control flip-flops GLBP (for left byte) and GRBP (for right byte) are type-D flip-flops clocked by the positive-going edge of signal GPK, which occurs at the end of time period T1. Both flip-flops will be set if a DMA write operation is being performed (ACDLY DWRTEN), a CPU full-word store-into-memory operation is being performed (ACDLY-MBLDADLB MBLDADRB), or data is being manually entered into the memory (MCWRENT-). Notice that when an STB instruction is executed, only the flip-flop corresponding to the new byte being written into memory will be set (ACDLY-MBLDADLB + ACDLY MBLDADRB). Under all other circumstances, both flip-flops will remain reset, indicating that either a non-memory access cycle (which can be ignored) or a full-word read operation has taken place.

4-572. The output states of the GLBP and GRBP flip-flops control the output gating of byte parity check bits to the MCDIPL and MCDIPR lines to the memory modules. The states of the parity check bits on these lines are written with the data word into memory during time period T3 of the memory access cycle. Since the write phase of all memory read operations is a restore function, the contents of flip-flops LBP and RBP are gated by signals GLBP- and GRBP- onto the parity check bit input lines. Memory write operations, on the other hand, require the generation of a parity check bit for new data held by the active memory buffer register and available on the MCDI lines. Parity tree output signals MCDIPL1 and MCDIPR1, being 0's when the parity of their inputs is odd and 1's when the parity of their inputs is even, provide the necessary state of the parity check bits needed to maintain odd parity and are therefore gated onto the lines by signals GLBP and GRBP.

4-573. The execution of STB instructions represents a unique "mixed" condition, where the unaffected data byte is read from memory and loaded into the CPU memory buffer register, and the new data byte to be stored is loaded from the accumulator into the same register. In this case, the parity check bit for the byte read from memory will be gated from the appropriate parity bit register (LBP or RBP), and the parity check bit for the new data byte will be gated from the appropriate parity tree (MCDIPL1 or MCDIPR1).

4-574. Only at the end of time period T2 of a full-word memory read cycle is memory word parity checked for errors. Parity error flip-flop PARER is normally in the reset state. However, if at the end of time period T2 of a full-word memory read cycle (MCRW GLBP- GRBP- TIRC2) a parity error has been detected by either of the comparators (LBPE + RBPE), the flip-flop will be set. This causes the CCFRUN flip-flop in the CPU to be directly reset, which in turn causes the sequence counter to return to the halt phase after executing the current instruction. It also inhibits the gating of priority interrupt data input and data output strobes DISB and DOSB, generally disabling the DIO system. Once the CPU has halted, SELECTED DISPLAY indicator light 13 lights, indicating the detection of a memory parity error (provided the DISPLAY SELECTOR switch is in the MS position).

4-575. The PARER flip-flop can be reset by pressing the RESET switch (MRESET-). The flip-flop is also reset by the same conditions that cause the sequence counter to advance from the halt phase to the fetch phase (SCDC0 SCDC1F0 CCFSYN1). These include pressing the RUN switch, the SINGLE STEP switch, or the SINGLE COMMAND switch.

4-576. PRIORITY INTERRUPT SYSTEM

4-577. The priority interrupt system may contain one, eight, or sixteen interrupt levels. The levels are numbered 00 through 15, with level 00 assigned lowest priority, and the highest-numbered level installed in the system having the highest priority. The basic 704 Processor contains the logic for priority level 00 on the Adder Flip-Flop card. It may be expanded to an eight-level system by installing one Priority Interrupt card, which contains the logic for priority levels 01 through 07, into a prewired connector. Expansion to the full 16-level configuration requires installation and wiring of a connector for a second Priority Interrupt card in parallel with the first.

4-578. The interrupt system logic shown in drawing 394582 is for an eight-level system configuration (logic on Adder Flip-Flop card plus logic on one Priority Interrupt card). When the system is configured with only one level of interrupt, Priority Interrupt card logic is not applicable. When the Priority Interrupt card logic is duplicated for 16 levels of interrupt, inputs and outputs of like name are connected in parallel, and others are connected to appropriate signal sources or destinations outside of the interrupt system. Such wiring is shown on the diagrams by means of footnotes. The discussion that follows covers the sixteen-level system. Operation of systems with less than sixteen levels is the same except for obvious differences in encoding and decoding levels and priority logic and is not discussed. Figure 4-30 is a block diagram of a priority interrupt system of n levels, where n is the highest level of the system.

4-579. Interrupt Inputs

4-580. Interrupt signals (INTRPT00-, etc) are received from devices on the data input output bus and the direct memory access bus. These signals are received as negative-true signals and are inverted in the interrupt system logic. If the power fail-safe option is installed in the computer, a power interrupt signal (PWRINT-) is also received from the unit via the dc power supply.

4-581. The teletypewriter set controller is normally assigned to interrupt level 00, and the power interrupt is connected to the highest-priority level available to the system. The power interrupt must be the only device on the highest priority level to ensure that it is serviced without delay before power shuts down.

4-582. Other devices on the data input-output bus and direct memory access bus are assigned to intermediate interrupt levels. These assignments are fixed at the time that the system is wired; no provision is made for patching inputs onto different levels. (The priorities assigned to the devices may be changed by changing the wiring in the device controllers, when desired.)

4-583. The interrupt inputs are only enabled during time period T0 of each machine cycle. This requires that the interrupt signals from the devices remain true (low) for at least 1.0 μs to ensure that they will be present during a T0 time period.

4-584. Interrupt Levels

4-585. The logic for each interrupt level contains two flip-flops: an "enable" flip-flop and an "active" flip-flop. The four possible states of these two flip-flops define four conditions for interrupt servicing, as follows:

ENABLE F/F	ACTIVE F/F	CONDITION
0	0	Disabled
1	0	Idle
1	1	Waiting
0	1	Active

4-586. When a level is in the disabled condition, interrupts from devices assigned to the level are not accepted or stored. The system in no way recognizes interrupts at disabled levels but will recognize all other interrupts at idle levels. To enable a priority interrupt level so that it can service interrupts, it must be transferred from the disabled condition to the idle state. When in the idle state, the level will receive an interrupt if it is not currently in the process of handling one.

4-587. An interrupt on a level that is in the idle condition places the level in the waiting condition until the interrupt is serviced. The outputs from

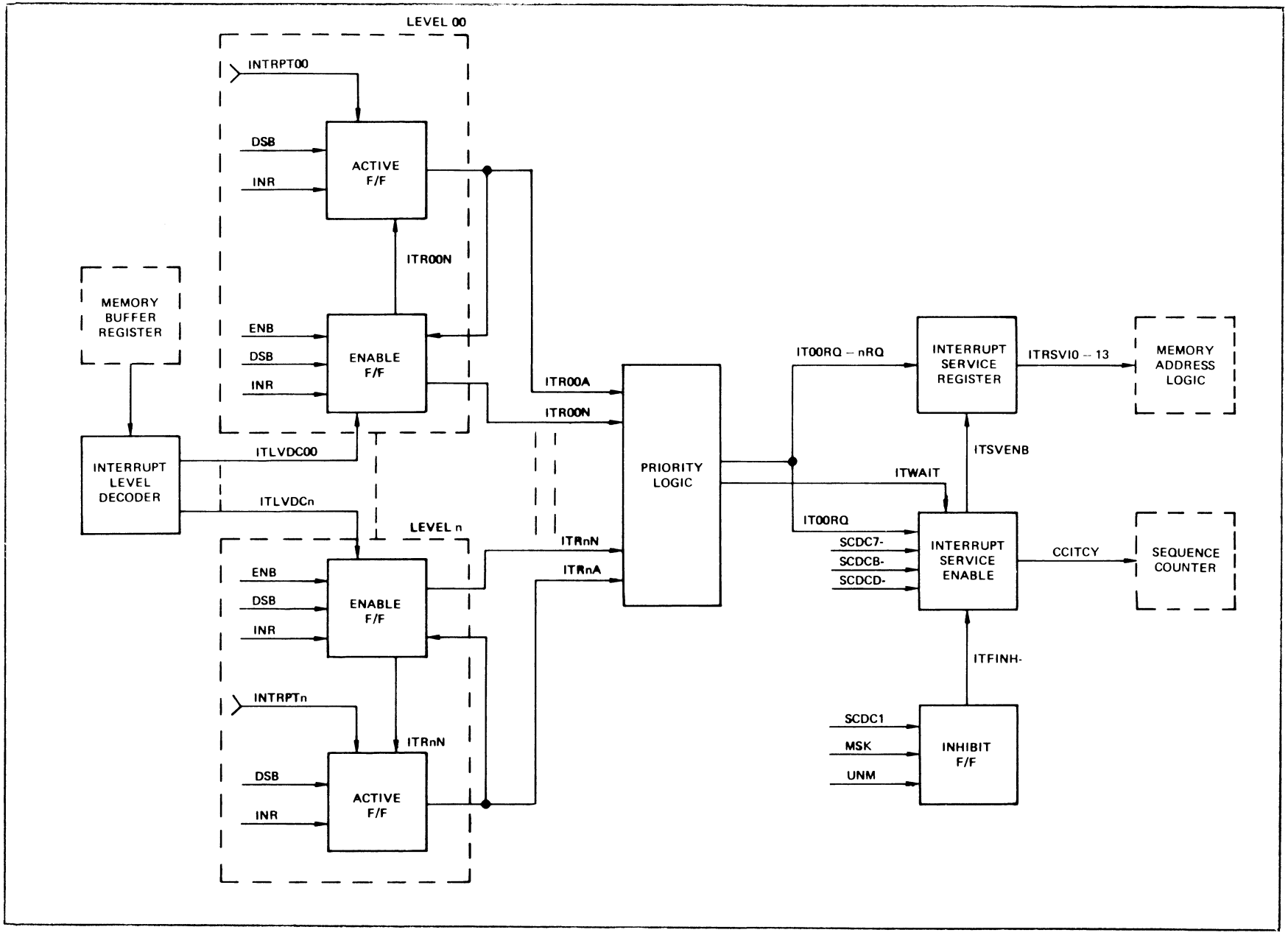


Figure 4-30. Priority Interrupt System Block Diagram

both the enable and active flip-flops of levels in the waiting state are true, and the priority logic generates an interrupt request signal appropriate to the highest level in the waiting state. When an interrupt is serviced, its level is placed into the active condition, and no other interrupts can be accepted on that level until the level returns to the idle condition at the conclusion of the interrupt service routine.

4-588. Program Control

4-589. Five program instructions control operations within the priority interrupt system. DSB and ENB instructions are used to disable or enable an individual level by transferring it from the idle to the disabled condition or the reverse under program control. An INR instruction is used to return individual levels from the active to the idle condition at the conclusion of an interrupt service routine. MSK and UNM instructions permit the entire priority interrupt system to be disabled (masked) or enabled (unmasked) from servicing further interrupts.

4-590. In interrupt-level oriented instructions DSB, ENB, and INR, the F2 field always specifies the interrupt level to be affected by the instruction. Bits 12 through 15 of the instruction word (MBR12 through MBR15) are decoded by an interrupt level decoder in the interrupt system logic to obtain a single, affective interrupt level decode signal (ITLVDC00, etc). This signal is used to gate control signals generated by the instruction being executed into the inputs of the enable and active flip-flops for the level specified by the instruction.

4-591. The DSB instruction resets both the enable flip-flop (ITR00N, etc) and the active flip-flop (ITR00A, etc) for the level addressed by its F2 field. Signal ITDSB (Dwg 394567, Sht 9) becomes true during time period T4 of the DSB instruction fetch phase (T4SCDC1 INDC003) and is applied to the flip-flops for all levels. The active interrupt level decode signal gates signal ITDSB into the reset inputs of both flip-flops for a particular level, and the flip-flops are reset at the end of time period T4. Resetting of an enable flip-flop prevents its corresponding active flip-flop from being set by an interrupt on that level.

4-592. The ENB instruction sets the enable flip-flop for the level addressed by its F2 field. Signal ITENB (Dwg 394567, Sht 9) becomes true during time period T4 of the ENB instruction fetch phase (T4SCDC1 INDC002) and is applied to the enable flip-flops for all levels. The active interrupt level decode signal gates signal ITENB into the set input of the enable flip-flop for a particular level, and the flip-flop is set at the end of time period T4, but only if the corresponding active flip-flop is reset. Since the active flip-flop is reset, setting the enable flip-flop places the level into the idle condition.

4-593. The INR instruction is placed at the end of each interrupt service routine, and its execution causes, among other things, the level to return from the active state to the idle state. This is done by setting the enable flip-flop and resetting the active flip-flop for the level addressed by the F2 field of the instruction. Other functions performed by the instruction during an interrupt return cycle are discussed in paragraph 4-605. Signal ITIDL becomes true during time period T4 of the INR instruction fetch phase (T4SCDC1 INDC001) and is applied to all levels. The active interrupt level decode signal gates signal ITIDL into the set input of the enable flip-flop and the reset input of the active flip-flop for a particular flip-flop, but only if the level is in the active state (ITR00N- ITR00A, etc). The flip-flops are set and reset, respectively, at the end of time period T4, placing the level in the idle condition.

4-594. Mask and unmask instructions MSK and UNM control the inhibit flip-flop ITFINH (Dwg 394567, Sht 9). When this flip-flop is set, signal ITFINH- is false and disables the servicing of interrupts on all levels of the system by disabling interrupt output signal CCITCY to the sequence counter logic. It has no effect on the reception and storage of interrupts on individual levels. The MSK instruction enables flip-flop ITFINH to be set at the end of its fetch phase time period T3 (INDC00A SCDC1 KKITF). The UNM instruction enables the flip-flop to be reset at the end of its fetch phase time period T3 (INDC00B SCDC1

KKITF). Any interrupts received while the interrupt system is inhibited will be serviced in the order of their priority after the UNM instruction is executed to re-enable the system.

4-595. Power failsafe interrupts must always be serviced immediately, regardless of whether the interrupt system is masked or not. If flip-flop ITFINH is set when power failure is detected, signal PFSINT- will unconditionally cause it to be reset at the end of time period T3 of the current machine cycle. Input ITFINHR2- to the ITFINH flip-flop reset gate is for a similar use by future logic options.

4-596. When the CPU power is turned on, signal CPSWRST- directly resets all flip-flops in the priority interrupt system except flip-flop ITFINH. This disables all of the priority interrupt levels and clears the interrupt service register. Flip-flop ITFINH is directly reset by MRESET-, which occurs during the next time period T4. The same action also takes place when the system RESET switch on the CPU control panel is pressed. After power is turned on or the RESET switch is pressed, separate ENB instructions must be executed to enable the desired interrupt levels.

4-597. Interrupt Processing

4-598. An interrupt signal consists of a low (true) level on one of the negative-true DIO bus interrupt lines (INTRPT00-, etc). These are gated to the set side of all active flip-flops whose corresponding enable flip-flop has been set. This occurs during each time period T0 (INTRPT00 INTR00N T0). This clock period is used because it allows maximum time to set up the interrupt service register and prepare the memory address register for forced addressing prior to the start of the next machine cycle.

4-599. The priority logic generates an interrupt request signal (IT00RQ-, etc) corresponding to the highest level for which both flip-flops are set (waiting condition). The active flip-flop for that level, being set, prevents the generation of interrupt requests on lower priority levels until the interrupt has been serviced and has returned to the idle condition. Signal ITWAIT- is false whenever any interrupt request signal higher than signal IT00RQ- is waiting for service, and enables signal ITSVENB.

4-600. The servicing of interrupts is enabled (but not necessarily accomplished) by signal ITSVENB (Dwg 394567, Sht 9) whenever any interrupt level is waiting for service (ITWAIT- or ITR00RQ- is false) and the CPU is not already in an interrupt service cycle (SCDC7- SCDCB- SCDCD-). This signal enables interrupt output signal CCITCY to be generated, if the interrupt system is unmasked (ITSVENB ITFINH-). It also enables interrupt service register clock signal KKITSVR and causes the number of the requesting level to be copied into the interrupt service register (ITRSV10 through ITRSV13, Dwg 394582, Sht 9) at the end of the next time period.

4-601. Interrupt signal CCITCY is checked by the sequence counter at the completion of each programmed instruction when CCCMEND is true and before the next instruction is fetched (paragraph 4-154). This may require one or several machine cycles, depending upon the nature of the instruction being executed. If an interrupt is received on a higher priority level during an intervening machine cycle T0 time period, the original interrupt request signal will be replaced by the higher priority request signal, and the number of the higher priority level will replace the number of the original priority level in the interrupt service register. Thus a higher interrupt level may "steal" an interrupt service cycle initiated by a lower level before the service cycle is started.

4-602. Once the sequence counter enters the interrupt service cycle (SCDC7 + SCDCB + SCDCD), signal ITSVENB is inhibited. Interrupts on other levels may be received and stored, but higher level interrupts cannot break into the interrupt service cycle. In addition, the sequence counter advances directly to the fetch phase of the first instruction of the interrupt service routine from phase D of the interrupt service cycle without checking the state of signal CCITCY, so that a higher level interrupt request waiting to be serviced at the end of the interrupt service cycle cannot be serviced until after the first instruction of the interrupt service routine has been executed. If

desired, this instruction can be a MSK instruction to prevent higher levels from interrupting. Since inhibit flip-flop ITFINH is set at the end of time period T3, signal CCITCY will then be inhibited before the sequence counter can enter another interrupt service cycle.

4-603. The outputs of the interrupt service register, signals ITRSV10 through ITRSV13, are used in the forced memory address logic to force addresses during the interrupt service cycle (paragraph 4-420). At the beginning of the cycle, the interrupt level being serviced is placed on the active state. Signal ITACT- (Dwg 394567, Sht 9) becomes false during time period T0 of the first phase of the interrupt service cycle (SCDC7 T0) and gates the interrupt request signal that initiated the cycle into the reset input of its corresponding enable flip-flop. The enable flip-flop is clocked reset at the end of time period T0.

4-604. Resetting of an enable flip-flop places the level into the active state and also terminates the request signal that initiated the service cycle. The level remains in the active state until the end of the interrupt service routine for that level, and no additional interrupts will be accepted on that level while it remains in the active state. The active flip-flop remains set and prevents lower level requests from being generated during the interrupt service routine.

4-605. An INR instruction addressed to the level being serviced is made the last instruction in each interrupt service routine. This instruction resets the active flip-flop and sets the enable flip-flop for the interrupt level at the end of the instruction fetch phase, which returns the level to the idle state and enables interrupt requests to be generated on the same or lower levels. However, at the end of the interrupt return cycle, the sequence counter advances directly to the fetch phase of the next instruction without generating signal CCCMEND, so at least one program instruction (or one instruction of an interrupted service routine) will be executed before a new interrupt can be serviced.

4-606. If the interrupt system was masked to prevent a higher level interrupt from interrupting the service routine, an UNM instruction must precede the ending INR instruction to re-enable the interrupt system. If a higher level interrupt is waiting to be serviced when the system is unmasked, it will not be serviced until the INR instruction and one instruction of the interrupted program have been executed.

4-607. Interrupt Service Cycle

4-608. The interrupt service cycle requires three machine cycles to execute and is performed in sequence counter phases 7, B, and D (SCDC7, SCDCB, and SCDCD). During the interrupt service cycle, the program count of the interrupted program and a machine status word are stored into memory, and an interrupt service routine linkage address is loaded into the program counter from memory.

4-609. The memory locations required for this function are reserved in the first few locations in memory, the size of storage depending upon the number of interrupt levels in the system. Memory locations are assigned to the interrupt levels in blocks of four: locations 0000 through 0003 are assigned to level 0, locations 0004 through 0007 are assigned to level 1, etc. The first location in each block is used to store the program count, the second is used to store the linkage address, and the third is used to store the machine status word. The fourth location in each block is not used by the interrupt system, but is included in the block because it is simpler to address locations in blocks of four than in blocks of three. These locations are not wasted, because they are used to store linkage addresses used by the standard executive program.

4-610. The sequence counter enters the interrupt service cycle from the CCCMEND state if an interrupt is waiting to be serviced (CCITCY). While in the CCCMEND state, the address of the first location in the block assigned to the level being serviced is forced into the memory address register by the memory address logic (paragraph 4-420). The states of the interrupt service register flip-flops are used in the forced address logic to specify the appropriate block of memory locations to be used.

4-611. During the first interrupt service phase (SCDC7), the contents of the program counter

register are stored into the first memory location in the block, and the address of the third location in the block is forced in the memory address logic for use in the second phase of the cycle (SCDCB).

4-612. In the second phase of the cycle, a machine status word is assembled and stored into the third location of the block. This machine status word includes the contents of the extension register and the states of flip-flops ADFNEG, ADFEQL, ADFOVF, and CCFGLB. Also, the address of the second location in the block is forced into the memory address register for use during the third phase of the cycle (SCDCD).

4-613. The address of the first instruction of the interrupt service routine appropriate to the interrupt level being serviced is read out of the second location of the block and loaded into the program counter register during the third phase of the cycle. The first five bits of the address are also copied into the extension register, and global control flip-flop CCFGLB is set at the end of the phase. Since phase D of the interrupt service cycle passes through the CCCMENDA state, interrupt signal CCITCY is not checked, and the sequence counter advances to phase 1 to fetch the first instruction of the interrupt service routine for execution.

4-614. Interrupt Return Cycle

4-615. At the conclusion of an interrupt service routine, an INR instruction is executed to return to the operation that was interrupted by the interrupt just serviced. This could be to a point in the main program or to a point in the interrupt service routine of a lower-order interrupt. The INR instruction requires three machine cycles to execute: an instruction fetch phase (SCDC1), an interrupt return phase (SCDC9), and a memory read phase (SCDC5).

4-616. During the interrupt return cycle, the interrupt level is placed into the idle state, the machine status is restored, and the program count at the point of interruption is loaded into the program counter register. The memory locations used in the interrupt return cycle are the same as those used in the interrupt service cycle, but the block addresses in the forced memory addresses are derived from the F2 field of the INR instruction rather than from the interrupt service register.

4-617. In the instruction fetch phase of INR instruction execution, the interrupt level just serviced is placed into the idle state, and the address of the third location in the block of memory locations assigned to the level is forced in the memory address logic for use in the interrupt return phase (SCDC9).

4-618. In the interrupt return phase, the machine status word is read and loaded into the extension register and flip-flops ADFNEG, ADFEQL, ADFOVF, and CCFGLB. The address of the first location in the block is formed in the memory address logic during this phase to be used in the memory read phase (SCDC5).

4-619. The purpose of the memory read phase is to read in the program count stored in location one of the block. The program count is loaded into the program counter register via the adder, and the sequence counter advances directly to the fetch phase of the next instruction of the interrupted program by passing through the CCCMENDA state. This causes the status of interrupt signal CCITCY to be ignored and ensures that at least one instruction of the interrupted program will be executed before another interrupt can be serviced.

4-620. TELETYPEWRITER SET CONTROLLER OPTION

4-621. While the teletypewriter set controller is usually contained in the CPU chassis, it communicates with the CPU only over the data input-output (DIO) bus in the same manner as external peripheral device controllers. The controller operates with modified Teletype Corp. Model 33 and Model 35 Automatic Send-Receive (ASR) Sets.

4-622. The description, theory of operation, and maintenance instructions for the teletypewriter sets are contained in the Teletype Corp. manuals supplied with the sets. These manuals cover only the unmodified units. The modifications to permit these sets to operate with the teletypewriter set controller are described in paragraphs 4-623 and 4-632.

4-623. Model 33 Teletypewriter Set Modifications

4-624. The modifications to permit communication between the Model 33 teletypewriter set and the teletypewriter set controller consist of changes in the wiring of the line relay and the addition of two relays and two indicators. The modified circuits are shown schematically in figure 4-31. The optional MANUAL INTERRUPT switch, which is mounted on the teletypewriter set, is also shown in figure 4-31.

4-625. The changes in the wiring of the line relay permit the set to operate off line when the power switch is set to LOCAL and on line with the controller when the switch is set to LINE. The relay is not energized in the local mode, and the serial character codes are supplied to the selector magnet driver from the distributor. The 60-vdc supply supplies the signal current which is controlled by the distributor and the keyboard or paper tape reader contacts.

4-626. Relays K1 and K2 are used in the line mode to send data to and receive data from the controller and are disabled in the local mode. Relay K1 is energized by the 60-vdc supply in the local mode, and its contacts are held open: signal TTYDIN, which is the output signal to the controller, is held true. The contacts of relay K2, which is controlled by input signal TTDOT from the controller, are disconnected from the selector magnet driver in the local mode and are shorted. Thus signal TTDOT can have no effect in the teletypewriter set in the local mode.

4-627. In the line mode, the line relay is energized. This disconnects the distributor from the selector magnet driver and connects it to the coil of relay K1. The contacts of relay K2 are unshorted and are connected across the input to the selector magnet driver. The 60-vdc supply is only used to supply the current to operate relay K1 in this mode.

4-628. Characters originated at the keyboard or paper tape reader are transmitted only to the controller in the line mode, and characters to the typing unit and paper tape punch are received only from the controller. Output characters are routed to the controller from the distributor via relay K1 and signal line TTYDIN. Input characters from the controller are routed to the selector magnet driver via signal line TTDOT and relay K2.

4-629. When it is desired to print characters being sent to the controller from the keyboard, the character sent to the controller is sent back to the selector magnet driver from the controller. This is a function of the controller logic and is discussed in paragraph 4-687.

4-630. The two indicator lights indicate the operating mode selected in the controller. The PTR light is lighted when input from the paper tape reader is desired, and the KBD light is lighted when input from the keyboard is desired. Both lights are out when the controller is disconnected or output to the printer or paper tape punch is desired.

4-631. The signals that control the indicator lights (TTKBDL- and TTPTRL-) perform no control functions in the teletypewriter set, and it is the responsibility of the operator to set the controls correctly on the teletypewriter set to perform the desired function. The operating modes of the controller are discussed in paragraph 4-664.

4-632. Model 35 Teletypewriter Set Modifications

4-633. The Model 35 teletypewriter set communicates with the teletypewriter set controller in the same manner as the Model 33 teletypewriter set. However, the construction of the sets differ considerably, and more extensive modification is required in the Model 35 set. The modified circuits are shown schematically in figure 4-32. The optional MANUAL INTERRUPT switch, which is mounted on the teletypewriter set, is also shown in figure 4-32.

4-634. The two added relays (K1 and K2) and the two added indicators (DS1 and DS2) perform the same functions as in the modified Model 33 sets. The resistor across the coil of relay K1 is omitted because the signal current in the modified Model 35 set is 20 ma, while it is 60 ma in the modified Model 33 set.

4-635. The line relay performs the same function in both sets, but different circuits are switched in the Model 35 set, and the effect on the controller in the local mode differs between the two sets.

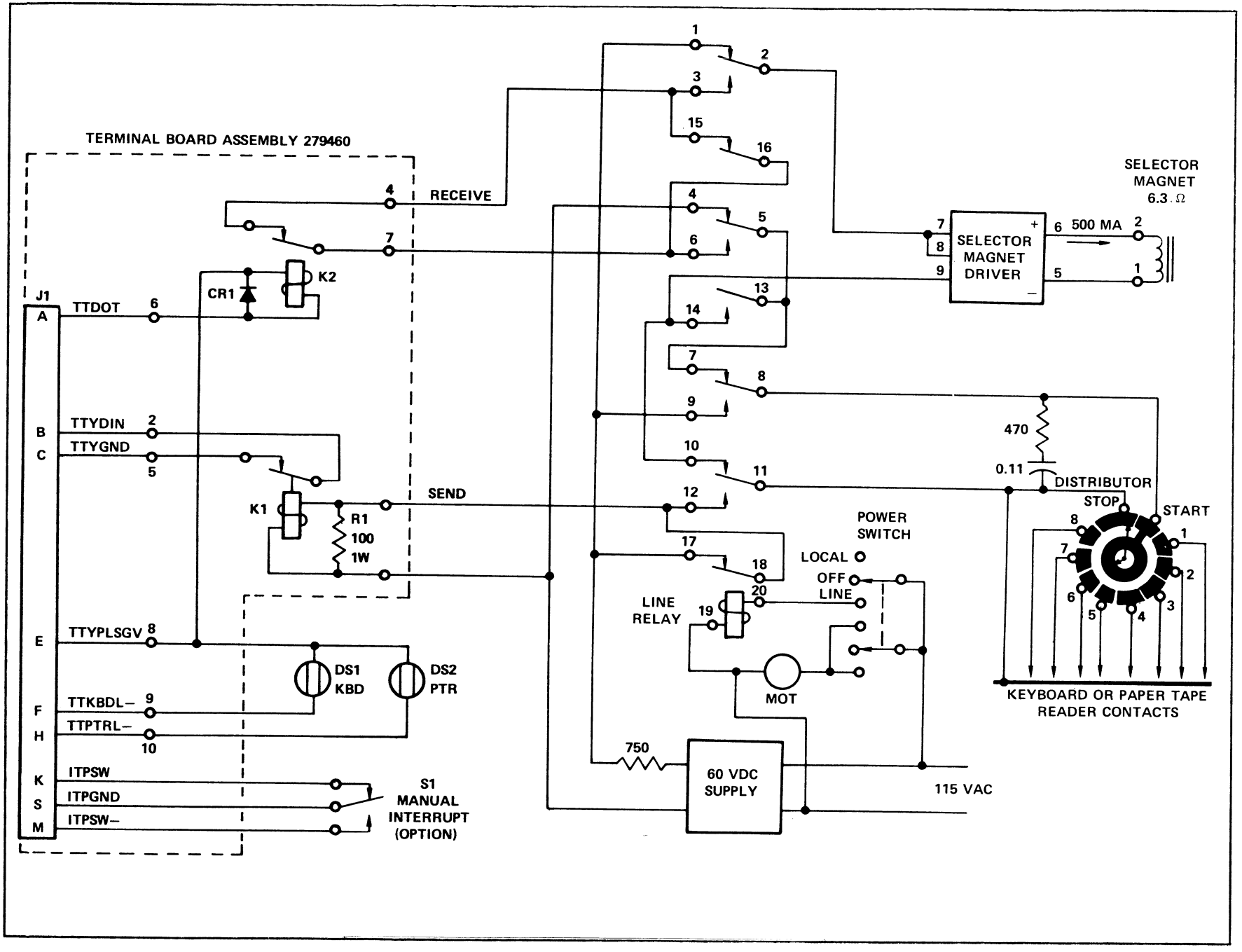


Figure 4-31. Controller/ASR33 Teletypewriter Set Interface

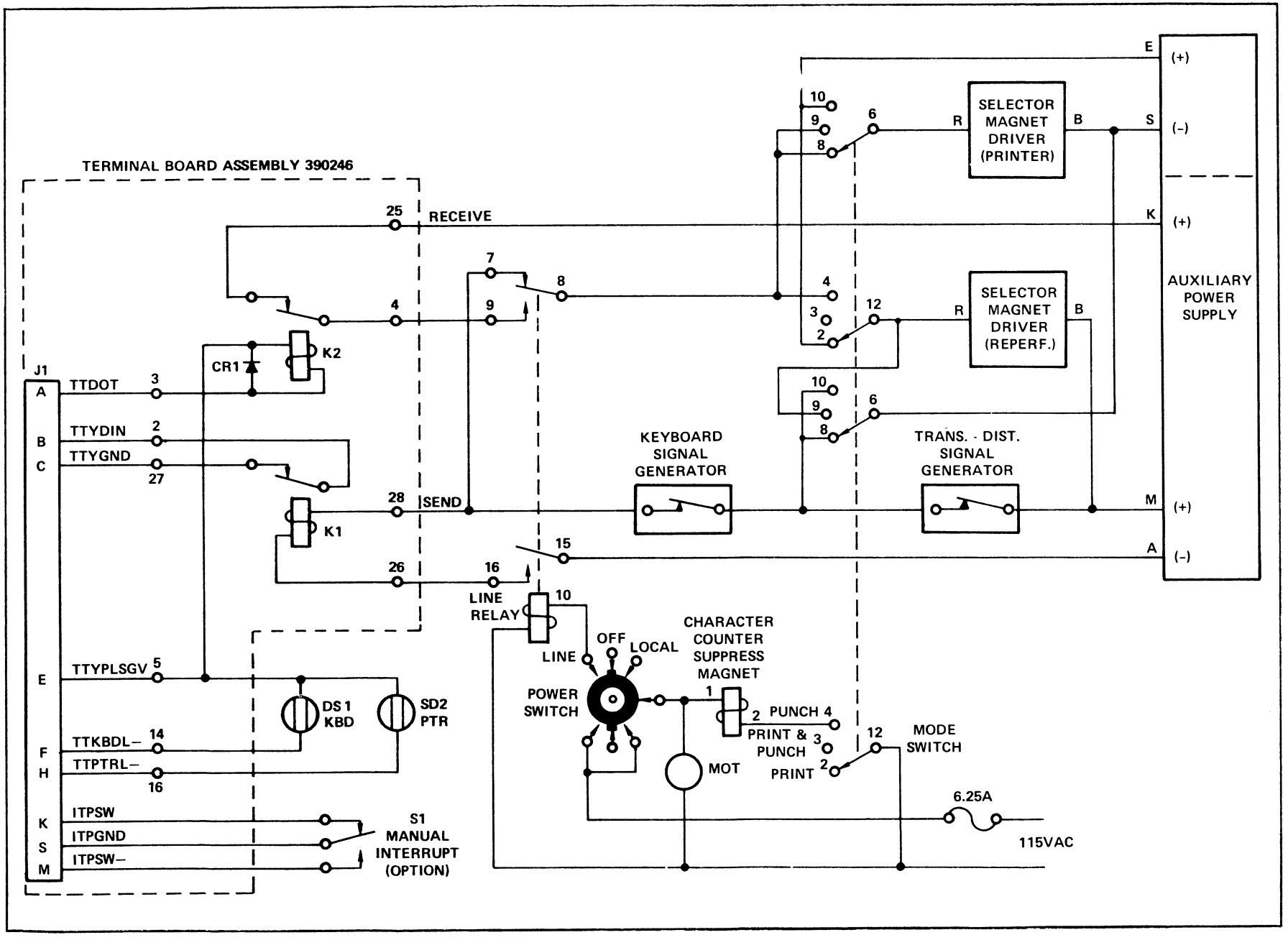


Figure 4-32. Controller/ASR35 Teletypewriter Set Interface

Separate signal generators are used for the keyboard and transmitter-distributor (paper-tape reader). These signal generators are connected in series through their normally-closed contacts so that either generator may place signals onto the signal line. Also, separate selector magnet drivers are used for the printer and reperforator (paper-tape punch), and either or both may be placed in series with the signal line depending on the setting of the MODE switch.

4-636. When the power switch is set to LOC, the line relay is not energized, and the series-connected signal generators are connected to one or both of the selector magnet drivers via the normally-closed contacts of the line relay and the MODE switch. The signal current (20 mA) is supplied from pin M of the auxiliary power supply. Relay K1 is not energized in this mode as it is in the modified Model 33 set. This holds signal TTYDIN false, and does not simulate a stop signal from the signal generators. The controller must not be in the keyboard or paper-tape reader modes (paragraph 4-664), or interrupt level 00 must be disabled when the Model 35 set is in local mode to avoid the continuous transmission of spurious characters to the CPU.

4-637. The line relay is energized when the power switch is set to ON LINE. This connects relay K1 to the signal generators and connects the contacts of relay K2 to the selector magnet drivers. The 20-mA signal current for the receive circuit is supplied from pin K of the auxiliary power supply. As in Model 33 sets, characters are sent to the controller via relay K1 and are received from the controller via relay K2.

4-638. The two indicator lights indicate the operating mode selected in the controller. The PTR light is lighted when input from the paper tape reader is desired, and the KBD light is lighted when input from the keyboard is desired. Both lights are out when the controller is disconnected or output to the printer or paper tape punch is desired.

4-639. The signals that control the indicator lights (TTKBDL- and TTPTRL-) perform no control functions in the teletypewriter set, and it is the responsibility of the operator to set the MODE switch to the correct position and to operate the teletypewriter set so as to provide the desired inputs or outputs.

4-640. The MODE switch is modified mechanically to reduce the number of switch positions from five to three, and the wiring to the switch is modified considerably. Only those sections of the mode switch that perform a function in the modified set are shown in figure 4-32. The three switch positions used are reidentified as PRINT, PRINT & PUNCH, and PUNCH.

4-641. The chief function of the MODE switch in the modified set is to switch the signal current to one or both selector magnet drivers and to disable the unused driver when only one is being used. The signal inputs are from either signal generator when the power switch is set to LOC and from relay K2 when the power switch is set to ON LINE.

4-642. In the PRINT position, the selector magnet driver for the printer is in series with the signal line, and the reperforator selector magnet driver is disabled by a steady 20-mA current supplied by a separate power supply on the auxiliary power supply card (pins E and S). The negative sides of the power supplies (pins A and S) are not connected together internally in the power supply board, and these two supplies operate independently of each other. The negative sides of the supplies are connected together when the mode switch is set to PRINT in order to return the signal current from the printer selector magnet to pin A of the supply and the disabling current from the reperforator selector magnet driver to pin S.

4-643. In the PRINT & PUNCH position of the MODE switch both the printer and reperforator selector magnet drivers are connected in series with the signal line. No disabling current is supplied by the auxiliary power supply in this mode.

4-644. Signal current is supplied only to the reperforator selector magnet driver when the MODE switch is set to PUNCH. The printer selector magnet driver is disabled by the disabling current from the auxiliary power supply. The character counter suppress magnet is also energized by the mode switch to permit sending characters

from the keyboard without operating the character counter mechanism.

4-645. Character Codes

4-646. Both the Model 33 and Model 35 teletypewriter sets employ the standard 8-level, 11-unit character transmission code. Teletypewriter sets used with the 704 Processor operate at 100 wpm and do not use even parity checking. The No. 8 code element, which is the parity bit, is always marking (1) in both models.

4-647. The character code is the 8-level American Standard Code for Information Interchange (ASCII). The character is transmitted as a series of eight spacing (0) or marking (1) pulses preceded by a start pulse (spacing) of the same duration as the character pulses and followed by a stop pulse (marking) of twice the duration of the character pulses. Thus the actual signal transmitted contains 11 units, based on the duration of one character pulse as one unit. At 100 wpm, the character is transmitted in 100 ms, and each unit is transmitted in 9.09 ms.

4-648. Transmission and reception of character codes is timed mechanically in the teletypewriter sets by rotating shafts. When tripped, the shafts make one revolution in 100 ms and actuate contacts that generate or receive the coding pulses. This action is simulated in the teletypewriter set controller by a shift register that is clocked at approximately the same rate and is used to transmit and receive the serial characters. Operation of the shift register is discussed in paragraphs 4-701 and 4-716.

4-649. Characters are transmitted, processed and stored in the same code format in which they are received. In text, the terms "ASCII code" and "teletypewriter code" are used interchangeably. The character codes used by the 704 Processor and their hexadecimal equivalents are listed in table 4-5.

4-650. Communication Between CPU and Teletypewriter Set Controller

4-651. The CPU and teletypewriter set controller communicate over the data input-output (DIO) bus by means of DIN and DOT program instructions and interrupts on level 00. The DIN and DOT instructions are used to select the operating modes of the controller, transfer data, and obtain status responses from the controller. The interrupt is used to signal the CPU that the controller is ready to accept a character from the CPU or has a character to transmit to the CPU.

4-652. The DIN and DOT instructions place an 8-bit command word on the data address lines (DAD08- through DAD15-) of the DIO bus. Data is transferred to the controller from the accumulator register in the CPU over eight of the data output lines (DOT08- through DOT15-), and data is transferred from an assembly register in the controller to the CPU accumulator register over eight of the data input lines (DIN08- through DIN15-). Status responses are returned to the CPU from the controller over data input lines DIN00- and DIN07-.

4-653. Each of the command words placed on the data address lines by DIN or DOT instructions consists of a four-bit device address code (bits 08 — 11) and a four-bit function code (bits 12 — 15). For convenience of notation, these four-bit codes are converted to two hexadecimal digits. The contents of the command word is specified in the F1 and F2 fields of the DIN or DOT instruction. The device address normally assigned to the teletypewriter set controller is E (1110). The function codes are discussed in paragraph 4-655.

4-654. Operation of the controller is synchronized with operation of the CPU by input strobe signal DISB-, output strobe signal DOSB-, and external clock signal KEXT1- from the CPU.

4-655. Function Codes

4-656. The four-bit function code permits a total of 16 different function codes. Most of the function codes may only be used with one instruction, either a DIN instruction or a DOT instruction, as shown in table 4-6. Function code 0 may be used with either a DIN or DOT instruction, and the function performed depends on the instruction

Table 4-5. ASCII (Teletypewriter) Character Codes and Hexadecimal Equivalents

Char.	87654321	Hex.	Char.	87654321	Hex.	Char.	87654321	Hex.	Char.	87654321	Hex.
@	11000000	C0	SP	10100000	A0	NULL	10000000	80		11100000	E0
A	11000001	C1	!	10100001	A1	SOM	10000001	81		11100001	E1
B	11000010	C2	”	10100010	A2	EOA	10000010	82		11100010	E2
C	11000011	C3	#	10100011	A3	EOM	10000011	83		11100011	E3
D	11000100	C4	$	10100100	A4	EOT	10000100	84		11100100	E4
E	11000101	C5	%	10100101	A5	WRU	10000101	85		11100101	E5
F	11000110	C6	&	10100110	A6	RU	10000110	86		11100110	E6
G	11000111	C7	’	10100111	A7	BELL	10000111	87		11100111	E7
H	11001000	C8	(	10101000	A8	FE_0	10001000	88		11101000	E8
I	11001001	C9	)	10101001	A9	TAB	10001001	89		11101001	E9
J	11001010	CA	*	10101010	AA	LF	10001010	8A		11101010	EA
K	11001011	CB	+	10101011	AB	VT	10001011	8B		11101011	EB
L	11001100	CC	,	10101100	AC	FORM	10001100	8C		11101100	EC
M	11001101	CD	—	10101101	AD	RETURN	10001101	8D		11101101	ED
N	11001110	CE	.	10101110	AE	SO	10001110	8E		11101110	EE
O	11001111	CF	/	10101111	AF	SI	10001111	8F		11101111	EF
P	11010000	D0	0	10110000	B0	DC_0	10010000	90		11110000	F0
Q	11010001	D1	1	10110001	B1	X ON	10010001	91		11110001	F1
R	11010010	D2	2	10110010	B2	R1 ON	10010010	92		11110010	F2
S	11010011	D3	3	10110011	B3	X OFF	10010011	93		11110011	F3
T	11010100	D4	4	10110100	B4	R1 OFF	10010100	94		11110100	F4
U	11010101	D5	5	10110101	B5	ERR	10010101	95		11110101	F5
V	11010110	D6	6	10110110	B6	SYNC	10010110	96		11110110	F6
W	11010111	D7	7	10110111	B7	LEM	10010111	97		11110111	F7
X	11011000	D8	8	10111000	B8	S_0	10011000	98		11111000	F8
Y	11011001	D9	9	10111001	B9	S_1	10011001	99		11111001	F9
Z	11011010	DA	:	10111010	BA	S_2	10011010	9A		11111010	FA
[	11011011	DB	;	10111011	BB	S_3	10011011	9B		11111011	FB
/	11011100	DC	<	10111100	BC	S_4	10011100	9C	ACK	11111100	FC
]	11011101	DD	=	10111101	BD	S_5	10011101	9D	ALT	11111101	FD
↑	11011110	DE	>	10111110	BE	S_6	10011110	9E	ESC	11111110	FE
←	11011111	DF	?	10111111	BF	S_7	10011111	9F	RUB OUT	11111111	FF

Table 4-5. ASCII (Teletypewriter) Character Codes and Hexadecimal Equivalents (Cont)

LEGEND			
/	Reverse slant	RETURN	Carriage return
↑	Up Arrow (Exponentiation)	SO	Shift out
←	Left Arrow (Implies/Replaced by)	SI	Shift in
SP	Space	DC_0	Device control (reserved for data link escape)
NULL	Blank		
SOM	Start of message	X ON	Transmitter on
EOA	End of address	R1 ON	Receiver on (TAPE)
EOM	End of message	X OFF	Transmitter off
EOT	End of transmission	R1 OFF	Receiver off (TAPE)
WRU	Who are you?	ERR	Error
RU	Are you ?	SYNC	Synchronizing character
BELL	Audible signal	LEM	Logical end of medium
FE_0	Format effector	S_n	Information separators
TAB	Horizontal tabulation	ACK	Acknowledge
LF	Line feed	ALT MODE	Escape (for communicators)
VT	Vertical tabulation	ESC	Escape (for data processing)
FORM	Form feed	RUB OUT	Delete

Table 4-6. Teletypewriter Set Controller Function Codes

Bits					Function Code Definition	
12	13 Tx Data	14 Out	15 In	Hexa.	DIN Instruction	DOT Instruction
0	0	0	0	0	Request Status	Disconnect teletypewriter set
X	0	0	1	1, 9	———	Select paper-tape reader (PTR mode)
X	0	1	0	2, A	———	Select print/punch (P/P mode)
X	0	1	1	3, B	———	Select keyboard (KBD mode)
X	1	0	0	4, C	Input character and disconnect	———
X	1	0	1	5, D	Input character (PTR mode)	———
X	1	1	0	6, E	———	Output character (P/P mode)
X	1	1	1	7, F	Input character (KBD mode)	———
1	0	0	0	8	———	Disconnect teletypewriter set

X indicates that state of bit 12 is irrelevant to this particular function code

used to transmit the code. This increases the number of functions that may be performed to 17, not all of which are used.

4-657. Except when requesting status, bit 12 has no significance in those function codes that merely select one of the modes of transferring data between the controller and the teletypewriter set because no data is transferred between the CPU and the controller by these instructions. When no data is transferred between the CPU and the controller, the data transfer mode is immaterial, and either of the pair of codes (0 and 8, 1 and 9, etc) may be used for the select operation.

4-658. Bit 13 determines whether data is transferred between the CPU and the controller or not. When the bit is 0, the mode of transferring data between the controller and the teletypewriter set is selected, but no data is transferred. (Bit 13 is also 0 when status is requested, but the status response to the CPU is not considered data.) When bit 13 is 1, data is transferred between the CPU and the controller.

4-659. Except when requesting status, bits 14 and 15 of the function code determine the mode of transferring data between the controller and the teletypewriter set. These modes are discussed in paragraph 4-664.

4-660. Function codes that transfer data between the CPU and the controller (4 through 7 and C through F) may also be used to select the mode of transferring data between the controller and the teletypewriter set, to retain the mode previously selected, or to disconnect the teletypewriter set.

4-661. When inputting data from the teletypewriter set, a select instruction must be executed to select the paper-tape reader or keyboard mode prior to executing the first instruction to transfer a character to the CPU. This is necessary because a character must be placed into the assembly register from the teletypewriter set before it can be transferred to the CPU.

4-662. Normally the instruction that transfers a character into the CPU specifies the previously selected mode in bits 14 and 15 of the function code, and subsequent characters are transferred in without the necessity of additional select instructions. It is also possible to input a character and disconnect the teletypewriter set with the same instruction (function codes 4 and C). These function codes have limited application and are seldom used.

4-663. It is not necessary to select the print/punch mode prior to outputting data to the teletypewriter set. The same function code (6 or E) may be used to transfer a character from the CPU to the controller assembly register, select the print/punch mode, and transfer the character from the assembly register to the teletypewriter set. Function codes 2 through A, which only select the print/punch mode, are also of limited application and are seldom used.

4-664. Controller/Teletypewriter Set Data Transfer Modes

4-665. Data is transferred between the controller and the teletypewriter set in serial form. An assembly register in the controller is used to receive parallel data from the CPU and to transmit the data in serial form to the teletypewriter set receive circuit via data output line TTDOT. The same register is used to receive serial data from the teletypewriter set send circuit via data input line TTYDIN and to transmit the data in parallel form to the CPU.

4-666. Note that the assembly register communicates only with the teletypewriter set send and receive circuits, not individual components of the set (keyboard, paper-tape punch, printer, and paper-tape reader). The controller has no control over the destination of data sent to the set (printer, paper-tape punch, or both) nor the source of data received from the set (keyboard or paper-tape reader). These are determined solely by the teletypewriter set controls and the manner in which the set is operated.

4-667. Four modes of transmitting data between the controller and the teletypewriter set may be used. These modes are specified by bits 14 and 15 of the teletypewriter set function codes (paragraph 4-665). The modes specified and the data paths set

up by these bits are shown in table 4-7. The KBD and PTR lights added to the teletypewriter set are also controlled by the mode selected, and the states of these lights in each mode are also shown in the table.

4-668. The data transfer modes only have significance when the teletypewriter set is operating in the ON LINE mode. When the set is operating in the LOCAL mode, the send and receive circuits are connected together internally and are disconnected from the controller input and output lines.

4-669. In the disconnect mode (00), there is no communication between the assembly register and the teletypewriter set. Data sent to the controller from the teletypewriter send circuit is returned to the receive circuit, and the assembly register is isolated from both circuits. Operation of the teletypewriter set in this mode is identical to operation in the LOCAL mode except for the routing of data between the send and receive circuits.

4-670. When inputting data from the paper-tape reader, it is usually not desired to print the data or punch a duplicate tape. The paper-tape reader mode (01) permits data to be transferred from the send circuit to the assembly register, but isolates the receive circuit so that the data will not be printed or punched.

4-671. When inputting data from the keyboard, it is usually desired to print out the characters being typed. In the keyboard mode (11), data that is transferred from the send circuit to the assembly register is also returned to the receive circuit to be printed and/or punched.

4-672. While input is normally from the paper-tape reader in the paper-tape reader mode and from the keyboard in the keyboard mode, the keyboard may be used in the paper-tape mode and vice versa. The only difference between the two modes is whether the data is returned to the receive circuit or not.

4-673. In the print/punch mode (10), data is transferred from the assembly register to the receive circuit, and the send circuit is isolated. The setting of the teletypewriter set controls determine whether the data being outputted is printed, punched (Model 35 only), or printed and punched.

4-674. Status Response

4-675. The status of the teletypewriter set controller may be obtained by executing a DIN instruction with address E and function code 0 (DIN E 0). The status response is returned on data input lines DIN00- and DIN07- of the DIO bus.

4-676. Bit 00 of the status response reflects the controller/teletypewriter set data transfer mode of the controller (paragraph 4-664). If the controller is in the disconnect mode, bit 00 is 0, and the controller is considered "not busy." If any of the other three modes is selected, bit 00 is 1, and the controller is considered "busy." Note that bit 00 reflects only the mode selected, not whether data is being transferred or is waiting in the assembly register to be transferred.

4-677. Bit 07 of the status response reflects the interrupt status of the controller. If no interrupt is waiting to be serviced, bit 07 is 0. If an interrupt has been sent to the CPU and has not been serviced, bit 07 is 1.

4-678. Interrupts

4-679. Interrupts are sent to the CPU on interrupt level 00. This is the lowest-priority interrupt level in a multi-level system. The interrupt is generated when a character is transferred (serially) between the controller and the teletypewriter set.

4-680. When inputting a character from the teletypewriter set (paper-tape reader or keyboard mode), the interrupt is generated when the last bit of the eight-bit character code has been shifted into the assembly register. The interrupt in this case signifies that a character is waiting in the assembly register to be transferred to the CPU.

Table 4-7. Controller/Teletypewriter Set Data Transfer Modes

Function Code Bits		Data Transfer Mode	Teletypewriter Indicator Lights		Data Flow (ON LINE Mode)
14	15		KBD	PTR	Controller / Teletypewriter Set
0	0	Disconnect	OFF	OFF	Assembly Register → Receive Ckt; Send Ckt
0	1	Paper-Tape Reader	OFF	ON	Assembly Register ← Send Ckt; Receive Ckt
1	0	Print/Punch	OFF	OFF	Assembly Register → Receive Ckt; Send Ckt
1	1	Keyboard	ON	OFF	Assembly Register ← Send Ckt; Receive Ckt

4-681. In the keyboard mode, the KBD light on the teletypewriter set is turned off by the interrupt and is turned back on when the character is transferred to the CPU. The light is turned off to indicate that the controller cannot accept another character and is turned on to indicate that another character may be typed. Characters typed while the light is off (in keyboard mode only) will not be accepted by the assembly register or will be garbled if the interrupt is serviced while the character is being transferred from the keyboard.

4-682. When outputting a character from the controller to the teletypewriter set (print/punch mode), the interrupt is generated when the first "stop" bit is transferred to the teletypewriter set. The interrupt in this case signifies that the character has been transferred to the teletypewriter set and that the controller is ready to receive another character from the CPU.

4-683. The interrupt logic and timing are discussed in paragraphs 4-701 and 4-716.

4-684. Controller Logic

4-685. The controller logic is shown in block diagram form in figure 4-33. The command word decode logic supplies control signals that determine the data transfer modes between the CPU and the assembly register and between the assembly register and the teletypewriter set. It also gates data into and out of the register, controls the initiation and termination of interrupts, and controls the generation of status responses.

4-686. The serial transmission of data between the assembly register and the teletypewriter set requires that the 11-unit code be transmitted from and received by the assembly register in the same form and with the same timing as used in the teletypewriter set. This function is performed by the clock enable logic, clock counter, input shift enable logic, shift logic, and sequencer.

4-687. Command Decoding

4-688. When a command word is addressed to the teletypewriter set controller, the decoding of the function code is enabled by signal TTADDC (Drawing 394587, Sheet 6). Signal TTADDC becomes true when an address of E (1110) is received on data address lines DAD08- through DAD11-.

Note

The device address of E for the teletypewriter set controller is a convention adopted for standardized system software. It can be changed by making appropriate jumper connections on the controller card. Refer to Section V.

4-689. The control signals generated when signal TTADDC becomes true depend on whether a DIN or DOT instruction is being executed by the CPU and whether status is being requested or not. If a DIN instruction is being executed, input strobe signal TTDISB is true, and the state of status request signal TTSTRQ determines whether a status response or data is returned to the CPU.

4-690. Signal TTSTRQ is true when status is requested (function code 0), and signal TTSTIN gates the status response onto data input lines DIN00- and DIN07-. The states of mode flip-flops TTFOUT and TTFIN determine the response on line DIN00-. If either flip-flop is set (TTFOUT + TTFIN), the response is 1. If both are reset (TTFOUT- TTFIN-), the response is 0. The state of interrupt flip-flop TTFINT determines the response on line DIN07-. The response is 1 if the flip-flop is reset and 0 if it is set.

Note

The functions of flip-flops TTFINT and TTFISF have been inverted in the process of hardware layout. That is to say, the TTFINT flip-flop must be reset (TTFINT- true) to send an interrupt to the CPU, and the TTFISF flip-flop must be reset (TTFISF- true) to enable input data shifting into the assembly register.

4-691. Signal TTSTRQ is false when any DIN instruction except a status request is executed, and

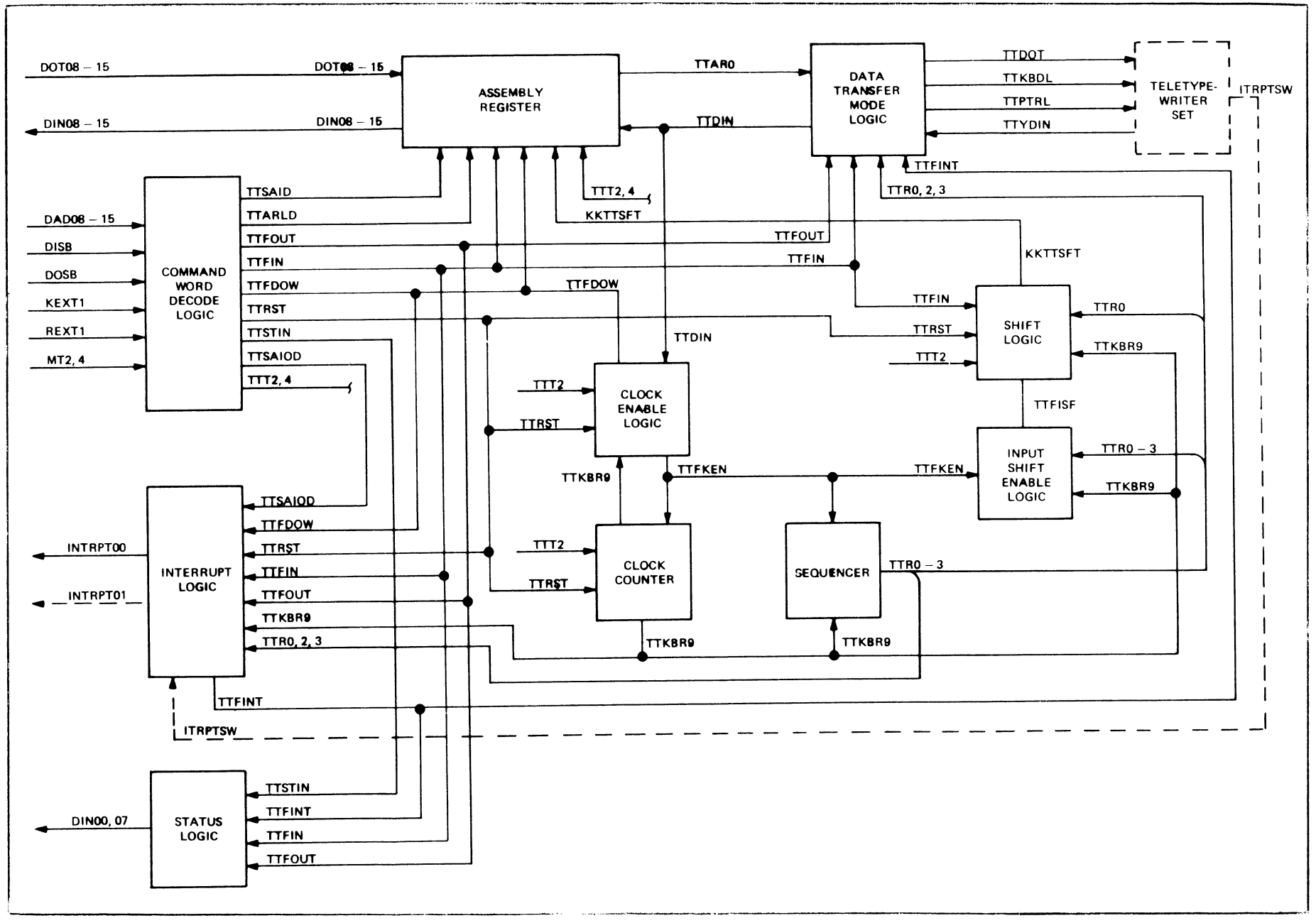


Figure 4-33. Teletypewriter Set Controller Block Diagram

the contents of the assembly register is gated onto data input lines DIN08- through DIN15- by signal TTSAID.

4-692. If a DOT instruction is being executed, output strobe signal TTDOSB is true, and bit 13 of the command word determines whether a select or data transfer operation is performed. If bit 13 is 1, signal TTARLD gates a character into the assembly register from data output lines DOT08- through DOT15- and sets data-out-waiting flip-flop TTFDOW. If bit 13 is 0, no data is transferred from the CPU to the assembly register by the DOT instruction, and flip-flop TTFDOW remains reset.

4-693. When either a DIN instruction (except a status request) or a DOT instruction is executed, signal TTSAIOD becomes true. This signal directly sets interrupt flip-flop TTFINT and enables mode flip-flops TTFOUT and TTFIN. The states of bits 14 and 15 of the function code are copied into these flip-flops whenever any instruction except a status request is addressed to the controller.

4-694. Flip-flops TTFOUT and TTFIN determine the mode of transmitting data between the controller and the teletypewriter set. (The four data transmission modes are discussed in paragraph 4-664.)

4-695. In the disconnect mode, both flip-flops are reset. The inputs to assembly register flip-flop TTARS are disabled by signal TTFIN being false, and data from the teletypewriter send circuit cannot be loaded into the assembly register via signals TTDIN and TTDIN-. Output from register flip-flop TTAR0 is disabled by signal TTFOUT being false, and data cannot be transmitted from the assembly register to the teletypewriter receive circuit via signal TTDOT. The output of one gate used to make up signal TTDOT is held true by signal TTFOUT being false, and signal TTKBORDC in the other gate is held true by both signals TTFIN and TTFOUT being false. Thus signal TTDOT reflects the state of signal TTYDIN, and data received from the teletypewriter send circuit via signal TTYDIN is returned to the receive circuit via signal TTDOT.

4-696. In the paper-tape reader mode, flip-flop TTFIN is set, and flip-flop TTFOUT is reset. This enables the inputs of assembly register flip-flop TTAR8 and allows data to be loaded into the assembly register from the teletypewriter send circuit. The output from flip-flop TTAR0 is still disabled (TTFIN- and TTFOUT false), but signal TTKBORDC is also false (TTFIN TTFOUT-), and signal TTDOT is held true. This prevents data being loaded into the assembly register from also being returned to the receive circuit.

4-697. In the print/punch mode, flip-flop TTFOUT is set, and flip-flop TTFIN is reset. This enables the output from assembly register flip-flop TTAR0 to be transmitted to the receive circuit via signal TTDOT and also disables the return of data from the send circuit to the receive circuit (TTFIN-TTFOUT). The reception of data from the send circuit by the register is also disabled by signal TTFIN being false.

4-698. In the keyboard mode, both flip-flop TTFOUT and flip-flop TTFIN are set. As in the paper-tape reader mode, the reception of data from the send circuit is enabled by signal TTFIN, and the tranmission of data from the register to the receive circuit is disabled (TTFIN- false). However, signal TTKBORDC is true in this mode, and data being loaded into the assembly register is also returned to the receive circuit.

4-699. Signals TTFIN and TTFOUT also control the KBD and PTR indicator lights on the teletypewriter set. The KBD indicator is lit in the keyboard mode if the assembly register is ready to accept another character (TTFINT TTFOUT TTFIN). If the last character transmitted to the register has not been transferred to the CPU, interrupt flip-flop TTFINT will be reset, and the KBD indicator will remain out until the character is transferred to the CPU. The PTR indicator is lit in the paper-tape reader mode (TTFIN TTFOUT-).

4-700. Signals TTFIN and TTFOUT also perform control functions in the interrupt logic and clock inhibit logic. These functions are discussed in the paragraphs that follow.

4-701. Character Input Operation

4-702. When either the paper-tape reader or keyboard mode is selected, signal TTFIN is true, and data transfer from the teletypewriter set to the CPU is enabled. Before a character is transmitted, interrupt flip-flop TTFINT is set (no interrupt) and clock enable flip-flop TTFKEN is reset. Signal TTFKEN being false directly resets sequencer flip-flops TTR0 — TTR3 and directly resets clock counter flip-flops TTKAR0 — TTKAR4 and TTKBR0 — TTKBR9 via signals TTKRDR1- through TTKRDR4-. Signal TTFKEN- is inverted and directly sets input shift flip-flop TTFISF to inhibit shift clock pulses.

4-703. The character is transmitted from the teletypewriter set as a series of eleven pulses of 9.09 ms duration. Two clock counter registers are used in the controller to generate a shift clock signal with very nearly the same period. The first counter register (TTKAR0 — TTKAR4) is a divide-by-nine ring counter that is clocked at the end of each time period T2 by signals TTT2A and TTT2B. The second counter register (TTKBR0 — TTKBR9) is a ten-stage binary counter that is clocked every ninth machine cycle by signal TTAR0- going false. The most-significant stage of the binary counter is set for 512 counters (4608 machine cycles) and reset for 512 counts, resulting in a clock output with a period of 9,216 machine cycles, or 9.216 ms. This results in a character transmission time of 101.376 ms rather than the nominal 100 ms of the teletypewriter set. The discrepancy is less than 2 percent and is well within the acceptable limits.

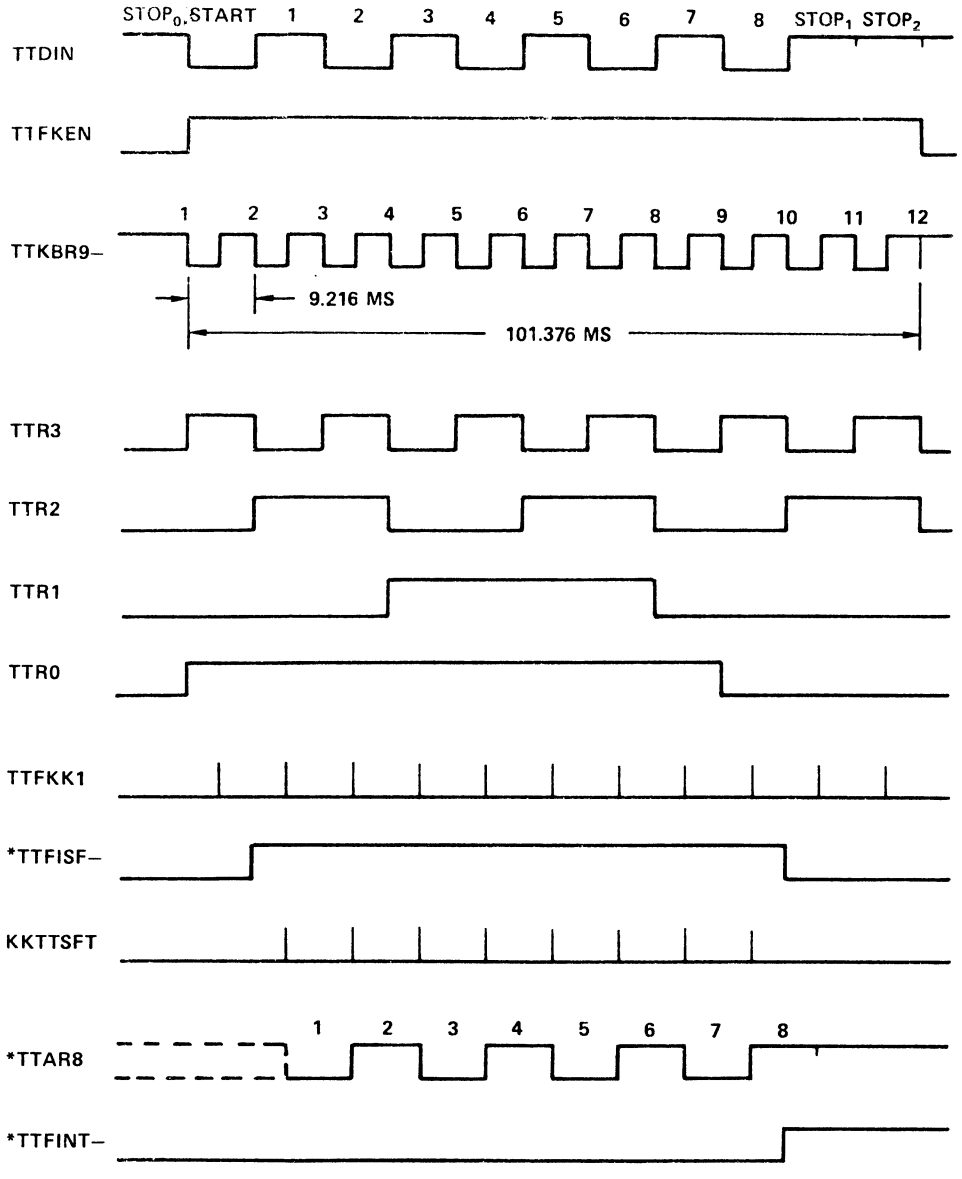
4-704. Before the character is transmitted, relay K1 in the modified teletypewriter set is held energized, and signal TTYDIN is held true. The first pulse of every character sent from the teletypewriter set is a "start" pulse, which is always spacing (no current). Relay K1 is deenergized during a spacing pulse and grounds signal TTYDIN, causing signal TTDIN- to become true. Clock enable flip-flop TTFKEN is directly set during the first time period T2 after signal TTDIN- becomes true (TTR0- TTR2- TTR3- TTT2 TTDIN-) and removes the direct reset from the sequencer and clock counter flip-flops.

4-705. The divide-by-nine ring counter is clocked at the end of the next T2 time period and flip-flop TTKAR0 is set. Signal TTKAR0- going false clocks binary counter flip-flops TTKBR0 and TTKBR1 and sets both of them. In turn, signal TTKBR1- going false clocks and sets flip-flops TTKBR2 and TTKBR3. The binary counter flip-flops are thus set in pairs until all are set. The propagation delay of approximately 200 ns through the counter is insignificant compared to the shift clock period of approximately 9.2 ms and can be ignored. Signal TTKBR9- becomes false when the last pair of flip-flops is set and clocks the sequencer flip-flops directly. It also clocks flip-flops TTFKEN, TTFISF, and TTFINT via signal KKTTF and enters into the shift clock logic. The sequence of operation in the character input operation is shown in figure 4-34.

4-706. The sequencer is advanced to the "start" configuration on the first negative transition of signal TTKBR9-. After 4608 machine cycles, signal TTKBR9- becomes true and enables flip-flop TTFKK1 to be set at the end of the next time period T2. Signal TTFKK1 remains true for one machine cycle, but does not cause signal KKTTSFT to become true because signal TTFISF- is still false. Flip-flop TTFKK2 is set at the same time that flip-flop TTFKK1 is reset and prevents more than one clock pulse from being generated by flip-flop TTFKK1 each time signal TTKBR9- becomes true.

4-707. The start pulse is not loaded into the assembly register because the clock pulse (TTFKK1) that occurs approximately half way through the start pulse does not generate a shift clock pulse (KKTTSFT). The start pulse carries no intelligence (other than that transmission of a character has started) and is not transmitted from the controller to the CPU, so there is no necessity for placing it into the assembly register.

4-708. The next pulse transmitted is the first (least-significant) bit of the eight-bit ASCII character code. This bit may be marking (current or 1) or spacing (no current or 0). In the example shown in figure 4-34, the character shown is an alternating series of 1's and 0's to illustrate the separate pulses. (This is the ASCII code for the letter U. Bit 8, the



CODE PULSE (TTDIN)	SEQUENCER STATES				CLOCK PULSE (TTKBR9-)
	TTR0	TTR1	TTR2	TTR3	
$STOP_0$	0	0	0	0	0
START	1	0	0	1	1
1	1	0	1	0	2
2	1	0	1	1	3
3	1	1	0	0	4
4	1	1	0	1	5
5	1	1	1	0	6
6	1	1	1	1	7
7	1	0	0	0	8
8	0	0	0	1	9
$STOP_1$	0	0	1	0	10
$STOP_2$	0	0	1	1	11
$STOP_0$	0	0	0	0	12

Figure 4-34. Character Input Operation Timing Diagram

parity bit, is shown as 0 for purposes of illustration. However, bit 8 is always 1 in actual characters in the 704 Processor system.)

4-709. Input shift flip-flop TTFISF is reset at the end of 9216 machine cycles (approximately at the end of the start pulse) and enables shift clock signal KKTTSFT. The eight bits of the character code are loaded into assembly register flip-flop TTAR8 on successive shift clock pulses (TTDIN-TTFIN or TTDIN TTFIN). Notice that the bits are inverted when they are loaded into the assembly register. Bits already placed into the register are shifted to the next flip-flop of the register each time a new bit is loaded into flip-flop TTAR8. When bit 8 is loaded into flip-flop TTAR8, bit 1 is shifted into flip-flop TTAR1, and all intermediate bits are shifted into their corresponding flip-flops.

4-710. The sequence counter is clocked by signal TTKBR9- each 9216 machine cycles and is advanced to the next state approximately at the end of each pulse received from the teletypewriter set. (The sequencer states during each input pulse are shown in figure 4-34.) During the bit 8 pulse, the setting of flip-flop TTFISF and the resetting of flip-flop TTFINT are enabled (TTR0- TTR2-TTR3). Bit 8 is loaded into the assembly register approximately half way through the pulse, and flip-flops TTFISF and TTFINT are set and reset respectively approximately at the end of the pulse. Setting flip-flop TTFISF inhibits shift clock signal KKTTSFT so that the contents of the assembly register cannot be altered after the character is placed into the register. Resetting flip-flop TTFINT places an interrupt onto the interrupt level assigned to signify that the controller is ready to transmit a character to the CPU.

4-711. Two stop pulses, both of which are marking (1), follow bit 8 of the character code. The stop pulses have no significance in the controller, and the interrupt is sent to the CPU approximately at the start of the first stop pulse in order to allow as much time as possible for the character to be transferred to the CPU before the next character is transmitted from the teletypewriter set. However, the stop pulses are significant in the teletypewriter set receive circuit if the controller is operating in the keyboard mode. Inhibiting the shift clock pulses and interrupting the CPU have no effect on signal TTDOT, and both stop pulses are returned to the receive circuit in this mode.

4-712. The sequencer is clocked approximately at the end of both clock pulses and advances to state 0 following the second stop pulse. The resetting of clock enable flip-flop TTFKEN is enabled during the second stop pulse (TTR0- TTR2 TTR3), and the flip-flop is reset at the same time that the sequencer advances to state 0. This directly resets the clock counters and halts operation of the controller. (The direct reset of the sequencer flip-flops and the direct set of flip-flop TTFISF maintain conditions that already exist.)

4-713. The error in the controller clock period results in the character input time being 101.376 ms rather than the nominal 100 ms required to transmit the character from the teletypewriter set. In intermittent character input operations, such as from the keyboard, the difference in character times is insignificant. However, in continuous input operations from paper tape, the cumulative error would result in loss of synchronization between the teletypewriter set and the controller after a few characters. To prevent this, clock enable flip-flop TTFKEN is directly reset during the first time period T2 following the receipt of a new start pulse, if the sequencer is still in the second stop pulse state (TTR0- TTR2 TTR3 TTT2A TTDIN-).

4-714. Directly resetting flip-flop TTFKEN causes the sequencer and clock counters to be directly reset, then flip-flop TTFKEN is directly set during the next time period T2 to start the next character input operation. The loss of one machine cycle to directly reset and set flip-flop TTFKEN is insignificant (compared to the controller clock period of 9216 machine cycles), and synchronization is effectively restored at the beginning of each start pulse.

4-715. When the interrupt is serviced by the CPU, the character in the assembly register is transferred to the CPU accumulator register by a DIN instruction. Signals TTSAID and TTSAIOD become true for one machine cycle during phase C of the DIN instruction. Signal TTSAID gates the character onto data input lines DIN08- through DIN15-, and

signal TTSAIOD directly sets interrupt flip-flop TTFINT to terminate the interrupt. The character is loaded into the CPU accumulator register at the end of the machine cycle.

4-716. Character Output Operation

4-717. When a character is transmitted from the CPU to the teletypewriter set, the controller may already be in the print/punch mode from a previous operation, or the controller may be placed into the print/punch mode by the same DOT instruction that transfers the character from the CPU accumulator register to the controller assembly register. Operation of the controller is the same in either case.

4-718. The interrupt signifying that the controller is ready to accept a new character is sent to the CPU as soon as the eighth code bit of the current character is transmitted to the teletypewriter set. If the interrupt is serviced promptly, the new character will be loaded into the assembly register near the start of the first stop pulse of the previous character. Operation of the controller does depend on whether transmission of a previous character to the teletypewriter set is still in progress or has been completed when a new character is loaded into the accumulator register from the CPU.

4-719. When the DOT instruction is executed to transfer the character, bit 13 of the function code is true and signal TTARLD becomes true during phase C of the instruction (TTADDC TTDOSB TTAD13). Signal TTSAIOD also becomes true during this phase (TTADDC TTDOSB) and enables the inputs of mode flip-flops TTFOUT and TTFIN and directly sets interrupt flip-flop TTFINT if it is reset. (Setting flip-flop TTFINT terminates a previous interrupt.)

4-720. At the end of time period T0, the states of bits 14 and 15 of the function code are copied into flip-flops TTFOUT and TTFIN, respectively. Flip-flop TTFOUT is set, and flip-flop TTFIN is reset in the print/punch mode. (If the controller is already in the print/punch mode, the states of the mode flip-flops are not altered.) Data-out-waiting flip-flop TTFDOW is also set by signal TTARLD at the end of time period T0. Setting this flip-flop initiates transmission of the character to the teletypewriter set in the present machine cycle, if transfer of a previous character is not still in progress. If the stop pulses of the previous character are being transmitted, flip-flop TTFDOW remains set until after the second stop pulse is transmitted, then initiates transmission of the new character.

4-721. During time period T2, signal TTARLD directly resets assembly register flip-flops TTAR1 — TTAR8 via signal TTARDR-. This places 0's into all of the code bits. If the stop pulses of a previous character are not being transmitted, the sequencer is in state 0, and register flip-flop TTAR0 is directly reset during this time period. If stop pulses are being transmitted, flip-flop TTAR0 is directly reset as soon as the sequencer enters state 0, indicating that transmission of the previous character is completed. In either case, flip-flop TTAR0 is directly reset to provide the start pulse (0) before the new character is transmitted to the teletypewriter set.

4-722. If the sequencer is in state 0, clock enable flip-flop TTFKEN is directly set during time period T2 and enables the clock counters and the sequencer (TTR0- TTR2- TTR3- TTT2 TTFDOW). If stop pulses are being transmitted, flip-flop TTFKEN is still set and is reset at the end of the second stop pulse. It is then directly set during the next time period T2 to start transmission of the new character.

4-723. During time period T4 of the DIO phase, delayed assembly register load signal TTARDL gates the character code bits into the direct set inputs of the assembly register (TTARLD TTT4). The inverted data output lines (DOT08- through DOT15-) of the data output bus are applied directly to the gates without being inverted. This results in the register flip-flops being directly set by 1 code bits and remaining reset for 0 code bits.

4-724. At the end of time period T2, the divide-by-nine clock counter (TTAR0 — TTAR4) is clocked. Assuming that flip-flop TTFKEN has been reset and has cleared the clock counters and is now set to enable transmission of the new character, flip-flop TTKAR0 is set the first time the counter

is clocked. Signal TTKAR0- going false clocks binary counter flip-flops TTKBR0 and TTKBR1 and sets both of them. In turn, signal TTKBR1- going false clocks and sets flip-flops TTKBR2 and TTKBR3. The binary counter flip-flops are thus set in pairs until all are set. The propagation delay of approximately 200 ns through the counter is insignificant compared to the shift clock period of approximately 9.2 ms and can be ignored. Signal TTKBR9- becomes false when the last pair of flip-flops is set and clocks the sequencer flip-flops directly. It also clocks flip-flops TTFKEN, TTFISF, and TTFINT via signal KKTTF and enters into the shift clock logic. The sequence of operation in the character output operation is shown in figure 4-35.

4-725. The sequencer is advanced to the "start" configuration on the first negative transition of signal TTKBR9-. This makes signal TTDOENB true (TTR0 + TTR2- TTR3) and gates the start pulse from flip-flop TTAR0 onto data output line TTDOT to the teletypewriter set (TTAR0- TTDOENB TTFIN- TTFOUT). Flip-flop TTFDOW is reset via signal TTDC9 by the first CPU clock pulse after the sequencer enters the start state (TTR0 TTR1- TTR2- TTR3) and enables flip-flop TTFINT to be reset near the end of the character output operation.

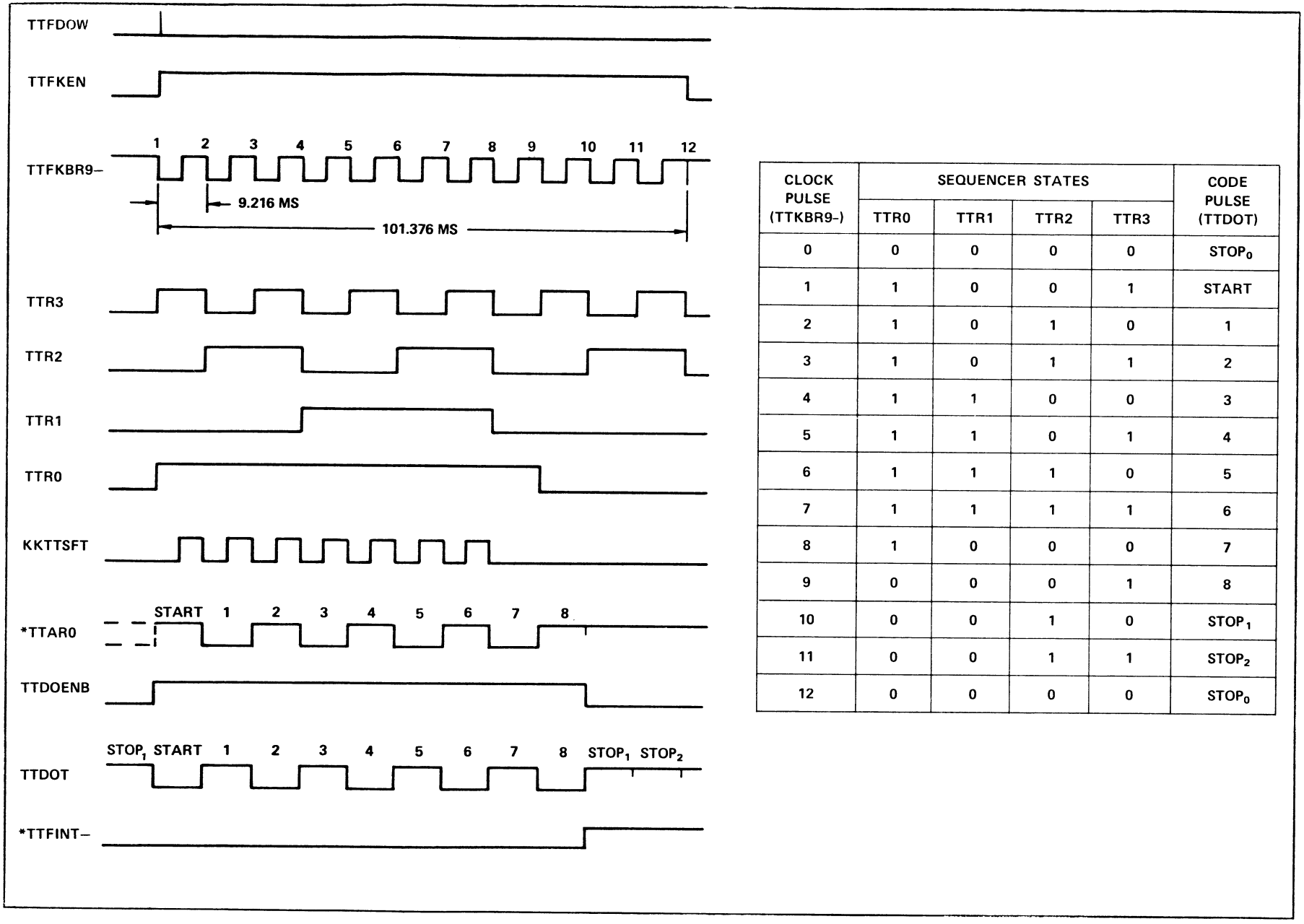
4-726. Shift clock signal KKTTSFT is false before the sequencer enters the start state because signal TTR0 is false (TTFIN- TTR0 TTKBR9-) and remains false when the start state is entered because signal TTRBR9- is now false. During the time that flip-flop TTR0 is set, signal KKTTSFT reflects the state of signal TTRBR9-. After 4608 machine cycles, both signals become true and remain true for an additional 4608 machine cycles. Both signals become false at the end of 9216 machine cycles: signal KKTTSFT shifts the contents of the assembly register one position toward flip-flop TTAR0, and signal TTKBR9- advances the sequencer to the next state. Flip-flop TTFISF is also reset at this time, but has no function in the character output operation.

4-727. The start pulse transmitted to the teletypewriter set is always spacing (no current or 0). When the contents of the assembly register are shifted, the first (least-significant) bit of the eight bit ASCII character code is shifted into flip-flop TTAR0 and is transmitted to the teletypewriter set. This bit may be marking (current or 1) or spacing (no current or 0). In the example shown in figure 4-35, the character shown is an alternating series of 1's and 0's to illustrate the separate pulses. This is the ASCII code for the letter U. Bit 8 (the parity bit) is shown as 0 for purposes of illustration. However, the bit 8 is always 1 in actual characters in the 704 Processor system.

4-728. The remaining bits of the character code are transmitted to the teletypewriter set on successive shift clock pulses. Since the period of the shift clock is 9.216 ms rather than 9.09 ms, there is a cumulative error in the occurrence of the code bits relative to the nominal bits times of the teletypewriter set. Bit 8 of the character code is transmitted approximately 1 ms after the start of the nominal bit 8 time. However, the teletypewriter set samples only a small segment near the center of each pulse to allow for minor timing errors between sets, so the discrepancy in the timing of the pulses sent from the controller is well within acceptable limits.

4-729. The total transmission time for the 11-unit code is 101.376 ms rather than the nominal 100-ms character time of the teletypewriter set. In character input operations, it is necessary to provide means for cutting short the last stop pulse to avoid losing synchronization with incoming characters. However, there is no need to shorten the character transmission time in output operations because the teletypewriter set finishes its cycle first and waits for the next character: synchronization is reestablished at the start of each character.

4-730. When bit 8 is shifted into flip-flop TTAR0, the sequencer is advanced to the bit 8 state: flip-flop TTR0 is reset and remains reset for the remainder of the output operation. Signal TTR0 being false holds shift clock signal KKTTSFT false so that no more shift clock pulses are applied to the assembly register after the last code bit is shifted into flip-flop TTAR0. This allows a new character to be loaded into the assembly register during the stop pulses without being prematurely shifted.



CLOCK PULSE (TTKBR9–)	SEQUENCER STATES				CODE PULSE (TTDOT)
	TTR0	TTR1	TTR2	TTR3	
0	0	0	0	0	$STOP_0$
1	1	0	0	1	START
2	1	0	1	0	1
3	1	0	1	1	2
4	1	1	0	0	3
5	1	1	0	1	4
6	1	1	1	0	5
7	1	1	1	1	6
8	1	0	0	0	7
9	0	0	0	1	8
10	0	0	1	0	$STOP_1$
11	0	0	1	1	$STOP_2$
12	0	0	0	0	$STOP_0$

Figure 4-35. Character Output Operation Timing Diagram

4-731. At the end of the bit 8 code pulse, flip-flop TTFISF is set, interrupt flip-flop TTFINT is reset (TTR0- TTR2- TTR3), and the sequencer advances to the first stop pulse state. Resetting flip-flop TTFINT sends an interrupt to the CPU, signifying that the assembly register is ready to accept a new character. Signal TTDOENB becomes false when the first stop state is entered and holds signal TTDOT true until the next start pulse occurs, so a new character may be loaded into the assembly register without affecting transmission of the stop pulses of the present character.

4-732. Two stop pulses, both of which are marking (1), are transmitted to the teletypewriter set following bit 8 of the character code. The sequencer is clocked at the end of both clock pulses and advances to state 0 at the end of the second stop pulse. Clock enable flip-flop TTFKEN is reset at the same time (TTR0- TTR2 TTR3) and directly resets the clock counters via signal TTKRDR to halt operation of the controller. The direct reset of the sequencer flip-flops and the direct set of flip-flop TTFISF maintain conditions that already exist.

4-733. COMPUTER POWER

4-734. The 704 Processor contains its own internal dc power supply. The power supply is a self-contained, chassis-mounted unit with multiple outputs that deliver all of the dc power for the CPU, up to four 4096-word memory modules, and the worst-case configuration of optional circuit cards that can be accommodated within the cabinet. Power is distributed at +3, +5, -5, +6, +12, and +24 volts from this supply.

4-735. Processors intended for domestic use are equipped with power supplies operating from 110-120-volt rms, 60-Hz, single phase power lines. If the processor is to be operated from 50-Hz lines, an alternate 110/220/240/250-volt rms power supply will be installed. Both have standard NEMA 3-wire grounded plugs on their line cords.

4-736. If more than four memory modules (16,384 words) are used, the additional module cards are installed in a second equipment cabinet. This cabinet is equipped with its own dc power supply (identical to the main cabinet power supply) and is capable of handling four additional memory modules as well as priority interrupt expansion circuit cards, etc. Main and auxiliary power supplies are controlled by the same ac control circuits located within the main cabinet.

4-737. As an option, the processor may be equipped with a power failsafe circuit card that monitors the ac line voltage, interrupts data processing to store operands and machine status, and shuts down the system when ac power failure is detected. These circuits are contained on a single circuit card, along with (or without) the hardware bootstrap option.

4-738. AC Control Circuits

4-739. The ac control circuits in the main cabinet transfer primary power to the main power supply and blower and, in effect, control power-on and power-off operations in any auxiliary cabinet power supplies as well. These control circuits may be seen in drawing 545435, the wiring diagram for the 704 Processor cabinet.

4-740. Primary power is routed from the power lines through terminal boards TB1 and TB2 and fuse F1 on the power supply chassis to the ON and OFF switches for processor power on-off control. Pressing the ON switch closes one set of normally-open contacts, energizing the coils of relays K1 and K2 which are connected together in parallel. Pin 4 and pin 7 contacts of relay K1 represent a latching switch that keeps the relays energized after the ON switch is released. Another set of ON switch contacts closes when the switch is pressed and grounds the RESET- line going to the Memory Control card master reset logic. Thus, the CPU is reset each time power is turned on.

4-741. Relay K2 has heavy-duty contacts which close when the relay is activated and transfer power to the main dc power supply, the rear panel fan, and the primary of step-down transformer T1. (This transformer is optional and is installed only in 704 Processors with the power failsafe feature.) Another set of normally-open contacts in the K1 relay close at the same time and may be used to control the transfer of primary power to a power

supply located in an auxiliary equipment cabinet. Notice that this REMOTE CONTROL circuit does not distribute primary power from the main cabinet but only provides a relay closure. With primary power distributed to the main and auxiliary power supplies (if any), the processor is turned on.

4-742. Pressing the OFF switch opens a normally-closed set of contacts which is in series with the K1 relay latching contacts. This breaks the circuit energizing the coils of both relays, allowing their contacts to open. At the same time, a second set of OFF switch contacts places a ground on the RESET- line, generating a master reset while power shuts down. This halts data processing and inhibits memory access during the shutdown interval.

4-743. DC Distribution

4-744. The wiring diagram for the 704 Processor main cabinet, drawing 545435, shows the major distribution of dc voltages within the cabinet. Terminal boards TB2 and TB3 are at the rear of the power supply chassis and handle the power supply outputs. The current density of the +5-volt logic level output is handled by three terminal board TB2 outputs, two of which are distributed to the standard plug-in circuit cards through the mother board. The other +5-volt line goes to the front panel assembly to be used primarily in front panel switching logic. Power at -5, +12, and +24 volts is distributed solely through the mother board.

4-745. Six-volt power, handled through power supply terminal board TB3, is used solely to light indicator lamps on the front panel assembly and on the teletypewriter set. Lamp drivers for these indicators control the lamps by switching their return lines. Terminal board TB3 is also the output for +3-volt power used on the DIO and DMA buses.

4-746. Pressing the OFF switch opens a normally-closed set of contacts that is in series with the K1 relay latching contacts. This breaks the circuit energizing the relay coils and allows them to open. Simultaneously, a second set of OFF switch contacts places a ground on the RESET- line, generating a master reset while the switch is held down. This halts data processing and inhibits memory access during power shutdown.

4-747. There are times when it is desirable for processor power to remain on at all times, with the front panel power control switches disabled. This is easily done by jumpering terminal board TB5 pin 8 to pin 9 which connects the relay coils directly across the ac power lines, bypassing the power ON and OFF switches. The processor will be turned on as long as the line cord is plugged in and fuse F1 is good. If this mode of operation is employed with a processor equipped with the power failsafe circuits and the power fails, the processor will be restarted automatically when power is restored.

4-748. Power Supply

4-749. The 704 Processor power supply is a single chassis assembly which supplies all dc power for the cabinet at voltages of +3, +5, -5, +6, +12, and +24 volts. It uses saturable, constant-voltage transformers to maintain regulation for line fluctuations of ±10 percent or less. All supply outputs except the +6-volt output are shunt regulated for load variations. The saturable nature of the power supply transformers offers sufficient overload protection in most cases. But in addition, the -5 and +6-volt supplies are further protected by self-resetting circuit breakers.

4-750. DC power from the power supply is distributed from power supply terminal boards TB2 and TB3 to the cabinet mother board and other active assemblies directly by inter-chassis cabling. The distribution of this power and the routing of ac control signals through the power supply are shown in drawing 545435. A complete schematic diagram and theory description of the power supply will be found in the power supply manufacturer's manual that is shipped with the processor documentation.

4-751. POWER FAILSAFE OPTION

4-752. (Information is not available at this time.)

4-753. AUTOMATIC BOOTSTRAP OPTION

4-754. (Information is not available at this time.)

Section V
MAINTENANCE

5-1. GENERAL

5-2. This section contains instructions for checkout, adjustment, troubleshooting, and repair of the 704 Processor. Normally, diagnostic programs are used for system checkout that provide error printout and fault isolation information. These programs and instructions for their use are given in the *704 Sensor Diagnostic Manual.* Instructions covered in this section are limited to manual troubleshooting, adjustments, and general repair procedures.

5-3. Fault isolation of the diagnostic program is to the circuit card level. This is in keeping with the maintenance concept of replacing a faulty circuit card with a spare card on hand or obtained through your field service representative and sending the defective card back to the factory for repair. The repair of circuit cards by the user, particularly memory module cards, is not recommended, since many contain components selected to Raytheon specifications and there is a good chance of doing erreparable damage to the circuit foil during soldering operations.

CAUTION

Attempted unauthorized repairs during the warranty period do not constitute "ordinary use" and may void your warranty. Consult with the field service representative.

5-4. SPECIAL TOOLS

5-5. Special tools required for processor troubleshooting and repair are listed in table 5-1. Users intending to do card replacement level maintenance only will need only the special Card Extractor, Raytheon Computer Part No. 545219.

5-6. TEST EQUIPMENT

5-7. Test equipment recommended for full maintenance of the 704 Processor is listed in table 5-2. Other available equipment may be substituted, provided its performance characteristics (accuracy, rise time, sweep rate, etc) equal or exceed those of the equipment specified. Special probe adapters will be needed to connect the oscilloscope probes to the wire-wrap pigtails of the circuit card connectors. These adapters must be fabricated as shown in figure 5-1.

Note

To avoid excessive noise pickup, the lead lengths shown in figure 5-1 must not be exceeded.

5-8. MAINTENANCE PROCEDURES

5-9. Routine Maintenance

5-10. Although most of the electromechanical peripheral devices in a 704 Processor System require periodic maintenance (cleaning, lubrication, and adjustment; refer to their technical manuals for schedules and procedures), the processor itself does not. As long as it is operating properly, it should not be tampered with in any way. This does not mean that the exterior of the cabinet and the front panel cannot be wiped down occasionally to maintain good appearance.

5-11. Whenever the processor is down and the cabinet is open for troubleshooting and repair,

Table 5-1. Special Tools

Description	Use	Raytheon Computer Part No.
704 Extractor-Extender Kit (consists of the following items which may be ordered separately):	User maintenance	545251
— Card Extractor	Circuit card removal	545219
— Extender Card	In-system checkout of card circuits	394596
— Extender Cables (2 reqd)	In-system checkout of card circuits	545237
— Pin Locator Mask	Quick identification of card connector pins	545459
Wire-Wrap Tool; Gardner-Denver Co., Quincy, Ill; model 14XA2	Installation of card connector wiring	531311-101
Wire-Wrap Bit; Gardner-Denver Co., Quincy, Ill; part no. 507063	For use with Wire-Wrap tool	531311-302
Wire-Wrap Sleeve; Gardner-Denver Co., Quincy, Ill; part no. 500350	For use with Wire-Wrap tool	531311-202
Left-Hand Unwrapping Tool; Gardner-Denver Co., Quincy, Ill; part no. 505084	Removal of card connector wiring	531311-401

check for heavy accumulations of dust inside that might restrict airflow or impair the dissipation of heat. In extreme cases, it may be necessary to remove all circuit cards so that their surfaces and the interior of the cabinet can be vacuumed out. Be very careful not to disturb the wiring, and replace the circuit cards back in their original locations. This type of thorough cleaning should not be required more than once or twice during the life of the instrument, under normal circumstances.

5-12. Fault Isolation

5-13. It is not possible to give a universal, step-by-step troubleshooting procedure that would be appropriate to all possible troubles. For example, it is considered good practice to check that all dc voltages are present and in tolerance (eliminate the power system as a source of trouble) if the trouble is broad and ill defined. One might be tempted to make it a general rule to always check the dc voltages as a first step, but this would be a waste of time if the trouble could be specifically defined as, say, bit 6 drops out every time a memory-read operation is performed. In short, nothing can take the place of common sense, a good understanding of how the machine works, and cumulative experience.

Table 5-2. Test Equipment

Equipment	Use
DC-50MHz Oscilloscope, Tektronix Type 547	Signal tracing, checking timing of clock and strobe pulses, waveform and signal level displays, etc.
Dual-Trace Plug-In Unit, Tektronix Type 1A2	Allows display of two signals for comparison.
DC-50MHz 10X Voltage Probes, Tektronix Type P6010 (2 reqd)	Oscilloscope probe applicable to subminiature circuit testing.
Oscilloscope probe adapters (Must be fabricated; see figure 5-1.)	Adapt oscilloscope probe for connection to pins on wire-wrap connectors and IC test clip.
Integrated Circuit Test Clip, A P Inc. part no. 912050 (2 reqd)	Clip over IC module lugs for test lead connection.
Volt-Ohm-Milliammeter, Simpson Model 260	Ac and dc voltage measurements; wiring continuity checks.

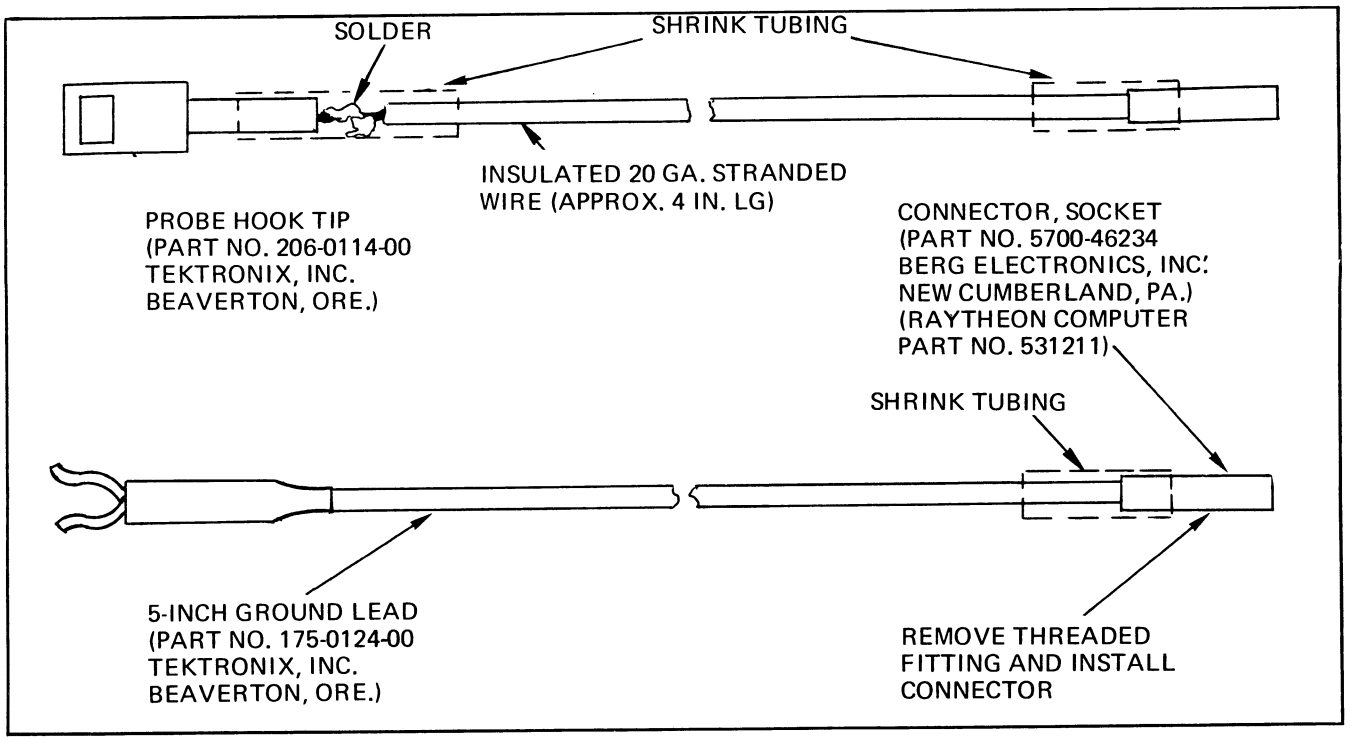


Figure 5-1. Oscilloscope Probe Adapters

5-14. Efficient troubleshooting is a three-step operation: (1) define the trouble as minutely as possible from its operational symptoms so that the number of possible causes is reduced to a manageable few; (2) figure out the possible causes of the trouble identified, and arrange them by degree of probability, most likely one first; and (3) eliminate each possible cause, one by one, until the trouble is found.

5-15. Much valuable information can only come from the machine operator. Don't let him get away with merely reporting his own opinion of the trouble (e.g., the memory isn't working). Find out exactly what he was doing operationally when the failure occurred. At what point was the program? How did he know he had a problem? What did he do to try to correct the situation? It might even help in the diagnostic process to try to duplicate the conditions under which failure occurred or was first noticed, using the single-step or command mode to get more information.

5-16. For those inexperienced in digital equipment troubleshooting, a few general assumptions are considered good practice. Where the possible source of trouble could be the equipment (hardware) or the program being run (software), consider the software to be the more probable cause and check it out first. If the faulty operation involves an electromechanical peripheral device and the trouble could be caused by the device, its controller, or by the processor, consider the device as being the most probable cause and the processor as the least probable cause.

5-17. Normally, fault isolation by spares replacement is discouraged in most cases, particularly where there is a general inoperable condition that might suggest catastrophic failure of many circuits. In such a case, it is better to try to point to the defective card through the running of the diagnostic programs. Indiscrimate card replacement might cause the replacement to be overloaded by another, undetected defective circuit.

5-18. There are two cases where the practice of "card swapping" is a most valuable troubleshooting technique. First, all four Arithmetic Cards in the processor are identical and may be interchanged without adverse effects. If a certain bit-oriented problem "follows" an Arithmetic Card that is "swapped" with another, some circuit on the card is defective. The same technique can be used to verify the failure of a Memory Module card in systems having more than 4096 words of memory. If the faulty location or locations in memory follow the card after swapping, the memory module is faulty rather than timing control, addressing, or memory data buffering circuits common to all.

5-19. Diagnostic Routines

5-20. General failures within the processor whereby the symptoms do not point to one or two easily checked possible causes, are usually more easily diagnosed by loading and running the 704 Sensor Diagnostic programs. These diagnostics will isolate the fault to the circuit card level. A manual accompanies the program that contains a general description of system checkout and troubleshooting procedures. It also includes instructions for performing Sensor bootstrap loading and procedures for running each diagnostic program.

5-21. Oscilloscope Measurements

5-22. When making oscilloscope measurements on printed circuit cards and connectors within the processor, special adapters listed in table 5-2 and shown in figure 5-1 must be fitted to the probes. All measurements must be made with respect to dc ground, not frame ground. The dc ground is completely isolated from the frame, and correct displays cannot be obtained by connecting the oscilloscope ground lead to the frame. The connection to dc ground may be made by connecting the probe ground lead to pin 7 of any logic element or to grounded pins (3, 4, 69, 70) on any circuit card connector.

CAUTION

After connecting ground lead to oscilloscope probe, wrap insulating tape around probe body and ground lead clip so that no bare metal is exposed. This is necessary to ensure that signals or the dc power will not be shorted to ground

when the probe is laid against the wire-wrap pigtails.

5-23. Extender Card and Cables

5-24. A card extender and extender cables permit circuit cards within the processor to be operated in such a position that their logic elements are accessible to an oscilloscope probe. These items, listed in table 5-1, are required tools for those users who perform circuit card troubleshooting and repair.

5-25. To extend a circuit card for testing access, proceed as follows:

a. Halt processor and turn off power. Circuit cards should never be removed or installed with processor power turned on.

b. Disconnect any wiring harness plug or plugs connected to front edge of circuit card.

c. Using special card extractor (part no. 545219) inserted into holes at front corners of circuit card, disconnect and remove card by pulling straight out.

d. Insert card extender (part no. 394596) into vacated top and bottom guides so that front edge card connectors are on component (right-hand) side, slide in, and press into rear card connectors.

e. Install circuit card to be tested onto extended card with component side to the right. Use extender cable (two are required for Sequence Counter card) to reconnect between the front panel interconnecting cable assembly and the circuit card front edge connector, if any.

f. To reinstall circuit card after testing, turn off power, disconnect extender cables, remove circuit card from card extender with an edgeways, up-and-down rocking motion to loosen from connectors, remove card extender separately with card extractor. Components must face to right when circuit card is reinstalled (card connectors will not align if card is put in backwards).

5-26. Circuit Card Locations

5-27. There are slot locations for 23 circuit cards within the 704 Processor cabinet. Pairs of printed circuit card connectors are installed in the first 17 of these locations and wired for ten basic configuration circuit cards plus seven standard option circuit cards. The remaining six card locations are unassigned and can be used for priority interrupt expansion plus any other special logic cards that may be peculiar to the system.

5-28. The circuit card slots are numbered from 1 to 23, starting at the left-hand side of the cabinet when viewed from the front. These slot numbers identify the exact card locations for interconnecting wire listing and can be seen screened on the rear guide rails when the rear panel is removed.

5-29. Circuit cards are further identified as to type by a three- or four-letter mnemonic contraction that is appropriate to the main function of the card. The mnemonic code names for all standard circuit cards will be found in table 5-3. These are used to identify card locations by card type and are stacked immediately above the upper guide for each location. Table 5-3 also identifies the correct circuit card assigned to each slot.

5-30. Card Connector Locations and Pin Numbers

5-31. There are two 72-pin circuit card connectors, one above the other, at the rear of each card slot. These are named for the card slot number plus the letter A or B which identify them by location. The letter A designates a top connector and the letter B designates a bottom connector. Thus the circuit card connector named 09B in a wire list is the bottom connector for card slot 9.

5-32. Circuit card connector pins are numbered 1 to 72, left to right and top to bottom, starting at the upper left-hand pin (1) and ending at the lower right-hand pin (72). So when viewed from inside the cabinet, all left-hand side pins are odd numbered (1, 3, 5, 7, etc.) and all right-hand side pins are even numbered. Naturally, the pins are reversed when viewed with the back panel removed from the wiring side. But pins 1 and 2 at the top and pins 71 and 72 at the bottom of each connector

Table 5-3. Circuit Card Location Chart

Slot	Card Type (CODE)
1	Adder Flip-Flop Card (ADF)
2	Sequence Counter Card (SCDC)
3	Instruction Card (INR)
4*	Multiply-Divide Card (M/D)
5	Arithmetic Card #1 (ARI; for bits 0 — 3)
6	Arithmetic Card #2 (ARI; for bits 4 — 7)
7	Arithmetic Card #3 (ARI; for bits 8 — 11)
8	Arithmetic Card #4 (ARI; for bits 12 — 15)
9	Memory Control Card (MEM)
10	Memory Module 0 (MAG; basic 4K)
11*	Memory Module 1 (MAG; to 8K)
12*	Memory Module 2 (MAG; to 12K)
13*	Memory Module 3 (MAG; to 16K)
14*	Direct Memory Access/Memory Parity Check (DMA)
15*	Priority Interrupt Card (INT; to 8 levels)
16	Teletypewriter Controller Card (TTY)
17*	Power Failsafe/Automatic Bootstrap (PFS)
18†	
19†	
20†	
21†	
22†	
23†	

* Circuit card is optional standard and may not be installed.
† Unassigned card location. Write in card name, when used.

are identified by circuit card etch. For even quicker and more positive pin identification than by counting, a pin locator mask, part no. 545459, can be slipped over the wire-wrap pigtails. See table 5-1 for details.

5-33. Eight 44-pin circuit card connectors plug into the front edges of some of the circuit cards as part of the wiring harness that interconnects with the front panel controls and indicators. These are designated and stamped P1 through P8. Connector P1 plugs into the left-hand most circuit card in slot 1, and the others are plugged-in in numerical order from left to right. Because of the wire length restrictions imposed by the wiring harness, it is not likely that these plugs will be accidentally connected to the wrong circuit card.

5-34. Logic Element Location and Type Designations

5-35. Integrated circuit logic elements mounted on the circuit cards are assigned reference designations by their location on the board and an eight-by-eight coordinate system of columns and rows. Looking at the component side of a circuit card with the main connector edge to the right, rows are laid out from top to bottom and named 1 through 8, in that order. Columns are laid out from right to left and are named A through H in the same order. A logic element identified by the designation 5B, for example, is to be found in row 5, column B of a particular circuit card which is identified either by its type or by its location. Not only is the logic element given this reference designation by location, but so are all of the curcuits within the element as well. To fully identify a particular circuit, such as a gate or a flip-flop, it is necessary to give the logic element reference designation plus one or more pin numbers for its particular input or output signals.

5-36. Logic element type designations refer to functional and electrical circuit characteristics without regard to application or physical location. For example, a certain type of logic element containing four 2-input AND gates has the arbitrary type designation of M01. Naturally, all logic elements on the same or other circuit cards that have the designation M01 are identical to one another. These type designations also appear in the logic diagrams and can be used to find detailed logic element circuit information given in Section VI.

5-37. Logic elements are of the 14-pin, flat pack variety which are soldered in place, and consequently, not subject to replacement by the user normally. But it is still useful to know how the logic elements are keyed for proper orientation and how the pin numbers are assigned for purposes of signal tracing. Figure 5-2 provides this information.

5-38. BASIC CHECKS AND ADJUSTMENTS

5-39. The basic checks and adjustments described in the paragraphs to follow should be used only when needed; that is, they should be performed only if some problem indicates the need rather than on any scheduled or arbitrary basis. Some procedures include detailed instructions based on the use of test equipment specified in table 5-2. These will have to be adapted accordingly if equivalent test equipment is used.

5-40. Power Supply Voltage Check

5-41. Erratic operation of the processor can result from one or more of the dc power supply voltages being out of tolerance. This is not a common occurrence, but it is worthwhile to check out computer power whenever overall reliability becomes degraded (e.g., a rash of memory parity errors occur). Ac and dc voltage values should be measured while the processor is turned on and running using a VTVM or VOM with a sensitivity of at least 20,000 ohms per volt. Oscilloscope measurement of ripple is satisfactory, provided that the instrument has been recently calibrated.

a. Remove four screws attaching rear panel to processor cabinet, and lay panel open on work bench.

b. Turn on processor, and using sensitive voltmeter, check voltage of ac primary power across power supply terminal board TB1, terminals 2 and 4. On domestic instruments, voltage value should be between 103 and 127 volts rms.

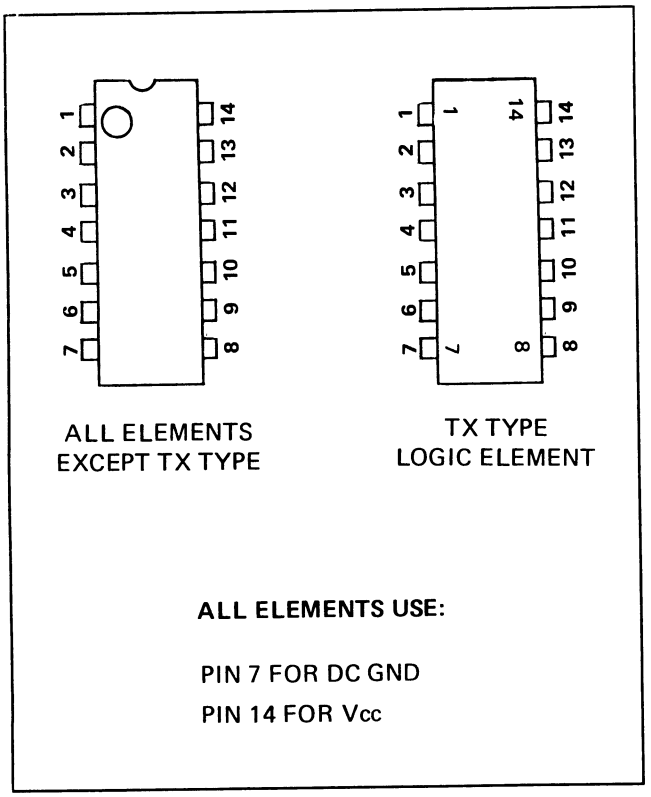


Figure 5-2. Logic Element Pin Number Assignments

Note

For a fully comprehensive test, processor should be connected to ac power through a variable autotransformer rated for at least 10 amperes so that power supply output voltages can be checked with input at both 103 volts and at 127 volts rms. This is not essential, however.

c. Load and run a looping test program that outputs to the teletypewriter set printer or paper tape punch.

d. While processor is running under this operational load, check power supply output voltages at the test points given in table 5-4.

e. Halt processor and recheck power supply output voltages at test points given in table 5-4. All voltages should still be within limits given in table.

Table 5-4. Power Supply Voltage Test Points

Supply Output	Test Points		Voltage Limits	Maximum Ripple (p-p)
	+	–		
+24V	TB2-8	TB3-3	24 ±0.5	250 mv
+12V	TB2-7	TB3-3	12 ±0.25	150 mv
+ 6V	TB3-4	TB3-3	6 ±0.6	750 mv
+ 5V	TB2-5	TB3-3	5 ±0.25	50 mv
+ 3V	TB3-6	TB3-3	3 ±0.3	50 mv
- 5V	TB3-3	TB2-6	5 ±0.1	50 mv

f. Turn off processor, replace power supply terminal board insulators, if removed, and close and secure rear panel.

5-42. Clock Distribution Check

5-43. Another possible source of intermittent troubles is an erratic clock driver. Usually, however, a failure in the clock distribution system will result in a positive malfunction; that is, it would hardly be classified as intermittent. Also, it is seldom necessary to check out the entire clock generation and distribution system point by point. Table 5-5 is a list of all easily accessible clock signals. Ease of access is dependent upon placing the Memory Control Card (MEM in slot 09) on a card extender.

5-44. Memory Cycle Timing Check

5-45. Trouble-free operation of the memory modules is dependent upon certain timing signals and the operations they control occurring within rather narrow limits. Performance may become erratic because of component aging that throws circuit delay or rise times out of tolerance. Figure 5-3 is a detailed timing diagram for a memory read-restore cycle, showing optimum timing relationships between major signals and allowable tolerances. The timing for a memory clear-write cycle is similar but less stringent and need not be checked if read-restore timing is acceptable, unless a total failure of the write function has occurred.

Table 5-5. System Clock Test Points

Signal	MEM Card Pin No.	Signal	MEM Card Pin No.
KEXT1-	B53	TIRC0	B19
		TIRC0-	B22
KKA	B55		
KKB	B57	TIRC1	B20
KKC	B59		
		TIRC2	B31
KK1	B58	TIRC2-	B46
KK2	B56		
KK3	B54	TIRC3-	B21
MT0-	A70	TIRC4	B17
MT2-	B09	TIRC3-	B18
MT4-	B62		
		TIRCA	B25

5-46. Power Failsafe Option Adjustment

5-47. (Information is not available at this time.)

5-48. REPAIR PROCEDURES

5-49. The removal and replacement of a defective circuit card is the approved method of repairing the 704 Processor. All attempts to isolate the faulty component on the card or to actually repair the circuit card are best left to the factory. Circuit card repair methods are not given here, and users insisting upon repairing their circuit cards do so at their own risk. Consult out local sales representative or field service office for additional information about repair policies and procedures.

5-50. Card Removal and Replacement

5-51. To remove and replace a circuit card:

a. Disconnect any wiring harness connector attached to circuit card front edge with a careful edgewise rocking motion while pulling straight out on connector.

b. Grip Card Extractor (545219) in one hand, and insert two pins on extractor arms into holes at top and bottom of circuit card front edge.

c. Pull on-axis with a slight up-and-down rocking motion edgewise to release circuit card from rear connectors. Once released, card is easily withdrawn.

d. To reinstall circuit card, orient component side to your right as you face cabinet, insert card into proper top and bottom guide rails (see top guide for card type), and slide card into slot until it enters rear connectors. Card extractor is not needed for this operation.

Note

Rear connectors are offset slightly from card center so that card cannot be installed backwards (components facing left).

e. Seat card into rear connectors by pressing evenly with both thumbs against top and bottom of circuit card front edge. Card is fully seated when its front edge is even with other cards.

f. Replace wiring harness connector or connectors disconnected in step a. Harness lacing will prevent connector from being installed incorrectly. To seat connector, use a slight rocking motion while pressing on.

5-52. Wiring Standards and Methods

5-53. With few exceptions connected with the power supply and front panel switches and indicators, all wiring connections in the processor are made by the wire-wrap method. A special single-conductor, wire-wrap wire is mechanically attached to a square post without solder by tightly wrapping the stripped wire around the post with a special wire-wrap gun. When repairing or modifying this wiring, observe the following:

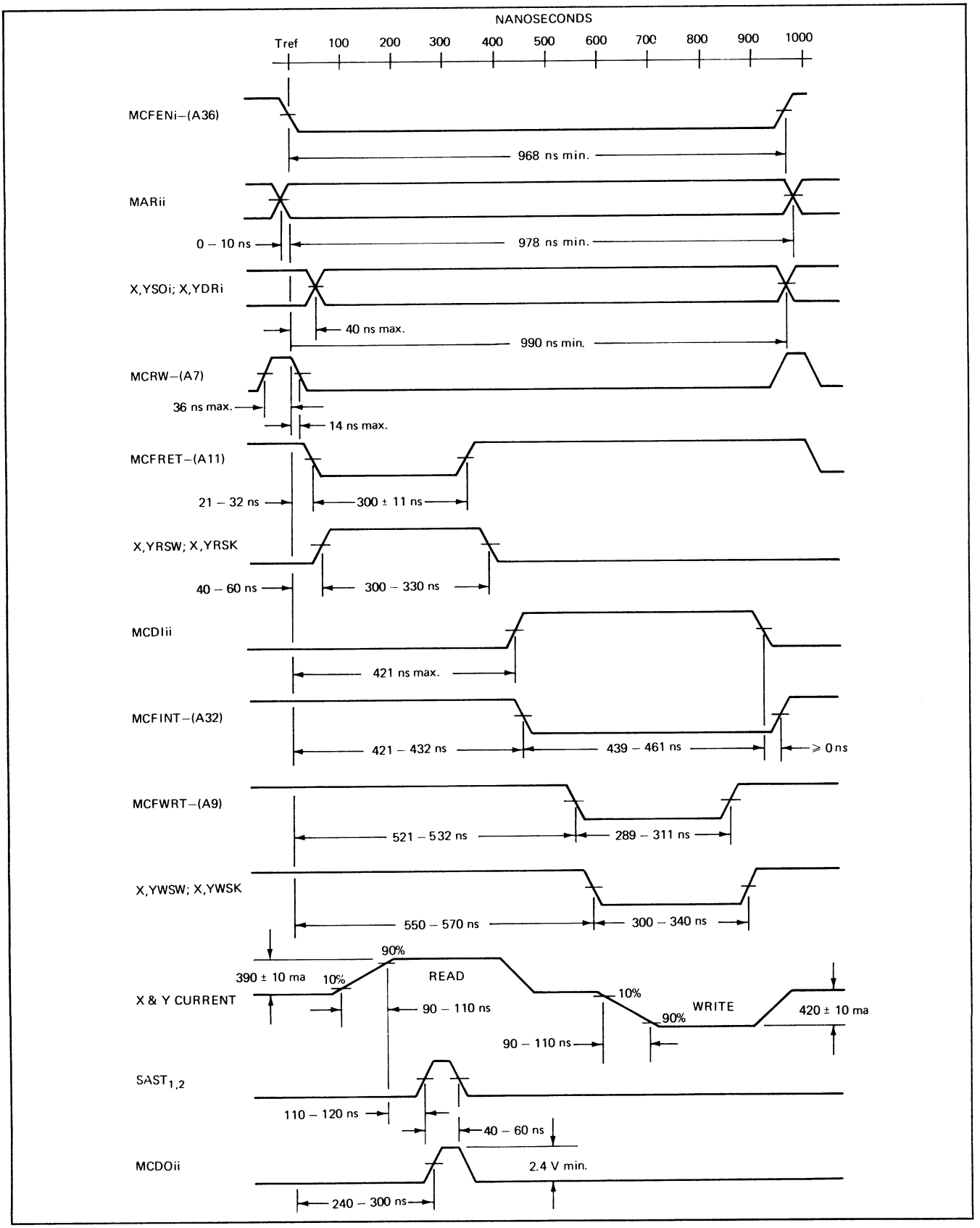


Figure 5-3. Memory Module Timing Specification

a. Use only white, No. 30 AWG, Kynar insulated, wire-wrap wire (Type IX, Brand-Rex Division, Americal ENKA Corp., Willamantic, Conn. or equivalent; Raytheon Computer Spec. No. 531176-309).

b. Strip wire ends 1-1/8 in. Nicked, scraped, or bent wires will not wrap correctly and must not be used.

c. When removing wire-wrap connections, use unwrapping tool specified in table 5-1. Do not reuse wires that have been unwrapped.

d. Use wire-wrap gun, bit, and sleeve specified in table 5-1 to make wire-wrap connections. Excessive hand pressure on gun during operation will prevent proper wrapping and must be avoided.

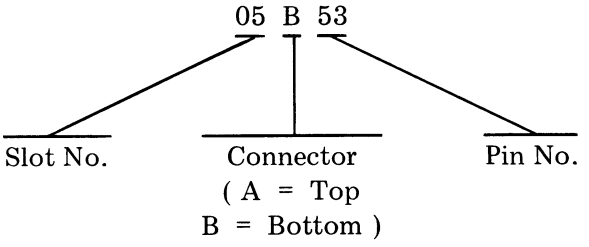
e. Standards for acceptable wire-wrap connections are shown in figure 5-4. The completed wrap must include one-half to one turn of insulation around post at its start. There must be no breaks in insulation that exposes conductor between connections. Bare conductor must make a minimum of 6-1/2 turns around post, and end of wire must not be pulled away from wrap more than one-half turn. There must be no overlapping of turns, and space between turns must not exceed one-half of bare wire diameter.

f. Route wires so than any tension on them tends to tighten wrap rather than to open or loosen it, as shown in figure 5-4. Wires should be dressed around the posts to form smooth curves. Sharp bends are not acceptable.

5-54. Reading the Signal List

5-55. The signal list is a computer-run document that presents information about signals entering and leaving the circuit cards — where the signals originate and where they are going. In other words, it gives interconnecting wiring between the circuit cards, as seen on the back of the mother board circuit card connectors. All connector pins carrying a signal of the same name are grouped together in the list, and these groups are arranged in alphanumeric sequence by signal name. The signal name of each group is entered on the first line of group in the last column, under SIGNAL NAME. Other figures appearing in this column are cumulative wire lengths in inches, which can be ignored.

5-56. Now to the matter of reading the list. When looking for the source and/or destinations of a signal, go to the group listing by signal name first. Each line entry represents one connector pin identified by the last five digits in the LOCATION column. (The first four digits, 1015, are the same for each entry throughout the list and stand for the mother board assembly of interwired connectors.) These last five digits indicate the slot location, connector, and pin, thus:



5-57. The example reference designation given above is for pin 53 of the bottom connector of circuit card slot 05. Another important bit of useful information that the signal list provides is which of the connector pins represents the source of the signal. The signal source is identified by the letter "S" entered immediately after its location reference designation. Each group has at least one line entry so designated. If more than one entry in any given group has the letter "S" in the S-column, it means that all are partial sources of the signal, that logic circuits on two or more circuit cards have their outputs interconnected as a wire-OR or wire-AND gate. All other lines without entries in the S-column are destinations, receiving the signal as inputs from the source.

5-58. The signal list is also a handy reference document for determining which logic diagram contains the generating logic for a signal. A column labeled CKT gives the three-digit mnemonic code for the circuit card type located in the slot location represented by the line entry. It is but an easy matter to look at the CKT column entry of the signal source line to determine which logic diagram

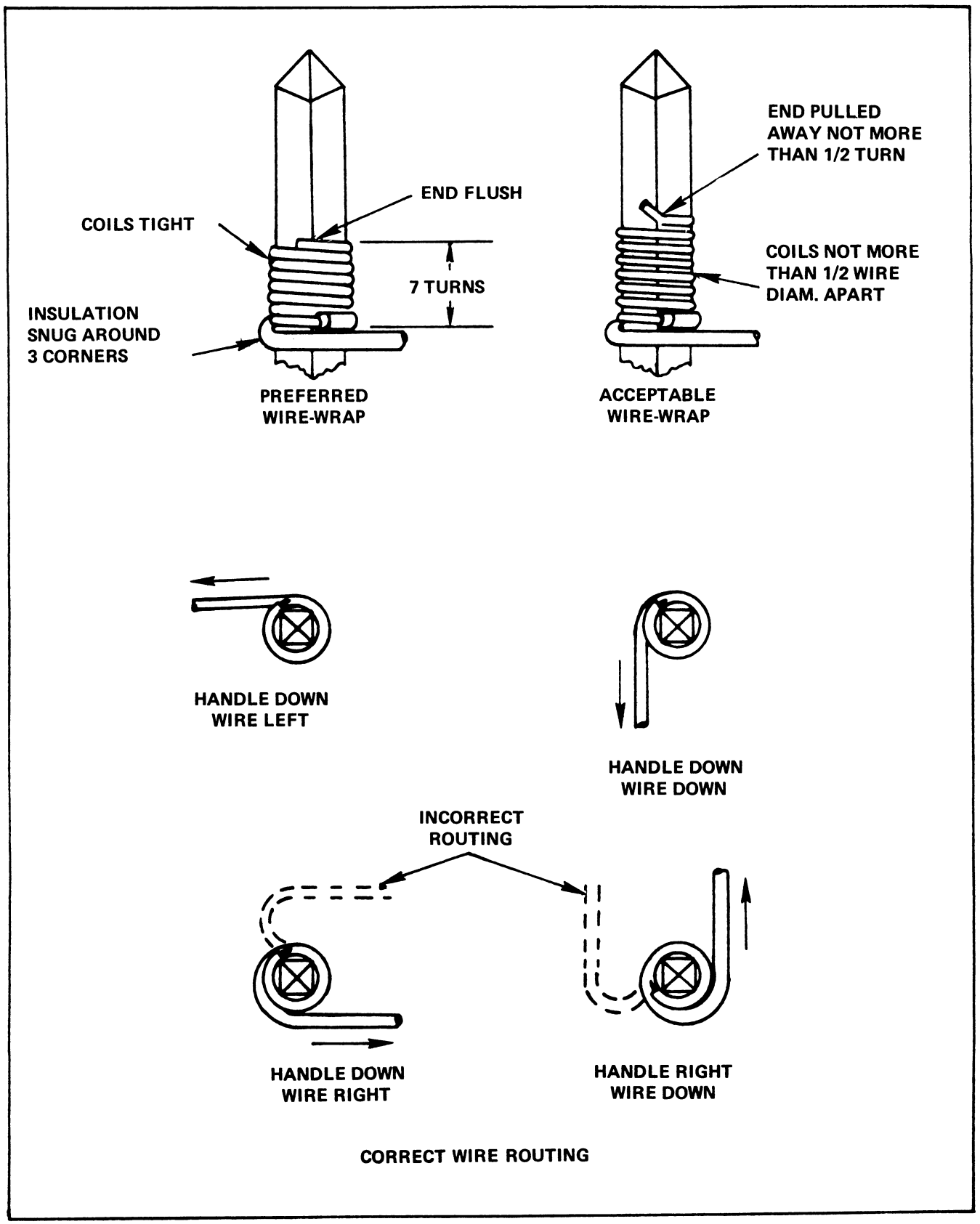


Figure 5-4. Wire-Wraps and Wire Routing.

to go to. For example, the signal source connector pin for signal ACLDAD is 03A31 (last line entry in group, designated the source in the S-column). The code INR is given in the CKT column for this line, indicating that the signal is generated on the Instruction card.

5-59. One other bit of useful information provided to the maintenance technician by the signal list is the layering of interconnecting wires. It will be noticed that a column named LI (for line in) appears to the left of the LOCATION column and that a column named LO (for line out) appears to the right of the S-column. The numbers 0, 1, and 2 entered under these columns indicate which connector pins are directly connected to one another and at what wiring level.

5-60. In using the wire-wrap technique, it is important that wiring be done in layers rather than in a top-to-bottom daisy-chain manner, as depicted in figure 5-5. The latter, unacceptable method does not allow a single wire to be replaced without replacing all or almost all of the wiring for the entire signal distribution, since rewrapping of an unwrapped wire is not permitted. The layer of wires next to the connector body in the acceptable method are called bottom-wrap wires and these are identified on the signal list by the number 1. Those farthest from the connector body are called top-wrap wires and are identified on the signal list by the number 2. The number 0 in either the LI or the LO column indicates "no connection" and identifies the end points of the signal distribution wiring chain.

5-61. When the motherboard is wired semiautomatically at the factory, all bottom-wrap wire connections are made first. For the typical signal group shown in figure 5-5, bottom-wrap wires have been indicated by heavy solid lines drawn between 1's of adjacent line entries. So in the example, pin 05B53 is connected to 06B53 and pin 07B53 is connected to 08B53 during bottom-wrap wiring. After all of the bottom-wrap wires are in place, top-wrap wires are overlayed upon them. These are indicated by the heavy dashed lines drawn between 2's of adjacent line entries. Top-level wires connect pin 06B53 to 07B53 and pin 08B53 to pin 03A31, the source of signal ACLDAD.

5-62. SYSTEM MODIFICATIONS

5-63. Power On-Off Switch Override

5-64. Some users prefer that an on-line system be protected from being shut down by any event short of a power failure, including operating front panel switches. To bypass the power ON and OFF switches on the front panel, proceed as follows:

a. Disconnect processor power cable from wall outlet, and remove cabinet rear connector panel.

b. Install a jumber wire (No. 16 AWG or larger) between terminals 8 and 9 of power supply terminal board TB5.

c. Replace cabinet rear connector panel. Processor will now be turned on whenever power cable plug is plugged into wall outlet and turned off when plug is removed from wall outlet.

Note

Installation of the jumber wire merely bypasses the power ON and OFF switches in the K1 power relay control circuit. Processing can be interrupted if this relay fails.

d. To restore the power control function to power ON and OFF switches at any time, merely disconnect power cable and remove terminal board TB5 jumper wire.

5-65. TTY Address Assignment

CAUTION

For purposes of software standardization, the teletypewriter set controller has been assigned the address E_{16} (1110). Changing the TTY circuit card address jumpers to another address assignment will destroy TTY 700-Series System compatibility.

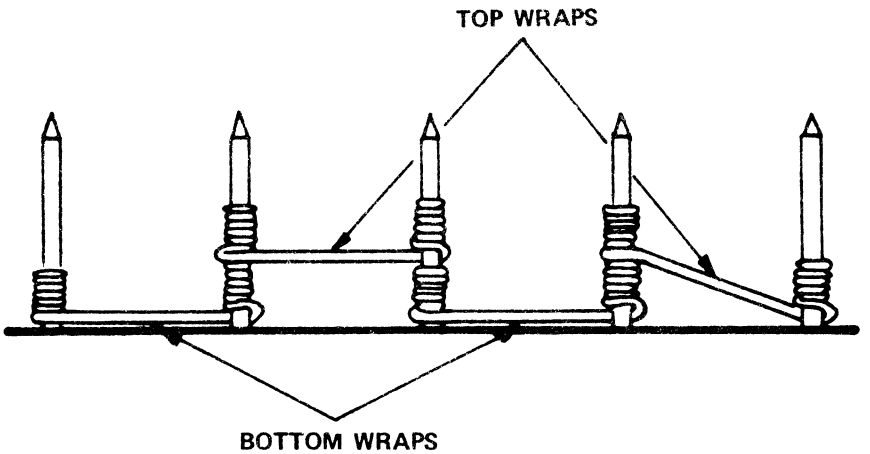
5-66. For some unusual reason, the user may wish to change the address assigned to the TTY

LNTH	NOTE	CKT	EQUATION	EQL	EO	LI	LOCATION	S	LO	WT	WSEQ	SIGNAL NAME
0,5		ARI	AR10	580		0	1015 05B53		1		001	ACLDAD
0,5		ARI	AR14	595		1	1015 06B53		2		002	
0,5		ARI	AR18	585		2	1015 07B53		1		003	
6,5		ARI	ARI1	580		1	1015 08B53		2		004	
8,0		INR	INR	140		2	1015 03A31	S	0		005	8,0/0,0

SOURCE

BOTTOM WRAPS — *TOP WRAPS*

CORRECT WIRE-WRAP SEQUENCE



INCORRECT WIRE-WRAP SEQUENCE

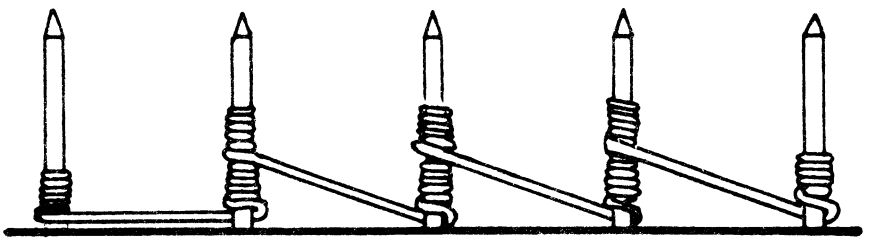


Figure 5-5. Sequence of Wiring from Wire List

controller to something other than E_{16}. This can be done by changing four jumper wires on the face of the TTY circuit card. Proceed as follows:

a. Turn off processor, open front panel access door, disconnect cable to front of TTY circuit card in slot location 16, and remove circuit card. Refer to paragraph 5-50 for correct way to remove circuit card.

b. Locate logic element pad at location coordinates 7B. Using light-duty iron or unsoldering tool (7-1/2 watts or less) quickly unsolder and remove four jumper wires bridging pad.

c. Insert four new jumper wires (insulated or sleeved No. 22 AWG) to select new address, according to appropriate jumper pattern given in table 5-6. Check orientation of adjacent logic elements to determine pin numbers. (Logic element 7A, pin 6, is connected to pin 1 of element pad 7B.)

d. Solder jumper wires in place, using an

Table 5-6. TTY Address Jumper Connections

Device Address		7B Jumpers (PIN — PIN)			
0	(0000)	8 — 9,	5 — 10,	3 — 11,	12 — 13
1	(0001)	8 — 9,	5 — 10,	3 — 11,	1 — 12
2	(0010)	8 — 9,	5 — 10,	2 — 11,	12 — 13
3	(0011)	8 — 9,	5 — 10,	2 — 11,	1 — 12
4	(0100)	8 — 9,	4 — 10,	3 — 11,	12 — 13
5	(0101)	8 — 9,	4 — 10,	3 — 11,	1 — 12
6	(0110)	8 — 9,	4 — 10,	2 — 11,	12 — 13
7	(0111)	8 — 9,	4 — 10,	2 — 11,	1 — 12
8	(1000)	6 — 9,	5 — 10,	3 — 11,	12 — 13
9	(1001)	6 — 9,	5 — 10,	3 — 11,	1 — 12
A	(1010)	6 — 9,	5 — 10,	2 — 11,	12 — 13
B	(1011)	6 — 9,	5 — 10,	2 — 11,	1 — 12
C	(1100)	6 — 9,	4 — 10,	3 — 11,	12 — 13
D	(1101)	6 — 9,	4 — 10,	3 — 11,	1 — 12
E	(1110)	6 — 9,	4 — 10,	2 — 11,	12 — 13
F	(1111)	6 — 9,	4 — 10,	2 — 11,	1 — 12

appropriate, light-duty soldering iron and 60/40 resin-core solder (Kester 44 or equivalent). Clip off lead excesses, and reinstall TTY circuit card.

5-67. TTY and Manual Interrupt Levels

Note

As standard practice, the TTY controller and optional manual interrupt are wired for priority interrupts at levels 0 and 1, respectively. This assumes, of course, that the manual interrupt option will be used with processors with eight or more priority levels installed.

5-68. It is possible that for some unusual application the user may wish the teletypewriter set controller or the manual interrupt option to interrupt at a higher priority level. To change interrupt priority level assignment, proceed as follows:

a. Turn off processor, open front panel access door, disconnect cable to front of TTY circuit card in slot location 16, and remove circuit card. Refer to paragraph 5-50 for correct way to remove circuit card.

b. Locate two circular pads at circuit card coordinates 5A and 6A on component side adjacent to connector B. On unmodified circuit card, there will be two short jumper wires bridging pins on 6A pad.

c. If teletypewriter set controller interrupt level is to be changed, unsolder and remove jumper connected at one end to pin labeled A. Use light-duty iron or unsoldering tool (7-1/2 watts or less) for this work. Jumper connected at one end to pin labeled B should be unsoldered and removed, if manual interrupt priority level is to be changed.

d. Insert new jumper wire (insulated or sleeved No. 22 AWG) between pin labeled A and pin whose number corresponds to new TTY controller interrupt level. Pin labeled B should be used to change manual interrupt priority level.

Note

Use pad 6A for assigning priority levels 0 through 7 and pad 5A for levels 8 through 15. Unlabeled pins are numbered counterclockwise from labeled pin 0 on pad 6A and pin 8 on pad 5A. Notice that pad 6A has two A pins and two B pins that may be used to assign more than one priority level to each device.

e. Solder jumper wires in place, using light-duty soldering iron and 60/40 resin-core solder (Kester 44 or equivalent). Clip off lead excesses, and reinstall TTY circuit card.

Section VI
DRAWINGS

6-1. GENERAL

6-2. This section contains 704 Processor drawings of significant use to the maintenance technician. Logic diagrams of each printed circuit card, schematics of the I.C. logic elements and interconnecting cables, and a source-destination signal list for mother board assembly connector wiring will be found here. Drawings are arranged by type: logic diagrams first, schematics next, and the signal list last. Indexes for each drawing type will be found below.

6-3. LOGIC DIAGRAMS

6-4. Multiple sheet logic diagrams are provided for each circuit card type except the memory module circuit card (memory module is included with schematics). Four logic diagrams cover each application of the Arithmetic circuit card separately. Except for dual Priority Interrupt circuit cards in 16-level machines, this is the only redundant usage of logic cards.

6-5. In general, the logic symbols used on these diagrams follow those set out in MIL-STD-806 and are more thoroughly defined in the I.C. logic element schematics. Numbers adjacent to the inputs and outputs of a symbol are the logic element pin numbers. The logic element type and location are identified within the logic symbol, as shown in figure 6-1.

6-6. The logic diagrams are arranged in drawing number order, as given in the index to logic diagrams. The page number given is that of the first sheet of each drawing.

6-7. SCHEMATICS

6-8. Schematics are included for the memory modules, the control panel circuit card, and the internal and external interconnecting cable assemblies immediately following the circuit card logic diagrams. They are arranged numerically by drawing number, as shown in the index to schematics.

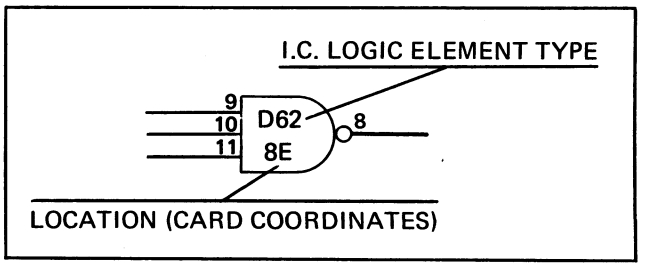


Figure 6-1. Typical Logic Symbol

6-9. INTEGRATED CIRCUIT DIAGRAMS

6-10. Immediately following the schematics, a pair of drawings is provided for each type of I.C. logic element used in the 704 Processor. Typically, these include the symbol used in the logic diagrams to represent the circuit and also an equivalent circuit schematic. Truth tables are also provided where these have been considered informative. These diagrams are arranged alphanumerically by type reference designation, as indicated in the index to I.C. logic element diagrams.

6-11. SIGNAL LIST

6-12. Pin-to-pin wiring between circuit card connectors on the mother board assembly are documented by a signal list, Drawing No. 545222, included at the end of this section. This list is arranged alphabetically and numerically by signal name and aids in the identification of the sources and destinations of all signals passing between circuit cards, by circuit card type, slot location, and connector pin number. Instructions for the interpretation of this list can be found in Section V.

INDEX TO LOGIC DIAGRAMS

INDEX TO SCHEMATICS

INDEX TO I.C. LOGIC ELEMENT DIAGRAMS

INDEX TO I.C. LOGIC ELEMENT DIAGRAMS (Cont)

SIGNAL LIST

RESERVE EO'S OUTSTANDING	REVISIONS							
	SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	X1	APPROVAL PER EO. 18493			JMCK	TLB	[illegible]	3/4/70
	X2	REVISED PER EO. 20885			MZ	TLB	[illegible]	5/28/70
	A	RELEASED PER EO. 19311			JMCK	TLB	TLB	3/4/70

SHEET 1 OF 11

DWG. NO. 394552

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GLOSSARY

ACCØØSRCD	ACCUMULATOR REGISTER BIT ØØ SHIFT RIGHT CIRCULAR DOUBLE
ACØ7SL	ACCUMULATOR REGISTER BIT Ø7 SHIFT LEFT
ACØ8SR	ACCUMULATOR REGISTER BIT Ø8 SHIFT RIGHT
ACCLKENB4	ACCUMULATOR CLOCK CONTROL LOGIC INPUT
ACCLKENBL	ACCUMULATOR REGISTER LEFT BYTE CLOCK ENABLE
ACCLKENBR	ACCUMULATOR REGISTER RIGHT BYTE CLOCK ENABLE
ACDSLOPT	ACCUMULATOR REGISTER SHIFT LEFT CIRCULAR DOUBLE OPTION INPUT
ACLDAD	ACCUMULATOR REGISTER LOAD FROM ADDER
ACLDAD3	ACCUMULATOR REGISTER LOAD FROM THE ADDERR LOGIC INPUT
ACLDAD3A	ACCUMULATOR REGISTER LOAD FROM THE ADDER LOGIC INPUT
ACLDDI	ACCUMULATOR REGISTER LOAD FROM DIO
ACLDOR	ACCUMULATOR REGISTER LOAD ADDER OR OUTPUT
ACLDXOR	ACCUMULATOR REGISTER LOAD ADDER EXCLUSIVE OR OUTPUT
ACRXX	ACCUMULATOR REGISTER BIT FOUR
ACRXXS	ACCUMULATOR REGISTER BIT XX SET INPUT
ACSLENB	ACCUMULATOR REGISTER SHIFT LEFT
ACSLOPT	ACCUMULATOR REGISTER SHIFT LEFT OPTION INPUT
ACSRENB	ACCUMULATOR REGISTER SHIFT RIGHT
ACSROPT	ACCUMULATOR REGISTER SHIFT RIGHT CIRCULAR DOUBLE OPTION INPUT
ACSROPT1	ACCUMULATOR REGISTER SHIFT RIGHT OPTION INPUT
ADENAC	ADDER ENABLE FROM ACCUMULATOR REGISTER
ADENAC2	ADDER ENABLE FROM ACCUMULATOR LOGIC INPUT
ADENACC	ADDER ENABLE FROM ACCUMULATOR REGISTER COMPLEMENT
ADENACCOP	ADDER ENABLE FROM ACCUMULATOR COMPLEMENT LOGIC INPUT
ADENACRB	ADDER ENABLE FROM ACCUMULATOR RIGHT BYTE
ADENEXB	ADDER ENABLE FROM EXTENSION REGISTER BYTE
ADENEXW	ADDER ENABLE FROM EXTENSION REGISTER WORD
ADENIX	ADDER ENABLE FROM INDEX REGISTER
ADENIX2	ADDER ENABLE FROM THE INDEX REGISTER LOGIC INPUT
ADENMBA	ADDER ENABLE FROM MEMORY BUFFER REGISTER LOGIC INPUT
ADENMBB	ADDER ENABLE FROM MEMORY BUFFER BYTE
ADENMBBC	ADDER ENABLE FROM MEMORY BUFFER BYTE COMPLEMENT
ADENMBC	ADDER ENABLE FROM MEMORY BUFFER COMPLEMENT
ADENMBL	ADDER ENABLE FROM MEMORY BUFFER LEFT BYTE
ADENMBR	ADDER ENABLE FROM MEMORY BUFFER RIGHT BYTE
ADENPC	ADDER ENABLE FROM PROGRAM COUNTER
ADENPC2	ADDER ENABLE FROM PROGRAM COUNTER LOGIC INPUT
ADINCRY	ADDER CARRY INPUT
ADONES	ZEROS ADDER BITS Ø5 AND Ø7 FOR DXS
CCCMENDX	COMMAND END LOGIC OUTPUT
CCFBYTE	CENTRAL CONTROL BYTE FLIP-FLOP
CCFGLB	CENTRAL CONTROL GLOBAL MODE FLIP-FLOP
CPSWDIS	DISPLAY MACHINE STATUS ENABLE
DISPXX	CONTROL PANEL DISPLAY BIT XX
EXLDAD1	EXTENSION REGISTER LOAD FROM ADDER LOGIC INPUT
EXLDPC	EXTENSION REGISTER LOAD FROM PROGRAM COUNTER
ICDCØ	ITERATION COUNTER DECODE ZERO
IN4SC5	INSTRUCTION DECODE FOUR AND SEQUENCER STATE FIVE
IN5SC5	INSTRUCTION DECODE FIVE AND SEQUENCER STATE FIVE
INDCDIO	INSTRUCTION DECODE DIO
INDCREAD	INSTRUCTION DECODE READ CYCLE
INDCSHIFT	INSTRUCTION DECODE SHIFT
INDGSKIP	INSTRUCTION DECODE FOR SKIP
INDCX	INSTRUCTION DECODE X
INDCXX	INSTRUCTION DECODE XX
INDCXXX	INSTRUCTION DECODE XXX
INRX	INSTRUCTION REGISTER BIT X
IXLDAD3	INDEX REGISTER LOAD FROM ADDER LOGIC OUTPUT
KK5	GATE CLOCK OUTPUT FIVE
MBRXX	MEMORY BUFFER REGISTER BIT XX
MRESET	MASTER RESET
SCDCX	SEQUENCER STATE X
SCDCX	CONTROL SEQUENCER STATE X
T1	TIMING INTERVAL REGISTER BIT ONE
T4	TIMING INTERVAL REGISTER BIT FOUR
T4SCDC5	TIMING INTERVAL REGISTER FOUR AND CONTROL SEQENCER STATE FIVE
TBDC1	TIMING INTERVAL REGISTER BIT B AND SEQUENCER STATE ONE
TIRCX	TIMING INTERVAL REGISTER BIT X

TABLE I

I.C. DESIGNATION	RAYTHEON PART NUMBER
DS8	531522-001
DEC	531647-001
M00	531593-006
M01	531593-005
M02	531593-007
M03	531593-008
M04	531593-014
M05	531593-004
M06	531593-017
M07	531593-015
M10	531593-002
M25	531593-009
M26	531593-012
M60A	531593-018
TX3	531596-002

3. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" CONNECTOR. C1 THRU C9

2. JUMPERS: SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⇒ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11
REVISION	A	A	A	A	A	A	A	A	A	A	A

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03, .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:

DRAWN	[signature]	3-13-70
CHECK	T. Bowles	3/4/70
APPR	[signature]	3/4/70
APPR	[signature]	3/4/70

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NEXT ASSY: N/A

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

INSTRUCTION CARD (LOGIC DIAGRAM)

CODE IDENT NO.	SIZE	394552
49956	D	

SCALE: NONE — SHEET 1 OF 11

RAYTHEON COMPUTER FORM 67-0064

DWG. NO. 394552 SHEET 1 OF 11

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACØØSRCD	S	B6	4
ACØ7SL	S	A63	4
ACØ8SR	S	A7	4
ACCLKENBA-		A32	4
ACCLKENBL	S	A58	4
ACCLKENBR	S	B36	4
ACDSLOPT-		A39	5
ACLDAD	S	A31	4
ACLDAD3-		A55	4
ACLDAD3A-		A70	4
ACLDDI	S	B65	4
ACLDOR	S	B44	4
ACLDXOR	S	B40	4
ACRØØ-		A9	5
ACRØØS	S	A26	5
ACRØ7		A18	5
ACRØ7S	S	A30	5
ACRØ8		A11	5
ACRØ8S	S	A28	5
ACRI5		A15	5
ACRI5S	S	A29	5
ACSLENB	S	A52	4
ACSLOPT-		A50	4
ACSRENB	S	A27	4
ACSROPT-		B4	4
ACSROPTI-		A42	4
ADENAC	S	B53	7
ADENAC2-		B9	7
ADENACC	S	B49	7
ADENACCOP-		B51	7
ADENACRB	S	B55	6
ADENEXB	S	B25	6
ADENEXW	S	A54	6
ADENIX	S	B23	6
ADENIX2-		B11	6
ADENMBA-		A37	6
ADENMBB	S	B43	6
ADENMBBC	S	B59	6
ADENMBC	S	B26	7
ADENMBC2-		B7	7
ADENMBC3-	S	B30	7
ADENMBL	S	A24	6
ADENMBR	S	A21	6
ADENPC	S	A8	7
ADENPC2-		A35	7
ADINCRY	S	B21	7
ADINCRYC-		B14	7
ADONES	S	B39	7
CCCMEND4	S	A61	10
CCCMEND5	S	A65	10
CCFBYTE-		B56	5
CCFGLB		B60	6
CPSWDSIN-		CA	8
DISPØØ-	S	CC	8
DISPØ1-	S	CD	8
DISPØ2-	S	CB	8
DISPØ3-	S	CK	8
DISPØ4-	S	CE	8
DISPØ5-	S	CJ	8
DISPØ6-	S	CH	8
DISPØ7-	S	CF	8
EXLDADI-	S	A66	5
EXLDPC	S	B46	5
ICDCØ-		A33	4
IN4SC5	S	B57	10
INDCØ	S	A5	10
INDCØ-	S	B58	9
INDCØØ	S	B22	10
INDCØØ1	S	A43	10
INDCØØ3	S	A60	10
INDCØØ6	S	A36	10

SIGNAL LIST

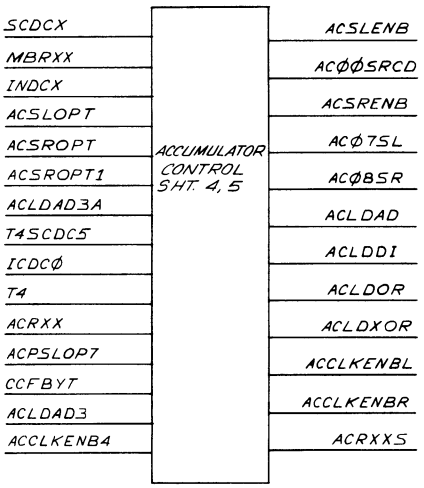
SIGNAL	SOURCE	CONN	SHEET
INDCØØX-	S	B45	9
INDCØ11	S	A62	10
INDCØ3-	S	A69	9
INDCØ4	S	B52	10
INDCØ5	S	B28	10
INDCØ7-	S	A38	9
INDCØ8-	S	B54	9
INDCØ8A	S	A57	10
INDCØ9	S	A44	10
INDCØ9-	S	B10	9
INDCØA-	S	B17	9
INDCØB-	S	B8	9
INDCØC-	S	B33	9
INDCØF-	S	B35	9
INDCIOR2	S	B29	10
INDC2-	S	B31	9
INDCAORB	S	B32	10
INDCBYTE	S	B64	10
INDCDIO	S	B3	10
INDCF	S	B61	10
INDCOPT	S	B5	9
INDCREAD	S	B67	10
INDCSHIFT	S	B20	10
INDCST	S	B48	10
INDCXSKIP	S	B15	5
INDCXXØ-		A12	5
INDCXX1-		A51	10
INDCXX2-		A59	10
INDCXX3-		A41	10
INDCXX4-		A64	5
INDCXX5-		A13	5
INDCXX6-		A53	4
INDCXX7-		A46	10
INDCXX8-		A14	5
INDCXX9-		A48	5
INDCXXA-		A45	10
INDCXXB-		A17	5
INDCXXC-		A20	5
INDCXXD-		A25	5
INDCXXE-		A23	5
INDCXXF-		A16	5
INØ4SC1-	S	B13	5
IXLDAD3-	S	A6	5
IXRØØ-		A22	5
KK3		B19	8
MBRØØ-		B68	8
MBRØ1-		B50	8
MBRØ2-		B47	8
MBRØ3-		B34	8
MBRØ4-		B62	6
MBRØ4B	S	B12	6
MBRØ5-		A67	8
MBRØ6-		B38	8
MBRØ7-		B18	8
MBRØ8-		A19	4
MBRIØ-		A68	4
MBRII-		A49	4
MRESET-		B66	8
SCDC1-		B37	5
SCDC3-		B24	5
SCDC4-		A47	4
SCDC5-		B42	4
SCDC7-		A10	7
SCDC8-		B27	6
SCDCC		B63	4
T4SCDC1		A40	4
TIRC1		B16	8
TIRC4		A34	4
TIRC4-		A56	4
TIRCA		B41	6

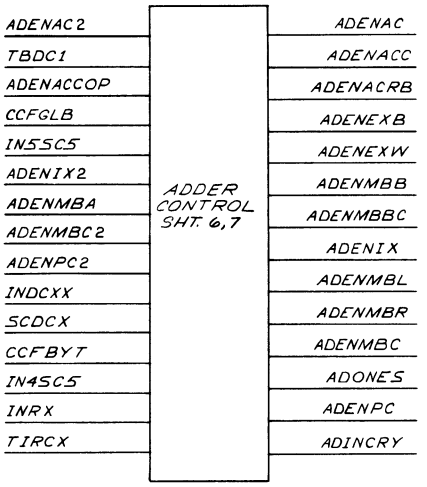
DWG NO. 394552 SHEET 2 OF

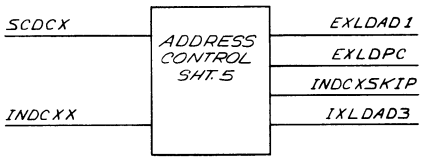
DWG NO. 394552 SHEET 2 OF

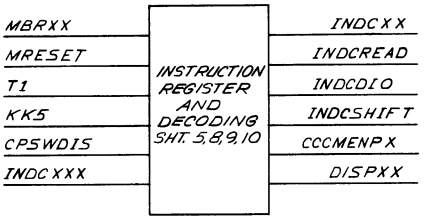
CODE IDENT NO.	SIZE		REV
49956	D	394552	A
SCALE NONE		SHEET 2	

RAYTHEON COMPUTER FORM 87-0085



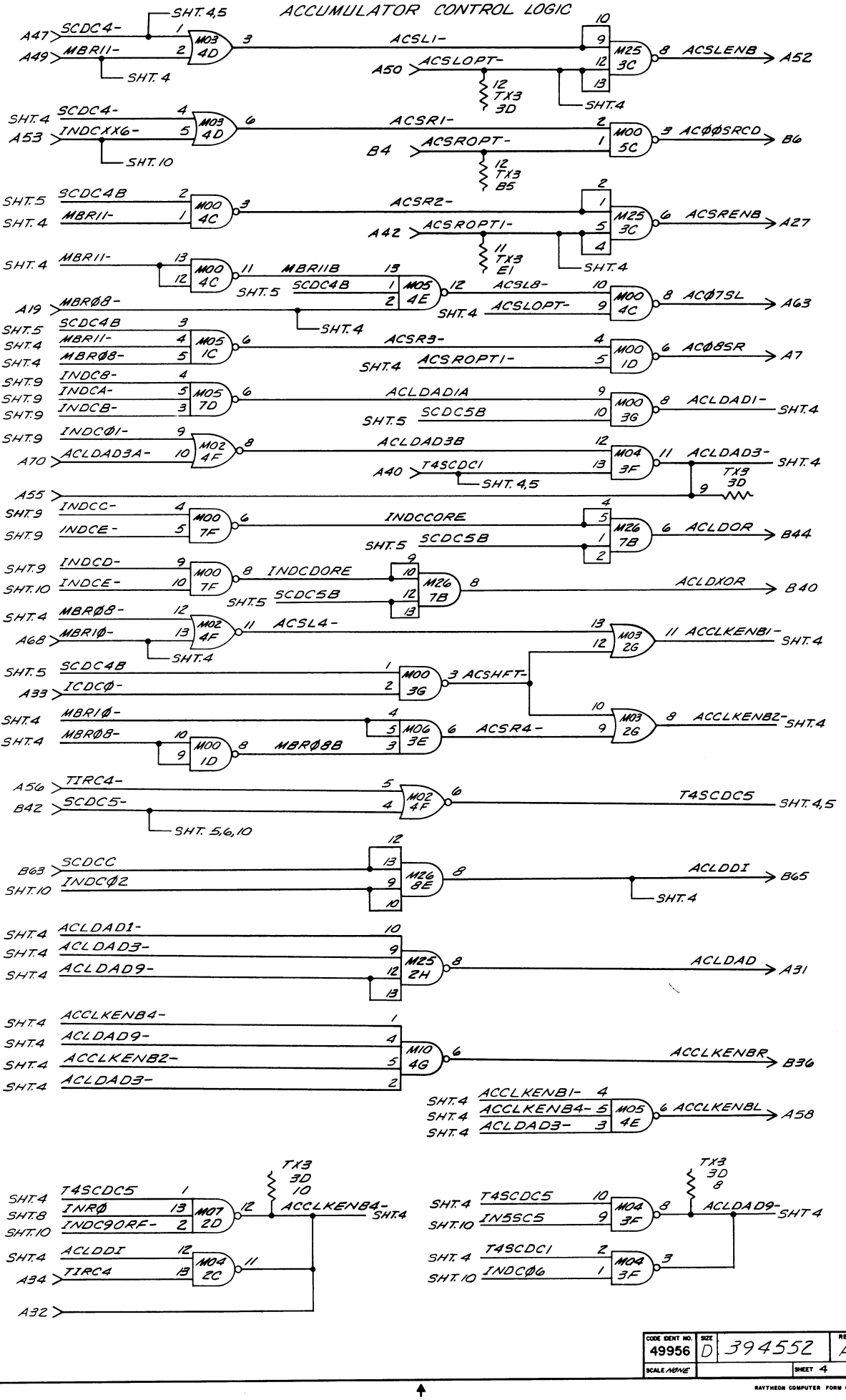


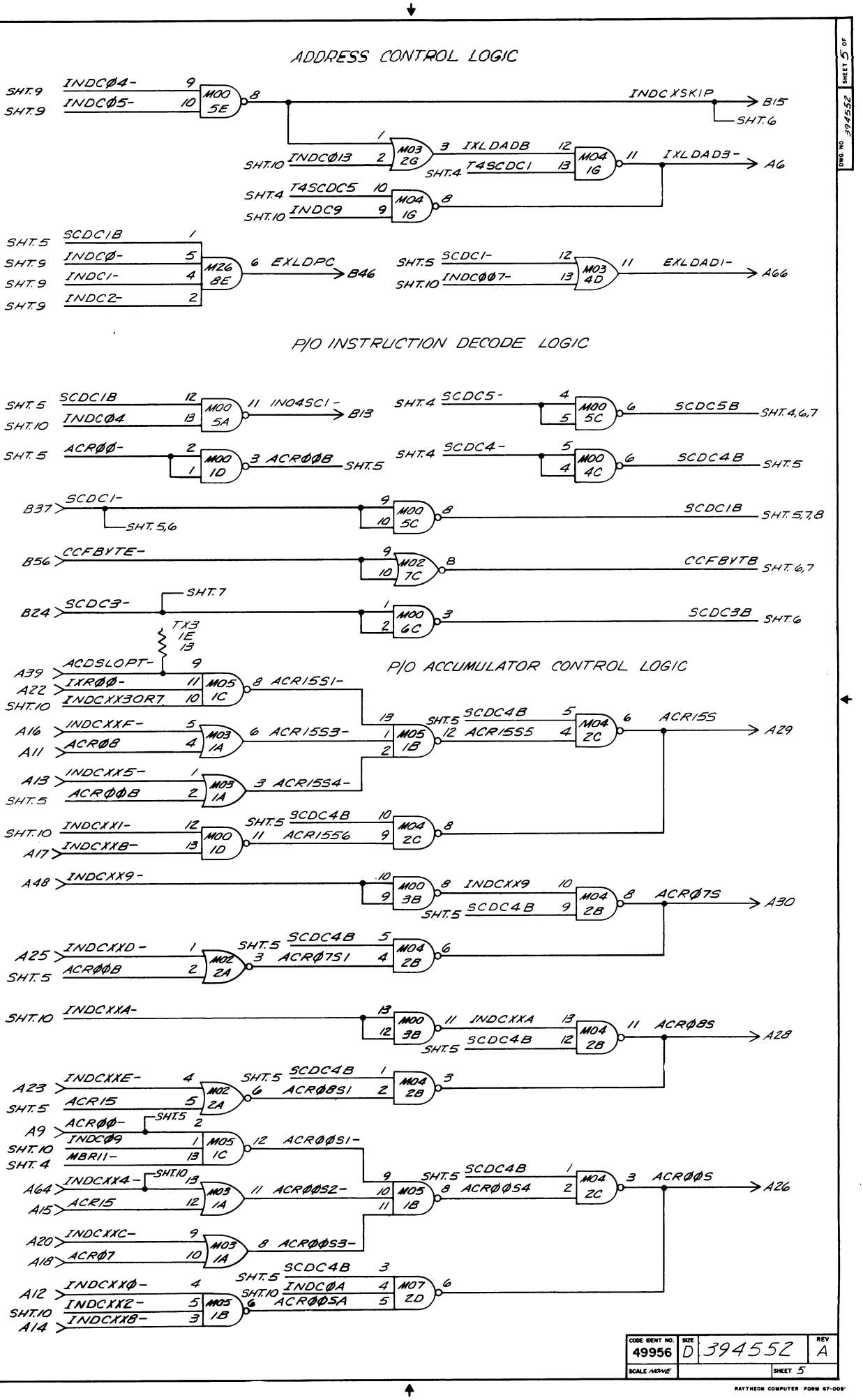


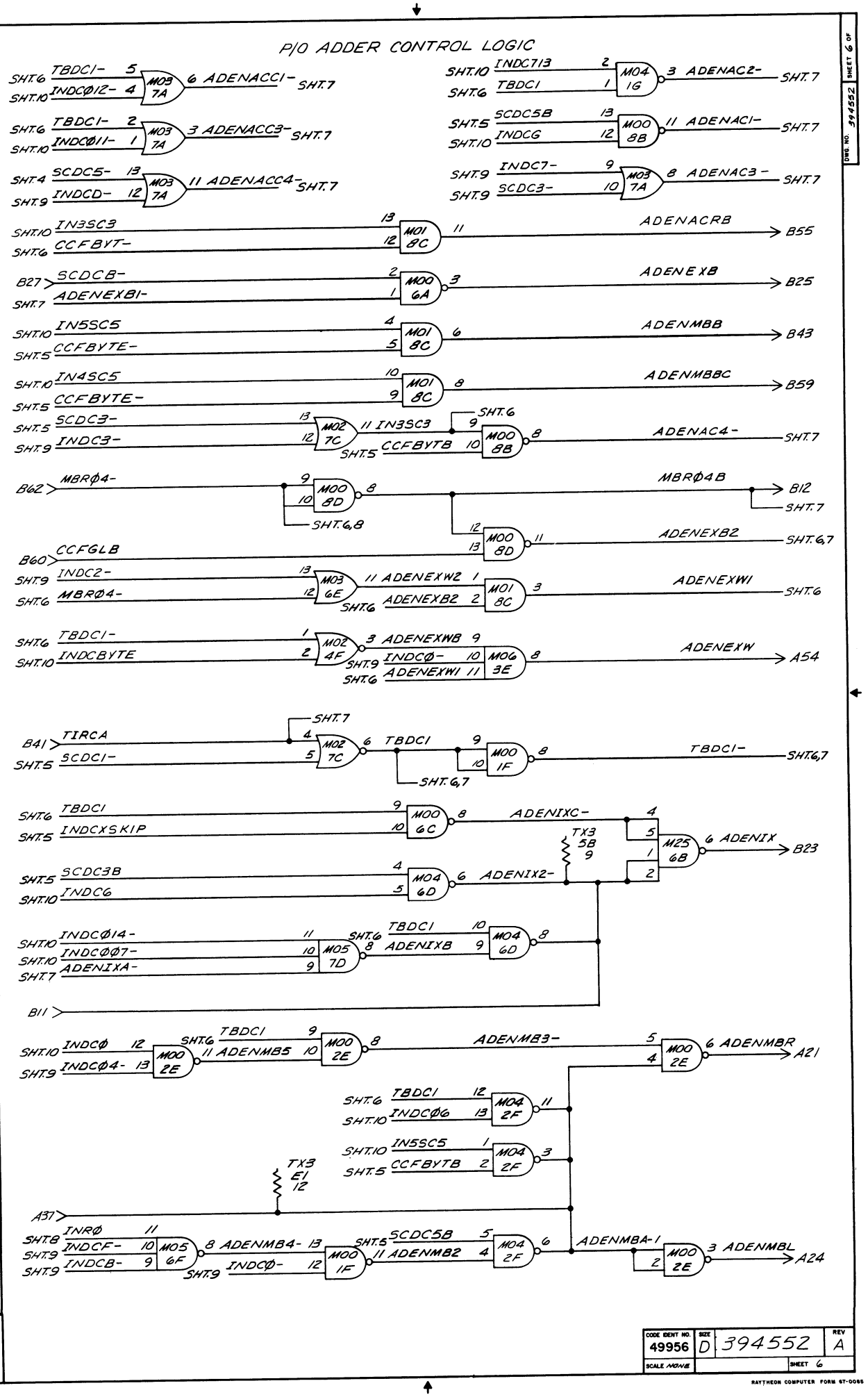


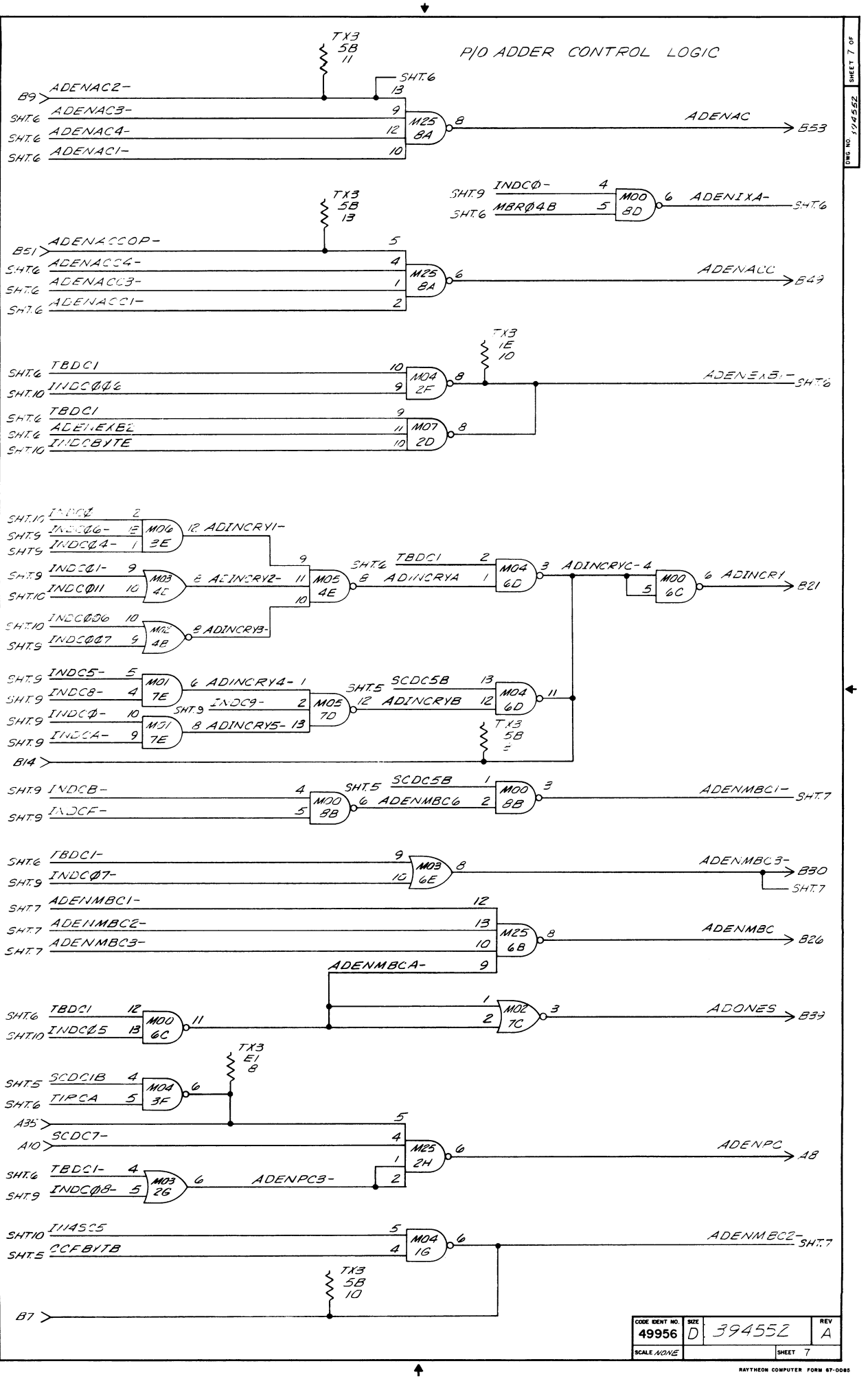
BLOCK DIAGRAM

CODE IDENT NO.	SIZE		REV
49956	D	394552	A
SCALE NONE			SHEET 3

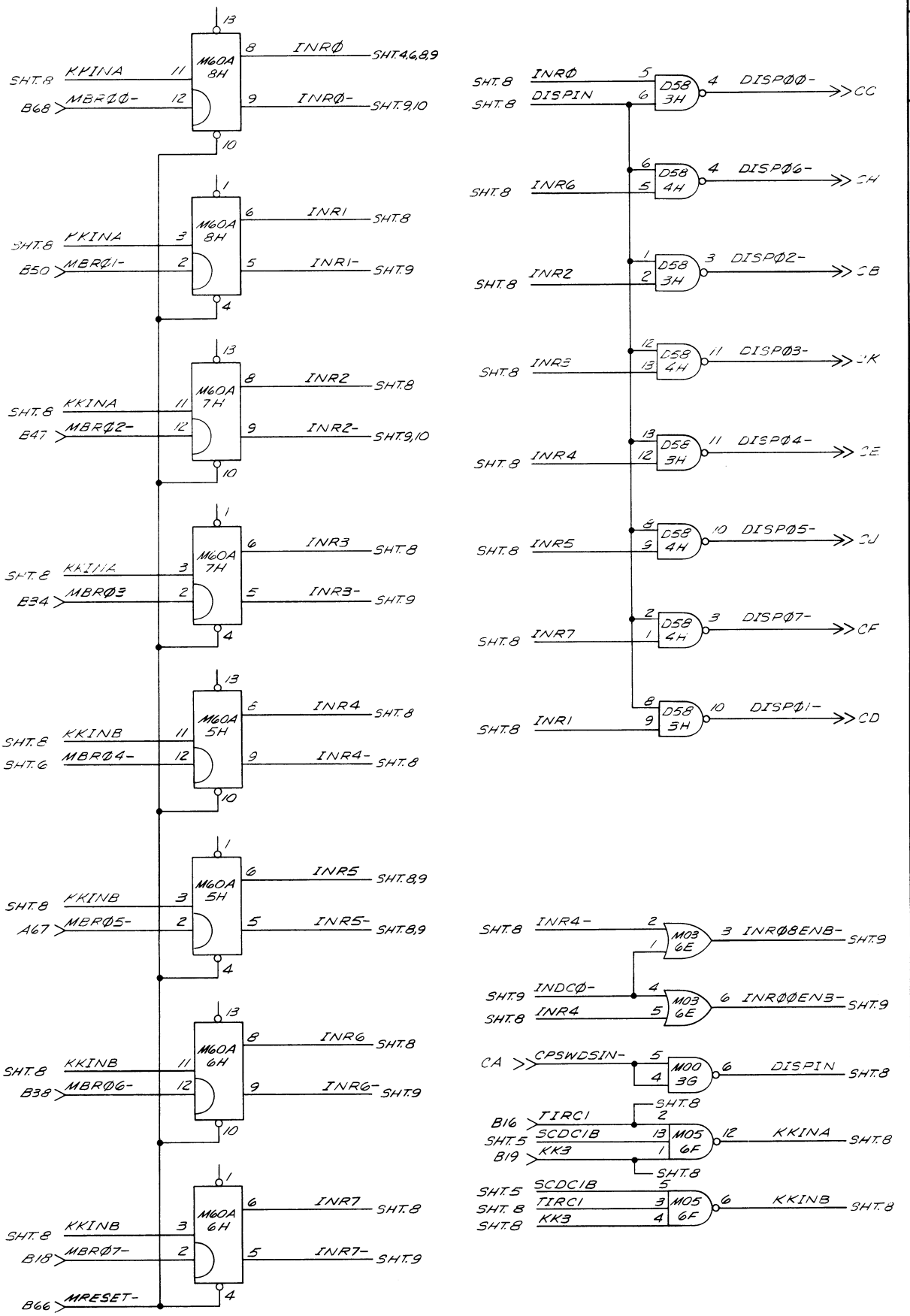

ACCUMULATOR CONTROL LOGIC
SHT. 4,5
A47 SCDC4- 1
A49 MBRI1- 2
M03 4D
SHT. 4
3
ACSLI-
10
9
M25 3C
8 ACSLENB
A52
A50 ACSLOPT-
12
13
12 TX3 3D
SHT.4
SHT.4 SCDC4- 4
A53 INDCXX6- 5
M03 4D
SHT. 10
6
ACSRI-
2
1
M00 5C
3 ACØØSRCD
B6
B4 ACSROPT-
12 TX3 B5
SHT.5 SCDC4B 2
SHT.4 MBRI1- 1
M00 4C
3
ACSR2-
2
1
M25 3C
6 ACSRENB
A27
A42 ACSROPTI-
5
4
11 TX3 E1
SHT.4
SHT.4 MBRI1- 13
12
M00 4C
11 MBRI1B
SHT.5 SCDC4B 1
2
M05 4E
13
12 ACSL8-
10
M00 4C
8 ACØ7SL
A63
A19 MBRØ8-
SHT.4
SHT.4
ACSLOPT-
9
SHT.5 SCDC4B 3
SHT.4 MBRI1- 4
SHT.4 MBRØ8- 5
M05 1C
6
ACSR3-
4
M00 1D
6 ACØ8SR
A7
SHT.4 ACSROPTI-
5
SHT.9 INDC8- 4
SHT.9 INDCA- 5
SHT.9 INDCB- 3
M05 7D
6
ACLDADIA
9
M00 3G
8 ACLDADI-
SHT.4
SHT.5 SCDC5B
10
SHT.9 INDCØI- 9
A70 ACLDAD3A- 10
M02 4F
8
ACLDAD3B
12
M04 3F
11 ACLDAD3-
SHT.4
A40 T4SCDC1
SHT. 4,5
TX3 3D
9
A55
SHT.9 INDCC- 4
SHT.9 INDCE- 5
M00 7F
6
INDCCORE
4
5
M26 7B
6 ACLDOR
B44
SHT.5 SCDC5B
1
2
SHT.9 INDCD- 9
SHT.10 INDCE- 10
M00 7F
8 INDCDORE
9
10
M26 7B
8
ACLDXOR
B40
SHT.5 SCDC5B
12
13
SHT.4 MBRØ8- 12
A68 MBRIØ- 13
M02 4F
11 ACSL4-
13
12
M03 2G
11 ACCLKENBI-
SHT.4
SHT.4
SHT.5 SCDC4B 1
A33 ICDCØ- 2
M00 3G
3 ACSHFT-
SHT.4 MBRIØ- 4
SHT.4 MBRØ8- 10
9
M00 1D
8 MBRØ8B
5
3
M06 3E
6 ACSR4-
10
9
M03 2G
8 ACCLKENB2-
SHT.4
A56 TIRC4- 5
B42 SCDC5- 4
M02 4F
6
T4SCDC5
SHT.4,5
SHT. 5,6,10
12
B63 SCDCC 13
SHT.10 INDCØ2 9
10
M26 8E
8
ACLDDI
B65
SHT.4
SHT.4 ACLDAD1- 10
SHT.4 ACLDAD3- 9
SHT.4 ACLDAD9- 12
13
M25 2H
8
ACLDAD
A31
SHT.4 ACCLKENB4- 1
SHT.4 ACLDAD9- 4
SHT.4 ACCLKENB2- 5
SHT.4 ACLDAD3- 2
M10 4G
6
ACCLKENBR
B36
SHT.4 ACCLKENBI- 4
SHT.4 ACCLKENB4- 5
SHT.4 ACLDAD3- 3
M05 4E
6 ACCLKENBL
A58
TX3 3D 10
SHT.4 T4SCDC5 1
SHT.8 INR Ø 13
SHT.10 INDC90RF- 2
M07 2D
12
ACCLKENB4-
SHT.4
SHT.4 ACLDDI 12
A34 TIRC4 13
M04 2C
11
A32
TX3 3D 8
SHT.4 T4SCDC5 10
SHT.10 IN55C5 9
M04 3F
8
ACLDAD9-
SHT.4
SHT.4 T4SCDC1 2
SHT.10 INDCØ6 1
M04 3F
3
DWG. NO. 394552
SHEET 4 OF
CODE IDENT NO. 49956
SIZE D
394552
REV A
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0088


ADDRESS CONTROL LOGIC
P/O INSTRUCTION DECODE LOGIC
P/O ACCUMULATOR CONTROL LOGIC
INDCXSKIP
IXLDADB
IXLDAD3-
EXLDPC
EXLDAD1-
SCDC1B
SCDC5B
SCDC4B
SCDC1B
CCFBYTB
SCDC3B
ACR15S
ACR07S
ACR08S
ACR00S
SCDC4B
SHT. 5


P/O ADDER CONTROL LOGIC
SHT.6 TBDC1- 5
SHT.10 INDCØ12- 4
M03 7A
6 ADENACC1- SHT.7
SHT.6 TBDC1- 2
SHT.10 INDCØ11- 1
M03 7A
3 ADENACC3- SHT.7
SHT.4 SCDC5- 13
SHT.9 INDCD- 12
M03 7A
11 ADENACC4- SHT.7
SHT.10 INDC713 2
SHT.6 TBDC1 1
M04 1G
3 ADENAC2- SHT.7
SHT.5 SCDC5B 13
SHT.10 INDCG 12
M00 8B
11 ADENAC1- SHT.7
SHT.9 INDC7- 9
SHT.9 SCDC3- 10
M03 7A
8 ADENAC3- SHT.7
SHT.10 IN3SC3 13
SHT.6 CCFBYT- 12
M01 8C
11 ADENACRB B55
B27 SCDCB- 2
SHT.7 ADENEXB1- 1
M00 6A
3 ADENEXB B25
SHT.10 IN5SC5 4
SHT.5 CCFBYTE- 5
M01 8C
6 ADENMBB B43
SHT.10 IN4SC5 10
SHT.5 CCFBYTE- 9
M01 8C
8 ADENMBBC B59
SHT.5 SCDC3- 13
SHT.9 INDC3- 12
M02 7C
11 IN3SC3
SHT.6 9
SHT.5 CCFBYTB 10
M00 8B
8 ADENAC4- SHT.7
B62 MBRØ4- 9
10
M00 8D
8 MBRØ4B B12 SHT.7
SHT.6,8
12
13
M00 8D
11 ADENEXB2 SHT.6,7
B60 CCFGLB
SHT.9 INDC2- 13
SHT.6 MBRØ4- 12
M03 6E
11 ADENEXW2 1
SHT.6 ADENEXB2 2
M01 8C
3 ADENEXW1 SHT.6
SHT.6 TBDC1- 1
SHT.10 INDCBYTE 2
M02 4F
3 ADENEXWB 9
SHT.9 INDCØ- 10
SHT.6 ADENEXW1 11
M06 3E
8 ADENEXW A54
SHT.7
B41 TIRCA 4
SHT.5 SCDC1- 5
M02 7C
6 TBDC1 9
10
M00 1F
8 TBDC1- SHT.6,7
SHT.6,7
SHT.6 TBDC1 9
SHT.5 INDCXSKIP 10
M00 6C
8 ADENIXC- 4
5
TX3 5B 9
1
2
M125 6B
6 ADENIX B23
SHT.5 SCDC3B 4
SHT.10 INDC6 5
M04 6D
6 ADENIX2-
SHT.10 INDCØ14- 11
SHT.10 INDCØØ7- 10
SHT.7 ADENIXA- 9
M05 7D
SHT.6 8
TBDC1 10
ADENIXB 9
M04 6D
8
B11
SHT.10 INDCØ 12
SHT.9 INDCØ4- 13
M00 2E
SHT.6 11 ADENMB5
TBDC1 9
10
M00 2E
8 ADENMB3- 5
4
M00 2E
6 ADENMBR A21
SHT.6 TBDC1 12
SHT.10 INDCØ6 13
M04 2F
11
SHT.10 IN5SC5 1
SHT.5 CCFBYTB 2
M04 2F
3
TX3 E1 12
A31
SHT.8 INRØ 11
SHT.9 INDCF- 10
SHT.9 INDCB- 9
M05 6F
8 ADENMB4- 13
SHT.9 INDCØ- 12
M00 1F
SHT.5 SCDC5B 5
11 ADENMB2 4
M04 2F
6 ADENMBA-1
2
M00 2E
3 ADENMBL A24
DWG. NO. 394552
SHEET 6 OF
CODE IDENT NO. 49956
SIZE D
394552
REV A
SCALE NONE
SHEET 6
RAYTHEON COMPUTER FORM 67-0085


P/O ADDER CONTROL LOGIC
ADENAC
ADENACC
ADENIXA-
ADENEXB1-
ADINCRY1-
ADINCRY2-
ADINCRY4-
ADINCRY5-
ADINCRYA
ADINCRYB
ADINCRYC-4
ADINCR1
ADENMBC1-
ADENMBC3-
ADENMBC
ADENMBC2-
ADENMBCA-
ADONES
ADENPC
ADENPC3-
SHEET 7 OF
DWG NO. 394552
SHEET 1 OF
DWG NO. 394552
CODE IDENT NO. 49956
SIZE D
394552
REV A
SCALE NONE
SHEET 7
RAYTHEON COMPUTER FORM 67-0085

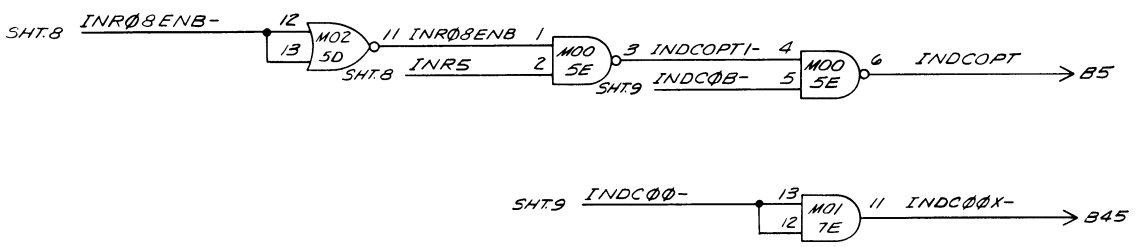
INSTRUCTION REGISTER

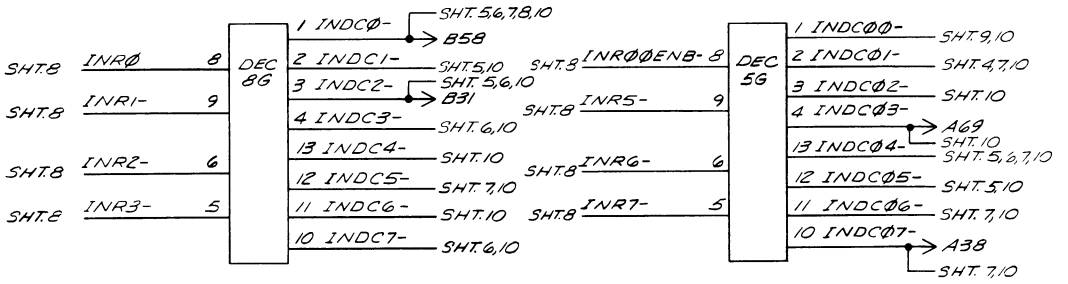


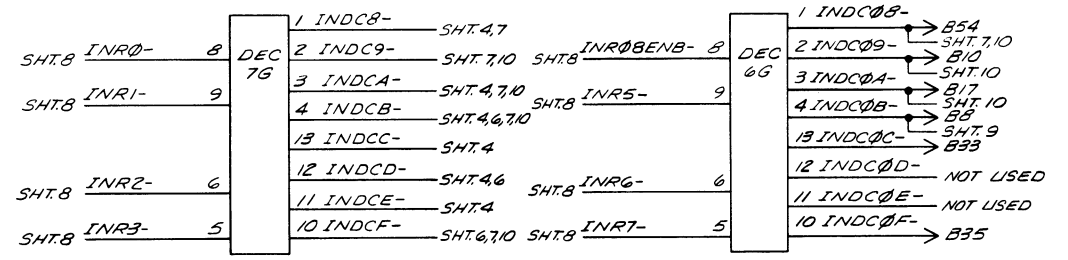
CODE IDENT NO.	SIZE		REV
49956	D	394552	A
SCALE NONE		SHEET 8	

RAYTHEON COMPUTER FORM 67-0085

P/O INSTRUCTION DECODE LOGIC







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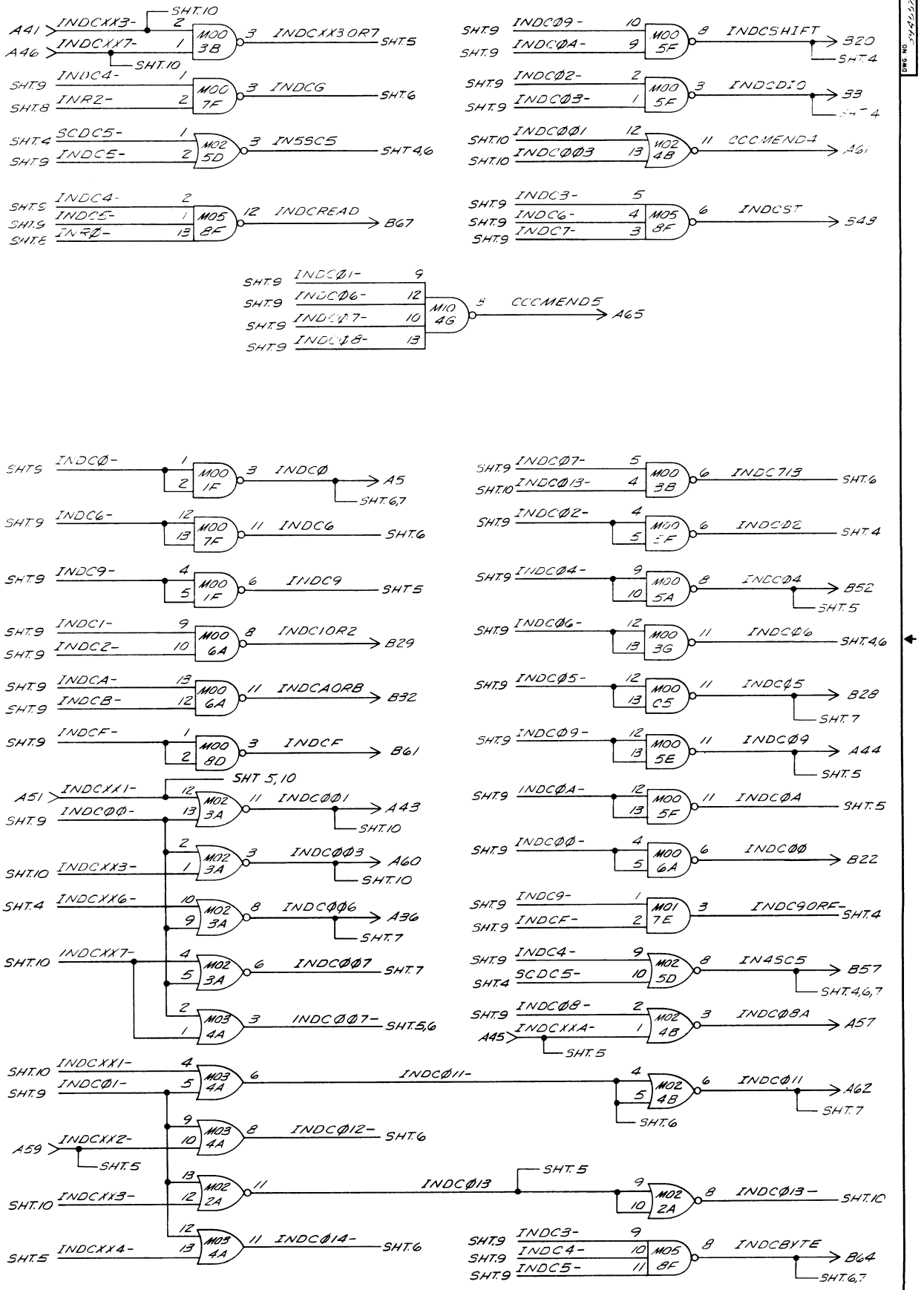
49956	D	394552	A
SCALE NONE		SHEET 9	

P/O INSTRUCTION DECODE LOGIC



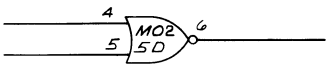
DWG NO. 394552 SHEET 10 OF

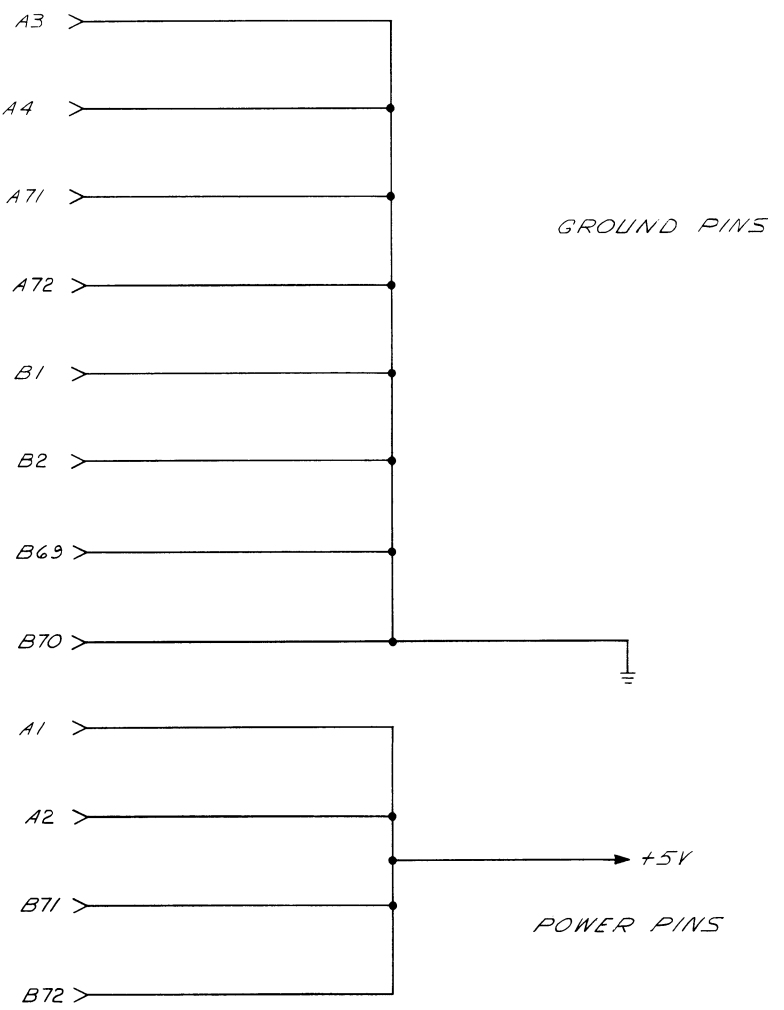
DWG NO. 394552 SHEET 10 OF

CODE IDENT NO.	SIZE		REV
49956	D	394552	A
SCALE NONE			SHEET 10

RAYTHEON COMPUTER FORM 67-0085

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	394552	A
SCALE NONE		SHEET 11	

RAYTHEON COMPUTER FORM 67-0085

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER E.O. 20319				M.F.	N.B.	
X2	REVISED PER E.O. 20915				K.P.	N.B.	
A	RELEASED PER E.O. 19311						
B	REVISED PER E.O. 21433						

SHEET 1 OF 13

DWG NO. 394557

TABLE OF CONTENTS

GLOSSARY

ACRDR-	DIRECT RESET TO ACCUMULATOR
AD3UMØØA	SIGN BIT FOR ARITHMETIC UNIT
ADENMBR-	ENABLE DATA FROM MEMORY BUFFER TO ADDER--RIGHT BYTE
ADENPC2-	ENABLE PROGRAM COUNTER TO ADDER
ADINCRYC-	INCREMENT COUNT IN ADDER
CCCLKEN	CPU NOT PREFORMING A SINGLE-STEP OPERATION
CCCMEND	END OF COMMAND
CCFCLK	DMA NOT ACCESSING MEMORY
CCFSKP	SKIP COMMAND
CCFSYNI	ENABLE FOR I MEMORY CYCLE
CCITCY	START INTERRUPT PROCESS
CPDIAEN	DISPLAY OF ENTER FUNCTION ENABLED
CPSWDCLR-	COMMON RESET FOR AC, MB, IX
CPSWDISP-	DISPLAY DATA AT CONTROL PANEL FROM MEMORY
CPSWDSAC-	DISPLAY ACCUMULATOR FROM CONTROL PANEL
CPSWDSIN-	DISPLAY MACHINE STATUS FUNCTIONS
CPSWDSIX-	DISPLAY INDEX REGISTER FROM CONTROL PANEL
CPSWDSMB-	DISPLAY MEMORY BUFFER FROM CONTROL PANEL
CPSWENT-	ENTER DATA TO MEMORY FROM CONTROL PANEL
CPSWHLT-	MACHINE HALT FROM CONTROL PANEL
CPSWMLCK-	CONTROL PANEL SWITCH MASTER LOCK-OUT
CPSWRST-	MASTER RESET FOR 704 SYSTEM
CPSWRUN-	ENABLE COMPUTER FROM CONTROL PANEL
CPSWSCOM-	SINGLE COMMAND FUNCTION FROM CONTROL PANEL
CPSWSNSX	SENSE SWITCH CONTROL FUNCTIONS FROM CONTROL PANEL
CPSWSSTP-	SINGLE STEP COMMAND FROM CONTROL PANEL
DISPIXX	DISPLAY DECODED STATES OF CONTROL SEQUENCER
EXLDADSRI-	LOAD EXTENSION REGISTER FROM ADDER--INDC1 OR INDC2
ICDCØ	ITERATION COUNT OF Ø
ICRX-	ITERATION COUNT TO MAR
INDCBYTE	BYTE COMMAND FROM INR
INDCXSKIP	SLIP COMMAND (IXS, DXS)
INDCXX	INSTRUCT REGISTER DECODES
ITRSVXX-	SERVICE INTERRUPTS
IXRDR-	DIRECT RESET TO INDEX REGISTER
MALDAD	LOAD ADDER INTO MEMORY ADDRESS
MALDADSR	SHIFT RIGHT MEMORY ADDRESS
MALDPC	LOAD PROGRAM INTO MEMORY ADDRESS
MARXX5	SET TERMS FOR MEMORY ADDRESS REGISTER
MBCLKEN	CLOCK ENABLE FOR MEMORY ADDRESS REGISTER
MBRDR -	DIRECT RESET TO MEMORY BUFFER
MCENMB	ENABLE MEMORY BUFFER DATA LINES FROM DMA
MCWRENT-	ENTER DATA TO MEMORY
MRESET-	MASTER RESET TO SYSTEM
PARER	RECOGNITION OF PARITY ERROR
PCLDAD	LOAD PROGRAM COUNTER FROM ADDER
PCRDR -	DIRECT RESET TO PROGRAM COUNTER
PFRST -	POWER-FAIL RESET
REXTI-	DIRECT RESET TO DIO PERIPHERALS
REXT2-	DIRECT RESET TO DMA PERIPHERALS
SCDCIFØ	RUN SINGLE COMMAND OR SINGLE STEP FUNCTION
SCDC4R	ARITHMETIC SHIFT FUNCTION, ITERATION COUNTER AT ZERO
SCDCCR	DIIO OR SKIP FUNCTION
SCDCX	CONTROL STATES FOR CONTROL SEQUENCER
SCRXOPT-	DISPLAY OPTIONAL FUNCTIONS

TABLE I

I.C. DESIGNATION	RAYTHEON PART NUMBER
M00	531593-006
M01	531593-005
M02	531593-007
M03	531593-008
M04	531593-014
M05	531593-004
M06	531593-017
M07	531593-015
M10	531593-002
M12	531593-016
M25	591593-009
M26	531593-012
M60/M60A	531593-018
M61	531593-011
D37	531531-001
D46	531147-001
D58	531522-001
D62	531148-001
TX2	531596-001
TX3	531596-002

3. THE FOLLOWING PINS ARE TIED TO GROUND ON C AND D CONNECTORS. C1 THRU C22, D1 THRU D22

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⇒ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13
REVISION	B	A	A	A	A	A	A	A	B	A	A	A	

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:

DRAWN	M. FOGEL	2-19-70
CHECK	N. BROTHERS	3-20-70
APPR	BARTE	3-20-70
APPR	D. ALLEN	3-20-70

NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

SEQUENCE COUNTER (LOGIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE D | 394557

SCALE NONE | SHEET 1 OF 13

DWG NO. 394557 SHEET 1 OF 13

RAYTHEON COMPUTER FORM 67-0086

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACRDR-	S	A32	9
ADENMBA-	S	A5Ø	11
ADENIPC2-	S	B67	11
ADINCRYC-	S	A39	11
ADSUMØØ-		B66	6
AUSUMØØA		B39	6
CCCLKEN	S	B19	1Ø
CCCMEND1-	S	B58	6
CCCMEND3-	S	B29	6
CCCMENDA		B43	6
CCCMEND5		B38	6
CCCMEND6-		B56	6
CCCMEND7-		B45	6
CCFCLK		B21	7
CCFRST-	S	A4Ø	9
CCFSKP		B59	7
CCFSKP-		B26	9
CCFSSTP-	S	B34	1Ø
CCFSYN1	S	A43	1Ø
CCITCY		B27	4
CPDIAEN	S	B54	1Ø
CPHLTL-	S	DR	1Ø
CPRUN-	S	A26	12
CPRUNENB-	S	DS	1Ø
CPRUNL-	S	DN	1Ø
CPSENSØ	S	A9	11
CPSENS1	S	A11	11
CPSENS2	S	A5	11
CPSENS3	S	A7	11
CPSSTP	S	A8	12
CPSSTPL-	S	DP	1Ø
CPSWDCLR-		DD	9
CPSWDISP		DH	12
CPSWDISP-		DA	12
CPSWDSAC-		DB	9
CPSWDSIN-		CS	1Ø
CPSWDSIX-		DC	9
CPSWDSMB-		CR	9
CPSWENT		CK	12
CPSWENT-		CL	12
CPSWHLT		CJ	12
CPSWHLT-		CH	12
CPSWMLCK-		DJ	12
CPSWPCLR-		CT	9
CPSWRST-		DL	9
CPSWRST-		A46	9
CPSWRUN		CZ	12
CPSWRUN-		CY	12
CPSWCOM		CP	12
CPSWCOM-		CX	12
CPSWSNSØ		DM	11
CPSWSNSØ-		CD	11
CPSWSNS1		CC	11
CPSWSNS1-		CB	11
CPSWSNS2		CE	11
CPSWSNS2-		CF	11
CPSWSNS3		CA	11
CPSWSNS3-		CW	11
CPSWSSTP		CM	12
CPSWSSTP-		CN	12
DISPI2-	S	DE	5
DISPI3-	S	DF	5
DISPI4-	S	CV	5
DISPI5-	S	DK	5
EXLDADSRI-	S	B44	6
ICDCØ		B60	6
ICDCØ-		A69	4
ICRØ-		A18	8
ICRI-		A20	8
ICR2-		A23	8
ICR3-		A25	8
INDCØ		B50	6
INDCØ-		B49	6
INDCØØ		B47	6
INDCØØØ		B37	4
INDCØØI		A54	5

SIGNAL LIST

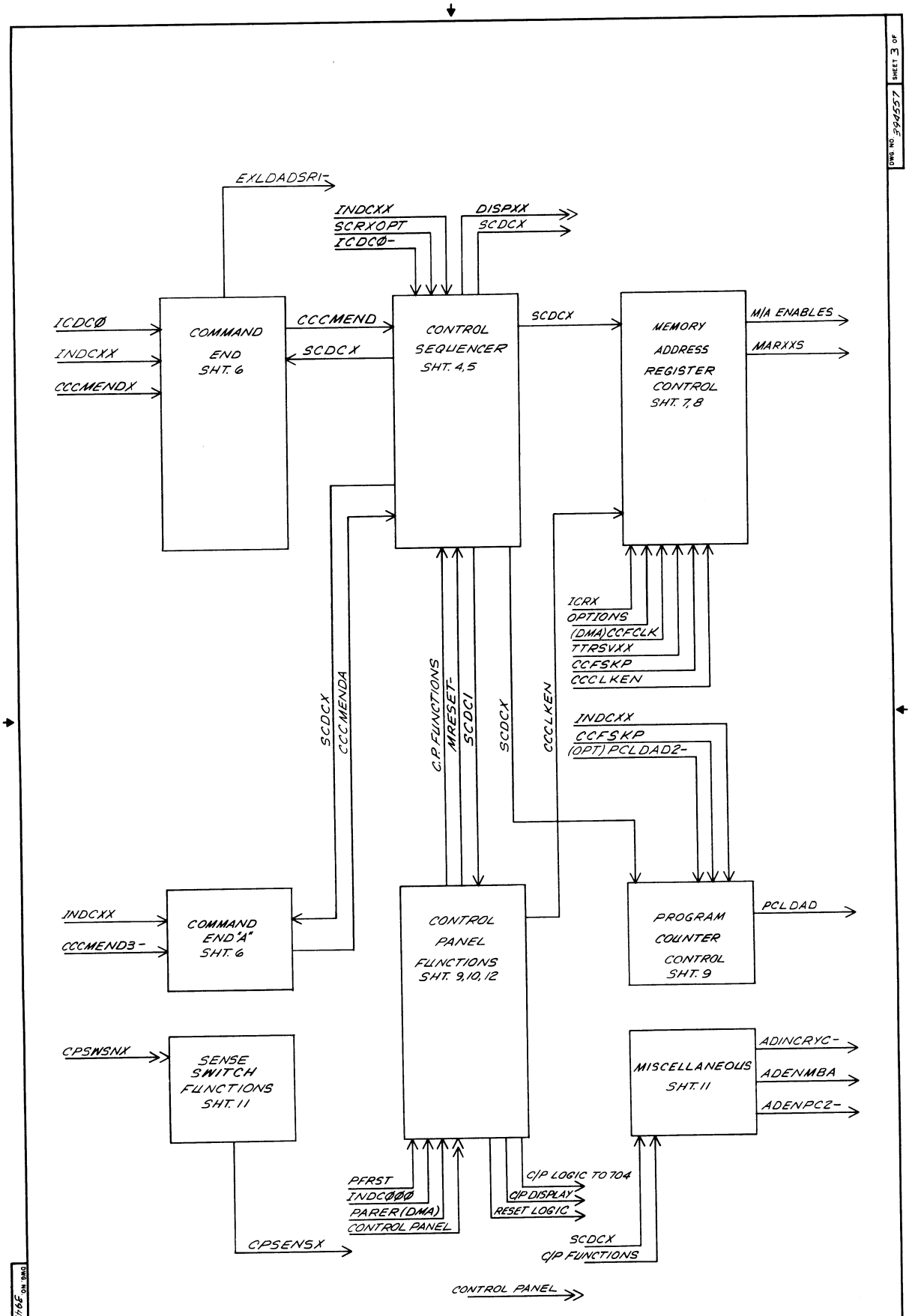
SIGNAL	SOURCE	CONN	SHEET
INDCØØ3		B62	6
INDCØ4		B41	6
INDCØ5		B68	6
INDCIOR2		B52	6
INDCBYTE		B53	7
INDCOIO		A48	4
INDCOPT		B64	6
INDCREAD		A59	4
INDCSHIFT		A67	4
INDCST		B7	7
INDCXSKIP		B33	9
ITRSVIØ-		A31	8
ITRSVII-		A29	8
ITRSVI2-		A27	8
ITRSVI3-		A13	8
IXRDR-	S	A34	9
KK2A		A65	5
KKBI		B15	7
MACLKEN	S	B13	7
MALDAD	S	B63	7
MALDAD-	S	B65	7
MALDADSR	S	B61	7
MALDADSR-		B57	7
MALDPC	S	B46	7
MALDPCI		B14	7
MARIØS	S	A16	8
MARIIS	S	A22	8
MARI2S	S	A21	8
MARI3S	S	A19	8
MARI4S	S	A17	8
MARI5S	S	A15	8
MBRDR-	S	A10	9
MCENB3	S	B28	5
MCENMAS	S	B31	7
MCENMB		A6	10
MCWRENT-	S	A45	12
MRESET-	S	B12	9
PARER-		B55	10
PCLDAD	S	B18	9
PCLDAD2-		B48	9
PCRDR-	S	A33	9
PERST-	S	B8	9
REXTI-	S	A66	10
REXT2-	S	A64	10
SCDCØ	S	B36	4
SCDCØ-	S	B40	4
SCDCØR	S	B10	4
SCDCIA	S	B42	4
SCDCI-	S	B35	4
SCDCIFØ	S	B22	4
SCDC3	S	B23	4
SCDC3-	S	B17	4
SCDC4	S	B30	4
SCDC4-	S	B32	4
SCDC4R	S	A63	4
SCDC5	S	B9	4
SCDC5-	S	B20	4
SCDC7	S	A61	4
SCDC7-	S	A47	4
SCDC7ORB-	S	A49	5
SCDC9	S	A41	5
SCDC9-	S	A37	5
SCDCB	S	A52	5
SCDCB-	S	A38	5
SCDCC	S	A36	4
SCDCC-	S	A24	4
SCDCCR	S	A51	4
SCDCD	S	A12	5
SCDCD-	S	A14	5
SCRIOPT-		B24	5
SCR2OPT-		A55	5
SCR3OPT-		A57	5
SCRFOPT-		A35	5
SCRFOPT-		CU	5
SCRØOPT-		A44	5
TIRCI		B25	9
TIRC4		B11	5
T4SCDCI	S	B51	

SHEET 2 OF
DWG. NO 394557

DWG. NO 394557
SHEET 2 OF

CODE IDENT NO.	SIZE		REV
49956	D	394557	A
SCALE NONE		SHEET 2	

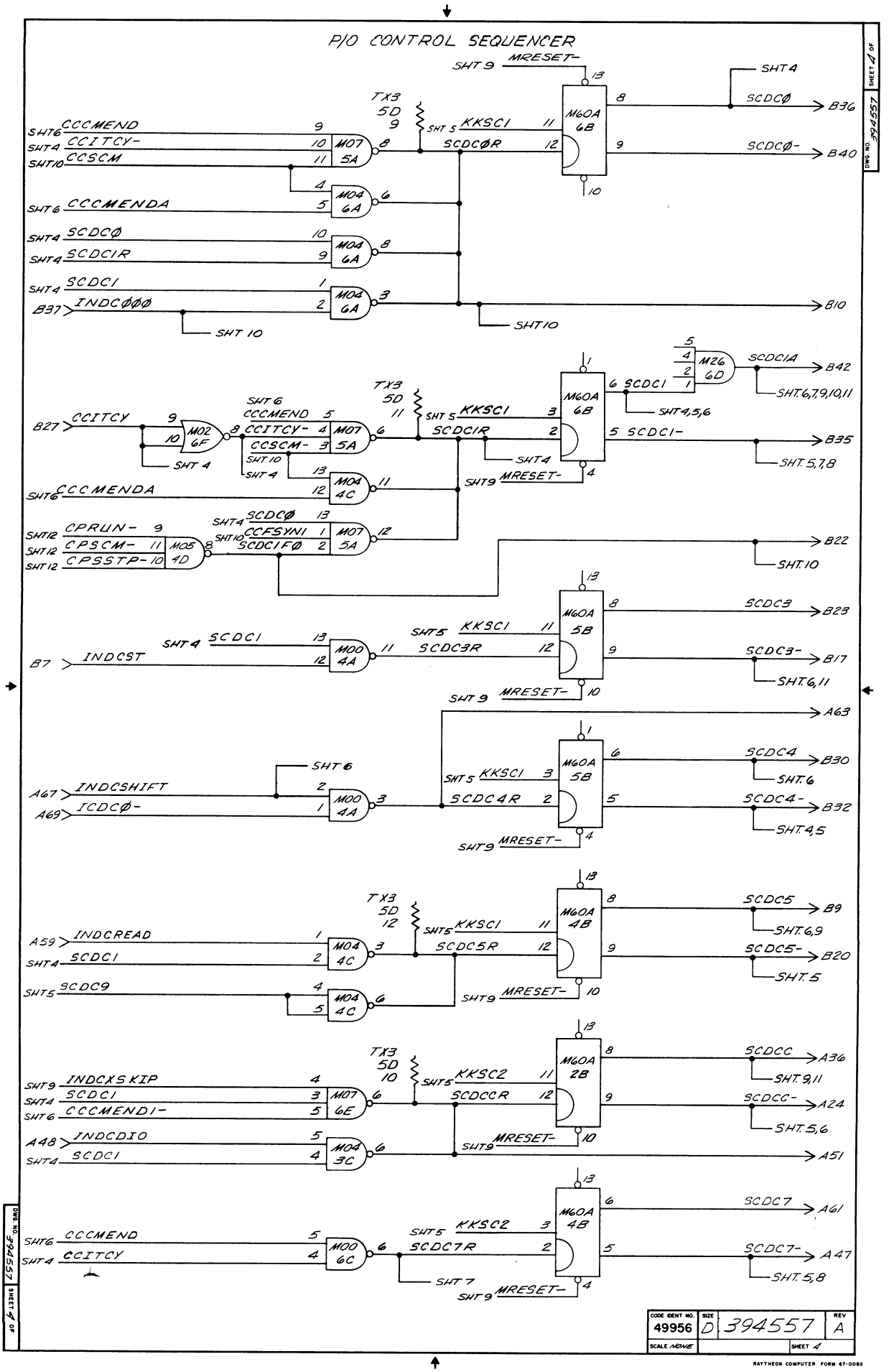
RAYTHEON COMPUTER FORM 67-0085



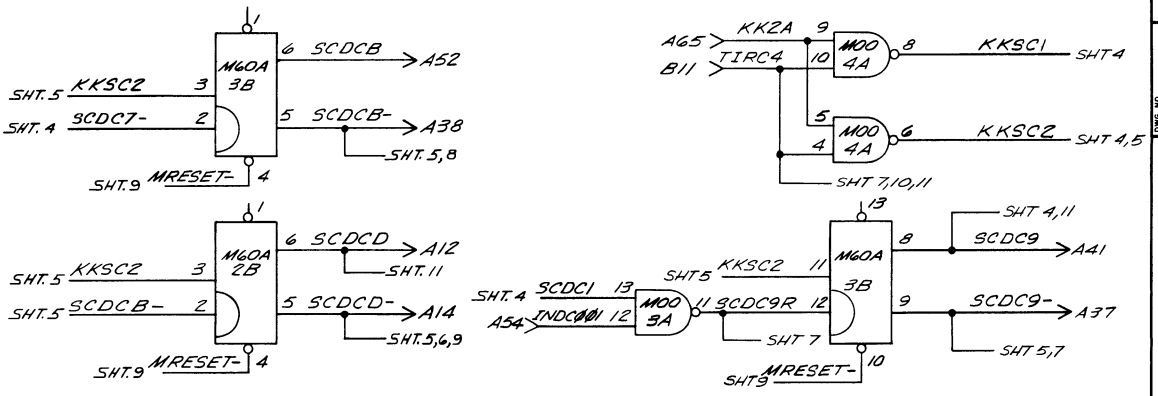
BLOCK DIAGRAM

CODE IDENT NO.	SIZE		REV
49956	D	394557	A
SCALE NONE		SHEET 3	

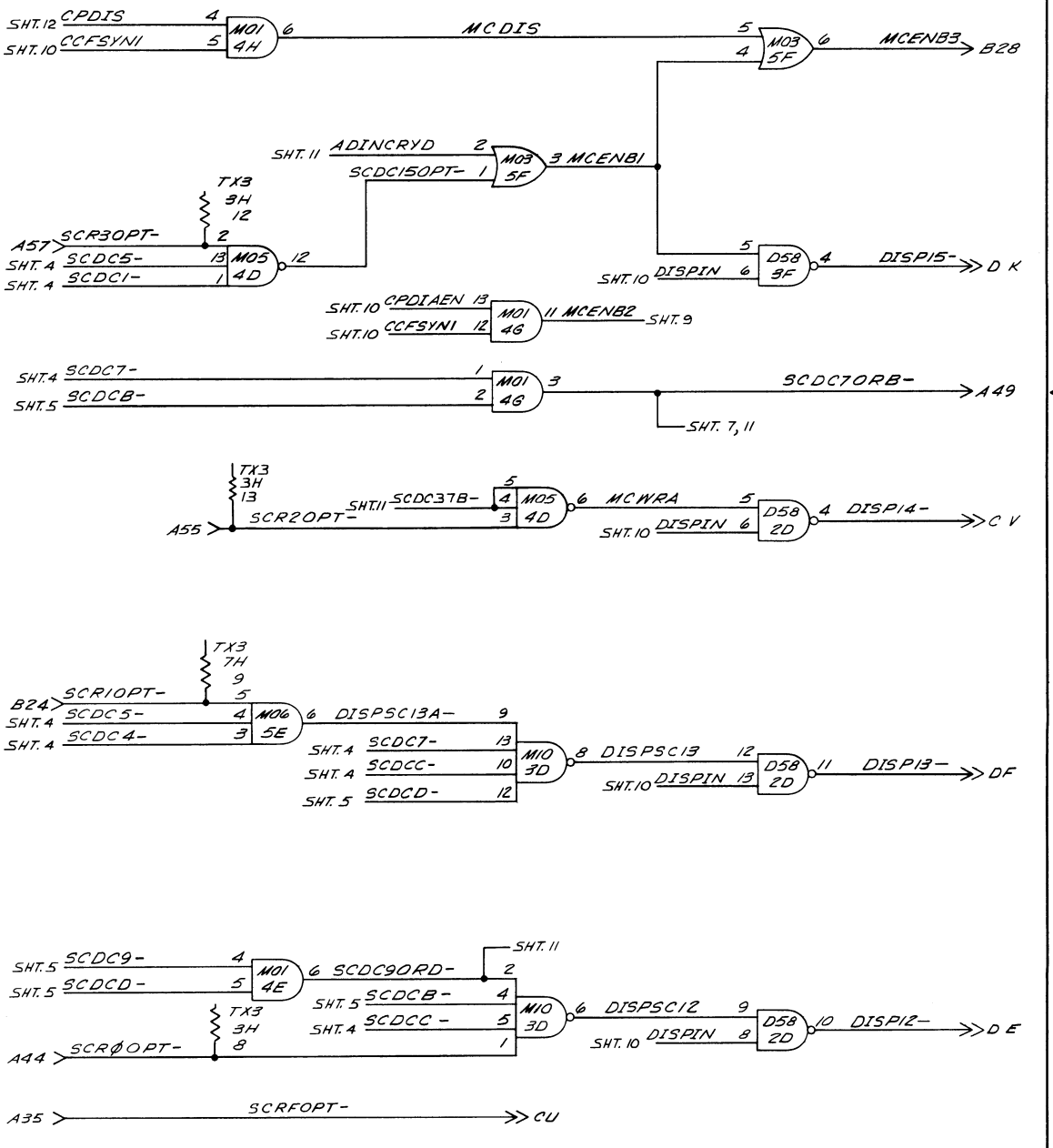
RAYTHEON COMPUTER FORM 67-0085


P/O CONTROL SEQUENCER
SHEET 4 OF 4
DWG NO 394557
SHT 9 MRESET-
SHT 4
SCDCØ
B36
SCDCØ-
B40
TX3 5D 9
SHT 5 KKSC1
SCDCØR
M60A 6B
M07 5A
CCCMEND
CCITCY-
CCSCM
SHT6
SHT4
SHT10
M04 6A
CCCMENDA
SCDCIR
SCDCI
INDCØØØ
B37
B10
SHT 10
SHT10
M26 6D
SCDCIA
B42
SHT.6,7,9,10,11
SCDCI
SHT4,5,6
SCDCI-
B35
SHT.5,7,8
B27
CCITCY
M02 6F
SHT 4
SHT 6
CCCMEND
CCITCY-
CCSCM-
SHT 10
SHT 4
SCDCIR
SHT4
SHT9 MRESET-
CPRUN-
CPSCM-
CPSSTP-
SHT12
M05 4D
SCDCØ
CCFSYNI
SCDCIFØ
SHT10
B22
SHT.10
SCDC3
B23
SCDC3-
B17
SHT.6,11
B7
INDCST
M00 4A
SCDC1
SHT4
SHT5 KKSC1
SCDC3R
A63
SHT6
A67
INDCSHIFT
A69
ICDCØ-
SCDC4
B30
SHT.6
SCDC4-
B32
SHT.4,5
SCDC4R
A59
INDCREAD
SCDC9
SHT5
SCDC5
B9
SHT.6,9
SCDC5-
B20
SHT.5
SCDC5R
SHT9 MRESET-
SHT5 KKSC2
SCDCCR
SCDCC
A36
SHT.9,11
SCDCC-
A24
SHT.5,6
INDCXSKIP
SCDCI
CCCMENDI-
A48
INDCDIO
A51
SHT9
SHT4
SHT6
SHT5
SCDC7
A61
SCDC7-
A47
SHT.5,8
SCDC7R
SHT 7
CODE IDENT NO. 49956
SIZE D
394557
REV A
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0085

P/O CONTROL SEQUENCER

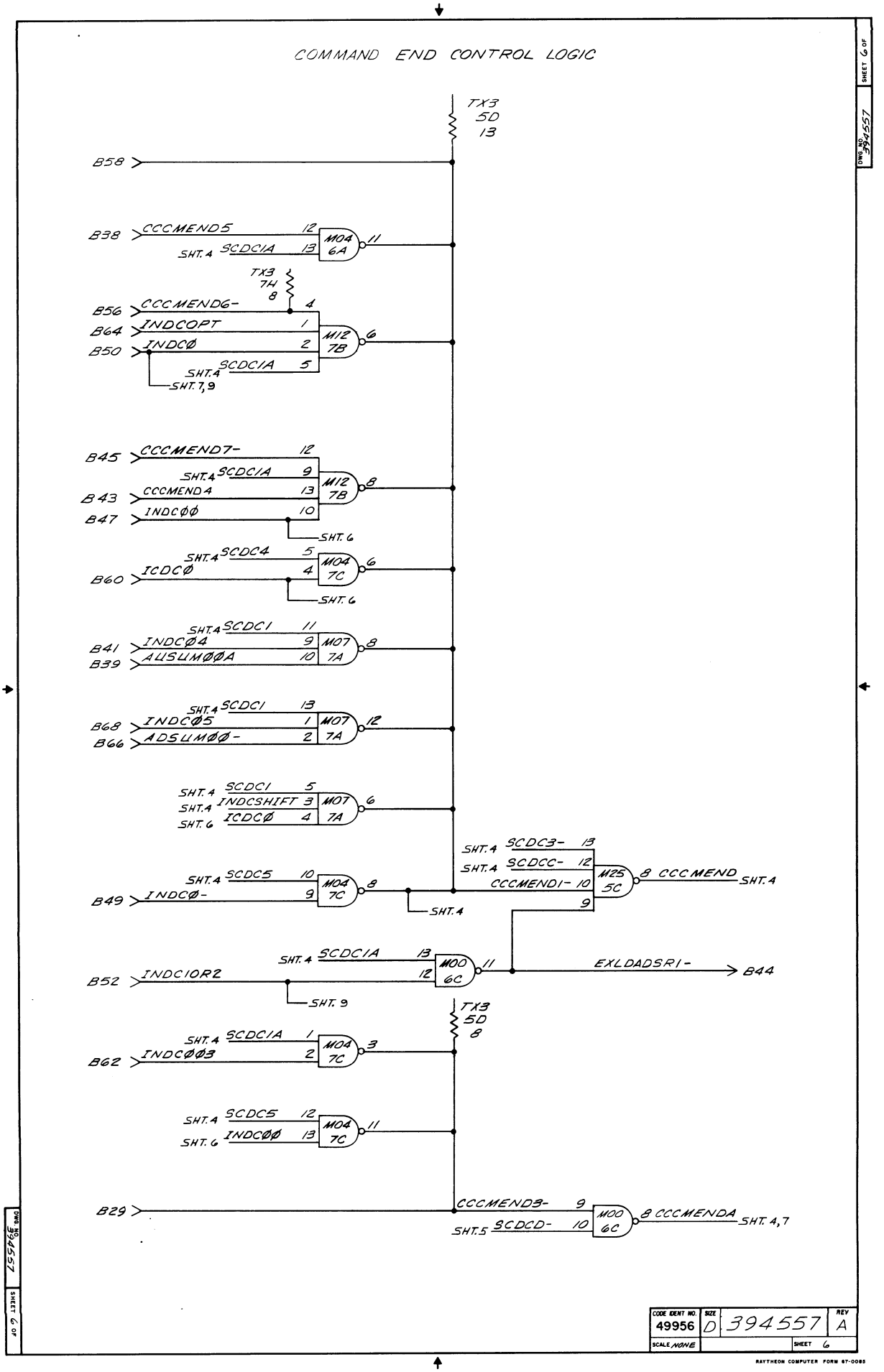


CONTROL SEQUENCER DISPLAY DECODER

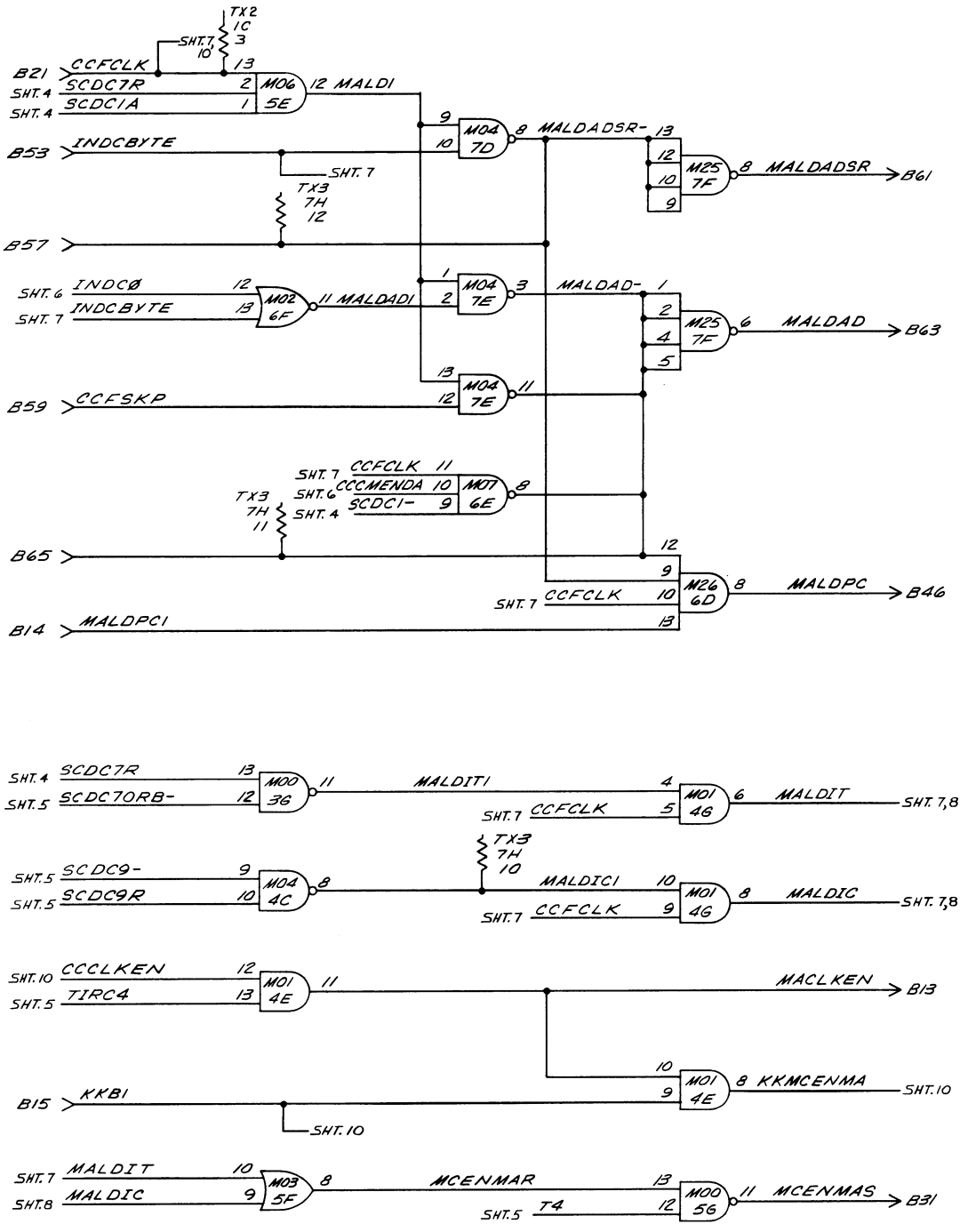


CODE IDENT NO.	SIZE		REV
49956	D	394557	A
SCALE NONE		SHEET 5	

RAYTHEON COMPUTER FORM 67-0085


COMMAND END CONTROL LOGIC
SHEET 6 OF
DWG NO 394557
TX3 5D 13
B58
B38 CCCMEND5 12
SHT. 4 SCDC1A 13
M04 6A
11
TX3 7H 8
B56 CCCMEND6- 4
B64 INDCOPT 1
B50 INDCØ 2
SCDC1A 5
SHT. 4
SHT. 7,9
M12 7B
6
B45 CCCMEND7- 12
SHT. 4 SCDC1A 9
B43 CCCMEND4 13
B47 INDCØØ 10
M12 7B
8
SHT. 6
SHT. 4 SCDC4 5
B60 ICDCØ 4
M04 7C
6
SHT. 6
SHT. 4 SCDC1 11
B41 INDCØ4 9
B39 ALUSUMØØA 10
M07 7A
8
SHT. 4 SCDC1 13
B68 INDCØ5 1
B66 ADSUMØØ- 2
M07 7A
12
SHT. 4 SCDC1 5
SHT. 4 INDCSHIFT 3
SHT. 6 ICDCØ 4
M07 7A
6
SHT. 4 SCDC3- 13
SHT. 4 SCDCC- 12
CCCMEND1- 10
M25 5C
8 CCCMEND
SHT. 4
9
SHT. 4 SCDC5 10
B49 INDCØ- 9
M04 7C
8
SHT. 4
SHT. 4 SCDC1A 13
B52 INDCIOR2 12
M00 6C
11
EXLDADSR1-
B44
SHT. 9
TX3 5D 8
SHT. 4 SCDC1A 1
B62 INDCØØ3 2
M04 7C
3
SHT. 4 SCDC5 12
SHT. 6 INDCØØ 13
M04 7C
11
B29
CCCMEND3- 9
SHT. 5 SCDCD- 10
M00 6C
8 CCCMENDA
SHT. 4,7
DWG NO 394557 SHEET 6 OF
CODE IDENT NO. 49956
SIZE D
394557
REV A
SCALE NONE
SHEET 6
RAYTHEON COMPUTER FORM 67-0085

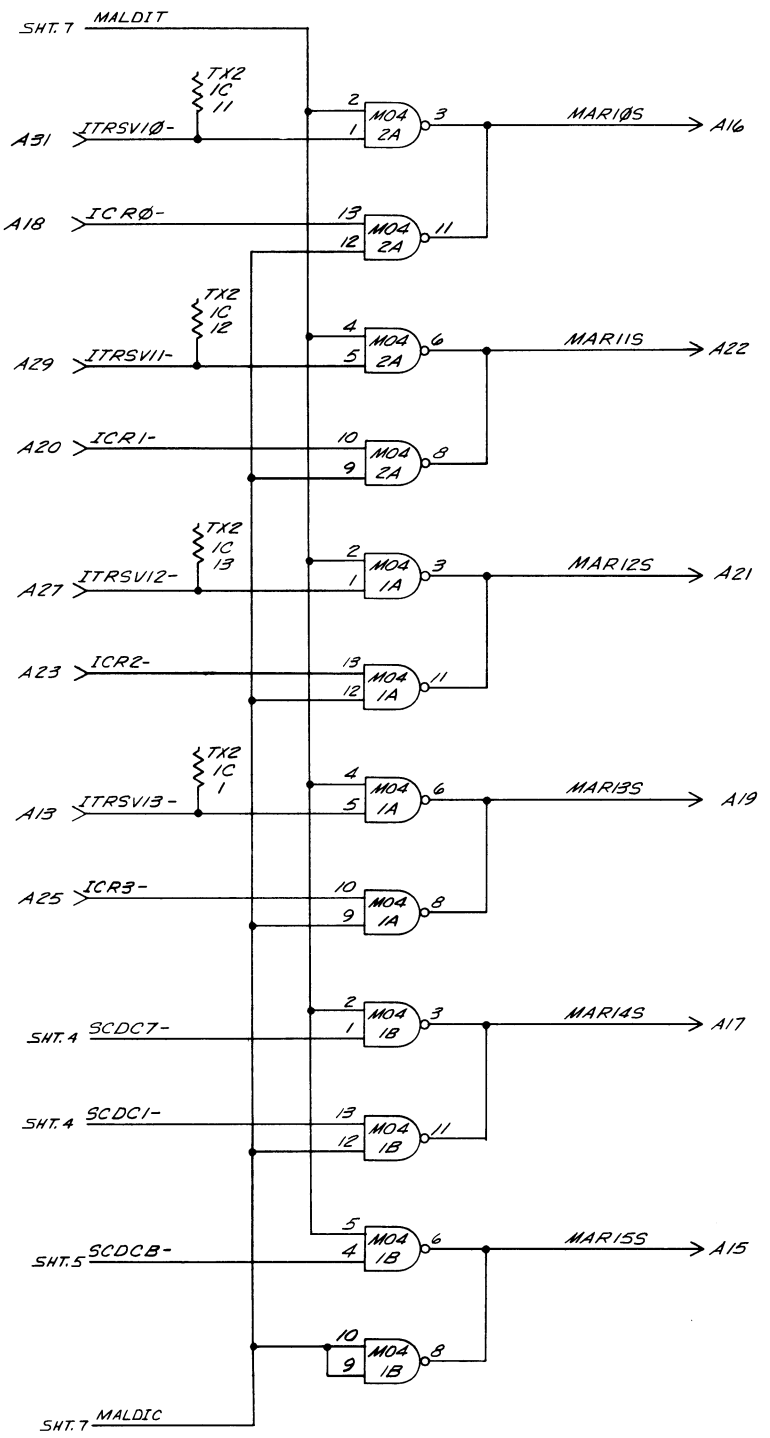
P/O MEMORY ADDRESS REGISTER CONTROL LOGIC



CODE IDENT NO.	SIZE		REV
49956	D	394557	A
SCALE NONE		SHEET 7	

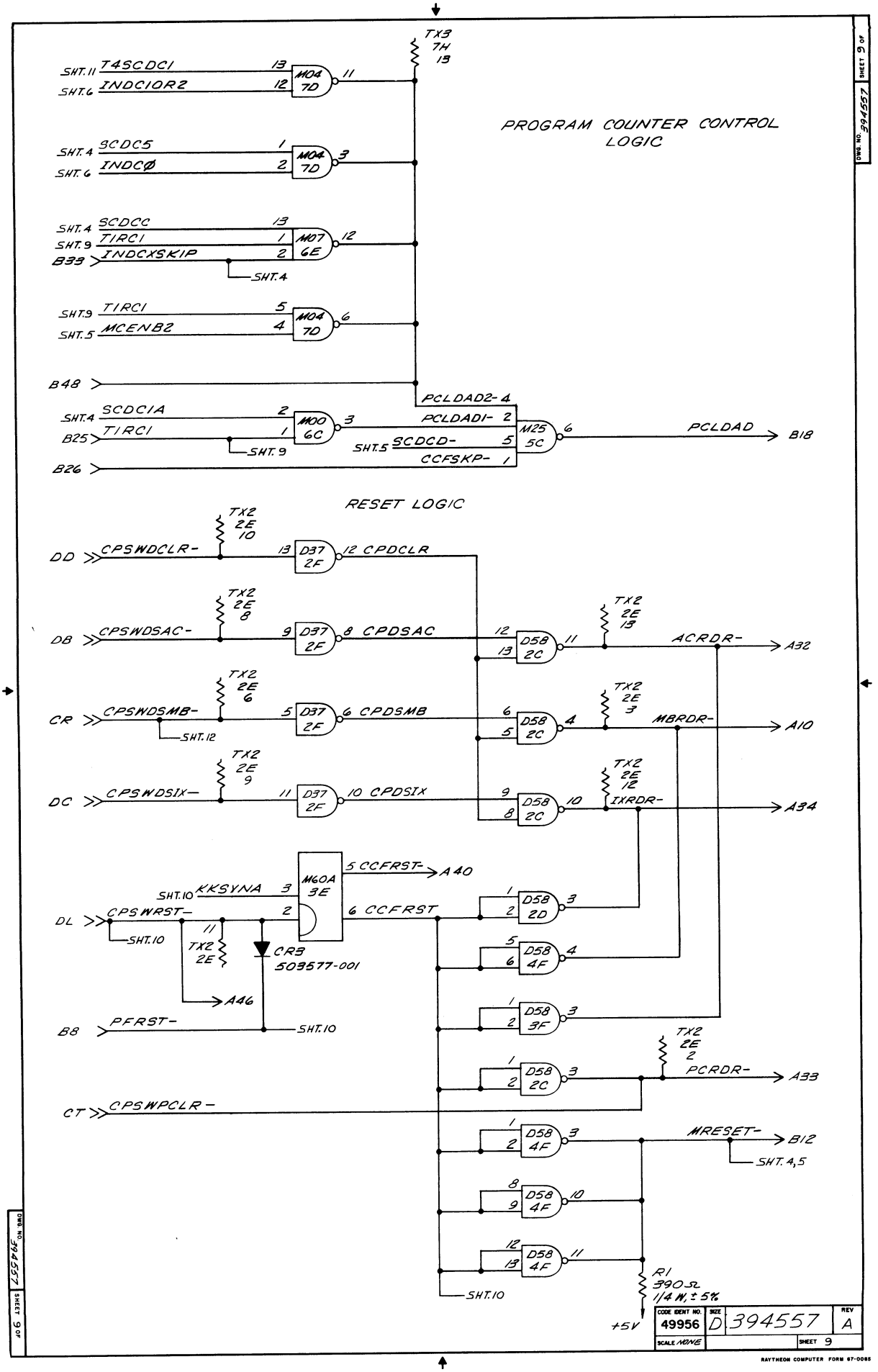
RAYTHEON COMPUTER FORM 67-0085

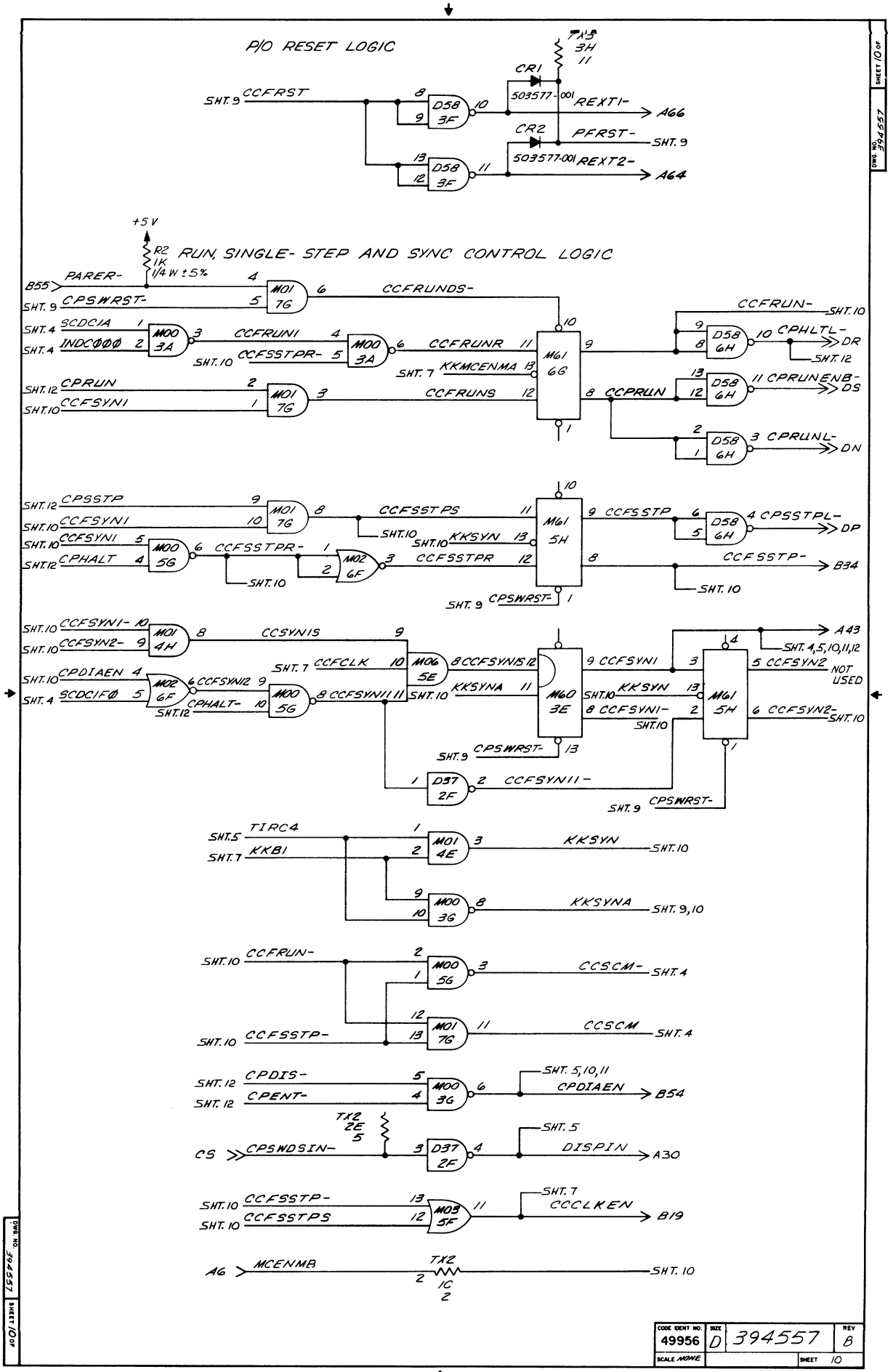
P/O MEMORY ADDRESS REGISTER CONTROL LOGIC

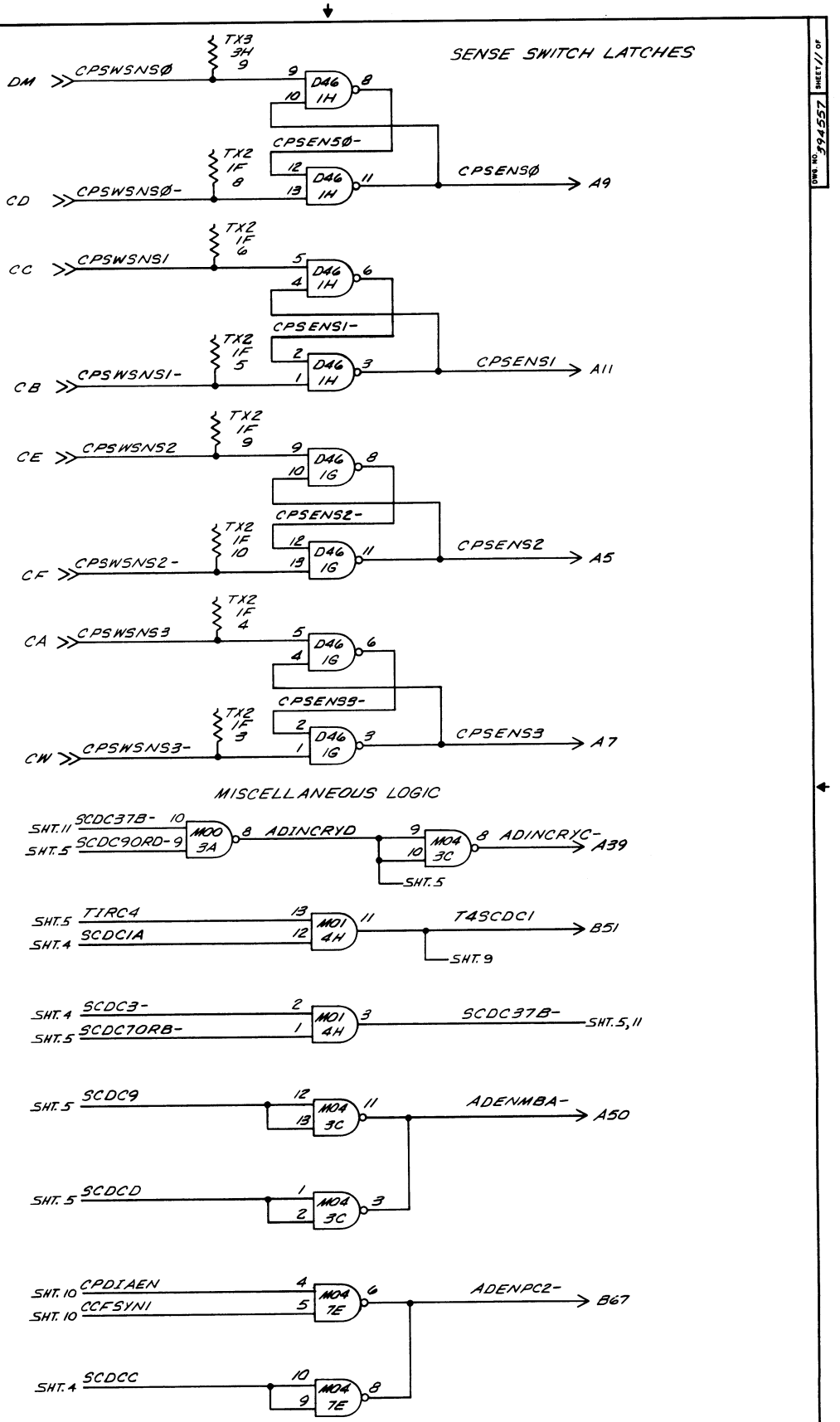


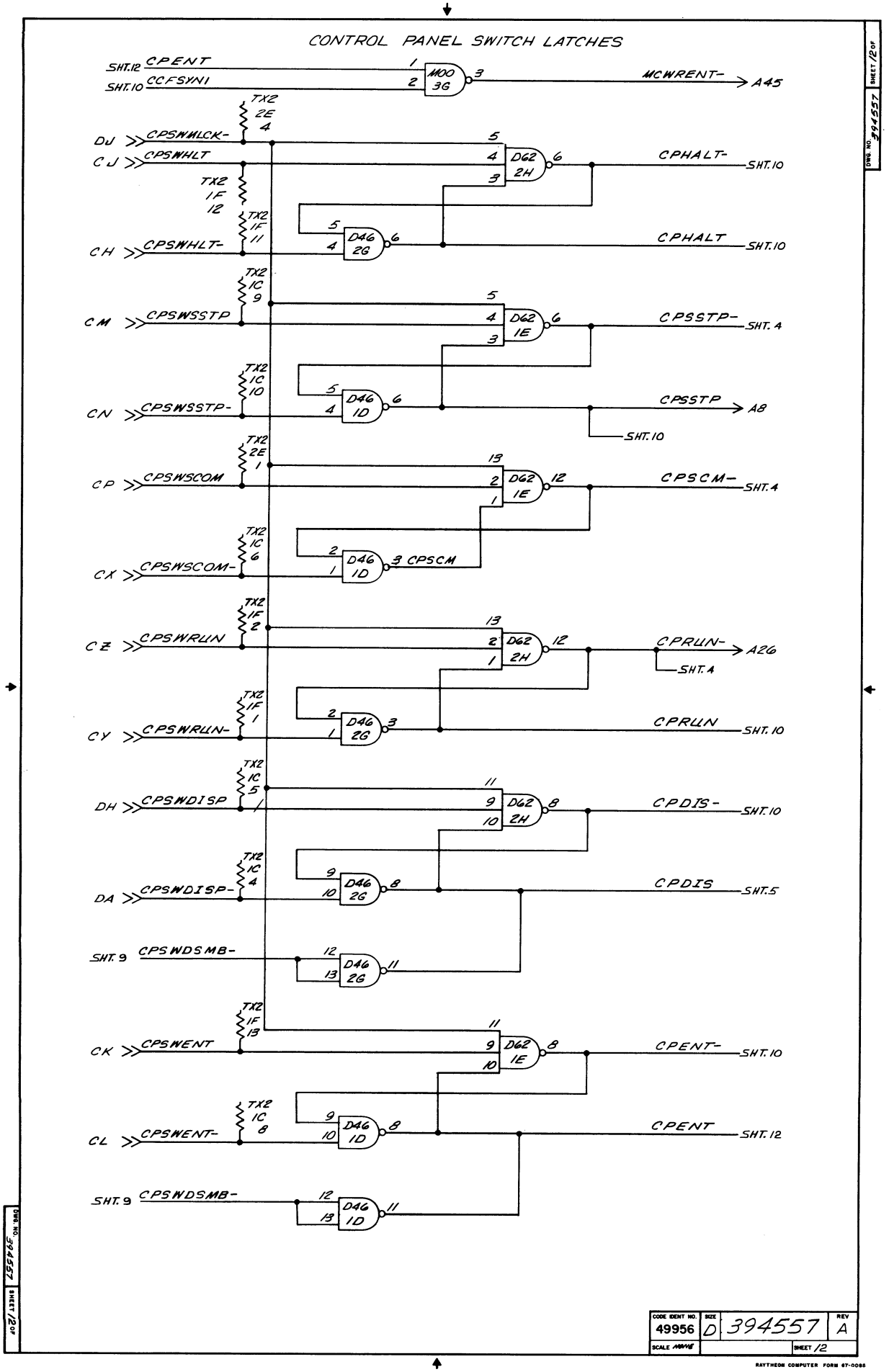
CODE IDENT NO.	SIZE		REV
49956	D	394557	A
SCALE NONE		SHEET 8	

RAYTHEON COMPUTER FORM 67-0085

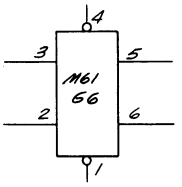

PROGRAM COUNTER CONTROL LOGIC
RESET LOGIC
T4SCDC1
INDCIOR2
SCDC5
INDCØ
SCDCC
TIRC1
INDCXSKIP
MCENB2
SCDCIA
PCLDAD2-4
PCLDADI-
SCDCD-
CCFSKP-
PCLDAD
CPSWDCLR-
CPDCLR
CPSWDSAC-
CPDSAC
ACRDR-
CPSWDSMB-
CPDSMB
MBRDR-
CPSWDSIX-
CPDSIX
IXRDR-
KKSYNA
CPSWRST-
CCFRST-
CCFRST
CR3
509577-001
PFRST-
PCRDR-
CPSWPCLR-
MRESET-
R1
390Ω
1/4W, ±5%
+5V
DWG. NO. 394557
SHEET 9 OF
CODE IDENT NO. 49956
SIZE D
394557
REV A
SCALE NONE
SHEET 9
RAYTHEON COMPUTER FORM 67-0088

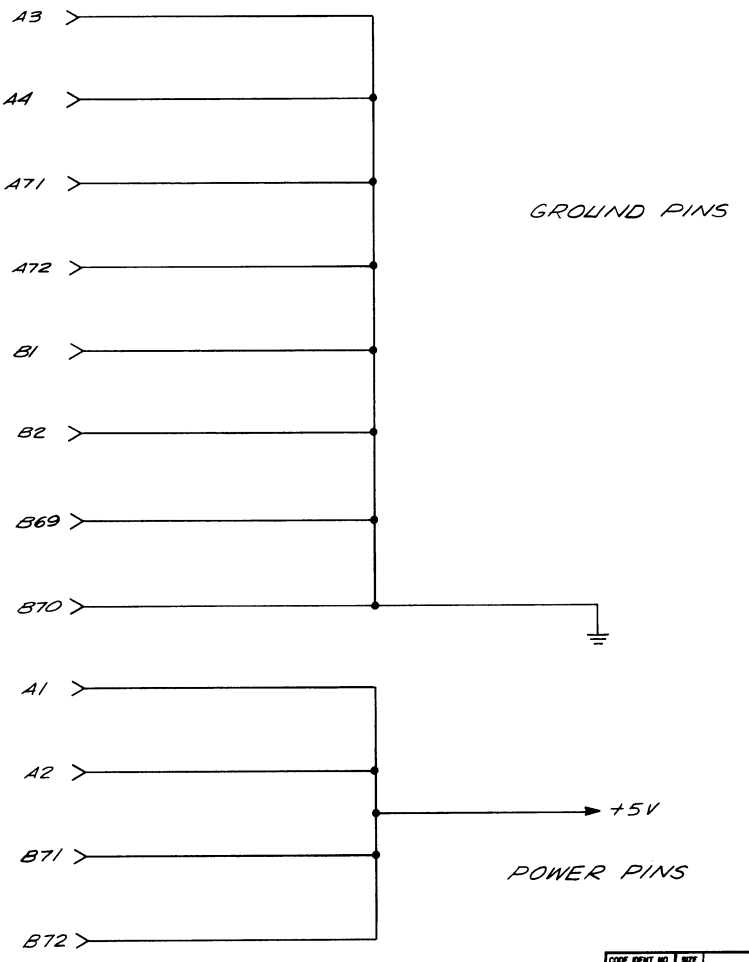

P/O RESET LOGIC
CCFRST
SHT. 9
D58 3F
CR1
503577-001
REXT1-
A66
CR2
PFRST-
SHT. 9
503577-001
REXT2-
A64
+5 V
R2 1K 1/4 W ±5%
RUN, SINGLE-STEP AND SYNC CONTROL LOGIC
PARER-
B55
CPSWRST-
SHT. 9
M01 7G
CCFRUNDS-
SCDCIA
INDC0000
SHT. 4
M00 3A
CCFRUNI
CCFSSTPR-
SHT. 10
M00 3A
CCFRUNR
KKMCENMA
SHT. 7
M61 6G
CCFRUN-
SHT. 10
D58 6H
CPHLTL-
DR
SHT. 12
CPRUNENB-
DS
CPRUNL-
DN
CPRUN
CCFSYNI
SHT. 12
SHT. 10
M01 7G
CCFRUNS
CCPRUN
CPSSTP
CCFSSTPS
CCFSSTP
CPSSTPL-
DP
CPHALT
CCFSSTPR-
M02 6F
CCFSSTPR
CCFSSTP-
B34
KKSYN
M61 5H
CPSWRST-
CCFSYNI-
CCFSYN2-
M01 4H
CCSYNIS
A43
SHT. 4,5,10,11,12
CPDIAEN
SCDCIFØ
M02 6F
CCFSYNI2
CPHALT-
M00 5G
CCFSYNII
CCFCLK
SHT. 7
M06 5E
CCFSYNIS
KKSYNA
M60 3E
CCFSYNI
CCFSYN2
NOT USED
CCFSYNII-
D37 2F
TIRC4
SHT. 5
KKBI
SHT. 7
M01 4E
KKSYN
SHT. 10
M00 3G
KKSYNA
SHT. 9,10
CCFRUN-
M00 5G
CCSCM-
SHT. 4
CCFSSTP-
M01 7G
CCSCM
CPDIS-
CPENT-
SHT. 12
M00 3G
SHT. 5,10,11
CPDIAEN
B54
TX2 2E
CPSWDSIN-
CS
D37 2F
SHT. 5
DISPIN
A30
CCFSSTP-
CCFSSTPS
M03 5F
SHT. 7
CCCLKEN
B19
MCENMB
A6
TX2 1C
SHT. 10
SHEET 10 OF
DWG NO. 394557
CODE IDENT NO. 49956
SIZE D
394557
REV B
SCALE NONE
SHEET 10
RAYTHEON COMPUTER FORM 67-0085


SENSE SWITCH LATCHES
DM
CPSWSNSØ
TX3 3H 9
D46 1H
CPSENSØ-
CPSENSØ
A9
CD
CPSWSNSØ-
TX2 1F 8
CC
CPSWSNS1
TX2 1F 6
CPSENS1-
CPSENS1
A11
CB
CPSWSNS1-
TX2 1F 5
CE
CPSWSNS2
TX2 1F 9
D46 1G
CPSENS2-
CPSENS2
A5
CF
CPSWSNS2-
TX2 1F 10
CA
CPSWSNS3
TX2 1F 4
CPSENS3-
CPSENS3
A7
CW
CPSWSNS3-
TX2 1F 3
MISCELLANEOUS LOGIC
SHT.11 SCDC37B-
SHT.5 SCDC90RD-9
M00 3A
ADINCRYD
M04 3C
ADINCRYC-
A39
SHT.5
SHT.5 TIRC4
SHT.4 SCDC1A
M01 4H
T4SCDC1
B51
SHT.9
SHT.4 SCDC3-
SHT.5 SCDC70RB-
SCDC37B-
SHT.5,11
SHT.5 SCDC9
M04 3C
ADENMBA-
A50
SHT.5 SCDCD
SHT.10 CPDIAEN
SHT.10 CCFSYN1
M04 7E
ADENPC2-
B67
SHT.4 SCDCC
DWG. NO. 394557
SHEET // OF
CODE IDENT NO. 49956
SIZE D
394557
REV A
SCALE NONE
SHEET //
RAYTHEON COMPUTER FORM 67-0086


CONTROL PANEL SWITCH LATCHES
SHT.12 CPENT
SHT.10 CCFSYN1
M00 3G
MCWRENT- A45
DJ CPSWHLCK-
CJ CPSWHLT
D62 2H
CPHALT- SHT.10
CH CPSWHLT-
D46 2G
CPHALT SHT.10
CM CPSWSSTP
D62 1E
CPSSTP- SHT. 4
CN CPSWSSTP-
D46 1D
CPSSTP A8
SHT.10
CP CPSWSCOM
CPSCM- SHT.4
CX CPSWSCOM-
3 CPSCM
CZ CPSWRUN
CPRUN- A26
SHT.4
CY CPSWRUN-
CPRUN SHT.10
DH CPSWDISP
CPDIS- SHT.10
DA CPSWDISP-
CPDIS SHT.5
SHT.9 CPSWDSMB-
CK CPSWENT
CPENT- SHT.10
CL CPSWENT-
CPENT SHT.12
SHT.9 CPSWDSMB-
DWG NO 394557 SHEET 12 OF
DWG NO 394557 SHEET 12 OF
CODE IDENT NO. 49956
SIZE D
394557
REV A
SCALE
SHEET 12
RAYTHEON COMPUTER FORM 67-0088

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	394557	A
SCALE NONE			SHEET 13

SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER E.O. 19084			M.F.	N.B.	F.A.	3/26/70
X2	REVISED PER E.O. 20823			M.F.	N.B.	N.B.	4/28/70
A	RELEASED PER E.O. 19311			M.F.	N.B.	N.B.	5/26/70
B	REVISED PER E.O. 21601			R	N.B.	N.B.	9/20/70

RESERVE EO'S OUTSTANDING

SHEET 1 OF · DWG. NO. 394562

TABLE OF CONTENTS

GLOSSARY

ACDLY	DMA ACCESSING MEMORY
ACLDAD3	LOAD THE ADDER INTO ACCUMULATOR
ACRZERO	ACCUMULATOR READING ALL ZEROS
ADFEQL	ADDER FUNCTION EQUAL
ADFNEG	ADDER FUNCTION NEGATIVE
ADFOVF	OVER-FLOW IN THE ADDER BUS
CCCLKEN	CPU NOT PERFORMING A SINGLE-STEP OPERATION
CCCMEND3-7	END OF COMMAND
CCFBYTE	CONTROL F/F BYTE OPERATION
CCFCLK	DMA NOT ACCESSING MEMORY
CCFSKP	SKIP INSTRUCTION
CCFSSTP	CPU NOT IN SINGLE-STEP MODE
CCFSYN1	ENABLE FOR 1 MEMORY CYCLE
CPDIAEN	DISPLAY OR ENTER FUNCTION ENABLED
CPSENSØ-3	SENSE SWITCHES SET FROM CONTROL PANEL
CPSSTP	ENABLE SINGLE-STEP FUNCTION
EXLDMB	LOAD MEMORY BUFFER INTO EXR
EXSENS	SET CCFSKP WITH EXTERNAL SENSE
ICDCØ	ITERATION COUNTER AT ZERO
ICDECOPT	DECREMENT ITERATION COUNTER WITH OPTIONS
ICRO-3	ITERATION COUNTER OUTPUTS
INDCOB	SKIP DECODED STATE FROM INR
INDCBYTE	BYTE COMMAND FROM INR
INDCXXØ-F	OUTPUT DECODED INSTRUCTIONS
KKGAT	GATED CLOCK TO 704 SYSTEM
KKUNG	UNGATED CLOCK TO 704 SYSTEM
MACLKEN	CLOCK ENABLE FOR MEMORY ENABLES
MALDPC	LOAD PROGRAM COUNTER TO MEMORY ADDRESS
MARØ1S-Ø3S	SET ADDRESS LINES TO MAR
MARDRL	MEMORY ENABLES RESET TO 'Ø'
MBLDADLB	LOAD THE ADDER INTO MBR (LEFT BYTE)
MBLDADRB	LOAD THE ADDER INTO MBR (RIGHT BYTE)
MBLDMCLB	LOAD OUTPUT FROM MEMORY TO MBR (LEFT BYTE)
MBLDMCRB	LOAD OUTPUT FROM MEMORY TO MBR (RIGHT BYTE)
MBRØ8-11	DATA OUT FROM MBR
MBRDR	DIRECT RESET TO MBR
MCENMAS	ENABLE MEMORY ADDRESS
MCFENO-3	MEMORY ENABLE TO INDIVIDUAL 4K STACKS
MCFINT	ENABLE MEMORY INHIBIT FUNCTION
MCFRET	ENABLE MEMORY READ FUNCTION
MCFWRT	ENABLE MEMORY WRITE FUNCTION
MCRW	ENABLE READ OR WRITE FUNCTION TO MEMORY
MCWRENT	ENTER DATA FROM CONTROL PANEL TO MEMORY
MTO-2-4	BUFFERED OUTPUTS FROM TIMING COUNTER
OPTRDWR	ENABLE READ OR WRITE FROM 704 OPTIONS
TIRCO-4	OUTPUTS FROM TIMING COUNTER

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
DEC	531667-001
M00	531593-006
M01	531593-005
M02	531593-007
M03	531593-008
M04	531593-014
M05	531593-004
M06	531593-017
M07	531593-015
M10	531593-002
M12	531593-016
M26	531593-012
M60/M60A	531593-018
M61	531593-011
TX3	531596-002

NOTES: UNLESS OTHERWISE SPECIFIED

1. → DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR
2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

DWG. NO. 394562 · SHEET 1 OF

SHEET	1	2	3	4	5	6	7	8	9	10	11	12
REVISION	B	A	A	A	A	A	A	A	A	A	B	A

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX

FINISH:

DRAWN M.A. Fogel 3-25-70
CHECK N. Bartha
APPR
APPR

NEXT ASSY N/A

RAYTHEON — RAYTHEON COMPANY, LEXINGTON, MASSACHUSETTS 02173

MEMORY CONTROL (LOGIC DIAGRAM)

CODE IDENT NO. 49956 · SIZE · 394562

SCALE NONE · SHEET 1 OF 12

RAYTHEON COMPUTER FORM

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACDLY-		A49	4
ACLOAD3A-	S	A6	9
ACR00		A15	7
ACR00-		A13	7
ACR15-		A16	7
ACRZEROϕ		A56	7
ACRZERO12		A51	7
ACRZERO4		A54	7
ACRZERO8		A53	7
ADFEQL		A24	7
ADFEQL-		A23	7
ADFNEG-		A19	7
ADFOVF		A32	7
CCCLKEN		B61	10
CCFBYTE-		A64	4
CCFCLK		B60	10
CCFRST-		B32	5
CCFSKP	S	A10	11
CCFSKP-	S	A8	11
CCFSSTP-		B3	4
CCFSYN1		B6	4
CCCMEND3-	S	B48	9
CCCMEND7-	S	B23	9
CPDIAEN		B4	4
CPSENSϕ		A36	11
CPSENS1		A38	11
CPSENS2		A40	11
CPSENS3		A37	11
CPSSTP		A69	4
DADϕ8-	S	A48	9
DADϕ9-	S	A47	9
DAD10-	S	A65	9
DAD11-	S	A66	9
EXLDMB	S	B63	5
EXSENS-		A60	11
ICDCO	S	B66	8
ICDCO-	S	B68	8
ICDECOPT-		B50	8
ICR1-	S	B16	8
ICR2-	S	B11	8
ICR3-	S	B64	8
ICR0-	S	B28	8
INDC$\phi\phi\phi$	S	A18	9
INDC$\phi\phi$2	S	A17	9
INDC$\phi\phi$4	S	A2ϕ	9
INDC$\phi\phi$5	S	A22	9
INDC$\phi\phi$A	S	A31	9
INDC$\phi\phi$B	S	A34	9
INDC$\phi\phi$X-		B24	9
INDCϕ8-		A45	11
INDCBYTE		A61	4
INDCXX0-	S	A14	9
INDCXX1-	S	A12	9
INDCXX2-	S	A11	9
INDCXX3-	S	A9	9
INDCXX4-	S	A26	9
INDCXX5-	S	A28	9
INDCXX6-	S	A25	9
INDCXX7-	S	A27	9
INDCXX8-	S	B3ϕ	9
INDCXX9-	S	B37	9
INDCXXA-	S	A3ϕ	9
INDCXXB-	S	A29	9
INDCXXC-	S	A39	9
INDCXXD-	S	A41	9
INDCXXE-	S	A42	9

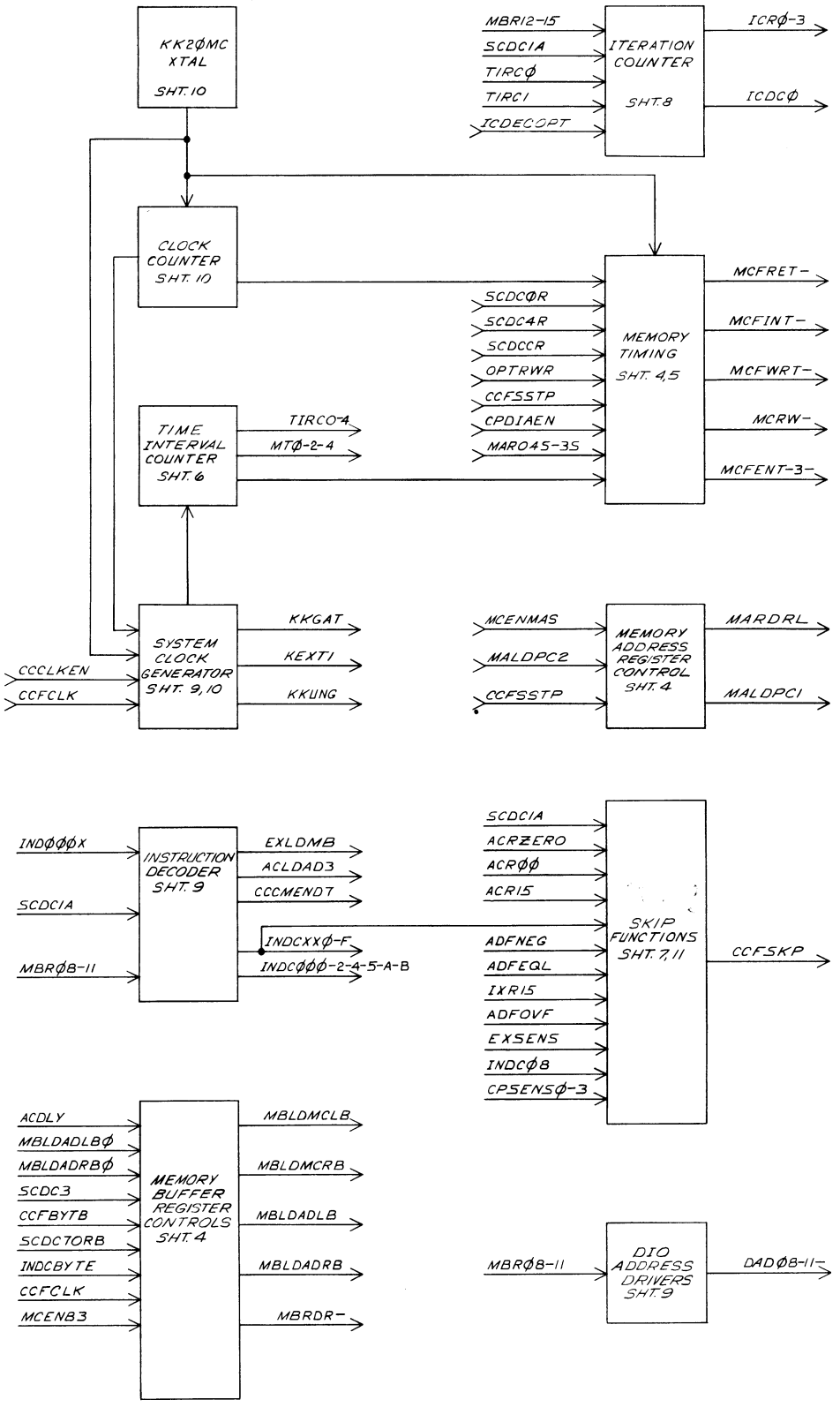
SIGNAL LIST

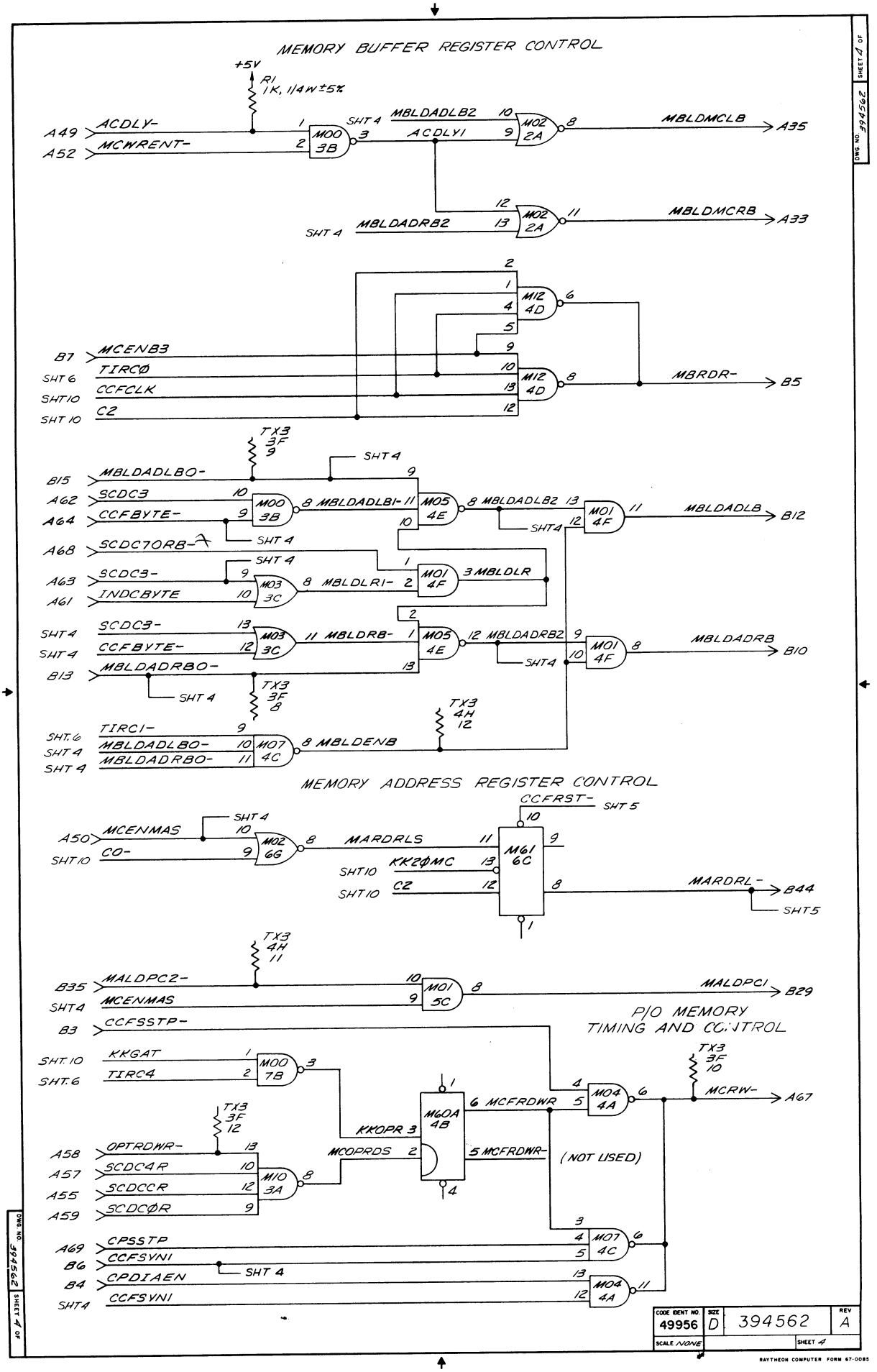
SIGNAL	SOURCE	CONN	SHEET
INDCXXF-	S	A44	9
IXR15-		A21	7
KEXTI-	S	B53	10
KK2	S	B56	10
KK3	S	B54	10
KK4	S	B58	10
KKA	S	B55	10
KKB	S	B57	10
KKC	S	B59	10
MACLKEN		B51	5
MALDPC1	S	B29	4
MALDPC2-		B35	4
MAR01S		B52	5
MAR02S		B65	5
MAR03S		B67	5
MARDRL-	S	B44	4
MBLDADLB	S	B12	4
MBLDADLBO-		B15	4
MBLDADRB	S	B1ϕ	4
MBLDADRBO-		B13	4
MBLDMCLB	S	A35	4
MBLDMCRB	S	A33	4
MBRϕ8-		A43	9
MBRϕ9-		A46	9
MBR10-		A5	9
MBR11-		A7	9
MBR12-		B38	8
MBR13-		B4ϕ	8
MBR14-		B41	8
MBR15-		B36	8
MBRDR-	S	B5	4
MCENB3		B7	4
MCENMAS		A5ϕ	4
MCFENϕ-	S	B26	5
MCFEN1-	S	B45	5
MCFEN2-	S	B47	5
MCFEN3-	S	B42	5
MCFINT-	S	B27	5
MCFRET-	S	B39	5
MCFWRT-	S	B33	5
MCRW-	S	A67	4
MCWRENT-		A52	4
MRESET-		B43	11
MTϕ-	S	A7ϕ	6
MT2-	S	B9	6
MT4-	S	B62	6
OPTRDWR-		A58	4
SCDCϕR		A59	4
SCDC1A		B34	5
SCDC3		A62	4
SCDC3-		A63	4
SCDC4		B49	8
SCDC4R		A57	4
SCDC7ORB-		A68	4
SCDCCR		A55	4
TIRCO	S	B19	6
TIRCO-	S	B22	6
TIRC1	S	B2ϕ	6
TIRC2	S	B31	6
TIRC2-	S	B46	6
TIRC3-	S	B21	6
TIRC4	S	B17	6
TIRC4-	S	B18	6
TIRCA	S	B25	6

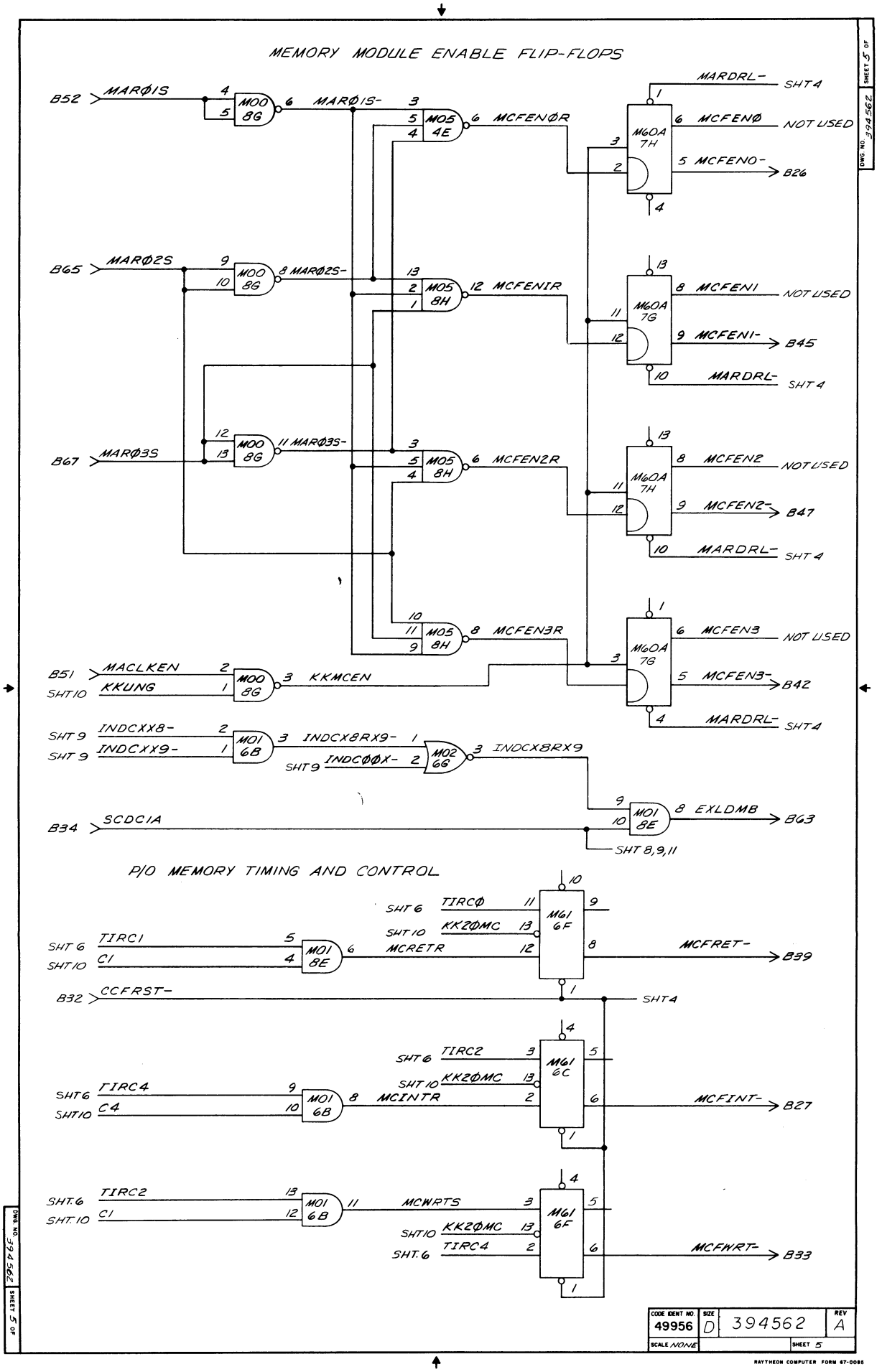
DWG NO 394562 SHEET 2 OF

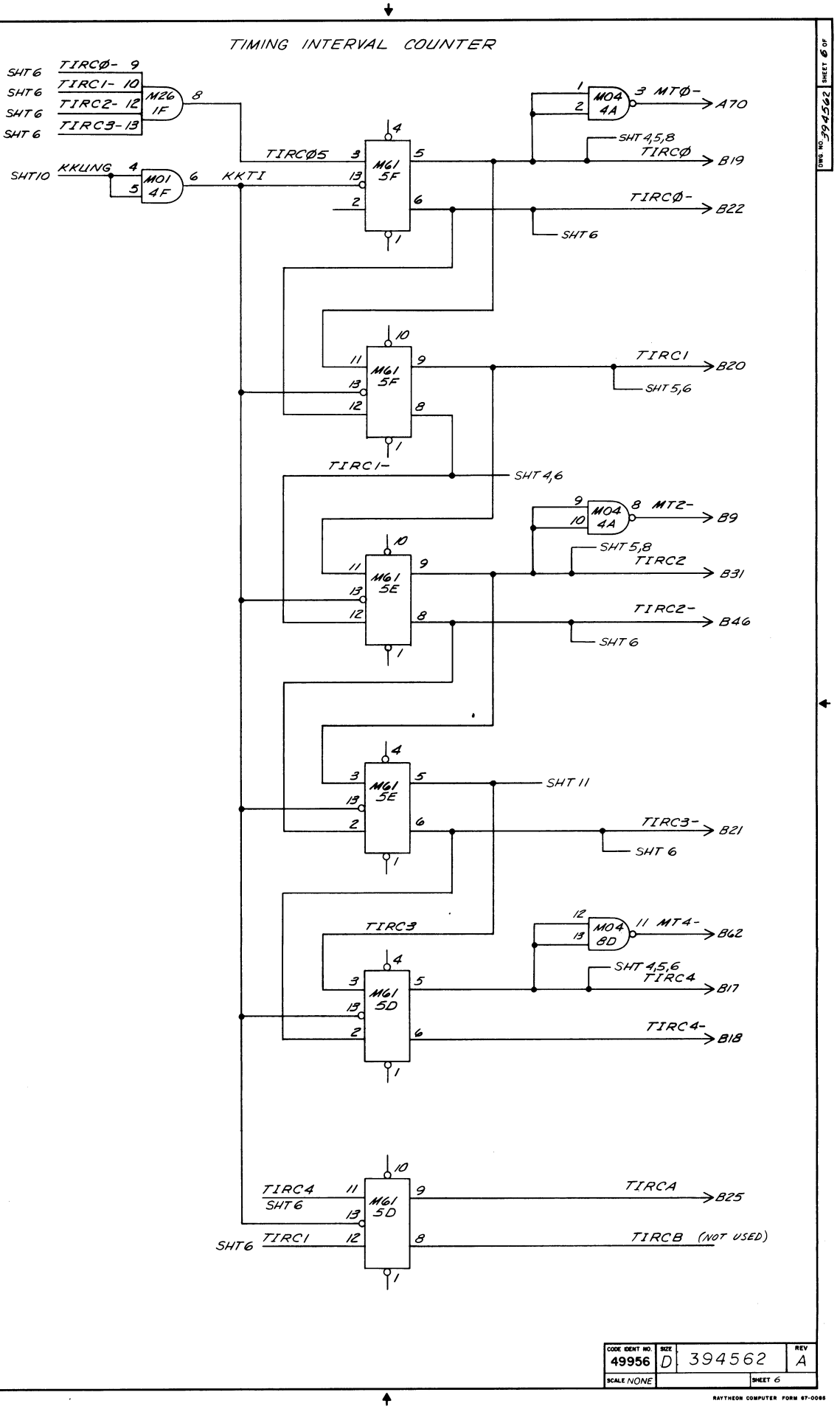
CODE IDENT NO.	SIZE		REV
49956	D	394562	A
SCALE NONE		SHEET 2	

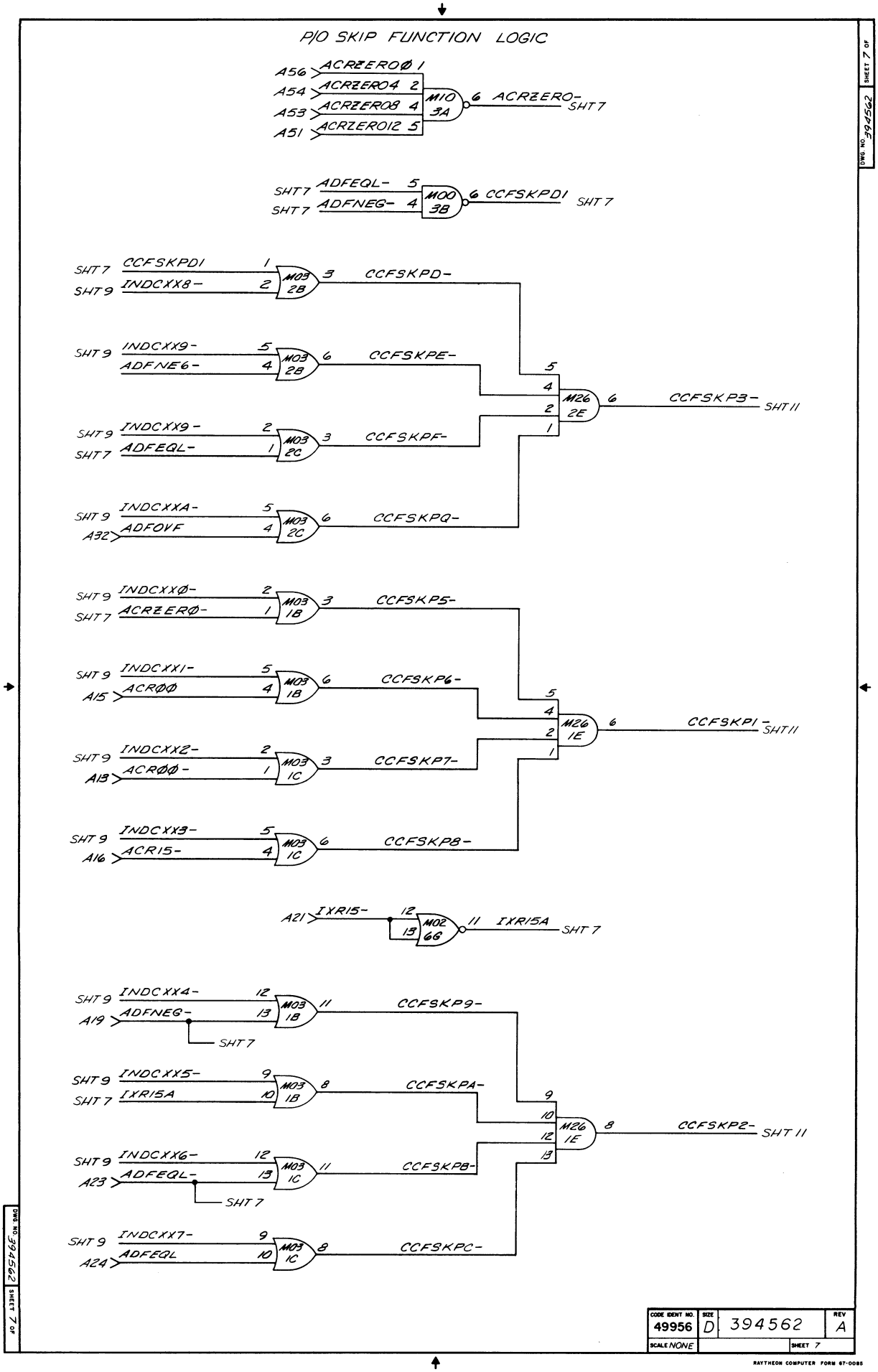
RAYTHEON COMPUTER FORM 67-0085

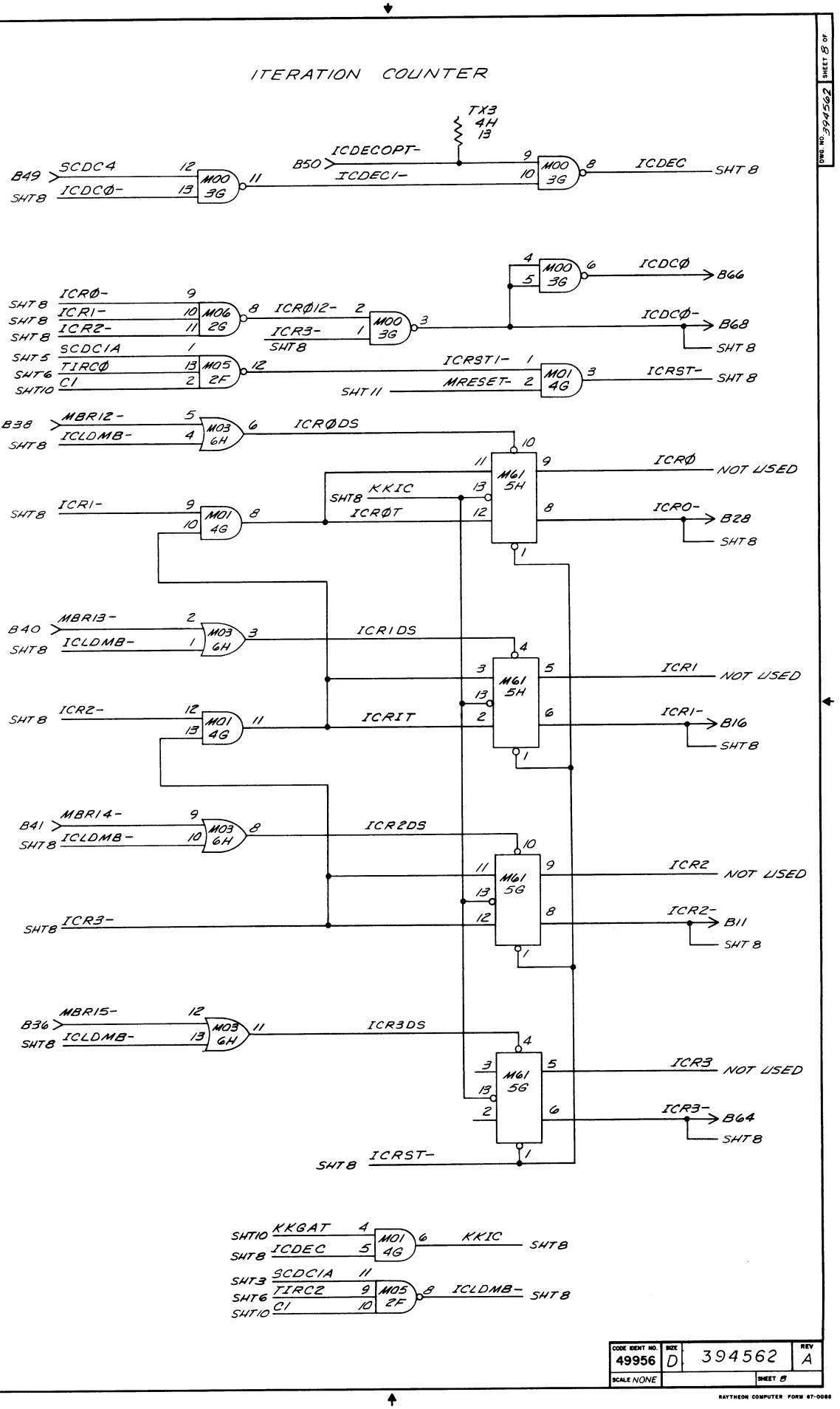

KK2ØMC XTAL SHT. 10
CLOCK COUNTER SHT. 10
TIME INTERVAL COUNTER SHT. 6
SYSTEM CLOCK GENERATOR SHT. 9, 10
CCCLKEN
CCFCLK
KKGAT
KEXTI
KKUNG
TIRCO-4
MTØ-2-4
MBRI2-15
SCDC1A
TIRCØ
TIRC1
ICDECOPT
ITERATION COUNTER SHT. 8
ICRØ-3
ICDCØ
SCDCØR
SCDC4R
SCDCCR
OPTRWR
CCFSSTP
CPDIAEN
MARØ45-35
MEMORY TIMING SHT. 4,5
MCFRET-
MCFINT-
MCFWRT-
MCRW-
MCFENT-3-
MCENMAS
MALDPC2
CCFSSTP
MEMORY ADDRESS REGISTER CONTROL SHT. 4
MARDRL
MALDPC1
INDØØØX
SCDC1A
MBRØ8-11
INSTRUCTION DECODER SHT. 9
EXLDMB
ACLDAD3
CCCMENDT
INDCXXØ-F
INDCØØØ-2-4-5-A-B
SCDC1A
ACRZERO
ACRØØ
ACR15
ADFNEG
ADFEQL
IXR15
ADFOVF
EXSENS
INDCØ8
CPSENSØ-3
SKIP FUNCTIONS SHT. 7, 11
CCFSKP
ACDLY
MBLDADLBØ
MBLDADRBØ
SCDC3
CCFBYTB
SCDCTORB
INDCBYTE
CCFCLK
MCENB3
MEMORY BUFFER REGISTER CONTROLS SHT. 4
MBLDMCLB
MBLDMCRB
MBLDADLB
MBLDADRB
MBRDR-
MBRØ8-11
DIO ADDRESS DRIVERS SHT. 9
DADØ8-11-
DWG. NO. 394562
SHEET 3 OF
CODE IDENT NO. 49956
SIZE D
394562
REV A
SCALE NONE
SHEET 3
RAYTHEON COMPUTER FORM 67-0085


MEMORY BUFFER REGISTER CONTROL
+5V
R1
1K, 1/4W ±5%
A49
ACDLY-
A52
MCWRENT-
M00 3B
SHT 4
MBLDADLB2
ACDLYI
M02 2A
MBLDMCLB
A35
SHT 4
MBLDADRB2
M02 2A
MBLDMCRB
A33
B7
MCENB3
SHT 6
TIRCØ
SHT10
CCFCLK
SHT 10
C2
M12 4D
MBRDR-
B5
TX3 3F 9
B15
MBLDADLBO-
A62
SCDC3
A64
CCFBYTE-
M00 3B
MBLDADLBI-
M05 4E
MBLDADLB2
M01 4F
MBLDADLB
B12
A68
SCDC7ORB-
A63
SCDC3-
A61
INDCBYTE
M03 3C
MBLDLRI-
M01 4F
MBLDLR
SHT4
SCDC3-
SHT4
CCFBYTE-
M03 3C
MBLDRB-
M05 4E
MBLDADRB2
M01 4F
MBLDADRB
B10
B13
MBLDADRBO-
TX3 3F 8
TX3 4H 12
SHT.6
TIRC1-
SHT4
MBLDADLBO-
SHT4
MBLDADRBO-
M07 4C
MBLDENB
MEMORY ADDRESS REGISTER CONTROL
CCFRST-
SHT 5
A50
MCENMAS
CO-
SHT10
M02 6G
MARDRLS
M61 6C
KK2ØMC
C2
MARDRL-
B44
SHT5
TX3 4H 11
B35
MALDPC2-
MCENMAS
M01 5C
MALDPC1
B29
P/O MEMORY TIMING AND CONTROL
B3
CCFSSTP-
SHT.10
KKGAT
SHT.6
TIRC4
M00 7B
KKOPR
M60A 4B
MCOPRDS
MCFRDWR
M04 4A
TX3 3F 10
MCRW-
A67
(NOT USED)
MCFRDWR-
TX3 3F 12
A58
OPTRDWR-
A57
SCDC4R
A55
SCDCCR
A59
SCDCØR
M10 3A
A69
CPSSTP
B6
CCFSYNI
SHT 4
B4
CPDIAEN
SHT4
CCFSYNI
M07 4C
M04 4A
DWG NO. 394562
SHEET 4 OF
SHEET 4 OF
DWG NO. 394562
CODE IDENT NO. 49956
SIZE D
394562
REV A
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0085


MEMORY MODULE ENABLE FLIP-FLOPS
B52 MARØ1S
M00 8G
MARØ1S-
M05 4E
MCFENØR
M60A 7H
MARDRL- SHT 4
MCFENØ NOT USED
MCFENO- B26
B65 MARØ2S
M00 8G
MARØ2S-
M05 8H
MCFENIR
M60A 7G
MCFENI NOT USED
MCFENI- B45
MARDRL- SHT 4
B67 MARØ3S
M00 8G
MARØ3S-
M05 8H
MCFEN2R
M60A 7H
MCFEN2 NOT USED
MCFEN2- B47
MARDRL- SHT 4
M05 8H
MCFEN3R
M60A 7G
MCFEN3 NOT USED
MCFEN3- B42
MARDRL- SHT 4
B51 MACLKEN
SHT 10 KKUNG
M00 8G
KKMCEN
SHT 9 INDCXX8-
SHT 9 INDCXX9-
M01 6B
INDCX8RX9-
SHT 9 INDCØØX-
M02 6G
INDCX8RX9
B34 SCDC1A
M01 8E
EXLDMB B63
SHT 8,9,11
P/O MEMORY TIMING AND CONTROL
SHT 6 TIRCØ
SHT 10 KKZØMC
M61 6F
MCRETR
M01 8E
SHT 6 TIRC1
SHT 10 C1
MCFRET- B39
B32 CCFRST-
SHT 4
SHT 6 TIRC2
SHT 10 KKZØMC
M61 6C
MCINTR
M01 6B
SHT 6 TIRC4
SHT 10 C4
MCFINT- B27
SHT 6 TIRC2
SHT 10 C1
M01 6B
MCWRTS
SHT 10 KKZØMC
SHT 6 TIRC4
M61 6F
MCFWRT- B33
DWG NO. 394562
SHEET 5 OF
CODE IDENT NO. 49956
SIZE D
394562
REV A
SCALE NONE
SHEET 5
RAYTHEON COMPUTER FORM 67-0085


TIMING INTERVAL COUNTER
SHT 6 TIRCØ- 9
SHT 6 TIRC1- 10
SHT 6 TIRC2- 12
SHT 6 TIRC3- 13
M26 1F
8
SHT10 KKUNG 4
5
M01 4F
6
KKTI
TIRCØ5
M61 5F
M04 4A
3 MTØ-
A70
SHT 4,5,8
TIRCØ
B19
TIRCØ-
B22
SHT 6
TIRC1
B20
SHT 5,6
TIRC1-
SHT 4,6
M04 4A
8 MT2-
B9
SHT 5,8
TIRC2
B31
TIRC2-
B46
SHT 6
M61 5E
SHT 11
TIRC3-
B21
SHT 6
TIRC3
M04 8D
11 MT4-
B62
SHT 4,5,6
TIRC4
B17
TIRC4-
B18
M61 5D
TIRC4
SHT 6
TIRCA
B25
SHT 6
TIRC1
TIRCB (NOT USED)
DWG NO 394562 SHEET 6 OF
CODE IDENT NO 49956
SIZE D
394562
REV A
SCALE NONE
SHEET 6
RAYTHEON COMPUTER FORM 67-0085

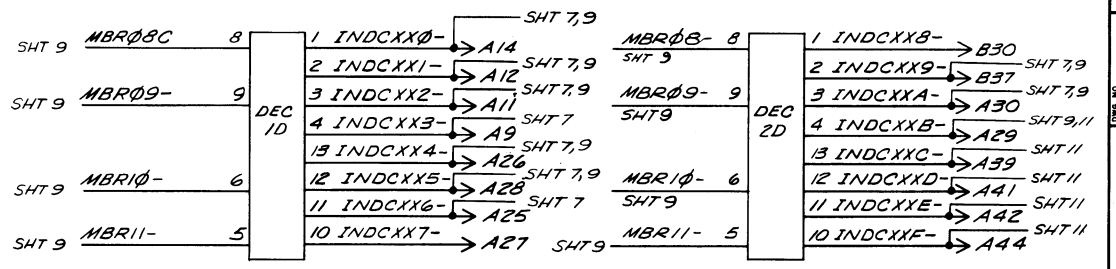

P/O SKIP FUNCTION LOGIC
A56 ACRZERØØ 1
A54 ACRZERO4 2
A53 ACRZERO8 4
A51 ACRZERO12 5
M10 3A
6 ACRZERO- SHT 7
SHT 7 ADFEQL- 5
SHT 7 ADFNEG- 4
M00 3B
6 CCFSKPDI SHT 7
SHT 7 CCFSKPDI 1
SHT 9 INDCXX8- 2
M03 2B
3 CCFSKPD-
SHT 9 INDCXX9- 5
ADFNE6- 4
M03 2B
6 CCFSKPE-
SHT 9 INDCXX9- 2
SHT 7 ADFEQL- 1
M03 2C
3 CCFSKPF-
SHT 9 INDCXXA- 5
A32 ADFOVF 4
M03 2C
6 CCFSKPQ-
5
4
2
1
M26 2E
6 CCFSKP3- SHT 11
SHT 9 INDCXXØ- 2
SHT 7 ACRZERØ- 1
M03 1B
3 CCFSKP5-
SHT 9 INDCXX1- 5
A15 ACRØØ 4
M03 1B
6 CCFSKP6-
SHT 9 INDCXX2- 2
A18 ACRØØ- 1
M03 1C
3 CCFSKP7-
SHT 9 INDCXX3- 5
A16 ACR15- 4
M03 1C
6 CCFSKP8-
5
4
2
1
M26 1E
6 CCFSKP1- SHT 11
A21 IXR15- 12
13
M02 6G
11 IXR15A SHT 7
SHT 9 INDCXX4- 12
A19 ADFNEG- 13
SHT 7
M03 1B
11 CCFSKP9-
SHT 9 INDCXX5- 9
SHT 7 IXR15A 10
M03 1B
8 CCFSKPA-
SHT 9 INDCXX6- 12
A23 ADFEQL- 13
SHT 7
M03 1C
11 CCFSKPB-
SHT 9 INDCXX7- 9
A24 ADFEQL 10
M03 1C
8 CCFSKPC-
9
10
12
13
M26 1E
8 CCFSKP2- SHT 11
DWG NO. 394562 SHEET 7 OF
DWG NO. 394562 SHEET 7 OF
CODE IDENT NO. 49956
SIZE D
394562
REV A
SCALE NONE
SHEET 7
RAYTHEON COMPUTER FORM 67-0085

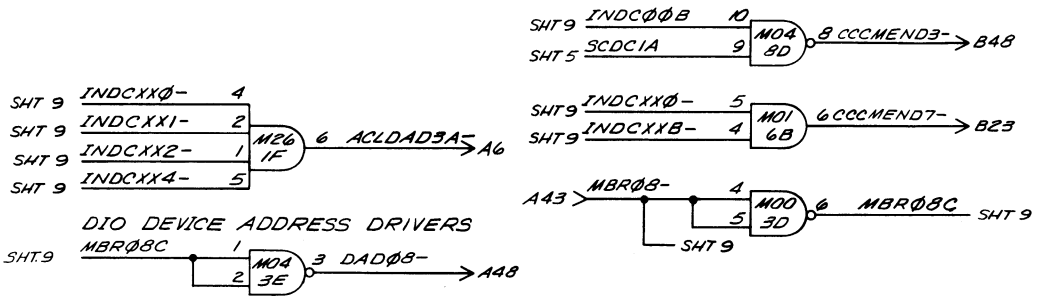


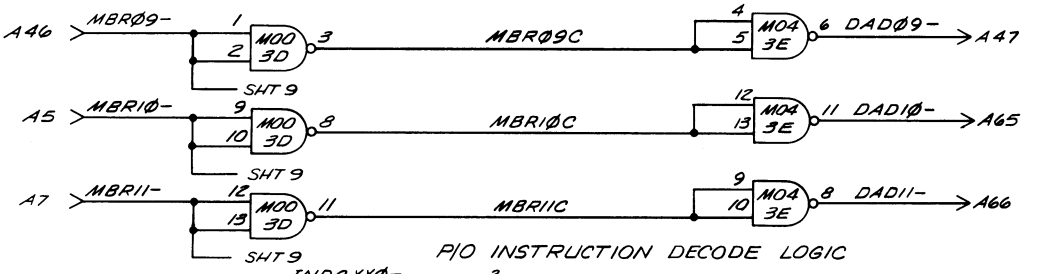
CODE IDENT NO.	SIZE		REV
49956	D	394562	A
SCALE NONE		SHEET 8	

RAYTHEON COMPUTER FORM 67-0088

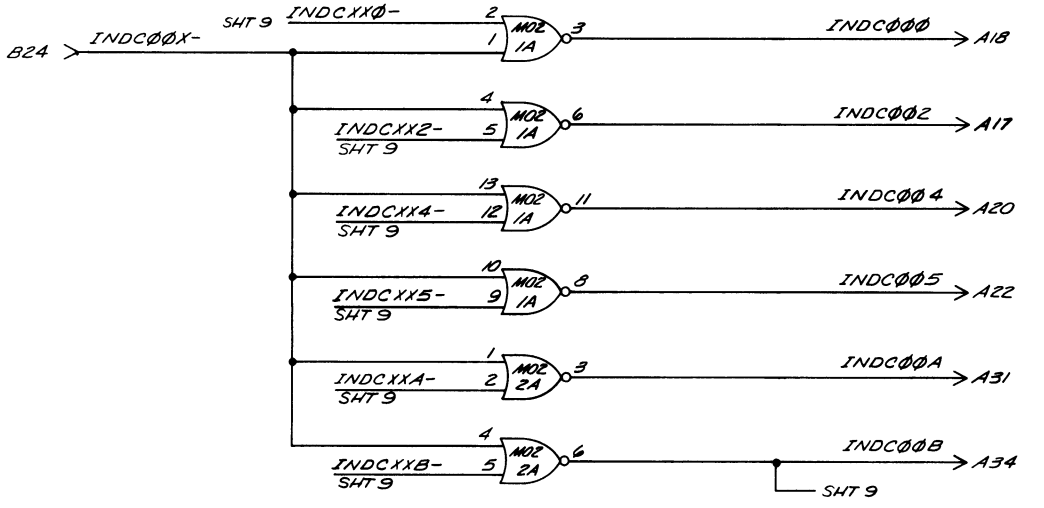
P/O INSTRUCTION DECODE LOGIC



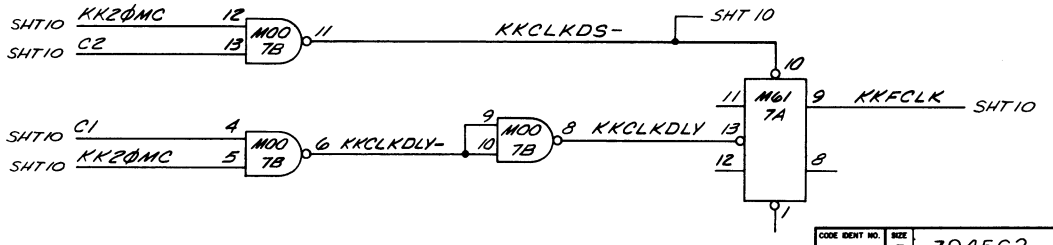




P/O INSTRUCTION DECODE LOGIC



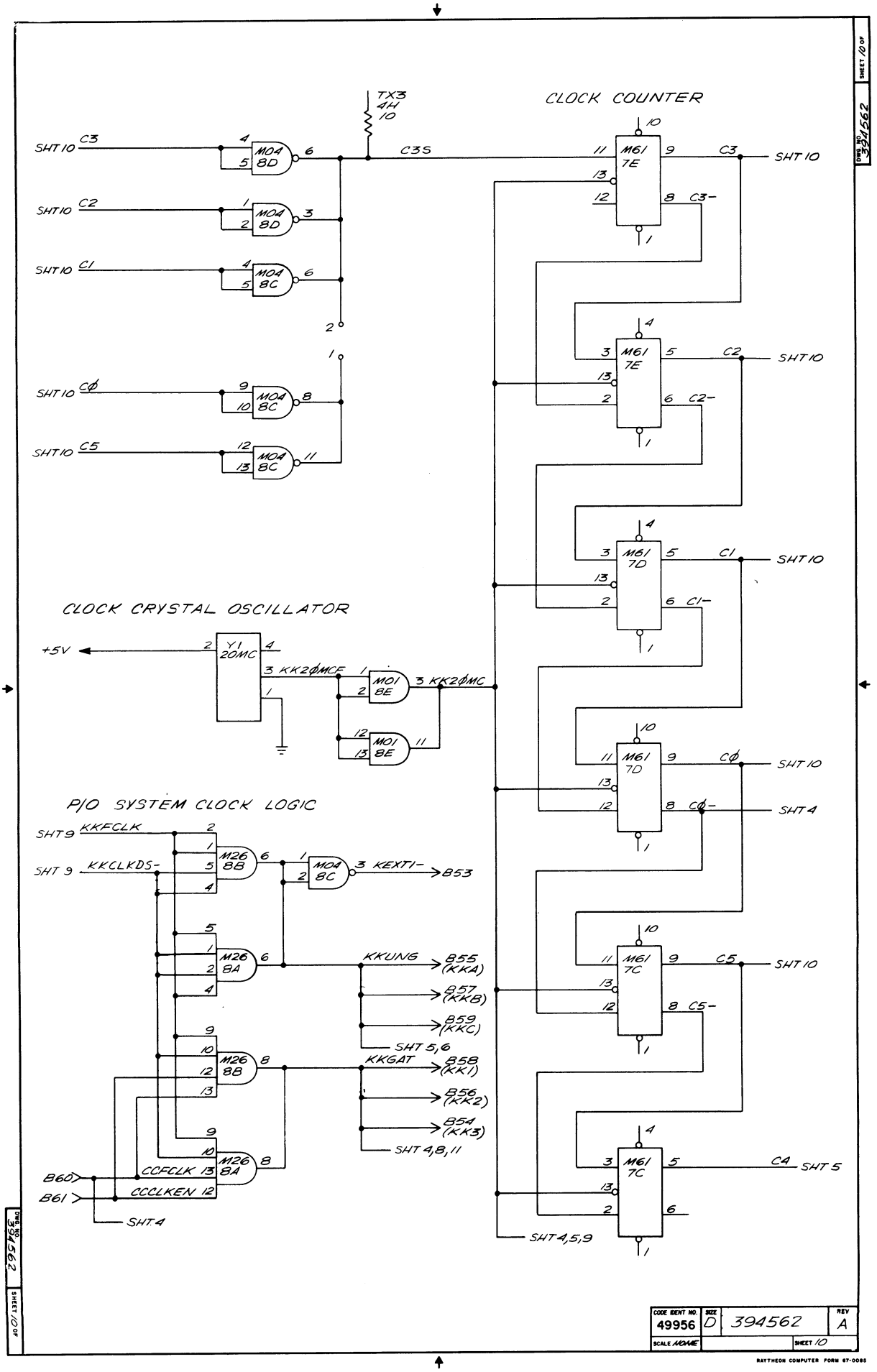
P/O SYSTEM CLOCK LOGIC

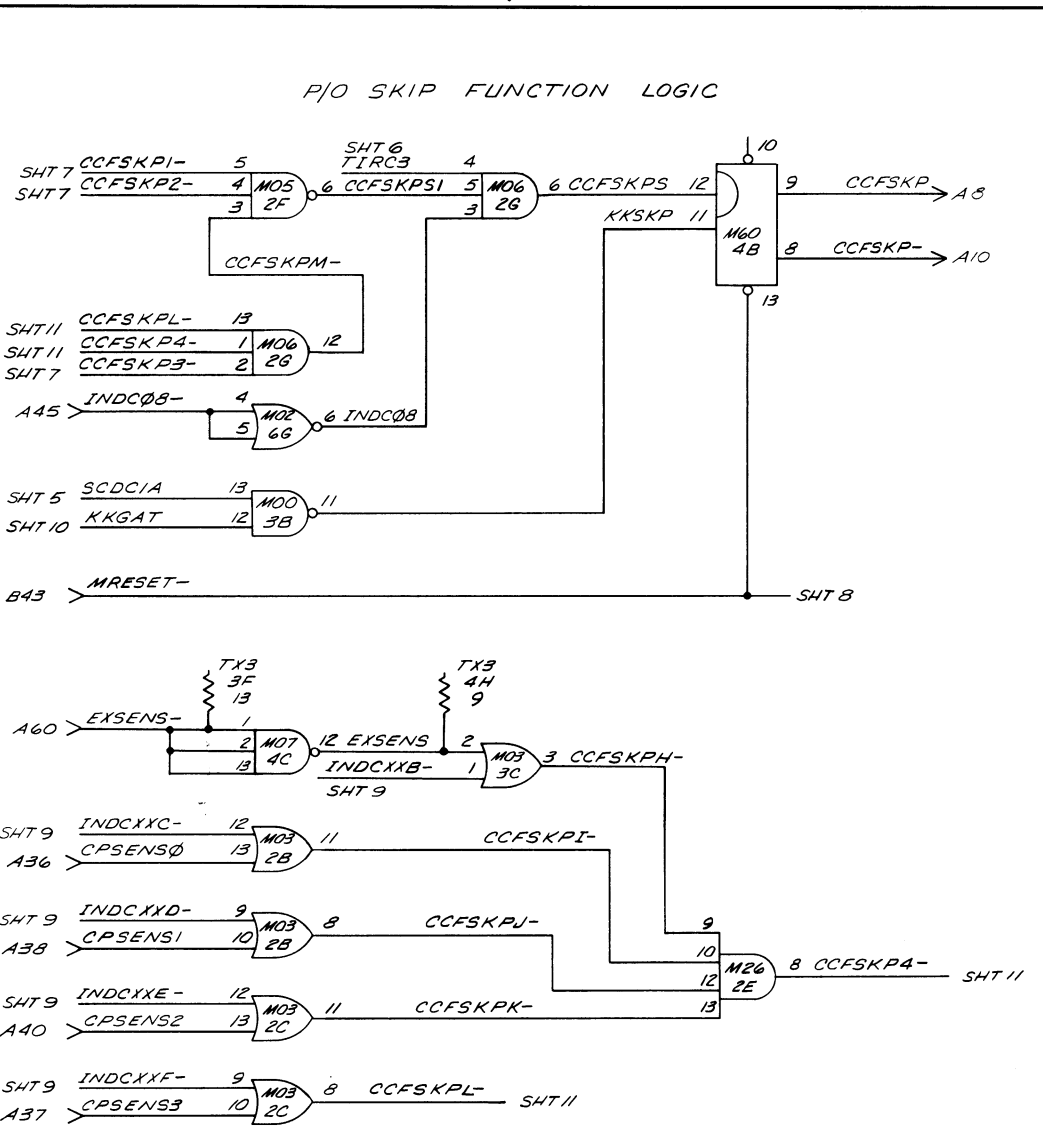


DWG. NO. 394562 SHEET 9 OF

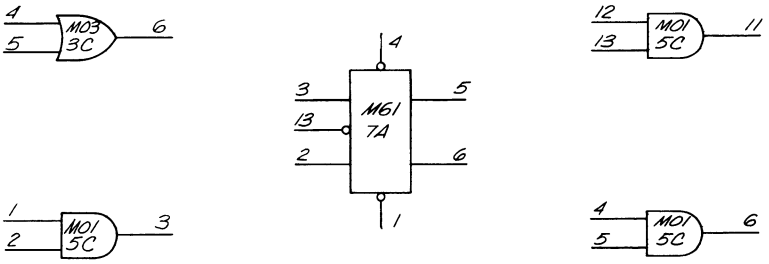
CODE IDENT NO.	SIZE		REV
49956	D	394562	A
SCALE NONE		SHEET 9	

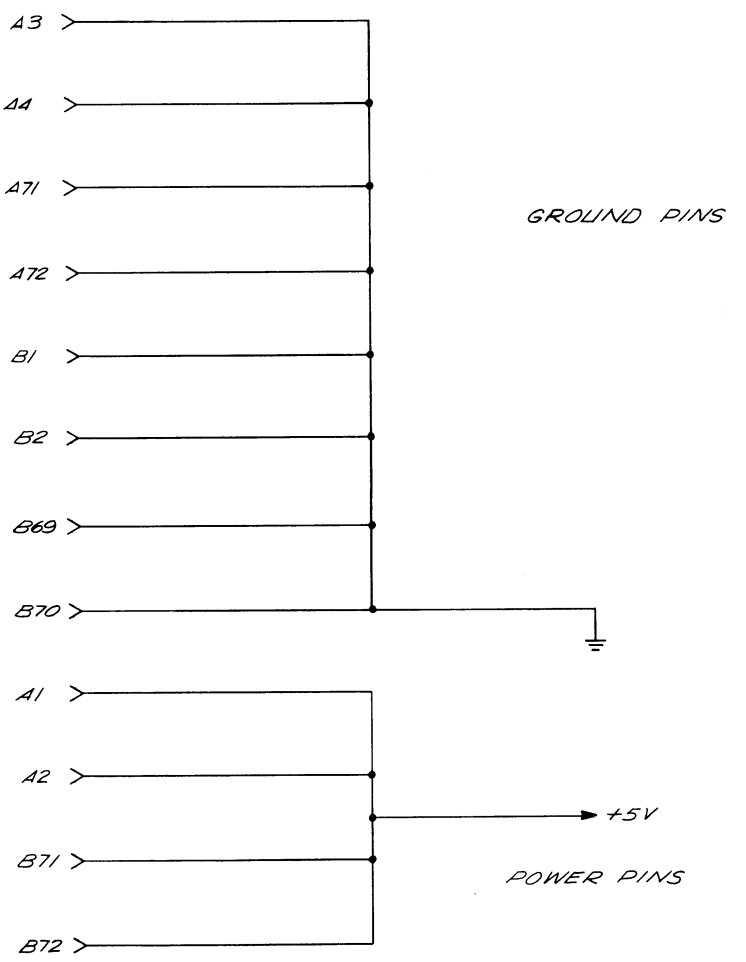
RAYTHEON COMPUTER FORM 87-0088


CLOCK COUNTER
CLOCK CRYSTAL OSCILLATOR
P/O SYSTEM CLOCK LOGIC
TX3 4H 10
SHT10 C3
SHT10 C2
SHT10 C1
SHT10 CØ
SHT10 C5
M04 8D
M04 8C
C3S
M61 7E
M61 7D
M61 7C
C3
C3-
SHT 10
C2
C2-
C1
C1-
CØ
CØ-
SHT 4
C5
C5-
C4
SHT 5
SHT4,5,9
+5V
Y1 20MC
3 KK2ØMCF
M01 8E
3 KK2ØMC
SHT9 KKFCLK
SHT 9 KKCLKDS-
M26 8B
M04 8C
3 KEXTI-
B53
M26 8A
KKUNG
B55 (KKA)
B57 (KKB)
B59 (KKC)
SHT 5,6
M26 8B
KKGAT
B58 (KK1)
B56 (KK2)
B54 (KK3)
SHT 4,8,11
M26 8A
B60
B61
CCFCLK
CCCLKEN
SHT 4
DWG NO. 394562
SHEET 10 OF
CODE IDENT NO. 49956
SIZE D
394562
REV A
SCALE NONE
SHEET 10
RAYTHEON COMPUTER FORM 67-0085


P/O SKIP FUNCTION LOGIC
SHT 7 CCFSKP1-
SHT 7 CCFSKP2-
M05 2F
SHT 6 TIRC3
CCFSKPS1
M06 2G
6 CCFSKPS
M60 4B
KKSKP
CCFSKP
A8
CCFSKP-
A10
CCFSKPM-
SHT 11 CCFSKPL-
SHT 11 CCFSKP4-
SHT 7 CCFSKP3-
M06 2G
A45 INDCØ8-
M02 6G
6 INDCØ8
SHT 5 SCDC1A
SHT 10 KKGAT
M00 3B
B43 MRESET-
SHT 8
TX3 3F 13
TX3 4H 9
A60 EXSENS-
M07 4C
12 EXSENS
INDCXXB-
SHT 9
M03 3C
3 CCFSKPH-
SHT 9 INDCXXC-
A36 CPSENSØ
M03 2B
CCFSKPI-
SHT 9 INDCXXD-
A38 CPSENS1
M03 2B
CCFSKPJ-
SHT 9 INDCXXE-
A40 CPSENS2
M03 2C
CCFSKPK-
M26 2E
8 CCFSKP4-
SHT 11
SHT 9 INDCXXF-
A37 CPSENS3
M03 2C
CCFSKPL-
SHT 11
DWG NO. 394562 SHEET 11 OF
DWG NO. 394562 SHEET 11 OF
CODE IDENT NO. 49956
SIZE D
394562
REV B
SCALE NONE
SHEET 11
RAYTHEON COMPUTER FORM 67-0085

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	394562	A
SCALE NONE		SHEET 12	

RAYTHEON COMPUTER FORM 67-0085

RESERVE EO'S OUTSTANDING

REVISIONS

SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER EO. 19085			[illegible]	N.B.	RA	[illegible]
X2	REVISED PER E.O. 20914			[illegible]	N.B.	N.B.	[illegible]
X3	REVISED PER E.O. 20824			[illegible]	N.B.	[illegible]	[illegible]
A	RELEASED PER E.O. 19311		✓	[illegible]	N.B.	N.B.	[illegible]
B	REVISED PER E.O. 21426			BR	[illegible]	[illegible]	7-7-70

SHEET 1 OF 12 — DWG. NO. 394567

TABLE OF CONTENTS

GLOSSARY

ACRXX	ACCUMULATOR REGISTER BIT XX
ADAXX	ADDER GATE A BIT XX
ADBXX	ADDER GATE B BIT XX
ADBZEROX	ADDER SUM OUTPUT FROM CARD X IS ZERO
ADENMBC3	ENABLE ADDER WITH MEMORY BUFFER COMPLEMENT FOR COMPARE LITERAL BYTE
ADFEQL	ADDER EQUAL FLIP-FLOP
ADFNEG	ADDER NEGATIVE FLIP-FLOP
ADFOVF	ADDER OVERFLOW FLIP-FLOP
ADFOVFR	ADDER OVERFLOW RESET FLIP-FLOP
ADFOVFS	ADDER OVERFLOW SET FLIP-FLOP
ADORXX-	ADDER OR BIT XX
ADSUMXX-	ADDER SUM BIT XX
CCFBYTE	BYTE OPERATION CONTROL FLIP-FLOP
CCFGLB	GLOBAL MODE CONTROL FLIP-FLOP
CCITCY	INTERRUPT ACTIVE AND UNMASKED
CPSWDISMS	CONTROL PANEL SWITCH DISPLAY MACHINE STATUS
DADXX	DIRECT INPUT/OUTPUT BUS ADDRESS BIT XX
DISB	DIRECT INPUT/OUTPUT BUS INPUT STROBE
DISPMS	DISPLAY MACHINE STATUS
DISPXX	CONTROL PANEL DISPLAY BIT XX
DOSB	DIRECT INPUT/OUTPUT BUS OUTPUT STROBE
EXLDAD	EXTENSION REGISTER LOADED FROM ADDER
EXLDADI	EXTENSION REGISTER LOADED FROM ADDER OR INPUT
EXLDADSR	EXTENSION REGISTER LOADED FROM ADDER, SHIFTED RIGHT
EXLDADSRI	EXTENSION REGISTER LOADED FROM ADDER SHIFTED RIGHT OR INPUT
EXLDMB	EXTENSION REGISTER LOADED FROM MEMORY BUFFER REGISTER
EXLDPC	EXTENSION REGISTER LOADED FROM PROGRAM COUNTER
EXRXX	EXTENSION REGISTER BIT XX
ICDCO	ITERATION COUNTER DECODED ZERO
IN4SC5	INSTRUCTION DECODE 4 AND SEQUENCER DECODE STATE 5
INDCXX	INSTRUCTION DECODER OUTPUT XX
INFSC5	INSTRUCTION DECODE F & SEQUENCER DECODE 5
INTRPTOO	INTERRUPT OO
ITOORQ	INTERRUPT OO MOST ACTIVE INTERRUPT
IT15AO1	HIGHER ORDER INTERRUPT ACTIVE (OPT)
ITACT	START INTERRUPT PROCESSING
ITDSB	DISABLE INTERRUPT
ITENB	ENABLE INTERRUPT
ITFINH	INTERRUPT FLIP-FLOP MASK
ITFINHR2	INTERRUPT MASK FLIP-FLOP RESET (OPT)
ITIDLE	INTERRUPT RETURN
ITROOA	INTERRUPT OO REQUESTED
ITROON	INTERRUPT OO ENABLED, BUT NOT PROCESSED
ITSVENB	ENABLE INTERRUPT SERVICE REGISTER
ITWAIT	HIGHER ORDER INTERRUPT AVAILABLE (OPT)
IXCLKENBL	LEFT SEGMENT INDEX REGISTER CLOCK CONTROL
IXCLKENBR	RIGHT SEGMENT INDEX REGISTER CLOCK CONTROL
IXLDAD3	INDEX REGISTER LOAD FROM ADDER INPUT TERM
IXLDADL	LEFT SEGMENT OF INDEX REGISTER LOAD FROM ADDER
IXLDADR	RIGHT SEGMENT OF INDEX REGISTER LOAD FROM ADDER
IXLDPC	INDEX REGISTER LOAD FROM PROGRAM COUNTER
IXR15S	INDEX REGISTER BIT 15 SET TERM
IXSL	INDEX REGISTER SHIFT LEFT
IXSLZRO	ZERO IXR15 ON DOUBLE SHIFT LEFT
IXSR	INDEX REGISTER SHIFT RIGHT
IXSRAC15	COPY ACCUMULATOR REGISTER BIT 15 INTO INDEX REGISTER ON DOUBLE SHIFT RIGHT
KK31	GATED CLOCK OUTPUT 3A REPOWERED
KK3A	GATED CLOCK OUTPUT 3A
MBRXX	MEMORY BUFFER REGISTER BIT XX
MBRXXD	MEMORY BUFFER REGISTER BIT XX REPOWERED
MRESET	MASTER RESET
PCRXX	PROGRAM COUNTER BIT XX
PFSINT	POWER FAILSAFE INTERRUPT (OPT)
PUARI	ARITHMETIC CARD PULL UP
SCDCX	SEQUENCER DECODED STATE X
SCDCXC	SEQUENCER DECODE STATE X REPOWERED
STBINH	OUTPUT STROBE INHIBIT (OPT)
TØ	TIMING INTERVAL REGISTER ZERO REPOWERED
T4C	TIMING INTERVAL REGISTER 4 REPOWERED
T4SCDC1C	TIMING INTERVAL REGISTER STATE 4 & SEQUENCER DECODE STATE 1
T4SCDC5C	TIMING INTERVAL REGISTER 4 & SEQUENCER DECODE STATE 5
TIRCX	TIMING INTERVAL REGISTER BIT X

TABLE I

I.C. DESIGNATION	RAYTHEON PART NUMBER
TX3	531596-002
TX2	531596-001
M61	531593-011
M60/M60A	531593-018
M26	531593-012
M25	531593-009
M12	531593-016
M07	531593-015
M05	531593-004
M04	531593-014
M03	531593-008
M02	531593-007
M01	531593-005
M00	531593-006
D58	531522-001

3. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" CONNECTOR. C1 THRU C22

2. JUMPERS: SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⇉ DENOTES FRONT PANEL CONNECTOR
→ DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

DWG. NO. 394567 SHEET 1 OF 12

SHEET	1	2	3	4	5	6	7	8	9	10	11	12
REVISION	B	B	B	B	B	B	B	B	B	B	B	B

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .010 MAX
FINISH:

DRAWN [signature] 3/20/70
CHECK N. Butler 3/26/70
APPR R ALLEN 4-1-70
APPR

NEXT ASSY N/A

RAYTHEON — RAYTHEON COMPANY LEXINGTON, MASSACHUSETTS 02173

ADDER FLIP-FLOP CARD (LOGIC DIAGRAM)

CODE IDENT NO. 49956 SIZE D 394567

SCALE NONE SHEET 1 OF 12

RAYTHEON COMPUTER FORM 67-00P

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACLDDI		A59	8
ACRØØ		B68	4
ACRØØ-		B66	4
ACRØI		B54	4
ACRI5-		B6Ø	11
ADAØØ-		A67	4
ADAØ8-		B33	5
ADBØØ-		A69	4
ADBØ8-		B31	5
ADBZEROØ		B37	5
ADBZERO12		B39	5
ADBZERO4		B35	5
ADBZERO8		B41	5
ADENMBC3-		B3	5
ADFEQL	S	B28	5
ADFEQL-	S	A49	5
ADFNEG	S	B26	5
ADFNEG-	S	BIØ	5
ADFOVF	S	B22	4
ADFOVFRI-	S	B47	4
ADFOVFS-	S	B64	4
ADORØØ-	S	B25	5
ADORØ8-		BI2	5
ADSUMØØ-		B7	4
ADSUMØØA	S	B8	4
ADSUMØI-		A63	7
ADSUMØ2-		A35	7
ADSUMØ3-		A37	7
ADSUMØ4-		44Ø	7
ADSUMØ5-		A6	8
ADSUMØ8-		B5	5
ADSUMI5-		A26	6
CCFBYTE-	S	A51	6
CCFGLB	S	A7Ø	6
CCITCY	S	AII	9
CPSWDSMS-		CE	4
DAD12-	S	A27	IØ
DAD13-	S	A23	IØ
DAD14-	S	A21	IØ
DAD15-	S	A25	IØ
DISB-	S	A48	8
DISPØØ-	S	CF	7
DISPØI-	S	CB	7
DISPØ2-	S	CD	7
DISPØ3-	S	CC	7
DISPØ4-	S	CA	8
DISPØ5-	S	CU	5
DISPØ6-	S	CT	5
DISPØ7-	S	CK	4
DISPØ8-	S	CL	6
DISPI3-	S	CR	8
DOSB-	S	BI8	8
EXLDADI-		A57	8
EXLDADSRI-		A44	8
EXLDMB		A33	7
EXLDPC		A2Ø	7
EXRØØ	S	A52	7
EXRØI	S	A24	7
EXRØ2	S	A36	7
EXRØ3	S	A43	7
EXRØ4	S	A29	8
ICDCØ		A34	IØ
ICDCØ-		B44	4
IN4SC5		B2Ø	5
INDCØØI		AI5	9
INDCØØ2		AI9	9
INDCØØ3		A14	9
INDCØØ4		B36	6
INDCØØ5		BI5	6
INDCØØ6		B58	11
INDCØØA		A7	9
INDCØØB		A47	9

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
INDCØII		B62	4
INDCØ3-		BI4	8
INDCØ7-		B5Ø	5
INDCØ8A		B5I	4
INDCØ9		B48	4
INDC2-		BI7	6
INDCAORB		B49	4
INDCBYTE		A5	6
INDCF		B2I	5
INDCXX3-		A64	11
INDCXX7-		B63	11
INTRPTØØ-		AI6	10
ITI6AØI-		A32	9
ITACT-	S	A54	9
ITDSB	S	A53	9
ITENB	S	AI7	9
ITFINHR2-		A3Ø	9
ITIDL	S	AI3	9
ITSVENB	S	AI8	9
ITWAIT-		A55	9
IXØØMB-		B32	11
IXCLKENBI-		B23	11
IXCLKENBL	S	B59	11
IXCLKENBR	S	B57	11
IXLDAD3-		BI9	11
IXLDADL	S	B65	11
IXLDADR	S	B3Ø	11
IXLDPC	S	A66	11
IXRI5S	S	B4Ø	11
IXSL	S	B6I	11
IXSLOPT-		B34	11
IXSLZRO	S	A6Ø	11
IXSR	S	B9	11
IXSRACI5	S	BI3	11
IXSROPT-		BII	11
KK3A		B53	4
KKB2		A9	IØ
MBRØØ-		B4	6
MBRØØD	S	B6	6
MBRØ5-		B27	5
MBRØ6-		B29	5
MBRØ7-		B45	4
MBRO8-		B42	6
MBRIO-		B55	11
MBRII-		B43	4
MBRI2-		A22	7
MBRI3-		A39	7
MBRI4-		A41	7
MBRI5-		A3I	8
MRESET-		A65	4
PCRØI-		AI	7
PCRØ2-		A8	7
PCRØ3-		A38	7
PCRØ4-		A42	7
PCRØ5		AIO	8
PFSINT-		A28	9
PUARI	S	B67	6
SCDCI-		B56	4
SCDC4		B46	4
SCDC4-		A62	11
SCDC5		B38	4
SCDC7		A56	9
SCDC7-		A45	9
SCDC9-		B24	4
SCDCB-		AI2	9
SCDCC-		A68	8
SCDCD-		A46	6
STBINH		A50	8
TIRCØ		A58	9
TIRC3-		BI6	4
TIRC4-		B52	4

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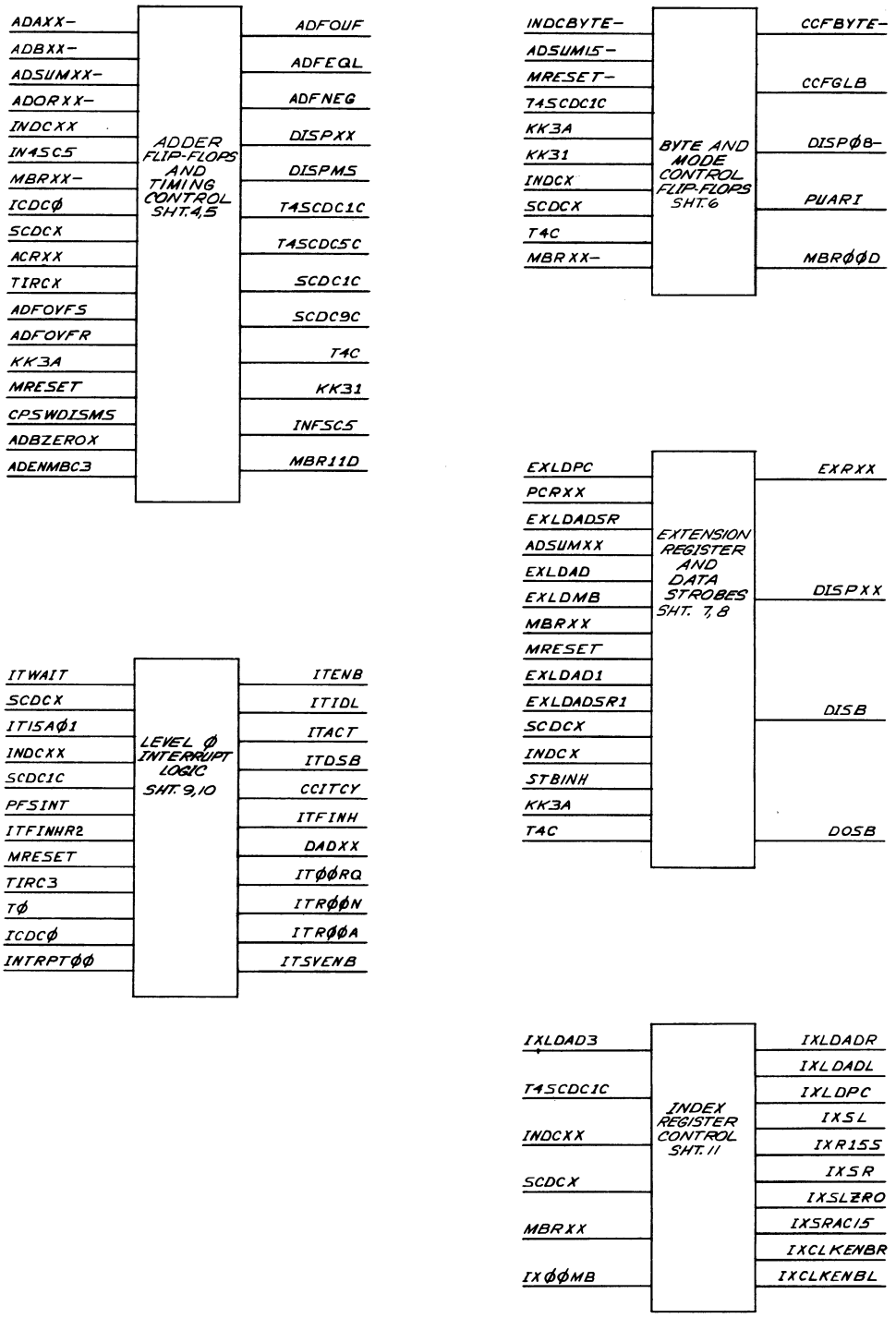
49956	D	394567	B
SCALE NONE		SHEET 2	



BLOCK DIAGRAM

CODE IDENT NO.	SIZE		REV
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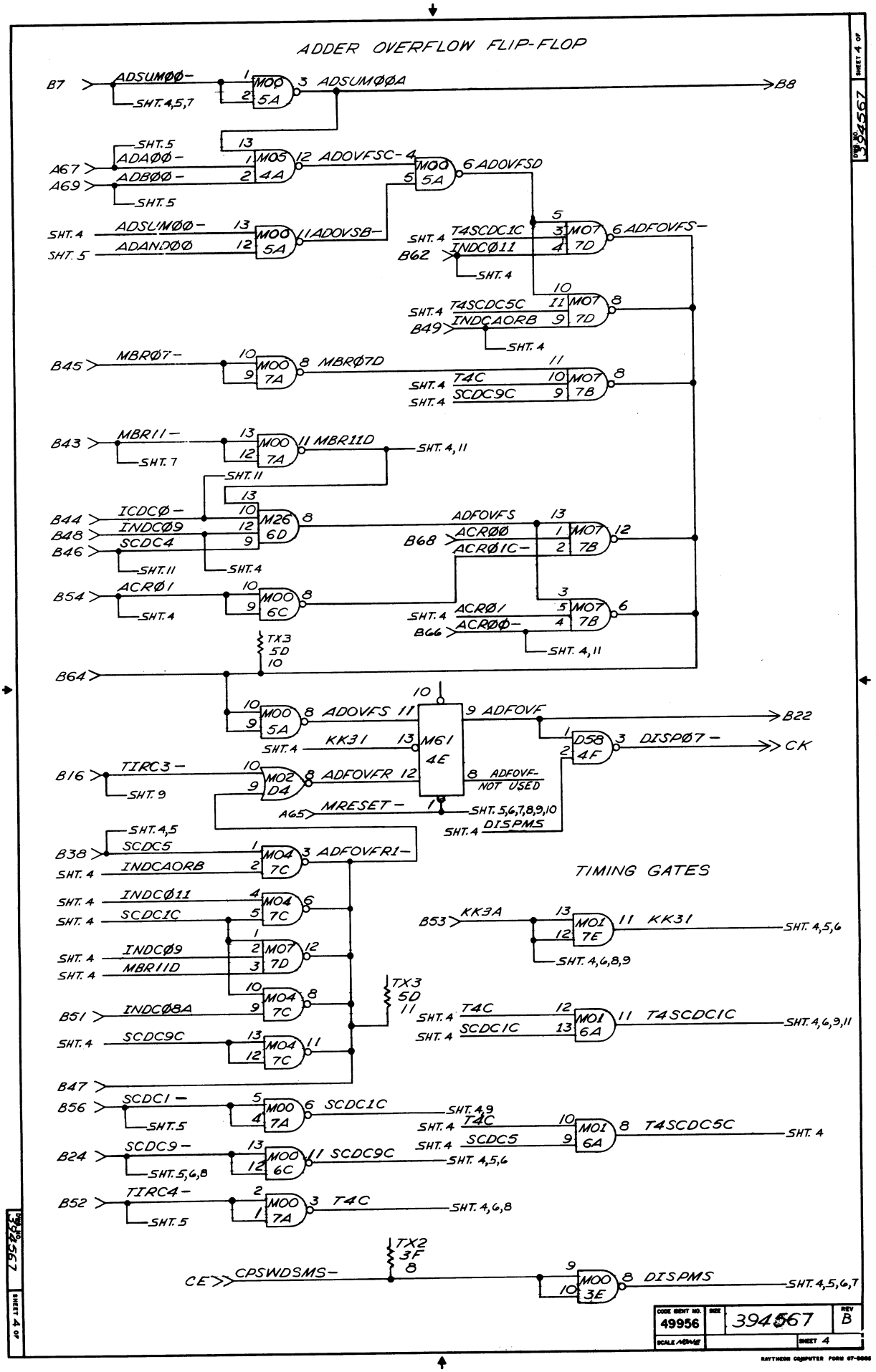
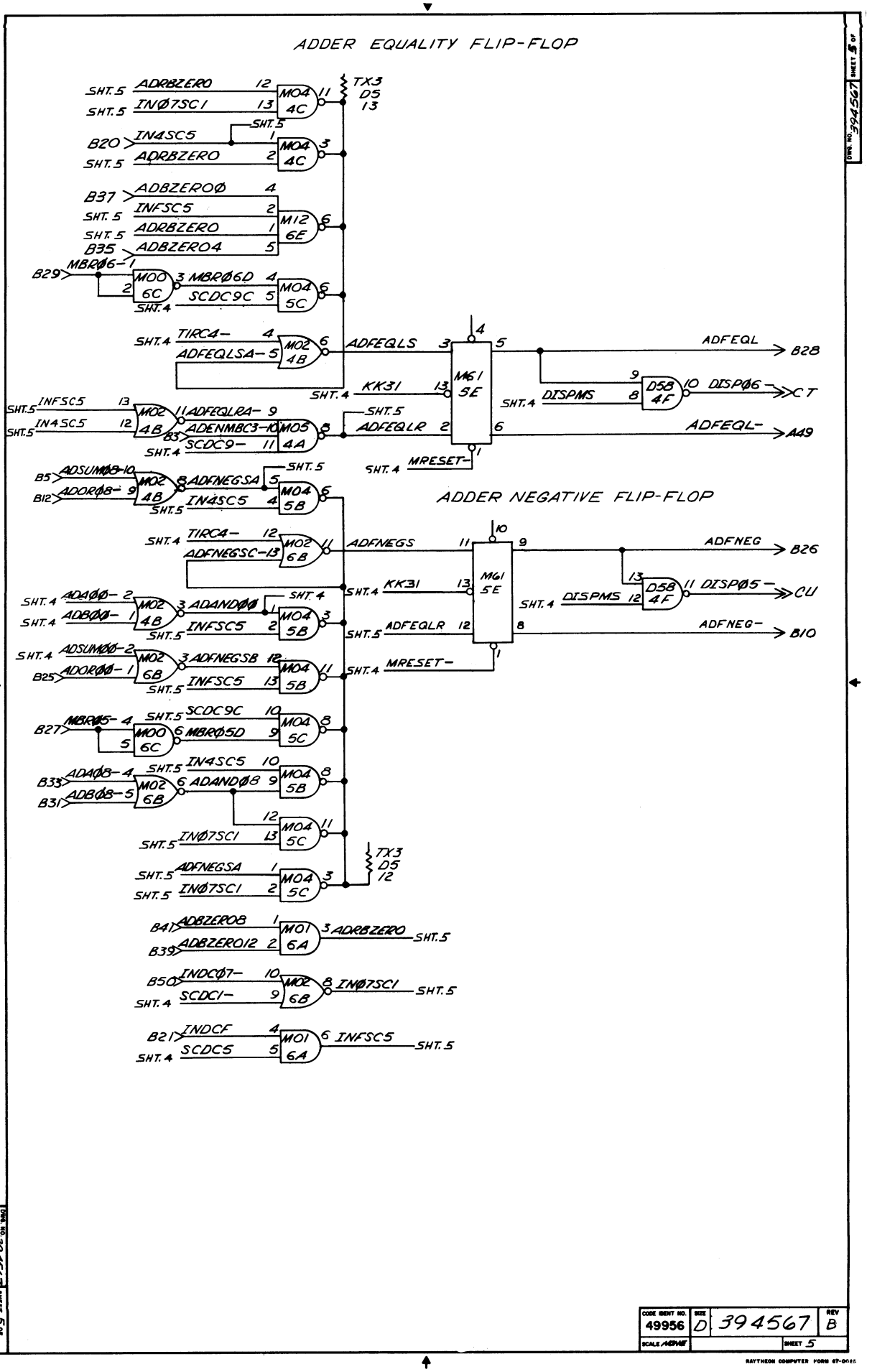
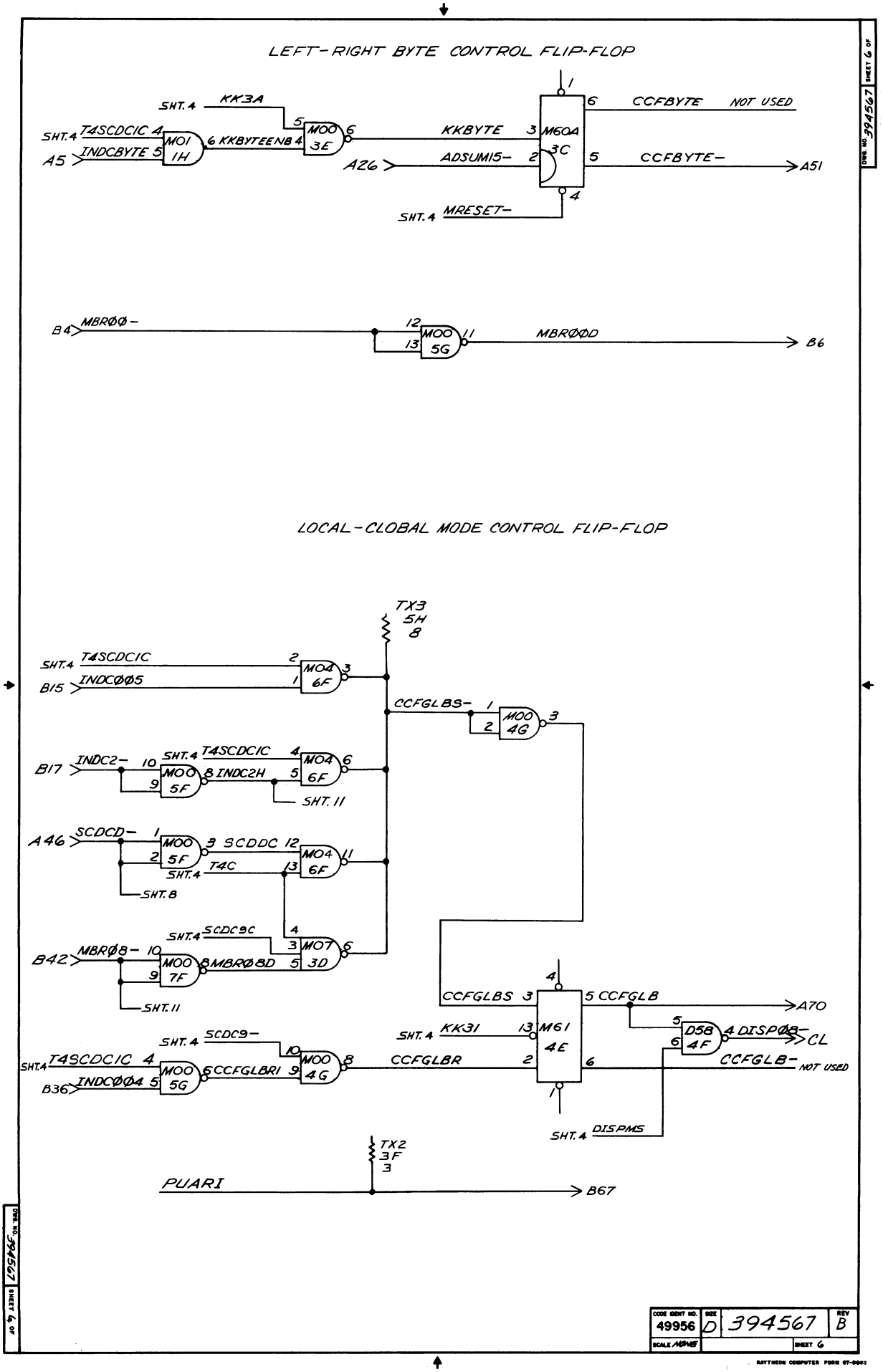
SCALE NONE			SHEET 3

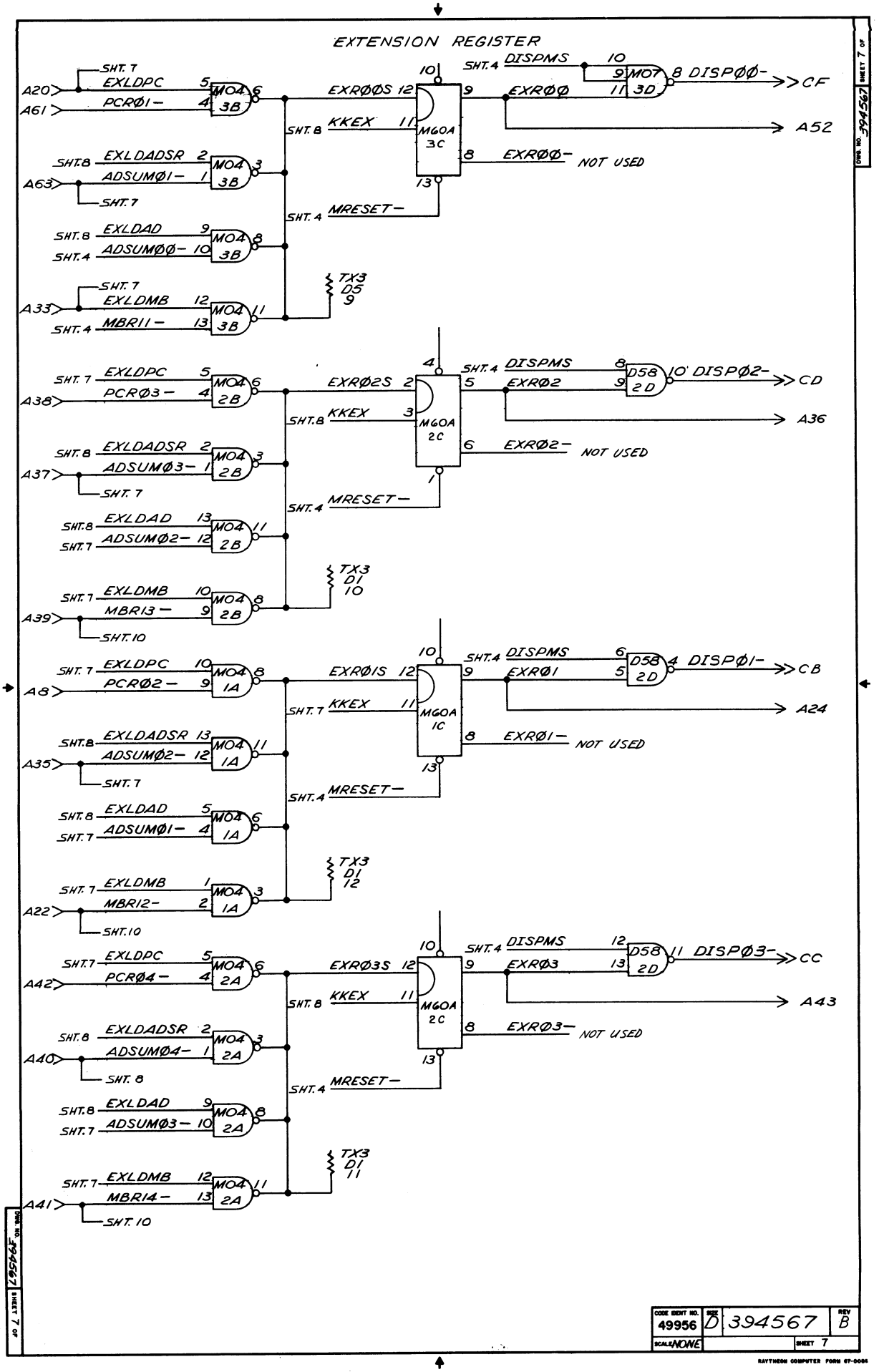
RAYTHEON COMPUTER FORM 67-0006

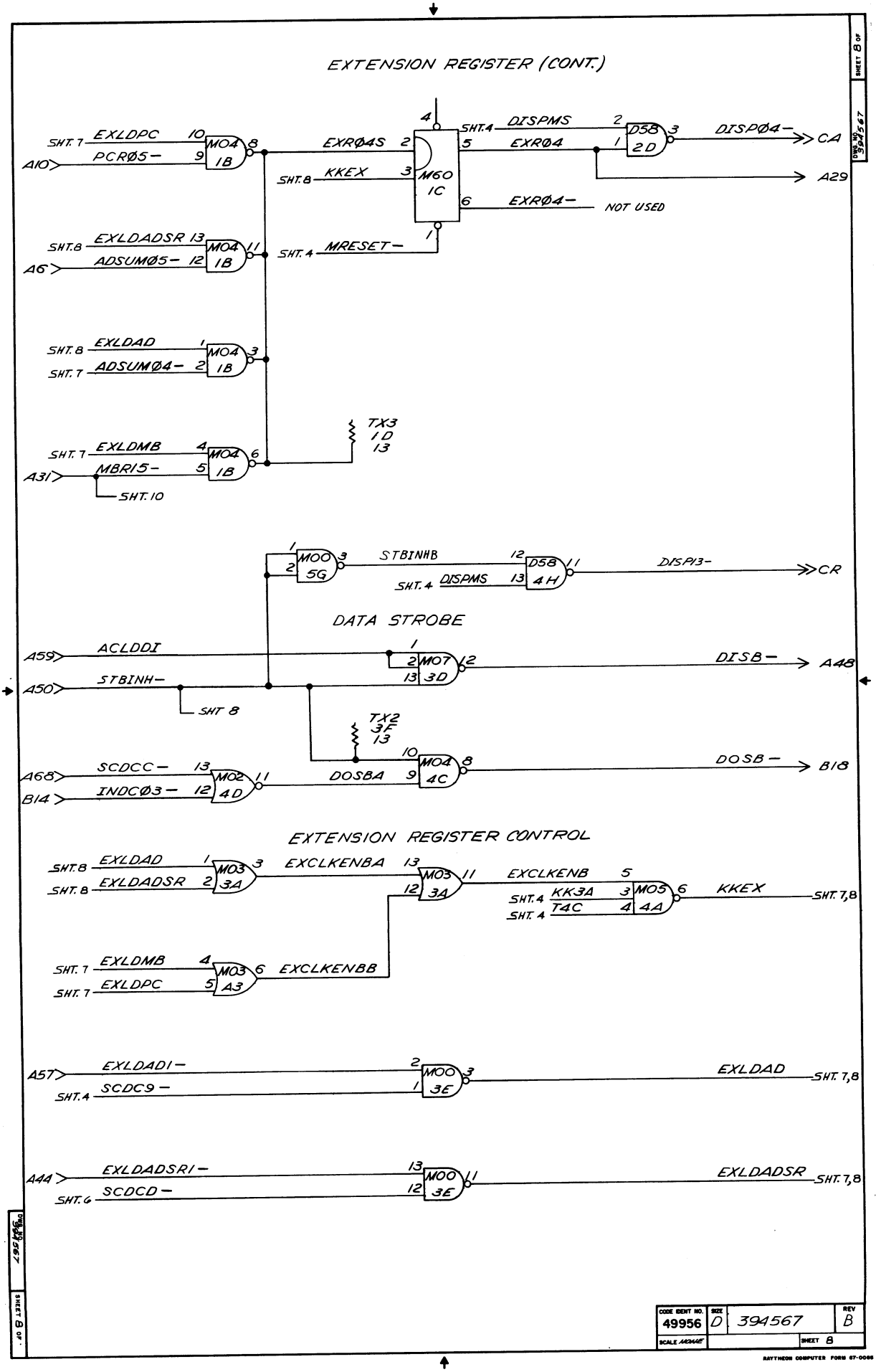
SHEET 3 OF
DWG. NO. 394567

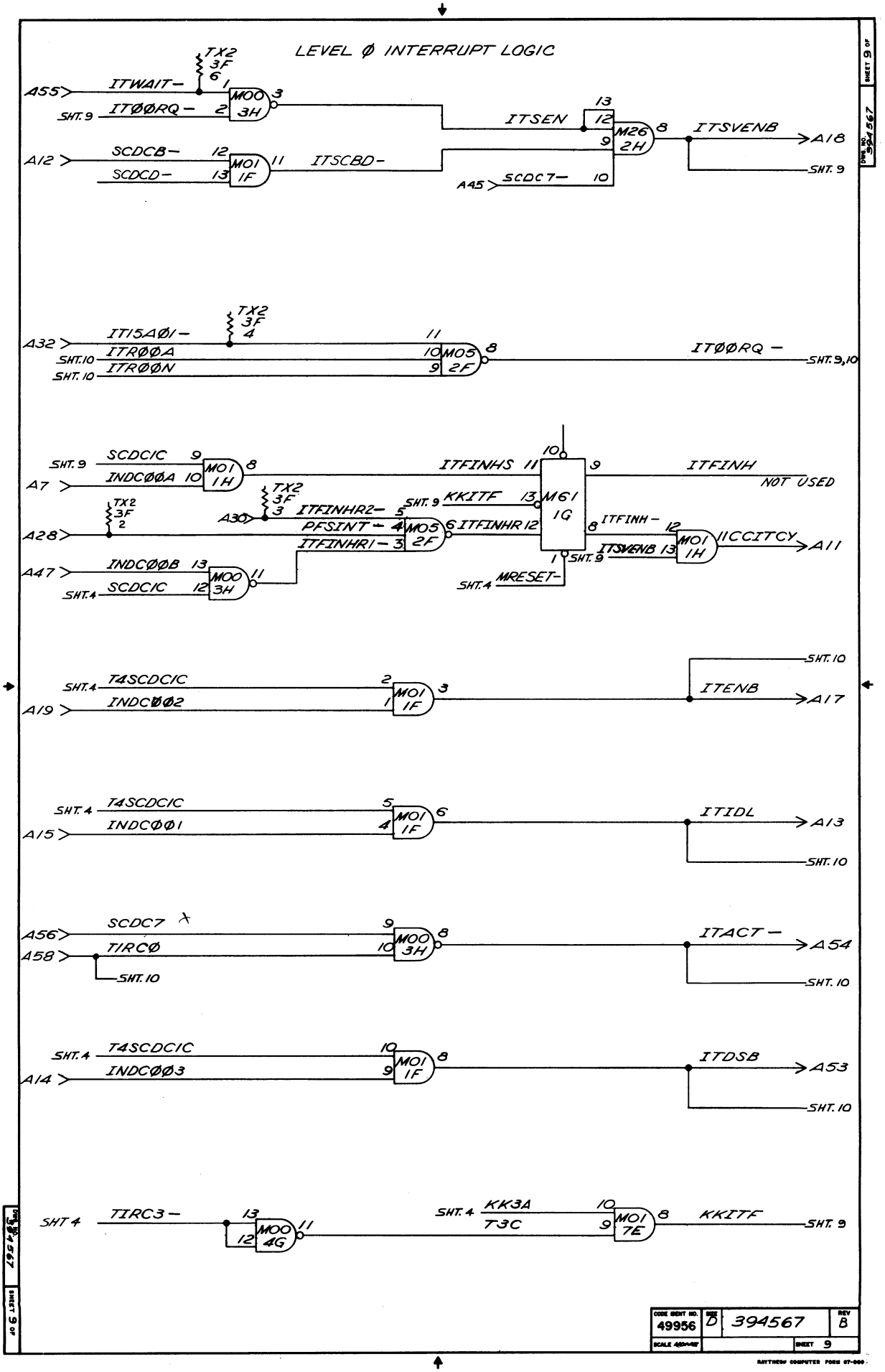

ADDER OVERFLOW FLIP-FLOP
B7
ADSUMØØ-
SHT. 4,5,7
M00 5A
ADSUMØØA
B8
SHT. 5
ADAØØ-
ADBØØ-
A67
A69
M05 4A
ADOVFSC-4
M00 5A
ADOVFSD
SHT. 5
SHT. 4
ADSUMØØ-
ADANDØØ
SHT. 5
M00 5A
ADOVSB-
SHT. 4
T4SCDC1C
INDCØ11
B62
M07 7D
ADFOVFS-
SHT. 4
T4SCDC5C
INDCAORB
B49
M07 7D
SHT. 4
B45
MBRØ7-
M00 7A
MBRØ7D
SHT. 4
T4C
SCDC9C
SHT. 4
M07 7B
B43
MBR11-
SHT. 7
M00 7A
MBR11D
SHT. 4, 11
SHT. 11
B44
B48
B46
ICDCØ-
INDCØ9
SCDC4
SHT. 11
M26 6D
SHT. 4
ADFOVFS
B68
ACRØØ
ACRØ1C-
M07 7B
B54
ACRØ1
SHT. 4
M00 6C
SHT. 4
ACRØ1
ACRØØ-
B66
M07 7B
SHT. 4, 11
TX3 5D
B64
M00 5A
ADOVFS
M61 4E
ADFOVF
B22
KK31
SHT. 4
D58 4F
DISPØ7-
CK
B16
TIRC3-
SHT. 9
M02 D4
ADFOVFR
ADFOVF-NOT USED
A65
MRESET-
SHT. 5,6,7,8,9,10
SHT. 4
DISPMS
SHT. 4,5
B38
SCDC5
SHT. 4
INDCAORB
M04 7C
ADFOVFR1-
TIMING GATES
SHT. 4
INDCØ11
SCDC1C
M04 7C
B53
KK3A
M01 7E
KK31
SHT. 4,5,6
SHT. 4,6,8,9
SHT. 4
INDCØ9
MBR11D
M07 7D
TX3 5D
SHT. 4
T4C
SCDC1C
M01 6A
T4SCDC1C
SHT. 4,6,9,11
B51
INDCØ8A
M04 7C
SHT. 4
SCDC9C
M04 7C
B47
B56
SCDC1-
SHT. 5
M00 7A
SCDC1C
SHT. 4,9
SHT. 4
T4C
SCDC5
M01 6A
T4SCDC5C
SHT. 4
B24
SCDC9-
SHT. 5,6,8
M00 6C
SCDC9C
SHT. 4,5,6
B52
TIRC4-
SHT. 5
M00 7A
T4C
SHT. 4,6,8
TX2 3F
CE
CPSWDSMS-
M00 3E
DISPMS
SHT. 4,5,6,7
394567
SHEET 4 OF
CODE IDENT NO. 49956
SIZE
394567
REV B
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0000

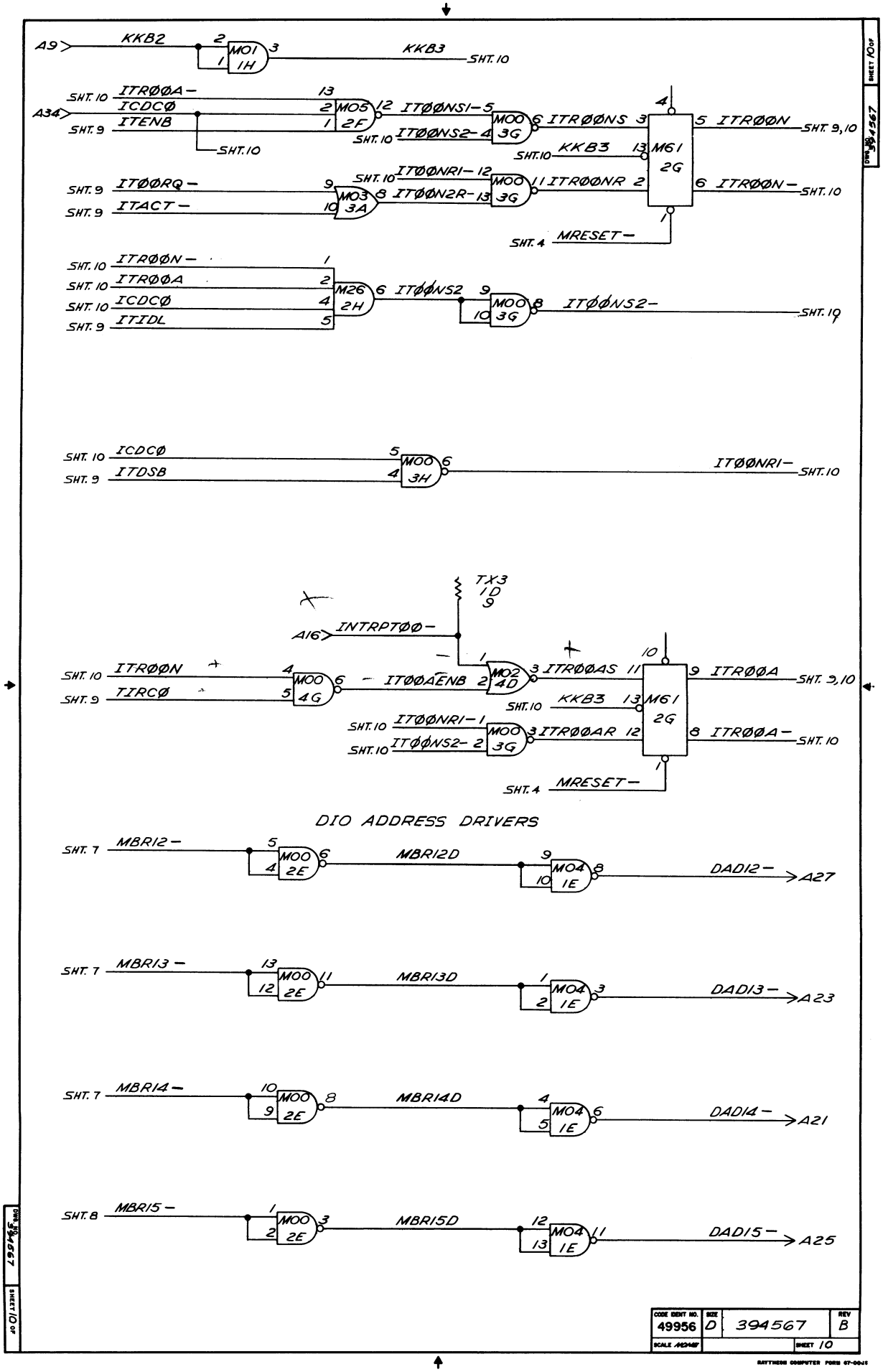

ADDER EQUALITY FLIP-FLOP
ADDER NEGATIVE FLIP-FLOP
ADRBZERO
INØ7SC1
IN4SC5
ADBZEROØ
INFSC5
ADBZERO4
MBRØ6-
MBRØ6D
SCDC9C
TIRC4-
ADFEQLSA-
ADFEQLS
ADFEQL
KK31
DISPMS
DISPØ6-
ADFEQLRA-
ADENMBC3-10
SCDC9-
ADFEQLR
MRESET-
ADSUMØ8-10
ADDRØ8-9
ADFNEGSA
TIRC4-
ADFNEGSC-13
ADFNEGS
ADFNEG
DISPØ5-
ADAØØ-2
ADBØØ-1
ADANDØØ
ADSUMØØ-2
ADDRØØ-1
ADFNEGSB
MBRØ5-4
MBRØ5D
ADAØ8-4
ADBØ8-5
ADANDØ8
ADFNEGSA
INDCØ7-
SCDC1-
INØ7SC1
INDCF
SCDC5
ADBZERO8
ADBZERO12
ADRBZERO
TX3
D5
DWG. NO. 394567
SHEET 5 OF
CODE IDENT NO. 49956
SIZE D
394567
REV B
SHEET 5
RAYTHEON COMPUTER FORM 67-0468

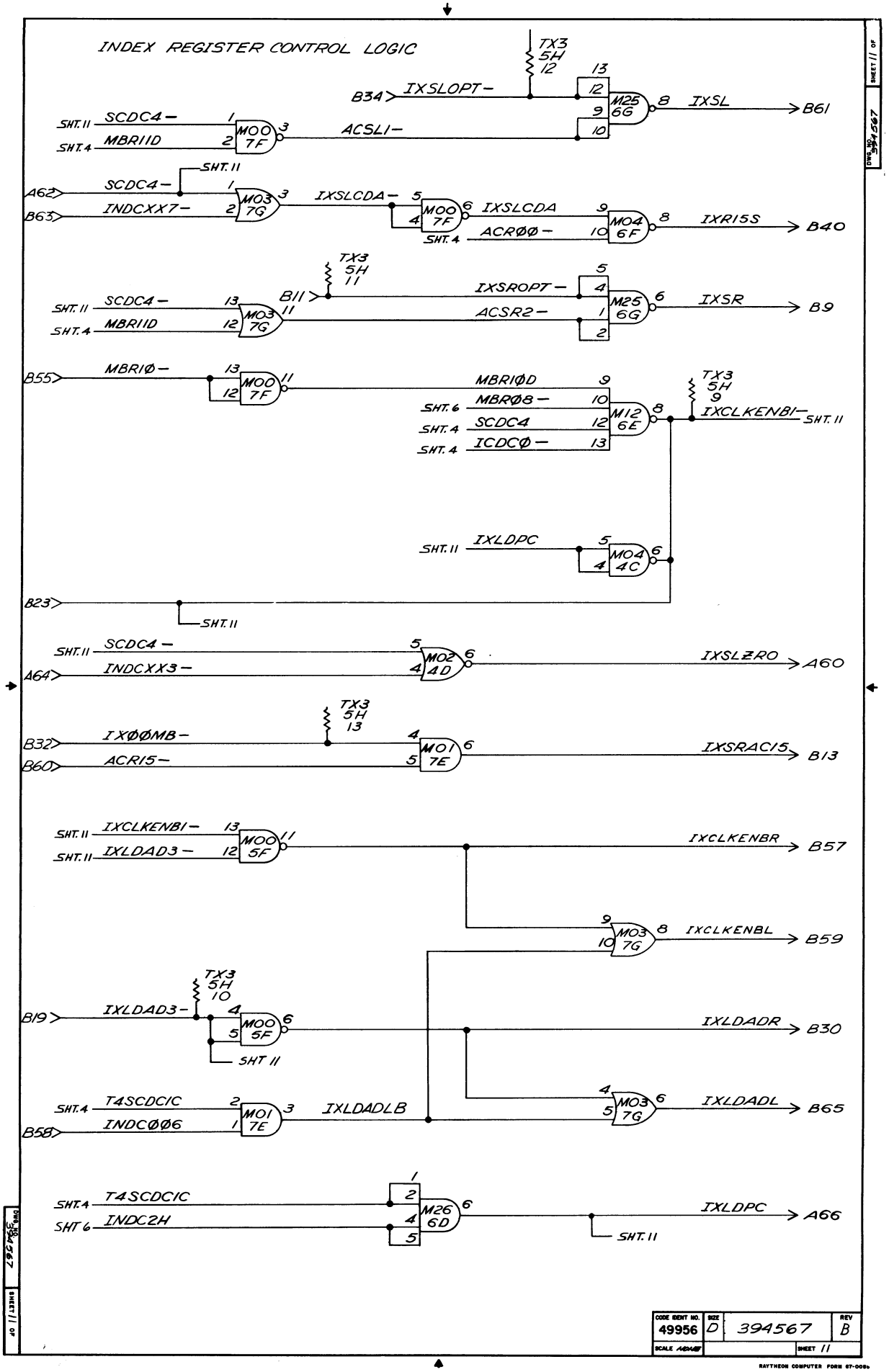

LEFT-RIGHT BYTE CONTROL FLIP-FLOP
SHT. 4 KK3A
SHT. 4 T4SCDCIC 4
INDCBYTE 5
A5
M01 1H
6 KKBYTEENB 4
M00 3E
6
KKBYTE 3
M60A 3C
1
6 CCFBYTE NOT USED
A26
ADSUM15- 2
5 CCFBYTE- A51
4
SHT. 4 MRESET-
B4 MBR00-
12
M00 5G
13
11 MBR00D B6
LOCAL-CLOBAL MODE CONTROL FLIP-FLOP
TX3 5H 8
SHT. 4 T4SCDCIC
B15 INDC005
M04 6F
CCFGLBS- 1
M00 4G
2
3
B17 INDC2- 10
M00 5F
9
SHT. 4 T4SCDCIC 4
8 INDC2H
M04 6F
5
6
SHT. 11
A46 SCDCD- 1
M00 5F
2
3 SCDDC 12
M04 6F
11
SHT. 4 T4C 13
SHT. 8
SHT. 4 SCDC9C
4
B42 MBR08- 10
M00 7F
9
8 MBR08D
M07 3D
3
6
SHT. 11
4
CCFGLBS 3
5 CCFGLB A70
SHT. 4 KK31 13
M61 4E
2
6
CCFGLBR
5
D58 4F
6
4 DISP08- CL
CCFGLB- NOT USED
1
SHT. 4 DISPMS
SHT. 4 SCDC9-
10
SHT. 4 T4SCDCIC 4
INDC0004 5
B36
M00 5G
6 CCFGLBRI 9
M00 4G
8
TX2 3F 3
PUARI
B67
CODE IDENT NO. 49956
SIZE D
394567
REV B
SHEET 6
SHEET 6 OF
DWG. NO. 394567
RAYTHEON COMPUTER FORM 67-0003


EXTENSION REGISTER
A20
A61
EXLDPC
PCRØ1-
MO4 3B
EXRØØS
KKEX
MG0A 3C
DISPMS
MO7 3D
EXRØØ
DISPØØ-
CF
A52
EXRØØ-
NOT USED
MRESET-
EXLDADSR
ADSUMØ1-
A63
EXLDAD
ADSUMØØ-
TX3 D5 9
A33
EXLDMB
MBR11-
A38
PCRØ3-
EXRØ2S
EXRØ2
DISPØ2-
CD
A36
EXRØ2-
A37
ADSUMØ3-
A39
MBR13-
A8
PCRØ2-
EXRØ1S
EXRØ1
DISPØ1-
CB
A24
EXRØ1-
A35
ADSUMØ2-
A22
MBR12-
TX3 D1 12
A42
PCRØ4-
EXRØ3S
EXRØ3
DISPØ3-
CC
A43
EXRØ3-
A40
ADSUMØ4-
A41
MBR14-
TX3 D1 11
SHT. 7
SHT. 8
SHT. 4
SHT. 10
SHEET 7 OF
DWG. NO. 394567
CODE IDENT NO. 49956
SIZE D
394567
REV B
SCALE NONE
SHEET 7
RAYTHEON COMPUTER FORM 67-0085

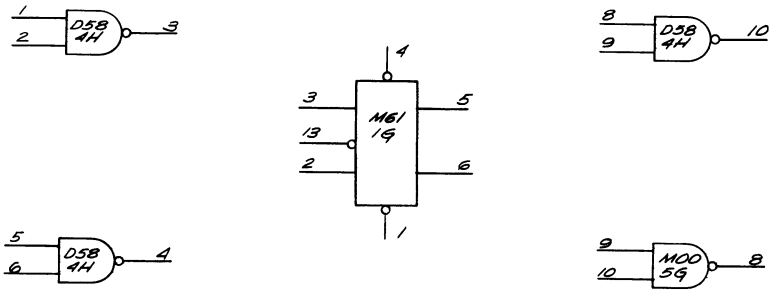

EXTENSION REGISTER (CONT.)
SHEET 8 OF
DWG NO 394567
SHT. 7 EXLDPC 10 MO4 8
PCRØ5- 9 1B
A10
EXRØ4S 2
SHT. 8 KKEX 3 M60 1C
4
SHT. 4 DISPMS 2
5 EXRØ4
D58 3
1 2D
DISPØ4- CA
A29
6 EXRØ4- NOT USED
1
SHT. 8 EXLDADSR 13 MO4 11
ADSUMØ5- 12 1B
A6
SHT. 4 MRESET-
SHT. 8 EXLDAD 1 MO4 3
SHT. 7 ADSUMØ4- 2 1B
TX3 1D 13
SHT. 7 EXLDMB 4 MO4 6
MBR15- 5 1B
A31
SHT. 10
1 MOO 3
2 5G
STBINHB 12 D58 11
SHT. 4 DISPMS 13 4H
DISP13- CR
DATA STROBE
A59 ACLDDI
1
2 MO7 12
13 3D
DISB- A48
A50 STBINH-
SHT. 8
TX2 3E 13
10 MO4 8
A68 SCDCC- 13 MO2 11
B14 INDCØ3- 12 4D
DOSBA 9 4C
DOSB- B18
EXTENSION REGISTER CONTROL
SHT. 8 EXLDAD 1 MO3 3
SHT. 8 EXLDADSR 2 3A
EXCLKENBA 13
12 MO3 3A 11
EXCLKENB 5
SHT. 4 KK3A 3 MO5 6
SHT. 4 T4C 4 4A
KKEX SHT. 7,8
SHT. 7 EXLDMB 4 MO3 6
SHT. 7 EXLDPC 5 A3
EXCLKENBB
A57 EXLDADI-
2 MOO 3
SHT. 4 SCDC9- 1 3E
EXLDAD SHT. 7,8
A44 EXLDADSRI-
13 MOO 11
SHT. 6 SCDCD- 12 3E
EXLDADSR SHT. 7,8
DWG NO 394567
SHEET 8 OF
CODE IDENT NO. 49956
SIZE D
394567
REV B
SCALE NONE
SHEET 8
RAYTHEON COMPUTER FORM 67-0088

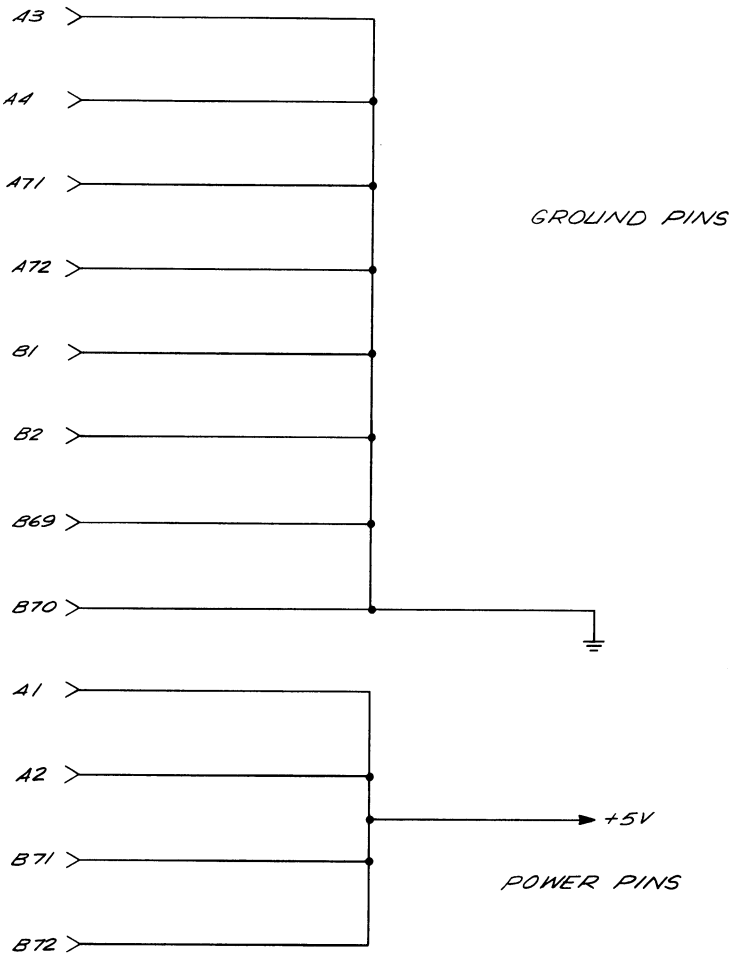

LEVEL Ø INTERRUPT LOGIC
A55
ITWAIT-
TX2 3F 6
M00 3H 3
SHT. 9
ITØØRQ-
ITSEN
M26 2H 8
ITSVENB
A18
SHT. 9
A12
SCDCB-
SCDCD-
M01 1F 11
ITSCBD-
A45
SCDC7-
A32
IT15AØ1-
TX2 3F 4
SHT. 10
ITRØØA
ITRØØN
M05 2F 8
ITØØRQ-
SHT. 9,10
SCDCIC
INDCØØA
M01 1H 8
ITFINHS
ITFINH
NOT USED
A7
TX2 3F 2
A28
TX2 3F 3
A30
ITFINHR2-
PFSINT-
ITFINHR1-
M05 2F 6
ITFINHR
M61 1G
KKITF
SHT. 9
ITFINH-
ITSVENB
M01 1H
IICCITCY
A11
A47
INDCØØB
SCDCIC
M00 3H 11
SHT. 4
MRESET-
SHT. 10
SHT. 4
T4SCDCIC
INDCØØ2
M01 1F 3
ITENB
A17
A19
SHT. 4
T4SCDCIC
INDCØØ1
M01 1F 6
ITIDL
A13
SHT. 10
A15
A56
SCDC7
A58
TIRCØ
M00 3H 8
ITACT-
A54
SHT. 10
SHT. 10
SHT. 4
T4SCDCIC
INDCØØ3
M01 1F 8
ITDSB
A53
SHT. 10
A14
SHT 4
TIRC3-
M00 4G 11
SHT. 4
KK3A
T3C
M01 7E 8
KKITF
SHT. 9
SHEET 9 OF
DWG. NO. 394567
CODE IDENT NO. 49956
SIZE D
394567
REV B
SHEET 9
RAYTHEON COMPUTER FORM 67-000


A9
KKB2
M01
1H
KKB3
SHT. 10
A34
ITRØØA–
ICDCØ
ITENB
M05
2F
ITØØNS1–5
ITØØNS2–4
M00
3G
ITRØØNS 3
ITRØØNR 2
M61
2G
5 ITRØØN
6 ITRØØN–
KKB3 13
MRESET–
SHT. 4
SHT. 9,10
ITØØRQ–
ITACT–
M03
3A
ITØØNRI–12
ITØØN2R–13
ITRØØN–
M26
2H
ITØØNS2
ITØØNS2–
ITIDL
ITDSB
3H
ITØØNRI–
TX3
1D
9
A16
INTRPTØØ–
M02
4D
ITØØAENB
ITRØØAS 11
ITRØØA
ITRØØAR 12
ITØØNRI–1
ITØØNS2–2
ITRØØA–
TIRCØ
4G
DIO ADDRESS DRIVERS
MBRI2–
MBRI2D
M04
1E
DADI2–
A27
MBRI3–
MBRI3D
DADI3–
A23
MBRI4–
MBRI4D
DADI4–
A21
MBRI5–
MBRI5D
DADI5–
A25
DWG NO 394567
SHEET 10 OF
CODE IDENT NO. 49956
SIZE D
394567
REV B
SCALE 4/24/87
SHEET 10
RAYTHEON COMPUTER FORM 67-0045


INDEX REGISTER CONTROL LOGIC
TX3 5H 12
B34 IXSLOPT-
M25 6G
IXSL
B61
SHT. 11 SCDC4-
SHT. 4 MBRIID
M00 7F
ACSLI-
A62 SCDC4-
B63 INDCXX7-
M03 7G
IXSLCDA-
M00 7F
IXSLCDA
M04 6F
ACRØØ-
IXR15S
B40
TX3 5H 11
B11
IXSROPT-
M25 6G
IXSR
B9
ACSR2-
B55 MBRIØ-
M00 7F
MBRIØD
MBRØ8-
SHT. 6
SHT. 4 SCDC4
SHT. 4 ICDCØ-
M12 6E
TX3 5H 9
IXCLKENBI-
SHT. 11
SHT. 11 IXLDPC
M04 4C
B23
SHT. 11
SHT. 11 SCDC4-
A64 INDCXX3-
M02 4D
IXSLZRO
A60
TX3 5H 13
B32 IXØØMB-
B60 ACR15-
M01 7E
IXSRAC15
B13
SHT. 11 IXCLKENBI-
SHT. 11 IXLDAD3-
M00 5F
IXCLKENBR
B57
M03 7G
IXCLKENBL
B59
TX3 5H 10
B19 IXLDAD3-
M00 5F
IXLDADR
B30
SHT 11
SHT. 4 T4SCDCIC
B58 INDCØØ6
M01 7E
IXLDADLB
M03 7G
IXLDADL
B65
SHT. 4 T4SCDCIC
SHT 6 INDC2H
M26 6D
IXLDPC
A66
SHT. 11
SHEET 11 OF
DWG. NO. 394567
CODE IDENT NO. 49956
SIZE D
394567
REV B
SHEET 11
RAYTHEON COMPUTER FORM 67-0086

UNUSED IC. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	394567	B
SCALE NONE		SHEET 12	

RAYTHEON COMPUTER FORM 67-0085

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
A	Released Per E.O. 19218						

DWG. NO. 394572 SHEET 1 OF 10

TABLE OF CONTENTS

GLOSSARY

ACCLKENB4	ACCUMULATOR CLOCK CONTROL LOGIC INPUT
ACLDAD3	ACCUMULATOR LOAD FROM THE ADDER LOGIC INPUT
ACRXX	ACCUMULATOR REGISTER BIT XX
ACRXXS	ACCUMULATOR REGISTER BIT XX SET
ACSLOPT	ACCUMULATOR SHIFT LEFT LOGIC INPUT
ACSROPT	ACCUMULATOR SHIFT RIGHT CIRCULAR DOUBLE LOGIC INPUT
ACSROPT1	ACCUMULATOR SHIFT RIGHT LOGIC INPUT
ADAXX	ADDER BUS A BIT XX
ADBXX	ADDER BUS B BIT XX
ADC02	ADDER CARRY 02
ADENACCOP	ADDER ENABLE FROM ACCUMULATOR COMPLIMENT LOGIC INPUT
ADENIX2	ADDER ENABLE FROM INDEX REGISTER LOGIC INPUT
ADENMBA	ADDER ENABLE FROM MEMORY BUFFER LOGIC INPUT
ADENMBC2	ADDER ENABLE FROM MEMORY BUFFER COMPLIMENT LOGIC INPUT
ADFOVFS	ADDER FLIP-FLOP OVERFLOW SET INPUT
ADINCRYC	ADDER INCREMENT CONTROL LOGIC INPUT
ADSUMXX	ADDER OUTPUT BIT XX
CCCMEND1	COMMAND END LOGIC INPUT
CCCMEND6	COMMAND END DISABLE
ICDECOPT	ITERATION COUNTER DECREMENT LOGIC INPUT
ICRX	ITERATION COUNTER BIT X
INDCXX	INSTRUCTION DECODE X
IX00MB	INDEX REGISTER BIT 00 SET LOGIC INPUT
IXCLKENB1	INDEX REGISTER CLOCK CONTROL LOGIC INPUT
IXLDAD3	INDEX REGISTER LOAD FROM ADDER LOGIC INPUT
IXR00	INDEX REGISTER BIT 00
IXR00MD	INDEX REGISTER BIT 00 REPOWERED
IXRDR	INDEX REGISTER DIRECT RESET
IXRXXS	INDEX REGISTER BIT XX SET INPUT
IXSLOPT	INDEX REGISTER SHIFT LEFT LOGIC OPTIONAL INPUT
IXSROPT	INDEX REGISTER SHIFT RIGHT LOGIC INPUT
KK2B	GATED SYSTEM CLOCK FOR MULTIPLY/DIVIDE
MBLDADRB0	MEMORY BUFFER LOAD RIGHT BYTE FROM ADDER LOGIC INPUT
MBLDARLB0	MEMORY BUFFER LOAD LEFT BYTE FROM ADDER LOGIC INPUT
MBR00D	MEMORY BUFFER REGISTER BIT 00 REPOWERED
MBR08	MEMORY BUFFER REGISTER BIT 08
MDDCX	DIVIDE SEQUENCER STATE X
MDF10MUL	MULTIPLY SEQUENCE STATE
MDRST	MULTIPLY/DIVIDE RESET
OPTRDWR	MEMORY READ-WRITE CONTROL LOGIC INPUT
SCDC1	SEQUENCER STATE ONE
SCR3OPT	DISP15 LOGIC INPUT
SCRFOPT	DISP11 LAMP DRIVER
TIRC1	TIMING INTERVAL REGISTER BIT ONE
TIRCX	TIMING INTERVAL REGISTER BIT X
TXMD	TIMING INTERVAL REGISTER BIT X REPOWERED

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
M00	531593-006
M01	531593-005
M02	531593-007
M03	531593-008
M04	531593-014
M05	531593-004
M06	531593-017
M07	531593-015
M10	531593-002
M25	531593-009
M26	531593-012
M60	531593-018
M61	531593-011

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. →» DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10
REVISION	A	A	A	A	A	A	A	A	A	A

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON:
DECIMALS: .XX ±.05, .XXX ±.010
ANGLES ±0° 30'
2. BREAK SHARP CORNERS .030 MAX
FINISH:

DRAWN M. Floyd 5-8-72
CHECK M. Bradley 5-10-72
APPR
APPR
NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

MULTIPLY/DIVIDE
(LOGIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE C | 394572
SCALE None | SHEET 1 of 10

RAYTHEON COMPUTER FORM 67-0086

DWG. NO. 394572 SHEET 1 OF 10

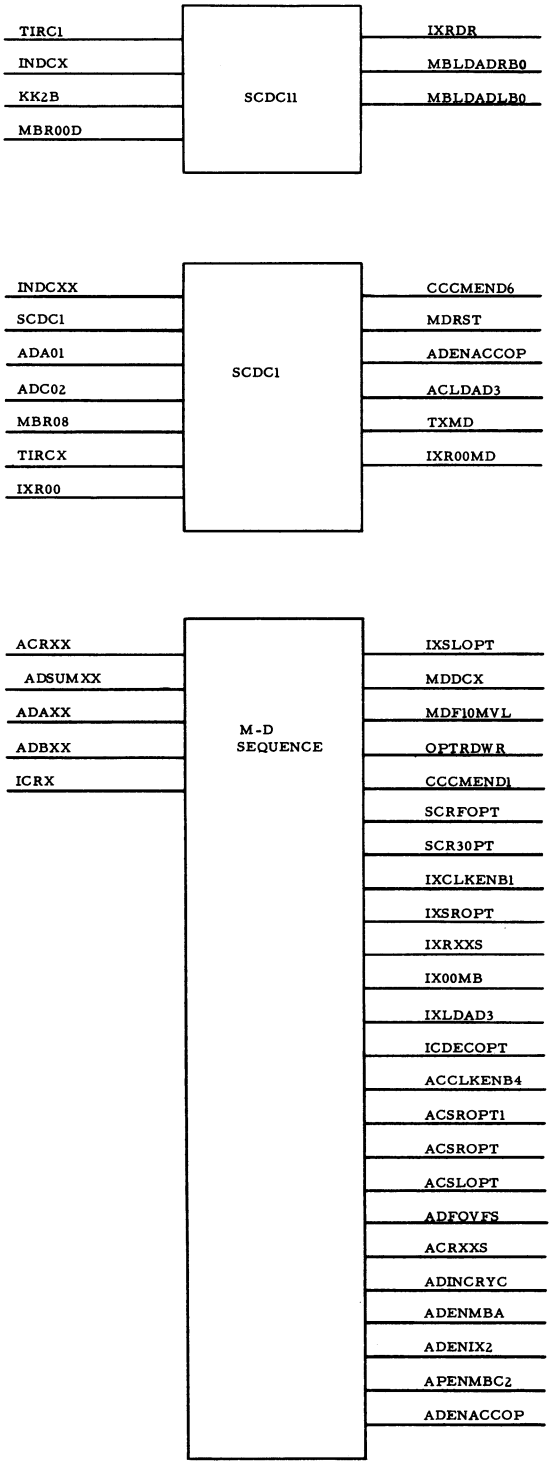
SIGNAL	SOURCE	CONN	SHEET
ACCLKENB4-	S	A6	09
ACLDAD3-	S	A45	04
ACR00S	S	B66	09
ACR01		B54	06
ACR15		A61	05
ACR15-		A51	05
ACR15S	S	B68	09
ACSLOPT-	S	A46	09
ACSROPT-	S	A48	09
ACSROPT1-	S	A21	09
ADA00-		A42	05
ADA01-		B57	04
ADA01-	S	A35	08
ADA02-	S	A26	08
ADA03-	S	A23	08
ADA04-	S	A19	08
ADA05-	S	A22	08
ADA06-	S	A10	08
ADA07-	S	A7	08
ADA08-	S	A38	08
ADA09-	S	A33	08
ADA10-	S	A27	08
ADA11-	S	A32	08
ADA12-	S	A18	08
ADA13-	S	A13	08
ADA14-	S	A12	08
ADA15-	S	A16	08
ADB00-		A44	05
ADC02-		B56	04
ADENACCOP-	S	B53	04
ADENIX2-	S	B36	04
ADENMBA-	S	A69	08
ADENMBC2-	S	A56	08
ADENPC2-	S	B50	04
ADFOVFR1-	S	B51	04
ADFOVFS-	S	A41	09
ADINCRYC	S	B3	08
ADSUM00-		A52	05
ADSUM00A		B18	05
ADSUM01-		A63	07
ADSUM02-		A57	07
ADSUM03-		B14	07
ADSUM04-		B7	07
ADSUM05-		B13	07
ADSUM06-		B8	07
ADSUM07-		B9	07
ADSUM08-		B24	08
ADSUM09-		B35	08
ADSUM10-		B27	08
ADSUM11-		B29	08
ADSUM12-		B41	08
ADSUM13-		B44	08
ADSUM14-		B40	08
ADSUM15-		A67	05
CCCMEND1-	S	A68	07
CCCMEND6-	S	B61	04
DISPIN		B20	05
ICDECOPT-	S	A8	07
ICR0-		B25	09
ICR1-		B23	09

SIGNAL	SOURCE	CONN	SHEET
ICR2-		B21	09
INDC0B-		B33	04
INDC0C-		B22	04
IX00MB-	S	B37	07
IXLDAD3-	S	A24	09
IXR00-		A37	04
IXR00S	S	A59	07
IXR01-		A40	08
IXR01S	S	A55	07
IXR02-		A28	08
IXR02S	S	A62	07
IXR03-		A25	08
IXR03S	S	B5	07
IXR04-		A17	08
IXR04S	S	B12	07
IXR05-		A20	08
IXR05S	S	B6	07
IXR06-		A5	08
IXR06S	S	B11	07
IXR07-		A9	08
IXR07S	S	B22	08
IXR08-		A36	08
IXR08S	S	B28	08
IXR09-		A31	08
IXR09S	S	B26	08
IXR10-		A30	08
IXR10S	S	B31	08
IXR11-		A29	08
IXR11S	S	B39	08
IXR12-		A15	08
IXR12S	S	B45	08
IXR13-		A11	08
IXR13S	S	B43	08
IXR14-		A14	08
IXR14S	S	B42	08
IXR15-		A34	08
IXR15S	S	B64	08
IXRDR-	S	B65	04
IXSLOPT-	S	A43	06
IXSROPT-	S	A53	07
KK2B		A70	04
MALDAD-	S	A60	04
MBLDADLB0-	S	B15	04
MBLDADRB0-	S	B17	04
MBR00-		B48	05
MBR00D		B19	04
MBR08-		B58	04
MRESET-		B49	04
OPTRDWR-	S	A66	07
PCLDAD2-		B63	07
SCDC1-		B52	04
SCDC11OP-	S	B60	04
SCDC1A		A64	04
SCR3OPT-	S	A49	05
SCRFOPT-	S	A47	05
T1RC2-		A50	05
TIRC1		B62	04
TIRC3-		B55	04
TIRC4-		B59	04
TIRCA		B30	04

DWG. NO. 394572 SHEET 2

CODE IDENT NO.	SIZE		REV
49956	C	394572	A
SCALE None			SHEET 2

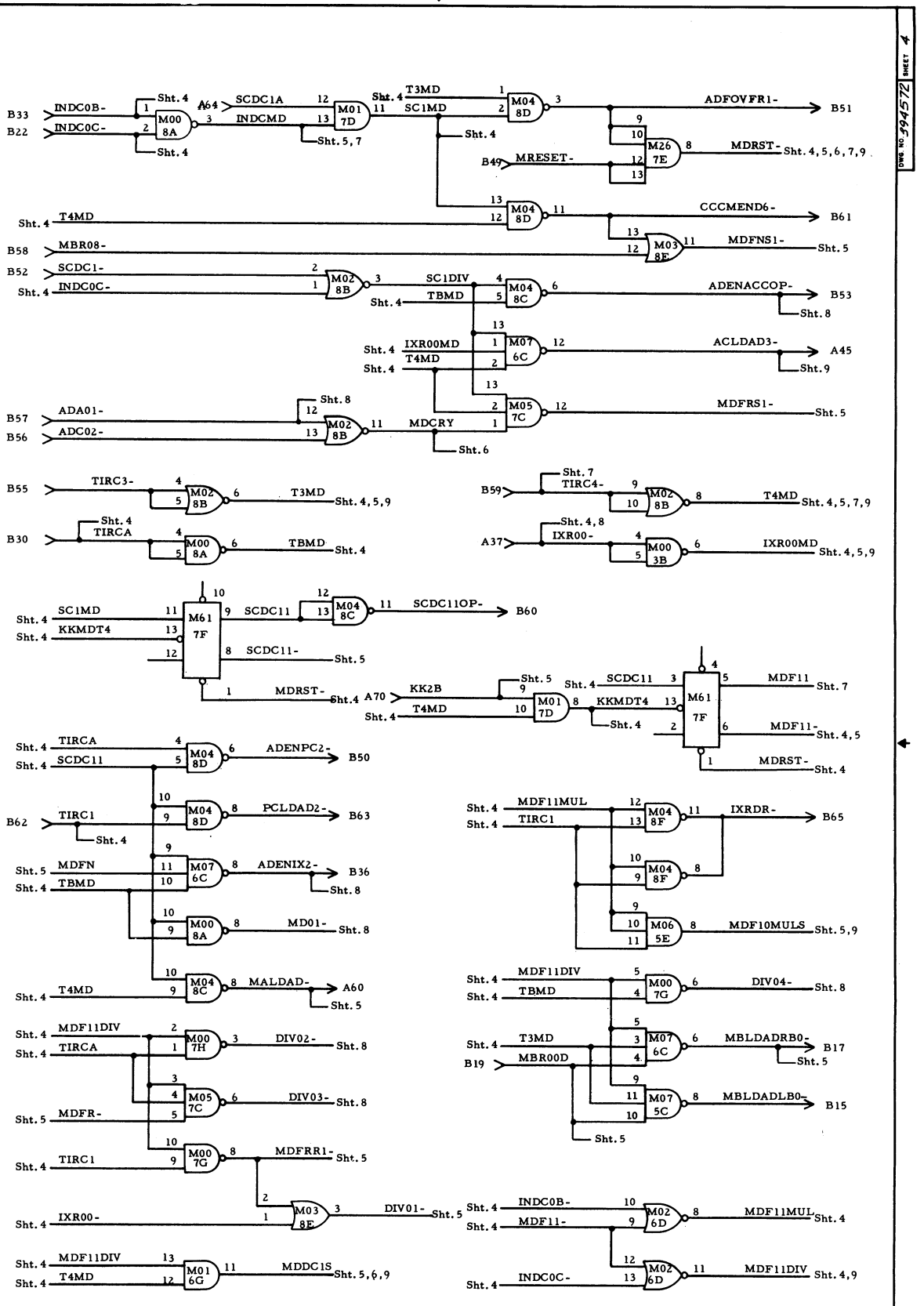
RAYTHEON COMPUTER FORM 67-0087



BLOCK DIAGRAM

CODE IDENT NO.	SIZE		REV
49956	C	394572	A
SCALE None		SHEET 3	

RAYTHEON COMPUTER FORM 67-0087

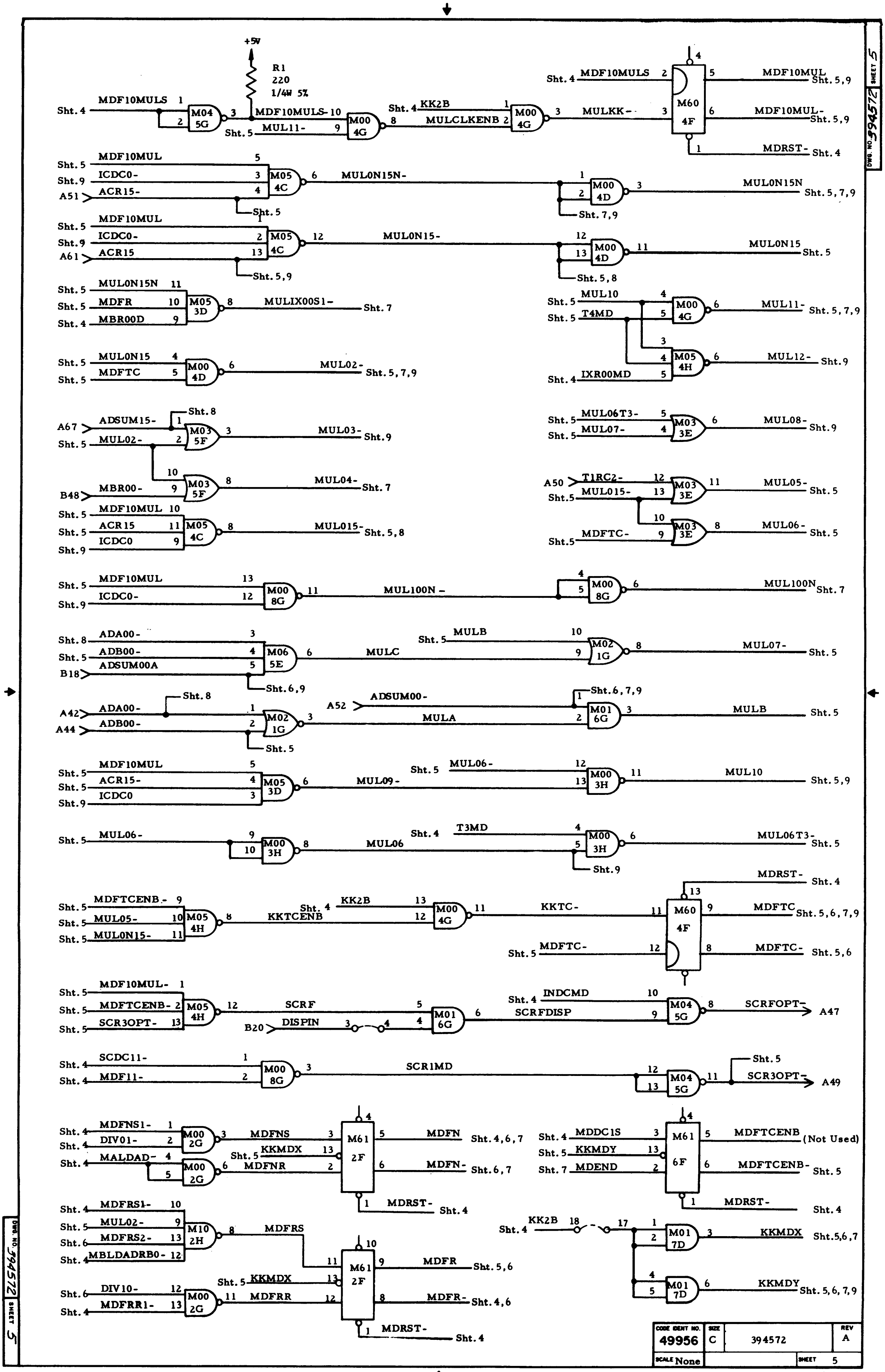


DWG NO. 394572 SHEET 4

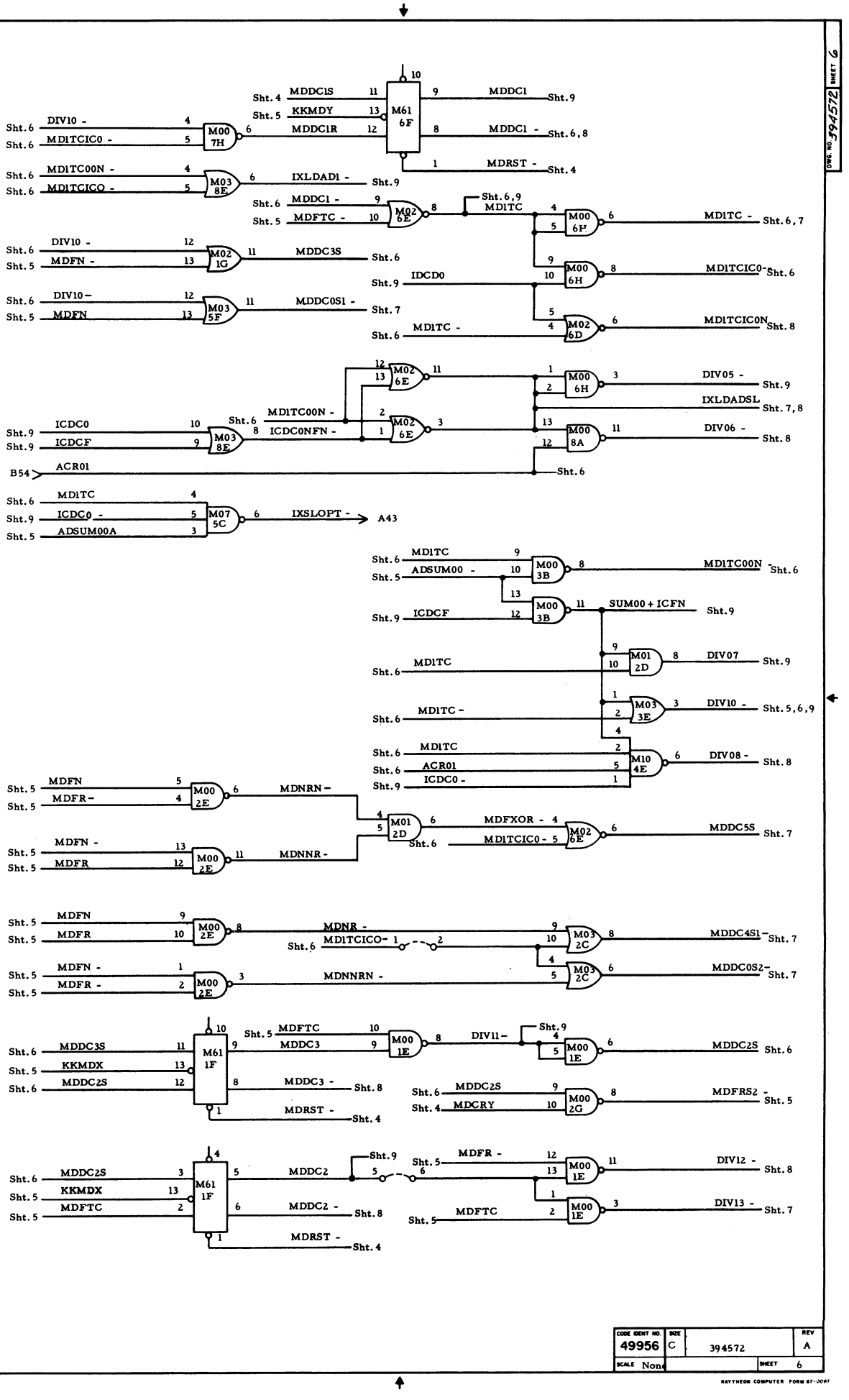
DWG NO. 394572 SHEET 4

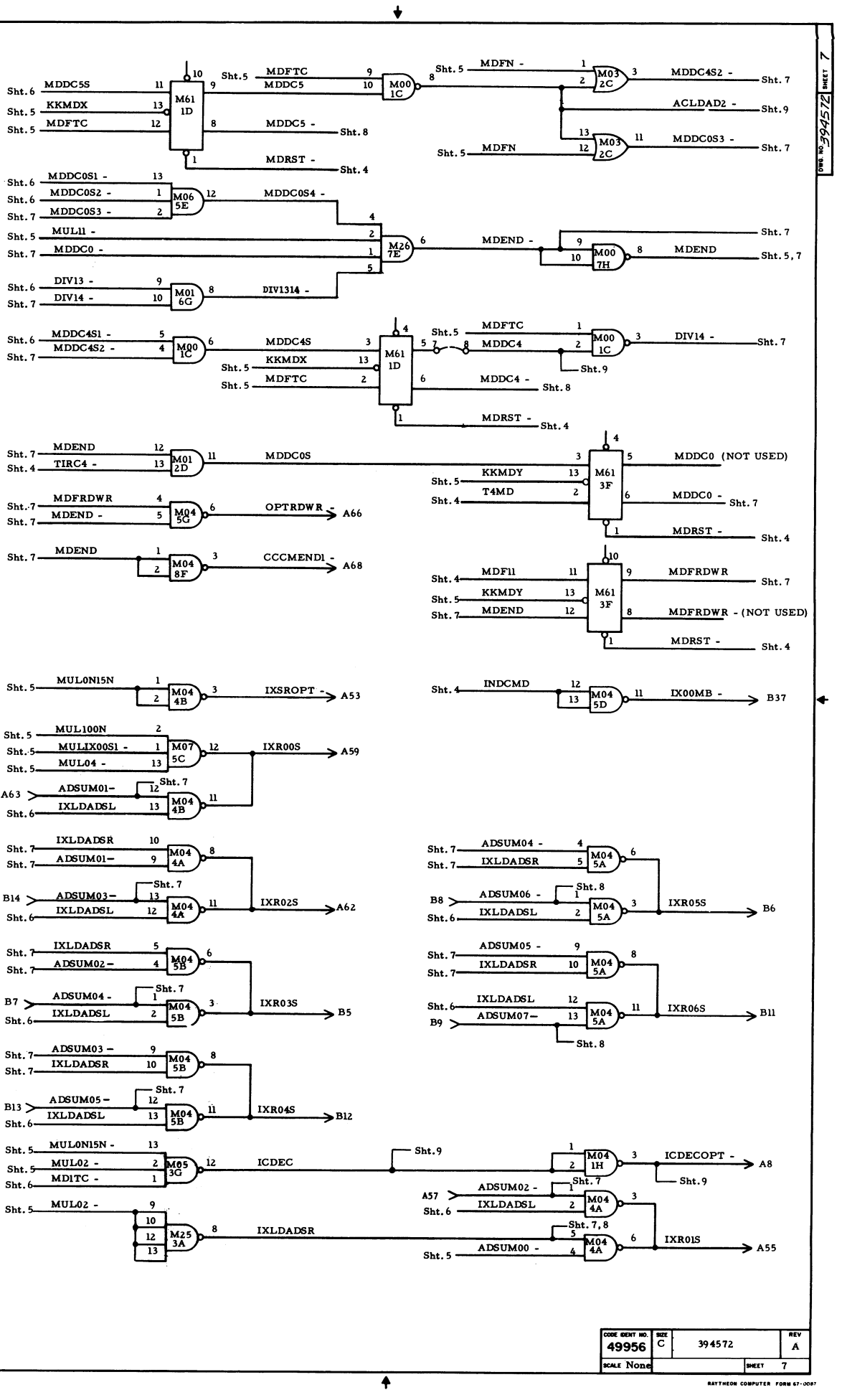
CODE IDENT NO.	SIZE		REV
49956	C	394572	A
SCALE None		SHEET 4	

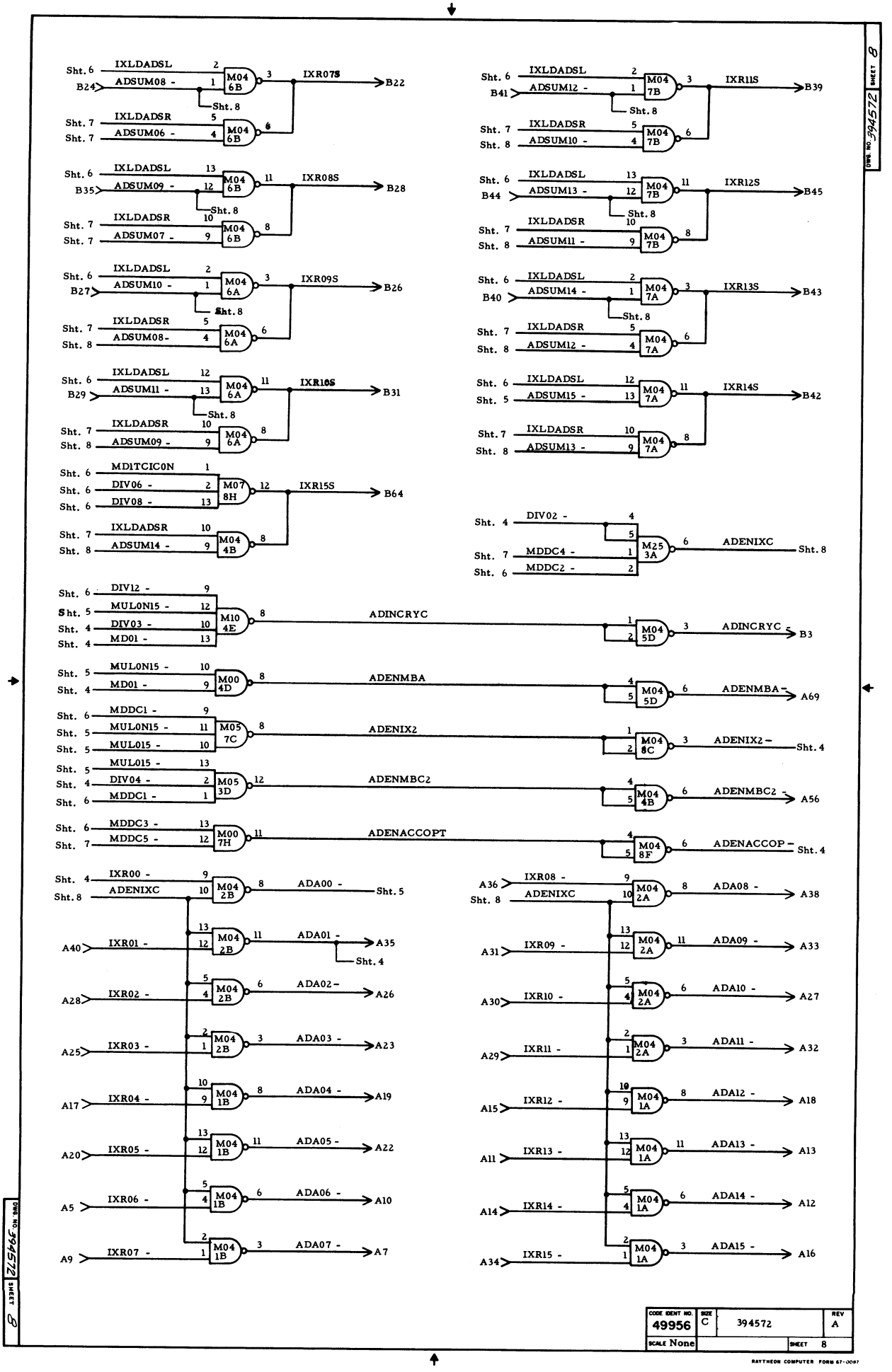
RAYTHEON COMPUTER FORM 67-0087

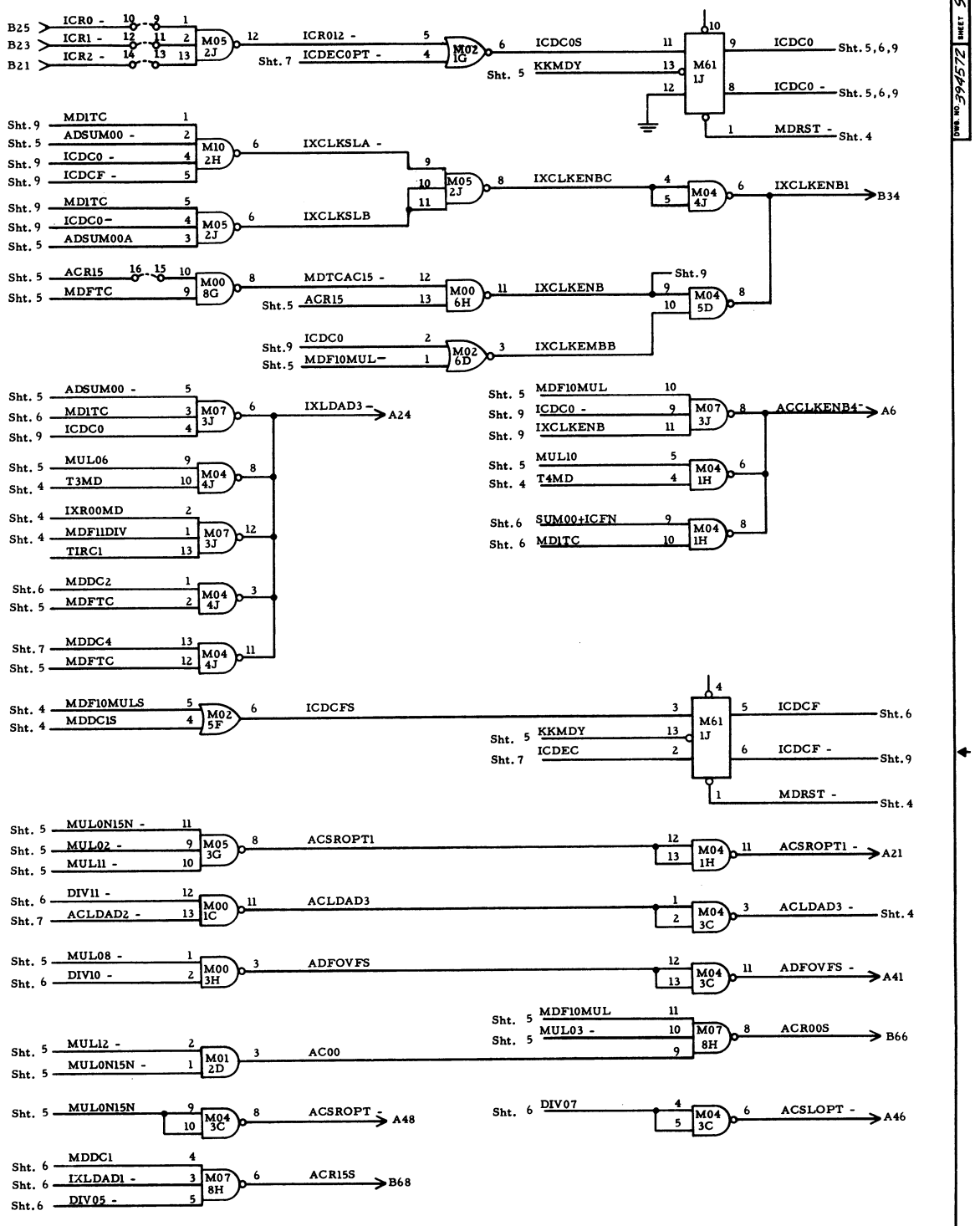


RAYTHEON COMPUTER FORM 67-0087

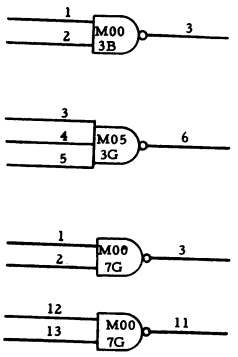

DWG. NO. 394572 SHEET 6
Sht. 4 MDDC1S 11
Sht. 5 KKMDY 13
M61 6F
10
9 MDDC1 Sht. 9
8 MDDC1 - Sht. 6,8
1 MDRST - Sht. 4
Sht. 6 DIV10 - 4
Sht. 6 MD1TCIC0 - 5
M00 7H
6 MDDC1R 12
Sht. 6 MD1TC00N - 4
Sht. 6 MD1TCICO - 5
M03 8E
6 IXLDAD1 - Sht. 9
Sht. 6 MDDC1 - 9
Sht. 5 MDFTC - 10
M02 6E
8
Sht. 6,9 MD1TC
4 M00 6F 6 MD1TC - Sht. 6,7
9 M00 6H 8 MD1TCIC0 - Sht. 6
5 M02 6D 6 MD1TCIC0N - Sht. 8
Sht. 6 DIV10 - 12
Sht. 5 MDFN - 13
M02 1G
11 MDDC3S Sht. 6
Sht. 6 DIV10 - 12
Sht. 5 MDFN 13
M03 5F
11 MDDC0S1 - Sht. 7
Sht. 9 IDCD0
Sht. 6 MD1TC -
12 M02 6E 11
13 M02 6E 3
1 M00 6H 3 DIV05 - Sht. 9
IXLDADSL Sht. 7,8
13 M00 8A 11 DIV06 - Sht. 8
12 Sht. 6
Sht. 6 MD1TC00N - 2
Sht. 9 ICDC0 10
Sht. 9 ICDCF 9
M03 8E
8 ICDC0NFN - 1
B54 ACR01
Sht. 6 MD1TC 4
Sht. 9 ICDC0 - 5
Sht. 5 ADSUM00A 3
M07 5C
6 IXSLOPT - A43
Sht. 6 MD1TC 9
Sht. 5 ADSUM00 - 10
M00 3B 8 MD1TC00N - Sht. 6
13
Sht. 9 ICDCF 12
M00 3B 11 SUM00 + ICFN Sht. 9
9
Sht. 6 MD1TC 10
M01 2D 8 DIV07 Sht. 9
1
Sht. 6 MD1TC - 2
M03 3E 3 DIV10 - Sht. 5,6,9
4
Sht. 6 MD1TC 2
Sht. 6 ACR01 5
Sht. 9 ICDC0 - 1
M10 4E 6 DIV08 - Sht. 8
Sht. 5 MDFN 5
Sht. 5 MDFR - 4
M00 2E 6 MDNRN -
4
5 M01 2D 6 MDFXOR - 4
Sht. 6 MD1TCIC0 - 5
M02 6E 6 MDDC5S Sht. 7
Sht. 5 MDFN - 13
Sht. 5 MDFR 12
M00 2E 11 MDNNR -
Sht. 5 MDFN 9
Sht. 5 MDFR 10
M00 2E 8 MDNR -
9
Sht. 6 MD1TCICO - 1 2
10 M03 2C 8 MDDC4S1 - Sht. 7
4
5 M03 2C 6 MDDC0S2 - Sht. 7
Sht. 5 MDFN - 1
Sht. 5 MDFR - 2
M00 2E 3 MDNNRN -
10
Sht. 6 MDDC3S 11
Sht. 5 KKMDX 13
Sht. 6 MDDC2S 12
M61 1F
9
Sht. 5 MDFTC 10
MDDC3 9
M00 1E 8 DIV11 -
Sht. 9 4
5 M00 1E 6 MDDC2S Sht. 6
8 MDDC3 - Sht. 8
1 MDRST - Sht. 4
Sht. 6 MDDC2S 9
Sht. 4 MDCRY 10
M00 2G 8 MDFRS2 - Sht. 5
4
Sht. 6 MDDC2S 3
Sht. 5 KKMDX 13
Sht. 5 MDFTC 2
M61 1F
5 MDDC2 Sht. 9
6 MDDC2 - Sht. 8
1 MDRST - Sht. 4
Sht. 5 MDFR - 12
6
13 M00 1E 11 DIV12 - Sht. 8
1
Sht. 5 MDFTC 2 M00 1E 3 DIV13 - Sht. 7
DWG. NO. 394572 SHEET 6
CODE IDENT NO. 49956
SIZE C
394572
REV A
SCALE None
SHEET 6
RAYTHEON COMPUTER FORM 67-0087

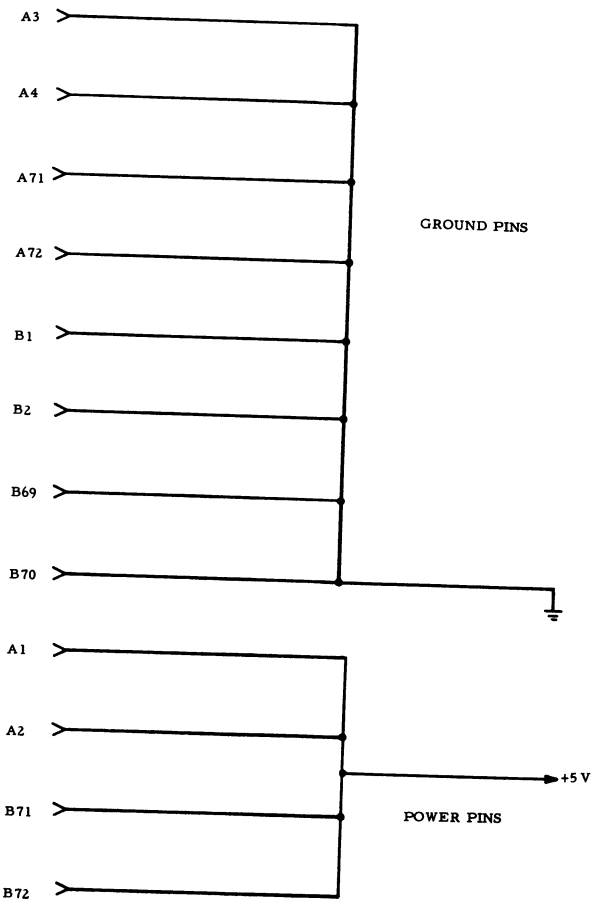

Sht. 6 MDDC5S 11
Sht. 5 KKMDX 13
Sht. 5 MDFTC 12
M61 1D
10
9
8
1
MDRST - Sht. 4
Sht. 5 MDFTC 9
MDDC5 10
M00 1C
MDDC5 - Sht. 8
Sht. 5 MDFN - 1
2
M03 2C
3
MDDC4S2 - Sht. 7
ACLDAD2 - Sht. 9
13
12
M03 2C
11
MDDC0S3 - Sht. 7
Sht. 5 MDFN
Sht. 6 MDDC0S1 - 13
Sht. 6 MDDC0S2 - 1
Sht. 7 MDDC0S3 - 2
M06 5E
12
MDDC0S4 -
4
2
1
5
M26 7E
6
MDEND -
Sht. 7
9
10
M00 7H
8
MDEND
Sht. 5, 7
Sht. 5 MULL1 -
Sht. 7 MDDC0 -
Sht. 6 DIV13 - 9
Sht. 7 DIV14 - 10
M01 6G
8
DIV1314 -
Sht. 6 MDDC4S1 - 5
Sht. 7 MDDC4S2 - 4
M00 1C
6
MDDC4S
3
M61 1D
4
5 7 8
Sht. 5 KKMDX 13
Sht. 5 MDFTC 2
6
MDDC4 - Sht. 8
1
MDRST - Sht. 4
Sht. 5 MDFTC 1
MDDC4
M00 1C
3
DIV14 - Sht. 7
Sht. 9
Sht. 7 MDEND 12
Sht. 4 TIRC4 - 13
M01 2D
11
MDDC0S
4
3
M61 3F
5
MDDC0 (NOT USED)
Sht. 5 KKMDY 13
Sht. 4 T4MD 2
6
MDDC0 - Sht. 7
1
MDRST - Sht. 4
Sht. 7 MDFRDWR 4
Sht. 7 MDEND - 5
M04 5G
6
OPTRDWR - A66
Sht. 7 MDEND 1
2
M04 8F
3
CCCMEND1 - A68
Sht. 4 MDF11 11
Sht. 5 KKMDY 13
Sht. 7 MDEND 12
M61 3F
10
9
MDFRDWR
Sht. 7
8
MDFRDWR - (NOT USED)
1
MDRST - Sht. 4
Sht. 5 MUL0N15N 1
2
M04 4B
3
IXSROPT - A53
Sht. 4 INDCMD 12
13
M04 5D
11
IX00MB - B37
Sht. 5 MUL100N 2
Sht. 5 MULIX00S1 - 1
Sht. 5 MUL04 - 13
M07 5C
12
IXR00S A59
A63 ADSUM01- 12 Sht. 7
Sht. 6 IXLDADSL 13
M04 4B
11
Sht. 7 IXLDADSR 10
Sht. 7 ADSUM01- 9
M04 4A
8
B14 ADSUM03- 13 Sht. 7
Sht. 6 IXLDADSL 12
M04 4A
11
IXR02S A62
Sht. 7 IXLDADSR 5
Sht. 7 ADSUM02- 4
M04 5B
6
B7 ADSUM04 - 1 Sht. 7
Sht. 6 IXLDADSL 2
M04 5B
3
IXR03S B5
Sht. 7 ADSUM03 - 9
Sht. 7 IXLDADSR 10
M04 5B
8
B13 ADSUM05 - 12 Sht. 7
Sht. 6 IXLDADSL 13
M04 5B
11
IXR04S B12
Sht. 5 MUL0N15N - 13
Sht. 5 MUL02 - 2
Sht. 6 MD1TC - 1
M05 3G
12
ICDEC
Sht. 9
1
2
M04 1H
3
ICDECOPT - A8
Sht. 9
Sht. 5 MUL02 - 9
10
12
13
M25 3A
8
IXLDADSR
A57 ADSUM02 - 1 Sht. 7
Sht. 6 IXLDADSL 2
M04 4A
3
Sht. 7, 8 5
Sht. 5 ADSUM00 - 4
M04 4A
6
IXR01S A55
Sht. 7 IXLDADSR 10
Sht. 7 ADSUM04 - 4
M04 5A
6
Sht. 7 IXLDADSR 5
B8 ADSUM06 - 1 Sht. 8
Sht. 6 IXLDADSL 2
M04 5A
3
IXR05S B6
Sht. 7 ADSUM05 - 9
Sht. 7 IXLDADSR 10
M04 5A
8
Sht. 6 IXLDADSL 12
B9 ADSUM07- 13 Sht. 8
M04 5A
11
IXR06S B11
DWG. NO. 394572 SHEET 7
DWG. NO. 394572 SHEET 7
CODE IDENT NO. 49956
SIZE C
394572
REV A
SCALE None
SHEET 7
RAYTHEON COMPUTER FORM 67-0087


Sht. 6 IXLDADSL 2 M04 6B 3 IXR07S → B22
B24 ADSUM08 - 1
Sht. 8
Sht. 7 IXLDADSR 5 M04 6B 6
Sht. 7 ADSUM06 - 4
Sht. 6 IXLDADSL 13 M04 6B 11 IXR08S → B28
B35 ADSUM09 - 12
Sht. 8
Sht. 7 IXLDADSR 10 M04 6B 8
Sht. 7 ADSUM07 - 9
Sht. 6 IXLDADSL 2 M04 6A 3 IXR09S → B26
B27 ADSUM10 - 1
Sht. 8
Sht. 7 IXLDADSR 5 M04 6A 6
Sht. 8 ADSUM08 - 4
Sht. 6 IXLDADSL 12 M04 6A 11 IXR10S → B31
B29 ADSUM11 - 13
Sht. 8
Sht. 7 IXLDADSR 10 M04 6A 8
Sht. 8 ADSUM09 - 9
Sht. 6 MDITCICON 1
Sht. 6 DIV06 - 2 M07 8H 12 IXR15S → B64
Sht. 6 DIV08 - 13
Sht. 7 IXLDADSR 10 M04 4B 8
Sht. 8 ADSUM14 - 9
Sht. 6 IXLDADSL 2 M04 7B 3 IXR11S → B39
B41 ADSUM12 - 1
Sht. 8
Sht. 7 IXLDADSR 5 M04 7B 6
Sht. 8 ADSUM10 - 4
Sht. 6 IXLDADSL 13 M04 7B 11 IXR12S → B45
B44 ADSUM13 - 12
Sht. 8
Sht. 7 IXLDADSR 10 M04 7B 8
Sht. 8 ADSUM11 - 9
Sht. 6 IXLDADSL 2 M04 7A 3 IXR13S → B43
B40 ADSUM14 - 1
Sht. 8
Sht. 7 IXLDADSR 5 M04 7A 6
Sht. 8 ADSUM12 - 4
Sht. 6 IXLDADSL 12 M04 7A 11 IXR14S → B42
Sht. 5 ADSUM15 - 13
Sht. 8
Sht. 7 IXLDADSR 10 M04 7A 8
Sht. 8 ADSUM13 - 9
Sht. 4 DIV02 - 4
5
Sht. 7 MDDC4 - 1 M25 3A 6 ADENIXC → Sht. 8
Sht. 6 MDDC2 - 2
Sht. 6 DIV12 - 9
Sht. 5 MUL0N15 - 12
Sht. 4 DIV03 - 10 M10 4E 8 ADINCRYC
Sht. 4 MD01 - 13
1
2 M04 5D 3 ADINCRYC → B3
Sht. 5 MUL0N15 - 10
Sht. 4 MD01 - 9 M00 4D 8 ADENMBA
4
5 M04 5D 6 ADENMBA → A69
Sht. 6 MDDC1 - 9
Sht. 5 MUL0N15 - 11
Sht. 5 MUL015 - 10 M05 7C 8 ADENIX2
1
2 M04 8C 3 ADENIX2 → Sht. 4
Sht. 5 MUL015 - 13
Sht. 4 DIV04 - 2 M05 3D 12 ADENMBC2
4
5 M04 4B 6 ADENMBC2 → A56
Sht. 6 MDDC1 - 1
Sht. 6 MDDC3 - 13
Sht. 7 MDDC5 - 12 M00 7H 11 ADENACCOPT
4
5 M04 8F 6 ADENACCOP → Sht. 4
Sht. 4 IXR00 - 9
Sht. 8 ADENIXC 10 M04 2B 8 ADA00 - → Sht. 5
A40 IXR01 - 13 12 M04 2B 11 ADA01 - → A35
Sht. 4
A28 IXR02 - 5 4 M04 2B 6 ADA02 - → A26
A25 IXR03 - 2 1 M04 2B 3 ADA03 - → A23
A17 IXR04 - 10 9 M04 1B 8 ADA04 - → A19
A20 IXR05 - 13 12 M04 1B 11 ADA05 - → A22
A5 IXR06 - 5 4 M04 1B 6 ADA06 - → A10
A9 IXR07 - 2 1 M04 1B 3 ADA07 - → A7
A36 IXR08 - 9
Sht. 8 ADENIXC 10 M04 2A 8 ADA08 - → A38
A31 IXR09 - 13 12 M04 2A 11 ADA09 - → A33
A30 IXR10 - 5 4 M04 2A 6 ADA10 - → A27
A29 IXR11 - 2 1 M04 2A 3 ADA11 - → A32
A15 IXR12 - 10 9 M04 1A 8 ADA12 - → A18
A11 IXR13 - 13 12 M04 1A 11 ADA13 - → A13
A14 IXR14 - 5 4 M04 1A 6 ADA14 - → A12
A34 IXR15 - 2 1 M04 1A 3 ADA15 - → A16
DWG NO 394572 SHEET 8
DWG NO 394572 SHEET 8
CODE IDENT NO. 49956 SIZE C 394572 REV A
SCALE None SHEET 8
RAYTHEON COMPUTER FORM 67-0087


B25 ICR0 -
B23 ICR1 -
B21 ICR2 -
M05 2J
ICR012 -
Sht. 7 ICDEC0PT -
M02 1G
ICDC0S
Sht. 5 KKMDY
M61 1J
ICDC0
ICDC0 -
MDRST -
Sht. 4
Sht. 9 MD1TC
Sht. 5 ADSUM00 -
Sht. 9 ICDC0 -
Sht. 9 ICDCF -
M10 2H
IXCLKSLA -
Sht. 9 MD1TC
Sht. 9 ICDC0-
Sht. 5 ADSUM00A
M05 2J
IXCLKSLB
M05 2J
IXCLKENBC
M04 4J
IXCLKENB1
B34
Sht. 5 ACR15
Sht. 5 MDFTC
M00 8G
MDTCAC15 -
Sht. 5 ACR15
M00 6H
IXCLKENB
Sht. 9
M04 5D
Sht. 9 ICDC0
Sht. 5 MDF10MUL-
M02 6D
IXCLKEMBB
Sht. 5 ADSUM00 -
Sht. 6 MD1TC
Sht. 9 ICDC0
M07 3J
IXLDAD3 -
A24
Sht. 5 MUL06
Sht. 4 T3MD
M04 4J
Sht. 4 IXR00MD
Sht. 4 MDF11DIV
TIRC1
M07 3J
Sht. 6 MDDC2
Sht. 5 MDFTC
M04 4J
Sht. 7 MDDC4
Sht. 5 MDFTC
M04 4J
Sht. 5 MDF10MUL
Sht. 9 ICDC0 -
Sht. 9 IXCLKENB
M07 3J
ACCLKENB4-
A6
Sht. 5 MUL10
Sht. 4 T4MD
M04 1H
Sht. 6 SUM00+ICFN
Sht. 6 MD1TC
M04 1H
Sht. 4 MDF10MULS
Sht. 4 MDDC1S
M02 5F
ICDCFS
Sht. 5 KKMDY
Sht. 7 ICDEC
M61 1J
ICDCF
Sht. 6
ICDCF -
Sht. 9
MDRST -
Sht. 4
Sht. 5 MUL0N15N -
Sht. 5 MUL02 -
Sht. 5 MUL11 -
M05 3G
ACSROPT1
M04 1H
ACSROPT1 -
A21
Sht. 6 DIV11 -
Sht. 7 ACLDAD2 -
M00 1C
ACLDAD3
M04 3C
ACLDAD3 -
Sht. 4
Sht. 5 MUL08 -
Sht. 6 DIV10 -
M00 3H
ADFOVFS
M04 3C
ADFOVFS -
A41
Sht. 5 MDF10MUL
Sht. 5 MUL03 -
M07 8H
ACR00S
B66
Sht. 5 MUL12 -
Sht. 5 MUL0N15N -
M01 2D
AC00
Sht. 5 MUL0N15N
M04 3C
ACSROPT -
A48
Sht. 6 DIV07
M04 3C
ACSLOPT -
A46
Sht. 6 MDDC1
Sht. 6 IXLDAD1 -
Sht. 6 DIV05 -
M07 8H
ACR15S
B68
DWG. NO. 394572 SHEET 9
DWG. NO. 394572 SHEET 9
CODE IDENT NO. 49956
SIZE C
394572
REV A
SCALE None
SHEET 9
RAYTHEON COMPUTER FORM 67-0087

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	C	394572	A
SCALE None			SHEET 10

RAYTHEON COMPUTER FORM 67-0087

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER E.O.20880			MF	MS	RA	7/11/70
A	RELEASED PER EO. 19311			HP	MS	MS	7/17/70
B	REVISED PER EO 21438			HP	MS	MS	7/17/70

DWG. NO. 394577 SHEET 1 OF 15

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GLOSSARY

ACDLY	ACKNOWLEDGE DELAY FLIP-FLOP
CCFCLK	CLOCK CONTROL
CCFSYN1	CONTROL PULSE SYNCHRONIZING FLIP-FLOP
DBWRTEN	WRITE ENABLE SIGNAL
DMBRDR	DMA BUFFER REGISTER DIRECT RESET
DMBRENB	DMA BUFFER REGISTER ENABLE
DMCLDEN	DMA CLOCK LOAD ENABLE SIGNAL TO LOAD DMBR
DMFREN	DMA REQUEST SIGNAL
DMFRQX	DMA REQUEST FLIP-FLOP
DMTX-	TX
DRDEN	DMA READ ENABLE SIGNAL
DTO-	TO
DWRTEN	DMA WRITE ENABLE SIGNAL
GLBP	GATE LEFT BYTE PARITY
GRBP	GATE RIGHT BYTE PARITY
KEXT2-	CLOCK
KKACKX	CLOCK
KKBRX	DMA WRITE CLOCK
LBP	LEFT BYTE PARITY
MAKX-	DMA ACKNOWLEDGE ON LINE X
MARXXS	MEMORY ADDRESS REGISTER SET TERM FOR BIT XX
MALDADLB	MEMORY BUFFER LOAD FROM ADDER LEFT BYTE
MALDADRB	MEMORY BUFFER LOAD FROM ADDER RIGHT BYTE
MCDIXX	DMA DATA TO MEMORY
MCDIPL	DMA PARITY TO MEMORY
MCDOXX	DATA FROM MEMORY TO DMA
MCDOPL	PARITY
MCENMB	MEMORY DATA IN FROM MEMORY BUFFER REGISTER
MCRW-	ENABLE MEMORY READ OR WRITE
MCWRENT-	ENTER DATA FROM CONTROL PANEL TO MEMORY
MMADXX-	MEMORY ADDRESS
MMDIXX-	DATA TO DMA BUFFER REGISTER
MMDOXX-	DATA FROM DMA BUFFER REGISTER
MRESET-	MASTER RESET
MRQX-	MEMORY REQUEST LINE X
MWTX-	WRITE SIGNAL LINE X
PARER	PARITY ERROR
RBP	RIGHT BYTE PARITY
RBPE	RIGHT BYTE PARITY ERROR
REXT2-	EXTERNAL RESET
SCDCØ	SEQUENCER DECODED STATE ZERO
SCDC1FØ	RUN, SINGLE COMMAND OR SINGLE STEP FUNCTION
STBINH-	ENABLE OUTPUT OR INPUT STROBE
TIRCφ	TO SIGNAL
TIRC1	T1 SIGNAL
TIRC2	T2 SIGNAL
TIRC3-	T3 SIGNAL
TIRC4	T4 SIGNAL

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
M00	531593-006
M01	531593-005
M04	531593-014
M05	531593-004
M06	531593-017
M15	531593-001
M26	531593-012
M51	531593-013
M60/M60A	531593-018
M61	531593-011
M74	531594-001
TX3	531596-002

(4) JUMPER PIN 9 OF 1D TO PIN 7 OF 1D (GROUND) IF PARITY W/O DMA

3. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" AND "D" CONNECTORS. C1B THRU C36B, D1B THRU D36B.

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⟫ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			
REVISION	B	B	B	A	A	A	A	A	A	A	A	A	A	B	B			

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON:
DECIMALS ANGLES
.XX ±.03 ± 0° 30'
.XXX ±.010
2. BREAK SHARP CORNERS .015 MAX
FINISH:

DRAWN	M. Fagnani	7-15-70
CHECK	M. Eaton	7/16/70
APPR	R. ALLEN	6-5-70
APPR		

NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

DMA/ PARITY (LOGIC DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	394577
SCALE NONE		SHEET 1 OF 15

RAYTHEON COMPUTER FORM 67-

DWG. NO. 394577 SHEET 1 OF 15

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACDLY	S	A14	6
ACDLY-	S	B51	6
CCFCLK	S	A7	6
CCFSYNI		A66	14
DMT2-	S	C14	7
DMT4-	S	C22	7
DMTO-	S	C23	7
KEXT2-	S	C15	7
KKC		A11	6
MAK2-	S	C10	6
MAK3-	S	C11	6
MAK4-	S	C9A	5
MAK5-	S	C12	5
MAK6-	S	C8A	5
MAK7-	S	C13	5
MARØ1S	S	B49	12
MARØ2S	S	B57	12
MARØ3S	S	B58	12
MARØ4S	S	B47	12
MARØ5S	S	B45	12
MARØ6S	S	B61	12
MARØ7S	S	B59	12
MARØ8S	S	B46	12
MARØ9S	S	B43	12
MAR1ØS	S	B63	12
MAR11S	S	B64	12
MAR12S	S	B41	12
MAR13S	S	B39	12
MAR14S	S	B67	12
MAR15S	S	B65	12
MBLDADLB		B53	14
MBLDADRB		B14	14
MCDIØ3	S	B34	8
MCDIØ6	S	B25	9
MCDIØØ	S	B21	8
MCDIØ1	S	B33	8
MCDIØ2	S	B35	8
MCDIØ4	S	B23	9
MCDIØ5	S	B22	9
MCDIØ7	S	B19	9
MCDIØ8	S	B9	1Ø
MCDIØ9	S	A53	1Ø
MCDI1Ø	S	B1Ø	1Ø
MCDI11	S	A51	1Ø
MCDI12	S	A55	11
MCDI13	S	A49	11
MCDI14	S	A57	11
MCDI15	S	A47	11
MCDIPL	S	B30	13
MCDIPR	S	B15	13
MCDOØØ		B37	8
MCDOØ1		B31	8
MCDOØ2		B40	8
MCDOØ3		B29	8
MCDOØ4		B28	9
MCDOØ5		B17	9
MCDOØ6		B27	9
MCDOØ7		B16	9
MCDOØ8		B11	1Ø
MCDOØ9		A67	1Ø
MCDO1Ø		B13	1Ø
MCDO11		A65	1Ø
MCDO12		A59	11
MCDO13		A45	11
MCDO14		A61	11
MCDO15		A43	11
MCDOPL		A35	14
MCDOPR		A37	14
MCENMB	S	A9	6
MCRW-	S	B52	6
MCWRENT-		B55	14

SIGNAL LIST

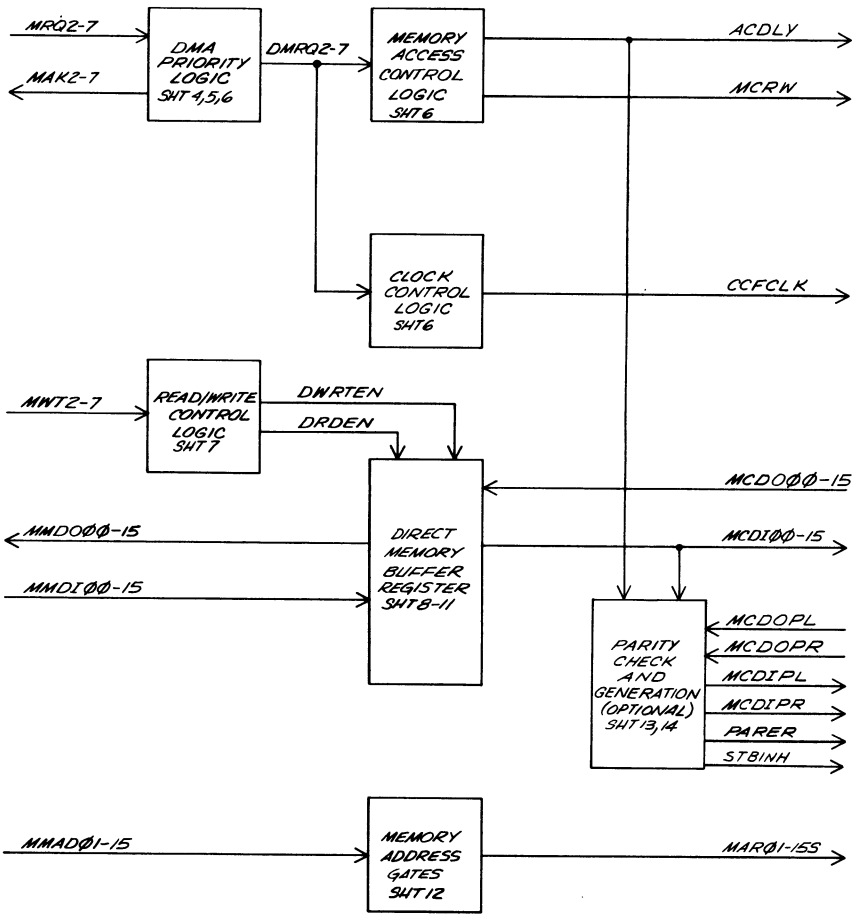
SIGNAL	SOURCE	CONN	SHEET
MMADØ1-		D25A	12
MMADØ2-		D35A	12
MMADØ3-		D36A	12
MMADØ4-		D34A	12
MMADØ5-		D24A	12
MMADØ6-		D32A	12
MMADØ7-		D33A	12
MMADØ8-		D31A	12
MMADØ9-		D23A	12
MMAD1Ø-		D29A	12
MMAD11-		D30A	12
MMAD12-		D23A	12
MMAD13-		D22A	12
MMAD14-		D26A	12
MMAD15-		D27A	12
MMDIØØ-		D20A	8
MMDIØ1-		D15A	8
MMDIØ2-		D21A	8
MMDIØ3-		D14A	8
MMDIØ4-		D12A	9
MMDIØ5-		D7A	9
MMDIØ6-		D13A	9
MMDIØ7-		D6A	9
MMDIØ8-		D4A	1Ø
MMDIØ9		C34A	1Ø
MMDI1Ø-		D5A	1Ø
MMDI11-		C32A	1Ø
MMDI12-		C3ØA	11
MMDI13-		C25A	11
MMDI14-		C31A	11
MMDI15-		C24A	11
MMDOØØ-	S	D19A	8
MMDOØ1-	S	D16A	8
MMDOØ2-	S	D18A	8
MMDOØ3-	S	D17A	8
MMDOØ4-	S	D11A	9
MMDOØ5-	S	D8A	9
MMDOØ6-	S	D1ØA	9
MMDOØ7-	S	D9A	9
MMDOØ8-	S	D3A	1Ø
MMDOØ9-	S	C35A	1Ø
MMDO1Ø-	S	D2A	1Ø
MMDO11-	S	D36A	1Ø
MMDO12-	S	C29A	11
MMDO13-	S	C26A	11
MMDO14-	S	C28A	11
MMDO15-	S	C27A	11
MRESET-		A68	14
MRQ2-		C2A	4
MRQ3-		C3A	4
MRQ4-		C4A	4
MRQ5-		C5A	4
MRQ6-		C6A	4
MRQ7-		C7A	4
MWT2-		C21A	7
MWT3-		C20A	7
MWT4-		C16A	7
MWT5-		C17A	7
MWT6-		C18A	7
MWT7-		C19A	7
PARER	S	B7	14
PARER-	S	A69	14
REXT2-	S	C33A	7
REXT2-		A63	7
SCDCØ		B3	14
SCDC1FØ		B5	14
STBINH-	S	A29	14
TIRCØ		A39	7
TIRC1		A17	14
TIRC2		A33	6
TIRC3-		A15	6
TIRC4		A41	7

DWG NO 394577 SHEET 2

DWG NO 394577 SHEET 2

CODE IDENT NO.	SIZE		REV
49956	D	394577	B
SCALE NONE		SHEET 2	

RAYTHEON COMPUTER FORM 67-0087

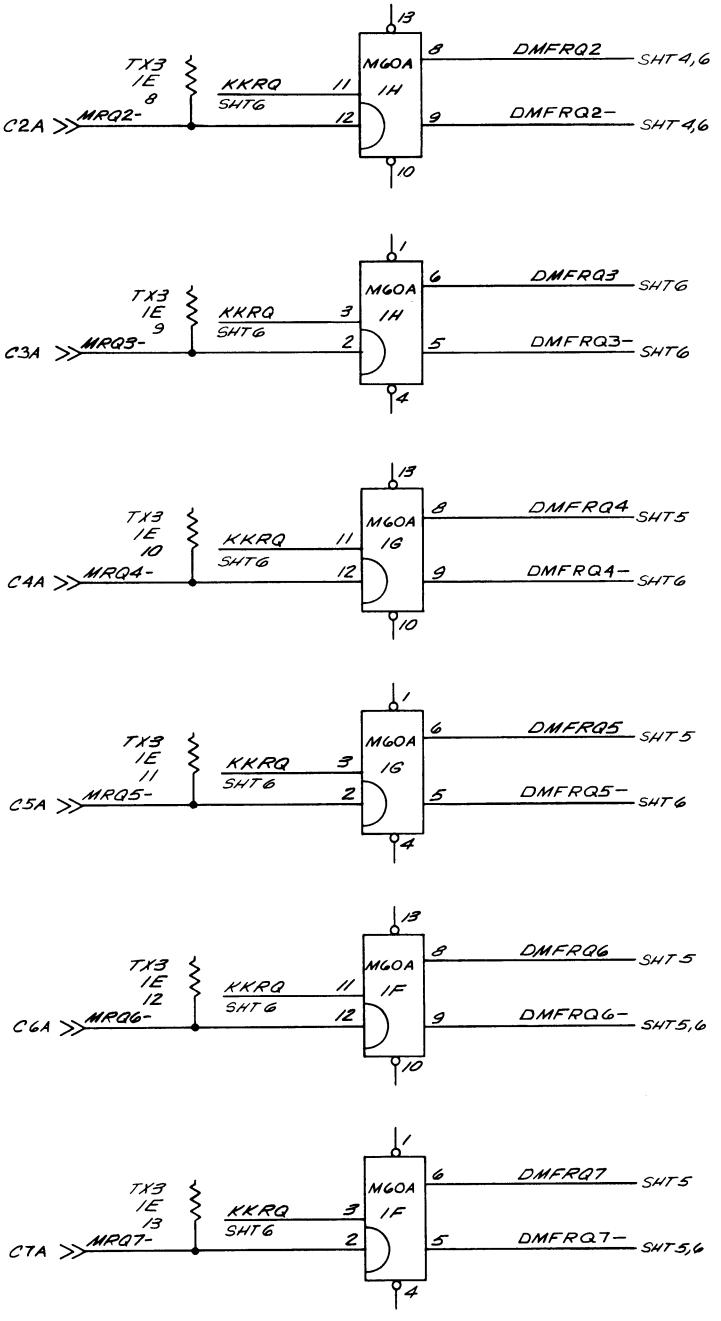


BLOCK DIAGRAM

CODE IDENT NO.	SIZE		REV
49956	D	394577	B
SCALE NONE			SHEET 3

RAYTHEON COMPUTER FORM 67-0045

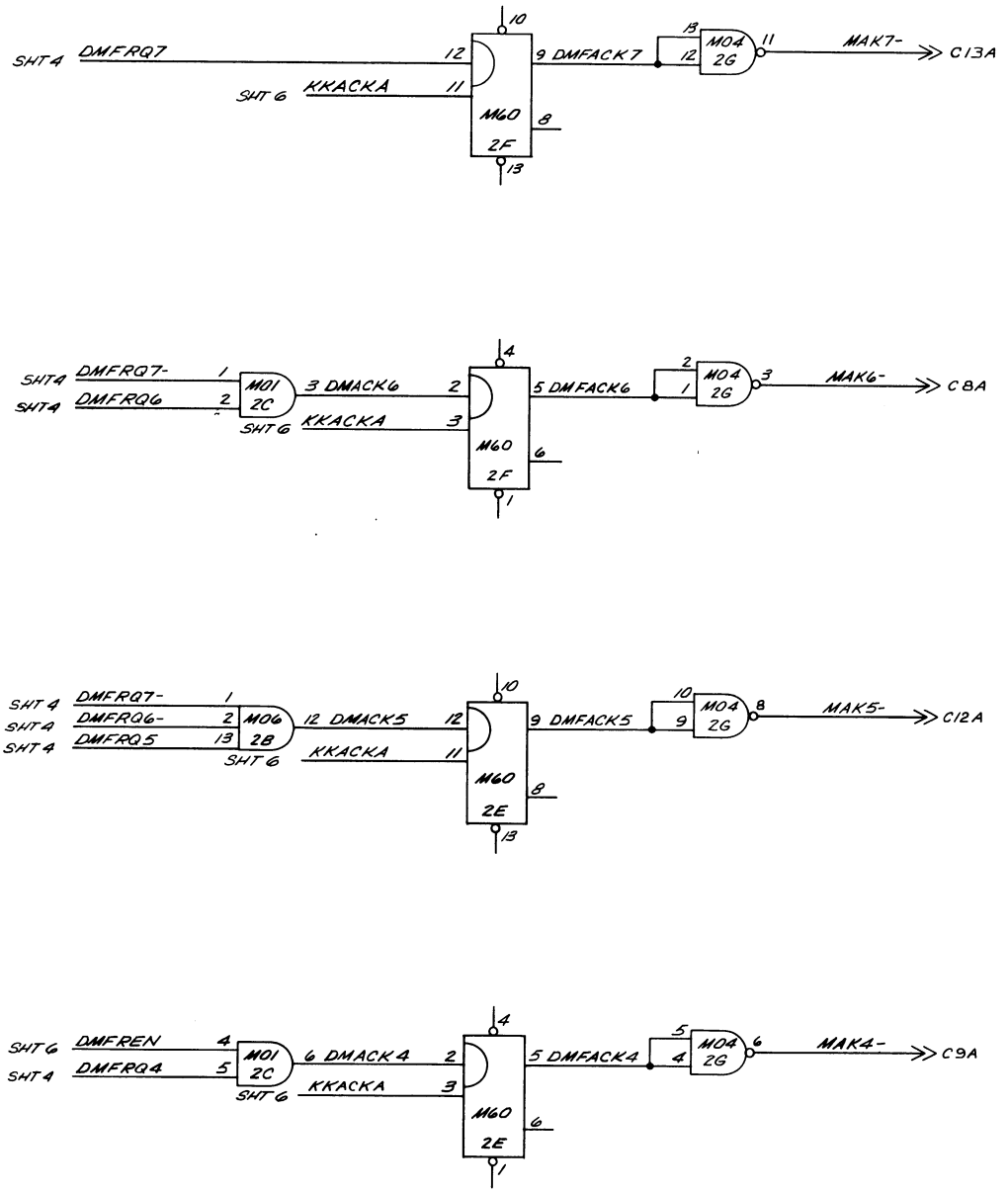
DMA REQUEST REGISTER



DWG. NO. 394577 SHEET 4 OF

CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE		SHEET 4	

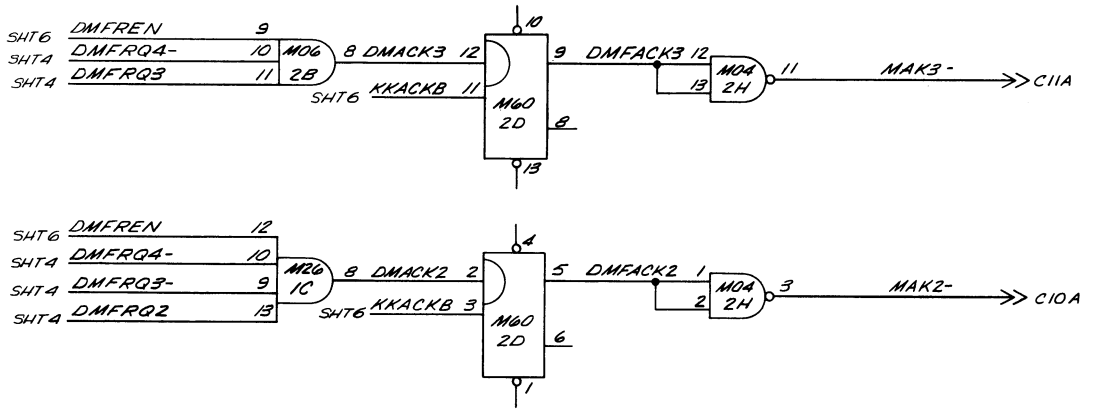
P/O DMA ACKNOWLEDGE REGISTER



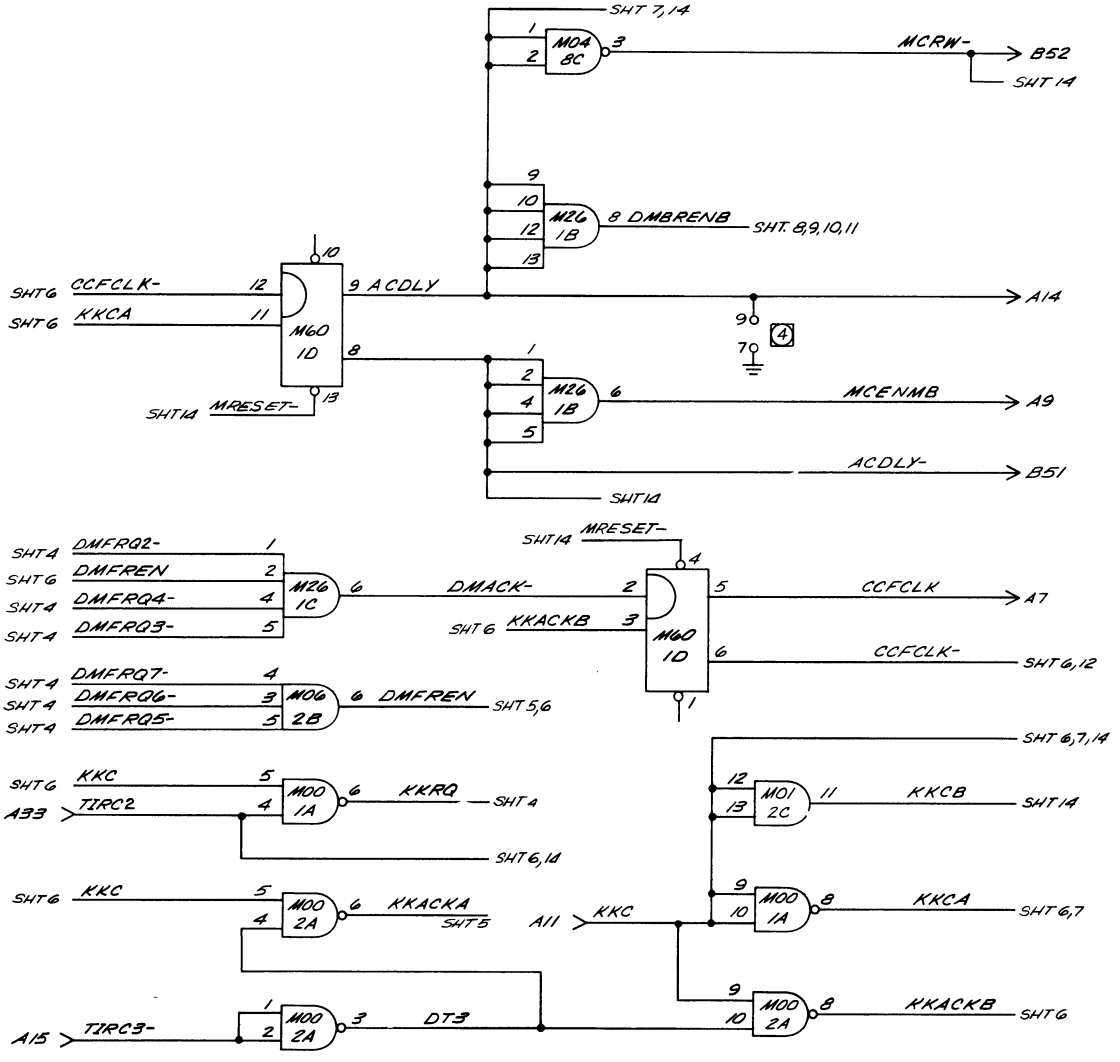
CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE		SHEET 5	

RAYTHEON COMPUTER FORM 67-0017

P/O DMA ACKNOWLEGE REGISTER

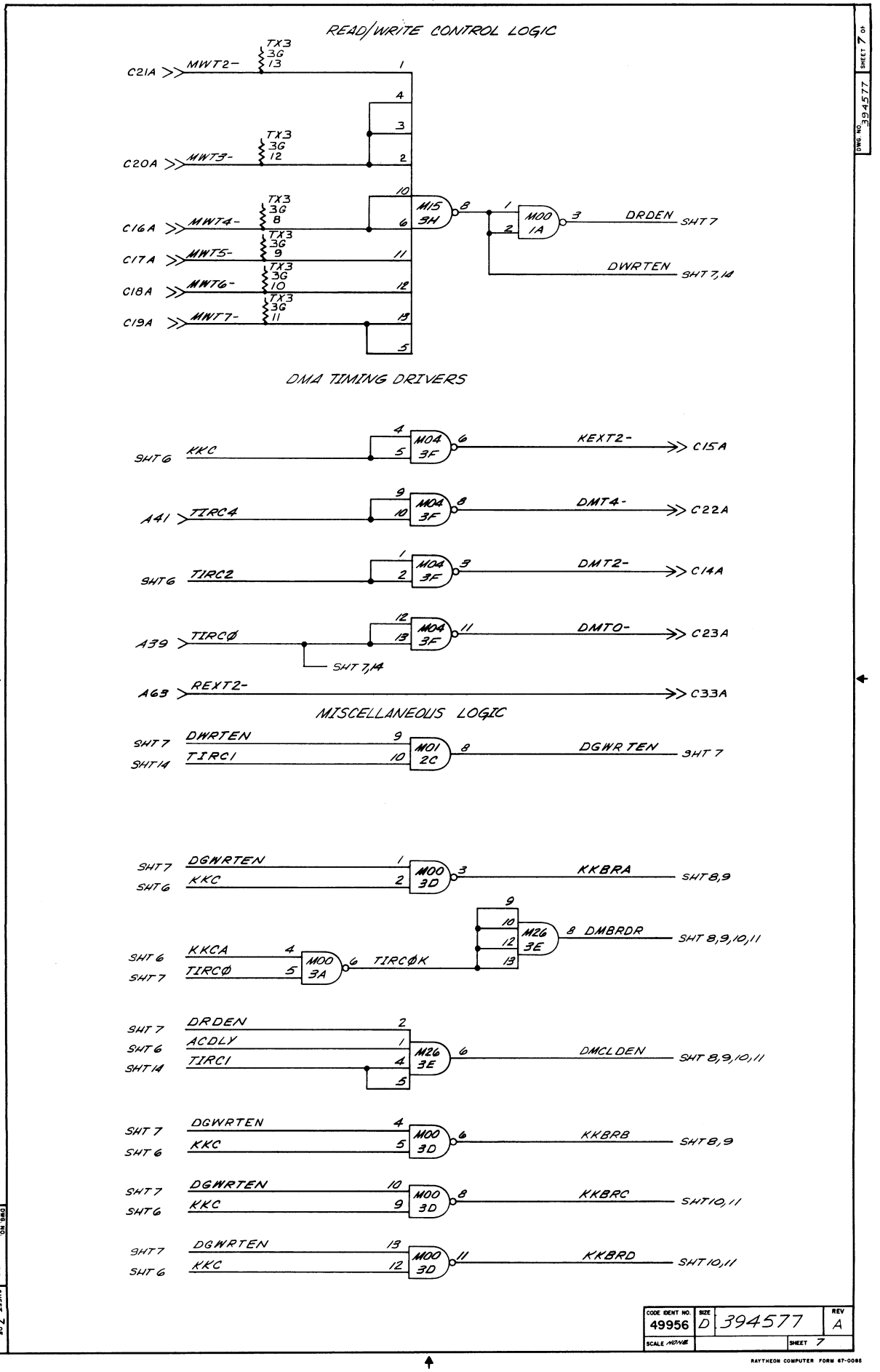


MEMORY ACCESS & CLOCK CONTROL LOGIC



CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE		SHEET 6	

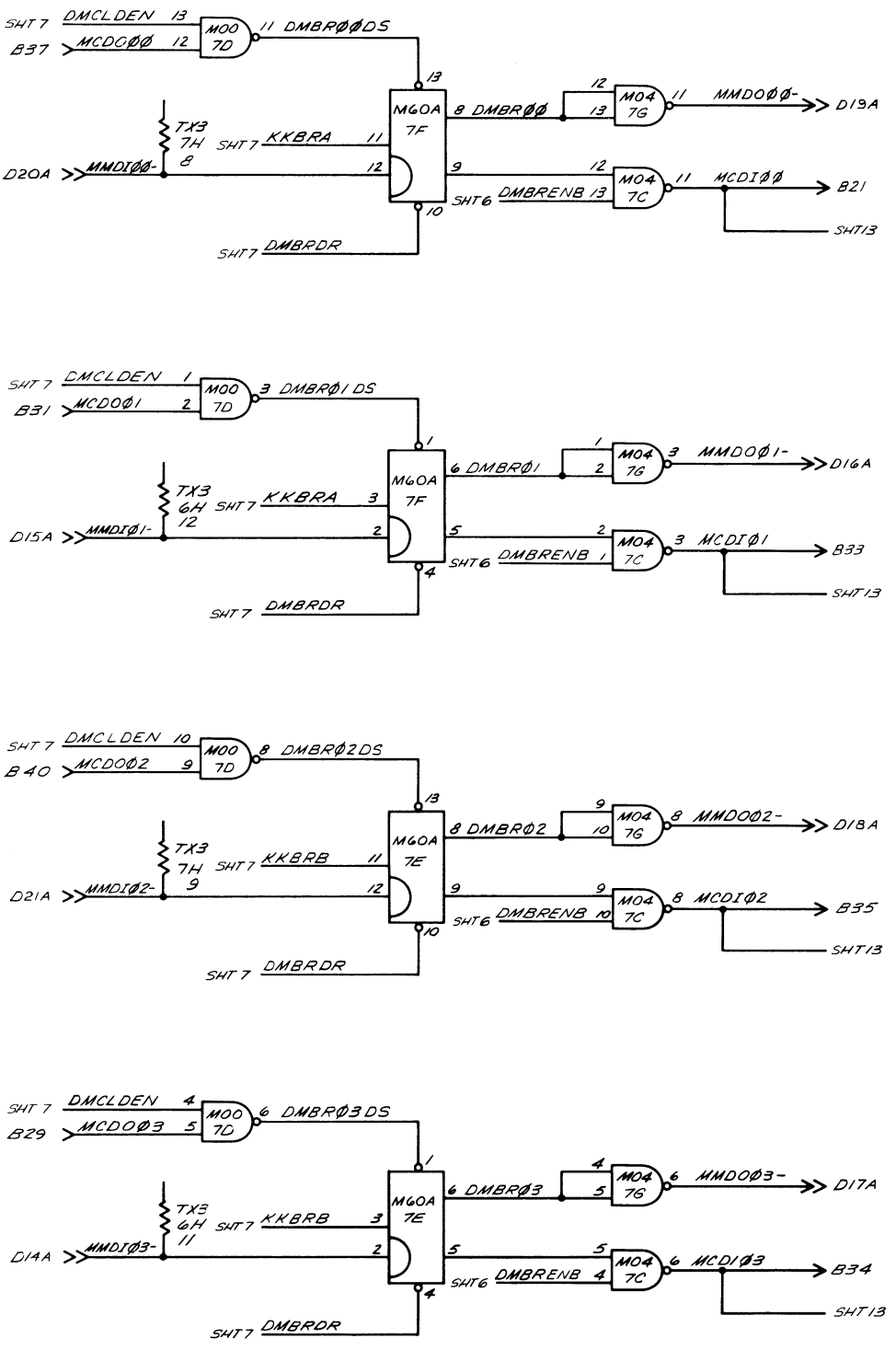
RAYTHEON COMPUTER FORM 87-0085



CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE		SHEET 7	

RAYTHEON COMPUTER FORM 67-0085

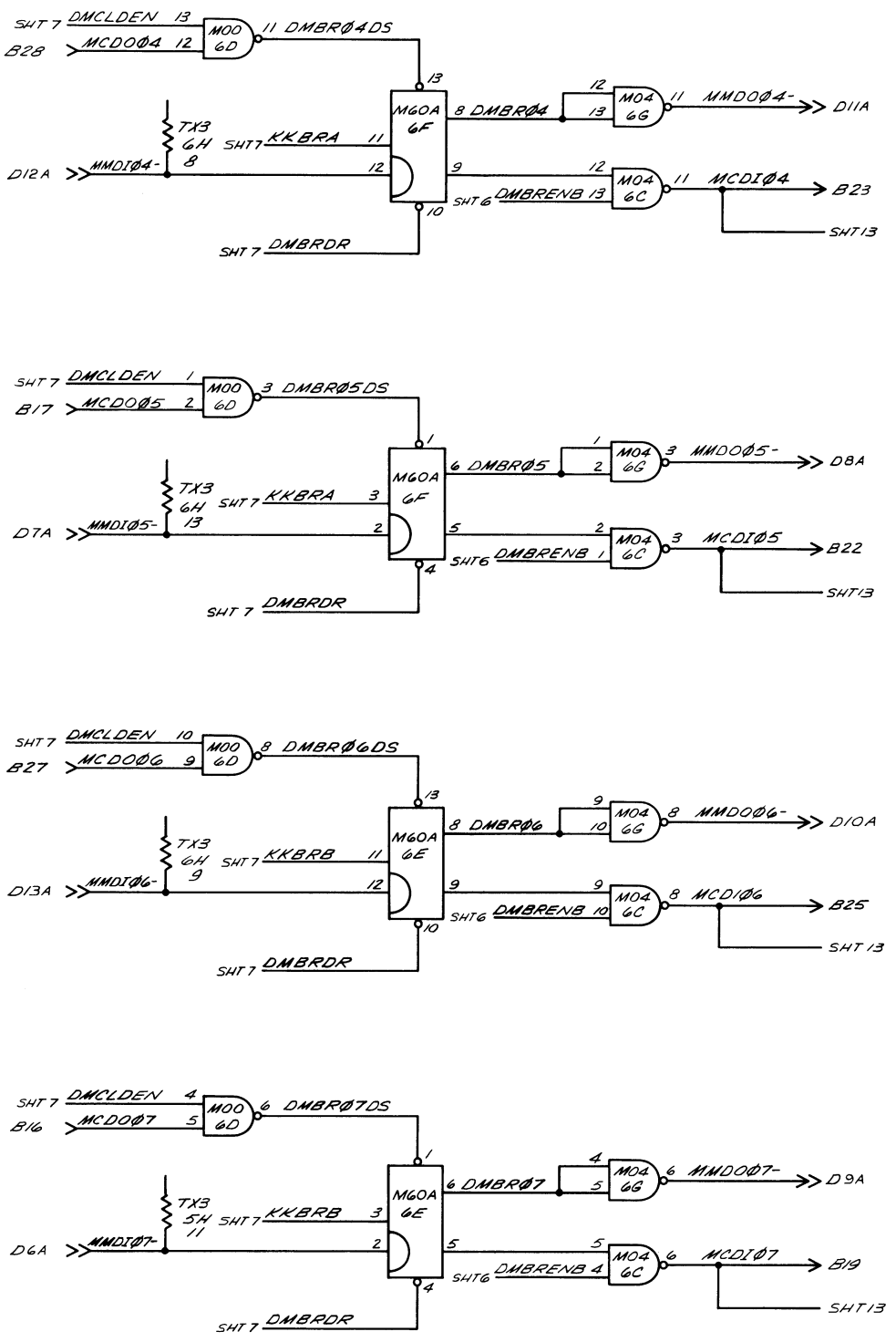
P/O DIRECT MEMORY BUFFER REGISTER



CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE			SHEET 8

RAYTHEON COMPUTER FORM 67-0086

P/O DIRECT MEMORY BUFFER REGISTER

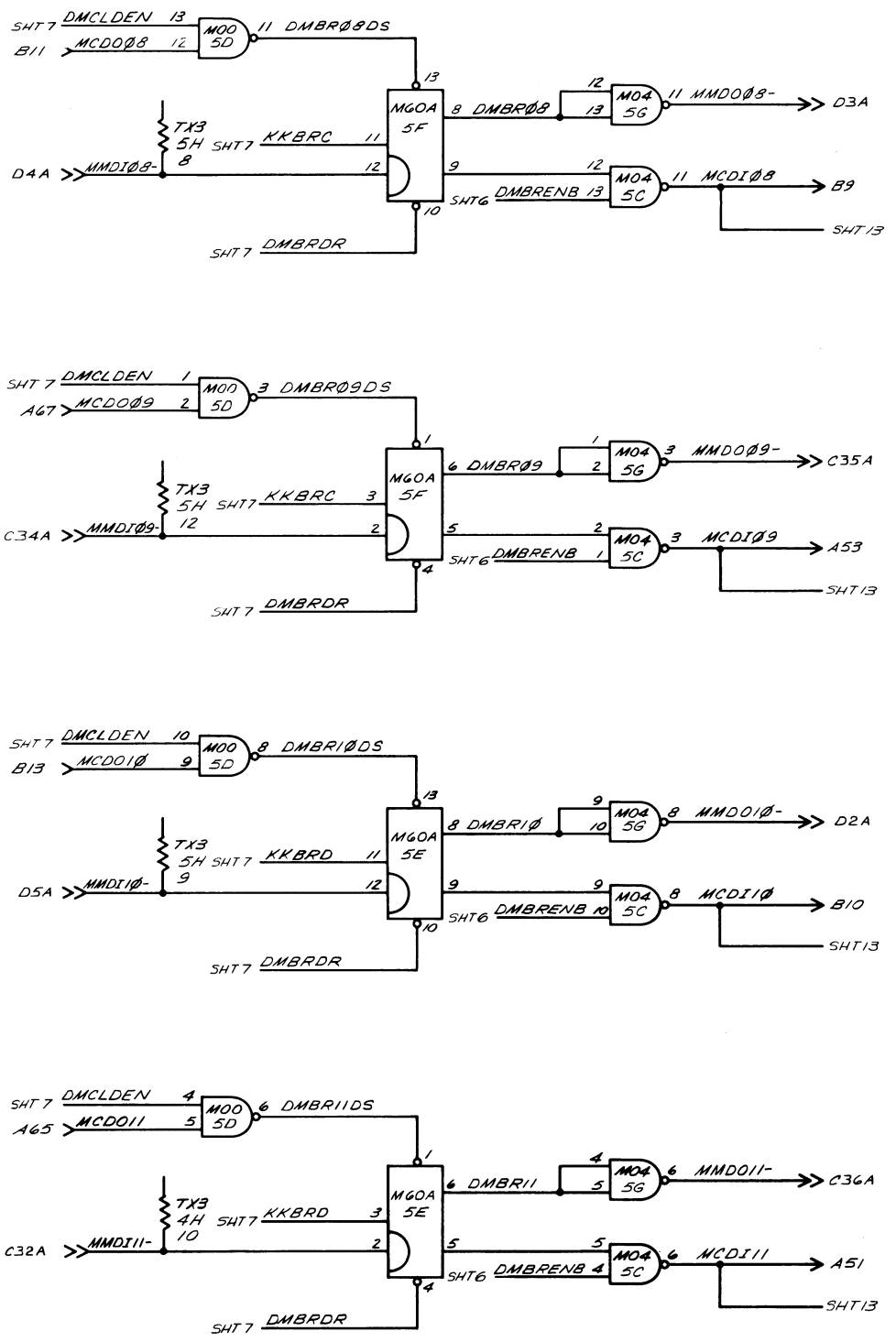


DWG. NO. 394577 SHEET 9 OF

CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE		SHEET 9	

RAYTHEON COMPUTER FORM 67-0085

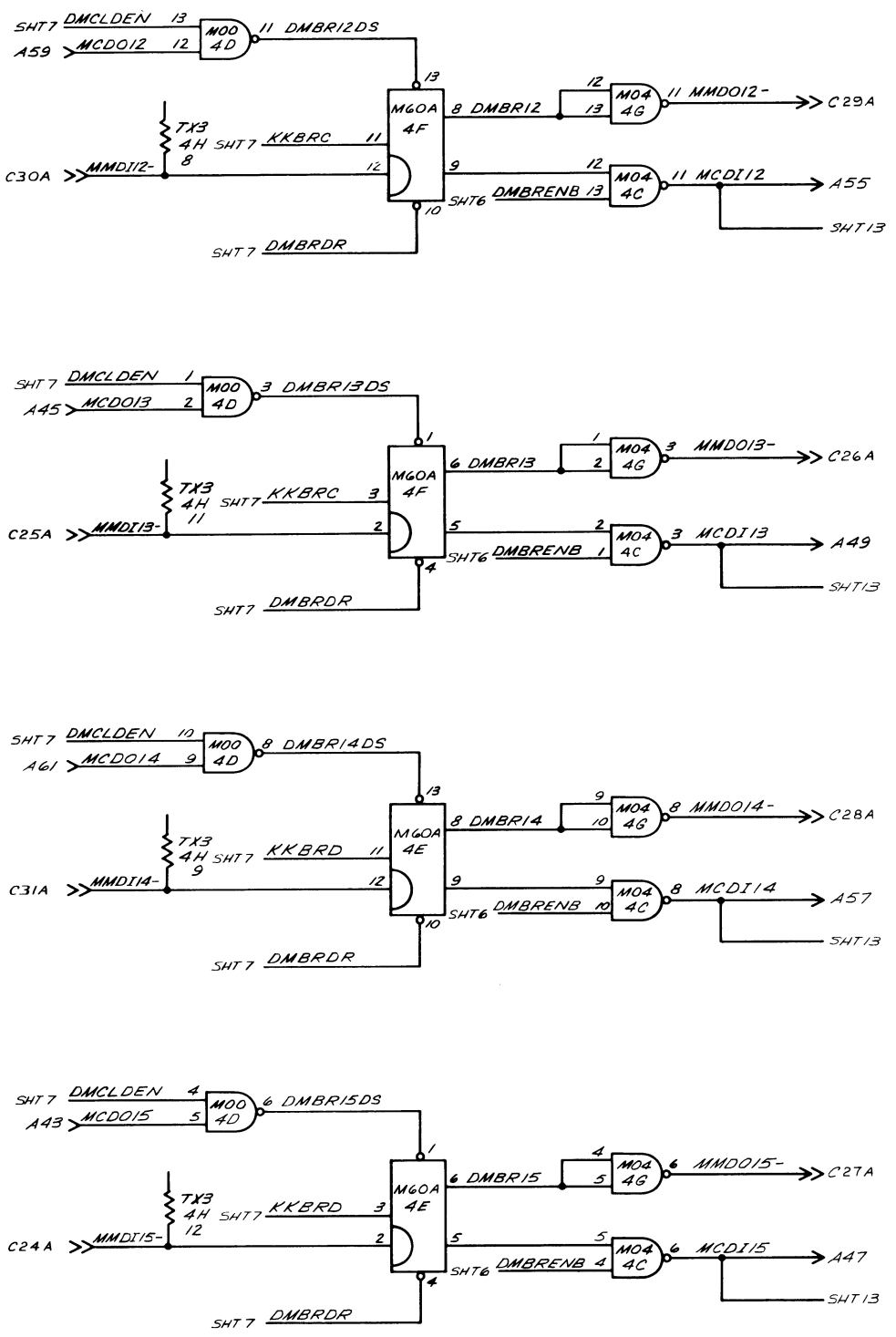
P/O DIRECT MEMORY BUFFER REGISTER



CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE			SHEET 10

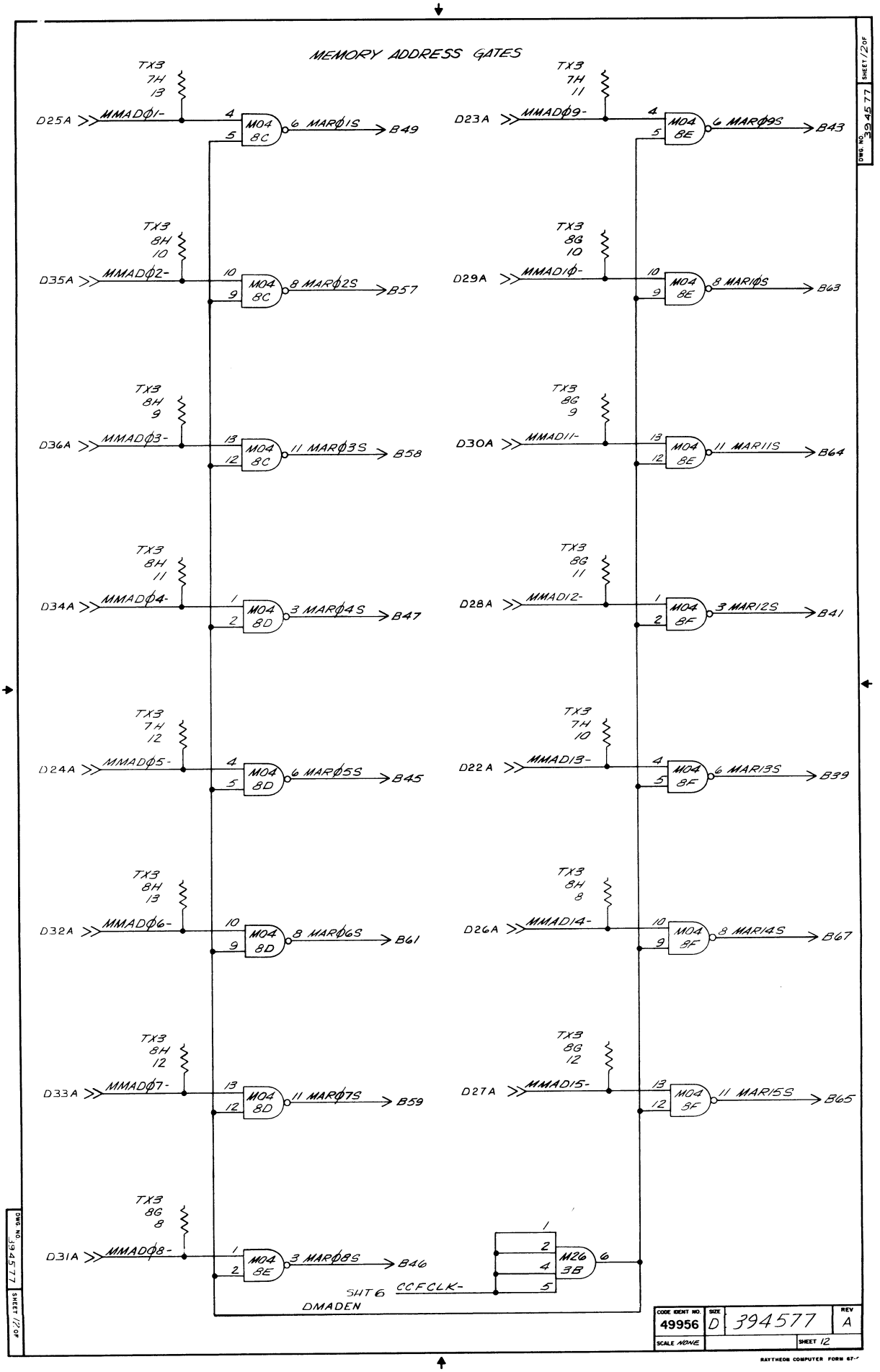
RAYTHEON COMPUTER FORM 67-0006

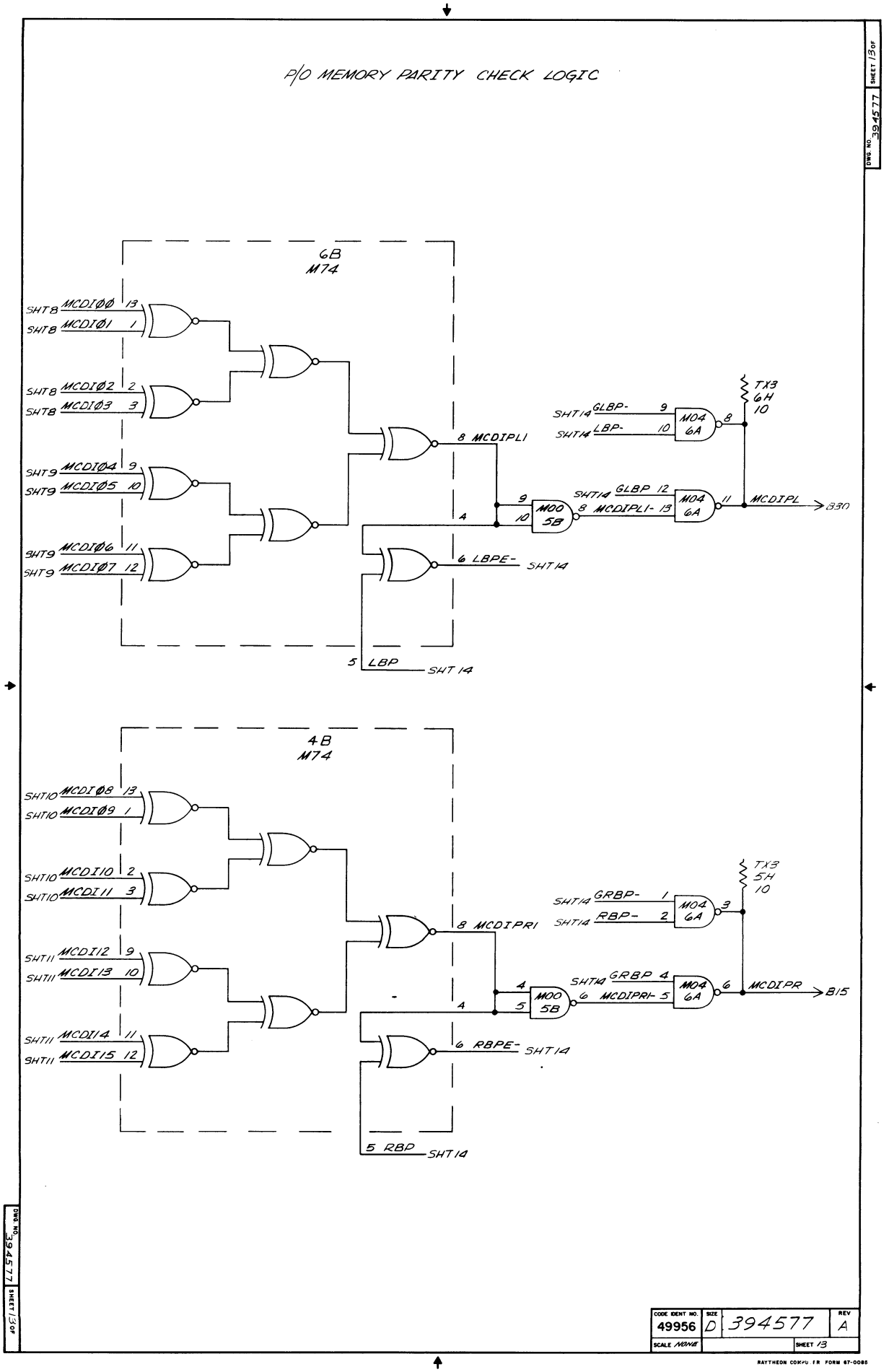
P/O DIRECT MEMORY BUFFER REGISTER

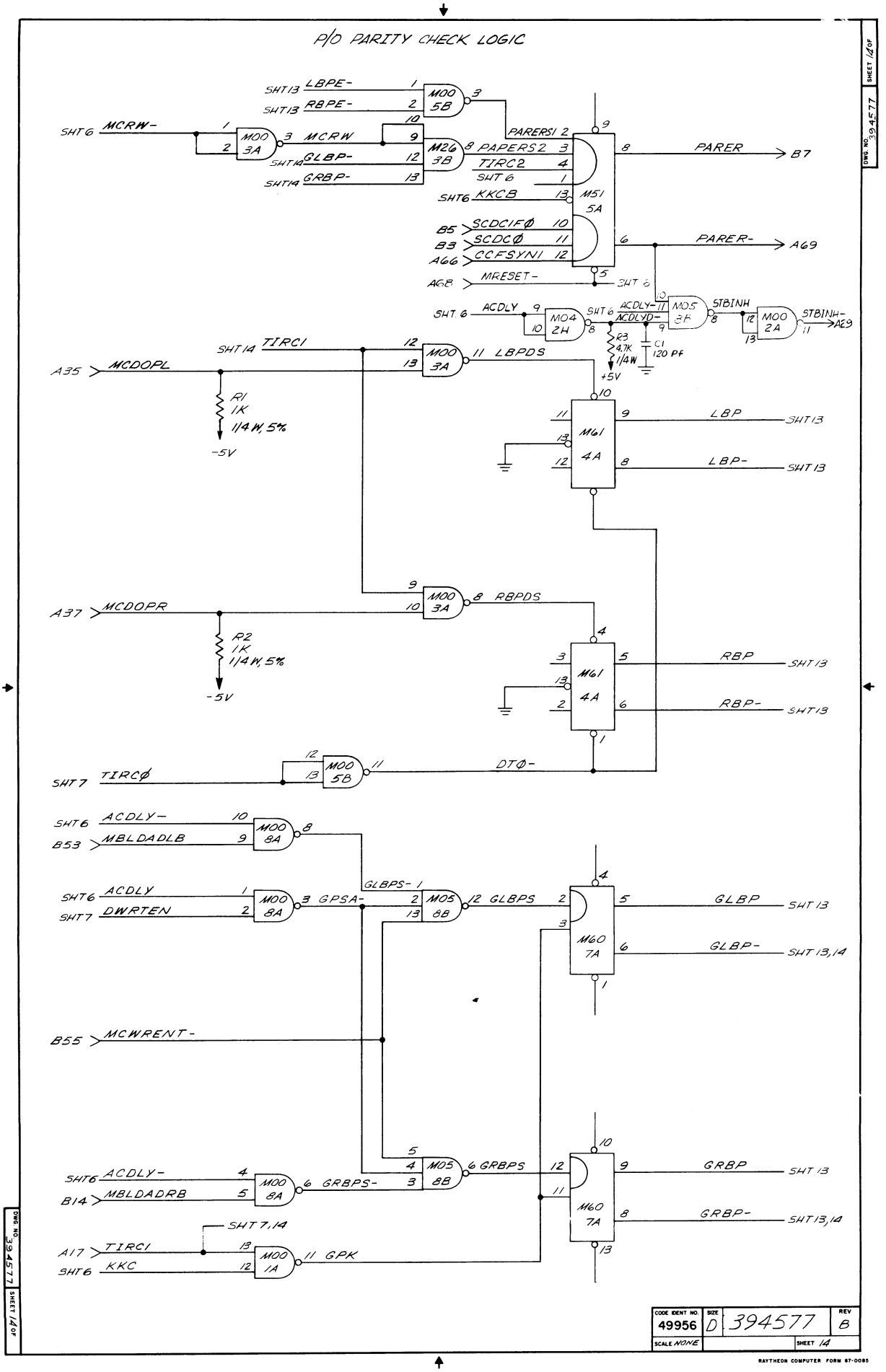


CODE IDENT NO.	SIZE		REV
49956	D	394577	A
SCALE NONE		SHEET 11	

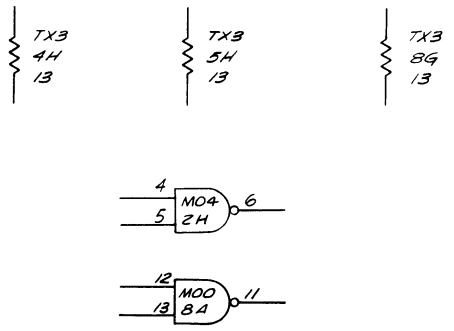
RAYTHEON COMPUTER FORM 67-0088

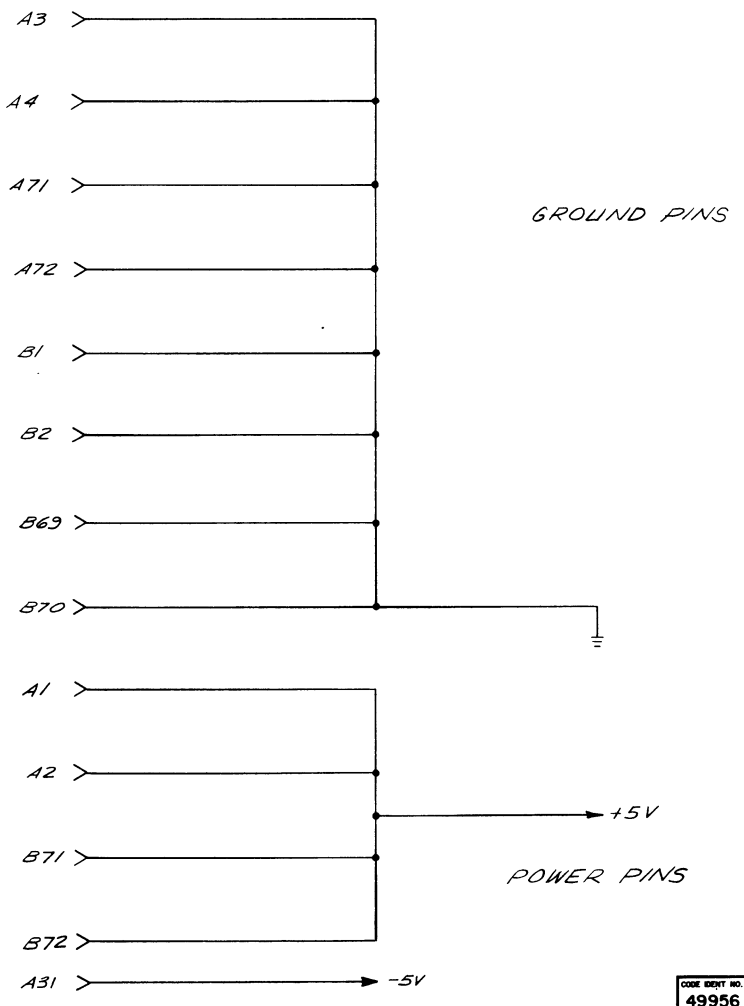

MEMORY ADDRESS GATES
TX3 7H 13
D25A
MMADØ1-
4
5
M04 8C
6 MARØ1S
B49
TX3 7H 11
D23A
MMADØ9-
4
5
M04 8E
6 MARØ9S
B43
TX3 8H 10
D35A
MMADØ2-
10
9
M04 8C
8 MARØ2S
B57
TX3 8G 10
D29A
MMADIØ-
10
9
M04 8E
8 MARIØS
B63
TX3 8H 9
D36A
MMADØ3-
13
12
M04 8C
11 MARØ3S
B58
TX3 8G 9
D30A
MMADI1-
13
12
M04 8E
11 MARI1S
B64
TX3 8H 11
D34A
MMADØ4-
1
2
M04 8D
3 MARØ4S
B47
TX3 8G 11
D28A
MMADI2-
1
2
M04 8F
3 MARI2S
B41
TX3 7H 12
D24A
MMADØ5-
4
5
M04 8D
6 MARØ5S
B45
TX3 7H 10
D22A
MMADI3-
4
5
M04 8F
6 MARI3S
B39
TX3 8H 13
D32A
MMADØ6-
10
9
M04 8D
8 MARØ6S
B61
TX3 8H 8
D26A
MMADI4-
10
9
M04 8F
8 MARI4S
B67
TX3 8H 12
D33A
MMADØ7-
13
12
M04 8D
11 MARØ7S
B59
TX3 8G 12
D27A
MMADI5-
13
12
M04 8F
11 MARI5S
B65
TX3 8G 8
D31A
MMADØ8-
1
2
M04 8E
3 MARØ8S
B46
SHT 6
CCFCLK-
DMADEN
1
2
4
5
M26 3B
6
DWG NO 394577 SHEET 12 OF
DWG NO 394577 SHEET 12 OF
CODE IDENT NO. 49956
SIZE D
394577
REV A
SCALE NONE
SHEET 12
RAYTHEON COMPUTER FORM 67-1


P/O MEMORY PARITY CHECK LOGIC
DWG. NO. 394577 SHEET 13 OF
6B
M74
SHT8 MCDI00 13
SHT8 MCDI01 1
SHT8 MCDI02 2
SHT8 MCDI03 3
SHT9 MCDI04 9
SHT9 MCDI05 10
SHT9 MCDI06 11
SHT9 MCDI07 12
8 MCDIPLI
4
6 LBPE- SHT14
5 LBP SHT14
9
10
M00
5B
SHT14 GLBP- 9
SHT14 LBP- 10
M04
6A
8
TX3
6H
10
SHT14 GLBP 12
8 MCDIPLI- 13
11
MCDIPL
B30
4B
M74
SHT10 MCDI08 13
SHT10 MCDI09 1
SHT10 MCDI10 2
SHT10 MCDI11 3
SHT11 MCDI12 9
SHT11 MCDI13 10
SHT11 MCDI14 11
SHT11 MCDI15 12
8 MCDIPRI
4
6 RBPE- SHT14
5 RBP SHT14
4
5
M00
5B
SHT14 GRBP- 1
SHT14 RBP- 2
M04
6A
3
TX3
5H
10
SHT14 GRBP 4
6 MCDIPRI- 5
6
MCDIPR
B15
DWG NO. 394577 SHEET 13 OF
CODE IDENT NO. 49956
SIZE D
394577
REV A
SCALE NONE
SHEET 13
RAYTHEON COMPU. FR FORM 67-0085


P/O PARITY CHECK LOGIC
SHT 13 LBPE-
SHT 13 RBPE-
M00 5B
SHT 6 MCRW-
M00 3A
MCRW
SHT 14 GLBP-
SHT 14 GRBP-
M26 3B
PARERS1
PAPERS2
TIRC2
SHT 6
SHT 6 KKCB
M51 5A
B5 SCDC1FØ
B3 SCDCØ
A66 CCFSYN1
A68 MRESET-
PARER
PARER-
B7
A69
SHT 6 ACDLY
M04 2H
SHT 6 ACDLY-
ACDLYD-
M05 3F
STBINH
M00 2A
STBINH-
A69
R3 4.7K 1/4W
C1 120 PF
+5V
SHT 14 TIRC1
A35 MCDOPL
M00 3A
LBPDS
R1 1K 1/4W, 5%
-5V
M61 4A
LBP
LBP-
SHT 13
A37 MCDOPR
RBPDS
R2 1K 1/4W, 5%
RBP
RBP-
SHT 7 TIRCØ
DTØ-
SHT 6 ACDLY-
B53 MBLDADLB
M00 8A
GLBPS-1
SHT 6 ACDLY
SHT 7 DWRTEN
GPSA-
M05 8B
GLBPS
M60 7A
GLBP
GLBP-
SHT 13,14
B55 MCWRENT-
GRBPS
GRBP
GRBP-
SHT 6 ACDLY-
B14 MBLDADRB
GRBPS-
SHT 7,14
A17 TIRC1
SHT 6 KKC
M00 1A
GPK
DWG. NO. 394577
SHEET 14 OF
CODE IDENT NO. 49956
SIZE D
394577
REV B
SCALE NONE
SHEET 14
RAYTHEON COMPUTER FORM 67-0085

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	394577	B
SCALE 1.0VE		SHEET 15	

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER EO 20727		⌐	MSF	MB	[illegible]	7/15/70
X2	REVISED PER EO. 20743		⌐	MSF	MB	MB	8/11/70
A	RELEASED PER EO 19311		⌐	MSF	MB	MB	11/14/70

SHEET 1 OF 12

DWG. NO. 394582

TABLE OF CONTENTS

GLOSSARY

CPSWRST	RESET SWITCH SIGNAL
INTRPTXX	INTERRUPT SIGNAL XX
ITØXRQ	INTERRUPT REQUEST SIGNAL X
ITISAXX	INTERRUPT INHIBIT SIGNAL XX
ITACTA	PLACE REQUESTING INTERRUPT LEVEL INTO ACTIVE STATE
ITDSBA	DISABLE ADDRESSED INTERRUPT LEVEL
ITENBA	ENABLE ADDRESSED INTERRUPT LEVEL
ITIDLA	RETURN ADDRESS INTERRUPT LEVEL TO IDLE STATE.
ITLVDCXX	DECODE INTERRUPT LEVEL ADDRESS XX
ITMBRIZ	MEMORY BUFFER SLIP SHOT REPOWERED
ITQXXYY	INTERRUPT REQUEST SIGNAL XXXX
IXRØXA	INTERRUPT ACTIVE REGISTER FLIP-FLOP X
IXRØXN	INTERRUPT ENABLE REGISTER FLIP FLOP X
ITRSVYY	INTERRUPT SERVICE REGISTER BIT XX
ITSVENB	ENABLE INTERRUPT SERVICE
ITWAIT	INTERRUPT WAITING SIGNAL
KKCY	CLOCK
MBRYX	MEMORY BUFFER REGISTER FLIP-FLOP XX
TIRCØ	TØ TIME INTERVAL

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
DEC	531667-001
M00	531593-006
M01	531593-005
M02	531593-007
M03	531593-008
M05	531593-004
M06	531593-017
M10	531593-002
M26	531593-012
M60A	531593-018
M61	531593-011
TX2	531596-001
TX3	531596-002

SHEET	1	2	3	4	5	6	7	8	9	10	11	12						
REVISION	A	A	A	A	A	A	A	A	A	A	A	A						

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON:
DECIMALS XX ±.03, XXX ±.000; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015MAX
FINISH:

DRAWN	M. Frank	4-3-70
CHECK	M. Gagnon	11/4/70
APPR	[illegible]	11/17/70
APPR		

NEXT ASSY: N/A

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

PRIORITY INTERRUPT CARD, 01-07 (LOGIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE | 394582

SCALE NONE | SHEET 1 OF 12

RAYTHEON COMPUTER FORM 67-000-

2. JUMPERS: SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION: SHOWN BY DASHED LINES ARE OPTIONS

1. ⇉ DENOTES FRONT PANEL CONNECTOR
→ DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

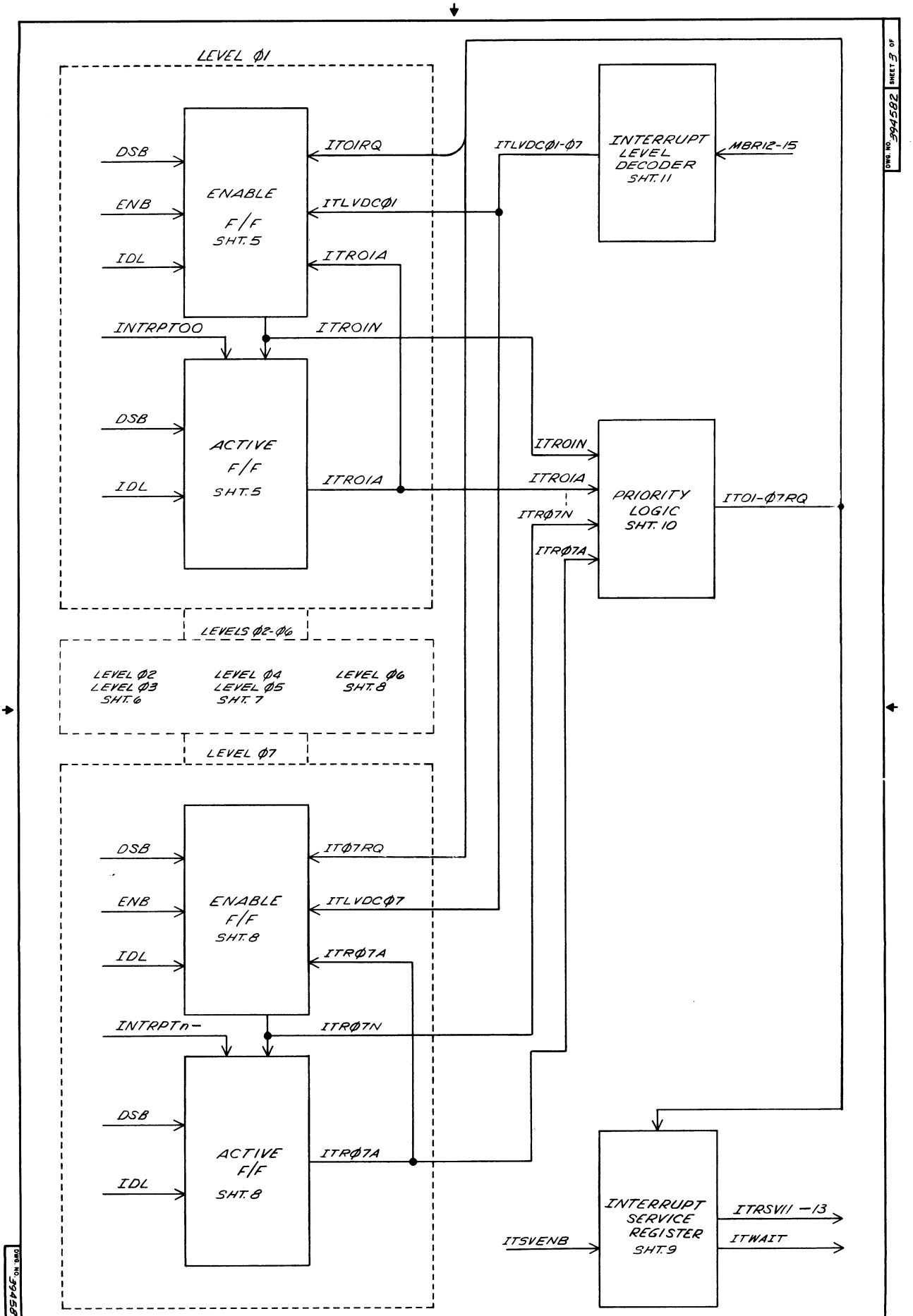
DWG. NO. 394582 SHEET 1 OF 12

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
CPSWRST-		A7,A8	9
INTRPTØ1-		A17	5
INTRPTØ2-		A29	6
INTRPTØ3-		A25	6
INTRPTØ4-		B39	7
INTRPTØ5-		B43	7
INTRPTØ6-		B55	8
INTRPTO7-		B51	8
INTRPTØ8-		A11,A14	4
INTRPTØ9-		A15,A18	4
INTRPT1Ø-		A27,A30	4
INTRPT11-		A23,A26	4
INTRPT12-		B37,B40	4
INTRPT13-		B41,B44	4
INTRPT14-		B53,B56	4
INTRPT15-		B49,B52	4
INTRPTXX-		A13	5
ITØ26AE	S	B61	9
ITØ8RQ-		B12	9
IT15AØ1-	S	A5	1Ø
IT15AØ8-		B22	1Ø
IT15AXX-	S	B21	1Ø
ITACT-		A49,A50	4
ITDSB		A51,A52	4
ITENB		B19,B20	4
ITIDL		B17,B18	4
ITMBR12	S	A44	11
ITQ159D-	S	A63	9
ITQ37BF-	S	A65	9
ITQA567-	S	B7	9
ITQ48C-	S	B9	9
ITQ9D-		A64	9
ITQAE-		A62	9
ITQBF-		A66	9
ITQC-		B1Ø	9
ITQCDEF-		B8	9
ITRSV1Ø-		A55,A58	4
ITRSV11-	S	A59	9
ITRSV12-	S	B15	9
ITRSV13-	S	B13	9
ITSVENB		A45,A46	9
ITWAIT-	S	B5	9
ITXXRQ-	S	B11	1Ø
KKCI		A53,A54	4
MBR12-		A43	11
MBR13-		B3,B4	11
MBR14-		A67,A68	11
MBR15-		A69,A70	11
TIRCØ		A47,A48	4

CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE			SHEET 2

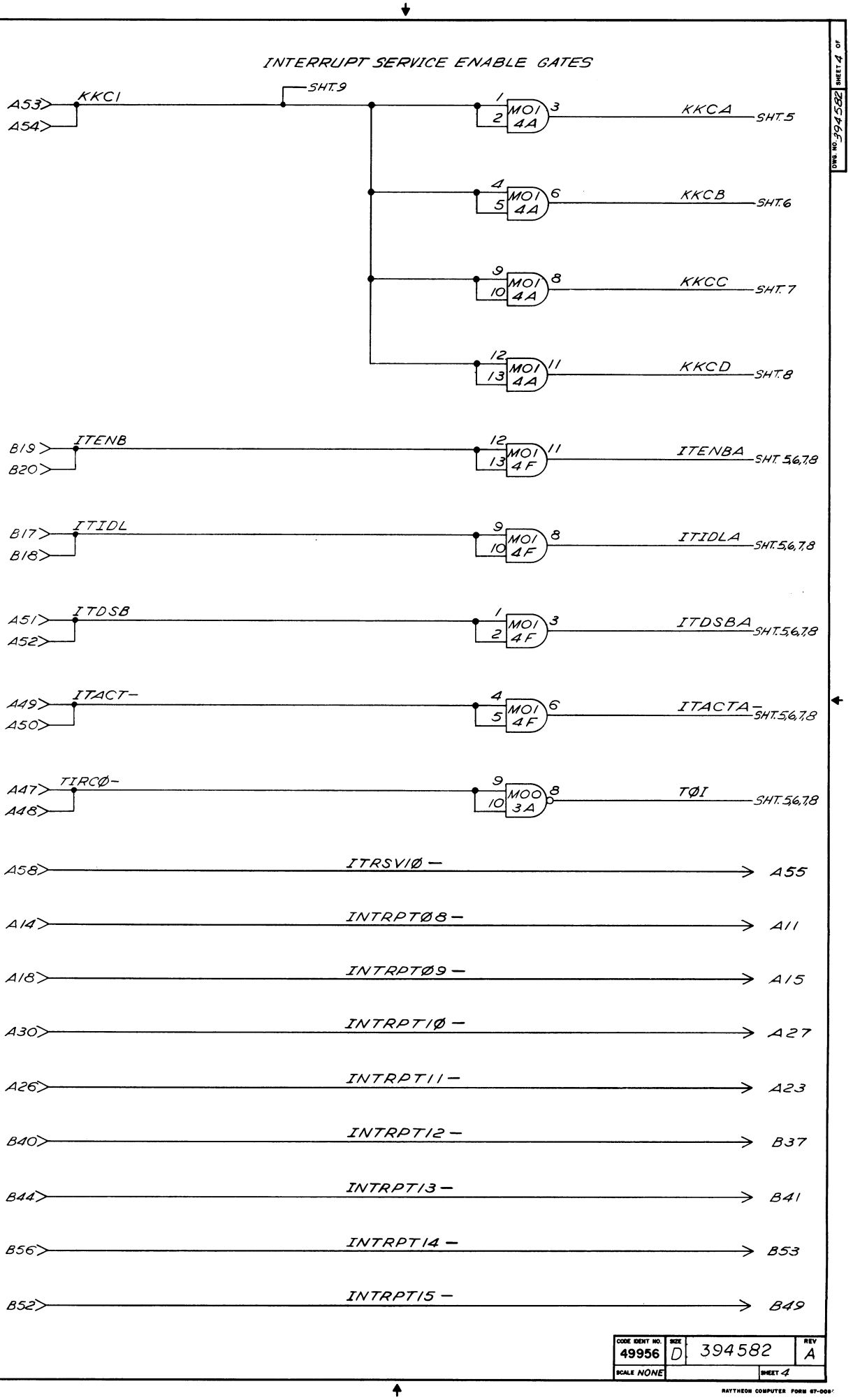
RAYTHEON COMPUTER FORM 67-0085

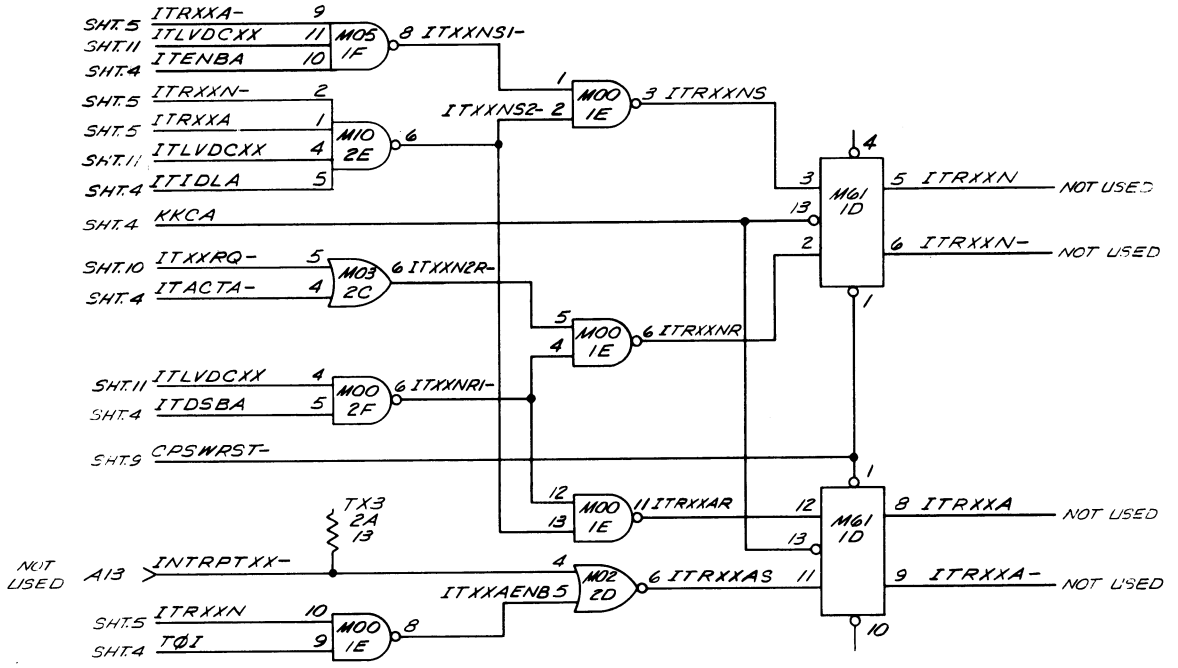


BLOCK DIAGRAM

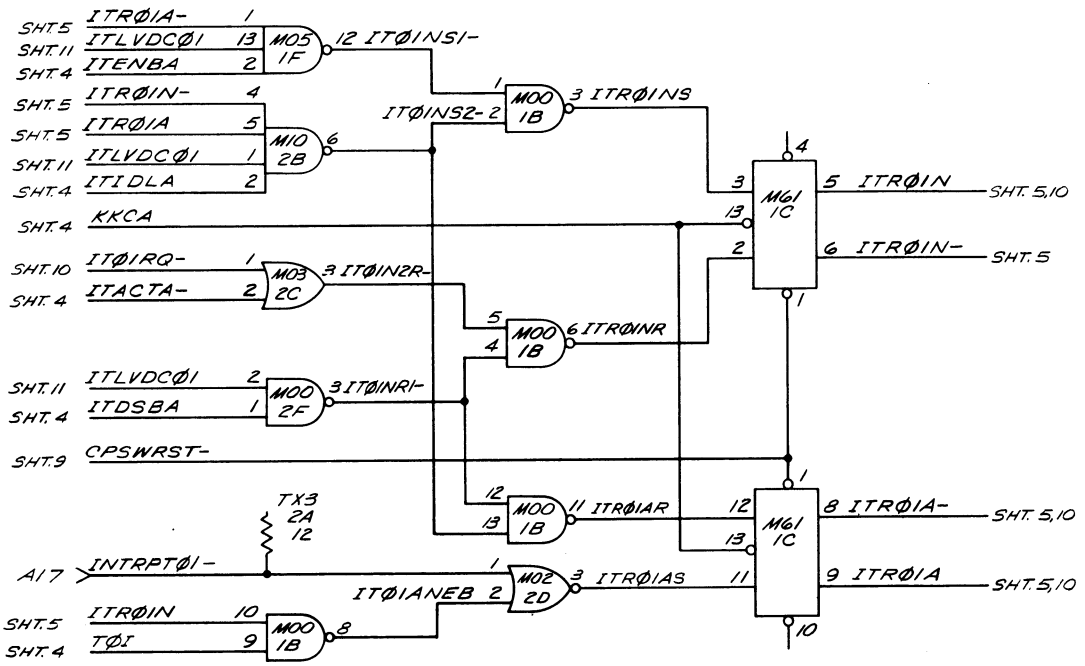
CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE		SHEET 3	

RAYTHEON COMPUTER FORM 67-0087


INTERRUPT SERVICE ENABLE GATES
A53
A54
KKCI
SHT.9
1
2
MOI 4A
3
KKCA
SHT.5
4
5
MOI 4A
6
KKCB
SHT.6
9
10
MOI 4A
8
KKCC
SHT.7
12
13
MOI 4A
11
KKCD
SHT.8
B19
B20
ITENB
12
13
MOI 4F
11
ITENBA
SHT.5,6,7,8
B17
B18
ITIDL
9
10
MOI 4F
8
ITIDLA
SHT.5,6,7,8
A51
A52
ITDSB
1
2
MOI 4F
3
ITDSBA
SHT.5,6,7,8
A49
A50
ITACT-
4
5
MOI 4F
6
ITACTA-
SHT.5,6,7,8
A47
A48
TIRCØ-
9
10
MOO 3A
8
TØI
SHT.5,6,7,8
A58
ITRSVIØ —
A55
A14
INTRPTØ8 —
A11
A18
INTRPTØ9 —
A15
A30
INTRPTIØ —
A27
A26
INTRPTII —
A23
B40
INTRPTI2 —
B37
B44
INTRPTI3 —
B41
B56
INTRPTI4 —
B53
B52
INTRPTI5 —
B49
SHEET 4 OF
DWG. NO. 394582
SHEET 4 OF
DWG. NO. 394582
CODE IDENT NO. 49956
SIZE D
394582
REV A
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0087



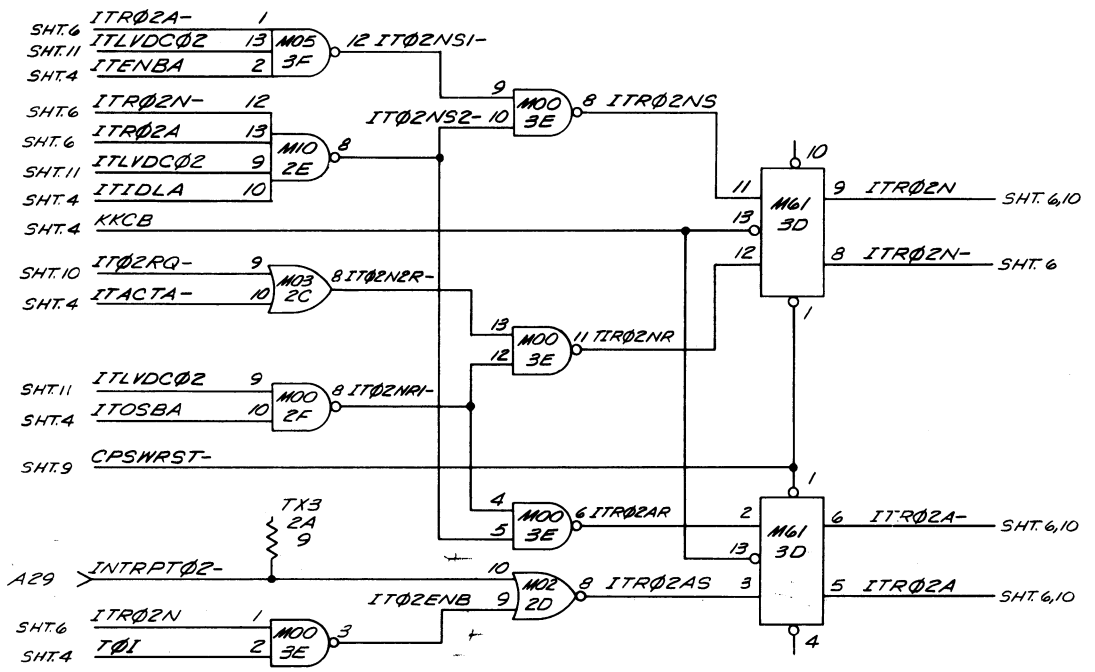
LEVEL Ø1 SERVICE FLIP-FLOPS



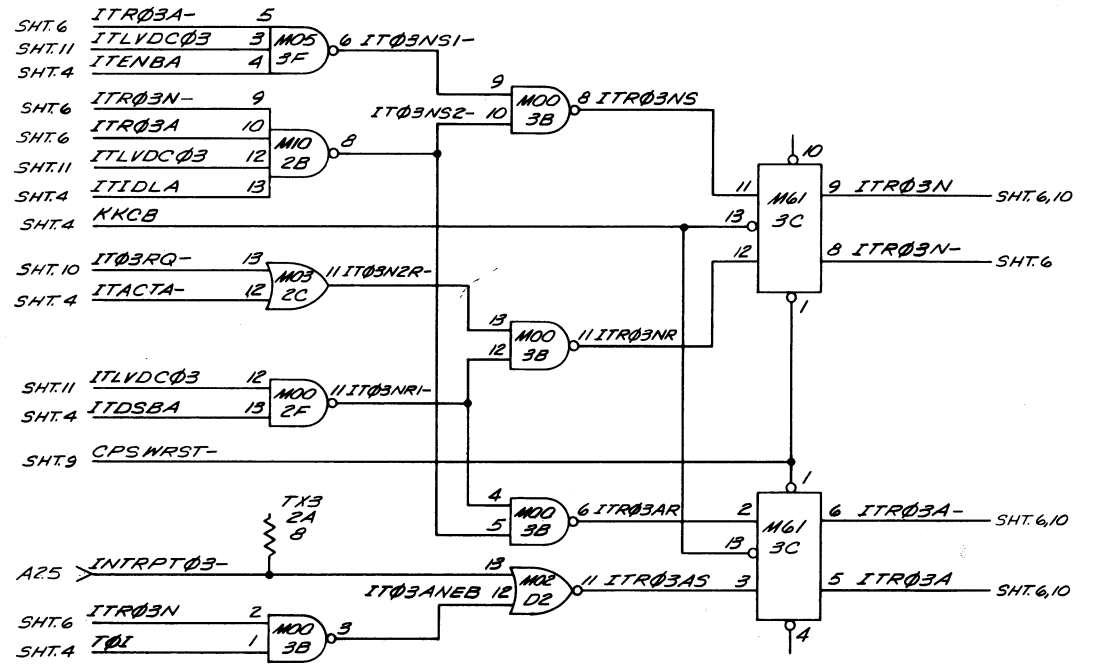
CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE			SHEET 5

RAYTHEON COMPUTER FORM 67-0001

LEVEL Ø2 SERVICE FLIP-FLOPS



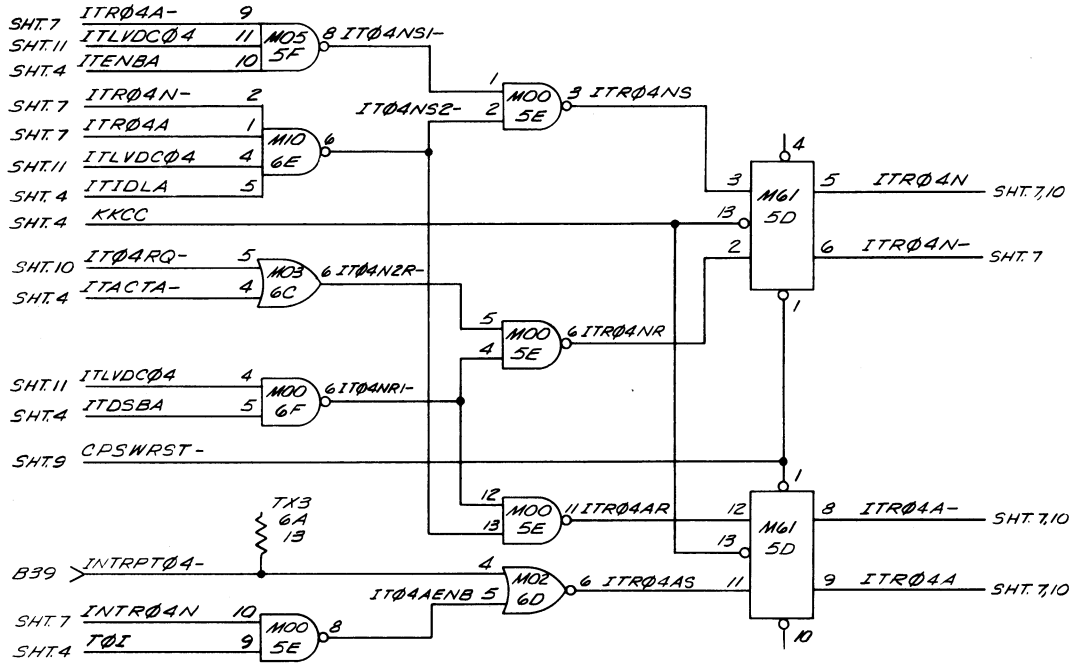
LEVEL Ø3 SERVICE FLIP-FLOPS



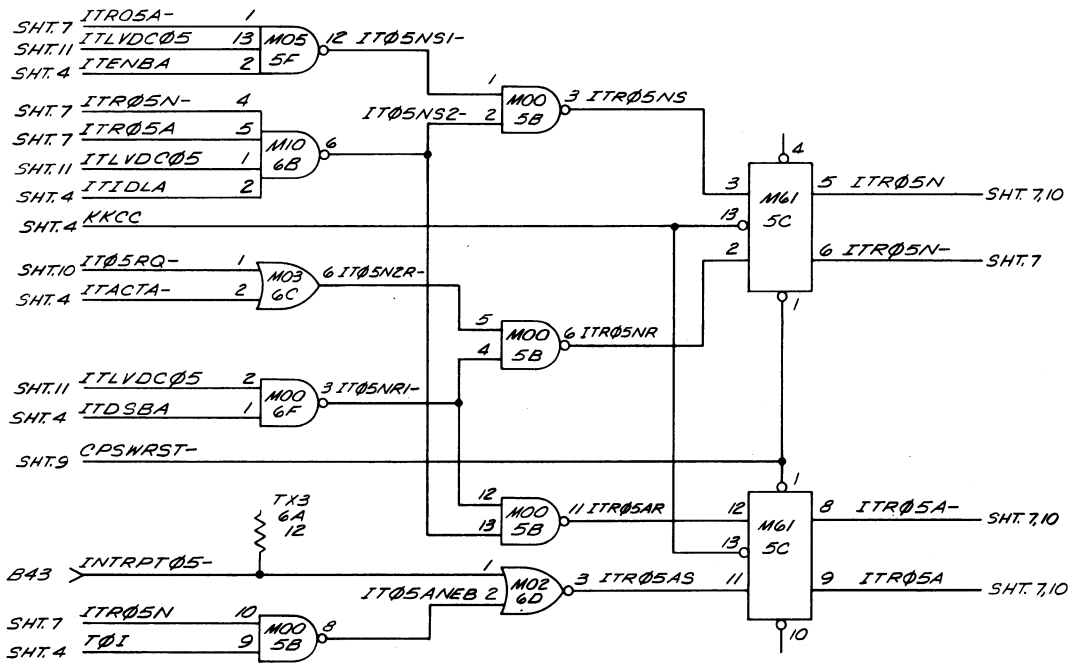
CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE		SHEET 6	

RAYTHEON COMPUTER FORM 07-0068

LEVEL Ø4 SERVICE FLIP-FLOPS



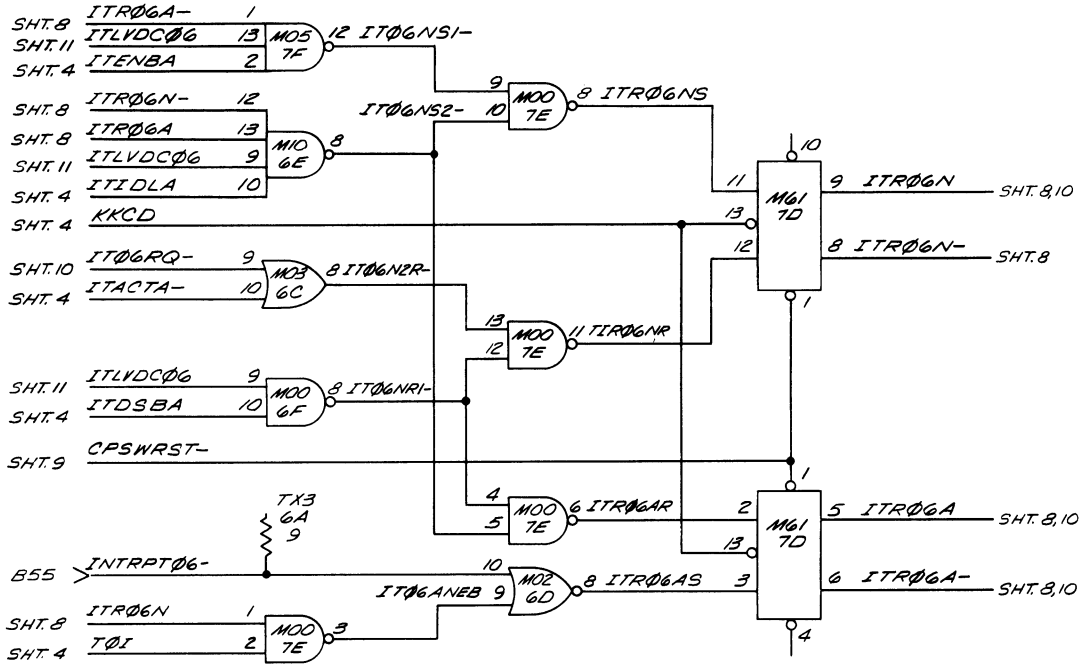
LEVEL Ø5 SERVICE FLIP-FLOPS



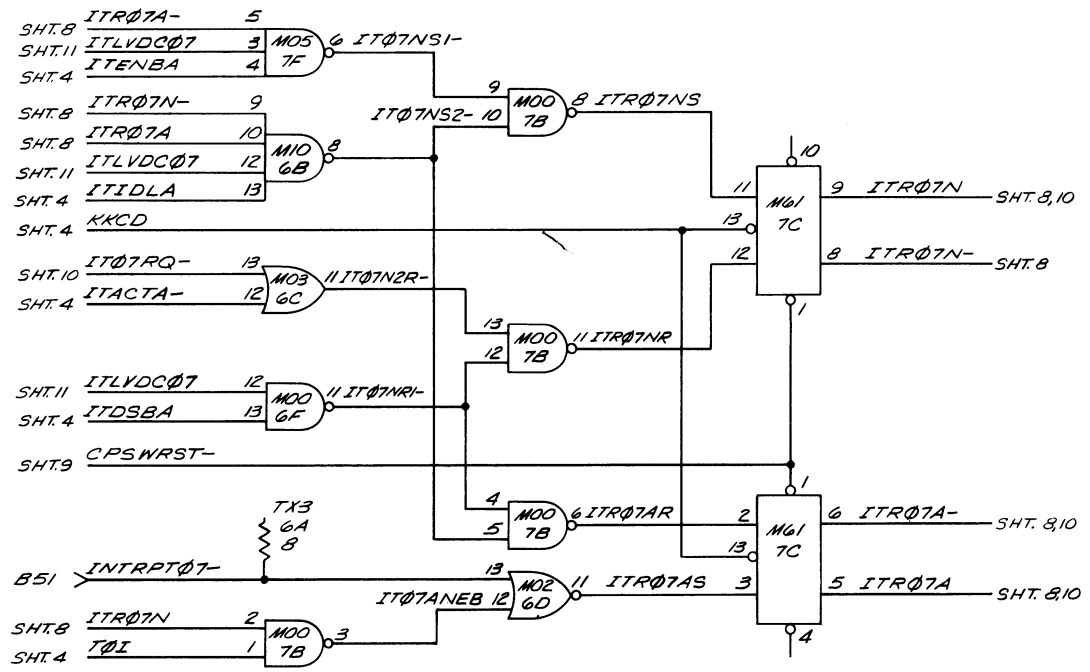
CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE			SHEET 7

RAYTHEON COMPUTER FORM 67-0008

LEVEL Ø6 SERVICE FLIP-FLOPS-



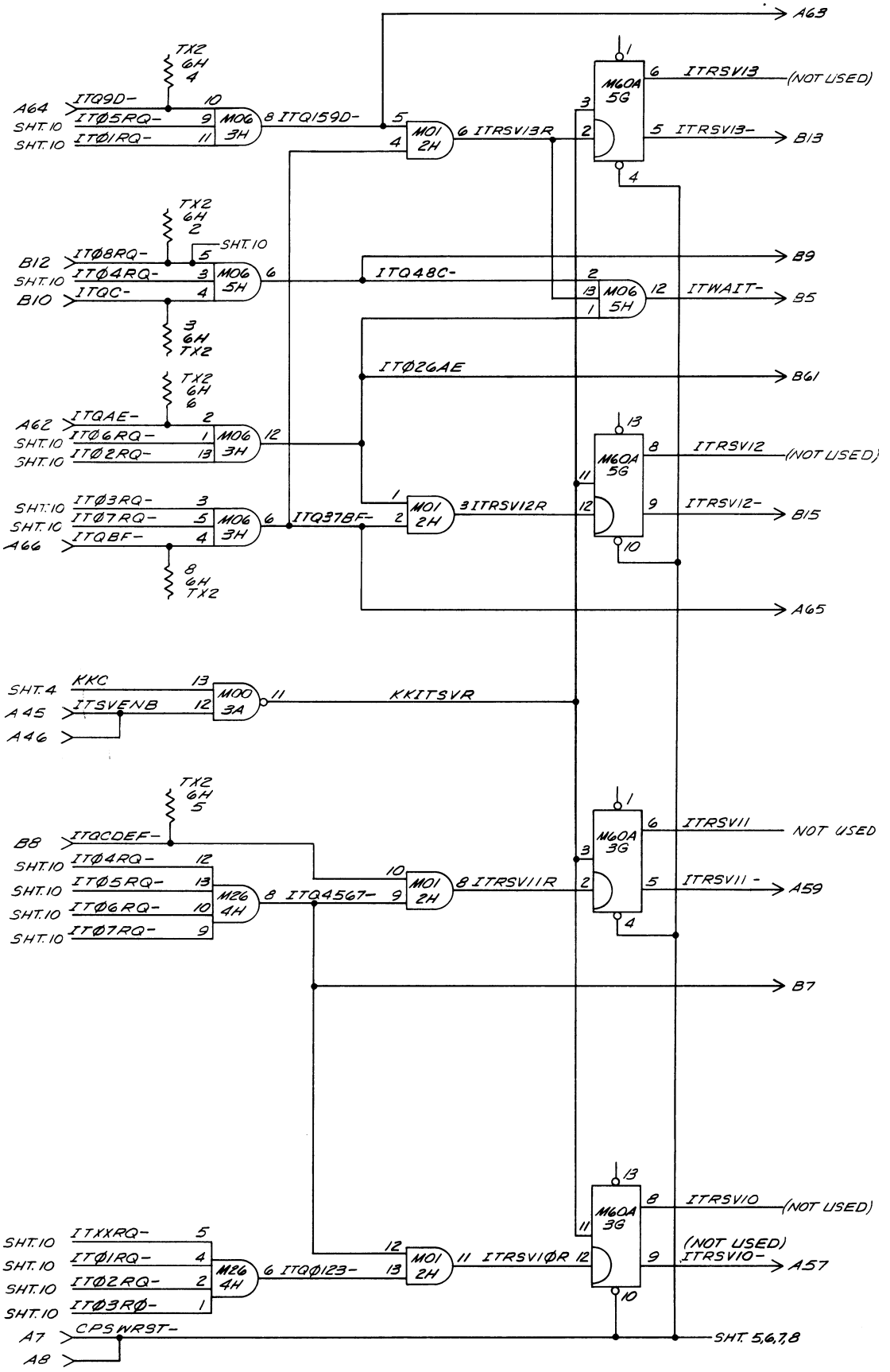
LEVEL Ø7 SERVICE FLIP-FLOPS



CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE		SHEET 8	

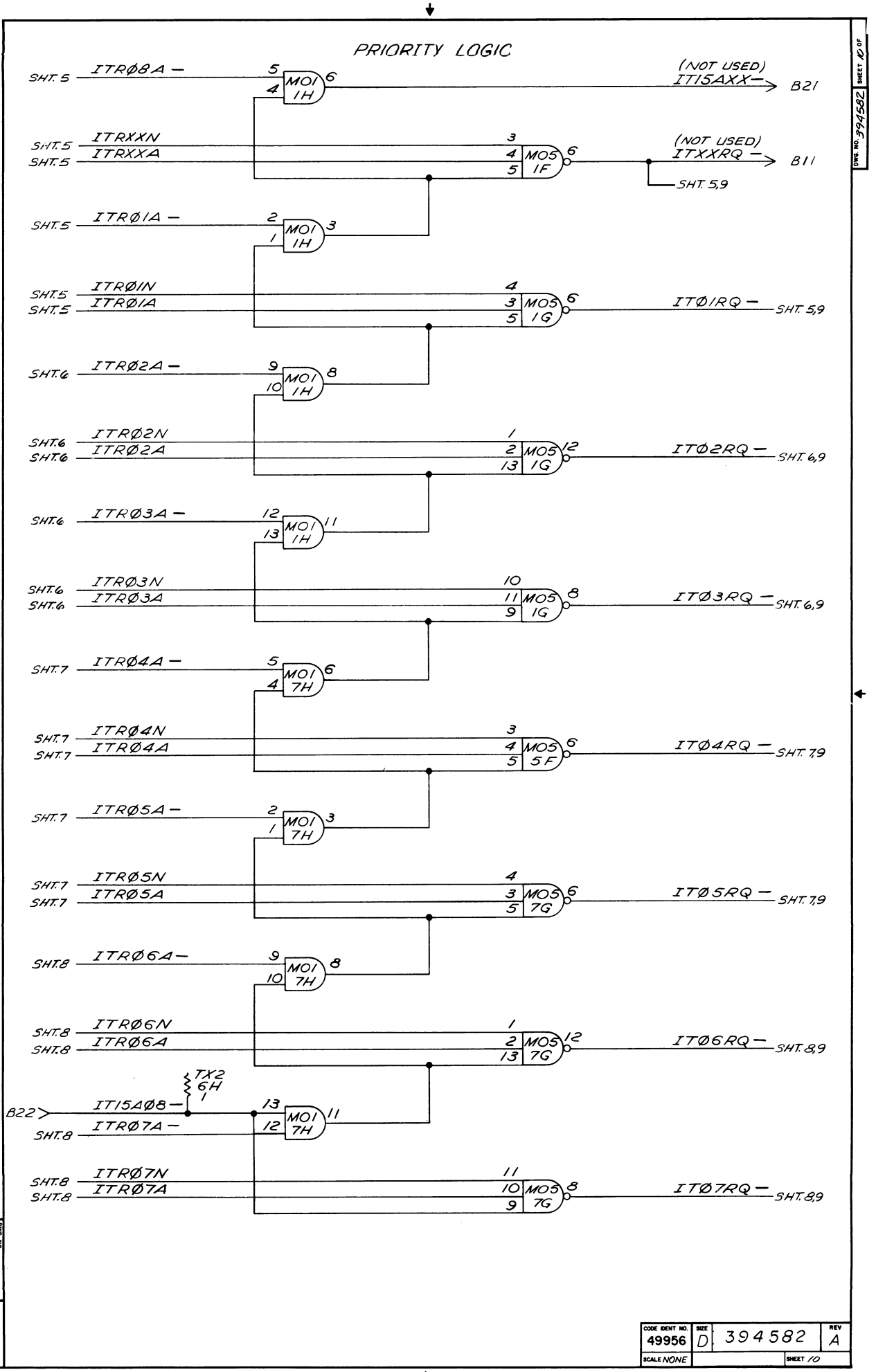
RAYTHEON COMPUTER FORM 67-0005

INTERRUPT SERVICE REGISTER

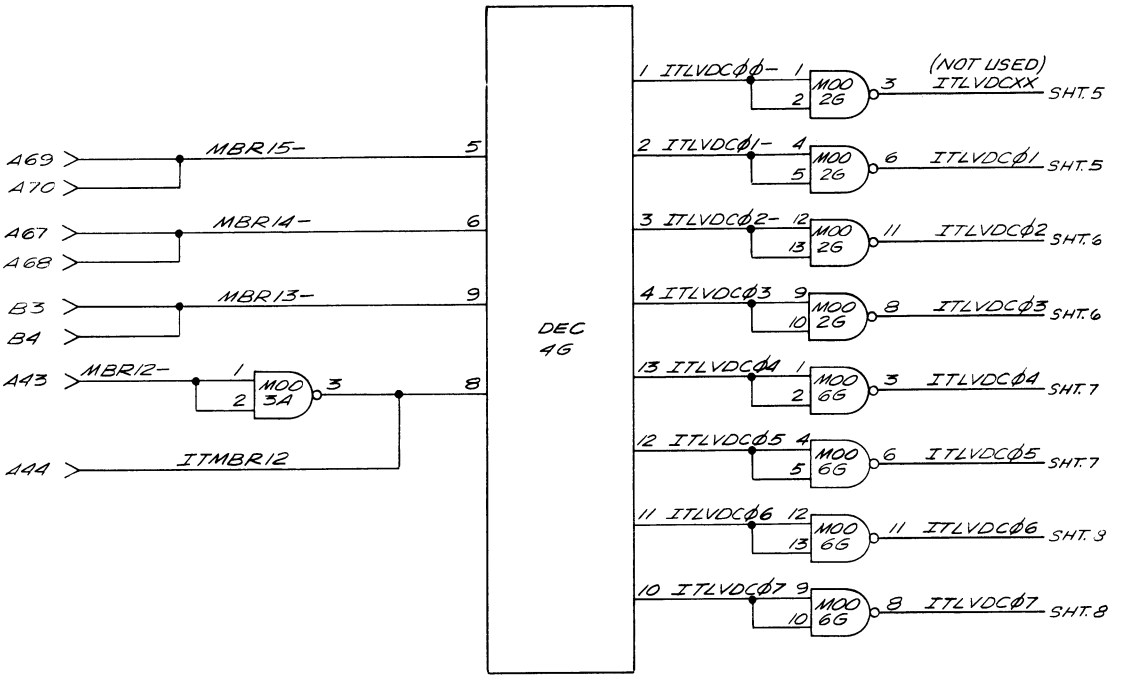


DWG. NO. 394582 SHEET 9 OF

CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE		SHEET 9	


PRIORITY LOGIC
SHT. 5
ITRØ8A –
5
4
M01
1H
6
(NOT USED)
IT15AXX–
B21
SHT. 5
SHT. 5
ITRXXN
ITRXXA
3
4
5
M05
1F
6
(NOT USED)
ITXXRQ –
B11
SHT. 5,9
SHT. 5
ITRØ1A –
2
1
M01
1H
3
SHT. 5
SHT. 5
ITRØ1N
ITRØ1A
4
3
5
M05
1G
6
ITØ1RQ –
SHT. 5,9
SHT. 6
ITRØ2A –
9
10
M01
1H
8
SHT. 6
SHT. 6
ITRØ2N
ITRØ2A
1
2
13
M05
1G
12
ITØ2RQ –
SHT. 6,9
SHT. 6
ITRØ3A –
12
13
M01
1H
11
SHT. 6
SHT. 6
ITRØ3N
ITRØ3A
10
11
9
M05
1G
8
ITØ3RQ –
SHT. 6,9
SHT. 7
ITRØ4A –
5
4
M01
7H
6
SHT. 7
SHT. 7
ITRØ4N
ITRØ4A
3
4
5
M05
5F
6
ITØ4RQ –
SHT. 7,9
SHT. 7
ITRØ5A –
2
1
M01
7H
3
SHT. 7
SHT. 7
ITRØ5N
ITRØ5A
4
3
5
M05
7G
6
ITØ5RQ –
SHT. 7,9
SHT. 8
ITRØ6A –
9
10
M01
7H
8
SHT. 8
SHT. 8
ITRØ6N
ITRØ6A
1
2
13
M05
7G
12
ITØ6RQ –
SHT. 8,9
TX2
6H
1
B22
IT15AØ8 –
SHT. 8
ITRØ7A –
13
12
M01
7H
11
SHT. 8
SHT. 8
ITRØ7N
ITRØ7A
11
10
9
M05
7G
8
ITØ7RQ –
SHT. 8,9
DWG. NO. 394582
SHEET 10 OF
DWG. NO. 394582
SHEET 10 OF
CODE IDENT NO. 49956
SIZE D
394582
REV A
SCALE NONE
SHEET 10
RAYTHEON COMPUTER FORM 67-0086

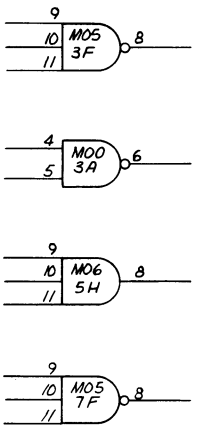
INTERRUPT LEVEL DECODER

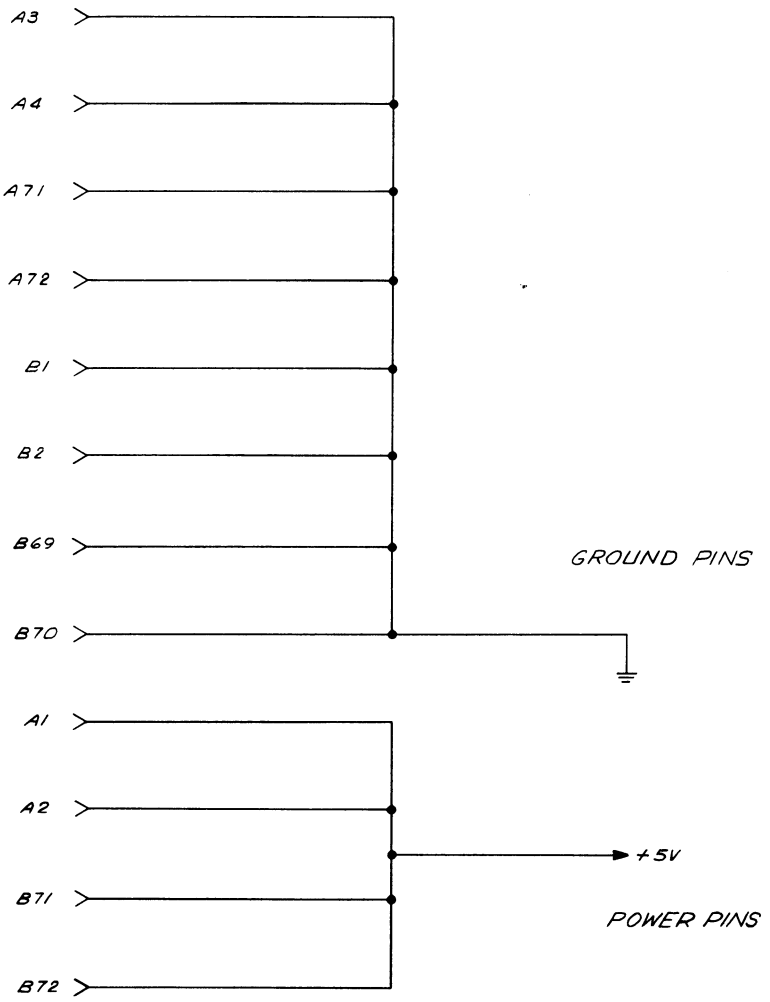


CODE IDENT NO.	SIZE		REV
49956	D	394582	A
SCALE NONE		SHEET 11	

RAYTHEON COMPUTER FORM 67-0085

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956		394582	A
SCALE NONE			SHEET 12

RAYTHEON COMPUTER FORM 67-0088

RESERVE E.O.'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
B	REVISED & REDRAWN 20457		L	JMF	HB	HB	9/70
C	REVISED PER EO. 20822		L	JMF	HB	HB	11/70
D	REVISED PER EO 19313			BCR	YB	YB	7/71

SHEET 1 OF 12

DWG NO. 394587

TABLE OF CONTENTS

GLOSSARY

KKTTF	CLOCK TTY CONTROLLER SEQUENCER FLAGS
TTADDC	TTY DEVICE ADDRESS CODE
TTARDL	ASSEMBLY REGISTER DATA LOAD
TTARDR	ASSEMBLY REGISTER DIRECT RESET
TTARLD	TTY ASSEMBLY REGISTER LOAD
TTAR0-TTAR8	ASSEMBLY REGISTER BIT 0-8
TTDC $\underline{K}$	TTY CONTROLLER SEQUENCER STATUS DECODE $\underline{K}$
TTDC $\underline{i}$ $\underline{j}$	TTY CONTROLLER SEQUENCER STATUS DECODE $\underline{i}$ OR $\underline{j}$
TTDC $\underline{i}$ $\underline{j}$ $\underline{K}$ $\underline{L}$	TTY CONTROLLER SEQUENCER STATUS DECODE $\underline{i}$ OR $\underline{j}$ OR $\underline{K}$ OR $\underline{L}$
TTFBNR	TTY CONTROLLER BINARY MODE
TTFDOW	TTY CONTROLLER DATA OUT WAIT
TTFIN	TTY CONTROLLER IN-MODE
TTFINT	TTY CONTROLLER INTERRUPT
TTFISF	TTY CONTROLLER DATA IN-SHIFT
TTFKEN	TTY CONTROLLER CLOCK ENABLE
TTFOUT	TTY CONTROLLER OUT-MODE
TTINOUT	TTY IN OR OUT MODE
TTKAR0-TTKAR4	TTY CONTROLLER CLOCK ASSEMBLY REGISTER BIT 0-4
TTKBR0-TTKBR9	TTY CONTROLLER CLOCK B REGISTER BIT 0-9
TTKRDR	TTY CONTROLLER CLOCK REGISTER DIRECT RESET
TTR0-TTR3	TTY CONTROLLER SEQUENCER REGISTER BIT 0-3
TTSAID	TTY SELECTED AS INPUT DEVICE
TTSAIOD	TTY SELECTED INPUT OR OUTPUT DEVICE
TTSAOD	TTY SELECTED AS OUTPUT DEVICE
TTSTIN	TTY STATUS IN
TTSTRQ	TTY STATUS REQUEST

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
D32	531143-001
D36	531274-001
D37	531531-001
D44	531145-001
D46	531147-001
D48	531231-001
D55	531535-001
D58	531522-001
D62	531148-001
M00	531593-006
M01	531593-005
M26	531593-012
M61	531593-011

6. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" CONNECTOR. C1 THRU C5, C20, C21, C22.
5. JUMPER PINS 1 AND 2, 5 AND 6 FOR OPTIONAL I.O.U. SEC. UNIT, (SHOWN)
4. OPTIONAL INTERRUPT LEVEL SHOWN AT LEVEL "I" AND IS USED WITH OPERATOR INTERRUPT OPTION ONLY.
3. INTERRUPT LEVEL SHOWN AT LEVEL "0," ONLY ONE LEVEL MAY BE SELECTED
2. **JUMPERS: SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS**
1. ⇒ **DENOTES FRONT PANEL CONNECTOR**
   → **DENOTES I/O CONNECTOR**

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11	12						
REVISION	D	D	D	C	C	D	D	C	C	C	D	D						

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
L TOLERANCES ON: DECIMALS .XX ± .05, .XXX ± .010; ANGLES ± 0° 30'
BREAK SHARP CORNERS .010 MAX
FINISH:

DRAWN	H. FOGEL	3-2-70
CHECK	H. BROTHERS	2/14/70
APPR	R. BARTZ	4/14/70
APPR	R. ALLEN	4/24/70

NEXT ASSY N/A

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

CONTROLLER, TELETYPE
(LOGIC DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	394587
SCALE NONE		SHEET 1 OF 12

RAYTHEON COMPUTER FORM 57-0084

DWG NO. 394587 SHEET 1 OF 12

SIGNAL LIST

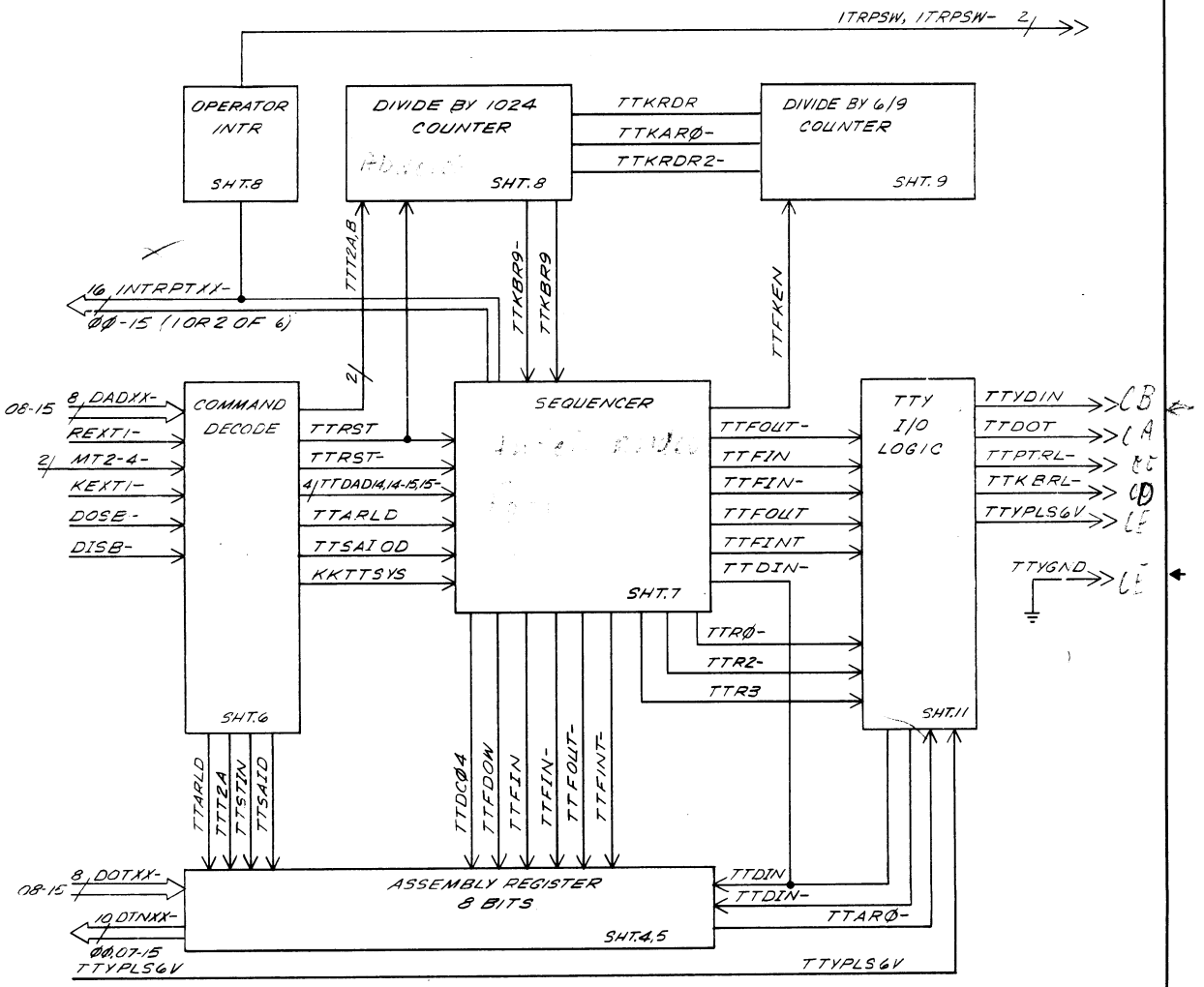
SIGNAL	SOURCE	CONN	SHEET
DAD08-		B37, B38	6
DAD09-		B39, B40	6
DAD10-		B41, B42	6
DAD11-		B51, B52	6
DAD12-		B63, B64	6
DAD13-		B61, B62	6
DAD14-		B59, B60	6
DAD15-		B57, B58	6
DIN00-	S	A35, A36	4
DIN07-	S	A21, A22	4
DIN08-	S	A19, A20	4
DIN09-	S	A17, A18	4
DIN10-	S	A15, A16	4
DIN11-	S	A13, A14	4
DIN12-	S	A11, A12	5
DIN13-	S	A09, A10	5
DIN14-	S	A07, A08	5
DIN15-	S	A05, A06	5
DISB-		B55, B56	6
DOSB-		B53, B54	6
DOT08-		A51, A52	4
DOT09-		A49, A50	4
DOT10-		A47, A48	4
DOT11-		A45, A46	4
DOT12-		A43, A44	5
DOT13-		A41, A42	5
DOT14-		A39, A40	5
DOT15-		A37, A38	5
INTRPT00-	S	B35, B36	7,8
INTRPT01-	S	B33, B34	7,8
INTRPT02-	S	B31, B32	7,8

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
INTRPT03-	S	B29, B30	7,8
INTRPT04-	S	B27, B28	7,8
INTRPT05-	S	B25, B26	7,8
INTRPT06-	S	B23, B24	7,8
INTRPT07-	S	B21, B22	7,8
INTRPT08-	S	B19, B20	7,8
INTRPT09-	S	B17, B18	7,8
INTRPT10-	S	B15, B16	7,8
INTRPT11-	S	B13, B14	7,8
INTRPT12-	S	B11, B12	7,8
INTRPT13-	S	B09, B10	7,8
INTRPT14-	S	B07, B08	7,8
INTRPT15-	S	B05, B06	7,8
ITRPSW		CX	8
ITRPSW-		CY	8
KEXT1-		B43, B44	6
MT0-		B49, B50	6
MT2-		B47, B48	6
MT4-		B45, B46	6
REXT1-		A69, A70	6
TTKBRL-	S	CD	11
TTPTRL-	S	CC	11
TTYDIN		CB	11
TTYGND		CE	11
TTYGND		C1	11
TTYGND		C2	11
TTYGND		C3	11
TTYGND		C4	11
TTYGND		C22	11
TTYPLSGV		CZ	11
TTYPLSGV	S	B67, B68	11

DWG. NO. 394587 SHEET 2 OF

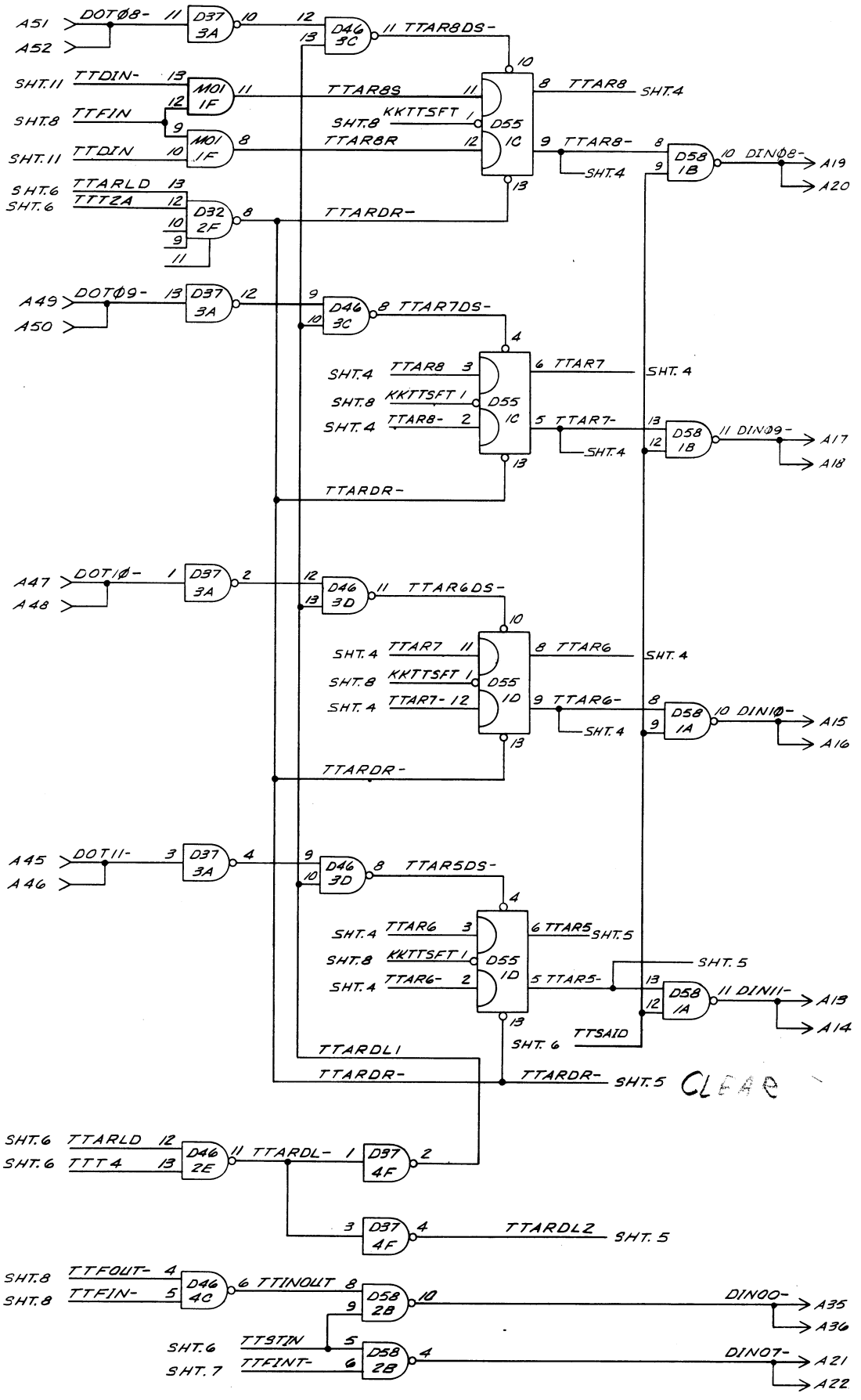
CODE IDENT NO.	SIZE		REV
49956	D	394587	D
SCALE NONE		SHEET 2	



BLOCK DIAGRAM

CODE IDENT NO.	SIZE		REV
49956	D	394587	D
SCALE NONE		SHEET 3	

RAYTHEON COMPUTER FORM 67-008F



ASSEMBLY REGISTER

CODE IDENT NO.	SIZE	DWG. NO.	REV
49956	D	394587	C
SCALE NONE		SHEET 4	

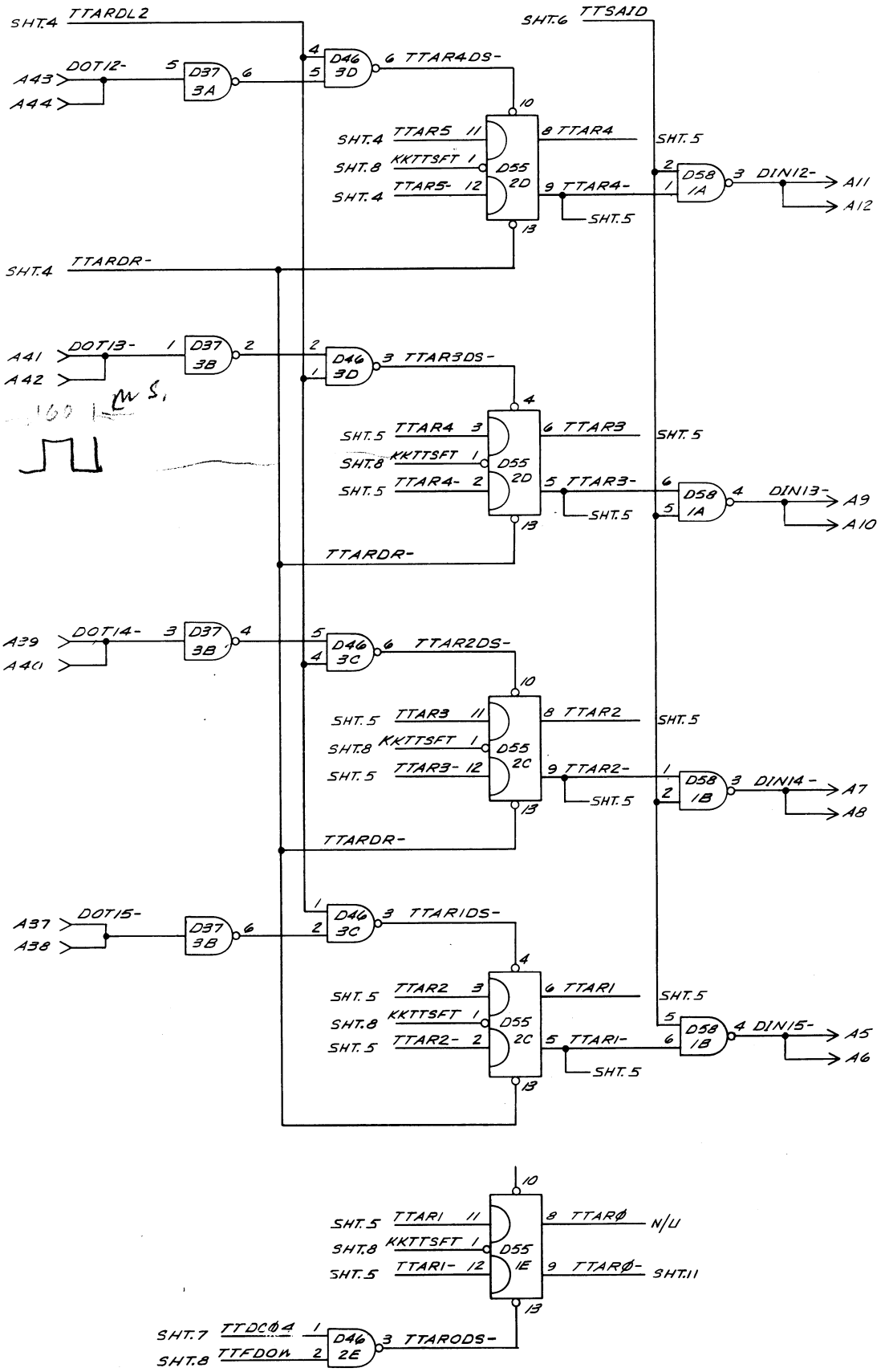
RAYTHEON COMPUTER FORM 6"-046

SHEET 4 OF

DWG. NO. 394587

SHEET 4 OF

DWG. NO. 394587

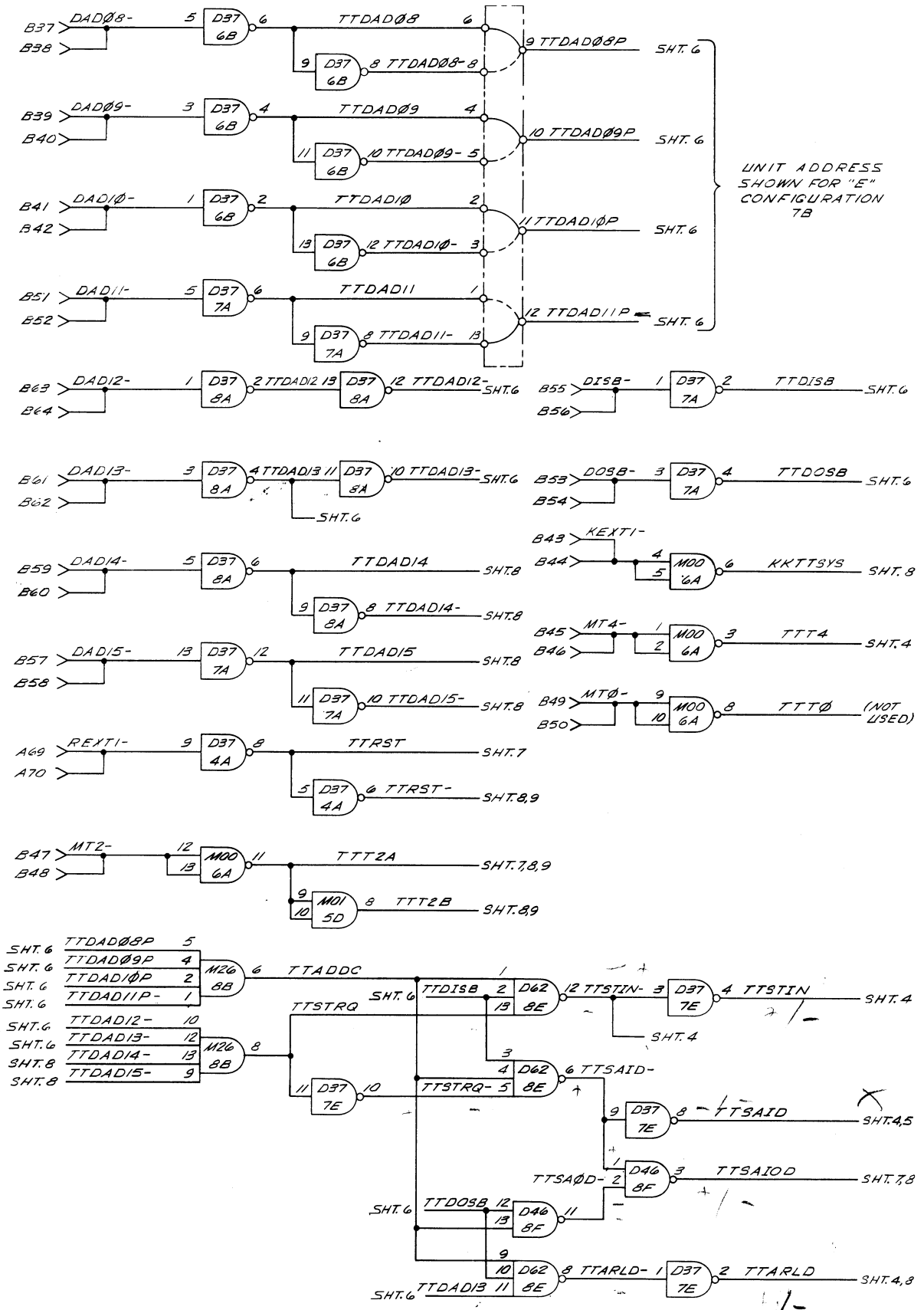


ASSEMBLY REGISTER

CODE IDENT NO.	SIZE		REV
49956	D	394587	C
SCALE NONE		SHEET 5	

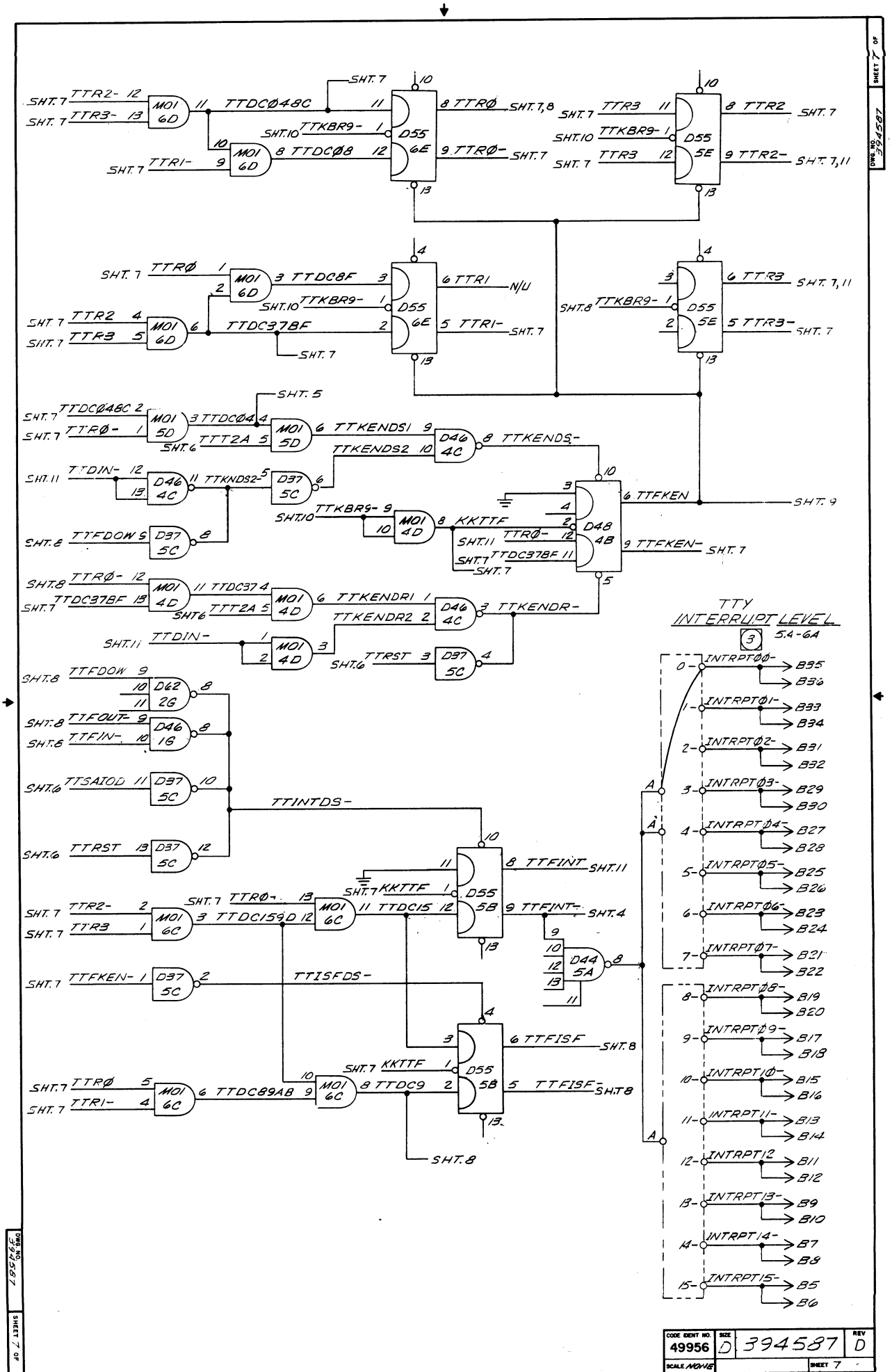
RAYTHEON COMPUTER FORM 07-0004

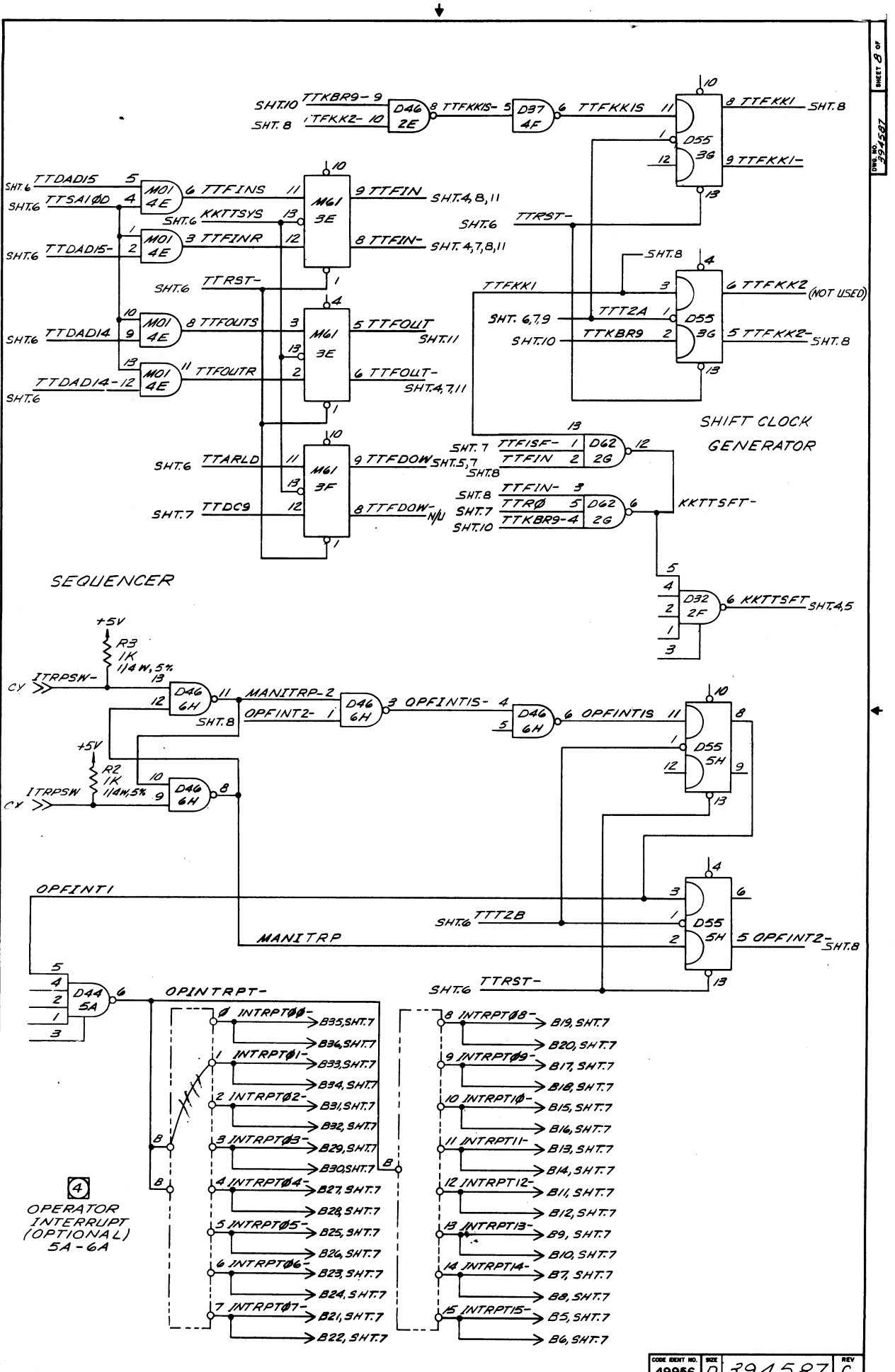
DWG. NO. 394587 SHEET 5 OF

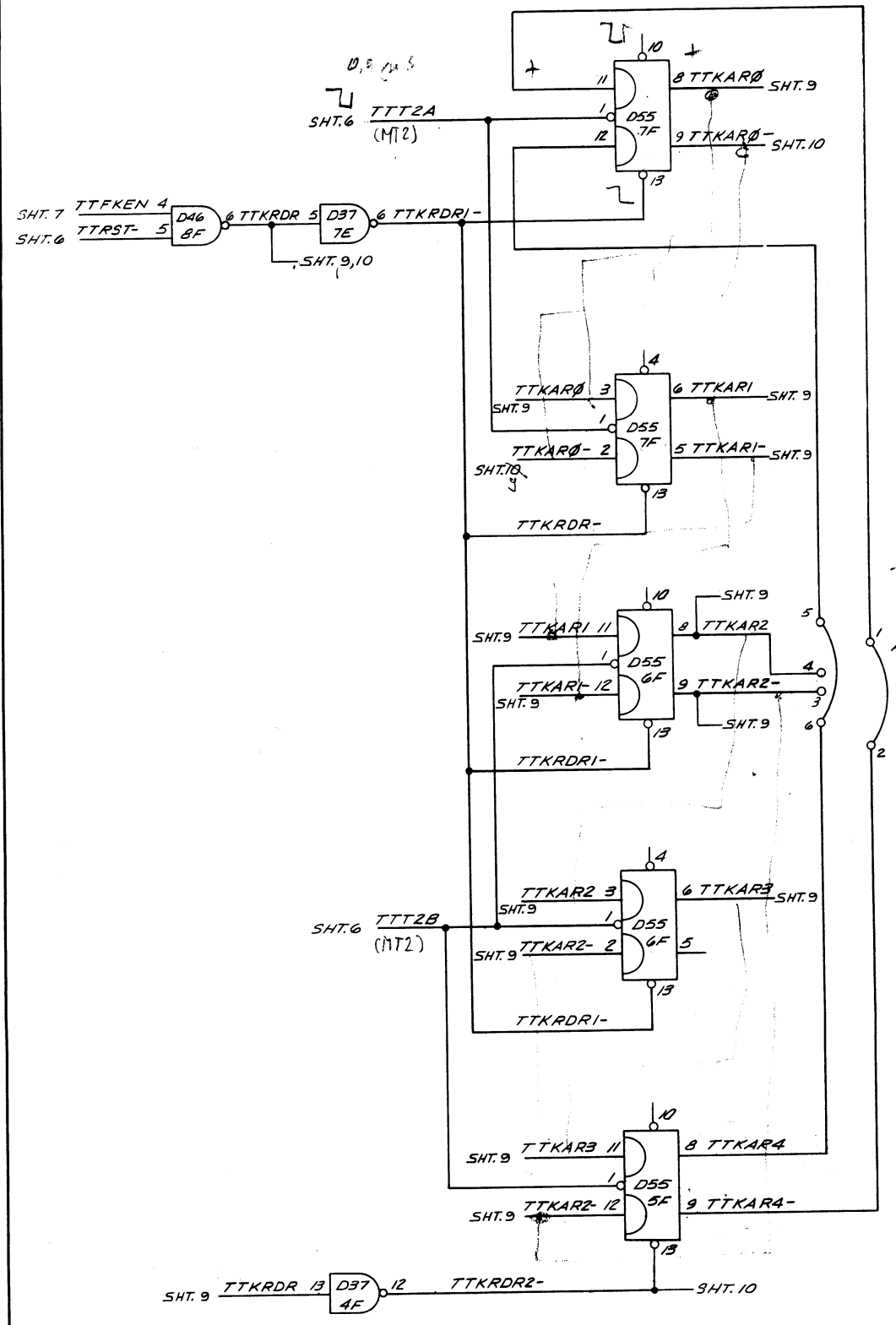


CODE IDENT NO.	SIZE		REV
49956	D	394587	D
SCALE NONE			SHEET 6

DWG. NO. 394587 SHEET 6 OF

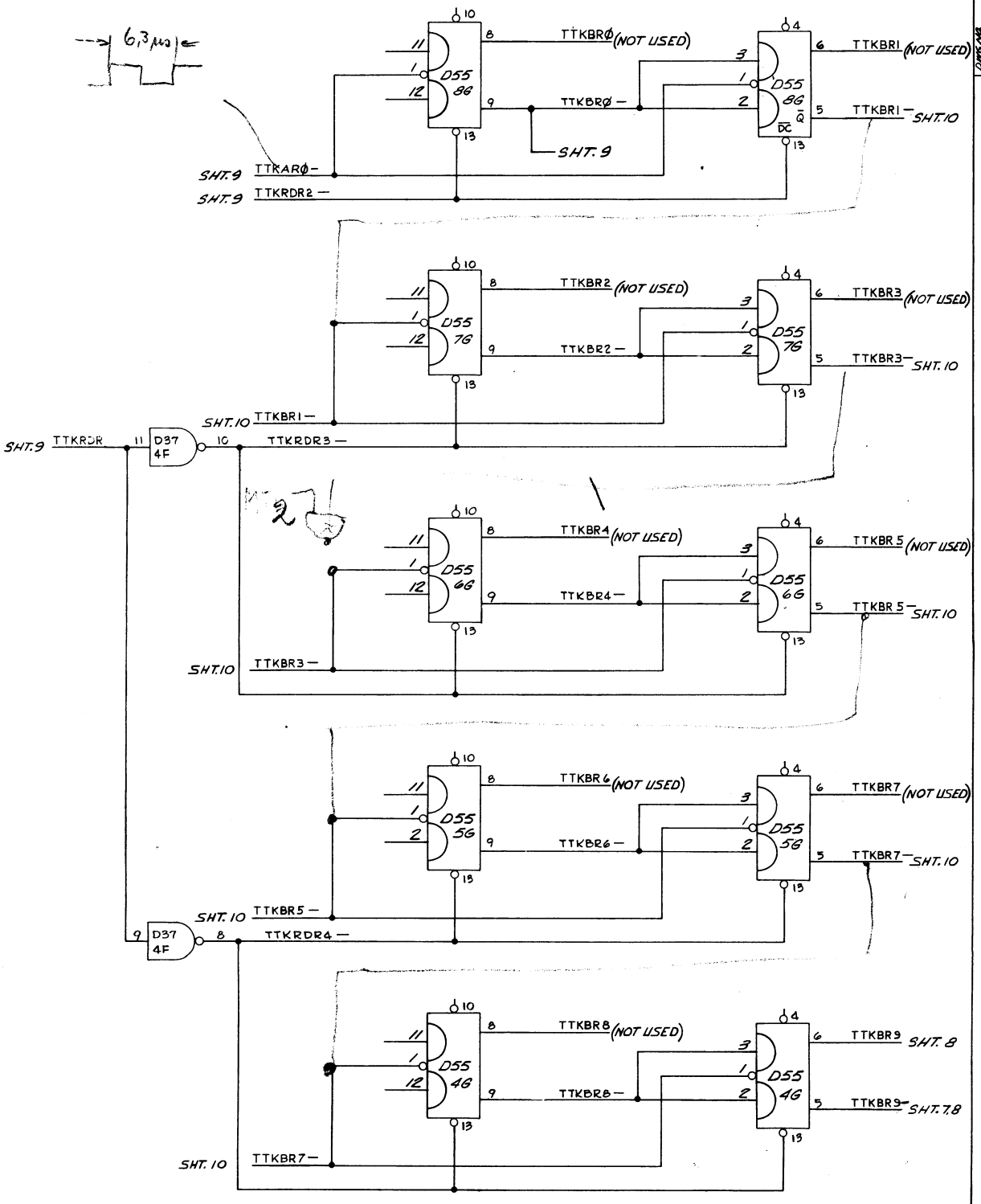

TTR2-
TTR3-
TTDCØ48C
TTKBR9-
TTDCØ8
TTRI-
TTRØ
TTR3
TTR2
TTR2
TTR3
TTDC8F
TTRI
N/U
TTDC37BF
TTRI-
TTDCØ48C
TTRØ-
TTDCØ4
TTT2A
TTKENDS1
TTKENDS2
TTKENDS-
TTDIN-
TTKNDS2-
TTFDOW
TTKBR9-
KKTTF
TTFKEN
TTFKEN-
TTDC37
TTDC37BF
TTKENDR1
TTKENDR2
TTKENDR-
TTRST
TTFOUT-
TTFIN-
TTSAIOD
TTINTDS-
TTFINT
TTFINT-
TTDC15
TTISFDS-
TTFISF
TTFISF-
TTDC89AB
TTDC9
SHT. 8
TTY
INTERRUPT LEVEL
3
5.4-6A
INTRPTØØ-
INTRPTØ1-
INTRPTØ2-
INTRPTØ3-
INTRPTØ4-
INTRPTØ5-
INTRPTØ6-
INTRPTØ7-
INTRPTØ8-
INTRPTØ9-
INTRPT1Ø-
INTRPT11-
INTRPT12
INTRPT13-
INTRPT14-
INTRPT15-
B35
B36
B33
B34
B31
B32
B29
B30
B27
B28
B25
B26
B23
B24
B21
B22
B19
B20
B17
B18
B15
B16
B13
B14
B11
B12
B9
B10
B7
B8
B5
B6


SHT.10 TTKBR9- 9
SHT. 8 TTFKKZ- 10
D46 2E
8 TTFKKIS- 5
D37 4F
6 TTFKKIS
D55 3G
8 TTFKKI SHT. 8
9 TTFKKI-
TTRST-
SHT.6
TTFKKI
TTT2A
TTKBR9
SHT. 6,7,9
SHT.10
6 TTFKKZ (NOT USED)
5 TTFKKZ- SHT. 8
SHIFT CLOCK GENERATOR
TTDADI5
TTSAIØD
TTDADI5-
KKTTSYS
TTFINS
TTFINR
M01 4E
M61 3E
9 TTFIN SHT.4, 8, 11
8 TTFIN- SHT. 4, 7, 8, 11
TTRST-
TTDADI4
TTDADI4-12
TTFOUTS
TTFOUTR
5 TTFOUT SHT.11
6 TTFOUT- SHT.4, 7, 11
TTARLD
TTDC9
9 TTFDOW SHT.5, 7
8 TTFDOW- N/U
TTFISF-
TTFIN
TTRØ
TTKBR9-4
D62 2G
KKTTSFT-
D32 2F
6 KKTTSFT SHT.4, 5
SEQUENCER
+5V
R3 1K 1/4 W, 5%
R2 1K 1/4W, 5%
ITRPSW-
ITRPSW
CY
D46 6H
MANITRP-2
OPFINT2-
OPFINTIS- 4
6 OPFINTIS
D55 5H
OPFINTI
MANITRP
TTT2B
5 OPFINT2- SHT.8
D44 5A
OPINTRPT-
Ø INTRPTØØ- B35, SHT.7
B34, SHT.7
1 INTRPTØ1- B33, SHT.7
B34, SHT.7
2 INTRPTØ2- B31, SHT.7
B32, SHT.7
3 INTRPTØ3- B29, SHT.7
B30, SHT.7
4 INTRPTØ4- B27, SHT.7
B28, SHT.7
5 INTRPTØ5- B25, SHT.7
B26, SHT.7
6 INTRPTØ6- B23, SHT.7
B24, SHT.7
7 INTRPTØ7- B21, SHT.7
B22, SHT.7
8 INTRPTØ8- B19, SHT.7
B20, SHT.7
9 INTRPTØ9- B17, SHT.7
B18, SHT.7
10 INTRPTIØ- B15, SHT.7
B16, SHT.7
11 INTRPTII- B13, SHT.7
B14, SHT.7
12 INTRPT12- B11, SHT.7
B12, SHT.7
13 INTRPT13- B9, SHT.7
B10, SHT.7
14 INTRPT14- B7, SHT.7
B8, SHT.7
15 INTRPTI5- B5, SHT.7
B6, SHT.7
4 OPERATOR INTERRUPT (OPTIONAL) 5A - 6A



DIVIDE BY 6/9 COUNTER

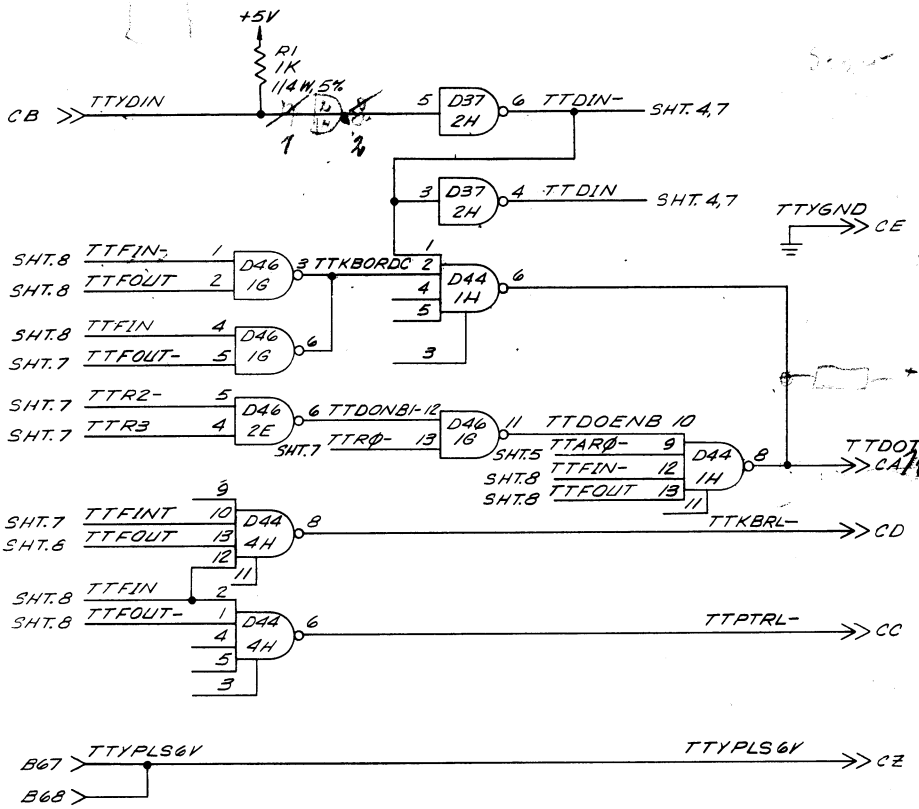
CODE IDENT NO.	SIZE		REV
49956	D	394587	C
SCALE NONE		SHEET 9	



DIVIDE BY 1024 RIPPLE COUNTER

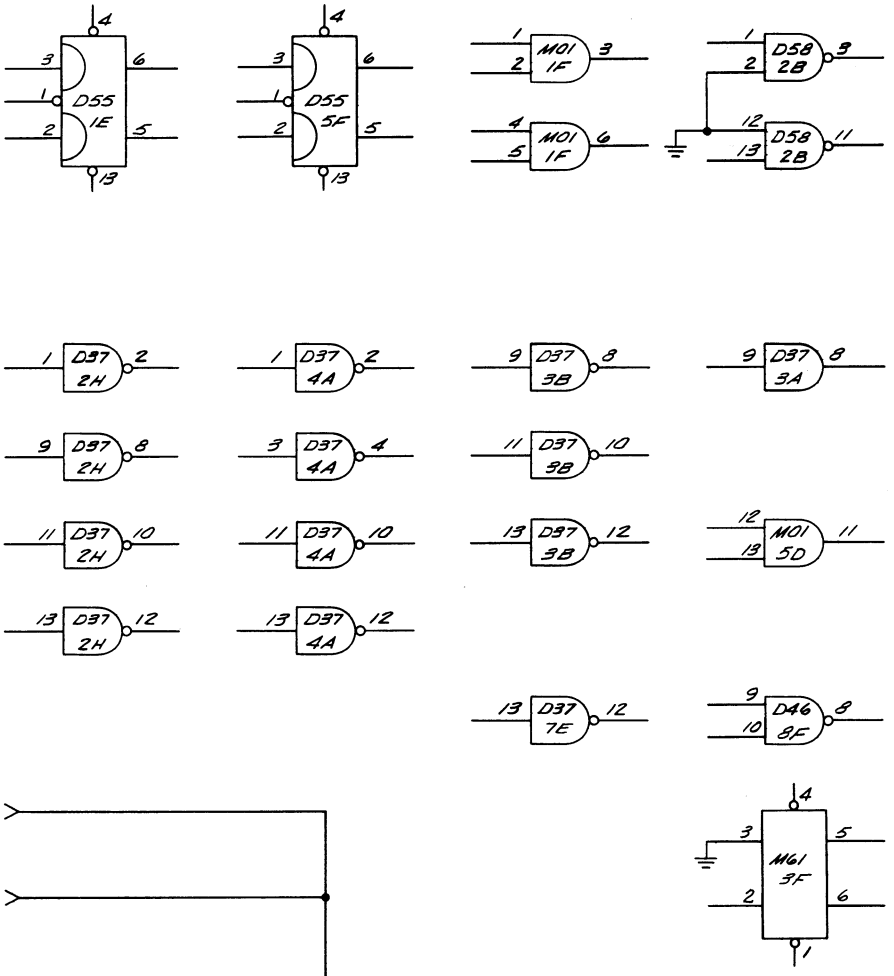
DWG. NO. 394587 SHEET 10

CODE IDENT NO.	SIZE		REVISIONS
49956	D	394587	C
SCALE NONE		SHEET 10	


+5V
R1
1K
1/4W 5%
CB
TTYDIN
D37 2H
TTDIN-
SHT. 4,7
TTDIN
TTYGND
CE
SHT. 8
TTFIN-
TTFOUT
D46 1G
TTKBORDC
D44 1H
SHT. 7
TTFOUT-
TTFIN
TTR2-
TTR3
D46 2E
TTDONBI-
TTRØ-
TTDOENB
TTARØ-
TTFIN-
TTFOUT
TTDOT
CA
TTFINT
D44 4H
TTKBRL-
CD
TTPTRL-
CC
B67
B68
TTYPLS6V
CZ

TTY I/O LOGIC

UNUSED I.C. PARTS



A3
A4
A71
A72
B1
B2
B69
B70

GROUND PINS

A1
A2
B71
B72

+5V

POWER PINS

DWG. NO. 394587 SHEET 12 OF
DWG. NO. 394587 SHEET 12 OF
CODE IDENT NO. 49956 | SIZE D | 394587 | REV D
SCALE NONE | SHEET 12
RAYTHEON COMPUTER FORM 67-0088

TO BE SUPPLIED WHEN AVAILABLE

POWER FAILSAFE AND
BOOTSTRAP CARD

394592

RESERVE EO'S OUTSTANDING	REVISIONS								
	SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	X1	APPROVAL PEP E.O 20470			MSF	MB	[illegible]	5/17/70
	X2	REVISED PER E.O. 20747			MSF	MB	MB	5/17/70
	A	RELEASED PER E.O. 19311			AP	MB	MB	5/17/70

SHEET 1 OF 11

DWG. NO. 545497

TABLE OF CONTENTS

GLOSSARY

ACØ1SRCD	ACCUMULATOR BIT ØØ LOAD FROM INDEX REGISTER BIT 15
ACCLKENBL	ACCUMULATOR LEFT BYTE CLOCK ENABLE
ACLDAL	ACCUMULATOR LOAD FROM THE ADDER
ACLLDI	ACCUMULATOR LOAD FROM DIRECT INPUT OUTPUT CHANNEL
ACLLOR	ACCUMULATOR LOAD FROM ADDER OR
ACLDXOR	ACCUMULATOR LOAD FROM ADDER EXCLUSIVE OR
ACRDR	ACCUMULATOR DIRECT RESET
ACRXX	ACCUMULATOR BIT XX
ACRXXS	ACCUMULATOR BIT XX SET TERM
ACRZERØØ	ACCUMULATOR BITS ØØ-Ø3 ARE ZERO
ACSLENB	ACCUMULATOR SHIFT LEFT ENABLE
AC3RENB	ACCUMULATOR SHIFT RIGHT ENABLE
ADAXX	ADDER GATE A BIT XX
ADBXX	ADDER GATE B BIT XX
ADZZEFCT	ADDER SUM BITS ØØ-Ø3 ARE ZERO
ADCXX	ADDER CARRY BIT XX
ADENAC	ADDER ENABLE FROM ACCUMULATOR
ADENACC	ADDER ENABLED FROM ACCUMULATOR COMPLEMENT
ADENACRB	ADDER ENABLED FROM ACCUMULATOR RIGHT BYTE
ADENEXB	ADDER ENABLE FROM EXTENSION REGISTER BYTE
ADENEXW	ADDER ENABLE FROM EXTENSION REGISTER WORD
ADENIX	ADDER ENABLED FROM INDEX REGISTER
ADENMBB	ADDER ENABLE FROM EXTENSION REGISTER
ADENMBC	ADDER ENABLE FROM MEMORY BUFFER COMPLEMENT
ADENMBL	ADDER ENABLE FROM MEMORY BUFFER LEFT BYTE
ADENPC	ADDER ENABLED FROM PROGRAM COUNTER
ADORXX	ADDER OR BIT XX
ADSUMXX	ADDER SUM BIT XX
ADXORXX	ADDER EXCLUSIVE OR BIT XX
CPSWDSAC	CONTROL PANEL SWITCH DISPLAY ACCUMULATOR
CPSWDSIX	CONTROL PANEL SWITCH DISPLAY INDEX REGISTER
CPSWPSMB	CONTROL PANEL SWITCH DISPLAY MEMORY BUFFER
CPSWXX	CONTROL PANEL DATA SWITCH BIT XX
DINXX	DIRECT INPUT CHANNEL BIT XX
DISPENEXX	CONTROL PANEL DATA SWITCH BIT XX INVERTED
DISPXX	CONTROL PANEL DISPLAY BIT XX
DOTXX	DIRECT OUTPUT CHANNEL BIT XX
EXRXX	EXTENSION REGISTER BIT XX
IXCLKENBL	INDEX REGISTER CLOCK ENABLE LEFT
IXLDADL	INDEX REGISTER LOAD FROM ADDER LEFT BYTE
IXLDPC	INDEX REGISTER LOAD FROM PROGRAM COUNTER
IXR15	INDEX REGISTER BIT 15
IXRDR	INDEX REGISTER DIRECT RESET
IXRXX	INDEX REGISTER BIT XX
IXRXXS	INDEX REGISTER BIT XX SET TERM
IXSL	INDEX REGISTER SHIFT LEFT
IXSR	INDEX REGISTER SHIFT RIGHT
IXSRAC15	INDEX REGISTER SHIFT RIGHT INPUT FROM ACCUMULATOR BIT 15
KKIA	GATED SYSTEM CLOCK
KKA	UNGATED SYSTEM CLOCK
MACLKEN	MEMORY ADDRESS REGISTER CLOCK ENABLE
MALDAD	MEMORY ADDRESS REGISTER LOAD FROM ADDER
MALDADSR	MEMORY ADDRESS REGISTER LOAD FROM ADDER SHIFTED RIGHT ONE BIT
MALDPC	MEMORY ADDRESS REGISTER LOAD FROM PROGRAM COUNTER
MARDRL	MEMORY ADDRESS REGISTER DIRECT RESET LEFT
MARXX	MEMORY ADDRESS REGISTER BIT XX
MARXXS	MEMORY ADDRESS REGISTER BIT XX SET TERM
MBLDADLB	MEMORY BUFFER LOAD FROM ADDER LEFT BYTE
MBLDMCLB	MEMORY BUFFER LOAD FROM MEMORY LEFT BYTE
MBRDR	MEMORY BUFFER REGISTER DIRECT RESET
MBRXX	MEMORY BUFFER REGISTER BIT XX
MCDIXX	MEMORY DATA INPUT BIT XX
MCDOXX	MEMORY DATA OUTPUT BIT XX
MCENMB	MEMORY DATA IN ENABLED FROM MEMORY BUFFER
PCLDAD	PROGRAM COUNTER LOAD FROM ADDER
PCRDR	PROGRAM COUNTER DIRECT RESET
PCRXX	PROGRAM COUNTER REGISTER BIT XX
PCRXXDS	PROGRAM COUNTER BIT XX DIRECT SET
PUARI	ARITHMETIC CARD UNUSED INPUT PULL UP

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
D37	531531-001
D46	531147-001
D58	531522-001
M00	531593-006
M01	531593-005
M04	531593-014
M07	531593-015
M26	531593-012
M27	531595-001
M60/M60A	531593-018
TX2	531596-001
TX3	531596-002

3. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" CONNECTOR. C1 THRU C22

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⇒ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11							
REVISION	A	A	A	A	A	A	A	A	A	A	A							

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN M. Fogle 5-10-70
CHECK M. Burke 5-20-70
APPR
APPR

NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

ARITHMETIC CARD, O
(LOGIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE D | 545497

SCALE NONE | SHEET 1 OF 11

DWG. NO. 545497 SHEET 11 OF 11

RAYTHEON COMPUTER FORM 67-0084

SIGNAL LIST

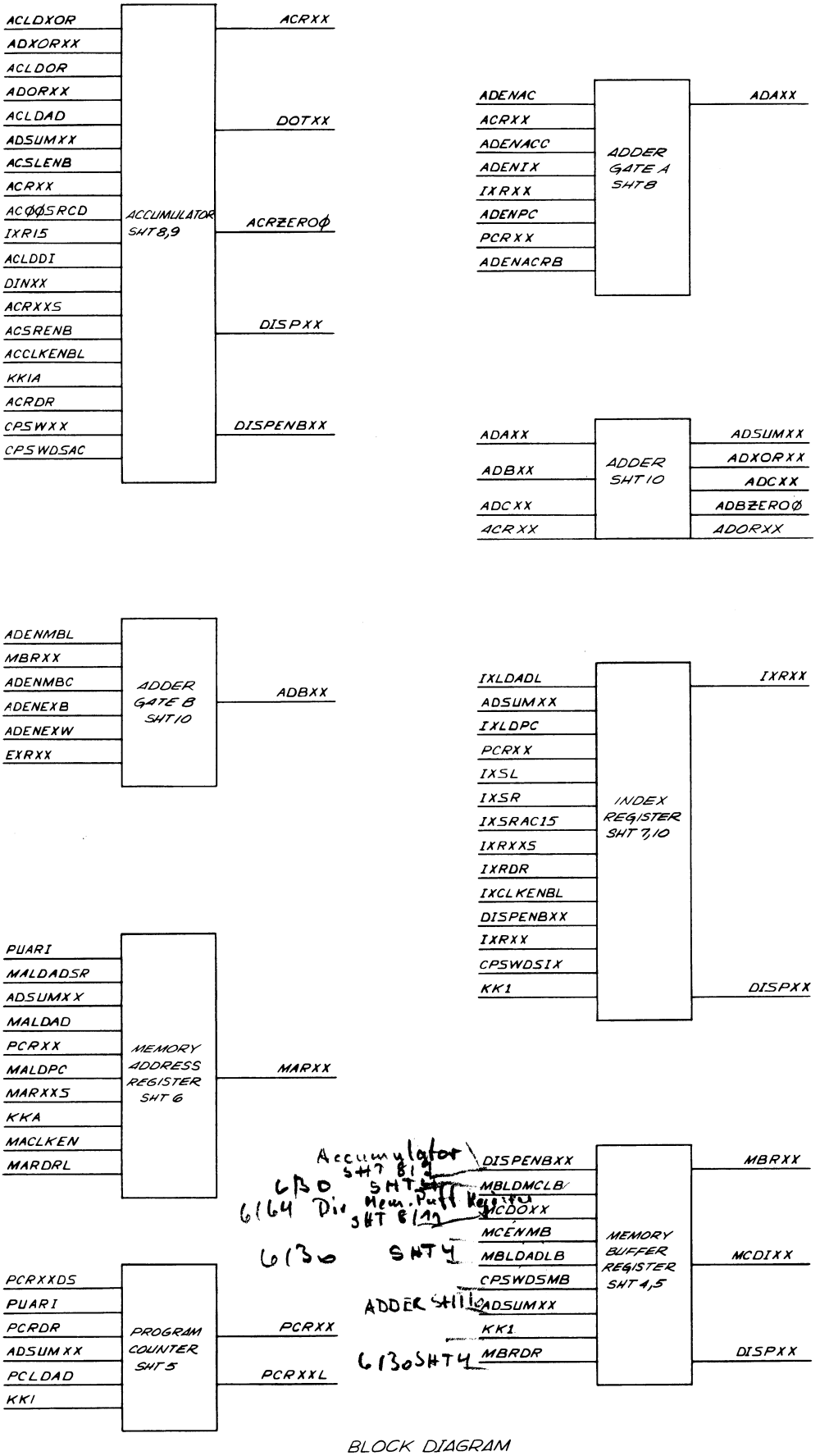
SIGNAL	SOURCE	CONN	SHEET
ACØØSRCD		B47	9
ACCLKENBL		A19	9
ACLDAD		B53	9
ACLDDI		B61	9
ACLDOR		B56	9
ACLDXOR		B54	9
ACRØØ	S	B42	9
ACRØØ-	S	B40	9
ACRØØS	S	B44	9
ACRØ1	S	B50	9
ACRØ1S	S	B48	9
ACRØ2	S	B59	8
ACRØ3	S	B65	8
ACRØ3-	S	B67	8
ACRØ3S	S	B62	8
ACRØ4-		B66	8
ACRØ8		A68	8
ACRØ9		B20	8
ACRIØ		B23	8
ACRII		B36	8
ACRDR-		B52	9
ACRZEROØ	S	B57	9
ACSLENB		B68	8
ACSLENB		B55	9
ACSRENB		B63	8
ACSRENB		B51	9
ADAØØ-	S	B4	8
ADAØ1-	S	B14	8
ADAØ2-	S	B26	8
ADAØ3-	S	B32	8
ADBØØ-	S	B6	10
ADBZEROØ	S	B64	10
ADCØØ-	S	A70	10
ADCØ2-	S	B25	10
ADCØ4-		B18	10
ADENAC		B21	8
ADENACC		B39	8
ADENACRB		B38	8
ADENEXB		B8	10
ADENEXW		B29	10
ADENIX		B34	8
ADENMBC		B35	10
ADENMBL		B3	10
ADENMBL		B37	10
ADENMBL		A67	10
ADENPC		B41	8
ADORØØ-	S	B22	10
ADSUMØØ-	S	A12	10
ADSUMØ1-	S	A18	10
ADSUMØ2-	S	A23	10
ADSUMØ3-	S	A31	10
BPGND		A14	6
BPGND		B11	10
BPGND		B19	10
CPSWØØ-		CU	9
CPSWØ1-		CV	9
CPSWØ2-		CW	9
CPSWØ3-		CX	9
CPSWDSIX-		CZ	10
CPSWDSMB-		CF	5
CPSWINSAC-		CY	9
DINØØ-		B49	9
DINØ1-		B46	9
DINØ2-		B58	8
DINØ3-		B60	8
DISPØØ-	S	CK	9
DISPØ1-	S	CL	9
DISPØ2-	S	CM	9
DISPØ3	S	CN	9
DOTØØ-	S	B7	8
DOTØ1-	S	B15	8
DOTØ2-	S	B24	8
DOTØ3-	S	B33	8
EXRØØ		B9	10
EXRØØ		B10	10
EXRØ1		B12	10

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
EXRØ1		B31	10
EXRØ2		B28	10
EXRØ2		B27	10
EXRØ3		B30	10
IXCLKENBL		A33	10
IXCLKENBL		A36	10
IXLDADL		A52	7
IXLDPC		A65	7
IXRØØ-	S	A42	7
IXRØØS	S	A44	7
IXRØ1-	S	A47	7
IXRØ1S	S	A50	7
IXRØ2-	S	A53	7
IXRØ2S	S	A55	7
IXRØ3-	S	A61	7
IXRØ3S		A49	7
IXRØ4-		A63	7
IXRI5-		B45	9
IXRDR-		A35	7
IXSL		A51	7
IXSR		A56	7
IXSRACI5		A37	7
KKI		A8	9
KKA		A24	6
MACLKEN		A21	6
MALDAD		A17	6
MALDADSR		A28	6
MALDPC		A16	6
MARØØ	S	A11	6
MARØØS	S	A14	6
MARØ1S	S	A13	6
MARØ1S	S	A15	6
MARØ2	S	A27	6
MARØ2S	S	A25	6
MARØ3	S	A34	6
MARØ3S	S	A29	6
MARDRL-		A32	6
MARDRL-		A26	6
MBLDADLB		A10	5
MBLDMCLB		A40	4
MBRØØ-	S	A39	4
MBRØ1	S	B17	4
MBRØ1-	S	A54	4
MBRØ2	S	A30	4
MBRØ2-	S	A58	4
MBRØ3	S	A69	4
MBRØ3-	S	A66	4
MBRDR-		A38	4
MCDIØØ	S	A64	4
MCDIØ1	S	A57	4
MCDIØ2	S	A60	4
MCDIØ3	S	A59	4
MCDOØØ		A46	4
MCDOØ1		A41	4
MCDOØ2		A48	4
MCDOØ3		A45	4
MCENMB		A62	4
PCLDAD		A6	5
PCRØØ-	S	A7	5
PCRØØDS-		CP	5
PCRØØL-	S	CD	5
PCRØ1-	S	A22	5
PCRØ1DS-		CR	5
PCRØ1L-	S	CC	5
PCRØ2-	S	A9	5
PCRØ2DS-		CS	5
PCRØ2L-	S	CB	5
PCRØ3-	S	A20	5
PCRØ3DS-		CT	5
PCRØ3L	S	CA	5
PCRDR-		B43	5
PUARI		B5	5
PUARI		A5	6

CODE IDENT NO.	SIZE		REV
49956	D	545497	A
SCALE NONE		SHEET 2	

RAYTHEON COMPUTER FORM 67-0085



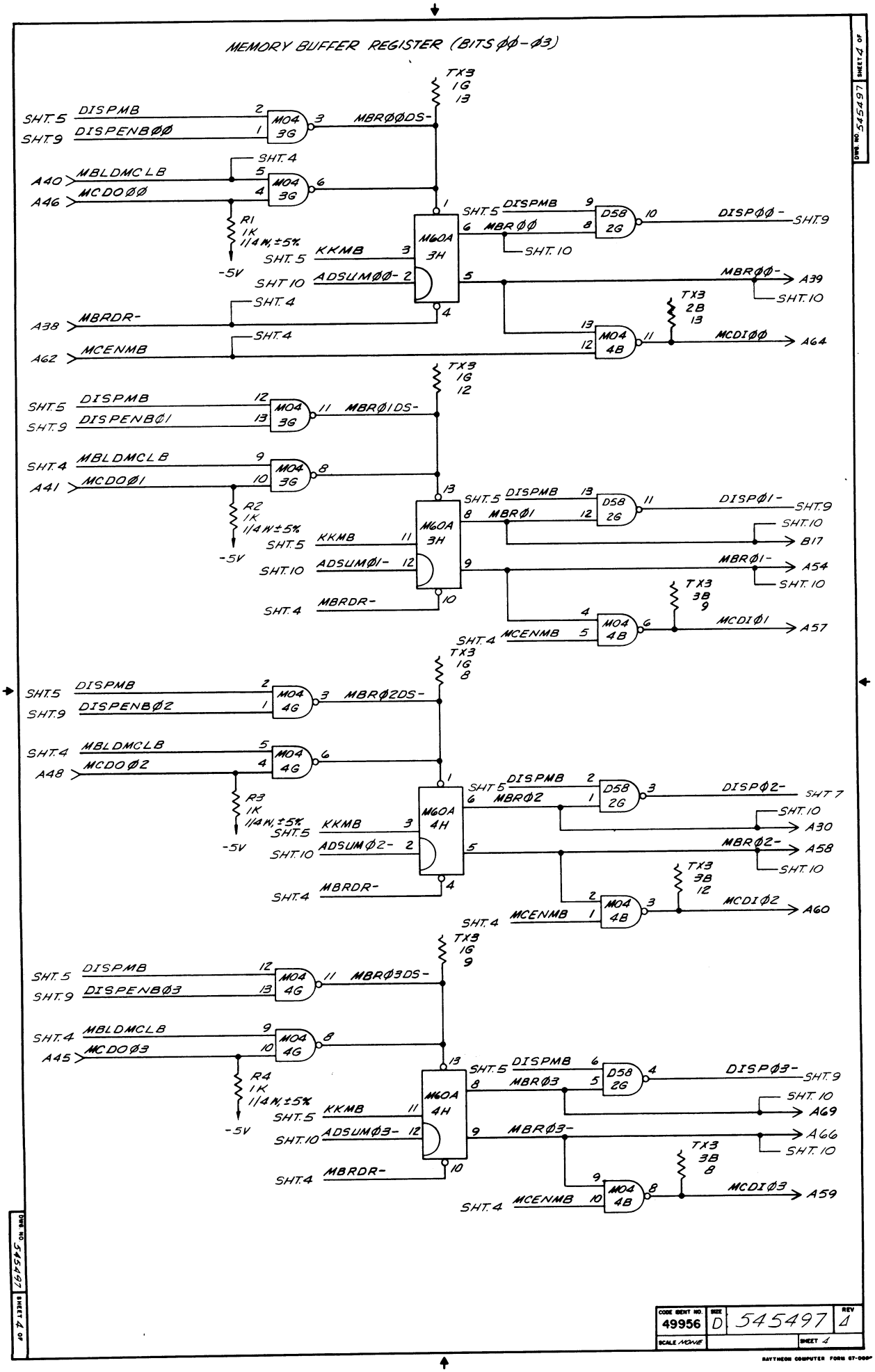
BLOCK DIAGRAM

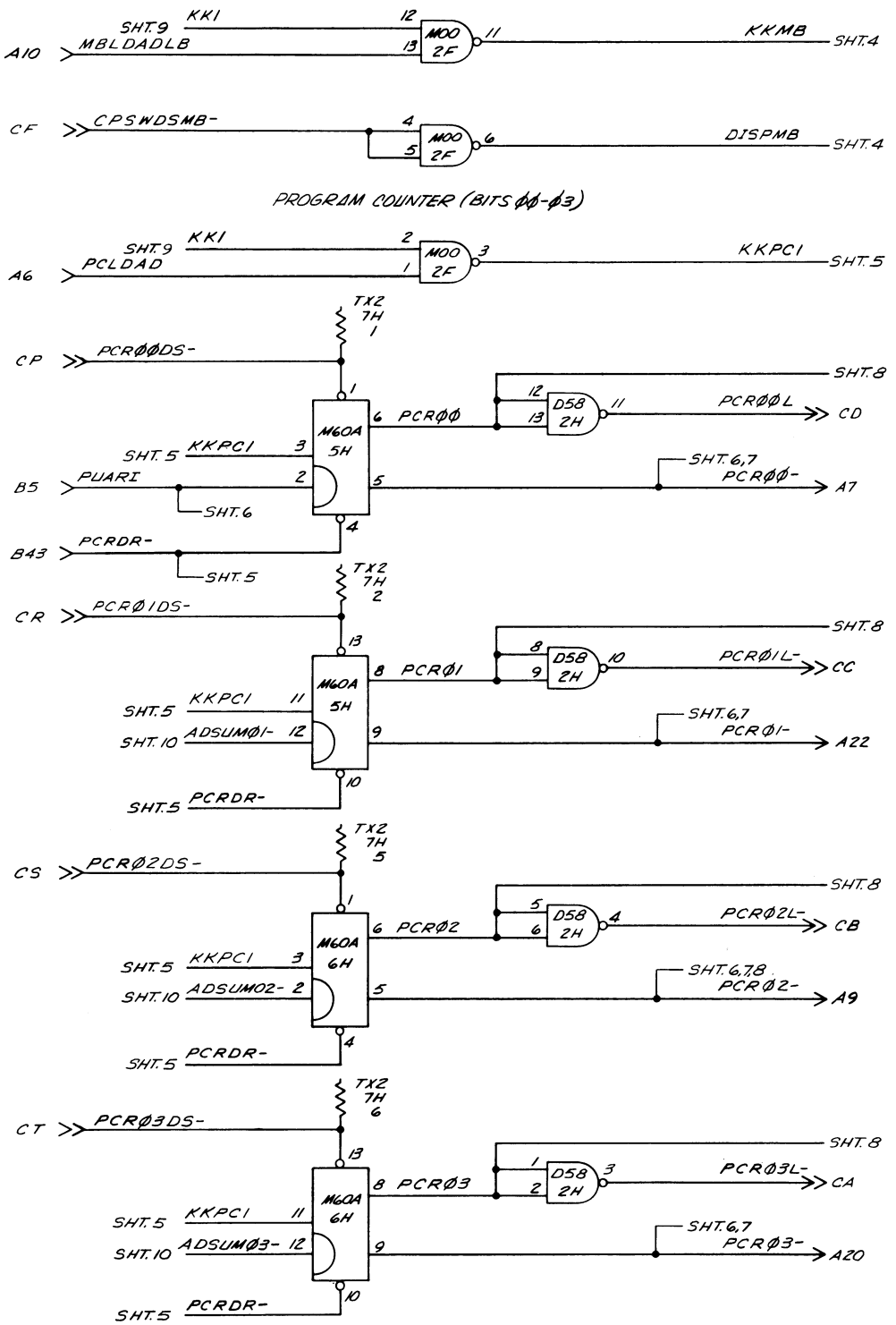
DWG NO 545497 SHEET 3 OF

DWG NO 545497 SHEET 3 OF

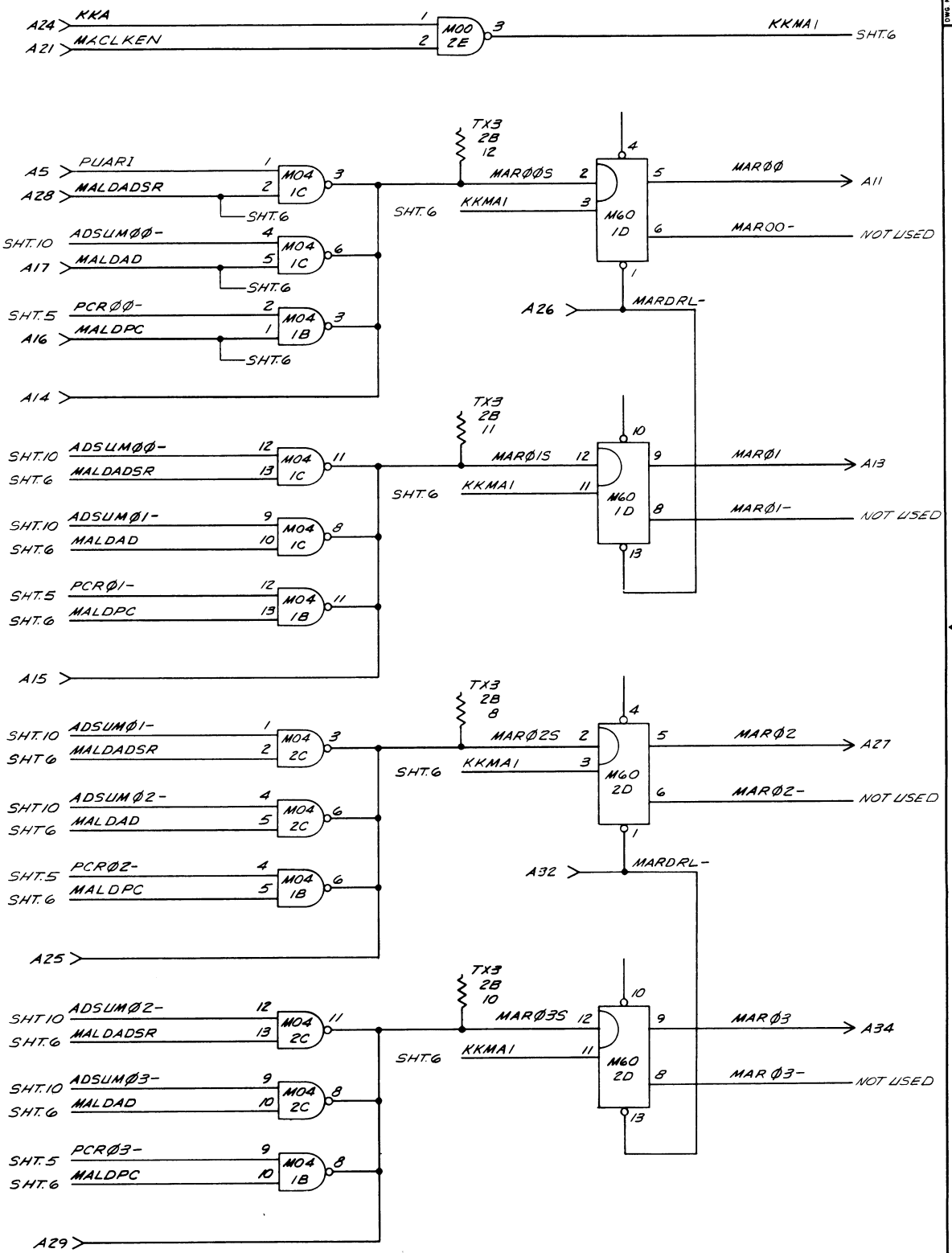
CODE IDENT NO	SIZE		REV
49956	D	545497	A
SCALE NONE		SHEET 3	

RAYTHEON COMPUTER FORM 67-0068


MEMORY BUFFER REGISTER (BITS ØØ-Ø3)
DWG NO 545497 SHEET 4 OF
TX3 1G 13
SHT.5 DISPMB
SHT.9 DISPENBØØ
M04 3G
MBRØØDS-
SHT.4
A40 MBLDMCLB
A46 MCDOØØ
R1 1K 1/4W, ±5%
-5V
SHT.5 KKMB
SHT.10 ADSUMØØ-
M60A 3H
SHT.5 DISPMB
MBRØØ
SHT.10
D58 2G
DISPØØ-
SHT.9
MBRØØ-
A39
SHT.10
A38 MBRDR-
A62 MCENMB
M04 4B
TX3 2B 13
MCDIØØ
A64
TX3 1G 12
SHT.5 DISPMB
SHT.9 DISPENBØ1
MBRØ1DS-
SHT.4 MBLDMCLB
A41 MCDOØ1
R2 1K 1/4W ±5%
SHT.5 KKMB
SHT.10 ADSUMØ1-
MBRDR-
MBRØ1
DISPØ1-
SHT.9
SHT.10
B17
MBRØ1-
A54
SHT.10
TX3 3B 9
MCDIØ1
A57
TX3 1G 8
SHT.5 DISPMB
SHT.9 DISPENBØ2
MBRØ2DS-
SHT.4 MBLDMCLB
A48 MCDOØ2
R3 1K 1/4W, ±5%
SHT.5 KKMB
SHT.10 ADSUMØ2-
MBRDR-
MBRØ2
DISPØ2-
SHT 7
SHT.10
A30
MBRØ2-
A58
SHT.10
TX3 3B 12
MCDIØ2
A60
TX3 1G 9
SHT.5 DISPMB
SHT.9 DISPENBØ3
MBRØ3DS-
SHT.4 MBLDMCLB
A45 MCDOØ3
R4 1K 1/4W, ±5%
SHT.5 KKMB
SHT.10 ADSUMØ3-
MBRDR-
MBRØ3
DISPØ3-
SHT.9
SHT.10
AG9
MBRØ3-
AG6
SHT.10
TX3 3B 8
MCDIØ3
A59
MCENMB
DWG NO 545497 SHEET 4 OF
CODE IDENT NO. 49956
SIZE D
545497
REV A
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-000P

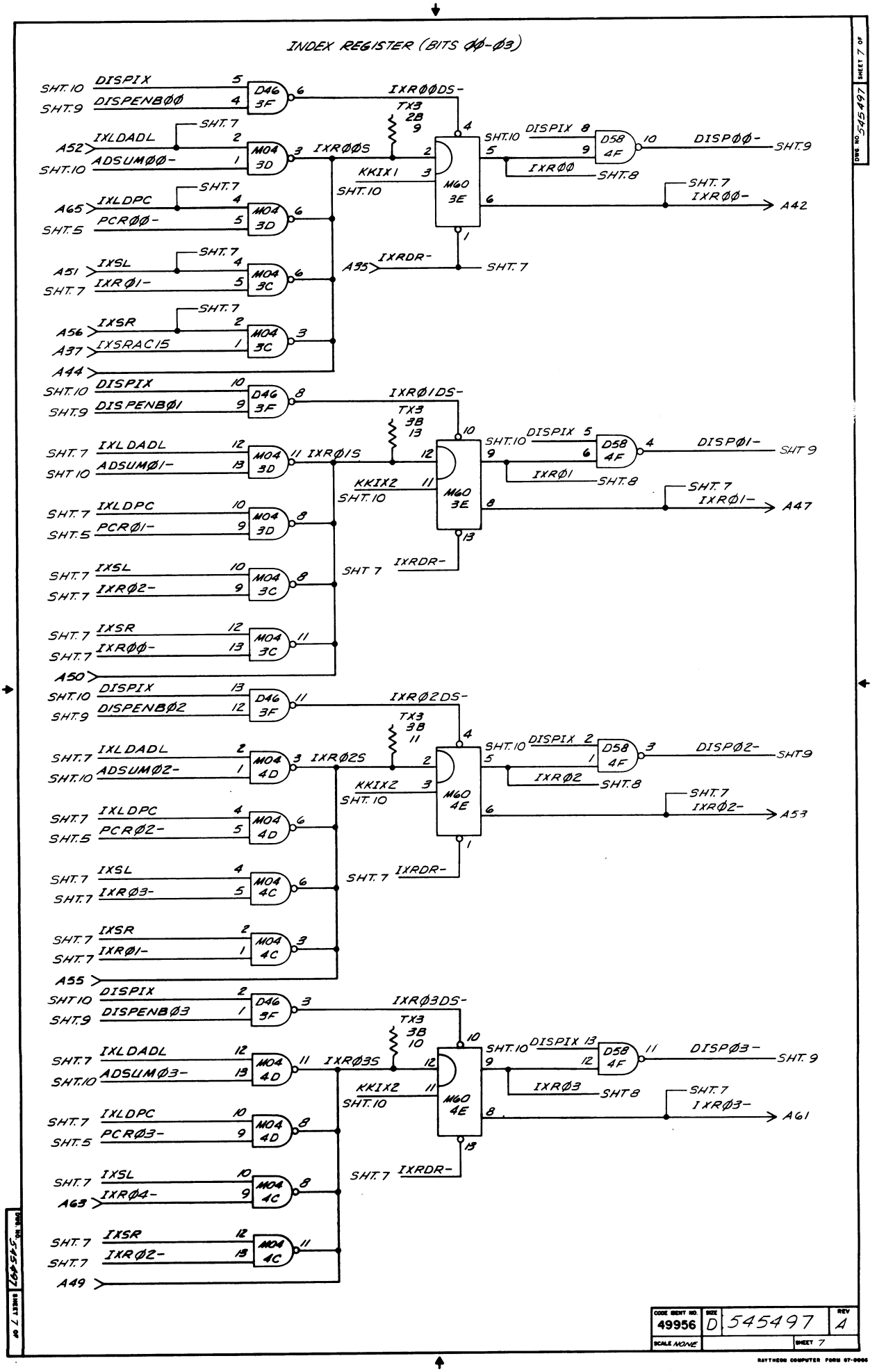

SHT.9
KKI
A10
MBLDADLB
M00 2F
KKMB
SHT.4
CF
CPSWDSMB-
DISPMB
PROGRAM COUNTER (BITS ØØ-Ø3)
PCLDAD
A6
KKPC1
CP
PCRØØDS-
TX2 7H 1
M60A 5H
PCRØØ
D58 2H
PCRØØL
CD
PUARI
B5
SHT.6
SHT.6,7
PCRØØ-
A7
B43
PCRDR-
CR
PCRØ1DS-
TX2 7H 2
PCRØ1
PCRØ1L-
CC
ADSUMØ1-
PCRØ1-
A22
CS
PCRØ2DS-
TX2 7H 5
M60A 6H
PCRØ2
PCRØ2L-
CB
ADSUMØ2-
SHT.6,7,8
PCRØ2-
A9
CT
PCRØ3DS-
TX2 7H 6
PCRØ3
PCRØ3L-
CA
ADSUMØ3-
PCRØ3-
A20

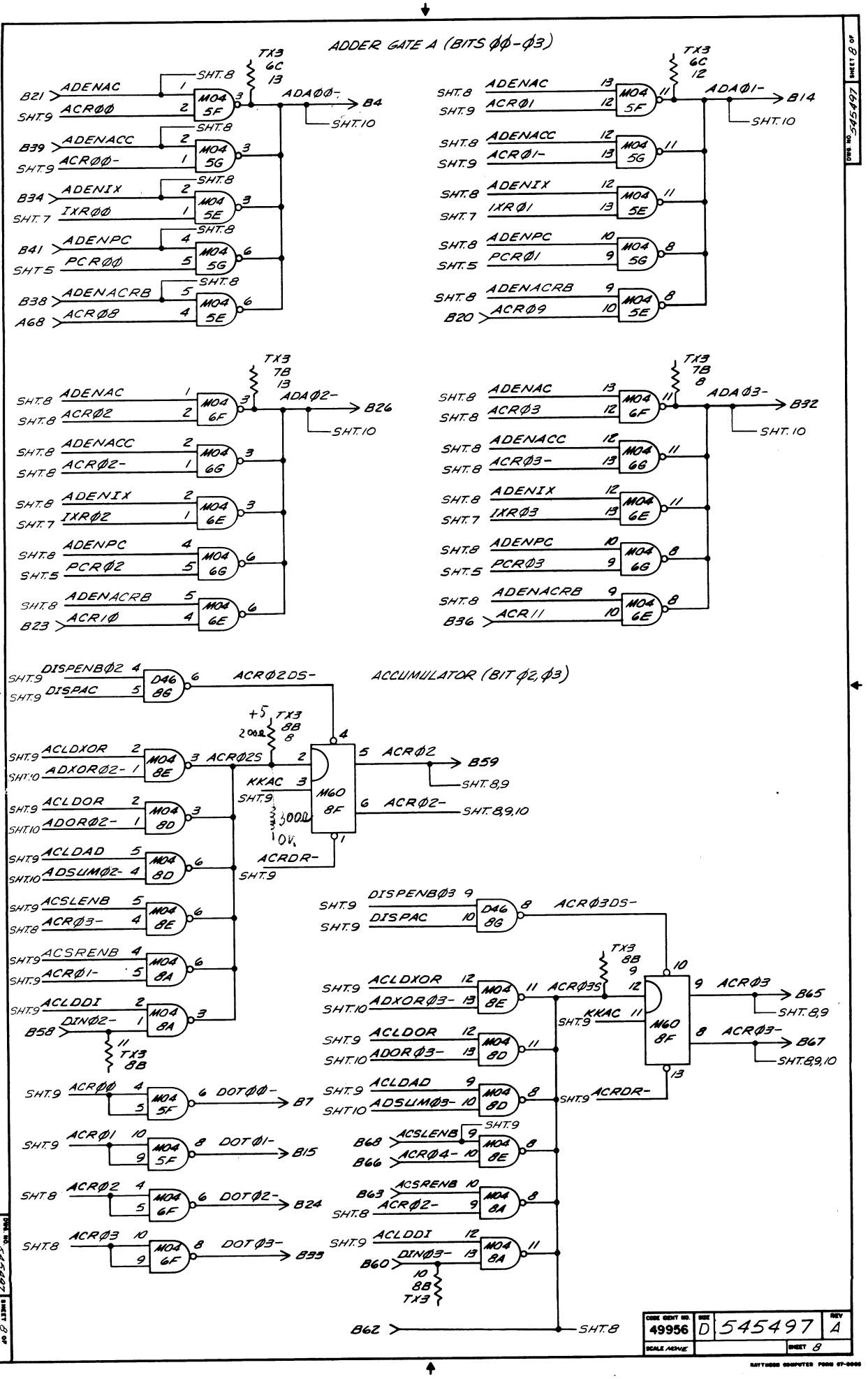
MEMORY ADDRESS REGISTER (BITS ØØ-Ø3)

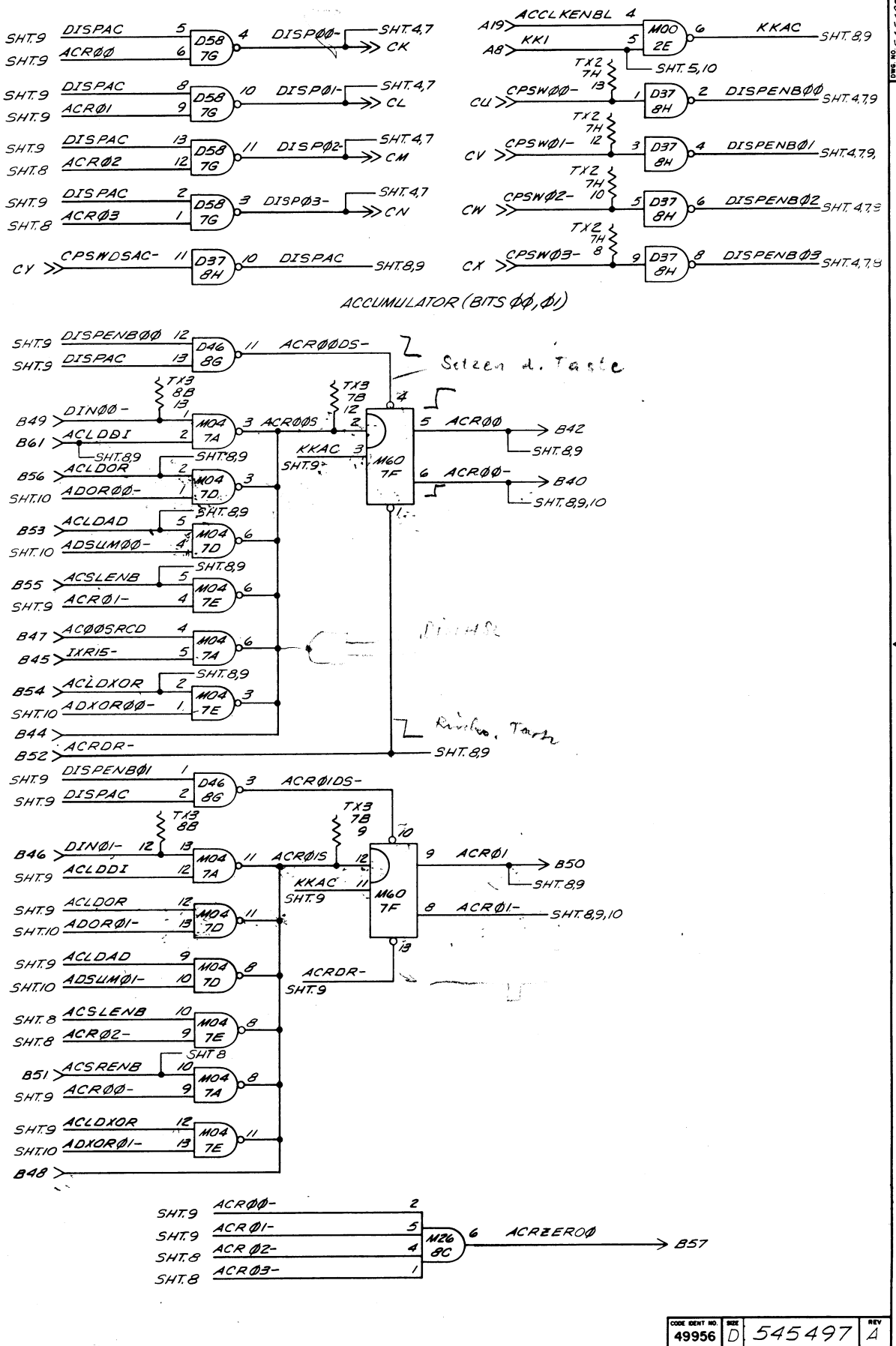


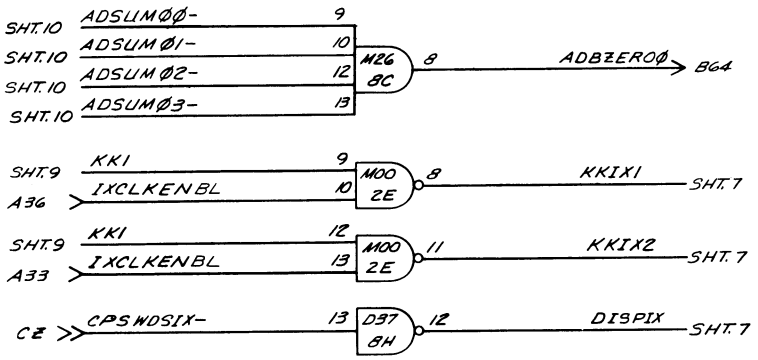
CODE IDENT NO	SIZE		REV
49956	D	545497	A
SCALE NONE		SHEET 6	

RAYTHEON COMPUTER FORM 67-0086

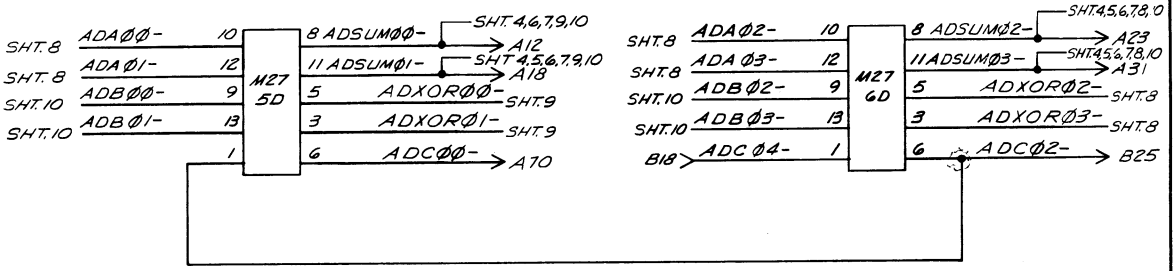

INDEX REGISTER (BITS ØØ-Ø3)
DISPIX
DISPENBØØ
D46 3F
IXRØØDS-
TX3 2B 9
IXLDADL
ADSUMØØ-
M04 3D
IXRØØS
KKIX1
M60 3E
DISPIX
D58 4F
DISPØØ-
IXRØØ
IXLDPC
PCRØØ-
IXSL
IXRØ1-
IXSR
IXSRAC15
IXRDR-
DISPIX
DISPENBØ1
IXRØ1DS-
TX3 3B 13
IXLDADL
ADSUMØ1-
IXRØ1S
KKIX2
DISPØ1-
IXRØ1
IXLDPC
PCRØ1-
IXSL
IXRØ2-
IXSR
IXRØØ-
DISPIX
DISPENBØ2
IXRØ2DS-
TX3 3B 11
IXLDADL
ADSUMØ2-
IXRØ2S
DISPØ2-
IXRØ2
IXLDPC
PCRØ2-
IXSL
IXRØ3-
IXSR
IXRØ1-
DISPIX
DISPENBØ3
IXRØ3DS-
TX3 3B 10
IXLDADL
ADSUMØ3-
IXRØ3S
DISPØ3-
IXRØ3
IXLDPC
PCRØ3-
IXSL
IXRØ4-
IXSR
IXRØ2-
A42
A47
A53
A61
A49
A50
A55
A63
A51
A52
A65
A56
A37
A44
A35
SHT. 7
SHT. 8
SHT. 9
SHT. 10
DWG NO 545497
SHEET 7 OF
49956
545497
REV A
SCALE NONE
SHEET 7


ADDER GATE A (BITS ØØ-Ø3)
ACCUMULATOR (BIT Ø2, Ø3)
DWG NO. 545497
SHEET 8 OF
SIZE D
REV A
CODE IDENT NO. 49956
SCALE NONE
SHEET 8
545497
SHEET 8 OF
RAYTHEON COMPUTER FORM 07-0000

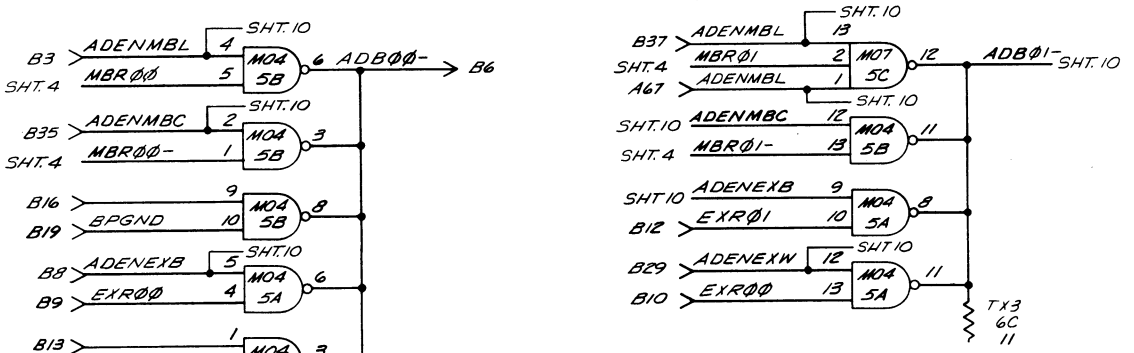

ACCUMULATOR (BITS ØØ, Ø1)
Screen d. Taste
Rückw. Taste

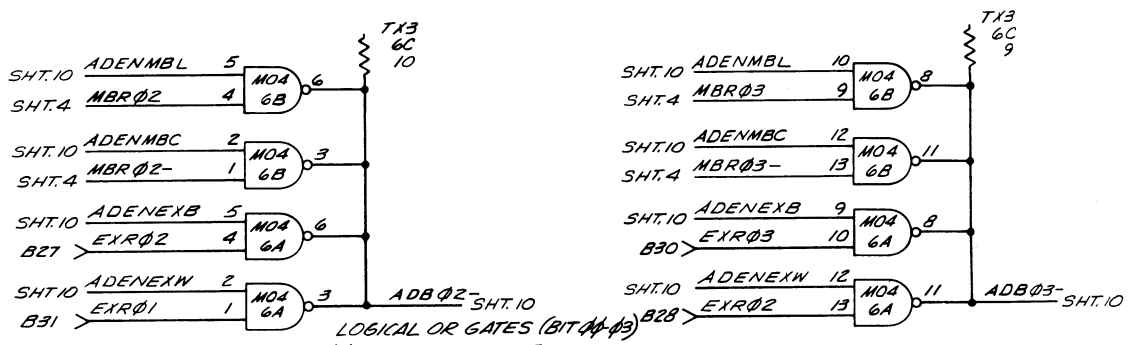


ADDER (BITS ØØ-Ø3)

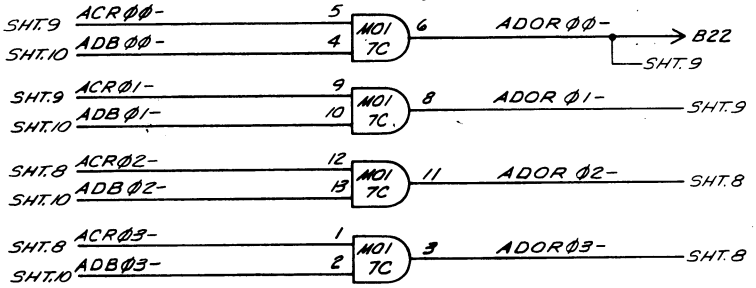


ADDER GATE B (BITS ØØ-Ø3)





LOGICAL OR GATES (BIT ØØ-Ø3)



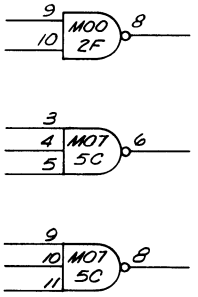
DWG NO. 545497 SHEET 10 OF

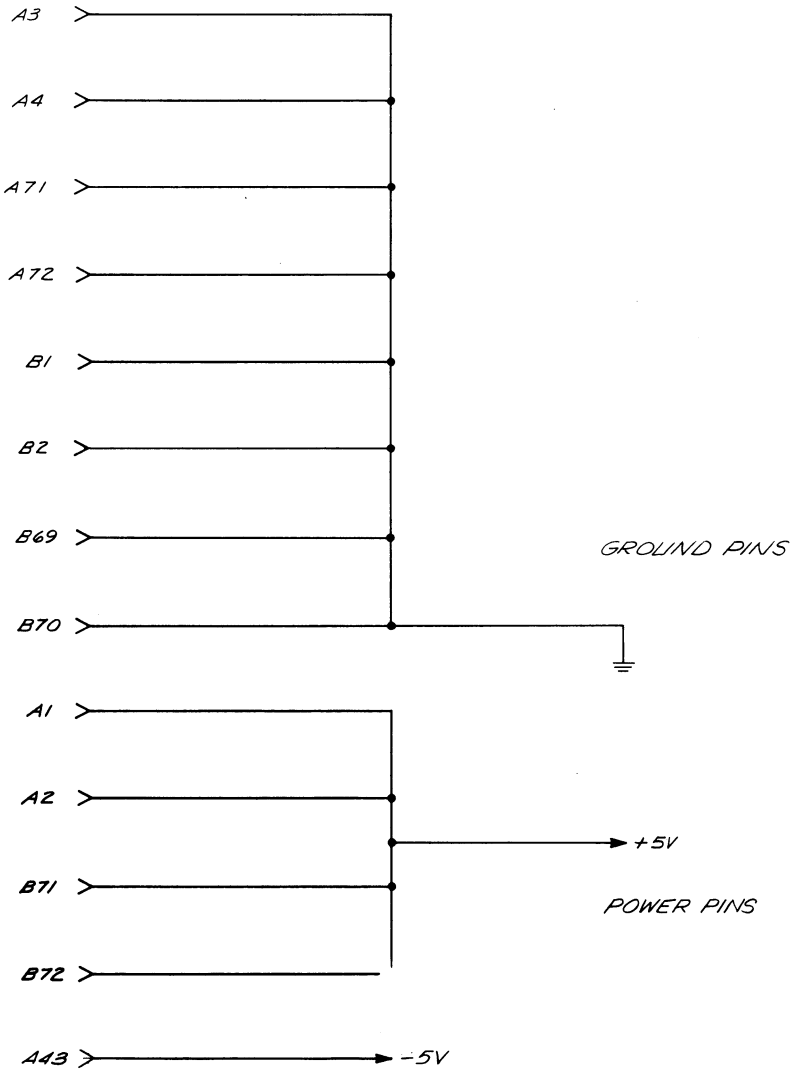
DWG NO. 545497 SHEET 10 OF

CODE IDENT NO.	SIZE		REV
49956	D	545497	A
SCALE NONE		SHEET 10	

RAYTHEON COMPUTER FORM 67-0066

UNUSED IC PARTS





CODE IDENT NO	SIZE		REV
49956	D	545497	A
SCALE NONE		SHEET //	

RAYTHEON COMPUTER FORM 67-0085

RESERVE EO'S OUTSTANDING

REVISIONS								
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER E.O. 20470			[illegible]	71.5	[illegible]	5/14/70
X2	REVISED PER E.O. 20746			MP	71.0	71.0	5/14/70
A	RELEASED PER E.O. 19311			[illegible]	71.0	71.5	5/13/70

SHEET 1 OF 11

DWG. NO. 545498

TABLE OF CONTENTS

GLOSSARY

ACCLKENBL	ACCUMULATOR LEFT BYTE CLOCK ENABLE
ACLOAD	ACCUMULATOR LOAD FROM THE ADDER
ACLDDI	ACCUMULATOR LOAD FROM DIRECT INPUT OUTPUT CHANNEL
ACLDOR	ACCUMULATOR LOAD FROM ADDER OR
ACLDXOR	ACCUMULATOR LOAD FROM ADDER EXCLUSIVE OR
AC∅7SL	ACCUMULATOR SHIFT LEFT BIT ∅7 ENABLE
ACRDR	ACCUMULATOR DIRECT RESET
ACRXX	ACCUMULATOR BIT XX
ACRXXS	ACCUMULATOR BIT XX SET TERM
ACRZERO4	ACCUMULATOR BITS ∅4-∅7 ARE ZERO
ACSLENB	ACCUMULATOR SHIFT LEFT ENABLE
ACSRENB	ACCUMULATOR SHIFT RIGHT ENABLE
ADAXX	ADDER BUS A BIT XX
ADBXX	ADDER BUS B BIT XX
ADBZERO4	ADDER SUM BITS ∅4-∅7 ARE ZERO
ADCXX	ADDER CARRY BIT XX
ADENAC	ADDER ENABLED FROM ACCUMULATOR
ADENACC	ADDER ENABLED FROM ACCUMULATOR COMPLEMENT
ADENACRB	ADDER ENABLED FROM ACCUMULATOR RIGHT BYTE
ADENEXB	ADDER ENABLE FROM EXTENSION REGISTER BYTE
ADENEXW	ADDER ENABLE FROM EXTENSION REGISTER WORD
ADENIX	ADDER ENABLED FROM INDEX REGISTER
ADENMBC	ADDER ENABLE FROM MEMORY BUFFER COMPLEMENT
ADENMBL	ADDER ENABLE FROM MEMORY BUFFER LEFT BYTE
ADENPC	ADDER ENABLED FROM PROGRAM COUNTER
ADFEQL	ADDER EQUAL FLIP-FLOP
ADFNEG	ADDER NEGATIVE FLIP-FLOP
ADFONES	ZERO ADDER BITS ∅5 AND ∅7 FOR INSTRUCTION DECODE ∅5
ADORXX	ADDER OR BIT XX
ADSUMXX	ADDER SUM BIT XX
ADXORXX	ADDER EXCLUSIVE OR BIT XX
CPSWDSAC	CONTROL PANEL SWITCH DISPLAY ACCUMULATOR
CPSWDSIX	CONTROL PANEL SWITCH DISPLAY INDEX REGISTER
CPSWDSMB	CONTROL PANEL SWITCH DISPLAY MEMORY BUFFER
CPSWXX	CONTROL PANEL DATA SWITCH BIT XX
DINXX	DIRECT INPUT CHANNEL BIT XX
DISPENBXX	CONTROL PANEL DATA SWITCH BIT XX INVERTED
DISPXX	CONTROL PANEL DISPLAY BIT XX
DOTXX	DIRECT OUTPUT CHANNEL BIT XX
EXRXX	EXTENSION REGISTER BIT XX
IN∅4SCI-	INSTRUCTION DECODE ∅4 AND SEQUENCER STATE ONE
IXCLKENBL	INDEX REGISTER CLOCK ENABLE LEFT
IXLDADL	INDEX REGISTER LOAD FROM ADDER LEFT BYTE
IXLDPC	INDEX REGISTER LOAD FROM PROGRAM COUNTER
IXRDR	INDEX REGISTER DIRECT RESET
IXRXX	INDEX REGISTER BIT XX
IXRXXS	INDEX REGISTER BIT XX SET TERM
IXSL	INDEX REGISTER SHIFT LEFT
IXSR	INDEX REGISTER SHIFT RIGHT
KK1A	GATED SYSTEM CLOCK
KKAI	UNGATED SYSTEM CLOCK
MACLKEN	MEMORY ADDRESS REGISTER CLOCK ENABLE
MALDAD	MEMORY ADDRESS REGISTER LOAD FROM ADDER
MALDADSR	MEMORY ADDRESS REGISTER LOAD FROM ADDER SHIFTED RIGHT ONE BIT
MALDPC	MEMORY ADDRESS REGISTER LOAD FROM PROGRAM COUNTER
MARDRL	MEMORY ADDRESS REGISTER DIRECT RESET LEFT
MARXX	MEMORY ADDRESS REGISTER BIT XX
MARXXS	MEMORY ADDRESS REGISTER BIT XX SET TERM
MBLDADLB	MEMORY BUFFER LOAD FROM ADDER LEFT BYTE
MBLDMCLB	MEMORY BUFFER LOAD FROM MEMORY LEFT BYTE
MBRDR	MEMORY BUFFER REGISTER DIRECT RESET
MALDADSR	MEMORY BUFFER REGISTER BIT XX
MCDIXX	MEMORY DATA INPUT BIT XX
MCDOXX	MEMORY DATA OUTPUT BIT XX
MCENMB	MEMORY DATA IN ENABLED FROM MEMORY BUFFER
PCLDAD	PROGRAM COUNTER LOAD FROM ADDER
PCRDR	PROGRAM COUNTER DIRECT RESET
PCRXX	PROGRAM COUNTER REGISTER BIT XX
PCRXXDS	PROGRAM COUNTER BIT XX DIRECT SET
SCDCB	SEQUENCES STATE B

TABLE I

I.C. DESIGNATION	RAYTHEON PART NUMBER
D37	531531-001
D46	531147-001
D58	531522-001
M00	531593-006
M01	531593-005
M04	531593-014
M07	531593-015
M26	531593-012
M27	531595-001
M60/M60A	531593-018
TX2	531596-001
TX3	531596-002

3. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" CONNECTOR. C1 THRU C22

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⇒ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11
REVISION	A	A	A	A	A	A	A	A	A	A	A

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS XX ± .05, XXX ± .010; ANGLES ± 0° 30'
2. BREAK SHARP CORNERS .030 MAX
FINISH:

DRAWN	MP Engle	5-07-70
CHECK	M. Bruch	5/14/70
APPR	BARTZ	5/14/70
APPR	[illegible]	5/14/70

NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

ARITHMETIC CARD, 4
(LOGIC DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	545498

SCALE NONE — SHEET 1 OF 11

RAYTHEON COMPUTER FORM 67-0004

DWG. NO. 545498 SHEET 1 OF 11

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACCLKENBL		A19	9
ACLDAD		B53	9
ACLDDI		B61	9
ACLDOR		B56	9
ACLDXOR		B54	9
ACØ7SL	S	B68	8
ACRØ4	S	B42	9
ACRØ3-		B45	9
ACRØ4-	S	B40	9
ACRØ4S	S	B44	9
ACRØ5	S	B50	9
ACRØ5S	S	B48	9
ACRØ6	S	B59	8
ACRØ7	S	B65	8
ACRØ7-	S	B67	8
ACRØ7S	S	B62	8
ACRØ8-		B66	8
ACRI2		A68	8
ACRI3		B20	8
ACRI4		B23	8
ACRI5		B36	8
ACRDR-		B52	9
ACRZERO4	S	B57	9
ACSLENB		B55	9
ACSRENB		B47	9
ACSRENB		B63	8
ACSRENB		B51	9
ADAØ4-	S	B4	8
ADAØ5-	S	B14	8
ADAØ6-	S	B26	8
ADAØ7-	S	B32	8
ADBØ4	S	B6	10
ADBZERO4	S	B64	10
ADCØ4-	S	A70	10
ADCØ6-	S	B25	10
ADCØ8-		B18	10
ADENAC		B21	8
ADENACC		B39	8
ADENACRB		B38	8
ADENEXB		B16	10
ADENEXW		B13	10
ADENIX		B34	8
ADENMBC		B35	10
ADENMBL		B3	10
ADENMBR		B37	10
ADENPC		B41	8
ADFEQL		B27	10
ADFNEG		B12	10
ADFOVF		B30	10
ADONES		B29	10
ADONES		B10	10
ADONES		B28	10
ADORØ4-	S	B22	10
ADSUMØ3-		A5	6
ADSUMØ4-	S	A12	10
ADSUMØ4-		B5	5
ADSUMØ5-	S	A18	10
ADSUMØ6-	S	A23	10
ADSUMØ7-	S	A31	10
BPGND		A3	11
BPGND		B9	10
BPGND		B31	10
CPSWØ4		CU	9
CPSWØ5		CV	9
CPSWØ6		CW	9
CPSWØ7		CX	9
CPSWDSIX-		CZ	10
CPSWDSMB-		CF	5
CPSWPSAC-		CY	9
DINØ4-		B49	9
DINØ5-		B46	9
DINØ6-		B58	8
DINØ7-		B60	8
DISPØ4-	S	CK	9
DISPØ5-	S	CL	9
DISPØ6-	S	CM	9

SIGNAL LIST

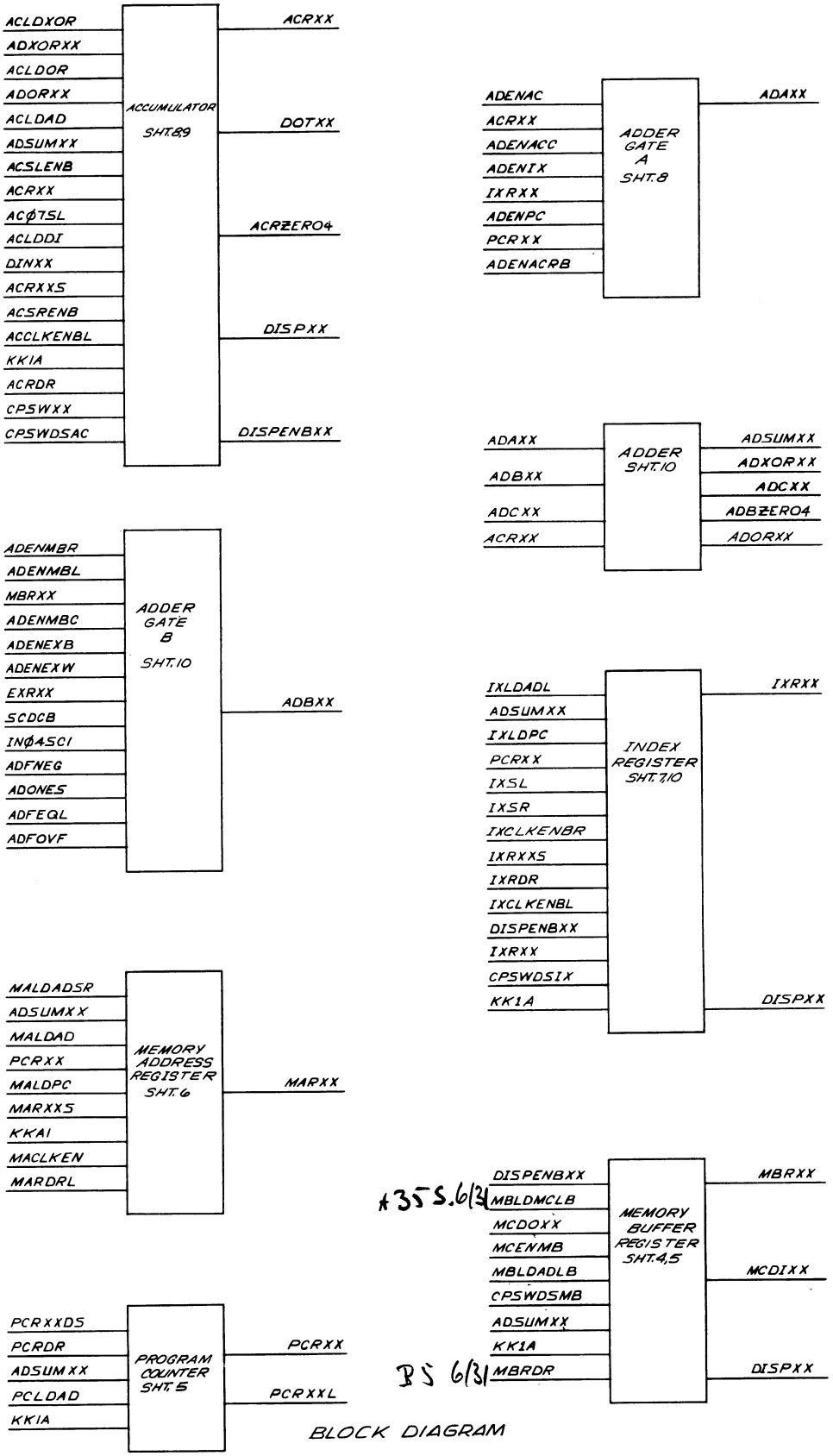
SIGNAL	SOURCE	CONN	SHEET
DISPØ7-	S	CN	9
DOTØ4-	S	B7	8
DOTØ5-	S	B15	8
DOTØ6-	S	B24	8
DOTO7-	S	B33	8
EXRØ3		B11	10
EXRØ4		B19	10
INØ4SCI-		A67	10
ICLKENBL		A36	10
ICLKENBR		A33	10
IXLDADL		A52	7
IXLDPC	S	A65	7
IXRØ3-	S	A37	7
IXRØ4-	S	A42	7
IXRØ4S	S	A44	7
IXRØ5-	S	A47	7
IXRØ5S	S	A50	7
IXRØ6-	S	A53	7
IXRØ6S	S	A55	7
IXRØ7-	S	A61	7
IXRØ7S	S	A49	7
IXRØ8-		A63	7
IXRDR-		A35	7
IXSL		A51	7
IXSR		A56	7
KKIA		A8	9
KKAI		A24	6
MACLKEN		A21	6
MALDAD		A17	6
MALDADSR		A28	6
MALDPC		A16	6
MARØ4	S	A11	6
MARØ4S	S	A14	6
MARØ5	S	A13	6
MARØ5S	S	A15	6
MARØ6	S	A27	6
MARØ6S	S	A25	6
MARØ7	S	A34	6
MARØ7S	S	A29	6
MARDRL-		A32	6
MARDRL-		A26	6
MBLDADLB		A10	5
MBLDMCLB		A40	4
MBRØ4-	S	A39	4
MBRØ5	S	B17	4
MBRØ5-	S	A54	4
MBRØ6	S	A30	4
MBRØ6-	S	A58	4
MBRØ7	S	A69	4
MBRØ7-	S	A66	4
MBRDR-		A38	4
MCDIØ4	S	A64	4
MCDIØ5	S	A57	4
MCDIØ6	S	A60	4
MCDIØ7	S	A59	4
MCDOØ4		A46	4
MCDOØ5		A41	4
MCDOØ6		A48	4
MCDOØ7		A45	4
MCENMB		A62	4
PCLDAD		A6	5
PCRØ4-	S	A7	5
PCRØ4DS-		CP	5
PCRØ4L-	S	CD	5
PCRØ5-	S	A22	5
PCRØ5DS-		CR	5
PCRØ5L-	S	CC	5
PCRØ6-	S	A9	5
PCRØ6DS-		CS	5
PCRØ6L-	S	CB	5
PCRØ7-	S	A20	5
PCRØ7DS-		CT	5
PCRØ7L-	S	CA	5
PCRDR-		B43	5
SCOCB		B8	10

DWG NO 545498 SHEET 2 OF

DWG NO 545498 SHEET 2

CODE IDENT NO.	SIZE		REV
49956	D	545498	A
SCALE NONE		SHEET 2	

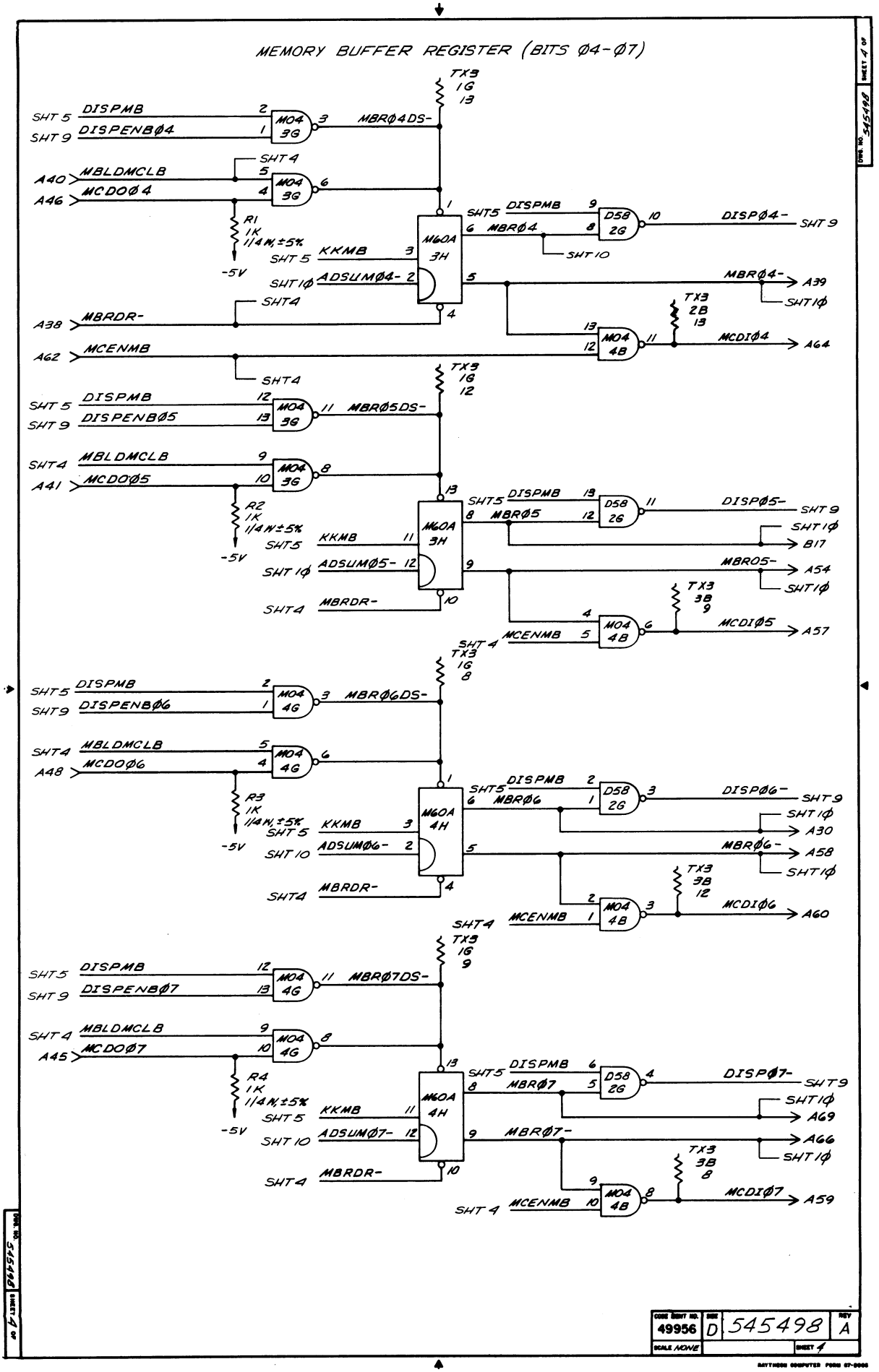
RAYTHEON COMPUTER FORM 67-0085

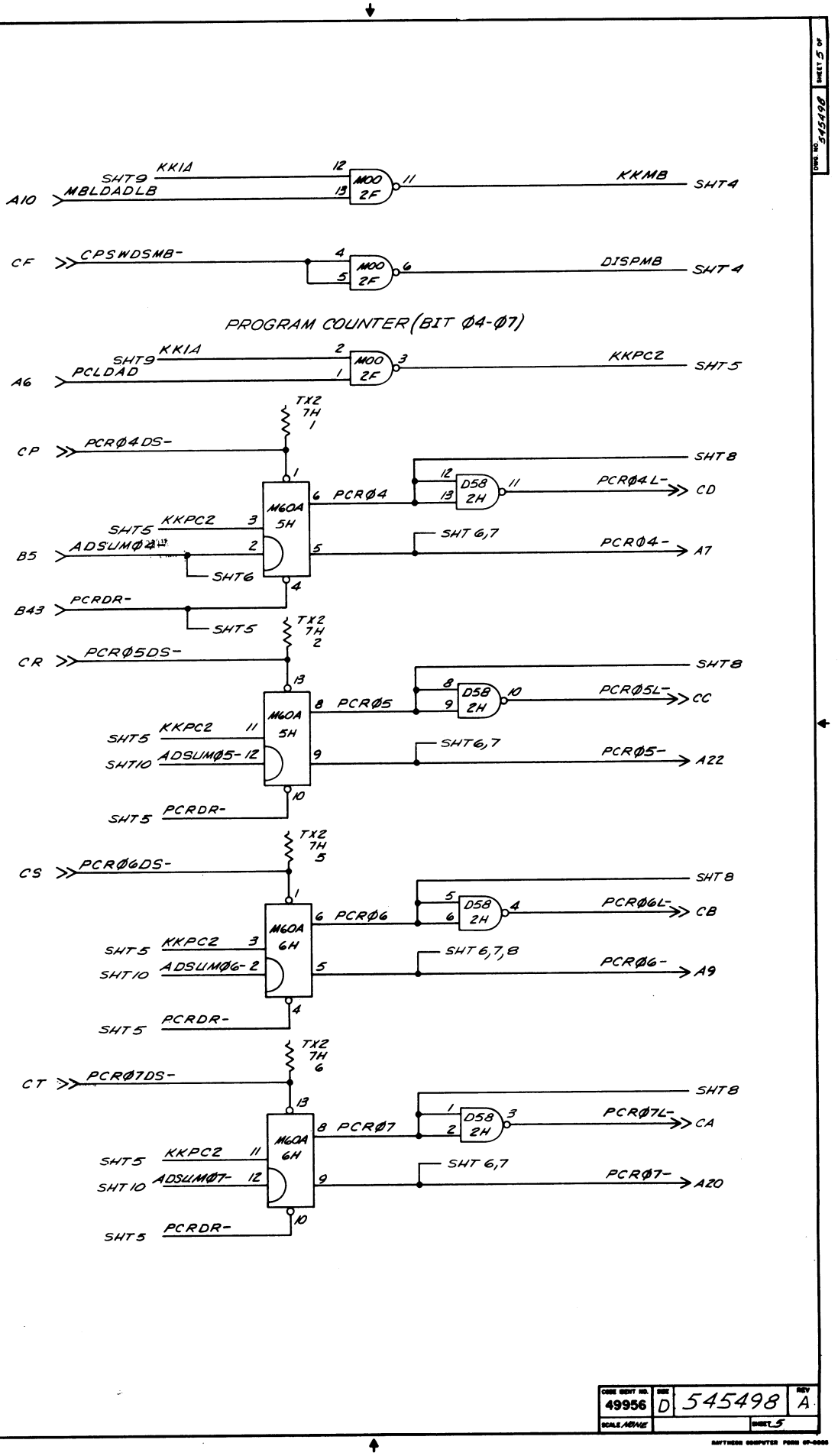


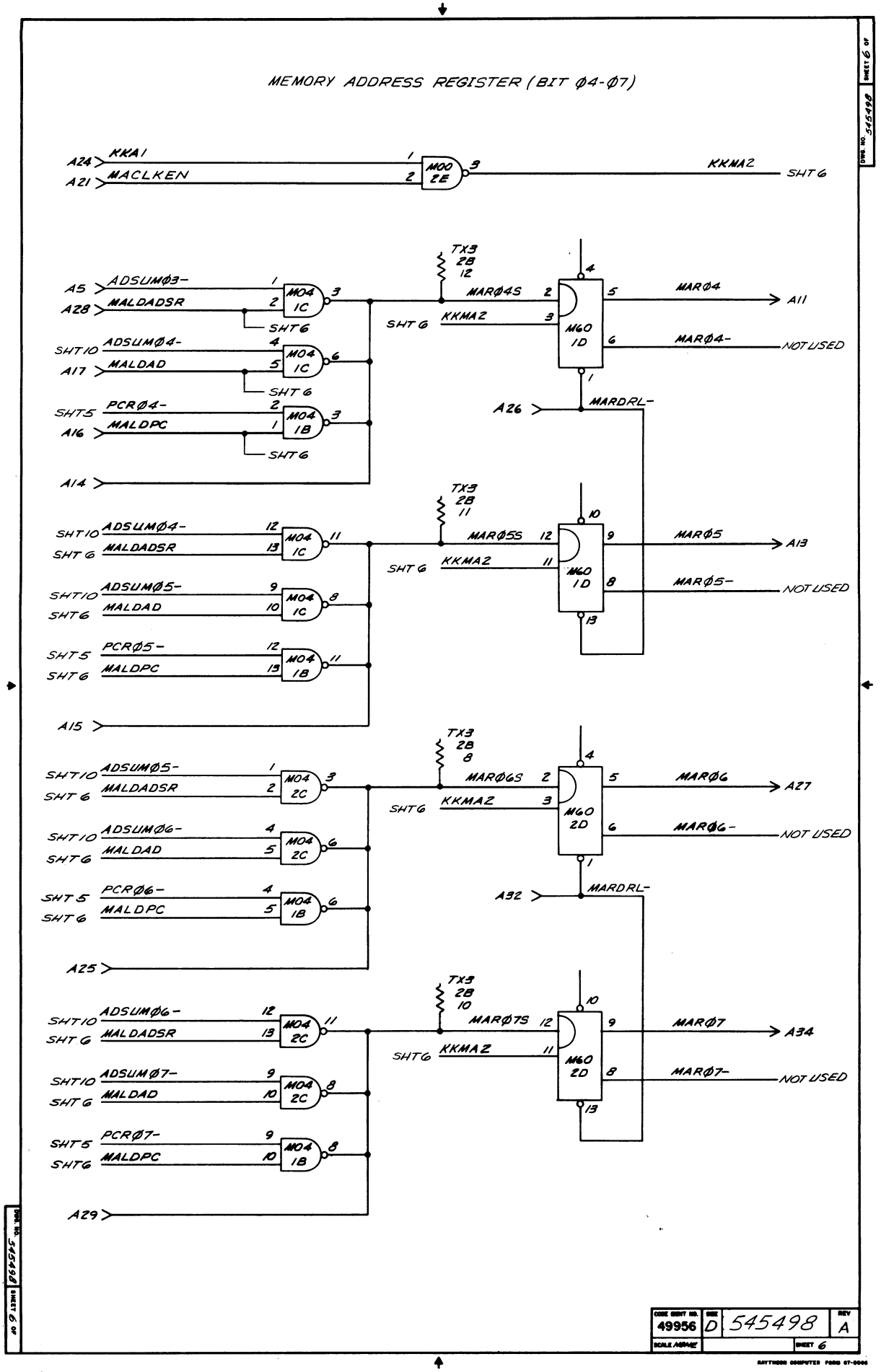
BLOCK DIAGRAM

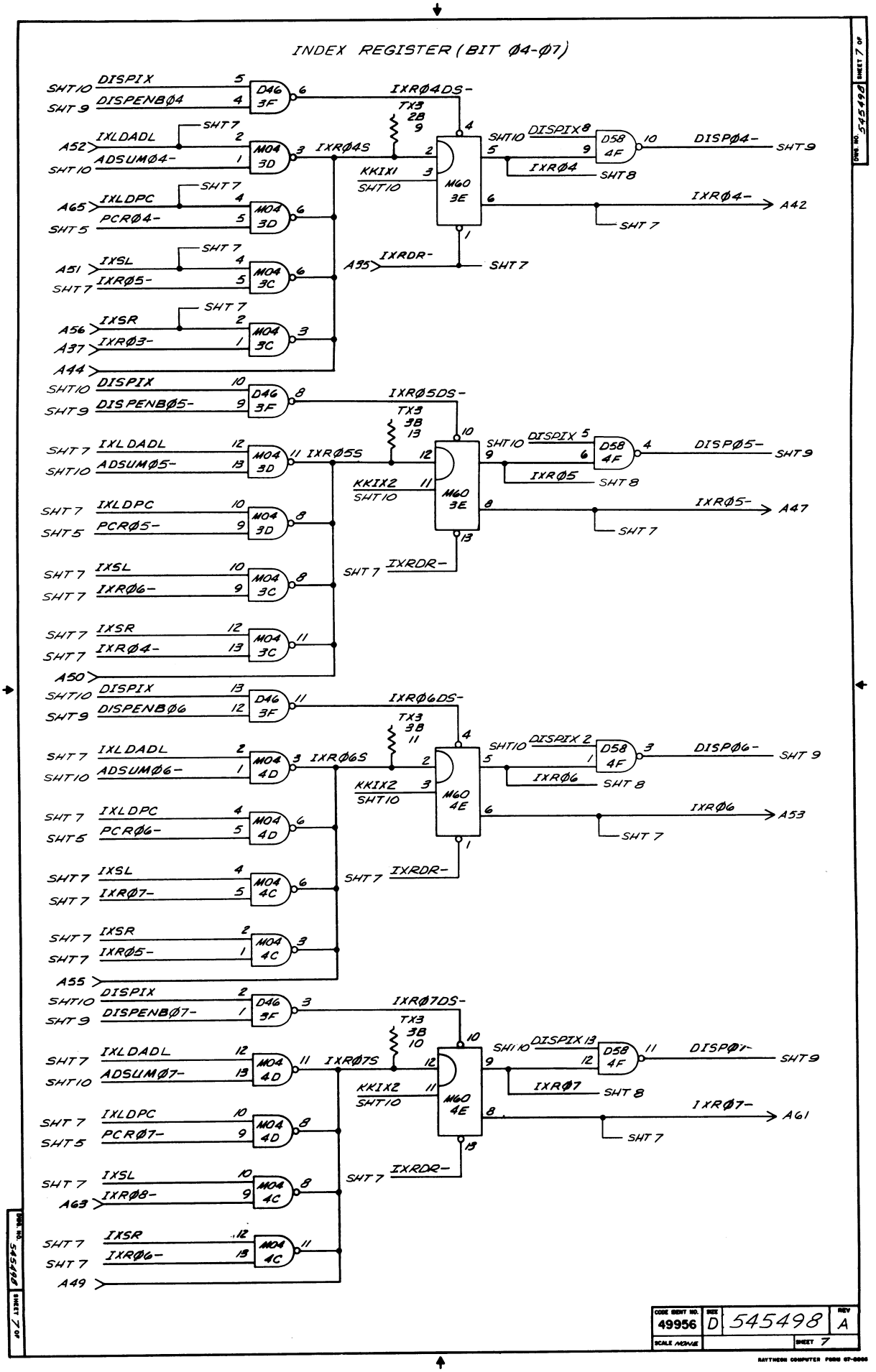
CODE IDENT NO.	SIZE		REV
49956	D	545498	A
SCALE NONE		SHEET 3	

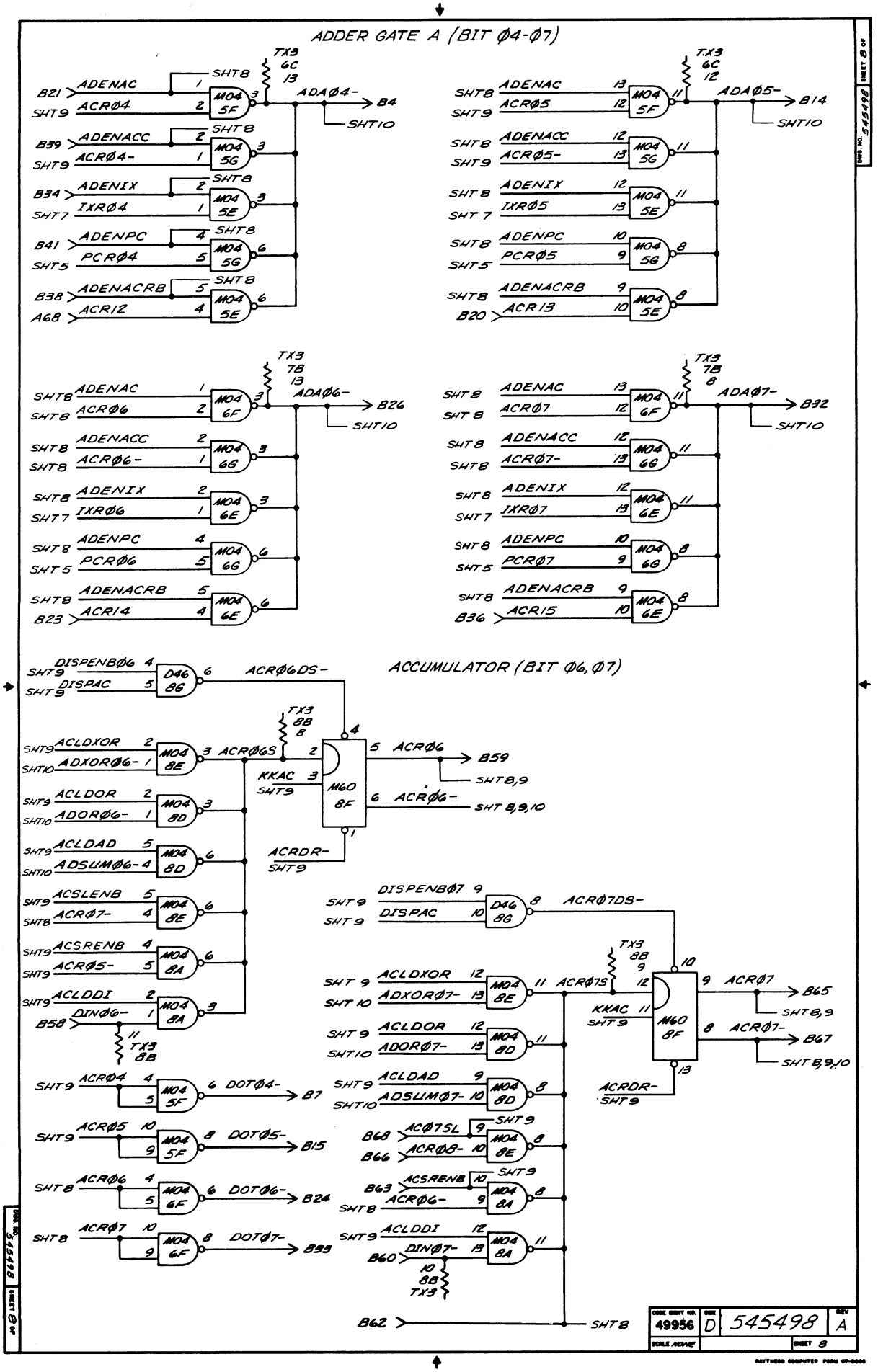
RAYTHEON COMPUTER FORM 57-0006

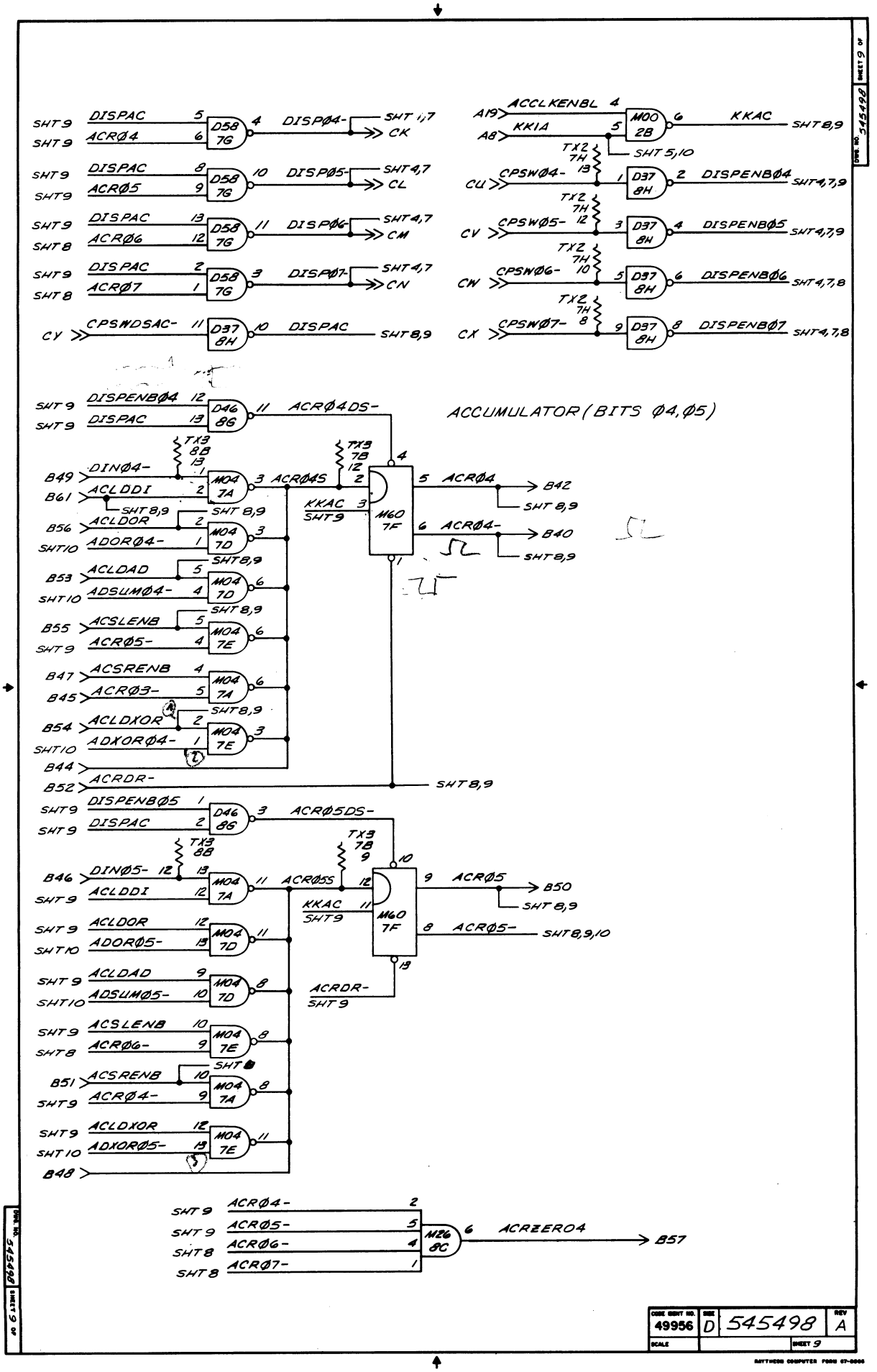

MEMORY BUFFER REGISTER (BITS Ø4-Ø7)
DWG NO 545498 SHEET 1 OF
TX3 1G 13
SHT 5 DISPMB
SHT 9 DISPENBØ4
M04 3G
MBRØ4DS-
SHT 4
A40 MBLDMCLB
A46 MCDOØ4
R1 1K 1/4W ±5%
-5V
M60A 3H
KKMB
SHT 5
SHT 10 ADSUMØ4-
SHT 5 DISPMB
SHT 9 MBRØ4
D58 2G
DISPØ4-
SHT 9
SHT 10
MBRØ4-
A39
SHT 1Ø
TX3 2B 13
A38 MBRDR-
M04 4B
MCDIØ4
A64
A62 MCENMB
TX3 1G 12
SHT 5 DISPMB
SHT 9 DISPENBØ5
MBRØ5DS-
SHT 4 MBLDMCLB
A41 MCDOØ5
R2 1K 1/4W ±5%
SHT 5 KKMB
SHT 1Ø ADSUMØ5-
SHT 4 MBRDR-
SHT 5 DISPMB
MBRØ5
DISPØ5-
SHT 9
SHT 1Ø
B17
MBRO5-
A54
TX3 3B 9
MCDIØ5
A57
SHT 4 MCENMB
TX3 1G 8
SHT 5 DISPMB
SHT 9 DISPENBØ6
MBRØ6DS-
SHT 4 MBLDMCLB
A48 MCDOØ6
R3 1K 1/4W ±5%
SHT 5 KKMB
SHT 10 ADSUMØ6-
SHT 4 MBRDR-
SHT 5 DISPMB
MBRØ6
DISPØ6-
SHT 9
SHT 1Ø
A30
MBRØ6-
A58
TX3 3B 12
MCDIØ6
A60
SHT 4 MCENMB
TX3 1G 9
SHT 5 DISPMB
SHT 9 DISPENBØ7
MBRØ7DS-
SHT 4 MBLDMCLB
A45 MCDOØ7
R4 1K 1/4W ±5%
SHT 5 KKMB
SHT 10 ADSUMØ7-
SHT 4 MBRDR-
SHT 5 DISPMB
MBRØ7
DISPØ7-
SHT 9
SHT 1Ø
A69
MBRØ7-
A66
TX3 3B 8
MCDIØ7
A59
SHT 4 MCENMB
DWG NO 545498 SHEET 4 OF
CODE IDENT NO. 49956
SIZE D
545498
REV A
SCALE NONE
SHEET 1
RAYTHEON COMPUTER FORM 07-0006


SHT9
KKIA
A10
MBLDADLB
M00 2F
KKMB
SHT4
CF
CPSWDSMB-
DISPMB
PROGRAM COUNTER (BIT Ø4-Ø7)
PCLDAD
A6
KKPC2
SHT5
TX2 7H
CP
PCRØ4DS-
M60A 5H
PCRØ4
D58 2H
PCRØ4L-
CD
SHT8
SHT6,7
PCRØ4-
A7
B5
ADSUMØ4
SHT6
B43
PCRDR-
CR
PCRØ5DS-
PCRØ5
PCRØ5L-
CC
PCRØ5-
A22
ADSUMØ5-
SHT10
CS
PCRØ6DS-
PCRØ6
PCRØ6L-
CB
PCRØ6-
A9
ADSUMØ6-
SHT6,7,8
CT
PCRØ7DS-
PCRØ7
PCRØ7L-
CA
PCRØ7-
A20
ADSUMØ7-

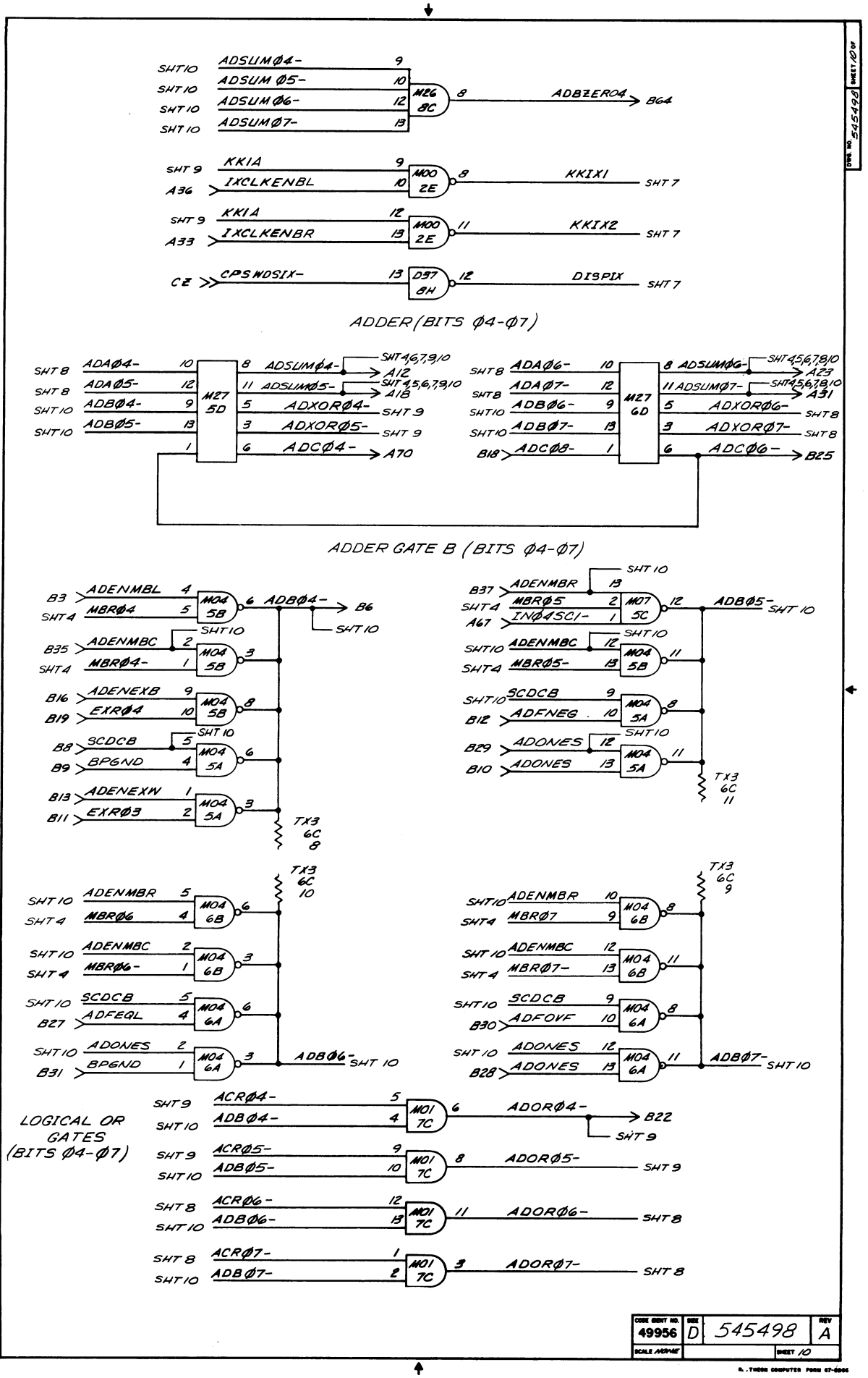

MEMORY ADDRESS REGISTER (BIT Ø4-Ø7)
A24
KKA1
A21
MACLKEN
M00 2E
KKMAZ
SHT 6
A5
ADSUMØ3-
A28
MALDADSR
M04 1C
SHT 6
SHT 10
ADSUMØ4-
A17
MALDAD
SHT 5
PCRØ4-
A16
MALDPC
M04 1B
A14
TX3 2B 12
MARØ4S
M60 1D
MARØ4
A11
MARØ4-
NOT USED
A26
MARDRL-
SHT 10
ADSUMØ4-
SHT 6
MALDADSR
M04 1C
ADSUMØ5-
MALDAD
PCRØ5-
MALDPC
M04 1B
A15
TX3 2B 11
MARØ5S
M60 1D
MARØ5
A13
MARØ5-
NOT USED
ADSUMØ5-
MALDADSR
M04 2C
ADSUMØ6-
MALDAD
PCRØ6-
MALDPC
M04 1B
A25
TX3 2B 8
MARØ6S
M60 2D
MARØ6
A27
MARØ6-
NOT USED
A32
MARDRL-
ADSUMØ6-
MALDADSR
M04 2C
ADSUMØ7-
MALDAD
PCRØ7-
MALDPC
M04 1B
A29
TX3 2B 10
MARØ7S
M60 2D
MARØ7
A34
MARØ7-
NOT USED
DWG. NO. 545498 SHEET 6 OF
CODE IDENT NO. 49956
SIZE D
545498
REV A
SHEET 6
RAYTHEON COMPUTER FORM 67-0006


INDEX REGISTER (BIT Ø4-Ø7)
DWG. NO. 545498 SHEET 7 OF
SHT 10 DISPIX 5
SHT 9 DISPENBØ4 4
D46 3F 6
IXRØ4DS-
TX3 2B 9
A52 IXLDADL 2
SHT 10 ADSUMØ4- 1
M04 3D 3
IXRØ4S
KKIX1 3
SHT 10
M60 3E
SHT 10 DISPIX 8
D58 4F 10
DISPØ4- SHT 9
IXRØ4 SHT 8
IXRØ4- A42
SHT 7
A65 IXLDPC 4
SHT 5 PCRØ4- 5
A95 IXRDR-
SHT 7
A51 IXSL 4
SHT 7 IXRØ5- 5
A56 IXSR 2
A37 IXRØ3- 1
A44
SHT 10 DISPIX 10
SHT 9 DISPENBØ5- 9
D46 3F 8
IXRØ5DS-
TX3 3B 13
SHT 7 IXLDADL 12
SHT 10 ADSUMØ5- 13
M04 3D 11
IXRØ5S
KKIX2 11
SHT 10
M60 3E
SHT 10 DISPIX 5
D58 4F 4
DISPØ5- SHT 9
IXRØ5 SHT 8
IXRØ5- A47
SHT 7
SHT 7 IXLDPC 10
SHT 5 PCRØ5- 9
SHT 7 IXRDR-
SHT 7 IXSL 10
SHT 7 IXRØ6- 9
SHT 7 IXSR 12
SHT 7 IXRØ4- 13
A50
SHT 10 DISPIX 13
SHT 9 DISPENBØ6 12
D46 3F 11
IXRØ6DS-
TX3 3B 11
SHT 7 IXLDADL 2
SHT 10 ADSUMØ6- 1
M04 4D 3
IXRØ6S
KKIX2 3
SHT 10
M60 4E
SHT 10 DISPIX 2
D58 4F 3
DISPØ6- SHT 9
IXRØ6 SHT 8
IXRØ6 A53
SHT 7
SHT 7 IXLDPC 4
SHT 5 PCRØ6- 5
SHT 7 IXRDR-
SHT 7 IXSL 4
SHT 7 IXRØ7- 5
SHT 7 IXSR 2
SHT 7 IXRØ5- 1
A55
SHT 10 DISPIX 2
SHT 9 DISPENBØ7- 1
D46 3F 3
IXRØ7DS-
TX3 3B 10
SHT 7 IXLDADL 12
SHT 10 ADSUMØ7- 13
M04 4D 11
IXRØ7S
KKIX2 11
SHT 10
M60 4E
SHT 10 DISPIX 13
D58 4F 11
DISPØ7- SHT 9
IXRØ7 SHT 8
IXRØ7- A61
SHT 7
SHT 7 IXLDPC 10
SHT 5 PCRØ7- 9
SHT 7 IXRDR-
SHT 7 IXSL 10
A63 IXRØ8- 9
SHT 7 IXSR 12
SHT 7 IXRØ6- 13
A49
DWG. NO. 545498 SHEET 7 OF
CODE IDENT NO. 49956
SIZE D
545498
REV A
SCALE NONE
SHEET 7
RAYTHEON COMPUTER FORM 07-0066

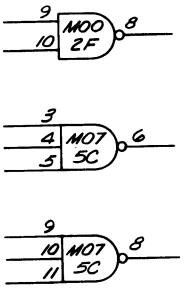

ADDER GATE A (BIT Ø4-Ø7)
ACCUMULATOR (BIT Ø6, Ø7)
DWG. NO. 545498 SHEET 8 OF
545498 SHEET 8 OF
49956
D
545498
A
SHEET 8

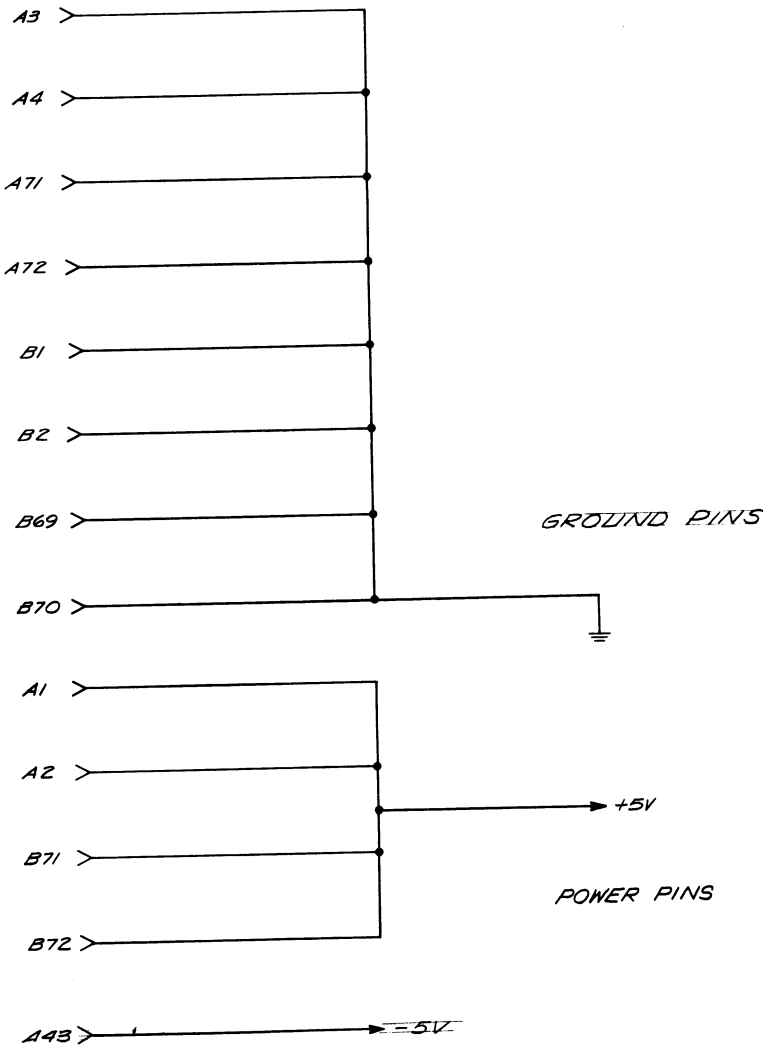


CODE IDENT NO.	SIZE	DWG. NO.	REV
49956	D	545498	A
SCALE		SHEET 9	


ADSUMØ4-
ADSUMØ5-
ADSUMØ6-
ADSUMØ7-
M26 8C
ADBZERO4
KKIA
IXCLKENBL
M00 2E
KKIXI
KKIA
IXCLKENBR
KKIXZ
CPSWDSIX-
D37 8H
DISPIX
ADDER (BITS Ø4-Ø7)
ADAØ4-
ADAØ5-
ADBØ4-
ADBØ5-
M27 5D
ADSUMØ4-
ADSUMØ5-
ADXORØ4-
ADXORØ5-
ADCØ4-
ADAØ6-
ADAØ7-
ADBØ6-
ADBØ7-
ADCØ8-
M27 6D
ADSUMØ6-
ADSUMØ7-
ADXORØ6-
ADXORØ7-
ADCØ6-
ADDER GATE B (BITS Ø4-Ø7)
ADENMBL
MBRØ4
ADENMBC
MBRØ4-
ADENEXB
EXRØ4
SCDCB
BPGND
ADENEXW
EXRØ3
M04 5B
M04 5A
ADBØ4-
TX3 6C 8
ADENMBR
MBRØ5
INØ4SCI-
ADENMBC
MBRØ5-
SCDCB
ADFNEG
ADONES
ADONES
M07 5C
ADBØ5-
TX3 6C 11
ADENMBR
MBRØ6
ADENMBC
MBRØ6-
SCDCB
ADFEQL
ADONES
BPGND
M04 6B
M04 6A
TX3 6C 10
ADBØ6-
ADENMBR
MBRØ7
ADENMBC
MBRØ7-
SCDCB
ADFOVF
ADONES
ADONES
TX3 6C 9
ADBØ7-
LOGICAL OR GATES (BITS Ø4-Ø7)
ACRØ4-
ADBØ4-
M01 7C
ADORØ4-
ACRØ5-
ADBØ5-
ADORØ5-
ACRØ6-
ADBØ6-
ADORØ6-
ACRØ7-
ADBØ7-
ADORØ7-
DWG. NO. 545498 SHEET 10 OF
CODE IDENT NO. 49956
SIZE D
545498
REV A
SHEET 10

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	545498	A
SCALE NONE		SHEET //	

RAYTHEON COMPUTER FORM 67-0005

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER E.O.20470			MS	TB	[illegible]	3/4/70
X2	REVISED PER E.O. 20745			[illegible]	TB	TB	5/4/70
A	RELEASED PER E.O. 19311			HP	TB	TB	9/27/68

SHEET 1 OF 11

DWG. NO. 545499

TABLE OF CONTENTS

GLOSSARY

ACØBSR	ACCUMULATOR BIT Ø8 SHIFT RIGHT ENABLE
ACCLKENBR	ACCUMULATOR RIGHT BYTE CLOCK ENABLE
ACLDAD	ACCUMULATOR LOAD FROM THE ADDER
ACLDDI	ACCUMULATOR LOAD FROM DIRECT INPUT OUTPUT CHANNEL
ACLDOR	ACCUMULATOR LOAD FROM ADDER OR
ACLDXOR	ACCUMULATOR LOAD FROM ADDER EXCLUSIVE OR
ACRDR	ACCUMULATOR DIRECT RESET
ACRXX	ACCUMULATOR BIT XX
ACRXXS	ACCUMULATOR BIT XX SET TERM
ACRZEROB	ACCUMULATOR BITS Ø8-11ARE ZERO
ACSLENB	ACCUMULATOR SHIFT LEFT ENABLE
ACSRENB	ACCUMULATOR SHIFT RIGHT ENABLE
ADAXX	ADDER GATE A BIT XX
ADBXX	ADDER GATE B BIT XX
ADBZEROB	ADDER SUM BITS Ø8-11 ARE ZERO
ADCXX	ADDER CARRY BIT XX
ADENAC	ADDER ENABLED FROM ACCUMULATOR
ADENACC	ADDER ENABLED FROM ACCUMULATOR COMPLEMENT
ADENIX	ADDER ENABLED FROM INDEX REGISTER
ADENMBB	ADDER ENABLE FROM MEMORY BUFFER LEFT BYTE COMPLEMENT
ADENMBBC	ADDER ENABLE FROM MEMORY BUFFER LEFT BYE COMPLEMENT
ADENMBC	ADDER ENABLE FROM MEMORY BUFFER COMPLEMENT
ADENMBR	ADDER ENABLE FROM MEMORY BUFFER RIGHT BYTE
ADENPC	ADDER ENABLED FROM PROGRAM COUNTER
ADORXX	ADDER OR BIT XX
ADSUMXX	ADDER SUM BIT XX
ADXORXX	ADDER EXCLUSIVE OR BIT XX
BPGND	BACK PLAINE GROUND FOR UNUSED GATES
CCFGLB	CENTRAL CONTROL FLIP FLOP GLOBAL MODE
CPSWDSAC	CONTROL PANEL SWITCH DISPLAY ACCUMULATOR
CPSWDSIX	CONTROL PANEL SWITCH DISPLAY INDEX REGISTER
CPSWPSMB	CONTROL PANEL SWITCH DISPLAY MEMORY BUFFER
CPSWXX	CONTROL PANEL DATA SWITCH BIT XX
DINXX	DIRECT INPUT CHANNEL BIT XX
DISPENBXX	CONTROL PANEL DATA SWITCH BIT XX INVERTED
DISPXX	CONTROL PANEL DISPLAY BIT XX
DOTXX	DIRECT OUTPUT CHANNEL BIT XX
IXCLKENBR	INDEX REGISTER CLOCK ENABLE RIGHT
IXLDADR	INDEX REGISTER LOAD FROM ADDER RIGHT BYTE
IXLDPC	INDEX REGISTER LOAD FROM PROGRAM COUNTER
IXRI5	INDEX REGISTER BIT 15
IXRDR	INDEX REGISTER DIRECT RESET
IXRXX	INDEX REGISTER BIT XX
IXRXXS	INDEX REGISTER BIT XX SET TERM
IXSL	INDEX REGISTER SHIFT LEFT
IXSR	INDEX REGISTER SHIFT RIGHT
KKA2	UNGATED SYSTEM CLOCK
KK1B	GATED SYSTEM CLOCK
MACLKEN	MEMORY ADDRESS REGISTER CLOCK ENABLE
MALDAD	MEMORY ADDRESS REGISTER LOAD FROM ADDER
MALDADSR	MEMORY ADDRESS REGISTER LOAD FROM ADDER SHIFTED RIGHT ONE BIT
MALDPC	MEMORY ADDRESS REGISTER LOAD FROM PROGRAM COUNTER
MARDRL	MEMORY ADDRESS REGISTER DIRECT RESET LEFT
MARXX	MEMORY ADDRESS REGISTER BIT XX
MARXXS	MEMORY ADDRESS REGISTER BIT XX SET TERM
MBLDADRB	MEMORY BUFFER LOAD FROM ADDER RIGHT BYTE
MBLDMCRB	MEMORY BUFFER LOAD FROM MEMORY RIGHT BYTE
MBRDR	MEMORY BUFFER REGISTER DIRECT RESET
MBRXX	MEMORY BUFFER REGISTER BIT XX
MCDIXX	MEMORY DATA INPUT BIT XX
MCDOXX	MEMORY DATA OUTPUT BIT XX
MCENMB	MEMORY DATA IN ENABLED FROM MEMORY BUFFER
MRESET	MASTER RESET
PCLDAD	PROGRAM COUNTER LOAD FROM ADDER
PCRDR	PROGRAM COUNTER DIRECT RESET
PCRXX	PROGRAM COUNTER REGISTER BIT XX
PCRXXDS	PROGRAM COUNTER BIT XX DIRECT SET
PUARI	ARITHMETIC CARD UNUSED INPUT PULL UP
SCDCB	SEQUENCER DECODE STATE B

TABLE 1

I.C. DESIGNATION	RAYTHEON PART NUMBER
D37	531531-001
D46	531147-001
D58	531522-001
M00	531593-006
M01	531593-005
M04	531593-014
M07	531593-015
M26	531593-012
M27	531595-001
M60/M60A	531593-018
TX2	531596-001
TX3	531596-002

3. THE FOLLOWING PINS ARE TIED TO GROUND ON 2" CONNECTOR, C1 THRU C22
2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS
1. ⇒ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11
REVISION	A	A	A	A	A	A	A	A	A	A	A

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON:
DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:

DRAWN M. Fogel 3.11.70
CHECK T. Bowtz 3/4/70
APPR [illegible] 3/4/70
APPR [illegible] 3/4/70
NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

ARITHMETIC CARD, 8 LOGIC DIAGRAM

CODE IDENT NO. 49956 | SIZE D | 545499

SCALE NONE | SHEET 1 OF 11

DWG. NO. 545499 SHEET 1 OF 11

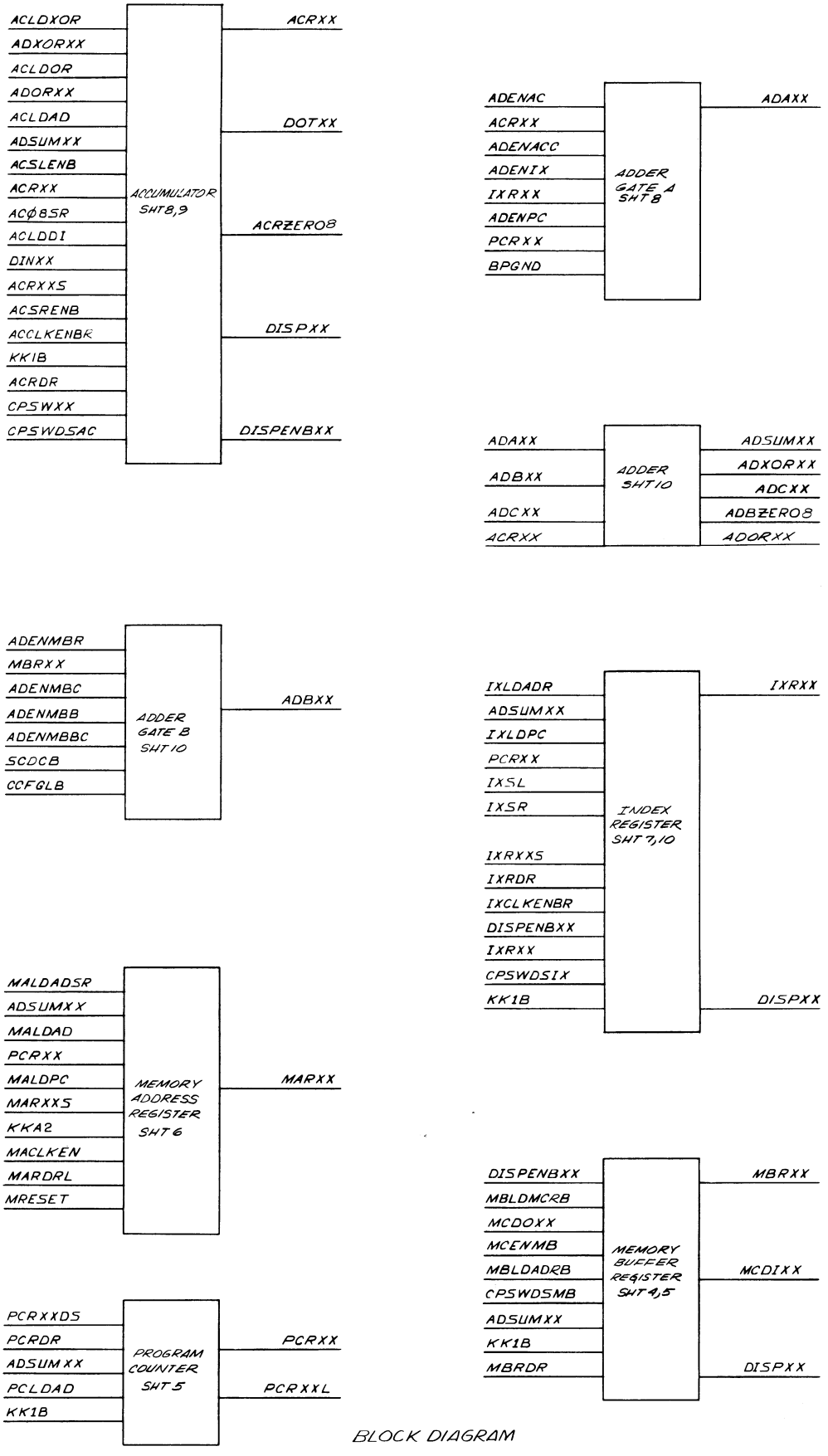
RAYTHEON COMPUTER FORM 67-0084

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACØ8SR		B47	9
ACCLKENBR		A19	9
ACLDAD		B53	9
ACLDDI		B61	9
ACLDOR		B56	9
ACLDXOR		B54	9
ACRØ7-		B45	9
ACRØ8	S	B42	9
ACRØ8-	S	B4Ø	9
ACRØ8S	S	B44	9
ACRØ9	S	B5Ø	9
ACRØ9S	S	B48	9
ACRIØ	S	B59	8
ACRII	S	B65	8
ACRII-	S	B67	8
ACRIIS	S	B62	8
ACRI2-		B66	8
ACRDR-		B52	9
ACRZEROB	S	B57	9
ACSLENB		B68	8
ACSLENB		B55	9
ACSRENB		B63	8
ACSRENB		B51	9
ADAØ8-	S	B4	8
ADAØ9-	S	B14	8
ADAIØ-	S	B26	8
ADAII-	S	B32	8
ADBØ8-	S	B6	IØ
ADBZEROB	S	B64	IØ
ADCØ8-	S	A7Ø	IØ
ADCIØ-	S	B25	IØ
ADCI2-		B18	IØ
ADENAC		B21	8
ADENACC		B39	8
ADENIX		B34	8
ADENMBB		B8	IØ
ADENMBBC		B29	IØ
ADENMBBC		B13	IØ
ADENMBC		B35	IØ
ADENMBR		B3	IØ
ADENMBR		B37	IØ
ADENMBR		A67	IØ
ADENPC		B41	8
ADORØ8	S	B22	IØ
ADSUMØ7-		A5	6
ADSUMØ8-		B5	5
ADSUMØ8-	S	A12	IØ
ADSUMØ9-	S	A18	IØ
ADSUMIØ-	S	A23	IØ
ADSUMII-	S	A31	IØ
BPGND		B36	8
BPGND		A68	8
BPGND		B2Ø	8
BPGND		B23	8
CCFGLB		B19	IØ
CPSWØ8-		CU	9
CPSWØ9-		CV	9
CPSWIØ-		CW	9
CPSWII-		CX	9
CPSWDSIX-		CZ	IØ
CPSWDSMB-		CF	5
CPSWDSAC-		CY	9
DINØ8-		B49	9
DINØ9-		B46	9
DINIØ-		B58	8
DINII-		B6Ø	8
DISPØ8-	S	CK	9
DISPØ9-	S	CL	9
DISPIØ-	S	CM	9
DISPII-	S	CN	9
DOTØ8-	S	B7	8
DOTØ9-	S	B15	8
DOTIØ-	S	B24	8
DOTII-	S	B33	8

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
IXCLKENBR		A33	IØ
IXCLKENBR		A36	IØ
IXLOADR		A52	7
IXLDPC		A65	7
IXRØ7-		A37	7
IXRØ8-	S	A42	7
IXRØ8S	S	A44	7
IXRØ9-	S	A47	7
IXRØ9S	S	A5Ø	7
IXRIØ-	S	A53	7
IXRIØS	S	A55	7
IXRII-	S	A61	7
IXRIIS	S	A49	7
IXRI2-		A63	7
IXRDR-		A35	7
IXSL		A51	7
IXSR		A56	7
KK1B		A8	9
KKA2		A24	6
MACLKEN		A21	6
MALDAD		A17	6
MALDADSR		A28	6
MALDPC		A16	6
MARØ8	S	A11	6
MARØ8S	S	A14	6
MARØ9	S	A13	6
MARØ9S	S	A15	6
MARIØ	S	A27	6
MARIØS	S	A25	6
MARII	S	A34	6
MARIIS	S	A29	6
MARDRL-		A26	6
MBLDADRB		A1Ø	5
MBLDMCRB		A4Ø	4
MBRØØ-		B11	IØ
MBRØØD		B9	IØ
MBRØ8-	S	A39	IØ
MBRØI-		B1Ø	IØ
MBRØ9	S	B17	4
MBRØI		B12	IØ
MBRØ9-	S	A54	4
MBRØ2-		B31	IØ
MBRIØ	S	A3Ø	4
MBRØ3-		B28	IØ
MBRIØ-	S	A58	4
MBRØ2		B27	IØ
MBRII	S	A69	4
MBRØ3		B3Ø	IØ
MBRII-	S	A66	4
MBRDR-		A38	4
MCDIØ8	S	A64	4
MCDIØ9	S	A57	4
MCDIIØ	S	A60	4
MCDIII	S	A59	4
MCDOØ8		A46	4
MCDOØ9		A41	4
MCDOIØ		A48	4
MCDOII		A45	4
MCENMB		A62	4
MRESET-		A32	6
PCLDAD		A6	5
PCRØ8-	S	A7	5
PCRØ8DS-		CP	5
PCRØ8L-	S	CD	5
PCRØ9-	S	A22	5
PCRØ9DS-		CR	5
PCRØ9L-	S	CC	5
PCRIØ-	S	A9	5
PCRIØDS-		CS	5
PCRIØL-	S	CB	5
PCRII-	S	A2Ø	5
PCRIIDS-		CT	5
PCRIIL-	S	CA	5
PCRDR-		B43	5
SCDCB		B16	IØ



BLOCK DIAGRAM

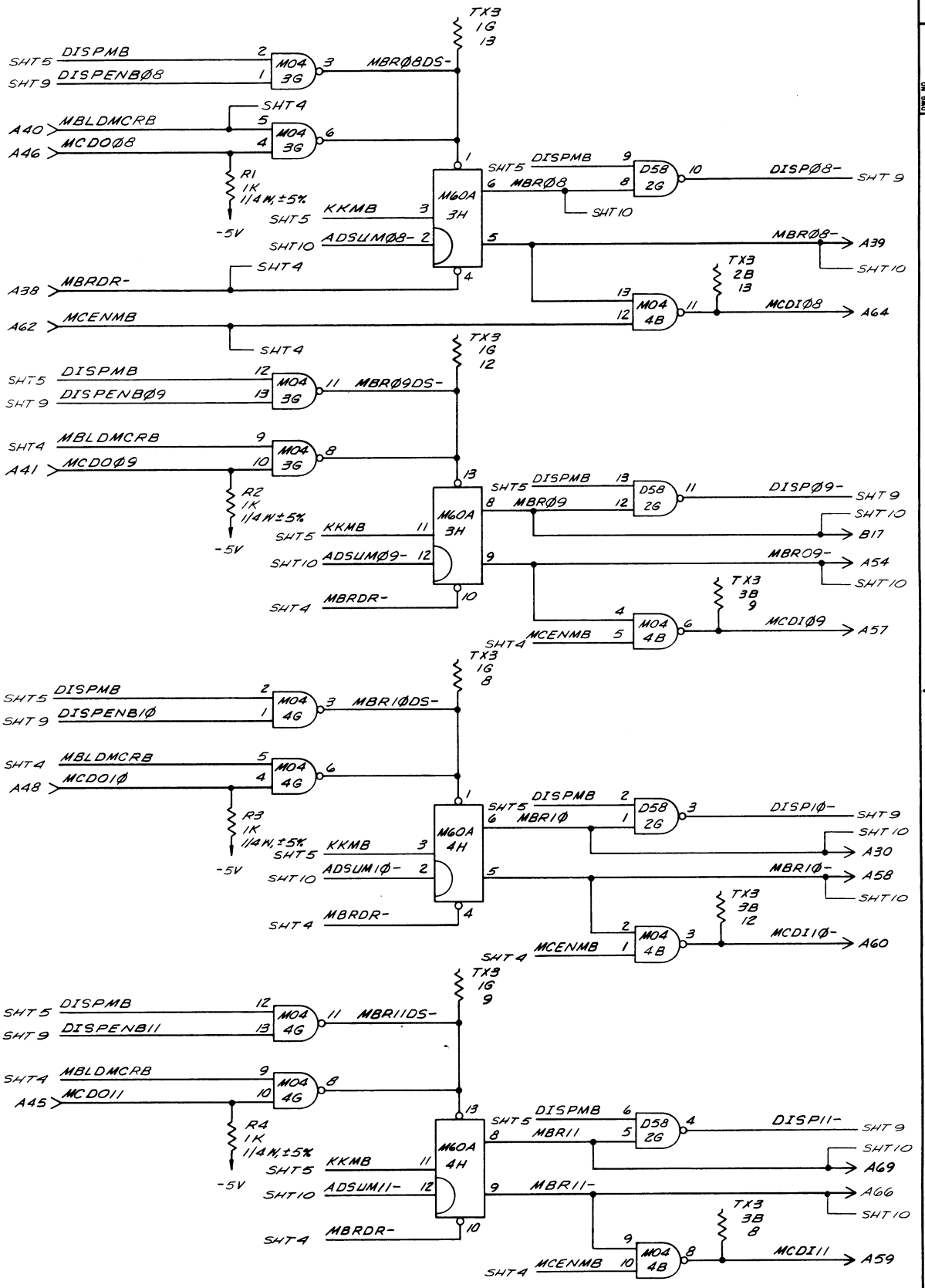
DWG NO. 545499 SHEET 3 OF

DWG NO. 545499 SHEET 3 OF

CODE IDENT NO	SIZE		REV
49956	D	545499	A
SCALE NONE		SHEET 3	

RAYTHEON COMPUTER FORM 67-0088

MEMORY BUFFER REGISTER (BITS Ø8-11)



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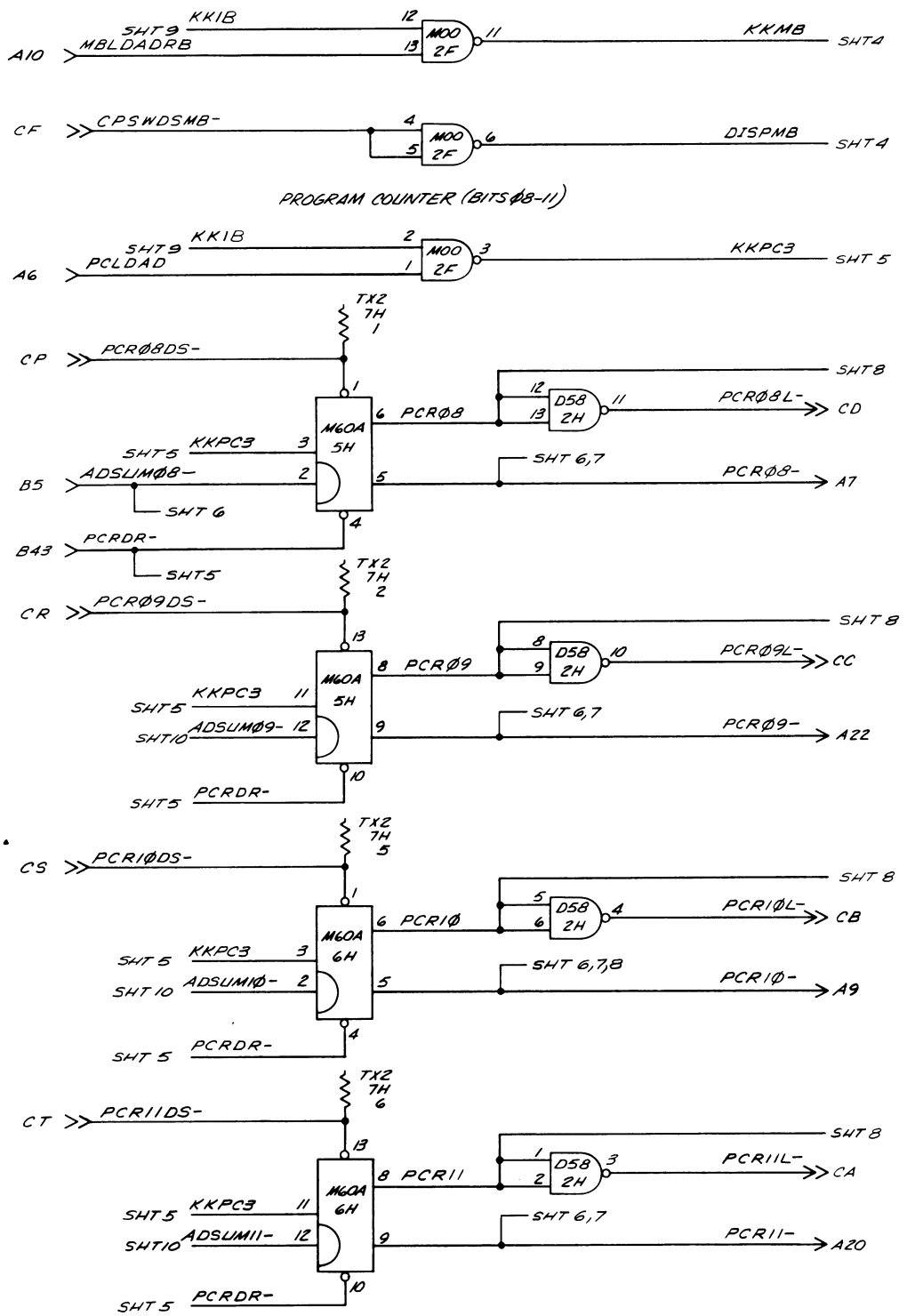
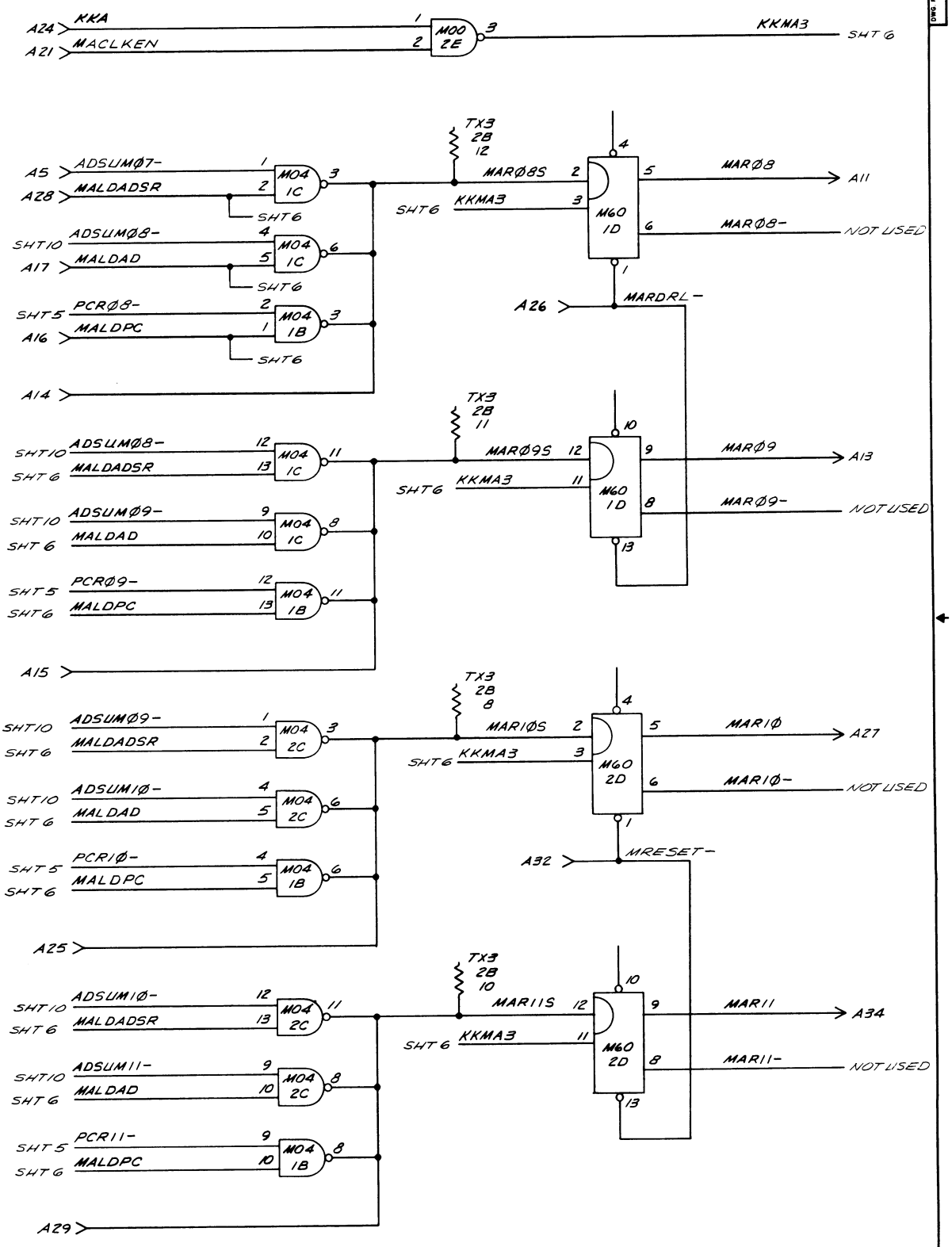
49956	D	545499	4
SCALE NONE		SHEET 4	

RAYTHEON COMPUTER FORM 57-0005


KKIB
SHT 9
MBLDADRB
A10
M00 2F
KKMB
SHT4
CF
CPSWDSMB-
DISPMB
PROGRAM COUNTER (BITS Ø8-11)
KKPC3
PCLDAD
A6
TX2 7H
CP
PCRØ8DS-
M60A 5H
PCRØ8
D58 2H
PCRØ8L-
CD
SHT 6,7
PCRØ8-
A7
B5
ADSUMØ8-
SHT 6
B43
PCRDR-
CR
PCRØ9DS-
PCRØ9
PCRØ9L-
CC
ADSUMØ9-
SHT10
PCRØ9-
A22
CS
PCRIØDS-
PCRIØ
PCRIØL-
CB
ADSUMIØ-
PCRIØ-
A9
CT
PCRIIDS-
PCRII
PCRIIL-
CA
ADSUMII-
PCRII-
A20

MEMORY ADDRESS REGISTER (BITS Ø8-11)



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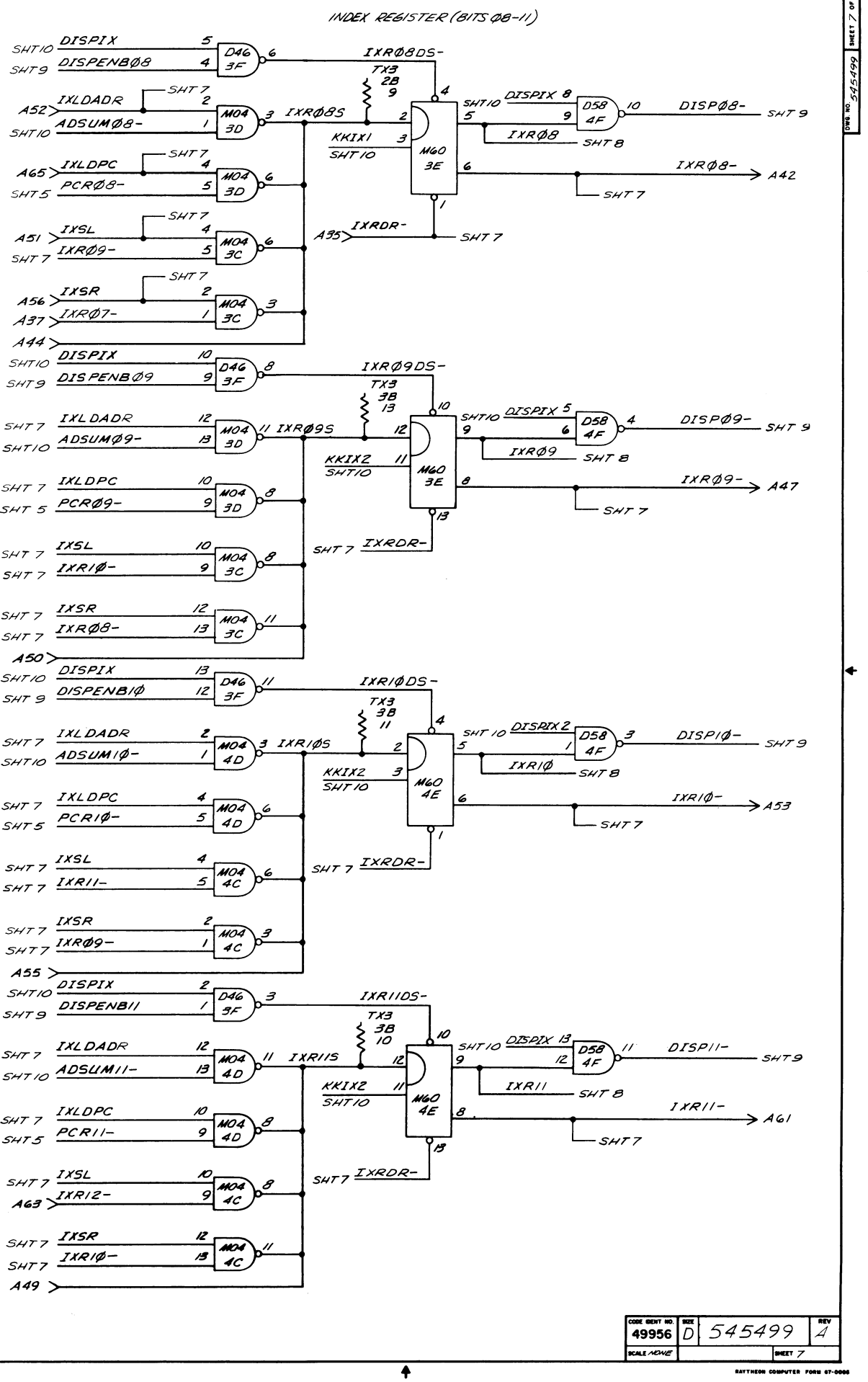
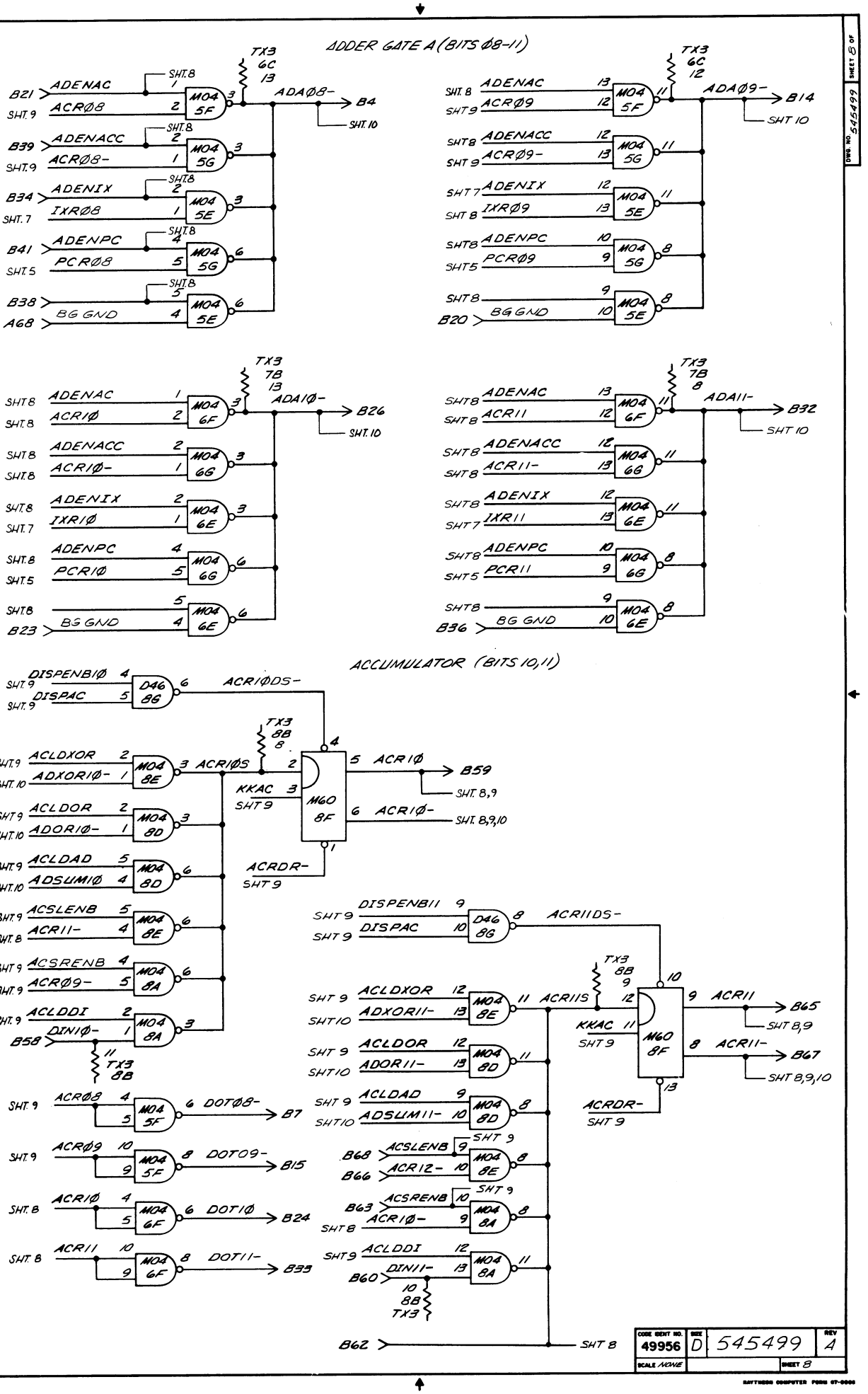
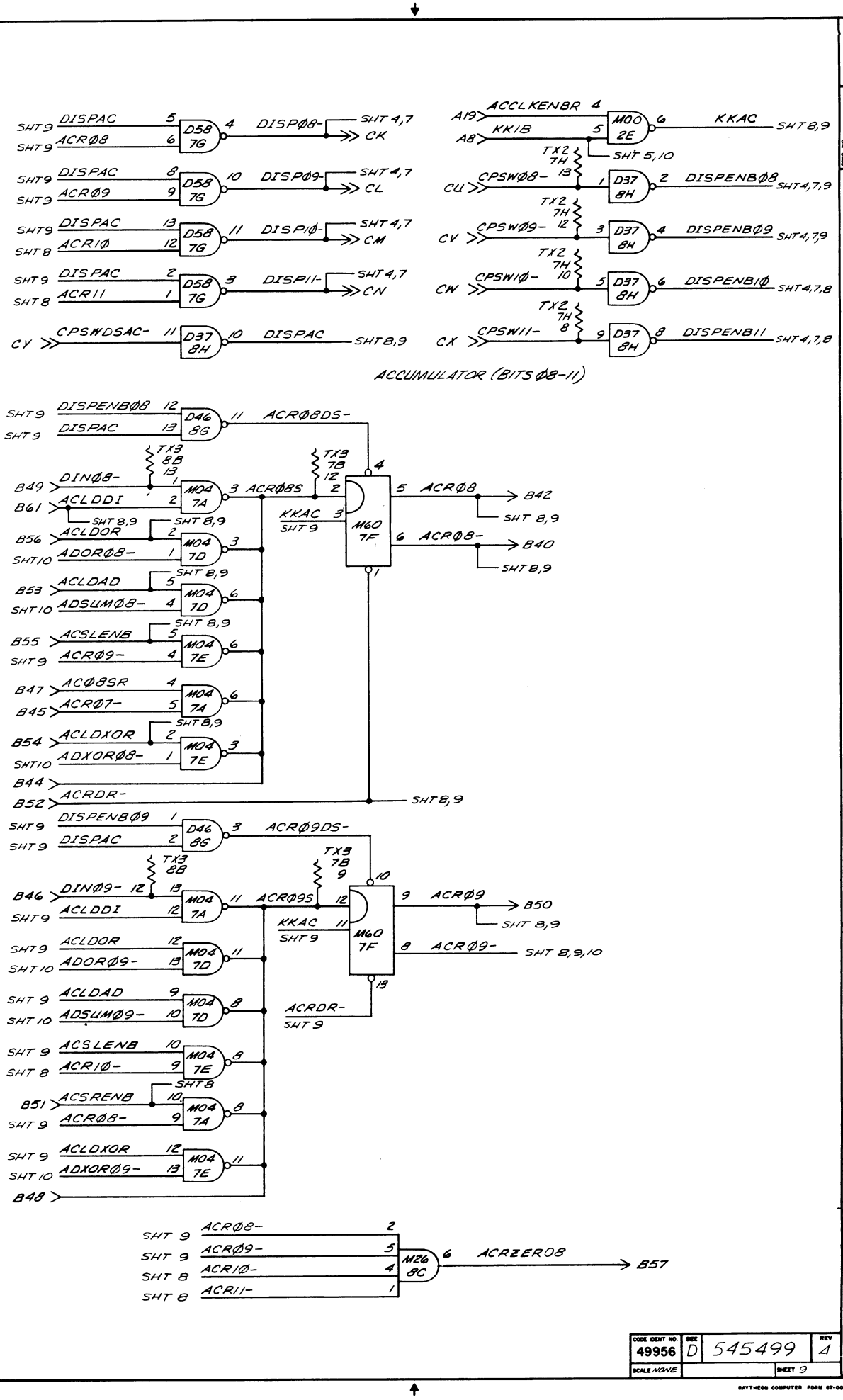
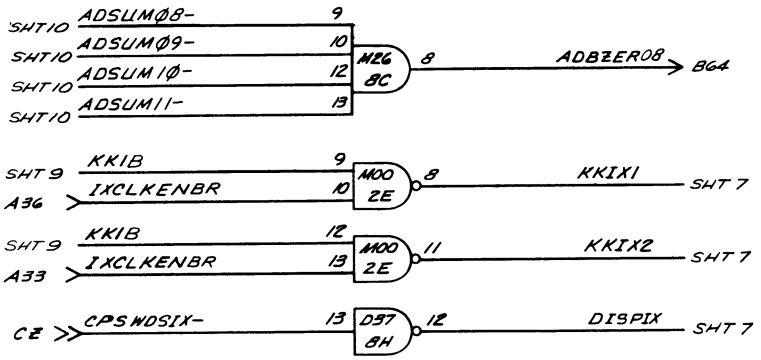
49956	D	545499	A
SCALE NONE		SHEET 6	

RAYTHEON COMPUTER FORM 67-0086

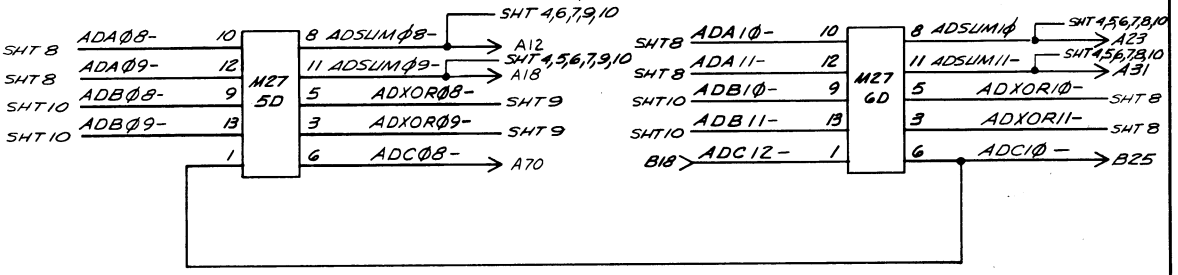

INDEX REGISTER (BITS Ø8-11)
DISPIX
DISPENBØ8
D46 3F
IXRØ8DS-
TX3 2B 9
IXLDADR
ADSUMØ8-
M04 3D
IXRØ8S
KKIX1
M60 3E
DISPIX 8
D58 4F
DISPØ8-
IXRØ8
IXRØ8-
A42
IXLDPC
PCRØ8-
IXRDR-
A35
IXSL
IXRØ9-
M04 3C
IXSR
IXRØ7-
A44
DISPENBØ9
IXRØ9DS-
TX3 3B 13
IXRØ9S
KKIX2
DISPIX 5
DISPØ9-
IXRØ9
IXRØ9-
A47
PCRØ9-
IXRIØ-
A50
DISPENBIØ
IXRIØDS-
TX3 3B 11
IXRIØS
DISPIX 2
DISPIØ-
IXRIØ
IXRIØ-
A53
PCRIØ-
IXRII-
A55
DISPENBII
IXRIIDS-
TX3 3B 10
IXRIIS
DISPIX 13
DISPII-
IXRII
IXRII-
A61
PCRII-
IXRI2-
A63
IXRIØ-
A49
SHT 10
SHT 9
SHT 7
SHT 5
SHT 8
A52
A65
A51
A56
A37
A90
A95
DWG NO 545499
SHEET 7 OF
CODE IDENT NO. 49956
SIZE D
545499
REV A
SCALE NONE
SHEET 7
RAYTHEON COMPUTER FORM 67-0006


ADDER GATE A (BITS Ø8-11)
ACCUMULATOR (BITS 10,11)
ADENAC
ACRØ8
ADENACC
ACRØ8-
ADENIX
IXRØ8
ADENPC
PCRØ8
BG GND
ADAØ8-
ACRØ9
ACRØ9-
IXRØ9
PCRØ9
ADAØ9-
ACRIØ
ACRIØ-
IXRIØ
PCRIØ
ADAIØ-
ACRII
ACRII-
IXRII
PCRII
ADAII-
DISPENBIØ
DISPAC
ACRIØDS-
ACLDXOR
ADXORIØ-
ACLDOR
ADORIØ-
ACLDAD
ADSUMIØ
ACSLENB
ACSRENB
ACLDDI
DINIØ-
ACRIØS
KKAC
ACRDR-
DOTØ8-
DOTØ9-
DOTIØ
DOTII-
DISPENBII
ACRIIDS-
ADXORII-
ADORII-
ADSUMII-
ACRIIS
ACRI2-
DINII-
B62
SHT 8
545499
D
49956
A

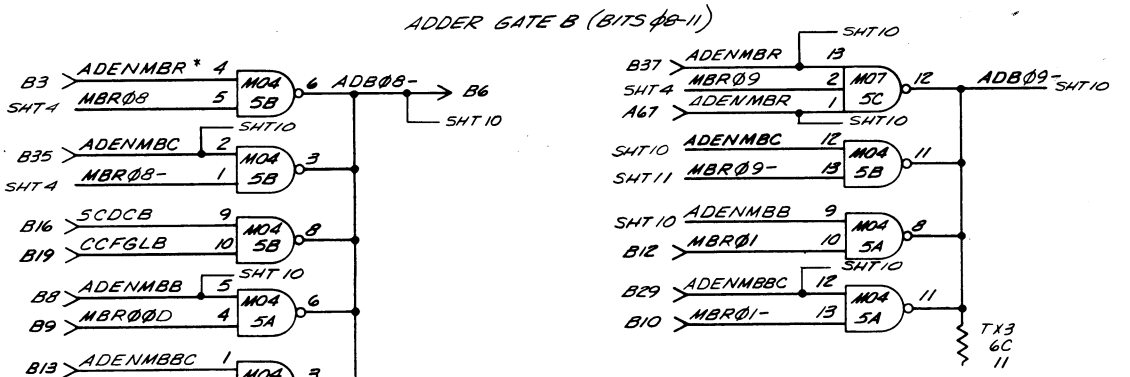

DWG NO 545499 SHEET 9 OF
SHT 9 DISPAC 5 D58 7G 4 DISPØ8- SHT 4,7 CK
SHT 9 ACRØ8 6
SHT 9 DISPAC 8 D58 7G 10 DISPØ9- SHT 4,7 CL
SHT 9 ACRØ9 9
SHT 9 DISPAC 13 D58 7G 11 DISPIØ- SHT 4,7 CM
SHT 8 ACRIØ 12
SHT 9 DISPAC 2 D58 7G 3 DISPII- SHT 4,7 CN
SHT 8 ACRII 1
CY CPSWDSAC- 11 D37 8H 10 DISPAC SHT 8,9
A19 ACCLKENBR 4
A8 KKIB M00 2E 5 6 KKAC SHT 8,9
SHT 5,10
TX2 7H
CU CPSWØ8- 13 D37 8H 1 2 DISPENBØ8 SHT 4,7,9
TX2 7H
CV CPSWØ9- 12 D37 8H 3 4 DISPENBØ9 SHT 4,7,9
TX2 7H
CW CPSWIØ- 10 D37 8H 5 6 DISPENBIØ SHT 4,7,8
TX2 7H
CX CPSWII- 8 D37 8H 9 8 DISPENBII SHT 4,7,8
ACCUMULATOR (BITS Ø8-11)
SHT 9 DISPENBØ8 12 D46 8G 11 ACRØ8DS-
SHT 9 DISPAC 13
TX3 8B
B49 DINØ8- 13 1
B61 ACLDDI 2 M04 7A 3 ACRØ8S
SHT 8,9
B56 ACLDOR 2 M04 7D 3
SHT 10 ADORØ8- 1
SHT 8,9
B53 ACLDAD 5 M04 7D 6
SHT 10 ADSUMØ8- 4
SHT 8,9
B55 ACSLENB 5 M04 7E 6
SHT 9 ACRØ9- 4
B47 ACØ8SR 4 M04 7A 6
B45 ACRØ7- 5
SHT 8,9
B54 ACLDXOR 2 M04 7E 3
SHT 10 ADXORØ8- 1
B44 ACRDR-
B52 SHT 8,9
TX3 7B 12
KKAC 3
SHT 9
M60 7F
2 4 5 ACRØ8 B42
SHT 8,9
6 ACRØ8- B40
SHT 8,9
1
SHT 9 DISPENBØ9 1 D46 8G 3 ACRØ9DS-
SHT 9 DISPAC 2
TX3 8B
B46 DINØ9- 12 13
SHT 9 ACLDDI 12 M04 7A 11 ACRØ9S
SHT 9 ACLDOR 12 M04 7D 11
SHT 10 ADORØ9- 13
SHT 9 ACLDAD 9 M04 7D 8
SHT 10 ADSUMØ9- 10
SHT 9 ACSLENB 10 M04 7E 8
SHT 8 ACRIØ- 9
SHT 8
B51 ACSRENB 10 M04 7A 8
SHT 9 ACRØ8- 9
SHT 9 ACLDXOR 12 M04 7E 11
SHT 10 ADXORØ9- 13
B48
TX3 7B 9
KKAC 11
SHT 9
M60 7F
10 9 ACRØ9 B50
SHT 8,9
8 ACRØ9- SHT 8,9,10
13
ACRDR-
SHT 9
SHT 9 ACRØ8- 2
SHT 9 ACRØ9- 5
SHT 8 ACRIØ- 4 M26 8C 6 ACRZERO8 B57
SHT 8 ACRII- 1
DWG NO 545499 SHEET 9 OF
CODE IDENT NO. 49956
SIZE D
545499
REV A
SCALE NONE
SHEET 9
RAYTHEON COMPUTER FORM 67-0006

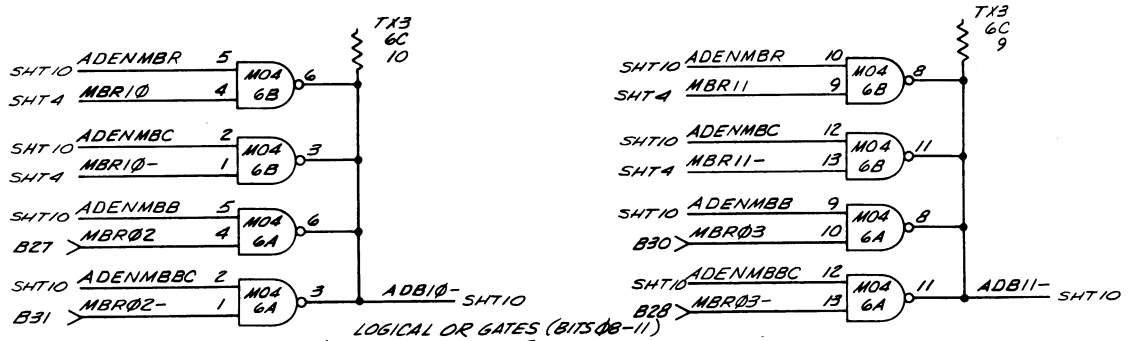


ADDER (BITS Ø8-11)

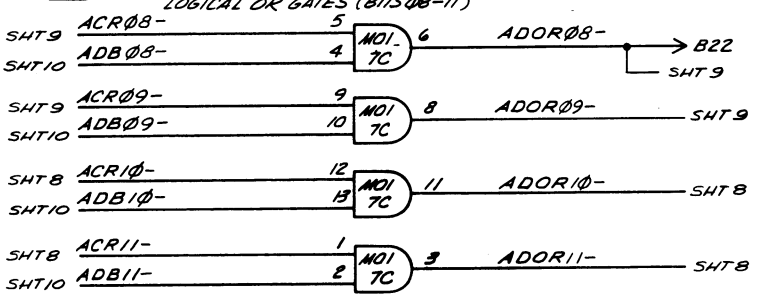


ADDER GATE B (BITS Ø8-11)

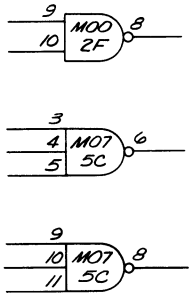


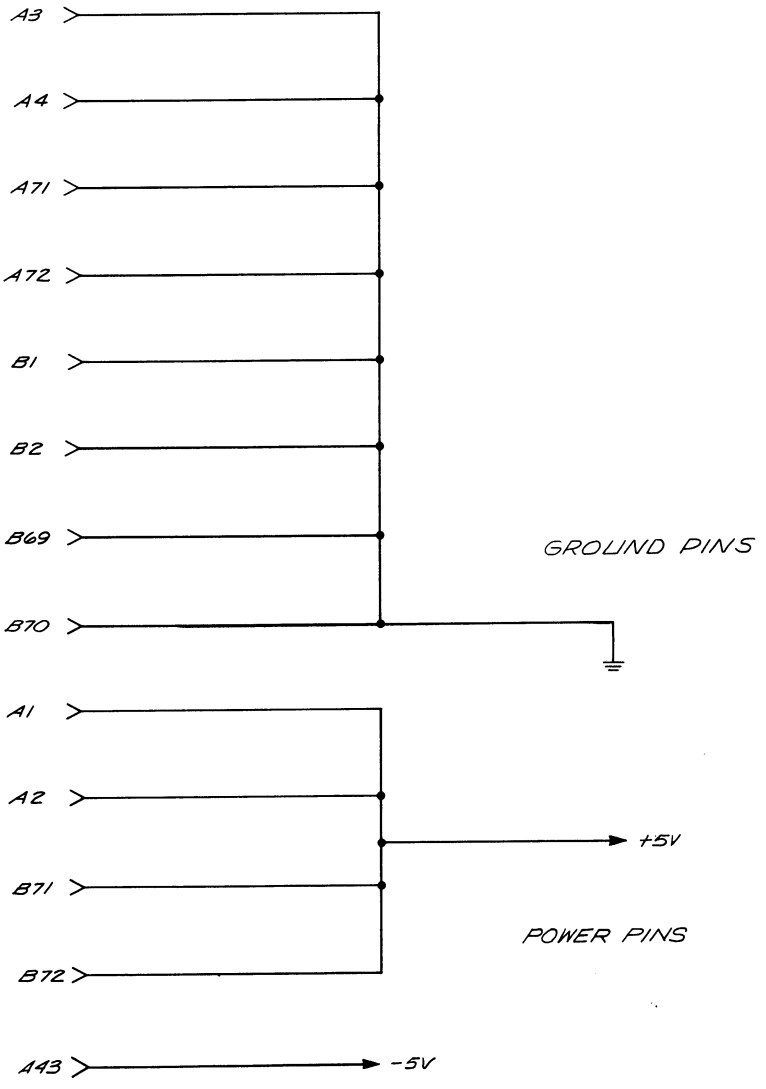


LOGICAL OR GATES (BITS Ø8-11)



UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	545499	A
SCALE NONE			SHEET 11

RAYTHEON COMPUTER FORM 67-0085

RESERVE EO'S OUTSTANDING	REVISIONS								
	SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	X1	APPROVAL PER E.O.20470			MCS	???	[illegible]	3/6/70
	X2	REVISED PER EO 20750			MD	???	???	5/13/70
	A	RELEASED PER EO/9311			MCS	???	???	9/21/70

SHEET 1 OF 11

DWG NO. 545500

TABLE OF CONTENTS

GLOSSARY

ACCLKENBR	ACCUMULATOR RIGHT BYTE CLOCK ENABLE
ACLDAD	ACCUMULATOR LOAD FROM THE ADDER
ACLDDI	ACCUMULATOR LOAD FROM DIRECT INPUT OUTPUT CHANNEL
ACLDOR	ACCUMULATOR LOAD FROM ADDER OR
ACLDXOR	ACCUMULATOR LOAD FROM ADDER EXCLUSIVE OR
ACRDR	ACCUMULATOR DIRECT RESET
ACRXX	ACCUMULATOR BIT XX
ACRXXS	ACCUMULATOR BIT XX SET TERM
ACRZERO12	ACCUMULATOR BIT 12-15 ARE ZERO
ACSLENB	ACCUMULATOR SHIFT LEFT ENABLE
ACSRENB	ACCUMULATOR SHIFT RIGHT ENABLE
ADAXX	ADDER GATE A BIT XX
ADBXX	ADDER GATE B BIT XX
ADBZERO12	ADDER SUM BITS 12-15 ARE ZERO
ADCXX	ADDER CARRY BIT XX
ADENAC	ADDER ENABLED FROM ACCUMULATOR
ADENACC	ADDER ENABLED FROM ACCUMULATOR COMPLEMENT
ADENIX	ADDER ENABLED FROM INDEX REGISTER
ADENMBB	ADDER ENABLE FROM MEMORY BUFFER REGISTER
ADENMBBC	ADDER ENABLE FROM MEMORY BUFFER REGISTER BYTE COMPLEMENT
ADENMBC	ADDER ENABLE FROM MEMORY BUFFER COMPLEMENT
ADENMBR	ADDER ENABLE FROM MEMORY BUFFER RIGHT BYTE
ADENPC	ADDER ENABLED FROM PROGRAM COUNTER
ADINCRY	ADDER CARRY INPUT
ADORXX	ADDER OR BIT XX
ADSUMXX	ADDER SUM BIT XX
ADXORXX	ADDER EXCLUSIVE OR BIT XX
BPGND	BACKPLANE GROUND PER UNUSED GATE
CPSWDSAC	CONTROL PANEL SWITCH DISPLAY ACCUMULATOR
CPSWDSIX	CONTROL PANEL SWITCH DISPLAY INDEX REGISTER
CPSWDSMB	CONTROL PANEL SWITCH DISPLAY MEMORY BUFFER
CPSWXX	CONTROL PANEL DATA SWITCH BIT XX
DINXX	DIRECT INPUT CHANNEL BIT XX
DISPENBXX	CONTROL PANEL DATA SWITCH BIT XX INVERTED
DISPXX	CONTROL PANEL DISPLAY BIT XX
DOTXX	DIRECT OUTPUT CHANNEL BIT XX
IXCLKENBR	INDEX REGISTER CLOCK ENABLE RIGHT
IXLDADR	INDEX REGISTER LOAD FROM ADDER RIGHT BYTE
IXLDPC	INDEX REGISTER LOAD FROM PROGRAM COUNTER
IXRDR	INDEX REGISTER DIRECT RESET
IXRXX	INDEX REGISTER BIT XX
IXRXXS	INDEX REGISTER BIT XX SET TERM
IXSL	INDEX REGISTER SHIFT LEFT
IXSLZRO	ZEROS IXR15 ON SHIFT LEFT DOUBLE
IXSR	INDEX REGISTER SHIFT RIGHT
KK2	GATED SYSTEM CLOCK
KKB	UNGATED SYSTEM CLOCK
MACLKEN	MEMORY ADDRESS REGISTER CLOCK ENABLE
MALDAD	MEMORY ADDRESS REGISTER LOAD FROM ADDER
MALDADSR	MEMORY ADDRESS REGISTER LOAD FROM ADDER SHIFTED RIGHT ONE BIT
MALDPC	MEMORY ADDRESS REGISTER LOAD FROM PROGRAM COUNTER
MARXX	MEMORY ADDRESS REGISTER BIT XX
MARXXS	MEMORY ADDRESS REGISTER BIT XX SET TERM
MBLDADRB	MEMORY BUFFER LOAD FROM ADDER RIGHT BYTE
MBLDMCRB	MEMORY BUFFER LOAD FROM MEMORY RIGHT BYTE
MBRDR	MEMORY BUFFER REGISTER DIRECT RESET
MBRXX	MEMORY BUFFER REGISTER BIT XX
MCDIXX	MEMORY DATA INPUT BIT XX
MCDOXX	MEMORY DATA OUTPUT BIT XX
MCENMB	MEMORY DATA IN ENABLED FROM MEMORY BUFFER
MRESET	MASTER RESET
PCLDAD	PROGRAM COUNTER LOAD FROM ADDER
PCRDR	PROGRAM COUNTER DIRECT RESET
PCRXX	PROGRAM COUNTER REGISTER BIT XX
PCRXXDS	PROGRAM COUNTER BIT XX DIRECT SET

TABLE 1	
I.C. DESIGNATION	RAYTHEON PART NUMBER
D37	531531-001
D46	531147-001
D58	531522-001
M00	531593-006
M01	531593-005
M04	531593-014
M07	531593-015
M26	531593-012
M27	531595-001
M60/M60A	531593-018
TX2	531596-001
TX3	531596-002

3. THE FOLLOWING PINS ARE TIED TO GROUND ON "C" CONNECTOR. C1 THRU C22

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. →» DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11
REVISION	A	A	A	A	A	A	A	A	A	A	A

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN	M. Segal	3-11-70
CHECK	M. Brodsky	3/17/70
APPR	Baetz	3/20/70
APPR	Call	3/17/70

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NEXT ASSY

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

ARITHMATIC CARD, 1
LOGIC DIAGRAM

CODE IDENT NO.	SIZE	
49956	D	545500
SCALE NONE		SHEET 1 OF 11

DWG NO. 545500 SHEET 11 OF 11

RAYTHEON COMPUTER FORM 67-0084

SIGNAL LIST

SIGNAL	SOURCE	CONN	SHEET
ACCLKENBR		A19	9
ACLDAD		B53	9
ACLDDI		B61	9
ACLDOR		B56	9
ACLDXOR		B54	9
ACR11-		B45	9
ACR12	S	B42	9
ACR12-	S	B40	9
ACR12S	S	B44	9
ACR13	S	B50	9
ACR13S	S	B48	9
ACR14	S	B59	8
ACR15	S	B65	8
ACR15-	S	B67	8
ACR15S	S	B62	8
ACRDR-		B52	9
ACRZERO12	S	B57	9
ACSLENB		B55	9
ACSRENB		B47	9
ACSRENB		B63	8
ACSRENB		B51	9
ADA12-	S	B4	8
ADA13-	S	B14	8
ADA14-	S	B26	8
ADA15-	S	B32	8
ADB12-	S	B6	10
ADBZERO12	S	B64	10
ADC12-	S	A70	10
ADC14-	S	B25	10
ADENAC		B21	8
ADENACC		B39	8
ADENIX		B34	8
ADENMBB		B8	10
ADENMBBC		B29	10
ADENMBBC		B13	10
ADENMBC		B35	10
ADENMBR		B3	10
ADENMBR		B37	10
ADENMBR		A67	10
ADENPC	S	B41	8
ADINCRY		B18	10
ADOR12-	S	B22	10
ADSUM11-		A5	6
ADSUM12-		B5	5
ADSUM12-	S	A12	10
ADSUM13-	S	A18	10
ADSUM14-	S	A23	10
ADSUM15-	S	A31	10
BPGND		B36	8
BPGND		B23	8
BPGND		B20	8
BPGND		A68	8
BPGND		B66	8
BPGND		B19	10
CPSWI2-		CU	9
CPSWI3-		CV	9
CPSWI4-		CW	9
CPSWI5-		CX	9
CPSWDSIX-		CZ	10
CPSWDSMB-		CF	5
CPSWDSAC-		CY	9
DIN12-		B49	9
DIN13-		B46	9
DIN14-		B58	8
DIN15-		B60	8
DISPI2-	S	CK	9
DISPI3-	S	CL	9
DISPI4-	S	CM	9
DISPI5-	S	CN	9
DOT12-	S	B7	8
DOT13-	S	B15	8
DOT14-	S	B24	8
DOT15-	S	B33	8
IXCLKENBR		A33	10
IXCLKENBR		A36	10

SIGNAL LIST

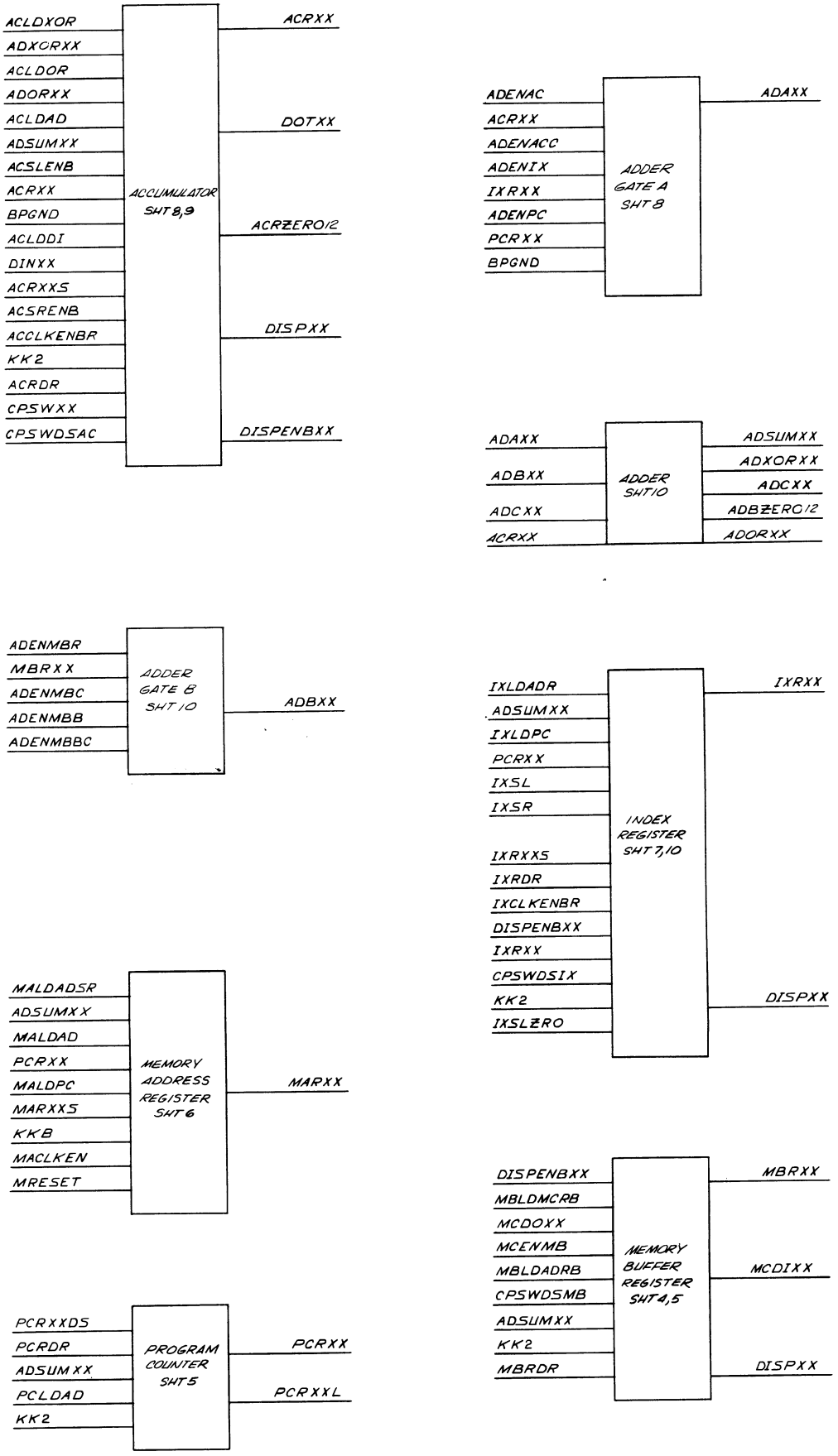
SIGNAL	SOURCE	CONN	SHEET
IXLDADR		A52	7
IXLDPC	S	A65	7
IXR11-		A37	7
IXR12-	S	A42	7
IXR12S	S	A44	7
IXR13-	S	A47	7
IXR13S	S	A50	7
IXR14-	S	A53	7
IXR14S	S	A55	7
IXR15-	S	A61	7
IXR15S	S	A49	7
IXRDR-	S	A35	7
IXSL	S	A51	7
IXSLZRO		A63	7
IXSR		A56	7
KK2		A8	9
KKB		A24	6
MACLKEN		A21	6
MALDAD		A17	6
MALDADSR		A28	6
MALDPC		A16	6
MAR12	S	A11	6
MAR13	S	A13	6
MAR13S	S	A15	6
MAR14	S	A27	6
MAR14S	S	A25	6
MAR15	S	A34	6
MAR15S	S	A29	6
MAR2S	S	A14	6
MBLDADRB		A10	5
MBLDMCRB		A40	4
MBR04-		B11	10
MBR12-	S	A39	4
MBR04B		B9	10
MBR13	S	B17	4
MBR05-		B10	10
MBR13-	S	A54	4
MBR05		B12	10
MBR14	S	A30	4
MBR06-		B31	10
MBR14-	S	A58	4
MBR07-		B28	10
MBR15	S	A69	4
MBR06		B27	10
MBR15-	S	A66	4
MBR07		B30	10
MBRDR-		A38	4
MCDI12	S	A64	4
MCDI13	S	A57	4
MCDI14	S	A60	4
MCDI15	S	A59	4
MCDO12		A46	4
MCDO13		A41	4
MCDO14		A48	4
MCDO15		A45	4
MCENMB		A62	4
MRESET-		A32	6
MRESET-		A26	6
PCLDAD		A6	5
PCR12-	S	A7	5
PCR12DS-		CP	5
PCR12L-	S	CD	5
PCR13-	S	A22	5
PCR13DS-		CR	5
PCR13L-	S	CC	5
PCR14-	S	A9	5
PCR14DS-		CS	5
PCR14L-	S	CB	5
PCR15-	S	A20	5
PCR15DS-		CT	5
PCR15L-		CA	5
PCRDR-		B43	5

DWG NO 545500 SHEET 2 OF

DWG NO 545500 SHEET 2 OF

CODE IDENT NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 2	

RAYTHEON COMPUTER FORM 67-0086



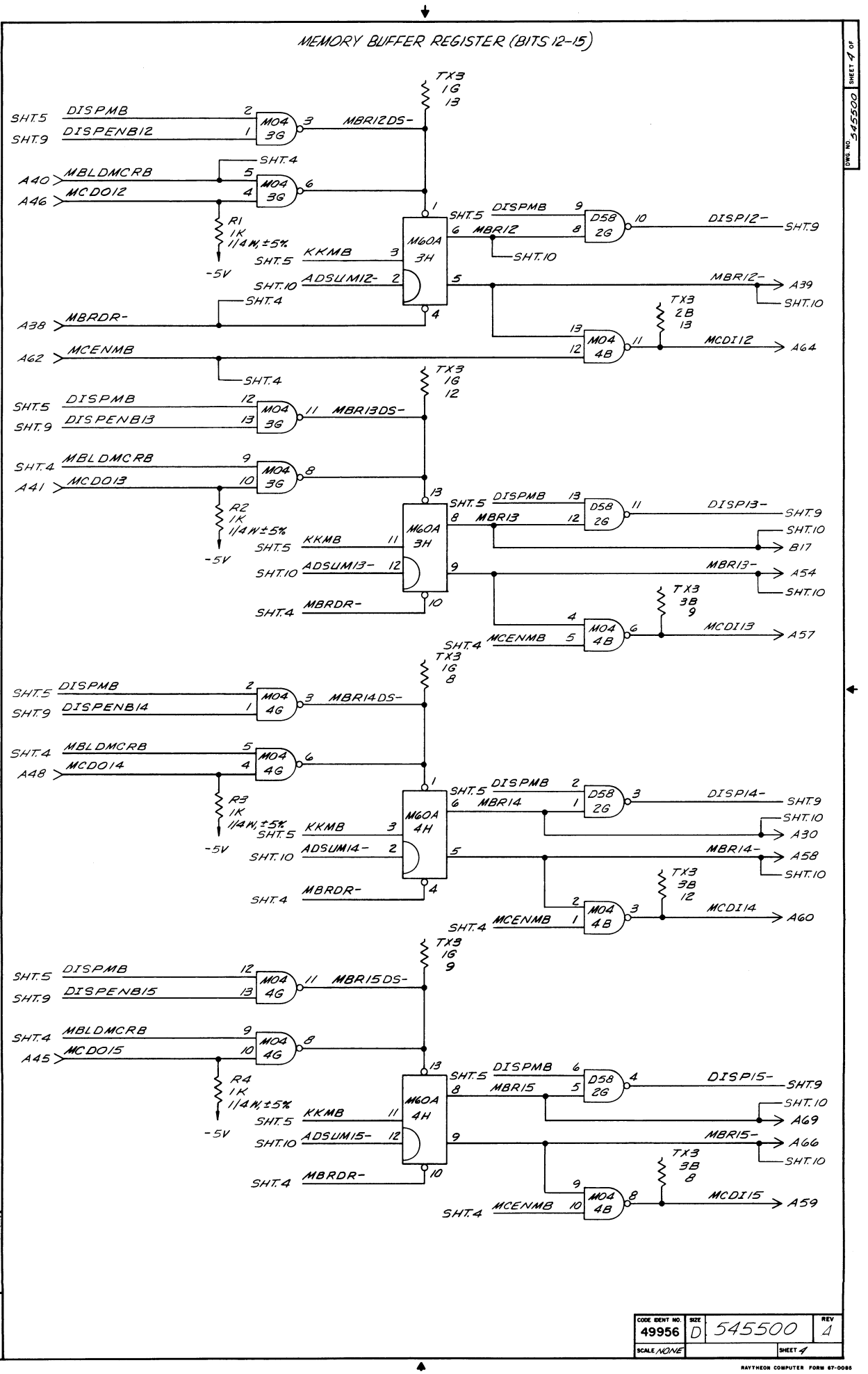
BOARD DIAGRAM

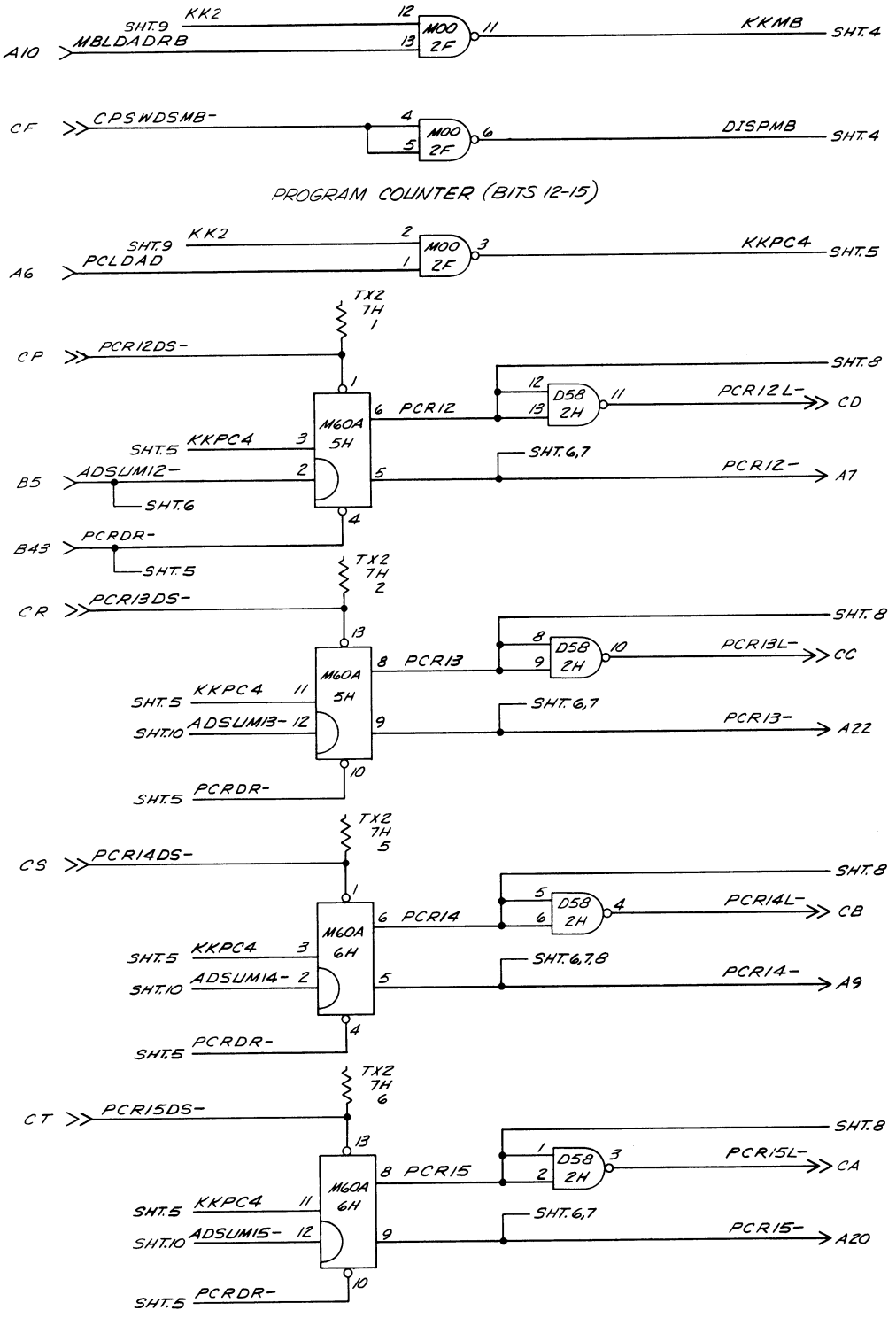
DWG. NO. 545500 SHEET 3 OF

DWG. NO. 545500 SHEET 3 OF

CODE IDENT NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 3	

RAYTHEON COMPUTER FORM 67-0068

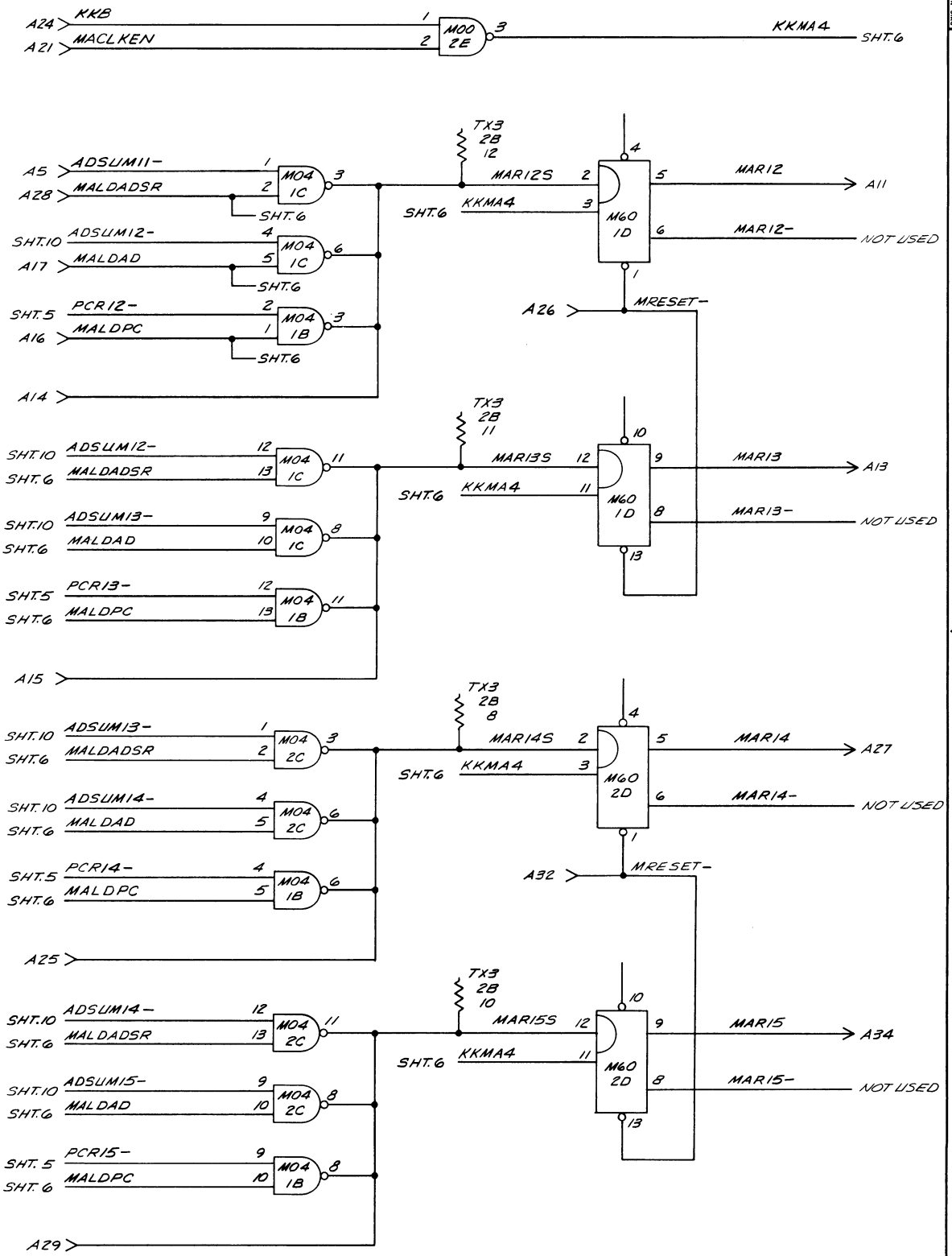

MEMORY BUFFER REGISTER (BITS 12-15)
DWG. NO. 545500 SHEET 4 OF
TX3 1G 13
SHT.5 DISPMB
SHT.9 DISPENB12
M04 3G
MBR12DS-
SHT.4
A40 MBLDMCRB
A46 MCDO12
R1 1K 1/4W, ±5%
-5V
M60A 3H
KKMB
ADSUM12-
SHT.5
SHT.10
MBR12
SHT.10
D58 2G
DISP12-
SHT.9
MBR12-
A39
SHT.10
A38 MBRDR-
TX3 2B 13
M04 4B
MCDI12
A64
A62 MCENMB
TX3 1G 12
SHT.5 DISPMB
SHT.9 DISPENB13
MBR13DS-
SHT.4 MBLDMCRB
A41 MCDO13
R2 1K 1/4W ±5%
MBR13
DISP13-
SHT.9
SHT.10
B17
ADSUM13-
MBR13-
A54
SHT.10
TX3 3B 9
MCDI13
A57
MCENMB
TX3 1G 8
SHT.5 DISPMB
SHT.9 DISPENB14
MBR14DS-
SHT.4 MBLDMCRB
A48 MCDO14
R3 1K 1/4W, ±5%
MBR14
DISP14-
SHT.9
SHT.10
A30
ADSUM14-
MBR14-
A58
SHT.10
TX3 3B 12
MCDI14
A60
MCENMB
TX3 1G 9
SHT.5 DISPMB
SHT.9 DISPENB15
MBR15DS-
SHT.4 MBLDMCRB
A45 MCDO15
R4 1K 1/4W, ±5%
MBR15
DISP15-
SHT.9
SHT.10
A69
ADSUM15-
MBR15-
A66
SHT.10
TX3 3B 8
MCDI15
A59
MCENMB
DWG. NO. 545500 SHEET 4 OF
CODE IDENT NO. 49956
SIZE D
545500
REV 4
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0085



CODE IDENT NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 5	

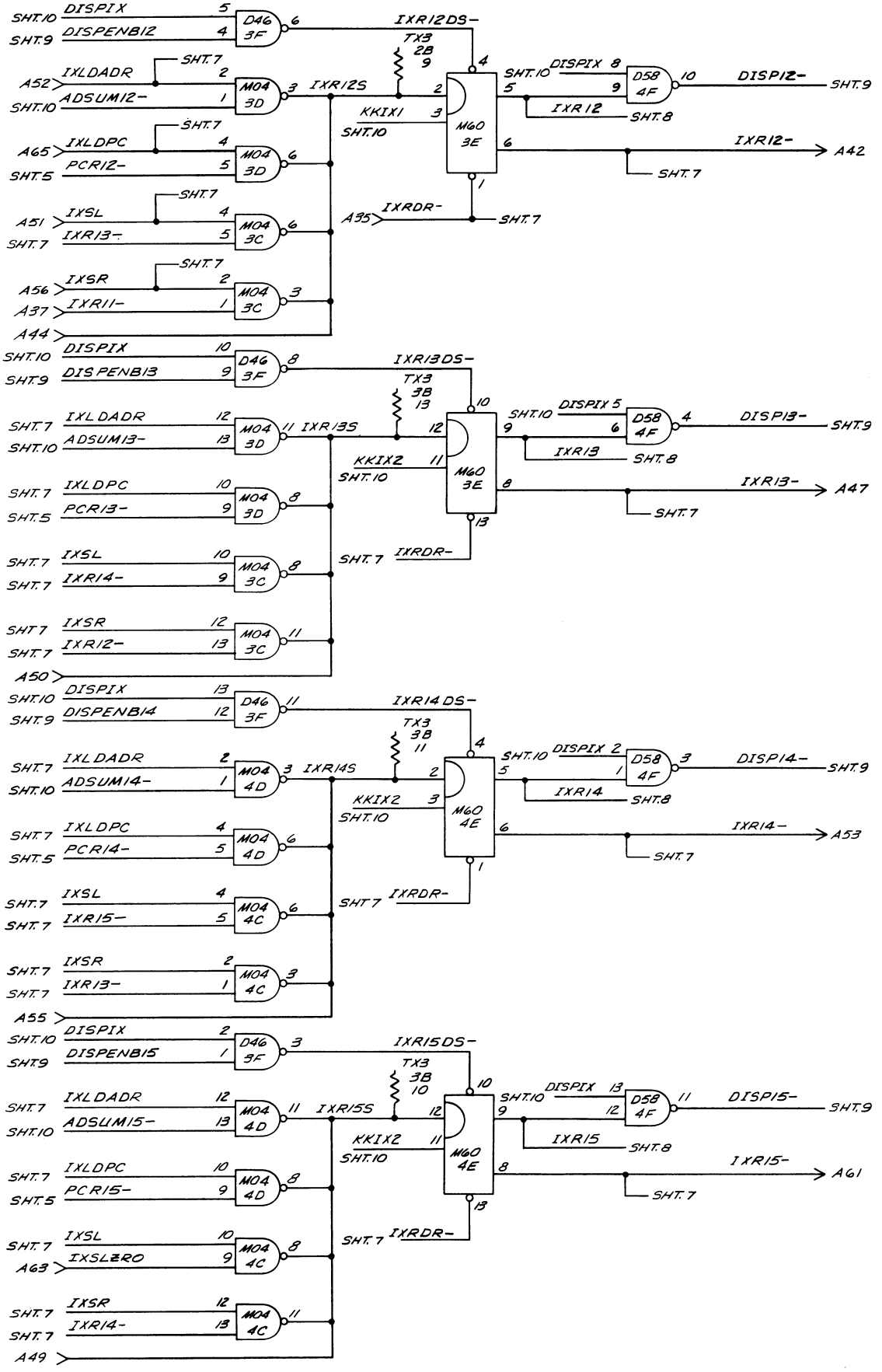
RAYTHEON COMPUTER FORM 67-0086

MEMORY ADDRESS REGISTER (BITS 12-15)



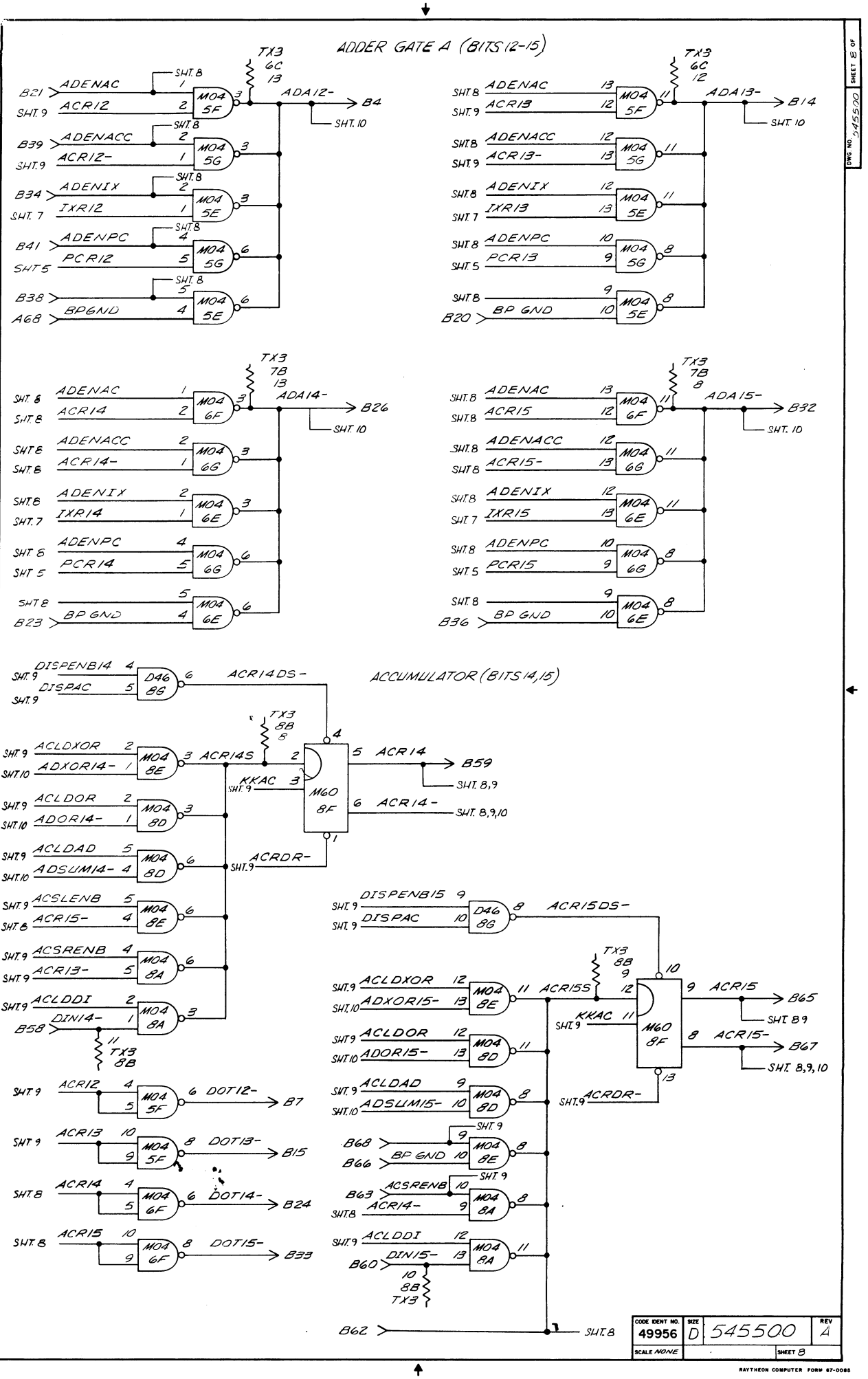
CODE IDENT NO	SIZE		REV
49956	D	545500	A
SCALE NONE			SHEET 6

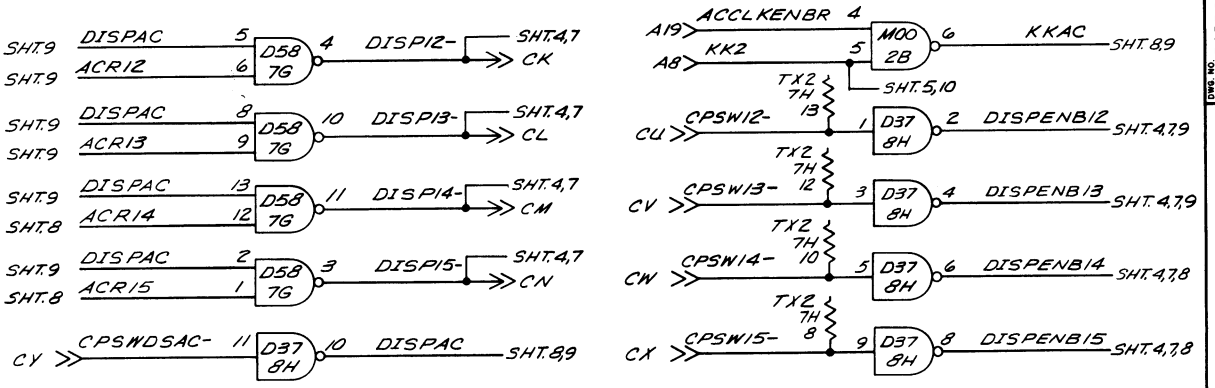
INDEX REGISTER (BITS 12-15)



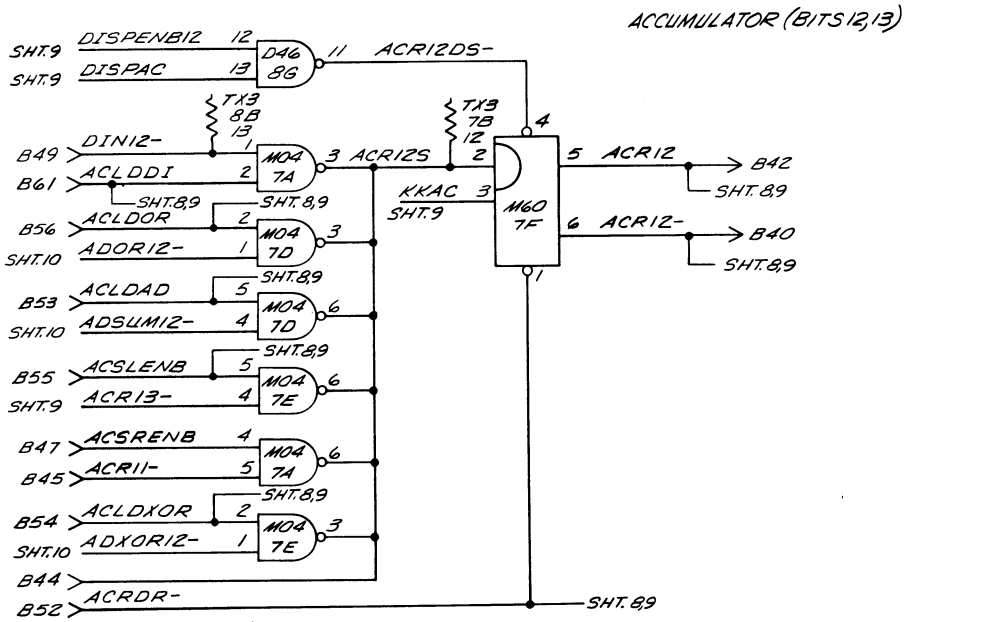
CODE IDENT. NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 7	

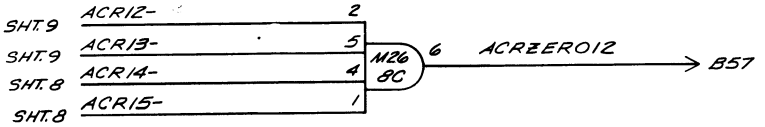
RAYTHEON COMPUTER FORM 67-0088


ADDER GATE A (BITS 12-15)
ACCUMULATOR (BITS 14,15)
ADENAC
ACR12
ADENACC
ACR12-
ADENIX
IXR12
ADENPC
PCR12
BPGND
ADA12-
ADENAC
ACR13
ADENACC
ACR13-
ADENIX
IXR13
ADENPC
PCR13
BP GND
ADA13-
ADENAC
ACR14
ADENACC
ACR14-
ADENIX
IXR14
ADENPC
PCR14
BP GND
ADA14-
ADENAC
ACR15
ADENACC
ACR15-
ADENIX
IXR15
ADENPC
PCR15
BP GND
ADA15-
DISPENB14
DISPAC
ACR14DS-
ACLDXOR
ADXOR14-
ACLDOR
ADOR14-
ACLDAD
ADSUM14-
ACSLENB
ACR15-
ACSRENB
ACR13-
ACLDDI
DIN14-
ACR14S
KKAC
ACRDR-
ACR14
ACR14-
DISPENB15
DISPAC
ACR15DS-
ACLDXOR
ADXOR15-
ACLDOR
ADOR15-
ACLDAD
ADSUM15-
BP GND
ACSRENB
ACR14-
ACLDDI
DIN15-
ACR15S
KKAC
ACRDR-
ACR15
ACR15-
ACR12
ACR13
ACR14
ACR15
DOT12-
DOT13-
DOT14-
DOT15-
B7
B15
B24
B33
B59
B65
B67
B26
B32
B58
B60
B62
B66
B68
B20
B21
B34
B36
B38
B39
B41
A68
B23
B63
TX3 6C 13
TX3 6C 12
TX3 7B 13
TX3 7B 8
TX3 8B 8
TX3 8B 9
TX3 8B
M04 5F
M04 5G
M04 5E
M04 6F
M04 6G
M04 6E
M04 8E
M04 8D
M04 8A
M60 8F
D46 8G
SHT. 8
SHT. 9
SHT. 10
SHT. 7
SHT. 5
SHT. 8,9
SHT. 8,9,10
DWG. NO. 545500
SHEET 8 OF
CODE IDENT NO. 49956
SIZE D
545500
REV A
SCALE NONE
SHEET 8
RAYTHEON COMPUTER FORM 67-0088

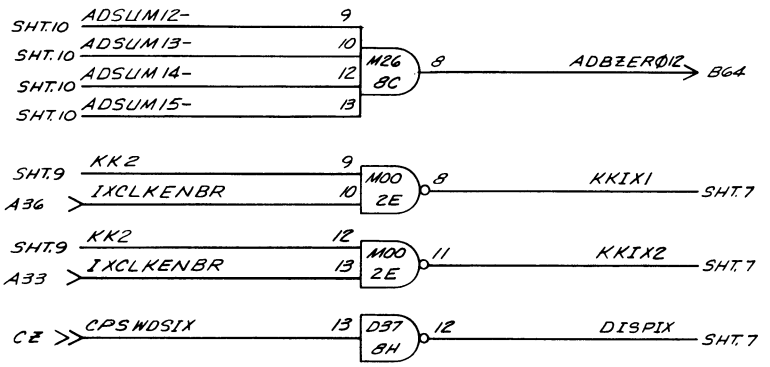


ACCUMULATOR (BITS 12,13)

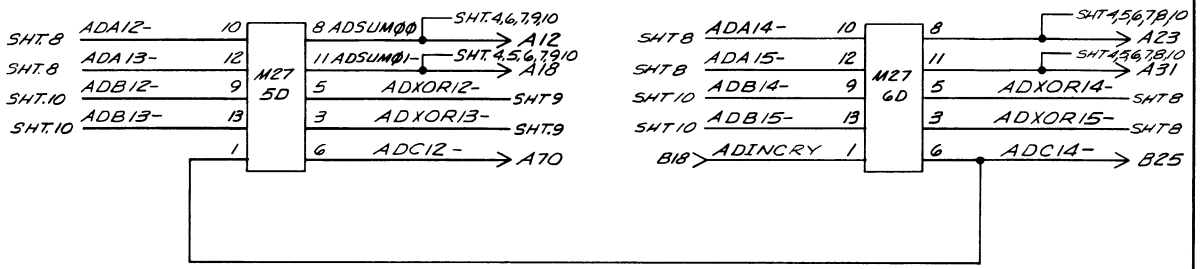




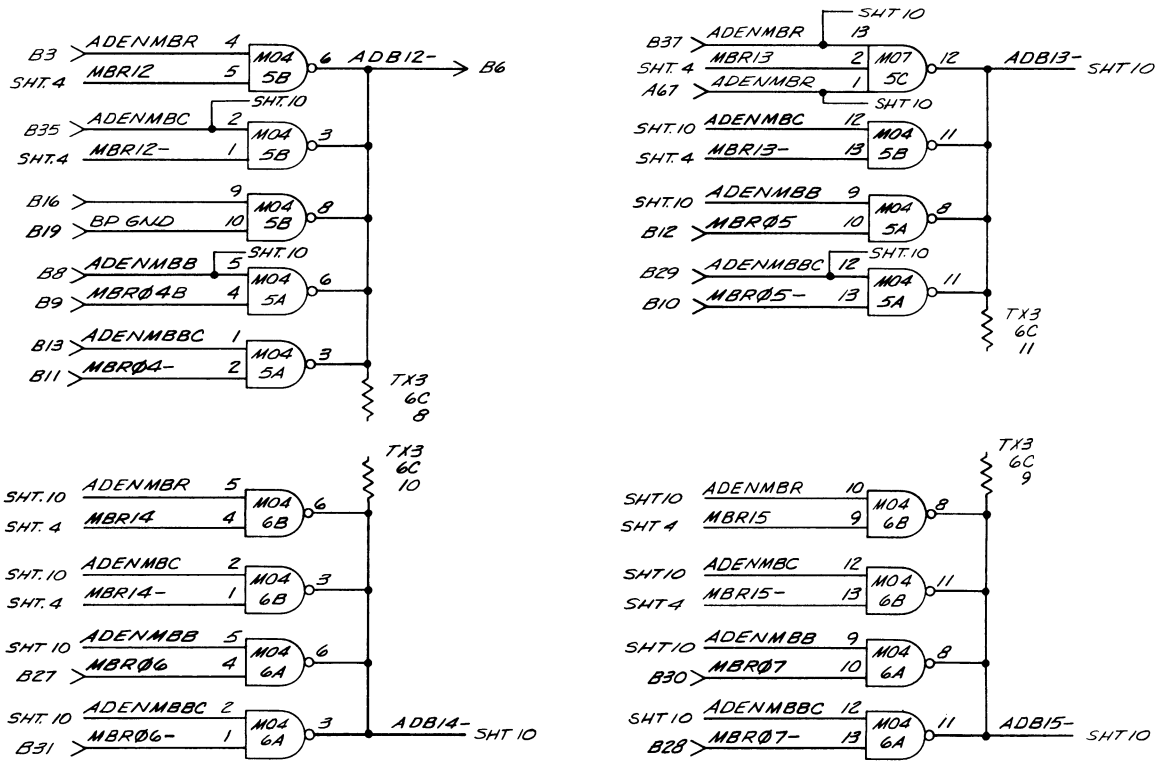
CODE IDENT NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 9	



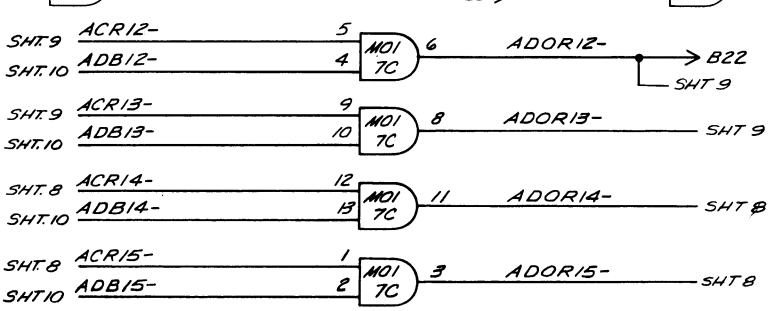
ADDER (BITS 12-15)



ADDER GATE B (BITS 12-15)



LOGICAL OR GATE (BITS 12-15)



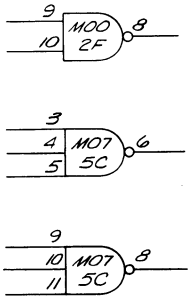
DWG. NO. 545500 SHEET 10 OF

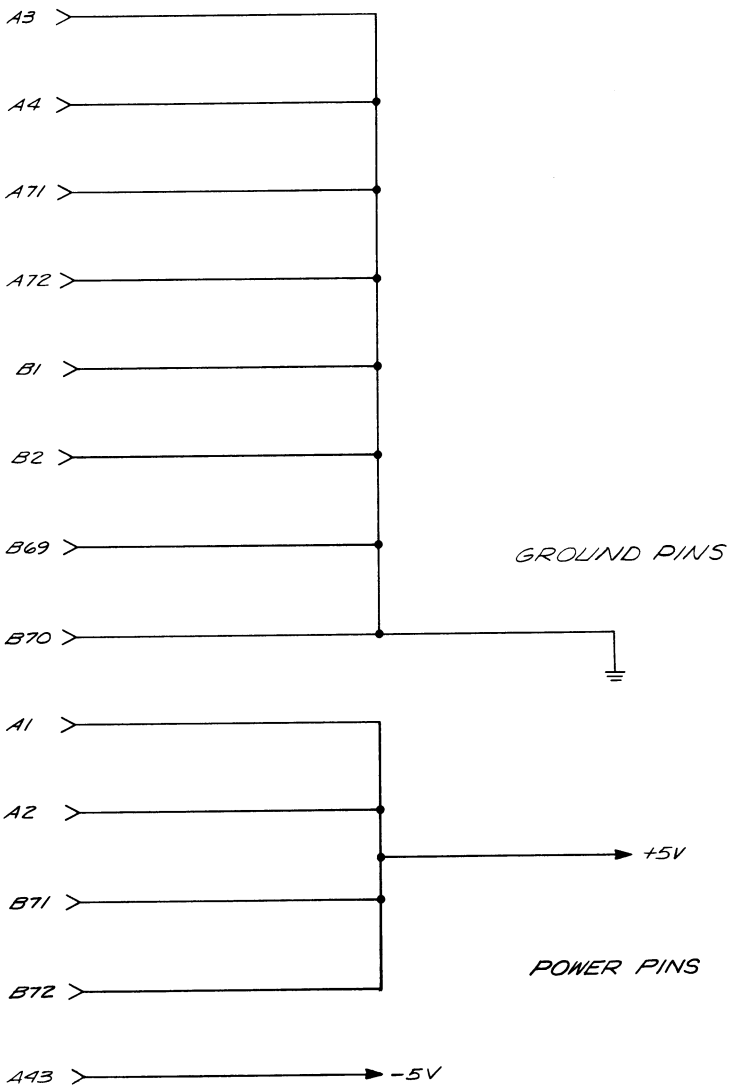
DWG. NO. 545500 SHEET 10 OF

CODE IDENT NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 10	

RAYTHEON COMPUTER FORM 67-0088

UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956	D	545500	A
SCALE NONE		SHEET 11	

RAYTHEON COMPUTER FORM 67-0085

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER E.O. 20922		✓	F.E	M.S	R.Ed	9/17
X2	REVISED PER E.O. 20744		✓	[illegible]	M.B	M.B	9/1/70
A	RELEASED PER EO. 19311			W.P.	M.B	M.S	8/21/70

SHEET 1 OF 12

DWG. NO. 545541

TABLE OF CONTENTS

GLOSSARY

CPSWRST	RESET SWITCH SIGNAL
INTRPTXX	INTERRUPT SIGNAL XX
ITØXRQ	INTERRUPT REQUEST SIGNAL X
ITI5AXX	INTERRUPT INHIBIT SIGNAL XX
ITI5RQ	INTERRUPT REQUEST SIGNAL 15
ITACTA	PLACE REQUESTING INTERRUPT LEVEL INTO ACTIVE STATE
ITDSBA	DISABLE ADDRESSED INTERRUPT LEVEL
ITENBA	ENABLE ADDRESSED INTERRUPT LEVEL
ITIDLA	RETURN ADDRESS INTERRUPT LEVEL TO IDLE STATE
ITLVDCXX	DECODED INTERRUPT LEVEL ADDRESS XX
ITMBRI2	MEMORY BUFFER SLIP SHOT POWERED
ITQXXXX	INTERRUPT REQUIEST SIGNAL XXXX
ITRØXA	INTERRUPT ACTIVE REGISTER FLIP-FLOP X
ITRØXN	INTERRUPT ENABLE REGISTER FLIF-FLOP X
ITRSVXX	INTERRUPT SERVICE REGISTER BIT XX
ITSVENB	ENABLE INTERRUPT SERVICE
KKCX	CLOCK
MBRXX	MEMORY BUFFER REGISTER FLIP-FLOP XX
TIR2CØ	TØ TIME INTERVAL

TABLE I

I.C. DESIGNATION	RAYTHEON PART NUMBER
DEC	531667-001
M00	531593-006
M01	531593-005
M02	531593-007
M03	531593-008
M05	531593-004
M06	531593-017
M10	531593-002
M26	531593-012
M60A	531593-018
M61	531593-011
TX2	531596-001
TX3	531596-002

2. JUMPERS; SHOWN BY SOLID LINES ARE THE MOST USED CONFIGURATION; SHOWN BY DASHED LINES ARE OPTIONS

1. ⋙ DENOTES FRONT PANEL CONNECTOR
   → DENOTES I/O CONNECTOR

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET	1	2	3	4	5	6	7	8	9	10	11	12						
REVISION	A	A	A	A	A	A	A	A	A	A	A	A						

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.05, .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .030 MAX
FINISH:

DRAWN	F. ROLDAN	4-9-70
CHECK	[illegible]	9/10/70
APPR	[illegible]	9/17/70
APPR		

NEXT ASSY N/A

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

PRIORITY INTERRUPT CARD, 08-15 (LOGIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE D | 545541

SCALE NONE | SHEET 1 OF 12

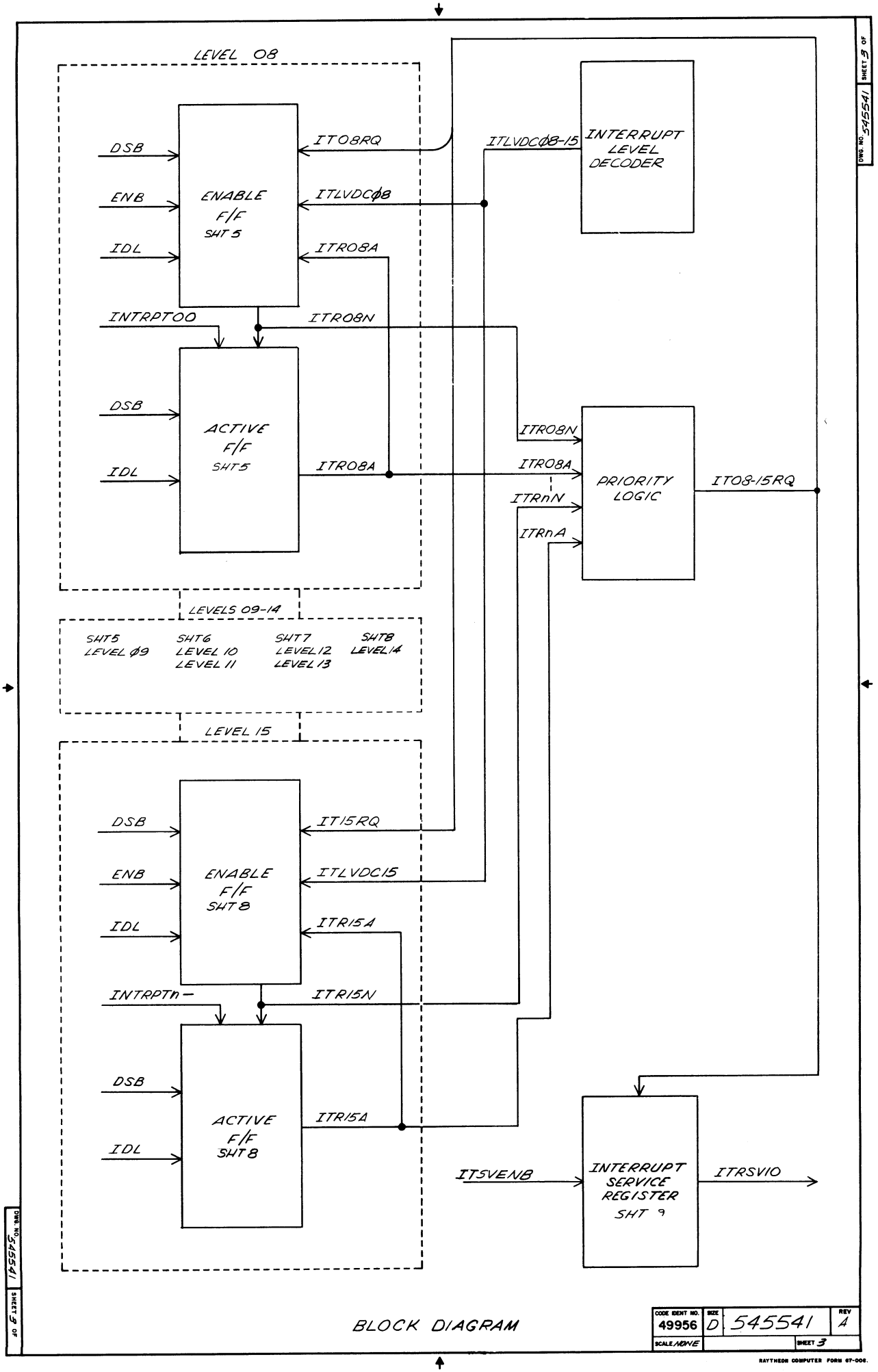
RAYTHEON COMPUTER FORM 67-046

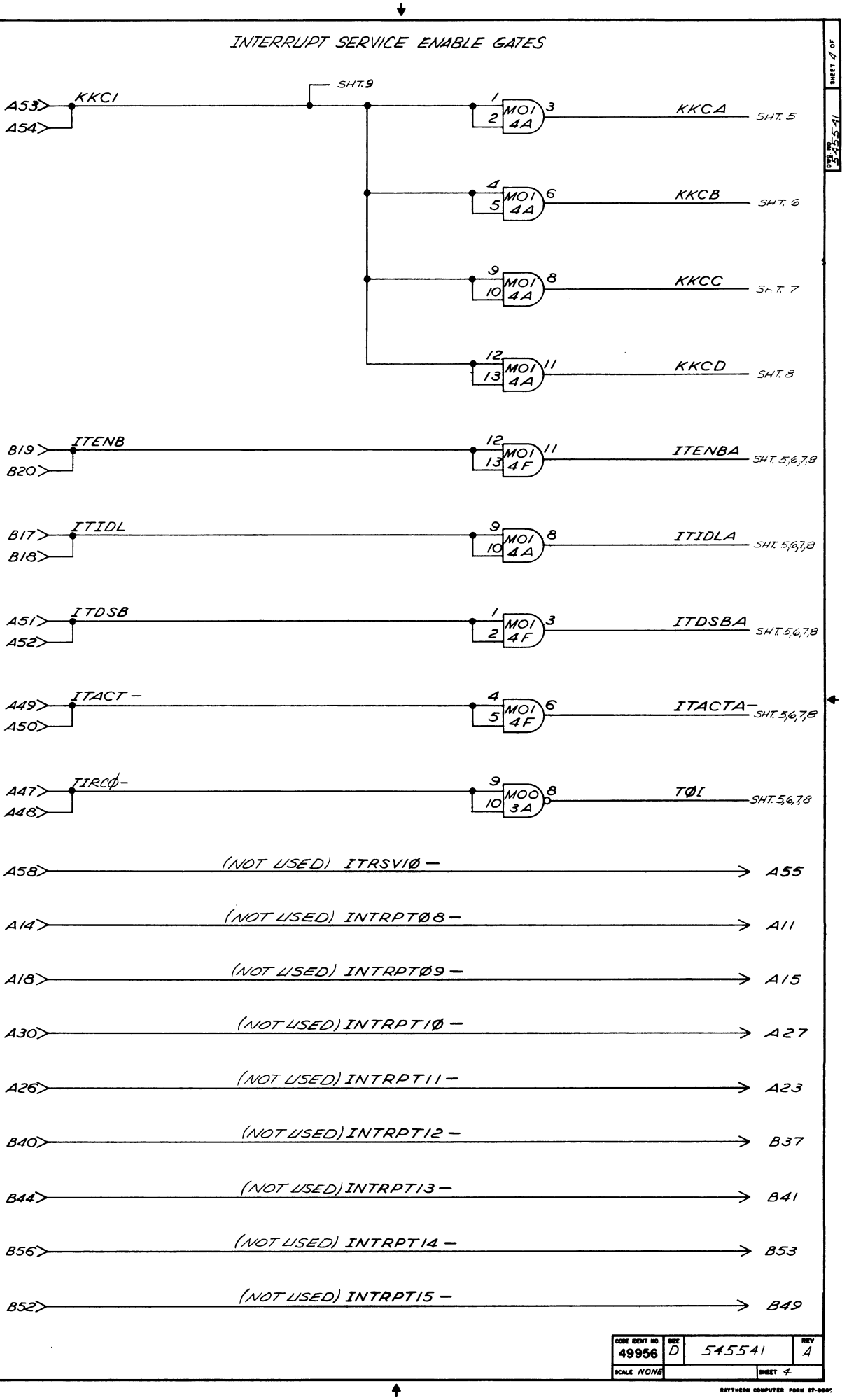
DWG. NO. 545541 SHEET 1 OF 12

SIGNAL LIST

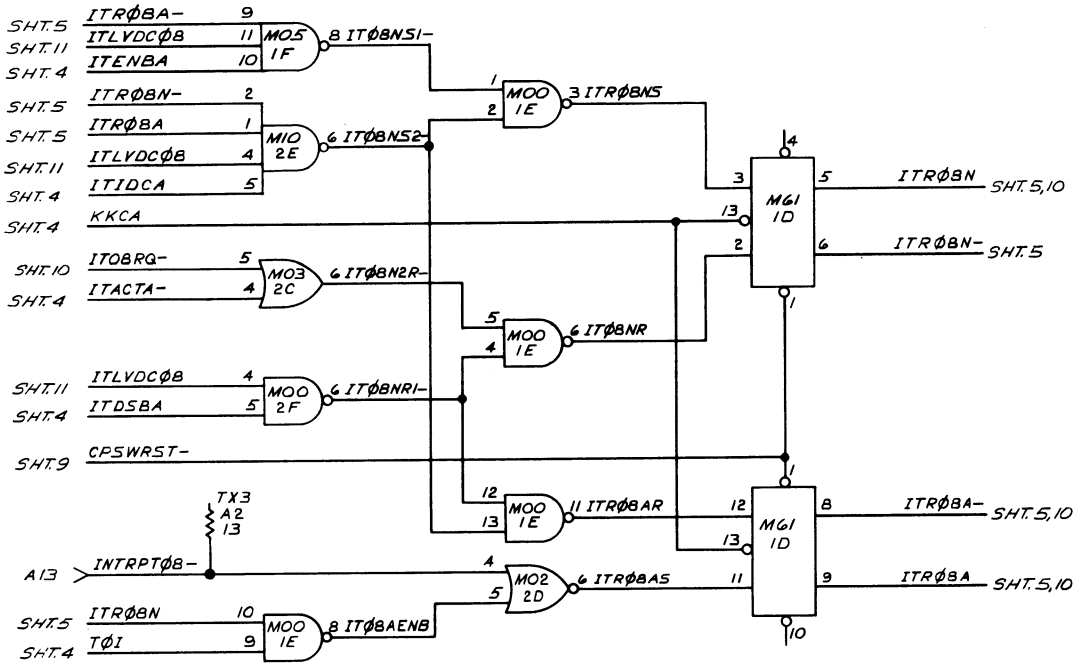
SIGNAL	SOURCE	CONN	SHEET
CPSWRST-	S	A7,A8	9
INTRPTØ8-		A13	5
INTRPTØ9-		A17	5
INTRPTIØ-		A29	6
INTRPTII-		A25	6
INTRPTI2-		B39	7
INTRPTI3-		B43	7
INTRPTI4-		B55	8
INTRPTI5-		B51	8
ITØ8RQ-	S	B11	1Ø
IT15AØ8-	S	B21	1Ø
IT15AØ9-	S	A5	1Ø
ITACT-		A49,A50	4
ITDSB		A51,A52	4
ITENB		B19,B20	4
ITIDL		B17,B18	4
ITMBRI2		A43	11
ITQ9D-	S	A63	9
ITQAE-	S	B61	9
ITQBF-	S	A65	9
ITQC-	S	B9	9
ITQCDEF-	S	B7,B8	9
ITRSVIØ-	S	A57	9
ITSVENB		A45,A46	9
KKC1		A53,A54	4
MBRI3-		B3,B4	11
MBRI4-		A67,A68	11
MBRI5-		A69,A70	4
TIRCØ-		A47,A48	4

CODE IDENT NO.	SIZE		REV
49956	D	545541	A
SCALE NONE		SHEET 2	

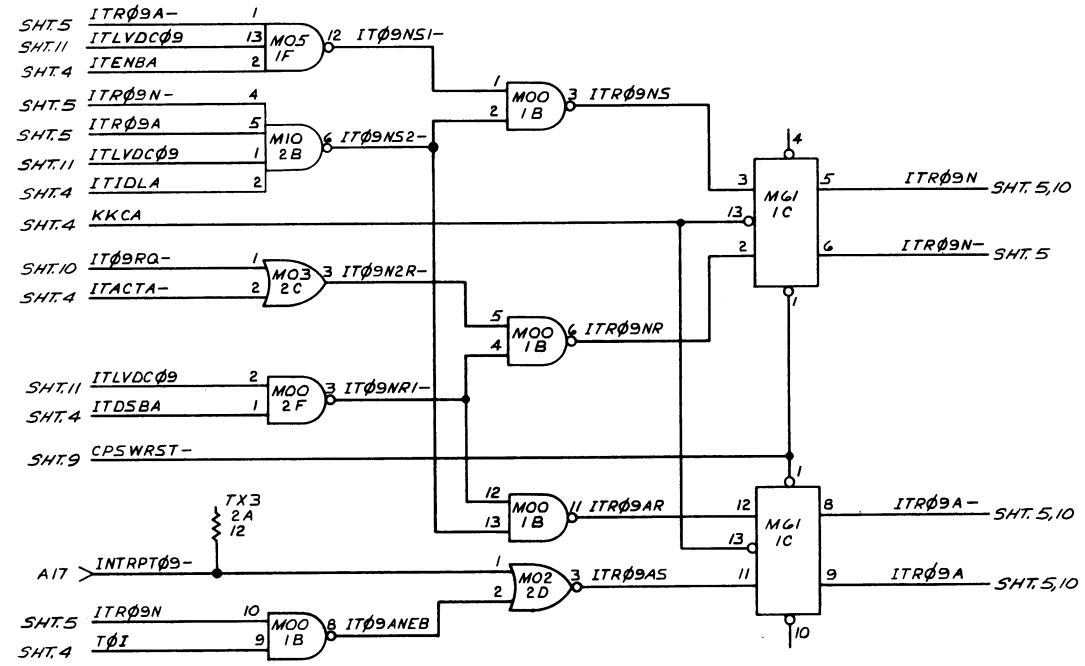

LEVEL 08
DSB
ENB
IDL
ENABLE F/F SHT 5
IT08RQ
ITLVDCØ8
ITR08A
INTRPT00
ITR08N
DSB
IDL
ACTIVE F/F SHT5
ITR08A
ITLVDCØ8-15
INTERRUPT LEVEL DECODER
ITR08N
ITR08A
ITRnN
ITRnA
PRIORITY LOGIC
IT08-15RQ
LEVELS 09-14
SHT5 LEVEL Ø9
SHT6 LEVEL 10 LEVEL 11
SHT7 LEVEL 12 LEVEL 13
SHT8 LEVEL 14
LEVEL 15
DSB
ENB
IDL
ENABLE F/F SHT 8
IT15RQ
ITLVDC15
ITR15A
INTRPTn
ITR15N
DSB
IDL
ACTIVE F/F SHT 8
ITR15A
IT5VENB
INTERRUPT SERVICE REGISTER SHT 9
ITRSVIO
DWG. NO. 545541
SHEET 3 OF
BLOCK DIAGRAM
CODE IDENT NO. 49956
SIZE D
545541
REV A
SCALE NONE
SHEET 3
RAYTHEON COMPUTER FORM 67-006.


INTERRUPT SERVICE ENABLE GATES
SHT. 9
A53
A54
KKCI
1
2
MOI 4A
3
KKCA
SHT. 5
4
5
MOI 4A
6
KKCB
SHT. 6
9
10
MOI 4A
8
KKCC
SHT. 7
12
13
MOI 4A
11
KKCD
SHT. 8
B19
B20
ITENB
12
13
MOI 4F
11
ITENBA
SHT. 5,6,7,8
B17
B18
ITIDL
9
10
MOI 4A
8
ITIDLA
SHT. 5,6,7,8
A51
A52
ITDSB
1
2
MOI 4F
3
ITDSBA
SHT. 5,6,7,8
A49
A50
ITACT –
4
5
MOI 4F
6
ITACTA –
SHT. 5,6,7,8
A47
A48
IIRCØ –
9
10
MOO 3A
8
TØI
SHT. 5,6,7,8
A58
(NOT USED) ITRSVIØ –
A55
A14
(NOT USED) INTRPTØ8 –
A11
A18
(NOT USED) INTRPTØ9 –
A15
A30
(NOT USED) INTRPT1Ø –
A27
A26
(NOT USED) INTRPT11 –
A23
B40
(NOT USED) INTRPT12 –
B37
B44
(NOT USED) INTRPT13 –
B41
B56
(NOT USED) INTRPT14 –
B53
B52
(NOT USED) INTRPT15 –
B49
SHEET 4 OF
DWG NO. 545541
SHEET 4 OF
DWG NO. 545541
CODE IDENT NO. 49956
SIZE D
545541
REV A
SCALE NONE
SHEET 4
RAYTHEON COMPUTER FORM 67-0005

LEVEL Ø8 SERVICE FLIP-FLOPS

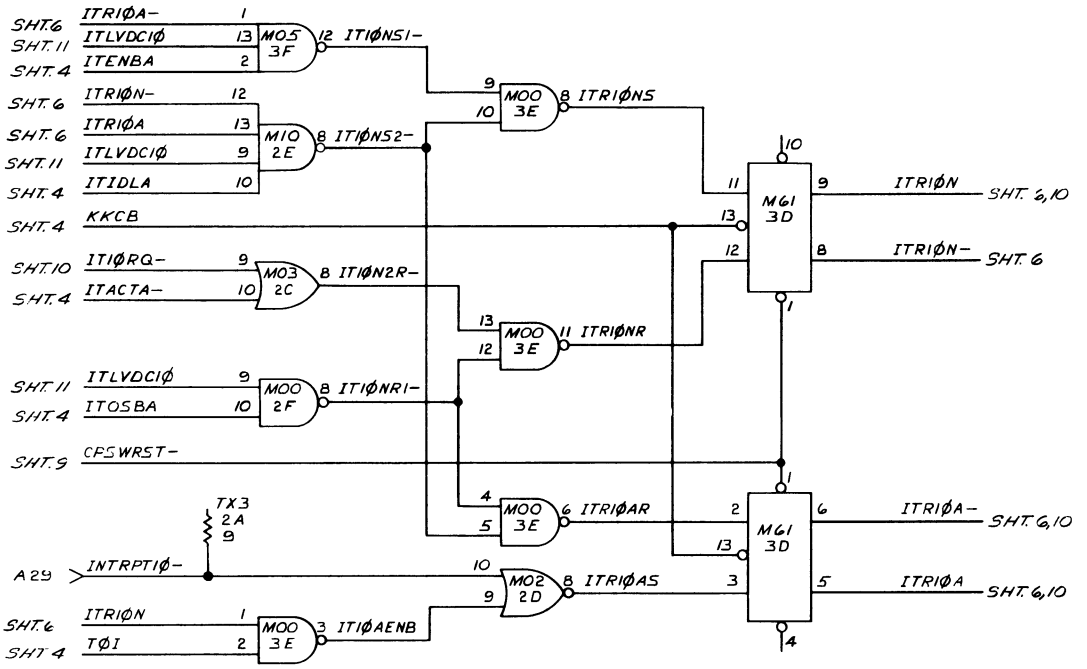


LEVEL Ø9 SERVICE FLIP-FLOP

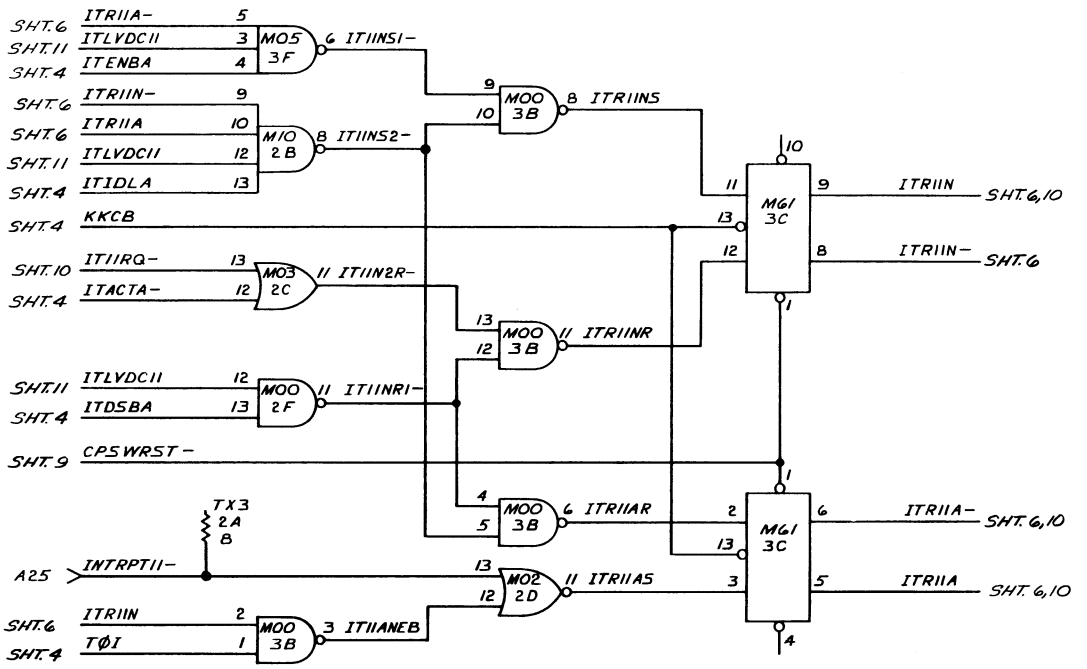


CODE IDENT NO.	SIZE		REV
49956	D	545541	A
SCALE NONE		SHEET 5	

LEVEL IØ SERVICE FLIP-FLOP



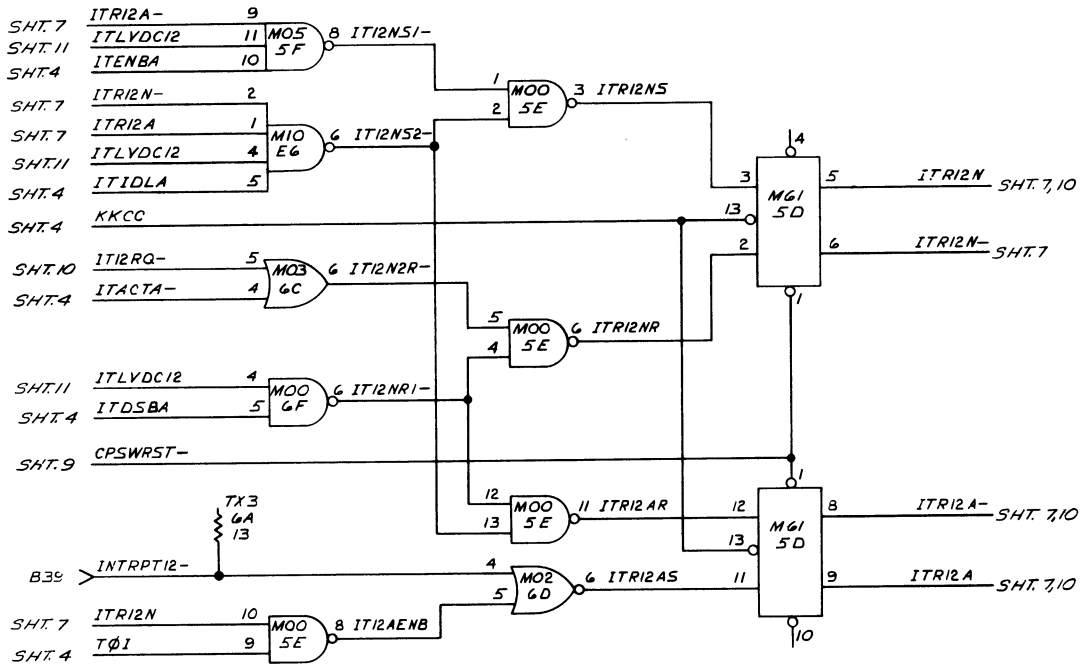
LEVEL II SERVICE FLIP-FLOP



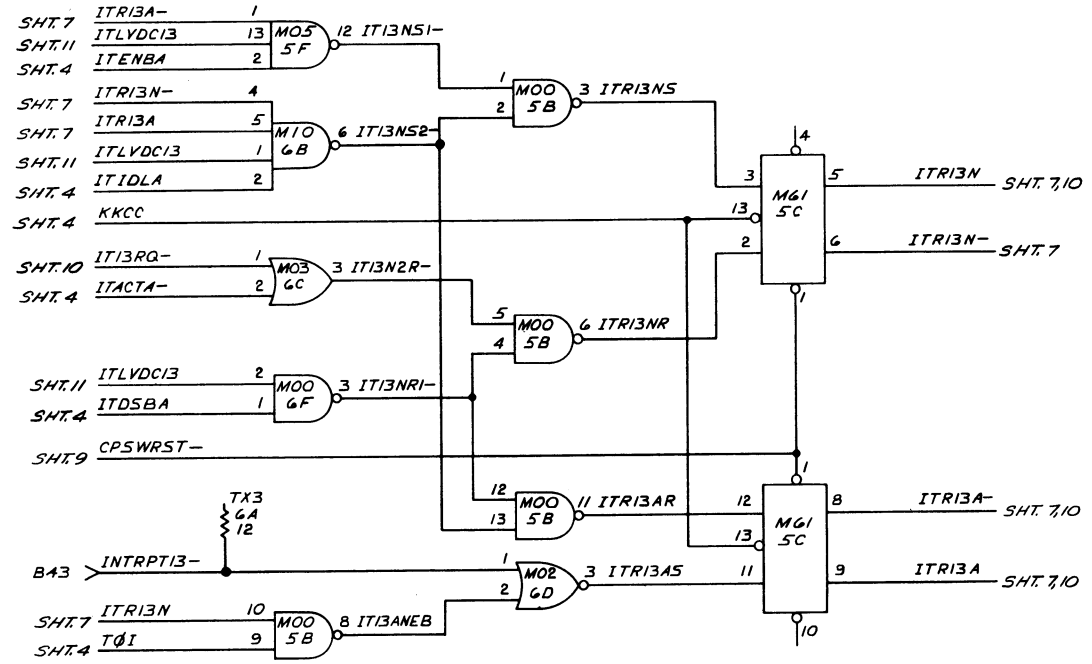
CODE IDENT NO.	SIZE		REV
49956	D	545541	4
SCALE NONE		SHEET 6	

RAYTHEON COMPUTER FORM 67-0006

LEVEL 12 SERVICE FLIP-FLOP



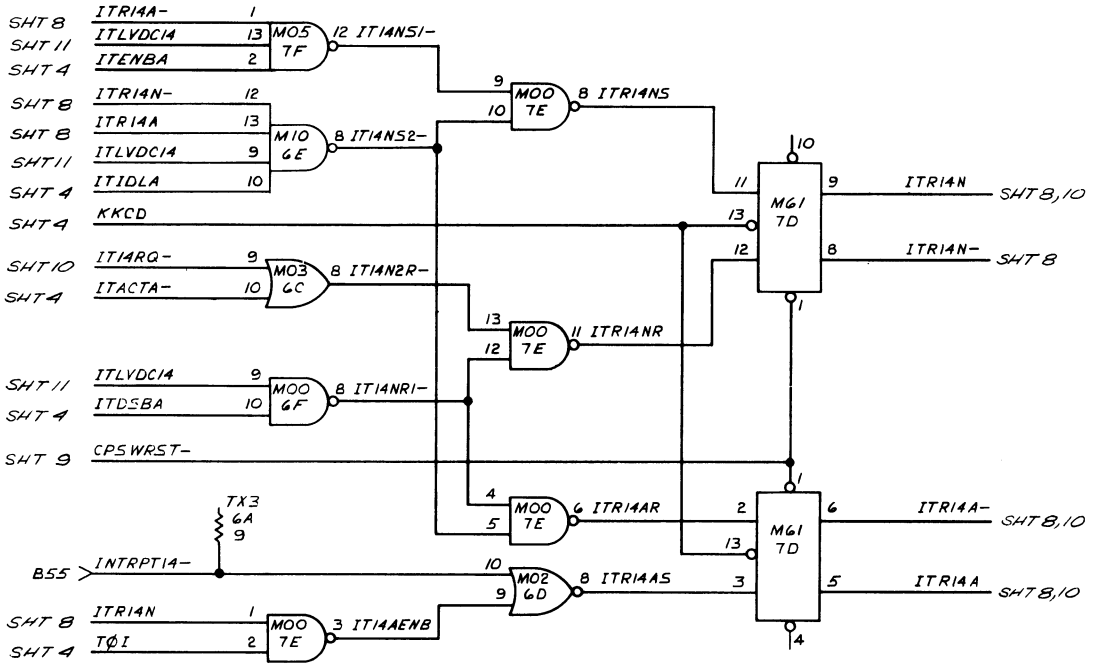
LEVEL 13 SERVICE FLIP-FLOP



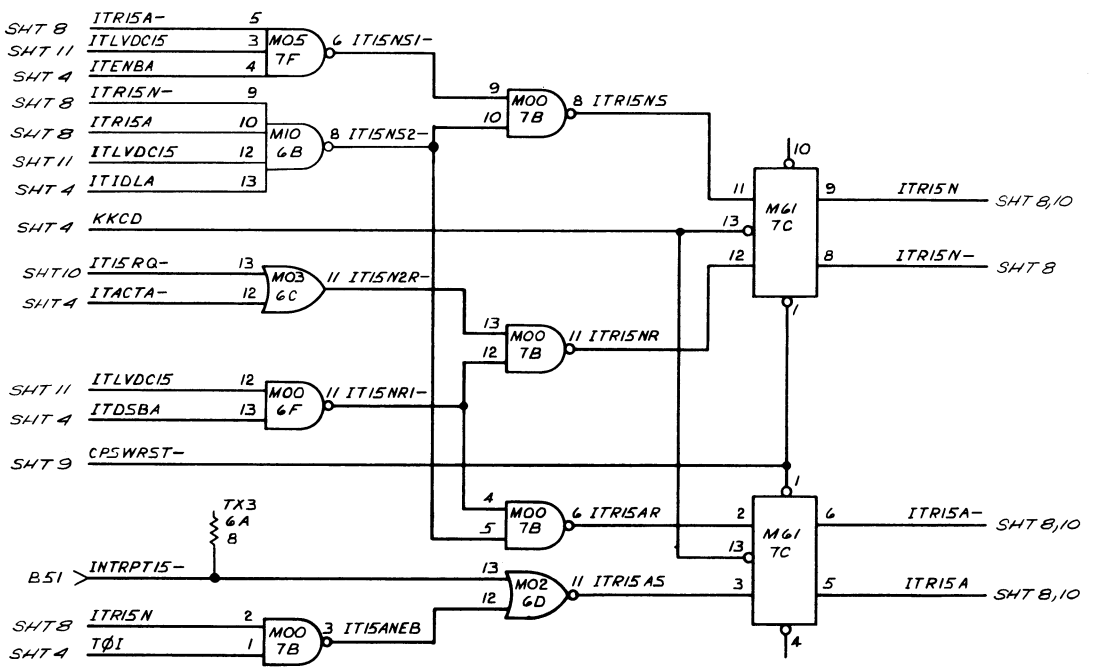
CODE IDENT NO.	SIZE		REV
49956	D	545541	A
SCALE NONE			SHEET 7

RAYTHEON COMPUTER FORM 67-0086

LEVEL 14 SERVICE FLIP-FLOP

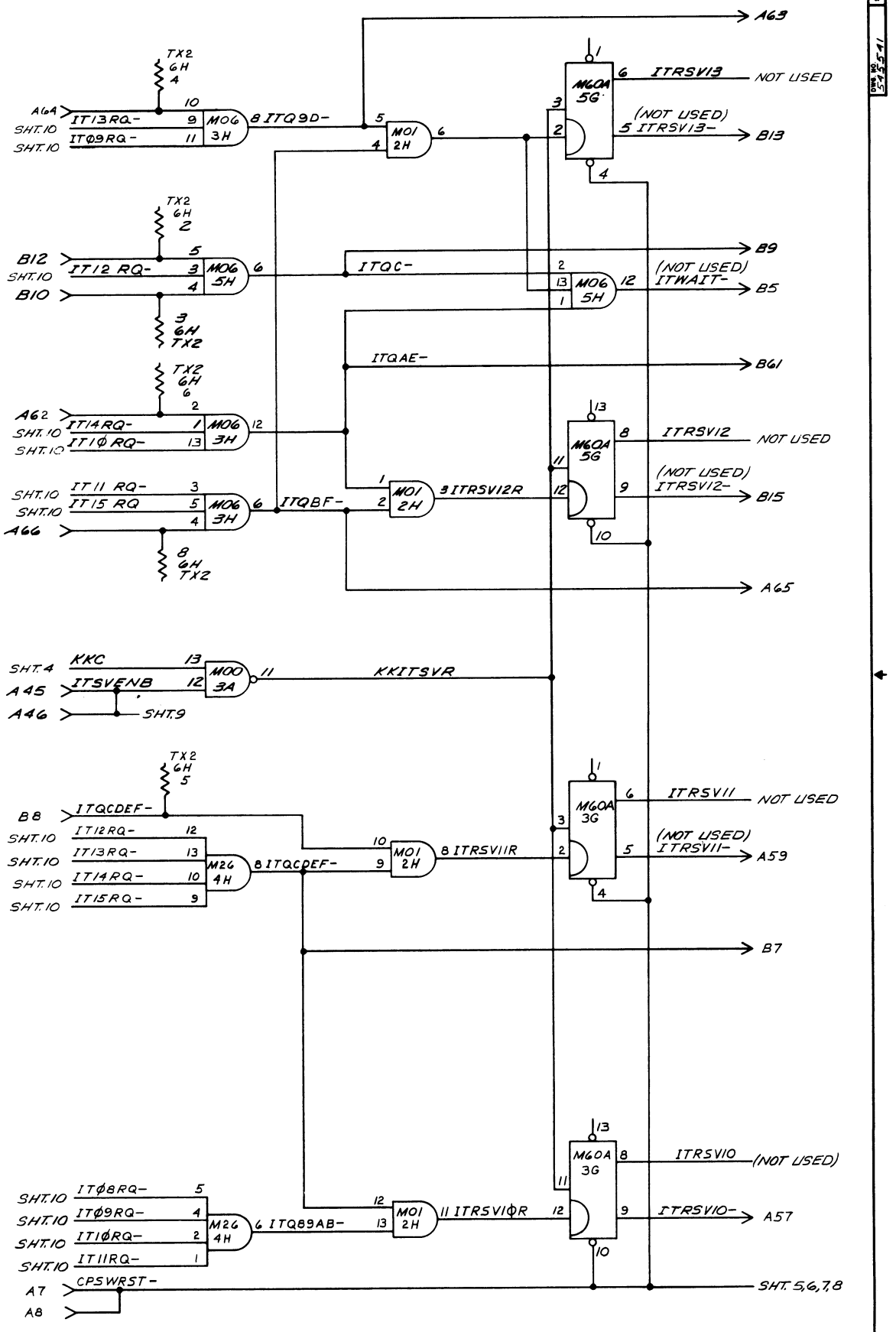


LEVEL 15 SERVICE FLIP-FLOP



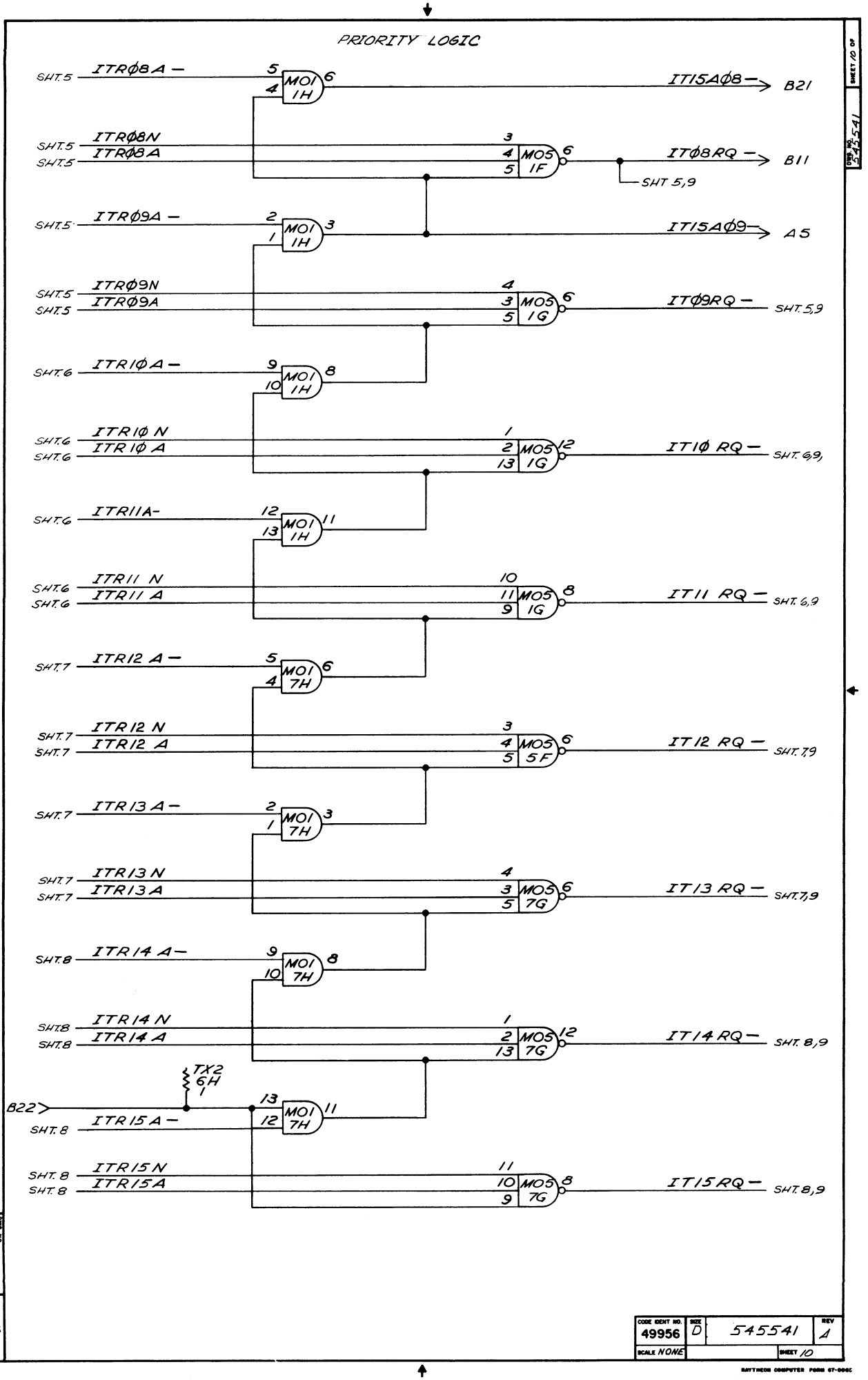
CODE IDENT NO.	SIZE		REV
49956	D	545541	A
SCALE NONE		SHEET 8	

INTERRUPT SERVICE REGISTER

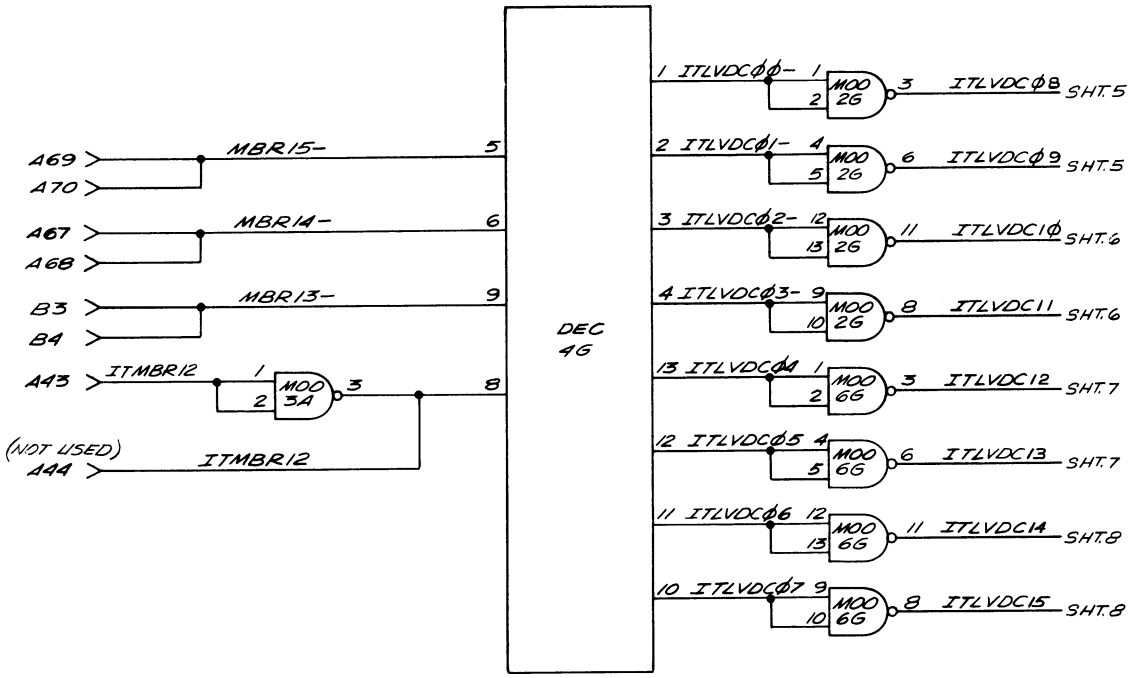


CODE IDENT NO.	SIZE		REV
49956	D	545541	A
SCALE NONE		SHEET 9	

RAYTHEON COMPUTER FORM 67-0006


PRIORITY LOGIC
SHT. 5 ITRØ8A —
5
4
M01 1H
6
IT15AØ8 — B21
SHT. 5 ITRØ8N
SHT. 5 ITRØ8A
3
4
5
M05 1F
6
ITØ8RQ — B11
SHT 5,9
SHT. 5 ITRØ9A —
2
1
M01 1H
3
IT15AØ9 — A5
SHT. 5 ITRØ9N
SHT. 5 ITRØ9A
4
3
5
M05 1G
6
ITØ9RQ — SHT. 5,9
SHT. 6 ITR1ØA —
9
10
M01 1H
8
SHT. 6 ITR1Ø N
SHT. 6 ITR1Ø A
1
2
13
M05 1G
12
IT1Ø RQ — SHT. 6,9
SHT. 6 ITR11A-
12
13
M01 1H
11
SHT. 6 ITR11 N
SHT. 6 ITR11 A
10
11
9
M05 1G
8
IT11 RQ — SHT. 6,9
SHT. 7 ITR12 A —
5
4
M01 7H
6
SHT. 7 ITR12 N
SHT. 7 ITR12 A
3
4
5
M05 5F
6
IT12 RQ — SHT. 7,9
SHT. 7 ITR13 A —
2
1
M01 7H
3
SHT. 7 ITR13 N
SHT. 7 ITR13 A
4
3
5
M05 7G
6
IT13 RQ — SHT. 7,9
SHT. 8 ITR14 A —
9
10
M01 7H
8
SHT. 8 ITR14 N
SHT. 8 ITR14 A
1
2
13
M05 7G
12
IT14 RQ — SHT. 8,9
TX2 6H 1
B22
13
12
M01 7H
11
SHT. 8 ITR15 A —
SHT. 8 ITR15 N
SHT. 8 ITR15 A
11
10
9
M05 7G
8
IT15 RQ — SHT. 8,9
DWG NO. 545541
SHEET 10 OF
DWG NO. 545541
SHEET 10 OF
CODE IDENT NO. 49956
SIZE D
545541
REV A
SCALE NONE
SHEET 10
RAYTHEON COMPUTER FORM 67-0006

INTERRUPT LEVEL DECODER



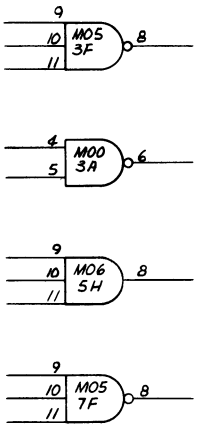
DWG. NO. 545541 SHEET 11 OF

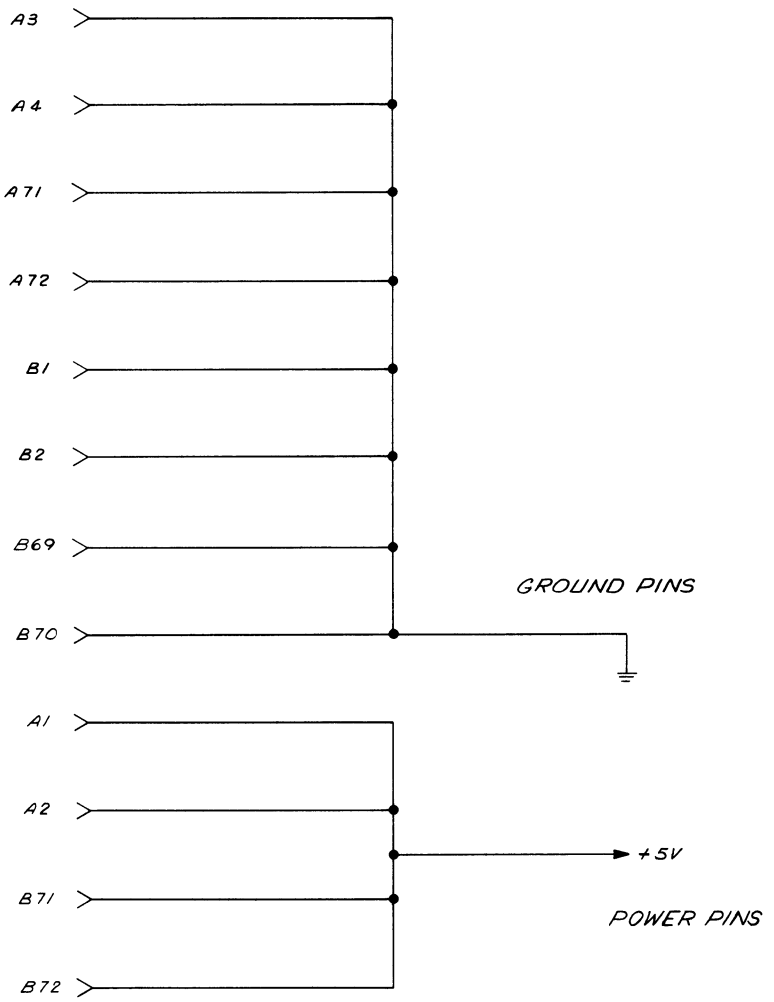
DWG. NO. 545541 SHEET 11 OF

CODE IDENT NO.	SIZE		REV
49956	D	545541	A
SCALE NONE			SHEET 11

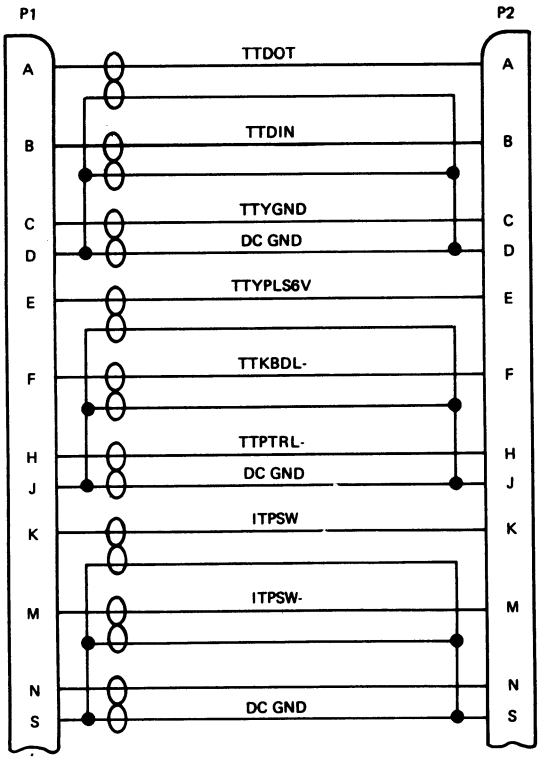
RAYTHEON COMPUTER FORM 67-0069

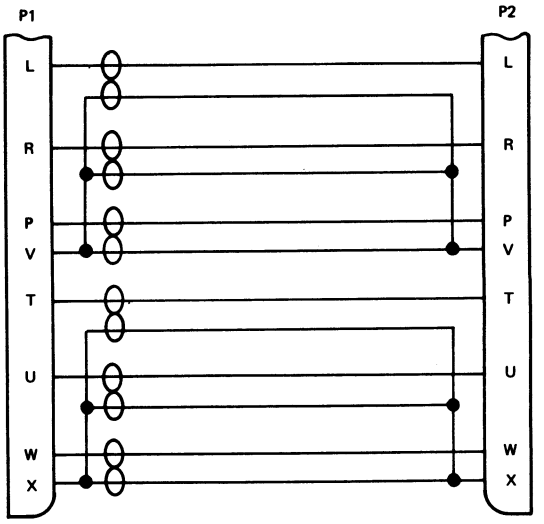
UNUSED I.C. PARTS





CODE IDENT NO.	SIZE		REV
49956		545541	A
SCALE NONE		SHEET 12	

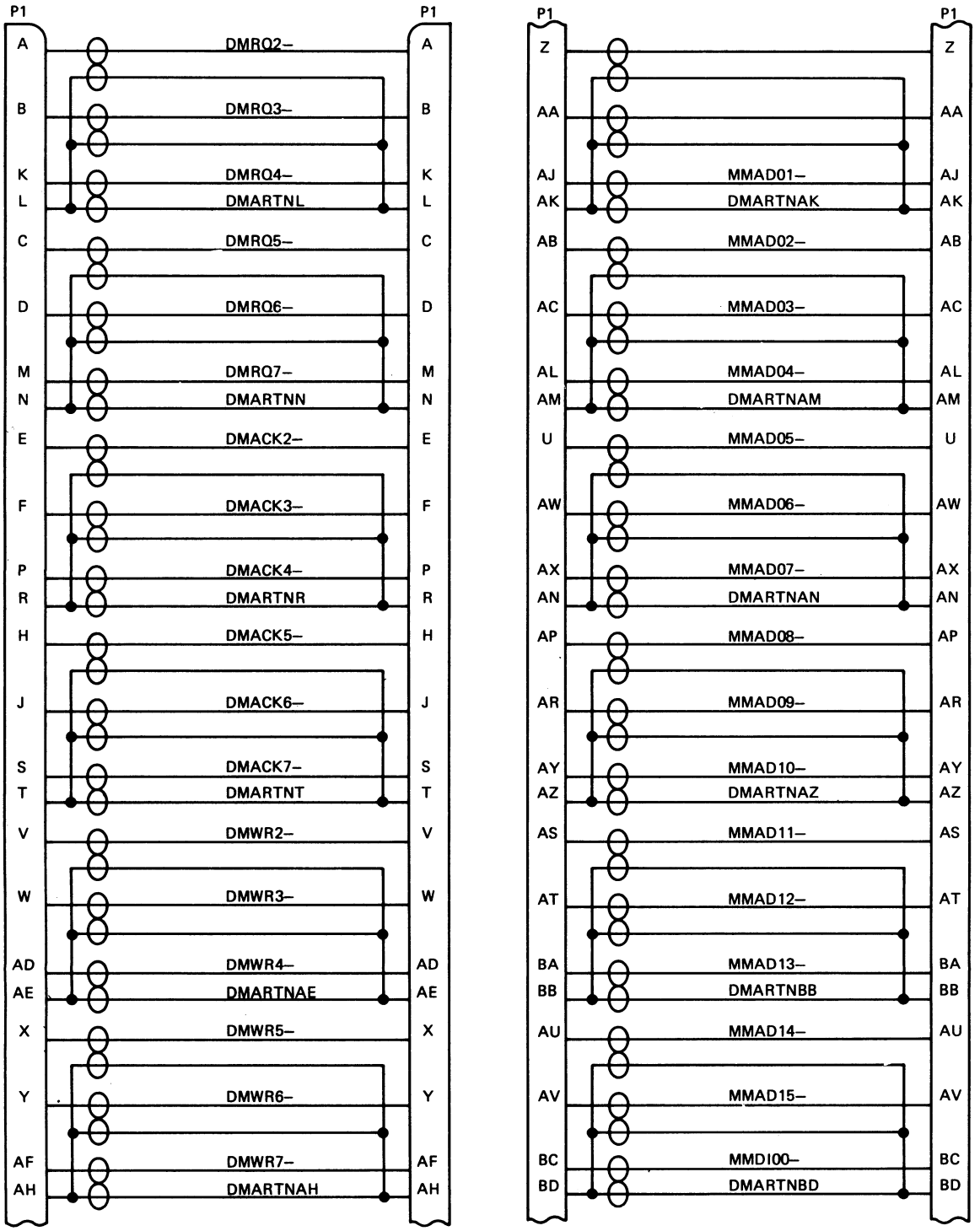




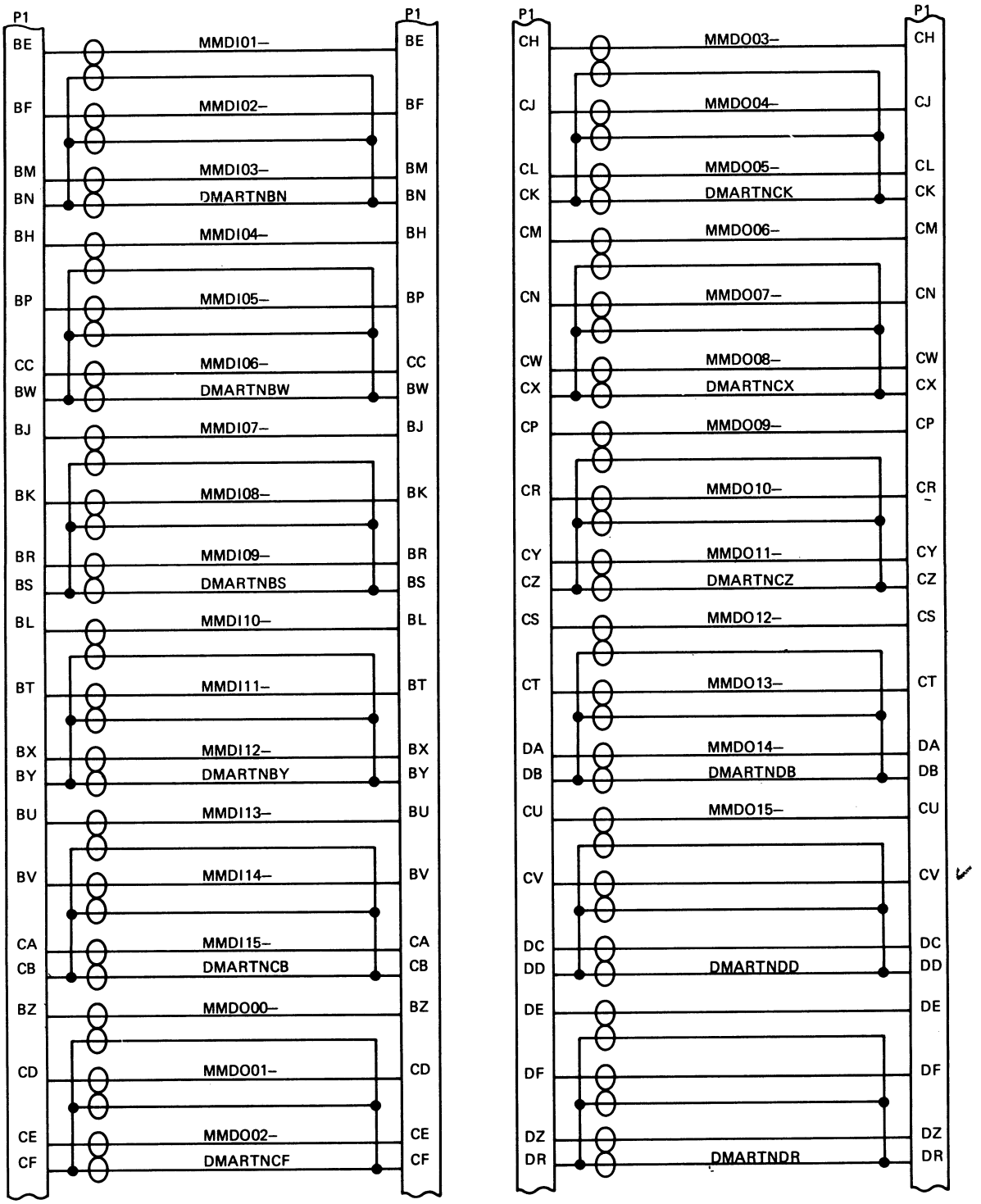
NOTE:

CONNECTORS P1 AND P2 ARE ELCO 00-8016-020-000-703 WITH 60-8017-0313 CONTACTS (RAYTHEON COMPUTER SPEC. NO. 530724-003 AND 530028-001).

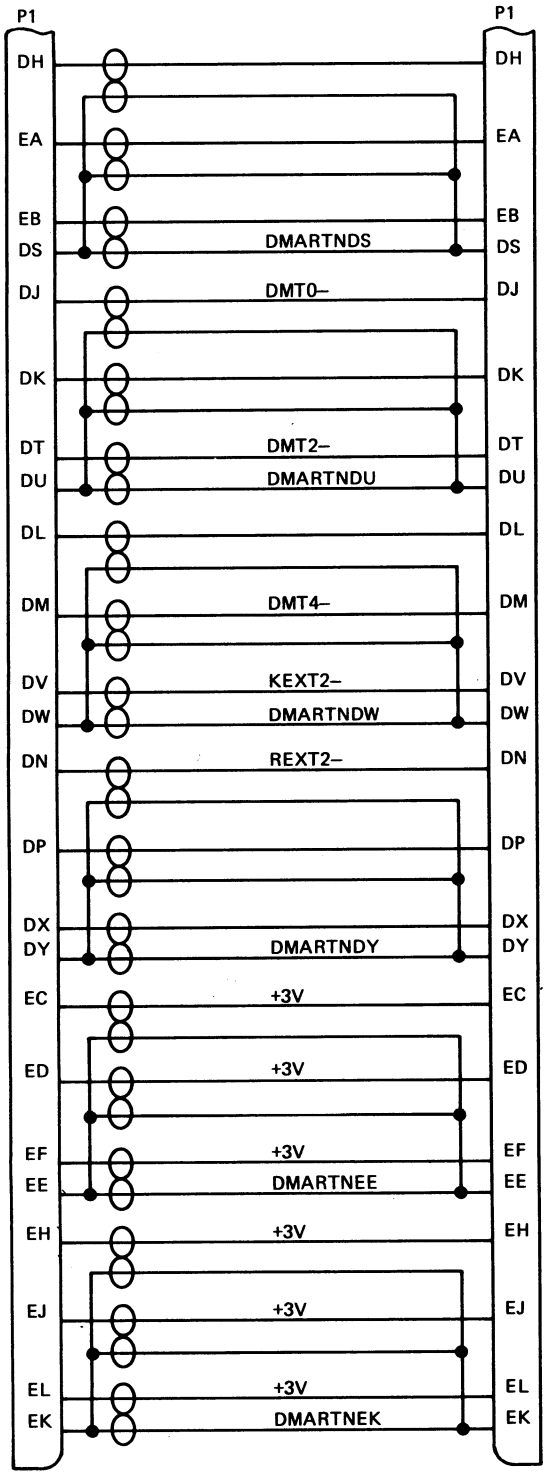
Drawing 278128. Teletypewriter Set Signal Schematic



Drawing 279557. DMA Signal Cable Schematic (Sheet 1 of 3)



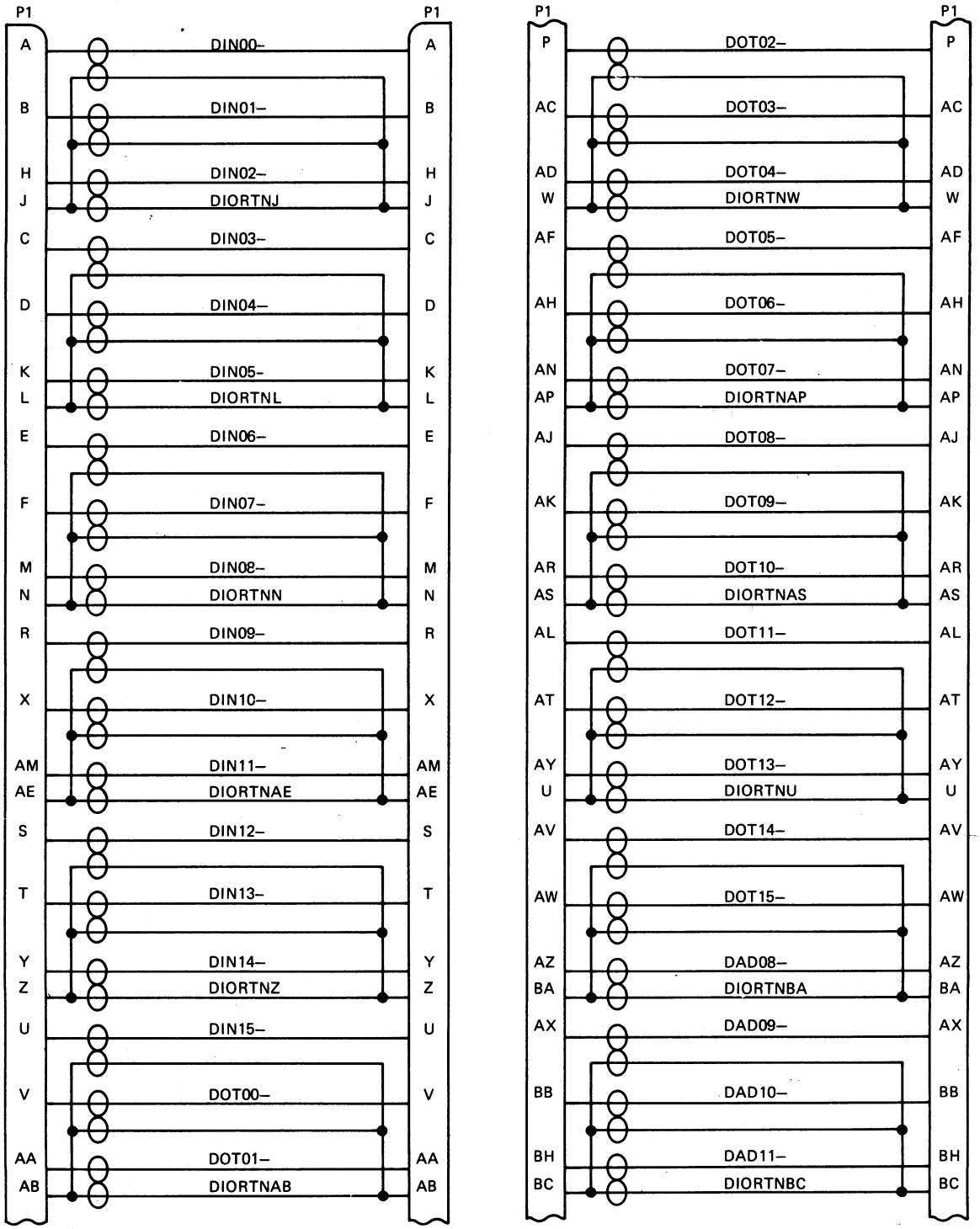
Drawing 279557. DMA Signal Cable Schematic (Sheet 2 of 3)



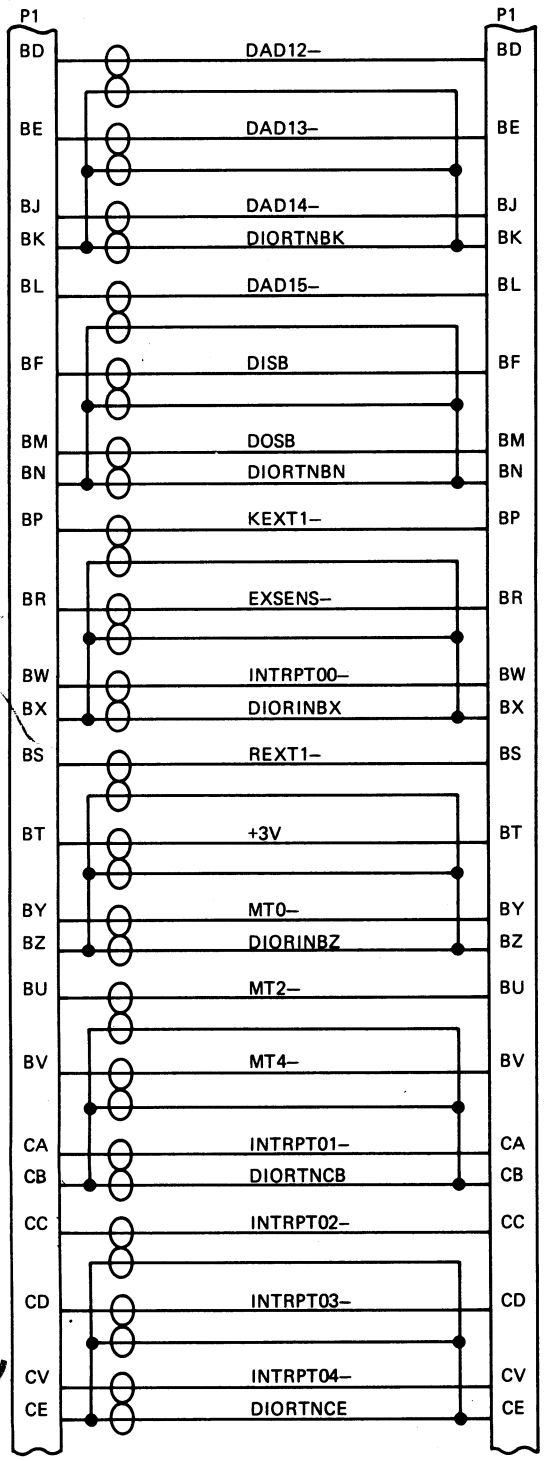
NOTE:

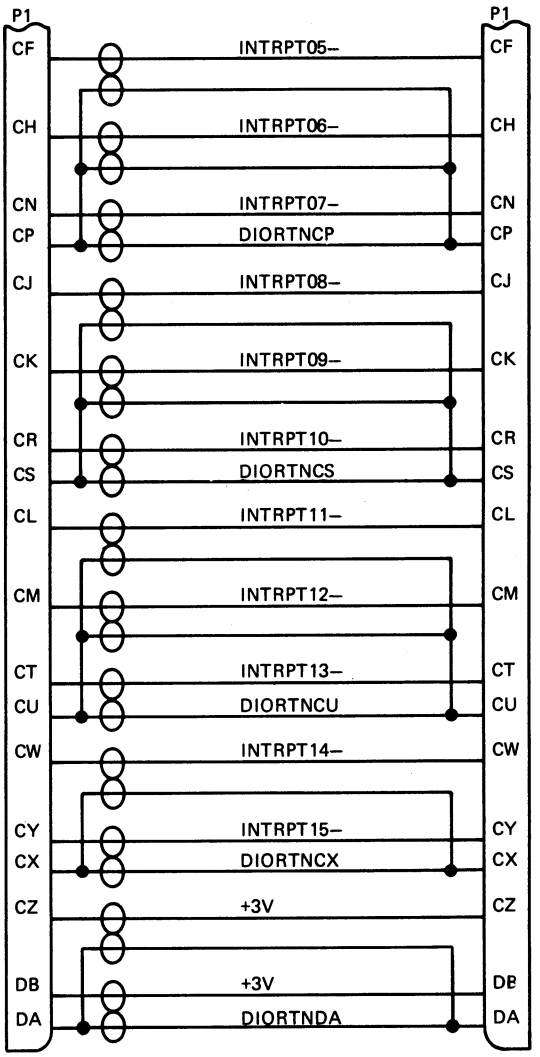
Connectors P1 are Elco 00-8016-120-000-703 with 60-8017-0313 contacts (Raytheon Computer Spec. No. 530724-006 and 530028-001).

Drawing 279557. DMA Signal Cable Schematic (Sheet 3 of 3)



Drawing 279558. DIO Signal Cable Schematic (Sheet 1 of 2)

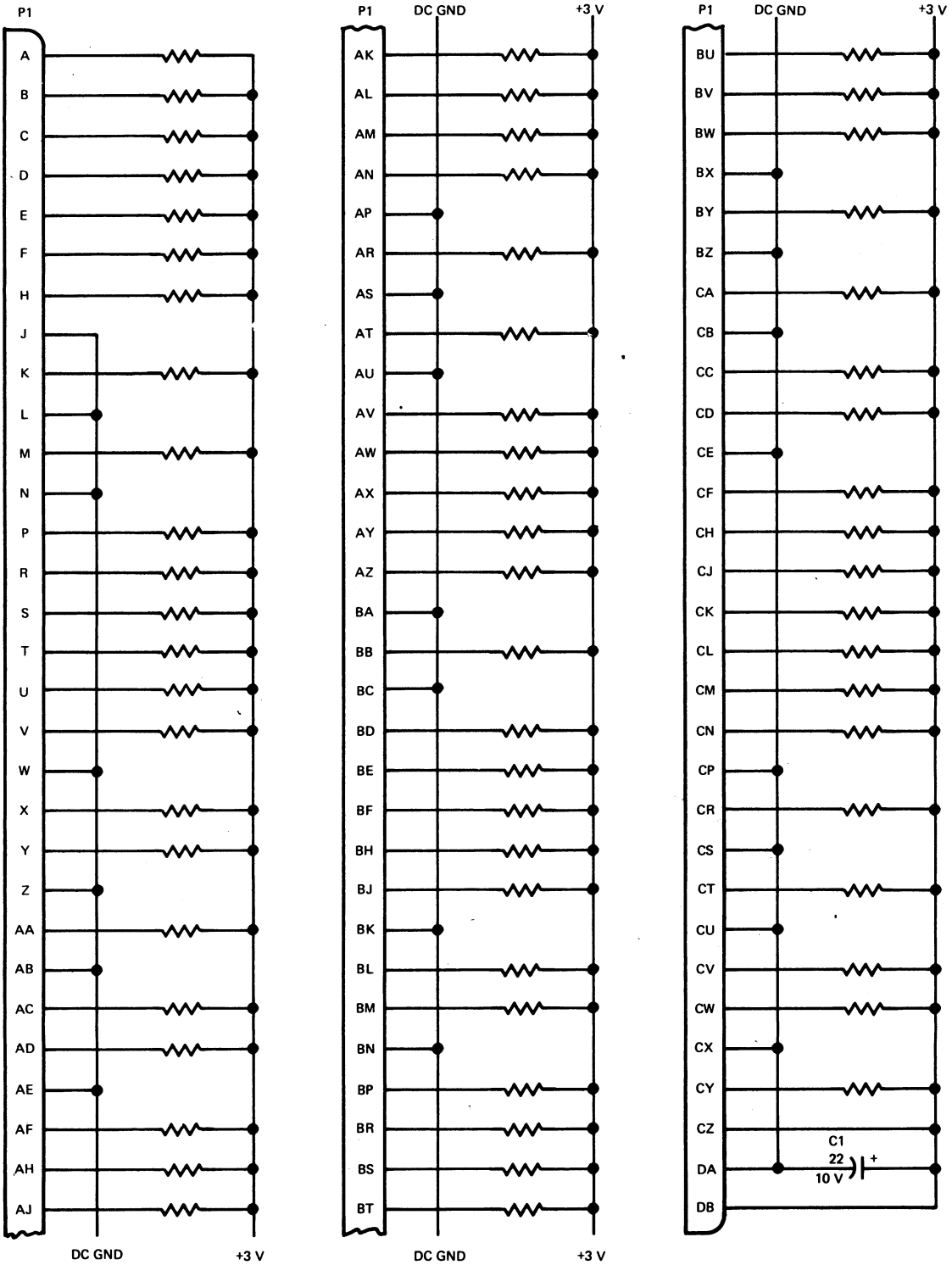




NOTE:

Connectors Plane Elco 00-8016-090-000-703 with 60-8017-0313 contacts (Raytheon Computer Spec. No. 530724-005 and 530028-001).

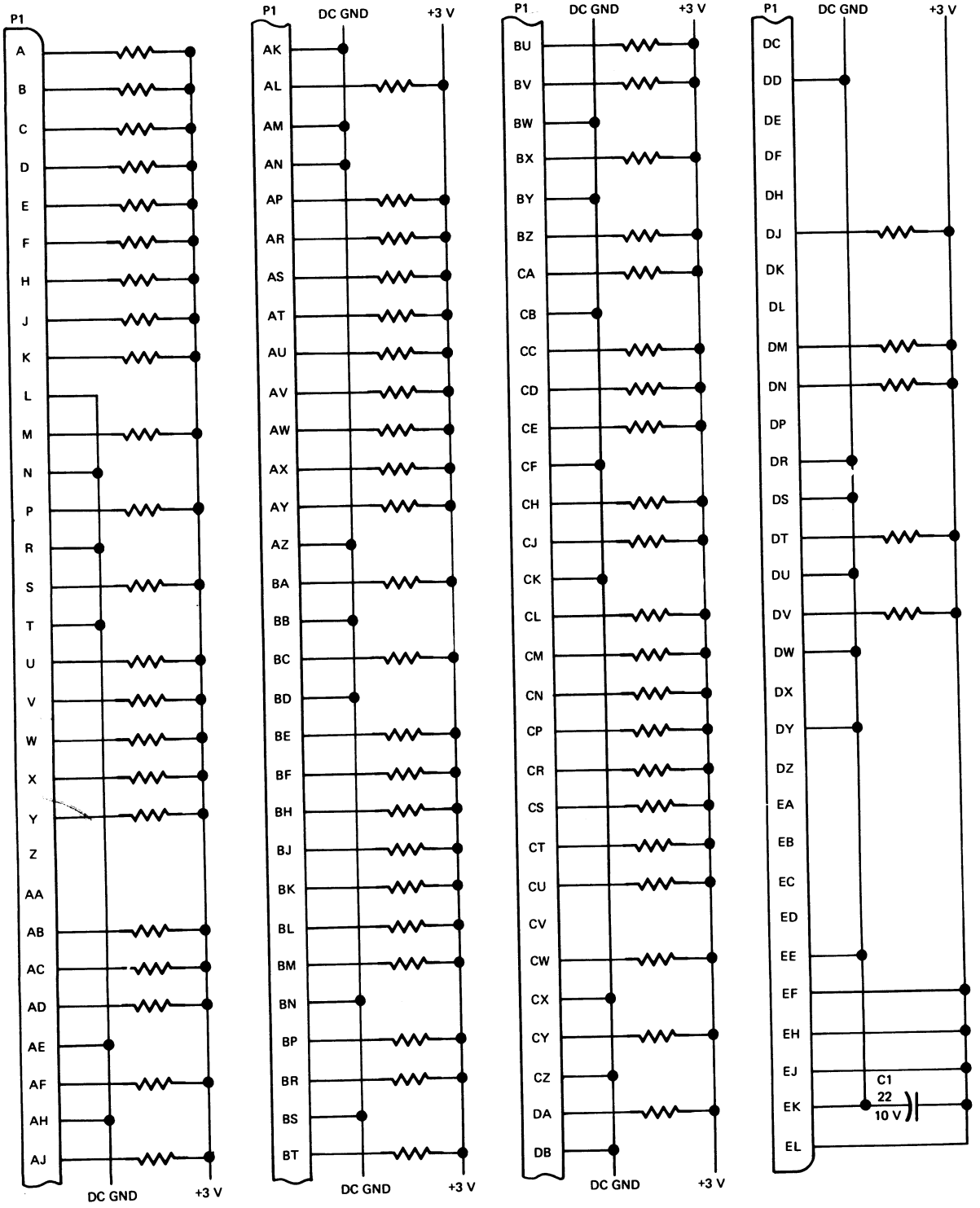
Drawing 279558. DIO Signal Cable Schematic (Sheet 2 of 2)



NOTES:

1. ALL RESISTORS ARE 120-OHM, 1/4 W.
2. CONNECTOR P1 IS ELCO 00-8016-090-000-703 WITH 60-8017-0313 CONTACTS. (RAYTHEON COMPUTER SPEC NO. 530724-005 AND 530028-001.

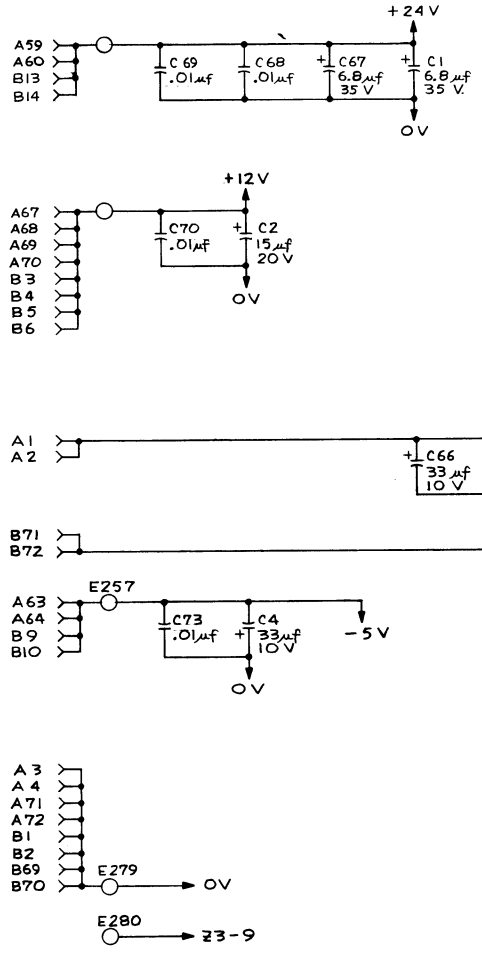
Drawing 279767. DIO Terminator Schematic



NOTES:

1. ALL RESISTORS ARE 120-OHM, 1/4 W
2. CONNECTOR P1 IS ELCO 00-8016-120-000-703 WITH 60-8017-0313 CONTACTS (RAYTHEON COMPUTER SPEC NO. 530724-006 AND 530028-001).

Drawing 279768. DMA and Memory Terminator Schematic



RESERVE EO'S OUTSTANDING	REVISIONS							
	SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	X1	APPROVAL PER E.O 20235			KB	JJB	[illegible]	7/31/70
	A	RELEASED PER E.O 20497			KB	JJB	[illegible]	7/6/70
	B	REVISED PER E.O. 21170			[illegible]	JJB	JJB	7/27/70
	C	REVISED PER E.O. 21221			[illegible]	JJB	JJB	7/6/70

4. ALL TRANSFORMERS ARE 531705-001.
3. ALL TRANSISTORS ARE 531700-001.
2. ALL DIODES ARE 531701-001.
1. ALL RESISTORS ARE 1/4 W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON:
DECIMALS .XX ±.03 .XXX ±.010
ANGLES ± 0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN	K. Bruce	19 MAR 70
CHECK	[illegible]	3/31/70
APPR	[illegible]	4 APR 1970
APPR	[illegible]	4 APR 70

NEXT ASSY 394691

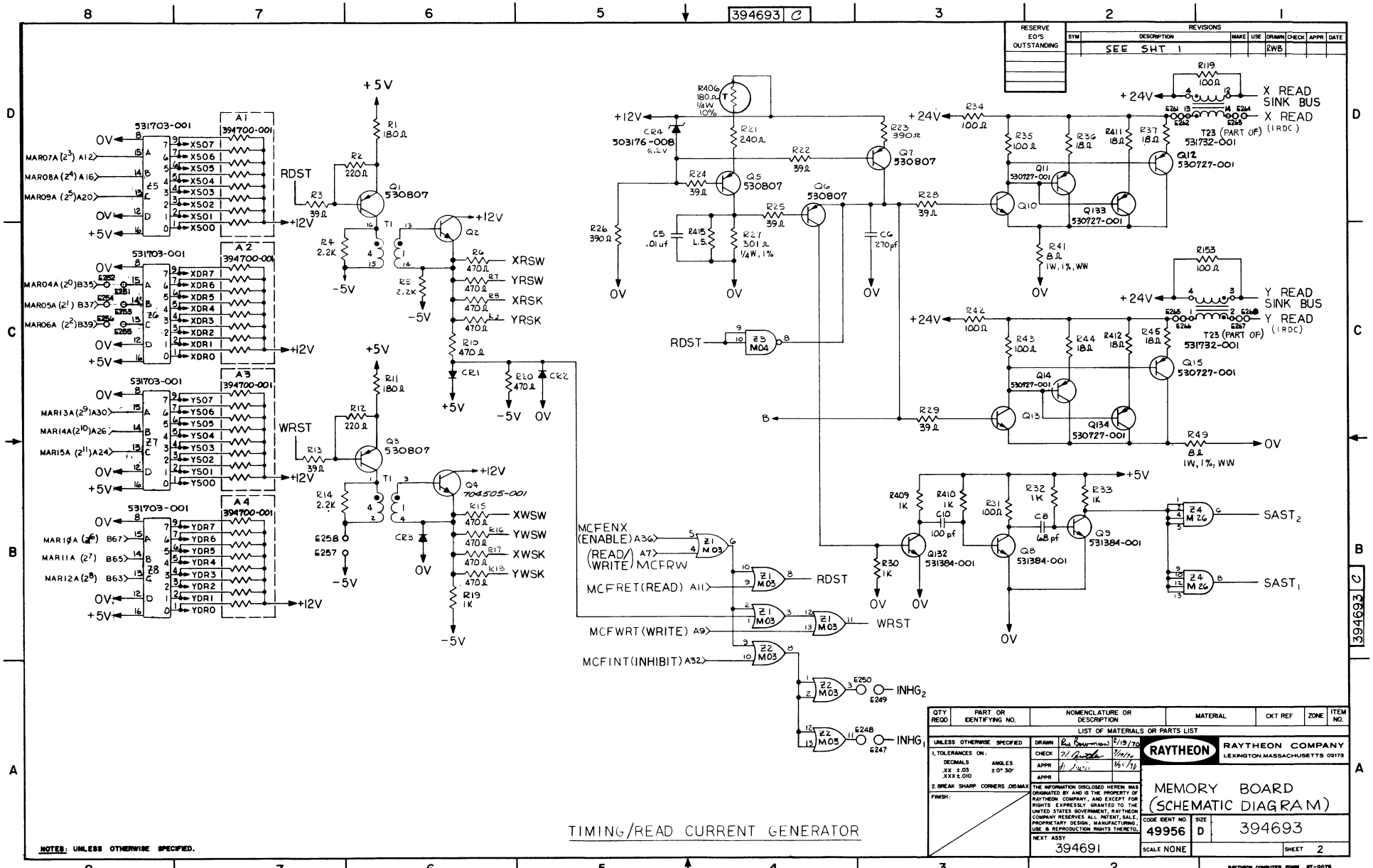
RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

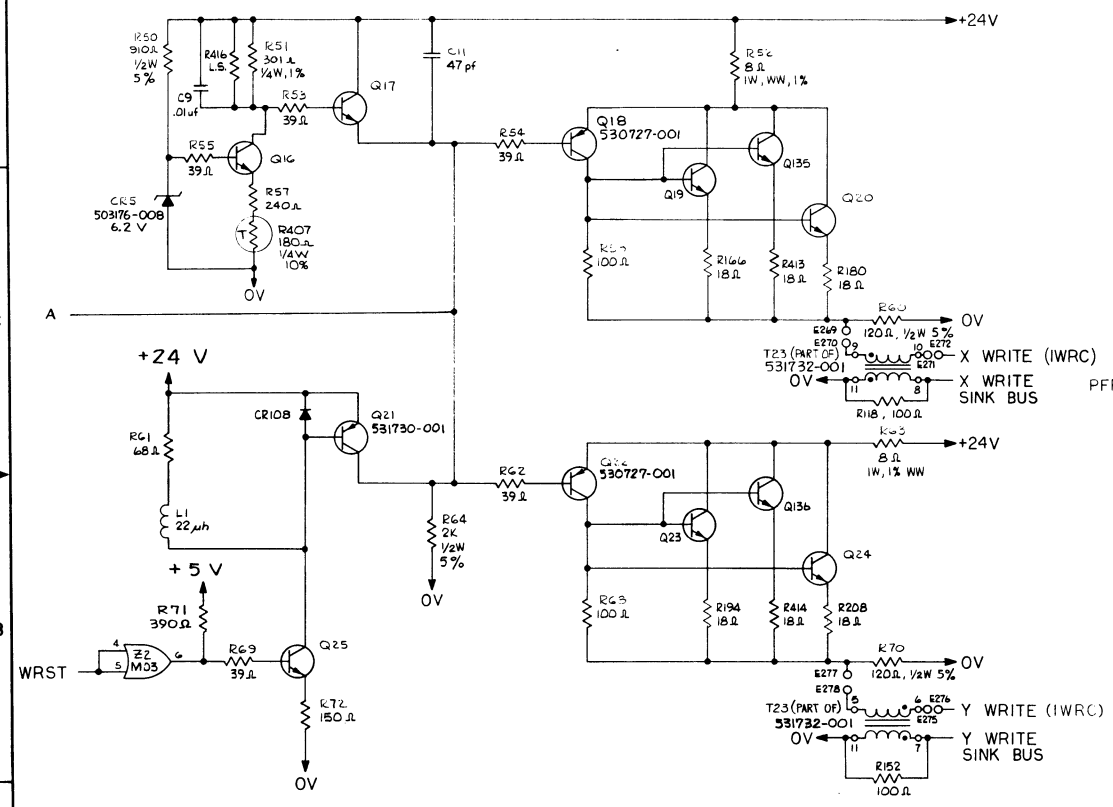
MEMORY BOARD (SCHEMATIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE D | 394693 | SCALE NONE | SHEET 1 OF 11

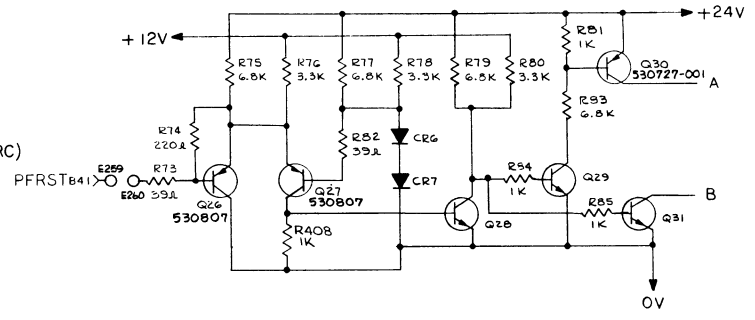
RAYTHEON COMPUTER FORM 67-0078

394693 C


394693 C
RESERVE EO'S OUTSTANDING
REVISIONS
SYM | DESCRIPTION | MAKE | USE | DRAWN | CHECK | APPR | DATE
SEE SHT 1 | 2WB
5311703-001
A1 394700-001
A2 394700-001
A3 394700-001
A4 394700-001
MAR07A (2^3) A12
MAR08A (2^4) A16
MAR09A (2^5) A20
MAR04A (2^0) B35
MAR05A (2^1) B37
MAR06A (2^2) B39
MAR13A (2^9) A30
MAR14A (2^10) A26
MAR15A (2^11) A24
MAR10A (2^6) B67
MAR11A (2^7) B65
MAR12A (2^8) B63
XS07 XS06 XS05 XS04 XS03 XS02 XS01 XS00
XDR7 XDR6 XDR5 XDR4 XDR3 XDR2 XDR1 XDR0
YS07 YS06 YS05 YS04 YS03 YS02 YS01 YS00
YDR7 YDR6 YDR5 YDR4 YDR3 YDR2 YDR1 YDR0
RDST
WRST
+5V
+12V
-5V
0V
Q1 530807
Q2
Q3 530807
Q4 704505-001
XRSW
YRSW
XRSK
YRSK
XWSW
YWSW
XWSK
YWSK
CR1
CR2
CR3
MCFENX (ENABLE) A36
(READ/WRITE) MCFRW A7
MCFRET (READ) A11
MCFWRT (WRITE) A9
MCFINT (INHIBIT) A32
INHG2
INHG1
Q5 530807
Q6 530807
Q7 530807
Q8 531384-001
Q9 531384-001
Q10 530727-001
Q11 530727-001
Q12 530727-001
Q13 530727-001
Q14 530727-001
Q15 530727-001
Q132 531384-001
Q133 530727-001
Q134 530727-001
CR4 503176-008 6.2V
T23 (PART OF) 5311732-001 (IRDC)
X READ SINK BUS
X READ
Y READ SINK BUS
Y READ
SAST2
SAST1
TIMING/READ CURRENT GENERATOR
NOTES: UNLESS OTHERWISE SPECIFIED.
QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL | CKT REF | ZONE | ITEM NO.
LIST OF MATERIALS OR PARTS LIST
UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:
DRAWN R. Bowman 8/19/70
CHECK M. Curtis 9/10/70
APPR M. Curtis 9/15/70
APPR
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF RAYTHEON COMPANY, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, RAYTHEON COMPANY RESERVES ALL PATENT, SALE, PROPRIETARY DESIGN, MANUFACTURING, USE & REPRODUCTION RIGHTS THERETO.
NEXT ASSY 394691
RAYTHEON COMPANY LEXINGTON, MASSACHUSETTS 02173
MEMORY BOARD (SCHEMATIC DIAGRAM)
CODE IDENT NO 49956
SIZE D
394693
SCALE NONE
SHEET 2
RAYTHEON COMPUTER FORM 07-0075



WRITE CURRENT GENERATOR



MEMORY PROTECT

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:

DRAWN R.W. Bowman 5/19/70
CHECK M. Burke 5/19/70
APPR
APPR

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NEXT ASSY 394691

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

MEMORY BOARD (SCHEMATIC DIAGRAM)

CODE IDENT NO. 49956 | SIZE D | 394693

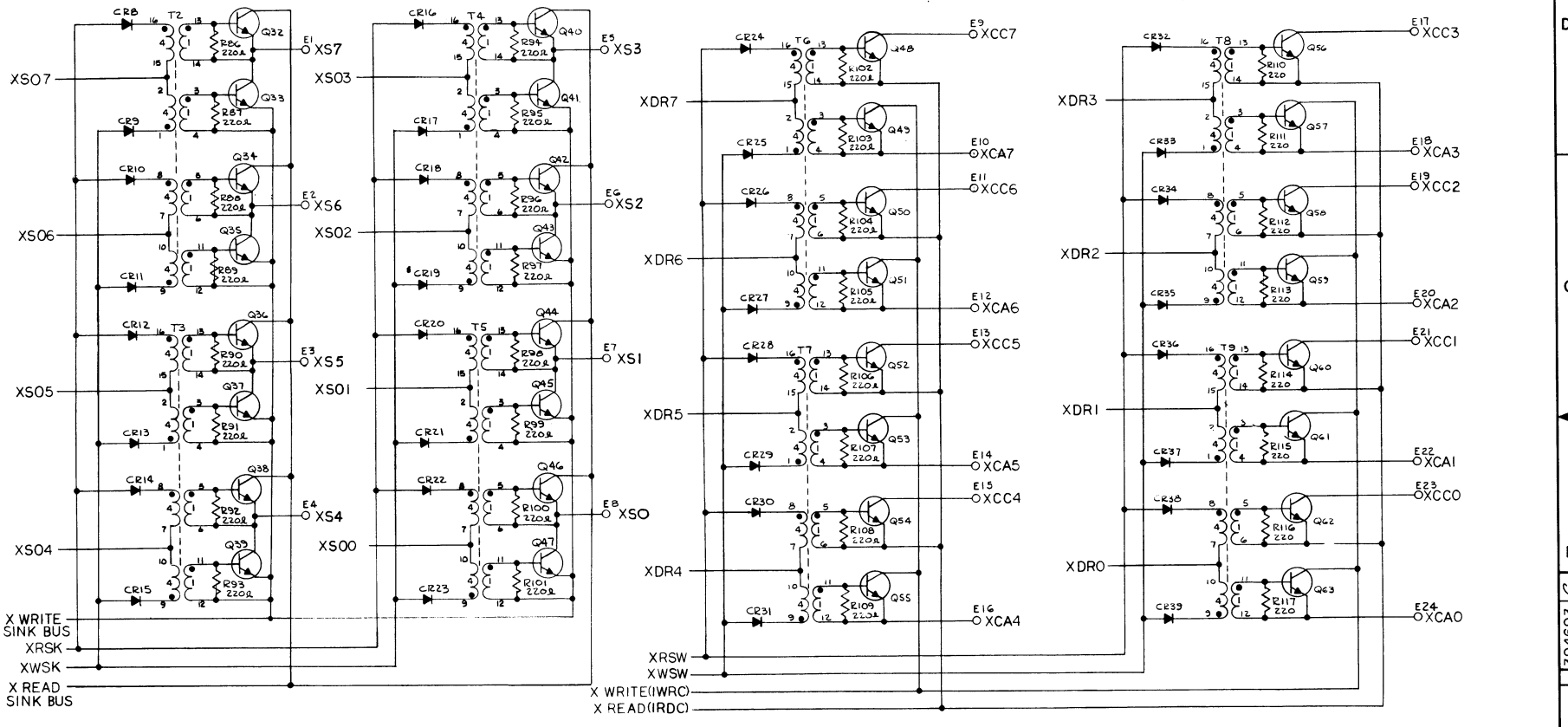
SCALE NONE | SHEET 3

RAYTHEON COMPUTER FORM 67-0075

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	SEE SHEET 1			RW			

NOTES: UNLESS OTHERWISE SPECIFIED.



X DRIVE AND SINK

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	SEE SHEET 1			RWB			

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN 3/19/70
CHECK 3/19/70
APPR 3/25/70
APPR

NEXT ASSY 394691

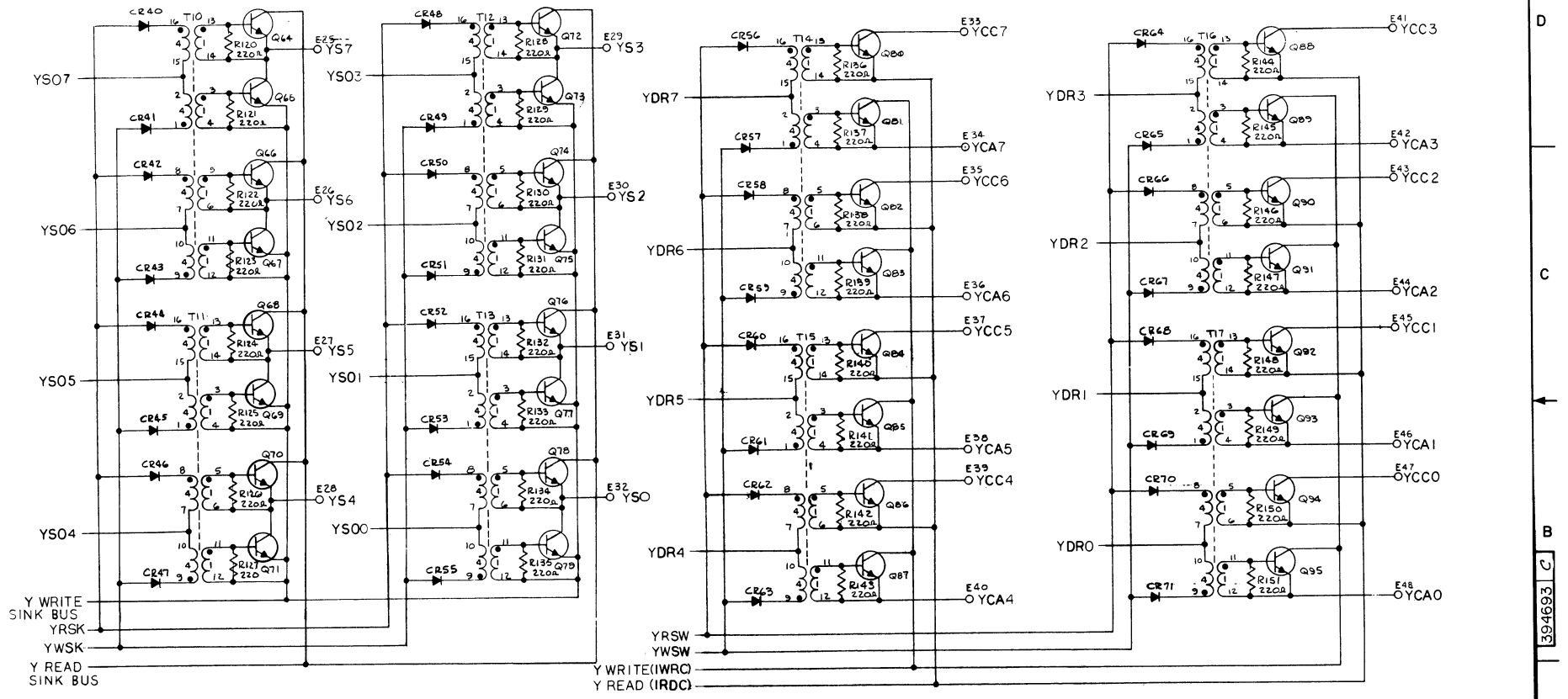
RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

MEMORY BOARD (SCHEMATIC DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	394693
SCALE NONE		SHEET 4

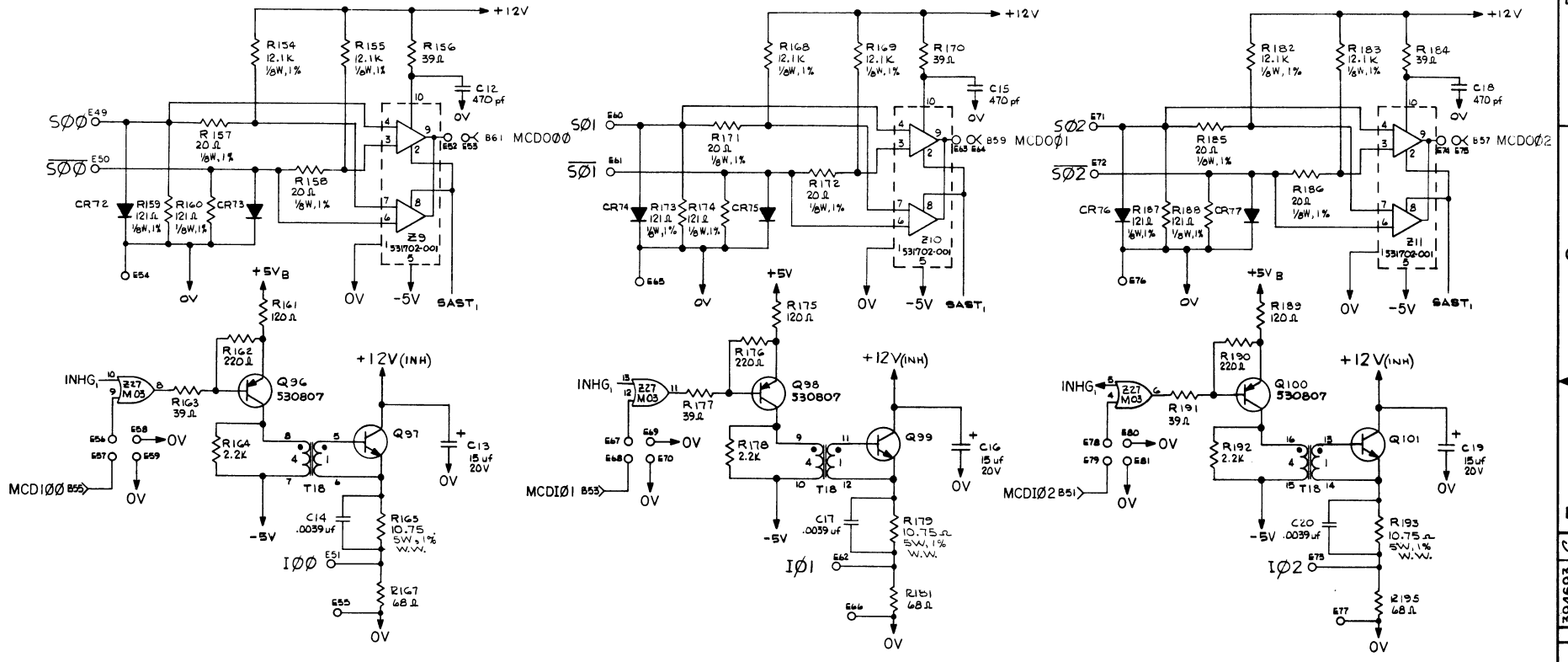
RAYTHEON COMPUTER FORM 67-0078

394693 C


394693 C
RESERVE EO'S OUTSTANDING
REVISIONS
SYM DESCRIPTION MAKE USE DRAWN CHECK APPR DATE
SEE SHEET 1 RWB
YS07
YS03
YS06
YS02
YS05
YS01
YS04
YS00
E25 YS7
E29 YS3
E26 YS6
E30 YS2
E27 YS5
E31 YS1
E28 YS4
E32 YS0
Y WRITE SINK BUS
YRSK
YWSK
Y READ SINK BUS
YDR7
YDR6
YDR5
YDR4
E33 YCC7
E34 YCA7
E35 YCC6
E36 YCA6
E37 YCC5
E38 YCA5
E39 YCC4
E40 YCA4
YRSW
YWSW
Y WRITE(IWRC)
Y READ (IRDC)
YDR3
YDR2
YDR1
YDR0
E41 YCC3
E42 YCA3
E43 YCC2
E44 YCA2
E45 YCC1
E46 YCA1
E47 YCC0
E48 YCA0
Y DRIVE AND SINK
QTY REQD
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
MATERIAL
CKT REF
ZONE
ITEM NO.
LIST OF MATERIALS OR PARTS LIST
UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .05 MAX
FINISH:
DRAWN 2/19/70
CHECK 3/6/70
APPR 3/6/70
APPR
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF RAYTHEON COMPANY, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, RAYTHEON COMPANY RESERVES ALL PATENT, SALE, PROPRIETARY DESIGN, MANUFACTURING, USE & REPRODUCTION RIGHTS THERETO.
NEXT ASSY 394691
RAYTHEON
RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173
MEMORY BOARD (SCHEMATIC DIAGRAM)
CODE IDENT NO. 49956
SIZE D
394693
SCALE NONE
SHEET 5
RAYTHEON COMPUTER FORM 67-0075

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	SEE SHEET 1			RWH			



DATA LOOP

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
LIST OF MATERIALS OR PARTS LIST						

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN R.J. Sherman 5/19/70
CHECK M. Curtis 5/19/70
APPR V. Liuzzi 5/21/70
APPR

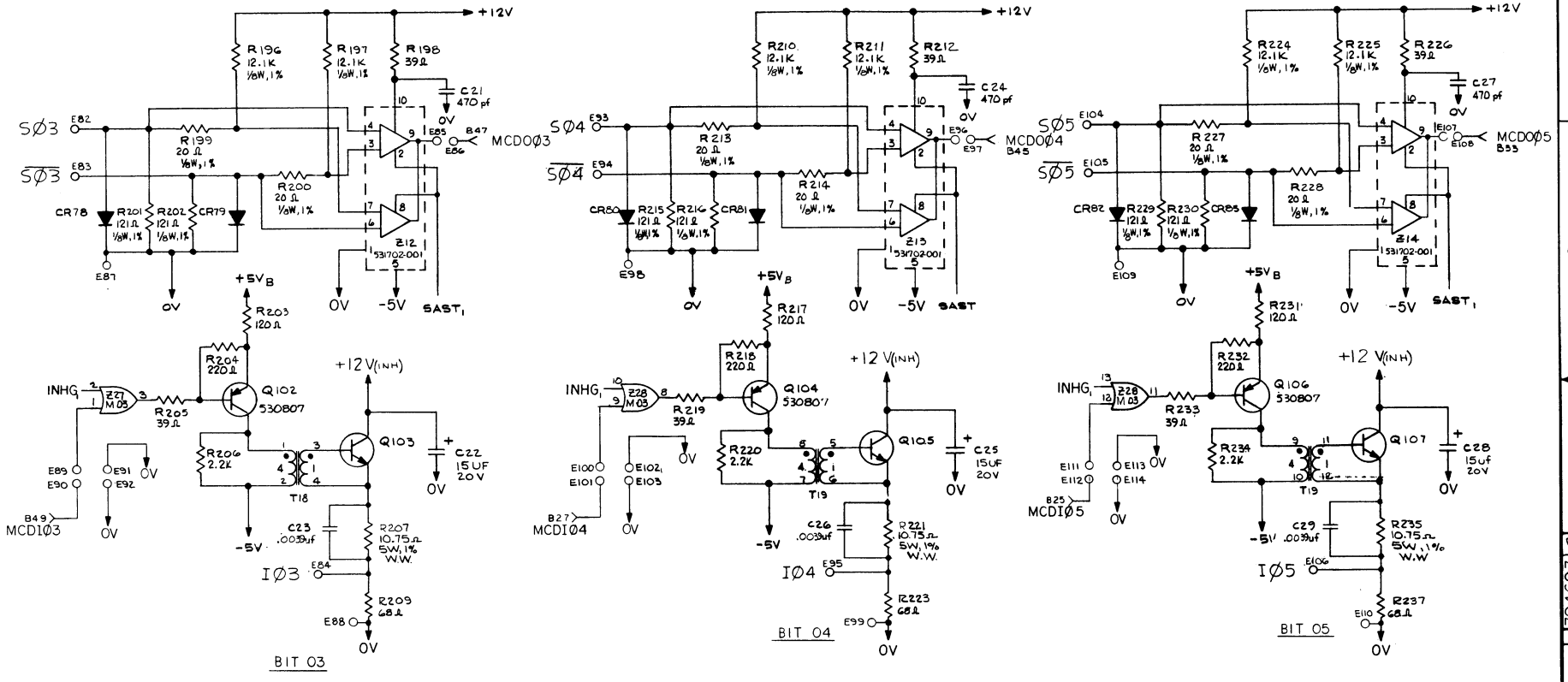
NEXT ASSY 394691

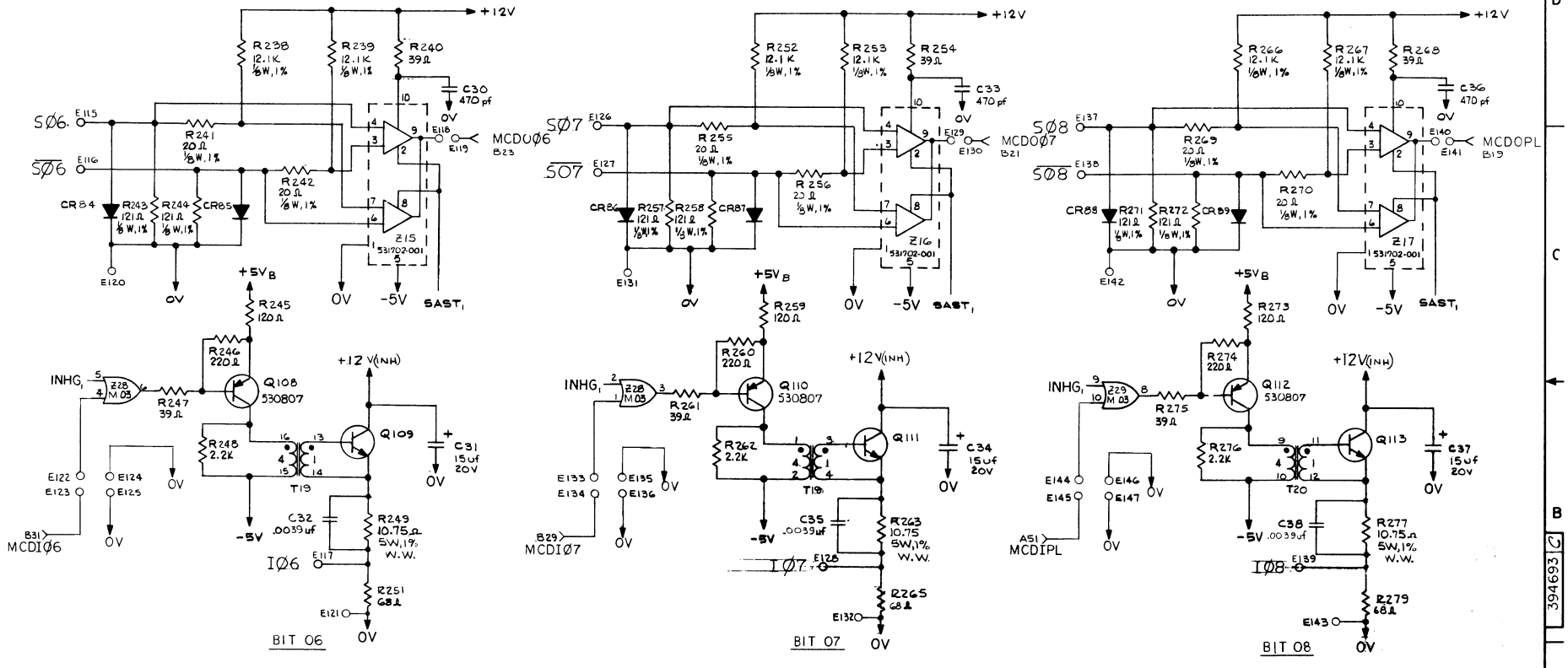
RAYTHEON COMPANY LEXINGTON, MASSACHUSETTS 02173

MEMORY BOARD (SCHEMATIC DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	394693
SCALE NONE		SHEET 6

RAYTHEON COMPUTER FORM 67-0076


+12V
R196 12.1K 1/8W,1%
R197 12.1K 1/8W,1%
R198 39Ω
C21 470 pf
SØ3
E82
SØ3
E83
R199 20Ω 1/8W,1%
R200 20Ω 1/8W,1%
CR78
R201 121Ω 1/8W,1%
R202 121Ω 1/8W,1%
CR79
E87
E85
E86
B47
MCDØØ3
Z12 5317702-001
0V
-5V
SAST1
+5VB
R203 120Ω
R204 220Ω
INHG1
Z27 M05
R205 39Ω
Q102 530807
+12V(INH)
Q103
C22 15UF 20V
E89
E90
E91
E92
B49
MCDIØ3
R206 2.2K
T18
C23 .0039uf
R207 10.75Ω 5W,1% W.W.
IØ3
E84
R209 68Ω
E88
BIT 03
R210 12.1K 1/8W,1%
R211 12.1K 1/8W,1%
R212 39Ω
C24 470 pf
SØ4
E93
SØ4
E94
R213 20Ω 1/8W,1%
R214 20Ω 1/8W,1%
CR80
R215 121Ω 1/8W,1%
R216 121Ω 1/8W,1%
CR81
E96
E97
B45
MCDØØ4
Z13 5317702-001
E98
R217 120Ω
R218 220Ω
Q104 530807
Q105
C25 15UF 20V
R219 39Ω
R220 2.2K
T19
C26 .0039uf
R221 10.75Ω 5W,1% W.W.
IØ4
E95
R223 68Ω
E99
B27
MCDIØ4
E100
E101
E102
E103
BIT 04
R224 12.1K 1/8W,1%
R225 12.1K 1/8W,1%
R226 39Ω
C27 470 pf
SØ5
E104
SØ5
E105
R227 20Ω 1/8W,1%
R228 20Ω 1/8W,1%
CR82
R229 121Ω 1/8W,1%
R230 121Ω 1/8W,1%
CR83
E107
E108
B33
MCDØØ5
Z14 5317702-001
E109
R231 120Ω
R232 220Ω
Q106 530807
Q107
C28 15uf 20V
R233 39Ω
R234 2.2K
T19
C29 .0039uf
R235 10.75Ω 5W,1% W.W
IØ5
E106
R237 68Ω
E110
B25
MCDIØ5
E111
E112
E113
E114
BIT 05
DATA LOOP
RESERVE ECO'S OUTSTANDING
REVISIONS
SYM DESCRIPTION MAKE USE DRAWN CHECK APPR DATE
SEE SHEET 1 RWB
NOTES: UNLESS OTHERWISE SPECIFIED.
QTY REQD PART OR IDENTIFYING NO. NOMENCLATURE OR DESCRIPTION MATERIAL CKT REF ZONE ITEM NO.
LIST OF MATERIALS OR PARTS LIST
UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:
DRAWN 7/19/70
CHECK 7/20/70
APPR 7/20/70
APPR
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF RAYTHEON COMPANY, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, RAYTHEON COMPANY RESERVES ALL PATENT, SALE, PROPRIETARY DESIGN, MANUFACTURING, USE & REPRODUCTION RIGHTS THERETO.
NEXT ASSY 394691
RAYTHEON COMPANY LEXINGTON, MASSACHUSETTS 02173
MEMORY BOARD (SCHEMATIC DIAGRAM)
CODE IDENT NO. 49956
SIZE D
394693
SCALE NONE
SHEET 7
RAYTHEON COMPUTER FORM 67-0078
394693C



DATA LOOP

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	SEE SHEET 1			RWB			

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	DKT REF	ZONE	ITEM NO.

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN R.W. Bowman 3/10/70
CHECK 3/19/70
APPR 3/25/70
APPR

THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF RAYTHEON COMPANY, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, RAYTHEON COMPANY RESERVES ALL PATENT, SALE, PROPRIETARY DESIGN, MANUFACTURING, USE & REPRODUCTION RIGHTS THEREIN.

NEXT ASSY 394691

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

MEMORY BOARD (SCHEMATIC DIAGRAM)

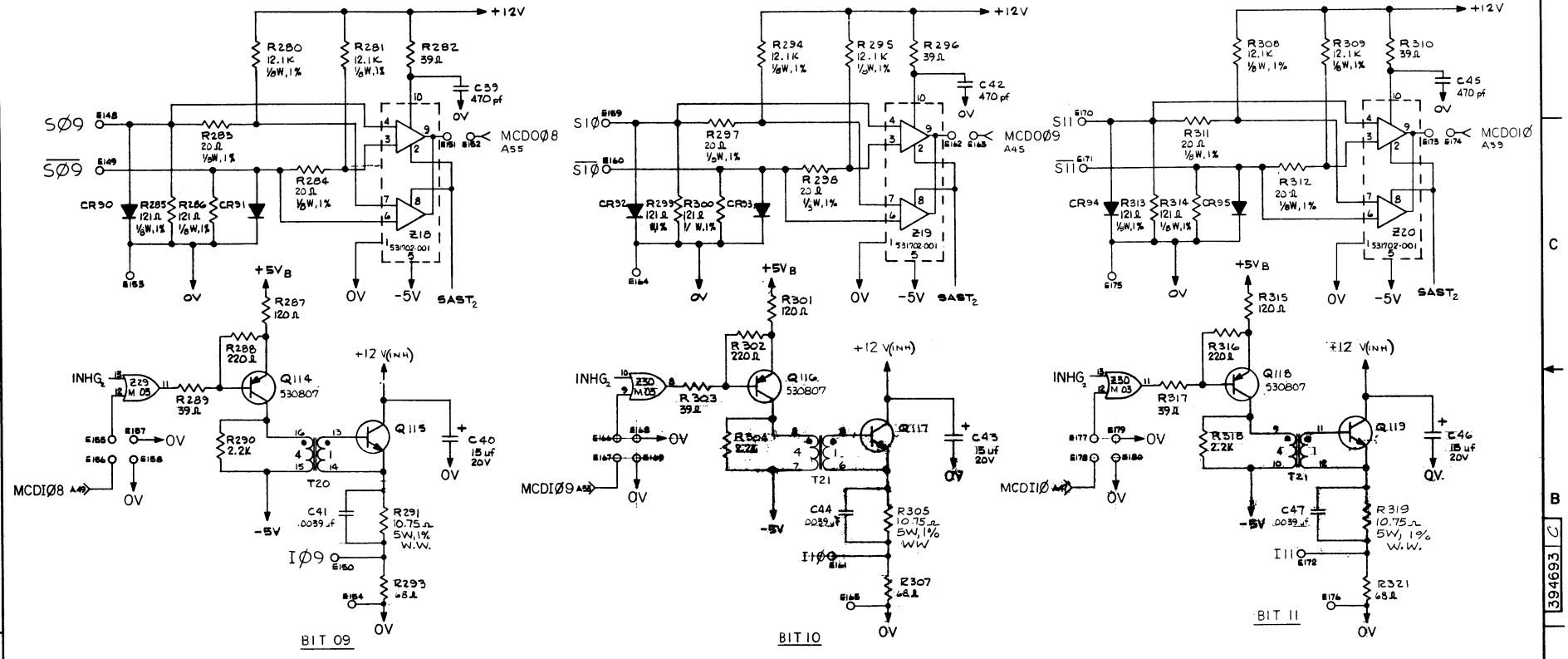
CODE IDENT NO. 49956 | SIZE D | 394693

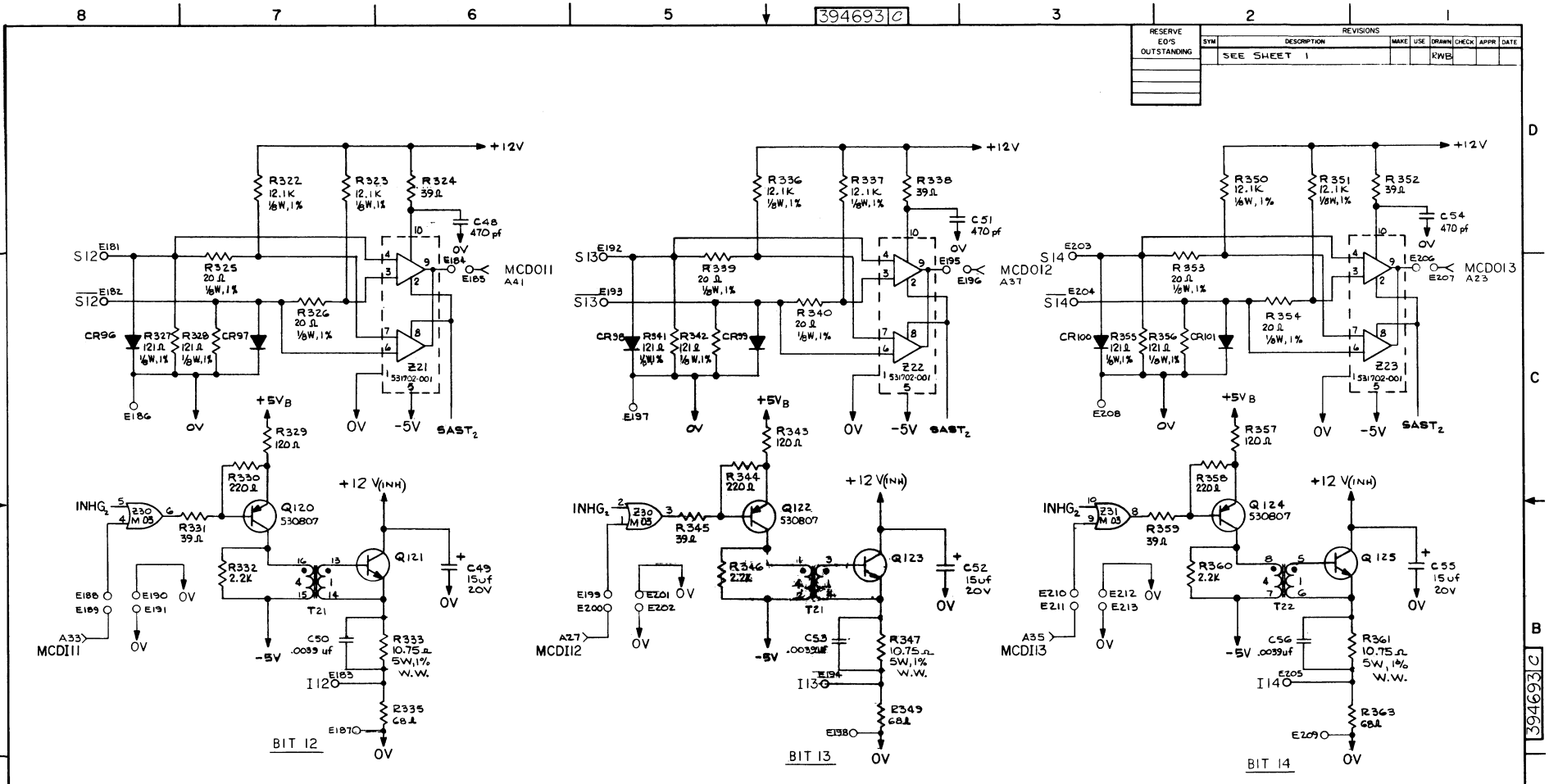
SCALE NONE | SHEET 8

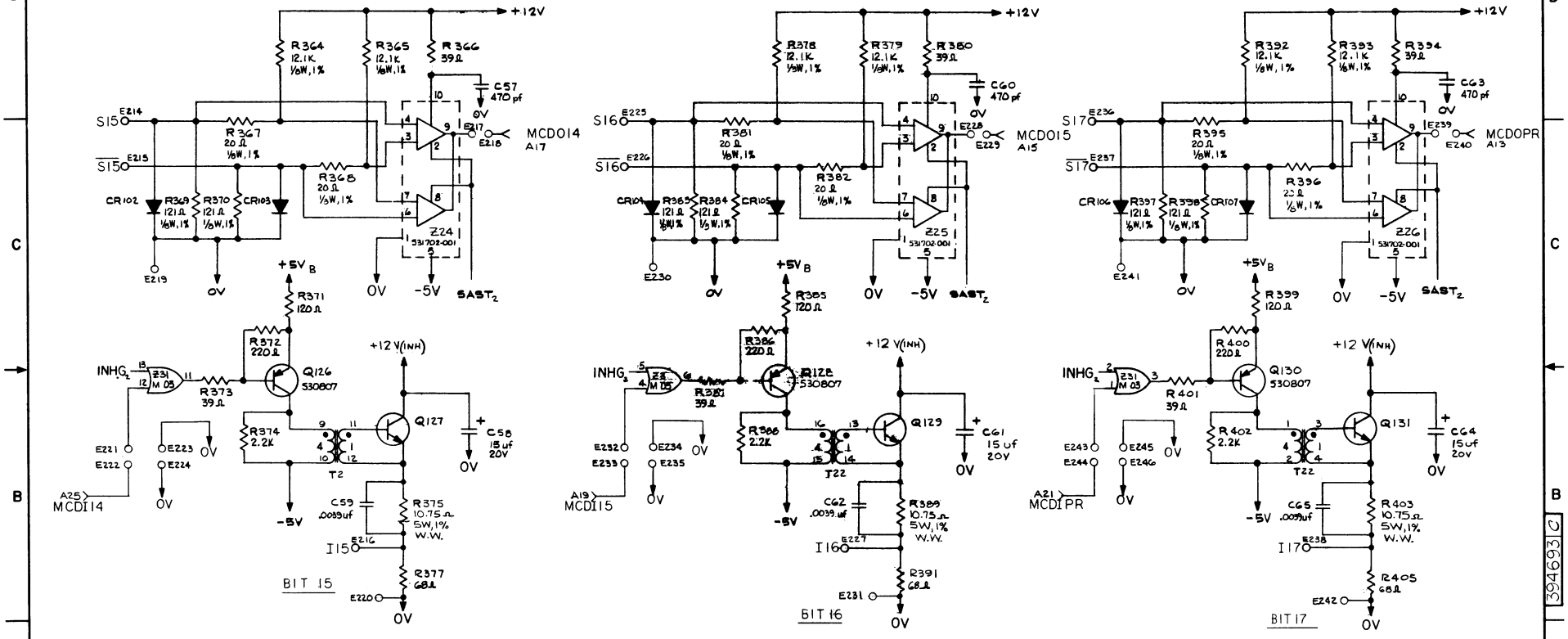
RAYTHEON COMPUTER FORM 87-0075

NOTES: UNLESS OTHERWISE SPECIFIED.

394693 C


+12V
R280 12.1K 1/8W,1%
R281 12.1K 1/8W,1%
R282 39Ω
C39 470 pf
S Ø 9
S Ø 9
R285 20Ω 1/8W,1%
R284 20Ω 1/8W,1%
CR90
R285 121Ω 1/8W,1%
R286 121Ω 1/8W,1%
CR91
MCDØØ8 A55
Z18 531702-001
+5V B
R287 120Ω
R288 220Ω
INHG2
Z29 M 05
R289 39Ω
Q114 530807
+12 V(INH)
R290 2.2K
Q115
C40 15 uf 20V
T20
C41 .0039 uf
R291 10.75Ω 5W,1% W.W.
I Ø 9
R293 68Ω
MCDIØ8 A49
BIT 09
S1Ø
S1Ø
R294 12.1K 1/8W,1%
R295 12.1K 1/8W,1%
R296 39Ω
C42 470 pf
R297 20Ω 1/8W,1%
R298 20Ω 1/8W,1%
CR92
R299 121Ω 1/8W,1%
R300 121Ω 1/8W,1%
CR93
MCDØØ9 A45
Z19 531702-001
R301 120Ω
R302 220Ω
INHG2
Z30 M 05
R303 39Ω
Q116 530807
+12 V(INH)
R304 2.2K
Q117
C43 15 uf 20V
T21
C44 .0039 uf
R305 10.75Ω 5W,1% WW
R307 68Ω
MCDIØ9 A54
BIT 10
S11
S11
R308 12.1K 1/8W,1%
R309 12.1K 1/8W,1%
R310 39Ω
C45 470 pf
R311 20Ω 1/8W,1%
R312 20Ω 1/8W,1%
CR94
R313 121Ω 1/8W,1%
R314 121Ω 1/8W,1%
CR95
MCDIØØ A39
Z20 531702-001
R315 120Ω
R316 220Ω
INHG2
Z30 M 05
R317 39Ω
Q118 530807
+12 V(INH)
R318 2.2K
Q119
C46 15 uf 20V
T21
C47 .0039 uf
R319 10.75Ω 5W,1% W.W.
I 11
R321 68Ω
MCDIIØ A40
BIT 11
0V
-5V
SAST2
DATA LOOP
394693 C
RESERVE EO'S OUTSTANDING
REVISIONS
SYM DESCRIPTION MAKE USE DRAWN CHECK APPR DATE
SEE SHEET 1 RWB
QTY REQD PART OR IDENTIFYING NO. NOMENCLATURE OR DESCRIPTION MATERIAL CKT REF ZONE ITEM NO.
LIST OF MATERIALS OR PARTS LIST
UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:
DRAWN 3/19/70
CHECK 3/19/70
APPR 3/19/70
APPR
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF RAYTHEON COMPANY, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, RAYTHEON COMPANY RESERVES ALL PATENT, SALE, PROPRIETARY DESIGN, MANUFACTURING, USE & REPRODUCTION RIGHTS THERETO.
NEXT ASSY 394691
RAYTHEON
RAYTHEON COMPANY LEXINGTON, MASSACHUSETTS 02173
MEMORY BOARD (SCHEMATIC DIAGRAM)
CODE IDENT NO. 49956
SIZE D
394693
SCALE NONE
SHEET 9
RAYTHEON COMPUTER FORM 67-0078
NOTES: UNLESS OTHERWISE SPECIFIED.


394693 C
RESERVE EO'S OUTSTANDING
REVISIONS
SYM DESCRIPTION MAKE USE DRAWN CHECK APPR DATE
SEE SHEET 1 RWB
+12V
R322 12.1K 1/8W,1%
R323 12.1K 1/8W,1%
R324 39Ω
C48 470 pf
S12 E181
S12 E182
R325 20Ω 1/8W,1%
R326 20Ω 1/8W,1%
E184
E185
MCD011 A41
CR96 R327 121Ω 1/8W,1% R328 121Ω 1/8W,1% CR97
Z21 531702-001
E186
0V
-5V
SAST2
+5VB
R329 120Ω
R330 220Ω
INHG2
Z30 M 05
R331 39Ω
Q120 530807
+12 V(INH)
Q121
R332 2.2K
T21
C49 15uf 20V
E188
E189
E190
E191
A33 MCD111
C50 .0039 uf
R333 10.75Ω 5W,1% W.W.
I12
E183
Z335 68Ω
E187
BIT 12
R336 12.1K 1/8W,1%
R337 12.1K 1/8W,1%
R338 39Ω
C51 470 pf
S13 E192
S13 E193
R339 20Ω 1/8W,1%
R340 20Ω 1/8W,1%
E195
E196
MCD012 A37
CR98 R341 121Ω 1/8W,1% R342 121Ω 1/8W,1% CR99
Z22 531702-001
E197
R343 120Ω
R344 220Ω
Q122 530807
Q123
R346 2.2K
T21
C52 15uf 20V
E199
E200
E201
E202
A27 MCD012
C53 .0039uf
R347 10.75Ω 5W,1% W.W.
I13
E194
Z349 68Ω
E198
BIT 13
R350 12.1K 1/8W,1%
R351 12.1K 1/8W,1%
R352 39Ω
C54 470 pf
S14 E203
S14 E204
R353 20Ω 1/8W,1%
R354 20Ω 1/8W,1%
E206
E207
MCD013 A23
CR100 R355 121Ω 1/8W,1% R356 121Ω 1/8W,1% CR101
Z23 531702-001
E208
R357 120Ω
R358 220Ω
Q124 530807
Q125
R360 2.2K
T22
C55 15uf 20V
E210
E211
E212
E213
A35 MCD013
C56 .0039uf
R361 10.75Ω 5W,1% W.W.
I14
E205
Z363 68Ω
E209
BIT 14
394693 C
DATA LOOP
QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL | CKT REF | ZONE | ITEM NO.
LIST OF MATERIALS OR PARTS LIST
UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:
DRAWN R. Bowman 2/19/70
CHECK M. Bardis 3/9/70
APPR H. Lawin 3/25/70
APPR
THE INFORMATION DISCLOSED HEREIN WAS ORIGINATED BY AND IS THE PROPERTY OF RAYTHEON COMPANY, AND EXCEPT FOR RIGHTS EXPRESSLY GRANTED TO THE UNITED STATES GOVERNMENT, RAYTHEON COMPANY RESERVES ALL PATENT, SALE, PROPRIETARY, DESIGN, MANUFACTURING, USE & REPRODUCTION RIGHTS THERETO.
NEXT ASSY 394691
RAYTHEON
RAYTHEON COMPANY LEXINGTON, MASSACHUSETTS 02173
MEMORY BOARD SCHEMATIC DIAGRAM)
CODE IDENT NO. 49956
SIZE D
394693
SCALE NONE
SHEET 10
RAYTHEON COMPUTER FORM 67-0078
NOTES: UNLESS OTHERWISE SPECIFIED.



DATA LOOP

RESERVE EO's OUTSTANDING

REVISIONS								
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
.	SEE SHEET 1			RWB			

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
LIST OF MATERIALS OR PARTS LIST						

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010; ANGLES ±0° 30'
2. BREAK SHARP CORNERS .015 MAX
FINISH:

DRAWN	[illegible]	3/9/70
CHECK	M. Burton	4/3/70
APPR	[illegible]	3/25/70
APPR		

NEXT ASSY 394691

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

MEMORY BOARD (SCHEMATIC DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	394693
SCALE NONE		SHEET 11

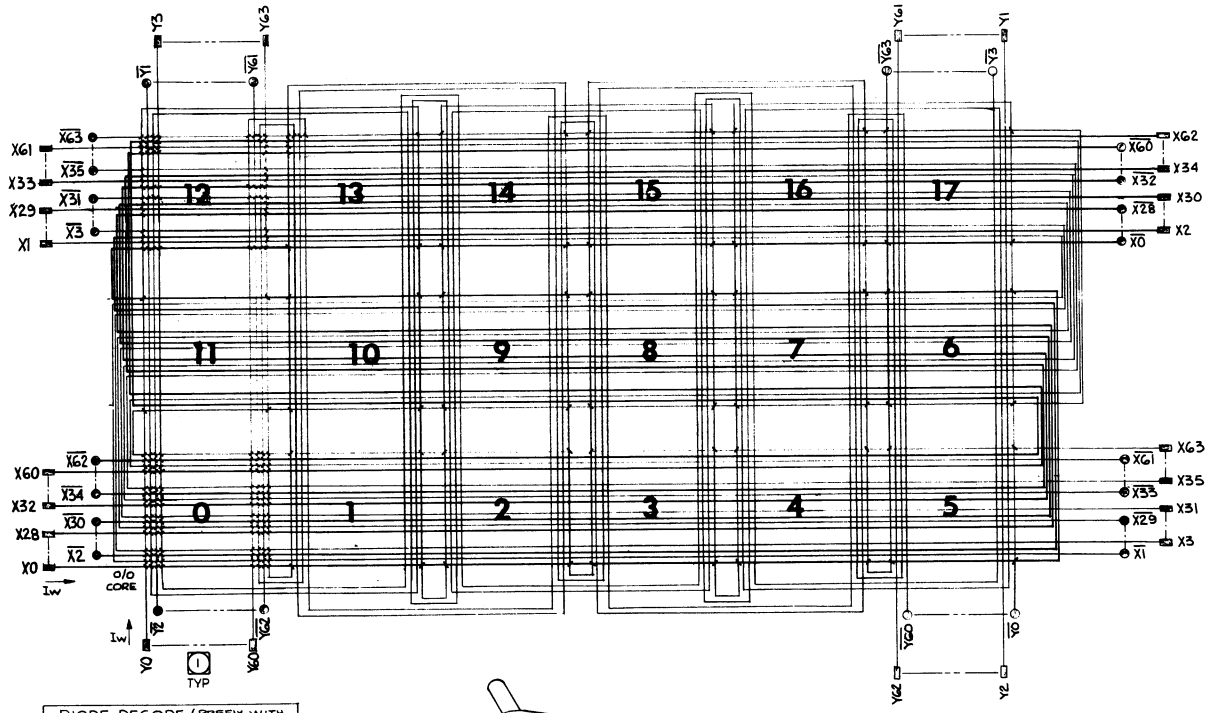
RAYTHEON COMPUTER FORM 67-0075

394693C

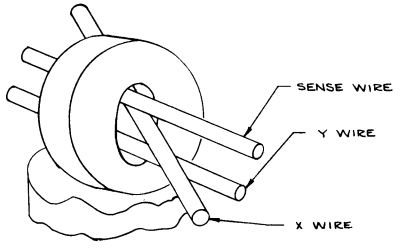
NOTES: UNLESS OTHERWISE SPECIFIED.

RESERVE EO'S OUTSTANDING

REVISIONS							
SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
X1	APPROVAL PER EO 19796			RB	[illegible]	[illegible]	1/8/70
A	RELEASED PER EO 19303			PF	[illegible]	[illegible]	7/9/70



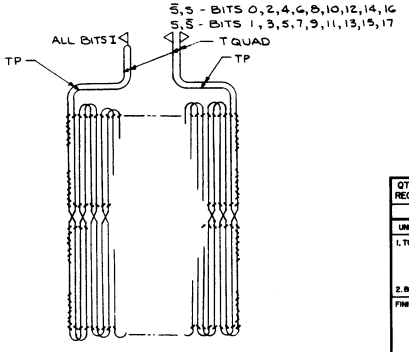
DIODE DECODE (PREFIX WITH X OR Y FOR COMPLETE DESIGNATION)								
CA0/CC0	0	4	8	12	16	20	24	28
CA1/CC1	1	5	9	13	17	21	25	29
CA2/CC2	2	6	10	14	18	22	26	30
CA3/CC3	3	7	11	15	19	23	27	31
CA4/CC4	60	56	52	48	44	40	36	32
CA5/CC5	61	57	53	49	45	41	37	33
CA6/CC6	62	58	54	50	46	42	38	34
CA7/CC7	63	59	54	51	47	43	39	35
	S0	S1	S2	S3	S4	S5	S6	S7



WIRE LAY

WIRING SEQUENCE

1. Y
2. X
3. SENSE / INHIBIT



	YO	YG3
X0	1	0
	1	0
	1	0
X31	1	0
X32	0	1
	0	1
	0	1
X63	0	1

WCP

2. DRIVE CURRENT POLARITIES ARE NEGATIVE READ AND POSITIVE WRITE.

(1) GROUPINGS SHOWN WITH PHANTOM LINES ARE IN SEQUENCE IN INCREMENTS OF 4 :
i.e. X0 | X1 | X2 | X3
X4 | X5 | X6 | X7
X8 | X9 | X10 | X11 ETC.

NOTES: UNLESS OTHERWISE SPECIFIED.

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	CKT REF	ZONE	ITEM NO.
		LIST OF MATERIALS OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS .XX ±.03 .XXX ±.010 ANGLES ±0° 30'
2. BREAK SHARP CORNERS .005 MAX
FINISH:

DRAWN	[illegible]	11/27/69
CHECK	[illegible]	2-3-70
APPR	[illegible]	11-28-69
APPR	R. ALLEN	2-4-70

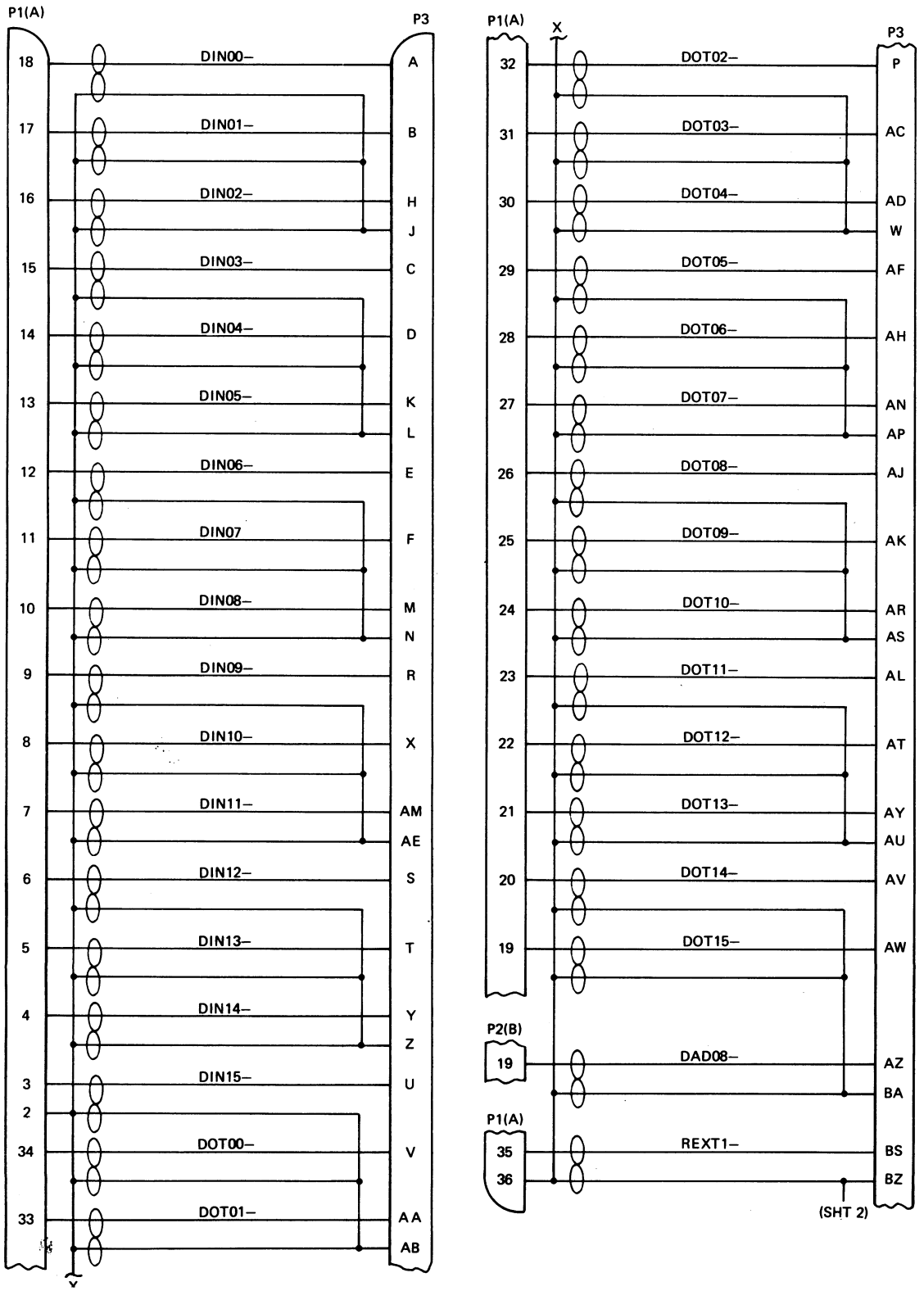
NEXT ASSY 394690

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

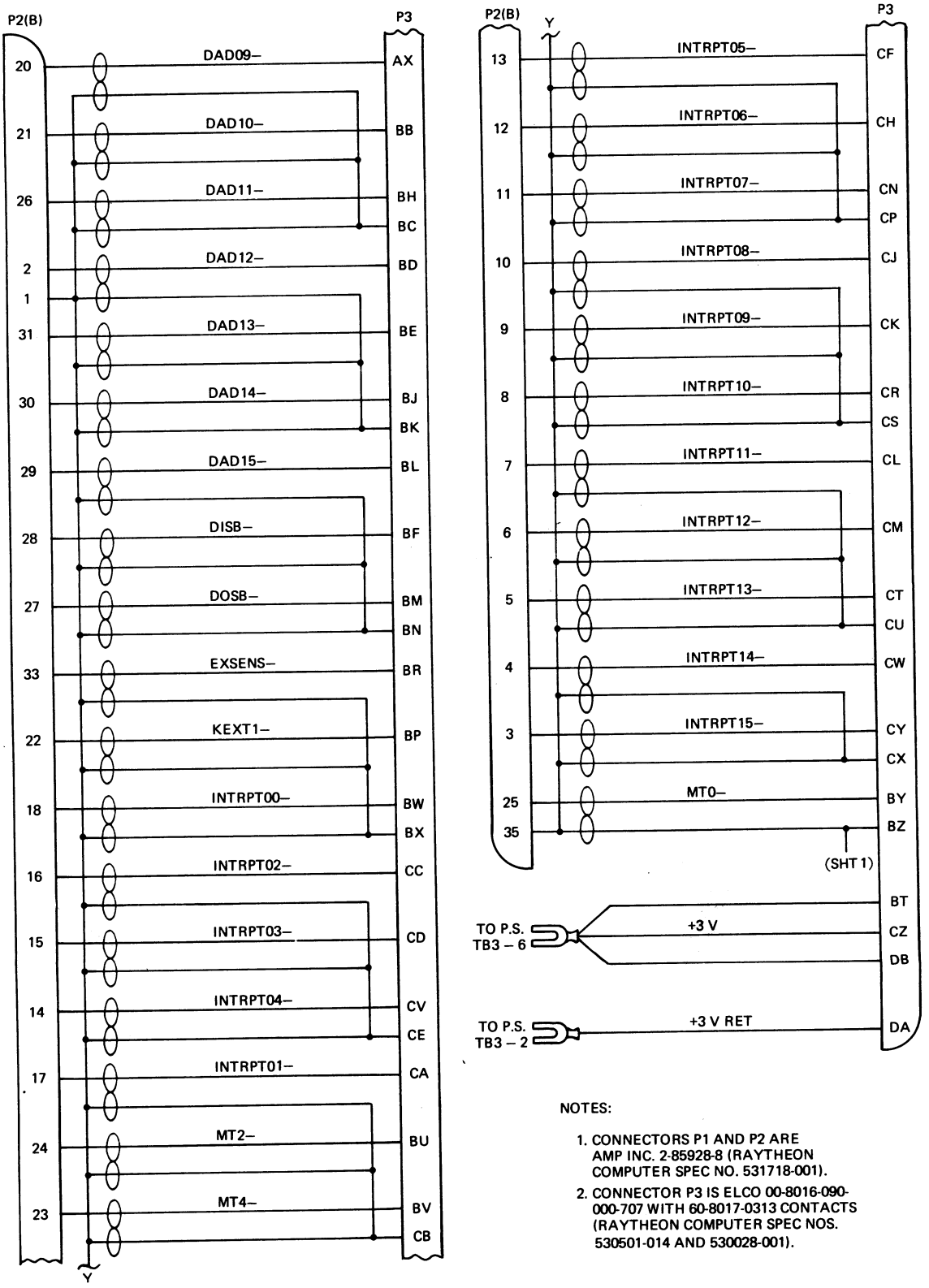
STACK, 4K x 18 BIT (WIRING DIAGRAM)

CODE IDENT NO.	SIZE	
49956	D	394696
SCALE NONE		SHEET 1 OF 1

RAYTHEON COMPUTER FORM 87-0075



Drawing 545013. DIO Connector Cable (Sheet 1 of 2)



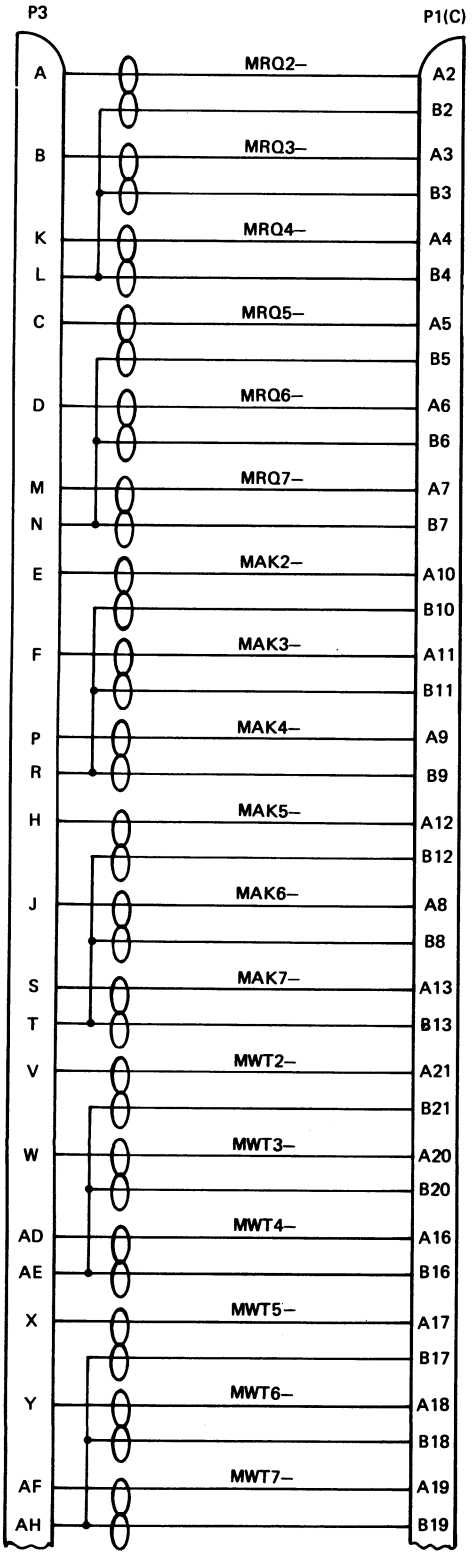
NOTES:

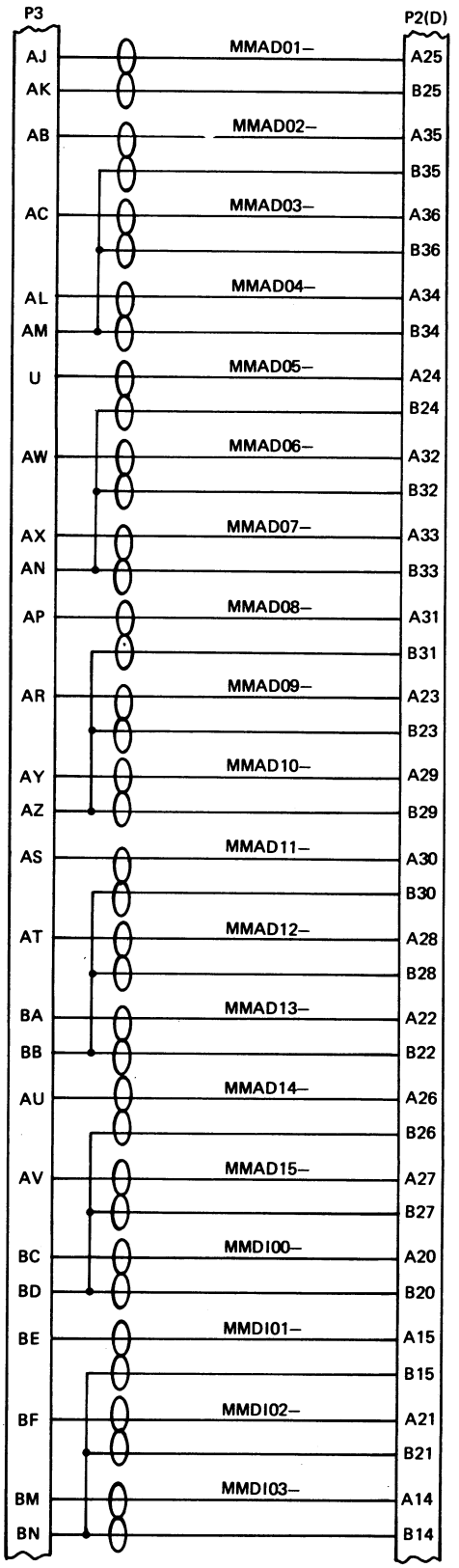
1. CONNECTORS P1 AND P2 ARE AMP INC. 2-85928-8 (RAYTHEON COMPUTER SPEC NO. 531718-001).
2. CONNECTOR P3 IS ELCO 00-8016-090-000-707 WITH 60-8017-0313 CONTACTS (RAYTHEON COMPUTER SPEC NOS. 530501-014 AND 530028-001).

Drawing 545013. DIO Connector Cable (Sheet 2 of 2)

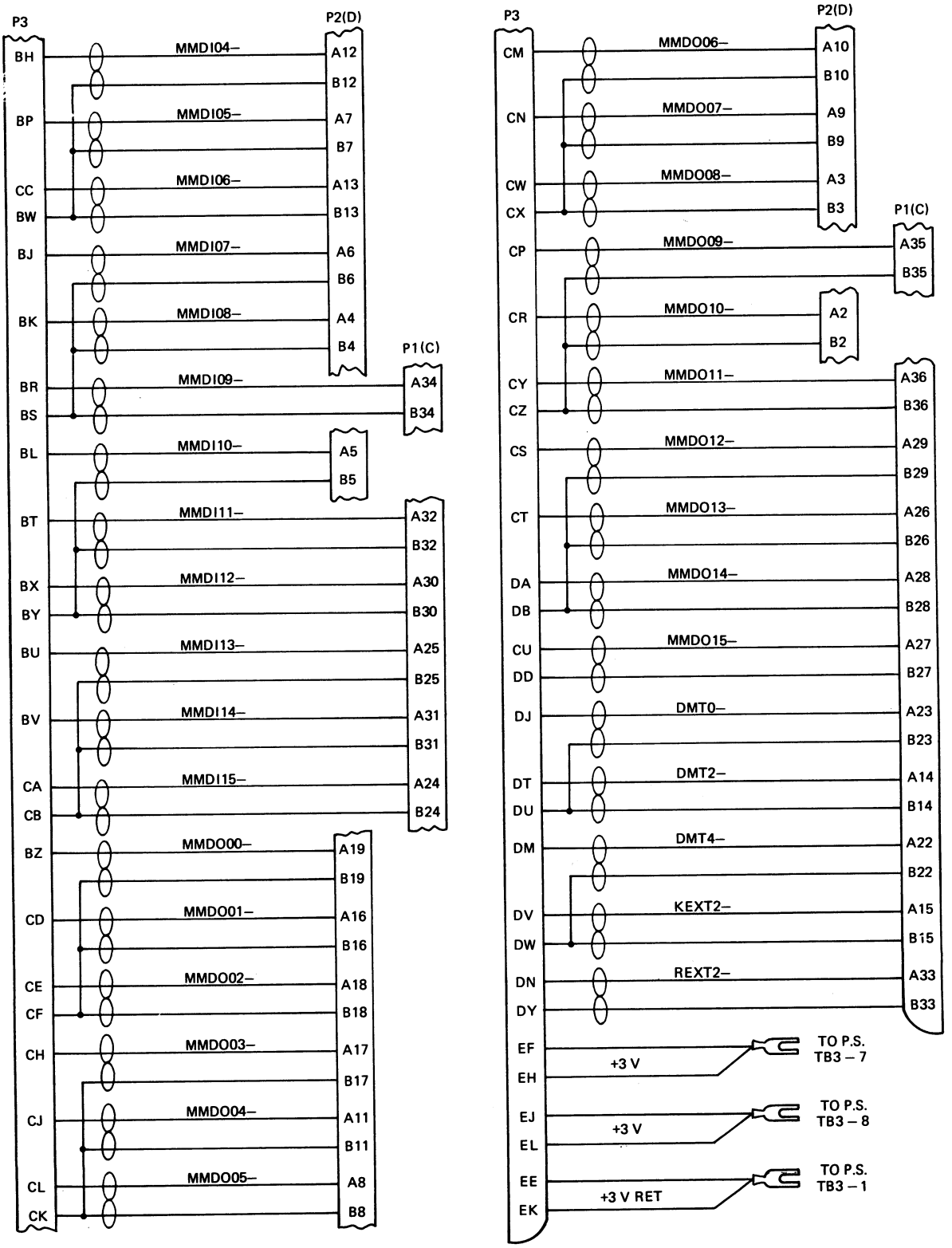
NOTES:

1. CONNECTORS P1 AND P2 ARE VIKING INDUSTRIES 2VH36/1JN5 (RAYTHEON COMPUTER SPEC NO. 531714-002).
2. CONNECTOR P3 IS ELCO 00-8016-120-000-707 WITH 60-8017-0313 CONTACTS (RAYTHEON COMPUTER SPEC NOS. 530501-006 AND 530028-001).

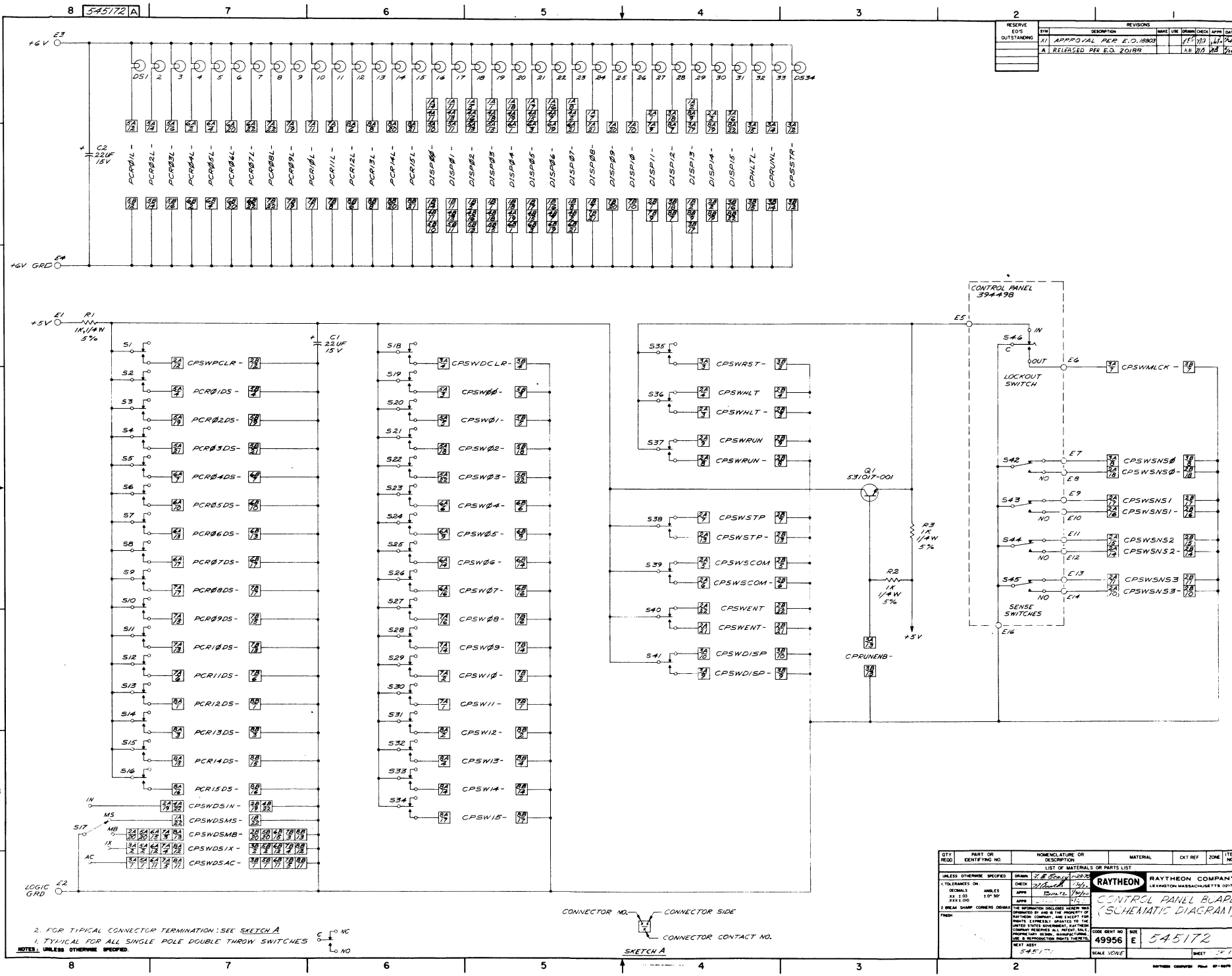


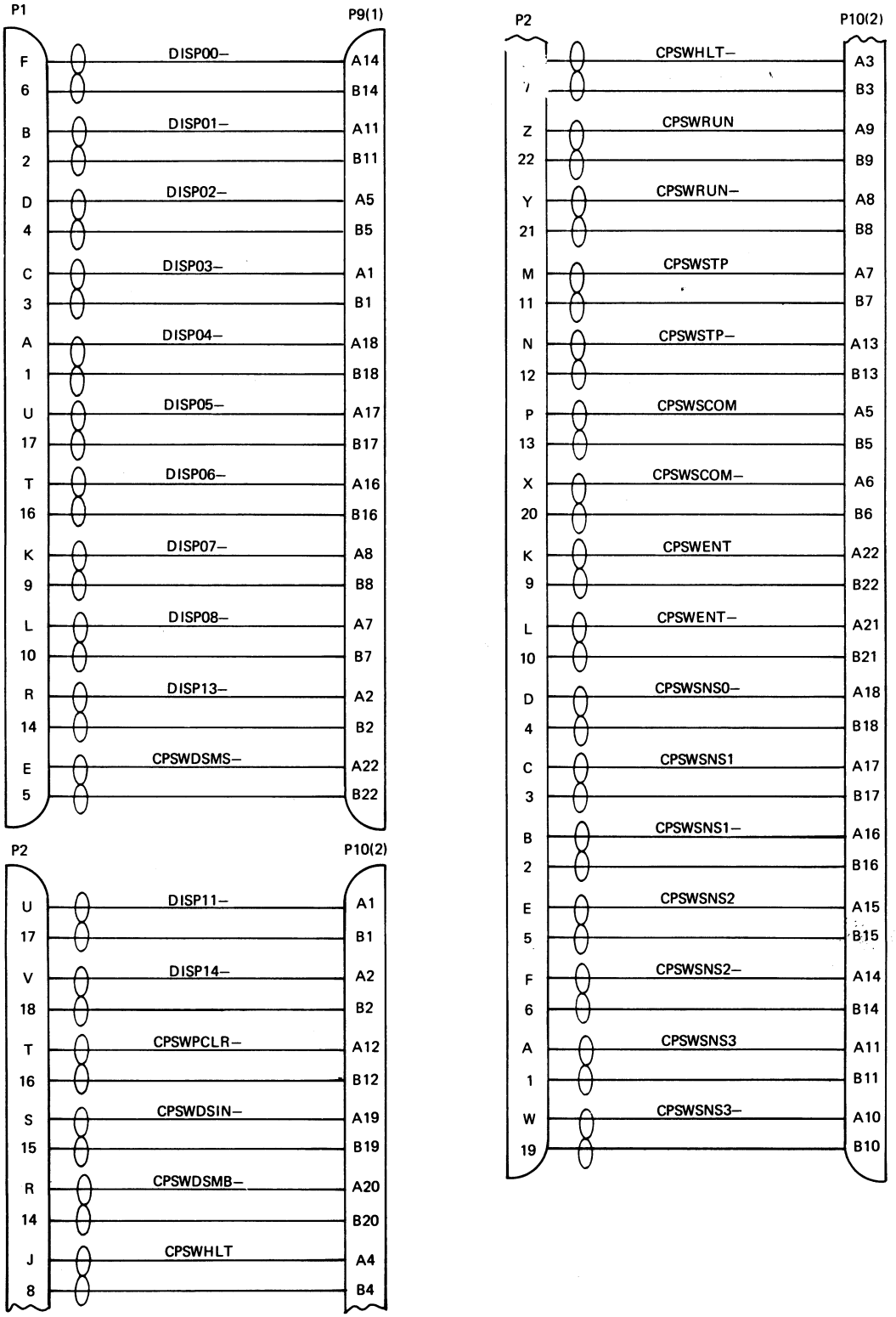


Drawing 545030. DMA Connector Cable (Sheet 1 of 2)



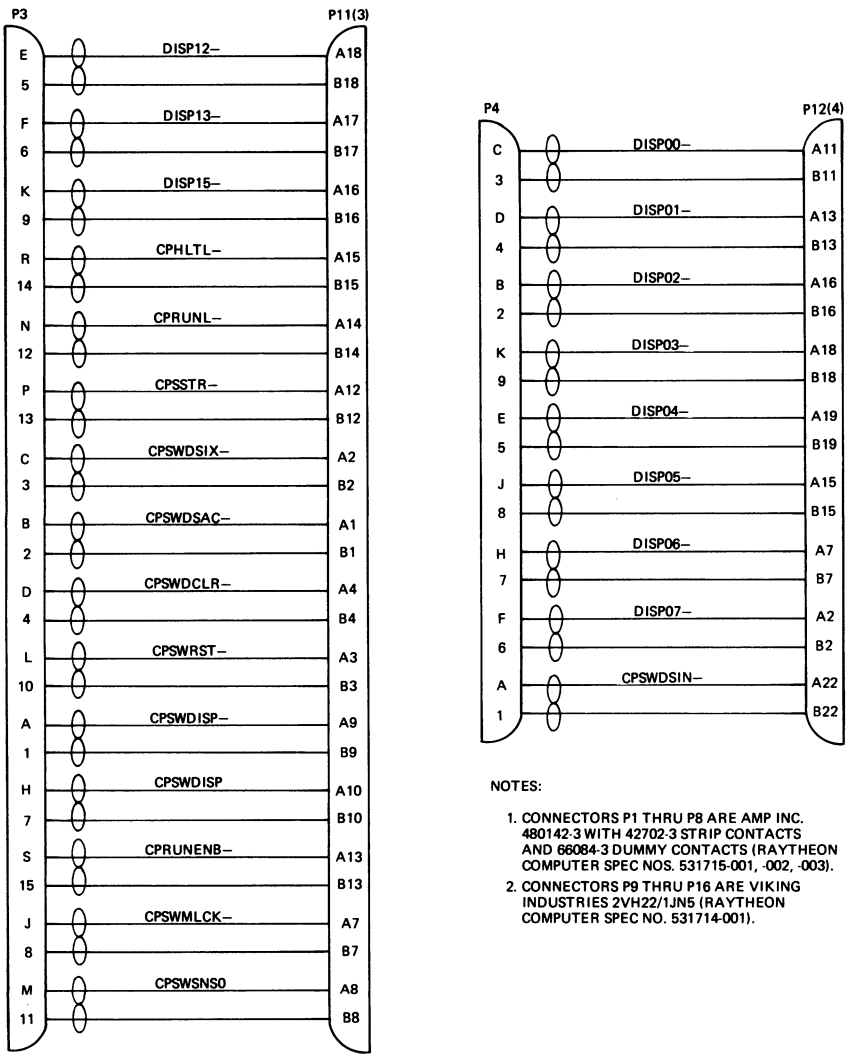
Drawing 545030. DMA Connector Cable (Sheet 2 of 2)


545172 A
REVISIONS
RESERVE EOS OUTSTANDING
SYM DESCRIPTION MAKE USE DRAWN CHECK APPR DATE
X1 APPROVAL PER E.O. 19803
A RELEASED PER E.O. 20199
+6V
+6V GRD
C2 22UF 15V
DS1 DS34
PCRØ1L PCRØ2L PCRØ3L PCRØ4L PCRØ5L PCRØ6L PCRØ7L PCRØ8L PCRØ9L PCRIØL PCRIIL PCRI2L PCRI3L PCRI4L PCRI5L
DISPØØ- DISPØ1- DISPØ2- DISPØ3- DISPØ4- DISPØ5- DISPØ6- DISPØ7- DISPØ8- DISPØ9- DISPIØ- DISPII- DISPI2- DISPI3- DISPI4- DISPI5- CPHLTL- CPRUNL- CPSSTR-
+5V
R1 1K, 1/4W 5%
C1 22UF 15V
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16
PCRØ1DS- PCRØ2DS- PCRØ3DS- PCRØ4DS- PCRØ5DS- PCRØ6DS- PCRØ7DS- PCRØ8DS- PCRØ9DS- PCRIØDS- PCRIIDS- PCRI2DS- PCRI3DS- PCRI4DS- PCRI5DS-
S17 IN MS MB IX AC
CPSWDSIN- CPSWDSMS- CPSWDSMB- CPSWDSIX- CPSWDSAC-
LOGIC GRD
S18 S19 S20 S21 S22 S23 S24 S25 S26 S27 S28 S29 S30 S31 S32 S33 S34
CPSWDCLR- CPSWØØ- CPSWØ1- CPSWØ2- CPSWØ3- CPSWØ4- CPSWØ5- CPSWØ6- CPSWØ7- CPSWØ8- CPSWØ9- CPSWIØ- CPSWII- CPSWI2- CPSWI3- CPSWI4- CPSWI5-
S35 S36 S37 S38 S39 S40 S41
CPSWRST- CPSWALT CPSWHLT- CPSWRUN CPSWRUN- CPSWSTP CPSWSTP- CPSWSCOM CPSWSCOM- CPSWENT CPSWENT- CPSWDISP CPSWDISP-
Q1 531017-001
R3 1K 1/4W 5%
R2 1K 1/4W 5%
CPRUNENB-
CONTROL PANEL 394498
E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E16
S46 IN C OUT
LOCKOUT SWITCH
CPSWMLCK -
S42 S43 S44 S45 NO
CPSWSNSØ CPSWSNSØ- CPSWSNS1 CPSWSNS1- CPSWSNS2 CPSWSNS2- CPSWSNS3 CPSWSNS3-
SENSE SWITCHES
CONNECTOR NO. CONNECTOR SIDE CONNECTOR CONTACT NO.
SKETCH A
C NC NO
2. FOR TYPICAL CONNECTOR TERMINATION: SEE SKETCH A
1. TYPICAL FOR ALL SINGLE POLE DOUBLE THROW SWITCHES
NOTES: UNLESS OTHERWISE SPECIFIED.
QTY REQD PART OR IDENTIFYING NO. NOMENCLATURE OR DESCRIPTION MATERIAL CKT REF ZONE ITEM NO.
LIST OF MATERIALS OR PARTS LIST
UNLESS OTHERWISE SPECIFIED
1. TOLERANCES ON: DECIMALS ANGLES XX ± .03 ± 0° 30' XXX ± .010
2. BREAK SHARP CORNERS .008 MAX
FINISH
DRAWN CHECK APPR APPR
RAYTHEON COMPANY LEXINGTON MASSACHUSETTS 02173
CONTROL PANEL BOARD (SCHEMATIC DIAGRAM)
CODE IDENT NO 49956 SIZE E 545172
SCALE NONE SHEET 1 OF 1
545172 A
6-182



Drawing 545217. Control Panel Signal Harness (Sheet 1 of 4)

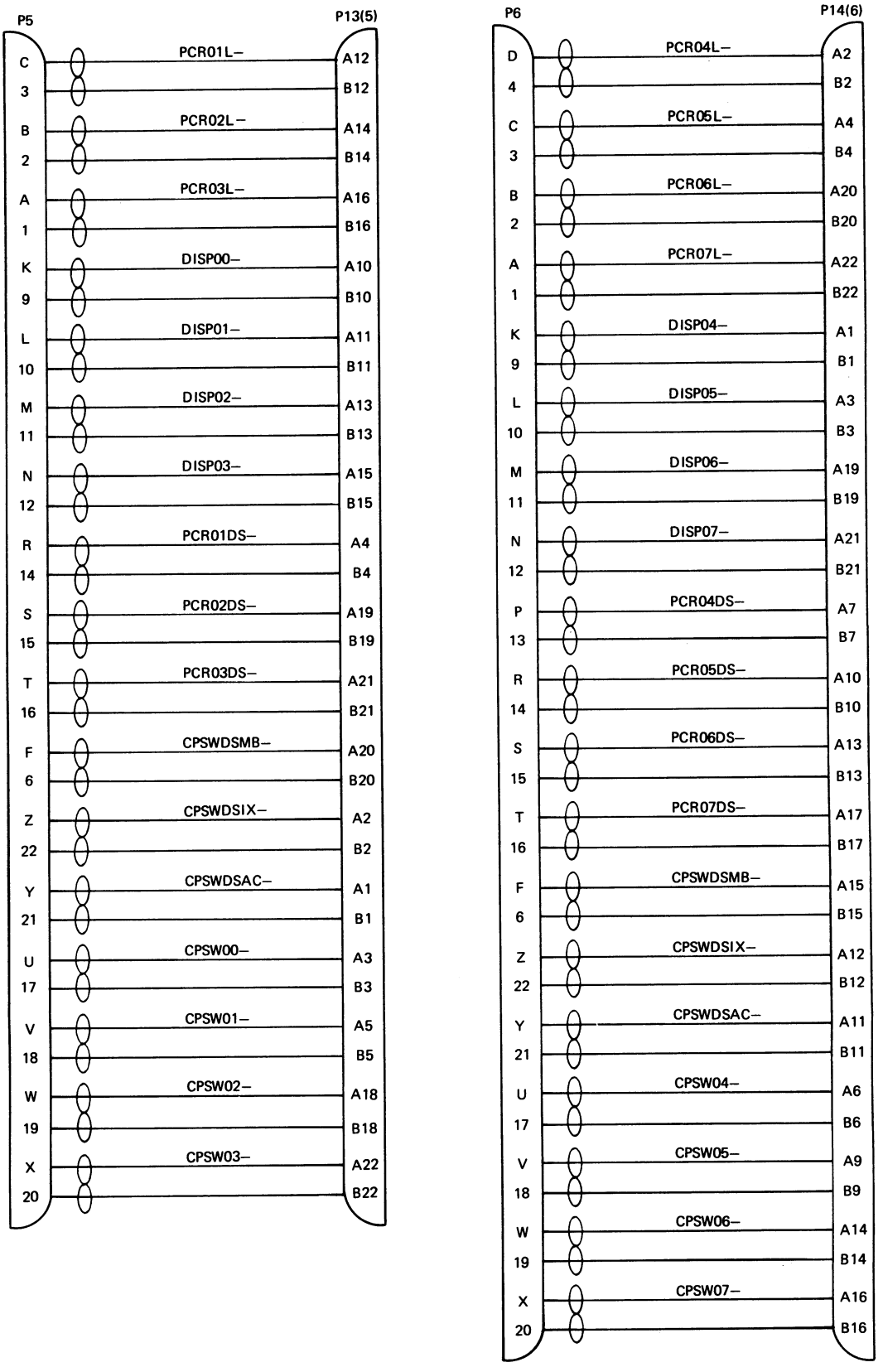
Hardware Rechner



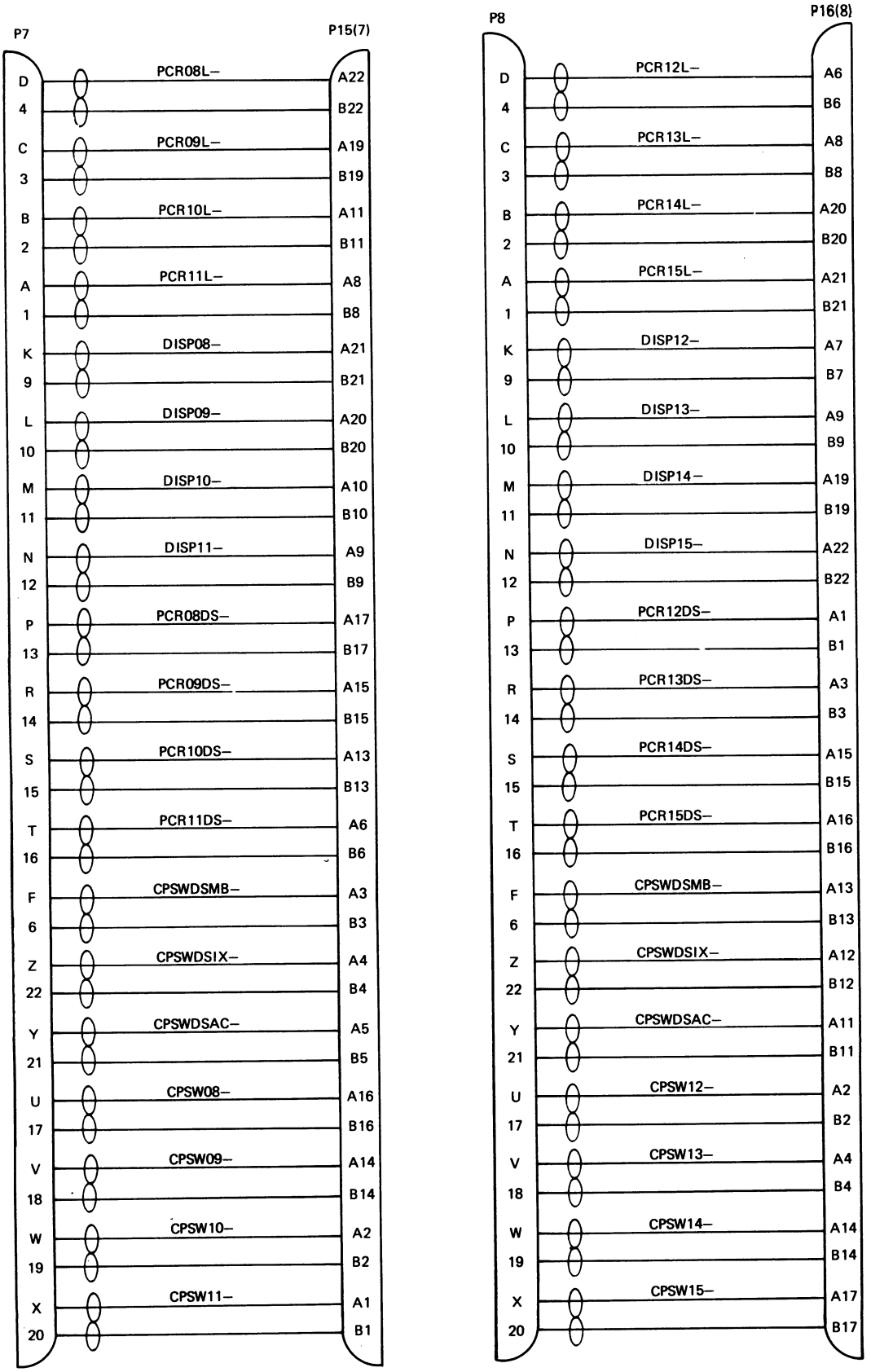
NOTES:

1. CONNECTORS P1 THRU P8 ARE AMP INC. 480142-3 WITH 42702-3 STRIP CONTACTS AND 66084-3 DUMMY CONTACTS (RAYTHEON COMPUTER SPEC NOS. 531715-001, -002, -003).
2. CONNECTORS P9 THRU P16 ARE VIKING INDUSTRIES 2VH22/1JN5 (RAYTHEON COMPUTER SPEC NO. 531714-001).

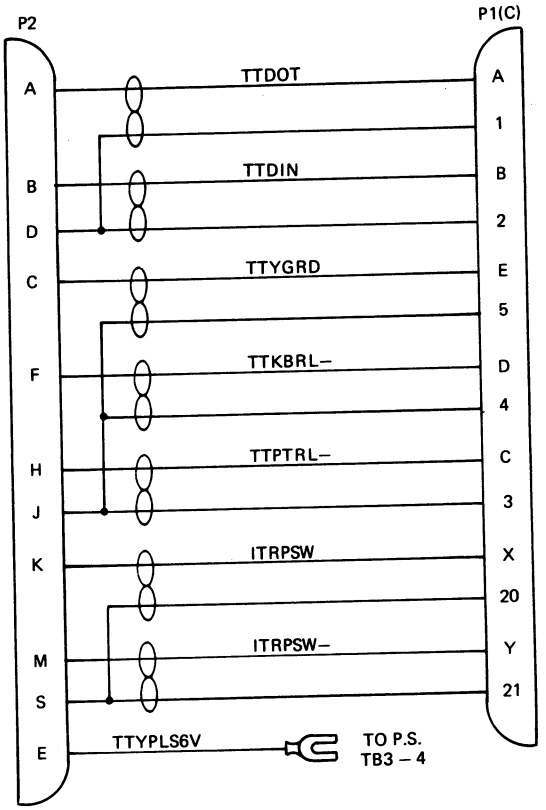
Drawing 545217. Control Panel Signal Harness (Sheet 2 of 4)



Drawing 545217. Control Panel Signal Harness (Sheet 3 of 4)



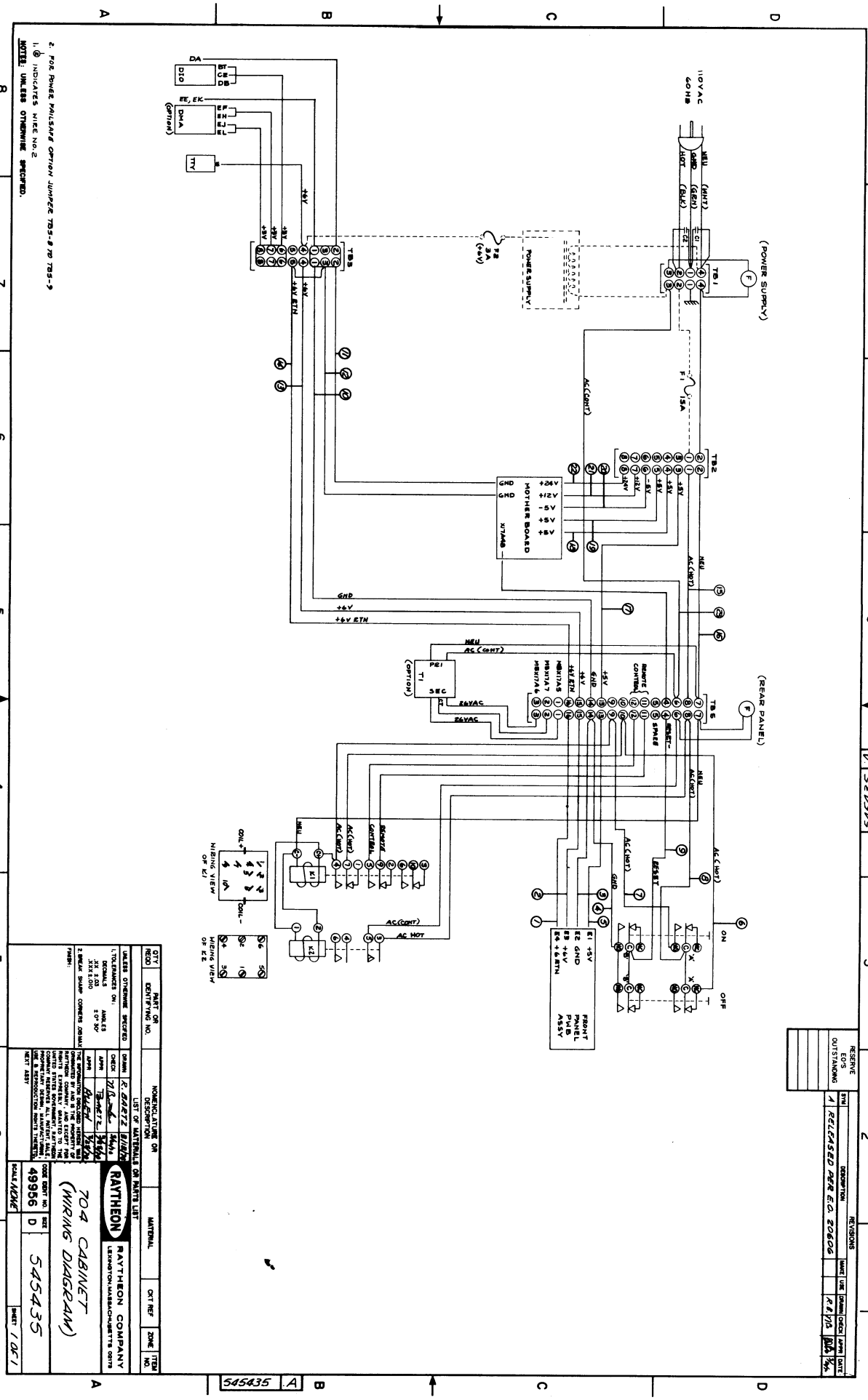
Drawing 545217. Control Panel Signal Harness (Sheet 4 of 4)



NOTES:

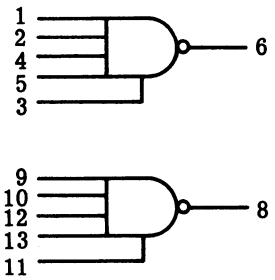
1. CONNECTOR P1 IS AMP INC. 480142-3 WITH 42702-3 CONTACTS (RAYTHEON COMPUTER SPEC NOS. 531715-001 AND -002).
2. CONNECTOR P2 IS ELCO 00-8016-020-000-707 WITH 60-8017-0313 CONTACTS (RAYTHEON COMPUTER SPEC NOS. 530501-013 AND 530028-001).

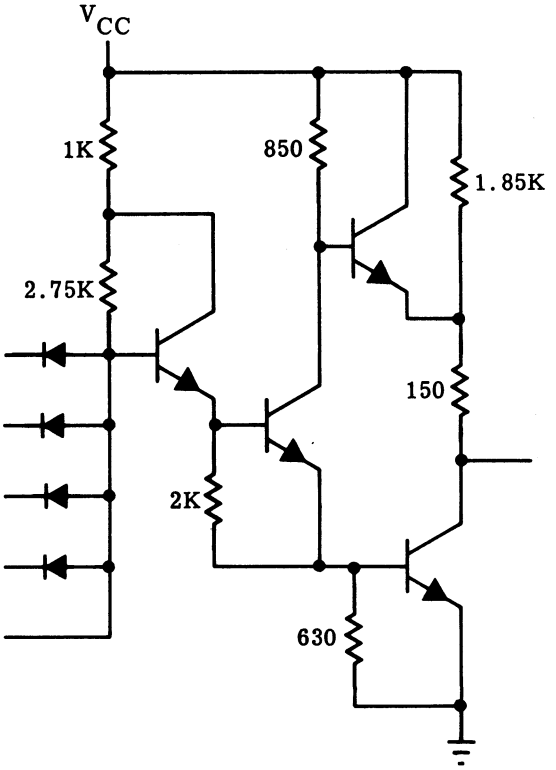
Drawing 545218. TTY Connector Cable


NOTES: UNLESS OTHERWISE SPECIFIED.
1. ⊕ INDICATES WIRE NO.2
2. FOR POWER FAILSAFE OPTION JUMPER TB5-8 TO TB5-9
(POWER SUPPLY)
(REAR PANEL)
MOTHER BOARD
POWER SUPPLY
704 CABINET (WIRING DIAGRAM)
545435
RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173
RELEASED PER E.O. 20606

TYPE D32
DUAL 4-INPUT BUFFER

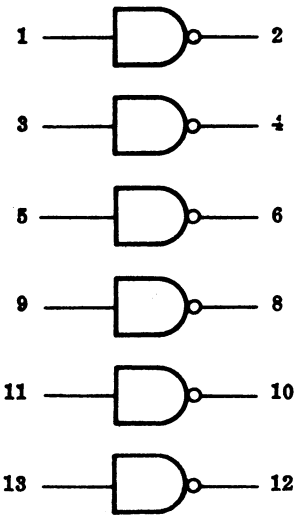
MOTOROLA MC832P
(RAYTHEON COMPUTER
SPEC. NO. 531143-001)

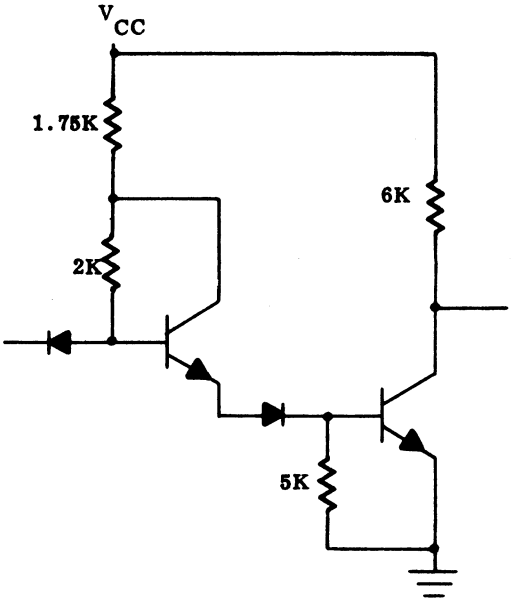




TYPE 36
HEX INVERTER

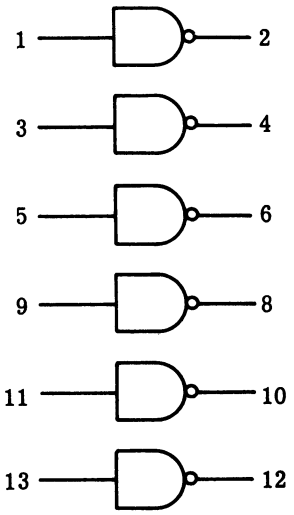
MOTOROLA MC836P
(RAYTHEON COMPUTER
SPEC. NO. 531274)

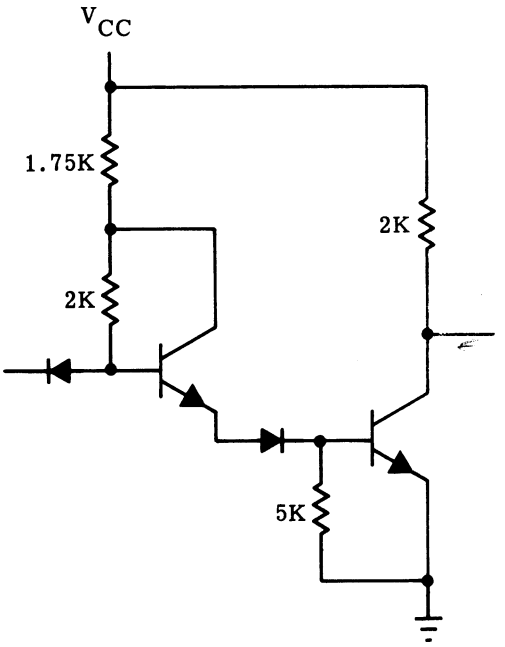




TYPE D37
HEX INVERTER

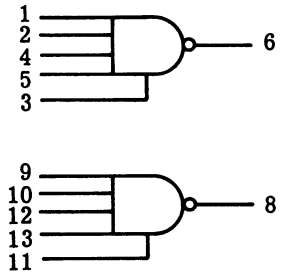
MOTOROLA MC837P
(RAYTHEON COMPUTER
SPEC. NO. 531531-001)

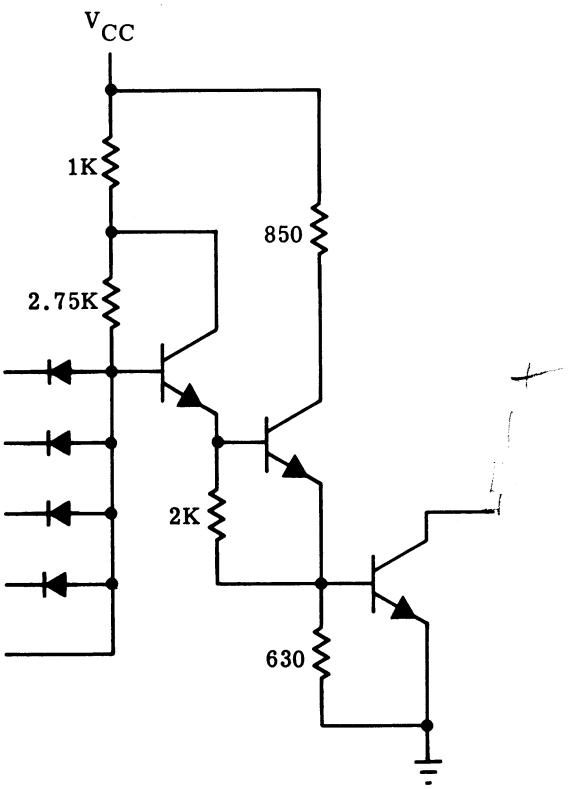




TYPE D44
DUAL 4-INPUT POWER GATE

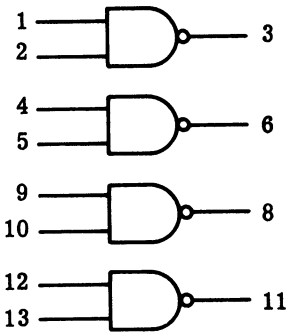
MOTOROLA MC844P
(RAYTHEON COMPUTER
SPEC. NO. 531145-001)

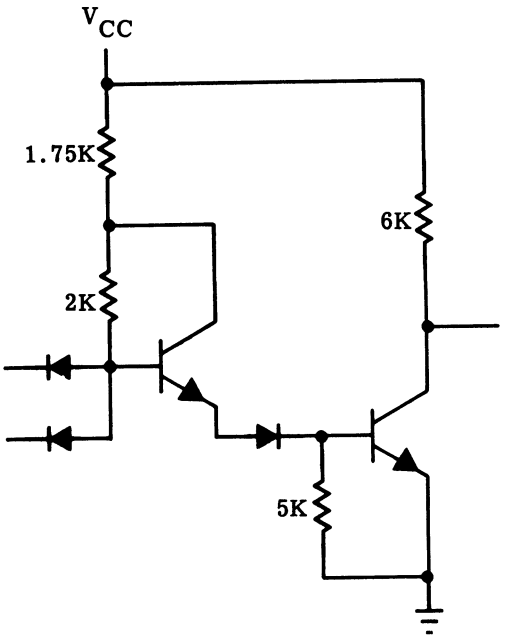




TYPE D46
QUAD 2-INPUT GATE

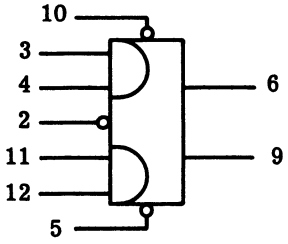
MOTOROLA MC846P
(RAYTHEON COMPUTER
SPEC. NO. 531147-001)





TYPE D48
CLOCKED RS FLIP-FLOP

MOTOROLA MC848P
(RAYTHEON COMPUTER
SPEC. NO. 531231-001)

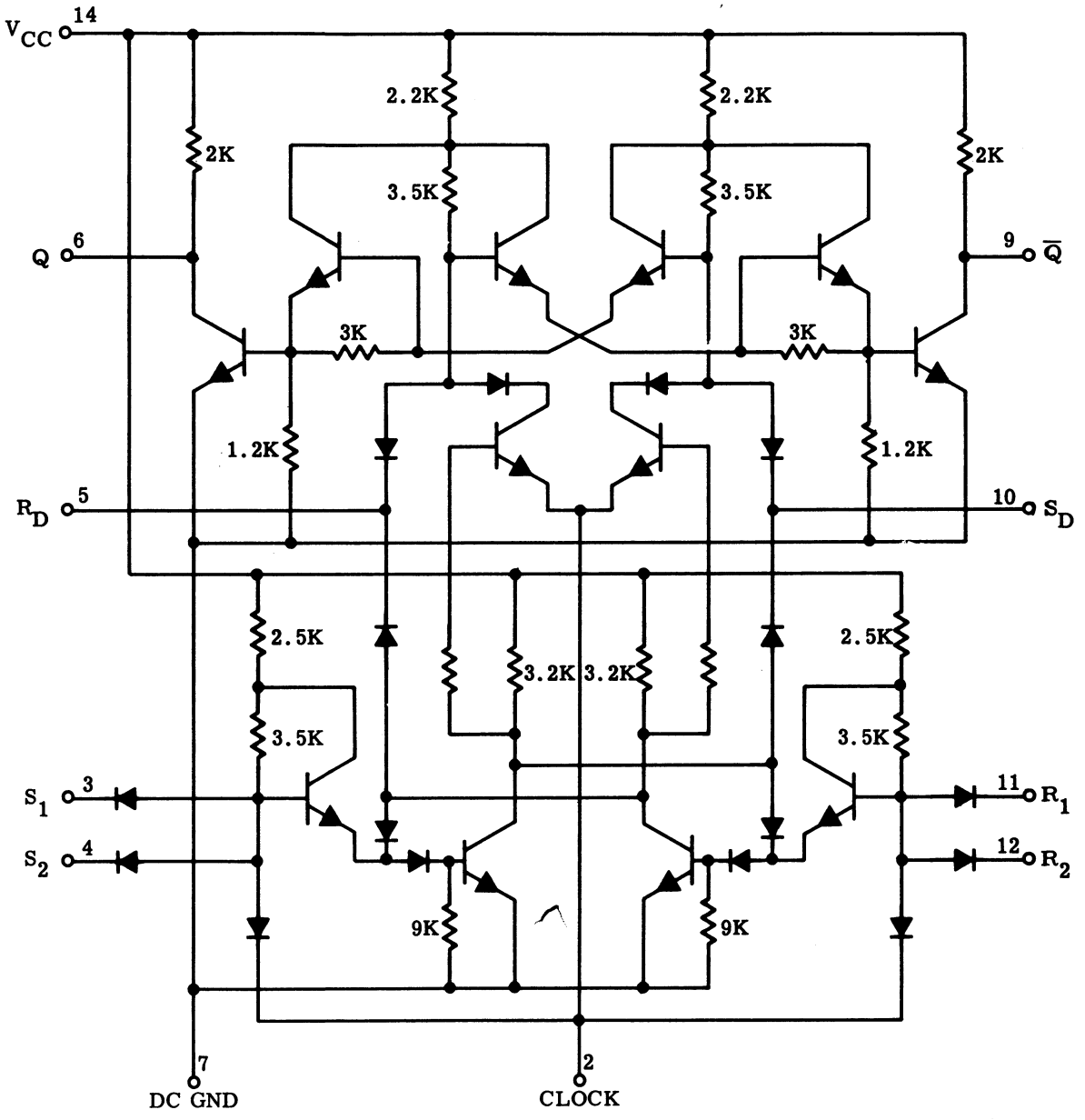


SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

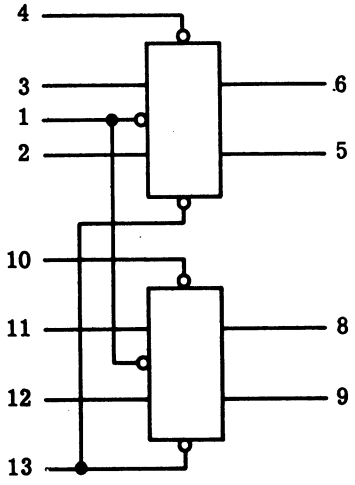
ASYNCHRONOUS TRUTH TABLE

S_D	R_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1



TYPE D55
DUAL J-K FLIP-FLOP

MOTOROLA MC855P
(RAYTHEON COMPUTER
SPEC. NO. 531535-001)

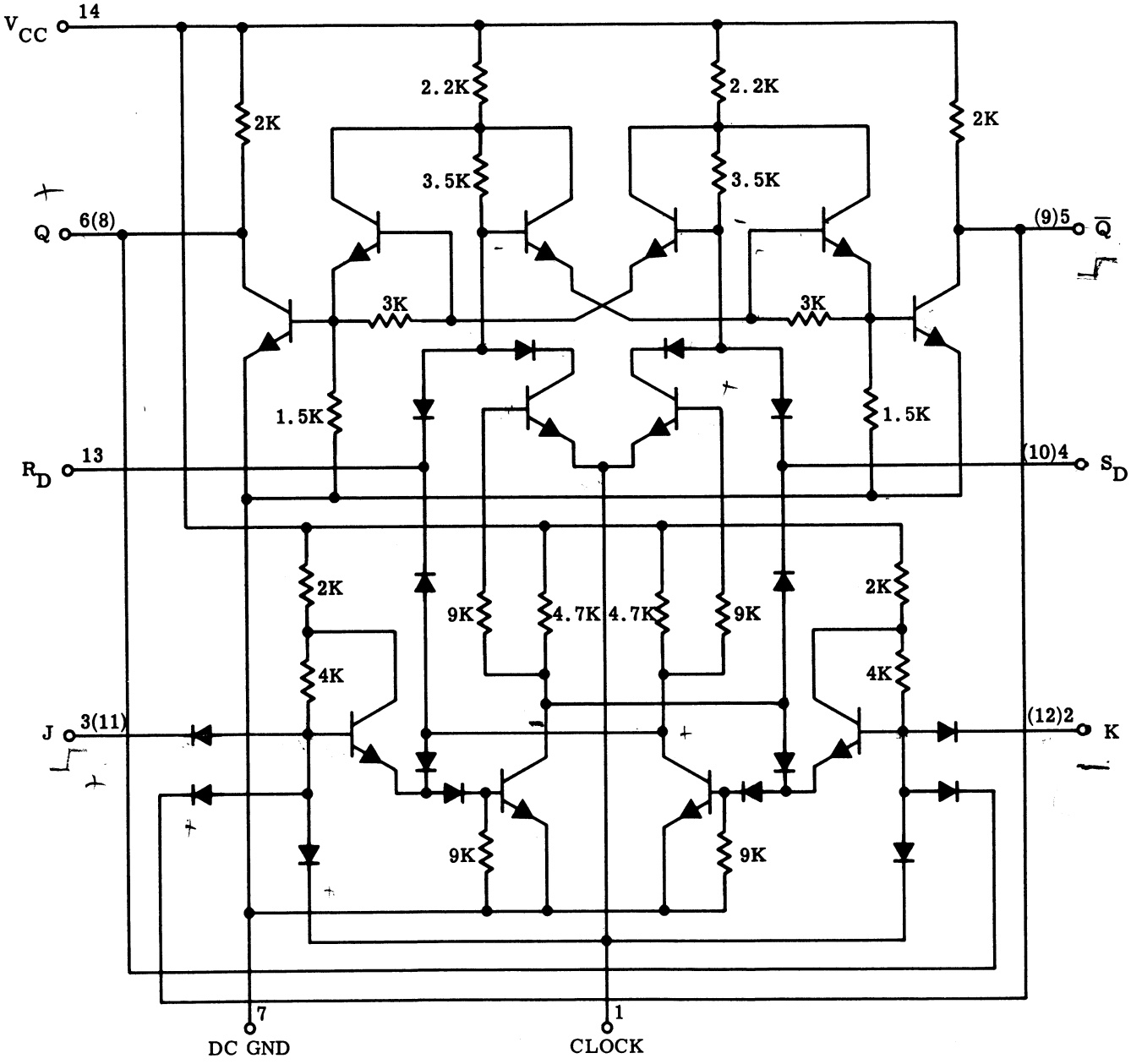


J-K TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

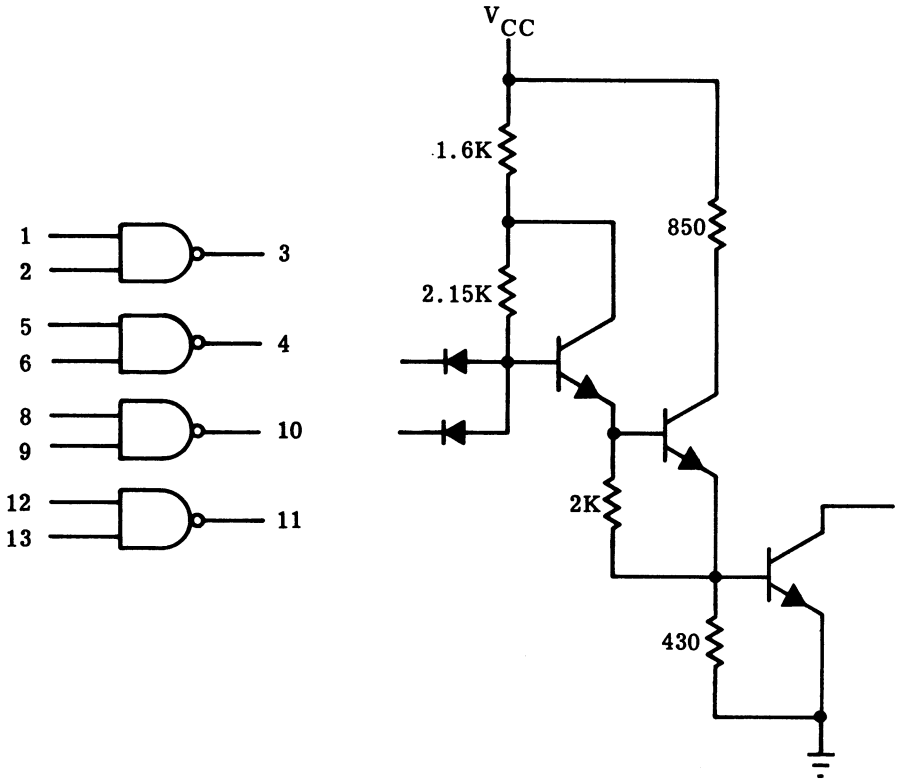
ASYNCHRONOUS TRUTH TABLE

S_D	R_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1



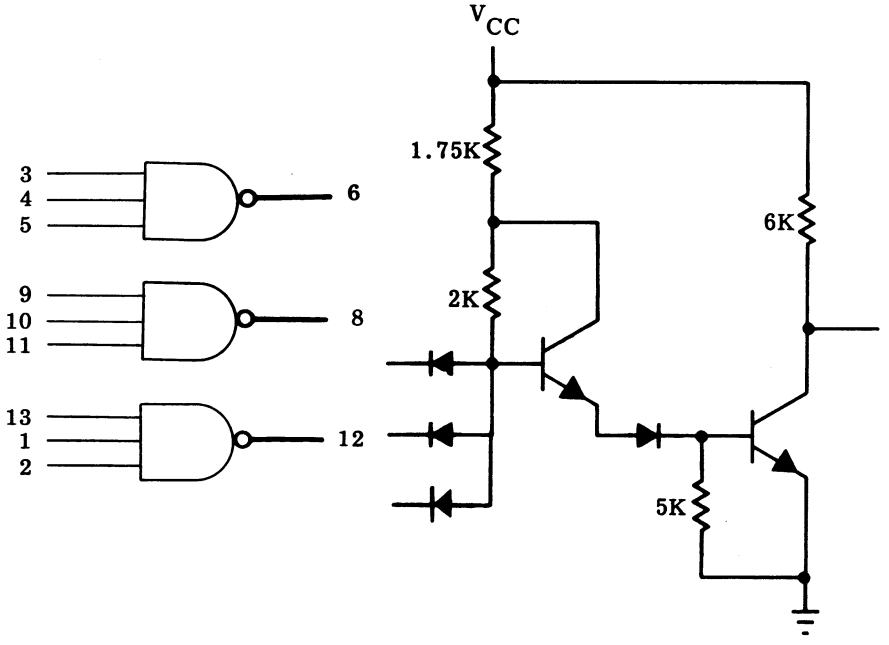
TYPE D58
QUAD 2-INPUT POWER GATE

MOTOROLA MC858P
(RAYTHEON COMPUTER
SPEC. NO. 531522-001)



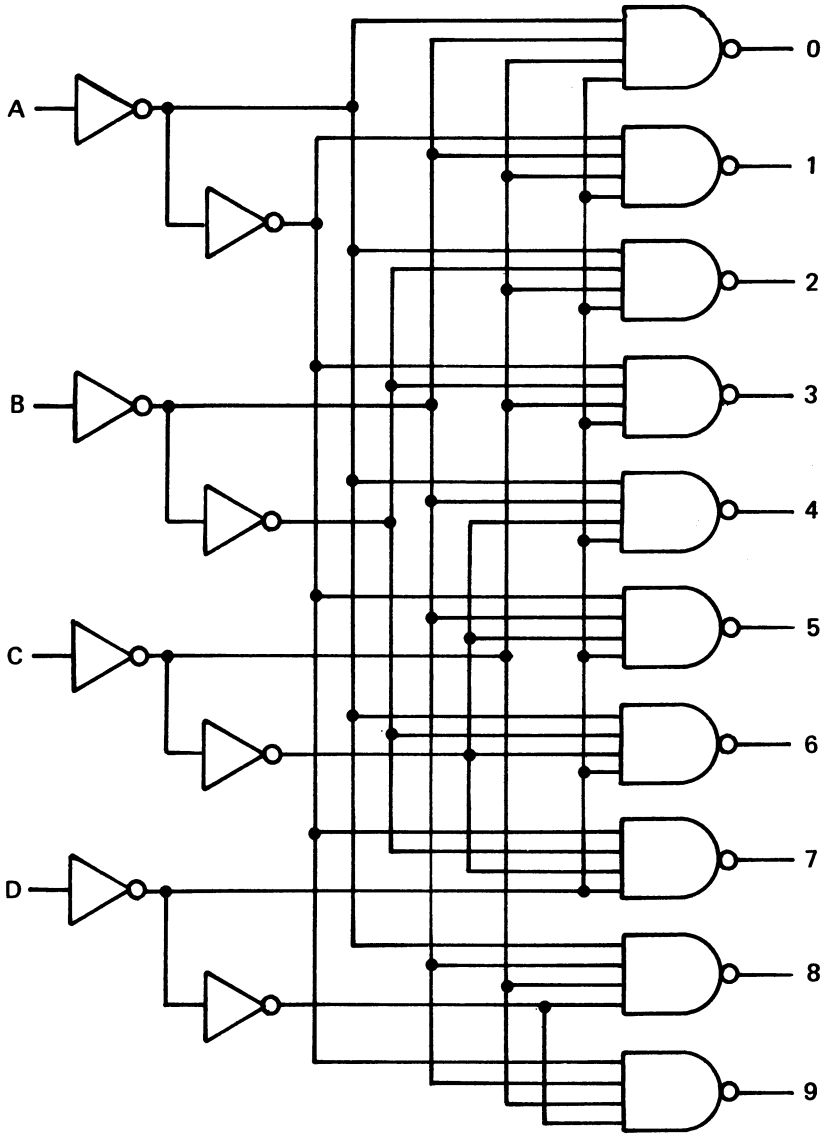
TYPE D62
TRIPLE 3-INPUT GATE

MOTOROLA MC862P
(RAYTHEON COMPUTER
SPEC. NO. 531148-001)



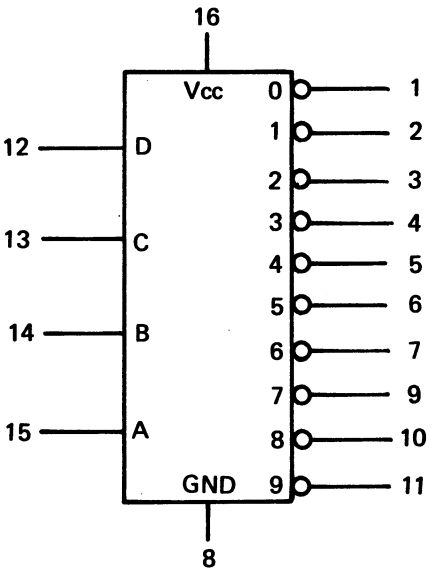
TYPE DEC
BCD-TO-DECIMAL DECODER

T.I. SN7445N
(RAYTHEON COMPUTER
SPEC NO. 531703-001)



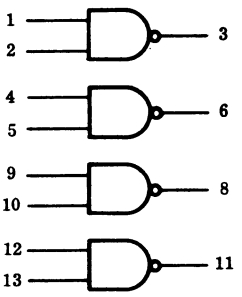
TRUTH TABLE

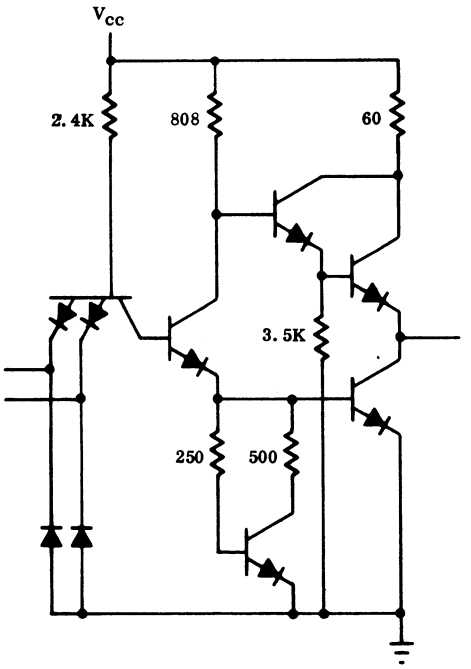
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1



TYPE M00
QUAD 2-INPUT NAND GATE

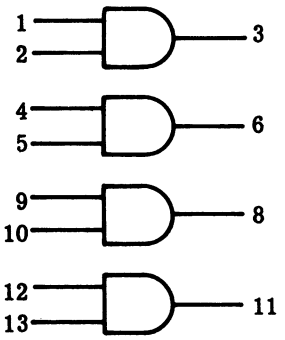
MOTOROLA MC3000R
(RAYTHEON COMPUTER
SPEC. NO. 531593-006)

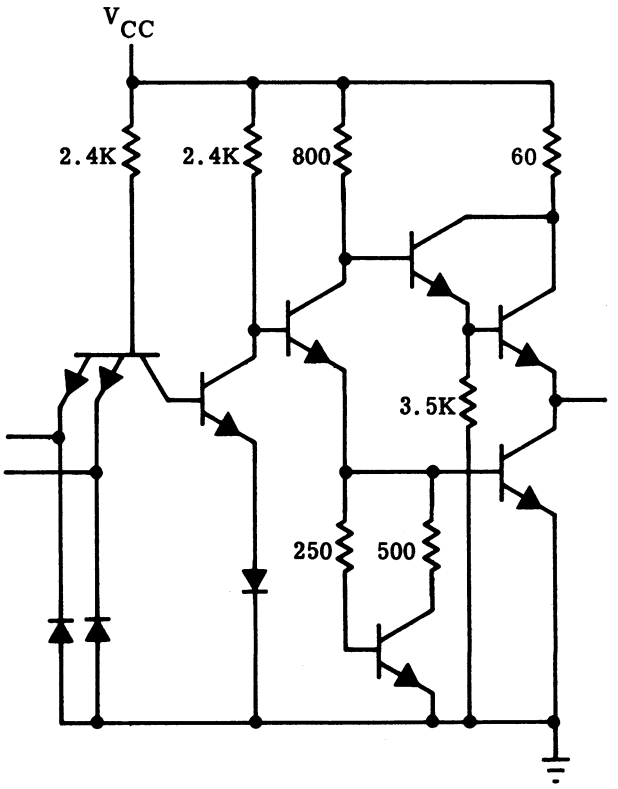




TYPE M01
QUAD 2-INPUT AND GATE

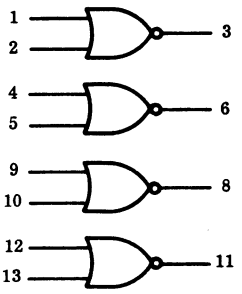
MOTOROLA MC3001R
(RAYTHEON COMPUTER
SPEC. NO. 531593-005)

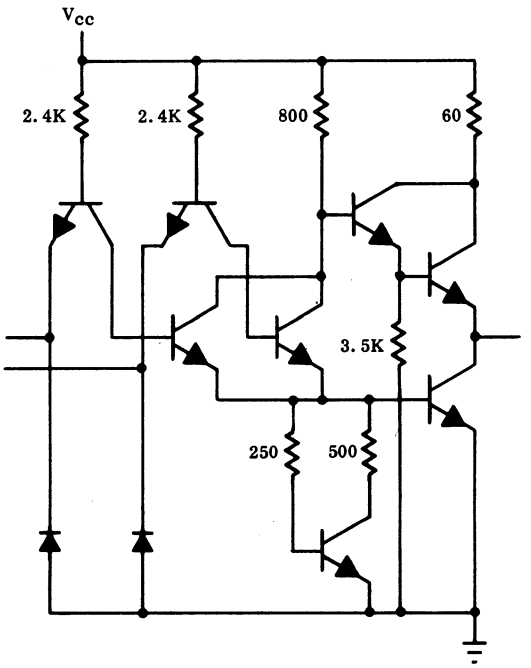




TYPE M02
QUAD 2-INPUT NOR GATE

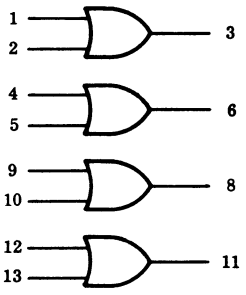
MOTOROLA MC3002R
(RAYTHEON COMPUTER
SPEC. NO. 531593-007)

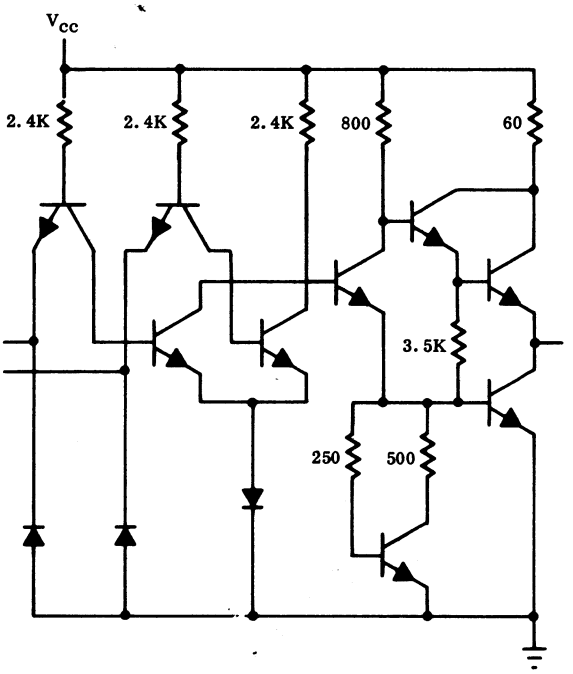




TYPE M03
QUAD 2-INPUT OR GATE

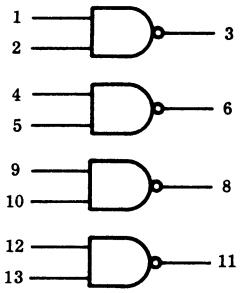
MOTOROLA MC3003R
(RAYTHEON COMPUTER
SPEC. NO. 531593-008)

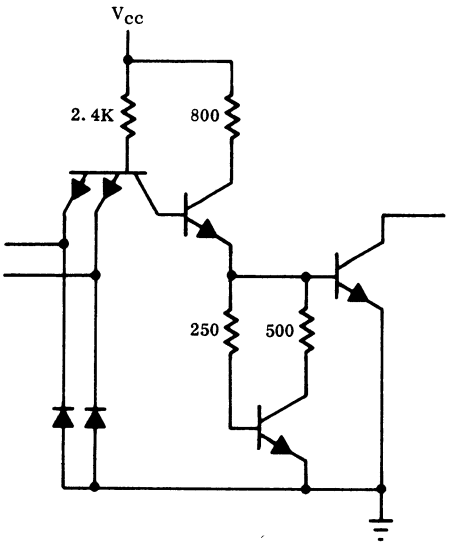




TYPE M04
QUAD 2-INPUT NAND GATE

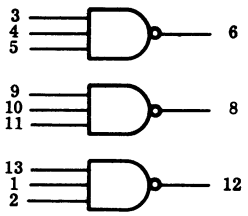
MOTOROLA MC3004R
(RAYTHEON COMPUTER
SPEC. NO. 531593-014)

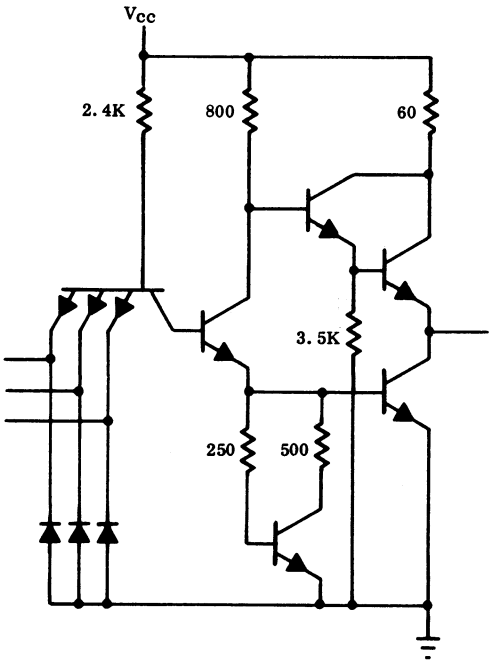




TYPE M05
TRIPLE 3-INPUT NAND GATE

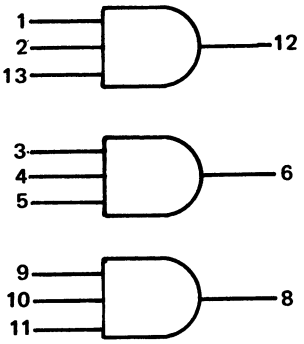
MOTOROLA MC3005R
(RAYTHEON COMPUTER
SPEC. NO. 531593-004)

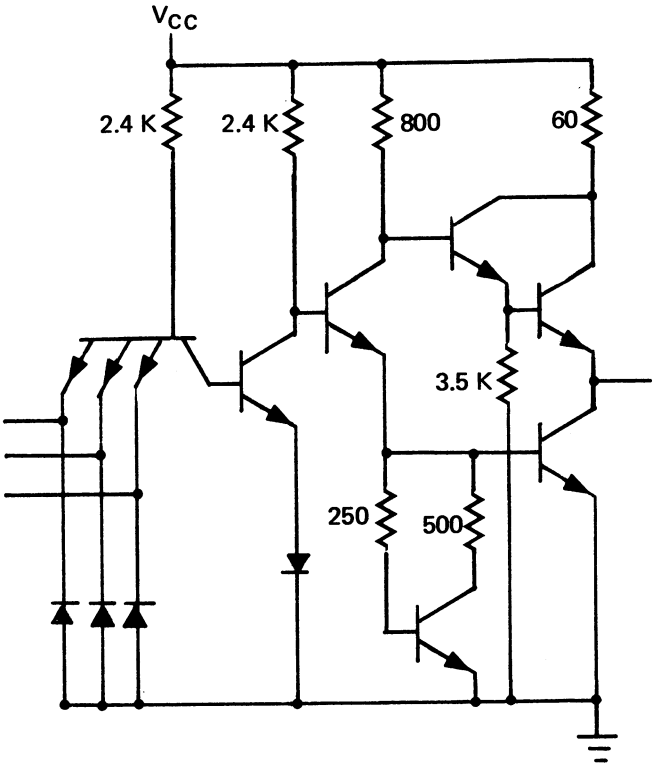




TYPE M06
TRIPLE 3-INPUT AND GATE

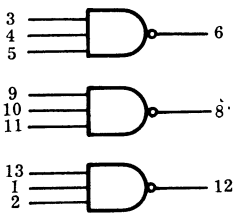
MOTOROLA MC3006R
(RAYTHEON COMPUTER
SPEC NO. 531594-001)

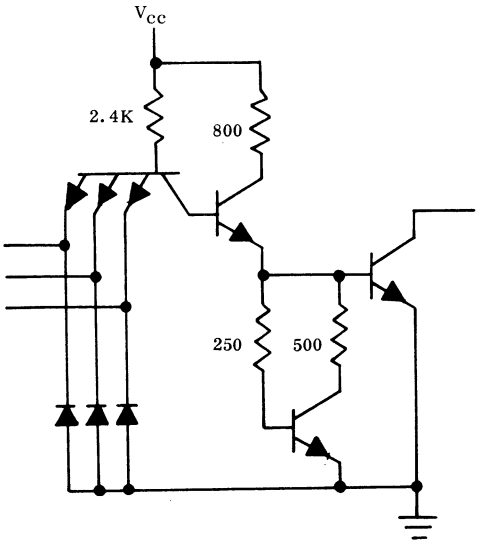




TYPE M07
TRIPLE 3-INPUT NAND GATE

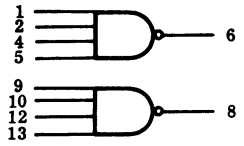
MOTOROLA MC3007R
(RAYTHEON COMPUTER
SPEC. NO. 531593-015)

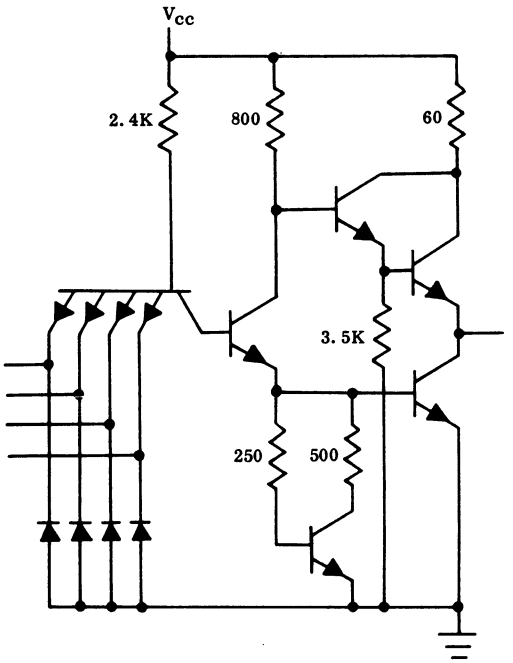




TYPE M10
DUAL 4-INPUT NAND GATE

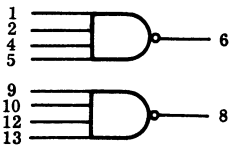
MOTOROLA MC3010R
(RAYTHEON COMPUTER
SPEC. NO. 531593-002)

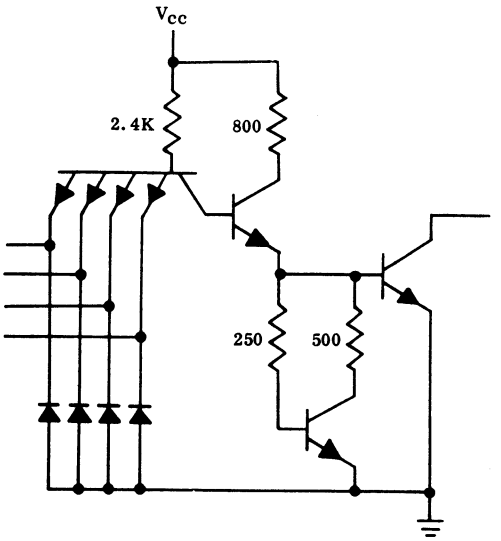




TYPE M12
DUAL 4-INPUT NAND GATE

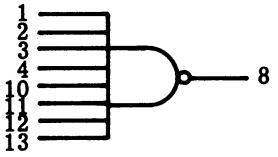
MOTOROLA MC3012R
(RAYTHEON COMPUTER
SPEC. NO. 531593-016)

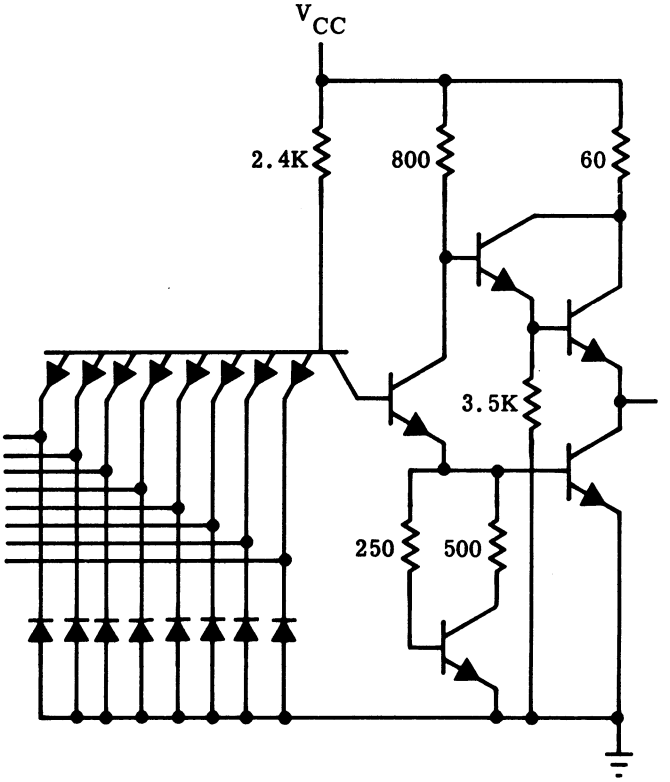




TYPE M15
SINGLE 8-INPUT
NAND GATE

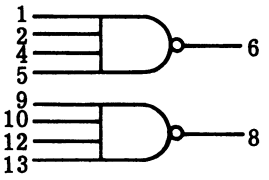
MOTOROLA MC3015R
(RAYTHEON COMPUTER
SPEC. NO. 531593-001)

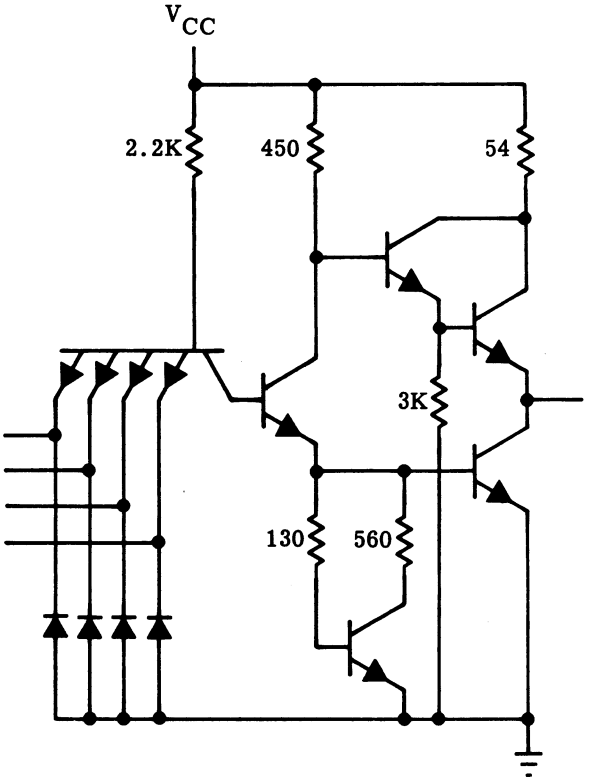




TYPE M25
DUAL 4-INPUT NAND
POWER GATE

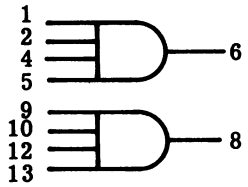
MOTOROLA MC3025R
(RAYTHEON COMPUTER
SPEC. NO. 531593-009)

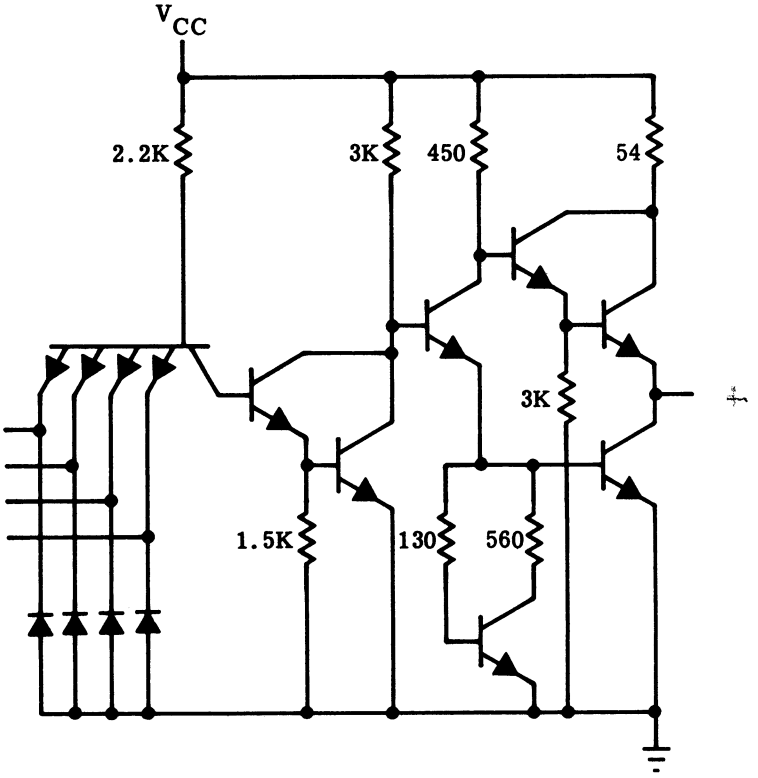




TYPE M26
DUAL 4-INPUT AND
POWER GATE

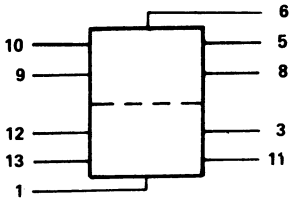
MOTOROLA MC3026R
(RAYTHEON COMPUTER
SPEC. NO. 531593-012)

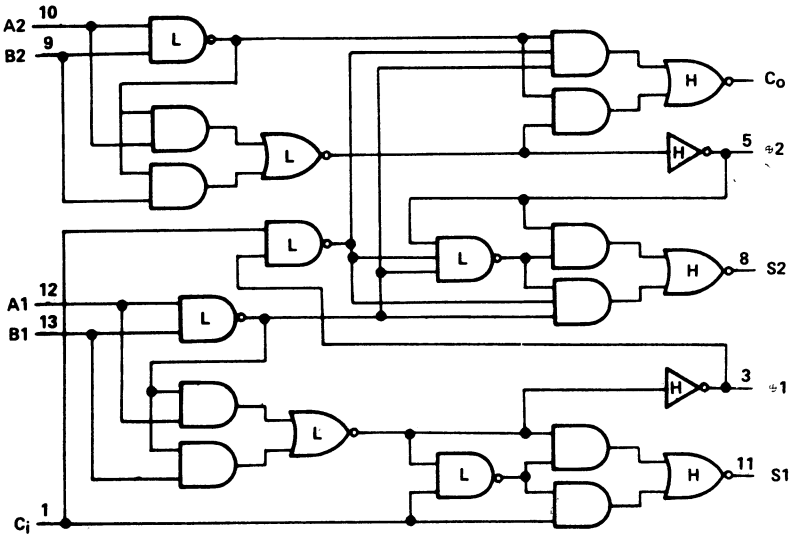




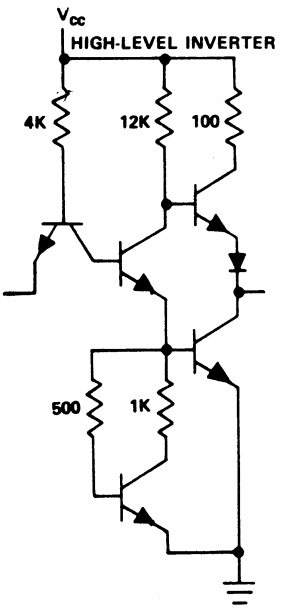
TYPE M27
2-BIT FULL ADDER

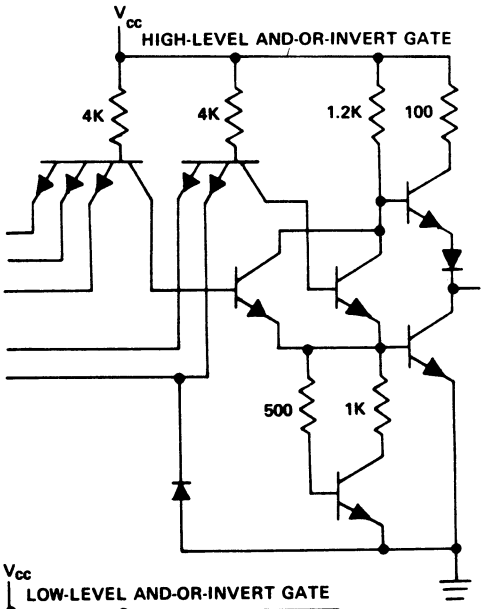
MOTOROLA MC4082R
(RAYTHEON COMPUTER
SPEC. NO. 531595-001)

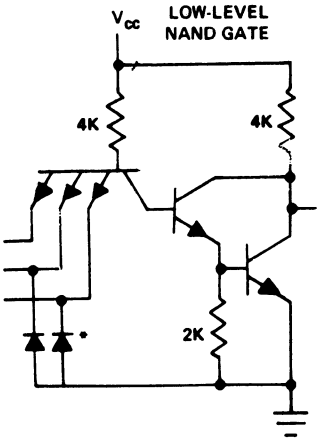


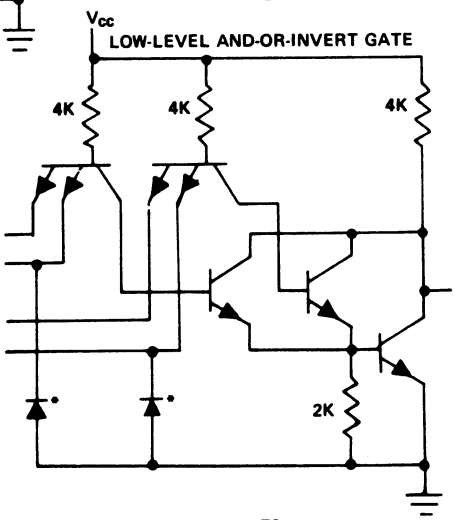


TRUTH TABLE											
INPUT				OUTPUT							
				Ci = 0			Ci = 1				
A1	B1	A2	B2	S1	S2	Co	S1	S2	Co	Σ1	Σ2
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	1	0	1	0
1	1	0	0	0	1	0	1	1	0	0	0
0	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	0	0	1	1	1
1	1	1	0	0	0	1	1	0	1	0	1
0	0	0	1	0	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	0	1	1	1
0	1	0	1	1	1	0	0	0	1	1	1
1	1	0	1	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	1	1	1	0
0	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	0	1	1	1	1	1	0	0





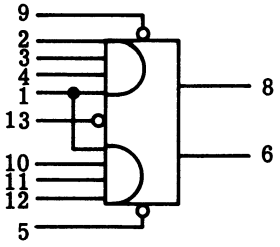




*DIODES USED ONLY ON EXTERNAL INPUTS

TYPE M51
AND J-K FLIP-FLOP

MOTOROLA MC3051R
(RAYTHEON COMPUTER
SPEC. NO. 531593-013)



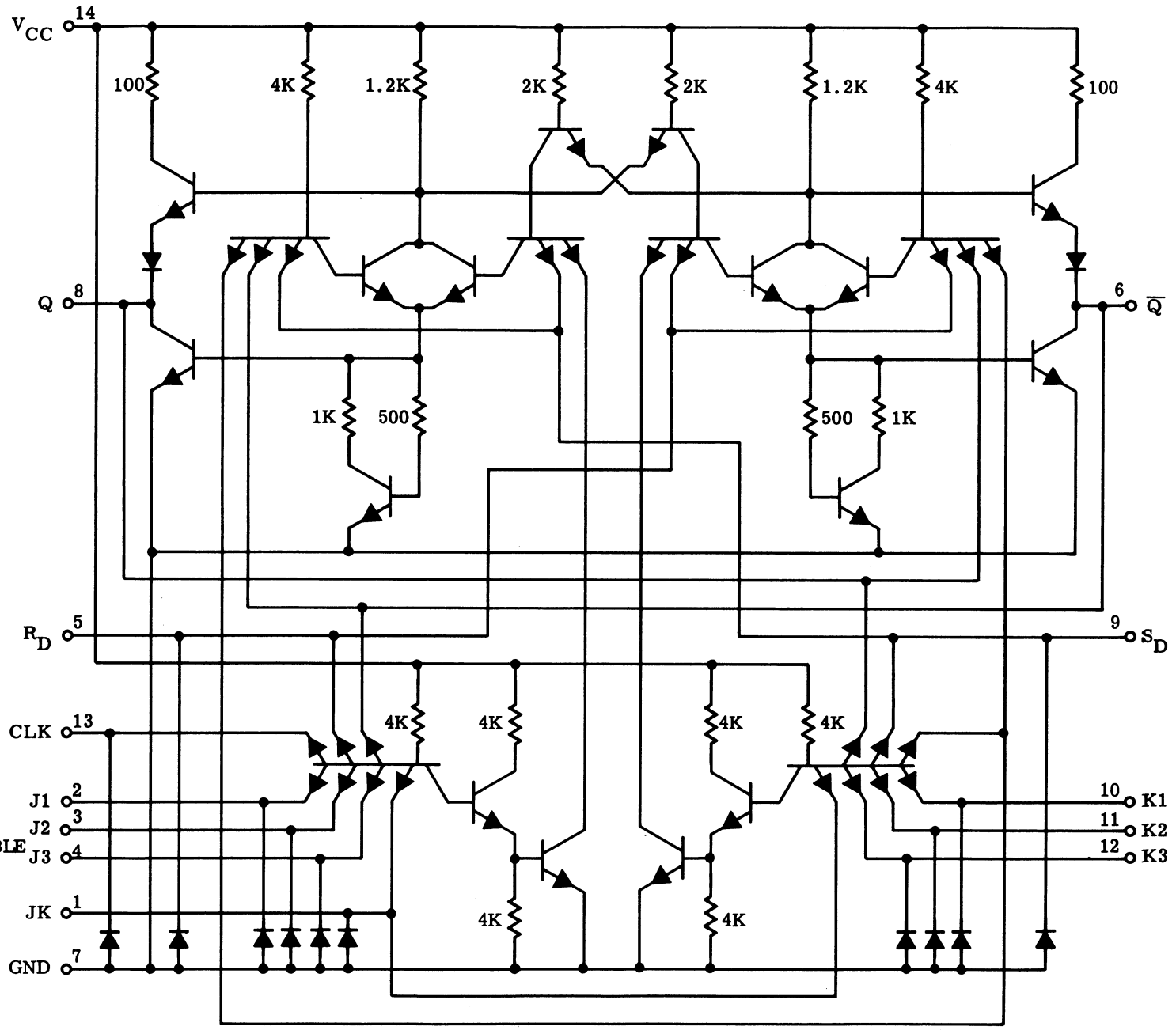
*J-K TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

*J=J1·J2·J3·JK
K=K1·K2·K3·JK

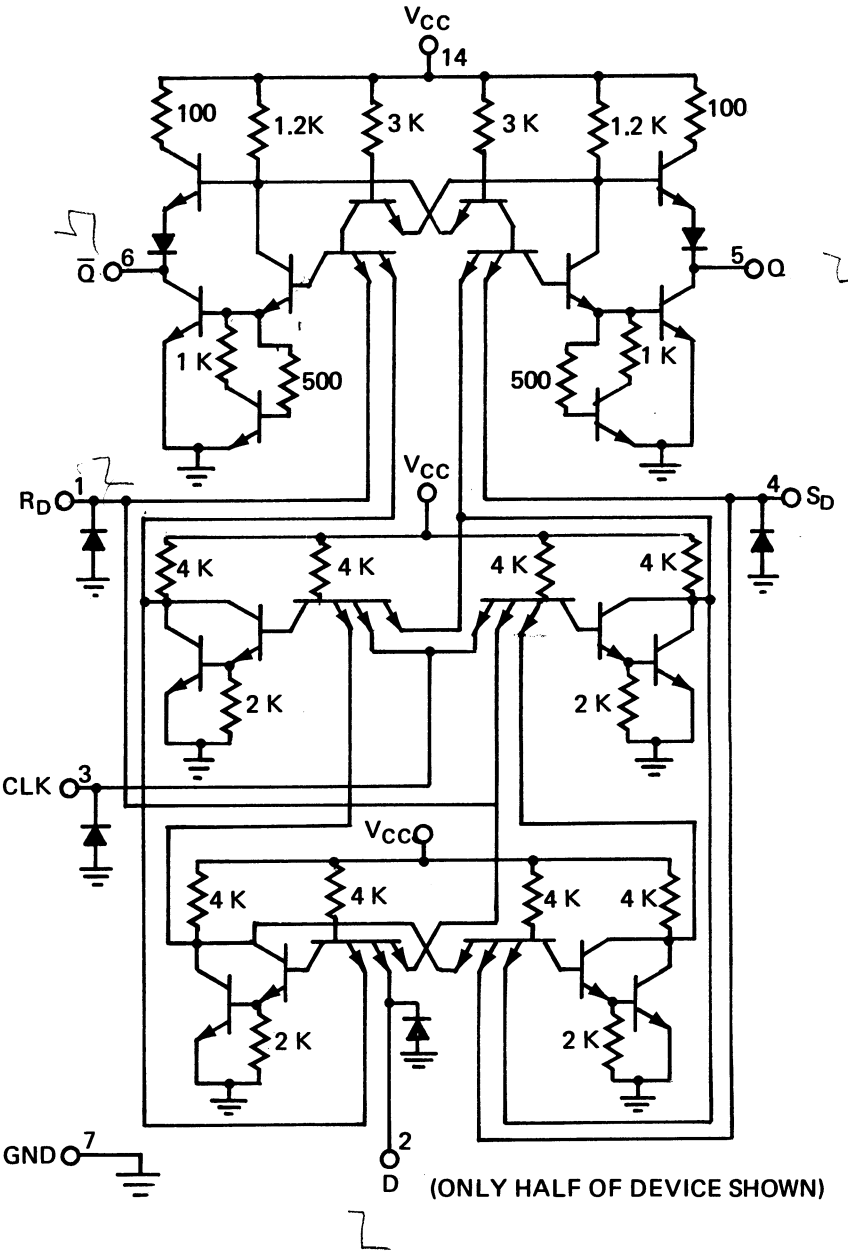
ASYNCHRONOUS TRUTH TABLE

S_D	R_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1



TYPE M60
TYPE M60A
DUAL TYPE D FLIP-FLOP

MOTOROLA MC3060R
(RAYTHEON COMPUTER
SPEC NO. 531593-018)



(ONLY HALF OF DEVICE SHOWN)

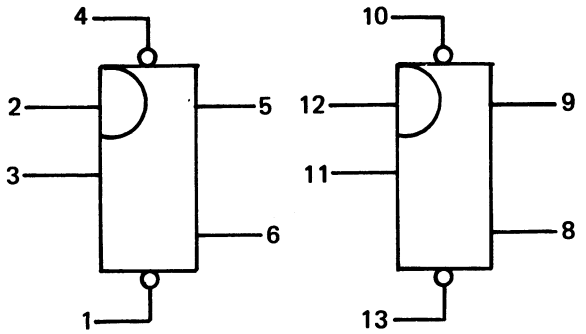
D-INPUT TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1
$Q^{n+1} = D^n$		

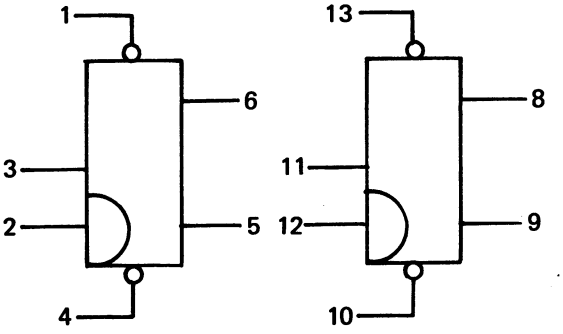
ASYNC TRUTH TABLE

S_D	R_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	?	?

USED AS D-TYPES (M60)

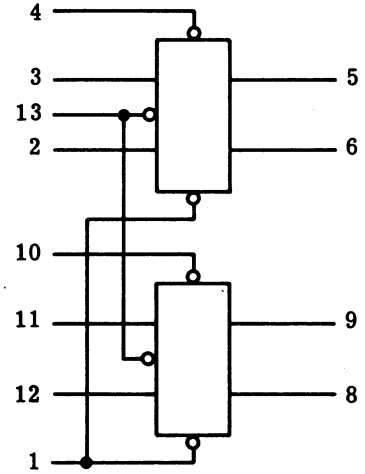


USED AS $\overline{D}$-TYPES (M60A)



TYPE M61
DUAL J-K FLIP-FLOP

MOTOROLA ! '3061R
(RAYTHEON COMPUTER
SPEC. NO. 531593-011)

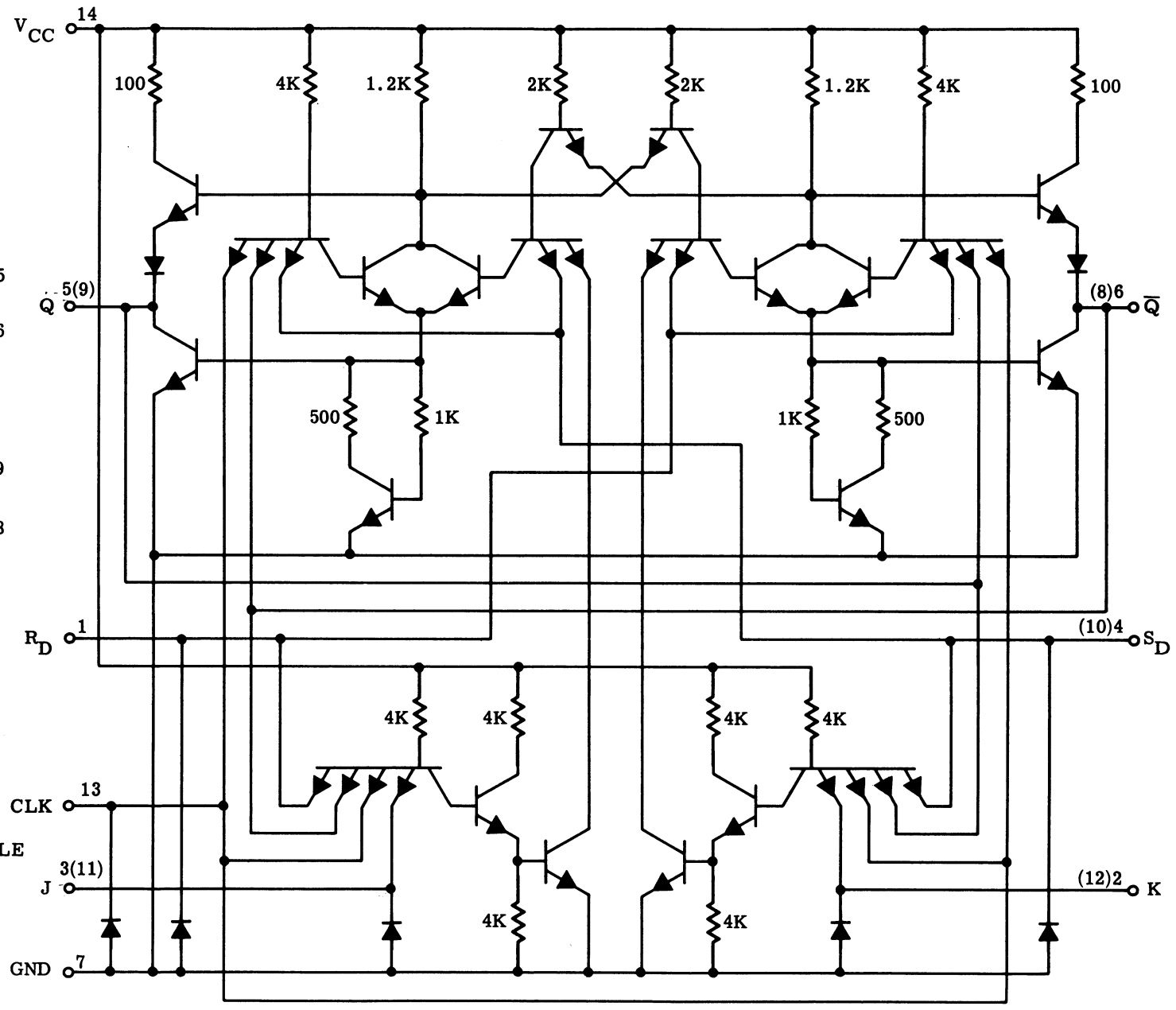


J-K TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

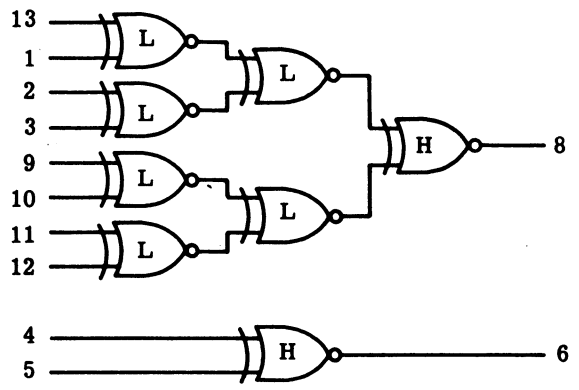
ASYNCHRONOUS TRUTH TABLE

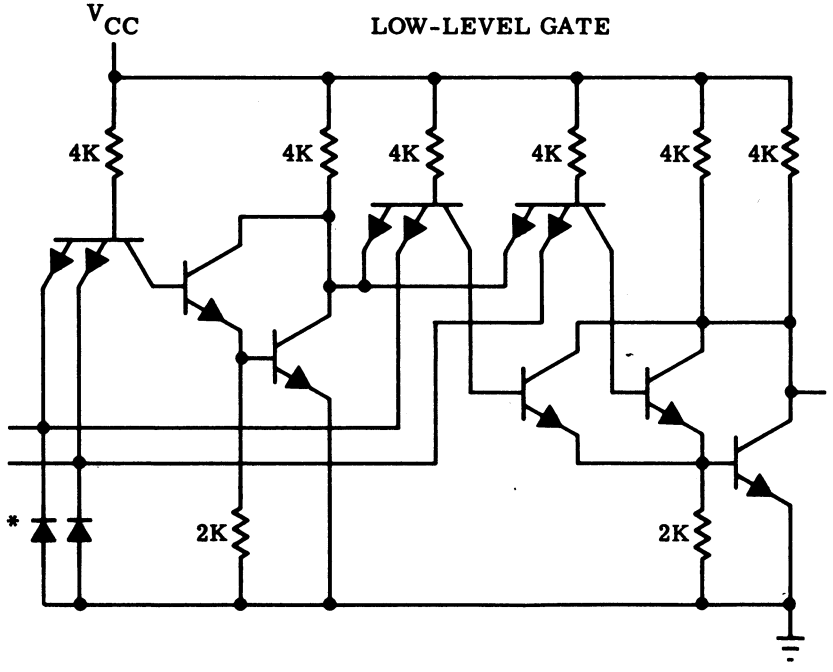
S_D	R_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

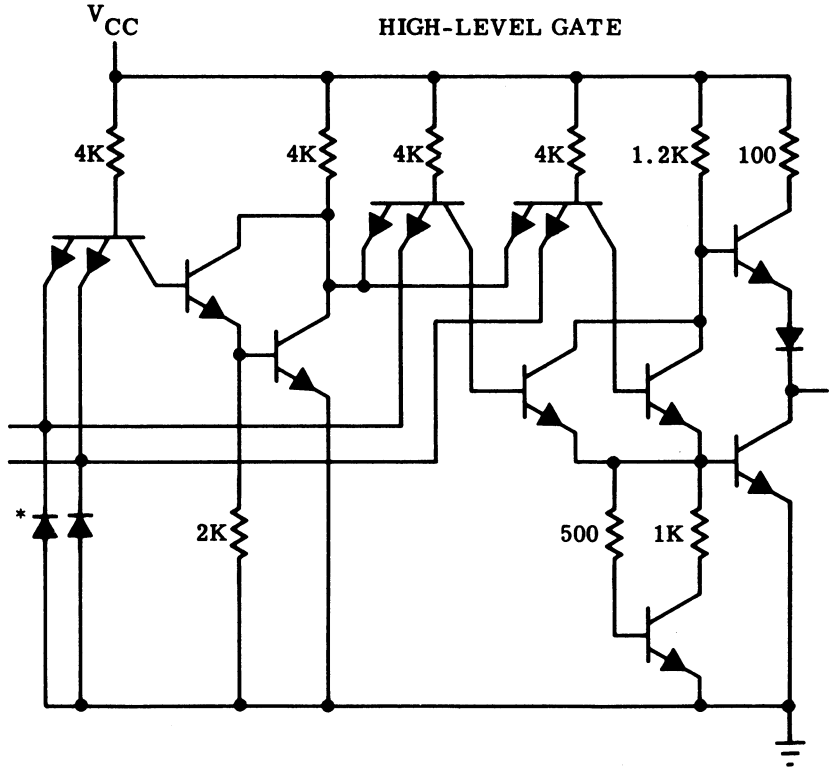


TYPE M74
8-BIT PARITY TREE

MOTOROLA MC4008R
(RAYTHEON COMPUTER
SPEC. NO. 531594-001)





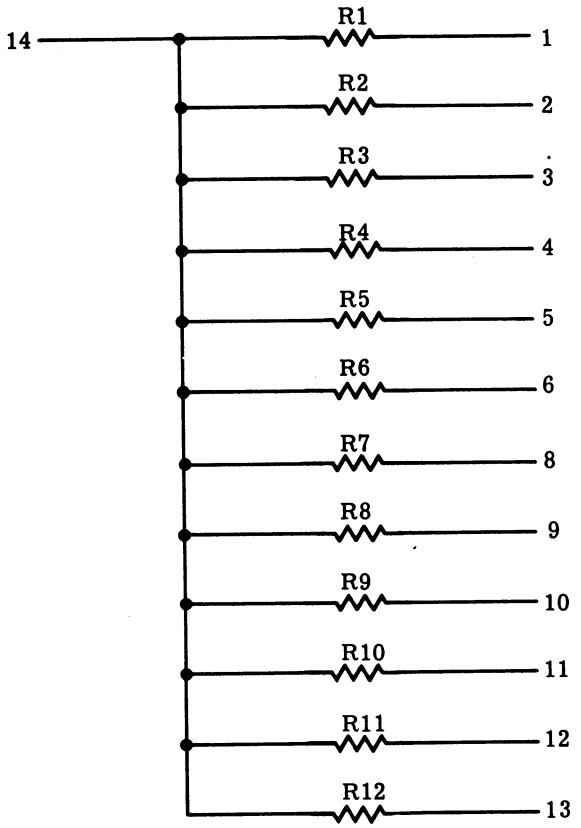


*DIODES USE ONLY ON INPUT GATES.

TYPE TX2
SWITCH TERMINATOR RESISTOR MODULE

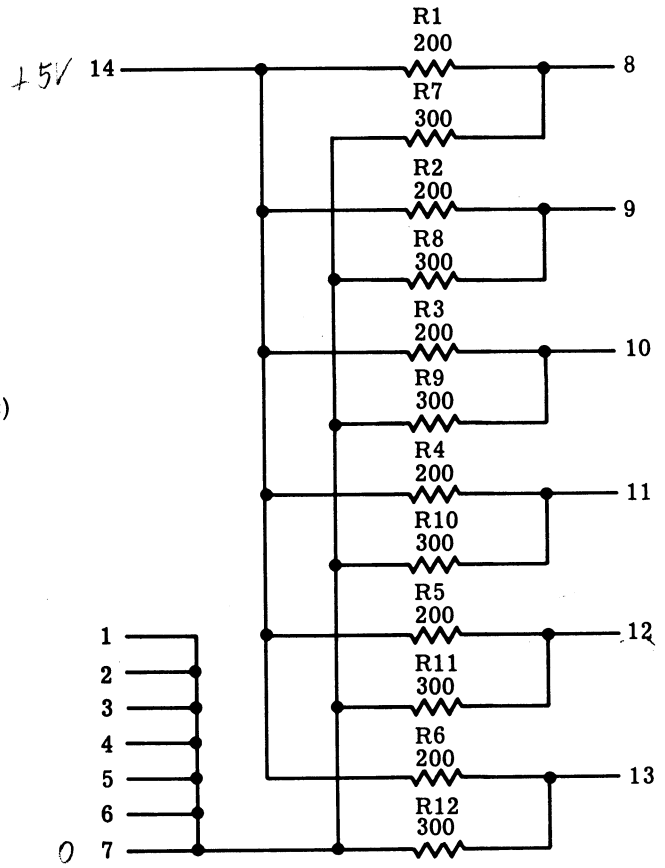
CTS OF BERNE SERIES 760-EL385010
(RAYTHEON COMPUTER SPEC. NO. 531596-001)

ALL RESISTORS ARE 1000-OHM



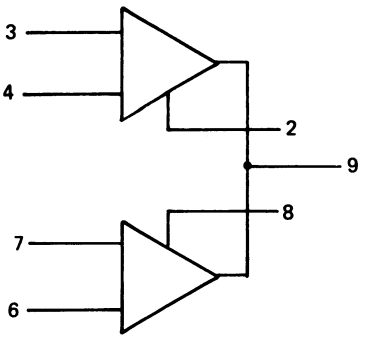
TYPE TX3
LONG LINE TERMINATOR RESISTOR MODULE

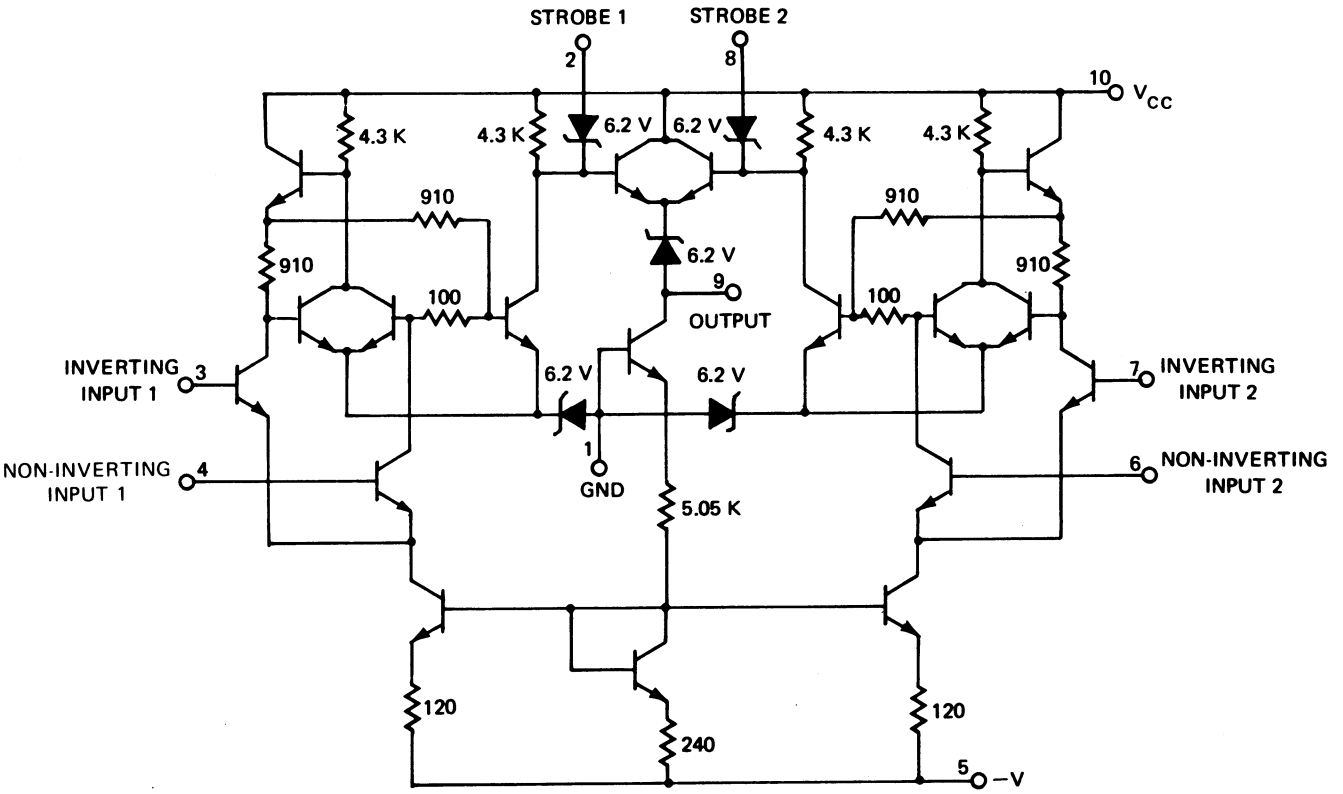
CTS OF BERNE SERIES 760-EL385014
(RAYTHEON COMPUTER SPEC. NO. 531596-002)



DUAL DIFFERENTIAL VOLTAGE COMPARATORS
(MEMORY SENSE AMPLIFIERS)

TEXAS INSTRUMENTS TYPE SN72 711L
(RAYTHEON COMPUTER
SPEC NO. 531702-001)





SIGNAL LIST

DRAWING 545222

RESERVE EO'S OUTSTANDING	REVISIONS							
	SYM	DESCRIPTION	MAKE	USE	DRAWN	CHECK	APPR	DATE
	X1	RELEASED PER EO # 18781				NB	RB	1/28/70
	A	RELEASED PER EO # 20160			KB	NB	NB	2/18/70
	B	REVISED PER EO # 20301			EVM			
	C	REVISED PER EO # 19164			EVM			
	D	REVISED PER EO # 21409			EVM			

DRAWN	LEECH	1-26-70
CHECK	N. BROTHERS	1-28-70
APPR	BARTZ	1-28-70
APPR		

NEXT ASSY 394782

RAYTHEON

RAYTHEON COMPANY
LEXINGTON, MASSACHUSETTS 02173

MOTHER BOARD ASSEMBLY
C SERIES - 704
(SIGNAL LIST)

CODE IDENT NO.	SIZE	
49956	B	545222

SCALE NONE

SHEET 1 OF 61

RAYTHEON COMPUTER FORM 67-0080

FILLER

GENERAL NOTES, UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS:

545224	WIRING INSTRUCTION PAPER TAPE
545223	LOCATION LIST

FILLET

0,5	ARI	ARI0	200	0	1015	05A43	1	001	=5V
0,5	ARI	ARI4	205	1	1015	06A43	2	002	
0,5	ARI	ARI8	200	2	1015	07A43	1	003	
1,5	ARI	ARI1	200	1	1015	08A43	2	004	
4,3	MAG	MAG0	040	2	1015	10A64	S 1	005	
2,0	DAM	DAM	040	1	1015	14A31	2	006	
9,3	PFS	PFS	290	2	1015	17A62	0	007	9,3/ 0,0
2,5	ARI	ARI0	550	0	1015	05B47	1	001	AC00SRCD
2,5	INR	INR	355	1	1015	03B06	S 0	002	2,5/ 0,0
5,8	ARI	ARI4	670	0	1015	06B68	1	001	AC07SL
5,8	INR	INR	300	1	1015	03A63	S 0	002	5,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
7,5		ARI	ARI8	555		0	1015 07B47		1	001	AC08BR
7,5		INR	INR	020		1	1015 03A07	S	0	002	7,5/ 0,0
1,3		M=D	M=D	335		0	1015 04A06	S	1	001	ACCLKENB4=
1,3		INR	INR	145		1	1015 03A32	S	0	002	1,3/ 0,0
0,5		ARI	ARI4	085		0	1015 06A19		1	001	ACCLKENBL
2,0		ARI	ARI0	080		1	1015 05A19		2	002	
2,5		INR	INR	275		2	1015 03A58	S	0	003	2,5/ 0,0
0,5		ARI	ARI1	080		0	1015 08A19		1	001	ACCLKENBR
5,8		ARI	ARI8	080		1	1015 07A19		2	002	
6,3		INR	INR	505		2	1015 03B36	S	0	003	6,3/ 0,0
0,0		DAM	DAM	025		0	1015 14A14	S	0	001	ACDLY
6,5		MEM	MEM	230		0	1015 09A49		1	001	ACDLY=
6,5		DAM	DAM	315		1	1015 14B51	S	0	002	6,5/ 0,0
0,0		INR	INR	180		0	1015 03A39		0	001	ACDSLOPT=
0,5		ARI	ARI0	580		0	1015 05B53		1	001	ACLDAD
0,5		ARI	ARI4	595		1	1015 06B53		2	002	
0,5		ARI	ARI8	585		2	1015 07B53		1	003	
6,5		ARI	ARI1	580		1	1015 08B53		2	004	
8,0		INR	INR	140		2	1015 03A31	S	0	005	8,0/ 0,0
0,8		M=D	M=D	475		0	1015 04A45	S	1	001	ACLDAD3=
0,8		INR	INR	260		1	1015 03A55	S	0	002	0,8/ 0,0
4,3		INR	INR	335		0	1015 03A70		1	001	ACLDAD3A=
4,3		MEM	MEM	015		1	1015 09A06	S	0	002	4,3/ 0,0
5,8		ADF	ADF	280		0	1015 01A59		1	001	ACLDDI
1,0		INR	INR	650		1	1015 03B65	S	2	002	
0,5		ARI	ARI0	620		2	1015 05B61		1	003	
0,5		ARI	ARI4	635		1	1015 06B61		2	004	
0,5		ARI	ARI8	625		2	1015 07B61		1	005	
8,3		ARI	ARI1	620		1	1015 08B61		0	006	8,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
1,0		INR	INR	545	0	1015 03B44	S	1		001	ACLDOR
0,5		ARI	ARIO	595	1	1015 05B56		2		002	
0,5		ARI	ARI4	610	2	1015 06B56		1		003	
0,5		ARI	ARI8	600	1	1015 07B56		2		004	
2,5		ARI	ARI1	595	2	1015 08B56		0		005	2,5/ 0,0
1,0		INR	INR	525	0	1015 03B40	S	1		001	ACLDXOR
0,5		ARI	ARIO	585	1	1015 05B54		2		002	
0,5		ARI	ARI4	600	2	1015 06B54		1		003	
0,5		ARI	ARI8	590	1	1015 07B54		2		004	
2,5		ARI	ARI1	585	2	1015 08B54		0		005	2,5/ 0,0
0,0		PFS	PFS	270	0	1015 17A05		0		001	ACPWRA
0,0		PFS	PFS	280	0	1015 17A06		0		001	ACPWRB
6,5		MEM	MEM	060	0	1015 09A15		1		001	ACR00
2,0		ARI	ARIO	525	1	1015 05B42	S	2		002	
8,5		ADF	ADF	665	2	1015 01B68		0		003	8,5/ 0,0
2,0		ADF	ADF	655	0	1015 01B66		1		001	ACR00=
6,5		ARI	ARIO	515	1	1015 05B40	S	2		002	
2,5		INR	INR	030	2	1015 03A09		1		003	
11,0		MEM	MEM	050	1	1015 09A13		0		004	11,0/ 0,0
5,8		INR	INR	115	0	1015 03A26	S	1		001	ACR00S
1,3		ARI	ARIO	535	1	1015 05B44	S	2		002	
7,1		M=D	M=D	350	2	1015 04B66	S	0		003	7,1/ 0,0
0,5		ARI	ARIO	565	0	1015 05B50	S	1		001	ACR01
1,3		M=D	M=D	150	1	1015 04B54		2		002	
1,8		ADF	ADF	595	2	1015 01B54		0		003	1,8/ 0,0
0,0		ARI	ARIO	555	0	1015 05B48	S	0		001	ACR01S
0,0		ARI	ARIO	610	0	1015 05B59	S	0		001	ACR02
0,0		ARI	ARIO	640	0	1015 05B65	S	0		001	ACR03

C LNTH	NOTE	CKT	EQUATION	EQL BO	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
1,3		ARI	ARI4	555	0	1015 06B45		1	001	ACR03=
1,3		ARI	ARI0	650	1	1015 05B67	S	0	002	1,3/ 0,0
0,0		ARI	ARI0	625	0	1015 05B62	S	0	001	ACR03S
0,0		ARI	ARI4	540	0	1015 06B42	S	0	001	ACR04
1,3		ARI	ARI0	645	0	1015 05B66		1	001	ACR04=
1,3		ARI	ARI4	530	1	1015 06B40	S	0	002	1,3/ 0,0
0,0		ARI	ARI4	550	0	1015 06B44	S	0	001	ACR04S
0,0		ARI	ARI4	580	0	1015 06B50	S	0	001	ACR05
0,0		ARI	ARI4	570	0	1015 06B48	S	0	001	ACR05S
0,0		ARI	ARI4	625	0	1015 06B59	S	0	001	ACR06
7,5		INR	INR	075	0	1015 03A18		1	001	ACR07
7,5		ARI	ARI4	655	1	1015 06B65	S	0	002	7,5/ 0,0
1,3		ARI	ARI8	545	0	1015 07B45		1	001	ACR07=
1,3		ARI	ARI4	665	1	1015 06B67	S	0	002	1,3/ 0,0
7,5		ARI	ARI4	640	0	1015 06B62	S	1	001	ACR07S
7,5		INR	INR	135	1	1015 03A30	S	0	002	7,5/ 0,0
3,5		ARI	ARI8	530	0	1015 07B42	S	1	001	ACR08
3,0		ARI	ARI0	325	1	1015 05A68		2	002	
6,5		INR	INR	040	2	1015 03A11		0	003	6,5/ 0,0
1,3		ARI	ARI4	660	0	1015 06B66		1	001	ACR08=
1,3		ARI	ARI8	520	1	1015 07B40	S	0	002	1,3/ 0,0
6,5		ARI	ARI8	540	0	1015 07B44	S	1	001	ACR08S
6,5		INR	INR	125	1	1015 03A28	S	0	002	6,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
2,0		ARI	ARI0	415	0	1015 05B20		1	001	ACR09
2,0		ARI	ARI8	570	1	1015 07B50	S	0	002	2,0/ 0,0
0,0		ARI	ARI8	560	0	1015 07B48	S	0	001	ACR09S
2,0		ARI	ARI0	430	0	1015 05B23		1	001	ACR10
2,0		ARI	ARI8	615	1	1015 07B59	S	0	002	2,0/ 0,0
2,0		ARI	ARI0	495	0	1015 05B36		1	001	ACR11
2,0		ARI	ARI8	645	1	1015 07B65	S	0	002	2,0/ 0,0
1,3		ARI	ARI1	540	0	1015 08B45		1	001	ACR11=
1,3		ARI	ARI8	655	1	1015 07B67	S	0	002	1,3/ 0,0
0,0		ARI	ARI8	630	0	1015 07B62	S	0	001	ACR11S
3,5		ARI	ARI4	330	0	1015 06A68		1	001	ACR12
3,5		ARI	ARI1	525	1	1015 08B42	S	0	002	3,5/ 0,0
1,3		ARI	ARI8	650	0	1015 07B66		1	001	ACR12=
1,3		ARI	ARI1	515	1	1015 08B40	S	0	002	1,3/ 0,0
0,0		ARI	ARI1	535	0	1015 08B44	S	0	001	ACR12S
2,0		ARI	ARI4	430	0	1015 06B20		1	001	ACR13
2,0		ARI	ARI1	565	1	1015 08B50	S	0	002	2,0/ 0,0
0,0		ARI	ARI1	555	0	1015 08B48	S	0	001	ACR13S
2,0		ARI	ARI4	445	0	1015 06B23		1	001	ACR14
2,0		ARI	ARI1	610	1	1015 08B59	S	0	002	2,0/ 0,0
2,5		INR	INR	060	0	1015 03A15		1	001	ACR15
3,5		M=D	M=D	100	1	1015 04A61		2	002	
2,0		ARI	ARI4	510	2	1015 06B36		1	003	
8,0		ARI	ARI1	640	1	1015 08B65	S	0	004	8,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
3,0		ARI	ARI1	650		0	1015 08B67	S	1		001	ACR15=
5,8		ADF	ADF	625		1	1015 01B60			2	002	
3,0		M=D	M=D	095		2	1015 04A51			1	003	
11,8		MEM	MEM	065		1	1015 09A16			0	004	11,8/ 0,0
2,0		ARI	ARI1	625		0	1015 08B62	S	1		001	ACR15S
7,5		M=D	M=D	365		1	1015 04B68	S	2		002	
9,5		INR	INR	130		2	1015 03A29	S	0		003	9,5/ 0,0
0,5		ARI	ARI0	575		0	1015 05B52			1	001	ACRDR=
0,5		ARI	ARI4	590		1	1015 06B52			2	002	
0,5		ARI	ARI8	580		2	1015 07B52			1	003	
6,5		ARI	ARI1	575		1	1015 08B52			2	004	
8,0		SCD	SCDC	135		2	1015 02A32	S	0		005	8,0/ 0,0
5,8		MEM	MEM	265		0	1015 09A56			1	001	ACRZER00
5,8		ARI	ARI0	600		1	1015 05B57	S	0		002	5,8/ 0,0
5,8		MEM	MEM	240		0	1015 09A51			1	001	ACRZER12
5,8		ARI	ARI1	600		1	1015 08B57	S	0		002	5,8/ 0,0
5,8		MEM	MEM	255		0	1015 09A54			1	001	ACRZER04
5,8		ARI	ARI4	615		1	1015 06B57	S	0		002	5,8/ 0,0
5,0		MEM	MEM	250		0	1015 09A53			1	001	ACRZER08
5,0		ARI	ARI8	605		1	1015 07B57	S	0		002	5,0/ 0,0
0,5		PFS	PFS	275		0	1015 17A08			1	001	ACSHIELD
0,5		PFS	PFS	265		1	1015 17A07			0	002	0,5/ 0,0
1,0		ARI	ARI8	660		0	1015 07B68			1	001	ACSLENB
0,8		ARI	ARI0	655		1	1015 05B68			2	002	
0,5		ARI	ARI0	590		2	1015 05B55			1	003	
0,5		ARI	ARI4	605		1	1015 06B55			2	004	
0,5		ARI	ARI8	595		2	1015 07B55			1	005	
5,8		ARI	ARI1	590		1	1015 08B55			2	006	
9,1		INR	INR	245		2	1015 03A52	S	0		007	9,1/ 0,0
0,5		INR	INR	235		0	1015 03A50			1	001	ACSLOPT=
0,5		M=D	M=D	355		1	1015 04A46	S	0		002	0,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
0,5		ARI	ARI1	630		0	1015 08B63		1	001	ACSRENB
0,5		ARI	ARI8	635		1	1015 07B63		2	002	
0,5		ARI	ARI4	645		2	1015 06B63		1	003	
0,8		ARI	ARI0	630		1	1015 05B63		2	004	
0,5		ARI	ARI4	585		2	1015 06B51		1	005	
0,5		ARI	ARI0	570		1	1015 05B51		2	006	
0,5		ARI	ARI4	565		2	1015 06B47		1	007	
0,5		ARI	ARI8	575		1	1015 07B51		2	008	
0,5		ARI	ARI1	570		2	1015 08B51		1	009	
6,5		ARI	ARI1	550		1	1015 08B47		2	010	
11,3		INR	INR	120		2	1015 03A27	S	0	011	11,3/ 0,0
2,5		INR	INR	345		0	1015 03B04		1	001	ACSROPT=
2,5		M=D	M=D	345		1	1015 04A48	S	0	002	2,5/ 0,0
1,0		INR	INR	195		0	1015 03A42		1	001	ACSROPT1=
1,0		M=D	M=D	340		1	1015 04A21	S	0	002	1,0/ 0,0
7,5		PFS	PFS	165		0	1015 17B34	S	1	001	ADA00=
2,5		ARI	ARI0	345		1	1015 05B04	S	2	002	
2,0		ADF	ADF	320		2	1015 01A67		1	003	
12,0		M=D	M=D	385		1	1015 04A42	S	0	004	12,0/ 0,0
8,5		PFS	PFS	170		0	1015 17B33	S	1	001	ADA01=
2,5		M=D	M=D	465		1	1015 04B57		2	002	
4,3		ARI	ARI0	390		2	1015 05R14	S	1	003	
15,3		M=D	M=D	390		1	1015 04A35	S	0	004	15,3/ 0,0
7,5		PFS	PFS	175		0	1015 17B32	S	1	001	ADA02=
5,0		ARI	ARI0	445		1	1015 05B26	S	2	002	
12,5		M=D	M=D	395		2	1015 04A26	S	0	003	12,5/ 0,0
7,5		PFS	PFS	180		0	1015 17B31	S	1	001	ADA03=
5,8		ARI	ARI0	475		1	1015 05B32	S	2	002	
13,3		M=D	M=D	400		2	1015 04A23	S	0	003	13,3/ 0,0
7,5		PFS	PFS	185		0	1015 17B23	S	1	001	ADA04=
4,3		ARI	ARI4	350		1	1015 06B04	S	2	002	
11,8		M=D	M=D	405		2	1015 04A19	S	0	003	11,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LO WT	WSEQ	SIGNAL NAME
7,5		PFS	PFS	190	0	1015 17B22	S	1	001	ADA05=
5,0		ARI	ARI4	400	1	1015 06B14	S	2	002	
12,5		M=D	M=D	410	2	1015 04A22	S	0	003	12,5/ 0,0
7,5		PFS	PFS	195	0	1015 17B21	S	1	001	ADA06=
5,8		ARI	ARI4	460	1	1015 06B26	S	2	002	
13,3		M=D	M=D	415	2	1015 04A10	S	0	003	13,3/ 0,0
7,5		PFS	PFS	200	0	1015 17B20	S	1	001	ADA07=
6,5		ARI	ARI4	490	1	1015 06B32	S	2	002	
14,0		M=D	M=D	420	2	1015 04A07	S	0	003	14,0/ 0,0
5,0		M=D	M=D	425	0	1015 04A38	S	1	001	ADA08=
3,0		ADF	ADF	490	1	1015 01B33		2	002	
6,5		ARI	ARI8	345	2	1015 07B04	S	1	003	
14,5		PFS	PFS	205	1	1015 17B06	S	0	004	14,5/ 0,0
6,5		PFS	PFS	210	0	1015 17B05	S	1	001	ADA09=
4,3		ARI	ARI8	395	1	1015 07B14	S	2	002	
10,8		M=D	M=D	430	2	1015 04A33	S	0	003	10,8/ 0,0
6,5		PFS	PFS	215	0	1015 17B04	S	1	001	ADA10=
5,0		ARI	ARI8	455	1	1015 07B26	S	2	002	
11,5		M=D	M=D	435	2	1015 04A27	S	0	003	11,5/ 0,0
6,5		PFS	PFS	220	0	1015 17B03	S	1	001	ADA11=
5,0		ARI	ARI8	485	1	1015 07B32	S	2	002	
11,5		M=D	M=D	440	2	1015 04A32	S	0	003	11,5/ 0,0
6,5		PFS	PFS	225	0	1015 17A70	S	1	001	ADA12=
5,0		ARI	ARI1	345	1	1015 08B04	S	2	002	
11,5		M=D	M=D	445	2	1015 04A18	S	0	003	11,5/ 0,0
6,5		PFS	PFS	230	0	1015 17A69	S	1	001	ADA13=
5,8		ARI	ARI1	395	1	1015 08B14	S	2	002	
12,3		M=D	M=D	450	2	1015 04A13	S	0	003	12,3/ 0,0
6,5		PFS	PFS	235	0	1015 17A68	S	1	001	ADA14=
5,8		ARI	ARI1	450	1	1015 08B26	S	2	002	
12,3		M=D	M=D	455	2	1015 04A12	S	0	003	12,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LO WT	WSEQ	SIGNAL NAME
6,5		PFS	PFS	240	0	1015 17A67	S	1	001	ADA15=
6,5		ARI	ARI1	480	1	1015 08B32	S	2	002	
13,0		M=D	M=D	460	2	1015 04A16	S	0	003	13,0/ 0,0
2,0		M=D	M=D	115	0	1015 04A44		1	001	ADB00=
2,5		ADF	ADF	330	1	1015 01A69		2	002	
4,5		ARI	ARI0	355	2	1015 05B06	S	0	003	4,5/ 0,0
0,0		ARI	ARI4	360	0	1015 06B06	S	0	001	ADB04=
3,0		ADF	ADF	480	0	1015 01B31		1	001	ADB08=
3,0		ARI	ARI8	355	1	1015 07B06	S	0	002	3,0/ 0,0
0,0		ARI	ARI1	355	0	1015 08B06	S	0	001	ADB12=
2,5		ADF	ADF	510	0	1015 01B37		1	001	ADBZER00
2,5		ARI	ARI0	635	1	1015 05B64	S	0	002	2,5/ 0,0
3,5		ADF	ADF	520	0	1015 01B39		1	001	ADBZER012
3,5		ARI	ARI1	635	1	1015 08B64	S	0	002	3,5/ 0,0
3,0		ADF	ADF	500	0	1015 01B35		1	001	ADBZER04
3,0		ARI	ARI4	650	1	1015 06B64	S	0	002	3,0/ 0,0
3,0		ADF	ADF	530	0	1015 01B41		1	001	ADBZER08
3,0		ARI	ARI8	640	1	1015 07B64	S	0	002	3,0/ 0,0
0,0		ARI	ARI0	335	0	1015 05A70	S	0	001	ADC00=
1,5		M=D	M=D	030	0	1015 04B56		1	001	ADC02=
1,5		ARI	ARI0	440	1	1015 05B25	S	0	002	1,5/ 0,0
2,5		ARI	ARI0	405	0	1015 05B18		1	001	ADC04=
2,5		ARI	ARI4	340	1	1015 06A70	S	0	002	2,5/ 0,0
0,0		ARI	ARI4	455	0	1015 06B25	S	0	001	ADC06=

C	LNTH	NOTE	CKT	EQUATION	EQL	EO	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
	2,5		ARI	ARI4	420		0	1015 06B18			1	001	ADC08=
	2,5		ARI	ARI8	340		1	1015 07A70	S		0	002	2,5/ 0,0
	0,0		ARI	ARI8	450		0	1015 07B25	S		0	001	ADC10=
	2,5		ARI	ARI8	415		0	1015 07B18			1	001	ADC12=
	2,5		ARI	ARI1	335		1	1015 08A70	S		0	002	2,5/ 0,0
	0,0		ARI	ARI1	445		0	1015 08B25	S		0	001	ADC14=
	2,0		INR	INR	590		0	1015 03B53	S		1	001	ADENAC
	0,5		ARI	ARI0	420		1	1015 05B21			2	002	
	0,5		ARI	ARI4	435		2	1015 06B21			1	003	
	0,5		ARI	ARI8	430		1	1015 07B21			2	004	
	3,5		ARI	ARI1	425		2	1015 08B21			0	005	3,5/ 0,0
	0,0		INR	INR	370		0	1015 03B09			0	001	ADENAC2=
	1,0		INR	INR	570		0	1015 03B49	S		1	001	ADENACC
	0,5		ARI	ARI0	510		1	1015 05B39			2	002	
	0,5		ARI	ARI4	525		2	1015 06B39			1	003	
	0,5		ARI	ARI8	515		1	1015 07B39			2	004	
	2,5		ARI	ARI1	510		2	1015 08B39			0	005	2,5/ 0,0
	0,5		INR	INR	580		0	1015 03B51			1	001	ADENACCOP=
	0,5		M=D	M=D	315		1	1015 04B53	S		0	002	0,5/ 0,0
	0,5		ARI	ARI4	520		0	1015 06B38			1	001	ADENACRB
	1,3		ARI	ARI0	505		1	1015 05B38			2	002	
	1,8		INR	INR	600		2	1015 03B55	S		0	003	1,8/ 0,0
	0,8		ARI	ARI4	410		0	1015 06B16			1	001	ADENEXB
	1,3		ARI	ARI0	365		1	1015 05B08			2	002	
	2,1		INR	INR	450		2	1015 03B25	S		0	003	2,1/ 0,0
	3,0		INR	INR	255		0	1015 03A54	S		1	001	ADENEXW
	1,0		ARI	ARI4	395		1	1015 06B13			2	002	
	4,0		ARI	ARI0	460		2	1015 05B29			0	003	4,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
1,3		INR	INR	440	0	1015 03B23	S	1	001	ADENIX
0,5		ARI	ARI0	485	1	1015 05B34		2	002	
0,5		ARI	ARI4	500	2	1015 06B34		1	003	
0,5		ARI	ARI8	495	1	1015 07B34		2	004	
2,8		ARI	ARI1	490	2	1015 08B34		0	005	2,8/ 0,0
1,3		M=D	M=D	495	0	1015 04B36	S	1	001	ADENIX2=
1,3		INR	INR	380	1	1015 03B11	S	0	002	1,3/ 0,0
0,8		INR	INR	170	0	1015 03A37		1	001	ADENMBA=
1,3		SCD	SCDC	220	1	1015 02A50	S	2	002	
2,1		M=D	M=D	375	2	1015 04A69	S	0	003	2,1/ 0,0
0,5		ARI	ARI1	365	0	1015 08B08		1	001	ADENMBB
2,5		ARI	ARI8	365	1	1015 07B08		2	002	
3,0		INR	INR	340	2	1015 03B43	S	0	003	3,0/ 0,0
0,5		ARI	ARI8	390	0	1015 07B13		1	001	ADENMBBC
1,0		ARI	ARI1	390	1	1015 08B13		2	002	
0,5		ARI	ARI8	470	2	1015 07B29		1	003	
2,5		ARI	ARI1	465	1	1015 08B29		2	004	
4,5		INR	INR	620	2	1015 03B59	S	0	005	4,5/ 0,0
0,8		INR	INR	455	0	1015 03B26	S	1	001	ADENMBC
0,5		ARI	ARI0	490	1	1015 05B35		2	002	
0,5		ARI	ARI4	505	2	1015 06B35		1	003	
0,5		ARI	ARI8	500	1	1015 07B35		2	004	
2,3		ARI	ARI1	495	2	1015 08B35		0	005	2,3/ 0,0
2,5		M=D	M=D	380	0	1015 04A56	S	1	001	ADENMBC2=
2,5		INR	INR	360	1	1015 03B07	S	0	002	2,5/ 0,0
2,0		ADF	ADF	340	0	1015 01B03		1	001	ADENMBC3=
2,0		INR	INR	475	1	1015 03B30	S	0	002	2,0/ 0,0
2,0		ARI	ARI0	500	0	1015 05B37		1	001	ADENMBL
0,5		ARI	ARI0	340	1	1015 05B03		2	002	
1,5		ARI	ARI4	345	2	1015 06B03		1	003	
2,5		ARI	ARI0	320	1	1015 05A67		2	004	
6,5		INR	INR	105	2	1015 03A24	S	0	005	6,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
3,0		INR	INR	090		0	1015 03A21	S	1		001	ADENMBR
0,5		ARI	ARI8	320		1	1015 07A67			2	002	
1,5		ARI	ARI1	320		2	1015 08A67			1	003	
0,5		ARI	ARI8	335		1	1015 07B03			2	004	
2,0		ARI	ARI1	340		2	1015 08B03			1	005	
0,5		ARI	ARI4	515		1	1015 06B37			2	006	
0,5		ARI	ARI8	510		2	1015 07B37			1	007	
8,5		ARI	ARI1	505		1	1015 08B37			0	008	8,5/ 0,0
0,5		ARI	ARI0	520		0	1015 05B41			1	001	ADENPC
0,5		ARI	ARI4	535		1	1015 06B41			2	002	
0,5		ARI	ARI8	525		2	1015 07B41			1	003	
7,5		ARI	ARI1	520		1	1015 08B41			2	004	
9,0		INR	INR	025		2	1015 03A08	S	0		005	9,0/ 0,0
6,5		INR	INR	160		0	1015 03A35			1	001	ADENPC2=
1,3		SCD	SCDC	585		1	1015 02B67	S	2		002	
8,5		M=D	M=D	485		2	1015 04B50	S	1		003	
16,3		PFS	PFS	150		1	1015 17B13	S	0		004	16,3/ 0,0
5,8		MEM	MEM	105		0	1015 09A24			1	001	ADFEQL
2,0		ARI	ARI4	465		1	1015 06B27			2	002	
7,8		ADF	ADF	465		2	1015 01B28	S	0		003	7,8/ 0,0
3,5		MEM	MEM	100		0	1015 09A23			1	001	ADFEQL=
3,5		ADF	ADF	230		1	1015 01A49	S	0		002	3,5/ 0,0
2,5		ARI	ARI4	390		0	1015 06B12			1	001	ADFNEG
2,5		ADF	ADF	455		1	1015 01B26	S	0		002	2,5/ 0,0
5,8		MEM	MEM	080		0	1015 09A19			1	001	ADFNEG=
5,8		ADF	ADF	375		1	1015 01B10	S	0		002	5,8/ 0,0
5,0		MEM	MEM	145		0	1015 09A32			1	001	ADFOVF
2,0		ARI	ARI4	480		1	1015 06B30			2	002	
7,0		ADF	ADF	435		2	1015 01B22	S	0		003	7,0/ 0,0
1,3		M=D	M=D	305		0	1015 04B51	S	1		001	ADFOVFR1=
1,3		ADF	ADF	560		1	1015 01B47	S	0		002	1,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EC	LI	LOCATION	S	LC	WT	WSEQ	SIGNAL NAME
6,5		M=D	M=D	360		0	1015 04A41	S	1		001	ADFOVFS=
6,5		ADF	ADF	645		1	1015 01B64	S	0		002	6,5/ 0,0
2,5		ARI	ARI1	410		0	1015 08B18		1		001	ADINCRY
2,5		INR	INR	430		1	1015 03B21	S	0		002	2,5/ 0,0
8,5		PFS	PFS	135		0	1015 17B17	S	1		001	ADINCRYC=
0,8		INR	INR	395		1	1015 03B14		2		002	
3,0		M=D	M=D	370		2	1015 04B03	S	1		003	
12,3		SCD	SCDC	170		1	1015 02A39	S	0		004	12,3/ 0,0
1,0		ARI	ARI4	380		0	1015 06B10		1		001	ADONES
0,5		ARI	ARI4	470		1	1015 06B28		2		002	
1,3		ARI	ARI4	475		2	1015 06B29		1		003	
2,8		INR	INR	520		1	1015 03B39	S	0		004	2,8/ 0,0
2,0		ADF	ADF	450		0	1015 01B25		1		001	ADOR00=
2,0		ARI	ARI0	425		1	1015 05B22	S	0		002	2,0/ 0,0
0,0		ARI	ARI4	440		0	1015 06B22	S	0		001	ADOR04=
2,5		ADF	ADF	385		0	1015 01B12		1		001	ADOR08=
2,5		ARI	ARI8	435		1	1015 07B22	S	0		002	2,5/ 0,0
0,0		ARI	ARI1	430		0	1015 08B22	S	0		001	ADOR12=
3,0		SCD	SCDC	580		0	1015 02B66		1		001	ADSUM00=
3,0		ADF	ADF	360		1	1015 01B07		2		002	
2,0		M=D	M=D	110		2	1015 04A52		1		003	
8,0		ARI	ARI0	045		1	1015 05A12	S	0		004	8,0/ 0,0
1,3		ADF	ADF	365		0	1015 01B08	S	1		001	ADSUM00A
1,5		M=D	M=D	120		1	1015 04B18		2		002	
2,8		SCD	SCDC	445		2	1015 02B39		0		003	2,8/ 0,0
2,5		ARI	ARI0	075		0	1015 05A18	S	1		001	ADSUM01=
1,3		M=D	M=D	155		1	1015 04A63		2		002	
3,8		ADF	ADF	300		2	1015 01A63		0		003	3,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
2,0		M=D	M=D	160	0	1015 04A37		1	001	ADSUM02=
2,0		ADF	ADF	160	1	1015 01A35		2	002	
4,0		ARI	ARI0	100	2	1015 05A23	S	0	003	4,0/ 0,0
4,3		M=D	M=D	165	0	1015 04B14		1	001	ADSUM03=
2,0		ADF	ADF	170	1	1015 01A37		2	002	
1,3		ARI	ARI0	140	2	1015 05A31	S	1	003	
7,6		ARI	ARI4	015	1	1015 06A05		0	004	7,6/ 0,0
2,5		ARI	ARI4	050	0	1015 06A12	S	1	001	ADSUM04=
3,5		ADF	ADF	185	1	1015 01A40		2	002	
1,0		M=D	M=D	170	2	1015 04B07		1	003	
7,0		ARI	ARI4	355	1	1015 06B05		0	004	7,0/ 0,0
5,0		M=D	M=D	175	0	1015 04B13		1	001	ADSUM05=
2,0		ARI	ARI4	080	1	1015 06A18	S	2	002	
7,0		ADF	ADF	015	2	1015 01A06		0	003	7,0/ 0,0
4,3		M=D	M=D	180	0	1015 04B08		1	001	ADSUM06=
4,3		ARI	ARI4	105	1	1015 06A23	S	0	002	4,3/ 0,0
1,3		ARI	ARI8	010	0	1015 07A05		1	001	ADSUM07=
4,3		ARI	ARI4	145	1	1015 06A31	S	2	002	
5,6		M=D	M=D	185	2	1015 04B09		0	003	5,6/ 0,0
2,0		ADF	ADF	350	0	1015 01B05		1	001	ADSUM08=
1,3		M=D	M=D	190	1	1015 04B24		2	002	
5,0		ARI	ARI8	350	2	1015 07B05		1	003	
8,3		ARI	ARI8	045	1	1015 07A12	S	0	004	8,3/ 0,0
6,5		M=D	M=D	200	0	1015 04B39		1	001	ADSUM09=
6,5		ARI	ARI8	075	1	1015 07A18	S	0	002	6,5/ 0,0
5,8		M=D	M=D	195	0	1015 04B27		1	001	ADSUM10=
5,8		ARI	ARI8	100	1	1015 07A23	S	0	002	5,8/ 0,0
1,3		ARI	ARI1	010	0	1015 08A05		1	001	ADSUM11=
5,0		ARI	ARI8	140	1	1015 07A31	S	2	002	
6,3		M=D	M=D	205	2	1015 04B29		0	003	6,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
5,0		ARI	ARI1	045	0	1015 08A12	S	1	001	ADSUM12=
2,5		ARI	ARI1	350	1	1015 08B05		2	002	
7,5		M=D	M=D	210	2	1015 04B41		0	003	7,5/ 0,0
6,5		M=D	M=D	215	0	1015 04B44		1	001	ADSUM13=
6,5		ARI	ARI1	075	1	1015 08A18	S	0	002	6,5/ 0,0
5,8		M=D	M=D	220	0	1015 04B40		1	001	ADSUM14=
5,8		ARI	ARI1	100	1	1015 08A23	S	0	002	5,8/ 0,0
2,5		ARI	ARI1	140	0	1015 08A31	S	1	001	ADSUM15=
2,5		M=D	M=D	105	1	1015 04A67		2	002	
5,0		ADF	ADF	115	2	1015 01A26		0	003	5,0/ 0,0
1,5		ARI	ARI1	645	0	1015 08B66		1	001	BPGND
0,5		ARI	ARI1	500	1	1015 08B36		2	002	
0,8		ARI	ARI8	505	2	1015 07B36		1	003	
0,5		ARI	ARI1	435	1	1015 08B23		2	004	
0,5		ARI	ARI1	420	2	1015 08B20		1	005	
0,5		ARI	ARI1	415	1	1015 08B19		2	006	
0,5		ARI	ARI8	440	2	1015 07B23		1	007	
1,0		ARI	ARI8	425	1	1015 07B20		2	008	
0,8		ARI	ARI4	485	2	1015 06B31		1	009	
0,5		ARI	ARI0	410	1	1015 05B19		2	010	
0,5		ARI	ARI0	380	2	1015 05B11		1	011	
2,0		ARI	ARI4	375	1	1015 06B09		2	012	
0,5		ARI	ARI1	325	2	1015 08A68		1	013	
3,0		ARI	ARI8	325	1	1015 07A68		2	014	
0,8		ARI	ARI0	055	2	1015 05A14	S	1	015	
13,9		ARI	ARI4	010	1	1015 06A03	S	0	016	13,9/ 0,0
0,0		PFS	PFS	010	0	1015 17B08		0	001	BSRMT=
3,5		MEM	MEM	670	0	1015 09B61		1	001	CCCLKEN
3,5		SCD	SCDC	345	1	1015 02B19	S	0	002	3,5/ 0,0
4,3		M=D	M=D	530	0	1015 04A68	S	1	001	CCCMEND1=
4,3		SCD	SCDC	540	1	1015 02B58	S	0	002	4,3/ 0,0
3,5		SCD	SCDC	395	0	1015 02B29		1	001	CCCMEND3=
3,5		MEM	MEM	555	1	1015 09B48	S	0	002	3,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
4,3		SCD	SCDC	465		0	1015 02B43			1	001	CCCMEND4
4,3		INR	INR	290		1	1015 03A61	S		0	002	4,3/ 0,0
3,5		SCD	SCDC	440		0	1015 02B38			1	001	CCCMEND5
3,5		INR	INR	310		1	1015 03A65	S		0	002	3,5/ 0,0
0,8		SCD	SCDC	530		0	1015 02B56			1	001	CCCMEND6=
0,8		M=D	M=D	310		1	1015 04B61	S		0	002	0,8/ 0,0
3,0		SCD	SCDC	475		0	1015 02B45			1	001	CCCMEND7=
3,0		MEM	MEM	430		1	1015 09B23	S		0	002	3,0/ 0,0
3,5		ADF	ADF	240		0	1015 01A51	S		1	001	CCFBYTE=
5,0		MEM	MEM	305		1	1015 09A64			2	002	
8,5		INR	INR	605		2	1015 03B56			0	003	8,5/ 0,0
8,5		DAM	DAM	010		0	1015 14A07	S		1	001	CCFCLK
3,5		MEM	MEM	665		1	1015 09B60			2	002	
12,0		SCD	SCDC	355		2	1015 02B21			0	003	12,0/ 0,0
3,5		ADF	ADF	335		0	1015 01A70	S		1	001	CCFGLB
2,5		ARI	ARI8	420		1	1015 07B19			2	002	
6,0		INR	INR	625		2	1015 03B60			0	003	6,0/ 0,0
5,8		MEM	MEM	475		0	1015 09B32			1	001	CCFRST=
5,8		SCD	SCDC	175		1	1015 02A40	S		0	002	5,8/ 0,0
8,5		SCD	SCDC	545		0	1015 02B59			1	001	CCFSKP
8,5		MEM	MEM	025		1	1015 09A08	S		0	002	8,5/ 0,0
6,5		SCD	SCDC	380		0	1015 02B26			1	001	CCFSKP=
6,5		MEM	MEM	035		1	1015 09A10	S		0	002	6,5/ 0,0
3,0		MEM	MEM	340		0	1015 09B03			1	001	CCFSSTP=
3,0		SCD	SCDC	420		1	1015 02B34	S		0	002	3,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
5,0		DAM	DAM	130	0	1015 14A66		1	001	CCFSYN1
4,3		MEM	MEM	355	1	1015 09B06		2	002	
9,3		SCD	SCDC	185	2	1015 02A43	S	0	003	9,3/ 0,0
5,8		SCD	SCDC	385	0	1015 02B27		1	001	CCITCY
5,8		ADF	ADF	040	1	1015 01A11	S	0	002	5,8/ 0,0
4,3		MEM	MEM	345	0	1015 09B04		1	001	CPDIAEN
4,3		SCD	SCDC	520	1	1015 02B54	S	0	002	4,3/ 0,0
9,5		SCD	SCDC	115	0	1015 02A26		1	001	CPRUN=
9,5		PFS	PFS	160	1	1015 17B11	S	0	002	9,5/ 0,0
7,5		PFS	PFS	115	0	1015 17B37		1	001	CPSENS0
3,5		MEM	MEM	165	1	1015 09A36		2	002	
11,0		SCD	SCDC	030	2	1015 02A09	S	0	003	11,0/ 0,0
7,5		PFS	PFS	120	0	1015 17B38		1	001	CPSENS1
3,5		MEM	MEM	175	1	1015 09A38		2	002	
11,0		SCD	SCDC	040	2	1015 02A11	S	0	003	11,0/ 0,0
3,5		MEM	MEM	185	0	1015 09A40		1	001	CPSENS2
3,5		SCD	SCDC	010	1	1015 02A05	S	0	002	3,5/ 0,0
3,5		MEM	MEM	170	0	1015 09A37		1	001	CPSENS3
3,5		SCD	SCDC	020	1	1015 02A07	S	0	002	3,5/ 0,0
4,3		MEM	MEM	330	0	1015 09A69		1	001	CPSSTP
4,3		SCD	SCDC	025	1	1015 02A08	S	0	002	4,3/ 0,0
8,5		PI	PI	010	0	1015 15A07		1	001	CPSWRST=
8,5		SCD	SCDC	200	1	1015 02A46		0	002	8,5/ 0,0
6,5		TTY	TTY	255	0	1015 16B37		1	001	DAD08=
6,5		MEM	MEM	225	1	1015 09A48	S	0	002	6,5/ 0,0
7,5		TTY	TTY	260	0	1015 16B39		1	001	DAD09=
7,5		MEM	MEM	220	1	1015 09A47	S	0	002	7,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
0,5		TTY	TTY	265		0	1015 16B41		1	001	DAD10=
6,5		MEM	MEM	310		1	1015 09A65	S	0	002	6,5/ 0,0
6,5		TTY	TTY	290		0	1015 16B51		1	001	DAD11=
6,5		MEM	MEM	315		1	1015 09A66	S	0	002	6,5/ 0,0
11,5		TTY	TTY	320		0	1015 16B63		1	001	DAD12=
11,5		ADF	ADF	120		1	1015 01A27	S	0	002	11,5/ 0,0
11,5		TTY	TTY	315		0	1015 16B61		1	001	DAD13=
11,5		ADF	ADF	100		1	1015 01A23	S	0	002	11,5/ 0,0
11,5		TTY	TTY	310		0	1015 16B59		1	001	DAD14=
11,5		ADF	ADF	090		1	1015 01A21	S	0	002	11,5/ 0,0
10,5		TTY	TTY	305		0	1015 16B57		1	001	DAD15=
10,5		ADF	ADF	110		1	1015 01A25	S	0	002	10,5/ 0,0
9,5		ARI	ARIO	560		0	1015 05B49		1	001	DIN00=
9,5		TTY	TTY	085		1	1015 16A35	S	0	002	9,5/ 0,0
8,5		ARI	ARIO	545		0	1015 05B46		1	001	DIN01=
8,5		TTY	TTY	080		1	1015 16A33	S	0	002	8,5/ 0,0
9,5		ARI	ARIO	605		0	1015 05B58		1	001	DIN02=
9,5		TTY	TTY	075		1	1015 16A31	S	0	002	9,5/ 0,0
9,5		ARI	ARIO	615		0	1015 05B60		1	001	DIN03=
9,5		TTY	TTY	070		1	1015 16A29	S	0	002	9,5/ 0,0
9,5		ARI	ARI4	575		0	1015 06B49		1	001	DIN04=
9,5		TTY	TTY	065		1	1015 16A27	S	0	002	9,5/ 0,0
8,5		ARI	ARI4	560		0	1015 06B46		1	001	DIN05=
8,5		TTY	TTY	060		1	1015 16A25	S	0	002	8,5/ 0,0

C	LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LB	WT	WSEQ	SIGNAL NAME
	9,5		ARI	ARI4	620		0	1015 06B58			1	001	DIN06=
	9,5		TTY	TTY	055		1	1015 16A23	S	0		002	9,5/ 0,0
	9,5		ARI	ARI4	630		0	1015 06B60			1	001	DIN07=
	9,5		TTY	TTY	050		1	1015 16A21	S	0		002	9,5/ 0,0
	9,5		ARI	ARI8	565		0	1015 07B49			1	001	DIN08=
	9,5		TTY	TTY	045		1	1015 16A19	S	0		002	9,5/ 0,0
	8,5		ARI	ARI8	550		0	1015 07B46			1	001	DIN09=
	8,5		TTY	TTY	040		1	1015 16A17	S	0		002	8,5/ 0,0
	9,5		ARI	ARI8	610		0	1015 07B58			1	001	DIN10=
	9,5		TTY	TTY	035		1	1015 16A15	S	0		002	9,5/ 0,0
	9,5		ARI	ARI8	620		0	1015 07B60			1	001	DIN11=
	9,5		TTY	TTY	030		1	1015 16A13	S	0		002	9,5/ 0,0
	9,5		ARI	ARI1	560		0	1015 08B49			1	001	DIN12=
	9,5		TTY	TTY	025		1	1015 16A11	S	0		002	9,5/ 0,0
	8,5		ARI	ARI1	545		0	1015 08B46			1	001	DIN13=
	8,5		TTY	TTY	020		1	1015 16A09	S	0		002	8,5/ 0,0
	9,5		ARI	ARI1	605		0	1015 08B58			1	001	DIN14=
	9,5		TTY	TTY	015		1	1015 16A07	S	0		002	9,5/ 0,0
	9,5		ARI	ARI1	615		0	1015 08B60			1	001	DIN15=
	9,5		TTY	TTY	010		1	1015 16A05	S	0		002	9,5/ 0,0
	10,5		TTY	TTY	300		0	1015 16B55			1	001	DISB=
	10,5		ADF	ADF	225		1	1015 01A48	S	0		002	10,5/ 0,0
			SCDC M/D				0	1015 02A30	S		1	001	DISPIN
							1	1015 04B30			0	002	
	8,5		TTY	TTY	295		0	1015 16B53			1	001	DOSB=
	8,5		ADF	ADF	415		1	1015 01B18	S	0		002	8,5/ 0,0

C	LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LO	WT	WSEQ	SIGNAL NAME
	7,5		TTY	TTY	165		0	1015 16A67			1	001	DOT00=
	7,5		ARI	ARI0	360		1	1015 05B07	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	160		0	1015 16A65			1	001	DOT01=
	7,5		ARI	ARI0	395		1	1015 05B15	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	155		0	1015 16A63			1	001	DOT02=
	7,5		ARI	ARI0	435		1	1015 05B24	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	150		0	1015 16A61			1	001	DOT03=
	7,5		ARI	ARI0	480		1	1015 05B33	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	145		0	1015 16A59			1	001	DOT04=
	7,5		ARI	ARI4	365		1	1015 06B07	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	140		0	1015 16A57			1	001	DOT05=
	7,5		ARI	ARI4	405		1	1015 06B15	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	135		0	1015 16A55			1	001	DOT06=
	7,5		ARI	ARI4	450		1	1015 06B24	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	130		0	1015 16A53			1	001	DOT07=
	7,5		ARI	ARI4	495		1	1015 06B33	S	0		002	7,5/ 0,0
	6,5		TTY	TTY	125		0	1015 16A51			1	001	DOT08=
	6,5		ARI	ARI8	360		1	1015 07B07	S	0		002	6,5/ 0,0
	7,5		TTY	TTY	120		0	1015 16A49			1	001	DOT09=
	7,5		ARI	ARI8	400		1	1015 07B15	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	115		0	1015 16A47			1	001	DOT10=
	7,5		ARI	ARI8	445		1	1015 07B24	S	0		002	7,5/ 0,0
	7,5		TTY	TTY	110		0	1015 16A45			1	001	DOT11=
	7,5		ARI	ARI8	490		1	1015 07B33	S	0		002	7,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
6,5		TTY	TTY	105	0	1015 16A43		1	001	DOT12=
6,5		ARI	ARI1	360	1	1015 08B07	S	0	002	6,5/ 0,0
6,5		TTY	TTY	100	0	1015 16A41		1	001	DOT13=
6,5		ARI	ARI1	400	1	1015 08B15	S	0	002	6,5/ 0,0
7,5		TTY	TTY	095	0	1015 16A39		1	001	DOT14=
7,5		ARI	ARI1	440	1	1015 08B24	S	0	002	7,5/ 0,0
7,5		TTY	TTY	090	0	1015 16A37		1	001	DOT15=
7,5		ARI	ARI1	485	1	1015 08B33	S	0	002	7,5/ 0,0
1,0		ADF	ADF	270	0	1015 01A57		1	001	EXLDAD1=
1,0		INR	INR	315	1	1015 03A66	S	0	002	1,0/ 0,0
5,0		ADF	ADF	205	0	1015 01A44		1	001	EXLDADSR1=
5,0		SCD	SCDC	470	1	1015 02B44	S	0	002	5,0/ 0,0
7,5		ADF	ADF	150	0	1015 01A33		1	001	EXLDMB *
7,5		MEM	MEM	680	1	1015 09B63	S	0	002	7,5/ 0,0
6,5		ADF	ADF	085	0	1015 01A20		1	001	EXLDPC
6,5		INR	INR	555	1	1015 03B46	S	0	002	6,5/ 0,0
0,5		ARI	ARIO	375	0	1015 05B10		1	001	EXR00
3,0		ARI	ARIO	370	1	1015 05B09		2	002	
3,5		ADF	ADF	245	2	1015 01A52	S	0	003	3,5/ 0,0
1,0		ARI	ARIO	470	0	1015 05B31		1	001	EXR01
5,0		ARI	ARIO	385	1	1015 05B12		2	002	
6,0		ADF	ADF	105	2	1015 01A24	S	0	003	6,0/ 0,0
0,5		ARI	ARIO	455	0	1015 05B28		1	001	EXR02
5,0		ARI	ARIO	450	1	1015 05B27		2	002	
5,5		ADF	ADF	165	2	1015 01A36	S	0	003	5,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EC	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
4,3		ADF	ADF	200		0	1015 01A43	S	1		001	EXR03
1,0		ARI	ARI4	385		1	1015 06B11		2		002	
5,3		ARI	ARIO	465		2	1015 05B30		0		003	5,3/ 0,0
5,0		ARI	ARI4	425		0	1015 06B19		1		001	EXR04
5,0		ADF	ADF	130		1	1015 01A29	S	0		002	5,0/ 0,0
5,8		TTY	TTY	325		0	1015 16B65		1		001	EXSENS=
5,8		PFS	PFS	295		1	1015 17A51	S	2		002	
11,6		MEM	MEM	285		2	1015 09A60		0		003	11,6/ 0,0
6,5		ADF	ADF	155		0	1015 01A34		1		001	ICDC0
0,8		SCD	SCDC	550		1	1015 02B60		2		002	
2,5		M=D	M=D	125		2	1015 04B67		1		003	
9,8		MEM	MEM	695		1	1015 09B66	S	0		004	9,8/ 0,0
1,3		INR	INR	150		0	1015 03A33		1		001	ICDC0=
1,3		M=D	M=D	090		1	1015 04A54		2		002	
3,5		SCD	SCDC	285		2	1015 02A69		1		003	
3,5		ADF	ADF	545		1	1015 01B44		2		004	
9,6		MEM	MEM	705		2	1015 09B68	S	0		005	9,6/ 0,0
7,5		MEM	MEM	565		0	1015 09B50		1		001	ICDECOPT=
7,5		M=D	M=D	570		1	1015 04A08	S	0		002	7,5/ 0,0
2,5		MEM	MEM	455		0	1015 09B28	S	1		001	ICR0=
5,8		M=D	M=D	130		1	1015 04B25		2		002	
8,3		SCD	SCDC	075		2	1015 02A18		0		003	8,3/ 0,0
2,5		MEM	MEM	395		0	1015 09B16	S	1		001	ICR1=
5,0		M=D	M=D	135		1	1015 04B23		2		002	
7,5		SCD	SCDC	085		2	1015 02A20		0		003	7,5/ 0,0
2,0		M=D	M=D	140		0	1015 04B21		1		001	ICR2=
5,0		MEM	MEM	375		1	1015 09B11	S	2		002	
7,0		SCD	SCDC	100		2	1015 02A23		0		003	7,0/ 0,0
3,0		MEM	MEM	685		0	1015 09B64	S	1		001	ICR3=
5,0		M=D	M=D	145		1	1015 04B00		2		002	
8,0		SCD	SCDC	110		1	1015 02A25		0		002	8,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LO	WT	WSEQ	SIGNAL NAME
2,5		ARI	ARI4	325		0	1015 06A67			1	001	IN04SC1=
2,5		INR	INR	390		1	1015 03B13	S		0	002	2,5/ 0,0
2,0		ADF	ADF	425		0	1015 01B20			1	001	IN4SC5
2,0		INR	INR	610		1	1015 03B57	S		0	002	2,0/ 0,0
7,5		SCD	SCDC	500		0	1015 02B50			1	001	INDC0
7,5		INR	INR	010		1	1015 03A05	S		0	002	7,5/ 0,0
0,8		SCD	SCDC	495		0	1015 02B49			1	001	INDC0=
0,8		INR	INR	615		1	1015 03B58	S		0	002	0,8/ 0,0
1,5		SCD	SCDC	485		0	1015 02B47			1	001	INDC00
1,5		INR	INR	435		1	1015 03B22	S		0	002	1,5/ 0,0
7,5		SCD	SCDC	435		0	1015 02B37			1	001	INDC000
7,5		MEM	MEM	075		1	1015 09A18	S		0	002	7,5/ 0,0
0,8		SCD	SCDC	235		0	1015 02A54			1	001	INDC001
2,0		INR	INR	200		1	1015 03A43	S		2	002	
2,8		ADF	ADF	060		2	1015 01A15			0	003	2,8/ 0,0
3,5		ADF	ADF	080		0	1015 01A19			1	001	INDC002
3,5		MEM	MEM	070		1	1015 09A17	S		0	002	3,5/ 0,0
5,0		SCD	SCDC	560		0	1015 02B62			1	001	INDC003
2,5		INR	INR	285		1	1015 03A60	S		2	002	
7,5		ADF	ADF	055		2	1015 01A14			0	003	7,5/ 0,0
6,5		ADF	ADF	505		0	1015 01B36			1	001	INDC004
6,5		MEM	MEM	085		1	1015 09A20	S		0	002	6,5/ 0,0
5,8		ADF	ADF	400		0	1015 01B15			1	001	INDC005
5,8		MEM	MEM	095		1	1015 09A22	S		0	002	5,8/ 0,0
6,5		ADF	ADF	615		0	1015 01B58			1	001	INDC006
6,5		INR	INR	165		1	1015 03A36	S		0	002	6,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
3,5		ADF	ADF	020	0	1015 01A07		1	001	INDC00A
3,5		MEM	MEM	140	1	1015 09A31	S	0	002	3,5/ 0,0
3,5		ADF	ADF	220	0	1015 01A47		1	001	INDC00B
3,5		MEM	MEM	155	1	1015 09A34	S	0	002	3,5/ 0,0
3,0		MEM	MEM	435	0	1015 09B24		1	001	INDC00X=
3,0		INR	INR	550	1	1015 03B45	S	0	002	3,0/ 0,0
5,0		ADF	ADF	635	0	1015 01B62		1	001	INDC011
5,0		INR	INR	295	1	1015 03A62	S	0	002	5,0/ 0,0
2,0		ADF	ADF	395	0	1015 01B14		1	001	INDC03=
2,0		INR	INR	330	1	1015 03A69	S	0	002	2,0/ 0,0
0,8		SCD	SCDC	455	0	1015 02B41		1	001	INDC04
0,8		INR	INR	585	1	1015 03B52	S	0	002	0,8/ 0,0
2,0		SCD	SCDC	590	0	1015 02B68		1	001	INDC05
2,0		INR	INR	465	1	1015 03B28	S	0	002	2,0/ 0,0
5,8		ADF	ADF	575	0	1015 01B50		1	001	INDC07=
5,8		INR	INR	175	1	1015 03A38	S	0	002	5,8/ 0,0
5,8		MEM	MEM	210	0	1015 09A45		1	001	INDC08=
5,8		INR	INR	595	1	1015 03B54	S	0	002	5,8/ 0,0
5,0		ADF	ADF	580	0	1015 01B51		1	001	INDC08A
5,0		INR	INR	270	1	1015 03A57	S	0	002	5,0/ 0,0
5,0		ADF	ADF	565	0	1015 01B48		1	001	INDC09
5,0		INR	INR	205	1	1015 03A44	S	0	002	5,0/ 0,0
0,0		INR	INR	375	0	1015 03B10	S	0	001	INDC09=
0,0		INR	INR	410	0	1015 03B17	S	0	001	INDC0A=

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
1,3		M=D	M=D	010		0	1015 04B33			1	001	INDC0B=
1,3		INR	INR	365		1	1015 03B08	S	0		002	1,3/ 0,0
0,8		M=D	M=D	015		0	1015 04B32			1	001	INDC0C=
0,8		INR	INR	490		1	1015 03B33	S	0		002	0,8/ 0,0
0,0		INR	INR	500		0	1015 03B35	S	0		001	INDC0F=
1,3		SCD	SCDC	510		0	1015 02B52			1	001	INDC10R2
1,3		INR	INR	470		1	1015 03B29	S	0		002	1,3/ 0,0
1,0		ADF	ADF	410		0	1015 01B17			1	001	INDC2=
1,0		INR	INR	480		1	1015 03B31	S	0		002	1,0/ 0,0
1,3		ADF	ADF	570		0	1015 01B49			1	001	INDCA0RB
1,3		INR	INR	485		1	1015 03B32	S	0		002	1,3/ 0,0
0,8		SCD	SCDC	515		0	1015 02B53			1	001	INDCBYTE
5,8		INR	INR	645		1	1015 03B64	S	2		002	
4,3		MEM	MEM	290		2	1015 09A61			1	003	
10,9		ADF	ADF	010		1	1015 01A05			0	004	10,9/ 0,0
2,5		SCD	SCDC	210		0	1015 02A48			1	001	INDCD10
2,5		INR	INR	340		1	1015 03B03	S	0		002	2,5/ 0,0
2,5		ADF	ADF	430		0	1015 01B21			1	001	INDCF
2,5		INR	INR	630		1	1015 03B61	S	0		002	2,5/ 0,0
3,0		SCD	SCDC	570		0	1015 02B64			1	001	INDC0PT
3,0		INR	INR	350		1	1015 03B05	S	0		002	3,0/ 0,0
5,8		SCD	SCDC	250		0	1015 02A59			1	001	INDCREAD
5,8		INR	INR	660		1	1015 03B67	S	0		002	5,8/ 0,0
2,5		SCD	SCDC	280		0	1015 02A67			1	001	INDCSHIFT
2,5		INR	INR	425		1	1015 03B20	S	0		002	2,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LC	WT	WSEQ	SIGNAL NAME
2,0		SCD	SCDC	290		0	1015 02B07			1	001	INDCST
2,0		INR	INR	565		1	1015 03B48	S	0		002	2,0/ 0,0
1,0		SCD	SCDC	415		0	1015 02B33			1	001	INDCXSKIP
1,0		INR	INR	400		1	1015 03B15	S	0		002	1,0/ 0,0
2,5		INR	INR	045		0	1015 03A12			1	001	INDCXX0=
2,5		MEM	MEM	055		1	1015 09A14	S	0		002	2,5/ 0,0
3,5		INR	INR	240		0	1015 03A51			1	001	INDCXX1=
3,5		MEM	MEM	045		1	1015 09A12	S	0		002	3,5/ 0,0
3,5		INR	INR	280		0	1015 03A59			1	001	INDCXX2=
3,5		MEM	MEM	040		1	1015 09A11	S	0		002	3,5/ 0,0
3,0		MEM	MEM	030		0	1015 09A09	S	1		001	INDCXX3=
1,3		INR	INR	190		1	1015 03A41		2		002	
4,3		ADF	ADF	305		2	1015 01A64		0		003	4,3/ 0,0
3,0		INR	INR	305		0	1015 03A64			1	001	INDCXX4=
3,0		MEM	MEM	115		1	1015 09A26	S	0		002	3,0/ 0,0
3,0		INR	INR	050		0	1015 03A13			1	001	INDCXX5=
3,0		MEM	MEM	125		1	1015 09A28	S	0		002	3,0/ 0,0
3,0		INR	INR	250		0	1015 03A53			1	001	INDCXX6=
3,0		MEM	MEM	110		1	1015 09A25	S	0		002	3,0/ 0,0
2,5		MEM	MEM	120		0	1015 09A27	S	1		001	INDCXX7=
5,8		INR	INR	215		1	1015 03A46		2		002	
8,3		ADF	ADF	640		2	1015 01B63		0		003	8,3/ 0,0
6,5		INR	INR	055		0	1015 03A14			1	001	INDCXX8=
6,5		MEM	MEM	465		1	1015 09B30	S	0		002	6,5/ 0,0
5,0		INR	INR	225		0	1015 03A48			1	001	INDCXX9=
5,0		MEM	MEM	500		1	1015 09B37	S	0		002	5,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
3,0		INR	INR	210		0	1015 03A45			1	001	INDCXXA=
3,0		MEM	MEM	135		1	1015 09A30	S	0		002	3,0/ 0,0
2,5		INR	INR	070		0	1015 03A17			1	001	INDCXXB=
2,5		MEM	MEM	130		1	1015 09A29	S	0		002	2,5/ 0,0
2,5		INR	INR	085		0	1015 03A20			1	001	INDCXXC=
2,5		MEM	MEM	180		1	1015 09A39	S	0		002	2,5/ 0,0
2,5		INR	INR	110		0	1015 03A25			1	001	INDCXXD=
2,5		MEM	MEM	190		1	1015 09A41	S	0		002	2,5/ 0,0
3,0		INR	INR	100		0	1015 03A23			1	001	INDCXXE=
3,0		MEM	MEM	195		1	1015 09A42	S	0		002	3,0/ 0,0
3,0		INR	INR	065		0	1015 03A16			1	001	INDCXXF=
3,0		MEM	MEM	205		1	1015 09A44	S	0		002	3,0/ 0,0
9,5		ADF	ADF	065		0	1015 01A16			1	001	INTRPT00=
4,3		PFS	PFS	245		1	1015 17A58	S	2		002	
13,8		TTY	TTY	250		2	1015 16B35	S	0		003	13,8/ 0,0
5,8		PI	PI	050		0	1015 15A17			1	001	INTRPT01=
5,8		TTY	TTY	245		1	1015 16B33	S	0		002	5,8/ 0,0
5,0		PI	PI	055		0	1015 15A29			1	001	INTRPT02=
5,0		TTY	TTY	240		1	1015 16B31	S	0		002	5,0/ 0,0
5,0		PI	PI	060		0	1015 15A25			1	001	INTRPT03=
5,0		TTY	TTY	235		1	1015 16B29	S	0		002	5,0/ 0,0
0,8		PI	PI	065		0	1015 15B39			1	001	INTRPT04=
0,8		TTY	TTY	230		1	1015 16B27	S	0		002	0,8/ 0,0
1,0		PI	PI	070		0	1015 15B43			1	001	INTRPT05=
1,0		TTY	TTY	225		1	1015 16B25	S	0		002	1,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
2,0		PI	PI	075		0	1015 15B55		1	001	INTRPT06=
2,0		TTY	TTY	220		1	1015 16B23	S	0	002	2,0/ 0,0
1,5		PI	PI	080		0	1015 15B51		1	001	INTRPT07=
3,0		TTY	TTY	215		1	1015 16B21	S	2	002	
4,5		PFS	PFS	250		2	1015 17A56	S	0	003	4,5/ 0,0
5,8		PI	PI	085		0	1015 15A11		1	001	INTRPT08=
5,8		TTY	TTY	210		1	1015 16B19	S	0	002	5,8/ 0,0
5,0		PI	PI	090		0	1015 15A15		1	001	INTRPT09=
5,0		TTY	TTY	205		1	1015 16B17	S	0	002	5,0/ 0,0
4,3		PI	PI	045		0	1015 15A27		1	001	INTRPT10=
4,3		TTY	TTY	200		1	1015 16B15	S	0	002	4,3/ 0,0
4,3		PI	PI	015		0	1015 15A23		1	001	INTRPT11=
4,3		TTY	TTY	195		1	1015 16B13	S	0	002	4,3/ 0,0
1,3		PI	PI	025		0	1015 15B37		1	001	INTRPT12=
1,3		TTY	TTY	190		1	1015 16B11	S	0	002	1,3/ 0,0
2,0		PI	PI	030		0	1015 15B41		1	001	INTRPT13=
2,0		TTY	TTY	185		1	1015 16B09	S	0	002	2,0/ 0,0
2,5		PI	PI	035		0	1015 15B53		1	001	INTRPT14=
2,5		TTY	TTY	180		1	1015 16B07	S	0	002	2,5/ 0,0
2,5		PI	PI	040		0	1015 15B49		1	001	INTRPT15=
2,5		TTY	TTY	175		1	1015 16B05	S	2	002	
5,0		PFS	PFS	255		2	1015 17A54	S	0	003	5,0/ 0,0
8,5		ADF	ADF	145		0	1015 01A32		1	001	IT15A01=
8,5		PI	PI	100		1	1015 15A05	S	0	002	8,5/ 0,0
8,5		PI	PI	095		0	1015 15A49		1	001	ITACT=
8,5		ADF	ADF	255		1	1015 01A54	S	0	002	8,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LO WT	WSEQ	SIGNAL NAME
8,5		PI	PI	105	0	1015 15A51		1	001	ITDSB
8,5		ADF	ADF	250	1	1015 01A53	S	0	002	8,5/ 0,0
9,5		PI	PI	110	0	1015 15B19		1	001	ITENB
9,5		ADF	ADF	070	1	1015 01A17	S	0	002	9,5/ 0,0
0,0		ADF	ADF	135	0	1015 01A30		0	001	ITFINHR2=
9,5		PI	PI	115	0	1015 15B17		1	001	ITIDL
9,5		ADF	ADF	050	1	1015 01A13	S	0	002	9,5/ 0,0
8,5		SCD	SCDC	130	0	1015 02A31		1	001	ITRSV10=
8,5		PI	PI	120	1	1015 15A55	S	0	002	8,5/ 0,0
8,5		SCD	SCDC	125	0	1015 02A29		1	001	ITRSV11=
8,5		PI	PI	125	1	1015 15A59	S	0	002	8,5/ 0,0
9,5		SCD	SCDC	120	0	1015 02A27		1	001	ITRSV12=
9,5		PI	PI	130	1	1015 15B15	S	0	002	9,5/ 0,0
9,5		SCD	SCDC	050	0	1015 02A13		1	001	ITRSV13=
9,5		PI	PI	135	1	1015 15B13	S	0	002	9,5/ 0,0
8,5		PI	PI	140	0	1015 15A45		1	001	ITSVENB
8,5		ADF	ADF	075	1	1015 01A18	S	0	002	8,5/ 0,0
8,5		ADF	ADF	260	0	1015 01A55		1	001	ITWAIT=
8,5		PI	PI	145	1	1015 15B05	S	0	002	8,5/ 0,0
1,0		ADF	ADF	485	0	1015 01B32		1	001	IXOOMB=
1,0		M=D	M=D	560	1	1015 04B37	S	0	002	1,0/ 0,0
1,5		ADF	ADF	440	0	1015 01B23		1	001	IXCLKENB1=
1,5		M=D	M=D	545	1	1015 04B34	S	0	002	1,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
0,5		ARI	ARI0	150	0	1015 05A33		1	001	IXCLKENBL
0,5		ARI	ARI0	165	1	1015 05A36		2	002	
6,5		ARI	ARI4	170	2	1015 06A36		1	003	
7,5		ADF	ADF	620	1	1015 01B59	S	0	004	7,5/ 0,0
6,5		ADF	ADF	610	0	1015 01B57	S	1	001	IXCLKENBR
0,5		ARI	ARI4	155	1	1015 06A33		2	002	
0,5		ARI	ARI8	150	2	1015 07A33		1	003	
0,5		ARI	ARI8	165	1	1015 07A36		2	004	
0,5		ARI	ARI1	150	2	1015 08A33		1	005	
8,5		ARI	ARI1	165	1	1015 08A36		0	006	8,5/ 0,0
5,0		ADF	ADF	420	0	1015 01B19		1	001	IXLDAD3=
1,0		M=D	M=D	565	1	1015 04A24	S	2	002	
6,0		INR	INR	015	2	1015 03A06	S	0	003	6,0/ 0,0
0,5		ARI	ARI4	250	0	1015 06A52		1	001	IXLDADL
5,8		ARI	ARI0	245	1	1015 05A52		2	002	
6,3		ADF	ADF	650	2	1015 01B65	S	0	003	6,3/ 0,0
0,5		ARI	ARI1	245	0	1015 08A52		1	001	IXLDADR
5,0		ARI	ARI8	245	1	1015 07A52		2	002	
5,5		ADF	ADF	475	2	1015 01B30	S	0	003	5,5/ 0,0
1,5		ADF	ADF	315	0	1015 01A66	S	1	001	IXLDPC
0,5		ARI	ARI0	310	1	1015 05A65		2	002	
0,5		ARI	ARI4	315	2	1015 06A65		1	003	
0,5		ARI	ARI8	310	1	1015 07A65		2	004	
3,0		ARI	ARI1	310	2	1015 08A65		0	005	3,0/ 0,0
0,8		ARI	ARI0	195	0	1015 05A42	S	1	001	IXR00=
1,0		M=D	M=D	060	1	1015 04A37		2	002	
1,8		INR	INR	095	2	1015 03A22		0	003	1,8/ 0,0
1,0		ARI	ARI0	205	0	1015 05A44	S	1	001	IXR00S
1,0		M=D	M=D	555	1	1015 04A59	S	0	002	1,0/ 0,0
0,5		M=D	M=D	225	0	1015 04A40		1	001	IXR01=
0,5		ARI	ARI0	220	1	1015 05A47	S	0	002	0,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
0,8		ARI	ARI0	235		0	1015 05A50	S	1		001	!XR01S
0,8		M=D	M=D	575		1	1015 04A55	S	0		002	0,8/ 0,0
1,3		M=D	M=D	230		0	1015 04A28		1		001	!XR02=
1,3		ARI	ARI0	250		1	1015 05A53	S	0		002	1,3/ 0,0
0,5		ARI	ARI0	260		0	1015 05A55	S	1		001	!XR02S
0,5		M=D	M=D	580		1	1015 04A62	S	0		002	0,5/ 0,0
1,3		ARI	ARI0	290		0	1015 05A61	S	1		001	!XR03=
1,0		ARI	ARI4	175		1	1015 06A37		2		002	
2,3		M=D	M=D	235		2	1015 04A25		0		003	2,3/ 0,0
2,5		ARI	ARI0	230		0	1015 05A49	S	1		001	!XR03S
2,5		M=D	M=D	585		1	1015 04B05	S	0		002	2,5/ 0,0
1,3		ARI	ARI0	300		0	1015 05A63		1		001	!XR04=
1,5		ARI	ARI4	200		1	1015 06A42	S	2		002	
2,8		M=D	M=D	240		2	1015 04A17		0		003	2,8/ 0,0
3,5		ARI	ARI4	210		0	1015 06A44	S	1		001	!XR04S
3,5		M=D	M=D	590		1	1015 04B12	S	0		002	3,5/ 0,0
1,5		M=D	M=D	245		0	1015 04A20		1		001	!XR05=
1,5		ARI	ARI4	225		1	1015 06A47	S	0		002	1,5/ 0,0
3,0		ARI	ARI4	240		0	1015 06A50	S	1		001	!XR05S
3,0		M=D	M=D	595		1	1015 04B06	S	0		002	3,0/ 0,0
2,5		M=D	M=D	250		0	1015 04A05		1		001	!XR06=
2,5		ARI	ARI4	255		1	1015 06A53	S	0		002	2,5/ 0,0
3,0		ARI	ARI4	265		0	1015 06A55	S	1		001	!XR06S
3,0		M=D	M=D	600		1	1015 04B11	S	0		002	3,0/ 0,0
1,3		ARI	ARI4	295		0	1015 06A61	S	1		001	!XR07=
2,0		ARI	ARI8	170		1	1015 07A37		2		002	
3,3		M=D	M=D	255		2	1015 04A09		0		003	3,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LO	WT	WSEQ	SIGNAL NAME
3,5		ARI	ARI4	235		0	1015 06A49	S	1		001	IXR07S
3,5		M=D	M=D	605		1	1015 04B22	S	0		002	3,5/ 0,0
1,3		ARI	ARI4	305		0	1015 06A63			1	001	IXR08=
1,3		ARI	ARI8	195		1	1015 07A42	S	2		002	
2,6		M=D	M=D	260		2	1015 04A36			0	003	2,6/ 0,0
4,3		ARI	ARI8	205		0	1015 07A44	S	1		001	IXR08S
4,3		M=D	M=D	610		1	1015 04B28	S	0		002	4,3/ 0,0
1,5		M=D	M=D	265		0	1015 04A31			1	001	IXR09=
1,5		ARI	ARI8	220		1	1015 07A47	S	0		002	1,5/ 0,0
4,3		ARI	ARI8	235		0	1015 07A50	S	1		001	IXR09S
4,3		M=D	M=D	615		1	1015 04B26	S	0		002	4,3/ 0,0
1,5		M=D	M=D	270		0	1015 04A30			1	001	IXR10=
1,5		ARI	ARI8	250		1	1015 07A53	S	0		002	1,5/ 0,0
4,3		ARI	ARI8	260		0	1015 07A55	S	1		001	IXR10S
4,3		M=D	M=D	620		1	1015 04B31	S	0		002	4,3/ 0,0
1,3		ARI	ARI1	170		0	1015 08A37			1	001	IXR11=
2,0		ARI	ARI8	290		1	1015 07A61	S	2		002	
3,3		M=D	M=D	275		2	1015 04A29			0	003	3,3/ 0,0
5,0		ARI	ARI8	230		0	1015 07A49	S	1		001	IXR11S
5,0		M=D	M=D	625		1	1015 04B39	S	0		002	5,0/ 0,0
1,3		ARI	ARI8	300		0	1015 07A63			1	001	IXR12=
2,5		ARI	ARI1	195		1	1015 08A42	S	2		002	
3,8		M=D	M=D	280		2	1015 04A15			0	003	3,8/ 0,0
5,8		ARI	ARI1	205		0	1015 08A44	S	1		001	IXR12S
5,8		M=D	M=D	320		1	1015 04B45	S	0		002	5,8/ 0,0
2,5		M=D	M=D	285		0	1015 04A11			1	001	IXR13=
2,5		ARI	ARI1	220		1	1015 08A47	S	0		002	2,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
5,0		ARI	ARI1	235		0	1015 08A50	S	1		001	IXR13S
5,0		M=D	M=D	325		1	1015 04B43	S	0		002	5,0/ 0,0
2,5		M=D	M=D	290		0	1015 04A14			1	001	IXR14=
2,5		ARI	ARI1	250		1	1015 08A53	S	0		002	2,5/ 0,0
4,3		ARI	ARI1	260		0	1015 08A55	S	1		001	IXR14S
4,3		M=D	M=D	330		1	1015 04B42	S	0		002	4,3/ 0,0
4,3		ARI	ARI0	340		0	1015 05B45			1	001	IXR15=
2,0		ARI	ARI1	290		1	1015 08A61	S	2		002	
2,0		M=D	M=D	295		2	1015 04A34			1	003	
8,3		MEM	MEM	090		1	1015 09A21			0	004	8,3/ 0,0
5,0		ARI	ARI1	230		0	1015 08A49	S	1		001	IXR15S
2,0		ADF	ADF	525		1	1015 01B40	S	2		002	
7,0		M=D	M=D	470		2	1015 04B64	S	0		003	7,0/ 0,0
6,5		M=D	M=D	505		0	1015 04B65	S	1		001	IXRDR=
1,0		SCD	SCDC	145		1	1015 02A34	S	2		002	
0,5		ARI	ARI0	160		2	1015 05A35			1	003	
0,5		ARI	ARI4	165		1	1015 06A35			2	004	
0,5		ARI	ARI8	160		2	1015 07A35			1	005	
9,0		ARI	ARI1	160		1	1015 08A35			0	006	9,0/ 0,0
5,8		ADF	ADF	630		0	1015 01B61	S	1		001	IXSL
0,5		ARI	ARI0	240		1	1015 05A51			2	002	
0,5		ARI	ARI4	245		2	1015 06A51			1	003	
0,5		ARI	ARI8	240		1	1015 07A51			2	004	
7,3		ARI	ARI1	240		2	1015 08A51			0	005	7,3/ 0,0
5,0		ADF	ADF	495		0	1015 01B34			1	001	IXSLOPT=
5,0		M=D	M=D	520		1	1015 04A43	S	0		002	5,0/ 0,0
3,0		ARI	ARI1	300		0	1015 08A63			1	001	IXSLZRO
3,0		ADF	ADF	285		1	1015 01A60	S	0		002	3,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
3,0		ADF	ADF	370		0	1015 01B09	S	1	001	IXSR
0,5		ARI	ARI0	265		1	1015 05A56		2	002	
0,5		ARI	ARI4	270		2	1015 06A56		1	003	
0,5		ARI	ARI8	265		1	1015 07A56		2	004	
4,5		ARI	ARI1	265		2	1015 08A56		0	005	4,5/ 0,0
4,3		ARI	ARI0	170		0	1015 05A37		1	001	IXSRAC15
4,3		ADF	ADF	390		1	1015 01B13	S	0	002	4,3/ 0,0
3,0		ADF	ADF	380		0	1015 01B11		1	001	IXSROPT-
3,0		M-D	M-D	550		1	1015 04A53	S	0	002	3,0/ 0,0
5,8		TTY	TTY	270		0	1015 16B43		1	001	KEXT1-
5,8		MEM	MEM	580		1	1015 09B53	S	0	002	5,8/ 0,0
7,5		ARI	ARI0	025		0	1015 05A08		1	001	KK1
7,5		MEM	MEM	640		1	1015 09B58	S	0	002	7,5/ 0,0
7,5		ARI	ARI4	030		0	1015 06A08		2	001	KK1A
7,5		MEM	MEM	645		2	1015 09B58	S	0	002	7,5/ 0,0
7,5		ARI	ARI8	025		0	1015 07A08		3	001	KK1B
7,5		MEM	MEM	650		3	1015 09B58	S	0	002	7,5/ 0,0
7,5		ARI	ARI1	025		0	1015 08A08		2	001	KK2
7,5		MEM	MEM	615		2	1015 09B56	S	0	002	7,5/ 0,0
5,8		SCD	SCDC	270		0	1015 02A69		1	001	KK2A
5,8		MEM	MEM	620		1	1015 09B56	S	0	002	5,8/ 0,0
2,5		M-D	M-D	070		0	1015 04A70		3	001	KK2B
2,5		MEM	MEM	610		3	1015 09B56	S	0	002	2,5/ 0,0
3,5		INR	INR	420		0	1015 03B19		2	001	KK3
3,5		MEM	MEM	585		2	1015 09B54	S	0	002	3,5/ 0,0
3,5		ADF	ADF	590		0	1015 01B53		1	001	KK3A
3,5		MEM	MEM	590		1	1015 09B54	S	0	002	3,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EC	LI	LOCATION	S	LC	WT	WSEQ	SIGNAL NAME
7,5		ARI	ARI0	105		0	1015 05A24			1	001	KKA
7,5		MEM	MEM	595		1	1015 09B55	S	0		002	7,5/ 0,0
6,5		ARI	ARI4	110		0	1015 06A24			2	001	KKA1
6,5		MEM	MEM	600		2	1015 09B55	S	0		002	6,5/ 0,0
6,5		ARI	ARI8	105		0	1015 07A24			3	001	KKA2
6,5		MEM	MEM	605		3	1015 09B55	S	0		002	6,5/ 0,0
7,5		ARI	ARI1	105		0	1015 08A24			2	001	KKB
7,5		MEM	MEM	625		2	1015 09B57	S	0		002	7,5/ 0,0
3,5		SCD	SCDC	330		0	1015 02B15			3	001	KKB1
3,5		MEM	MEM	630		3	1015 09B57	S	0		002	3,5/ 0,0
8,5		ADF	ADF	030		0	1015 01A09			1	001	KKB2
8,5		MEM	MEM	635		1	1015 09B57	S	0		002	8,5/ 0,0
8,5		DAM	DAM	020		0	1015 14A11			1	001	KKC
8,5		MEM	MEM	655		1	1015 09B59	S	0		002	8,5/ 0,0
7,5		PI	PI	020		0	1015 15A53			2	001	KKC1
7,5		MEM	MEM	660		2	1015 09B59	S	0		002	7,5/ 0,0
0,5		ARI	ARI0	090		0	1015 05A21			1	001	MACLKEN
0,5		ARI	ARI4	095		1	1015 06A21			2	002	
0,5		ARI	ARI8	090		2	1015 07A21			1	003	
5,0		ARI	ARI1	090		1	1015 08A21			2	004	
3,5		SCD	SCDC	320		2	1015 02B13	S		1	005	
10,0		MEM	MEM	570		1	1015 09B51			0	006	10,0/ 0,0
7,5		SCD	SCDC	565		0	1015 02B63	S		1	001	MALDAD
0,5		ARI	ARI0	070		1	1015 05A17			2	002	
0,5		ARI	ARI4	075		2	1015 06A17			1	003	
0,5		ARI	ARI8	070		1	1015 07A17			2	004	
9,0		ARI	ARI1	070		2	1015 08A17			0	005	9,0/ 0,0
5,8		M=D	M=D	500		0	1015 04A60	S		1	001	MALDAD=
5,8		SCD	SCDC	575		1	1015 02B65	S		0	002	5,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EC	LI	LOCATION	S	LC	WT	WSEQ	SIGNAL NAME
0,5		ARI	ARIO	125		0	1015 05A28		1		001	MALDADSR
0,5		ARI	ARI4	130		1	1015 06A28		2		002	
0,5		ARI	ARI8	125		2	1015 07A28		1		003	
7,5		ARI	ARI1	125		1	1015 08A28		2		004	
9,0		SCD	SCDC	555		2	1015 02B61	S	0		005	9,0/ 0,0
0,0		SCD	SCDC	535		0	1015 02B57	S	0		001	MALDADSR=
6,5		SCD	SCDC	480		0	1015 02B46	S	1		001	MALDPC
0,5		ARI	ARIO	065		1	1015 05A16		2		002	
0,5		ARI	ARI4	070		2	1015 06A16		1		003	
0,5		ARI	ARI8	065		1	1015 07A16		2		004	
8,0		ARI	ARI1	065		2	1015 08A16		0		005	8,0/ 0,0
3,0		SCD	SCDC	325		0	1015 02B14		1		001	MALDPC1
3,0		MEM	MEM	460		1	1015 09B29	S	0		002	3,0/ 0,0
0,0		MEM	MEM	490		0	1015 09B35		0		001	MALDPC2=
0,0		ARI	ARIO	040		0	1015 05A11	S	0		001	MAR00
0,0		ARI	ARIO	050		0	1015 05A13	S	0		001	MAR01
7,5		ARI	ARIO	060		0	1015 05A15	S	1		001	MAR01S
4,3		MEM	MEM	575		1	1015 09B52		2		002	
11,8		DAM	DAM	310		2	1015 14B49	S	0		003	11,8/ 0,0
0,0		ARI	ARIO	120		0	1015 05A27	S	0		001	MAR02
7,5		ARI	ARIO	110		0	1015 05A25	S	1		001	MAR02S
4,3		MEM	MEM	690		1	1015 09B65		2		002	
11,8		DAM	DAM	335		2	1015 14B57	S	0		003	11,8/ 0,0
0,0		ARI	ARIO	155		0	1015 05A34	S	0		001	MAR03
7,5		ARI	ARIO	130		0	1015 05A29	S	1		001	MAR03S
5,0		MEM	MEM	700		1	1015 09B67		2		002	
12,5		DAM	DAM	340		2	1015 14B58	S	0		003	12,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
6,5		ARI	ARI4	045	0	1015 06A11	S	1	001	MAR04
1,0		MAG	MAG0	205	1	1015 10B35		2	002	
1,0		MAG	MAG1	200	2	1015 11B35		1	003	
1,0		MAG	MAG2	200	1	1015 12B35		2	004	
9,5		MAG	MAG3	200	2	1015 13B35		0	005	9,5/ 0,0
8,5		DAM	DAM	305	0	1015 14B47	S	1	001	MAR04S
8,5		ARI	ARI4	060	1	1015 06A14	S	0	002	8,5/ 0,0
6,5		ARI	ARI4	055	0	1015 06A13	S	1	001	MAR05
1,0		MAG	MAG0	210	1	1015 10B37		2	002	
1,0		MAG	MAG1	205	2	1015 11B37		1	003	
1,0		MAG	MAG2	205	1	1015 12B37		2	004	
9,5		MAG	MAG3	205	2	1015 13B37		0	005	9,5/ 0,0
8,5		DAM	DAM	295	0	1015 14B45	S	1	001	MAR05S
8,5		ARI	ARI4	065	1	1015 06A15	S	0	002	8,5/ 0,0
5,8		ARI	ARI4	125	0	1015 06A27	S	1	001	MAR06
1,0		MAG	MAG0	215	1	1015 10B39		2	002	
1,0		MAG	MAG1	210	2	1015 11B39		1	003	
1,0		MAG	MAG2	210	1	1015 12B39		2	004	
8,8		MAG	MAG3	210	2	1015 13B39		0	005	8,8/ 0,0
9,5		DAM	DAM	350	0	1015 14B61	S	1	001	MAR06S
9,5		ARI	ARI4	115	1	1015 06A25	S	0	002	9,5/ 0,0
2,5		ARI	ARI4	160	0	1015 06A34	S	1	001	MAR07
1,0		MAG	MAG0	220	1	1015 10A12		2	002	
1,0		MAG	MAG1	215	2	1015 11A12		1	003	
1,0		MAG	MAG2	215	1	1015 12A12		2	004	
5,5		MAG	MAG3	215	2	1015 13A12		0	005	5,5/ 0,0
8,5		DAM	DAM	345	0	1015 14B59	S	1	001	MAR07S
8,5		ARI	ARI4	135	1	1015 06A29	S	0	002	8,5/ 0,0
2,0		ARI	ARI8	040	0	1015 07A11	S	1	001	MAR08
1,0		MAG	MAG0	225	1	1015 10A16		2	002	
1,0		MAG	MAG1	220	2	1015 11A16		1	003	
1,0		MAG	MAG2	220	1	1015 12A16		2	004	
5,0		MAG	MAG3	220	2	1015 13A16		0	005	5,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LO WT	WSEQ	SIGNAL NAME
8,5		DAM	DAM	300		0	1015 14B46	S	1	001	MAR08S
8,5		ARI	ARI8	055		1	1015 07A14	S	0	002	8,5/ 0,0
2,0		ARI	ARI8	050		0	1015 07A13	S	1	001	MAR09
1,0		MAG	MAG0	230		1	1015 10A20		2	002	
1,0		MAG	MAG1	225		2	1015 11A20		1	003	
1,0		MAG	MAG2	225		1	1015 12A20		2	004	
5,0		MAG	MAG3	225		2	1015 13A20		0	005	5,0/ 0,0
8,5		DAM	DAM	290		0	1015 14B43	S	1	001	MAR09S
8,5		ARI	ARI8	060		1	1015 07A15	S	0	002	8,5/ 0,0
7,5		ARI	ARI8	120		0	1015 07A27	S	1	001	MAR10
1,0		MAG	MAG0	235		1	1015 10B67		2	002	
1,0		MAG	MAG1	230		2	1015 11B67		1	003	
1,0		MAG	MAG2	230		1	1015 12B67		2	004	
10,5		MAG	MAG3	230		2	1015 13B67		0	005	10,5/ 0,0
8,5		DAM	DAM	355		0	1015 14B63	S	1	001	MAR10S
2,0		ARI	ARI8	110		1	1015 07A25	S	2	002	
10,5		SCD	SCDC	065		2	1015 02A16	S	0	003	10,5/ 0,0
7,5		ARI	ARI8	155		0	1015 07A34	S	1	001	MAR11
1,0		MAG	MAG0	240		1	1015 10B65		2	002	
1,0		MAG	MAG1	235		2	1015 11B65		1	003	
1,0		MAG	MAG2	235		1	1015 12B65		2	004	
10,5		MAG	MAG3	235		2	1015 13B65		0	005	10,5/ 0,0
8,5		DAM	DAM	360		0	1015 14B64	S	1	001	MAR11S
2,0		ARI	ARI8	130		1	1015 07A29	S	2	002	
10,5		SCD	SCDC	095		2	1015 02A22	S	0	003	10,5/ 0,0
7,5		ARI	ARI1	040		0	1015 08A11	S	1	001	MAR12
1,0		MAG	MAG0	245		1	1015 10B63		2	002	
2,0		MAG	MAG1	240		2	1015 11B63		1	003	
1,5		MAG	MAG2	240		1	1015 12B63		2	004	
12,0		MAG	MAG3	240		2	1015 13B63		0	005	12,0/ 0,0
8,5		DAM	DAM	285		0	1015 14B41	S	1	001	MAR12S
3,0		ARI	ARI1	055		1	1015 08A14	S	2	002	
11,5		SCD	SCDC	090		2	1015 02A21	S	0	003	11,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
1,5		ARI	ARI1	050	0	1015	08A13	S	1	001	MAR13
1,0		MAG	MAG0	250	1	1015	10A30		2	002	
1,0		MAG	MAG1	245	2	1015	11A30		1	003	
1,0		MAG	MAG2	245	1	1015	12A30		2	004	
4,5		MAG	MAG3	245	2	1015	13A30		0	005	4,5/ 0,0
8,5		DAM	DAM	275	0	1015	14B39	S	1	001	MAR13S
2,5		ARI	ARI1	060	1	1015	08A15	S	2	002	
11,0		SCD	SCDC	080	2	1015	02A19	S	0	003	11,0/ 0,0
1,3		ARI	ARI1	120	0	1015	08A27	S	1	001	MAR14
1,0		MAG	MAG0	255	1	1015	10A26		2	002	
1,0		MAG	MAG1	250	2	1015	11A26		1	003	
1,0		MAG	MAG2	250	1	1015	12A26		2	004	
4,3		MAG	MAG3	250	2	1015	13A26		0	005	4,3/ 0,0
8,5		DAM	DAM	370	0	1015	14B67	S	1	001	MAR14S
2,5		ARI	ARI1	110	1	1015	08A25	S	2	002	
11,0		SCD	SCDC	070	2	1015	02A17	S	0	003	11,0/ 0,0
1,3		ARI	ARI1	155	0	1015	08A34	S	1	001	MAR15
1,0		MAG	MAG0	260	1	1015	10A24		2	002	
1,0		MAG	MAG1	255	2	1015	11A24		1	003	
1,0		MAG	MAG2	255	1	1015	12A24		2	004	
4,3		MAG	MAG3	255	2	1015	13A24		0	005	4,3/ 0,0
8,5		DAM	DAM	365	0	1015	14B65	S	1	001	MAR15S
2,5		ARI	ARI1	130	1	1015	08A29	S	2	002	
11,0		SCD	SCDC	060	2	1015	02A15	S	0	003	11,0/ 0,0
0,5		ARI	ARI0	115	0	1015	05A26		1	001	MARDRL=
0,5		ARI	ARI0	145	1	1015	05A32		2	002	
0,5		ARI	ARI4	150	2	1015	06A32		1	003	
0,5		ARI	ARI4	120	1	1015	06A26		2	004	
5,8		ARI	ARI8	115	2	1015	07A26		1	005	
7,8		MEM	MEM	535	1	1015	09B44	S	0	006	7,8/ 0,0
0,5		ARI	ARI0	035	0	1015	05A10		1	001	MBLDADLB
5,0		ARI	ARI4	040	1	1015	06A10		2	002	
5,0		MEM	MEM	380	2	1015	09B12	S	1	003	
10,5		DAM	DAM	325	1	1015	14B53		0	004	10,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	SO	LI	LOCATION	S	LS	WT	WSEQ	SIGNAL NAME
2,0		M=D	M=D	515		0	1015 04B15	S	1		001	MBLDADLB0=
5,8		MEM	MEM	390		1	1015 09B15		2		002	
7,8		PFS	PFS	140		2	1015 17B15	S	0		003	7,8/ 0,0
0,5		ARI	ARI8	035		0	1015 07A10		1		001	MBLDADRB
5,0		ARI	ARI1	035		1	1015 08A10		2		002	
4,3		MEM	MEM	370		2	1015 09B10	S	1		003	
9,8		DAM	DAM	185		1	1015 14B14		0		004	9,8/ 0,0
2,0		M=D	M=D	510		0	1015 04B17	S	1		001	MBLDADRB0=
5,8		MEM	MEM	385		1	1015 09B13		2		002	
7,8		PFS	PFS	145		2	1015 17B16	S	0		003	7,8/ 0,0
1,0		MEM	MEM	160		0	1015 09A35	S	1		001	MBLDMCLB
0,5		ARI	ARI4	190		1	1015 06A40		2		002	
1,5		ARI	ARI0	185		2	1015 05A40		0		003	1,5/ 0,0
0,5		MEM	MEM	150		0	1015 09A33	S	1		001	MBLDMCRB
0,5		ARI	ARI1	185		1	1015 08A40		2		002	
1,0		ARI	ARI8	185		2	1015 07A40		0		003	1,0/ 0,0
1,0		INR	INR	665		0	1015 03B68		1		001	MBR00=
2,0		M=D	M=D	080		1	1015 04B48		2		002	
2,5		ARI	ARI8	380		2	1015 07B11		1		003	
3,5		ADF	ADF	345		1	1015 01B04		2		004	
9,0		ARI	ARI0	180		2	1015 05A39	S	0		005	9,0/ 0,0
1,3		ARI	ARI8	370		0	1015 07B09		1		001	MBR00D
1,3		M=D	M=D	085		1	1015 04B19		2		002	
2,6		ADF	ADF	355		2	1015 01B06	S	0		003	2,6/ 0,0
1,0		ARI	ARI8	385		0	1015 07B12		1		001	MBR01
1,0		ARI	ARI0	400		1	1015 05B17	S	0		002	1,0/ 0,0
3,0		ARI	ARI0	255		0	1015 05A54	S	1		001	MBR01=
2,5		ARI	ARI8	375		1	1015 07B10		2		002	
5,5		INR	INR	575		2	1015 03B50		0		003	5,5/ 0,0
5,0		ARI	ARI8	460		0	1015 07B27		1		001	MBR02
5,0		ARI	ARI0	135		1	1015 05A30	S	0		002	5,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
3,5		ARI	ARI0	275		0	1015 05A58	S	1		001	MBR02=
2,0		ARI	ARI8	480		1	1015 07B31		2		002	
5,5		INR	INR	560		2	1015 03B47		0		003	5,5/ 0,0
3,0		ARI	ARI8	475		0	1015 07B30		1		001	MBR03
3,0		ARI	ARI0	330		1	1015 05A69	S	0		002	3,0/ 0,0
3,0		ARI	ARI0	315		0	1015 05A66	S	1		001	MBR03=
2,0		ARI	ARI8	465		1	1015 07B28		2		002	
5,0		INR	INR	495		2	1015 03B34		0		003	5,0/ 0,0
3,5		ARI	ARI4	185		0	1015 06A39	S	1		001	MBR04=
3,0		ARI	ARI1	380		1	1015 08B11		2		002	
6,5		INR	INR	635		2	1015 03B62		0		003	6,5/ 0,0
2,0		ARI	ARI1	370		0	1015 08B09		1		001	MBR04B
2,0		INR	INR	385		1	1015 03B12	S	0		002	2,0/ 0,0
1,0		ARI	ARI1	385		0	1015 08B12		1		001	MBR05
1,0		ARI	ARI4	415		1	1015 06B17	S	0		002	1,0/ 0,0
3,0		ADF	ADF	460		0	1015 01B27		1		001	MBR05=
1,5		INR	INR	320		1	1015 03A67		2		002	
3,0		ARI	ARI4	260		2	1015 06A54	S	1		003	
7,5		ARI	ARI1	375		1	1015 08B10		0		004	7,5/ 0,0
5,0		ARI	ARI1	455		0	1015 08B27		1		001	MBR06
5,0		ARI	ARI4	140		1	1015 06A30	S	0		002	5,0/ 0,0
1,0		ADF	ADF	470		0	1015 01B29		1		001	MBR06=
2,0		INR	INR	515		1	1015 03B38		2		002	
3,5		ARI	ARI1	475		2	1015 08B31		1		003	
6,5		ARI	ARI4	280		1	1015 06A58	S	0		004	6,5/ 0,0
3,0		ARI	ARI1	470		0	1015 08B30		1		001	MBR07
3,0		ARI	ARI4	335		1	1015 06A69	S	0		002	3,0/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EG	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
2,0		ADF	ADF	550		0	1015 01B45		1	001	MBR07=
2,0		INR	INR	415		1	1015 03B18		2	002	
3,0		ARI	ARI1	460		2	1015 08B28		1	003	
7,0		ARI	ARI4	320		1	1015 06A66	S	0	004	7,0/ 0,0
1,5		ADF	ADF	535		0	1015 01B42		1	001	MBR08=
5,8		M=D	M=D	035		1	1015 04B58		2	002	
1,0		MEM	MEM	200		2	1015 09A43		1	003	
2,0		ARI	ARI8	180		1	1015 07A39	S	2	004	
10,3		INR	INR	080		2	1015 03A19		0	005	10,3/ 0,0
0,0		ARI	ARI8	410		0	1015 07B17	S	0	001	MBR09
1,0		MEM	MEM	215		0	1015 09A46		1	001	MBR09=
1,0		ARI	ARI8	255		1	1015 07A54	S	0	002	1,0/ 0,0
0,0		ARI	ARI8	135		0	1015 07A30	S	0	001	MBR10
4,3		ADF	ADF	600		0	1015 01B55		1	001	MBR10=
2,0		INR	INR	325		1	1015 03A68		2	002	
3,0		ARI	ARI8	275		2	1015 07A58	S	1	003	
9,3		MEM	MEM	010		1	1015 09A05		0	004	9,3/ 0,0
0,0		ARI	ARI8	330		0	1015 07A69	S	0	001	MBR11
5,0		ADF	ADF	540		0	1015 01B43		1	001	MBR11=
2,0		INR	INR	230		1	1015 03A49		2	002	
3,0		ARI	ARI8	315		2	1015 07A66	S	1	003	
10,0		MEM	MEM	020		1	1015 09A07		0	004	10,0/ 0,0
3,0		ADF	ADF	095		0	1015 01A22		1	001	MBR12=
5,0		ARI	ARI1	180		1	1015 08A39	S	2	002	
6,5		MEM	MEM	505		2	1015 09B38		1	003	
14,5		PI	PI	150		1	1015 15A43		0	004	14,5/ 0,0
0,0		ARI	ARI1	405		0	1015 08B17	S	0	001	MBR13

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
3,0		ADF	ADF	180		0	1015 01A39			1	001	MBR13=
4,3		ARI	ARI1	255		1	1015 08A54	S		2	002	
5,0		MEM	MEM	515		2	1015 09B40			1	003	
12,3		PI	PI	155		1	1015 15B03			0	004	12,3/ 0,0
0,0		ARI	ARI1	135		0	1015 08A30	S		0	001	MBR14
3,5		ADF	ADF	190		0	1015 01A41			1	001	MBR14=
4,3		ARI	ARI1	275		1	1015 08A58	S		2	002	
6,5		MEM	MEM	520		2	1015 09B41			1	003	
14,3		PI	PI	160		1	1015 15A67			0	004	14,3/ 0,0
0,0		ARI	ARI1	330		0	1015 08A69	S		0	001	MBR15
3,5		ADF	ADF	140		0	1015 01A31			1	001	MBR15=
3,5		ARI	ARI1	315		1	1015 08A66	S		2	002	
5,8		MEM	MEM	495		2	1015 09B36			1	003	
12,8		PI	PI	165		1	1015 15A69			0	004	12,8/ 0,0
2,0		SCD	SCDC	035		0	1015 02A10	S		1	001	MBRDR=
0,5		ARI	ARI0	175		1	1015 05A38			2	002	
0,5		ARI	ARI4	180		2	1015 06A38			1	003	
0,5		ARI	ARI8	175		1	1015 07A38			2	004	
3,5		ARI	ARI1	175		2	1015 08A38			1	005	
7,0		MEM	MEM	350		1	1015 09B05	S		0	006	7,0/ 0,0
5,0		ARI	ARI0	305		0	1015 05A64	S		1	001	MCDI00
1,0		MAG	MAG0	045		1	1015 10B55			2	002	
1,0		MAG	MAG1	040		2	1015 11B55			1	003	
1,0		MAG	MAG2	040		1	1015 12B55			2	004	
2,0		MAG	MAG3	040		2	1015 13B55			1	005	
10,0		DAM	DAM	210		1	1015 14B21	S		0	006	10,0/ 0,0
5,8		ARI	ARI0	270		0	1015 05A57	S		1	001	MCDI01
1,0		MAG	MAG0	050		1	1015 10B53			2	002	
1,0		MAG	MAG1	045		2	1015 11B53			1	003	
1,0		MAG	MAG2	045		1	1015 12B53			2	004	
1,3		MAG	MAG3	045		2	1015 13B53			1	005	
10,1		DAM	DAM	255		1	1015 14B33	S		0	006	10,1/ 0,0

C	LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LO	WT	WSEQ	SIGNAL NAME
	5,0		ARI	ARI0	285		0	1015 05A60	S	1		001	MCDI02
	1,0		MAG	MAG0	055		1	1015 10B51		2		002	
	1,0		MAG	MAG1	050		2	1015 11B51		1		003	
	1,0		MAG	MAG2	050		1	1015 12B51		2		004	
	1,3		MAG	MAG3	050		2	1015 13B51		1		005	
	9,3		DAM	DAM	265		1	1015 14B35	S	0		006	9,3/ 0,0
	5,0		ARI	ARI0	280		0	1015 05A59	S	1		001	MCDI03
	1,0		MAG	MAG0	060		1	1015 10B49		2		002	
	1,0		MAG	MAG1	055		2	1015 11B49		1		003	
	1,0		MAG	MAG2	055		1	1015 12B49		2		004	
	1,3		MAG	MAG3	055		2	1015 13B49		1		005	
	9,3		DAM	DAM	260		1	1015 14B34	S	0		006	9,3/ 0,0
	3,5		ARI	ARI4	310		0	1015 06A64	S	1		001	MCDI04
	1,0		MAG	MAG0	065		1	1015 10B27		2		002	
	1,0		MAG	MAG1	060		2	1015 11B27		1		003	
	1,0		MAG	MAG2	060		1	1015 12B27		2		004	
	1,0		MAG	MAG3	060		2	1015 13B27		1		005	
	7,5		DAM	DAM	220		1	1015 14B23	S	0		006	7,5/ 0,0
	3,5		ARI	ARI4	275		0	1015 06A57	S	1		001	MCDI05
	1,0		MAG	MAG0	070		1	1015 10B25		2		002	
	1,0		MAG	MAG1	065		2	1015 11B25		1		003	
	1,0		MAG	MAG2	065		1	1015 12B25		2		004	
	1,3		MAG	MAG3	065		2	1015 13B25		1		005	
	7,8		DAM	DAM	215		1	1015 14B22	S	0		006	7,8/ 0,0
	4,3		ARI	ARI4	290		0	1015 06A60	S	1		001	MCDI06
	1,0		MAG	MAG0	075		1	1015 10B31		2		002	
	1,0		MAG	MAG1	070		2	1015 11B31		1		003	
	1,0		MAG	MAG2	070		1	1015 12B31		2		004	
	1,0		MAG	MAG3	070		2	1015 13B31		1		005	
	8,3		DAM	DAM	225		1	1015 14B25	S	0		006	8,3/ 0,0
	4,3		ARI	ARI4	285		0	1015 06A59	S	1		001	MCDI07
	1,0		MAG	MAG0	080		1	1015 10B29		2		002	
	1,0		MAG	MAG1	075		2	1015 11B29		1		003	
	1,0		MAG	MAG2	075		1	1015 12B29		2		004	
	1,0		MAG	MAG3	075		2	1015 13B29		1		005	
	8,3		DAM	DAM	205		1	1015 14B19	S	0		006	8,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EG	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
1,3		ARI	ARI8	305		0	1015 07A64	S	1		001	MCDI08
1,0		MAG	MAG0	085		1	1015 10A49			2	002	
1,0		MAG	MAG1	080		2	1015 11A49			1	003	
1,0		MAG	MAG2	080		1	1015 12A49			2	004	
3,0		MAG	MAG3	080		2	1015 13A49			1	005	
7,3		DAM	DAM	165		1	1015 14B09	S	0		006	7,3/ 0,0
1,5		ARI	ARI8	270		0	1015 07A57	S	1		001	MCDI09
1,0		MAG	MAG0	090		1	1015 10A53			2	002	
1,0		MAG	MAG1	085		2	1015 11A53			1	003	
1,0		MAG	MAG2	085		1	1015 12A53			2	004	
1,0		MAG	MAG3	085		2	1015 13A53			1	005	
5,5		DAM	DAM	095		1	1015 14A53	S	0		006	5,5/ 0,0
1,3		ARI	ARI8	285		0	1015 07A60	S	1		001	MCDI10
1,0		MAG	MAG0	095		1	1015 10A47			2	002	
1,0		MAG	MAG1	090		2	1015 11A47			1	003	
1,0		MAG	MAG2	090		1	1015 12A47			2	004	
3,0		MAG	MAG3	090		2	1015 13A47			1	005	
7,3		DAM	DAM	170		1	1015 14B10	S	0		006	7,3/ 0,0
2,0		ARI	ARI8	280		0	1015 07A59	S	1		001	MCDI11
1,0		MAG	MAG0	100		1	1015 10A33			2	002	
1,0		MAG	MAG1	095		2	1015 11A33			1	003	
1,0		MAG	MAG2	095		1	1015 12A33			2	004	
1,3		MAG	MAG3	095		2	1015 13A33			1	005	
6,3		DAM	DAM	090		1	1015 14A51	S	0		006	6,3/ 0,0
2,0		ARI	ARI1	305		0	1015 08A64	S	1		001	MCDI12
1,0		MAG	MAG0	105		1	1015 10A27			2	002	
1,0		MAG	MAG1	100		2	1015 11A27			1	003	
1,0		MAG	MAG2	100		1	1015 12A27			2	004	
2,0		MAG	MAG3	100		2	1015 13A27			1	005	
7,0		DAM	DAM	100		1	1015 14A55	S	0		006	7,0/ 0,0
1,5		ARI	ARI1	270		0	1015 08A57	S	1		001	MCDI13
1,0		MAG	MAG0	110		1	1015 10A35			2	002	
1,0		MAG	MAG1	105		2	1015 11A35			1	003	
1,0		MAG	MAG2	105		1	1015 12A35			2	004	
1,3		MAG	MAG3	105		2	1015 13A35			1	005	
5,8		DAM	DAM	085		1	1015 14A49	S	0		006	5,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
2,0		ARI	ARI1	285		0	1015 08A60	S	1		001	MCDI14
1,0		MAG	MAG0	115		1	1015 10A25		2		002	
1,0		MAG	MAG1	110		2	1015 11A25		1		003	
1,0		MAG	MAG2	110		1	1015 12A25		2		004	
2,0		MAG	MAG3	110		2	1015 13A25		1		005	
7,0		DAM	DAM	105		1	1015 14A57	S	0		006	7,0/ 0,0
2,5		ARI	ARI1	280		0	1015 08A59	S	1		001	MCDI15
1,0		MAG	MAG0	120		1	1015 10A19		2		002	
1,0		MAG	MAG1	115		2	1015 11A19		1		003	
1,0		MAG	MAG2	115		1	1015 12A19		2		004	
2,0		MAG	MAG3	115		2	1015 13A19		1		005	
7,5		DAM	DAM	080		1	1015 14A47	S	0		006	7,5/ 0,0
1,0		MAG	MAG0	030		0	1015 10A51		1		001	MCDIPL
1,0		MAG	MAG1	030		1	1015 11A51		2		002	
1,0		MAG	MAG2	030		2	1015 12A51		1		003	
4,3		MAG	MAG3	030		1	1015 13A51		2		004	
7,3		DAM	DAM	245		2	1015 14B30	S	0		005	7,3/ 0,0
1,0		MAG	MAG0	035		0	1015 10A21		1		001	MCDIPR
1,0		MAG	MAG1	035		1	1015 11A21		2		002	
1,0		MAG	MAG2	035		2	1015 12A21		1		003	
5,0		MAG	MAG3	035		1	1015 13A21		2		004	
8,0		DAM	DAM	190		2	1015 14B15	S	0		005	8,0/ 0,0
6,5		ARI	ARI0	215		0	1015 05A46		1		001	MCD000
1,0		MAG	MAG0	125		1	1015 10B61	S	2		002	
1,0		MAG	MAG1	120		2	1015 11B61	S	1		003	
1,0		MAG	MAG2	120		1	1015 12B61	S	2		004	
1,5		MAG	MAG3	120		2	1015 13B61	S	1		005	
11,0		DAM	DAM	270		1	1015 14B37		0		006	11,0/ 0,0
6,5		ARI	ARI0	190		0	1015 05A41		1		001	MCD001
1,0		MAG	MAG0	130		1	1015 10B59	S	2		002	
1,0		MAG	MAG1	125		2	1015 11B59	S	1		003	
1,0		MAG	MAG2	125		1	1015 12B59	S	2		004	
2,0		MAG	MAG3	125		2	1015 13B59	S	1		005	
11,5		DAM	DAM	250		1	1015 14B31		0		006	11,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
5,8		ARI	ARI0	225		0	1015 05A48			1	001	MCD002
1,0		MAG	MAG0	135		1	1015 10B57	S		2	002	
1,0		MAG	MAG1	130		2	1015 11B57	S		1	003	
1,0		MAG	MAG2	130		1	1015 12B57	S		2	004	
1,5		MAG	MAG3	130		2	1015 13B57	S		1	005	
10,3		DAM	DAM	280		1	1015 14B46			0	006	10,3/ 0,0
5,8		ARI	ARI0	210		0	1015 05A45			1	001	MCD003
1,0		MAG	MAG0	140		1	1015 10B47	S		2	002	
1,0		MAG	MAG1	135		2	1015 11B47	S		1	003	
1,0		MAG	MAG2	135		1	1015 12B47	S		2	004	
1,3		MAG	MAG3	135		2	1015 13B47	S		1	005	
10,1		DAM	DAM	240		1	1015 14B29			0	006	10,1/ 0,0
5,0		ARI	ARI4	220		0	1015 06A46			1	001	MCD004
1,0		MAG	MAG0	145		1	1015 10B45	S		2	002	
1,0		MAG	MAG1	140		2	1015 11B45	S		1	003	
1,0		MAG	MAG2	140		1	1015 12B45	S		2	004	
1,5		MAG	MAG3	140		2	1015 13B45	S		1	005	
9,5		DAM	DAM	235		1	1015 14B28			0	006	9,5/ 0,0
5,0		ARI	ARI4	195		0	1015 06A41			1	001	MCD005
1,0		MAG	MAG0	150		1	1015 10B33	S		2	002	
1,0		MAG	MAG1	145		2	1015 11B33	S		1	003	
1,0		MAG	MAG2	145		1	1015 12B33	S		2	004	
1,3		MAG	MAG3	145		2	1015 13B33	S		1	005	
9,3		DAM	DAM	200		1	1015 14B17			0	006	9,3/ 0,0
4,3		ARI	ARI4	230		0	1015 06A48			1	001	MCD006
1,0		MAG	MAG0	155		1	1015 10B23	S		2	002	
1,0		MAG	MAG1	150		2	1015 11B23	S		1	003	
1,0		MAG	MAG2	150		1	1015 12B23	S		2	004	
1,0		MAG	MAG3	150		2	1015 13B23	S		1	005	
8,3		DAM	DAM	230		1	1015 14B27			0	006	8,3/ 0,0
4,3		ARI	ARI4	215		0	1015 06A45			1	001	MCD007
1,0		MAG	MAG0	160		1	1015 10B21	S		2	002	
1,0		MAG	MAG1	155		2	1015 11B21	S		1	003	
1,0		MAG	MAG2	155		1	1015 12B21	S		2	004	
1,3		MAG	MAG3	155		2	1015 13B21	S		1	005	
8,6		DAM	DAM	195		1	1015 14B16			0	006	8,6/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
1,3		ARI	ARI8	215	0	1015 07A46		1	001	MCD008
1,0		MAG	MAG0	165	1	1015 10A55	S	2	002	
1,0		MAG	MAG1	160	2	1015 11A55	S	1	003	
1,0		MAG	MAG2	160	1	1015 12A55	S	2	004	
3,0		MAG	MAG3	160	2	1015 13A55	S	1	005	
7,3		DAM	DAM	175	1	1015 14B11		0	006	7,3/ 0,0
1,5		ARI	ARI8	190	0	1015 07A41		1	001	MCD009
1,0		MAG	MAG0	170	1	1015 10A45	S	2	002	
1,0		MAG	MAG1	165	2	1015 11A45	S	1	003	
1,0		MAG	MAG2	165	1	1015 12A45	S	2	004	
1,5		MAG	MAG3	165	2	1015 13A45	S	1	005	
6,0		DAM	DAM	135	1	1015 14A67		0	006	6,0/ 0,0
1,3		ARI	ARI8	225	0	1015 07A48		1	001	MCD010
1,0		MAG	MAG0	175	1	1015 10A39	S	2	002	
1,0		MAG	MAG1	170	2	1015 11A39	S	1	003	
1,0		MAG	MAG2	170	1	1015 12A39	S	2	004	
3,5		MAG	MAG3	170	2	1015 13A39	S	1	005	
7,8		DAM	DAM	180	1	1015 14B13		0	006	7,8/ 0,0
1,5		ARI	ARI8	210	0	1015 07A45		1	001	MCD011
1,0		MAG	MAG0	180	1	1015 10A41	S	2	002	
1,0		MAG	MAG1	175	2	1015 11A41	S	1	003	
1,0		MAG	MAG2	175	1	1015 12A41	S	2	004	
1,5		MAG	MAG3	175	2	1015 13A41	S	1	005	
6,0		DAM	DAM	125	1	1015 14A65		0	006	6,0/ 0,0
1,0		ARI	ARI1	215	0	1015 08A46		1	001	MCD012
1,0		MAG	MAG0	185	1	1015 10A37	S	2	002	
1,0		MAG	MAG1	180	2	1015 11A37	S	1	003	
1,0		MAG	MAG2	180	1	1015 12A37	S	2	004	
1,5		MAG	MAG3	180	2	1015 13A37	S	1	005	
5,5		DAM	DAM	110	1	1015 14A59		0	006	5,5/ 0,0
1,3		ARI	ARI1	190	0	1015 08A41		1	001	MCD013
1,0		MAG	MAG0	190	1	1015 10A23	S	2	002	
1,0		MAG	MAG1	185	2	1015 11A23	S	1	003	
1,0		MAG	MAG2	185	1	1015 12A23	S	2	004	
1,5		MAG	MAG3	185	2	1015 13A23	S	1	005	
5,8		DAM	DAM	075	1	1015 14A45		0	006	5,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
2,0		ARI	ARI1	225		0	1015 08A48			1	001	MCDG14
1,0		MAG	MAG0	195		1	1015 10A17	S	2		002	
1,0		MAG	MAG1	190		2	1015 11A17	S	1		003	
1,0		MAG	MAG2	190		1	1015 12A17	S	2		004	
2,5		MAG	MAG3	190		2	1015 13A17	S	1		005	
7,5		DAM	DAM	115		1	1015 14A61		0		006	7,5/ 0,0
2,0		ARI	ARI1	210		0	1015 08A45		1		001	MCDG15
1,0		MAG	MAG0	200		1	1015 10A15	S	2		002	
1,0		MAG	MAG1	195		2	1015 11A15	S	1		003	
1,0		MAG	MAG2	195		1	1015 12A15	S	2		004	
2,0		MAG	MAG3	195		2	1015 13A15	S	1		005	
7,0		DAM	DAM	070		1	1015 14A43		0		006	7,0/ 0,0
1,0		MAG	MAG0	020		0	1015 10B19		1		001	MCDGPL
1,0		MAG	MAG1	020		1	1015 11B19		2		002	
1,0		MAG	MAG2	020		2	1015 12B19		1		003	
4,3		MAG	MAG3	020		1	1015 13B19		2		004	
7,3		DAM	DAM	050		2	1015 14A35		0		005	7,3/ 0,0
1,0		MAG	MAG0	025		0	1015 10A13		1		001	MCDGPR
1,0		MAG	MAG1	025		1	1015 11A13		2		002	
1,0		MAG	MAG2	025		2	1015 12A13		1		003	
1,5		MAG	MAG3	025		1	1015 13A13		2		004	
4,5		DAM	DAM	055		2	1015 14A37		0		005	4,5/ 0,0
3,0		MEM	MEM	360		0	1015 09B07		1		001	MCENB3
3,0		SCD	SCDC	390		1	1015 02B28	S	0		002	3,0/ 0,0
5,0		MEM	MEM	235		0	1015 09A50		1		001	MCENMAB
5,0		SCD	SCDC	405		1	1015 02B31	S	0		002	5,0/ 0,0
3,0		SCD	SCDC	015		0	1015 02A06		1		001	MCENMB
0,5		ARI	ARI0	295		1	1015 05A62		2		002	
0,5		ARI	ARI4	300		2	1015 06A62		1		003	
0,5		ARI	ARI8	295		1	1015 07A62		2		004	
5,8		ARI	ARI1	295		2	1015 08A62		1		005	
10,3		DAM	DAM	015		1	1015 14A09	S	0		006	10,3/ 0,0
0,0		MEM	MEM	445		0	1015 09B26	S	1		001	MCFEN0=
		MAG	MAG0	010		1	1015 10A36		0		002	

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LO WT	WSEQ	SIGNAL NAME
5,8		MAG	MAG1	010	0	1015 11A36		1	001	MCFEN1=
5,8		MEM	MEM	540	1	1015 09B45	S	0	002	5,8/ 0,0
6,5		MAG	MAG2	010	0	1015 12A36		1	001	MCFEN2=
6,5		MEM	MEM	550	1	1015 09B47	S	0	002	6,5/ 0,0
6,5		MAG	MAG3	010	0	1015 13A36		1	001	MCFEN3=
6,5		MEM	MEM	525	1	1015 09B42	S	0	002	6,5/ 0,0
~~0,0~~		~~MAG~~	~~MAG0~~	~~010~~	~~0~~	~~1015 10A34~~		~~0~~	~~001~~	~~MCFEN0~~
5,0		MEM	MEM	450	0	1015 09B27	S	1	001	MCFINT=
1,0		MAG	MAG0	265	1	1015 10A32		2	002	
1,0		MAG	MAG1	260	2	1015 11A32		1	003	
1,0		MAG	MAG2	260	1	1015 12A32		2	004	
8,0		MAG	MAG3	260	2	1015 13A32		0	005	8,0/ 0,0
6,5		MEM	MEM	510	0	1015 09B39	S	1	001	MCFRET=
1,0		MAG	MAG0	270	1	1015 10A11		2	002	
1,0		MAG	MAG1	265	2	1015 11A11		1	003	
1,0		MAG	MAG2	265	1	1015 12A11		2	004	
9,5		MAG	MAG3	265	2	1015 13A11		0	005	9,5/ 0,0
6,5		MEM	MEM	480	0	1015 09B33	S	1	001	MCFWRT=
1,0		MAG	MAG0	275	1	1015 10A09		2	002	
1,0		MAG	MAG1	270	2	1015 11A09		1	003	
1,0		MAG	MAG2	270	1	1015 12A09		2	004	
9,5		MAG	MAG3	270	2	1015 13A09		0	005	9,5/ 0,0
3,0		MEM	MEM	320	0	1015 09A67	S	1	001	MCRW=
1,0		MAG	MAG0	280	1	1015 10A07		2	002	
1,0		MAG	MAG1	275	2	1015 11A07		1	003	
1,0		MAG	MAG2	275	1	1015 12A07		2	004	
5,8		MAG	MAG3	275	2	1015 13A07		1	005	
2,5		PFS	PFS	130	1	1015 17B12	S	2	006	
14,3		DAM	DAM	320	2	1015 14B52		0	007	14,3/ 0,0
6,5		DAM	DAM	330	0	1015 14B55		1	001	MCWRENT=
3,0		MEM	MEM	245	1	1015 09A52		2	002	
9,5		SCD	SCDC	195	2	1015 02A45	S	0	003	9,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LO WT	WSEQ	SIGNAL NAME
2,0		PFS	PFS	015	0	1015 17B09		1	001	MRESET=
5,0		DAM	DAM	140	1	1015 14A68		2	002	
0,5		ARI	ARI1	145	2	1015 08A32		1	003	
0,8		ARI	ARI1	115	1	1015 08A26		2	004	
3,5		ARI	ARI8	145	2	1015 07A32		1	005	
2,0		ADF	ADF	310	1	1015 01A65		2	006	
2,0		SCD	SCDC	315	2	1015 02B12	S	1	007	
1,0		M=D	M=D	040	1	1015 04B49		2	008	
2,5		INR	INR	655	2	1015 03B66		1	009	
19,3		MEM	MEM	530	1	1015 09B43		0	010	19,3/ 0,0
6,5		TTY	TTY	285	0	1015 16B49		1	001	MT0=
6,5		MEM	MEM	335	1	1015 09A70	S	0	002	6,5/ 0,0
5,8		TTY	TTY	280	0	1015 16B47		1	001	MT2=
5,8		MEM	MEM	365	1	1015 09B09	S	0	002	5,8/ 0,0
5,0		TTY	TTY	275	0	1015 16B45		1	001	MT4=
5,0		MEM	MEM	675	1	1015 09B62	S	0	002	5,0/ 0,0
2,0		MEM	MEM	275	0	1015 09A58		1	001	OPTRDWR=
2,0		M=D	M=D	525	1	1015 04A66	S	0	002	2,0/ 0,0
2,5		PFS	PFS	300	0	1015 17A60		1	001	P12V
2,5		MAG	MAG3	280	1	1015 13A68		0	002	2,5/ 0,0
2,0		PFS	PFS	305	0	1015 17A61		1	001	P24V
2,0		MAG	MAG3	285	1	1015 13A60		0	002	2,0/ 0,0
0,0		DAM	DAM	160	0	1015 14B07	S	0	001	PARER
5,8		SCD	SCDC	525	0	1015 02B55		1	001	PARER=
~~7,5~~		~~ADF~~	~~ADF~~	~~235~~	~~1~~	~~1015 01A58~~		~~2~~	~~002~~	
13,3		DAM	DAM	145	1	1015 14A69	S	0	002	13,3/ 0,0
5,8		SCD	SCDC	340	0	1015 02B18	S	1	001	PCLDAD
0,5		ARI	ARI0	015	1	1015 05A06		2	002	
0,5		ARI	ARI4	020	2	1015 06A06		1	003	
0,5		ARI	ARI8	015	1	1015 07A06		2	004	
7,3		ARI	ARI1	015	2	1015 08A06		0	005	7,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LO	WT	WSEQ	SIGNAL NAME
1,0		SCD	SCDC	490		0	1015 02B48			1	001	PCLDAD2=
9,5		M=D	M=D	490		1	1015 04B63	S		2	002	
10,5		PFS	PFS	155		2	1015 17A65	S		0	003	10,5/ 0,0
0,0		ARI	ARIO	020		0	1015 05A07	S		0	001	PCR00=
10,5		PFS	PFS	020		0	1015 17B63			1	001	PCR01=
3,0		ADF	ADF	290		1	1015 01A61			2	002	
13,5		ARI	ARIO	095		2	1015 05A22	S		0	003	13,5/ 0,0
10,5		PFS	PFS	025		0	1015 17B62			1	001	PCR02=
1,5		ARI	ARIO	030		1	1015 05A09	S		2	002	
12,0		ADF	ADF	025		2	1015 01A08			0	003	12,0/ 0,0
10,5		PFS	PFS	030		0	1015 17B61			1	001	PCR03=
2,0		ADF	ADF	175		1	1015 01A38			2	002	
12,5		ARI	ARIO	085		2	1015 05A20	S		0	003	12,5/ 0,0
10,5		PFS	PFS	035		0	1015 17B60			1	001	PCR04=
2,5		ADF	ADF	195		1	1015 01A42			2	002	
13,0		ARI	ARI4	025		2	1015 06A07	S		0	003	13,0/ 0,0
9,5		PFS	PFS	040		0	1015 17B59			1	001	PCR05=
2,0		ARI	ARI4	100		1	1015 06A22	S		2	002	
11,5		ADF	ADF	035		2	1015 01A10			0	003	11,5/ 0,0
10,5		PFS	PFS	045		0	1015 17B58			1	001	PCR06=
10,5		ARI	ARI4	035		1	1015 06A09	S		0	002	10,5/ 0,0
9,5		PFS	PFS	050		0	1015 17B57			1	001	PCR07=
9,5		ARI	ARI4	090		1	1015 06A20	S		0	002	9,5/ 0,0
9,5		PFS	PFS	055		0	1015 17B48			1	001	PCR08=
9,5		ARI	ARI8	020		1	1015 07A07	S		0	002	9,5/ 0,0
9,5		PFS	PFS	060		0	1015 17B49			1	001	PCR09=
9,5		ARI	ARI8	095		1	1015 07A22	S		0	002	9,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
9,5		PFS	PFS	065	0	1015 17B47		1	001	PCR10=
9,5		ARI	ARI8	030	1	1015 07A09	S	0	002	9,5/ 0,0
9,5		PFS	PFS	070	0	1015 17B45		1	001	PCR11=
9,5		ARI	ARI8	085	1	1015 07A20	S	0	002	9,5/ 0,0
9,5		PFS	PFS	075	0	1015 17B43		1	001	PCR12=
9,5		ARI	ARI1	020	1	1015 08A07	S	0	002	9,5/ 0,0
8,5		PFS	PFS	080	0	1015 17B42		1	001	PCR13=
8,5		ARI	ARI1	095	1	1015 08A22	S	0	002	8,5/ 0,0
9,5		PFS	PFS	085	0	1015 17B44		1	001	PCR14=
9,5		ARI	ARI1	030	1	1015 08A09	S	0	002	9,5/ 0,0
8,5		PFS	PFS	090	0	1015 17B46		1	001	PCR15=
8,5		ARI	ARI1	085	1	1015 08A20	S	0	002	8,5/ 0,0
5,8		SCD	SCDC	140	0	1015 02A33	S	1	001	PCRDR=
0,5		ARI	ARI0	530	1	1015 05B43		2	002	
0,5		ARI	ARI4	545	2	1015 06B43		1	003	
0,5		ARI	ARI8	535	1	1015 07B43		2	004	
6,5		ARI	ARI1	530	2	1015 08B43		1	005	
13,8		PFS	PFS	125	1	1015 17B18	S	0	006	13,8/ 0,0
4,3		SCD	SCDC	295	0	1015 02B08		1	001	PFRST=
1,0		MAG	MAG0	015	1	1015 10B41		2	002	
1,0		MAG	MAG1	015	2	1015 11B41		1	003	
1,0		MAG	MAG2	015	1	1015 12B41		2	004	
5,0		MAG	MAG3	015	2	1015 13B41		1	005	
12,3		PFS	PFS	285	1	1015 17A48	S	0	006	12,3/ 0,0
9,5		ADF	ADF	125	0	1015 01A28		1	001	PFSINT=
9,5		PFS	PFS	260	1	1015 17A52	S	0	002	9,5/ 0,0
3,5		ADF	ADF	660	0	1015 01B67	S	1	001	PUARI
5,0		ARI	ARI0	350	1	1015 05B05		2	002	
8,5		ARI	ARI0	010	2	1015 05A05		0	003	8,5/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
8,5		TTY	TTY	170		0	1015 16A69		1	001	REXT1=
8,5		SCD	SCDC	275		1	1015 02A66	S	0	002	8,5/ 0,0
7,5		DAM	DAM	120		0	1015 14A63		1	001	REXT2=
7,5		SCD	SCDC	265		1	1015 02A64	S	0	002	7,5/ 0,0
3,0		PFS	PFS	105		0	1015 17B52		1	001	SCDC0
7,5		DAM	DAM	150		1	1015 14B03		2	002	
10,5		SCD	SCDC	430		2	1015 02B36	S	0	003	10,5/ 0,0
0,0		SCD	SCDC	450		0	1015 02B40	S	0	001	SCDC0=
3,5		MEM	MEM	280		0	1015 09A59		1	001	SCDC0R
3,5		SCD	SCDC	305		1	1015 02B10	S	0	002	3,5/ 0,0
1,0		ADF	ADF	605		0	1015 01B56		1	001	SCDC1=
0,5		SCD	SCDC	425		1	1015 02B35	S	2	002	
1,0		INR	INR	510		2	1015 03B37		1	003	
2,5		M=D	M=D	025		1	1015 04B52		0	004	2,5/ 0,0
0,0		M=D	M=D	480		0	1015 04B60	S	0	001	SCDC11CP=
		M-D	M-D			0	1015 04A64		1	000	
0,8		SCD	SCDC	460		1	1015 02B42	S	2	001	SCDC1A
~~2,5~~		~~M-D~~	~~M-D~~	~~020~~		~~1~~	~~1015 04B47~~		~~2~~	~~002~~	
5,8		MEM	MEM	485		2	1015 09B34		1	002	
9,1		PFS	PFS	110		1	1015 17B25		0	003	9,1/ 0,0
7,5		DAM	DAM	155		0	1015 14B05		1	001	SCDC1F0
7,5		SCD	SCDC	360		1	1015 02B22	S	0	002	7,5/ 0,0
4,3		MEM	MEM	295		0	1015 09A62		1	001	SCDC3
4,3		SCD	SCDC	365		1	1015 02B23	S	0	002	4,3/ 0,0
3,5		MEM	MEM	300		0	1015 09A63		1	001	SCDC3=
0,8		INR	INR	445		1	1015 03B24		2	002	
4,3		SCD	SCDC	335		2	1015 02B17	S	0	003	4,3/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
3,0		MEM	MEM	360		0	1015 09B49		1	001	SCDC4
1,0		ADF	ADF	355		1	1015 01B46		2	002	
4,0		SCD	SCDC	400		2	1015 02B30	S	0	003	4,0/ 0,0
1,0		INR	INR	220		0	1015 03A47		1	001	SCDC4=
3,5		ADF	ADF	295		1	1015 01A62		2	002	
4,5		SCD	SCDC	410		2	1015 02B32	S	0	003	4,5/ 0,0
3,0		MEM	MEM	270		0	1015 09A57		1	001	SCDC4R
3,0		SCD	SCDC	260		1	1015 02A63	S	0	002	3,0/ 0,0
1,5		ADF	ADF	515		0	1015 01B38		1	001	SCDC5
1,5		SCD	SCDC	300		1	1015 02B09	S	0	002	1,5/ 0,0
1,3		INR	INR	535		0	1015 03B42		1	001	SCDC5=
1,3		SCD	SCDC	350		1	1015 02B20	S	0	002	1,3/ 0,0
0,5		ADF	ADF	265		0	1015 01A56		1	001	SCDC7
0,5		SCD	SCDC	255		1	1015 02A61	S	0	002	0,5/ 0,0
2,0		INR	INR	035		0	1015 03A10		1	001	SCDC7=
0,5		ADF	ADF	210		1	1015 01A45		2	002	
2,5		SCD	SCDC	205		2	1015 02A47	S	0	003	2,5/ 0,0
3,5		MEM	MEM	325		0	1015 09A68		1	001	SCDC7ORB=
3,5		SCD	SCDC	215		1	1015 02A49	S	0	002	3,5/ 0,0
0,0		SCD	SCDC	180		0	1015 02A41	S	0	001	SCDC9
4,3		ADF	ADF	445		0	1015 01B24		1	001	SCDC9=
4,3		SCD	SCDC	160		1	1015 02A37	S	0	002	4,3/ 0,0
0,8		ARI	ARI8	405		0	1015 07B16		1	001	SCDCB
3,0		ARI	ARI4	370		1	1015 06B08		-2	002	
3,8		SCD	SCDC	230		2	1015 02A52	S	0	003	3,8/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL EQ	LI	LOCATION	S	LG WT	WSEQ	SIGNAL NAME
4,3		INR	INR	460	0	1015 03B27		1	001	SCDCB=
1,3		SCD	SCDC	165	1	1015 02A38	S	2	002	
5,6		ADF	ADF	045	2	1015 01A12		0	003	5,6/ 0,0
6,5		INR	INR	640	0	1015 03B63		1	001	SCDCC
6,5		SCD	SCDC	155	1	1015 02A36	S	0	002	6,5/ 0,0
2,5		ADF	ADF	325	0	1015 01A68		1	001	SCDCC=
2,5		SCD	SCDC	105	1	1015 02A24	S	0	002	2,5/ 0,0
3,0		MEM	MEM	260	0	1015 09A55		1	001	SCDCCR
3,0		SCD	SCDC	225	1	1015 02A51	S	0	002	3,0/ 0,0
0,0		SCD	SCDC	045	0	1015 02A12	S	0	001	SCDCD
2,0		ADF	ADF	215	0	1015 01A46		1	001	SCDCD=
2,0		SCD	SCDC	055	1	1015 02A14	S	0	002	2,0/ 0,0
0,0		SCD	SCDC	190	0	1015 02A44		0	001	SCR0CPT=
0,0		SCD	SCDC	370	0	1015 02B24		0	001	SCR1CPT=
0,0		SCD	SCDC	240	0	1015 02A55		0	001	SCR2CPT=
1,0		SCD	SCDC	245	0	1015 02A57		1	001	SCR3CPT=
1,0		M=D	M=D	540	1	1015 04A49	S	0	002	1,0/ 0,0
1,0		SCD	SCDC	150	0	1015 02A35		1	001	SCRFCPT=
1,0		M=D	M=D	535	1	1015 04A47	S	0	002	1,0/ 0,0
		ADF	ADF		0	1015 01A50		1	001	STBINH=
		DAM	DAM		1	1015 14A29	S	0	002	
5,8		INR	INR	185	0	1015 03A40		1	001	T4SCDC1
5,8		SCD	SCDC	505	1	1015 02B51	S	0	002	5,8/ 0,0
5,8		DAM	DAM	060	0	1015 14A39		1	001	TIRC0
4,3		MEM	MEM	410	1	1015 09B19	S	2	002	
10,1		ADF	ADF	275	2	1015 01A58		0	003	10,1/ 0,0

C LNTH	NOTE	CKT	EQUATION	EQL	EG	LI	LOCATION	S	LG	WT	WSEQ	SIGNAL NAME
5,8		PI	PI	170		0	1015 15A47			1	001	TIRC0=
5,8		MEM	MEM	425		1	1015 09B22	S		0	002	5,8/ 0,0
2,0		M=D	M=D	065		0	1015 04B62			1	001	TIRC1
0,8		SCD	SCDC	375		1	1015 02B25			2	002	
2,5		INR	INR	405		2	1015 03B16			1	003	
6,5		MEM	MEM	415		1	1015 09B20	S		2	004	
11,8		DAM	DAM	035		2	1015 14A17			0	005	11,8/ 0,0
6,5		DAM	DAM	045		0	1015 14A33			1	001	TIRC2
2,0		MEM	MEM	470		1	1015 09B31	S		2	002	
8,5		M=D	M=D	075		2	1015 04B46			0	003	8,5/ 0,0
5,0		M=D	M=D	300		0	1015 04A50			1	001	TIRC2=
5,0		MEM	MEM	545		1	1015 09B46	S		0	002	5,0/ 0,0
7,5		DAM	DAM	030		0	1015 14A15			1	001	TIRC3=
6,5		PFS	PFS	095		1	1015 17B64			2	002	
3,0		MEM	MEM	420		2	1015 09B21	S		1	003	
2,5		M=D	M=D	045		1	1015 04B55			2	004	
19,5		ADF	ADF	405		2	1015 01B16			0	005	19,5/ 0,0
5,8		DAM	DAM	065		0	1015 14A41			1	001	TIRC4
3,0		MEM	MEM	400		1	1015 09B17	S		2	002	
4,3		SCD	SCDC	310		2	1015 02B11			1	003	
13,1		INR	INR	155		1	1015 03A34			0	004	13,1/ 0,0
4,3		INR	INR	265		0	1015 03A56			1	001	TIRC4=
3,0		MEM	MEM	405		1	1015 09B18	S		2	002	
1,0		M=D	M=D	050		2	1015 04B59			1	003	
8,3		ADF	ADF	585		1	1015 01B52			0	004	8,3/ 0,0
1,0		INR	INR	530		0	1015 03B41			1	001	TIRCA
2,0		M=D	M=D	055		1	1015 04B30			2	002	
6,5		MEM	MEM	440		2	1015 09B25	S		1	003	
9,5		PFS	PFS	100		1	1015 17B65			0	004	9,5/ 0,0
0,0		TTY	TTY	330		0	1015 16B67			0	001	TTYPLS6V

E N D O F L I S T 1900 RECORDS