Firmware Manual

February, 1996

Rev. B

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Chapter 6 Miscellaneous Information

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Chapter 1 General Information

1.1 Revision History

REVISION	CONTACT	DATE	DESCRIPTION
A	Bob Condie	9/12/95	Initial Release
B	Bob Condie	1/29/96	Revision Release

1.2 Scope

The purpose of this manual is to document the Sirocco firmware commands. This manual documents deviations from the SCSI and AT specifications. In addition to documenting the external interface, certain internal features of the firmware and its architecture are described.

1.3 Sirocco Firmware Features

- K7 CPU
  - 32 bit CPU
  - 40 MHz internal system clock
  - General purpose register architecture
  - 16 M byte linear address space

- µCode download
  - ATA CAM compatible
    Opcode 92h

  - SCSI 2 compatible
    Write buffer opcode 3Bh

  - µCode verification
    µCode checksum and valid product code
    Rom checksum and version stamp

- Double burst correction on the fly
- Triple burst offline correction
- Dynamic cache segments
- Up to 26 pending random write command cache
- Concurrent read / write cache process
- DPA phase 3 error logging and reporting

- New AT block
  - Enhanced auto features
    Supports LBA and MULTIPLE command mode of operation
    Multiple sector auto read/write transfer
    Auto reads across commands
  - PIO mode 4
  - DMA multiword mode 2

- SCSI - 3 message and power saving mode support
- SCAM support
  - Power - on configurable ID's

1.4 Applicable Documents

SCSI-II Specification
CAM ATA Specification
LEO Specification.
Sirocco Selfscan User's Guide (QNTM P/N)
Sirocco SCSI Product Manual (QNTM P/N)
Sirocco AT Product Manual (QNTM P/N)
Quantum DPSG Unified Superset Command Manual
Quantum DPA Implementation Guide
Compaq ATA Drive Failure Prediction Spec. Version 1.30 Proposal

Chapter 2 Defect Management

2.1 The Defect List

Two different lists are stored on system cylinder -2 and -3:

1. Primary defect list (P list) - this list contains the defects found in defect scans at the factory. Only the factory test software has the capability to define the P list. The P list contains the description for defects only. No information regarding their replacement is included.

2. Working list (W list) - typically, the W list is a union of the P and G lists, plus it contains all information necessary to locate the replacement to all defects.
   Grown defect list (G list) - this list contains the defects found in the field during operation of the drive. All user's reassigned defects (i.e. with Reassign Block) and auto-reallocated defects are recorded in this list.

The host may access the P and G lists with the Read Defect Data SCSI command (Read Defect AT Extended command). The G list is decoded from information stored in the W list.

The W list is used by defect management whenever a logical-to-physical address conversion is called for. This list is not accessible with standard SCSI commands.

2.1.1 Replacement Strategy

Sirocco reserve one spare sector per cylinder for 1.7 GB and 2.5 GB drives. It utilizes two methods for sector replacement - inline and offline sparing.

2.1.1.1 Inline Sparing

Inline sparing is where a defective sector is replaced by the next immediate sector; all sectors thereafter within the same cylinder is shifted, logically, by one. (see figure 2.1) The access penalty is very small for inline replacement which is one sector time. Whenever possible, defects are spared with inline replacement at the factory. In the unlikely event where there are multiple defects on the same cylinder, additional spare sectors must be allocated from adjacent cylinders. This is defined as offline replacement. Accessing the defective sector requires a short seek and latency. All grown defects are offline spared during drive operation. However, the drive will attempt to inline spare all known defects when a Format Unit command is issued.

2.1.1.2 Offline Sparing

Off line sparing is where a defective sector is replaced by a spare sector located at the end of a cylinder. Defect management will try to replace the defective sector with a spare on the same cylinder. If this is not possible, as in the case of the spare is already in use, defect management will find a spare sector located on an adjacent cylinder. The disadvantage to this is the performance hit caused by the seek. Figure 2.1 contains an example of an offline spare.

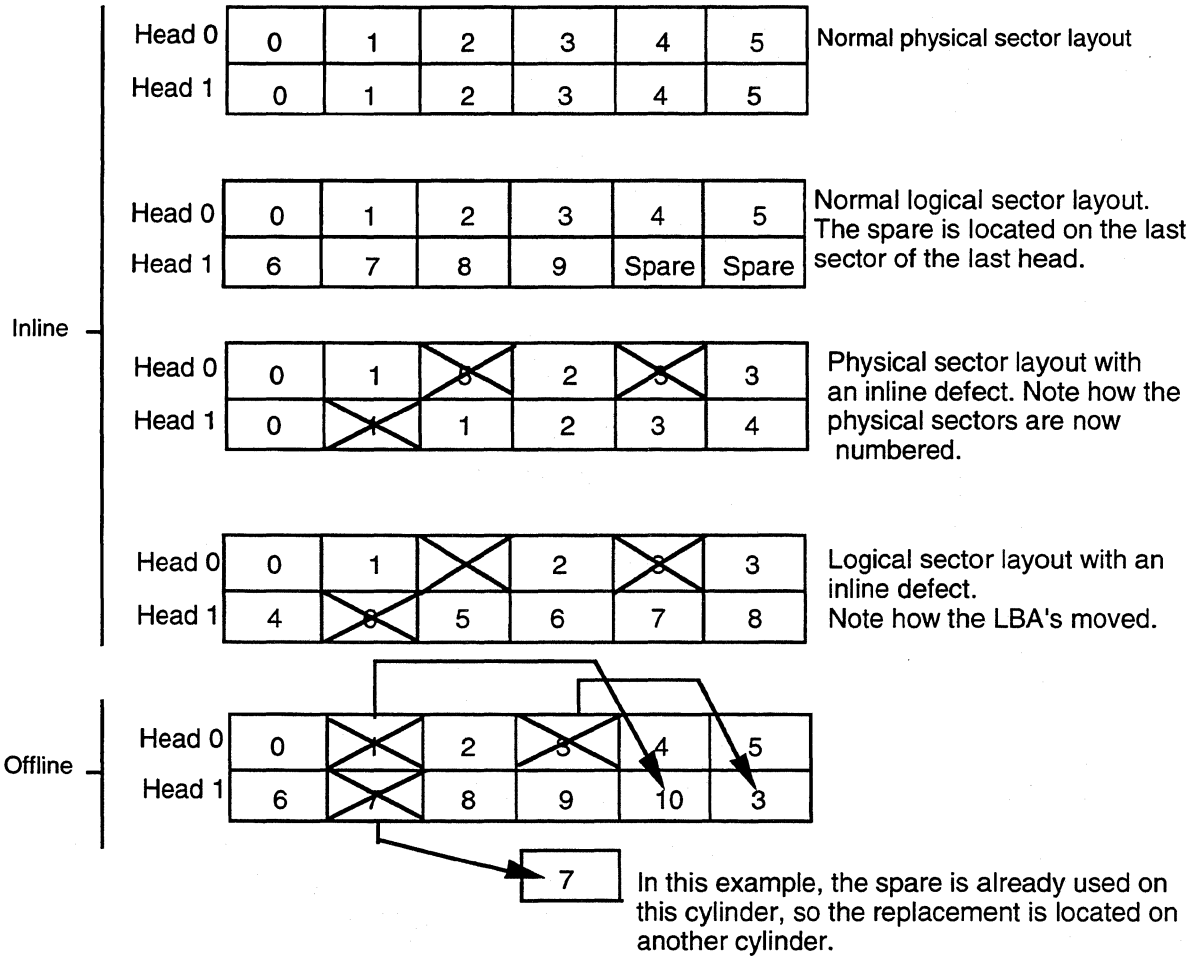

Figure 2-1 Inline and Offline Examples

2.1.1.3 Orphans

An orphan occurs when a replacement sector goes bad. The replacement is assigned a new sector and the original replacement sector is tagged as an orphan in the defect list. It is no longer used. Defect management skips over defect entries that are tagged orphans.

2.1.2 Defect List Data Structure

The defect lists maintained and accessed by the defect management system consist of 7 byte defect entries. The P list contains only defect entries while the W list contains both defect and replacement cylinder information. The defect list structure is illustrated below.

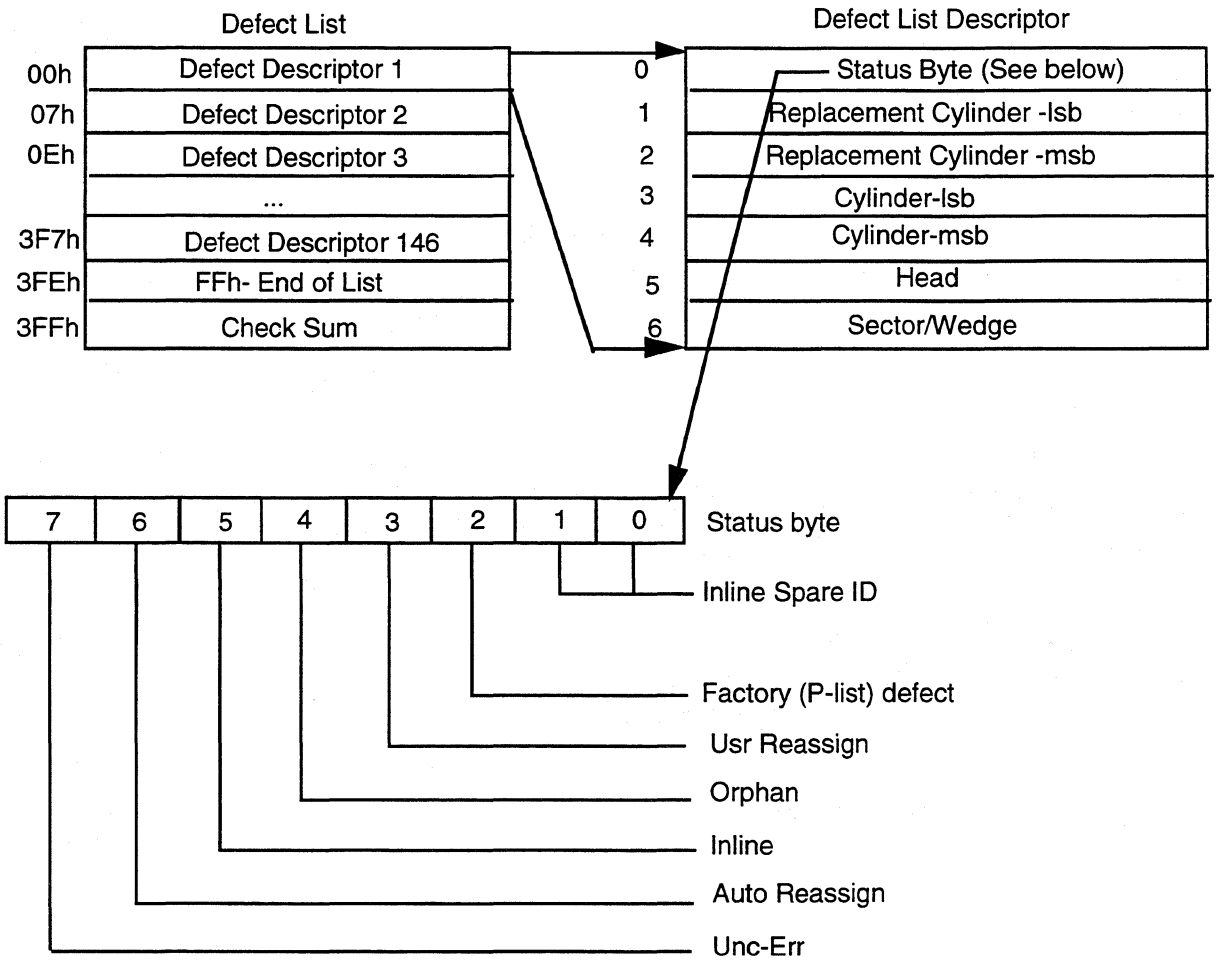

Figure 3-2 Defect List Data Structure

The end of list marker is placed after the last entry in the list.

The checksum is placed at the end of the list, and the empty area in the list is filled with zeros. When this byte is added to the rest of the bytes in the list, the **lsb** of the checksum will equal ASCII "L".

Defect type is used to distinguish between P list entries (factory defect) and G list entries (auto reallocated and user reassigned).

Replacement type is used by defect management to find the correct physical sector for a given LBA.

2.2 Defect List Storage

Up-to-date versions of the P and W lists are saved on the disk, only the W list needs to be resident in RAM during drive operation. Each defect list may require up to 8192 bytes of storage, therefore, a total of 16 sectors per list are reserved to hold the defect lists on a system track. See section 3 for System Cylinder layout for the location of the lists. Since the W list is limited to 8192 bytes in size, a maximum of 1170 defects may be recorded in a Sirocco drive.

2.3 LBA to CHS Conversion

There are two entry points for performing the LBA to CHS conversion. Given an LBA, the caller invokes INIT_LBA_TO_CHS to initiate the conversion process.

INIT_LBA_TO_CHS determines the destination cylinder for the logical block and scans for known defects from the beginning of that cylinder. The function returns the CHS of the first valid sector plus a value indicating the number of consecutive data sectors starting from the first accessible sector.

It is left to the caller to decide how many sectors are actually required to complete its operation. If sectors are needed in addition to the first series of consecutive sectors, the caller uses the INIT_LBA_TO_CHS function to locate the next series of sectors.
NEXT_LBA_TO_CHS requires no input parameter and returns the same information as INIT_LBA_TO_CHS. Since media defects are spares, there should be large number of contiguous cylinders with no defects for a typical drive. Basing on this fact, when a location on the disk is accessed, defect management firmware locates a range of "defect - free" cylinders in both directions of the current position. Once the range is defined, subsequent access made within the range will not require any reference to the defect list.

2.4 Auto Reallocation

Reallocation during read or write operation is processed on sector by sector basis. Reallocation operation is done differently between a read and write command. The differences are identified below:

2.4.1 Read Operation

If an uncorrectable error occurred, the sector in error is still considered as a potential defective sector and auto reallocation will not be perform immediately. A defect entry will be added to the W-list with bit 7 of the status byte set to indicate the defect is a pending defect. If a subsequent read operation recovered the data with triple burst ECC correction, the potential defective sector is subject to ten write/verify test before it will be reallocated. If any of the ten tests fail, the defect is considered repeatable and the sector is reallocated. If all ten tests pass, then the failure is considered non-repeatable and the sector is left as is.
If a subsequent read operation recovered the data without using triple ECC correction or unable to recovered the data, then the pending defect entry will not be removed from W-list. Also the pending defect entry can only be removed from the W-list with either a reassign, a format or a write command.

2.4.2 Write Operation

For write command, the correct data that was received from the host is already available in the buffer so it safe to perform the ten write/verify test on the defective sector. If any of the ten tests fail, the defect is considered repeatable and the sector is reallocated. If all ten tests pass, then the failure is considered non-repeatable and the sector is left as is and the correct data is written to this sector.

2.4.3 Super Mode

For testing purpose, a user can create ECC error and then force auto reallocation with a write command. Each time an ECC is created, it is added to the W-list as pending defect. A write command causes auto reallocation to occur and the pending defect entry is removed from W-list after auto reallocation is finished.

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Chapter 3 System Cylinders

3.1 General Information

Six cylinders on all drives are reserved for system and test usage. These cylinders contain drive configuration information, drive test information, and diskware. Customers cannot access these reserved cylinders. The reserved cylinders are only accessible with physical address commands which are protected diagnostic commands.

Data is stored on heads 0 and 1 in the OD system area.

The reserved cylinders are assigned as follows:

Cylinder	Description Outer System Area
-1	Guardband
-2	System
-3	Copy of cylinder -2
-4	Diskware
-5	Copy of cylinder -4
-6	Test data/Error logging

Note : The data on the system cylinder, unless specified otherwise, will use the following rules:

ASCII fields must be left justified, terminated with binary 0, and padded with binary 0's.
ASCII fields read by the drive firmware, such as the serial number, must be right justified with spaces and terminated with 0.

3.2 System / Firmware Cylinders

This cylinder is reserved for system and firmware usage. It contains modepage information, configuration information, defect list, and format information for the drive.

Sector usages of cylinder -2 and -3 are as follows :

Sector	Description
0	Saved mode page
1 - 12	Configuration pages
13 - 28	Working defect list
29 - 44	Primary defect list
45 - 60	T - List
61 - 76	Format header bytes zone 0-15
77	Apple system sector for rd/wr of OS information
78	Passport sector
79 - 82	Servo defect list
83 - 92	Log sense and log select
93	Unused
94 - 130	Error log
131 - 137	Reserved for in-line defect sparing

Sector Usages of cylinder -4 and -5 are as follows:

Sector	Description
0 - 1	Boot loader
2 - 4	Vector table
5 - 61	Resident Diskware
62- 65	Overlay 0
66- 69	Overlay 1
70- 73	Overlay 2
74- 77	Overlay 3
78- 81	Overlay 4
82- 85	Overlay 5
86- 89	Overlay 6
90- 93	Overlay 7
94- 130	Unused
131- 137	Spare sector

- **Saved Mode Pages**

  The data stored on these sectors is only the changeable part of the mode pages. See the section on Mode Pages for more details.

- **Configuration Pages**

  This area contains the drives configuration information such as the revision level, number of heads, etc. See the Read Configuration superset command for a detailed explanation of the data contained in this sector.

- **Defect List Sectors**

  These sectors contain the defect lists used during the drives normal operation. See the chapter on Defect Management for more information.

- **Format Header Sectors**

  In order for the firmware to format the drive, it needs to know the count byte information for the split sector data fields. Since there is no simple algorithm to generate this information, the count bytes must be stored in a table. We allocated 16 sectors on the system cylinder to hold this information. Each sector contains the count byte information for a particular zone.

3.3 Test Equipment / Error logging Cylinders

The test equipment cylinder is reserved for test process usage. This cylinder contains test parameters and data collected during production test.

The sector usages of cylinder -6 are as follows:

Sector	Description
0	Software Serial #
1	Interlock
2	Reserved
3	Config center
4	Reserved
5 - 14	Test process history queue
15 - 19	Process defect list
20 - 30	Selfscan results
31 - 39	Selfscan script
40 - 41	Selfscan command history
42 - 58	Selfscan defect list
59 - 62	Selfscan servo defect list
63 - 66	Selfscan channel adaptives
67	Selfscan fail
68	Soft error table
69 - 71	Selfscan soft error list
72 - 73	Reserved
74 - 125	Selfscan overlay
126	Selfscan variables
127 - 130	Unused
131 - 137	Reserved for inline sparing

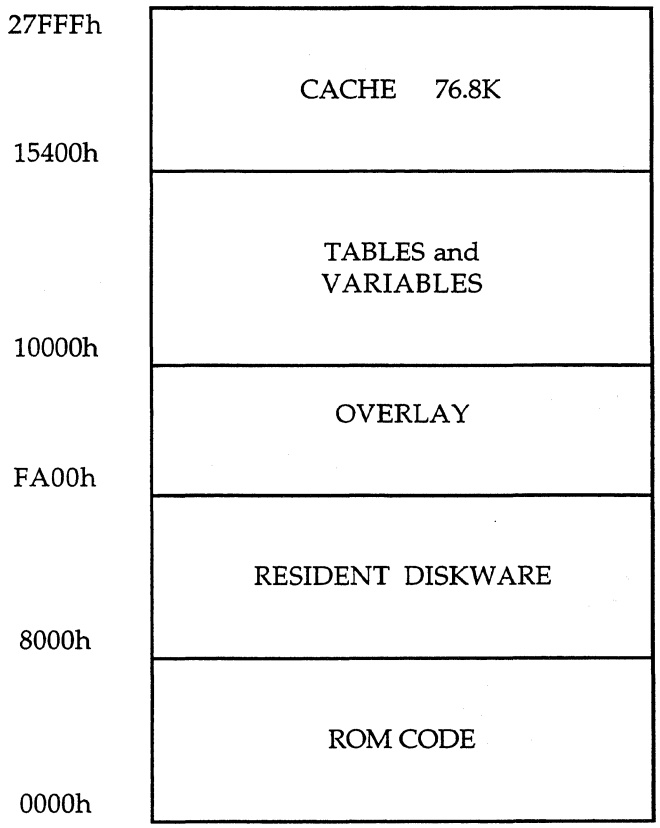
Chapter 4 Diskware

4.1 Introduction

The Sirocco architecture is designed to support diskware and memory overlay. Part of the Buffer memory is used to load firmware from disk and the processor is able to execute the firmware directly from the buffer. When the Sirocco drive is power up, a portion of the Sirocco diskware is loaded into Resident Diskware area in RAM from system cylinder. This portion in Resident Diskware is permanent during whole run-time. The overlay Diskware area stores one of eight overlays at a time which is loaded dynamically based on which is needed.

4.2 Memory Map

The DRAM memory map for Sirocco is organized as follows:



The firmware is partitioned between the ROM code and the Diskware. The ROM code contains all of the routines necessary to power up the drive and read the diskware into the Buffer. It also contains routines that allow the Diskware to be written to the disk via the host interface. All time critical code is located in the ROM because the processor is able to execute ROM code much faster than Diskware code. The Diskware code contains non time critical code that is not required for powering up the drive. The Diskware code also contains provisions to allow firmware bugs in the ROM code to be corrected by mapping erroneous subroutines from ROM into the Diskware.

4.3 Diskware Code Organization

The diskware code space is partitioned into two parts, a resident part and an overlay part. The Resident diskware is loaded during the drive power up initialization and remains in memory while the drive is powered on. The Overlay diskware is loaded when needed.

Address Range	Description
8000h - F7FFh	Resident Diskware (Vector Table; Code)
F800h - FFFFh	Overlay Diskware

The Resident Diskware contains a vector table which is used by the ROM code for accessing Diskware subroutines and data, and for mapping erroneous ROM subroutines into Diskware subroutines. During power up initialization a default vector table is copied from ROM, this is replaced by the actual vector table when the Diskware is loaded from disk.

4.4 Diskware Storage Requirements

The diskware is stored on reserved system cylinders in memory image format. Configuration page 15 specifies where the overlays are stored on the system cylinders and where the overlays are loaded into the processor memory. Generally system cylinder information is stored in multiple places for redundancy, although the overlay configuration page only specifies where the first copy of the diskware is stored. Redundant copies of the diskware are stored according to the firmware redundancy algorithm for system cylinder information. The Sirocco firmware stores redundant system cylinder information on physical head 0 and 1 in system cylinder areas.

Configuration Page 15 - Overlay Page

Field Offset	Description
0	Element number definition
1	Load address
4	Size- number of sectors
5	Cylinder
7	Alternate Cylinder
9	Starting Sector
11	Element number definition
12 - 21	Same fields as above
:	:
165	FFh - End marker

4.5 Write Buffer Command

Write Buffer command with the download option for SCSI and ATA is used to update the diskware. The Write Buffer command is described in the respective interface documents (SCSI ANSI X3T9.2/375R, ATA ANSI X3T9.2/791D). The download options are vendor specific, this specification will define the Quantum implementation of this option.

4.5.1 ATA Write Buffer Command

The command is an optional, class 3 command. The op code used is 92h. Parameters used are the FR, SC, SN, CY registers. (see table 9-1 of the ATA specification). It is also a PIO Data Out command (see section 10.2 of the ATA specification). The head bits of the Drive/Head register shall always be set to zero. The Sector register shall be used to extend the Sector Count register, creating an effective sector count 16 bits long. The Cylinder High and Low registers are reserved.

The value of the Features register shall be used to determine the time the update takes effect, whether it is saved for future use, and any future functions:

Feature register values for Download diskware.

bit 2 1 0	
0 0 1	download is for immediate, temporary use. (Ramware)
1 1 1	save downloaded code for future reference by value of cylinder and specify it as the default for immediate and future use.

Feature register value of 0FEh specifies a download for immediate temporary use with no servo recal.

4.6 Diskware Download Theory of Operation

The write buffer command will download diskware. The download elements are a diskware downloader, an optional diskware boot loader, diskware control page, and diskware overlay entries. The diskware downloader shall be validated by a good checksum, valid product code, compare of the ROM version stamp and ROM checksum. Once the diskware downloader is validated, the diskware downloader will execute.

The diskware downloader will validate the diskware control page and diskware overlay entries by a good checksum, valid product code, compare of the ROM version stamp and ROM checksum. The diskware downloader will put the drive in a "ROM only" state (servo and spindle to run out the ROM) and move the overlay entries to the locations directed to by the diskware control page. The last overlay entry to move is the vector table. Care must be exercised to disable the currently running functions when this table is loaded (i.e. servo and spindle functions that are currently running in "ROM only" mode). Upon completion of the vector table move, the handler will initialize drive mode and configuration page parameters with the ROM defaults. The handler will start execution of the diskware in ram.

The download and save mode will additionally save the diskware data to the reserved cylinders as specified in the diskware control page.

The optional diskware boot loader is firmware that at power up will be read from disk and it will read and validate the remaining diskware elements.

4.7 Diskware Elements

All the diskware elements have a common header at the beginning of each element. The diskware element header is defined as follows:

Byte	Definition of field
0	Element Type
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Length of the element
8-14	Element dependent
15	Checkbyte
16	Start of element data
n	End of element data

Description of the bytes in the page

Byte 0	Type of element. 80h - Diskware downloader 81h - Diskware control page 82h - Diskware boot loader 00h - Vector Table 01h - Resident 1xh - Resident overlay x 03h - Self Scan resident 3xh - Self Scan overlay x
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-14	Element dependent.
Byte 15	Checkbyte of the element.
Byte 16	Start of the diskware element data.
Byte n	End of the diskware element data.

4.8 Diskware Downloader

The diskware downloader consists of element header and data. The downloader definition is defined as follows:

Byte	Definition of field
0	Element type (080h).
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Size of the downloader
8-11	Downloader execution address
12-14	Reserved
15	Checkbyte
16	Start of downloader code
n	End of downloader code

Description of the bytes in the diskware downloader.

Byte 0	Element type for the diskware downloader.
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-11	Downloader start of execution address.
Byte 12-14	Reserved.
Byte 15	Checkbyte of the diskware downloader.
Byte 16	Start of the diskware downloader program.
Byte n	End of the diskware downloader program.

4.9 Diskware Control Page

The Diskware control page contains diskware entries. A maximum of twenty entries are available in this page. The diskware control page is 512 bytes long and is defined as follows:

Byte	Definition of field
0	Element Type (81h)
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Length of the page (01h)
8-14	Reserved
15	Checkbyte
16	Element type 0
17-19	Load Address
20	Size
21-22	Cylinder
23-24	Alternate Cylinder
25-26	Starting Sector
27	Element type 1
28-37	Definitions same as bytes 17-26
38	Element type 2
39-48	Definitions same as bytes 17-26
49	Element type 3
50-59	Definitions same as bytes 17-26
60	Element type 4
61-70	Definitions same as bytes 17-26
71	Element type 5
72-81	Definitions same as bytes 17-26
82	Element type 6
83-92	Definitions same as bytes 17-26
93	Element type 7
94-103	Definitions same as bytes 17-26
104	Element type 8
104-114	Definitions same as bytes 17-26
115	Element type 9
116-125	Definitions same as bytes 17-26
n	End of overlay entries (0FFh)
n+1-511	Fill (00h)

Description of the bytes in the page

Byte 0	Element type overlay control page (081h)
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-14	Reserved.
Byte 15	Checkbyte of diskware control page.
Byte 16	Element number definition.
Byte 17-19	Load address is the memory address of the overlay. The load address is three bytes of a four byte address with the least significant byte zero.
Byte 20	Size in 512 sectors
Byte 21-22	Cylinder is where primary copies of the overlay will be stored.
Byte 23-24	Alternate Cylinder is where alternate copies of the overlay will be stored.
Byte 25-26	Starting sector is where the overlay starts.
Byte 27-n	Additional overlay entries.
Byte n+1	End of overlay entries (0FFh marks the end of the entries).
Byte n+2-511	Fill pads out from the End of overlay marker to byte 511.

4.10 Diskware Overlay Entry Data

All the disk parameters for the diskware data are defined in the diskware control page. Each overlay has a element header. The overlay data is defined as follows:

Byte	Definition of field
0	Element Type
1	Product Code
2-4	ROM Version Stamp
5-6	ROM Checksum
7	Size
8-14	Reserved
15	Checkbyte
16	Start of overlay data
n	End of overlay data

Description of the bytes in the page

Byte 0	Element type.
Byte 1	Product code unique to each product.
Byte 2-4	Copy of the ROM version stamp.
Byte 5-6	Copy of the ROM checksum.
Byte 7	Length of this data page in 512 sectors.
Byte 8-14	Reserved.
Byte 15	Checkbyte of the overlay entry data.
Byte 16	Start of the overlay entry data.
Byte n	End of the overlay entry data.

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Chapter 5 Error Correcting Code

5.1 ASIC ECC Comparison

Sirocco RAION	Vs	Fireball LEO
• 8 bits per symbol		Same
• 3 interleaves		Same
• 6 redundancy bytes per interleave		4 redundancy bytes per interleave.
• 2 cross-check bytes		Same
• 18 ECC bytes and 2 CRC bytes		12 ECC bytes and 2 CRC bytes
• Single-Error Correction:		Same
• Double-Error Correction on the fly		Not on the fly
• Triple-Error Correction		Not available
• 3 Bytes CRC per ID field		Same

5.2 Reed Solomon Generator Polynomial in RAION ASIC

5.2.1 ECC Polynomial

The ECC polynomial is defined as follows:

$$G(X) = X^6 + \alpha^{169} X^5 + \alpha^{179} X^4 + \alpha^{25} X^3 + \alpha^{184} X^2 + \alpha^{179} X + \alpha^{15}$$

$$= (X + 1)(X + \alpha^1)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4)(X + \alpha^5)$$

5.2.2 Cross Check Polynomial

The Cross - Check Polynomial is defined as follows:

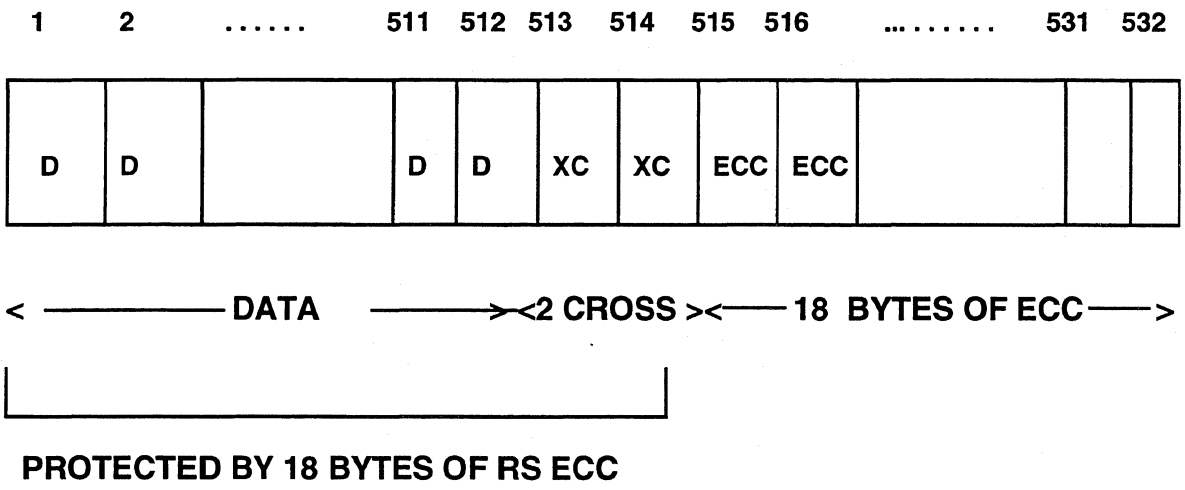
$$XC(X) = X^2 + \alpha^{143} X + 1$$
$$= (X + \alpha^{127})(X + \alpha^{128})$$

5.2.3 CRC Polynomial

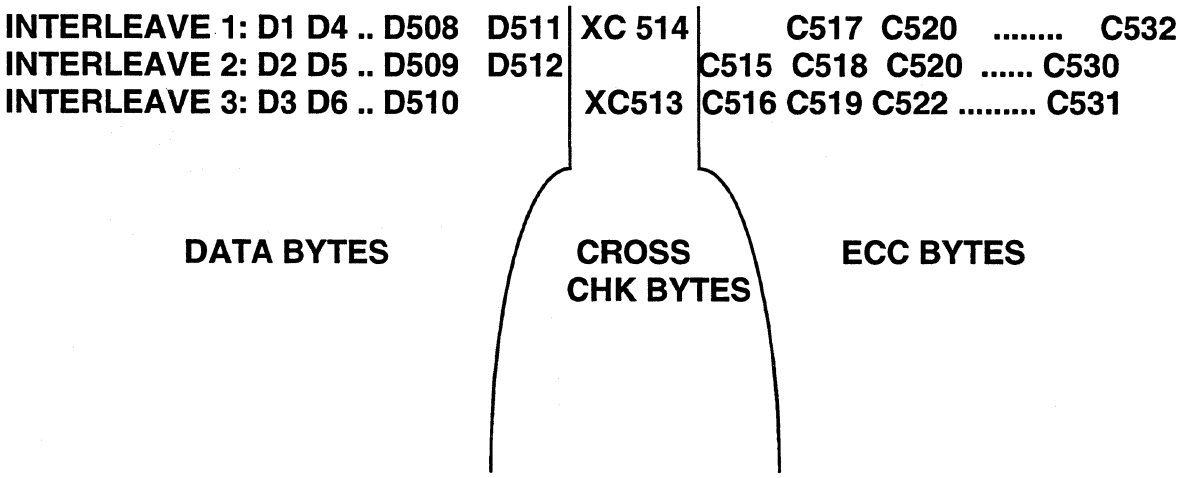
$$CRC(X) = X^3 + \alpha^{203} X^2 + \alpha^{203} X + 1$$
$$= (X + \alpha^{-1})(X + \alpha^0)(X + \alpha^1)$$

5.3 RAION ASIC

5.3.1 1 Sector Data Field with ECC Bytes



5.3.2 Bytes Interleaving



5.4 ECC Principles of Operation

- ECC hardware includes REED-SOLOMON (RS) Encoder/Decoder circuit that is used to generate redundancies during write mode and syndromes during read mode.
- ECC hardware also checks the values of the syndromes to detect errors.
- All corrections will be done in Firmware.

5.5 Cross Check Bytes

- There are 2 cross check bytes per data filed.
- Used to " Double Check" the main correction, and therefore reduced the miscorrection probability of the REED-SOLOMON (RS) ECC correction.

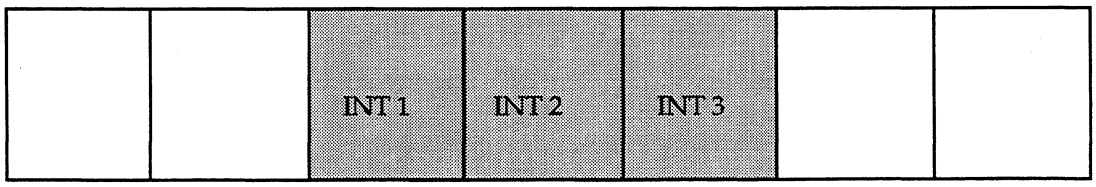
5.6 ECC Correction On - the - Fly

- The expression "On - the - Fly" means an error correction process which is carried out with minimized data flow interruption, and which does not requires one or more disk rotation latencies (revolutions) for carrying out the correction process.
- In order to perform ECC "On - the Fly", it is necessary to detect and correct the data errors in the background while the sequencer is still active, so that is does not stop the flow of data block during a typical transfer of multiple blocks.

5.7 Single Burst Error

- Single burst error is defined as an error occurring in one byte within one of the interleaves.
- Can have up to three erroneous bytes within a sector, provided that each byte of the three occupies a different interleave.
- Correct up to 24 bits I.E., 1 byte per interleave. Guarantee to correct 17 bits.

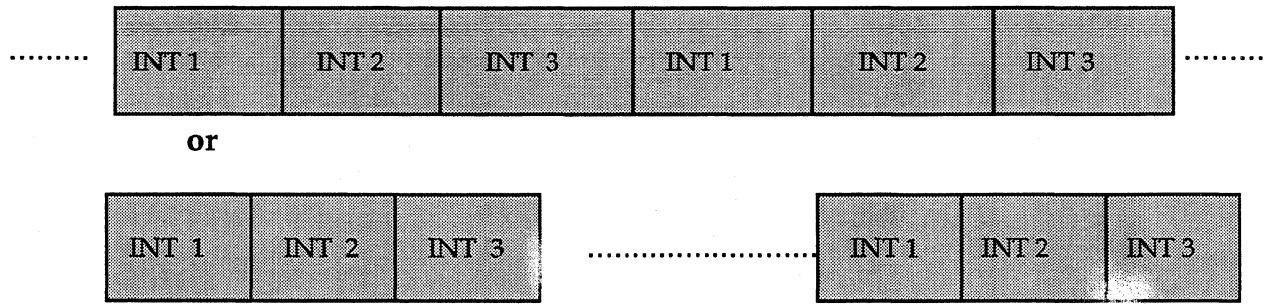
5.7.1 Correctable of 24 Bit Single Burst Error



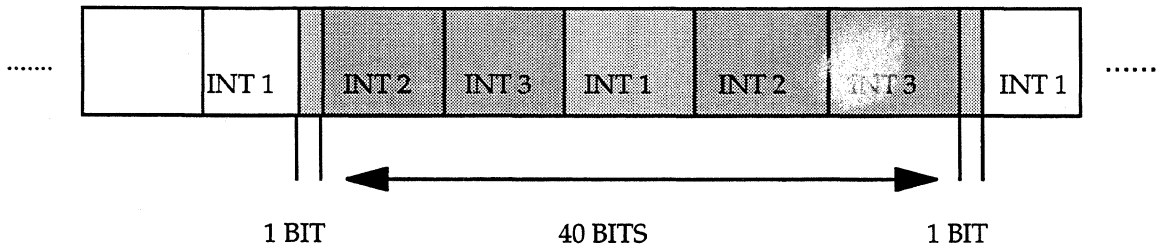
5.8 Double Burst Error

- A double burst error is defined as an error occurring in two bytes within one of the interleaves.
- Correctable double burst errors must have two or fewer erroneous bytes per interleaves.
- Correct up to 48 bits I.E., 2 bytes per interleave. Guarantee to correct 41 bits.

5.8.1 Correctable 48 Bit of Double Burst Error



5.8.2 Uncorrectable (On - the -Fly) 42 Bit of Double Burst Error

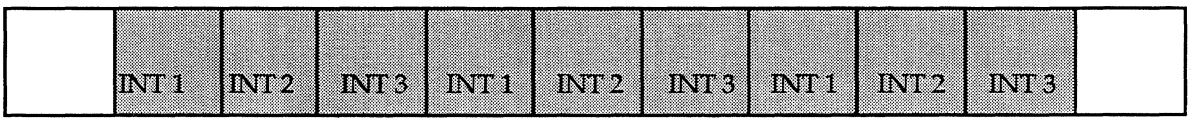


Note :
The 42 bit error is uncorrectable, while the other two 48 bit errors are correctable. The reason for the 42 bit error is uncorrectable is that occupies two interleave 2S, and two interleave 3S, but occupies three interleave 1S, where as the limit is two bytes per interleave. This 42 bit error can be corrected if the drive rereads the sector and applies triple burst error correction techniques.

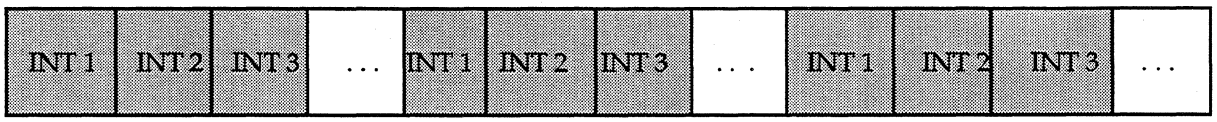
5.9 Triple Burst Error

- Triple burst error is defined as an error occurring in three bytes within one of the interleaves.
- Correctable triple burst errors must have three or fewer erroneous bytes per interleaves.
- Correct up to 72 bits I.E., 3 bytes per interleave. Guarantee to correct 65 bits.

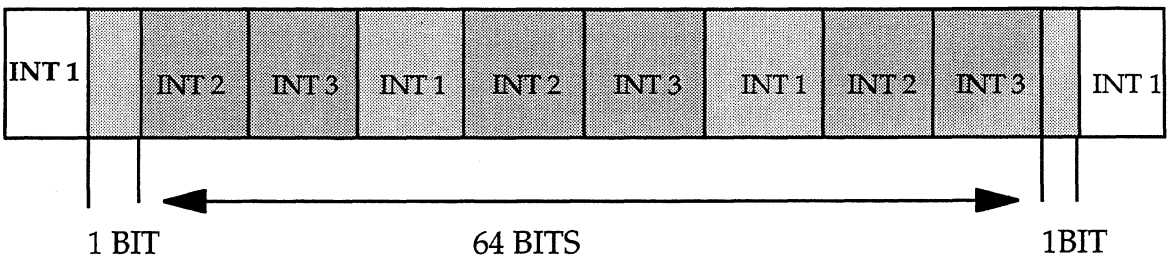
5.9.1 Correctable 72 Bit of Triple Burst Error



or



5.9.2 Uncorrectable 72 Bit of Triple Burst Error



5.10 Multiple Random Burst Errors

- Can correct up to 72 bits of multiple random errors, provided that the bytes in error follow the guidelines for correctable triple burst errors. Up to 48 bits of multiple random errors can be corrected On- the -Fly if two or fewer bytes per interleave.

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Chapter 6 Miscellaneous Information

6.1 Programmable Trigger

Firmware allows certain conditions to generate a scope trigger. The conditions under which a trigger pulse is generated is controlled by Configuration Page 12 which consists of one byte. The eight bits are used to control whether a pulse is to be generated on an associated condition. If the bit is set and the condition occurs, a 1 microsecond (approximately) pulse is generated. Multiple trigger conditions may be specified at a time. The supported bits and associated conditions are as follows:

Bit	Description
0	---
1	Seek time out
2	Seek fault
3	---
4	ECC error
5	Sequencer read/write error
6	Sequencer overrun/underrun
7	Sequencer time out

As an example, to enable a pulse on either a seek time-out or ECC error, enter the following DIAG command line: DEPB 0 18 , WRCONF 12

The programmable scope trigger magically appears on microprocessor port P0.7.

6.2 Drive Parameter Analysis

Drive Parameter Analysis (DPA) feature has been implemented on Sirocco AT drives. The DPA feature can be turned on by setting bit 7 byte 1 of config page 19 to one. Once the DPA feature is turned on the user can send **dpa enable** command to start monitoring some parameters of the Sirocco AT drive.

A set of two sectors (89, 90) have been reserved on Cylinder -2 and -3 to store DPA related data and variables. Sector 89 to store DPA related variables and sector 90 is used to store Warranty Threshold Values.

An opcode B0H has been defined for DPA related commands. This command has a number of separate functions which are selectable by a subopcode via the Features Register. The drive checks a specific password in Cylinder Low & High Registers before it accepts a DPA Command as valid.

Password for a valid DPA Command is:

0x4F	Cylinder Low
0xC2	Cylinder High
0xB0	Command Opcode

The Sirocco drive supports following DPA commands:

DPA Subcode	Function
0xD0	Returns Drive Attribute Values. The drive returns 512 bytes and saves the attributes to disk (sector 89 Cylinder -1)
0xD1	Read Warranty Threshold Values. The drive returns 512 bytes of data from Warranty Threshold values sector (sector 90 Cylinder -2, -3)
0xD2	Enable/ Disable Autosave
0xD3	Write Current Attribute Values to the disk (sector 89 Cylinder -2, -3)
0xD7	Write Warranty Threshold values to the disk (sector 90 Cylinder -2, -3)
0xD8	Enable DPA data collection and DPA Command decode
0xD9	Disable DPA data collection and DPA Command decode
0xDA	Check Warranty

6.2.1 Drive Attributes Supported

Attribute ID Number	Attribute Name
1	Read Error Rate
3	Spin Up Time
4	Start/stop Count
5	Reallocated Sector Count (grown defects)
7	Seek Error Rate
9	Power On Hours Count
11	Recal Retry Count
12	Drive Power Cycle Count

6.2.2 Drive Attribute Value Data Structure

The following data structure defines the 512 bytes that make up the Drive Attribute Value information.

Bytes	Drive Attribute Data Structure Description
2	Data Structure Revision Number
12	First of the supported Drive Attributes
12	Second of the supported Drive Attribute
	..
	..
	..
12	30th of the supported Drive Attributes
6	Off - line data collection status byte (Not Supported)
2	Drive Failure Prediction Capability Word **Bit** 0 = Attributes Saved by Drive before Entering Power Mode 1 = Attributes Auto Save Capability
92	Reserved (0x00)
48	Vendor Unique (0x00)
1	Quantum Checksum Byte
1	Data Structure Checksum Byte
Total 512	

The Data Structure Revision Number identifies which version of this data structure is implemented.

Quantum Checksum Byte is calculated so that sum of all bytes in Data Structure is 'C'. The Data Structure Checksum is a simple 8 bit addition of the first 511 bytes in the data structure with the Checksum value being the two's complement of this sum.

6.2.3 Drive Attribute Format

Bytes	Drive Attribute Description
1	Attribute ID Number
2	Status Flags
1	Normalized Attribute Value
1	Worst Ever Normalized Attribute Value
6	Raw Attribute Value
1	Reserved (0x00)
Total 12	

6.2.4 Status Flags

Bit	Description
0	If set to 1, an Attribute value exceeding Threshold constitute a failure
1	If set to 1, the Attribute value is updated during on line testing
2	If set to 1, it's a performance Attribute
3	If set to 1, it's an error rate Attribute
4	If set to 1, it's an event count Attribute
5	If set to 1, it's self preserving Attribute
6	Reserved
7	Reserved
8-15	Reserved

6.2.5 Normalized Attribute Value

Valid numbers are 0x01 - 0xFE

Normalized Value	Description
0x01	Minimum value
0x64	Initial value prior to data collection
0xFE	Maximum value. Data count is saturated. Value not valid

6.2.6 Worst Ever Normalized Attribute Value

Valid numbers are 0x01 - 0xFE

Normalized Value	Description
0x01	Minimum value
0x64	Initial value prior to data collection
0xFE	Maximum value. Data count is saturated. Value not valid

6.3 AT Configuration Command Format

BYTE	BITS								DEFAULT
	7	6	5	4	3	2	1	0	
0-31	QUANTUM CONFIGURATION KEY								
32	RESERVED = 0						PE	CE	03H
33	RESERVED = 0								00H
34	RESERVED = 0								00H
35	RESERVED = 0								00H
36	AWRE	ARRE	N/A	RC	ECC	N/A	N/A	DCR	C0H
37	NUMBER OF RETRIES								08H (1)
38	ECC CORRECTION SPAN								18H (2)
39	RESERVED = 0					WCE	RUEE	0	06H
40-511	RESERVED = 0								00H

KEY:

PE	Prefetch Enable
CE	Cache Enable
AWRE	Automatic Write Reallocation Enable
ARRE	Automatic Read Reallocation Enable
RC	Read Continuous
ECC	Enable Early Correction
DCR	Disable Correction
WCE	Write Cache Enable
RUEE	Reallocation Uncorrectable Error Enable

COMMENTS:
1. This number reflects number of times through group retry sequence.
2. Triple burst correction and double burst on the fly enabled.

6.4 Configuration Pages

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 0	0	0	Customer no.		1	1	0
Pg 1	0	1	Jumper setting		2	2	0
Pg 2	0	15	Vendor name	16 bytes ASCII characters	16	16	"QUANTUM "
Pg 3	0	15	Product ID	16 bytes ASCII characters—model dependent	16	16	"SIROCCO_1700 " or "SIROCCO_2100 " or "SIROCCO_2550 "
Pg 4	0	7	Drive Revision Level	where I = interface (A/S) rr = rom rev dd = diskware rev c = fmt/conf rev s = selfscan rev	8	8	Current version (Irr.ddcs)
Pg 5	0	11	Drive Serial No.	12 bytes of drive serial # in ASCII	12	12	—
Pg 6	0	31	Customer Name	32 bytes customer name in ASCII	32	32	"GENERIC"
Pg 7	0	0	AT Config. Bit 0 - ID_Permanent Bit 1 - DASP_SPIKE Bit 2 - DIS_WIGGLE_RTY Bit 3 - CACHE_DEGUG Bit 4 - COMMAND_HISTORY Bit 5 - AUTO_ARM_CONFIG Bit 6 - AUTO_RD_CONFIG Bit 7 - IDLE_PWR_DN_ENABLE	Misc1 0-ret.log. CHS always; 1-ret. cur.log. CHS Silent (Stealth) servo Silent (Stealth) servo Cache debug info saved by cmd hist Save command history Auto Arm config. set Auto Read config. set 0-enter stdby mode when timeout occurs	1	16	60H

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 7	1	1		Misc 2	1		40H
			Bit 0 - ID_528MB_ def	0-don't limit def. chs in ID data to 528MB			
			Bit 1 - SEEK_WITH_OFF SET	0-clear POS_OFFS w/every seek			
			Bit 2 - SEEK_W/_OFFSE T_MASK				
			Bit 3 - NO_CALCULATE _MJ	0-don't calc. microjog automatically			
			Bit 4 - IOR_DELAY 0	Salty IV usage			
			Bit 5 - IOR_DELAY 1	Salty IV usage			
			Bit 6 - DMA_MODE_0	1-DMA mode 1 enable			
			Bit 7 - DMA_MODE_1	1-DMA mode 2 enable			
	2	3		Logical cylinders/drive	2		1056
	4	4		Logical heads/cylinder	1		16
	5	5		Logical sectors/track	1		63
	6	6		Minimum power time	1		0
	7	7		Transfer read delay	1		50
	8	8		Transfer write delay	1		50
	9	9	TA_RECOV_PAR MS	TA enable/disable	1		7H
			TAR	Bit 0-enable/disable TA recovery			
			AMR	Bit 1-enable Address Mark recovery			
			IDRR	Bit 2 -enable ID recovery on Read			
			IDRW	Bit 3 -enable ID recovery on Write			
	10	14		Reserve bytes for future	5		0
	15	15	Page revision number		1		0
Pg 8	0	0	Number of heads	Model dependent	1	1	2/4/6
Pg 9	0	15	Configuration validation	0, 1, FF,2,FE,3,FD,4,FC,5, FB,6,FA,7,F9,8	16	16	<---
Pg 10			Non Adaptive Zone Table				
	0	1	starting cylinder		2	555	0
	2	5	Starting logical sector address		4		xxxx
	6	6	Sectors per track	138 sect/track for Z0, system	1		8A

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 10	7	8	Sectors per zone		3		xxxx
	9	9	Track /head skew		1		0
	10	10	Cylinder skew				0
	11	11	Z0_10	M value for clock synthesizer	1		5D
	12	12	Z0_11	N value for clock synthesizer	1		1D
	13	13	Z0_12	Clock synthesizer loop res/multiplier	1		E4
	14	14	Z0_16	Slow_PD/TRIMT	1		7
	15	15	Z0_17	Servo Continuous Filter Cutoff Freq	1		5
	16	16	Z0_19	Tune	1		9
	17	17	Z0_1A	TWAI/TWAO	1		5
	18	18	Z0_1B	8 LSBs flash digitizer output latch counter	1		0
	19	19	Z0_1D	AGC internal capacitor	1		BF
	20	20	Z0_1E	Servo Control	1		3F
	21	21	Z0_21	TST1/TST2 output port select	1		40
	22	22	Z0_23	Frequency	1		80
	23	23	Z0_26	Quality Monitor Control	1		A7
	24	24	Z0_27	ENDEC Control	1		E0
	25	25	Z0_28	ENDEC Control	1		7
	26	26	Z0_29	RD/WR Gate Logic/Extended WR gate	1		21
	27	27	Z0_2A	Power Mode Select	1		80
	28	28	Z0_2D	Read Path test	1		0
	29	29	Z0_2E	Digital Test	1		0
	30	30	Z0_2F	Test Mode Select	1		0
	31	31	Z0_36	TWA/SYNFREE	1		30
	32	32	Z0_38	TA CNTRL: Thermal Asperity Control	1		30
	33	33	Z0_39	TA-FAM: Force AM after TA Time	1		5E
			Zone				
	34	67	1	Same as 0-33	34		
	68	101	2	Same as 0-33	34		
	102	135	3	Same as 0-33	34		
	136	169	4	Same as 0-33	34		
	170	203	5	Same as 0-33	34		
	204	237	6	Same as 0-33	34		
	238	271	7	Same as 0-33	34		
	272	305	8	Same as 0-33	34		
	306	339	9	Same as 0-33	34		
	340	373	10	Same as 0-33	34		

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 10	374	407	11	Same as 0-33	34		
	408	441	12	Same as 0-33	34		
	442	475	13	Same as 0-33	34		
	476	509	14	Same as 0-33	34		
	510	543	15	Same as 0-33	34		
	544	545	Maximum Cylinder	Data Cylinders=0 ... 5899	2		170C
	546	549	Maximum Logical Sector Address		4		
		550	Head (track) wedge skew	Set to 45	1		2D
		551	Cylinder wedge skew	Set to 45	1		2D
		552	Number of Zones	N=16	1		10H
		553	Wedges Per Track	W=90	1		5A
		554	Page Revision Number		1		F7
Pg 11	0	3	Number of User Accessable Sectors	# of user accessible sector at ROM default #NAME?	4	4	0FFH, 0FFH, 0FFH, 0FFH
Pg 12	0	0	Trigger Msk	0 - true bump 1 - seek timeout 2 - servo fault 3 - TNA error 4 - ecc error 5 - sequencer r/w error 6 - sequencer underrun/overrun 7 - sequencer timeout	1	1	0
Pg 13	0	1	Drive family and Model	Family = 16H, Model = 2, 4, 6 (heads)	2	2	16H, 2 or 16H, 4 or 16H, 6
Pg 14	0	5	HW head map	Hardware head map, user head map	6	6	03H,0,0, 03H,0,0 or 0FH,0,0, 0FH,0,0 or 3FH,0,0 3FH,0,0
Pg 15			Diskware Overlay				
	0	0	overlay number: 0	Vector table	1	167	
	1	3	RAM load address		3		
	4	4	Size in sectors		1		
	5	6	Cylinder		2		
	7	8	Alternate cylinder		2		
	9	10	Sector		2		
	11	21	Overlay 1	F/W Resident overlay	11		
	22	32	Overlay 2	F/W Overlay 0	11		
	33	43	Overlay 3	F/W Overlay 1	11		
	44	54	Overlay 4	F/W Overlay 2	11		

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 15	55	65	Overlay 5	F/W Overlay 3	11		
	66	76	Overlay 6	F/W Overlay 4	11		
	77	87	Overlay 7	F/W Overlay 5	11		
	88	98	Overlay 8	Reserved	11		
	99	109	Overlay 9	Reserved	11		
	110	120	Overlay 10	Reserved	11		
	121	131	Overlay 11	Reserved	11		
	132	142	Overlay 12	Reserved	11		
	143	153	Overlay 13	Reserved	11		
	154	164	Overlay 14	Reserved	11		
	165	165	End of list pad		1		FFH
	166	166	Page rev. no.		1		
Pg 16	0	1	HDA control Flags	0 - no_spin_down 1 - rcal_on_fatal_err 2 - not used 3 - kill_low_pwr 4 - enable_active_brake 5 - not used 6 - rd_on_arrival 7 - not used	2	2	68H
Pg 17			Adaptive Zone Table				
	0	0	Z0_HD0_00	DC Tap	1	2689	077 (Adaptive)
	1	1	Z0_HD0_01	TAP 1	1		4F
	2	2	Z0_HD0_02J	TAP 2	1		BB
	3	3	Z0_HD0_03	TAP 4	1		F9
	4	4	Z0_HD0_04	TAP 5	1		55
	5	5	Z0_HD0_05	TAP 6	1		BA
	6	6	Z0_HD0_06	TAP 7	1		39
	7	7	Z0_HD0_07	TAP 8	1		80
	8	8	Z0_HD0_08	TAP 9	1		80
	9	9	Z0_HD0_09	TAP 10	1		5B
	10	10	Z0_HD0_0A	DFE TAP 1	1		80
	11	11	Z0_HD0_0F	VGA	1		81
	12	12	Z0_HD0_13	Read Continuous Filter Cutoff Freq	1		64
	13	13	Z0_HD0_14	Read Continuous Filter Zero Freq	1		8E
	14	14	Z0_HD0_15	ACC/ATT	1		78
	15	15	Z0_HD0_18	Servo Zero Frequency	1		6F
	16	16	Z0_HD0_1F	Servo Amplitude	1		27
	17	17	Z0_HD0_20	Write Precomp	1		89
	18	18	Z0_HD0_22	GUG/TDFEOFF/TWUG	1		CB
	19	19	Z0_HD0_24	FUG/PHUG	1		2E
	20	20	Z0_HD0_30	Leading DFE control	1		0
	21	21	Z0_HD0_35	Leading DFE Delay/Trailing DFE Delay	1		0

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 17	22	22	Z0_HD0_37	MR ID AC	1		72
	23	23	Z0_HD0_3A	MR Non-linearity COMP	1		0
	24	24	Z0_HD0_MTI	MR/TF Currents (NOT SHIVA PROG) MR Bias, upper 4 bits TF Wrl, lower 2 bits	1		62
	25	25	Z0_HD0_MJ0	Micro-jog, lower byte	1		8D
	26	26	Z0_HD0_MJ1	Micro-jog , upper byte	1		FD
	27	27	Z0_HD0_DV	Dummy variable, reserve byte	1		0
			Head				
	28	55	HD1	Same as 0 - 27	28		
	56	83	HD2	Same as 0 - 27	28		
	84	111	HD3	Same as 0 - 27	28		
	112	139	HD4	Same as 0 - 27	28		
	140	167	HD5	Same as 0 - 27	28		
			Zone				
	168	335	1	Same as 0 - 167	168		
	336	503	2	Same as 0 - 167	168		
	504	671	3	Same as 0 - 167	168		
	672	839	4	Same as 0 - 167	168		
	840	1007	5	Same as 0 - 167	168		
	1008	1175	6	Same as 0 - 167	168		
	1176	1343	7	Same as 0 - 167	168		
	1344	1511	8	Same as 0 - 167	168		
	1512	1679	9	Same as 0 - 167	168		
	1680	1847	10	Same as 0 - 167	168		
	1848	2015	11	Same as 0 - 167	168		
	2016	2183	12	Same as 0 - 167	168		
	2184	2351	13	Same as 0 - 167	168		
	2351	2519	14	Same as 0 - 167	168		
	2520	2687	15	Same as 0 - 167	168		
		2688	Page rev. no.		1		F7
Pg 18	0	381	Non Adaptive Servo		382	382	
Pg 19			DPA Page				0
	0	0	DPA Master Switch	bit 7 =1/0=Enable/Disable	1	18	0
	1	1	EL_PERIOD	Auto update period	1		0
	2	5	SEEK_DR	Max. # of seeks/data range	4		FFFFFFFF
	6	7	MAX_SK_ERROR _DR	Max. # of seek errors/data range	1		FF
	8	11	READ_DR	Max. # of sectors read/data range	4		FFFFFFFF
	12	12	MAX_RD_ERROR _DR	Max. # of read errors/data range	1		FF

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 19	13	14	SPINUP_DR	Max. # of spinup/data range	2		FFFF
	12	12	MAX_RD_ERROR _DR	Max. # of read errors/data range	1		FF
	13	14	SPINUP_DR	Max. # of spinup/data range	2		FFFF
	15	16	MAX_SPIN-UP_DR	Maximum spinup time	2		FFFF
	17	17	RECAL_DR	Max. # of recal/data range	1		FF
	18	18	Page Revision Number		1		0
Pg 20	0	0	Not Used		1	1	0
Pg 21			Servo Variables				
	0	1151		1152 bytes used for Adaptive Servo variables	1152	1153	TBD
	1152	1152	Page rev. no.		1		
Pg 22			E2PROM				
	0	0		Not Used	1	1	0
Pg 23			MICRO-JOG				
	0	0	Z0_HD0_VGA	Amplitude	1	84	0 (Adaptive)
	1	1	Z0_HD0_MSE	BER	1		0
	2	3	Z0_HD0_MJ	Microjog value	2		FD8DH
	4	4	Z0_HD1_VGA	Amplitude	1		0
	5	5	Z0_HD1_MSE	BER	1		0
	6	7	Z0_HD1_MJ	Microjog value	2		FD8DH
	8	8	Z0_HD2_VGA	Amplitude	1		0
	9	9	Z0_HD2_MSE	BER	1		0
	10	11	Z0_HD2_MJ	Microjog value	2		FD8DH
	12	12	Z0_HD3_VGA	Amplitude	1		0
	13	13	Z0_HD3_MSE	BER	1		0
	14	15	Z0_HD3_MJ	Microjog value	2		FD8DH
	16	16	Z0_HD4_VGA	Amplitude	1		0
	17	17	Z0_HD4_MSE	BER	1		0
	18	19	Z0_HD4_MJ	Microjog value	2		FD8DH
	20	20	Z0_HD5_VGA	Amplitude	1		0
	21	21	Z0_HD5_MSE	BER	1		0
	22	23	Z0_HD5_MJ	Microjog value	2		FD8DH
	24	24	Z15_HD0_VGA	Amplitude	1		0
	25	25	Z15_HD0_MSE	BER	1		0
	26	27	Z15_HD0_MJ	Microjog value	2		01ECH
	28	28	Z15_HD1_VGA	Amplitude	1		0
	29	29	Z15_HD1_MSE	BER	1		0
	30	31	Z15_HD1_MJ	Microjog value	2		01ECH
	32	32	Z15_HD2_VGA	Amplitude	1		0
	33	33	Z15_HD2_MSE	BER	1		0
	34	35	Z15_HD2_MJ	Microjog value	2		01ECH

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 23	36	36	Z15_HD3_VGA	Amplitude	1		0
	37	37	Z15_HD3_MSE	BER	1		0
	38	39	Z15_HD3_MJ	Microjog value	2		01ECH
	40	40	Z15_HD4_VGA	Amplitude	1		0
	41	41	Z15_HD4_MSE	BER	1		0
	42	43	Z15_HD4_MJ	Microjog value	2		01ECH
	44	44	Z15_HD5_VGA	Amplitude	1		0
	45	45	Z15_HD5_MSE	BER	1		0
	46	47	Z15_HD5_MJ	Microjog value	2		01ECH
	48	49	HD0_SLOPE	Microjog Slope	2		31A3H
	50	51	HD1_SLOPE	Microjog Slope	2		31A3H
	52	53	HD2_SLOPE	Microjog Slope	2		31A3H
	54	55	HD3_SLOPE	Microjog Slope	2		31A3H
	56	57	HD4_SLOPE	Microjog Slope	2		31A3H
	58	59	HD5_SLOPE	Microjog Slope	2		31A3H
	60	61	Z0_HD0_MJ	Servo Odd/Even Microjog Center	2		0
	62	63	Z0-HD1_MJ	Servo Odd/Even Microjog Center	2		0
	64	65	Z0-HD2_MJ	Servo Odd/Even Microjog Center	2		0
	66	67	Z0-HD3_MJ	Servo Odd/Even Microjog Center	2		0
	68	69	Z0-HD4_MJ	Servo Odd/Even Microjog Center	2		0
	70	71	Z0-HD5_MJ	Servo Odd/Even Microjog Center	2		0
	72	73	Z15_HD0_MJ	Servo Odd/Even Microjog Center	2		0
	74	75	Z15_HD1_MJ	Servo Odd/Even Microjog Center	2		0
	76	77	Z15_HD2_MJ	Servo Odd/Even Microjog Center	2		0
	78	79	Z15_HD3_MJ	Servo Odd/Even Microjog Center	2		0
	80	81	Z15_HD4_MJ	Servo Odd/Even Microjog Center	2		0
	82	83	Z15_HD5_MJ	Servo Odd/Even Microjog Center	2		0
Pg 24			Identify Drive Page				
	0	1	Word 0- General Config bit sig.	Parameters for AT identify Drive command	2	138	5A04H
	2	3	Word 1-Space hldr(log. cyls)	Note that all bytes are in reversed order	2		0
	4	5	Word 2-Reserved		2		0
	6	7	Word 3-Space hldr(log. hds)		2		0

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 24	8	9	Word 4-Space hldr(Unfmt'd bytes/trk)	Unformatted Bytes/Track	2		0
	10	11	Word 5-Number Unfmt'd bytes/trk)		2		0002H
	12	13	Word 6-Space hldr	Sectors/Track	2		0
	14	15	Word 7-Vendor unique		2		0
	16	17	Word 8-Vendor unique		2		0
	18	19	Word 9-letters 'QT' in reversed order		2		5451H
	20	21	Word 10-Space hldr Serial Number		2		0
	22	23	Word 11-Space hldr Serial Number		2		0
	24	25	Word 12-Space hldr Serial Number		2		0
	26	27	Word 13-Space hldr Serial Number		2		0
	28	29	Word 14-Space hldr Serial Number		2		0
	30	31	Word 15-Space hldr Serial Number		2		0
	32	33	Word 16-Space hldr Serial Number		2		0
	34	35	Word 17-Space hldr Serial Number		2		0
	36	37	Word 18-Space hldr Serial Number		2		0
	38	39	Word 19-Space hldr Serial Number		2		0
	40	41	Word 20-Buffer type-Dual type		2		0300H
	42	43	Word 21-Space hldr (Buffer size)	512 bytes increments	2		0
	44	45	Word 22- #of ECC bytes on RD/WR lng		2		0400H
	46	47	Word 23-26-Space hldr- F/w rev		2		0
	48	49	Word 24 - Space hldr		2		0
	50	51	Word 25 - Space hldr		2		0
	52	53	Word 26 - Space hldr		2		0
	54	55	Word 27-46 Blank Char.		2		2020H

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 24	56	57	Word 28-Blank Char.		2		2020H
	58	59	Word 29-Blank Char.		2		2020H
	60	61	Word 30-Blank Char.		2		2020H
	62	63	Word 31-Blank Char.		2		2020H
	64	65	Word 32-Blank Char.		2		2020H
	66	67	Word 33-Blank Char.		2		2020H
	68	69	Word 34-Blank Char.		2		2020H
	70	71	Word 35-Blank Char.		2		2020H
	72	73	Word 36-Blank Char.		2		2020H
	74	75	Word 37-Blank Char.		2		2020H
	76	77	Word 38-Blank Char.		2		2020H
	78	79	Word 39-Blank Char.		2		2020H
	80	81	Word 40-Blank Char.		2		2020H
	82	83	Word 41-Blank Char.		2		2020H
	84	85	Word 42-Blank Char.		2		2020H
	86	87	Word 43-Blank Char.		2		2020H
	88	89	Word 44-Blank Char.		2		2020H
	90	91	Word 45-Blank Char.		2		2020H
	92	93	Word 46-Blank Char.		2		2020H
	94	95	Word 47-Vendor unique	Max. sectors on RD/WR Multi. sectors	2		0880H
	96	97	Word 48-Can/Can't perform dble wrd I/O		2		0
	98	99	Word 49- Drive Capability	(DMA, LBA and IORDY)	2		000FH
	100	101	Word 50- Reserved		2		0
	102	103	Word 51- PIO data transfer cycle time	Bits 7-0 - Mode 2	2		0002H

Page	From byte	To byte	Function	Description	Bytes	Length	Default
Pg 24	104	105	Word 52- DMA data transfer cycle time	Bits 7-0 - Mode 2	2		0002H
	106	107	Word 53- Fields valid	set if word 54-58 & 64-70 are valid	2		0300H
	108	109	Word 54- Space hldr	Number of current cylinders	2		0
	110	111	Word 55- Space hldr	Number of current heads	2		0
	112	113	Word 56- Space hldr	Number of current sectors	2		0
	114	115	Word 57- Space hldr	Current capacity in sectors	2		0
	116	117	Word 58- Space hldr		2		0
	118	119	Word 59- Space hldr	bit 8- Multiple sector setting valid bit 7-0 - Cur. set. of #of sectors per RD/WR multi.	2		0
	120	121	Word 60- Space hldr	Number of user addressable sectors (LBA)	2		0
	122	123	Word 61- Space hldr		2		0
	124	125	Word 62- Single word DMA Xfer mode	Active/Supported	2		0704H
	126	127	Word 63- Multiple word DMA Xfer mode	Active/Supported	2		0704H
	128	129	Word 64- (15-8)Reserved/ (7-0) Advance PIO Mode		2		0300H
	130	131	Word 65- Min. Multi-word DMA	Xfer cycle time per word (120 ns)	2		07800H
	132	133	Word 66- MFG's recommended multi-word DMA	Xfer cycle time (120 ns)	2		07800H
	134	135	Word 67- Min. PIO Xfer cycle time	w/o IORDY flow control (333 ns)	2		04D01H
	136	137	Word 68- Min. PIO Xfer cycle time	w/IORDY flow control (120 ns)	2		07800H

6.5 Firmware Error Code

Value	Error Name	Description
Hex		
00h	EC_NO_ERROR	No Error detected at Drive level
Startup errors		
01h	EC_BAD_OVERLAY	Medium error, all overlay copies was bad or due to uncorrectable
02h	EC_READ_DISKWARE	Error during reading of diskware
03h	EC_BUFFER_RAM	Ram error (most likely found in a diagnostic)
04h	EC_ROM_CHKSUM	Internal ROM checksum error.
05h	EC_RES_CHKSUM	Marker for resident code chechsum
06h	EC_ROM_RES_VERSION	Marker for ROM and resident code are incompatable.
07h	EC_ROM_OVR_VERSION	Marker for ROM and overlay are incompatable
08h	EC_OVL_CHKSUM	Marker for overlay check sum.
09h	EC_VT_CHKSUM	Marker for diskware vector table checksum
0Ah	EC_ROM_VT_VERSION	ROM and vector table versions are incompatable
0Bh	EC_SEQ_RAM_FAIL	Failure in writing to sequencer format table
0Ch	EC_SEQ_ROLLOVER	Sequencer rollover register failure
Command errors		
0Dh	EC_REC_BAD_FORMAT	Requested format in Read Defect Data not available
0Eh	EC_INV_COMMAND	Invalid command
0Fh	EC_INV_LBA	Invalid LBA
10h	EC_INV_CDB	Invalid bits set in CDB
11h	EC_INV_PARAMETER	Invalid fields in parameters
12h	EC_INVALID_HEAD	Invalid head specified
13h	EC_INVALID_CYL	Invalid cylinder specified
14h	EC_INVALID_SECTOR	Invalid sector specified
15h	EC_BAD_MODE_PAGE	Some param(s) in the mode pages found to be bad during init
16h	CMD_NOT_USED_1	
17h	CMD_NOT_USED_2	
18h	CMD_NOT_USED_3	
19h	CMD_NOT_USED_4	
System errors		
1Ah	EC_BAD_DFCT_LIST	Bad defect list
1Bh	EC_DFCT_LIST_FULL	Defect list is full
1Ch	EC_NO_ALT_SECTS	No more alternate sectors available
1Dh	EC_WRITE_SYSTEM	Error in writing to system sector
1Eh	EC_READ_SYSTEM	Error in reading from a system sector
1Fh	EC_ASSERT_ERROR	Logical assertion (firmware consistency check) error
20h	EC_RESET_OCCURRED	Reset occurred
21h	EC_SCSI_PARITY	SCSI bus parity error
22h	EC_BAD_ASICS	Cannot set register in controller chip
23h	SYS_NOT_USED_1	
24h	SYS_NOT_USED_2	
25h	SYS_NOT_USED_3	
Data/Read/Write errors		
26h	EC_ON_FLY_CORRECTED	Correctable data field via on the fly algorithm
27h	EC_REC_DATA_EQUAL	Data error recovered via ECC w/ 2 consecutive = syndromes
28h	EC_REC_DATA_LAST	Data error recovered via ECC on last retry
29h	EC_WRITE_FAULT	Write fault
2Ah		Recovered Write fault
2Bh	EC_WG_IN_WEDGE	Write gate still asserted when wedge detected

Value	Error Name	Description
2Bh	EC_WG_IN_WEDGE	Write gate still asserted when wedge detected
2Ch		Recovered - Write gate still asserted when wedge detected
2Dh	EC_DATA_ECC	Uncorrectable data field ECC error
2Eh		Recovered - Uncorrectable data field ECC error
2Fh	EC_CRC_CONT	Marker for CRC/Continue
30h		Recovered - Marker for CRC/Continue
31h	EC_ID_SYNC_TMO	AM mark not found for ID field
32h		Recovered - AM mark not found for ID field
33h	EC_ID_AM_CONT	AM mark not found for ID field with internal continue
34h		Recovered - AM mark not found for ID field with internal continue.
35h	EC_DATA_SYNC_TMO	Data field sync time-out
36h		Recovered - Data field sync time-out
37h	EC_NO_RECORD_FOUND	No record found
38h		Recovered - No record found
39h	EC_WUS_WRITE_FLT	WUS Write fault (bump)
3Ah		Recovered - WUS Write fault (bump)
3Bh	EC_UNXPCTD_SEQ_ERR	Unexpected sequencer error
3Ch		Recovered - Unexpected sequencer error
3Dh	EC_ID_MISCOMP	Latched ID miscompare
3Eh		Recovered - Latched ID miscompare
3Fh	EC_SEQ_TIMEOUT	Sequencer time-out
40h		Recovered - Sequencer time-out
41h	EC_UNDERRUN	Underrun error
42h		Recovered - Underrun error
43h	EC_INVALID_DATA	Data read was written after reallocation of uncorrectable data
44h		Recovered - reallocation
45h	RW_NOT_USED_1	
46h	RW_NOT_USED_2	
Servo errors		
47h	EC_RECALING	Drive is up to speed and recalibrating
48h	EC_STOPPED	Drive has not been told to spin up
49h	EC_FMT_FAILURE	Track format is invalid during PES measurement
4Ah	EC_BAD_SYNC	Bad Servo Sync
4Bh		Recovered - Bad Servo Sync
4Ch	EC_BAD_SAM	Bad Servo Address Mark
4Dh		Recovered - Bad Servo Address Mark.
4Eh	EC_BAD_DATA	Bad Track Number Data (Gray Code Error)
4Fh		Recovered - Bad Track Number Data (Gray Code Error)
50h	EC_SERVO_DEFECT	Servo Defect (Bad Servo Sample)
51h		Recovered - Servo Defect (Bad Servo Sample)
52h	EC_BUMPED	Bump Detected
53h		Recovered - Bump Detected
54h	EC_OFF_TRACK	While on-track, Gray code track # does not match desired trk
55h		Recovered - While on-track, Gray code track # does not match desired trk
56h	EC_LOST_LOCK	Fatal Servo Error: Multiple bad Sync/SAM during SETTLE/ON_TRK
57h		Recovered - Fatal Servo Error: Multiple bad Sync/SAM during SETTLE/ON_TRK
58h	EC_OVRSAMPL_SVO	Failure to enter servo oversampling mode

Value	Error Name	Description
59h	EC_MISS_SVO_INT_0	Fatal Servo Error: Missing Servo Interrupts Without Mask
5Ah	EC_MISS_SVO_INT_1	Fatal Servo Error: Missing Servo Interrupts With Mask
5Bh	EC_BAD_HEAD_SELECT	Head read from ID not equal to selected head
5Ch	EC_OUT_SPEED	Speed is out of range
5Dh		Recovered - Speed is out of range
5Eh	SVO_NOT_USED_1	
5Fh	SVO_NOT_USED_2	
60h	SVO_NOT_USED_3	
61h	SVO_NOT_USED_4	
Seek errors		
62h	EC_SEEK_ERROR	Seek error
63h		Recovered - Seek error
64h	EC_SEEK_ERR_NO_RTY	Seek error
65h		Recovered - Seek error
66h	EC_SEEK_TIMEOUT	Seek time-out with no servo fault
67h		Recovered - Seek time-out with no servo fault
68h	SK_NOT_USED_1	
69h	SK_NOT_USED_2	
6Ah	SK_NOT_USED_3	
6Bh	SK_NOT_USED_4	
Recal/Fatal operation errors		
6Ch	EC_RCL_CS_PES	Recal fault: Coarse Slope PES Gain calibration
6Dh		Recovered - Recal fault: Coarse Slope PES Gain calibration.
6Eh	EC_RCL_AEQBH	Recal fault: Fine Slope PES Gain calibration at AEQBH
6Fh		Recovered - Recal fault: Fine Slope PES Gain calibration at AEQBH
70h	EC_RCL_AEQBL	Recal fault: Fine Slope PES Gain calibration at AEQBL
71h		Recovered - Recal fault: Fine Slope PES Gain calibration at AEQBL
72h	EC_RCL_ON_TRACK	Recal fault: Cannot lock to track
73h		Recovered - Recal fault: Cannot lock to track
74h	EC_RCL_NO_SAM	Recal fault: Cannot detect SAM during un_parking
75h		Recovered - Recal fault: Cannot detect SAM during un_parking.
76h	EC_RCL_SK_OD	Recal fault: Cannot seek to OD area to get near system cylinder.
77h		Recovered - Recal fault: Cannot seek to OD area to get near system cylinder
78h	EC_RCL_SK_FS_PES	Recal fault: Cannot seek to Fine Slope PES Gain calibration
79h		Recovered - Recal fault: Cannot seek to Fine Slope PES Gain calibration
7Ah	EC_RCL_SK_NULLI	Recal fault: Seek failure during Nulli calibration
7Bh		Recovered - Recal fault: Seek failure during Nulli calibration
7Ch	EC_RCL_SK_VSCALE	Recal fault: Seek failure during V_SCALE adaptation
7Dh		Recovered - Recal fault: Seek failure during V_SCALE adaptation
7Eh	EC_RCL_SK_KLOOP	Recal fault: Seek failure during LOOPK calibration
7Fh		Recovered - Recal fault: Seek failure during LOOPK calibration
80h	EC_RCL_SK_RRO	Recal fault: Seek failure during Repeatable Run-Out calibration

Value	Error Name	Description
81h		Recovered - Recal fault: Seek failure during Repeatable Run-Out calibration
82h	EC_RCL_SK_REZERO	Recal fault: Seek failure to track 0 during rezero
83h		Recovered - Recal fault: Seek failure to track 0 during rezer
84h	EC_RCL_KLOOP	Recal fault: Unable to complete LOOPK calibration
85h		Recovered - Recal fault: Unable to complete LOOPK calibration
86h	EC_RCL_RRO	Recal fault: Unable to complete Repeatable Run-Out calibration
87h		Recovered - Recal fault: Unable to complete Repeatable Run-Out calibration
88h	EC_RCL_MAP_HDS	Recal fault: Cannot detect reliable SAM on one or more heads
89h		Recovered - Recal fault: Cannot detect reliable SAM on one or more heads
8Ah	EC_MOTOR_FAULT	Motor unable to get up to speed
8Bh		Recovered - Motor unable to get up to speed
8Ch	EC_RCL_FAIL_WEDGE_SYNC	Failed seek to band used to sync wedges
8Dh		Recovered - Failed seek to sync wedges
8Eh	RCL_NOT_USED_1	
SMART Specific errors		
8Fh	EC_FAIL_PRED_THRES_MET	DPA variables have reached max
90h	EC_LOG_COUNTER_AT_MAX	Log counter at maximum
91h	EC_SPINUP_THRES_EXCEEDED	The spinup time threshold is exceeded
92h	EC_MED_DEF_THRES_EXCEEDED	The media defects threshold is exceeded
93h	EC_START_STOP_THRES_EXCEE DED	The Start/Stop threshold is exceeded
94h	EC_COMPAQ_THRES_EXCEEDED	The Compaq attribute threshold is exceeded
95h	EC_THRESHOLD_CND_MET	Threshold condition met
AT Specific SMART errors		
96h	EC_INV_FP_REVISION	Invalid revision in the Failure Prediction structure
97h	EC_INV_FP_FEATURES	Invalid function in the Features register
98h	EC_FP_DISABLE	Failure prediction operations are disabled
99h	EC_READ_FP_SECTORS	Can't read any of the FP sectors from the media
9Ah	EC_WRITE_FP_SECTORS	Can't write to any of the FP sectors from the media
9Bh	EC_INV_FP_PASSWORD	Execute Drive Failure Prediction Command is attempted without the?
9Ch	EC_INV_FP_CHKSM	The checksum in a Warranty Threshold Data structure sent to
9Dh	AT_NOT_USED_1	
9Eh	AT_NOT_USED_2	
9Fh	AT_NOT_USED_3	

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