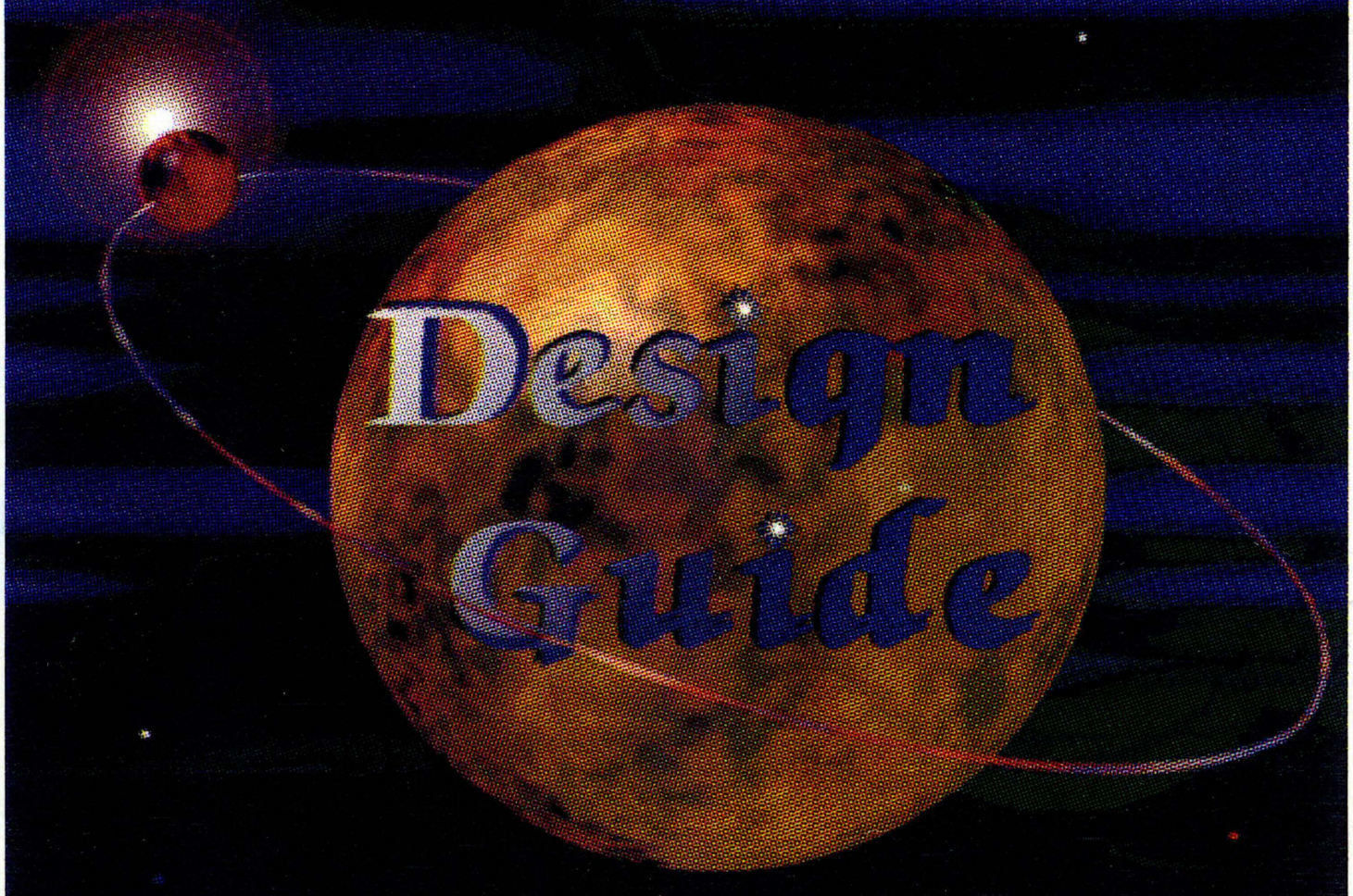
Europa



Design Guide

October 1994 Rev. B

Confidential

Table of contents

*** Indicates the updates from Rev. A to Rev. B in text, figures and/or tables.**

Table of contents

*** Indicates the updates from Rev. A to Rev. B in text, figures and/or tables.**

Table of contents

*** Indicates the updates from Rev. A to Rev. B in text, figures and/or tables.**

TABLES

FIGURES

Section 1 Background Information

1.1 General Description

Europa is a family of 2.5-inch form factor rigid disk products with capacities of 270 MB, 405 MB, 540 MB (12.5 mm high) and 810 MB, 1080 MB (19 mm high). AT interface will be available.

Description	# of Data Disks	# of Data Surfaces	Capacity
A. 1/2" AT	1	2	270 MB
B. 1/2" AT	2	3	405 MB
C. 1/2" AT	2	4	540 MB
D. 3/4" AT	3	6	810 MB
E. 3/4" AT	4	8	1080 MB

Table 1-1 Summary of Europa product line.

1.2 Basic Development Assumptions

Positions Quantum as responsive to 2 key notebook market trends with a leadership product. The 1/2" high drive is targeted for new, thinner notebooks known as slim-line. The 3/4" high drive is targeted for a class of powerful notebook computers with desktop functionality and high performance.

The need to bring Europa to market within a critical "time-window" dictates that Fast Cycle Time methods be used in the product development.

Manufacturing will be done in Japan by MKE, lowering process risk and increasing cost competitiveness.

Design Leverage from Daytona mechanics as much as possible.

1.2.1 Top Development Priorities

1) Time to market: full spec. evaluations in February 1995. Mass Pro by April 1995.
2) High capacity: 270 MBs formatted per disk.
3) Low power consumption.
4) Cost.

1.2.2 Top Development Risks

1) Integrating MR heads into a production drive.
2) Integrating the PRML read channel.
3) Making the servo function at 5300TPI with adequate TMR.

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Section 2 Specifications

This section provides the physical, electrical, and environmental specifications for the Europa 270, 405, 540, 810, 1080 MB hard disk drive.

2.1 Enhancements

The following are enhancements to the Europa Drive:

Europa	Daytona
• MR Heads	Thin Film Heads
• PRML Channel	Peak Detect
• 5300 TPI	3100 TPI
• 499.8 Mb/in^2	221.97 Mb/in^2
• 2 Burst ECC on the Fly	Single Burst ECC on the Fly
• Burst Transfer Rate 13 MB/s	4 MB/s
• State Space Control Servo	
• 4 Burst Servo Write	3 Burst Servo Write
• ECC 160 bit RS with Cross Check	ECC 112 bit RS with Cross Check

2.2 General Specification

2.2.1 Capacity/Format/Channel Specification

MODEL	270 MB	405 MB	540 MB	810 MB	1080 MB
Spindle Speed	3799.15 RPM	3799.15 RPM	3799.15 RPM	3799.15 RPM	3799.15 RPM
Servo Method	Embedded	Embedded	Embedded	Embedded	Embedded
Servo Sample Per Track	88	88	88	88	88
ID Radius	0.6533 in	0.6533 in	0.6533 in	0.6533 in	0.6533 in
OD Radius	1.2098 in	1.2098 in	1.2098 in	1.2098 in	1.2098 in
Stroke	0.5565 in	0.5565 in	0.5565 in	0.5565 in	0.5565 in
Recording Code	8/9 PRML	8/9 PRML	8/9 PRML	8/9 PRML	8/9 PRML
Recording Zone	16	16	16	16	16
TPI	5300	5300	5300	5300	5300
Flux Change Per Inch (Max.)	106,097	106,097	106,097	106,097	106,097
Bits Per Inch (Max.)	94,308	94,308	94,308	94,308	94,308
Areal Density (Max.)	499.8 Mb/in^2	499.8 Mb/in^2	499.8 Mb/in^2	499.8 Mb/in^2	499.8 Mb/in^2
Data Rate (Max.)	39.37 Mb/s	39.37 Mb/s	39.37 Mb/s	39.37 Mb/s	39.37 Mb/s
Data Raye (Min.)	24.44 Mb/s	24.44 Mb/s	24.44 Mb/s	24.44 Mb/s	24.44 Mb/s
Number of Disks	1	2	2	3	4
Number of Heads	2	3	4	6	8
Formatted Capacity (MBytes)	270.267	406.149	542.031	813.796	1085.560
Cylinders	2949	2949	2949	2949	2949
User Data Cylinders	2925	2925	2925	2925	2925
Data Tracks	5850	8775	11700	17550	23400
Data Surfaces	2	3	4	6	8
Sectors Per Track	Variable	Variable	Variable	Variable	Variable
Data Bytes Per Sector	512	512	512	512	512
Spare Sectors (1 per cylinder)	2925	2925	2925	2925	2925
AT Logical Capacity (Bytes)	270,167,040	405,250,560	540,334,080	810,501,120	1080,668,160
AT Logical Sectors	527,670	791,505	1,055,340	1,583,010	2,110,680
AT Logical Cylinder	2665	2665	4059	4059	3608
AT Logical Heads	11	11	13	13	15
AT Logical Sectors/Track	18	27	20	30	39
Buffer & RAM	Single 64K x 16 DRAM (1 MB)	Single 64K x 16 DRAM (1 MB)	Single 64K x 16 DRAM (1 MB)	Single 64K x 16 DRAM (1 MB)	Single 64K x 16 DRAM (1 MB)
Cache Size	86 KB (Minimum)	86 KB (Minimum)	86 KB (Minimum)	86 KB (Minimum)	86 KB (Minimum)
Data Format	I.D. after Wedge (Multiple Sectors per Wedge)	I.D. after Wedge (Multiple Sectors per Wedge)	I.D. after Wedge (Multiple Sectors per Wedge)	I.D. after Wedge (Multiple sectors per wedge)	I.D. after Wedge (Multiple sectors per wedge)
ECC	160 bit RS with Cross Check	160 bit RS with Cross Check	160 bit RS with Cross Check	160 bit RS with Cross Check	160 bit RS with Cross Check

Table 2-1 Capacity/Format/Channel Specification

2.2.2 AT Interface Specification

Interface Features	DisCache and WriteCache Adaptive Segmentation AutoRead, AutoWrite and AutoTransfer Local Bus with IOCHRDY Fast Multiword DMA LBA Mode Double Burst ECC on-the-fly
Interface	ATA/CAM
Interface Transfer Rate	Sustained 8.33MB/s without flow control[1] **PIO**[2] Up to mode 4 @ 16MB/s **DMA** Up to mode 2 @ 16MB/s
Performance	
Sequential Throughput[3]	
Read	5MB/s (4096 Byte Record)
Write	5MB/s (4096 Byte Record)
PC Bench Disk Harmonic	TBD
Q-Bench Data Access Time	TBD

Table 2-2 AT Interface Specification

Notes to Table 2-2:

1. Between handshakes.
2. Rates above 8.33MB/s require IOCHRDY.
3. Performance is typical for outer zone.

2.3 Timing Parameters

	Typical [1] Nominal	Maximum[1] Nominal
Command Overhead[2]	1 ms	N/A
Head Switch Time[3]	5 ms	6 ms
Single Track Seek[4]	5 ms	8 ms
Average Seek[5]	16 ms	19 ms
Full Stroke Seek[6]	24 ms	27 ms
Average Rotational Latency	7.9 ms	
Power On[7] or Sleep To Drive Ready[8]	3.5 s (1 Disk) 4.0 s (others)	
Standby To Drive Ready	2.0 s (1 Disk) 2.5 s (2 Disk) 3.0 s (3, 4 Disk)	
Idle To Drive Ready	0.5 s	
Power Down To Spindle Stop	5 s	

Table 2-3 Timing Specifications

Notes to Table 2-3:

Quoted seek times include head settling time, but do not include command overhead time or rotational latency time.

1. Typical means average performance across a population of drives under nominal temperature (25°C), voltage (+5Vdc) and no applied shock or vibration. Maximum means average performance of the worst case drive in a population under nominal temperature, voltage and no applied shock or vibration.

2. Command overhead is approximated by measuring response time to a seek of zero length.

3. Head Switch is the average time to stop track following on one surface and begin track following on any other surface within any one cylinder.

4. Single Track Seek time is calculated by seeking, track by track, from the outermost track to the innermost track and back; the elapsed time is then divided by twice the number of tracks.

5. Average Seek time is the mean value for all possible seek combinations.

6. A minimum of 100 full stroke seeks per drive must be averaged to establish the full stroke seek specification value.

7. Power On: the time from the supply voltages reaching operating range to the drive being able to accept any command.

8. Drive Ready: in this mode the disks are spinning at rated speed, the drive is able to accept and execute commands requiring disk access with further delay.

2.4 Disk Errors

Error Type	
Recoverable Read Errors[1]	1 Event per 10^{10} bits read
Correctable Read Errors[2]	1 Event per 10^{12} bits read
Uncorrectable Read Error[3]	1 Event per 10^{14} bits read
Seek Errors[4]	1 Error per 10^{6} seeks

Table 2-4 Error types and rates

Notes to Table 2-4:

1. Recoverable Read errors are those which require up to 8 retries for data correction. Errors corrected by ECC on the fly are not considered recovered read errors. Read on arrival is disabled to meet this specification.

2. Correctable errors are those read errors which require the triple burst error correction algorithm to be applied for data correction. This correction is typically applied only after the programmed retry count is exhausted.

3. Uncorrectable read errors are those errors that is not correctable using an error correcting code (ECC) or retries. The drive terminates retry reads either when a repeating error pattern occurs or after eight unsuccessful retries and application of double burst error correction.

4. A seek error occurs when the actuator fails to reach or remain on the requested cylinder, and the drive requires the execution of the full recalibration routine to locate the requested cylinder.

5. Error rates are for worst case temperature & voltage.

2.5 Power Requirements

Europa hard disk drive operates from one supply voltage:

- + 5 V ± 5%

The allowable ripple and noise for supply voltage: (measured at drive connector.)

- + 5 V 50 mV P-P 0 Hz-10 MHz

2.5.1 Drive Power Dissipation

AT Drive Power Dissipation

Please refer to Table in Section 6.8.1 for power dissipation of the Europa Drive in various operation modes for 2 Disk and 4 Disk versions.

2.5.2 Power Reset Limits

When powering up, the drive will remain reset (inactive) until V_{HT} reset limits are exceeded. When powering down, the drive will become reset when supply voltage drops below the V_{LT} threshold.

POR THRESHOLDS

DC Supply	5V
V_{LT}	4.269V (Max.)
V_{HT}	4.616V (Max.)
Hysteresis	25 mV (Min.)

Table 2-5 Power Reset Limits

2.6 Environmental

2.6.1 Environmental Conditions

The drive will meet all of its operating performance specifications when operated within its operating environment and will sustain no damage or permanent performance degradations when subjected to the non-operating environment. Where applicable, SI units as well as American Standard units have been given.

Parameter	Operating	Non-operating
Temperature	5°C to 55°C 41°F to 131°F	-40°C to 65°C -40°F to 149°F
Temperature Gradient	20°C/hr. Maximum	20°C/hr. Maximum
Humidity[1] Max. Wet Bulb Temp.	10 to 90% RH 29°C 84.2°F	10 to 90% RH 38°C 100.4°F
Humidity Gradient	30% per hour	30% per hour
Altitude[2]	-200 to 10,000 ft -60.96 to 3048 m	-200 to 40,000 ft -60.96 to 12192 m
Shock Linear (Max.) Linear (Apple, Max.) Linear (Compaq, Max.) Rotational (Compaq, Max.)	 10G, 11mSec[3] 30G, 3mSec[5]	 100.0 G, 11mSec[4] 300.0 G, 2mSec[6] 20K rad/s2, 2mSec[7]
Vibration Vibration (Apple) 1 octave/min.	1 G, P-P 5-300 Hz 2 Gs, P-P	5 Gs P-P 5-300Hz

Table 2-6 Environmental Specifications

Notes to Table 2-6:

1. Humidity: these figures do not take condensation into account. See Appendix D for humidity charts for low and medium temperatures.
2. Altitude: relative to sea level.
3. While drive is in seek, read and write mode.
4. Without permanent hardware damage.
5. While drive is in seek and read mode only.
6. Compaq criteria. Damage allowed. 1 drop per axis maximum.
7. For Europa 270: rotational shock spec. is 10,000 rad/s2.

2.6.2 Electromagnetic Conditions

SENSITIVITY TO MAGNETIC FIELDS

The drives will meet all specifications with less than 6 gauss field applied in any orientation.

2.7 Mechanical

Height	0.492 ± 0.008 in	(12.50 ± 0.20 mm)	(2 Disk)
	0.742 ± 0.008 in	(18.80 ± 0.20 mm)	(4 Disk)
Length	3.94 ± 0.020 in	(100.0 ± 0.50 mm)	
Width	2.75 ± 0.008 in	(69.8 ± 0.2 mm)	
Weight	0.277 lb	(126 gm)	(2 Disk)
	0.403 lb	(183 gm)	(4 Disk)

2.8 Acoustics

This will be measured in an anechoic chamber, with background noise < 20 dbA, with PCB face down.

2.8.1 Sound Power

	Measured Noise	Distance
Idle on Track	4.0 bels	1M

Table 2-7 Acoustical specifications

2.8.2 Sound Pressure

	Measured Noise	Distance
Idle on Track	33 dbA (max.)[1]	1M

Table 2-8 Acoustical specifications

Notes to Table 2-8:

1. With no prominent discrete tones. Prominent discrete tones are defined here as the frequency bands (in the 1/3 octave bands) which have a db level higher than the average of the 2-adjacent bands by more than 5 db.

2.9 Reliability

Field MTBF[1] @ 25° C	350,000
Component Life	5 YEARS
Start/Stops (40° C, 15% RH)	40,000

Table 2-9 Reliability specifications

Notes to Table 2-9:

1. The Quantum MTBF numbers represent MTBF predictions per TR-TSY-000332 issue Bell-Core, Sept. 1990 and represent the minimum MTBF that Quantum or a customer would expect from the drive.

2.10 Hard Defects During Manufacture

During manufacturing and test, no drive shall re-allocate more than 1 block/ Megabyte.

540 drive will have no more than 540 defective blocks

2.11 Connector/Jumper

2.11.1 AT I/O POWER CONNECTOR

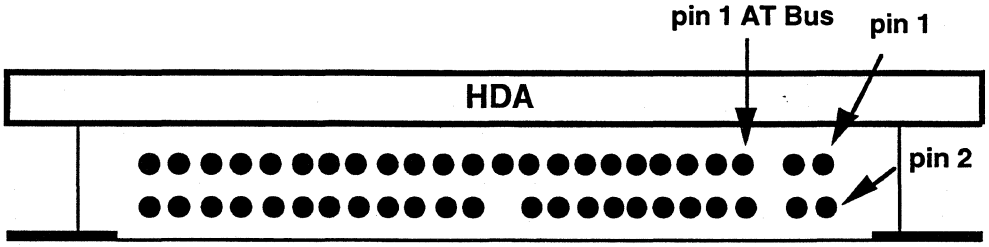


Figure 2-1 AT I/O DC Power Connector

Notes to Figure 2-1:

1. Pin 1 through pin 4 of the connector are used as factory test points.

+5.0V DC	pin 48 (Motor) pin 47 (Digital)
Ground	pin 46 (Motor) pin 8, 25, 28, 30, 32, 36, 49 (Digital)

Table 2-10 AT I/O Power Connector Pwr/Gnd pin assignments

2.11.2 AT JUMPER

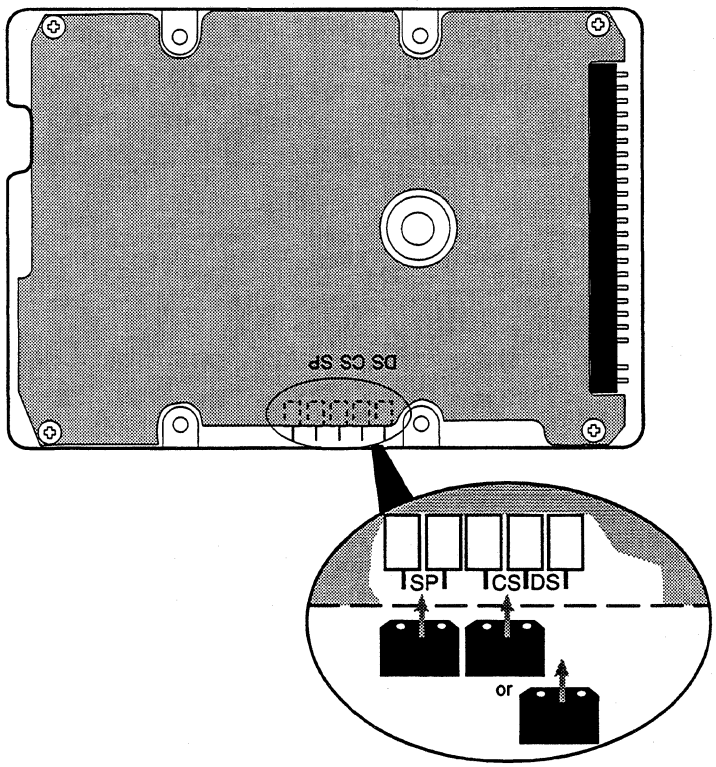


Figure 2-2 Jumper location on PCB

CS	Cable Select
DS	Drive Select
SP	Slave Present

Table 2-11 AT Jumper Operational Mode

2.11.2.1 Jumper Configuration

This subsection describes how to configure the Europa Drive AT prior to installation in a system. The location of the jumper pins on the underside of the printed circuit board (PCB) control these options as shown in Figure 2-3.

Europa AT hard disk drives can be configured as a master or a slave drive, using either the jumper blocks on the drive's controller board or by grounding certain lines on the interface connector.

There are two sets of jumper pins. The SP set (the two jumper pins at the left of Figure 2-3) is labeled "SP" for slave present. The other set (three jumper pins) has two labels "CS" and "DS" for Cable Select and Drive Select. The center pin is common to both the CS and the DS positions.
When a jumper block is on the center pin and the pin nearest the interface connector, DS is enabled. When a jumper block is on the center pin and the pin furthest from the interface connector, CS is enabled.

2.11.2.2 Cable Select (CS) Jumper

The drive can be configured such that its status as a master drive or slave drive can be determined by the cabling from the host system. This is extremely helpful when AT drive is used as a removable subsystem where it can be either a master drive or a slave drive depending upon the cable to which it is connected.

When a drive is configured for cable selection, it is the master drive if pin 28 is grounded and a slave if pin 28 is not grounded.

For systems that do not use Pin 28 for another purpose (e.g., Spindle Synchronization), the host system can tie Pin 28 to ground. Then the cable connecting the host to the master has Pin 28 enabled (i.e., a circuit exists), while the cable connecting the slave to either the host or the master has the Pin 28 line severed.

Systems that use Pin 28 can use the cable selection method by performing the following:

1. Connect the system cable in the following order:
   host <--> slave <--> master

2. Cut the Pin 28 line between the slave and the master. This allows Pin 28 to operate normally (an open—severed connection) between the host and the slave.

3. Tie Pin 28 (within the master drive header) to a nearby ground (Pin 30, for example).

This process will allow the master drive to have Pin 28 grounded while allowing the Pin 28 to be open between the host and slave drive.

2.11.2.3 Master Drive with Slave Present

When Europa AT hard disk drives are configured as a master drive, the drive looks for a slave drive by monitoring the PDIAG/DASP lines.

Some hard disk drives when configured as a slave drive do not indicate their presence on these two lines (Europa Drive does). To indicate that a slave is present for these drives (when using Europa Drive as a master), the slave present (SP) pins on Europa Drive master must be jumpered as shown in Figure 2-2.

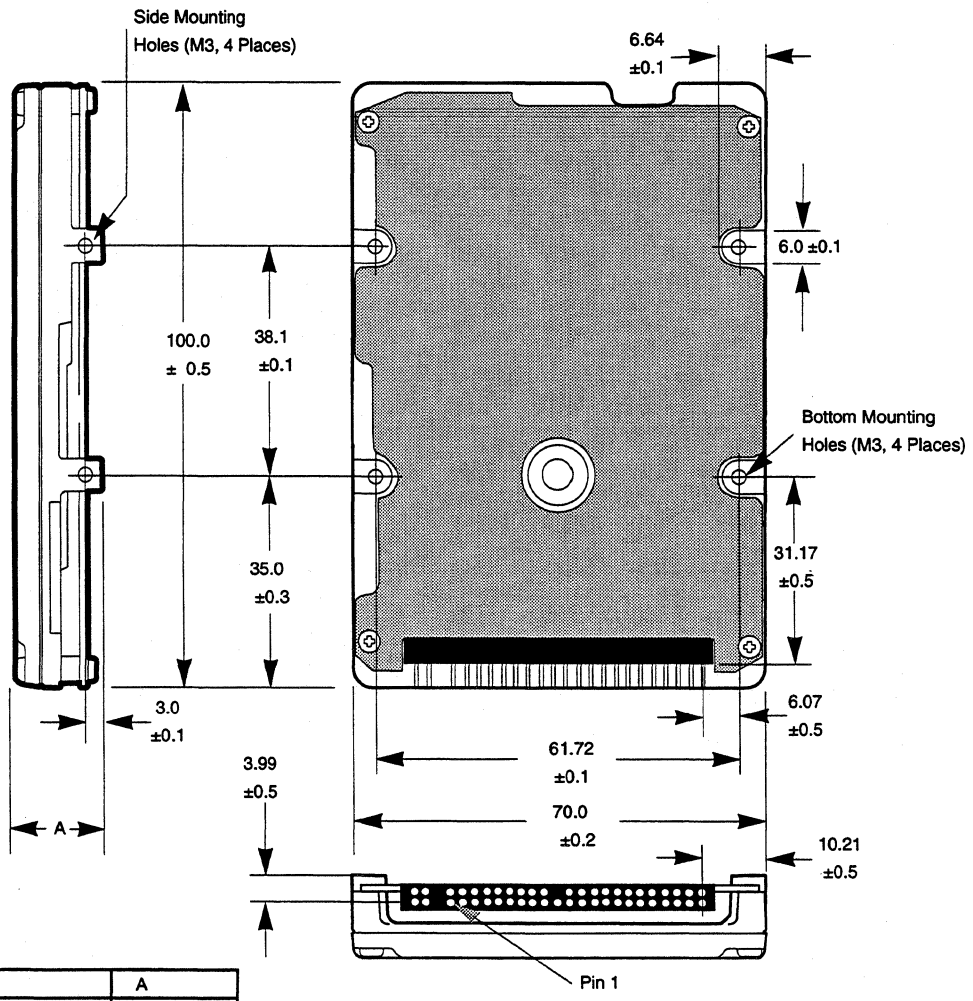
2.12 Mounting

2.12.1 Orientation

The Europa family of drives may be mounted in any orientation and nominal position is PCB face down.

2.12.2 Mounting

For mounting, M3 screws are recommended. To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 40 inch-ounces.



	A
Europa 270MB	12.5 ± 0.2
405,540MB	12.5 ± 0.2
810,1080MB	18.80 ± 0.2

All dimensions are in millimeters.

Figure 2-3 Mounting Dimensions

2.12.3 Clearance

Clearance from the drive (except shock mount brackets or faceplate) to any other surface shall be 0.05 in minimum.

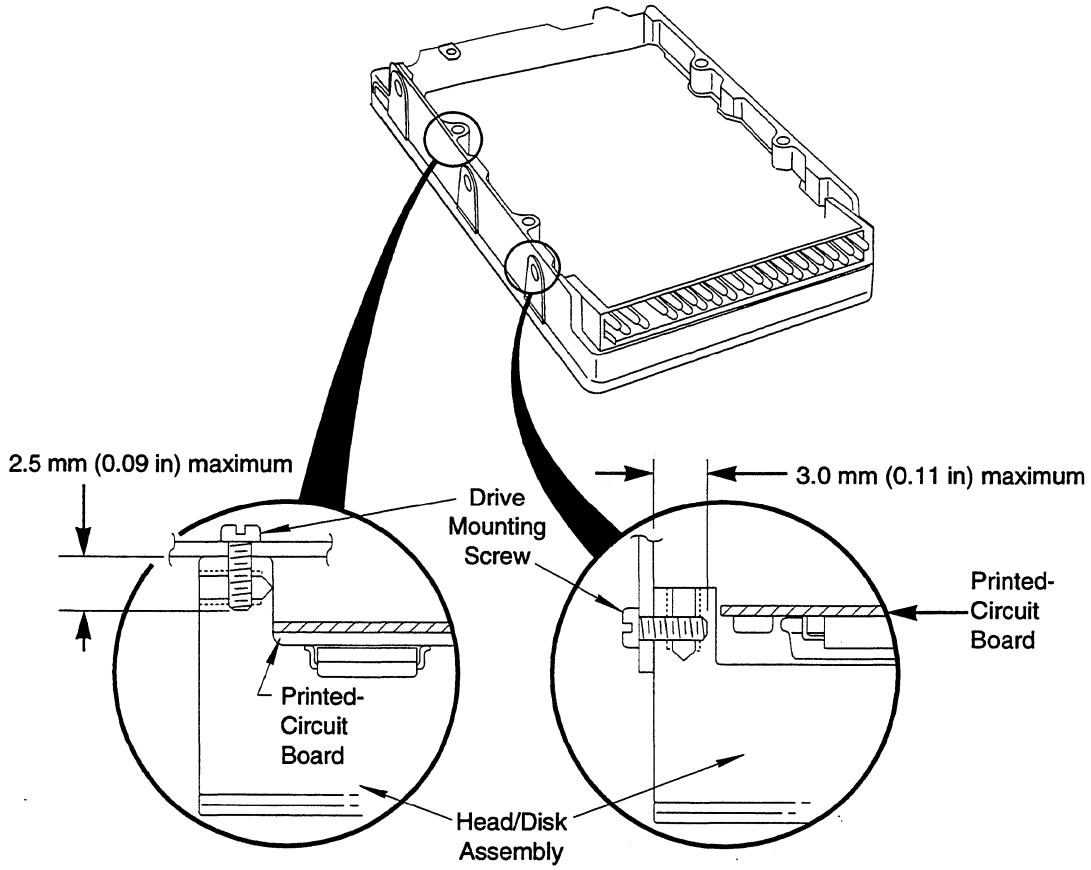


Figure 2-4 Drive Mounting Screw Clearance

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Section 3 Track Specifications

The Europa disk drives are shipped from the factory as "hard sectored" drives. That is, all physical sector addresses are written on the disks before the drives are shipped. As a result, sector size and number of sectors per track are not user selectable. The information given in this section is the physical format of Europa as it is defined at the factory prior to shipment.

Note that the physical format is in contrast to the logical format of the drive, which is how the drive appears to the host system.

3.1 Track Locations

	Gap Centerline	Outside Corner of Slider	Inside Corner of Slider
Disk edge radius (nominal)	1.2795		
Disk chamfer radius (nominal)	1.2736		
Outer crash stop compressed radius	1.2381	1.2598	N/A
Outer crash stop uncompressed radius	1.2090	N/A	N/A
System data (Cyl -24)	1.2097		
Zone 1 outside radius	1.2052		
Zone 15 inside radius	0.6533		
Largest Inner crash stop uncompressed radius	0.6272		N/A
Largest Inner crash stop compressed radius	0.5918	N/A	0.4779
Disk clamp outside radius	0.4685	N/A	N/A
Spindle hub radius	0.3933		
Pivot-to-spindle distance	1.6578		
Head arm length to center gap	1.5425		

Table 3-1 Track Locations

The actuator sweeps out an angle of 23.85° from crash stop to crash stop. This is measured from a line passing through the pivot and the geometric center of the slider. From the start of servos to the end of servos the angle is 20.78°.

3.2 Track Format

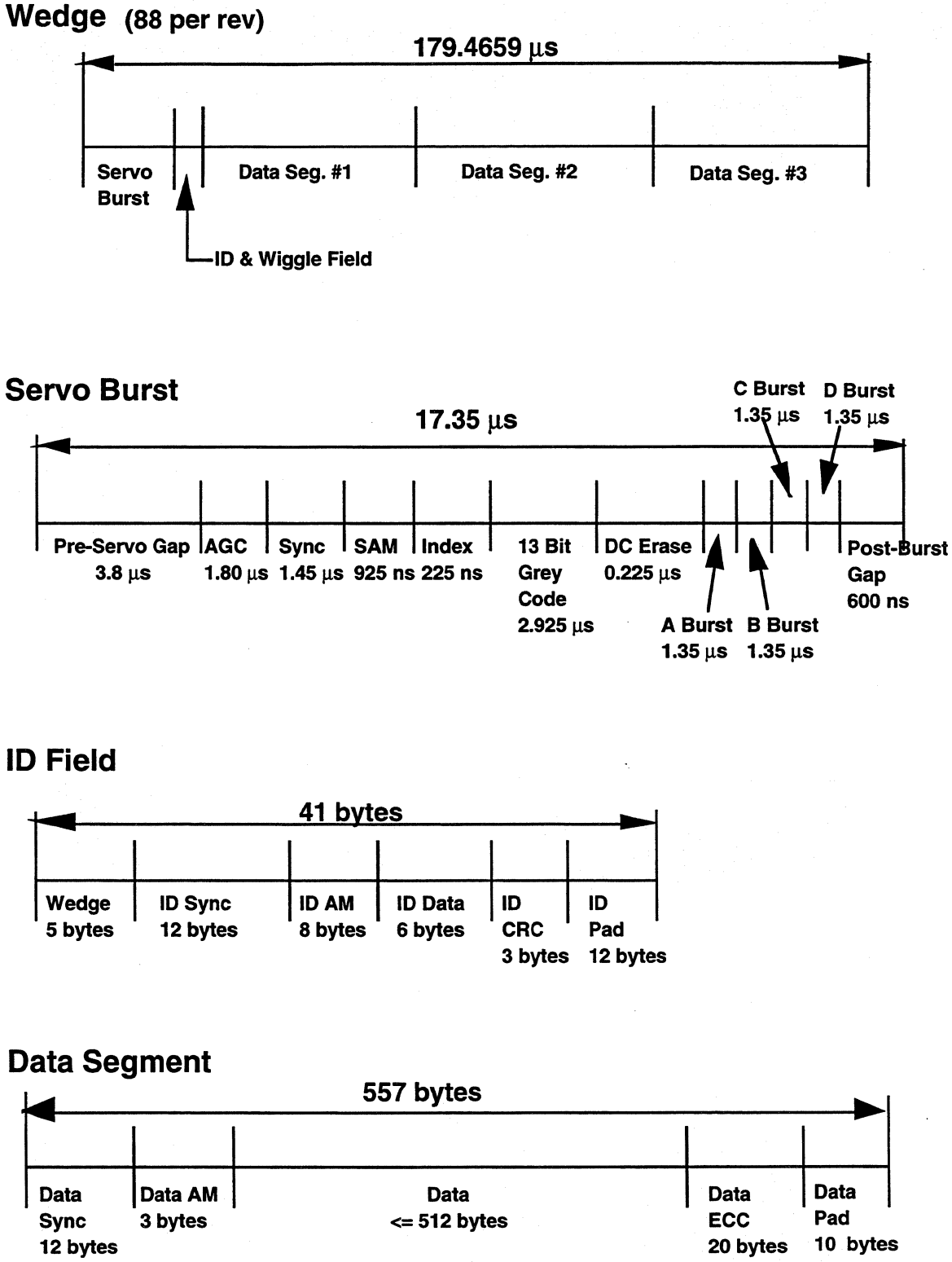

Figure 3-1 Track Format

Europa Zone Specification

Zone Number	Zone Outside Radius	Zone Inside Radius	No. Cyl.	Sectors Per Track	Sectors Per Zone [1]	Bytes Per Sector	Sector Time uSec	Data Rate Mb/Sec	Write Clock (MHz)	Fmax (Sine) (MHz)
System	1.2097	1.2052	24	88	2112	512	145.54	30.62	34.44	17.22
1	1.2052	1.1684	195	110	21450	512	113.20	39.37	44.29	22.14
2	1.1684	1.1316	195	108	21060	512	115.68	38.52	43.33	21,67
3	1.1316	1.0948	195	105	20475	512	117.95	37.78	42.50	21.25
4	1.0948	1.0580	195	105	20475	512	117.95	37.78	42.50	21.25
5	1.0580	1.0212	195	104	20280	512	120.31	37.04	41.67	20.83
6	1.0212	0.9844	195	99	19305	512	125.33	35.56	40.00	20.00
7	0.9844	0.9476	195	99	19305	512	125.33	35.56	40.00	20.00
8	0.9476	0.9108	195	94	18330	512	130.77	34.07	38.33	19.17
9	0.9108	0.8741	195	88	17160	512	145.54	30.62	34.44	17.22
10	0.8741	0.8373	195	88	17160	512	145.54	30.62	34.44	17.22
11	0.8373	0.8005	195	82	15990	512	148.53	30.00	33.75	16.88
12	0.8005	0.7637	195	77	15015	512	156.66	28.84	32.00	16.00
13	0.7637	0.7269	195	70	13650	512	167.10	26.67	32.00	15.00
14	0.7269	0.6901	195	66	12870	512	182.29	24.44	27.50	13.75
15	0.6901	0.6533	195	66	12870	512	182.29	24.44	27.50	13.75

Table 3-2 Zone Specification

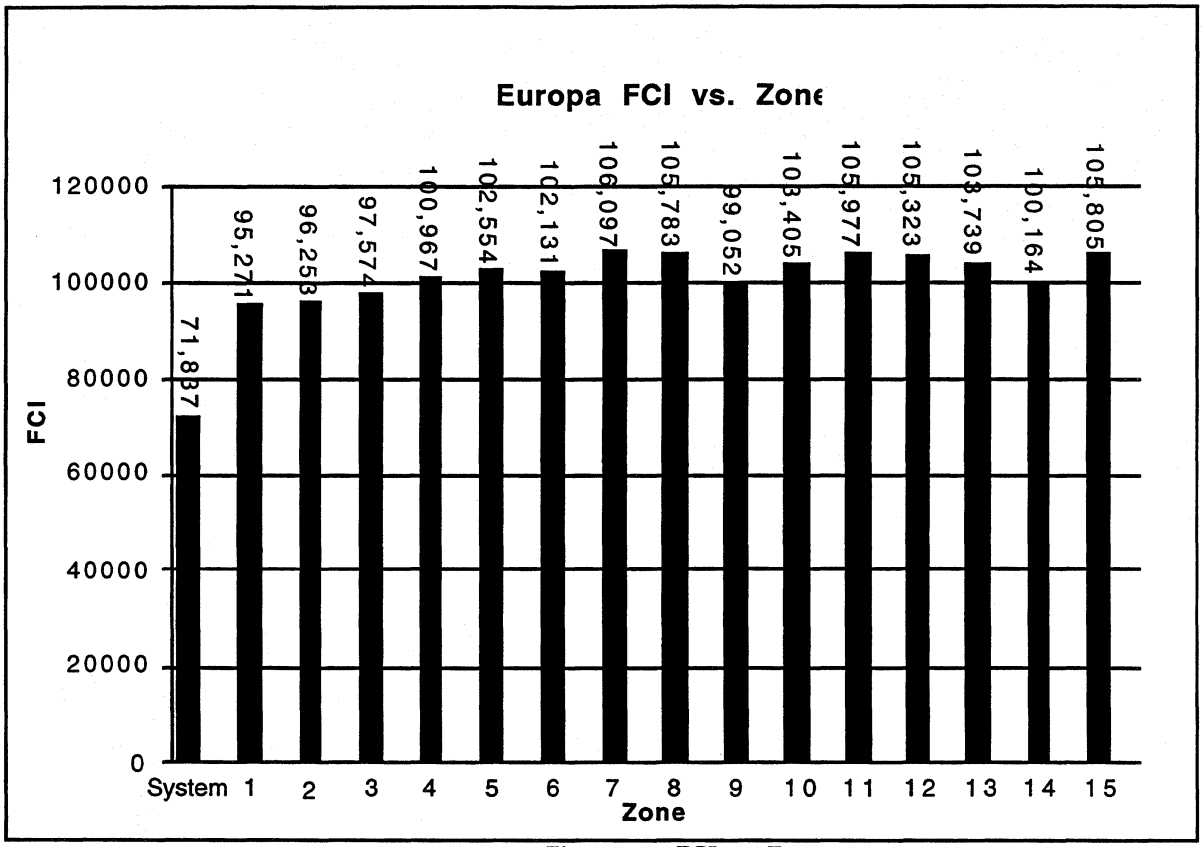

Figure 3-2 FCI vs Zone

3.3 Cylinder Contents

Cylinder Contents	Zone	Cylinder Range	Date Rate Mb/S	Sectors Per Track
User Data	15	2730 - 2924	24.44	66
	14	2535 - 2729	24.44	66
	13	2340 - 2534	26.67	70
	12	2145 - 2339	28.44	77
	11	1950 - 2144	30.00	82
	10	1755 - 1949	30.62	88
	9	1560 - 1754	30.62	88
	8	1365 - 1559	34.07	94
	7	1170 - 1364	35.56	99
	6	975 - 1169	35.56	99
	5	780 - 974	37.04	104
	4	585 - 779	37.78	105
	3	390 - 584	37.78	105
	2	195 - 389	38.52	108
	1	0 - 194	39.37	110
Test Equip. Data Error logging	System	-1	30.62	88
System Firmware	System	-2	30.62	88
Diskware	System	-3	30.62	88
Diskware	System	-4	30.62	88
Test Equip. Data Error logging	System	-5	30.62	88
System Firmware	System	-6	30.62	88
Diskware	System	-7	30.62	88
Diskware	System	-8	30.62	88
Not in Use	System	-9 to -24	N/A	N/A

Table 3-3. Cylinder contents breakdown.

Notes to Table 3-3:

1. Zone 1 is the outermost zone, zone 15 is the innermost zone.

2. Eight cylinders on all drives are reserved for system, Diskware and test usage. These cylinders contain drive configuration information, drive test information, and diskware. Customers cannot access these reserved cylinders. The reserved cylinders are only accessible with physical address commands which are protected diagnostic commands.

3. Data is repeated on cyl -1 and cyl -5, cyl -2 and cyl -6, cyl -3 and cyl -7 also repeated on cyl -4 and cyl -8, and is stored in the OD system areas for redundancy. Data is read from and written to these areas according to the firmware redundancy algorithm.

4. The test equipment cylinder (-1, -5) is reserved for test equipment usage. This cylinder contains test parameters and data collected during production test. Writing on this cylinder may erase some important information and cause the drive to be rejected and sent back to the servo writer station.

   The sector usage is as follow:

Sector	Usage
0	Serial number data.
1	Process interlock.
2	Reserved.
3	Configuration center.
4	Reserved.
5 - 14	Test process history
15 - 30	Process test defect list.
31	Reserved.
32 - 40	Self scan results.
41 - 48	Self scan test parameters.
49 - 59	Self scan defect list.
60 - 61	Self scan - RRO/NRRO results.
62 - 65	Logical scan log.
66	NULLI calibration data.
67	Head stability test
68 - 70	Servo defect map.
71 - 83	Not in use.
84 - 87	Reserved for process test flow mapping.

5. The System cylinder (-2, -6) is reserved for system usage. It contains mode page information, configuration information, defect lists, and format information for the drive. Writing on this cylinder may erase some important information and prohibit the drive from operating.

   The sector usage is as follows:

Sector	Usage
0	AT mode select pages 1 and 2.
1	AT mode select pages 3 and 4.
2 - 6	Configuration pages.
7 - 10	Working defect list .
11 - 14	Primary defect list .
15 - 18	Temporary defect list.
19 - 34	Format ID bytes.
35 - 47	Parameter analysis.
48 - 63	Reserved main overlay.
64 - 79	Selfscan overlay 4.
80 - 83	Not in use.
84 - 87	Reserved for process test flow mapping.

6. The Diskware cylinders (-3, -7), (-4,-8) are reserved for Diskware usage. The sector usage is as follows:

Cylinder -3,-7

Sector	Usage
0 - 63	Main diskware.
64 - 80	Selfscan overlay 3.
81 - 83	Not in use.
84 - 87	Reserved for process test flow mapping.

Cylinder -4, -8

Sector	Usage
0 - 47	Self scan main.
48 - 63	Selfscan overlay 1.
64 - 79	Selfscan overlay 2.
80 - 83	Not in use.
84 - 87	Reserved for process test flow mapping.

3.4 Track and Cylinder Skewing

Since the Europa drives are storage subsystems with integrated controllers, the function and design of the controller can be optimized specifically for the drive. One method of optimization employed by Quantum to improve data throughput is skewing sector addresses.

The purpose of track and cylinder skewing is to minimize latency time and thus increase data throughput when data is sequentially accessed to or from the disk. The two types of skewing employed, track and cylinder skewing, are described below.

3.4.1 Track Skewing

Track skewing reduces latency time which results when the drive must switch read/write heads to access sequential data. A track skew is employed such that the next logical sector of data to be accessed will be under the read/write head once the head switch is made and data is ready to be accessed.

Since head switch times are defined on Europa, the sector addresses can be optimally positioned across track boundaries to minimize the latency time which results when a head switch has to be performed.

3.4.2 Cylinder Skewing

Cylinder skewing is also used on Europa to minimize latency time during sequential accessing of data. However, instead of minimizing latency time due to head switching, as with track skewing, cylinder skewing is used to minimize latency time due to a single-cylinder seek.

The next logical sector of data which crosses a cylinder boundary is positioned on the drive such that after a single-cylinder seek is performed, and the drive is ready to continue accessing data, the sector to be accessed is positioned directly under the read/write head. Therefore, the cylinder skew takes place between the last sector of data on the last head at a cylinder and the first sector of data on the first head at the next cylinder.

Since single-cylinder seek times are defined on the drive, the sector addresses can be optimally positioned across cylinder boundaries to minimize the latency time which results when a seek has to be performed.

The optimal values for track and cylinder skew are determined empirically using a sample population of drives. Skew values based on preliminary data is shown below:

Zone Number	SPT	Wedge Hd Skew	Sector Cyl Skew	Hd Skew	Cyl Skew
System	88	TBD	TBD	TBD	TBD
1	110	TBD	TBD	TBD	TBD
2	108	TBD	TBD	TBD	TBD
3	105	TBD	TBD	TBD	TBD
4	105	TBD	TBD	TBD	TBD
5	104	TBD	TBD	TBD	TBD
6	99	TBD	TBD	TBD	TBD
7	99	TBD	TBD	TBD	TBD
8	94	TBD	TBD	TBD	TBD
9	88	TBD	TBD	TBD	TBD
10	88	TBD	TBD	TBD	TBD
11	82	TBD	TBD	TBD	TBD
12	77	TBD	TBD	TBD	TBD
13	70	TBD	TBD	TBD	TBD
14	66	TBD	TBD	TBD	TBD
15	66	TBD	TBD	TBD	TBD

Table 3-4. Europa Skew Optimization

Section 4 Mechanical

4.1 Motor

The 2.5" spindle motor to be used in the "Europa" Hard Disk Drive (Both two Disk & four Disk Version) is intended to be a "rotating shaft" design that is integral to the drive baseplate. One single screw diskclamp design will be implemented. Back-emf commutation technology will be used to drive motor. (Hall-less design concept).

4.1.1 Reference Documents

Spindle Motor Assembly	75-106946-01 75-106909-01	(2 Disk) (4 Disk)
Spindle Motor Driver	20-107180-01	
Disk 65mm X 20mm X 0.635mm	61-106983-01	
Disk Clamp	40-104391-01	
Spacer Disk	40-104418-01	

Table 4-1 Reference documents for spindle motor

4.1.2 General Specifications

Number of Poles	12
Number of Phases	3
Motor Type	Brushless DC
Driving Mode	BiPolar Y, with center tap
Commutation	Back- emf (Hall-less)
Number of Stator Slots	9
Mounting Orientation	Any Orientation
Flex Circuit Pin Descriptions	
Pin 1	w
Pin 2	v
Pin 3	u
Pin 4	center tap

Table 4-2 General specifications for spindle motor

4.1.3 Mechanical Characteristics

Dimensions per Drawing Number	75-106909-01 75-106946-02	(4 Disk) (2 Disk)
Weight	80 gm 55 gm	(4 Disk) (2 Disk)
Rotor Hub Inertia with Disk	143.0 g-cm2 72.0 g-cm2	(4 Disk) (2 Disk)
Torque Constant (Typ.)	85 gr-cm/A +10% - 5% 54 gr-cm/A +10% - 5%	(4 Disk) (2 Disk)
Torque Ripple	30% (Max.)	
Load Inertia[1]	125 gr-cm2 60 gr-cm2	(4 Disk) (2 Disk)
Motor Inertia	18 gr-cm2 12 gr-cm2	(4 Disk) (2 Disk)
Total Inertia	143 gr-cm2 72 gr-cm2	(4 Disk) (2 Disk)
Stiction Load (0 RPM) (Max.)	5 gr-cm	
Friction Load[2] (3800 RPM) (Max)	6 gr-cm	
Indent Torque (Cogging Torque)	5gf-cm (Max)	
Bearing Type	see 4.1.6.1	
Bearing PreLoad	0.9 Kg ± 10% 0.9 Kg ± 10%	(4 Disk) (2 Disk)
Seal Type[3]	Conductive Ferro Fluid	
Non-Repetitive Run-out (NRRO)[4]	0.35 µm (Max.)	
0<f<50Hz	0.10µm (Max.)-0-P	
50Hz<100Hz	0.05µm (Max.).-0-P	
100Hz<f<200 Hz	0.034µm (Max.).-0-P	
f<200 Hz	0.025µm (Max.).-0-P	
Repetitive Run-out (@ 4000 rpm)		
Radial[5]	8 µm (Max.)	
Axial	30 µm (Max.)	
Imbalance, bare spindle	0.1 gm-cm	
Acoustic noise[6]	<33dBA @ 100 cm	

Table 4-3 Mechanical specifications for spindle motor

Notes to Table 4-3:

1. Inertial load includes two disks, a 2.50 mm thick disk spacer, a disk clamp for Europa 540 MB and four disks, three 2.50 mm thick disk spacer, a disk clamp for Europa 1080MB.

2. Viscous drag.

3. Seal must withstand 80mm of H_20 (internal or external pressure while stationary) without fluid leaking.

4. NRRO should be measured at spindle assembly level that includes complete set of disks, spacers, one diskclamp and one screw.
NRRO measured at bare motor level does not reflect the actual NRRO measured at drive level.

5 Measured repetitive radial runout at 3800 rpm. The difference between the repetitive runout measured at 50Hz and the same measurement performed at 60Hz shall not exceed 5µin.

6. Measured in HDA, with fully loaded disks, spacers and clamp, with no prominent discrete tones. Prominent discrete tones defined as frequency bands (1/3 octave bands) which have a dB level higher than average of the two adjacent bands by 5 dB.

4.1.4 Electrical Characteristics

Supply Voltage Requirements	5 V (DC) ± 5%	
Minimum Motor Voltage[1]	3.05 V DC	(4 Disk)
	3.05 V DC	(2 Disk)
Coil Resistance (24°C)[2]	2.95 Ω (Max.)	(4 Disk)
	2.70 Ω (Nom.)	
	2.75 Ω (Max.)	(2 Disk)
	2.50 Ω (Nom.)	
Coil Inductance (f = 1kHz) (Max)	0.50 mH	(4 Disk)
	0.35 mH	(2 Disk)
Voltage Constant	0.0083 V-S/rad	(4 Disk)
	0.0059 V-S/rad	(2 Disk)
Back EMF (@5-70°C, 3800 rpm)	3.46 V +10% - 5% (0-p)	(4 Disk)
	2.25 V +10% - 5% (0-p)	(2 Disk)
Running Current[3] (Max)	150 mA	(4 Disk)
	130 mA	(2 Disk)
Starting Current (Min)	0.9 A	(4 Disk)
	0.9 A	(2 Disk)
Magnetic Flux Leakage[4]	3 Gauss (Max.) (0-p)	
Insulation resistance (Min)	50 M Ω	
Breakdown voltage	AC 250V for 1 Sec.	

Table 4-4 Electrical specifications for spindle motor

Notes to Table 4-4:

1. Measured at winding.
2. Measured across any two windings.
3. Measured with 5 gm-cm external load.
4. At 16.6 mm radius. Measured in any direction, non-operational.

4.1.5 Operating Parameters

Rotational Speed	3800 RPM ± 0.5%	
Direction of Rotation[1]	Counterclockwise	
Running Torque[2]	10.0 gr-cm (min.)	(4 Disk)
	10.0 gr-cm (min.)	(2 Disk)
Starting Torque[3]	64.5 gr-cm (min.)	(4 Disk)
	36 gr-cm (min.)	(2 Disk)
Start Time[4]	2.0 sec (max.)	

Table 4-5 Operating Parameters for spindle motor

Notes to Table 4-5:

1. CCW as viewed from hub side.
2. Measured @ 3800 RPM.
3. Minimum torque measured with 0.9 A (for 2 Disk), 0.9 A (for 4 Disk) to the motor, in any rotor position throughout environmental temperature range.
4. Measured @ 24° C, 5 Volts.

4.1.6 Materials

The materials used in the construction of the spindle motor are to be approved by Quantum Engineering. No changes are to be incorporated without receiving Engineering approval.

4.1.6.1 Mechanical Components

Hub		Wrought Aluminum (No castings)	
	Thermal Expansion on Ø20mm	22.9 X 10-6/° C	
Magnets Neodymium, encapsulated		Plastic-bonded	
Shaft		416 Stainless Steel or better	
Bearings, double-shielded ball[1]		4 Disk	2 Disk
	Size	9x4x2.6	9x4x2.6
	Vendor NSK Shielded	B4-50	B4-50
	NMB	940ZY	940 ZY
Bearing Lubrication		Andoc- C	
Aluminum Surface Coating		Alodine 1000 or equiv.	

Table 4-6 Mechanical components for spindle motor.

Notes to Table 4-6:

1. Bearings from different manufacturers cannot be mixed in the same motor.

4.1.6.2 Electrical Components

Lead Wire	Flex Circuit	
Winding Wire	Modified Polyester	(Base Coat)
	Polyamide	(Top Coat)
	Copper Molex 1mm pitch	
Mating Connector	JAE IL-402-04S-S1L-SA	

Table 4-7 Electrical components for spindle motor

4.1.7 Environment

	Operating	Non-Operating	Storage
Temperature	5°C to 55°C 41°F to 131°F	-40°C to 65°C -40°F to 149°F	-40°C to 65°C -40°F to 149°F
Humidity[1] Max wet bulb	10% to 90% RH 29°C 84.2°F	10% to 90% RH 38°C 100.4°F	
Shock	10 G 11 ms Half sine 30 G 3 ms	100 G 11 ms Half sine[2] 300 G 02 ms Half sine[2]	
Vibration (peak to peak)	1 G 5 - 300 Hz (P-P)	5 G 5 - 300 Hz (P-P)	

Table 4-8 Environment specifications for spindle motor

Notes to Table 4-8:

1. No condensation allowed.

2. With no loss of preload or change in acoustic noise.

4.1.8 Quality Assurance Provisions

Identification
All motors must carry a manufacturer's identification, a revision level, a part number, and manufacturing date code on protective bag.

Burn-in
4 hours at 60°C. (non-operating)

4.1.9 Cleanliness/Contamination

Motors must be free of dirt, burrs, and/or any other foreign materials. Motor should be sealed in individual bags, protected from moisture and ready for a class 100 clean room (See Appendix D).

4.2 VCM

The Europa VCM is a flat coil design which utilizes an encapsulated coil/rotor assembly. The rotor is balanced with a brass weight molded into the coil encapsulation. The four disk design has magnets on both the upper and lower magplates, while the two disk design only has magnets on the upper magplate with the lower magplate acting as a return path. This VCM design is based on the Daytona VCM with the difference being modifications made to accommodate the pushpin servowriter.

4.3 HGA

The Europa utilizes an extended swage plate suspension assembly in order to reduce the between disk spacing. The extended swage plate is swaged away from the disk area. This allows a thicker arm section on the e-block and allows better manufacturability during the swage process. A 50% slider will be used with an MR element for reading and an inductive element for writing. The addition of the MR element means there will be four wires per head. A tubeless design will be used for the head wires.

4.4 Maglatch

The Europa will use the same magnetic latch as used on Daytona.

4.5 Crash Stops

The Europa will use the same crash stops as used on Daytona.

4.6 FPCB

An "up and over" FPCB design will be used on the 4 disk Europa. An "up and over design" means that in addition to the FPCB sitting on the floor of the baseplate casting, the FPCB will have an additional fold coming over the top of the FPCB on the floor. This effectively doubles the size of the FPCB. A VTQFP (Very Thin Quad Flat Pack) will be used on the 4 disk pre-amp and a TQFP (Thin Quad Flat Pack) will be used on the 2 disk pre-amp. The length of wiring and trace length from the heads to the pre-amp is kept to a minimum on the Europa design. This is necessary in order to minimize the total inductance. The pre-amp being used requires the inductance to be kept to a minimum in order to maximize the bandwidth of the pre-amp circuit. Also, an attempt is made to maximize the amount of ground plane on the FPCB in order to help reduce noise.

4.7 Basecasting

The basecasting used on Europa is based on the Daytona design. Modifications to the casting have been made to accommodate the pushpin servowriter. These modifications include adding material to provide an area to machine a clockhead access hole on the side of the baseplate and moving some bosses to provide access for the pushpin through the bottom of the baseplate.

4.8 Top cover

The Europa top cover is based on the Daytona/Uzi top cover design. A slight modification is required (adding a notch on one side of the cover) to provide access to the clockhead hole on the baseplate. Stiffening ribs have been added to increase the rigidity of the top cover.

4.9 Ferro Fluid Seal

A conductive ferro fluid seal will be used on the spindle motor in order to provide a conductive path from the disks through the spindle. This will help to prevent a charge build up between the heads and the disks which could damage the MR elements on the heads. A Z-type seal will be used to provide a low profile ferro seal while maximizing the bearing spacing on the spindle motor.

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Section 5 Heads/Media

5.1 Heads/Media General Requirements

Operating Environment

Temperature	0° to 55° C (32° to 131° F)
Maximum Temperature Gradient	24° C/hr (43.2° F/hr)
Humidity	5 to 90% RH, non-condensing
Maximum Wet-Bulb Temperature	40° C (104° F)
Altitude	-200 to 3050 m
Cleanliness	Class 100
Stray Magnetic Field	< 25 Oe

Shipping and Storage Environment

Temperature	-40° to 75° C (-40° to 167° F)
Maximum Temperature Gradient	48°C/hr (118.4° F/hr)
Humidity	5 to 95% RH, non-condensing
Maximum Wet-Bulb Temperature	46° C (115° F)
Altitude	-200 to 12,192 m
Cleanliness	Class 100
Stray Magnetic Field	< 25 Oe

Test Environment

Temperature	23 ± 3° C (73 ± 5° F)
Humidity	30 to 70% RH, non-condensing
Altitude	0 to 914 m (0 to 3,000 ft)
Cleanliness	Class 100
Rotational speed	3800 rpm ± 5%
Stray Magnetic Field	< 6 Oe

Stiction/friction testing will be performed under the Operating environmental conditions.

Handling

The MR read sensor is sensitive to capacitive discharge at all times and ground straps (resistance $<10^6\ \Omega$) must be used when handling the device. Parts should only be handled with ESD-Safe tip tweezers or equivalent.

The MR read sensor is sensitive to corrosion and so the air bearing surface should only be cleaned with semiconductor grade isopropyl alcohol. No chemicals should be used on any part of the slider other than the air bearing surface.

Shipping container resistivity should be less than 10^{12} per square.

Zone Descriptions of Test Disk

Zone Radii

The applicable zone radii, shown in the table below are referenced to the gap of the active transducer.

Radius	mm	in.	Zone description	Skew at GAP	Slider C.G. Radius mm	Slider C.G. skew
R0	9.982	0.3930	Disk ID			
R1	11.900	0.4685	Clamping Zone OD			
R2	14.707	0.5790	Landing Zone ID	-1.01	14.707	-5.200
R3	**16.695**	**0.6573**	**Recording Zone - Z15(ID)**	**1.84**	**16.085**	**-1.737**
R4	17.564	0.6915	Recording Zone - Z14(ID)	2.99	16.931	-0.365
R5	18.433	0.7257	Recording Zone - Z13(ID)	4.09	17.779	0.937
R6	19.301	0.7599	Recording Zone - Z12(ID)	5.15	18.627	2.181
R7	20.170	0.7941	Recording Zone - Z11(ID)	6.18	19.477	3.374
R8	21.039	0.8283	Recording Zone - Z10(ID)	7.18	20.328	4.523
R9	21.908	0.8625	Recording Zone - Z 9(ID)	8.14	21.179	5.633
R10	22.776	0.8967	Recording Zone - Z 8(ID)	9.09	22.031	6.709
R11	**23.642**	**0.9352**	**Recording Zone - Z7(ID)**	**10.02**	**22.992**	**7.753**
R12	24.521	0.9654	Recording Zone - Z 6(ID)	10.93	23.745	8.785
R13	25.397	0.9999	Recording Zone - Z 5(ID)	11.84	24.606	9.791
R14	26.274	1.0344	Recording Zone - Z 4(ID)	12.72	25.468	10.777
R15	27.150	1.0689	Recording Zone - Z 3(ID)	13.60	26.330	10.744
R16	28.026	1.1034	Recording Zone - Z 2(ID)	14.47	27.193	12.695
R17	28.905	1.1380	Recording Zone - Z 1(ID)	15.32	28.059	13.634
R18	30.599	1.2047	Recording Zone - Z 0(ID)	16.96	29.728	15.411
R19	**30.658**	**1.2087**	**Recording Zone - Z0(OD)**	**17.01**	**29.870**	**15.471**
R20	30.851	1.2146	Disk OD			
R2 - R19			Flyable Zone			

5.2 Heads Mechanical Requirements

5.2.1 Slider Specifications

Transducer, Pole Tip Area, Face View

Method of Measurement
The measurement of the pole tip dimensions should be performed using a high power (1000X, 2000X-3000X preferred) optical microscope with electronic line-width measurement capability or measured magnetically on the spin stand (as noted).

Write Pole (WP2) Width*	4.0 ± 0.5 µm
Write Pole (WP2) Thickness	4.0 ± 0.4 µm (REF)
Write Gap	0.4 ± 0.05 µm (REF)
Read Gap	0.32 ± 0.05 µm (REF)
MR read width (magnetic measurement)	3.0 ± 0.4 µm
Write to Read Separation (the distance between centers of write and read gaps)	≤ 4.5 µm with Merged write/read design
Write to Read Offset (magnetic measurement)	0 ± 0.8 um at radius R11

* Pole width is measured at gap.

Transducer, Pole Tip Area, Profile View

Pole Tip Recession (Write and Read elements)	≤10 nm (≤ 0.4 µin)
Pole Tip Protrusion	None allowed

Turns for write head	10 to 15	
Leads	4	

Slider Dimensions

Length	2.000 ± 0.030 mm	(0.080 ± 0.001in)
Width	1.600 ± 0.030 mm	(0.0630 ± 0.001in)
Thickness	0.431 ± 0.050mm	(0.0170 ± 0.0019in)

ABS Rails

Width	constant flying height air bearing design	
Taper Angle	30 ± 15 minutes	
Taper Length	203 ± 50 µm	(.008 ± 0.002 in)
Bleed Slot Depth (REF)	27.9 ± 15.2 µm	(0.0011 ± 0.0006 in)
Bleed Slot Width (REF)	≥ 200 µm	(≥ .007 in)
Surface Finish	≤ 13 nm	(≤ 0.5 µin)
Crown (HGA level)	13 to 64 nm	(0.5 to 2.5 µin)
Camber (HGA level)	0 to 25 nm	(0 to 1 µin)
Flatness (HGA level)	≤ 20 nm	(≤ 0.8 µin)
Carbon overcoat (REF)	10 nm	(0.4 µin)

5.2.2 Head Load Force

Preload in nominal flying position	0.034 ± 0.0029 N (3.5 ± 0.35 grams force)

5.2.3 Z-Height

The z-height is to be 0.584 mm (0.023 in).

5.2.4 Flying Height

Innermost Track
With the transducer at radius R2, the disk rotating at 3800 rpm, and a skew angle of R3 degree at the gap, the following flying characteristics shall be achieved:

Nominal transducer rail clearance	76.2 ± 20.3 nm	(3.00 ± 0.80 µin)
Slider roll, trailing edges	25 ± 25 nm	(1 ± 1 µin)
Slider pitch, both rails	127 nm Min.	(5.0 µin Min.)

Outermost Track
With the transducer at radius R19, the disk rotating at 3800 rpm, and a skew angle of R19 degrees at the gap, the following flying characteristics shall be achieved:

Nominal transducer rail clearance	76.2 ± 20.3 nm	(3.00 ± 0.80 µin)
Slider roll, trailing edges	25 ± 25 nm	(1 ± 1 µin)
Slider pitch, both rails	380 nm	(15 µin) MAX

Minimum Flying Height
The minimum flying height of any point on either rail shall always exceed 55.9 nm (2.20 µin) at any disk radius in the Flyable Zone.

Maximum Flying Height
The flying height at the transducer shall never exceed 96.5 nm (3.8 µin)(REF.) at any disk radius in the Flyable Zone.

Flight-height measurements taken with equipment based on a Phasemetrics flying height transducer (or equivalent), with a spot size not to exceed 60 µm (0.0024 in), are acceptable when calibrated by a method and schedule approved by the equipment manufacturer.

5.2.5 Suspension

Hutchinson Technology Incorporated (HTI) P/N 0101321 for up facing heads & 0101323 for down facing heads. Prior written approval from Quantum is required to substitute a different part number or supplier.

5.2.6 Bond Strength

Slider -to-Flexure
The slider-to-flexure bond strength, when measured by a pull test shall be ≥ 70 gm.

Wire-to-Bond Pad
The single-wire wire-to-bond-pad bond strength, when measured by a pull test (after conformal coat is applied) at 30^0 from the bond-pad plane, shall be ≥ 17 gm.

5.2.7 Durability of the slider

Start/Stop Test

Procedure:
The test shall be performed for a minimum of **60,000 stop/start cycles** using a Test Disk. The head gap shall be positioned over the disk at radius R2 with 0° skew (at the gap). The disk speed shall be **3800 RPM ± 5%**. The acceleration and deceleration time shall be 9 ± 5 sec, with a minimum stop time between cycles of 3 sec. A 2.5 MHz data pattern shall be written prior to and after the 60,000 start/stop cycles.

Results:
The head shall have no apparent signs of wear or degradation. The readback amplitude at the completion of the test shall be > 90% of the original readback amplitude. Slider shall meet electrical performance specifications at all times during the test. The HF ID amplitude (with respect to either zone) shall change no more than 10% at any time during the test. Maximum coefficient of stiction between the disk surface and a head, measured at sampling rate of 2000 Hz, shall not exceed 0.8 after 60,000 start/stop cycles.

5.2.8 Slider Material

Aluminum Titanium Carbide

5.2.9 Durability of the MR Sensor

Accelerated Electromigration test
The MR sensor shall have resistance change less than 2% after 30 mA read current supplied for 20 hours at temperature of 25° C.

Minimum Breakdown Voltage between MR Head Sensor and Disk
The minimum breakdown voltage between MR head sensor and disk during contact shall be at least 3 Volts.

5.2.10 Wire (Tubeless)

Wire colors for MR read head and TF write head should be

	MR read head		TF write head	
Vendor	positive	negative	positive	negative
ALPS	Red	Green	Black	Black
AMC	Red	Green	Blue	Blue
RMM	Red	Green	Yellow	Yellow
TDK	Red	Green	Brown	Brown

Wire type to be gold plated copper alloy with triple-layer polyethylene coating.

Wire twist shall be 25 ± 3 turns/inch. The local variation, anywhere over the length, shall not exceed the average variation by more than 10%.

The wire insulation shall withstand temperatures up to 343° C (650° F) with no change in physical properties.

The wire insulation shall withstand wire tinning temperatures up to TBD° C (TBD° F).

The wire insulation shall not generate static electricity at the low temperatures of the operating, shipping, and storage conditions.

The wire gauge shall be 48.

5.3 Heads Static Electrical Characteristics

5.3.1 DC Resistance

The DC head resistance for MR read head, as measured between tinned portions of leads, shall be between 15 and 30Ω.

The DC head resistance for TF write head, as measured between tinned portions of leads, shall be $\leq$ 22 Ω.

5.3.2 Inductance

The inductance for MR read head at the wire terminals, when measured at 1 MHz, shall be $\leq$ 50 nH.

The inductance for TF write head at the wire terminals, when measured at 1 MHz, shall be $\leq$ 250 nH.

5.3.3 Hi-Pot Test

The resistance between the write coil winding or read element and any conductive part on the flexure assembly shall be > 10^5 Ω with 50 v DC applied. This is applicable with the head in either the loaded or unloaded position.

The breakdown voltage between the write coil and the pole tips must be greater than 300 v DC.

The resistance between the write coil winding and permalloy poles shall be > 10^5 Ω with 20 v DC applied.

The resistance across the slider-to-flexure bond shall be < 2 kΩ.

The resistance across the write coil and read element shall be > 10^5 Ω.

5.4 Heads Dynamic and Electrical Characteristics

5.4.1 Test Conditions

Test Environment
The test environment shall conform to Section 5.1 Test Environment.

DC Erasure
Unless otherwise specified, all write operations shall be preceded by a DC erase operation, and all read operations shall be preceded by a micro jog operation.

Test Frequencies

Recording Zone	Radius(inch)(ID)	LF (MHz)	HF (MHz)
Z -15	0.6573	2.13	8.50
Z -14	0.6915	2.24	8.94
Z -13	0.7257	2.35	9.39
Z -12	0.7599	2.46	9.83
Z -11	0.7941	2.57	10.27
Z -10	0.8283	2.68	10.71
Z - 9	0.8625	2.79	11.15
Z - 8	0.8967	2.90	11.60
Z - 7	0.9352	3.03	12.10
Z - 6	0.9654	3.12	12.49
Z - 5	0.9999	3.23	12.93
Z - 4	1.0344	3.35	13.38
Z - 3	1.0689	3.46	13.82
Z - 2	1.1034	3.57	14.27
Z - 1	1.1380	3.68	14.72
Z - 0	1.2087	3.91	15.65

5.4.2 Read/Write Electronics

Read/ Write Preamp

The read/write preamp shall be a SSI 2010R with a TBD external dampening resistor across the head. The total lumped and distributed capacitance across the head, excluding the preamp, shall be < 15 pF.

Write Current

The current amplitude measured at the head termination connector shall be 60 ± 2 mA p-p.

Waveform Asymmetry

The difference between any two positive and negative current pulses shall be ≤ 1 ns. That is, $|T1| - |T2| \leq |1\ ns|$. The risetime Tr and falltime Tf shall be < 5 ns.

Overshoot
5 % of Iw where $I_W = I_{W+} - I_{W-}$

DC Erase Current
The DC erase current shall be 60 ± 2 mA p-p.

Read bias current
The DC read bias current shall be 13 ± 0.5 mA.

Post-Amplification Frequency and Phase Characteristics
The frequency response, of any post-amplifier, shall be flat, to within ± 0.5 dB, to TBD MHz. The -3 dB rolloff point shall be TBD MHz. The attenuation above TBD MHz shall not be less than that given by a line drawn through 0 dB at TBD MHz with a slope of 18 dB/octave. The group delay shall be flat to within ± 2 ns over the range from 150 kHz to TBD MHz.

Transfer Characteristics
For inputs between 0.15 mV and 3 mV, the transfer characteristics shall be linear within ± 3%.

Processing Filters
For parametric measurements, a 5-pole Butterworth filter (f_{CO} = 100 MHz) is required. For bit shift measurements, a SSI 8001 programmable filters (f_{CO} = 13 Mhz, 13 dB Boost at Z0 , f_{CO} = 11 Mhz, 13 dB Boost at Z7 and f_{CO} = 9 Mhz, 8 dB Boost at Z15) are required .

5.5 Heads Acceptance Requirements

Track Average Amplitude (TAA)
Using a Test Disk, track average amplitude is defined as the average peak-to-peak amplitude over the entire track under test.

Amplitude
TAAHF ≥ 350 µV peak-to-peak at any track. See Section 5.4.1 for test frequencies.

Resolution
The resolution shall be > 65% for any track.

Overwrite
The overwrite shall be more negative than -32 dB for any radius.

Isolated Pulse Width
The average PW_{50} of the positive and negative isolated pulses shall be ≤ 450 nm at any radius.

Amplitude Asymmetry
The Amplitude Asymmetry shall be ≥ -15 % and ≤ 15 %.

Bit shift
The bit shift for a 10^{-7} BER, when written with a 80A0 NRZ pattern, shall be ≤ 11.8 ns (≥ 20% window margin) at radius R3, ≤ 8.3 ns (≥ 20% window margin) at radius R11, and ≤ 6.4 ns (≥ 20% window margin) at radius R19.

Write to Read Offset
0 ± 0.8 um at radius R11

Waveform Stability
One of the tests listed in this section should be used.

Sigma Amplitude
The sigma of the TAA_{HF} shall be ≤2.5% of the mean TAA_{HF} when TAA_{HF} is measured at any radius.

Sigma Bitshift
The sigma of the bitshift shall be less than 15% of the quantity described by (half window - mean bitshift).

Sigma Error Rate
Using a fixed window of 50% of half window, sigma of the log of the error rate shall not exceed 0.12 of the mean of the log of the error rate.

5.6 Heads Physical Defects

Refer to Europa Head Specification for detail information.

5.7 Heads Packaging Requirements

Current Requirements
Head packaging shall provide complete protection against physical damage, **electrostatic discharge**, or contamination. The packaging surface, both inside and outside, shall not accumulate static charge resulting in greater than 100 v of surface voltage. Any anti-static chemicals used must not degrade the Class 100 environment.

Production Requirements
For Head Packaging Instructions, see MKE P/N 48-70013301 (Down-facing), 48-70013401 (Up-facing)

5.8 Media Mechanical Requirements

5.8.1 Dimensions

Outside Diameter	65.00 ± 0.10mm (2.559 ± 0.004 in)
Inside Diameter	20.00 ± 0.05/-0.00 mm (0.787 ± 0.002/-0.000 in)
Concentricity of OD to ID	≤ 35 µm (0.001 4 in)
Thickness	0.635 ± 0.0125 mm (0.025 ± 0.0005 in)
Flatness	≤ 18 µm (0.0007 in) diametrical ≤ 35 µm (0.0014 in) circumferentially
OD Roundness	< 18 µm (0.0007 in)

Edge Condition
The outside and inside edges of the disk shall be chamfered to the following dimensions:

Angle:	45 ± 5 degrees
Length:	0.15 ± 0.08mm (0.006 ± 0.003 in)

Taper
The substrate thickness, measured on any radial line from OD to ID, shall at the OD be the same as the ID to within the tolerance +12.7/-51 µm (+0.0005/-0.002 in).

Dimensions are to be interpreted as per ANSI Y14.5.

Measurements are to be made at 23 ± 2° C (73 ± 4 °F)

5.8.2 Physical Characteristics

Surface Roughness

The axial surface roughness shall be measured with an optical profilometer.

Flyable Zone(Reference)
The arithmetic-average surface roughness shall be ≤5 nm (0.2 µin), with a maximum protrusion height of15 nm (0.6 µin) above the average.

Clamping Zone
The arithmetic-average surface roughness shall be ≤ 300 nm (11.8 µin), with a maximum protrusion height of 0.76 µm (30 µin) above the average.

Axial Runout, Velocity and Acceleration

Measurement Method
The axial runout, velocity and acceleration shall be measured within the Flyable Zone, at 3800 rpm ± 5%, with a disk clamping force of 500 N . The measurement method shall

use a non-contacting probe with an active diameter d_p, where 1.52 mm (0.060 in) $\leq d_p \leq$ 1.70 mm (0.067 in); and a 7.0 kHz low-pass filter with 18 dB/octave attenuation.

Axial Runout(PV)
The axial runout shall be ≤ 0.035 mm (0.0014 in) TIR and contained within the deflection limits given below.

Axial Deflection
The axial deflection at radius R6 shall be # ± 0.05 mm (0.002 in) from the reference plane defined by the lower clamping surface.

Axial Velocity	≤ 10 mm/sec (0.39 in/sec)
Axial Acceleration	≤8 mm/sec^2 (0.31 in/sec^2)
Moment of inertia	≤ 4.6x10^{-3} gm-m^2

Magnetic Requirements

Magnetic Material	CoNiCrPt or CoCrTa, CoNiCrTa
Coercivity	2000 ± 80 Oe (REF)
Circumferential Coercivity Variation	< 50 Oe
Remanence - Thickness Product	150 G-um (1.2 memc/cm^2) (REF)
Squareness (Br/Bs)	≥ 0.85 (REF)

Glide Height
In the Flyable Zone , there shall be no head-to-disk contacts when the head is flying at the flight heights shown below:

Disk Radii		Glide Height	
mm	in	µm	µin
TBD[1]- 30.83 (R1 - R19)	0.5818- 1.2140	0.038	1.5

1. Landing zone must be flyable.

Coefficient of Thermal Expansion
The coefficient of thermal expansion of the disk substrate material shall be 24 ± 1 x 10^{-6}/°C over a range of 10 to 57°C (13.3 ± 0.5 x 10^{-6}/°F over a range of 50 to 135°F)

Maximum Speed
The disk shall be capable of meeting all requirements after withstanding the effect of stress induced at a speed of 6000 RPM for 1 minute.

5.8.3 Clamping Zone

For all points on both surfaces in the Clamping Zone, the axial deviation from a flat plane shall be ≤ 3.6 µm (142 µin).

No identification, part, or serial numbers; logos; manufacturing identifiers; or similar information shall be placed in the Clamping Zone and must not affect flatness, load, or durability.

Both sides of the disk shall be electrically conductive.

5.8.4 Durability of the Magnetic Surfaces

Continuous-Running Wear Test

The disk shall withstand the effects of a Test Head gliding on the disk at 100 ± 2 rpm, at radius R6, for 48 hours. After completion of this test, any HF amplitude change due to disk wear shall be less than 10%.

Continuous Start Stop Test

The test shall be performed for a minimum of 60,000 stop/start cycles using a Test Head. The head gap shall be positioned over the disk at radius R3 with R3 skew. The disk speed shall be 3800 rpm ± 5%. The acceleration and deceleration time shall be 25 ± 5 sec, with a minimum stop time between cycles of 3 sec. A 5.63 MHz data pattern shall be written prior to and after the 60,000 start/stop cycles.

Results:
The disk shall have no apparent signs of wear or degradation. The readback amplitude at the completion of the test shall be > 90% of the original readback amplitude.

5.8.5 Overcoat and Friction of Magnetic Surfaces

Overcoat of the Magnetic Surface

Overcoat Material
The disk overcoat material shall be sputtered Hydrogenated carbon or Quantum-approved alternative. Once Supplier becomes qualified, Supplier must obtain prior written authorization from Quantum for any change in overcoat, lubricant and/or application process.

Overcoat Thickness
20 ± 3 nm (0.8 ± 0.12 µin) for carbon (REF)

Overcoat Durability
The top coat shall be able to withstand the operating and storage and the durability requirements.

Lubricant
The disk shall have a Quantum-approved lubricant. Supplier will be required to submit to Quantum a full disclosure of the lubricant type, composition, and application

process. Once Supplier becomes qualified, Supplier must obtain prior written authorization from Quantum for any change in lubricant and/or application process.

Lubricant Life
The lubricant shall remain on and adequately lubricate the disk for at least 5 years.

Head/Disk Friction

Test Requirements
The coefficient of friction between the disk surface and a head, the test method, and the methods of calculation are described in ANSI X3B7/88-02, and shall be performed over the entire Flyable Zone, and for any operating or storage condition .

Dynamic Friction Coefficient
The dynamic friction coefficient shall not exceed 0.3 using a Test Head with a 3.5 gm load.

Stiction
The measurement shall be made with a Test Head which has a 3.5 gm preload. The static friction coefficient shall not exceed 0.5 after contact for 24 hours, and shall not exceed 1.0 after any time period and after 80,000 contact start/stop cycles with 90% confidence.

5.9 Media Acceptance Requirements

Track Average Amplitude (TAA)
Using a Test Disk, track average amplitude is defined as the average peak-to-peak amplitude over the entire track under test.

Amplitude
$TAA_{HF} \geq 350\ \mu V$ at any radius within the GUARANTEED DATA Zone.

Resolution
The resolution shall be > 65 % for any radius.

Overwrite
OVWT shall be more negative than -32dB at any radius.

PW50
PW50 $\leq$ 450 nm at radius .

Residual Noise
The media residual noise ratio shall not be more positive than -28dB at any radius.

Positive Modulation
No positive modulation shall be allowed within the GUARANTEED DATA Zone.

Negative Modulation
No negative modulation shall be allowed within the GUARANTEED DATA Zone.

Bit shift
The bit shift for a 10^{-7} BER, when written with a 80A0 NRZ pattern, shall be ≤ 11.8 ns (≥ 20% window margin) at radius R3, ≤ 8.3 ns (≥ 20% window margin) at radius R11, and ≤ 6.4 ns (≥ 20% window margin) at radius R19.

5.10 Defects

Definition
A defect is physical imperfection on the disk that causes either an extra or a missing pulse in the Recording Zones.

There shall be ≤ 60 defects per surface and the length of any one defect shall not exceed 15 bytes when using the test frequencies.

Defect scanning shall be performed at a maximum track-to-track Test-Head step increment of 4.7 µm (189 µin).

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Section 6 Drive Electronics

6.1 Read Channel Lite

The Lite chip is Quantum's first fully integrated partial-response maximum-likelihood (PRML) recording channel. It combines the functions of the Rocky and the Bullwinkle chip set used in Empire+ drive, with a target power consumption of 600 mW at 60 MHz channel rate. Low power is achieved by novel analog circuitry, by reducing the speed of key digital circuits, and by running the digital portion at 3.3 V. (the digital portion can also run at 5 V. with increased performance, but at a higher power). The Lite channel supports user rates from 17.78 to 53.33 Mbits/sec (20 to 60 MHz channel rate.)

Lite includes hardware that allows drive self-optimization and conforms to AT&T's Shiva interface specifications.

6.1.1 Lite Digital Description:

The digital portion of Lite is based on the Rocky architecture, but includes fundamental changes in order to achieve the desired low power goal. The major changes are a more compact CPU, new timing loop circuitry, simplified gain loop circuitry, 5-tap FIR filter and reduced adaptation logic, a pole-tip filter to counteract the effects of thin-film heads, an offset loop to adjust for signal d.c. offsets up to 16 lsbs, an enhanced register file including the ability to read back final loop values and to bypass all control loops, and a 3-wire serial interface to reduce pin count. The changes also include a new clock generation block with circuitry to enable and disable individual clock signals. Lite also includes a mean-squared error (MSE) block used to optimize channel performance, thermal asperity compensation circuitry, and an on-board viewing dac for ease of debugging.

6.1.2 Lite Digital Functional Description:

The digital portion of the Lite chip can be divided into 20 main blocks:

- Input multiplexer for digital debug
- FIR filter for digital signal shaping
- PTF filter for thin film head undershoot cancellation
- Viterbi detector for maximum-likelihood detection
- Postcoder for conversion back to NRZ
- Timing loop for timing synchronization
- Offset loop for d.c. offset control
- Gain loop for signal amplitude control
- Equalizer loop for self adaptation
- AM detect for byte boundary synchronization
- Serializer/Deserializer for NRZ interface and encode/decode
- Precoder for inverse channel function
- FIR Training for FIR filter optimization
- MSE for overall channel optimization
- Clock deglitch for switching between read and write clocks
- Clock generator for gated clock implementation
- CPU for chip control
- Register file for chip programming
- Test multiplexer for digital debug
- Viewing DAC for ease of debug

In read mode data is received from the analog-to-digital converter in the analog side of Lite through the input multiplexer and equalized with the 5-tap FIR filter and the pole-tip filter. The PTF can be bypassed and its clock disabled for products with MR heads. All the necessary blocks are enabled by the clock generation block. The timing, gain, and offset loops compute the required adjustments and send the corrections back to the analog side of Lite. The equalization block (FCA) has the ability to update the FIR coefficients. The adaptation rate can be programmed to be from every 2 to 8 cycles. The Viterbi detector performs maximum-likelihood detection on the samples and its output is sent through the postcoder and to the serdes block. After detection of the address mark, the detected data is decoded and converted into a 2-bit wide stream, which is sent to the controller.

In write mode just the blocks needed are enabled. The 2-bit wide user data stream is encoded and serialized in the serdes block and sent to the precoder. The precoded data is sent to the analog side of Lite to be precompensated. Lite writes it's own preamble and sync byte, according to the Shiva interface. Another feature of Lite is that the encoder can be bypassed, allowing the user to write any desired pattern. Lite can be also programmed to write DC, preamble pattern, or a 127-bit pseudorandom sequence.

The digital portion of Lite is controlled by a state machine called the CPU. It selects the different modes of the chip based on external pin signals (i.e. read gate, etc.) and the contents of the register file. The test multiplexer block allows for capturing various signals internal to the chip using a logic analyzer. The test multiplexer can be activated during read and write modes.

The digital portion of Lite has been designed to be tested independently of the analog side. Test mode is enabled by setting a bit in the register file. This bit enables the data input pins (SD[5:0]) and the external clock pin (MCLK), bypassing the analog-to-digital converter and the internal clock source. The onboard digital-to-analog converter can be used for real-time debug. It's input is connected to the six most significant test mode pins (TST[9:4].)

Lite also includes a multiple purpose block called MSE, which is short for mean-squared-error, to be used for system optimization. Actually, there is no squaring operation. The MSE is composed of a multiplexer, a quantizer, and an accumulator. The MSE accumulates the absolute value of the error between the actual samples and it's expected value. The smaller the MSE number, the better the system will perform. MSE can be programmed to get sampled from the FIR input (A/D samples), FIR output, and PTF output (for PTF optimization). There is also a special mode where the MSE block counts errors between the Viterbi detector and a threshold detector. The usefulness of this feature is yet to be tested. Another mode of operation for the MSE block is it's ability to count errors derived from either one of the three PR4 levels. This is useful for optimization of write precompensation using a special pattern and for measuring MR head asymmetry.

Lite also contains special circuitry to partially counteract the effect of thermal asperities that are generated when the MR element collides with surface defects or debris. When thermal asperity mode is enabled, the A/D range is effectively doubled by reducing the signal gain by half. If a thermal asperity is detected, the gain and timing loops are frozen for the duration of the event.

6.1.3 Lite Digital Specification:

- Maximum voltage: 3.6 V.
- Minimum voltage: 3.0 V.
- Nominal voltage: 3.3 V.
- Peak power for digital portion: 270 mW @ 3.6 V, 53 Mbps, adaptive read mode
- Max channel rate: 60 MHz (53 Mbps)
- Min channel rate: 20 MHz (17 Mbps)
- Package: 80 pin VQFP (14mm x 14mm x 1.27 mm)
- Part number: 14-106704-02

6.1.4 Lite Digital block diagram

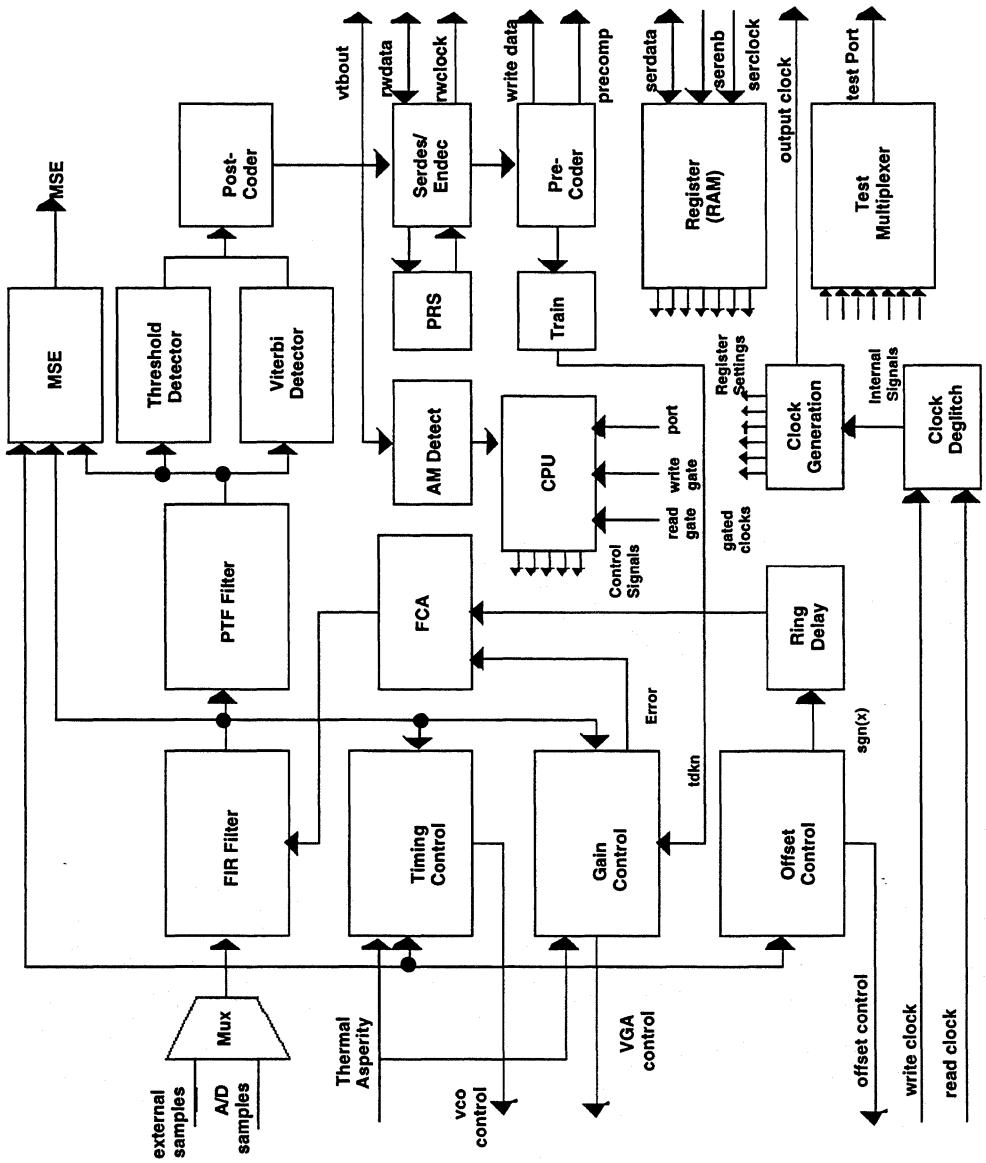


Figure 6-1 Lite Digital Block Diagram

6.1.5 Lite Analog Description:

The analog portion of this ASIC is used to process read and write data for a magnetic recording interface. It contains amplitude and timing referencing and control systems, analog signal filtering, servo signal processing, frequency synthesis and analog-to-digital conversion blocks.

This implementation defines minimal time-averaged power consumption as a major priority. All functional blocks have power management capability and quickly recover from *sleep* mode. This ASIC system runs on nominal Vdd supplies of 5.0 VDC for the digital section and 5.0 VDC for the analog section. This ASIC system also runs on nominal Vdd supplies of 3.3 VDC for the digital section, 5.0 VDC for the analog section and 5.0 VDC for the I/O function. Timing, amplitude and speed-related specifications do not degrade as the supply voltage is increased from 3.3 to 5.0 VDC.

6.1.6 Lite Analog Performance Characteristics

Test Parameter	Test Condition	Min.	Nominal	Max.
Analog Supply voltage		4.5 volts	5.0 volts	5.5 volts
DigitalSupply voltage		3.0 volts	3.3 volts	3.6 volts
I/O Supply voltage		4.5 volts	5.0 volts	5.5 volts
Analog Power consumption	absolute maximum all systems in "Read Mode"			306 mW
A/D clock rate		20 MHz		60 MHz
Operating Temp		0°C		70°C

Table 6-1 Lite Analog Performance for Mixed Volt Operation

Test Parameter	Test Condition	Min.	Nominal	Max.
Analog Supply voltage		4.5 volts	5.0 volts	5.5 volts
DigitalSupply voltage		3.0 volts	3.3 volts	3.6 volts
I/O Supply voltage		4.5 volts	5.0 volts	5.5 volts
Analog Power consumption	absolute maximum all systems in "Read Mode"			306 mW
A/D clock rate		≥20 MHz		≥60 MHz
Operating Temp		0°C		70°C

Table 6-2 Lite Analog Performance for 5 Volt Operation

Notes to Table 6-1, 6-2:

All defined minimums and maximums in the following electrical performance specification tables are "worst case" performance unless otherwise noted. "Worst case" performance is to be met under "worst case" conditions for that particular parameter, where the conditions are any valid combination of temperature, voltage, time and process defined for this chip.

6.1.7 Lite Analog Functional Description:

The analog portion of the Lite chip can be divided into 11 main blocks:

- Analog Control Block
  Controls read/write/servo/idle mode states for the analog blocks
  Controls power up/down states
  Controls test mux

- Variable Gain Amplifier
  Triple impedance front end- squelch, open and read mode
  DAC control of gain level during data mode
  Analog AGC control of gain level during servo mode
  Gain versus control voltage function is exponential
  Gain hold function for analog mode
  Fully differential signal paths
  No external components

- Signal Filter
  Fully differential signal paths
  High pass filter in the LPF data path for DC offset cancellation
  Separate control registers for Servo and Data modes
  No external components

- Offset Control
  DAC control of DC level during data mode
  7 bit 2's complement real time control
  ±16 lsb range
  No external components

- Analog to Digital Converter
  6-bit flash architecture
  5.25-bit worst case resolution
  100 mW worst case power
  Guaranteed monotonic non decreasing slope
  Differential signal input
  No external components

- Zero Phase Restart & Voltage Controlled Oscillator
  Zero Phase Restart triggered on normal LPF data
  0° to 360° phase delay after initial ZPR detect
  8 bits for fine VCO control
  No external components

- Frequency Synthesizer
  - Temperature & V_{dd} compensated
  - 5 bits for M
  - 6 bits for N
  - Current-mode control of slaves
  - No external components

- Write Data Precompensation
  - TTL - level single-ended output
  - PECL - level differential output
  - Level-sensitive or Edge-sensitive output
  - Internal VCO used to develop delay
  - Fundamental delay proportional to T_{system}
  - Actual delay proportional to 4-bit control register setting
  - No external components

- Analog Servo AGC
  - Settle time to 1% of ±4dB step is 7 peaks of full wave rectifier data
  - Symmetrical attack and decay envelopes
  - Exponential attack / decay rates
  - Decay qualified by minimum amplitude threshold on analog input
  - Differential signal path through the full wave rectifier
  - External voltage reference input for servo ADC range matching
  - No external components

- Servo Peak Detector
  - Threshold adjustable from 20% to 80% in 4% steps (4 bits)
  - Polarity qualification available
  - Polarity signal available

- Servo Sample and Holds
  - 32 selectable charge rates
  - Charge rate dynamic range 1:48
  - Exponential charge slope (g_m/C)
  - 3-Wire control
  - No external components

ADDRESS	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
17 (23)	FIR0	X	X	w0	w0	w0	w0	w0	w0	FIR coefficients
18 (24)	FIR1	X	X	w1	w1	w1	w1	w1	w1	
19 (25)	FIR2	X	X	w2	w2	w2	w2	w2	w2	
1A (26)	FIR3	X	X	w3	w3	w3	w3	w3	w3	
1B (27)	FIR4	X	X	w4	w4	w4	w4	w4	w4	
1C (28)	SELECT	thrvtbn	msesel[1]	msesel[0]	signalsel[1]	signalsel[0]	clksel[2]	clksel[1]	clksel[0]	thrvtbn: Choose Viterbi or threshold detector msesel[1:0]: selects what levels to include in MSE calculation 00 -> middle 01 -> top 10 -> bottom 11 -> all signalsel[1:0]: Selects on what signal to measure MSE 00 -> A/D output 01 -> FIR output 10 -> PTF output 11 -> detector miscompare error clksel: Selects what internal clock is sent to output pin.
1D (29)	DKVTB	X	X	dkval5	dkval4	dkval3	dkval2	dkval1	dkval0	PRML ternary levels for Viterbi (nominal 010000)
1E (30)	DMAP	periodenb	endecbypass	rwclkenb	thrmap[4]	thrmap[3]	thrmap[2]	thrmap[1]	thrmap[0]	periodenb: periodicity chacker enable (only in adaptive or training) endecbypass: bypass endec and precoder rwclkenb: enable rwclk to stay on all the time thrmap[4:0]: absolute threshold value for defect map detector.
1F (31)	AGCVAL	X	X	agcval5	agcval4	agcval3	acgval2	agcval1	agcval0	agcval5-0: gain control loop value at end of read
20 (32)	VCOVAL	vcoval7	vcoval6	vcoval5	vcoval4	vcoval3	vcoval2	vcoval1	vcoval0	vcoval7-0: vco control loop value at end of read
21 (33)	TIMING0	tswenb	X	n2	n2	n2	n1	n1	n1	tswenb: enable timing loopswitching from input to output of FIR filter Timing step size (acquisition) $\alpha = 2^{-n2} + 2^{-n1}$
22 (34)	TIMING1	Azfreqn	Tzfreqn	n4	n4	n4	n3	n3	n3	Timing step size (tracking) $\alpha = 2^{n4} + 2^{n3}$ Azfreqn: zero frequency term during acquisition Tzfreqn: zero frequency term during tracking
23 (35)	TIMING2	m4	m4	m3	m3	m2	m2	m1	m1	Timing step size (tracking) $\beta = 2^{-m4} + 2^{-m3}$ Timing step size (acquisition) $\beta = 2^{-m2} + 2^{-m1}$
24 (36)	GAIN0	inittmn	Trkhold	p2	p2	p2	p1	p1	p1	p1: gain step size (acquisition) $\gamma = 2^{-p1}$ p2: gain step size (tracking) $\gamma = 2^{-p2}$ inittmn: reset test mux and power down VIEW DAC Trkhold: hold gain during tracking in adaptive and training modes
25 (37)	FCA0	prcval1	prcval0	r1	r1	r1	r2	r2	r2	r1: FCA step size (FIR acq) r2: FCA step size (FIR tracking) prcval: precoder initial condition
26 (38)	ACQDONE	X	X	acqdone5	acqdone4	acqdone3	ackdone2	acqdone1	acqdone0	AcqDOne5-0: Acquisition length in bytes
27 (39)	TRNCOUNT	trncnt7	trncnt6	trncnt5	trncnt4	trncnt3	trncnt2	trncnt1	trncnt0	Length of training field in bytes
28 (40)	MISC0	TAenb	Tstmode	SerDatPU	RWDatPU	t1	t1	TholdEnX	ScramEn	TAen: Thermal asperity mode enable Tstmode: enables test mode SerDatPU: enables weak pull-up RWDatPU: enables weak pull-up t1: Offset loop step size TholdEn: Timing hold enable (not implemented) ScramEn: Scrambler enable

Figure 6-2 Lite Digital Register Associations

6.1.8 Lite Analog block diagram

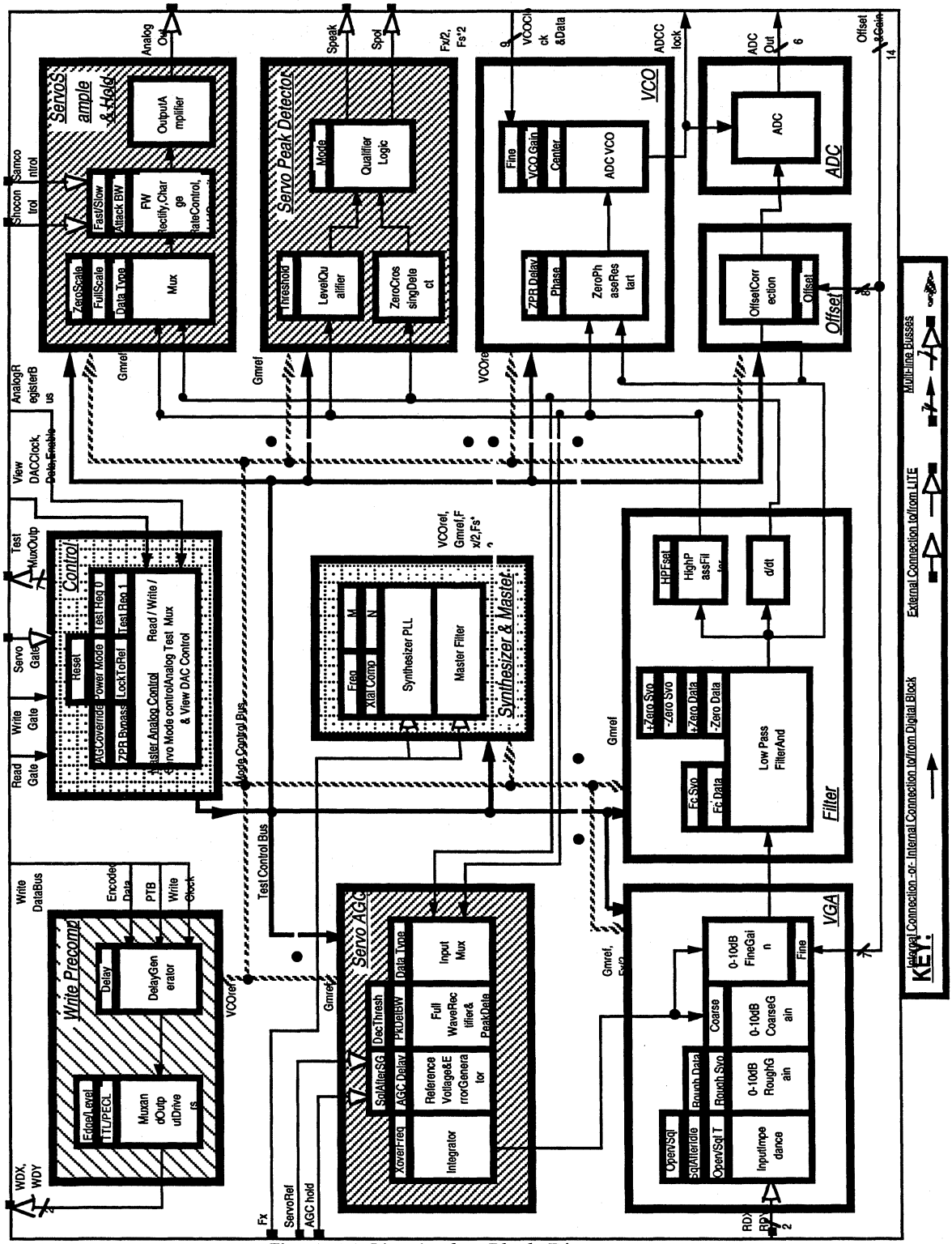


Figure 6-3 Lite Analog Block Diagram

6.2 Preamp

6.2.1 General Specifications

The QMP911 is a read/write preamplifier designed specifically for a combination magnetoresistive read transducer and a thin film writer. The primary transducer that is intended for use with this preamp is a SAL MR. The preamp architecture is a current bias current sense device. Due to this architecture the impedance is very low, in the order of 5 ohms when in operation, as compared to the traditional high input impedance preamplifiers used with thin film heads.

The writer is differential but the reader is single ended. One side of the MR reader is the positive connection while the other side of the reader is the grounded connection, internal to the preamp. There are a total of four lead connections per head, two for the writer and two for the reader. The bias current is programmable between 10-20 mA using an external resistor. The write current is also programmable between 10-40mA (b-p) using an external resistor.

The device has a fast recovery circuit to handle thermal asperities as well as MR head shorting. There are two control pins to enable/disable the thermal asperity and MR head short detection circuitry. This recovery circuit is also implemented for the head select and R/W or W/R recovery. The preamplifier does not remove thermal asperities from the signal.

6.2.2 Features

- Current Bias/Current Sense architecture
- Operates from a single +5V supply, (±10%)
- Low power idle mode
- 4 and 8 channel capacity
- Dual input to reader with one side grounded internally
- True differential output
- Wide MR resistance range: rmr = 15Ω to 30Ω
- Programmable bias current: 10 to 20mA
- Minimum gain of 200V/V @ rmr = 30Ω
- Bandwidth, BW = 50MHz, Min. BW @ 0dB is 45MHz
- Equivalent input noise, Vnoise = 0.65 nV/root Hz @ rmr = 30Ω
- Programmable write current: Iw = 10mA to 40mA (base to peak), Lw = 200nH & Rw = 15Ω
- Write current rise time = 5.5ns (Lw = 200 nH, Iw = 40mA, F = 40MHz)
- Fast Recovery Times:
  - Head select <1.2 µsec nominal, 2.0 µsec max.
  - Write to read recovery <1.2 µsec nominal, 2.0µsec max.
  - Read to write recovery <1.2µsec nominal, 2.0µsec max.

Input Capacitance <15pF for both reader and writer

- Preamp to tolerate input inductance, L_{series} - 105 to 110nH nominal
- Multichannel servo write
- Read and write fault detection
- MR head protection, excessive MR bias current
- Thermal asperity/Capacitive discharge protection. Programmable on/off
- PECL inputs for WDX and WDY
- Channel separation 45dB at all frequencies
- PSRR -36dB at 25 MHz
- CMRR -36dB at 25MHz
- A prebias circuit for the MR sensor while in write mode
- Input control lines to include:
  - Head select, HS0 through HS2 with internal pull-down resistors
  - Bias voltage, Vbias, Programmable
  - R/-W with internal pull-up resistors
  - -CS with internal pull-up resistors
  - Thermal asperity/Capacitive discharge protection, Enable/disable
- Output lines to include
  - Read and write fault to include thermal asperities and head short
- Plastic TQFP package

6.3 Microcontroller

The NEC μPD787012 and μPD78P7012 are members of the K-Series of microcontrollers. These 32-/16-bit devices with a minimum instruction time of 60 ns at 33MHz are designed for high-speed real-time process control.

6.3.1 Features

- High speed instruction execution by pipeline processing: 60.0 ns at internal 33 MHz
- Clock multiplex function (PLL): can be operated at 6.6 MHz(external)/ 33 MHz(internal)
- General purpose register architecture
  - High orthogonality /symmertricalness instruction set
- High speed multiplication (dedicated hardware incorporated)
  - 16 bits x 16 bits (signed) Multiply in 6 clocks
  - 40 bits + 16 bits x 16 bits (signed) Multiply in 6 clocks
- Instructions for high performance control
  - Powerful instructions for product sum operation
- Enhanced bit manipulation instructions important in control field
- Powerful set of addressing modes improving compiler efficiency for high level language
  - Fourteen addressing modes for operand address
- Wide memory space
  - Program/data: 16 Mbyte, linear addressing
- Expanded short direct address space with high operability : 1Kbyte
- Variety of general purpose registers: 512 bytes incorporated
  - 32 bit x 8 registers x 16 banks
  - 16 bit x 16 registers x 16 banks
  - 8 bit x 16 registers x 16 banks
- Future improvement oriented instruction set
  - Instruction set fully compatible with 78K/III and 78K/VI series

6.3.2 Overall of K7 Address Map

K7ADDRESS	USAGE	DRAM ADDRESS
FFFFFF FFF000	4K SFR	FFFB00 - FFFCFF Resides here CPU Internal
FFEFFF FFE000	4K Internal RAM space (1K used now) Varibles & Tables	
FFDFFF FF8400	23K DRAM Tables & varibles	7DFFF-78400 *
FF83FF FF8000	1K ASIC registers (16 bit only)	FF8000 - FF81FF Expandable with ASIC Change
FF7FFF FF0000	• 32K DRAM Variables	77FFF-70000
FEFFFF FE0000	1K ASIC registers (8 bit only)	FEFB00 - FEFCFF
FDFFFF FD0000	+ 64K External SRAM or EPROM	
FCFFFF FC0000	+ 64K External SRAM or EPROM	
FBFFFF FB0000	+ 64K External SRAM or EPROM	
FAFFFF FA0000	+ 64K External SRAM or EPROM	
F9FFFF F90000	+ 64K External SRAM or EPROM	
F8FFFF F80000	+ 64K External SRAM or EPROM	
F7FFFF F00000	• 512K Mirror of F80000- FFFFFF	
EFFFFF 800000	• 7168K Mirror of F00000- FFFFFF	
7FFFF 200000	• 6144K Mirror of 000000- 1FFFFF	
1FFFFF 180000	• 512K Mirror of 100000- 17FFFF	
17FFFF 170000	64K DRAM Tables & Varibles	7FFFF 70000
16FFFF 160000	64K DRAM code	6FFFF 60000
15FFFF 150000	64K DRAM Buffer	5FFFF 50000
14FFFF 140000	64K DRAM Buffer	4FFFF 40000
13FFFF 130000	64K DRAM Buffer	3FFFF 30000
12FFFF 120000	64K DRAM Buffer	2FFFF 20000
11FFFF 110000	64K DRAM Buffer	1FFFF 10000
10FFFF 100000	64K DRAM Buffer	0FFFF 00000
0FFFFF 010000	• 960K Mirror of 000000-0FFFFF	
00FFFF 008000	32K DRAM	0FFFF 08000
07FFF 000000	32K Internal ROM space	

Table 6-3 K7 Address map

Notes to Table 6-3:

1. • Unused, alternate DRAM access area
2. + Unused, available for external memory
3. * Allows for local jump (±32K) from Internal ROM space for Variables and Tables
4. Four High order address bits required Bit 23 = 1 => stack and ASIC
   Bit 23 = 0 => DRAM
   Bit[18-16] decode the 8 64K pages of DRAM.

6.3.3 Difference between K7 vs K3

	K7	K3
State clock	Up to 33.33 MHz	20 MHz
Power	375 mW	375 mW
Signed Multiply	6 clks	14 clks
Sat- MAC	9 clks	26 clks (no sat)
Internal RAM	1 Kbyte	640 byte
External Bus size	8/16 bit	8 bit
Code size	1.25	1.0
Package	100 pin QFP	64 pin QFP
Cost (94-95)	550-530 Yen	580-520 Yen

Table 6-4 Difference between K7 vs K3

6.4 ASIC

The NEPTUNE is a CMOS VLSI component that combines a programmable RAM-base disk formatter, the high bandwidth Buffer Controller, and a host interface for both ATA and SCSI standards. It is based on the same netlist as the LEO ASIC used in the Fireball drive. Only the pinouts have been changed to accommodate the inward-facing PCB used in 2.5" drives.

The NEPTUNE has power saving features built in, it provides an automatic low-power dynamic mode to stop transactions on the ATA or SCSI bus, as well as stopping internal clock in each separate block or shut off internal clock completely in sleep mode.

The NEPTUNE combined from 10 main blocks:

- Host Interface (AT) or (SCSI) module
- Buffer Control (BFR) module
- Motor Interface (MTR) module
- Analog to Digital Converter (ADC) module
- Servo Control (TNA) module
- Serial Interface (SER) module
- Microprocessor Interface (UPI) module
- Sequencer Control (SEQ) module
- Error Correction Control (ECC) module
- Top Test (TST) module

6.4.1 Capabilities and Features

6.4.1.1 Host Interface

ATA Standard Interface

- Supports ATA Standards Interface
- On-chip 24mA drivers
- 16 bit wide fast DMA transfer on host bus up to 16-20 Mbytes/sec
- Supports Auto Functions
- LBA and CHS support
- Transfer rate: 8 Mb/s in sustained mode and 20 Mb/s in burst mode

6.4.1.2 Embedded Servo

- Generates control signals for burst amplitude measurement
- Support tri-burst and quad-burst servo wedge
- SAM: 14T or 9T programmable
- Detects necessary syncs 2T vs 3T in wedge area
- Keep wedge high in find mode until locked
- Read tracks number in wedge area
- Supports Thermal Asperity logic

6.4.1.3 DRAM Buffer Interface

- Support 64K x 16 or 256K x16 DRAM, no parity
- Bufferware, uP firmware executes from the DRAM buffer memory
- CPU direct access, uP accesses directly from the DRAM buffer memory
- Wait state control
- 32 Mbytes/s maximum buffer bandwidth
- 12 Mbytes/s maximum disk channel bandwidth
- 10 Mbytes/s maximum host channel bandwidth

6.4.1.4 Control Disk Read/Write

- Generates Readgate, Write gate, etc. for R/W component
- 2 bit wide decoded data "Shiva" type interface
- RAM based control store (30 bits x 36 words)
  - Handles split data fields for constant rate servo wedges in multiple zone drives
  - No microprocessor intervention needed for up to full track read/write
  - Format information (where variable breaks for sector are) contained in the headers
- ID after wedge
- 24 bit CRC and Triple burst with 160 bit REED-SOLOMON ECC algorithm, allows "ECC on-the-fly"

6.4.1.5 Microprocessor Functions

- Supports K7 NEC Microprocessors
- Single Crystal architecture use for both system and Microprocessor clocks
- Memory mapping allows access to full DRAM
- Demuxes MAD bus
- Generates different clock rates, allows clocks to be slowed or stopped for power conserving modes

6.4.1.6 Serial Interface Functions

- Serial interface with Read and Write mode to R/W and spindle, VCM driver
- Allows 10, 20 and 40 MHz operating modes

6.4.1.7 Analog to Digital Converter Functions

- Successive approximation type 8 bits A/D Converter, 3.3 usec conversion time, linearity ± 1/2 LSB, with power down mode
- Supports new Read channel " Shiva" interface

6.5 DRAM

A 1 Mbit 80 nS Fast Page Mode DRAM in a 64 K x 16 organization with upper and lower write enable packaged in a 40 pin SOJ.

Address map in LEO Specification.

6.6 Motor/VCM

The TLS2205 (Peachfuzz) is a combination voice-coil and spindle-motor driver with voltage monitor integrated circuit. This circuit is designed for small-form-factor, high-performance hard disk drives. The TLS2205 integrates a three-phase brushless dc motor driver with a linear full-bridge voice-coil driver. Additional circuitry is added for power-up and power-down sequencing of the driver amplifiers used for motor speed control. A brake function can be invoked on the spindle motor after the head is in a safe landing zone. External sense resistors are used for precision spindle motor and VCM current monitoring. Automatic head retract is provided for voltage or thermal fault conditions.

VCM

- ±0.4 A MOS H-Bridge Power Amplifier
- No Crossover Distortion
- Precision VCM Control Loop with External Sense Resistor
- Internal 8-Bit Control DAC with Four Gain Ranges
- Controlled-Velocity Head Retract
- Compensation Adjust Terminals for Bandwidth Control
- Capability for External Velocity Feedback
- Low $r_{DS\ (on)}$, 2 Ω Total
- No External Retract Power Supply Isolation Components Required

Spindle-Motor

- Hall- or Back-EMF Commutation Circuitry
- 3-Phase Driver with 1.3A MOS Output
- Programmable Frequency-Locked Speed Control Loop
- Bipolar or Unipolar Driver Modes
- Programmable Start-Up Current
- Internal Schottky Diodes for Retract Power Source
- Linear Spindle Current Control
- Low $r_{DS\ (on)}$, 1.3 Ω Total
- Controlled Brake Function
- Speed Sense Tachometer Output
- Sector Data Tachometer Signal Input (Optional)

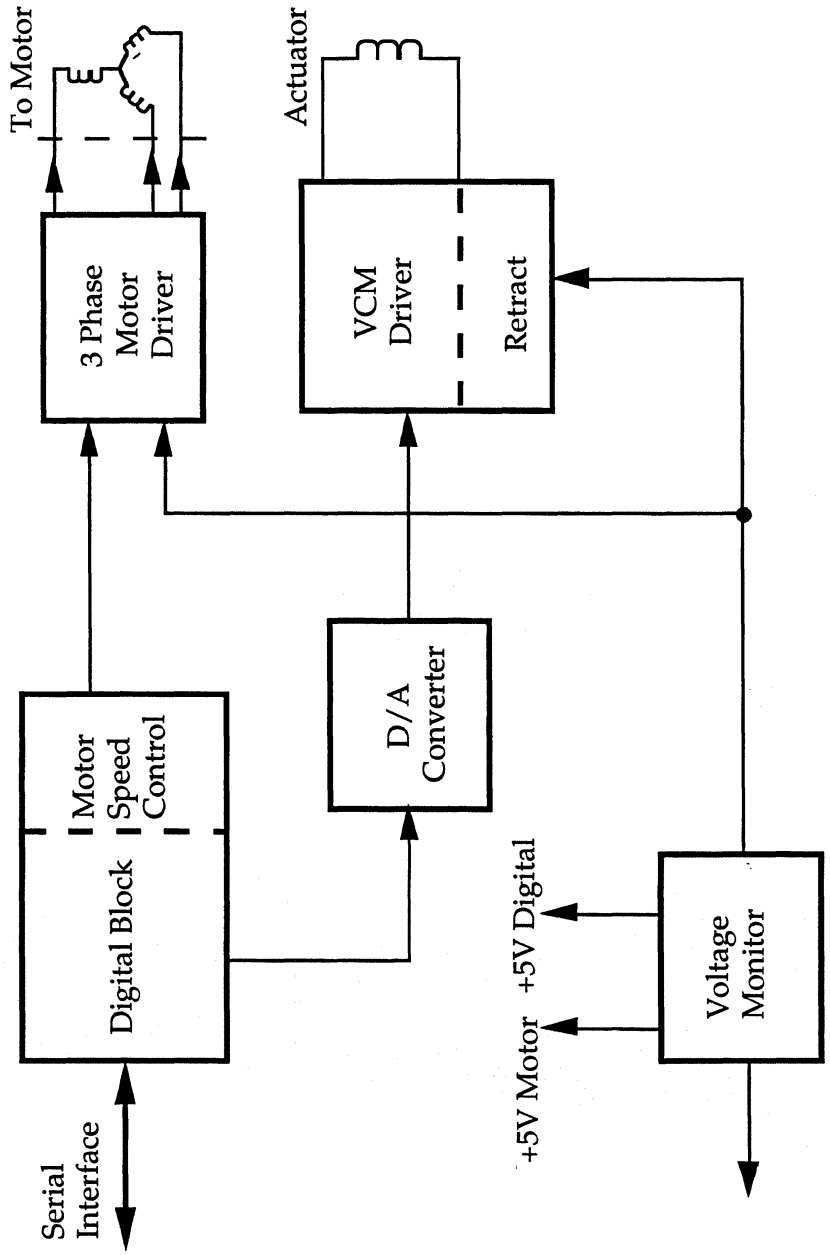


Figure 6-4 VCM/Motor TLS2205 Block Diagram

6.7 PCB

6.7.1 PCB Layout Consideration

PCB consists of four layers: a component/signal plane, a +5V power plane , a ground plane and a signal plane. PCB has components only on one side. The four layer design provides an opportunity to:

6.7.1 Separate high frequency clock signals and other high current traces from noise-sensitive low amplitude analog signals such as readback signals.

6.7.2 Shield high frequency digital signals so as to reduce the energy dissipated by RFI emissions.

6.7.3 Provide ample ground planes for better ESD protection.

6.7.4 Use wide voltage and ground planes to prevent current loops that creates impedance difference between the power supplies and various parts of the PCB.

6.7.5 Provide adequate heatsinking capability for high current lines (spindle motor and VCM).

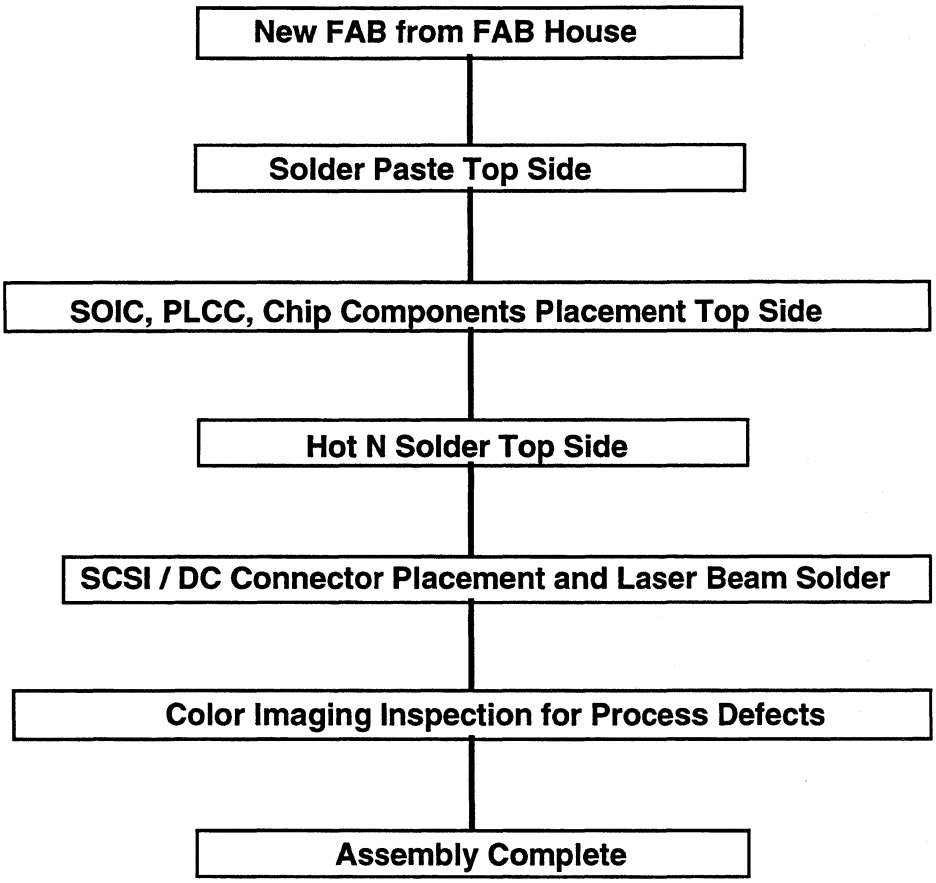
6.7.6 Provide power plane and trace keep out areas where drive mounting screw damage can occur.

6.7.2 Component Selection and Assembly Process

All land sizes were chosen for best placement registration to avoid misalignment, no contact, tombstoning resulting from unequal termination wetting and other SMD parts related solder problems. The fiducial marks at PCB corners help the high resolution vision feedback IC placement machine, especially necessary for fine-pitched QFP placements(0.5 mm pin spacing).

PCB components selection was limited, besides performance, price and availability considerations, by package to fit the form factor, automatic placement, solder and other assembly equipment restrictions, ease of testing requirements, etc. The height requirement for the top side is 4.6 mm max, and for the bottom side 0.4 mm max. In order to meet these requirements, all components are mounted only on the top side while traces run on both sides. The current MKE PCB assembly process is illustrated in the next page.

6.7.3 PCB Assembly Process



6.7.4 Connector

In the current version of the Europa design, the following connectors are used:

AT/DC 50 pin 2mm CONN.	DuPont SMT #92730-001	QNTM # 22-103368-01
R/W FLEX 20 pin CONN.	Molex 52207-2090	N/A
MOTOR 4 pin CONN.	JAE IL-402-16S-S1L-SA	QNTM # 22-102146-01
ID JUMPER (AT ONLY)	Augut CN-EX035A8A02 2 mm RA. SMT 2 pin	QNTM # 22-102137-01
ID JUMPER (AT ONLY)	Augut CN-EX035A8A03 2 mm RA. SMT 3 pin	QNTM # 22-102138-01

6.7.5 AT PCB Block Diagram

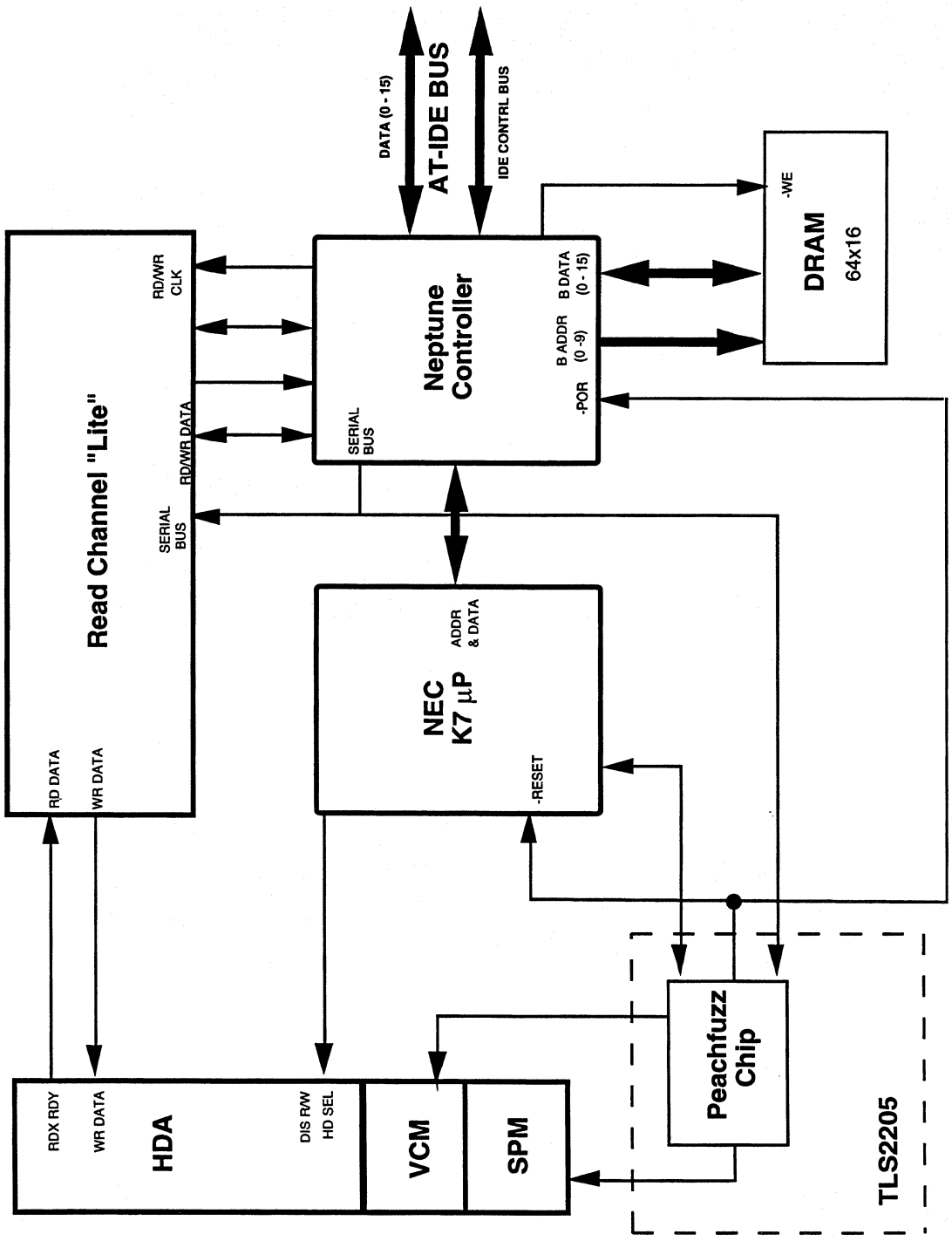


Figure 6-5 AT PCB Block Diagram

6.8 Power Budget

The following estimates for Europa 1 Disk, 2 Disk and 4 Disk AT configurations show power dissipation in each major component of the drive electronics (including spindle motor and VCM), for each of the standard operating modes of the drive.

6.8.1 Power Budget

5V Power in mW								
Section	Sleep	Standby	Idle (@ ID)	Trk Follow (Active) (@ MD)	Random Seek	Write (@ MD)	Read (@ MD)	Peak Spin-up
5V D								
K7	0	0	25	125	385	385	385	385
DRAM	5	25	25	75	75	200	200	75
Serial Port								
Leo	100	100	170	200	210	460	460	210
Lite	0	0	0	200	200	600	600	0
Pre-Amp & Heads	0	0	0	50	50	250	325	0
5V D total mW	**105**	**125**	**220**	**650**	**920**	**1895**	**1970**	**670**
5V M								
Ref. Voltages	15	15	15	15	15	15	15	15
Miscellaneous								
Peachfuzz	15	15	50	50	50	50	50	50
Spindle								
1-Disk	0	0	275	275	275	275	275	4000
2-Disk	0	0	425	425	425	425	425	5000
4-Disk	0	0	500	500	500	500	500	5000
Actuator								
1-Disk	0	0	0	150	1000	150	150	0
2-Disk	0	0	0	150	1000	150	150	0
4-Disk	0	0	0	200	1000	200	200	0
5V M tot al mW (4-Disk)	**30**	**30**	**565**	**765**	**1565**	**765**	**765**	**5065**
Total in Watts								
1-Disk	**0.135**	**0.155**	**0.56**	**1.14**	**2.26**	**2.385**	**2.46**	**4.735**
2-Disk	**0.135**	**0.155**	**0.71**	**1.29**	**2.41**	**2.535**	**2.61**	**5.735**
4-Disk	**0.135**	**0.155**	**0.785**	**1.415**	**2.485**	**2.66**	**2.735**	**5.735**

Table 6-5 Power Budget

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Section 7 Firmware Organization

7.1 Firmware Feature

The following features are to be supported for Europa:

AT:

- Support NEPTUNE Auto Features
  (Auto Read/Auto Write/Auto Transfer)
  - Multiple Auto Read/Write transfers
  - CHS, LBA and DMA transfers
- Auto feature interfacing with Cache
- Local Bus IDE/Fast DMA/Turbo IDE and DMA (20MB/s)

7.2 Caching

Europa incorporates DisCache, an 86K cache, to enhance drive performance. This integrated feature is user-programmable, using the SET CONFIGURATION command, and can significantly improve system throughput.

7.2.1 Read Cache Description

DisCache anticipates host-system requests for data and stores that data for faster access. When the host requests a particular segment of data, the caching feature uses a prefetch strategy to "look-ahead" and automatically store the subsequent data from the disk into high-speed RAM (Random Access Memory). If the host requests this subsequent data, the RAM is accessed rather than the disk.

Since typically 50 percent or more of all disk requests are sequential, there is a high probability that subsequent data requested will be in the cache. This cached data can be retrieved in microseconds rather than milliseconds. As a result, DisCache can provide substantial time savings during half or more of all disk requests. In these instances, DisCache may save most of the disk transaction time by eliminating the seek and rotational latency delays that dominate the typical disk transaction. For example, in a 1K-byte data transfer, these delays comprise 90 percent of the elapsed time.

DisCache works by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a non-caching controller, Quantum's disk controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a full cache segment is read or a new command is received. The cache memory is a DRAM buffer allocated to hold the data which can be directly accessed by the host via any READ and WRITE commands. The memory functions as a group of segments (ring buffers) with rollover points at the end of each segment (buffer). The unit of data stored is the logical block (i.e., a multiple of the 512 byte sector). Therefore, all accesses to the cache memory must be in multiples of the sector size. In those cases where the cache memory must be

used for scratch memory, as in the case of the commands shown below, the cache will be emptied. The commands that will force emptying of the cache are:

AT

- SOFT RESET
- IDENTIFY DRIVE
- READ LONG
- WRITE LONG
- FORMAT TRACK
- SLEEP
- READ DEFECT

7.2.2 Write Cache

When a write command is executed with write caching enabled, the drive stores the data to be written in a DRAM cache buffer and immediately sends a COMMAND COMPLETE message to the host before the data is actually written on the disk. The host is then free to move on to the other tasks, such as preparing data for the next data transfer, without having to wait for the drive to seek to the appropriate track or rotate to the specified sector.

While the host is preparing data for the next transfer, the drive immediately writes the cached data to the disk, usually completing the operation in less than TBD ms after issuing COMMAND COMPLETE. With WriteCache, a single-block random write, for example, requires only about TBD ms of host time. Without WriteCache, the same operation would occupy the host for about TBD ms.

WriteCache allows data to be transferred in a continuous flow to the drive rather than as individual blocks of data separated by disk access delays. This is achieved by taking advantage of the ability to write blocks of data sequentially on a disk that is formatted with a 1: 1 interleave. This means that as the last byte of data is transferred out of the write cache, and the head passes over the next sector of the disk, the first byte of the next block of data is ready to be transferred; thus there is no interruption or delay in the data transfer process.

The WriteCache algorithm allows new data to be transferred into the cache from the host while simultaneously writing previous data from the cache into the disk.

7.2.3 StackWrite

WriteCache allows sequential write data to be cached. StackWrite allows the accumulation of non-sequential write data to be stored in the cache buffer. Up to TBD non-sequential segments can be accumulated.

All cached data will be written onto the disk prior to responding to any non-write command.

7.2.4 Performance Benefits

In a drive without DisCache, during sequential reads, there would be a delay due to rotational latency even if the disk actuator were already positioned at the desired cylinder. DisCache eliminates this rotational latency time -- 7 milliseconds on average -- when requested data resides in the cache.

Moreover, the drive often must service requests from multiple processes in a multitasking or multiuser environment. In these instances, while each process may request data sequentially, the disk drive must share time among all these processes. In most disk drives, the heads must move from one location to another. With DisCache, even if another process interrupts, the drive continues to access the data sequentially from its high-speed memory. In handling multiple processes, DisCache achieves it most impressive performance gains, saving both seek and latency time -- TBD milliseconds on average -- when desired data resides in the cache.

7.2.5 Flexibility, Ease of Use, Speed

DisCache was originally designed to be flexible because cache performance is highly application-dependent. Several parameters are automatically adjusted by the drive. This allows the drive to continuously optimize its performance. The remaining options which are still programmable enable users to adjust caching parameters to optimize performance. These options can be specified and subsequently modified using the SET CONFIGURATION command.

Parameter	DisCache Function	Input Range	Default Value
Read Cache	Enable Read Cache 0 = disable, 1 = enable	0, 1	1 (enabled)
Maximum Number of Read Segments	Sets the maximum number of read cache segments to maintain	1 - 8	2
Maximum Prefetch	Maximum number of sectors to prefetch		Dynamic
Minimum Prefetch	Minimum number of sectors to prefetch		Dynamic
Write Cache	Enable Write Cache 0 = disable, 1 = enable	0, 1	1 (enabled)
Maximum Number of WriteStack Segments	Sets the maximum number of non-sequential WriteStack segments to stack (1 = WriteStack disabled)	1 - 12	12

Table 7-1 DisCache parameters.

Through the use of these programmable parameters, the caching feature can be tailored to optimize individual system performance. The programmable parameters shown in Table 18-1 can be found on SET CONFIGURATION. When the Cache Enable/Disable bit (Byte 32, bit 0), is set to zero, caching is disabled. Disabling the cache reduces command overhead. When disabling the cache, you essentially disable the prefetching and house-keeping required to manage the cache. The default value of this bit is one (Cache enabled).

The Read cache is divided into segments. Each segment contains one cache entry. A cache entry consists of the requested READ data plus its corresponding prefetch data.

7.3 Defect Management

Three different defect lists are stored on system cylinder -2:

1. Primary defect list (P list)—this list contains the defects found in SelfScan at the factory. Only the factory test software has the capability to define the P list. The P list contains the information on defects only. No information regarding each sector's replacement is included.

2. Working list (W list)—the W list is a union of the P list and newly discovered defects, plus it contains all information necessary to locate the replacement for all defects. The "newly discovered" portion of the list contains the defects found in the field during operation of the drive. All user's reassigned defects (i.e., with autoreallocation, format track, reassign physical) are recorded in this list.

3. Temporary list—during an update of the W list (a block reallocation for example) the original W list is stored to this area before any modifications are made to it. This allows data recovery of the old list if any error happens during the generation of the new list.

The W list is used by defect management whenever a logical-to-physical address conversion is called for. This list is not accessible with standard AT commands, but may be read using customer special commands.

7.3.1 Defect List Storage

Up-to-date versions of the P and W lists are saved on the disk, and only the W list needs to be resident in DRAM during drive operation. Each defect can occupy up to 2048 bytes of storage, therefore, a total of 4 sectors per list are reserved to hold the defects list on the system track. See Chapter 5, System Cylinder Layout, for data recorded on the drive, and the location of the lists. Since the W list is limited to 2048 bytes in size, and each entry for a defect consumes 6 bytes, a maximum of 341 defects may be recorded on the drive.

7.3.2 Defect List Data Structure

The defect lists, maintained and accessed by the defect management system, consist of 6-byte defect entries. The P list contains only defect entries while the W list contains both defect and replacement cylinder information. The defect list structure is illustrated below.

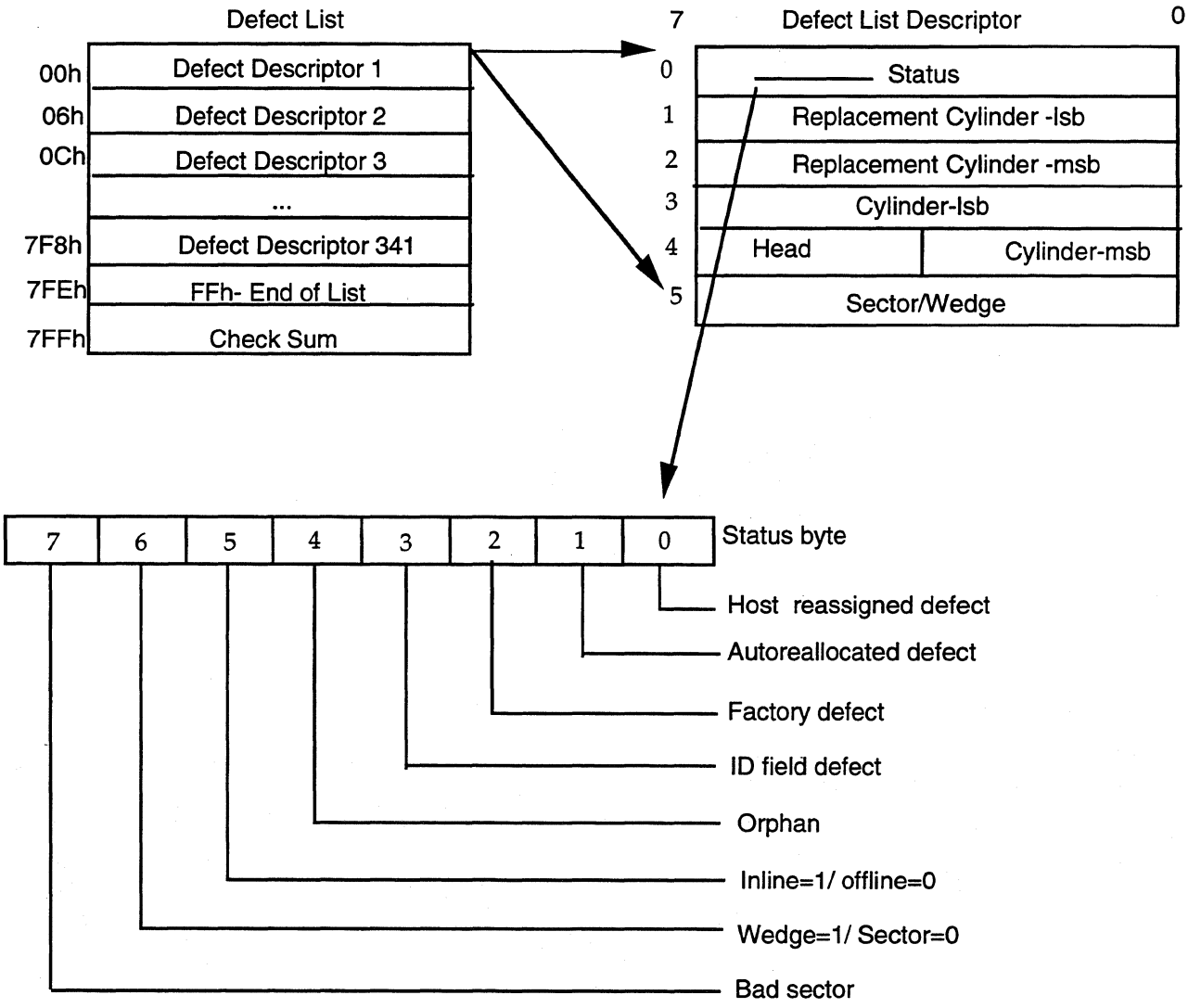

Figure 7-1 Defect List Data Structure

Bits 0-2 are used to distinguish between P list entries (factory defect) and "newly discovered" list entries (auto reallocated and user reassigned).

Bits 3-7 are used by defect management to find the correct physical sector for a given LBA.

The end of list marker is placed after the last entry in the list.

The checksum is placed at the end of the list, and the empty area in the list is filled with zeros. When this byte is added to the rest of the bytes in the list, the lsb of the checksum will equal ASCII "L" .

7.3.3 Defective Sector Replacement Strategy

Europa reserves one alternate sector per cylinder for defect sparing. and it utilizes two methods for sector replacement. They are inline and offline sparing.

7.3.3.1 Inline Sparing

Inline sparing is where a defective sector is replaced by the next immediate sector—all sectors thereafter within the same cylinder are shifted , logically, by one. (see next figure). The access penalty is very small for inline replacement, which is one sector time. Whenever possible, defects are spared with inline replacement at the factory. In the unlikely event where there are multiple defects on the same cylinder, additional spare sectors must be allocated from adjacent cylinders. This is defined as offline replacement. Accessing the defective sector requires a short seek and latency. MI grown defects are offline spared during drive operation. However, the drive will attempt to inline spare all known defects when a Format Unit command is issued.

7.3.3.2 Offline Sparing

Offline sparing is where a defective sector is replaced by a spare sector located at the end of a cylinder. Defect management will try to replace the defective sector with a spare on the same cylinder. If this is not possible, as in the case of the spare is already in use, defect management will find a spare sector located on an adjacent cylinder. The disadvantage to this is the performance degradation caused by the seek. The next figure contains examples of different types of sparing.

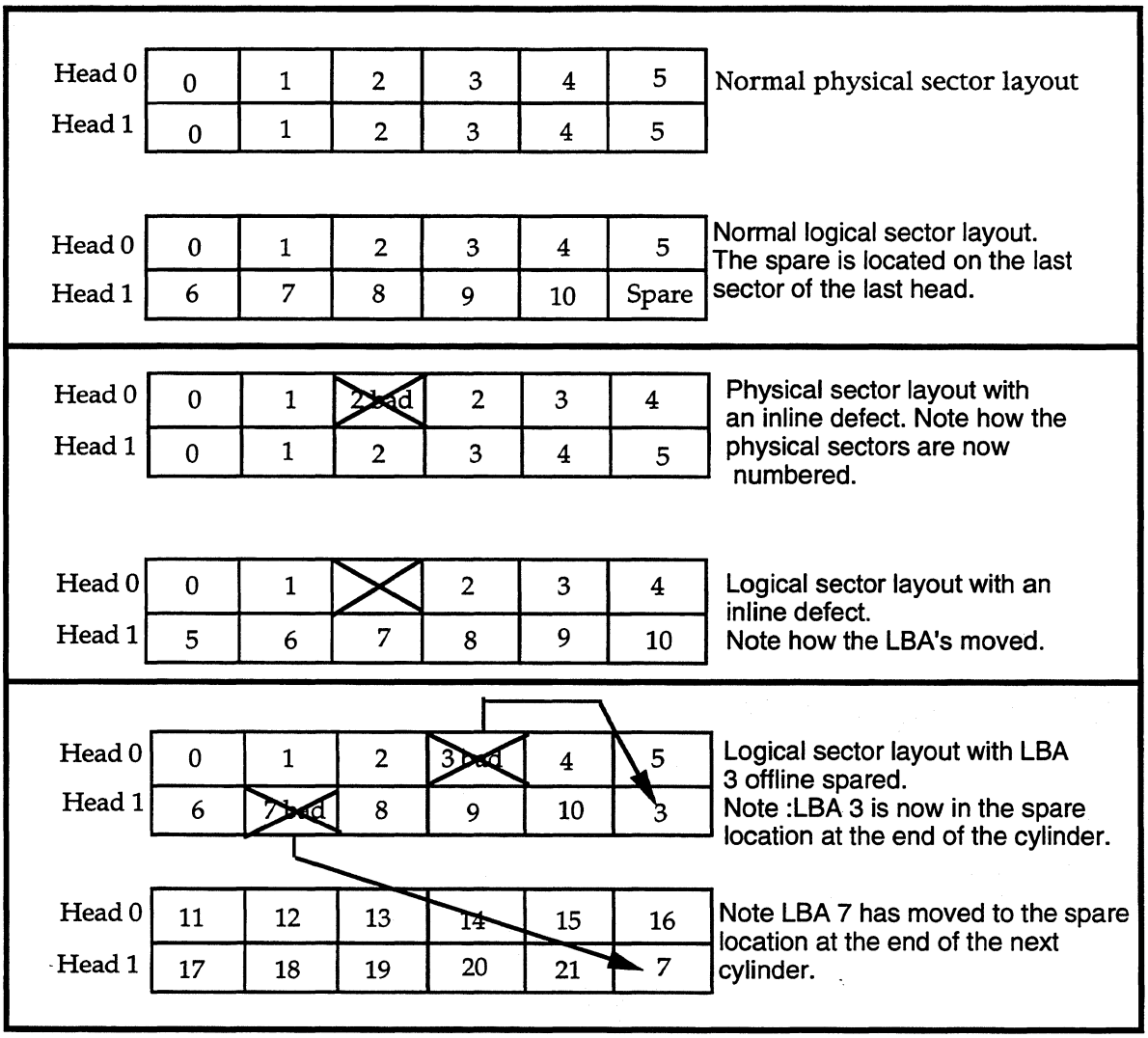

Figure 7-2 Examples of Different Types of Sparing

7.3.4 Auto Reallocation

Reallocation during a read operation is processed on a sector-by-sector basis. When a sector determined to be defective by the read or write firmware, it is then subjected to a write/verify test before it will be reallocated. Using the data read from the defective sector, the drive writes to and reads the sector (for up to) ten times. If any of the ten tests fail, the defect is considered repeatable and the sector is reallocated. If all ten tests pass. then the failure is considered nonrepeatable and the sector is left as is.

7.3.5 Orphans

An orphan occurs when a replacement sector goes bad. The replacement is assigned a new sector and the original replacement sector is tagged as an orphan in the defect list. It is no longer used. Defect management skips over defect entries that are tagged as orphans.

7.3.6 Track Format - Bad Wedge ID

If a defect occurs in the ID field, there is a potential for losing 3 sectors using the ID-per-wedge format. The sector before the defect, the sector with the defect. and the sector after the defect may have to be tagged as bad (due to split sectors). This can be avoided by moving the ID field to a new location within that wedge (See example B and C, below).

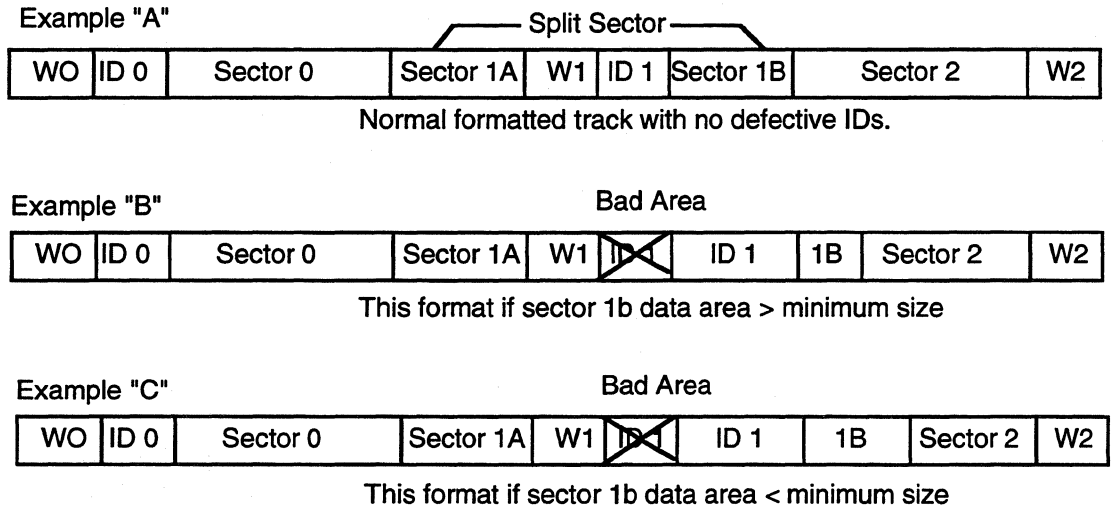

Figure 7-3 Bad Wedge ID

The sectors (areas) that are labeled as bad are entered into the Primary defect list (P list) an formatted as In-Line defects.

7.4 Error Correcting Code

7.4.1 ECC Features

- 8 bits per symbol.
- 3 interleaves.
- 6 redundancy bytes per interleave.
- 2 cross-check bytes.
- 18 ECC bytes and 2 cross-check bytes: total of 20 redundancy bytes.
- ECC hardware includes Reed-Solomon encoder/decoder circuit that is used to generate redundancies during write mode and syndromes during read mode. The hardware also checks the values of the syndromes to detect error. All corrections will be done in firmware.
- Single-Error Correction:
  — Correct up to 24 bits (i.e. 1 byte per interleave).
  — Guarantee to correct 17 bits.
- Double-Error Correction:
  — Correct up to 48 bits (i.e. 2 bytes per interleave).
  — Guarantee to correct 41 bits.
- Triple-Error Correction:
  — Correct up to 72 bits (i.e. 3 bytes per interleave).
  — Guarantee to correct 65 bits.
- Random Multiple-burst error case: correct up to 9 bytes.
- Scan-path is available for testability.
- ECC syndromes and cross-checks can be observed by selecting the ECC registers from (E0)h to (F3)h.

7.4.2 ECC Equations

7.4.2.1 Galois Field

The Galois field for the ECC and cross-check polynomials is generated using the extension field theory and is described as follows:

- Sub Field GF(2^4):

Let elements of the sub field be represented by powers of beta. The sub field is defined by:

$P_{sub}(X) = X^4 + X + 1$

with $beta^1$ = (02)h as the first element of GF(2^4) over GF(2).

- Extension Field GF(2^8):

Let elements of the extension field be represented by powers of alpha. The extension field is defined by the following polynomial:

$P(Z) = Z^2 + Z + f_0$

where

f_0 = (08)h as a constant and

$alpha^1$ = (12)h as the first element of GF(2^8) over GF(2).

7.4.2.2 ECC Polynomial

The ECC polynomial is defined as follows:

$$ECC(X) = X^6 + alpha^{169}*X^5 + alpha^{179}*X^4 + alpha^{25}*X^3 + alpha^{184}*X^2 + alpha^{179}*X + alpha^{15}$$

$$= (X + 1)*(X + alpha^1)*(X + alpha^2)*(X + alpha^3)*(X + alpha^4)*(X + alpha^5)$$

7.4.2.3 Cross - Check Polynomial

The Cross - Check Polynomial is defined as follows:

$$XC(X) = X^2 + alpha^{143}*X + 1$$

$$= (X + alpha^{127})*(X + alpha^{128})$$

7.5 Description of CRC

7.5.1 CRC for ID Field

The ID data is protected by 3-byte Reed-Solomon CRC. The values of CRC bytes can be observed by selecting the following registers: (F4)h for CRC0, (F5)h for CRC1, and (F6)h for CRC2.

7.5.2 CRC Equations

7.5.2.1 Galois Field

The Galois field for the CRC polynomial is the same as the ECC and the cross-check polynomials.

7.5.2.2 CRC Polynomial

The CRC polynomial is defined as follows:

$$CRC(X) = X^3 + alpha^{203}*X^2 + alpha^{203}*X + 1$$

$$= (X + alpha^{-1})*(X + alpha^0)*(X + alpha^1)$$

7.6 Probabilities

7.6.1 Probability Model

Assumption 1: every symbol has equal error probability and error pattern is occurred completely random.

Assumption 2: each error burst is associated with a single byte.

Probability numbers are defined as follows:

- P_s : raw error rate (events/bit). This number is obtained before ECC system.
- P_h : probability of hard error (events/bit) obtained after on-the-fly ECC.
- P_{ue} : probability of uncorrectable errors (events/bit) when the number of symbol errors exceeds the correction capability of the code.
- P_{mc}: probability of miscorrection. This is a conditional probability that depends on the number of errors occurring.
- P_{xc} : misdetection probability of the cross-checks.
- P_e : probability of decoding error when the ECC incorrectly decodes and sends erroneous data to customer.

7.6.1.1 Probability of Uncorrectable Errors:

Probability of uncorrectable errors (events/bit) when the number of symbol errors exceed the correction capability of the code.

$$P_u = \frac{1}{n*m}\sum_{i>t}^{n}\binom{n}{i}(P_s*m)^i*(1-P_s*m)^{n-i} \qquad (1)$$

where

n : number of symbols per interleave including redundancy symbols.
m: symbol width in bits.
t : correction capability in symbols.
P_s*m : raw symbol error rate (events/symbol).

7.6.1.2 Probability of Miscorrection

The Reed-Solomon ECC is characterized as a maximum distance separable (MDS) code in which d = n - k + 1. We are using an incomplete decoder for a t-error-correcting code that t is equal to (n - k)/2. This means that the ECC only corrects all errors with t symbols or less and does not attempt to correct more than t error symbols. When an error burst of a received word is less than or equal to t symbols, the code corrects without any miscorrection errors. This means that P_{mc} is equal to zero. If there is error greater than t symbols, the code either sends an uncorrectable message or decodes the error patterns and error locations incorrectly. The value of P_{mc} then can be estimated as follows:

$$P_{mc} = q^{-r} * V(t) \qquad (2)$$

where

$q = 2^m = 2^8 = 256$.

r = n - k --> (code's redundancy).

$$V(t) = \sum_{s=0}^{t} \binom{n}{s} * (q-1)^s$$

(volume of a Hamming sphere of radius t)

Therefore,

- For $e \leq t$, $P_{mc} = 0$ (3a)
- For $e > t$, $$P_{mc} = \frac{\sum_{s=0}^{t} \binom{n}{s} * (q-1)^s}{q^r}$$ (3b)

(where e: number of symbol errors).

7.6.1.3 Probability of Misdetection of Cross-Checks

The probability of misdetection of the cross-checks can be estimated as follows:

$$P_{xc} = \frac{1}{q^{rxc}} \quad (4)$$

where

rxc : number of cross-check symbols.

7.6.1.4 Probability of Decoding Error

This probability can be translated as the probability of transferring erroneous data to customer. P_e can be obtained by taking the product of P_u, P_{mc}, and P_{xc} :

$$P_e = P_u * P_{mc} * P_{xc} \quad (5)$$

7.6.2 Error Probabilities

7.6.2.1 ON-THE-FLY CORRECTION (SINGLE- OR DOUBLE-ERROR CORRECTION)

Assumption: $P_s = 10^{-7}$ (raw soft error rate).

$$P_u = \frac{1}{176*8} \sum_{i=3}^{176} \binom{176}{i} (10^{-7}*8)^i * (1-10^{-7}*8)^{176-i}$$

$= 3.3 * 10^{-16}$

$$P_{mc} = \frac{\sum_{s=0}^{2} \binom{176}{s} * (256-1)^s}{256^6}$$

$$= 3.5 * 10^{-6}$$

$$P_{xc} = \frac{1}{256^2} = 1.5 * 10^{-5}$$

$$P_e = P_u * P_{mc} * P_{xc} = 1.7 * 10^{-26}$$

7.6.2.2 Off-line Correction (Triple-Error Correction)

Assumption: $P_s = P_h = 10^{-10}$ ---> hard error rate
(i.e. hard errors beyond the correction capability of on-the-fly ECC)

$$P_u = \frac{1}{176*8} \sum_{i=4}^{176} \binom{176}{i} (10^{-10} * 8)^i * (1 - 10^{-10} * 8)^{176-i}$$

$$= 1.12 * 10^{-32}$$

$$P_{mc} = \frac{\sum_{s=0}^{3} \binom{176}{s} * (256-1)^s}{256^6}$$

$$= 5.0 * 10^{-2}$$

$$P_{xc} = \frac{1}{256^2} = 1.5 * 10^{-5}$$

$$P_e = P_u * P_{mc} * P_{xc} = 8.4 * 10^{-39}$$

7.6.2.3 Summary

In the off-line correction case, the probability of miscorrection (P_{mc}) is 5.0E-2 that is quite high and unacceptable. In order to improve this probability number we use two cross-checks to detect miscorrection. These two cross-checks make the effective miscorrection probability equal to 7.0E-7 (i.e. $P_{mc} * P_{xc}$ = 5E-2 * 1.5E-5 = 7.0E-7) which is better than P_{mc} by itself.

In addition to the two cross-checks, we also employ an off-line correction algorithm in firmware that rereads a number of times with on-the-fly ECC, and performs triple-error correction only when hard error is detected. These criteria improve P_s from 10^{-7} to 10^{-10} (i.e. P_h) which effectively improve the probability of transferring erroneous data to customer as depicted above. Note that we assume the worst case here with P_h = 10^{-10}, because the typical number should be about 10^{-14}.

7.7 Microprocessor Memory Map, Diskware and F/W Organization

The Europa architecture has been designed to support Diskware. Part of the Buffer memory is used to load firmware from disk and the processor is able to execute the firmware directly from the buffer memory.

The firmware is partitioned between the CPU ROM and the Diskware. The CPU ROM code contains all of the routines necessary to power up the drive and read the Diskware into the Buffer. It also contains routines that allow the Diskware to be written to the disk via the host interface. All time critical code is located in the CPU ROM because the processor is able to execute CPU ROM code much faster than Diskware code. The Diskware code contains firmware that is not required for spinning up the drive. The Diskware code also contains provisions to allow for possible engineering firmware changes in the CPU ROM code to be corrected by mapping erroneous subroutines from CPU ROM into the Diskware.

The Diskware code space is partitioned into two parts, a resident part and an overlay part. The resident Diskware is loaded during the drive power up initialization and remains in memory while the drive is powered on. The overlay Diskware is loaded on an as needed basis, at present there are two overlay defined, one for Selfscan and one for normal operation.

The Diskware is stored on reserved system cylinders in memory image format. A new configuration page 15 specifies where the overlays are stored on the system cylinders and where the overlays are loaded into the processor memory. Generally system cylinder information is stored in multiple places for redundancy, the overlay configuration page only specifies where the first copy of the Diskware is stored. Redundant copies of the Diskware are stored according to the firmware redundancy algorithm for system cylinder information. The Europa firmware stores redundant system cylinder information on all physical heads in system cylinder areas.

Configuration Page 15 - Overlay Page

Byte	
0	=01 (normal diskware)
1 - 3	Microprocessor load address
4	Size of overlay in sectors
5 - 6	Cylinder of primary copy
7 - 8	Cylinder of alternate copy
9 - 10	Starting sector of overlay
11	=02 (selfsacn main)
12 - 20	See bytes 1- 10
21	=03 (selfscan overlay 1)
22 - 30	See bytes 1- 10
31	=04 (selfscan overlay 2)
32 - 40	See bytes 1- 10
41	=05 (selfsacn overlay 3)
42 - 50	See bytes 1- 10
51	=06 (selfsacn overlay 4)
52 - 60	See bytes 1- 10
61	= FFH (end marker)

The NEC K7 microprocessor has a 16 MB address space. On Europa, it is organized as follows:

Address	Size	Description
FFFFFF		Top of internal memory
FFFE00	512	Start of special function registers
FFFD80	128	Start of register banks
FFFA70	784	Start of servo and other critical variables
FFFA00	112	Start of stack
FF817F		Top of ASIC
FF8000	384	Start of ASIC
27FFF		Top of external memory
1A400	55K	Start fo read segments
12400	32K	Start of write segment
11D00	3.5K	Start of variables
11500	2K	Start of defect table
11400	.5K	Start of cache table
10A00	2.5K	Start of configuration pages
10800	1K	Start of stacked write
10600	.5K	Start of fixed buffer
10200	1K	Start of temporary buffer
10000	.5K	Start of sector buffer
08000	32K	Start of diskware
00000	32K	Start of ROM

Table 7-2 Europa Memory Map

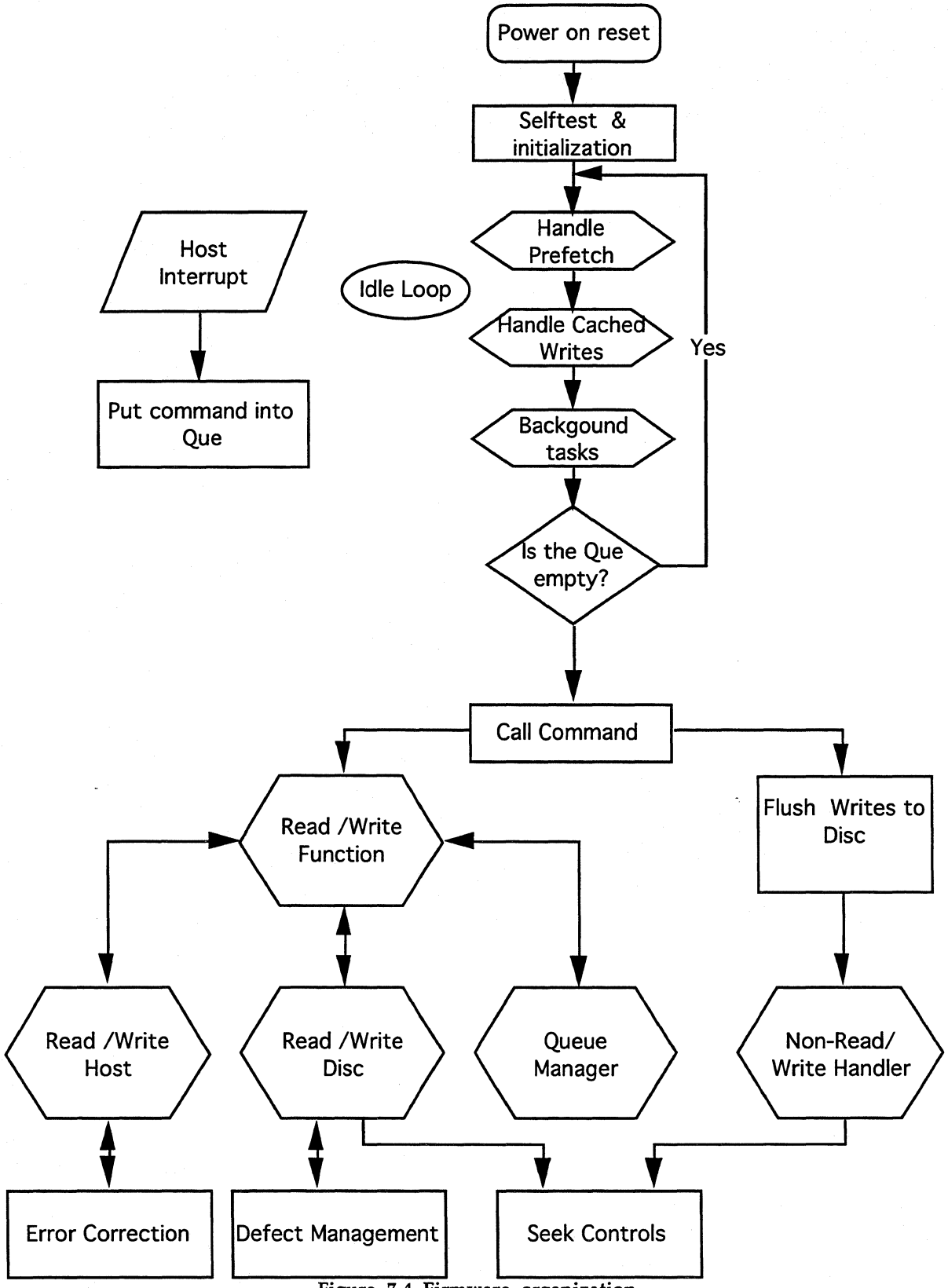

Figure 7-4 Firmware organization

Section 8 Servo Design

8.1 General Description

The Europa servo is an embedded sector servo system using MR technology to achieve 5300 TPI. State space control technique is used for its ability to handle sensor noise and the flexibility to allow more involved algorithm, such as adaptation, should the situation require.

8.2 MR Head Considerations

The use of MR head, with advantages such as high level signal which is independent of the head/media speed, adds considerable complexity to the servo system, some of which are briefly described in this section

8.2.1 Microjog

The MR head uses separate elements for the read and write operations. As a result, the servo must "microjog" when it changes the write operation to read , or vice versa. This microjog distance is dependent on:

- Track number
- Tangential read/write element separation
- Radial offset between the magnetic centers of the read and write element. This offset is used as a head design parameter to balance the microjog distance (opposite direction) at the ID and OD, which minimizes the amount of track servoing.

8.2.2 Ontrack/Offtrack Servo

Ontrack servo is defined as the servo operation to maintain track following when servo bursts A = C . Offtrack servo is the operation to maintain track following with an offset between -50% to +50% of a track. The ontrack servo uses the best linear region of the servo bursts, which results in better track following performance than offtrack servo. Therefore, the **ontrack servoing is used in the write data operations.** On the other hand, the offtrack servoing is used mainly in read operations. For a rad operation on any track, the servo seeks to that track with an offset that is equal to the microjog distance associated with that track (and head). The servo settles directly to the offtrack position.

Besides read operations, offtrack servoing is also used for formatting, read/write offset measuring, and other testing and optimization during the development and manufacturing processes. The following factors can affect offtrack servoing:

1. The linear property of the servo track profile, particularly at the ±25% offtrack region where the decoding algorithm must switch between A and C bursts to calculate the position error signal (PES).

2. The gray code near ±50% offtrack region may not be accurate (error = ± 1) and it also may result in a soft error. Currently, the servo code ignores these errors while offtrack is more than 25%.

The offtrack servo necessitates the addition of the 4th burst.

8.2.3 Read/Write element offset measurement

In order to calculate the amount of microjog needed at each track, the read/write element offset must be measured at the Inner Diameter (ID), Outer Diameter (OD), and Mid Band (MB) tracks. This measurement requires offtrack servoing with an offtrack range more than the normal microjog distance.

8.2.4 Bias current

MR head requires bias current to "rotate" the magnetic domain to the appropriate operating point. This bias current has strong effects on the slope of the PES signal, which is calibrated by the RECAL routine at power up time. It is essential to keep the bias current constant to avoid the need to recalibrate PES slope other than at the power up time.

8.2.5 Read width vs. write width

The MR head allows the designer to select different widths for the read and write elements. In general, a separated and narrower read element requires less stringent TMR; however, the read element cannot be too narrow, as it would decrease signal amplitude and it would create problems in the servo track profile, which would have a steeper slope and a wider saturated region. The read element width of 2/3 of the track width was selected for this reason, and it also allows the possibility of using the servo burst width equal to 2/3 of the track width, if needed, to improve the servo track profile linearity.

8.2.6 ID Field

Accessing the ID field affects the servo function in a number of ways, such as:

1. The requirement to position the head to assure the ID field reading
2. Ability to servo offtrack during formatting of the ID field

8.3 Mode of Operation

Head position is digitally controlled in a servo interrupt service routine (ISR). The microprocessor is interrupted by the TNA one time for every servo wedge. In the ISR, the servo firmware looks at the state of some flags to decide how to handle the position information available. One of three general control algorithm is used for generating current commands:

- Velocity seek
- Settle
- Track Follow

8.3.1 Seek Mode

The primary objective of Seek Mode is to move the read/write head from one concentric track radial position to another concentric track radial position under the physical constraints of the actuator acceleration factor and power consumption. In doing so, it has to accelerate the actuator as quickly as possible and then switch to controlled deceleration as soon as possible to stop just in time when it arrives at the target track position

A long seek (seek length > 64 tracks) consists of accelerating, coasting, decelerating, linear velocity, and then settling. A medium seek (seek length between 33 and 64 tracks) starts immediately with linear velocity. A short seek (seek length < 32 tracksZ) also starts with linear velocity using low bandwidth coefficients.

In order to have the correct acceleration to deceleration switching and controlled deceleration operation for various seek lengths, a phase plane velocity vs. position trajectory guide is employed. Hence, both position and velocity state information of the actuator are vital

Control strategy should avoid excessive overshoot of velocity profile trajectory when switching, and should make actuator adhere to the trajectory profile while decelerating without too much noise in the control by using feed forward. It should also provide consistent final conditions of seek mode for the next servo settle mode initial conditions.

8.3.2 Settle Mode

The Settle Mode is designed with high DC stiffness and high phase margin for good damping and fast settling for seek arrival transients. The servo switches fro m seek mode to settle mode when it is within position error and velocity limits. The settle mode requires two bursts (A, C or B, D) to calculate the position error. When the head is moved more than 1/4 track from the target, the servo switches back to the linear velocity.

8.3.3 Track Follow Mode

When the servo stays within position error and velocity limits for ten consecutive samples, it switches to the track following mode with write enabled. When the servo detects a bump and an error condition in the previous sample (including a bump condition), it disables write and switches to linear velocity to bring the head back to target.

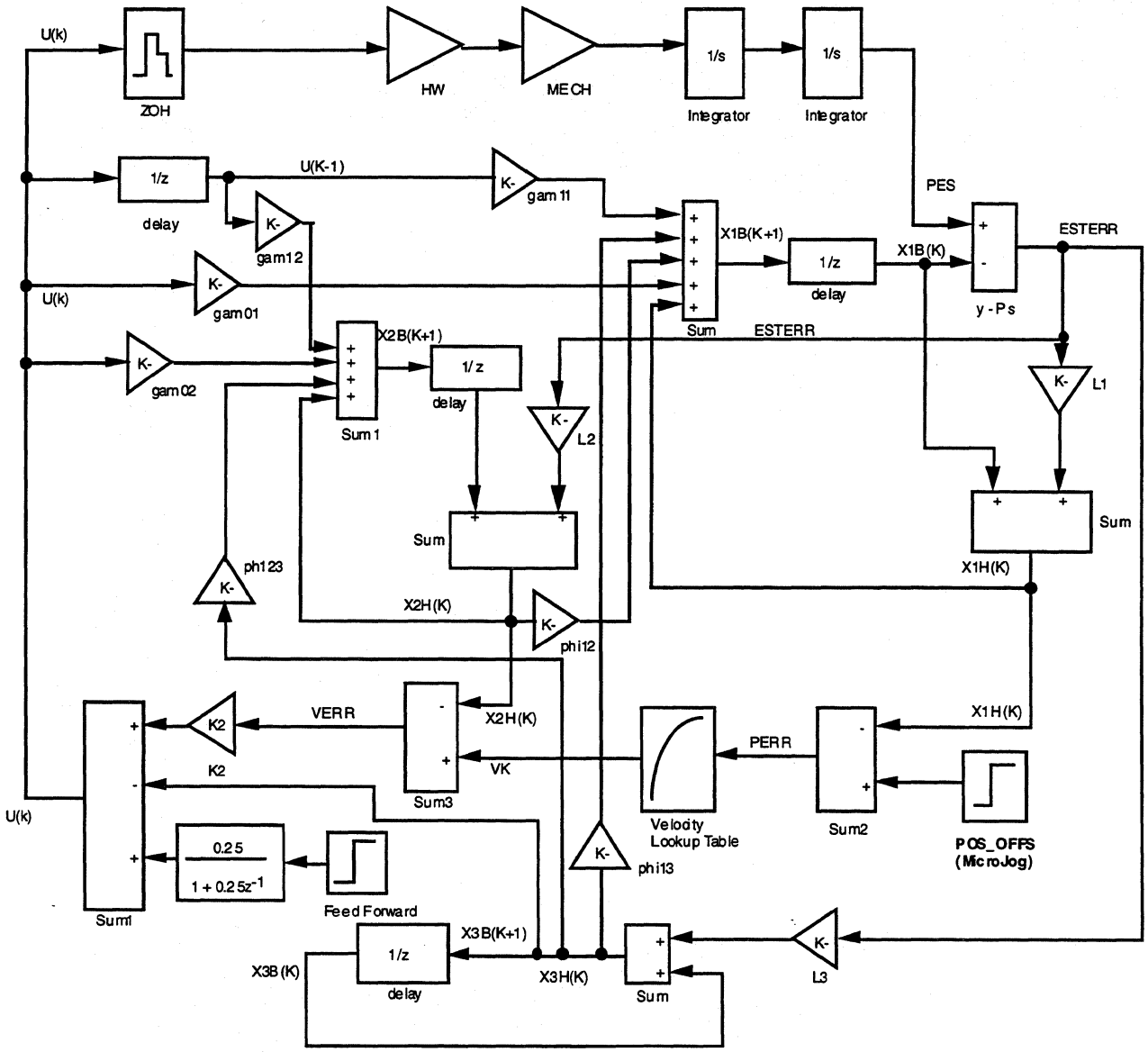

Figure 8-1 Seek Mode

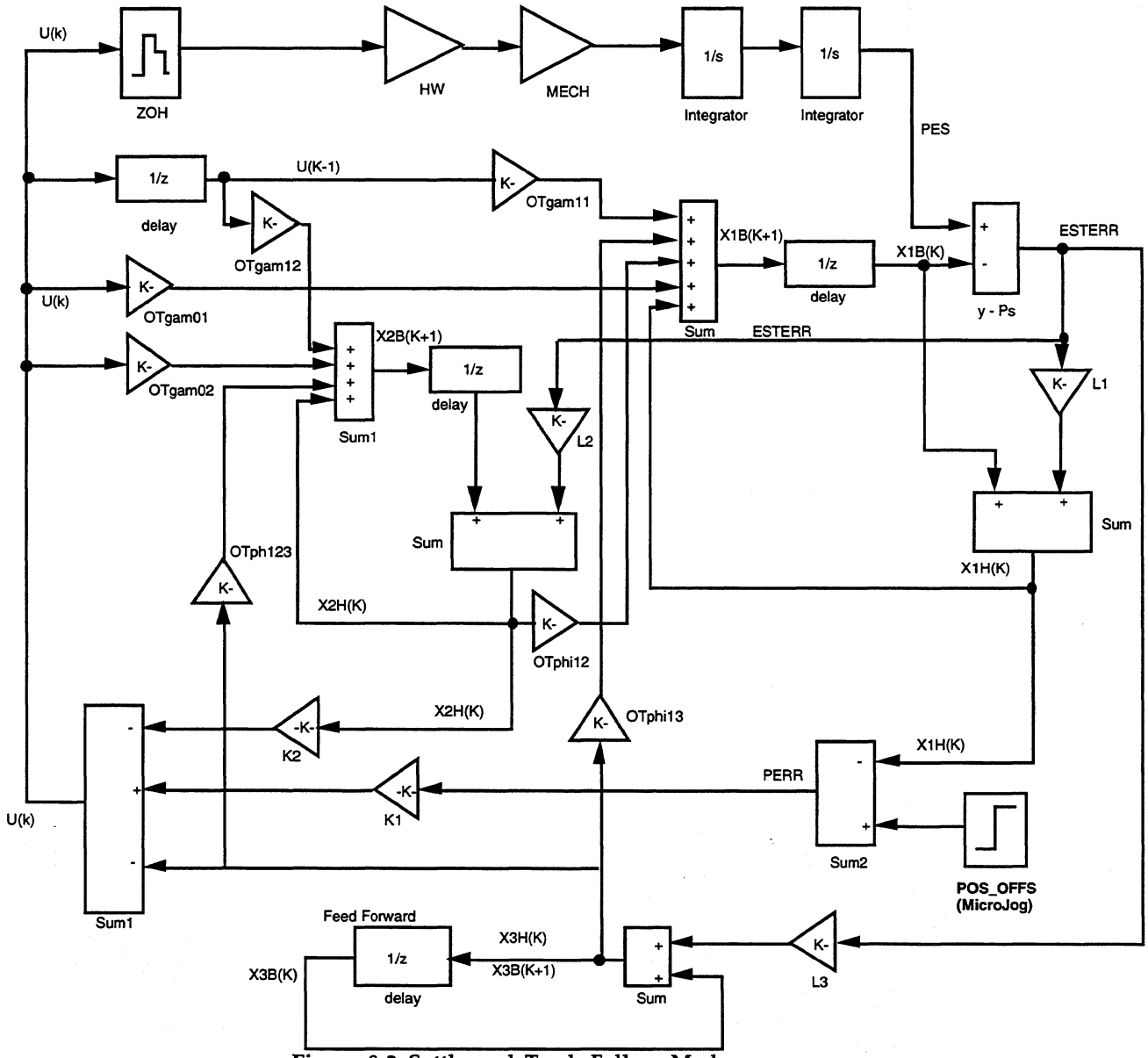

Figure 8-2 Settle and Track Follow Mode

8.4 Servo Error Budget

TMR ITEMS	PROPOSED	
	-3 SIGMA	+3 SIGMA
NRRO (No vibration)	TBD	TBD
NRRO(under vibration)	TBD	TBD
NRRO (under shock)	TBD	TBD
Settling, Read Ready	TBD	TBD
Settling, Write Ready	TBD	TBD
Servo Dither	TBD	TBD
Servowriter DC Error	TBD	TBD
Servowriter AC Error	TBD	TBD
Elastic Thermal Disk Shift	TBD	TBD
Perm. Thermal Disk Shift	TBD	TBD
Actuator Dither (under vibration)	TBD	TBD
Actuator Dither (under shock)	TBD	TBD
Shock (10G 11 ms)	TBD	TBD

Table 8-1 Europa error budget

Notes to Table 8-1:

1. All distributions above were approximated from actual data or simulation studies.

2. -3 sigma to + 3 sigma contain (or hold) 99.74% of total histogram, and histogram not necessarily Gaussian distribution.

8.5 Servo System Parameters

Components or parameter	Europa Spec	
TPI	5300	track/inch (intended)
# of cylinders	2949	cylinder
# of sector/rev	88	sector
Spindle speed	3800.00	RPM
Sample period	179.00	µsec
Alias frequency	2787	Hz
Arm radius to head[1]	1.543	inch
Inertia[2]		
(2 disk)	9.00	gm-cm^2
(4 disk)	17.00	gm-cm^2
Torque constant[3]		
(2 disk)	0.023	nm/amp
(4 disk)	0.048	nm/amp
Acceleration factor		
(2 disk)	25500.00	1/amp-sec^2
(4 disk)	25900.00	1/amp-sec^2
Coil resistance (@ 25°C)[4]		
(2 disk)	14.00	ohm
(4 disk)	14.30	ohm
Max. head velocity	56.00	in/sec
Power amp Lo gain[5]	0.00053	amp/bit
Power amp Mid gain[5]	0.00105	amp/bit
Power amp Hi gain[5]	0.0021	amp/bit
Coil inductance[6]		
(2 disk)	130	µH
(4 disk)	240	µH
Max. voltage[7]	TBD	volt

Table 8-2 Servo related parameters

Notes to Table 8-2:

1. The distance from actuator pivot to read/write head gap is measured by Quality Assurance X-Y table and caliper measurement.

2. Inertia is measured by means of the Torsion pendulum method.

3. Torque factor is measured by applying a constant current to voice coil and measuring the torque on the actuator across the ID-to-OD band. The currents applied are ± 100 ma, ± 200 ma, and ± 300 ma respectively for each measurement.

4. Coil resistance is measured by means of a Digital ohmmeter.

5. Gain of DAC stage included.

6. Coil inductance is measured by means of a Digital impedance meter.

7. Available @ Power amp outputs w/ nominal 5 volt supply.

8.6 Multi Bursts

The offtrack servoing requires the use of a 4th burst, called D-burst, to completely decode the positional error between -50% to +50% offtrack. Basically, the A and C bursts are used to decode between -25% to +25% offtrack and B and D bursts are used for the rest. During the seek mode, either A burst or B burst is used.

8.7 Sampling Rate

Refer to changes for ASIC for SAM to SAM timing to allow lower sample rates, slower spindle speeds.

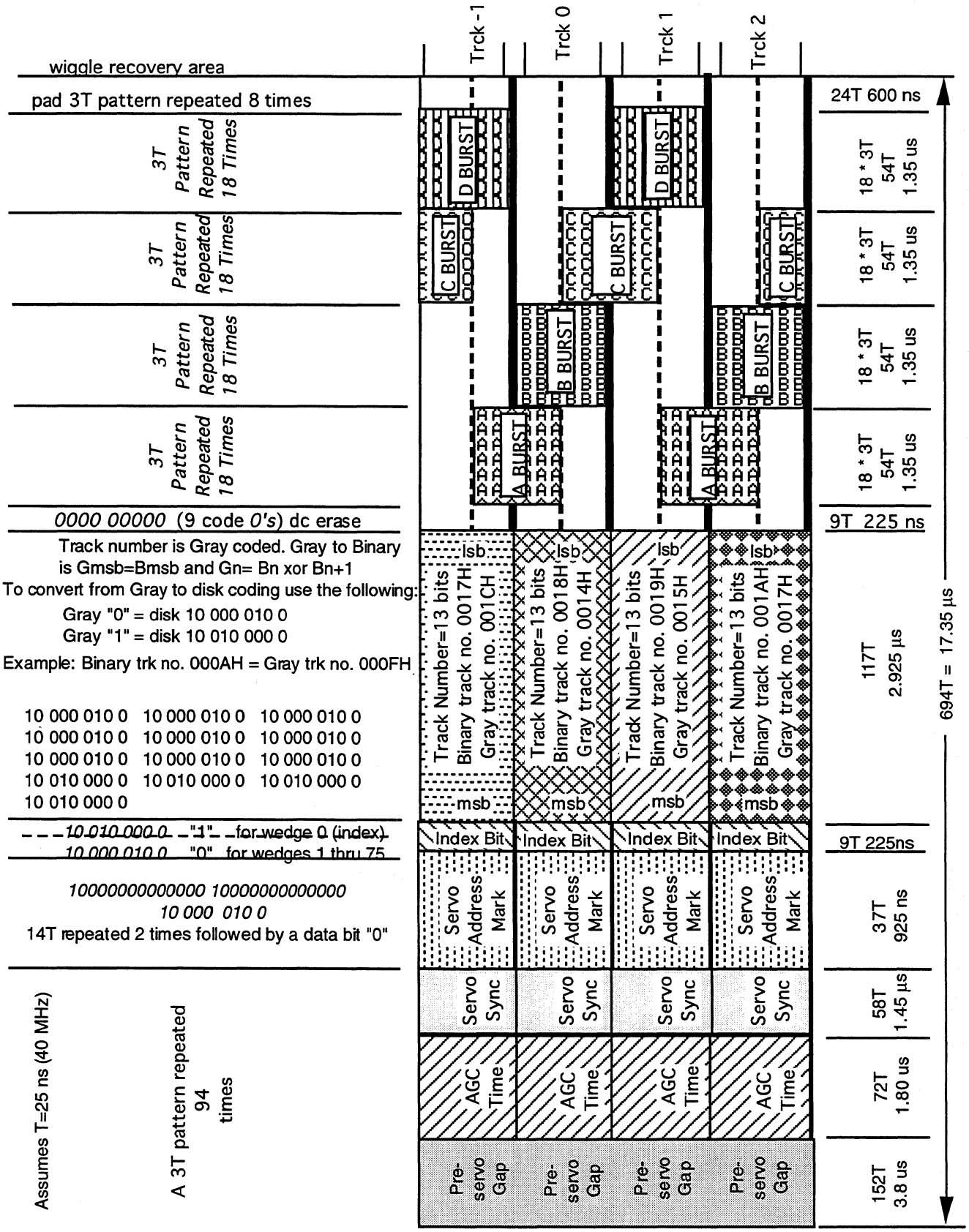

Figure 8-3 Servo Wedge Format

8.8 Servo Electronics

8.8.1 Peak Detect Channel for Servo Bursts

The peak detector channel extracts the amplitude of the A, B, C and D Bursts from the servo wedges. A weighted average Peak and Hold circuit, which resides in the Read/Write ASIC, was implemented. The gate inputs to the peak detector, and the control of which bursts are sampled, are sent from the Servo Controller module of the Disk Controller and Host Interface ASIC. The timing of these gate inputs (i.e., delay to start and duration) is programmable.

The analog average output of the sampled servo bursts are converted to digital format via the eight-bit Analog to Digital Converter (ADC). This ADC is also part of the Servo Controller module in the Disk Controller and Host Interface ASIC. The servo firmware reads the digital burst value to determine the actual head position.

8.8.2 Actuator Driver

The actuator driver includes an 8-bit DAC plus 4 gain ranges, a power amplifier capable of ±0.4A and a precision current sense amplifier that can detect load current with a single resistor in series with the voice-coil motor (VCM). The retract control circuitry is fully integrated and does not require external isolation of the device power supply terminals such as external isolation transistor/diodes. Voice coil driver auxiliary digital control functions include an output-disable and low-power sleep mode following a retract of the VCM to the landing zone. During a fault condition, the actuator is disabled.

The actuator driver is integrated with the spindle driver in one IC.

8.9 Servo Error Recovery

8.9.1 Self-recovered Servo Errors

The background code that monitors the servo simply has to report to the host the recovered error that the servo has found. The recovery of this type of error does not require external interference.

8.9.2 Fatal Servo Errors

When the servo detects five consecutive synchs, SAMs errors, or spindle speed error, it reports a "lost lock" error and starts a full recal.

8.10 Power Management

TBD

Section9 Test Plan

9.1 General Description

This is a preliminary Production Test Plan for the Europa drives. The final test plan will mature from this proposal.

9.2 Servo Writer Station (Pre Production-MP)

The Europa drive uses the push-pin type servo writer; writing the servo with the cover on the HDA. The servo-writer writes wedges on each track of each surface. This station verifies the integrity of the wedges. In verify mode, the head is positioned at the track center of the outermost track, and then moved in one track increments to each successive track center, using the laser as the position reference. Checks are made of the amplitudes of each servo burst against the minimum and maximum amplitude required for the drive AGC and servo to operate. Also, a check of the encoded track number, and of the Sync and Servo Address Mark (SAM) fields are made. The total stroke of the drive is checked.

A Servo Writer is a complex, very accurate test system consisting of three major blocks:

- A precision mechanical clamping system mounted on a granite plate to achieve high mechanical stability and very low sensitivity to vibration.
- The laser positioning system used to accomplish accurate positioning in the process of writing and verifying servo bursts.
- The read/write/verify and control electronics.

9.2.1 Servo Writer Station Tests

The tests performed at the servo writer station are as follows:

- Parametrics

  - Clock Head AGC
    This test verifies the clock head is responding and functional.

  - Track Average Amplitude (TAA), ID
    This test will test each head for an open or short circuit. A high frequency pattern is written at the ID and then read back and compared to a minimum signal value.

    If hf_TAA < min_TAA_limit (**TBD mV**) then FAIL

- Resolution, ID

  The head resolution test measures the relative gain at two different frequencies. A high frequency pattern is written at the ID and read back, then followed by a low frequency pattern which is also read back. The ratio of the track average amplitude signal levels, for the two patterns, is compared to a resolution limit.

  If ((hf_TAA / lf_TAA) * 100) < resolution _limit (**TBD%**) then FAIL

- Positive and Negative Modulation, ID

  This test measures the degree of signal modulation for a high frequency pattern written at the ID.

  If hf_high > (100 + modulation_limit) (**TBD%**) then FAIL
  OR
  If hf_low < (100 - modulation_limit) (**TBD%**) then FAIL

  where:
  hf_high = (track_amplitude_max / TAA) * 100
  hf_low = (track_amplitude_min / TAA) * 100

- Measure Stroke

  This test measures the actuator stroke from the inner crash stop to the outer inner crash stop in laser counts. The measurement is made by slewing the actuator between crash stops.

  If laser count is less than a minimum count, then FAIL
  If laser count is greater than max. count, then FAIL

- Mag Latch

  The Mag Latch test measures the actuator current required to unlock the Mag Latch. It also measures the latch pick position by slewing the head from OD to ID.

- Write Clock Track

  A clock track is written, using a separate clock head, to provide timing and synchronization signals for subsequent writing of servo wedges. The clock head is positioned outside of the outer crash stop so as not to impinge on the reserved data area of the media.

  If the operation is unsuccessful, then FAIL

- Write Servo Wedge and Serial Number
  There are 88 equally spaced servo wedges per track. A servo wedge contains SYNC, servo address mark (SAM), track index, track number and ABCD burst information. The relative amplitude of each A, B, C and D burst provides position information (relative to track center) for each data head. Servo wedges are written at 1/3 track intervals on every data surface. The laser positioning system provides the precise position feedback needed for the servo writer/data head positioning servo loop. In addition, if the heads go off track while writing servos, the current track will be rewritten, starting at the previous written track. If timing lock is lost (from the clock track) while writing servos, then the current track will be rewritten. Both excessive off-track errors or lost lock errors will abort and fail the servo write process. Serial numbers are also written on the cylinder -TBD.

  If the operation is unsuccessful, then FAIL

- Verify Servo Wedges
  Verify all servo wedges on the system cylinders, of all heads.
  Allow no defective wedges on the system cylinders.
  Verify only the top (worst) surface, for the rest of the tracks.

  - Off Track Test:
    Track type is the remainder of the track number divided by 4

Track type 1	If A_avg > C_avg or A_avg > D_avg then error.
Track type 2	If C_avg > B_avg or C_avg > A_avg then error.
Track type 3	If B_avg > C_avg or B_avg > D_avg then error.
Track type 4	If D_avg > A_avg or D_avg > B_avg then error.

  - Track PES:
    If |PES_avg - prev_PES_avg| > limit (**TBD**%)then ERROR

    Where Position Error Signal (PES) is

Track type 1	PES = D_avg - C_avg.
Track type 2	PES = A_avg - B_avg.
Track type 3	PES = C_avg - D_avg.
Track type 4	PES = B_avg - A_avg.

    This test measures track location with respect to the previous track and indicates track squeeze.

  - Average A+C to B:

Track type 1	IF (C_avg + D_avg - B_avg) > limit (**TBD** %), then error.
Track type 2	IF (A_avg + B_avg - D_avg) > limit (**TBD** %), then error.
Track type 3	IF (C_avg + D_avg - A_avg) > limit (**TBD** %), then error.
Track type 4	IF (A_avg + B_avg - C_avg) > limit (**TBD** %), then error.

  This test is used to detect a bit shift between half tracks during a write. A bit shift will cause a small increase in amplitude of the AGC compensated A and C bursts, for which this test is designed to detect. This test is only valid if read head element is smaller than 2/3 of the track pitch.

- Index
  Check that the index is present.

- Wedge Error Overflow
  If # of soft errors (wedge errors) > limit then ERROR

- Wedge
  Wedge tests are performed for each wedge.

- A/B/C/D Tests (| A avg - A | , etc.)
  This test compares each burst amplitude on track "N" with the average from that of track "N-4". This is done because the pattern repeats every 4 tracks . This test was designed to detect media defects.
  If | A_avg - A | > limit (**TBD**) then ERROR
  If | B_avg - B | > limit (**TBD**) then ERROR
  If | C_avg - C | > limit (**TBD**) then ERROR
  If | D_avg - D | > limit (**TBD**) then ERROR

- AGC Tests
  This test will detect a low amplitude AGC field.

  If AGC voltage < limit (**TBD**) then ERROR

- TNA, SYNC, SAM or ID
  This test checks the servo wedges for missing sync, SAM, or index. TNA errors may be caused by media defects or poor S/N ratios. Also checks SAM to SAM timing.

- Track number
  This test checks that the correct gray code track numbers are read.

- Wedge PES
  Track types 1 and 3 (odd): If | (C-D) - (prev_odd_wedge_C - prev_odd_wedge_D) | < limit (**TBD** %), then error.
  Track types 0 and 2 (even): If | (A-B) - (prev_even_wedge_A - prev_even_wedge_B) | < limit (**TBD** %), then error.

- Track Errors
  If Track error(s) is(are) reported during verify, then retry track verify 3 times.
  If track errors reported on 2 out of 3 retries, then FAIL VERIFY.

- Wedge Errors
  If #_of_Bad_Wedges > 1 then FAIL Verify
  If number of soft errors > limit then FAIL.

  A wedge is bad if, and only if, verify reports errors for a wedge (hard wedge error) on 2 out of 3 retries.

9.3 HDA Test

The HDA Test will be done on a sample basis during mass production. It will be used to determine the consistency of parametric distributions resulting from the head/disk interface. It is used for qualifying head and media vendors during the pre-production builds.

The HDA Tester consists of a 486 PC operating a LeCroy 7200A (Digitizing Oscilloscope) through a GPIB port. The HDA under test is connected to the LeCroy via a captured product board and a converter board.

Since the LeCroy 7200 is a digitizing oscilloscope, there are practical limitations on the amount of sample points that can be stored and analyzed in a reasonable amount of time As a result, the data sample for the parametric tests is gathered by looking at a "segment" of the wedge to wedge data area between the 88 servo wedges.

The tests that are performed by the Analog Parametric Tester are organized below by the read/write patterns they employ.

9.3.1 System Initialization

System Initialization is done to spin up the HDA and set up the LeCroy scope for operations.

- HDA Spin Up
  Power is applied to the captured product board, which results in the HDA and product board "coming ready" as a drive system.

- Verify and Reset LeCroy Scope
  The LeCroy goes through a brief reset and self checking routine.

- Check LeCroy Configuration
  The host computer ensures the LeCroy is correctly configured.

9.3.2 Load RAMWare

The load RAM Ware sequence is done to configure the RAM memory on the PCB and read the HDA serial number for the TEST.OUT file.

- Auto Detect
  The Auto Detect feature in UPT determines the drive model. This is done by interrogating the interface, to determine if it is AT or SCSI, and then reading the drive model number with inquiry commands.

- Write Buffer
  The Write Buffer command is used to set up the drive's memory and load the RAM Ware onto the drive.

- Modify Config Page 16
  Configuration page 16 is modified to disable the power saving mode. This will keep the preamp on during the test.

- Load Pages 10, 17, etc.
  Configuration pages 10 and 17 are then loaded into the drive's memory. TBD other pages may be loaded.

- Read Drive Serial Number
  The drive serial number is then read from the substituted Gray code on cylinders TBD (see servowriter station) and stored in the PC's on-board
  memory.

- Calibrate Micro-Jog
  We must compensate for the offset between the read and write elements in MR heads. The offsets are different for each zone and head, and must be measured at program startup.

Throughout the test, after writing but before making any measurement, a microstep operation will be performed to place the read element directly over the written data.

9.3.3 HF and LF Frequency Testing

Several measurements are made and tested against limits during this test. They include Amplitude (both HF and LF), Resolution, Modulation, Overwrite, and Phase Distortion..

The HF and LF frequencies are zone dependent. The HF frequency is 1/4 of the write clock frequency and the LF frequency is 1/12 of the write clock frequency. Prior to writing and reading the test patterns, a DC erase is performed.

- HF TAA

  HF TAA (Track Average Amplitude) measures the average peak-to-peak amplitude of the read back signal after writing a simple, repeating high frequency pattern.

  It is measured for zones TBD by writing the HF frequency (for the zone) on each head. The wave form may be rewritten and read back several times if required by measurement variability.

  The average HF TAA in each of the 88 segments is calculated and stored. From that the reported HF TAA is calculated by averaging the results of each segment together.

  HF TAA is performed in order to measure the signal strength of the read back wave form and to calculate modulation.

  Successful result: TBD

- LFTAA

  LF TAA measures the average peak-to-peak amplitude of the read back signal after writing a simple, repeating low frequency pattern.

  It is measured for zones TBD by writing the LF frequency (for the zone) on each head. The wave form may be rewritten and read back several times if required by measurement variability.

The average LF TAA in each of the 88 segments is calculated and stored. From that the reported LF TAA is calculated by averaging the results of each segment together.

LF TA A is measured in order to calculate resolution.

- Resolution

Resolution is expressed as a percent and is easily calculated from the results of the HF TAA and LF TAA measurements. It serves as a crude approximation of the frequency response for the write/read signal path and is primarily used to gauge the effects of inter symbol interference in the head/disk interface.
The formula is as follows:

$100*(TAA_{HF}/TAA_{LF})$.

Resolution is reported for every head in each zone that HF TAA and LF TAA measurements are made.

Successful result: TBD

- Modulation

Modulation is a measure of how much the read back amplitude on a track is varying and is expressed as a percentage of deviation from the average. Positive modulation measures the deviation above the average and, correspondingly, negative modulation below the average. It is determined by establishing which of the 88 segments has the lowest and highest average HF TAA readings. It is primarily used as an indicator of "once around" variations in the magnetic film on the disk or repeatable run out in the HDA. It is easily calculated by dividing the minimum and maximum values by the average, subtracting 1 and multiplying by 100.
The formula is as follows:

Positive Modulation: $100*((\text{Max HF } TAA_{seg}/\text{Ave HF HF } TAA_{seg}) - 1)$

Negative Modulation: $100*(1 - (\text{Min HF } TAA_{seg}/\text{Ave HF HF } TAA_{seg}))$

Modulation is reported for every head in each zone that HF TAA measurements are made.

Successful result: TBD

- Overwrite Test

The Overwrite Test is designed to measure the ability of a head to erase a data pattern by writing directly over it. Since the worst case is a low frequency pattern overwritten by a high frequency pattern, that sequence is used in the test. Overwrite is used as a primary measure of head performance.

The test is accomplished by AC erasing the track being tested, as well as TBD % off-track an either side, to remove contributions from any previous data on the track. A low frequency (LF) pattern is written once around, and read back measurements are made (in dBV) using a Fourier transform to determine the power level at LF. Then a high frequency (HF) pattern

is written once around. and read back measurements are made (in dBV) using a Fourier transform to determine the power level at LF. The sequence may be repeated several times and averaged if required by measurement variability.

The overwrite value is expressed in decibels (dB) and is the difference between the TAA of the original low frequency pattern and the overwritten (or residual) TAA of the same low frequency.

The formula is as follows:

OW(dB) = LFdBV-ResdBV

Where:
LFdBV = LF TAA measurement in dBV
ResdBV = Residual LF TAA measurement in dBV

Successful result: TBD

9.3.4 Isolated Pulse Testing

Isolated pulse testing is done by writing a very low frequency pattern in order to ensure the read back pulses have no effect on each other. The frequencies used are zone dependent and correspond to 1/32 of the write clock frequency. Prior to writing and reading the test pattern, a DC erase is performed.

- PW50 Test

  PW50 is the primary variable used to characterize the shape of read back pulses. It is accomplished by measuring the width of a read back pulse which is isolated (i.e. far away) from neighboring pulses. The measurement is made by determining the peak amplitude of the pulse then measuring its width (in nanoseconds) at 50% of the peak amplitude. PW50 is an essential measurement for monitoring the effects of inter symbol interference. In the PRML read channel, PW50/T, where T is the clock period, is an important parameter for optimized read channel performance

  PW5O is measured for zones TBD on each head. The wave form may be rewritten and read back several times if required by measurement variability.

  The sampled wave forms from the 88 segments are stored and the reported PW5O is calculated by averaging the width of the stored pulses.

  Successful result: TBD

- Asymmetry Test

  MR heads sometimes produce more current for positive than negative pulses (or vice-versa). Asymmetry is measured by comparing the average amplitude of positive pulses (referenced to base) with the average amplitude of negative pulses.

  Asymmetry is measured for zones TBD on each head The wave form may be rewritten and read back several times if required by measurement variability.
  Asymmetry (%) = Abs(negAvg - posAvg)/AvgPkPk * 100

  Successful result: TBD

9.3.5 Pseudo Random Pattern Testing

Pseudo random pattern testing is done by writing a 127-bit pseudo random pattern. The pseudo random pattern is derived from the polynomial $X^7 + X^3 + 1$ The read back wave form is read several times and an averaged wave form is processed by the LeCroy Digitizing Oscilloscope.

This testing is done on all heads in zones TBD.

- Non-Linear Transition Shift

  An accurate measurement of non linear transition shift is an important consideration for optimizing the write pre-compensation values. The phenomenon results from transitions being physically shifted from their proper positions as a result of demagnetization from a neighboring transition during the writing process. Non linear transition shift is primarily associated with media performance.

  Note that this phenomenon is different from linear transition shift (otherwise known as inter symbol interference) that results in shifting of the amplitude peak in the read back wave form due to linear, superposition effects.

  The measure of non-linear transition shift is expressed as a percentage of the clock period.

  Successful result: TBD

- Signal to Noise Ratio

  The signal to noise ratio is the primary measure of how much noise is in the write/read signal path. Signal to noise is used as a primary indicator for soft error rate performance.

  The signal to noise ratio is automatically calculated by the LeCroy Digitizing Oscilloscope by correlating the read back wave form to itself using an onboard "auto correlation" function. The measurement is made by shifting the read back wave form by a multiple of the clock period and calculating a correlation coefficient., R, between the original and shifted wave forms. The signal to noise ratio is easily derived from the correlation coefficient.

  The equation is as follows:

  $$SNR = 10*\log10(R/(1-R))\ dB$$

  Successful result: TBD

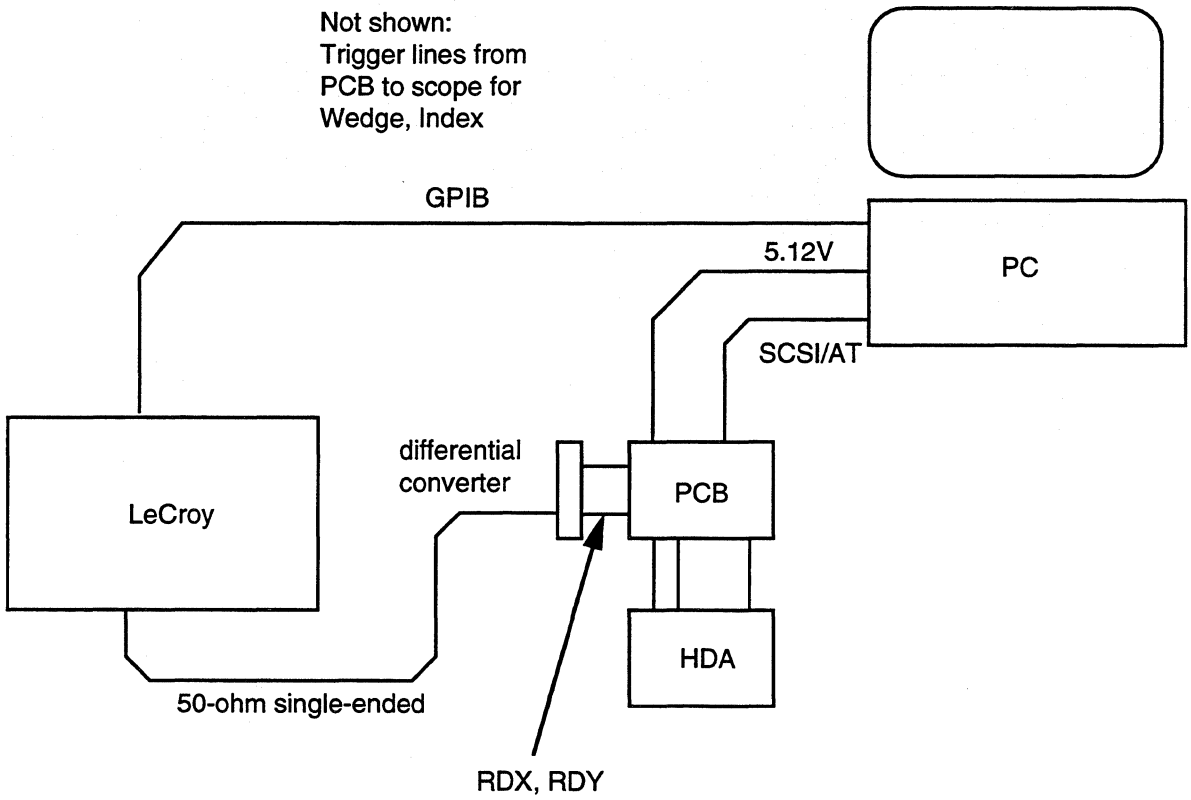

Figure 9-1 AP Tester Hardware

9.4 PCB Test (Pre Production-MP)

This test is run on a slave HDA, with pogo pin connectors and an external current detection board. This test is run on every PCB, and is limited to 40 seconds. The only things we should test here, are things which can't be tested anywhere else, or features which will screen out potential line failures in a minimum time.

- Autodetect
  This test determines and initializes the drive interface.

- RAMware Download
  This test loads the ramware.

- RAM test
  This test performs write/read/compare of the RAM memory, so that to verify the integrity of the DRAM. This is done for all data and address lines.

- Seek Test
  This test is performed to verify the integrity of the servo control circuitry, actuator, and motor. This is accomplished by performing TBD seeks with TBD stroke.

- PCB Read/Write Test
  This test checks the functionality of the read/write circuitry. It is accomplished by formatting track, writing it with specified pattern, and reading back with full compare. It is done for one cylinder in each zone to verify that thw PCB works at all frequencies the drive will require. No unrecoverable defects are allowed.

- LED Test
  This test is to verify the functionality of the LED circuitry

- DMA test
  This test is to verify the functionality of the DMA path and capability of DMA data transfer. It is accomplished using a short write/read sequence in the enabled DMA mode (assuming the AT adapter capable of DMA will be available).

9.5 Digital Scan (Pre Production-Pre_MP)

This process is a series of test which are designed to tell us as much about the drives as possible before we get into production. The results of these tests should give us enough information to optimize the drive design, and the test process as we approach mass production.

Since this test will be eliminated before mass production, the test time is not critical, but should be kept under 12 hours in order to give us feedback in a reasonable time.

- Load RAMWare

- Equalizer Training
  Load the default configuration page 10 right after power-up.
  Write twice to the system track a pseudo-random sequence (PRS) with sync. mark. (On chip PRS should be used and, and the seed generator will be pre-determined.
  Assert read gate for at least 4 sectors.
  Ignore ECC errors.
  Read back all internal values of FIR, DFE, and AGC registers.
  Store the new value as the default value.
  If disk-ware down-load is unsuccessful, an adaptive value of FIR, DFE, and AGC should be replaced in RAM then retry disk-ware again. If diskware is successful with the new values, then they should be stored on the system track.

- Initialize System Cylinder
  First the serial number is read from the HDA. Test the system cylinders: verify wedges, defect scan, and format in-line.

- Load Diskware/ Initialize Firmware
  Load diskware, configuration pages; initialize firmware defaults, and clear defect lists.

- Wedge Verify.
  Verify servo wedge. Use this data to measure the effectiveness of the verify test in Servo Writer station.

Number of times wedge must pass	TBD
Number of bad tracks	TBD
Max. number of bad wedges per track	TBD

- KLOOP Calibration
  This is a new procedure, which moves the actuator to several locations, and performs a single frequency Bode measurement. This information is used to compensate for variations in magnets. This information is written on the drive, and used to aid in the power-up, recal procedure.

- Start / Stop - Power Cycle.
  Start / Stop for TBD cycles, waiting TBD seconds after stop and TBD seconds after start.

  Fail if start up time is > TBD seconds.
  Fail if stop time is > TBD seconds.

- Random Seek.
  Measure seek time for 5000 random seeks with read on arrival enabled.

  Max. TBD ms.

- Sequential Head Switch Time.
  Measure sequential head switch times from OD to ID with read on arrival disabled. Calculate what percentage are above TBD ms. Head switch from last to 0 includes a single track seek, and should be counted independently.

  TBD percent allowed > TBD ms for head switch time within the same cylinder.
  TBD percent allowed > TBD ms for single track seek (head switch across cylinder).

- Fixed Length Seek Time.
  Seek sequentially from cylinder 0, incrementing by 1 cylinder until reaching maximum cylinder. Do the same thing back to cylinder 0. Repeat for increments of 2, TBD..., and max cylinders.

Stroke length	Iterations	Limits (ms)
1		TBD
Full		TBD

- Servo Dump
  Reads servo constants. This test is informational only. No Pass / Fail criteria
  Number of locations across stroke (number of places to measure) TBD

- Head Gain
  This is an informational test to help set optimal design parameter (head gain). The test is performed on the inner cylinders of each zone.
  No Pass / Fail criteria

- Guard-band Erase.
  For each track, on each head, move off-track in both directions, and erase. This removes any noise from the guard-bands.

- Adaptive Equalization.
  - Adapt the following parameters:
    Load default configuration page 10, right after power-up.
    Microjog.
    Filter boost.
    Current bias.
    VGA gain.
    VCO center frequency.
    VCO ZPR.

  - MSE Test
    Measure mean square error using the LITE chip; on and off-track.

  - Measure HDA Parametrics.
    TBD

  - Partial Response Amplitude margin
    Measure amplitude margin for a random data pattern.

- Format.
  Sector format the drive.

- Format Inline, (with move ID feature).
  Format with inline spares; this version uses the "move ID" feature to allow the drive to recover some sectors with defects in the ID field.

- Physical Sequential Stress Write/Read with ECC Disabled
  Defect scan with intelligent scratch-fill which retests adjacent and error tracks. Physical scans are performed with ECC on-the-fly disabled for raw error rate.

  Scan defects with TBD patterns (TBD, ..., and random). For all patterns, do 1 write loop, TBD read loops, 3 read retries, and 3 write/read retries for defective sectors. Read on arrival is disable. For Random patterns, scan at high threshold, offtrack at -TBD%, TBD%, and TBD%. For other patterns, scan at mid threshold, offtrack at TBD%, 0%, and TBD%. All hard and soft defects are logged in the defect list. Soft defects will be changed

to hard if found again in the later test patterns

	1 Disk	2 Disk	4 Disk
Maximum hard defects per drive	TBD	TBD	TBD
Maximum hard defects per head	TBD	TBD	TBD
Maximum hard defects per cylinder	TBD	TBD	TBD
Maximum seek errors per drive	TBD	TBD	TBD

- Format Inline, (with move ID feature).
  Format with inline spares; this version uses the "move ID" feature to allow the drive to recover some sectors with defects in the ID field.

- Logical Sequential/Random Write/Read with H/W ECC Enable
  Soft error rate test using sequential and random seek patterns. Soft error is defined as any recoverable error that occurs only once. This test is used to make sure no additional hard and non-recoverable defects are found after format inline. Test algorithm as follows:
  - Sequential write/read the drive with TBD data pattern.
  - Run TBD random seek writes with a random data pattern.
  - Run TBD random seek reads.
  - Sequentially read the entire drive.
  - Repeat loop.

  Allow TBD hard and TBD non-recovered errors.
  All hard errors and non-recovered errors are logged in the selfscan defect list and then reas signed.
  Soft error limit is 1 in $10E^{TBD}$ bits transferred.
  Raw error limit is 1 in $10E^{TBD}$ bits transferred.
  Hard errors allowed is TBD.
  Non-recovered errors allowed is TBD.
  Read bump limit is TBD.
  Write bump limit is TBD.
  Double burst recovered error limit of $10E^{12}$

- ECC Test
  Perform test on ID and OD, sampling 10 times each pattern. Corrupt data byte(s) and verify correction. Verify detection of large ECC errors.

- PERR.
  Measures RRO / NRRO for 200 revs on cylinders 0, max/4, max/2, 3max/4, max.

Maximum NRRO	TBD%
Maximum RRO	TBD%

- Null.
  Measure actuator current in track following mode and compares to fail limits.

  Number of locations across stroke (number of places to measure) TBD

- Off Track.
  Measures the ID and OD offtrack read capabilities for all heads and all zones of the drive. Measurements are taken at the ID cylinder of each zone. 5 retries in verifying good test track with 2T pattern and high threshold. 1 retry offtrack measurement. Write random patterns on test tracks, and their adjacent tracks. All tracks are written on track.

  Allowed 10 read errors in 10E7 bits transferred. Start from TBD% down to TBD%. Minimum offtrack read capabilities is TBD%.

- Sequential Throughput.
  Sequential throughput test using random and 0x50 data patterns, (256 blocks per transfer for AT products) transferring 10MB data on OD. Should this be done on tracks without off-line spares?

  Minimum rate for AT TBD

- Random Throughput.
  Random throughput test using random and 0x50 data patterns, 1 block per transfer for 2000 blocks.

  Minimum rate for AT TBD

- Save Test Results

9.6 Diskware Station (Pre MP-MP)

The diskware download station prepares the drive to write data to the system cylinders. It downloads the diskware and sets up the drive to execute SelfScan when power is applied. The download station is running under the software control of the UPT2 program.

- Load RAMWARE
  At this step we will load the necessary additional firmware, to run in conjunction with the ROM firmware to perform the functions needed to allow the functionality required.

- Auto Detect
  Auto Detect determines the drive model. This is done by interrogating the interface, to determine the drive type, and number of heads.

- Write Buffer
  The Write Buffer command is used to download the RAMWARE into the DRAM buffer.

- Load Configuration Pages
  The appropriate Configuration pages are then loaded into the drive's DRAM buffer.

- Read Drive Serial Number
  The drive serial number is read from the location written at the Servo Writer stage and stored in the drive's DRAM buffer, and written in the appropriate Configuration page.

  Due to the utilization of the PRML channel and MR heads, optimization of the heads and media must be accomplished, and micro-jog values must be determined before data can be reliably written to the system cylinders. Once these optimization and micro-jog values have been determined, the following steps can be performed, in preparation for the actual writing of DISKWARE to the media.

- Format System Cylinders
  Performing a low level format on the dive is necessary before any data can be written. Only the system cylinders need to be formatted at this point. The data cylinders are formatted after defect scanning is completed during SelfScan.

- Defect Scan and In-line Sparing
  A brief defect scan is performed prior to writing the system cylinders. Any defects found are spared in-line.

- Load Diskware
  DISKWARE is the portion of the firmware that will eventually be stored to the media and loaded into the drive's DRAM buffer at power up. It is sometimes referred to as RAMWARE while it is resident in the DRAM buffer (i.e. before it is actually stored on the media). The following commands and operations are required to perform the DISKWARE downloading to the DRAM buffer.

  -Write Buffer (Download)
  The Write Buffer (with Download option) command is used to load the drive firmware and the SelfScan firmware onto the system cylinders.

  -Write Configuration Pages
  The Configuration pages are then written onto the system cylinders

  -Initialize System Cylinders
  The system cylinders are initialized to prepare the drive for the remaining steps in the test process.

  -Write Format File
  The format file (.FMT file) is written onto the system cylinders. The format file will be used to do a low level format during SelfScan.

  - Initialize Defect Lists
  The P-list, G-list, and W-list are set up with no entries on the system cylinders.

  -Load SelfScan Script
  The SelfScan script is loaded by copying the SSO File to the system cylinders. The SelfScan password is enabled in the file so the SelfScan sequence will execute automatically the next time power is applied to the drive. The SelfScan execution can also be initiated via jumpers.

9.7 Self Scan Test (Pre MP-MP)

This process is a self-contained series of tests which are the core of our testing. All features of the drive which can be tested internally should be tested here.

The 'script' for this station is written on the drives negative cylinders at the Diskware station. The script to automatically run this test is also loaded at Diskware, and the password removed at the end of the Self scan test. The Self scan script is kept on the drive, and can be invoked at any time by sending the drive the self-scan superset command. Each routine saves data to the negative cylinders. Any additional data required, (defect lists, etc.), will be saved on other locations as directed by software. The data collected in this test is retrieved at the final scan station.

- Servo Verify
  This command is executed with the equivalent of "tightened" bump and defect limits. Every wedge on the entire drive is inspected. Once a wedge is deemed to have repeatable defects in the SAM, ID, Sync, gray code, or bump detect areas, an entry will be made in the Servo Defect Map, which resides on the System Cylinders. This map is loaded on every power up, and is referred to for each seek during normal operation. In the case of a match to the destination track, both the previous wedge position information and estimator values are used to help in determining accurate position information upon arrival.

  There is a limit of one servo defect per track. If two servo defects are found on any track, it is considered a fatal error, and the test fails. The drive must be rewritten at the servo writer in this case. There is also a limit of 306 total servo defects per drive.

	7 4	3 0
0	Status	
1	Cylinder - lsb	
2	Cylinder - msb	
3	Not Used	Head
4	Wedge Number	

Table 9-1 Servo Defect List Descriptor

Status Byte:
Bit 0: PERR out of range
Bit 1: Track ID error
Bit 2: Not used
Bit 3: Defect
Bit 4: Bump error
Bit 5: Data error
Bit 6: Sync error
Bit 7: SAM error

- Stability Margin Test.
  This is a new test designed to adjust servo gain at several locations, and check for loss of servo lock.

- NULL Calibration
  This is a new test, which plots the null current in both directions at several points, and writes these values to the drive. These values will be used at drive power-up to reduce the number of measurements, and improve power-up time.

- SAM to SAM Profile Calibration
  This is a new procedure, which plots the timing of the SAMs around the track. This information is used to aid in motor speed calculations.

- KLOOP Calibration
  This is a new procedure, which moves the actuator to several locations, and performs a single frequency Bode measurement. This information is used to compensate for variations in magnets. This information is written on the drive, and used to aid in the power-up, recal procedure.

- VSCALE Calibration
  This is a new test which measures the deceleration profile of the actuator; and calculates the initial VSCALE factor, and feed-forward value. These values are stored on the drive, and used to aid in the power-up recal procedure.

- Buffer RAM Test.
  Writes known pattern to memory, and read/verifies for data miscompares. Test all areas of the buffer RAM including code, cache, and firmware data areas. The test runs comple mentary patterns.

  Fail if any error.

- Start/Stop.
  Start / Stop for 5 cycles, waiting 5 seconds after start. This test measures the minimum, average, and maximum start/stop times.

  Fail if start-up time is > TBD seconds.

- Random Seek.
  Measure seek time, (average and maximum), for 5000 random seeks with read on arrival enabled.

  Max. TBD ms.

- Head Switch/ Single Track Seek.
  Measure sequential head switch times from OD to ID with read on arrival disabled. Calculate the percentage above TBD ms. Head switch from last to 0 includes a single track seek, and should be counted independently.

  2 percent allowed > TBD ms for head switch time within the same cylinder.
  2 percent allowed > TBD ms for single track seek (head switch across cylinder).

- Full Stroke Seek Time.
  Seek from ID to OD, and OD to ID TBD times, measure maximum minimum and average seek time.

- Guard-band Erase.
  For each track, on each head, move off-track in both directions, and erase. This removes any noise from the guard-bands.

- Adaptive Equalization.

  - Adapt the following parameters:
    Load default configuration page 10, right after power-up.
    Microjog.
    Filter boost.
    Current bias.
    VGA gain.
    VCO center frequency.
    VCO ZPR.

  - MSE Test
    Measure mean square error using the LITE chip; on and off-track.

  - Measure HDA Parametrics.
    TBD

  - Partial Response Amplitude margin
    Measure amplitude margin for a random data pattern.

- Wedge to Wedge Scan.
  This is a sequential test used to detect defect, particularly in the areas which are normally overwritten with header information. Several patterns and marginalizing techniques are used.

- Format.
  Format the drives data tracks.

- Format Inline, (with move ID feature).
  Format with inline spares; this version uses the "move ID" feature to allow the drive to recover some sectors with defects in the ID field.

- Physical Sequential Stress write / read with ECC disabled.
  This is a sequential defect scan. Physical scans are performed with ECC on-the-fly disabled for raw error rate.

  Scan defects with TBD patterns (TBD,..., and random). For all patterns, do 1 write loop, TBD read loops, 8 read retries, and 8 write/read retries for defective sectors. Read on arrival is disabled. For TBD patterns, scan at raised slice levels, off-track at TBD%. For other patterns, scan at uneven slice levels, off-track at TBD%, plus additional PRML

specific stress options. All hard and soft defects are logged in the selfscan defect list. Soft defects will be changed to hard if found again in the later test patterns.

	1 Disk	2 Disk	4 Disk
Maximum hard defects per drive	TBD	TBD	TBD
Maximum hard defects per head	TBD	TBD	TBD
Maximum hard defects per cylinder	TBD	TBD	TBD
Maximum seek errors per drive	TBD	TBD	TBD

- Defect Verify / Scratch Check.
  For every defect encountered during physical sequential defect scans, retest TBD tracks before and after the defective track, and the defective track for possible scratch. Use TBD patterns (TBD). For each pattern, do 1 write, TBD reads, 8 read retries, and 8 write / read retries on the defective sectors.

  There is no pass / fail limit. All additional defects are flagged.

- Format Inline, (with move ID feature).
  Format with inline spares; this version uses the "move ID" feature to allow the drive to recover some sectors with defects in the ID field. Factory defect list (P list) and working defect list (W list) are created.

  One or more track format error fails the test.

- Logical Sequential/Random write/read with H/W ECC enabled.
  Soft error rate test using sequential and random seek patterns. Soft error is defined as any recoverable error that occurs only once. This test is used to make sure no additional hard and non-recoverable defects are found after format inline.
  Test algorithm as follows:
  - Sequential write/read the drive with TBD data pattern.
  - Run TBD random seek writes with a random data pattern.
  - Run TBD random seek reads.
  - Sequentially read the entire drive.
  - Repeat loop.

  Allow TBD hard and TBD non-recovered errors.
  All hard and non-recovered errors are logged in the selfscan defect list and then reassigned.
  Soft error limit is 1 in TBD bits transferred.
  Raw error limit is 1 in TBD bits transferred.
  Hard errors allowed is TBD.
  Non-recovered errors allowed is TBD.
  Read bump limit is TBD.
  Write bump limit is TBD.
  Double burst recovered error limit of 1 in 10^{12} bits read.

- Head Stability Test.
  Measure the variation of TAA due to writing; i.e. amplitude covariance.

- ECC Test.
  Perform test on ID and OD cylinders, sampling 10 times each pattern. Corrupt data byte(s) and verify correction. Verify detection of large ECC errors.

- Runout.
  Test for repeatable run out (RRO) and non repeatable run out (NRRO) by invoking the self scan command "RRO/NRRO" for 200 revolutions on cylinders 0, max/4, max/2, 3max/4, and ID.

  RRO and NRRO limits are TBD%

- Null Test.
  The form of this test may change from previous products, to collect additional data..
  Measures actuator current over the full stroke, ID to OD, and OD to ID.

- Sequential Throughput.
  Measure throughput from the disk to the drive RAM, in order to reduce or eliminate the need for this test in final station. While this is not a complete throughput test, most of the potential problems should show up here; and no host limitations will influence the results. This is done by transferring large sequential block to verify data and retry rates meet spec.; the accuracy of this measurement will be related to the time run.

- Random Throughput.
  This is the same as the sequential throughput test, except random blocks are transferred.

- Random Seek.
  Measure seek time, (minimum, average and maximum), for 5000 random seeks with read on arrival enabled.

  Max. TBD ms.

- Start/Stop.
  Start / Stop for 5 cycles, waiting 5 seconds after start. This test measures the minimum, average, and maximum start / stop times.
  Fail if start-up time is > TBD seconds.

- Delete Password
  Delete password indicating Self Scan is not to be run during the next power-up.

9.8 Final Station (Pre Production-MP)

The station is used to test the drive through the interface, and to collect all the selfscan information. This is also the station that should simulate the customer environment.

- Servowriter Report
  This procedure dumps the data written by the servowriter (serial number, model and servowriter version number).

- Selfscan Report.
  The selfscan results data are read from the disk and interpreted. The calculations for soft error rate are done.

- Start/Stop.
  The test is designed to verify the drive functionality after power-up, check recal consistency. The drive is repeatedly powered down and up and the time for the drive to get ready is measured.

- Read/Write/Full Compare Test.
  This procedure verifies the drive's ability to reliably rewad and write through the interface.

- Logical Sequential Test.
  This procedure writes and reads specified amount of data, checks the integrity of drive's defect lists. The worst case pattern is used and no unrecovered defects are allowed.

- Throughput Test.
  Measures the thoughput from the drive to the host. The rate is a measure of the time to read or write the data, including loss due to retries or soft errors, seek errors, or drive problems. It is TBD if both the sequential and random throughput measures will be used.

- Configuration.
  This operation configures the drive as the generic drive.

- Write Results
  Writes the TEST.OUT file to the host. This is includes the results of the selfscan and the final test.

Appendix A Schedule and Major Model Milestones

				Quantity		
		Goal	**Location**	**HDAs**	**SCSI**	**AT**
Oct	10/93	E1 build	Quantum	10		
Feb	23/94	E2 build	Quantum/MKE	25		
Jun	13/94	P0 SCSI	MKE (HDA only)	50	50	0
Aug	19/94	P0 AT	MKE (HDA only)	50	0	50
Nov	07/94	P1 build (2Disk)	MKE	600	0	800
Dec	xx/94	P1.5 build (4Disk)	MKE	800	0	
Feb	13/95	P2 build	MKE	1000	0	1000
Apr	03/95	Mass production	MKE	large	0	large

Table A-1. Scheduling goals from E1 build through mass production.

	E1	E2	P0 SCSI	P0 AT	P1	P2
Hardware Level	• Modified Daytona mechanics • Modified Daytona electronics • 84910 channel • Koni controller • TI 21010 Preamp • 3100 TPI heads	• HDA built at MKE • E1 electronicsE1 electronics •5000 TPI heads	• Leo SCSI controller • PRML Lite read channel • K7 µProcessor • In form factor • HDA built at MKE	• Neptune controller • PRML Lite read channel • K7 µProcessor • In form factor • HDA built at MKE	• "Mass Pro" HDA • MKE-built PCB	"Mass Pro" HDA • Final Preamp
Objective	• Preliminary Code Development In-drive MR head eval • EVT tests: mechanical, electrical motor control optimization, preamp evaluation	• MKE MR Head Process Trial EVT1 units • HDA Characterization • Density demonstration	• Code & Electronics debug	• Code & Electronics debug • Head/media DOE • CSS testing • EVT2 testing	• DVT • Mfg process trial • Customer Demo units	• DMT • Confirm mfg. & test process • Customer qual units
Acceptance Criteria	• EVT1 plan signed off	• No ESD induced head yield loss during assembly process • Complete execution of EVT1 • DEMO 5000 TPI, 95KFCI • EVT2 plan signed off	• P0 SCSI Leo SCSI controller	• DVT plan signed off • Complete execution of EVT2	•Acceptable integration into 2 top customers' systems • Complete execution of DVT • Yield 80% min. • Drive meets perf. specs.	• Product quals begun at key customers • Complete execution of DMT • Yield 90% min.

Figure A-1 Models defined

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Appendix B Standards

Europa drives will meet the following regulatory specifications:

Underwriter Laboratory (UL)

Europa drive will meet the current edition of UL 1950, Standard for safety: Information technology equipment including business equipment.

Locked Rotor Test acceptable for UL 1950, No.950 will be included as part of UL Certification.

UL Recognition shall be obtained without any special or unusual conditions of acceptability. A copy of the UL Recognition Report, including Conditions of acceptability, will be provided.

The drive will bear the UL required identification markings which provide proof of UL Recognition. Use of the UL backwards "UR" is preferred.

Canadian Standards Association (CSA)

Europa drive will meet the current edition of CSA - C22.2 No. 950-M89.
information technology equipment including business equipment.

Locked Rotor Test acceptable for CSA 22.2, No. 950 will be included as part of CSA Certification.

CSA Certification shall be obtained without any special or unusual conditions of acceptability. A copy of the CSA Certification Report, including Conditions of acceptability, will be provided.

The drive will bear the CSA required identification markings which provide proof of CSA Certification.

European standards (VDE and TUV)

Verband Deutscher Electroechnier (VDE)
Technisher Uberwachungs Verein (TUV)

Europa drive will meet the current edition of EN 60 950. European Community Regulations for safety of Information technology equipment including Electrical business equipment and IEC950, Safety of Information technology equipment including Electrical business equipment.The drive will also meet the requirements of DIN/VDE 0805,Safety specification for business machines.

Locked Rotor Test acceptable for EN60 950 and IEC 950 will be included as part of VDE and TUV approval.

Approval shall be obtained without any special or unusual conditions of acceptability. A copy of the report, License and Construction Data Forms will be provided.

The drive will bear VDE or TUV required identification markings which provide proof of VDE and TUV approval.

FCC

FCC Rules for radiated and conducted emissions, Part 15, Subpart J, for class B equipment.

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Appendix C Packing

General Information

Quantum seeks not only to ship products that provide the latest in technological features, but also to ensure that these products arrive at the customer's site in the same condition that they left our factories.

Shipping Containers

Two (2) sizes of shipping containers will be required for Europa products. These are:

1. 1-Pack Shipping Container
2. 32/36-Pack Shipping Containers.

The 1-Pack Container hold one (1) disk drive, and the 32/36-Pack holds thirty-two/thirty-six (32/36).

* The shipping containers shall be sufficient to protect the parts enclosed, and must comply with the packaging requirements of the latest issue of Uniform Freight Classification Rules, or other applicable carrier requirements.

* The containers are intended for single-use.

* Container sizes should be selected such that when arranged upright on a 4-way 40"Wx48"D pallet, the containers do not overhang the edges of the pallet deck. Containers when arranged on the pallet, should maximize utilization of the pallet deck area and the available 48" load height.

* Closures must permit handling without specific precautions.

* The corrugation used in these containers must have sufficient strength to prevent collapsing of the container under double stacked pallet loads.

Identification

* Each shipping container must be identified on sides #3 and #4 (See Figure C-2) with the following basic information:

    A. Quantum Logo
    B. Symbols to indicate:
        1. The proper orientation of the TOP of the container.
        2. The container contents are FRAGILE.
        3. The container should be protected from water, rain, etc.
        4. The container contents are sensitive to static electricity.

* The following letters should appear on side #5: "_ of _". This permits identifying each container as part of a group with a marking pen, e.g. 5 of 12.

Documentation

* 1-Pack Carton: TBD
* 1-Pack Insert: TBD
* Desiccant: TBD
* Anti-Static Bag: TBD
* Static Warning Label: TBD

Packaged Finished Goods Product Shock & Vibration Test Standards

This section outlines the laboratory test levels required to assure the arrival of Quantum Finished Goods (F/G) products to the end user without damage or loss of performance beyond the published specifications. The packaged products must be tested prior to product release to assure adequate protection against the shipping and handling hazards anticipated in the domestic and international distribution network.

* REFERENCE CONDITIONS AND TOLERANCES

  Unless otherwise stated, the ambient conditions of the laboratory and tolerances for test conditions are:

Temperature	23 °C ± 5°C
Humidity	30% to 70% RH (not controlled)
Acceleration	+15%, -5% Peak
Velocity Change	+10%, -2%
Frequency	±0.5 Hz

Table C-1. Assumed ambient conditions and tolerances for test conditions.

* APPLICATION

  This specification shall apply to all Quantum products which are identified with the name "Quantum" and/or the Quantum logo applied to the product regardless of whether the product was fully or partially manufactured and packaged by Quantum or an outside supplier.

  NOTE: This test standard is a procedure to assure the maximum values of shock (Critical Acceleration) are NOT exceeded. Also, this standard details the vibration tests required to assure the packaged cushion resonances will NOT damage the Quantum F/G packaged product.

* EXCEPTIONS OR DEVIATIONS

Any exceptions or deviations from the product standards must be approved by the Engineering Product Manager, the Product Marketing Manager and Quality Assurance. Any deviation or exemptions must noted in the Product Plan. Quantum O.E.M. customer and O.E.M. supplier requirements must be reviewed by Quality Assurance prior to contractual finalization by Quantum to avoid both over-packaging and under-packaging of Quantum products.

* FINISHED GOODS PRODUCT TESTS

- Vibration
    a. resonance search / Dwell
    b. resonance endurance - SINE wave
    c. stacked resonance

- Shock: "Free Fall Drop"

* PRE-TEST AND POST-TEST INSPECTION AND FUNCTIONAL TEST

All specimens must be thoroughly functionally tested prior for submission of packaging testing and the characteristic data recorded for comparison with post test data. The product must be visually inspected prior to packaged testing.

After the shock and vibration tests are performed the specimen must be functionally tested to assure the unit is performing to specification. The specimens must be carefully inspected for structural, cosmetic and mechanical damage after shock and vibration tests.

The units under test shall be inspected and functionally tested between each segment of the shock and vibration tests series.

* PACKAGING ACCEPTANCE

If during any segment of the F/G packaged product test the product fails to meet the required functional specifications, or the product has incurred structural damage, or the unit has been cosmetically blemished (other than fixturing markings), the packaging shall be considered "FAILED".

Note: any intermittent problems should be considered "FAILED".

If packaging is considered "FAILED", the system should be rechecked to assure the system under test was not an unreliable sample and more samples must be tested to confirm either an acceptable or non-acceptable sample.

Before final acceptance, the system under test will be "burned-in" for 30 continuous days and retested to assure there are no latent failures introduced in the abuse testing.

* CARTON ORIENTATION

The cartons are identified by figure C-1.

* VIBRATION TESTS

- Resonance Search

  Resonance search within a range of 3-200-3 Hz. at a constant acceleration input of 0.5Gs must be performed on three axes of the packaged assembly. An X-Y Log-Log plot must be permanently recorded for each axis tested at each monitoring position. If the packaged unit can conceivable be shipped in a position other than the upright position, all three axes must undergo a resonance search.

- Resonance Dwell-SINE Wave

  Each potential shipping axis must be endurance tested for a total one hour, 15 minutes per resonant frequency at an input of 0.5Gs acceleration. If the requirement of a full one hour cannot be achieved, the balance of the hour must be performed with the vibration system continually sweeping from 3-200-3 Hz. 0.5Gs constant acceleration input.

- Pallet Stack, Resonance Endurance Test must be performed with the Finished Goods cartons stacked in the normal shipping orientation in a single column to the anticipated maximum height of a pallet load. For safety reasons, the proper fences (lateral support restraints) must be utilized.

  After each axis is endurance tested, inspect all products in the column stack for cosmetic and structural damage. Then perform a functional test on the unit checking for intermittent or permanent malfunction.

* RESONANCE SEARCH

The vibration system frequency adjusted for stacked resonance (maximum displacement of the top unit) at an input acceleration of 0.5Gs of the table.

* RESONANCE DWELL

The endurance test to run a total of 15 minutes at the stacked resonance frequency.

* SHOCK TEST: FREE FALL DROP TEST

The free fall drop test must be performed using a drop test mechanism which will provide accurate and repeatable drop heights. Also, the mechanism must be able to assure accurate and repeatable package orientation during impacts.

The acceleration levels must be monitored by the use of accelerometers and the resulting curves permanently recorded on photographs. The levels detected must not exceed the critical acceleration determined by the bare unit damage boundary tests.

* TEST SEQUENCE

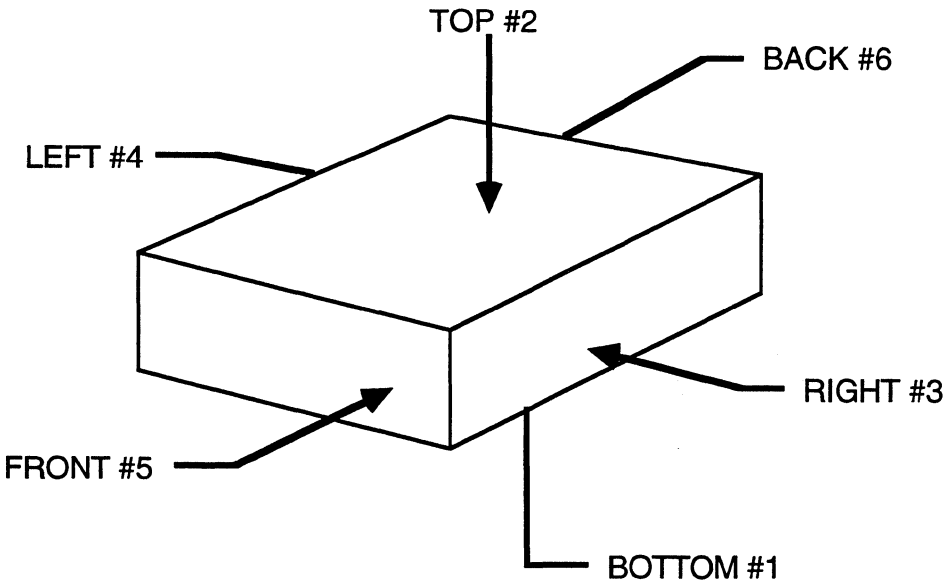

Figure C-1. Europa carton face identification.

The package product shall be shock tested by dropping the F/G package in the following sequence:

DROP #	IMPACT
1	bottom (1)
2	top (2)
3	right (3)
4	left (4)
5	front (5)
6	back(6)
7	edge (2-3)
8	edge (5-3)
9	edge (5-2)
10	corner (2-3-5)

Table C-2. Free fall drop testing sequence.

* DROP HEIGHTS

Gross Weight	Drop Height	No. of Drops
0 - 20 lbs.	30 inches	10
21 - 40 lbs.	24 inches	10
41 - 60 lbs.	18 inches	10
61 - 80 lbs.	12 inches	10
81 - 200 lbs.	6 inches	10
200 lbs. and above[1]	15/9 inches[2]	1/5

Table C-3. Drop heights required for F/G Quantum products

Notes to Table C-3:

1. If the F/G items are unitized (palletized), 10 impacts at 9 inches are required on the bottom orientation only.

2. First number is the base or bottom drop, second number is the drops on all other surfaces.

After drop testing the product, reinspect for structural and cosmetic damage. Also retest for intermittent and permanent functional malfunction. Subject the units run through the shock tests to a 30 day burn-in test before the final functional test is performed.

* COMPRESSION TEST

Floating platen compression test equipment shall be used in this test in accordance with ASTM D-642-76. The test shall be conducted on five (5) identical packages with all internal packaging components and an actual product or dummy load. The average of the five (5) tests shall be used to determine the acceptability of the container/package system.

Compressive forces are to be taken to the maximum required load or to failure. The maximum compressive rate is 0.5 inches per minute.

The minimum acceptable compressive resistance (load) will be based on the HIGHEST value calculated by using the following methods:

A. Four (4) times the greatest expected compressive load during transportation or storage.

B. Ten (10) times the weight of the product intended to be packaged.

C. 300 lbs. compression resistance.

* REFERENCE DOCUMENTS
National Safe Transit Association (N.S.T.A.) Test procedures Project 1A.1973

* A.S.T.M. DOCUMENTS

D-642-76	Compression Test for Shipping Containers
D-775-61(73)	Drop Test for Shipping Containers
D-880-79	Incline Impact Test For Shipping Containers
D-996-78	Packaging and Distribution Environments def. of terms
D-999-76	Vibration Testing of Shipping Containers
D-1083-53(79)	Testing Large Shipping Containers and Crates
D-3331-77	Assessment of Mechanical-Shock Fragility Using Package Cushioning Materials
D-3332-77	Mechanical-Shock Fragility of Products, Using Shock Machines
D-35680-80	Vibration (Vertical Sinusoidal Motion) Test of Products

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Appendix D Air Cleanliness (Class 100)

Classification of air cleanliness is based on particle count with maximum allowable number of specified minimum sized particles per unit volume and on statistical average particles size distribution.

DEFINITION OF CLASS 100[1]

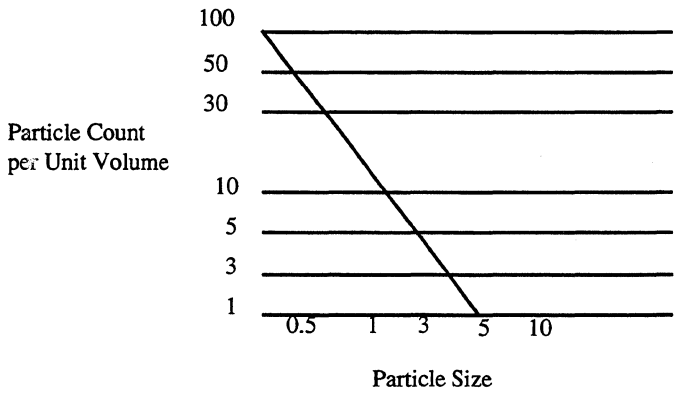
The particle count shall not exceed a total of 100 particles per cubic foot (3.5 particles per liter) of size 0.5 μm or larger.

The statistical average particle size distribution may deviate from this curve because of local or temporary conditions. Counts below 10 particles per cubic foot (0.35 particles per liter) are unreliable except when a larger number of samplings are taken.

TEST METHOD[2]

For particles in the 0.5 to 5.0 μm size range, equipment employing light scattering principles shall be used. The air in the controlled environment is sampled at a known flow rate. Particles contained in the sampled air are passed through an illuminated sensing zone in the optical chamber of the instrument. Light scattered by individual particles is received by a photodetector which converts the light pulses into electrical current pulses. An electronic system relates the pulse height to particle size and counts the pulses such that the number of particles in relation to particle size is registered or displayed.

The count of particles of a given size shall not exceed value shown in the graph below.



1. U.S.A. Federal Standard 209B, available from the General Services Administration; Specifications Activity; Printed Materials Supply Division; Building 197; Naval Weapons Plant; Washington D.C. 20407, U.S.A.

2. American Society for Testing and Materials; Standard ASTM F 50; 1916 Race Street; Philadelphia, Pennsylvania 19103, U.S.A. Society for Testing and Materials; Standard ASTM F

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Appendix E Humidity Charts

These charts are given as reference for any who care to gain a greater understanding of the humidity specifications given in the Environment section. Except for references to specific figure numbers, the explanation is quoted directly from that monster of a book that Don Westwood owns, Marks' Standard Handbook for Mechanical Engineers, McGraw-Hill Book Co., Eighth Edition, New York, © 1978. It's probably a copyright violation, but who's checking?

Psychrometric charts are usually plotted, as indicated by the example Figure D-1, with dry-bulb temperature as abscissa and specific humidity as ordinate. Since the specific humidity is determined by the vapor pressure and the barometric pressure (which is constant for a given chart), and is nearly proportional to the vapor pressure, a second ordinate scale, departing slightly from uniform graduations, will give the vapor pressure. The saturation curve (relative humidity = 100%) gives the specific humidity and vapor pressure for a mixture of air and saturated vapor. Similar curves below it give results for various values of relative humidity. Inclined lines of one set carry fixed values of the wet-bulb temperature, and those of another set carry fixed values of v_a, cubic feet per pound of air. Many charts carry additional scales of enthalpy or Σ function.

Any two values will locate the point representing the state of the atmosphere, and the desired values can be read directly. Figures D-2 and D-3 are psychrometric charts from the General Electric Company and Ellenwood and Mackey, "Thermodynamic Charts," covering a dry-bulb temperature range from 32 to 300°F. They are accurate only for a barometric pressure of 29.92 in Hg.

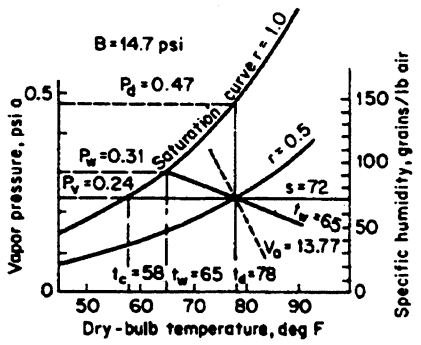

Figure E-1 Skeleton humidity chart

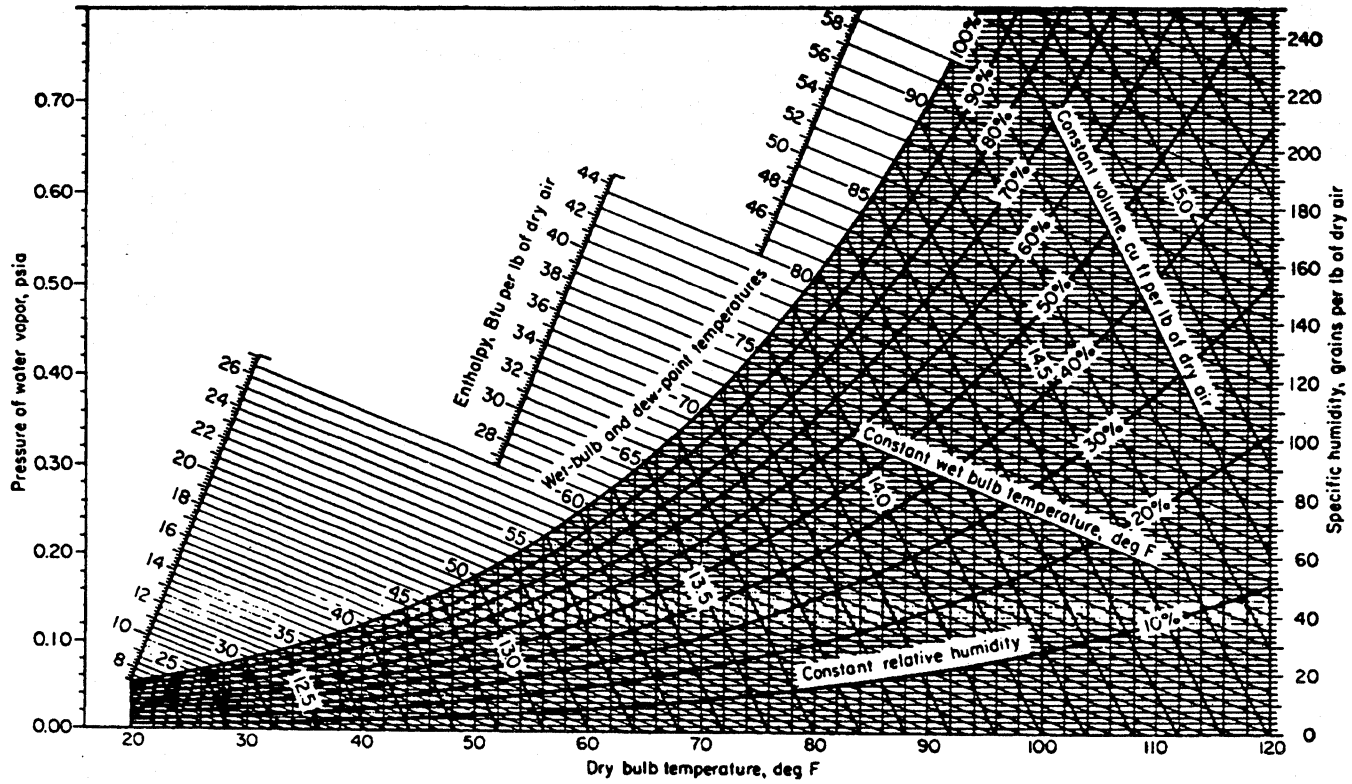

Figure E-2 Humidity chart for low temperatures.
Barometric pressure 14.969 psia
(Copyright by General Electric Co.)

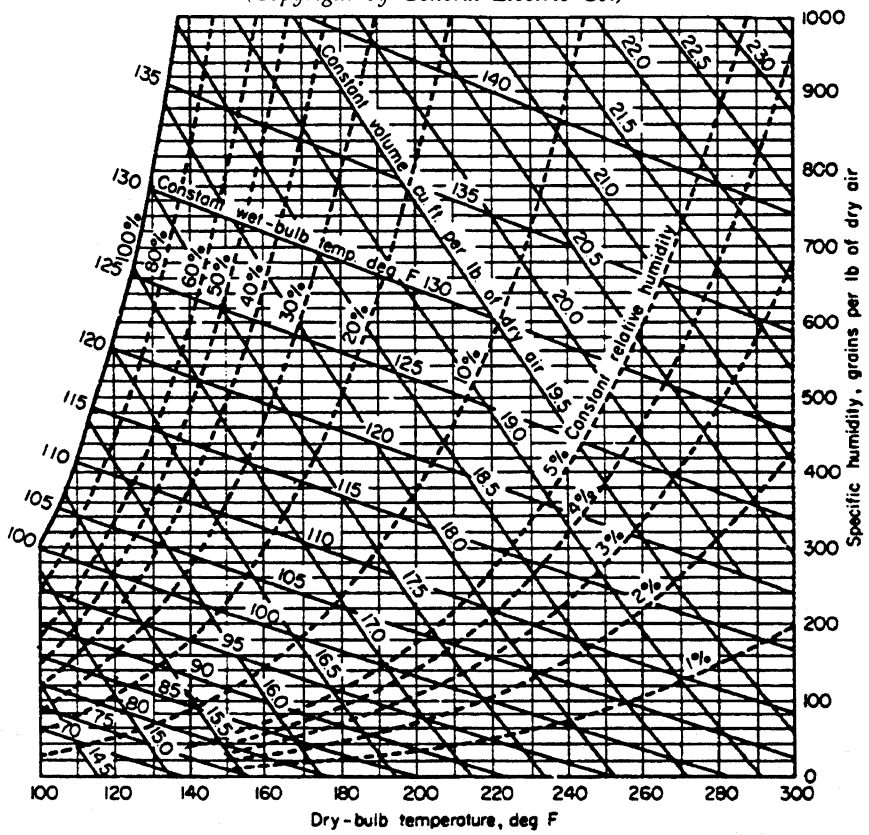

Figure E-3 Humidity chart for medium temperatures
(From Ellenwood and Mackey, "Vapor Charts," Wiley.)