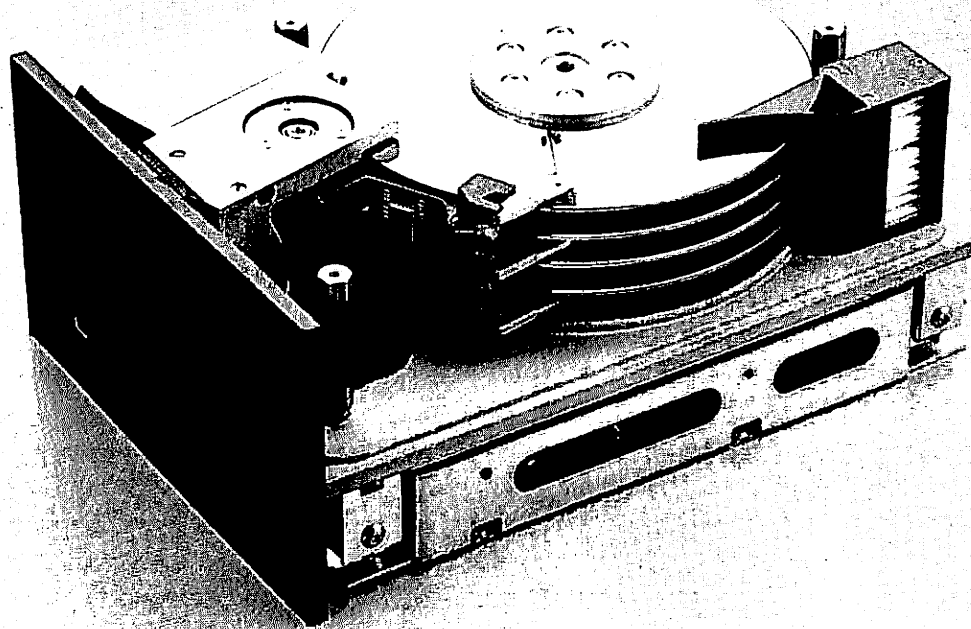




**OEM
Service Manual**

V100 Series
5.25 Inch Winchester
Disk Drives



OEM Service Manual

V100 Series
5.25 Inch Winchester
Disk Drives

SHEET REVISION TABLE															
P/N 308100 Revision Ltr A EC 10299															
SHT	i	ii	iii	iv	v	vi	vii	viii	ix	1	2	3	4	5	6
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHT	97	98	99	100											
REV LTR	A	A	A	A											

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1 INTRODUCTION

1.1 General Description

The Priam V100 Family of Disk Drives is a series of random access storage devices using 2, 3, or 4 nonremovable 5¼ inch disks. Each disk surface employs one movable head to service up to 1166 tracks. Total unformatted capacities of four models are 30.8 (V130), 51.4 (V150), 72.0 (V170), and 85.0 (V185) megabytes.

Fast access time and high track density are achieved through the use of a rotary voice coil head positioner in conjunction with a dedicated servo surface.

The inherent simplicity of mechanical construction allows maintenance free operation throughout the life of the drive. Both electronic boards are mounted outside the sealed head disk assembly, allowing field serviceability.

Mechanical and contamination protection for the heads, actuator and disks is provided by an impact resistant metal cover. A self contained re-circulating system supplies clean air through a 0.3 micron filter. A separate filter allows for ambient pressure equalization without introduction of contaminants. Adequate air flow and uniform temperature distribution throughout the head and disk area are assured.

The track following servo system allows the heads to continuously follow the recorded track, and reduces off track due to non-repetitive spindle run-out, vibration, and environmental temperature changes: Read and write operations can be performed after power up with no thermal stabilization delay.

Superior data integrity results from the use of shock isolators, carbon overcoated metal film media, a head landing/shipping zone, and automatic actuator lock.

The electrical/physical interface is compatible with other available ST412/506 interfaced products, and includes the same data transfer rate, connectors, DC power, mechanical mounting holes and package size.

Customer options include:

1. Radial operation—Outputs active without drive selected.
2. Power On sequencing for multiple drive applications.
3. Non-Multiplexed Index.
4. Write Protect.
5. Radial Seek Complete.

1.2 Specification Summary

1.2.1 Physical Specifications

Power requirements

12 VDC \pm 10%.

Maximum Ripple 120 mV P-P @ 10.92 VDC Minimum.

Peak Current 4.5 Amp-Motor Start For 10 Seconds.

Running Current 2.0 Amp avg. (Track Following).

Peak Running Current 2.8 Amp (Seeking).

Maximum Power Dissipation 54 Watts Peak for 10 Seconds during motor start.

Average Power Dissipation 27 Watts (12 Volts).

5 VDC \pm 5%

Maximum Ripple 120 mV P-P @ 4.88 VDC Minimum.

1.5 Amp avg./max.

Average Power Dissipation 7.5 Watts (5 Volts).

Dimensions and Weight

Height*	3.25 in (8.26 cm)
Width*	5.75 in (14.61 cm)
Depth*	8.00 in (20.32 cm)
Weight	6 lb (2.72 kg)

* Does not include Faceplate

Environmental Limits

Ambient Temperature

Operating 4°C to 50°C (40°F to 122°F)

Nonoperating -40°C to 60°C (-40°F to 140°F)

Gradient Less than 10°C (18°F)/hour

Relative Humidity

Operating	8% to 80% (noncondensing)
Operating	Maximum Wet Bulb 85°F
Nonoperating	5% to 95% (noncondensing)
Nonoperating	Maximum Wet Bulb 85°F

Shock and Vibration

Operating	2G max, 11 ms. Half Sine Wave .010" dA, 2-22 Hz; .25G, 22-600Hz
Nonoperating	20G max, 11 ms. Half Sine Wave .040" dA, 2-22 Hz; 1.0G, 22-600Hz
Transport	25G's into HDA, 42" Packaged Drop.

Altitude

Operating	-305 m (-1000 ft) to +3,000 m (+10,000 ft)
Nonoperating	-305 m (-1000 ft) to +12,000 m (+40,000 ft)

Acoustical Noise 50 dBa, one meter from cover

1.2.2 Functional Specifications

Storage capacity

	V130	V150	V170	V185
Unformatted*	30.8MB	51.4MB	72.0MB	85.0MB
Formatted (typical sector formats)				
(32 × 256 bytes)	24.3MB	40.4MB	56.6MB	66.9MB
(17 × 512 bytes)	25.8MB	43.0MB	60.1MB	71.0MB
Data tracks	2961	4935	6909	8162
Data Cylinders	987	987	987	1166
Disks	2	3	4	4
Data Surfaces	3	5	7	7
Heads, Read/Write	3	5	7	7
Head, Servo	1	1	1	1
Bytes per Track				
Unformatted		10,416		
Formatted (typical sector formats)				
32 × 256 byte sectors		8,192		
17 × 512 byte sectors		8,704		
Maximum Bit Density (bits/inch)	9,897	9,897	9,897	10,526
Maximum Flux Density (flux reversals/inch)	9,897	9,897	9,897	10,526
Track Density (tracks/inch)	960	960	960	1,047
Access time (including settling and transmission of step pulses)				
Track-to-track: 5 milliseconds Maximum				
Average: 30 milliseconds ± 10%				
Maximum: 60 milliseconds				
Maximum Average Latency Time: 8.33 milliseconds				

Rotational Speed: 3600 rotations/minute \pm 0.1%
 Data Transfer Rate: 5 megabits/second (625 kilobytes/second)
 *Recording Code: Modified Frequency Modulation (MFM)
 Interface: ST412/506 Compatible
 Start Time: Less than 25 seconds
 Stop Time: Less than 25 seconds

*NOTE: All models support the use of 2.7 RLL encoding in addition to MFM. When used with a controller utilizing RLL encoding, drive capacity may be expected to increase up to 50% over the values stated above. Note that error rate criteria may vary depending upon the type of RLL encoding scheme used.

1.2.3 Reliability Specifications

Mean-time-between-failures (MTBF)	More than 20,000 power on hours
Mean-time-to-repair (MTTR)	less than 30 minutes
Component life	5 years
Error rate	
Recoverable Errors	1 per 10 ¹⁰ bits read
Unrecoverable Errors	1 per 10 ¹² bits read
Seek Errors	1 per 10 ⁶ seeks

1.2.4 Disk Defects

Disk defects are imperfections in the media surface. No unit will be shipped if surface analysis identifies more than 30, 50, 70, or 85 total defective tracks/drive for the V130, V150, V170, and V185 respectively. Note that even at these maximum values, only 1% of the drive capacity is unavailable. **Additionally, no defects will be present on cylinder 0, heads 0, 1, and 2.**

Testing for defects involves an analysis of the total media surface under marginalized test conditions. Defect information is included on the test data sheet shipped with the drive, and on the error map label affixed to the drive. Format is cylinder number, head number and bytes from index. Location accuracy is \pm 10 bytes.

In a single format operation, it is probable that errors will not be detected on all of the locations defined. However, all should be considered defects and flagged by the using system to ensure long term data reliability.

The use of an error correction code (ECC) rather than cyclic redundancy check (CRC) is recommended for best data integrity.

2 FUNCTIONAL CHARACTERISTICS/OVERVIEW

2.1 General Operation

The V100 Series drives consist of read/write, head positioning and control electronics, rotary voice coil actuator, media, air filtration system, and disk spin motor.

These components perform the following functions:

1. Interpret and generate control signals.
2. Position and maintain the heads over the desired track.
3. Maintain precise disk rotation speed.
4. Read and write data.
5. Provide a contamination-free environment.

2.2 Read/Write, Servo and Control Electronics

Electronics are packaged on two printed circuit boards. The outermost board, to which control and data signals are connected, includes:

1. R/W circuits.
2. Interface drivers and receivers.
3. Microprocessor and associated logic.
4. Write fault detection.
5. Drive selection.
6. Optional interface functions.
7. Index circuit.

The second PCB, mounted under the top board, accepts the required DC voltages and performs the following functions:

1. Disk spin motor control.
2. Head actuator positioning.
3. Track 0 detection.
4. -10 voltage regulator.
5. Power monitoring.

2.3 Drive Mechanism

A brushless 3 phase DC drive motor rotates the spindle disk assembly at 3600 rpm. The spindle is driven directly with no belt or pulley being used. A crystal controlled phase lock loop maintains precise speed regulation. The motor and spindle are dynamically balanced to ensure a low vibration level. Dynamic braking is used to quickly stop the motor when power is removed. The base plate assembly is shock mounted to the side mounting frames to minimize transmission of vibration through the chassis or frame. Index signal is derived from a transducer inside the drive motor.

2.4 Air Filtration System (Figure 2-1)

The disks, read/write heads and actuator are fully enclosed in a module using an integral recirculation air system and absolute filter to maintain a clean environment. A separate filter permits ambient pressure equalization without entry of contaminants.

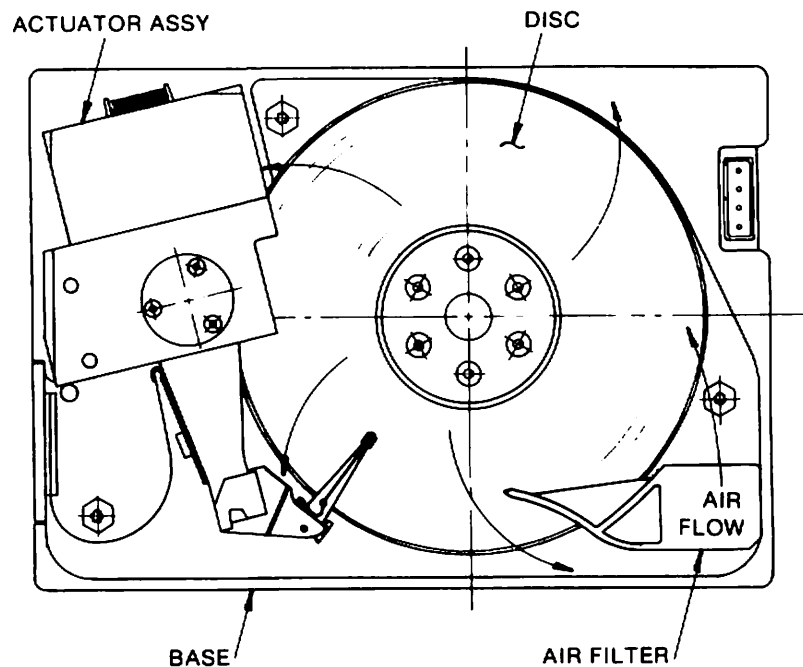


Figure 2-1
Air Filtration System

2.5 Positioning Mechanism (Figure 2-2)

The read/write heads and servo head are mounted onto a rotary actuator supported by precision ball bearings. A bobbin-type voice coil mounted between two permanent magnets provides the driving force required to rotate the actuator for head positioning. Crash stops are provided to protect the head assemblies should a malfunction cause the actuator to lose control. When the drive is powered down, the actuator is driven to a head landing zone on the inner diameter of the disk. Simultaneously, the actuator is automatically locked over the landing zone to prevent possible head/media damage when the drive is subjected to transport shock or movement around the office.

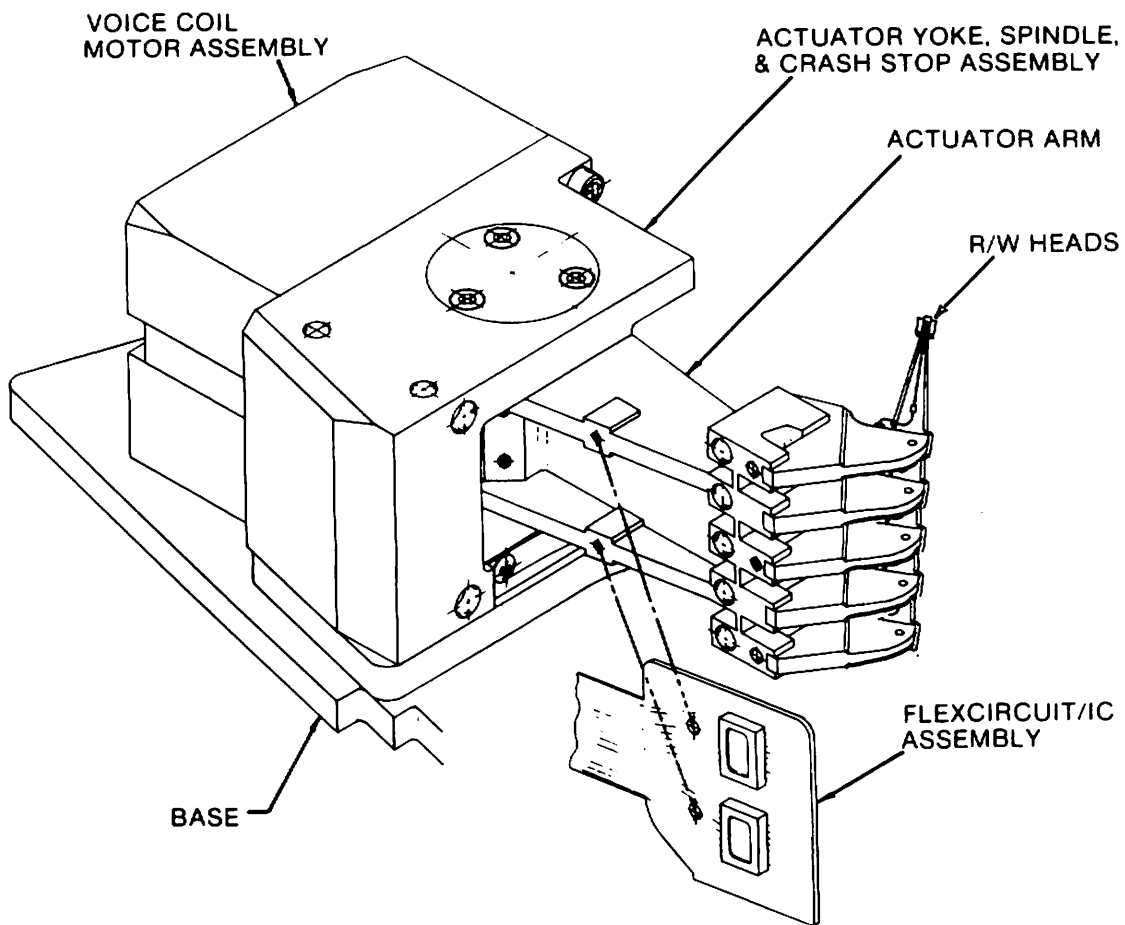


Figure 2-2
Read/Write Head Positioning Mechanism

2.6 Read/Write Heads and Disks

Winchester technology heads and media are used in the V100 Series disk drives. Maximum recording density is 10,526 flux changes per inch. The heads are connected to the external electronics via a flat flexible printed circuit cable. Three integrated circuits are mounted on the cable adjacent to the heads. The circuits provide write current, head selection, and read signal amplification. Amplification of the low level read signal prior to its leaving the sealed unit provides superior signal-to-noise ratio and less sensitivity to noise in the ground system and mounting frame.

2.7 Servo System

Actuator positioning and head track following is accomplished on a closed loop basis using a dedicated servo surface. During seek operations, track crossing information is used to optimize actuator deceleration. A "dual frequency" technique is used. This technique is based on amplitude differences between alternating servo tracks written at two different frequencies. On-track for a data head is realized when the servo head is positioned exactly between the two servo tracks. Essentially, the servo head continuously samples the two frequencies, sums and averages the signals, then positions the head at the point where this averaged signal is strongest—exactly between the two tracks. The resultant error signal is linearly proportional to the error (off-track) size, and indicates the off-track direction.

The dual-frequency servo offers several advantages relative to classical di-bit and tri-bit methods:

1. It is relatively insensitive to servo surface media defects. The di-bit/tri-bit methods generally require an "error-free" servo surface. This reduces manufacturing yields (particularly for high track density media) and increases the cost of the servo disk. Since the dual-frequency servo continuously samples f_A and f_B amplitudes, media defects are averaged out and not sensed by the servo.
2. Because the dual-frequency method uses a relative amplitude difference of f_A and f_B frequency, servo head azimuth alignment is not critical. This alignment is critical in di-bit and tri-bit methods, however, again raising production costs and increasing service requirements.
3. Since f_A and f_B frequencies are recorded well below data frequencies, write data noise is easily filtered out in the event it is injected into the servo read channel via read/write head to servo head cross talk.

Track 0 is derived from the servo surface information, eliminating the need for a separate sensor for this purpose.

3 FUNCTIONAL OPERATIONS

3.1 Power Sequencing (Figure 3-1)

Plus 5 and +12 volts may be applied in any order; however, both voltages must be applied to start the spindle drive motor. A speed sense circuit ensures the spindle is up to speed before recalibrating the heads to track 0. TRACK 0, SEEK COMPLETE and READY signals on the interface will become true sequentially. The drive will not perform read, write or seek functions until READY becomes true. No commands should be attempted until READY is true. STEP pulses will be ignored, and WRITE GATE will cause a WRITE FAULT.

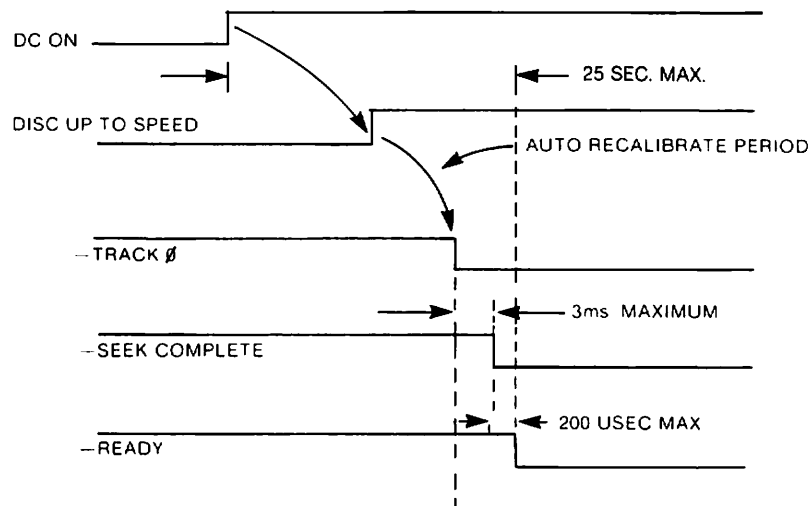


Figure 3-1
Power Up Sequence

3.2 Drive Selection

Drive selection occurs when one of the DRIVE SELECT lines is activated. Only the selected drive will respond to the input signals, and only that drive's output signals are then gated to the controller interface (see Section 5.6.1 for exception).

3.3 Track Accessing

Read/write head positioning is accomplished by:

- A) Deactivating WRITE GATE.
- B) Activating the appropriate DRIVE SELECT line.
- C) Being in the READY condition with SEEK COMPLETE true.
- D) Selecting the appropriate DIRECTION IN state.
- E) Pulsing the STEP line.

Each step pulse will cause the heads to move either 1 track in or 1 track out, depending on the level of the DIRECTION line. A low level on the DIRECTION line will cause a seek inward toward the spindle; a high, outward toward track 0.

3.4 Head Selection

Any of the heads can be selected by placing the head's binary address on the three (3) HEAD SELECT lines:

DRIVE	NUMBER OF DATA HEADS	HEAD ADDRESSES
V130	3	0, 1, 2
V150	5	0, 1, 2, 3, 4
V170	7	0, 1, 2, 3, 4, 5, 6
V185	7	0, 1, 2, 3, 4, 5, 6

3.5 Read Operation

Reading data is from the disk and is accomplished by:

- A) Deactivating the WRITE GATE line.
- B) Activating the appropriate DRIVE SELECT line.
- C) Assuring the drive is READY.
- D) Selecting the appropriate HEAD SELECT levels.

3.6 Write Operations

Writing data onto the disk is accomplished by:

- A) Activating the DRIVE SELECT line.
- B) Assuring the drive is READY and SEEK COMPLETE is true.
- C) Selecting the proper HEAD SELECT levels.
- D) Ensuring no WRITE FAULT conditions exist.
- E) Activating WRITE GATE and placing data on the WRITE DATA line.

3.7 System Integration Considerations

The drive is designed with sufficient margin to allow meeting specified error rates under all DC supply voltage variations and environmental conditions listed under specifications. External factors affecting error rates are the data separator in the controller and system/ground noise levels. These items subtract from the overall margin of the drive as shipped.

Examples of system/ground noise influences are:

- Radiated and conducted noise from switching power supplies.
- Proximity of drive to noise sources such as CRTs.
- Circulating ground currents and ground loops in the system cabling and ground connections.

Examples in the data separator are:

- Nominal data bit centering in the separator data window with a data pattern which exhibits no superposition bit shift.
- Phase lock loop frequency and phase response.

4 THEORY OF OPERATION

4.1 Overview

The V100 Series disk drive consists of a sealed head-disk assembly (HDA) containing a rotary voice-coil head positioning mechanism (actuator), media, read/write heads, a servo head, a spindle motor, and air filtration components. Also included in drive assembly, external to the HDA, are two printed circuit boards that perform read/write, servo, and interface control electronics.

Interpretation and generation of control signals are performed by a microprocessor and a programmable logic array (PLA). Positioning of the heads is achieved by driving the actuator with a dedicated track following servo system. Speed control of the spindle motor is performed by a phase-controlled driver circuit using a 360-Hz reference signal. Encoded data is written to and read from the disks by means of a read/write data channel. Write errors are reported by read preamplifier/write driver ICs in the read/write data channel. Contamination protection for the heads, actuator, and media is achieved by enclosing these components in a sealed head-disk assembly having a built-in air filter.

The following paragraphs provide a more detailed description of the disk drive components and electronic circuits, as shown in the disk drive functional block diagrams (Figures 8-1 and 9-1).

4.2 Head-Disk Assembly

Details of the components contained in the sealed head-disk assembly are provided in the following paragraphs.

4.2.1 Actuator

The read/write heads and servo head are mounted on a rotary arm supported by precision ball bearings. A bobbin-type voice coil is attached to the rotary arm and mounted between two permanent magnets. These components comprise a rotary voice-coil head positioning mechanism (actuator). This mechanism provides the driving force required to move the rotary arm for head positioning. The magnetic field in the gap between the magnets allows the acceleration of the rotary arm to be controlled by the voice-coil current. Drive current for the voice coil is supplied by the actuator servo control circuit. Crash stops are provided to protect the heads should a malfunction cause the actuator servo control circuit to lose control. When the disk drive is powered down, the rotary arm is driven to a non-data area head landing zone at the inner diameter of the disk. Simultaneously, the arm is automatically locked over the landing zone to prevent possible head/media damage if the disk drive is inadvertently subjected to excessive shock during relocation or shipment. Drive current for the actuator lock solenoid is supplied by an actuator lock driver circuit.

4.2.2 Recording Media

The recording media consists of a carbon overcoated thin film metal magnetic coating on either side of a 130-millimeter (5.12 inch) diameter aluminum substrate. In the V100 Series, there are several such disks in the sealed head-disk assembly, with up to seven surfaces used for data and one surface used for prerecorded servo information.

4.2.3 Read/Write Heads

The disk drive employs Winchester technology read/write heads, one for each data surface. The heads are designed to fly above the disks supported by a thin cushion of air, which acts as an air bearing to the heads. The flying height is approximately 16 microinches at the inner diameter of the disk. When the disk drive is powered down, the actuator moves the heads to a "landing zone" at the inner diameter of the disks where the heads come to rest on the surface.

Each head consists of a gapped ferrite core mounted in a ferrite slider. There are two windings wound around the ferrite core and the windings are connected at a common point and phased such that the common point acts as a center tap. These windings are used for both reading and writing by detecting or producing a magnetic field at the tap in the ferrite core.

In a write operation, data is written by passing a current through the windings of the selected head. This current generates a flux field across the gap and aligns the magnetic particles contained in the surface of the disk. The writing process orients the poles of each magnetized particle to permanently store the direction of the flux field as the particles pass beneath the head. The direction of the flux field is a function of the write current direction. Erasing is accomplished by writing over any data which may have been previously recorded on the disk.

In the read operation, as the data surface passes beneath a head, the magnetically stored flux fields intersect the gap in the ferrite core. Gap motion through the flux field causes a voltage to be induced into the windings wound around the core. This induced voltage is analyzed by the read circuitry to define the data recorded on the surface of the disk. Each flux reversal, caused by a write current polarity change, generates a readback voltage pulse.

There are two read preamplifier/write driver ICs mounted on the rotary arm of the actuator, adjacent to the heads. Each IC provides write current, head selection, and read signal amplification for four read/write heads. The ICs are connected to the read/write data channel electronics external to the sealed head-disk assembly via a flexible printed-circuit cable.

4.2.4 Read Preamplifier/Write Driver IC

The read preamplifier/write driver IC is a standard integrated circuit designed for disk drive read/write head control. The IC can select 1 of 4 heads, read from or write to the selected head, and supply a write fault signal. One IC is used in the V130 and there two ICs in all other V100 Series Drives. Control signals for the ICs are supplied by the head select and control logic block.

The IC is enabled by Chip Enable signal CE-L. Binary Head Select signals HS1-H, HS2-H are decoded by the IC to select the desired head. Reading and writing is controlled by Write Select signal WS. When WS is high, the write mode is selected, and when WS is low, the read mode is selected.

When the IC is in the write mode, differential current applied across the DX, DY lines is used to switch the current drawn from the write current source to the head of the selected channel. Head voltage swings, generated by the switching of write current through the inductive head, are monitored by a head transition detect circuit in the IC. Absence of proper head voltage swings indicates an open or short in either half of the head winding or an absence of write current. This will cause a current to flow into the Unsafe (US) output line. This line is connected to the fault detector which will pass a write fault message to the PLA.

When the IC is in the read mode, data is read from the selected head, amplified, and output on the differential DX, DY lines to the read chain amplifier and signal conditioner. If a fault condition exists such that write current is applied to the IC when it is in the read mode, the write current will be drawn from the Unsafe line and the fault will be detected by the fault detector.

4.2.5 Servo Head

The servo head is a read-only head constructed similarly to the read/write heads. The output of the head is amplified by a servo preamplifier IC mounted on the rotary arm of the actuator.

4.2.6 Servo Preamplifier IC

The servo preamplifier IC is a two-stage differential amplifier designed for use as a preamplifier for a magnetic servo head. The preamplifier output, labeled SERVO+, SERVO-, is connected to the input of the actuator servo control demodulator via the flexible printed-circuit cable used to connect the read preamplifier/write driver ICs to the read/write data channel.

4.2.7 Spindle Motor

The spindle motor is a 3-phase brushless DC motor which spins the disks at a speed of 3600 rpm. Incorporated in the motor are three Hall-effect sensors which are used by the spindle speed control circuit to indicate which of the three phases should be driven. An optical sensor in the motor provides an Index signal, INDX-L.

4.2.8 Air Filtration Components

A self-contained recirculating filter supplies clean air through a 0.3 micron filter to the sealed head-disk assembly. A separate filter allows for ambient pressure equalization within the sealed head-disk assembly without the induction of contaminants.

4.3 Servo PCB

Functions performed by the servo PCB are described in the following paragraphs.

4.3.1 Actuator Lock Driver

The actuator lock is controlled by a solenoid which is energized at power on after the microprocessor detects that the spindle motor is up to speed (At Speed signal true). At this time, the microprocessor activates its Pick line which in turn causes the actuator lock driver to energize the lock solenoid. The actuator arm is now released, allowing the heads to move over the disks.

4.3.2 Clock Generator

The clock generator consists of a crystal oscillator and a number of count-down registers. The clock generator has five outputs—9.216 MHz for the microprocessor, 1152 kHz and 576 kHz for the demodulator in the actuator servo control circuit, 92.1 kHz for the spindle speed checker circuit, and 360 Hz for the spindle speed control circuit.

4.3.3 Spindle Speed Control

The three Hall-effect sensor outputs from the spindle motor are input to a ROM commutator in a solid-state spindle speed control circuit which decides which of the three outputs from the circuit should be driven to spin the motor in the proper direction. The speed of the motor is controlled by a phase-lock frequency regulator which compares a 360-Hz signal from the clock generator with the signals from the three Hall-effect sensors. This regulator circuit provides feedback to drivers in the speed control circuit such that the speed of the motor is maintained at 3600 rpm, plus or minus 3.6 rpm.

At power on, after the Power On Reset signal is turned off, the microprocessor sets the Stop Motor signal false, causing the spindle motor brake to pick. At the same time, the microprocessor disables the spindle speed control circuit by deactivating the Normal Regulation line. This allows the spindle motor to accelerate without any speed regulation. The microprocessor monitors the motor speed by measuring the time interval between Index pulses. When the time interval between the pulses indicates that the speed is within one percent of 3600 rpm, the microprocessor enables the speed control circuit by activating the Normal Regulation line. The microprocessor stops the spindle motor by application of Stop Motor to the spindle speed control and relay driver circuits.

4.3.4 Spindle Speed Checker

The spindle speed checker circuit monitors the speed of the spindle motor by measuring the time between Index pulses from the spindle motor Hall-effect sensor compared with a 92.1-kHz reference signal from the clock generator. The microprocessor monitors the At Speed and Counter Not Ready outputs from the speed checker circuit and shuts down operation of the disk drive if the speed is determined to be outside of a predetermined range.

4.3.5 Spindle Motor Brake Relay and Relay Driver

The spindle speed control circuit includes a dynamic brake which brings the spindle motor to a rapid halt when the microprocessor issues a Stop Motor signal. Stop Motor activates the relay driver which in turn causes the spindle motor brake relay to connect low-value resistors across the winding of the spindle motor. At the same time, Stop Motor input to the speed control circuit disables the 3-phase drive to the motor.

4.3.6 Actuator Servo Control

Actuator positioning and head track following is achieved on a closed loop basis using a dedicated servo surface. The servo system employs a dual frequency technique based on an amplitude difference between alternating servo tracks written at two different frequencies. On track is realized for a data head when the servo head is positioned exactly between two servo tracks. In operation, a

demodulator circuit continuously samples the two frequencies from the servo head, sums and averages the two signals, and produces a position error signal (PES). This PES signal is linearly proportional to the error (off track) amount and also indicates the off track direction.

During track following, the PES voltage is input to a transconductance amplifier which supplies drive current to the actuator voice coil. This causes the actuator to hold the servo head at a point where the PES voltage is zero—exactly between the two servo tracks. Since the servo head and the read/write heads are fixed on the rigid rotary arm of the actuator, any movement of the servo head is translated to all of the read/write heads.

The position error signal is also used during a seek operation. As the rotary arm is moving across the disks during a seek, the PES voltage develops track crossing pulses which are counted by the microprocessor to determine track location. Also, the slope of the PES voltage is used to determine the velocity of the rotary arm during the seek operation.

The dual frequency technique described above is relatively insensitive to servo surface media defects. Also, servo head azimuth alignment is not a critical factor in the operation of the system.

The actuator servo control circuitry includes a demodulator, mode select switch, tachometer, digital-to-analog converter (DAC), and amplifier. Details of these circuits are provided in the following paragraphs.

4.3.7 Demodulator

The Servo+, Servo- signal (read from the servo surface via the servo head and the servo preamplifier IC) consists of a combination of the frequencies recorded on alternate servo tracks—700 kHz and 1020 kHz. This signal is amplified and then separated into two frequencies by two identical mixer channels in the demodulator. In one channel, the 700 kHz is mixed with 576 kHz from the clock generator to produce 124 kHz. In the other channel, the 1020 kHz is mixed with 1152 kHz from the clock generator to produce 132 kHz. Higher frequencies are attenuated with active low-pass filters in the mixer channels. The two outputs from the mixer channels are rectified, averaged, and fed to the input of a difference amplifier. The output of this amplifier is Position Error Signal (PES). When the servo head is positioned exactly between two servo tracks (read/write head on track), PES is zero. Displacement from this position (read/write head off track) causes PES to go either positive or negative, depending on the direction of offset and with an amplitude equal to the amount of the offset.

The rectified and averaged outputs from the two mixer channels are also fed to a summing and AGC amplifier which supplies an AGC voltage to the amplifier at the input of the demodulator.

The demodulator also contains a track zero detector. This circuit senses the presence of a third frequency (1100 kHz) recorded on the servo surface to identify track zero. The Track 0 output from the detector is coupled to the microprocessor and the Track Zero signal TRK0-L on the ST412/506 Interface.

4.3.8 Mode Select Switch

The mode select switch is a solid-state circuit which places the actuator servo control circuitry in either a seek (velocity) or track follow mode of operation. Operation of the switch is controlled by the Seek signal from the microprocessor.

4.3.9 Seek Mode

The seek mode of operation is selected by the microprocessor when it switches the mode select switch to the seek position with the Seek line. This selects a number of circuit blocks which together comprise a negative feedback servo control system supplying drive current to the actuator voice coil. These circuits include a velocity digital-to-analog converter (DAC), tachometer, slope selector, current inverter, on-peak detector, inverter, and power amplifier.

4.3.10 Velocity DAC

The velocity DAC is a standard integrated-circuit digital-to-analog converter which outputs a velocity DC voltage to the servo system in response to an 8-bit velocity command from the microprocessor.

4.3.11 Tachometer

The tachometer provides a measurement of the actuator velocity by differentiating the slope of the PES signal as the actuator crosses tracks. However, the PES voltage becomes non-linear at the peaks of its triangle-shaped waveform. Therefore, at this time the power amplifier current to the actuator voice coil is integrated to provide an indication of actuator velocity.

4.3.12 Slope Selector

The slope selector circuit, programmed by the Even In signal from the microprocessor, selects a PES slope of the proper polarity for the tachometer to provide a negative feedback.

4.3.13 Current Inverter

The current inverter, with a gain of plus or minus one and programmed with the Odd In signal from the microprocessor, selects a current of the proper polarity from the power amplifier for input to the tachometer.

4.3.14 On-Peak Detector

The on-peak detector operates at approximately 3.5 volts to initiate the switch between the differentiated PES signal and the integrated motor current in the tachometer. The output of the On-Peak detector is also coupled to the microprocessor to signal track crossings.

4.3.15 Power Amplifier

The power amplifier is a transconductance amplifier which supplies current to the actuator voice coil in response to an error voltage input. The amplifier output lines are labeled VCMA, VCMB. The amplifier is enabled by the Servo Enable line from the microprocessor.

4.3.16 Inverter

The inverter has a gain of plus or minus one and is programmed with signal Odd In from the microprocessor. The purpose of the inverter is to select an error voltage of the correct polarity for input to the power amplifier. The input to the inverter is from the tachometer (seek mode) or signal PES (track follow) as selected by the mode-select switch.

4.3.17 Track Follow Mode

The track follow mode of operation is selected by the microprocessor at the end of a seek operation when the addressed track has been reached. Signal PES is applied via the track follow position of the mode select switch through the inverter to the input of the power amplifier. Signal Odd In from the microprocessor programs the inverter to select a PES voltage of the proper polarity to provide a negative feedback signal to the amplifier.

4.3.18 Off-Track Detector

The off-track detector monitors the amplitude of the PES signal and provides an Off Track output to the microprocessor whenever the PES voltage exceeds plus or minus 1.5 volts.

4.3.19 Seek Operation

The disk drive must have Ready RDY-L and Seek Complete SKCMP-L true before a seek operation can begin. With the disk drive in this state, the microprocessor is in its basic loop, monitoring Motor Speed, Off Track, and looking for either a Step STEP-L pulse or Write Gate WGATE-L, both of which are gated by Drive Select DS0-L. When a Step pulse is received, the Step signal forces Seek Complete SKCMP-L false. If Write Gate is true and Seek Complete goes false, a fault condition will

be issued, automatically deactivating the write circuitry. When a Step pulse is received and Write Gate is not true, then the microprocessor will initiate a seek operation. The microprocessor will set the direction of the seek from the information on the Direction DIR-L line. The microprocessor will also set the seek mode, at which time the actuator servo control circuit will cause the actuator to move. The speed at which the actuator moves is dependent on the rate at which the Step pulses are received. Maximum performance of the actuator is attained if the time interval between Step pulses is less than 39 microseconds.

The microprocessor counts the track crossings until there are no more step pulses and the actuator is crossing the last track. At this time, the microprocessor switches the actuator servo control from the seek mode to the track follow mode. The microprocessor now starts a settling timer and looks for an off-track condition. If an off-track condition exists, the microprocessor restarts the settling timer. This is done until the off-track condition is cleared plus settling time. Once this is accomplished, the microprocessor sets the Seek Complete SKCMP-L line.

4.3.20 Restore to Track 0 Operation

To perform a restore to track 0 operation, the microprocessor enables the actuator servo control circuit and moves the actuator over the data area and out of the landing zone into the outer guard band area. Once the microprocessor detects that the actuator is in the outer guard band area, the microprocessor will cause the actuator servo control circuit to settle the actuator on a data track. The microprocessor will set direction out with a slow velocity, and count the track crossings until the track zero signal is detected. The microprocessor will now cause the servo control circuit to lock onto a track and check for the track 0 signal. After the servo control circuit is locked onto track 0, the microprocessor will initialize its maximum and minimum track counter. When this is accomplished, the microprocessor will activate Drive Ready signal DRV and Seek Complete signal SKCMP-L.

4.3.21 Power On Reset (POR)

The power on reset circuit monitors the +5V, +12V, and -10V voltages in the disk drive. (The +5 and +12 voltages are input from an external power supply and the -10 volt supply is generated internally in the disk drive.) At power on, the Power On Reset output signal is active, holding the electronics in disk drive in a reset condition until the voltages reach their proper levels. During operation of the disk drive, if any one of the voltages falls below a predetermined level, Power On Reset will become active and shut down operation of the disk drive.

4.4 Data PCB

Functions performed by the Data PCB are described in the following paragraphs.

4.4.1 Microprocessor and PLA

The V100 Series employs a microprocessor and a programmed logic array (PLA) to control its internal operations. These devices receive commands from the device dependent controller over the control lines of the ST412/506 Interface bus. These operations include servo control, spindle speed control, read/write operations, and error/fault reporting.

The microprocessor consists of a single chip microcomputer IC which incorporates an 8-bit central processing unit (CPU), 8 kilobytes of program memory (ROM), 256 bytes of data memory (RAM), input/output lines, and a serial port. The microcomputer is clocked by an external 9.126-MHz clock generator. (This generator also provides 1.152-MHz and 576-kHz signals for the actuator servo control demodulator and a 360-Hz signal for the spindle motor speed control circuit.)

The programmed logic array is a custom-designed IC which augments the operation of the microprocessor. Functions handled by the PLA include status logic, write fault monitor, read/write selection, and step control.

4.4.2 Microprocessor/PLA Control Signals

Signals generated by the microprocessor for control purposes within disk drive include: Seek, Odd In, Pick, Counter Reset, Normal Regulation, Stop Motor, Inner Track, Servo Enable, Even In, Velocity Command, Speed, and Seek Complete. PLA generated signals include Write Gate, Seek Complete, Write Fault, and Ready.

Signals input to the microprocessor from circuitry internal to disk drive include: Power On Reset, Index, At Speed, Count Not Ready, Fault, Track 0, Off Track, On Peak, Direction In, Write Gate, and 9.216 MHz clock. Internal inputs to the PLA include Power On Reset, Fault, Write Gate, Drive Select, Stop, Seek Complete, and At Speed.

4.4.3 Disk Drive Control Functions

The ST412/506 Interface control signals input to disk drive via input buffers are Step STEP-L, Drive Select DS0-L, Head Select HS0-L through HS8-L, Direction DIR-L, and Write Gate WGATE-L. These signals are applied to either the microprocessor or the PLA.

The ST412/506 Interface control signals output from disk drive via output drivers are Seek Complete SKCMP-L, Track 0 TRK0-L, Write Fault WFLT-L, and Ready RDY-L. The majority of these signals are output by the microprocessor or the PLA.

Head Select lines HS0-L through HS8-L are applied via input buffers to head select and control logic which outputs Chip Enable signal CE and head select lines to the read preamplifier/write driver ICs in the sealed head-disk assembly.

4.4.4 Input Buffers

The ST412/506 Interface control signals from the controller are input to the microprocessor and the PLA via schmitt trigger input buffers.

4.4.5 Output Drivers

The ST412/506 control signals from disk drive are output via open-collector drivers. Each driver is capable of sinking a maximum of 48 milliamperes at its low level (true state) with a maximum of 0.4 measured at the driver. When the driver is in its high level (false state), the driver transistor is off. The output control signals are gated by a Drive Select line developed from the Drive Select input DS0-L.

4.4.6 Disk Drive Data Functions

Data signals passed between disk drive and the controller are passed over the ST412/506 Interface data lines. MFM Read Data signals RMFM+, RMFM- from the read/write data channel are output to the controller via a differential line driver. MFM Write Data signals WMFM+, WMFM- from the controller are input to the drive read/write data channel via a line driver.

4.4.7 Read/Write Data Channel

The read/write data channel includes head select and control logic, a read chain which amplifies and qualifies the differential MFM-encoded read signal from the read preamplifier/write driver ICs in the sealed head-disk assembly, and a write channel which converts the TTL-level MFM-encoded write data signal from the controller into write current drive for the read preamplifier/write driver ICs.

4.4.8 Head Select and Control Logic

The head select and control logic block performs a hardware decode of ST412/506 Head Select signals HS0-L through HS4-L and the Write Gate signal from the PLA. The output signals from the block enable the write driver/read preamplifier IC, select one of four read/write heads, and activate the read function or write function. The output lines are labeled Chip Enable CE0-L, CE1-L; binary Head Select bits HS1-H, HS2-H; and Write Enable WS. When two ICs are used to control seven heads, Chip Enable CE0-L selects one IC for controlling heads 0 through 3, and CE1-L selects the other IC for controlling heads 4 through 6. Signals HS1-L, HS2-H, and WS are input to both ICs.

4.4.9 Read Chain

The read chain receives differential voltage DX, DY from the read preamplifier portion of the read preamplifier/write driver ICs. This signal represents magnetic transitions seen by the head as it flies over the magnetic media. Whenever the head passes over a magnetic transition, the preamplifier differential output peaks. The read chain amplifies this differential analog signal and converts it to a stream of differential logic-level pulses, one for every signal peak. These MFM-encoded pulses are sent to the controller for decoding. The read chain circuitry includes an amplifier/signal conditioner stage and a differential line driver.

4.4.10 Amplifier/Signal Conditioner

In the amplifier section of the block, the differential DX, DY input is amplified, filtered and subjected to automatic gain control (AGC). A diode matrix at the input of the amplifier, controlled by the Write Enable signal from the microprocessor, isolates the read chain from the write chain during a write operation. The AGC circuit compensates for signal variations caused by normal differences in head flying height, head characteristics, and media. The AGC circuit includes an AGC hold feature which maintains AGC control when writing. Following AGC, the signal is differentiated, filtered and input to a zero-crossing detector which converts the differential analog signals into logic-level pulses.

The signal conditioner section prevents noise in the analog input signal from producing false zero-crossings. This is achieved by applying the input of the zero-crossing detector to a gating circuit which effectively screens out spurious pulses caused by noise.

4.4.11 Differential Line Driver

The qualified output signal is coupled via a differential line driver to the ST412/506 Interface. The output lines from the line driver are labeled RMFM+, RMFM-.

4.4.12 Write Chain

The write chain receives differential MFM-encoded write data from the controller and converts the data to a differential signal suitable for transmission to the write driver section of the read preamplifier/write driver ICs. The write chain circuitry includes a line receiver, a transition generator, a write current source, and a write fault detector.

4.4.13 Line Receiver

The line receiver translates the differential MFM-encoded write data on the ST412/506 Interface WMFM+, WMFM- lines into a single-ended format suitable for input to the transition generator. The output of the line receiver is a positive-going pulse for every magnetic transition to be written on the disk.

4.4.14 Transition Generator

The transition generator divides the MFM frequency by two so that the logic level of the output determines the direction of current through the head. Each transition in MFM generates a transition on the media.

4.4.15 Write Current Source

The write current source provides current for the read/write heads and supplies a write control (WC) signal to the read preamplifier/write driver ICs. The write current source is enabled by the Write Gate line from the PLA and has two outputs, selected by the Inner Track line. For tracks 0 to 511, the write current output is 32 milliamperes and for tracks 512 and above, the write current is 27.5 milliamperes.

4.4.16 Write Fault Detector

During a write operation, the microprocessor monitors certain key parameters of the function via the write fault detector. If an abnormal condition is detected, the PLA activates the Write Fault signal WFLT-L. Inputs to the write fault detector include Unsafe signal US from the write driver/read preamplifier IC, and other logic lines. The faults which can cause WFLT-L to become active are discussed in sections 4.5.8 and 5.3.3.

4.5 Operational Sequence

The following paragraphs describe the series of events which occur from the time power is applied to the drive to the actual writing and reading of data.

4.5.1 Power On Reset

Power On Reset is active, holding the drive electronics in a reset condition, until the +5 volt, +12 volt DC power supplies are on.

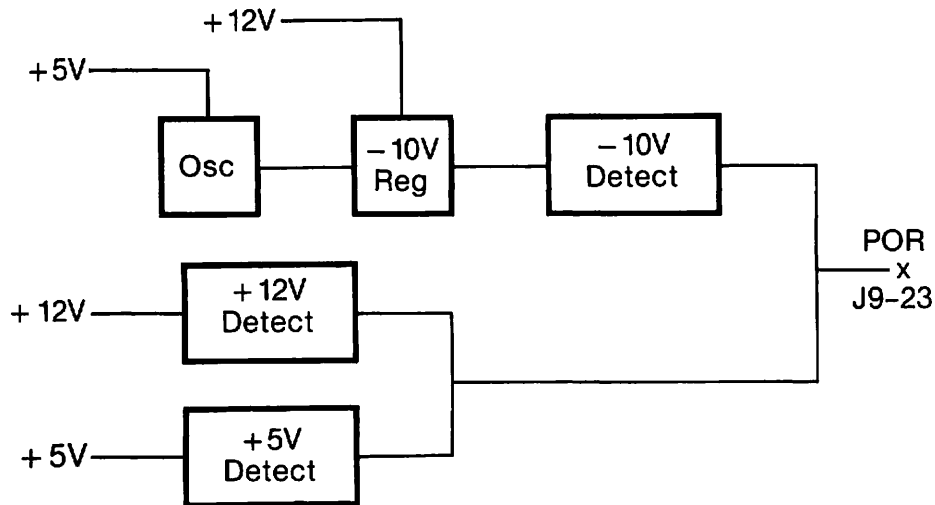


Figure 4-1
Power Reset

If any of the above functions fail, Power On Reset will be activated.

4.5.2 Motor Start

After the POR is turned off, the microprocessor checks the Customer Option line called Start Motor to see if it is true. If so, the processor forces the Stop Motor signal false which causes the motor brake relay to pick. The processor also disables the line called Normal Regulation, thus allowing the motor to accelerate without any regulation. The processor monitors the motor speed by measuring the time between index pulses. When the time between index pulses reaches $<1\%$ of 3600 rpm, the processor activates the line called Normal Regulation.

The Motor Speed Regulator is a phase lock frequency regulator which uses 360 Hz from the driver oscillator and signals from the three Hall-Device sensors from the motor to control the speed of the motor.

The processor monitors the lines called At Speed and Count Not Ready to ensure that the motor is operating correctly throughout the rest of the time that the drive is in operation.

Reference Servo Diagrams Section 9

4.5.3 Actuator Lock

The actuator lock is picked after At Speed is true to the processor. The processor activates the line called Pick, which in turn activates the actuator lock driver. By picking the actuator lock, this allows the actuator to move the head out into the data zone of the pack. The processor waits for a period of time before enabling the servo to ensure that the actuator lock did pick.

Reference Servo Diagrams Section 9

4.5.4 Servo Restore to Track 0

The processor enables Pick which moves the actuator over the data area and out of the landing zone to the outer guard band area. Once the processor detects that the actuator is in the outer guard band area, the processor will cause the servo to move to and settle on a data track. The processor will Set Direction Out and a slow velocity, counting track crossings until the track 0 signal is detected. The processor will cause the servo to lock onto a track and check for the track 0 signal. After the servo is locked onto a track and track 0 is activated, the processor will initialize its minimum and maximum track counter. When this is accomplished the processor will activate Drive Ready and Seek Complete.

Reference Data Board Diagrams Section 8 and Servo Board Diagrams Section 9

4.5.5 Seek Operation

The Drive has to have Ready and Seek Complete active before a seek operation can start. With the drive in this condition, the processor is in its basic loop monitoring Motor Speed, Off Track and looking for either a Step pulse or Write Gate which are gated by Drive Select. When a Step pulse is received, the Step pulse forces Seek Complete false. If Write Gate is active and Seek Complete goes false, this will cause a fault condition to be issued, automatically deactivating the write circuitry. When a Step pulse is received and Write Gate is not active, then the processor will initiate a Seek operation. The processor will set the direction of motion from the interface line called Direction. It will also set Seek mode, at this time the servo will start to move. The speed in which the servo moves is dependent on the rate at which the Step pulses are received and the distance it has to travel. The servo will reach its maximum velocity if the pulse rate of the Step pulses is faster than 39 microseconds.

The processor counts the number of track crossings and compares it to the number of Step pulses. When the servo is crossing the last track, the processor switches the servo from Seek mode to Position mode. It starts the settling timer and looks for an Off-Track condition.

If an Off-Track condition exists, the processor restarts the settling timer. This is done until the Off-Track condition is cleared plus settling time. Once this is accomplished, the processor sets Seek Complete.

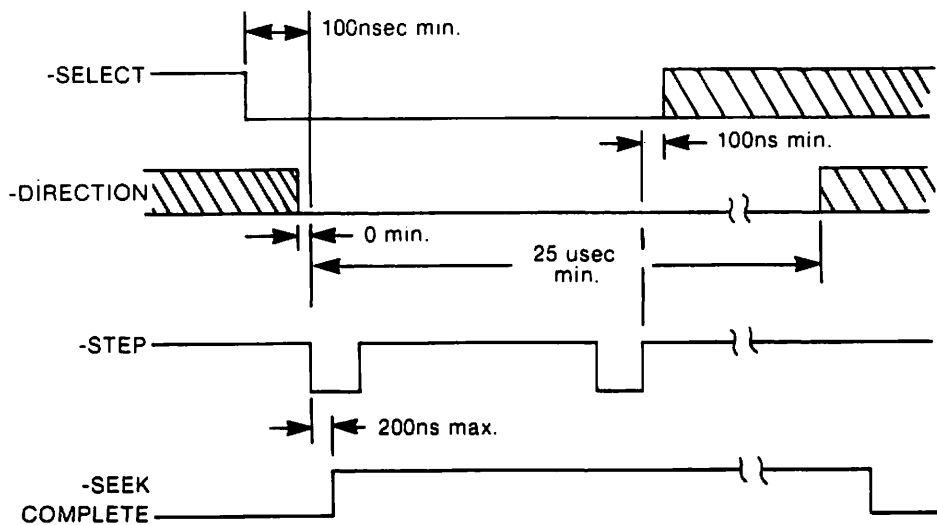


Figure 4-2
General Seek Timing

- DIRECTION change can be concurrent with the first STEP.
- DIRECTION must not be changed within 25 μ sec from the leading edge of the first STEP pulse; after this time, it is latched and ignored until Seek Complete is true.
- SEEK COMPLETE will go false within 200ns after the leading edge of STEP.
- Drive cannot be deselected prior to the trailing edge of the last STEP pulse + 100ns to assure detection of the last pulse.

4.5.6 Track Format

The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors. The format is a soft sectored type which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. The ID field is followed by a user supplied data field.

The format is a slightly modified version of the IBM System 34 double density format which is commonly used on floppy disk drives. The encoding method is Modified Frequency Modulation (MFM).

Figure 4-4 shows the track format based on 32 sectors, each having 256 bytes of user information. The beginning of both the ID and data fields are flagged by unique characters called address marks. An address mark is two bytes in length. The first byte is an "A1" data pattern. This is followed by either an "FE" pattern for an ID address mark, or an "F8" pattern for the data address mark.

The "A1" pattern is made unique by violating the encoding rules of MFM omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination that occurs on the track. See Figure 4-3 depiction of the "A1" byte. Each ID and data field is followed by a 16-bit cyclic redundancy check (CRC) character used for a particular data pattern.

Surrounding the ID and Data fields are gaps to establish physical and timing relationships between these fields.

4.5.6.1 GAP 1

Gap 1 is to provide for variations in Index detection. Gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field preceding the first ID field.

4.5.6.2 GAP 2

Gap 2 follows the CRC bytes of the ID field, and continues to the data field address mark. It provides a known area for the data field write splice to occur. The latter portion of this gap serves as the sync up area for the data field AM. Gap 2 is 16 bytes. Minimum length required is determined by the "lock up" performance of the phase-lock-loop in the data separator, which is part of the host control unit.

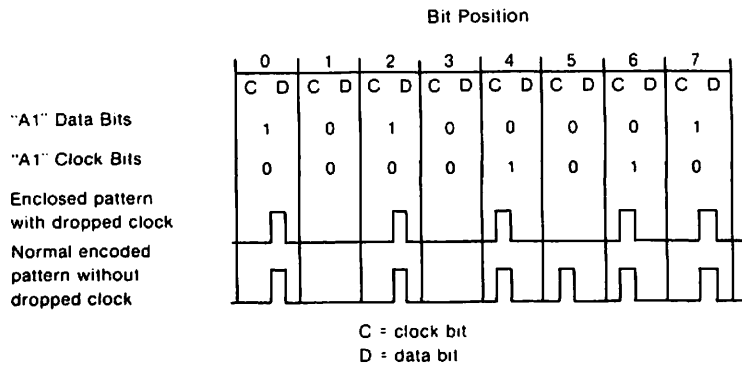


Figure 4-3
"A1" Address Mark Byte

4.5.6.3 GAP 3

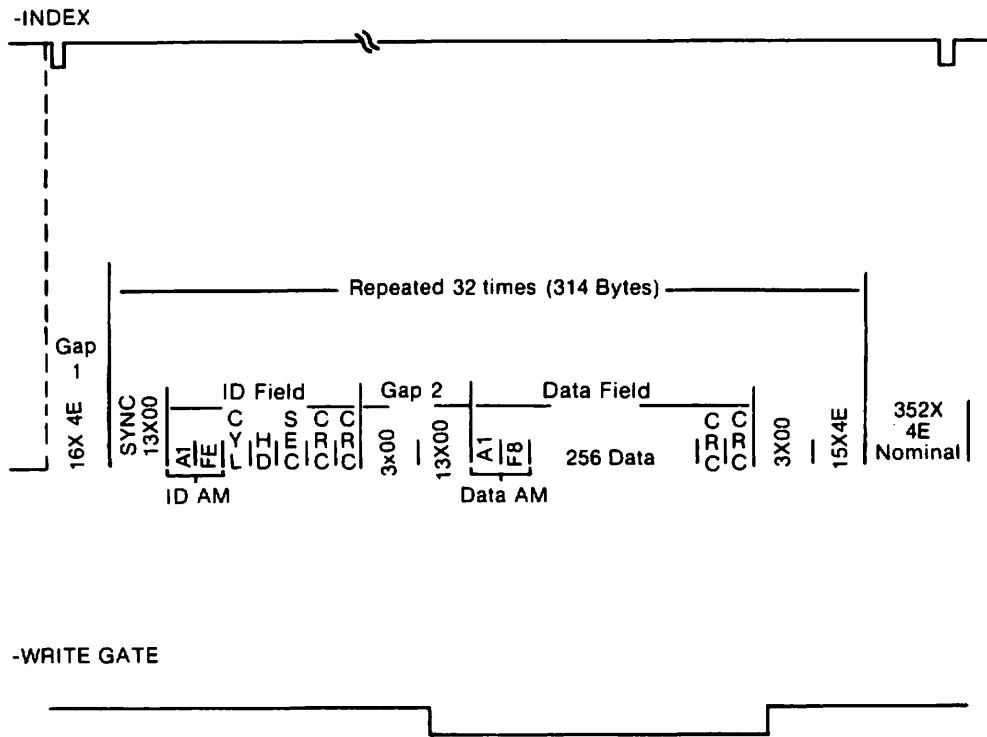
Gap 3 following each data field allows for the spindle speed variations. This allows for the situation where a track has been formatted while the disk is running faster than normal, then write updated with the disk running slower than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field could be overwritten. The gap allows a $\pm 3\%$ speed variation (actual drive spec is $\pm 0.1\%$). Minimum gap is 8 bytes for a 256-byte record size.

4.5.6.4 GAP 4

Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depend on the exact rotating speed during the format operation.

4.5.6.5 SECTOR INTERLEAVING

Most track formats use an interleave factor of 4. That is, sequentially sectored ID numbers are 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26, etc. This allows sufficient system turnaround time to process multiple sectors during a single revolution, thus enhancing through-put of typical file read/write operations. The 8-microsecond write/read recovery time of the V100 drives permits use of an interleave factor of 1, however.



NOTES:

1. Nominal Track Capacity = 10,416 Bytes
2. Total Data Bytes/Track = 256 × 32 = 8,192
3. Sector interleave factor is 4. Sequential ID fields are sector numbered 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26 . . . etc.
4. CRC Fire Code = $x^{27} + x^{23} + x^6 + 1$
5. Bit 5 of Head Byte reserved for numbering cylinders greater than 256.
6. Bit 6 of Head Byte reserved for numbering cylinders greater than 512. Bit 7 of Head Byte reserved for numbering cylinders greater than 1024.
7. The V100 Series drives are shipped unformatted.

Figure 4-4
Typical Track Format

4.5.7 Read Operation/Head Select

The processor is not actively involved in a normal read/write operation. The head select is done directly by a hardware decode of the three head select interface lines along with Drive Select. Drive Select also enables the read data line drivers on the interface.

The read data is passed to the controller as MFM encoded data. It is the responsibility of the drive controller to decode the data and identify address mark, gaps, and the different types of data fields on the specific track being read by the drive. The drive can only tell the controller where the beginning and ending of the track is, and that is with a signal called Index.

Reference Data Board Diagrams Section 8

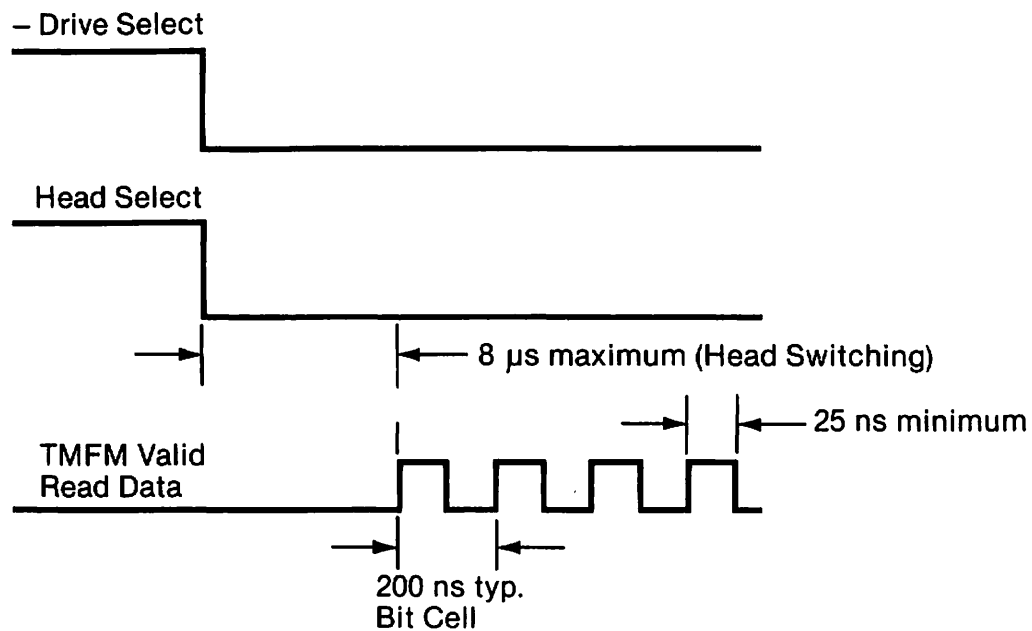


Figure 4-5
Typical Read Timing

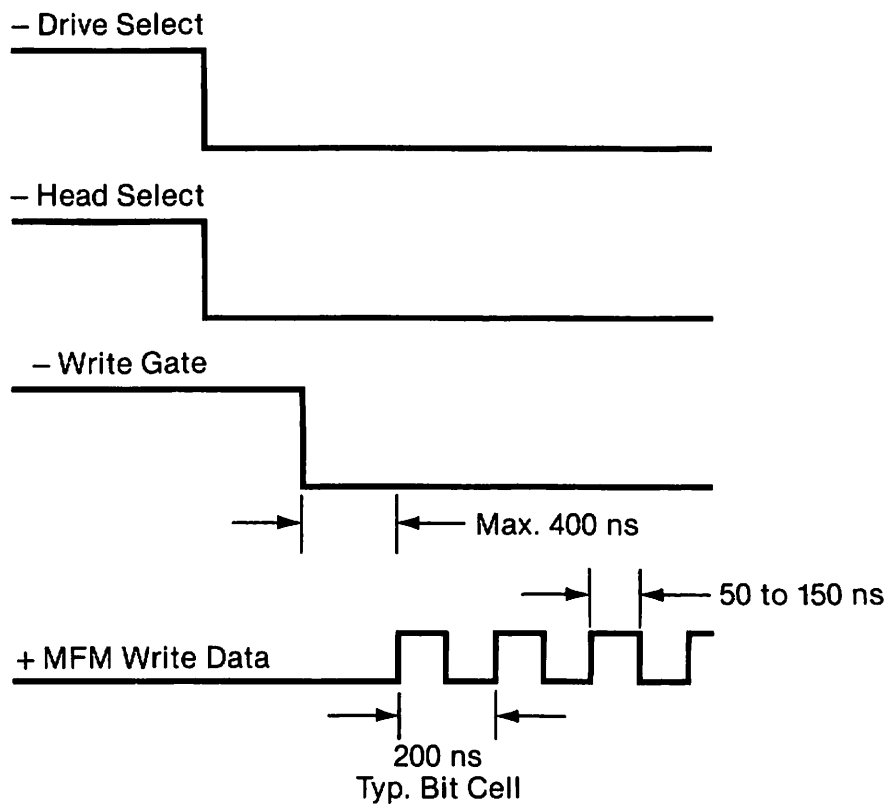


Figure 4-6
Write Data Timing

4.5.8 Write Operation/Fault Detection

During a write operation the microprocessor monitors two important items. They are:

1. **Off-track**—If this occurs, the processor posts a fault condition.

If an Off-track occurs during a Write sequence, the drive will present a not Seek Complete and Write Fault (as long as Write Gate is true). The drive requires the Off-track signal to be false for 20 milliseconds before testing the Select line. This assures that the cause of Off-track has been removed.

The following is a suggestion for handling this fault sequence:

Start: Write Fault with not Seek Complete

- 1) Start 25 millisecond timer
- 2) Deselect Drive
- 3) Wait 20 microseconds
- 4) Select Drive
- 5) Test Status
Status good—return to normal operations
- 6) Has Timer elapsed
Yes—go to drive bad routine
No—go to 1)

The above sequence assumes that the cause of the Off-track was an impulse which caused only 1 or 2 Off-tracks and heads do not change track. If the impulse is extreme or a constant severe vibration is the cause, the drive may go through RECAL and self test which could take as long as one second after the cause is removed.

If no Write Fault occurs with the Off-track, the drive will automatically resume normal operation after settling or RECALing, depending on the severity of the original cause.

2. **Chip Fault**—The chip fault monitors write current and not write gate, no write current and write gate, multihead select, and illegal head select. Chip fault will be set if any of these conditions happen and a fault condition will be posted.

If no fault conditions exist, a write operation can be performed.

There are two types of write operations. One is what is called the format write. This write operation typically starts when the leading edge of index occurs and continues until the leading edge occurs again. A typical track format is shown in Figure 4-4. The second type of write operation is called an update write. This type of write has to know where the field is located on the track before it can be written.

The drive, regardless of which type of write operation, performs the same sequence of events in order to accomplish the operation.

Reference Data Board Diagrams Section 8

4.6 Error Definition

4.6.1 Soft (Recoverable) Errors

Soft or recoverable errors are specified to occur at a rate equal to or less than one in 10^{10} bits transferred.

Data patterns and track position shall not affect data error performance.

To be considered recoverable, the error must be recovered in no more than five attempts to read the record.

4.6.2 Hard (Non-Recoverable) Errors

Hard or non-recoverable errors are specified to occur at a rate equal to or less than one in 10^{12} bits transferred.

A hard error is one which remains after five attempts to read the record in which the error is located.

4.6.3 Seek (Access Position) Errors

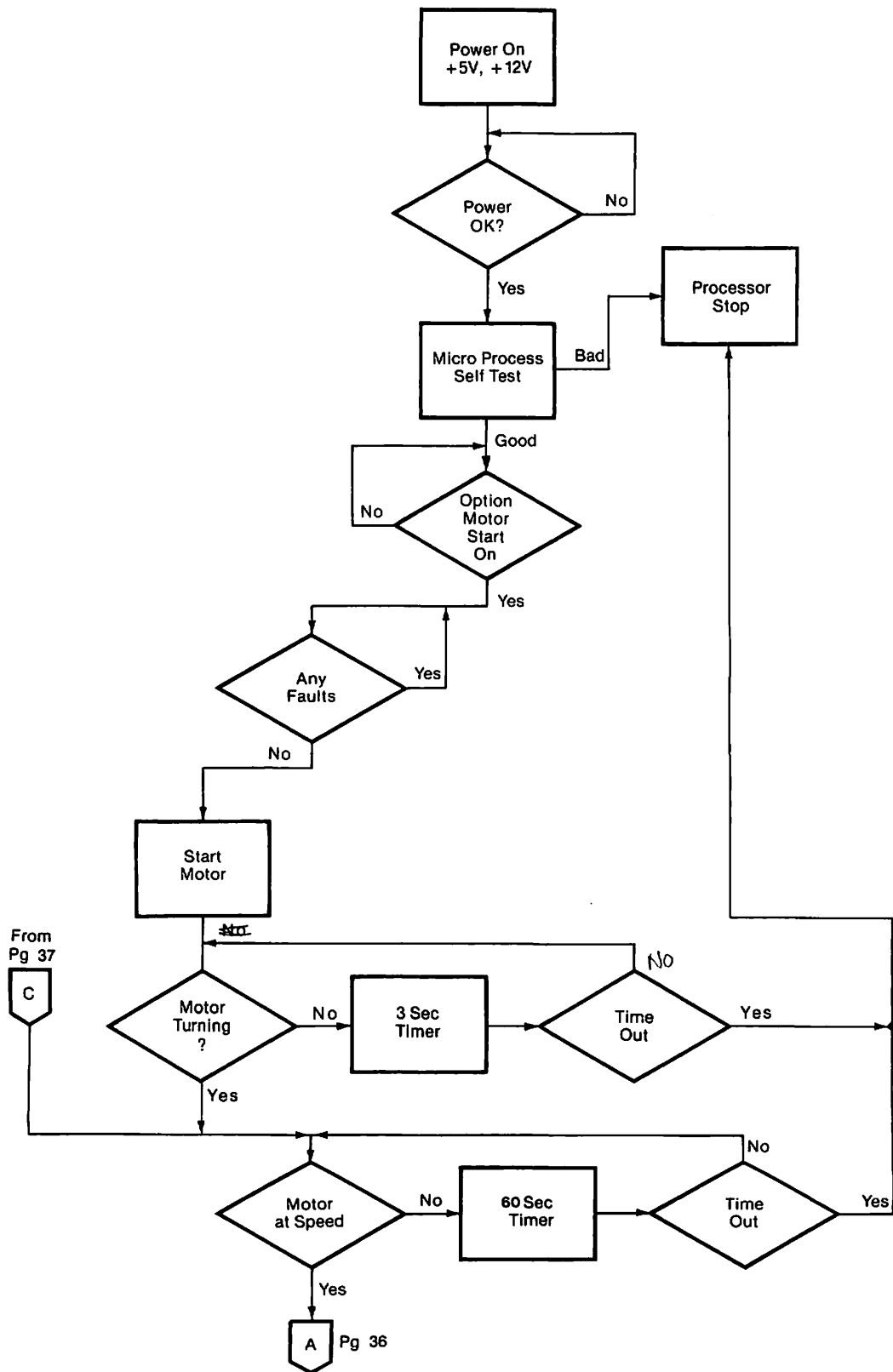
Seek errors are specified to occur at a rate equal to or less than one in 10^6 seeks.

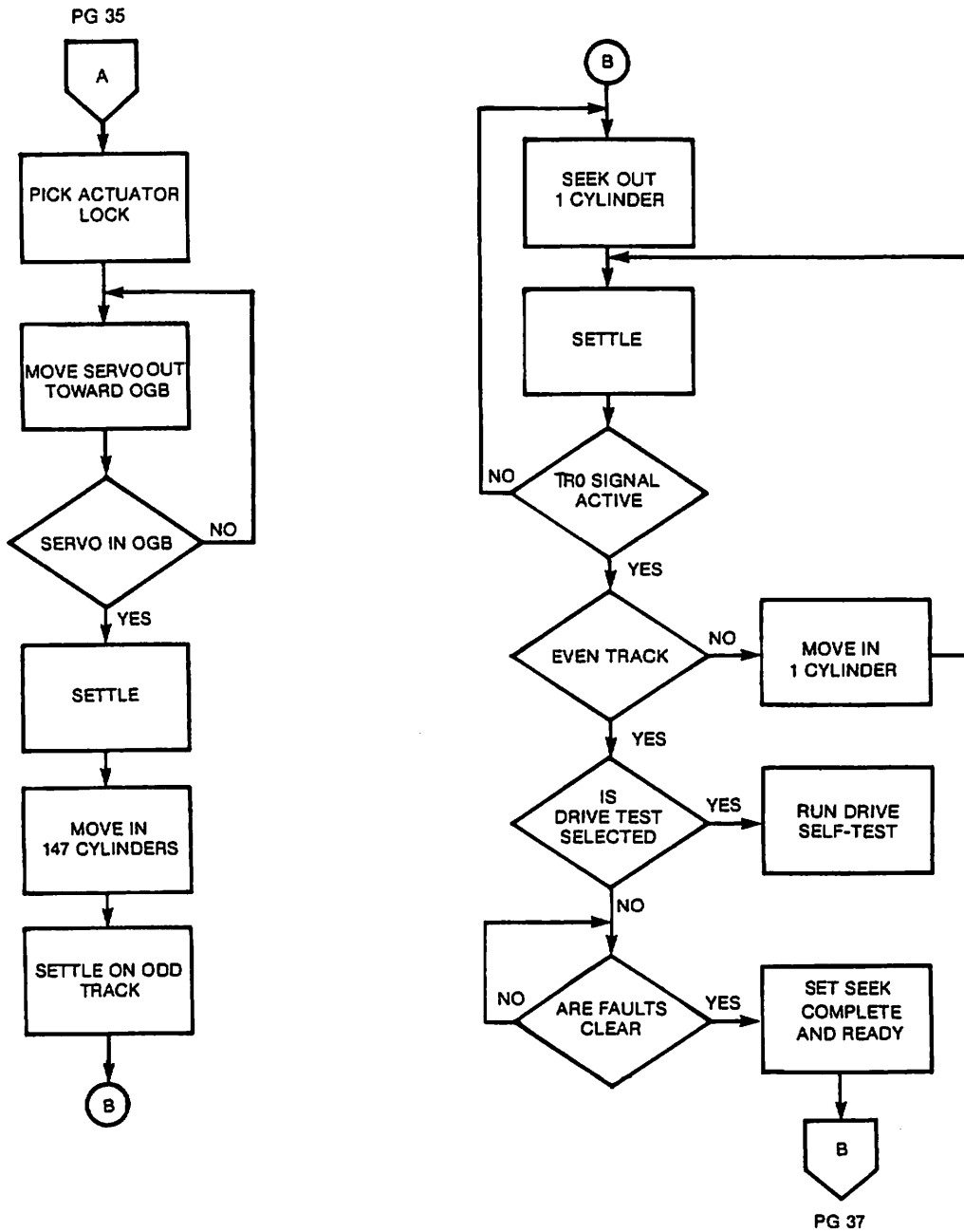
A permanent seek error is one which remains after the execution of the following procedure:

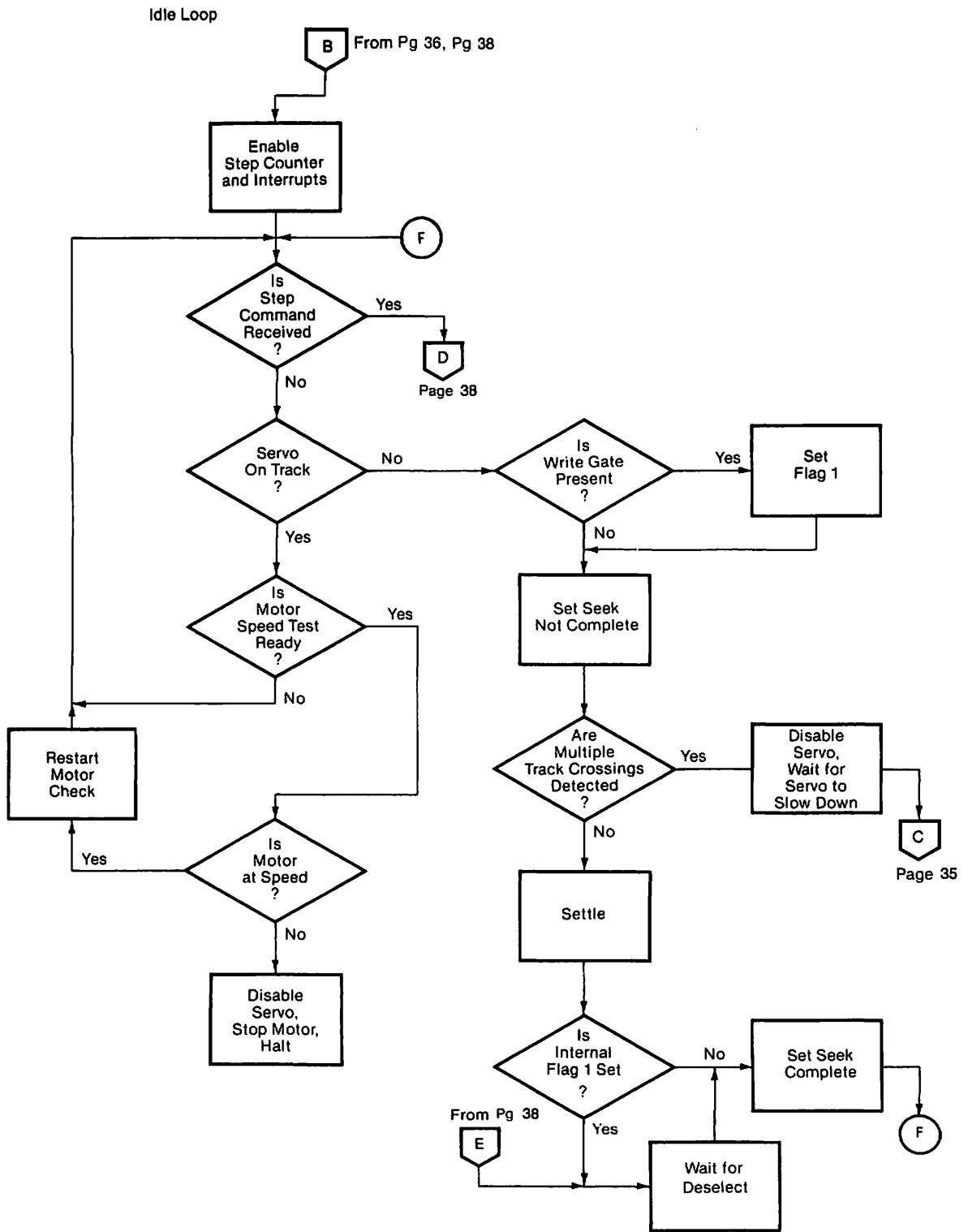
- Re-read record five times.
- Recalibrate to Track 0 and re-seek to error cylinder.
- Re-read record five times.
- Seek to inner-most cylinder and re-seek to error cylinder.
- Re-read record five times.

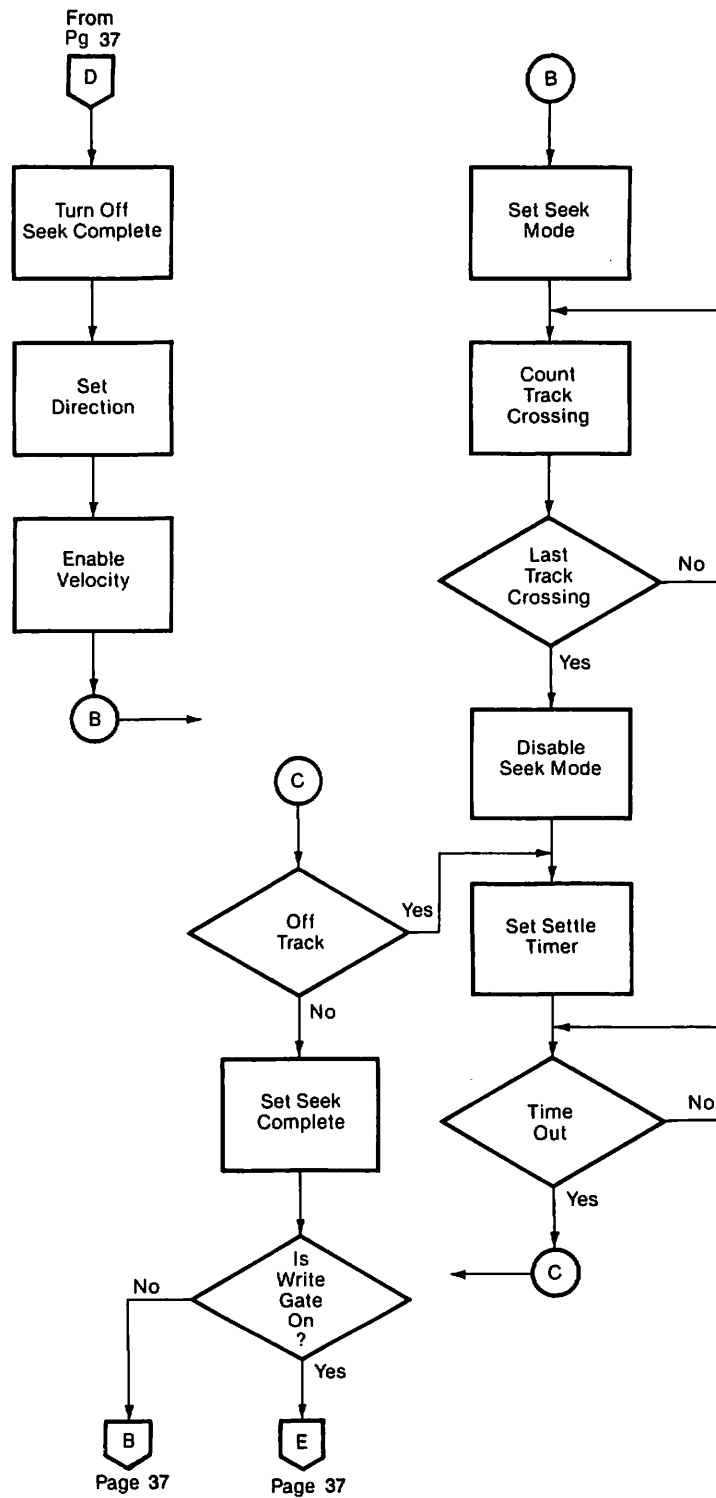
A soft error seek is one which is cleared at any point in the procedure above.

4.7 Drive Operation Flow Chart









5 ELECTRICAL INTERFACE

5.1 Electrical Interface Overview

The interface to the V100 can be divided into three categories, each of which is physically separated:

1. Control signals
2. Data signals
3. DC Power

All control lines are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the host (output) via interface connector J1/P1. The data transfer signals are differential in nature and provide data either to (Write) or from (Read) the drive via J2/P2 (defined by EIA RS-422).

Tables 5-1 through 5-3 and Figures 5-1 through 5-3 show connector pin assignments and interconnection of cabling between the host controller and drives.

Table 5-1
J1/P1 Connector Pin Assignment

GND RTN PIN	SIGNAL PIN	SIGNAL NAME	TERMINATED?
1	2	-NOT USED	YES
3	4	-HEAD SELECT 2 ²	YES
5	6	-WRITE GATE	YES
7	8	-SEEK COMPLETE	NO
9	10	-TRACK Ø	NO
11	12	-WRITE FAULT	NO
13	14	-HEAD SELECT 2 ⁰	YES
15	16	-RESERVED (TO J2 PIN 7)	NO
17	18	-HEAD SELECT 2 ¹	YES
19	20	-INDEX	NO
21	22	-READY	NO
23	24	-STEP	YES
25	26	-DRIVE SELECT 1	YES
27	28	-DRIVE SELECT 2	YES
29	30	-DRIVE SELECT 3	YES
31	32	-DRIVE SELECT 4	YES
33	34	-DIRECTION IN	YES

NOTE: THE TERMINATIONS ON J1 SIGNALS CAN BE REMOVED BY REMOVING THE RESISTOR PACK FROM ITS SOCKET ON THE DATA (OUTSIDE) BOARD.

Table 5-2
J2/P2 Connector Pin Assignment

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	-DRIVE SELECTED
4	3	RESERVED
6	5	SPARE
8	7	RESERVED (TO J1 PIN 16)
	9	SPARE
	10	SPARE
12	11	GND
	13	+MFM WRITE DATA
	14	-MFM WRITE DATA
16	15	GND
	17	+MFM READ DATA
	18	-MFM READ DATA
20	19	GND

} Permanently Terminated

Table 5-3
P3—DC Connector Pin Assignments

VOLTAGE	
PIN 1 + 12 VOLTS DC	PIN 2 + 12 VOLT RETURN
PIN 4 + 5 VOLTS DC	PIN 3 + 5 VOLT RETURN

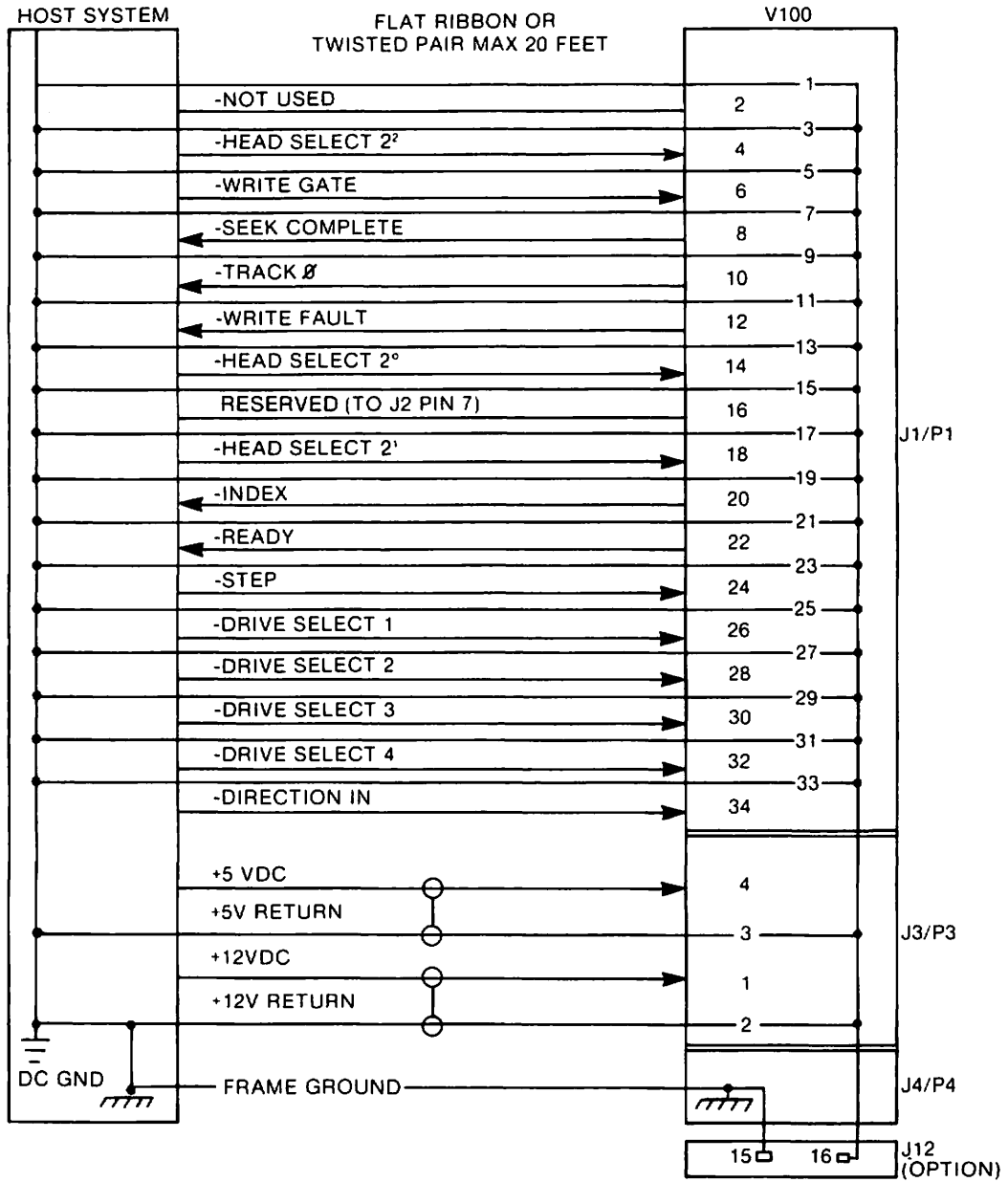


Figure 5-1
Control Signals

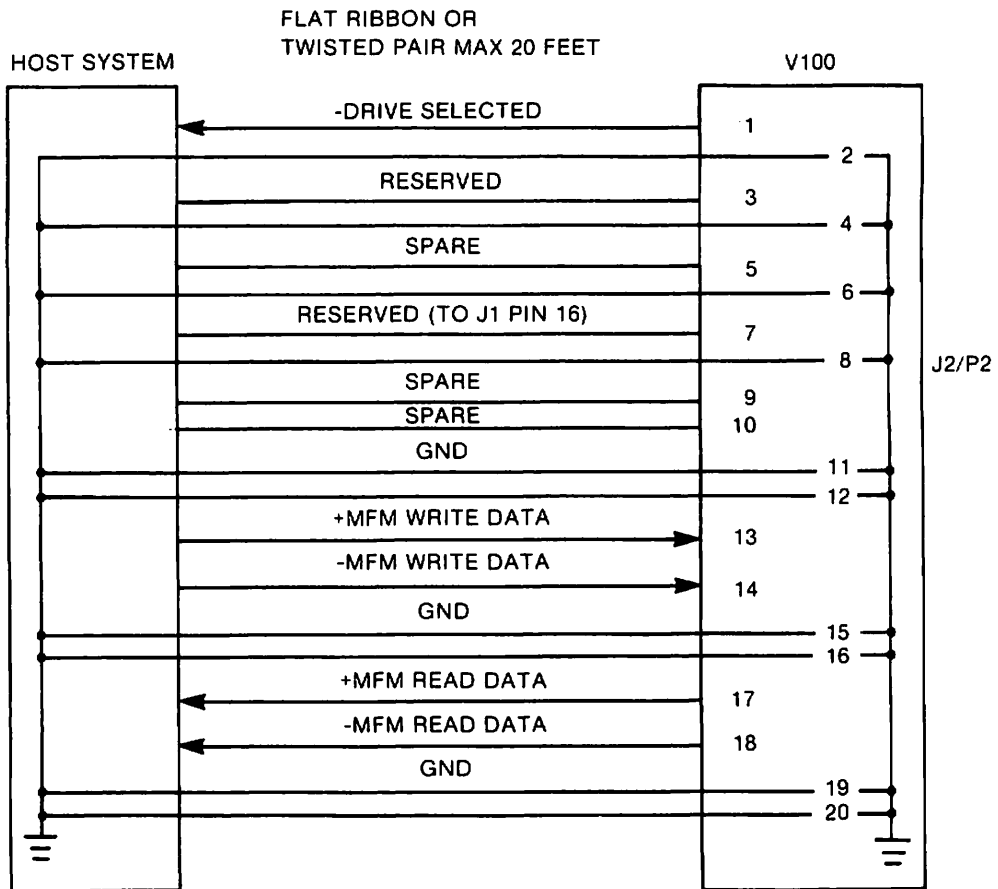
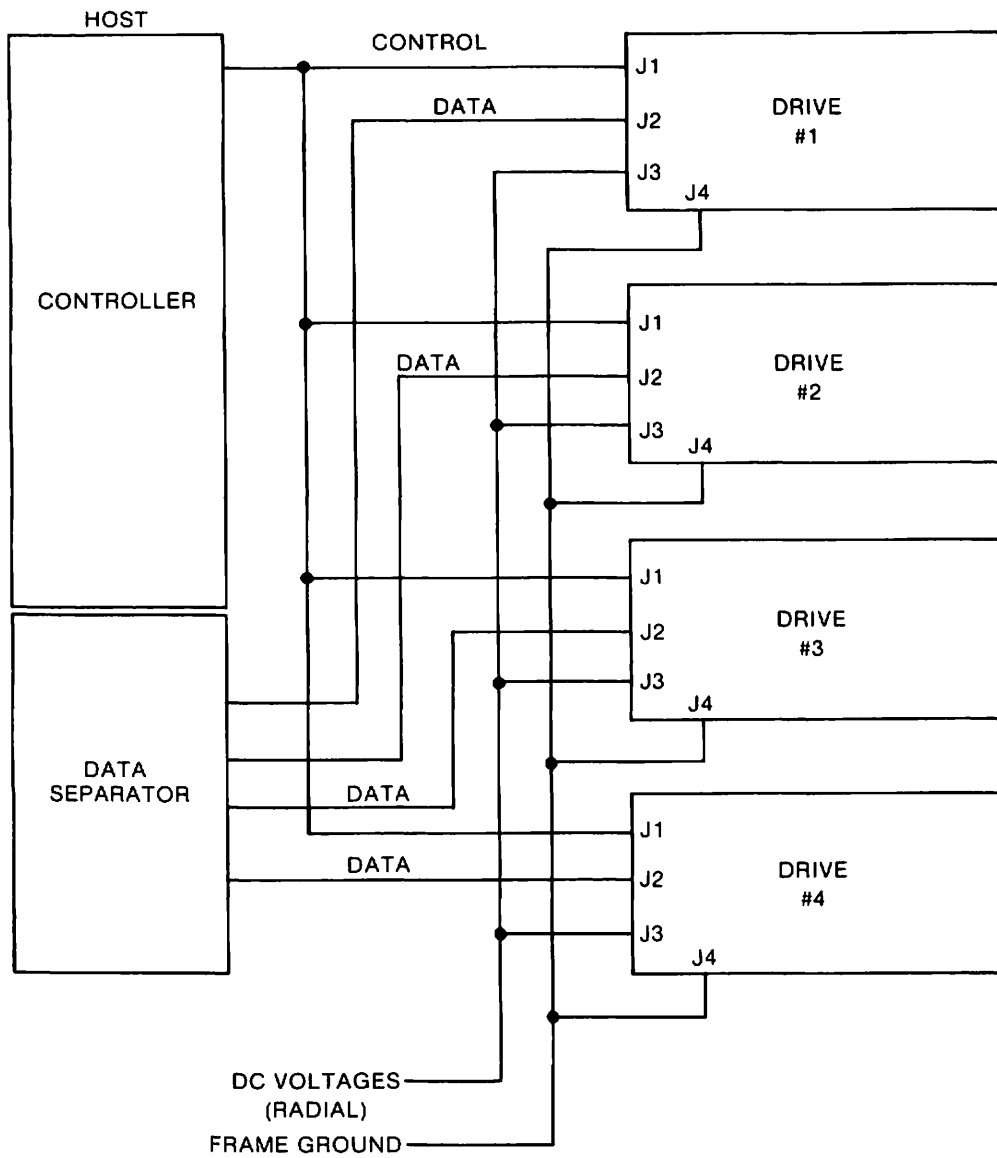


Figure 5-2
Data Signals



Note: Termination resistor pack to be installed only in the last physical drive on line.

Figure 5-3
Typical Connection 4-Drive System

5.2 Control Input Lines

The control input signals are of two types: those to be multiplexed in a multiple drive system, and those intended to do the multiplexing. The control input signals to be multiplexed are WRITE GATE, HEAD SELECT 2⁰, HEAD SELECT 2¹, HEAD SELECT 2², STEP and DIRECTION IN. The signal to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to Figure 5-4 for the recommended circuit.

TRUE 0.0VDC to 0.4VDC @ 1 = 48mA (MAX), Active, Logic 1.

FALSE 2.5VDC to 5.25VDC @ 1 = +250 μ A (OPEN COLLECTOR), Inactive, Logic 0.

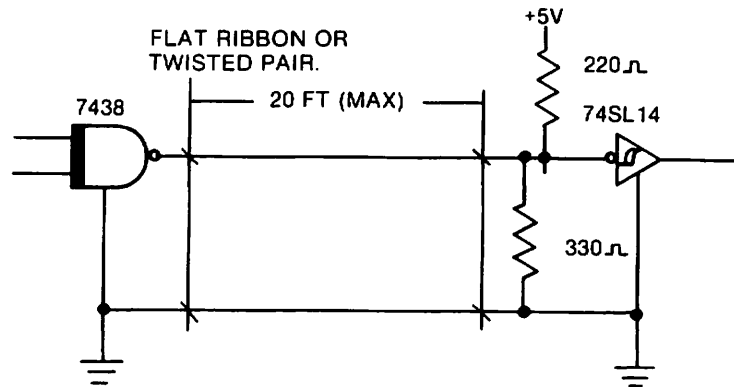


Figure 5-4
Control Signals Driver/Receiver Combination

5.2.1 Write Gate

The active state of this signal, or low level, enables write data to be written on the disk. The inactive state of this signal, or high level, enables data to be transferred from the drive.

A 220/330-ohm resistor pack allows for line termination.

5.2.2 Head Select 2^0 , 2^1 , and 2^2

These three lines allow selection of each individual read/write head in a binary coded sequence as shown below:

HEAD SELECTED	HEAD SELECT LINE		
	2^2	2^1	2^0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0

A 220/330-ohm resistor pack allows for line termination.

5.2.3 Direction In

This signal defines direction of motion of the R/W head when the STEP line is pulsed. A high level defines the direction as "out" and if a pulse is applied to the STEP line, the R/W heads will move away from the center of the disk. If this line is a low level, the direction of motion is defined as "in" and the R/W heads will move toward the center of the disk. Change in direction must meet the requirement shown in Figure 4-2.

A 220/330-ohm resistor pack allows for line termination.

5.2.4 Step

This interface line is a control signal which causes the R/W head to move in the direction of motion defined by the DIRECTION IN line. The access motion is initiated during the low level of the signal pulse. V100 drives operate in buffered seek mode only. See Figure 5-5 for timing considerations.

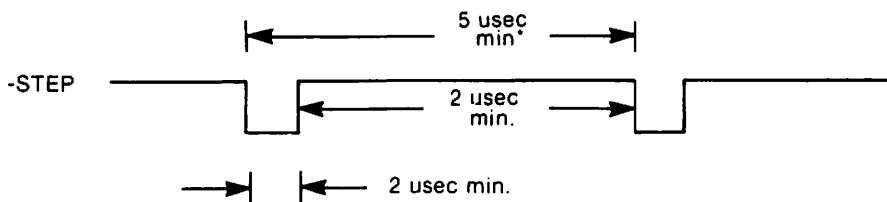


Figure 5-5
Buffered Step

- * No maximum, however, seek complete will come true if rate is slower than 5ms (1 track + settle).
- Step periods exceeding 39 μ sec will extend access times.

One Step Pulse = One Step = One Track

The processor will automatically stop the head over the most inner or outer track if the number of step pulses exceeds the number of data tracks available in the direction given. This feature allows a fast recalibrate to Track 0. Simply issue 1167 or greater step pulses in the direction toward Track 0. The heads will automatically stop at Track 0, regardless of where they were originally positioned.

Note: The innermost accessible track on the V130, V150, or V170 is track 1003. The innermost track on a V185 is track 1167.

If the processor expects to arrive at Track 0 and the Track 0 indicator is not true, an Auto re-cal will be performed before SEEK COMPLETE becomes true.

A 220/330-ohm resistor pack allows for line termination.

5.2.5 Drive Select 1-4 (Figure 5-9)

DRIVE SELECT, when a low level, connects the drive interface to the control lines. Cutting the appropriate shunts at IC position will determine which select line on the interface will activate that drive. The following table indicates which DRIVE SELECT shunts must be cut.

J6 OPTIONS		
DRIVE SELECT	CUT SHUNTS OR	SHORTING PLUGS
DS1	10-7, 11-6, and 12-5	Short 9-8
DS2	9-8, 11-6, and 12-5	Short 10-7
DS3	9-8, 10-7, and 12-5	Short 11-6
DS4	9-8, 10-7, and 11-6	Short 12-5

5.3 Control Output Lines

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and the collector leakage current is a maximum of 250 μ A.

All J1 output lines are enabled by their respective DRIVE SELECT line.

Figure 5-4 shows the recommended circuit.

5.3.1 Seek Complete

This line will go to a low level or true state when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when SEEK COMPLETE is false.

SEEK COMPLETE will go false in four cases:

1. A recalibration sequence is initiated (by drive logic) at power on, if the R/W heads are not over track zero.
2. 200ns max after the leading edge of a step pulse or series of step pulses.
3. Any momentary loss of +5 volts or +12 volts or spindle speed.
4. If internal servo error signal OFF TRACK is active during writing or reading.

5.3.2 Track 0

This interface signal indicates a low level or true state only when the drive's R/W heads are positioned at cylinder zero (the outermost data track).

5.3.3 Write Fault

This signal becomes TRUE whenever a condition arises which makes writing unsafe. This will occur under the following conditions:

1. WRITING

- A. Open head
- B. Shorted head
- C. No Write current
- D. An Off-track occurs

Write fault line must be edge detected and latched in the controller. If an "off-track" error is detected by the servo system during a write operation, write fault will be asserted, but only as long as the controller is giving write gate. Internally, Write gate is shut off within 12 μ sec of seeing "off-track."

- E. Invalid or multiple heads are selected
- F. Spindle speed loss while writing
- G. A Write is attempted when SEEK COMPLETE is false
- H. A Write is attempted when the drive is write protected through the WRITE PROTECT option
- I. WRITE gate but not write data
- J. Attempted Write with READY false

2. READING

- A. Write current appears in the head

The drive will accept no more commands once a WRITE FAULT is detected by the processor.

5.3.4 Index (Figure 5-6)

This interface signal is provided by the drive once each revolution (16.67ms nom.) to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX. Only the transition from high to low is valid for timing purposes. The signal is generated by a transducer in the spindle motor.

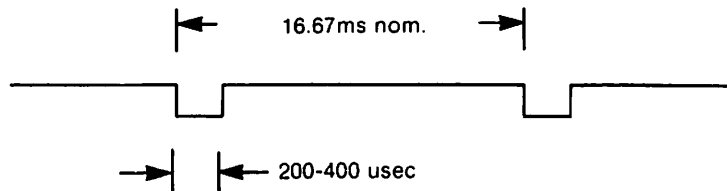


Figure 5-6
Index Timing

5.3.5 Ready

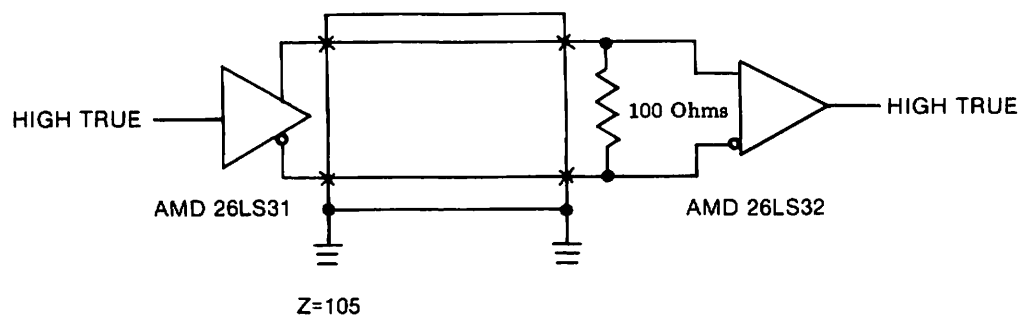
This signal will go true after power up if the DC voltages are within specification, the disks are at speed and the head position is recalibrated. If there is a fault in the power or the spindle speed control, READY will go false. It will not go true until the fault has cleared and the head position is recalibrated. The time after power on for READY to be true is 25 seconds maximum. No commands should be attempted while READY is false.

Although the motor speed is normally regulated to $\pm 0.1\%$ by the motor speed control circuitry, an independent audit is continually taken by the processor. If a speed variation greater than $\pm 2\%$ is detected, the processor will force READY false, lock the actuator, and stop the motor. Power up cycling is required to restart the drive.

5.4 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Two pairs of balanced signals are used for the transfer of data: WRITE DATA and READ DATA. Figure 5-7 illustrates the driver/receiver combination used in the drive for data transfer signals.



FLAT RIBBON OR TWISTED PAIR
MAXIMUM 20 FEET

NOTE: ANY EIA RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE.

Figure 5-7
Data Line Driver/Receiver Combination

5.4.1 MFM Write Data

This is a differential pair that defines the transitions to be written on the track. The transition of +MFM WRITE DATA line going more positive than the -MFM WRITE DATA line will cause a flux reversal on the track, provided WRITE GATE is active. This signal must be driven to an inactive state (+MFM WRITE DATA more negative than -MFM WRITE DATA) by the host system when in a read mode. **Write precompensation must not be used.**

5.4.2 MFM Read Data

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

5.4.3 Read/Write Timing

The timing diagram shown in Figure 5-8 depicts the necessary sequence of events (with associated timing restrictions) for proper read/write operation of the drive.

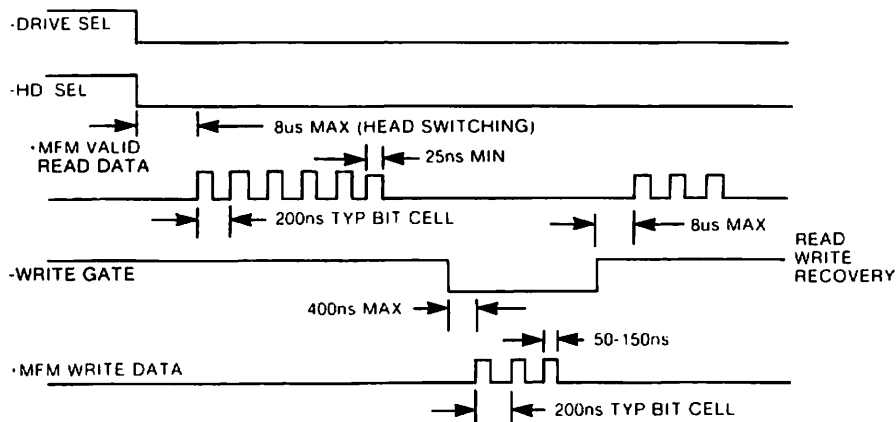


Figure 5-8
Read/Write Data Timing

5.5 Drive Selected

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 5-9. This signal will go active when the proper DRIVE SELECT line is active (see 5.6.1). The DRIVE SELECT X line at J1/P1 is activated by the host system.

5.6 Customer Options

Two options are implemented via J6 on the outer printed circuit board (Figure 5-9) near connector J1. These options are selected by means of a shunt block or dipswitch on early models, or by pins with a moveable jumper on current models.

5.6.1 Radial and Select

As shipped, pins 1-16 and 2-15 are always open. Drive Select jumpers on the shunt block are all shorted when shipped. Dipswitches and pins will have only Drive Select 1 selected. Outputs are not active until the drive is selected. Pin groups 1-16, 5-12, 6-11, 7-10, and 8-9 control the Drive Select function. The function desired is left shorted; the others must be opened.

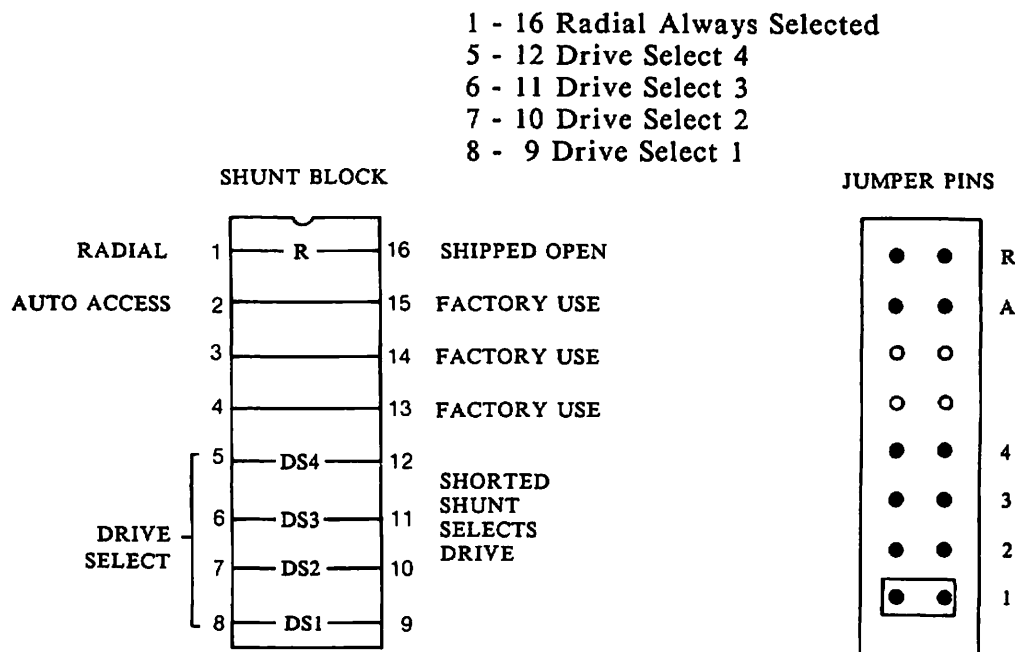


Figure 5-9
J6 Option Selection

5.6.2 Auto Access

As shipped, pins 2-15 are open. If shorted, the drive will perform a repeating series of predetermined seek operations with no signals required on the interface upon power up. This is normally used in the Priam factory to provide dynamic exercise of the drive during manufacturing burn-in. Auto Access is also referred to as "Self Test".

The following additional options are implemented by pads (J12) on the Data PCB near interface connector J2 (Figures 5-10 and 6-1).

5.6.3 Power Sequencing (PS)

A trace pad (J12-1) is available which, when shorted to DC ground, will inhibit starting of the DC spin motor, even if DC voltages are applied. When not connected to ground, the drive will sequence up normally. This can be used in multiple drive installations to minimize in-rush motor start currents on the +12V line. The function can be implemented by connection of an external wire, or bridging the trace to one of the unused pins on the interface connectors. Ground connections are available at J12.

5.6.4 Non-Multiplexed Index (NMI)

This trace pad (J12-5) can be connected to a spare pin on the J2 interface to provide an INDEX signal even when the drive is not selected. This signal is not driven by a line driver and may not meet cable length specifications.

5.6.5 Write Protect (WP)

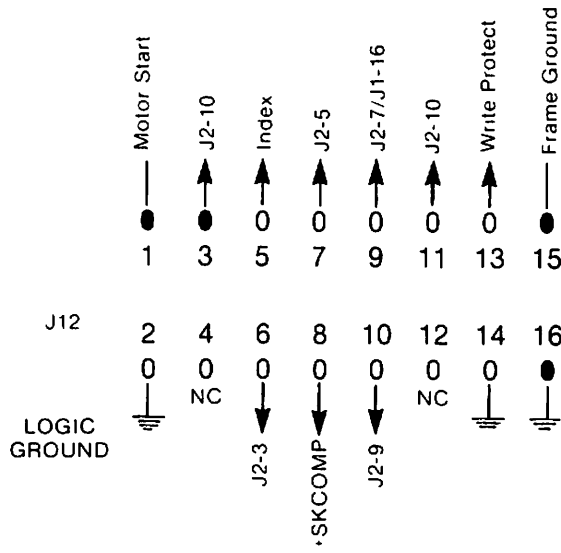
A pad (J12-13) is available which can be used to inhibit write operations on the drive when shorted to DC ground. If desired, an external switch can be connected to the pad, providing a manual write protect function. Ground connections are available at J12.

5.6.6 Radial Seek Complete (SC)

This trace pad (J12-8) can be connected to a spare pin on the J2 interface to provide a seek complete signal even if the drive is not selected. This is useful in some applications to enhance multiple seek overlap functions. This signal is not driven by a line driver and may not meet cable length specifications.

5.6.7 Grounding

As shipped, the printed circuit board DC logic ground is connected to the drive frame through the Head/Disk Assembly by a shorting plug installed in location J12, connecting pin 15 with pin 16. In some installations, disconnecting the PCB logic ground from the side frame may give better results, depending on overall system grounding and noise level.



2 rows of 8 holes each through square pads. Spacing .100 x .100 inches. Hole size .037 ± .003". Jumper pins in locations ● above can be easily connected together using a standard .100 jumper plug. As shipped, pins 15 and 16 are shorted.

**Figure 5-10
PCB Option Pads (J12)**

6 PHYSICAL INTERFACE

6.1 Physical Interface Overview

The electrical interface between the V100 and the host controller is via four connectors:

1. J1—Control signals (multiplexed)
2. J2—Read/write signals (radial)
3. J3—DC power input
4. J4—Frame ground

Refer to Figure 6-1 for connector locations.

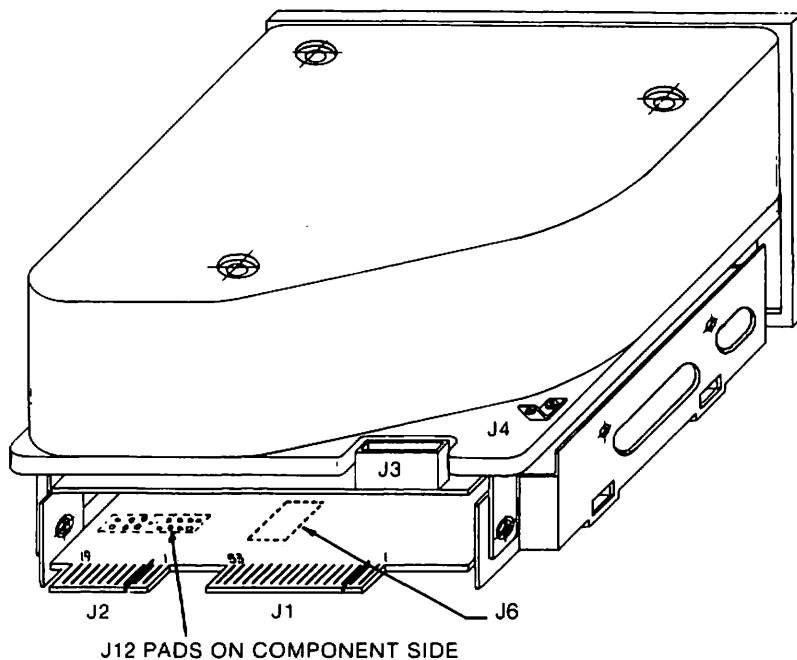


Figure 6-1
Interface Connector Physical Locations

6.2 J1/P1 Connector—Control Signals

Connection of J1 is through a 34-pin edge connector. The dimensions for the connector are shown in Figure 6-2. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is labeled. The recommended mating connector for P1 is AMP ribbon connector P/N 88373-3 or Molex 15-35-1341. All odd pins are ground.

A key slot is provided between pins 4 and 6.

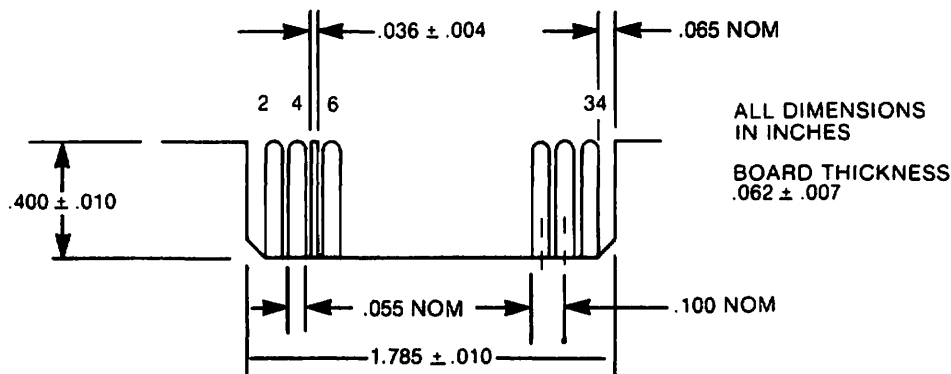


Figure 6-2
J1 Connector Dimensions

6.3 J2/P2 Connector—Data Signals

Connection to J2 is through a 20-pin edge connector. The dimensions for the connector are shown in Figure 6-3. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6, or Molex P/N 15-35-1201. Pin 2 is labeled.

A key slot is provided between pins 4 and 6.

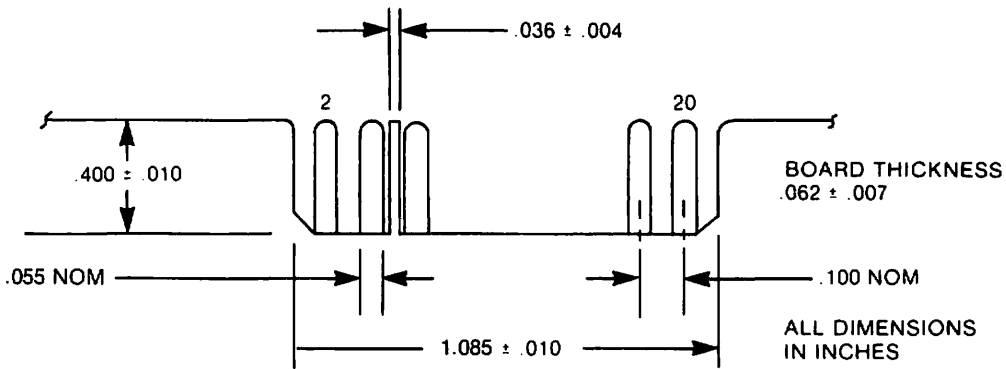


Figure 6-3
J2 Connector Dimensions

6.4 J3/P3 Connector—DC Power

DC power connector (J3) is a 4-pin AMP Mate-N-Lok connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4 (Strip) or P/N 61173-4 (Loose piece). J3 pins are numbered as shown in Figure 6-4.

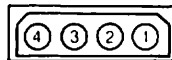


Figure 6-4
J3 Connector-Inner PCB Solder Side

Table 6-1
DC Power Requirements

J3 Connector	Current AMPS	
	MAX	TYP
Pin 4 — +5 Volts DC ±5% Pin 3 — +5 Volts Return	1.5	1.5
Pin 1 — +12 Volts DC ±10% Pin 2 — +12 Volts Return	4.5 *	SEE FIGURE 6-5

*Occurs only during power up, per curve. Figure 6-5

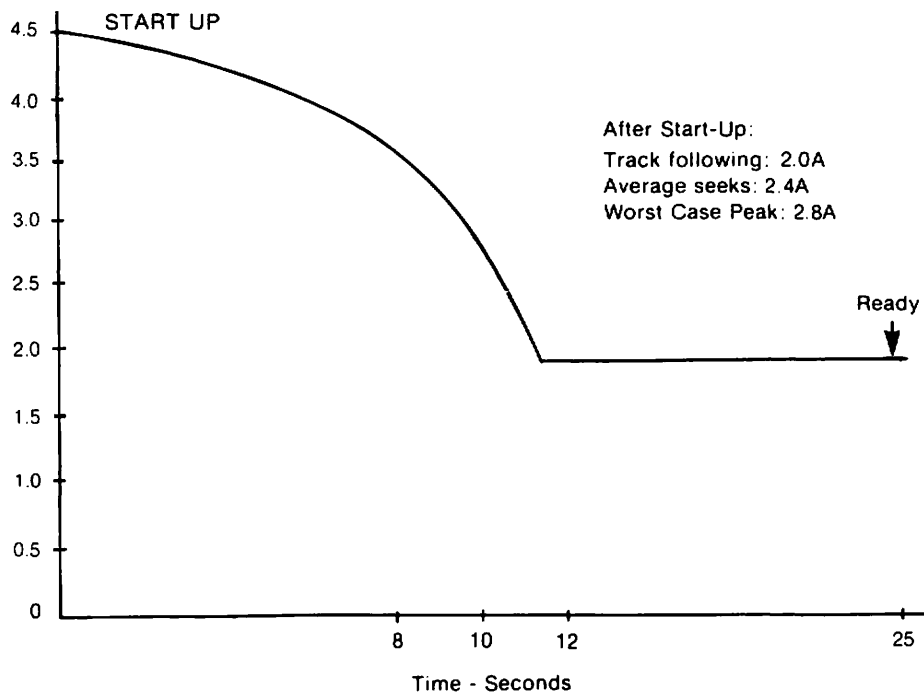


Figure 6-5
Typical & Maximum 12V Current Requirements

6.5 J4/P4 Frame Ground Connector

Faston AMP P/N 61761-2

Recommended mating connector AMP 62187-1.

If used, the hole in J4 will accommodate a wire of size 18AWG maximum.

6.6 Drive Physical Cabling

Figure 6-6 shows the Internal and External Cabling of the V100 Drive.

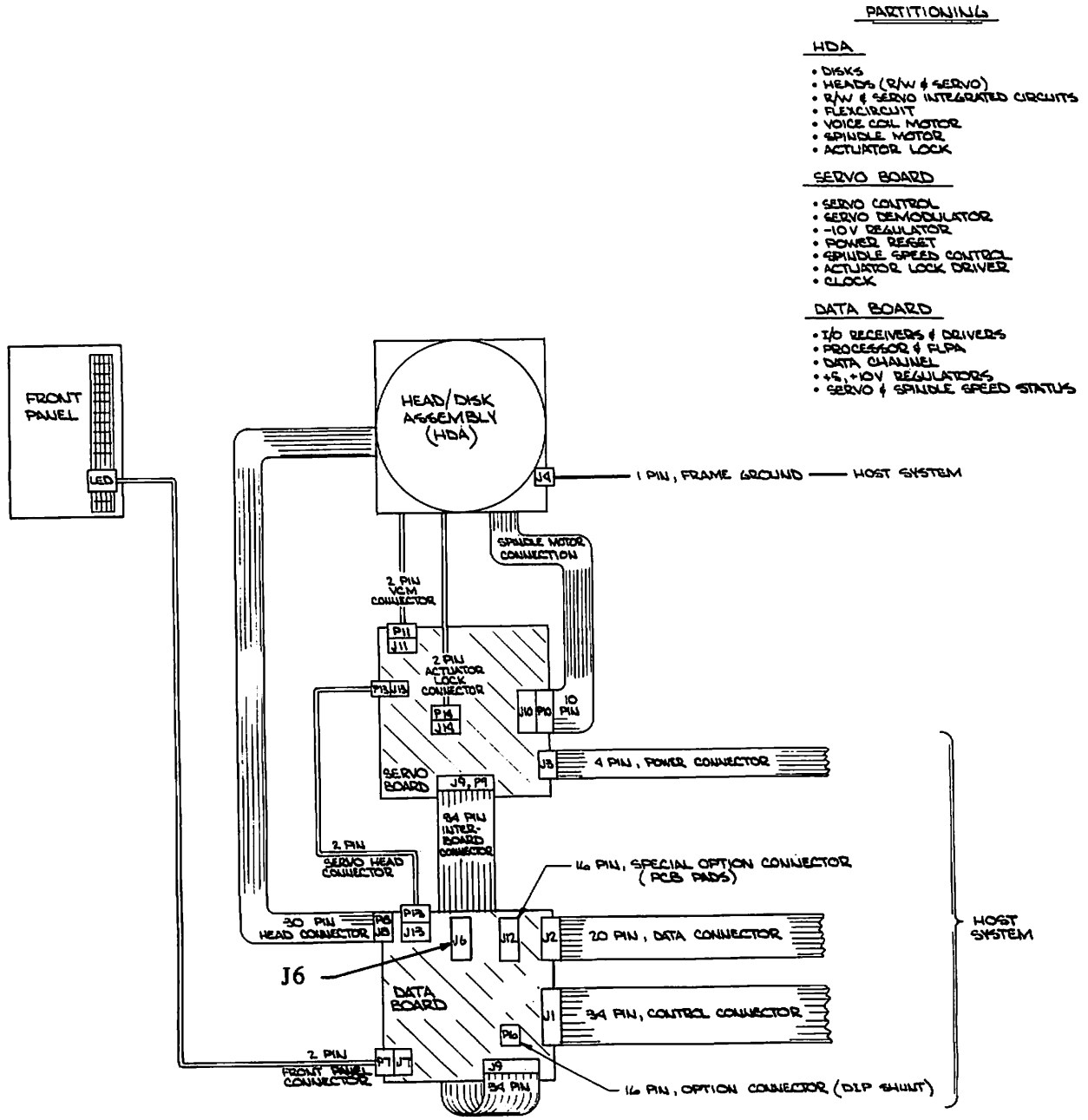


Figure 6-6
Drive Internal and External Cabling

7 PHYSICAL SPECIFICATIONS

7.1 Overview

This section describes the mechanical dimensions and mounting recommendations for the V100.

7.2 Mounting Orientation

Recommended orientation is either vertical on either side or horizontal with PCB down. In the final mounting configuration, ensure that operation of the four shock mounts is not inhibited.

7.3 Mounting Holes

Eight mounting holes, four on the bottom and two on each side, are provided for mounting the drive in an enclosure. The size and location of these holes, shown in Figure 7-1, are identical to the industry standard minifloppy drive.

7.4 Physical Dimensions

Overall height/width/depth and other key dimensions are shown in Figures 7-1 and 7-2. As in the case of the mounting holes, the dimensions are identical to the minifloppy, allowing a direct physical replacement.

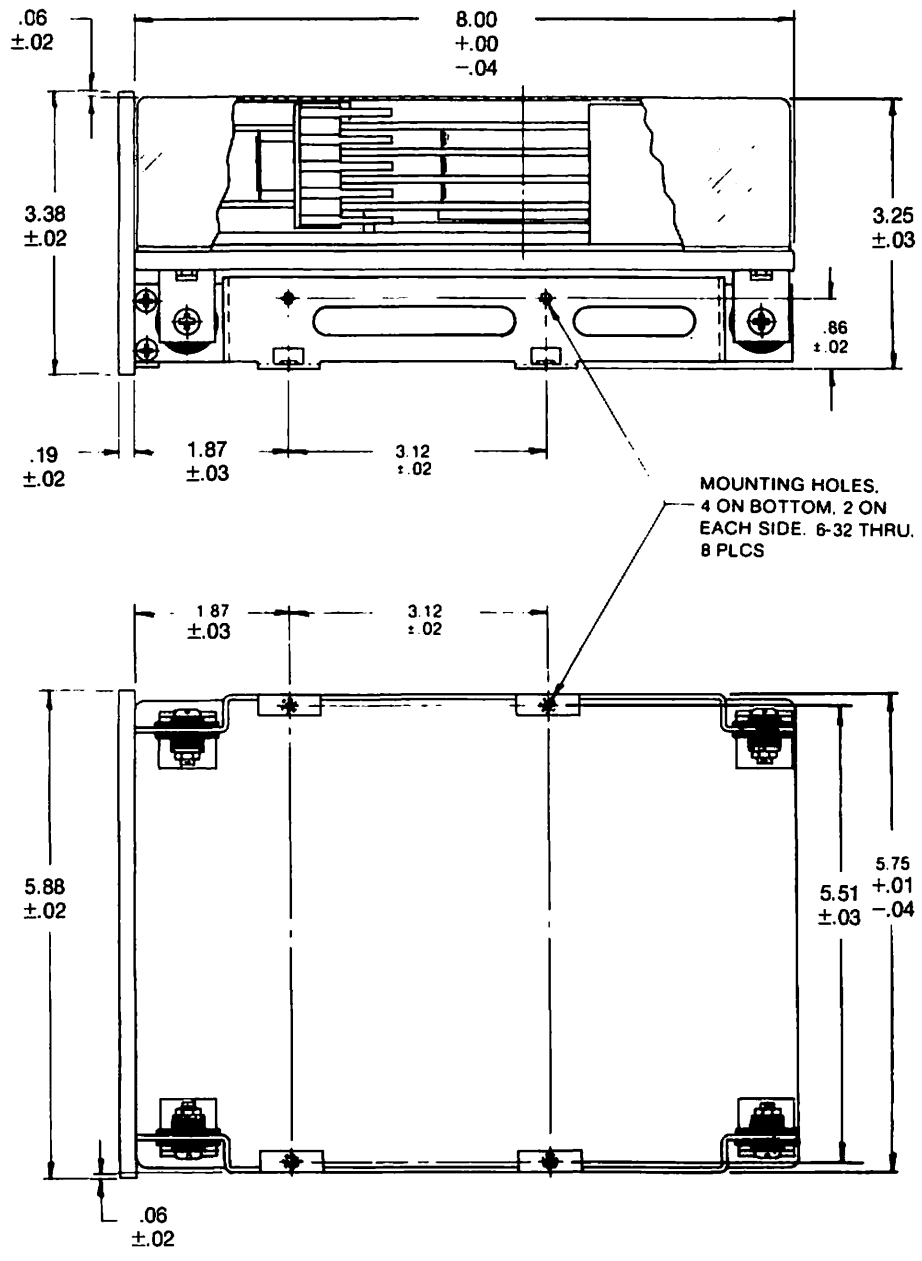


Figure 7-1
Mounting Physical Dimensions

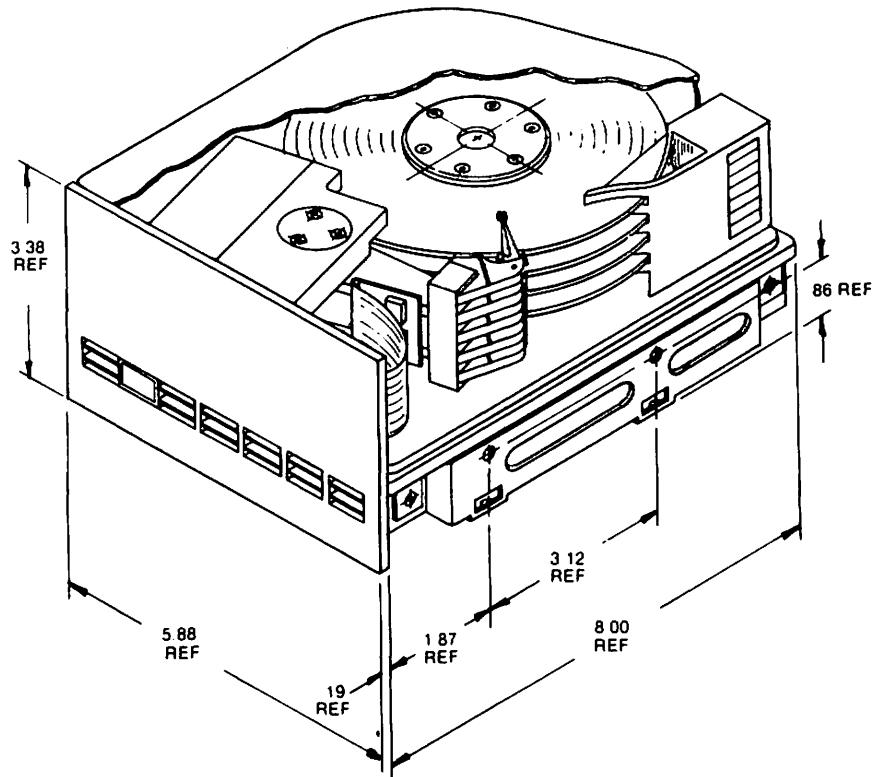


Figure 7-2
Overall Physical Dimensions

7.5 Faceplate

The faceplate is for cosmetic purposes only, serving no structural requirement, and can be easily removed. Remove the four screws adjacent to the side frames and disconnect the light emitting diode. The recommended mating plug for J7 is AMP P/N 640442-2.

7.6 Shipping Requirement

The actuator is automatically locked whenever the drive is powered down. When shipped as a single unit, the original shipping container should be used. The container is designed to ensure no drive damage will occur if the container is dropped from a height of 42" or less.

8 DATA PCB BLOCK DIAGRAM (ALL MLC LEVELS)

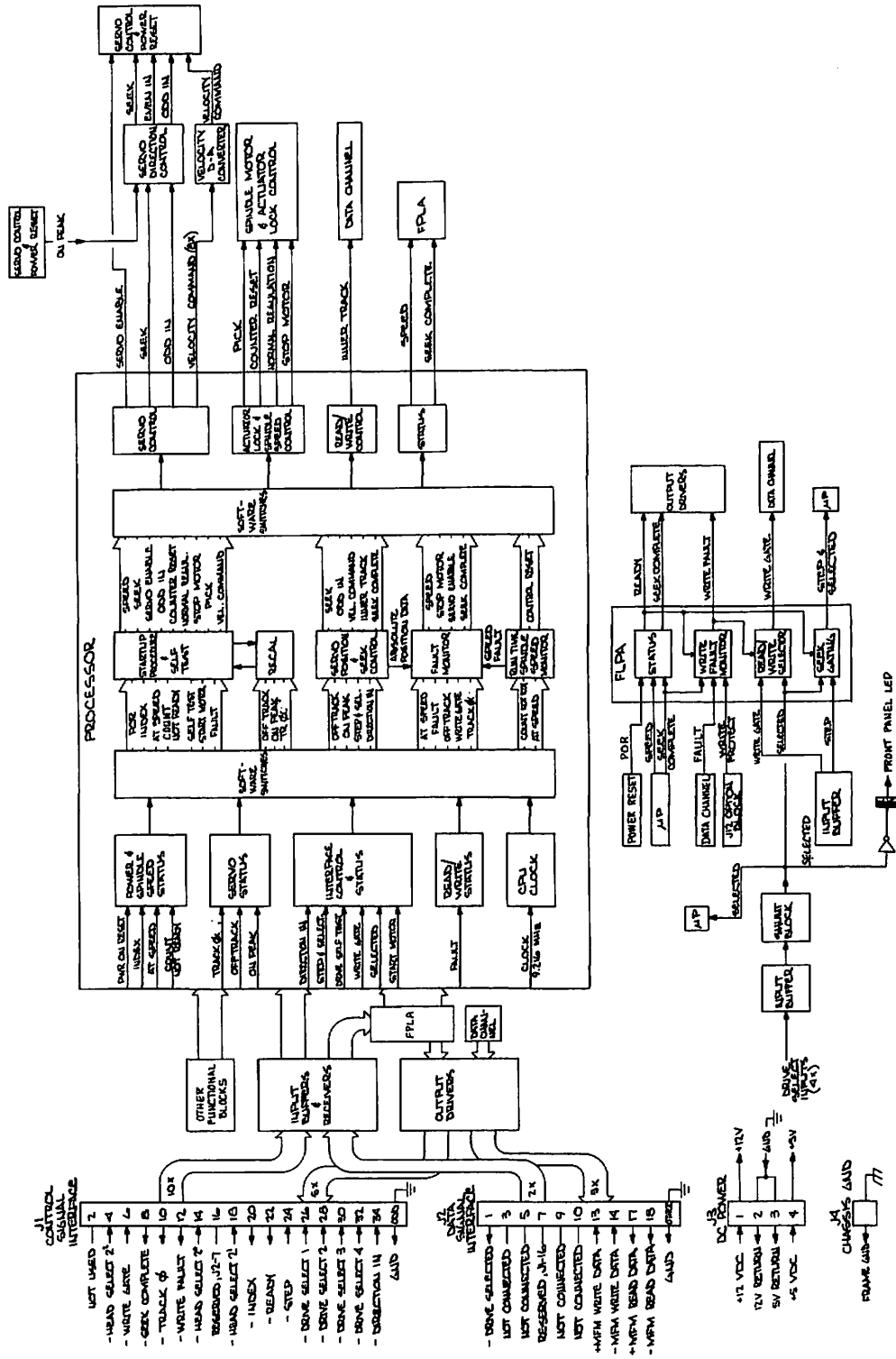


Figure 8-1
Data PCB Block Diagram (Page 1 of 2)

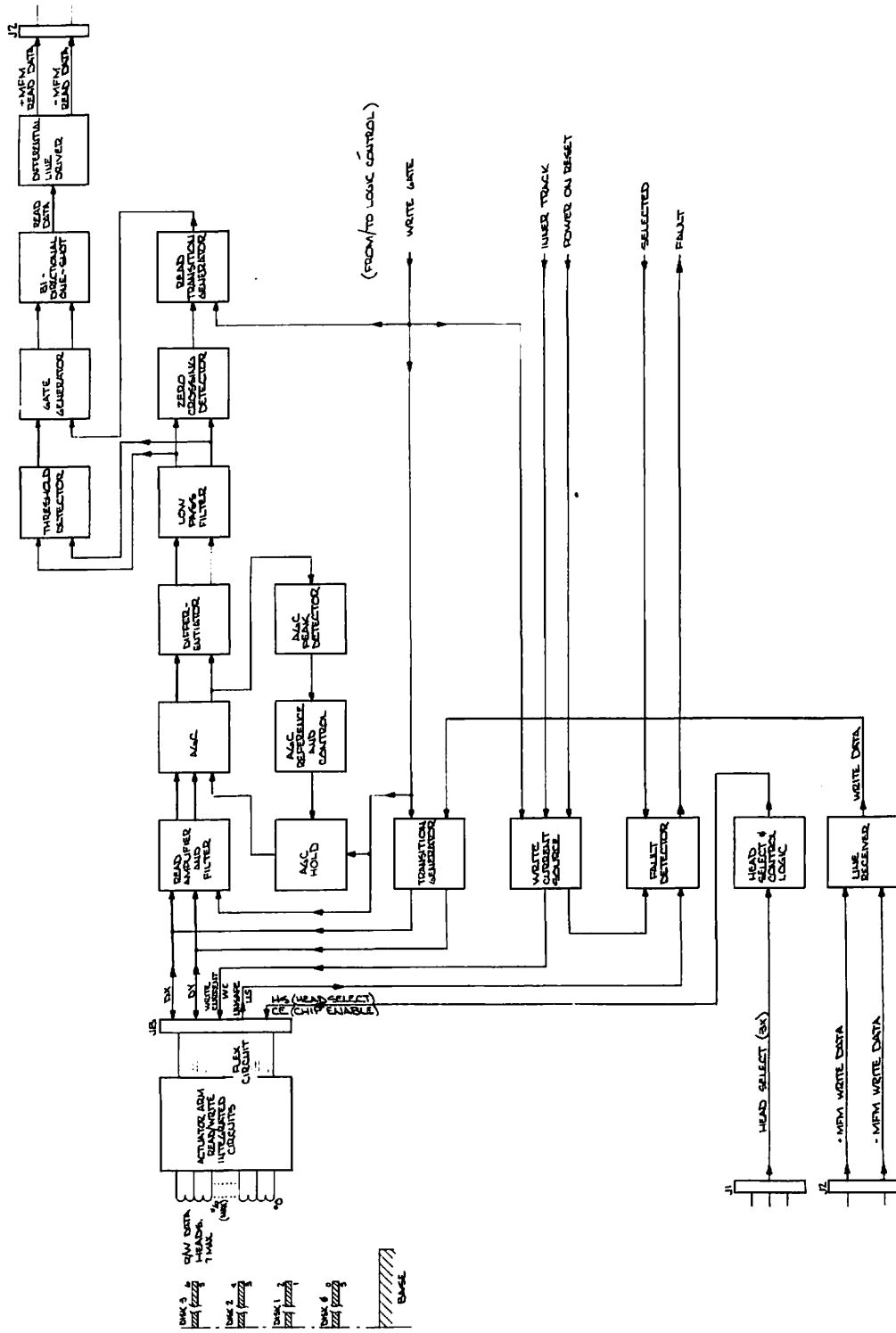


Figure 8-1
Data PCB Block Diagram (Page 2 of 2)

9 SERVO PCB BLOCK DIAGRAM (ALL MLC LEVELS)

SERVO PCB BLOCK DIAGRAM

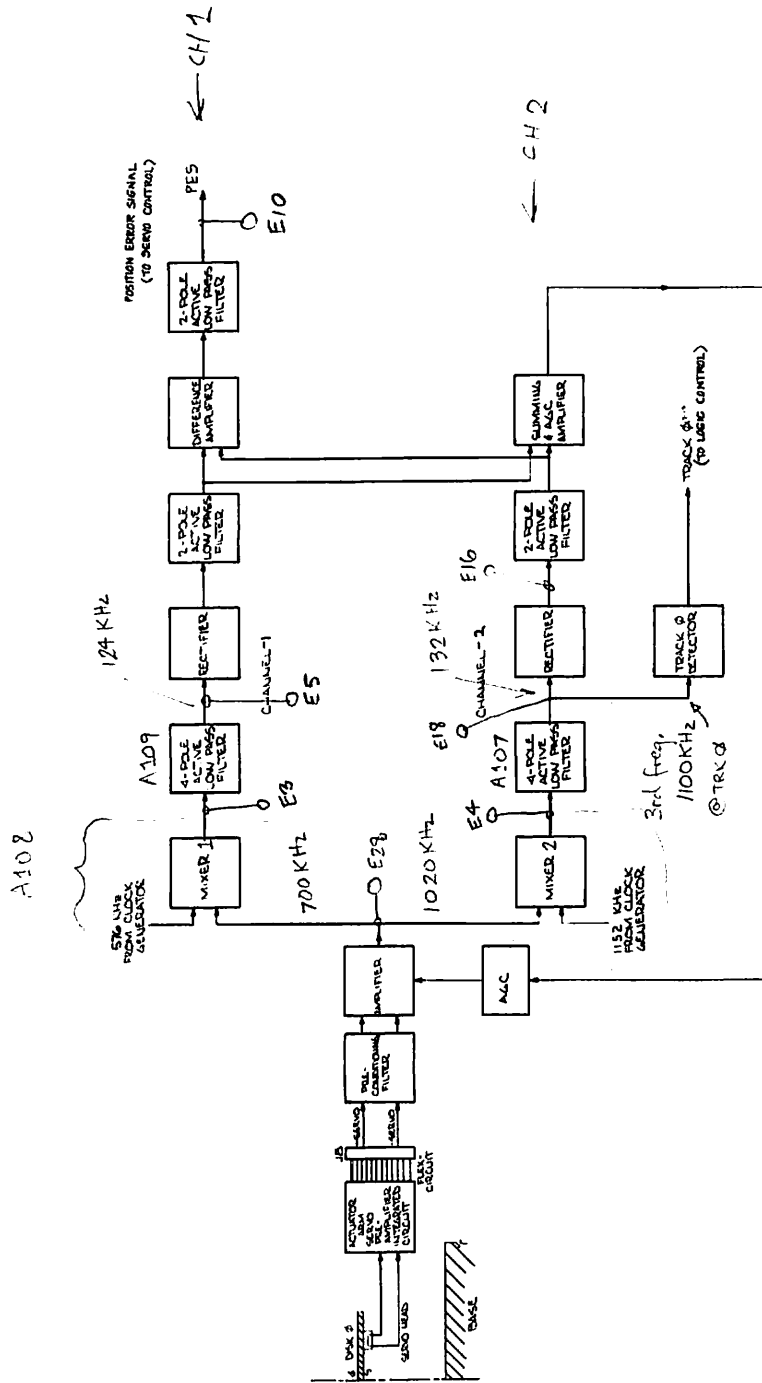


Figure 9-1
Servo PCB Block Diagram (Page 1 of 3)

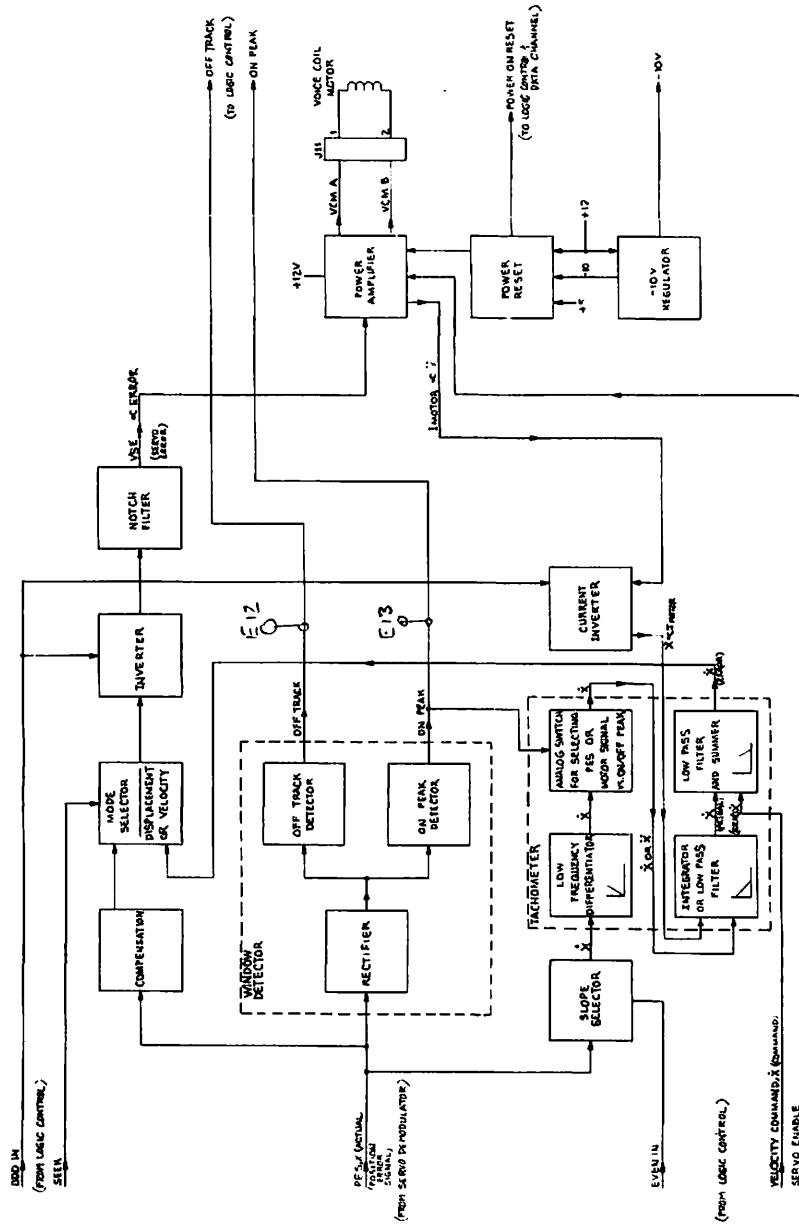


Figure 9-1
Servo PCB Block Diagram (Page 2 of 3)

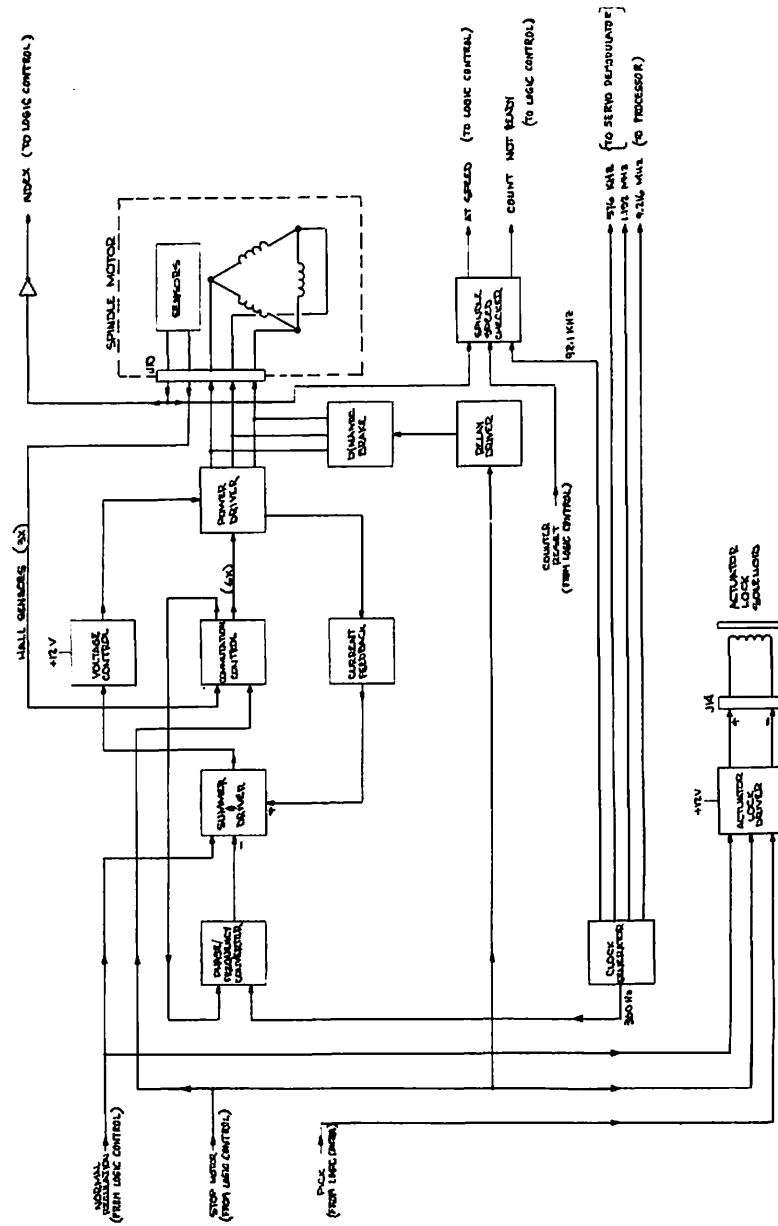


Figure 9-1
Servo PCB Block Diagram (Page 3 of 3)

10 MAINTENANCE/REPAIR (ALL MLC LEVELS)

10.1 Overview

The V100 Disk Drive does not require preventive maintenance. If field maintenance or repair is required, certain restrictions apply. Primarily, the environmentally sealed Head/Disk Assembly (HDA) must not be opened. Priam considers any existing warranties invalid if the HDA has been tampered with.

10.2 Removal of Parts Not Requiring a Clean Room Environment

Note: When working with the Priam V100 disk drive, place it on a soft padded surface.

10.2.1 Front Cover

Tools Required: 5/64" Hex Allen Wrench

- 1) Remove (4) 6-32×1/4" mounting screws which hold the Front Cover to the Side Frames.
- 2) Disconnect P7 from J7.
- 3) Remove the Front Panel.
- 4) To reinstall, reverse the above procedure.

10.2.2 Side Frames

Tools Required: 5/64" Hex Allen Wrench/or Phillips screwdriver

- 1) Remove the Front Cover (Procedure 10.2.1).
- 2) Remove (4) 6-32×1/2" screws holding the two separate Side Frames.
- 3) Remove each Side Frame, noting their orientation.
- 4) To reinstall, reverse the above procedure.

Note: All MLC levels – torque all Side Frame screws to 10 in.-lb.

10.2.3 Data PCB

Tools Required: 5/64" Hex Allen Wrench/or Phillips screwdriver

- 1) Remove the Front Cover (Procedure 10.2.1).
- 2) Remove the Side Frames (Procedure 10.2.2).
- 3) Disconnect P8 from J8.
- 4) Disconnect P13 from J13.
- 5) Remove (4) screws from data PCB.
- 6) Raise the Data PCB away from the heat sinks on the Servo PCB.
- 7) Remove P9 from J9 on the Servo PCB connecting the two PCBs together.
- 8) To reinstall, reverse the above procedure.

Note: MLC 1.X - when installing screws, use LOCTITE brand "small thread locker" and torque screws to 2 in.-oz.

10.2.4 Servo PCB

Tools Required: 1/4" Hex Nut Driver

- 1) Remove the Data PCB (Procedure 10.2.3).
- 2) Disconnect P11 from J11.
- 3) Disconnect P14 from J14.

- 4) Loosen and remove the (4) hex standoffs (MLC 1.X only). For MLC 2.X, remove the red O-rings and plastic standoffs.
- 5) Raise the Servo PCB, ensuring that the PCB does not hang up on the motor fan blades (or actuator lock solenoid in the case of MLC1.X).
- 6) Disconnect P10 from J10.
- 7) Remove the Servo PCB insulator.
- 8) To reinstall, reverse the above procedure.
Note: MLC 1.X only - when installing standoffs, use LOCTITE brand "small thread locker" and torque standoffs to 2 in.-oz.

10.3 Repair and Adjustments

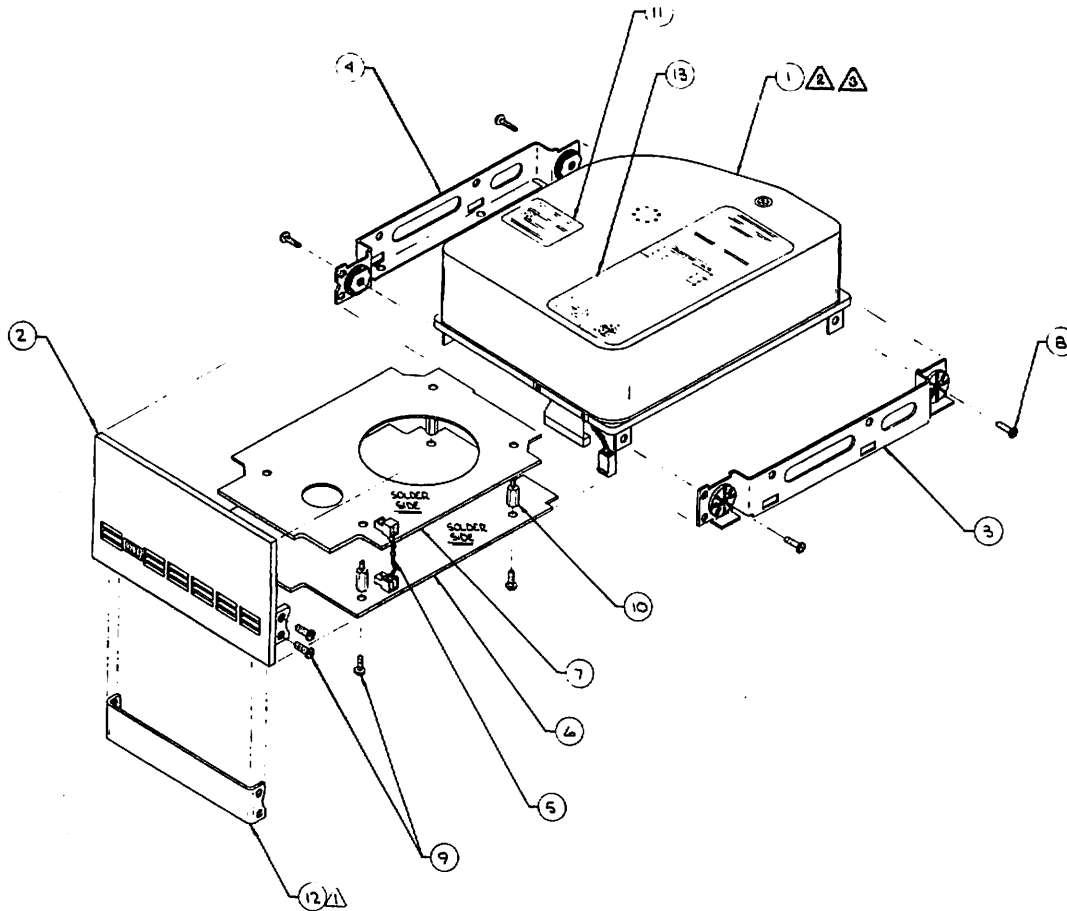
10.3.1 Data PCB

Replacement of the Data PCB requires no adjustments to be performed.

10.3.2 Servo PCB

Replacement of the Servo PCB requires no adjustments to be performed. All adjustable pots on the Servo PCB are factory set.

10.4 Spare Parts List, Figure 10-1 (MLC-1.X)



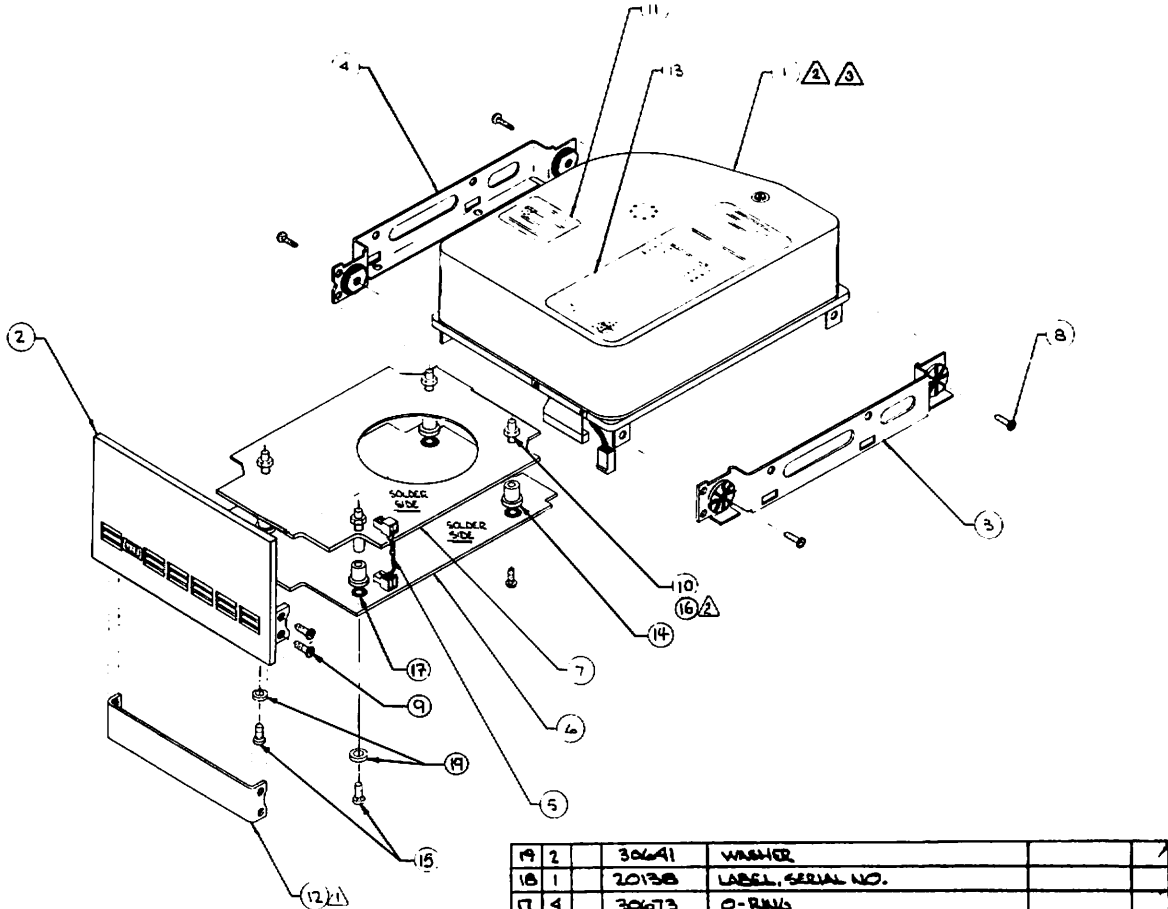
NOTES

- ⚠ OPTIONAL: TO BE USED AT CUSTOMER REQUEST IN PLACE OF ITEM 2.
- ⚠ P/N 10033 HDA V130
P/N 10032 HDA V150
P/N 10009 HDA V170
- ⚠ SPECIFY MLC 1.X WHEN ORDERING AN HDA ASSEMBLY

13	1	20115	ERROR MAP		
12	1	20109	CHASSIS BRACKET, FRONT		
11	1	20090	LABEL		
10	4	30286	STANDOFF, .530" 6-32 M/F		5.0
9	B	30147	SCREW, 6-32 x 1/4 ZINC-PLT BHCS		5.0
8	4	30576	SCREW, 6-32 x 3/8 ZINC-PLT BHCS		10.0
7	1	10042	PCB ASM, SERVO, S.O.		
6	1	10041	PCB ASM, DATA, S.O.		
5	1	10040	CABLE ASM, SERVO HEAD		
4	1	10036	CHASSIS ASM, RIGHT		
3	1	10035	CHASSIS ASM, LEFT		
2	1	10034	FRONT PANEL ASM		
1	1	10009	HEAD/DISK ASM (HDA) V170		
<small> P/N 10033 HDA V130 P/N 10032 HDA V150 P/N 10009 HDA V170 </small>					
PARTS LIST					

Figure 10-1
Spare Parts List/Assembly (MLC-1.X)

10.5 Spare Parts List, Figure 10-2 (MLC-2.X)



- NOTES**
- △ OPTIONAL: TO BE USED AT CUSTOMER REQUEST IN PLACE OF ITEM 2.
 - △ APPLY TO THREADS OF ITEM 10
 - △ P/N 10058 HDA V130
P/N 10057 HDA V150
P/N 10056 HDA V170
P/N 11001 HDA V185
 - △ SPECIFY MLC 2.X WHEN ORDERING AN HDA ASSEMBLY

19	2	30641	WASHER		
18	1	20138	LABEL, SERIAL NO.		
17	4	30673	O-RING		
16	AR	30896	ADHESIVE, THREADLOCKING		
15	4	30674	SCREW, 4-40 x 1/8 ZINC-PLT TIPS		4.0
14	4	20514	SPACER, PCB		
13	1	20115	ERROR MAP		
12	1	20109	CHASSIS BRACKET, FRONT		
11	1	20070	LABEL		
10	4	20516	STANDOFF, PCB		6.0
9	4	30417	SCREW, 6-32 x 1/4 ZINC-PLT BHCS		3.0
8	4	30658	SCREW, 6-32 x 3/8 ZINC-PLT PHPS		10.0
7	1	10061	PCB ASM, SERVO, HYBRID		
6	1	10060	PCB ASM, DATA, HYBRID		
5	1	10040	CABLE ASM, SERVO HEAD		
4	1	10036	CHASSIS ASM, RIGHT		
3	1	10035	CHASSIS ASM, LEFT		
2	1	10034	FRONT PANEL ASM		
1	1	10009	HEAD/DISK ASM (HDA) V170		

Figure 10-2
Spare Parts List/Assembly (MLC-2.X)

11 V100 TEST POINTS (MLC 1.X)

11.1 Data PCB Test Points (MLC-1.X)

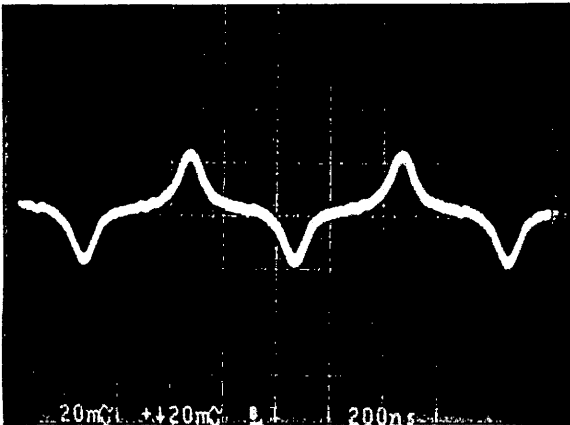
1. TP E6 and E9 - Read Data from Preamp
2. TP E7 and E8 - Output of Read Amplifier
3. TP E4 and E5 - Output of AGC
4. TP E1 and E2 - Output of Differentiator
5. TP U22 Pin 2 - Output from Peak Detector
6. TP U22 Pin 3 - Output from Zero Crossing Detector
7. TP U15 Pin 3 - Read Data
8. TP U32 Pin 3 - Write Data

Note: Test Equipment

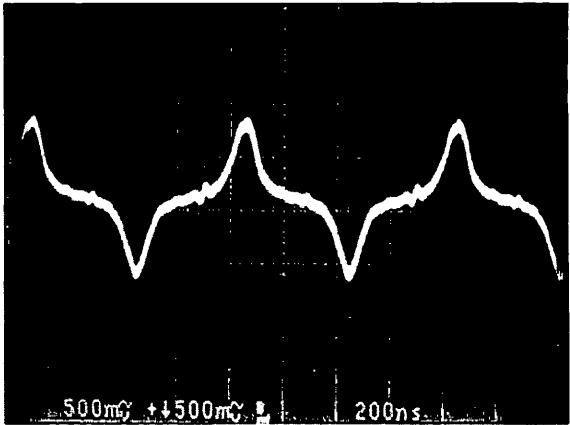
1. Tektronix Scope 7704 or equivalent
2. Tektronix Scope Probes P6201 or equivalent

Figure 11-1
Data PCB Test Point Descriptions

1. E6 and E9 (1F DATA PATTERN)

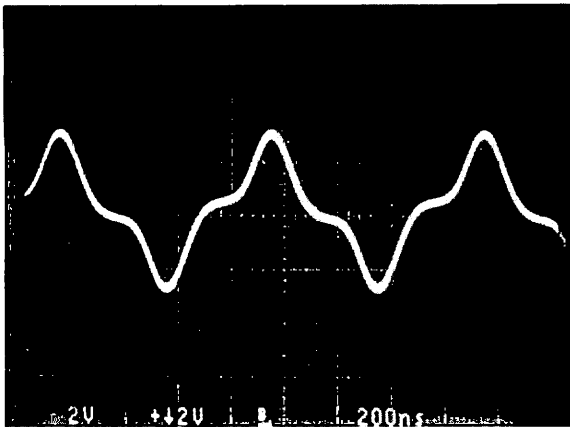


2. E7 and E8 (1F DATA PATTERN)



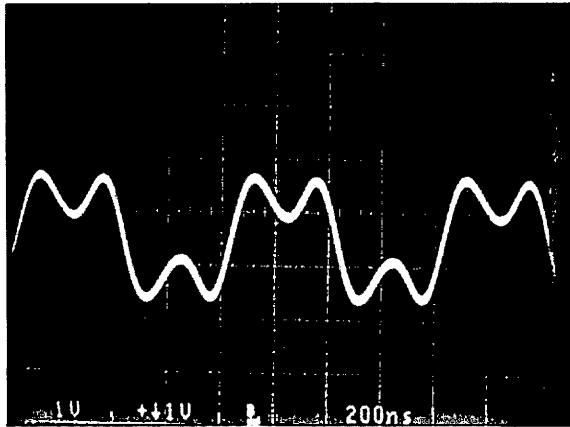
800 MV
TO 2.2 V

3. E4 and E5 (1F DATA PATTERN)



Typical
4 to 6 Volts
Differential

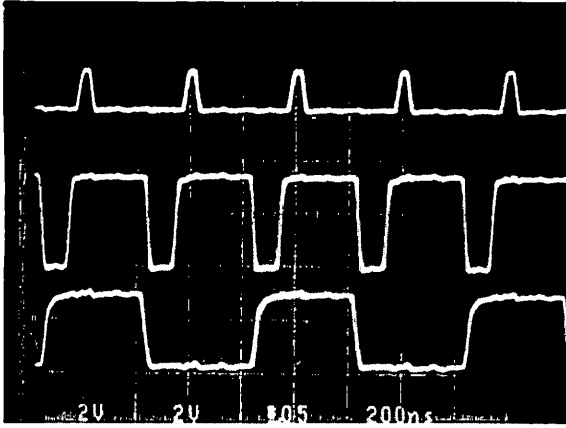
4. E1 and E2 (1F DATA PATTERN)



1.8 to 2.4 V
Typical Differential

Figure 11-2
Test Point Outputs

5. PEAK DETECT U22-2, ZEROS
CROSSING U22-3 READ DATA
U15-3 (1F DATA PATTERN)



6. WRITE DATA U32-3
(1F DATA PATTERN)

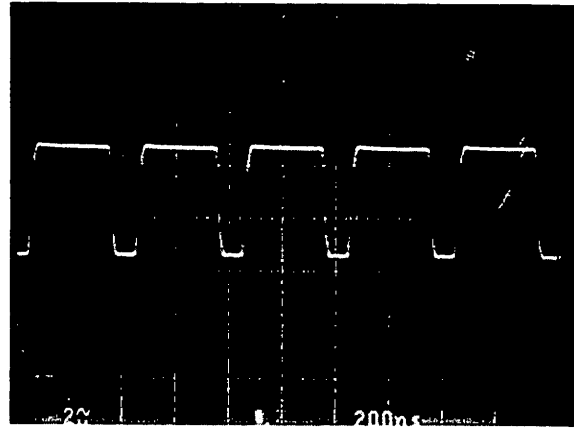


Figure 11-2 (continued)
Test Point Outputs

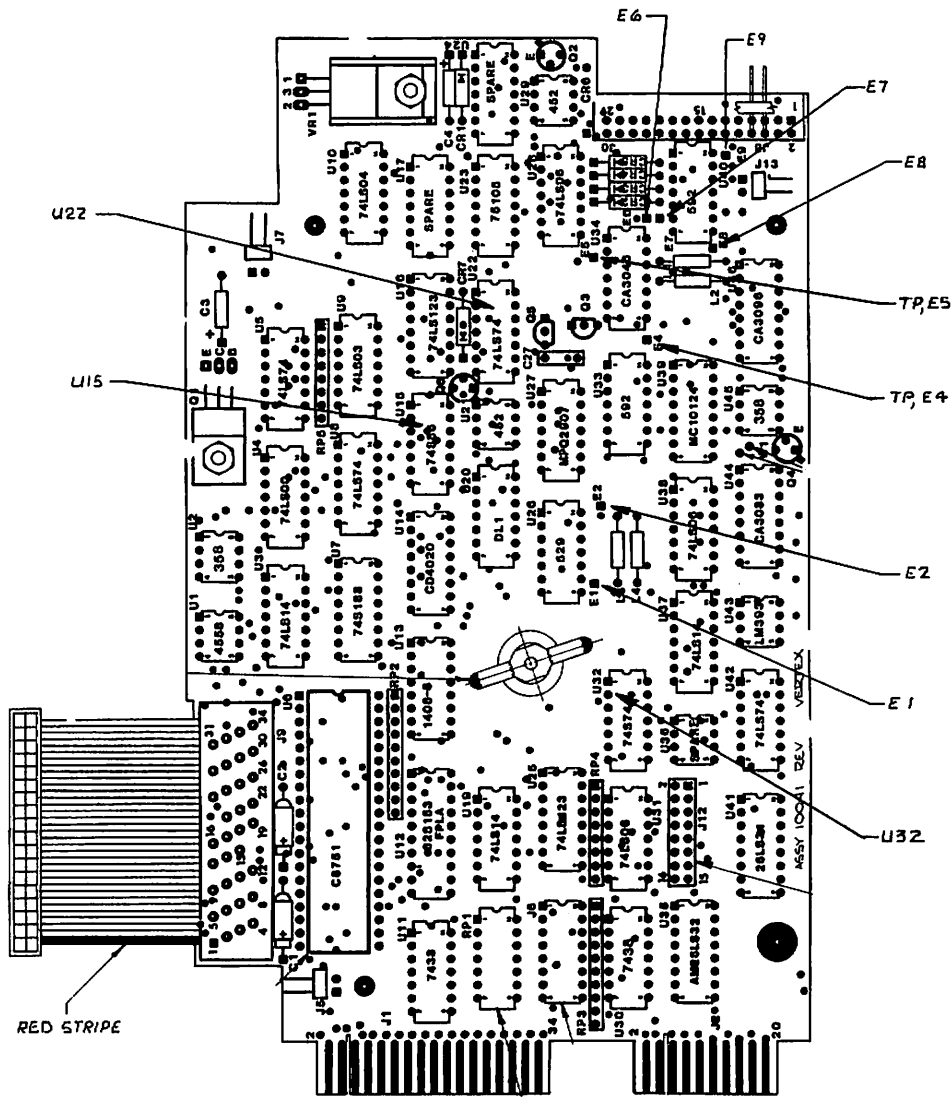


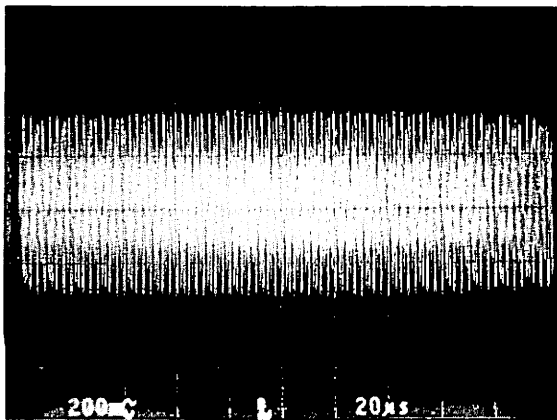
Figure 11-3
MLC 1.X Test Point Locations
Data PCB

11.2 Servo PCB Test Points (MLC-1.X)

1. TP 1 - Servo Head Data Output
2. TP 2 - Channel 1 Mixer Output
3. TP 3 - Channel 2 Mixer Output
4. TP 4 - Low Pass Filter Output Ch 1
5. TP 5 - Low Pass Filter Output Ch 2
6. TP 6 - Track \emptyset Detect Output
7. TP 9 - Channel 2 Rectifier Output
8. TP 10 - Channel 1 Rectifier Output
9. TP 11 - Position Error Signal Servo
10. TP 14 - Off Track Detect Output
11. TP 15 - On Peak Output Seeking
12. TP 16 - Velocity Error Signal
13. TP 17 - Velocity Command
14. TP 19 - Servo Error
15. TP 20 - Motor Speed Control Oscillator Signal

Figure 11-4
Servo PCB Test Point Descriptions

1. TP1 SERVO HEAD DATA OUTPUT
TRACK FOLLOWING



2. TP2 CHANNEL 1 MIXER
OUTPUT TRACK FOLLOWING

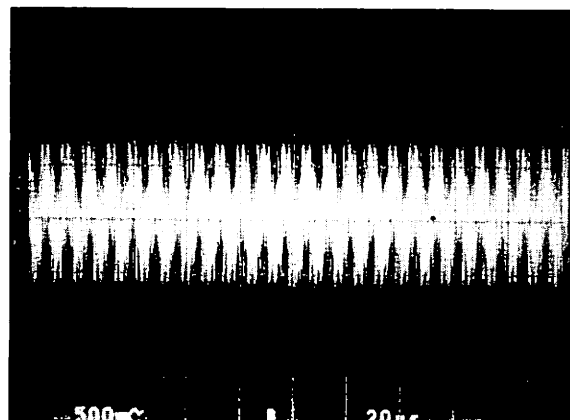
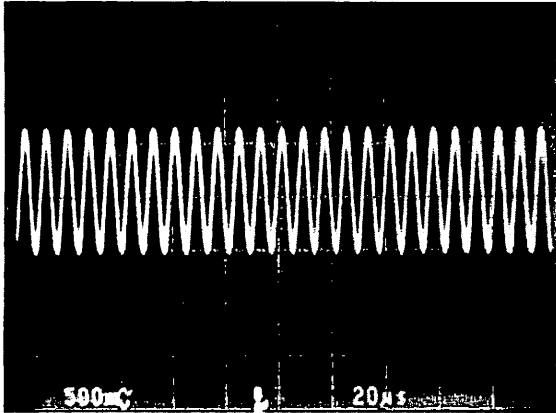
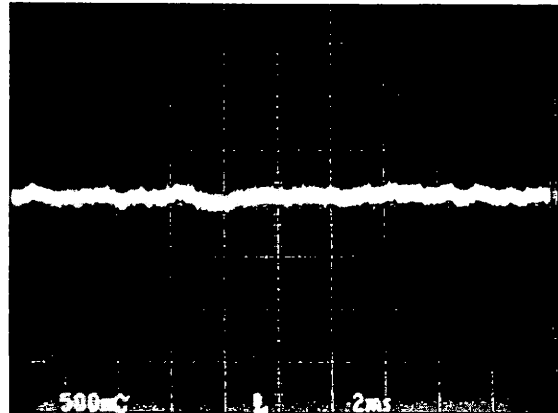


Figure 11-5
Test Point Outputs

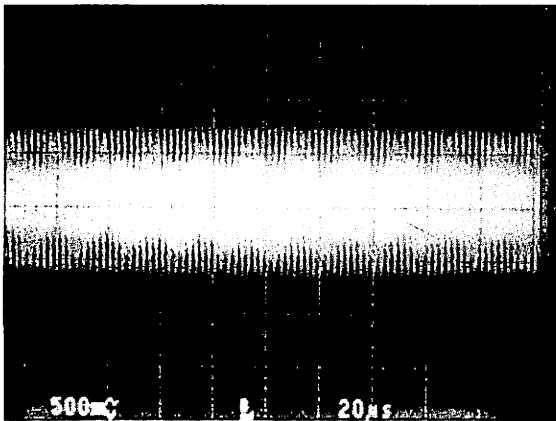
4. TP4 CHANNEL 1 LOW PASS
OUTPUT TRACK FOLLOWING



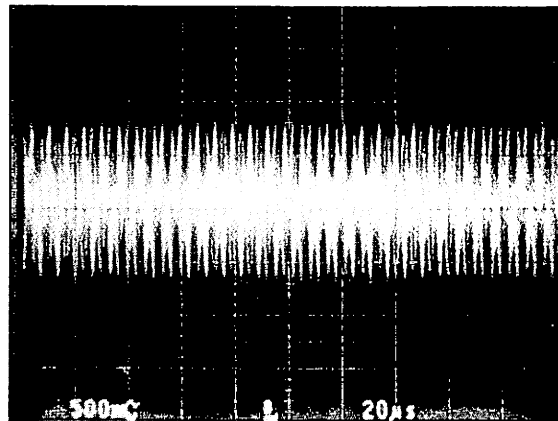
5. TP10 CHANNEL 1 RECTIFIER
OUTPUT TRACK FOLLOWING



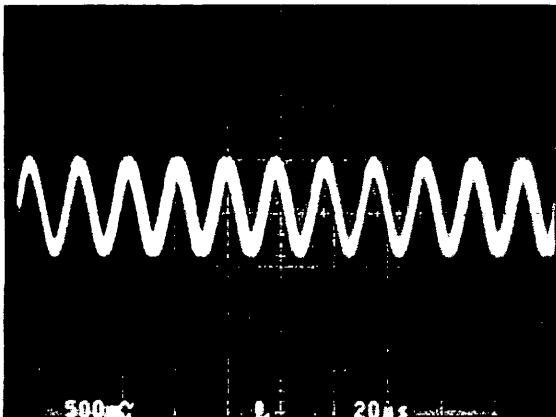
3. TP3 CHANNEL 2 MIXER OUTPUT
AT TRACK 0, TRACK FOLLOWING



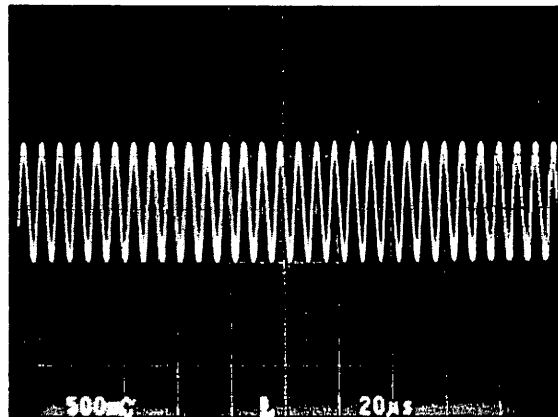
AT TRACK 1,
TRACK FOLLOWING



TP5 CHANNEL 2 LOW PASS FILTER
OUTPUT AT TRACK 0,
TRACK FOLLOWING



AT TRACK 1,
TRACK FOLLOWING

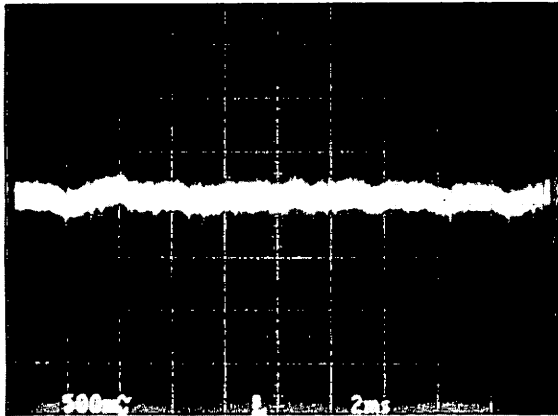


TP6 IS LOW

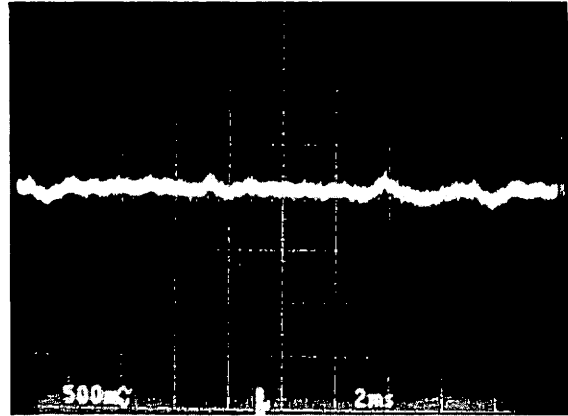
TP6 IS HIGH

Figure 11-5 (continued)
Test Point Outputs

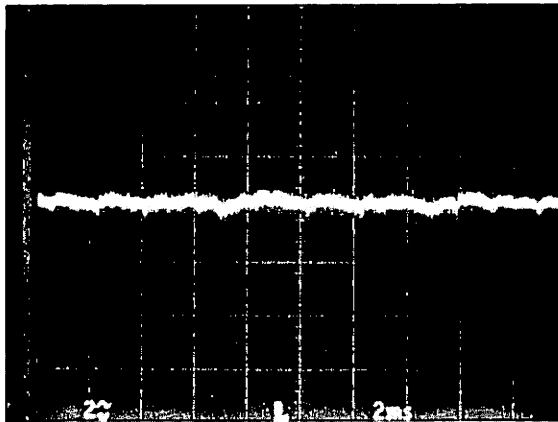
TP9 CHANNEL 2 RECTIFIER
OUTPUT AT TRACK 0,
TRACK FOLLOWING



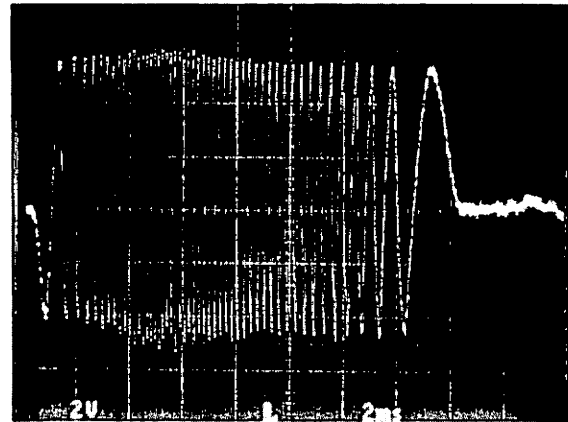
AT TRACK 1,
TRACK FOLLOWING



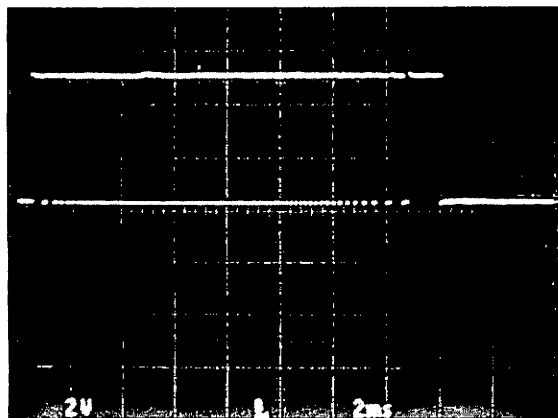
TP11 POSITION ERROR SIGNAL (PES)
TRACK FOLLOWING



PES SIGNAL 100
TRACK SEEK



TP14 OFFTRACK DETECT
OUTPUT 100 TRACK SEEK



TP15 ON PEAK DETECT
OUTPUT 100 TRACK SEEK

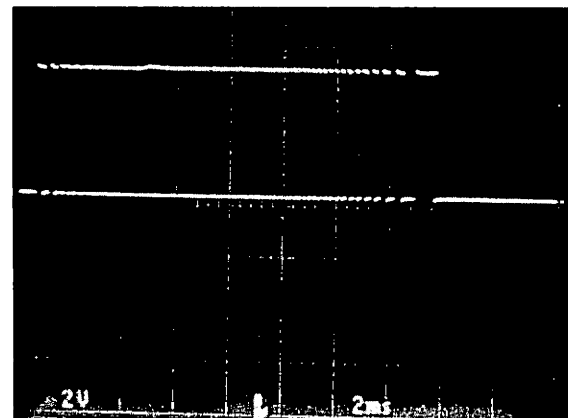
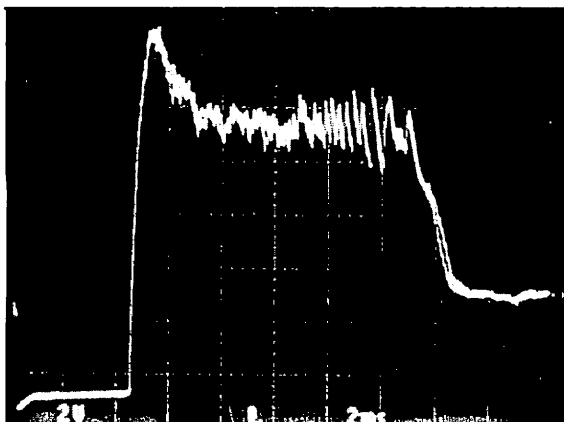
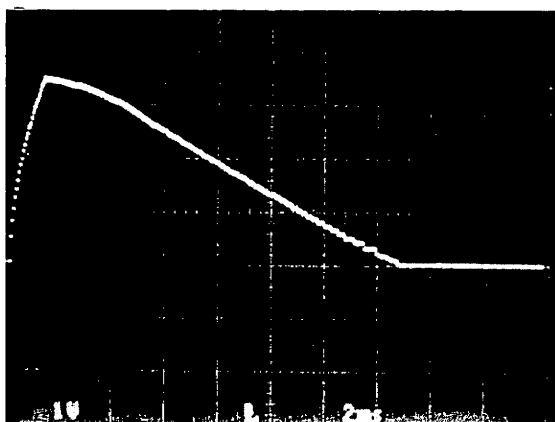


Figure 11-5 (continued)
Test Point Outputs

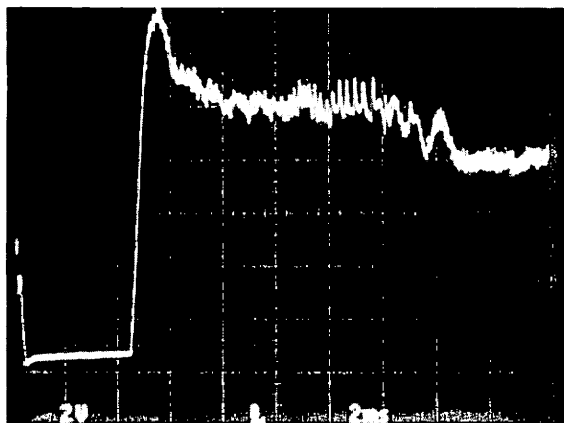
TP16 VELOCITY ERROR
SIGNAL 100 TRACK SEEK



TP17 VELOCITY COMMAND
100 TRACK SEEK



TP19 SERVO ERROR
SIGNAL 100 TRACK SEEK



TP20 MOTOR SPEED CONTROL
OSCILLATOR OUTPUT 360 Hz

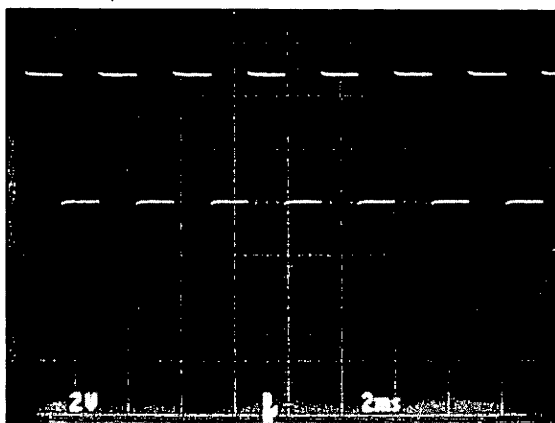


Figure 11-5 (continued)
Test Point Outputs

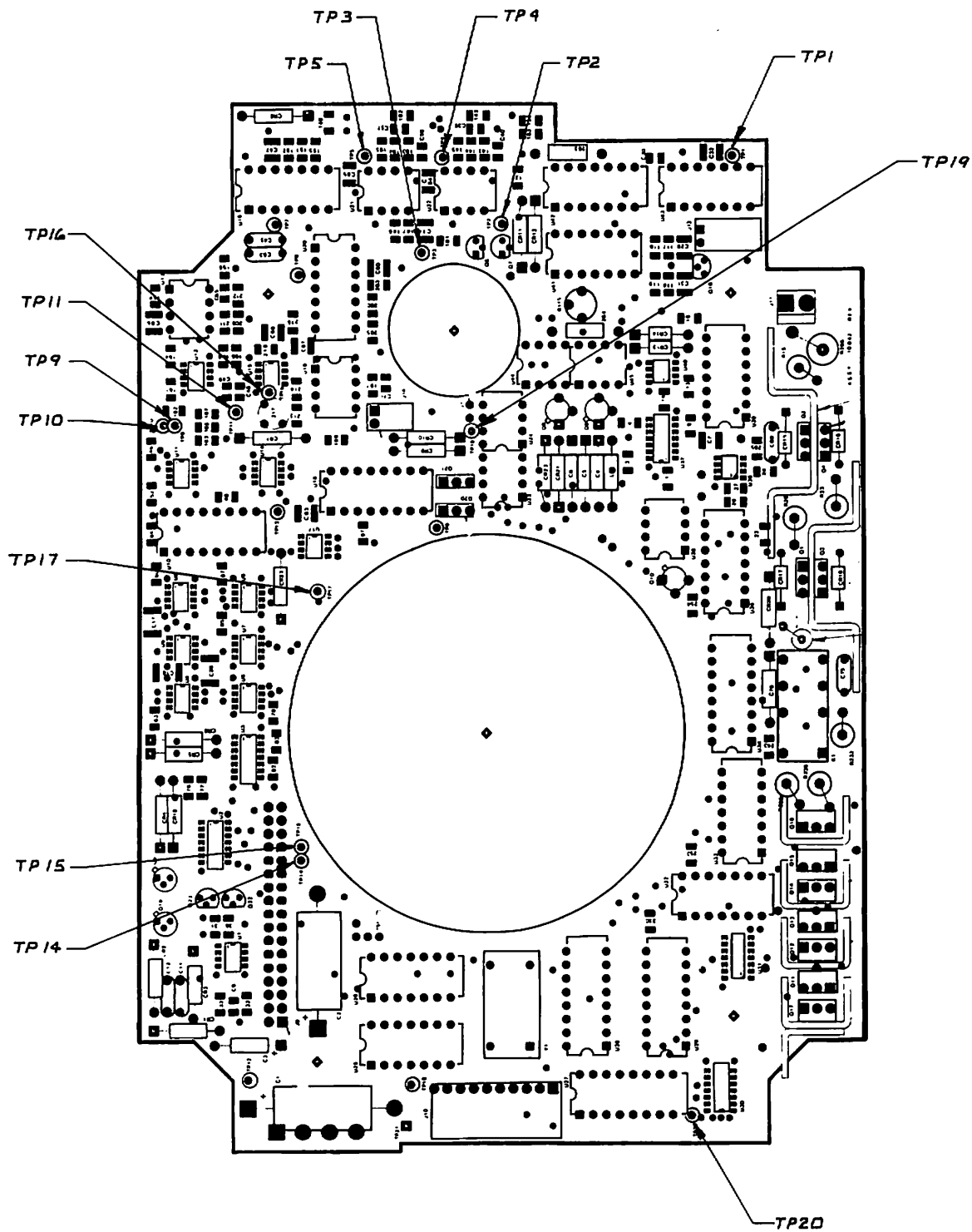


Figure 11-6
MLC 1.X Test Point Locations
Servo PCB

12 V100 TEST POINTS (MLC 2.X)

12.1 Data PCB Test Points (MLC 2.X)

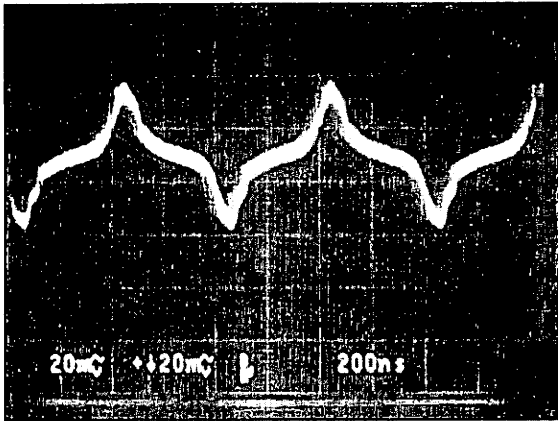
1. TP E12 and E8 - Read Data from Preamp
2. TP E6 - Output of Read Amplifier
3. TP E7 - Output of AGC
4. TP E4 and E5 - Output of Differentiator
5. U18 Pin 38 - On Peak Detector
6. TP U14 Pin 11 - Zero Crossing Detector
7. TP U14 Pin 3 - Read Data

Note: Test Equipment

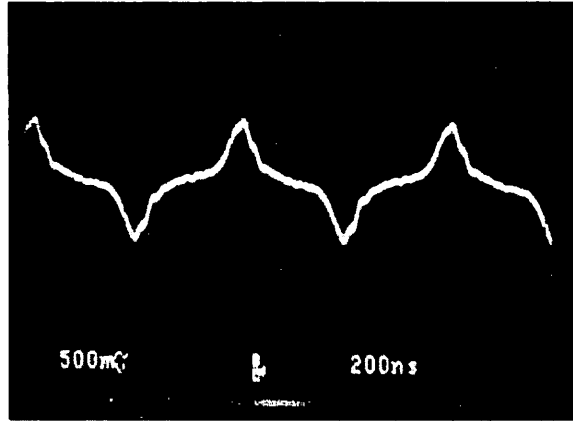
1. 7704 Tektronix Scope or equivalent.
2. P6201 Tektronix Scope Probes.

Figure 12-1
Data PCB Test Point Descriptions

1. E12 (1F DATA PATTERN)

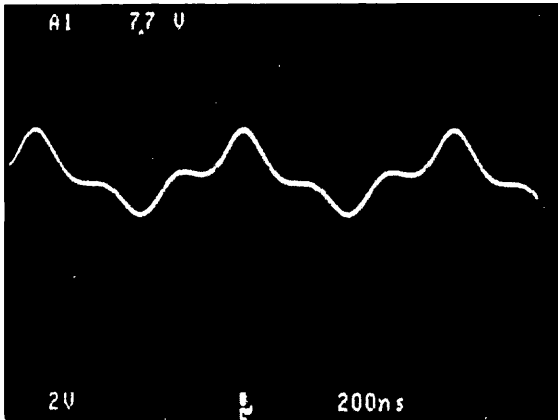


2. E6 (1F DATA PATTERN)



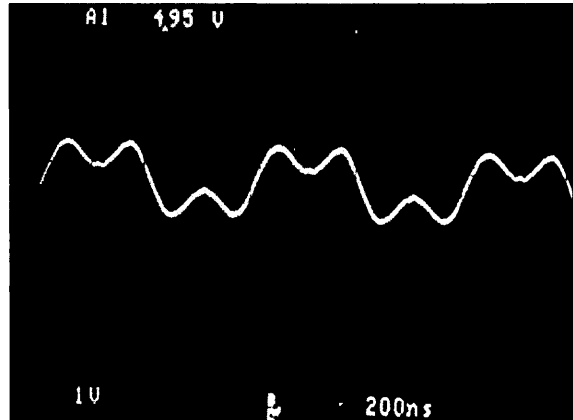
800 MV
TO 2.2V

3. E7 (1F DATA PATTERN)



TYPICAL 4 TO 6 VOLTS
DIFFERENTIAL

4. E4 AND E5 (1F DATA PATTERN)



1.8 TO 2.4 VOLTS
TYPICAL DIFFERENTIAL

Figure 12-2
Test Point Outputs

5. 1. PEAK DETECT U18 PIN 38
2. ZERO CROSSING DETECT. U14-11
3. READ DATA U14 PIN 3 (IF DATA PATTERN)

WRITE DATA U18 PIN 32
(IF DATA PATTERN)

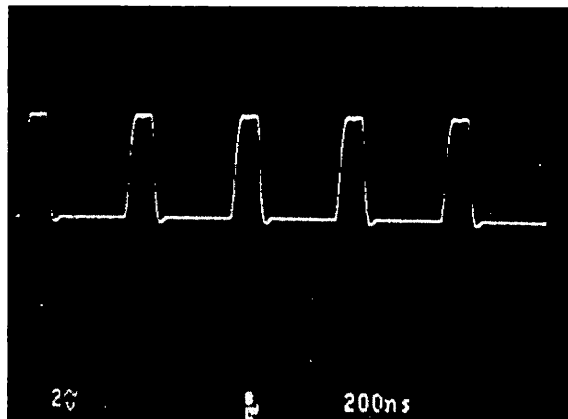
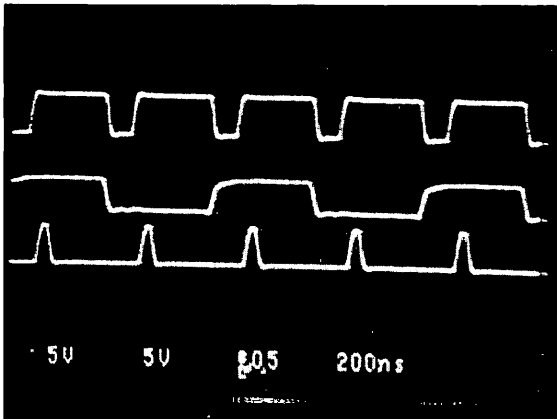


Figure 12-2 (continued)
Test Point Outputs

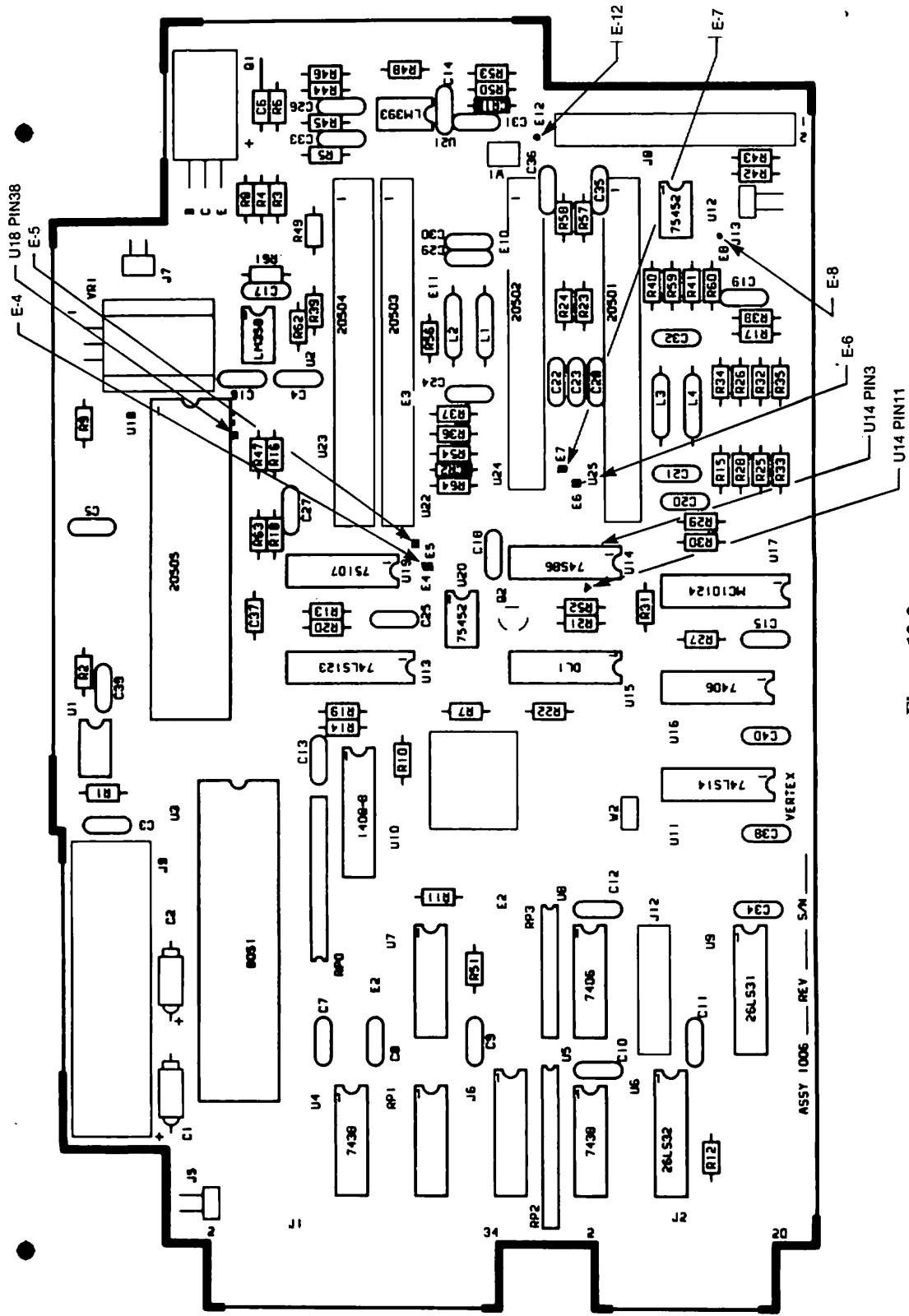


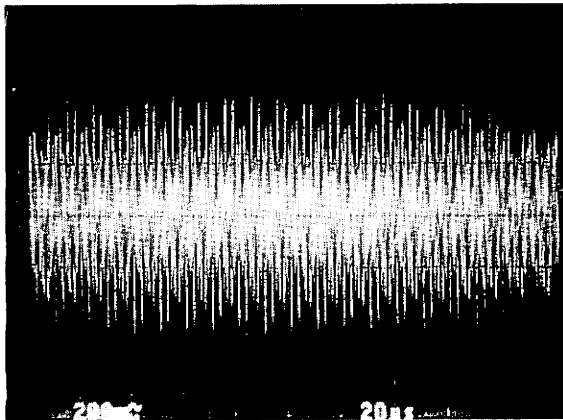
Figure 12-3
MLC 2.X Test Point Locations
Data PCB

12.2 Servo PCB Test Points (MLC 2.X)

1. E28 - Servo Head Data Output
2. E3 - Channel 1 Mixer Output
3. E4 - Channel 2 Mixer Output
4. E5 - Channel 1 Low Pass Filter Output
5. E18 - Channel 2 Low Pass Filter Output
6. E21 - Track \emptyset Detector Output
7. E16 - Channel 2 Rectifier Output
8. E6 - Channel 1 Rectifier Output
9. E10 - Position Error Signal (PES)
10. E12 - Offtrack Detector Output
11. E13 - On Peak Detector Output Seeking
12. E15 - Velocity Error Signal
13. E9 - Velocity Command
14. E17 - Servo Error Signal
15. E26 - Motor Speed Control Signal (360 Hz)

Figure 12-4
Servo PCB Test Point Descriptions

1. E28 SERVO HEAD DATA
OUTPUT TRK FOLLOWING



2. E3 CHANNEL 1 MIXER OUTPUT
TRACK FOLLOWING

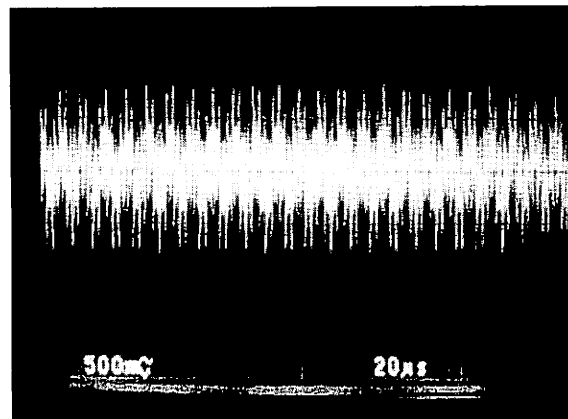
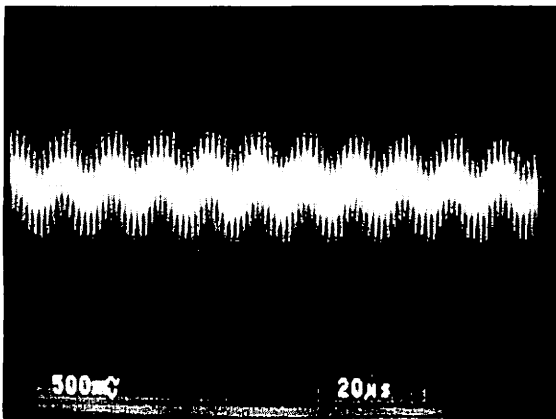
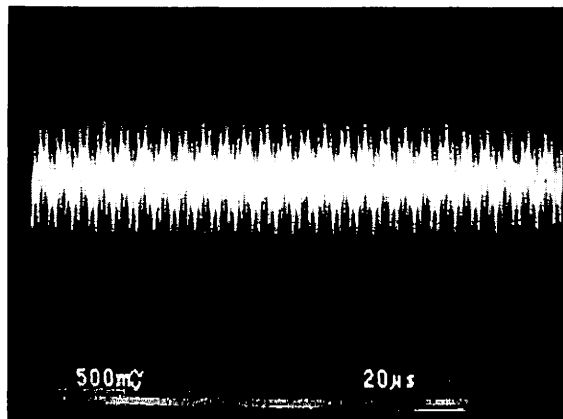


Figure 12-5
Test Point Outputs

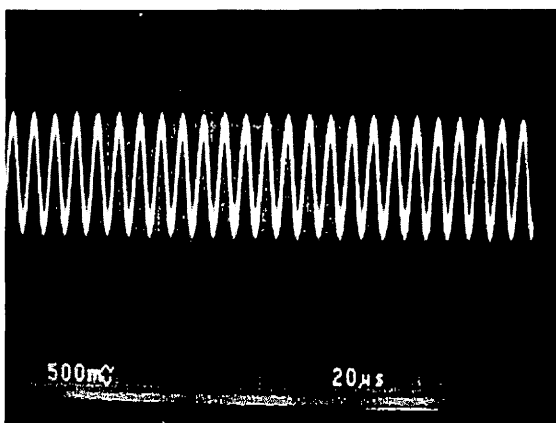
3. E4 CHNL 2 MIXER OUTPUT
TRACK FOLLOWING @ TRK 0



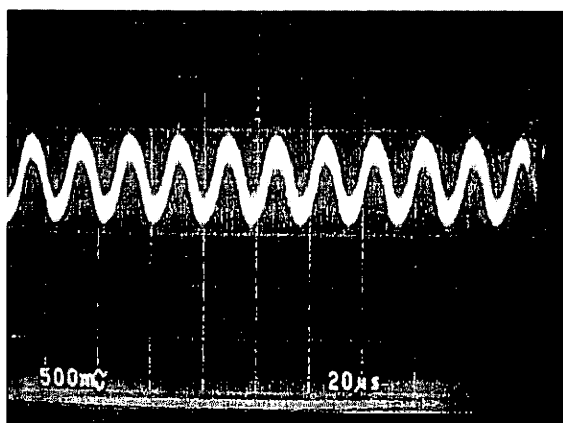
3A. CHANNEL 2 MIXER OUTPUT
TRACK FOLLOWING @ TRK 1



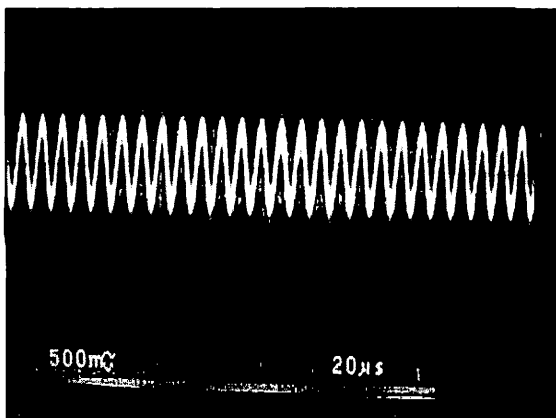
4. E5 CHANNEL 1 LOW PASS FILTER
OUTPUT TRACK FOLLOWING
AT TRK 0



5. E18 CHANNEL 2 LOW PASS FILTER
OUTPUT TRACK FOLLOWING
AT TRACK 0



5A. E18 CHANNEL 2 LOW PASS FILTER
OUTPUT TRACK FOLLOWING
AT TRACK 1



6. E16 CHANNEL 2 RECTIFIER OUTPUT
TRACK FOLLOWING AT TRK 0

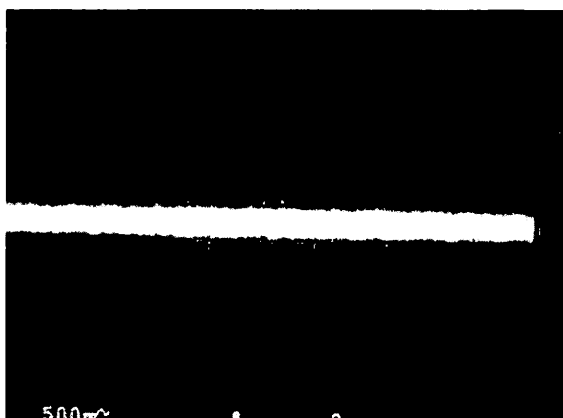
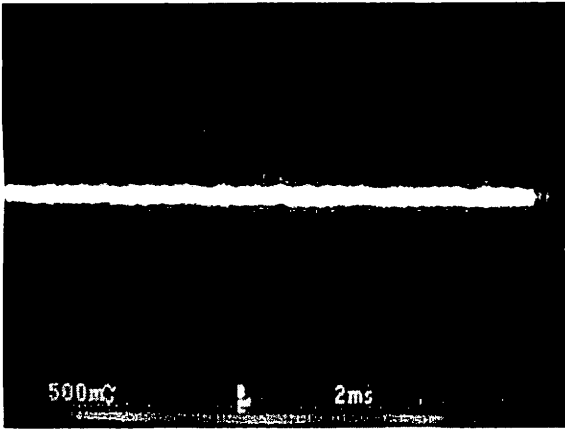
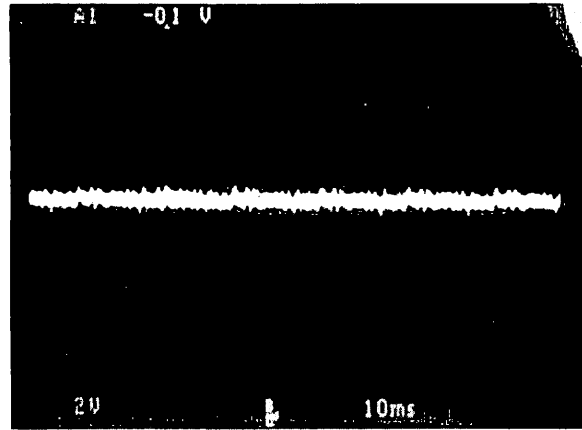


Figure 12-5 (continued)
Test Point Outputs

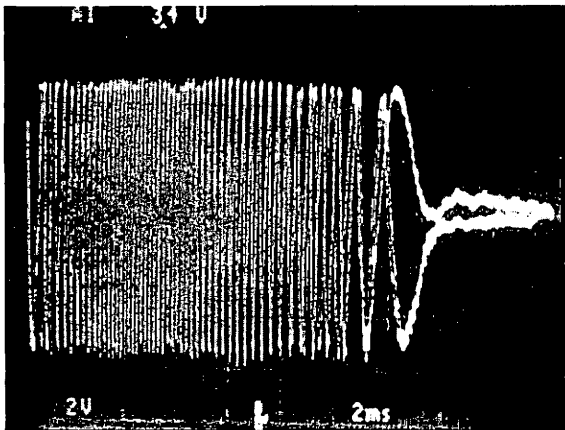
6A. E16 CHANNEL 2 RECTIFIER OUTPUT
TRACK FOLLOWING AT TRK 1



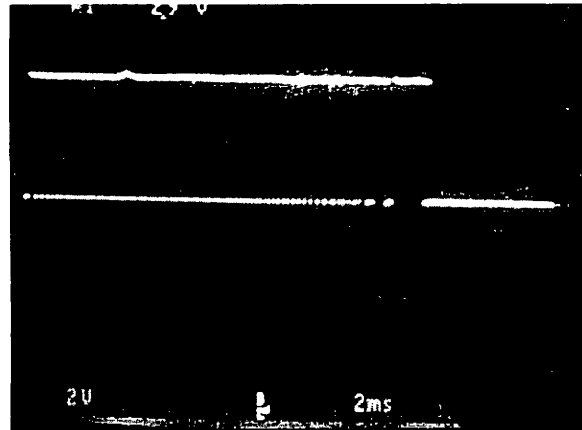
7. E10 POSITION ERROR SIGNAL (PES)
TRACK FOLLOWING AT TRK 0



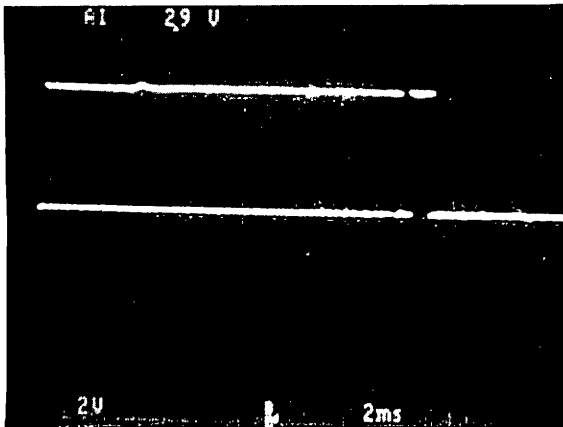
7A. PES SIGNAL E10
100 TRACK SEEK



8. E12 OFFTRACK DETECTOR OUTPUT
100 TRACK SEEK



9. E13 ON PEAK DETECTOR OUTPUT
100 TRACK SEEK



10. E15 VELOCITY ERR. SIGNAL OUTPUT
(TRIGGER ON E19)
100 TRACK SEEK

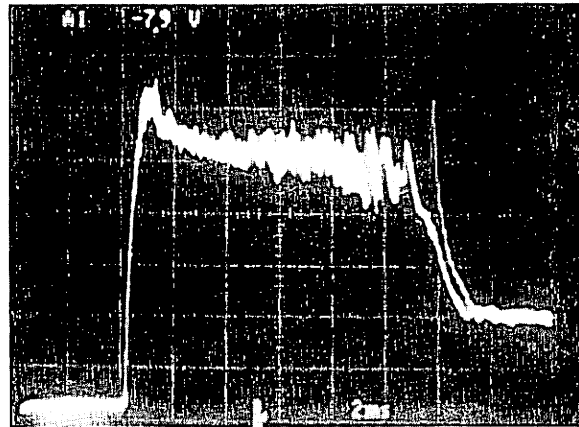
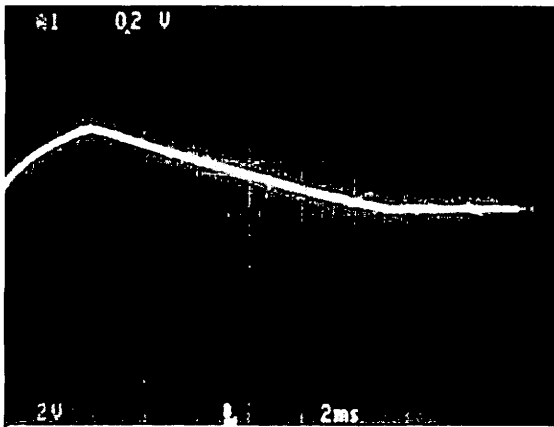
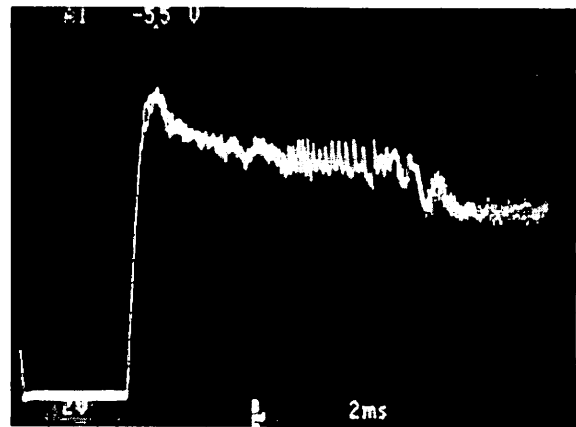


Figure 12-5 (continued)
Test Point Outputs

11. E9 VELOCITY COMMAND SIGNAL
100 TRACK SEEK, (TRIGGER
ON E19)



12. E17 SERVO ERR. SIGNAL
100 TRACK SEEK



13. E26 MOTOR SPEED CONTROL
OSCILLATOR SIGNAL
360 Hz

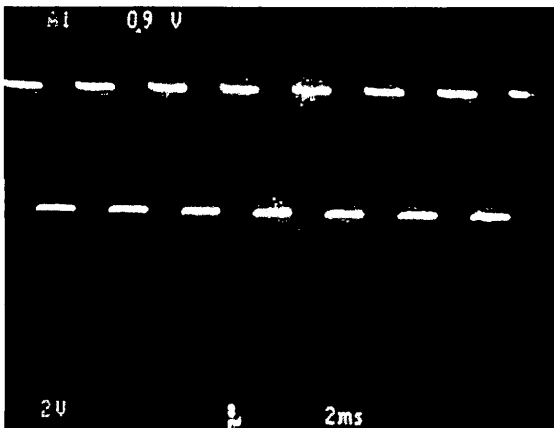


Figure 12-5 (continued)
Test Point Outputs

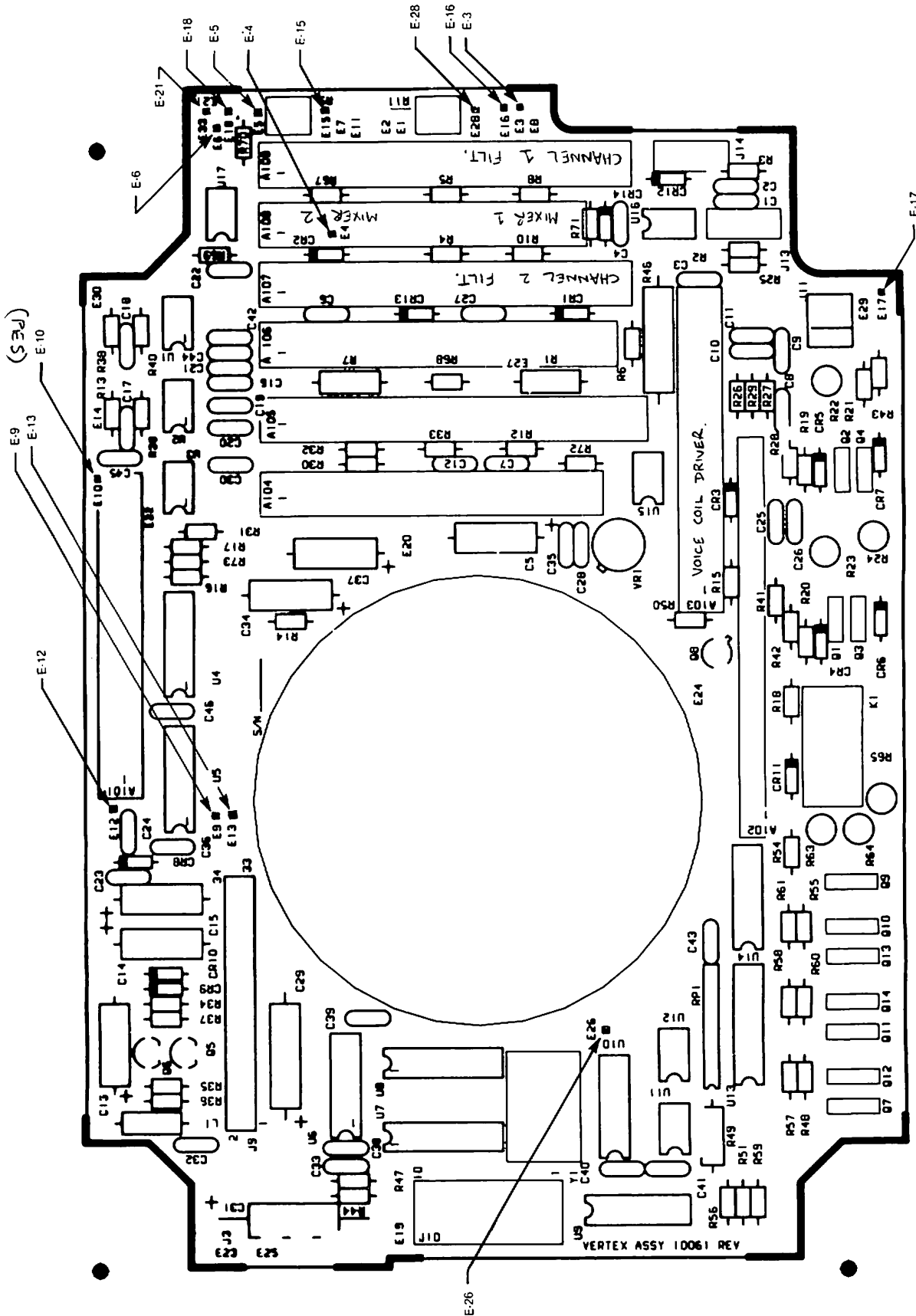


Figure 12-6.
MLC 2.X Test Point Locations
Servo PCB

APPENDIX A

UNPACKING AND HANDLING GUIDE

A.1 Introduction

This manual contains procedures for installing all Priam V100 disk drives. Included are instructions for unpacking and inspection, handling guidelines, shipping instructions, and an unpacking checklist.

A.2 Unpacking the Drive

A.2.1 Shipping Damage Inspection

Priam disk drives are packaged to withstand normal handling in reusable shipping containers. It is the customer's responsibility to notify the carrier if shipping damage should occur to a drive.

When the shipment is received, examine the shipping container for obvious signs of shipping damage. Most insurance adjusters require inspection of the damaged container. Notify the carrier and Priam Customer Service immediately if shipping damage is discovered.

Note: When handling the drive while still in the shipping container, ensure that the container remains in the upright position indicated by the attached labels.

A.2.2 Opening the Shipping Container

Both the single and multiple drive shipping containers consist of an outer carton and inner packaging. Open the outer carton by cutting the tape securing the top flaps.

A.2.3 Removing Drive From Shipping Container

Single-Pack (Figure A-1)

1. Cut tape.
2. Remove top foam pad from shipping container.
3. Using two hands, lift drive up and out of foam cushion.

Caution! Dropping the drive can cause severe damage to the Head Disc Assembly. Such damage is not covered under the warranty.

Place the drive on a clean, flat, padded surface. Remove and discard plastic bag. Retain the shipping container and inner packaging for any future shipments of the drive.

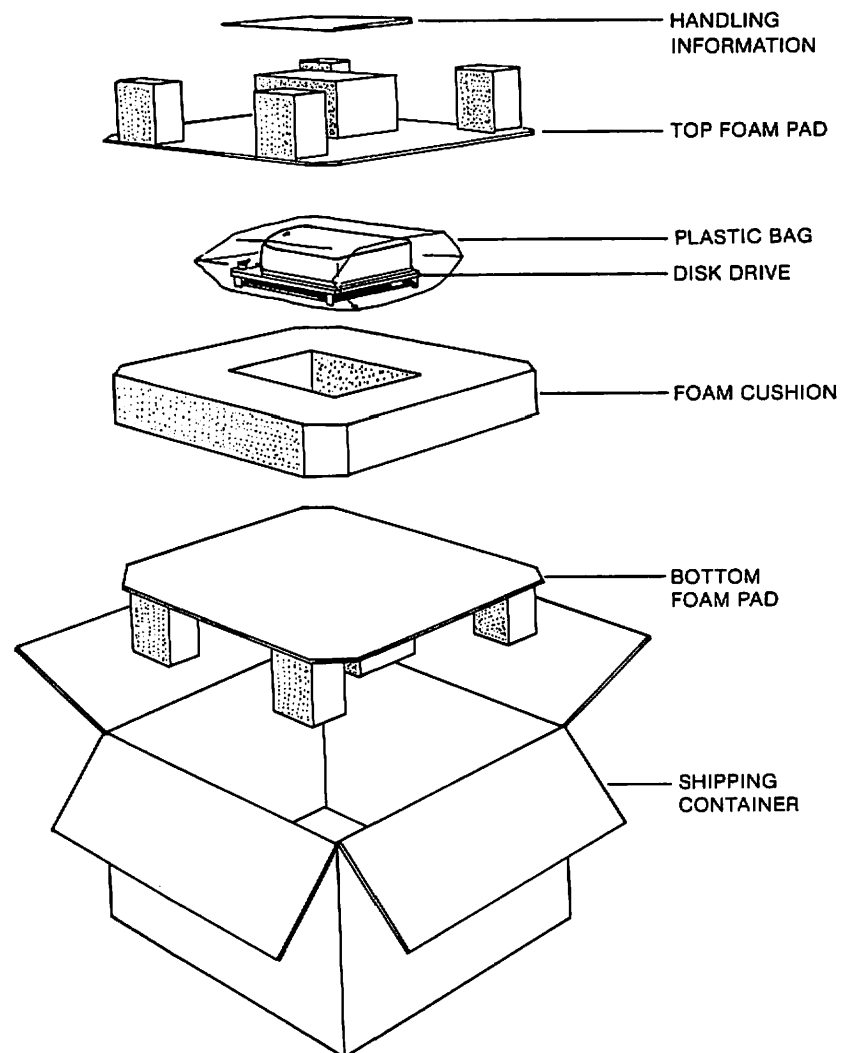


Figure A-1
Single Drive Packaging

Four-Pack (Figure A-2)

1. Cut tape.
2. Remove top foam cushion from shipping container.
3. Using two hands, lift inner drive container up and out of foam cushion.
4. Open inner drive container, and again using two hands, carefully remove each drive.

Caution! Dropping the drive can cause severe damage to the Head Disc Assembly. Such damage is not covered under the warranty.

Place the drive on a clean, flat, padded surface. Remove and discard plastic bag. Retain the shipping container and inner packaging for any future shipments of the drive.

Eight-Pack (Figure A-3)

1. Cut tape.
2. Remove top foam cushion from shipping container.
3. Using two hands, lift drive up and out of foam cushion.
4. Set each drive on clean, flat, padded surface.
5. Carefully lift empty foam cushion out of the shipping container.
6. Remove remaining 4 drives from shipping container.

Caution! Dropping the drive can cause severe damage to the Head Disc Assembly. Such damage is not covered under the warranty.

Remove and discard plastic bag. Retain the shipping container and inner packaging for any future shipments of the drive.

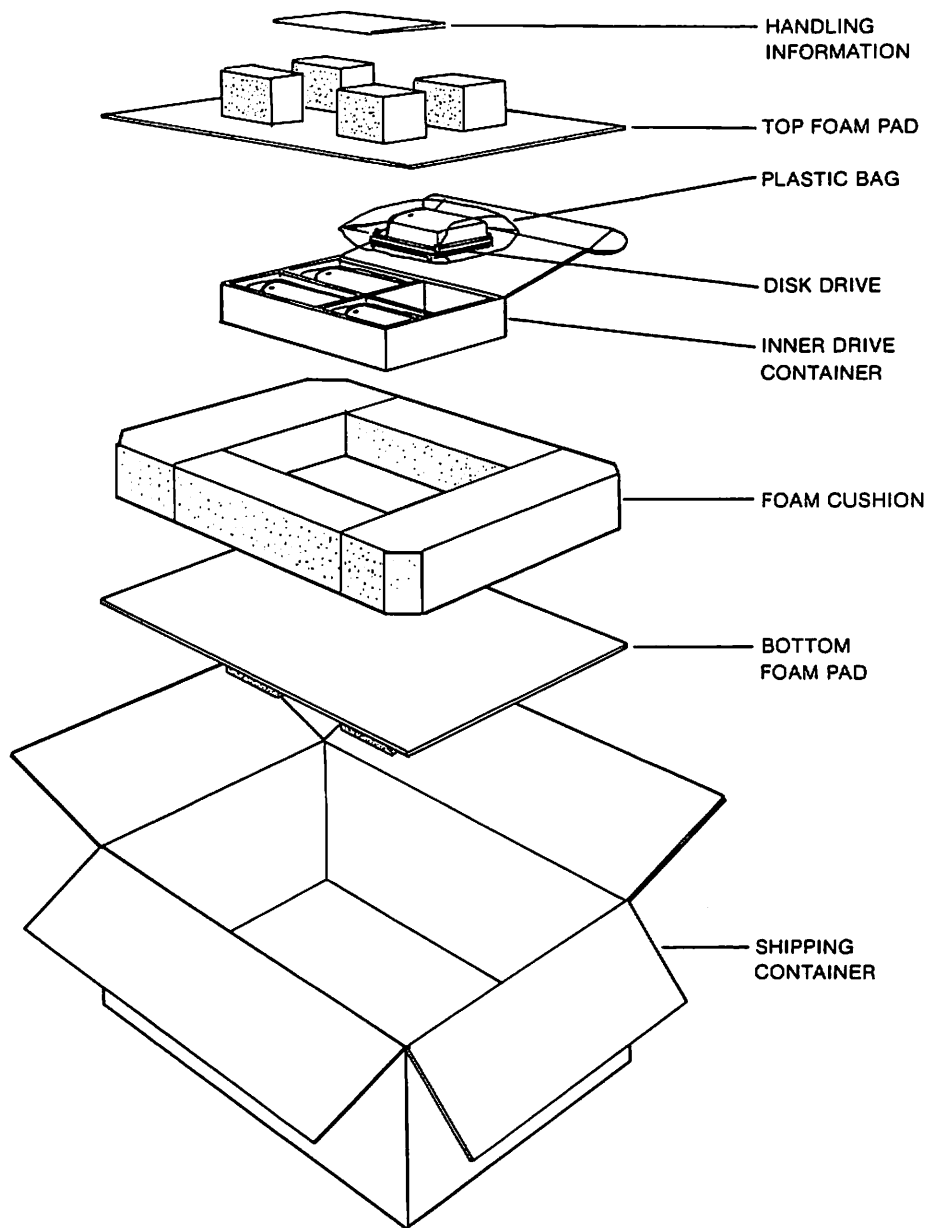


Figure A-2
Four-Pack Drive Packaging

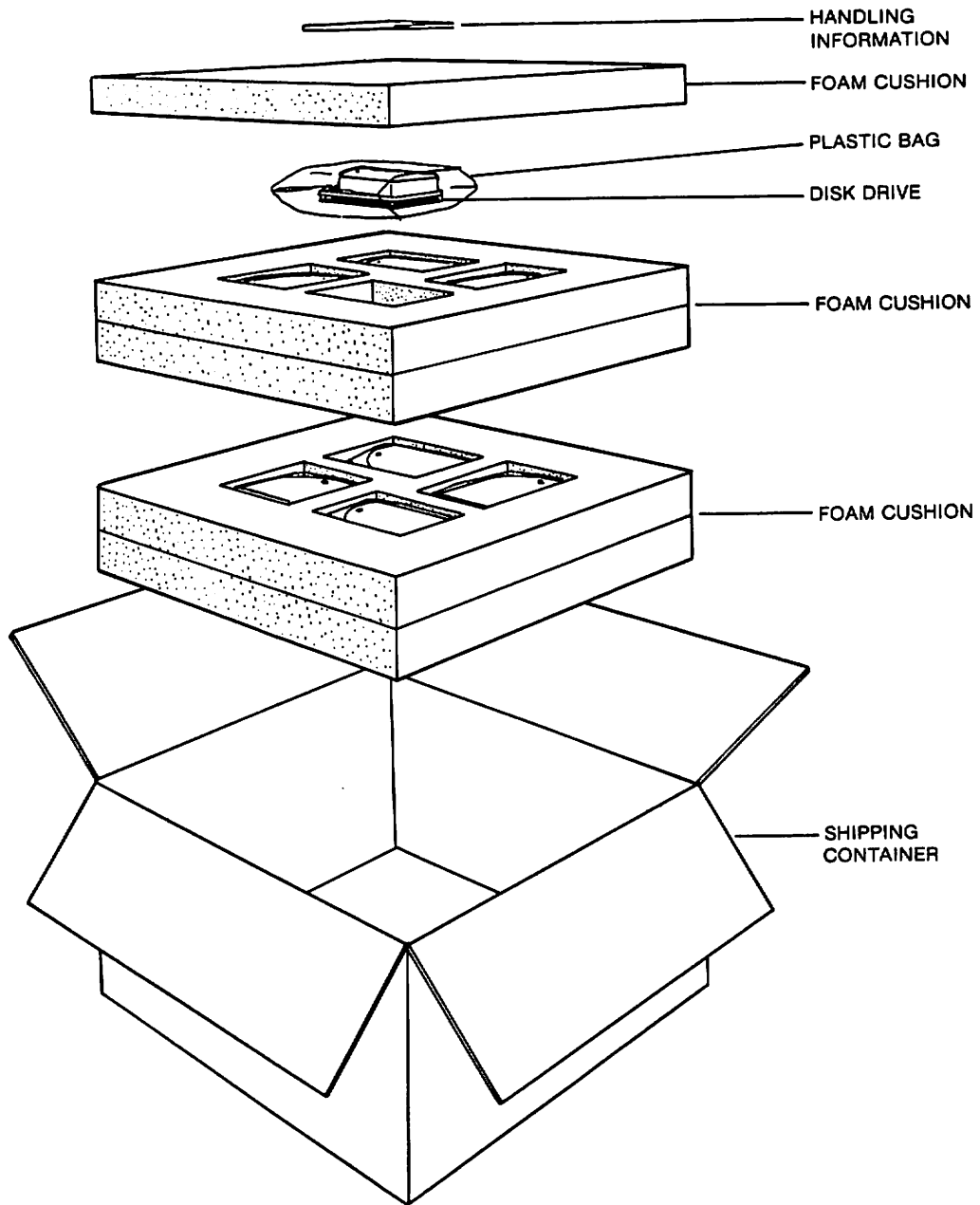


Figure A-3
Eight-Pack Drive Packaging

A.2.4 Inspection Procedures

After unpacking the disk drive, inspect it thoroughly for damage hidden by the packaging and for loose components or fittings as follows:

- a. Inspect interior for shipping damage.
- b. Examine internally mounted components for loose or missing hardware.
- c. Tighten all loose hardware.
- d. Clean frame interior by removing loose debris.

A.3 Handling Procedures

A.3.1 Shock and Vibration Precautions

The drives must be handled in such a manner as not to exceed the Non-Operational Shock and Vibration limits specified in the Priam V100 OEM Manual (P/N 308100).

A.3.2 Automatic Head Actuator Lock

This automatic lock requires no action by the user. When the drive is powered down, the actuator is automatically locked to prevent possible head/media damage when shipping and handling the drive.

A.3.3 Drive Handling Guidelines

Adhere to the steps outlined in Table A-1 when handling disk drives.

Table A-1. Winchester Disc Drive Handling Guidelines

- o Do not drop drive from any height. Set drive down carefully on padded surface.
- o Carts used to transport drives should have soft rubber wheels to absorb shock. Place foam pad under drives when transporting.
- o Store and transport drive in a vertical position with long dimension horizontal or flat, top up, and drive motor down. Drive must rest on flat surface. Do not put papers, etc. under drive.
- o Do not dress or reposition components, wires, or cables.
- o Do not place drives in vertical position closer than 2 to 3 inches apart to avoid hitting and breaking components.
- o Avoid manual rotation of spindle or movement of carriage. Damage to disk surface may occur if the heads move with respect to the disk surface.
- o Do not remove seals from Head/Disk Assembly. This may result in contamination which can affect drive operation. Do not attempt to disassemble Head/Disk Assembly.
- o Do not place objects on top of drive (especially metallic objects).
- o Do not store drive where possibility exists of condensation from humid air.

A.4 Shipping Requirements

A.4.1 Automatic Head Actuator Lock

This automatic lock requires no action by the user. When the drive is powered down, the actuator is automatically locked to prevent possible head/media damage when shipping and handling the drive.

A.4.2 Shipping a Stand-Alone Unit

After the drive is removed from the system, the drive must be packaged to withstand the environmental extremes specified in the V100 OEM Manual. Use of the original Priam shipping container is recommended. Do not rewrap the drive in plastic, as damage may occur from resulting humidity.

A user designed shipping container may be substituted if it meets or exceeds the Priam specifications.

Note: Failure to ship the drive in a proper container will void the Priam warranty.

Important! Remove slides, brackets, parts of enclosures, and cables from the drive before placing it in the shipping container.

A.4.3 Shipping Drive Mounted in an Enclosure

When shipping a drive while still installed in a system, adhere to all environmental specifications in the V100 OEM Manual. If the system or enclosure cannot be packaged for shipment so that the drive will meet the specifications in the OEM Manual, it is recommended that the drive(s) be removed from the system or enclosure prior to shipment and shipped as a stand-alone unit. Refer to paragraph 4.2 for stand-alone shipping instructions.

A.4.4 Return Authorization

Contact Priam Customer Service for a return authorization number prior to shipping a drive or assembly to Priam.

A.5 Other Documentation

Manuals, specifications, schematics and other technical documents are available from Priam. To order additional data, contact Priam Technical Support at:

Priam Technical Support
20 West Montague Expressway
San Jose, CA 95134

Phone: (408) 946-4600
TWX: 910-338-0293

UNPACKING CHECKLIST

Model _____

S/N _____

Date _____

This checklist is provided to aid in the unpacking and handling of Priam V100 Disk Drives. It is important for the protection of your warranty that these instructions be followed exactly. Refer to the indicated paragraphs of this document for more details on each step.

1. Carefully inspect the shipping container (inside and out) for obvious damage (paragraph A.2.1). **DO NOT PROCEED IF THERE APPEARS TO BE SHIPPING DAMAGE.**
2. Open the shipping container. Avoid using sharp instruments to open the container. Remove the information packet (paragraph A.2.2).
3. Open the inner container. Using both hands, lift the drive out of the shipping container (paragraph A.2.3).

Caution! Do not lift the drive by means of the printed circuit assembly.

4. Remove and discard plastic bag.
5. Inspect the drive for shipping damage, particularly loose, broken or unfastened connectors or wires (paragraph A.2.4).
6. Tighten all loose hardware.
7. Clean the cabinet interior by removing loose debris.

Note: Priam recommends saving the shipping container and inner packaging for reuse in possible shipping or storing of the equipment.

Reader Comments

Your comments concerning this publication are important to us. Please take the time to complete this questionnaire and return it to Priam Corporation.

Title of Publication: V100 OEM Service Manual

Document Number: 308100 REV LTR A EC 10299

Your Hardware Model: _____

Describe your likes/dislikes concerning this document:

Technical Information: _____

Supporting Diagrams: _____

Ease of Use: _____

Your Name: _____

Company and Address: _____

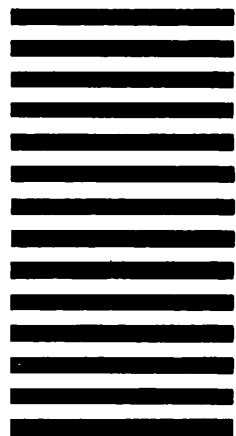
Your Position/Department: _____



NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES



BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 6673 SAN JOSE, CA



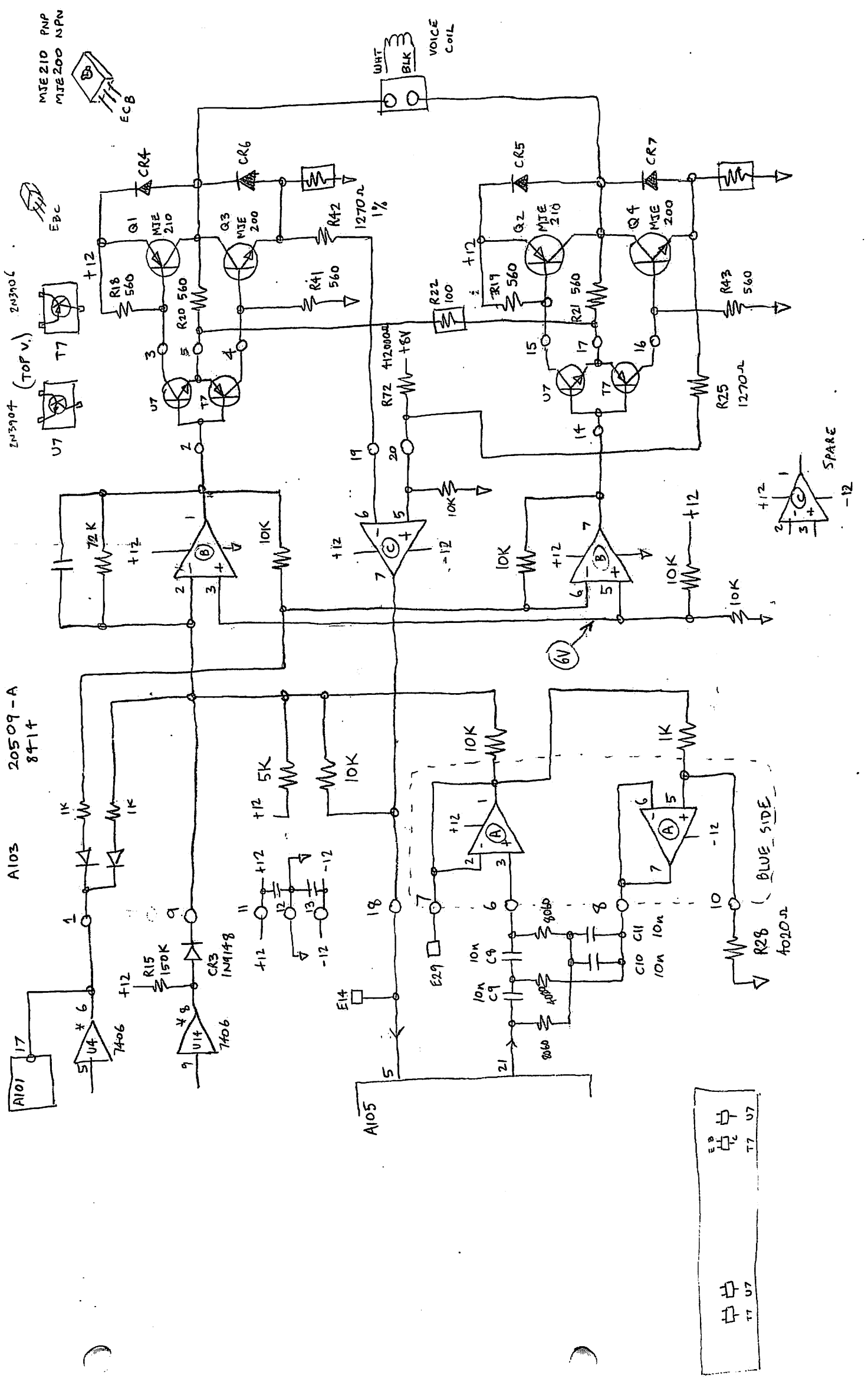
POSTAGE WILL BE PAID BY ADDRESSEE

Priam Corporation
ATTN: Tech Support
20 W. Montague Expressway
San Jose, CA 95134



20 West Montague Expressway
San Jose, California 95134

(408) 946-4600
TWX 910-338-0293



MJE 210 PNP
MJE 200 NPN

2N3904 (TOP V.)
EBC

2N3904

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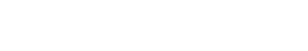
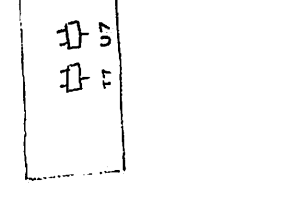
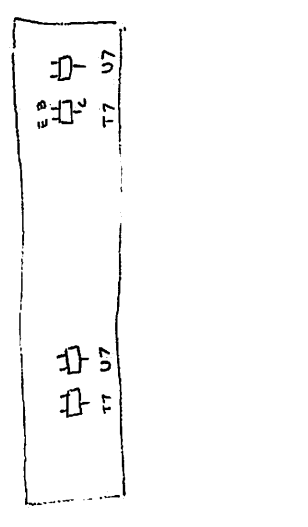
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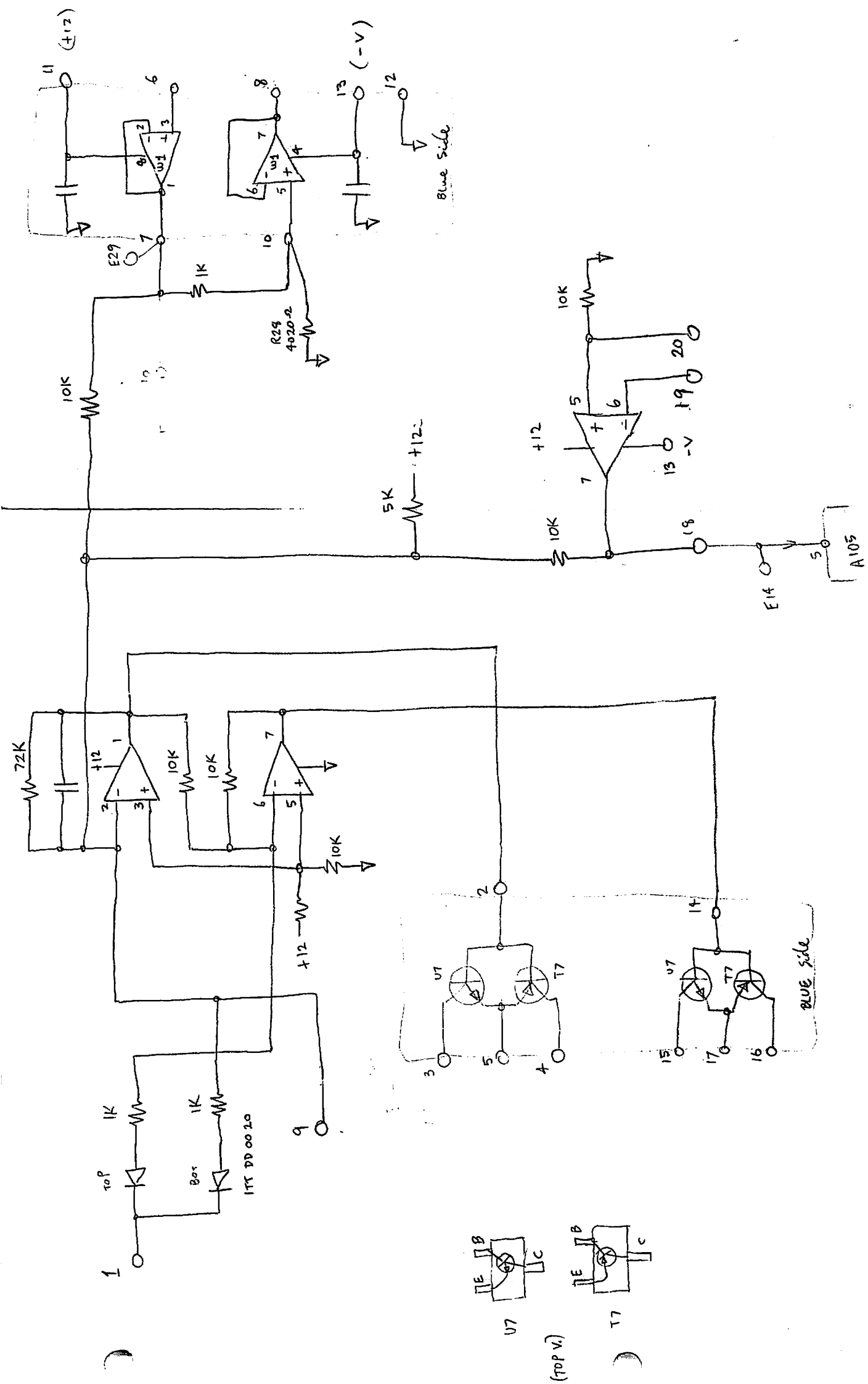
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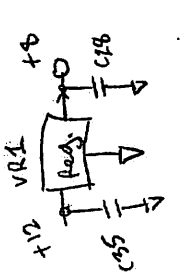
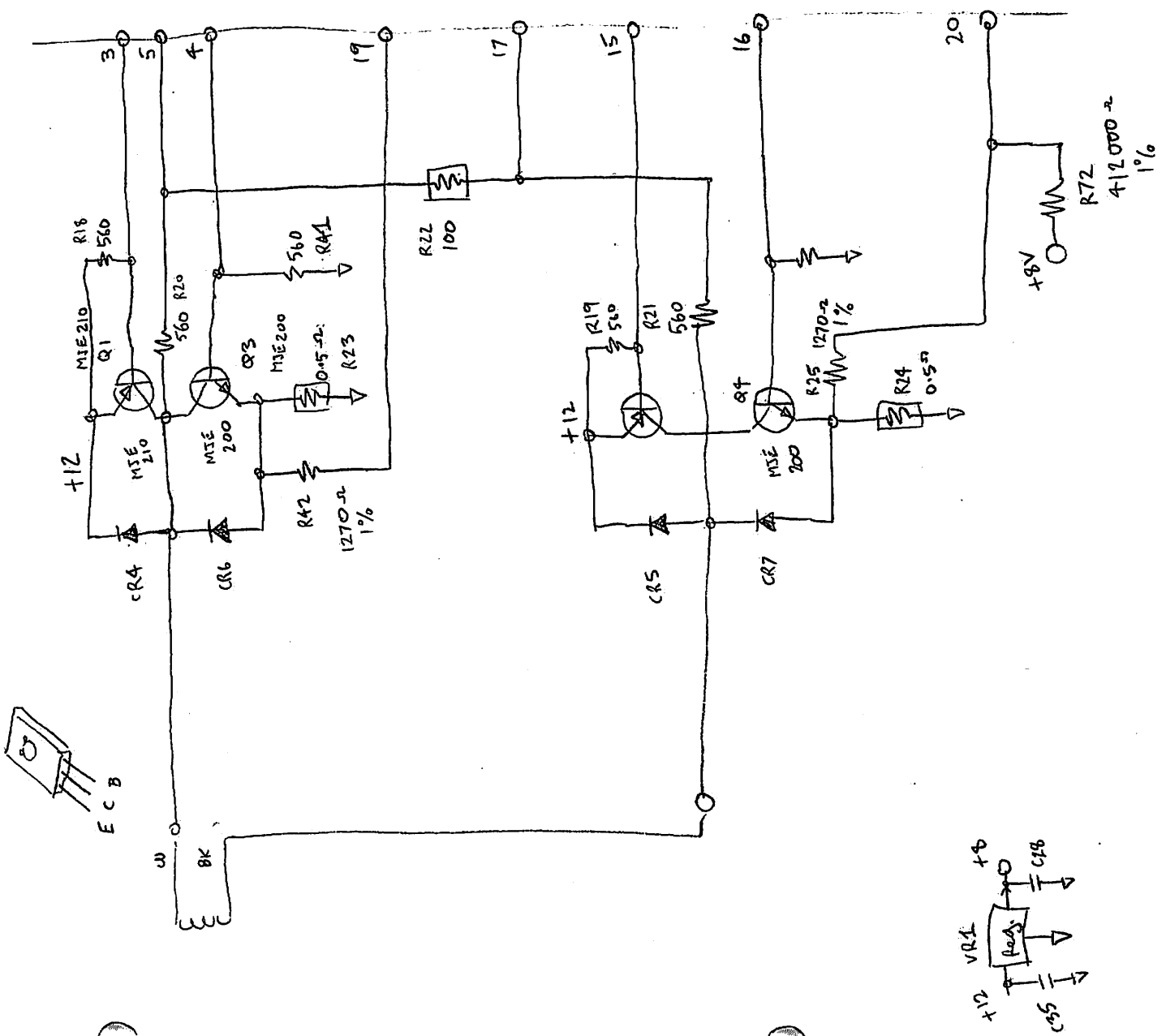
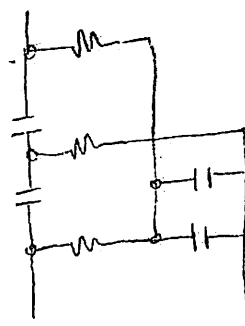
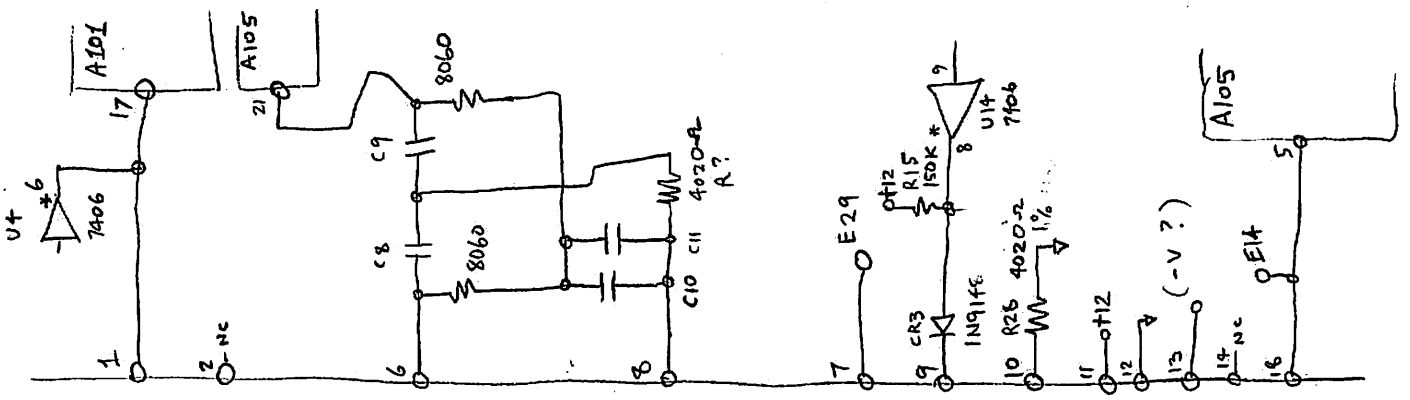


VOICE COIL
WHT
BLK

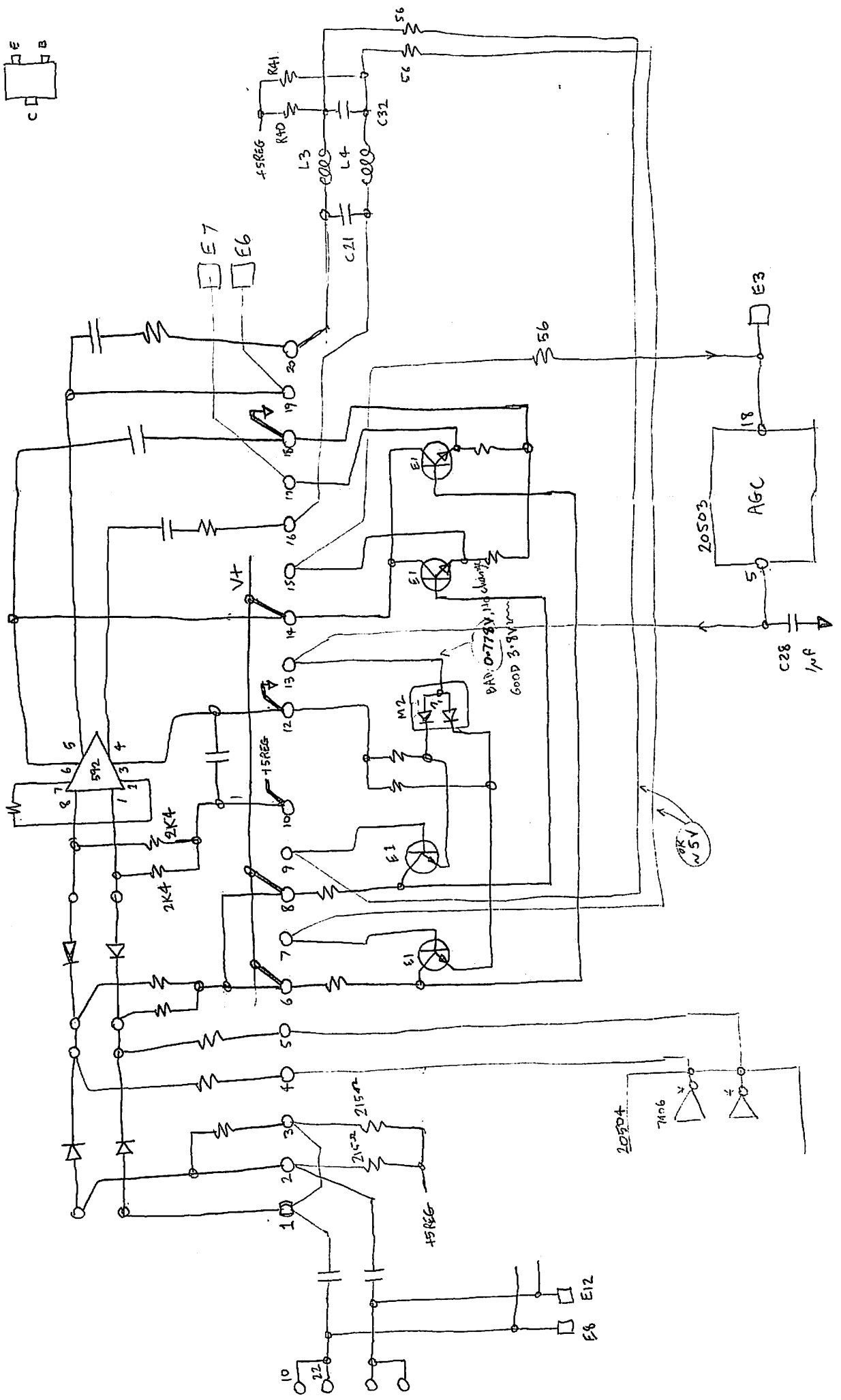
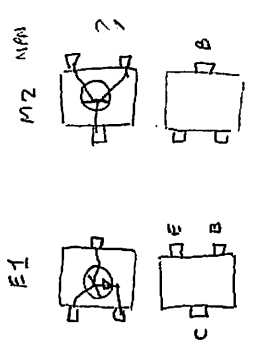
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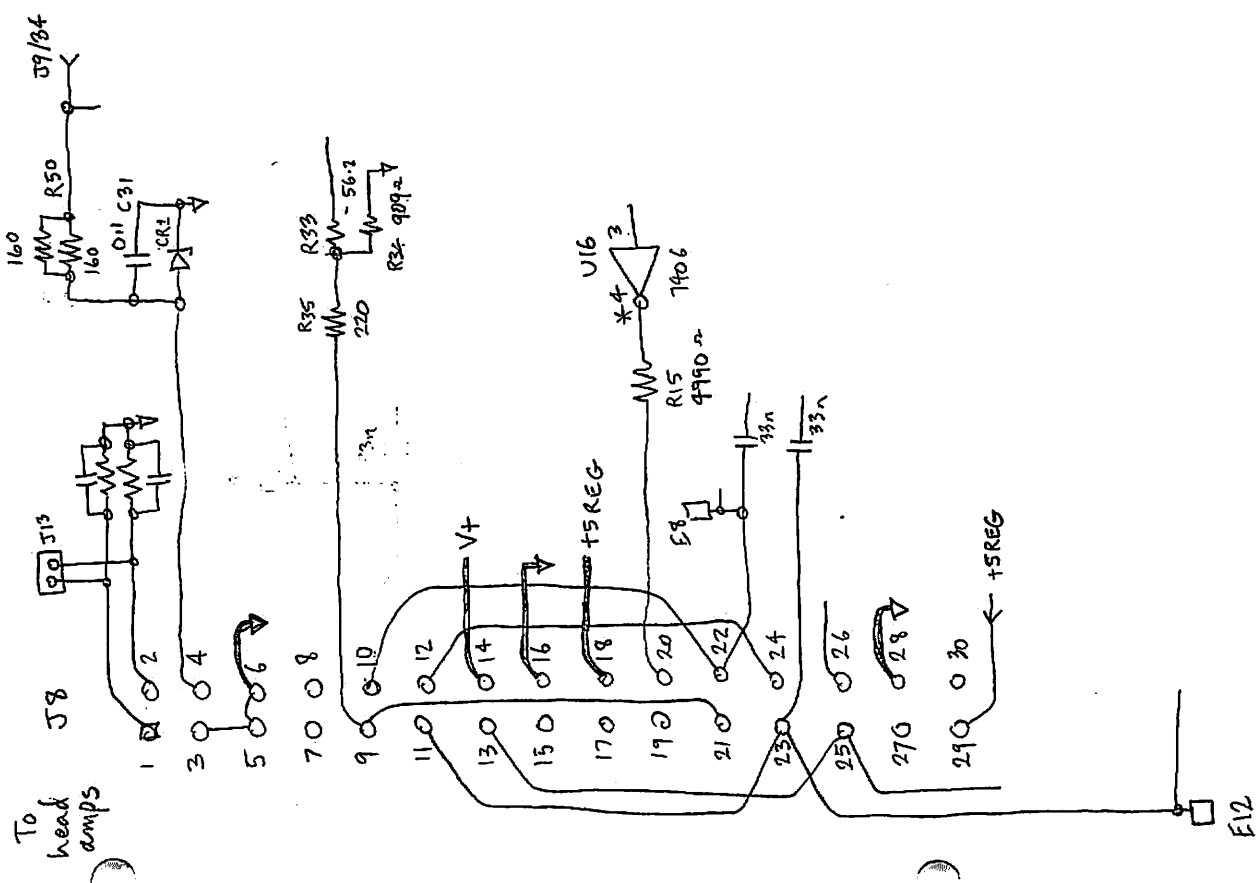
BLUE SIDE





20501 Read amp, filter

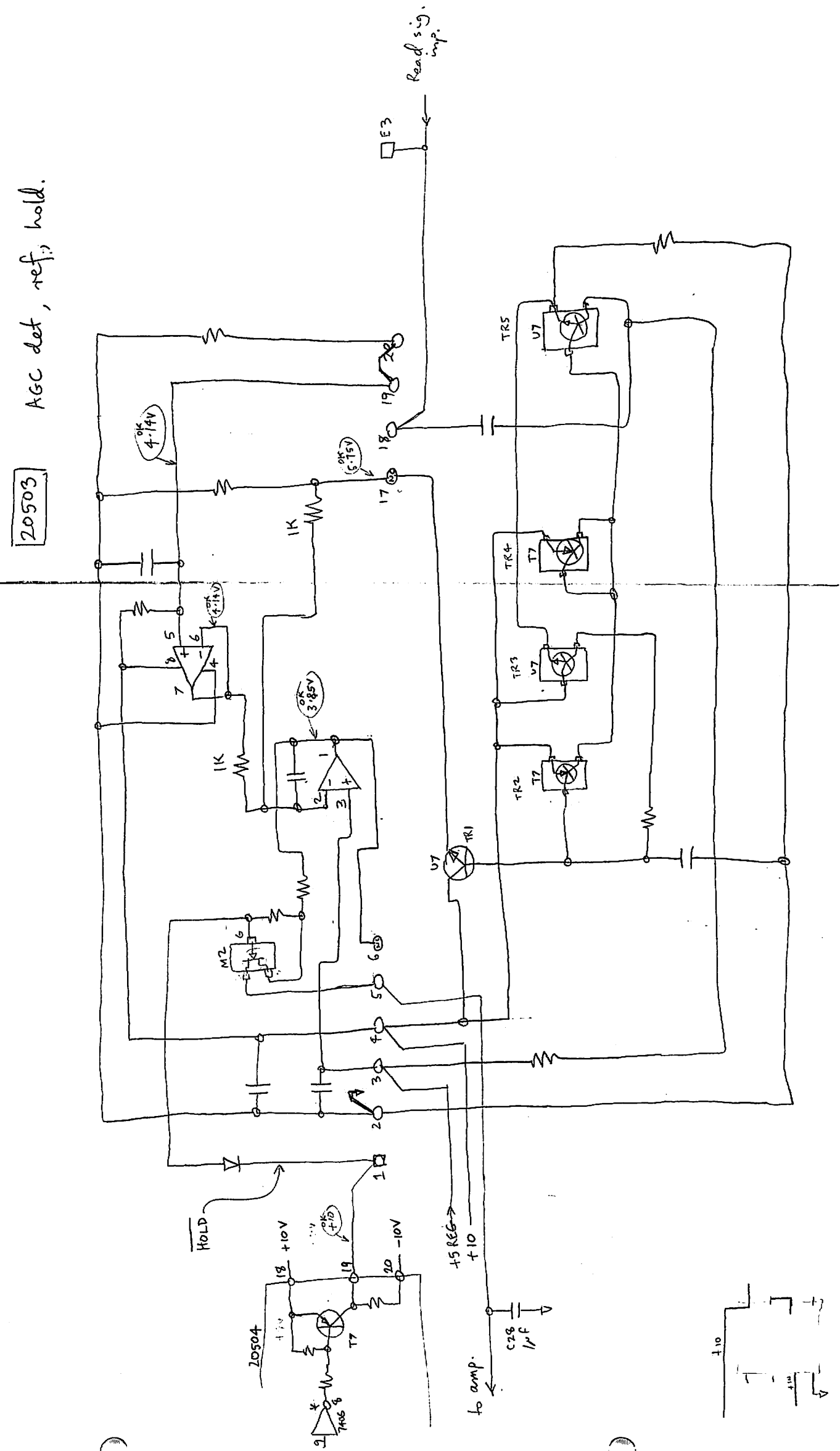


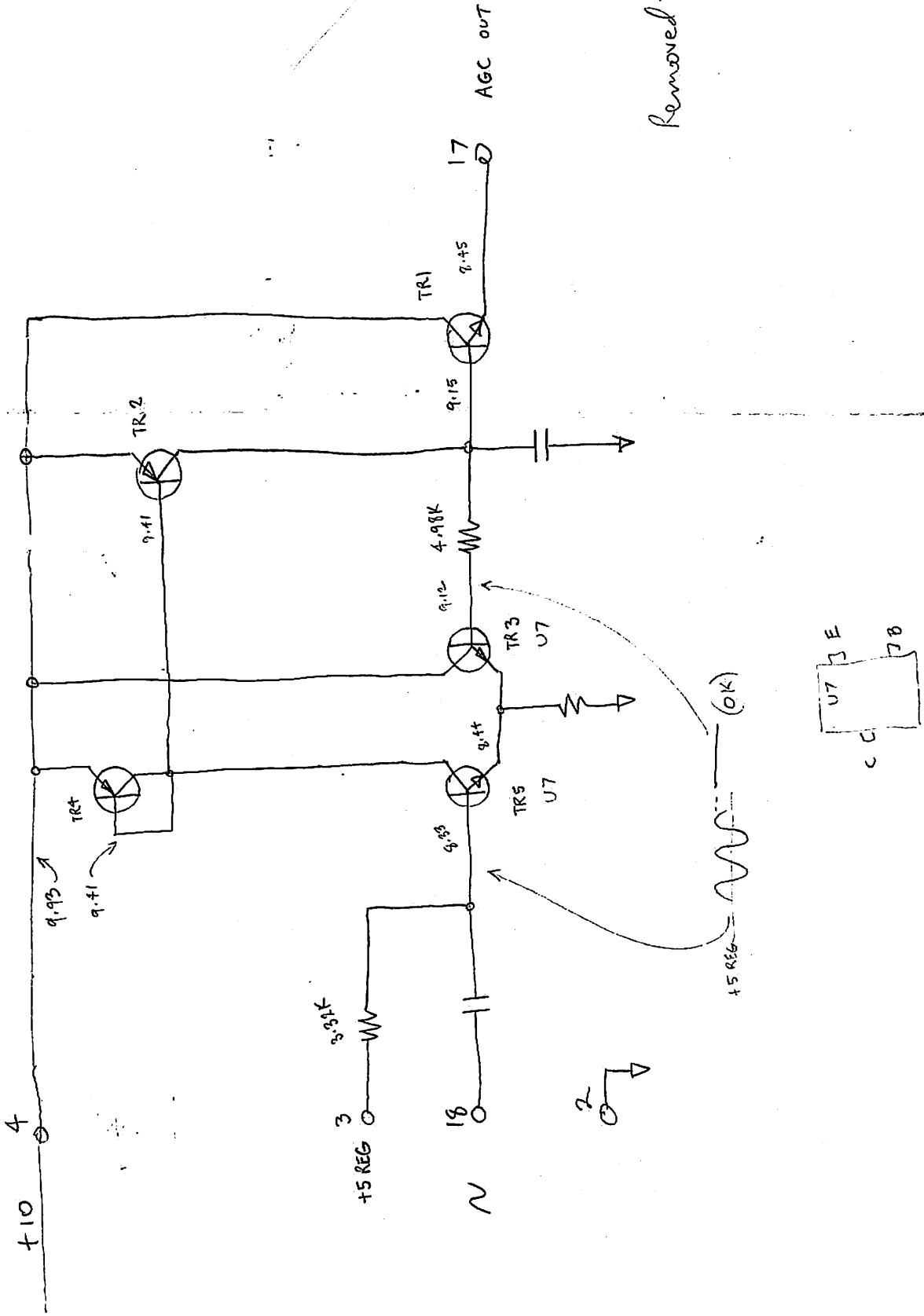


AGC det, ref, hold.

20503

Read sig.
imp.





Removed TR5. TR4 + 2 STILL ON!