PM-S1132

Semiconductor Memory Manual

Plessey
Peripheral
Systems

PM-S1132

Semiconductor Memory Manual

April 1978 - Revision A

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET 0-0

FORM 000021

Preface

This manual provides the information needed to install, operate, maintain, and troubleshoot the PM-S1132 Semiconductor Memory manufactured by Plessey Peripheral Systems, Irvine, California.

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		0-4

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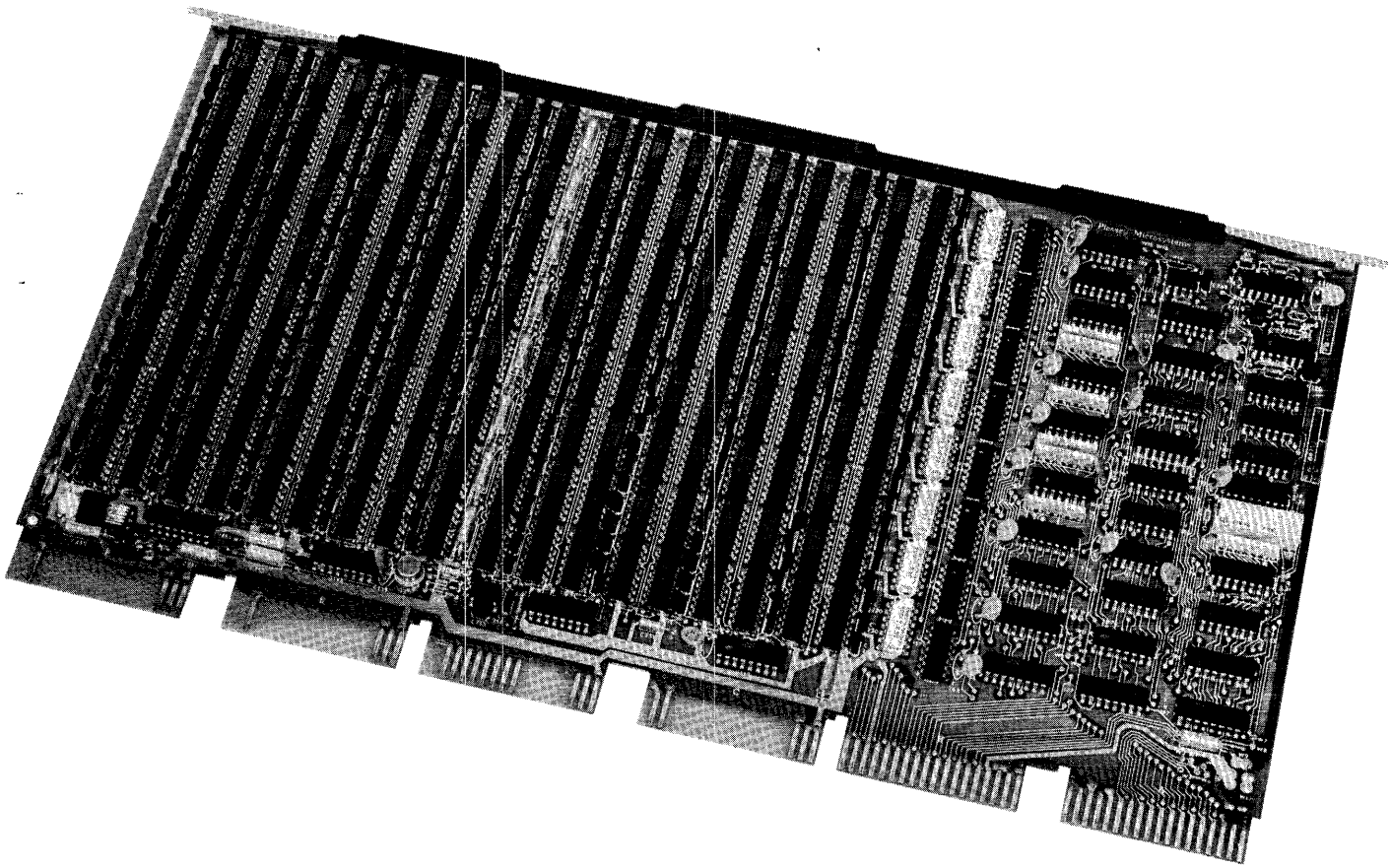

PM-S1132 SEMICONDUCTOR MEMORY

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A	52648	MA 700755
SCALE	REV A	SHEET 0-6

Section 1

General Information

1.1 INTRODUCTION

This manual provides the information needed to install, operate, maintain and troubleshoot the PM-S1132 semiconductor memory manufactured by Plessey Peripherals, Irvine, California 92714.

The material is arranged into five sections as follows:

- Section 1 - GENERAL INFORMATION

  This section contains a brief functional description of the PM-S1132 and a description of the electrical specifications of the memory.

- Section 2 - INSTALLATION

  This section explains the requirements and procedures for equipment installation. Address selection and memory versions are also described.

- Section 3 - FUNCTIONAL DESCRIPTION

  This section contains a detailed functional description of the PM-S1132 including addressing, timing and control circuits, and chip layouts.

- Section 4 - THEORY OF OPERATION

  This section contains a circuit logic description of the PM-S1132 memory.

- Section 5 - MAINTENANCE AND TROUBLESHOOTING

  This section describes maintenance and troubleshooting procedures. It contains troubleshooting charts to aid in decoding the failing 4K RAM.

- Appendices - The appendices contain the parts list, logic diagrams, and assembly drawings required for a complete understanding of the unit.

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1.2 GENERAL DESCRIPTION

The PM-S1132 is a 64K byte dynamic MOS memory designed to operate in the Digital Equipment Corporation (DEC) PDP-11 series computers.* The PM-S1132 is designed using 4K dynamic MOS random access memories (RAM). The memory is available with or without parity in any of the following capacities: 8K, 16K, 24K, 32K, 40K, 48K, 56K, and 64K bytes.

1.2.1 Characteristics of MOS Devices

The use of MOS memory circuits provides economical and operational advantages. The cost-per-bit for MOS memories is low and remains approximately constant with use.

MOS memory provides a non-destructive readout. This eliminates the write-after-read cycle time associated with core memory. Power consumption with dynamic MOS devices, such as the ones used in the PM-S1132, is low. The disadvantage of MOS devices is volatility, i.e., using battery-supported power supplies which will maintain data retention for as long as several hours. The PM-S1132 is designed with a low-power mode (jumper selectable) to maximize the effectiveness of battery-powered operation.

Another characteristic of dynamic MOS devices is that they must be cycled periodically to ensure date validity. This is known as a refresh cycle. The PM-S1132 contains all the necessary logic and timing circuits to ensure that refresh cycles are performed. Should a processor or NPR request come during a refresh cycle, it is held up until the refresh cycle is completed, and then processed. The amount of time lost to bus masters because of refresh is dependent on the bus activity. For a system that uses the bus at a maximum cycle time of 500ns the loss of memory availability is less than two percent.

1.2.2 Memory Configuration

The PM-S1132 is available in two basic configurations. It is important to specify the correct configuration for the backplane and system in which the memory is to be installed.

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Versions 100 Through 115 - 18-bit Parity Memory

The -100 series memories are for use in parity applications where the DEC M7850 or the Plessey PM-7850/100 parity controller is used. These memories can be installed in any of the following backplane units:

- PM-D11/SPC-1 — Double system unit memory and SPC modified Unibus backplane.
- PM-D11/SPC-2 — Single system unit memory and SPC modified Unibus backplane.
- DEC DD11-C — Single system unit memory and SPC modified Unibus backplane.
- DEC DD11-D — Double system unit memory and SPC modified Unibus backplane.
- DEC DD11-P — Double systems unit DEC processor backplane.

Versions 200 Through 207 - 16-bit Non-Parity Memory

The -200 series memories are for use in non-parity applications. They can be installed in any of the following backplanes:

- PM-F11/SPC — Double system unit memory and SPC backplane.
- PM-F11/SPC-1 — Single system unit memory and SPC backplane.
- PM-D11/SPC-1 — Double system unit memory and SPC modified Unibus backplane.
- PM-D11/SPC-2 — Single system unit memory and SPC modified Unibus backplane.
- DEC DD11-C — Single system unit memory and SPC modified Unibus backplane.
- DEC DD11-D — Double system unit memory and SPC modified Unibus backplane.
- DEC DD11-P — Double systems unit DEC processor backplane.

Memory Capacity

Within each of the series listed above, the PM-S1132 is available in versions of different capacities as listed in Table 1-1.

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VERSIONS	MEMORY CAPACITY
107, 115, 207	8K bytes
106, 114, 206	16K bytes
105, 113, 205	24K bytes
104, 112, 204	32K bytes
103, 111, 203	40K bytes
102, 110, 202	48K bytes
101, 109, 201	56K bytes
100, 108, 200	64K bytes

Table 1-1: PM-S1132 Memory Capacities

1.2.3 Battery Back-up Option

The PM-S1132 provides a jumper selectable battery back-up option. With this option, the +5V BAT and +15 BAT terminals on the backplane are routed to the memory in order to sustain the memory during a power fail mode.

1.2.4 Memory Access Time

The access time for the 100-107 and 200-207 versions is 375ns maximum. The access time for the 108-115 versions is 260ns maximum. The access time is defined as the time from when master sync (MSYN) is accepted by the memory to the time the slave sync pulse (SSYN) is asserted by the memory to indicate that data is available.

1.2.5 Memory Cycle Time

The cycle time for the 100-107 and 200-207 versions is 475ns maximum. The cycle time for the 108-115 versions is 425ns maximum. The cycle time is defined as the time from when master sync (MSYN) is accepted by the memory to the time when the memory can accept the next master sync pulse. The refresh conflict time is excluded when defining the cycle time of the memory.

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1.3 MECHANICAL DESCRIPTION

The PM-S1132 memory is designed to fit mechanically into the PDP-11 series computers. It occupies the space of one standard DEC hex printed circuit board and can be installed into consecutive memory slots. The dimensions of the board assembly are 8.875 inches by 15.688 inches.

1.4 MODES OF OPERATION

The PM-S1132 operates in several modes including full word read and write, byte read and write, and read-modify-write. These modes are determined by the state of address bit AØØ and control lines CØ and C1. The modes of operation are described in detail in Section 3; a brief description of each mode is contained in the following text.

- DATI (Read Cycle): In this mode the memory reads data from a specified location and presents this data to the data bus.
- DATO (Write Cycle): In this mode the memory writes new data from the data bus into a specified location in memory.
- DATOB (Write Byte Cycle): In this mode the memory performs a write on a specified byte of data. The other byte of data is not affected.
- DATIP (Read-Modify-Write): In this mode the memory performs two memory cycles: a read (DATI) followed by either a DATO or a DATOB operation as specified by the processor.
- Refresh Cycle: In this mode the memory performs a memory refresh cycle as described below.

1.5 REFRESH CYCLE

The PM-S1132 memory module is designed using 4K-bit dynamic MOS random access memories. Being dynamic, these memories require refreshing. Refresh cycles occur at a periodic rate of approximately 31μsec. That is, every 31μsec the memory is disabled and refreshed at the refresh counter address. Each refresh cycle requires one memory cycle time.

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Should a processor or NPR request occur while a refresh cycle is in progress, this request is stored and accomplished immediately following the refresh cycle. On the other hand, if a 31μsec refresh request occurs while the memory is performing a processor or NPR request the refresh request is stored and accomplished following this cycle. Memory refresh is transparent to Unibus transactions.

1.6 INTERFACE

The input signals to the memory are as follows:

SIGNAL NAME	FUNCTION
MSYNL	Master Sync
CØL, ClL	Control Lines
AØØL - A17L	Address Lines
DØØL - D15L	Data Lines
PAL, PBL or PAR PØ, PAR Pl	Parity Lines
PAR DET	Parity Detect
DCLO	Power Fail

Output signals from the memory are:

SIGNAL NAME	FUNCTION
SSYNL	Slave Sync
INT SSYN	Internal Slave Sync
DØØL - D15L	Data Lines
PAL, PBL or PAR PØ, PAR Pl	Parity Lines

The function of each interface signal is described in Section 3.

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1.7 MEMORY SPECIFICATION

Table 1-2 lists the PM-S1132 specifications.

CHARACTERISTIC	SPECIFICATION
Access Time	375ns (Versions 100-107 & 200-207) 260ns (Versions 108-115)
Cycle Time	475ns (Versions 100-107 & 200-207) 425ns (Versions 108-115)
Interface Signal Levels: High (inactive) Low (active)	 +2.4V to 5.0V 0V to 0.8V
Operating Temperature	0°C to +60°C
Non-Operating Temperature	-40°C to +85°C
Operating Humidity	10% to 90% without condensation
Mechanical Shock	Housed in its shipping container in accordance with MIL-STD-81ØB method 516, procedure V.
Non-Operating Thermal Shock	±25°C per hour maximum
Mechanical Dimensions Width Depth	 15.688 inches 8.875 inches

Table 1-2: PM-S1132 Specifications

1.8 POWER REQUIREMENTS

The PM-S1132 memory is designed to operate on the +15V and +5V power supplies and can be strapped for battery back-up. The maximum power requirements for each 64K byte memory module are shown in Table 1-3.

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VOLTAGE	SELECTED	NON-SELECTED	BATTERY
+5V	2.5A	2.3A	1.7A
+15V	Ø.65A	Ø.52A	Ø.52A

Table 1-3: Power Requirements

DC power for the PM-S1132 is routed as shown in Table 1-4.

DC SUPPLY	PINS
+5V Battery Back-up	BD1
+5V Supply	AA2, BA2, CA2, DA2, EA2, FA2
+15V Battery Back-up	AR1
+15V Supply	CU1

Table 1-4: DC Power Connection

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Section 2

Installation

This section provides information for the installation and operation of the PM-S1132 memory system. It lists the various memory versions available and explains how to incorporate the options. Information for setting the memory to a particular address block is also included.

2.1 UNPACKING AND INSPECTION

The PM-S1132 is shipped in a special packing carton designed to keep the board from receiving excessive mechanical shock and vibration and to give it maximum protection during shipment. The packing carton should be retained in case the memory requires reshipment.

To unpack the memory, remove any packing materials and visually inspect the memory board for physical damage. Check all hardware attached to the board.

2.2 MEMORY VERSIONS

The PM-S1132 is available in 24 different versions as listed in Table 2-1.

2.3 JUMPERS

Jumpers are used to convert memory configurations and enable battery, parity, 30K, and 31K options. All PM-S1132 memories are shipped jumpered for non-battery operation. The user can exercise this option by connecting the appropriate jumpers. Jumper connections are defined below. Table 2-2 describes which connections are to be used for each of these options.

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CAPACITY	CONFIGURATION	PART NUMBER	MODEL NUMBER
8K byte	Parity	700755-107	PM-S1132/107
8K bytes	Parity	700755-115	PM-S1132/115
16K bytes	Parity	700755-106	PM-S1132/106
16K bytes	Parity	700755-114	PM-S1132/114
24K bytes	Parity	700755-105	PM-S1132/105
24K bytes	Parity	700755-113	PM-S1132/113
32K bytes	Parity	700755-104	PM-S1132/104
32K bytes	Parity	700755-112	PM-S1132/112
40K bytes	Parity	700755-103	PM-S1132/103
40K bytes	Parity	700755-111	PM-S1132/111
48K bytes	Parity	700755-102	PM-S1132/102
48K bytes	Parity	700755-110	PM-S1132/110
56K bytes	Parity	700755-101	PM-S1132/101
56K bytes	Parity	700755-109	PM-S1132/109
64K bytes	Parity	700755-100	PM-S1132/100
64K bytes	Parity	700755-108	PM-S1132/108
8K bytes	Non-Parity	700755-207	PM-S1132/207
16K bytes	Non-Parity	700755-206	PM-S1132/206
24K bytes	Non-Parity	700755-205	PM-S1132/205
32K bytes	Non-Parity	700755-204	PM-S1132/204
40K bytes	Non-Parity	700755-203	PM-S1132/203
48K bytes	Non-Parity	700755-202	PM-S1132/202
56K bytes	Non-Parity	700755-201	PM-S1132/201
64K bytes	Non-Parity	700755-200	PM-S1132/200

Table 2-1: PM-S1132 Versions

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JUMPERS	FUNCTION
W1 to W2	Enables PAL
W1 to W3	Enables PAR PØ
W4 to W5	Enables PBL
W4 to W6	Enables PAR P1
W7 to W8	Enables PAR DET
W9 to W10	Connects memory to +5VDC battery option for battery back-up
W9 to W11	Connects battery back-up circuitry to +5VDC power supply
W12 to W13	Connects +15VDC circuitry to power supply
W12 to W14	Connects memory to +15VDC battery option for battery back-up
W15 to W16	Enables 30K and 31K options
W25 to W26	Enables 31K option

FUNCTION	JUMPER CONNECTIONS
Modified Unibus (100 series) Battery Option No battery Option	 W1-W3, W4-W6, W7-W8, W9-W10, W12-W14 W1-W3, W4-W6, W7-W8, W9-W11, W12-W13
Standard Unibus (200 series)	W9-W11, W12-W13
30K Option	Cut etch between U169-1 and U169-2 on the solder side of the memory board and add W15 to W16.
31K Option	Cut etch between U169-1 and U169-2 on the solder side of the memory board and add W15 to W16. Cut etch between U188-5 and U188-6 on the solder side of the memory board and add W25 to W26.

*The battery option is not available for the Standard Unibus.

Table 2-2: Jumper Connections for Memory Configurations

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Jumpers are also used to configure row select options used for addressing the different memory versions. The connections are defined in Table 2-3.

VERSION	JUMPER CONNECTIONS
8K bytes (107, 115, 207)	WA to WF, WA to WH, and WB to WD. WA and WB are Grounds.
16K bytes (106, 114, 206)	WA to WF, WB to WH, and WC to WD
24K bytes (105, 113, 205) 32K bytes (104, 112, 204)	WA to WF, WC to WD, and WG to WH
40K bytes (103, 111, 203) 48K bytes (102, 110, 202) 56K bytes (101, 109, 201) 64K bytes (100, 108, 200)	WE to WF, WG to WH, and WC to WD

Table 2-3: Jumper Connections for Row Select Options

2.4 MEMORY INSTALLATION

The PM-S1132 can be installed in any of the following computers:

CPU TYPE	CHASSIS SIZE	COMPUTER TOTAL MEMORY CAPACITY
PDP-11/05, 11/10	5.25 x 10.5"	56K bytes
PDP-11/35 11/40	10.5 x 21"	248K bytes
PDP-11/45, 11/50, 11/55	21"	248K bytes
PDP-11/04	5.25 x 10.5"	56K bytes
PDP-11/34	5.25 x 10.5"	248K bytes
PDP-11/60		248K bytes

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The PM-S1132 can also be installed in the following expansion chassis: Plessey PM-1150/2A, PM-1150/4, PM-1150/4A, PM-1150/5, PM-1150/6, and the DEC BA11-K. It is compatible with conventional or modified Unibus backplanes, including: Plessey PM-F11/SPC, PM-F11/SPC-1, PM-D11/SPC-1, PM-D11/SPC-2, DEC DD11-C, DD11-D, and DD11-P.

The PM-S1132 cannot be installed in the PM-F11/SPC backplane slots 7 and 8. In the other backplanes, the PM-S1132 can be installed in any slot except the first and last slots which are used for Unibus cable and/or termination card. In the Unibus backplane system, the first and last slots are wired as standard Unibus for Unibus-in and Unibus-out connection. The Unibus pin assignments are listed in Table 2-4.

2.5 ADDRESS SELECTION

Each memory must be set to respond to specific address locations. Since all the memories on the Unibus receive master sync simultaneously, address selection is necessary so that only the selected memory will respond.

The PM-S1132 address selection is set in 8K byte memory block increments from 0 to 248K bytes. (Memory selection between 248K and 256K bytes is always inhibited since this block is reserved for I/O addresses only). Address selection is accomplished using a ten position DIP switch. Switches one through five are used to set the lower limit address, and switches six through ten are used to set the upper limit address of the memory.

Table 2-5 lists the starting and ending address switch settings for the PM-S1132.

NOTE: The following memory versions can only be addressed on 64K byte blocks and must be the starting memory for each block: 24K, 40K, 48K, and 56K byte memory versions.

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CONNECTOR A			
		A2	+5V
BUS DØØ L	C1	C2	GND
BUS DØ2 L	D1	D2	BUS DØ1 L
BUS DØ4 L	E1	E2	BUS DØ3 L
BUS DØ6 L	F1	F2	BUS DØ5 L
BUS DØ8 L	H1	H2	BUS DØ7 L
BUS D1Ø L	J1	J2	BUS DØ9 L
BUS D12 L	K1	K2	BUS D11 L
BUS D14 L	L1	L2	BUS D13 L
BUS PA L	M1	M2	BUS D15 L
PAR P1	N1	N2	BUS PB L
PAR PØ	P1		
+15 BAT	R1		
GND	T1	T2	

Table 2-4a: Interface Connections

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CONNECTOR B			
		A2	+5V
		C2	GND
+5V BAT	D1		
INT SSYN	E1		
		F2	DCLO
BUS AØ1 L	H1	H2	BUS AØØ L
BUS AØ3 L	J1	J2	BUS AØ2 L
BUS AØ5 L	K1	K2	BUS AØ4 L
BUS AØ7 L	L1	L2	BUS AØ6 L
BUS AØ9 L	M1	M2	BUS AØ8 L
BUS A11 L	N1	N2	BUS A1Ø L
BUS A13 L	P1	P2	BUS A12 L
BUS A15 L	R1	R2	BUS A14 L
BUS A17 L	S1	S2	BUS A16 L
GND	T1	T2	BUS CØ1 L
BUS SSYNL	U1	U2	BUS CØØ L
BUS MSYNL	V1		

Table 2-4b: Interface Connections

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CONNECTORS C, D, E, AND F	
PIN	SIGNAL
CA2, DA2	+5V
EA2, FA2	+5V
CC2, DC2	GND
EC2, FC2	GND
CT1, DT1	GND
ET1, FT1	GND
CU1 (Conventional Unibus)	+15V
DK2	BG7 IN
DL2	BG7 OUT
DM2	BG6 IN
DN2	BG6 OUT
DP2	BG5 IN
DR2	BG5 OUT
DS2	BG4 IN
DT2	BG4 OUT

Table 2-4c: Interface Connections

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STARTING							ENDING ADDRESS						
OCTAL	DECIMAL BYTES	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	OCTAL	DECIMAL BYTES	SW1-6	SW1-7	SW1-8	SW1-9	SW1-10
000000	0K	ON	ON	ON	ON	ON	017776	8K	OFF	ON	ON	ON	ON
020000	8K	OFF	ON	ON	ON	ON	037776	16K	ON	OFF	ON	ON	ON
040000	16K	ON	OFF	ON	ON	ON	057776	24K	OFF	OFF	ON	ON	ON
060000	24K	OFF	OFF	ON	ON	ON	077776	32K	ON	ON	OFF	ON	ON
100000	32K	ON	ON	OFF	ON	ON	117776	40K	OFF	ON	OFF	ON	ON
120000	40K	OFF	ON	OFF	ON	ON	137776	48K	ON	OFF	OFF	ON	ON
140000	48K	ON	OFF	OFF	ON	ON	157776	56K	OFF	OFF	OFF	ON	ON
160000	56K	OFF	OFF	OFF	ON	ON	177776	64K	ON	ON	ON	OFF	ON
200000	64K	ON	ON	ON	OFF	ON	217776	72K	OFF	ON	ON	OFF	ON
220000	72K	OFF	ON	ON	OFF	ON	237776	80K	ON	OFF	ON	OFF	ON
240000	80K	ON	OFF	ON	OFF	ON	257776	88K	OFF	OFF	ON	OFF	ON
260000	88K	OFF	OFF	ON	OFF	ON	277776	96K	ON	ON	OFF	OFF	ON
300000	96K	ON	ON	OFF	OFF	ON	317776	104K	OFF	ON	OFF	OFF	ON
320000	104K	OFF	ON	OFF	OFF	ON	337776	112K	ON	OFF	OFF	OFF	ON
340000	112K	ON	OFF	OFF	OFF	ON	357776	120K	OFF	OFF	OFF	OFF	ON
360000	120K	OFF	OFF	OFF	OFF	ON	377776	128K	ON	ON	ON	ON	OFF
400000	128K	ON	ON	ON	ON	OFF	417776	136K	OFF	ON	ON	ON	OFF
420000	136K	OFF	ON	ON	ON	OFF	437776	144K	ON	OFF	ON	ON	OFF
440000	144K	ON	OFF	ON	ON	OFF	457776	152K	OFF	OFF	ON	ON	OFF
460000	152K	OFF	OFF	ON	ON	OFF	477776	160K	ON	ON	OFF	ON	OFF
500000	160K	ON	ON	OFF	ON	OFF	517776	168K	OFF	ON	OFF	ON	OFF
520000	168K	OFF	ON	OFF	ON	OFF	537776	176K	ON	OFF	OFF	ON	OFF
540000	176K	ON	OFF	OFF	ON	OFF	557776	184K	OFF	OFF	OFF	ON	OFF
560000	184K	OFF	OFF	OFF	ON	OFF	577776	192K	ON	ON	ON	OFF	OFF
600000	192K	ON	ON	ON	OFF	OFF	617776	200K	OFF	ON	ON	OFF	OFF
620000	200K	OFF	ON	ON	OFF	OFF	637776	208K	ON	OFF	ON	OFF	OFF
640000	208K	ON	OFF	ON	OFF	OFF	657776	216K	OFF	OFF	ON	OFF	OFF
660000	216K	OFF	OFF	ON	OFF	OFF	677776	224K	ON	ON	OFF	OFF	OFF
700000	224K	ON	ON	OFF	OFF	OFF	717776	232K	OFF	ON	OFF	OFF	OFF
720000	232K	OFF	ON	OFF	OFF	OFF	737776	240K	ON	OFF	OFF	OFF	OFF
740000	240K	ON	OFF	OFF	OFF	OFF	757776	248K	OFF	OFF	OFF	OFF	OFF

NOTE: TO DISABLE THE MEMORY FROM BEING SELECTED, SWITCHES POSITION SW1-1 TO SW1-5 AND SW1-6 TO SW1-10 SHOULD BE THE SAME.

Table 2-5: Address Switch Settings

Section 3

Functional Description

3.1 INTRODUCTION

This section describes the operation of the PM-S1132 memory system. Figure 3-1 contains an overall block diagram of the system. The diagram shows the relationship between the timing and control, address selection, memory array, and refresh circuitry.

3.2 DATA TRANSFER SEQUENCE

This subsection describes the data transfer sequence between the memory and a bus master.

The memory receives commands, address, and data information from the Unibus. The bus master places address data and control information on the Unibus lines, waits 150ns to allow for bus delay (front-end deskew) and memory internal decode delay, and then initiates master sync (MSYN).

The memory decodes the address information from the bus and if it does not fall within the memory's address, MSYN is blocked. The memory is not accessed and therefore remains in a stand-by state.

- For a read cycle (DATI) the following sequence takes place: The bus master places address and control information on the Unibus, waits 150ns for front-end deskew and then initiates MSYN.

  The memory decodes the address and begins a memory cycle. When data is available (access time) the memory places the data on the bus and asserts SSYN. The bus master receives SSYN, waits for a minimum of 75ns (data deskew) and then strobes data and negates MSYN. The memory receives the cleared MSYN and removes the data from the bus and clears SSYN.

  After a 75ns minimum delay the (tail-end deskew) bus master removes address and control lines from the bus. The bus is now free and may be requested by another bus master. All bus masters must go through the priority arbitration circuit at the processor in order to gain control of the bus.

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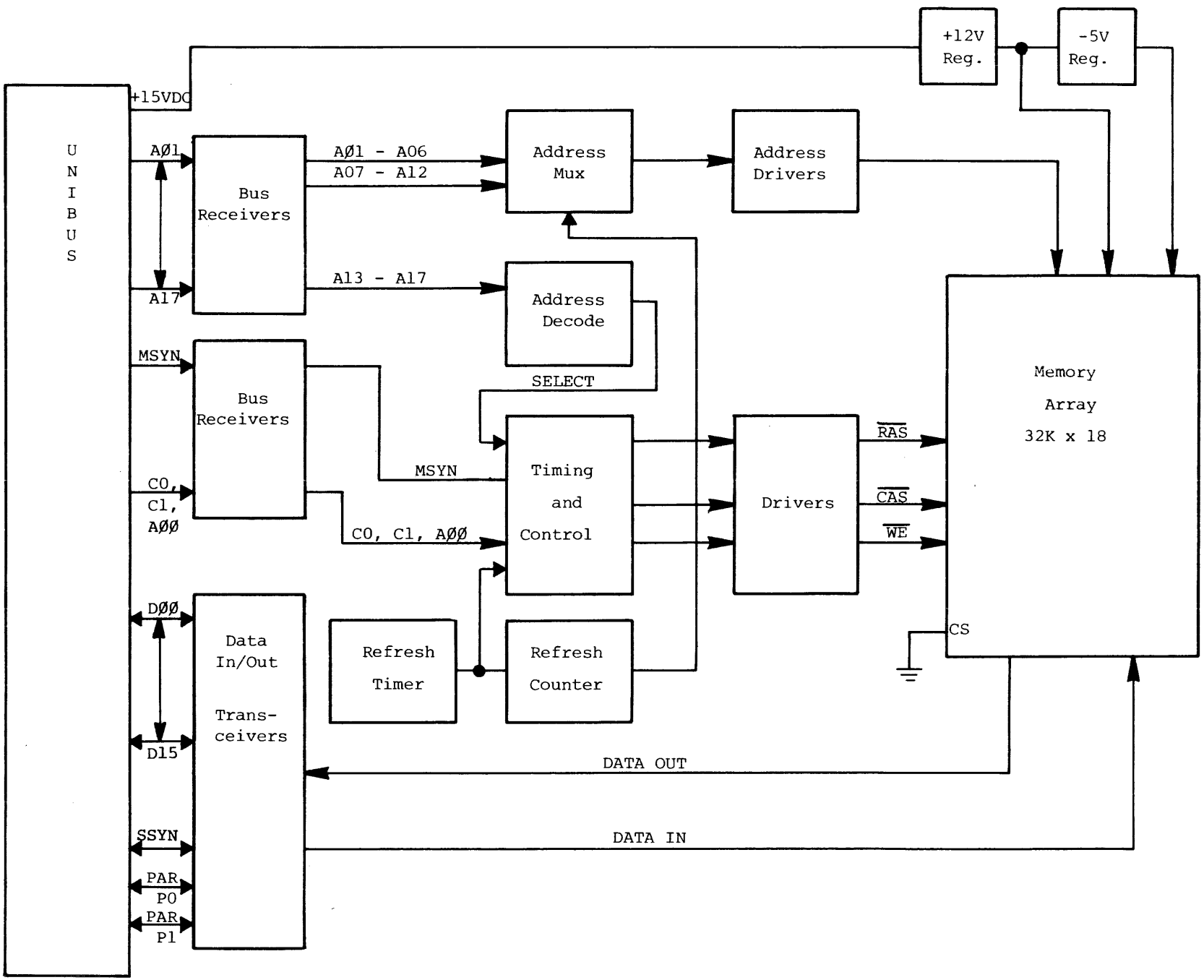

Figure 3-1: PM-S1132 System Block Diagram

- For a write cycle (DATO or DATOB) the following sequence takes place: The bus master places address, data and control information on the Unibus lines, waits for at least 150ns (front-end deskew) and then initiates MSYN.

  The memory decodes the address information from the bus and begins a memory cycle after receiving MSYN. At access time SSYN is asserted by the memory. Upon receipt of the asserted SSYN, the bus master negates MSYN which may remove the data from the data bus.

  After a 75ns minimum delay (tail-end deskew) the bus master removes address and control lines from the bus. The bus is now free and may be requested by another bus master.

  When SSYN is asserted by the memory (access time) the memory will continue its cycle and cannot be accessed until the cycle is complete. If an MSYN from the Unibus is asserted while the memory is in a cycle, the memory accepts the new command after completion of the cycle. This mode of operation (bus master waiting to start memory cycle) can occur only when a refresh cycle is being performed by the memory.

Unlike core, MOS memory provides non-destructive readouts. Therefore, the write-after ready cycle time associated with core memory is eliminated. By the time a new bus cycle is started, the MOS memory has completed its cycle and is ready to accept new commands from the Unibus.

3.3 INTERFACE SIGNALS

The memory interfaces with the processor and peripherals via card edge connectors on the bottom of the memory card. The memory inputs interface with the processor via Unibus compatible bus receivers and transceivers. The receivers and transceivers present one bus load to the Unibus. Output signals are driven by open collector drivers and Unibus transceivers. The interface signals are described in Table 3-1. Interface timing is shown in Figures 3-1 and 3-2.

3.4 MODES OF OPERATION

The two control lines CØ and C1 in conjunction with address bit AØØ are used to select one of six modes of operation. Table 3-2 lists the modes of operation. Each mode is described in the following text.

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SIGNAL	FUNCTION
BUS MSYN	MASTER SYNC: The application of MSYN when the memory is not busy initiates a memory cycle if the memory is addressed.
BUS CØL, BUS C1L	CONTROL LINES: The state of these two lines in conjunction with address input line AØØ determines the memory mode of operation. The control lines must be stable a minimum of 75ns before MSYN is asserted and remain stable until MSYN is removed.
BUS AØØL through A17L	ADDRESS LINES: Addressing of the memory is accomplished via 18 unidirectional address input lines identified as AØØL through A17L. AØØL is used for byte selection in the DATOB mode. AØ1L through A12L are used to decode one of 4096 address locations within the memory. A13L through A17L are used to define the starting and ending address of the memory. Addresses A13L through A17L are switch-selectable to any starting and ending addresses from 0 to 124K in 4K boundaries. The address inputs must be stable a minimum of 75ns before MSYN is asserted and remain stable until MSYN is removed.
BUS DØØL through BUS D15L	DATA LINES: The data lines are bidirectional lines on which data is carried to and from the memory. In the DATO and DATOB modes, data to the memory must be stable a minimum of 75ns before MSYN is asserted and remain stable until SSYN is asserted. In the DATI and DATIP modes, data is output from the memory on these lines. The data-out is stable at access time and remains stable until MSYN is removed.

Table 3-1a: Interface Signal Function

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SIGNAL	FUNCTION
BUS PAL, BUS PBL, OR PAR PØ, PAR P1	PARITY BITS: These are parity bits. PAL and PBL are used for bytes 0 and 1 for the standard Unibus; PAR PØ and PAR P1 are used for bytes 0 and 1 with the modified Unibus.
BUS SSYN	SLAVE SYNC: The slave sync signal is used to acknowledge access to the processor. SSYN is asserted by the memory at access time during a read or write cycle and remains asserted until MSYN is removed.
DCLO	POWER FAIL: DCLO is initiated by the power supply and is available to all units on the Unibus. This signal remains high so long as all power supply DC voltages are within specified limits. DCLO is asserted by the power supply. When DCLO is asserted, it causes memory access to be blocked and switches the memory to a non-selectable mode or to a battery back-up mode if battery back-up is being utilized.
PAR DET L	PARITY DETECT: This signal is grounded on the modified Unibus whenever a parity controller is installed. The PAR DET L signal causes the memory to output an INT SSYNL instead of BUS SSYNL.
INT SSYNL	INTERNAL SLAVE SYNC: This signal is generated by the memory when the parity controller is present on the modified Unibus. Its function is to notify the parity controller that data from the memory is present or has been received. The parity controller generates or checks parity then sends BUS SSYNL to the central processor.

Table 3-1b: Interface Signal Function

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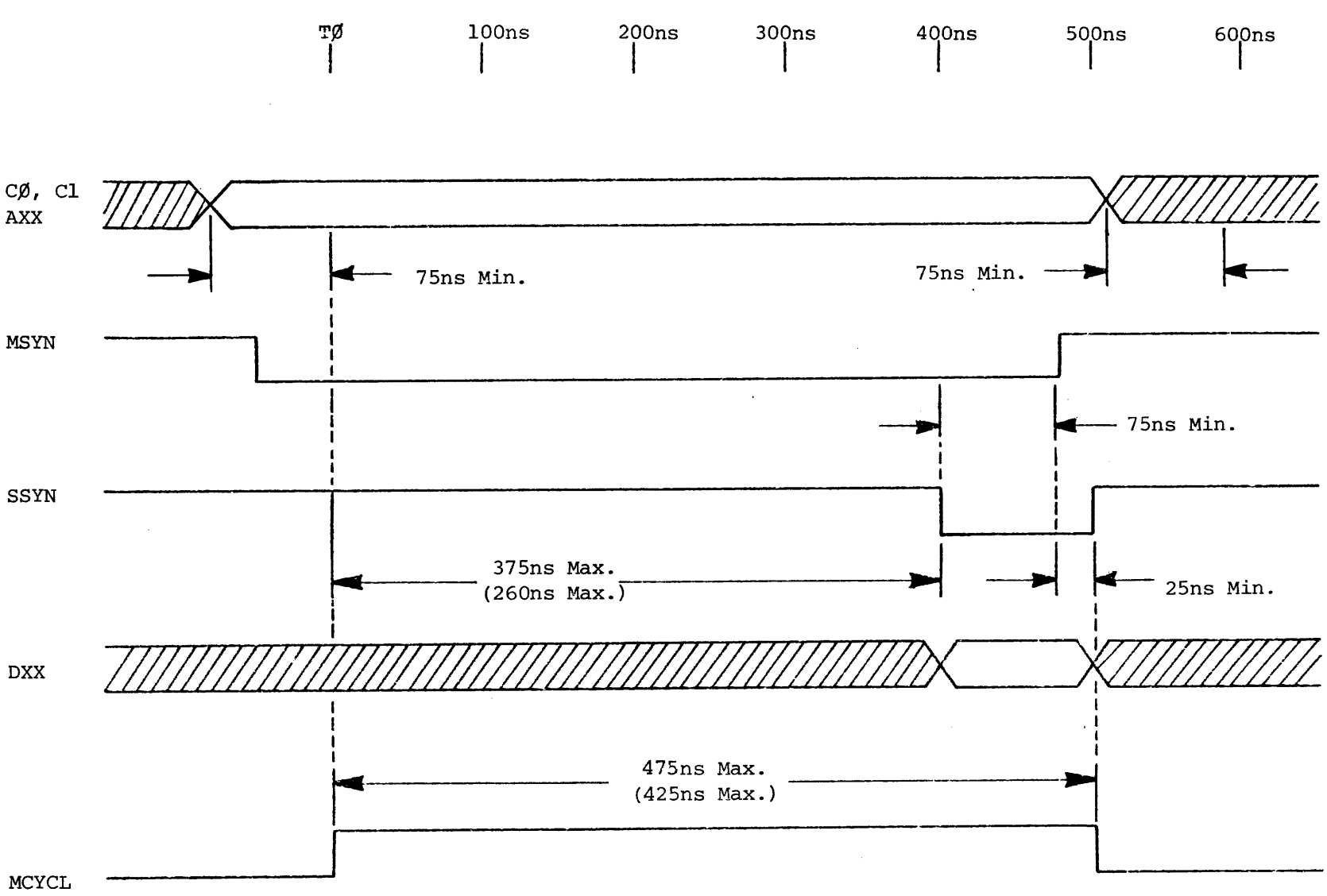

MCYCL - Denotes memory cycle

Means - May be high or low but must be stable

( ) Indicates timing for Versions 108-115.

Means - Value is irrelevant

Figure 3-2: PM-S1132 DATI (READ) TIMING

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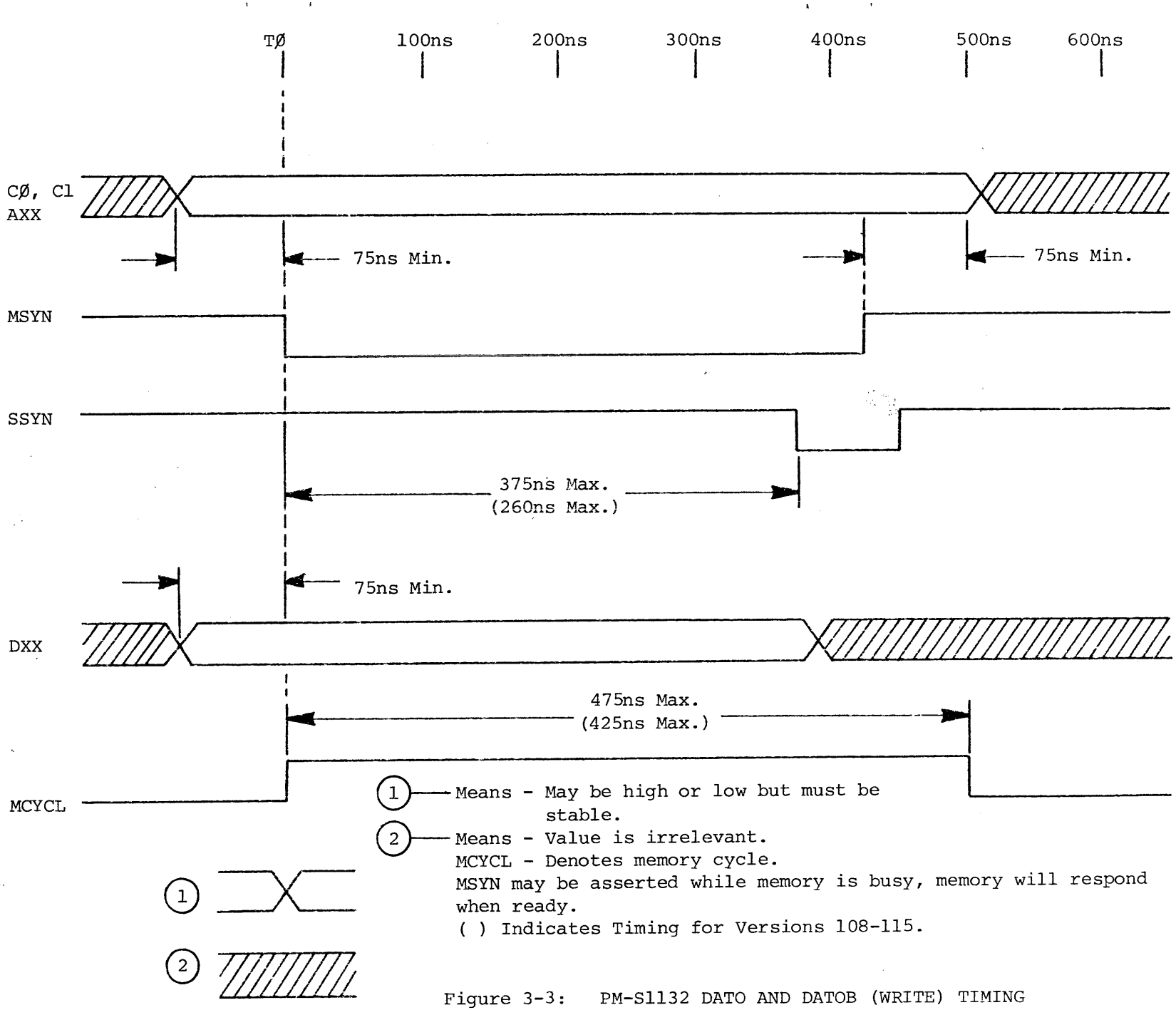
SIZE A | CODE IDENT NO. 52648 | DWG NO. MA 700755 | REV | SCALE | SHEET 3-7



1 — Means - May be high or low but must be stable.

2 — Means - Value is irrelevant.

MCYCL - Denotes memory cycle.

MSYN may be asserted while memory is busy, memory will respond when ready.

( ) Indicates Timing for Versions 108-115.

Figure 3-3: PM-S1132 DATO AND DATOB (WRITE) TIMING

BUS FUNCTION	MENEMONIC	AØ	C1	CØ	MEMORY FUNCTION
Data In	DATI	X*	0	0	Read
Data In Pause	DATIP	X	0	1	Read-modify-write
Data Out	DATO	X	1	0	Write
Data Out Byte Ø	DATOBØ	0	1	1	Write byte Ø
Data Out Byte 1	DATOB1	1	1	1	Write byte 1
Refresh	REF	X	X	X	Refresh Cycle

*Where X indicates that the value is irrevelant

Table 3-2: Memory Modes of Operation

3.5 TIMING AND CONTROL

The master sync pulse (MSYNL) from the bus master initiates the memory cycle providing that the memory is not cycling or in a refresh cycle. The PM-S1132 generates its own internal timing as shown in Figure 3-3.

For a read cycle, $\overline{WE}$ is high. It is decoded from the state of the control lines CØ and C1 on the Unibus. For a write cycle $\overline{WE}$ is low. Data-in is latched at the negative transition (leading edge) of CAS.

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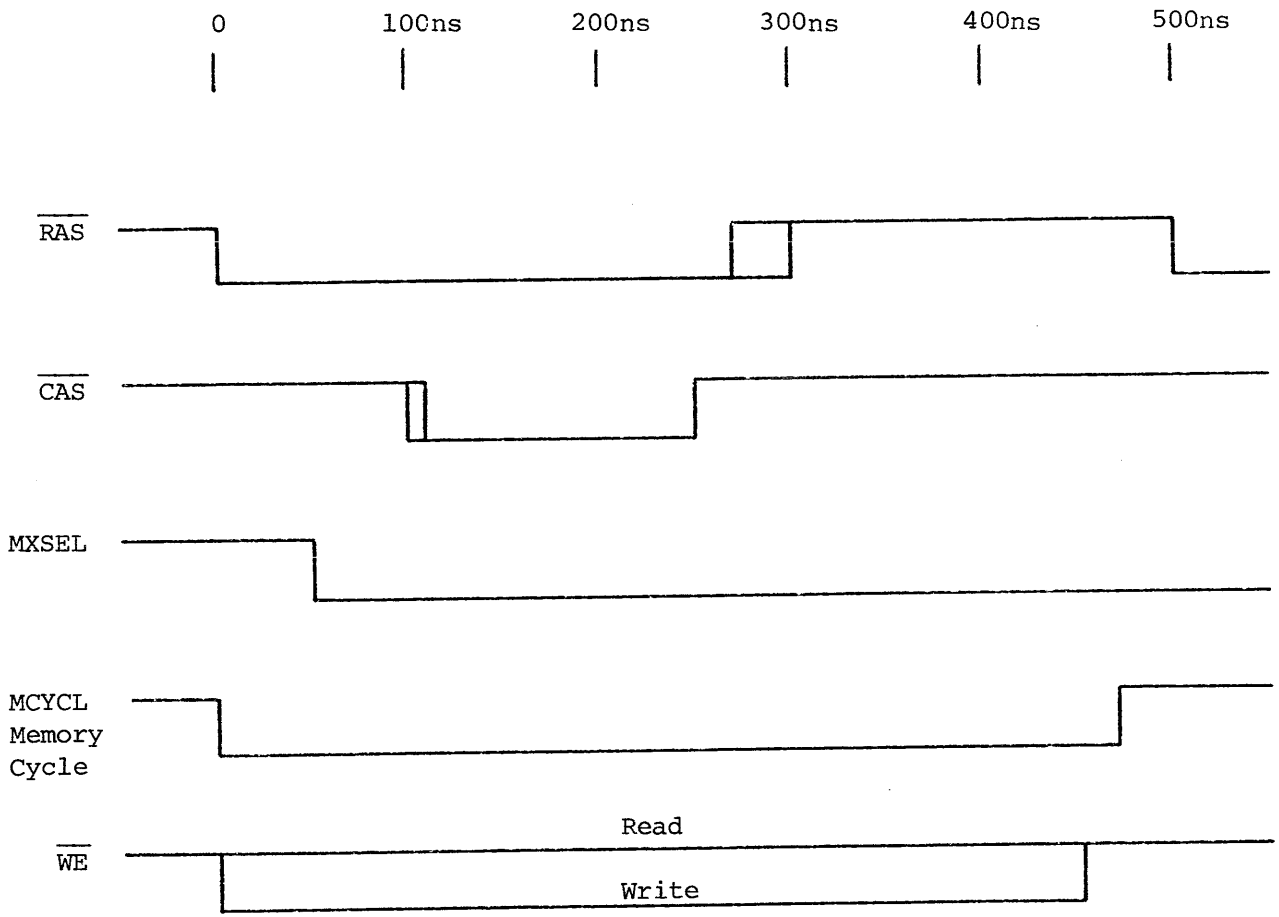

Figure 3-4: PM-S1132 Internal Timing

Section 4

Theory of Operation

This section describes the logic diagrams for the PM-S1132 memory. The logic diagrams are contained in the appendix and are referenced by sheet number throughout the section.

4.1 MEMORY ARRAY

The memory array contains 4096 x one bit, N-channel, MOS memory devices. There are eight rows of 18 of these devices on a 64K byte parity memory. Different versions can be configured by depopulating these rows.

4.2 ADDRESS SELECTION CIRCUIT (SCHEMATIC SHEET 2)

The address selection circuit of the PM-S1132 memory compares the Unibus address contained on the address lines with a pre-selected address block set on the board. The address block is selected on the memory using a ten-position DIP switch designated SW1. The memory block is selectable in 4K increments from 0 to 124K. Address switch settings are listed in Table 2-4.

Figure 4-1 illustrates the address selection circuit. The circuit contains two five bit comparators: U183 and U184. Comparator U184 is used to select the lower limit block, the starting address of memory. U183 is used to select the upper limit block, the ending address of memory.

The output of lower limit comparator U184 is low when the Unibus address is equal to or greater than the pre-selected address in switch SW1 positions one through five. A low at the output of the lower limit comparator U184 enables the upper limit comparator U183, a high at the output of the lower comparator disables the upper limit comparator.

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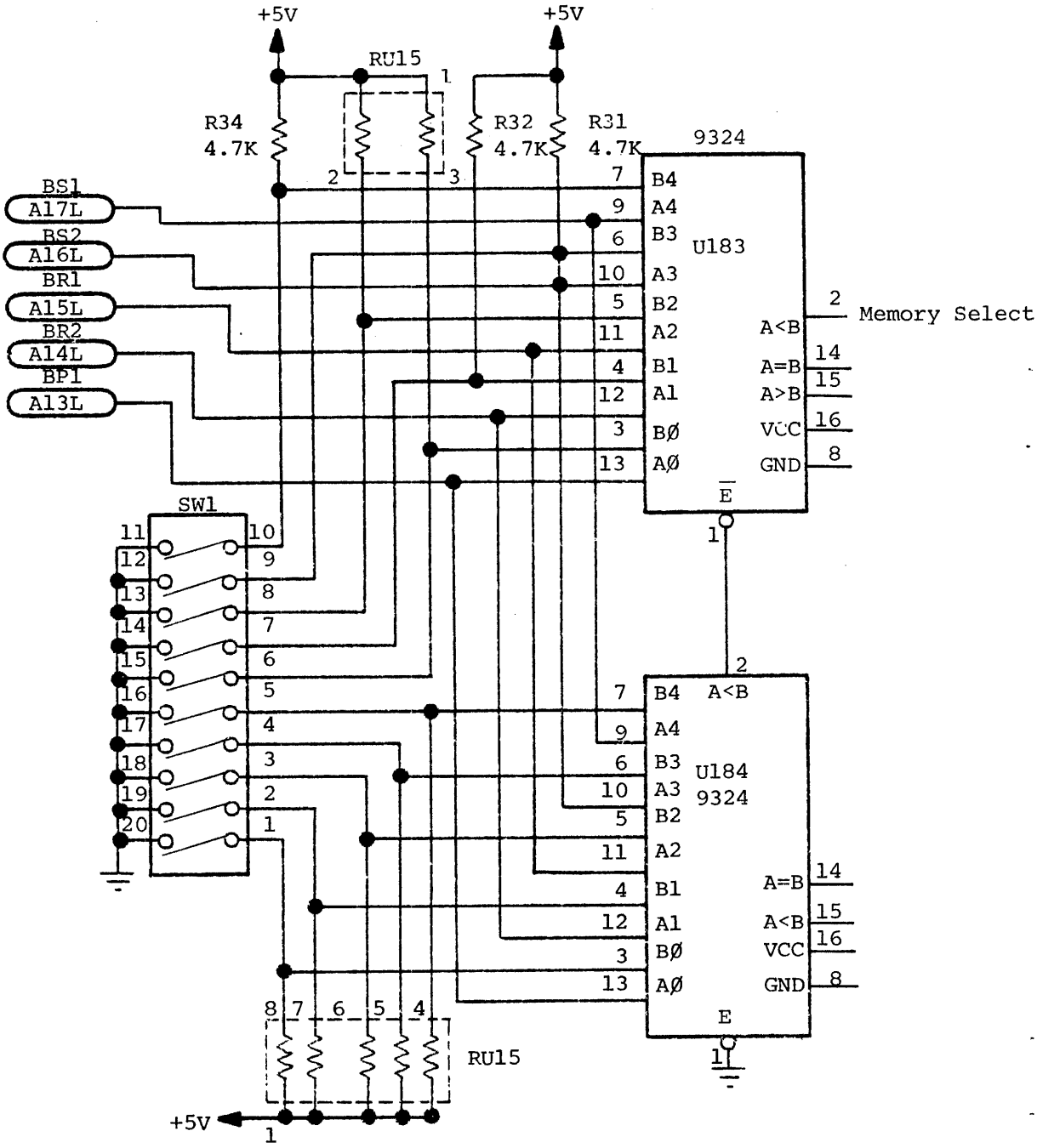

Figure 4-1: Address Selection Circuit

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A	52648	MA 700755
SCALE	REV	SHEET 4-2

The output of the upper limit comparator U183 is high only if the Unibus address is less than the pre-selected address in switch SW1 positions six through ten and the output of the lower limit comparator is low.

4.3 MEMORY SELECT CIRCUIT (SCHEMATIC SHEET 2)

The PM-S1132 memory is selected only when the Unibus master issues an address which falls within the address block to which the memory is set. A master sync pulse (MSYN) from the Unibus starts the memory cycle if the following conditions are true:

- The memory is not currently performing either a memory cycle or a refresh cycle.
- Slave sync from the previous cycle has been cleared.
- The memory is set to respond to the address block addressed by the bus master.

Figure 4-2 illustrates the memory select functions of the PM-S1132.

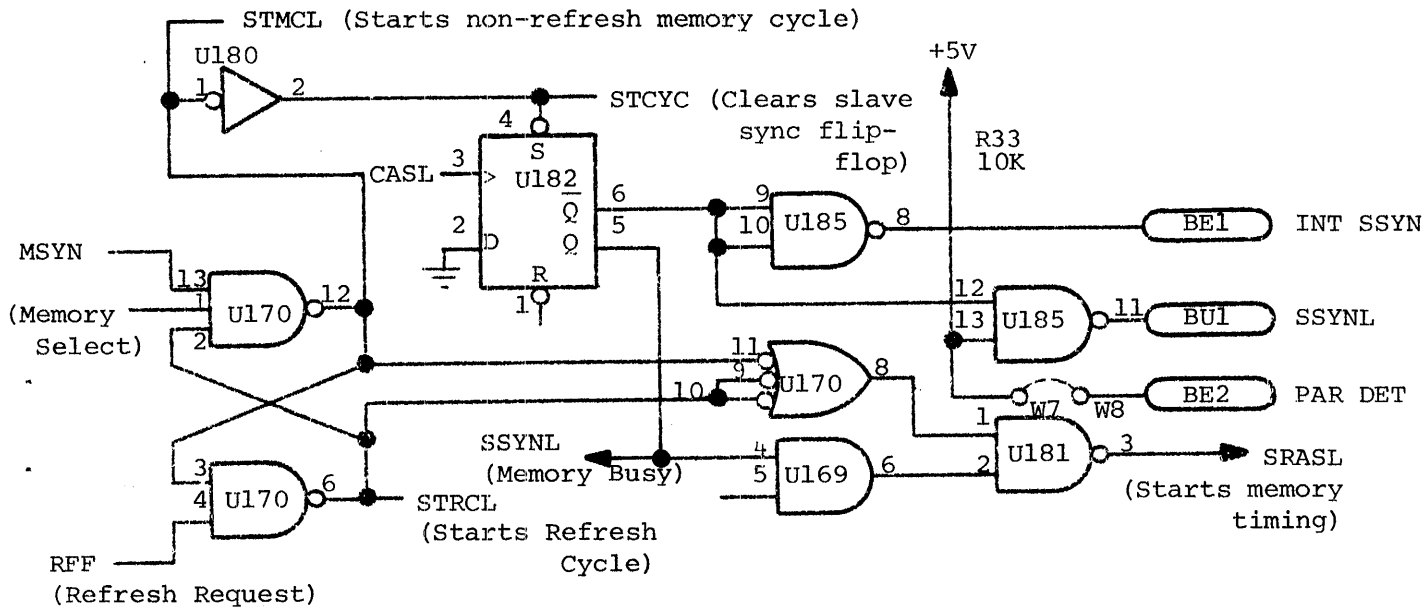

Figure 4-2: Memory Select Circuit

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV	SHEET 4-3

FORM 000021

4.4 MEMORY TIMING CIRCUITS (SCHEMATIC SHEET 2)

Memory timing is initiated by master sync (MSYN) whenever all of the conditions for cycle initiate are met. Memory and refresh cycle timing are initiated as shown in Figure 4-2.

The timing required for the PM-S1132 MOS semiconductor memory is generated as shown in Figure 4-3. The timing signals generated and their functions are listed below:

SIGNAL	DEFINITION	FUNCTION
RAS	Row address strobe	Starts the memory cycle and latches the row address bits A12-AØ7 into the MOS RAMS.
CAS	Column address strobe	Latches the column address to bits AØ6-AØ1 and data during a write cycle into the MOS RAMS
MXSL	Multiplexer select	Multiplexes the row and column address bits A12-AØ1 into the address inputs of the MOS RAM IC's.
	Memory Busy	Blocks any new memory initiation commands during a memory or refresh cycle. Indicates that the memory is busy and still cycling.

4.5 MEMORY REFRESH CIRCUIT (SCHEMATIC SHEET 2)

Refresh of the memory array is accomplished by performing a memory cycle at each of the 64 row addresses within each two millisecond time interval. The timing of the PM-S1132 refresh circuit insures that all row addresses are selected for refresh within the two millisecond time frame. This is accomplished by requesting a refresh cycle approximately every 30µs. The PM-S1132 refresh circuit is as shown in Figure 4-4.

Refresh timer IC U167 is set to trigger at a periodic rate of approximately every 30µs. This sets the refresh flip-flop output U168-9 to indicate that a refresh cycle is pending. The output of timer U167 is also connected to the reset input of the refresh flip-flop allowing a power-on reset

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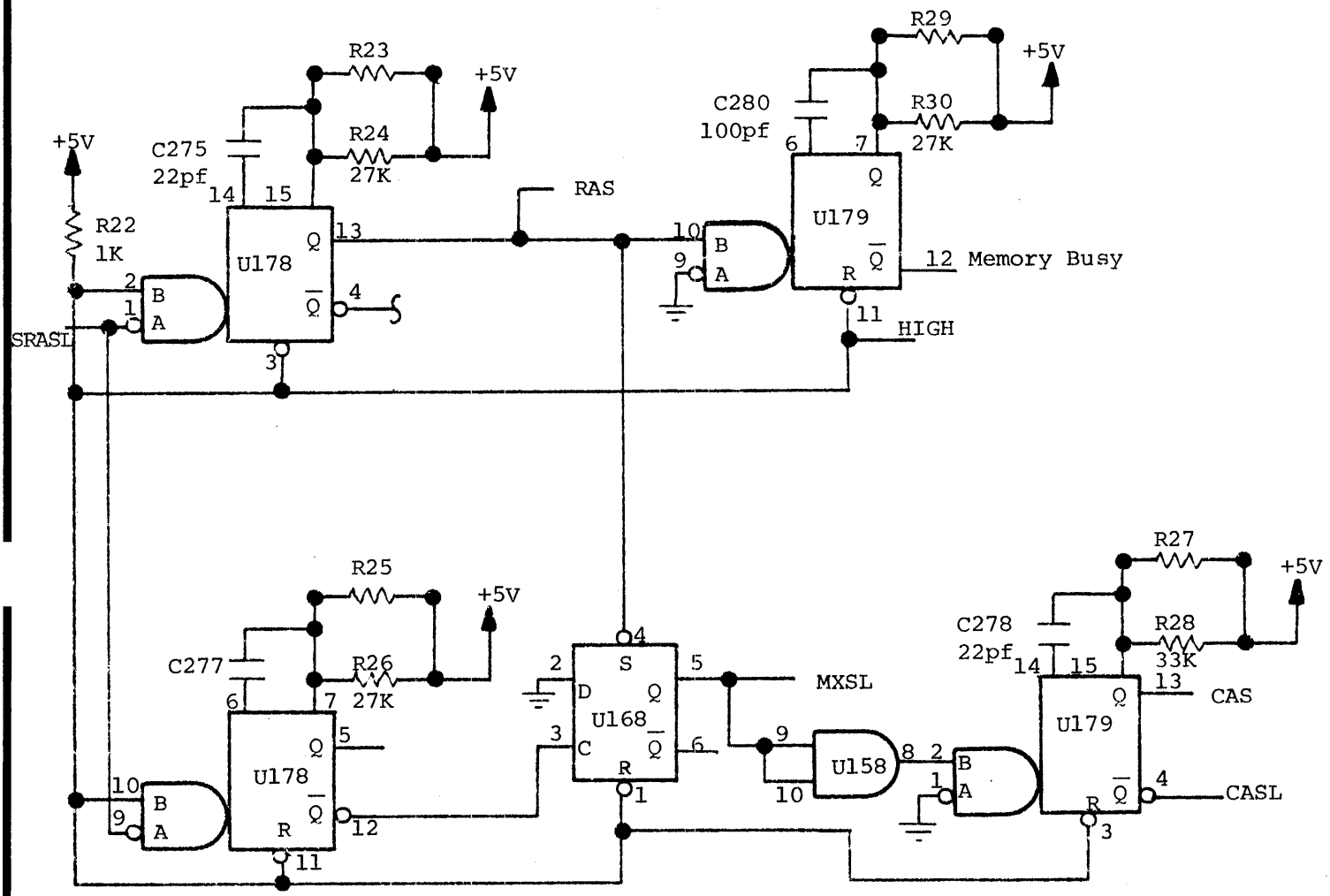

Figure 4-3: Timing Requirements for the PM-S1132 MOS Semiconductor Memory

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET 4-5

condition. The refresh flip-flop is set by the trailing edge of the timer output pulse.

Signal STRC at the input of U158-5 is high only during a refresh cycle. This causes the timing pulse CAS at U158-4 to reset the refresh flip-flop after one cycle of refresh. The refresh circuit initiates one cycle of refresh approximately every 30μs.

A six bit refresh counter is used to refresh the 64 row addresses of the MOS RAM's. The counter circuit is shown in Figure 4-5. U174 and U175 are four bit counters which are connected in series to function as a six bit counter. The counter is incremented once for each refresh cycle.

The time span between refresh cycles is approximately 30μs, thus generating one refresh cycle for each of the 64 row addresses within a 2ms time interval.

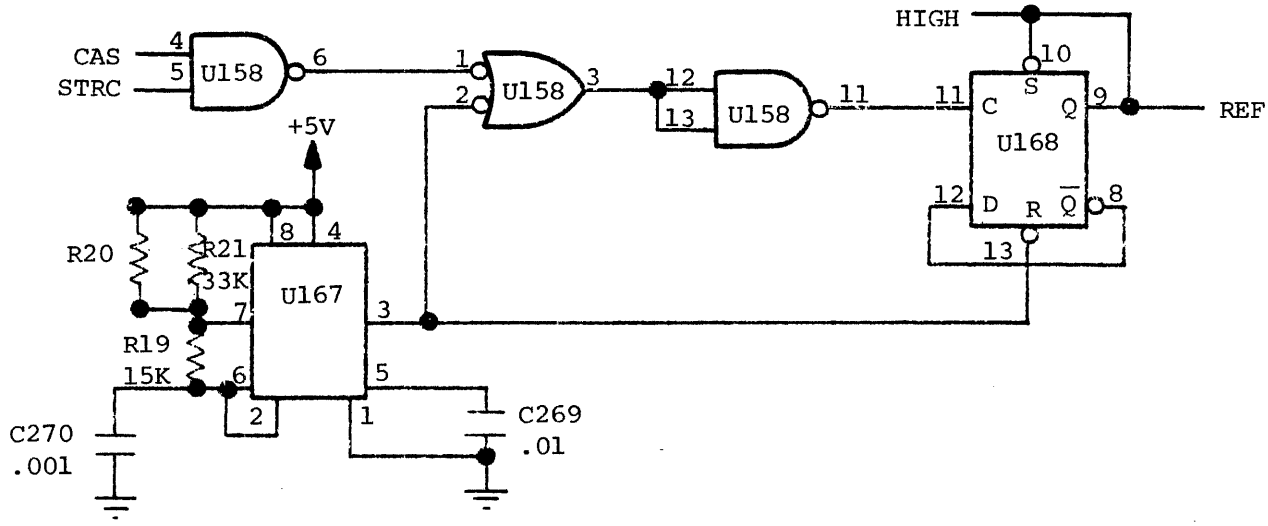

Figure 4-4: Memory Refresh Circuit

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET 4-6

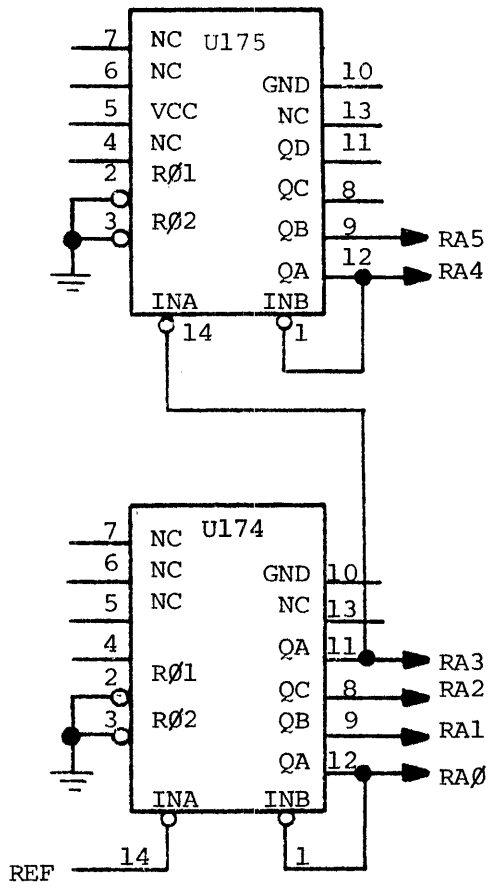

Figure 4-5: Refresh Counter Circuit

4.6 ADDRESS MULTIPLEXING (SCHEMATIC SHEET 3)

The 12 address bits required to decode one of the 4096 cell locations within the 4K RAM's are multiplexed onto six common address lines. The multiplexer circuit is shown in Figure 4-6. U163 through U165 are dual four line to one line data selectors/multiplexers. The select inputs at pin two and pin fourteen select one of four inputs for the multiplexer as shown in Table 4-1.

Input select pin two (STMCL) is low for a memory cycle and high for a refresh cycle. The refresh address is generated by the refresh counter U174 and U175. Input select pin 14 (MXSL) is high at the beginning of the cycle to enable the row address bits AØ1 through A12. After a pre-determined delay,

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SIZE	CODE IDENT NO.	DWG NO.
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SCALE	REV	SHEET 4-7

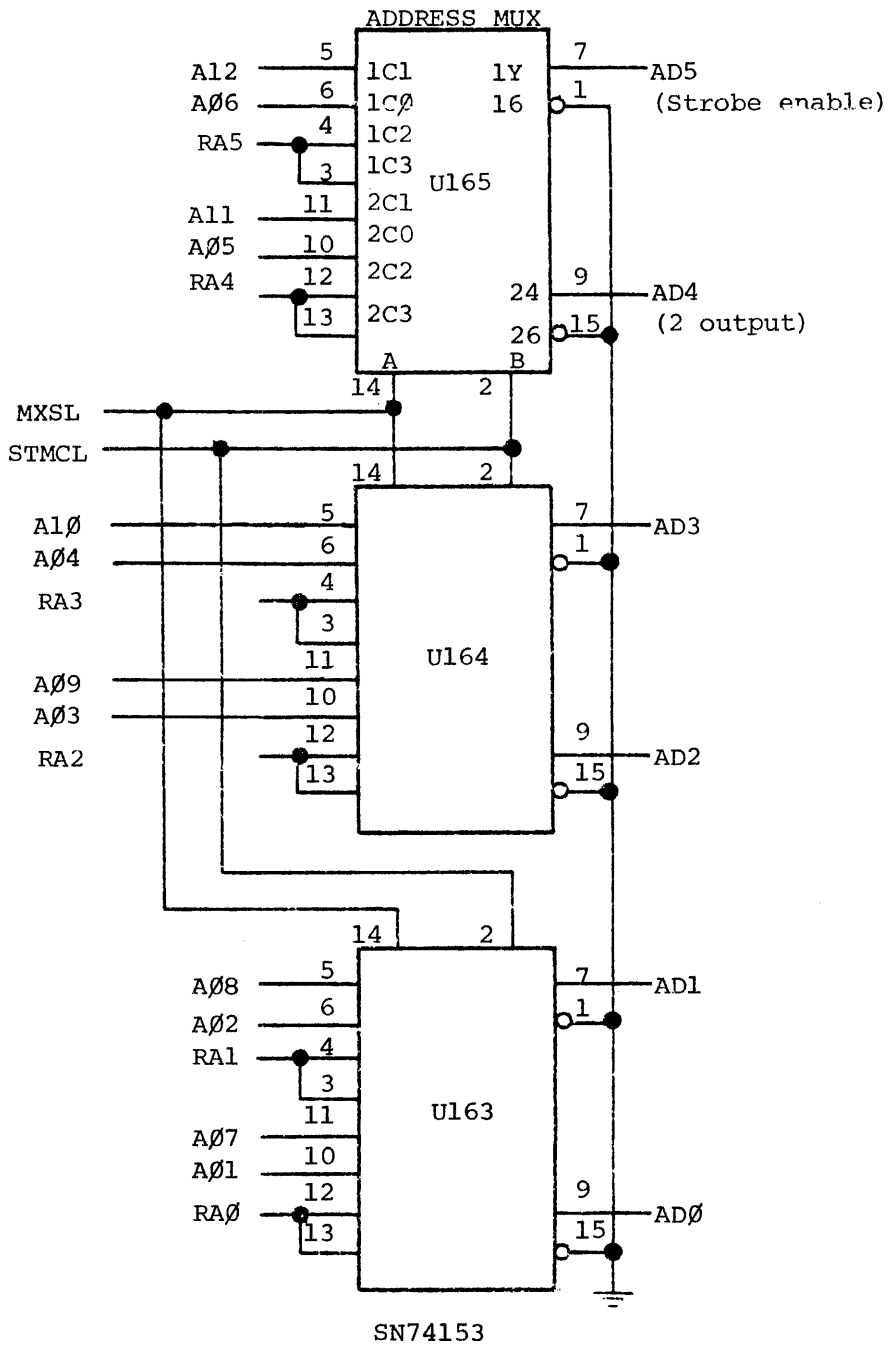

Figure 4-6: Address Multiplexer

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV	SHEET 4-8

pin 14 (MXSL) goes low to enable the column address bits AØ1 through AØ6.

SELECT INPUTS			DATA INPUTS			STROBE	OUTPUT
A	B	CØ	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant.

Table 4-1: Function Table for IC SN74153

4.7 SLAVE SYNC CIRCUIT (SCHEMATIC SHEET 2)

The slave sync pulse, SSYN, is the memory's acknowledgement to the bus master in response to a master sync (MSYN). The PM-S1132 slave sync circuit is depicted in Figure 4-7.

At the end of each memory cycle (MSYN cleared) and during a refresh cycle, signal STMCL at U180-1 is set high which holds the slave sync flip-flop U182 at its reset state. (SSYN is cleared.)

At the beginning of each bus memory cycle, STMCL is held low and remains low until the slave sync signal from the memory is received by the bus master which in turn clears master sync (MSYN) and sets STMCL high again.

At the trailing edge of timing pulse CASL (generated at the output of U179-4) the slave sync flip-flop is set at U182-3. The bus master, sensing that valid data is on the bus, issues the negation of master sync which clears

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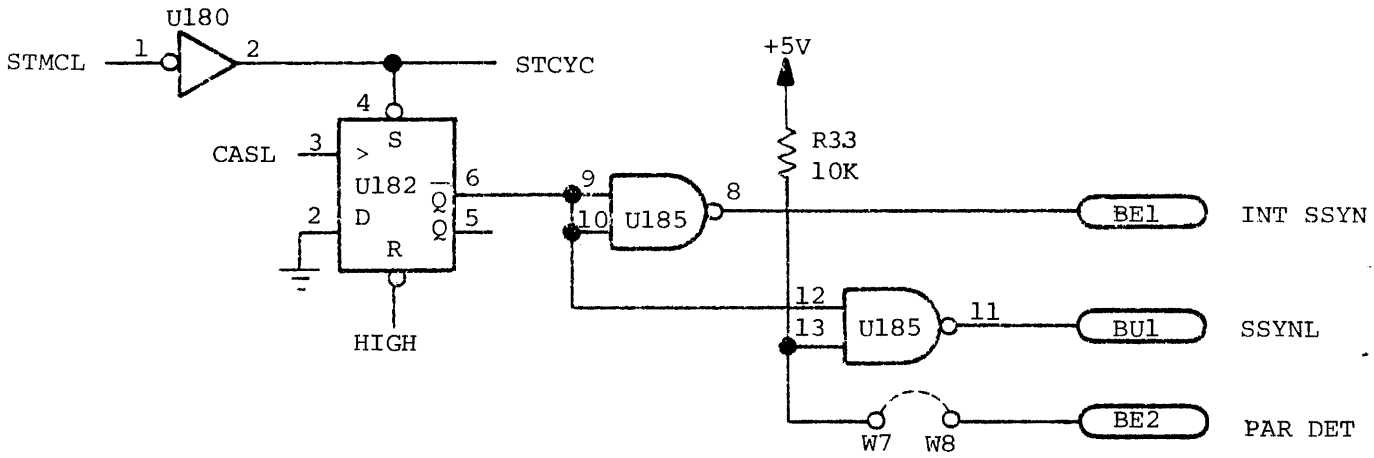

Figure 4-7: Slave Sync Circuit

the slave sync flip-flop. If the slave sync flip-flop is not cleared the Q output (U182-5) is set low inhibiting the initiation of a new memory cycle.

PAR DET (BE2) and INT SSYN (BE1) are used only if the memory is a parity memory used with a parity controller. For non-parity operation, jumpers W7 and W8 are open and INT SSYN is not used. For parity operation, W7 and W8 are jumpered. The parity controller grounds the PAR DET line which causes the slave sync pulse to be re-routed from the memory to the parity controller on the INT SSYN line. After the parity controller checks for good parity, it sends SSYN to the bus master via BUS SSYN at BU1.

Note: The PM-S1132 slave sync timing is the same for a read (DATI) or a write (DATO) cycle.

4.8 MEMORY MODES OF OPERATION (SCHEMATIC SHEET 3)

Two Unibus control lines, CØ and C1, and address bit AØØ are used to select one of five modes of operation as shown in Table 4-2.

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MODE	CØ	C1	AØØ
Read (DATI)	High	High	X
Write (DATO)	High	Low	X
Write Byte Ø	Low	Low	High
Write Byte 1	Low	Low	Low

Where X indicates that the value is irrelevant.

Table 4-2: Selection of Operation Modes

The PM-S1132 mode control circuit is shown in Figure 4-8. During a refresh cycle, the memory is forced into a read mode for both bytes by signal STRCL at U181-12. This signal (STRCL) is always low for a refresh cycle and high for a memory cycle. A low during a refresh cycle causes inputs U171-3 and -5 to set high which disables both inputs (the output of U171 is high only if both inputs are low).

STCYC at U181-9 is always low for a refresh cycle and high for a memory cycle. This blocks data from being gated into the Unibus data lines during a refresh cycle. C1 at U181-13 is low for a read cycle (inverted from the Unibus via the Unibus receivers U186). This causes U181-10 to be set high which enables data-out (DOENL) from the memory onto the Unibus data lines.

During a byte mode, CØ and C1 are both high (inverted from the Unibus), C1 enables both inputs U171-3 and -5. U171-2 and -6 are enabled depending upon the state of address bit AØØ and CØ. Both inputs U171-9 and -11 are set low for a byte mode; to enable outputs at U171-10 or -13, the other input must be high. If address bit AØØ at U169-10 is set high (inverted from the Unibus), U169-8 is enabled. This initiates a write byte 1 cycle. If address bit AØØ is set low, U171-12 is enabled. This initiates a write byte Ø cycle.

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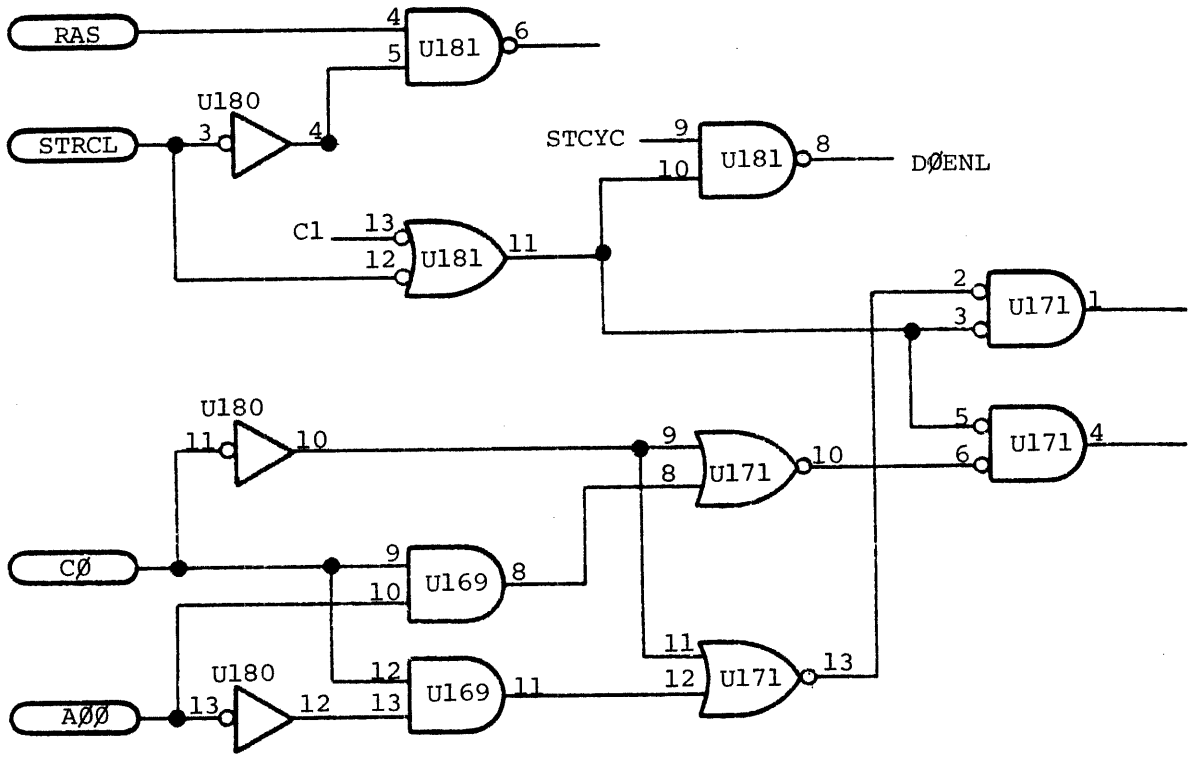

Figure 4-8: Mode Control Circuit

4.9 ADDRESS, RAS, CAS, AND WE DRIVERS (SCHEMATIC SHEETS 3 AND 4)

A typical address RAS, CAS, or WE driver is shown in Figure 4-9.

SN74SØ4

Figure 4-9: Address and Control Driver

Six address drivers are used for each bank or row of RAM's. A total of 48 address drivers are used. A 39 ohm resistor is used as series termination for each driver.

One driver is used for RAS, CAS, and WE for each row. The RAS drivers are selected by the row select logic. In total, seven drivers are used for each of the three signals.

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV	SHEET 4-12

4.10 ROW SELECT (SCHEMATIC SHEET 3)

The row select logic decodes the selected memory in 8K blocks as shown in the row select circuit in Figure 4-10.

During a memory cycle signal STMCL at U176, pins 4 and 5, are low and RAS at U176 pin 6 is high. This condition enables U176, as a one-of-eight decoder and one-of-eight output, will be selected by address bits A13, A14, and A15. Address jumper selection of U176 is defined in Section 2-3. The U176 decoder selects one of eight 8K blocks of memory and provides the RAS timing to the memory array.

During a refresh cycle, STMCL at U176 pins 4 and 5 are high disabling U176 outputs. STRC at U181 pin 5 is high enabling RAS to be applied to all rows simultaneously.

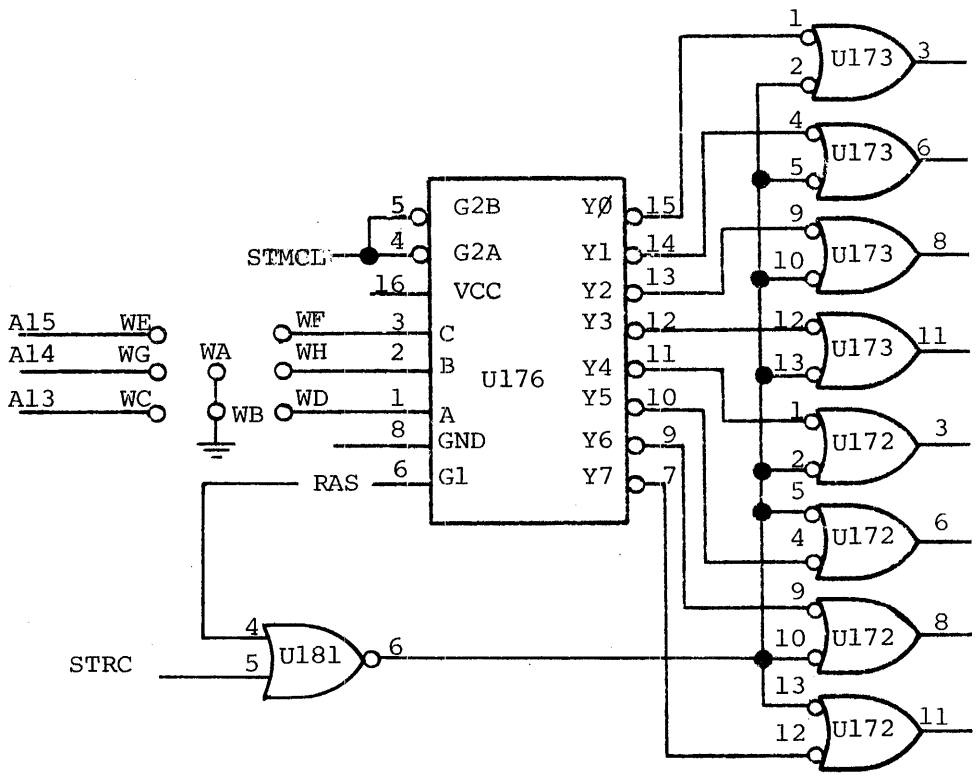

Figure 4-10: Row Select Circuit

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET 4-13

4.11 RAM LAYOUT (SCHEMATIC SHEETS 5 THROUGH 12)

The PM-S1132 contains eight rows of 4K x 1 MOS RAM IC's. Each row contains 18 RAM's on parity memories and 16 RAM's on non-parity memories. A total of 144 IC's are used for the parity version; and 128 IC's are used for the non-parity version. The 4K RAM pin configuration is depicted in Figure 4-11.

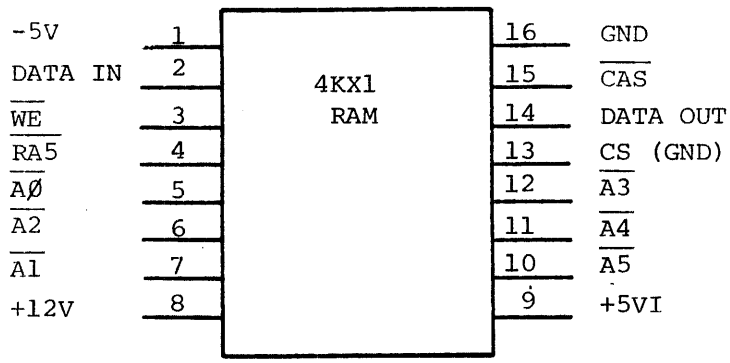

Figure 4-11: 4K RAM Pin Configuration

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4.12 -5V, +12V, AND +5V DC POWER SUPPLIES (SCHEMATIC SHEET 14)

The -5VDC power supply for the 4K RAM's is generated by U147 which is used as a +12V oscillator plus a half wave rectifier with a filter capacitor and voltage regulator IC Q2. The supply is shown in Figure 4-12.

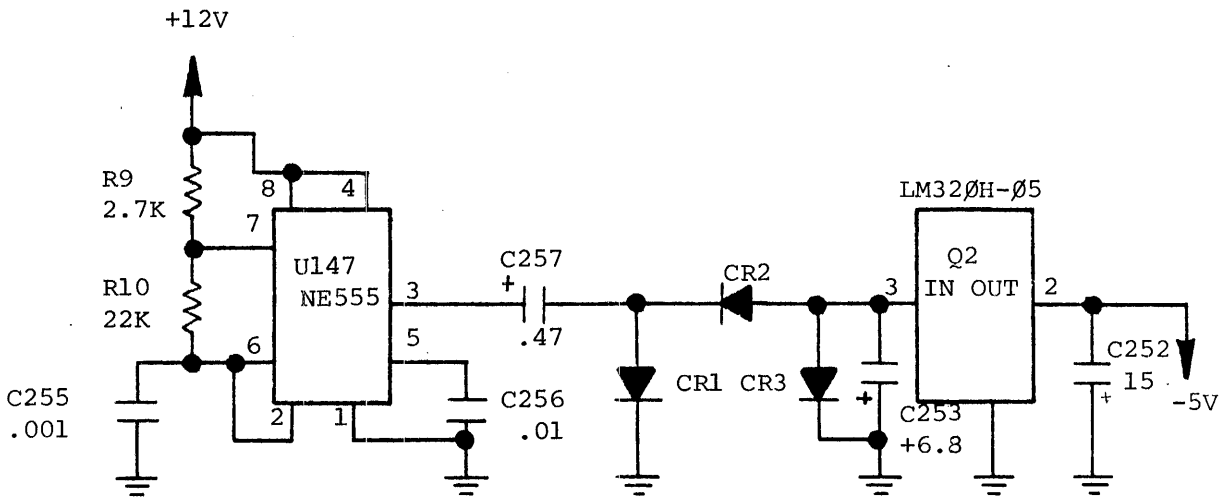

Figure 4-12: -5V DC SUPPLY

The frequency of the free running oscillator U147 is approximately 8KHz per second. Diodes CR1 and CR2 are used as half wave rectifiers and C253 is used as a filter capacitor. The voltage regulator Q2 regulates the output voltage at -5V.

The +12V DC supply is obtained from the +15V DC supply. Either the +15V BAT can be used or the +15V provided for SPC's. The voltage source is selected using jumpers W12, W13, and W14 as shown in Figure 4-13. Refer to Section 2 for jumper information.

The +5V is obtained either from the SPC backplane +5V pins or the battery backup pins. The source of voltage is selected using jumpers W9, W10, and W11. Figure 4-14 illustrates the strapping for the +5V supply. Detailed jumper and battery backup option information is contained in Section 2.

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET 4-15

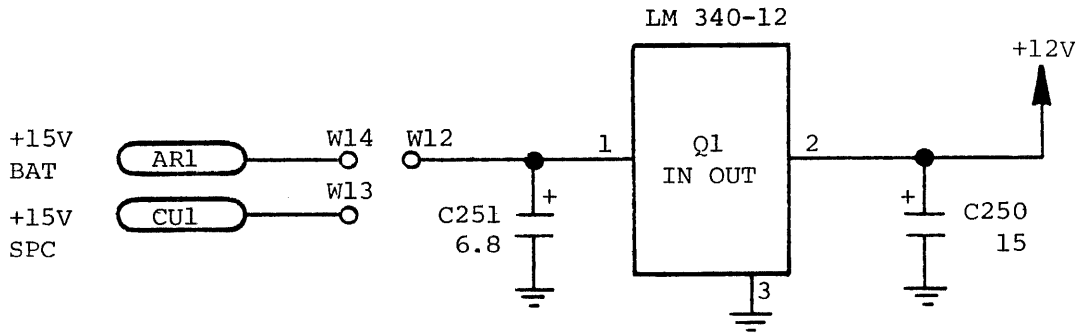

Figure 4-13: +12V DC Supply

Detailed jumper and battery backup option information is contained in Section 2.

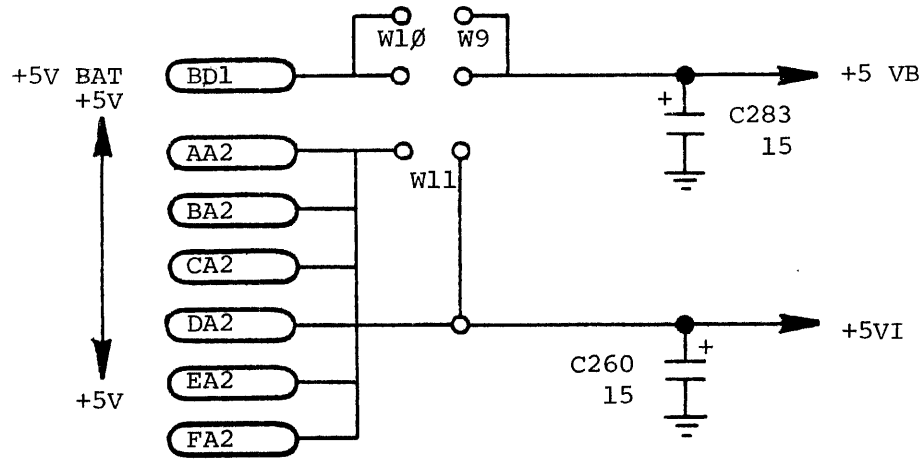

Figure 4-14: +5V Strapping

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV	SHEET 4-16

Section 5

Maintenance and Troubleshooting

This section contains maintenance and troubleshooting information for the PM-S1132 semiconductor memory system. The logic description contained in Section 4 and the drawings in the appendix can be used as references to this section.

5.1 PRINTED CIRCUIT BOARD CLEANING

The printed circuit interface contacts should be cleaned when dust or dirt has built up on the surfaces. Instant contact cleaner, alcohol, or freon can be used for cleaning contacts.

When a printed circuit contact is to be cleaned, the memory card should be held with its contacts down so that the fluid will thoroughly saturate the contact area. While the contacts are still wet, scrub them with a soft natural bristle brush.

CAUTION

Under no circumstances should an eraser or other abrasive be used on the gold plated interface contacts.

To remove dust from the memory board, a soft brush should be used. Clear, oil-free pressurized air (5psi maximum) can be used to clean the board.

5.2 GENERAL REPAIRS

Discrepancies in memory system operation are, in general, one of the following types:

- Operation failures which are caused by faulty reference control input logic or timing circuits.
- Partial data word failures which are caused by faulty IC chip or timing circuits.

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If no definite failure pattern is apparent, adjusting DC supply input voltages ±5% from the nominal values could help to cause a hard failure which can then be located.

Note: It is strongly recommended that all memories requiring repair be returned to the factory for rework. All returned units should be accompanied by a detailed description of the failure.

5.3 INTERNAL TIMING SET-UP

Refresh Timing

The refresh timing is set to approximately 30µs. The refresh signal is measured at U158 pin 11. Refresh timing is adjusted by lab set resistor R2Ø. Refresh timing is shown in Figure 5-1.

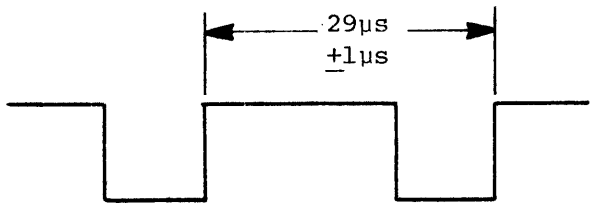

Figure 5-1: Refresh Timing

Row Address Select (RAS) Timing

RAS timing is set to approximately 260 nanoseconds. The RAS signal is measured at U162 pin 2. RAS timing is adjusted by lab set resistor R23. See Figure 5-2.

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Column Address Select (CAS) Timing

CAS timing is set by two separate lab set resistors. The CAS signal is measured at U162 pin 4. The leading edge of CAS is delayed from the leading edge of RAS by approximately 110 (50)* nanoseconds. The delay is adjusted by lab set resistor R25. This delay (CAS1) sets the time that the column address is strobed into the RAM.

The pulse width of CAS is set to approximately 150 (100)* nanoseconds (CAS2). The trailing edge of CAS is set to turn off five to ten nanoseconds earlier than the trailing edge of RAS (CAS3). Lab set resistor R27 adjusts the pulse width of CAS. See Figure 5-2.

Cycle Time

$\overline{\text{MCYC}}$ sets the cycle time of the memory. The trailing edge of MCYC (U179 pin 12) is set from the trailing edge of RAS. The timing is approximately 100 nanoseconds and is adjusted by lab set resistor R29. Timing is shown in Figure 5-2.

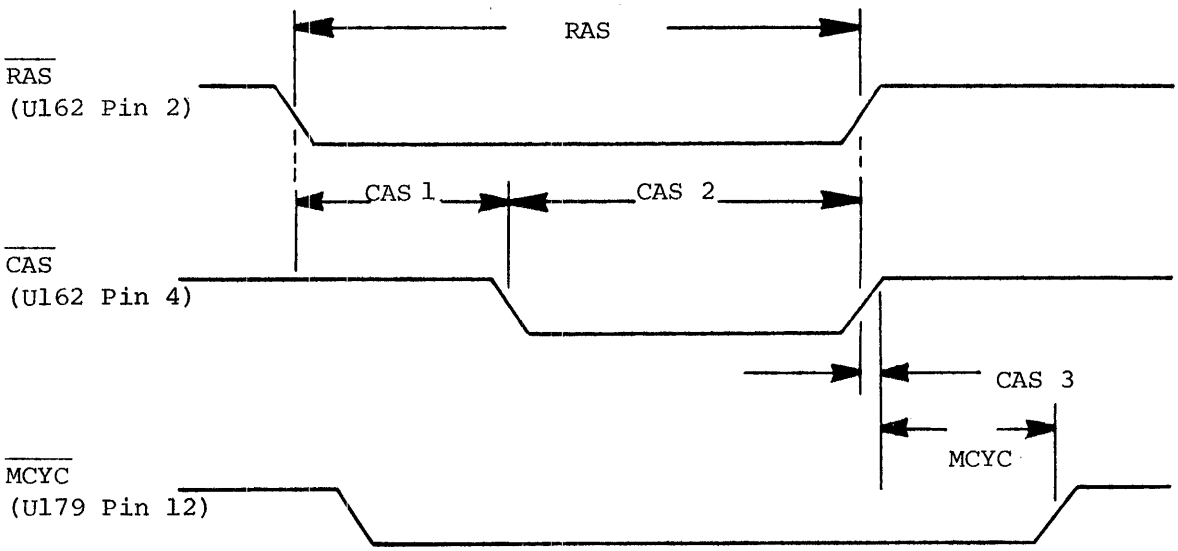

Figure 5-2: Memory Timing

* The numbers in ( ) are for the 108-115 versions.

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Memory Cycle Time

The cycle time of the memory is set for 475 (425) ns or less. The cycle time is measured from U186 pin 11 (MSYN) to U179 pin 12 (MCYC). Figure 5-3 illustrates the memory cycle.

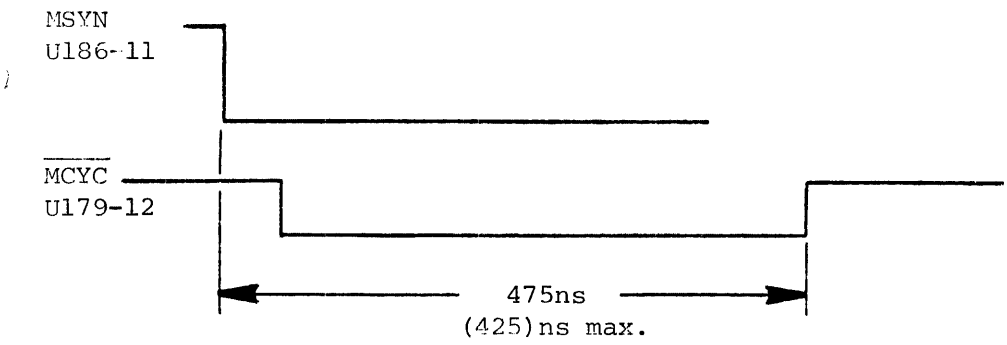

Figure 5-3: Memory Cycle

Memory Access Time

The maximum access time of the PM-S1132 is as specified in paragraph 1.2.3. Access time is defined as the time from when MSYN is asserted at the memory to the time SSYN is asserted. The access time is measured from MSYN (U186 pin 11) to SSYN (U185 pin 11). Figure 5-4 depicts the access time.

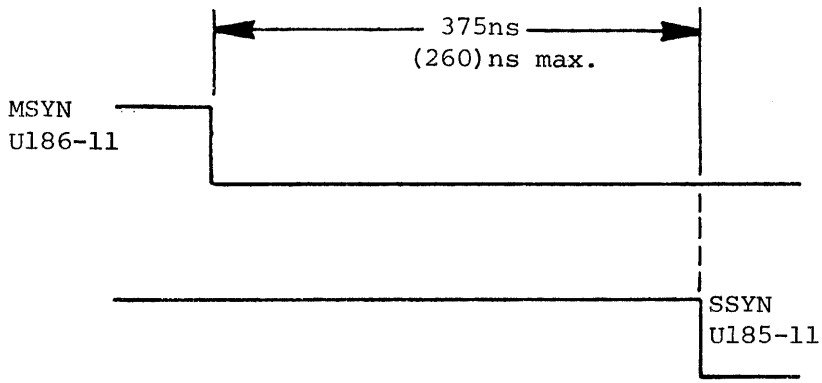

Figure 5-4: Access Time

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5.4 TROUBLESHOOTING PROCEDURE

In order to detect a malfunction in the memory card, it is useful to first isolate the general area of the memory board that causes the malfunction. Then in a step-by-step manner isolate the exact location of the failure.

All of the interface signals and the DC supply voltages must be present. Interface signals to and from the memory are outlined in Figure 5-5.

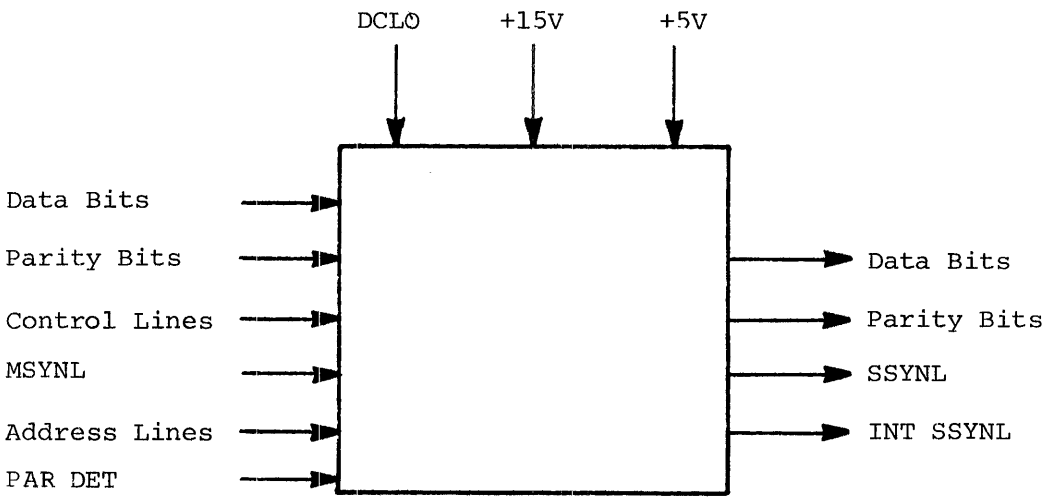

Figure 5-5: Interface Signals

The master sync (MSYN) from the bus master initiates the memory cycle. Before the memory can respond to MSYN, the following conditions must be met:

- The memory must be set to the address block in which the selected address falls.
- The memory must complete its present cycle before it is ready to accept a new MSYN command.
- The slave sync signal (SSYN) from the previous cycle must be cleared.
- The DCLO signal from the bus master must be inactive (high).

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DZKMA memory diagnostics will provide the following error type-out:

LOCATION GOOD BAD PC ERROR PAS FLG

The Location provides the memory address, Good indicates good data, and Bad is the suspected bad data received from the memory. For example:

Error typeout: 057356 003210 003010

- 057356 is the memory address in error. Find this error address in Table 5-3. The table will identify the bank in error.
- 003210 identifies good data. This is the data pattern that the CPU is expecting to receive from memory.
- 003010 identifies bad data. The difference between the good and bad data will identify the bit(s) in error. For this example bit 7 is in error. Table 5-6 identifies the bit locations within each bank.

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Bit failures are decoded to the IC level. Each IC contains 8K bytes of memory which is organized as shown in Figure 5-6.

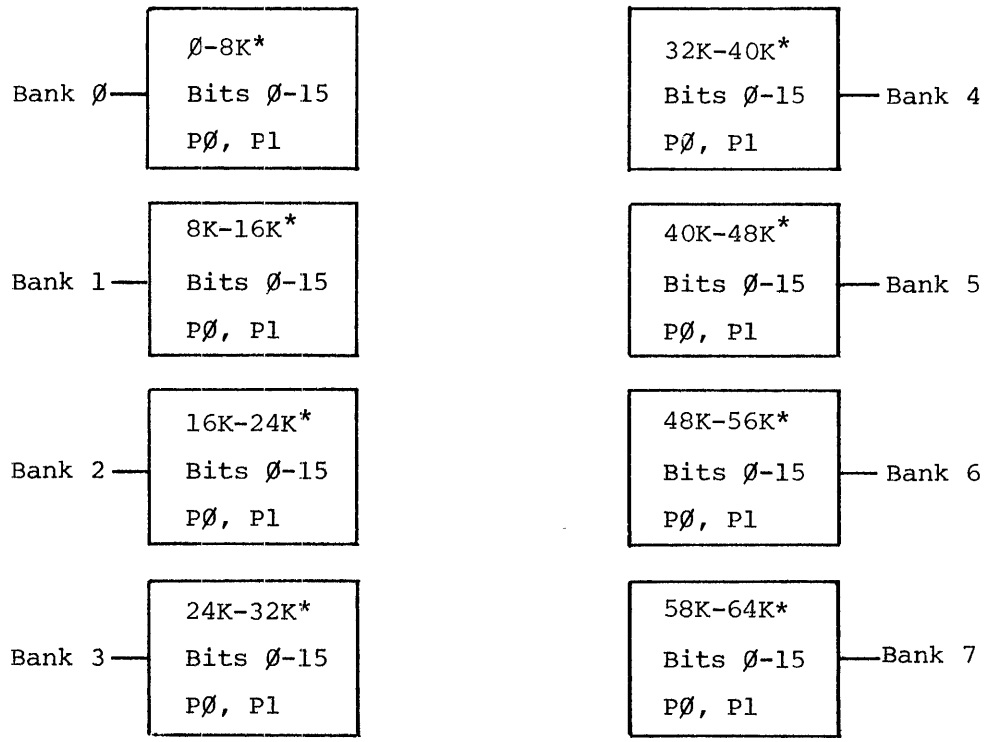

Figure 5-6: IC Arrangement for a 64K byte Parity Memory System

The PM-S1132 memory system can be depopulated to accommodate 8K, 16K, 24K, 40K, or 56K byte memory sizes. For example, an 8K memory can have 8K RAM's only in Bank Ø. A 32K byte memory can have 8K byte RAM's in banks Ø, 1, 2, and 3. Each bank of memory is identified by an 8K byte block address contained within a 64K byte block. See Figure 5-6.

The following information is included to help isolate a memory failure to a specific 4K RAM.

- Determine the memory address and data bit that is in error by running memory diagnostics.
- Determine in which bank of 8K RAMs this error would be located on the memory system. Tables 5-3 through 5-5 locate the bank in error, as identified by the memory diagnostics. These tables are defined for the PM-S1132 versions and the octal and decimal addresses are provided, as well as the bank of memory associated with each address.

* = bytes

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ERROR ADDRESS		BANK		
	DECIMAL	VERSION*		
OCTAL	(K BYTES)	24K BYTE	32K BYTE	64K BYTE
000000 - 017776	0 - 8K	0	0	0
020000 - 037776	8K - 16K	1	1	1
040000 - 057776	16K - 24K	0	2	2
060000 - 077776	24K - 32K	1	3	3
100000 - 117776	32K - 40K	0	0	4
120000 - 137776	40K - 48K	1	1	5
140000 - 157776	48K - 56K	0	2	6
160000 - 177776	56K - 64K	1	3	7
200000 - 217776	64K - 72K	0	0	0
220000 - 237776	72K - 80K	1	1	1
240000 - 257776	80K - 88K	0	2	2
260000 - 277776	88K - 96K	1	3	3
300000 - 317776	96K - 104K	0	0	4
320000 - 337776	104K - 112K	1	1	5
340000 - 357776	112K - 120K	0	2	6
360000 - 377776	120K - 128K	1	3	7
400000 - 417776	128K - 136K	0	0	0
420000 - 437776	136K - 144K	1	1	1
440000 - 457776	144K - 152K	0	2	2
460000 - 477776	152K - 160K	1	3	3
500000 - 517776	160K - 168K	0	0	4
520000 - 537776	168K - 176K	1	1	5
540000 - 557776	176K - 184K	0	2	6
560000 - 577776	184K - 192K	1	3	7
600000 - 617776	192K - 200K	0	0	0
620000 - 637776	200K - 208K	1	1	1
640000 - 657776	208K - 216K	0	2	2
660000 - 677776	216K - 124K	1	3	3
700000 - 717776	124K - 132K	0	0	4
720000 - 737776	132K - 140K	1	1	5
740000 - 757776	140K - 148K	0	2	6

Table 5-1: Error Bit Locations within Banks for 24K, 32K, and 64K Byte Versions

* 40K, 48K, and 56K byte versions can only be addressed as a full memory from address 0 in a given 64K byte block. Use the 64K byte version for bank error information.

* 24K byte versions can only be operated as a 24K byte memory starting from address 0 in a given 64K byte block. Use the 64K byte version for bank error information.

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SIZE A | CODE IDENT NO. 52648 | DWG NO. MA 700755
SCALE | REV A | SHEET 5-9

TOP OF MEMORY BOARD

BANK SELECTED	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT PA
7	U1	U2	U3	U4	U5	U6	U7	U8	U9
6	U19	U2Ø	U21	U22	U23	U24	U25	U26	U27
5	U37	U38	U39	U4Ø	U41	U42	U43	U44	U45
4	U55	U56	U57	U58	U59	U6Ø	U61	U62	U63
3	U73	U74	U75	U76	U77	U78	U79	U8Ø	U81
2	U91	U92	U93	U94	U95	U96	U97	U98	U99
1	U1Ø9	U11Ø	U111	U112	U113	U114	U115	U116	U117
0	U127	U128	U129	U13Ø	U131	U132	U133	U134	U135

BOTTOM (CONNECTOR)

Table 5-2a: 4K RAM Failure Diagnostic

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TOP OF MEMORY BOARD

BANK SELECTED	BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15	BIT PB
7	U1Ø	U11	U12	U13	U14	U15	U16	U17	U18
6	U28	U29	U3Ø	U31	U32	U33	U34	U35	U36
5	U46	U47	U48	U49	U5Ø	U51	U52	U53	U54
4	U64	U65	U66	U67	U68	U69	U7Ø	U71	U72
3	U82	U83	U84	U85	U86	U87	U88	U89	U9Ø
2	U1ØØ	U1Ø1	U1Ø2	U1Ø3	U1Ø4	U1Ø5	U1Ø6	U1Ø7	U1Ø8
1	U118	U119	U12Ø	U121	U122	U123	U124	U125	U126
0	U136	U137	U138	U139	U14Ø	U141	U142	U43	U44

BOTTOM (CONNECTOR)

Table 5-2b: 4K RAM Failure Diagnostic

Appendix A

Parts List

SK PL-700755-100 REV. X7

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET A-1

PARTS LIST	Plessey Memories Incorporated Santa Ana, California	PREPARED BY: KRAVANIS DATE 23 JAN 76	PARTS LIST NO. SKPL700755-100	REV LTR X7
ASSY TITLE: BOARD ASSEMBLY PM-51132 32K x 18		CHECKED BY: [illegible] DATE 1-27-76 RESP DSGN: [illegible] DATE 1-27-76 RESP QA: [illegible] DATE 1-27-76 OTHER: [illegible] DATE	CODE IDENT NO. 52648 D NO 123-1500 B NO. CONTRACT NO	SH 1 OF 9

LTR	DESCRIPTION	DATE	APPROVED
X1	REL TO DEV PER ERO 500511	1-27-76	[illegible]
X2	REVISED & REDRAWN X1 REV. & OBSOLETED	7-13-76	[illegible]
X3	ITEM 15 WAS 700115-001	9-16-76	
YA	PAT NAME CHANGED PER ARTWK REQUEST 'C'	10-11-76	[illegible]
X5	DELETED TBT 65, ADDED ITEMS 17, & 82.	3-16-77 5-10-77	[illegible]
X6	INCORP E01540 LL	11-16-77	[illegible]
X7	INCORP E01590 LL	11-16-77	[illegible]

LTR	DESCRIPTION	DATE	APPROVED

ENGINEERING RELEASE
COGNIZANT ENGINEER D. FOX
NOT FOR FABRICATION UNLESS SIGNED BELOW
[illegible] DATE [illegible]

U158	4	R24, 26, 30	30	C11-20, 41-50, 71-80, 101-110, 131-140, 161-170 C191-200, 221-230 256, 269	47
U163-165	5	R21, 28	31		
U185	6	R22,	32		
U170	7	R31, 32, 34	33		
U180	8	R36	34	C251, 253	48
U172, 173, 181	9	R1-8, R11-18	35	C254, 259, 261-268 271-274, 276, 279 281, 282	49
U168, 182	10	R10	36		50
U178, 179	11		37		51
U176	12	CR1-3	38	C249, 258	52
U183, 184	13	RU9-14	39	C241-248, 250 252, 260, 285	
U150-157, 159-162	14	RU1-8	40		
U174, 175	15	RU15	41		
U171	16	C257	42		53
U169	17	C255, 270	43		54
U166, 177, 186, 187	18	C275, 278	44		55
U145, 146, 148, 149	19	C280	45		56
R1-144	20	A1-10, 21-40 51-70, 81-100 111-130, 141-160 171-190, 201-220 231 240	46		57
U183	21				58
U147, 167	22			Q2	59
SW1	25			Q1	
R4	26			R20, 23, 25, 27, 29 ARE LAB SET	
R33	27				
R19	28				
	29				

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET A-2

PARTS LIST	Plessey Memories Incorporated, Santa Ana, California	CODE IDENT NO 52648	PARTS LIST NO SKPL700755-100	SH 3	REV

ITEM SELECT	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/T USAGE: C/T CODE	INV ON HAND	PAR	UNIT COST
		1	700754-001	PWB/ MEMORY BOARD				1	B				
								2					
								3					
X2		1	SN7400N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		4	A				
		3	SN74S153N	I.C./DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	T.I.	01295		5	A				
		1	SN7438N	I.C./ QUAD 2-INPUT POS NAND BUFFERS W/OC	T.I.	01295		6	A				
X2		1	SN74S10N	I.C./QUAD 2-INPUT EXCLUSIVE-OR GATES	T.I.	01295		7	A				
X2		1	SN7404N	I.C./QUAD 2-INPUT POS-OR GATES	T.I.	01295		8	A				
X2		3	SN74S00N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		9	A				
X2		2	SN74S74	I.C./DUAL D-TYPE POS EDGE-TRIGGERED FLIP-FLOPS W/PRESET/CLEAR	T.I.	01295		10	A				
		2	SN74123N	I.C./RETRIGGERABLE MONOSTABLE MULTIVIBRATORS W/CLEAR	T.I.	01295		11	A				
		1	SN74S138N	I.C/DECODERS/DEMULTIPLEXERS	T.I.	01295		12	A				
X2		2	9324	I.C./ 4 BIT MAGNITUDE COMPARATOR	FAIRCHILD	07263		13	A				
X2		12	SN74S04N	I.C./HEX INVERTERS	T.I.	01295		14	A				
		2	SN7493A	I.C./ DECODE, DIV BY TWELVE & BINARY COUNTERS	T.I.	01295		15	A				
		1	SN7402N	I.C./QUAD 2-INPUT POS NOR GATES	T.I.	01295		16	A				
		1	SN7408N	I.C./QUAD 2-INPUT POS AND GATES	T.I.	01295		17	A				
		4	DM8837	I.C./HEX UNIFIED BUS RECEIVER	NATIONAL	27014		18	A				
X2		4	DM8838	I.C./ QUAD UNIFIED BUS TRANSCEIVER	NATIONAL	27014		19	A				
X2		144	4096-3DC 4096-6	I.C./4096-BIT RANDOM ACCESS MEMORY	FAIRCHILD MOSTEK	07263 50088		20	A				
X4		1	SN74H130	I.C./8 INPUT NAND GATE	T.I.	01295		21					
		2	NE-555	I.C./ TIMER	SIGNETICS	18324		22	A				
								23					
								24					
		1	CTS 206-10	DIP SWITCH	CTS-BERNE	11236		25	A				
X2		1	RC07GF 273J	RES/ 2.7K, ±5%, 1/4W	MIL-R-11			26	A				

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV	SHEET A-3

PARTS LIST	Plessey Memories Incorporated, Santa Ana, California	CODE IDENT NO. 52648	PARTS LIST NO SKPL700755-100	SH 5	REV LTR X7

REFERENCE	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
X2		1	RC07GF103J	RES/ 10K, ±5%, 1/4W	MIL-R-11			27	A				
X2		1	RC07GF153J	RES/ 15K ±5%, 1/4W	MIL-R-11			28	A				
X2								29					
X2		3	RC07GF273J	RES/ 27K ±5%, 1/4W	MIL-R-11			30	A				
X2		2	RC07GF333J	RES/ 33K ±5%, 1/4W	MIL-R-11			31	A				
X4		1	RC07GF102J	RES/ 1K ±5%, 1/4W	MIL-R-11			32	A				
X4		3	RC07GF472J	RES/ 4.7K ±5%, 1/4W	MIL-R-11			33	A				
X7		1	RC07GF101J	RES/100Ω ±5%, 1/4W	MIL-R-11			34	A				
X2		16	RC05GF330J	RES/33Ω, ±5%, 1/8W	MIL-R-11			35	A				
X2		1	RC07GF223J	RES/22K, ±5%, 1/4W	MIL-R-11			36	A				
X2								37					
X		3	138000-001	DIODE				38	B				
X6		6	750-83-R33	RES MODULE, 33Ω	CTS	75378		39	A				
X2		8	899-3-R39	RES. MODULE, 39Ω	BECKMAN	73138		40	A				
X6		1	750-83-R47K	RES. MODULE, 47K	CTS	75378		41	A				
X2		1	150D474 X0035A2	CAP/.47μf, ±20%, 35V	SPRAGUE	05571		42	A				
X2		2	CK05BX102K	CAP/ .001μF ±10%, 200V	MIL-C-11015			43	A				
X2		2	CK05BX220K	CAP/ 22 pF ±10%, 200V	MIL-C-11015			44	A				
X2		1	CK05BX101K	CAP/ 100 pF ±10%, 200V	MIL-C-11015			45	A				
X4		160	CK05BX104K	CAP/ .1μF ±10%, 50V	MIL-C-11015			46	A				
X4		82	CK05BX103K	CAP/ .01μF ±10%, 100V	MIL-C-11015			47	A				
X2		2	150D685 X0035B2	CAP/6.8μf, ±20%, 35V	SPRAGUE	05571		48	A				
X4		18	C0698160 E103Z	CAP/ .01μF +80-20%, 16V	SPRAGUE	05571		49	A				
X4								50					
X4		2	150D475 X0020A2	CAP/ 4.7μF ±20%, 10V	SPRAGUE	05571		51	A				
X		12	150D156 X0020B2	CAP/ 15μF ±20%, 20V	SPRAGUE	05571		52	A				

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET A-4

PARTS LIST	Plessey Memories Incorporated, Santa Ana, California	CODE IDENT NO. 52648	PARTS LIST NO. SKPL700755-100	SH 7	REV LTR A

LOCATION	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
X2								53					
								54					
								55					
X2								56					
								57					
		1	LM320H-05	REGULATOR / -5V (TO-5)	SIGNETICS	18324		58	A				
		1	LM340T-12	REGULATOR / +12V (TO-220)	SIGNETICS	18324		59	A				
X2								60					
								61					
X2								62					
								63					
X2								64					
								65					
								66					
		1	IC 79	TRANSIPAD (TO-5)	MILTON ROSS	07047		67	A				
X5								68					
		1	700407-001	STIFFENER				69	B				
		6	N-440-1/4	SCREW / 4-40 X 1/4 NYLON BINDER HEAD	WECKESSER	95987		70	A				
								71					
								72					
X3		2	700330-001	HANDLE / EXTRACTOR				73	B				
		2	700331-001	SPACER				74	B				
		2	MS51957-4	SCREW / 2-56 X 5/16				75	G				
		2	NAS1291C02	NUT / HEX, #2, SELF-LOCKING				76	G				
X3		2	NW4-2814	WASHER, NYLON	WECKESSER	95987		77	A				
								78					

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET A-5

PARTS LIST	Plessey Memories Incorporated Santa Ana, California	CODE IDENT NO. 52648	PARTS LIST NO SKPL700755-100	SH 2	REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
		1	N-440-1/4	SCREW-NYLON, 4-40 X 1/4 LG FLAT HEAD, COLOR; NATURAL	WECKESSER	95987		79	A				
		1	N-440-X	NUT-NYLON, 4-40, COLOR; NATURAL	WECKESSER	95987		80	A				
		1	7903-10-51	INSULATOR	BERGQUIST COMP.			81	A				
X5		AR	5952	WIRE (28 AWG KYNAR INSUL.) COLOR: OPTIONAL	ALPHA	23172		82	A				
		AR	SN63WRAP3	SOLDER	QQ-S-571			83	G				

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET A-6

Appendix B

Assembly Drawing

SK 700755 REV. X6

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET B-1

FORM 000021

Appendix C

Schematic Diagrams

SK SD 700755 REV. X5

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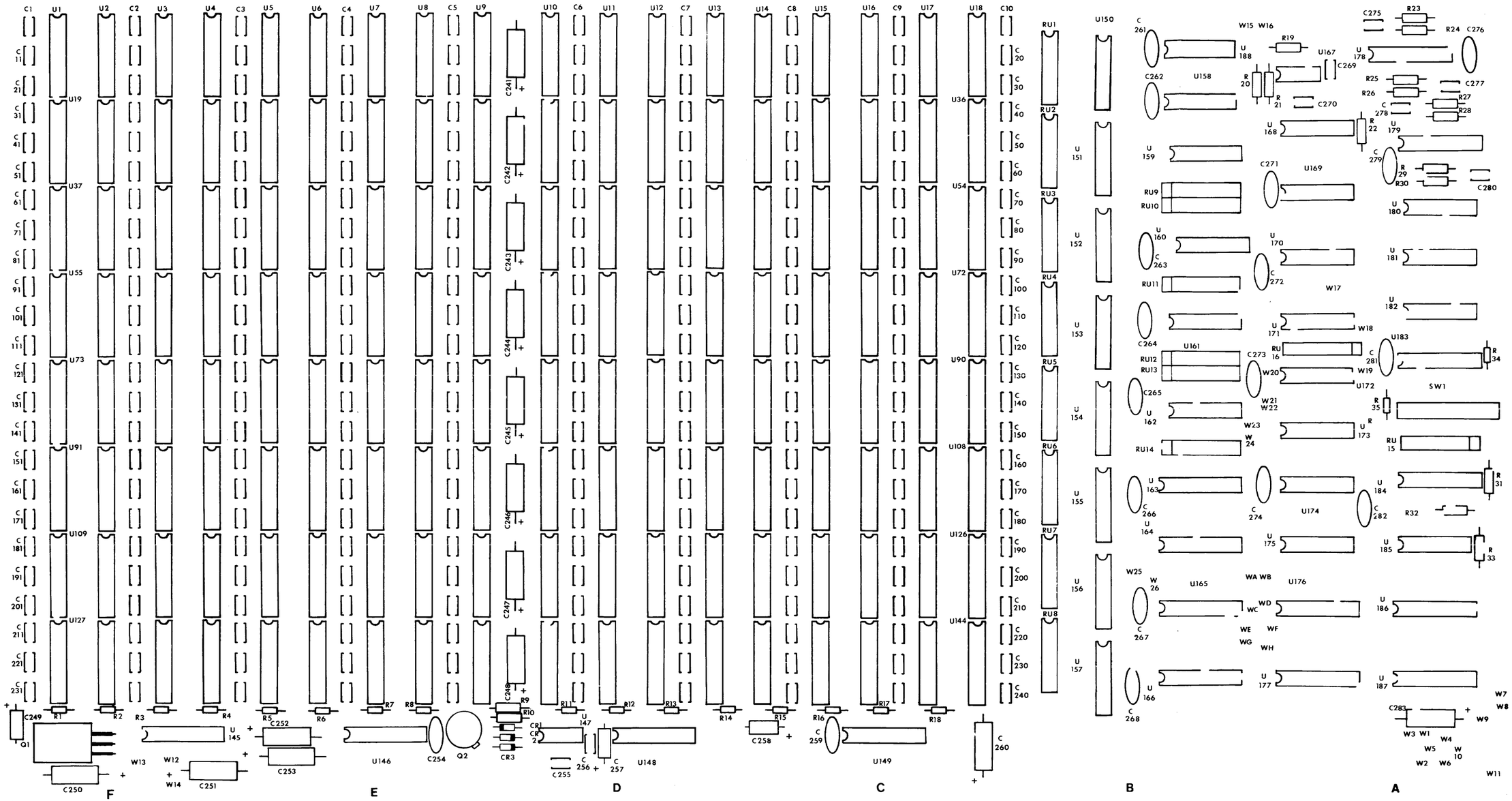
SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV A	SHEET C-1



JUMPER WIRE CHART

VERSION	JUMPERS	NOTES	VERSION	JUMPERS	NOTES
-100, -101 -108, -109	W1 to A3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	9 10	-200, -201	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	10
102 110	W1 to A3, A4 to W6, A7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, W4 to W24	9 10	-202	W9 to W11, W12 to W13, WC to WD, WF to WF, WG to W11, W18 to W24	10
-103 -111	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	9 10	-203	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	10
-104 -112	W1 to A3, W4 to W6, W7 to W8, A9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	9 10	-204	W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	10
-105 -113	A1 to W3, A4 to A6, A7 to W8, W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH,	9 10	-205	W9 to W11, W12 to W13 WA to WF, WC to WD, WG to WH	10
-106 -114	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, W8 to WH, WC to WD	9 10	-206	W9 to W11, W12 to W13, WA to WF, W8 to WH WC to WD	10
-107 -115	W1 to W3, W4 to W6, W7 to W8, W9 to A11, W12 to W13, WA to WF, WA to WH, W8 to WD	9 10	-207	W9 to W11, W12 to W13, WA to WF, WA to WH, W8 to WD	10

PM-S1132 ASSEMBLY DRAWING
NUMBER 700755 REV X6

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	MA 700755
SCALE	REV	SHEET B-2

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X1	REL TO ECN PER ERO 500857	8-11-76	
	X2	ADDED SHEET 14 & NOTES 6 & 7	1-12-77	
	X3	ADDED NOTE 11 & REVISED SHT 14	3-16-77	
	X4	INCORP EO1540	11-15-77	
	X5	INCORP EO1590	11-15-77	

LAST DESIGNATION USED	
RESISTOR	R36
RESISTOR MODULE	RU15
CAPACITOR	C283
INTEGRATED CKT	U188
DIODE	CR3

NOT USED	
C277	CAPACITOR
R35	RESISTOR

REF DESIG	GATES USED PER TOTAL	PART NUMBER
U180	5/6	SN7404
U182	1/2	SN74S74

SOLDER SIDE — A CONNECTOR — COMPONENT SIDE

SIDE 2		SIDE 1
	V	
	U	
	T	GND
	S	
	R	+5V BAT
	P	PAR PØ
PBL	N	PAR P1
D15L	M	PAL
D13L	L	D14L
D11L	K	D12L
DØ9L	J	D10L
DØ7L	H	DØ8L
DØ5L	F	DØ6L
DØ3L	E	DØ4L
DØ1L	D	DØ2L
GND	C	DØØL
	B	
+5V	A	

SOLDER SIDE — B CONNECTOR — COMPONENT SIDE

	V	MSYNL
CØL	U	SSYNL
C1L	T	GND
A16L	S	A17L
A14L	R	A15L
A12L	P	A13L
A10L	N	A11L
A08L	M	A09L
A06L	L	A07L
A04L	K	A05L
A02L	J	A03L
A00L	H	AØ1L
DC LØ	F	
PAR DET	E	INT SSYN
	D	+5V BAT
GND	C	
	B	
+5V	A	

SOLDER SIDE — C CONNECTOR — COMPONENT SIDE

SIDE 1		SIDE 2
	V	
	U	+15 SRC
	T	GND
	S	
	R	
	P	
	N	
	M	
	L	
	K	
	J	
	H	
	F	
	E	
	D	
GND	C	
	B	NPG OUT
+5V	A	NPG IN

SOLDER SIDE — D CONNECTOR — COMPONENT SIDE

	V	
	U	
BG4 OUT	T	
BG4 IN	S	
BG5 OUT	R	
BG5 IN	P	
BG6 OUT	N	
BG6 IN	M	
BG7 OUT	L	
BG7 IN	K	
	J	
	H	
	F	
	E	
	D	
GND	C	
	B	
+5V	A	

SOLDER SIDE — E CONNECTOR — COMPONENT SIDE

SIDE 2		SIDE 1
	V	
	U	
	T	GND
	S	
	R	
	P	
	N	
	M	
	L	
	K	
	J	
	H	
	F	
	E	
	D	
GND	C	
	B	
+5V	A	

SOLDER SIDE — F CONNECTOR — COMPONENT SIDE

	V	
	U	
	T	GND
	S	
	R	
	P	
	N	
	M	
	L	
	K	
	J	
	H	
	F	
	E	
	D	
GND	C	
	B	
+5V	A	

6. 30K OPTION
CUT ETCH U169-1 & U169-2, SOLDER SIDE.
ADD: W15 TO W16.

5. 31K OPTION
CUT ETCH U169-1 & U169-2, SOLDER SIDE.
ADD: W15 TO W16.
CUT ETCH U188-5 & U188-6 SOLDER SIDE.
ADD: W25 TO W26.

4. ALL CAPACITOR VALUES ARE IN μF, 50V.

[3] VALUES ARE LAB SET PER TEST SPEC TS700755

2. ALL DIODES ARE 138000-001.

1. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

[12] FOR VERSIONS -108 THRU -115:
(A) CUT ETCH: U178-12 (SOLDER SIDE)
(B) ADD JUMPER: U181-3 TO U168-3

11. FOR BATTERY BACKUP OPTION: VERSION -100 THRU -115, -200 THRU -207, JUMPER WIRES ARE AS FOLLOWS: W9 TO W10, W12 TO W14. ALL OTHER JUMPERS TO REMAIN THE SAME.

10. DESIGNATIONS SHOWN IN PARENTHESES (2/A3) INDICATES WHERE SIGNAL ORIGNATES OR TERMINATES
ZONE DESIGNATION
SHEET NUMBER

9. SIGNALS SHOWN IN RECTANGLE
AA2 ARE I/O CONNECTIONS
BOARD SIDE
PIN DESIGNATION
CONNECTOR DESIGNATION

ENGINEERING RELEASE
COGNIZANT ENGINEER
NOT FOR FABRICATION UNLESS SIGNED BELOW
DATE 8-12-76

NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION / MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
		PARTS LIST			

PART/ASSY NO. & QTY PER ASSY: X5
PART/ASSY REV LTR
PART NO. SK SD700755-100 PI-S1132 | NEXT ASSY | USED ON
APPLICATION

DO NOT SCALE DRAWING
SCREW THREADS PER HANDBOOK H-28
COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM
REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R
ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1
STANDARD HOLE TOLERANCE PER ANSI B32.1
TOLERANCES ON: XX = ± .03 XXX = ± .010 ANGLES = ± 0° 30'
INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH
UNLESS OTHERWISE SPECIFIED

CONTRACT NO.

DRAWN	H. W. BLANK	8/13/76
CHECK	D. Tuck	8-14-76
ENGR		
PROJ. ENGR		
PROD. DESIGN		8/17/76
OTHER APPROVALS		

Plessey Memories Incorporated
Santa Ana, California

DWG TITLE
SCHEMATIC DIAGRAM
MEMORY SYSTEM
PN-S1132

SIZE	CODE IDENT NO.	DWG NO.	REV
D	52648	SK SD700755	X5

SCALE: NONE | SHEET 1 OF 14 | DISTR NO. 1909-0

DWG NO SK SD700755 REV X5

FORM NO. 000012

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

ADDRESS RECEIVERS

DM8837 — U166 — A17L BS1, A16L BS2, A15L BR1, A14L BR2, A13L BP1, A12L BP2 — A15 (3/D8), A14 (3/D8), A13 (3/D8), A12 (3/D3)

DM8837 — U177 — A11L BN1, A10L BN2, A09L BM1, A08L BM2, A07L BL1, A06L BL2 — A11 (3/D3), A10 (3/C3), A09 (3/C3), A08 (3/B3), A07 (3/B3), A06 (3/D3)

DM8837 — U187 — A05L BK1, A04L BK2, A03L BJ1, A02L BJ2, A01L BH1, A00L BH2 — A05 (3/D3), A04 (3/C3), A03 (3/C3), A02 (3/B3), A01 (3/B3), A00 (3/B8)

DM8837 — U186 — C0L BU2, C1L BT2, MSYNL BV1, PAL AM1, PAR P0 AP1, DC L0 BF2, PBL AN2, PAR P1 AN1 — W2, W1, W3, W5, W4, W6 — C0 (3/B8), C1 (3/C7), MSYN (2/D4), PAI (5-12/C2), PBI (5-12/B2)

+5V, RU15, R34 4.7K, R32 4.7K, R31 4.7K

9324 — U183 — B4, A4, B3, A3, B2, A2, B1, A1, B0, A0 — A<B, A=B, A>B, VCC, GND — U169-2 (2/A5), U169-3 (2/A5)

SW1

9324 — U184 — B4, A4, B3, A3, B2, A2, B1, A1, B0, A0 — A<B, A=B, A>B, VCC, GND — RU15

STMCL (3/D7) — U180 SN7404 — STCYC (3/C7)

SN74S74 — U182 — CASL (2/A1)

R33 10K +5V

MSYN (2/D6) — U170 — U169-2 (2/A5), U169-3 (2/A5)

U185 SN7438 — BE1 INT SSYN

U185 SN7438 — BU1 SSYNL

W7 W8 — BE2 PAR DET

U170 SN74S10 — STRCL (3/C8)

U181 SN74S00 — SRASL (2/B4)

U169 SN7408

SN7400 — (2/A1) CAS (3/C5), (3/C6) STRC — U158

HIGH

SN74S74 — U168 — REF (3/A7)

SN7400 — U158

R20, R21 33K, R19 15K — U167 NE-555 — C270 .001, C269 .01

R36 100Ω, R29, R30 27K, C280 100pf

R23, R24 27K, C275 22pf

RAS (3/C7)

U178 SN74123 — R22 1K — SRASL (2/D1)

U179 SN74123 — HIGH

R25, R26 27K, C277

SN74S74 — U168 — MXSL (3/C3)

SN74123 — U179 — CAS (2/C4), (3/B5); CASL (2/D3)

U178 SN74123

R27, R28 33K, C278 22pf

SN7400 — U158

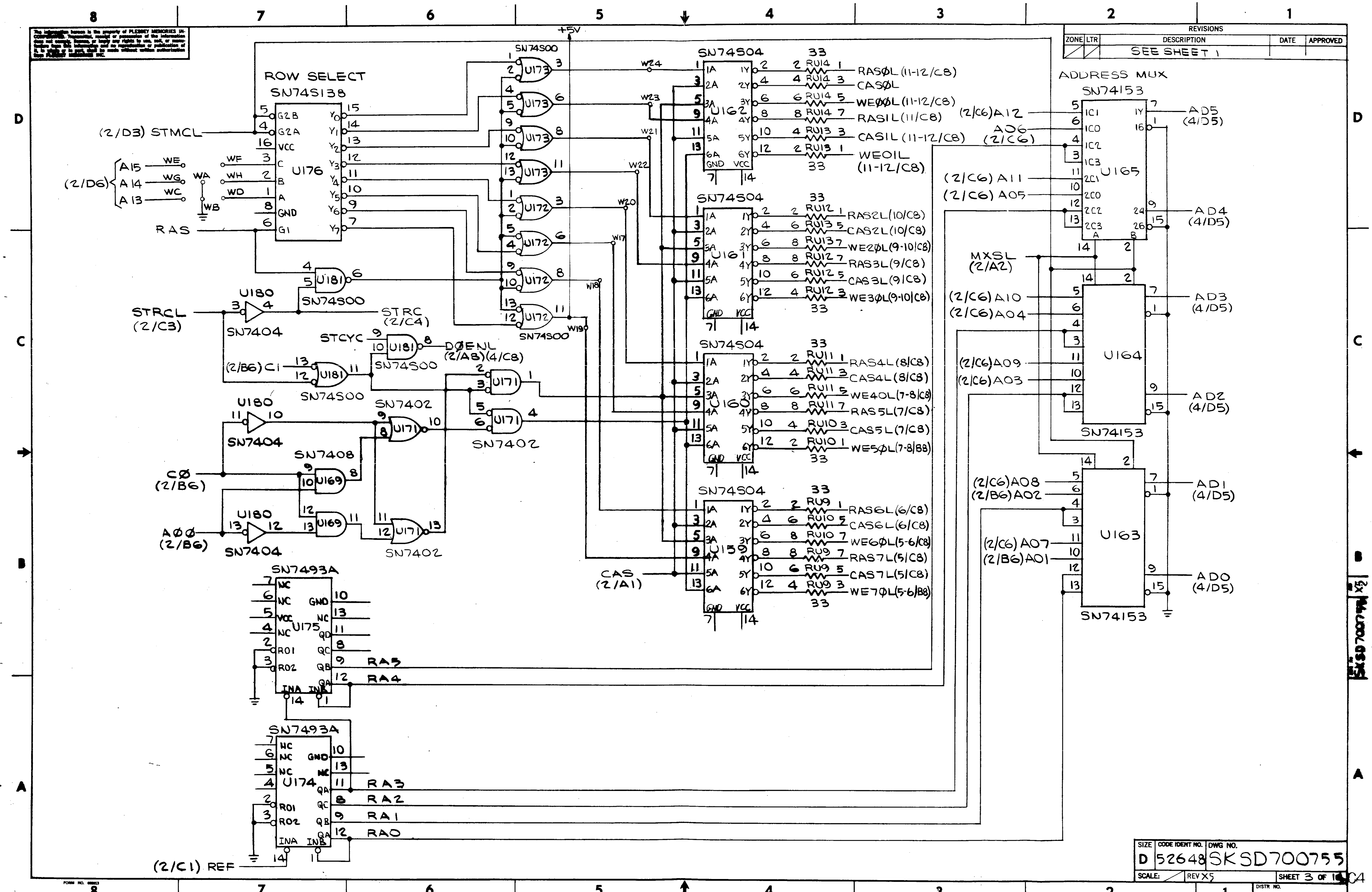
PA0 (5-12/C2), DØENL (3/C6), PB0 (5-12/B2) — SN7404 U180 — SN7438 U185

A15, A14, A13, A12 — U188 SN7H30 — W15, W16 — U168 SN7408 — U170-1 (2/D3), U183-2 (2/D4)

A11, W26, W25

SIZE	CODE IDENT NO.	DWG NO.	REV
D	52648	SKSD700755	X5
SCALE:		SHEET 2 OF 3	
		DISTR NO.	

FORM NO. 00613



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
SEE SHEET 1
ROW SELECT
SN74S138
U176
(2/D3) STMCL
(2/D6) A15 A14 A13
WE WG WC WF WH WD WA WB
RAS
STRCL
(2/C3)
U180
SN7404
STRC
(2/C4)
STCYC
DØENL
(2/AB) (4/C8)
(2/B6) C1
U181
SN74S00
U173
U172
U171
SN7402
SN7408
U169
CØ
(2/B6)
AØØ
(2/B6)
+5V
W24 W23 W21 W22 W20 W17 W18 W19
SN74S04
U162
U161
U160
U159
CAS
(2/A1)
33
RU14 RU13 RU12 RU11 RU10 RU9
RASØL (11-12/C8)
CASØL
WEØØL (11-12/C8)
RAS1L (11/C8)
CAS1L (11-12/C8)
WE01L (11-12/C8)
RAS2L (10/C8)
CAS2L (10/C8)
WE2ØL (9-10/C8)
RAS3L (9/C8)
CAS3L (9/C8)
WE3ØL (9-10/C8)
RAS4L (8/C8)
CAS4L (8/C8)
WE4OL (7-8/C8)
RAS5L (7/C8)
CAS5L (7/C8)
WE5ØL (7-8/B8)
RAS6L (6/C8)
CAS6L (6/C8)
WE6ØL (5-6/C8)
RAS7L (5/C8)
CAS7L (5/C8)
WE7ØL (5-6/B8)
ADDRESS MUX
SN74153
U165
U164
U163
(2/C6) A12
A06 (2/C6)
(2/C6) A11
(2/C6) A05
MXSL
(2/A2)
(2/C6) A10
(2/C6) A04
(2/C6) A09
(2/C6) A03
(2/C6) A08
(2/B6) A02
(2/C6) A07
(2/B6) A01
AD5 (4/D5)
AD4 (4/D5)
AD3 (4/D5)
AD2 (4/D5)
AD1 (4/D5)
AD0 (4/D5)
SN7493A
U175
U174
NC VCC GND RO1 RO2 QA QB QC QD INA INB
RA5 RA4 RA3 RA2 RA1 RA0
(2/C1) REF
SIZE D CODE IDENT NO. 52648 DWG NO. SKSD700755
SCALE: REV X5 SHEET 3 OF 1
DISTR NO.

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REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		

DATA TRANSCEIVERS

DM8838 — U145

DØØL	AC1	1	BUS3	IN3 2 → DØØI
			OUT3 3	R1 33 → DØI (5-12/C8)
DØ1L	AD2	4	BUS4	IN4 5 → D10I
		8	GND	OUT4 6 → D11I (5-12/C7)
DØ2L	AD1	15	BUS1	IN1 14 → D20I
		16	VCC	OUT1 13 → D21I (5-12/C6)
				IN2 11 → D30I
DØ3L	AE2	12	BUS2	OUT2 10 → D31I (5-12/C6)
			DB 7	DA 9

DØENL (3/C6)

DM8838 — U146

DØ4L	AE1	1		2 → D40I
				R5 33 → D41I (5-12/C5)
DØ5L	AF2	4		5 → D50I
		8		6 → D51I (5-12/C4)
DØ6L	AF1	15		14 → D60I
		16		13 → D61I (5-12/C3)
DØ7L	AH2	12		11 → D70I
				10 → D71I (5-12/C3)
				7 9

DM8838 — U148

DØ8L	AH1	1		2 → D80I
				R11 33 → D81I (5-12/B8)
DØ9L	AJ2	4		5 → D90I
		8		6 → D91I (5-12/B7)
D1ØL	AJ1	15		14 → D1Ø0I
		16		13 → D1ØI (5-12/B6)
D11L	AK2	12		11 → D110I
				10 → D111I (5-12/B6)
				7 9

DM8838 — U149

D12L	AK1	1		2 → D120I
				R15 33 → D121I (5-12/B5)
D13L	AL2	4		5 → D130I
		8		6 → D131I (5-12/B4)
D14L	AL1	15		14 → D140I
		16		13 → D141I (5-12/B3)
D15L	AM2	12		11 → D150I
				10 → D151I (5-12/B3)
				7 9

ADDRESS DRIVERS

SN74S04 — RU8 — U157 — (12/D8)

(3/B1) AD0	1	2 → AØØL
(3/B1) AD1	9	8 → AØ1L
(3/B1) AD2	3	4 → AØ2L
(3/B1) AD3	13	12 → AØ3L
(3/B1) AD4	11	10 → AØ4L
(3/D1) AD5	5	6 → AØ5L
	14 7	39

SN74S04 — RU7 — U156 — (11/D8)

	1	2 → A1ØL
	9	8 → A11L
	3	4 → A12L
	13	12 → A13L
	11	10 → A14L
	5	6 → A15L
	14 7	39

SN74S04 — RU6 — U155 — (10/D8)

	1	2 → A2ØL
	9	8 → A21L
	3	4 → A22L
	13	12 → A23L
	11	10 → A24L
	5	6 → A25L
	14 7	39

SN74S04 — RU5 — U154 — (9/D8)

	1	2 → A3ØL
	9	8 → A31L
	3	4 → A32L
	13	12 → A33L
	11	10 → A34L
	5	6 → A35L
	14 7	39

SN74S04 — RU4 — U153 — (8/D8)

(3/B1) ADØ	1	2 → A4ØL
(3/B1) AD1	9	8 → A41L
(3/C1) AD2	3	4 → A42L
(3/C1) AD3	13	12 → A43L
(3/D1) AD4	11	10 → A44L
(3/D1) AD5	5	6 → A45L
	14 7	39

SN74S04 — RU3 — U152 — (7/D8)

	1	2 → A5ØL
	9	8 → A51L
	3	4 → A52L
	13	12 → A53L
	11	10 → A54L
	5	6 → A55L
	14 7	39

SN74S04 — RU2 — U151 — (6/D8)

	1	2 → A6ØL
	9	8 → A61L
	3	4 → A62L
	13	12 → A63L
	11	10 → A64L
	5	6 → A65L
	14 7	39

SN74S04 — RU1 — U150 — (5/D8)

	1	2 → A7ØL
	9	8 → A71L
	3	4 → A72L
	13	12 → A73L
	11	10 → A74L
	5	6 → A75L
	14 7	39

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X5	SHEET 4 of 26

FORM NO. 88823

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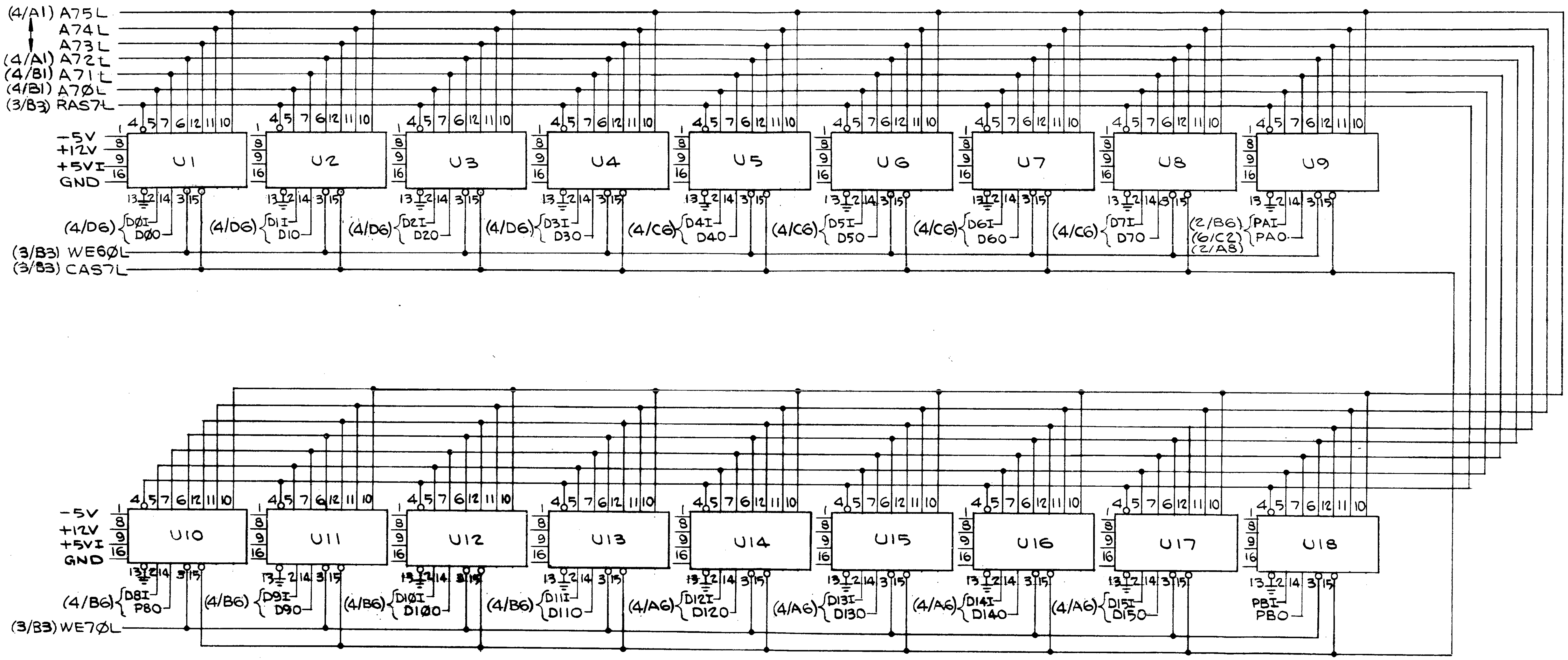
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X'	SHEET 5 OF 16

DISTR NO.

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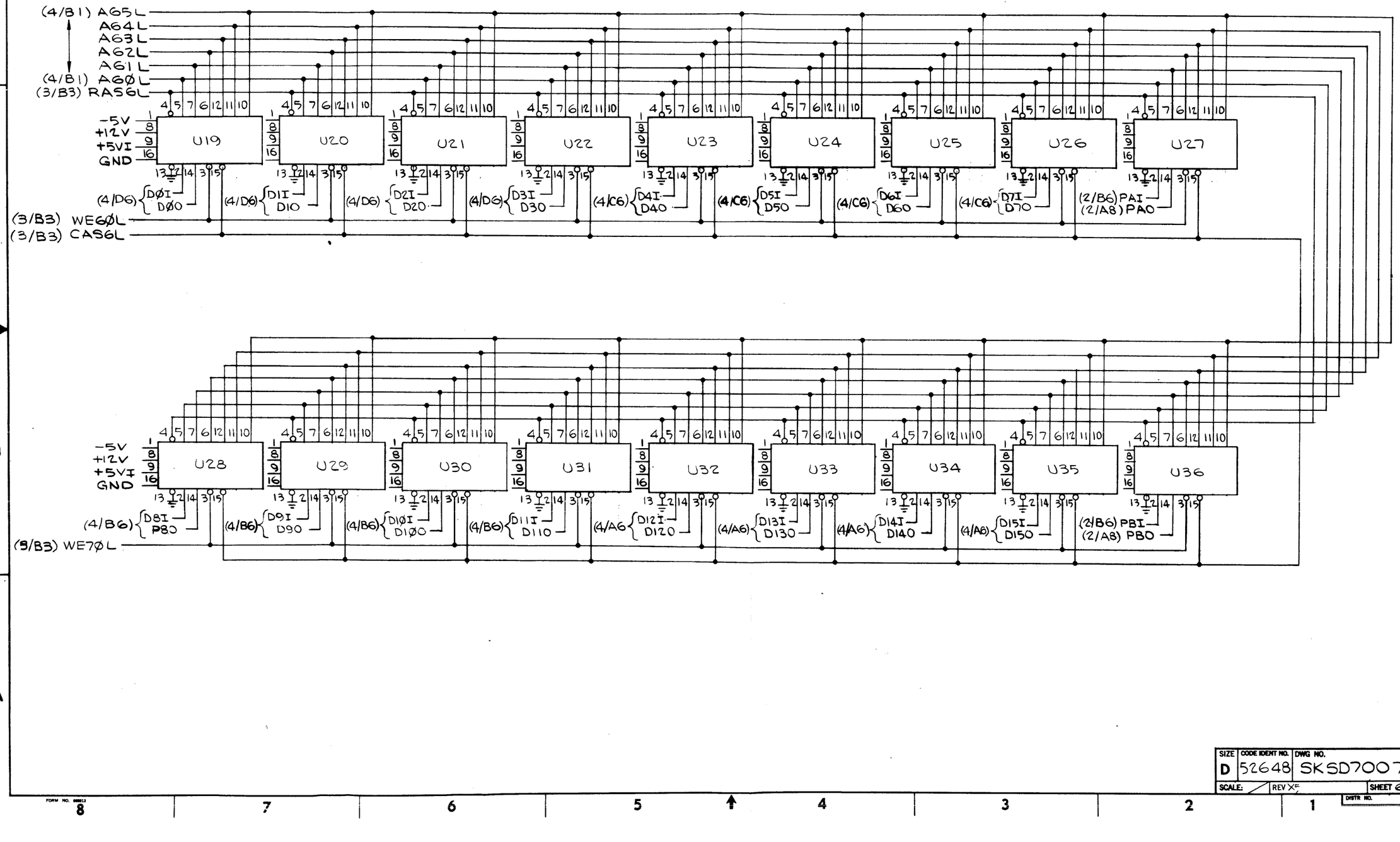
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755

SCALE: | REV X | SHEET 6 OF 16 | DISTR NO.

SKSD700755 X5

FORM NO. 600813

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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/C1) A55L
A54L
A53L
A52L
A51L
(4/C1) A50L
(3/C3) RAS5L

-5V
+12V
+5VI
GND

U37 U38 U39 U40 U41 U42 U43 U44 U45

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) PAI
(2/A8) PA0

(3/C3) WE4ØL
(3/C3) CAS5L

-5V
+12V
+5VI
GND

U46 U47 U48 U49 U50 U51 U52 U53 U54

(4/B6) D8I P80
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
(2/B6) PBI
(2/A8) PB0

(3/B3) WE5ØL

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X	SHEET 7 OF 14
		DISTR NO.

SKSD700755 X3

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REVISIONS			
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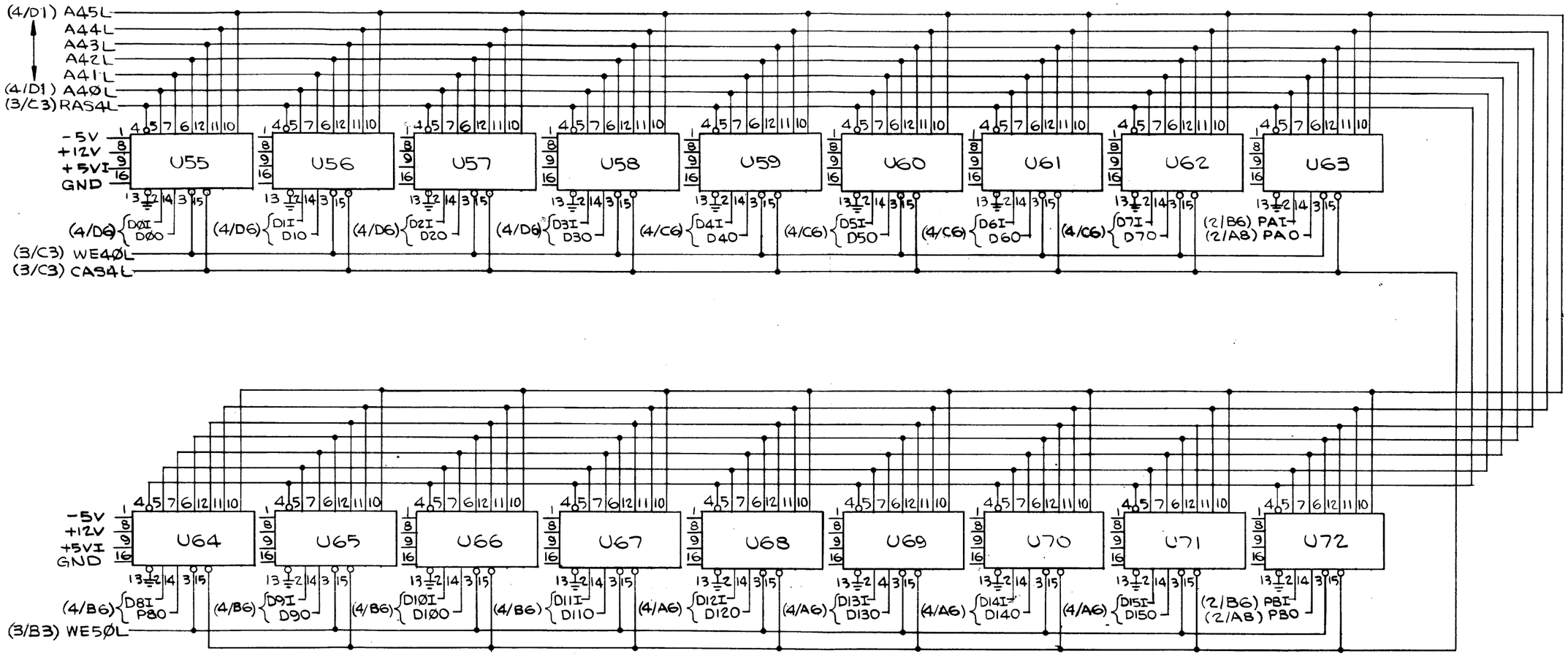
	SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X5	SHEET 8 OF 16
		DATA NO.

SKSD700755 X5

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REVISIONS			
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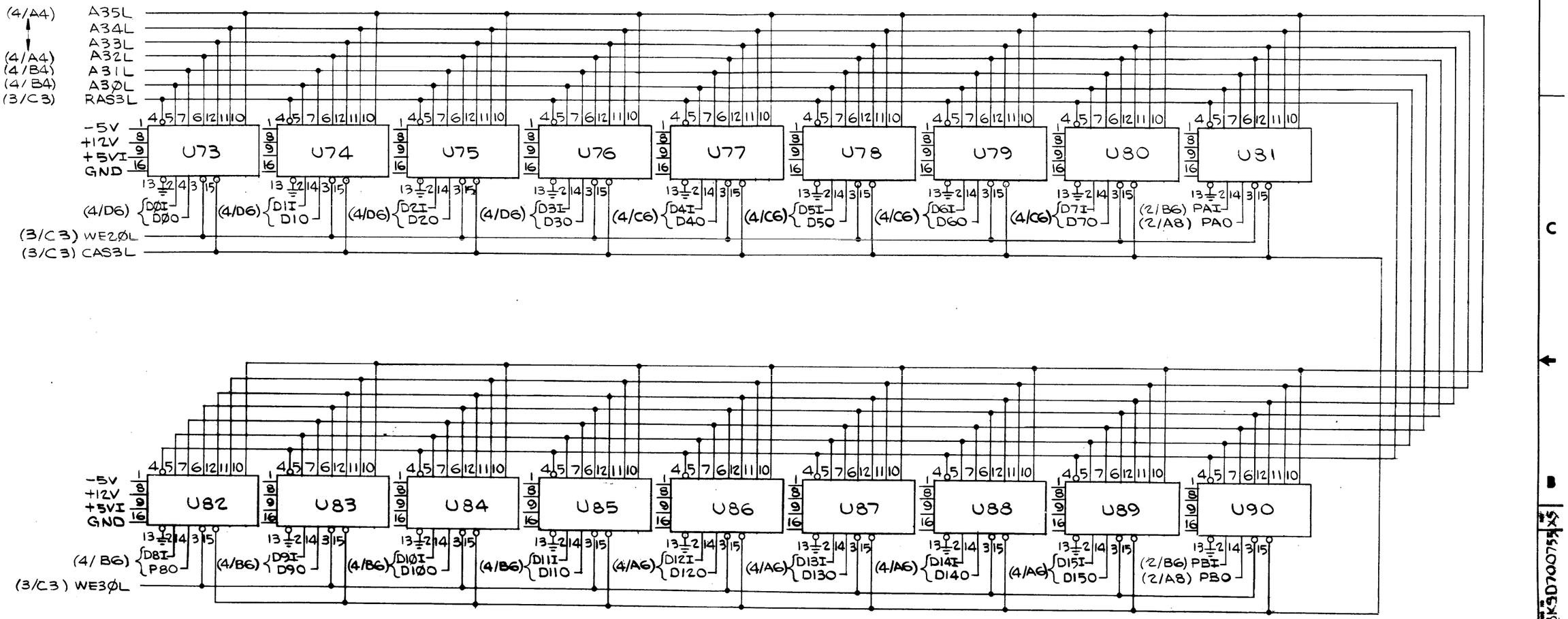
	SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755

SCALE: REV X[L] SHEET 2 OF 10

DISTR NO.

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SKSD700755 X5

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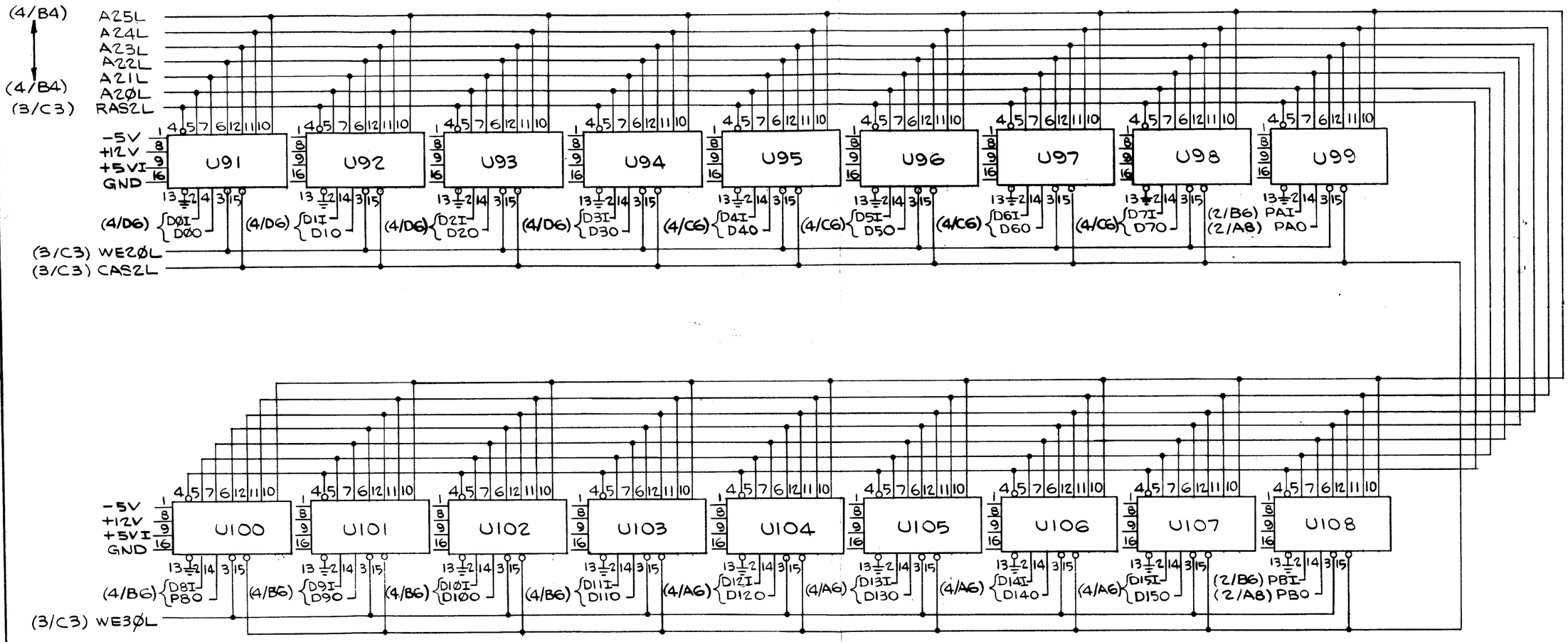
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X5	SHEET 10 OF 14
		DISTR NO.

SKSD700755 X5

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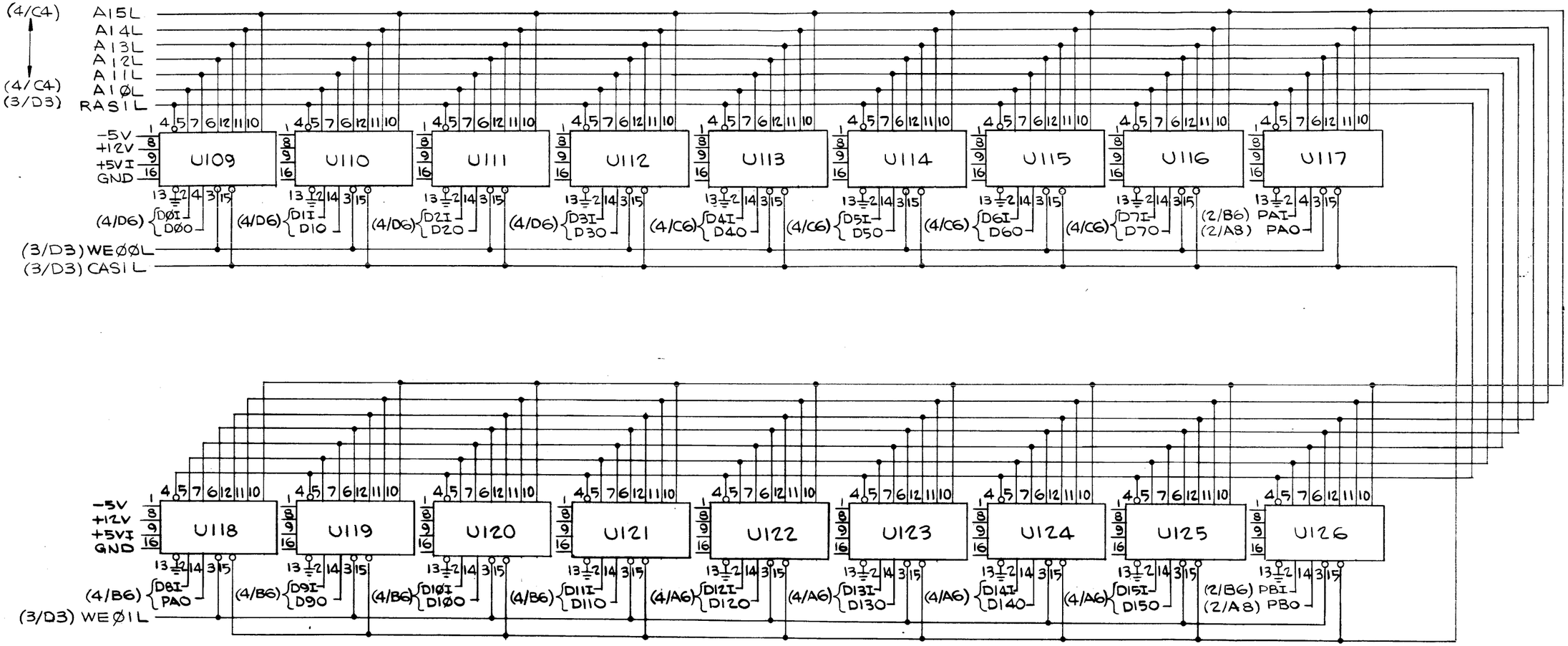
REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X[illegible]	SHEET 11 OF 14
		DISTR NO.

SKSD700755 X5

FORM NO. 000813

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REVISIONS			
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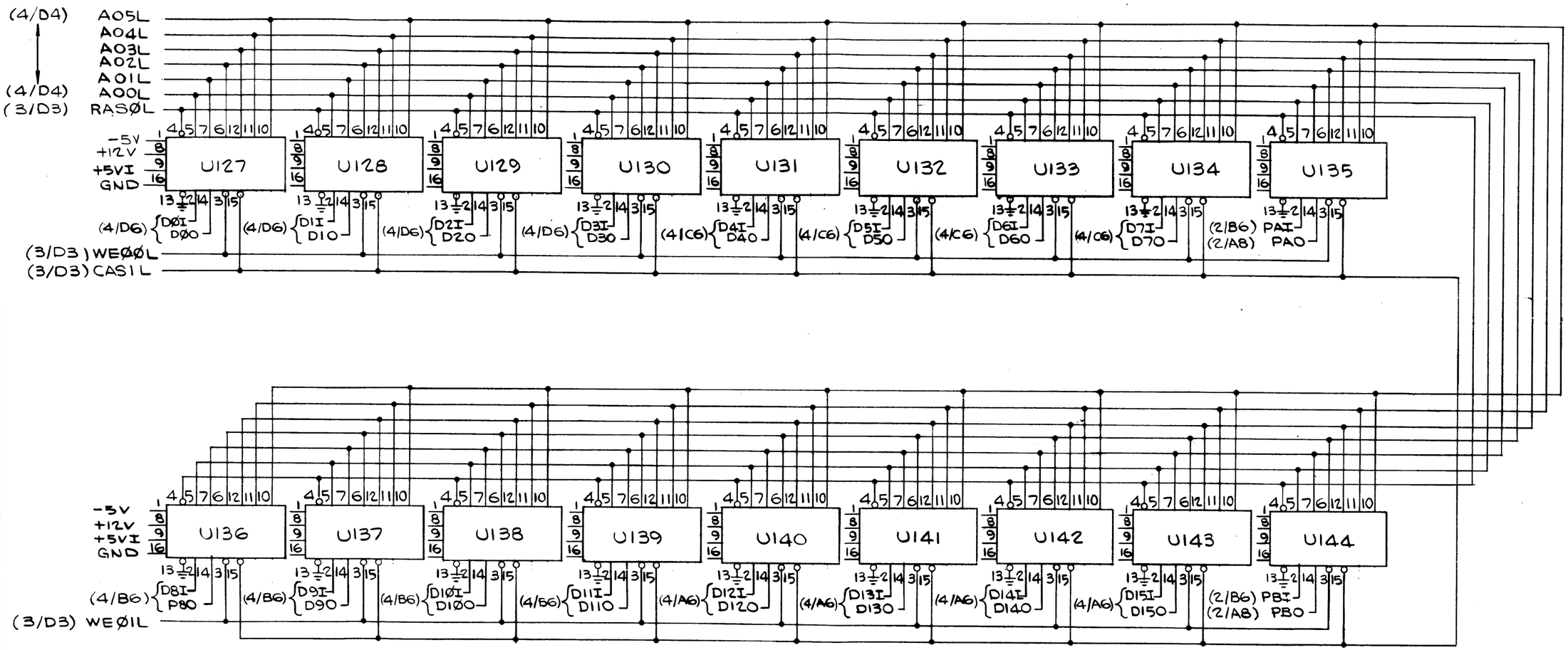

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE:	REV X5	SHEET 2 OF 14
		DISTR NO.

SKSD700755X5

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
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-5V: C1 .1, +C2 .1, C3 .1, C4 .1, C4 .1, C5 .1, C6 .1, C7 .1, C8 .1, C9 .1, C10 .1, C31 .1, C32 .1, C33 .1, C34 .1, C35 .1, C36 .1, C37 .1, C38 .1

-5V: C39 .1, C40 .1, C61 .1, C62 .1, C63 .1, C64 .1, C65 .1, C66 .1, C67 .1, C68 .1, C69 .1, C70 .1, C91 .1, C92 .1, C93 .1, C94 .1, C95 .1, C96 .1, C97 .1

-5V: C98 .1, C99 .1, C100 15, C121 .1, C122 .1, C123 .1, C124 .1, C125 .1, C126 .1, C127 .1, C128 .1, C129 .1, C130 .1, C151 .1, C152 .1, C153 .1, C154 .1, C155 .1, C156 .1

-5V: C157 .1, C158 .1, C159 .1, C160 .1, C181 .1, C182 .1, C183 .1, C184 .1, C185 .1, C186 .1, C187 .1, C188 .1, C189 .1, C190 .1, C211 .1, C212 .1, C213 .1, C214 .1, C215 .1

-5V: C216 .1, C217 .1, C218 .1, C219 .1, C220 .1, C249 4.7 10V, C258 4.7 10V, C252 15

+5VI: C11 .01 100V, C12 .01 100V, C13 .01 100V, C14 .01 100V, C15 .01 100V, C16 .01 100V, C17 .01 100V, C18 .01 100V, C19 .01 100V, C20 .01 100V

+5VI: C41 .01 100V, C42 .01 100V, C43 .01 100V, C44 .01 100V, C45 .01 100V, C46 .01 100V, C47 .01 100V, C48 .01 100V, C49 .01 100V, C50 .01 100V, C71 .01 100V, C72 .01 100V, C73 .01 100V, C74 .01 100V, C75 .01 100V, C76 .01 100V, C77 .01 100V, C78 .01 100V, C79 .01 100V

+5VI: C80 .01 100V, C101 .01 100V, C102 .01 100V, C103 .01 100V, C104 .01 100V, C105 .01 100V, C106 .01 100V, C107 .01 100V, C108 .01 100V, C109 .01 100V, C110 .01 100V, C131 .01 100V, C132 .01 100V, C133 .01 100V, C134 .01 100V, C135 .01 100V, C136 .01 100V, C137 .01 100V, C138 .01 100V

+5VI: C139 .01 100V, C140 .01 100V, C161 .01 100V, C162 .01 100V, C163 .01 100V, C164 .01 100V, C165 .01 100V, C166 .01 100V, C167 .01 100V, C168 .01 100V, C169 .01 100V, C170 .01 100V, C191 .01 100V, C192 .01 100V, C193 .01 100V, C194 .01 100V, C195 .01 100V, C196 .01 100V, C197 .01 100V

+5VI: C198 .01 100V, C199 .01 100V, C200 .01 100V, C221 .01 100V, C222 .01 100V, C223 .01 100V, C224 .01 100V, C225 .01 100V, C226 .01 100V, C227 .01 100V, C228 .01 100V, C229 .01 100V, C230 .01 100V, C254 .01 +80,-20% 16V, C259 .01 +80,-20% 16V, C268 .01 +80,-20% 16V, C281 .01 +80,-20% 16V, C282 .01 +80,-20% 16V

+5VB: C261 .01 +80,-20% 16V, C262 .01 +80,-20% 16V, C263 .01 +80,-20% 16V, C264 .01 +80,-20% 16V, C265 .01 +80,-20% 16V, C266 .01 +80,-20% 16V, C267 .01 +80,-20% 16V, C271 .01 +80,-20% 16V, C272 .01 +80,-20% 16V, C273 .01 +80,-20% 16V, C274 .01 +80,-20% 16V, C276 .01 +80,-20% 16V, C279 .01 +80,-20% 16V

+12V: C21 .1, C22 .1, C23 .1, C24 .1, C25 .1, C26 .1, C27 .1, C28 .1, C29 .1, C30 .1, C51 .1, C52 .1, C53 .1, C54 .1, C55 .1, C56 .1, C57 .1, C58 .1, C59 .1

+12V: C60 .1, C81 .1, C82 .1, C83 .1, C84 .1, C85 .1, C86 .1, C87 .1, C88 .1, C89 .1, C90 .1, C111 .1, C112 .1, C113 .1, C114 .1, C115 .1, C116 .1, C117 .1, C118 .1

+12V: C119 .1, C120 .1, C141 .1, C142 .1, C143 .1, C144 .1, C145 .1, C146 .1, C147 .1, C148 .1, C149 .1, C150 .1, C171 .1, C172 .1, C173 .1, C174 .1, C175 .1, C176 .1, C177 .1

+12V: C178 .1, C179 .1, C180 .1, C201 .1, C202 .1, C203 .1, C204 .1, C205 .1, C206 .1, C207 .1, C208 .1, C209 .1, C210 .1, C231 .1, C232 .1, C233 .1, C234 .1, C235 .1

+12V: C236 .1, C237 .1, C238 .1, C239 .1, C240 .1, C241 15 20V, C242 15 20V, C243 15 20V, C244 15 20V, C245 15 20V, C246 15 20V, C247 15 20V, C248 15 20V, C250 15 20V

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SK SD700755
SCALE:	REV X5	SHEET 13 OF 14
		DISTR NO.

SK SD700755 X5

FORM NO. 686613

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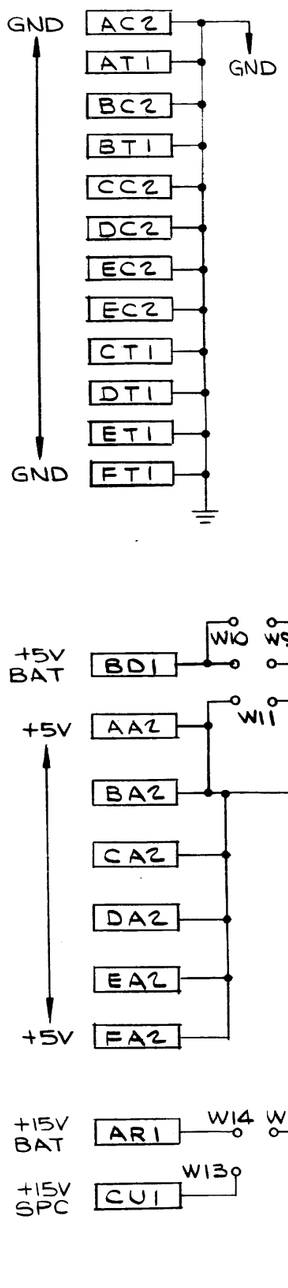
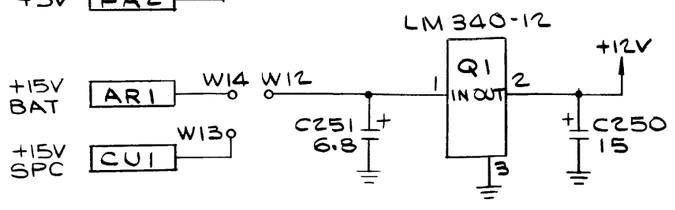
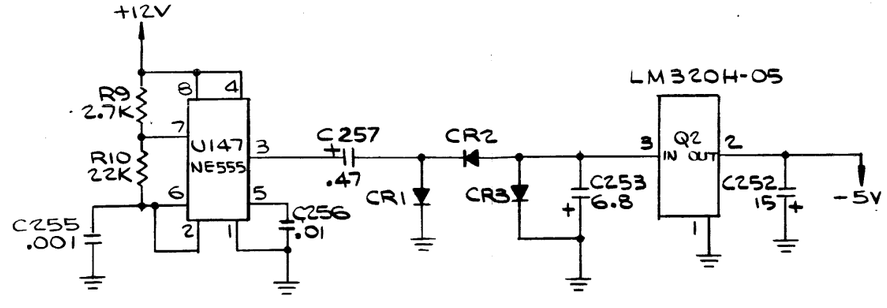
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

JUMPER WIRE CHART

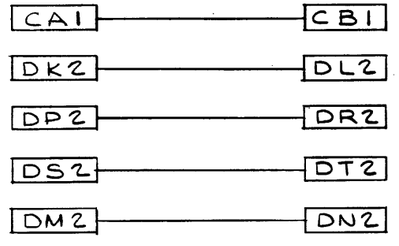
VERSION	JUMPERS		VERSION	JUMPERS	
-100, -101 -108, -109	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(11) (12)	-200, -201	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(11)
-102 -110	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(11) (12)	-202	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH, W18 to W24,	(11)
-103 -111	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(11) (12)	-203	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(11)
-104 -112	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	(11) (12)	-204	W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	(11)
-105 -113	W1 to W3, W4 to W6, W7 to W8, W9 to W11 W12 to W13, WA to WF, WC to WD, WG to WH,	(11) (12)	-205	W9 to W11, W12 to W13 WA to WF, WC to WD, WG to WH,	(11)
-106 -114	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WB to WH, WC to WD	(11) (12)	-206	W9 to W11, W12 to W13, WA to WF, WB to WH, WC to WD	(11)
-107 -115	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13 WA to WF, WA to WH, WB to WD	(11) (12)	-207	W9 to W11, W12 to W13, WA to WF, WA to WH, WB to WD	(11)







BUS GRANTS



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SKSD700755
SCALE: 1/1	REV X5	SHEET 1 OF 1
		DISTR NO.

SKSD700755 X5

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Released to Prod. per E.O. 5854	5-17-79	
B	Incorporated E.O. 3664	5-1-80	

PRODUCTION RELEASE

TABLE OF CONTENTS

DO NOT SCALE DRAWING
SCREW THREADS PER HANDBOOK H-28
COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM
REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R
ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1
STANDARD HOLE TOLERANCE PER ANSI 10387
TOLERANCES ON XX = ± .03 XXX = ± .010 ANGLES = ± 0° 30'
INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH
UNLESS OTHERWISE SPECIFIED

CONTRACT NO.

DRAWN	N. Glass	5-24-79
CHECK	N. Glass	5-24-79
DESIGN		
PROJ. ENGR.	R. Osborne	5-24-79
		5-24-79
OTHER APPROVALS		

Plessey Peripheral Systems

DRAWING TITLE: MAINTENANCE DRAWING PACKAGE

PM-S1132 Semiconductor Memory System

SIZE	CODE IDENT NO.	DWG NO.
B	52648	MD 700755

SCALE: | SHEET 1 OF 1(27)

Maintenance Drawing Package

Products Covered by this Drawing Package
PM-S1132/100
PM-S1132/108
PM-S1132/200

Plessey Peripheral Systems

PM-S1132 / 1

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REL TO PROD PER EO 2519	9-18 78	
	B	INCORP EO 3625	5-7-80	

(11) ADDRESSABLE OPTIONS (-103 & -203 VERSIONS) 8K TO 28K. CUT AND LIFT PINS U162-1 & 9. ADD JUMPERS W18 TO U162-9 (PIN) AND W17 TO U162-1 (PIN).

(2) FOR BATTERY BACK UP OPTION: VERSION -100 THRU -115, -200 THRU -207, JUMPER WIRES ARE AS FOLLOWS: W9 TO W10. W12 TO W14. ALL OTHER JUMPERS TO REMAIN THE SAME.

(9) VERSIONS -108 THRU -115:
CUT ETCH: U178-12 (SOLDER SIDE)
ADD WIRE: U181-3 TO U168-3

(8) ITEMS NOTED IN P/L MUST BE INSTALLED AND CLEANED WITH ALCOHOL ONLY AFTER ALL OTHER COMPONENTS HAVE BEEN INSTALLED AND CLEANED WITH FREON.

7. 30K OPTION - CUT ETCH U169-1 & U169-2 SOLDER SIDE. ADD JUMPER FROM W15 TO W16. ISOLATE U166-5 & U166-15 JUMPER FROM U166-5 TO U166-15. ADD 4.7K, 1/4W RESISTOR BETWEEN U166-15 & U166-16.

6. 31K OPTION - CUT ETCH AT U169-1 & U169-2 SOLDER SIDE ADD: JUMPER FROM W15 TO W16. CUT ETCH AT U188-5 & U188-6 SOLDER SIDE. ADD JUMPER FROM W25 TO W26. ISOLATE U166-5 & U166-15. JUMPER FROM U166-5 TO U166-15 ADD 4.7K, 1/4W RESISTOR BETWEEN U166-15 & U166-16.

(5) COMPONENT LEAD TRIM & SOLDER BUILD-UP TO BE AS NOTED.

(4) TRANSIPAD (ITEM 67) TO BE INSTALLED UNDER TRANSISTOR PRIOR TO INSTALLING ON BOARD.

(3) MARK ASSEMBLY VERSION NUMBER, LATEST ASSY REV. LETTER, SERIAL NUMBER AND EIA DATE CODE USING BLACK INK PER MIL-M-13231, GROUP III. LOCATE APPROX AS SHOWN.

2. FOR SCHEMATIC DIAGRAM SEE DRAWING SD 700755.

1. ASSEMBLE AND INSPECT PER WORKMANSHIP STANDARDS MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED.

BIT SIZE REF	-115	-114	-113	-112	-111	-110	-109	-108	-207	-206	-205	-204	-203	-202	-201	-200	-107	-106	-105	-104	-103	-102	-101	-100	NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION / MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
	PART/ASSY NO. & QTY PER ASSY																									PARTS LIST				
4K x 18	X																								(9)	FOR PARTS LIST SEE	PL700755-115			24
8K x 18		X																									-114			23
12K x 18			X																								-113			22
16K x 18				X																							-112			21
20K x 18					X																						-111			20
24K x 18						X																					-110			19
28K x 18							X																				-109			18
32K x 18								X																	(9)		-108			17
4K x 16									X																		-207			16
8K x 16										X																	-206			15
12K x 16											X																-205			14
16K x 16												X															-204			13
20K x 16													X												(11)		-203			12
24K x 16														X													-202			11
28K x 16															X												-201			10
32K x 16																X											-200			9
4K x 18																	X										-107			8
8K x 18																		X									-106			7
12K x 18																			X								-105			6
16K x 18																				X							-104			5
20K x 18																					X				(11)		-103			4
24K x 18																						X					-102			3
28K x 18																							X				-101			2
32K x 18																								X		FOR PARTS LIST SEE	PL700755-100			1

PART/ASSY REV LTR		
-115	FINAL	PM-S1132
-114	FINAL	PM-S1132
-113	FINAL	PM-S1132
PART NO	NEXT ASSY	USED ON
APPLICATION		

PART/ASSY REV LTR		
-112	FINAL	PM-S1132
-111	↑	↑
-110	↑	↑
-109	↑	↑
-108	↑	↑
-206	FINAL	PM-S1132
PART NO	NEXT ASSY	USED ON
APPLICATION		

PART/ASSY REV LTR		
-205	FINAL	PM-S1132
-204	↑	↑
-203	↑	↑
-202	↑	↑
-201	↑	↑
-200	↑	↑
-107	FINAL	PM-S1132
PART NO	NEXT ASSY	USED ON
APPLICATION		

PART/ASSY REV LTR		
-106	FINAL	PM-S1132
-105	↑	↑
-104	↑	↑
-103	↑	↑
-102	↑	↑
-101	↑	↑
-100	FINAL	PM-S1132
PART NO	NEXT ASSY	USED ON
APPLICATION		

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28

COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM

REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R

ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1

STANDARD HOLE TOLERANCE PER AND 10307

TOLERANCES ON: XX = ± .03 XXX = ± .010 ANGLES = ± 0° 30'

INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5

DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH

UNLESS OTHERWISE SPECIFIED

PRODUCTION RELEASE

CONTRACT NO.		
DRAWN	TYBURSKI	9-3-76
CHECK		9-8-76
ENGR		
PROJ. ENGR	D. Fox	9-13-76
PROD. DESIGN		9-13-76
OTHER APPROVALS		

Plessey Memories Incorporated
Santa Ana, California

DWG TITLE
BOARD ASSEMBLY, MEMORY PM-S1132

SIZE	CODE IDENT NO.	DWG NO.
D	52648	700755

SCALE: 1/1 SHEET 1 OF 3

DWG NO 700755 REV B1

PM-S1132/2

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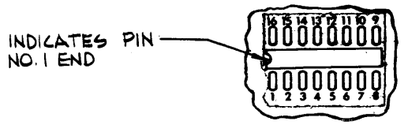
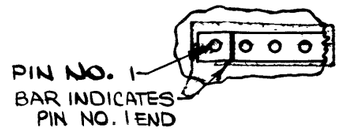
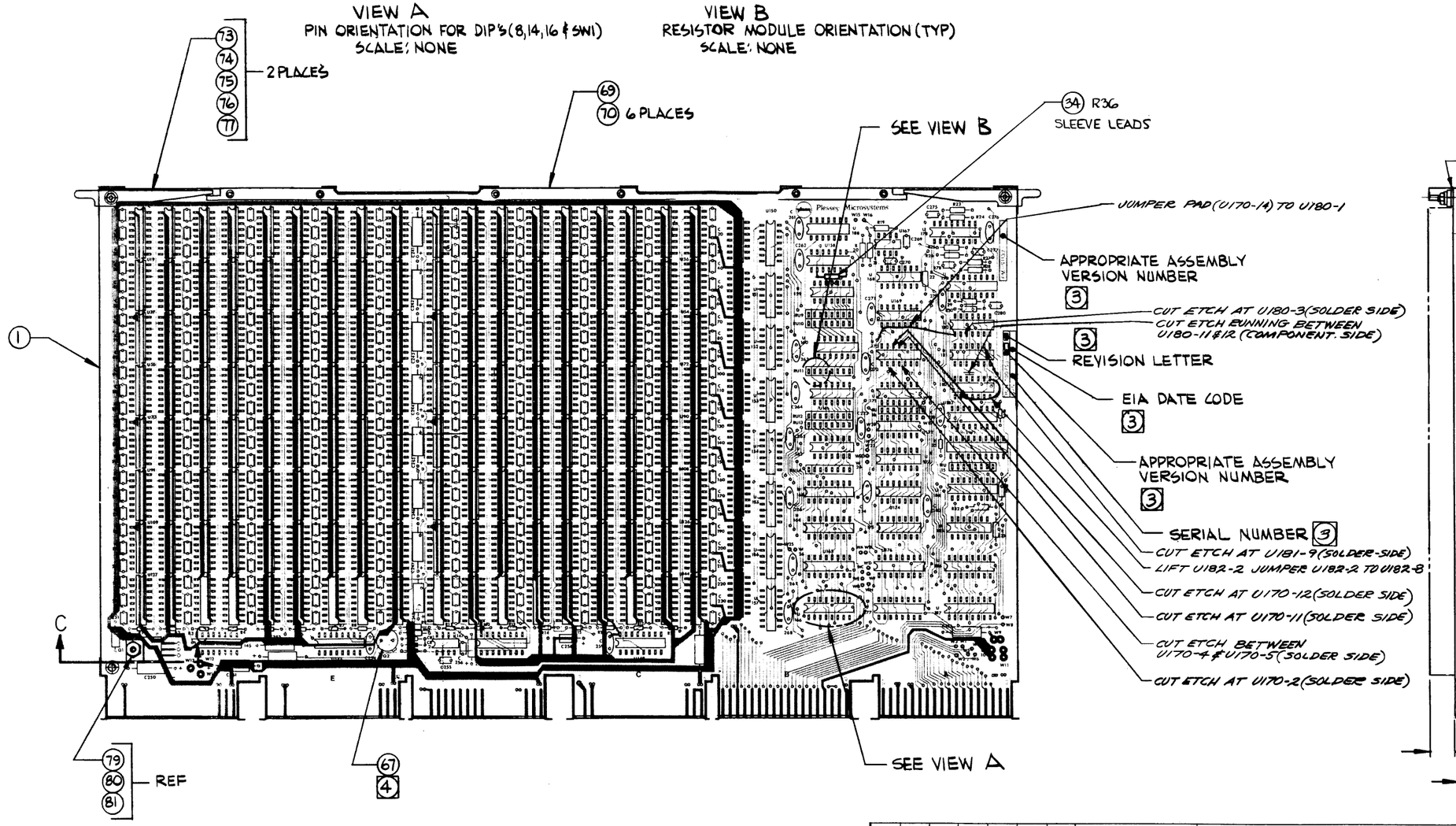
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



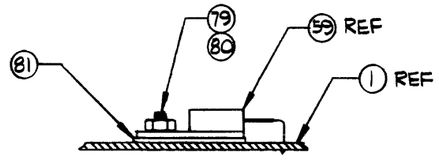
VIEW A
PIN ORIENTATION FOR DIP'S (8,14,16 & SW1)
SCALE: NONE



VIEW B
RESISTOR MODULE ORIENTATION (TYP)
SCALE: NONE



JUMPER CHART	
FROM	TO
U182-11	U181-1
U182-12	U182-7
U182-10	U170-5
U182-9	U181-12
U182-13	U182-1
U170-2	U170-4
U170-4	U181-2
U182-8	U180-1
U182-4	U170-13
U181-9	U182-6



SECTION C-C
INSTALLATION OF ITEM 59 (Q1)
SCALE: NONE

													5
													4
													3
													2
													1
PART/ASSY NO. & QTY PER ASSY						NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION / MATERIAL			SPEC/SOURCE	CODE IDENT NO.	FIND NO.
						PARTS LIST							

PART/ASSY REV LTR		
PART NO.	NEXT ASSY	USED ON
APPLICATION		

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28
COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM
REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R
ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1
STANDARD HOLE TOLERANCE PER ANSI B32.1
TOLERANCES ON: XX = ± .05 XXX = ± .030 ANGLES = ± 0° 30'
INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH
UNLESS OTHERWISE SPECIFIED

CONTRACT NO.	
DRAWN	
CHECK	
ENGR	
PROJ. ENGR	
PROD. DESIGN	
OTHER APPROVALS	

Plessey Memories Incorporated
Santa Ana, California

DWG TITLE
BOARD ASSEMBLY, MEMORY PM-S1132

SIZE	CODE IDENT NO.	DWG NO.
D	52648	700755
SCALE: 1/1	REV: B	SHEET 2 OF 3

DISTR NO. 123470

REV B
DWG NO 700755
43-011

FORM NO. 000012

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REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		

JUMPER WIRE CHART

VERSION	JUMPERS	NOTES	VERSION	JUMPERS	NOTES
-100, -101 -108, -109	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD WE to WF, WG to WH	(9) (10)	-200, -201	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(10)
-102 -110	W1 to W3, W4 to W6, W7 to W8, W9 to W11 W12 to W13, WC to WD, WE to WF, WG to WH,	(9) (10)	-202	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(10)
-103 -111	W1 to W3. W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(9) (10)	-203	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(10)
-104 -112	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	(9) (10)	-204	W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	(10)
-105 -113	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH,	(9) (10)	-205	W9 to W11, W12 to W13 WA to WF, WC to WD, WG to WH	(10)
-106 -114	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WB to WH, WC to WD	(9) (10)	-206	W9 to W11, W12 to W13, WA to WF, WB to WH WC to WD	(10)
-107 -115	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WA to WH, WB to WD	(9) (10)	-207	W9 to W11, W12 to W13, WA to WF, WA to WH, WB to WD	(10)

SIZE	CODE IDENT NO.	DWG NO.
D	52643	700755
SCALE: 1/1	REV: B	SHEET 3 OF 3

BISHOP GRAPHICS/ACCUPRESS FORM NO. 000013

M-S 1132/3

PARTS LIST | **Plessey Memories Incorporated** Santa Ana, California

PREPARED BY: KRAVANIS 23 JAN 76 | CHECKED BY: 1-27-76 | MFG ENGR: 1-27-76 | MFG MGR: P.F.X 1-27-76 | ENGR: 5-10-77

PARTS LIST NO. PL700755-100 | REV LTR A

CODE IDENT NO. 52648 | P.O. NO. 1234500 | DRAWING NO. B | SH 1 OF 9

ASSY TITLE: BOARD ASSEMBLY, MEMORY, PM-51132 32K x 18

CONTRACT NO.

LTR	DESCRIPTION	DATE	APPROVED
A	ECL TO PROD PER EO 2519-1	9-15-76	

LTR	DESCRIPTION	DATE	APPROVED

PRODUCTION RELEASE

REV STATUS OF SHEETS	REV LTR	A	A	A	A	A	A	A	A	A	
	SHEET	1	2	3	4	5	6	7	8	9	10

INTERNET SYMBOLS USED AS FOLLOWS:
A = PURCHASED ITEM; B = ALTERED ITEM; C = FABRICATED ITEM; D = SELECTED ITEM; E = SPECIFICATION OR SOURCE CONTROL ITEM; F = CUSTOMER FURNISHED ITEM; G = BULK ITEM

PARTS LIST | **Plessey Memories Incorporated** Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-100 | SH 2 | REV LTR A

CROSS INDEX OF REFERENCE DESIGNATIONS TO FIND NO.

REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.
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					56		
					57		
U188	21			Q2	58		
U147,167	22			Q1	59		
SW1	25			R20,23,25,27,&29 ARE LAB SET			
R9	26						
R33	27						
R19	28						
	29						

PARTS LIST | **Plessey Memories Incorporated** Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-100 | SH 3 | REV LTR A

ITEM ACCESS	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
		1	700754-001	PWB/MEMORY BOARD				1	B				
								2					
								3					
		1	SN7400N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		4	A				
		3	SN74S153N	I.C./DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	T.I.	01295		5	A				
		1	136000-038	I.C./ QUAD 2-INPUT POS NAND BUFFERS W/OC				6					
		1	SN74S10N	I.C./QUAD 2-INPUT EXCLUSIVE-OR GATES	T.I.	01295		7	A				
		1	SN7404N	I.C./QUAD 2-INPUT POS-OR GATES	T.I.	01295		8	A				
		3	SN74S00N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		9	A				
		2	SN74S74	I.C./DUAL D-TYPE POS EDGE-TRIGGERED FLIP-FLOPS W/PRESET/CLEAR	T.I.	01295		10	A				
		2	SN74123N	I.C./RETRIGGERABLE MONOSTABLE MULTIVIBRATORS W/CLEAR	T.I.	01295		11	A				
		1	SN74S138N	I.C/DECODERS/DEMULTIPLEXERS	T.I.	01295		12	A				
		2	9324	I.C./ 4 BIT MAGNITUDE COMPARATOR	FAIRCHILD	07263		13	A				

PARTS LIST | **Plessey Memories Incorporated** Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-100 | SH 4 | REV LTR A

ITEM ACCESS	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
		12	SN74S04N	I.C./HEX INVERTERS	T.I.	01295		14	A				
		2	SN7493A	I.C./ DECODE, DIV BY TWELVE & BINARY COUNTERS	T.I.	01295		15	A				
		1	SN7402N	I.C./QUAD 2-INPUT POS NOR GATES	T.I.	01295		16	A				
		1	SN7408N	I.C./QUAD 2-INPUT POS AND GATES	T.I.	01295		17	A				
		4	DM8837	I.C./HEX UNIFIED BUS RECEIVER	NATIONAL	27014		18	A				
		4	DS8641	I.C./ QUAD UNIFIED BUS TRANSCEIVER	NATIONAL	27014		19	A				
		144	4096-3DC 4096-6	I.C./4096-BIT RANDOM ACCESS MEMORY	FAIRCHILD MOSTEK	07263 50088		20	A				
		1	SN74H30	I.C./8 INPUT NAND GATE	T.I.	01295		21					
		2	NE-555	I.C./TIMER	SIGNETICS	18324		22	A				
								23					
								24					
		1	3-435668-0	DIP SWITCH	AMP	04618		25	A				
		1	RC07GF273J	RES/2.7K, ±5%, 1/4W	MIL-R-11			26	A				

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-100 | REV A | SHEET 1 OF 3 | SCALE

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Form 000087

PARTS LIST — **Plessey Memories Incorporated**, Santa Ana, California — CODE IDENT NO 52648 — PARTS LIST NO PL700755-100 — SH 5 — REV LTR A1

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
		1	RC07GF103J	RES/ 10K, ±5%, 1/4W	MIL-R-11			27	A				
		1	RC07GF153J	RES/ 15K ±5%, 1/4W	MIL-R-11			28	A				
								29					
		3	RC07GF273J	RES/ 27K ±5%, 1/4W	MIL-R-11			30	A				
		2	RC07GF333J	RES/ 33K ±5%, 1/4W	MIL-R-11			31	A				
		1	RC07GF102J	RES/ 1K ±5%, 1/4W	MIL-R-11			32	A				
		3	RC07GF472J	RES/ 4.7K ±5%, 1/4W	MIL-R-11			33	A				
		1	RC07GF101J	RES/100Ω ±5%, 1/4W	MIL-R-11			34	A				
		16	RC05GF330J	RES/33Ω, ±5%, 1/8W	MIL-R-11			35	A				
		1	RC07GF223J	RES/ 22K, ±5%, 1/4W	MIL-R-11			36	A				
								37					
		3	138000-001	DIODE				38	B				
		6	750-83-R33	RES MODULE, 33Ω	CTS	75378		39	A				

PARTS LIST — **Plessey Memories Incorporated**, Santa Ana, California — CODE IDENT NO 52648 — PARTS LIST NO PL700755-100 — SH 6 — REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
		8	899-3-R39	RES. MODULE, 39Ω	BECKMAN	73138		40	A				
		1	750-81-R47K	RES. MODULE, 47K	CTS	75378		41	A				
		1	150D474 X0035A2	CAP/.47uf, ±20%, 35V	SPRAGUE	05571		42	A				
		2	CK05BX102K	CAP/ .001uf ±10%, 200V	MIL-C-11015			43	A				
		2	CK05BX220K	CAP/ 22 pf ±10%, 200V	MIL-C-11015			44	A				
		1	CK05BX101K	CAP/ 100 pf ±10%, 200V	MIL-C-11015			45	A				
		160	CK05BX104K	CAP/ .1uf ±10%, 50V	MIL-C-11015			46	A				
		82	CK05BX103K	CAP/ .01uf ±10%, 100V	MIL-C-11015			47	A				
		2	150D685 X0035B2	CAP/ 6.8uf, ±20%, 35V	SPRAGUE	05571		48	A				
		18	CGA103 Z5Z	CAP/ .01uf, +80-20%, 50V	UNITRODE			49	A				
								50					
		2	150D475 X0020A2	CAP/ 4.7uf ±20%, 10V	SPRAGUE	05571		51	A				
		12	150D156 X0020B2	CAP/ 15uf ±20%, 20V	SPRAGUE	05571		52	A				

PARTS LIST — **Plessey Memories Incorporated**, Santa Ana, California — CODE IDENT NO 52648 — PARTS LIST NO PL700755-100 — SH 7 — REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
								53					
								54					
								55					
								56					
								57					
		1	LM320H-05	REGULATOR/ -5V (TO-5)	SIGNETICS	18324		58	A				
		1	LM340T-12	REGULATOR/ +12V (TO-220)	SIGNETICS	18324		59	A				
								60					
								61					
								62					
								63					
								64					
								65					

PARTS LIST — **Plessey Memories Incorporated**, Santa Ana, California — CODE IDENT NO 52648 — PARTS LIST NO PL700755-100 — SH 8 — REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
								66					
		1	10079	TRANSIPAD (TO-5)	MILTON ROSS	07047		67	A				
								68					
		1	700407-001	STIFFENER				69	B				
		6	N-440-1/4	SCREW/ 4-40 X 1/4 NYLON BINDER HEAD	WECKESSER	95987		70	A				
								71					
								72					
		2	700330-001	HANDLE/ EXTRACTOR				73	B				
		2	700331-001	SPACER				74	B				
		2	MS51957-4	SCREW/ 2-56 X 5/16				75	G				
		2	NAS1291C02	NUT/HEX, #2, SELF-LOCKING				76	G				
		2	NW4-2814	WASHER, NYLON	WECKESSER	95987		77	A				
								78					

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-100 | REV A | SHEET 2 of 3 | SCALE

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Form 000087

PARTS LIST	Plessey Memories Incorporated, Santa Ana, California	CODE IDENT NO. 52648	PARTS LIST NO. PL700755-100	SH 9	REV LTR A

ITEM NO.	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	STM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
		1	N-440-1/4	SCREW-NYLON, 4-40 X 1/4 LG FLAT HEAD, COLOR; NATURAL	WECKESSER	95987		79	A				
		1	N-440-X	NUT-NYLON, 4-40, COLOR: NATURAL	WECKESSER	95987		80	A				
		1	7903-10-51	INSULATOR	BERGQUIST COMP.			81	A				
		AR	5952	WIRE (28 AWG KYNAR INSUL.) COLOR: OPTIONAL	ALPHA	23172		82	A				
		AR	SN63WRAP3	SOLDER	QQ-S-571			83	G				

SIZE	CODE IDENT NO.	DWG NO.	REV
B	52648	PL 700755-100	A

SCALE

SHEET 3 of 3

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PARTS LIST | Plessey Microsystems

ASSY TITLE: BOARD ASSY, MEMORY, PM-S1132 32K X 18

PREPARED BY: L. LAMBERT 10-14-77 | CHECKED BY: J. Trenkle 2-1-78 | NEXT HIGHER ASSY: RB 2-1-78 | NEXT HIGHER ASSY: R.R. Johnston 2-1-78 | APPROVED: D. Davis 9-11-78

PARTS LIST NO. PL 700755-108 | REV LTR A | CODE IDENT NO. 52648 | DWG NO. 1234520 REV B | SH 1 OF 9

CONTRACT NO

LTR	DESCRIPTION	DATE	APPROVED
A	REL TO PROD PER EO 2519	9-11-78	

PRODUCTION RELEASE

REV STATUS OF SHEETS	REV LTR	A	A	A	A	A	A	A	A	A	
	SHEET	1	2	3	4	5	6	7	8	9	10

INTERPRET SYMBOLS USED AS FOLLOWS:

A = PURCHASED ITEM; B = FABRICATED ITEM; C = SPECIFICATION OR SOURCE CONTROL ITEM; D = ALTERED ITEM; E = SELECTED ITEM; F = CUSTOMER FURNISHED ITEM; G = REFERENCE ITEM

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-108 | SH 3 | REV LTR A

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
	1	700754-001	PWB/MEMORY BOARD				1	B				
							2					
							3					
	1	SN7400N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		4	A				
	3	SN74S153N	I.C./DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	T.I.	01295		5	A				
	1	136000-038	I.C/ QUAD 2-INPUT POS NAND BUFFERS W/OC				6					
	1	SN74S10N	I.C./QUAD 2-INPUT EXCLUSIVE-OR GATES	T.I.	01295		7	A				
	1	SN7404N	I.C./QUAD 2-INPUT POS-OR GATES	T.I.	01295		8	A				
	3	SN74S00N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		9	A				
	2	SN74S74	I.C./DUAL D-TYPE POS EDGE-TRIGGERED FLIP-FLOPS W/PRESET/CLEAR	T.I.	01295		10	A				
	2	SN74123N	I.C./RETRIGGERABLE MONOSTABLE MULTIVIBRATORS W/CLEAR	T.I.	01295		11	A				
	1	SN74S138N	I.C/DECODERS/DEMULTIPLEXERS	T.I.	01295		12	A				
	2	9324	I.C./ 4 BIT MAGNITUDE COMPARATOR	FAIRCHILD	07263		13	A				

PARTS LIST | Plessey Microsystems | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-108 | SH 2 | REV LTR A

CROSS INDEX OF REFERENCE DESIGNATIONS TO FIND NO.

REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.
U158	4	R24,26,30	30	C11-20, 41-50,	47		
U163-165	5	R21,28	31	71-80, 101-110			
U185	6	R22	32	131-140, 161-170			
U170	7	R31,32,34	33	191-200, 221-230			
U180	8	R36	34	256, 269			
U172,173,181	9	R1-8, R11-18	35	C251, 253	48		
U168,182	10	R10	36	C254, 259, 261-268	49		
U178,179	11		37	271-274, 276, 279,			
U176	12	CR1-3	38	281, 282			
U183,184	13	RU9-14	39		50		
U150-157, 159-162	14	RU1-8	40	C249, 258	51		
U174,175	15	RU15	41	C241-248, 250	52		
U171	16	C257	42	252, 260, 283			
U169	17	C255, 270	43		53		
U166,177,186,187	18	C275, 278	44		54		
U145,146,148,149	19	C280	45		55		
U1-144	20	C1-10, 21-40	46		56		
		51-70, 81-100			57		
		111-130, 141-160		Q2	58		
U188	21	171-190, 201-220		Q1	59		
U147,167	22	231-240		R20,23,25,27 & 29 ARE LAB SET			
SW1	25						
R9	26						
R33	27						
R19	28						
	29						

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-108 | SH 4 | REV LTR A

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
	12	SN74S04N	I.C./HEX INVERTERS	T.I.	01295		14	A				
	2	SN7493A	I.C./ DECODE, DIV BY TWELVE & BINARY COUNTERS	T.I.	01295		15	A				
	1	SN7402N	I.C./QUAD 2-INPUT POS NOR GATES	T.I.	01295		16	A				
	1	SN7408N	I.C./QUAD 2-INPUT POS AND GATES	T.I.	01295		17	A				
	4	DM8837	I.C./HEX UNIFIED BUS RECEIVER	NATIONAL	27014		18	A				
	4	DS8641	I.C./ QUAD UNIFIED BUS TRANSCEIVER	NATIONAL	27014		19	A				
	144	4027-2	I.C./ 4096-BIT RANDOM ACCESS MEMORY	FAIRCHILD MOSTEK	07263 50088		20	A				
	1	SN74H30	I.C/8 INPUT NAND GATE	T.I.	01295		21					
	2	NE-555	I.C./ TIMER	SIGNETICS	18324		22	A				
							23					
							24					
	1	3-435668-0	DIP SWITCH	AMP	04618		25	A				
	1	RC07GF 272J	RES/ 2.7K, ±5%, 1/4W	MIL-R-11			26	A				

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-108 | REV A | SHEET 1 of 3 | SCALE

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Form 000087

PM-S1132

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO 52648 | PARTS LIST NO PL700755-108 | SH 5 | REV A

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
	1	RC07GF103J	RES/ 10K, ±5%, 1/4W	MIL-R-11			27	A				
	1	RC07GF153J	RES/ 15K ±5%, 1/4W	MIL-R-11			28	A				
							29					
	3	RC07GF273J	RES/ 27K ±5%, 1/4W	MIL-R-11			30	A				
	2	RC07GF333J	RES/ 33K ±5%, 1/4W	MIL-R-11			31	A				
	1	RC07GF102J	RES/ 1K ±5%, 1/4W	MIL-R-11			32	A				
	3	RC07GF472J	RES/ 4.7K ±5%, 1/4W	MIL-R-11			33	A				
	1	RC07GF101J	RES/100Ω ±5%, 1/4W	MIL-R-11			34	A				
	16	RC05GF330J	RES/33Ω, ±5%, 1/8W	MIL-R-11			35	A				
	1	RC07GF223J	RES/ 22K, ±5%, 1/4W	MIL-R-11			36	A				
							37					
	3	138000-001	DIODE				38	B				
	6	750-83-R33	RES MODULE, 33Ω	CTS	75378		39	A				

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO 52648 | PARTS LIST NO PL700755-108 | SH 6 | REV A

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
	8	899-3-R39	RES. MODULE, 39Ω	BECKMAN	73138		40	A				
	1	750-81-R47K	RES. MODULE, 47K	CTS	75378		41	A				
	1	150D474 X0035A2	CAP/.47uf, ±20%, 35V	SPRAGUE	05571		42	A				
	2	CK05BX102K	CAP/ .001uF ±10%; 200V	MIL-C-11015			43	A				
	2	CK05BX220K	CAP/ 22 pF ±10%, 200V	MIL-C-11015			44	A				
	1	CK05BX101K	CAP/ 100 pf ±10%, 200V	MIL-C-11015			45	A				
	160	CK05BX104K	CAP/ .1uF ±10%, 50V	MIL-C-11015			46	A				
	82	CK05BX103K	CAP/ .01uF ±10%, 100V	MIL-C-11015			47	A				
	2	150D685 X0035B2	CAP/ 6.8 uf, ±20%, 35V	SPRAGUE	05571		48	A				
	18	CGA103 Z02	CAP/ .01uF +80-20%, 50V	UNITRODE			49	A				
							50					
	2	150D475 X0020A2	CAP/ 4.7uF ±20%, 10V	SPRAGUE	05571		51	A				
	12	150D156 X0020B2	CAP/ 15uF ±20%, 20V	SPRAGUE	05571		52	A				

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO 52648 | PARTS LIST NO PL700755-108 | SH 7 | REV A

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
							53					
							54					
							55					
							56					
							57					
	1	LM320H-05	REGULATOR/ -5V (TO-5)	SIGNETICS	18324		58	A				
	1	LM340T-12	REGULATOR/ +12V (TO-220)	SIGNETICS	18324		59	A				
							60					
							61					
							62					
							63					
							64					
							65					

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO 52648 | PARTS LIST NO PL700755-108 | SH 8 | REV A

NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
							66					
	1	10079	TRANSIPAD (TO-5)	MILTON ROSS	01047		67	A				
							68					
	1	700407-001	STIFFENER				69	B				
	6	N-440-1/4	SCREW/ 4-40 X 1/4 NYLON BINDER HEAD	WECKESSER	95987		70	A				
							71					
							72					
	2	700330-001	HANDLE/ EXTRACTOR				73	B				
	2	700331-001	SPACER				74	B				
	2	MS51957-4	SCREW/ 2-56 X 5/16				75	G				
	2	NAS1291C02	NUT/HEX, #2, SELF-LOCKING				76	G				
	2	NW4-2814	WASHER, NYLON	WECKESSER	95987		77	A				
							78					

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-108 | REV A | SHEET 2 of 3 | SCALE

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Form 000087

PARTS LIST	Plessey Memories Incorporated, Santa Ana, California	CODE IDENT NO 52648	PARTS LIST NO PL700755-108	SH 9	REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE: C/I CODE	INV ON HAND	PAR	UNIT COST
		1	N-440-1/4	SCREW-NYLON, 4-40 X 1/4 LG FLAT HEAD, COLOR; NATURAL	WECKESSER	95987		79	A				
		1	N-440-X	NUT-NYLON, 4-40, COLOR: NATURAL	WECKESSER	95987		80	A				
		1	7903-10-51	INSULATOR	BERGQUIST COMP.			81	A				
		AR	5952	WIRE/ 28 AWG KYNAR INSUL.) COLOR: OPTIONAL	ALPHA	23172		82	A				
		AR	SN63WRAP3	SOLDER	QQ-S-571			83	G				

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-106 | REV A | SCALE | SHEET 3 of 3

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Form 000087

PARTS LIST | Plessey Peripheral Systems

BOARD ASSY, MEMORY, PM-S1132, 32K X 16

PREPARED BY	[illegible]	8-19-76
CHECKED BY	[illegible]	8-20-76
RESP ENG	J. BELL	9-16-76
APPRV	D. [illegible]	9-7-76
DOC CONTROL	[illegible]	9-19-76

PARTS LIST NO. PL700755-200 | REV LTR A

CODE IDENT NO. 52648 | DWG NO. 1234570 REV B | SH 1 OF 9

MODEL NO.

LTR	DESCRIPTION	DATE	APPROVED
A	REL TO PROD PER ECO 2519	9-15-76	[illegible]

PRODUCTION RELEASE

REV STATUS OF SHEETS											
REV LTR	A	A	A	A	A	A	A	A	A		
SHEET	1	2	3	4	5	6	7	8	9	10	

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 3 | REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	STM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
		1	700754-001	PWB/MEMORY BOARD				1	B				
								2					
								3					
		1	SN7400N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		4	A				
		3	SN74S153N	I.C./DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	T.I.	01295		5	A				
		1	136000-038	I.C./ QUAD 2-INPUT POS NAND BUFFERS W/OC				6					
		1	SN74S10N	I.C./QUAD 2-INPUT EXCLUSIVE-OR GATES	T.I.	01295		7	A				
		1	SN7404N	I.C./QUAD 2-INPUT POS-OR GATES	T.I.	01295		8	A				
		3	SN74S00N	I.C./QUAD 2-INPUT POS NAND GATES	T.I.	01295		9	A				
		2	SN74S74	I.C./DUAL D-TYPE POS EDGE-TRIGGERED FLIP-FLOPS W/PRESET/CLEAR	T.I.	01295		10	A				
		2	SN74123N	I.C./RETRIGGERABLE MONOSTABLE MULTIVIBRATORS W/CLEAR	T.I.	01295		11	A				
		1	SN74S138N	I.C/DECODERS/DEMULTIPLEXERS	T.I.	01295		12	A				
		2	9324	I.C./4 BIT MAGNITUDE COMPARATOR	FAIRCHILD	07263		13	A				

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 2 | REV LTR A

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R20,23,25,27,&29 ARE LAB SET	

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 4 | REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	STM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
		12	SN74S04N	I.C./HEX INVERTERS	T.I.	01295		14	A				
		2	SN7493A	I.C./ DECODE, DIV BY TWELVE & BINARY COUNTERS	T.I.	01295		15	A				
		1	SN7402N	I.C./QUAD 2-INPUT POS NOR GATES	T.I.	01295		16	A				
		1	SN7408N	I.C./QUAD 2-INPUT POS AND GATES	T.I.	01295		17	A				
		4	DM8837	I.C./HEX UNIFIED BUS RECEIVER	NATIONAL	27014		18	A				
		4	DS8641	I.C./ QUAD UNIFIED BUS TRANSCEIVER	NATIONAL	27014		19	A				
		128	4096-3DC 4096-6	I.C./4096-BIT RANDOM ACCESS MEMORY	FAIRCHILD MOSTEK	07263 50088		20	A				
		1	SN74H30	I.C./8 INPUT NAND GATE	T.I.	01295		21	A				
		2	NE-555	I.C./TIMER	SIGNETICS	18324		22	A				
								23					
								24					
		1	3-435 668-0	DIP SWITCH	AMP	04618		25	A				
		1	RC07GF 273J	RES/2.7K, ±5%, 1/4W	MIL-R-11			26	A				

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-200 | REV A | SHEET 1 of 3 | SCALE

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Form 000087

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 5 | REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
		1	RC07GF103J	RES/ 10K, ±5%, 1/4W	MIL-R-11			27	A				
		1	RC07GF153J	RES/ 15K ±5%, 1/4W	MIL-R-11			28	A				
								29					
		3	RC07GF273J	RES/ 27K ±5%, 1/4W	MIL-R-11			30	A				
		2	RC07GF333J	RES/ 33K ±5%, 1/4W	MIL-R-11			31	A				
		1	RC07GF102J	RES/ 1K ±5%, 1/4W	MIL-R-11			32	A				
		3	RC07GFA72J	RES/ 4.7K ±5%, 1/4W	MIL-R-11			33	A				
		1	RC07GF101J	RES/ 100Ω ±5%, 1/4W	MIL-R-11			34					
		16	RC05GF330J	RES/ 33Ω, ±5%, 1/8W	MIL-R-11			35	A				
		1	RC07GF223J	RES/ 22K, ±5%, 1/4W	MIL-R-11			36	A				
								37					
		3	138000-001	DIODE				38	B				
		6	750-83-R33	RES MODULE, 33Ω	CTS	75378		39	A				

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 6 | REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
		8	899-3-R39	RES. MODULE, 39Ω	BECKMAN	73138		40	A				
		1	750-81-R4.7K	RES. MODULE, 4.7K	CTS	75378		41	A				
		1	150D474 X0035A2	CAP/ .47μf, ±20%, 35V	SPRAGUE	05571		42	A				
		2	CK05BX102K	CAP/ .001μf ±10%, 200V	MIL-C-11015			43	A				
		2	CK05BX220K	CAP/ 22 pf ±10%, 200V	MIL-C-11015			44	A				
		1	CK05BX101K	CAP/ 100 pf ±10%, 200V	MIL-C-11015			45	A				
		160	CK05BX104K	CAP/ .1μf ±10%, 50V	MIL-C-11015			46	A				
		82	CK05BX103K	CAP/ .01μf ±10%, 100V	MIL-C-11015			47	A				
		2	150D685 X0035B2	CAP/ 6.8μf, ±20%, 35V	SPRAGUE	05571		48	A				
		18	CGA105 Z5Z	CAP/ .01μf +80-20%, 50V	UNITRODE			49	A				
								50					
		2	150D475 X0020A2	CAP/ 4.7μf ±20%, 10V	SPRAGUE	05571		51	A				
		12	150D156 X0020B2	CAP/ 15μf ±20%, 20V	SPRAGUE	05571		52	A				

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 7 | REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
								53					
								54					
								55					
								56					
								57					
		1	LM320H-05	REGULATOR/ -5V (TO-5)	SIGNETICS	18324		58	A				
		1	LM340T-12	REGULATOR/ +12V (TO-220)	SIGNETICS	18324		59	A				
								60					
								61					
								62					
								63					
								64					
								65					

PARTS LIST | Plessey Memories Incorporated, Santa Ana, California | CODE IDENT NO. 52648 | PARTS LIST NO. PL700755-200 | SH 8 | REV LTR A

ITEM	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	SYM	C/I USAGE C/I CODE	INV ON HAND	PAR	UNIT COST
								66					
		1	10079	TRANSIPAD (TO-5)	MILTON ROSS	07047		67	A				
								68					
		1	700407-001	STIFFENER				69	B				
		6	N-440-1/4	SCREW/ 4-40 X 1/4 NYLON BINDER HEAD	WECKESSER	95987		70	A				
								71					
								72					
		2	700330-001	HANDLE/ EXTRACTOR				73	B				
		2	700331-001	SPACER				74	B				
		2	MS51957-4	SCREW/ 2-56 X 5/16				75	G				
		2	NAS1291C02	NUT/ HEX, #2, SELF-LOCKING				76	G				
		2	NWM-2814	WASHER, NYLON	WECKESSER	95987		77	A				
								78					

SIZE B | CODE IDENT NO. 52648 | DWG NO. PL 700755-200 | REV A | SHEET 2 of 3 | SCALE

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Form 000087

PARTS LIST	Plessey Memories Incorporated, Santa Ana, California	CODE IDENT NO. 52648	PARTS LIST NO. PL700755-200	SH 9	DWG LTR A

ITEM NO.	NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIND NO.	STM	C/I USAGE C/I CODE	C/I USAGE INV ON HAND	C/I USAGE PAR	C/I USAGE UNIT COST
		1	N-440-1/4	SCREW-NYLON, 4-40 X 1/4 LG FLAT HEAD, COLOR; NATURAL	WECKESSER	95987		79	A				
		1	N-440-X	NUT-NYLON, 4-40, COLOR; NATURAL	WECKESSER	95987		80	A				
		1	7903-10-51	INSULATOR	BERGQUIST COMP.			81	A				
		AR	5952	WIRE / 28 AWG KYNAR INSUL., COLOR: OPTIONAL	ALPHA	23172		82	A				
		AR	SN63WRAP3	SOLDER	QQ-S-571			83	G				

SIZE	CODE IDENT NO.	DWG NO.	REV	SHEET
B	52648	PL 700755-200	A	3 of 3
SCALE				

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Form 000087

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REL TO PROD PER EO 2519	7.18.78	
	B	INCORP EO 3625	5-7-80	

LAST DESIGNATION USED	
RESISTOR	R36
RESISTOR MODULE	RU15
CAPACITOR	C283
INTEGRATED CKT	U188
DIODE	CR3

NOT USED	
C277	CAPACITOR
R35	RESISTOR

REF DESIG	GATES USED PER TOTAL	PART NUMBER
U180	5/6	SN7404

SOLDER SIDE — A CONNECTOR — COMPONENT SIDE

SIDE 2		SIDE 1
	V	
	U	
	T	GND
	S	
	R	+15V
	P	PAR PØ
PBL	N	PAR P1
D15L	M	PAL
D13L	L	D14L
D11L	K	D12L
DØ9L	J	D10L
DØ7L	H	DØ8L
DØ5L	F	DØ6L
DØ3L	E	DØ4L
DØ1L	D	DØ2L
GND	C	DØØL
	B	
+5V	A	

SOLDER SIDE — B CONNECTOR — COMPONENT SIDE

	V	MSYNL
CØL	U	SSYNL
C1L	T	GND
A16L	S	A17L
A14L	R	A15L
A12L	P	A13L
A10L	N	A11L
A08L	M	AØ9L
A06L	L	AØ7L
A04L	K	AØ5L
A02L	J	AØ3L
A00L	H	AØ1L
DC LØ	F	
PAR DET	E	INT SSYN
	D	+5V BAT
GND	C	
	B	
+5V	A	

SOLDER SIDE — C CONNECTOR — COMPONENT SIDE

SIDE 2		SIDE 1
	V	
	U	+15 SPC
	T	GND
	S	
	R	
	P	
	N	
	M	
	L	
	K	
	J	
	H	
	F	
	E	
	D	
END	C	
	B	NPG OUT
+5V	A	NPG IN

SOLDER SIDE — D CONNECTOR — COMPONENT SIDE

SIDE 2		SIDE 1
	V	
	U	
BG4 OUT	T	
BG4 IN	S	
BG5 OUT	R	
BG5 IN	P	
BG6 OUT	N	
BG6 IN	M	
BG7 OUT	L	
BG7 IN	K	
	J	
	H	
	F	
	E	
	D	
GND	C	
	B	
+5V	A	

SOLDER SIDE — E CONNECTOR — COMPONENT SIDE

SIDE 2		SIDE 1
	V	
	U	
	T	GND
	S	
	R	
	P	
	N	
	M	
	L	
	K	
	J	
	H	
	F	
	E	
	D	
GND	C	
	B	
+5V	A	

[13] 8K TO 28K ADDRESSABLE OPTION FOR -103 & -203 VERSIONS: CUT AND LIFT U162-1 & 9. ADD WIRES FROM W18 TO U162-9 & FROM W17 TO U162-1.

[12] FOR VERSIONS -105 THRU -115:
(A) CUT ETCH: U178-2 (SOLDER SIDE)
(B) ADD JUMPER: U181-3 TO U168-3

6. 30K OPTION
CUT ETCH U169-1 & U169-2, SOLDER SIDE.
ADD: W15 TO W16.

5. 31K OPTION
CUT ETCH U169-1 & U169-2, SOLDER SIDE.
ADD: W15 TO W16.
CUT ETCH U188-5 & U188-6 SOLDER SIDE.
ADD: W25 TO W26.

4. ALL CAPACITOR VALUES ARE IN μF, 50V.

[3] VALUES ARE LAB SET PER TEST SPEC TS700755

2. ALL DIODES ARE 138000-001.

1. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

11. FOR BATTERY BACKUP OPTION: VERSION -100 THRU -115, -200 THRU -207, JUMPER WIRES ARE AS FOLLOWS: W9 TO W10, W12 TO W14. ALL OTHER JUMPERS TO REMAIN THE SAME.

10. DESIGNATIONS SHOWN IN PARENTHESES (2/A3) INDICATES WHERE SIGNAL ORIGNATES OR TERMINATES
ZONE DESIGNATION
SHEET NUMBER

9 SIGNALS SHOWN IN RECTANGLE
AA2 ARE I/O CONNECTIONS
BOARD SIDE
PIN DESIGNATION
CONNECTOR DESIGNATION

PRODUCTION RELEASE

NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION / MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
PART/ASSY NO. & QTY PER ASSY		PARTS LIST			

PART/ASSY REV LTR

SD700355-100 TS1132

PART NO. | NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28
COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM
REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010
ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1
STANDARD HOLE TOLERANCE PER ANSI B5.10
TOLERANCES ON: XX = ± .03 XXX = ± .010 ANG = ± 0° 30'
INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH
UNLESS OTHERWISE SPECIFIED

CONTRACT NO.

DRAWN	A. W. BLANK	4/13/76
CHECK	D. Wentink	8-11-76
ENGR		
PROJ. ENGR		
PROD. DESIGN		8/16/76
OTHER		
APPROVALS		

Plessey Memories Incorporated
Santa Ana, California

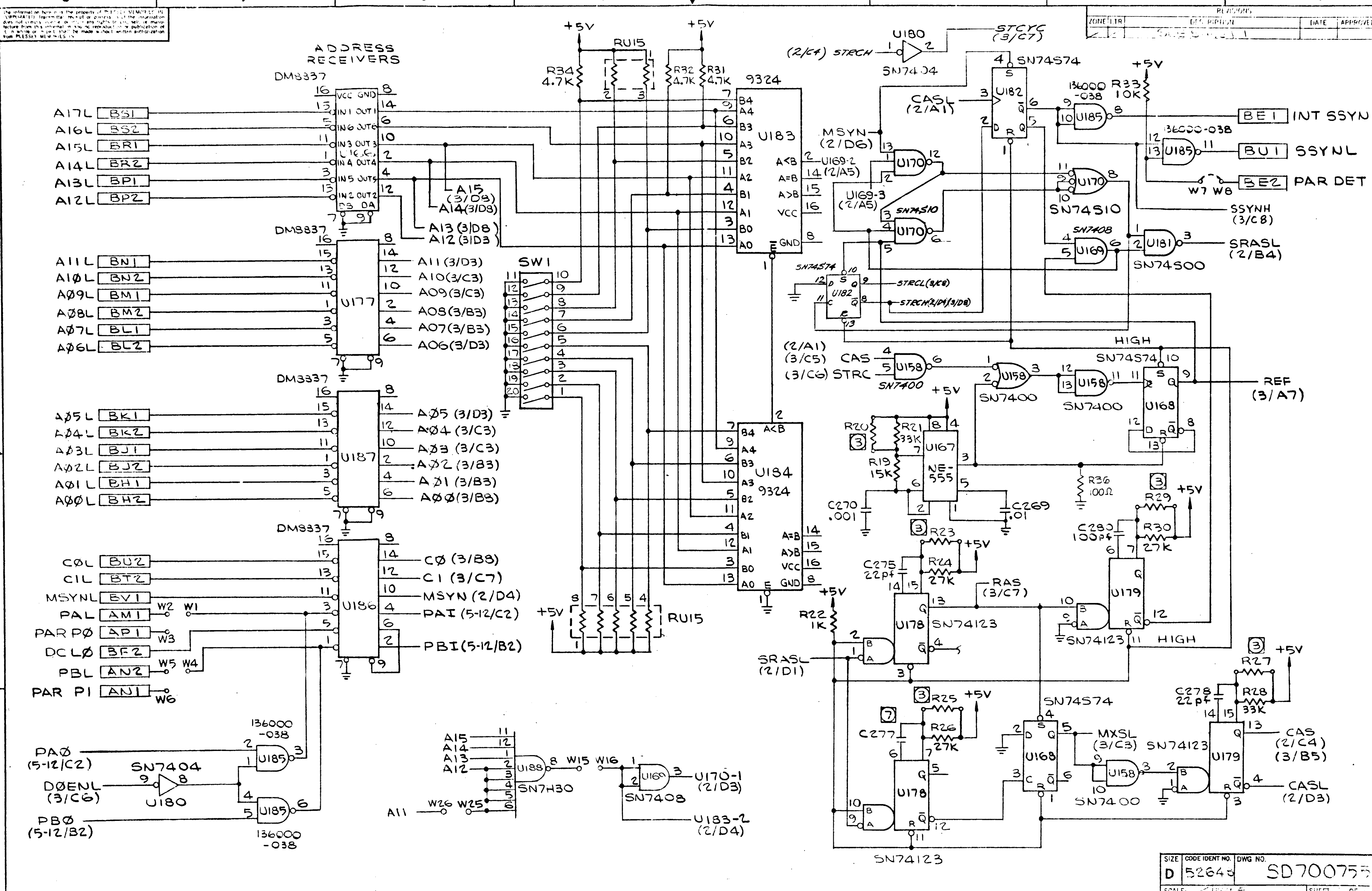
DWG TITLE
SCHEMATIC DIAGRAM
MEMORY SYSTEM
PM-5113Z

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755

SCALE: NONE | SHEET 1 OF 14

DISTR NO. 1929C0 N

SD700755 B



SIZE D | CODE IDENT NO. 52643 | DWG NO. SD700755

SCALE: | SHEET

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

ROW SELECT
SN74S138
U176
(2/C4) STECH
(2/D6) A15 WE, A14 WG, A13 WC
WA, WB, WC, WD, WF, WH
RAS
SN74S00
U181
U180
SN7404
STRCL (2/C3)
STRC (2/C4)
SSYNH (2/C1)
(2/B6) C1
DØENL (2/A3)(4/C8)
SN7402
SN7408
CØ (2/B6)
AØØ (2/B6)
+5V
U173
U172
W24
W23
W21
W22
W20
W17
W18
W19
SN74S04
U162
U161
U163
U159
33
RAS ØL (11-12/C8)
CAS ØL
WEØØL (11-12/C8)
RAS IL (11/C8)
CAS IL (11-12/C8)
WEOIL (11-12/C8)
RAS 2L (10/C8)
CAS 2L (10/C8)
WE2ØL (9-10/C8)
RAS 3L (9/C8)
CAS 3L (9/C8)
WE3ØL (9-10/C8)
RAS 4L (8/C8)
CAS 4L (8/C8)
WE4ØL (7-8/C8)
RAS 5L (7/C8)
CAS 5L (7/C8)
WE5ØL (7-8/B8)
RAS 6L (6/C8)
CAS 6L (6/C8)
WE6ØL (5-6/C8)
RAS 7L (5/C8)
CAS 7L (5/C8)
WE7ØL (5-6/B8)
CAS (2/A1)
ADDRESS MUX
SN74153
U165
U164
U163
(2/C6) A12
A06 (2/C6)
(2/C6) A11
(2/C6) A05
MXSL (2/A2)
(2/C6) A10
(2/C6) A04
(2/C6) A09
(2/C6) A03
(2/C6) A08
(2/B6) A02
(2/C6) A07
(2/B6) A01
AD5 (4/D5)
AD4 (4/D5)
AD3 (4/D5)
AD2 (4/D5)
AD1 (4/D5)
ADØ (4/D5)
SN7493A
U175
U174
RA5
RA4
RA3
RA2
RA1
RAØ
(2/C1) REF

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: A	SHEET 3 OF 14
		DISTR NO.

SD700755 B

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REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		

DATA TRANSCEIVERS

DS8641 U145

DØØL	AC1	1	BUS3	IN3	2 — DØØI (5-12/C8)
				OUT3	3 — R1 33 — DØ1I
DØ1L	AD2	4	BUS4	IN4	5 — D10I (5-12/C7)
		8	GND	OUT4	6 — R2 33 — D11I
DØ2L	AD1	15	BUS1	IN1	14 — D20I (5-12/C6)
		16	VCC	OUT1	13 — R3 33 — D21I
				IN2	11 — D30I (5-12/C6)
DØ3L	AE2	12	BUS2	OUT2	10 — R4 33 — D31I
			G3	G4	7, 9

DØENL (3/C6)

DS8641 U146

DØ4L	AE1	1			2 — D40I (5-12/C5)
					3 — R5 33 — D41I
DØ5L	AF2	4			5 — D50I (5-12/C4)
		8			6 — R6 33 — D51I
DØ6L	AF1	15			14 — D60I (5-12/C3)
		16			13 — R7 33 — D61I
DØ7L	AH2	12			11 — D70I (5-12/C3)
					10 — R8 33 — D71I
					7, 9

DS8641 U148

D08L	AH1	1			2 — D80I (5-12/B8)
					3 — R11 33 — D81I
D09L	AJ2	4			5 — D90I (5-12/B7)
		8			6 — R12 33 — D91I
D10L	AJ1	15			14 — D100I (5-12/B6)
		16			13 — R13 33 — D101I
D11L	AK2	12			11 — D110I (5-12/B6)
					10 — R14 33 — D111I
					7, 9

DS8641 U149

D12L	AK1	1			2 — D120I (5-12/B5)
					3 — R15 33 — D121I
D13L	AL2	4			5 — D130I (5-12/B4)
		8			6 — R16 33 — D131I
D14L	AL1	15			14 — D140I (5-12/B3)
		16			13 — R17 33 — D141I
D15L	AM2	12			11 — D150I (5-12/B3)
					10 — R18 33 — D151I
					7, 9

ADDRESS DRIVERS

SN74S04 RU8 U157

(3/B1) AD0	1	9	3	13	11	5
(3/B1) AD1	9	8	4	12	10	6
(3/B1) AD2	3	13	11	5		
(3/B1) AD3	13	12	10	6		
(3/B1) AD4	11	11	12	8		
(3/D1) AD5	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		AØØL	AØ1L	AØ2L	AØ3L	AØ4L AØ5L

(12/D8)

SN74S04 RU7 U156

	1	9	3	13	11	5
	9	8	4	12	10	6
	3	13	11	5		
	13	12	10	6		
	11	11	12	8		
	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A1ØL	A11L	A12L	A13L	A14L A15L

(11/D8)

SN74S04 RU6 U155

	1	9	3	13	11	5
	9	8	4	12	10	6
	3	13	11	5		
	13	12	10	6		
	11	11	12	8		
	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A2ØL	A21L	A22L	A23L	A24L A25L

(10/D8)

SN74S04 RU5 U154

	1	9	3	13	11	5
	9	8	4	12	10	6
	3	13	11	5		
	13	12	10	6		
	11	11	12	8		
	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A3ØL	A31L	A32L	A33L	A34L A35L

(9/D8)

SN74S04 RU4 U153

(3/B1) AD0	1	9	3	13	11	5
(3/B1) AD1	9	8	4	12	10	6
(3/C1) AD2	3	13	11	5		
(3/C1) AD3	13	12	10	6		
(3/D1) AD4	11	11	12	8		
(3/D1) AD5	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A4ØL	A41L	A42L	A43L	A44L A45L

(8/D8)

SN74S04 RU3 U152

	1	9	3	13	11	5
	9	8	4	12	10	6
	3	13	11	5		
	13	12	10	6		
	11	11	12	8		
	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A5ØL	A51L	A52L	A53L	A54L A55L

(7/D8)

SN74S04 RU2 U151

	1	9	3	13	11	5
	9	8	4	12	10	6
	3	13	11	5		
	13	12	10	6		
	11	11	12	8		
	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A6ØL	A61L	A62L	A63L	A64L A65L

(6/D8)

SN74S04 RU1 U150

	1	9	3	13	11	5
	9	8	4	12	10	6
	3	13	11	5		
	13	12	10	6		
	11	11	12	8		
	5	3	13	14		
	14	2	1	7		
	7	13	12			
		8	9			
		4	11			
		12	12			
		10	10			
		6	8			
		2	3			
		39				
		A7ØL	A71L	A72L	A73L	A74L A75L

(5/D8)

SD700755 REV B

SIZE	CODE IDENT NO.	DWG NO.
D	52643	SD700755

SCALE: NONE SHEET 1 OF

DISTR NO.

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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/A1) A75L
A74L
A73L
(4/A1) A72L
(4/B1) A71L
(4/B1) A70L
(3/B3) RAS7L

-5V
+12V
+5VI
GND

U1 U2 U3 U4 U5 U6 U7 U8 U9

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) (6/C2) (2/A8) PAI PA0

(3/B3) WE0L
(3/B3) CAS7L

U10 U11 U12 U13 U14 U15 U16 U17 U18

(4/B6) D8I P80
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
PBI PB0

(3/B3) WE7ØL

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 5 OF 12

SD700755 B

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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/B1) A65L
A64L
A63L
A62L
A61L
(4/B1) A60L
(3/B3) RAS6L
(3/B3) WE60L
(3/B3) CAS6L

-5V
+12V
+5VI
GND

U19: (4/D6) D0I, D00
U20: (4/D6) D1I, D10
U21: (4/D6) D2I, D20
U22: (4/D6) D3I, D30
U23: (4/C6) D4I, D40
U24: (4/C6) D5I, D50
U25: (4/C6) D6I, D60
U26: (4/C6) D7I, D70
U27: (2/B6) PAI, (2/A8) PA0

U28: (4/B6) D8I, P80
U29: (4/B6) D9I, D90
U30: (4/B6) D10I, D100
U31: (4/B6) D11I, D110
U32: (4/A6) D12I, D120
U33: (4/A6) D13I, D130
U34: (4/A6) D14I, D140
U35: (4/A6) D15I, D150
U36: (2/B6) PBI, (2/A8) PB0

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: E	SHEET 2 OF 4
		DISTR NO.

SD700755

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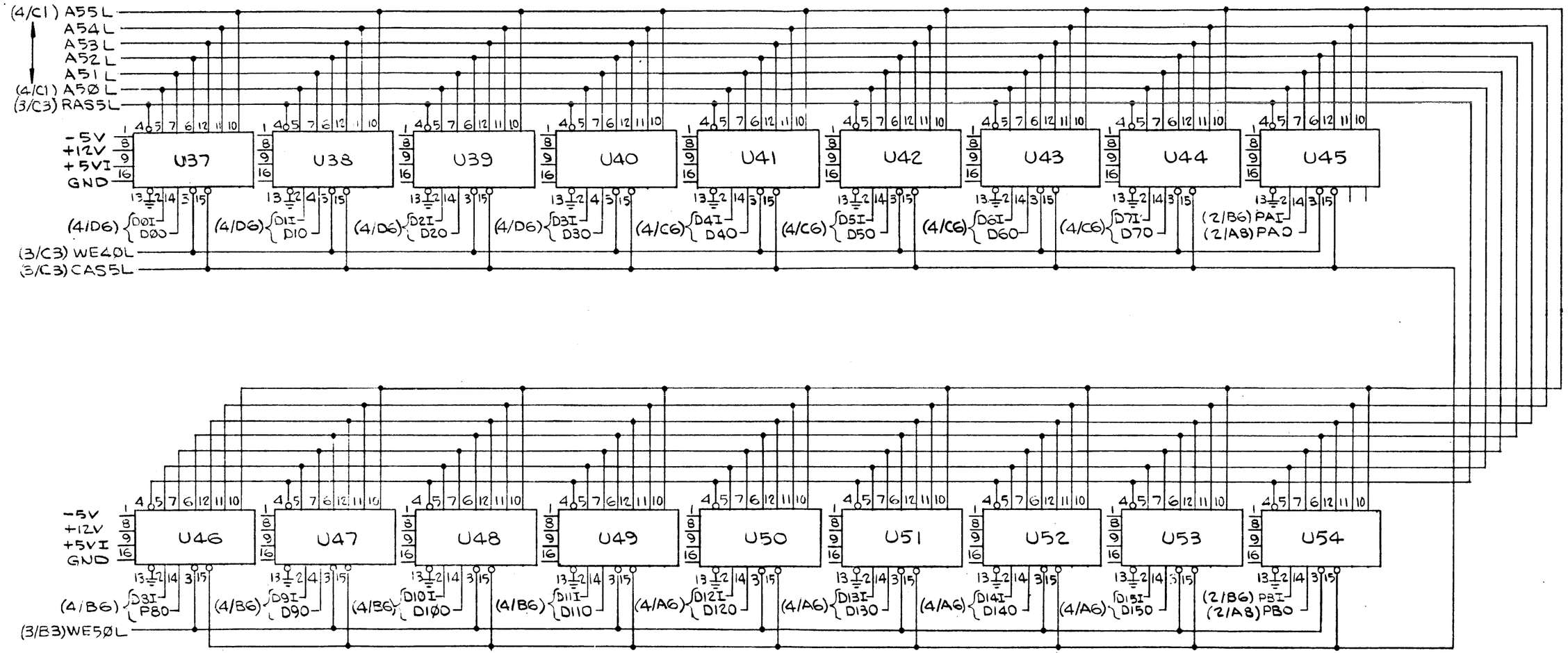
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 7 OF 14

DISTR NO.

SD700755 B

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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/D1) A45L
A44L
A43L
A42L
A41L
(4/D1) A40L
(3/C3) RAS4L

-5V
+12V
+5VI
GND

U55 U56 U57 U58 U59 U60 U61 U62 U63

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) PAI
(2/A8) PA0
(3/C3) WE4ØL
(3/C3) CAS4L

U64 U65 U66 U67 U68 U69 U70 U71 U72

(4/B6) D8I P80
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
(2/B6) PBI
(2/A8) PB0
(3/B3) WE5ØL

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 8 OF
		DISTR NO.

SD700755 B

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REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/A4) A35L
A34L
A33L
(4/A4) A32L
(4/B4) A31L
(4/B4) A30L
(3/C3) RAS3L

-5V
+12V
+5VI
GND

U73 U74 U75 U76 U77 U78 U79 U80 U81

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) PAI
(2/A8) PA0

(3/C3) WE2ØL
(3/C3) CAS3L

U82 U83 U84 U85 U86 U87 U88 U89 U90

(4/B6) D8I P80
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
(2/B6) PBI
(2/A8) PB0

(3/C3) WE3ØL

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755

SCALE: | REV: B | SHEET 9 OF 14 | DISTR NO.

SD700755

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/B4) A25L
A24L
A23L
A22L
A21L
(4/B4) A20L
(3/C3) RAS2L

-5V
+12V
+5VI
GND

U91 U92 U93 U94 U95 U96 U97 U98 U99

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) PAI
(2/A8) PA0

(3/C3) WE2ØL
(3/C3) CAS2L

-5V
+12V
+5VI
GND

U100 U101 U102 U103 U104 U105 U106 U107 U108

(4/B6) D8I P80
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
(2/B6) PBI
(2/A8) PB0

(3/C3) WE3ØL

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 10 OF 12
		DISTR NO.

SD700755 B

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/C4) A15L
A14L
A13L
A12L
A11L
(4/C4) A10L
(3/D3) RASIL

-5V
+12V
+5VI
GND

U109 U110 U111 U112 U113 U114 U115 U116 U117

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) PAI
(2/A8) PA0

(3/D3) WE0L
(3/D3) CASIL

-5V
+12V
+5VI
GND

U118 U119 U120 U121 U122 U123 U124 U125 U126

(4/B6) D6I PA0
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
(2/B6) PBI
(2/A8) PB0

(3/D3) WE01L

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 11 OF 14

DISTN NO.

SD700755 B

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

(4/D4) A05L
A04L
A03L
A02L
A01L
(4/D4) A00L
(3/D3) RASØL

-5V
+12V
+5VI
GND

U127 U128 U129 U130 U131 U132 U133 U134 U135

(4/D6) D0I D00
(4/D6) D1I D10
(4/D6) D2I D20
(4/D6) D3I D30
(4/C6) D4I D40
(4/C6) D5I D50
(4/C6) D6I D60
(4/C6) D7I D70
(2/B6) PAI
(2/A8) PA0

(3/D3) WEØØL
(3/D3) CAS1L

U136 U137 U138 U139 U140 U141 U142 U143 U144

(4/B6) D8I P80
(4/B6) D9I D90
(4/B6) D10I D100
(4/B6) D11I D110
(4/A6) D12I D120
(4/A6) D13I D130
(4/A6) D14I D140
(4/A6) D15I D150
(2/B6) PBI
(2/A8) PB0

(3/D3) WEØIL

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 2 OF 15
		DISTR NO.

SD700755 B

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

-5V: C1 .1, C2 .1, C3 .1, C4 .1, C4 .1, C5 .1, C6 .1, C7 .1, C8 .1, C9 .1, C10 .1, C31 .1, C32 .1, C33 .1, C34 .1, C35 .1, C36 .1, C37 .1, C38 .1

-5V: C39 .1, C40 .1, C61 .1, C62 .1, C63 .1, C64 .1, C65 .1, C66 .1, C67 .1, C68 .1, C69 .1, C70 .1, C91 .1, C92 .1, C93 .1, C94 .1, C95 .1, C96 .1, C97 .1

-5V: C98 .1, C99 .1, C100 15, C121 .1, C122 .1, C123 .1, C124 .1, C125 .1, C126 .1, C127 .1, C128 .1, C129 .1, C130 .1, C151 .1, C152 .1, C153 .1, C154 .1, C155 .1, C156 .1

-5V: C157 .1, C158 .1, C159 .1, C160 .1, C181 .1, C182 .1, C183 .1, C184 .1, C185 .1, C186 .1, C187 .1, C188 .1, C189 .1, C190 .1, C211 .1, C212 .1, C213 .1, C214 .1, C215 .1

-5V: C216 .1, C217 .1, C218 .1, C219 .1, C220 .1, C248 4.7 10V, C252 15

+5VI: C11 .01 100V, C12 .01 100V, C13 .01 100V, C14 .01 100V, C15 .01 100V, C16 .01 100V, C17 .01 100V, C18 .01 100V, C19 .01 100V, C20 .01 100V

+5VI: C41 .01 100V, C42 .01 100V, C43 .01 100V, C44 .01 100V, C45 .01 100V, C46 .01 100V, C47 .01 100V, C48 .01 100V, C49 .01 100V, C50 .01 100V, C71 .01 100V, C72 .01 100V, C73 .01 100V, C74 .01 100V, C75 .01 100V, C76 .01 100V, C77 .01 100V, C78 .01 100V, C79 .01 100V

+5VI: C80 .01 100V, C101 .01 100V, C102 .01 100V, C103 .01 100V, C104 .01 100V, C105 .01 100V, C106 .01 100V, C107 .01 100V, C108 .01 100V, C109 .01 100V, C110 .01 100V, C131 .01 100V, C132 .01 100V, C133 .01 100V, C134 .01 100V, C135 .01 100V, C136 .01 100V, C137 .01 100V, C138 .01 100V

+5VI: C139 .01 100V, C140 .01 100V, C161 .01 100V, C162 .01 100V, C163 .01 100V, C164 .01 100V, C165 .01 100V, C166 .01 100V, C167 .01 100V, C168 .01 100V, C169 .01 100V, C170 .01 100V, C191 .01 100V, C192 .01 100V, C193 .01 100V, C194 .01 100V, C195 .01 100V, C196 .01 100V, C197 .01 100V

+5VI: C198 .01 100V, C199 .01 100V, C200 .01 100V, C221 .01 100V, C222 .01 100V, C223 .01 100V, C224 .01 100V, C225 .01 100V, C226 .01 100V, C227 .01 100V, C228 .01 100V, C229 .01 100V, C230 .01 100V, C254 .01 +80-20% 16V, C259 .01 +80-20% 16V, C268 .01 +80-20% 16V, C281 .01 +80-20% 16V, C282 .01 +80-20% 16V

+5VB: C261 .01 +80-20% 16V, C262 .01 +80-20% 16V, C263 .01 +80-20% 16V, C264 .01 +80-20% 16V, C265 .01 +80-20% 16V, C266 .01 +80-20% 16V, C267 .01 +80-20% 16V, C271 .01 +80-20% 16V, C272 .01 +80-20% 16V, C273 .01 +80-20% 16V, C274 .01 +80-20% 16V, C276 .01 +80-20% 16V, C279 .01 +80-20% 16V

+12V: C21 .1, C22 .1, C23 .1, C24 .1, C25 .1, C26 .1, C27 .1, C28 .1, C29 .1, C30 .1, C51 .1, C52 .1, C53 .1, C54 .1, C55 .1, C56 .1, C57 .1, C58 .1, C59 .1

+12V: C60 .1, C81 .1, C82 .1, C83 .1, C84 .1, C85 .1, C86 .1, C87 .1, C88 .1, C89 .1, C90 .1, C111 .1, C112 .1, C113 .1, C114 .1, C115 .1, C116 .1, C117 .1, C118 .1

+12V: C119 .1, C120 .1, C141 .1, C142 .1, C143 .1, C144 .1, C145 .1, C146 .1, C147 .1, C148 .1, C149 .1, C150 .1, C171 .1, C172 .1, C173 .1, C174 .1, C175 .1, C176 .1, C177 .1

+12V: C178 .1, C179 .1, C180 .1, C201 .1, C202 .1, C203 .1, C204 .1, C205 .1, C206 .1, C207 .1, C208 .1, C209 .1, C210 .1, C231 .1, C232 .1, C233 .1, C234 .1, C235 .1

+12V: C236 .1, C237 .1, C238 .1, C239 .1, C240 .1, C241 15 20V, C242 15 20V, C243 15 20V, C244 15 20V, C245 15 20V, C246 15 20V, C247 15 20V, C248 15 20V, C250 15 20V

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700755
SCALE:	REV: B	SHEET 3 OF 1

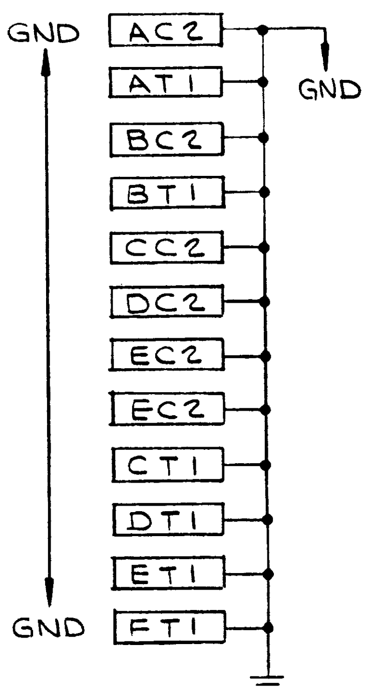
DISTR NO.

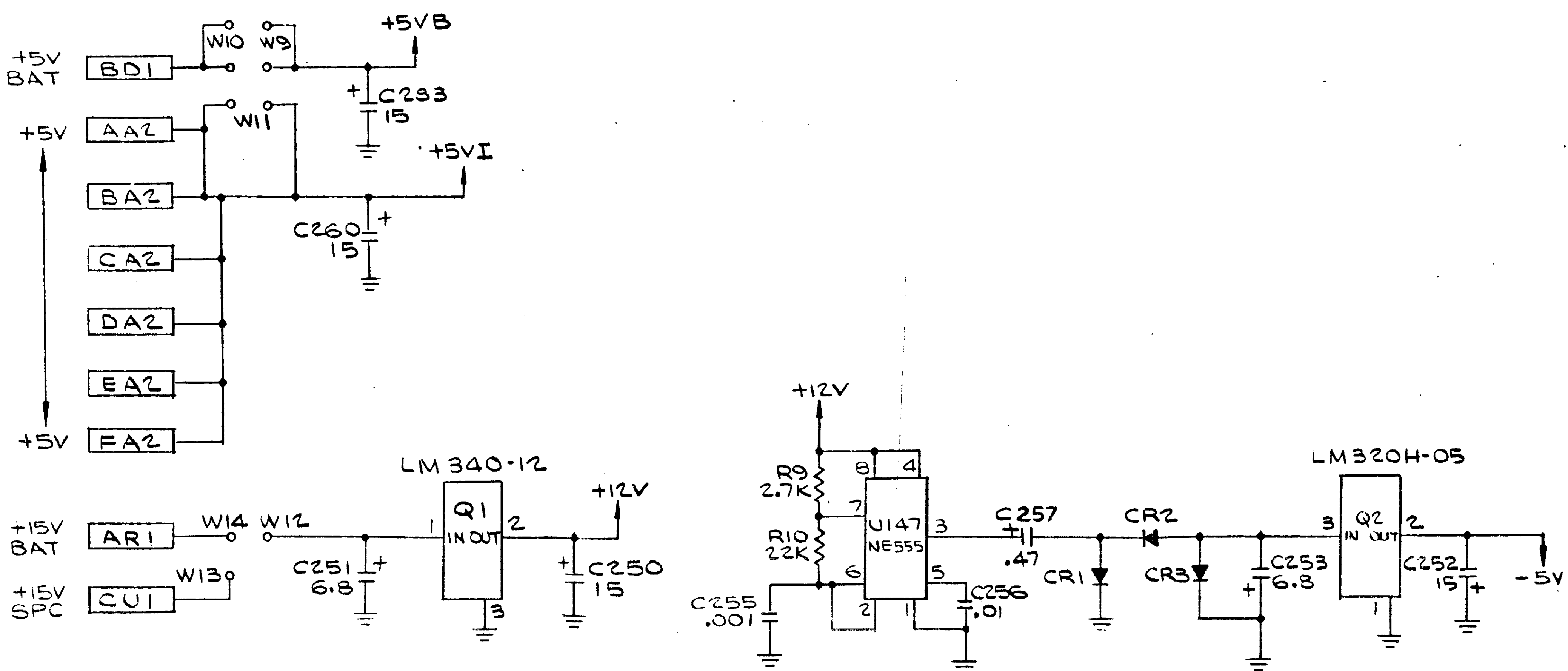
FORM NO 800013

SEE SHEET 1

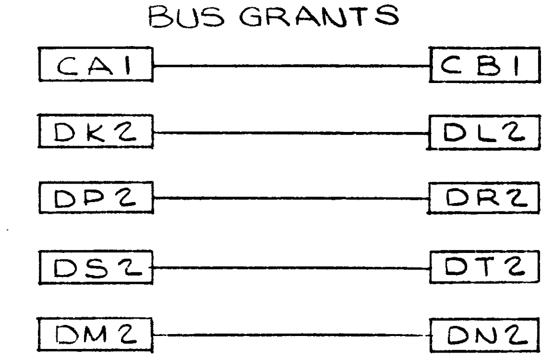
JUMPER WIRE CHART

VERSION	JUMPERS		VERSION	JUMPERS	
-100, -101 -108, -109	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(11) (12)	-200, -201	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(11)
-102 -110	W1 to W3 W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(11) (12)	-202	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH	(11)
-103 -111	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(11) (12) (13)	-203	W9 to W11, W12 to W13, WC to WD, WE to WF, WG to WH,	(11) (13)
-104 -112	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	(11) (12)	-204	W9 to W11, W12 to W13, WA to WF, WC to WD, WG to WH	(11)
-105 -113	W1 to W3, W4 to W6, W7 to W8, W9 to W11 W12 to W13, WA to WF, WC to WD, WG to WH,	(11) (12)	-205	W9 to W11, W12 to W13 WA to WF, WC to WD, WG to WH,	(11)
-106 -114	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13, WA to WF, WB to WH, WC to WD	(11) (12)	-206	W9 to W11, W12 to W13, WA to WF, WB to WH, WC to WD	(11)
-107 -115	W1 to W3, W4 to W6, W7 to W8, W9 to W11, W12 to W13 WA to WF, WA to WH, WB to WD	(11) (12)	-207	W9 to W11, W12 to W13, WA to WF, WA to WH, WB to WD	(11)





BUS GRANTS



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