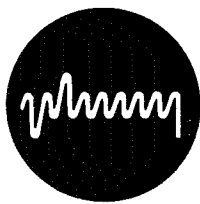


PM-DC/8
Disc Controller Manual



Plessey
Microsystems

FUNCTIONAL DESCRIPTION
PM DC/8 DISC DRIVE CONTROLLER

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SIZE

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52648

DWG NO.

MA 700655

REV

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SECTION I

FUNCTIONAL DESCRIPTION

PM DC/8 DISC CARTRIDGE
DRIVE CONTROLLER

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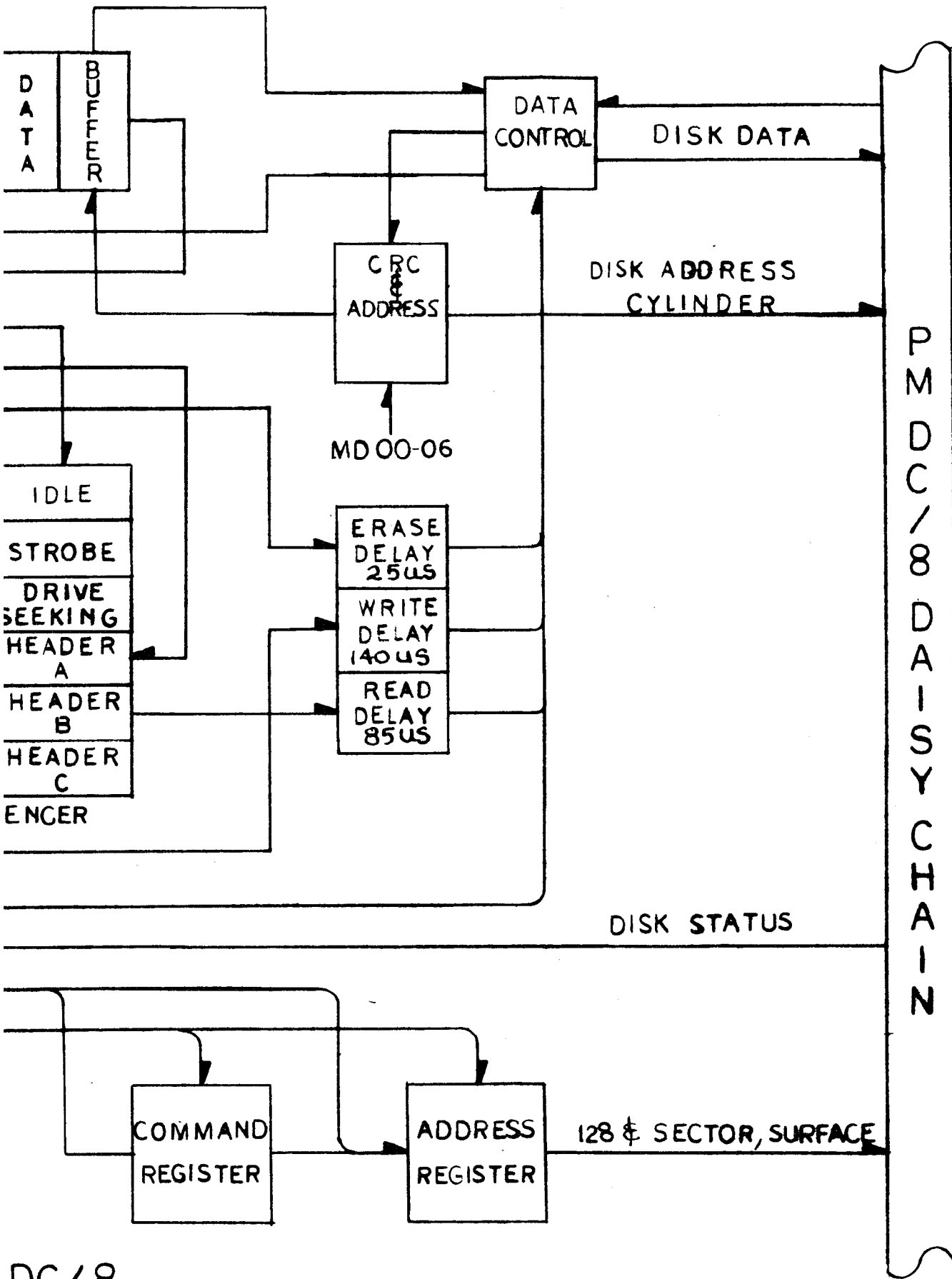
The interface between the DC/8 Disc Drive Control and the PDP-8* computer are via the single cycle data break feature.

Refer to the Digital Equipment* small computer handbook for a full description of the data break interface.

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DC/8

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1.0 CONTROL COMMANDS

1.1 Skip On Disc Done or Error (DSKP) 6741₈

When the conditions for transfer done are met or an error flag condition exists the instruction immediately following the DSKP will not be executed.

1.2 Clear All (DCLR) 6742₈

Bits 10 and 11 are decoded by the DC/8 logic to reset disc functions per the Table 1.2 and reset the accumulator to zero.

1.3 Load Disc Address and Execute Control Command (DLAG) 6743₈

This instruction is used in conjunction with the (DLDC) instruction to cause the disc drive to execute a seek and read or write from/to specified memory locations.

The contents of the accumulator are transferred to the disc address register to form the first 7 bits of the cylinder address and the complete 16 sector and one of 2 surfaces disc drive address. The accumulator is left cleared. The (DLAG) instruction will cause the disc drive controller to execute commands previously stored in the command register using target memory addresses specified by the current address register. The bit identification is specified in Table 1.3.

1.4 Load Current Memory Address (DLCA) 6744₈

Execution of this instruction causes the transfer of the contents of the accumulator to the current memory address register of the disc controller, leaving the accumulator cleared. The 12 bit current address register is combined with bits 6, 7 & 8 of the disc command register (DLDC) to form a 15 bit extended memory address per Figure 1.4.

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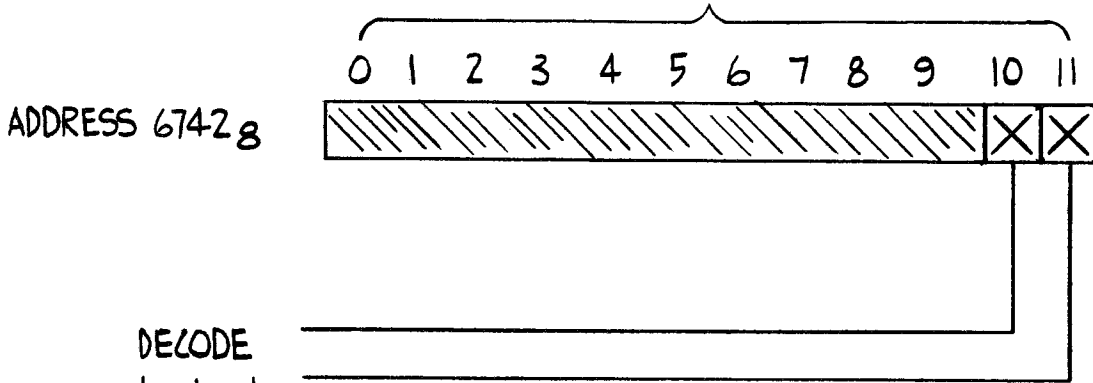
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Table 1.2

ACCUMULATOR



DECODE		BIT			
	10	11			
	0	0	DCLS	CLEAR THE ACCUMULATOR AND DISC STATUS REGISTER	
	0	1	DCLL	CLEAR THE ACCUMULATOR AND SETS ALL THE DC/B CONTROL FUNCTIONS TO THE ZERO STATE DOES NOT EFFECT THE DD/B SETS THE DC/B STATUS REGISTER TO ZERO'S NOTE: THIS COMMAND DOES NOT REGARD ANY DC/B CONTROL FUNCTIONS AND WILL TRUNCATE ANY CURRENT OPERATION	
	1	0	DCLD	RESTORE SELECTED DISC DRIVE TO THE HOME POSITION	
	1	1	DCLS	SAME AS DECODE 00	

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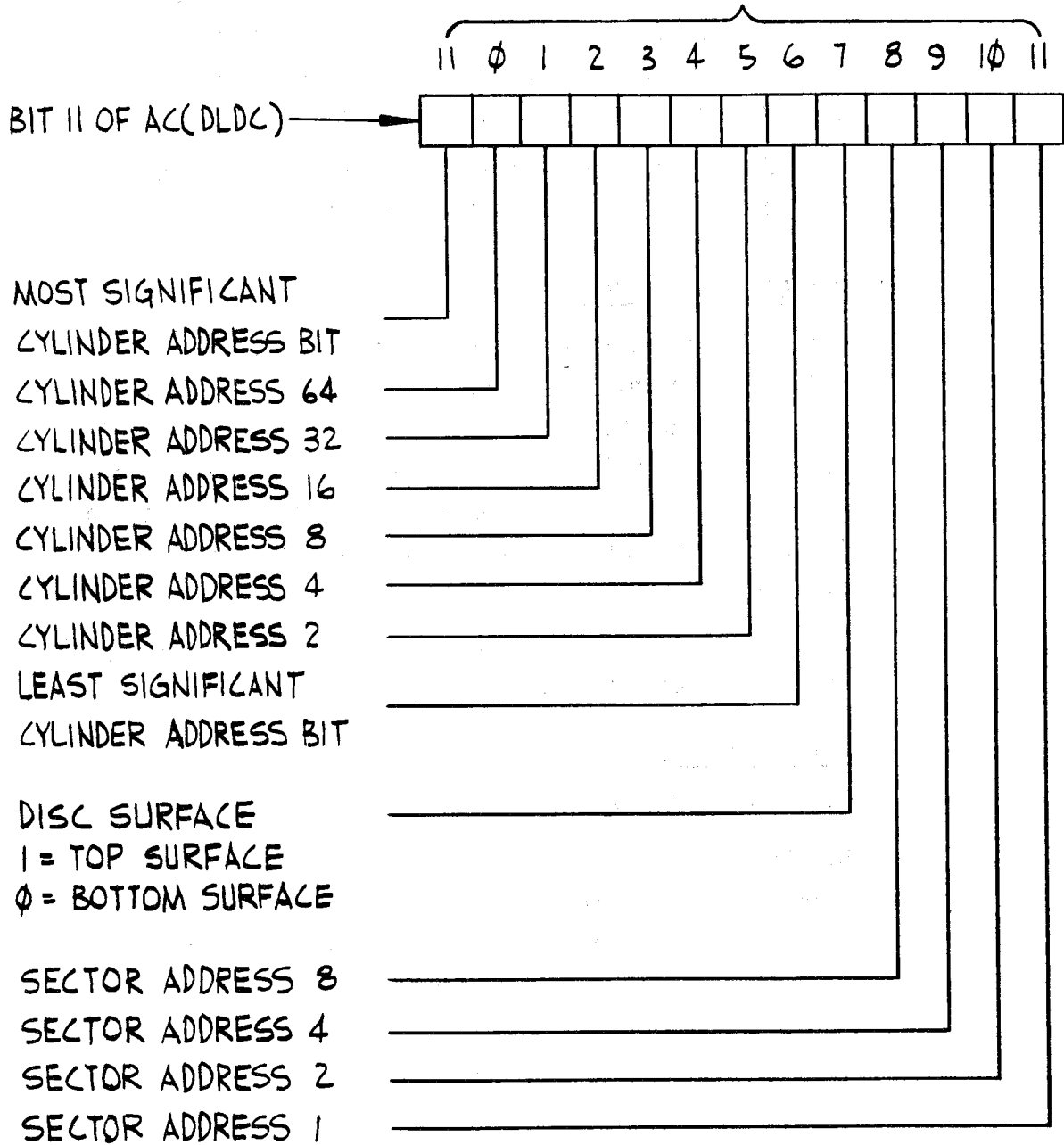
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Table 1.3

(DLAG) ADDRESS 6743₈

ACCUMULATOR



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1.4 Load Current Memory Address (DLCA) 6744₈ (continued)

This address is incremented once for each data transfer and asserted to the PDP8 Omnibus* during the data transfer between the DC/8 buffer storage and main memory. Address 11 thru zero are incremented module 12 fashion while EMA bits 0, 1 & 2 can be set by the program only.

1.5 Read disc status register (DRST) clear and load the AC with the contents of the disc status register.

Bit 00 Transfer Done

Bit 00 is set equal to a one in the status register for the following reasons. The controller has completed a data transfer; when the drive signals "seek complete" resulting from a seek only instruction; when the selected disc drive has completed a "restore" operation and bit 04 is set in the command register; when an error occurs during the execution of a disc operation.

If bit 03 is set in the command register bit 00 setting will cause an interrupt to occur.

Bit 01 Transfer Done

Bit 01 Ready To Seek Read or Write

Bit 01 is set, equal to a one, when the selected disc drive carriage head positioner is in place over the selected cylinder and the drive is ready to accept another seek command or a data transfer command.

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Table 1.5

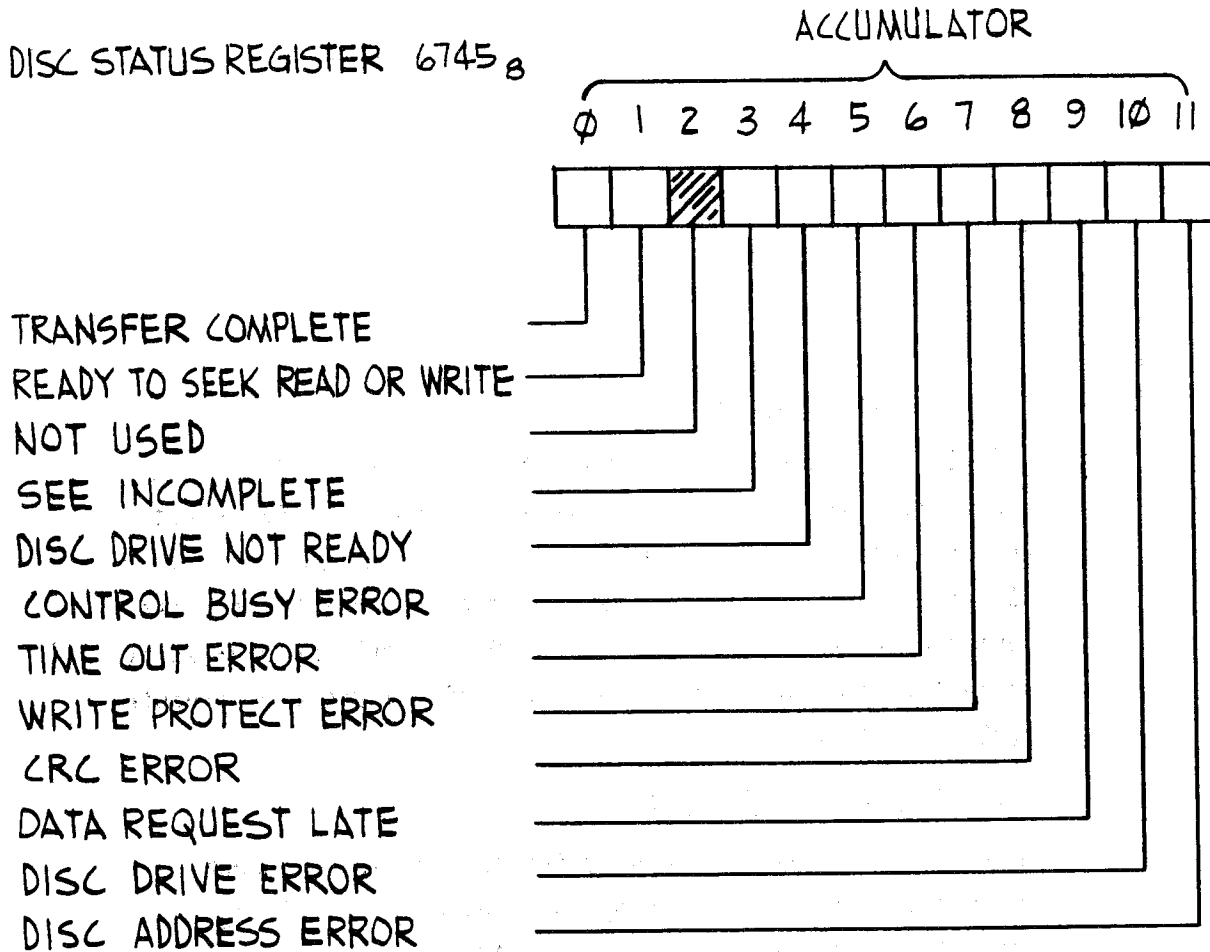
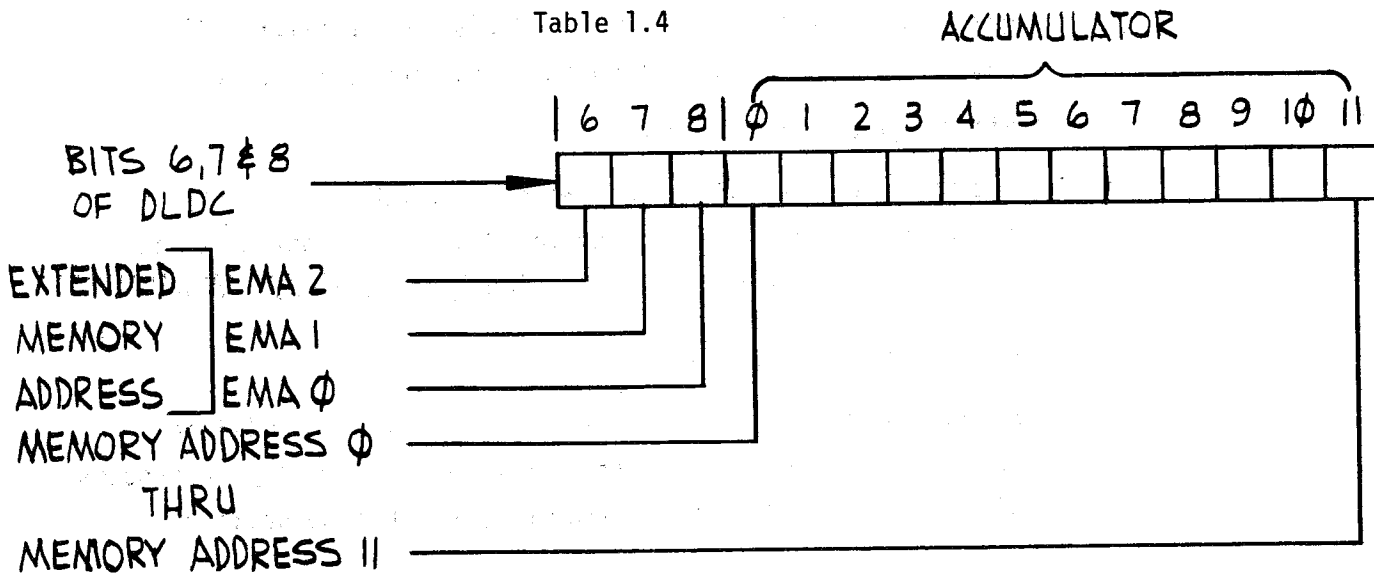


Table 1.4



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Bit 03 Seek Incomplete

Bit 03 is set, equal to a one, when a selected disc drive fails to complete a seek cylinder command. Bit 03 is set by the seek incomplete signal from the selected disc drive. If the (DLAG) instruction is executed with bit 03 set disc drive error bit 10 will set. Bit 03 can only be cleared by a restore command (Bit 10 set 1 and bit 11 reset 0) execute (DCLR) instruction.

Bit 04 Disc Drive Not Ready

When bit 04 is set the disc drive is not ready or unable to become ready due to an operational error requiring operator intervention. If the (DLAG) instruction is executed and bit 04 is set bit 10 disc drive error will set. The clearing of bit 04 requires operator intervention.

Bit 05 Control Busy Error

Bit 05 is set, equal to one, when the DLAG, DLCA or DLDC instructions are executed and the disc drive controller is busy having not completed a previously issued instruction.

Bit 00 is reset, equal to zero.

A command overlay causing the control busy error will not be allowed to be executed and the command currently in process will be completed with transfer complete bit 00 setting.



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Bit 06 Time Out Error

Bit 06 is a control watchdog timer enabled whenever control is set busy. Control timer when enabled is allowed to count 7 revolutions of the disc media and sets time out error at the start of the eighth revolution. Control timer is reset by the Idle flip flop going true before the start of the eighth revolution. (280 milliseconds). Time Out Error sets the done interrupt if enabled. Time out error indicates a hardware fault and can be cleared by (DCLR).

Bit 07 Write Protect Error

Bit 07 is set, equal to one, when an attempt has been made to write data to a write protected disc. The write protect is cleared by manually moving the cartridge protect or fixed protect switch of the selected disc drive downward. Protected discs are indicated by the presence of write protect switch illumination.

Bit 08 CRC Error

Bit 08 is set to a one when the postamble CRC character read from the disc media does not compare with the CRC character generated by the major register board as the data field was read. CRC error forces the control to the idle state setting transfer complete and truncating any operation in process. If the CRC error was caused by a soft data error then the sector may be reread with a new read command. If the data cannot be reread successfully then the data field has a hard data error and must be rewritten. Cyclic redundancy check polynomial = 3072 bits divided $N^{16} + N^{15} + N^2 + 1$.

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SCALE	REV	SHEET 10



Bit 09 Data Request Late

Bit 09 is set to a one on the event that the processor does not respond to a data break request within 22.5 micro seconds indicating data overrun to the controllers 4 word data buffer. Data Request Late forces the control to the idle state setting transfer complete.

A new transfer sequence must be initiated in order to continue the transfer of data. The sector in the process of being read when Data Request Late occurred must be reread.

Computer service latency to a data break request cannot exceed 6.5 micro seconds when all the ranks of the input buffer are full, or 13 microseconds if 2 ranks are full.

Data Request Late timings are true whether the operation is a read or a write.

Bit 10 Drive Status Error

Bit 10 is set to a one when any of the following conditions exist and the (DLAG) instruction is executed.

1. Disc prime power off.
2. Address switches #1 & #2 are incorrectly set to the disc drive.
3. Disc cartridge not mounted or cartridge door not closed.
4. Disc not up to speed (Drive will not come ready even though broom cycle is completed)
5. Erase or write current is present without write gate.
6. The carriage servo mechanism has been detected inoperative.
7. Controller attempts to address a nonexistent cylinder (Sets transfer complete).
8. Seek incomplete is set.

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	SCALE	REV	SHEET 11



Bit 11 Cylinder Address Error

Bit 11 is set to a one if a header label is read that does not compare with the header information stored on the Major Registers Board. This event could have been caused by either a servo positioner error or a read error. Transfer complete is set.

The cylinder address may be read from the CRC register using the maintenance instruction. The disc drive should be restored and a new seek issued.

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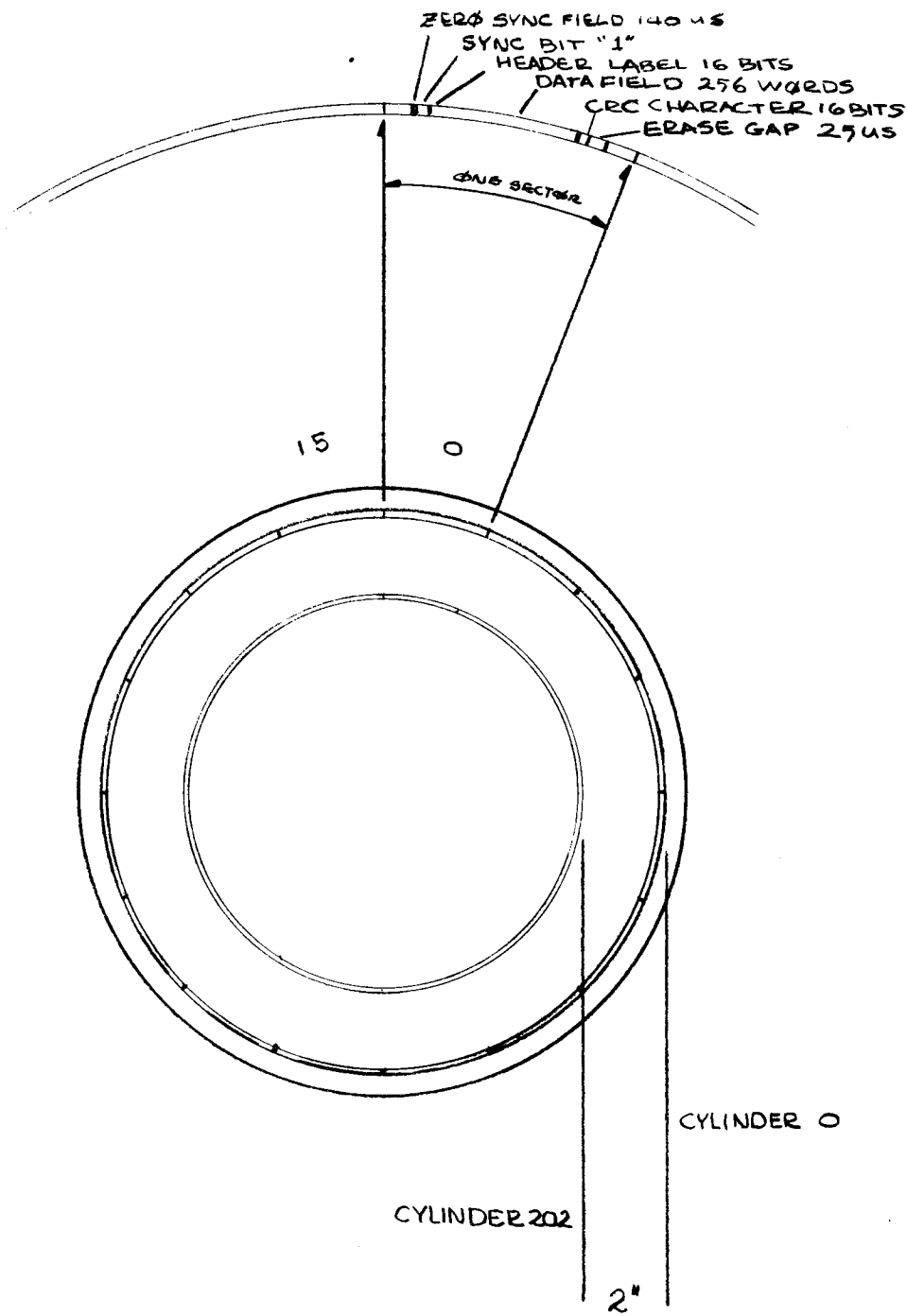
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DATA FORMAT PMDC/8 - PMDD/8

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SCALE	REV	SHEET 13



1.6 Load Disc Command Register (DLDC) 6746₈

This instruction is used in conjunction with the (DLAG) instruction to cause the disc drive to execute various control commands.

The contents of the accumulator are transferred to the disc controller command register leaving the accumulator cleared.

Actual initiations of command functions take place when the (DLAG) instruction is executed. The functional characteristic of each bit loaded to the command register is presented in the following paragraphs.

1.6.1 The settings of bits 0, 1 & 2 will determine the command function to be executed when the (DLDC) instruction is issued. These bit settings are coded 0 thru 5 in binary coded octal format to determine the particular function. See Table 1.6.1.

(00₈) Read Data: This is the command function usually used to transfer data from the disc media to the CPU. When the read command is acted upon the disc drive will seek to the physical cylinder, surface & sector address specified by the (DLDC-DLAG) instructions and compare the header information previously written with the contents of the controller registers. When a match is achieved the transfer of one block of serial data commences. 256 words for a full block 128 words if the half block bit is set. Data is deserialized and loaded to Rank 1 of the four word controller data buffer.

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1.6.1 (Continued)

Data is subsequently shifted in twelve bit parallel form ~~from the all empty ranks to Rank 4,~~ and as data break requests are ~~monitored~~ by the CPU the data is asserted on the Omnibus* data lines. A data break request will be issued whenever a Rank of the four word data buffer is full and a data break request will be pending for all full Ranks. The CPU's ability to keep up with the data transfers from the disc is monitored by the Data Request Late flag. At the conclusion of the block transfer the CRC word is read by the control logic and compared with the CRC computed during the read operation. Transfer Done status is set and an interrupt can be activated at the conclusion of each block or half block read.

(01g) Read All: This command is used to verify header labels written when a disc cartridge has been newly formatted. The Read All command responds to data in the same manner as the Read Data command with the exception that headers are not verified before a transfer of data can commence. This feature allows an addressing word corresponding to the header address information to be read from the data field without regard to the information that actually exists in the header field.

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1.6.1 (Continued)

(02g) Write Protect: The write protect command can be used to set the write protect line on disc drives that are equipped with the remote write protect feature. When so equipped, the write protect can only be over-ridden by physically pushing off the write protect switch on the write protected disc drive. See paragraph 1.5, Write Protect Error.

If an attempt is made to write to a write protected disc drive, Write Protect Error(bit 07 of the disc status register) will be set and the write will be inhibited.

(03g) Seek Only: The seek only command is used to initiate seeks to more than one disc drive at a time; this reduces the access latency when information might be resident on more than one disc drive. When the seek only command is issued, the selected disc drive will perform the seek specified by the (DLDC, DLAG) instructions, however the address information will not be compared with the block's header information.

The Transfer Done flag will be set when the Seek Only command is executed. Bit 4 can be set to a one in the control command register to specify the Transfer Done flag to be set again when the "seek complete" actually takes place.

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1.6.1 (Continued)

Note: Care must be taken to avoid overlapping seeks to disc drives with unit numbers set to equal the same physical disc drive, i.e. units number 1 and number 2 usually are set to equal disc drive number 0 removable disc and fixed disc respectively. Both discs share the same carriage head positioner mechanism.

(04₈) Write Data: This is the command function usually used to transfer data from the CPU to the disc media. When the write command is acted upon, the disc drive will seek to the physical cylinder, surface, sector address previously specified by the (DLDC, DLAG) instructions and compare the header information previously written with the contents of the controller registers. When a match is achieved, the transfer of one block of serial data commences (256 words for a full block 128 words if the halfblock bit is set). Data is loaded from the Omnibus* to Rank 1 of the four word controller data buffer in 12 bit parallel format.

Data is subsequently shifted in parallel format thru all empty Ranks to Rank 4 where serialization takes place. From Rank 4, data is shifted out serially thru double frequency, crystal controlled clocking logic to the disc drive.

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1.6.1 (Continued)

Data is captured from the CPU as single cycle data break requests are honored. A Data Break Request will be issued whenever a Rank of the four word data buffer is empty and a Data Break Request will be pending for all empty ranks.

The CPU's capability to maintain data flow is monitored by the Data Request Late flag. At the conclusion of the data transfer a cyclic redundancy check character of the full data block is recorded.

(05_g) Write All: This command is used to format a new disc cartridge prior to actual usage in a computing system. The Write All responds to data in the same manner as the write data command with the exception that headers are not verified before a transfer of data can commence. This feature allows an addressing word corresponding to the header address information to be written to the sector data field without regard to the information that actually exists in the header field.

To format a new disc cartridge, all that is necessary is for the program to address each and every sector of the disc, writing one word each time. The controller will then take responsibility to write the header information that was physically used to access the disc and the program can write its own header verification word.

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1.6.2 Bit 03 Interrupt Enable

The disc drive controller interrupt system is armed by the setting of bit 03 equal to 1 in the DC/8 command register. With the controller interrupt armed, a program interrupt is initiated by the setting of Transfer Done or Error Flag.

1.6.3 Bit 04 Seek Complete Transfer Done

The setting of bit 04 to a 1 in the DC/8 command register will cause Transfer Done flag to occur on the completion of a seek by the selected disc drive. See seek only 1.6.1.

1.6.4 Bit 05 Read/Write Half Block

The setting of bit 05 (half block bit) equal to a 1 in the DC/8 command register will cause the disc system to transfer a truncated (128 word) block of data. During a write, with the half block bit set, 128 words of data are transferred from main memory to the disc drive followed by 128 words of zeroes generated by the controller logic. A CRC character is written after the 128 words of zero's and Transfer Done flag is asserted. During a read with the half block bit set 128 words of data are transferred to main memory, then a pause in CPU controller activity takes place while a CRC character is calculated based on the entire 256 word record. The calculated CRC is compared to the CRC written on the disc and Transfer Done flag is asserted.

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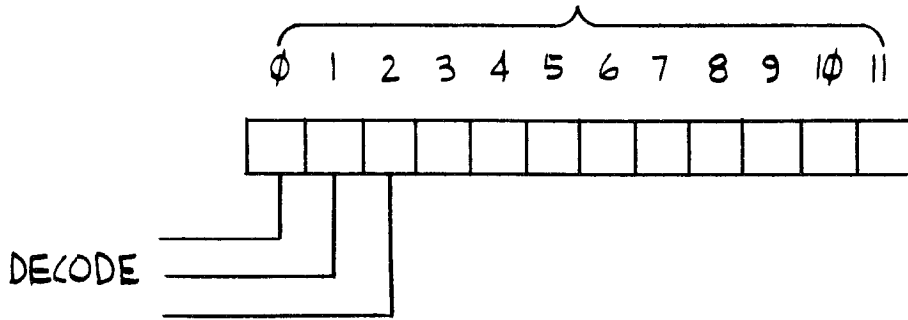
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SEEK/READ/WRITE FUNCTION BITS

ACCUMULATOR



BIT	0	1	2	FUNCTION
0 ₈	0	0	0	READ DATA (READ CHECK)
1 ₈	0	0	1	READ ALL (IGNORE HEADER) CHECK
2 ₈	0	1	0	WRITE PROTECT SELECTED DRIVE
3 ₈	0	1	1	SEEK ONLY
4 ₈	1	0	0	WRITE DATA (WRITE CHECK)
5 ₈	1	0	1	WRITE ALL (IGNORE HEADER) CHECK

Table 1.6.1

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1.6.5 Bits 6, 7 & 8 Select Extended Memory

The setting of bits 6, 7 & 8 in the command register determine the selection of extended memory address fields and are used as the most significant bits of a source, destination address for direct memory transfers by the disc controller. Bits 0 thru 11 of the memory address are provided by the Current Address Register. Bits 6, 7 & 8 become EMA bits, 2, 1 & 0 respectively and are asserted to the omnibus* per table 1.6.5 for each direct memory transfer.

The EMA bits are not effected by overflow from the Current Address Register and must be reset to select a new memory address field. If Current Address Register overflow occurs without the resetting of the EMA bits, the data transfer in process will exhaust its record space by wrapping around the selected memory address field.

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Table 1.6.5

COMMAND REGISTER BIT EXTENDED MEMORY BIT	Φ6 EMA2	Φ7 EMA1	Φ8 EMA Φ	SELECTED MEMORY FIELD
	Φ	Φ	Φ	FIELD Φ
	Φ	Φ	1	FIELD 1
	Φ	1	Φ	FIELD 2
	Φ	1	1	FIELD 3
	1	Φ	Φ	FIELD 4
	1	Φ	1	FIELD 5
	1	1	Φ	FIELD 6
	1	1	1	FIELD 7

Table 1.6.6

BIT 9	BIT 10	LOGICAL UNIT
Φ	Φ	# Φ
Φ	1	# 1
1	Φ	# 2
1	1	# 3

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SIZE

A

CODE IDENT NO.

DWG NO.

MA 700655

SCALE

REV

SHEET

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1.6.6 Bits 9 & 10 UNIT SELECT

Bits 9 and 10 of the Command Register are decoded to select one of four logical disc units per Table 1.6.6.

Unit select functionally establishes the communications path between the PM-DC/8 and the PM-DD/8 disc units available and must be used when data or control information is passed. Interpretation of the unit select lines can be established by the position of the two thumbwheel switches at the rear of the disc drives, rather than re-establishing the disc drive logical position in the daisy chain. Care must be taken in the setting of the thumbwheel switches to assure that only one disc drive unit occupies a logical unit position in the chain.

1.6.7 Bit 11 Extended Cylinder Address

Bit 11 of the command register is the most significant bit of the disc cylinder address register (bit significance 128). Bit 11 is stored with the disc address to form an eight bit cylinder address selection word. See Table 1.3. The usable cylinder range is 203_{10} or 312_8 . Addresses above 203_{10} will cause an illegal address error.

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	A		MA 700655
	SCALE	REV	SHEET 23



SECTION II
MAINTENANCE FEATURES

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1.7 Disc Maintenance (DMAN) 6747₈

The disc maintenance instruction is used to condition the DC/8 major registers such that they are linked to the fourth rank of the data buffer to be read to the accumulator or memory. The disc maintenance instruction can also be used when loading data to the DC/8 from the accumulator or memory. The (DCLC) instruction paragraph 1.2 must be used to terminate a function when changing modes from read to write or write to read. The maintenance functions are shown in Table 1.7 followed by a detailed description.

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Table 1.7

BIT	FUNCTION
00	ENABLE MAINTENANCE MODE DISABLE (DLAG)
01	ENABLE SHIFT TO DATA BUFFER RANK 4 (DB4)
02	SHIFT CRC TO DB4
03	SHIFT COMMAND REGISTER TO DB4
04	SHIFT SURFACE & SECTOR TO DB4
05	SHIFT ACI0 TO DB1
06	INITIATE SINGLE CYCLE DATA BREAK
07	TRANSFER DB4 TO THE ACCUMULATOR
08	NOT USED
09	NOT USED
10	DATA BIT FOR MAINTENANCE DATA SHIFT
11	NOT USED

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SCALE	REV	SHEET 26



1.7.1 Bit 00 Maintenance Mode

The maintenance mode is enabled by executing the (DMAN) instruction with accumulator bit 00 set to equal 1. The maintenance mode disables the (DLAG) instruction. The maintenance control bit is cleared by the (DCLC) clear control command.

Bit 01 Shift Enable

The execution of (DMAN) with accumulator bit 01 set equal to 1, sets Rank 4 of the 4 word data buffer to shift mode to receive maintenance data.

Bit 02 Shift CRC

The execution of (DMAN) with accumulator bit 02 set equal to 1 will cause bit 10 of the accumulator to load into bit position 01 of the CRC Register and shift the CRC Register one place into Rank 4 of the data buffer. AC10 → CRC01 CRC 16 → DB4 (PM00)

Twelve executions of (DMAN) with bit 02 set would fill DB4 with 12 bits of the CRC. Execution of (DMAN) with bit 07 set will transfer this value to the accumulator. To input the remaining 4 CRC bits. Shift CRC four more times and load this value from DB4 to the accumulator.

CRC Bits 4-11 contain the disc cylinder address when the CRC register is used as the Disc Address register Bits 1, 2 & 3 and 12, 13, 14, 15 & 16 would be zeros.

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A		MA 700655
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1.7.1 (Continued)

Bit 03 Shift Command Register to DB4

The execution of (DMAN) with the accumulator bit 03 set equal to a 1 shifts the command register one place left to DB4 and Bit 11 of the command register to Bit 00 of DB4. Twelve shifts will load the entire command register to DB4.

Bit 04 Shift Surface And Sector to DB4

The execution of (DMAN) with accumulator bit 04 set equal to 1 will shift the sector surface address register left one place to DB4. Five shifts will load the entire sector surface register to DB4.

Bit 05 Shift AC 10 to DB1

Execution of the (DMAN) instruction with accumulator bit 05 set equal to a 1 will shift accumulator bit 10 left one place to the least significant bit position of Rank 1 of the 4 word data buffer. The bit counter and word counter are incremented in the same manner as they would be by incoming disc data. (DCLC) must be issued to clear the action and results of (DMAN) with 05 set.

Bit 06 Initiate Single Cycle Data Break

The execution of the (DMAN) instruction with accumulator bit 06 set equal to a 1 will allow a single cycle data break to occur. Control information specified by the command register will be executed. Data transfer will occur using the memory address specified by the current address register and the extended memory address register. DB1 thru DB4 will transfer and act on data in their normal manner with the Data Request Late flag being active. Thus a read must occur for every write to avoid Data Request Late.

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SIZE A	CODE IDENT NO.	DWG NO. MA 700655
SCALE	REV	SHEET 28



Accumulator Bit 06 is cleared automatically when Data Break Request is serviced. (DCLC) is used to reset the command register and make DB4 appear empty.

Bit 07 Transfer DB4 to the accumulator

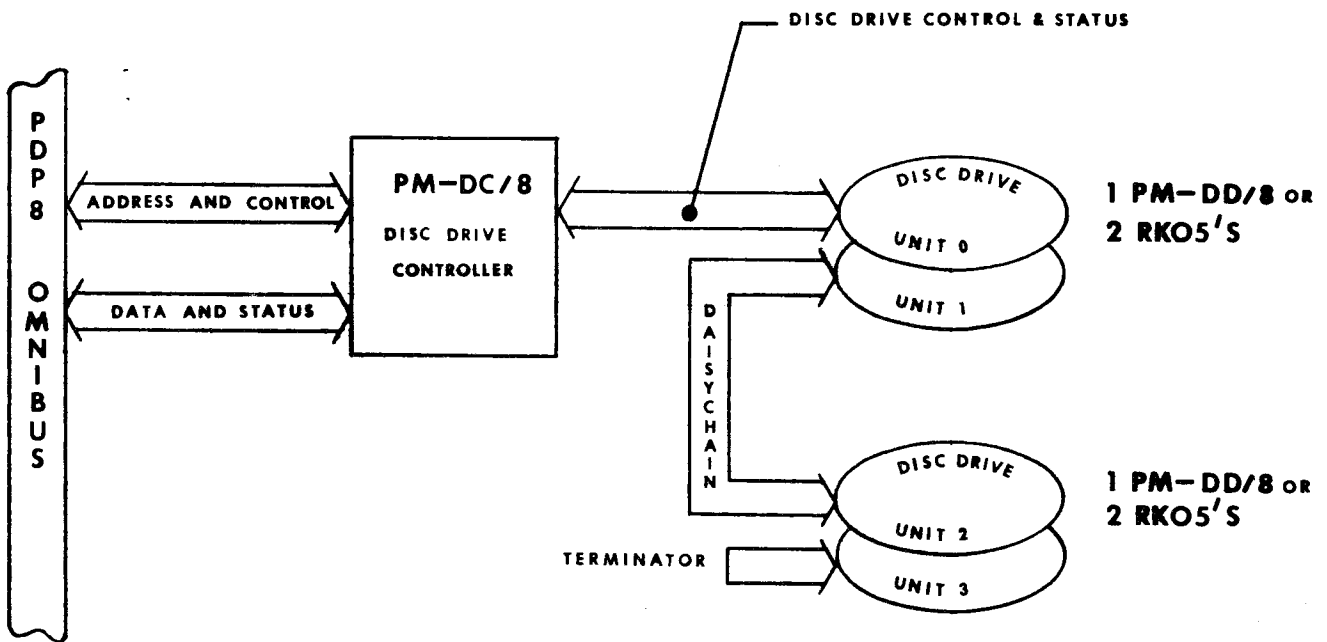
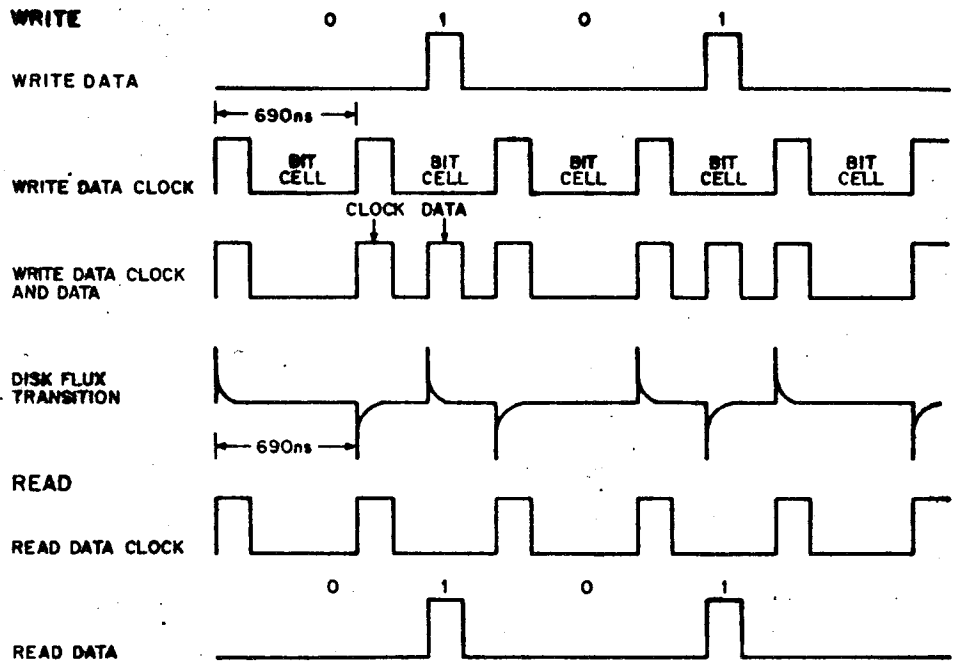
The execution of (DMAN) with accumulator bit 07 set equal to a 1 will cause one word of information to be loaded from DB4 to the accumulator.

Bit 10 Data Bit

Bit 10 is used as a data bit in conjunction with various maintenance functions.

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SIZE	CODE IDENT NO.	DWG NO.
A		MA 700655
SCALE	REV	SHEET 29



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SIZE A	CODE IDENT NO.	DWG NO. MA 700655
SCALE	REV	SHEET 30



SECTION III

INSTALLATION PROCEDURE & PM-DD/8 SPECIFICATIONS

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CODE IDENT NO.

DWG NO.

MA 700655

SCALE

REV

SHEET

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REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
-	REL FOR PROD PER ERO 500712	2-18-76	JES

APPLICATION	
NEXT ASSY	USED ON

PRODUCTION RELEASE

REV STATUS OF SHEETS	REV LTR																				
	SHEET																				
	REV LTR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28

COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM

REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R

ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1

STANDARD HOLE TOLERANCE PER AND 10387


TOLERANCES ON: XX ± .03, XXX ± .010, ANGLES ± 0°30'

INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.3

DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH

UNLESS OTHERWISE SPECIFIED

CONTRACT NO.	
DRAWN T. Githens	2/17/76
CHECK J. Boll	2/18/76
DESIGN	
PROJ. ENGR D. Nakaya	2/18/76
OTHER APPROVALS	

 **Plessey Memories Incorporated**
Santa Ana, California

DWG TITLE
PLESSEY DISC DRIVE SYSTEM (PM-DS/8B)
INSTALLATION PROCEDURE

SIZE A	CODE IDENT NO. 52648	DWG NO. IP 700715
SCALE:	SHEET 1 OF 11	

FORM 000020

DISTR NO.



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SIZE

A

CODE IDENT NO.

52648

DWG NO.

IP 700715

SCALE

REV -

SHEET

2

PLESSEY DISC DRIVE INSTALLATION PROCEDURE

1.0 REQUIRED ITEMS

Disc Drive Manual	MA700540
Allen Wrench	5/64in.
Phillips Screwdriver	Xcelite X-108 #1
Common Screwdriver	Xcelite R-3166 3/16 x 6
4" Adjustable Wrench	Crescent etc.
Cable Extractor	3M

2.0 UNPACKING AND INSPECTION

- 2.1 Inspect shipping container for evidence of damage incurred during shipment. Reporting obvious damage to the carrier company.
- 2.2 Open the top side of the shipping container.
- 2.3 Remove the inner container and open the top side of the inner container.
- 2.4 Remove the top and side styrofoam liners.

2.5 Grip the unit along both sides of the casting while lifting the unit out of the ~~container~~.

CAUTION: Do not support the unit via the handle on the front panel.

- 2.6 Remove the protective plastic bag.
- 2.7 The shipping container and internal packing material may be retained for future repacking of the unit. A replacement container may be ordered Plessey No. 300166.

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SIZE	CODE IDENT NO.	DWG NO.
A	52648	IP 700715
SCALE	REV -	SHEET 3



3.0 DISC TOP COVER REMOVAL

- 3.1 Using a 5/64 allen wrench remove the six screws on the top surface of the cover.
- 3.2 Release the front door locking mechanism which may be depressed toward the rear of the unit by means of an access window located on the right side panel of the top cover toward the front of the unit. While holding the locking mechanism depressed open the front door. See Figure 1 for locations.

4.0 CARRIAGE SHIPPING RESTRAINT REMOVAL

- 4.1 Release the cabinet lock mechanisms located on each side of the drive by depressing them in an upward direction (See Figure 1 for location). This will release the slides. While holding the cabinet latch mechanism, push the disc slides toward the rear of the machine in order to gain access to the positioner assembly.

- 4.2 Remove the restraint retaining screw then reinstall it, as shown, in the stowed position.

NOTE: The restraint retaining screw secures the carriage rear stop and MUST be re-installed. See Figure 2 for location.

- 4.3 Plug in P-16 on power supply.

5.0 INITIAL CHECKOUT

- 5.1 Slightly elevate the front of the drive to give clearance for the motor pulley for temporary desk top checkout.
- 5.2 Apply AC power to the drive. The power cord receptacle is located in the drive back panel.
- 5.3 Turn the power switch on. The load lamp should illuminate.
- 5.4 Insert a "scratch" cartridge into the drive.

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SIZE A	CODE IDENT NO. 52648	DWG NO. IP 700715
SCALE	REV -	SHEET 4



5.0 INITIAL CHECKOUT: (Continued)

- 5.5 Turn the run/load switch to RUN. After approximately 20 seconds the Ready lamp should illuminate.
- 5.6 Connect the Drive Bus cable to J-22 on the I/O connector board.
- 5.7 Run diagnostics or a DEC program to verify that the disc is operating properly.

6.0 RACK MOUNTING

- 6.1 Turn the Run/Load switch to the load position. After approximately 20 seconds the load lamp should illuminate.
- 6.2 Remove the cartridge and turn the power switch off.
- 6.3 Remove the A.C. power cord from the drive.
- 6.4 Remove the back panel as follows:
 - a. Remove the 2 screws securing the A.C. receptacle to the back panel.
 - b. Using the 3M cable extractor remove the cable from J-21 on the I/O connector.
 - c. Remove the 4 screws securing the back panel to the drive slides.
- 6.5 Remove the slides as follows:
 - a. Using the 3M cable extractor remove the cable from the DIB board J20.
 - b. Remove the 4 screws securing the slides to the drive. See Figure 1.
- 6.6 Mount the slides in the rack using the mounting hardware provided. The slide brackets may be adjusted to fit the rack by loosening the bracket fastening screws at the front and rear of the slide. The rear of the slide attaches to the rack by means of the bracket adjustment screw. (See Figure 1).

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SIZE A	CODE IDENT NO. 52648	DWG NO. IP 700715
SCALE	REV -	SHEET 5



- 6.7 After both slides are mounted, fully extend them and set the drive on the extended slides.
- 6.8 Fasten the rails to the drive.
- 6.9 Mount the drive back panel and connect the ribbon cable to the DIB and I/O boards.
- 6.10 Reconnect the A.C. receptacle.
- 6.11 Reinstall the drive top cover.

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SCALE	REV -	SHEET 6



7.0 CONTROLLER INSTALLATION

- 7.1 Ensure PDP-8 power is turned off.
- 7.2 Ensure correct jumpers are installed to select the device code assigned to this disc controller. The data and buffer board (700645) is normally shipped with the 674X device code 675X through 677X may be used (See Table 1).
- 7.3 Install jumpers to select priority assigned to disc controller. priority jumpers on major board *700647). See Table 2.
- 7.4 Connect disc bus cable. (700696) onto control board (700643)

NOTE: Cable labeled "P1" and "P2".
- 7.5 Insert three (3) card PDP 8 disc controller (PM-DC/8) into the omnibus - See Figure 3.

NOTE: Major board (700647) if inserted incorrectly,, will apply +15V, -15V, -5, and +5V to logic input/output gates. Insert all boards with connectors "A", "B", "C", and "D" down and into the OMNIBUS.
- 7.6 Install PM-DS/8 top connector (700713-100) onto the three disc control boards.

8.0 ACCEPTANCE TEST

The following diagnostics must be run in the order shown to satisfy minimum test requirement. Refer to instruction in diagnostic document to run test.

- 8.1 RK8-E discless control diagnostic - 2 passes
- 8.2 RK8-E drive control diagnostic - 1 pass
- 8.3 RK8-E formatter - 1 pass
- 8.4 RK8-E data reliability test - optional

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52648

DWG NO.

IP 700715

SCALE

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SHEET

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TABLE I
DEVICE SELECT JUMPER INSTALLATION

OCTAL CODE	INSTALL FOLLOWING JUMPER ON P/N 700645 BOARD
674X	W2, W3
675X	W2
676X	W3
677X	NONE

TABLE II
PRIORITY SELECTION

PRIORITY	INSTALL JUMPER ON P/N 700647 BOARD
PRIORITY 0 (HIGHEST)	W1 & W4
PRIORITY 1	W2, W3, & W5

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DWG NO.

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SCALE

REV -

SHEET

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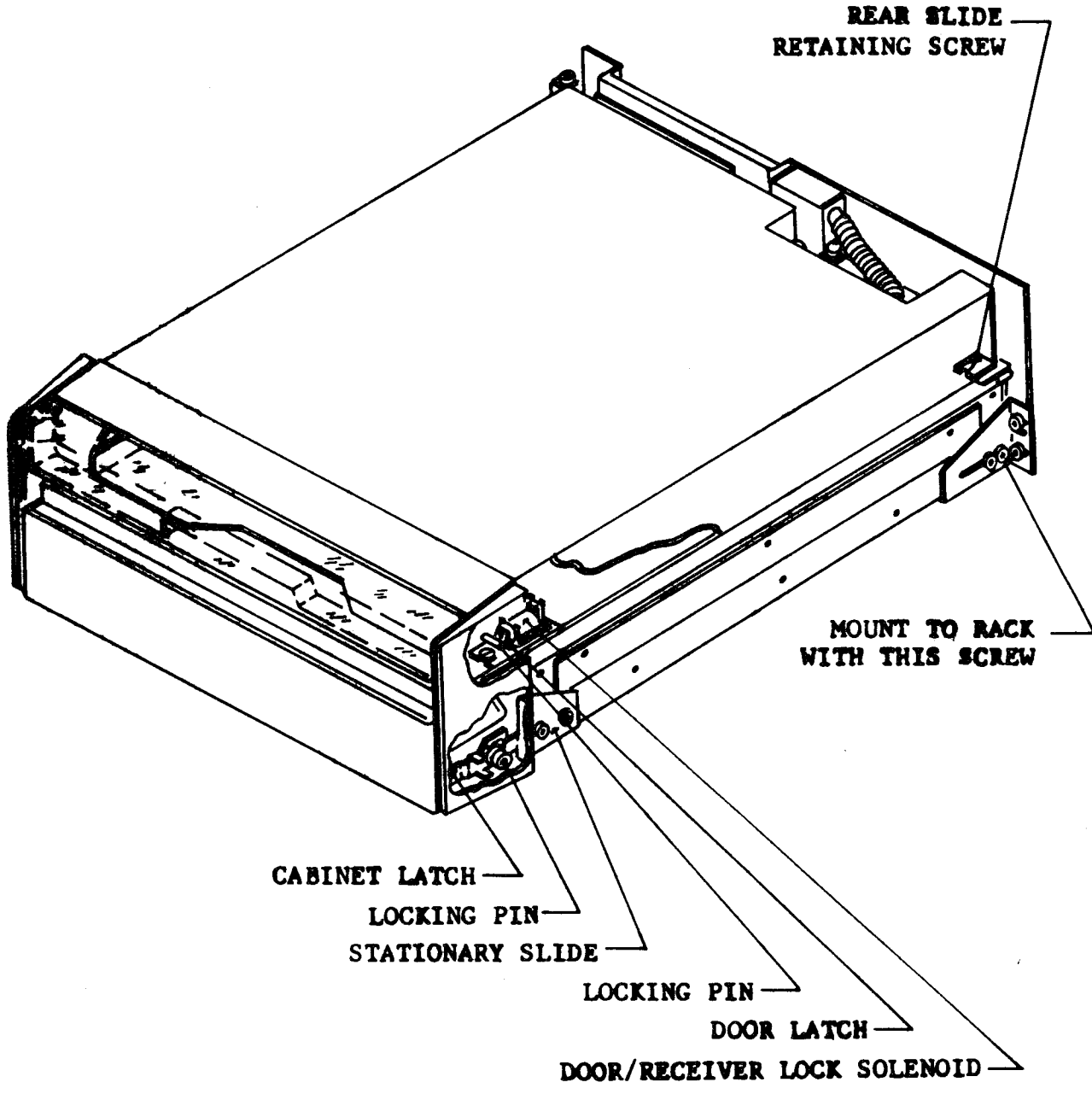
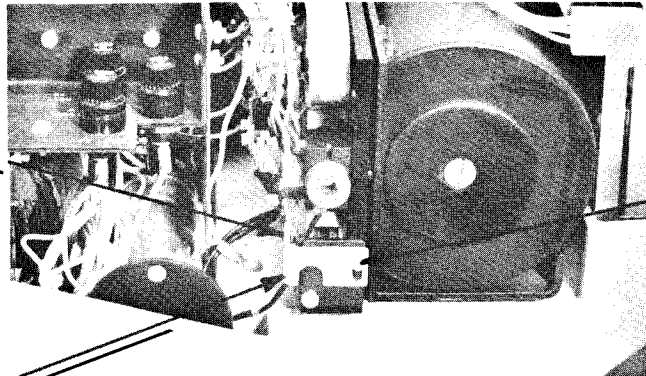


FIGURE 1

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SIZE	CODE IDENT NO.	DWG NO.
A		IP 700715
SCALE	REV	SHEET 9

SHIPPING RESTRAINT

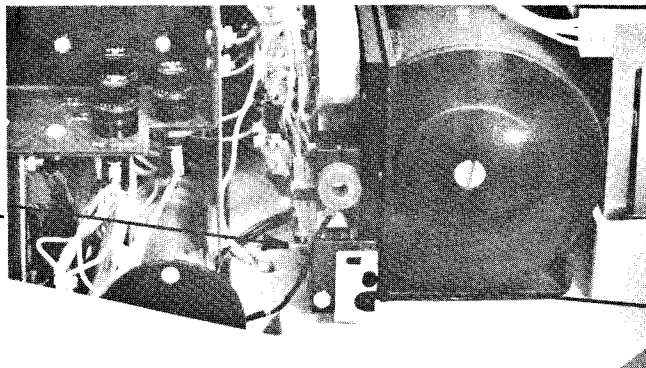


POSITIONED ON
RETRACT SWITCH
ACTUATOR

RESTRAINT
RETAINING
SCREW

SHIPPING
RESTRAINT

INSTALLED POSITION



RETRACT SWITCH
ACTUATOR

RESTRAINT

STOWED POSITION

FIGURE 2

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SIZE A	CODE IDENT NO.	DWG NO. JP 700715
SCALE	REV	SHEET 10



INTERCONNECT
BOARD
P/N 700713

COMPONENT
SIDE

DATA AND
STATUS BRD
P/N 700645

CONTROL BOARD
P/N 700463

MAJOR BRD
P/N 700647

FIGURE 3

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CODE IDENT NO.

DWG NO.

A

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REV

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APPENDIX
PM-DD/8 DUAL DISC SPECIFICATION

Please note that these specifications (capacity) represent two (2) logical unit addresses within the same chassis.

SPECIFICATIONS:

Gross Capacity:	5.0 M Bytes
Transfer Rate:	11.1usec/word
Recording Density:	2200 Bits/Inch, max.
Track Density:	100 tracks/inch
Disc Rotational Speed	1500 RPM
Speed Variation:	<u>±</u> 1% Max.
Access Times:	
Track to Track	15ms
Average	50ms
Maximum	90ms
Reliability:	
Recoverable errors(Max.)	1 in 1×10^{10} bits -ransferred
Non-recoverable errors (Max.)	1 in 1×10^{12} bits transferred
Mean timebetween failure (MTBF)	5000 hrs.
Mean time to repair (MTTR)	Less than 1 hour
Surfaces/Drive:	4
Tracks/Surface:	200 + 3 Spare
Sectors/Track:	16
Words/Sector:	256
Time for 1/2 revolution	20
Recording Mode:	Double frequency encoded
Cartridge Unload/Load Cycle:	60 seconds
Cartridge:	IBM 2315 type (D.E.C. compatible)

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CODE IDENT NO.

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SPECIFICATIONS (Continued)

Power Requirements:

100, 110, 120, 130, 200,
220, 230, 240, 250, and
260 VAC \pm 10% 47-63Hz

Physical Dimensions:

Height 7.00 inches
Width 17.60 inches
Length 22.00 inches
Weight 80 Lbs.
19 inch standard RETMA mounting

Environment (Operational)

Temperature 50 to 100 degrees F
Humidity 5 to 95% non condensing
(R.H.)

Models:

PM-DDA/8 RK05-AA
PM-DDB/8 RK05-BB

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SIZE

CODE IDENT NO.

DWG NO.

A

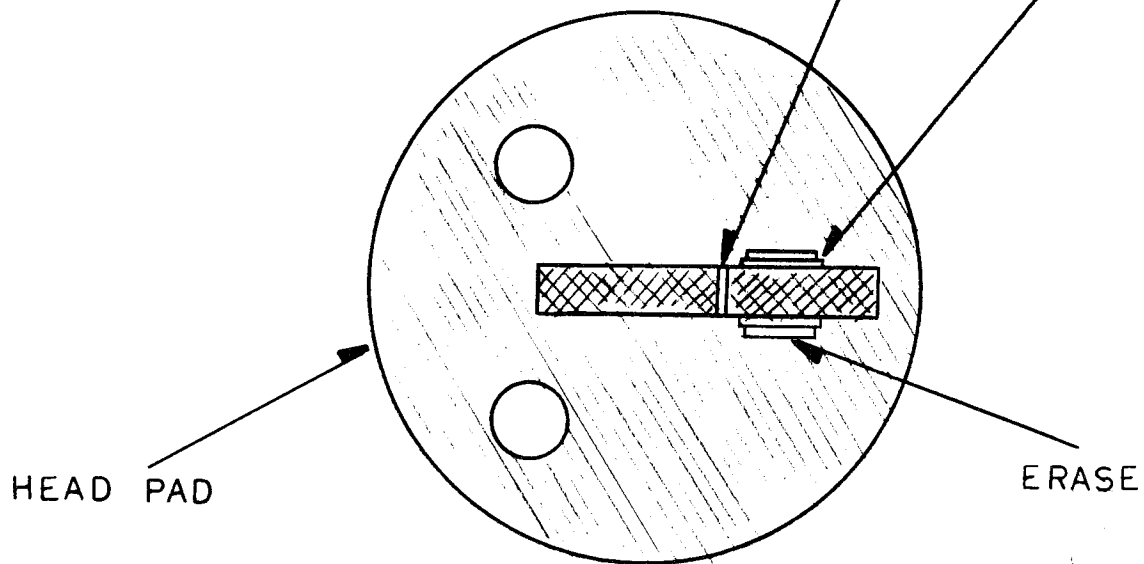
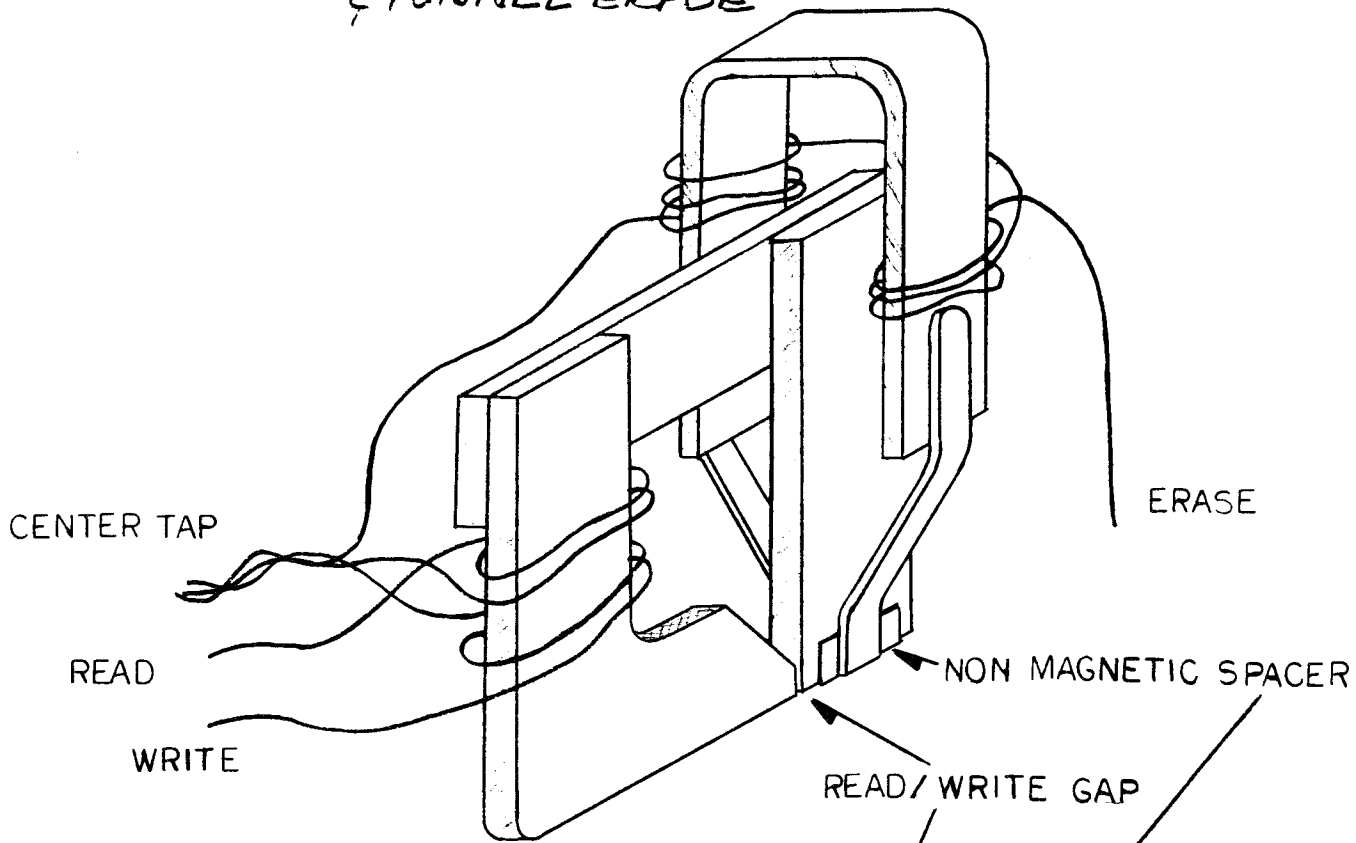
MA 700655

SCALE

REV

SHEET 44

READ WRITE HEAD
& TUNNEL ERASE



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SECTION IV
SCHEMATICS

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SIZE

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CODE IDENT NO.

DWG NO.

MA 700655

SCALE

REV

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PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PL 700643-100	SM 3	REV LTR D					
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FINO	SYN	C/I USAGE				
								C/I CODE	TRY ON HAND	P A R	UNIT COST	
	1	700642-001	P.W.B./CONTROL			1	B					
	2	3432-1002	CONNECTOR, 40PIN	3M CO.	26066	2	A					
D						3						
D						4						
						5						
	6	SN74161	SYNCHRONOUS 4-BIT COUNTERS	TEXAS INSTR	01295	6	A					
	2	SN74H04	HEX INVERTER	TEXAS INSTR	01295	7	A					
	8	SN7400	QUAD 2-INPUT POS-NAND GATES	TEXAS INSTR	01295	8	A					
	3	SN7404	HEX INVERTER	TEXAS INSTR	01295	9	A					
	1	SN74H10	TRIPLE 3-INPUT POS-NAND GATES	TEXAS INSTR	01295	10	A					
	6	SN7402	QUAD 2-INPUT POS-NOR GATES	TEXAS INSTR	01295	11	A					
	9	SN7474	DUAL D-TYPE POS-EDGE TRIGGERED FLIP-FLOP	TEXAS INSTR	01295	12	A					
D	3	SN7408	QUAD 2-INPUT POS-AND GATES	TEXAS INSTR	01295	13	A					

PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PL 700649-100	SM 4	REV LTR C					
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FINO	SYN	C/I USAGE				
								C/I CODE	TRY ON HAND	P A R	UNIT COST	
	1	SN74H52	EXPANDABLE 4 WIDE AND-OR GATES	TEXAS INSTR	01295	14	A					
	1	SN7442	4-LINE-TO-10-LINE DECODERS	TEXAS INSTR	01295	15	A					
	2	SN7410	TRIPLE 3-INPUT POS-NAND GATE	TEXAS INSTR	01295	16	A					
	2	SN74123	DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR W/CLEAR	TEXAS INSTR	01295	17	A					
	4	196021-380	QUAD 2-INPUT RECEIVERS			18	A					
	4	SN75452	DUAL PERIPHERAL POS-NAND DRIVER	TEXAS INSTR	01295	19	A					
	1	SN7496	5-BIT SHIFT REGISTERS	TEXAS INSTR	01295	20	A					
	1	SN7485	4-BIT MAGNITUDE COMPARATOR	TEXAS INSTR	01295	21	A					
	1	SN74H76	DUAL J-K TYPE FLIP-FLOPS W/PRESET AND CLEAR	TEXAS INSTR	01295	22	A					
C	2	CD15FD 221J03	CAPACITOR, 220pf, ±5%	CORNELL-DUBILIER	93790	23	A					
	4	CS13BF 685M	CAPACITOR, TANT, 6.8uf	MIL-C-26655		24	A					
	29	CO69B1 60E103Z	CAPACITOR, .01uf, ±20%	SPRAGUE	05571	25	A					
B	2	CD15FD 471J03	CAPACITOR, 470pf	CORNELL-DUBILIER	93790	26	A					

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 48



PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700643-100	SH 5	REV. LTR B				
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIN D	SYM	C/I USAGE			
								C/I CODE	INV ON HAND	P A R	UNIT COST
2	CD15FC 821J03	CAPACITOR, 820pf, ±5%	CORNELL-DUBILIER	93790		27	A				
1	CD15FD 181J03	CAPACITOR, 180pf, ±5%	CORNELL-DUBILIER	93790		28	A				
1	CD15FC 561J03	CAPACITOR, 560pf, ±5%	CORNELL-DUBILIER	93790		29	A				
2	X463UW	CAPACITOR, .022μf, ±10%, 50V	T R W	84411		30	A				
1	CD15CD 100J03	CAPACITOR, 10pf, ±5%	CORNELL-DUBILIER	93790		31	A				
B	1	CK06 BX-472K	CAPACITOR, 4700 pf, 200 V, 10%	MIL-C-11015		32	A				
1	JKT0-80	CRYSTAL OSCILLATOR 5.760 MHZ	CTS	75378		33	A				
B	1	138000-001	DIODE			34	A				
A	2	100013-011	RESISTOR, MODULE, 390Ω, ±5%			35	E				
A	2	100013-012	RESISTOR, MODULE, 180Ω, ±5%			36	E				
						37					
6	RC07G F102J	RESISTOR, 1K, 5%, 1/4W	MIL-R-11			38	A				
6	RC07G F101J	RESISTOR, 100Ω, 5%, 1/4W	MIL-R-11			39	A				

PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700643-100	SH 6	REV. LTR A				
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIN D	SYM	C/I USAGE			
								C/I CODE	INV ON HAND	P A R	UNIT COST
						40					
						41					
						42					
						43					
1	RC07G 562J	RESISTOR, 5.6K, 5%, 1/4W	MIL-R-11			44	A				
A	1	RN60D 2432 F	RESISTOR, 24.3K, 1%, 1/4W	MIL-R-10509		45	A				
3	RC07G F391J	RESISTOR, 390Ω, 5%, 1/4W	MIL-R-11			46	A				
3	RC07G F181J	RESISTOR, 180Ω, 5%, 1/4W	MIL-R-11			47	A				
						48					
A	AR	5951	WIRE, 30AWG SOLID, KYNAR INSULATION	ALPHA WIRE	23172	49	G				
	AR	SN63WRAP3	SOLDER	QQ-5-571		50	G				
	REF	5D700643	SCHEMATIC DIAGRAM CONTROL, PM-DC/B			51	C				
	REF	T5700643	TEST SPECIFICATION CONTROL, PM-DC/B			52	C				

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 49

PARTS LIST	Plessey Memories Incorporated Santa Ana, California	PL 700645-100	REV LTR B
		CODE IDENT NO. 52648	SH OF 2

BOARD ASSEMBLY, DATA BUFFER & STATUS, PM-DC/8			
LTR	DESCRIPTION	DATE	APPROVED
-	REL TO PROD PER EDO 500657	20 NOV 77	Dwt JB
A	INCORPORATED EO 1215	6-1-76	JB
B	INCORPORATED EO 1270	9-8-76	JB

PRODUCTION RELEASE

REV STATUS OF SHEETS	REV LTR	BB	-	-	AB	-														
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PARTS LIST	Plessey Memories Incorporated Santa Ana, California	CODE IDENT NO. 52648	PARTS LIST NO. PL 700645-100	SH 2	REV LTR B
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CROSS INDEX OF REFERENCE DESIGNATIONS TO FIND NO.

REFERENCE DESIGNATION	F I N O.	REFERENCE DESIGNATION	F I N O.	REFERENCE DESIGNATION	F I N O.	REFERENCE DESIGNATION	F I N O.
U1, U10, U16, U18, U19, U25	3	U37	19	C16	35	C25 IS LAB SET	-
U2, U3, U5, U6, U12	4	U38	20	C17, C30	36		
U4, U7, U11, U13, U52	5	U41, U57	21		37		
UB	6	U43	22	C26, C31	38		
U9, U42, U44, U47	7	U50	23	C27, C29	39		
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U14, U15, U23, U24	8	U56	25		41		
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U21, U63	10	U62	27	R1	43		
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U29, U35, U49, U53	12		29	R4, R5	45		
U30, U46	13		30	R6, 19, 21, 22, 23, 29, 31	46		
U31	14	C1, 7, 12, 13, 18, 19, 20	31	R7, R12	47		
U32, U45	15	C6, C21	32	R8, R13	48		
U33	16	C2, 3, 4, 5, 8, 9, 10,	33	R10, R30	49		
U34, U59	17	C11, 14, 22, 23, 24	34	R11	50		
U36, U54, U55, U58	18	C15	34	R14 - R16	51		

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 50



PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700645-100	SH 3	REV LINE —				
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y M	C/I USAGE			
								C/I CODE	INV ON HAND	P A R	UNIT COST
1	700644-001	P.W.B./DATA BUFFER & STATUS				1	5				
6	SN7495	4-BIT PARALLEL-ACCESS SHIFT REGISTER	TEXAS INSTR	01295		3	A				
5	136021-380	QUAD 2-INPUT RECEIVERS				4	A				
5	SN7438	QUAD 2-INPUT NAND BUFFERS W/OPEN-COLLECTOR OUTPUTS	TEXAS INSTR	01295		5	A				
1	136020-384	QUAD 2-INPUT RECEIVERS				6	A				
7	SN7402	QUAD 2-INPUT POS-NOR GATES	TEXAS INSTR	01295		7	A				
4	SN74174	HEX/QUAD D-TYPE FLIP-FLOP W/CLEAR	TEXAS INSTR	01295		8	A				
3	SN74157	QUAD 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	TEXAS INSTR	01295		9	A				
2	SN7440	DUAL 4-INPUT POS-NAND BUFFERS	TEXAS INSTR	01295		10	A				
1	SN7442	4-LINE-TO-10-LINE DECODERS	TEXAS INSTR	01295		11	A				
4	SN7408	QUAD 2 INPUT POS-AND GATES	TEXAS INSTR	01295		12	A				
2	SN74H76	DUAL J-K FLIP-FLOPS W/PRESET AND CLEAR	TEXAS INSTR	01295		13	A				

PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700645-100	SH 4	REV LINE —				
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y M	C/I USAGE			
								C/I CODE	INV ON HAND	P A R	UNIT COST
1	SN74123	DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR W/CLEAR	TEXAS INSTR	01295		14	A				
2	SN74H53	EXPANDABLE 4-WIDE AND-OR INVERT GATES	TEXAS INSTR	01295		15	A				
1	SN74H74	DUAL D-TYPE POS-EDGE TRIGGERED FLIP-FLOP	TEXAS INSTR	01295		16	A				
2	SN7404	HEX INVERTER	TEXAS INSTR	01295		17	A				
4	SN7400	QUAD 2-INPUT POS-NAND GATES	TEXAS INSTR	01295		18	A				
1	SN7432	QUAD 2-INPUT POS-OR GATES	TEXAS INSTR	01295		19	A				
1	SN7496	5-BIT SHIFT REGISTERS	TEXAS INSTR	01295		20	A				
2	SN7474	DUAL D-TYPE POS-EDGE TRIGGERED FLIP-FLOP	TEXAS INSTR	01295		21	A				
1	SN74H04	HEX INVERTER	TEXAS INSTR	01295		22	A				
1	SN7410	TRIPLE 3-INPUT POS-NAND GATE	TEXAS INSTR	01295		23	A				
1	SN74193	SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK W/CLEAR)	TEXAS INSTR	01295		24	A				
1	SN7485	4-BIT MAGNITUDE COMPARATOR	TEXAS INSTR	01295		25	A				
1	SN74H00	QUAD 2-INPUT POS-NAND GATES	TEXAS INSTR	01295		26	A				

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 51



PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700645-100	SH 5	REV. LTR A				
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIN O. D.	SY M.	C/I USAGE			
								C/I CODE	INV ON HAND	P A R	UNIT COST
	1	SN7437	QUAD 2-INPUT POS-NAND BUFFERS	TEXAS INSTR	01295		27 A				
	1	TZAI1-10	75 NS DELAY LINE	RHOMBUS IND	16714		28 A				
							29				
							30				
	7	CS13BF 685M	CAPACITOR, TANT, 6.8uf	MIL-C-26655			31 A				
A	2	150D475X 0010A2	CAPACITOR, TANT, 4.7uf, 10V	SPRAGUE	05571		32 A				
	12	C069B1 60E103E	CAPACITOR, .01uf, 50V	SPRAGUE	05571		33 A				
	1	CD15ED 390J03	CAPACITOR, 39pf, 500V	CORNELL-DUBILIER	93790		34 A				
	1	CD15CD 100J03	CAPACITOR, 10pf, 500V	CORNELL-DUBILIER	93790		35 A				
	2	CD15FD 181J03	CAPACITOR, 180pf,	CORNELL-DUBILIER	93790		36 A				
							37				
	2	CD15FD 331J03	CAPACITOR, 330pf	CORNELL-DUBILIER	93790		38 A				
	2	CD15FD 471J03	CAPACITOR, 470pf	CORNELL-DUBILIER	93790		39 A				

PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700645-100	SH 5	REV. LTR B				
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FIN O. D.	SY M.	C/I USAGE			
								C/I CODE	INV ON HAND	P A R	UNIT COST
							40				
							41				
							42				
	1	RC07GF 222J	RESISTOR, 2.2K, 5%, 1/4W	MIL-R-11			43 A				
B	13	RC07GF 102J	RESISTOR, 1K, 5%, 1/4W	MIL-R-11			44 A				
B	2	RC07GF 512J	RESISTOR, 5.1K, 5%, 1/4W	MIL-R-11			45 A				
	7	RC07GF 101J	RESISTOR, 100Ω, 5%, 1/4W	MIL-R-11			46 A				
	2	RC07GF 391J	RESISTOR, 390Ω, 5%, 1/4W	MIL-R-11			47 A				
	2	RC07GF 181J	RESISTOR, 180Ω, 5%, 1/4W	MIL-R-11			48 A				
B	2	RC07GF 472J	RESISTOR, 4.7K, 5%, 1/4W	MIL-R-11			49 A				
	1	RC07GF 331J	RESISTOR, 330Ω, 5%, 1/4W	MIL-R-11			50 A				
B	3	RC07GF 201J	RESISTOR, 200Ω, 5%, 1/4W	MIL-R-11			51 A				
							52				

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 52



PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700645-100	SM I	REV. LTR -					
QTY REQD	NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y M	C/I USAGE			
									C/I CODE	INV ON HAND	P A R	UNIT COST
AR		5951	WIRE, 30 AWG SOLID, KYNAR INSULATION, COLOR: OPTIONAL	ALPHA WIRE	23172		53G					
AR		SN63WRAP3	SOLDER	QQ-S-571			54G					
							55					
							56					
REF		SD700645	SCHEMATIC DIAGRAM				57C					
REF		TS700645	TEST SPECIFICATION				58C					

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	A	52648	MA 700655
SCALE	REV	SHEET	53




PARTS LIST	 Plessey Memories Incorporated Santa Ana, California	DATE BY <i>GATES 11/7/71</i>	DATE LISTED BY	PL700647-100	SM
		DATE BY <i>20 NOV 71</i>	DATE LISTED BY <i>11/2/75</i>	CODE IDENT NO. 52648	OF 6
BOARD ASSEMBLY MAJOR REGISTER, PM-DC/8					

LTR	DESCRIPTION	DATE	APPROVED	LTR	DESCRIPTION	DATE	APPROVED
-	REL TO PROD PER ERD 50065B	20 NOV 71	<i>Dist 78</i>				

PRODUCTION RELEASE

REV STATUS OF SHEETS	REV LTR	1	2	3	4	5	6	7	8	9	10	ENTERPREY SYMBOLS: U, M, A, F, B, L, C, S		
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PARTS LIST	 Plessey Memories Incorporated Santa Ana, California	CODE IDENT NO. 52648	DATE LISTED BY	PL700647-100	SM 2
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CROSS INDEX OF REFERENCE DESIGNATIONS TO FIND NO.

REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.	REFERENCE DESIGNATION	FIND NO.
U2, 4, 21, 22, 26, 41	4	U29, 30, 31	20		36		
U28, 42	5	U7, 10	21		37		
U1, 3	6	U5, 6, 8, 9	22		38		
U13, 14, 27	7	U37, 38, 46	23		39		
U25	8	U39	24	C20	40		
U12	9		25	C2-4, 6-19, 21, 22, 24-31	41		
U34, 36, 40, 47, 48, 49	10		26	34-42, 46, 47, 49, 51, 52			
U11	11		27	C1, 5, 32, 33, 43, 44, 45, 48, 50	42		
U35	12	R2	28				
U18, 19, 32, 33	13	R1	29				
U20	14	R3, 4, 5, 6, 7	30				
U15	15		31				
U23, 24	16		32				
U17	17	RU3, 4	33				
U43, 44, 45	18	RU1, 2	34				
U16	19		35				

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 54

PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700647-100	SM 3	REV LTR —					
NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FINO	SYN	C/I USAGE			
									C/I CODE	INV ON HAND	P A R	UNIT COST
	1	100646-001	P.W.B. - MASTER REGISTER				1	B				
							2					
							3					
	6	SN 7400	QUAD 2-INPUT POS-NAND BUFFERS	T. I.	01295		4	A				
	2	SN 7402	QUAD 2-INPUT POS-NOR GATES	T. I.	01295		5	A				
	2	SN 7404	HEX INVERTER	T. I.	01295		6	A				
	3	SN 7408	QUAD 2-INPUT POS-AND GATES	T. I.	01295		7	A				
	1	SN 7410	TRIPLE 3-INPUT POS-NAND GATES	T. I.	01295		8	A				
	1	SN 7411	TRIPLE 3-INPUT POS-AND GATES	T. I.	01295		9	A				
	6	SN 7438	QUAD 2-INPUT POS-NAND BUFFERS W/OPEN COLLECTOR	T. I.	01295		10	A				
	1	SN 7440	DUAL 4-INPUT POS-NAND BUFFERS	T. I.	01295		11	A				
	1	SN 74H52	EXPANDABLE 4-WIDE AND-OR GATES	T. I.	01295		12	A				
	4	SN 7474	DUAL D-TYPE POS-EDGE-TRIGGERED FLIP-FLOP	T. I.	01295		13	A				

PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700647-100	SM 4	REV LTR —					
NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	FINO	SYN	C/I USAGE			
									C/I CODE	INV ON HAND	P A R	UNIT COST
	1	SN 74H74	DUAL D-TYPE POS-EDGE-TRIGGERED FLIP-FLOP	T. I.	01295		14	A				
	1	SN 7486	QUAD 2-INPUT EXCLUSIVE-OR-GATES	T. I.	01295		15	A				
	2	SN 7496	5-BIT SHIFT REGISTERS	T. I.	01295		16	A				
	1	SN 745139	DECODERS/DEMULTIPLEXERS	T. I.	01295		17	A				
	3	SN 74161	SYNCHRONOUS 4-BIT COUNTERS	T. I.	01295		18	A				
	1	SN 74174	HEX/QUAD D-TYPE FLIP-FLOPS W/CLEAR	T. I.	01295		19	A				
	3	SN 74179	4-BIT PARALLEL-ACCESS SHIFT REGISTERS	T. I.	01295		20	A				
	2	SN 75451	DUAL PERIPHERAL POS-AND DRIVER	T. I.	01295		21	A				
	4	SN 75452	DUAL PERIPHERAL POS-NAND DRIVER	T. I.	01295		22	A				
5	3	136021-380	QUAD 2-INPUT RECEIVER				23	B				
	1	136020-384	QUAD 2-INPUT RECEIVER				24	B				
							25					
							26					

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SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 55

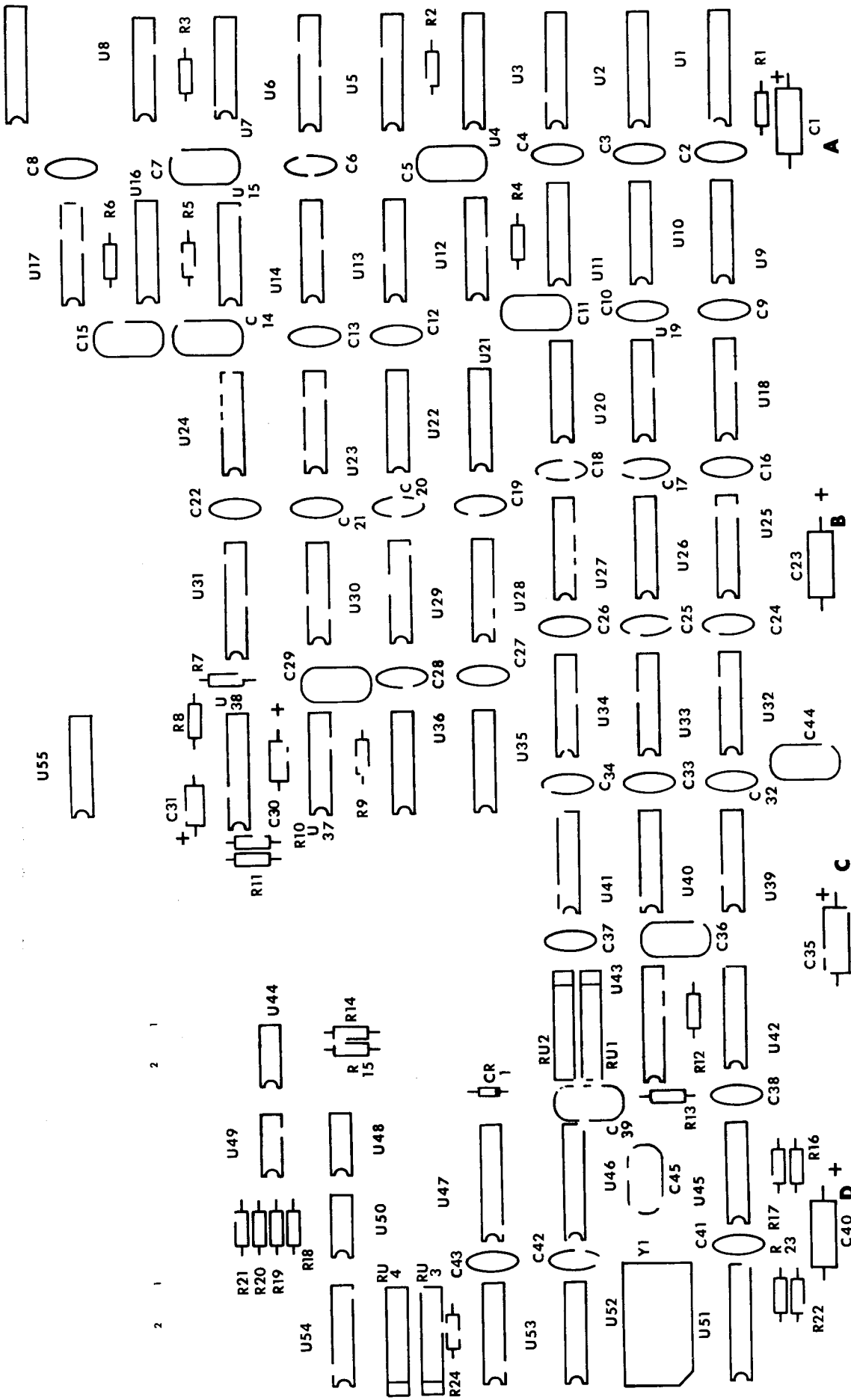


PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700647-100	SM 5	C/I USAGE					
NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y H	C/I CODE	INV ON HAND	P A R	UNIT COST
								27				
	1	RC07GF101J	RESISTOR, 100Ω ±5%, 1/4 WATT	MIL-R-11				28 G				
	1	RC07GF100J	RESISTOR, 10Ω ±5%, 1/4 WATT	MIL-R-11				29 G				
	5	RC07GF102J	RESISTOR, 1K ±5%, 1/4 WATT	MIL-R-11				30 G				
								31				
								32				
	2	100013-011	RESISTOR MODULE, 390 Ω	CTS P/N 750-81-R390				33 B				
	2	100013-012	RESISTOR MODULE, 180 Ω	CTS P/N 750-81-R180				34 B				
								35				
								36				
								37				
								38				
								39				

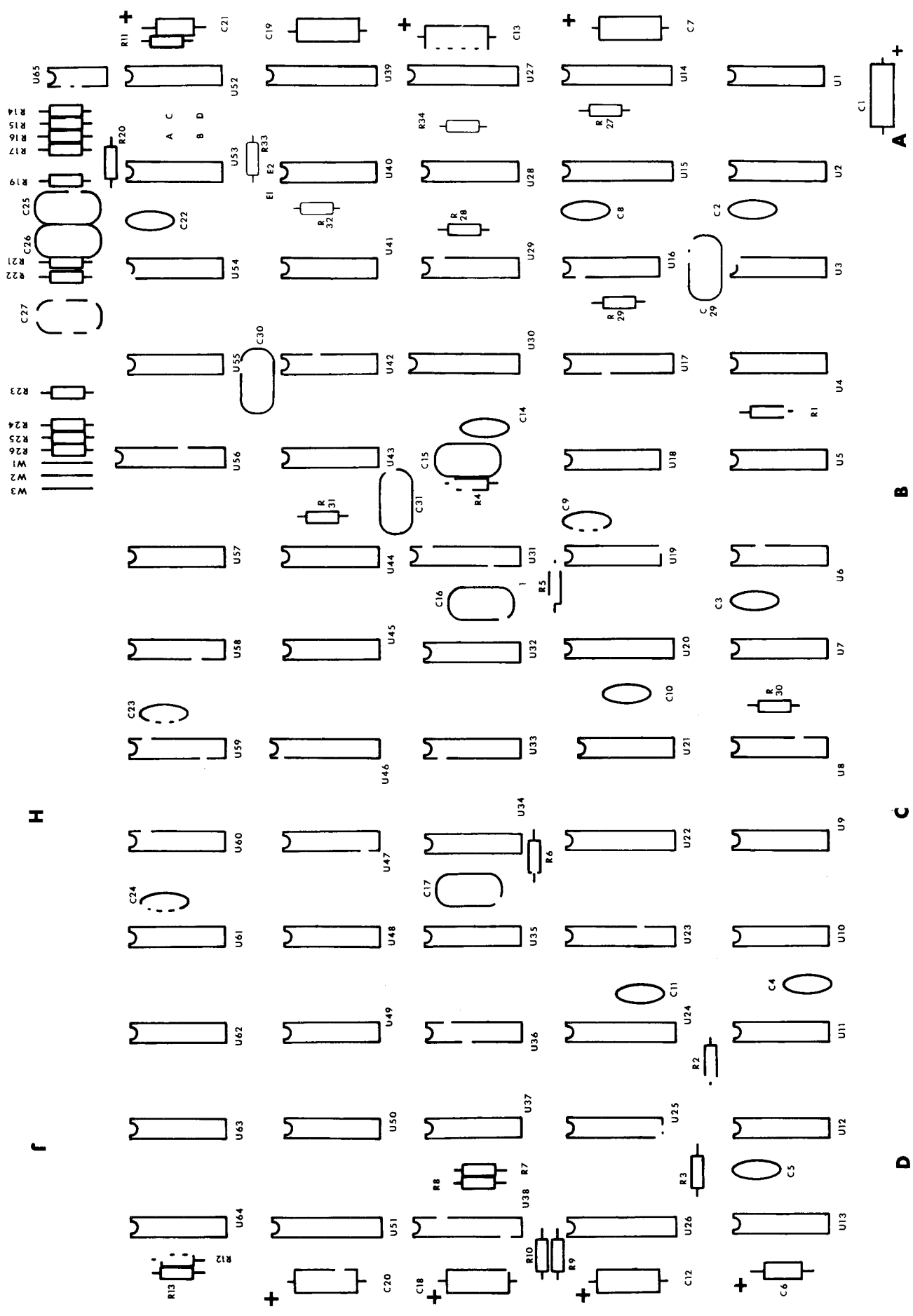
PARTS LIST		Plessey Memories Incorporated Santa Ana, California		CODE IDENT NO. 52648	PARTS LIST NO. PL700647-100	SM 6	C/I USAGE					
NOTE	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y H	C/I CODE	INV ON HAND	P A R	UNIT COST
	1	CD15FD471JQ3	CAPACITOR, 470 pF ±5%, 500V	CORNELL-DUBILIER	93790			40 A				
X2	41	4069B160 E103Z	CAPACITOR, .01 μF ±20%, 16V	SPRAGUE	05571			41 A				
	9	150D156 X0020BZ	CAPACITOR, 15 μF ±20%, 20V	SPRAGUE	05571			42 A				
								43				
	AR	SN63WRAP3	SOLDER	QQ-S-571				44 G				
	AR	5951	WIRE, 30 AWG SOLID, KYNAR INSUL., COLOR: OPTIONAL	ALPHA WIRE	23172			45 A				
								46				
								47				
								48				
								49				
								50				
	REF	SKSD700647	SCHMATIC DIAGRAM MASTER REGISTER					51 K				
	REF	TS700647	TEST SPECIFICATION MASTER REGISTER					52 K				

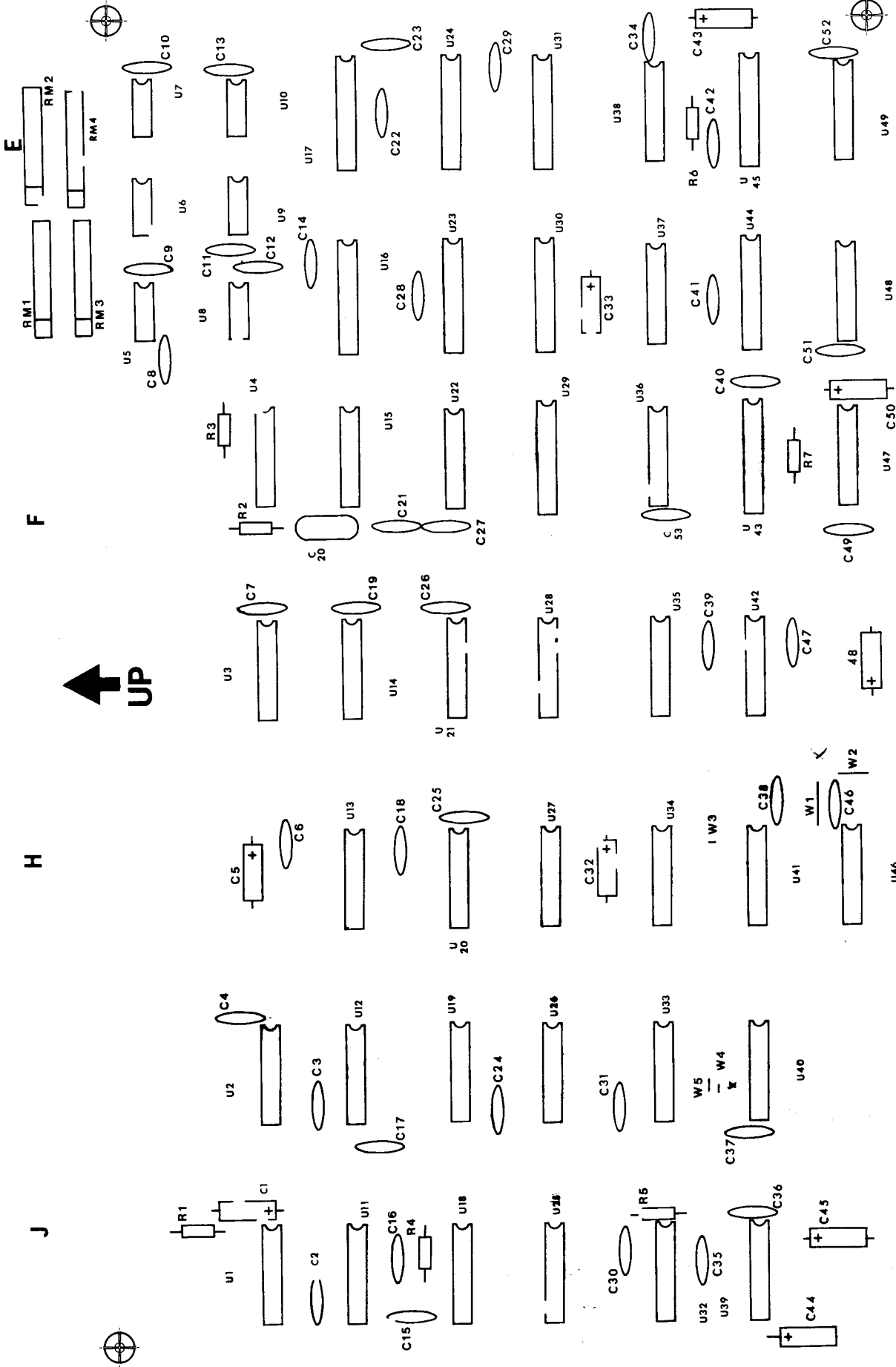
The information hereon is the property of PLESSEY MEMORIES INCORPORATED. Transmittal, receipt, or possession of the information does not comply, license, or imply any rights to use, sell, or manufacture from this information and no reproduction or publication of it, in whole or part, shall be made without written authorization from PLESSEY MEMORIES, INC.

SIZE A	CODE IDENT NO. 52648	DWG NO. MA 700655
SCALE	REV	SHEET 56



COMPONENT LAYOUT Control Board 700643





A

B

C

D

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-		REL TO PROD PER ERO 500708	1-15-76	<i>[Signature]</i>
A		INCORPORATED EO # 1173	5-13-76	<i>[Signature]</i>
B		INCORPORATED EO 1214	6-1-76	<i>[Signature]</i>
C		INCORPORATED EO 1269	9-2-76	<i>[Signature]</i>

SIDE 2		SIDE 1	
DISC SEEK FAIL L	A	CRC DATA H	
DISC ADD 64 L	B	RD CLK 1 H	
DISC ADD 16 L	C	IDLE (1) H	
DISC DRIVE ϕ L	D	RDY S/R/W H	
DISC ADD 128 L	E	FILE RDY H	
STROBE (1) H	F	CLR SECTOR AD L	
DISC ADD 4 L	H	CLR ALL L	
DISC ADD 32 L	J	B DATA 11 H	
DISC ADD 2 L	K	B DATA 10 H	
DISC RDY S/R/W L	L	B DATA 9 H	
LD DISC ADDRS H	M	B DATA 8 H	
CRC 16 (1) H	N	DISC DRIVE 3 L	
SECTOR ADDRS (1) H	P	DISC DRIVE 2 L	
B DATA 7 H	R	DISC DRIVE 1 L	
HALF BLOCK H	S	DISC ADD 1 L	
FUNCTION ϕ 2 H	T	DISC ADD 8 L	
FUNCTION ϕ 0 H	U	DATA ENABLE (1) H	
FUNCTION ϕ 1 H	V	EUAB DATA L	
6 PM 30K H	A	12 BIT OK H	
CLR DRIVE CMD L	B	DISC FILE RDY L	
DRV REV ϕ H	C	DISC CAPACITY EX L	
DISC WRT STATUS L	D	END STATE (ϕ) H	
ERROR CLR L	E	LAST WORD PL H	
SECTOR SEEK (ϕ) H	F	WRITE (1) H	
BTP2 H	H	PM DATA 11 H	
SHIFT WRT BUFF L	J	BTP3 H	
BRK ENAB CLK H	K	SET IDLE PL L	
B LAST BRK H	L	LD MAIN SHIFT L	
BTP3 OK H	M	DATA CLK OK H	
LAST BRK (1) H	N	SHIFT CRC L	
MAIN (ϕ) H	P	DATA STATE (ϕ) H	
IDLE (ϕ) H	R	DATA IN (ϕ) H	
RD SHIFT DB L	S	CLR CNTRS L	
HI MAIN SHFT L	T	RTRY - L	
BRK IN CLK H	U	SHFT SURF/SEK H	
WRT CMD L	V	STATE ENAB B H	

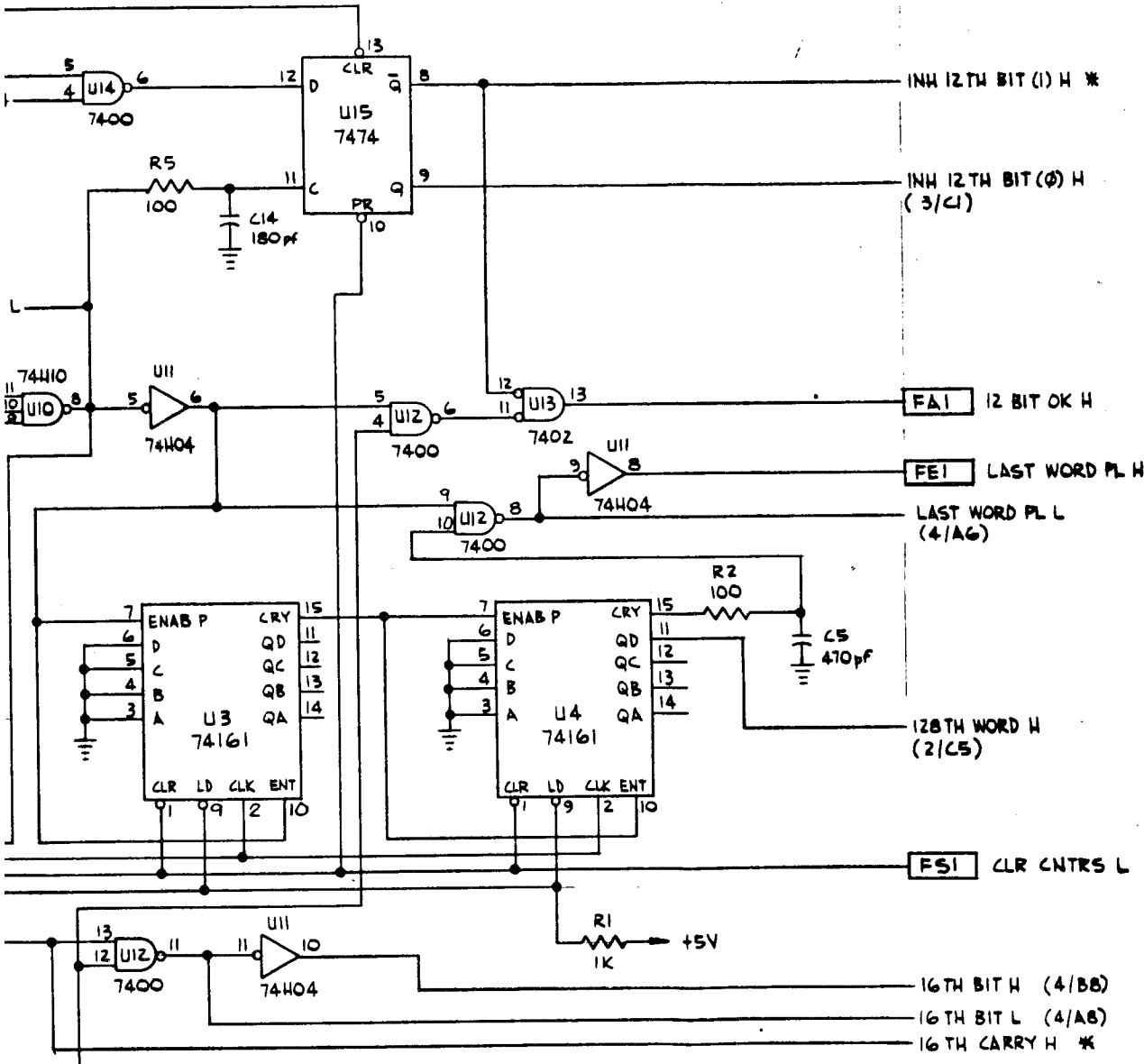
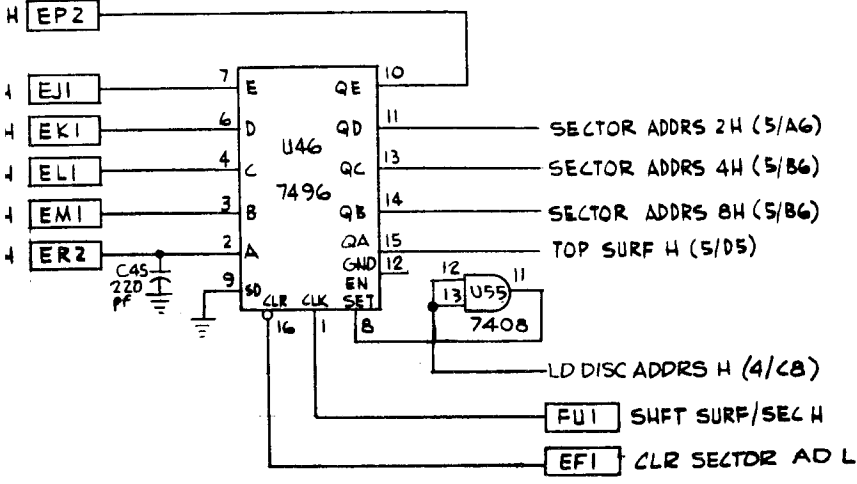
1		21	DISC ADD 1 L
2	GND	22	GND
3	DISC CAPACITY EX L	23	DISC DRIVE ϕ L
4	GND	24	GND
5	DISC SEEK FAIL L	25	DISC ADD 32 L
6	GND	26	GND
7	DISC ACKNOWLEDGE L	27	DISC RDY S/R/W L
8	GND	28	GND
9	DISC SEC 2 L	29	DISC ADD 128 L
10	GND	30	GND
11	DISC DRIVE 3 L	31	DISC WRT CLK DAT AT L
12	GND	32	GND
13	DISC RESTORE L	33	DISC ADD 16 L
14	GND	34	GND
15	DISC DRIVE 2 L	35	DISC ADD 64 L
16	GND	36	GND
17	DISC ADD 4 L	37	DISC ADD 2 L
18	GND	38	GND
19	DISC DRIVE 1 L	39	DISC ADD 8 L
20	GND	40	GND

PRODUCTION RELEASE

PART/ASSY NO. & QTY PER ASSY					NOTE PART OR IDENTIFYING NO.					NOMENCLATURE OR DESCRIPTION / MATERIAL					SPEC/SOURCE		CODE IDENT NO.		FIND NO.						
PART/ASSY REV LTR					DO NOT SCALE DRAWING					CONTRACT NO.					Plessey Memories Incorporated		Santa Ana, California		A						
700643-100 PM-DC/B					SCREW THREADS PER HANDBOOK H-88 COUNTERBORE AND SPOTFACE FILLET RADIUS TO BE .015 MAXIMUM REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .015R ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1 STANDARD HOLE TOLERANCE PER AND 9007 TOLERANCES ON: .01 = ± .001, .001 = ± .0005, ANGLES = ± 30°					DRAWN <i>KRAVANIS</i> 1-15-76					DWG TITLE					SIZE		CODE IDENT NO.		DWG NO.	
NEXT ASSY USED ON					INTERPRET DIMENSIONS AND TOLERANCES PER USAS 14.5 DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH UNLESS OTHERWISE SPECIFIED					CHECKED <i>DwTuck</i> 2-17-76					SCHEMATIC DIAGRAM CONTROL PM-DC/8					D		52648		SD700643	
APPLICATION					OTHER APPROVALS					PROJ. ENGR <i>Humb</i> 2-17-76					PROD. DESIGN <i>John</i> 2-17-76					SCALE: -		REV: C		SHEET 1 OF 9	

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ZONE		LTR		REVISIONS	DATE	APPROVED
				DESCRIPTION		
				SEE SHEET 1		



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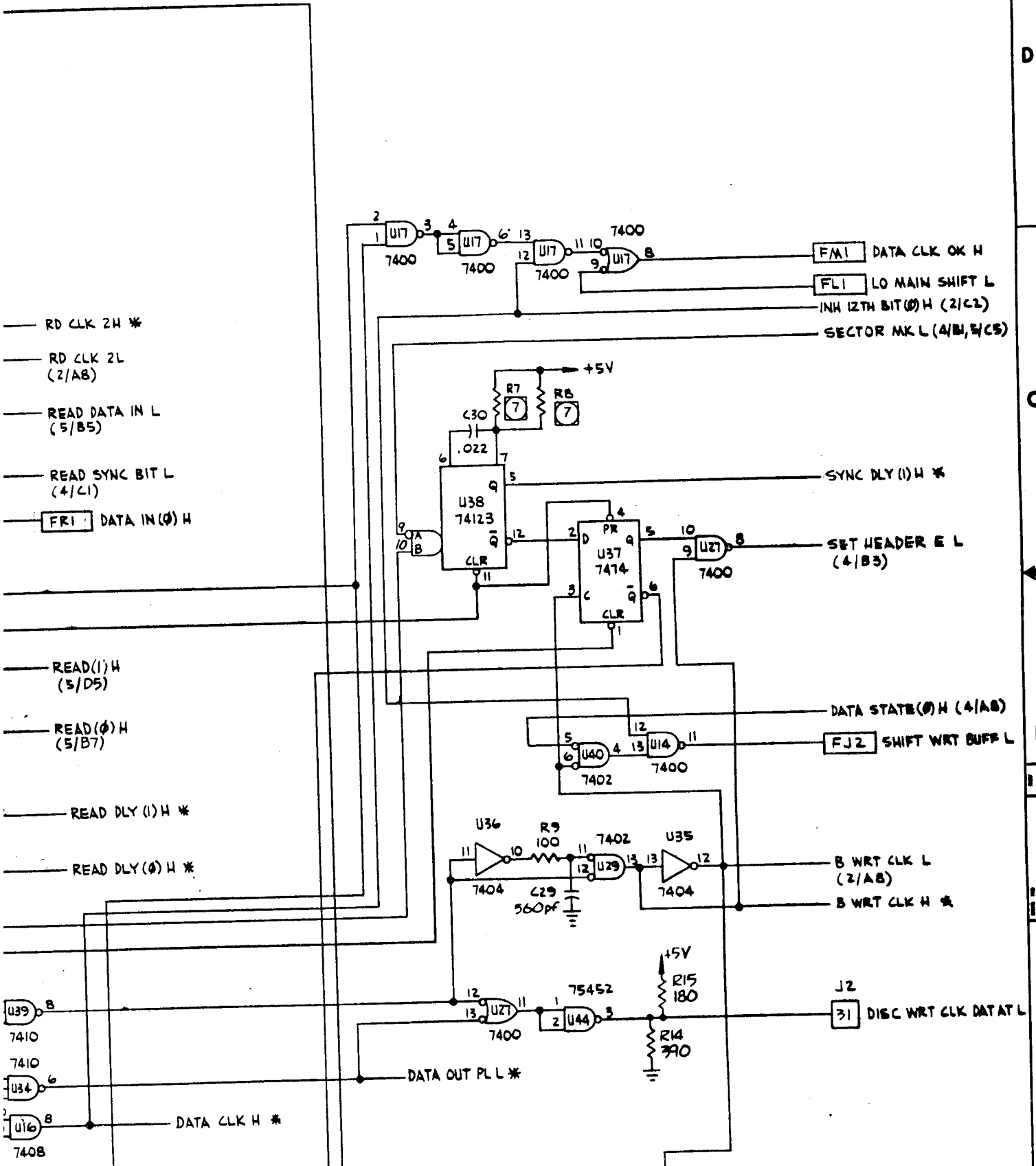
B

SD700643

A

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD 700643
SCALE: —	REV: C	SHEET 2 OF 5
DISTR NO.		

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
SEE SHEET 1				



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD 700643
SCALE: -	REV: C	SHEET 3 OF 5

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C

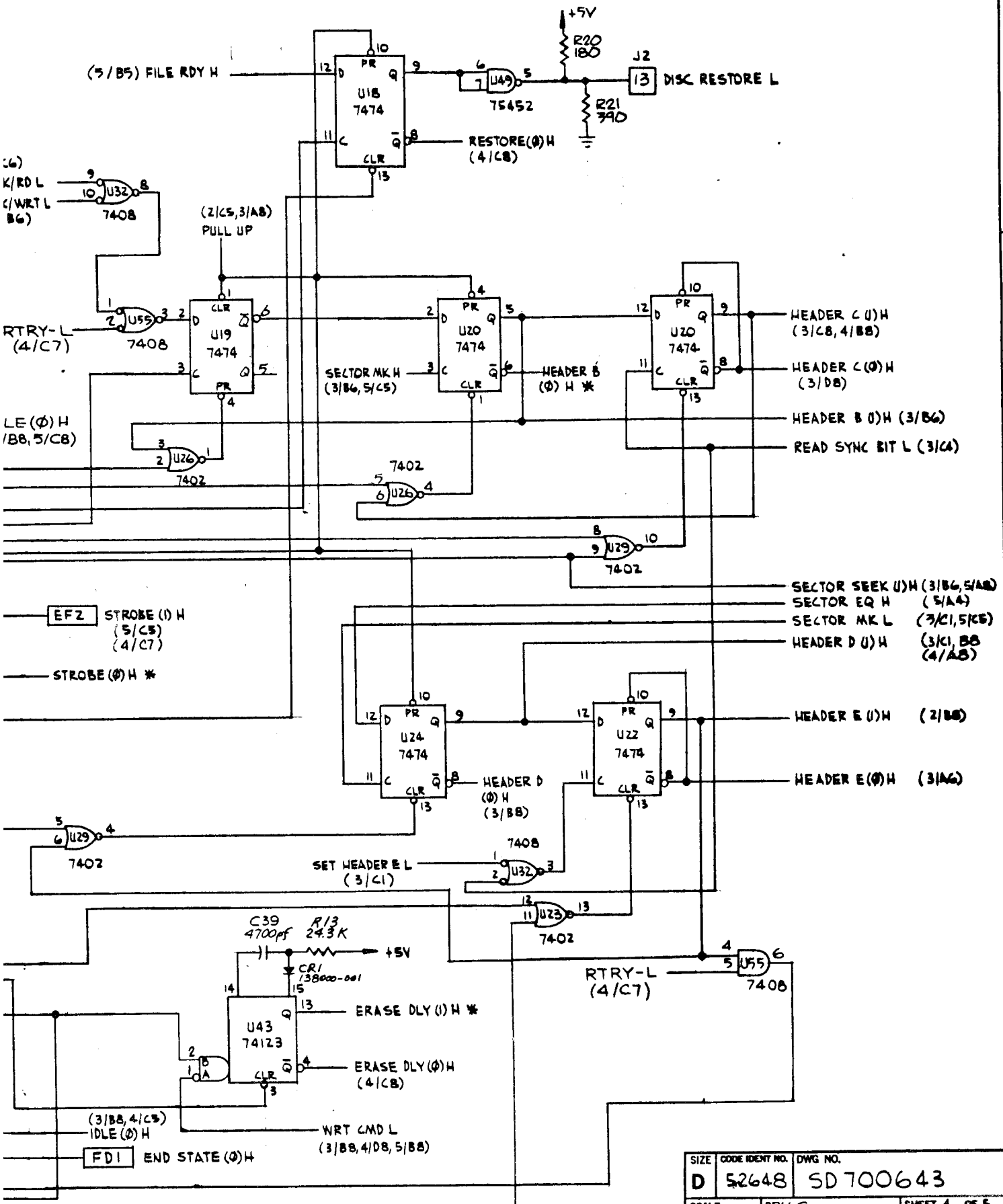
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SD700643

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ZONE		LTR		DESCRIPTION	DATE	APPROVED
				SEE SHEET 1		

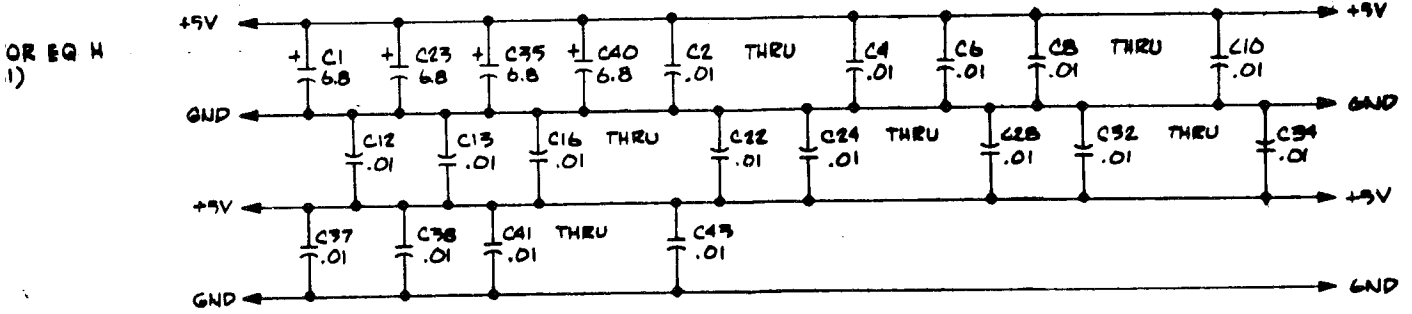
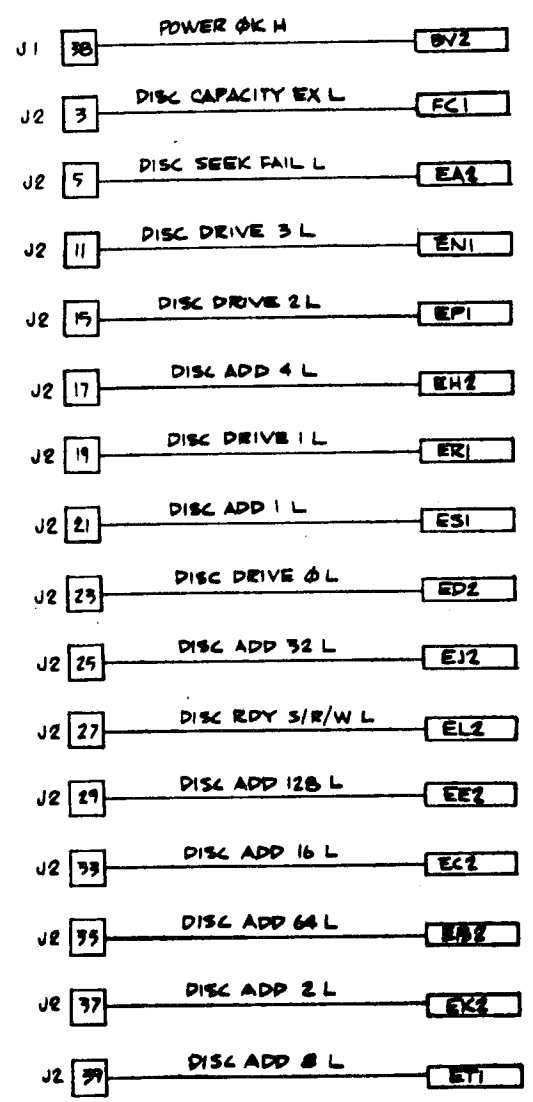
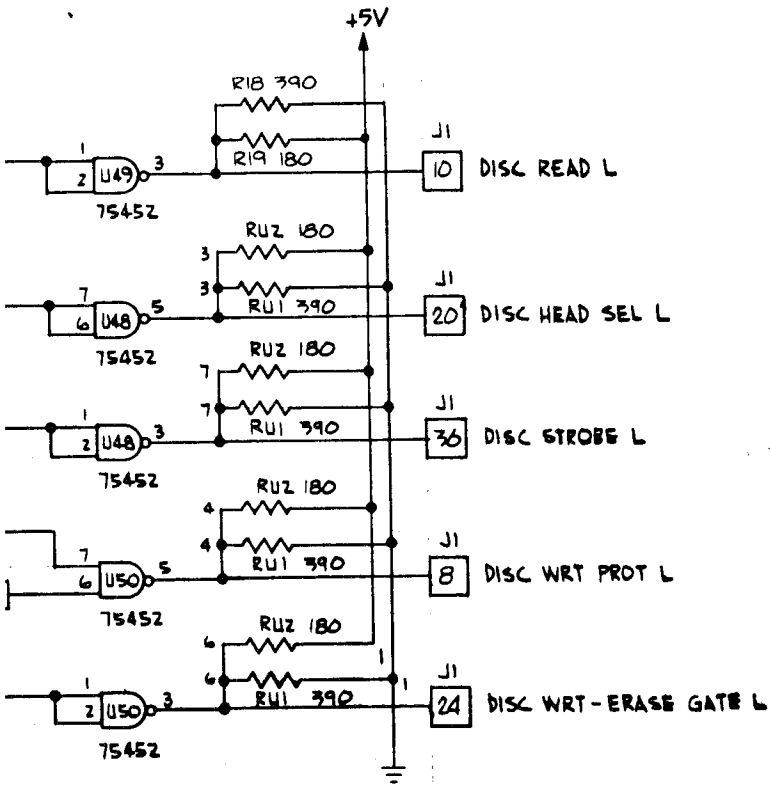


SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700643
SCALE: -	REV: C	SHEET 4 OF 5
		DISTR NO.

D
C
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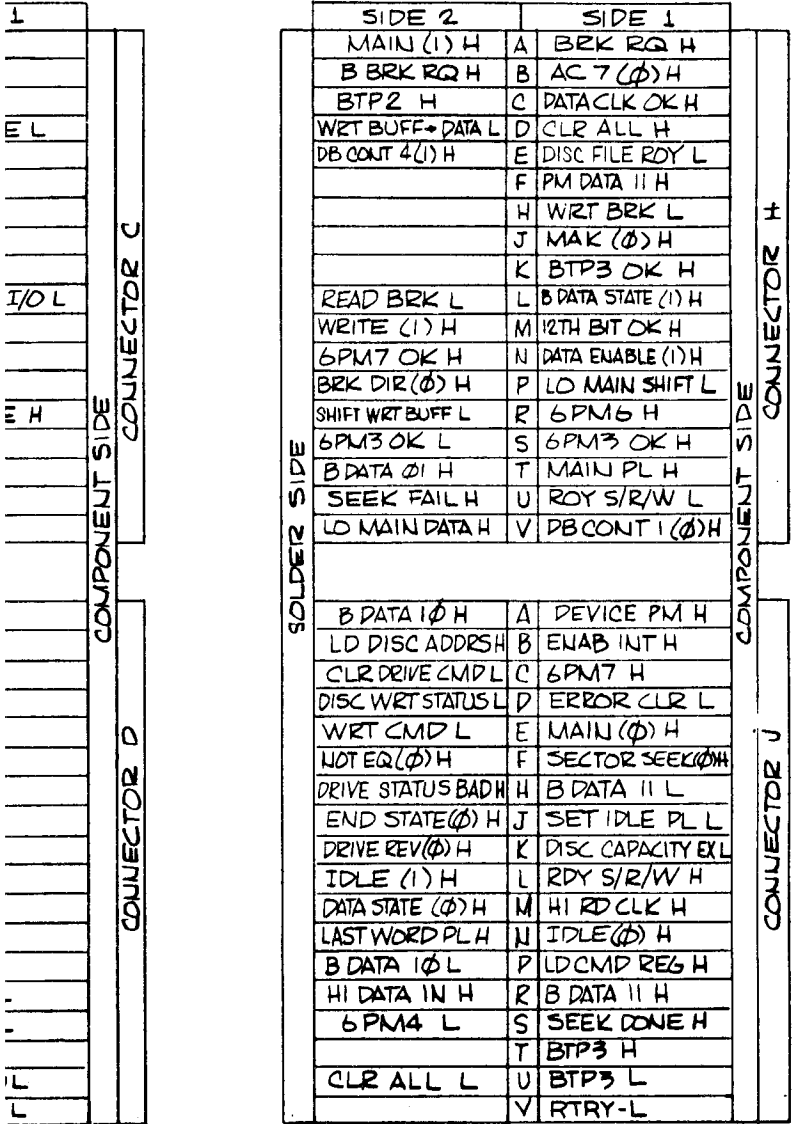
SD700643

ZONE		LTR		REVISIONS	DATE	APPROVED
				DESCRIPTION		
				SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD 700643
SHEET: -	REV: C	SHEET 5 OF 5
DISTR NO.		

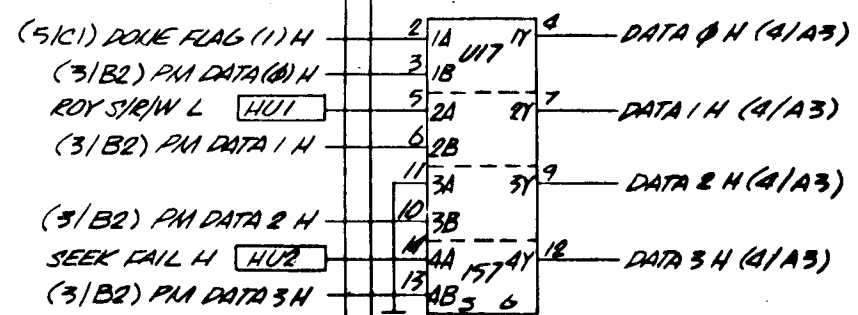
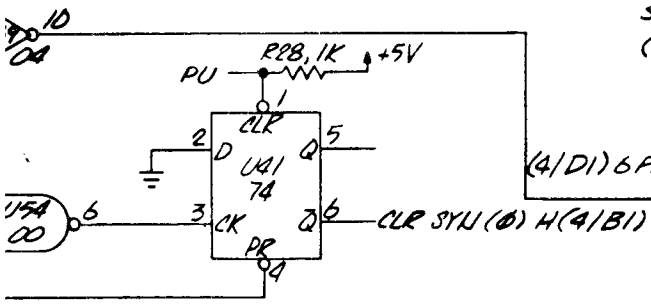
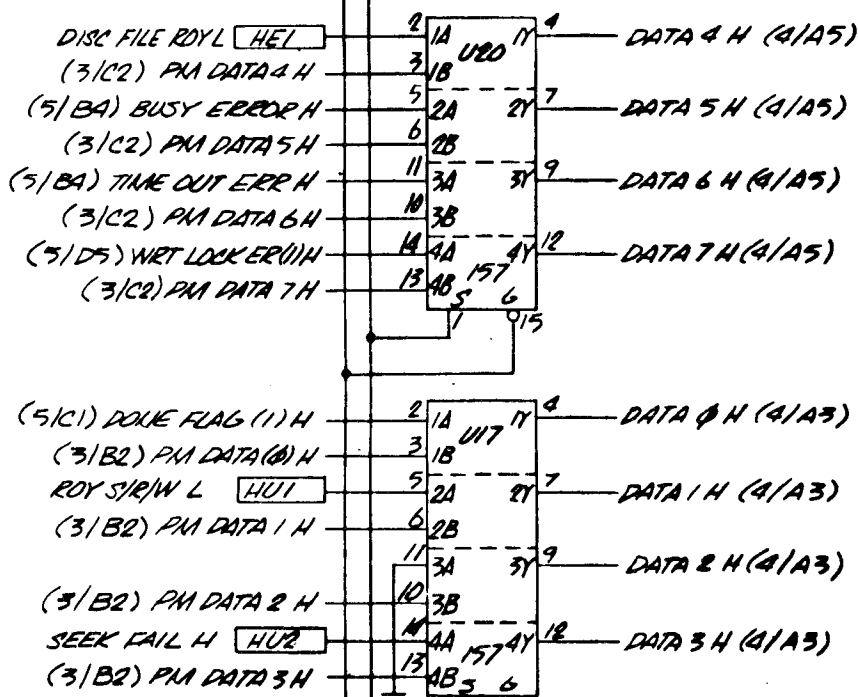
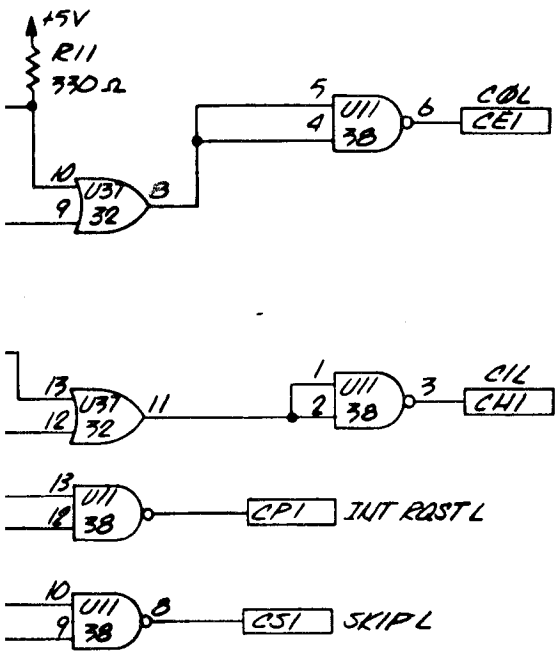
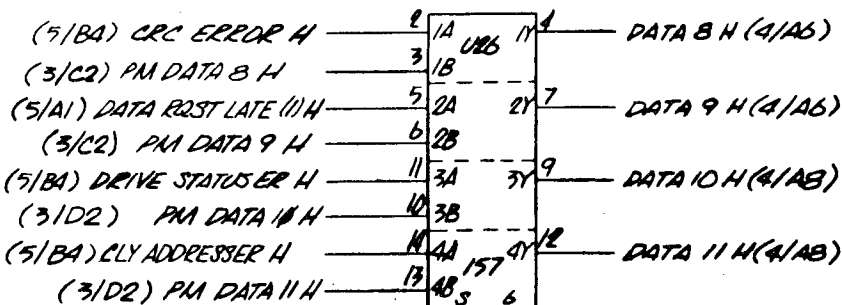
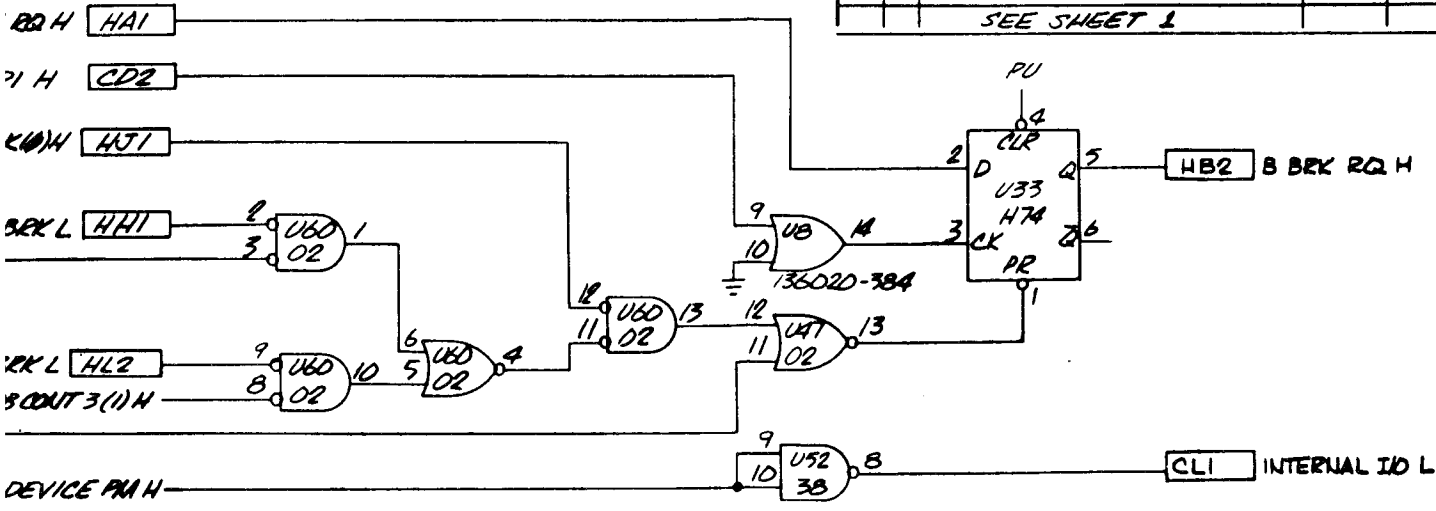
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-		REL TO PROD PER ERO 500686	12-9-75	DM
A		INCORP EO 1166	2-27-76	DM
B		INCORPORATED EO 1215	6-1-76	DM
C		INCORPORATED EO 1270	9-8-76	DM



PRODUCTION RELEASE

PART/ASSY NO. & QTY PER ASSY		NOTE: PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION / MATERIAL		SPEC/SOURCE	CODE IDENT NO.	FIND NO.
PART/ASSY REV LTR		DO NOT SCALE DRAWING		CONTRACT NO.		Plessey Memories Incorporated Santa Ana, California		
700645-100 PMA-DC1/B		<small>SCREW THREADS PER HANDBOOK H-38 COUNTERBORE AND SPOTFACE FILLET RADIUS TO BE 25% MAXIMUM REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .008" ROUGHNESS OF MACHINED SURFACES 125/1000 PER USAS B6.1 STANDARD HOLE TOLERANCE PER ANSI 3.2B TOLERANCES ON: JOE ± .005 JOOK ± .001 ANGLES ± 2° 30'</small>		DRAWN <i>GATES</i> 12-2-75 CHECK <i>D. Gates</i> 12-22-75 ENGR <i>D. Gates</i> 12/2/75 PROJ. ENGR PROD. DESIGN <i>J. Gates</i> 12/1/75		DWG TITLE <i>SCHEMATIC DIAGRAM DATA BUFFER AND STATUS PMA-DC1/B</i> SIZE D CODE IDENT NO. 52648 DWG NO. SD700645		
NEXT ASSY USED ON		APPLICATION		OTHER APPROVALS		SCALE: NONE REV: C		SHEET 1 OF 5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
SEE SHEET 1				



SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700645
SCALE: 1:1	REV C	SHEET 2 OF 5

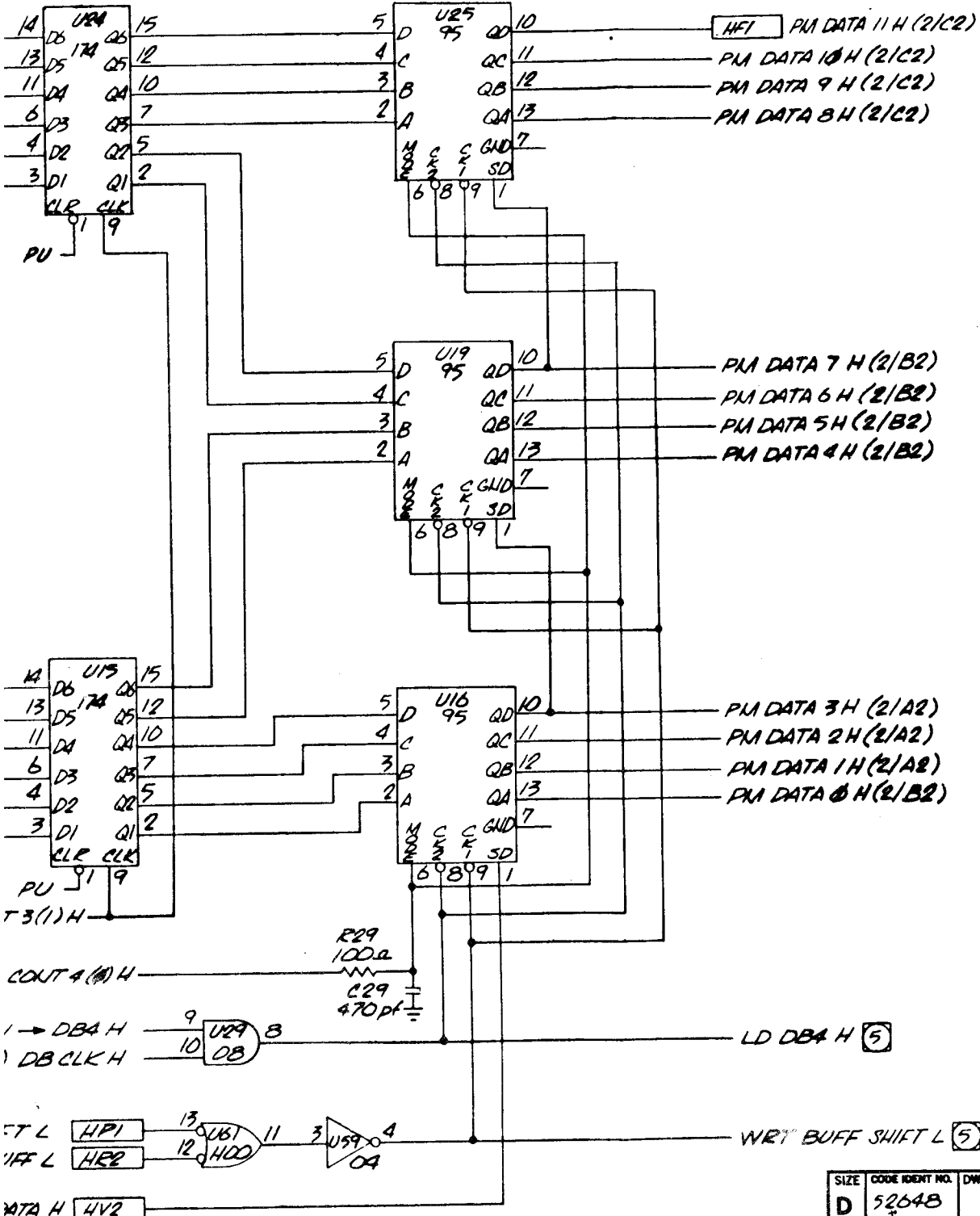
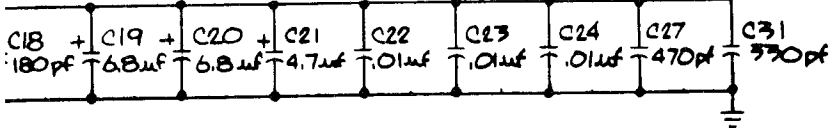
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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



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SD700645

SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD700645
SCALE: 1/101A REV C		SHEET 3 OF 5

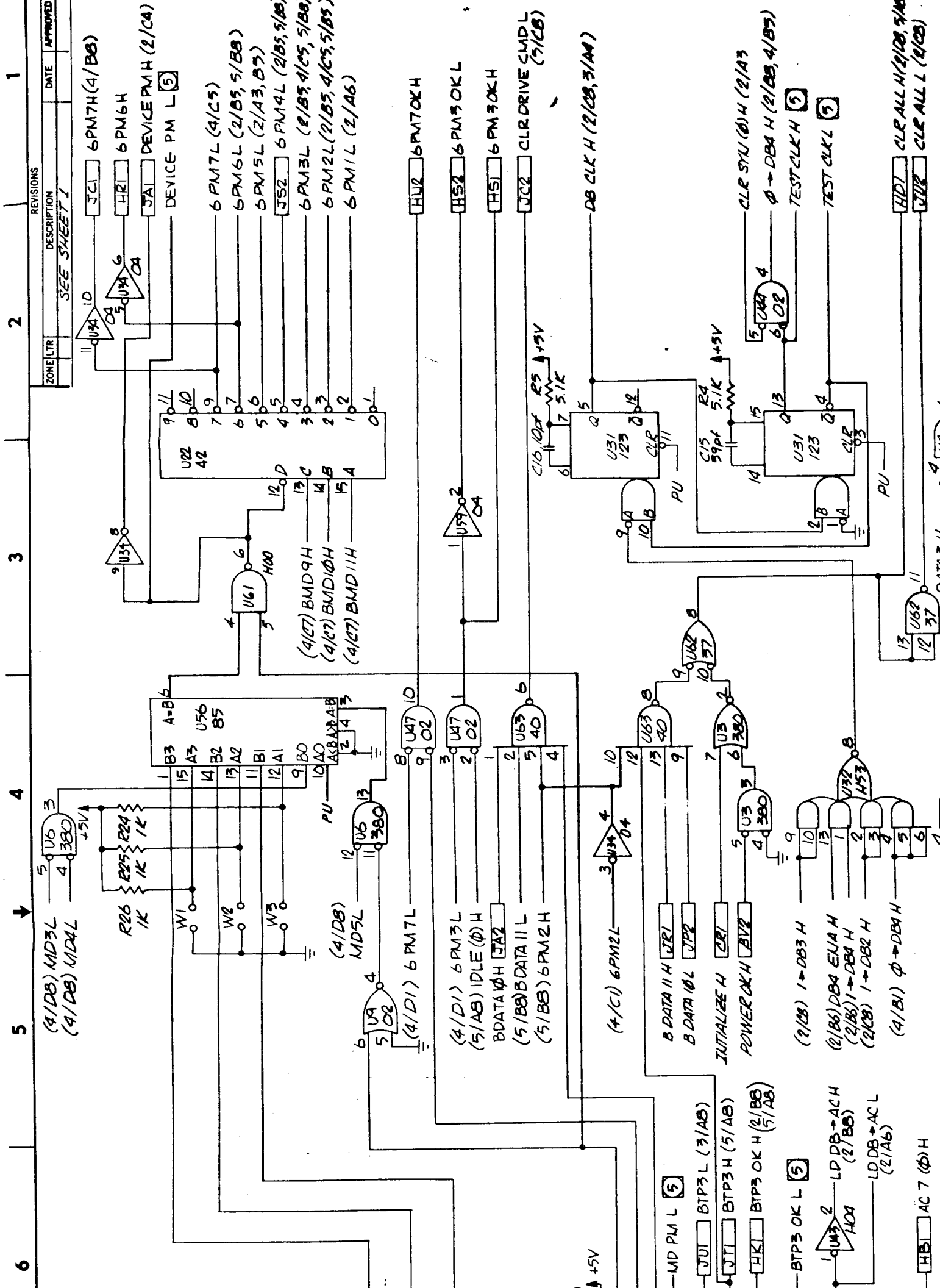
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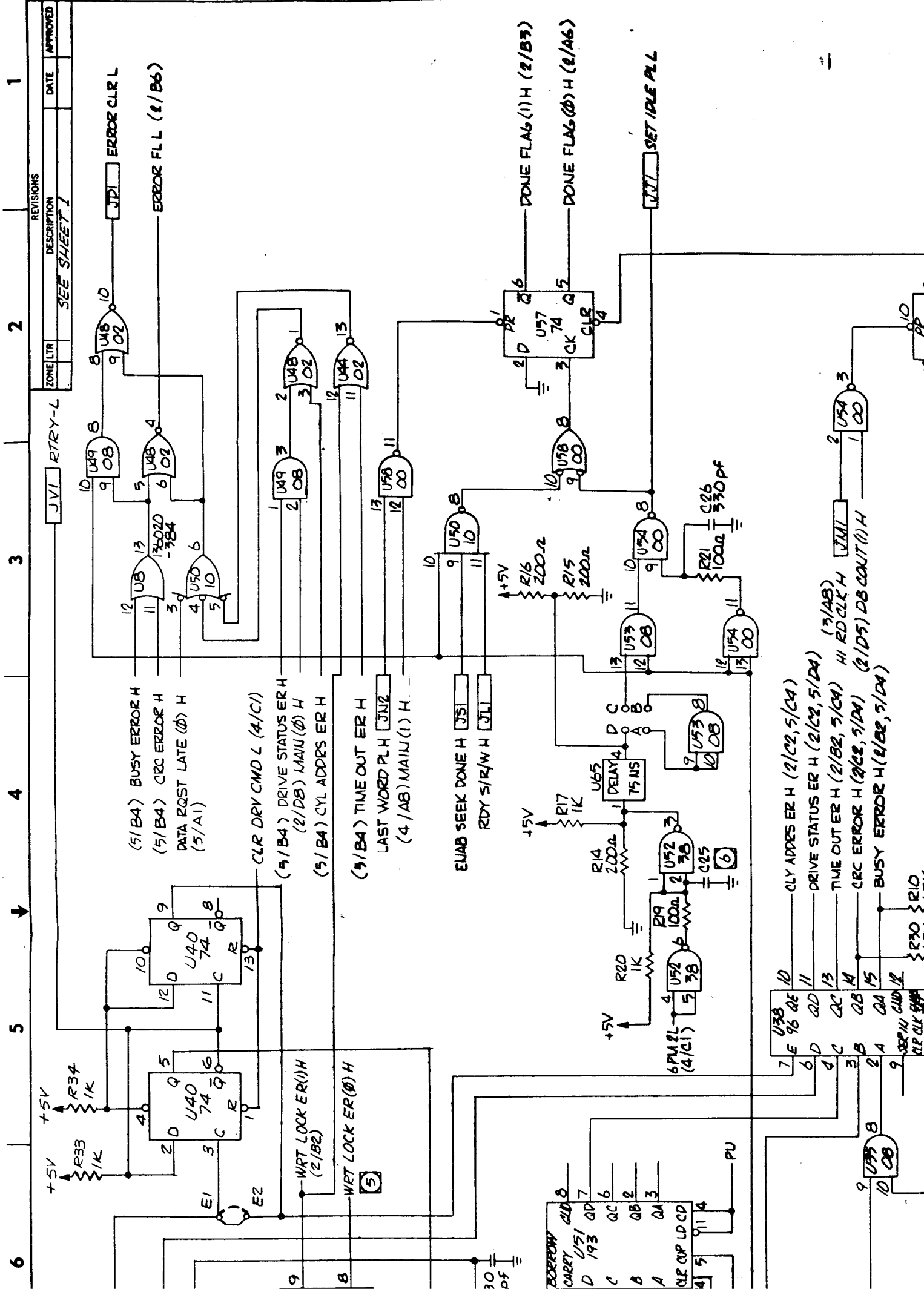
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DISTR NO.





REVISIONS	DATE	APPROVED
ZONE LTR	DESCRIPTION	SEE SHEET 1

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JVI RTRY-L

U49 08
U48 02
U50 10
U57 02
U58 00
U59 08
U60 08
U51 08
U52 08
U53 08
U54 08

(5/B4) BUSY ERROR H
(5/B4) CRC ERROR H
DATA RQST LATE (Ø) H
(5/A1)

CLR DRV CMD L (4/C1)
(5/B4) DRIVE STATUS ER H
(2/DB) MAIN (Ø) H
(5/B4) CYL ADDRES ER H
(5/B4) TIME OUT ER H
LAST WORD PL H JN2
(4/AB) MAIN (1) H

ENAB SEEK DONE H J51
RDY S/R/W H J51

JPI ERROR CLR L
ERROR FLL (2/B6)

U48 02
U49 08
U57 02
U58 00
U59 08
U60 08

(3/AB) DONE FLAG (1) H (2/B3)
(3/AB) DONE FLAG (Ø) H (2/A6)
SET IDLE PULL J57

U53 08
U54 08
U59 08
U60 08

U53 08
U54 08

JVI JN1

U53 08
U54 08
U59 08
U60 08

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U53 08
U54 08

U53 08
U54 08

JN2

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JN3

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JN4

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JN5

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U54 08

JN6

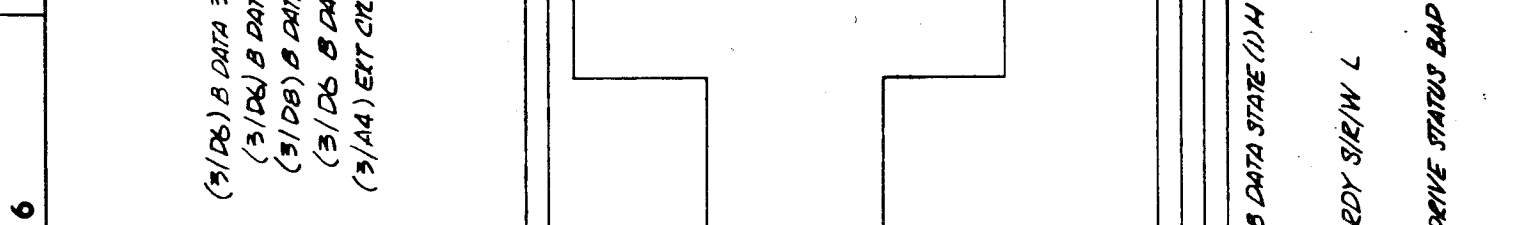
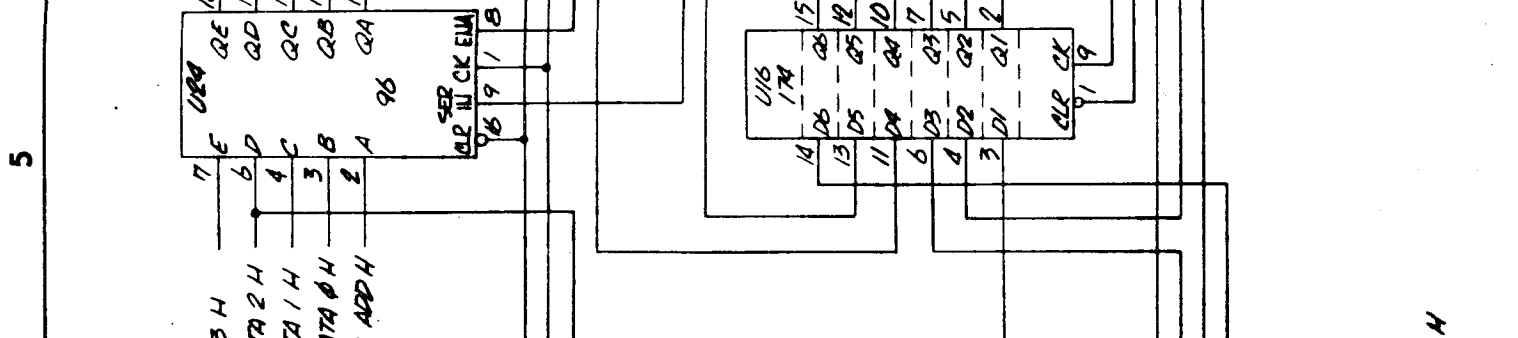
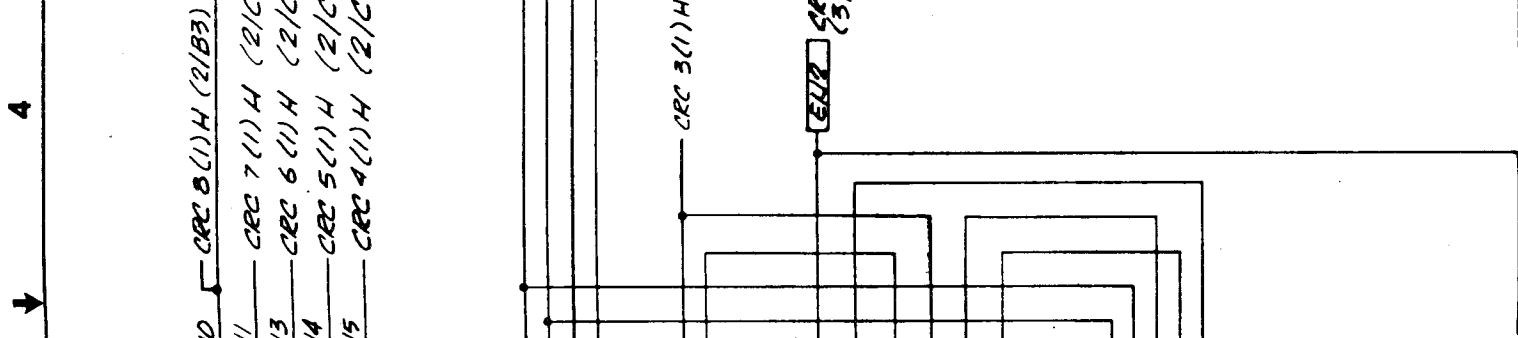
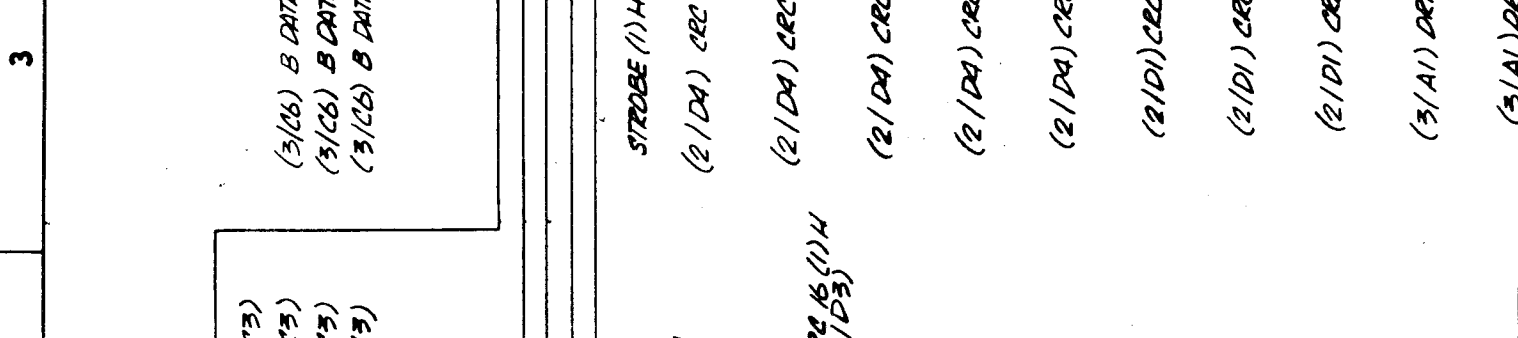
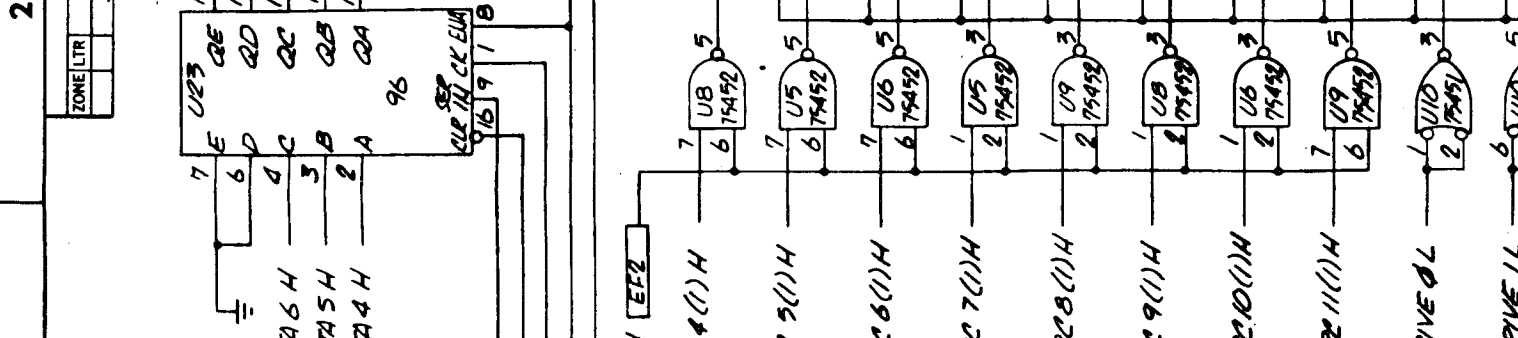
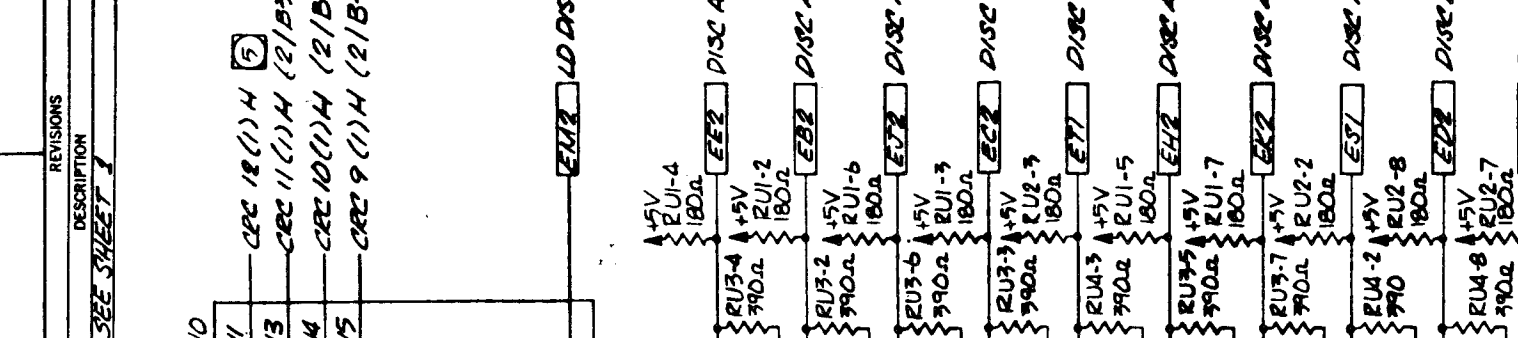
U53 08
U54 08

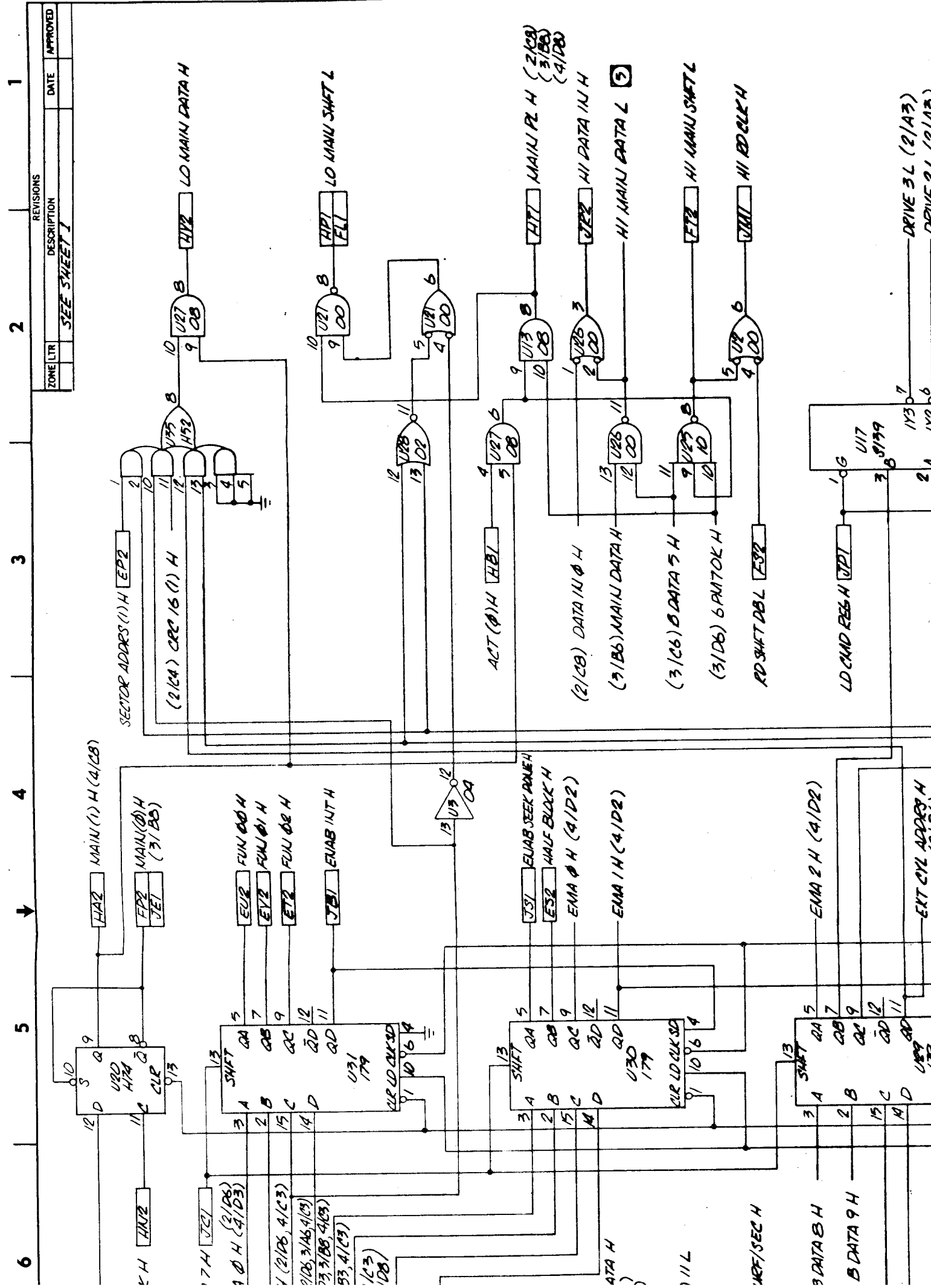
U53 08
U54 08

U53 08
U54 08

U53 08
U54 08

30 pf
+5V
-15V
R33 1K
R34 1K
R16 200Ω
R17 1K
R14 200Ω
R19 100Ω
R20 1K
R21 100Ω
R15 200Ω
R22 300pf
C25
C26
6P1A2L (4/C1)
7402
7400
7401
7404
7408
7409
7410
7412
7413
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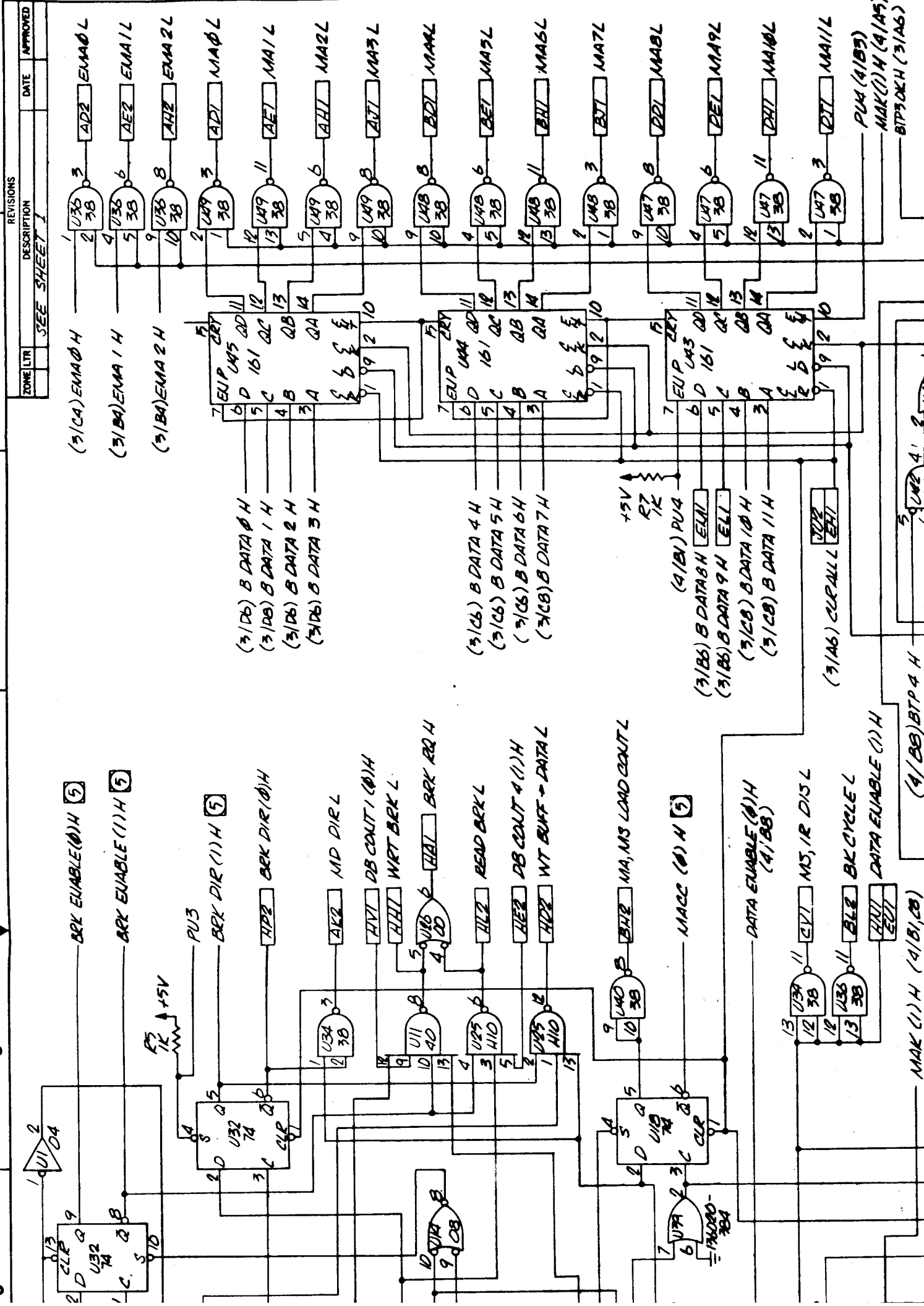




ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

6 5 4 3 2 1

DRIVE 3 L (2/A3)
DRIVE 2 L (2/A3)



REVISIONS		DATE	APPROVED
ZONE LTR	DESCRIPTION		
	SEE SHEET 1		