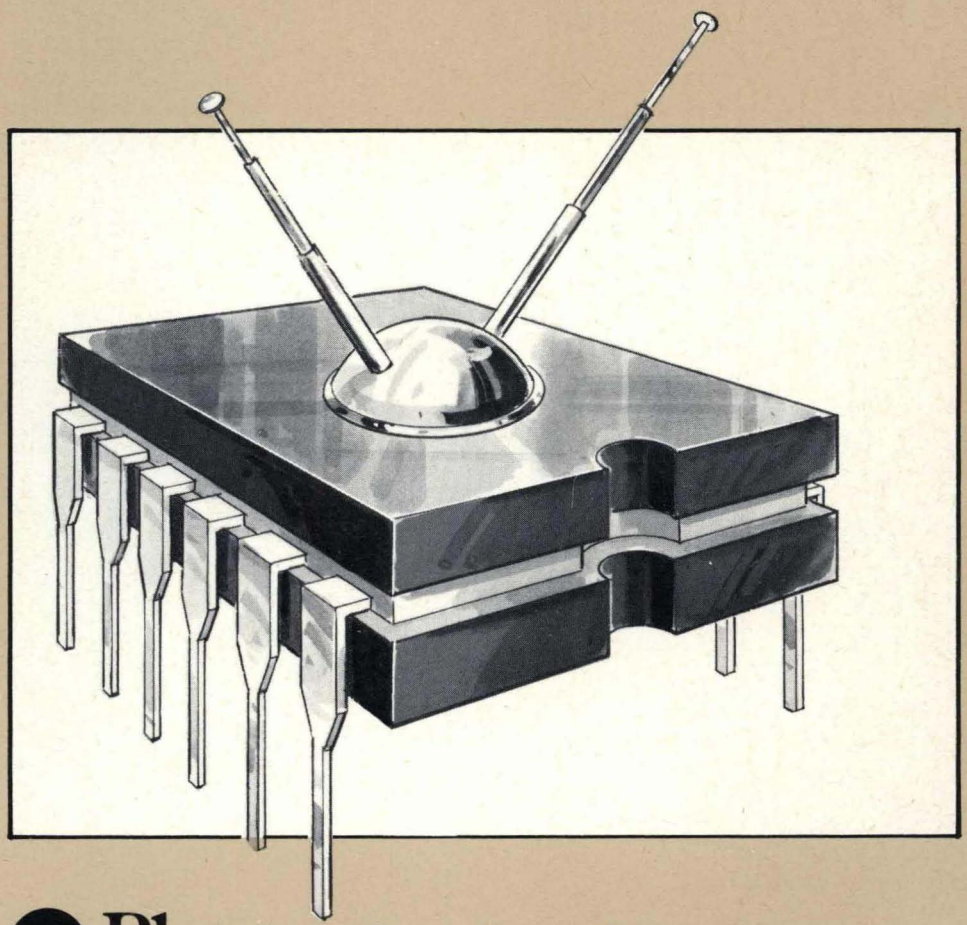
Television IC Handbook



Plessey Semiconductors

Television IC Handbook

$3.50

PLESSEY Semiconductors

TELEVISION IC HANDBOOK

APRIL 1981

Plessey Semiconductors
1641 Kaiser Avenue
Irvine, CA. 92714

$3.50

PSI 1775

Contents

1. PRODUCT RANGE INFORMATION

Building Block IC's

Plessey integrated circuits are on the leading edge of technology without pushing the ragged edge of capability.

We developed the first 2 GHz counter. And a family of prescalers and controllers for your TV, radio and instrumentation frequency synthesizers.

We have a monolithic 1 GHz amplifier. And a complete array of complex integrated function blocks for radar signal processing and radio communications.

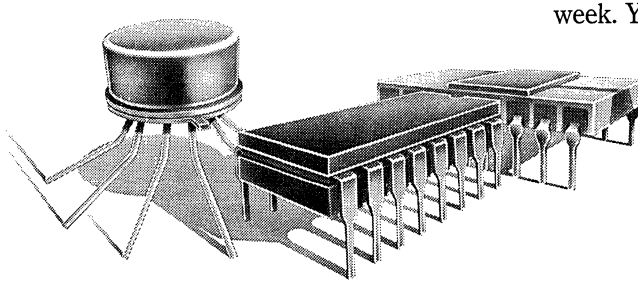
We can supply data conversion devices with propagation delays of just 2½ nanoseconds.

And a range of MNOS logic that stores data for a year when you remove the power, yet uses only standard supplies and is fully TTL/CMOS-compatible.

To develop this edge, we developed our own processes, both bipolar and MOS. The processes were designed for quality and repeatability, then applied to our high volume lines. Most of our IC's are available screened to MIL-STD-883B, and our quality levels exceed the most stringent military, TV and automotive requirements.

Millions of Plessey complex function building block IC's are being used in TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.

Our global scope of operations, our high volume manufacturing facilities, our proprietary processes ensure that we will continue to deliver state-of-the-art technology and reliability in IC devices at the appropriate prices and in the required volumes. Day after day. Week after week. Year after year.



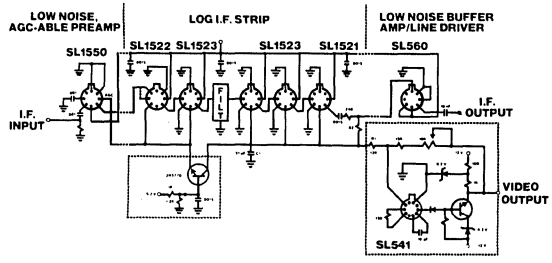
Plessey Semiconductors

1641 Kaiser Avenue, Irvine, CA 92714. (714) 540-9979

Radar Signal Processing

Since the performance of a radar receiver is critically dependent on the performance of its I.F. strip, we offer a range of "building block" IC's that can be used in systems with different performance requirements and configurations.

The logarithmic I.F. strip shown is an example of a low cost, high performance strip fabricated with Plessey IC's. It uses only five devices and a single interstage filter to achieve a logging range of 90 dB, ±1 dB accuracy, −90 dBm tangential sensitivity and a video rise time of 20 ns or less.



Three other Plessey IC's complete the system simply and economically. The AGC-able SL1550 on the front end improves noise figure, dynamic range and sensitivity. The SL541 lets you vary video output levels, with on-chip compensation making it easy to use. And the SL560 is a "gain block" that replaces your hybrid and discrete amplifiers, usually with no external components.

Another advanced system function block is the Plessey SL531 True Log Amplifier. A 6-stage log strip requires a minimum of external components (one capacitor, one resistor per stage), yet has a band-width of 500 MHz, a dynamic range of 70 dB and has a phase shift of only ±3° over its entire range. As with most of our other devices, it operates over the full MIL-temp range and is available screened to MIL-STD-883.

The chart summarizes our Radar Signal Processing IC's. Whether you're working with radar and ECM, weapons control or navigation and guidance systems, our IC's are a simpler, less expensive, more flexible alternative to whatever you're using now for any I.F. strip up to 160 MHz.

For more details, please use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

PLESSEY IC'S FOR RADAR I.F.'S

Wideband Amplifiers for Successive Detection Log Strips

SL521	30 to 60 MHz center frequency, 12 dB gain.
SL523	Dual SL521 (series).
SL1521	60 to 120 MHz center frequency, 12 dB gain.
SL1522	Dual SL1521 (parallel).
SL1523	Dual SL1521 (series).

Low Phase Shift Amplifiers

SL531	True log I.F. amplifier, 10-200 MHz, ±0.5°/10 dB max phase shift.
SL532	400 MHz bandwidth limiting amplifier, 1° phase shift max. when overdriven 12 dB.

Linear Amplifiers

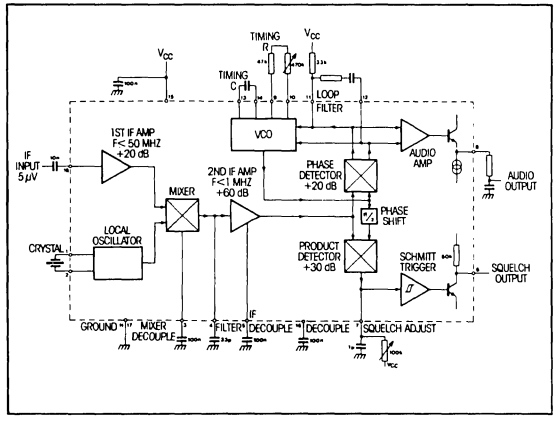
SL550	125 MHz bandwidth, 40 dB gain, 25 dB swept gain control range, 1.8 dB noise figure, interfaces to microwave mixers.
SL1550	320 MHz bandwidth version of SL550.
SL560	300 MHz bandwidth, 10 to 40 dB gain, 1.8 dB noise figure drives 50 ohm loads, low power consumption.

Video Amplifiers and Detectors

SL510	Detector (DC to 100 MHz) and video amplifier (DC to 24 MHz) may be used separately, 11 dB incremental gain 28 dB dynamic range.
SL511	Similar to SL510 with DC to 14 MHz video amplifier, 16 dB incremental gain.
SL541	High speed op amp configuration, 175 V/μs slew rate 50 ns settling time, stable 70 dB gain, 50 ns recovery from overload.

Radio Communications

Our comprehensive line of radio system function blocks is cutting costs, increasing reliability and reducing the size of systems in applications that range from commercial communications to military manpack radios.



Using our bipolar Process I, the Plessey SL600 Series (hermetic) and SL1600 Series (plastic DIP) feature a high degree of integration, low power consumption and exceptional system design flexibility for I.F.'s up to 10.7 MHz.

Our SL6000 Series uses our bipolar Process III to extend our building block concept even further. Devices all feature advanced circuit design techniques that permit higher levels of integration, lower power consumption and exceptional performance.

Typical is our SL6600, a monolithic IC that contains a complete IF amplifier, detector, phase locked loop and squelch control. Power consumption is a meager 1.5 mA at 6 V, S/N ratio is 50 dB, dynamic range is 120 dB and THD is just 1.3% for 5 kHz peak deviation. The SL6600 can be used at I.F. frequencies up to 50 MHz, with deviations up to 10 kHz.

If any of the Plessey devices appear interesting, use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK. The Handbook includes full details on our integrated circuits, along with a number of applications circuits and design tips that will help you get the maximum system benefits from Plessey products.

Or if your need is more urgent, contact your nearest Plessey Semiconductors representative.

PLESSEY RADIO IC'S

Amplifiers		
SL610	SL1610	140 MHz bandwidth, 20 dB gain, 50 dB AGC range, low 4 dB N.F., low distortion.
SL611	SL1611	100 MHz bandwidth, 26 dB gain, sim. to SL610.
SL612	SL1612	15 MHz bandwidth, 34 dB gain, 70 dB AGC range, 20 mW power consumption.
SL613		145 MHz bandwidth, 12 dB gain, limiting amp/detector.
Mixers		
SL640	SL1640	Double balanced modulator eliminates diode rings up to 75 MHz, standby power 75 mW typical.
Detectors and AGC Generators		
SL620	SL1620	AGC with VOGAD (Voice Operated Gain Adjusting Device).
SL621	SL1621	AGC from detected audio.
SL623	SL1623	AM SSB detector and AGC from carrier.
	SL1625	AM detector and AGC from carrier.
SL624		AM/FM/SSB/CW detector with audio amplifier.
Audio Amplifiers		
SL622		Microphone amp. with VOGAD and sidetone amp.
SL630	SL1630	250 mW microphone/headphone amplifier.
I.F. Amplifiers/Detectors		
SL6600		FM double conversions with PLL detector.
SL6640		FM single conversion, audio stage (10.7 MHz).
SL6650		FM single conversion (10.7 MHz).
SL6690		FM single conversion, low power for pagers (455 kHz).
SL6700		AM double conversion.
Audio Amplifiers		
SL6270		Microphone amplifier with AGC.
SL6290	SL6270	with speech clipper, buffer and relay driver.
SL6310		Switchable audio amplifier (400 mW/9V/8 ohms).
SL6440		High-level mixer.

R. F. Hybrids

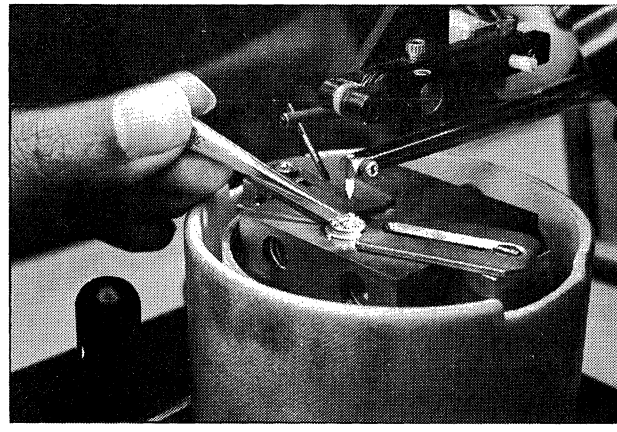
To enhance your systems even further, we have established an R.F. hybrid manufacturing facility in our Irvine, California, U.S.A. headquarters.

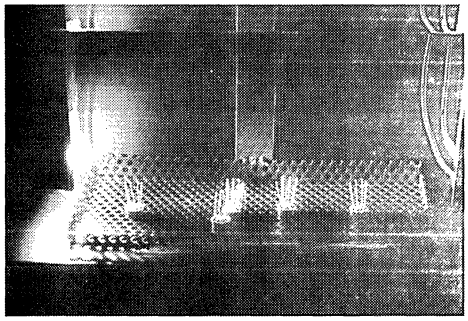
For small production quantities or extremely complex functions, our hybrid capabilities can save you time and money while improving your system performance, reducing system size and increasing system reliability. We can help with your I.F. strips, instrumentation front ends, synthesizer subsystems, high speed A-to-D and D-to-A converters and other complex high-frequency functions.

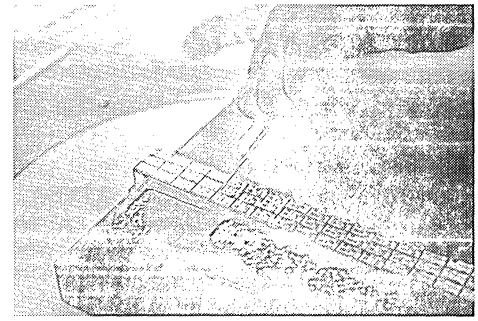
They can be fabricated to MIL-STD-883 using thick and thin film techniques, using our own integrated circuits in combination with discrete transistors, diodes and other components.

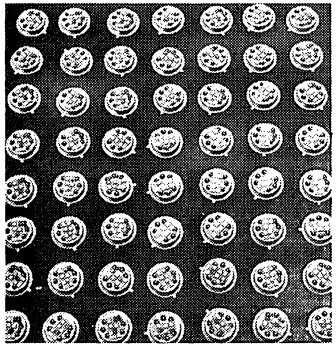
Our IC functions represent the state-of-the-art in high frequency integration, with f_t's as high as 5 GHz. The chips are backed by an in-depth in-house systems knowledge that encompasses radar, radio communications, telecommunications analog and digital conversion, frequency synthesis and a broad range of applications experience.

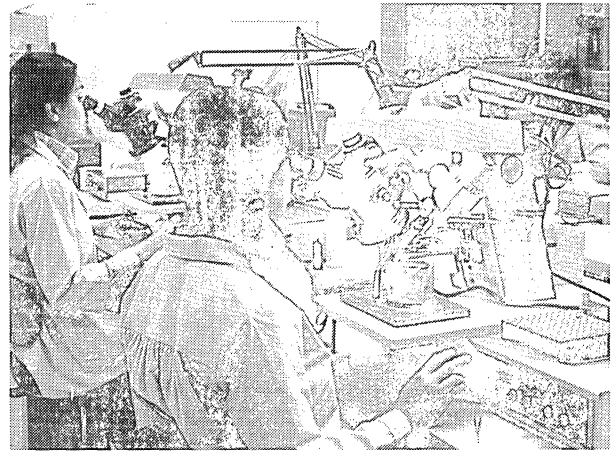
We can work to your prints, or we can design a full system based on your "black box" specifications. For more information, please contact: Plessey Semiconductors, 1641 Kaiser Avenue, Irvine CA 92714, (714) 540-9979.

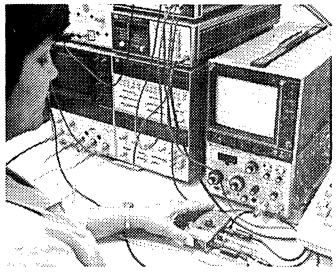


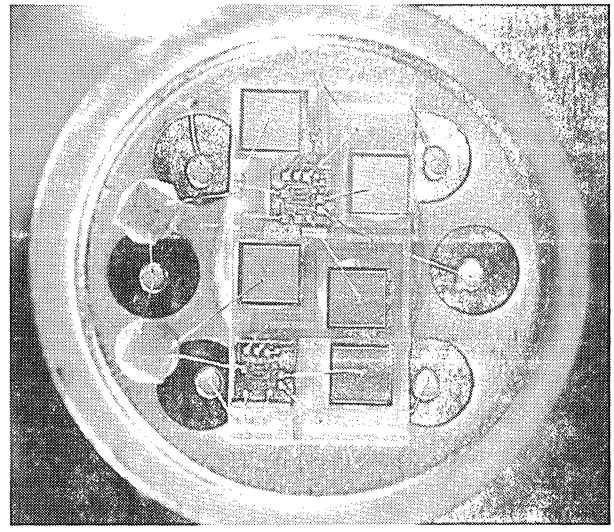












Frequency Synthesis

Plessey's IC's offer a quick and easy way to lower synthesizer costs while increasing loop response and channel spacing all the way from dc through the HF, VHF, UHF, TACAN and satellite communications bands.

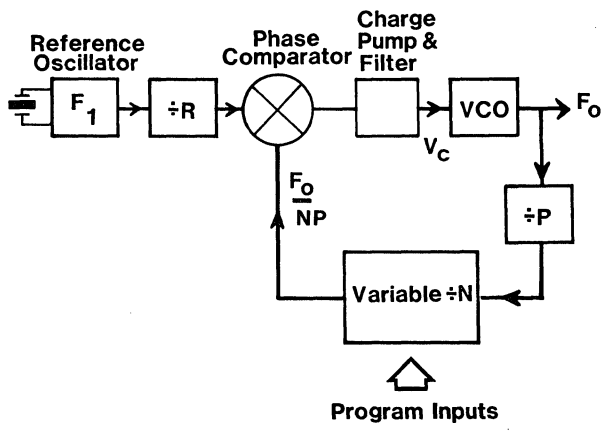
Our single-modulus prescalers operate at frequencies all the way up to 1.8 GHz. They feature self-biasing clock inputs, TTL/CMOS-compatibility and all guaranteed to operate to at least the frequencies shown, most of them over the temperature range from −55°C to +125°C.

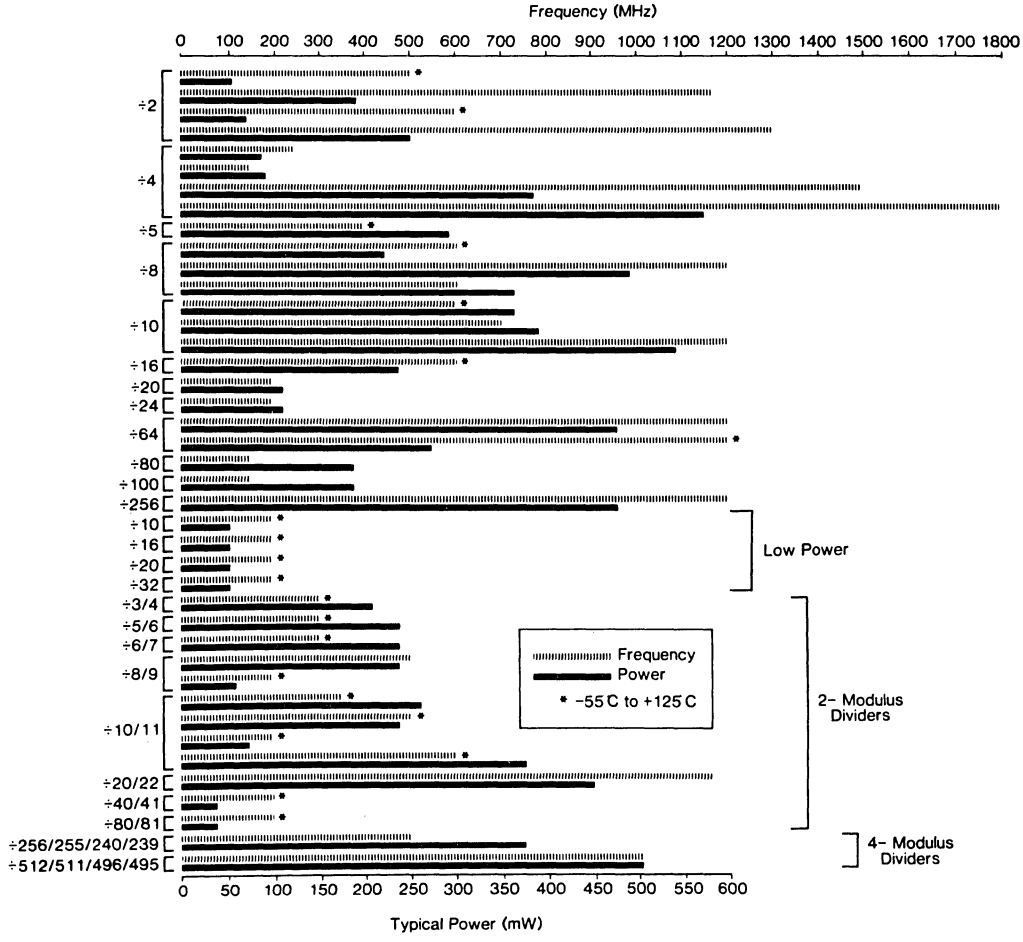
Our 2-modulus and 4-modulus dividers expand your system flexibility and allow even tighter channel spacing. All of them provide low power consumption, low propagation delay and ECL-compatibility.

To simplify your systems even further, we also offer highly integrated control chips. Our NJ8811, for example, includes a crystal oscillator maintaining circuit, a programmable reference divider, a programmable divider to control the four-modulus prescaler and a high performance phase/frequency comparator so that you can phase lock your synthesizer to a crystal with none of the usual headaches and hassles.

We've put together a FREQUENCY SYNTHESIZER IC HANDBOOK that details all of the Plessey IC's and includes a number of applications circuits, practical examples of how Plessey integrated circuits can simplify your designs and improve system performance.

For your copy of the Handbook, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.




Frequency (MHz)
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800
÷2
÷4
÷5
÷8
÷10
÷16
÷20
÷24
÷64
÷80
÷100
÷256
÷10
÷16
÷20
÷32
÷3/4
÷5/6
÷6/7
÷8/9
÷10/11
÷20/22
÷40/41
÷80/81
÷256/255/240/239
÷512/511/496/495
Low Power
2- Modulus Dividers
4- Modulus Dividers
Frequency
Power
* -55°C to +125°C
0 50 100 150 200 250 300 350 400 450 500 550 600
Typical Power (mW)

Telecommunications

Plessey functional building block IC's are exceptionally versatile. Designed from a systems standpoint, they reduce complexity and lower costs while increasing the performance of telecommunications systems.

Our SL600 Modulator/Phase Locked Loops are used in waveform generators and in AM, PAM, FM, FSK, PSK, PWM, tone burst and Delta modulators.

Our SL1000 Series amplifiers meet the most stringent demands of telephone transmission equipment.

Our transistor arrays with up to five electrically and thermally matched transistors on a chip are ideal for discrete and hybrid amplifiers and mixers. In addition to standard second-source devices that plug directly into your designs, we have a number of devices designed for your low noise and ultra-high frequency applications.

The Plessey TELECOMMUNICATIONS IC HANDBOOK contains complete information on all of these devices, as well as application notes, to help you get the most out of them. To get your copy, please use the postage-paid reply card at the back of this book or call your nearest Plessey Semiconductors representative.

Telecommunications Devices

MJ1440	HDB3 encoder/decoder
MJ1444	PCM synchronizing word generator
MJ1445	PCM synchronizing word receiver
MJ1471	HDB3/AMI encoder/decoder

Data Communications MOS

MP3812	32 x 8-bit FIFO memory, serial or parallel, up to 0.25 MHz data rates, easily stacked.
MJ2841	64 x 4-bit FIFO memory, 5 MHz clock rate.

Modulator/Phase Locked Loops

SL650	Modulator/PLL for AM, PAM, SCAM, FM, FSK, PSK, tone-burst and Delta modulation; VFO variable 100:1.
SL651	Similar to SL650 without auxiliary amplifier.
SL652	Similar to SL650, low cost.

Telephone Circuits

SL1001	Modulator/demodulator, 50 dB carrier and signal suppression, −112 dBm noise level.
SL1021	3 MHz channel amplifier, stable remote gain control.
SL1025	FDM balanced modulator, 50 dB carrier and signal suppression, 5 dB conversion gain.
SL1030	200 MHz wideband amplifier, programmable gain, low noise.

Transistor Arrays

PLESSEY PART NO.	2ND-SOURCE PART NO.	PLESSEY PART NO.	2ND-SOURCE PART NO.
SL3081	CA3081	SL3051	CA3951
SL3082	CA3082	SL355	NONE
SL3083	CA3083	TBA673	TBA673
SL3183	CA3183	SL1495	CA1495L
SL3146	CA3146	SL1496	MC1496G
SL3093	CA3093	SL1496	MC1496L
SL3018	CA3018	SL1595	MC1595L
SL3018A	CA3018A	SL1596	MC1596G
SL3118A	CA3118A	SL1596	MC1596L
SL3118	CA3118	SL3054	CA3054
SL3050	CA3050	SL3086	CA3086

SL360	High frequency matched pair, f_t=2.5 GHz.
SL363	Low noise matched pair, f_t=2.2 GHz.
SL2363/4	5GHz dual long-tailed pair.
SL3145	Five transistor array, f_t=2.5 GHz.

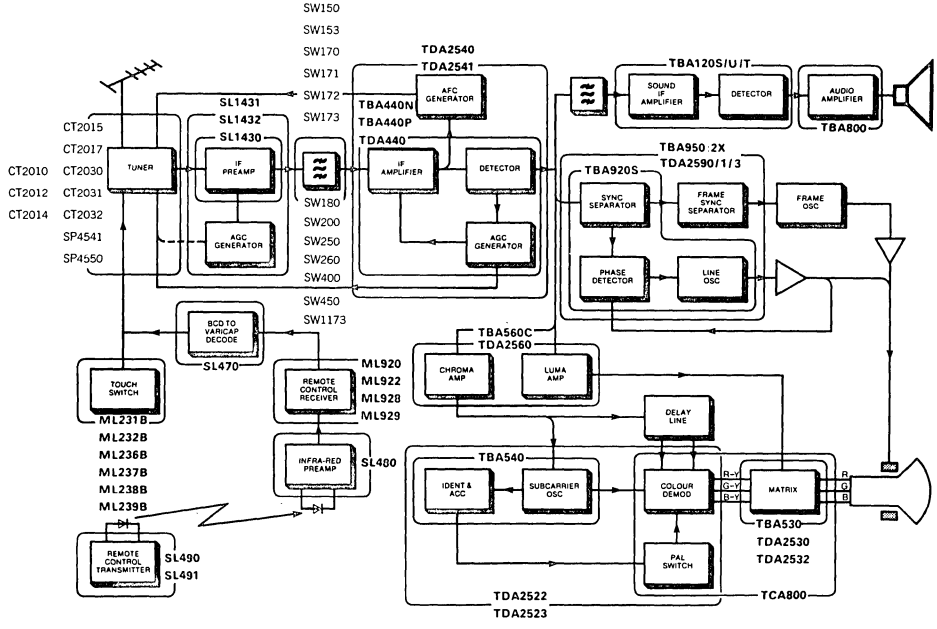
Television IC's

Plessey integrated circuits are in millions of homes, in television sets around the world.

Economical and reliable, our devices cover the range from remote controls to touch tuners to frequency synthesizers, as well as a range of second-source devices for the IF color processing and line oscillators.

For the 1980's, we have introduced the Plessey KEY System, designed for maximum flexibility, simplicity and ease of manufacture. The KEY System frequency synthesizer offers accurate, high stability frequency selection, channel and program identification, and the very finest digital fine tuning. It can be configured to receive up to four completely different standards (PAL, SECAM, SECAMF, and NTSC) in a single TV set. It has 100 channel capability per standard, and includes a 32-program non-volatile memory that contains channel, fine tuning and standards information. And it can be interfaced to a Plessey or other microprocessor for games, Teletext or similar applications.

Complete data on all our television devices has been assembled in our TELEVISION IC HANDBOOK, along with application notes to make them even easier to use. Please use the postage-paid reply card at the back of this book to order your copy, or simply contact your nearest Plessey Semiconductors representative.



ALL TBA, TCA, TDA DEVICES ARE SECOND-SOURCED.

ECL III Logic and Data Conversion

As radar and communications systems become faster and more complex, the need arises for digital processing. We have developed a family of functions with speeds unequalled anywhere.

Part of our family is a range of ECL III logic that is a direct plug-in replacement for MECL logic, including low impedance as well as high impedance devices. We extended the range by adding functions with lower delays and much higher operating speeds. Our SP16F60, for example, is the world's fastest dual 4-input OR/NOR gate, with a switching speed of just 500 picoseconds. Devices can also be selected for certain specifications (such as threshold voltage or slew rate on our SP1650/1, toggle rates or delays on our SP1670) to handle your most demanding applications. We've also developed a family of high speed comparators and circuits for ultra-high speed A-to-D converters. Our latching SP9750 high speed comparator features a maximum settling time of 2 ns, a propagation delay of 3.5 ns and is capable of operating at rates up to 100 million samples per second.

Currently, our devices are being used in radar and video processing, nucleonics systems, transient recorders and secure speech transmission systems. We have compiled a number of application notes and details on the devices in our ECL III LOGIC AND DATA CONVERSION IC HANDBOOK. To get your copy, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.

HIGH SPEED ECL III LOGIC

SP1648	Voltage controlled oscillator
SP1650	Dual A/D comparator, Hi-Z
SP1651	Dual A/D comparator, Lo-Z
SP1658	Voltage controlled multivibrator
SP1660	Dual 4-I/P OR/NOR gate, Hi-Z
SP1661	Dual 4-I/P OR/NOR gate, Lo-Z
SP1662	Quad 2-I/P NOR gate, Hi-Z
SP1663	Quad 2-I/P NOR gate, Lo-Z
SP1664	Quad 2-I/P OR gate, Hi-Z
SP1665	Quad 2-I/P OR gate, Lo-Z
SP1666	Dual clocked R-S Flip-Flop, Hi-Z
SP1667	Dual clocked R-S Flip-Flop, Lo-Z
SP1668	Dual clock latch, Hi-Z
SP1669	Dual clock latch, Lo-Z
SP1670	Master-slave D Flip-Flop, Hi-Z
SP1671	Master-slave D Flip-Flop, Hi-Z
SP1672	Triple 2-I/P exclusive-OR gate, Hi-Z
SP1673	Triple 2-I/P exclusive-OR gate, Lo-Z
SP1674	Triple 2-I/P exclusive-NOR gate, Hi-Z
SP1675	Triple 2-I/P exclusive-NOR gate, Lo-Z
SP1692	Quad line receiver
SP16F60	Dual 4-I/P OR/NOR gate

HIGH SPEED DATA CONVERSION PRODUCTS

SP9680	High speed latched comparator.
SP9685	Ultra-fast comparator; 0.5 ns typical set-up time; typical 2.2 ns propagation delay; excellent CMR.
SP9687	Dual SP 9685.
SP9750	High speed latched comparator with precision current source, wired-OR decoding; 2 ns min. set-up time; 2.5 ns propagation delay.
SP9752	2-bit ADC expandable to 6-bit ADC; very fast 125 MHz clock.
SP9754	4-bit ADC expandable to 8-bit ADC; very fast 100 MHz clock.
SP9768	8-bit DAC; extremely fast; available 3rd quarter 1980.
SP9778	8-bit SAR; works with SP9768 to make a two-chip successive approximation ADC (20 MHz clock); available 4th quarter 1980.

MNOS Non-Volatile Logic

As semiconductors become more pervasive in military and commercial applications, the need for non-volatile data retention becomes more and more critical.

Plessey NOVOL MNOS devices answer that need, and will retain their data for at least a year (−40°C to +70°C) in the event of "power down" or a system crash.

Our devices all operate from standard MOS supplies and are fully compatible with your TTL/CMOS designs. The high voltages normally associated with electrically-alterable memories are generated on-chip to make system interface simpler and less expensive.

Plessey NOVOL devices provide a reliable, sensible alternative to CMOS with battery back-up or mechanical, electro-mechanical and magnetic devices. Applications include metering, security code storage, microprocessor back-up, elapsed time indicators, counters, latching relays and a variety of commercial, industrial and military systems.

For more information, contact your nearest Plessey Semiconductors representative, or use the postage-paid reply card at the back of this brochure to order your copy of the Plessey NOVOL literature package.

PLESSEY NOVOL MNOS

MN9102	4-bit Data Latch (+5V, −12V)
MN9105	4-Decade Up/Down Counter (+5V, −12V)
MN9106	6-Decade Up Counter (12V only)
MN9107	100-Hour Timer (12V only)
MN9108	10,000-Hour Timer (12V only)
MN9110	6-Decade Up Counter with Carry (12V only)
MN9210	64 x 4-Bit Memory
*	8 x 4-Bit Memory
*	6-Decade Up/Down Counter, BCD Output
*	6-Decade Up/Down Counter with Preset BCD Output

* COMING SOON

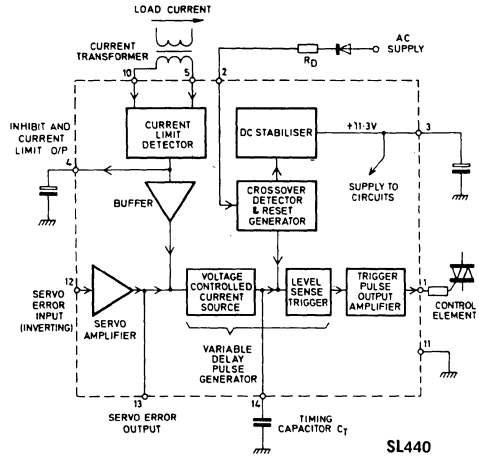
Power Control

Plessey power control devices are highly integrated not just to solve the problems, but to solve them at a lower cost than any other available method.

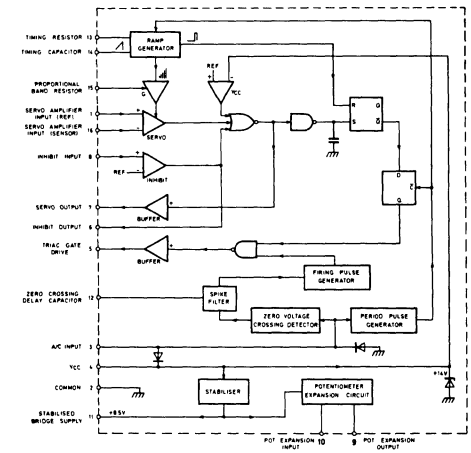
For timing, our devices use a pulse integration technique that eliminates the need for expensive electrolytic capacitors, thus increasing accuracy and repeatability while reducing costs. An integral supply voltage sensing circuit inhibits triac gate drive circuitry if the supply is dangerously low to prevent half-wave firing and firing without achieving complete bulk conduction. A zero-voltage spike filter prevents misfiring on noise inputs. Symmetrical control prevents the introduction of dc components onto the power lines.

Devices have been tailored for specific applications as indicated in the chart. For more information, please use the postage-paid reply card at the back of this book to order our POWER CONTROL IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

SL440	**Proportional phase control for motors, lamps and lower power, fast response heating.**
SL441	**Similar to SL440, with proportional temperature control and thermister malfunction sensing, for hairdryers, soldering irons and food warmers.**
SL442	**Switch mode power supply control, up to 40 kHz, integral oscillator, variable ratio space/mark pulses, soft-start, dynamic current limiting, OVP.**
SL443	**Similar to SL441 with manual power control, long timing periods for hot plates, electric blankets and traffic lights.**
SL444	**Similar to SL441 for 240V permanent magnet motor with thermal trip, current limit detector.**
SL445	**Proportional or On/Off control, temperature trip/ inhibit circuitry, LED and alarm drive facilities, for ovens, heaters, industrial temperature controllers.**
SL446	**On/Off servo loop temperature controller, low external component count, for water and panel heaters, refrigerators, irons.**
TBA1085	**Motor speed control**



SL440



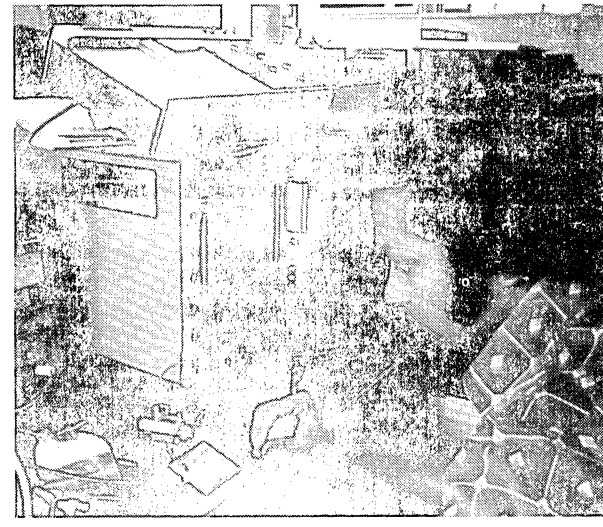
SL445

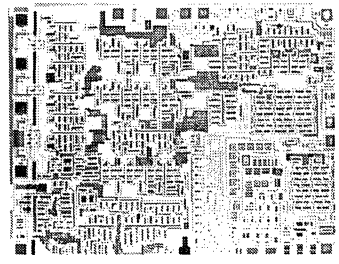
Processes, Testing and Quality Control

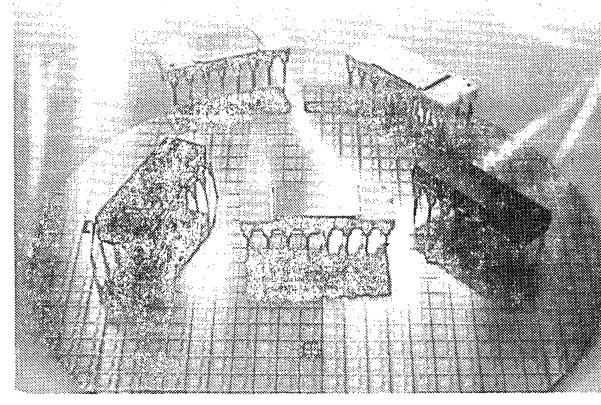
Just as we applied our systems knowledge to the partitioning of functions to make our IC's extremely flexible and cost effective, we also developed an internal system concept to ensure that we could deliver our state-of-the-art solutions year after year.

Our concept of standard processes and rigid design rules ensures that our devices are reproducible this year, next year and five years from now. Our continuing investment in research and development ensures that any new products we introduce will be on the leading edge of technology, yet with the same high performance and reliability that our customers have come to expect as the Plessey standard.

The result is that millions of Plessey devices have been built into TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.





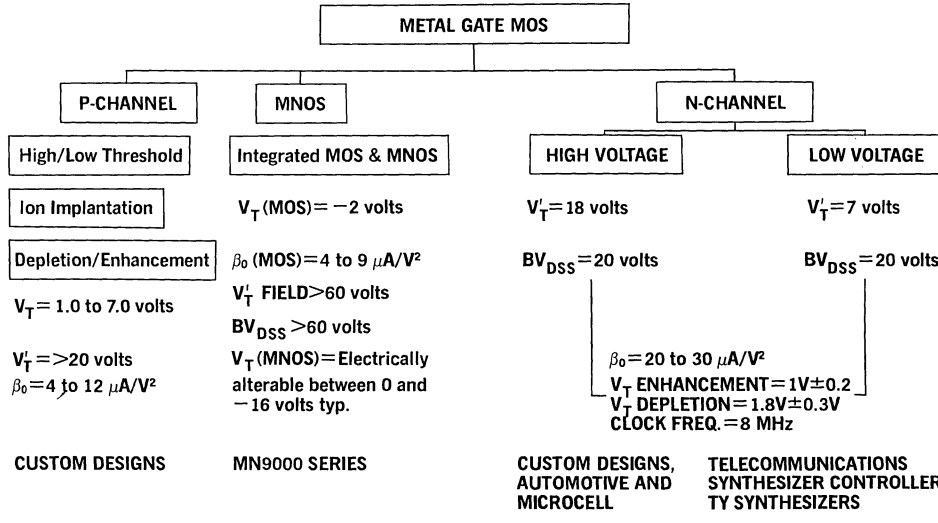


Plessey MOS Processes

P-channel metal gate MOS has been in production for years and is used for both standard Plessey products and custom LSI. Using ion implantation to modify transistor and field threshold voltages, we can reproduce virtually any p-channel metal gate process, with or without depletion loads.

MNOS (non-volatile) is essentially a p-MOS process with variable threshold memory transistors fabricated alongside conventional MOS transistors. A modified oxide-nitride gate dielectric permits the injection and retention of charge to change the threshold voltage. Current Plessey products will retain an injected charge for at least a year, and include an on-chip high voltage generator so that they may be used with standard supply voltages.

N-channel metal gate MOS uses an auto-registration co-planar process with layout similar to our p-MOS. Ion implantation is used to define the threshold voltage of the depletion and enhancement transistors. The constant-current-like characteristics of depletion load devices give the most effective driving capability, and enhancement-depletion technology simplifies design and increases packing density. The field threshold voltage is also controlled by an ion implant, allowing the use of a lightly doped substrate. This reduces both the body constant and the junction capacitance and results in faster switching speeds.



Plessey Bipolar Processes

Bipolar Process I is a conventional buried +N layer diffusion process with f_t=600 MHz and other characteristics similar to industry-standard processes. Applications range from high reliability military devices to high volume consumer products.

Process Variant	A	B	G	D
Application	General Purpose	Non Saturating Logic	Saturating Logic	Linear Consumer
BV_{CBO} @ 10μA	20V min.	10V min.	10V min.	45V min.
BV_{EBO} @10μA	5.3V to 5.85V	5.15V min.	5.15V min.	6.8V to 7.4V
LV_{CEO}	12V min.	8V min.	8V min.	20V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.43V max.	0.32V max.	0.43V max.	0.6V max.
h_{FE} @ I_C=5mA, V_{CE}=5V	40 to 200	50 min.	50 min.	50 to 200
f_T @ I_C=5mA, V_{CE}=5V	500 MHz	500 MHz min.	500 MHz min.	350 MHz min.

Bipolar High Voltage (HV) Process is a variant of Process I that yields an LV_{ceo} greater than 45 volts. Doping levels can be controlled and an extra diffusion used to fabricate a buried avalanche diode with a 40 V breakdown for absorbing powerful noise transients without being destroyed.

Process Variant	CA
BV_{CBO} @ 10μA	80V min.
BV_{EBO} @ 10μA	7.2V to 8.0V
LV_{CEO}	45V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.4V max.
h_{FE} @ I_C=5mA V_{CE}=5V,	80 to 300
f_T @ I_C=5mA, V_{CE}=5V	250 MHz min.

Bipolar Process III uses very shallow diffusion and extremely narrow spacing for high frequency integrated circuits with unusually low power consumption and high packing densities. An f_t of 2.5 GHz allows us to routinely produce analog amplifiers with bandwidths as high as 300 MHz and low power dividers and prescalers that operate at frequencies up to 1.2 GHz. Process variants allow us to produce devices with an extended β, higher breakdown voltages and very small geometries.

Process Variant	WE
Application	Digital
BV_{CBO} @ 10μA	10V min.
BV_{EBO} @ 10μA	5.1V to 5.8V
LV_{CEO}	7V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=5mA, V_{CE}=2V	40 to 200
f_T @ I_C=5mA, V_{CE}=2V	1.8 GHz

Bipolar Process 3V is an extension of our Process III. Ion implantation and washed emitters have given the process an f_t=6.5 GHz, allowing us to produce dividers working at 2 GHz, logic gates with delays of less than 500 picoseconds and linear amplifiers at 1 GHz.

Process Variant	WV
Application	Digital
BV_{CBO} @ 10μA	8V min.
BV_{EBO} @ 10μA	3.0V to 5.0V
LV_{CEO}@ 5mA	6V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=10mA, V_{CE}=5V	40 to 120
f_T @ I_C=5mA, V_{CE}=2V	6.5 GHz

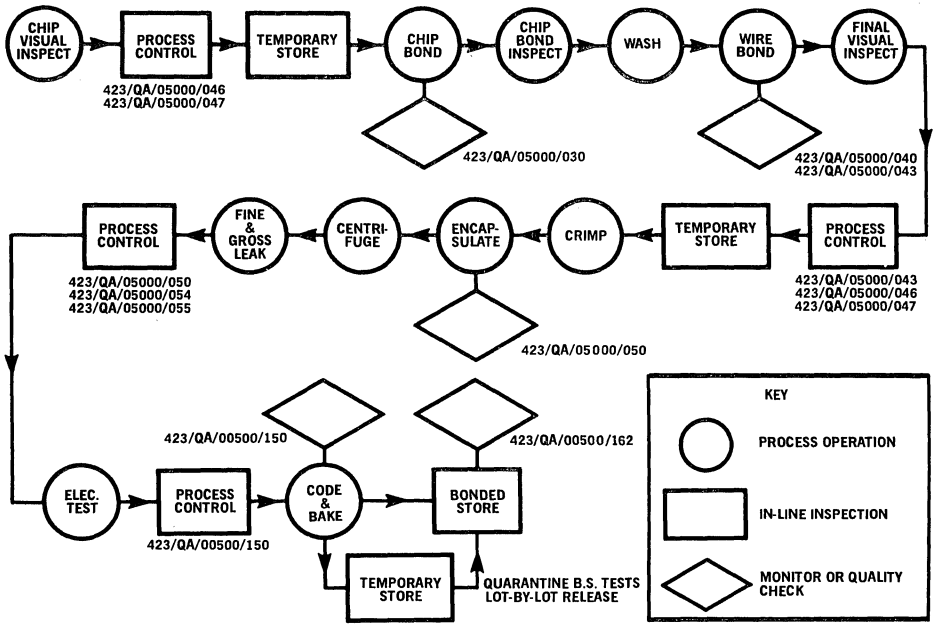
Testing and Quality Control

A major thrust of our development work is to ensure that our processes will routinely produce reliable devices. Our Process III has a projected MTBF of 400,000 hours while our Process I is even better.

Our facilities include the latest test equipment (such as the Macrodata MD501, Teradyne J324 and Fairchild Sentry VII and Sentinel) to allow us to perform all the necessary functional and parametric testing in-house. We have an internal capability to provide specific applications-oriented screening, and most Plessey IC's are available screened to MIL-STD-883 and other international specifications. Our quality levels exceed the most stringent military, TV and automotive requirements as a matter of course.

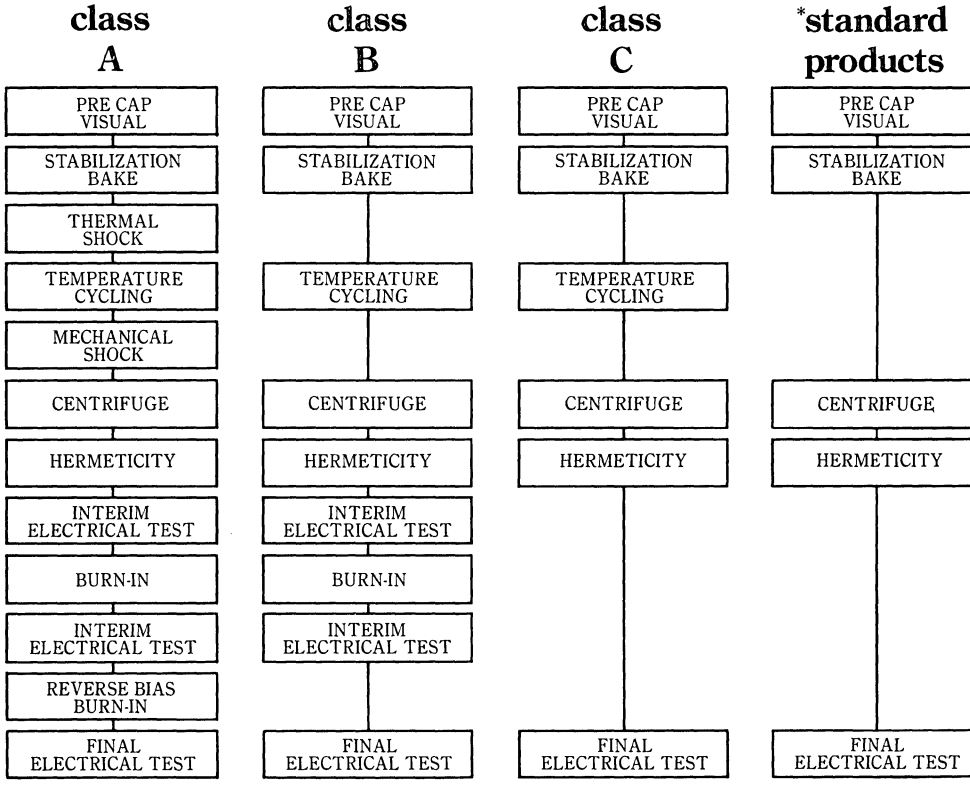
But the best proof of all these claims is our products themselves. After you've reviewed the products that could help you with your systems, use the postage-paid reply card or contact your nearest Plessey representative for complete details.

ASSEMBLY OF INTEGRATED CIRCUITS
QUALITY ASSURANCE



I.C. Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

2. TV FREQUENCY SYNTHESISER

INTRODUCTION

The Key System is a second-generation frequency synthesis kit of integrated circuits, developed by Plessey Semiconductors for the television market. The first generation system (which many other manufacturers have since attempted to emulate) prompted suggestions from customers for other features that they would like to see incorporated into such a system. This valuable input, combined with Plessey Semiconductors' expertise in frequency synthesis and high speed dividers, led to the design of the Key System.

The Key System is not simply a re-vamp of the first-generation kit, but rather a complete redesign. The aim was to simplify the television designer's task by offering circuits which could be grouped together in cost-effective modular blocks. By choosing an appropriate selection from the wide range of options available within the Key System, the designer can quickly assemble a configuration which is tailored to his specific requirements.

Fig.1 shows, in simplified form, the essential elements of the Key System.

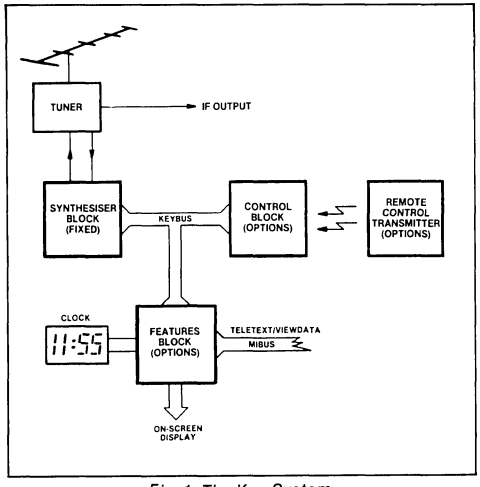


Fig. 1 The Key System

The Synthesiser Block (comprising three integrated circuits which are common to all Key System configurations) provides highly accurate phase-locked loop tuning and is used in conjunction with a conventional varicap tuner. The Synthesiser Block is controlled by means of coded information transmitted on the **Keybus** data highway by the **Control Block.**

Just as the Synthesiser Block contributes precision and stability of tuning, so the Control Block provides the versatility of the Key System through the wide range of optional circuits and configurations available. Control Block options include local and remote programme selection, dedicated control ICs, microprocessor control and a selection of four read-only memory 'Key' circuits programmed with tuning information for the most common PAL, SECAM and NTSC standards.

To allow expansion to higher levels of sophistication, Plessey Semiconductors have developed a range of optional circuits for the **Features Block.** These circuits (again, controlled via the Keybus) at present provide digital clock, on-screen display, and a Keybus-Mibus interface for Teletext and Viewdata.

In Keyway 1, the component ICs of the Key System are described, and a number of configurations illustrated. In addition, the general principles of frequency synthesis are discussed in Appendix 1 and a summary of Key System circuits is given in Appendix 2.

THE SYNTHESISER BLOCK

Fig.2 shows the Synthesiser Block, comprising the CT2010, CT2012 and CT2017. Together with the varicap-controlled VCO in the tuner, they form a phase-locked loop which is controlled via the Keybus. The CT2010 includes a sensitive prescaler which requires no additional pre-amplification of the tuner's local oscillator signal. Radiation from the circuits in the Synthesiser Block is very low: screening round these circuits is, therefore, not necessary.

The Synthesiser Block contributes the following features:

- ÷20 prescaler (CT2010)
- ÷19/20 two-modulus divider (CT2010)
- Delay-tolerant modulus control
- 2.5kHz reference frequency (CT2012)
- Power low detector (CT2017)
- Signal quality detector (CT2017)
- Varicap control (CT2017)
- 'Exact' tuning in 50kHz fine tuning steps

Full technical data for the CT2010, CT2012 and CT2017 are published in Keydata, Synthesiser Block.

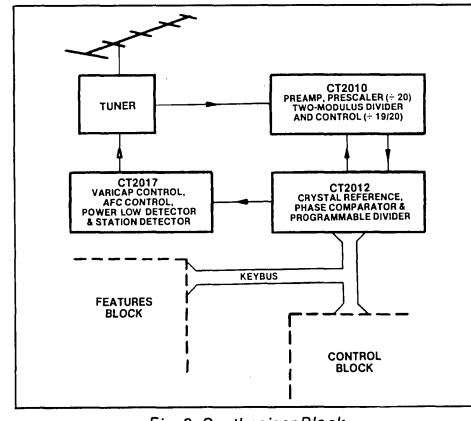


Fig. 2 Synthesiser Block

KEYBUS

The Keybus is a four-line bi-directional data plus multiplex clock highway. Control codes are

sent along the Keybus when the clock is low, and data when clock is high. Ones or zeroes are inserted between adjacent codes or data words to avoid spurious instructions. All devices driving the Keybus should have open drain outputs, for which pull-up resistors (nominally 4kΩ) are included in the CT2012.

CONTROL BLOCK

The integrated circuits from which a variety of Control Block configurations can be constructed include: three Control circuits CT2014, CT2015 or CT1650A/PIC1650Z-20 microprocessor; a choice of up to four CT2030 series Key ROMs (each programmed with 100 channels of stored frequency and name information and the ML1900 and ML1910 remote control receiver/transmitter combination.

Also optional to the Key System Control Block is the ER1400/NC7400 non-volatile memory, which can be used to store (against each programme number) Key location, channel number (channel name and band accessed from Key), fine tuning adjustments and Auto on/off information.

An alternative to the use of any of the above Control circuit options is a Control Block consisting of a microprocessor chosen and programmed by the system designer. This choice still enables the benefits of the Plessey Key System Synthesiser Block to be reaped, while using the microprocessor to perform other functions as well as controlling the phase-locked loop.

Key Circuits (CT2030 series)

The emphasis throughout the Key System is high technical performance and flexibility at a competitive price. For this reason we have designed the Key circuits, each one of which contains a 100 channel ROM to tune to the correct channel frequencies for a particular IF. Hence, each Key is designed for one particular standard. Obviously, since we have gone to the trouble of giving the possibility of 'exact' tuning (by using 50kHz fine tuning steps in the PLL), it makes sense to use the exact frequency rather than an approximation based on another transmission standard's IF. Up to four Key circuits can be attached to the Keybus, giving the opportunity for a multistandard system.

In addition to holding the frequency list for one particular standard, information is also stored in each Key circuit for the channel name and band against each channel number. The necessary interface logic for the non-volatile programme memory is also present on each Key circuit. Since these devices are pin compatible with each other, their position on the Keybus is immaterial, any Key can occupy the prime (Key 0) position through which any other Keys will interface with the programme memory.

The CT1650A/PIC1650Z-20 does not require an external Key circuit to be added to the bus. Information from one Key, the CT2030 (Pal B & G) has been included in the memory of this microprocessor.

The Non-Volatile Programme Memory

An optional add-on to every Control Block is a non-volatile programme memory. We have used the well-proven 14 x 100 ER1400/NC7400 which is available from a number of suppliers. This is capable of storing the following information for each of 32 programmes: Key location, channel number, fine tuning information (50kHz steps), Auto Mode bit. The Key location information is not stored in the single-standard microprocessor version.

On selection of a programme number, the non-volatile memory is read to give the Key location; this will access the appropriate division ratio stored against the channel number in the relevant Key. The correction tuning information is also fed out of the programme memory and, if the Auto bit is set, the system will switch to Auto Mode. In this mode of operation the digital signals from the CT2017 AFC Control are sent to the control circuit (CT2014, CT2015 or CT1650A, etc.) where they are used to change the frequency in the PLL in 50kHz steps. If the correction tuning is changed manually, the Auto Mode bit will be cancelled. Therefore, in order to store both correction tuning data and set the Auto Mode bit, the correction tuning must be stored first.

CT2200 Display Driver

If one wishes to show the programme selected on LED displays, then the CT2200 non-multiplexed display driver can be used in conjunction with two seven-segment, common-anode arrays.

This device takes the 5-bit binary input, 00000 to 11111, and directly drives two displays, 1 to 32. The only external components needed are for brightness control (as illustrated in Fig.3). The CT2200 is driven from the +5V supply used throughout the system.

ML1900/10 Remote Control

The Remote control circuits, the ML1910 receiver and the ML1900 transmitter offer the following features:

- Up to 288 commands (including Teletext, Viewdata, etc.)
- 'Base Mode' plus eight shift modes
- Six analogues, 64 levels
- ML1910 receiver doubles as 'local' keyboard encoder
- Full compatibility with CT2015 and ML2000 series (see Features Block, below)

FEATURES BLOCK

It may be that the designer would like to add to his system some special feature which can be activated from local or remote control. Our ML2000 series is designed to work with the ML1900 series to meet just such a requirement, allowing the manufacturer to add that individual touch to his product range. We will be happy to discuss this type of development. These special Features circuits are designed to be controlled externally from the Keybus with the minimum of external components.

Circuits already in development are:

- **ML2001** Keybus/Mibus interface for teletext and viewdata
- **ML2020** 12 or 24 hour crystal clock (LED and/or on-screen display)
- **ML2040** On-screen display (includes channel name, e.g. S14)

SYSTEM CONFIGURATIONS
A Basic CT2014 System

A system giving local or remote selection of up to 32 programmes is shown in Fig.3. Channel information is stored in the non-volatile memory by a 14 line digital input. This configuration is well suited to the rental market.

Many viewers, once their television set has been 'tuned' to certain stations, prefer to select just programme numbers. The configuration shown in Fig.3 allows the programme memory to be set up by using switches (as shown in Fig.4) to enter details of transmission standard, channel number, fine tuning and the signal tracking option (Auto). Of course, since the Key System uses frequency synthesis, the stations required do not have to be transmitting in order to initialise the programme memory. Having programmed the memory, if access to the switches is prohibited, this tuning information is fixed in the non-volatile programme store. Thus, accidental off-tuning of the set is not possible. Access to the fine tune and Auto switches allows re-tuning limited to the correct channel only.

If only one Key is used then the switches for KEY SELECT are not required. The particular Key chosen, depends on the market region being served.

To fill a memory location, first the particular programme number is selected, then the appropriate Key and the desired channel number are set up on the switches. Closing the TUNE switch causes the Key and channel number to be written in the selected memory location. In most cases, this will be all that is required. However, if

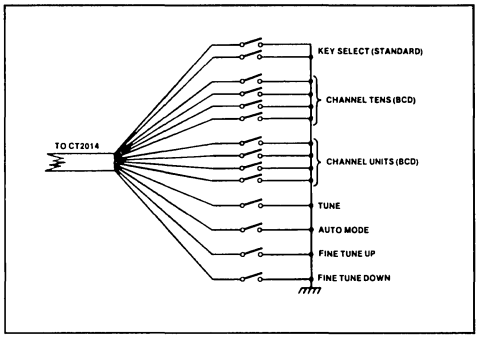


Fig. 4 Switches to initialise the programme memory

for any reason the transmitted signal is not exactly in the centre of the channel, then the system can be tuned to an off-centre frequency by using the manual fine tune switches. These enable a tuning correction to be stored in the memory location in 50kHz steps from −3.9MHz to +4MHz of the channel centre.

These switches have immediate effect on the picture and programme memory. They operate with roll over at end of channel, so it is impossible to tune outside the desired channel.

If the transmitted signal is likely to drift, the Auto bit may be set in the memory location. This will activate the Auto Mode, fine tuning the system using AFC (whilst remaining in the phase-locked loop), every time that particular programme is chosen.

Programme selection can be either by local or remote control; the input used is five bit binary.

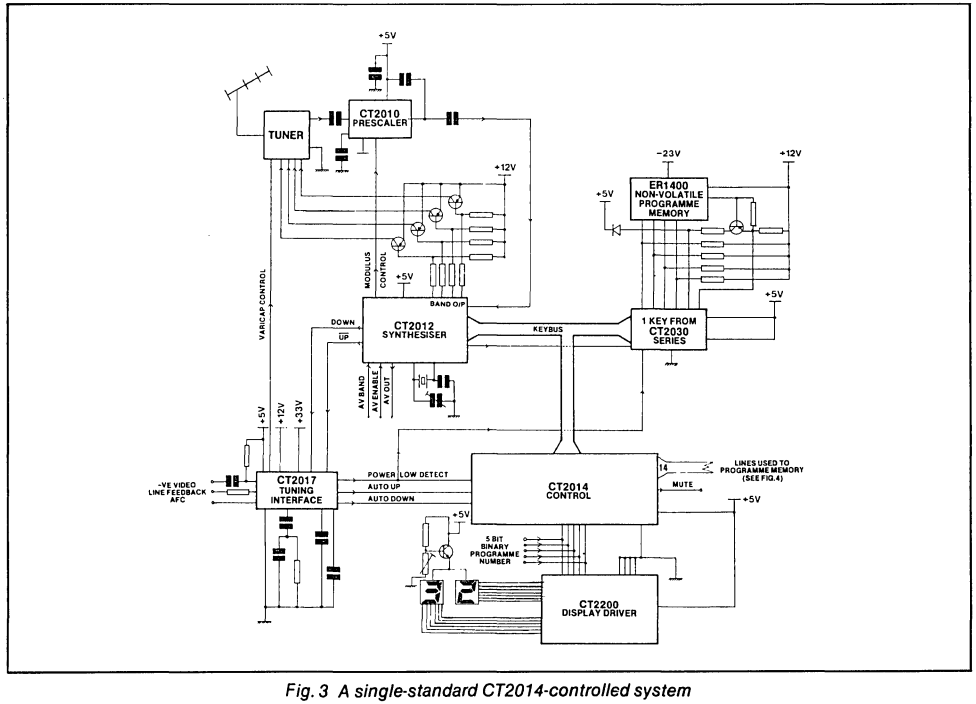


Fig. 3 A single-standard CT2014-controlled system

Multistandard CT2014 control

The Control Block in Fig.5 is similar to the one in Fig.3, the difference being that the user is allowed local control of channel and fine tuning. Up to 32 programmes can be selected from local or remote control. Fine tuning can also be controlled remotely with the addition of some logic.

Fig.5 shows how the basic system, already described, can be expanded. The method of initialising the programme memory is as before but, in this case, the viewer may be allowed to directly change Key (standard), channel or fine tuning information allocated to a programme number.

Up to four Keys can be added to the Keybus, giving a multistandard system. This option is also available with CT2015 control.

The method by which the Key and channel tens and units are selected is optional. Either BCD switches, or a running counter can be used. However, single pole switches may be preferable if the user is not allowed access to these switches. If the viewer is permitted to select a station by channel number then one or several memory locations can be allocated for such use. The new channel information can only be tuned to and stored in the memory when TUNE is enabled. If a STORE command is required instead of automatic programme update, then a CT2015 configuration should be used (see Figs.7 and 8). If no programme store is required then, as in all Key System configurations the non-volatile programme memory may be omitted.

The channel number and fine tuning information stored in the memory can be accessed via the Control circuit by the 5 bit programme number. This input is well suited to remote control interfaces. The CT2200 is again used to display the selected programme number whilst a 7447 is used to display the Key and channel numbers chosen.

As already indicated, it may be desirable to place the switches for Key and channel number away from the front of the set. The TUNE button is required to update this information, so it too may be concealed for the purposes of everyday operation of the receiver. The FINE TUNE UP, FINE TUNE DOWN and AUTO push button switches do not affect the channel number accessed, therefore they may be left on the control panel of the set. Both fine tune switches operate with 'roll over' within the 8MHz channel as does the AUTO switch. If a viewer has difficulty returning to a signal which he has tuned away from, he can return by keeping one of the fine tune switches depressed or by simply pressing the AUTO button. Any fine tune adjustments and the AUTO command are automatically stored in the non-volatile memory against that programme number.

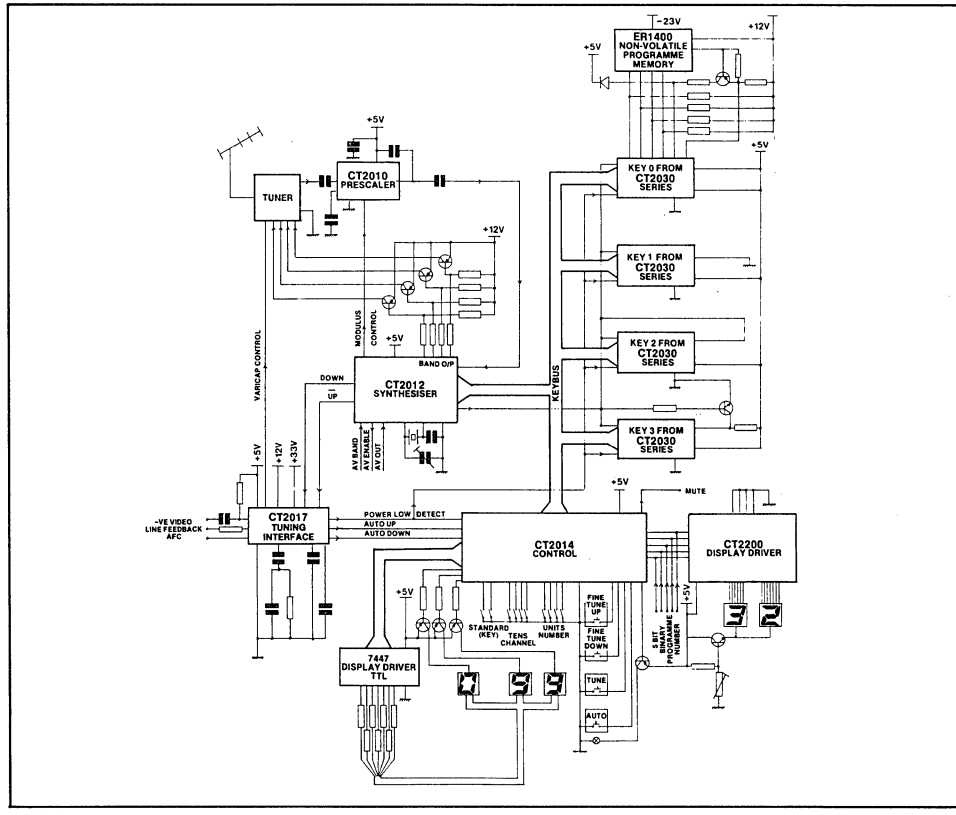


Fig. 5 A multistandard CT2014-controlled system

Microprocessor control

We have already indicated that the Synthesiser Block (CT2010, CT2012 and CT2017) is very well suited to a microprocessor application, an example of which is shown in Fig.6.

The Control Block is connected to the Synthesiser Block via the Keybus as before. One Key is programmed into the microprocessor (CT1650A/PIC1650Z-20). Features available are manual and auto fine tuning, channel and programme selection, plus a channel sweep. Remote control can be expanded from programme selection to operating the other features.

The CT2014 provides several configurations which are ideal for the European Market or others where station selection is by programme number. The CT1650A/PIC1650Z-20 gives a little more, for markets where sometimes channel numbers are used for tuning by the viewer, but usually all that is required from remote control is programme selection. As well as local or remote control of up to 32 programmes, push-button local controls allow channel selection, channel sweep, fine tuning, AUTO selection and programme step. This version fills the gap between the simple and comprehensive frequency synthesis systems.

It will be observed that no Key circuit is present in this application. This is because the CT1650A/PIC160Z-20 has an internal 'key', for PAL B and G.

To initialise the programme memory, first select the required location then the channel number (by Channel Tens Step and Channel Units Step). If the station is off-centre then any necessary fine tuning performed is also automatically stored. Similarly if AUTO MODE is selected, the AUTO bit is set for that programme. Again, because of the automatic programme information update feature in this system, it is recommended that either the programme memory is disconnected or a special location is allocated for temporary channel tuning.

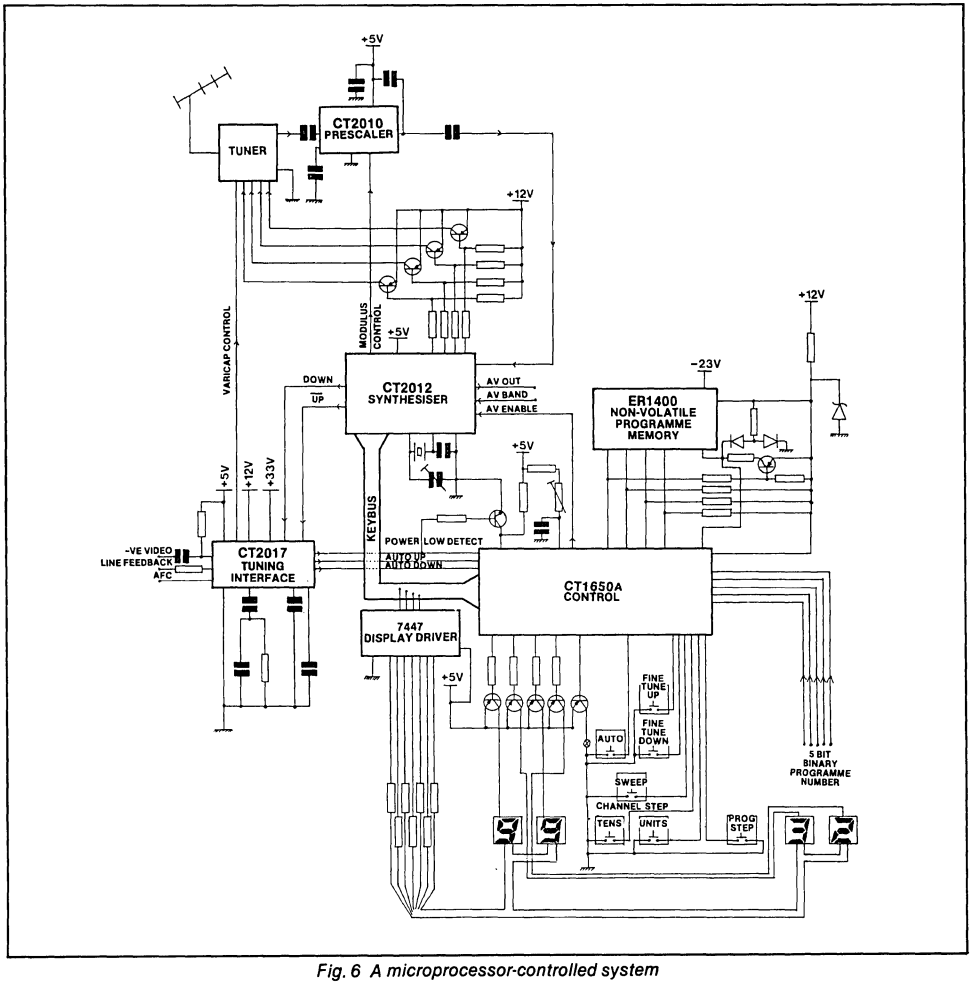


Fig. 6 A microprocessor-controlled system

Multistandard CT2015 system

The configuration of the Control Block shown in Fig.7 allows full control of all features, which are: direct channel and programme selection, manual and auto fine tuning, sweep, store, channel tens and units stepping, programme stepping, and selection of up to 4 standards (by using the Key circuits).

The CT2015 control also allows other devices to be added to the Keybus, for example, clock, Teletext/Viewdata interface and on-screen display.

The CT2015 control circuit gives the manufacturer the ability to configure his own system, which in terms of features and performance leads the market. It is the most versatile of the Key System control options.

The CT2015 interfaces, through the Keybus, with the ML1910—a remote control receiver which doubles as a keyboard encoder. The ML1900 remote control series is briefly described later in this edition of Keyway and, together with the ML2001 (KEYBUS/MIBUS interface), more fully in Keyway 5.

The features offered with the configuration shown in Fig.7 are: direct channel and programme selection, channel and programme stepping, channel sweep, store command, manual and Auto fine tuning (again, 50kHz step), control of a teletext decoder, control of a clock, six analogues, 32 programmes, storing fine tuning adjustments and 'Switch to Auto' command, choice of up to four transmission standards, and standard, channel and programme number displays.

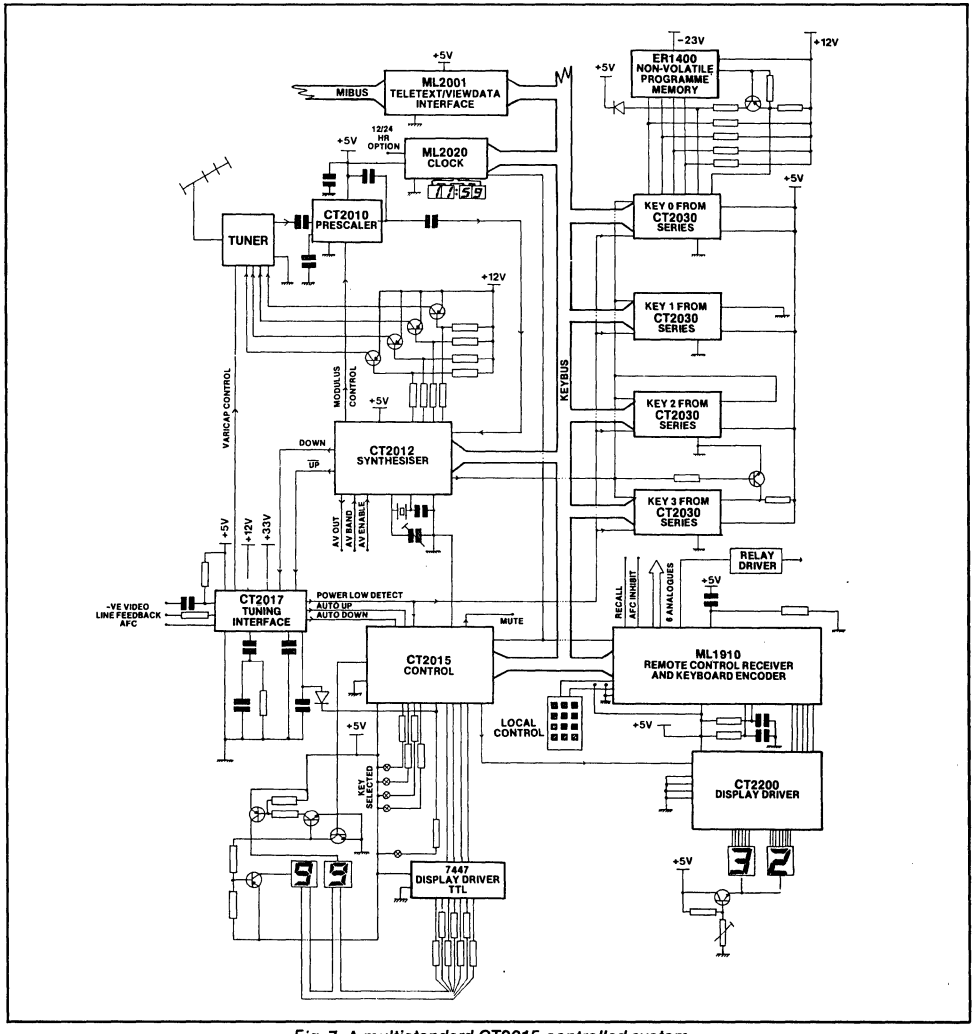


Fig. 7 A multistandard CT2015-controlled system

Single Standard CT2015 system, with full remote control

The system configuration of Fig.8 shows how the system illustrated in Fig.7 can be converted to full remote control. The CT2200 and 7447 display drivers have been replaced by the ML2040, which of course could have been used in the previous system. The Key circuit could be any one of the CT2030 series. The choice depends on the market which the system is designed for. More Keys could be used if a multistandard system were to be required.

The logic that controls the Keybus in the CT2015 enables other Features Block circuits to be added to the Keybus, for example, the ML2020 clock circuit. By 'polling' round the devices, the CT2015 allocates use of the Keybus to such circuits in turn, according to a priority setting in each Features circuit.

The features offered with this configuration are: direct channel and programme selection, channel and programme stepping, channel sweep, store command, manual and Auto fine tuning (again 50kHz step) six analogues, 32 programmes, storing fine tuning adjustments and 'switch to Auto' command, choice of up to four transmission standards, and standard, channel and programme number on-screen displays.

All of the tuning features available in the configuration of Fig.7 are also present in this system, with the addition of the remote control facility. The local and remote keyboards can be identical as each is capable of initiating the full 288 command instruction set which is possible with the ML1900 series.

A possible Keyboard with transmitter codes (F is MSB) is shown in Fig.9.

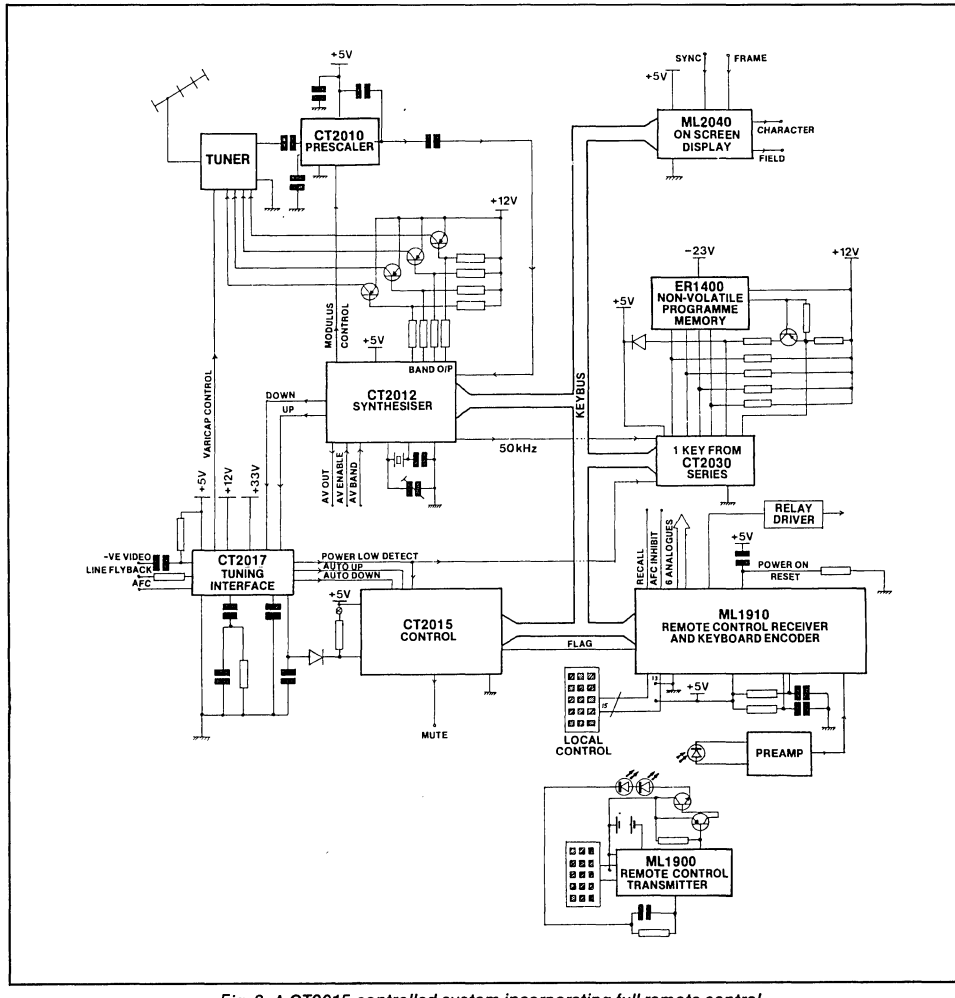


Fig. 8 A CT2015-controlled system incorporating full remote control

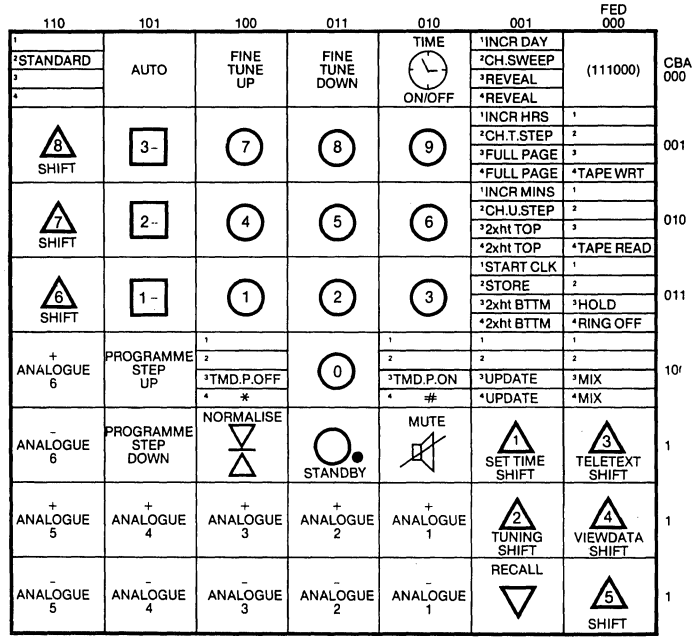


Fig. 9 A possible keyboard with transmitter codes

Summary

The **Synthesiser Block** (CT2010/12/17) contributes the following features:

- 'Exact' tuning in 50kHz fine tuning steps
- Delay-tolerant modulus control
- Sensitive prescaler
- Power-low detector
- No extra screening required
- Signal quality detector

Key circuits (CT2030 series) give:

- 1 standard per "Key"
- 100 channels per "Key"
  —required division ratio
  —channel name
  —band

Control Circuit options

The facilities available with the various control circuit options are as follows:

CT2014

- Choice of single or multistandard system
- Remote control programme selection option
- Limited use of Features Block circuits
- Direct channel and standard selection (BCD input)

CT2015

- Choice of single or multistandard system
- Remote control selection option
- Full use of Features Block circuits
- Direct channel selection
- Direct programme selection
- Store command
- Channel sweep
- Channel tens/units step
- Programme step up/down
- Keybus control logic

CT1650A/PIC1650Z-20

- Single standard microprocessor system
- Direct channel selection (tens and units steps)
- Programme number step
- Channel sweep
- Remote control selection option
- Limited use of Features Block circuits

APPENDIX 1

THE KEY SYSTEM – FREQUENCY SYNTHESIS FOR TELEVISION

The Basic Loop

The Plessey Key Frequency Synthesis System is based on the principle of the phase locked loop (PLL). A basic PLL is shown in Fig.1. In this case the output, f_o, from the voltage controlled oscillator is divided by a number, N, to give a convenient comparison frequency, f_c. The other input for comparison is the reference frequency, f_r, derived from a frequency standard.

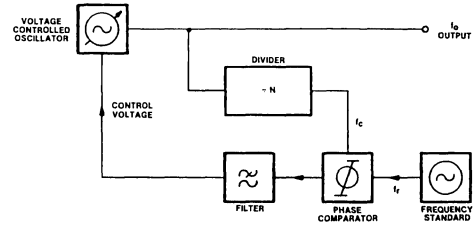


Fig. 1 Basic phase-locked loop

The phase comparator produces a voltage which is fed back via a filter to the voltage controlled oscillator. This feedback loop enables the local oscillator frequency, f_o, to be phase locked to the reference frequency, f_r. Thus:

$$f_o = N.f_c$$

and when phase lock occurs, $f_c = f_r$. so

$$f_o = N.f_r \qquad (1)$$

By choosing an appropriate reference frequency, f_r, and a suitable divider whole number N, we can now synthesise a series of frequencies, f_o, in steps of f_r. However, such a basic loop gives a very limited range of frequencies.

A Simple System

A simple practical system is shown in Fig.2. In this case, an output from the varicap controlled local oscillator is divided down by a fixed prescaler of division ratio, A, and a programmable divider of division ratio, N, to a convenient comparison frequency, f_c. An accurate stable frequency, f_r, is established by dividing down the output of a crystal oscillator. The two frequencies, f_c and f_r are compared by a phase/frequency comparator and a voltage is fed back via an active filter to the local oscillator. This feedback loop enables the frequency of the local oscillator, f_o, to be phase locked such that

$$f_o = \frac{N.A.f_x}{n} \qquad (2)$$

where f_x is the frequency of the crystal oscillator and n is the ratio of the fixed divider that follows it.

The programmable divider is controlled by the channel selector. Thus, when a certain channel is selected the selector would provide the required divider ratio code to the programmable divider making the value of N to be such that f_o becomes equal to the required local oscillator frequency to receive the channel allowing for the offset due to the intermediate frequency (IF).

Since each channel requires a certain band in the tuner, the channel selector also provides the correct band select code to switch the tuner to the corresponding band.

The stability of the frequency setting of the local oscillator will be entirely defined by

$$\frac{N.A.\Delta f_x}{n}$$

where Δf_x is the stability of the crystal oscillator.

We thus have a very useful system of tuning TV channels with the accuracy and stability of a crystal oscillator.

With the simple system shown in Fig.2, the local oscillator frequency can be preset to any value in steps of

$$\frac{A.f_x}{n} \quad \text{or} \quad A.f_r$$

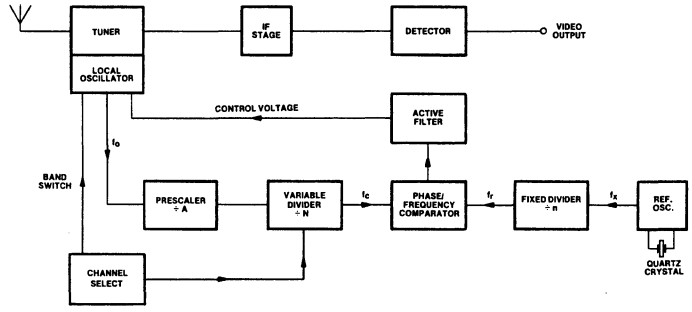


Fig. 2 Simple practical synthesiser

Thus A and f_r determine the value of the frequency step that can be achieved in the system. The value of f_r is dependant on the following factors:

1. the lock up time of the phase locked loop to the selected channel. Normally this should be 200ms max.
2. the ripple on the varactor line should be low enough not to cause any noticeable pattern on the screen.
3. the loop should not oscillate under any condition.

Considering these factors the value of f_r is normally limited to 2kHz minimum. Having decided on the value of f_r the value A is automatically set for a certain frequency step requirement in the system. For example, for a frequency step of 50kHz and $f_r = 2.5$kHz.

$$A = \frac{50}{2.5} = 20$$

Now the local oscillator frequency in a TV tuner can be up to 1000MHz, and this would mean having a programmable divider input frequency of

$$\frac{1000}{20} = 50\text{MHz}$$

which is rather high.

The Key System Principle

The Key Synthesiser uses a two modulus divider after the prescaler and before the programmable divider. This gives a much more manageable input frequency and control function. The modulus control is designed so that it can tolerate delay in the control loop and distortion in the control waveform. The positive going edge of each control pulse is only used to change the divider modulus during one complete cycle of its output. Fig.3 shows the block diagram of the Key Synthesiser.

The two modulus divider divides by a ratio, M, unless it has received a control pulse, when it divides once by a ratio M−1. For each complete output cycle of the programmable divider there are N complete input cycles fed to it from the two modulus divider. If, during these N output cycles of the two modulus divider it receives P pulses to its modulus control, it will divide by M−1 for P output cycles and for N−P output cycles it will divide by M. So for N output cycles of the two modulus divider, the number of input cycles is:

$$P(M-1) + (N-P)M$$

After division by the programmable divider, ÷N, this number of cycles produces one cycle at the input of the phase comparator.

When the loop is locked the local oscillator frequency, f_o, is given by

$$f_o = A[P(M-1) + (N-P)M]f_r$$
$$= (M.N-P).A.f_r \qquad (3)$$

An incremental change in the number of pulses, P, to the modulus control will thus change the local oscillator frequency, f_o, by a step $A.f_r$. In the Key System the prescaler, A, is ÷20 and the reference frequency at the comparator is 2.5kHz giving an incremental frequency step of 50kHz.

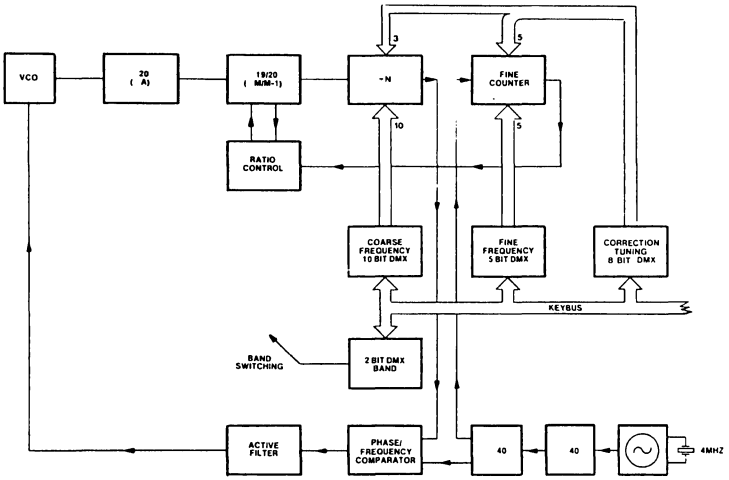


Fig. 3 Simplified Key System Synthesiser Block diagram

The two modulus divider gives ÷ 19 or ÷ 20 so that the maximum frequency into the programmable divider is only

$$\frac{f_o}{A.(M-1)} = \frac{1000\,MHz}{20.(19)} \approx 2.6\,MHz$$

and the local oscillator frequency in equation (3) above now becomes

$$f_o = N\ MHz - 50.P\ kHz$$

So N may be used to define a frequency as a whole number of MHz and P need only have a value 0 to 19 giving 20 steps of 50kHz between values of N. In practice not only does an original frequency need to be defined, but also any manual or automatic frequency correction. This gives

$$f_o = (Q + 1 - Q_c)MHz - 50\,(P + P_c)kHz \qquad (4)$$

where Q is the frequency number (10 bits)

Q_c is the frequency number correction (3 bits)

P is the fine tuning number (5 bits)

P_c is the fine tuning number correction (5 bits)

The programmable divider counts down from the loaded number, Q, until it reaches the correction number, Q_c, when it takes one cycle to synchronously reload and the whole operation repeats.

When a channel is entered initially

$$Q_c = 4 \text{ and } P_c = 0$$

so if TV channel 21 in standard G were required for example, then

$$Q = 514 \text{ and } P = 17$$

which gives

$$f_o = (514 + 1 - 4)MHz - 50\,(17 + 0)kHz$$
$$= 510.15\,MHz$$

It is also possible to correction tune around the original channel frequency with a range of - 3.95MHz to + 4MHz in 50kHz steps. This is achieved by using P_c to provide a further 0 to 19 steps of 50kHz and Q_c to provide 0 to 7 steps of 1MHz. The values of Q, Q_c, P, P_c and the band selection code are obtained via the Keybus with the appropriate tuning commands.

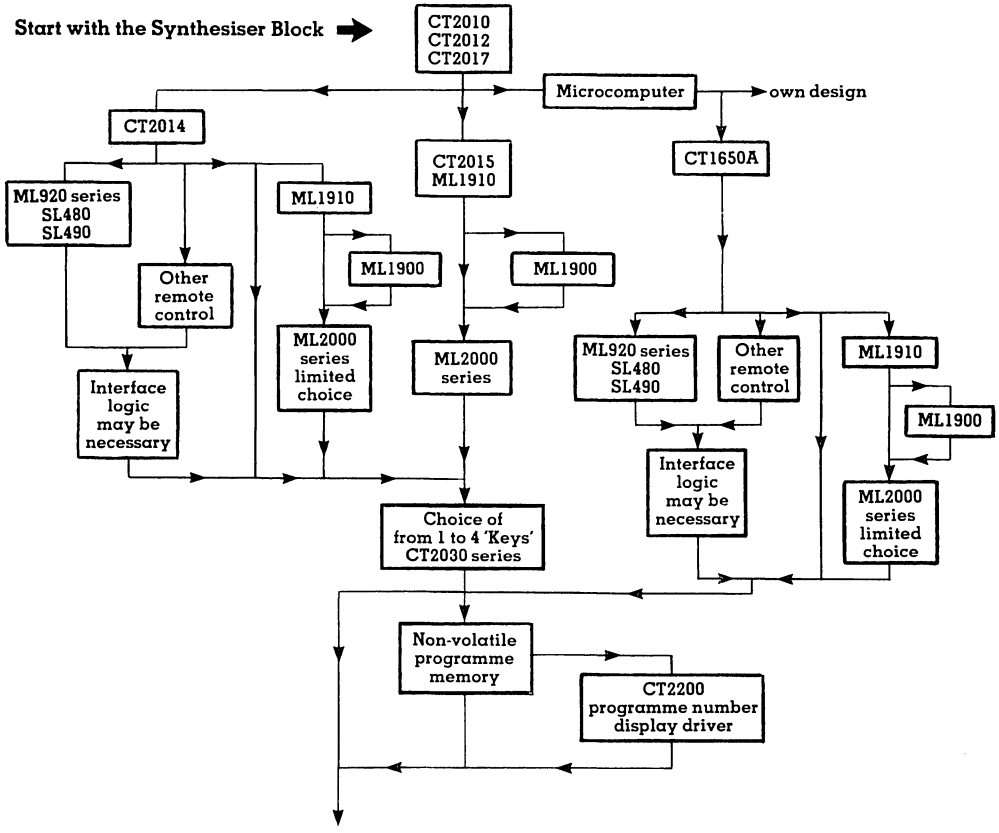
APPENDIX 2

KEY SYSTEM DEVICES

		Typical Supply Voltage	Typical Current
Synthesiser Block			
CT2010	1 GHz, 2 Modulus Divider ÷ 380/400; 10mV Input	5V	90mA
CT2012	PLL Synthesiser; crystal reference; programmable divider; phase comparator. Keybus (4 bit data highway & multiplex clock) input.	5V	25mA
CT2017	Tuner interface—varicap control—station detector; AFC control; power low detector.	5V 12V 33V	12mA 9mA 4mA
Key System Control Circuit Options			
CT2014	Digital Switch entry, Control IC. Up to 32 programmes, 400 channels and 4 standards. Manual and auto fine tuning.	5V	15mA
CT2015	Control IC with full remote control interface. Up to 32 programmes, 400 channels and 4 standards. Manual and Auto fine tuning; channel sweep. Keybus control.	5V	20mA
CT1650A/ **PIC1650Z-20**	Microprocessor Control. 32 programmes, 100 channels and 1 standard. Manual and Auto fine tuning, channel sweep.	5V 9V	35mA 1mA
Key Circuits			
	Each CT2030 series integrated circuit is a ROM for 100 channels with frequency and name information via Keybus. Key 0 can be interfaced with an ER1400 non-volatile programme memory.	5V	6mA
CT2030	European PAL Key		
CT2031	European SECAM Key		
CT2032	North American NTSC Key		
CT2033	British Isles PAL Key		
Programme Memory			
ER1400/ **NC7400**	Non-volatile memory, stores channel number, transmission standard and fine tuning information for 32 programmes.	9V and -26V OR 12V and -23V	5mA 5mA
Remote Control			
ML1900	Remote Control Transmitter; 6 bit PPM; 56 codes; burst mode output.	9V Standby	2mA 1μA
ML1910	Remote Control Receiver; 6 bit PPM; 56 codes; 55 code local input; 6 analogues with 63 levels; 32 programmes; total of 288 commands (via Keybus).	5V	35mA
Display Drivers			
CT2200	32 Number LED Display Driver, drives two 7 segment common anode LED arrays, 5 bit binary input; 1-32 display output, 20mA per segment; 13 direct drive outputs.	5V	3mA
***ML2040**	On Screen Display, displays programme and channel number, channel name, time and day. Control via Keybus; display and blanking output.		
Miscellaneous			
***ML2020**	7 day clock, quartz crystal controlled; 12/24 hour with day, hour and minute setting—output via Keybus or direct drive to LED displays.		
***ML2001**	Teletext/Viewdata Interface, allows Mibus control from Keybus.		

*Further details to be announced.

THE ROUTE TO YOUR SYSTEM



YOUR OWN SYSTEM

CT2010, CT2012, CT2017	Synthesiser Block
CT2014, CT2015, CT1650A	Control options (choose one)
ML920 series, SL480, SL490	Remote Control (see Consumer News Vol.2, No.2)
ML1900	Remote Control Transmitter
ML1910	R/C Receiver and Keyboard Encoder (see Keyway 5)
ML2000 series	Features Block circuits
CT2030 series	Key circuits (ROMs)
CT2200	5 bit binary input, 1-32 display driver

3. INFRA-RED REMOTE CONTROL

INFRA-RED REMOTE CONTROL SYSTEMS

To offer remote control as a means of achieving additional sales is fairly widespread these days, with cost prohibitive factor in some cases. At first, wired connections were used, and still are, for example, cheap remote control toys, TV games, slide projectors etc. Then came ultra-sonics, and finally in the past few years, the switch to Infra-red.

Infra-red systems offers several advantages over radio and ultra-sonic equipment in certain applications. No licence is required-signals can be easily confined by walls - or directed by narrow beams. Infra-red transmissions are not subjected to electromagnetic interference, infra-red noise is very rare in factories, offices or houses and if the signal is modulated, then corruption by flicker is very unlikely. Radio links, on the other hand, may be affected by many sources of interference, and in some applicaions, e.g. toys, the potentional hazard of aerials as a spike to a childs eyes should be avoided. Ultra-sonic links suffer from multi-path interference and can also be affected by spurious noise generation, for example bells and jingling coins or keys.

An infra-red link consists of a modulated source driving a light emitting diode which radiates at a wave length in the infra-red region (850 to 970nm). The light is transmitted through an optical system which may flood an area or concentrate the energy which is amplified and decoded to recover information that was transmitted. A basic system is shown in Fig.1. Energy levels are, typically, only a few milliwatts and therefore harmless.

Applications have been developed for both nearrow and broad beam systems. Broad beams are used for "anywhere in a room" controls, for example TV, teletext and viewdata controllers, garage doors, light dimmers, toys, slide projectors and hi-fi units. The range for broad beam systems can be between 12 to 30 meters, where choice of emitter diodes, quality of components used and pcb design, will determine the ultimate range obtained. Narrow beams on the other hand, are particularly suitable for industrial controls, security systems, computer peripheral and TV transmitter links. The range for narrow beam systems may be half a mile or more and, as these units can be designed to have a spread of no more than 10ft in 2000ft, and are virtually independant of weather conditions, they are excellent for building-to-building work particularly in data and TV transmission.

Plessey Semiconductors Limited have developed a range of remote control circuits tailored to various requirements in the TV, Industrial, Professional and Consumer market sectors.

Data sheets on the various integrated circuits involved are available on request, together with suggested circuits on a number of domestic applications.

Integrated circuits involved are as follows:-

SL490 - Easily extendable 32 command PPM transmitter drawing negligable standby current

SL491 - As above, but PPm transmission is in burst mode instead of in a continuous fashion.

SL480 - Infra-red pulse preamplifier containing 3 amplifier stages, the gain of each being capable of adjustment, to suit the application.

SL470 - Capable of decoding up to 10 programmes and incorporates direct varicap voltage selection and TTL level compatible inputs.

The following are Receiver chips that demodulates the PPM signal transmitted by the SL490/491.

ML920 - 20 programme memory, 3 D/A converters plus 6 other facilites.

ML922 - As above, but with only 10 programme memory.

ML923 - 16 programme memory, 1 D/A converter plus 6 other facilites.

ML924 - 5 digital outputs whose response to PPM codes be programmed by 6 control lines. Has a handshake interface which provides communication with microprocessors and computers.

ML925 - Designed to control either a toy vehicle with 2 speed drive motors and a three position latching steering system, or a vehicle with momentary action steering and a third motor, typically a winch.

ML928/9 - General purpose receivers, latching 16 of the 32 codes transmitted by the SL490/1.
The ML928 responds to codes 00000 to 01111 and the ML929 to codes 10000 to 11111.

ML926/7 - As above, but with unlatched outputs.

Other components needed for an infra-red system are the emitter diodes and the photo diode.

The photo diode used is a highly critical component. Several manufacturers have developed photo diodes for use in the infra-red region-the characteristics of one such device is shown in Fig.2. This is a low leakage p.i.n. device with planar construction; the active area is 7.5mm². A silicon nitride layer over the chip acts as both a passivating coating and an efficient anit-reflection layer. A dye in the plastic housing transmits well in the near infra-red part of the spectrum (700nm to 1100nm), but is strongly absorbant to visible light (400nm to 700nm). The spectral response of silicon, in addition, is higher in the infra-red than in the blue green region. Planar construction keeps the reverse leakage current low, which is very important in small signal applications.
Usable signal to noise ratios can be achieved with photo current as low as 10nA provided the load is carefully chosen.

Many alternative infra-red high efficiency L.E.D's are available; typical emission characteristics are also shown in Fig.2. Increased sophistication of epitaxial techniques is likely to mean that increased power conversion efficiency will be available over the next few years. It is usual to drive these L.E.D's with pulses of current which peak at much higher than rated values, keeping the duty cycle such that mean rated power is never exceeded. In this way transmission distances are increased.

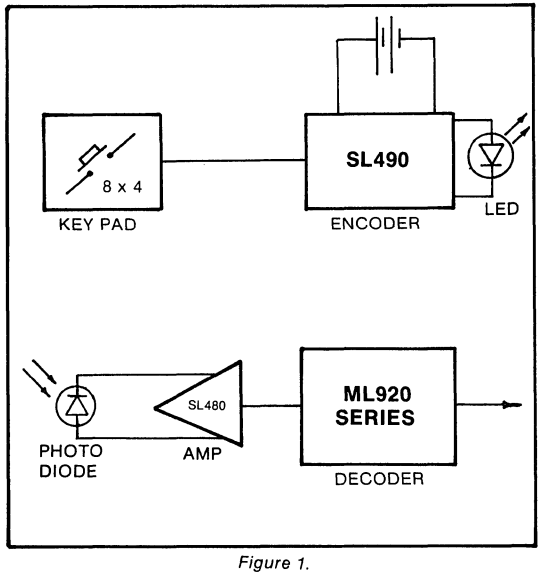


Figure 1.

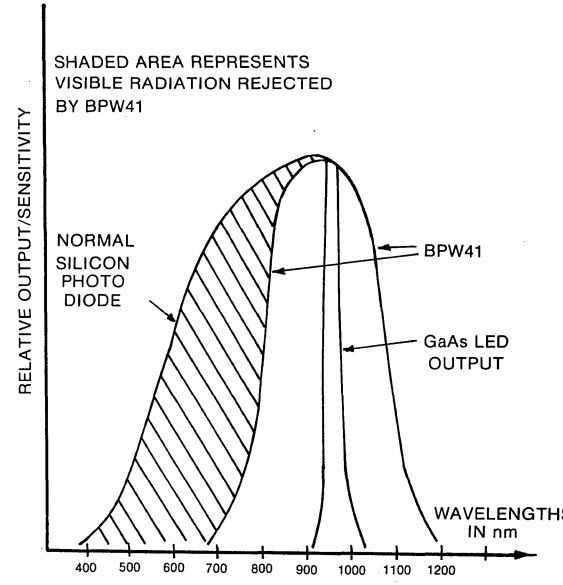


Figure 2.

Transmitter Chip SL490

Fig.3. shows the circuit for a simple infra-red transmitter where the PPM output pin 2 of the SL490 is fed to the base of the PNP transmitter TR1 via R1 and R2, producing an amplified current pulse in the collector about 15usec wide. The pulse is further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red light output is controlled by the quantity, type, and connection method of the diodes and also the gain at high currents of the transistors.

The common solution where cost is important is to use 2 single chip diodes, such as the Siemans CQY99 CONNECTED SERIES.

Improved output can be obtained by using four CQY99 diodes in a series parallel arrangement, but is usually simpler to use 2 multi-chip diodes such as the Telefunken CQX47 connected to parallel or single CQX19 which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflected

When building the transmitter, care should be taken with the choice of the capacitor C2 and with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8 amps.

Transistor choice is also important and any substitues should have high current gain characteristics and switching speeds similar to those specified in Fig.3.

An increase in output can be obtained be reconnecting TR2 in a common emitter mode, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequencies

Although the ML920 series of remote control receivers is designed to work over a wide range of PPM frequencies, the actual usable range may be resricted by the application. The analogue outputs on the ML920, ML922 and ML923 serve as a good example, since the outputs will step up or down, one step for each pair of PPM word received. This in turn fixes the rate of increment or decrement of the volume or color controls of a TV set.

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig.3, power consumption will increase with frequency. It is thus advisable that with a battery power supply, the slowest PPM rate consistant with adequate response time, should be chosen.

Setting Up Procedure

When designing a system using the SL490/491 transmitters and the ML20 series receivers, it is not necesssary to adjust the PPM rate on both transmitter and receiver. The usual arrangement is to have a fixed resistor of 33K from pin 16 of the SL490/491 and to choose the capacitor connected for pin 16 to pin 17 to give the required PPM rate. The value is calculated from the formula 'to' = 1.4CR. Provided fairly close tolerance components are used for C1 and R1, then assenbled transmitter units should be interchangeable without adjustment.

The timing components on the receiver can be selected using the formula $frx = \frac{1}{0.15CR}$ where $frx = \frac{40}{'to'}$, 'to' being the P.P.M. logic "0" time from the transmitter.

The value of R for the receiver should be between 47K and 200K, a typical arrangement being to use a 47K resistor and a 100K pot as shown in Fig.4. The capacitor should be selected from the above formula to give the nominal frequency somewhere near the mid-range setting of the potentiometer.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter P.P.M. logic "0" time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope to reduce circuit loading.

When adjusting the ML920, the monitor output can be used for setting up, but in this case, a figure of 1/20th of the transmitter P.P.M. logic "0" time should be used as the mirror output is at half the oscillator frequency.

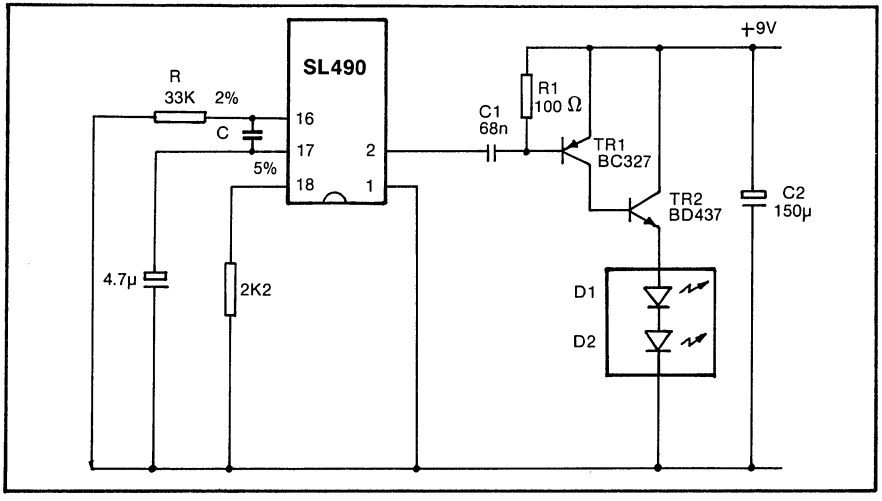


Fig. 3. Infra-red Transmitter

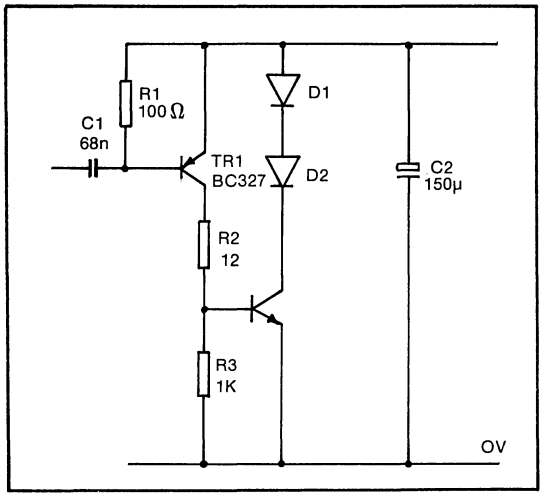


Fig. 3. Common Emitter Arrangement

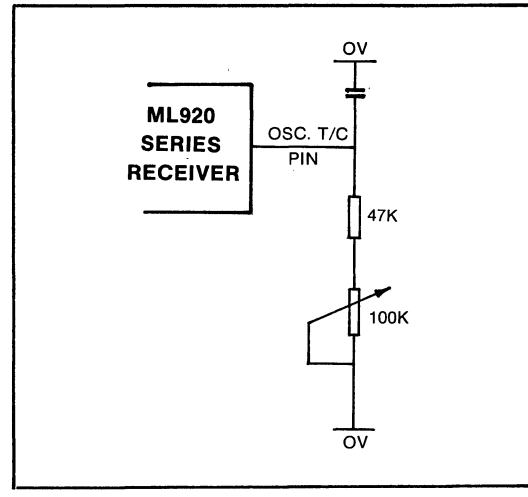


Fig. 4. Recommended Receiver Time Constant Components

The SL480

The circuit diagram of the SL480 infra-red pulse amplifier is shown in Fig.5. Pulses generated by a infra-red receiver diodes are amplified to a suitable level for direct connection to the input of any of the Plessey Semiconductors ML900 series of remote control receiver circuits.

For basic operation, the receiver diode and SL480 input is biased with a single resistor to the positive supply as shown in Fig.6. Any infra-red light reaching the diode generates a leakage current which causes a voltage drop across the bias resistor.

The SL480 Input stage consists of a compound emitter follower (TR1 and TR2) which provides a high input impedance and allows a relatively high diode load resistor as well as a voltage drop of around 1.3V between the input and the bases of the first amplifier stage (TR6,TR7).

Transistors TR6 and TR7 form a differential amplifier which is designed to prevent low frequency or D.C. input signals from reaching subsequent stages of the amplifier. Since the bases of transistors TR6 and TR7 are internally connected by the 6.3K resistor R3 low frequency signals are applied to both sides simultaneous causing no change in collector current and therefore no output to the second stage. Higher frequency signals are amplified because TR7 base is decoupled externally on pin 7.

Stage 2 gain is provided by a similar differential amplifier to stage 1 except that the relativly stable d.c. input voltage provided y stage 1 output allows the use of a tail resistor R11 rather than a current source. Decoupling of A.C. signals is provided at pin 8.

Stage 3 is similar to stage 1, but with a extra current mirror (TR24 to TR26) to provide signal inversion at the output

The standing current in the output load resistor and thus the output voltage, is set by the current in R15. This current will amount to about 100μA, and give an output voltage about 5V below the positive rail with a 15V supply.

It should be noted that there is a parasitic zener diode of about 6V in parallel with the ouput load resistor R19, this will be destroyed if the output is shorted to the negative supply rail. Stage 3 decoupling is provided at pin 1.

With a 15V supply, the input stage will operate with input voltages ranging from 15volts down to 5volts. This will allow the device to function satisfactorily in high ambient light conditions which produces high leakage currents in the receiving diode. A single transistor circuit is shown in Fig.3, which prevents the input voltage to the SL480 changing for diode leakage currents up to several miliamps. By carefull choice of R & C values, this circuit can be made to give extra rejection of low modulation such as that produced by incandescent lamps.

If required, the gain of each of the SL480 can be set individually by connecting a resistor in series with the decoupling capacitor. A 6K resistor will reduce the stage gain to half its full value of about 40dB. Normally it is only necessary to reduce the gain of the second stage with about 33-56K.

As with any high gain device, care is needed in the layout of printed circuit boards to prevent instability. All decoupling and input components should be mounted close to the SL480.

Decoupling of the power supplies local to the SL480 is advisable. Aresistor of about 560 Ω in series with the negative rail and a parallel capacitor of 68μF being adequate (See fig.7).

The decoupling resistor should always be in the negative supply as the ML920 series remote control circuits have a threshold close to the positive rail, and any voltage drop here would reduce the noise immunity.

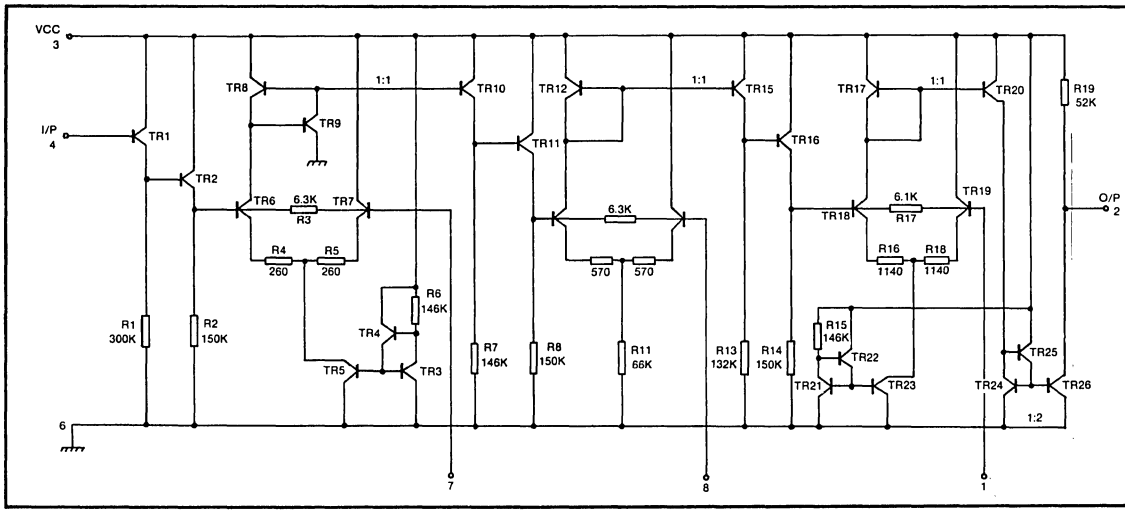


Figure 5.

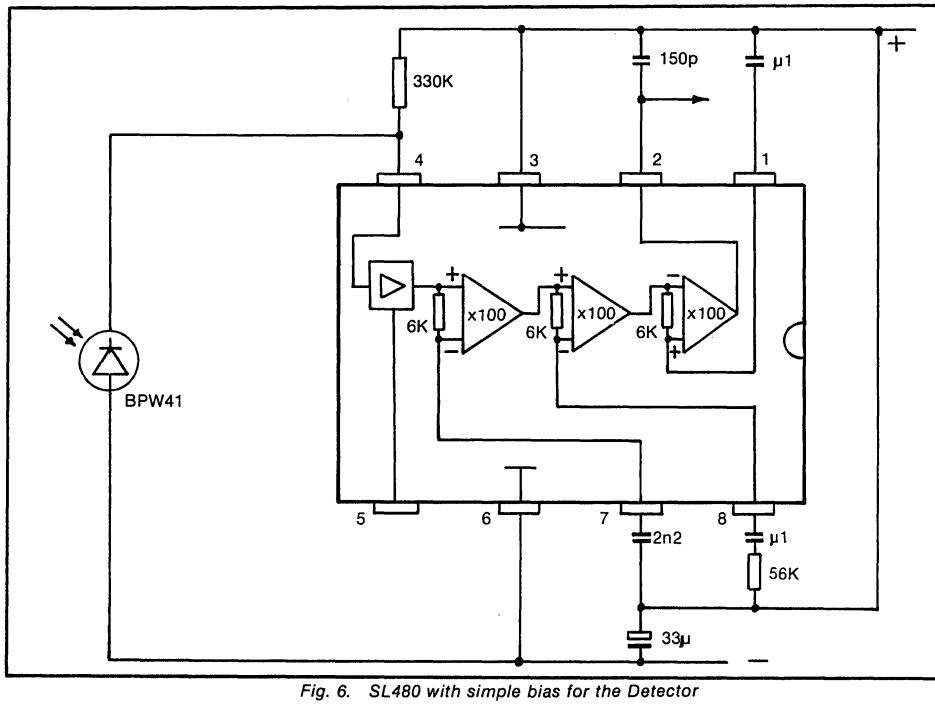


Fig. 6. SL480 with simple bias for the Detector

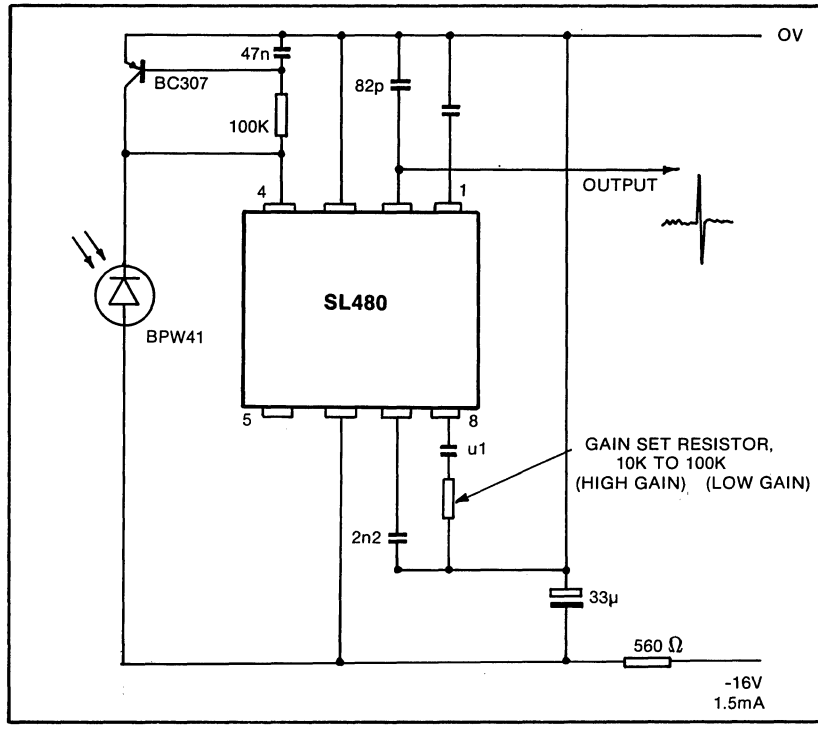


Fig. 7. Typical Infra-red Amplifier application with ImprovedDetector Biasing.

4. REMOTE CONTROL FOR TOYS

The new remote control circuits now available are the SL470 10-programme decoder for high voltage varicap line drive; the SL490 infra-red preamplifier with direct drive for the ML920 series; the SL490 remote control transmitter; the ML920

The new remote control circuits now available are the SL470 10-programme decoder for high voltage varicap line drive; the SL480 infra-red preamplifier with direct drive for the ML920 series; the SL490 remote control transmitter; the ML920 20-programme remote control receiver; the ML922 remote control receiver providing three analogue outputs, 10 latched programmes and on/standby, mute etc; the ML928 remote control receiver/encoder providing four latched outputs controlled by 16 transmitter commands; the ML929, basically similar to the ML928 but operating on a different set of 16 transmitter commands; the ML926, similar to the ML928 but giving momentary, unlatched outputs; the ML925 for motor control in toys and models and, available soon the SL491 for burst mode transmission.

SL470

This device decodes up to 10-programmes, incorporates direct varicap voltage selection and TTL level compatible inputs. It can be directly driven by the ML922 receiver and has a low component count for low cost applications.

SL480

The SL480 is a bipolar integrated circuit containing three amplifier stages. Its output is directly compatible with the ML920 range of remote control receiver circuits, and it is in an eight lead plastic package. A feature of the device is that the gain/bandwidth of the amplifier stages can be adjusted to suit the application (see Fig.1).

Pin functions, SL480

1. Decoupling point
2. Output decoupled with capacitor and fed directly to receiver PPM input.
3. Positive supply
4. Detector input
5. Not used
6. Negative supply
6. Negative supply
7. Decoupling point
8. Decoupling point

SL490

The SL490 remote control transmitter is an easily extendable 32 command, pulse position modulation transmitter which draws negligible standby current. It can be used effectively with any ML920 series remote control receiver.

The ML490 pulse-transmitting remote controller, used in conjunction with the ML920 receiver offers the possibility of controlling up to 20 television programme selections, brightness/volume/color control in up to 32 steps, and a number of other functions both for television use and elsewhere.

A wide variety of domestic, commercial and industrial appliances can be controlled by the SL490/ML920 combination. Apart from use with television and toys the system can control such diverse equipment as, for example, radios and tuners, tape and record decks, garage doors, automatic telephone answering machines and slide projectors.

ML922

This device demodulates the PPM (Pulse Position Modulation) signal received from the SL490 transmitter. The ML922 was originally designed for television remote control systems but can easily be adapted for use in radios, tuners, tape and record decks, lamps and lighting, industrial control and monitoring, and toys and models.

The ML922 demodulates the PPM signal received from the SL490 and after error checking the received code can condition a 10-programme memory or one of the three D/A converters, the output of each having its normalised level at three eighths of maximum

The receiver timing can be set by adjusting the oscillator time constant to give 40 periods at pin 6 equal to a 0 interval on the received PPM input.

ML920

The ML920 is a 20-programme version of the ML922, but has (in addition to the facilities offered by the ML922) a 'recall' output which can be used to trigger an on-screen display in TV applications.

ML928 and ML929

Both these devices are general purpose remote control receivers each designed to receive and latch 16 of the 32 codes transmitted by the SL490 circuit as 5-bit PPM.

The ML928 responds to codes 00000 to 01111 only, and the ML929 responds to codes 10000 to 11111. Both devices are packaged in 8-lead plastic DIL to minimise board area. The on-chip oscillator can be adjusted from 15Hz to 150kHz, allowing different transmission rates.

Both devices have a high degree of immunity to incorrect codes; there must be two correct and consecutive codes received before the outputs can change. As with ML922 these devices were initially designed to be used with television remote control. They have, however, a wide range of applications, particularly in toys.

ML926

This device has momentary outputs. Normally low (off) selected outputs go high (on) during reception of the appropriate code. After transmission has finished the outputs return to the low state. The device is similar to the ML928 except for its four positive logic unlatched outputs.

ML925

Up to three independent motors, as well as lights, flasher and horn, may be driven by this 18-pin device. Four speeds are possible with both forward and reverse giving a very flexible toy or model controller.

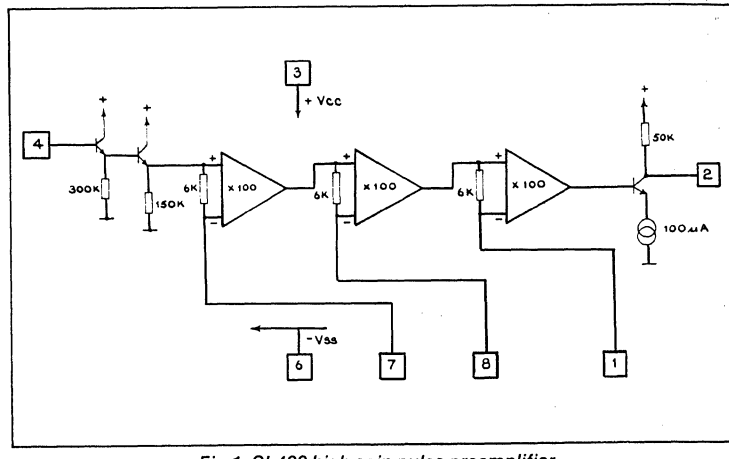


Fig.1 SL480 high gain pulse preamplifier

SL490 remote control transmitter

General description

The SL490 is an 18-pin bipolar, remote control, pulse transmitting monolithic circuit for use with the ML920/ML922/ML926/ML929/ML925/ML926 receivers.
Single pole switches arranged in a 4 x 8 matrix of 32 keys (1 out of 4 and 1 out of 8) are encoded by the device which then may give either a modulated carrier frequency from an on-chip oscillator or a DC pulse output. A standby current of only 6uA or so is taken from a 9V supply by the device until any switch closure is detected. In this system of PP3 battery has a working life approaching the length of its shelf life.

The modulated output can drive an ultrasonic transducer directly and be tuned to the natural resonant frequency of the crystal, thus enabling inexpensive transducers to be used.

A five-bit pulse position modulated signal is used, giving 32 basic commands which can be used in a TV remote control system to select 20-programmes, control 3 analogue functions and provide 6 additional switching functions.

Apart from the battery, switch matrix and transducer, only three capacitors and two resistors are needed externally. A single RC selects carrier options and defines frequency, the other RC defining the modulation rate.

Output capability is direct ultrasonic transducer feed, and complementary outputs with or without active pull-ups. Continuous or pulsed visual indication can be driven directly from pin 2. The carrier oscillator can be disabled for pulsed operation of infra-red, and more than one set of 32 commands can be used by changing the modulation rate and carrier frequency.

Despite the comprehensive range of facilities offered by this remote control system, the SL490 makes the transmitter a very simple unit. Fig.2. outlines the block diagram of the transmitter.

Circuit Operation

The device transmits a code word as a group of six pulses, and each of the five intervals between these pulses can take up one of two possible values, a short interval corresponding to a '1' or a long interval corresponding to a '0'. Fig.3 shows the timing relationship between the pulses '1', '0' and 'S' - the space or synchronisation gap between words.

The ratio of the intervals representing '1', '0' and 'S' is 2:3:6 and is fixed by the device. In addition the width of the pulse is about one sixth of a '1' interval or 1/3:2 on the above ratio scale. In this way 32 different codewords can be transmitted by the 5-bit code.

A particular codeword is selected by switching one out of four current sinks (one of these current sinks is 0V). All decoding is done by the integrated circuit as in Fig. 2.

The circuit draws only about 6uA from the supply until a switch closure is detected, at which time power is applied to the whole circuit. The appropriate PPM code is then generated repeatedly until the switch is released, and the device reverts to standby after the complete codeword has been transmitted.

Fig. 4 and 5 show the output voltage waveforms obtainable. Fig.4. shows a lower than normal carrier frequency compared with the pulse width. This is done for clarity although the device would operate satisfactorily with such timing.

For infra-red operation a two transistor amplifier is used to feed very narrow high current pulses to gallium arsenide infra-red diodes, such as two Plessey GAL32B. If a higher output is required three or four GAL32C diodes can be used in parallel. The pulse nature of the signal allows the diode emitter to work at a higher light output efficiency and the battery current to be reduced. Fig.12 shows a circuit for driving infra-red emitting diodes.

The receiver amplifier

At the receiving end of the link the system will need some sort of gain and bandwidth defining stages, before the detected signal is fed to the ML920 series receiver. Usually two, or at most three, amplifier stages are sufficient with some fairly simple active filtering. In the case of the infra-red link the SL480 can be used with an infra-red filter before the photo detector.

For ultrasonic transmission a general purpose operational amplifier may be used for the front end. After filtering and amplifying the ultrasonic frequency, a simple diode detector can be used. The detected PPM can then be fed to the receiver via a buffer amplifier stage. An ultrasonic frequency of between 32kHz and 44kHz should be chosen to avoid the second and third harmonic of the TV line output stage. An inexpensive transducer can be chosen with its natural resonant frequency within this band, and can be driven at its natural resonance to improve power output and simplify loading. The actual bandwidth needed about the carrier is approximately 100Hz. The data rate can be chosen by considering the rate at which the analogue outputs of the receiver are required to step.

If, for example analogue output to sweep its full range of 32 steps in about 10 seconds, this requires one step about every 300ms but because of the receiver error checking code comparator, the transmitter word rate should be set to 150ms (see Table 1). Referring to Fig. 3 it will be seen that if the code word period, including the interword space, is 162ms it will give the required analogue full range change in about 10 seconds. The only adjustment needed in the receiver is to set the oscillator time constant, so that 40 time periods on the oscillator (20 periods on the monitor pin 9 of the ML920) corresponds to a ±0± interval of incoming PPM (Fig.6 and Table 1).

Up to 10 per cent variation in demodulator timing oscillator frequency can be tolerated by each of the transmitting and receiving devices.

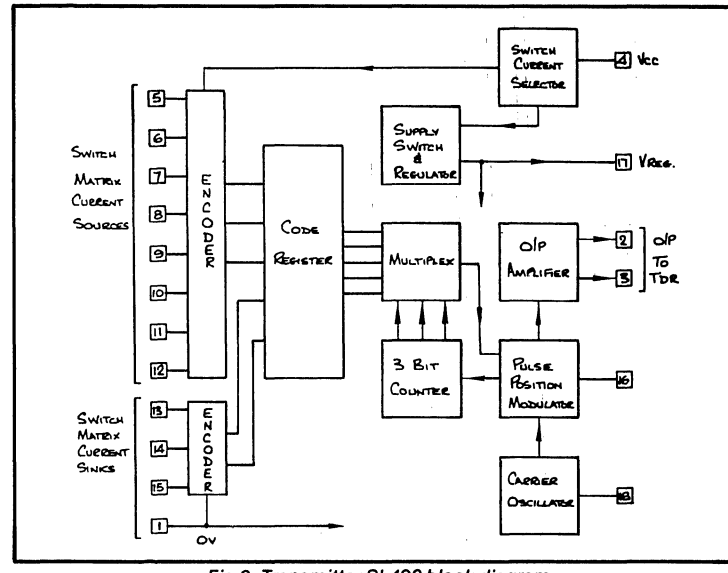


Fig.2 Transmitter SL490 block diagram

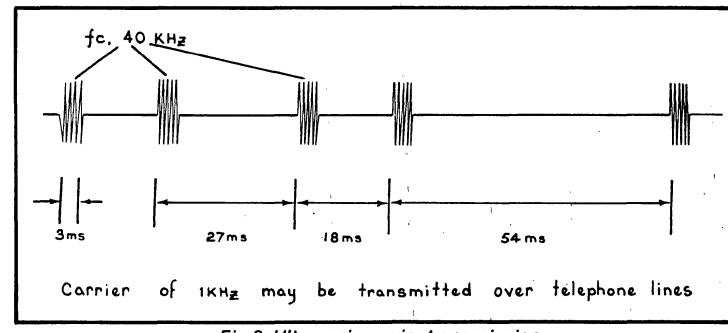


Fig.3 Ultrasonic carrier transmission

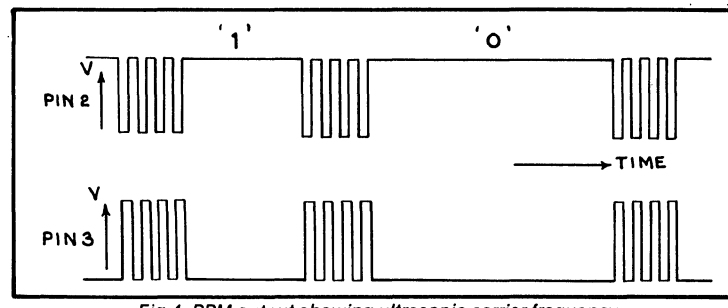


Fig.4 PPM output showing ultrasonic carrier frequency

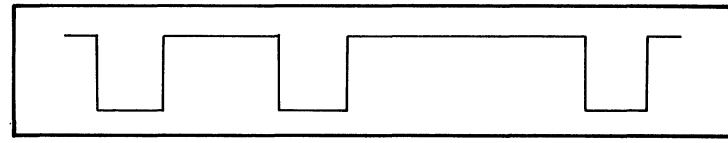


Fig.5 PPM output (pin 2) with no carrier

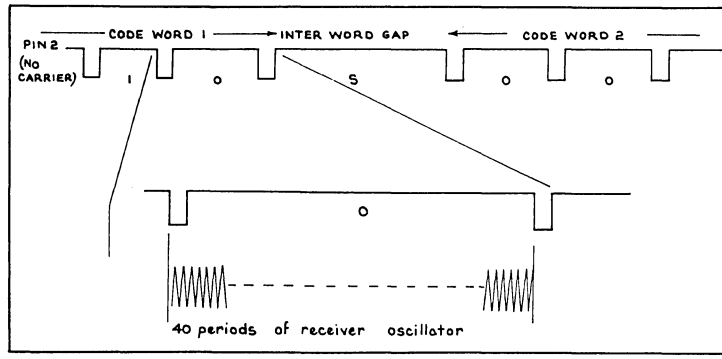


Fig.6 System timing

'O' period (ms)	TX C(µF)	RX C (nF)	Osc. (kHz)
40	0.82	100	1
20	0.47	68	2
10	0.22	33	4
5	0.1	15	8
2.5	0.047	8.2	16
1.25	0.027	3.9	32
0.625	0.015	1.8	64
0.312	0.0068	0.82	128

Table 1 TX and RX Timing

An infra-red link

For most remote control work, infra-red links have advantages over ultrasonic links-less multipath interference, lower spurious radiation, less annoyance to humans and animals, a higher modulation rate capability and more robust transducers. High efficiency, infra-red, light emitting diodes (LED's) are relatively inexpensive and can incorporate both reflctor and lens for a more concentrated beam of light.

Multichip assemblies are also becoming more common and these can take fairly high currents. LED's become more efficient at higher currents, and pulse and multiplex systems are common for display work. Thus a PPM system can be made to operate an LED at quite high outputs for a small increase in battery current. Two or three LED's can be connected in series at lower currents, and these emitters can have different orientation on their axes if required.

On the receiver side a photodiode or phototransistor can be used with an appropriate infra-red filter. Fig.7 shows how a photodetector response, although peaking in the near infra-red region, has good detection properties at visible light wavelengths and into the ultra-violet. As the energy emitted from a gallium arsenide LED is, in the main, a narrow band emission at 940nm, a correctly chosen filter will greatly attenuate most of the interfering signals. Other noise sources which have large emissions in the infra-red (for example a tungsten filament lamp) can be rejected by filtering or by carrier modulation of the infra-red link.

Both amplitude modulation and frequency modulation have been used, but neither has the simplicity nor all the advantages that a pulse system can offer in LED driving efficiency and detection economy. Pulse position modulation using a narrow pulse, high current drive to a gallium arsenide LED enables a very good signal-to-noise ratio to be obtained at the demodulator. Reception remains uninterrupted by most external influences. Very bright sunlight or the close proximity of a high output fluorescent gas discharge tube has a minimal effect, especially in the case of the SL480 with its daylight bias arrangement (see Fig.9).

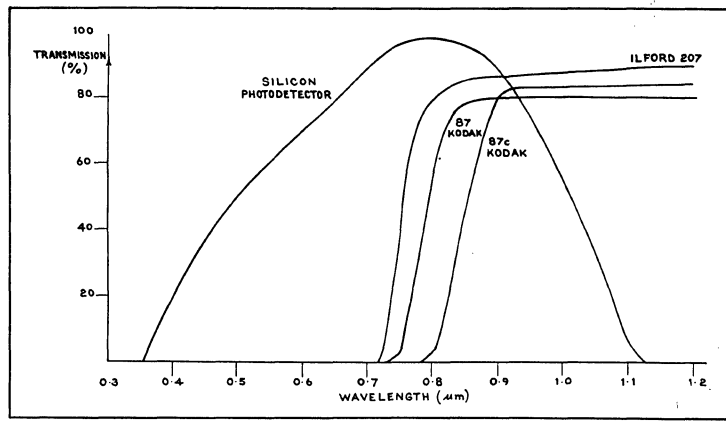


Fig.7 Optical response characteristics

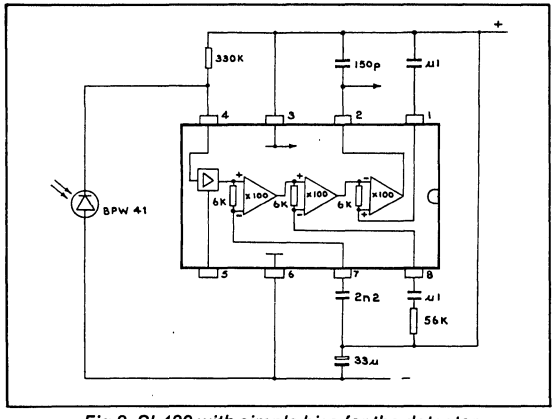


Fig.8 SL480 with simple bias for the detector

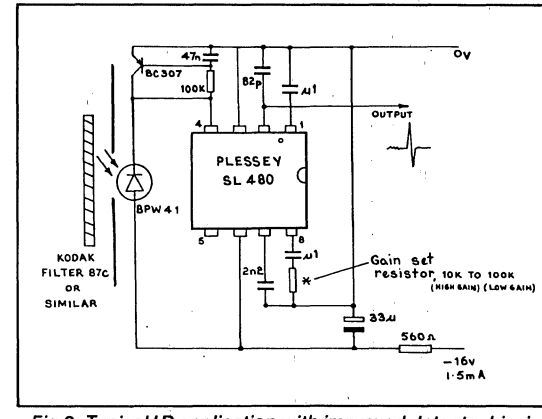


Fig.9 Typical IR application with improved detector biasing

SL480 infra-red pulse preamplifier

The SL480 is a low cost, low external component count, front end amplifier for infra-red pulses (see Fig.8 and 9).

It has three gain stages, each with a gain 100, and differential inputs with inverting input bonded out to provide access both for decoupling and frequency determination.

Input impedances are typically 6k , enabling the amplitude and frequency response to be defined by only a few capacitors and resistors.

The output of the SL480 can be fed directly to any ML920 series receiver and gives a positive pulse. A positive common supply should be used between receiver and amplifier for best noise immunity.

The diode is reverse biased and conducts a small leakage current only, the current increasing as light falls on the diode.

All SL480 series devices accept supply voltages from 5V to 18V and have low current demand, typically 1.5mA.

The overall gain is generous; at least one gain setting resistor should be used to avoid any instability problems.

Applications

Fig.10 shows a typical remote control system for infra-red control of a 10 programme television set. An additional SL490 in the set gives full control from the local position as well as the remote keyboard so push button control of the programmes and color brightness and volume is achieved on set. However, such a system may equally simply be applied to industrial communications or model areas with similar advantages.

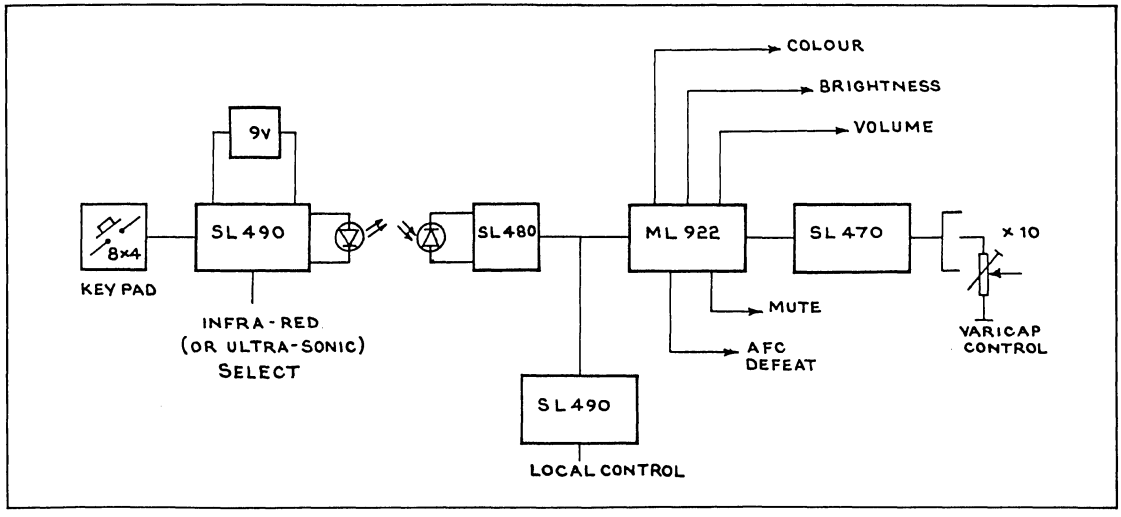


Fig.10 A typical remote control for TV

The transmitter

As mentioned previously a digital pulse modulation system may be used on almost any link; ultrasonic, infra-red, radio or cable. Figs.11, 12 and 13 show how the SL490 may be applied to three different types of link with very few additional components. In Fig.11 low cost transducers may be used and the transmitter carrier may be tuned on pin 18 to the narrow band resonance point. The complementary output of the device gives double the drive to the load. A fixed value of RC timing has been used at pin 16 to give a data rate of about 6 words per second, necessarily slow for a simple ultrasonic system.

The infra-red transmitter (Fig.12) uses a pulse output with no carrier, from pin 2, at a rate of 20 words per second. C3 and R2 allow the complementary pair, TR1 and TR2, to conduct for about 15μs at every negative leading edge of the PPM waveform. Pulse currents of up to 6amps have been achieved with such a circuit but care should be taken to minimise the impedance of the current path. Connections should be made as short as possible and C4 should be a low inductance type.

When simultaneous operation of more than one transmitter is required (e.g. video games, model racers etc.)

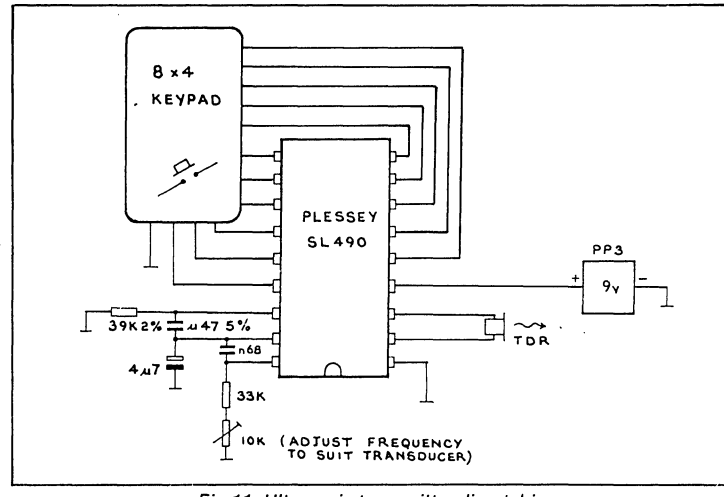


Fig.11 Ultrasonic transmitter direct drive

each signal should be periodically interrupted to allow the other access without jamming. This may be achieved by an externally generated waveform applied to pin 16 of the SL490 or by using the newly developed Plessey Semiconductors Burst Mode Transmitter, the SL491. This circuit has a modified second oscillator on pin 18 to allow multi-transmitter burst mode operation.

In the radio control transmitter in Fig.13 the internal carrier oscillator of the SL490 is inhibited by a resistor of 2.2k at pin 18. The negative pulse output at pin 2 is then used to key a 27MHz crystal controlled oscillator/output stage. The total quiescent current is a few microamps and even when keyed at 50 words per second the duty cycle is only about 15% .

The transmitter will enable both indoor and outdoor operation of various toys and models. A third transistor stage may be used to increase the range.

Various receivers are of course possible, from a multi-channel crystal controlled synthesiser superhet to a three transistor type shown in Fig.14 with just RF amplifier, regenerative detector and output stage which may be directly connected to any ML920 series receiver.

The ML928 remote control receiver is used in this circuit, suitable for controlling tracked models such as military vehicles or earth moving equipment. Either relays (Fig.15) or transistor switches (Fig.16) may be used.

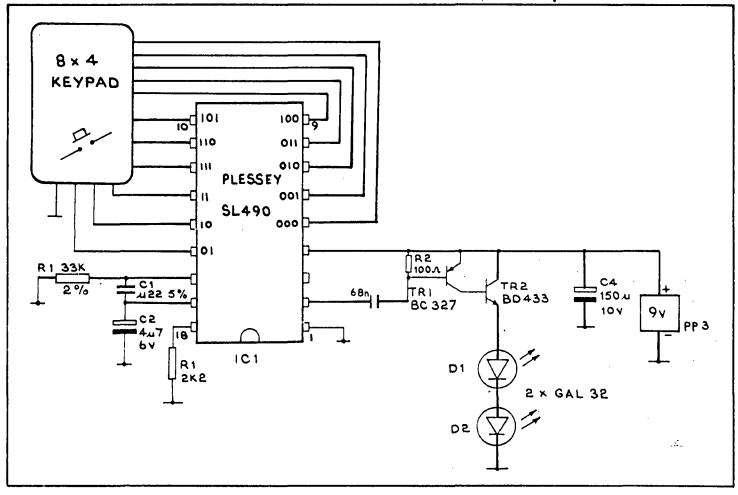


Fig.12 Infra-red transmitter

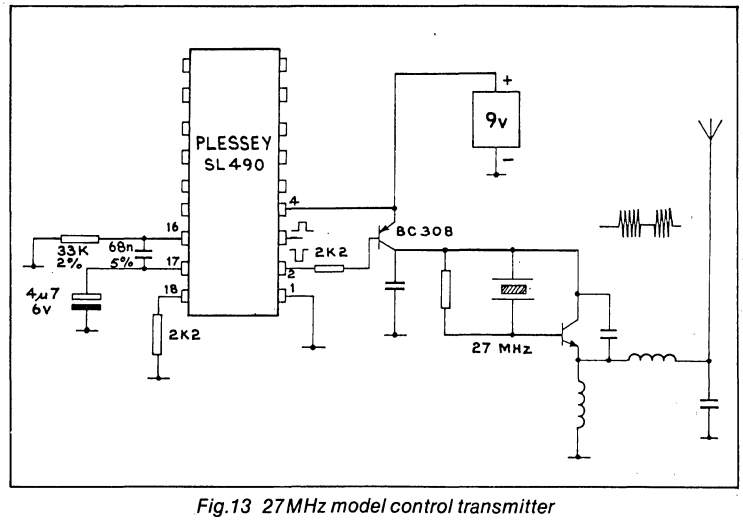


Fig.13 27MHz model control transmitter

Responding to codes 00000 to 01111 only, the ML928 receives and latches 16 or the 32 codes transmitted by the SL490 remote control transmitter. Fig.17 shows how the SL480 interfaces with the ML928.

In the field of military models, the tank is a pacticularly good example of a two-motor application for this circuit. Both tracks can be independently controlled, together with (for example) turret rotation and cannon elevation, giving the model accurate scale operating characteristics and versatility.

However, for a more complex control involving up to three motors, lights, flasher and horn the ML925 can be used.

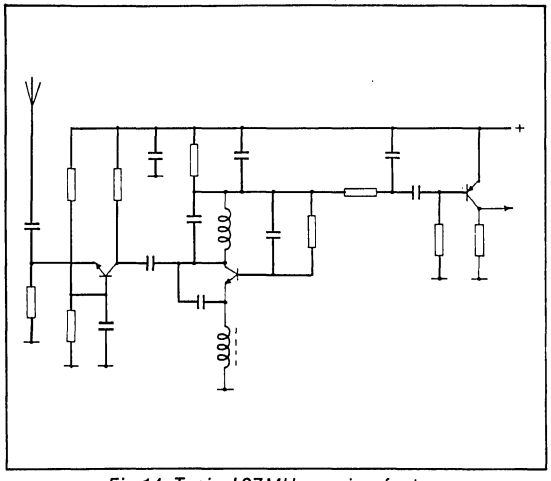


Fig.14 Typical 27MHz receiver for toys

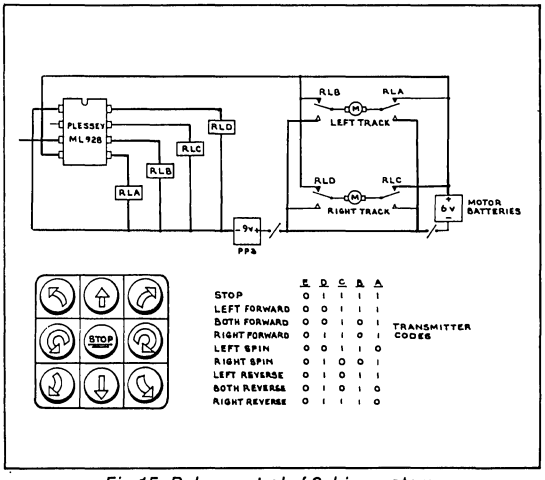


Fig.15 Relay control of 2 drive motors

Time proportional or 3-position steering

Not only does the ML925 give a multi-function control capability but also several working modes are possible. Two similar models may be operated independently with burst-mode transmission and two sets of command.

Fig.18 shows how the ML925 may be used in an infra-red control system for a truck. The supply rail (pin 1), oscillator (pin 2) and PPM input (pin 3) are standard ML920 series specification. Motor control outputs to 'steering' and 'winch' are momentary outputs while 'drive' is a latched outputs. Only one output pin of the motor drive pair will go high at any one time to give a forward or reverse sense and the 'no-drive' condition exsists when neither pin is high.

An additional oscillator at pin 6 is used to give a flashing output at pin 5 or pin 4. It also produces three different chopped waveforms at the 'drive' nad 'steering' outputs so that four different speeds are possible. Other outputs that may be toggled on or off are 'lights' (pin 13) and 'hazard' (pin 4) which gives a flashing signal. 'Flasher' (pin 5) is a permanently flashing signal and 'horn' (pin 18) gives a momentary output. Pin 15 is used to select either one of two command sets for simultaneous control of two toys.

Another type of model may use 3-position steering where a center position is needed as well as full left or full right. Fig.18 shows how this may be achieved very simply with the ML925. The center steering position is marked by an insulated section with positive and negative supply rails at either end. The sense contact is wired to the steering feedback input (pin 14) of the chip which can then quickly decide to center the steering from either full left or full right positions. For this facility the 'vehicle type selct' input (pin 12) is connected to the positive supply.

'Minimum components' ML922

Fig. 20 shows a simple IR television control using the ML922 remote control receiver. The system provides three primary functions; power, programme and sound. Other functions-mute, step (up or down) intersation AFC defeat, interstation mute-are also available if required.

Oscillator timing is set up as usual with a resistor value of about 50K. The exact value is established by preset adjustment.

This circuit, together with a 5-command transmitter (Fig. 12) gives a low component count, low cost remote control system for analogue and digital functions.

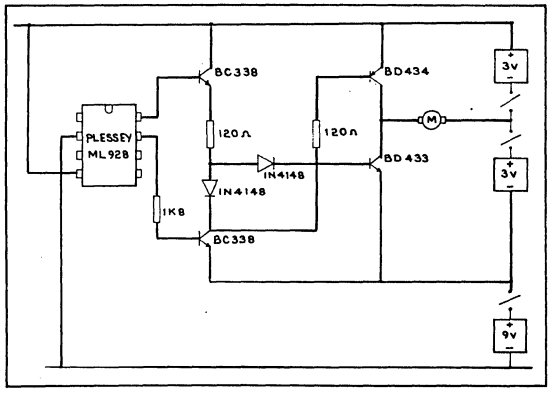


Fig.16 6V 1A transistor motor drive

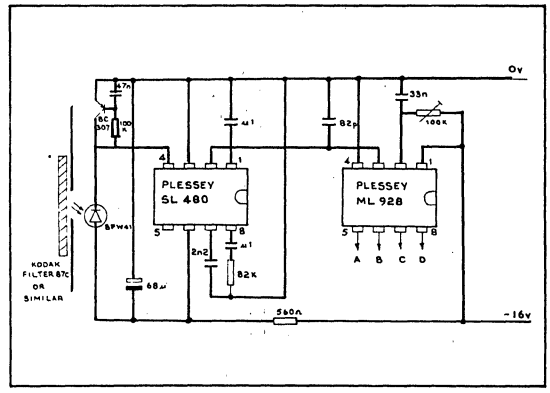


Fig.17 Compact infra-red receiver

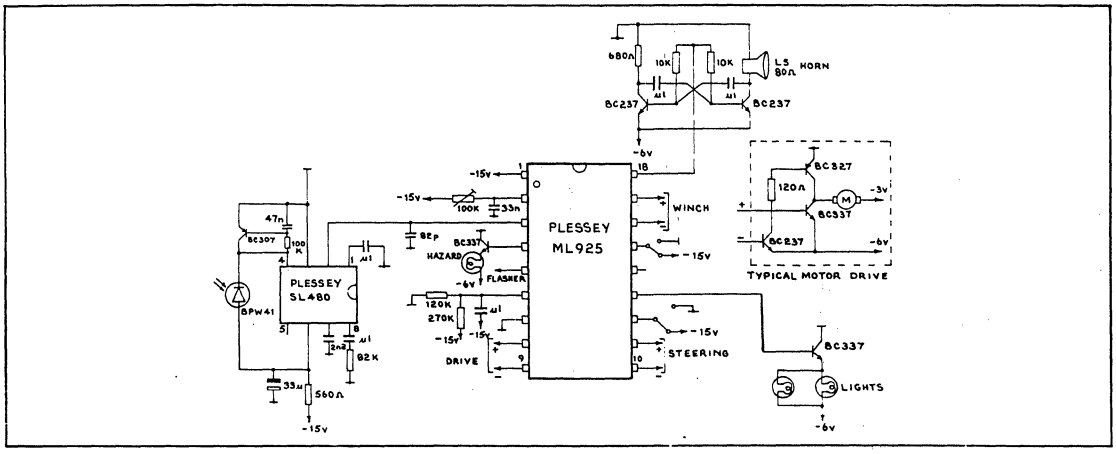


Fig.18 Infra-red drive for car or truck

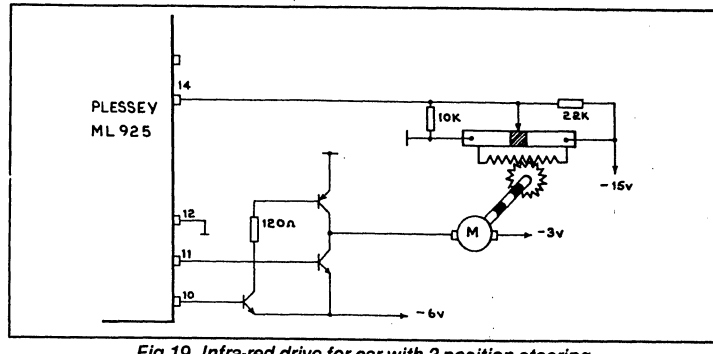


Fig.19 Infra-red drive for car with 3-position steering

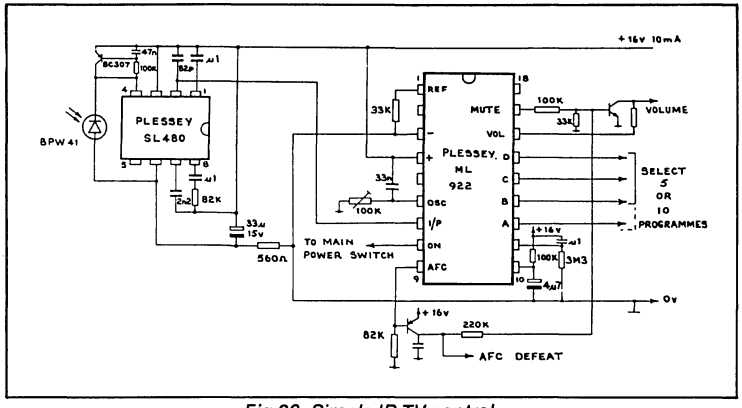


Fig.20 Simple IR TV control

5. ELECTRONIC TOUCH CONTROL

Introduction

Electronic touch selection was initially incorporated into TV tuners to overcome most of the difficulties associated with mechanically interlocked switches such as unstable contact resistance and misoperation of the mechanical latching mechanism. These problems increase as more channels are needed and as electronic varactor tuning was introduced electronic touch selection was a natural, partner development.

The primary requirement of any touch system is to sense the impedance of a finger across two selection contacts. A memory and display facility is then used to remember the last selection made and indicated this state. All previous selections are usually cancelled. Such selection systems have beedn used not only for TV touch tuning but also in FM stereo tuners and AC power control although the major commerical application by far is the TV market especially where European consumers are requiring more than 12 programme sets. The reliability hazard of a multiple interlinked mechanical system becomes acceptable. A single chip solid state solution is very attractive. Such a system will require each TV channel to have

1. A touch sense input.
2. An output for varactor tuning.
3. A channel indicator.

Other facilities required may be stepping mode for a remote control option, the ability of system expansion by cascading units, a muting facility for the sound channel and disabling the AFC during the selection change, a preset state of switch on and possibly a band switching function.

The ML230 Series

Plessey Semiconductors have developed a series of low threshold P—MOS touch control devices to cater for the majority or requirements. MOS integrated circuits are ideally suited to the high impedance input requirements of touch sensing circuits. A higher order of integration is achievable with MOS technology so that all requirements may be realised with a single device. A high noise immunity and a very economic supply current make these devices ideally suited to TV touch tuning.

The basic touch sensing, laching and output configuration is shown in Fig. 1. Apositive sense input normally has a voltage which is more negative than 0.6(V DD-V SS) on one of the channel touch sensing inputs. A simplified representation of the circuit is shown in Figs. 2 and 3. A voltage comparator with a threshold voltage of 0.5(V DD-V SS) is used to set the channel bistable memory and reset all other channels. One output transistor then enables the varicap output line for tuning while the other holds the input at V SS and possible drives an indicator. The varactor supply and output are separated from the main device sensing circuit and slection logic supply in all ML230 series devices, so that nothing need interfere with the tuning voltage regulation. The 'ON' resistance of the varicap outputs in guaranteed to be less than 100ohms at 10mA for devices in the series.

Table 1 shows a range of Plessey Touch Selection devices and lists some of the different facilities they offer.

	ML231B	ML232B	ML236B	ML237B	ML238B	ML239B
Number of pins or package	16	16	24	18	24	24
Number of channels	6	6	6	6	8	8
Neons[2]	Yes	Yes	Yes	Yes[1]	Yes	Yes[1]
LEDs[4]	Yes	Yes	Yes	Yes[3]	Yes	Yes[3]
Sensitivity, R_F (100M, Mains)	Yes	Yes	Yes	Yes	Yes	Yes
(50M, High DC)	Yes	Yes	Yes	Yes	Yes	Yes
(20M, V_{SS} DC)	Yes	Yes	Yes	Yes	Yes	Yes
Channel Selection, +ve	Yes	Yes	Yes	—	Yes	—
−ve (GND)	—	—	—	Yes	—	Yes
Stepping Facility	—	Yes	Yes	Yes	Yes	Yes
Mute O/P	—	—	Yes	Yes	Yes	Yes
Clear I/P	—	—	Yes	—	Yes	Yes
Cascadable	—	—	Yes	—	—	—
Channel Selected, Power Up	3	Any[6]	Any[6]	1	1	1
Band Selection[1]	Yes	Yes	Yes	Yes	Yes	Yes

NOTES
1. Neons with a ± 10% tolerance on striking voltage.
2. Neons with a ± 20% tolerance on striking voltage.
3. LED's used at a current below 5mA.
4. LED's used at a current below 10mA.
5. With Neons or LED's at reduced sensitivity.
6. Some external components are required.

TABLE 1. ML230 Series

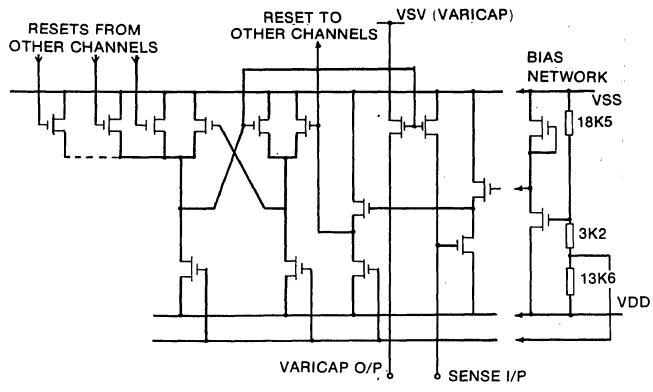


Fig. 1 Basic channel arrangement of a multichannel touch selection device.

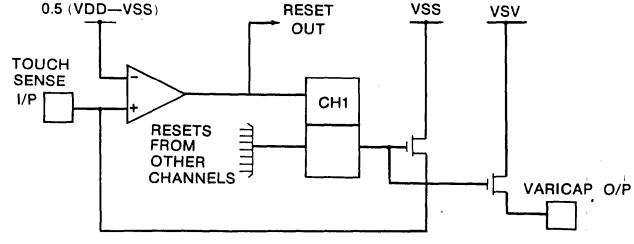


Fig. 2 Part of a touch control showing channel 1 only.

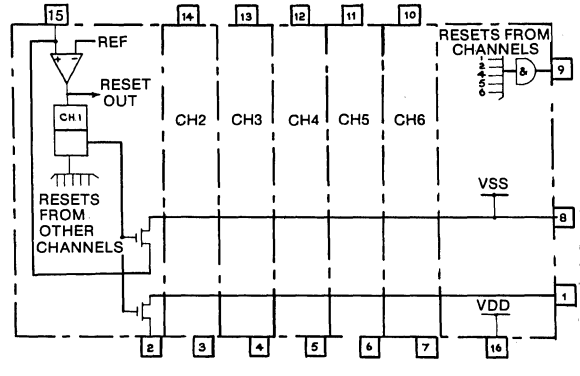


Fig. 3 Basic 6 channel touch selector, ML231.

Design considerations

The ML230 series of integrated ciruits can be easily designed into many applications and internal protection is included, but resonable care should be taken as with any other MOS device particularly before and during connecting the device to the external circuit. The independant V_S varicap supply should not exceed V_{SS} and for optimum drive should not be less than V_{SS} -0.7V. All devices are tested at 30V and 36V and some applications exist where successful performance has been achieved with $V_{SS}-V_{DD}=16V$.

Touch Sensing

The requirement of the touch sensing inputs is to sense safely a finger resistance which could be over 20Mohms. BS415 suggests a comfort limit of 0.3mA peak and specifies a safety limit of 0.7mA peak current flowing between any accessible conductor (in this case the touch plates) and any other externally fed conductor (in this case 240V 50Hz). Thus a minimum resistance, R1, can be calculated:-

$$R1 = \frac{240 \times \sqrt{2}}{0.7} \text{ k ohms}$$

$$= 485 \text{ kohms}$$

Also the maximum leakage of the ML230 series inputs is specified as 1μ A, the input leakage resistor, R1, in Figs.4(a) and 4(b) has to pass this leakage current without allowing the input of the device to approach too closely to the sensing threshold.

Minimum input threshold voltage=0.4 (V DD−V SS). Choose a safe limit of input voltage, e.g. V DD+10V.

$$R1 = \frac{10V}{1\mu A} = 10\text{Mohm}$$

Fig.4(a) shows how a touch sensing circuit may be arranged to operate using the 33V or so of the device supply. R2 and R3 are both safety components needed in the case of unisolated, usual, television chassis arrangement. A lower finger resistance will be needed to be sensed by such a low voltage circuit. Let this maximum worst case finger resistance be Rf. Then for sensing at the highest threshold:-

$$\frac{Rf+R2+R3}{10} = \frac{0.4}{0.6}$$

Therefore Rf =5.5M

This sensitivity is adequate if good touch contacts are used but he arrangement shown in Fig.4(b) will provide better sensitivity. In this case

$$Rf + 16.8 = \frac{240\sqrt{2}}{2}$$

Thus Rf = 150Mohms

It will be noted from Table 1 that two devices. ML237 and ML239 are available for touch selection by a negative potential. These circuits overcome any difficulties experienced in selection when the user is statically charged due to a dry atmosphere and carpeting of a synthetic fibre material. Problems in selection associated with a low impedance ground path such as when the user is in contact with a metal radiator can be solved by ensuring that devices have their inputs conditioned towards ground when they are being selected.

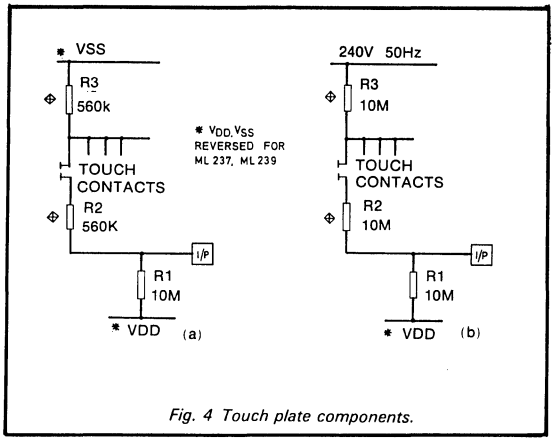


Fig. 4 Touch plate components.

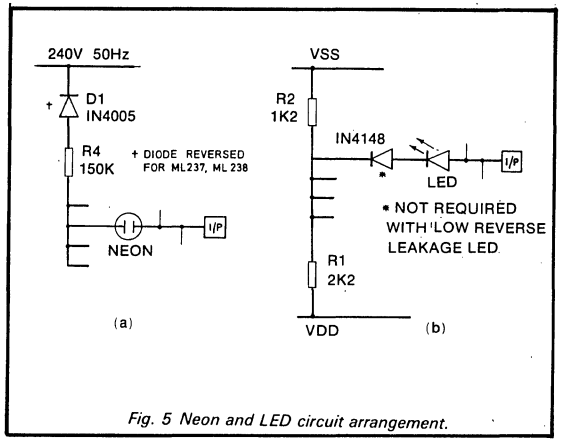


Fig. 5 Neon and LED circuit arrangement.

Channel Indication Using Neons

Miniature wire ended neons can easily be used as channel indicators. The ML230 series incorporates low impedance current driving elements operating on the channel selection inputs. This means that the outputs to the tuning voltage presets need be used for any other function. This isolation gives better tuning stability. Fig.5(a) shows how easily a neon such as Hivac 3L type can be incorporated into a mains voltage touch sensing arrangement similar to that shown in Fig.4(b). The direction of the diode will be reversed for negative touch sensing circuits ML237 and ML239. Neon indicators are cheap and only demand a current of 0.3mA to 1mA to fully illuminate a miniature wire ended type. They do however, require a high voltage supply in order to strike satisfactorily. To add a neon indicator to the touch circuit shown in Fig.4(a) a supply of 150V and a series resistor 0.7mA. When using neons with lower voltage touch sensing circuits care should be taken that the neon striking does not degrade the touch sensitivity . A neon 'hold off' transistor may be required, particularly with the ML237 and ML239 negative sensing circuits when low voltage touch sensing is used. Such a circuit is shown in Fig.6. Immediately the input voltage falls below the threshold due to a finger resistance across the touch contacts, a mute pulse is generated which turns on the BC546 transistor. With this transistor on, the voltage across the neons is reduced to 33V and all neons are extinguished. After the mute pulse the BC546 transistor turns off and allows the new channel indicator to strike across the full 103V supply. The transistor switch thus ensures that all previous indicators are cleared and no leakage paths exist to interfere with the new selection.

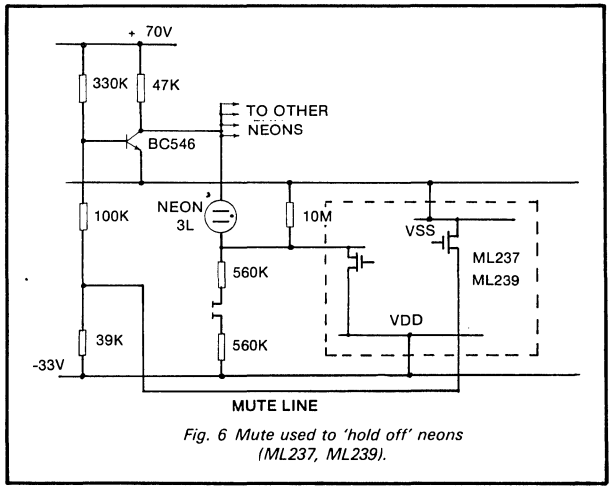


Fig. 6 Mute used to 'hold off' neons (ML237, ML239).

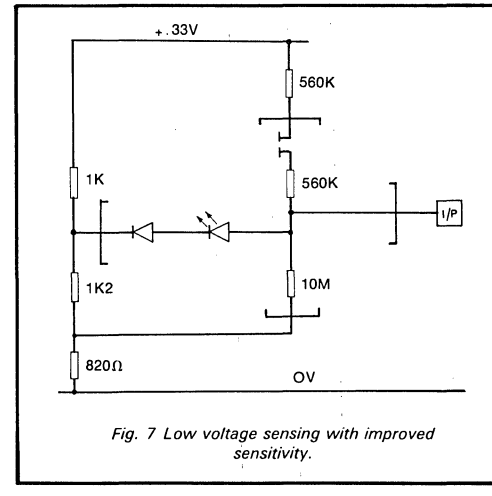


Fig. 7 Low voltage sensing with improved sensitivity.

LED Channel Indicators

LEDs can easily be used as channel indicators provided that the maximum drive current is not exceeded. As can be seen from the data sheets the 'ON' resistance of all ML230 series varicap outputs is less than 100ohms at a current of 10mA. The input 'ON' resistance is a maximum or 250ohms at a current of 10mA except when using the ML237 and ML239 when the maximum current is 2mA. Thus LED's can be driven at 10 or 12mA from the outputs or a current of 4 or 8mA may be used from the input pins in the case of the ML231, ML232, ML236 and ML238.

Fig. 7 shows a low voltage sensing circuit with LED indicators. The LED current is defined by the 1.2K and 820ohm resistor as about 10mA. An offset voltage is fed from 920ohm resistor via the 10M leakage resistor to the input. This offset voltages of 11.8V in the case of Fig. 7 increases the touch sensitivity to 20Mohms. The diodes supplement the reverse characteristics of the LED's. The 1k resistor sets a voltage of 0.6 V SS on this diode, to reverse bias it when no channel is selected. This is important at turn or when the ML236 is cascaded, because LED leakage could cause spurious selection.

The difficulty in using the ML237 or ML239 inputs to drive higher current indicators is due to the fact that the MOS transistors used as source followers given an appreciable voltage drop. This could lead to the channel selection threshold being exceeded and so channel selection would not be stable. Fig. 8 shows an example of such an input characteristic. More current than the guaranteed 2mA may be sunk by the input, but as the voltage increases towards the threshold, stable selection becomes more difficult to maintain. The load lines shown given an indication of the series resistance required, but is should be remembered that Fig. 8 is only an example and not typical of all devices. Also, the threshold voltage specification is 0.4 to 0.6(V $_{SS}$-V $_{DD}$).

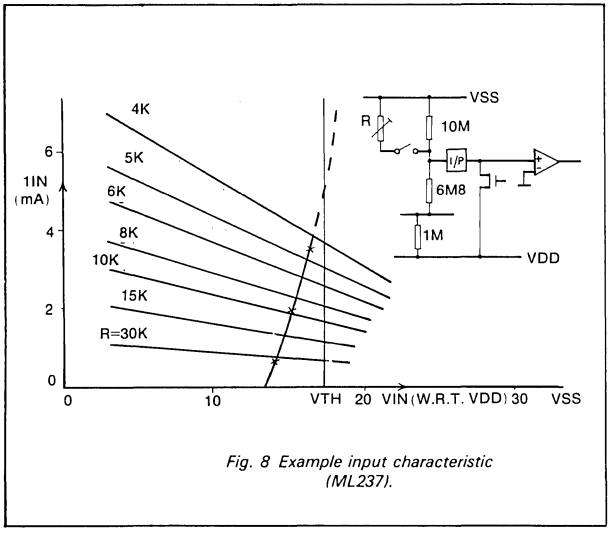


Fig. 8 Example input characteristic (ML237).

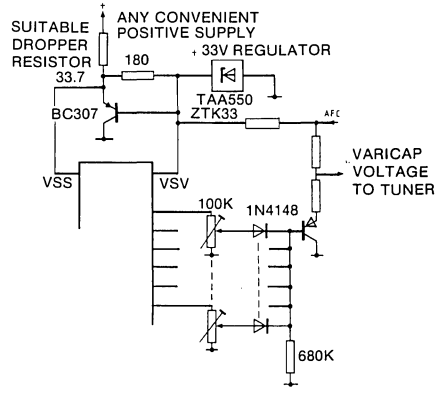


Fig. 9 Varicap Supply and Selection.

Varicap voltage switches

All ML230 series devices are guaranteed to have an output resistance of less than 100ohm for their varicap output switches. This means that excellent regulation can be maintained for the varicap output voltage. As mentioned previously the varicap supply, V SS, is brought out to a different pin Fig. 9 shows the simplest arrangement that allows different tuning voltages to be present using the 100K variable potentiometers. Only one MOS switch is shown and only 3 channels, but 6, 8 or more channels can be accommodated. However many channels are used only one MOS switch wil be 'ON' at any time. The diodes allow the potentiometer settings to be independent of each other. One idea for temperature compensation is shown, but a number of systems can be used to compensate for not only the varicap drift and the varicap supply stability but also the 0.5V/ o C or so change in voltage across the MOS switch and the 2.3V/ o C of the diodes. Forward biased diodes, zener diodes and thermistors may all be utilised for best temperature stability.

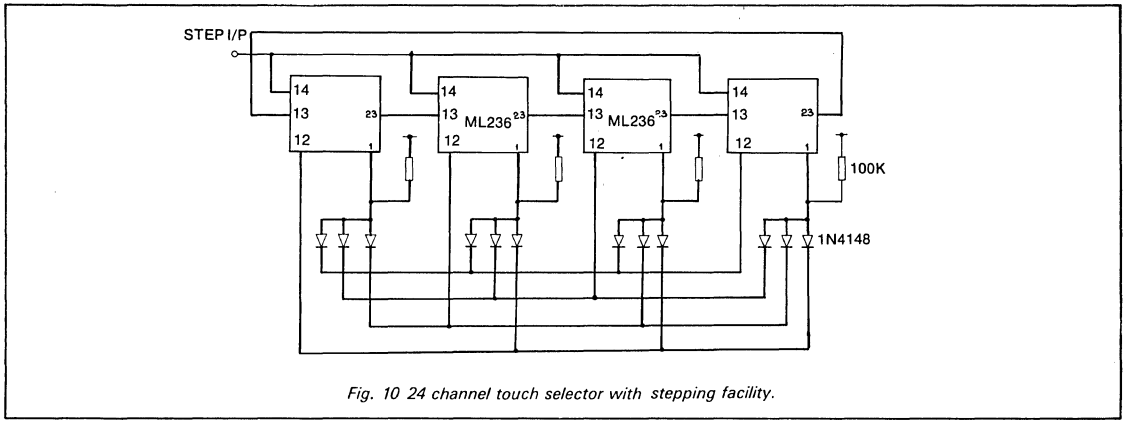


Fig. 10 24 channel touch selector with stepping facility.

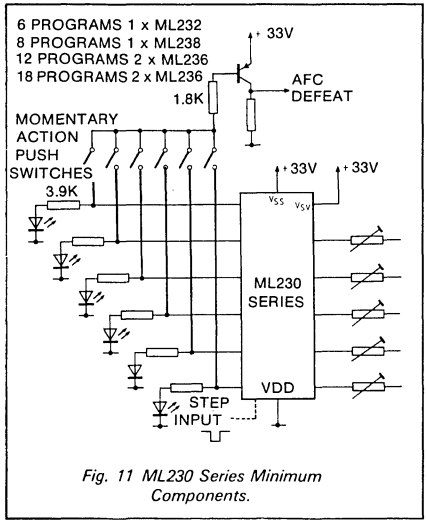


Fig. 11 ML230 Series Minimum Components.

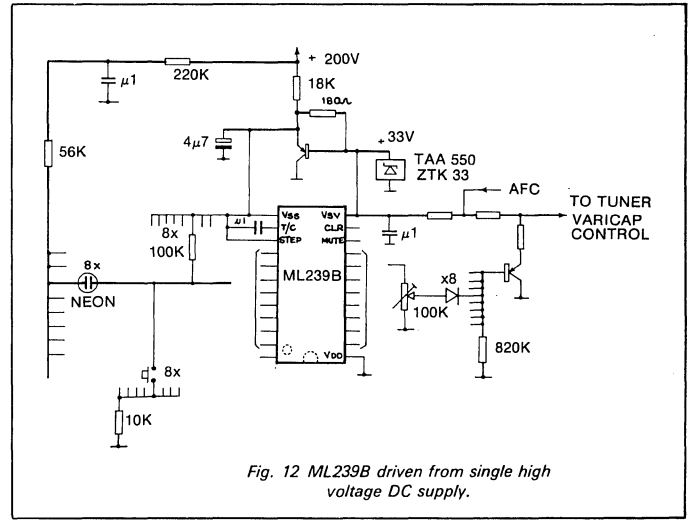


Fig. 12 ML239B driven from single high voltage DC supply.

A universal application

Appendix 1 contains a printed wiring layout, circuit configuration and component details for a positive or negative touch selection application using LED's or neons respectively. Most of the component details have been covered previously and either circuit can be easily adapted for other slightly different requirements.

Included in the ML236 data sheet is an application circuit for a 12 channel touch selector using 2 devices. Fig.10 clearly illustrates how any number of ML236 devices may be cascaded, diodes will be needed if more than 2 devices are cascaded.

Fig.11 incorporates an AFC defeat function when momentary action push switches are used. Very few components are needed for this configuration which offers all the main facilities.

The circuit in Fig.12 only requires a single supply for neon, chip and varicaps. A shunt regulator controlled from the varicap zener feeds the chip and the varicap tuning voltage out is temperature compensated.

ML238 application circuit

It will be seen from Appendix 1 that the ML238 circuit uses a low voltage (33V) touch selection supply with improved sensitivity circuitry. The mute time constant capacitor of 22nF gives a mute time of about 18ms at a V_{SS} of 33V. When a stepping input applied the mute time is increased by the width of the stepping pulse. Some temperature compensation is afforded by the diode connecting the lower end of the preset potentiometers to chassis. An added facility not previously mentioned is the band selection circuitry for

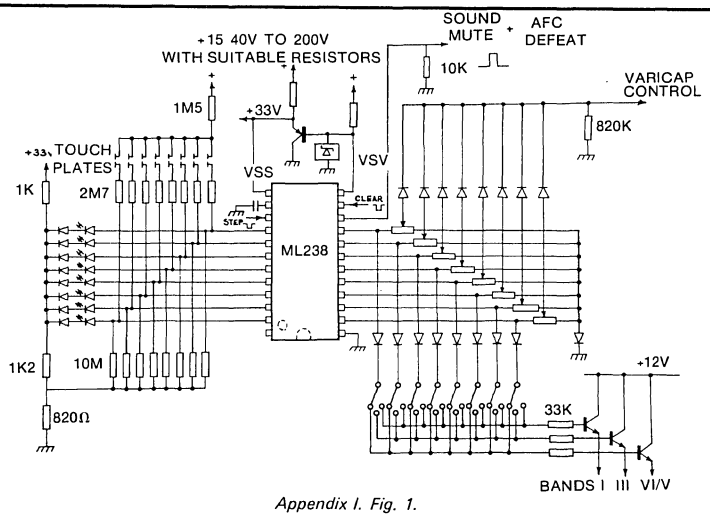
multi-tuner arrangements. The set of 3 way switches allow band I III IV/V to be selected automatically for any channel via the 3 emitter followers.

ML239 application

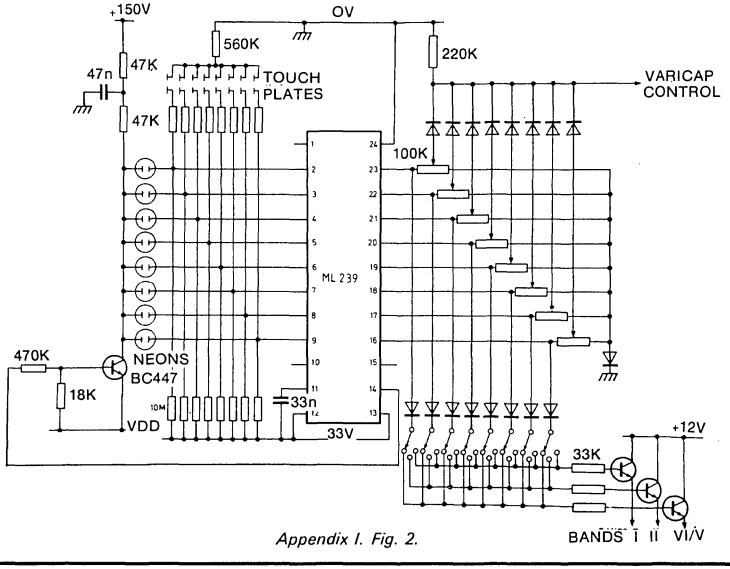
Appendix 1 gain shows a low voltage touch selection supply for this device. A new selection is made when an input becomes more negative (towards chassis) and falls below the input threshold. Thus this device in this application will not only switch when the user has a high (negative) static charge, but will also switch satisfactorily when the user is at ground potential (due to contact with a central heating radiator say).

A 150V DC supply is used for the high intensity neons because such neons have a high striking voltage. A high voltage transistor, turned on by the mute output is ued to turn off all indicators during a channel change. This transistor has to withstand the full neon striking voltage and also survive if no neon is on, during start up for instance. The BC447 transistor used has an 80V BV_{CBO} and BV_{CEO} . Also it is used with an 18k base-emitter resistor. The touch sensitivity is not quite as good as the previous application and so the touch plate resistors are kept low at 560k, the minimum allowable by the safety limit.

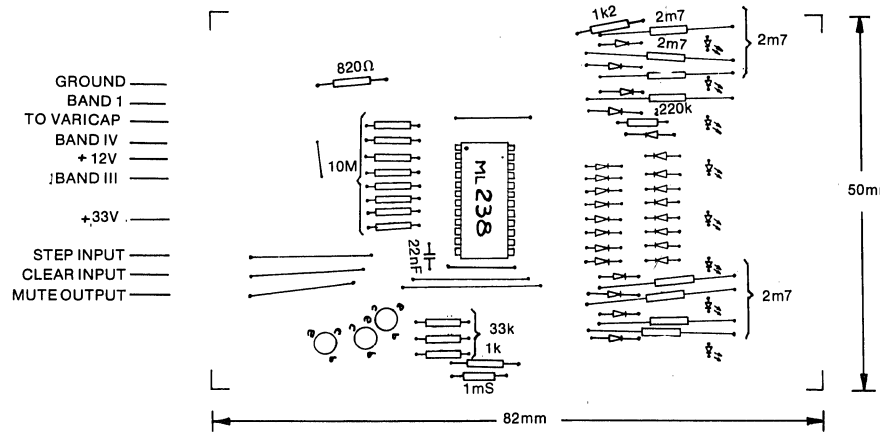
Appendix 1



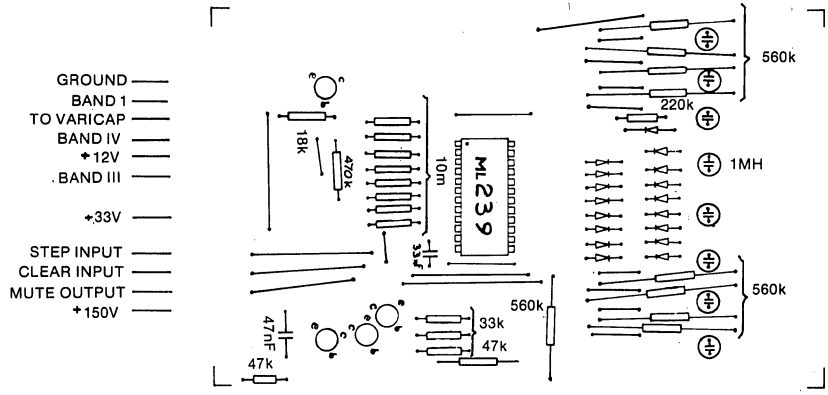
Appendix I. Fig. 1.



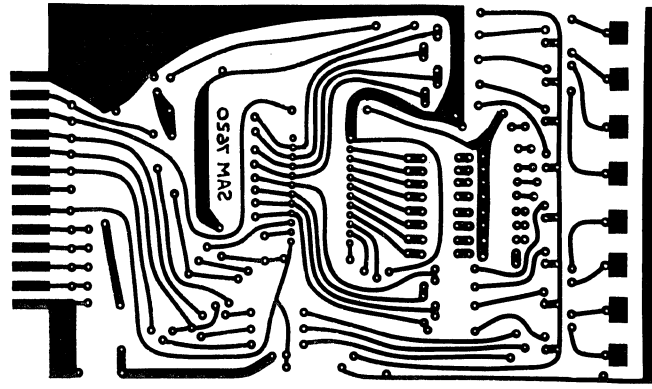
Appendix I. Fig. 2.



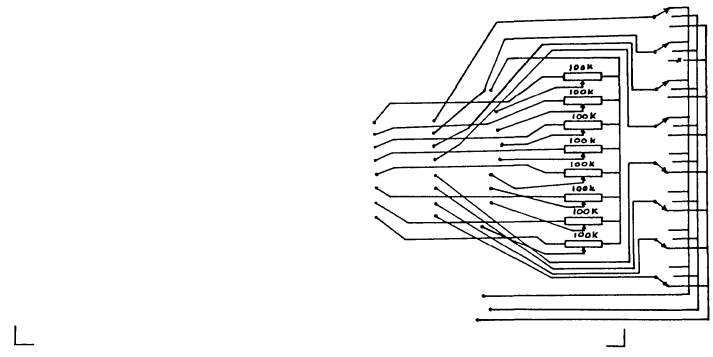
Appendix I. Fig. 3.



Appendix I. Fig. 4.

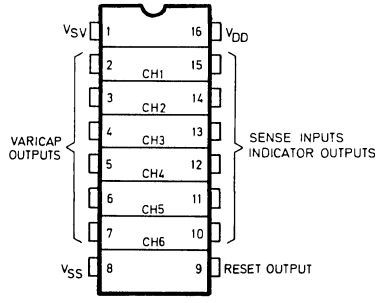


Appendix I. Fig. 5.

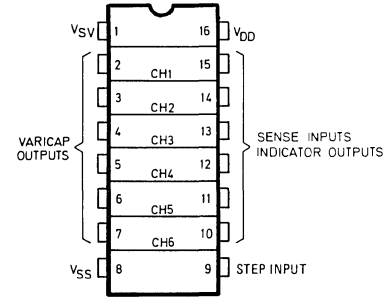


Appendix I. Fig. 6

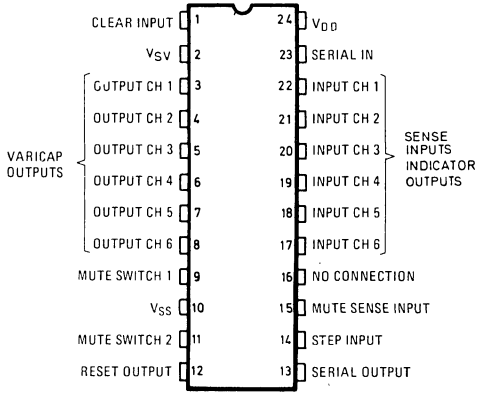
Appendix 2: Pin Connection Diagrams



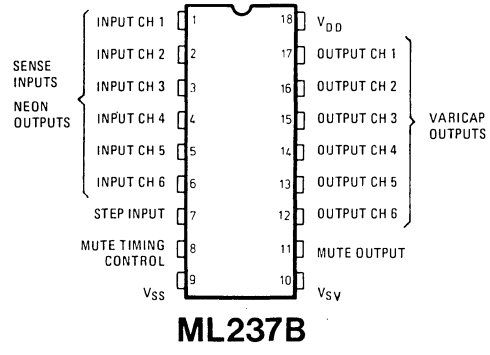
ML231B



ML232B



ML236B



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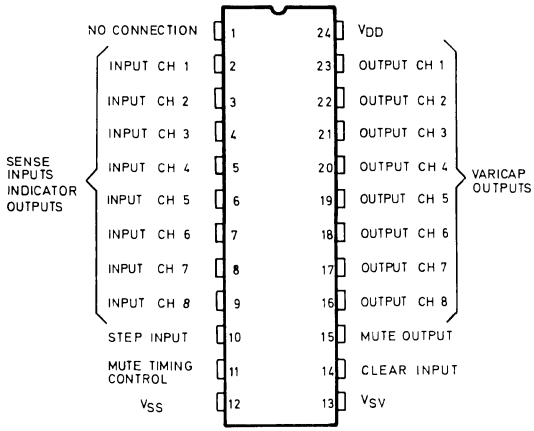

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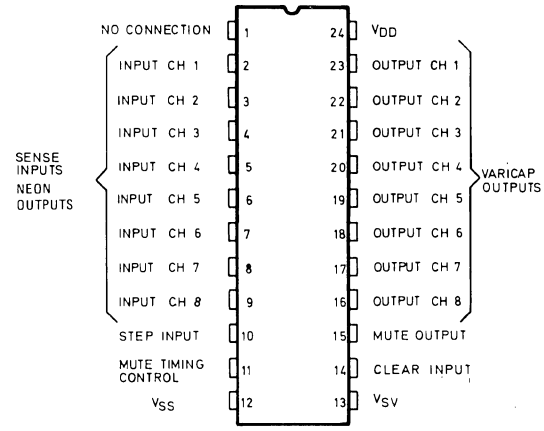


ML239B

6. REMOTE CONTROL USING PPM

Introduction

Plessey Semiconductors have developed and produced two integrated circuits that when combined give on e of the most flexible remote control systems on the market. The SL490 is a pulse-transmitting remote controller, for use in conjunction with the ML920 receiver.

Methods of control can be achieved by cable, sound, ultrasonic, visible light, infra-red or radio frequency.

On a television set, it is possible to control the Brightness, Volume and Color in 32 steps from minimum to maximum. In addition, facilities for Sound Mute, Color Kill and Normalise, as well as a number of other options which will be fully described later, are incorporated within the system. The system can be used with Television having 8,10,12,16 or 20 programme selections. If more than 20 selections are needed, the system is easily expanded.

Commands are transmitted by codes via a pulse position modulated signal. The SL490 can give a modulated carrier frequency from the on-chip oscillator. This on-chip oscillator, used for carrier generation, is selectable so that pulses with or without a carrier frequency may be transmitted.

The Pulse Width/Modulation Rate is variable, and PPM results in:-

(i) An economy of Channel Width

(ii) A greater number of Commands Binary Codes, transmitted in a Pulse Position Modulated Signal help in ensuring that incorrect signals do not operate the receiver. 5 bits of information contained within 6 pulses are transmitted and when detected by the receiver are checked. Pulses must be of the correct pulse width, in the correct position, the gap between words must be as designated, and finally, two identical words must be received before the receiver is allowed to action the sinal.Consequently this system is virtually immune to incorrect signals.

As current is conducted only when a contact is made by a key switch, negligable power is consumed from the battery in the transmitter, thus ensuring that battery life is nearly as long as shelf life.

A whole series of domestic appliances may be controlled by just one transmitter. For example, since the remote control system can be used for Television, Radio/Tuner, Tape/Recorder Decks. Garage Doors etc., then with just one transmitter the following can be controlled remotely:-

(i) the garage doors may be opened.
(ii) a porch light may be switched on
(iii) a radio, tape recorder or television may be switched on and the desired programme selected.
(iv) cooker hotplates or oven setting may be adjusted.

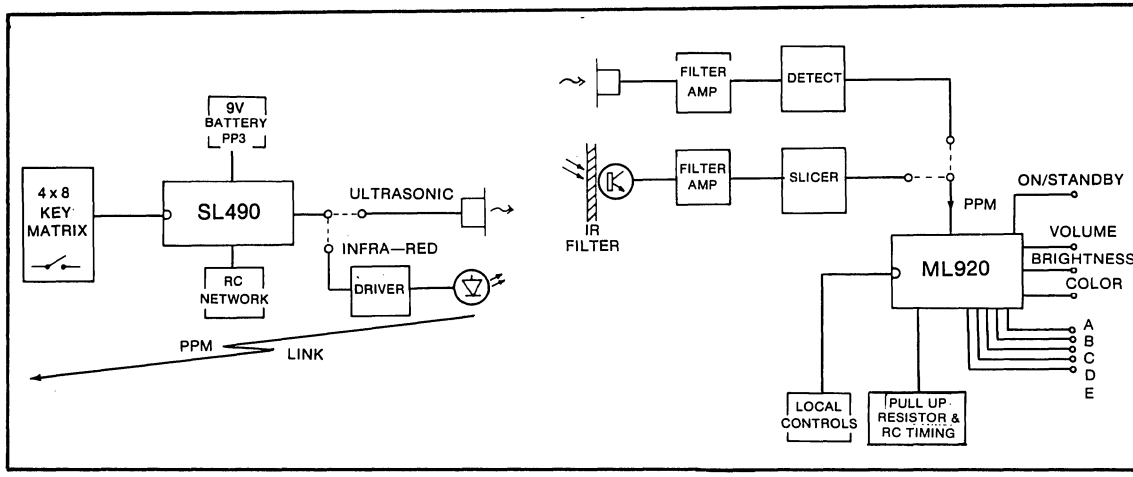


Fig. 1. Plessey Remote Control System Block Diagram

Other Possibilities

(1) An automatic telephone answering machine can itself be commanded to relay all its messages over the telephone, instead of having to manually play-back the telephone messages.

(2) The Remote Control of Toys and Models.

(3) Industrial Control e.g. may be used to trigger, interrogate, and transmit back information from a sub-station to the Main station, so that data can be analysed and appropriate actions carried out.

In general, all systems that have in the past relied on some method of manual triggering such that infromation, data etc. can be recorded and perhaps appropriately actioned, can noe be remotely triggered and remotely actioned.

The Transmitter Unit

The SL490 though initially designed with TV remote control in mind may be used whenever a compact pulse coded digital transmission system can be realised. A basic 5-bit code is used giving 32 code words which can be modulated as pulse position modulation (ppm) onto a single carrier frequency or transmitted as baseband pulse position modulation. Fig.1 shows how an ultrasonic or infra-red link may be used to control 3 analogue settings, select up to 20 channels and give 6 other control functions by using an SL490 ppm transmitter and a ML920 ppm receiver. The SL490 could equally well be used to drive a cable link or a radio link.

Only single pole switches are needed in the key matrix and fairly high 'on' switch resistance may be tolerated. The transmitter has a very low standby current (leakage only), and a transmission is economical on power due to the design and low duty cycle of pulses fed to the load. An ultrasonic transducer may be fed directly using only 2 resistors and 3 capacitors external to the device. Thus, small battery, ahnd held, portable operation is easily implemented and low cost ultrasonic transducers may be used at their natural resonant frequency.

For infra-red operation, a 2 or 3 transistor amplifier is used to feed very narrow high current pulses to a gallium arsenide, infra-red emitting diodes, such as the Plessey GAL32. If a higher output is required, 3 or 4 GAL32 diodes can be used in parallel. The pulse nature of the signal allows the diode emitter to work at a higher light output efficiency and the battery current to be reduced. Figs.2,3 and 4 show the output voltages waveforms obtainable. Fig.2 shows a lower than normal carrier frequency compared to the pulse width. This is done for clarity although the device would operate satisfactory with such timing.

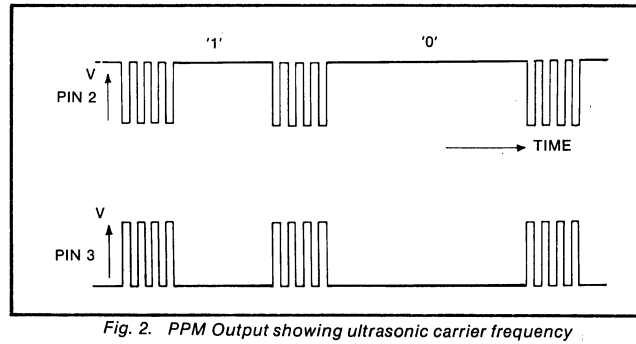


Fig. 2. PPM Output showing ultrasonic carrier frequency

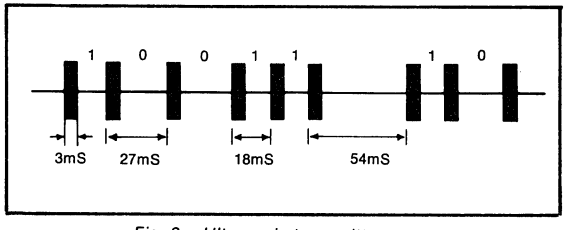


Fig. 3. Ultrasonic transmitter output (For A '1' period of 18mS)

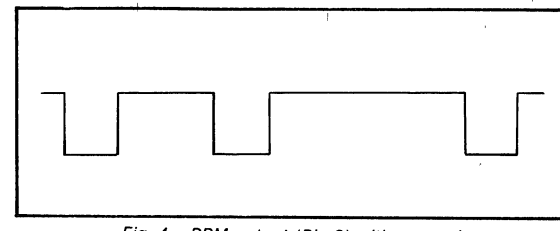


Fig. 4. PPM output (Pin 2) with no carrier

The Receiver Amplifier

At the receiving end of the link, the system will require some sort of gain and bandwidth defining stages, before the detected signal is fed to the ML920 receiver. Usually 2 or at the most 3 amplifier stages are sufficient with some fairly simple active filtering, and in the case of the infra-red link, an infra-red filter, required before the photo transistor. After filtering and amplifying the ultrasonic frequency, a simple diode detector may be used. The detected PPM can then be fed to the ML920 via a buffer amplifier stage. Fig.5 shows how an ultrasonic frequency of 33KHZ to 43KHZ may be chosen to avoid the second and third harmonic of the TV line output stage.

An inexpensive transducer may be chosen with its natural resonant frequency within this band, and driven at its natural resonance which simplifies loading and improves power output. The actual bandwidth needed about the carrier is approximately 10KHZ. The data rate may be chosen by considering the rate at which the analogue outputs of the ML920 are required to step. If for example we require an analogue output to sweep its full range (32 steps) in about 10 seconds, this requires one step every 300msec or so, but because of the receiver error checking code comparator, the transmitter word rate should be set to 150msec.

Referring to Fig.3, it will be seen that the code word period including the inter-word space is 162msec which will give the required analogue change rate, full range in about 10 seconds. The only adjustment needed in the receiver is to set the oscillator time constant, so that 20 time periods on the receiver monitor, (pin 9), corresponds to a '0' interval of the incoming PPM (see Fig.6). The demodulator timing oscillator frequency tolerances of up to 10% in both the transmitter and the receiver. This can be seen from the timing window durations of Fig.6.

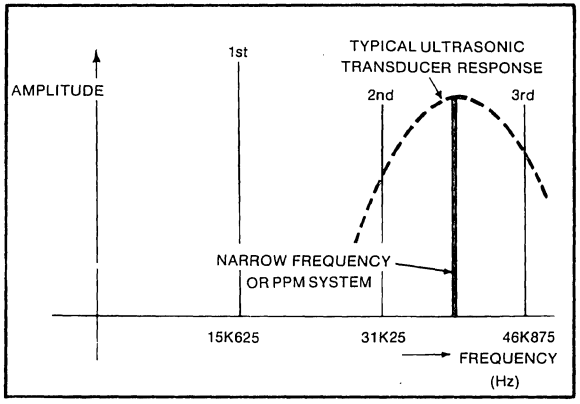


Fig. 5. Ultrasonic transducer reponse with line frequency and its harmonics

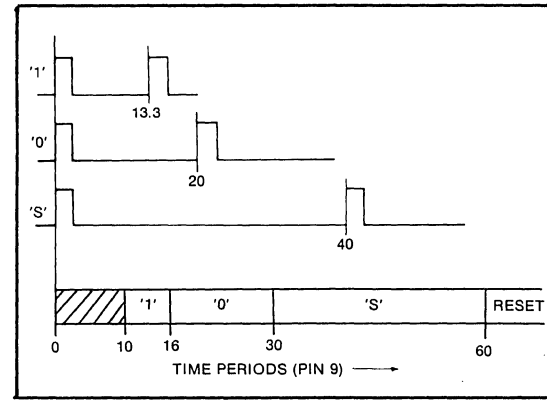


Fig. 6. PPM Demodulator timing

An infra-red link

For short range remote control, infra-red links have advantages over ultrasonic links-less multipath interference, lower spurious radiation, less annoyance to humans and animals, a higher modulation rate capability and more robust transducers. High efficiency infra-red light emitting diodes (LED) are relatively inexpensive and can incorporate both reflector and lens for a more concentrated beam light. Multichip assemnlies are also becoming more common and these can take fairly high currents. LED's become more efficient at higher currents, and pulse an d multiplex systems are common for display systems. Thus a PPM system can be made to operate a LED at quite high outputs for small increase in battery current. More than one LED may be connected in series at lower currents and in parallel at higher currents, and these emitters can have different orientation of their axes if required.

On the receiver side, a photo diode or photo transistor can be used with an appropriate infra-red filter. Fig.7 shows how a photo detector response, although peaking in the near infra-red region, has good detection properties at visible light wavelengths and into the ultra-violet. As the energy emitted from a gallium arsenide LED is in the main a narrow band emission at 940nm, a correctly chosen filter will attenuate greatly most of the interferring noise signals. Other noise sources which have large emissions in the infra-red e.g. a tungsten filament lamp, can be rejected by carrier modulation of the infra-red link.

Both amplitude modulation and frequency modulation have been used, but neither have simplicity nor all the advantages that a pulse system can offer in LED driving efficiency and economy of detection. Pulse Position Modulation using a narrow pulsed high current drive to a gallium arsenide LED, enables a very good signal to noise ratio to obtained at the demodulation. Only photo-detector saturation (in very bright sunlight for example) or the very close proximity of a high output fluorescent gas discharge tube could cause the reception to be interrupted.

SL490 - remote control receiver

General description

The SL490 ia an 18 pin, bipolar, remote control pulse transmitting monolithic circuit for use with the ML920 Receiver Single pole switches arranged in a 4 x 8 matrix or 12 keys (1 out of 4 and 1 out of 8) are encoded by the device which then gives a modulated carrier frequency from an on-chip oscillator. A standby current of only 6uA or so is taken from a 9V supply by the device until any switch closure is detected. (A PP3 battery can have a battery life of about two years in this system). The modulated output can drive an ultrasonic transducer directly at its natural resonant frequency, enabling inexpensive crystals to be used. A 5 bit pulse position modulated signal is used giving 32 basic commands. These commands could be used in a TV remote control system to select 20 programs, control 3 analogue functions and provide 6 additional switching functions. Apart from the battery, switch, matrix and transducer, only 3 capacitors and 2 resistors are needed externally. A single RC selects carrier options and defines frequency. The other RC defines modulation rate. Output capability is direct ultrasonic transducer feed, and complimentary outputs with or without active pull ups. Continuous or pulsed visual indication can be driven directly from pin 2. Carrier oscillator may be disabled for pulsed operation of infra-red. More than one set of 32 commands may be utilised by changing modulation rate/carrier frequency.

Despite the comprehensive range of facilities offered by this remote control system, the SL490 makes the transmitter a very simple unit. Fig. 8 outlines the block diagram of the transmitter.

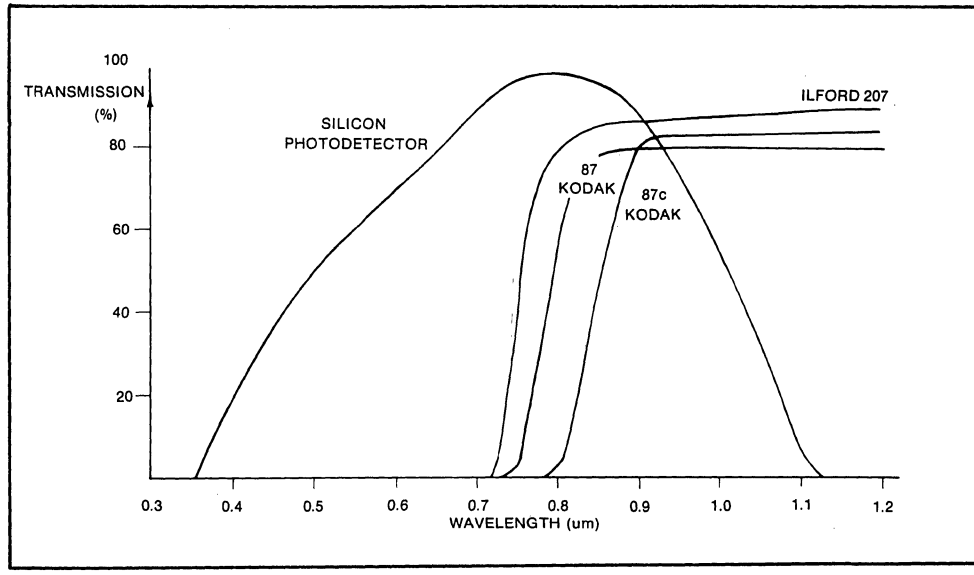


Fig. 7. Optical Response Characteristics

Circuit operation

The device transmits a code word as a group of 6 pulses. Each of the five intervals between these pulses may take up 2 possible values, a short interval corresponding to a '1' OR A LONG INTERVAL CORRESPONDING 1' or a long interval corresponding

to a '0'. Fig.3 shows the timing relationship between pulses '1', '0' and 'S', the space or synchronisation gap between words. The ratio of the intervals representing '1','0' and 'S' is 2:3:6 and is fixed by the device. In addition the width of the pulse is about 1/6th of '1' interval or 1/3:2 on the above ratio scale. Thus 32 different codewords may be transmitted by the 5 bit code.

A particular codeword is selected by switching one out of eight current sources to one out of four current sinks (one of these current sinks is 0 Volts). All decoding is done by the integrated circuit, (see Fig.10). The circuit draws only about 6uA from the supply until a switch closure is detected. Power is then applied to the whole circuit. The appropriate PPM code is then generated repeatedly until the switch is released, whence, the device reverts to standby, after the codeword being transmitted is completed.

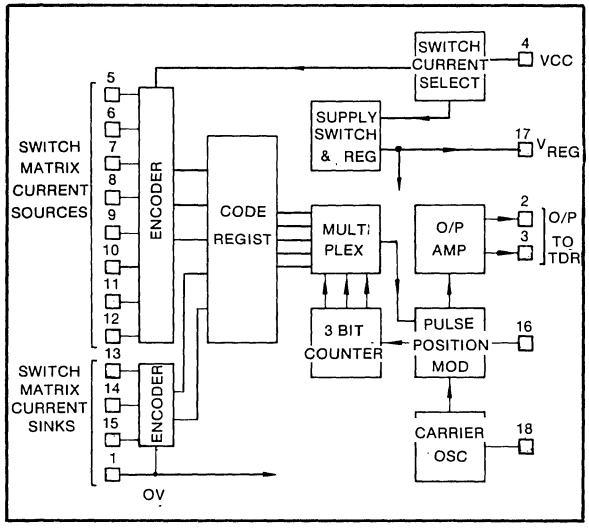


Fig. 8. Transmitter SL490 Block Diagram

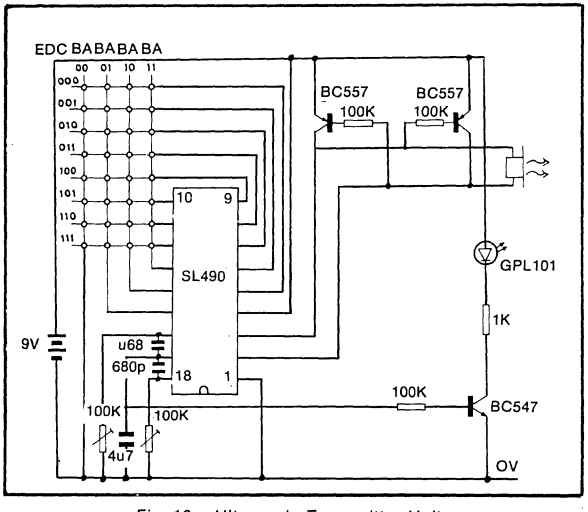


Fig. 10. Ultrasonic Transmitter Unit

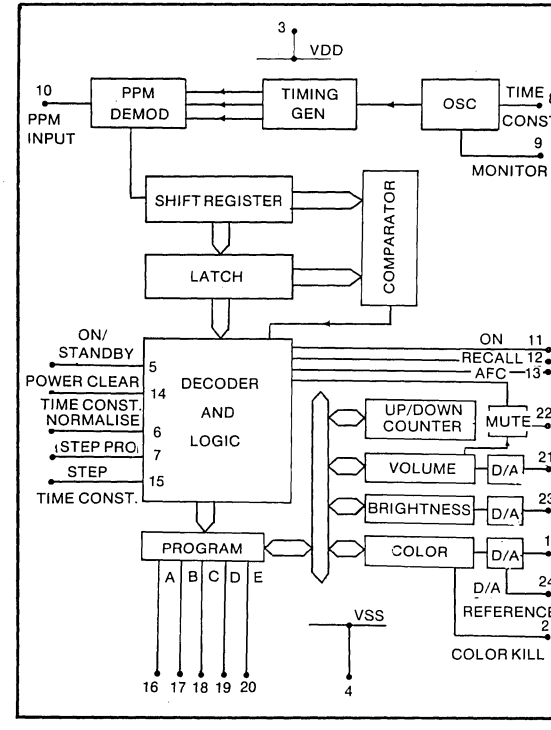


Fig. 9. Remote Control Receiver ML920 Block Diagram

ML920 - remote control receiver

General description

The ML920 is a 24 pin PMOS/LSI monolithic circuit, designed to decode the 32 possible 5 bit codes transmitted by the SL490. It functions as a remote control receiver of pulse position modulated signals. After demodulation, verification and comparison of 2 consecutive codewords, the incoming pulse position modulated signal is decoded to give 20 channels, 3 analogue controls plus 6 other control functions. It requires a supply of about 17 Volts and 12mA. Fig.9 outlines the block diagram of the Receiver.

Circuit Operation

The ML920 operates on a timescale fixed by the on-chip oscillator and an external R and C time constant that defines its frequency. A counter is reset whenever an input pulse is received (see Fig.6). The counter defines timing windows for the following pulse. After a pulse is received the input is disabled until a count of 10. This is to prohibit any possibilities of pulse echoes of multipath reflections upsetting the correct transmission. If a pulse is received after a count of 10 has been attained, it will be accepted as a '1', a 'O' or an 'S' ('S' is the synchronisation interval or interword space). If a space is received, then a check is made to ensure that 6 pulses have previously been received. If no pulse has been received when the counter reaches 60, then a general reset takes place, and the start of a new codeword is awaited. Only when two successive codewords have been correctly received and a comparison check to prove that the two codewords are identical, is the infromation passed to the decoder to be acted upon.

The ML920 has 3 Digital-Analogue converters on its chip. Its outputs are in the form of current sinks which have 32 current levels from O to about 1mA. In Television, this eliminates some interface circuitry and allows this device to control circuits such as the TBA120S and the TBA560. Hence, direct controls of the Volume, Brightness and Color of the set is possible. An Up/Down counter is incorporated into the 5 bit data highway and this allows channel, volume, brightness or color words to be read, incremented and re-written into their respective stores. If 'color' is zero then 'color kill' is automatically generated. The circuit also has sound mute which turns the sound down to zero instantly, thus avoiding the ramping down of the sound through a 32 step volume control, as it has a slow rate of change to allow fine control. When the mute button is pressed a second time, the television reverts to its original volume. The ON/STANDBY output switches the TV on from the standby condition or vice-versa.

ML920 Pin Functions

Negative Logic: '0' is OV (V_{ss}) '1' is – 17V (V_{DD})

Pin	Name	Function
3	VDD	—17V power supply
4	VSS	OV power supply
5	ON/STANDBY I/P	A '1' on this pin will toggle pin 11 (ON O/P), generate RECALL and AFC VOLUME, BRIGHTNESS and COLOR, reset MUTE and set channel code 00000.
6	NORMALISE I/P	A '1' will normalise the VOLUME, BRIGHTNESS and COLOR outputs A RECALL signal is generated and MUTE is reset.
7	PROGRAM STEP	The program code will step up by 1 as long as this pin is held at logic '1'. The time period between steps is defined by an RC constant attached to pin 15. On reaching 20 the next step returns to 1. On output is set to ON, and AFC is generated. If the TV goes from Standby to ON, RECALL is generated and VOLUME, BRIGHTNESS and COLOR are normalised. If VOLUME is 0, MUTE is reset.
8	OSC. TIME CONSTANT	An RC time constant is formed for the clock timing be connecting external components one resistor and one capacitor, to this pin. Adjusted so that period of outputs on pin 9 is 1/20 of '0' interval of incoming ppm. by
9	OSCILLATOR MONITOR	This output is a division of two of the oscillator, and is available for testing and setting purpose

10	PPM I/P	The output of the front end amplifier is connected here such that the signal is in the form of positive pulses seperated by time periods whose length define the data. With no signal PPM input is at a logic 1.
11	ON O/P	Open drain output. Logic 1 denotes TV set ON: Logic '0' TV set standby. Set to 1 when program number changes Set to 0 power clear or by Transmitter selected 'Standby'. Toggle to opposite state by manual ON/STANDBY control
12	RECALL O/P	Open drain output A '1' may be used to trigger an on-screen display. A static output is generated by the manual controls ON/STANDBY and NORMAL. A pulse is generated by any channel change if the circuit switches to 'ON' at the time, and by RECALL and NORMALISE commands from the transmitter.
13	AFC O/P	Open drain output. Logic 1 can inhibit the tuner AFC A static output is generated by manual ON/STANDBY control. A pulse is generated by any program number change.
14	POWER CLEAR	A capacitor and resistor connected here define the time delay for the power clear circuit which normalises all D—A outputs etc.
15	PROGRAM STEP TIME CONSTANT	An R—C time constant defines the time period between increments of the channel when stepping.
16—20	PROGRAM	5 Outputs encode 20 program numbers in binary code E D C B A Program 1 is 0 0 0 0 0 Program 20 is 1 0 0 1 1 E is first and A is last in the PPM pulse train. Program 1 is set when ON goes to a '1'.
21,23,1	VOLUME BRIGHTNESS COLOR	These three outputs are from three 5 bit current mirror D/A converters. They are referenced to the current drawn from pin 24, Iref, and give 32 steps, Iref/8 per step, from 0 to 31/8 Iref. The outputs will be set to 12/8 Iref by the NORMALISE I/P the mormalise code from the transmitter or when the ON output goes to a '1'.
22	MUTE O/P	This will change state (toggle) on reception of a mute command but if VOLUME O/P is zero MUTE O/P is held at '0'.
24	D/A REFERENCE	A current drain Iref, set by a single external resistor will fix the nominal step of the D/A outputs to Iref/8.
2	COLOR KILL	This O/P gives a logic '0' when the COLOR D/A output is zero.

Applications

Ultrasonic Transmitter

As previously mentioned the SL490 PPM transmitter and ML920 PPM receiver can be used whenever a binary digital channel exists to control both digital and analogue functions. Fig.10 shows how an additional NPN transistor (BC547) may be used to drive a visible light LED is required. Two PNP transistors (BC557) may also be added as shown as active 'pull ups' to increase the power fed to the ultrasonic transducer at the expense of a slight increase in battery current consumption. Without these, the output current is limited to about 5mA by internal pull up resistors, but even with the transducer directly powered from pins 2 and 3, adequate load power is obtained by the 18V effective output swing.

The modulation rate of the PPM signal is set by the CR network on pin 16. With the 220nF capacitor shown, a variable resistor set at 50Kohms should give a PPM speed such that the word rate is 150mS, but almost any

desired rate can be selected if required. The CR network on pin 18 similarly sets the desired carrier frequency. In this particular application the 1.5nF capacitor and the 22Kohms resistor are used to set the carrier frequency to the natural resonance of the transducer, about 38KHZ. By choosing a suitable capacitor and trimming resistor, a wide range of carrier frequencies (0 to 200KHZ) are possible.

Ultrasonic Receiver

Before the received Ultrasonic signal can be detected and fed to the ML920 PPM demodulator, it must be amplified. Some frequency selectivity is also desirable and this can be achieved by an operational amplifier, active filter stage. Fig.11 shows how an SL748 can be used as the first amplifier stage. Some lower output transducers may require an additional single transistor amplifier stage before this. The amplified signal is detected by the NPN transistor (BC547) and after smoothing, is fed to the interface amplifier. The input of this amplifier is biased so that a threshold is set up just above the noise level. The output is thus reasonably noise free and sufficient amplitude to drive the ML920 directly into pin 10. This receiver together with the transmitter has been used to give a working range of 6m without active pull ups and 8m with active pull ups although this does depend on transducer efficiency. The word rate used is about 6 per second giving a command rate of 1 receiver command every 300mS. The circuit and component layout is shown in Fig.14 and Fig.15.

Infra-red Transmitter

For infra-red transmitter unit, the SL490 is easily made to give out a carrier frequency, or converted so that the output will consist of narrow DC pulses. If no carrier frequency is needed for the PPM output then no capacitor is needed on pin 18 and resistor value should be reduced to 2.2Kohms. A narrow current pulse is derived from pin 3 shown in Fig.12 and this is used to drive the LED array by a PNP-NPN configuration, (in this instance the NPN transistor is a Darlington pair). The arrangement gives up to 10Amps. current pulses and can be used as extreme ranges with a sensitive receiver.

Battery consumption is only increased by 50% because of the low duty cycle load current pulse: pulse width may be reduced to less than 15uS, but phototransistor response may be decreased for narrower infra-red pulses. Usually sufficient power output will be available when a simple NPN output configuration with 1 to 3 LED's connected in series. Parallel connection is only needed at higher currents when adequate current sharing takes place between LED's of the same type. The current pulse is drawn from 470uF capacitor which should not have excessive inductance or long connections to the load. In addition if a visible light is needed to indicate that the transmitter is operating, a red LED may be connected directly to pin 2, the other output pin. (unused in this application). This is also shown in Fig.12.

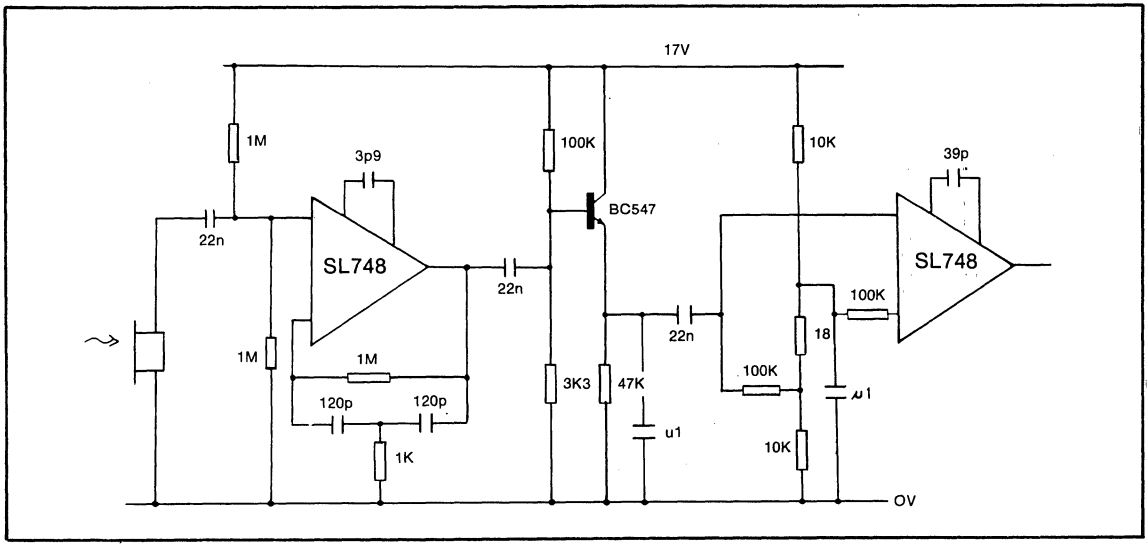


Fig. 11. Ultrasonic Receive Amplifier

Infr-Red Receiver

The photodetector should have a filter with adequate cutoff towards the visible light region. A Kodak type 87C is suitable and allows a high gain, operational amplifier, active filter stage to give very good sensitivity (Fig.13 shows such a configuration). The circuit should be well screened from electrical noise. Indeed the screen can be extended over the photodetector lens as an open mesh. The BPW34 photodiode gives a good response to weak signals down to a 10uS pulse width. The SL748 in Fig.13 filters the detected infra-red signal and amplifies the pulse, feeding it to a CMOS 2 input and gate. The first gate is biased in class A and the other 2 form a monostable. Some sensitivity control and monostable threshold variation are achieved by a simple 1M ohm potentiometer. This gives a very clean pulse at the output which is transistor buffered and fed to the ML920 PPM receiver. The ultimate range of the transmitter receiver was found to be 27 m. More usual ranges may be dealt with by using only a single output NPN transistor and transmitter LED, where the range was found to be about 8 m. The word time used was 75ms, twice the speed of the ultrasonic link. The layout and component positions can be seen in Fig.16 and Fig.17.

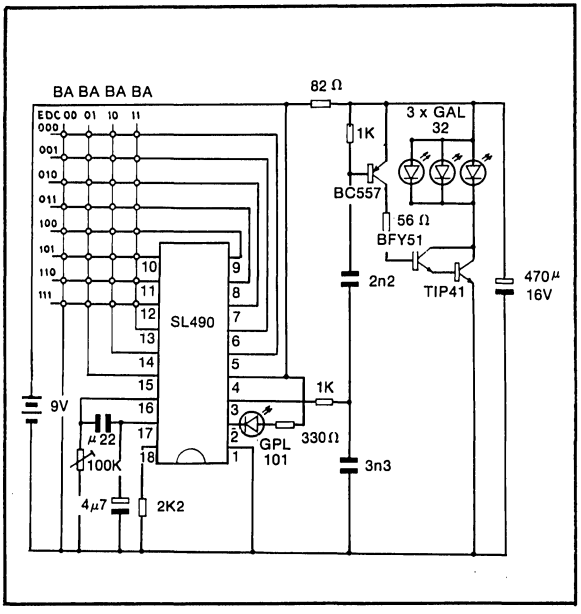


Fig. 12. Infra-Red Transmitter

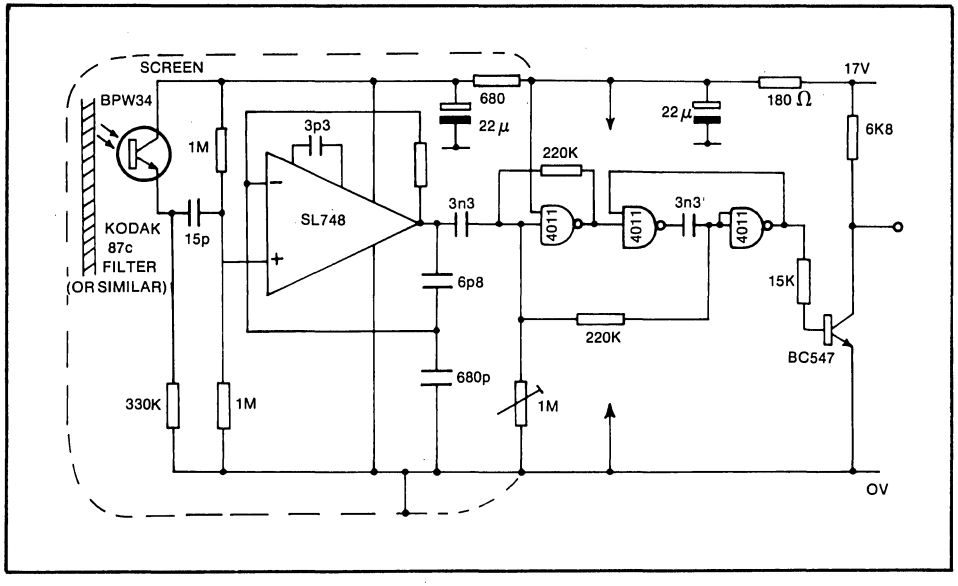


Fig. 13. Infra—Red Receiver for PPM

Very little is needed externally to this device, there being a high degree of integration on the chip. Pull up load resistors of about 50K ohms are required, however, on all digital outputs except the oscillator monitor. Fig.18 shows this and the other basic requirements. The whole receiver timing is set by a single RC time constant on pin 8. Final adjustment is achieved by monitoring pin 9 which gives a buffered, divide by 2 of the main oscillator. The correct setting will be when 20 complete cycles on pin 9 occur for a '0' interval in the received PPM signal. Two other time constants may be needed: a power start up RC on pin 14 which clears and intialises the chip when its supply is switched on and a second time constant on pin 15 may be needed if the program step is used. This defines the stepping rate.

The analogue outputs will need a current mirror reference on pin 24 (about 0.35mA) and 5 bit D/A converter outputs themselves will each need a current sink for the 0 to 1.4mA or so to which they may be set.

For maximum linearity these current sinks should not allow their voltage to exceed 5V or so (3.9K ohms maximum), but this may be increased to 10V if 10% linearity can be tolerated. The 3 manually controlled local inputs are shown in Fig.18 as simple switched resistor pull ups. Some debounce may be needed in extreme cases.

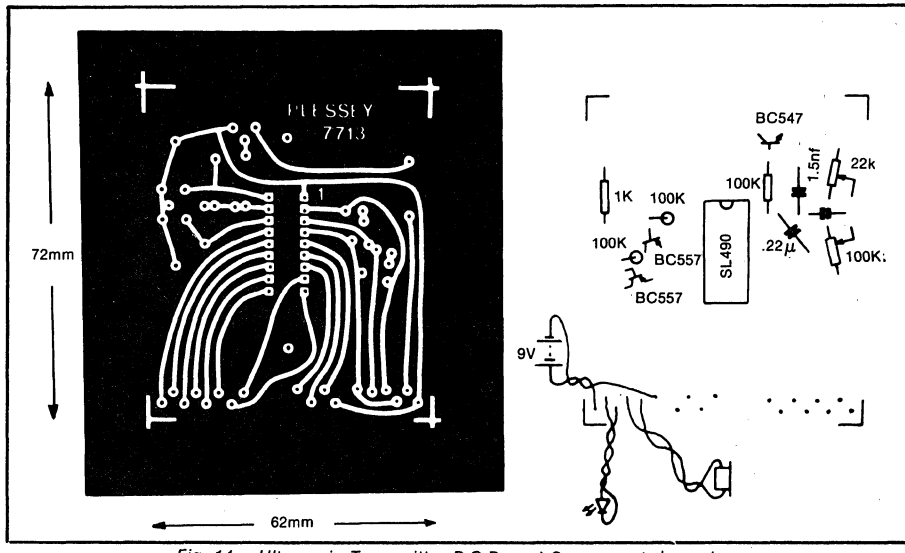


Fig. 14. Ultrasonic Transmitter P.C.B. and Component Layout

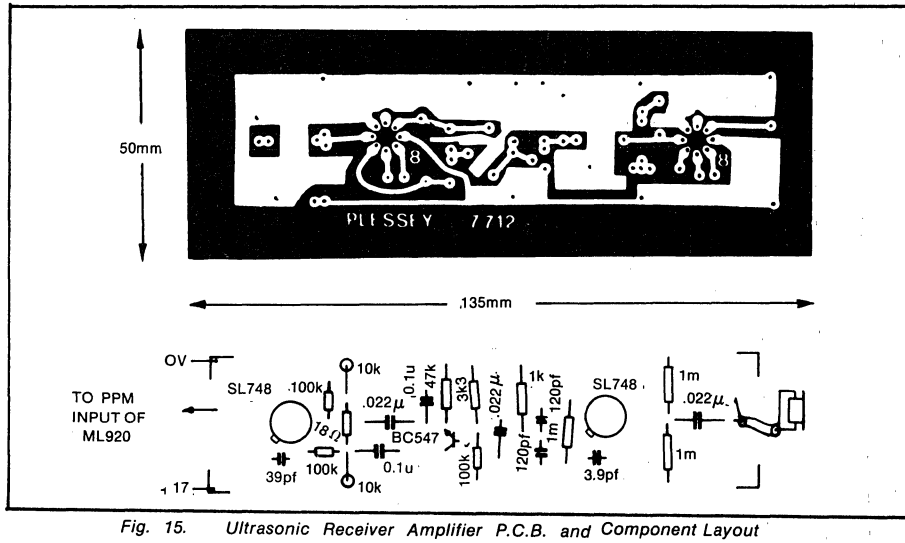


Fig. 15. Ultrasonic Receiver Amplifier P.C.B. and Component Layout

Up to 20 channels may be set, selected individually and stepped sequentially. If less than 20 channels are needed then 6,8,10,12 and 16 are readily catered for. 10 channels may be utilised with no modifications, instead of the latched output E,D,C,B,A, being decoded, the least significant bit, A, is ignored. When stepping, a double channel step is needed to get to the next used channel. If stepping is not required any number of channels may, of course, be used. Fig.19 allows fast 'end' around stepping of unused channels in a 16 or 8 channel system. When an unused program number is detected the step input is held low and the step time constant is switched to 'very fast'. A similar circuit may be used to cater for complete stepping facilities with 12 or 6 channels.

As previously mentioned the analogue outputs are current sources giving 32 steps of current in the range 0 to 1.4mA. This may be controlled by the current mirror reference on pin 24. Greatest linearity is obtained if the current sink resistor on the D/A outputs do not exceed 3.9K ohms giving a 0 to 5V control range. However, a 0 to 10V range may be obtained with higher resistor values if some reduction in linearity can be tolerated. The simplest form of local asjustment of analogue control levels is to make the current sink resistor variable, but if more sophistication is required then Fig.20 shows how an operational amplifier may be used. This circuit enables both the range and the DC value of the control voltage at the output of the operational amplifier to be set and operated by either the remote control or the local control.

If local push-switch control of the analogue functions is desired, then Fig.21 shows how an additional SL490 with few external components may be used. The output of this SL490 is 'teed' into the receiver PPM line at the base of the buffer transistor. On/Standby, Normalise, Step, Mute and Recall are all now available as local controls from push-switches which require no debounce via the local control transmitter.

One transmitter can be used to control more than one receiver. Fig.22 shows how a simple slider switch can change the modulation rate of the PPM to control another 32 command set receiver. As long as the command rates differ by more than 30%, no cross coupling should be experienced because of the high integrity of the receiver PPM demodulator timing. Fig.22 also suggests how an MOS transistor 'memory' and 2 push switches may replace the 2 position switch.

In some cases a fourth analogue control output may be required from the receiver and it can be seen in Fig.23 how this might be achieved with the addition of some logic elements and a D/A ladder network. 16 channel selections are available, freeing 4 commands for other uses. Because of commands becoming 'mixed' it is recommended that the step facility is not used in configurations where additional commands have been incorporated. This simplifies decoding circuitry greatly.

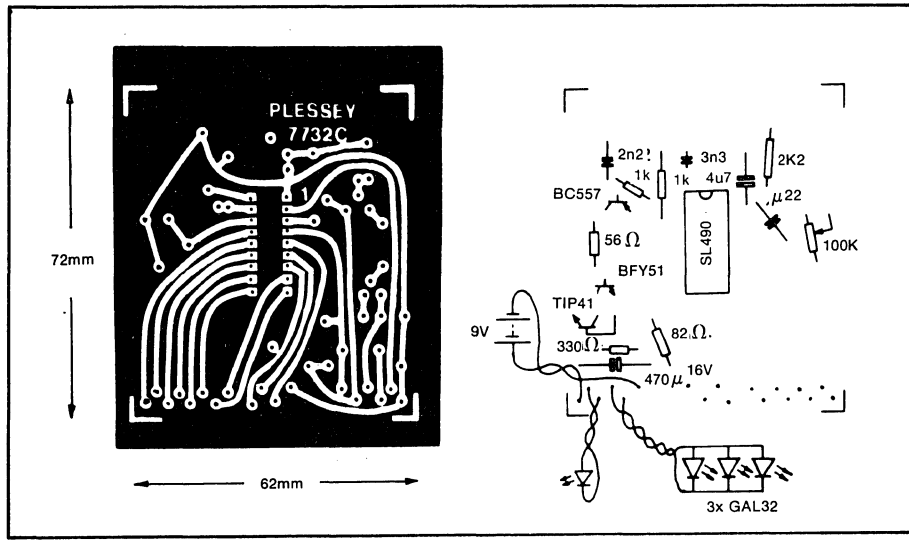


Fig. 16. Infra-red Transmitter P.C.B and Component Layout

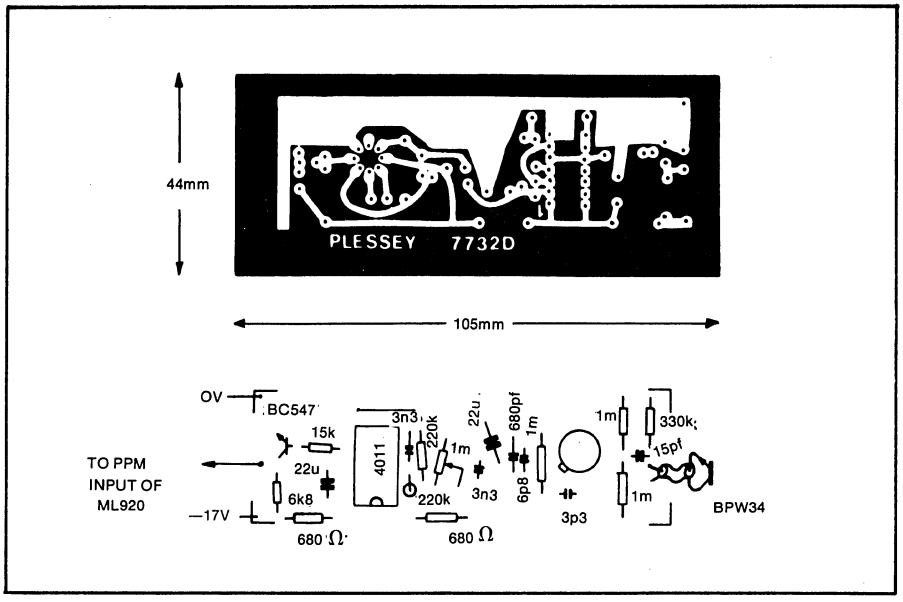


Fig. 17. Infra-red Receiver Amplifier P.C.B. and Component Layout

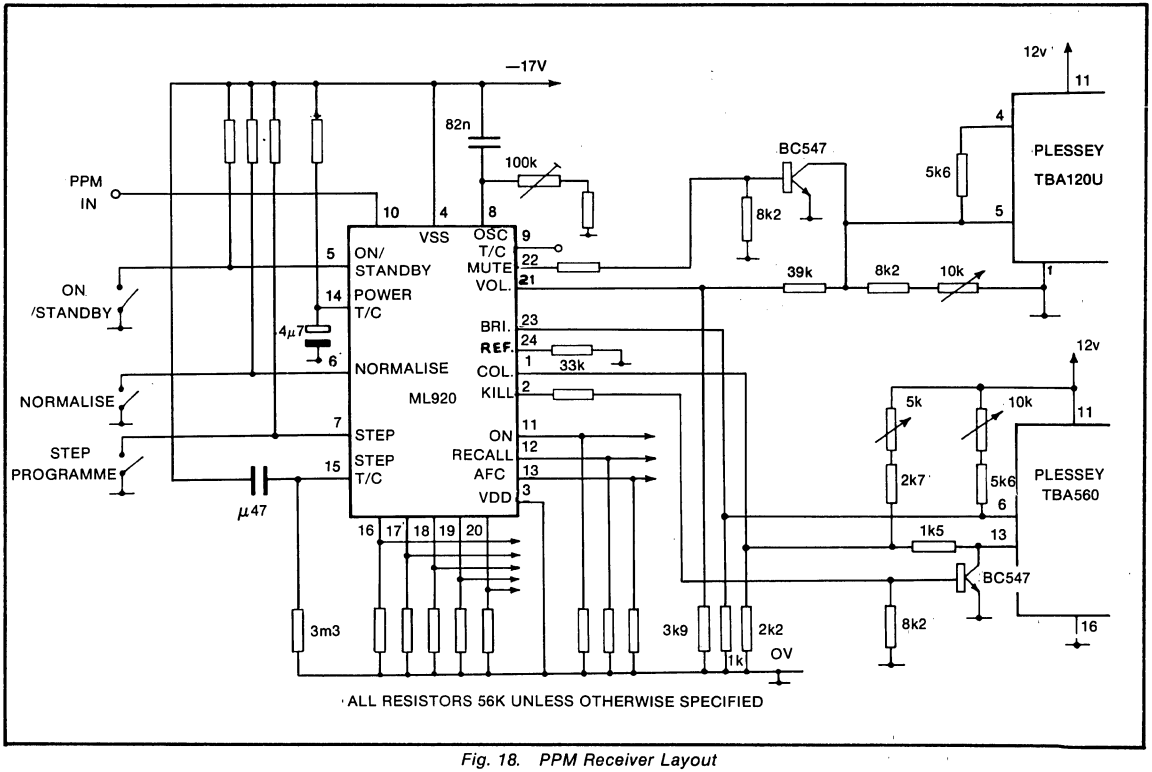


Fig. 18. PPM Receiver Layout

TRANSMITTER CODE	FUNCTION
E D C B A	
0 0 0 0 0	Program 1
0 0 0 0 1	Program 2
0 0 0 1 0	Program 3
0 0 0 1 1	Program 4
0 0 1 0 0	Program 5
0 0 1 0 1	Program 6
0 0 1 1 0	Program 7
0 0 1 1 1	Program 8
0 1 0 0 0	Program 9
0 1 0 0 1	Program 10
0 1 0 1 0	Program 11
0 1 0 1 1	Program 12
0 1 1 0 0	Program 13
0 1 1 0 1	Program 14
0 1 1 1 0	Program 15
0 1 1 1 1	Program 16
1 0 0 0 0	Program 17
1 0 0 0 1	Program 18
1 0 0 1 0	Program 19
1 0 0 1 1	Program 20
1 0 1 0 0	Color +
1 0 1 0 1	Programme Step +
1 0 1 1 0	Volume +
1 0 1 1 1	Brightness +
1 1 0 0 0	Standby
1 1 0 0 1	Mute
1 1 0 1 0	Recall
1 1 0 1 1	Normalise
1 1 1 0 0	Color —
1 1 1 0 1	Programme Step —
1 1 1 1 0	Volume —
1 1 1 1 1	Brightness —

TABLE 1. BASIC 32 COMMAND SET

TRANSMITTER CODE	FUNCTION
E D C B A	
0 0 0 0 0	Program 0
0 0 0 0 1	Program 1
0 0 0 1 0	Program 2
0 0 0 1 1	Program 3
0 0 1 0 0	Program 4
0 0 1 0 1	Program 5
0 0 1 1 0	Program 6
0 0 1 1 1	Program 7
0 1 0 0 0	Program 8
0 1 0 0 1	Program 9
1 0 1 0 0	Color +
1 0 1 1 0	Volume +
1 0 1 1 1	Brightness +
1 1 0 0 0	Standby
1 1 0 0 1	Mute
1 1 0 1 0	Recall
1 1 0 1 1	Normalise
1 1 1 0 0	Color —
1 1 1 1 0	Volume —
1 1 1 1 1	Brightness —
0 1 0 1 0	Page Select
0 1 0 1 1	Program Select
0 1 1 0 0	Page Time Select
0 1 1 0 0	Page Display
0 1 1 0 1	Picture Display
1 0 0 0 0	Reset Newsflash
1 0 0 0 1	Inhibit Newsflash
1 0 0 1 0	Reveal Text
1 0 0 1 1	Freeze Page

TABLE 2. MODIFIED TELETEXT COMMAND SET

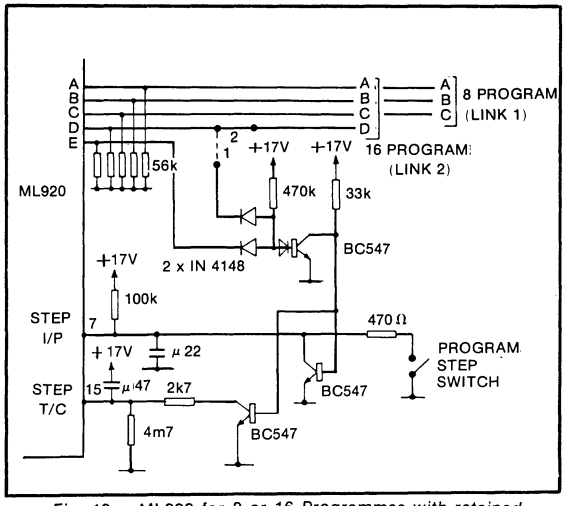


Fig. 19. ML920 for 8 or 16 Programmes with retained stepping function

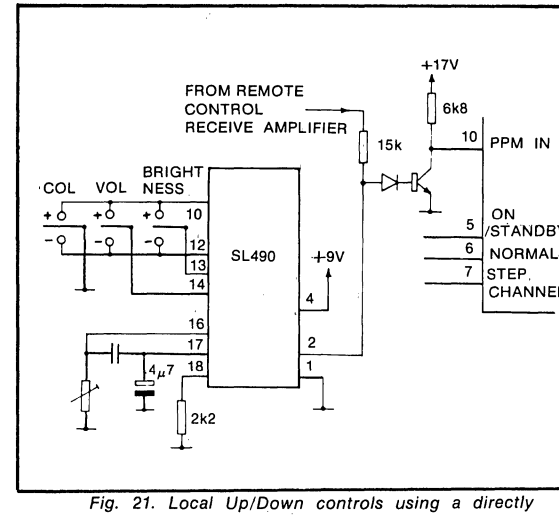


Fig. 21. Local Up/Down controls using a directly connected SL490

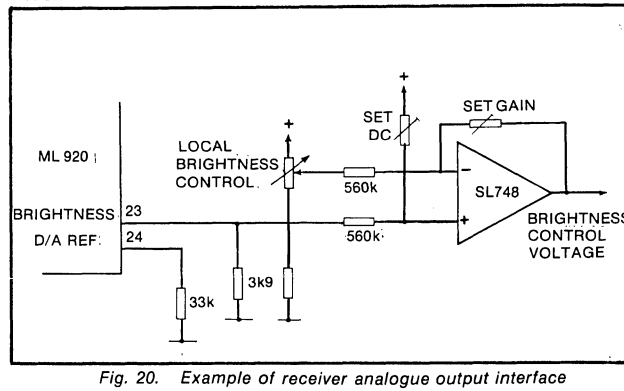
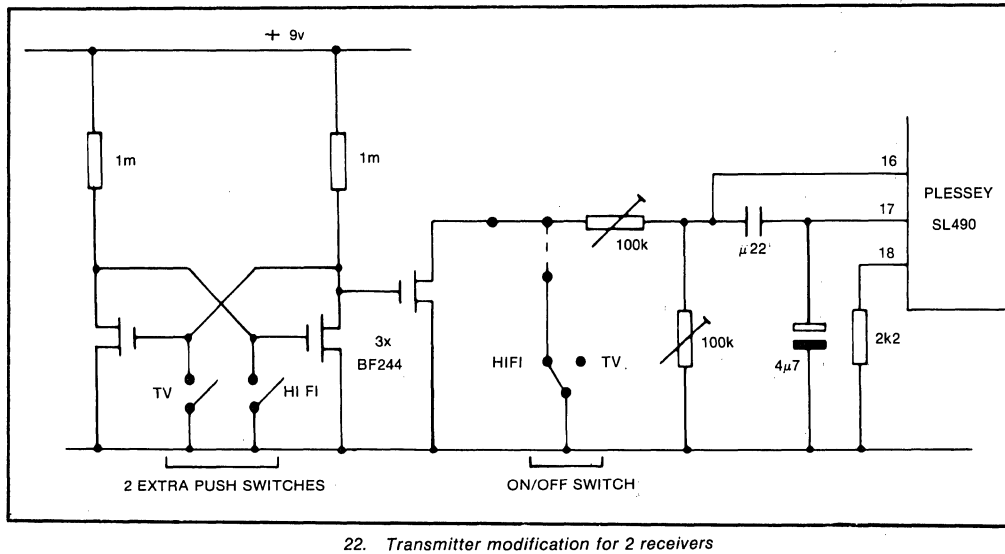


Fig. 20. Example of receiver analogue output interface with local control



22. Transmitter modification for 2 receivers

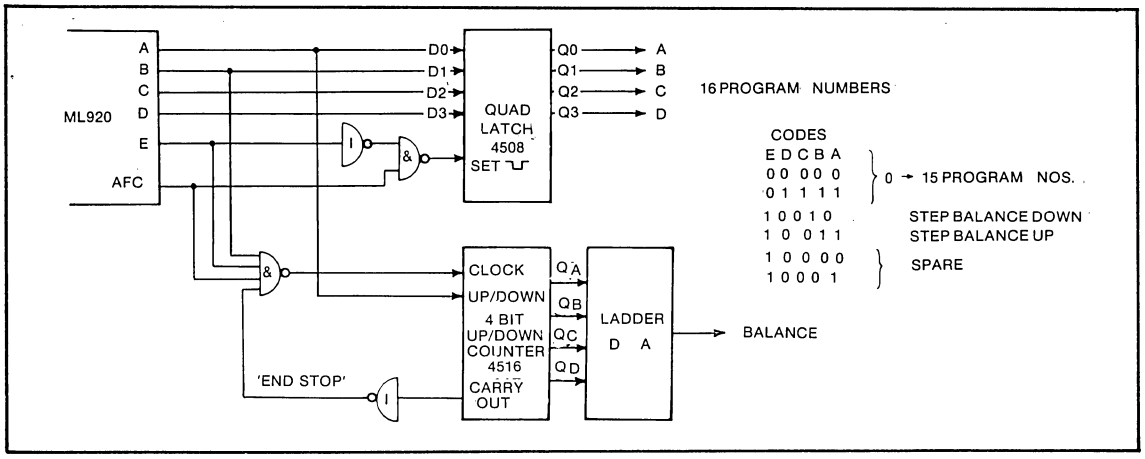


Fig. 23. Application with fourth analogue control plus 16 programmes

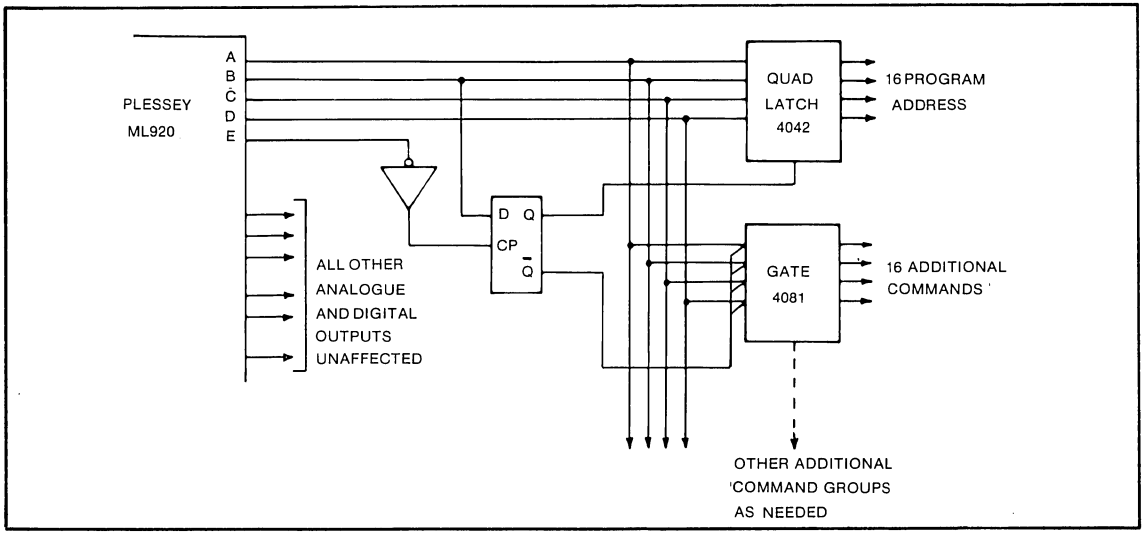


Fig. 24. Receiver modification for additional commands

The basic command set of 32 can be extended ad infinitum. All that is needed are shift up and shift down keys to produce as many extra commands as desired. Fig. 24 gives an example of how 16 channels may be stored and after receipt of the code E, D, C, B, A as 1001 *(shift up) the channel selection is stored and a quad gate is enabled which gives 16 more available commands. In this application, other controls remain operative and it is only the 16 channel selection, that cannot be altered until after 1000 *(shift down) is received. A shift stepping method may thus be utilised to produce as many different sets of 16 command groups as are required. The only limiting factor is in indicating to the user which is the current command set.

An example of a particular application of an external command set is in teletext. Fig. 25 shows how a television set incorporating teletext may have its remote control keyboard laid out. The interface logic required to realise all these functions is shown in Fig. 26 and is easily realised with CMOS logic. The quad latch is used to store the programme number 0 to 9, as a BCD digit while teletext selections are being made. The negative true logic outputs, A, B, C, D, E of the channel selection highway from the ML920 may be inverted at the output of the quad latch by connection to the Q side of the output.

The monostable is triggered by the negative AFC pulse and produces a delayed and well defined stroke pulse to indicate the availability of 'good' data on the highway. The package requirement is as follows:—

Function	Number	Package Type	Quantity
3 input gates	5	4025	2
2 input gates	6	4001	1
		4011	1
inverters	3	spare gates in above packages may be used	
quad latch	1	4042	1
monostable	1	4528	1

Table 2 shows the full list of commands and how they are allocated. When reading the table in conjunction with Fig. 26 it should be remembered that negative logic convention is used at the output, A, B, C, D, E of the ML920.

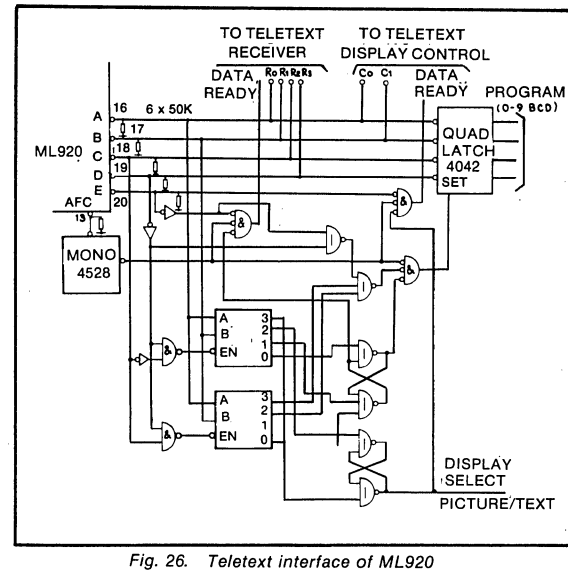


Fig. 26. Teletext interface of ML920

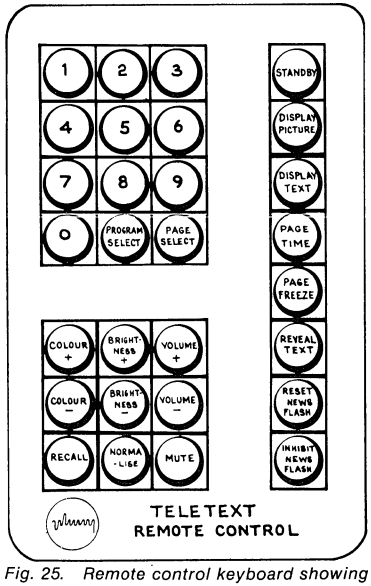


Fig. 25. Remote control keyboard showing how available teletext commands may be incorporated

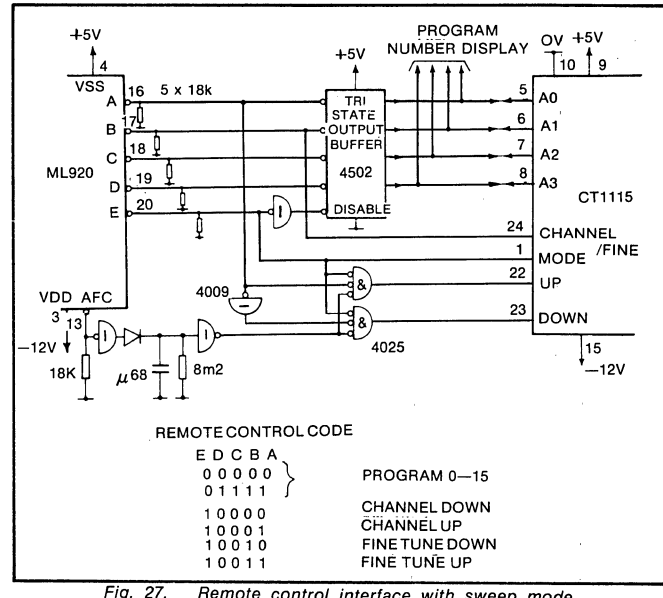
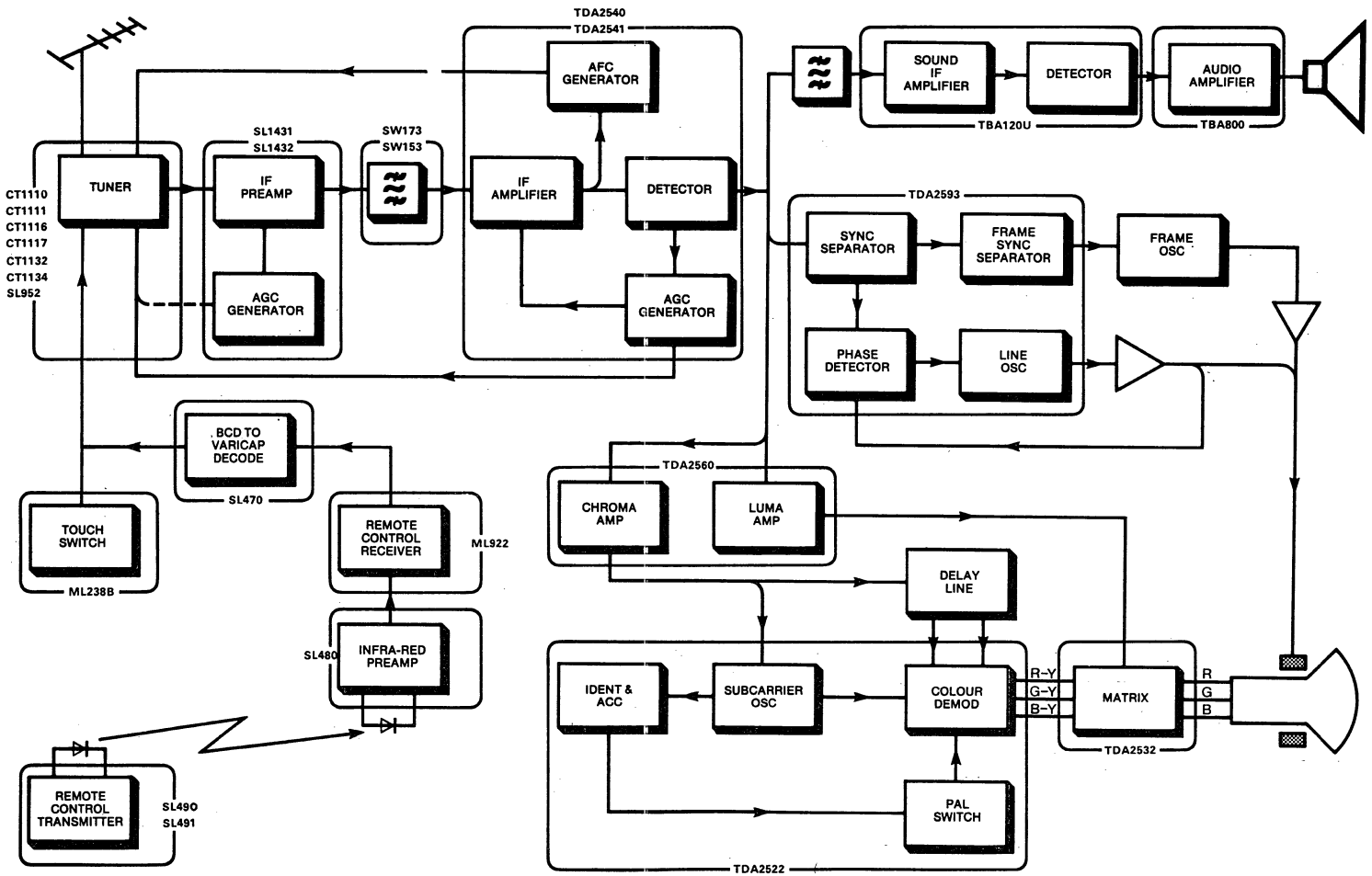


Fig. 27. Remote control interface with sweep mode frequency synthesis tuning

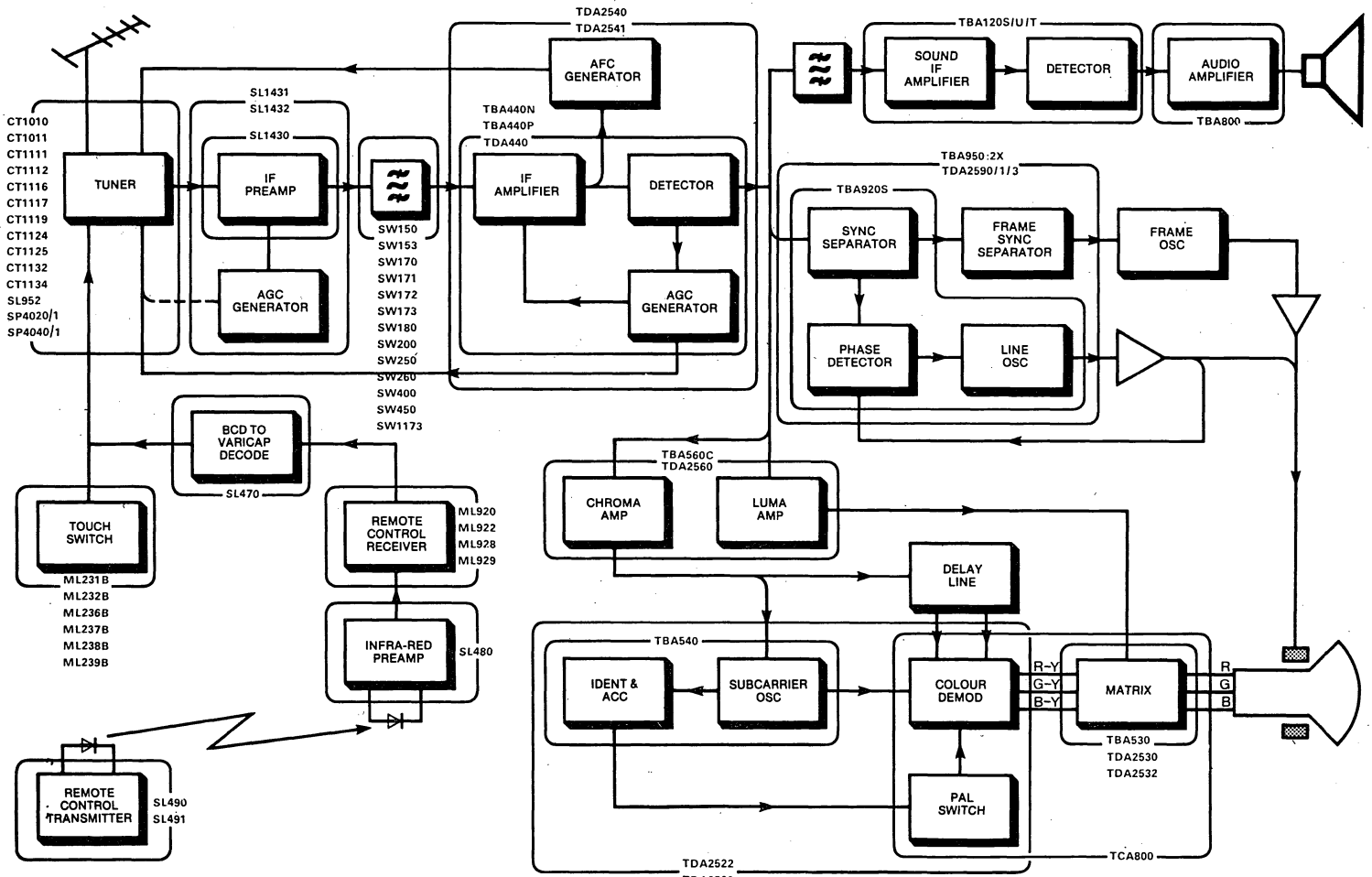
Remote Control of DCT

The remote control can easily be used for programming the Direct Channel Tuning, frequency synthesis system or in fact any synthesised tuner with a binary selection input. In Fig.27 it can be seen how easily a sweep mode Plessey DCT can be conditioned to coarse tune by incrementing or decrementing the channel number (equivalent to 8MHz steps in the UHF Band). In this way the tuning information for up to 16 channels can be programmed by sweeping to the desired channel. When the programme number is changed, the channel selected is allocated automatically to the old programme number. The new programme number will then call up and tune its own channel or be available for a new channel allocation if the sweep is continued. Fine tuning information may also be remotely controlled in steps of 125kHz and the last fine tuning information set will be stored for future reference.

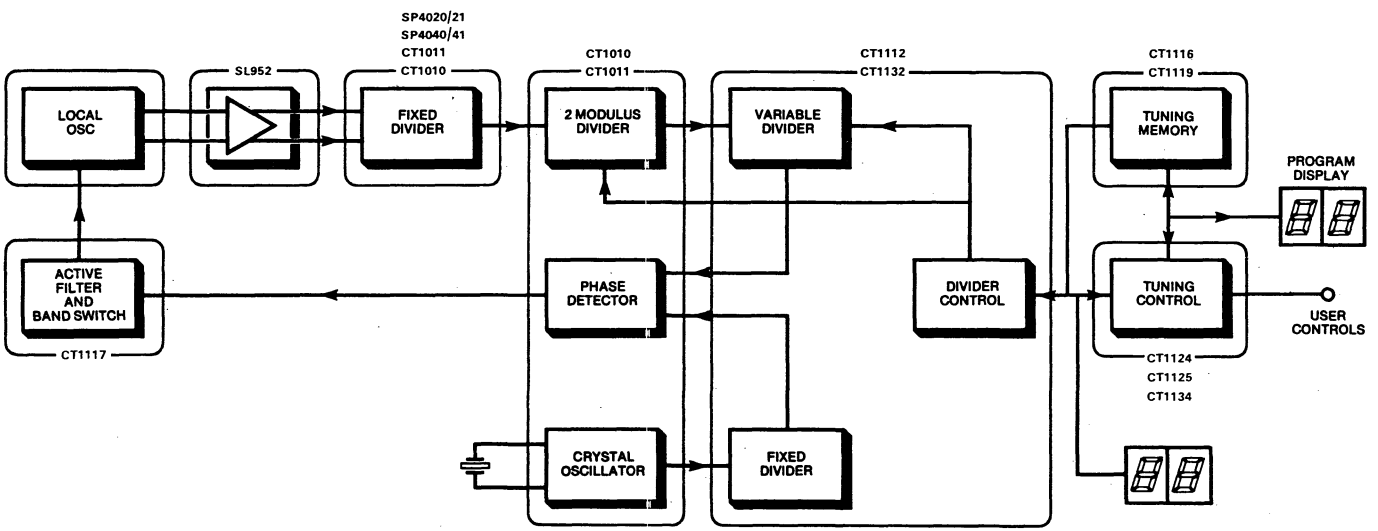
INTEGRATED CIRCUITS FOR TV (PREFERED SOLUTION)



INTEGRATED CIRCUITS FOR TV



INTEGRATED CIRCUITS FOR TV FREQUENCY SYNTHESIS



7. TECHNICAL DATA

PLESSEY
Semiconductors

CT2010

1 GHz ÷ 380/400 PRESCALER

The CT2010 is a 380/400 two modulus divider which will operate at frequencies between 80 MHz and 1 GHz. The device is the prescaler used in the Plessey Key Frequency Synthesis Tuning System.

The input is terminated by a nominal 50 ohms and should be AC coupled to the signal source. The reference pin should be AC decoupled. The decoupling should be effective over the full operating frequency range.

The divider contains a fixed divide by 20 followed by a divide by 19/20. The divide by 19/20 divides by 20 when no control pulses are applied to the control input. The divide by 19/20 will divide by 19 once for every positive going edge applied to the control pin. The control input edge is latched and synchronised so that the following output cycle, commencing with a negative edge, is produced by 380 input cycles to the whole divider stage, rather than 400. This means that the device is highly tolerant of delay in the control loop and distortion of the control waveform.

To ensure that there is an output cycle produced by 380 input cycles for every control pulse, the rate of control pulses should not exceed half the output frequency. (See timing diagrams.)

The output source impedance is nominally 100 ohms. The output swing is nominally 300 mV and swings down from the positive supply.

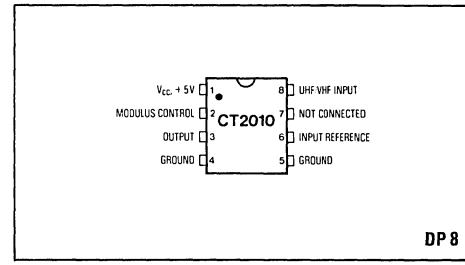


Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
UHF input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating ambient temperature	-10°C to +65°C

FEATURES

- On-chip Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Low Output Radiation
- Single ECL Output
- 5V Logic Level Control Input
- Control Independent of Distortion and Delay

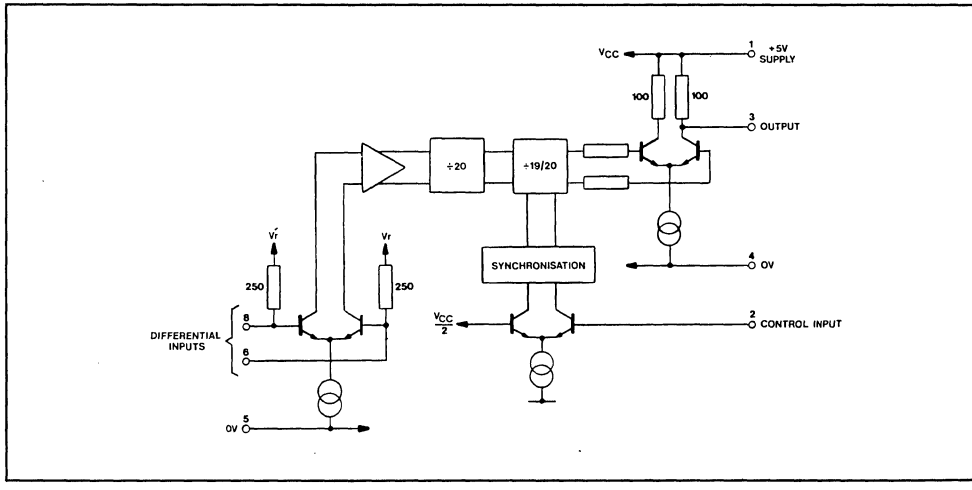


Fig.2 CT2010 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Test circuit: Fig.3
$V_{cc} = 5V$, $T_{amb} = 25°C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	1	4.5		5.5	V	
Supply current	1		90	110	mA	
Input voltage, 80MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
V_{IN} 300MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
500MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
700MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
1000MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
Output voltage swing	3	240	300		mV	p-p, no load
Output impedance	3		100		Ω	
Control input, high	2	$2/3V_{cc}$				
	2			50	μA	
low	2			$1/3V_{cc}$		
	2	-10			μA	
pulse width	2	0.2	3		μs	

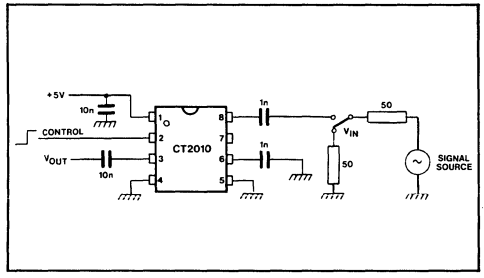


Fig.3 Test configuration

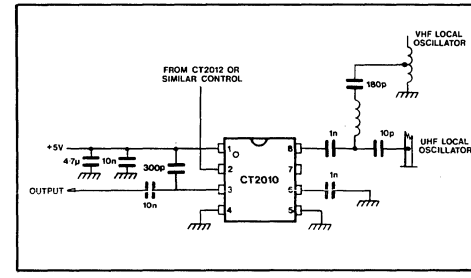


Fig.4 Typical application with combined input

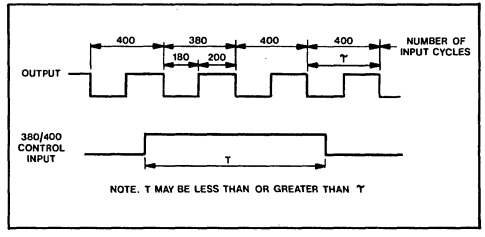


Fig.5 Timing diagram

PLESSEY
Semiconductors

CT2012

PLL SYNTHESISER FOR TV

The CT2012 forms the heart of the Plessey Key Frequency Synthesis Tuning System by taking data from the system control and data highway (the Keybus) when TUNE or FINE TUNE code is recognised and then using this data to control the frequency of the local oscillator in a television tuner with a phase locked loop (PLL).

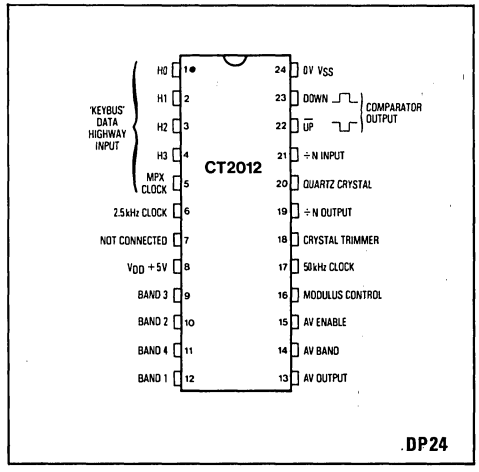


Fig.1 Pin connections

FEATURES

- High Sensitivity Divider Input
- Improved Control of Two-Modulus Divider
- Fully Keybus Controlled
- On-chip Frequency Standard and Comparator
- Four Band Selection Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	+7V
Pin Voltage, pins 9—13	+14V
Voltage, all other pins	+7V
Operating temperature range	-10°C to +65°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = +5V
Test circuit: Fig.3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	8	4.5		5.5	V	
Supply current	8		22	45	mA	Outputs unloaded
Keybus inputs, high	1—5	V_{DD}-1			V	Leakage 10μA max.(Pin 5 only)
low	1—5			0.8	V	
Internal pullup resistor	1—4	2	4	6	kΩ	
÷N input, peak-peak swing	21	200			mV	Sine wave via external capacitor
Internal capacitance	21			10	pF	
External frequency standard input, pin 20 not connected high	18	V_{DD}-1			V	100μA max. sinking
low	18			0.8	V	100μA max. sourcing
Quartz crystal standard	18, 20		4		MHz	20pF parallel resonance
AV Band and enable inputs	14, 15	V_{DD}-1			V	Leakage 10μA max.
	14, 15			0.8	V	
Band and AV outputs, unselected	9—13			13.2	V	Free drain, leakage 10μA max.
selected	9—13			5	V	1mA sinking
÷N output, high	19			7	V	Free drain, leakage 10μA max.
low	19			0.4	V	0.3mA sinking

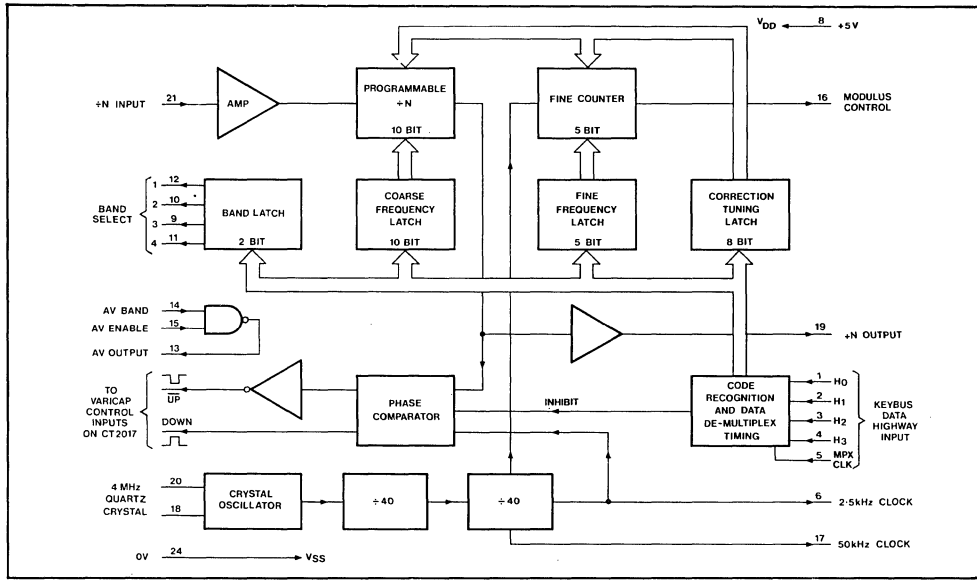


Fig.2 CT2012 block diagram

Apart from the CT2012 and the tuner, the PLL needs two other integrated circuits: a ÷380/400 PRESCALER (the CT2010) and the synthesiser tuning interface (the CT2017), which includes a charge pump, an active filter and an output stage to drive the varicap line which controls the local oscillator in the tuner.

In a typical system re-tuning of the television receiver will come from a control circuit (such as the CT2014) following some input from the viewer. This input will be new channel, fine tuning information or an instruction to access a word of non-volatile memory. In every case, the control circuit will send the required channel and fine tuning information to the CT2012.

The FINE TUNE code is used to directly transfer the FINE TUNE number from the control circuit to the synthesiser and is separate from TUNE to reduce the highway use and the time delay during manual and automatic adjustment tuning.

The CT2012 contains six main parts:

(a) A section to recognise the TUNE code (hexadecimal 1D) or FINE TUNE code (hex. 1E) on the Keybus and then to latch all of the relevant tuning information.
(b) A 10 bit programmable divider with an amplifier on its clock input to allow use of a small swing on the output of the PRESCALER and hence to reduce radiation.
(c) A fine tuning system which generates the correct pulses to control the modulus of the prescaler and so give a small shift in synthesised frequency.
(d) A crystal oscillator circuit (for 4MHz crystal) and fixed ÷1600 divider to give 2.5kHz comparison frequency and fine tuning timing.
(e) A phase and frequency comparator driven by the programmable divider and the fixed divider.
(f) Logic for band decoding and for video time-constant switching for audio visual (AV) mode logic.

The Keybus highway is used to carry both instructions and data around the Key System. To separate these two functions the codes are transmitted when the Multiplex Clock is low and the data when it is high; all zeroes or all ones are inserted to fill the gaps between adjacent code or data words to avoid spurious instructions. In order to improve the system's immunity to noise on the highway the Multiplex Clock may be stopped between operations so that noise is not clocked into any circuit, and so should have no effect, and ideally the highway and Multiplex Clock lines will be stopped in their lower impedance state to reduce noise amplitudes.

It is expected that all devices driving the highway will have Open Drain outputs, for which pull-up resistors (nominal 4kΩ) are included in the CT2012.

To safely detect control codes edge sensitive latches are clocked on the rising ('0' to '1') edges of the Multiplex Clock and have their inputs driven by gates looking for a TUNE code (0001 followed by 1101) or a FINE TUNE (0001 followed by 1110).

Time	State				Remarks
	H3	H2	H1	H0	
C1	0	0	0	1	Control code
C2	1	1	0	1	
D1					Not used by Synthesiser
D2					
D3					
D4	B1	B0	Q9	Q8	Band (B), Frequency (Q) and Fine Frequency (P) from Key.
D5	Q7	Q6	Q5	Q4	
D6	Q3	Q2	Q1	Q0	
D7	0	0	0	P4	
D8	P3	P2	P1	P0	

Table 1 Tuning sequence on Keybus

Time	State				Remarks
	H3	H2	H1	H0	
C1	0	0	0	1	Control code
C2	1	1	1	0	
D1	Q_{C2}	Q_{C1}	Q_{C0}	P_{C4}	Correction tuning
D2	P_{C3}	P_{C2}	P_{C1}	P_{C0}	

Table 2 Correction tuning sequence on Keybus

Signal	Pin	High (source current) V_{DD} −0.5V min	Low (sink current) 0.4V max
2.5kHz Clock	6	0.5mA	2.0mA
$\overline{UP}$ DOWN 50kHz Clock	22 23 17	0.1mA	0.8mA
Modulus Control	16	0.1mA	0.3mA

.Table 3 Logic output currents

Pin No.	Name	Function	
8 24	V_{DD} V_{SS}	+5V 0V } Power supply	
1 2 3 4	H0 H1 H2 H3	Four line highway, H0 is LSB. Inputs, 0V and 5V logic levels nominal. 4K ± 50% pull-up resistors (to V_{DD}) in device.	KEYBUS
5	MULTIPLEX CLOCK	Highway timing input, 0V and 5V nominal logic levels.	
6	2.5kHz CLOCK	2.5kHz output from crystal via reference divider. May be used to give Multiplex Clock.	Outputs with 0V to 5V nominal swing.
17	50kHz CLOCK	50kHz output from crystal via reference divider. Use when setting crystal trimmer.	
22 23	$\overline{UP}$ DOWN	Increase frequency when low Decrease frequency when high } Comparator outputs to charge pump in Tuning Interface IC	
16	MODULUS CONTROL	Controls PRESCALER division ratio by pulsing high up to 38 times each comparison cycle.	
20	QUARTZ CRYSTAL	One crystal pin and the fixed capacitor.	
18	QUARTZCRYSTALTRIMMER	Second crystal pin and trimmer capacitor.	
21	÷N INPUT	Low level input clock to Programmable Divider. Should be AC coupled.	
12 9 11 10 13	BAND 1 BAND 3 BAND 4 BAND 2 AV OUTPUT	Band output selected by code 00 Band output selected by code 01 Band output selected by code 10 Band output selected by code 11 Time constant switch, pulls low only if AV band selected and AV enable is high	Open drain outputs for external pull-up to +12V.
14	AV BAND	Input from band switch to allow AV mode to be selected.	
15	AV ENABLE	Selects shorter time constants for locking television receiver to video tape recorder or equivalent. Will be driven by diode decoder from Programme Number lines. High for AV mode, only operative when AV band is selected.	
19	÷N OUTPUT	Output of programmable divider provided for test purposes only.	

TUNING RANGE

Combining the Fine Offset range, 0 to 19 steps of 50kHz with the Programmable Divider range, 80 to 1023 steps of 1MHz, allows tuning of the local oscillator for all television broadcast channels in bands I, III, IV, V, to within 25kHz. In practice almost all television channels are integer multiples of 50kHz and so may be received EXACTLY (apart from any slight crystal or IF error).

The correction tuning system gives a range of -3.95 to +4.00MHz in 50kHz steps around the nominal frequency.

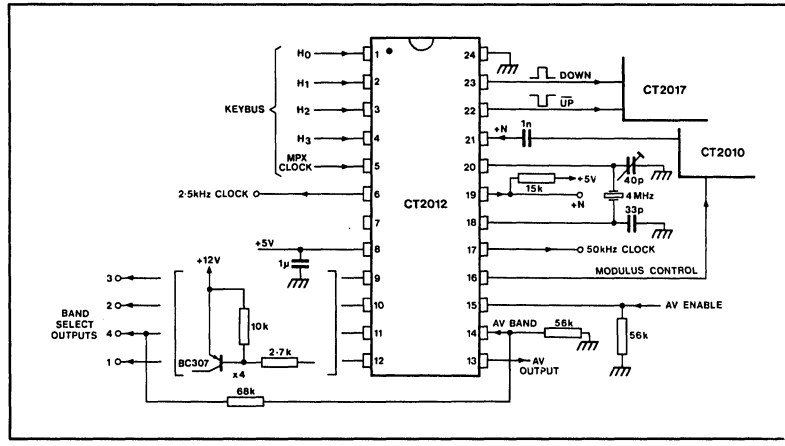


Fig.3 CT2012 test and application circuit

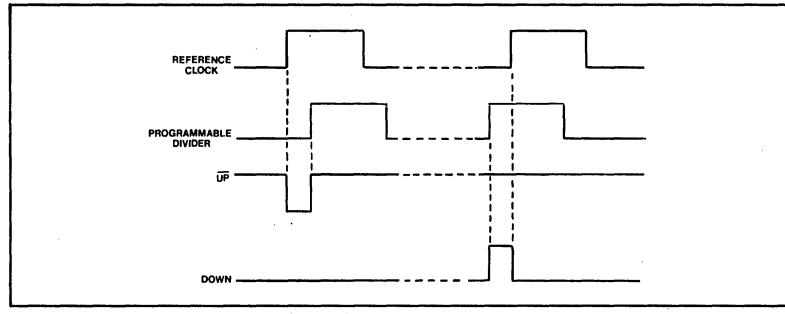
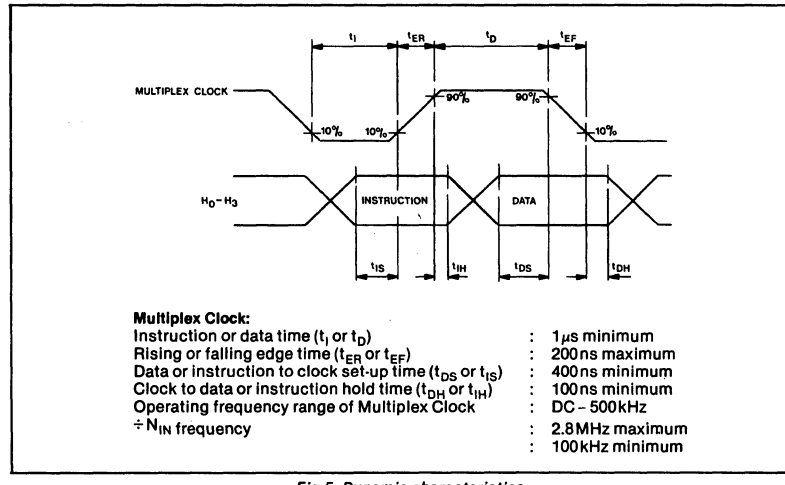


Fig.4 Phase comparator timing



Multiplex Clock:

Instruction or data time (t_I or t_D)	:	1µs minimum
Rising or falling edge time (t_{ER} or t_{EF})	:	200ns maximum
Data or instruction to clock set-up time (t_{DS} or t_{IS})	:	400ns minimum
Clock to data or instruction hold time (t_{DH} or t_{IH})	:	100ns minimum
Operating frequency range of Multiplex Clock	:	DC - 500kHz
$\div N_{IN}$ frequency	:	2.8MHz maximum
	:	100kHz minimum

Fig.5 Dynamic characteristics

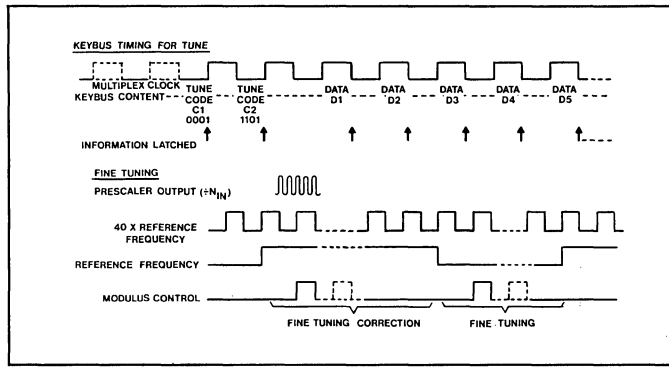


Fig.6 Simplified timing diagrams

PLESSEY
Semiconductors

CT2017

SYNTHESISER TUNING INTERFACE

The CT2017 is designed for use in Frequency Synthesis Tuning Systems, in particular the Plessey Key System.

The device contains a charge pump with a high impedance voltage follower, a signal detect circuit, a digital AFC circuit and a power on low detect circuit.

FEATURES

- Low Varicap Driver
- Active Filter Charge Pump
- Logic Level Control
- Signal Quality Detector
- AFC Input Option
- Auto Up, Auto Down Logic Level Tuning Correction
- Power Low Detector

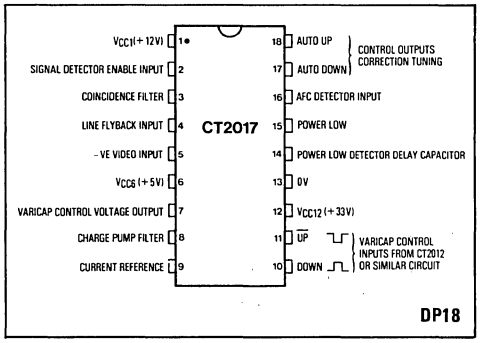


Fig.1 Pin connections

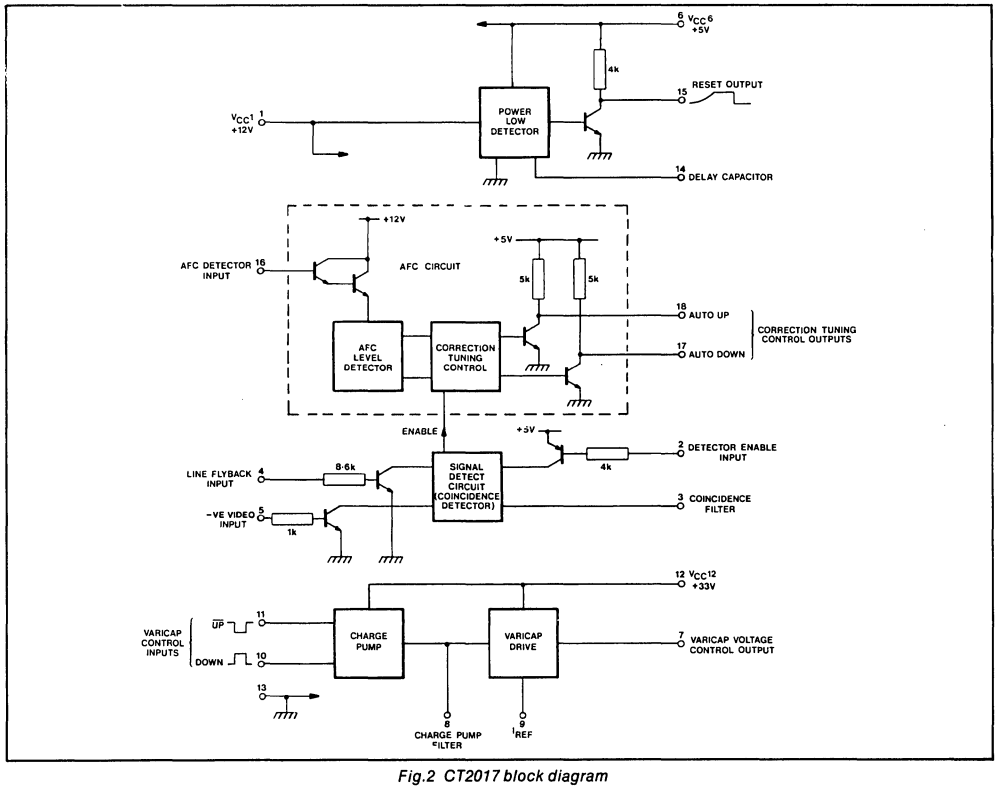


Fig.2 CT2017 block diagram

The charge pump is operated by two 5V logic inputs $\overline{UP}$ (active low) and DOWN (active high). These inputs turn on a charge current and discharge current respectively. The charge pump circuit and its voltage follower operate from the +33V supply rail. The combined charge pump, external filter and voltage follower may be used as the filter and varicap driver for synthesis tuning systems.

The signal detect circuit is used in tuning systems capable of automatically sweeping the received broadcast bands. The circuit examines the line synchronisation pulse and line flyback pulse for coincidence. When a regular supply of adequate coincident line synchronisation pulses occurs, the filter voltage falls. This indicates a received signal of a sufficient strength to produce a viewable picture.

When the signal detect filter voltage is higher than the signal detectors threshold the AUTO UP and AUTO DOWN outputs are clamped at Logic '0'. When the filter detect voltage is below the level detector's threshold the AUTO UP and AUTO DOWN outputs are enabled. The enabling of AUTO UP and AUTO DOWN may be used to indicate that a signal of adequate strength has been received and the sweep may be stopped.

Using appropriate external components, pin 5 may be used as a sync pulse separator, when fed with negative video or a positive line sync pulse input.

The signal strength recognised as good depends on the signal to noise ratio at the input to pin 5. This will depend on the type of sync separation used, whether noise gating is used and the noise figure of the signal processing circuits.

A digital AFC circuit, which comprises AFC level detector and correction tuning control, examines the AFC signal ('S' curve) produced by conventional television AFC circuits. The circuit produces an AUTO UP Logic '1' output when the AFC voltage is greater than the upper AFC threshold, and an AUTO DOWN Logic '1' output when the AFC voltage falls below the lower AFC threshold. Both outputs are Logic '0' when the AFC voltage is between the upper and lower thresholds.

CORRECTION TUNING

The AUTO UP and AUTO DOWN outputs may be used to adjust the correction tuning number of a synthesis tuning system and hence produce a digitally quantised AFC.

The power low detector circuit compares the +5V supply and the +12V supply against internal reference levels. When either supply falls below its relevant reference level the delay capacitor is discharged and the power low detector reset output is set to logic '1'. When the supplies exceed their relevant reference levels, the delay capacitor is charged to the threshold level, which turns on a transistor and the output is set to logic '0' after a delay.

The resulting output pulse may be used for setting the logic of the tuning synthesiser and for protecting the memory from corruption during power on and power off.

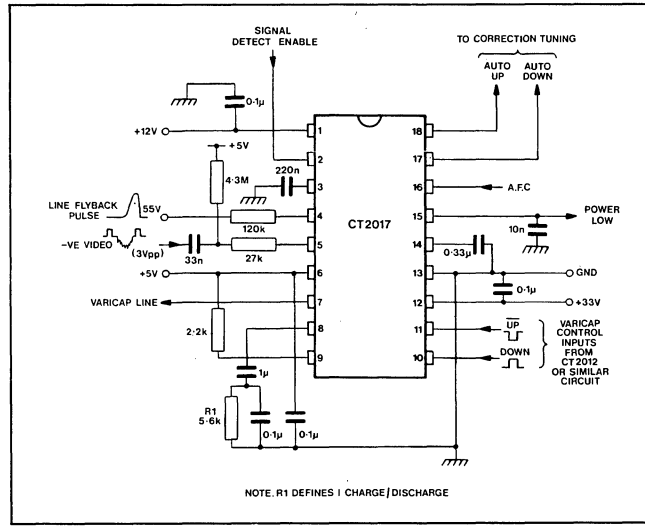
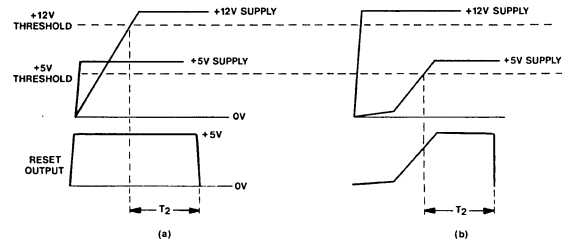


Fig.3 Test and application circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{CC1} = +12V$, $V_{CC6} = +5V$, $V_{CC12} = +33V$
Test circuit: Fig.3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range						
V_{CC1} (+12V)	1	10.8		13.2	V	
V_{CC6} (+5V)	6	4.5		5.5	V	
V_{CC12} (+33V)	12	31		36	V	
Supply current						
V_{CC1} (+12V)	1		8	12	mA	
V_{CC6} (+5V)	6		12	20	mA	$V_5 = 0V$, $V_{10} = 0V$, $V_{11} = 5V$
V_{CC12} (+33V)	12	3.3	4.5	5.5	mA	$I_9 = 2mA$, $V_{10} = 0V$, $V_{11} = +5V$
Varicap control						
Output range available	7	0.9		29.5	V	$I_9 = 2mA$ (R_9 2.2kΩ) $V_{CC}12 = 33.0V$
Output leakage current	7			40	nA	$V_{11} = +5V$, $V_{10} = 0V$
$\overline{UP}$ control input active	11			1	V	
$\overline{UP}$ control input inactive	11	3			V	
$\overline{UP}$ control input current	11			50	μA	$V_{11} = +5V$
DOWN control input active	10	3			V	
DOWN control input inactive	10			1	V	
DOWN control input current	10			50	μA	$V_{10} = +5V$
AFC control						
Detector high threshold	16	7.0	7.5	8.0	V	
Detector low threshold	16	4.1	4.5	4.9	V	
Detector window	16	2.8	3.0	3.2	V	
Input current	16			2.5	μA	$V_{16} = +12V$
Correction tuning outputs (AUTO UP, AUTO DOWN)						
Voltage high	17, 18	4.5			V	V_{17} high = DOWN; V_{18} high = UP Current source = 50μA
Voltage low	17, 18			0.5	V	Both low = inactive, current sink = 2mA
Line flyback threshold						
High	4	2			V	
Low	4			0.7	V	
Negative video input						
Threshold	5		0.7		V	
Sync pulse switching current	5			12	μA	
Leakage current	5			0.3	μA	$V_5 = -5V$
Coincidence detector						
Enable	2	4.5			V	
Inhibit	2			2	V	
Threshold	3		2.4		V	
Power on detector						
Output voltage	15	4.5			V	Current source = 50μA
Normal				0.5	V	Current sink = 2mA
Detector threshold						
V_{CC1} (+12V)	1	9.2	9.9	10.6	V	See Figs.4 and 5
V_{CC6} (+5V)	6	3.7	4	4.3	V	See Figs.4 and 5
Delay capacitor charging current	14		10		μA	
Delay threshold	14		9		V	



Notes

1. T_2 period timed by delay capacitor
2. Output is connected to +5V supply via a pull-up resistor
3. T_2 is set by value of capacitor, charging current and output threshold voltage. Charging current is normally 10μA. Threshold voltage is normally 9V.

Fig.4 Power low detector timing diagram (Power on)

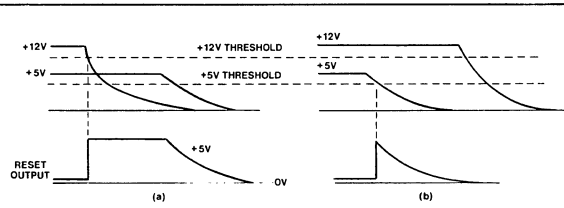


Fig.5 Power low detector timing diagram (Power off)

ABSOLUTE MAXIMUM RATINGS

+12V supply (V_{CC1})	+20V
+5V supply (V_{CC6})	+20V
+33V supply (V_{CC12})	+40V
Operating temperature range	-10°C to +65°C
Storage temperature range	-55°C to +125°C

PLESSEY
Semiconductors

CT2200

5-BIT BINARY TO 13-SEGMENT DECODER/DRIVER

The CT2200 is an N-channel MOS integrated circuit, designed to directly drive two 7-segment LEDs to display the numbers 1 to 32, with leading zeros suppressed. The circuit is ideal for applications such as the programme number display of a television receiver. The display is controlled by a 5-bit binary input port, weighted so that the number shown (1-32) is one more than the binary input (0-31) to avoid programme 0. The 5 lines can come from a remote control receiver or from any other source of continuous 5-bit data.

Common anode LEDs can be driven directly with a current limiting resistor in series with each output (see Fig.5) or by using some other form of brightness control (see Fig.6). By driving each segment individually the interference problems associated with multiplexed displays are avoided.

A blanking input is provided so that the display can be turned off or can be made to flash with an external pulsed signal.

Only 13 lines are needed for two 7-segment displays because segment Tf is never lit for the numbers 1 to 32 and so does not need to be decoded and driven. Segment identification is shown in Fig.2.

The 13 outputs of the output encoder drive the gates of large output transistors to give two states: OFF and SINK CURRENT; as there can be up to 12 outputs on at once, each sinking 20mA, four 0V pins are provided to reliably carry this current. **ALL FOUR PINS (3, 7, 18, 22) MUST BE CONNECTED TO 0V.**

The number of segments required for each character is shown in Fig.3.

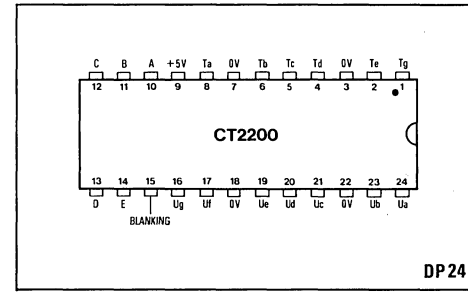


Fig.1 Pin connections

FEATURES

- Direct Segment Drive — Non-Multiplexed
- 5V Supply
- Blanking Input
- Leading Zero Suppressed
- Minimum Segment Pattern per Character
- 20mA Drive per Segment
- 5-Bit Binary Input

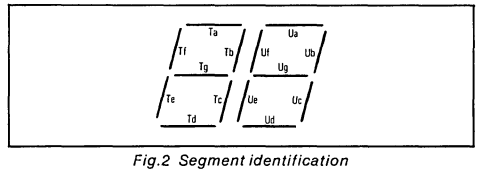


Fig.2 Segment identification

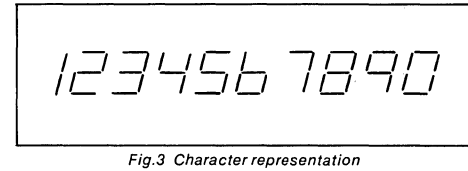


Fig.3 Character representation

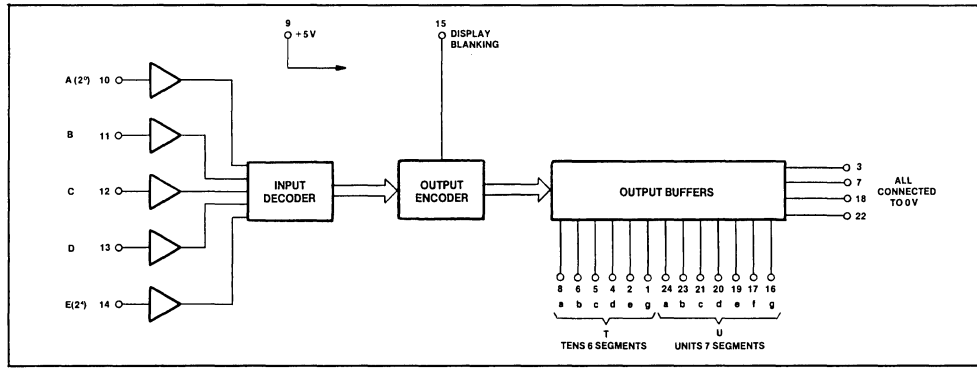


Fig.4 Block diagram

ELECTRICAL CHARACTERISTICS (see Fig.5)

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{DD} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	9	4.5	5	5.5	V	
Supply current	9			5	mA	
Input voltage high	10-14	4			V	
Input voltage low	10-14			0.8	V	
Leakage current	10-14			10	μA	$V_{IN} = +5V$
Capacitance	10-14			10	pF	
Output voltage	1, 2, 4-6, 8, 16, 17, 19-21 23, 24			1	V	Sinking 20mA
Recommended series resistor (if used)			120		Ω	

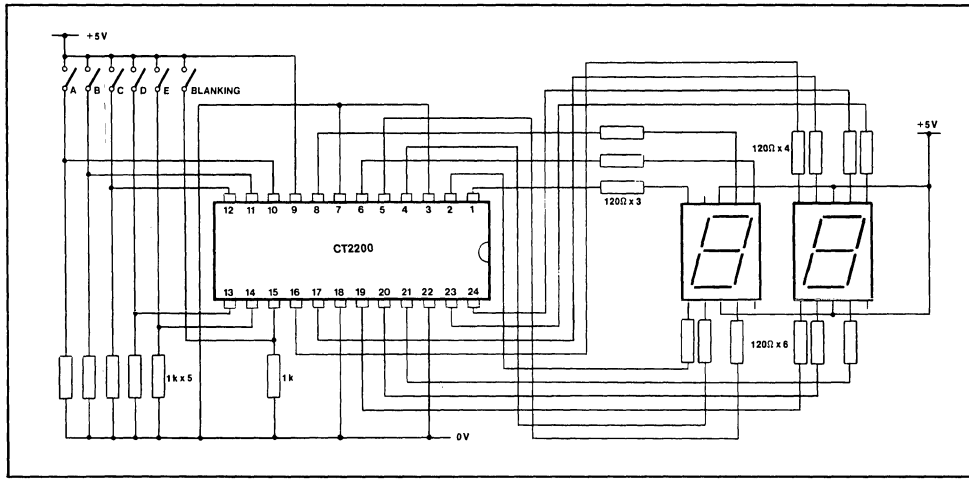


Fig.5 Test circuit and application using load resistors (see also Fig.6)

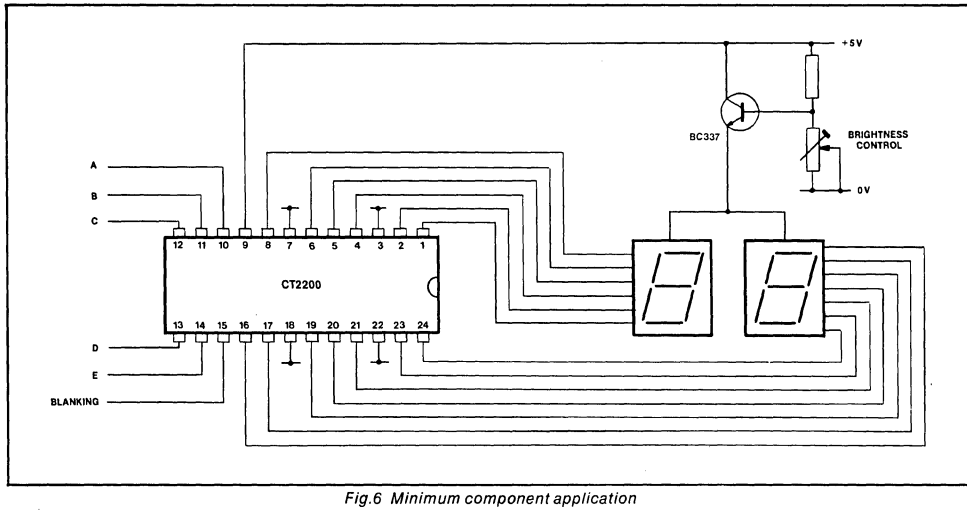


Fig.6 Minimum component application

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	+7V
Input or output voltage	+7V
Output current	30mA
Ambient operating temperature	−10°C to +65°C
Storage temperature	−55°C to +125°C

ML231B

MOS TOUCH TUNER

The ML231B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates — replacing conventional mechanical push-buttons for channel selection. Neons may be used to indicate the selected channel, while the latched output of the ML231B drives the varicap tuner via a bias selection network.

An additional output is provided which goes high with no channel selected and may be used externally to select channel 3 so as to prevent the existence of a null state.

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, V_{SS}–V_{DD}	36V
Varicap voltage V_{SV} w.r.t. V_{SS}	+0.3V

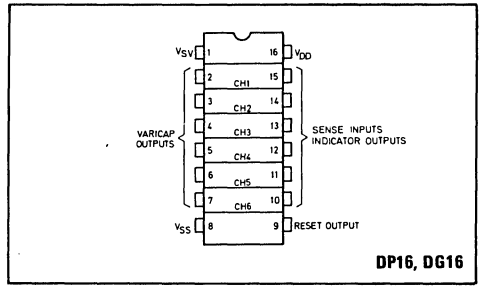


Fig. 1 Pin connections

FEATURES

- Six-channel Capability
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Low Current Drain
- Reset O/P Prevents Null State

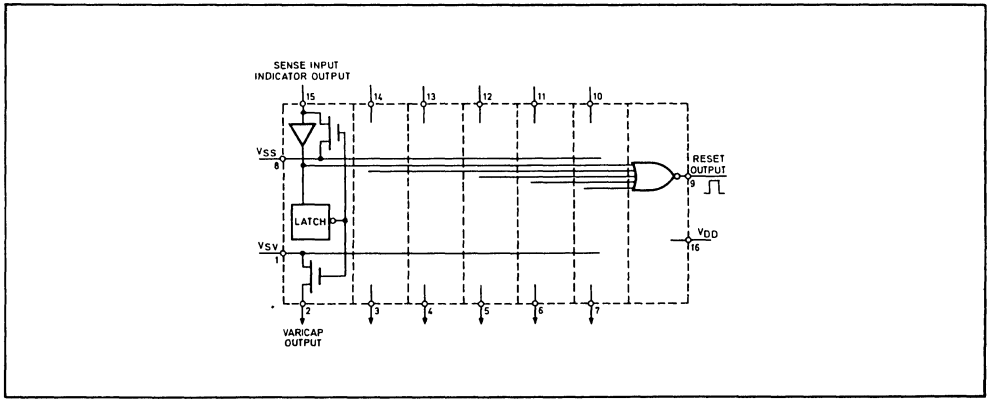


Fig. 2 Functional diagram
(positive logic)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input current			1	μA	V_{in} = 0V
Supply current	2	4	5.5	mA	
R_{ON} of varicap switch		50	100	Ω	Iout = 10mA
R_{ON} indicator switch		125	250	Ω	Iout = 4mA
Sense input threshold	$0.4V_{SS}$	$0.5V_{SS}$	$0.6V_{SS}$	V	
Reset O/P voltage high	V_{SS} −10			V	Iout = 0.5mA

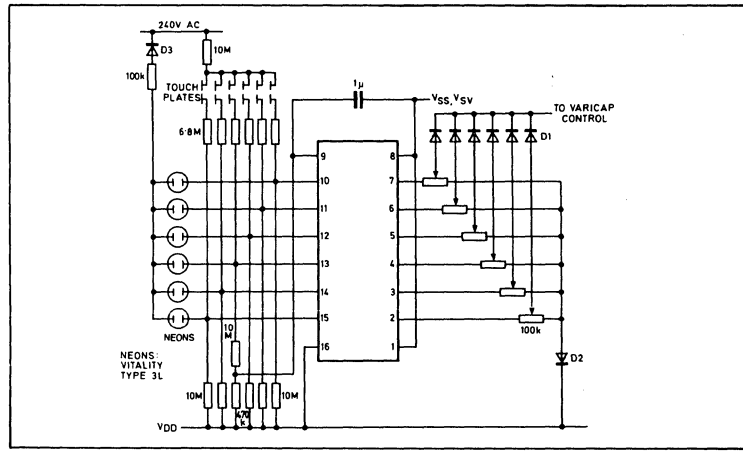


Fig. 3 Typical application circuit

Reset output = $\overline{CH1 \cdot CH2 \cdot CH4 \cdot CH5 \cdot CH6}$

= $\overline{1+2+3+4+5+6+3}$

ML232B

MOS TOUCH TUNER

The ML232B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates — replacing conventional mechanical push-buttons for channel selection. Neons may be used to indicate the selected channel, while the latched output of the ML232B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input pin, will cause the selected channel output to advance by one.

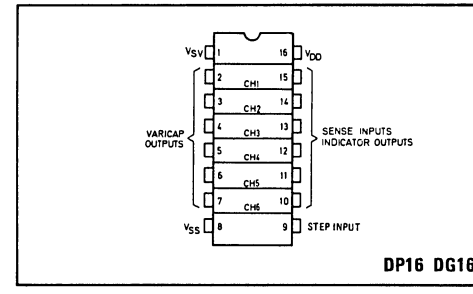


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, V_{SS}–V_{DD}	36V
Varicap voltage V_{SV} w.r.t. V_{SS}	+0.3V

FEATURES

- Six-channel Capability
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Low Current Drain
- Remote Control Stepping Facility

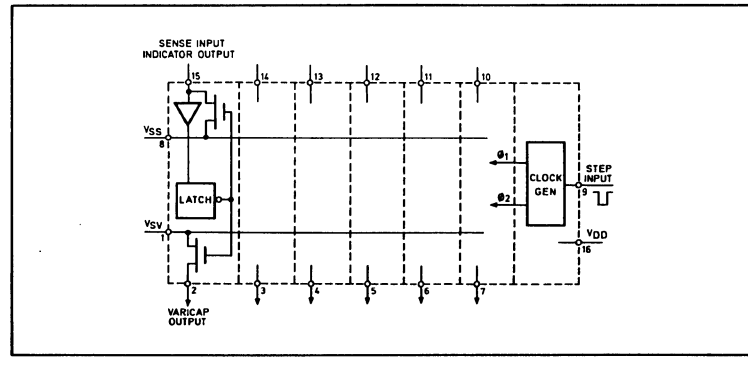


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input current			1	μA	V_{in} = 0V
Supply current	2	4	5.5	mA	
R_{ON} of varicap switch		50	100	Ω	Iout = 10mA
R_{ON} of indicator switch		125	250	Ω	Iout = 4mA
Sense input threshold	0.4V_{SS}	0.5V_{SS}	0.6V_{SS}	V	
Step pulse level	0		V_{SS} −29	V	
Step pulse width	0.1		1	ms	T_{amb} = 0°C to +65°C

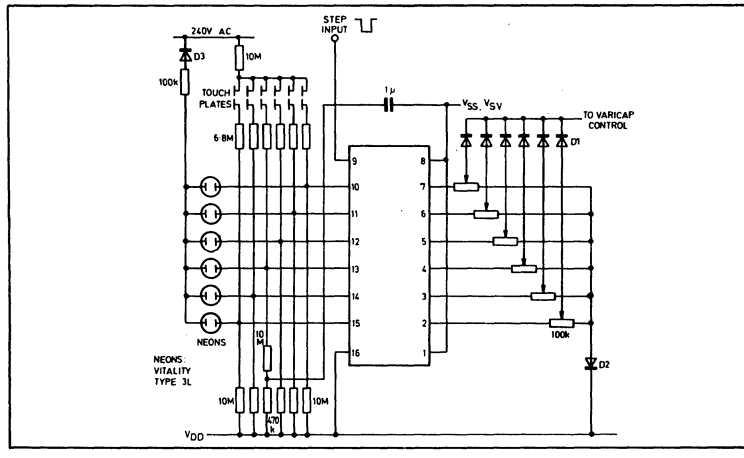


Fig. 3 Typical application circuit

ML236B

6-CHANNEL CASCADABLE TOUCH CONTROL INTERFACE

The ML236B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons or LEDs may be used to indicate the selected channel, while the latched output of the ML236B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse causes the selected channel to advance by one.

FEATURES

- 6-Channel Capability – Cascadable
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Facility
- A Negative Pulse on Clear Resets All Channels

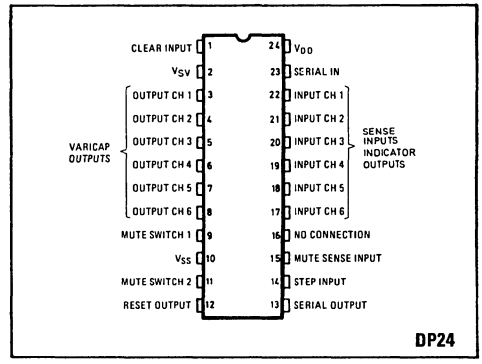


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Vss −VDD supply	36V
Varicap voltage VSV	Vss +0.3V

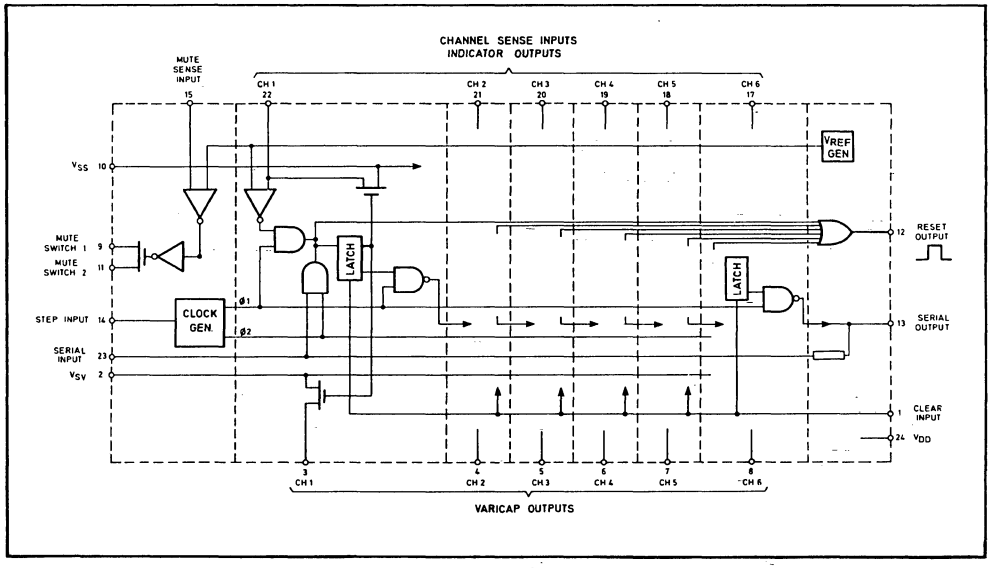


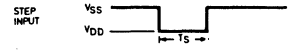
Fig. 2 ML236B functional block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3	5	mA	
Input current			1	µA	V_{IN} = 0
R_{ON} of varicap switch		60	125	Ω	I_{OUT} = 8mA
R_{ON} of indicator switch		125	250	Ω	I_{OUT} = 4mA
V_{th} sense I/P threshold	0.4	0.5	0.6	Vss	
Clear, step pulse level	0		Vss –10	V	
Ts step pulse width	0.2		1	ms	
Clear pulse width	0.2			ms	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
Serial and reset O/P	Vss –1			V	'1'
			Vss –11	V	'0'
Serial and reset I/P	Vss –1.5			V	'1'
			Vss –10	V	'0'

NOTES
Stepping selection:



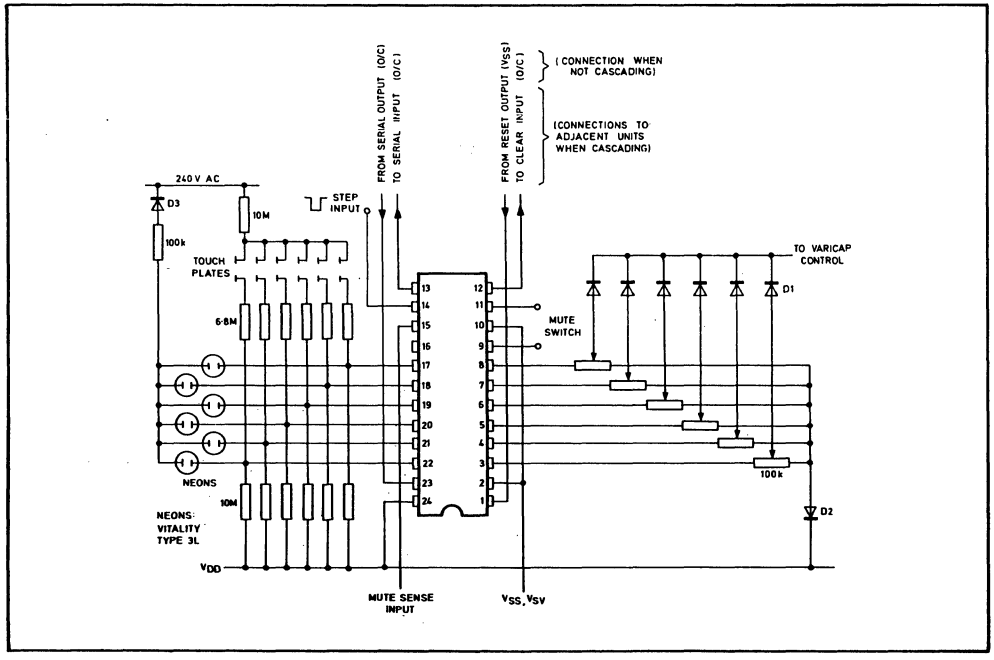


Fig. 3 Typical applications using neons as channel indicators

APPLICATION NOTES

Application using LEDs as channel indicators

In applications where the use of mains is not desired channel selection can be made by using the +30V V_{SS} supply as a compromise but at the expense of reduced input sensitivity. In this case LEDs can be used as channel indicators.
Sensitivity may be improved at lower voltage by using a tapped LED current limiting resistor to derive a higher input voltage. (Fig. 5)

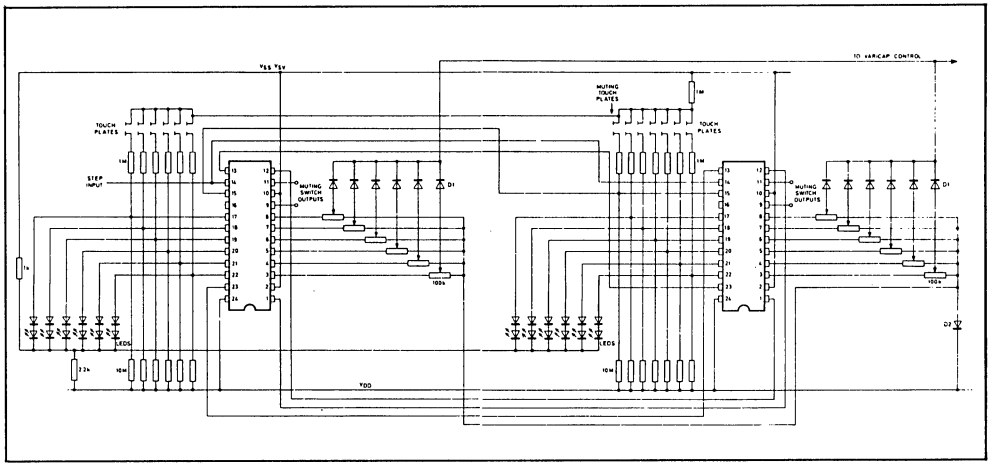


Fig. 4 12-channel application using LEDs as indicators

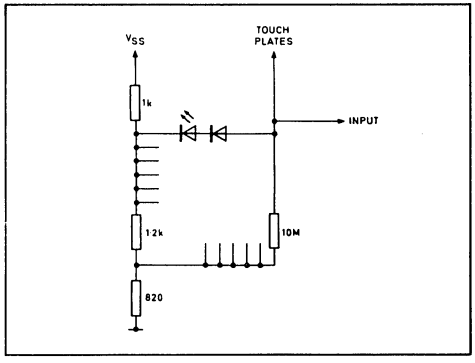


Fig. 5 Improved sensitivity for 33V operation

ML237B

6-CHANNEL TOUCH CONTROL INTERFACE

The ML237B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML237B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

FEATURES

- 6-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selected Channel 1 on Power-up
- Channels Are Selected With a Negative (or Earth) Input

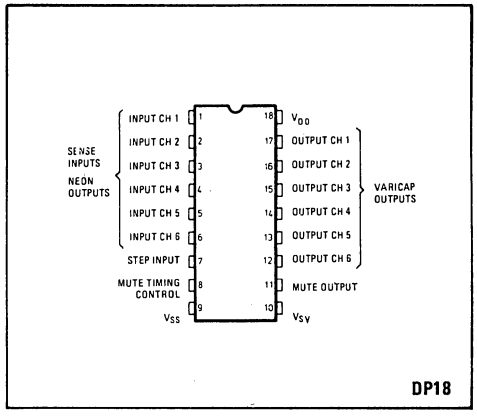


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, V_{SS}–V_{DD}	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

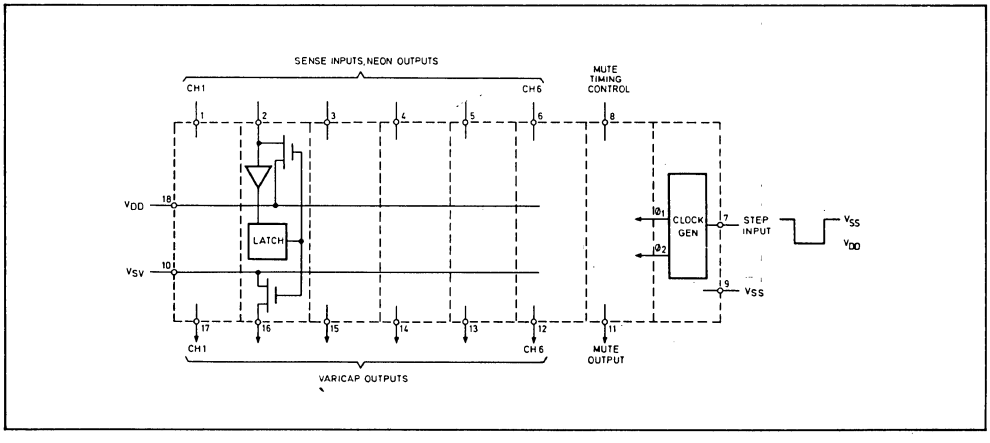


Fig. 2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

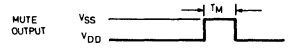
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current			1	μA	$V_{IN} = V_{SS}$
Output leakage			1	μA	V_{OUT} = 0
Mute switch O/P leakage			10	μA	V_{OUT} = 0
Supply current		5	8	mA	
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
Step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
Mute switch R_{ON}		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	Vss	
Step input current	10		1000	μA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68 μF
Step pulse level	0		Vss −29	V	

NOTES

The mute timing can be increased by using a higher value of capacitor (C_M)

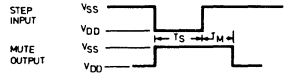
Touch plate selection:



Tm ≃ Cm x 0.6ms/nF

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_S

Stepping selection:



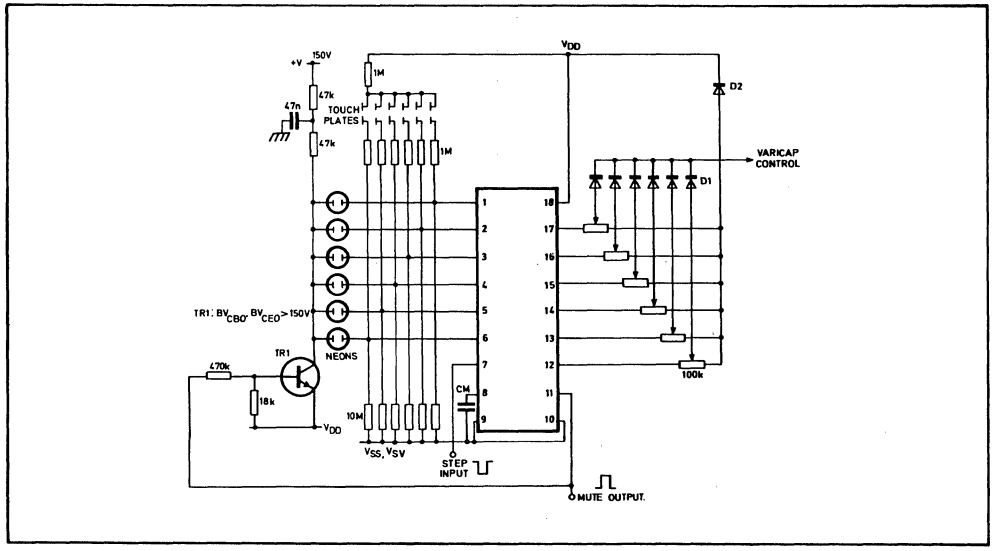


Fig. 3 Typical applications using neons as channel indicators

ML238B

8-CHANNEL TOUCH CONTROL INTERFACE

The ML238B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons or LEDs may be used to indicate the selected channel, while the latched output of the ML238B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel to advance by one.

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1

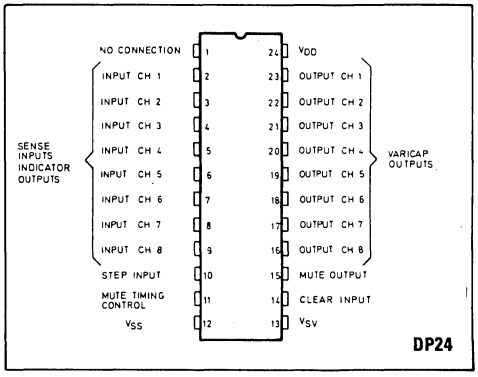


Fig 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, Vss–VDD	36V
Varicap voltage Vsv	Vss +0.3V

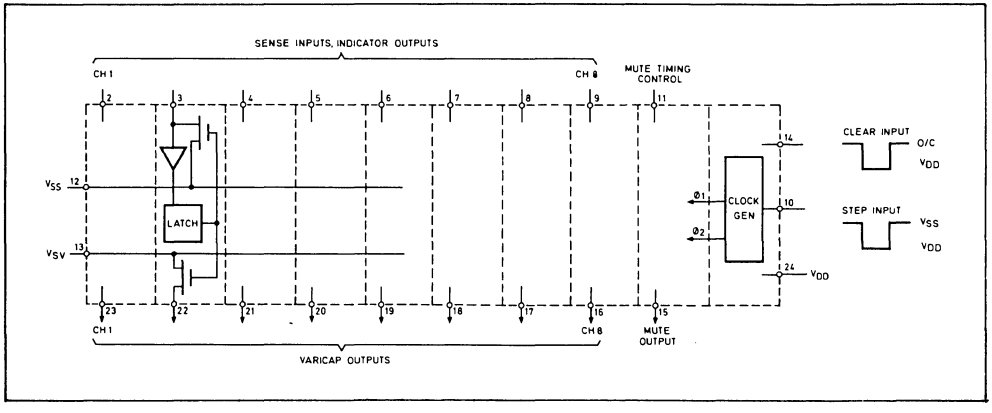


Fig. 2 Functional block diagram

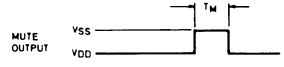
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Output leakage			1	µA	V_{out} = 0
Supply current		6	9	mA	
Input current			1	µA	V_{in} = 0V
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
R_{ON} of indicator switch		180	300	Ω	I_{OUT} = 10mA
I/P threshold	0.4	0.5	0.6	V_{SS}	
Step pulse level	0		V_{SS} −29	V	
T_S step pulse width	0.2			ms	>.0 5 Tm
Clear pulse level	0		V_{SS} −29	V	
Clear pulse width	0.2			ms	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
T_m mute timing		400		ms	Cm = 0.68µF
Step I/P current	10		1000	µA	V_{in} = 0
Mute O/P leakage			10	µA	V_{OUT} = 0

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m) (See Fig. 4).

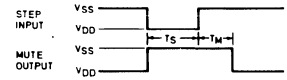
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

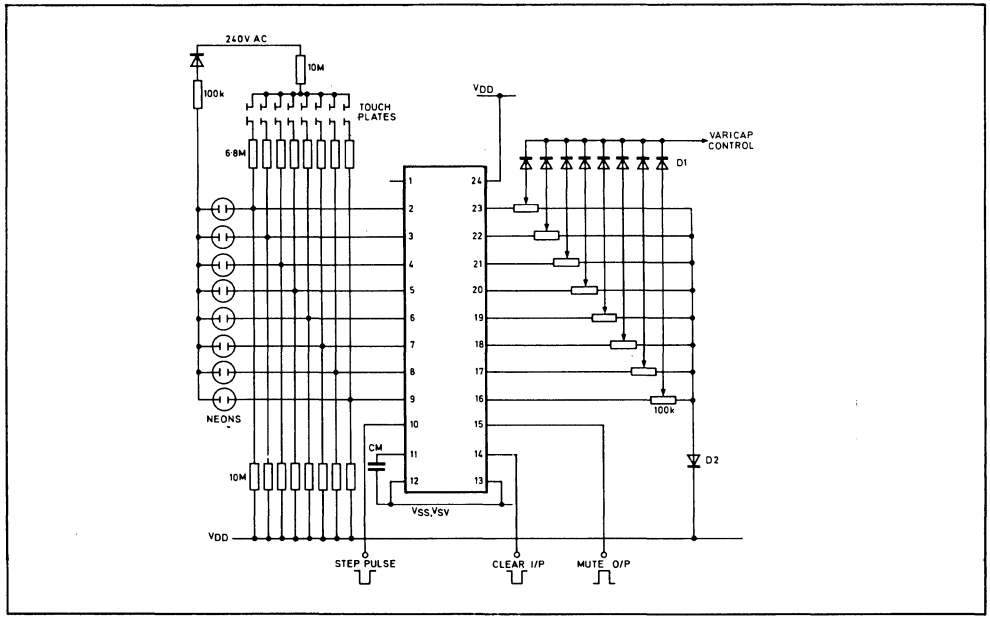


Fig. 3 Typical applications using neons as channel indications.

APPLICATION NOTES

Application using LEDs as channel indicators

In applications where the use of mains is not desired channel selection can be made by using the +30V V_{SS} supply as a compromise but at the expense of reduced input sensitivity. In this case LEDs can be used as channel indicators.
The 1.2kΩ and 820Ω resistors limit the LED current to 10mA, whilst the diode ensures less than 1μA leakage when the LED is reverse biased. It is desirable to have a 1MΩ resistor between the touch plates and the input as a safeguard against static.
On selection of a channel, the potential divider chain comprising the 1MΩ resistor, the finger resistance and the 10MΩ resistor sets the threshold voltage on the input pin. When the channel is selected the IC provides a current source to the LED.

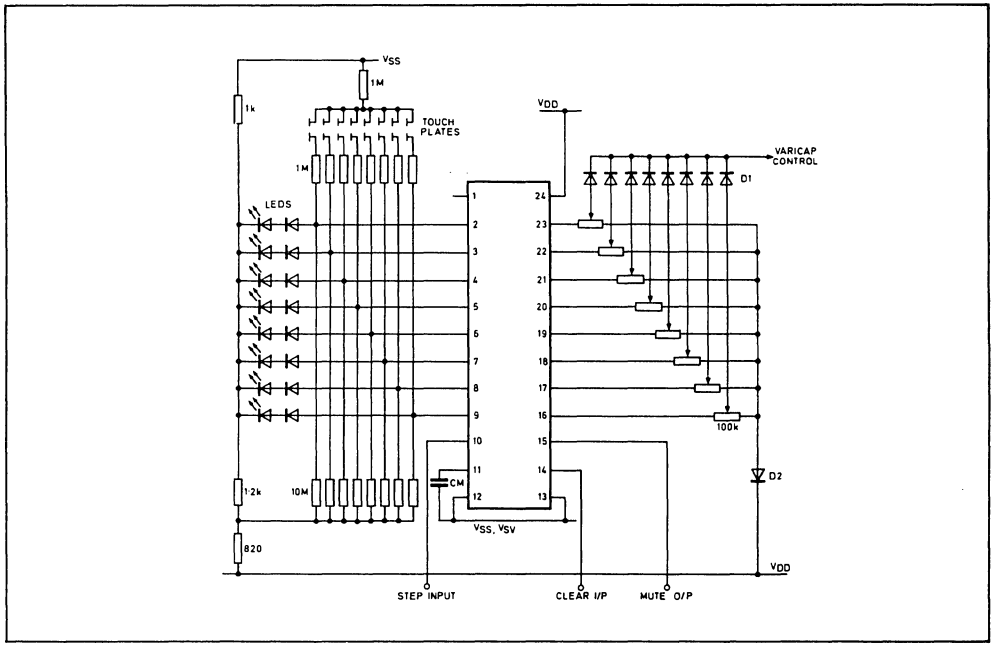


Fig. 4 Low voltage, improved sensitivity using LED indicators

ML239B

8 – CHANNEL TOUCH CONTROL INTERFACE

The ML239B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML239B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

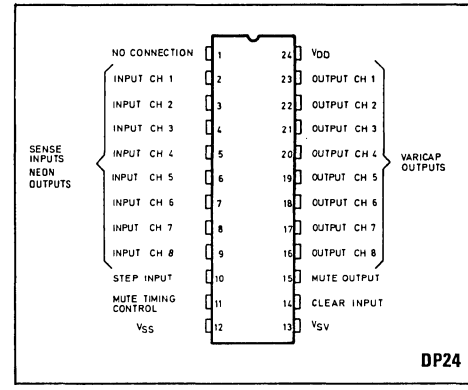


Fig. 1 Pin connections

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1
- Channels are Selected with a Negative (or Earth) Input

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	–10°C to +65°C
Storage temperature	–10°C to +85°C
V_{SS}–V_{DD} supply	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

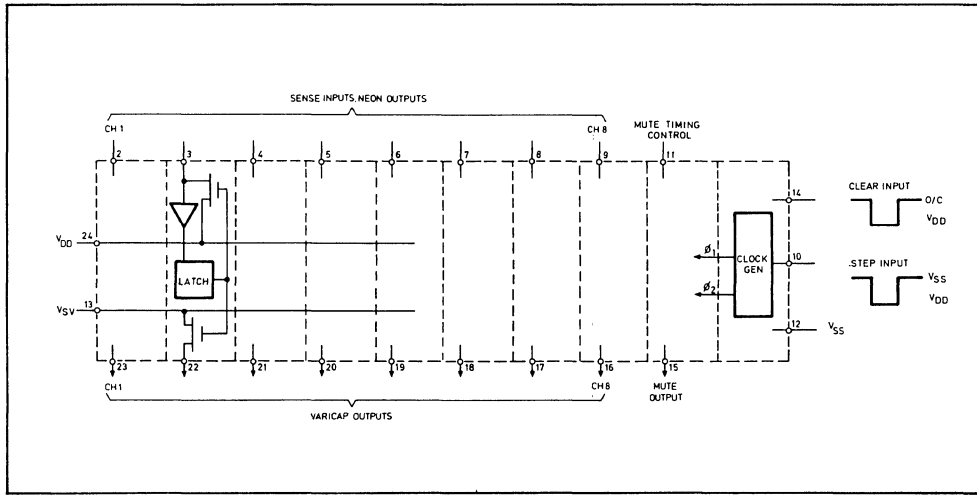


Fig. 2 Functional Block Diagram

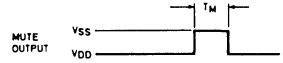
ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Step, clear pulse level	0		V_{SS} −29	V	
Input current			1	µA	V_{IN} = V_{SS}
Output leakage			1	µA	V_{OUT} = 0
Mute switch O/P leakage			10	µA	V_{OUT} = 0
Supply current		6	9	mA	
R_{ON} of varicap switch		50	1000	Ω	I_{OUT} = 10mA
Clear step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1	mA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68µF

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m)

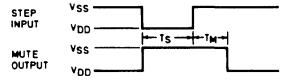
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

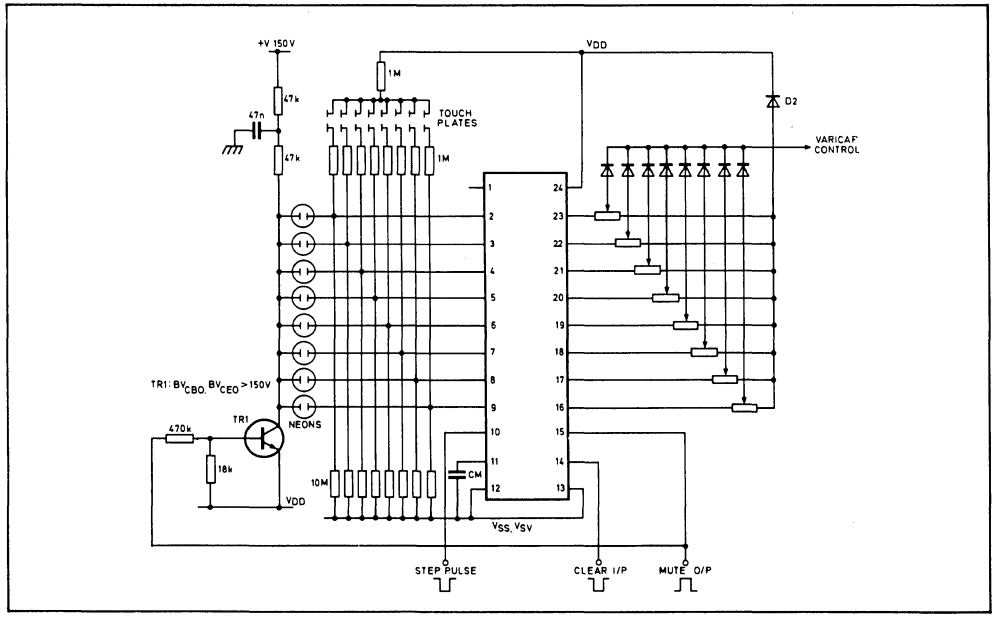


Fig. 3 Typical applications using neons as channel indications

PLESSEY
Semiconductors

ML920
REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML920 demodulates the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 20 programme memory or one of three D/A converters.

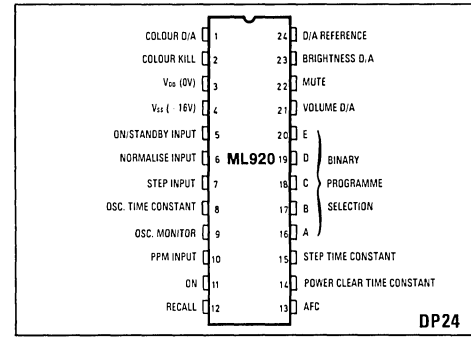


Fig. 1 Pin connections

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 5 bit binary, 20 programmes
- Analogue controls: 3 static current mirror converters, 32 step with normalise level
- Other outputs: On, Recall Display, AFC, Mute, Colour Kill, Oscillator Monitor
- Local inputs: On/Standby, Step, Normalise

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used With Ultrasonic or Infra-red System
- Up to 20 Programmes With Latched Binary Output
- 3 D/A Outputs With Normalise Level At $\frac{3}{8}$ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Colour Kill, Recall etc.

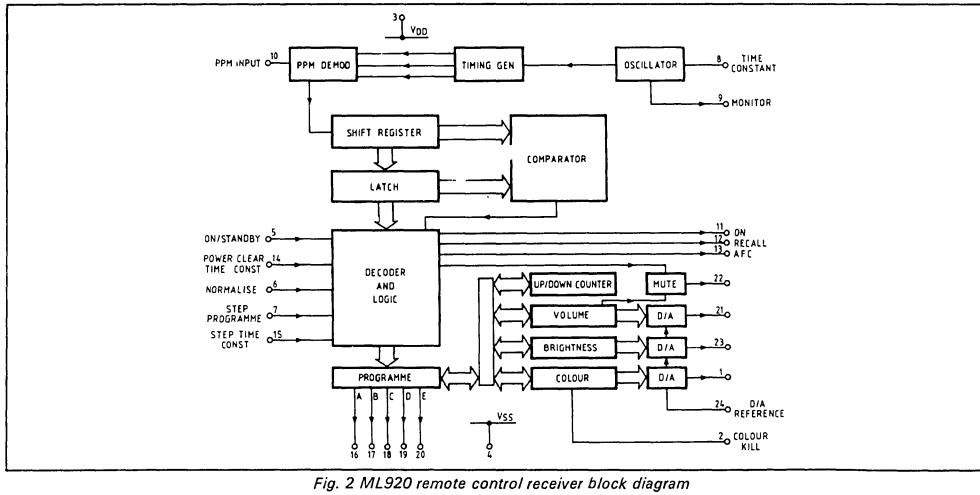


Fig. 2 ML920 remote control receiver block diagram

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):

V_{SS} = 0V
V_{DD} = −16V
T_{amb} = 25°C

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5, 6, 7,	−1		0	V	
low		V_{DD}		V_{DD} +3.5	V	
Output logic level high	2, 11-13, 16-20, 22	−1		0	V	50k to V_{DD}
low		V_{DD}		V_{DD} +0.5	V	50k to V_{DD}
Analogue output current range (pins 1, 21, 23)	1, 21, 23	0		$\frac{31}{8}$	I_{REF}	3.9k to V_{DD}
Analogue step size	1, 21, 23	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{REF}	$V_{out} < V_{DD}$ +5V
D/A reference, I_{REF}	24	−250	−345	−455	μA	33k to V_{DD}
Oscillator timing	9		1.5k		Hz	C = 22n, R=100k See note 1
Power clear time constant	14		400		ms	C = 4.7μ R=100k
Step time constant	15		1		s	C = 470n R = 3.3M
Monitor output 'high'	9	−1		0	V	Internal load
'low'		V_{DD}		V_{DD} +0.5	V	provided
PPM input logic level high		-1		0	V	
PPM input logic level low	10	V_{DD}		-6	V	
PPM input pulse width		1		$22T_{osc}$	μs	$T = \frac{1}{f_{osc}}$

Note 1. R_{osc} (Pin 8) is 47k - 200kΩ, 2fmon (Pin 9) = $f_{osc} \simeq \frac{1}{0.15CR}$

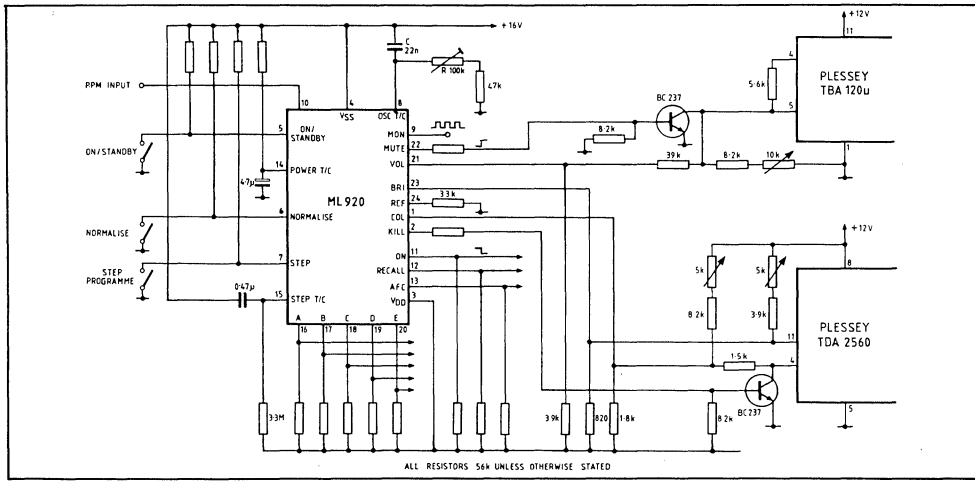


Fig. 3 PPM receiver application

PIN FUNCTIONS

Negative Logic: 0 is 0V (V_{SS}), 1 is −17V (V_{DD})

1, 21, 23. Colour, Volume, Brightness
These three outputs are from three 5 bit current mirror D/A converters. They are referenced to the current drawn from pin 24, I_{ref}, and give 32 steps, $I_{ref}/8$ per step, from 0 to 31/8 I_{ref}. The outputs will be set to 12/8 I_{ref} by the NORMALISE input, the normalise code from the transmitter, or when the ON output goes to a 1.

2. Colour kill
This output gives a logic 0 when the COLOUR D/A output is zero.

3. V_{DD}
−17V power supply

4. V_{SS}
0V power supply

5. On/Standby input
A 1 on this pin will toggle pin 11 (ON O/P), generate

RECALL and AFC, normalise VOLUME, BRIGHTNESS and COLOUR, reset MUTE and set channel code 00000.

6. Normalise input

A 1 will normalise the VOLUME, BRIGHTNESS and COLOUR outputs. A RECALL signal is generated and MUTE is reset.

7. Channel step

The channel code will step up by 1 as long as this pin is held at logic 1. The time period between steps is defined by an RC constant attached to pin 15. On reaching 20 the next step returns to 1. On output is set to ON, and AFC is generated. If the TV goes from Standby to ON, RECALL is generated and VOLUME, BRIGHTNESS and COLOUR are normalised. If VOLUME is not 0, MUTE is reset.

8. Oscillator time constant

An RC time constant is formed for the clock timing by connecting external components, one resistor and one capacitor, to this pin. Adjusted so that period of output on pin 9 is 1/20 of 0 interval of incoming PPM.

9. Oscillator monitor

This output is a division of two of the oscillator, and and is available for testing and setting purpose.

10. PPM I/P

The output of the front end amplifier is connected here such that the signal is in the form of positive pulses separated by time periods whose length define the data. With no signal, PPM input is at a logic 1.

11. On O/P

Open drain output. Logic 1 denotes TV set ON: Logic 0 TV set standby. Set to 1 when channel number changes. Set to 0 by power clear or by transmitter selected Standby. Toggle to opposite state by manual ON/STANDBY control.

12. Recall O/P

Open drain output. A 1 may be used to trigger an on-screen display. A static output is generated by the manual controls ON/STANDBY and NORMALISE.

A pulse is generated by any channel change if the circuit switches to ON at the time, and by RECALL and NORMALISE commands from the transmitter.

13. AFC O/P

Open drain output. Logic 1 can inhibit the tuner AFC.

A static output is generated bymanual ON/STANDBY control. A pulse is generated by any channel number change.

14. Power clear

A capacitor and resistor connected here define the time delay for the power clear circuit, which normalises all D–A outputs etc.

15. Channel step time constant

An R–C time constant defines the time period between increments of the channel number when stepping.

16 –20. Channel outputs

5 Outputs encode 20 channel numbers in binary code

EDCBA
Channel 1 is 00000
Channel 20 is 10011

E is first and A is last in the PPM pulse train.

Channel 1 is set when ON goes to a 1

21. Volume.

See Pin 1

22. Mute O/P

This will change state (toggle) on reception of a mute command and VOLUME O/P is zero MUTE O/P is held at 0.

23. Brightness

See Pin 1

24. D/A Reference

A current drain I_{ref}, set by a single external resistor will set the nominal step of the D/A outputs to $I_{ref}/8$.

Transmitter code	Function
EDCBA	
00000	Programme 1
00001	Programme 2
00010	Programme 3
00011	Programme 4
00100	Programme 5
00101	Programme 6
00110	Programme 7
00111	Programme 8
01000	Programme 9
01001	Programme 10
01010	Programme 11
01011	Programme 12
01100	Programme 13
01101	Programme 14
01110	Programme 15
01111	Programme 16
10000	Programme 17
10001	Programme 18
10010	Programme 19
10011	Programme 20
10100	Colour +
10101	Programme Step +
10110	Volume +
10111	Brightness +
11000	Standby
11001	Mute
11010	Recall
11011	Normalise
11100	Colour –
11101	Programme Step –
11110	Volume –
11111	Brightness –

Table 1 Basic 32 command set

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to –25V
Voltage at any input	+0.3V to –25V
Operating voltage range, V_{DD}	–14V to –18V
Maximum power dissipation	600mW
Operating temperature range	–10°C to +65°C
Storage temperature range	–55°C to +125°C

PLESSEY
Semiconductors

ML922

REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML922 demodulates the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 10 programme memory or one of three D/A converters.

The receiver timing may be set by adjusting the oscillator time constant to give 40 periods at pin 6 equal to a 0 interval on the received PPM input.

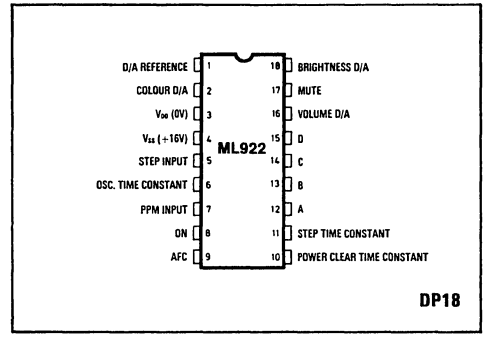


Fig. 1 Pin connections

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used With Ultrasonic or Infra-red System
- Up to 10 Programmes With Latched Binary Output
- 3 D/A Outputs With Normalise Level At $\frac{3}{8}$ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Etc.

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 4 bit binary, 10 programmes
- Other outputs: On, AFC, Mute
- Local inputs: Programme step

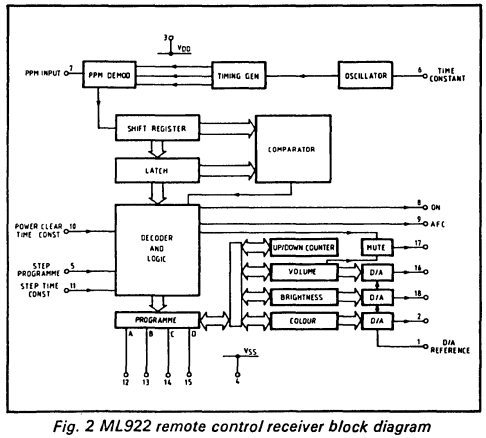


Fig. 2 ML922 remote control receiver block diagram

Transmitter code	Function
EDCBA	
0000X	Programme 1
0001X	Programme 2
0010X	Programme 3
0011X	Programme 4
0100X	Programme 5
0101X	Programme 6
0110X	Programme 7
0111X	Programme 8
1000X	Programme 9
1001X	Programme 10
10100	Analogue 1 +
10101	Programme Step +
10110	Analogue 2 +
10111	Analogue 3 +
11000	Standby
11001	Mute (Analogue 2)
11011	Normalise
11100	Analogue 1 –
11101	Programme Step –
11110	Analogue 2 –
11111	Analogue 3 –

Table 1 Basic 21 command set for ML922

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):
V_{SS} = 0V
V_{DD} = −16V
T_{amb} = 25°C

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5	−1		0	V	
low		V_{DD}		V_{DD} + 3.5	V	
Output logic level high	8, 9, 12-15, 17	−1		0	V	50k to V_{DD}
low		V_{DD}		V_{DD} + 0.5	V	50k to V_{DD}
Analogue output current range	2, 16, 18	0		$\frac{31}{8}$	I_{ref}	3.9k to V_{DD}
Analogue step size	2, 16, 18	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{ref}	V_{out} < V_{DD} +5V
D/A reference, I_{REF}	1	−250	−345	−455	µA	33k to V_{DD}
Oscillator timing	6		3		kHz	C = 22n, R = 100k See note 1
Power clear time constant	10		400		ms	C = 4.7µ R = 100k
Step time constant	11		2		s	C = 470n R = 3.3M
PPM input logic level high	7	-1		0	V	
PPM input logic level low	7	V_{DD}		-6	V	
PPM input pulse width	7	1		22T_{OSC}	µs	

Note 1. $R_{osc.}$ (pin 6) is 25k → 200kΩ. $f_{osc.} \simeq \frac{1}{0.15CR}$

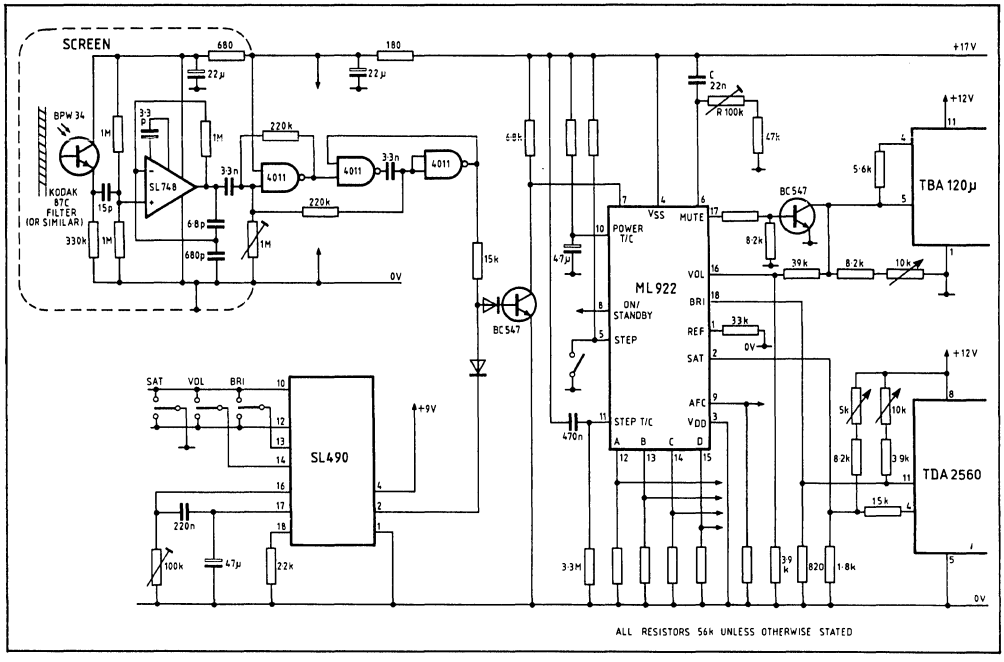


Fig. 3 PPM infra-red receiver application with local up/down controls using a directly connected SL490

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to −25V
Voltage at any input	+0.3V to −25V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

PLESSEY
Semiconductors

ML923

REMOTE CONTROL RECEIVER

The ML923 is an MOS/LSI monolithic integrated circuit for use as a receiver of remote control signals for television control. It accepts 24 of the 32 codes transmitted by the SL490 transmitter circuit in the Pulse Position Modulation (PPM) method of coding.

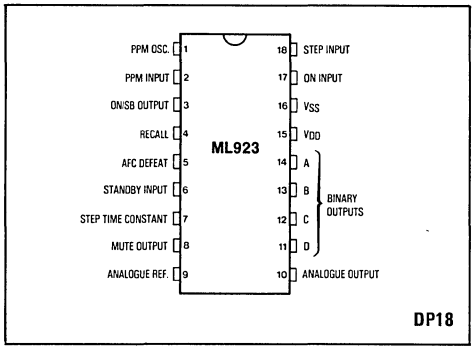


Fig.1 Pin connections

FEATURES

- 16 Channel Selection Codes
- Single Analogue Output
- Mute Output (Toggle)
- On-set Controls — Channel Step, ON, Reset
- Normalise to $\frac{3}{8}$ of Max Output on Analogue Output
- Outputs Provide Control of ON/STANDBY, Analogue Mute, and AFC Defeat
- Choice of Power-Up Function:
  a) Power Up to Standby State, Switch to ON State by Local or Remote Command and STANDBY by Remote Command.
  b) Power Up to ON State, Switch OFF with Solenoid Operated Mains Switch by Local or Remote Command.

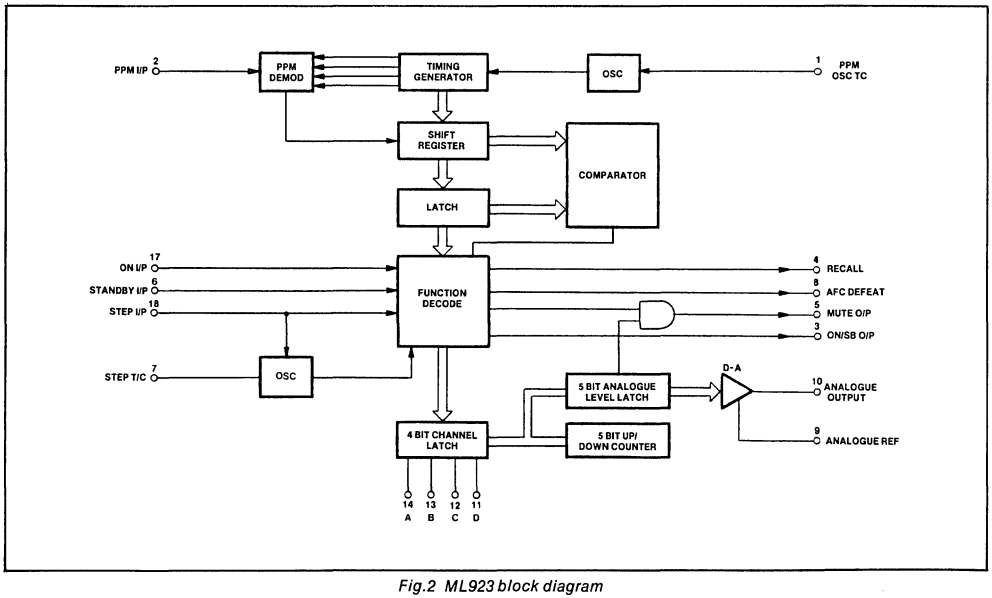


Fig.2 ML923 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{SS} = 0V$, $V_{DD} = -16V$

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1	14		18	V	
Supply current	1		6		mA	
Input logic level high	6, 17, 18	-1		0	V	
Input logic level low		V_{DD}		$V_{DD}+3.5$	V	
Output logic level high	3, 4, 11, 14	-1.5		0V	V	50k to V_{DD}
Output logic level low	8	V_{DD}		$V_{DD}+0.5$	V	
Analogue output current range	10	0		$\frac{31}{8}$	1 Ref	3.9k to V_{DD}
Analogue step size	10	0	$\frac{1}{8}$	$\frac{1}{4}$	1 Ref	$V_{out} < V_{DD}+5V$
D/A reference, I ref	9	-250	-345	-455	mA	33kΩ to V_{DD}
PPM		15		150k	Hz	Typical TC
Oscillator frequency	1		3k		Hz	C = 22nF R = 100kΩ
On input or standby input time constant for power on	6 or 17	250		500	ms	
Step time constant	7		1		s	C = 470nF R = 3.3MΩ
PPM input logic level high ('1')	2	-1		0	V	
PPM input logic level low ('0')	2	V_{DD}		-6	V	
PPM input pulse width	2	1		22 T_{osc}	μs	$T = \frac{1}{f_{osc}}$

Note 1 R_{osc} (pin 5) is 47kΩ - 200kΩ $\quad f_{osc} \simeq \frac{1}{0.15CR}$

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillater may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same operating area).

A counter is reset whenever a pulse is received and allowed to count at half the oscillator frequency. For example, taking an oscillator frequency of 1.56kHz:—

Resetting is blocked for the first 14ms and windows from 14ms to 22ms and from 22ms to 40ms determine whether a '1' or a '0' is present. Periods between pulses of 40ms to 80ms are recognised as word intervals. Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code. Channel step time period is derived from an external time constant.

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, -16V

1. Oscillator Time Constant An RC Time Constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to the pin; the signal must consist of a normal logic '0' level with pulses to logic '1', corresponding to the PPM pulse from the transmitter.

3. ON/SB Output Open drain output. Logic '0' denotes onset. Logic '1' standby set. Set to '0' when channel number changes, and by ON input at logic '0', set to '1' by standby input or by transmitter selected OFF.

4. Recall O/P Open drain output. A '0' may be used to trigger an on-screen display. A '0' is output during an input at pin 17, ON input. The pulse to logic '0' is generated by any channel change if circuit switches to ON from Standby, and by recall and normalise commands from the remote transmitter.

5. AFC O/P Open drain output. A logic '0' can inhibit tuner AFC. A static output is generated by manual ON control. A pulse is generated by any channel number change.

6. Standby Input A logic '0' will select standby state and normalise the analogue output to 3/8 maximum and select programme 1. An RC time constant may be connected to select standby at power ON.

7. Channel Step Time Constant An RC time constant defines the time period between increments of the channel number when stepping.

8. MUTE Output This will change state (toggle) on receptin of a Mute command or will remain at logic '1' if the D-A output is zero. The output is reset by any channel change command.

9. Analogue Reference A current drain attached to this input will define the current step of the D-A output. The current is equal to 8 output current steps.

10. Analogue Output The output of a current mirror D-A convertor provides a current source of between 0mA and 1.3mA. It is variable in 32 steps, UP or DOWN. It is normalised to 3/8 maximum value by the ON/SB input, and by normalise command from the transmitter.

11, 12, 13, 14. Channel Selection Outputs These outputs encode the 16 channels in binary code.

	A	B	C	D
Channel 1	0	0	0	0
Channel 16	1	1	1	1

Set to channel 1 on set switch ON.

15. V_{DD} - 14V to - 18V power supply

16. V_{SS} 0V (Ground)

17. ON I/P A logic '0' will switch the ON/SB output to ON (logic '0'). Channel 1 is selected and analogue output is normalised to 3/8 maximum. An RC time constant may be connected to select set ON at power on. The AFC defeat signal is generated and Mute is reset.

18. Step Input The channel code will step up by 1 as long as the pin is held at logic '0'. The time period between steps is defined by an RC constant on pin 10. When the channel code reaches 16 it will go to 1 next step. A step input will set ON/SB output to ON and normalise the analogue output. Mute is reset if analogue = 0.

Note:
1. An output is available to give sound mute during programme switching. With the inclusion of an extra switch on the transmitter and a transistor in the receiver, remote control of mute is possible.
2. To incorporate accurate fine tuning the addition of a single transistor provides AFC defeat as long as any local programme switch is kept depressed.

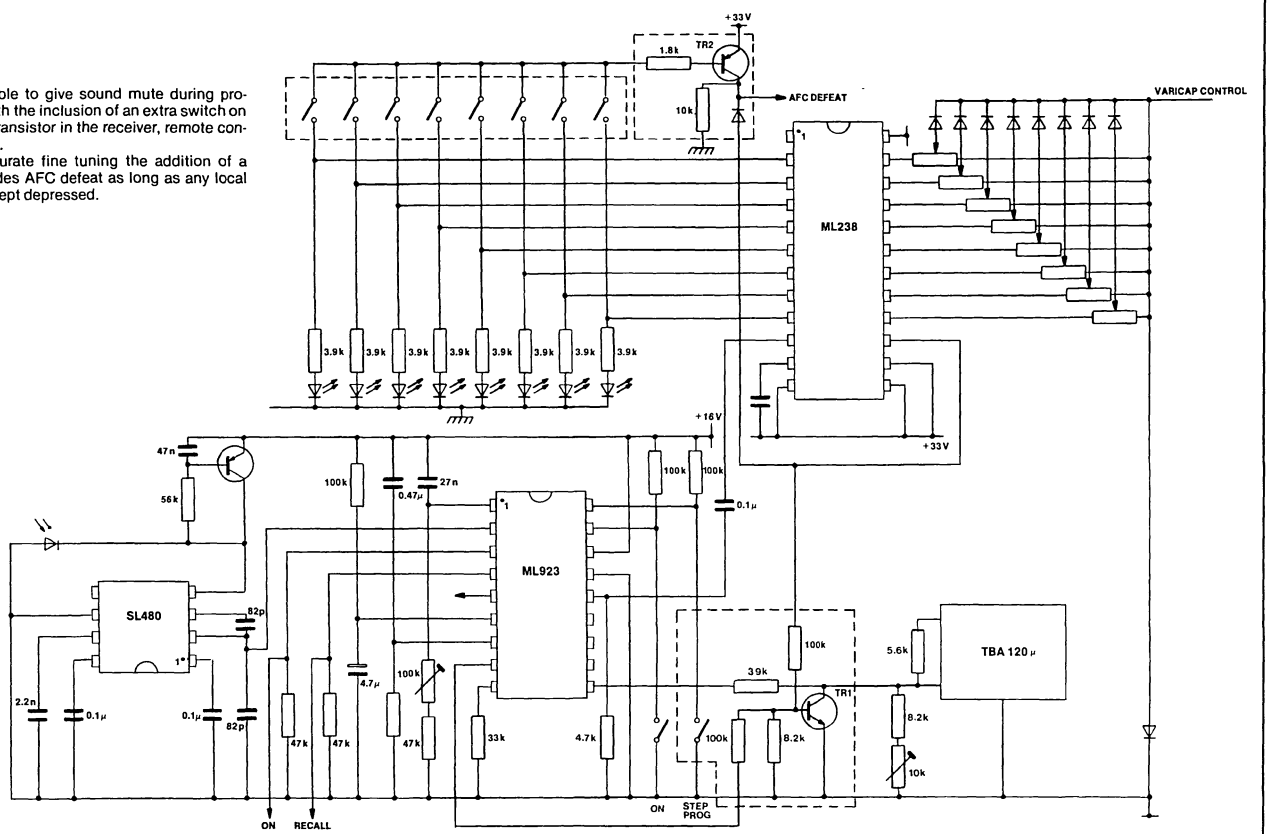


Fig.3 Receiver application

CODE					FUNCTION
E	D	C	B	A	
0	0	0	0	0	Channel 1
0	0	0	0	1	Channel 2
0	0	0	1	0	Channel 3
0	0	0	1	1	Channel 4
0	0	1	0	0	Channel 5
0	0	1	0	1	Channel 6
0	0	1	1	0	Channel 7
0	0	1	1	1	Channel 8
0	1	0	0	0	Channel 9
0	1	0	0	1	Channel 10
0	1	0	1	0	Channel 11
0	1	0	1	1	Channel 12
0	1	1	0	0	Channel 13
0	1	1	0	1	Channel 14
0	1	1	1	0	Channel 15
0	1	1	1	1	Channel 16
1	0	1	0	1	Channel Step +
1	0	1	0	0	Analogue +
1	1	0	1	0	Recall
1	1	0	0	1	Mute (Toggle)
1	1	0	1	1	Normalise
1	1	0	0	0	OFF
1	1	1	0	1	Channel Step-
1	1	1	0	0	Analogue-

Table 1 Command set

PLESSEY
Semiconductors

ML924

REMOTE CONTROL RECEIVER

The ML924 is an MOS/LSI integrated circuit for use as a receiver of remote control signals generated by the SL490 transmitter circuit, using PPM (Pulse Position Modulation) encoding technique. The receiver has 5 digital outputs whose response to PPM codes may be programmed by six control lines. It has a handshake interface which provides communication with microprocessors and computers.

FEATURES

- 5 Open drain outputs with enable
- Handshake or interrupt microprocessor and computer interface signals
- On-Chip oscillator
- 6 control lines to programme output response
- 3 selectable output modes

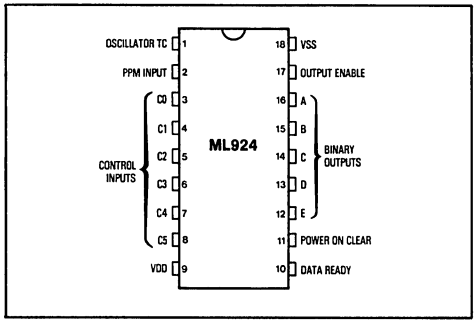


Fig.1 Pin connections (top view)

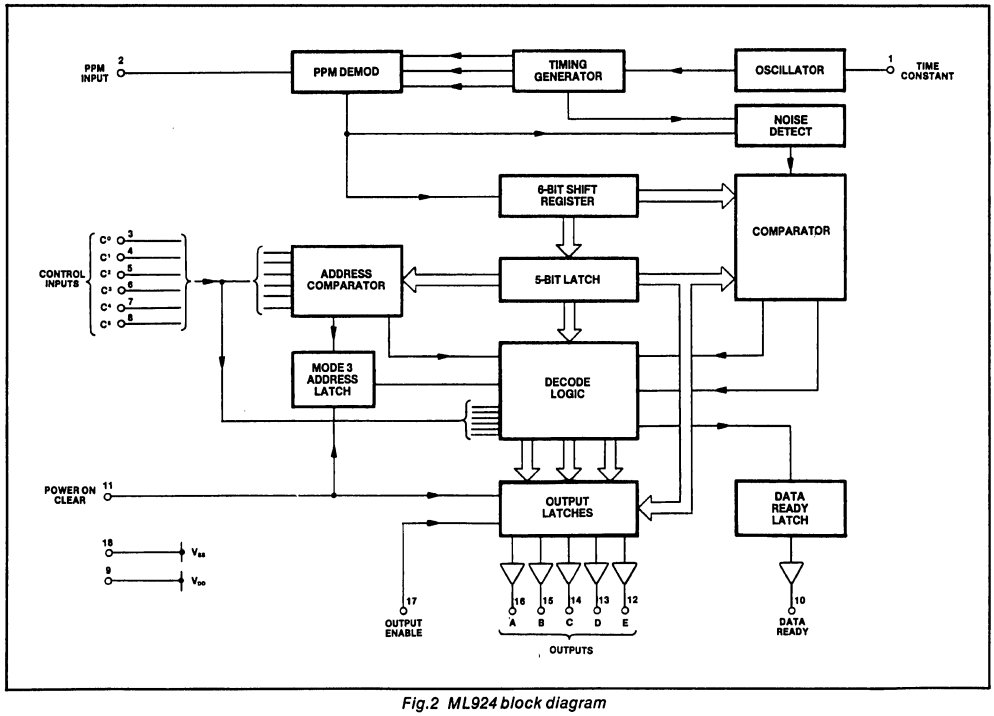


Fig.2 ML924 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
VSS = 0V; VDD = -16V; T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	9	12		18	V	
Supply current	9		6		mA	
Input logic level high ('1')	3-8, 17	-1		0	V	
Input logic level low ('0')		VDD		VDD + 3.5	V	
Output logic level high ('1')	10, 12-16	-1		0V		50k to VDD
Output logic level low ('0')		VDD		VDD + 0.5	V	
Oscillator frequency	1	15	3k	150k	Hz	Typical TC: C = 22nF, R = 100kΩ
PPM input logic level high ('1')	2	-1		0V		
PPM input logic level low ('0')		VDD		-6V		
PPM input pulse width	2	1		22Tosc	s	$T = \frac{1}{fosc}$
Power clear time constant	11	1	400		ms	

NOTE

Rosc (Pin 1) is 56kΩ to 150kΩ, $fosc \simeq \frac{1}{0.15\,CR}$

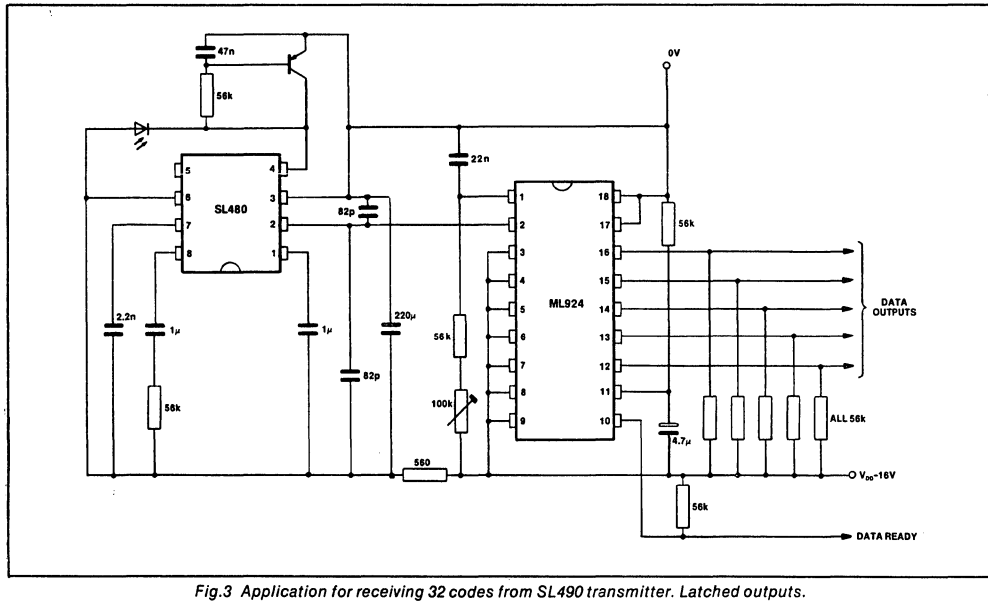


Fig.3 Application for receiving 32 codes from SL490 transmitter. Latched outputs.

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, 16V

1. Oscillator TC An RC time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to this pin; the signal must consist of a normal logic '0' level with pulses to logic '1'.

3-8. Control Word C_0 to C_5 Six control bits form the control word which programs the response of the five outputs (see Table 1).

9. V_{DD} -12V to -18V Power Supply.

10. Data Ready Open drain output. An output of logic '1' indicates the reception of a valid PPM word. It will remain at logic '1' for the duration of transmission.

11. Power Clear A capacitor and resistor connected to this pin define the time delay for the Power Clear Circuit.

12-16. Outputs E-A Open drain outputs which respond to the PPM input as defined in Table 1.

17. Output Enable A logic '1' will enable outputs A to E. A logic '0' will turn all outputs off.

18. V_{SS} 0V (Ground).

OPERATING NOTES

The receiver operates on a time scale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same area).

A counter is reset whenever a pulse is received and allowed to count at half the oscillator frequency. For example, at an oscillator frequency of 1.5kHz, resetting is blocked for the first 14ms and windows from 22ms to 40ms determine whether a '1' or a '0' is present. Periods between pulses of 40ms to 80ms are recognised as word intervals. Checks are made to ensure 6 pulses of 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

By means of the six control lines, the outputs can respond to the PPM input data in three ways:

1. 5 bit binary output with combinations of latched or momentary responses as shown in table 1.

2. 4 independant outputs with combinations of latched or momentary output as shown in table 1. Any output on 1 or 4 receivers can be addressed by each PPM word.

3. The PPM word can be an address or data depending on the logic state of bit **e**. If PPM bit **e** is '0', the remaining four bits (**a, b, c** and **d**) select one of 16 receivers. If bit **e** is '1', bits **a** to **d** control the outputs A to D. Outputs can be all latched or all momentary.

Control Word						Control Mode	Output Response					Interpretation of PPM Words									
C5	C4	C3	C2	C1	C0		E	D	C	B	A	e	d	c	b	a	e	d	c	b	a
0	0	0	0	0	0	1	LA	LA	LA	LA	LA	E	D	C	B	A					
0	0	0	0	0	1	1	LA	LA	LA	LA	M	PPM decoded on all outputs immediately									
0	0	0	0	1	1	1	LA	LA	LA	M	M										
0	0	0	1	1	1	1	LA	LA	M	M	M										
0	0	1	1	1	1	1	LA	M	M	M	M										
0	1	1	1	1	1	1	M	M	M	M	M										
0	0	1	0	Z	Z	2	—	S/R	S/R	S/R	S/R	0	Y	Y	Z	Z	1	Y	Y	Z	Z
0	1	0	0	Z	Z	2	—	S/R	S/R	S/R	M	Output address		Receiver address			Output address		Receiver address		
0	1	0	1	Z	Z	2	—	S/R	S/R	M	M	Resets an S/R type output					Sets an S/R type output or pulses a momentary output				
0	1	1	0	Z	Z	2	—	S/R	M	M	M										
1	0	Z	Z	Z	Z	3	—	LA	LA	LA	LA	0	Z	Z	Z	Z	1	D	C	B	A
1	1	Z	Z	Z	Z	3	—	M	M	M	M	Address mode		Receiver address			Data mode	PPM data sent to outputs of addressed receiver			

Table 1

NOTES:

1. Control Mode 1: Direct Response to the PPM Code
2. Control Mode 2: ZZ is a 2 bit address for the receiver
   YY selects one of 4 outputs

YY	OUTPUT
00	A
01	B
10	c
11	D

3. Control Mode 3: ZZZZ is a 4 bit address that selects, by which of 16PPM codes a receiver will be selected.
   If PPM bit **e** = '1', the rest of that PPM word will be read as data. If PPM bit **e** = '0' the rest of that PPM word will be read as an address.

ABSOLUTE MAXIMUM RATINGS

VDD supply and all inputs wrt VSS	+0.3V to -25V
Storage temperatures	-55°C to +125°C
Operating temperature ambient	-10°C to +65°C

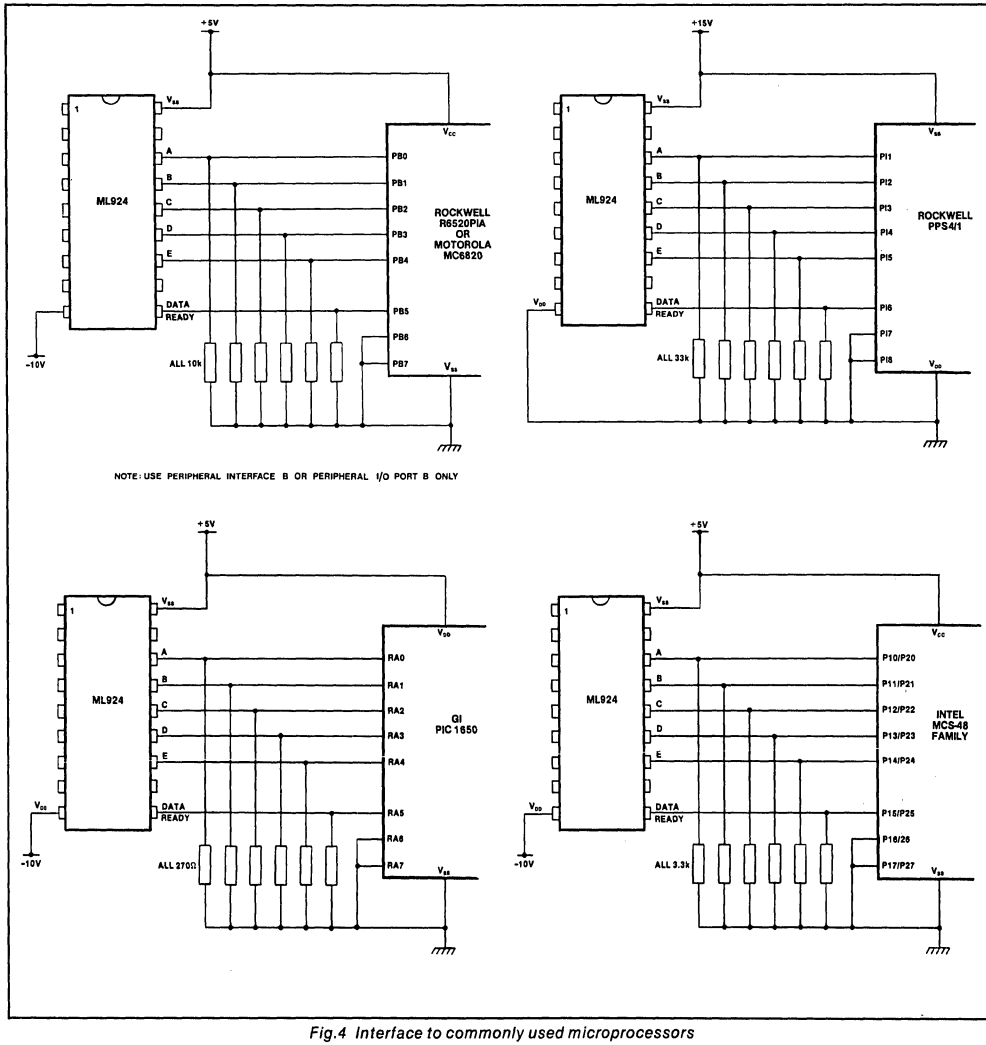


Fig.4 Interface to commonly used microprocessors

PLESSEY
Semiconductors

ML925

REMOTE CONTROL RECEIVER FOR TOYS

The ML925 is an MOS/LSI integrated circuit for use as a decoder of PPM remote control commands transmitted by the SL490 or SL491 circuit. It is designed to control either a toy vehicle with two-speed drive motor and a three position latching steering system, or a vehicle with momentary action steering and a third motor, typically a winch. This second vehicle type also has four selectable speeds. Both types have horn, headlights, hazard flasher and turn indicator facilities.

The circuit can operate on the first set of 16 SL490 commands or the second set of 16, thus giving simultaneous control of two independent vehicles with the same integrated circuit type in both.

FEATURES

- Multifunction Toy Control
- High Power, Free Drain Buffers on all Outputs
- Uses Well-Proven High Security PPM Coding with Double Word Checking
- Minimum Component Interfaces Required to Motors and Lamps
- Direct Connection to SL480 Infra-red Preamplifier

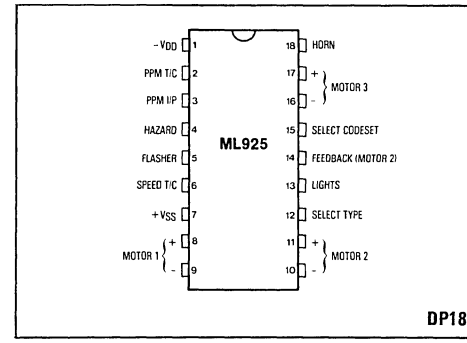


Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply inputs with respect to V_{SS}	+0.3V to -25V
Storage temperature	-55°C to +125°C
Operating ambient temperature	-10°C to +65°C

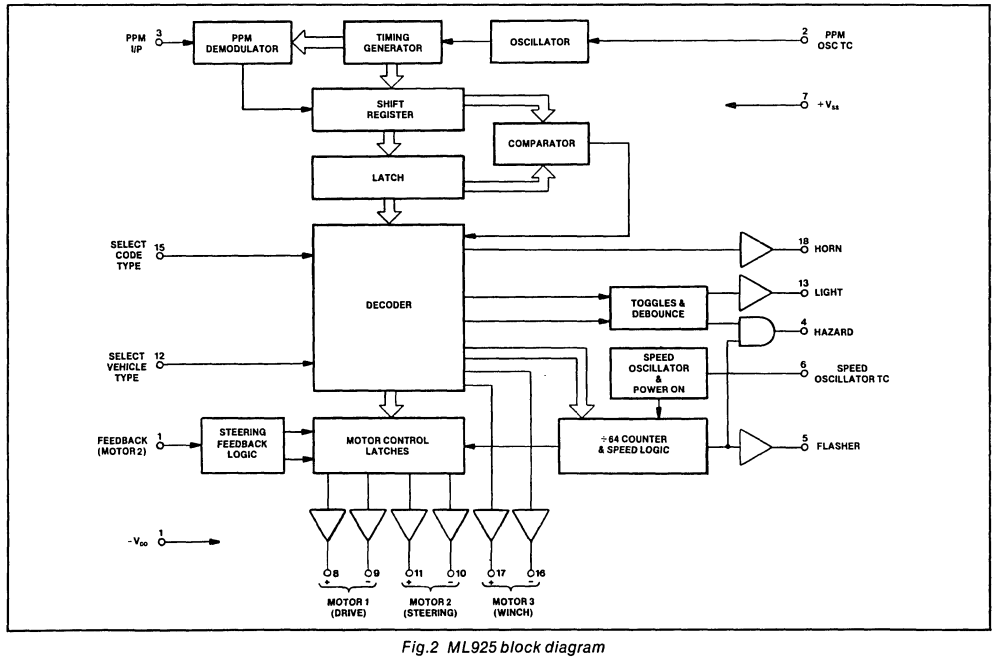


Fig.2 ML925 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{SS} = 0V$, $V_{DD} = -15V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{DD}	1	-12	-15	-18	V	
Supply current	1		8	12	mA	
PPM input high	3	-1		0	V	
low	3	V_{DD}		-6	V	
Code or type select high	12, 15	-1		0	V	
low	12, 15	V_{DD}		-10	V	
Steering feedback, speed time	6, 14	-2.5	-3	-3.5	V	
Constant threshold						
Output voltage motor drives	8-11 16, 17		-0.2	-0.5	V	Output current = 10mA
other drives	4, 5 13, 18		-0.2	-0.5	V	Output current = 5mA
Output leakage all outputs				1	μA	Output voltage = -15V
PPM oscillator frequency	2	15		150k	Hz	
			4		kHz	C = 33nF, R = 50kΩ
Speed control oscillator	6		50		Hz	R_{pos} = 120k, R_{neg} = 270kΩ, C = 100nF
Flasher rate	5		0.8		Hz	For pin 6 as above
PPM input pulse width	3	1		22T	μs	T = 1/f at pin 2

TRANSMITTER CODES					VEHICLE TYPE	
E	D	C	B	A	TYPE A, 'CAR'	TYPE B, 'TRUCK'
X	0	0	0	0	STOP	STOP
X	0	0	0	1	FORWARD STRAIGHT	FORWARD
X	0	0	1	0	REVERSE STRAIGHT	REVERSE
X	0	0	1	1	HORN (MOMENTARY)	HORN (MOMENTARY)
X	0	1	0	0	NOT USED	NOT USED
X	0	1	0	1	FORWARD LEFT	STEER LEFT (MOMENTARY)
X	0	1	1	0	REVERSE LEFT	'WINCH IN' (MOMENTARY)
X	0	1	1	1	FLASHER ON/OFF	FLASHER ON/OFF
X	1	0	0	0	NOT USED	NOT USED
X	1	0	0	1	FORWARD RIGHT	STEER RIGHT (MOMENTARY)
X	1	0	1	0	REVERSE RIGHT	'WINCH OUT' (MOMENTARY)
X	1	0	1	1	LIGHT ON/OFF	LIGHTS ON/OFF
X	1	1	0	0	SPEED 1	SPEED 1
X	1	1	0	1	SPEED 1	SPEED 2
X	1	1	1	0	SPEED 2	SPEED 3
X	1	1	1	1	SPEED 2	SPEED 4

Table1 Decoder response to PPM codes

CIRCUIT DESCRIPTION

The decoder operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to a wide range of frequencies to allow different decoders to respond to different PPM rates. PPM words consist of six narrow pulses separated by 5 gaps, a short gap for a '1' and a long gap for a '0', in the ratio 2 to 3. Words are separated by a gap of ratio 6. Two complete correct adjacent words are required before the decoder will respond.

A second on-chip oscillator provides a frequency which sets the mark/space ratio of the motor speed control and hazard and indicator flasher rate. A power-on reset is also provided during initial power-up.

Simultaneous control of two independent vehicles is possible. For one vehicle the first bit of the 5-bit transmitted code is a '0' and for the second vehicle the first bit is a '1' as shown in Table 1.

OPERATING NOTES

1. In Table 1, X determines one of two vehicles to be controlled by independent controllers within the same area. The same decoder design can drive either vehicle. X = 0 for vehicle 1, X = 1 for vehicle 2.
2. Momentary controls only give an output for the duration of a PPM command stream, i.e. for as long as a transmitter button is depressed.
3. Hazard and lights control codes provide a toggle action; push once for on, push again for off. There is an internal time-out within the decoder to cater for interruptions in the PPM stream by noise.
4. Vehicle type A will drive at half or full speed and has a latching drive. The steering has three positions: hard left, centre and hard right and is driven momentarily during code transmission. The centre position may be indicated by a contact running on a conductive track attached to the steering bar (see fig.4). The track should have a non-

conducting section at the centre and the two halves should be taken to V_{SS} and V_{DD} respectively. The contact, which should be fixed to the body of the vehicle, is attached to a pin on the decoder and a two resistor bias network. The contact must not conduct with either area when in the centre position.

5. Vehicle type B also has a latched drive direction , which remains latched until STOP is pressed; but its steering is momentary, so that it will progress left (say) until the command is removed, and stay in that position until a further steering command is received. This provides a time-proportional steering system.

6. Vehicle type B has four possible drive speeds; quarter, half, three-quarters and full speed. From STOP or power-on the speed selected is quarter, or speed 1. Further speeds are selected by the four latched speed select commands. The steering speed or rate of progression is proportional to the drive speed.

7. Vehicle type B has provision for single speed driving of a third motor (forward or reverse). Control of this motor is momentary, stopping when commands cease to be transmitted.

8. One output of the decoder provides a continuous flashing signal. This can be gated with various other outputs of the decoder (using simple transistor gates) to give automatic flashing lights or buzzers when functions are operating. Examples are: left and right turn indicators, buzzer when reversing, warning lamp when winch in operation or siren switched on and off by 'lights' command.

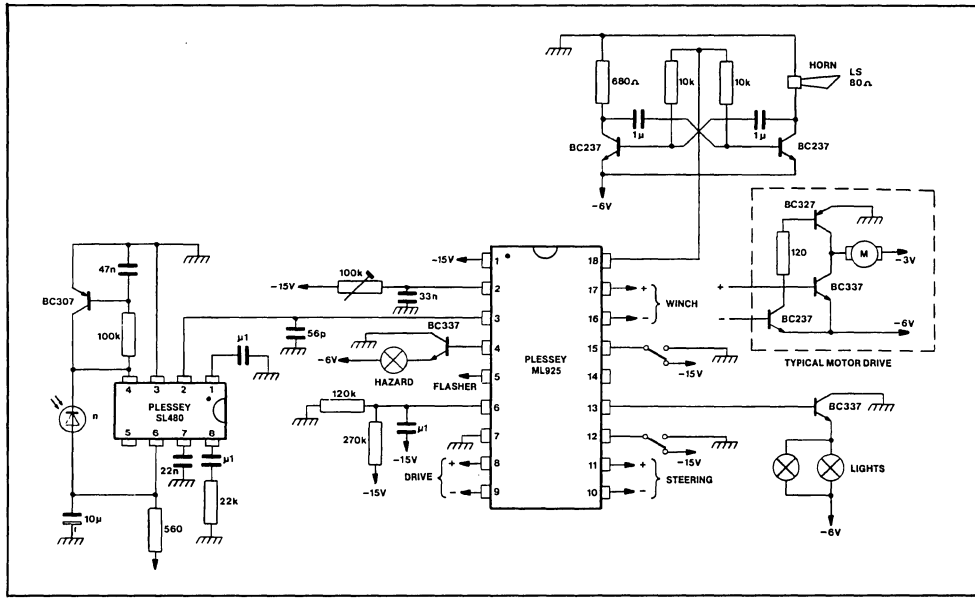


Fig.3 Infra-red control for car or truck

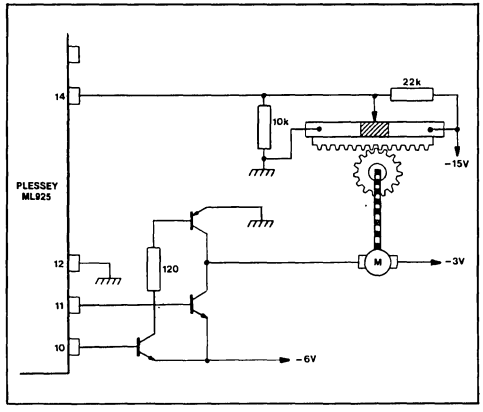


Fig.4 Infra-red control for vehicle with 3-position steering

PIN FUNCTIONS

1. **V_{DD}**
   -12V to -18V power supply.

2. **Oscillator time constant**
   An RC time constant of a capacitor to V_{SS} and a resistor to V_{DD} defines the internal clock frequency for demodulating PPM.

3. **PPM input**
   The output of the 'front end' amplifier is connected here; the signal must be a normally low level of -6V, and have PPM pulses going positive to -1V.

4. **Hazard**
   An open drain output to drive a flashing lamp or buzzer at a rate determined by pin 6 time constant. Toggled on or off by a single PPM code.

5. **Indicator signals**
   A permanently pulsing output at a rate determined by pin 6 time constant. Open drain drive.

6. **Speed time constant and power-on reset**
   A capacitor and resistor to V_{DD} and a resistor to V_{SS} define the frequency of the motor speed control pulses and the warning and indicator pulses.

7. V_{SS}
0V power supply.

8. Forward
Open drain high power latched drive to the drive motor circuit. When on, the drive motor should move the vehicle forward.

9. Reverse
Open drain high power latched drive to the drive motor circuit. When on, the drive motor should move the vehicle in reverse.

10. Steer left
Open drain high power drive to the steering motor circuit. When on, the steering should move on the left.

11. Steer right
Open drain high power drive to the steering motor circuit. When on, the steering should move to the right.

12. Vehicle type
An input to determine the type of vehicle and the interpretation of control codes. V_{SS} selects Type A (car) V_{DD} selects type B (truck).

13. Lights
Open drain output to drive headlights etc. Toggled on or off by a single PPM code.

14. Steering
An input from the centre contact of the steering feedback system for vehicle type A. A resistor to V_{SS} and a resistor to V_{DD} are required as a bias chain.

15. Code set
An input to determine which set of 16 PPM codes the decoder responds to. V_{DD} will select the first 16 (E = 0) and V_{SS} will select the last 16 (E = 1).

16. Third motor +
Open drain high power drive to a third motor circuit for vehicle type B.

17. Third motor–
Open drain high power drive to a third motor circuit for vehicle type B. Drives motor in opposite direction to pin 16.

18. Horn
Open drain output to drive a horn or buzzer. A momentary output selected by one PPM code.

Operation of the various functions is described more fully in 'operation' and in Table 1.

PLESSEY
Semiconductors

ML926/7

REMOTE CONTROL RECEIVERS
(With Momentary Outputs)

The ML926 and ML927 are MOS LSI monolithic circuits for use as receivers of remote control signals for television control and many other applications. They are general purpose devices each receiving sixteen of the thirty-two codes transmitted by the SL490 circuit as pulse position modulation (PPM).

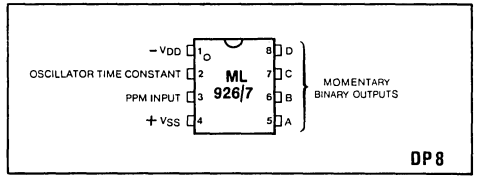


Fig. 1 Pin connections

FEATURES

- Minimum Package Size – 8-Lead Minidip
- Four Outputs Indicate in Binary the Code Currently Being Received, and Are Switched Off (Low) When No Valid Code is Detected.
- On-Chip Oscillator
- High Power, Free Drain, Output Buffers

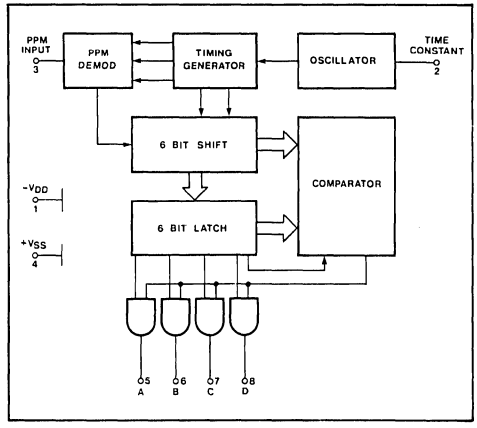


Fig 2 Block diagram

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same area).

A counter is reset whenever a pulse is received, and allowed to count at half the oscillator frequency. For example, take an oscillator frequency of 1.5kHz:—

Resetting is blocked for the first 14 ms and windows from 14ms to 22ms and from 22ms to 40ms determine whether a '1' or a '0' is present. Periods between pulses of 40ms to 80ms are recognised as word intervals. Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

The ML926 responds only to codes 00001 to 01111 from the SL490 transmitter whereas the ML927 responds to codes 10001 to 11111.

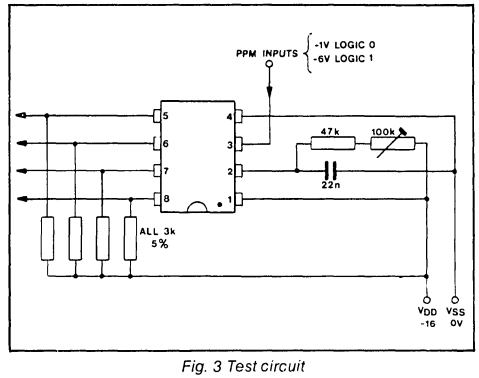


Fig. 3 Test circuit

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to -25V
Storage temperature	−55°C to +125°C
Operating temperature ambient	-10°C to +65°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
$V_{DD} = -16V$
$T_{amb} = 25°C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		12	14	18	V	
Current consumption	1	2	3	4	mA	
PPM input						
Input logic level high	3	−1		O	V	
Input logic level low	3	V_{DD}		−6	V	
Input pulse width	3	1		$22T_{OSC}$	μsec	$T = \frac{1}{f_{osc}}$
Oscillator time constant See Note 1						
Oscillator frequency	2	15		150k	Hz	
			3k		Hz	Typical TC: 22nF to Vss 100k to V_{DD}
Variation wrt V_{DD}			1		%/V	
Output voltage high	5-8	-1.5		0	V	R_L = 3.0K to VDD
Output device leakage (Output OFF)	5-8			1	μA	

Note 1. R_{osc} (Pin 2) is 47kΩ → 200kΩ, $f_{OSC} \simeq \frac{1}{0.15CR}$

PIN FUNCTIONS

1. V_{DD}
−14V to −18V power supply

2. Oscillator time constant
An RC time constant of a capacitor and resistor at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal logic 'low' level with pulses to logic 'high' corresponding to the PPM pulses from the transmitter.

4. V_{SS}
0V (ground)

5-8. A,B,C,D
Four open drain high power transistors give a binary coded output of the valid code being received.

	Momentary binary outputs	
Transmitter Code	ML926	ML927
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 0 1	0 0 0 1	↓ ↓ ↓ ↓
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0	0 0 0 0	0 0 0 0
1 0 0 0 1	↓ ↓ ↓ ↓	0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0		0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

Table 1 Response to SL490 codes

PLESSEY
Semiconductors

ML928/9

REMOTE CONTROL RECEIVERS
(WITH LATCHED OUTPUTS)

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra-red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML928 and ML929 are general purpose remote control receivers, each receiving and latching 16 of the 32 codes transmitted by the SL490 circuit in the PPM (Pulse Position Modulation) mode. The ML928 responds to codes 00000 to 01111 only, and the ML929 to codes 10000 to 11111. Both devices are packaged in 8-lead minidip to minimise board area. The on-chip oscillator may be adjusted from 15Hz to 150kHz, allowing different transmission rates. They have a high degree of immunity to incorrect codes; there must be two consecutive correct codes received before the outputs can change.

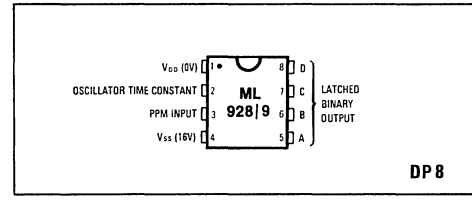


Fig. 1 Pin connections

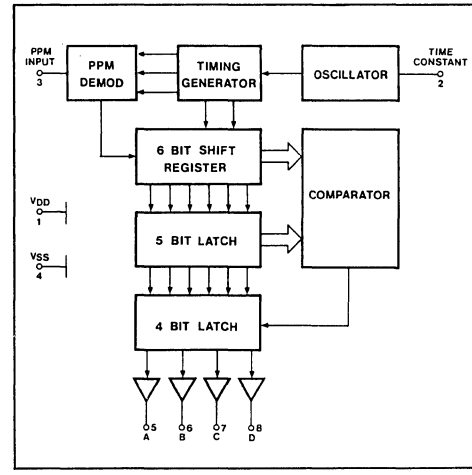


Fig. 2 ML928, ML929 remote control receivers block diagram

FEATURES

- Accepts 5 Bit PPM
- On-Chip Oscillator, 15Hz to 150kHz Range
- Easily Used With Ultrasonic, Infra-Red or Other Transmission Media
- Four High Drive Outputs
- 16 Latched States
- Minimum Sized Package

QUICK REFERENCE DATA

- Power Supply: 12V to 18V. Typical 4mA at 16V.
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 Bit with successive codeword comparison
- Outputs: Maximum 15mA sourced from open drain drive
- Logic convention: Logic 0 – output transistor ON, pulls output to V_{SS}
  Logic 1 – output transistor OFF

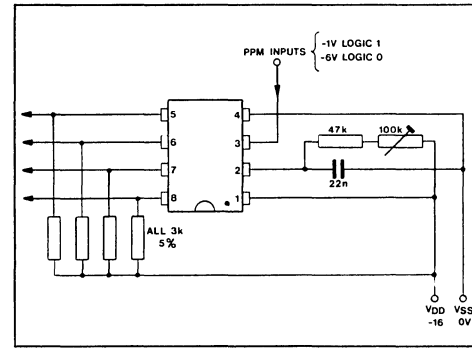


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{SS} = 0V
V_{DD} = −16V
T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Current Consumption V_{DD}	1	3	4	5	mA	
Supply voltage	1	−12		−18	V	
PPM input	3					
Logic '0' level		−1		0	V	
Logic '1' level		V_{DD}		−6	V	
Input pulse width		1		$22T_{osc}$	μs	$T_{osc} = \frac{1}{f_{osc}}$
Oscillator Timing	2					
Frequency		15		150k	Hz	
			4k		Hz	Typical TC: 22nF to Vss, 100kΩ to V_{DD}
Variation w.r.t. V_{DD}			1		%/V	
Latched binary output	5, 6, 7, 8	-1.5		0V	V	RL = 3.0k to VDD
Logic '0' output voltage						
Output leakage in logic '1' state				1	μA	

Note 1. $R_{osc.}$ (pin 2) is 25k → 200 kΩ. $f_{osc.} \simeq \frac{1}{0.15CR}$

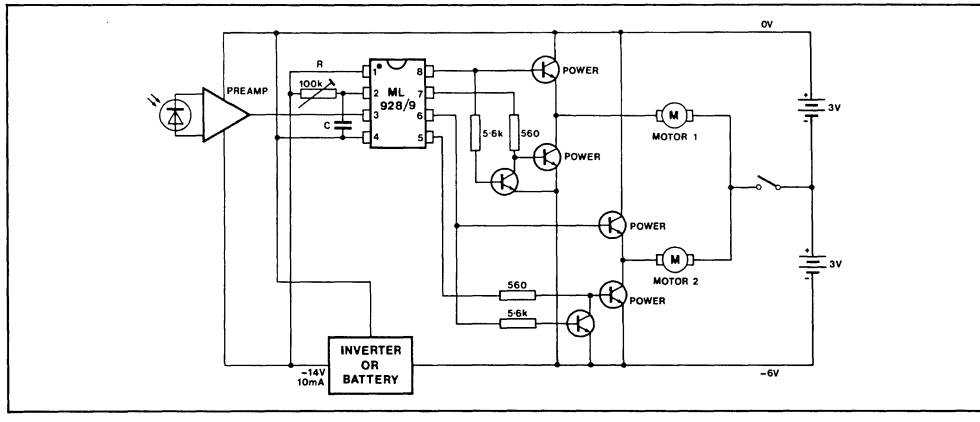


Fig. 4 Forward and reverse drive of two small DC motors

PIN FUNCTIONS

Negative logic: '0' is 0V (V_{SS}), '1' is − 12V to −18V (V_{DD})

1. V_{DD}
−12V to −18V power supply

2. Oscillator time constant
An R-C time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz at 150Hz and should be set so that there are 40 periods in one 't_o' transmitter pulse interval.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal logic '1' level with pulses to logic '0' corresponding to the PPM pulses from the transmitter.

4. V_{SS}
0V (ground)

5-8. A,B,C,D
Four open-drain high power transistors give a binary coded latched output of the last valid code received.

Transmitter Code	Latched binary outputs	
	ML928	ML929
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	
0 0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	No change
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0		0 0 0 0
1 0 0 0 1		0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0	No change	0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

Table 1 Response to SL490 codes

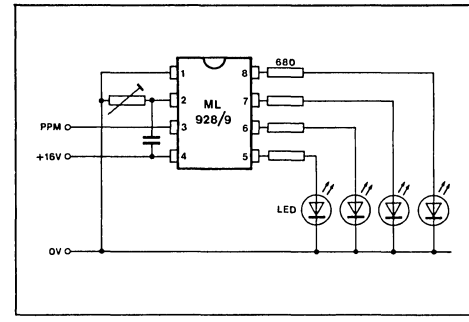


Fig. 5 Direct drive of LEDs

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to −25V
Storage temperature	−55°C to +125°C
Operating temperature ambient	−10°C to +65°C

PLESSEY
Semiconductors

SL470

BCD TO 1 OF 10 DECODER/VARICAP DRIVER

FEATURES

- Up To 10 Programmes
- Direct Varicap Voltage Selection
- TTL Level Compatible Inputs
- May be Directly Driven by ML920 Series Receivers
- Low Component Count
- Low Cost
- Can Be Used To Drive Indicators

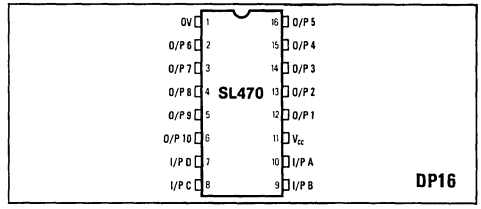


Fig. 1 Pin connections

QUICK REFERENCE DATA

- Power supply 33V 3mA
- 1 out of 10 outputs selected high
- Output drive 2mA
- Input 4 Bit BCD, TTL compatible

D(2^3)	C(2^2)	B(2^1)	A(2^0)	O/P (high)
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10

Table 1 Decode table

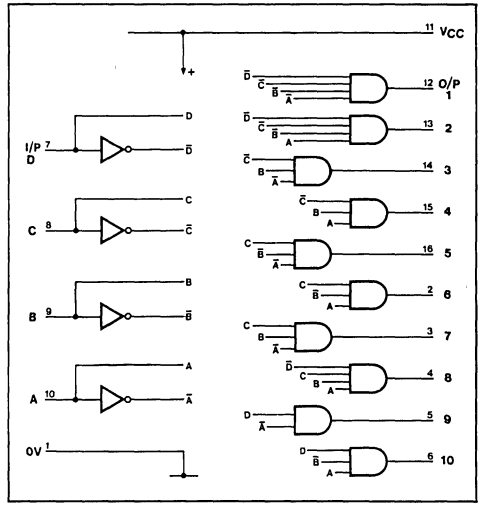


Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C
Vcc = 33V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage	11	30	36		V	
Supply current	11		3	6	mA	O/Ps unloaded
Selected output level	2–6, 12–16		Vcc - 1.5	Vcc–3.5	V	I_{OUT} = 2mA
Unselected output levels	2–6, 12–16	0.5			V	100k load to 0V
Input high state	7–10	1.7		5	V	
Input low state	7–10	–0.3		+0.4	V	
Input current	7–10			1.5	mA	V_{in} = 1.7V

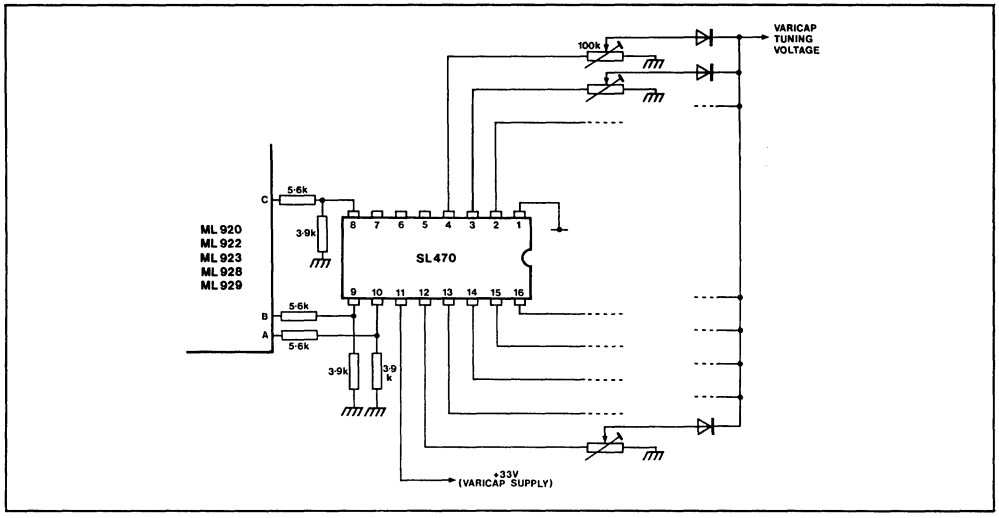


Fig.3 Typical application circuit for 8 programmes

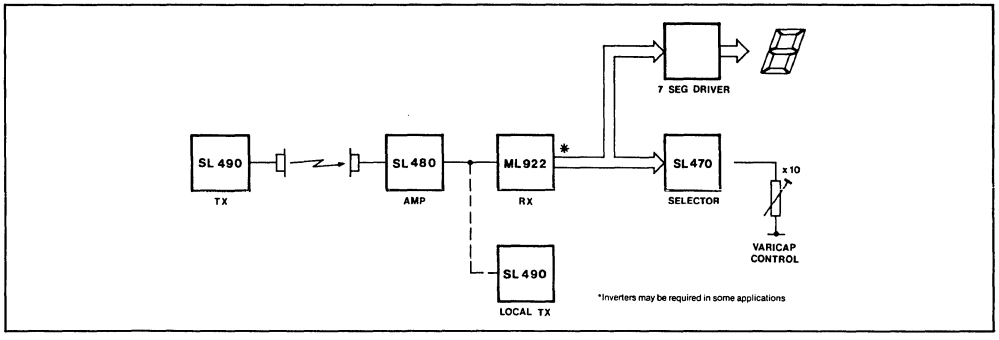


Fig. 4 Complete remote control system

ABSOLUTE MAXIMUM RATINGS

Storage temperature	—55°C to +125°C
Operating temperature	—10°C to +65°C
Supply voltage	36V

PLESSEY
Semiconductors

SL480

INFRA-RED PULSE PRE-AMPLIFIER

The SL480 is a bipolar integrated circuit containing three amplifier stages. Its output is directly compatible with the ML920 range of remote control receiver circuits. It is packaged in an 8-lead plastic package. The gain of the amplifier stages may be adjusted to suit the application. The input impedance is approximately 20MΩ.

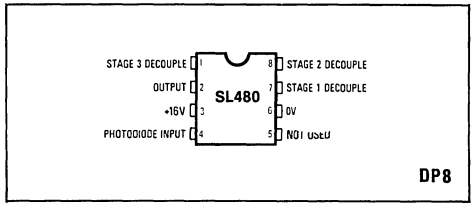


Fig. 1 Pin connections

FEATURES

- Minimum Component Solution to Infra-Red Detection
- Adjustable Gain
- Directly Compatible With Plessey ML920 Range of Receivers
- May Be Used As A General Purpose 100kHz Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply, Vcc	20V
Maximum power dissipation	480mW
Operating temperature range	–10°C to +65°C
Storage temperature range	–55°C to +125°C

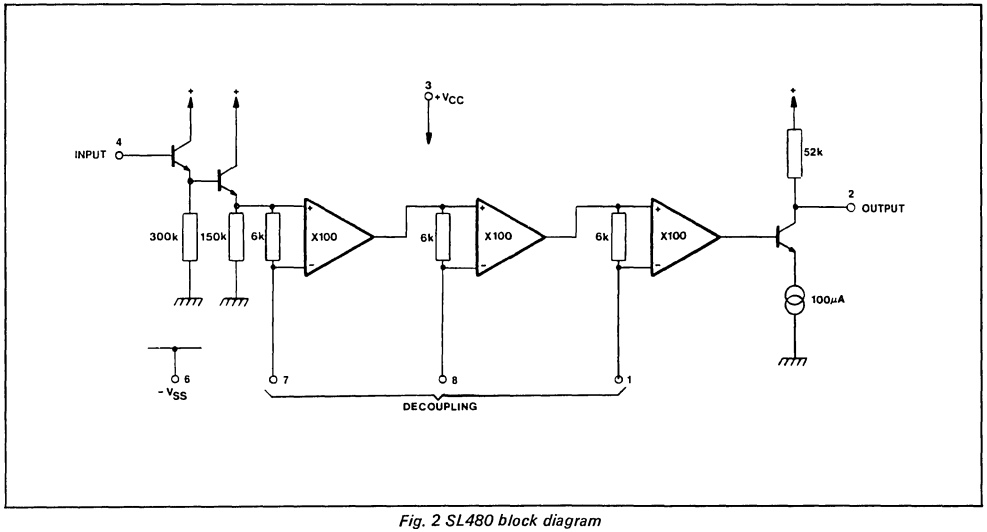


Fig. 2 SL480 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$
$V_{cc} = +15V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	3	12		18	V	
Supply current	3		1.5	4	mA	
Open loop gain	4, 2		100		dB	Sum of 3 stage gains
Input impedance	4		20		MΩ	
Output current sink	2		100		μA	
Internal pullup resistor	2		50		kΩ	
Quiescent O/P voltage (low)	2	9	11		V	At reduced gain
Pulse output (high)	2	15.5			V	No load

OPERATING NOTES

An external resistor of, typically, 330kΩ between pins 4 and 3 provides current for the photo detector diode connected across pins 4 and 6. Any voltage generated across the diode by incident light is amplified.

The gain of each stage may be readily adjusted by external resistors in series with decoupling capacitors between pins 7, 8 or 1 and ground. For maximum gain the resistors are dispensed with except at pin 8.

Typical decoupling capacitors are 22nF. The output goes high towards Vcc when light is detected. This is compatible with the PPM input of the ML920 series of remote control receivers. The SL480 is compatible with the full power supply range of the ML920 series and can also be used at a lower supply voltage as long as Vcc is common to Vss of the MOS device, i.e. common positive.

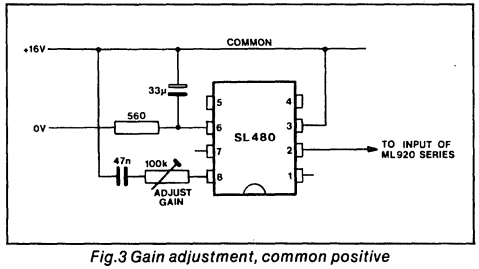


Fig.3 Gain adjustment, common positive

The circuit diagram of the SL480 infra-red pulse amplifier is shown in Fig.5. Pulses generated by an infra-red receiver diode are amplified to a suitable level for direct connection to the input of any of the Plessey Semiconductors ML900 series of remote control receiver circuits.

For basic operation, the receiving diode and SL480 input is biased with a single resistor to the positive supply. Any infra-red light reaching the diode generates a leakage current which causes a voltage drop across the bias resistor.

The SL480 input stage consists of a compound emitter follower (TR1 and TR2) which provides a high input impedance and allows a relatively high diode load resistor as well as a voltage drop of around 1.3V between the input and the bases of the first amplifier stage (TR6, TR7).

Transistors TR6 and TR7 form a differential amplifier which is designed to prevent low frequency or DC input signals from reaching subsequent stages of the amplifier. Since the bases of transistors TR6 and TR7 are internally connected by the 6.3k resistor R3, low frequency signals are applied to both sides simultaneously causing no change in collector current and therefore no output to the second stage. Higher frequency signals are amplified because TR7 base is decoupled externally on pin 7.

Stage 2 gain is provided by a similar differential amplifier to stage 1 except that the relatively stable DC input voltage provided by stage 1 output allows the use of a tail resistor R11 rather than a current source. Decoupling of AC signals is provided at pin 8.

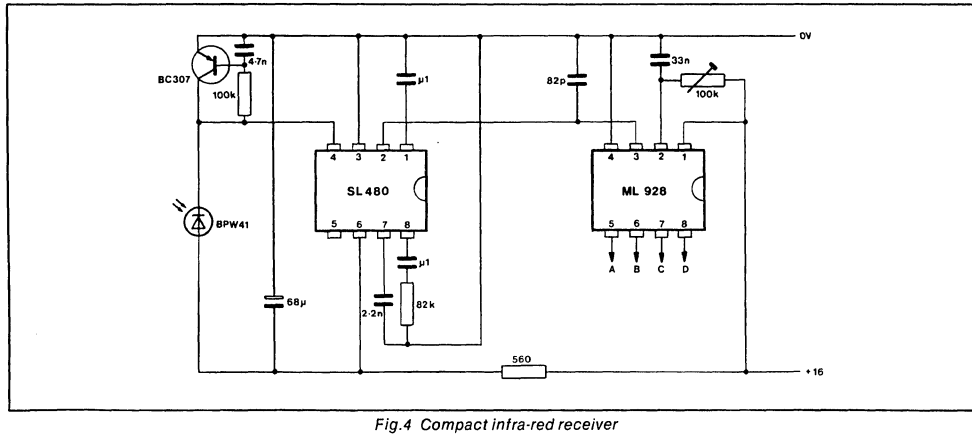


Fig.4 Compact infra-red receiver

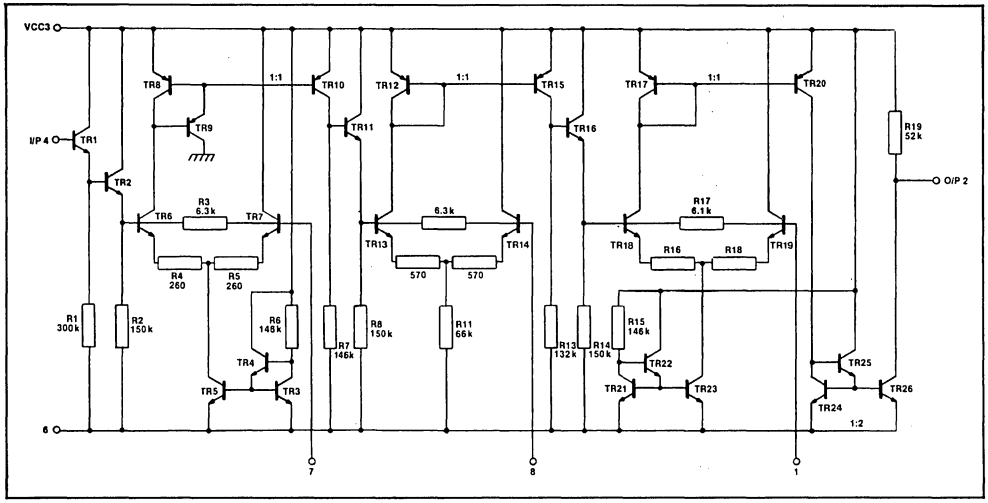


Fig.5 SL480 circuit diagram

Stage 3 is similar to stage 1, but with an extra current mirror (TR24 to TR26) to provide signal inversion at the output.

The standing current through the output load resistor and thus the output voltage, is set by the current in R15. This current will amount to about 100μA, and give an output voltage about 5V below the positive rail with a 15V supply.

It should be noted that there is a parasitic zener diode of about 6V in parallel with the output load resistor R19; this diode will be destroyed if the output is shorted to the negative supply rail. Stage 3 decoupling is provided at pin 1.

With a 15V supply, the input stage will operate with input voltages ranging from 15V down to 5V. This will allow the device to function satisfactorily in high ambient light conditions which produce high leakage currents in the receiving diode. A single transistor circuit is shown in Fig.6, which prevents the input voltage to the SL480 changing for diode leakage currents up to several milliamps. By careful choice of R and C values, this circuit can be made to give extra rejection of low frequency modulation such as that produced by incandescent lamps.

Under conditions of very high ambient light the circuit may show signs of instability. This can be prevented by connecting a 2.2k resistor in series with the transistor emitter.

If required, the gain of each stage of the SL480 can be set individually by connecting a resistor in series with the decoupling capacitor. A 6k resistor will reduce the stage gain to half its full value of about 40dB. Normally it is only necessary to reduce the gain of the second stage with about 33-56k.

If preferred the decoupling components on pins 1, 7 and 8 can be earthed to the negative supply on pin 6.

As with any high gain device, care is needed in the layout of printed circuit boards to prevent instability. All decoupling and input components should be mounted close to the SL480. A suitable printed circuit layout for the SL480 is shown below.

Decoupling of the power supplies local to the SL480 is advisable. A resistor of about 560ohms in series with the negative rail and a parallel capacitor of 68microfarads being adequate (see Fig.6).

The decoupling resistor should always be in the negative supply as the ML920 series remote control circuits have a threshold close to the positive rail, and any voltage drop here would reduce the noise immunity.

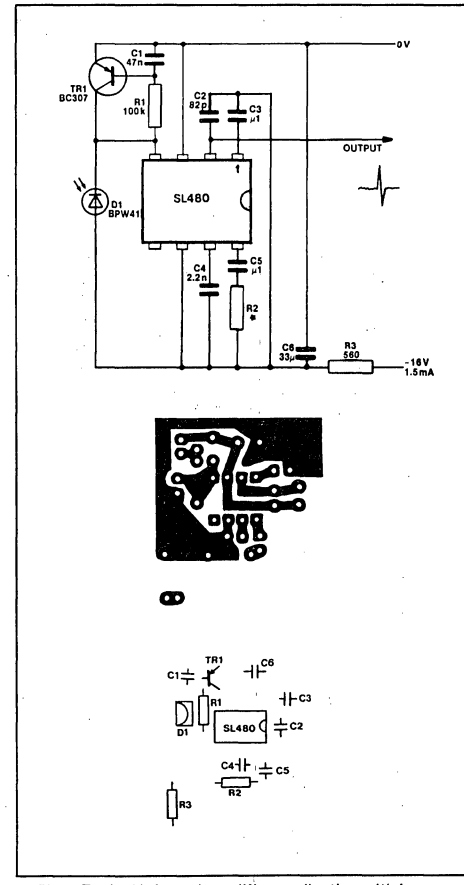


Fig.6 Typical infra-red amplifier application with improved detector biasing

PLESSEY
Semiconductors

SL490

REMOTE CONTROL TRANSMITTER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL490 is an easily extendable, 32 command, pulse position modulation transmitter drawing negligible standby current. It may be used with the ML920 series of remote control receivers.

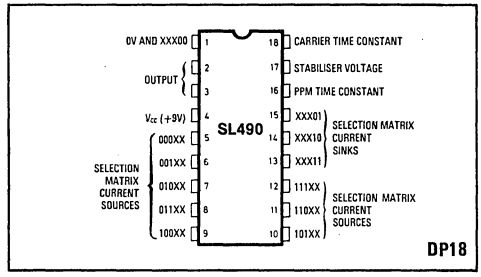


Fig. 1 Pin connections

FEATURES

- Ultrasonic or Infra-red Transmission
- Direct Drive for Ultransonic Transducer
- Direct Drive of Visible LED When Using Infra-red
- Very Low Power Requirements
- Pulse Position Modulation Gives Excellent Immunity From Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance Up To 1kΩ Tolerated
- Few External Components
- Anti-Bounce Circuitry On Chip

QUICK REFERENCE DATA

- Power Supply: 9V, Standby 6μA, Operating 8mA
- Modulation: Pulse Position With or Without Carrier
- Coding: 5 Bit Word Giving a Primary Command Set of 32 Commands
- Key Entry: 8 × 4 Single Pole Key Matrix
- Date Rate: Selectable 1 Bit/Sec to 10k Bit/Sec.
- Carrier Frequency: Selectable 0Hz (no carrier) to 200KHz.

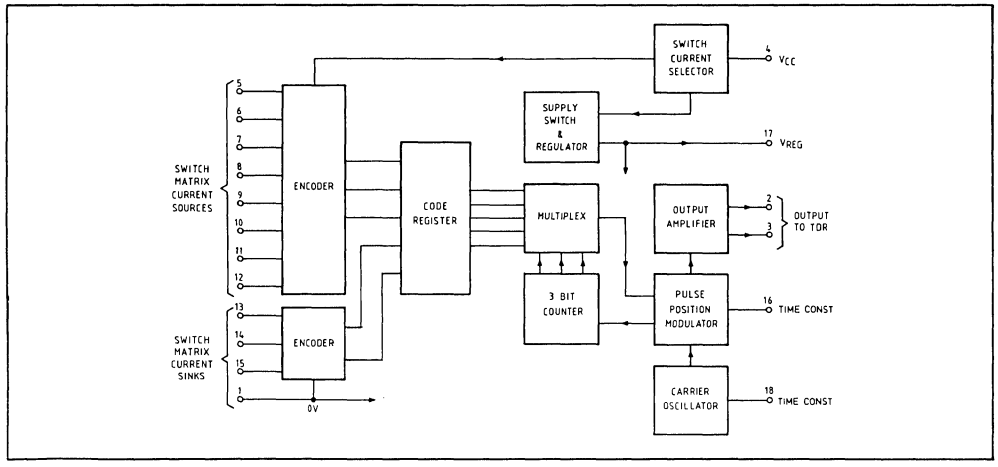


Fig. 2 SL490 transmitter block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test conditions (unless otherwise stated):
T_{amb} = 25°C fc = 40kHz
Vcc = +7V to + 9.5V t_1 = 18ms

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		8	16	mA	Vcc = 9.5V
Standby supply current	4			30	µA	
Stablised voltage	17	4.3	4.6	4.9	V	
Output current available	17			1	mA	
Output voltage swing	2, 3	1		Vcc	V	Unloaded
Output current	2, 3			5	mA	Peak value
External switch resistance				1	kΩ	
External switch closure time		6			ms	
External carrier oscillator resistor required, R2	18	20	40	80	kΩ	C2 = 680pF
External PPM resistor R_1 required	16	15	30	60	kΩ	C1 = 0.68µF
Ratio t_o/t_1	2, 3	1.4	1.5	1.6		
Pulse width, t_p	2, 3	2	3	4	ms	
Inter word gap, t_g	2, 3	50	54	58	ms	
Variation of t_o with V_{CC} t_o with V_{CC} = 9.5V t_o with V_{CC} = 7.5V	2,3	0.96		1.04		
Pulse width T_p	2,3	2	3	4	ms	
Inter word gap t_g	2,3	50	54	58	ms	

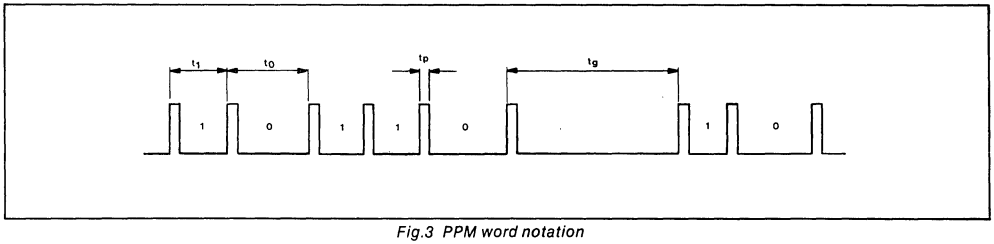


Fig.3 PPM word notation

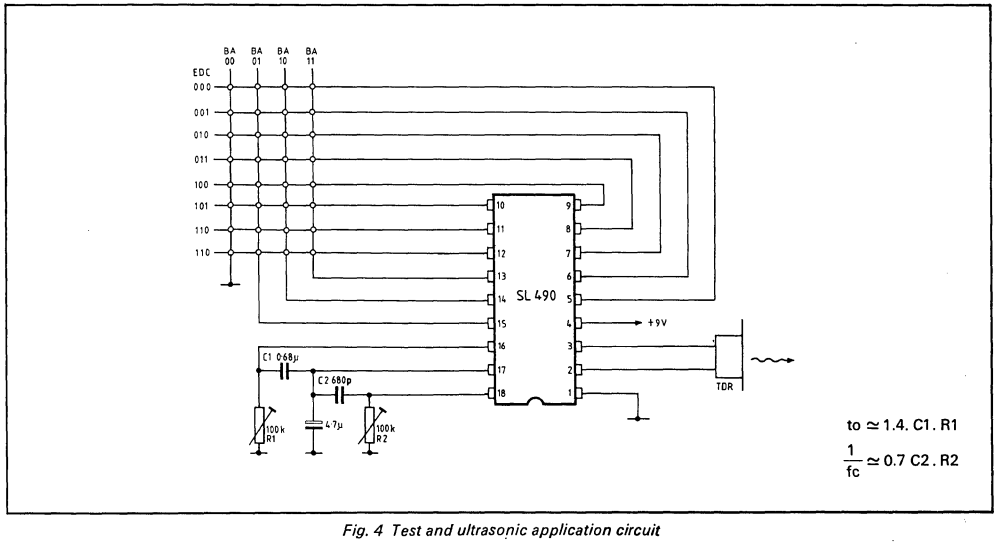


Fig. 4 Test and ultrasonic application circuit

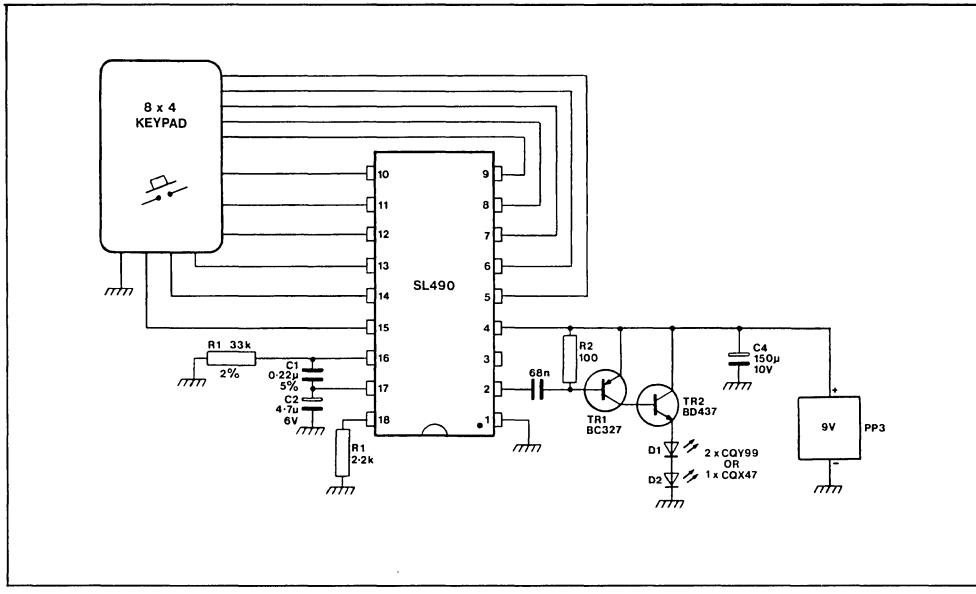


Fig.5 Infra-red application circuit

OPERATING NOTES

Fig.5 shows the circuit for a simple infra-red transmitter where the PPM output from pin 2 of the SL490 is fed to the base of the PNP transmitter TR1, producing an amplified current pulse about 15µsec wide. This pulse is further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red output is controlled by the quantity, type, and connection method of the diodes and also by the gain at high currents of the transistors.

The most common solution where cost is important is to use 2 single-chip diodes, such as the CQY99 connected in series.

Improved output can be obtained by using four CQY99 diodes in a series parallel arrangement, but it is usually simpler to use 2 multichip diodes such as the CQX47 connected in parallel or a single CQX19 which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflector.

When building the transmitter, care should be taken with the choice of the capacitor C2 and with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8Amps.

Transistor choice is also important and any substitutes should have high current gain characteristics and switching speeds similar to those specified in Fig.3.

An increase in output can be obtained by connecting TR2 in common emitter configuration, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequencies

Although the ML920 series of remote control receivers is designed to work over a wide range of PPM frequencies, the actual usable range may be restricted by the application. The analogue outputs on the ML920, ML922 and ML923 serve as a good example, since the outputs will step up or down, one step for each pair of PPM words received. This in turn fixes the rate of increment or decrement of the volume or colour controls of a TV set.

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig.5, power consumption will increase with frequency. It is thus advisable that with a battery power supply, the slowest PPM rate consistent with adequate response time should be chosen.

Setting Up Procedure

When designing a system using the SL490/491 transmitters and the ML920 series receivers, it is not necessary to adjust the PPM rate on both transmitter and receiver. The usual arrangement is to have a fixed resistor of 33k from pin 16 of the SL490/491 and to choose the capacitor connected for pin 16 to pin 17 to give the required PPM rate. The value is calculated from the formula $t_o = 1.4CR$. Provided fairly close tolerance components are used for C1 and R1, then assembled transmitter units should be interchangeable without adjustment.

The timing components on the receiver can be selected using the formula

$$f_{rx} = \frac{1}{0.15CR} \text{ where } f_{rx} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

The value of R for the receiver should be between 47k and 200k, a typical arrangement being to use a 47k fixed resistor and a 100k pot as shown in Fig.6. The capacitor should be selected from the above formula to give the nominal frequency somewhere near the mid-range setting of the potentiometer.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic 0 time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

When adjusting the ML920, the monitor output can be used for setting up, but in this case, a figure of 1/20th of the transmitter PPM logic 0 time should be used as the monitor output is at half the oscillator frequency.

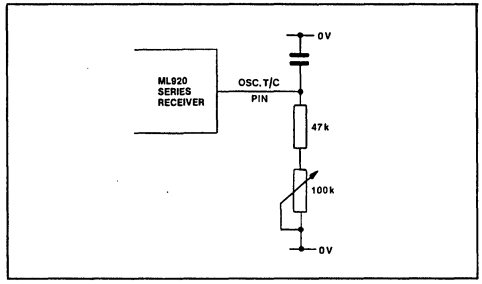


Fig.6 Recommended receiver time constant components

ABSOLUTE MAXIMUM RATINGS

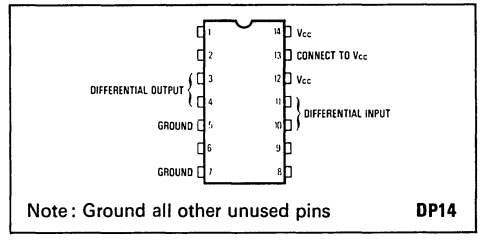
Supply voltage	7V to 9.5V
Total power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

SL 952
UHF AMPLIFIER

The SL952 amplifier has been designed to drive the prescaler (SP4020, CT1110 etc) in a frequency synthesis system directly from the tuner's local oscillator.

It features a differential output to reduce local oscillator radiation, and a differential input, which may be used to couple the outputs from a VHF and a UHF tuner (see Fig. 3).

The device operates from a single 5V supply with a minimal number of external components and is encapsulated in a 14 lead DIL package.



Note: Ground all other unused pins **DP14**

Fig. 1 Pin connections (top)

FEATURES

- Low Cost
- High Gain
- Minimal External Component Count
- Good Limiting Characteristics
- 1GHz Response
- 5V Supply

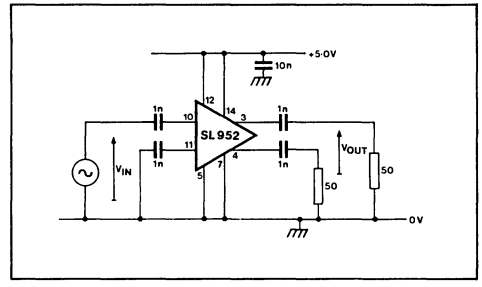


Fig. 2 Test circuit

ABSOLUTE MAXIMUM RATINGS

Vcc +10V
Ambient temperature 0°C to +65°C
Storage temperature −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc = 5.0V
TAMB = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.75	5.00	5.50	V	
Supply current		70	90	mA	
DC output level		3.2		V	
Output offset		100	600	mV	
Maximum differential output swing	600			mVp–p	950MHz
Differential voltage gain	30	35		dB	100MHz
Differential voltage gain	30	35		dB	500MHz
Differential voltage gain	15	26		dB	950MHz

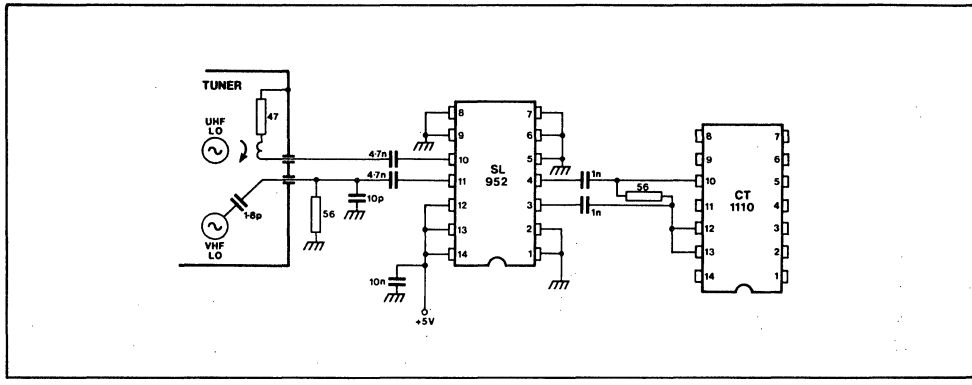


Fig. 3 Typical application for TV frequency synthesis

SL 1430

TV IF PREAMPLIFIER

The SL1430 is a fixed gain IF preamplifier for television with an output optimised for driving Plessey second generation low capacitance surface acoustic wave (SAW) filters. The addition of one external capacitor allows the amplifier to drive normal capacitance SAW filters from Plessey or from other manufacturers.

The device features on chip decoupling and differential output, requiring a minimal number of external components to be used.

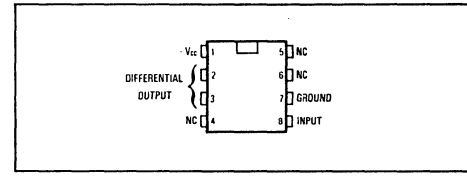


Fig. 1 Pin connections (top view)

FEATURES

- Low cost
- Low noise
- Low external component count
- Low distortion
- Direct 12V operation
- Can be used with different types of SAW filters

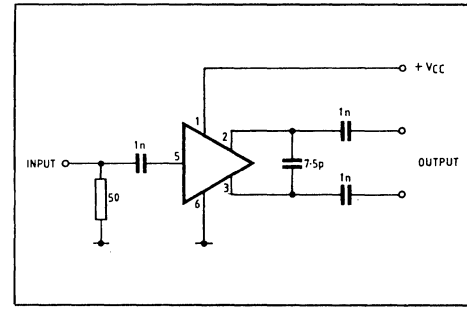


Fig. 2 Test circuit

QUICK REFERENCE DATA

- 26dB gain at 40MHz
- 12V supply at 25mA
- 120mV rms. input handling

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5 pF (Pins 2 and 3)
Measurements made using test circuit Fig. 2.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−0.5v to +25v
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

Characteristic	Pin	Value Min	Value Typ	Value Max	Units	Conditions
Supply voltage	1	7	12	13.5	V	
Quiescent current	1	15	25	35	mA	Pins 2, 3O/C
Cut-off frequency (−3dB)	5, 2/3	60	110		MHz	
Voltage gain		23	26	29	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% crossmodulation	5		75		mV	(wanted level 20mV unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mV	rms.
Noise figure	5		4		dB	
Input impedance	5		300Ω// 4.2pF			

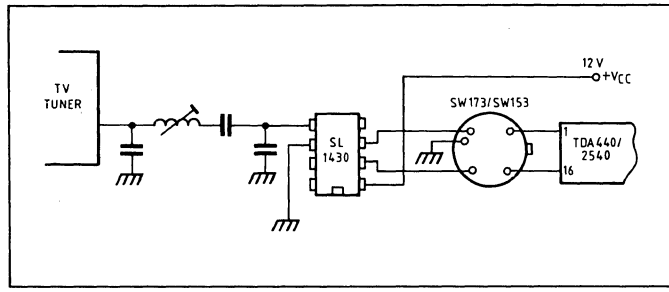


Fig. 3 Typical applications

SL1430 TYPICAL CHARACTERISTICS AT ,12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10KHz

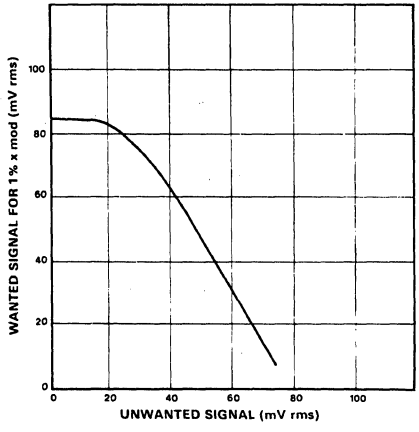


Fig. 4 Cross modulation performance (see note 1)

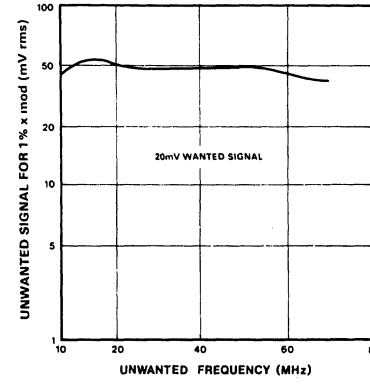


Fig. 6 Cross modulation performance V frequency of unwanted signal (see note 1)

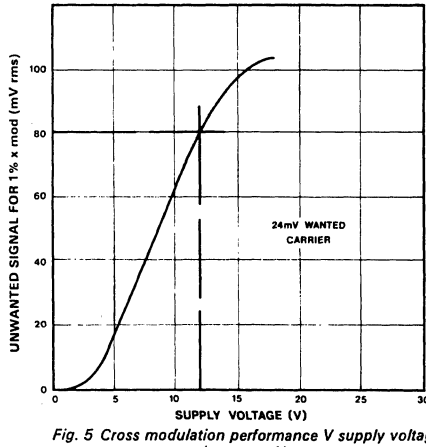


Fig. 5 Cross modulation performance V supply voltage (see note 1)

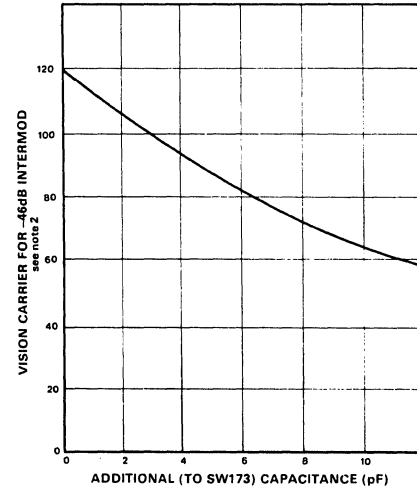


Fig. 7 Intermodulation performance v. load capacitance

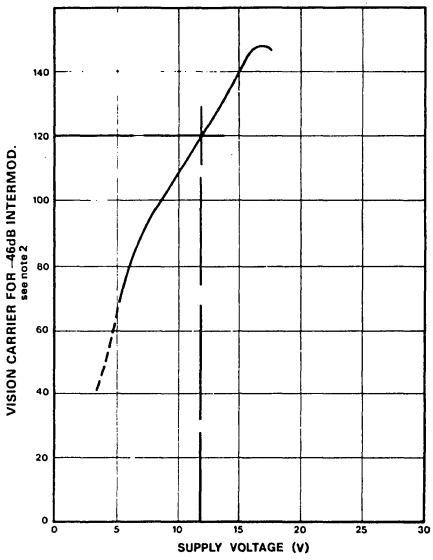


Fig. 8 Intermodulation performance v. supply voltage

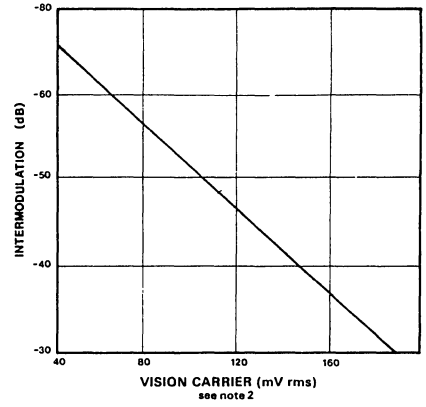


Fig. 9 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

SL 1431/2

TV IF PREAMPLIFIERS WITH AGC GENERATOR

The SL1431 and SL1432 are fixed gain IF preamplifiers for television with a differential output optimised for driving Plessey surface acoustic wave (SAW) filters. Besides providing the necessary gain block between the tuner and SAW filter they also supply a properly derived, broadband AGC signal to the tuner, the SL1431 providing the correct sense signal for a PNP tuner, and the SL1432 for an NPN tuner. The tuner AGC threshold is internally preset to a value to allow adequate signal handling in the SL1431 and SL1432 and does not normally require any external adjustment. However, to account for the large variations in signal handling capability which is encountered on some tuners, the tuner AGC threshold may be externally adjusted by altering the bias on pin 1.

Both devices feature on-chip decoupling for a minimum external component count.

AGC Signal

For high input signal levels the voltage on pin 7 goes low with SL1431 and high with the SL1432.

QUICK REFERENCE DATA

- 26dB Gain at 40MHz
- 12V Supply at 25mA
- 120mV R.M.S. Input Handling
- 15mA Tuner AGC Capability

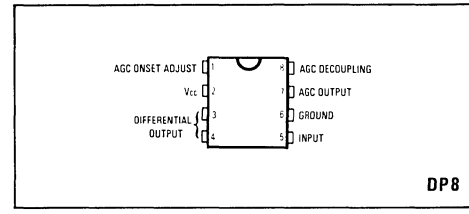


Fig. 1 Pin connections

FEATURES

- Properly Derived Tuner AGC
- Low Cost
- Low Noise
- Low External Component Count
- Low Distortion
- Direct 12V Operation
- Can be used with Different Types of SAW Filters

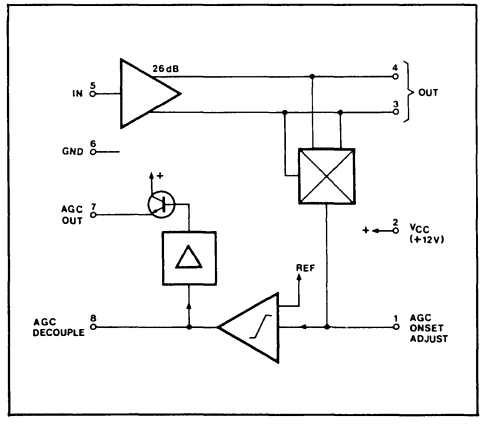


Fig. 2 Block diagram

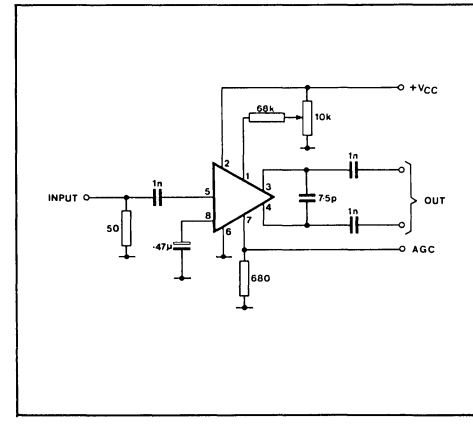


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +125°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5pF (Pins 3 and 4)
Measurements made using test circuit Fig. 3.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Voltage	2	7	12	13.5	V	
Quiescent Current	2	15	25	33	mA	Pins o/c
Cut-off frequency (—3dB)	5	60	110		MHz	
Voltage gain		23	26	29	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% cross-modulation	5		75		mV	(wanted level 20mV, unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mVrms	
Noise figure	5		4		dB	
Input impedance	5		300Ω //4.2pF			
Tuner AGC						
Output current	7	15	20		mA	@ 10.0 V
Input impedance	1		6		kΩ	

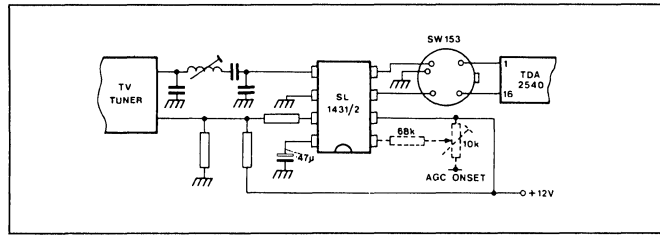


Fig. 4 Typical applications

SL1431 TYPICAL CHARACTERISTICS AT ,12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10KHz

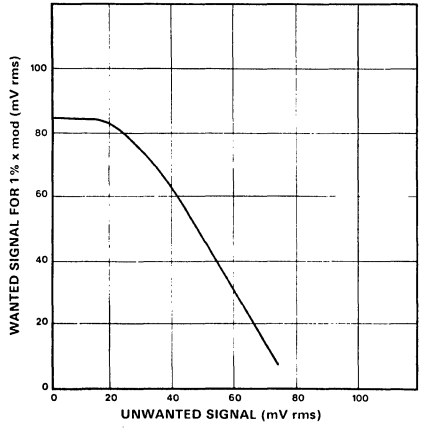


Fig. 5 Cross modulation performance (see note 1)

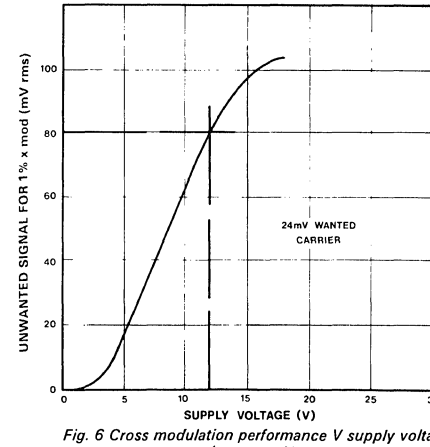


Fig. 6 Cross modulation performance V supply voltage (see note 1)

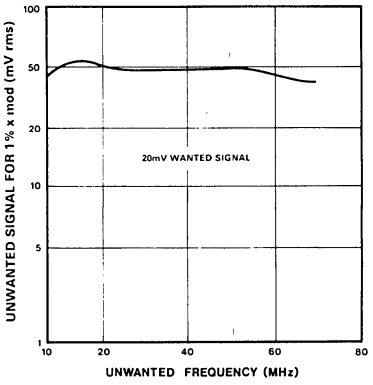


Fig. 7 Cross modulation performance V frequency of unwanted signal (see note 1)

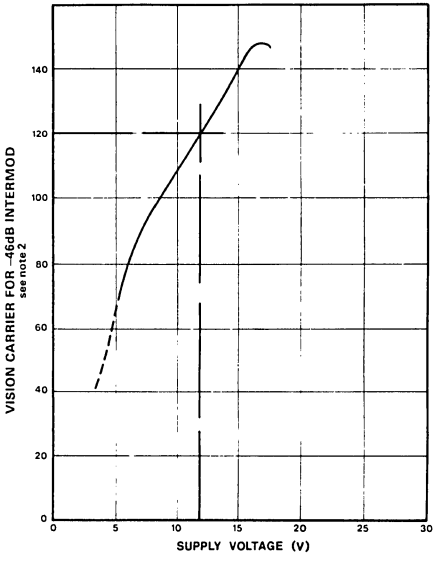


Fig. 9 Intermodulation performance v. supply voltage

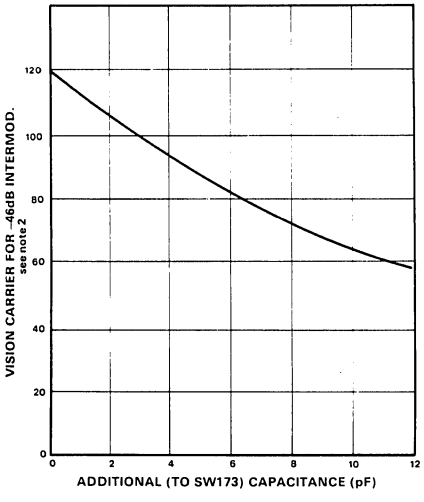


Fig. 8 Intermodulation performance v. load capacitance

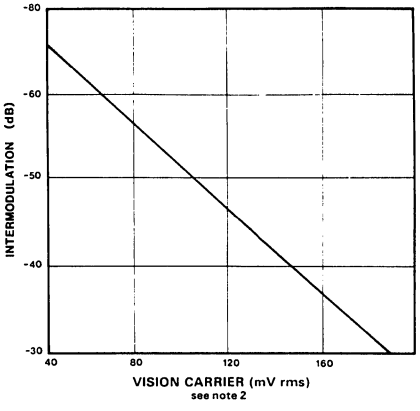


Fig. 10 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

SL 1440

PARALLEL SOUND AND VISION IF AMPLIFIERS AND DETECTORS

This IC is designed to operate with a two output port surface acoustic wave IF filter, one output for vision and chrominance carriers with no sound carrier, and one output for the sound carrier only.

The IC amplifies and detects the sound and vision carrier in two separate channels, the detectors being of the wide band switching type, not requiring any tuning. An AGC system is applied to the vision channel, the sound channel being made to hard limit.

There is no facility for tuner AGC, an SL1431 should be used to provide this signal, operating before the SWAF to provide superior overload performance and needing no preset adjustment.

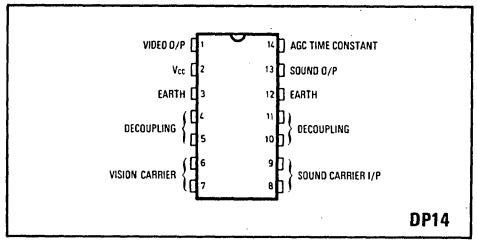


Fig. 1 Pin connections (top view)

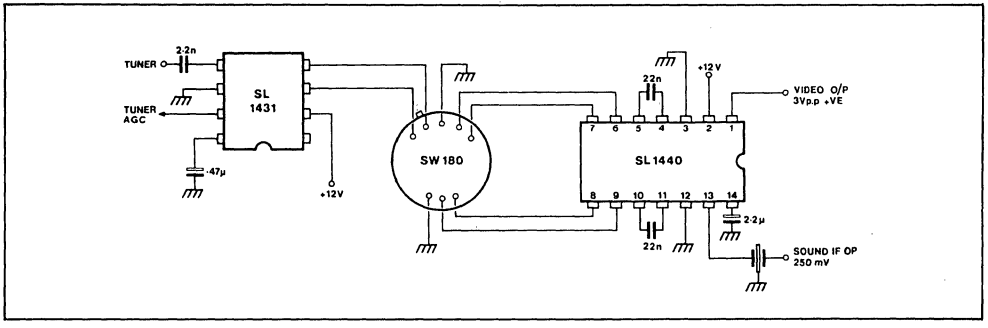


Fig. 2 Typical application SL1440

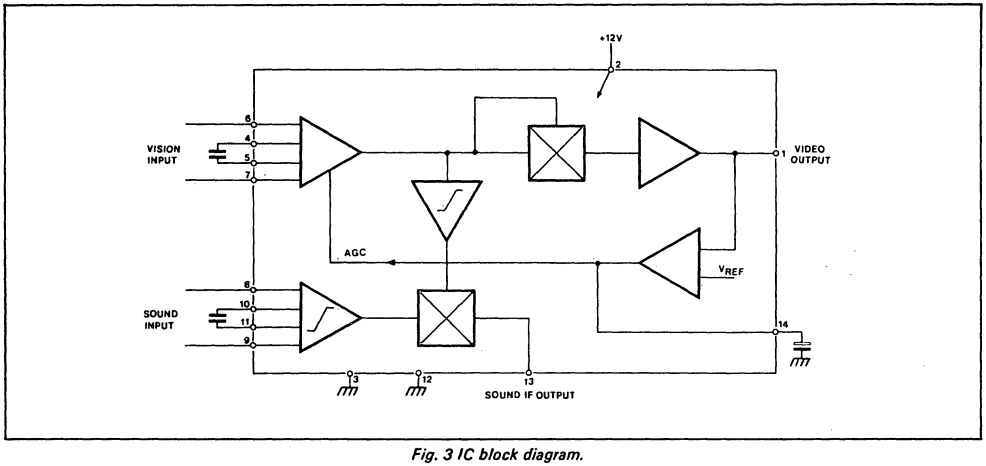


Fig. 3 IC block diagram.

SP4020 SP4021

VHF/UHF ÷ 64 PRESCALERS

The SP4020 and SP4021 are ECL divide by 64s which will operate at frequencies in excess of 950MHz, and are intended for use as prescalers in television receiver synthesiser tuners.

The SP4020 has separate inputs for VHF and UHF and the devices have a typical power dissipation of 470mW at the nominal supply voltage of +6.8V.

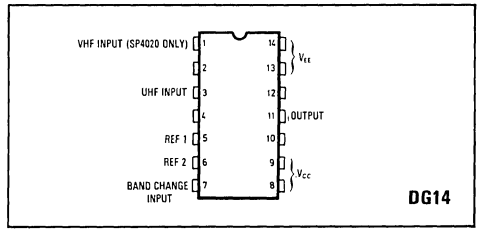


Fig. 1 Pin connections

FEATURES

- Dual Input Ports for VHF and UHF (SP4020)
- Self-Biasing Clock Inputs
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input (SP4020)
- Push-Pull TTL O/P

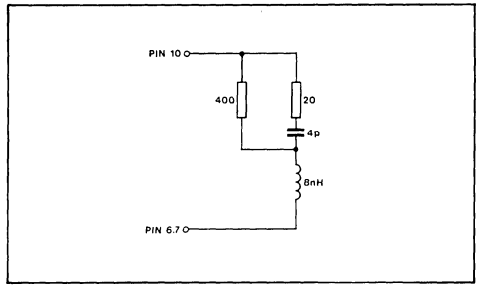


Fig. 2 Equivalent small signal input impedance (80MHz–1GHz)

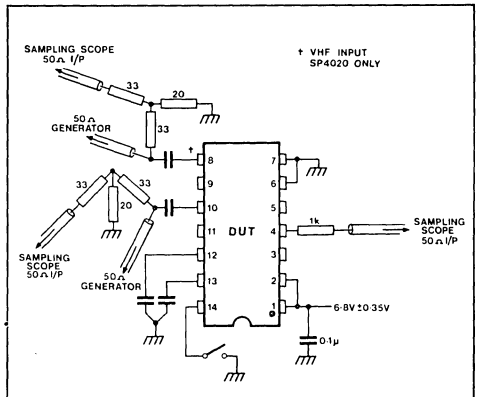
OPERATING NOTES

Two input ports are available on the SP4020. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring at high frequencies. Both inputs are terminated by a nominal 400 Ω and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1GHz.

When the device is switched to the VHF input, an input hysteresis of 50mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF\,1} - V_{REF\,2}$

If the SP4021 is required to operate with a sinewave input below 100MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). At low frequency the output will change when one of the clock change inputs changes from a low to a high level. Self oscillation may result if the input signal falls below the minimum specified.

The devices may be operated down to very low frequencies if a square wave input with an edge speed greater than 200V/μs is used.



Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

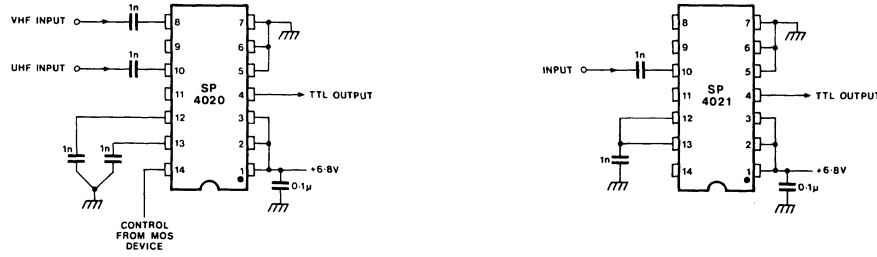
Fig. 3 AC test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{EE} = oV, Vcc = +6.45V to +7.15V
Clock input voltage sinusoidal
T_A: +25°C
Pin 14 O/P

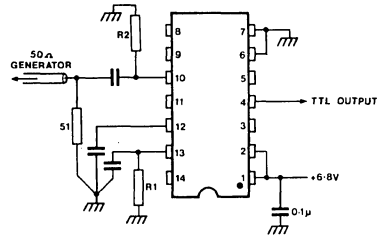
Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1,2	6.45	6.80	7.15	V	
Supply current	1,2	40	68	90	mA	Vcc = 6.8V
Output level high	4	2.5	3.5	5.0	V	−1mA
Output level low	4		0.3	0.5	V	5mA
Band change input (SP4020 only)						See Note 1
High level	14	2.5			V	For UHF input
Low level	14			0.4	V	For VHF input
Low level I/P current	14			−0.8	mA	@ 0.4V
Max. clamp current	14	−3			mA	@ −0.7V
Sensitivity						
SP4020:-						
VHF I/P 100MHz	8		100	300	mVp–p	Pin 14 to 0V
VHF I/P 300MHz			50	300	mVp–p	Pin 14 to 0V
UHF I/P 500–800MHz	10		100	300	mVp–p	
UHF I/P 950MHz			50	300	mVp–p	See Note 2
SP4021:-						
I/P 100MHz	10		120	400	mVp–p	
I/P 300–800MHz			100	300	mVp–p	
I/P 950MHz			50	300	mVp–p	See Note 2
Overload level						
SP4020:-						
VHF I/P 100–300MHz	8	0.9	2.0		Vp–p	
UHF I/P 100–950MHz	10	0.9	2.0		Vp–p	Pin 14 to 0V
SP4021:-						
I/P 100–300MHz	10	1.0	2.0		Vp–p	
I/P 500–950MHz	10	0.9	2.0		Vp–p	

Note 1 TTL type including negative input voltage clamp
Note 2 This is measured with the device in a low profile socket; soldered results show, typically, a 25% improvement.



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 Application circuit



Capacitors are 1nF unless otherwise stated. Values should be increased if operation below 10MHz is required.

For 50mV hysteresis R1 = 36kΩR2 = ∞
For 100mV hysteresis R1 = 18kΩR2 = 18kΩ

Fig. 5 Wideband operation

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC} – V_{EE}	0V to +10V
Input voltage, clock inputs	2.5V p–p
Band change input (SP4020)	+7.2 to –0.5V or –10mA
Output current	+30mA to –30mA
Operating temperature	0°C to +65°C
Storage temperature	–55°C to +125°C

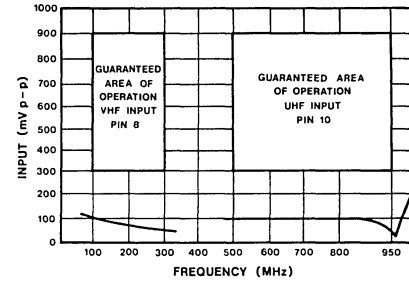


Fig. 6 SP4020 typical sensitivity with limits of operation when used in application circuit (Fig. 4)

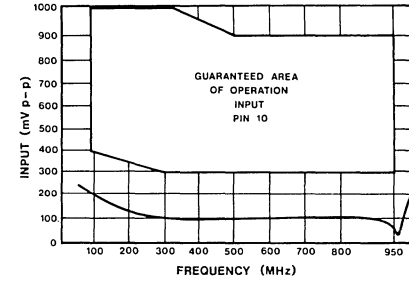


Fig. 7 SP4021 Typical sensitivity with limits of operation when used in application circuit (Fig. 4) with pin 14 open circuit.

SP4040 SP4041

VHF/UHF ÷256 PRESCALERS

The SP4040 and SP4041 are ECL divide by 256 which will operate at frequencies in excess of 950MHz, and are intended for use as prescalers in television receiver synthesiser tuners.

The SP4040 has separate inputs for VHF and UHF and the devices have a typical power dissipation of 500mW at the nominal supply voltage of +6.8V.

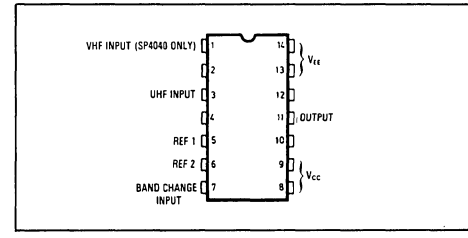


Fig. 1 Pin connections

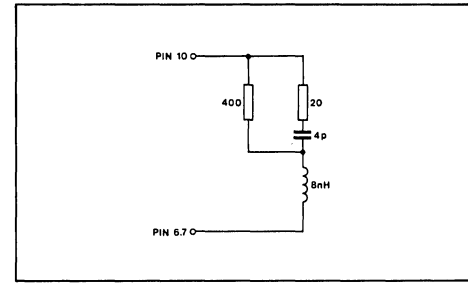


Fig. 2 Equivalent small signal input impedance (80MHz–1GHz)

FEATURES

- Dual Input Ports for VHF and UHF (SP4040)
- Self-Biasing Clock Inputs
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input (SP4040)
- Push-Pull TTL O/P

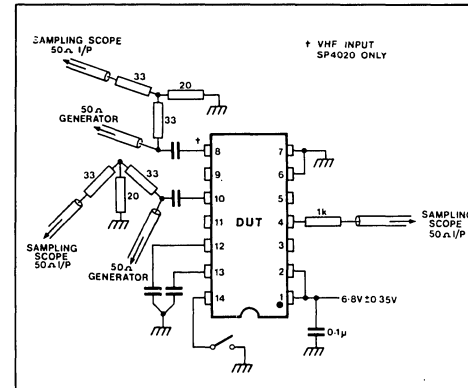
OPERATING NOTES

Two input ports are available on the SP4040. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring at high frequencies. Both inputs are terminated by a nominal 400 Ω and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1GHz.

When the device is switched to the VHF input, an input hysteresis of 50mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF\,1} - V_{REF\,2}$

If the SP4041 is required to operate with a sinewave input below 100MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). At low frequency the output will change when one of the clock change inputs changes from a low to a high level. Self oscillation may result if the input signal falls below the minimum specified.

The devices may be operated down to very low frequencies if a square wave input with an edge speed greater than 200V/μs is used.



Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

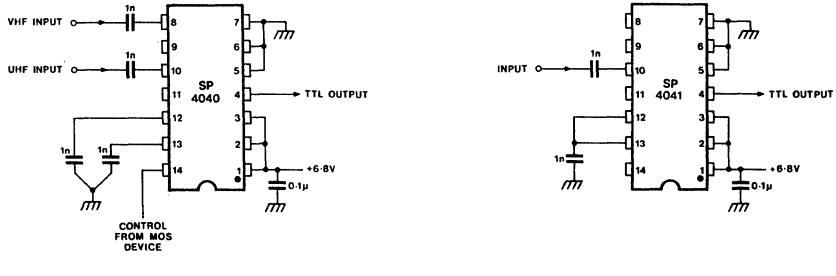
Fig. 3 AC test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{EE} = oV, Vcc = +6.45V to +7.15V
Clock input voltage sinusoidal
T_A: +25°C
Pin 14 O/P

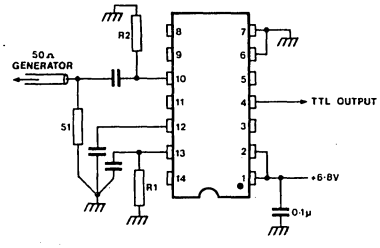
Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1,2	6.45	6.80	7.15	V	
Supply current	1,2	50	70	95	mA	V_{CC} = 7.15V
Output level:						
High	4	2.5	3.5	5.0	V	−1mA
Low	4		0.3	0.5	V	5mA
Band change input						
High level	14	2.5			V	For UHF input } SP4040
Low level	14			0.4	V	For VHF input } only
Low level I/P current	14			−0.8	mA	@ 0.4V } only
Max. clamp current	14	−3			mA	@ −0.7V } only
Sensitivity						
SP4040:-						
VHF I/P 100MHz	8		120	300	mVp–p	Pin 14 to 0V
300MHz			100	300	mVp–p	Pin 14 to 0V
UHF I/P 500–800MHz	10		100	300	mVp–p	
950MHz	10		250	440	mVp–p	Note 1
SP4041:-						
100MHz	10		400	550	mVp–p	
200MHz	10		300	400	mVp–p	
300MHz	10		150	350	mVp–p	
500–700MHz	10		100	300	mVp–p	
800MHz	10		200	400	mVp–p	
950MHz	10		400	700	mVp–p	Note 1
Overload level						
SP4040:-						
VHF I/P 100–300MHz	8	1.0	2.0		Vp–p	
UHF I/P 500–600MHz	10	1.0	2.0		Vp–p	Pin 14 to 0V
SP1041:-						
100MHz	10	1.2	2.0		Vp–p	
300MHz	10	1.0	2.0		Vp–p	
500–600MHz	10	1.0	2.0		Vp–p	
950MHz	10	1.2	2.5		Vp–p	

Note 1. This is measured with the device in a low profile socket; soldered in results show typically a 25% improvement.



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 Application circuit



Capacitors are 1nF unless otherwise stated. Values should be increased if operation below 10MHz is required.

For 50mV hysteresis R1 = 36kΩR2 = ∞
For 100mV hysteresis R1 = 18kΩR2 = 18kΩ

Fig. 5 Wideband operation

ABSOLUTE MAXIMUM RATINGS

Power supply voltage Vcc – VEE	0V to +10V
Input voltage, clock inputs	2.5V p–p
Band change input (SP4040)	+7.2 to –0.5V or –10mA
Output current	+30mA to –30mA
Operating temperature	0°C to +65°C
Storage temperature	–55°C to +125°C

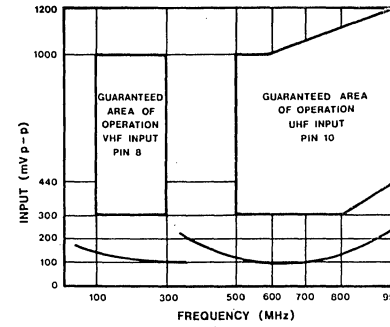


Fig. 6 SP4040 typical sensitivity with limits of operation when used in application circuit (Fig. 4)

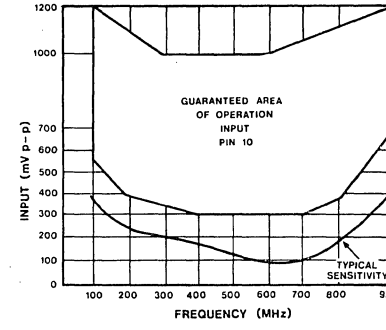


Fig. 7 SP4041 Typical sensitivity with limits of operation when used in application circuit (Fig. 4) with pin 14 open circuit.

SW150 SW153 SW170 SW173 SW200 SW250 SW400 SW450

SURFACE ACOUSTIC WAVE COLOUR TV IF FILTERS

This comprehensive range of TV IF filters utilises Plessey Surface Acoustic Wave technology and is suitable for use in colour or monochrome television receivers world wide. The frequency pass-band and phase response of each of these highly stable devices are tailored to the relative transmission standard. The devices require no adjustment and are packaged in a totally hermetic Metal/Glass T08 package.

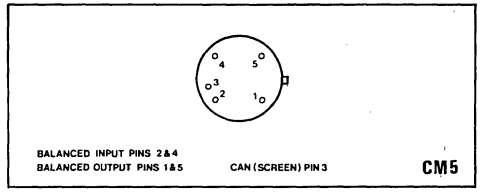


Fig. 1 Pin connections (viewed from beneath)

FEATURES

- No Adjustment Necessary
- Low Cost
- Compact Dimensions
- High Stability
- High Reliability
- Comprehensive Range of Standards Available

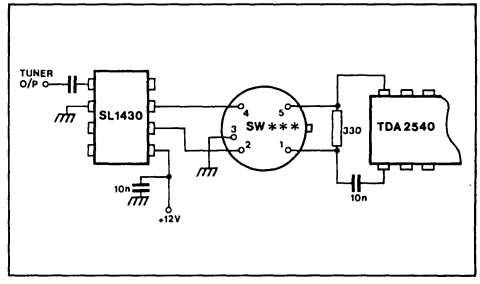


Fig. 2 Typical application

APPLICATION NOTES

The input drive and output load circuitry should provide a low impedance across at least one device port to minimise spurious signals due to secondary device characteristics. Fig. 2 shows a typical application, the SL1430 providing a very low drive impedance. The 330 Ω load resistor is included to ensure stability of the TDA2540 and may be omitted in some designs that do not use this device.

Care must be taken with the printed circuit board layout, and the use of balanced input and output is advised to ensure low levels of direct breakthrough. The device must also be mounted with minimum lead length. Application introduced direct breakthrough will exhibit itself as a deterioration in amplitude and group delay ripple, and a screen image approximately 1.5μs before the main response.

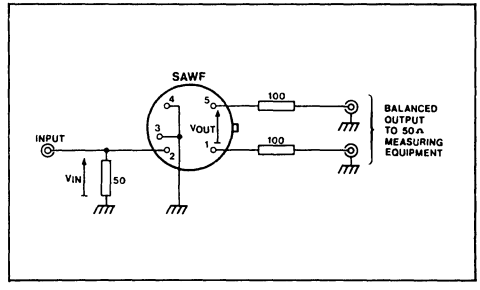


Fig. 3 Test circuit

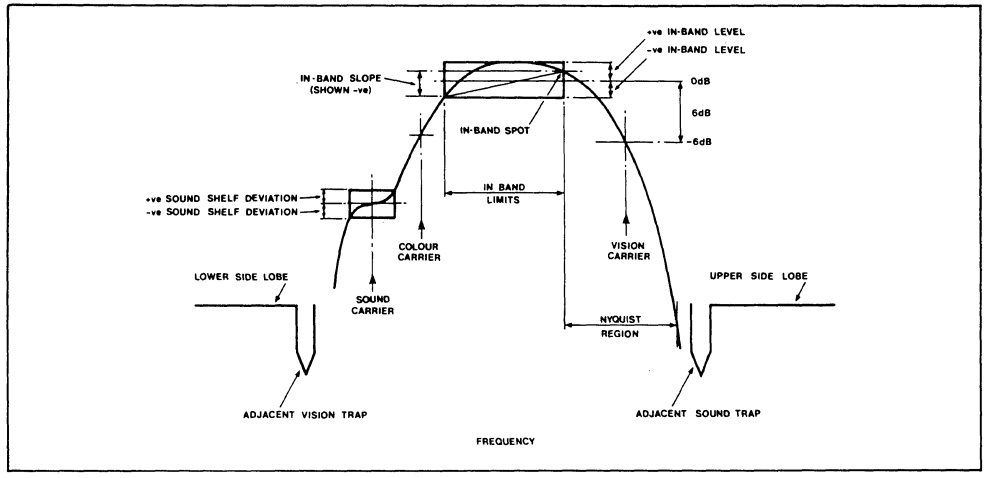


Fig. 4 Amplitude characteristics

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) :-

Ambient temperature	+35°C
Input drive impedance	50 Ω
Load impedance	300 Ω balanced

The amplitude level at the vision carrier frequency is taken to be —6dB and is then used as a reference for all other relevant measurements (see Fig. 4).
The insertion loss is defined as the voltage ratio V_{IN}/V_{OUT} in the test circuit (Fig. 3) and is expressed in dB.

The amplitude characteristics given in the Electrical Characteristic tables are defined in Fig. 4. The response in the Nyquist region is guaranteed by the measurement of the 2T $\sin^2$ pulse and bar K rating after synchronous demodulation.

In band amplitude and group delay ripple is defined as the worst deviation from the mean over any 500Khz bandwidth between the two defined in-band frequency limits.

The measurement of spurious outputs includes those due to internal reflections and direct breakthrough, a 2T $\sin^2$ pulse being used and measurements being made between 2 and 1μs before, and 1 and 4μs after, the centre of the main response.

SW150

The SW150 is a TV IF filter for the United Kingdom PAL standard, system I, with a vision carrier frequency of 39.5MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	39.5		Ref. level	—6	dB	
Colour carrier	35.1	—7	—3	0	dB	
Sound carrier	33.5	—27	—24	—21	dB	
Sound shelf deviation	33.2–33.8		±3		dB	
In-band level	36–38	—3	0	2	dB	
In band spot	38	—2	0	1.5	dB	
In-band slope	35.5	0	—2	—4	dB	w.r.t. level at 38MHz
In-band ripple	36–38		0.5	1	dB	Peak
Adjacent vision trap	31.5	—45	—55		dB	
Adjacent sound trap	41.5	—42	—50		dB	
Lower side lobe	26.5–31.5	—38	—45		dB	
Upper side lobe	41.5–46.5	—36	—42		dB	
	46.5–100		—30		dB	
Insertion loss	38.0		17	21	dB	
2T $\sin^2$ pulse and bar K rating	39.5		1.5	2	%	
Group delay:-						
Ripple	36.0–39		5	10	ns	
Deviation	34.5–40.5		10	40	ns	
Spurious outputs	39.5		—46	—40	dB	
Temperature coefficient of frequency			—90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1kΩ// 12pF			
Output pins 1 & 5			1.6kΩ// 10pF			

SW153

The SW153 is a TV IF filter for the United Kingdom PAL standard, system I, with a vision carrier frequency of 39.5MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	39.5		Ref. level −6		dB	
Colour carrier	35.1	−6	−3	0	dB	
Sound carrier	33.5	−25	−22	−19	dB	
Sound shelf deviation	33.2–33.8		±1	±3	dB	
In-band level	36–38	−2	0	2	dB	
In band spot	38	−1.5	0	1.5	dB	
In-band slope	35.5	0	−1	−2	dB	w.r.t. level at 38MHz
In-band ripple	36–38		0.5	1	dB	Peak
Adjacent vision trap	31.5	−45	−55		dB	
Adjacent sound trap	41.5	−40	−50		dB	
Lower side lobe	26.5–31.5	−40	−50		dB	
Upper side lobe	41.5–46.5	−36	−42		dB	
	46.5–100		−30		dB	
Insertion loss	38.0		21	25	dB	
2T $\sin^2$ pulse and bar K rating	39.5		1.5	2	%	
Group delay:-						
Ripple	36.0–39.0		5	10	ns	
Deviation	34.5–40.5		10	40	ns	
Spurious outputs	39.5		−46	−40	dB	
Temperature coefficient of frequency			−90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6k Ω// 8pF			
Output pins 1 & 5			1.8k Ω// 10pF			

SW170

The SW170 is a TV IF filter for the European PAL standard, systems B and G, with a vision carrier frequency of 38.9MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	38.9		Ref. level −6		dB	
Colour carrier	34.5	−7.5	−4	−2.5	dB	
Sound carrier	33.4	−27	−22	−18	dB	
Sound shelf deviation	33.1–33.5		±3		dB	
In-band level	35.5–37.4	−3	0	2	dB	
In band spot	37.4	−1.5	0	1.5	dB	
In-band slope	35.5	−0.5	−2	−3	dB	w.r.t. level at 37.4MHz
In-band ripple	35.5–37.4		0.5	1	dB	Peak
Adjacent vision trap						
VHF	30.9	−36	−40		dB	
UHF	31.9	−38	−45		dB	
Adjacent sound trap						
UHF	40.4	−38	−45		dB	
VHF	41.4	−36	−40		dB	
Lower side lobe	27.5–31.9	−35	−40		dB	
Upper side lobe	40.4–45	−35	−40		dB	
	45–100		−20		dB	
Insertion loss	37.4		18	24	dB	
2T $\sin^2$ pulse and bar K rating	38.9		2	3	%	
Group delay:-						
Ripple	36–38		25		ns	Peak
Deviation	34.5		170		ns	Reference 0 @ 38.9MHz
	35.15		0		ns	Reference 0 @ 38.9MHz
	36.9		−90		ns	Reference 0 @ 38.9MHz
Spurious outputs	38.9		−46	−40	dB	
Temperature coefficient of frequency			−90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1k Ω// 12pF			
Output pins 1 & 5			1.6k Ω// 10pF			

SW173

The SW173 is a TV IF filter for the European PAL standard, systems B and G, with a vision frequency of 38.9

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	38.9		Ref. level	–6	dB	
Colour carrier	34.5	–5	–3.5	–2	dB	
Sound carrier	33.4	–23	–20	–17	dB	
Sound shelf deviation	33.1–33.5		+4/–1	+6/–3	dB	
In-band level	35.5–37.4	–2	0	1	dB	
In-band spot	37.4	–1	0	1	dB	
In-band slope	35.5	0	–1.5	–2.5	dB	wrt level at 37.4MHz
In-band ripple	35.5–37.4		0.75	1.5	dB	Peak
Adjacent vision trap						
VHF	30.9	–40	–43		dB	
UHF	31.9	–43	–48		dB	
Adjacent sound trap						
UHF	40.4	–43	–48		dB	
VHF	41.4	–40	–43		dB	
Lower side lobe	27.5–3[illegible].9	–36	–40		dB	
Upper side lobe	40.4–45	–37	–42		dB	
	45–100		–30		dB	
Insertion loss	37.4		22	26	dB	
2T $\sin^2$ pulse and bar K rating	38.9		2	3	%	
Group delay						
Ripple	36–38		25	50	ns	Peak
Deviation	34.1		400		ns	Reference 0 @ 38.9MHz
	34.5		170		ns	Reference 0 @ 38.9MHz
	35.15		0		ns	Reference 0 @ 38.9MHz
	36.9		–90		ns	Reference 0 @ 38.9MHz
	37.9		–53		ns	Reference 0 @ 38.9MHz
	39.9		–53		ns	Reference 0 @ 38.9MHz
Spurious outputs	38.9		–46	–40	dB	
Temperature coefficient of frequency			–90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 8pF			
Output pins 1 & 5			1.8kΩ// 10pF			

SW200

The SW200 is a TV IF filter for the North American NTSC standard, systems M and N, with a vision carrier frequency of 45.75MHz.

Characteristics	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	45.75		Ref. level	–6	dB	
Colour carrier	42.17	–7	–4	0	dB	
Sound carrier	41.25	–24	–20	–16	dB	
In-band level	43–44.25	–3	0	3	dB	
In-band ripple	43–44.25		0.5	1.5	dB	Peak
Adjacent vision trap	39.75	–40	–50		dB	
Adjacent sound trap	47.5	–35	–45		dB	
Lower side lobe	35–39.75	–35	–40		dB	
Upper side lobe	47.5–52.5	–30	–36		dB	
Insertion loss			19	25	dB	
2T $\sin^2$ pulse and bar K rating			2	3	%	
Group delay:-						
Ripple	43–44.25		10		ns	
Deviation	42–46		50		ns	
Spurious outputs	45.75		–44	–38	dB	
Temperature coefficient of frequency			–90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1kΩ// 13pF			
Output pins 1 & 5			1.5kΩ// 11pF			

SW250

The SW250 is a TV IF filter for the French SECAM standard, systems L and L', with a vision carrier frequency of 32.7MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	32.7		Ref. level −6		dB	
Colour carrier region	37	−2	0	1	dB	
	38	−3	−6	−9	dB	
In-band level	34.5–36	−2	0	2	dB	
In-band ripple	34.5–36		0.5	1	dB	Peak
Adjacent vision trap	40.7	−38	−43		dB	
Adjacent sound trap	31.2	−46	−50		dB	
Own sound						
UHF	39.2	−43	−46		dB	
VHF	43.85	−43	−46		dB	
Lower side lobe	26–31.2	−36	−40		dB	
Upper side lobe	39.2–40.7	−38	−43		dB	
	40.7–45	−36	−40		dB	
	45–90		−30		dB	
Insertion loss	34.5		19	25	dB	
2T sin² pulse and bar K rating	32.7		2	3	%	
Group delay:-						
Ripple	34.5–36		10		ns	
Deviation	34.5–36		10	50	ns	
Spurious outputs	32.7		−46	−40	dB	
Temperature coefficient of frequency			−90		ppm/°C	
Small signal impedance						
Input pins 2 & 4			1.6k Ω// 10pF			
Output pins 1 & 5			1.2k Ω// 11pF			

SW400

The SW400 is a TV IF filter for the Australian PAL standard, systems B and G, with a vision carrier frequency of 36.875MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	36.875		Ref. level −6		dB	
Colour carrier	32.445	−7	−3	−1	dB	
Sound carrier	31.375	−26	−22	−18	dB	
In-band level	33.475– 35.375	−3	0	2	dB	
In band ripple	33.475– 35.375		0.5	1.5	dB	Peak
Adjacent vision trap						
VHF	28.875	−36	−40		dB	
UHF	29.875	−38	−45		dB	
Adjacent sound trap						
VHF	28.375	−38	−45		dB	
UHF	39.375	−36	−40		dB	
Lower side lobe	25.0– 29.875	−35	−40		dB	
Upper side lobe	38.375– 43.0	−35	−40		dB	
Insertion loss	35.375		18	24	dB	
2T sin² pulse and bar K rating	36.875		2	3	%	
Group delay						
Ripple	32.5–35.375		25		ns	
Deviation	32.445		175		ns	Reference 0 @ 36.875MHz
	34.125		0		ns	
	34.875		−80		ns	
Spurious outputs	36.875		−46	−40	dB	
Temperature coefficient of frequency			−90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1k Ω// 12pF			
Output pins 1 & 5			1.6k Ω// 10pF			

SW450

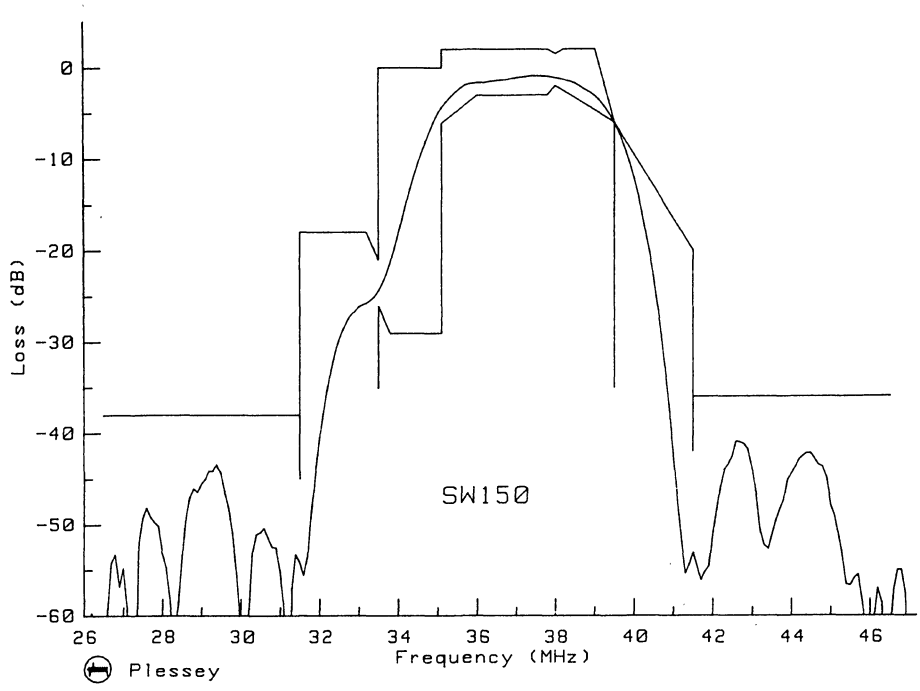
The SW450 is a TV IF filter for the South African PAL standard, system I, with a vision carrier frequency of 38.9MHz.

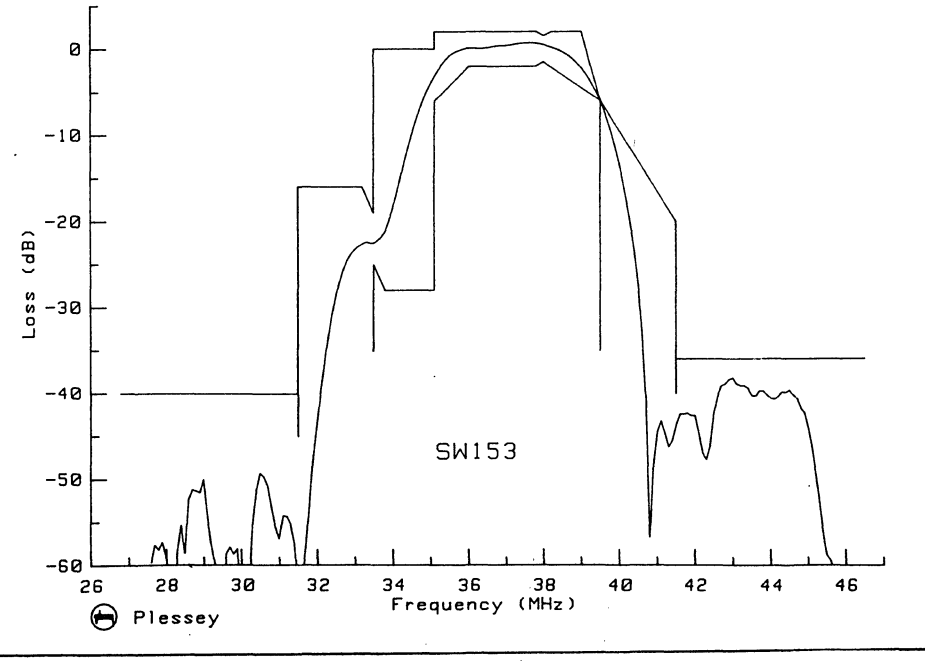
Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	38.9		Ref. level −6		dB	
Colour carrier	34.47	−7	−4	0	dB	
Sound carrier	32.9	−34	−30	−26	dB	
In-band level	35.5–37.4	−3	0	2	dB	
In-band ripple	35.5–37.4		0.5	1.5	dB	Peak
Adjacent vision trap	30.9	−38	−46		dB	
Adjacent sound trap	40.9	−38	−43		dB	
Lower side lobe	25.8–30.9	−36	−40		dB	
Upper side lobe	40.9–46	−36	−40		dB	
Insertion loss	37.4		17	23	dB	
2T $\sin^2$ pulse and bar K rating	38.9		1.5	2	%	
Group delay:-						
Ripple	35.5–37.4		10		ns	
Deviation	35.5–37.4		25	50	ns	
Spurious outputs	38.9		−46	−40	dB	
Temperature coefficient of frequency			−90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1kΩ// 12pF			
Output pins 1 & 5			1.6kΩ// 10pF			

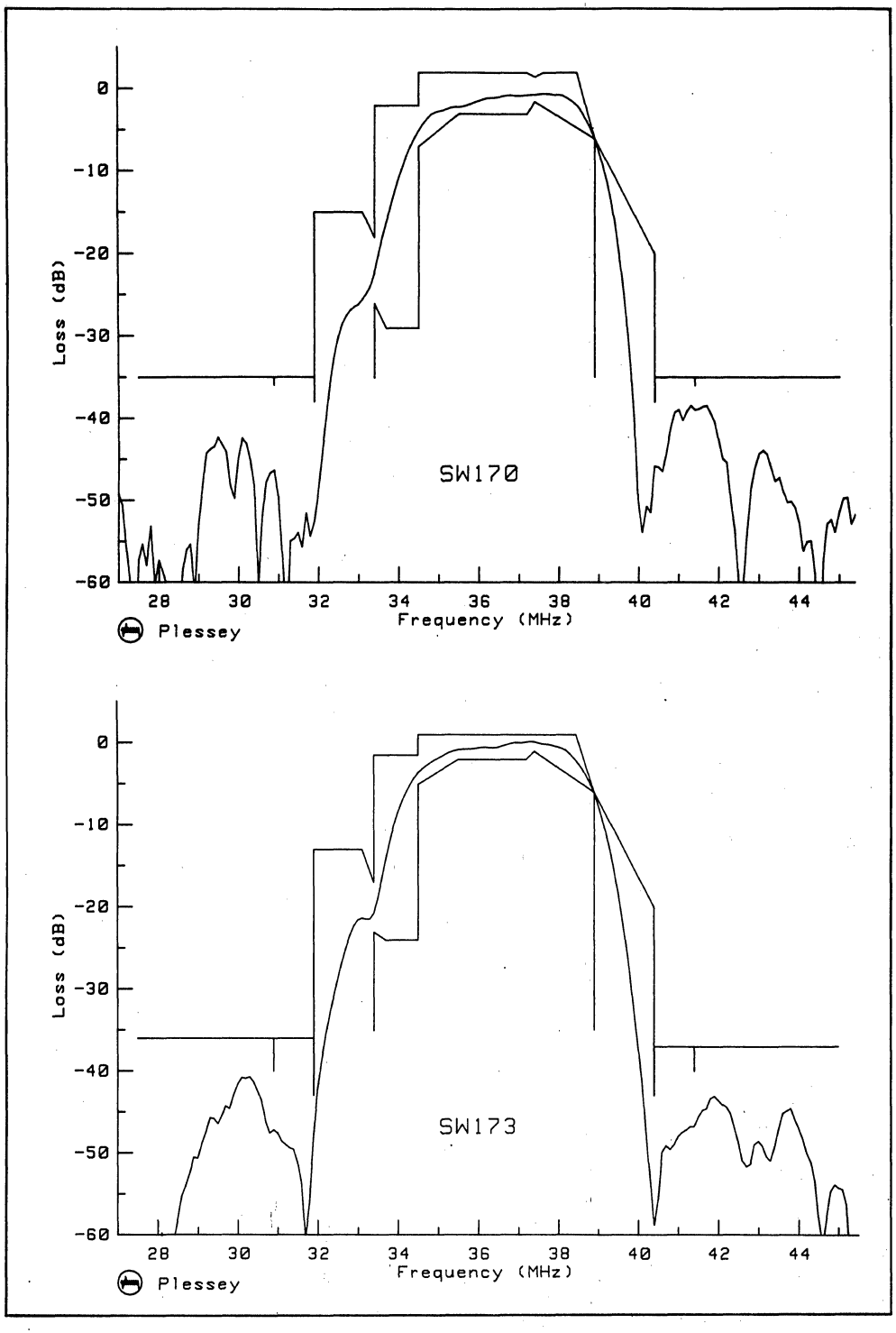
ABSOLUTE MAXIMUM RATINGS

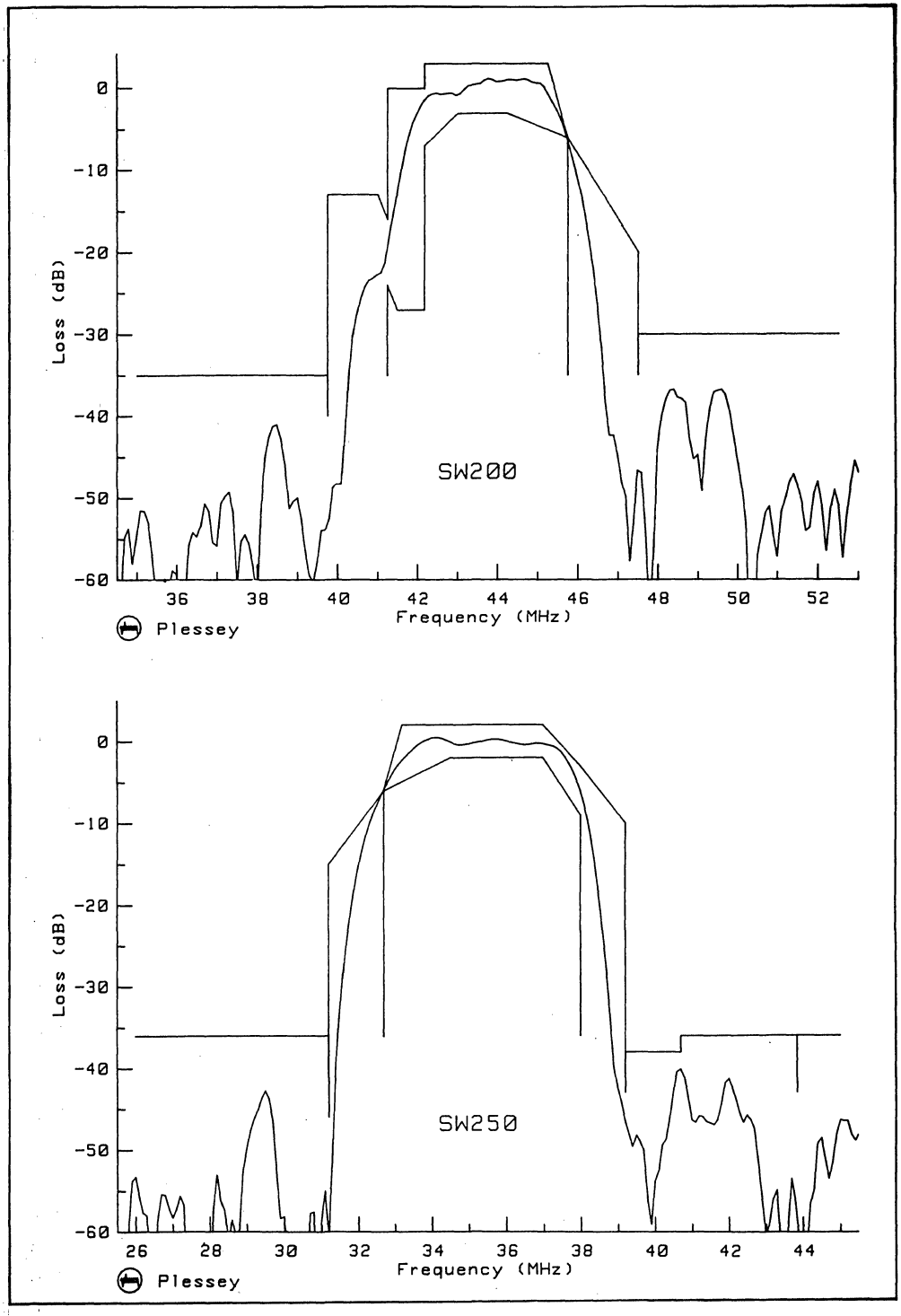
Storage temperature	−25°C to +85°C
Operating temperature	−10°C to +70°C
Pin to pin voltage	30V (short term) 10V (continuous)
Pin to case voltage	100V

TYPICAL AMPLITUDE RESPONSES






0
-10
-20
-30
-40
-50
-60
Loss (dB)
SW170
28
30
32
34
36
38
40
42
44
Frequency (MHz)
Plessey
0
-10
-20
-30
-40
-50
-60
Loss (dB)
SW173
28
30
32
34
36
38
40
42
44
Frequency (MHz)
Plessey


0
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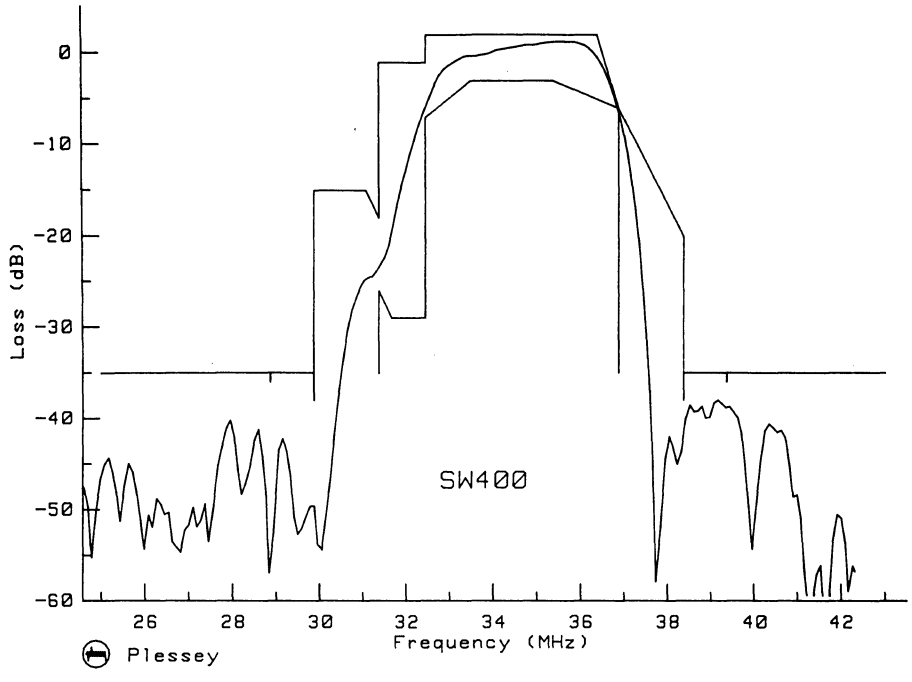
-20
-30
-40
-50
-60
Loss (dB)
SW200
36
38
40
42
44
46
48
50
52
Frequency (MHz)
Plessey
0
-10
-20
-30
-40
-50
-60
Loss (dB)
SW250
26
28
30
32
34
36
38
40
42
44
Frequency (MHz)
Plessey


0
-10
-20
-30
-40
-50
-60
Loss (dB)
SW400
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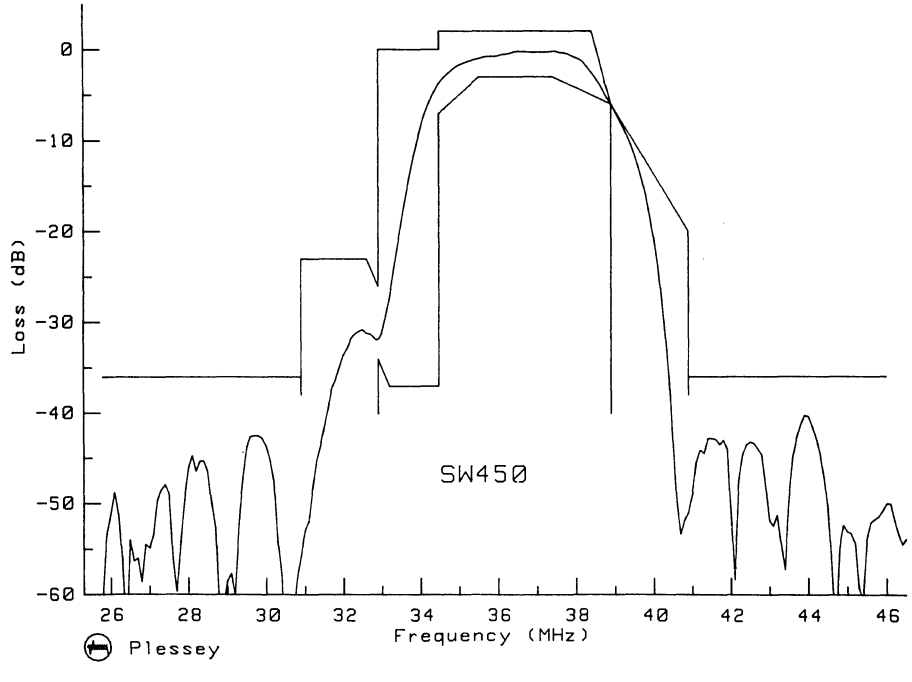
28
30
32
34
36
38
40
42
Frequency (MHz)
Plessey


0
-10
-20
-30
-40
-50
-60
Loss (dB)
SW450
26
28
30
32
34
36
38
40
42
44
46
Frequency (MHz)
Plessey

TBA120S

LIMITING IF AMPLIFIER/FM DETECTOR

The TBA120S is a symmetrical 8-stage limiting amplifier with a symmetrical coincidence demodulator and remote DC volume control. The circuit is especially suited for the sound IF section of TV receivers and for FM/IF amplification/demodulation in FM radio receivers.

An auxiliary circuit, consisting of a transistor with free base and collector and a 12V Zener diode, is also incorporated on the chip. The transistor can be used as an AF preamplifier (I_C<5mA) or as a bass/treble switch using voltage-controlled on/off switching of an R-C circuit.

The Zener diode can be used to stabilize the chip supply voltage or that of other circuits in the system (I_Z<15mA).

The TBA120S is supplied in two group variants, with volume as the parameter. A decrease in volume of 30 dB requires a resistor between pin 5 and earth with a value depending on the group number as shown in the following table. The group number is printed on the package.

Group	III	IV
R_5(kΩ)	2.1–2.5	2.4–2.9

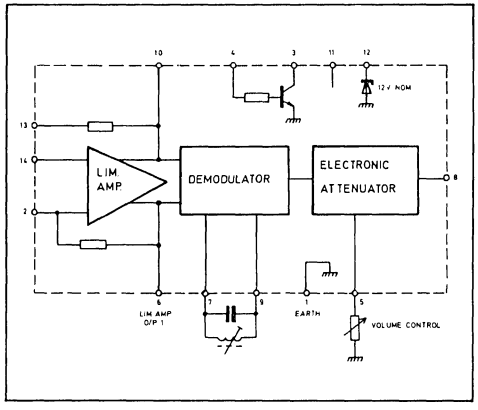


Fig. 2 SBA120S block diagram

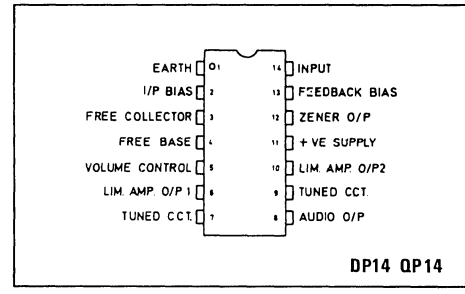


Fig. 1 Pin connections

FEATURES

- Outstanding Limiting Qualities
- High AM Suppression
- Wide Supply Voltage Range
- Low External Component Count

APPLICATIONS

- TV Sound Systems
- FM Radio Receivers
- FM Tuners

QUICK REFERENCE DATA

- Supply Voltage: +12V (Typ.)
- Operating Frequency: Up to 12MHz
- Current Consumption: 14mA (Typ.)
- IF Voltage Gain: 68dB (Typ.)
- AF Output Voltage: 1.1V r.m.s. (Typ.)
- Volume Control Range: 70dB (Typ.)
- Second Source Availability

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{CC} = +12V
T_A = +25°C
f = 5.5MHz
Δf = ±50kHz
f_{mod} = 1kHz

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Amplifier/demodulator						
Frequency range	f	0		12	MHz	
IF voltage gain V_6/V_{14}	G_V		68		dB	
IF output voltage	V_{opp}		250		mV	Limiting each output
AF output voltage	V_{AF}		1.1		V r.m.s.	V_i=10mV, Q=45, K=4%
			0.55		V r.m.s.	V_i=10mV, Q=20, K=1%
Input voltage at start of limiting	V_{lim}		30	60	μV	Q=45
Input impedance	Z_i	15/6	40/4.5		kΩ/pF	
Output resistance (pin 8)	R_O		2.6		kΩ	
Volume control range	$\frac{V_{AF\ max}}{V_{AF\ min}}$		70		dB	
DC component of o/p signal	V_8		7.3		V	V_i=0
AM suppression	a_{AM}	45	55		dB	V_i=500μV, m=30%
Potentionmeter resistance	R_5					
−1dB down			3.7	4.7	kΩ	
−70dB down		1.0	1.4		kΩ	
Control voltage	V_5					
−1dB down			2.4	2.6	V	
−70dB down			1.3		V	
Total current requirement	I_{cc}	10	14	18	mA	R_5 = ∞
		12	16	20	mA	R_5 = 0
Auxiliary circuit						
Zener voltage	V_{12}	12.5	13.5	14.5	V	I_{12} = 5mA
Zener resistance	R_z		30		Ω	
Transistor breakdown voltage	BV_{CEO}	13			V	I_4=0, I_3=500μA
Current gain	h_{FE}	30			−	I_3=1mA

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}:	18V
Operating temperature	−10°C to +70°C
Storage temperature	−25°C to +125°C
Total power dissipation, P_{tot}	
Continous:	400mW
Max. 1 min:	500mW
Zener current, I_{12}	
Continuous:	15mA
Max. 1 min:	20mA
Volume control voltage, V_5:	4V
Collector current, I_3:	5mA
Current I_4:	2mA
Shunt resistance $R_{13/14}$:	⩽ 1kΩ

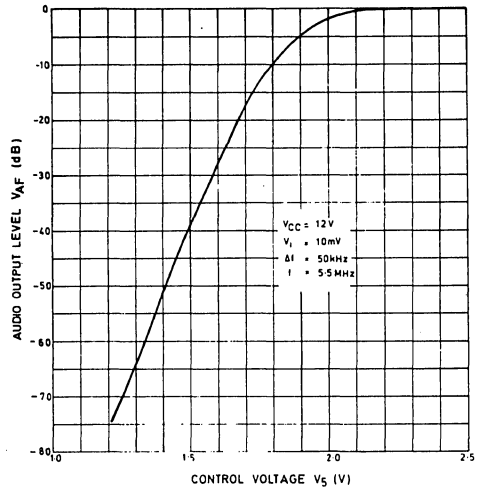


Fig. 3 Volume control voltage characteristic

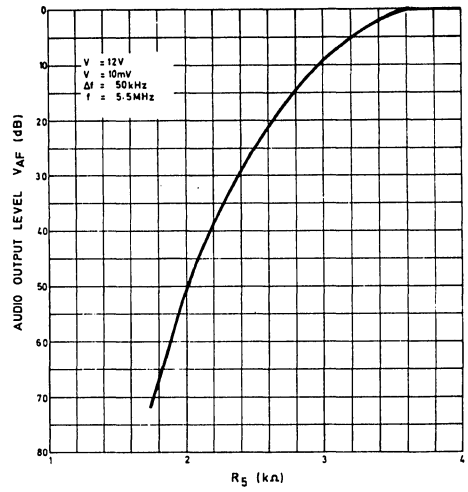


Fig. 4 Volume control resistance characteristic

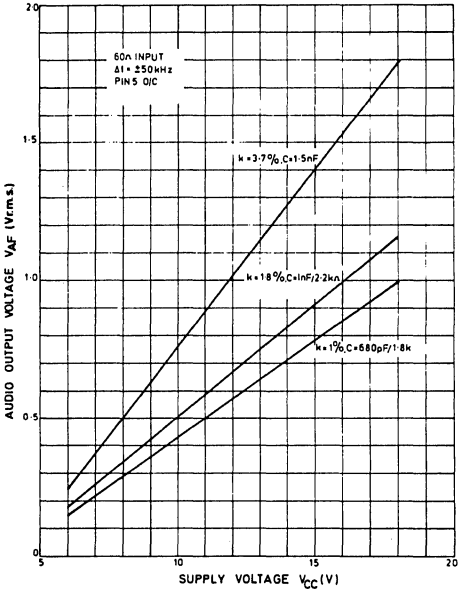


Fig. 5 Audio output v. supply voltage

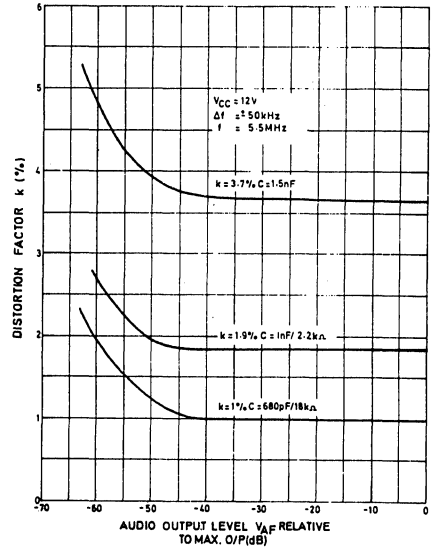


Fig. 6 Distortion factor (k) as a function of audio output voltage V_{AF}

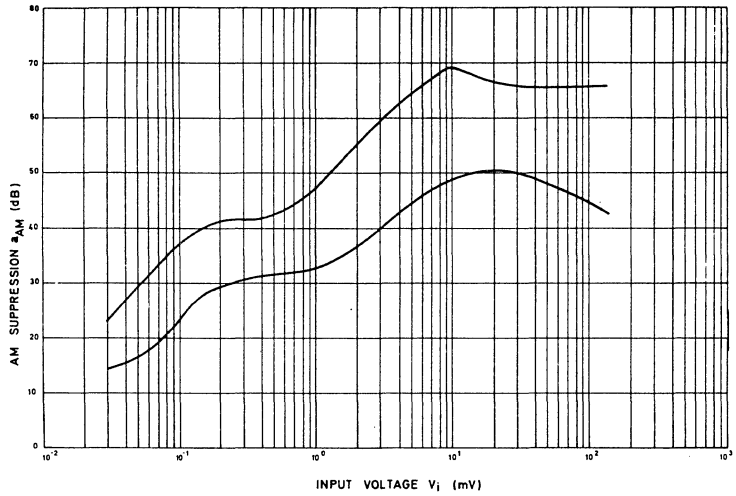


Fig. 7 AM suppression characteristics

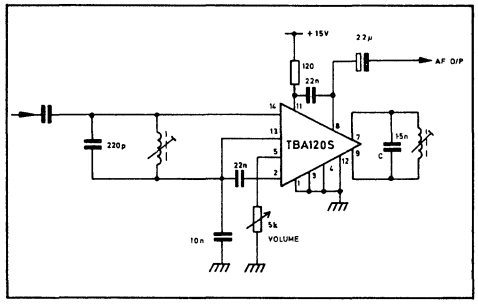
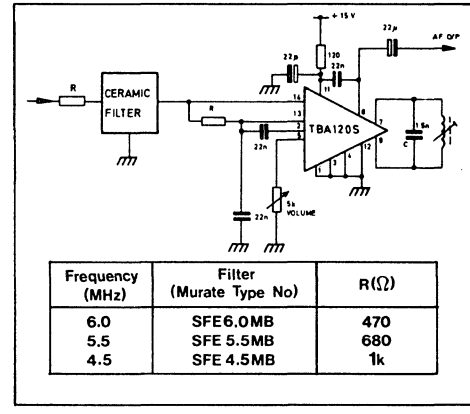


Fig. 8 Recommended application circuit, 5.5MHz



Frequency (MHz)	Filter (Murate Type No)	R(Ω)
6.0	SFE6.0MB	470
5.5	SFE 5.5MB	680
4.5	SFE 4.5MB	1k

Fig. 9 Application circuit using ceramic filter. (For good selectivity, the ceramic filter should be combined with an LC circuit.) ▷

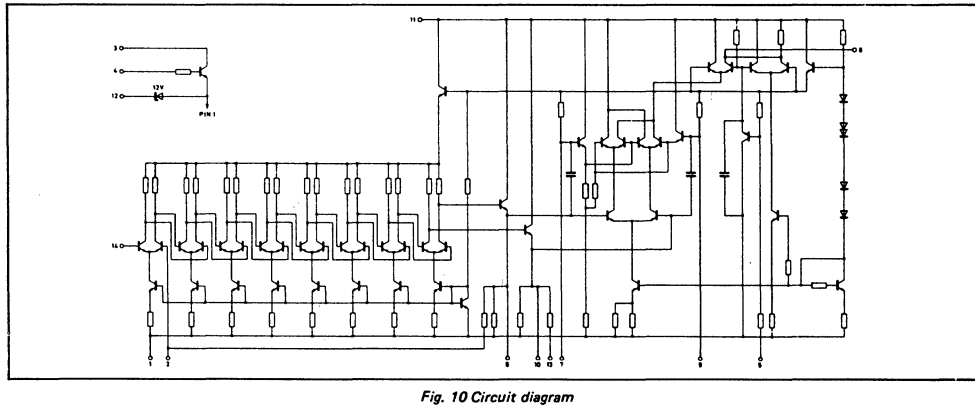


Fig. 10 Circuit diagram

TBA 120T TBA 120U

FM IF AMPLIFIER AND DEMODULATOR

The TBA120T and TBA120U are symmetrical 8-stage limiting amplifiers with symmetrical coincidence demodulator and remote DC volume control. The circuits are especially suitable for the sound IF section of TV receivers and for FM/IF amplification/demodulation in FM radio receivers. An additional audio output is provided at constant level (before the volume control) for the connection of video recorders and headphones, together with an audio input for video recorder playback.

The audio output voltage is at constant level with supply voltages between 10 and 18V and is of the same level as the TBA120S operating from a 15V supply.

The devices are insensitive to supply voltage hum, and there is therefore little need for smoothing capacitors.

FEATURES

- Outstanding Limiting Qualitites
- High AM Suppression
- Wide Supply Voltage Range
- Low External Component Count
- Low Intermodulation due to IF Voltage
- No Selection for Volume Control Characteristic Necessary
- Designed for use with Ceramic Filters (TBA120T only)

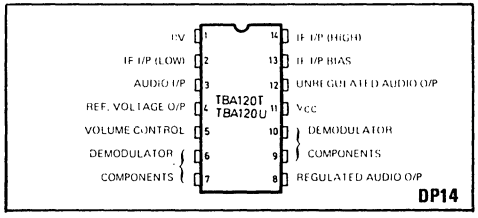


Fig. 1 Pin connections

APPLICATIONS

- TV Sound Systems
- FM Radio Receivers
- FM Tuners

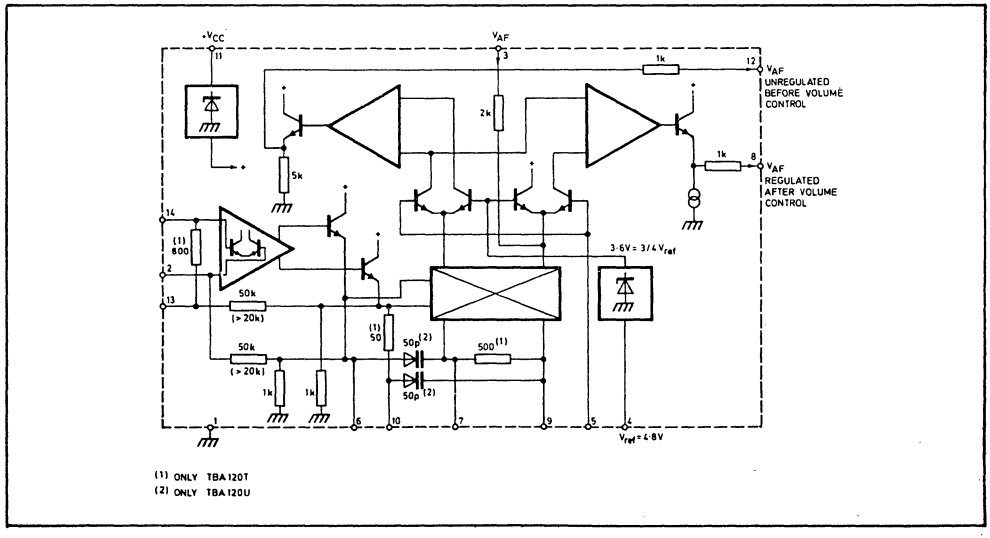


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

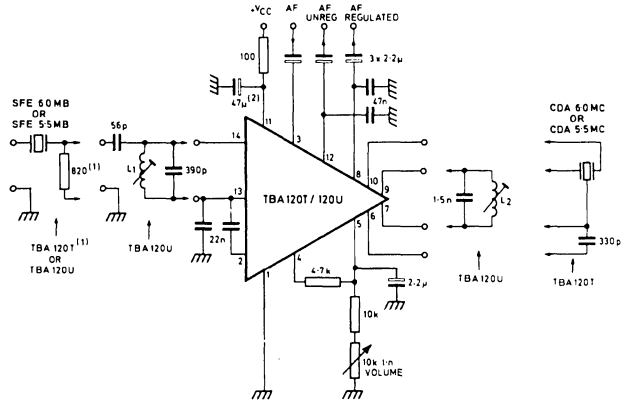
Test conditions (unless otherwise stated):
V_{CC} = 12V
T_{amb} = +25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Total current consumption	I_{CC}	9.5	13.5	17.5	mA	
IF voltage gain V_6/V_{14}	G_V		68		dB	f_{IF} = 5.5 MHz
Output voltage with limiting at each output			250		mVp-p	
Output impedance Pin 8	R_8		1.1		kΩ	
Pin 12	R_{12}		1.1		kΩ	
Input impedance	R_3		2		kΩ	
Internal impedance	R_4		12		Ω	
DC level of output signal (V_{in} = 0)	V_8		4		V	V_{in} = 0
	V_{12}		5.6		V	
Stabilized voltage	V_4	4.2	4.8	5.3	V	
Residual IF voltage without deemphasis	V_8		20		mV	
	V_{12}		30		mV	
AF gain (AF not regulated)	V_8/V_3		7.5			
Regulation at certain ratio of divider	$V_{AF/8}$	20	28	36	dB	R_{4-5} = 5kΩ, R_{5-1} = 13kΩ
Range of volume control (referred to pin 8)	$\frac{V_{AFmax}}{V_{AFmin}}$	70	85		dB	
Resistance (see note 1)	R_{4-5}	1		10	kΩ	
Input voltage for limitation	V_{inlim}		30	60	μV	f_{IF} = 5.5 MHz, Δf = ± 50kHz, f_{mod} = 1kHz
Hum suppression	V_8/V_{11}		35		dB	
	V_{12}/V_{11}		30		dB	
TBA 120T only:						
Input impedance	Z_{in}		800//5		Ω//pF	f_{IF} = 5.5 Mhz
AM suppression	a_{AM}	50	60		dB	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 500μV, f_{mod} = 1kHz, m = 30%
AF output voltage	V_8	650	900		mV	f_{IF} = 5.5 MHz, Δf = ±50kHz,
	V_{12}	400	650		mV	f_{mod} = 1kHz
TBA 120U only:						
Input impedance	Z_{in}	15//6	40//4.5		kΩ//pf	f_{IF} = 5.5 MHz
AM suppression	a_{AM}	50	60		dB	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 500μV, f_{mod} = 1kHz, m = 30%
AF output voltage	V_{8eff}	850	1200		mV	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 500μV, f_{mod} = 1kHz,
	V_{12eff}	600	1000		mV	$Q_8 \approx 45$, k = 4%
Harmonic distortion	k		1		%	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 10mV, f_{mod} = 1kHz, $Q_8 \approx 20$

NOTE
1. If DC volume control is not used, pin 4 must be connected direct to pin 5.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	18V	Reference voltage O/P current, I_4	5mA
Operating ambient temperature, T_{amb}	−10 to +65°C	IF input resistance, R_{13-14} (TBA120U)	⩽ 1kΩ
Storage temperature, T_{stg}	−55 to +125°C	Range of supply operation, V_{CC}	10 to 18V
Total power dissipation, P_{tot}	400mW	Frequency range, f	0 to 12 MHz
Volume control voltage, V_5	6V		



NOTES
1. This 820Ω resistor is not necessary for the TBA120T, when using the SFE 5.5MB
2. Omitting the 47µF capacitor on pin 11 changes volume control range
3. L1: $Q_0 \approx 73$
4. L2: $Q_0 \approx 40$

Fig. 3 Recommended application circuit

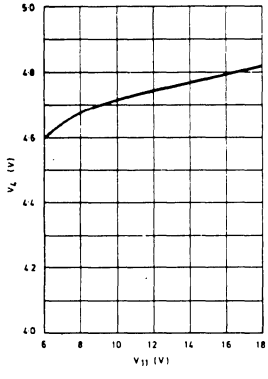


Fig. 4 Z voltage v. supply voltage

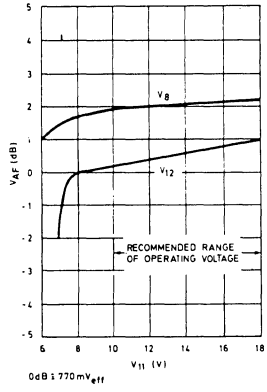


Fig. 5 AF output voltage v. supply voltage

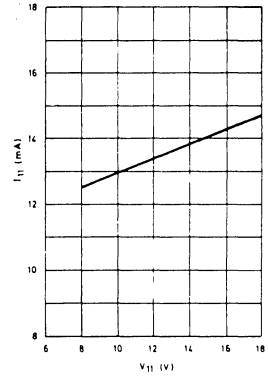
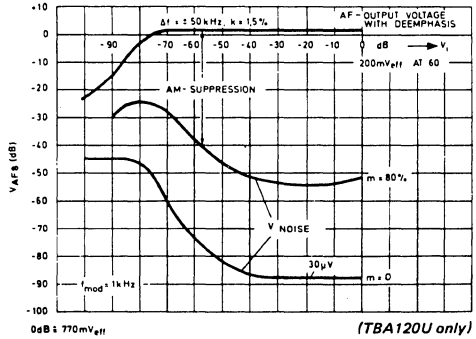
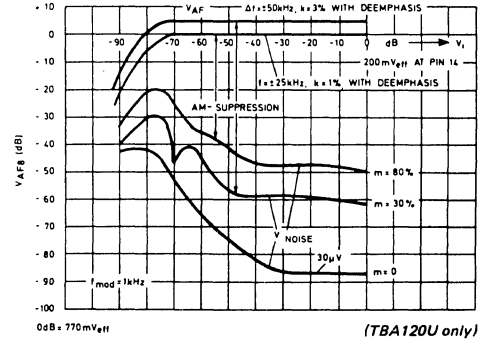


Fig. 6 Total current consumption v. supply voltage



(TBA120U only)

Fig. 7 AF output voltage and noise voltage v. input voltage (input Murata SFE 5.5MB)



(TBA120U only)

Fig. 8 AF output voltage and noise voltage v. input voltage (input 60Ω impedance, broadband)

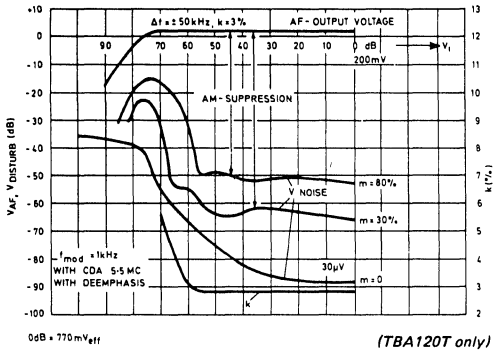


Fig. 9 AF output voltage (pin 8), noise voltage and harmonic distortion v. input voltage.

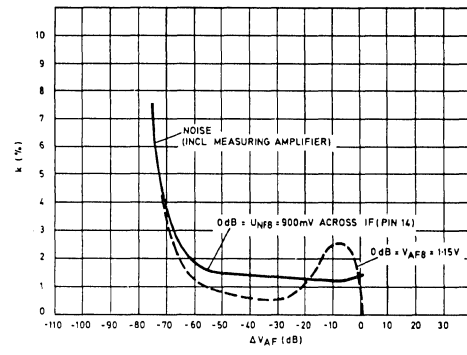


Fig. 10 Harmonic distortion v. volume control

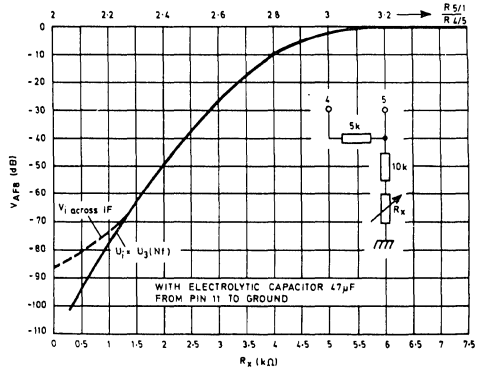


Fig. 11 AF output voltage (pin 8) v. potentiometer resistance and v. ratio of resistances

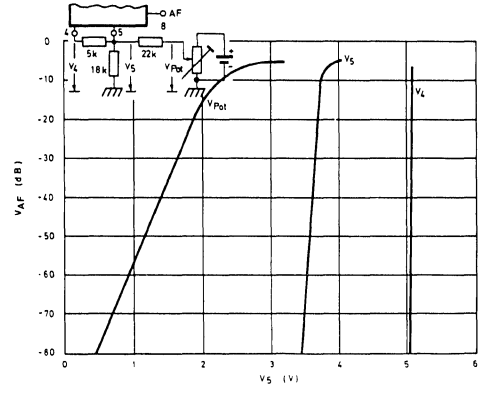
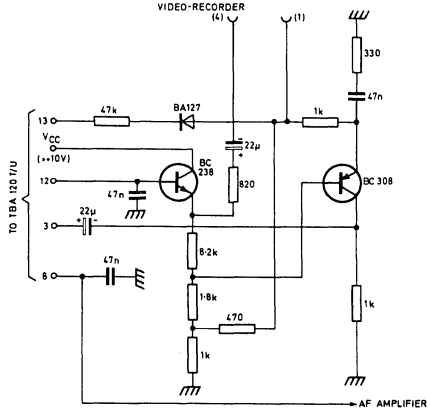


Fig. 12 AF output voltage (pin 8) v. voltage feeding into pin 5 V_{IRF} = 60mV$_{eff}$, f_{IF} = 5.5 MHz, Δf = ±50kHz, f_{mod} = 1kHz, V_{CC} = 18V



Function:

When switching voltage applied, the emitter follower (BC238) on the output is blocked and the buffer stage (BC308) is switched on. It includes a pre-emphasis to balance the de-emphasis at the AF output. The IF amplifier is put out of operation by the diode, BA127, and the 47kΩ resistor. The remote controllable volume regulator in the TBA120T/U is used for recording and playback.

SOCKET (1): SWITCHING VOLTAGE: FOR PLAYBACK +12 V
FOR INPUT NC
SOCKET (4) SIMULTANEOUS INPUT AND OUTPUT FOR AF

Fig. 13 Circuit for direct connection to video recorders

TBA 440 N/P

VIDEO IF AMPLIFIER DEMODULATOR

The TBA440 (TBA440N for NPN tuners, TBA440P for PNP tuners) comprises a high-gain regulated video IF amplifier, a controlled demodulator and two low-resistance video outputs with positive and negative signal as well as the complete key control and delayed tuner control.

ABSOLUTE MAXIMUM RATINGS

Supply voltage steady	15V
transitory	16.5V
Voltage at pin 5	20V
Voltage at pin 4	5V
Voltage at pin 14	5V
Operating ambient temperature	-10° to $+60^{\circ}C$
Total power dissipation at $T_{amb} \leqslant 55^{\circ}C$	700mW
Ohmic resistance between pins 8 and 9	20Ω

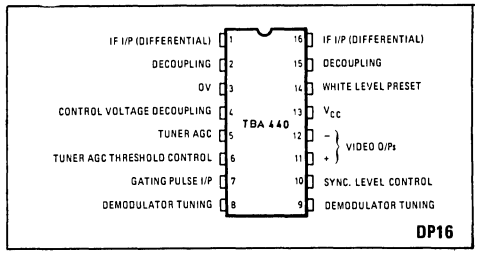


Fig. 1 Pin connections

FEATURES

- Complete Video IF in one IC
- High Sensitivity
- Positive and Negative Video Signals
- Gated AGC and Delayed AGC for Tuner
- White and Black Levels Separately Adjustable
- Ability to Control PIN Diode Attenuators

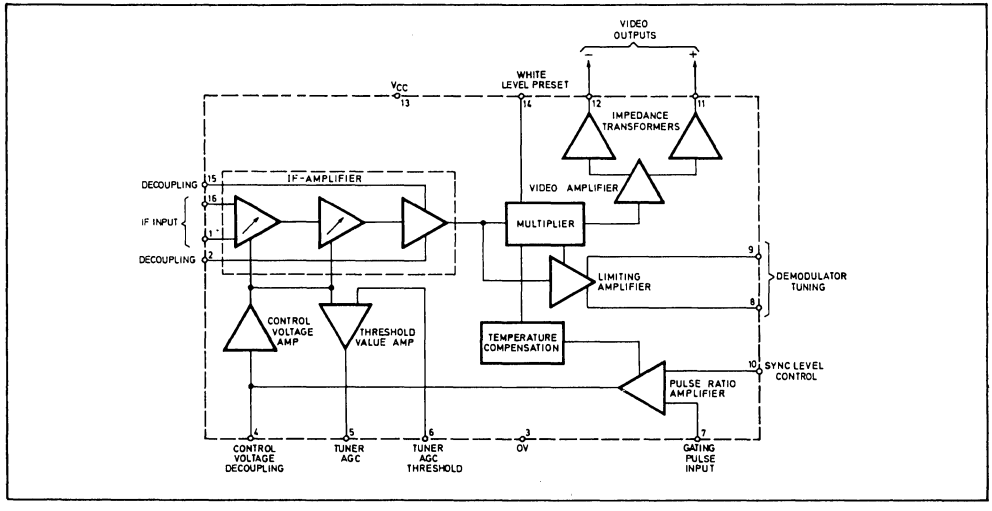


Fig. 2 TBA440 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C
V_{CC} = +13V
Reference point is pin 3 (0V)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}	13	10.5	13	15	V	
Current consumption	13	28	40	52	mA	V_{CC} = 15V
DC output voltage	11	4.1	5.1	6.1	V	V_{in} = 0V, $R_{14} = \infty$
	11		6.2		V	V_{in} = 0V, R_{14} = 0
	12	0 5	1.1	1.8	V	V_{in} = 0V, $R_{14} = \infty$
	12		2.5		V	V_{in} = 0V, R_{14} = 0
White level deviation						
$\Delta V_{11}/\Delta V_{13}$	11, 13		0.15			
$\Delta V_{12}/\Delta V_{13}$	12, 13		0.05			
Resistance R_{14-3} for ΔV_{11} = 1V	14 3		1		kΩ	
AGC threshold V_{10} = sync pulse level for R_{10-11} = 0	10,11		1.2		V	$V_{10} = V_{11}$
Regulating slope R_{10-11}/V_{11}	10, 11		4.5		kΩ/V	
Sync. pulse level with async. or without gating pulses	11		0.2		V	
Control current for tuner pre amp.	5	10	15		mA	$V_5 > 2V$, 10dB after AGC (TBA440P) 10dB before AGC (TBA440N)
IF control voltage for max gain	4	0		0.5	V	
for min gain	4	2.5		5	V	
Gating pulse voltage	7	−2		−5	V	
Residual IF voltage	11, 12		50		mV	
Output current to earth	11, 12			5	mA	
Output current to V_{13}	11, 12			−1	mA	
Input impedance at max gain	1		1.8//2		kΩ//pF	
at min gain	1		1.9//0		kΩ//pF	
Input voltage for V_{11} = 3V p-p	1		100		μV	Input 60Ω via 3:5 transformer
Video bandwidth			7		MHz	
AGC range		52	58		dB	
Intermodulation			55		dB	Input 0.3 to 1.5V p-p

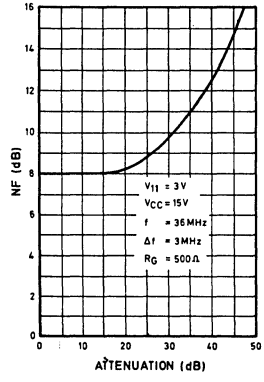


Fig. 3 Noise figure v. attenuation (measured at video frequency)

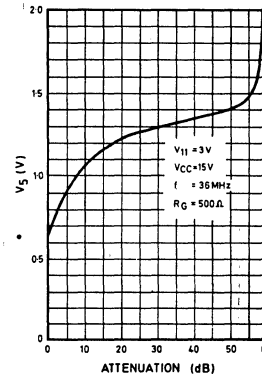


Fig. 4 Control voltage v. attenuation

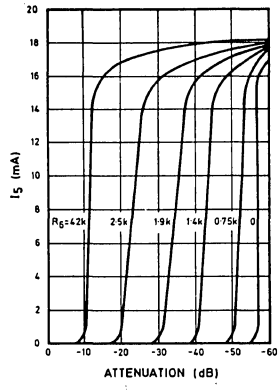


Fig. 5 Tuner control current v. attenuation with R_6 as parameter (TBA440P)

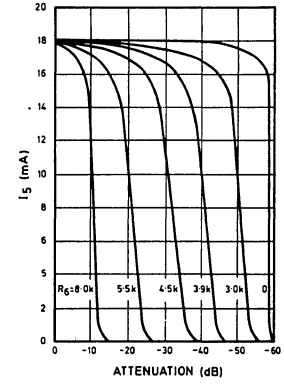


Fig. 6 Tuner control current v. attenuation with R_6 as parameter (TBA440N)

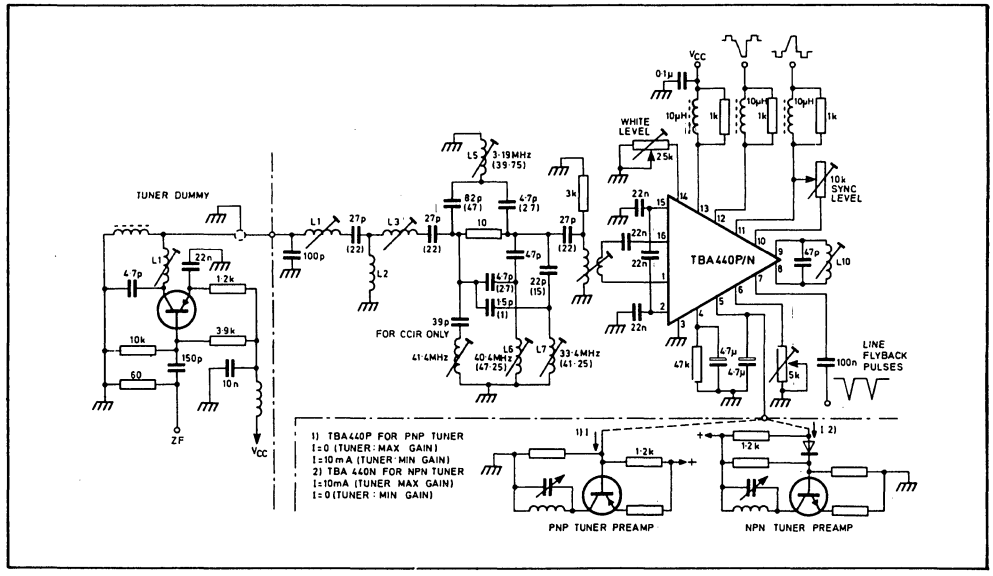


Fig. 7 IF application with TBA440P or TBA440N for CCIR standard (values in brackets for U.S. standard)

TBA530

RGB MATRIX PRE-AMPLIFIER

The TBA530 is an integrated R–G–B matrix pre-amplifier for colour television receivers incorporating a matrix pre-amplifier for R–G–B cathode or grid drive of the picture tube without clamping circuits. The chip layout has been designed to ensure tight thermal coupling between all transistors in each channel to minimise thermal drifts between channels. Also, each channel follows an identical layout to ensure equal frequency behaviour of the three channels.

This integrated circuit has been designed to be driven from the TBA520 synchronous demodulator integrated circuit.

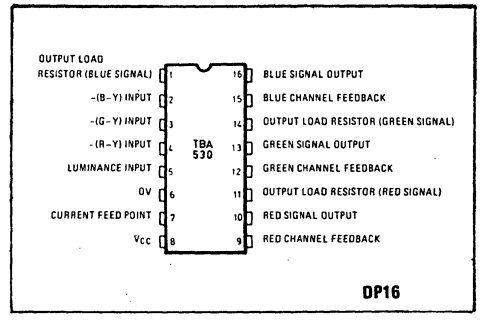


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	13.2V
Supply currents:–	
$I_1 = I_{11} = I_{14}$ max	10mA
$I_{10} = I_{13} = I_{16}$ max	50mA*
Total power dissipation at $T_{amb} = 60°C$, P_{TOT}	400mW*
Storage temperature	–55 to +125°C
Operating ambient temperature	–10 to +60°C

At increased voltages due to external failures (e.g., collector-base breakdown in the output transistors) a maximum current of 50mA is permitted between pins 16 and 8, 13 and 8, 10 and 8. The maximum permissible power dissipation is then 500mW.

QUICK REFERENCE DATA

- Supply Voltage (Nominal) 12V
- Total Supply Current (Nominal) 30mA
- Operating Ambient Temperature Range –10 to +60°C
- Gain of Luminance and Colour-difference Channels (Typ.) 100

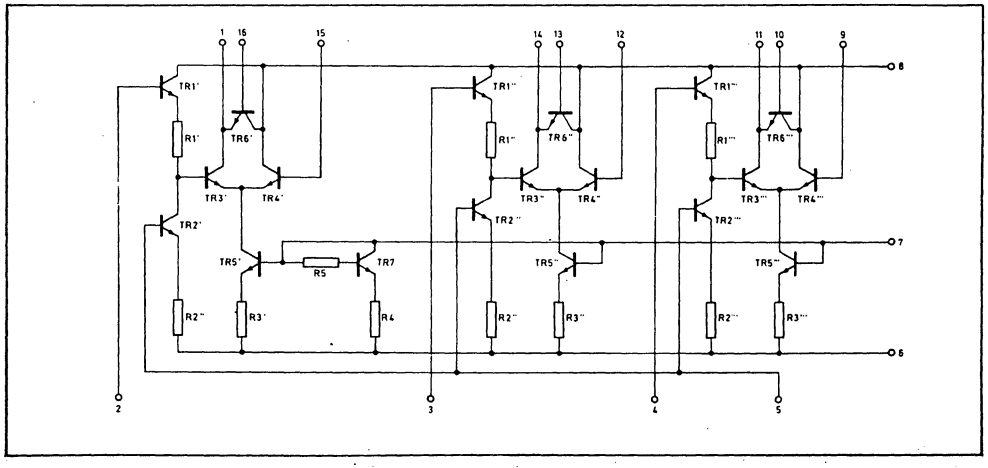


Fig. 2 TBA530 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):–

V_{CC} = +12V, T_{amb} = +25°C

Black level: $V_{R-Y} = V_{G-Y} = V_{B-Y} = 7.5V$

V_Y = 1.5V

Reference = pin 6

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Gain of colour channels (B–Y, G–Y, R–Y)	G_2		100		–	
	G_3		100		–	f = 0.5MHz (see note 1)
	G_4		100		–	
Ratio of gain of luminance amplifier to colour amplifiers		0.9		1.1	–	
DC output voltages	V_R		140		V	
	V_G		140		V	See note 2
	V_B		140		V	
Input resistance of colour difference amplifiers	R_2		60		kΩ	
	R_3		60		kΩ	f = 1kHz
	R_4		60		kΩ	
Input capacitance of colour difference amplifiers	C_2		3		pF	
	C_3		3		pF	f = 1MHz
	C_4		3		pF	
Input resistance of luminance amplifier	R_5		20		kΩ	f = 1kHz
Input capacitance of luminance amplifier	C_5		10		pF	f = 1MHz
3dB bandwidth of all channels	B		6		MHz	
Total current drain	I_{TOT}		30		mA	

NOTES

1. G is defined as the voltage ratio between the input signals at the pins 2, 3, 4 and the output signals at the collectors of the output transistors.
2. At the collectors of the output transistors. The value of this voltage is also dependent on the external circuitry.

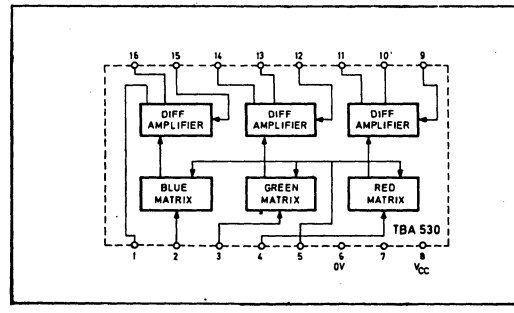


Fig. 3 TBA530 circuit diagram

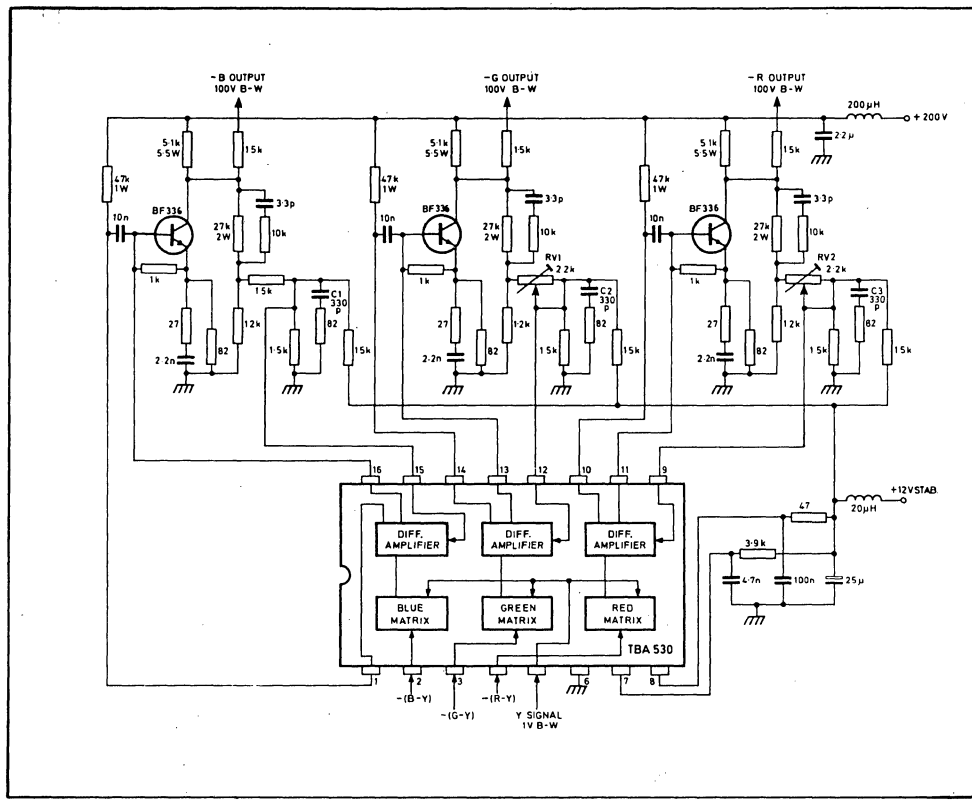


Fig. 4 Typical application diagram

FUNCTIONAL DESCRIPTION

Pin

1. Output load resistor, blue signal
   (Also pins 11 and 14 for red and green signals respectively.) Resistors (47kΩ, 1W) connected to +200V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by the IC and the DC feedback and is approximately +8V. The maximum current which can be allowed at each of these pins is 10mA.
2. −(B−Y) input signal
   This signal is fed via a low-pass filter from the TBA520 demodulator IC (pin 7) having a DC level of about +7.5V. The input resistance for this pin is typically 60kΩ with an input capacitance of less than 5pF (similarly for pins 3 and 4).
3. −(G−Y) input signal
   The DC black level of this signal is about +7.5V. (See pin 2.)
4. −(R−Y) input signal
   The DC black level of this signal is about +7.5V. (See pin 2.)
5. Luminance signal input
   The DC level on this pin for picture black is +1.6V. The required signal amplitude is 1V black-to-white with negative-going syncs (or blanking) for cathode drive as shown. The input resistance at this pin is 20kΩ approximately with a capacitance of less than 15pF.
6. Negative supply (earth).
7. Current feed point
   A current of approximately 2.5mA is required at this pin, fed via a 3.9kΩ resistor from +12V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7nF is necessary.
8. Positive 12V supply
   Maximum supply voltage permitted, 13.2V. Current consumption approximately 30mA.
9. Red channel feedback (green channel, pin 12; blue channel, pin 15)
   The DC working points and gains of both the output stages and the IC amplifier stages are stabilised by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by setting correctly the DC levels of the colour difference signals produced by the TBA520 demodulator IC. The gains of the R−G−B output stages are adjusted to give the correct white points setting on the picture tube by adjusting the potentiometers in the feedback paths (RV1, RV2).
10. Red signal output (green and blue signal outputs on 13 and 16)
    These pins are internally connected with pins 11, 14 and 1 respectively via zener type junctions to give a DC level shift appropriate for driving the output transistor bases directly. To by-pass the Zener junctions at HF three 10nF capacitors are required.
11. Output load resistor, red channel (see pin 1).
12. Green channel feedback (see pin 9).
13. Green signal output (see pin 10).
14. Output load resistors, green channel (see pin 1).
15. Blue channel feedback (see pin 9).
16. Blue signal output (see pin 10).

OPERATING NOTES

Careful attention to earth paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon HF response of inevitable differences the compensating capacitors C_1 and C_2 and C_3 may be appropriately selected for any given board layout.

The signal black level at the collectors of the R−G−B output stages depends upon the +12V supply, the DC level of the colour difference signals from the TBA520 demodulator IC and the black level potential of the luminance signal applied to the TBA530 matrix IC. The DC levels of the signals produced and handled by the IC's are designed to have approximately proportional tracking with the 12V supply potential,

$$\text{i.e.,}\ \frac{\Delta V\ (\text{DC level, signal})}{\Delta V_{12V}} \simeq \frac{V_{nom}\ (\text{DC level, signal})}{12}$$

To ensure that changes in picture black level due to variations on the 12V supply to the IC's occur in a predictable way, all the IC's should be operated from a common supply line. This is specially important for the TBA520 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12V supply should have a stability of not worse than ±3% due to operational variations.

To reduce the possibility of patterning on the picture due to radiation of the harmonics of the products of the demodulation process, the leads carrying the drive signals to the picture tube should be as short as the receiver layout will allow. Resistors (typically 1.5kΩ connected in series with the leads and mounted close to the collectors of the output transistors provide useful additional filtering of harmonics.

TBA 540

REFERENCE COMBINATION

The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate ACC, colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

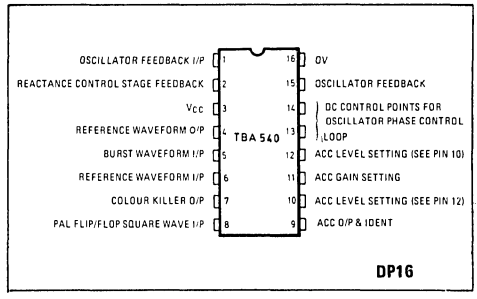


Fig. 1 Pin connections

QUICK REFERENCE DATA

- Supply Voltage, $V_{3\text{-}16}$: 12V (Nom.)
- Total Current Drain, I_3 : 38mA (Typ.)
- R-Y Ref. Output, $V_{4\text{-}16}$: 1.4Vpp (Typ.)
- Colour Killer Output, $V_{7\text{-}16}$
  Colour ON : 12V (Typ.)
  Colour OFF: 250mV (Max.)
- ACC Output Voltage, $V_{9\text{-}16}$:—
  at Correct Phase of PAL Switch : +0.2 to +4V
  at Incorrect Phase of PAL Switch : +4 to +11V

ABSOLUTE MAXIMUM RATINGS

Voltages are referred to pin 16

Electrical

Supply voltage V_3 (V_{CC})	13.2V
Total power dissipation at T_{amb} = +60°C	700 mW
Surge current, minimum duty cycle 10:1, I_{7max}	50mA

Temperature

Storage temperature, T_{stg}	−55°C to +125°C
Operating temperature, T_{amb}	−10°C to +60°C

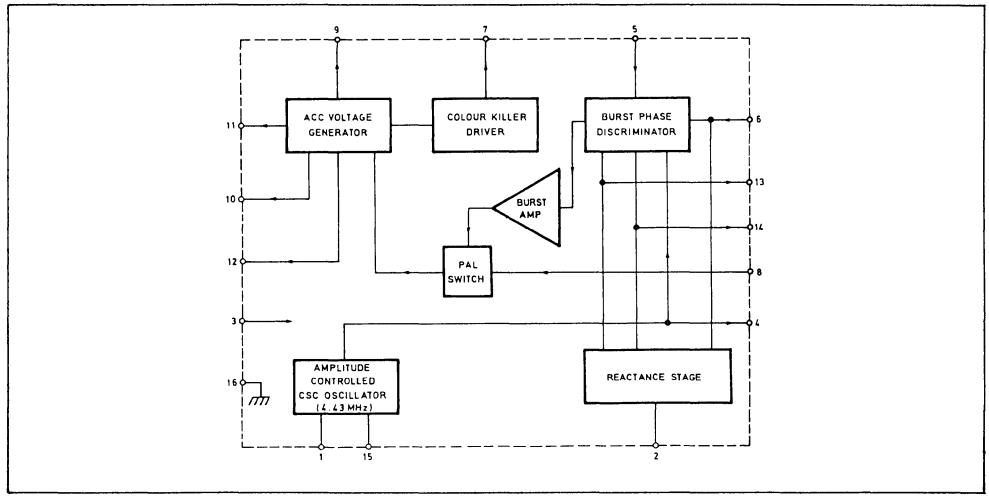


Fig. 2 TBA540 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} (V_3) = +12V, T_{amb} = +25°C, V_5 = 1.5Vp-p burst, V_8 = 2.5Vp-p PAL square wave.
Voltages referred to pin 16

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output Signals						
B-Y reference signal output	4	1	1.4	2	Vp-p	
Colour killer output	7					
colour 'on'			12		V	
colour 'off'			100	250	mV	
ACC output signal range	9					
at correct phase of PAL switch			+4 to +0.2		V	
at incorrect phase of PAL switch			+4 to +11		V	
Oscillator Section (Amplifier)						
Input resistance	15		3.5		kΩ	
Input capacitance	15		5		pF	
Voltage gain, $G_{15\text{-}1}$	15-1		4.7			
Reactance Control Section						
Voltage gain, $G_{15\text{-}2}$	15-2		1.3			Pins 13 and 14 interconnected
Rate of change of gain with phase difference between burst and reference signal, $\frac{\Delta G_{15\text{-}2}}{\Delta\phi 5\text{-}4}$	15-2		5		rad^{-1}	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Oscillator Feedback Output

The crystal receives its energy from this pin. The output impedance is approximately 2kΩ in parallel with 5pF.

2. Reactance Control Stage Feedback

This pin is fed internally with a sinewave derived from the reference output (pin 4) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12V Supply

The maximum voltage must not exceed 13.2V.

4. Reference Waveform Output

This pin is driven internally by the regenerated subcarrier waveform in B-Y phase. (The output is in B-Y rather than R-Y phase as the burst phase network produces a lag of 90° of the burst applied to pin 5.) An output amplitude of nominally 1.4V peak-to-peak is produced at low impedance. No DC load to earth is required. A DC connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-)B-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a DC blocking capacitor, is therefore necessary.

5. Burst Waveform Input

A burst waveform amplitude of 1.5V peak-to-peak is required to be AC coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this pin is approximately 1kΩ and a threshold level of 0.7V must be exceeded before the burst signal becomes effective. A DC bias of 400mV is internally derived for pin 5.

The absolute level of the tip of the burst at pin 5 will normally reach 1.5V.

6. Reference Waveform Input

This pin requires a reference waveform in the -(B-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A DC connection between pins 4 and 6 must be made via the transformer.

7. Colour Killer Output

This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typically 10kΩ) connected to +12V. The unkilled and killed voltages on this pin are then +12V and <250mV respectively. (The voltage range on pin 9 over which switching of the colour killed output on pin 7 occurs is nominally +2.5V.)

8. PAL Flip-Flop Square Wave Input

A 2.5V peak-to-peak square wave derived from the PAL flip-flop (in the TBA520 or TBA990 demodulator IC) is required at this pin, AC – coupled via a capacitor. The input impedance is about 3.3kΩ.

9. ACC Output

An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero burst input signal the DC potential produced at pin 9 is set to be +4V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at pin 9 is determined by the control characteristic of the ACC amplifier, i.e., for the TBA560 from 0.8 to 1V. The potential on pin 9 will fall to a value within this range as the burst input signal is stabilised to an amplitude of 1.5V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cut-off function in the TBA520 demodulator IC.

10. ACC Level Setting

The network connected between pins 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. ACC Gain Control

RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5V peak-to-peak) under ACC control.

12. See Pin 10.

13. See Pin 14.

14. DC Control Points in Reference Control Loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of DC balancing of the reactance stage and the connection of the bandwidth-determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

The filter network consists of R2, C2, C3 and C4. The DC potentials on these pins are nominally +6V.

15. Oscillator Feedback

The input impedance at this pin is nominally 3.5kΩ in parallel with 5pF. No DC connection is required on this pin. The voltage gain in the IC between pins 15 and 1 is nominally 4.7 times.

16. Negative Supply (earth).

OPERATING NOTES

Performance and Comments

Initial adjustment

(a) Remove burst signal.
(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1.
(c) Set the ACC level adjustment RV1, to give +4V on pin 9. Remove short circuit.
(d) Apply burst signal.
(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400Hz deviation of crystal frequency, ±10°.
(b) Typical holding range, ±600Hz. (c)
(c) Typical pull-in range ±300Hz.
(d) Temperature coefficient of oscillator frequency, only 2Hz/°C maximum.

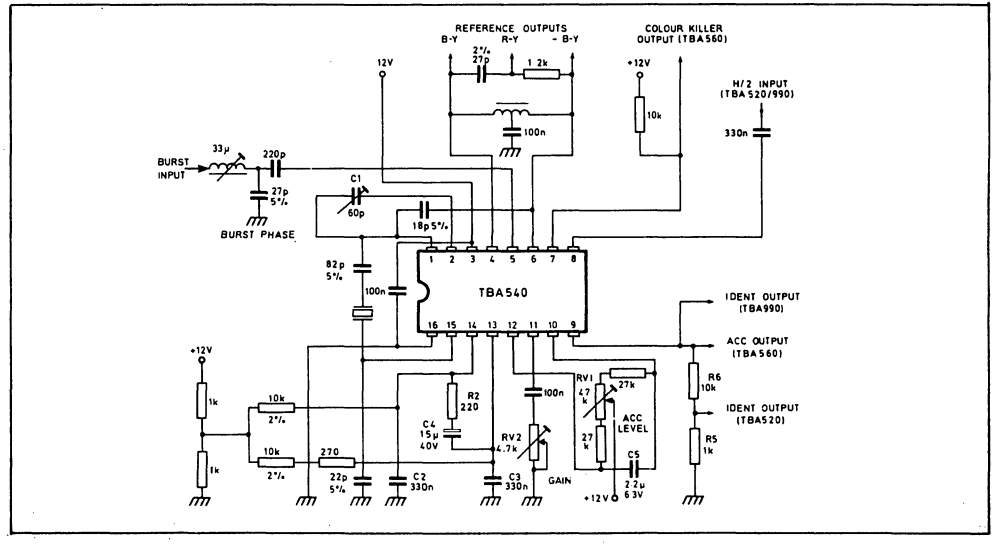


Fig. 3 Typical application diagram

TBA 560 C

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TBA560C is an integrated circuit for colour television receivers incorporating circuits for the processing and control of the luminance and chrominance signals. It can be used in conjunction with the TBA520 or TBA990, 530, 540, 550 and TCA800 integrated circuits.

The luminance part provides luminance delay line matching, DC contrast control, black level clamp circuit, brightness control and flyback blanking.

The chrominance part provides chroma amplification with ACC, DC chroma gain control which tracks with the contrast control, separate saturation control, burst gate, chroma signal flyback blanking colour killer and PAL delay line driver.

The TBA560C is not an equivalent of the TBA500 and 510 although it performs similar functions to those circuits.

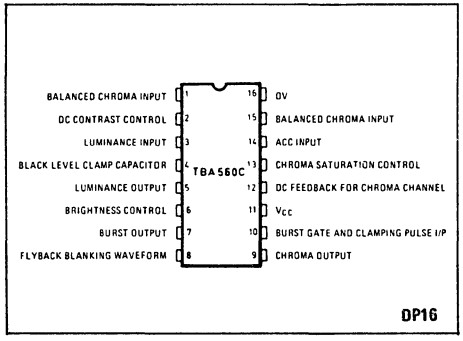


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Voltages are referred to pin 16

Electrical

V_{11} max.	Supply voltage (note 1)		13.2V
V_1	0 to +5V	V_{10} min.	−5V
V_2	0 to +12V (note 2)	V_{12}	−5 to +6V
V_4	0 to +6V	V_{13}	−3 to +6.5V (note 2)
V_6	0 to +3V	V_{14}min.	−5V
V_8	−5 to +5V	V_{15}	0 to +5V

Currents (positive when flowing into the integrated circuit)

I_1	0 to +1mA	I_9	−10 to 0mA
I_3	−1 to +3mA	I_{10}max.	+3mA
I_5	−5 to 0mA	I_{14}max.	+1mA
I_6	−1 to +1mA	I_{15}	0 to +1mA
I_7	−3 to +2mA		
P_{tot}max.	Total power dissipation T_{amb} = 60°C (note 1)		580mW

Temperature

Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

Notes

1. Permissible during receiver switch on transient V_{11}max. 16V, P_{tot}max. 700mW for t ⩾ 60sec.
2. V_2 and V_{13} must always be lower than V_{11}

QUICK REFERENCE DATA

- Supply Voltage (Nom.) (V_{11-16}) 12V
- Supply Current (Nom.) (I_{11}) 30mA
- Luminance Signal Input Current (Typ.) ($I_{3(p-p)}$) 0.4mA
- Luminance Output Signal at Nominal Contrast Setting (Typ.) and Input Current as Above ($V_{5-16(p-p)}$) 1V (See Note 1)
- Chrominance Input Signal (Min.) ($V_{1-15(p-p)}$) 4mV
- Chrominance Input Signal (Max.) $V_{1-15(p-p)}$) 80mV
- Chrominance Output Signal at Nominal Contrast and Saturation Setting (Typ.) ($V_{9-16(p-p)}$) 1V (See Note 1)
- Contrast Control Range ⩾20dB
- Saturation Control Range ⩾20dB
- Burst Output (Closed ACC Loop) (Typ.) ($V_{7-16(p-p)}$) 1V

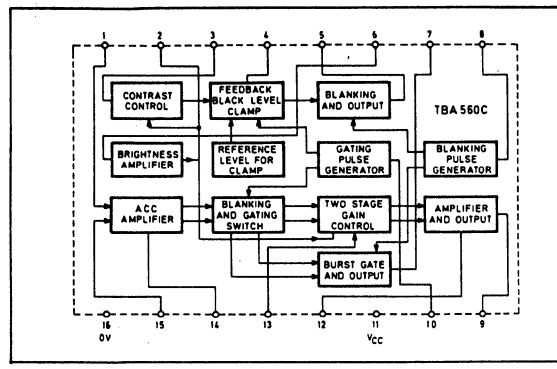


Fig. 2 TBA560C block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} = +12V, T_{amb} = +25°C test circuit = Fig. 6, voltages referred to pin 16

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}	11	10.8	12	13.2	V	
Required Input Signals						
Chrominance input signal, p-p value of colour bars with 75% saturation, V_{1-15}	1,15	4		80	mV p-p	
Luminance input current, black-to-white	3		0.4	1.5	mA p-p	
Contrast control voltage range for 20dB control	2	2	3.7	5.6	V	See note 1 and Fig. 3
Brightness control voltage for black level of 1.5V at O/P	6		1.3		V	See note 2 and Fig. 4
Saturation control voltage range 20dB control	13	2.7	4.4	6.2	V	See note 1 and Fig. 5
Flyback blanking pulse amplitude	8					
for 0V blanking level at pin 5		0	−0.5	−1	V pk	
for 1.5V blanking level at pin 5		−2	−2.5	−3	V pk	
Burst keying (back porch) pulse (+ve going)	10	0.05		3	mA pk	
Colour killer	13	0.5		1	V	
Automatic chrominance control starting level (−ve going)	14		1.2		V	See note 3
Obtainable Output Signals						
Luminance output voltage (black-to-white)	5		1	3	V p-p	I_3 = 0.4mA p-p, V_2 = 3.7V
Black level shift				100	mV	See notes 1 and 4
Burst signal amplitude	7		1		V p-p	
Chrominance signal at nominal contrast and saturation	9		1		V p-p	See note 1
3dB bandwidth of chrominance and luminance amplifier			5		MHz	
Change of ratio of luminance to chrominance				2	dB	Contrast control 10dB

NOTES
1. Nominal contrast or saturation = maximum value −6dB. Thus, the control is +6 to −14dB on the nominal.
2. When V_6 is increased to above 1.7V, the black level of the output signal remains at 2.7V.
3. A negative-going potential provides a 26dB ACC range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of 500mV min.
4. Black level shift is specified as that due to changes of contrast and video content at constant brightness setting.

FUNCTIONAL DESCRIPTION

1. Balanced Chroma Signal Input (in conjunction with pin 15)

This is derived from the chroma signal bandpass filter, designed to provide a push-pull input. An input signal amplitude of at least 4mV peak-to-peak is required between pins 1 and 15. Both pins require DC potential of approximately +3.0V. This is derived as a common mode signal from a network connected to pin 7 (burst output). In this way DC feedback is provided over the burst channel to stabilise its operation. All figures for the chrominance signal are based on a colour bar signal with 75% saturation; i.e., burst-to-chroma ratio of input signal is 1:2.

2. DC Contrast Control

With +3.7V on this pin, the gain in the luminance channel is such that a 0.4mA black-to-white input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 1V black-to-white. A variation of voltage on pin 2 between +5.6V and +2V gives a corresponding gain variation of +6 to >−14dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals. Beam current limiting can be applied via the contrast control network as shown in the peripheral circuit, when a separate overwind is available on the line output transformer.

3. Luminance Signal Input

This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and a DC blocking capacitor and requires to be about 0.4mA peak-to-peak amplitude. A DC bias current is required via a 12kΩ resistor to the +12V line.

4. Charge Storage Capacitor for Black Level Clamp

5. Luminance Signal Output

An emitter follower provides a low impedance output signal of 1V black-to-white amplitude at nominal contrast setting having a nominal black level in the range 0 to +2.7V. An external emitter load resistor is required, not less than 1kΩ. If a greater luminance output is required than 1V, with normal control settings, the input current swing at pin 3 should be increased in proportion.

6. Brightness Control

Over the range of potential +0.9 to +1.7V the black level of the luminance output signal (pin 5) is increased from 0 to +2.7V. The output signal black level remains at +2.7V when the potential on pin 6 is increased above +1.7V.

7. Burst Output

A 1V peak-to-peak burst (controlled by the ACC system) is produced here. Also, to achieve good DC stability by negative feedback in the burst channel the DC potential at this pin is fed back to pins 1 and 15 via the chroma input transformer.

8. Flyback Blanking Input Waveform

Negative going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than −1V negative excursion, or DC coupled pulses of similar amplitude whose negative excursion is at zero volts DC are applied, the signal level at the luminance output (pin 5) during blanking will be 0V. However, if the blanking pulses applied to pin 8 have an amplitude of −2 to −3V the signal level at the luminance output during blanking will be +1.5V. The negative pulse amplitude should not exceed −5V.

9. Chroma Signal Output

With a 1V peak-to-peak burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 1V peak-to-peak. An external network is required which provides DC negative feedback in the chroma channel via pin 12.

10. Burst Gating and Clamping Pulse Input

A positive pulse of not less than 50μA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync. pulse or picture line periods during normal operations of the receiver.

11. +12V Supply (V_{CC})

Correct operation occurs within the range 10.8 to 13.2V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 580mW at 60°C ambient temperature.

12. DC Feedback for Chroma Channel (see pin 9)

13. Chroma Saturation Control

A control range of +6dB to>−14dB is provided over a range of DC potential on pin 13 from 6.2 to 2.7V. Colour killing is also achieved at this terminal by reducing the DC potential to less than +1V, e.g., from the TBA540 colour killer output terminal. The minimum "kill factor" is 40dB.

14. ACC Input

A negative-going potential gives an ACC range of about 26dB starting at +1.2V. From 1V to 800mV the steepest part of the characteristic occurs, but a small amount of gain reduction also occurs from 800mV to 500mV. The input resistance is at least 50kΩ.

15. Chroma Signal Input (see pin 1)

16. Negative Supply, 0V (Earth)

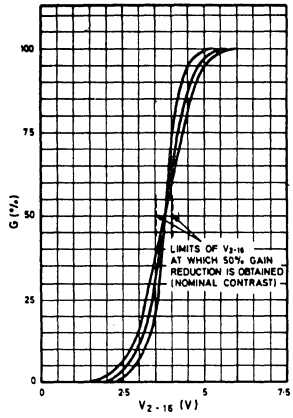


Fig. 3 Contrast control characteristic (luminance amplifier)

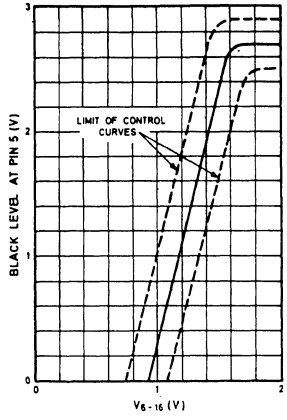


Fig. 4 Control of black level at output of luminance amplifier

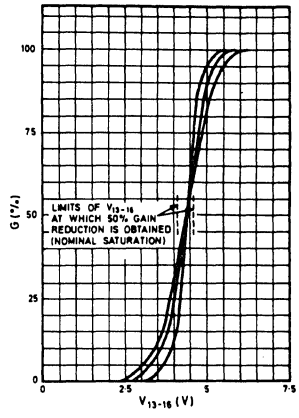


Fig. 5 Chrominance amplifier saturation characteristic

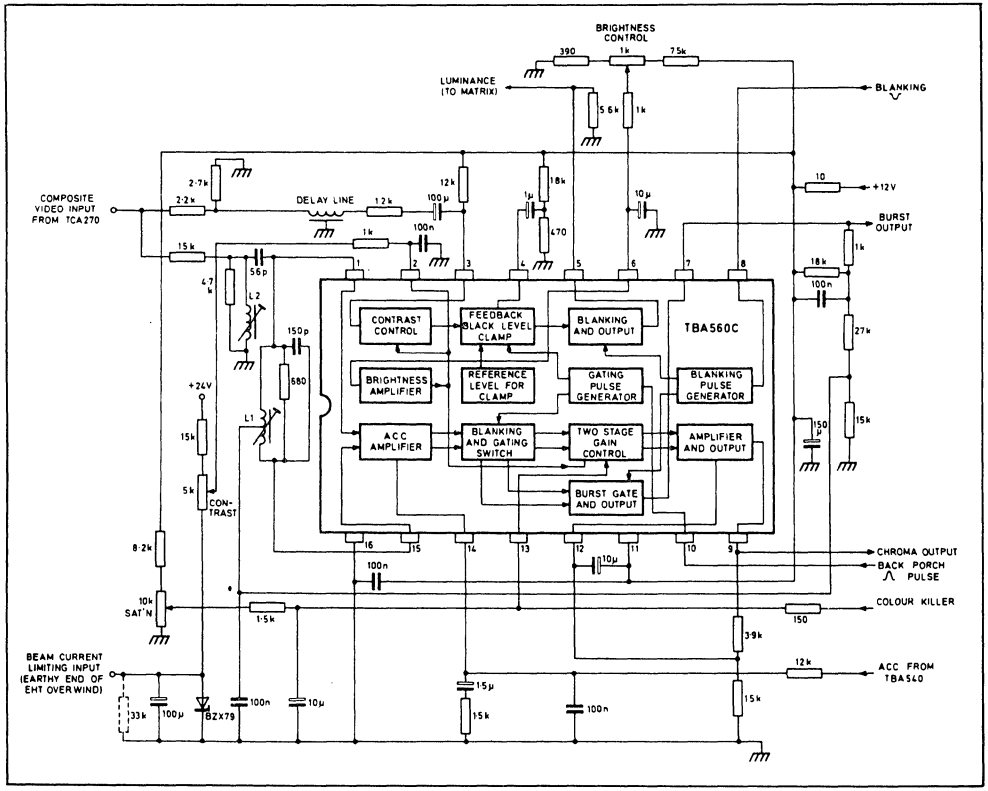


Fig. 6 Application diagram

TBA800

5W AUDIO AMPLIFIER

The TBA800 is a robust high efficiency audio amplifier especially designed for Television Receivers.

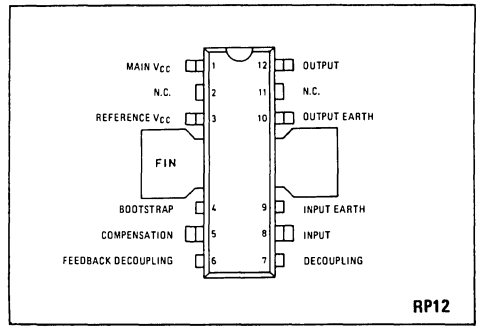


Fig. 1 Pin connections

FEATURES

- Wide Supply Voltage Range
- High Efficiency
- Low Cost
- Second Source Availability

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Pin 1 or 3 V_{CC}	30V
Peak load current	Pin 12	1.5A
Power dissipation		5W (case temp 90°C)
Operating temperature (with 25°C/W heat sink)		
		−10°C to +65°C
Junction temperature		150°C
Storage temperature		−25°C to +125°C

QUICK REFERENCE DATA

- Supply Voltage Range: 5 to 30V
- Efficiency at 4W: 70%
- Power Into 16Ω Load (V_{CC} = 24V): 5W

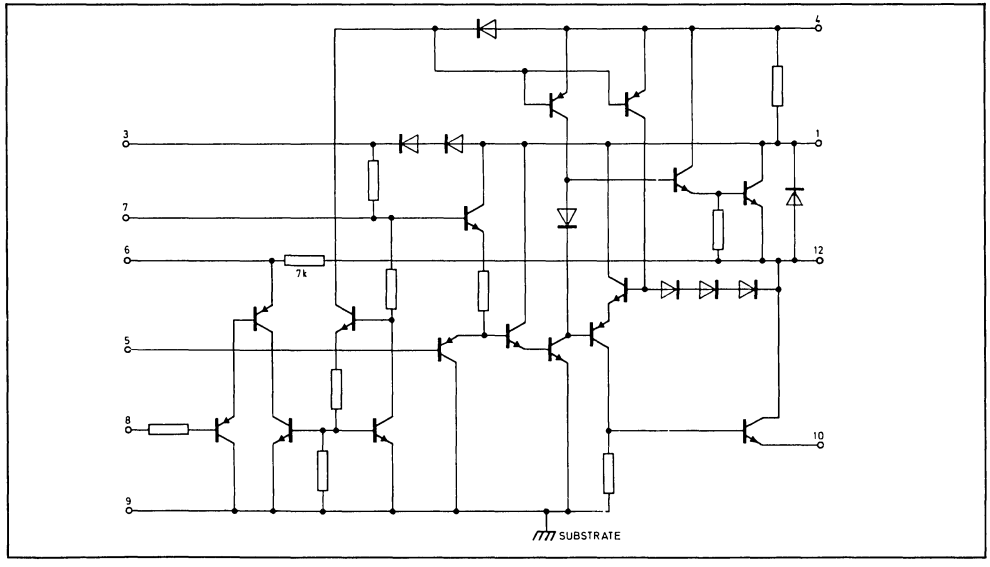


Fig. 2 TBA800 circuit diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = +25°C
V_{CC} = 24V Rf = 56Ω R_L = 16Ω frequency 1 kHz
Reference point is pin 9
Measurements made in typical application circuit, Fig. 8

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC}	1, 3	5	24	30	V	
Quiescent output voltage	12	11	12	13	V	
Quiescent current	1, 3		9	20	mA	
Input current	8		1	5	μA	
Output power	12	4.4	5		W	10% THD
Input voltage	8		80		mV	Output power 5W
Input impedance	8		5		MΩ	
3dB bandwidth			40 to 20k		Hz	
Total harmonic distortion	12		0.5		%	o/p power 50mW to 2.5mW
Open loop gain			70		dB	Rf = 0Ω
Closed loop gain		39	42	45	dB	Rf = 56Ω
Input noise voltage	8		5		μV	40Hz to 20kHz
Input noise current	8		0.2		nA	
Efficiency			70		%	Output power 4W
Thermal resistance				70	°C/W	Junction to ambient
				12	°C/W	Junction to *fin*

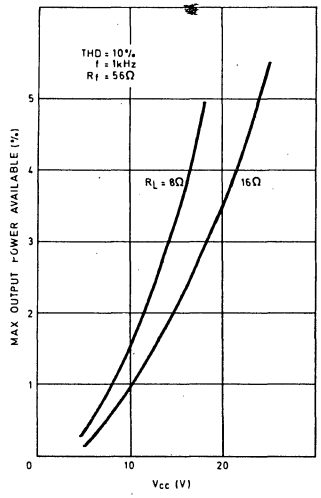


Fig. 3 Max. available output power v. supply voltage

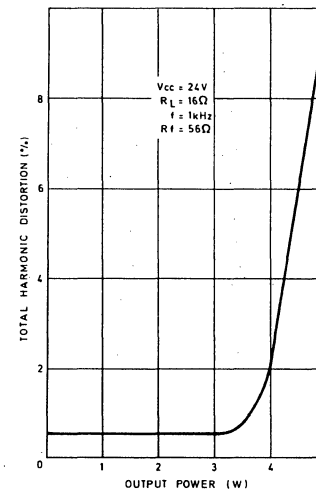


Fig 4 Total harmonic distortion v. output power

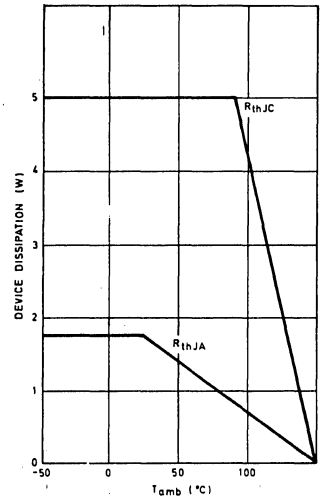


Fig. 5 Device power dissipation v. ambient temperature

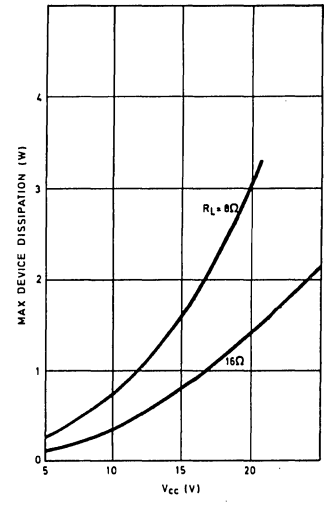


Fig. 6 Max. device power dissipation v. supply voltage

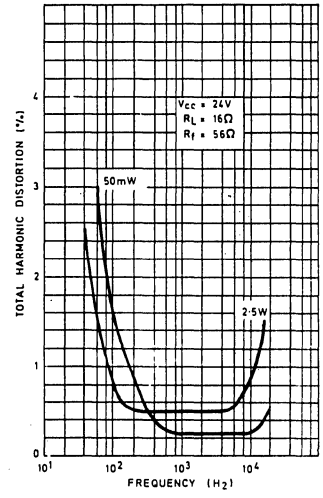
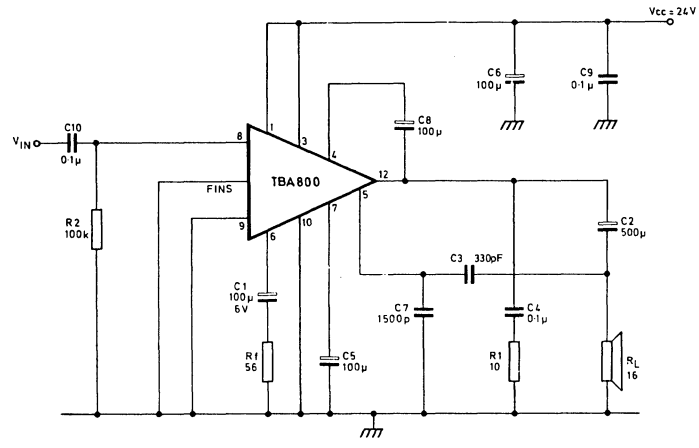


Fig. 7 Total harmonic distortion v. frequency



The supply voltage *must be disconnected* before inserting the integrated circuit into the socket.

Fig. 8 Typical application

APPLICATION NOTE

When using a supply of 10V or less, pin 3 should not be connected and the bootstrap capacitor C8 should be omitted.

TBA 920 TBA 920S

LINE OSCILLATOR COMBINATION

The TBA920 is a silicon integrated circuit designed for TV receiver applications. It accepts the composite video signal, separates sync. pulses with the added safeguard of noise gating and provides a sync. output for the vertical integrator. Also incorporated is the line oscillator together with two phase comparators: one to compare flyback pulses to the oscillator and the other for sync. phase comparison. The TBA920S is a special selection of the TBA920 (see Electrical Characteristics).

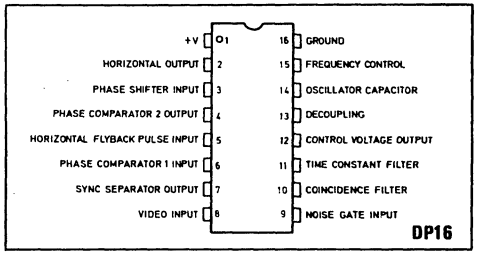


Fig. 1 Pin connections

FEATURES

- Sync separator
- Noise Gate
- Line Oscillator
- Dual Phase Comparator
- Suitable for Thyristor or Transistor Systems

QUICK REFERENCE DATA

Supply Voltage (nom.)	12V
Supply Current (nom.)	36mA
Video I/P (+ve Sync.)	3V
Flywheel Pull-in Range	±1kHz
Output Current	20mA

ABSOLUTE MAXIMUM RATINGS

Reference point is pin 16 unless otherwise stated

Supply voltage, V_{CC}	13.2V
Voltage at pin 3, V_3	0 to 13.2V
Voltage at pin 8, $-V_8$	12V
Voltage at pin 10, V_{10}	−0.5 to +5V
Average current pin 2, I_{2av}	20mA
Peak current, pin 2, I_{2pk}	200mA
Peak current, pin 5, I_{5pk}	10mA
Peak current. pin 7, I_{7pk}	10mA
Peak current, pin 8, I_{8pk}	10mA
Peak current, pin 9, I_{9pk}	10mA
Total power dissipation, P_{tot}	600mW
Storage temperature, T_{stg}	−55 to +125°C
Operating ambient temperature, T_{amb}	−10 to+60°C

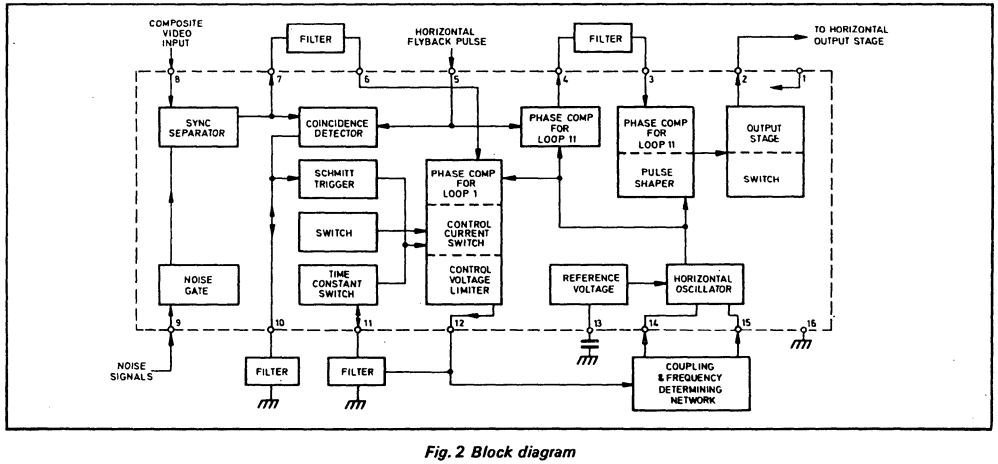


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} = +12V
T_{amb} = +25°C
Reference point pin 16
Measured in test circuit Fig. 3 (CCIR standard)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Current consumption	I_1		35		mA	I_2 = 0
REQUIRED INPUT SIGNALS						
Video Signal (Pin 8)						
Input voltage, peak-to-peak	$V_{in\ p\text{-}p}$	1	3	7	V	Positive-going sync.
Peak input current during sync. pulse	I_{8pk}		100		μA	
Noise Gating (Pin 9)						
Input voltage, peak	V_{9pk}	0.7			V	
Input current, peak	I_{9pk}	0.03		10	mA	
Input resistance	R_9		200		Ω	
Flyback Pulse (Pin 5)						
Input voltage, peak	V_{5pk}		±1		V	
Input current, peak	I_{5pk}	0.05	1		mA	
Input resistance	R_5		400		Ω	
Pulse duration	t_5	10			μs	f_o = 15625 Hz
DELIVERED OUTPUT SIGNALS						
Composite Sync. Pulses, +ve, Pin 7						
Output voltage, p-p	$V_{7p\text{-}p}$		10		V	
Output resistance						
at leading edge of pulse (emitter follower)	R_7		50		Ω	
at trailing edge	R_7		2.2		kΩ	
Additional external load resistance	R_{7ext}	2.0			kΩ	
Driver Pulse (Pin 2)						
Output voltage, p-p	$V_{2p\text{-}p}$		10		V	
Average output current	I_{2av}			20	mA	
Peak output current	I_{2pk}			200	mA	
Output resistance (low ohmic)	R_2		15		Ω	
Output pulse duration			2.5		Ω	V_2 = +10.5V, external resistor pins 2 – 16
when synchronised	t_2		12 to 32		μs	See operating notes (1)
Permissible delay between leading edge of output pulse and flyback pulse	t_{otot}		0 to 15		μs	t_5 = 12μs
Supply voltage at which output pulses are obtained	V_{CC}	4			V	
Oscillator						
Free-running frequency	f_o		15625		Hz	R_{15} = 3.3kΩ, See operating notes (2)
Spread of frequency at nominal values of peripheral components	$\frac{\Delta f_o}{f_o}$					
TBA920				±5	%	See note 1 " "
TBA920S				±1.5	%	See note 1 " "
Frequency change when decreasing supply down to minimum 4V	$\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$			10	%	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$		16.5		Hz/μA	
Adjustment range of network in circuit of Fig. 3	$\frac{\Delta f_o}{f_o}$		±10		%	

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Influence of supply voltage on frequence at V_p = 12V	$\frac{\delta f_o/f_o}{\delta V_p/V_{pnom}}$			5	%	
Control Loop I (Between Sync. Pulse and Oscillator)						
Control voltage range	V_{12}		0.5 to 5.5		V	
Control current, peak	I_{2pk}		±2		mA	V_{10}>4.5V, V_6>1.5V
			±6		mA	V_{10}<2V, V_6>1.5V
Loop gain of APC system	$\frac{\Delta f}{\Delta t}$		1		kHz/µs	Time coincidence between sync. pulse and flyback pulse or V_{10}>4.5V
			3		kHz/µs	No time coincidence or V_{10}<2V
Capture and holding range	Δf		±1		kHz	See note 2
Pull-in time	t		20		ms	$\Delta f/f_o$ = ±3% (Δf=470Hz), see Fig. 3
Switch-over from high control sensitivity to low control sensitivity after capture	t		20		ms	See Fig. 3
Control Loop II (Between Flyback Pulse and Oscillator)						
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	t_{dtot}		0 to 15		µs	
Static control error	$\frac{\Delta t}{\Delta t_d}$			0.5	%	See operating notes (3)
Peak output current during flyback pulse	I_{4pk}		±0.7		mA	
Overall Phase Relation						
Phase relation between leading edge of sync. and middle of flyback pulse	t		4.9		µs	See operating notes (4)
Tolerance of phase relation	Δt					
TBA920				±0.7	µs	See operating notes (5)
TBA920S				±0.4	µs	See operating notes (5)
Voltage for t_2 = 12 to 32µs	V_3		6 to 8		V	
Adjustment sensitivity	$\frac{\Delta t_2}{\Delta V_3}$		10		µs/V	
Input current	I_3			2	µA	
External Switch-over of Parameters (Loop Filter and Loop Gain) of Control Loop I (e.g. for Video Recorder Application). See Note 3						
Required switch-over voltage	V_{10}	4.5			V	R_{11} = 150Ω
				2.0	V	R_{11} = 2kΩ
Required switch-over current	I_{10}		80		µA	R_{11} = 150Ω, V_{10} = 4.5V
			120		µA	R_{11} = 2kΩ, V_{10} = 2.0V

NOTES
1. Exclusive of external component tolerances
2. Adjustable with R_{12-15}
3. With sync. pulses at pins 7 and 8; without RC network at pin 10

OPERATING NOTES

1. The output pulse duration is adjusted by shifting the leading edge (V_3 from 6V to 8V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.
For a line output stage with a BU108 high voltage transistor the resulting duration is about 22μs, and in such a way that the line output transistor is switched on again about 8μs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.
2. The oscillator frequency can be changed for other TV standards by an appropriate value of C_{14}.
3. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync. pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
4. This phase relation assumes a luminance delay line with a delay of 500ns between the input of the sync. separator and the drive to the picture tube. If the sync. separator is inserted after the luminance delay line or if there is no delay line at all (monochrome sets), then the phase relation is achieved at C_5 = 560pF.
5. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a DC voltage to pin 3.

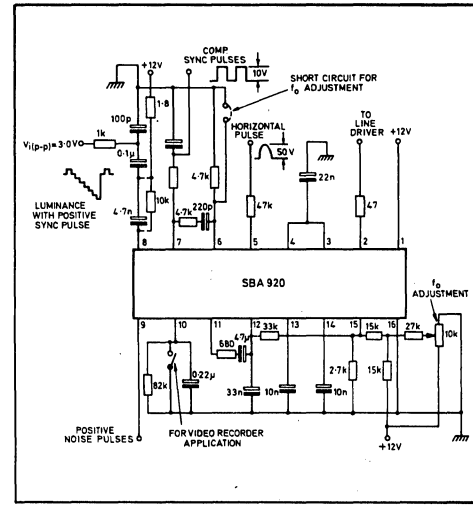


Fig. 3 Application diagram

TBA950 : 2X

LINE OSCILLATOR COMBINATION

The TBA950 :2X is a monolithic integrated circuit for pulse separation and line synchronisation in TV receivers with transistor output stages.

The TBA950 :2X comprises the sync. separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers prepared frame sync. pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration few external components are needed.

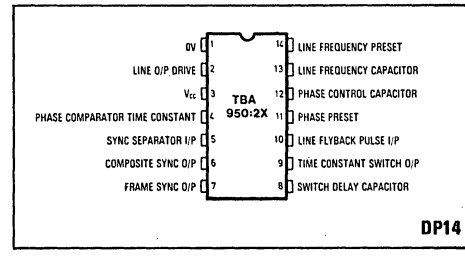


Fig. 1 Pin Connections

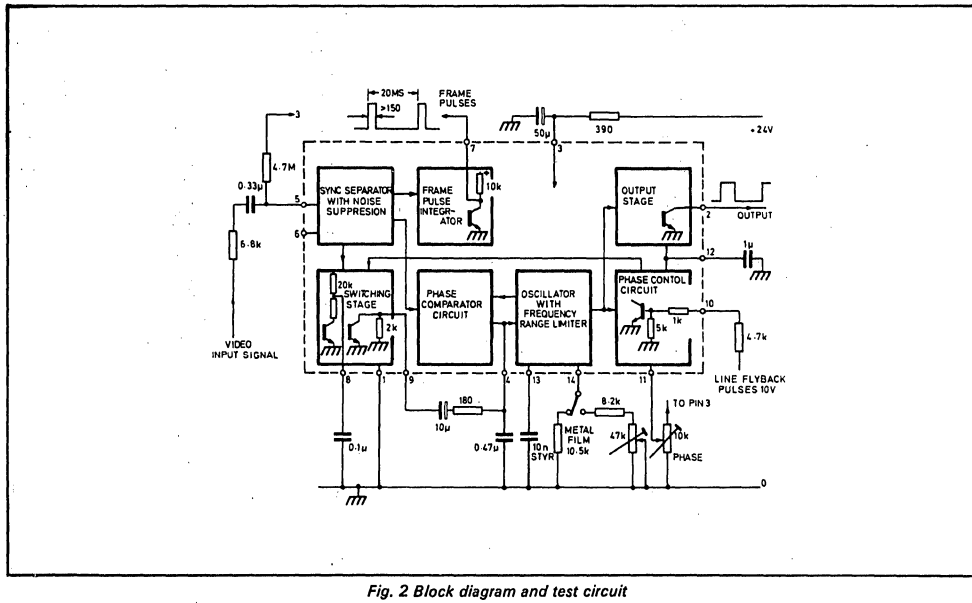


Fig. 2 Block diagram and test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$
$f_o = 15625Hz$ in the test circuit Fig.2 (see note 1)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Amplitude of frame pulse	V_1		>8		V	
Frame pulse duration	t_7		>150		µs	
Output resistance at pin 7 (high state)	$R_{out\ 7}$	7.5	10	13	kΩ	
Amplitude of sync. pulse	V_6		>8		V	
Output resistance at pin 6	$R_{out\ 6}$	2.5		4.5	kΩ	
Output pulse duration	t_2	25		28.5	µs	Typical range
Residual output voltage	$V_{2\ res}$		<0.55		V	$I_2 = 20mA$
Oscillator frequency	f_o	14843	15625	16406	Hz	$C_{13/1} = 10nF$ $R_{14/1} = 10.5kΩ$
Frequency pull-in range	$\pm\Delta f_F$	400		1000	Hz	Typical range
Frequency holding range	$\pm\Delta f_H$	400		1000	Hz	Typical range
Slope of phase comparator control loop	df_o/dt_d		2		kHz/µs	
Gain of phase control	dt_d/dt_p		20			
Phase shift between leading edge of composite video signal and line flyback pulse (see note 2) adjustable by V_{11}	t_v	−1		3.5	µs	Typical range

NOTES
1. By modification of the frequency-determining network at pins 13 and 14, these ICs can also be used for other line frequencies.
2. The limited flyback pulse should overlap the video signal sync. pulse on both edges.

OPERATING NOTES

The sync. separator separates the synchronizing pulses from the composite video signal. The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync. pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network hitherto required between sync. separator and frame oscillator is no longer needed. Since the frame sync. pulse duration at pin 7 is subject to production spreads it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF polystyrene capacitor at pin 13 which is charged and discharged periodically by two internal current sources: The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync. pulses. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync. pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g. due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync. pulse on both edges (see Fig. 3).

The switching stage has an auxiliary function. When the two signals supplied by the sync. separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin. 9. Thus the time constant of the filter

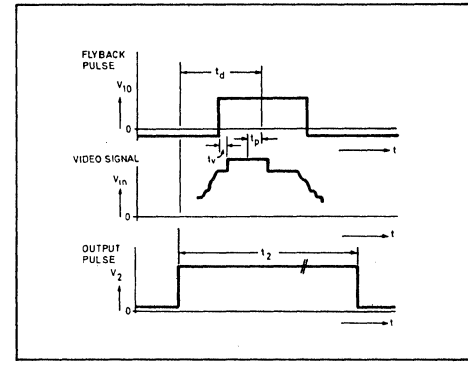


Fig. 3 Phase relationships

network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50Hz. This arrangement ensures disturbance-free operation.

For video recording operation this automatic switch-over can be blocked by a positive current fed into pin 8, e.g. via a resistor connected to pin 3. It may also be useful to connect a rsistor of about 630 Ω or 1 kΩ between pin 9 and earth. The capacitor at pin 4 may be lowered, e.g. to 0.1µF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e.g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to $V_3 = 4V$ and shuts off when V_3 falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_3 reaches 4.5V, In the range between $V_3 = 4.5V$ and full supply the shape and frequency of the output pulses are practically constant.

RECOMMENDED OPERATING CONDITIONS

For operating circuits Figs. 4 and 5

Input current during sync. pulse I_5	$>5\mu A$
Composite video input signal $V_{in\ p\text{-}p}$	3(1 to 6)V
Input current during line flyback pulse I_{10}	0.2 to 2 mA
Switchover current I_8	$>2mA$
Time difference between the output pulse at pin 2 and the line flyback pulse at 10, t_d	$<20\mu s$
Current consumption (see Fig. 6) I_3	$<31mA$
Ambient operating temperature range, T_{amb}	0 to $+60°$

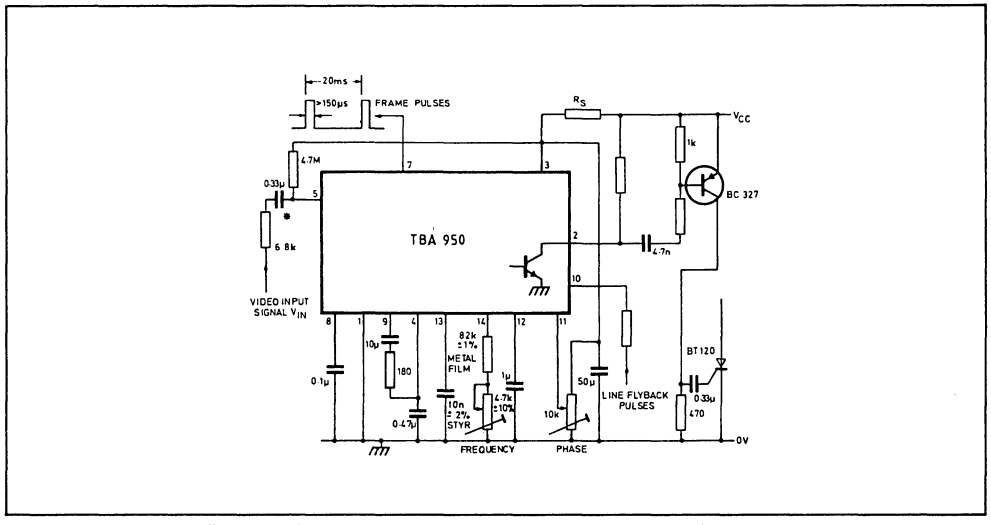


*Fig. 4 Operating circuit (thryistor output stage) *Input circuitry must be optimised*

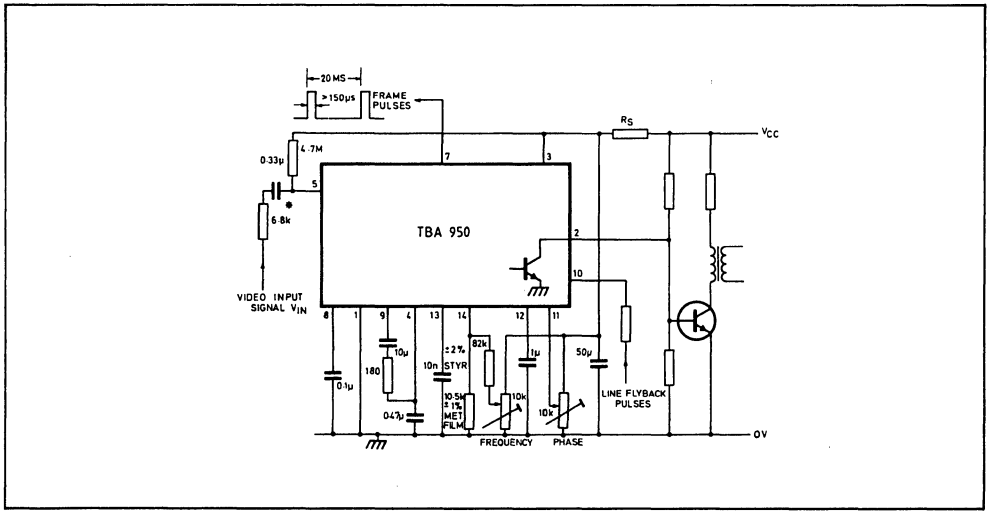


*Fig. 5 Another possiblity for line frequency adjustment (transistor output stage) *Input circuitry must be optimised*

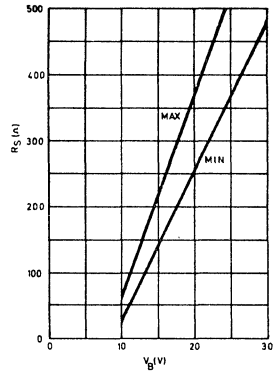


Fig. 6 Graph for determining the supply series resistor R_5

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to pin 1

Supply current (see Fig. 6) I_5:	45mA
Input current I_5:	2mA
Input voltage V_5	−6V
Output current I_2	22mA
Output voltage V_2:	12V
Switch-over current for video recording I_8	5mA
Phase correction voltage V_{11}:	0 to V_3
Operating temperature range	−10°C to +60°C
Storage temperature range	−55°C to +125°C

PLESSEY Semiconductors

CONSUMER

TV CIRCUIT

TCA800

COLOUR DEMODULATOR WITH FEEDBACK CLAMPS

A monolithic integrated circuit for colour television receivers incorporating two active synchronous demodulators for the F_{B-Y} and $\pm F_{R-Y}$ signals, a G-Y matrix, PAL switch bistable and RGB matrix, suitable for driving simple single transistor video output stages. The circuit incorporates three feedback clamps to stabilise the black level, to eliminate the problem of thermal drift in the demodulators.

OPERATING NOTES

For alternative applications in a simple decoder circuit, it must be possible to trigger the flip-flop so that it runs in the correct ident. phase by means of an AC coupled, 2 volt p-p square wave, derived from the APC loop in the reference generator circuit. (The normal input line timebase pulse would still be applied in order to provide clamp pulses.)

Input impedance of output amplifier (BF337) (Expressed as parallel resistance and capacitance.)

R (typ.) 5kΩ
C (typ.) 80pF

The above values are given for suitable design of output stages i.e. emitter follower with 5mA current capability.

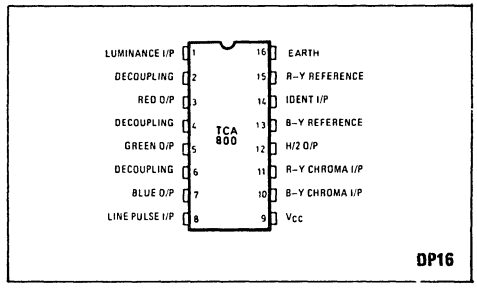


Fig. 1 Pin connections

QUICK REFERENCE DATA

V_{supply} -(Nominal) 12V
I_{supply} -(Nominal) (I_8 = 0.5mA) 47mA
Voltage Gain of Chrominance (R-Y) Signal Channel (typ.) $V_{in(p-p)}$ = 50mV; f = 4.43MHz; Video Gain = X20 17.5V/V
Voltage Gain of Luminance (Y) Channel V_{in} (Black-to-White) = 1V (p-p) 5V/V
Operating Temperature Range −10 to +55°C

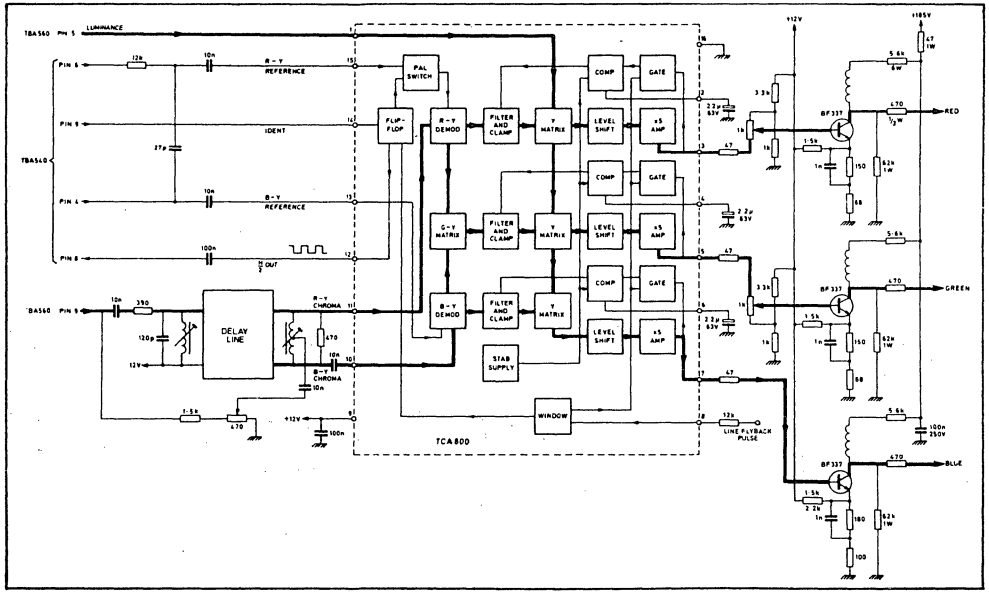


Fig. 2 Block diagram and typical application circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C, V_{CC} = +12V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage range	9	10.8	12	13.2	V	
Voltage gain of chrominance (R-Y) signal channel			17.5		V/V	$V_{in\ p\text{-}p}$ = 50mV, f = 4.43MHz, video gain = X20
Voltage gain of luminance (Y) channels			5		V/V	$V_{in\ (black\text{-}to\text{-}white)}$ = 1V p-p
Bandwidth (−3dB) of luminance channel from Y input to R-G-B outputs			10		MHz	
Bandwidth (−3dB) of chroma channel from $F_{(R\text{-}Y)}$, $F_{(B\text{-}Y)}$ inputs to R-G-B outputs			1		MHz	
Ratio of demodulated signals						
$V_{(B\text{-}Y)}/V_{(R\text{-}Y)}$		1.60	1.78	1.96		Defined with equal chroma input signals
$V_{(G\text{-}Y)}/V_{(R\text{-}Y)}$		0.76	0.85	0.94		and measured at output pins (see note 1)
Input Characteristics						
Chrominance input impedance (expressed as resistance and parallel capacitance	10, 11					
R			1000		Ω	
C				10	pF	f = 4.43MHz, V_{in} = 20mV sinewave
Luminance (Y) input blanking level (fixed by TBA560)	1	1.4	1.5	1.8	V	
Luminance (Y) input, black level potential (nominal brightness set by brightness control of TBA560)	1		1.7		V	
Luminance (Y) input black-to-white amplitude (adjusted by contrast control of TBA560)	1		1.0		Vp-p	
Reference input impedance (expressed as resistance and parallel capacitance)	13, 15					
R			5.0		kΩ	f = 4.43MHz
C			5.0	10	pF	
Reference input voltage (from TBA540)	13, 15	0.5	1.0	2.0	V p-p	
Phase shift between reference inputs and chroma input signal to give coincidence at the synchronous demodulators	13, 15		10		degrees	
Ident. voltage for ident 'off'	14	+6			V	
Ident. voltage for ident 'on'	14			+7.0	V	
Ident. current for ident 'off'	14			0.1	mA	
Tracking of ident. threshold with a supply variation of ±10% $\frac{\Delta V_{threshold} \cdot V_{CC}}{V_{threshold} \cdot \Delta V_{CC}}$	14		1.0			
Required line pulse input current to clamps and H/2 flip-flop	8	0.3	0.45	0.6	mA	
Window level (see note 2)	8		+12.5		V	
Line input impedance	8	0.6	1.0	1.4	kΩ	
Output Characteristics						
R-G-B outputs blanking level	3, 5 7		2.0		V DC	Blanking level at pin 1 = 1.5V
Common mode variation of black level variation over a temperature range of 40°C		See note 3				
Blanking-to-white level output voltage capability of each output amplifier channel	3, 5, 7	6		8	V p-p	

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Difference in clamped blanking level of outputs i.e., R to G to B	3,5,7			50	mV	
Differential drift of clamped output blanking levels over temperature range of 40°C	3, 5, 7			25	mV	
Residual 4.43MHz signal at R-G-B outputs						
Red				150	mV p-p	
Blue				300	mV p-p	
H/2 square wave output amplitude	12	2.5	3.5		V p-p	Measured with 3kΩ load i.e. TBA540

NOTES
1. These values are chosen to minimise errors in flesh tones and of the luminance of the green component. The matrix equation for the derivation of the G-Y component is given by G-Y = −0.51(R-Y) −0.19(B-Y). (This is derived from the basic colour equation Y = 0.30R + 0.59G +0.11B.) Measured at the tube cathodes with 100V p-p video drive.
2. In order to provide a clamp pulse which occurs inside the blanking waveform and free from the edge spikes, it is necessary to window the line pulse at about two thirds of its amplitude.
3. In order to partially compensate for drift in output stages a negative temperature coefficient to compensate for the variation in the video output transistor has been incorporated.

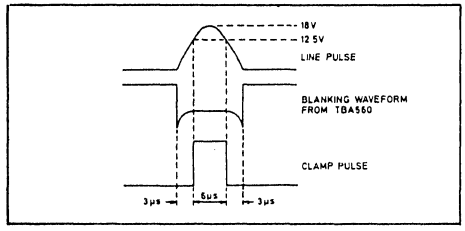


Fig. 3 Line pulse, blanking and clamp timings

ABSOLUTE MAXIMUM RATING

Max. dissipation @ +55°C = 900mW
Storage temperature range −55°C to +125°C

PLESSEY
Semiconductors

CONSUMER
TV CIRCUIT

TDA 440
VIDEO IF AMPLIFIER/DEMODULATOR

The TDA440 incorporates the following functions:

1. Three-stage symmetrical IF (broad band) amplifier with first and second stages AGC-controlled.
2. Controlled video carrier demodulator.
3. Video drive amplifier with low-pass response and output independent of supply fluctuations.
4. Gated AGC section for IF amplifier.
5. Delayed regulated output voltage for the tuner preamplifier.

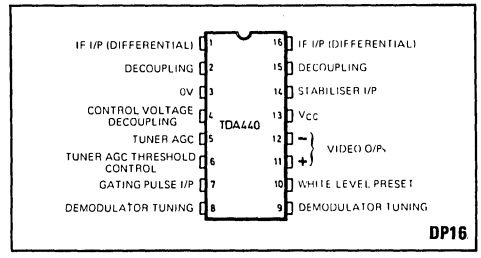


Fig. 1 Pin connections.

FEATURES

- High Gain – High Stability
- Constant Input Impedance Independent of AGC
- Low Noise Independent of AGC
- High Supply Rejection
- Low RF Breakthrough to Video O/Ps
- Fast AGC Action
- Very Low Intermodulation Products
- Minimum Differential Error
- Positive and Negative Video O/Ps
- Low Impedance Video O/Ps
- Temperature Compensated
- Peak White Adjustable

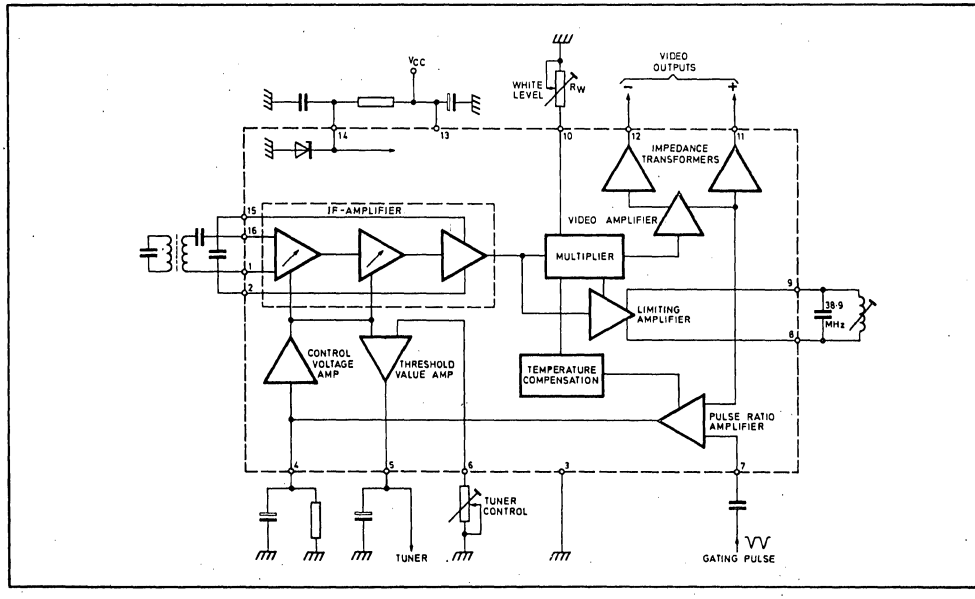
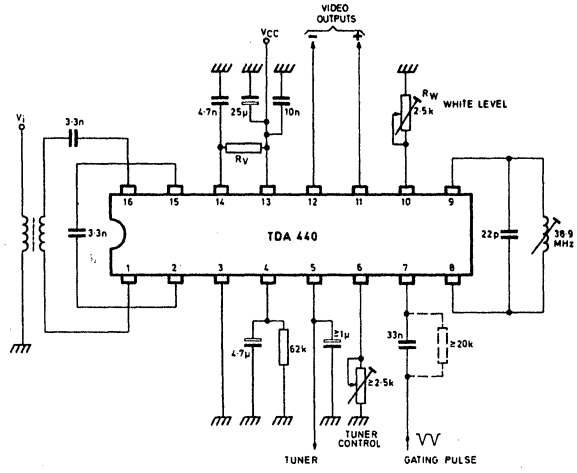


Fig. 2 TDA440 block diagram.

ABSOLUTE MAXIMUM RATINGS

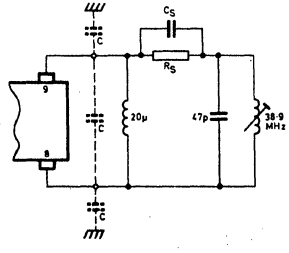
Reference point is pin 3

Rating	Pin	Symbol	Value	Units
Supply voltage range	13	V_{CC}	10 to 15	V
Low voltage stabiliser supply current	14	I_s	50	mA
Open loop voltage	5	V_5	15	V
Video DC output current				
Average positive	12	I_{12}	5	mA
Peak positive	12	I_{12}	30	mA
Average negative	11	I_{11}	5	mA
Peak negative	11	I_{11}	30	mA
White level control	10	V_{10}	3.2	V
Power dissipation at $T_{amb} \leqslant 55°C$		P_{tot}	700	mW
Ambient temperature range		T_{amb}	−10 to +65	°C
Storage temperature range		T_{stg}	−55 to +125	°C



Supply voltage *must be disconnected* before inserting the integrated circuit into the test socket.

Fig. 3 Test and application circuit.



C = Parasitic capacitance at pins 8 and 9 should be kept to a minimum.
C_S = 6 to 10pF series capacitance.
f_O = Series resonant frequency = 38,9 − (1,8 to 2,75) MHz.
R_S = Series resonance damping (determines tuning characteristics) = 1.8 to 3.3kΩ. E.G., with R_S = 2.4kΩ, tuning range, f, = 3MHz.

Fig. 4 Modifications to Fig. 3 for improving audio interference and cross-colour characteristics.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C
V_{CC} = +12V
Reference point is pin 3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}	13	10	12	15	V	
Supply current, I_{13}	13	15	19	25	mA	
Supply voltage, stabiliser input	14	5.5	5.8	6.4	V	I_{14} = 40mA
Positive video DC output voltage	11		5.5		V	
White level adjustment range for positive video DC output voltage	11			4.8	V	R_W (pin 10) = ∞
		6.5			V	R_W (pin 10) = 0
Peak black clamping level for positive video DC output voltage	11	1.75	1.9	2.15	V	
DC output current	11		3.2		mA	Reference point pin 13
Negative video DC output voltage	12		5.6		V	
Available tuner control current	5	7	7.5		mA	10dB after onset of tuner control action
Negative gating pulse	7	1.5	3	5	Vp-p	
Composite video output level	11		3.3		Vp-p	V_{11} = 5.5VDC
			4.2		Vp-p	V_{11} = 6.4VDC
AGC range, ΔAGC		50	56		dB	
Video 3dB bandwidth		8	10		MHz	
Video frequency response change			1.0	2.0	dB	ΔAGC = 50dB, video bandwidth = 0 to 5 MHz
Symmetrical input voltage for 3.3Vp-p output (pin 11)	1-16	100	150	220	μVr.m.s	
Maximum IF voltage level present at video outputs over the full AGC range	11,12			30	mV	f = 38.9MHz
				50	mV	f = 77.8MHz (2nd harmonic)
Sound IF voltage level present at video outputs with selective circuit	12	30			mV	f = 5.5MHz, $\frac{\text{picture carrier level}}{\text{sound carrier level}}$ = 30dB
Differential gain of negative comp. video output signal for full black to white swing				15	%	
Suppression of sound carrier/colour subcarrier (1.07MHz) w.r.t colour subcarrier level		40			dB	Picture carrier = 0dB, IF colour subcarrier level = −6dB, IF sound carrier level = −24dB
Input impedance	1					Reference point pin 16
AGC max.			1.4//2		kΩ//pF	
AGC min.			1.4//1.9		kΩ//pF	

TDA2522/3

COLOUR DEMODULATOR COMBINATION

The TDA2522 and TDA2523 are integrated synchronous demodulators for colour television receivers. The devices incorporate an 8.8MHz oscillator followed by a divider giving two 4.4MHz reference signals, a keyed burst phase detector for optimum noise behaviour, an ACC detector and amplifier, a colour killer, two synchronous demodulators for the (B-Y) and (R-Y) signals, a PAL switch and a PAL flip-flop with internal identification.

The symmetrical demodulators include integrated capacitors to reduce unwanted carrier signals at the outputs which are taken from temperature-compensated emitter followers. The outputs of the TDA2522 are suitable for use with the TDA2530. The TDA2523 outputs are inverted for use with a direct transistor drive.

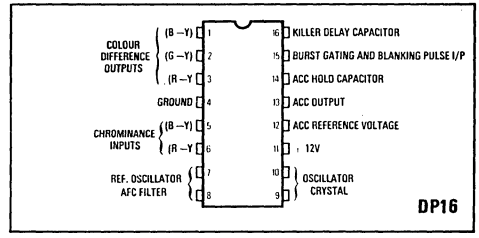


Fig. 1 Pin connections

QUICK REFERENCE DATA

- Supply Voltage (pin 11): 12V typ.
- Supply Current: 40mA typ.
- Colour Difference Signals:
  - (R –Y) (pin 3): >2.4V p–p
  - (G –Y) (pin 2): >1.35V p–p
  - (B –Y) (pin 1): >3V p–p
- Chrominance Input Signal (Including Burst):
  - R –Y (pin 6) 500mV p–p
  - B –Y (pin 5) 350mV p–p
- Colour Difference Signal Output Impedance 250 Ω typ.

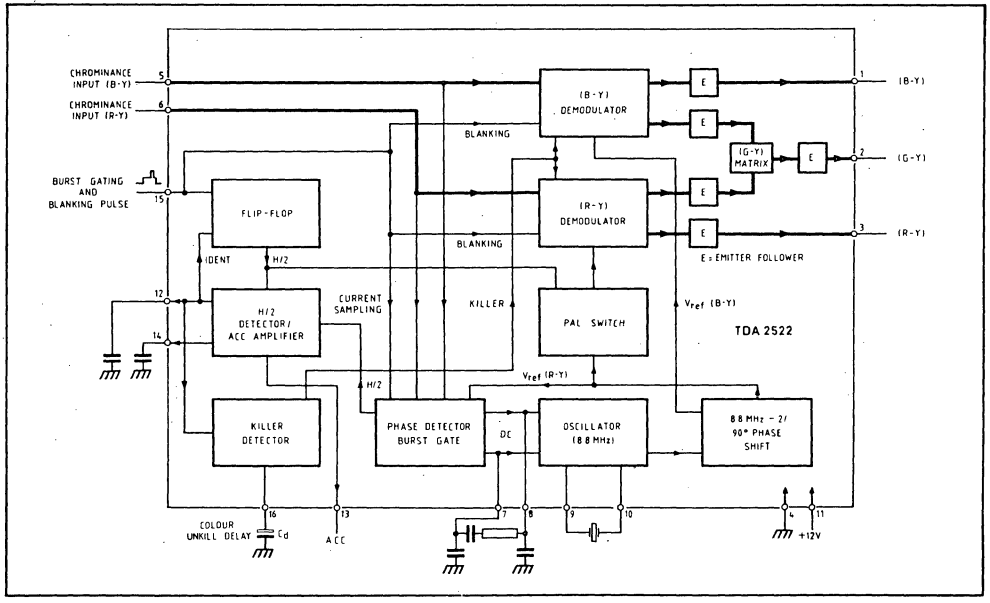


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions unless (otherwise stated):
Supply voltage, pin 11 = +12V
Tamb = +25°C
Measurements referred to pin 4

Charateristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Demodulator						
Ratio of demodulated signals:						
B–Y/R–Y	1/3		1.78		–	
G–Y/R–Y	2/3		0.85		–	See note 1
G–Y/R–Y	2/3		0.17		–	See note 2
Colour difference outputs:						
(R–Y)	3	2.4			Vp–p	
(G–Y)	2	1.35			Vp–p	
(B–Y)	1	3			Vp–p	
Chrominance input signal (including burst):						
R–Y	6		500		mVp-p	See note 3
B–Y	5		350		mVp–p	
Colour difference signal output impedances:						
(R–Y)	3		250		Ω	
(G–Y)	2		250		Ω	
(B–Y)	1		250		Ω	
H/2 ripple at R–Y O/P	3			10	mVp-p	
Blanking and keying pulse:						
Burst keying active for	15	7.5			Vp–p	
Burst keying inactive for	15			6.5	Vp–p	
Blanking active for	15	2			Vp–p	
Blanking inactive for	15			1	Vp–p	
Reference section						
Phase difference between reference and burst				±5	Deg.	Crystal frequency deviation ±400Hz
Overall holding range			±500		Hz	Using typical crystal
Burst signal input	5–6		0.25		Vp–p	Keying pulse width = 4μs,
Oscillator input resistance	10		270		Ω	
Oscillator input capacitance	10				pF	See note 5
Oscillator output resistance	9		200		Ω	
ACC reference voltage	12		7		V	
ACC voltage at correct phase	14		5.5		V	Burst = 0.25Vp–p
ACC voltage with zero burst	14		7.0		V	
ACC amplifier output voltage range	13	0.5		5.0	V	$I_{13} < \pm 200\mu A$
Colour killer						
Via pin 14:						
Colour off	14	6			V	
Colour on	14			5.6	V	
Via pin 16:						
Colour off	16	7			V	
Colour on	16			5	V	
Colour unkill delay			20		ms/μF	See note 6

NOTES
1. The demodulators are driven by a chrominance signal of equal amplitude for the (R—Y) and (B—Y) components. The phase of the (R—Y) chrominance signal equals the phase of the (R—Y) reference signal. The same holds for the (B—Y) signals.
2. As note 1, but with the phase of the (R—Y) reference signal reversed.
3. Colour bar with 75% saturation.
4. The burst amplitude is kept constant by ACC action, but depends linearly on the keying pulse width.
5. To be established.
6. The delay depends on the value of Cd (see Fig. 2)

FUNCTIONAL DESCRIPTION

Functions listed by pin number.

	TDA2522	TDA2523
1.	-(B-Y) signal output	(B-Y) signal output
2.	-(G-Y) signal output	(G-Y) signal output
3.	-(R-Y) signal output	(R-Y) signal output

These outputs are of low impedance from temperature compensated emitter follower stages that require external loads of 10kΩ. Internal filtering of the colour difference output signals to give a −3dB bandwidth of 1MHz allows the three signals to be fed directly to the luminance matrix. The TDA2522 may be AC coupled to the TDA2530, and the TDA2523 may be used with direct transistor drive.

4. Negative supply (Ground)

5. Chrominance B−Y input signal

An input signal of approximately 350mV p-p (colour bars) is required at this pin. The B−Y component of colour burst must be included with the input chrominance signal.

6. Chrominance R−Y input signal

An input signal of approximately 500mV p-p (colour bars) is required, including the R−Y colour burst component.

7. Reference oscillator APC loop filter

8. Reference oscillator APC loop filter

Between pins 7 and 8 are connected the APC loop low pass filter components. The difference voltage between these pins is connected internally to the oscillator reactance stage.

9. Oscillator feedback

10. Oscillator feedback

A series network consisting of the 8.8MHz crystal and an adjustable tuning capacitor is connected between pins 9 and 10. Division from the 8.8MHz oscillator within the IC produces the 4.4MHz quadrature reference carriers which are then applied to the colour demodulators.

11. Positive 12V supply

The maximum voltage must not exceed 14V.

12. ACC hold capacitor

The capacitor connected from this pin to ground is normally charged to a potential of about 7V.

13. ACC output potential

An output potential varying inversely with the input colour burst amplitude is available at pin 13. Maximum ACC gain of the TDA2560 is provided when the ACC potential from pin 13 of the device is greater than about 1.4V.

14. ACC hold capacitor

The capacitor connected from this pin to ground is normally charged to a potential of 5.5V. On monochrome reception the potential will be 7.0V and while identing it may instantaneously increase to about 8V. A 100Ω resistor may be connected in series with the capacitor from pin 14, see pin 15.

15. Burst gating and blanking pulse input.

The two-level positive pulse required at this pin is used for burst gating and flip-flop triggering, at a sampled level of 7V. A negative going pulse of about 100mV p-p, derived from the colour burst, may be inspected across a 100Ω resistor in series with the capacitor from pin 14 to ground, should the sandcastle pulse shape require some adjustment. At a level of about 1.5V the pulse width should be suitable for chroma blanking.

16. Killer delay capacitor

The value of a capacitor connected from pin 16 to ground determines the delay of un-killing. By this means the state of continuous switching of the killer with marginal signals, may be avoided. Connecting pin 16 to ground unkills the system.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (pin 1)	14V
Total power dissipation	600mW
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

TDA2530/2

RGB Matrix Preamplifier (with clamps)

The TDA2530 and TDA2532 are integrated RGB matrix preamplifiers for colour television receivers, incorporating a matrix preamplifier (for RGB cathode drive of the picture tube) with clamping circuits.

This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator IC.

The TDA2532 has been designed for use with on-screen data display systems.

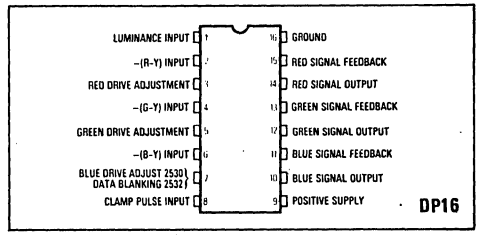


Fig. 1 Pin connections (top view)

QUICK REFERENCE DATA

- Supply Voltage (pin 9): 12V typ.
- Operating Ambient Temperature Range: –10 to +60°C
- Luminance Input Resistance (pin 1): 100kΩ min
- Colour Difference Input Currents (pins 2, 4 & 6):
  Unclamped 2μA typ.
  During Clamping –0.2 to +0.2mA
- Clamping Pulse Input Current (pin 8): 20μA max.
- Gain of RGB Preamplifiers: 0dB typ.
- Gain DC Adjustment Range: ±3dB typ.
- Error Amplifier Gain (Conductance): 20mA/V typ.
- Feedback Input Currents (pins 11, 13 & 15): 2μA typ.
- Output Current Swing (pins 10, 12 & 14): –4.4 to +4.4mA

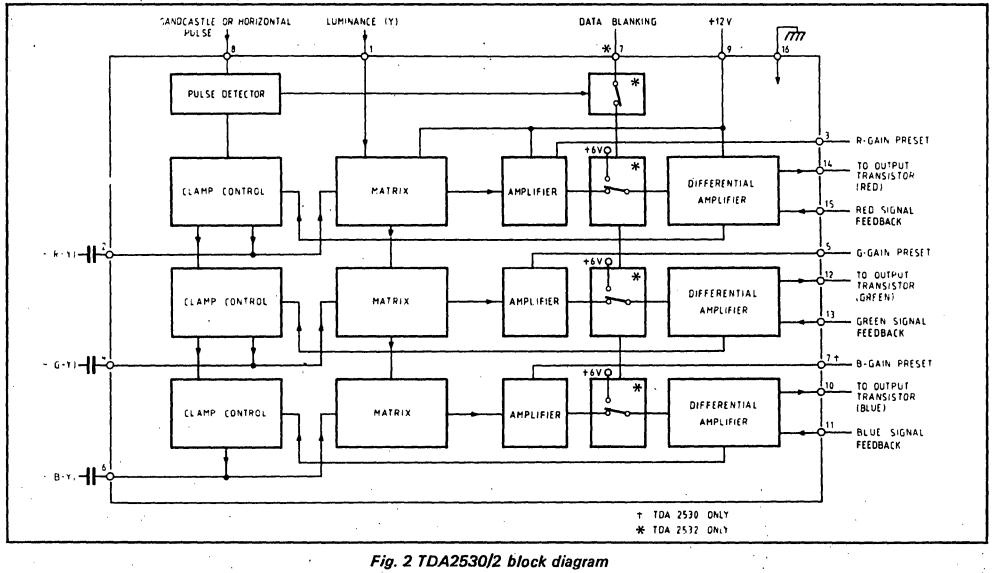


Fig. 2 TDA2530/2 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage (pin 9) = +12V
Luminance input (pin 1) = 1.5V
T_{amb} = +25°C
Measurements refer to pin 16
Test circuit Fig. 3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Current consumption	9		50		mA	
Luminance input	1					
Black level			1.5		V	
Black-to-white input voltage			1.0		Vp-p	
Input resistance		100			kΩ	
Colour Difference Input						
Input signals						
—(R–Y)	2		1.4		Vp-p	See Note 1
—(G–Y)	4		0.82		Vp-p	See Note 1
—(B–Y)	6		1.78		Vp-p	See Note 1
Input currents	2, 4, 6		2	4	μA	
Input currents during clamping	2, 4, 6	±0.2			mA	
Clamp Pulse Input for DC Feedback	8					
Clamping voltage						
ON		7.5		12	V	See Note 2
OFF		0		5.5	V	See Note 2
Clamping current						
ON				1	μA	
OFF				20	μA	
Feedback Input	11, 13, 15					
DC level during clamping			$0.5V_9$		V	
Gain Adjustment for Colour Drive						
Adjustment voltage range	3, 5, 7	0		10	V	See Note 4
Adjustment voltage for nominal gain	3, 5, 7		5		V	See Note 4
Nominal gain between colour difference inputs, luminance input and colour feedback inputs	11, 13, 15		0		dB	
Adjustment range of nominal gain	3, 5, 7	±3			dB	$At = \Delta V_{3,5,7,} = \pm 5V$
Differential Amplifier						
Feedback input current	11, 13, 15		2		μA	
Error amplifier gain			20		mA/V	
Output current swing	10, 12, 14		±4.4		mA	
Integrated load resistance	10, 12, 14		680		Ω	See Note 3
Output bias voltage	10, 12, 14		8		V	See Note 3 and applications information
Data blanking (TDA2532 only)	7		≥1		V	Pins 10, 12, 14 go to +6V

NOTES
1. The allocation of —(R–Y), —(G–Y) and —(B–Y) signals to pins 2, 4 and 6 respectively, is not mandatory as all three channels are identical.
2. Switching from clamping ON to OFF occurs at about 6V.
3. The integrated load resistors include series diodes; this means that the resistors can be ignored when $V_{10}, V_{12}, V_{14} > V_9$. Under this condition, external load resistors must be chosen such that the current is nominally 4.4mA. See Fig. 3.
4. The TDA2532 uses pin 7 for data blanking, the gain of one channel is therefore internally preset.

APPLICATIONS INFORMATION (fig 3)

The clamping level, V_{CL} of the video output stages, with set clamping level potentiometers in their mid-positions, is given by:

$$V_{CL} = V_9 \left(1 + \frac{R1}{R2} - \frac{R1}{R3}\right)$$

The gain of the video output stages is given by:

$$\text{Gain} = 1 + \frac{R1}{R2} + \frac{R1}{R3} + \frac{R1}{R4}$$

Attention should be given to earth paths, avoiding common impedances between the input (decoder) side and the output stages.

Printed track area connected to the feedback pins should be kept to a minimum.

To ensure a matched performance of the video output stages, a symmetrical layout of three stages should be employed.

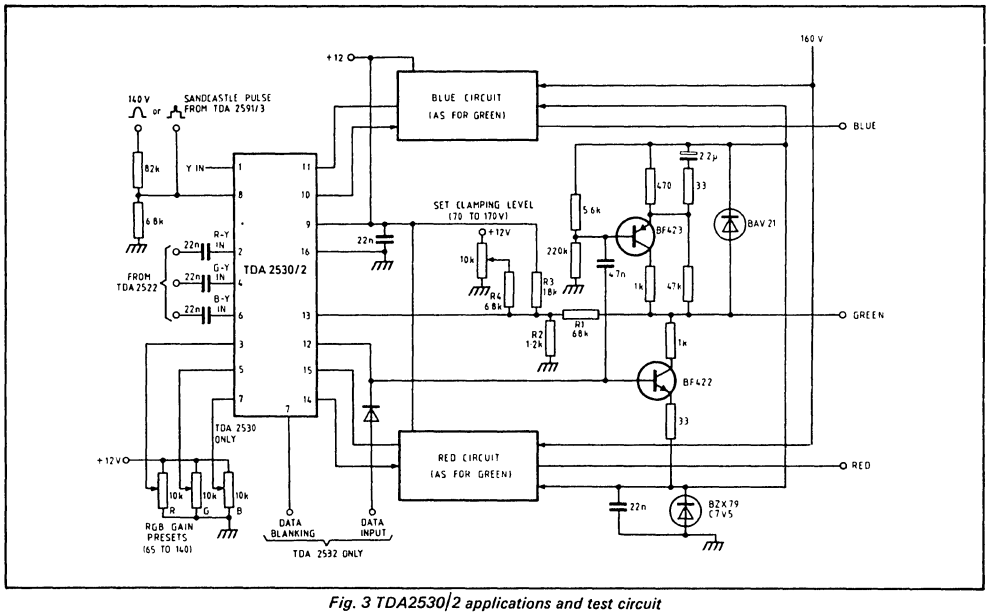


Fig. 3 TDA2530/2 applications and test circuit

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Luminance signal input.
A 1V black to white positive going luminance input signal is required. Blanking level should be at 1.5V and black level at 1.7V

2. −(R−Y) input signal
The input signal is required to be AC coupled from a low impedance source such as the TDA2522. The coupling capacitor also acts as a clamp capacitor for the TDA2530/2 red output. As the colour difference input impedance is at least 100kΩ, low value coupling capacitors may be used.

3. Red drive adjustment.
A gain variation of the red channel of at least ±3dB about the nominal, is obtained as the DC potential at this pin varies by ± 5V about the nominal of 5V. If no connection is made to a gain controlling pin the channel concerned assumes the nominal gain.

4. −(G−Y) input signal (see pin 2)

5. Green drive adjustment (see pin 3)

6. −(B−Y) input signal (see pin 2)

7. TDA2530: Blue drive adjustment (see pin 3)
TDA2532: Data blanking input.
When this pin is taken above 1V the colour output signals on pins 10, 12 and 14 are inhibited, the outputs being clamped to 6V.

8. Clamp pulse input
A positive going line pulse input is required and the pulse should exceed a threshold DC level set by the TDA2530/2 of 7.5 V. An input current of about 0.2mA is required. A maximum current of 1mA should not be exceeded.

9. Positive 12V supply.

10. Blue signal output

11. Blue signal feedback
The signal gain of both the video output stages and IC amplifier are stabilised by the feedback circuits. DC clamping is achieved by sampling of the feedback level during blanking. The black level potentials at the collectors of the video output stages may be varied independently by adjustable DC current sources applied to the feedback input pins. The DC levels at these pins are such that the feedback resistor and a resistor network between the 12V supply and earth provide a potential of 6V during blanking.

12. Green signal output

13. Green signal feedback (see pin 11)

14. Red signal output

15. Red signal feedback (see pin 11)

16. Negative supply (earth)

ABSOLUTE MAXIMUM RATINGS

Voltages	
Supply voltage (V_9)	15V
Pin 1, 2, 3, 4, 5, 6 & 7	0V to V_9
Pin 8	V_9
Pin 10	V_9 to V_9 + 3V
Pin 12	V_{13} to V_9 + 3V
Pin 14	V_{15} to V_9 + 3V
Pins 11, 13 and 15	0.3V_9 to V_9
Current	
Pin 8	1mA
Thermal	
Total power dissipation	1W
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

TDA2540 TDA2541

TELEVISION IF AMPLIFER AND DEMODULATOR (TDA2540 for NPN tuners, TDA2541 for PNP tuners)

The TDA2540 and TDA2541 are IF amplifier and demodulator circuits for colour and monochrome television receivers using NPN and PNP tuners respectively. The two circuits are in other respects identical. A VCR switch is incorporated for switching off the video signal when inserting a VCR playback signal.

FEATURES

- Gain-Controlled Wideband Amplifier, Providing Complete IF Gain
- Synchronous Demodulator
- White Spot Inverter
- Video Preamplifier with Noise Protection
- DC Controlled AFC
- AGC Circuit with Noise Gating
- Tuner AGC Output
- VCR Switch

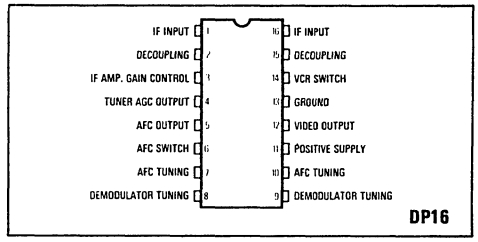


Fig. 1 Pin connections (top view)

QUICK REFERENCE DATA

- Supply Voltage (pin 11): 12V typ.
- Supply Current: 50mA typ.
- IF Input Voltage at f = 38.9MHz (pins 1 & 16): 100μV RMS typ.
- Video Output Voltage (pin 12): 3V typ.
- IF Voltage Gain Control Range: 64dB typ.
- Signal-to-noise Ratio at V_{in} = 10mV: 58dB typ.
- AFC O/P Voltage Swing for Δf = 100kHz (pin 6): 10V min.

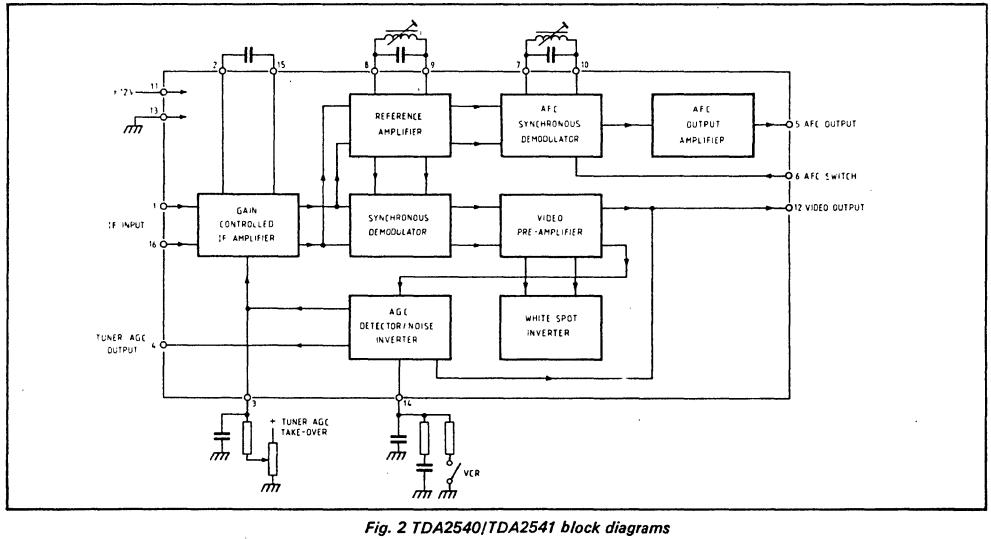


Fig. 2 TDA2540/TDA2541 block diagrams

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage (pin 11) = 12V
T_{amb} = +25°C
Measurements referred to pin 13
Test circuits Figs. 9 & 10

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Current			50		mA	
Supply voltage range	11	10.2	12	13.8	V	
IF input voltage for onset of AGC	1–16		100	150	µV RMS	f = 38.9 MHz
Differential input impedance	1–16		2//2		kΩ// pF	
Zero-signal output level	12	5.7	6.0	6.3	V	
Top sync. output level	12	2.9	3.07	3.2	V	
AFC output voltage swing	6	10	11		V	Δ f = 100kHz
IF voltage control range			64		dB	
Signal-to-noise ratio			58		dB	V_{in} = 10mV, See Note 1
Video amplifier 3dB bandwidth			6		MHz	
Differential gain			4	10	%	
Differential phase			2	10	deg.	
Carrier signal at video output			4	30	mV	
2nd harmonic of carrier at video output			20	30	mV	
Change of frequency at AFC output voltage swing of 10V			100	200	kHz	
Intermodulation at 1.1MHz						
Blue		46	60		dB	} See Note 2 and Figs 3 and 4
Yellow		46	50		dB	
Intermodulation at 3.3MHz		46	54		dB	
AFC switches off at:	6			2.5	V	
VCR switches off at	14			1.1	V	
White spot inverter threshold			6.6		V	
White spot insertion level			4.7		V	See Fig 5
Noise inverter threshold level			1.8		V	
Noise insertion level			3.8		V	
Typical tuner AGC output current	4	0		10	mA	
Tuner AGC output voltage	4			0.3	V	I_4 = 10mA
Tuner AGC output leakage current	4			15	µA	V_{14} = 3V, V_4 = 12V

NOTES:

1. $S/N = \frac{V_{out}\text{ black-to-white}}{V_{in}\text{ at bandwidth = 5MHz}}$

2. Intermodulation at 1.1MHz = $20 \log \frac{V_{out}\text{ at 4.4MHz}}{V_{out}\text{ at 1.1MHz}}$

3. Intermodulation at 3.3MHz = $20 \log \frac{V_{out}\text{ at 4.4MHz}}{V_{out}\text{ at 3.3MHz}}$

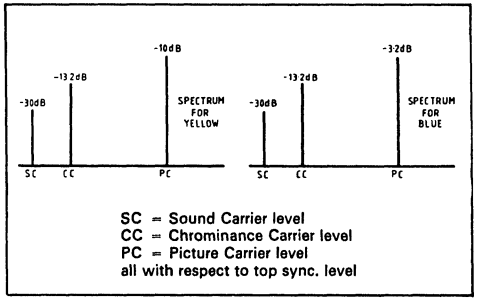


Fig. 3 Input conditions for intermodulation measurements – standard colour bar with 75 percent contrast

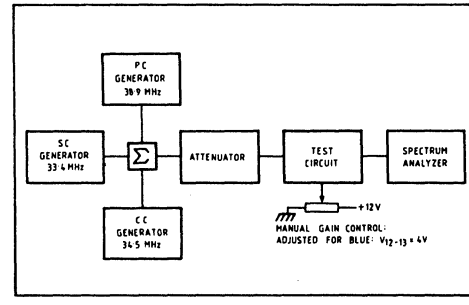


Fig. 4 Test set-up for intermodulation

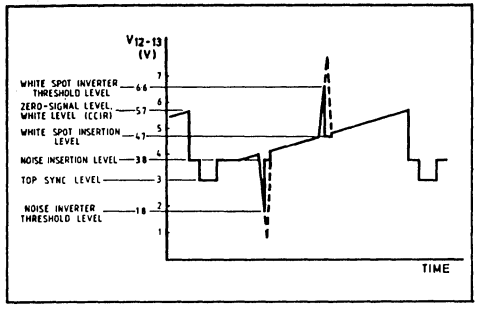


Fig. 5 Video output waveform showing white spot and noise inverter threshold levels

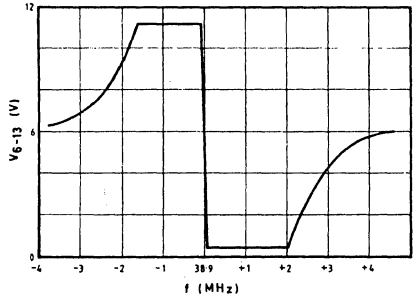


Fig. 6 AFC output voltage (pin 6) as a function of frequency

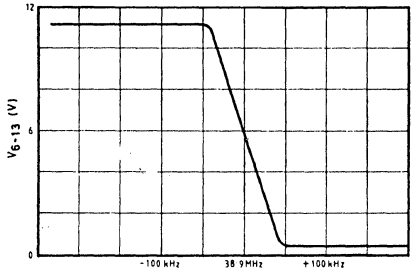


Fig. 7 Expansion of Fig. 6

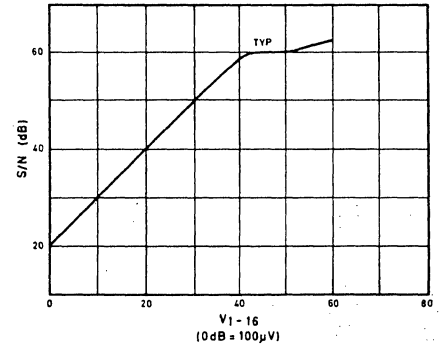


Fig. 8 Signal-to-noise ratio as a function of input voltage

APPLICATIONS INFORMATION

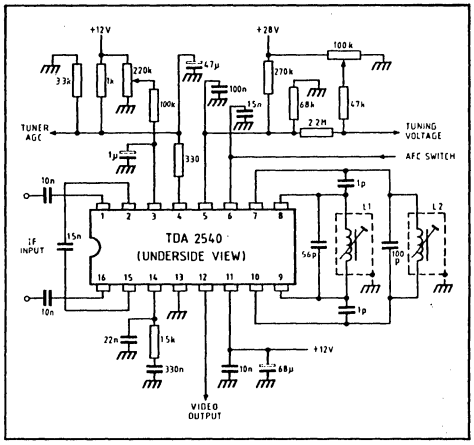


Fig. 9 TDA2540 typical application circuit

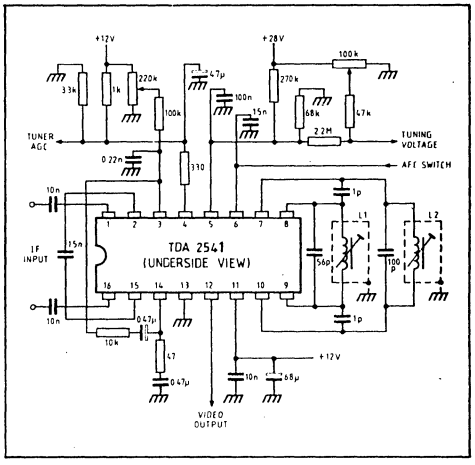


Fig. 10 TDA2541 typical application circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltage	13.8V
Tuner AGC voltage	12V
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

TDA2560

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TDA2560 is an integrated circuit for use in colour television receiver decoding systems, and consists of a luminance amplifier and a chrominance amplifier. The luminance amplifier has a low input impedance so that luminance delay line matching is very easy. The chrominance amplifier has a combined chroma and burst output, the burst signal amplitude unaffected by contrast and saturation control.

QUICK REFERENCE DATA

- Supply Voltage (pin 8) 12V typ.
- Supply Current 45mA typ.
- Luminance Signal Input Current (Black-to-White Value) (pin 14) 0.2mA typ.
- Chrominance Input Signal (pins 2 & 1) 4 to 80 mVp-p
- Luminance Output Signal at Nominal Contrast (Black-to-White Value) (pin 10) 3V typ.
- Chrominance Output Signal at Nominal Contrast and Saturation and 1.25Vp-p Burst Output (pin 6) 2.5Vp-p typ.
- Contrast Control Range >20dB
- Saturation Control Range >20dB

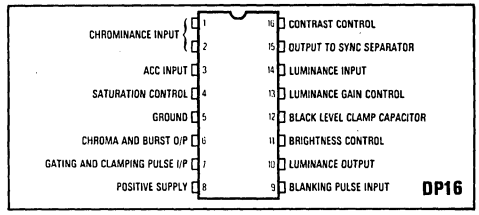


Fig. 1 Pin connections (top view)

FEATURES

Luminance Amplifier

- DC Contrast Control
- DC Brightness Control
- Black Level Clamp
- Blanking
- Additional Video O/P with +ve Sync.

Chrominance Amplifier

- Gain Control Amplifier
- Chrominance Gain Control Tracked with Contrast Control
- Separate DC Saturation and Contrast Controls
- Direct Delay Line Drive

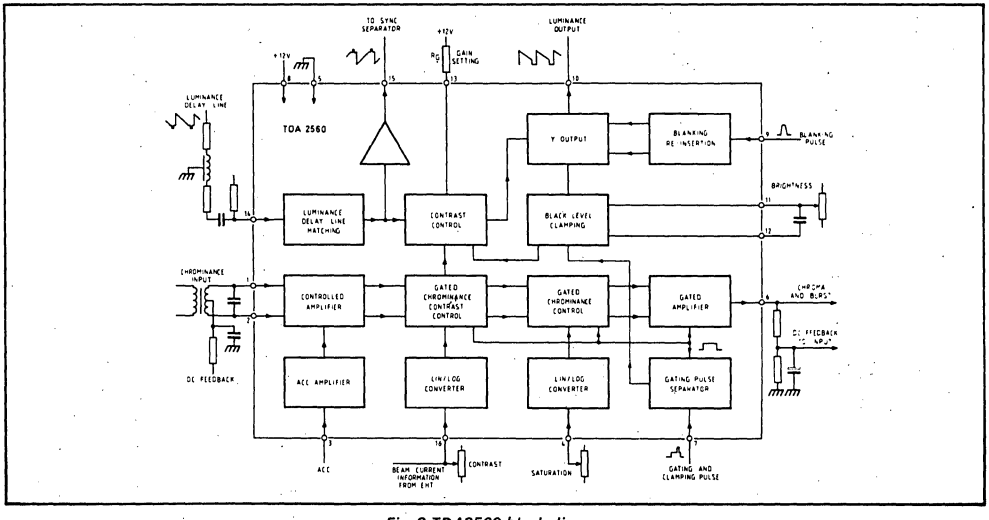


Fig. 2 TDA2560 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage (pin 8) = +12V
T_{amb} = +25°C
Gain setting resistor, R_G, (pin 13) = 2.7kΩ
Measurements referred to pin 5
Test circuit Fig. 5

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage range	8	10	12	14	V	
Supply current	8		45		mA	Load on pin 6 = 1.5kΩ no load on pins 10 and 15
Permitted supply line hum	8			100	mAp–p	
Luminance Amplifier						
Input signal current	14		0.2		mA	Black-to-white value
Input bias current	14		0.25		mA	
Input impedance	14		150		Ω	Input bias current = 0.25mA
Gain	13					See operating Note 1
Contrast control range		20			dB	
Contrast control voltage range	16					See Fig. 3
Contrast control current	16			8	μA	
Black level range	10	1		3	V	
Typical brightness control voltage range	11	1		3	V	
Brightness control current	11			20	μA	$V_{11} > 4V$
Black level temperature stability			0.1		mV/°C	
Black level stability when changing contrast						See functional description (pin 10)
Bandwidth (−3dB)		5			MHz	At nominal contrast (Max contrast setting −3dB)
Output voltage	10		3		V	Black-to-white value
Output to sync separator	15		3.4		Vp–p	I_{14} = 0.2mA black-to-white
Black level clamp pulse	7					See Operating Note 2
ON		7		V_8	V	
OFF				5	V	
Blanking pulse	9					See Operating Note 3
ON		2.5		4.5		For 0V on pin 10
OFF				1.5	V	
ON		6		V_8	V	For 1.5V on pin 10
OFF				4.5	V	
Chrominance Amplifier						See note 1
Input signal	2–1	4		80	mVp–p	
Chrominance output signal at nominal contrast and saturation level	6		2		Vp–p	See note 2
Max. chrominance output	6		4.6		V	
Bandwidth (−3dB)			6		MHz	
Ratio of burst and chrominance at nominal contrast and saturation						See Operating Notes 4 and 5
ACC starting voltage	3		1.2		V	See Operating Note 6
ACC range		30			dB	
Tracking between luminance and chrominance with contrast control			±1		dB	10dB control
Saturation control range		20			dB	
Saturation control voltage range	4					See Fig. 4
Gating pulse	7					
ON		2.3		5	V	
OFF				1	V	
Width		8			μs	
Signal-to-noise ratio		46			dB	
Phase shift between burst and chrominance				5	deg	

NOTES:
1. All figures for the chrominance signals are based on a colour bar signal with 75 per cent saturation: i.e. burst-to-chrominance ratio is 1 :2.
2. At a burst signal of 1V peak-to-peak: see also Operating Notes 4 and 5.

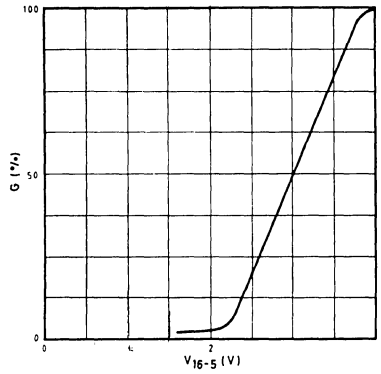


Fig. 3 Contrast control of luminance and chrominance amplifier

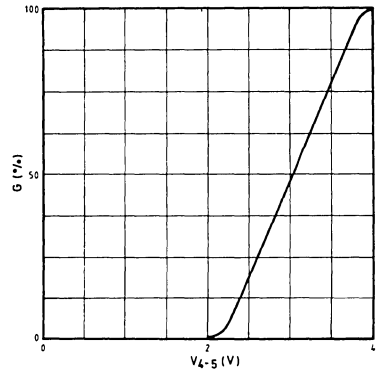


Fig. 4 Saturation control of chrominance amplifier

FUNCTIONAL DESCRIPTION

Functions listed by pin number.

1. and 2. Balanced chrominance input signal
This is derived from the chrominance signal bandpass filter, designed to provide a push-pull input. A signal amplitude of at least 4mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 will be 3V.

3. ACC input
A negative-going potential, starting at +1.2V, gives a 40dB range of ACC. Maximum gain reduction is achieved at an input voltage of 500mV.

4. Chrominance saturation control
A control range of +6dB to —14dB is provided over a range of DC potential on pin 4 from +2 to +4V. The saturation control is a linear function of the control voltage.

5. Negative supply (ground)

6. Chrominance signal output
For nominal settings of saturation and contrast controls (max. — 6dB for saturation, and max. —3dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The ACC circuit of the TDA2522 will hold the colour burst amplitude constant at the input of the TDA2522. As the PAL delay line is situated here between the TDA2560 and TDA2522 there may be some variation of the nominal 1V peak-to-peak burst output of the TDA2560, according to the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide DC negative feedback in the chroma channel via pins 1 and 2.

7. Burst gating and clamping pulse input
A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide (at least 8μs) at the actuating level of 2.3V.

8. +12V power supply
Correct operation occurs within the range 10 to 14V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this may be restricted due to consideration of tracking between the power supply variations and picture contrast and chroma levels.

9. Flyback blanking input waveform
This pin is used for blanking the luminance amplifier. When the input pulse exceeds the +2.5V level, the output signal is blanked to a level of about 0V. When the input exceeds a +6V level, a fixed level of about 1.5V is inserted in the output. This level can be used for clamping purposes.

10. Luminance signal output
An emitter follower provides a low impedance output signal of 3V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3V. An external emitter load resistor is not required.
The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12V supply. At an input bias current I_{14} of 0.25mA during black level the amplifier is compensated so that no black level shift more than 10V occurs at contrast control. When the input current deviates from the quoted value the black level shift amounts to 100mV/mA.

11. Brightness control
The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3V may be obtained.

12. Black level clamp capacitor

13. Luminance gain setting resistor
The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12V. Nominal luminance output amplitude is then 3V black-to-white at pin10 when this resistor is 2.7kΩ and the input current is 0.2mA black-to-white. Maximum and minimum values of this resistor are 3.9kΩ and 1.8kΩ.

14. Luminance signal input
A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0.2mA

black-to-white. The luminance signal may be coupled to pin 14 via a DC blocking capacitor and, in addition, a resistor employed to give a DC current into pin 14 at black level of about 0.25mA. Alternatively DC coupling from a signal source such as the TDA2541 may be employed.

15. Luminance signal output for sync separator purposes

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3.4V peak-to-peak when the luminance signal input is 0.2mA black-to-white.

16. Contrast control

With 3V on this pin the gain of the luminance channel is such that 0.2mA black-to-white at pin 14 gives a luminance output on pin 10 of 3V black-to-white. The nominal value of 2.7kΩ is then assumed for the resistor from pin 13 to the +12V supply. The variation of control potential at pin 16 from 2 to 4V gives —17 to +3dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.

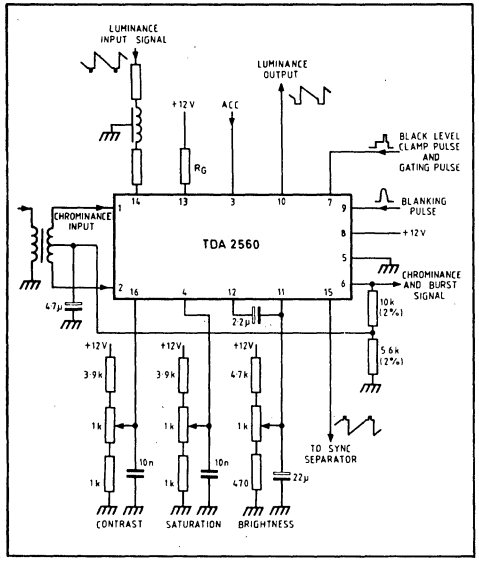


Fig. 5 Application and test circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltage	14V
Total power dissipation	930mW
Storage temperature	—55°C to +125°C
Operating ambient temperature	—10°C to +65°C

OPERATING NOTES

1. The gain of the luminance amplifier can be adjusted by setting the gain of the contrast control circuit with selection of the discrete resistor R_G (see Fig. 5). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is the spread of the ratio of the delay line matching resistors and the resistor R_G). At R_G = 2.7kΩ the output voltage at nominal contrast (maximum —3dB) is 3V black-to-white for an input current 0.2mA black-to-white.
2. The pulse applied to pin 7 is used for gating of the chrominance amplifier and black level clamping. The latter function is actuated at a +7V level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2.3V and switches it back to normal setting when the pulse falls below 1V.
3. The blanking pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds the 2.5V level the output signal is blanked to a level of about 0V. When the input exceeds a +6V level a fixed level of typ. +1.5V is inserted in the output signal. This level can be used for clamping purposes.
4. The chrominance and burst signal are both available on pin 6. The burst signal is not affected by the contrast and saturation control and is kept constant by the ACC circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for the insertion losses. This means that the output signal of the TDA 2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting the ratio of burst to chrominance signal at the output is typically indentical to that at the input.
5. Nominal contrast is specified as maximum contrast —3dB. Nominal saturation is specified as maximum saturation —6dB.
6. A negative-going control voltage gives a decrease in gain.

TDA2590

LINE OSCILLATOR COMBINATION

The TDA2590 is an integrated line oscillator circuit for colour television receivers using thyristor or transistor line deflection output stages.

The circuit incorporates a line oscillator which is based on the threshold switching principle, a line deflection output stage capable of direct drive of thyristor deflection circuits, phase comparison between the oscillator voltage and both the sync pulse and line flyback pulse. Also included on the chip is a switch for changing the filter characteristic and the gate circuit when used for VCR.

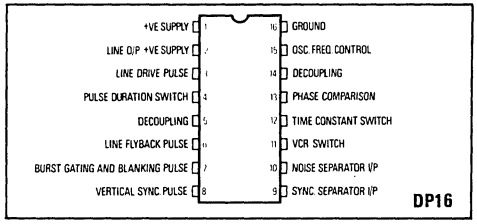


Fig. 1 Pin connections (top view)

FEATURES

- Coincidence Detector
- Sync Separator
- Noise Separator
- Vertical Sync Separator
- Colour Burst Keying
- Line Flyback Pulse Generator
- Output Pulse Phase Shifter
- Output Pulse Duration Switching
- Sync Gating Pulse Generator
- Low Supply Voltage Protection

QUICK REFERENCE DATA

- Supply Voltage (pin 1) 12V typ.
- Supply Current 30mA typ.
- Sync Separator Input (pin 9) 3V p-p typ.
- Pulse Duration Switch Input (pin 4)
  at t = 6μs 9.4V to V_1
  at t = 14μs + t_d 0V to 4V
- VCR Switch ON (pin 11) 0V to 1.5V and 9V to V_1

Output signal

- Vertical Sync Pulse (pin 8) 11V p-p (typ.)
- Burst Gating Pulse (pin 7) 11V p-p (typ.)
- Line Drive Pulse (pin 3) 10.5V p-p (typ.)

ABSOLUTE MAXIMUM RATINGS

Voltages	
Supply pin 1 (when supplied by the IC)	13.2V
Supply pin 2	18V
Pin 4	0V to 13.2V
Pin 9	−6V to +6V
Pin 10	−6V to +6V
Pin 11	0V to 13.2V
Currents	
Pin 2	400mA peak
Pin 3	400mA peak
Pin 4	1mA peak
Pin 6	10mA peak
Pin 7	10mA peak
Pin 11	2mA peak
Power dissipation	
Total power dissipation	800mW
Temperature	
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

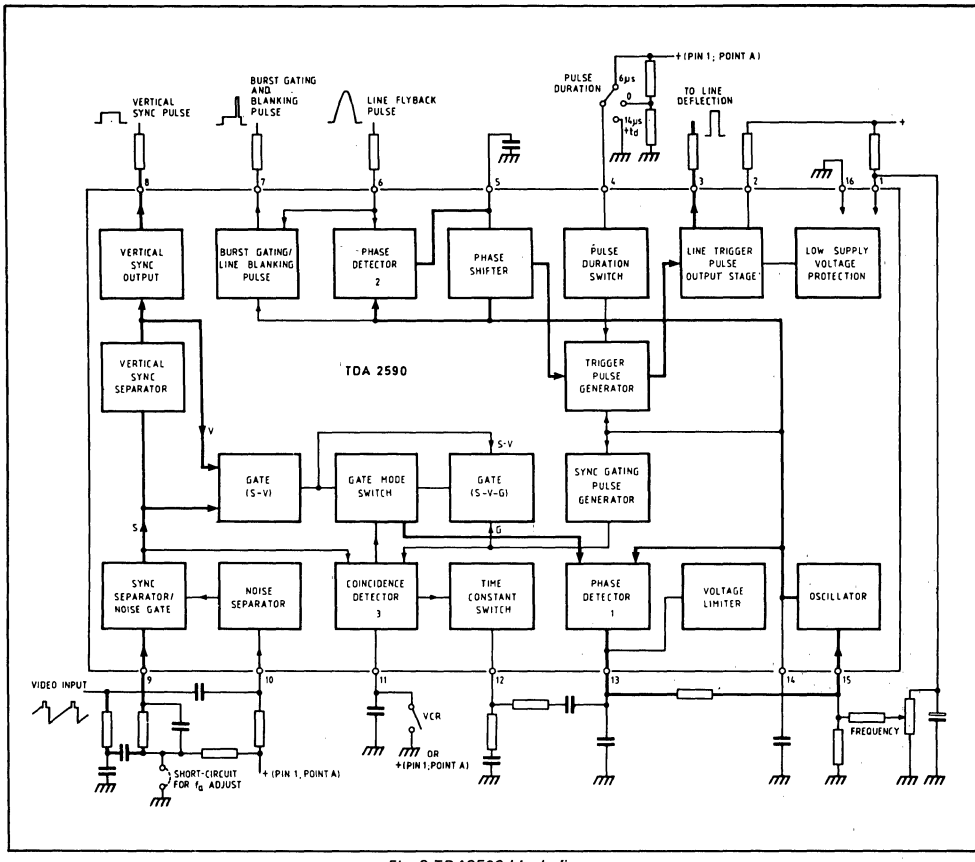


Fig. 2 TDA2590 block diagram

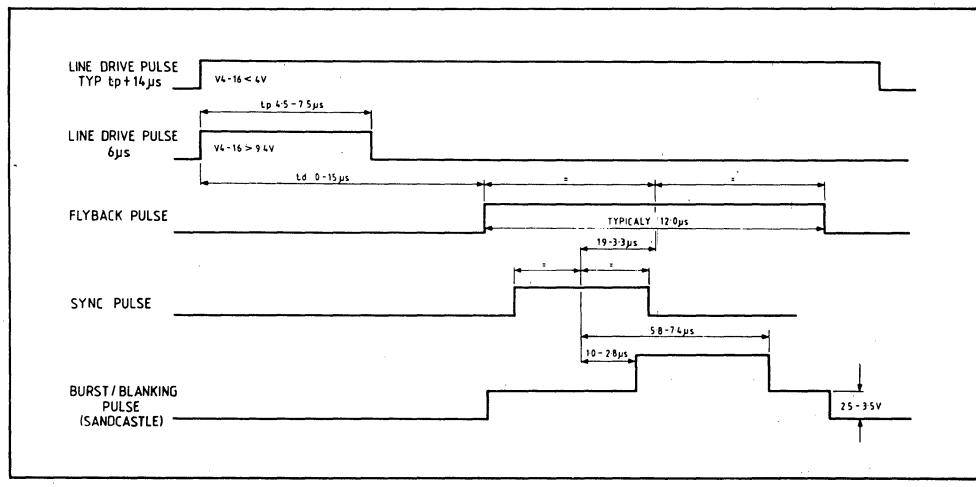


Fig. 3 TDA2590 timing relationships

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_1 = 12V$
$T_{amb} = +25°C$
Refer to timing diagram, Fig. 3 and Application circuit, Fig. 4
Voltages are referred to pin 6

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Sync separator	9					
Input switching voltage			0.8		V	
Input keying current		5		100	µA	
Input blocking current				1	µA	$V_9 = -5V$
Input switching current				5	µA	
Noise separator	10					
Input switching voltage			1.4		V	
Input keying current		5		100	µA	
Input switching current			150		µA	
Input blocking current				1	µA	$V_{10} = -5V$
Line flyback pulse	6					
Input current		10			µA	
Input switching voltage			1.4		V	
Input limiting voltage		−0.7		+1.4	V	
Input resistance			400		Ω	
Pulse duration switch	4					
Input voltage		9.4		V_1	V	$t = 6µs$
Input current		200			µA	
Input voltage		0		4.0	V	$t = 14µs + t_d$
Input current		200			µA	
Input voltage		5.4		6.5	V	$t = 0, V_3 = 0$
Input current (input open)			0		µA	See note 1
VCR switch	11					
Input voltage (typical range)		0		1.5	V	See note 2
		9		V_1	V	
Input current		200			µA	$V_{11} = 0V$ to 1.5V
Output current		1		2	mA	$V_{11} = 9V$ to V_1
Vertical sync pulse (positive going)	8					
Output voltage		10	11		Vp–p	
Output resistance			2		kΩ	
Burst gating pulse (positive-going)	7					
Output voltage		10	11		Vp–p	
Output resistance			400		Ω	
Blanking pulse	7					
Output voltage (typical range)		2.5		3.5	Vp–p	
Output resistance			400		Ω	
Line drive pulse (positive going)	3					
Output voltage			10.5		Vp–p	
Output current (average value)			100		mA	
Output resistance for leading edge of line pulse			2.5		Ω	
Output resistance for trailing edge of line pulse			20		Ω	
Oscillator	14					
Threshold voltage low level			4.4		V	
Threshold voltage high level			7.6		V	
Discharge current			0.47		mA	
Phase comparison ($ø_1$: sync pulse/oscillator)	13					
Control voltage range (typ)		3.8		8.2	V	
Control current		1.9	2.1	2.3	mAp–p	
Output blocking current				1	µA	$V_{13} = 4V$ to 8V
Output resistance		High (see note 3)				$V_{13} = 4V$ to 8V
		Low (see note 4)				$V_{13} < 3.8V$ or $> 8.2V$
Time constant switch	12					
Output voltage			6		V	
Output current				1	mA	
Output resistance			100		Ω	$V_{11} = 2.5V$ to 7V
			60		kΩ	$V_{11} < 1.5V$ or $> 9V$

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Coincidence detector (ϕ_3)	11					
Output voltage typical range		0.5		6	V	
Output current:						
without coincidence			0.1		mAp–p	
with coincidence			0.5		mAp–p	
Phase comparison (ϕ_2: oscillator/ line flyback pulse)	5					
Control voltage range (typ)		5.4		7.6	V	
Control current			1		mAp–p	
Output resistance		High (see note 3)				$V_5 = 5.4V$ to $7.6V$
			8		kΩ	$V_5 < 5.4V$ or $> 7.6V$
Input current at blocked phase detector				5	μA	$V_5 = 5.4V$ to $7.6V$
Applications (see Fig. 4)	9					
Sync separator						
Input voltage (negative video signal)		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Noise gating	10					
Input voltage		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Superimposed noise voltage				7	Vp–p	
Vertical sync pulse separator						
Delay between leading edge of input and output signal, t_{on}			12		μs	
Delay between trailing edge of input and output signal, t_{off}				t_{on}	μs	
Output voltage	8		11		Vp–p	
Output resistance	8		2		kΩ	
Oscillator						
Frequency: free running			15.625		kHz	$C_{14} = 4.7nF$, $R_{15} = 10k\Omega$
Spread of frequency, $\Delta f_o/f_o$				±5	%	See note 5
Frequency control sensitivity, $\Delta f_o/\Delta I_{15}$			31		Hz/μA	
Adjustment range of network in Fig. 2			±10		%	
Influence of supply voltage on frequency $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$				±0.05		See note 5, $V_1 = 12V$
Change of frequency when V_1 drops to 5V				±10	%	See note 5
Temperature coefficient of oscillator frequency per °C				$\pm 10^{-4}$		
Phase comparison (ϕ_1: sync pulse/oscillator)						
Control sensitivity			2		kHz/μs	
Catching and holding range (82kΩ between pins 13 and 15)			±780		Hz	$R_{13-15} = 82k\Omega$
Spread of catching and holding range			±10		%	See note 5
Phase comparison (ϕ_2: oscillator/ line flyback pulse)						
Permissible delay between leading edge of output pulse and leading edge of flyback pulse, Δtd		0		15	μs	
Static control error, td/td				0.2	%	
Overall phase relation See Note 6						
Phase relation between middle of sync pulse and the middle of the flyback pulse, t			2.6		μs	
Tolerance of phase relation Δt				0.7	μs	
Adjustment sensitivity of overall phase relation	5					
caused by: adjustment voltage $\Delta V_5/\Delta t$			0.1		V/μs	
adjustment current, $\Delta I_5/\Delta t$			30		μA/μs	

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Burst gating pulse						
Phase relation between middle of sync pulse at the input and the trailing edge of the burst gating pulse	7	5.8	6.6	7.4	µs	At 7V level
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse	7	1.0	1.9	2.8	µs	$V_7 = 7V$ At 7V level
Line drive pulse						
Output pulse duration, t_p for thyristor O/P	3	4·5	6.0	7.5	µs	$V_4 > 9.4V$
Output pulse duration, t_p for transistor O/P	3		14 + t_d		µs	$V_4 < 4V$, see note 7
Supply voltage for switching off the output pulse	1		4		V	
Internal gating pulse						
Pulse duration			7.5		µs	

NOTES
1. May also be left unconnected
2. VCR 'on' is normally achieved by connecting pins 11, via the VCR switch, to either ground or V_1
3. Current source
4. Emitter follower
5. Excluding external component tolerances
6. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase detector 2 (see Fig. 2)
7. t_d = switch-off delay of line output stage.

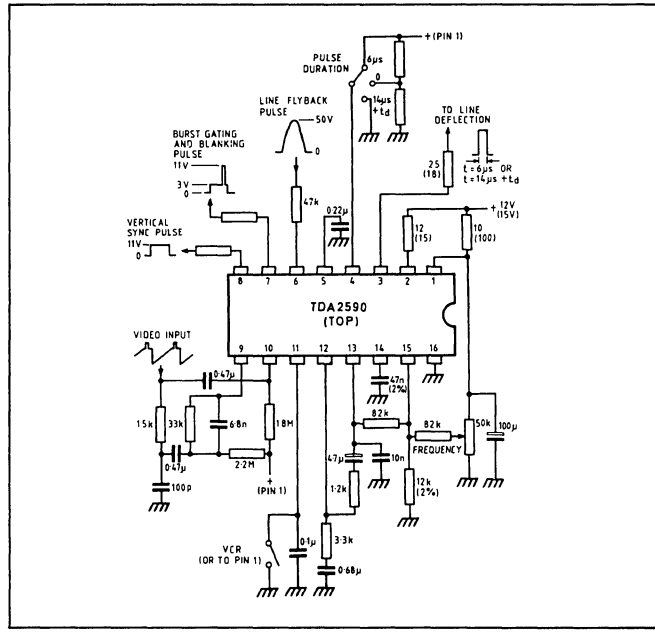


Fig. 4 Application and test circuit

TDA2591/3

LINE OSCILLATOR COMBINATION

The TDA2591 and TDA2593 are integrated line oscillator circuits for colour television receivers using thyristor or transistor line deflection output stages.

The circuits incorporate a line oscillator which is based on the threshold switching principle, a line deflection output stage capable of direct drive of thyristor deflection circuits, phase comparison between the oscillator voltage and both the sync pulse and line flyback pulse. Also included on the chip is a switch for changing the filter characteristic and the gate circuit when used for VCR.

The TDA2593 generates a sandcastle pulse (at pin 7) suitable for use with the TDA2532.

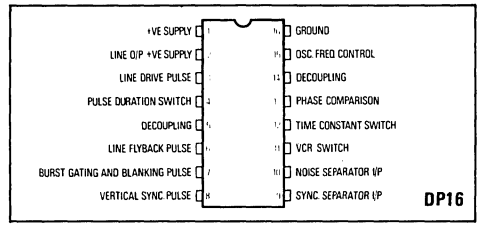


Fig.1 Pin connections (top view)

FEATURES

- Coincidence Detector
- Sync Separator
- Noise Separator
- Vertical Sync Separator
- Colour Burst Keying
- Line Flyback Pulse Generator
- Output Pulse Phase Shifter
- Output Pulse Duration Switching
- Sync Gating Pulse Generator
- Low Supply Voltage Protection

QUICK REFERENCE DATA

- Supply Voltage (pin 1) 12V typ.
- Supply Current 30mA typ.
- Sync Separator Input (pin 9) 3V p-p typ.
- Pulse Duration Switch Input (pin 4)
  at $t = 7\mu s$ 9.4V to V_1
  at $t = 14\mu s + t_d$ 0V to 4V
- VCR Switch ON (pin 11) 0V to 1.5V and 9V to V_1

Output signal

- Vertical Sync Pulse (pin 8) 11V p-p (typ.)
- Burst Gating Pulse (pin 7) 11V p-p (typ.)
- Line Drive Pulse (pin 3) 10.5V p-p (typ.)

ABSOLUTE MAXIMUM RATINGS

Voltages		
Supply pin 1 (when supplied by the IC)	13.2V	
Supply pin 2	18V	
Pin 4	0V to 13.2V	
Pin 9	−6V to +6V	
Pin 10	−6V to +6V	
Pin 11	0V to 13.2V	
Currents		
Pin 2	400mA peak	650mA thyristor drive only
Pin 3	400mA peak	650mA thyristor drive only
Pin 4	1mA peak	
Pin 6	10mA peak	
Pin 7	10mA peak	
Pin 11	2mA peak	
Power dissipation		
Total power dissipation	800mW	
Temperature		
Storage temperature	−55°C to +125°C	
Operating ambient temperature	−10°C to +60°C	

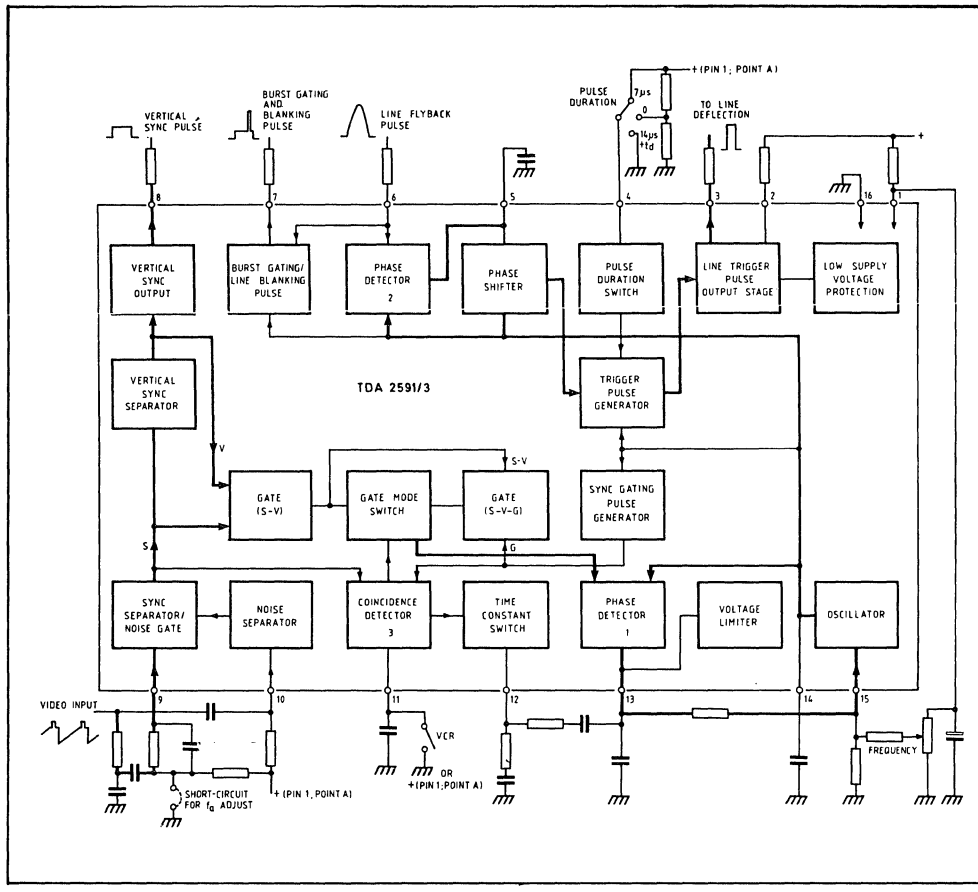


Fig. 2 TDA2591/3 block diagram

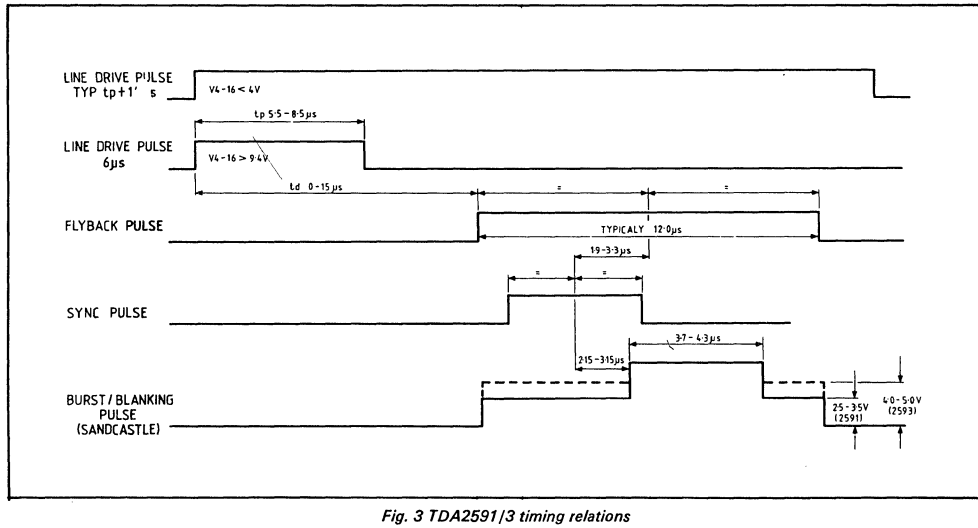


Fig. 3 TDA2591/3 timing relations

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage, $V_1 = 12V$
$T_{amb} = +25°C$
Refer to timing diagram, Fig. 3 and Application circuit, Fig. 4
Voltages are referred to pin 6

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Sync separator	9					
Input switching voltage			0.8		V	
Input keying current		5		100	µA	
Input blocking current				1	µA	$V_9 = -5V$
Input switching current				5	µA	
Noise separator	10					
Input switching voltage			1.4		V	
Input keying current		5		100	µA	
Input switching current			150		µA	
Input blocking current				1	µA	$V_{10} = -5V$
Line flyback pulse	6					
Input current		10			µA	
Input switching voltage			1.4		V	
Input limiting voltage		−0.7		+1.4	V	
Input resistance			400		Ω	
Pulse duration switch	4					
Input voltage		9.4		V_1	V	$t = 7µs$
Input current		200			µA	
Input voltage		0		4.0	V	$t = 14µs + t_d$
Input current		200			µA	
Input voltage		5.4		6.5	V	$t = 0, V_3 = 0$
Input current (input open)			0		µA	See note 1
VCR Switching	11					
Input voltage (typical range)		0		1.5	V	See note 2
		9		V_1	V	
Input current		200			µA	$V_{11} = 0V$ to 1.5V
Output current		1		2	mA	$V_{11} = 9V$ to V_1
Vertical sync pulse (positive going)	8					
Output voltage		10	11		Vp–p	
Output resistance			2		kΩ	
Burst gating pulse (positive-going)	7					
Output voltage		10	11		Vp–p	
Output resistance			400		Ω	
Blanking pulse	7					
Output voltage (typical range) 2591		2.5		3.5	Vp–p	
Output voltage (typical range) 2593		4.0		5.0	Vp–p	
Output resistance			400		Ω	
Line drive pulse (positive going)	3					
Output voltage			10.5		Vp–p	
Output current (average value)			100		mA	
Output resistance for leading edge of line pulse			2.5		Ω	
Output resistance for trailing edge of line pulse			20		Ω	
Oscillator	14					
Threshold voltage low level			4.4		V	
Threshold voltage high level			7.6		V	
Discharge current			0.47		mA	
Phase comparison ($ø_1$: sync pulse/oscillator)	13					
Control voltage range (typ)		3.8		8.2	V	
Control current		1.9	2.1	2.3	mAp–p	
Output blocking current				1	µA	$V_{13} = 4V$ to 8V
Output resistance		High (see note 3)				$V_{13} = 4V$ to 8V
		Low (see note 4)				$V_{13} < 3.8V$ or $> 8.2V$
Time constant switch	12					
Output voltage			6		V	
Output current				1	mA	
Output resistance			100		Ω	$V_{11} = 2.5V$ to 7V
			60		kΩ	$V_{11} < 1.5V$ or $> 9V$

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Coincidence detector (ϕ_3)	11					
Output voltage typical range		0.5		6	V	
Output current:						
without coincidence			0.1		mAp–p	
with coincidence			0.5		mAp–p	
Phase comparison (ϕ_2: oscillator/ line flyback pulse)	5					
Control voltage range (typ)		5.4		7.6	V	
Control current			1		mAp–p	
Output resistance		High (see note 3)				$V_5 = 5.4V$ to 7.6V
			8		kΩ	$V_5 < 5.4V$ or $> 7.6V$
Input current at blocked phase detector				5	μA	$V_5 = 5.4V$ to 7.6V
Applications (see Fig. 4)	9					
Sync separator						
Input voltage (negative video signal)		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Noise gating	10					
Input voltage		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Superimposed noise voltage				7	Vp–p	
Vertical sync pulse separator						
Delay between leading edge of input and output signal, t_{on}			12		μs	
Delay between trailing edge of input and output signal, t_{off}				t_{on}	μs	
Output voltage	8		11		Vp–p	
Output resistance	8		2		kΩ	
Oscillator						
Frequency: free running			15.625		kHz	$C_{14} = 4.7nF$, $R_{15} = 10k\Omega$
Spread of frequency, $\Delta f_o/f_o$				±5	%	See note 5
Frequency control sensitivity, $\Delta f_o/\Delta I_{15}$			31		Hz/μA	
Adjustment range of network in Fig. 2			±10		%	
Influence of supply voltage on frequency $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$				±0.05		See note 5, $V_1 = 12V$
Change of frequency when V_1 drops to 5V				±10	%	See note 5
Temperature coefficient of oscillator frequency per °C				$\pm 10^{-4}$		
Phase comparison (ϕ_1: sync pulse/oscillator)						
Control sensitivity			2		kHz/μs	
Catching and holding range (82kΩ between pins 13 and 15)			±780		Hz	$R_{13-15} = 82k\Omega$
Spread of catching and holding range			±10		%	See note 5
Phase comparison (ϕ_2: oscillator/ line flyback pulse)						
Permissible delay between leading edge of output pulse and leading edge of flyback pulse, Δtd		0		15	μs	
Static control error, td/td				0.2	%	
Overall phase relation See Note 6						
Phase relation between middle of sync pulse and the middle of the flyback pulse, t			2.6		μs	
Tolerance of phase relation Δt				0.7	μs	
Adjustment sensitivity of overall phase relation	5					
caused by: adjustment voltage $\Delta V_5/\Delta t$			0.1		V/μs	
adjustment current, $\Delta I_5/\Delta t$			30		μA/μs	

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Burst gating pulse						
Pulse width	7	3.7	4.0	4.3	µs	At 7V level
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse	7	2.15	2.65	3.15	µs	$V_7 = 7V$ At 7V level
Line drive pulse						
Output pulse duration, t_p	3	5.5	7.0	8.5	µs	$V_4 > 9.4V$
	3		$14 + t_d$		µs	$V_4 < 4V$, see note 7
Supply voltage for switching off the output pulse	1		4		V	
Internal gating pulse						
Pulse duration			7.5		µs	

NOTES
1. May also be left unconnected
2. VCR 'on' is normally achieved by connecting pins 11, via the VCR switch, to either ground or V_1
3. Current source
4. Emitter follower
5. Excluding external component tolerances
6. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase detector 2 (See Fig. 2)
7. t_d = switch-off delay of line output stage.

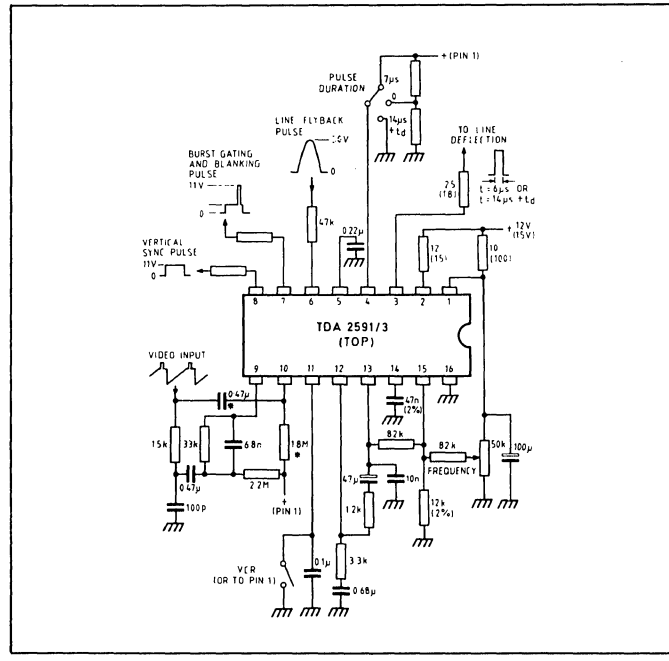
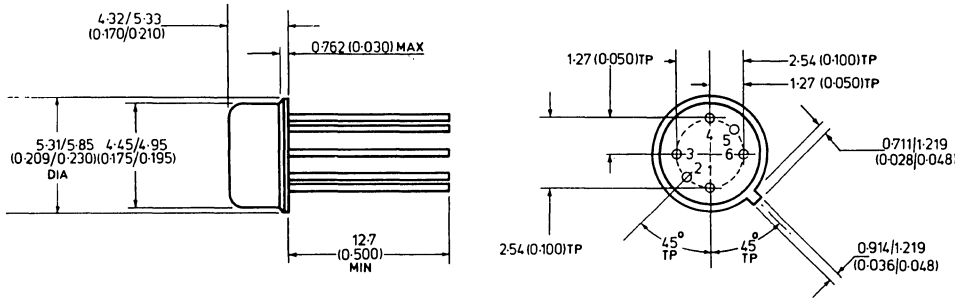


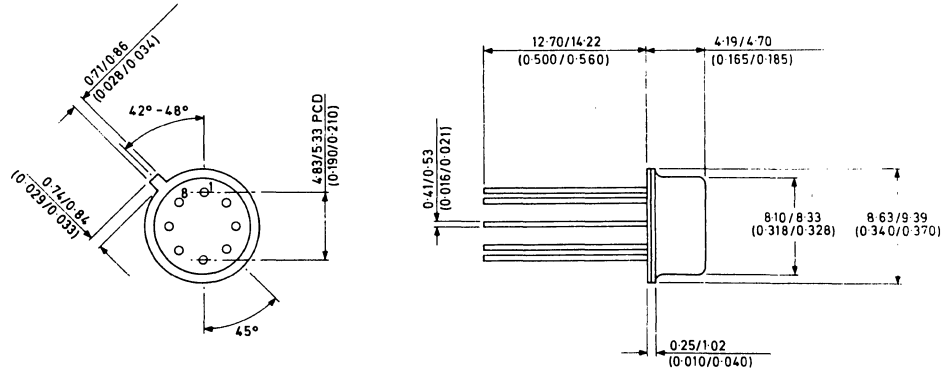
Fig. 4 Application and test circuit

8. PACKAGES



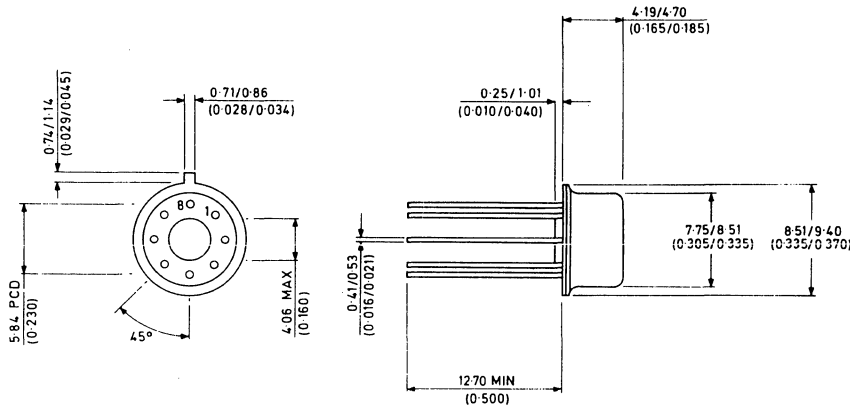
6 LEAD TO-71

CM6



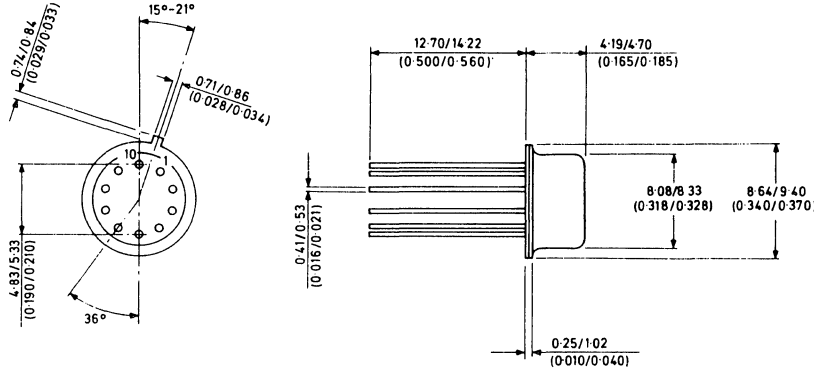
8 LEAD TO-5 (5·08mm PCD)

CM8



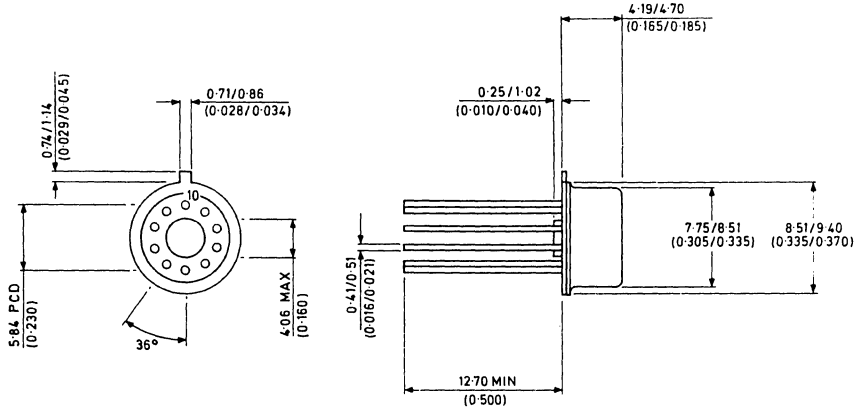
8 LEAD TO-5 (5·84mm PCD) WITH STANDOFF

CM8



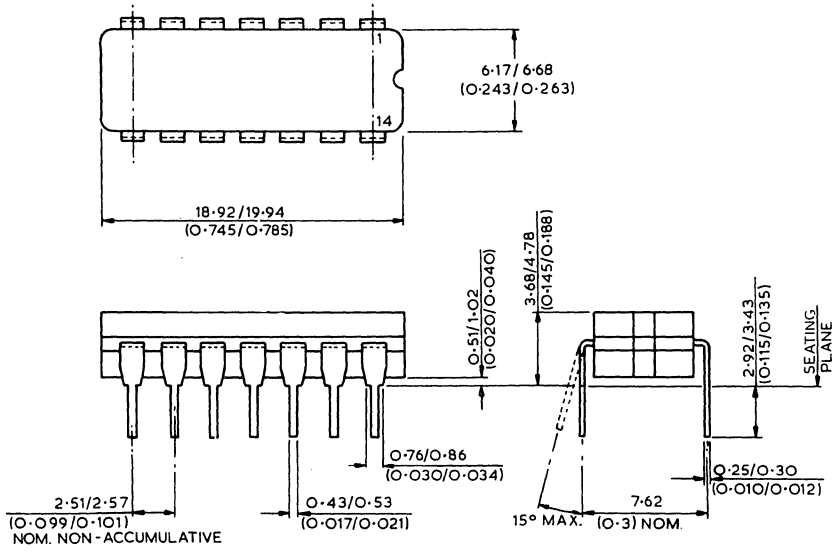
10 LEAD TO-5

CM10



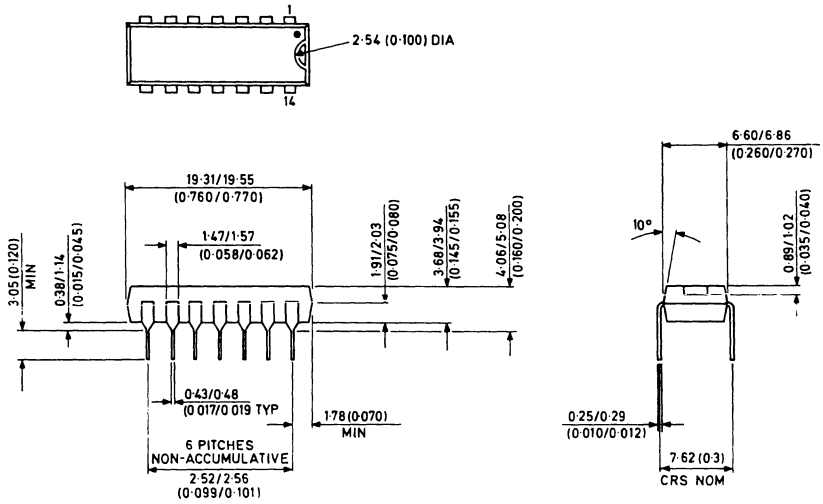
10 LEAD TO-100 (5·84 mm PCD) WITH STANDOFF

CM10



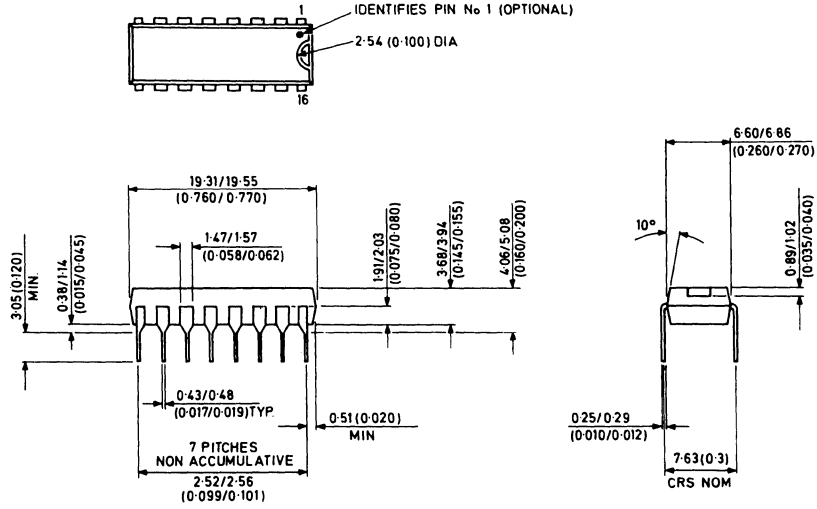
DG14

14 LEAD CERAMIC D.I.L.



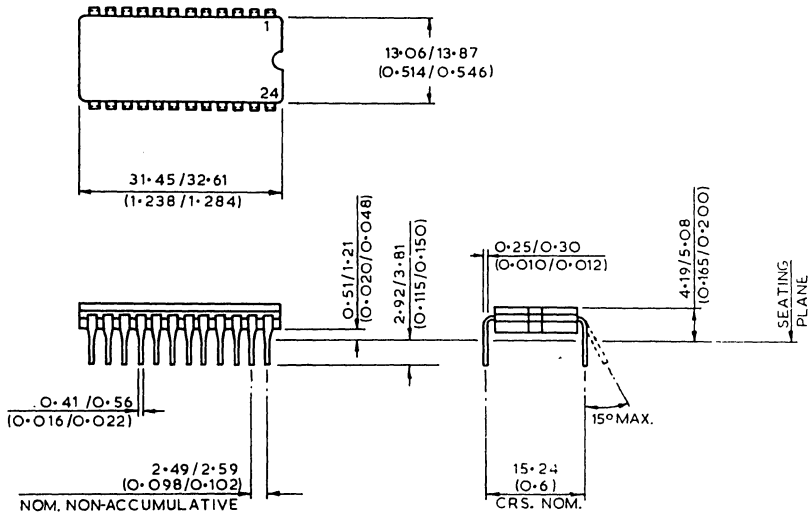
14 LEAD PLASTIC D.I.L.

DP14

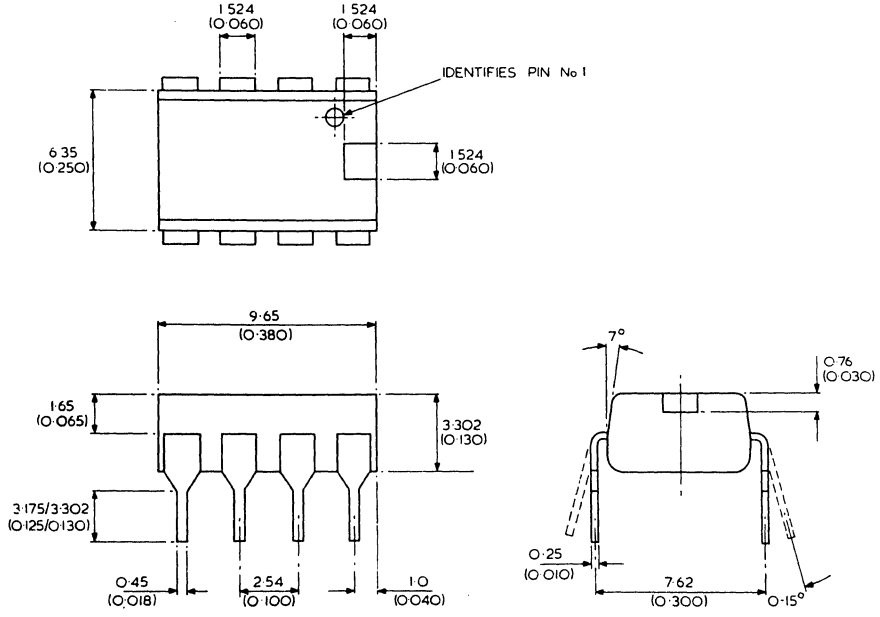


16 LEAD PLASTIC DIL

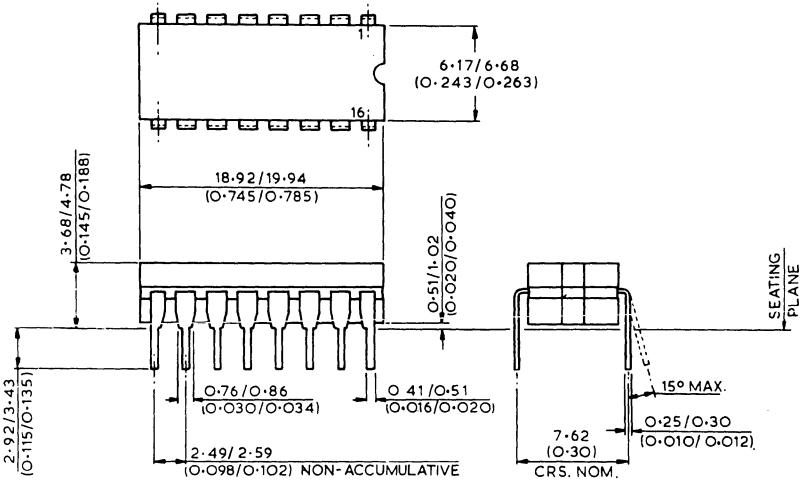
DP16



DG24 24 LEAD CERAMIC D.I.L.

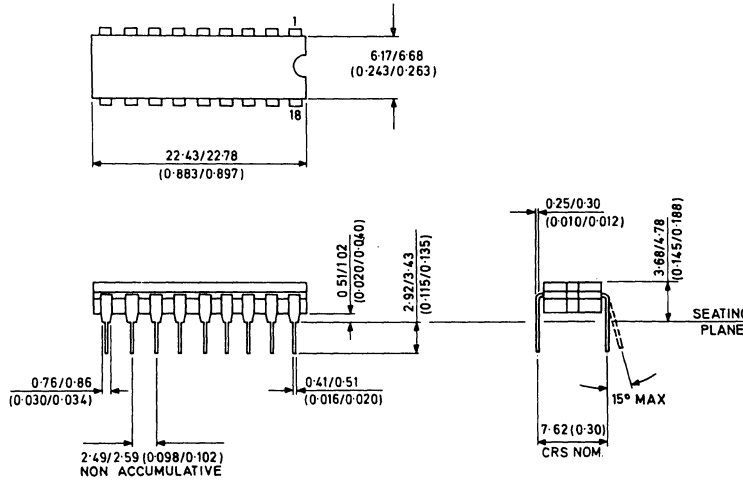


DP8 8 LEAD PLASTIC D.I.L.



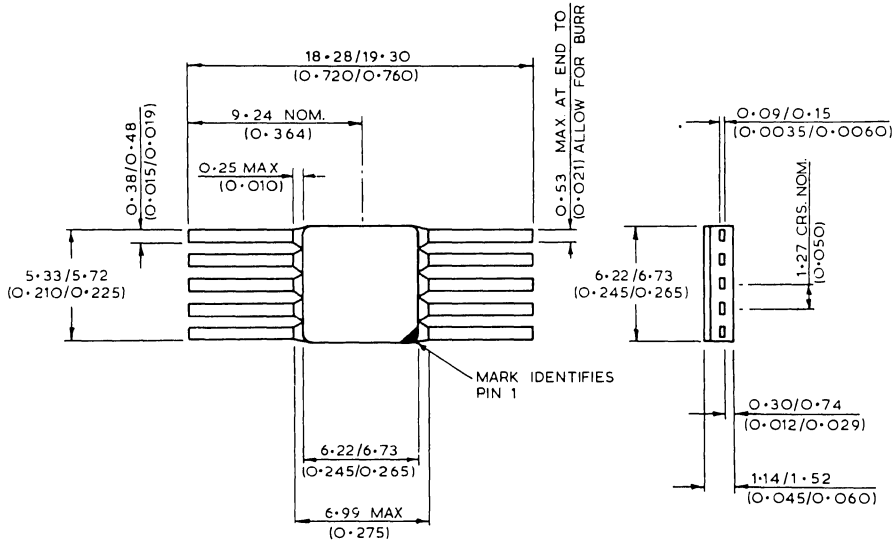
16 LEAD CERAMIC D.I.L.

DG16

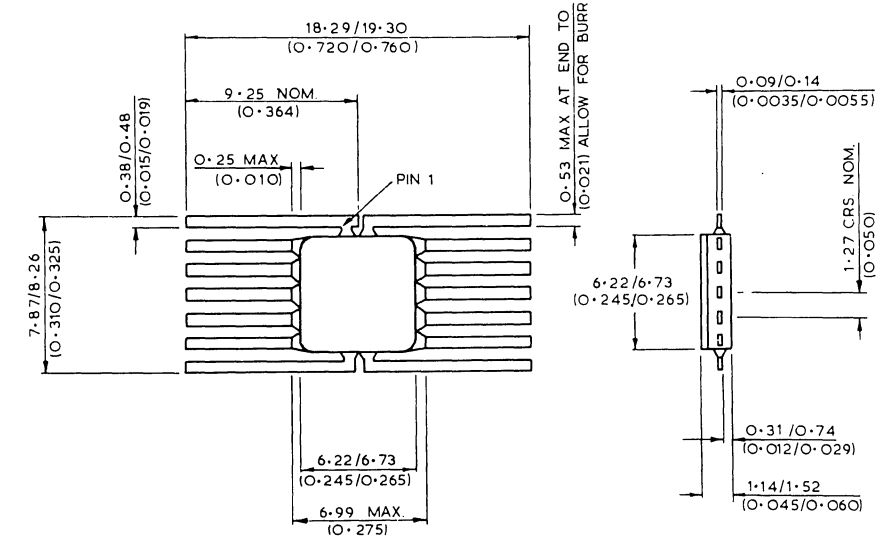


18 LEAD CERAMIC DIL

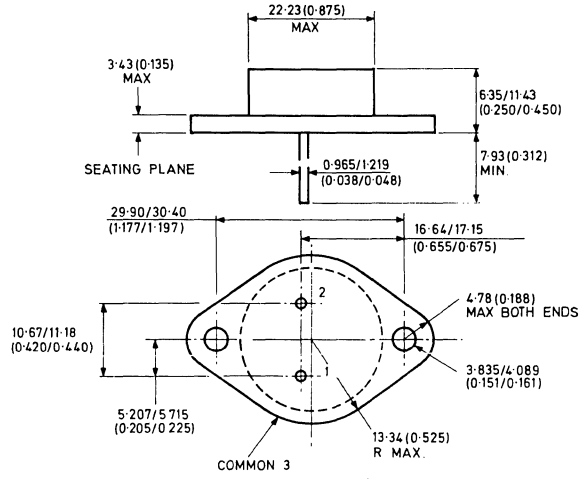
DG18



GM10 10 LEAD FLAT PACK



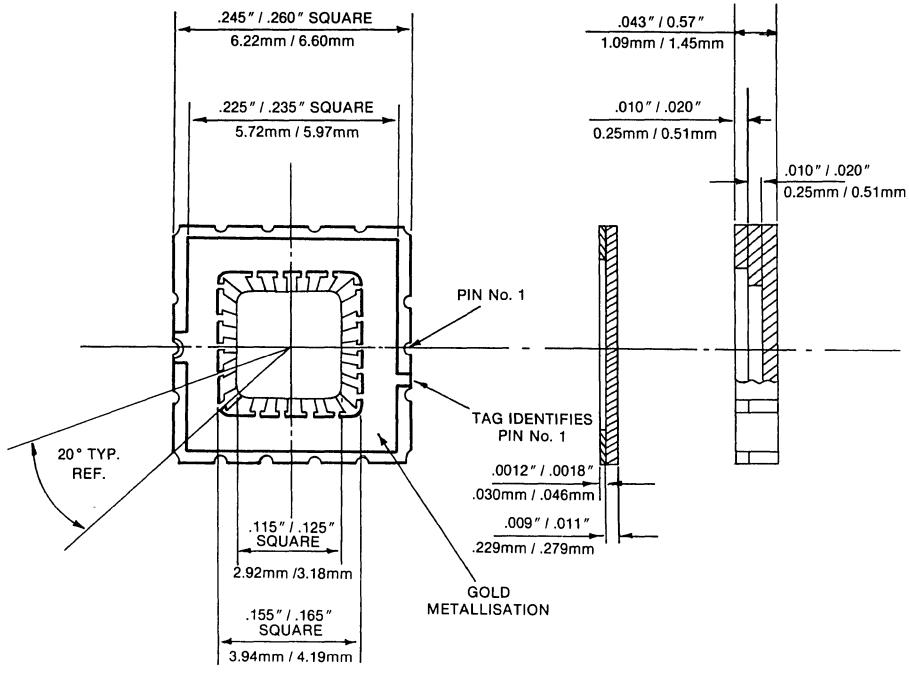
GM14 14 LEAD FLAT PACK



NOTE : CASE IS THIRD ELECTRICAL CONNECTION

TO-3

KM 3



18 LEAD LEADLESS CARRIER

GC 18

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