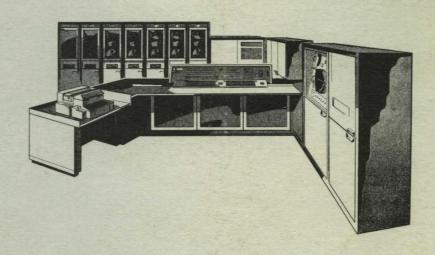
W.A. WELCH

SERIAL NO.

PHILCO 2000 SYSTEM
COMPUTER, MODEL 210

MEMORY, SERIES 2200
PART II



PHILCO CORPORATION

GOVERNMENT AND INDUSTRIAL GROUP • COMPUTER DIVISION 3900 WELSH ROAD, WILLOW GROVE, PENNSYLVANIA

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1. TRANSISTOR SWITCHING CIRCUITS

1.1 INTRODUCTION

PHILCO 2000 uses all transistor logical circuitry. Accordingly, a good working knowledge of the operation of transistor digital circuits is essential to anyone maintaining the machine.

This section will describe in detail a theory of transistor operation, leading through transistor digital circuits, S-2000 logical circuits and hardware arrangement. A theory of transistor operation is presented to give some insight which may help to understand why transistor circuits behave as they do. Also described are special driver circuits, A.C. distribution and control scheme and the D.C. transistor power supplies.

The discussion of transistor operation will concern principally the germaium junction type of transistor. Operation of the junction transistor is essentially similar to the surface barrier type used in S-2000.

1.2 PRINCIPLES OF TRANSISTOR SWITCHING

A transistor at first examination appears to be nothing more than two semiconductor diodes (rectifiers) connected back to back. Therefore, the study may reasonably begin with the basic P-N junction which forms a semiconductor diode. Following will be an extension to transistor operation and then a study of basic amplifier circuits.

P-N JUNCTION

The basic diode junction might be loosely defined as an area where in nearly pure germanium changes in impurity concentration in a very specific manner. Minute concentrations of impurities in germanium material have a profound effect upon its conducting ability.

GERMANIUM PROPERTIES

Germanium is classed as a semiconductor material.

Apparently it is neither a good conductor nor a good insulator. Metals, being good conductors, are characterized by the presence of many free electrons due to their atomic structure. Conversely, good insulators have

practically no free electrons because the electrons are tightly bound by an interatomic relationship. A semiconductor material has its electron bonds relatively easily broken by heat energy so that it has appreciable conduction at room temperature. The number of free electrons which may be found is a function of temperature and increases with increasing temperature.

Atoms of a material are held together because they tend to share electrons so that the imperfection of each atom is complemented by adjacent atoms. Thus, pure germanium with four electrons of the eight electrons needed to fill the outer electron shell is bound in a crystaline lattice structure similar to a diamond (carbon). Each atom shares the electrons with its neighbor.

However, as stated above, at room temperature germanium is observed to be a reasonably good conductor. Not all of the electrons are bound in the crystaline lattice. Due to temperature agitation many are able to escape. The free electrons can serve as a means of conducting current. If a voltage is applied across the crystal so that an electric field is set up within the crystal the electrons will drift toward the positive electrode. Electrons pass into the positive electrode from the crystal and are supplied to the crystal from the negative electrode. So far the discussion sounds very similar to current condution through a wire. The difference is that those electrons existing in the crystal are thermally generated.

Generation of a free electron from the interatomic structure implies that a vacancy must exist in the atomic lattice due to departure of the electron from the structure. This vacancy called a "hole" has a positive charge equivalent to the charge of the missing electron. Moreover, this hole is free to move through the crystal. Motion is accomplished by filling the vacancy from an adjacent atom thereby creating a new hole as a result of eliminating the former one. Now to embellish the picture above a little more, let us assume that a voltage is applied as above. Electron flow is from the crystal to the positive electrode. Hole movement is toward the negative electrode because electrons are supplied at that point.

The concept of electron and hole conduction is a very important concept for the understanding of transistor operation. Already familiar is the concept of electron flow normally used for vacuum tubes where current flow is known to exist almost entirely by means of electrons. Less sophisticated scientists years ago admittedly did not know which polarity the current carriers had nor were they sure that current was carried by only one type of carrier. Their choice of "conventional flow

(from the positive source) has been used successfully to explain, in a consistant manner, most of the phenomena found in electrical science. "Electron" flow may be employed with equal success. We may conclude that the choice of current flow, no matter how absurd it may seem, in view of actual physical theory, may be a very satisfactory tool for understanding. Moreover, since the electrons or holes or whatever there are never become confused by man's conventions, we are relatively free to select any convention we wish as long as it is applied in exactly the same manner each time and the results are predicted with accuracy. In this discussion as in any other such discussion of semiconductors, the use of two current carriers or "carriers" (electrons and holes) makes the understanding of transistor operation much simpler. Scientists have found that the two carriers actually have some distinctive individual characteristics although they differ essentially only in the matter of polarity.

The conducting ability of germanium at a given temperature may be enhanced by the addition of minute quantities of impurities into the crystaline structure.

DOPING TO GIVE N TYPE OR P TYPE MATERIAL

A number of chemical elements are similar to germanium (such as carbon above). Also a number of chemical elements have five of the eight electrons needed to fill the outer shell and there are chemical elements having three of the eight electrons.

Suppose one such element, Arsenic, is added to the germanium lattice. Arsenic is a material having five electrons in its outer electron shell. In the lattice four of its five electrons complete the interatomic structure of the crystal. The fifth atom is free to move in a random fashion because it is not required by the lattice of the crystal. The crystal conduction is improved because of the free electrons thus made available. The crystal is called "N" type because it can act as a donor of electrons.

Suppose, instead, that Indium is added to the germanium lattice. Indium is a material having three electrons in its outer electron shell. In the lattice all three of its electrons are used and a vacancy exists as well. This vacancy is usually termed a "hole". The crystal is called "P" type because it can act as an acceptor of free electrons. The crystal conduction is improved because electrons can be supplied externally at one contact point and removed at another contact point. Conduction may be assumed to occur by holes rather than electrons.

One must realize that there are always two types of carriers present in a particular structure (N or P type) simultaneously.

One carrier is the "majority" carrier due to doping as discussed. "The other carrier is the "minority" carrier due to breaking of the bonds to thermally. Thus pure germanium at some temperature above absolute zero will have an equal number of carriers (holes and electrons). Doped germanium at the same temperature will have the same total number of carriers but the largest number of them will be either holes or electrons depending upon how the material was doped.

SURFACE CHARACTERISTICS

As just discussed, doping of the germanium can produce either N or P type material. Both N and P type characteristics can be found in a crystal of N type germanium near the surface of the crystal. As discussed above, sharing of electrons completes the outer electron shell of each atom with eight electrons, a full shell. However, near the surface of the crystal there are no adjacent atoms from which to borrow electrons. Electrons are drawn from the internal body of the N type crystal to help complete these shells. After some of the closer electrons have moved to the surface, a net negative charge accumulates near the surface tending to repel any further electrons so that a barrier is set up. Thus on the surface side of the barrier a predominantly acceptor material exists (holes) and on the crystal side of the barrier a predominantly donor material exists (electrons). This mechanism for hole production is important for the surface barrier transistor but is not used in the junction transistor.

Having understood the concept of hole and electron carriers, one is ready to study rectifier action of the junction

UNIDIRECTIONAL CONDUCTION

More precisely defined, a junction is the area where in the donor-acceptor concentration of the germanium changes in a specific manner. The rectifying junction is contained in a single crystal of material. The donor to acceptor concentration changes across the junction from P type to N type. The change may be abrupt or gradual with minor significance in regard to operation but is generally considered to be abrupt for purpose of explanation.

Assume such a junction as shown in Figure 1-1, last page of this chapter. With voltage applied across the junction having the indiscated polarity the N type region is made negative with respect to the P type region. Free electrons and holes (majority) carriers are swept to-

ward the junction from N and P type material respectively and cross it to combine. Since there are a large number of current carriers moving across the junction, the resistance of the junction is very low. The voltage drop across the junction is typically a fraction of a volt. Only the majority carriers are important here.

If the applied voltage is reversed, the minority carriers become important.

LEAKAGE CURRENT

With voltage applied as in Figure 1-2, the majority carriers are drawn away from the junction. However, the minority carriers (generated by thermal agitation) tend to move to the junction where they recombine. Thus a small "leakage" current flows. This current tends to remain nearly constant without any relation to the applied voltage (if greater than about -0.1 volt) until a point is reached where current increases rapidly as voltage is increased. This is the breakdown point and the voltage is called the breakdown voltage of the junction. The most common mechanism of breakdown is by avalanche where collisions of carriers and atoms results in generation of additional carriers due to the large energy supplied to the original carriers.

Since the minority carriers result from thermal agitation, leakage increases as the temperature increases. Moreover, leakage does not increase directly with temperature but rather very much more rapidly (nearly doubles with each 10° C increase). For this reason, careful attention to the ambient temperature of any junction is extremely important. While careful circuit design may allow a relatively wide range of temperature, a germanium diode or transistor becomes relatively useless in the region above about 75° C because of leakage current. Silicon types are usable somewhat above 125° C. Typical designs with germanium material permit operation around 40 to 50° C maximum where no special attention is given to temperature compensation. S-2000 has no special temperature componsating circuit design because the ambient temperature is not expected to become excessive.

TRANSISTOR ACTION

The junction transistor is essentially two P-N junctions back-to-back with a region common to both junctions. They may be arranged P-N-P or N-P-N depending upon the manufacturing technique

and the circuit requirements. Operation of the two types is essentially the same. The P-N-P is the more common type. The following explanation applies also to N-P-N junction transistors if the terms "electrons" and "holes" are interchanged.

TRANSISTOR OPERATION

Shown in Figure 1-3 is the arrangement and symbol for the P-N-P junction transistor. External circuit connections are such that the left hand junction is usually forward biased (electron flow is from base to emitter). In other words the emitter and base are functioning as a junction diode in its forward conducting direction. The collector and base junction is reverse-biased so that leakage current would flow. However, one osbserves a much larger current than that due to leakage alone. The explanation is that not all of the carriers entering the base region from the emitter recombine in the base. Most of the carriers diffuse across the base and enter the collector region due to the electric field set up by the reverse collector-sbase bias. The carriers crossing into the collector are minority carriers in the collector region. As previously discussed, these carriers recombine in the collector region and provide current flow through the base-collector junction. There are two components of collector current: (1) that due to leakage of the reverse biased collector-base junction and (2) and that due to holes emitted from the emitter which survive the trip across the base region and enter the collector.

Obviously not all of the holes can cross the base. Some are bound to recombine in the base region. However, 98% to 99% of them are successful as a rule. The base region is very narrow so that carriers stand an excellent chance of crossing without recombining.

To summarize, the emitter-base junction is forward biased to a varying degree by controlling the current flow for the purpose of injecting holes into the base region; the collector-base junction is reverse biased for the purpose of collecting nearly all of the emitted holes. Power amplification occurs because the forward voltage drop of the emitter-base junction is very small (usually a few tenths of a volt) whereas the collector-base voltage is comparatively high (limited only by the breakdown voltage of the junction). Thus the product of collector voltage and current is higher than the product of emitter voltage and current even though the emitter current is a little greater than the collector current.

Transistors have some terms applied to them which are similar to vacuum tube terminology. A transistor is "cut-off" when only leakage current flows across the collector-base junction. This corresponds to minimum emitter-base current or a reverse biased emitter-base junction. A P-N-P transistor is "saturated" when holes are injected into the base region much more rapidly than they can be removed by the available collector current. The "dissipation" of a transistor is approximately the product of the collector-base voltage and the collector current. Both "cut-off" and "saturation" conditions provide the minimum dissipation for a transistor. At "cut-off", the collector current is very small. At "saturation", the collector-base voltage is very small (a few tenths of a volt). Thus for digital applications (on-off) a small transistor may operate a load in watts many times greater than its maximum dissipation (15 or 20 times). Such a feat could hardly be expected from vacuum tubes. Because drift due to changing leakage current can be effectively "designed out" of digital circuitry and because of its high efficiency as an electronic switch the transistor is ideally suited to digital circuits with one qualification. It should always operate in the region where it is either close to "cut-off" or "saturation". Otherwise depending upon circuit design, dissipation may become excessive and prevent proper operation of the circuit and possible destruction of the transistor.

SURFACE BARRIER TRANSISTOR

The surface barrier has the same characteristics as any other P-N junction. Only the method of carrier production is different. Thus when the emitter-base junction is forward biased, holes are repelled from the barrier region into the crystal by the metalic electrode attached to the crystal. Similarly to the junction transistor, the injected holes diffuse across the narrow base region to recombine at the collector surface barrier or junction.

TIME CONSIDERATIONS

The speed of response of a transistor circuit is dependent upon the particular transistor employed and the circuits into which it is designed. In general, the larger transistors are relatively slower in speed of response than the smaller transistors. One of the most significant problems in digital circuits is the phenomena of minority carrier storage in the base region when the transistor is operated in a saturated mode. Because holes are being injected into the base region faster than the collector can remove them, they tend to accumulate to some degree with

time. Then when the transistor is switch off by reducing the emitter base current, the collector current continues until the minority carriers are all swept out by the collector.

TRANSISTOR AMPLIFIER-SWITCH

As discussed above, the transistor is a highly efficient switch and provides power amplification as well. One may show many similarities to vacuum tube circuit arrangements. However, there are some striking differences as well. Following is a discussion of the basic circuits compared and contrasted with vacuum tube equivalent circuits.

TRANSISTOR INVERTER

Figure 1-4 shows a transistor inverter circuit and a vacuum tube inverter circuit arranged to operate in substantially the same manner. The principal difference is that the transistor is controlled by current supplied to the base such that the emitter-base junction is forward biased whereas the vacuum tube is controlled by the voltage applied between the cathode and the grid. Assume both the transistor and the tube are "cutoff". This would be obtained by a negative signal on the grid for the tube. The transistor would be cut-off by a slightly positive voltage from base to emitter. Output terminal (a) is at the same potential as the supply voltage. If a positive going signal is applied to the grid of the tube (relative to ground) such that the effect of the previous negative signal is cancelled, the tube conducts heavily and terminal (a) changes to a very small value of voltage. Similarly as the base of the transistor has applied a negative going signal: such that emitter base current flows, increased current flow through the transistor changes the potential of terminal (a) to a very small value of voltage.

Since the tube is made "active" or conducting by the positive signal which in turn causes the tube output load voltage to be less positive, the tube circuit is termed an inverter. Similarly the transistor is an inverter because a negative signal caused the output of the transistor circuit to be less negative. A "grounded cathode" tube circuit is thus shown to be nearly equivalent of a "grounded emitter" transistor circuit in function. There are two differences in the circuits shown, the P-N-P transistor operates with negative going signals instead of positive going signals and current <u>must</u> be supplied to control a transistor.

The control current required by the transistor is typically

about 1/20 to 1/50 of the load current it switches in a grounded emitter configuration although in some particular transistors a much smaller current may be adequate.

Although there are a variety of different circuit equivalents between the two devices, the only other one here considered is the emitter follower transistor circuit and its vacuum tube equivalent.

TRANSISTOR EMITTER FOLLOWER

The "emitter follower" transistor circuit is very similar to the vacuum tube "cathode follower" circuit, (See Figure 1-5). The cathode of the vacuum tube tends to follow any variation of the grid voltage relative to ground. It does not change quite as much as the grid voltage so that some slight loss of voltage swing results. Similarly the emitter of the transistor tends to follow the base voltage changes and a slight loss of voltage swing also results. Both circuits find application where power amplification (increased current capacity) is required and/or a lower driving impedance is needed for circuits driven by them. Both circuits do not invert the input signal. The output changes in the same direction as the input.

SBT OPERATING CHARACTERISTICS

A surface barrier transistor, as used in S-2000, when switched "on" has only a fraction of a volt dropped across it. Typically this voltage is on the order of O-2 volts.

- 02 to 05

A transistor switched "off" conducts a current on the order of 20 microamps.

Depending on the circuit values and the particular logic configuration, the collector to ground voltage in "on" and "off" states varies. A standard definition of these levels for the grounded emitter configuration is:

On: Collector to ground voltage not more than 0.1 volts negative.

Off: Collector to ground voltage not less than 1.0 volts negative.

Thus with these defining levels one may determine the state of a given portion of the circuitry by measurement.

The time required to switch from one state to the other is on the order of one tenth of a microsecond.

Transistor circuitry for TRANSAC may be "direct coupled" or " resistance coupled".

D. C. TRANSISTOR COUPLING

Coupling is the term describing the manner of connecting several stages of transistors to form a logical network. One of these methods is "direct coupling".

In this method, the base of the driven transistor is connected directly to the collector of the driving transistor. As shown in Figure 1-6, if transistor 1 is "on" the emitter-base voltage of transistor 2 is -0.1 volt or less (the drop across the conducting transistor). Transistor 2 is cut-off because virtually no current is supplied to the base. Not all junction transistors will be cut-off by such an emitter-base voltage, but the surface barrier transistor is readily cut-off. If transistor 1 is cut-off, current will be drawn through the collector resistance, R_C, and the emitter-base junction of transistor 2 to bias it in the forward direction. Transistor 2 is thus held "on". (Note that in this purely direct coupled circuitry, the collector of transistor 1 will not be sufficiently negative to meet the definition above of the ON condition because the emitter-base forward drop of transistor 2 is appreciably less than a volt.)

The principal advantages of the direct coupled circuitry are the use of only one supply voltage (2 or 3 volts), and the small number of additional components used in addition to the transistors. The main disadvantage is that an inversion of the signal occurs in each stage because only the inverter circuit can be used. Also one transistor usually can drive only one other base.

Resistance coupled circuitry can offset some of the disadvantages while retaining most of the advantages.

R.C. TRANSISTOR COUPLING

As shown by Figure 1-7, the inverter has an additional

resistor placed in series with the base. The inverter is normally driven by an emitter follower as in Figure 1-5. The emitter follower is capable of driving about six R. C. inputs (inverter inputs). Capacitor C_c is added to the circuit to speed the response of the driven transistor. In switching the transistor "on" it provides a larger base current initially. In switching the transistor "off", the capacitor provides assistance in removing the excess holes in the base region by means of stored charge.

The resistor in the emitter circuit of the emitter follower is connected to a positive source of voltage whose value is so chosen to provide a nearly constant current flow through the transistor but without causing excessive heat dissipation.

The S-2000 uses resistance coupled transistor logic (RCTL).

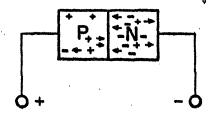


FIGURE I-I. CONDUCTING JUNCTION

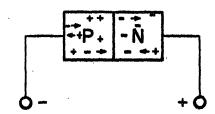


FIGURE 1-2. BACK-BIASED DIODE JUNCTION

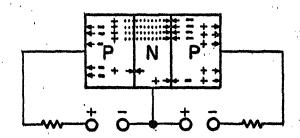


FIGURE 1-3. PNP JUNCTION TRANSITOR

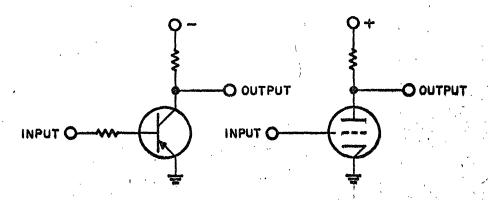


FIGURE 1-4. INVERTER

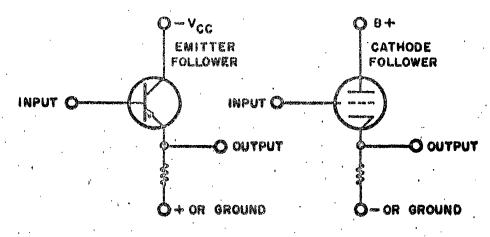
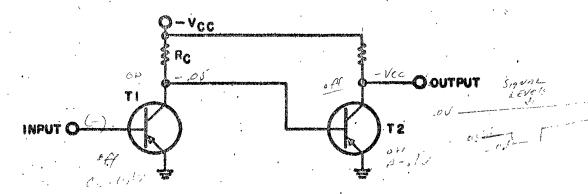
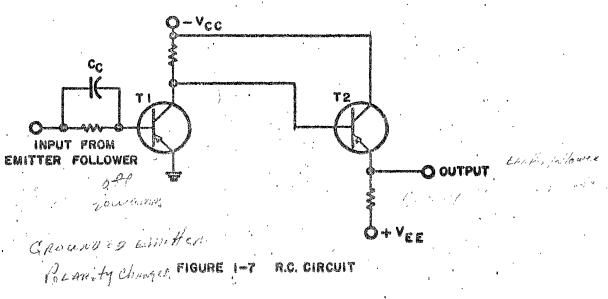


FIGURE 1-8



DIRECT COUPLED TRANSISTOR CIRCUITRY



R.C. CIRCUIT

2. S-2000 CIRCUITS

2.1 STANDARD LOGIC CIRCUITS

The following discussion will describe the standard building block circuits used to perform arithmetic and control operations. Emphasis will be placed upon understanding of circuit operation. Conventional symbols will be shown as convenient in the text. No attempt is made to cover the complete arrangements of components in all possible logic configurations. A few of the more common combinational schemes will be pointed out.

INVERTER OR COMMON EMITTER CIRCUIT

Shown in Figure 2-1 is the inverter or common emitter circuit. It is R.C. coupled as discussed above. The emitter may be either grounded or connected as discussed below for other circuit functions. Its output is used to drive one emitter follower.

EMITTER FOLLOWER

Shown in Figure 2-2 is the emitter follower circuit. Its operation was described above, and can drive up to six common emitters. Essentially it serves as the power amplifier for a resistance coupled stage. A resistor may be added in series with the base when an emitter-follower is driven by another emitter-follower to suppress oscillation. Frequently the combination of inverter to emitter-follower is found as shown in Figure 2-3. Logically the combination functions as an inverter but with a higher load capability.

SERIES GATES

Logical operations of "and" and "or" can only be provided by combinational circuitry. An example is the "series gate" or "two-high gate" shown in Figure 2-4. This circuit is an inverter if both transistor bases are driven by negative going signals. Thus if both transistors are switched "on", the voltage from the top transistor collector to ground will be positive going. If either one or both are switched "off", the upper collector will be negative going. In critical timing applications a resistor may be added (shown dotted) between V_{CC} and the bottom transistor collector. The purpose of this resistor is to provide a means of dissipating stored holes in the bottom transistor. Supposing that the bottom transistor is

driven and then has the driving signal removed without having switched the top transistor "on". Ordinarily the stored holes can be recombined by the reverse bias, collector-base current. Since the top transistor never functioned to connect the bottom transistor collector, the normal means of hole storage dissipation was not provided. If a short time later, a signal is applied to the upper transistor base, a positive output will result until the excess holes are removed from the bottom transistor. Thus the bottom transistor would tend to store an input condition which would give a temporary false output from the gate. The additional resistor provides the means to assure that the bottom transistor is "cleaned up".

PARALLEL GATES

Parallel gates may be made by paralleling the collectors of inverters or the emitters of emitter-followers. The parallel gate-common emitter is shown in Figure 2-5. Negative input to either transistor base produces a positive going output. If both inputs are negative and subsequently both are switched positive, the time for hole storage clean-up is increased somewhat in the parallel collector gate over clean-up time in a simple inverter.

Figure 2-6 shows a parallel emitter gate. Negative input to either base produces negative output.

TYPICAL CIRCUIT ARRANGEMENTS FOR LOGIC FUNCTIONS

From the preceding discussions, one observes that a large variety of logic functions can be provided by series and parallel combinations. Some typical examples are given below:

A parallel R.C. gate circuit as shown in Figure 2-7 parallels inverters and two-high gates.

The Two-High Selection Tree shown in Figure 2-8 is another combination.

In the Two-High Selection Gate Circuit of Figure 2-9, the upper transistor of the series gate actually consists of a group of paralleled inverters.

FLIPFLOP

Shown in Figure 2-10 is the flipflop consisting of two inverteremitter follower combinations. Each emitter follower output is connected to the base of the opposing inverter. If one inverter is "on" (i.e., its output signal is positive) its load, the emitter follower, will also have a positive output. A positive input to the other inverter will hold it "off" (i.e., its collector is negative). So also is the driver emitter follower output. A negative input to the first inverter holds it stably in the state first assumed/

Setting of the flipflop, to 1 or 0, is accomplished by a positive signal at A or B, respectively. (As the logic usually develops a negative set signal, an inverter not shown in Figure 2-10 is used to produce the required input polarity to the flipflop.)

SINGLE SHOT

The single shot consists essentially of a flipflop with additional RC coupling arrangements to give a specific transient performance. Upon application of a negative-going input pulse at A the singleshot assumes the opposite condition to its normal one. This condition is maintained for a definite length of time and then the singleshot returns to its normal state. Terminal B goes negative and C positive during the active (instable) period.

Comparison of the circuits of Figure 2-10 with Figure 2-11 shows that a resistor and capacitor have been added between an emitter-follower and an inverter. A differentiating circuit is placed at the single-shot input so that only the leading edge of the input driving pulse is utilized to drive the single-shot. The singleshot will respond only once to a negative signal, regardless of its duration.

A negative going input signal gives a positive output from the parallel gate to the emitter follower it is driving. The emitter-follower in turn supplies a positive input through the discharge capacitor to hold the next inverter cut-off temporarily. After passing through another emitter follower the parallel gate is held "on" to continue the active state of the singleshot.

After the interstage capacitor C₂ has charged sufficiently to permit the base of the inverter input it drives to swing apprecially negative, this inverter output begins to swing positive. This causes the inverters in the parallel gate to swing negative so that the singleshot assumes its normal state.

The time that the singleshot is in the active condition is a function of the capacitor C₂ and the adjustable resistance. Larger resistance and capacitance values will give a longer output pulse duration. The diode checks the swing of the parallel gate base when the input signal is positive going to prevent large voltages on this base.

NEON DRIVER

Shown in Figure 2-12 is the neon driver circuit. The neon lamp is fired if about 90 volts is dropped across its electrodes. It is extinguished if the voltage across its electrodes is dropped under about 42 volts.

If the transistor is switched "off', its collector will tend to swing toward the negative collector supply voltage of -48.5 volts. Because the other electrode of the lamp is tied to + 41.5 volts, 90 volts are dropped across the lamp to fire it. It remains lit at the operating voltage peculiar to each particular lamp (less than 90 volts) with current limited by the resistors in series with it. Regardless of any signal levels customarily supplied to the transistor base, should the switch be open, the transistor will be "off" and the lamp lit.

Lif the switch is closed and a negative going signal is applied as input to the transistor base the transistor is switched "on". Its collector is positive going (1. e., at about ground potential). Only +41.5 volts are available for the neon lamp. This is insufficient to maintain the gas discharge in the lamp. As a result the lamp is extinguished.

RELAY DRIVER

The relay driver schematic is shown in Figure 2-13. It is essentially an inverter type of circuit except that the collector resistor is replaced by the solenoid of the relay. Since a negative signal turns the transistor "on", a negative signal actuates the relay.

The diode and resistor combination provides a path for current sustained by the solenoid flux decay. When the transistor is switched "off" the inductance of the solenoid attempts to maintain the "on" current flow. Without the discharge circuit the transistor would be required to dissipate the stored energy possibly at an excessively high collector voltage. The resistor provides a path for discharge current thereby limiting transistor collector voltage and dissipation.

MANUAL SET CIRCUIT

As shown in Figure 2-14, the manual set circuit switches 41.5 volts through a 10K resistor to an inverter collector. Since the flipflop is set by means of a positive signal at the collector, any source of positive going voltage is adequate.

The SG-22 diodes shown eliminate sneak paths from one flipflop to another when the manual set switch is not being operated. The diode is not necessary if only one flipflop is being set from the switch.

2.2 ASSEMBLIES AND PHYSICAL LAYOUT

The hardware of the computer is organized by standardizing the circuitry into units. A unit may consist of a circuit stage or part
of a stage. The units are produced on an etched circuit "module" whose
dimensions are approximately 4-7/8" x 13/16". A module may contain
several units of the same type. For example, the HG2 module contains all
the circuitry for a series gate (two-High Gate) with the exception of the
collector resis or. The HG2 module contains two such units.

The collector resistor is placed on the module that contains the emitter follower unit, such as the En module. (El has our collector-resistor emitter-follower units). One propose in placing that resistor in the emitter follower module is to enable joining several grounded emitters to one resistor to form a parallel gate. The GGl module, for example, has four grounded emitter units minus the collector resistors. It may be reasonably deduced that most modules contain four transistors. Another module, Cl, contains four units, each having a collector resistor and an emitter follower, but lacing the emitter resistor. This, of course, nables forming an emitter follower gate.

For inverter stages, the GO1 module has two units, each comprised of a complete grounded emitter and emitter follower configuation. This same module, with the required connections will also form a flipflop. It is so used, with two units on adjacent GO1 modules joined to form the flipflop.

The single shot occupies an entire module. SSI is a typical single shot module. In this instance, the module contains five transistors.

In all, over fifty module types are used in the computer.

The module contains etched circuitry on one surface. Components are location on the other side. The transistors are mounted by pairs in two white nylon receptacles, which are riveted to the module. The transistor leads are soldered to the appropriate points of the etched circuits. Advantage is taken of the etching process to clearly mark the wiring points, on the module, for each component lead. Small etched letters and numbers adjacent to the drilled holes indicate the connections for the leads. For transistors, the letters "C", "E" and "B" identify the connections for the collector, emitter and base respectively.

The transistor is marked with a red line near the collector lead. Looking downward at the glass base seal of the transistor, the leads are arrayed clockwise, collector, base, emitter. When the transistor is placed in the nylon receptacle, a small nylon disk with three holes is inserted over the leads to keep them separated. The disk has a triangular notch on its circumference adjacent to one of the holes. The collector lead is always inserted through this hole; and the collector lead is subsequently identified by this notch.

Up to twenty-one modules may be mounted on a "card", an etched circuit board measuring approximately 5-1/4" x 12-1/4" (See Figure 2-15). A maximum of fourteen jumper wires is used for connections between a module and its card. Two (the ones at each end of the module) are the voltage connections. The remainder of the connecting circuit points are identified by relating them to one of the three terminals of a transistor. If a module terminal is designated as "E4", for example, that terminal is connected by an etched circuit line to join the emitter lead of transistor number 4. The five transistor locations are standardized and numbered.

Figure 2-16 shows the SSI module schematic and physical layout. If the <u>card</u> is vertically held so that when looking at the component side, the cards' terminals are at the left end, the transistor locations on any module, reading from bottom to top, are 1, 2, 5, 3 and 4. The other components are given the same number as the transistor with which they are functionally related. The transistor 5 position is not always used.

The card, Figure 2-15, has numbered module positions. The CA card uses eighteen modules, for example, the locations indicated by the etched numbers within the circles.

The modules are mounted on one surface of the card. Etched lines are used on both sides. Connections between the sides are made by "feed-throughs", wires soldered to the etching on both sides through drilled holes in the card. The etching area surrounding a hole is known as a "land".

The card has fifty terminals, twenty-five on each side and numbered 1 to 50. Terminals 26 to 50 are at the module side of the card, terminals 1 to 25 on the other. Terminals 1 and 26 are at the top of the card.

The outer terminals are used for the voltages:

Terminals 1, 2	ground
Terminals 26	-3.5 V
Terminals 24	+ 41.5 V
Terminals 49	-48.5 V
Terminals 50	+6 V

The components, not on modules, at the end of the card are the neon indicator circuits. The name of the card is given, in etched letters, at this end.

Cards plug into connector jacks in the computer cabinets. The back panel wiring interconnects the 300 card positions. Figure 2-17 shows the console and cabinets of the computer.

Each cabinet has one hundred card positions, four horizontal rows of twenty-five cards numbered 001 to 100. Viewed from the front, the 001 position is at the upper left corner. The cabinets are in turn identified as J11XXX, J12XXX and J13XXX, left to right from the front view. (The cards are inserted on this side.)

The cabinet doors are panelled with transparent plastic sheets to permit viewing the neon indicators with the doors closed. The panels are imprinted to identify each neon. These neons display the contents of registers, flipflops, counters etc., that are not displayed at the console above. Figure 2-18 is a reproduction of the imprinting on the door panels. The numbers give the bit position of the register or counter.

Figure 2-19 is the back plane view of the six cabinets comprising the index register and an 8192 word memory circuitry.

The index registers are located in the J34XXX cabinet in the lower right. The other cabinets (shown with the doors removed) comprise the memory. The six cabinets are located to the right of and just behind the console.

2.3 POWER

Despite the size and complexity of the S-2000, a relatively small number of power supplies are required. However a fairly elaborate A.C. distribution system is required to turn these supplies on and off in an ordered sequence, as well as control of the power to the various fans, heaters, motors and alarm circuits. The following section describes the A.C. distribution and the D.C. power supplies.

A.C. DISTRIBUTION AND CONTROL

The A.C. distribution and control system distributes regulated and unregulated A.C. from the power mains to the power supplies, cooling fans and other equipment at the control of the operator. Upon depressing the START switch, on the console, power is supplied to the fans and the D.C. power supplies. The computer supply comes on first, and after a few seconds, the supply for memory is turned on. This is to ensure no loss of data stored in the memory during the turn-on. The reverse order is used in turn-off. The power to the cooling fans is maintained for an interval after power is removed from the D.C. supplies to dissipate the residual heat.

The Power Supply consists of five package units. These units are: (Figure 2-20 shows the front panels of the units)

- (1) Line Voltage Regulator General Radio Co. 1570-AL.
- (2) Control
- (3) (-) 3.5 volt source.
- (4) (+) 6 volt source.
- (5) (+)41.5, (-)32, and (-)48.5 volt sources

For information concerning line voltage regulator see manufacturer's data.

The descriptions to follow will be broken down into description of the control unit followed by descriptions of each individual voltage source. Although three sources are combined in one unit, as listed above, each source is essentially isolated except for a common line voltage input and common protective circuitry contact arrangements. For definitions of symbols used in the text and schematic refer to the referenced drawing for each description.

Interconnections between units are shown in Figure 2-21.

CONTROL UNIT

The Control Unit (Figure 2-22) controls the application of A.C. input power to the sources and contains the protective circuitry (except meter relays) which a sure operation of the power supply only with output voltages within the limits set by the meter relays. The controls are the master circuit breaker for the entire power supply and "Protective Circuit Disable switch. Indication provided are "Protective Circuit On", "D.C. Supply Fault", and "Regula et A.C. On". All connections are hrough the Cannon Connector J14601.

Normal Starting Sequence:

With regulated A.C. "on", voltage is supplied to terminals 2 and 3. Transformer T is energized and positive voltage appears between points (a) to (g) and negative voltage from points (b) to (g). The "Protective Circuit On" light is lighted and relay Z1 is actuated. With the voltage source inputs connected between terminals 9 and 10, "D.C. Supply Fault" light is lighted. Unit is ready for actuation of the circuit breaker.

With CBl switched "on", contact C' completes a path from terminal 3 to terminal 10. Contact C2 completes a circuit from terminal 2 through con act of Zl, through coil of relay Z2 to terminal 3 actuating Z2. A circuit is completed through Z2 contacts from terminal 2 to 9. "Regulated A.C. on" light is lighted and A.C. power is delivered to the voltage source inputs. "D.C. Supply fault" light is extinguished. Time delay motor M in TDl begins to run with the actuation of Z2 commencing a three second delay period. Terminals 4, 7 are connected to point (b) to supply negative voltage to meter relay locking contacts and prevent meter lower limit contacts from sticking.

At the end of the 3 second period, TDl contacts are actuated closing the circuit from point (a) through "protective circuit disable" switch Sl, circuit breaker trip coil, TDl contacts to terminals 4, 7. Resistance Rl limits the current through the trip coil due to the voltage between points (a) and (b) such that a negligible drop in voltage across the CBl trip coil results. Thus terminals 4, 7 are essentially at the same potential as point (a) relative to point (g) after completion of the time delay period. Protective circuit is now fully operative.

NORMAL SHUT OFF SEQUENCE

The circuit breaker is tripped off manually. Contact C2 breaks the circuit through relay Z2 operating coil. Contact Z2 opens the circuit from terminals 2 to terminals 9. Contact C1 opens circuit from terminals 3 to terminals 10. "Regulated A.C. on" light is extinguished and "D.C. Supply Fault" light is lighted. A.C. power is removed from the input of the voltage sources. Time Delay, TD1 resets supplying negative voltage to terminals 4, 7.

FAULT SHUT-OFF SEQUENCE

Any meter contact striking either high or low limits connects terminals 4, 7 to point (g) through the locking coil contacts. Voltage is dropped from point (a) through "Protective Circuit Disable" switch S1, Trip Coil, TD1 Contact, through terminals 4, 7, Meter Relay returning through terminal 1 and then to point (g). Sufficient current flows through CB1 trip coil to trip the circuit breaker. Shut off is the same as B above except that circuit breaker is not tripped manually.

OPERATION WITH PROTECTIVE CIRCUIT OVER-RIDE

Operation is similar to A above except relay contact Z1 is shunted by actuation of switch S1 and the trip coil circuit is broken by S1. Thus the circuit breaker must be tripped either by manual operation of circuit breaker or release of "Protective Circuit Disable" switch S1.

NOTES:

In case of failure of Protection Circuit supply as evidenced by "Protective Circuit On" light being extinguished, relay Zl will open circuit of relay coil Z2 removing power from inputs of voltage sources. The circuit breaker will not be tripped. Actuation of Sl will reapply power to the source inputs.

D.C. POWER SUPPLIES

Transistorized D.C. power supplies are relatively new. Essentially the circuitry is similar to vacuum tube type voltage regulators. A transistor is used as a variable resistance in series with the load and an ordinary transformer-rectifier-filter combination. The output D.C. voltage is sensed and compared with a reference voltage in the supply

(Zener reference diode). Any error is amplified and used to change the effective resistance of the regulating ("pass") transistor.

Special meters and circuitry are used to switch off the supply if the output voltage exceeds the preset limits in either direction.

One representative supply is described here, as they are similar in design.

(+) 6 Volt Supply (Figure 2-23)

This Vol age Source of the Computer and Control Unit Power Supply contains three important functional sections.

- (a) EDC1 Load and Regulator Voltage Supply
- (b) EDC2 Bias Supply
- (c) Voltage Regulator

EDC1 Load and Regulator Voltage Supply

With voltage supplied to the primary of Tl input voltage and CB 14801 closed, the dodes connected to Tl rectify the A.C. voltage to provide a pulsating uni-directional current flow through capacitor C4, the voltage regulator amplifiers and the external load returning to Tl secondary center top. Sufficient capacitance is provided so that the average load current can be supplied from a nearly constant source. Any small ripple on EDCl is substantially removed by the voltage regulator before appearing as output voltage.

EDC2 Bias Voltage

Similarly EDC2 is developed by the diodes connected to T2 to provide pulsating unidirectional current to filter consisting of R9, C5 and C6. The additional components R9 and C6 provide improved filtering over that obtainable with a single capacitor. Since substantially pure D.C. bias current is required and no regulator is provided, necessary filtering must be provided by the two stage network employed in the EDC2 supply. Resistor R10 limits the inrush current drawn from T2 and protects T2 in case of short or overload on EDC2 supply.

Voltage Regulator

The voltage regulator consists of a voltage reference and a high gain direct coupled transistor amplifier. These are connected as a closed loop regulating system.

In the regulating system, a reference voltage (the drop across a voltage reference diode) is compared with the output terminal voltage by means of a suitable network. Any error detected is amplified and use to adjust current passed by a transistor in series with the external load. As load voltage tends to become too high, less current is passed to the load. As load voltage tends to become too low, more current is passed. Thus the error is corrected by automatically adjusting load current to the proper value such that a virtually constant output voltage is maintained.

Following is a detailed discussion of the amplifier operation assuming the output voltage tends to become too high.

Transistors TR1 and TR2 are carefully matched low leakage transistors connected to form a differential D.C. amplifier. This circuit has the property of tending to cancel almost entirely the temperature changing characteristics of one transistor by equivalent changes in a second transistor. With sensing terminals properly connected to the voltage output terminals as shown, current flows through two parallel branches: resistor R4 and Z; and the series network containing R1, R2 and R3. Diode Z is the reference diode. Since the voltage sensed is higher than the inverse break-down voltage of the diode, a nearly constant voltage appears across Z.

The base of TR1 will tend to remain at a fixed voltage more negative than the +output terminal of the supply regardless of potential between the + and - output terminals of the supply.

TR1, being an emitter follower, will tend to maintain its emitter, and that of TR2, at a fixed potential more negative than the + output terminal. However the voltage at the base of TR2 will vary proportionally as any potential change between the + and - terminals.

Output terminal voltage changes will cause a direct variation in the forward bias on TR2. For example, if the terminal voltage increases, the voltage level at the base of TR2 would become more negative with respect to its emitter voltage level.

This would result in a larger TR2 collector current and a positive-going signal at the base of TR3. TR3, an NPN in an emitter follower configuration, will respond with an increase in its emitter current. Its emitter will swing more positive.

Voltage EDC2 tends to bias TR4 into saturation so that maximum collector current would flow. Transistor TR3 tends to supply current in opposition to the bias current of TR4. As TR3 conducts increasing collector current, (due to increasing output voltage from the supply), TR4 conducts less collector current. Transistor TR4 operates as an emitter follower to control TR5.

Transistor TR5 is connected in series with the load on the voltage source. Reduced collector current in TR4 causes reduced emitter-base current in TR5. Thus TR5 increases the effective resistance in series with the load by decreasing the current passed to the load tending to correct the error in output voltage. The resistors R5 and R6 bleed off the leakage current of TR5.

Capacitor Cl provides the necessary low output impedance for high frequency components of load current. C2 tends to suppress any tendency for oscillation in the differential amplifier current.

- 3.5 Volt Supply (Figure 2-24)

The (-) 3.5 Volt Source of the Computer and Control Power Supply essentially functions similarly to the (+) 6 Volt Source except for the addition of another transistor amplifier in the regulator and other minor details of circuitry. Parts symbols are the same on both schematic diagrams for equivalent functional components.

Input power is supplied to connector J14701A pins 2 and 3. Diode CRl is utilized to assist in temperature compensation of Z. Because of the low output voltage of this source, a reference diode having a negligible temperature coefficient of voltage can not be used. The change in forward drop of the specially chosen diode CRl due to temperature just cancels the change in Z reference voltage. Sensing terminals 6 and 21 must be connected as shown.

Transistors are used for TR5 to provide the required load current without excessive dissipation. An extra stage of emitter follower amplification is provided by TR6 to improve the regulator performance.

Leakage bleed off is provided as follows: TR5 by R6 and TR6 by R16. Resistors R17 and R16 stabilize the operating point of TR6. The sensing coil of Meter Relay M, 14701 is connected to the (-) output terminal because the supply develops a negative voltage with reference to the S-2000 ground point.

-32 Volt Supply (Figure 2-25)

The functioning of the EDC1 and EDC2 supplies of the computer and Control Power Supply (-) 32 Volt source is the same as the (-) 6 volt source. A single transformer, T, having two secondaries A and B is used. Voltage regulator operation differs in details. Input power is applied to connector J14901A pins 2 and 9.

VOLTAGE REGULATOR

Following is a detailed discussion of the voltage regulator amplifier operation assuming the output voltage tends to become too high.

Transistors TR1 and TR2 are carefully matched low leakage transistors connected to form a differential D.C, amplifier. This circuit has the property of tending to cancel almost entirely the temperature changing characteristics of one transistor by equivalent changes in a second transistor. With sensing terminals properly connected to the voltage output terminals as shown, current flows through two parallel branches: resistor R4 and Z; and the series network containing R1, R2 and R3. Diode Z is the reference diode. Since the voltage sensed is higher than the inverse breakdown voltage of the diode, a nearly constant voltage drop appears across Z.

The differential amplifier maybe considered as emitter coupled. Transistor TRI is an emitter follower. Thus voltage from point (a) to point (r) is slightly greater in magnitude than the voltage from point (b) to point (r). However, voltage between points (b) and (r) varies directly as the voltage between points (a) and (r). Because of the common emitter connection, TR2 has this same voltage between points (b) and (r) as its emitter voltage. Transistor TR2 collector current varies with the difference in voltage between points (b) and (c) or more precisely, the current flow between points (b) and (c). As point (b) tends to become more positive with respect to point (c), TR2 collector current increases. Thus as point (a) tends to become more positive with respect to point (c) TR2 collector current increases.

Since point (c) is connected through the reference diode to the (-) sensing terminal, point (c) will follow an increase in terminal voltage such that point (c will change approximately the same number of mill volts as the (-) output terminal. Point (a) will increase only as a fraction of the output voltage change due to the divider network Rl, R2, R3. Consequently point (a) will tend to become more positive with respect to point (c) increasing TR2 collector current.

Transi tor TR3 collector current increases due to the increased current supplied to its base by the TR2 collector.

Voltage EDC2 tends to bias TR4 into saturation so that maximum collector current would flow Transistor TR3 tends to supply current in opposition to the bias current of TR4. As TR3 conducts increasing collector currents, (due to increasing output voltage from the supply), TR4 conducts ess collector current. Transistor TR4 operates as an emitter follower to control TR5.

Transistor TR5 is connected to series with the load on the voltage source. Reduced collector current in TR4 causes reduced emitter-base current in TR5. This TR5 increases the effective resistance in series with the load by decreasing the current passed to the load tending to correct the error in output voltage. Resistor R11 limits the maximum current from the supply and permits TR4 to satura e TR5 more fully when necessary because TR4 collector supply voltage is slightly higher than TR5. The resistors R5 and R6 bleed off the leakage current of TR5.

Capacitor Cl provides the necessary low output impedance for high frequency components of load current.

Capacitor C2 tends to suppress any tendency for oscillation in the differential amp office current.

Resistor R14 limits the max mum current which can be drawn from winding A.

- 48.5 Volt Supply (Figure 2-26)

The (-) 48.5 Volt Source of the Computer and Control Power Supply essentially functions the same as the (-) 32 Volt Source. Parts symbols on both schematic diagrams are the same for equivalent functional components. Sensing terminals 3 and 17 must be connected as shown.

41.5 Volt Supply (Figure 2-27)

The (+) 41.5 Volt Source of the Computer and Control Power Supply essentially functions the same as the (-32) Volt Source. Parts symbols on both schematic diagrams are the same for equivalent functional components. Sensing terminals 2 and 16 must be connected as shown. The sensing coil of the Meter Relay is connected to the (+) output terminal because the supply develops a positive voltage with reference to the S-2000 ground point, pins 1 and 3. Diode CR2 is not necessary in the (+) 12 Volt Supply because the voltage which may be dropped across TR4 and TR5 is not sufficient to cause any damage to them. Sensing terminals 16 and 2 must be connected as shown. Two pass transistors TR5, are adequate for this source. Capacitor C3 is needed with this Source. The sensing coil of Meter Relay M35802 is connected to the (+) output terminal because the supply develops a positive voltage with reference to the S-2000 ground point.

POWER SUPPLY ADJUSTMENTS

These adjustments may be made to each individual Voltage Source

- Source output voltage is adjusted with screwdriver adjustment adjacent to each Meter Relay.
- MARGINAL 1.

 CHECK PAG
 CEFABLISHING 2.

 Whith howariant as there supply 3.

 (DONOT DO HERE)
- Upper limit contact of Meter Relay is adjusted with the right hand screw on the Meter face.
- Example
- Lower limit contact of Meter Relay is adjusted with the left hand screw on the Meter face.

Say 67 63 PRECAUTIONS

Be sure that sensing leads are connected to the proper polarity output terminals. Failure to do so may result in damage to the voltage regulator components.

Do not adjust the lower Meter Relay adjusting screw (center of movement face). The meter has been calibrated at the check point (arrow) to 1% accuracy. Tampering with this screw affects the meter accuracy.

MAINTENANCE PROCEDURES

To simplify the checking of the supply in case of a malfunction, the following procedure is recommended.

Procedure: (output voltage too high)

- 1. With supply input voltage switched "off", measure the resistance of each of the pass transistors (TR5 on the schematic drawings) and transistors TR4, TR6 and TR3 from collector to emitter. Resistance should read about 100 ohms. If resistance measures zero or nearly zero, one or more pass transistors are shorted. Defective pass transistors will read zero others will read about 1/4 ohm.
- 2. If step (1) shows the transistors to be satisfactory, switch the supply "on". Place a 1K ohms variable resistor across TR3 from emitter to collector. If output varies around the nominal output voltage (plus or minus a few percent) the amplifier following TR3 is operating properly.
- 3. If steps 1 and 2 are satisfactory, remove the 1K resistor and connect a 10K ohms variable resistor from TR3 base to the (-) sensing line. If output varies around the nominal voltage, TR3 is operating properly.
- 4. If the sense leads have been connected improperly to the output terminals, diode Z and transistors TR1 and TR2 have probably been destroyed. With the D.C. voltmeter, check the reference diode voltage. (This will be 5.4 volts on units having output voltages greater than 3.5 volts and 2.5 to 3 volts on the low voltage units).
- 5. If all previous steps have been completed satisfactorily the differential amplifier transistors are presumably defective and should be replaced with another matched pair.

Procedure: (if current voltage is too low)

- Measure EDC2 output voltage to be about
 to 6 volts. Defective component is in EDC2
 supply if voltage is very much lower than 5 volts.
- 2. Measure EDC1 output voltage to be greater than the nominal output voltage of the particular Voltage Source being tested. If less or zero, EDC1 supply is probably defective.

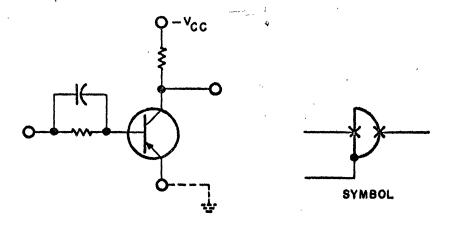


FIGURE 2-1 INVERTER OR COMMON EMITTER CIRCUIT

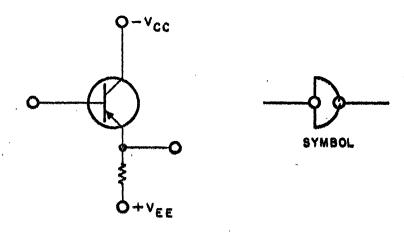


FIGURE 2-2 EMITTER FOLLOWER CIRCUIT

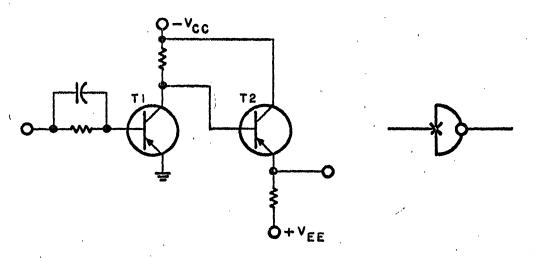


FIGURE 2-3 COMMON EMITTER-EMITTER FOLLOWER

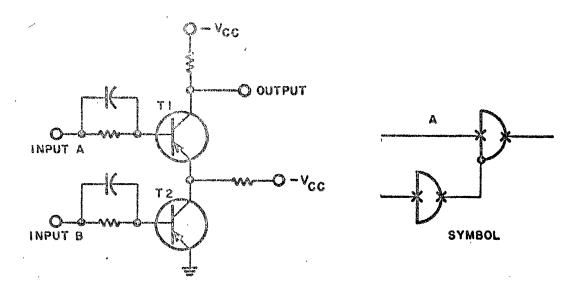


FIGURE 2-4 SERIES OR TWO-HIGH GATE

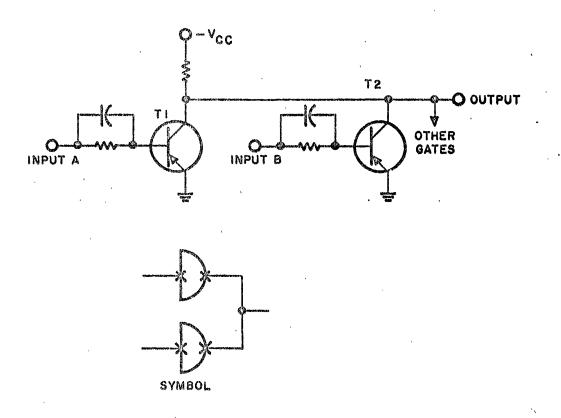


FIGURE 2-5 PARALLEL COLLECTOR GATE

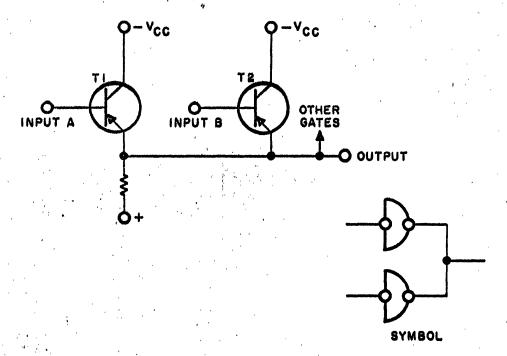


FIGURE 2-6 PARALLEL EMITTER FOLLOWER GATE

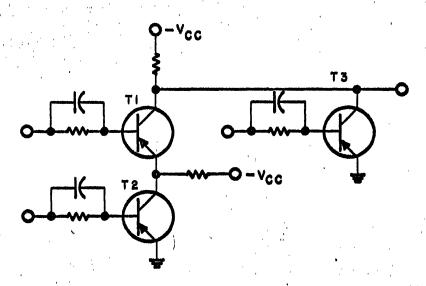


FIGURE 2-7 PARALLEL RC GATE

 $\frac{\partial}{\partial x} = \frac{\partial}{\partial x} \left(\frac{\partial}{\partial x} - \frac{\partial}{\partial x} \right) \left(\frac{\partial}{\partial x} - \frac{\partial}{\partial x} - \frac{\partial}{\partial x} \right) \left(\frac{\partial}{\partial x} - \frac{\partial}{\partial x} - \frac{\partial}{\partial x} - \frac{\partial}{\partial x} \right) \left(\frac{\partial}{\partial x} - \frac{\partial}{\partial x} - \frac{\partial}{\partial x} - \frac{\partial}{\partial x} \right) \left(\frac{\partial}{\partial x} - \frac{\partial}{\partial x} -$

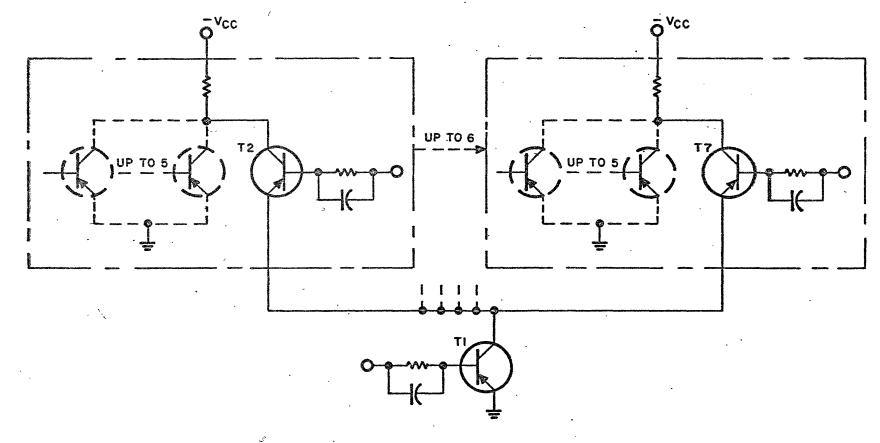


FIGURE 2-8 TWO HIGH SELECTION TREE

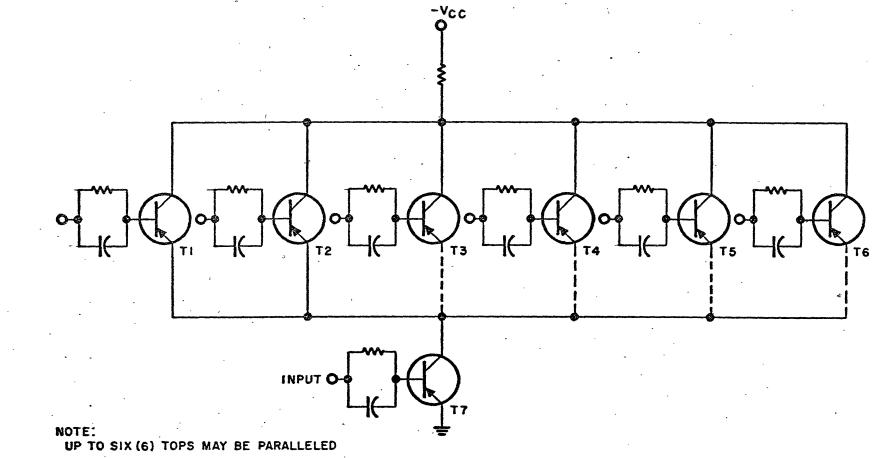


FIGURE 2-9 TWO HIGH SELECTION GATE

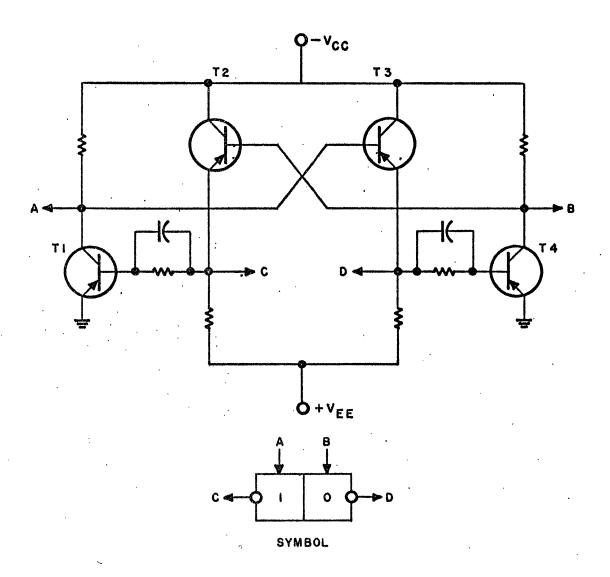


FIGURE 2-10 FLIP-FLOP

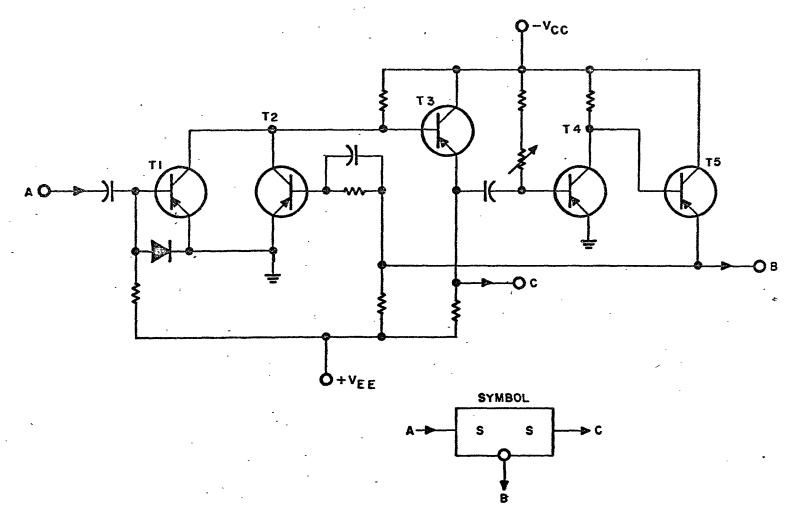


FIGURE 2-11 RESISTANCE COUPLED SINGLE SHOT

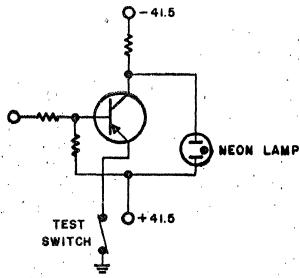


FIGURE 2-12 NEON DRIVER

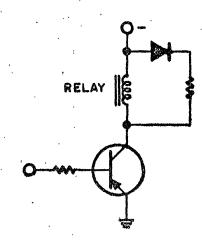


FIGURE 2-13 RELAY DRIVER

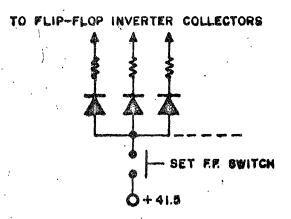
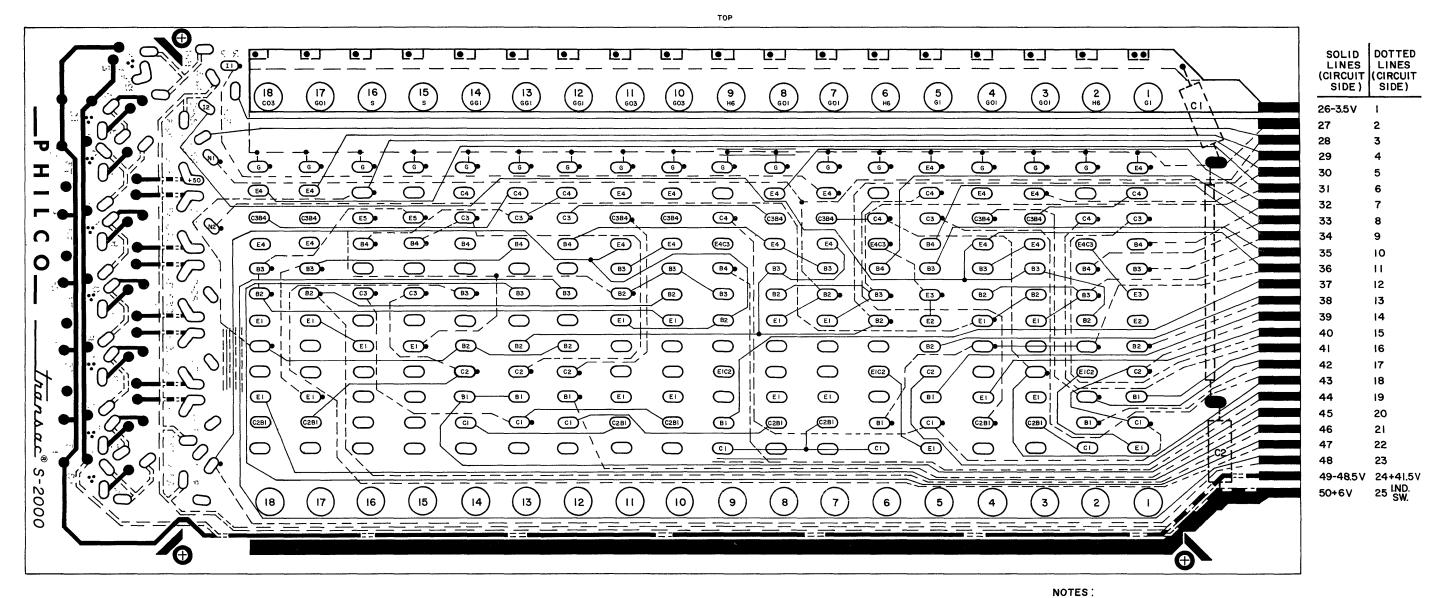
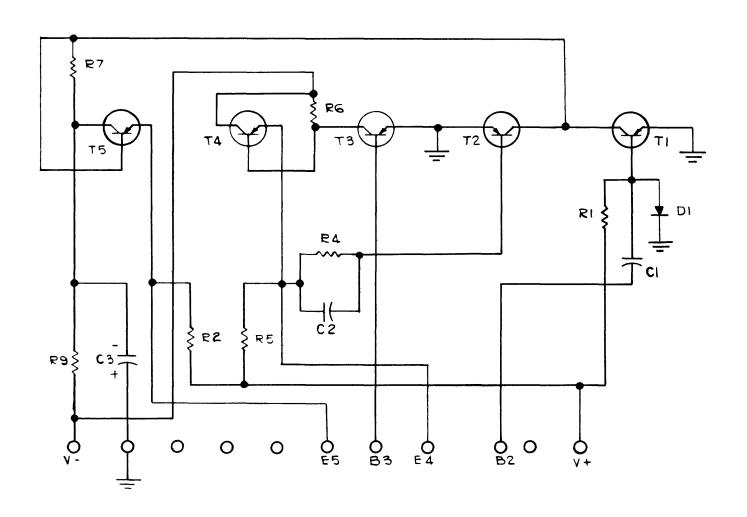


Figure 2-14 Manual Set Circuit



I. FEED THRU IS
INDICATED AT LAND
NEAREST DOT.

Figure 2-15 CA Card



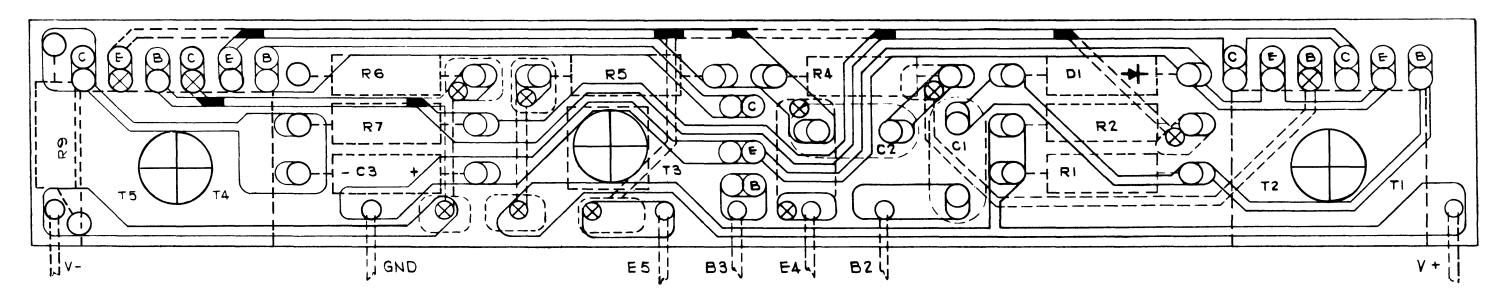


Figure 2-16 SS1 Module

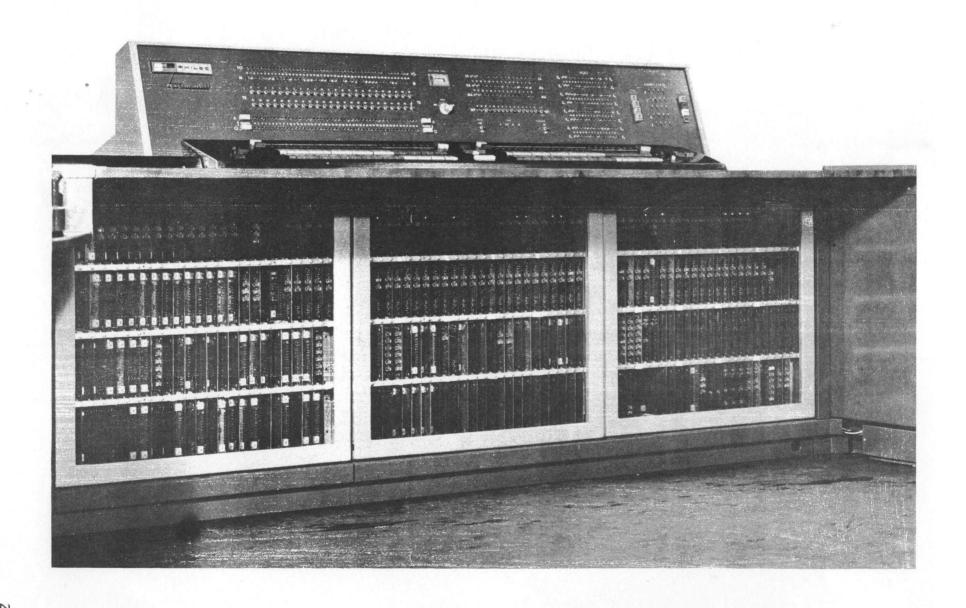
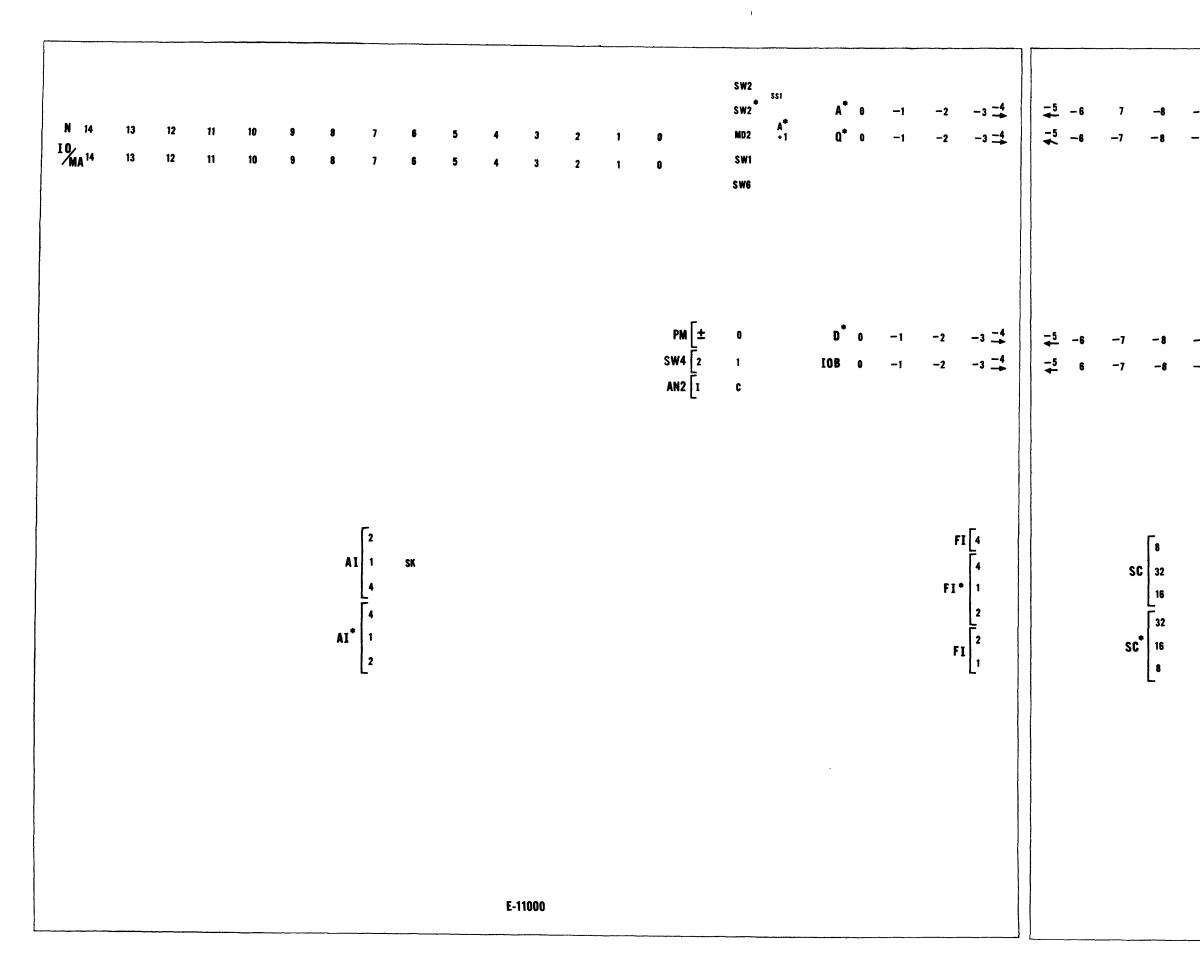


Figure 2-17 Computer and Console



ADV. Filt.

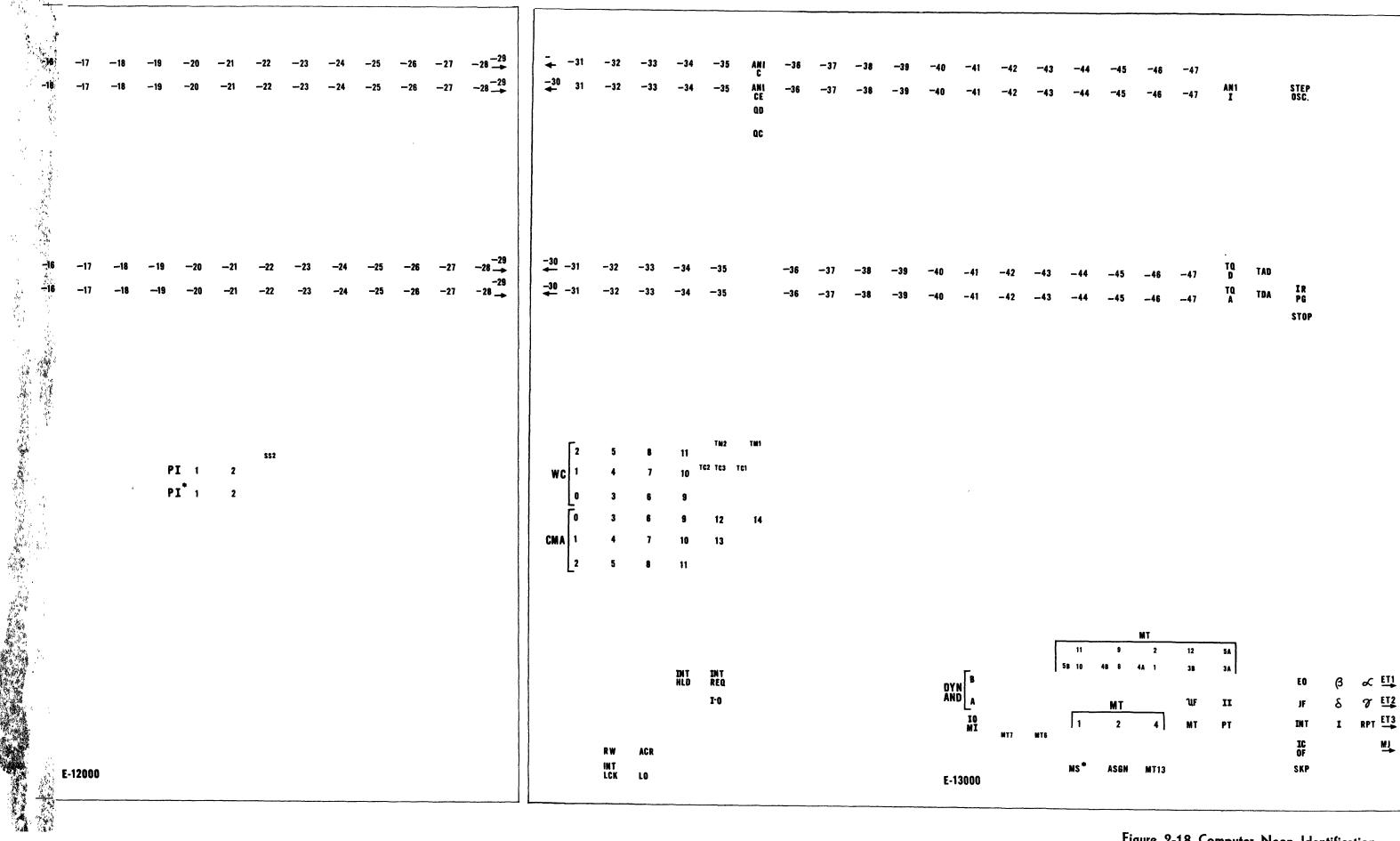


Figure 2-18 Computer Neon Identification

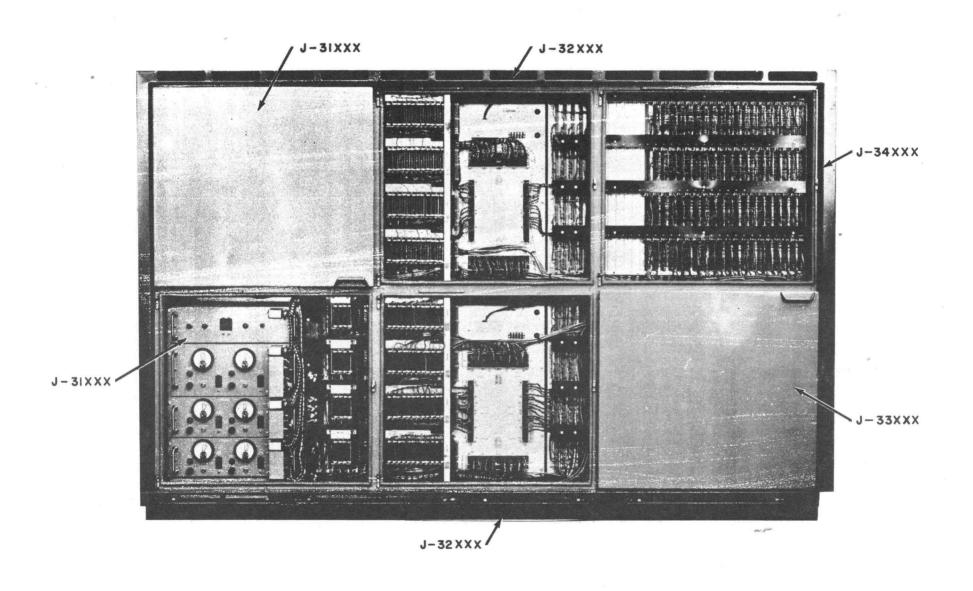
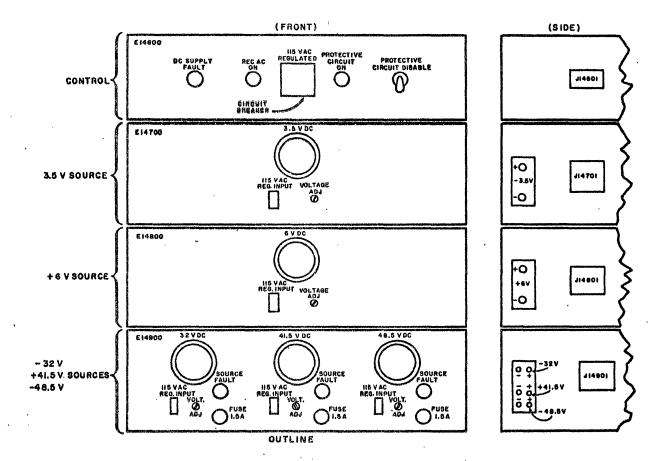


Figure 2-19 Memory and Index Registers Cabinets (8192 Word Memory)



LINE VOLTAGE REGULATOR NOT SHOWN, IS MOUNTED EXTERNAL TO MACHINE

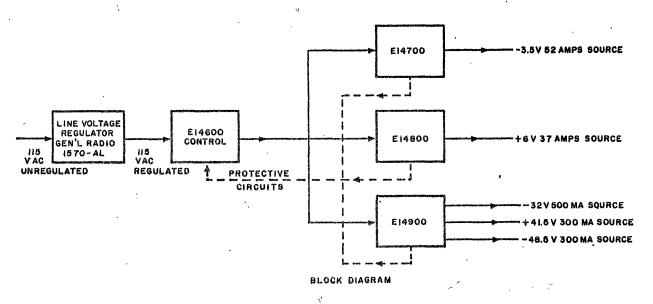


Figure 2-20 Power Supply Front Panels, Block

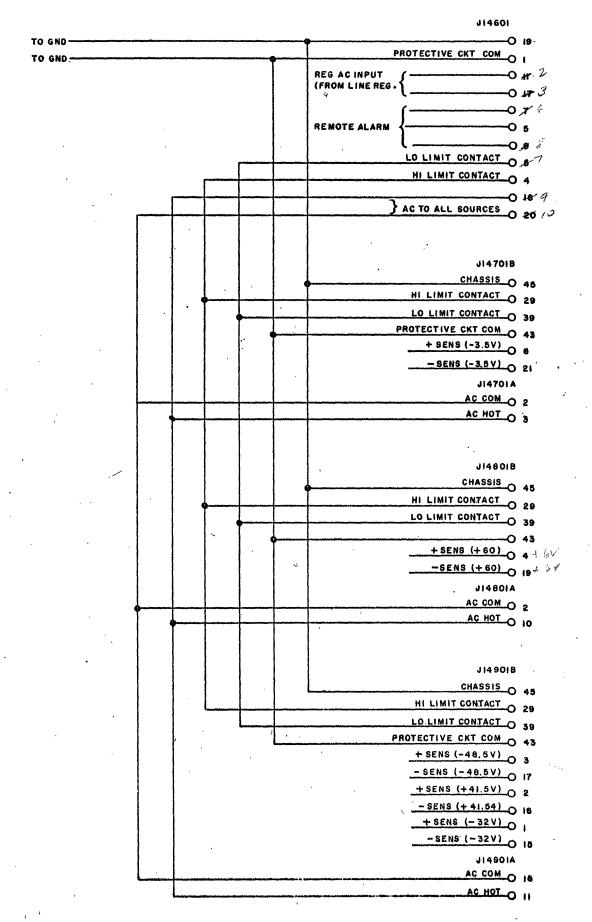


Figure 2-21 Power, Supply Cabling

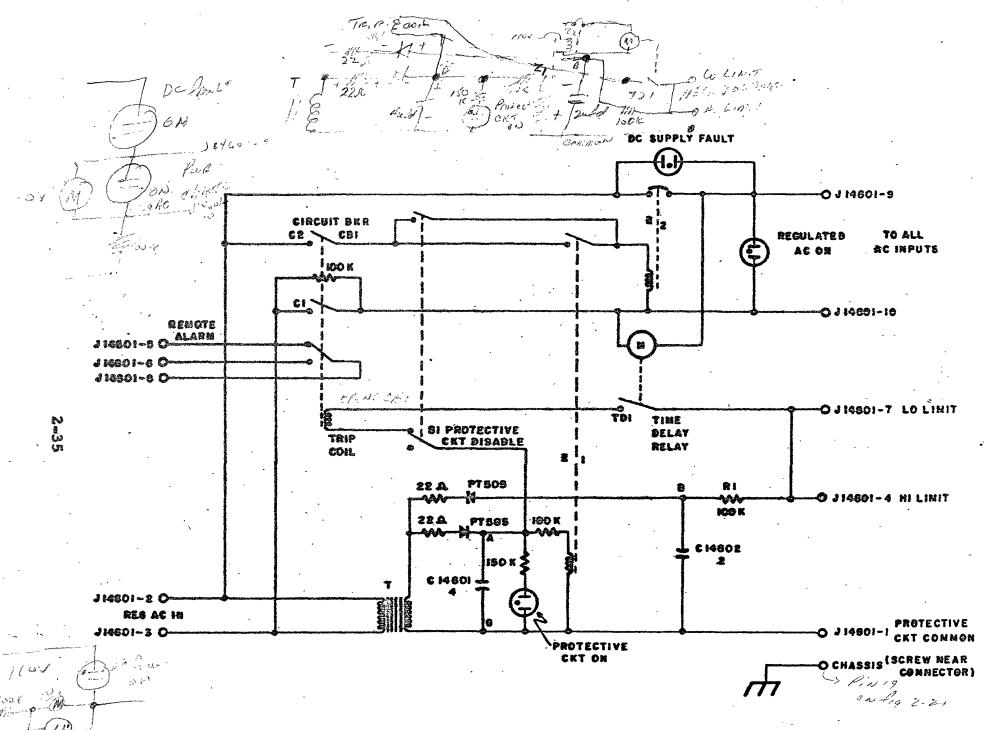
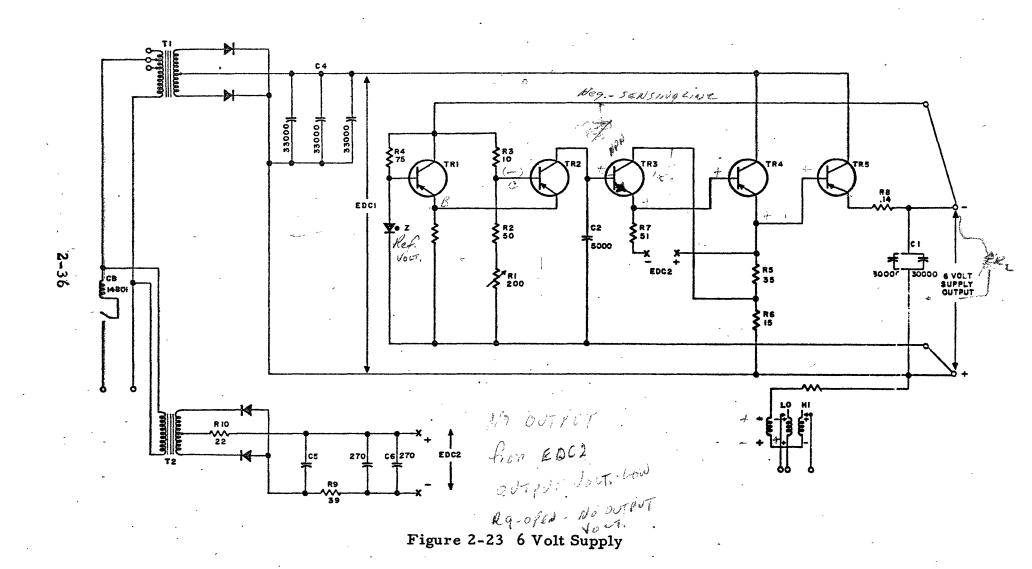
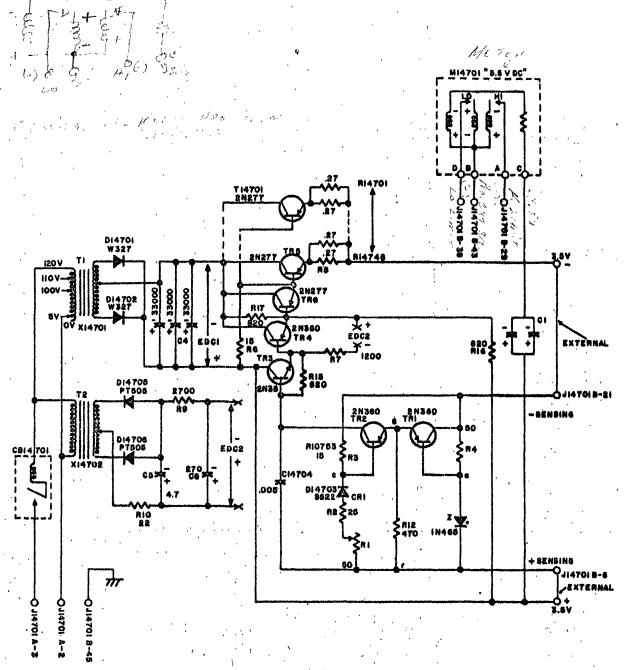


Figure 2-22 Power Supply Control Circuit





PIN DESIGNATIONS

J14701 A

2 - AC COM

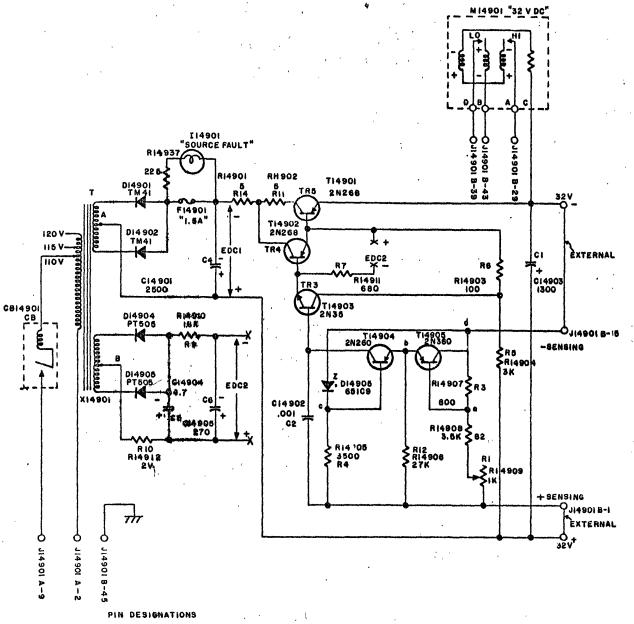
- AC HOT

J14701 B

6-(+) Bensing 21-(-) Bensing 29-HI LIMIT CONTACT

39-LO LIMIT CONTACT 48-PROTECTIVE CKT COM 45-CHASSIS

Figure 2-24 3, 5 Volt Supply



J14901 A

2-AC COM

9-AC HOT

J14901 B

I - (+) SENSING
IS - (-) SENSING
29 - HI LIMIT CONTACT
39 - LO LIMIT CONTACT

43- PROTECTIVE CKT COM 45- CHASSIS

32 Volt Supp y Figure 2-25

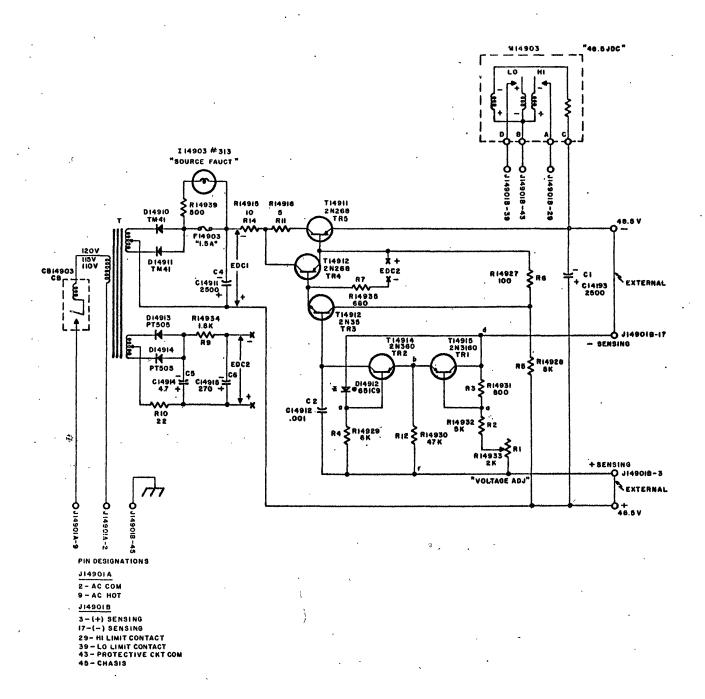
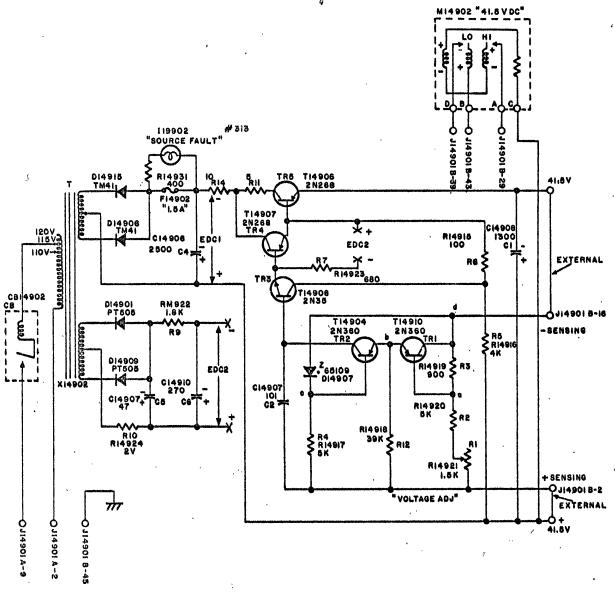


Figure 2-26 48.5 Volt Supply



PIN DESIGNATIONS

J14901A 2- AC COM 9- AC HOT J14901B

2-(+) SENSING
16-(-) SENSING
29-HI LIMIT CONTACT
39-LO LIMIT CONTACT
42-PROTECTIVE CKT COM
48-CHASSIS

Figure 2-27 41.5 Volt Supply

INTRODUCTION

In debugging or maintaing a computer, the oscilloscope is a powerful diagnostic instrument. When properly utilized it can be used to very quickly and accurately locate and determine the type of trouble or failure. A great deal of success, however, remains in the ability of the operator to correctly use and correctly interpret the instrument's presentation.

It is the purpose of this section to discuss the type of electrical faults that occur in the S-2000 logic circuits and the characteristic effects each displays. The discussion will assume that the logic is correct and will limit itself to fault conditions occasioned by component and/or material failure and/or drift. Usually logic errors create (or destroy) signals which are correct from circuit and electrical viewpoints, but are in error in time or position. These errors may be determined by recourse to logic, flow and block diagrams. Material or component faults, however, create signals (waveforms and/or levels) that are abnormal. Proper interpretation is necessary to specifically locate the fault.

3.1 TYPES OF FAULTS

The most common faults that occur in S-2000 are listed in relative decreasing order of occurence:

- 1. Improper use of oscilloscope and test equipment.
- 2. High resistance or open solder joints.
- 3. Leaky or shorted collector-to-emitter of emitter-follower.
- 4. Open emitter or emitter-follower
- 5. High leakage current in grounded-emitter.
- 6. Shorted collector-to-emitter of grounded-emitter.
- 7. Open printed circuit line.
- * Surface-barrier transistor logic circuits.

- 8. Shorted printed circuit lines.
- 9. High resistance or open contact of card corrector.
- 10. Improper component or value of component.
- 11. Broken bus lead.

Less common faults are:

- 1. Open base or collector of emitter-follower.
- 2. Open base, emitter or collector of grounded-emitter.
- 3. Collector-to-base short of grounded-emitter.

Relatively rare faults are:

- 1. Open or shorted capacitor.
- 2. Open or shorted resistor.
- 3. Out-of-tolerance resistor or capacitor.

Note that many of the above faults will have similar symptoms and their relative occurrence is a guide to the type of failure at hand. For example; open or shorted resistors and capacitors rarely, if ever, occur. Generally it is a poor solder joint, open contact, open printed circuit line or shorted circuit lines.

CAUSES OF FAULTS

The typical causes of the various type faults are described below: a knowledge of which will help prevent faults and also help interpret the "case histories" of failures.

Improper Use of Equipment

Improper use of the oscilloscope is one of the most common faults, especially among inexperienced personnel. An oscilloscope misused and misinterpreted can cause considerable lost time in searching for and correcting non-existent fault conditions, and may even

be destructive to the circuitry. One should take care to be certain that the oscilloscope probe is properly adjusted and calibrated. Most oscilloscopes have built-in 1,000 cycle square wave calibration signals. The ground return to the probe lead should be short when waveforms are to be critically analyzed. One should not connect the probe to the circuit under study with hook-up wire. Proper connections may be inconvenient, but are essential when fast rise times, short pulse widths and noise are to be observed and studied.

The probe should be used at all times. Makeshift connections greatly negate the useful characteristics of the oscilloscope (particularly wide bandwidth and low input capacity) and are often the cause of peculiar waveforms. They may even be the cause of circuit malfunction because of excessive stray capacity, coupling into other wires, and shorted pins. This is particularly important around single shots and timing flip-flops.

One should always be careful not to cause shorts when connecting test equipment or temporary wires to the connector pins. Most emitter-follower failures are directly caused by such oversights.

High Resistance or Open Solder Joints

High resistance or open solder joints are a common problem. They may occur at any time and have a tendency to be temperature sensitive because of unequal expansion of the wire, solder and/or printed board material. They are especially prevalent after extended periods of operation at relatively high ambient temperatures. This is because the physical processes which effect their failure are proportional to the integrated product of time and temperature. A rough measure of this product is the amount of gray coloration that appears on the surface of the solder.

Poor solder joints occur most often between the solder and tinned bus wire, sometimes between solder and component leads, and, only rarely, between the solder and printed circuit lines. Feed through wires are more susceptible since there are two solder-to-bus-wire joints. This is generally attributed to the fact that tinned wire and leads suffer from surface changes when stored for long periods (as is the case in production stocking) and exposed to oxygen, sulfur and human perspiration. The printed circuit lines have an immersion gold coating and thus suffer much less. Considerable attention is given to proper storage of wire and components, and where possible, immersion gold-coating. Considerable care is given in production (and should be given in repair) to a proper soldering procedure, especially concerning temperature and flux. The temperature should be such that the solder flows easily and wets the surface. Only pine rosin and alcohol (usually butyl) should be used. Any

residue must be completely removed with a solvent. Ethylene dichloride, amyl acetate (banana oil) and butyl alcohol are suitable solvents. All of these solvents are inflammable. They can be toxic if left on the skin for long periods or if inhaled to excess. Small amounts should be used in a well ventilated place. Smoking during use is undesirable. Flux residues tend to be hygroscopic and sticky, thus collecting dust and salts in an electolytic medium. This will attack the joint. No other fluxes can be used as they invariably contain ionic substances that are difficult to remove and will always attack the joint.

Care should be taken to keep the cards clean and free from corrosive substances such as: human perspiration; sulfur bearing substances as rubber products and food particles; and tar bearing substances, such as cigar and cigarette smoke.

The above may seem trivial but is really of great importance when it is remembered that there are nearly a quarter million solder joints in the central arithmetic and memory control alone, that each must go through at least 2,000 hours of debugging and testing time, and must have a useful life of at least ten years.

Particular attent on should be paid to the effects of changing temperature on poor solder joints, and in generating poor solder joints among the weak sisters. The rise in ambient air temperature in the central computer is about 8° Celsius (Centigrade) over that of the intake air. Some of the component leads and solder joints may be as high as 15°C over that of the intake air. Since the coefficients of thermal expansion of copper and eutectic solder differ by 12 X 10° per degree Celsius, this 15°C temperature rise and fall (when turning the computer on and off) causes a differential movement between the copper and solder of two parts in ten thousand. This is not serious in properly "wetted" solder joints, but will eventually cause failure in poor joints. Since the solder has the larger co-efficient of thermal expansion, there is a greater tendency for a marginal joint to be open when the computer is running warm (the ambient air temperature is high) than when it is running coller.

The thermal time constants are rather long for the card about 20 minutes and for a module cabinet about one hour. It requires about four to five thermal time constants to obtain thermal equilibrium. Thus, about 4 to 5 hours are required for all the internal components to reach thermal equilibrium and about 80 to 100 minutes for a card, if it is put cold into a warm cabinet.

It is interesting to note that the magnetic drum has the longest thermal time constant in the computer, somewhat over two hours. The thermal time constant of the core stacks is about 30 minutes. Thus the drum requires about 8 to 10 hours and the core stacks about 120 to 150 minutes to reach final thermal equilibrium.

Emitter-Follower Failures

Leaky or shorted collector-to-emitter and open emitter of emitter-followers are perhaps the most common transistor failures to be encountered. Most of these are causes by negligent use of test equipment or shorted pin connections. A few, especially in the initial hours (first 500) of debugging, are due to defective transistors (dirty surface, poor welds, defective seals, crystal imperfections, etc.). The total of these seldom amounts to more than 6 to 12 transistors. After the initial failures, nearly all failures can be attributed to human errors, until about 12 to 15 thousand hours of operation when a very few failures (order of magnitude, 0.03%) may result because of decreasing punchthrough voltage.

These particular faults result from excessive power dissipation. This will be caused by shorting the emitter of the emitter-follower to ground or to the positive voltage, or accidently paralleling two emitter resistors together. (The last is sometimes done because of temporary logic modifications). Faults will also be caused by excessive stray capacity to an emitter handling signals with high pulse repetition rates; defects internal to the transistor and punch through voltage decrease with age; transient currents due to improperly grounded soldering irons, and/or test equipment. Whether a collector-to-emitter short or open emitter occurs depends on which portion of the transistor is weaker, respectively, the crystal between collector and emitter or the indium emitter dot. On rare occasions the base or collector of the emitter-follower may open or there may be a collector to base short.

It should be noted that what often appears as an open emitter, base or collector, is simply a poor solder joint. When any transistor is removed, it should be tested separately. Replacing a transistor may, by the very act, unknowingly repair a poor solder joint and the removed transistor unfairly held at fault unless it is tested separately.

* (The only soldering iron approved for use on the S-2000 is one with an isolation transformer whose secondary is grounded, by a clip lead, to the computer ground.)

Grounded Emitter Failures

The most common grounded-emitter failure, but less common than emitter-follower failures, is high leakage or a collector-to-emitter short. Initially a few of these failures are due to defective transistors, as in the emitter-follower case. Later, nearly all are due to human error, as in the emitter-follower, until about two to three thousand hours of operation when one may occasionally find a grounded-emitter transistor with a rapidly increasing leakage current caused by aging.

Flip-flops are most sensitive to leaky grounded emitters, because of the internal feedback loop, which causes the flip-flop to favor one of its two sides (either remain in that state or continually reset itself to that state, regardless of the signals applied).

A leaky grounded-emitter may generate occasional false signals. This is because the leakage current acts as a bias keeping the grounded-emitter in the small signal region in an area where the dynamic beta is quite high. Any signal to the base will be amplified and may cause a build up at the collector which will eventually generate a false signal depending on the pulse width and repetition rate at the base. This, typically, shows up in parallel "and" gates that are supposed to be off. High temperature and high negative voltage, because they increase the overall leakage, tend to accentuate these affects. Increasing the negative voltage may be used as a marginal check to detect the imminence of this type of fault.

Other faults in the grounded-emitter such as an open base or collector, shorted collector to base are not common and are probably more often a poor solder joint as previously explained.

Printed Circuit Faults

"Printed circuit" boards are actually made by an etching process. Starting with the board stock, a sandwich of two sheets of copper (each 0.027 inch thick) bonded to a 1/16" paper - phenolic sheet, the surfaces are coated with a photosensitive emulsion. A film negative is placed in contact with each surface and the board is exposed to high intensity light. The transparent areas of the negative are located where the copper circuit is desired. Light penetrating these areas hardens the emulsion directly beneath.

After exposure, the unhardened emulsion is removed by a solvent. The board is then placed in an acid etching solution. The copper will be removed, by the chemical process, except where it is shielded from the etchant by the hardened emulsion (the "resist"). After etching the resist is cleaned from the board to bare the copper "wiring."

The most common printed circuit faults are open or shorted printed circuit lines. The open line may be due to mechanical separation of copper by hairlines scratches caused by an imperfect resist which allowed the etchant to contact the copper across the printed circuit line. Opens may also occur because of electrolytic action upon the copper of imperfectly cleaned boards, especially if the copper lines are undercut by the etchant. Most opens are detected in the initial board inspections. Others, however, may occur after soldering, or after long periods of time, as the mechanical contact is often sufficient to maintain temporary electrical continuity. Opens may also possibly be caused by mishandling of the cards; dropping, scratching, etc.. Repair is effected by solder.

Shorted printed circuit lines are caused by projections of metal which were not removed in the etching, solder bridging, too close mechanical tolerances, and pencil lines (pencil lead is very conductive). Repair is effected with a pen-knife, razor blade, or cleaning.

High Resistance or Open Contacts

In the standard logic circuits, a high resistance or open contact, is rare. There is a great tendency to use "contact trouble" as a catch-all to explain unknown or erratic fault conditions. The contact materials have been carefully chosen (rhodium on nickel for the card, and gold plating on the connector) and the mechanical tolerances are checked in the debugging stage. Outside of mechanical tolerance faults (which are removed during debugging) there are probably few, if any, failures caused by contacts at the signal voltage levels employed in the S-2000 logic.

However, contacts are a major source of trouble when small signal voltages (less than 0.1 volt) must be passed at small currents (less than 0.1 ma). This situation is to be found in all core sense amplifiers, drum read amplifiers, and magnetic tape read amplifiers.

The major enemy to good contacts; is dirt and film formations. Its best ally is cleanliness. Cleanliness cannot be overemphasized as its lack is by far the major cause of contact failure.

The primary culprits are human perspiration, sulfur bearing compunds (rubber bands and erasers), tar bearing compounds (cigarette smoke) and dust. A malfunctioning contact: can most often be corrected by simply removing and re-inserting the card several times to mechanically clean the surface. An occasional malfunction is caused by too great mechanical variation between the connectors and cards (out of tolerance). A rare malfunction (at least in the early life of the computer) is caused by fatigue of the spring contracts.

The contacts, both on the card and in the connectors, should be thoroughly cleaned with ethylene di-chloride and kept clean. Human perspiration is the major contaminant and its application to the contact areas should be very carefully avoided. Perspiration can travel from two to three inches across the surface of the card from the point of contact. The two major sources of perspiration are fingers and dandruff. Dandruff can be especially dangerous since it may also carry commercial oils and shampoo residues.

These precautions will limit film formation to environmental causes. Films will eventually form in from two to six months. As these may cause malfunction where small level signals are to be passed, it is a good maintenance procedure every two months, to clean the contacts by one or two removals, and re-insertions of all cards that have small signal amplifiers. In addition, every six months, clean all contacts (at least those on the card) with ethylene di-chloride. It would be wise to be certain that all cards in the computer have been cleaned as above.

The best argument for cleanliness can be one figure.

There are over 20,000 contacts in central computer and memory control alone. It is simple to avoid this type of intermittents and obscure troubles by good practices.

Other Faults

Occasionally a bus wire, particulary those that connect module and the card, may be broken through mishandling or because the wire was nicked or damaged. Excessive movement and flexure of the back-panel wiring may also cause failure due to breaks.

Wrong values of resistors or condensers may cause marginal operation. These are sometimes difficult to find. The wrong value" may be the effect of a high resistance solder joint.

Open or shorted resistors or capacitors will probably never occur, except perhaps for the tantalytic by-pass capacitors on some of the cards. One can almost immediately suspect a printed circuit fault or a poor solder joint.

Operation in a high ambient temperature will often cause an increase in poor solder joints, which are commonly mistaken for "component failures". The simple replacement of a component often, unknowingly, repairs the poor solder joint. Proper operation is achieved and the component, unless separately tested, is unjustly blamed.

3.2 DETECTION OF FAULTS WITH THE OSCILLOSCOPE

Following are the symptoms of faults as they appear on the oscilloscope. It would be impractical to reproduce every possible variation that could occur in equipment as complex as the S-2000 and with back-panel wiring as a strong modifier. The important symptoms will be discussed in sufficient detail so that they will be readily recognizable in the demonstrated cases.

It should be noted that the S-2000 in most part, is a binary, asynchronous, level system. There is no clock and operation depends upon the attaining of one or the other of two signal discrimination levels. These levels are -0.1 volt or more positive for one state, and -1.5 volts or more negative for the other state. These are respectively referred to as the positive and negative discrimination levels. There is a minimum pulse width (the minimum time a level must be present) that must be maintained to insure operation (propagating through "trees", operating flip flops, operating gates, etc.). This requires that careful attention be paid the timing flip flop (TC cards, such as AT, IT, etc.) and single-shot outputs. This minimum pulse width is disadvantageous in that it materially contributes to the limitation of the maximum speed of the machine. It is advantageous in that it provides some noise immunity. In the present S-2000 logic circuits, the typical pulse width is 0.35 microseconds. However portions of the circuitry respond to shorter pulse widths (down to 0.1 microseconds).

The lack of a central clock pulse in the S-2000 is advantageous in that, except for logic limitations, it allows the machine to operate at its maximum speed. In addition, it avoids the crosstalk problems inherent in clocked computers, caused by the large clock pulse currents. The several "clocks" associated with the memory and input / output present no special problems since they are distributed by standard! logic circuitry. The logic circuitry is designed such that there is little

net change in the power supply currents; while one logic stage is going "off" the next is going "on", etc.

There are several important items to look for in diagnosing faults in the S-2000 logic circuits:

- 1. The voltage levels.
- 2. The time slope while changing levels (i.e., "rise" or "fall" times). (To avoid confusion hereafter, "negative going rise time" and "positive going rise time" will be used to specifically refer to going from positive to negative and negative to positive discrimination levels, respectively).
- 3. The delay between 50% points.
- 4. Pulse stretching or shortening.
- 5. General pulse appearance neglecting minor deviations caused by wiring reflections, stray impedances, minor noise, etc..

Typical faults of the logic circuit shown in Figure 3-1 will be illustrated. The figures above the logic symbols are identifying numbers. The electrical circuit for each of the logic symbols is also shown. All waveforms will be with respect to ground and identified by a number and one of three letters: the number referring to those in Figure 3-1, and the letter referring to the base, collector or emitter. For example, waveform 5C refers to logic element 5 and specifically its collector. The odd numbered elements are grounded-emitters, the even numbered ones are emitter-followers.

The logic of Figure 3-1 is to illustrate the differences between lightly loaded and heavily loaded circuitry. Logic element 2, an emitter-follower is heavily loaded, unlike elements 4 and 6. This will affect the waveforms of elements 1, 2 and 3, and cause them to differ somewhat from those waveforms associated with elements 4, 5, 6 and 7.

The first case to be studied will be the control case, all circuitry normal. Then each diseased condition will be studied individually. The cases to be studied are (see Figure 3-1 for nomenclature):

CASE	ELECTRICAL FAULT	WA.	VEF	ORM	s sh	OWN	ī		,			
1	Everything normal.	1B,	1 C ,	2E,	3B,	3 C ,	4E,	5B,	5C,	6E,	7B,	7C
	Emitter Follower Troubles.											
2A	C to E of 6 shorted.							5B,	5C,	6E		
3 A	C to E of 6 leaky.						•	5B,	5C,	6E,	7B,	,7C
4A	Open E of 6					•		·5B,	5 C ,	6E,	7B,	7C
5 A	R _E of 6 open	ř.						5B,	5C,	6E,	7B,	·7C
6A	Open B of 6								5C,	6E.		
7A	Open C of 6							5B,	5C,	6E,	7B,	7 C
2B	C to E of 2 shorted	1B,	1C,	2E								
3B	C to E of 2 leaky	1B,	1C,	2E,	3B,	3C						
4B	Open E of 2	1B,	1C,	2E,	3B,	3 C						
5B	R _E of 2 open	1B,	1C,	2E,	3B,	3C				•		
6B	Open B of 2		1C,	2E	·							
7B	Open C of 2	1B,	1C,	2E,	3B,	3C					•	`
("A" cases are lightly loaded and "B" cases are heavily loaded circuitry.)												
	Grounded Emitter Troubles	1					i.		,			
8A	C to E of 5 leaky)				,	,	5B,	5 C	,		
9A	Open E of 5			,			,	5B,	5C		<u>.</u>	
10A	R _B of 5 open	•			Ċ		4E,	5B,	5 C			
11A ·	C _B of 5 open						4E,	5B,	5 C			
12A	R _C of 5 open		•				4E,	5B,	5C,	6E,	7B,	7C

CASE	ELECTRICAL FAULT	WAVEFORMS SHOWN
13A	R _B of 5 shorted	4E, 5B, 5C,
8B	C to E of 3 leaky	3B, 3C,
9B	Open E of 3	3B, 3C
10B	R _B of 3 open	2E, 3B, 3C
11B	C _B of 3 open	2E, 3B, 3C
12B.	RC of 3 open	2E, 3B, 3C, 4E, 5B, 5C
13B	R _B of 3 shorted	2E, 3B, 3C

^{(&}quot;A" cases are driven from a lightly loaded emitter-follower, and "B" cases from a heavily loaded one.)

Careful distinction should be made between the symptom, the electrical fault, and the actual fault. The logical error and the defective waveforms are the symptoms. The electrical faults listed are functionally what is wrong. The actual fault is the defect itself. For example, cases 10A and 13A, respectively list R_B as open or shorted. As a circuit function this may occur, but almost never because R_B itself is open or shorted, but usually because of a poor solder joint, a broken printed circuit line, a shorted printed circuit line, etc.

As a large variety of actual faults may cause the same electrical fault, it is more convenient to classify faults according to the electrical malfunction.

All waveforms for each case are clearly labelled. All time scales read from left to right and are 0.1 microsecond/cm except for case 100 which is shown at 500 microsecond/cm to mustrate a peculiar symptom of the disease. All ground levels are labelled -->!! for reference. These waveforms apply to the use of the following Tektronix oscilloscopes, models 531, 535, 541, 545, or 551.

Consider Case 1 with everything normal. Note carefully the levels, the pulse widths, the pulse shapes and "rise" times. Compare 6E to 2E, 7B to 3B, and 5C to 1C, and note particularly the difference in

levels attained, the pulse shape and rise times. Elements 5 and 6 are lightly leaded, and 1 and 2 heavily leaded circuitry. Note that the pulse width from 1B to 5B or 7B has not changed. Take careful notice of the relationship of the levels (the steady state or flat tops of the pulses) both negative and positive with respect to ground.

Observe that the positive going signal on the emitter of a heavily loaded emitter-follower (2E) is unable to follow the driving collector (1C) as well as a lightly loaded one (4E following 3C). This is because the large load capacity will not allow the emitter voltage to change rapidly and the base going swiftly positive temporarily cuts the emitter-follower off (i.e., non-conducting). The lightly loaded emitter-followers remain on at all times and biased in the active region of the collector characteristics. Do not pay undue attention to trivial details in waveforms such as slight oscillations or hash (often seen on cascaded emitter-followers with long lengths of back panel wiring attached). As long as these are small and beyond the discrimination levels, they are of little significance. However, do not neglect any malformations that extend into the discrimination levels or are causing malfunctions or false signals.

One must become very familiar with the above normal waveforms. They should be memorized and one should be able to sketch them to scale from memory. Note in particular the levels, rise times, and delays. These are the normal waveforms and all fault deviations will be described as the deviation from these normal waveforms.

Emitter-follower defects will be located in element 6 for the lightly loaded case, and in element 2 for the heavily loaded case.

Consider cases 2A and 2B, a collector-to-emitter short. This is most readily recognized as the emitter (6E and 2E) approaches the negative supply voltage (-3.5V) regardless of the base signal. Note also that the negative level of the driving collector (5C and 1C) is more negative than normal since transistor action is lost and the base to emitter diode is now back-biased. This is more noticeable in the heavily loaded cases (1C).

Cases 3A and 3B illustrate an intermediate condition, a leaky collector-to-emitter. Note that the driving collector negative level increases and the emitter's positive level becomes more negative. The emitter's negative level tends to become more negative than normal, but is often difficult to note. This overall negative shift and compression of

the signal tends to bias the following bases negative (7B and 3B) holding these transistors "on" or their collectors positive (7C and 3C). It does not take much excess leakage current to cause malfunction.

Cases 4A and 4B illustrate an open emitter of an emitter-follower. Note that the driving collector (5C and 1C) appears as in cases 2 and 3, but that the emitters (6E and 2E) are now greatly positive (instead of negative) regardless of the signal on the base. (See also case 6, which is similar.)

Cases 5A and 5B illustrate R of an emitter-follower being open. Again, the driving collector appears as in cases 2, 3 and 4. The driven bases (7B and 3B) will be held negative as in case 3. This case may most readily be differentiated from the preceding cases by the very great increase in positive going-rise times, as seen on the emitter (6E and 2E). This is because the discharge path for hole storage through the following bases is interrupted. This case is very often mistaken for a leaky emitter-follower. The tell-tale increase in positive-going rise time is the clue. Loss of positive voltage (general or local) will cause similar waveforms.

Cases 6A and 6B, an open base of the emitter-follower, cannot be differentiated from an open emitter (case 4) while in situs but both cases correctly identify the transistor as the villain. See discussion of case 4.

Cases 7A and 7B, an open collector of an emitter-follower, may be recognized by the clamping of the collector of the driving transistor (5C and 1C) to a positive voltage, being much more positive than the positive discrimination level. This collector waveform is reproduced at the emitter (6E and 2E) and the driven base (7B and 3B). As these bases are always held positive, the driven transistors collectors are always negative. (7C and 3C). This case is similar to case 12 and often both possibilities must be tried.

Cases 8A and 8B, a leaky grounded-emitter can generally be recognized when severe, as a material decrease in the negative level. All other aspects of the waveform are normal. In the early stages of increasing leakage current, it is often difficult to find the fault directly, and must be found by more sophisticated methods as described previously under grounded emitter failures.

Cases 9A and 9B, an open emitter of a grounded-emitter, can be recognized by its distinctive base waveform (it being like that from the driving emitter) coupled by its collector being held negative.

Cases 10A and 10B and 10C, R_B being open, can be recognized for high repetition rate pulses by its base waveform being similar to the driving emitter and the entire waveform shifted positive. This case may not cause trouble in certain low repetition rate negative input pulses as illustrated in case 10C repeated for a low repetition rate on a 500 microsecond/cm scale. The base waveform shows a distinctive discharge time constant, but the collector waveform is "normal". As the repetition rate is increased, "failure" will eventually occur. Positive input pulses will always fail in this fault.

Cases 11A and 11B, C_B being open, is recognizable by the large increase in hole storage delay (i.e., large increase in the delay of the positive-going input pulse) and the distinctive distortion of the base waveform. At the base, this increase in hole storage delays tends to stretch negative-going input pulses and shrink positive-going input pulses. Compare 5C to 3C of this case.

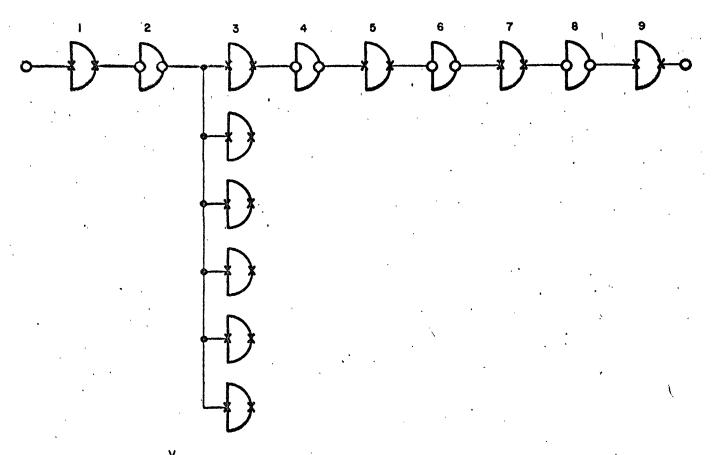
Cases 12A and 12B, R being open is very difficult to distinguish from case 7, and often both cases must be considered. See discussion of case 7. Local or general loss of negative voltage will give similar results.

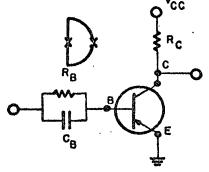
Cases 13A and 13B, a shorted base resistor R_B, often is not noted as such until excessive power dissipation in the base to emitter diode causes the grounded emitter state to become leaky. It can be recognized by the driving emitter waveform appearing directly on the base. This fault often does not cause functional failure except where the slight increase in delay (due to heavy saturation of the grounded emitter stage) or the heavy loading effect (in heavily loaded driving emitter-followers) will cause associated circuit functions not to propogate properly.

CONCLUSION:

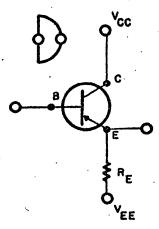
Normal operation and twelve varieties of faults under light and heavily loaded conditions have been discussed in detail (25 cases). Other varieties of faults provide such obvious symptoms (such as the collector always being negative of a grounded emitter whose base is open) that they are not discussed in detail. Notation has been made of the causes of most faults, their relative order of occurrence and remedies suggested.

3-15





GROUNDED-EMITTER



EMITTER - FOLLOWER

Figure 3-1 Illustrative Logic Circuit
3-16

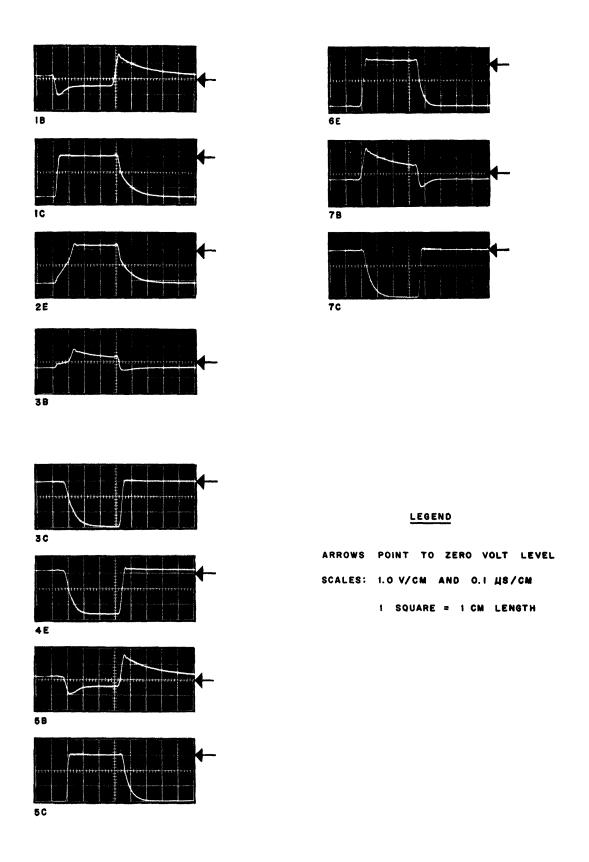
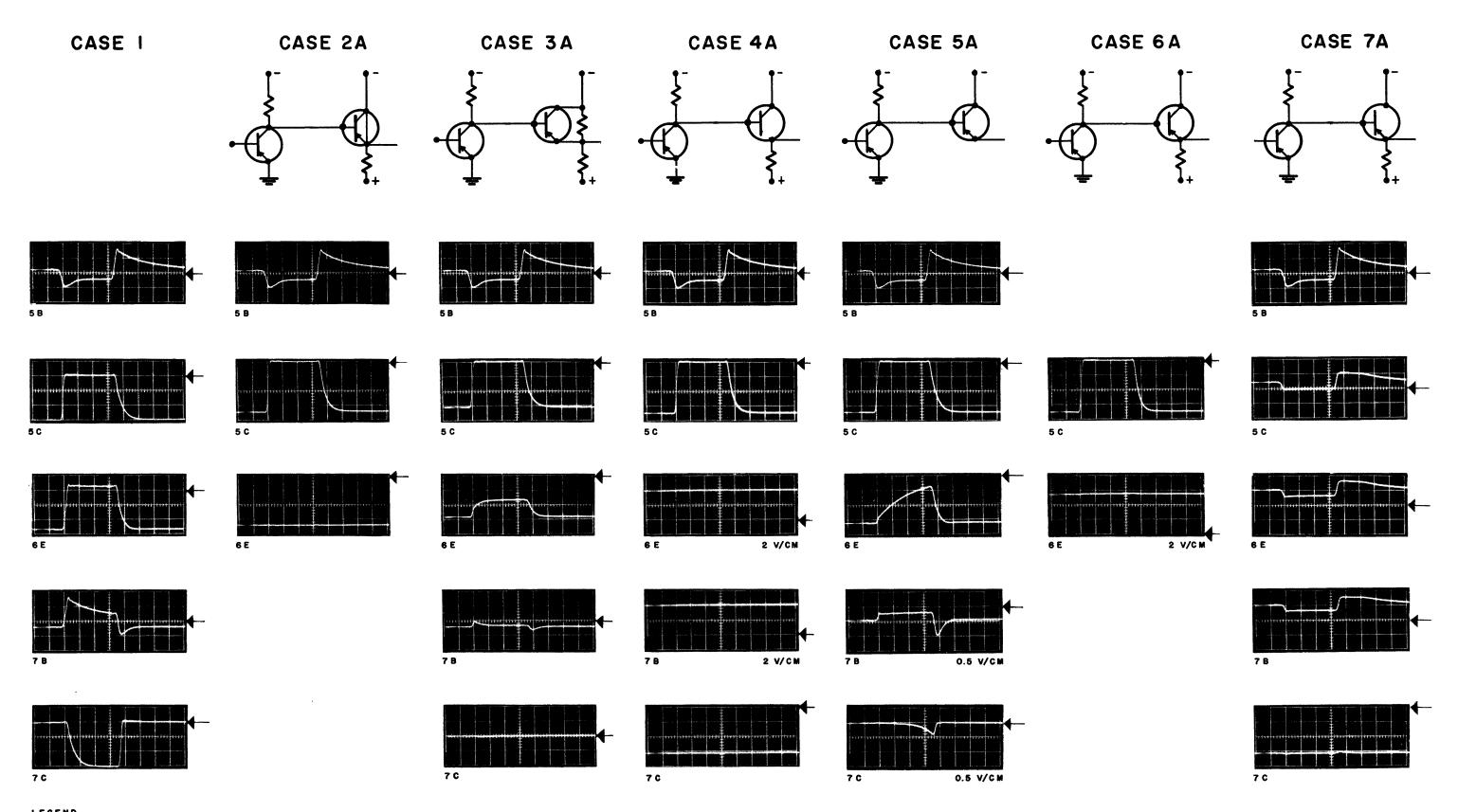


Figure 3-2 Case 1 Normal Circuit



ARROWS POINT TO ZERO VOLT LEVEL
SCALES: 1.0 V/CM AND 0.1 US/CM UNLESS OTHERWISE MARKED
I SQUARE = 1 CM LENGTH

Figure 3-3 EF Troubles
Light Loading

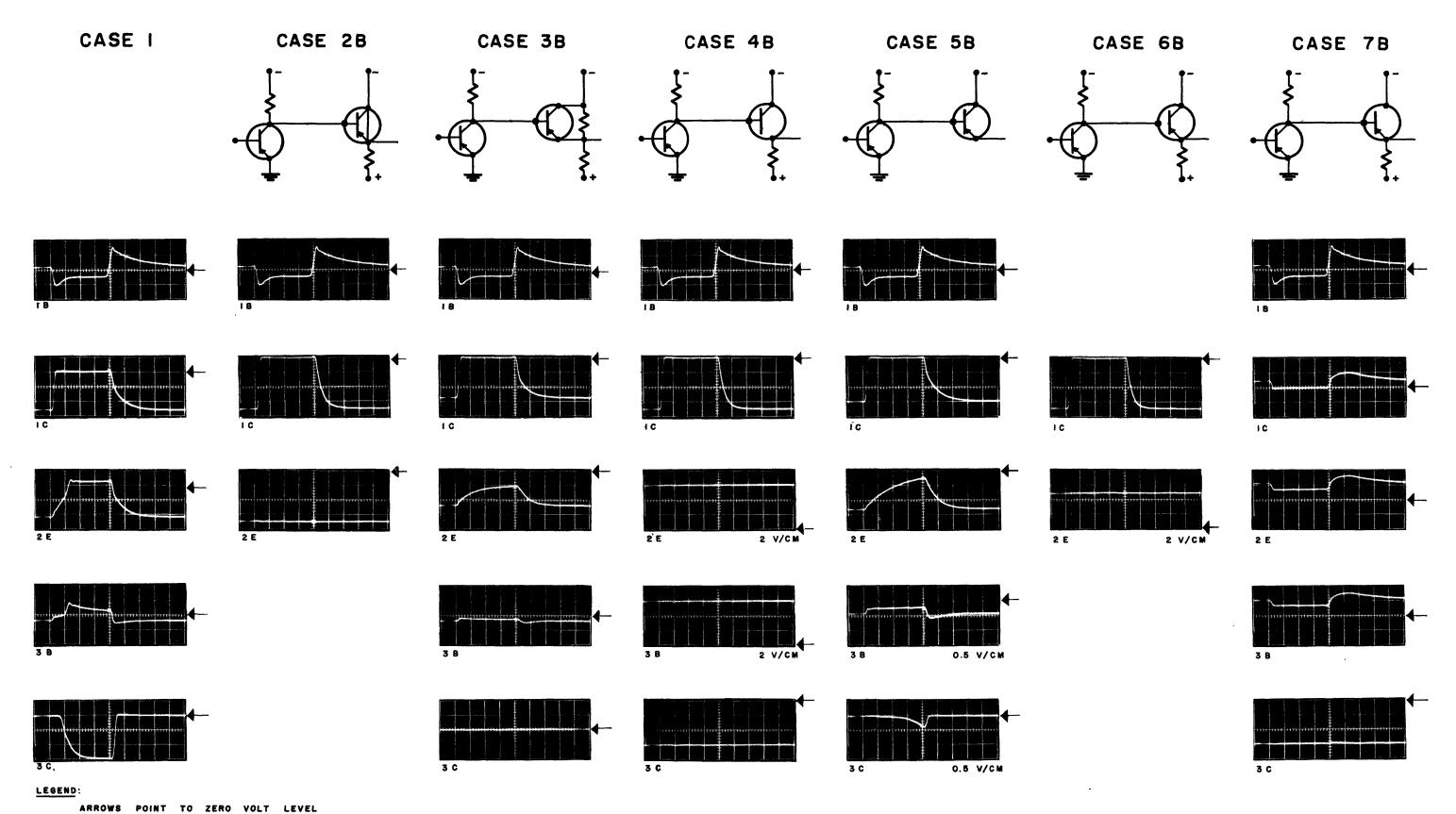


Figure 3-4 EF Troubles
Heavy Loading

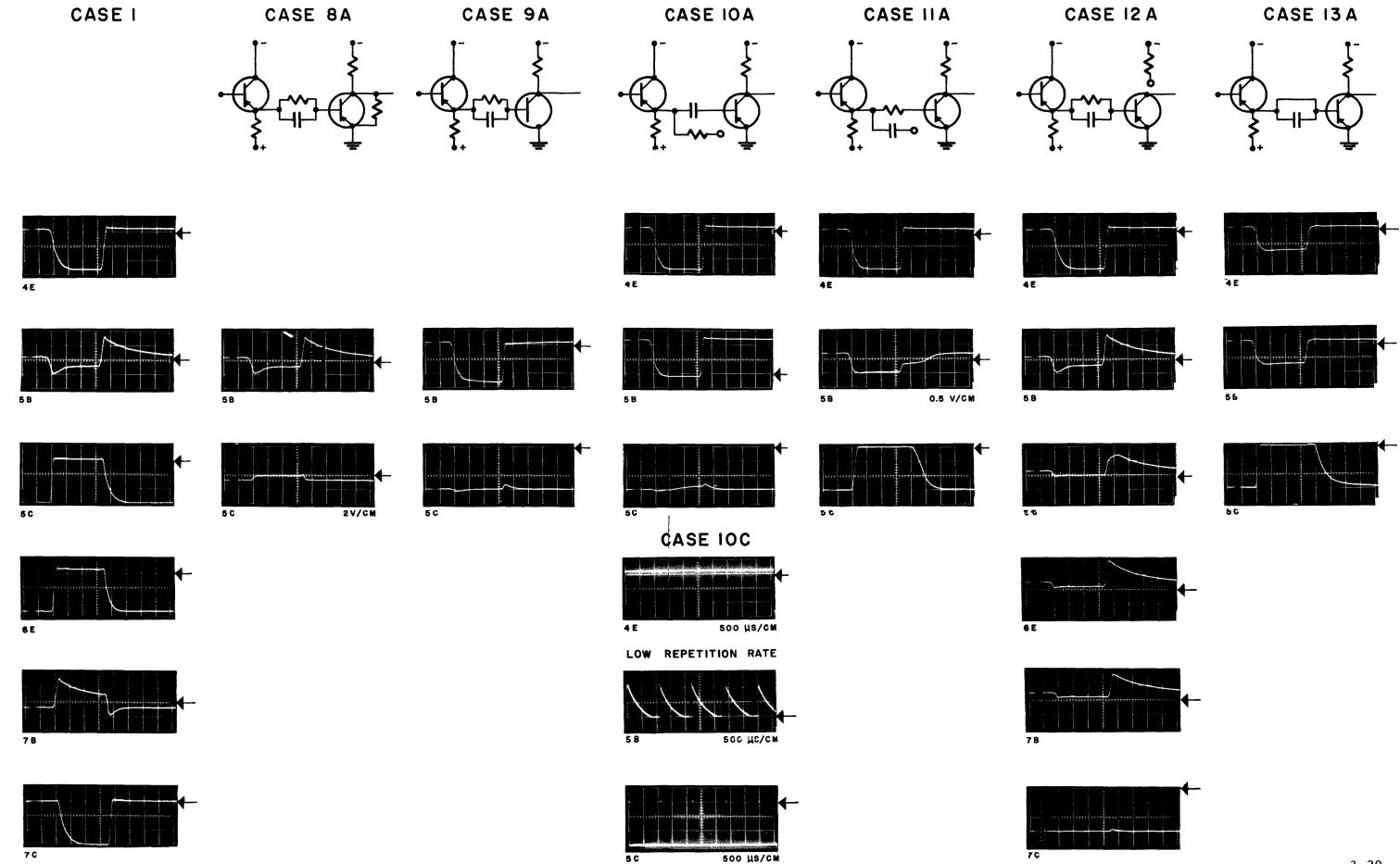


Figure 3-5 GE Troubles
Light Loading

LEGEND:

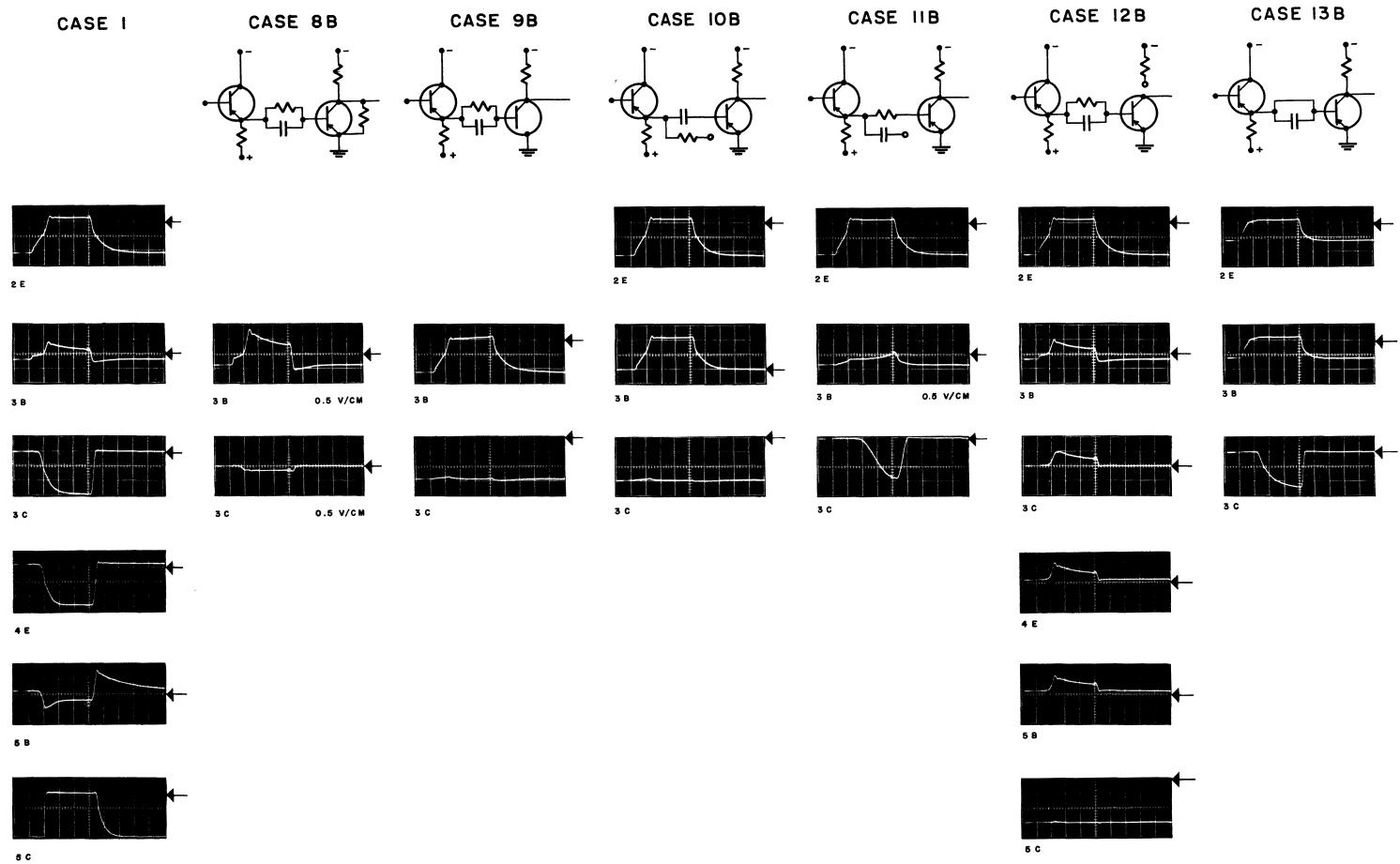


Figure 3-6 GE Troubles
Heavy Loading

Observation point: Base of grounded emitter

SYMPTOM	POSSIBLE ELECTRICAL FAULTS	POSSIBLE ACTUAL FAULTS
Base waveform normal in shape but reduced in amplitude and biased negative.	Leaky C to E of driving EF (case 3)	Leaky EF transistor; shorted printed circuit line; dirty card.
Base at highly negative level.	Shorted C to E of driving EF (case 2)	Same as above.
Base waveform distorted and held negative	R _E of driving EF open (case 5)	Poor solder joint; local or general loss of positive supply
Base waveform highly positive (+5 to +6 v).	Open E or B of driving EF (cases 4, 6)	E of EF burned open; poor solder joint.
Base waveform positive (+1.5 to +2 v).	Open C of driving EF (case 7)	Poor solder joint, local or general loss of negative supply.
Base waveform positive (+0.5 to +1 v)	R c of G.E. ahead of the driving E.F. is open (case 12)	Same as above.
Base waveform similar to that of driving E.F.	Open emitter of G.E. Open base of G.E. (case 9)	Poor solder joint.
At high repetition rates the base waveform is similar to driving E.F. but shifted positive. At low repetition rates there is a distinctive discharge curve.	Open R _B of G.E. (case 10)	Poor solder joint.
Positive-going rise is greatly increased and lack of normal overshoots.	Open C _B of G.E. (case 11)	Poor solder joint.
Base waveform the same as driving emitter but negative level decreased	R _B shorted (case 13)	Shorted printed circuit line.

Analyis of Symptoms

Table 3-1

Observation point: Emitter of emitter follower

SYMPTOM	POSSIBLE ELECTRICAL FAULT	POSSIBLE ACTUAL FAULTS
Emitter highly negative regardless of input signal. Signal if present is small	Leaky or shorted C to E (cases 2 and 3).	Leaky or shorted transistor; shorted printed circuit line; dirty card.
Emitter highly positive (about + 5 to + 6 v)	Open emitter or base (cases 4 and 6).	Emitter burned open; poor solder joint.
Emitter positive (about +0.5 to + 1.0 v) Does not go negative with signal.	R _C of driven G.E. open (case 12).	Poor solder joint; local or general loss of negative supply.
Emitter positive (about +1.5 to +2 v.)	Open collector (case 7)	Poor solder joint; local or general loss of negative supply.
Large increase in positive-going rise time.	R _E open (case 5)	Poor solder joint; local or general loss of negative supply.
Significant decrease in negative signal level at emitter.	Shorted R _B of driven G.E. Poor base connection of E.F. Leaky driving G.E. (cases 8 and 13)	Shorted printed circuit line about driven G.E.; poor solder joint about base of E.F.; damping resistor in tandem E.F.'s too high or poor solder joint; negative supply voltage too low; locally or generally; leaky driving G.E.

Observation point: Collector of grounded emitter

SYMPTOM	POSSIBLE ELECTRICAL FAULT	POSSIBLE ACTUAL FAULT
Significant decrease of negative level at collector. Flip-flop favors one side. Occasional false signals.	Leaky G.E. (case 8)	Leaky G.E.; dirty card; local or general loss of negative supply
Collector stays negative	Open emitter of G.E. Open collector of G.E. Open base of G.E. (case 9)	Poor solder joint. defective transistor.
Collector stays positive, signal shifted positive	R C of G.E. open Collector of following E.F. is open. (cases 7 and 12)	Poor solder joint; local or general loss of negative supply
Some increase in delay, particularly in the negative-going slope. (Often difficult to observe).	R _B of G.E. shorted. (case 13)	Shorted printed circuit line
Positive input produces no output; low rep. rate negative input is effective and high rep. rate fails.	R _B of G.E. open	Poor solder joint

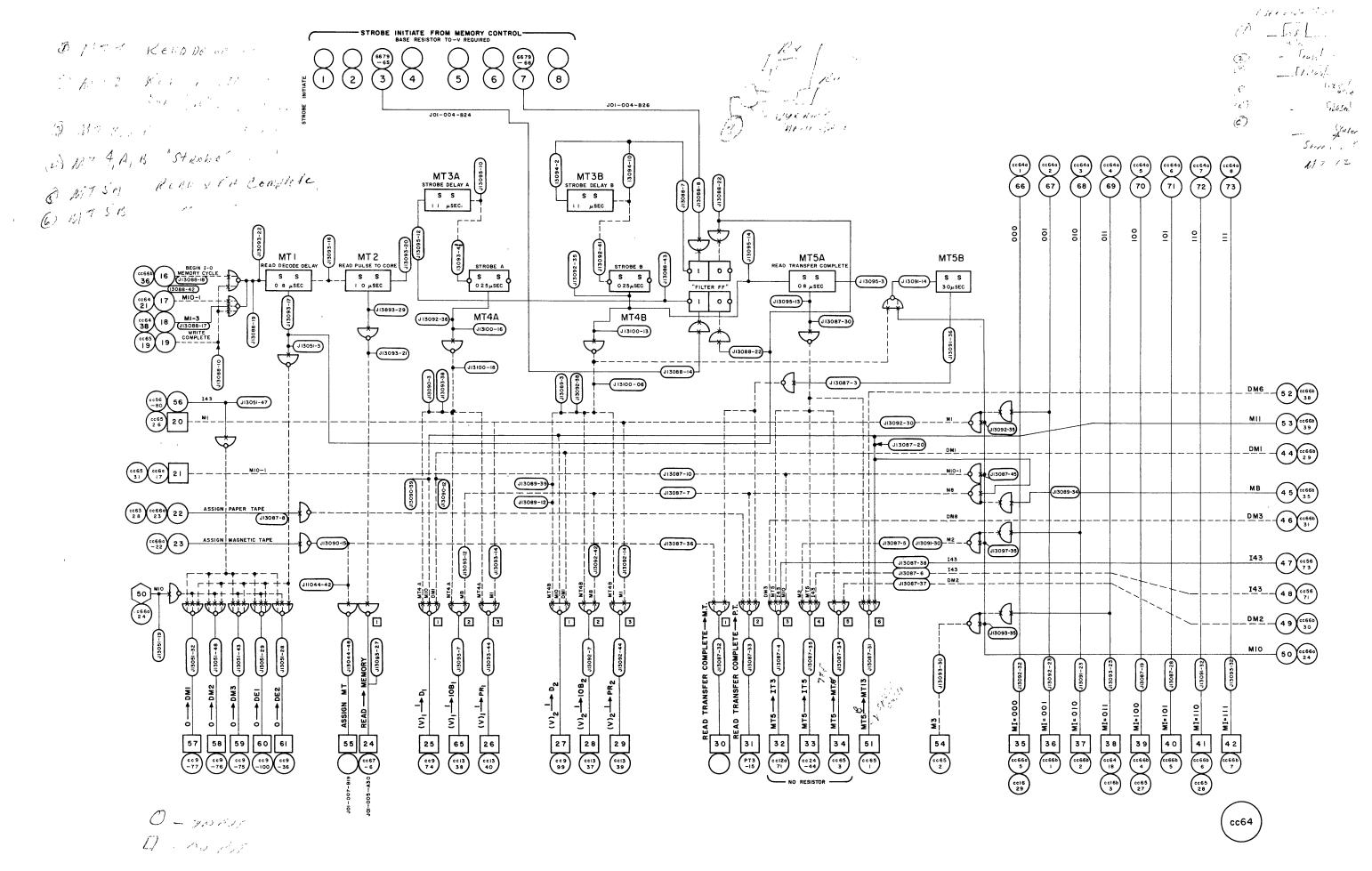


Figure 4-9 Memory Timing Chain for Read (Sheet 1 of 2)

4. MAGNETIC CORE MEMORY

4.1 PRINCIPLES OF OPERATION

MAGNETIC PROPERTIES

The use of magnetic cores as a storage device is primarily based upon two properties of certain ferromagnetic materials, remanence and non-linearity of magnetic response. The manganese magnesuim ferrites used display a large value of remanence, the amount of magnetization remaining after the removal of a magnetizing force. In these ferrites, the remanent level of magnetization approaches that induced by the magnetizing force and implies the ability to store recoverable information. The storage is termed non-volatile since it requires no external power to maintain it.

The non-linearity of the response implies a critical value of magnetizing force and the ability to discriminate in the selection of one, among many cores by proper application of magnetizing force values.

The existence of two possible polarities of magnetization readily lends itself to the storage of binary information.

B-H CURVE

An idealized major hysteresis loop of a ferrite with desirable response is shown Figure 4-1. +Bs and -Bs indicate the saturation levels of flux density, of the two polarities of magnetization; +H_M and -H_M the required magnetizing forces respectively. +Br and -Br represent the remanent levels of magnetization following the removal of the saturating, magneto motive force. The two polarities are arbitrarily identified as + and -. For binary information storage -Br is assigned to one binary value and +Br to the other. Conventionally the negative polarity is assigned to the binary one value. A binary one is stored by driving the core to saturation in the negative direction. Saturation in the opposite, positive polarity represents a zero. The read-out, a method of sensing information in a core is performed by driving it to saturation in the positive polarity. As reading always precedes writing, the core is in the zero condition just prior to writing. A zero is stored in a core by not writing a one.

The steep vertical slopes of the loop show that a relatively large voltage pulse will be generated as the core is driven from one saturation polarity to the other. The non-linearity, represented by the

horizontal components of the loop show that a magnetizing force of one half the saturating value will not switch the core's polarity. However, a relatively small value of voltage pulse will be generated during the application of $+ H_M / 2$ or $- H_M / 2$.

APPLICATION FOR INFORMATION STORAGE

As previously mentioned a binary one is stored by application of a current pulse producing a force of -H_M in magnitude. This termed "writing" a one. A binary zero would be stored by not writing a one. To determine this information at any time following, the core is readeout by the application of +H_M. As the generated voltage is a function of the rate of change of flux density, the difference in magnitudes of voltages generated by driving from -Br to +Bs in one case, and from +Br to +Bs in the other can be distinguished.

This read-out process is destructive as/the binary information is eradicated. An additional process is necessary to subsequently reenter the information in the core for continued storage.

CORE WIRING

Physically, the core is a toroid which is threaded by the read-write wires for the drive currents and a wire to sense the voltage pulse generated during reading. The threaded wires are equivalent to one-turn loops around the core.

CORE PLANE

The mass of binary information that must be stored requires an organization to minimize the complexity of selecting the desired core at any time. One memory unit of TRANSAC S-2000 stores 4096 words, requiring 196,608 cores.

The cores are arranged in a grid with the drive wires acting as coordinates. To illustrate with a simpler core plane than is found in the S-2000, Figure 4-2 shows an organization of 36 cores. Each column has a separate drive wire as does each perpendicular row. These are commonly known as X and Y wires. To select a particular core for reading or writing currents are energized in the appropriate X and Y lines. The current in each line only produces an $H_{\rm M}/2$ force. Only the selected core, where the currents coincide is capable of being switched. The other cores threaded

by that pair of X and Y lines are termed "half selected". Referring to Figure 4-1, the effect of \pm H/2 can be determined. It should be noted that the half selected cores do radiate a varying magnetic field while driven. The design of the core storage cannot ignore this undesirable response. This matrix of cores is usually referred to as a "core plane".

For convenience of core selection in binary machine, the number of cores in a plane is usually a power of two.

MEMORY ORGANIZATION

The logic of storage use determines the minium complexity of the storage system organization. Required is a system of storing a number of multi-bit words where-in access to only one word is required at any monent. If the computer is a parallel machine with each information bit simultaneously required, storage is best organized so that the number of core planes equals the number of bits in a word. Each bit of the word is stored in a different plane. All the planes are driven by the selected pair of X and Y lines.

Each core plane represents the same bit value for all words. The number of cores in a plane therefore equals the number of words stored. If only one word is accessed at any time only one sense winding is required per plane. A third function in each plane is provided by the "inhibit winding". Each core has one such winding.

READ AND WRITE

To read a core-currents are driven through the selected X and Y lines, their direction of current flow driving the core at their coincidence to +Bs.

The same X, Y lines can be used for writing (into the cores) with currents of the opposite polarity applied to the planes, if an additional inhibitory force is applied to those planes whose bit value should remain zero. This implies that all cores of the selected word were in the binary zero condition before writing. This is the condition following read. Where a core is to remain zero, the inhibit current of $+H_{\rm M}/2$ value is applied for a net force of $-H_{\rm M}/2$ at the selected core. See Figure 4-3. A single inhibit winding suffices for the plane as only one core is selected.

MEMORY CYCLE

A standardized control sequence is indicated by the methods of reading and writing. The memory cycle consists of a read followed by a write. The variable is whether a zero or one is written. If the operation required is a transfer of information from memory, the information sensed during read is stored in the flip-flop of a register after passing through sense amplifiers. Each bit is simultaneously transferred; the read process driving all selected cores to zero. During the write part of the memory cycle the information is reentered in the cores. Each inhibit winding is controlled by one of the flip-flops and is active during the write operation if a flipflop represents a zero.

When transferring to memory from a register the read operation is used to clear the selected cores to zero. The information sensed during the reading of the cores is not utilized. During write the register flipflops again control the inhibit windings.

UNDESIRED CORE RESPONSES

The response of the half selected cores lying along the pair of X, Y lines must be considered as they receive a magnetizing force of $+ H_{\rm M}/2$ during read. Figure 4-4 illustrates the remanent flux density of core that was initially saturated to $-B_{\rm S}$ and subsequently received a series of $+ H_{\rm M}/2$ pulses. HR, 2R and 3R are the remanent values after one, two and three Half Read ($+H_{\rm M}/2$) pulses. The change in density for $-B_{\rm R}$ to HR is considerable due to the non-linearity of the toe region of the B-H curves. Following this first half read the rate of change decreases rapidly and the remanent value effectively stabilizes in the region of 4R.

Another group of responses accurs when the operating conditions of the half selected core are a sequence of Half Read and Half Write pulses alternately (HR, HW, HR, HW...) These conditions occur when a "l" was read from the selected core and reentered in that core during write. Also, if the half selected core were along the Y line it would receive - H_M/2 during write even if a "0" had been read from the selected core. The inhibit line is run parallel to the X line.

The remanent values for this sequence are indicated as HR; HR, HW; HR, HW, HR; HR, HW, HR, HW. The response tends to stabilize around a closed minor loop containing the latter two points.

STROBING

A distinction can be made between the signal generated by a selected core switching from "1" to "0" and the undesirable noise of the half selected cores. The shape of the voltage pulse from the half selected core is a function of the rate of change of current amplitude. This pulse will peak at time t₁, in Figure 4-5. The selected core does not begin to switch until some time after +H_M has been reached. The signal peak occurs later than t₁. By sampling the sense output at the moment the signal can be expected to be at a maximum, the effect of noise is reduced. This procedure is termed "strobing". The strobe pulse is generated by using the the read drive current to trigger a delay circuit. In this way close control is kept of the timing.

SENSE WIRE ROUTING

In order to further reduce noise effectiveness, the sense winding is threaded thru the core plane so its orientation to the magnetic fields of half of the cores is in one direction and its orientation for the remaining half of the plane is in the opposite direction. Noise generated by the half selected cores will tend to cancel as the total number of half selected cores in the plane is an even number. This requires that the sensing amplifier circuits be responsive to signals of either polarity as the orientation of the selected core will determine the polarity of the switching voltage across the sense winding.

CORE ISOLATION AND WIRE ROUTING

To minimize the magnetic field coupling between cores they are positioned to be perpendicular to their immediately adjacent cores. Figure 4-6 shows the core arrangement and wiring methods for another small plane. The final consideration for wire routing was to simplify, as much as possible, the threading of wires through the cores for plane assembly on a production scale.

4.2 PHILCO-2000 MEMORY ORGANIZATION

One memory unit stores 4096 words, 48 bit word length (2 12 = 4096)

Each bit of a word is stored in a plane of 4096 cores arrayed as a 64 x 64 matrix. The arrangement is similar to that of

Figure 4-6. All cores in a plane represent the same bit value for 4096 words.

The 48 planes are stacked vertically in two groups of 24 planes each. The separation into two groups of 24 is necessary to limit the inductance of a circuit to a value that permits attaining the required current rise time. These two "half stacks" (termed "A" and "B") comprise the memory unit. See Figure 4-7.

The 48 bits of a word are stored in cores lying along an axis perpendicular to the planes. Each X line threads through the 24 planes in serial fashion, as does each Y line.

Each plane has a separate sense winding threaded diagonally through the matrix.

Each plane has a separate inhibit winding threaded parallel to the X lines.

The memory unit is maintained at a controlled ambient temperature of 40° C $\pm 2^{\circ}$ for optimum performance.

The computer can control up to a maximum of 8 memory units (32768 words or approximately 1 1/2 million bits).

ADDRESS SELECTION

A word location in memory is accessed by decoding the memory address to select on X and one Y line. (The division of the memory unit into two half stacks will be monentarily ignored.) An individual line is selected by the combination of energizing one "switch" and one "driver" circuit.

The switch enables either of two drivers to be effective while one of the latter is turned on. With 64 X and 64 Y lines, 32 switches are required for the 32 pairs of X lines in the half stack. Thirty two switches are required for the Y lines in the half stack.

The pair of lines connected to a switch are called the "O" line and the "line. One driver connects to all the O lines and another driver to all of the 1 lines. One pair of drivers is required for read; another pair for write.

The circuits of the A half stack for example, will therefore total as follows:

Function	Number Total	Names
X Lines	64	
Y Lines	64	
Switches	64	32XA switches 32YA switches
Drivers	8	Read 0 X Read 0 Y Read 1 X Read 1 Y Write 0 X Write 0 Y Write 1 X Write 1 Y

The B half stack has its own 64 switches and is driven by another set of eight drivers.

The twelve bit address is decoded as follows:

2 ⁰ through 2 ⁴	select one XA and one XB switch
2 ⁵	select (in conjunction with memory timing signals) the two R0 or the two R1 drivers for X and subsequently the two W0 or the two W1 drivers for X.
26 through 210	select one YA and one YB switch
2 ¹¹	select the drivers for Y (in the same way as for X).

Figure 4-8 illustrates the selection method. The sixth bit (2⁵ for X and 2¹¹ for Y) is gated with the function signals (Read, Write) from the Memory Timing chain. If more than one memory unit is connected to the computer, up to three additional address bits are required. This additional level of decoding is added as indicated to select one of up to eight

sets of drivers for the 32,768 word memory.

At any one time, four drivers can be energized, two for X and two for Y. The switches are operative over the entire memory cycle. The function signals determine the operative time of the drivers.

STROBE INITIATE

At the Strobe Initiate must be closely related to the rise time of the drive currents these signals originate in the read driver circuits themselves. The signals from the operative Read X and Read Y drivers in a half stack are matched in an AND gate to insure proper timing before being sent to the timing chain control circuits. The two half stacks provide separate origins for the two Strobe Initiate signals to allow for individual circuit variations.

SENSING

The 48 sensing lines in the memory unit one for each plane. are connected to the sense amplifiers. The amplifier outputs are mixed with similar output lines from the other memory units in the sense network; each of whose 48 output lines goes to a flipflop in a register through Switch 8 during a transfer from memory.

INHIBIT

For transfer to memory, whether it be information just read out or new information, the 48 flipflops of a register will control the inhibit drivers through Switch 3 and memory unit selection. If a flipflop is reset to zero, the associated inhibit driver for the plane is energized.

4.3 MEMORY TIMING CHAIN

The memory cycle is controlled primarily by a group of singleshots (the "MT" singleshots) which are sequentially active. They are consecutively numbered in ascending order (Figure 4-9).

MT 1, the first in the chain, provides an interval for the decoding of the memory address to select the four switches. When the memory is assigned to the computer, M 10 becomes active (ref. 6.3.3, "Memory Assignment"). M 10 activates the (MA) —SW7 signal which

transfers the address to the decode network. As M.10 will be active until the assignment is completed, the switches remain selected during the memory operation. (If the memory cycle were for an I-O transfer, Mll active causes (IOMA) \rightarrow SW7). The circuitry requires time to respond and MTI (approximately 1.2 μ s) serves that purpose.

Initial control clearing is also performed at this time. The end of MT 1 triggers MT2.

MT2 energizes the two selected read drivers to pulse an X and Y line in each half stack.

The timing of the next action in the sequence is controlled by the memory itself. The Strobe Initiate signals are taken from the outputs of the two read drivers (X and Y) in each half stack. (See Figure 4-10, Read Driver, "Output to C C.") Essentially it indicates when the currents in both X and Y reach the required amplitude. These signals returning from the X and Y drivers in the half stack are ANDed together. The gate output is the Strobe Initiate. Each half stack independently develops its Strobe Initiate signal. This is discussed on page 4-12.

As previously described an interval occurs between the application of the required currents and the switching of the cores. The information stored in the cores will not be available until the cores switch.

The Strobe Initiate is therefore used to initiate the timing of this delay prior to actually strobing the sense amplifier outputs. The Strobe Initiate sets 1 to the Filter flipflop. The 1's output of the flipflop triggers the MT3 single shot. MT3 provides the delay required to the moment of core switching. The end of MT3 triggers the MT4 singleshot which provides the actual strobing signal. During MT4's active period, the ones from the sense amplifiers are transferred to the appropriate register (PR, D or IOB).

The MT4B (B half stack) also triggers MT5A and MT5B the singleshots for the Read Transfer Complete timings. These control activities at the end of the read for computer and input-output respectively.

(Assuming that an uninterrupted memory cycle is in progress, the sequence of MT's will be continued./

In this case MT5A, while active, clears the M display

register. The end of MT5A triggers MT7 and MT8. (MT6 is the address decode delay which is needed only for a split memory cycle. It is bypassed when proceeding to write immediately following read.)

The inhibit drivers are energized before the write drivers to insure the former will be fully on while writing. MT7 permits the register (D, PR or IOB) to pick up the inhibit drivers. MT8 provides a delay before turning on the write drivers.

The end of MT8 triggers MT9 which energizes the write drivers. The active periods of MT7 and MT9 overlap.

MT8 also triggers MT10 which transfers the information being written to the M register as well. (If the MA = MP control is being used to stop the computer, the Stop FF is set to 1 at this time.)

The end of MT10 triggers MT11 which commences the control operations for ending the memory cycle.

If the computer is to proceed to IT3 or IT5 from this point, MT11 will set the associated IT timing flipflop, to 1.

MT11 also sets a 1 to MT13, which is the only MT flipflop in the memory timing chain. At the end of MT11, MT13 will clear MI to zero, making M0 active. MT13 will also initiate a memory assignment sequence.

The control activities at the end of a memory cycle are performed during MT11 to permit the computer to proceed as soon as possible after the information has been transferred to memory. However, another memory cycle cannot be initiated until sufficient time has elapsed for the write and inhibit currents to be attenuated. MT12 furnishes part of this delay. It is triggered by the end of MT11. While MT12 is active, it prevents the initiation of a memory cycle. The total delay in this instance is the time of MT11 plus MT12.

In the case of a split memory cycle, MT5B provides the required delay, equivalent to MT12, before initiating the memory assignment sequence. (MT5B is about $3 \mu s.$)

The periods of the singleshots shown in Figure 4-9 are nominal. The singleshots are adjusted to provide optimum performance of each memory.

The action of the Filter flipflop configuration permits only the first pulse appearing on the Strobe Initiate Line after MT1 to be accepted as a genuine Strobe Initiate signal in a memory cycle. The write driver current, for example, will generate noise on the Strobe Initiate signal line. This is ineffective as the flipflop is already set to one and MT3 cannot be retriggered.

4.4 MEMORY CIRCUITS

namely:

Figure 4-10 shows all the types of memory circuitry,

Read Driver
Write Driver
Switch
Sense Amplifier
Inhibit Driver

The X and Y lines are transformer coupled to the drive circuits. A line is pulsed by a combination of a low impedance connection to - 15 v (through the final transistor of the switch) to one side of a primary winding is provided by turning on a switch. The other end of the primary is connected to ground via the grounded emitter stage of the driver.

The dot notation at the windings indicate the opposite directions of the read and write currents/

A test terminal is provided at each secondary winding for observation of the current waveform through the 1 ohm resistor?

Switch

The switch contains a grounded emitter input stage followed two stages of current amplification through PNP emitter followers to drive the bases of the four transistors connected to the pulse transformer windings. In the normal, or unselected state of the switch, T1 is on.

When selected its input is made positive. T2 and T3 provide the amplication necessary to drive the base of the one output transistor (T6, T7, T8 or T9) connected to an Read or Write Driver and transformer winding. The switch input is normally held negative. This is the computer logical - 3.5 nominal level. The bases of T6 through T9 are biased off, being

held at approximately ground level.

When a switch is selected, its input level is raised to ground, cutting off the input stage and driving the final stage bases to approximately - 15 v.

The NPN diode - connected transistors provide the means of rapidly discharging the distributed capacitance of the circuitry to ground. This is required when attempting to deactivate the switch at the end of the memory operation. During the time the switch was active (selected) this capacitance charges to approximately 15 volts, at the emitters of T2 and T3 for example. When turning off the switch, this charge can be dissipated through the NPN's and T1.

Read Driver

The read driver contains two stages of signal level conversion (from 3 to 6 to 12 volts). These are followed by complementary symmetry emitter followers which drive the base of the output PNP stage. The collector of the latter is connected to the pulse transformer through the adjustable RC network which enables adjustment for optimum rise time of the read driver pulse. The nominal value of the half current is 375 ma.

The Strobe Initiate Pulse is sent to the memory timing controls through the NPN emitter follower connected to the driver output stage.

The read driver input is normally positive, holding its end of the transformer primary winding at the -15 v, level.

During the active period of MT2, the input goes negative, bottoming the input stage. Its collector goes to ground driving the base of the NPN in the next stage. Through the two emitter followers the output stage is switched on to pulse the transformer winding.

The terminal labeled "Output to CC" is wired to the circuits shown on sheet CC 79 of the schematic logic. The positive, active Strobe Initiate signal passes through an OR gate composed of NPN transistors, and then an inverter. The coincidence of the X and Y line Strobe Initiate signals for the half stack is then tested for by the emitter follower AND gate.

REDUCTION OF TRANSISTOR TURN-OFF TIME

In order to reduce the memory cycle time it is necessary to limit the operating time of the memory circuits to the time required for response. To extend the period beyond this time serves no useful purpose. For example to maintain the read current beyond the period necessary to switch the cores is undesirable as it increases the total length of the memory cycle. Similarly for the write and inhibit drivers. It is advantageous to turn them off as quickly as possible.

It is necessary to drive the output stage into saturation to achieve the required current and rise time. The size of the coupling capacitor to the base of the final stage, 0.02 ufd, is an indication of the desired speed and current amplitude. In turn-off, therefore, a means must be devised to reduce the minority carrier stage time in the base. In the case of the PNP transistors used as the final driver stage, the concern is with hole storage in the base.

A complementary symmetry circuit is used (Figure 4-11). When the driver is activated the input goes negative and the PNP emitter follower drives the base of the final stage heavily into saturation. A base-emitter current of the magnitude of 200 ma., has electron flow from the base terminal into the base region of the transistor, T3:.

When subsequently deactivating the driver, the input is made positive. This turns off Tl and turns on T2, the NPN emitter follower. T2 and T3 lie across a 6 volt supply through base-emitter of T3 and the emitter-collector of T2.

A large current source is available with the current amplification through T2 to dissipate the hole storage in the base of T3. This current in T3 (electron flow away from its base terminal) is referred to as the "reverse base current" to distinguish it from the base current of a turned-on transistor.

It is necessary to have two cascaded stages of complementary symmetry emitter followers to achieve the required base current amplitudes at T3.

A similar result is effected by the capacitor of an RC coupled base. The energy stored in the capacitor while the transistor is on (base current charges the capacitor) is used as a current source to supply the reverse base current when turning off the transistor.

CLAMPING LEVEL

It is necessary to protect the transistors against exceeding their rated voltage. The situation arises from the counter e.m.f. generated by the highly inductive core circuit as the read (or write) current pulse is ended.

The diode-connected transistor, on the output line, clamps it to a level slightly more negative than - 15 volts as the current through the X or Y line is cut off.

WRITE DRIVER

The driver is identical to the read driver, aside from lacking the Strobe Initiate stage. This is, of course, not required during the write timings. The adjustable network of the output line is also not required.

INHIBIT DRIVER

The inhibit driver is a duplicate of the write driver, except that the former must drive a larger number of cores. The inhibit

must drive an entire plane (64×64) whereas the write drives one line in each plane of the half stack (64×24). The supply voltage of the output stage of the inhibit driver is accordingly raised to - 32 volts. The driver is direct coupled to the inhibit winding.

A diode-connected transistor is placed across the inhibit winding to shunt the current generated by the counter e.m.f.

SENSE AMPLIFIER

This amplifier, in addition to providing the necessary amplification from approximately 60 millivolts to 3 volts, has two other requirements. It must respond to a signal of either polarity. The orientation of the sense winding through the core determines the polarity of the induced voltage when the core switches (ref. "Sense Wire Routing").

The sense amplifier must also discriminate against noise due to the inductive and capacitive pick-up on both lines of the sense winding in the core plane. The noise is primarily generated by the read, write and inhibit currents. The stack is shielded to minimize external noise pick up.

This noise would seriously interfere with reading memory as the signal-to-noise ratio would be low and the timing of the strobe (examing the output of the sense amplifier) is critical. The noise, if permitted to influence the amplifier would require amplifier recovery time considerations.

The largest component of the noise is "common mode" noise, wherein the same polarity is generated on both lines of the sense winding with respect to ground. Discrimination can be made against common mode noise

A balanced input and differential amplifier circuit is used for these purposes. It is responsive only to a difference of potential between the two sense winding terminals (S1, S3 of Figure 4-10) rather than a potential to ground.

As amplified by the two NPN transistors, the signal coupled through the transformer will be the potential between the primary winding terminals 1 and 4. Common mode noise will alter the currents in each half of the primary winding, both either increasing or decreasing.

The net difference across the entire winding is zero.

A switching core will induce a potential difference between S1 and S3 terminals. The current through one half of the primary winding will increase as the current in the other half winding decreases.

The secondary winding circuit responds to a signal change. One of the two PNP transistors will turn on, cutting off the following grounded emitter stage. After further amplification to attain the computer circuit levels, the sense amplifier output is taken from an emitter follower. The sense amplifier output is normally negative (3 volts) and ground if a one is sensed during the read.

Amplifier adjustment is available so that the timing of the 24 sense amplifiers in the half stack can be matched. The PNP transistors, 354-3008-1, are specially selected for their base characteristics. The value of the collector resistor of the preceding stage determines the signal level at the base of 354-3008-1. The resistor value is selected during debugging to provide the desired timing of the sense amplifier output.

It might be noted here that when a one is being written the sense amplifier will respond. Time is allowed for the amplifier to recover at the end of the memory cycle.

The diodes shunting the secondary winding protect against transients that may be created during power turn on or turn off. They will hold the emitter level to + 0.6 volt or less positive and load down the transformer.

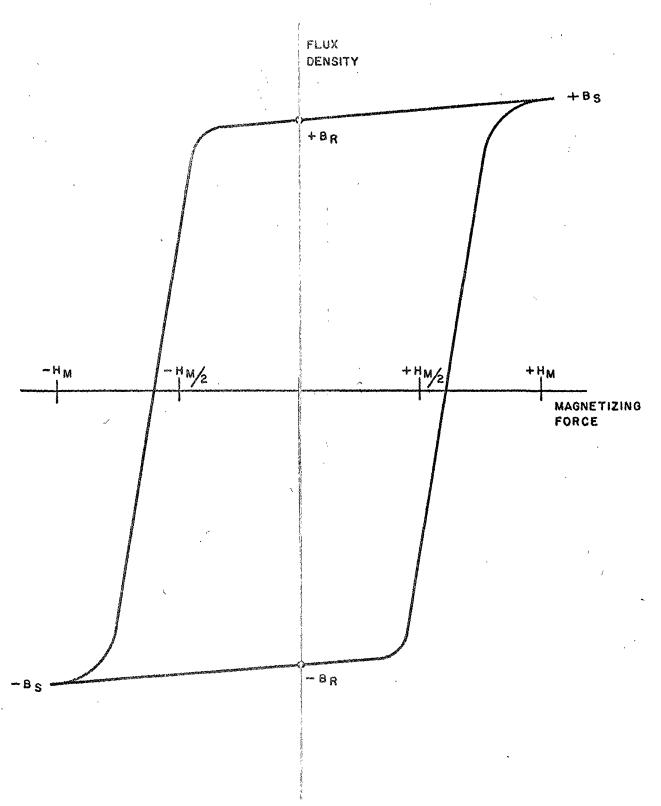
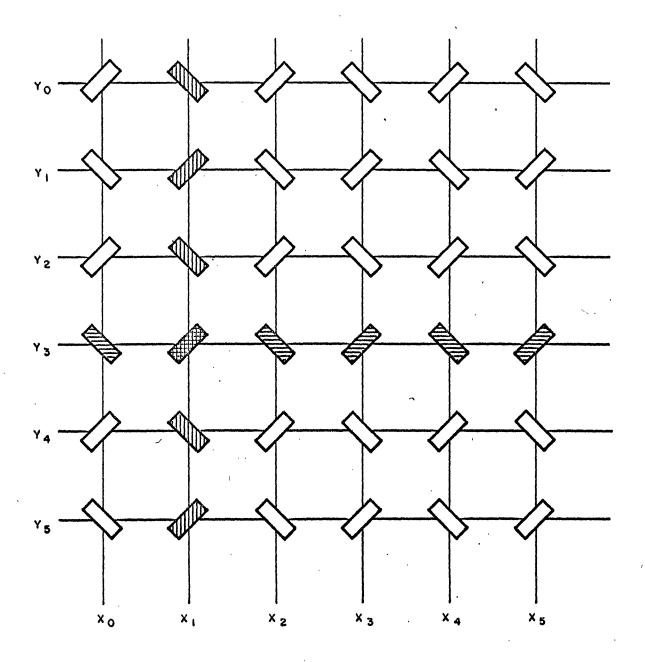


Figure 4-1 Rectangular B-H Loop



SELECTED CORE

HALF SELECTED CORES

UNSELECTED CORES

Figure 4-2 36 Bit Core Plane

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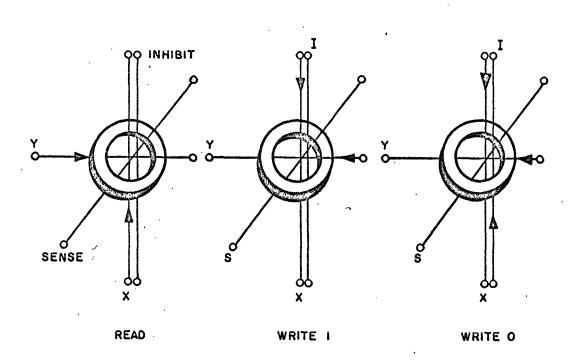


Figure 4-3 Current Direction for Various Functions

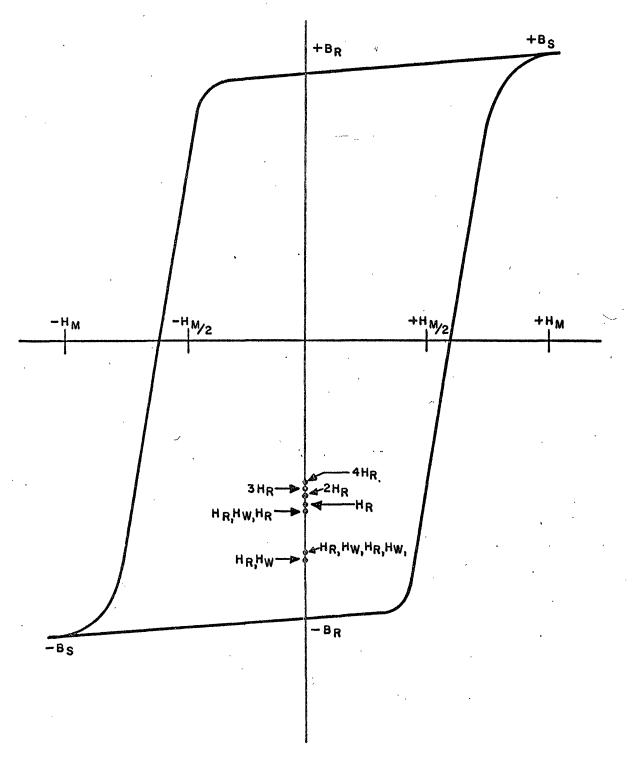


Figure 4-4 Half Selected Core Response

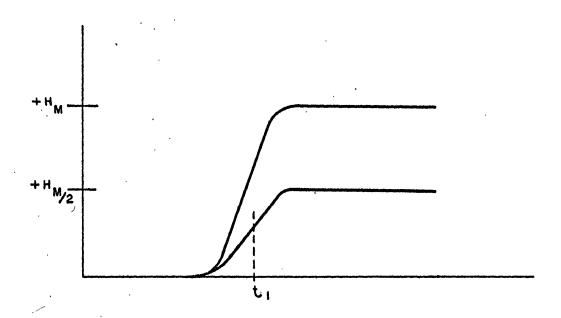


Figure 4-5 Current Rise Times in Driver Core

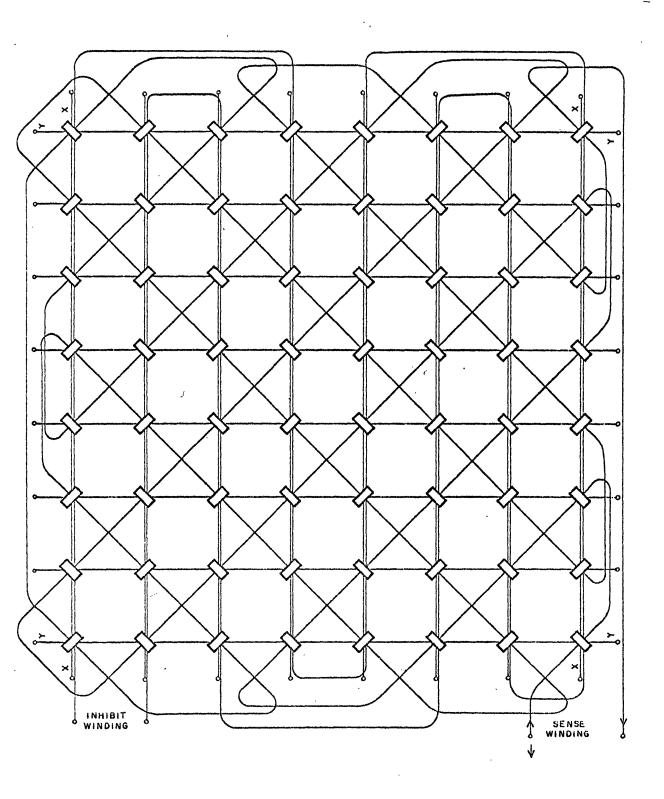


Figure 4-6 8 x 8 Core Plane Wiring Schematic

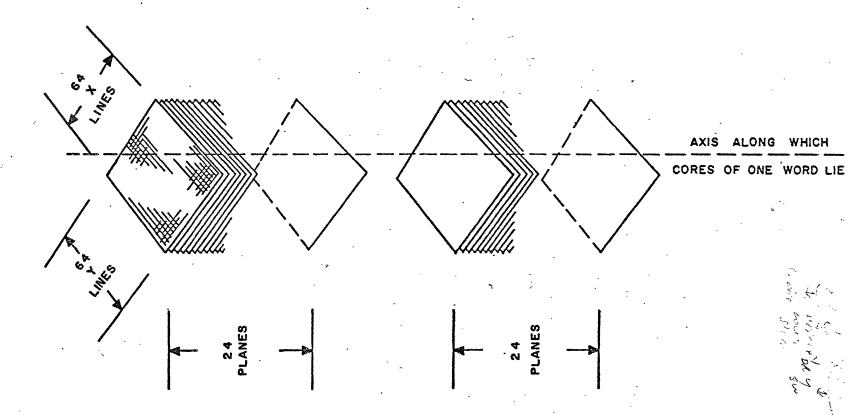


Figure 4-7 Memory Core Stack

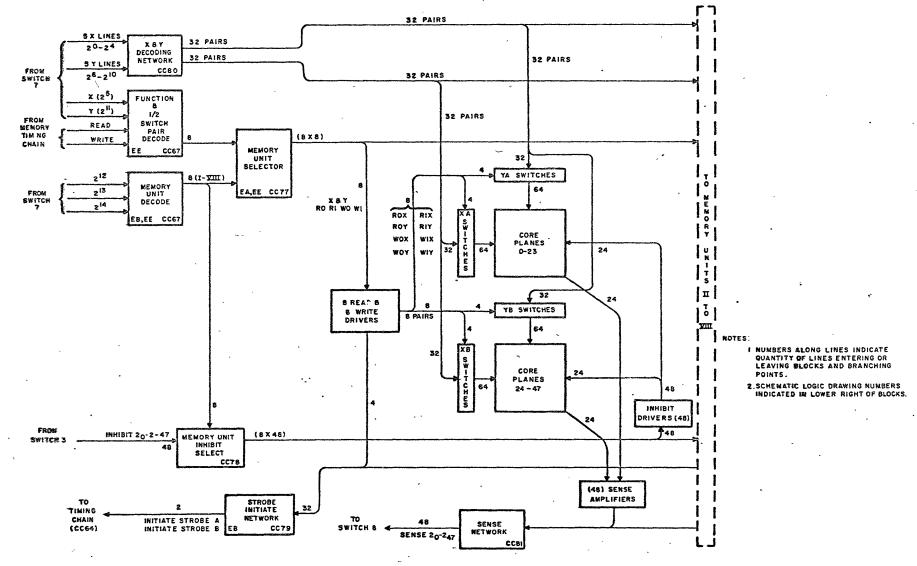
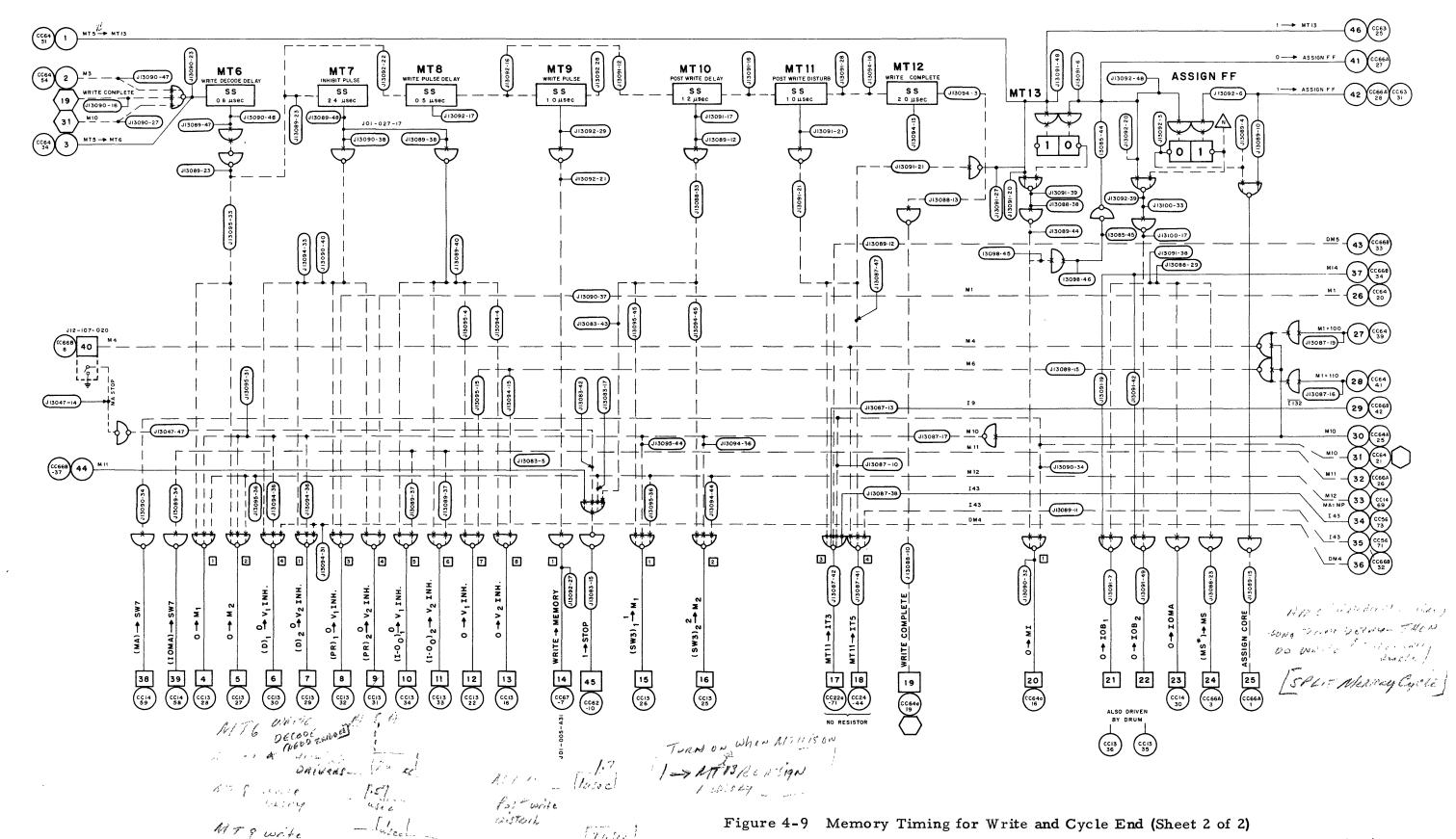


Figure 4-8 Block Diagram - Memory Signal Routing



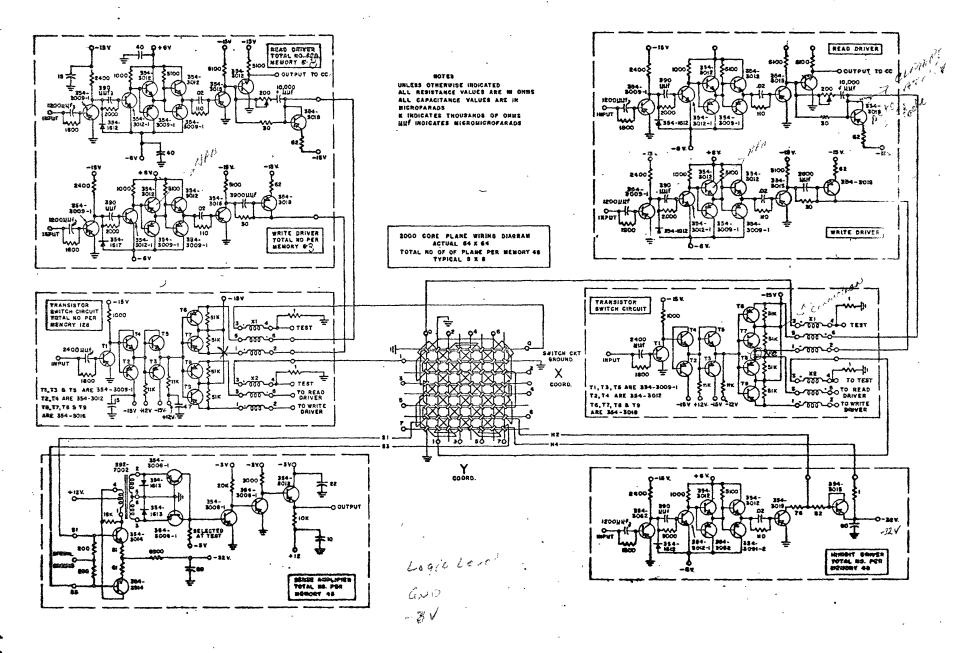


Figure 4-10 PHILCO 2000 Memory Circuits

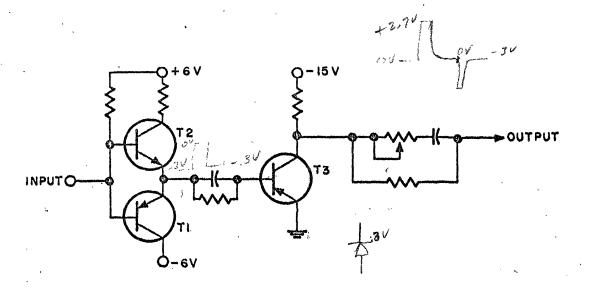


Figure 4-11 Complementary Symmetry Circuit