PEC application notes

Models 7x20, 6x60, 7x40, AND 6x40 NRZI Tape Transports

FOREWORD

This document is intended to supplement the PEC Product Specifications for Models 7X20, 6X60, 7X40, and 6X40 Tape Transports. It supplies additional technical information and suggests techniques by which the transports may be integrated into the user's equipment. Note that the recommendations contained herein, particularly regarding the IBG length and timing, are aimed at providing maximum system flexibility.

PEC

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I. GENERAL

All tape transport models referenced in this document are manufactured by PERIPHERAL EQUIPMENT CORPORATION, 9600 Irondale Avenue, Chatsworth, California.

These transports conform to the NRZI format established by the American National Standards Institute (ANSI) and are IBM compatible. They are designed for applications in data acquisition or computer systems where the connection of one or more transports is required at minimum cost.

Two different head configurations are available on PEC transports. The transports utilizing single-stack heads are Read/Write units; dual-stack versions provide simultaneous Read After Write capability. The available models are listed in Table 1.

The design of the interface electronics is a feature of these transports. Up to four independently addressable transports can be attached to a system by a simple "daisy-chain" connection to a common interface. This facilitates the expansion of an existing system and, at the same time, reduces cabling to a minimum. Transports which are to be "daisy-chained" should be fitted with a PEC Multiple Transport Adapter (MTA) to facilitate cabling.

Table 1
Models Available

Model	Head	Format	Reel Size (Inches)	Density (cpi)	Standard Speeds (ips)	Data Transfer Rate (KHz Maximum)
7820-9	Single	9 Track	7	800	6.25, 12.5	10.0
7820-75	Single	7 Track	7	800/556	6.25, 12.5	10.0/6.95
7820-72	Single	7 Track	7	800/200	6.25, 12.5	10.0/2.5
7520-72	Single	7 Track	7	556/200	6.25, 12.5	6.95/2.5
7840-9	Dual	9 Track	7	800	12.5	10.0
7840-75	Dual	7 Track	7	800/556	12.5	10.0/6.95
7840-72	Dual	7 Track	7	800/200	12.5	10.0/2.5
7540-72	Dual	7 Track	7	556/200	12.5	6.95/2.5
6860-9	Single	9 Track	10-1/2	800	12.5, 18.75, 25, 37.5, 45, 75	60.0
6860-75	Single	7 Track	10-1/2	800/556	12.5, 18.75, 25, 37.5, 45, 75	60.0/41.6
6860-72	Single	7 Track	10-1/2	800/200	12.5, 18.75, 25, 37.5, 45, 75	60.0/15.0
6560-72	Single	7 Track	10-1/2	556/200	12.5, 18.75, 25, 37.5, 45, 75	41.6/15.0
6840-9	Dual	9 Track	10-1/2	800	12.5, 18.75, 25, 37.5, 45, 75	60.0
6840-75	Dual	7 Track	10-1/2	800/556	12.5, 18.75, 25, 37.5, 45, 75	60.0/41.6
6840-72	Dual	7 Track	10-1/2	800/200	12.5, 18.75, 25, 37.5, 45, 75	60.0/15.0
6540-72	Dual	7 Track	10-1/2	556/200	12.5, 18.75, 25, 37.5, 45, 75	41.6/15.0

1-1. TAPE FORMATS

Details of the 9- and 7-track formats are shown in Figures 1, 2, and 3 for information and clarification.

The 9-track NRZI format differs from the 7-track format in several respects. In the 9-track format a Cyclic Redundancy Check Character (CRCC) is included in order to obtain track-in-error information for subsequent error correction. In 7-track formats even parity is employed when writing BCD and odd parity is used when writing Binary. The 7-track File Mark will always have even parity. Therefore, when reading binary and parity checking, the File Mark characters will be incorrect parity.

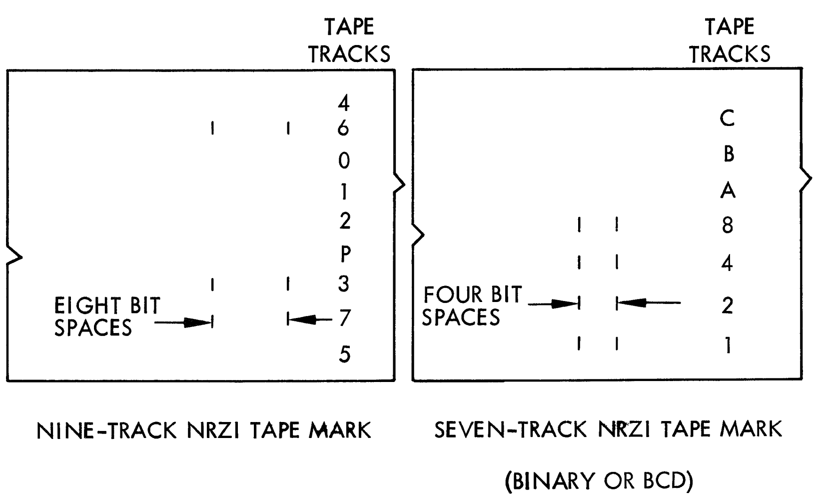
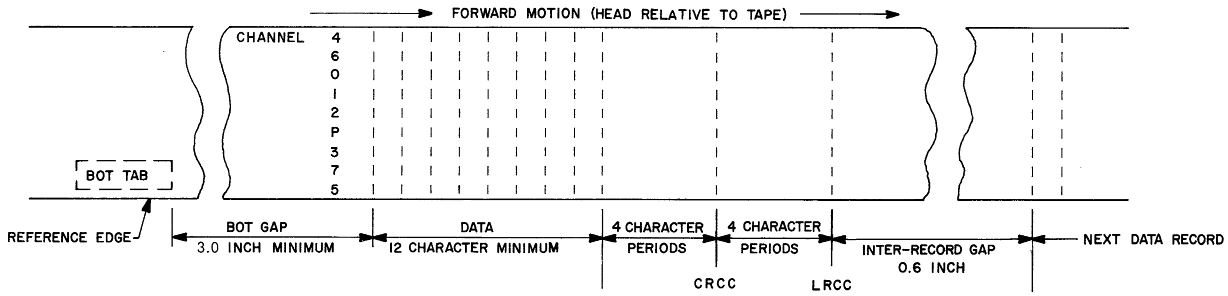


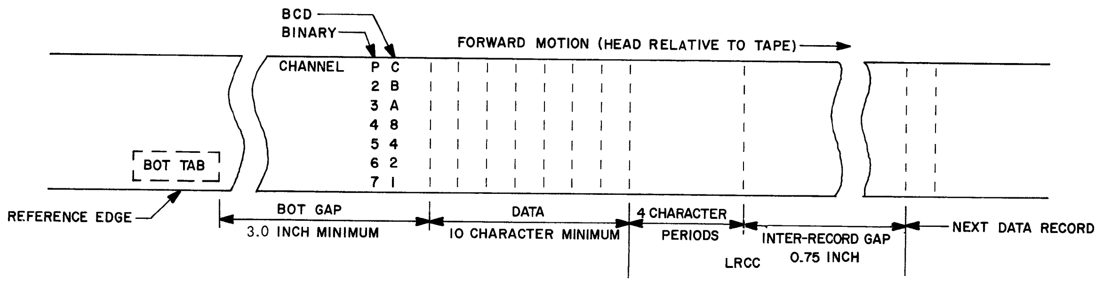
Figure 1. NRZI File Marks



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

Figure 2. 9-Track Format



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.75 INCH) FROM THE FOLLOWING RECORD.
6. DATA PACKING DENSITY MAY BE 200, 556, OR 800 BITS PER INCH.

Figure 3. 7-Track Format

II. SYSTEM CONFIGURATION

2-1. SINGLE TRANSPORT CONFIGURATION

A single transport connected to a controller will normally be all that is required. The cable length between the transport and the controller must not exceed 20 feet*. Only one select line is utilized and line termination resistors are provided in the transport for all interface lines.

2-2. MULTIPLE TRANSPORT CONFIGURATION

Up to four tape transports may be connected to a system provided the total cable length does not exceed 20 feet*. When this configuration is required, the PEC Multiple Transport Adapter (MTA) should be used.

Line terminating resistors are required at the controller for all incoming signals and at the furthest removed transport for all outgoing signals.

A typical multiple transport installation is shown in Figure 4.

It is possible for the controller to execute any command on any transport and in any sequence provided the selected transport is On Line and Ready.

Execution of an Off Line Command (OFFC) will reset the On Line flip-flop in the selected transport. This transport will not respond to further external commands until it is manually placed On Line again by the operator.

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*When using PEC's Multiple Transport Adapter with ribbon cable, the cable length is limited to a maximum of 40 feet.

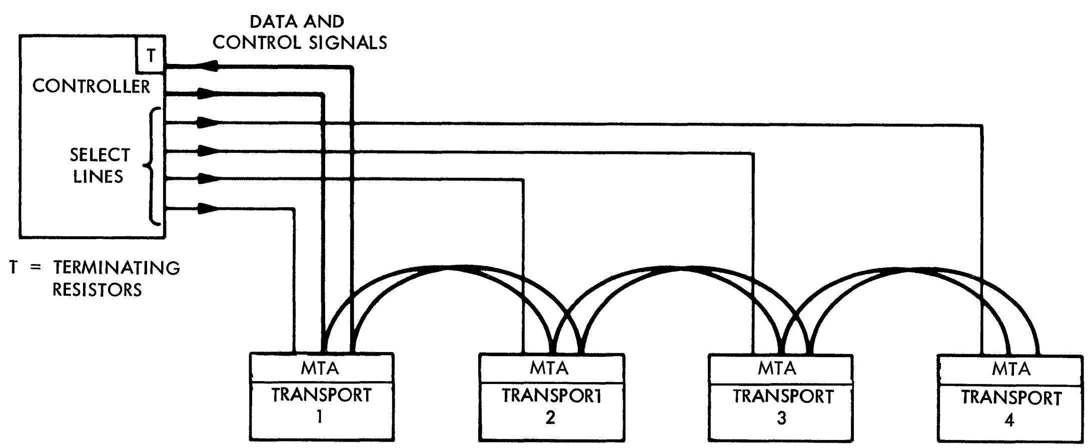


Figure 4. Daisy-Chain Connection

2-3. TRANSPORT STATUS

The status of a transport can be inspected by enabling the appropriate SELECT line and monitoring the various status signals which are summarized as follows.

ON LINE	Transport under remote control
RDY	Transport ready to accept remote commands
RWD	Rewinding
EOT	End of Tape
LDP	Load Point (BOT)
FPT	File Protect (no Write Enable ring on file reel)

2-4. TRANSPORT CONTROL LINES

The transport can be controlled by enabling the appropriate select line and applying the relevant control signals.

RTH1	Selects threshold level 1.
RTH2	Selects threshold level 2.
OVW	Overwrite provides slow turn-on and turn-off of write current and is used in conjunction with SWS to edit selected data blocks.
SFC	Synchronous Forward Command moves tape in the forward direction.
SRC	Synchronous Reverse Command moves tape in the reverse direction.
RWC	Rewind Command.
SWS	Set Write Status. Selects the Write or Read mode of operation.
OFC	Off Line Command. Selects the local mode of operation.
SLT	Electrically connects the transport to the controller.

2-5. MULTIPLE TRANSPORT ADAPTER (MTA)

The Multiple Transport Adapter (MTA) facilitates the connecting of up to four transports to a single controller. The MTA consists of two basic parts: an MTA/Cable Assembly and an MTA Terminator Assembly. The MTA/Cable Assembly mounts onto a transport and facilitates cabling to the next transport. The last transport in the line is mounted with an MTA/Terminator Assembly.

The MTA has the capabilities of providing status information to the controller/formatter interface for proper format selection in the control unit. The status provided are as follow: transport type (NRZ or PE), head type (single or dual), and speed (high or low). The MTA also provides the capability for local or remote transport identification. For more detailed information on the MTA refer to PEC Application Note No. 71717.

2-6. TRANSPORT MOTION CONTROL

The position of the magnetic head relative to data when the tape comes to rest in the Inter-Record Gap (IRG) is determined by the tape stop/start times and distances together with the pre-record and post-record delays built into the customer's controller.

Pre-record and post-record delays for tape speeds from 6.25 to 75 ips are summarized in Table 2 for Models 7X20, 7X40, 6X60, and 6X40.

With PEC Models 7X40 and 6X40 (dual-stack head), the controller should be designed to perform a simultaneous read-after-write data check. Under these circumstances, the termination of a Write command is not initiated when the last character is written, but by detection of a gap at the end of the record by the read logic. A Write Normal post-record delay, according to Table 2, is then given before tape motion is stopped. In single-stack head transports this delay

Table 2

Pre-Record and Post-Record Delays at 25 ips*

Function	Pre-Record Delays (milliseconds)		Post-Record Delays (milliseconds)	
	9 Track	7 Track	9 Track	7 Track
1. Write From BOT	226	226	3	3
2. Write Normal				
Single Stack	23	28	3	3
Dual Stack	17	22	3	3
3. Write File Mark	150	150	3	3
4. Read From BOT	60	60	0	0
5. Read Forward (Normal)	12	12	0	0
6. Read Reverse (Normal)	12	12	3	8
7. Read Reverse (Edit)	12	12	8	13
8. Start/Stop Time	15	15	15	15

* To calculate delays for other tape speeds, scale inversely to tape speed; i.e.,

$$\text{Write From BOT at 75 ips} = \frac{25}{75} \times 226 = 75.5$$

ensures that the tape comes to rest further into the IRG than it would after a read operation. This prevents the possibility of unerased gap areas in a Write, Read Reverse, Read Forward, Write sequence of commands. The IRG generated from a Write-Write sequence of commands can be calculated as shown in Table 3.

For a Read-Write sequence of commands, the IRG will be 0.075 inch shorter. A command that involves a change of tape direction or a change in Read/Write status should not be given until tape motion has ceased.

When a write error occurs, it is necessary to backspace over the erroneous record and rewrite. For each iteration, the new record will be written approximately 0.125 inch further down the tape which results in a longer IRG. This movement is determined by the controller timing shown in Table 2. These times are chosen to prevent

Table 3
IRG Calculations

Description	9 Track (Inches)	7 Track (Inches)
1. 3 msec post-record delay at 25 ips	0.075	0.075
2. Stop distance	0.190	0.190
3. Start distance	0.190	0.190
4. Remainder of pre-record delay at 25 ips	0.200	0.325
Total	0.655	0.780

inadvertent backing into the previous record. Also, if a write error were caused by a bad spot on the tape, the new record would move off this spot.

The delays listed in Table 2 are usually implemented in the form of individual one-shot elements or are dealt with collectively using counter-techniques. One-shots are generally more expensive but offer greater flexibility for last-minute changes to the delay periods.

The counter-technique is entirely digital and has the added advantage that the same logic can be used with tape transports having different tape speeds by simply changing the clock frequency. Such a scheme is illustrated in Figure 5.

The sequence is initiated by a START pulse when SFC or SRC goes true. This sets F1 or F2 depending on whether or not the tape is at BOT. The 9-stage counter is now activated. When a count is reached corresponding to the pre-record delay for the particular command in progress, one of the gates (G1 through G5) is operated and both the flip-flop and counter are reset. A pulse is generated on BEGIN DATA which is used by the controller logic to initiate the transfer of data to or from tape.

On completion of the transfer, an END DATA pulse from the controller sets F3. The appropriate post-record delay is now generated in a manner similar to that previously described using gates G6 through G8.

Finally, the STOP pulse resets SFC or SRC, which stops tape motion and terminates the command.

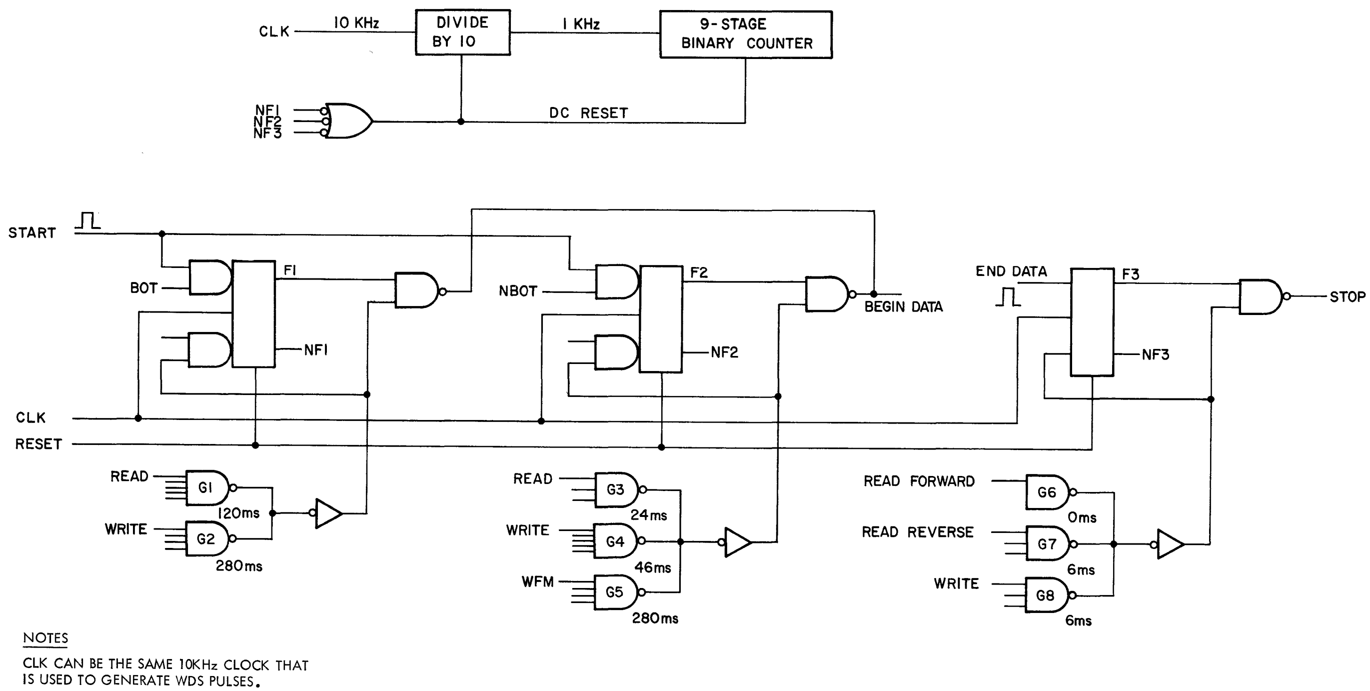


Figure 5. Delay Generation — Counter Method (at 12.5 ips)

2-7. COMMAND SEPARATION

The Models 7X20, 6X60, 7X40, and 6X40 Tape Transports have no inherent program restriction. However, for correct system operation, the customer should ensure that tape motion has ceased before attempting to:

(1) Change tape direction. This preserves the integrity of transport stop/start times and distances for the user's read and write logic.

(2) Change Read/Write status. This prevents the possibility of unerased areas of tape being left in the IBG.

One method of achieving this is simply to separate all commands by at least the transport stop time. This should be adequate for the majority of the transport applications.

Alternatively, if maximum performance is required, additional logic can be added to detect the two conditions previously described. A new command, provided it is of the same type and direction as the previous one, is then allowed to commence immediately even though the transport may still be decelerating from the previous command. This is made possible by the transport's linear acceleration and deceleration ramps which are such that all timing described in Table 2 remains valid. The net result is a time saving of up to one start/stop time (30 milliseconds at 12.5 ips) per command.

The only resultant side effect is that the IRG generated during Write commands may be slightly longer than normal. This difference has a maximum value of 0.095 inch and can usually be neglected in the interest of overall system performance. It is plotted in Figure 6 as a function of the command separation.

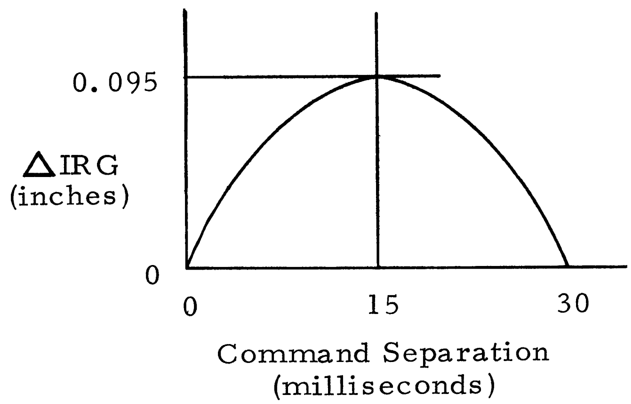


Figure 6. ΔIRG as a Function of the Command Separation at 12.5 ips

2-8. CIRCUIT CONFIGURATION

The interface circuit configuration is illustrated in Figure 7. This design is based on the limited temperature range (0 to 75°C) of DTL 930 Series integrated circuits. DTL 944, 932, or TTL 7416 power gates are used as transmitters and DTL 936 inverters, DTL 946 dual input gates or TTL 74XX are used as receivers.

All signal inputs should be included in one harness and all outputs in a second harness. The two harnesses can be run in close proximity. The maximum transmission distance is 20 feet. The signals are transmitted by individual twisted pairs to reduce crosstalk.

The circuits are designed so that either a disconnected wire or removal of power at the transmitter results in a false signal being interpreted at the receiver end of the harness. The minimum recommended pulse width is 1 μsecond.

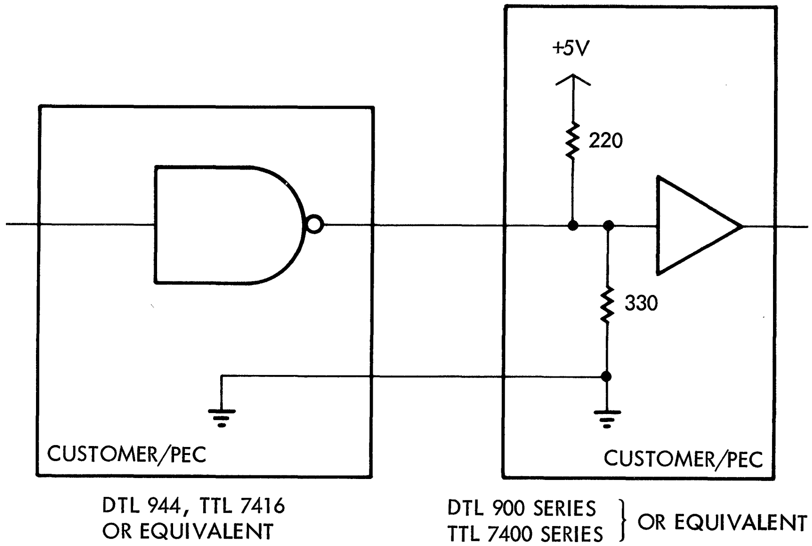


Figure 7. Interface Circuit

The twisted pairs should have the following characteristics.

(1) Maximum length of 20 feet.*

(2) Not less than 1 twist per inch.

(3) 22- or 24-gauge conductors with minimum insulation thickness of 0.01 inch.

It is important that the ground side of each twisted pair be grounded within 6 inches of the interface circuit to which it is connected.

The following figures give the noise margin remaining after accounting for worst-case crosstalk.

	0^oC	25^oC	50^oC
Low Level (millivolts)	450	250	200
High Level (millivolts)	300	450	550

*When using PEC's Multiple Transport Adapter with ribbon cable, the cable length is limited to a maximum of 40 feet.

III. WRITE OPERATION

A write operation is one in which tape motion takes place with write current flowing in the read/write heads. Writing normally occurs in the forward direction for commands such as Write Record, Write File Mark, or Erase. However, it is also possible to write in the reverse direction (e.g., reverse Erase), but this is not a recommended procedure.

An interface line, Set Write Status (SWS), under the control of the customer, specifies whether a read or a write command is required. Shortly after a forward or reverse command (Synchronous Forward (SFC) or Synchronous Reverse (SRC)) is given at the beginning of each data transfer, the condition of SWS is sampled and stored in a control flip-flop (WRT) in the transport logic. If a write command is required, WRT is set true and turns on write current in the heads. For read commands, WRT is set false, turning off the write current.

WRT retains the present read/write status until it is overwritten at the beginning of the next command, or it is forcibly reset to the false state by one of the following.

(1) A Rewind command (RWC).

(2) Switching to the off-line mode, either by an Off Line command (OFFC) or by pressing the ON LINE control.

(3) Loss of interlock.

A command that involves a change of read/write status should not be given until tape motion has ceased.

3-1. WRITE FORWARD

The following sequence of events will take place when writing a record in the NRZI format using either a single-stack head (Models 7X20 and 6X60) or a dual-stack head (Models 7X40 and 6X40) and one of the standard tape speeds. Typical waveforms are illustrated in Figure 8.

(1) Wait for tape motion to cease. Set SWS true.

(2) Set SFC true, starting tape motion. The WRT flip-flop will set true shortly afterward.

(3) Generate a pre-record delay as specified in Table 2 according to speed.

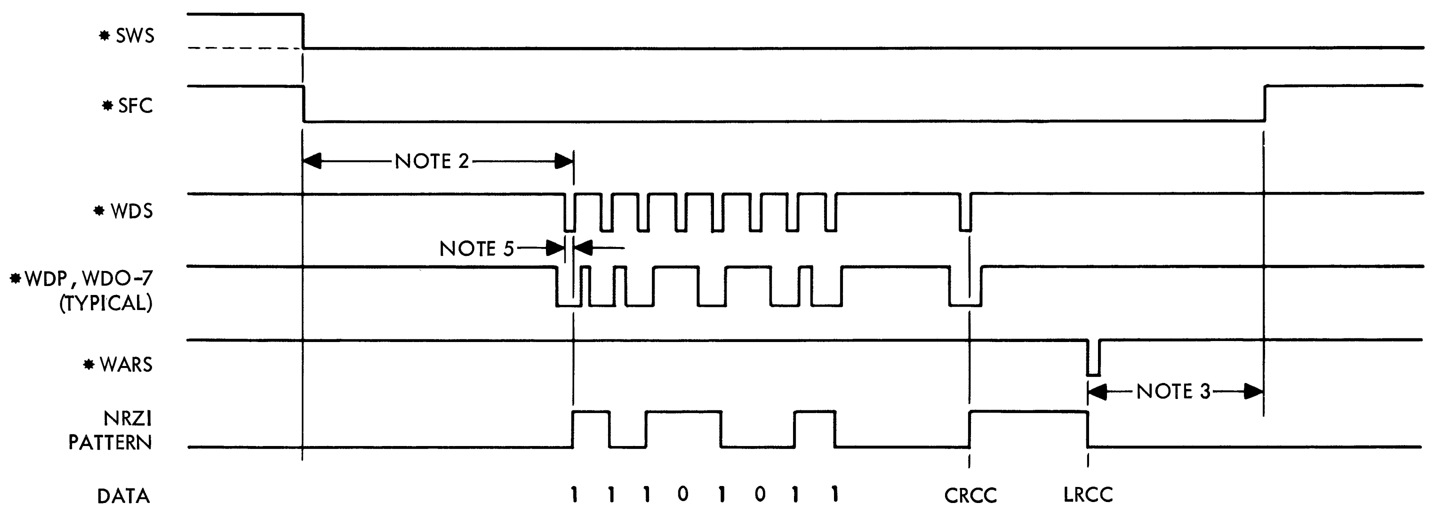
(4) Generate WDS pulses together with appropriate data on WDP, WD0-7 (9-track), WD2-7 (7-track) for each data character to be written onto the tape. This frequency is equal to density multiplied by speed. The tolerance is ±0.25 percent.

NOTE

For a Write File Mark command, a single character is written. For 9-track formats, a "1" bit is written in Channels 3, 6, and 7. In 7-track formats, a "1" bit is written in Channels 4, 5, 6, and 7.

(5) 9-track only: Leave a 3-character gap, then generate an extra WDS pulse together with CRCC data on WDP, WD0-7. (CRCC is suppressed for Write File Mark.)

(6) Leave a 3-character gap, then generate a pulse on WARS. The leading edge of this pulse resets the write register in the transport, thus writing the LRCC onto the tape.



NOTES

1. CUSTOMER GENERATES THE WAVEFORMS MARKED.*
2. PRE-RECORD DELAY SHOULD BE SET IN ACCORDANCE WITH TABLE 2.
3. POST-RECORD DELAY SHOULD BE SET IN ACCORDANCE WITH TABLE 2.
4. THE COMBINED PRE- AND POST-RECORD DELAYS DEFINE THE INTER-RECORD GAP.
5. WDS HAS A MINIMUM PULSE WIDTH OF 1 μSECOND. WRITE DATA LINES WDP, WDO-7 MUST BE STEADY DURING, AND FOR 0.5 μSECOND EITHER SIDE OF WDS.
6. THE SWS LINE IS SET TRUE FOR WRITE COMMANDS ONLY. THIS WAVEFORM IS SAMPLED BY THE TRANSPORT LOGIC AT THE BEGINNING OF EACH DATA TRANSFER, AND MUST BE HELD STEADY FOR AT LEAST 20 μSECONDS AFTER THE LEADING EDGE OF SFC (OR SRC).
7. INTERFACE WAVEFORMS ARE SHOWN LOW-TRUE, AS THEY APPEAR ON THE INTERFACE CABLE.

Figure 8. Write Waveforms

(7) Generate a post-record delay as specified in Table 2 according to speed. This delay ensures that the tape comes to rest further into the IRG than it would after a read operation. This prevents the possibility of unerased gap areas in a Write, Read Reverse, Read Forward, Write sequence of commands.

(8) Set SFC false. The tape decelerates and comes to rest as specified in Table 2 according to speed.

(9) WRT remains set and will continuously erase tape until some subsequent Read, Rewind, or Off Line command is given (or the interlock is broken).

3-2. OVERWRITE (EDIT)

The Overwrite (Edit) function is normally employed when it is desired to change a record located among other records. To successfully overwrite a given record, the tape must first be positioned at the same place from which the original record was written. After writing the new record, the write current must be turned off while the tape is in motion. This is done to eliminate the inherent noise transient associated with a collapsing magnetic field. The provision for current turn-off while the transport is in motion is provided by the Overwrite (OVW) interface line.

The following procedure should be followed when overwriting a record utilizing either a single-stack head transport (Models 7X20 and 6X60) or a dual-stack head transport (Models 7X40 and 6X40) and one of the standard tape speeds. This procedure applies only to those transports which have the Overwrite interface line. For a more detailed explanation of the Overwrite function, refer to Edit Application Note, PEC Document No. 70711.

(1) Locate the record to be changed.

(2) Wait for the tape motion to cease, then set SWS false.

(3) To read the record in reverse set SRC true. Tape motion will start and the transport will be in read mode.

(4) Generate a post-record delay for Read Reverse (Edit) as specified in Table 2 (item 7). This delay ensures that the tape comes to rest nominally at the same place from which the original record was written.

(5) Wait for the tape motion to cease, then set SWS true.

(6) Set Overwrite (OVW) true.

(7) Set SFC true, starting tape motion. The transport will be in the write mode.

(8) Generate a pre-record delay for Write Normal as specified in Table 2 (item 2) according to speed.

(9) Generate WDS pulses together with appropriate data on WDP, WD0-7 for each data character to be written onto the tape. This frequency is equal to density multiplied by speed. The tolerance is ±0.25 percent.

NOTE

The new record length must be the same length as the original record in order to maintain the integrity of the inter-record gap.

(10) On 9-track systems, leave a 3-character gap and write the CRCC in the fourth character slot.

(11) Leave a 3-character gap, then generate a pulse on WARS. The leading edge resets the write register in the transport, thus writing the LRCC onto the tape in the fourth character slot after the last character is written.

(12) Generate a post-record delay as specified in Table 2 according to speed.

(13) Subsequent operation can now be performed as desired.

3-3. VERTICAL PARITY GENERATION

The vertical parity bit (VRC) recorded in Channel P on 9-track systems is generated so that the total number of "1" bits in each data character (not the CRCC or LRCC) is always odd. On 7-track systems, even parity is used when writing BCD.

3-4. CRC GENERATION (9-TRACK SYSTEMS ONLY)

The CRCC is based on a modified cyclic code and provides a more rigorous method of error detection than using the VRC or LRC checks only. When reading, it can also be used in conjunction with the VRC and LRCC checks for error correction, provided that the errors are confined to a single channel. For a more detailed description of CRCC refer to PEC Application Note, Document No. 70701.

The CRCC can be generated according to the following rules:

(1) Each data character is added to the contents of a CRC register (CRCR) without carry - each bit being exclusively ORed to the corresponding bit of the CRCR.

(2) This information then undergoes a circular shift right of one place, such that each bit is copied into the adjacent CRCR flip-flop:

(CRCP → CRC0, etc.)

(3) If the bit entering CRCP is a "1", the bits entering CRC2, CRC3, CRC4, and CRC5 are inverted.

(4) Steps (1), (2), and (3) are repeated for each data character of the record.

(5) The contents of all CRCR positions, except CRC2 and CRC4, are inverted and the resultant character is written onto the tape.

Figure 9 shows a block diagram of a CRCR. Note that this circuit requires one clock pulse for each data character, and that no extra shift is required after the last data character.

If it is required to regenerate the CRCC during a Read Reverse command, the significance of the data bits entering the CRCR must also be reversed.

The CRCC has the following properties.

(1) It can be an all-zeroes character.

(2) Its value is such that the LRCC always has odd parity (therefore the LRCC can never be all-zeroes).

(3) It has odd parity if there are an even number of data characters, or even parity for an odd number of data characters.

For compatibility reasons, the correct CRCC should always be written onto tape even though it is intended not to make use of it for read checking.

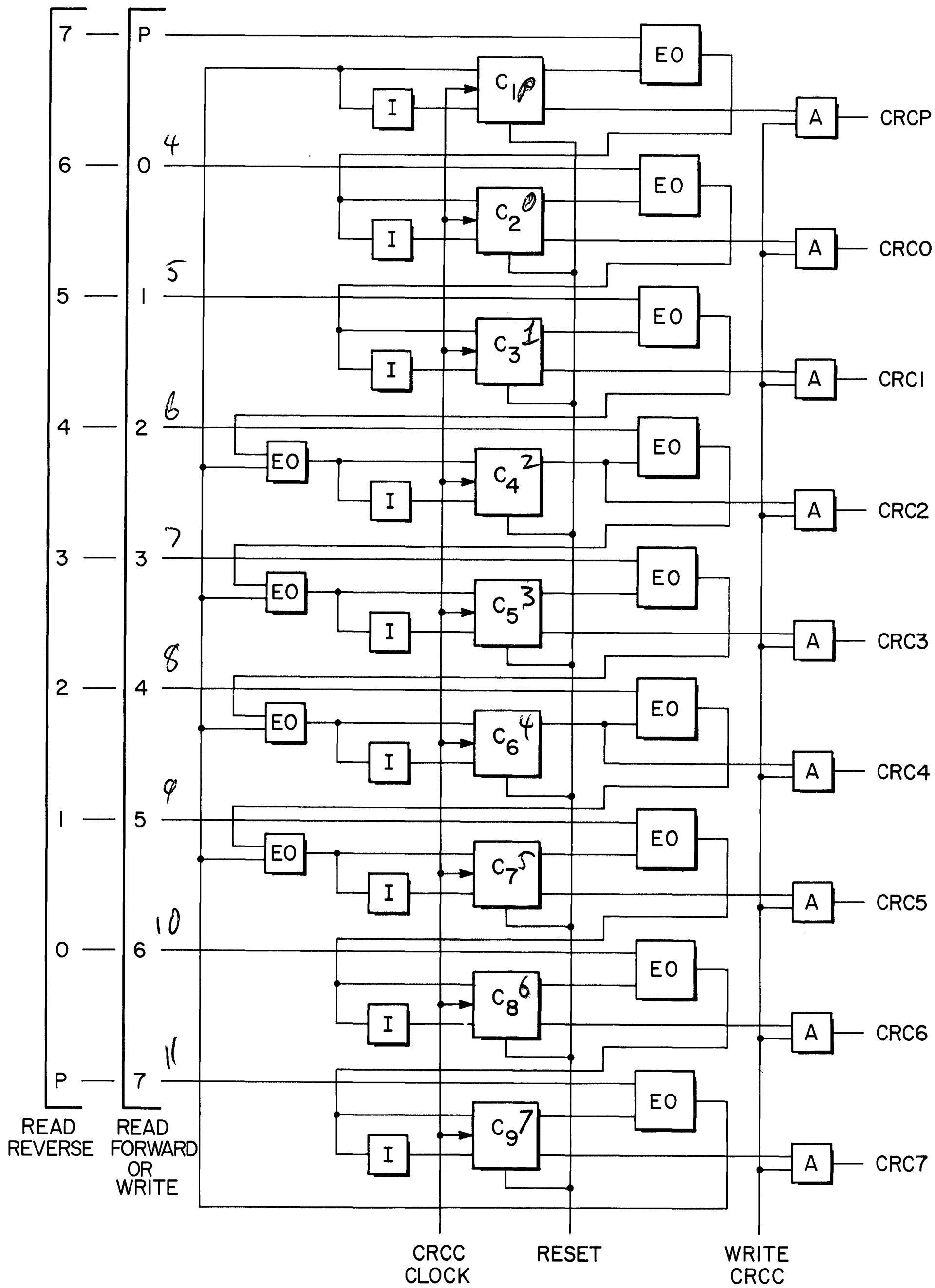


Figure 9. Cyclic Redundancy Check Register

3-5. ERASING

Erasing is required only when it is necessary to abandon a specific area of tape after repeated write errors. This can be accomplished by using any one of the following methods.

(1) Backspace over the erroneous record and rewrite. For each iteration, the new record will be written approximately 0.125 inch further down the tape, leaving a longer IRG behind it.

(2) Backspace over the erroneous record, write file mark, backspace, then rewrite. This will leave an erased gap of about 4 inches.

(3) Erased gaps of any length can be generated by executing a dummy write command with the WDS line suppressed.

IV. READ OPERATION

The transport must be on line and ready before a read operation can take place. When it is desired to perform only a read operation, removal of the Write Enable ring ensures that the tape is not inadvertently erased.

4-1. READ THRESHOLDS

Different read thresholds are employed to ensure that no write errors have occurred during a previous write operation. For Models 7X20 and 6X60 (single-stack heads) interface line RTH1 under the customer's control is used to select the proper threshold. For Models 7X40 and 6X40 (dual-stack heads) the threshold selection is an automatic function of the write/read status flip-flop (WRT). On all systems, the capability of an extra low read threshold for data recovery is provided through the interface line RTH2.

The high threshold level is used to ensure that when data is written on tape, it is above 50 percent of the nominal amplitude. On subsequent read operations, the threshold or clip level is reduced to 20 percent of nominal amplitude to ensure data recovery. The extra low threshold for data recovery selects 10 percent of the nominal amplitude as the read level. The RTH interface line(s) must be held steady for the duration of each record.

Following is a list of settings for these threshold levels.

(1) Models 7X20 and 6X60 Only.

(a) RTH1 False: Low threshold. This threshold level is normally selected.

(b) RTH1 True: High threshold. This threshold level is selected only when verifying a record that has just been written.

(2) Models 7X20, 6X60, 7X40, and 6X40*

(a) RTH2 False: Low threshold. This threshold level is normally selected for Read-After-Write data checks or for normal read operations.

(b) RTH2 True: Extra low threshold. This threshold level is selected only when it is required to recover very low amplitude data. On models where RTH1 is also employed, RTH1 must be false to select this extra low threshold.

*This function is not currently available on these transports.

4-2. READ DATA

Although the individual bits of each data character are recorded simultaneously, they are read back from tape over a finite band of time. This skewing effect is caused by small static or dynamic misalignments of the tape path and by the effects of bit crowding.

In PEC transports, the static skew has been reduced to such a degree that individual deskew logic and adjustments for each track becomes unnecessary.

The transport read electronics first amplifies, then peak detects the read data from each track. This information is then copied into a skew register which assembles the 9, or 7, bits of each character into parallel form (see Figure 10). The outputs from the skew register are transmitted to the user's equipment on interface lines RDP, RD0-7 (or RD2-7).

Another interface line, Read Data Strobe (RDS), is used to sample RDP, RD0-7 (or RD2-7). This waveform consists of a pulse for each character read from tape, and the trailing edge of each pulse should be used to sample the data lines.

4-3. READ FORWARD

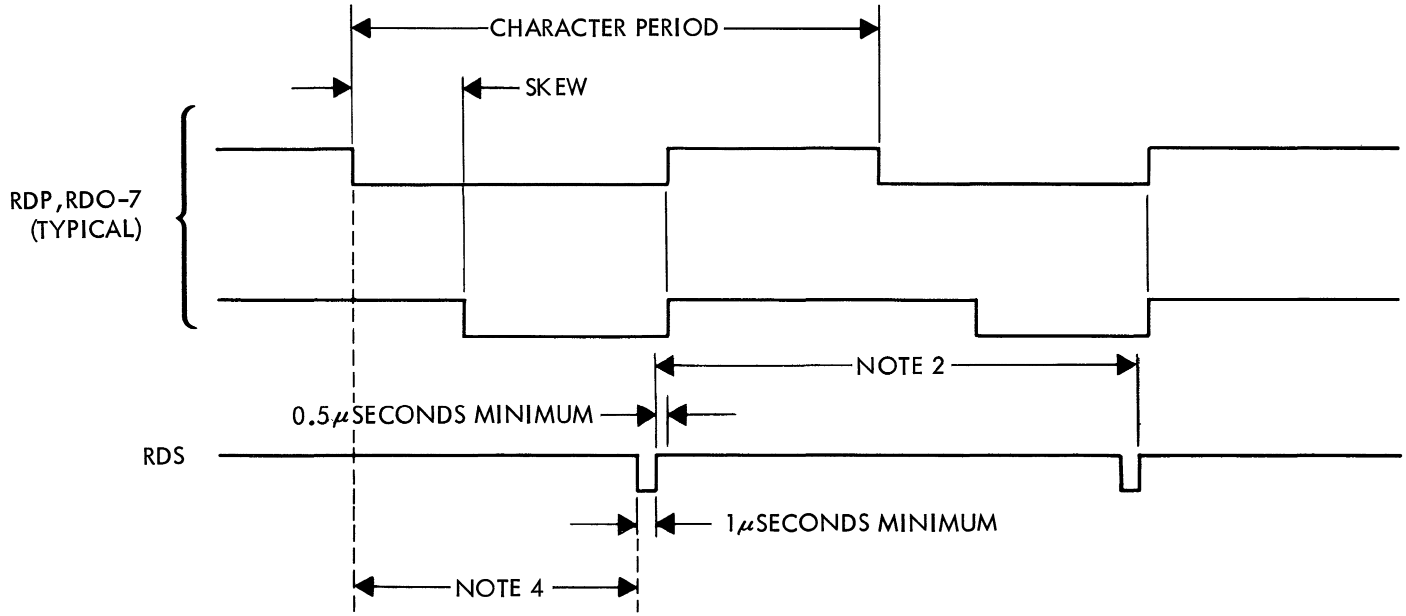
One of the simplest and safest ways of implementing the read control logic is to make use of two "missing pulse detector" circuits. The first circuit continually looks for the gap between the last data character and the CRCC or LRCC and has an optimum setting of 2-1/2 character periods. The second circuit searches for a 16-character gap at the end of the record. When this is found, the read circuits are disabled and a halt command is given to the transport. The second circuit ensures that (except for the most massive of drop-outs) the transport will always come to rest in a genuine IRG.

Typical read waveforms for such a scheme are shown in Figure 11. The sequence of events is as follows:

(1) Set SFC true.

(2) Generate a pre-record delay as specified in Table 2. according to speed which suppresses read data while the tape is accelerating and the IRG is being traversed.

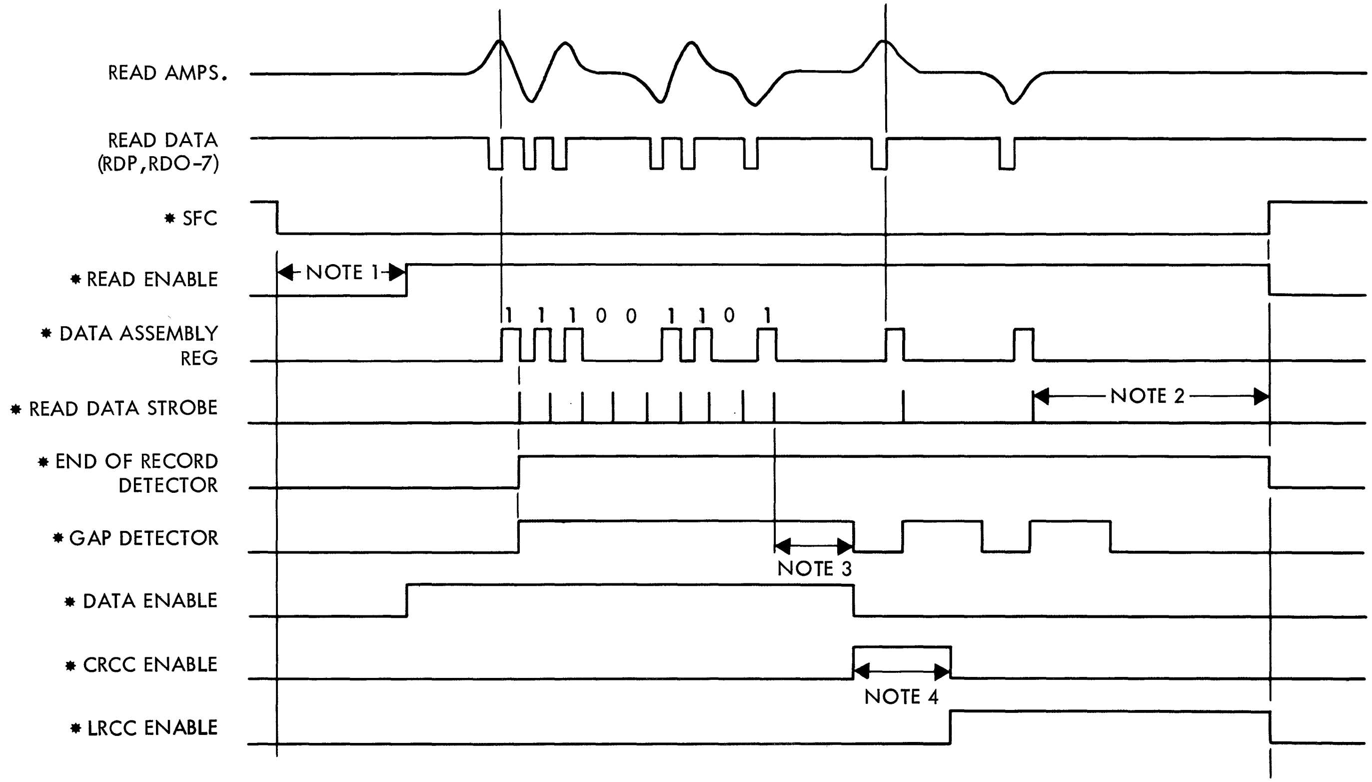
(3) Read data arrives and Read Data Strobes are generated. The first strobe pulse activates both the gap detector and the end of record detector.



NOTES

1. RDP, RD0-7 SHOULD BE SAMPLED ON THE TRAILING EDGE OF EACH RDS PULSE.
2. CHARACTER PERIOD AVERAGES $\frac{1}{BV}$, WHERE B=DENSITY AND V=TAPE VELOCITY. HOWEVER, THIS CAN VARY CONSIDERABLY DUE TO THE COMBINED EFFECTS OF BIT CROWDING AND SKEW.
3. THESE WAVEFORMS ARE SHOWN LOW-TRUE, AS THEY APPEAR ON THE INTERFACE CABLE.
4. RDS OCCURS NOMINALLY 46% OF CHARACTER PERIOD.

Figure 10. Read Data Waveforms



NOTES

1. THE PRE-RECORD DELAY SHOULD BE SET IN ACCORDANCE WITH TABLE 2. THIS GATES OUT UNWANTED READ DATA WHILE THE TRANSPORT IS ACCELERATING AND TRAVERSING THE IRG.
2. TAPE MOTION IS STOPPED AND THE READ CIRCUITS DISABLED WHEN A GAP OF 16 CHARACTER PERIODS IS DETECTED.
3. GAP DETECTOR DELAY IS 2-1/2 CHARACTER PERIODS.
4. THIS IS A FIXED DELAY OF 3 CHARACTER PERIODS. THE CRCC WILL OCCUR DURING THIS TIME.
5. CUSTOMER GENERATES THE WAVEFORMS MARKED.*
6. INTERFACE WAVEFORMS ARE SHOWN LOW-TRUE, AS THEY APPEAR ON THE INTERFACE CABLE.

Figure 11. Read Forward Waveforms

(4) Each character is processed in one or more of the following ways.

(a) Check for vertical parity error.

(b) Copy into the LRC check register.

(c) Copy into the CRC check register.

(d) Assemble into word or copy directly from memory.

(5) A gap of 2-1/2 character periods is detected. This triggers a delay of 3-character periods. Any character occurring during this time can be treated as a CRCC (9-track) and will be checked against the regenerated CRCC now held in the CRCR.

(6) All succeeding characters can be treated as a LRCC and will be checked against the contents of the LRC check register.

(7) A 16-character gap is detected. This disables the read logic and sets SFC false, stopping tape motion.

4-4. READ REVERSE

This can be implemented in a manner similar to read forward, except that special provision must be made because the LRCC and CRCC occur first. In addition, the significance of data bits entering the CRCR for check purposes must be reversed (see Figure 9).

A post-record delay as specified in Table 2 according to speed is required between the detection of end of record and the stopping of tape motion (setting SRC false). This will bring the tape to rest in the optimum position in the IRG for subsequent read or write commands.

4-5. FILE MARK DETECTION

Since it is generally required to detect a File Mark in either the forward or reverse direction, no use can be made of the 3-1/2 inch gap that separates it from the previous record on the tape.

To qualify as a File Mark, a record should meet the following conditions:

(1) It must consist of a single data character with an identical LRCC.

(2) The data character has the required pattern (000010011 for 9-track, 0001111 for 7-track).

(3) There is no CRCC check character for 9-track.

V. SUMMARY

The information contained in this document is intended to provide sufficient information to aid in the design of a controller for NRZI encoding and decoding. PERIPHERAL EQUIPMENT CORPORATION manufactures a Formatter unit which accomplishes the tasks outlined in this document. The interfacing to the Formatter is greatly simplified and can easily be implemented into the user's system. For additional information on the Formatter unit refer to PEC Application Note No. 70712.

NOTES

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PEC

9600 IRONDALE AVENUE, CHATSWORTH, CALIFORNIA 91311, (213) 882-0030 TWX (910) 494-2093

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