MODELS T8640A AND T8660A SYNCHRONOUS WRITE SYNCHRONOUS READ TAPE TRANSPORTS

## MODELS T8640A AND T8660A SYNCHRONOUS WRITE SYNCHRONOUS READ TAPE TRANSPORTS

PERTEC DIVISION

## FOREWORD

This manual provides operating and service instructions for the Synchronous Write/ Synchronous Read Tape Transports, Models T8640A and T8660A, manufactured by the PERTEC DIVISION of PERTEC COMPUTER CORPORATION, Chatsworth, California.

The content includes a detailed description, specifications, installation instruction, and checkout of the transport. Also included are theory of operation and preventive maintenance instructions. Section VII contains photo parts lists and schematics.

All graphic symbols used in logic diagrams conform to the requirements of ANSI Y32.14 and all symbols used in schematic diagrams are as specified in ANSI Y32.2.

## SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PERTEC agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact PERTEC SERVICE - our trained service staff will be pleased to assist you.

## PERTEC SERVICE

North America:
California \& Canada - (213) 998-7676
All other - TOLL FREE (800) 423-5156
TWX (910) 494-2093
Europe:
10 Portman Road
Reading, Berkshire RG3 1DU
England
Phone Reading (734) 582-115
TWX (851) 847-101

## PROPRIETARY NOTICE

Information contained in this document is copyright by PERTEC Computer Corporation and may not be duplicated in full or in part by any person without prior written approval of PERTEC Computer Corporation. Its purpose is to provide the User with adequately detailed documentation so as to efficiently install, operate, maintain, and order spare parts for the equipment supplied. Every effort has been made to keep the information contained in this document current and accurate as of the date of publication or revision. However, no guarantee is given or implied that the document is error-free or that it is accurate with regard to any specification.

## TABLE OF CONTENTS

Page
SECTION I - GENERAL DESCRIPTION AND SPECIFICATIONS
1.1 Introduction ..... 1-1
1.2 Purpose of Equipment ..... 1-1
1.3 Physical Description of Equipment ..... 1-1
1.4 Functional Description ..... 1-2
1.5 Mechanical and Electrical Specifications ..... 1-5
1.5.1 Interface Specifications ..... 1-8
SECTION II - INSTALLATION AND INITIAL CHECKOUT
2.1 Introduction ..... 2-1
2.2 Uncrating the Transport ..... 2-1
2.3 Power Connections ..... 2-2
2.4 Initial Checkout Procedure ..... 2-2
2.5 Interface Connections ..... 2-5
2.6 Rack Mounting the Transport ..... 2-6
SECTION III — OPERATION
3.1 Introduction ..... 3-1
3.2 Cleaning the Head and Guides ..... 3-1
3.3 Loading Tape on the Transport ..... 3-1
3.3.1 Bringing Tape to Load Point (BOT) ..... 3-2
3.3.2 Unloading Tape ..... 3-3
3.4 Manual Controls ..... 3-3
3.4.1 ON/OFF ..... 3-3
3.4.2 LOAD ..... 3-4
3.4.3 ON LINE ..... 3-4
3.4.4 REWIND ..... 3-5
3.4.5 WRT EN (WRITE ENABLE) ..... 3-5
3.4.6 1600 CPI ..... 3-5
3.4.7 RESET ..... 3-5
3.4.8 SELECT (Optional) ..... 3-5
3.4.9 FPT (File Protect) (Optional) ..... 3-5
3.4.10 Maintenance Switch ..... 3-5
3.5 Interface Inputs (Controller to Transport) ..... 3-6
3.5.1 Select (ISLT) ..... 3-6
3.5.2 Synchronous Forward Command (ISFC) ..... 3-6
3.5.3 Synchronous Reverse Command (ISRC) ..... 3-6
3.5.4 Rewind Command (IRWC) ..... 3-6
3.5.5 Set Write Status (ISWS) ..... 3-7
3.5.6 Write Data Lines (IWDP, IWDO—IWD7) ..... 3-7
3.5.7 Write Data Strobe (IWDS) ..... 3-7
3.5.8 Write Amplifier Reset (IWARS) ..... 3-7
3.5.9 Off-Line (IOFFC) ..... 3-7
3.5.10 Overwrite (IOVW) ..... 3-7
3.5.11 Read Threshold (IRTH2) (T8640A Transport) ..... 3-7
3.5.12 Read Threshold (IRTH1) (T8660A Transport) ..... 3-8
3.5.13 Read Threshold (IRTH2) (T8660A Transport) ..... 3-8
3.5.14 Load and On-Line (ILOL) (Optional) ..... 3-8

## TABLE OF CONTENTS (Continued)

Page
3.6 Interface Outputs (Transport to Controller) ..... 3-8
3.6.1 Ready (IRDY) ..... 3-8
3.6.2 Read Data (IRDP, IRD0—IRD7) ..... 3-8
3.6.3 On-Line ..... 3-8
3.6.4 Load Point (ILDP) ..... 3-8
3.6.5 End of Tape (IEOT) ..... 3-9
3.6.6 Rewinding (IRWD) ..... 3-9
3.6.7 File Protect (IFPT) ..... 3-9
3.7 Interface Timing ..... 3-9
3.7.1 Write and Read Waveforms ..... 3-9
SECTION IV - THEORY OF OPERATION
4.1 Introduction ..... 4-1
4.2 Organization of the Transport ..... 4-1
4.3 Functional Subsystems Description ..... 4-4
4.3.1 Power Supply ..... 4-4
4.3.2 Capstan Drive System ..... 4-5
4.3.3 Tape Storage and Reel Servo Systems ..... 4-7
4.3.4 Data Electronics ..... 4-9
4.3.5 Tape Control System ..... 4-20
SECTION V - PRINTED CIRCUIT BOARDS THEORY OF OPERATION
5.1 Introduction ..... 5-1
5.2 Data F PCBA (T8640A) ..... 5-2
5.2.1 Circuit Description ..... 5-2
5.3 Data G PCBA (T8660A) ..... 5-5
5.3.1 Circuit Description ..... 5-5
5.4 Tape Control J PCBA ..... 5-8
5.4.1 Circuit Description ..... 5-8
SECTION VI - MAINTENANCE AND TROUBLESHOOTING
6.1 Introduction ..... 6-1
6.2 Fuse Identification ..... 6-1
6.3 Scheduled Maintenance ..... 6-1
6.3.1 Cleaning the Transport ..... 6-1
6.4 Part Replacement Adjustments ..... 6-2
6.5 Electrical Adjustments ..... 6-2
6.5.1 Adjustment Philosophy ..... 6-5
6.5.2 $+5 v$ and $-5 v$ Regulators ..... 6-5
6.5.3 EOT/BOT Amplifier ..... 6-6
6.5.4 Capstan Servo Offset ..... 6-7
6.5.5 Ramp Timing ..... 6-8
6.5.6 Tape Speed ..... 6-10
6.5.7 Rewind Speed ..... 6-13
6.5.8 Read Amplifier Gain ..... 6-14
6.5.9 Threshold Generator (Model T8640A Only) ..... 6-16
6.5.10 Threshold Generator (Model T8660A Only) ..... 6-16

## TABLE OF CONTENTS (Continued)

Page
6.6 Mechanical Adjustments ..... 6-17
6.6.1 Tension Arm Limit Switches ..... 6-17
6.6.2 Tension Arm Interlock Switch ..... 6-17
6.6.3 Load Limit Switch ..... 6-18
6.6.4 Gear Motor Limit Switch ..... 6-19
6.6.5 Gear Motor Assembly ..... 6-20
6.6.6 Tension Arm Position Sensor ..... 6-21
6.6.7 Tape Path Alignment ..... 6-23
6.6.8 Universal Tape Path Alignment Tool ..... 6-23
6.6.9 Tape Path Alignment - Takeup ..... 6-23
6.6.10 Takeup Arm Guide Roller ..... 6-25
6.6.11 Tape Path Alignment - Supply ..... 6-29
6.6.12 Supply Arm Guide Roller ..... 6-31
6.6.13 Skew Measurement and Adjustment (Model T8640A) ..... 6-35
6.6.14 Skew Measurement and Adjustment (Model T8660A) ..... 6-37
6.6.15 Head Replacement ..... 6-39
6.6.16 Photosensor Replacement ..... 6-42
6.6.17 Flux Gate Adjustment (Model T8640A) ..... 6-42
6.6.18 Capstan Motor Replacement ..... 6-43
6.6.19 Reel Motor Belt Tension ..... 6-44
6.6.20 Tape Tension ..... 6-45
6.6.21 Supply Reel Hub Replacement ..... 6-49
6.6.22 Takeup Reel Hub Replacement ..... 6-49
6.6.23 Supply Reel Hub Expansion Ring Adjustment ..... 6-50
6.6.24 Write Lockout Assembly ..... 6-50
6.6.25 Tape Cleaner Cleaning and Replacement ..... 6-50
6.7 Maintenance Tools ..... 6-51
6.8 Troubleshooting ..... 6-52
SECTION VII - PARTS LISTS, LOGIC LEVELS AND WAVEFORMS AND SCHEMATICS
7.1 Introduction ..... 7-1
7.2 Illustrated Parts Breakdown ..... 7-1
7.3 Recommended Spare Parts ..... 7-1
7.4 Part Number Cross Reference ..... 7-1
7.5 PCBA Interconnections ..... 7-1
7.6 Logic Levels and Waveforms ..... 7-1
APPENDIX A - GLOSSARY OF TERMS

## LIST OF ILLUSTRATIONS

Figure Page
1-1 Model T8640A Tape Transport, Front View ..... 1-2
1-2 Models T8640A/T8660A Tape Transport, Rear View ..... 1-2
1-3 Model T8640A Tape Transport, Block Diagram ..... 1-3
1-4 Model T8660A Tape Transport, Block Diagram ..... 1-4
1-5 Interface Configuration ..... 1-8
2-1 Carton Placement for Removal of Transport ..... 2-2
2-2 Interface Cable Installation ..... 2-5
2-3 Rack Mounting the Transport ..... 2-7
2-4 Installation Diagram ..... 2-8
3-1 Tape Path ..... 3-1
3-2 Supply Reel Hub, Unlocked ..... 3-3
3-3 Supply Reel Hub, Locked ..... 3-3
3-4 Operational Control Panel ..... 3-4
3-5 Maintenance Switch ..... 3-6
3-6 PE Write and Read Waveforms ..... 3-9
4-1 Organization of T8640A Tape Transport ..... 4-2
4-2 Organization of T8660A Tape Transport ..... 4-3
4-3 Power Supply, Block Diagram ..... 4-4
4-4 Transformer Primary Connections ..... 4-6
4-5 Capstan Servo Block Diagram ..... 4-6
4-6 Typical Capstan Servo Waveforms ..... 4-7
4-7 Reel Servo Diagram ..... 4-8
4-8 Comparison of NRZI and PE Recording Modes ..... 4-10
4-9 9-Track PE Allocation, Spacing, and Format ..... 4-10
4-10 PE Write and Read Waveforms ..... 4-11
4-11 One Channel of Data Electronics, Model T8640A ..... 4-12
4-12 One Channel of Data Electronics, Model T8660A ..... 4-13
4-13 Timing Diagram, Data Recording ..... 4-15
4-14 Timing Diagram, Data Reproduction ..... 4-19
4-15 Tape Control System, Block Diagram ..... 4-27
4-16 Bring-to-Load-Point Sequence Waveforms ..... 4-21
4-17 Rewind Sequence Waveforms ..... 4-26
5-1 Master-Slave Flip-Flop, Simplified Logic Diagram ..... 5-1
5-2 Data F PCBA Test Point and Connector Placement ..... 5-3
5-3 Timing and Signal Relationships, One Channel Read Electronics ..... 5-4
5-4 Data G PCBA Test Point and Connector Placement ..... 5-6

## LIST OF ILLUSTRATIONS (Continued)

Figure ..... Page
5-5 Timing and Signal Relationships, One Channel Read Electronics ..... 5-7
5-6 Tape Control J PCBA Test Point and Connector Placement ..... 5-9
5-7 Heatsink Assembly ..... 5-10
6-1 Ramp Levels and Timing ..... 6-9
6-2 Gear Motor Limit Switch Assembly, Rear View ..... 6-19
6-3 Takeup Tape Path Alignment ..... 6-24
6-4 Supply Tape Path Alignment ..... 6-30
6-5 Skew Waveform (Typical) ..... 6-36
6-6 Skew Waveform (Typical) ..... 6-38
6-7 Head Alignment Template ..... 6-40
6-8 Single-Stack (9-degree) Heat-to-Tape Positioning ..... 6-41
6-9 Dual-Stack (12-degree) Heat-to-Tape Positioning ..... 6-41
6-10 Flux Gate Adjustment ..... 6-43
6-11 Reel Servo Belt Tension Adjustment ..... 6-45
6-12 Supply Tape Tension Adjustment ..... 6-46
6-13 Takeup Tape Tension Adjustment ..... 6-48
6-14 Tape-In-Path (TIP) Reflector Adjustment ..... 6-51
7-1 T8000A Series Transports, Photo Parts Index, Front View ..... 7-2
7-2 T8000A Series Transports, Photo Parts Index, Rear View with PCBAs ..... 7-4
7-3 T8000A Series Transports, Photo Parts Index, Rear View (PCBAs Removed) ..... 7-6

## LIST OF TABLES

Table Page
1-1 Mechanical and Electrical Specifications, Model T8640A ..... 1-6
1-2 Mechanical and Electrical Specifications, Model T8660A ..... 1-7
2-1 Interface Connections, Model T8640A ..... 2-6
2-2 Interface Connections, Model T8660A ..... 2-6
5-1 Jumper Connections, Format ..... 5-14
5-2 Jumper Connections, Options ..... 5-16
6-1 Fuse Identification ..... 6-2
6-2 Preventive Maintenance Schedule ..... 6-2
6-3 Part Replacement Adjustments, Model T8640A ..... 6-3
6-4 Part Replacement Adjustments, Model T8660A ..... 6-4
6-5 Strobe Disks ..... 6-13
6-6 System Troubleshooting ..... 6-53
7-1 T8000A Series Transports, Photo Parts List ..... 7-3
7-2 T8000A Series Transports, Photo Parts List ..... 7-5
7-3 T8000A Series Transports, Photo Parts List ..... 7-7
7-4 T8000A Recommended Spare Parts List ..... 7-8
7-5 Part Number Cross Reference ..... 7-9
7-6 T8000A Series Transports PCBA Interconnections ..... 7-13

## SECTION I <br> GENERAL DESCRIPTION AND SPECIFICATIONS

### 1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the Synchronous Write/Synchronous Read Tape Transports, Models T8640A and T8660A, manufactured by the PERTEC DIVISION of PERTEC COMPUTER CORPORATION, Chatsworth, California.

### 1.2 PURPOSE OF EQUIPMENT

The tape transport has the capability of recording digital data on 9-track magnetic tape at tape speeds up to 45 ips in 1600 cpi Phase Encoded ANSI and IBM compatible format. The data can be completely recovered when tape is played back on any ANSI and IBM compatible transport, or equivalent.

The transport can also synchronously read any 9-track Phase Encoded magnetic tape, at tape speeds up to 45 ips, which has been recorded in Phase Encoded ANSI and IBM compatible format.

The Model T8640A transport utilizes a dual-stack head which has the read and write heads separated by 0.15 inch. This enables simultaneous read and write operations to be performed so data just recorded by the write head can be read by the read head after the tape has moved approximately 0.15 inch. This technique allows writing and checking of data in a single pass.

The Model T8660A transport utilizes a single head for both reading and writing data. Changing from the Read mode to the Write mode is accomplished through internal switching logic.

The transports are designed to operate directly from voltages of 95 to 250 v ac single phase, 48 to 400 Hz power.

### 1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

The Model T8640A transport is shown in Figure 1-1 (the Model T8660A transport is identical in appearance). Tape reels up to $101 / 2$ inches in diameter may be used. All electrical and mechanical components necessary to operate the transport are mounted on the deck which is designed to be hinge mounted in a standard 19-inch EIA rack.

The transport is equipped with an erase head which is automatically activated when writing.

The hinged dust cover protects the magnetic tape, magnetic head, capstan, and other tape path components from dust and other contaminants.

The operational controls, which are illuminated when the relevant functions are being performed, are mounted on a control panel on the front deck and are accessible with the dust cover door closed. Power is supplied through a strain-relieved cord with a standard 3 -pin plug. Interface signals are routed through three printed circuit connectors that plug directly into the printed circuit boards (PCBAs). Access to the PCBAs is from the rear, as shown in Figure 1-2.


Figure 1-1. T8640A Tape Transport, Front View


Figure 1-2. T8640A/T8660A Tape Transports, Rear View

### 1.4 FUNCTIONAL DESCRIPTION

Figures 1-3 and 1-4 are block diagrams of the T8640A and T8660A transports, respectively. A single capstan drive is used for controlling tape motion during the Synchronous Write, Synchronous Read, and Rewind modes. Tape tension is maintained at 7.5 to 10 ounces.

The capstan is controlled by a velocity servo. Velocity information is generated by a dc tachometer directly coupled to the capstan motor shaft and produces a voltage proportional to the rotational velocity of the capstan. This voltage is compared to the reference voltage from the ramp generators using operational amplifier techniques and the difference is used to control the capstan motor. This capstan control technique gives precise control of tape accelerations and tape velocities, thus minimizing tape tension transients.

During a writing operation, tape is accelerated in a controlled manner to the required velocity. This velocity is maintained and data characters are written on the tape at a constant rate such that: Bit Density $=$ Character Rate $\div$ Tape Velocity. When data recording is complete, tape is decelerated to zero velocity in a controlled manner.

Since the writing operation relies on a constant tape velocity, Inter-Record Gaps (IRGs) containing no data must be provided to allow for tape acceleration and deceleration periods. Control of tape motion to produce a defined IRG is provided externally by the customer controller, in conjunction with the tape acceleration and deceleration characteristics defined within the transport.

During a read operation, tape is accelerated to the required velocity; the acceleration time is such that the tape velocity becomes constant before data signals are received.

Nine data channels are presented to the interface.


Figure 1-3. T8640A Tape Transport Block Diagram


Figure 1-4. T8660A Tape Transport Block Diagram

The end of a record is detected in the customer's controller by using Missing Pulse Detector circuits and the tape is commanded to decelerate in a controlled manner.

The transport can operate in the Read mode in either the forward or reverse direction.
When operating in a shuttling mode (e.g., Synchronous Forward, Stop, Synchronous Reverse, and Stop) no turnaround delay is required between the end of one motion command and the beginning of the next motion command in the opposite direction. However, to preserve the normal stop/start times and distances, and to guarantee complete erasure of the gaps, the customer must ensure that tape motion has ceased before changing tape direction or Read/Write status.

In addition to the capstan control system, the transport consists of a mechanical tape storage system, supply and takeup reel servo systems, magnetic head and its associated electronics, and control logic.

The mechanical storage system buffers the relatively fast starts and stops of the capstan from the high inertia of the supply and takeup reels. As tape is taken from or supplied to the storage system, a photoelectric sensor measures the displacement of the storage arm and feeds an error signal to the reel motor amplifier. The capstan ramp signal is amplified and used to control the reel motor such that the reel will either supply or take up tape to maintain the storage arm in its nominal operating position. The storage arm system is designed to give a constant tape tension as long as the arm is within its operating region. This tape path design minimizes tape wear because there is only relative motion of the tape oxide at the magnetic head and tape cleaner.

The magnetic head writes and reads the flux transitions on the tape under control of the data electronics. Switching from the Read After Write to the Read Only mode on the T8640A is accomplished by remote command; switching from the Write to the Read mode on the T8660A is also accomplished by remote command.

The control logic operates on manual commands to enable tape, once loaded, to be brought to the Load Point. At this stage, remote commands control tape motion, writing, and reading. The logic also provides rewind and unload functions in conjunction with the manual REWIND control.

The transport is supplied with a photoelectric sensor for detection of the Beginning of Tape (BOT) tab and End of Tape (EOT) tab. The BOT and EOT signals are sent as a voltage level to the customer's equipment. The BOT signal is also used internally in the transport for control purposes.

The transport is designed with an interlock to protect the tape from damage to component or power failure, or incorrect tape threading. A tape cleaner is provided to minimize tape contamination.

### 1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

Table 1-1 details the mechanical and electrical specifications for the T8640A; Table 1-2 details the mechanical and electrical specifications for the T8660A. Both models are designed to qualify for UL approval.

Table 1-1
Mechanical and Electrical Specifications, Model T8640A


Table 1-2
Mechanical and Electrical Specifications, Model T8660A

| Tape (Computer Grade) |  |
| :---: | :---: |
| Width | $12.6492 \pm 0.0508 \mathrm{~mm}$ ( 0.5 inch ) |
| Thickness | 0.0381 mm ( 1.5 mil ) |
| Tape Tension | 2.224 N (8.0 ounces) |
| Reel Diameter | 266.7 mm (10.5 inches) maximum |
| Recording Mode (ANSI and IBM compatible) | 1600 cpi Phase Encoded |
| Magnetic Head | Single Stack (with Erase Head) |
| Tape Speed, Standard | $\begin{gathered} 1.14,0.953,0.633,0.476,0.317 \mathrm{~m} / \mathrm{s} \\ (45,37.5,25,18.75,12.5 \mathrm{ips}) \end{gathered}$ |
| Instantaneous Speed Variation | $\pm 3 \%$ maximum |
| Long-Term Speed Variation Forward Reverse | $\pm 1 \%$ maximum $\pm 3 \%$ maximum |
| Rewind Speed | $5.08 \mathrm{~m} / \mathrm{s}$ (200 ips) nominal |
| Interchannel Displacement Error | Refer to Paragraph 6.6.14.1 |
| Stop/Start Time at $1.14 \mathrm{~m} / \mathrm{s}$ ( 45 ips ) (inversely proportional to tape speed; measured from 0 to $90 \%$ of actual speed) | $6.5 \pm 0.3 \mathrm{msec}$ |
| Stop/Start Displacement | $4.83 \pm 0.51 \mathrm{~mm}(0.19 \pm 0.02 \mathrm{inch})$ |
| Beginning of Tape (BOT) and End of Tape (EOT) Detectors | Photoelectric (Note 1) IBM Compatible |
| Weight | 38.6 kg (85 pounds) |
| Dimensions |  |
| Height | 622.3 mm (24.5 inches) (Note 2) |
| Width | 482.6 mm (19.0 inches) |
| Depth (from Mounting Surface) <br> Card Cage Open <br> Card Cage Closed | 431.8 mm ( 17.0 inches) maximum 304.8 mm (12.0 inches) maximum |
| Operating Temperature | $2^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}\left(35^{\circ} \mathrm{F}\right.$ to $\left.122^{\circ} \mathrm{F}\right)$ |
| Non-Operating Temperature | $-45^{\circ} \mathrm{C}$ to $71^{\circ} \mathrm{C}\left(-50^{\circ} \mathrm{F}\right.$ to $\left.160^{\circ} \mathrm{F}\right)$ |
| Operating Altitude | 0 to 6,096 m (0 to 20,000 feet) |
| Non-Operating Altitude | 0 to 15,240 m (0 to 50,000 feet) |
| Power |  |
| Volts ac | $\begin{gathered} 95,100,110,115,125,190,200,210, \\ 215,220,225,230,235,240,250 \end{gathered}$ |
| Watts (maximum on high line) | 300 |
| Hertz | 48 to 400 |
| Mounting | Standard 482.6 mm (19 inch) EIA Rack |
| Electronics | All silicon |
| Notes: |  |
| 1. Approximate distance from detection area to head gap equals 30.5 mm ( 1.2 inches). <br> 2. Includes special filler panel. |  |

### 1.5.1 INTERFACE SPECIFICATIONS

Levels: True $=$ Low $=0 v$ (approximately)
False $=$ High $=+3 v$ (approximately)
Pulses: Levels as above. Edge transmission delay over 20 feet of cable is not greater than 200 nsec.

The interface circuits are designed so that a disconnected wire results in a false signal.
Figure 1-5 shows the configuration for which the transmitters and receivers have been designed.


Figure 1-5. Interface Configuration

## SECTION II <br> INSTALLATION AND INITIAL CHECKOUT

### 2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating the transport, and the procedure for electrically connecting and performing the initial checkout of the transport.

### 2.2 UNCRATING THE TRANSPORT

The transport is shipped in a protective container which meets the National Safe Transit Specification (Project 1A, Category 1). The container is designed to minimize the possibility of damage during shipment. The following procedure describes the recommended method for uncrating the transport.
(1) Place the shipping container on a low, flat surface. Ensure that the carton is positioned so that the shipping label, model and serial number information, is visible on the top surface of the carton.
(2) Remove or cut tape from around top of carton and open top flaps. Leave the four polyurethane corner blocks in place between the inner and outer cartons. Refer to Figure 2-1 (A).
(3) Fold outer carton flaps out and away from carton.
(4) Remove Operating and Service Manual taped to inside carton.
(5) Slit tape holding inner carton flaps together.
(6) With the four corner blocks still in place, rotate packing assembly 90 degrees to position shown in Figure 2-1 (B); rotate another 90 degrees until the entire packing assembly is resting upon the four corner blocks and is in the position shown in Figure 2-1(C).

## NOTE

Leaving corner blocks in place prevents inner carton from dropping down possibly causing damage to the transport.
(7) Lift outer carton upward and away from inner carton.
(8) Tilt inner carton and remove blocks at each corner and at the same time fold inner carton flaps out and away from carton.
(9) Lift inner carton up and away from steel shipping framework supporting transport. Note that transport is upside down. Invert shipping framework 180 degrees.
(10) Before removing protective cardboard surrounding rear area of transport from shipping framework, remove hardware kit stapled to it and remove $1 / 2$-inch filler panel taped to the left inboard side of protective cardboard. Remove tape from power cord and remove protective cardboard from shipping framework.

## NOTE

Hardware kit contains all necessary hardware to place transport in service.
(11) Remove tape from transport door and head cover.
(12) Check the contents of the shipping container against the packing slip; investigate the contents for possible damage; notify the carrier immediately if any damage is noted.


Figure 2-1. Carton Placement for Removal of Transport
(13) Check that the identification label (located at the rear of the tape deck) bears the correct model number and line voltage requirements.

CAUTION
if the actual line voltage at the installation DIFFERS FROM THAT ON THE IDENTIFICATION LABEL, the coded jumper plug on the power supply must be changed. REFER TO SECTION IV OF THIS MANUAL.
(14) Check all Molex connectors used in the tape transport and the plugin relays on the PCBAs for full engagement with their mating parts.

### 2.3 POWER CONNECTIONS

A fixed power cord is supplied for use in a polarized 115 v outlet. For other power sockets, the supplied plug must be removed and replaced with the correct plug.

### 2.4 INITIAL CHECKOUT PROCEDURE

Section III contains a detailed description of all transport controls and indicators. To check the operation of the transport before placing it in the system, the following procedure should be performed.

CAUTION
NEVER EXERT PRESSURE ON A TENSION ARM ROLLER While attempting to move the arm into the OPERATING REGION FROM LOAD POSITION. DAMAGE TO the arm actuator gear motor or to the ROLLER GUIDE SHAFT MAY RESULT.
(1) Connect the power cord (replace power plug and change power jumper plug if necessary).
(2) Set the transport power switch to ON.
(3) Load tape on the transport as described in Paragraph 3.3.
(4) Depress the LOAD control momentarily to apply capstan motor and reel motor power.
(5) Depress the LOAD control momentarily a second time to initiate the Load sequence. Tape will move forward and stop when it reaches the BOT tab. The LOAD indicator should illuminate when the BOT reaches the photosensor and remain illuminated until tape moves off the Load Point. At this point, there will be no action when the LOAD control is depressed.
(6) Check On-line by depressing the control repeatedly and observing that the ON LINE indicator is alternately illuminated and extinguished.
(7) With the deck open, i.e., Tape Control PCBA accessible, and the transport Off-line (ON LINE indicator extinguished), run several feet of tape onto the takeup reel by activating the 3-position Maintenance switch located on the tape control PCBA. The Maintenance switch in the up position causes tape to move forward; in the center position, the switch stops tape motion; in the down position, the tape moves in the reverse direction. Refer to Paragraph 3.7 and Figure 3-5 for details concerning the use of the Maintenance switch.
(8) With the transport Off-line, activate the Maintenance switch so that tape moves in reverse direction (Maintenance switch down). Check that if the transport is placed On-line, the action of the Maintenance switch is inhibited. Tape will move in the reverse direction until the BOT tab reaches the photosensor, then it will stop.
(9) Using the Maintenance switch, run several feet of tape onto the takeup reel. Momentarily depress the REWIND control to initiate the Rewind mode and light the REWIND indicator. Tape will rewind past the BOT tab, enter the Load sequence, return to the BOT tab, and stop with the LOAD indicator illuminated. If the REWIND control is momentarily depressed when tape is at BOT, the LOAD indicator will be extinguished and the tape will run in reverse at a low speed until tape tension is lost. This action is used to unload tape. The reel can now be removed as outlined in Paragraph 3.5.
(10) Visually check the tape path components for correct tape tracking (tape rides smoothly in the head guides, etc.).

Should line voltage be lost at any time during the initial checkout of the transport, proceed as follows.

## NOTE

The tape unit is designed to provide dynamic braking to the tape reels in case of power loss. Therefore, minimum tape spillage and no damage to the tape will occur.
(1) Set the power switch/indicator to OFF.
(2) Determine and correct the cause of power loss before reapplying power to the transport.

> NOTE

Refer to Sections VI and VII of this manual for fuse sizes and maintenance procedures.
(3) Manually retension tape and check for correct seating in the guides.
(4) Set the power switch/indicator to ON.
(5) Ensure that the ON LINE indicator is extinguished.
(6) Depress and release the LOAD control; power is now applied to the capstan and reel motors. Tape tension is also established and the tape storage arms are now in the operating position.

## CAUTION

ensure that tape is positioned correctly on ALL GUIDES OR TAPE DAMAGE MAY RESULT.
(7) Depress and release the REWIND control; tape will rewind past the BOT tab, enter the Load sequence, return to the BOT tab and stop with the LOAD indicator illuminated.
(8) Resume initial checkout of the transport.

### 2.5 INTERFACE CONNECTIONS

It is assumed that interconnection of PERTEC and Customer equipment uses a harness of individual twisted pairs, each with the following characteristics.
(1) Maximum length of 20 feet.
(2) Characteristic impedance of 110 to 150 ohms.
(3) 22- or 24 -gauge conductor with minimum insulation thickness of 0.254 mm ( 0.01 inch).

It is important that the ground side of each twisted pair is grounded within a few inches of the board to which it is connected.

Three printed circuit edge connectors are required for each transport. These are ELCO connectors, Part No. 00-6007-036-980-002 (PERTEC 503-0036), which can be supplied (no charge) upon request. Each connector must be wired by the customer and strain relieved as shown in Figure 2-2. Interface signals are thus routed directly to and from the PCBAs. Table 2-1 shows the input/output lines for the T8640A transport; Table 2-2 shows the input/output lines for the T8660A transport. Details relating to the interface are contained in Section III.

### 2.6 RACK MOUNTING THE TRANSPORT

The physical dimensions of the transport are such that it may be mounted in a standard 482.6 mm (19-inch) EIA rack; 622.3 mm ( 24.5 inches) of panel space, including a $1 / 2$-inch spacer panel, is required. With the cardcage closed, a depth of at least 304.8 mm ( 12.0 inches) is required behind the mounting surface for units without an MTA installed. Figures 2-3 and 2-4 illustrate the procedure for mounting the transport, as follows.

## CAUTION

the transport weighs 85 POUNDS. CARE SHOULD be taken to avoid injury to personnel or DAMAGE TO THE TRANSPORT.
(1) Install the hinge pin blocks on the EIA rack (see Figure 2-3 for correct positioning). Do not fully tighten the screws. Place a shim washer on the top hinge pin.
(2) Set the shipping frame down with the front door of the transport facing up (i.e., lying in a horizontal position). Remove the screws securing the Z-shaped shipping blocks to the frame.

## CAUTION

SECURE THE EIA RACK SO THAT IT WILL NOT TIP OR MOVE WHEN THE TRANSPORT IS POSITIONED UPON THE HINGE PIN BLOCKS.
(3) Hang the transport on the hinge pin blocks by lifting it up to the hinge pin blocks on a 45-degree angle to its closed position (see Figure 2-4).
(4) Remove the $Z$-shaped shipping blocks from the tape deck.
(5) Adjust the hinge pin blocks on the EIA rack so that the transport hangs symmetrically in the rack. Tighten the screws.
(6) Check that the fastener engages behind the EIA rack.
(7) Clean the tape deck as described in the maintenance procedure.


Figure 2-2. Interface Cable Installation

Table 2-1
Interface Connections, Model T8640A
Table 2-2
Interface Connections, Model T8660A

| Transport Connector Mating Connector |  |  | 36 Pin Etched PC Edge Connector 36 Pin ELCO 00-6007-036-980-002 <br> Signal* |
| :---: | :---: | :---: | :---: |
| Connector | Live Pin | Gnd Pin |  |
| $\begin{gathered} \text { J101 } \\ \text { Tape } \\ \text { Control } \\ \text { PCBA } \end{gathered}$ | $\begin{gathered} \mathrm{D} \\ \mathrm{~F} \\ 1 \\ \mathrm{~J} \\ \mathrm{~A} \\ 18 \\ \mathrm{~V} \\ \mathrm{C} \\ \mathrm{E} \\ \mathrm{H} \\ \mathrm{~L} \\ \mathrm{~K} \\ \mathrm{~B} \\ \mathrm{~T} \\ \mathrm{M} \\ \mathrm{~N} \\ \mathrm{U} \\ \mathrm{R} \\ \mathrm{P} \\ 15 \end{gathered}$ | $\begin{array}{r} 4 \\ 6 \\ 2 \\ 2 \\ 8 \\ 8 \\ 8 \\ 8 \\ 3 \\ 5 \\ 7 \\ 10 \\ 9 \\ 2 \\ 16 \\ 11 \\ 12 \\ 17 \\ 14 \\ 13 \end{array}$ | DATA DENSITY SELECT (IDDS) <br> DATA DENSITY INDICATOR (IDDI) <br> LOAD ON LINE (ILOL) <br> SELECT 0 (ISLTO) <br> SELECT 1 (ISLT1) <br> SELECT 2 (ISLT2) <br> SELECT 3 (ISLT3) <br> SYNCHRONOUS FORWARD Command (ISFC) <br> SYNCHRONOUS REVERSE Command (ISRC) <br> REWIND Command (IRWC) <br> OFF-LINE Command (IOFFC) <br> SET WRITE STATUS (ISWS) <br> OVERWRITE Command (IOVW) <br> READY (IRDY) <br> ON-LINE Command (IONLINE) <br> REWINDING (IRWD) <br> END OF TAPE (IEOT) <br> LOAD POINT (ILDP) <br> FILE PROTECT (IFPT) <br> WRITE AMPLIFIER RESET (IWARS) ** |
| $\begin{aligned} & \text { J102 } \\ & \text { Data } \\ & \text { PCBA } \end{aligned}$ |  | $\begin{array}{r} 1 \\ 3 \\ 5 \\ 6 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \\ 17 \\ 18 \end{array}$ | WRITE DATA STROBE (IWDS) <br> WRITE AMPLIFIER RESET (IWARS) <br> READ THRESHOLD 1 (IRTH1) <br> READ THRESHOLD 2 (IRTH2) <br> WRITE DATA PARITY (IWDP) <br> WRITE DATA 0 (IWDO) <br> WRITE DATA 1 (IWD1) <br> WRITE DATA 2 (IWD2) <br> WRITE DATA 3 (IWD3) <br> WRITE DATA 4 (IWD4) <br> WRITE DATA 5 (IWD5) <br> WRITE DATA 6 (IWD6) <br> WRITE DATA 7 (IWD7) |
| $J 103$ <br> Data <br> PCBA | $\begin{array}{r} 1 \\ 3 \\ 4 \\ 8 \\ 9 \\ 14 \\ 15 \\ 17 \\ 18 \end{array}$ | A C D J K R S U V | READ DATA PARITY (IRDP) <br> READ DATA 0 (IRDO) <br> READ DATA 1 (IRD1) <br> READ DATA 2 (IRD2) <br> READ DATA 3 (IRD3) <br> READ DATA 4 (IRD4) <br> READ DATA 5 (IRD5) <br> READ DATA 6 (IRD6) <br> READ DATA 7 (IRD7) |
| *See Section III for definitions of interface functions. <br> **This signal must be grounded externally to J102, pin C of the Data PCBA. |  |  |  |



Figure 2-3. Rack Mounting the Transport


Figure 2-4. Installation Diagram

## SECTION III OPERATION

### 3.1 INTRODUCTION

This section explains the manual operation of the transport and defines the interface functions with regard to timing, levels, and interrelationships.

### 3.2 CLEANING THE HEAD AND GUIDES

The brief operation described in Paragraph 6.4 should be performed daily to realize the data reliability capabilities of the transport.

### 3.3 LOADING TAPE ON THE TRANSPORT

The supply reel (reel to be recorded or reproduced) is at the top, adjacent to the manual controls (see Figure 3-1). Tape must unwind from the supply reel when the reel is turned in a clockwise direction. Note that the presence of a Write Enable ring on the reel is required to close the interlocks which allow writing.


Figure 3-1. Tape Path

Tape loading is easily accomplished through use of a quick-release supply hub. Figure 3-2 shows the hub in the unlocked position, i.e., ready for mounting a $101 / 2-$ inch reel of tape. When the hub is in the unlocked position, note that a red band is visible. A view of the hub with a reel of tape loaded and the latch in the locked position is shown in Figure 3-3.

The following procedure is followed when loading a reel of tape on the transport.
(1) Unlock the quick-release actuator on the supply reel by depressing the indented section of the latch exposing the red band.
(2) Position a reel of tape over the quick-release hub. The Write Enable ring (or slot) of the tape reel must be toward the transport.

NOTE
It is not necessary to hold the reel against the back flange of the hub. When the reel is placed on the hub, six reelretaining pawls provide proper alignment of the reel.
(3) Lock the quick-release hub actuator. This is done by depressing the indented section of the actuator.

The reel is now properly mounted and is ready for tape threading. Thread tape along the path shown in Figure 3-1. Wrap the tape leader onto the installed takeup reel so that tape will be wound onto the reel when it is rotated clockwise. Wind several turns onto the takeup reel, then turn the supply reel counterclockwise until slack tape has been taken up.

NOTE
The transport is supplied with the takeup reel installed. Refer to Section VI for installation and removal instructions for the reel, if required.

### 3.3.1 BRINGING TAPE TO LOAD POINT (BOT)

After tape has been manually tensioned and checked for correct seating in the guides, then, to bring the tape to Load Point:
(1) Set the power switch to ON. The indicator will be illuminated.
(2) Depress and release the LOAD control. This enables the tension arm cocking motor which causes the tension arms to move to their operating region. When the arms have moved to the $3 / 4$ position of the total arm movement, power will be applied to the capstan and reel servos which brings the tape to the correct operating tension and position.

CAUTION
CHECK THAT TAPE IS POSITIONED CORRECTLY ON ALL GUIDES OR TAPE DAMAGE MAY RESULT.
(3) Depress and release the LOAD control a second time. This will cause tape to move forward at the operating velocity. Recheck tape tracking in the guides and close the dust cover.

CAUTION
the dust cover should remain closed at all times when tape is on the takeup reel. data RELIABILITY MAY BE IMPAIRED BY CONTAMINANTS IF THE COVER IS LEFT OPEN.
When the reflective tab is at the Load Point (the BOT tab is detected), tape stops with the front edge of the tab approximately one inch from the magnetic head gap. The transport is now ready to receive external commands.


Figure 3-2. Supply Reel Hub, Unlocked


Figure 3-3. Supply Reel Hub, Locked

### 3.3.2 UNLOADING TAPE

To unload a recorded tape, complete the following procedure if power has been switched off; if power is on, start at Step (3).
(1) Set the power switch to ON. The indicator will be illuminated.
(2) Depress and release the LOAD control; tape will become tensioned.
(3) Depress and release the REWIND control. When tape has rewound to the BOT tab, it will come to a controlled stop. Tape overshoots and the transport enters the Load sequence to bring tape to rest at the BOT.
(4) Depress and release the REWIND control a second time. This initiates an unload action which moves tape in reverse at a low speed until tension is lost. The tension arms move to the tape threading position.
(5) Open the dust cover and wind the end of tape onto the supply reel.
(6) Unlock the quick-release actuator by depressing the indented section.
(7) Remove the reel of tape and close the dust cover.

### 3.4 MANUAL CONTROLS

Seven operational controls with indicators are located on the control panel on the front of the transport. The operational control panel is shown in Figure 3-4. The following paragraphs describe the functions of these controls.

### 3.4.1 ON/OFF

The ON/OFF power control is a toggle action switch/indicator which connects line voltage to the power transformer. The indicator is illuminated when power is ON and the $+5 v$ regulator is operating. When power is turned ON:
(1) All power supplies are established.
(2) All of the motors are open-circuited.
(3) A reset signal is applied to key control flip-flops.
(4) If the tape path is open, tension arms will move to the tape threading position.


Figure 3-4. Operational Control Panel

### 3.4.2 LOAD

The LOAD control is a momentary switch/indicator. When the tension arms are in the retracted position, depressing and releasing the LOAD control for the first time after power is switched ON energizes the servo systems by connecting the motors to the drive circuits. The servo systems are energized after the arms have moved more than $3 / 4$ into the operating area and tape is tensioned. The reset signal is removed after the tension arm actuator motors have moved the arms out of the normal operating area.

When the tension arms are in the load position, depressing and releasing the control for the first time after power is switched ON will start the tension arms moving into the operating area. The reset signal is removed and the tape will now be tensioned.

Depressing and releasing the LOAD control for the second time causes tape to move to the Load Point and stop. The transport is now ready to receive external commands. While the BOT tab is located over the photosensor, the LOAD indicator is lit, indicating that the transport is ready for use. The LOAD control is disabled after the first LOAD or manual REWIND command has been given and can only be reenabled by loss of tape tension or restoration of power after power has been off.

### 3.4.3 ON LINE

The ON LINE control is a momentary switch/indicator which is enabled after an initial Load or Rewind sequence has been initiated. Depressing and releasing the switch after an initial Load or Rewind sequence is initiated switches the transport to an On-line mode and illuminates the indicator. In this condition the transport can accept external commands provided it is also Ready and Selected.

The transport will revert to the Off-line mode if any of the following occur.
(1) ON LINE is depressed a second time.
(2) External OFF-LINE command (IOFFC) is received.
(3) Tape tension is lost.
(4) RESET switch/indicator is depressed.

### 3.4.4 REWIND

The REWIND control is a momentary switch/indicator which is enabled only in the Off-line mode. Depressing and releasing the control causes tape to rewind at 200 ips after an 0.1 -second delay. Upon reaching the BOT tab, the rewind ceases and the Load sequence is automatically entered. The BOT tab will overshoot the photosensor, move forward, and stop at the Load Point.

If the REWIND control is depressed and released when tape is at Load Point (LOAD indicator illuminated), the tension arms will move to a position close to their stops and tape will move in the reverse direction until tape tension is lost.

The REWIND indicator is illuminated throughout any rewind operation including the subsequent Load sequence, where relevant. A manual REWIND command will override the Load sequence.

### 3.4.5 WRT EN (WRITE ENABLE)

The WRT EN indicator is illuminated whenever power is ON and a reel of tape with a Write Enable ring installed is mounted on the transport.

### 3.4.6 1600 CPI

This is an indicator which is illuminated whenever power is applied to the transport.

### 3.4.7 RESET

The RESET control is a momentary action swtich/indicator which stops all manual commands except Unload and manual Maintenance switch commands when the switch is depressed. Depressing the RESET switch when the transport is On-line causes the transport to revert to the Off-line mode.

### 3.4.8 SELECT (OPTIONAL)

The Select switch is an option which must be specified at the time the transport is ordered. It is an 8 -position rotary switch which provides selective addressing of four transports. The address (0-3) can be changed only when the transport is in the Off-line mode.

### 3.4.9 FPT (FILE PROTECT) (OPTIONAL)

The FPT indicator is an option which must be specified at the time the transport is ordered. The indicator is illuminated whenever power is ON and a reel of tape without a Write Enable ring installed is mounted on the transport.

### 3.4.10 MAINTENANCE SWITCH

In addition to the manual controls and indicators located on the front panel, the Tape Control PCBA has a 3-position toggle switch (illustrated in Figure 3-5) that provides manual control of tape motion when the transport is in the Off-line mode.

When the switch is in the up position, tape will move in the forward direction at nominal speed; when the switch is in the center position, tape motion will cease; when the switch is in the down position, tape will move in the reverse direction at nominal speed.


Figure 3-5. Maintenance Switch

### 3.5 INTERFACE INPUTS (CONTROLLER TO TRANSPORT)

All waveform names are chosen to correspond to the logical true condition. Receivers belong to the DTL 930 series where the True level is Ov and the False level is nominally +3 v . Figure $1-5$ is a schematic of the interface circuit.

### 3.5.1 SELECT (ISLT)

This is a level which, when true, enables all of the interface drivers and receivers in the transport, thus connecting the transport to the controller. It is assumed that all of the interface inputs discussed in the following paragraphs are gated with SELECT.

### 3.5.2 SYNCHRONOUS FORWARD COMMAND (ISFC)

This is a level which, when true and the transport is Ready (Paragraph 3.6.1) and On-line (Paragraph 3.6.3), causes tape to move forward at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times.

### 3.5.3 SYNCHRONOUS REVERSE COMMAND (ISRC)

This is a level which, when true and the transport is Ready (Paragraph 3.6.1) and On-line (Paragraph 3.6.3), causes tape to move in the reverse direction at the specified velocity. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times. An ISRC will be terminated upon encountering the BOT tab, or ignored if given when tape is at Load Point.

### 3.5.4 REWIND COMMAND (IRWC)

This is a pulse (minimum width of $1 \mu \mathrm{sec}$ ) which, if the transport is Ready, causes tape to move in the reverse direction at 200 ips after a 0.3-second delay. Upon reaching BOT, the rewind ceases and the Load sequence is automatically initiated. Tape now moves forward and comes to rest at BOT.

The REWIND indicator is illuminated for the duration of the Rewind and the following Load sequence. An IRWC is ignored if tape is already at BOT.

The velocity profile is trapezoidal with a rise time of approximately 1.0 second and a fall time of approximately 0.5 second.

### 3.5.5 SET WRITE STATUS (ISWS)

This is a level which must be true for a minimum period of 20 usec after the leading edge of an ISFC (or ISRC) when the Write mode of operation is required. The leading edge of the delayed ISFC (or ISRC) is used to sample the ISWS signal and sets the Write/Read flip-flop in the Write state.

If the Read mode of operation is required, the ISWS signal must be false for a minimum period of $20 \mu \mathrm{sec}$ after the front edge of an ISFC (or ISRC), in which case the Write/Read flip-flop will be set to the Read state.

### 3.5.6 WRITE DATA LINES (IWDP, IWDO—IWD7)

These are Phase Encoded waveforms representative of data bits which, at the time of IWDS, are transferred into the Write flip-flops. The transport must be in the Write mode for data transfer to occur.

The Write Data lines should have settled at least 0.5 usec before the leading edge of the IWDS and should remain steady until $0.5 \mu \mathrm{sec}$ after the trailing edge of the IWDS pulse.

### 3.5.7 WRITE DATA STROBE (IWDS)

This is a pulse ( 1 usec minimum width) for each flux reversal to be recorded. The frequency of the IWDS is twice the character transfer rate. The IWDP and IWDO-IWD7 levels must be steady for 0.5 usec before, during, and after the IWDS. The trailing edge of IWDS is employed to copy the phase encoded waveform into the transport.

### 3.5.8 WRITE AMPLIFIER RESET (IWARS)

This is a pulse ( 1 usec minimum width) which, when true, turns off the write current in the transport. This signal occurs coincident with the last flux transition of the postamble and is used only in conjunction with Overwrite (Paragraph 3.5.10).

### 3.5.9 OFF-LINE (IOFFC)

This is a level or pulse of a minimum width of $1 \mu \mathrm{sec}$ which resets the On-line flip-flop to the false state, placing the transport under manual control. It is gated by SELECT, allowing an OFF-LINE command to be given while a rewind is in progress. OFF-LINE must be separated by at least 1 usec from a REWIND command.

### 3.5.10 OVERWRITE (IOVW)

This is a level which, when true, conditions the appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the Write mode to use the IOVW feature. The Set Write Status (ISWS) signal must be used in conjunction with IOVW when updating isolated records.

### 3.5.11 READ THRESHOLD (IRTH2) (T8640A TRANSPORT)

This is a level which, when true, selects a low threshold level for the Read circuits. This level is selected only when it is required to recover very low amplitude data. IRTH2 must be held steady for the duration of each record being read.

### 3.5.12 READ THRESHOLD (IRTH1) (T8660A TRANSPORT)

This is a level which, when true, conditions the read electronics to operate in the high read threshold mode. When false, the read electronics revert to the normal read threshold. The true level will normally be used only when it is required to perform a read-after-write data check.

### 3.5.13 READ THRESHOLD (IRTH2) (T8660A TRANSPORT)

This is a level which, when true and in the Read mode and IRTH1 is false, selects an extra low threshold level for the Read circuits. This level will normally be made true only when it is required to recover very low amplitude data. IRTH2 must be held steady for the duration of the record.

### 3.5.14 LOAD AND ON-LINE (ILOL) (OPTIONAL)

This is a pulse which, when true, enables a remote load sequence. A second pulse on this line, spaced a minimum of 1 second from the initial pulse, causes the transport to be placed on-line. This option must be specified when the transport is ordered.

### 3.6 INTERFACE OUTPUTS (TRANSPORT TO CONTROLLER)

All the interface outputs discussed in the following paragraphs are gated with SELECT and ON-LINE.

### 3.6.1 READY (IRDY)

This is a level which is true when the transport is ready to accept any external command, i.e., when
(1) Tape tension is established.
(2) Initial LOAD or REWIND command has been completed.
(3) No subsequent REWIND command is in progress.
(4) Transport is on-line.

### 3.6.2 READ DATA (IRDP, IRDO—IRD7)

The signals on these 9 lines are the outputs of the 9 peak detectors, individually gated with the outputs of an envelope detector associated with each channel. These signals are a replica of the PE waveforms used to drive the write amplifiers.

The characteristics of any threshold detector are such that the signal from approximately four successive bits must exceed the threshold level before the detector will enable the output gate for its channel. If the signal suddenly ceases (e.g., due to a dropout), the threshold detector disables the output gate to its channel approximately two bits after the dropout.

### 3.6.3 ON-LINE

This is a level which is true when the On-line flip-flop is set. When true, the transport is under remote control; when false, the transport is under local control.

### 3.6.4 LOAD POINT (ILDP)

This is a level which is true when the transport is Ready and tape is at rest with the BOT tab under the photosensor. The signal goes false after the tab leaves the photosensor area.

### 3.6.5 END OF TAPE (IEOT)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photosensor. Circuitry using this output should not assume that the transitions to and from the true state are clean.

### 3.6.6 REWINDING (IRWD)

This is a level which is true when the transport is engaged in any Rewind operation or the Load sequence following a Rewind operation.

### 3.6.7 FILE PROTECT (IFPT)

This is a level which is true when power is ON and a reel of tape (without a Write Enable ring installed) is mounted on the transport.

### 3.7 INTERFACE TIMING

### 3.7.1 WRITE AND READ WAVEFORMS

Figure 3-6 shows the Phase Encoded write and read waveforms. The controller generates all command waveforms.


Figure 3-6. PE Write and Read Waveforms

# SECTION IV <br> THEORY OF OPERATION 

### 4.1 INTRODUCTION

This section provides an operational description of the transports.
The transports have the mechanical and electronic components necessary to handle tape in such a manner that data can be reproduced from a tape recorded on any 9 -track, phase encoded, ANSI and IBM compatible tape transport, and a tape can be recorded from which data can be completely recovered when played back on any 9-track ANSI and IBM compatible tape transport. The transports consist of the following components.
(1) Power supply
(2) Capstan drive system
(3) Tape storage and reel servo systems
(4) Magnetic head and associated tape guides and cleaner
(5) Data electronics
(6) Tape control system.

### 4.2 ORGANIZATION OF THE TRANSPORT

A highly modular construction technique has been adopted, with all of the major components and subassemblies interconnected by means of connectors rather than the more conventional wiring techniques. Refer to Figure 4-1 for the T8640A tape transport configuration; refer to Figure 4-2 for the T8660A tape transport configuration.

The Tape Control PCBA and the Data PCBA are mounted in a card cage parallel to the tape deck. The Tape Control PCBA contains the conrol logic, reel servo amplifiers, capstan servo amplifier, voltage regulators, photosensor amplifiers, and interlock relay. With the exception of the magnetic head, all of the deck-mounted components (power supply, motors, tension arm position sensors, photosensors, etc.) plug directly into the circuit board. A printed circuit edge connector carries the interface signals to and from the board.

The Data PCBA (nearest the deck) is dedicated to the writing and reading of data. Write data signals enter by means of a printed circuit edge connector on one end of the board; they are buffered and transferred to the write head through a connector (one of two) in the middle of the board. Read signals enter the board via the head connector (second of the two) and are fed to the amplifiers, peak detectors, envelope detectors, and transmitters. Digital read signals, together with a Read Data Strobe, are transmitted by means of a second interface edge connector.

DC power and three control levels are obtained from the Tape Control PCBA through a single harness.

### 4.3 FUNCTIONAL SUBSYSTEMS DESCRIPTION

### 4.3.1 POWER SUPPLY

Figure 4-3 is a block diagram of the power supply which is in two parts. The first part, the power supply module, is fastened to the deck plate. The module contains the power transformer, rectifier, capacitors, fuses, and a number of power resistors. Two unregulated supplies are generated at nominal voltages of $+18 \mathrm{v},-18 \mathrm{v}$.


Figure 4-1. T8640A Tape Transport Organization


Figure 4-2. T8660A Tape Transport Organization


Figure 4-3. Power Supply Block Diagram

The second part consists of the $\pm 10 \mathrm{v}$ and $\pm 5 \mathrm{v}$ regulators which are located on the Tape Control PCBA. Interconnection between the two parts is provided by a harness from the power supply module which plugs into the Tape Control PCBA via a 9 -pin and a 6 -pin connector.

Selection of proper ac voltage taps on the power transformer is facilitated through use of a coded jumper plug assembly shown in Figure 4-4. A cross reference of various line voltages to jumper plug assemblies (PERTEC part numbers and pin connections) is also shown.

Line voltage is connected to the transformer via the POWER control. The POWER control neon indicator is connected across 115 vac , independent of line voltage. Unregulated dc (at a nominal $\pm 18 \mathrm{v}$ under load) is used to power the motors and voltage regulators. Four regulated supplies are generated. The +10 v and -10 v supplies can supply up to 1.0 amp . The +5 v and -5 v supplies are adjusted, regulated, and can supply 3.0 amps and 1.0 amp , respectively. Connections may be provided to the optional microformatter 5 v regulator.

Overvoltage protection on all regulated supplies is provided by an SCR crowbar circuit. The SCRs are connected between the +18 v and Ov and between the -18 v and Ov . The activation of either SCR will blow the applicable fuse and turn off the regulators on the other supply line. A short circuit on any regulator output will turn off all of the regulators.

### 4.3.2 CAPSTAN DRIVE SYSTEM

Figure $4-5$ is a block diagram of the capstan servo which consists of three parts: the deck-mounted capstan drive assembly, consisting of the motor-tachometer combination and the capstan; the ramp generators; and, the capstan drive amplifier on the Tape Control PCBA. Relay contacts disconnect the motor from the amplifier when tape tension is lost. When the motor is disconnected, a low resistance path to ground is established for enhancing the capstan motor stop profile.

Tape is moved by the capstan at a velocity determined by the velocity servo and the output of one of the two ramp generators. If the Forward ramp generator is selected, the voltage at resistor R 1 rises at a rate corresponding to the required start time of the tape. The amplifier then accelerates the motor and the tape; the feedback voltage from the tachometer produces current in resistor R4, which tends to reduce the amplifier input current produced by the selected ramp generator. The voltage at resistor R1 stops rising after the required start time and the velocity builds up to the point where the currents in resistors R4 and R1 are approximately equal and opposite.

The Forward ramp generator is activated by the SYNCHRONOUS FORWARD command (ISFC) or a Load sequence. The Reverse ramp generator is activated by a SYNCHRONOUS REVERSE command (ISRC) and the Rewind ramp generator by a REWIND command (IRWC), either remote or manual. When the transport is in the standby condition, neither ramp generator is activated. In this case, the velocity servo holds the capstan stationary.

Both Forward and Reverse ramps rise and fall in a time calculated to produce start-stop distances of $0.19 \pm 0.02 \mathrm{inch}$, e.g., 15.0 msec for a 25 ips transport. Typical waveforms are shown in Figure 4-6.

The Rewind ramp rise and fall times are not critical; they are approximately 1 sec for start and 0.5 sec for stop. They are chosen so as to allow the reel servos to keep up with the rise and fall in tape speed.


| AC LINE <br> VOLTAGE | PERTEC <br> PART NO. | CON <br> TO |  |  |  | PIN 23 <br> TO | PIN 1 <br> TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | PIN 24 <br> TO | FROM | TO |  |  |  |
| 95 | $104533-01$ | 3 | 19 | 8 | 16 |  |  |
| 100 | $104533-02$ | 6 | 19 | 11 | 16 |  |  |
| 110 | $104533-03$ | 9 | 19 | 14 | 16 |  |  |
| 115 | $104533-04$ | 6 | 22 | 11 | 17 |  |  |
| 125 | $104533-05$ | 9 | 22 | 14 | 17 |  |  |
| 190 | $104533-06$ | 3 | 19 |  |  | 8 | 16 |
| 200 | $104533-07$ | 6 | 19 |  |  | 11 | 16 |
| 210 | $104533-08$ | 6 | 19 |  |  | 14 | 16 |
| 215 | $104533-09$ | 6 | 22 |  |  | 11 | 16 |
| 220 | $104533-10$ | 9 | 19 |  |  | 14 | 16 |
| 225 | $104533-11$ | 9 | 22 |  |  | 11 | 16 |
| 230 | $104533-12$ | 6 | 22 |  |  | 11 | 17 |
| 235 | $104533-13$ | 9 | 22 |  |  | 14 | 16 |
| 240 | $104533-14$ | 6 | 22 |  |  | 14 | 17 |
| 250 | $104533-15$ | 9 | 22 |  |  | 14 | 17 |
|  |  |  |  |  |  |  |  |

Figure 4-4. Transformer Primary Connections


Figure 4-5. Capstan Servo Block Diagram


Figure 4-6. Typical Capstan Servo Waveforms

### 4.3.3 TAPE STORAGE AND REEL SERVO SYSTEMS

Identical non-linear position servos control the supply and takeup of tape by the reels. Figure 4-7 is a diagram of one complete reel servo, together with part of a second, and the relevant interconnections. The components of the servo are:
(1) Tension arm position sensor
(2) Pulleys, belt, tension arm, and tape reel
(3) Reel motor
(4) Servo amplifiers (delay network, current limiter, and power amplifier) on the Tape Control PCBA.

The tension arms establish tape tension and isolate the inertia of the reels from the capstan. Low-friction ball bearing guides are used to minimize tape tension variations. The angular position of the tension arm is sensed by a photosensitive potentiometer which produces a voltage output proportional to the arm position. This output is amplified and drives the reel motor in the direction to center the tension arm. The geometry of the tension arm and spring ensures that only negligible tape tension changes occur as the storage arm moves through a 60 -degree arc.

With tape stationary, the storage arms take a position such that the amplified tension arm sensor output, when applied to the reel motor, provides sufficient torque to balance the tension arm spring torque.

Initially, when the tension arm is in the center of its range, the sensor is set by rotating the shutter on the tension arm shaft for +0.6 v output at the emitter of the input transistor of the stabilization network.

When the capstan injects a tape velocity transient in either direction, the arm moves and the high gain amplifier, together with the current limiter, causes a predetermined current to flow in the reel motor in such a direction to stop the arm at a predetermined position. In addition, a voltage from the Forward/Reverse capstan ramp generator, suitably delayed, is


Figure 4-7. Reel Servo Diagram
subtracted from the arm sensor input. This causes the steady state displacement of the arm to be large in spite of the high amplifier gain so that storage associated with the complete arm movement is available when the capstan velocity reverses. The high amplifier gain ensures little variation in arm displacement as the reel velocity varies due to changes in the effective reel diameter from an empty to full reel condition.

Without tape, the arms rest against the stops and the tension arm limit switch is open, deenergizing the interlock relay. When the relay is deenergized, the two reel motors are disconnected from their respective amplifiers and connected to ground (the supply motor directly, and the takeup motor via a resistor); thus providing a dynamic braking effect. The characteristics of the system ensure that when power is lost in the Rewind mode, the two reels come to rest in such a manner that proper tape tension is not exceeded and significant tape spillage does not occur. The dynamic braking feature is also useful when tape tension is lost in the tape unload operation.

The reel motors operate from two voltage sources supplied by the power supply. One voltage source supplies the reel servo amplifiers when tape is transported, the other voltage source enables the reel motors to rewind tape onto the supply reel at approximately 200 ips . Transfer of the reel motor voltages is accomplished by a relay located on the Tape Control PCBA.

### 4.3.4 DATA ELECTRONICS

Information is recorded on tape in the Phase Encoded (PE) mode. The PE system interprets a flux change toward the magnetization direction of the IRG as one bit. A flux change in the opposite direction represents a zero bit. A phase flux reversal is written between successive one bits or between successive zero bits to establish proper polarity. Thus, up to two flux changes are required per bit for the PE method of data decoding.

The PE method of recording data differs from the NRZI method in that the NRZI employs only one flux change in either direction to represent a one bit, and the lack of a flux change to represent a zero bit.

Figure 4-8 illustrates the basic recording waveform components of the NRZI and PE modes. Note that in the PE mode there is a flux shift within each cell period indicative of a one or zero bit. The direction of magnetic flux change on the tape at the center of the bit cell determines its value (zero or one).

Figure 4-9 illustrates the relevant 9-track allocation, spacing, and format of 1600 cpi PE tape. Consecutive data channels are not allocated to consecutive tracks. This organization increases tape system reliability because the most used data channels are located near the center of the tape. Consequently, they are least subject to errors caused by contamination of the tape.

The data block is preceded by a preamble consisting of 40 bytes of all zeros and one byte of all ones. Note that the data block is followed by a postamble which is the mirror image of the preamble, i.e., one byte of all ones followed by 40 bytes of all zeros.

The preamble and postamble bursts are configured so that during a Read Reverse operation, their functions are interchangeable.


Figure 4-8. NRZI and PE Recording Mode Comparison


Figure 4-9. 9-Track PE Allocation, Spacing, and Format

During a Read operation, as tape passes over the read/write head, any flux pattern recorded on tape (one or zero) generates a waveform in its appropriate data track. It is important to note that during a Read Reverse operation the read signal is inverted, i.e., a one bit is a negative transition and a zero bit is a positive transition.

Figure 4-10 illustrates the waveforms that occur on a channel during a write and read-back operation. Magnetization transitions recorded on tape are not perfectly sharp because of the limited resolution of the magnetic recording process.

During read-back, the voltage induced in the head is amplified, differentiated, and then applied to a Schmitt trigger and an envelope detector. The differentiator and Schmitt trigger form a peak detector. The envelope detector performs a gating function. Thus, the output is present on the interface line only when a data block is present.


Figure 4-10. PE Write and Read Waveforms

Figures 4-11 and 4-12 are functional logic diagrams of one channel of data electronics and the relevant common control logic for T8640A and T8660A, respectively, and are to be used only for purposes of describing system operation.

### 4.3.4.1 Operation with Dual- and Single-Stack Heads

The T8640A transport utilizes a dual-stack head which enables simultaneous read and write operations to take place, thus allowing writing and checking of data in a single pass.

Gap scatter and parallelism between the write and read heads is held within tight limits so that correction is not necessary.

The read head azimuth adjustment is provided by shimming the fixed head guides adjacent to the head so that the tape tracks at 90 degrees to the read head gap.

The T8660A transport utilizes a single-stack head for both read and write operations. Azimuth alignment is accomplished again by shimming the fixed head guides adjacent to the head so that the tape tracks at exactly 90 degrees to the head gap.


Figure 4-11. One Channel of Data Electronics (T8640A)


Figure 4-12. One Channel of Data Electronics (T8660A)

### 4.3.4.2 Data Recording (Dual Stack Model T8640A)

Figure $4-13$ is a timing diagram illustrating the relationship of signals during data recording and should be referred to in conjunction with Figure 4-11. Assume that the transport is Selected, Ready, On-line, and has a Write Enable ring installed. The WRT POWER control line will therefore be at $+5 v$ providing power for the head driver circuits.

When an ISFC is received, the MOTION signal generated on the Tape Control PCBA goes high, removing one input of OR gate U7.

In operation, the leading edge of the ISFC is delayed, differentiated and the resulting pulse is used to sample the condition of the SET WRITE STATUS line. If this is true, the following action takes place.
(1) The Write/Read mode flip-flop U41B is set.
(2) The NWRT waveform becomes low.
(3) The $-5 v$ driver (Q3) is turned on.
(4) The erase head is energized through Q4.
(5) The $C_{D}$ input of $U 3$ goes high. The polarity of the field from the erase and write heads under these conditions is such that tape will be erased in an IBMcompatible direction.

The ISFC command also enables the ramp generator, which causes tape to accelerate to the prescribed velocity. After a time (T1) determined by the required interrecord gap (IRG) displacement, the WRITE DATA (IWD) inputs together with the IWDS are supplied to the interface connector. Preamble, data block, and postamble are recorded.

IWD is received by interface receiver U1 and is strobed into flip-flop U3 at the trailing edge of IWDS. On the WRITE DATA lines (IWDP - IWD7), a one is a positive-going edge at data flux reversal time and a zero is a negative-going edge. The phase edge can be positive- or negative-going. Both outputs of flip-flop U3 are fed to head driver transistors Q1 and Q2, which cause current to flow in one half or the other of the center-tap head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes in direction in accordance with the input signal IWD.

At the completion of the postamble, ISFC goes false after the post-record delay time (T2). The ramp generator is disabled and the tape velocity decelerates to zero.

The IRG displacement consists of the following.
(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.
(2) The start distance: the distance traveled while tape is accelerating to the prescribed velocity.
(3) An additional distance determined by the prerecord time (T1), from the ISFC command going true to the time of the first IWDS and the post-record time (T2), from the end of the postamble to ISFC going false. (Time delays T1 and T2 are provided by the customer's controller.)

ISFC


2 VEL

3
3
L
BIT PATTERN
(INTERFACE)
IWDO-7
IWDO-7
(TYPICAL)

4 IWDS

(1) THIS DIRECTION OF CURRENT IS SUCH AS TO MAGNETIZE TAPE IN THE DIRECTION
OF THE IBG.

Figure 4-13. Data Recording Timing Diagram

### 4.3.4.3 Overwrite Operation (Model T8640A)

The Overwrite (IOVW) function allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced. This restriction is necessary since replacing a block of data with a block longer than the original could result in an IRG distance which is less than the minimum allowed, or in writing over the next record. If the new data is shorter than the existing block, errors could result since some unerased portion of the old data would remain.

Additionally, when write and erase currents are switched off abruptly there is a small area of tape which is influenced by the collapsing magnetic fields of the heads. This constitutes flux transients on the tape which appear as spurious signals when read back. The Overwrite feature of the transport has effectively eliminated this problem by turning the write current off slowly while tape is still in motion.

## NOTE

Refer to PERTEC Application Note, Editing Pre-Recorded Tapes, 6000/7000 Series Tape Transports [Document No. 70711] for control and timing restrictions associated with Overwrite.

To update a previously recorded record, the transport must be Selected, Ready, On-line, and have a Write Enable ring installed. Additionally, the IOVW signal from the controller must be true and the coincident with ISWS and ISFC.

Overwrite operation is terminated by the IWARS signal disabling the WRT PWR circuitry. This action causes the write current to ramp down to zero as the tape decelerates to rest. The transient pulse, generated when the write current is switched off, is spread over a longer distance on the tape and produces a negligible signal on replay.

### 4.3.4.4 Data Recording (Single-Stack Model T8660A)

Figure 4-13 is a timing diagram illustrating relationship of signals during data recording and should be referred to in conjunction with Figure 4-12. Assume that the transport is Selected, Ready, On-line, and has a Write Enable ring installed. The WRITE POWER control line will therefore be at +5 v , providing power for the head driver circuits.

When an ISFC is received, the MOTION signal generated on the Tape Control PCBA goes high, removing one input of OR gate U7 via U6.

In operation, the leading edge of the ISFC is delayed, differentiated and the resulting pulse is used to sample the condition of the SET WRITE STATUS line. If this is true, the following action takes place.
(1) The Write/Read mode flip-flop U41B is set.
(2) The NWRT waveform becomes low.
(3) The $-5 v$ driver (Q3) is turned on.
(4) The erase head is energized through Q4.
(5) The $C_{D}$ input of U3 goes high. The polarity of the field from the erase and write heads under these conditions is such that tape will be erased in an IBMcompatible direction.

The ISFC command also enables the ramp generator, which causes tape to accelerate to the prescribed velocity. After a time (T1) determined by the required interrecord gap (IRG) displacement, the WRITE DATA inputs together with the IWDS are supplied to the interface connector. Preamble, data block, and postamble are recorded.

IWD is received by interface receiver U1 and is strobed into flip-flop U3 at the trailing edge of IWDS. On the WRITE DATA lines (IWDP-IWD7), a one is a positive-going edge at data flux reversal time and a zero is a negative-going edge. The phase edge can be positive- or negative-going. Both outputs of flip-flop U3 are fed to head driver transistors Q1 and Q2, which causes current to flow in one half or the other of the center-tap head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction in accordance with the input signal IWD.

At the completion of the postamble, ISFC goes false after the post-record delay time (T2). The ramp generator is disabled and the tape velocity decelerates to zero.

The IRG displacement consists of the following.
(1) The stop distance: the distance traveled during the tape deceleration period to zero velocity.
(2) The start distance: the distance traveled while the tape is accelerating to the prescribed velocity.
(3) An additional distance determined by the prerecord time (T1), from the ISFC command going true to the time of the first IWDS and the post-record time (T2), from the end of the postamble to ISFC going false. (Time delays T1 and T2 are provided by the customer's controller.)

### 4.3.4.5 Overwrite Operation (Model T8660A)

The Overwrite function allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced. This restriction is necessary since replacing a block of data with a block longer than the original could result in an IRG distance which is less than the minimum allowed, or in writing over the next record. If the new data is shorter than the existing block, errors could result since some unerased portion of the old data would remain.

Additionally, when write and erase currents are switched off abruptly there is a small area of tape which is influenced by the collapsing magnetic fields of the heads. This constitutes flux transients on the tape which appear as spurious signals when read back. The Overwrite feature of the transport has effectively eliminated this problem by turning the write current off slowly while tape is still in motion.

## NOTE

Refer to PERTEC Application Note, Editing Pre-Recorded Tapes, 6000/7000 Series Tape Transports [Document No. 70711] for control and timing restrictions associated with Overwrite.

To update a previously recorded record, the transport must be Selected, Ready, On-line, and have a Write Enable ring installed. Additionally, the IOVW signal from the controller must be true and coincident with ISWS and ISFC.

Overwrite operation is terminated by the IWARS signal disabling the WRT PWR circuitry. This action causes the write current to ramp down to zero as the tape decelerates to rest. The transient pulse, generated when the write current is switched off, is spread over a longer distance on the tape and produces a negligible signal on replay.

### 4.3.4.6 Data Reproduction (Dual-Stack Model T8640A)

When an ISFC is received, the following occur.
(1) The MOTION signal generated on the Tape Control PCBA goes true so that NAND gate U4 (Figure 4-11) is enabled.
(2) The Forward ramp generator is enabled and the tape accelerates to the prescribed velocity.

Figure 4-14 illustrates typical PE read timing and waveforms and should be referred to in conjunction with Figure 4-11. Data signals from the magnetic head are fed by a shielded cable to the read amplifier.

The differentiated signal is fed to a Schmitt trigger which squares the signal and outputs it to line driver U4. The differentiated signal is also applied to the envelope detector which requires four successive characters greater than the threshold before its output goes high to enable the line driver U4. The output of the envelope detector goes false when the differentiated read signal envelope goes below the threshold for more than two successive characters.

When the transport is in the Read While Write mode, a threshold level of approximately 45 percent of the nominal peak output is generated regardless of the IRTH2 waveform levels. When the transport is in the Read mode and IRTH2 is high, the threshold level is approximately 15 percent of the nominal peak output.

The IRTH2 line, when low and the transport is in the Read mode, will generate a read threshold of approximately 7.5 percent of the nominal peak output to enable the user to recover very low amplitude data. Operation at this threshold is recommended only after an attempt has been made to read the data at the normal read threshold level.

### 4.3.4.7 Data Reproduction (Single-Stack Model T8660A)

When an ISFC is received, the following occur.
(1) The MOTION signal generated on the Tape Control PCBA goes true so that NAND gate U4 (Figure 4-12) is enabled.
(2) The Forward ramp generator is enabled and the tape accelerates to the prescribed velocity.

Figure 4-14 illustrates typical PE read timing and waveforms, and should be referred to in conjunction with Figure 4-12. Data signals from the magnetic head are fed by a shielded cable to the read amplifier.

The differentiated signal is fed to a Schmitt trigger which squares the signal and outputs it to line driver U4. The differentiated signal is also applied to the envelope detector which requires four successive characters greater than the threshold before its output goes high to enable line driver U4. The output of the envelope detector goes false when the differentiated read signal envelope goes below the threshold for more than two successive characters.

When the transport is in the Read mode, and both IRTH1 and IRTH2 waveforms are high, a threshold level of approximately 15 percent of nominal peak output is generated. During the Write mode, IRTH1 is low. When IRTH1 is low, the threshold level is 45 percent of the nominal peak output regardless of the IRTH2 level.


NOTES:

1. TRANSPORT MUST BE SELECTED, READY, AND ON-LINE AND GATED WITH SFC OR SRC
2. PREAMBLE IS SHOWN SHORTENED TO SIMPLIFY DRAWING. PREAMBLE CONSISTS OF 40 ZEROS FOLLOWED BY ONE I.
3. POSTAMBLE NOT SHOWN. POSTAMBLE CONSISTS OF ONE 1 FOLLOWED BY 40 ZEROES.
flux Polarity of interblock gap

Figure 4-14. Data Reproduction Timing Diagram

When the IRTH2 line is low, the IRTH1 line is high, and the transport is in the Read mode, a read threshold of approximately 7.5 percent of the nominal peak output is generated to enable the user to recover very low amplitude data. Operation at this threshold is recommended only after an attempt has been made to read the data at the normal threshold level, i.e., when both IRTH1 and IRTH2 are high.

### 4.3.5 TAPE CONTROL SYSTEM

The tape control system consists of the circuits necessary to control tape motion. This includes manual controls, interlocks, and logic. The operation of the tape control system can best be described by detailing the functions in the following order.
(1) Bring-to-Load-Point sequence
(2) Forward/Reverse tape motion commands
(3) Rewind sequence
(4) Unloading of tape.

Figure $4-15^{*}$ is a functional logic diagram of the tape control system and should be referred to for the following discussion; in most cases component labels are compatible with those designated on Tape Control Schematic No. 102333.

Cleanup flip-flops, which eliminate the problems of switch contact bounce, are associated with four manual control switches: U5A, U5C with LOAD; U19B, U19C with ON LINE; U6B, U6E with REWIND; and, U4B, U4E with RESET. Relay K1 has four changeover contacts, three of which (K1A, K1B, and K1C) are used to connect the reel and capstan servo motors, while the fourth (K1D) is used in conjunction with the tension arm limit switch as a system interlock. The tension arm limit switch is operated by a cam on the supply reel tension arm and remains closed when the cam is within its normal operating region. The limit switch opens at both extremes of the arm travel so that protection against over-tension as well as under-tension conditions is provided.

### 4.3.5.1 Bring-to-Load-Point Sequence

The system will be described by considering the sequence required to bring the tape to the BOT (Load Point) when the arms are in the tape threading position and there is no tape in the tape path. Figure $4-16$ shows the waveforms which are generated during this sequence.

When power is initially applied (Plot 1), the Interlock and Arm-Up-Stop switches will be open. INTLK (U13A) and RST (U13B) will be low. Therefore, RST resets control flip-flops RW1 (U17B), RW2 (U17A), RW3 (U23A), and LOAD (U29A). The low levels of RW1 and LOAD made NBUSY (U31B) high. Thus, flip-flop FLR (U37A, U37D) is reset. RAC (across R254, C63-C65) is initially low and resets flip-flop UNL (U23B). RAC also resets flip-flops U21A and U21B via gates U9B and U9A. RAC goes high after the delay of the RC network (Plot 2).

When a reel of tape is mounted and the tape path is closed, TIP (U12A) goes high (Plot 3). With NRAC (U16E) and NTIP (U18B) low CLR (U16F) becomes high (Plot 4).

Depressing the LOAD switch/indicator for the first time momentarily sets the LOAD control cleanup flip-flop (U5A, U5C) (Plot 5). All inputs to gate U9C become high and flip-flop U21B is toggled. The Q output of U21B, ANDed with the high output of the 0.75 second single-shot causes the output of U47A to go low and transistors Q15 and Q16 to

[^0]

Figure 4-16. Bring-to-Load-Point Sequence Waveforms
turn on (Plot 7). Therefore, the arm actuator motor begins to turn and the tension arms begin to move (supply tension arm moves down; takeup tension arm moves up). The Arm-Up-Stop switch returns to its NC condition.

When the tension arms reach the end of their operating range, the normally open (NO) contact of the arm down-stop switch closes. This causes the NSTAC to go low and the STAC (Plot 10) to go high. NSTAC going low activates the 0.75 second single-shot causing its output to go low, inhibiting U7B. When U7B output goes high, U47A, Q15, and Q16 are deactivated and the arm actuator motor stops.

STAC (Plot 10) going high causes the output of U8B to go low. The interlock relay driver is activated and relay K1 latches, connecting the transport motors to their respective amplifiers. Tape is tensioned, the tension arm interlock switch closes, and after a time delay determined by R40, R41 and C14, INTLK goes high (Plot 9). INTLK is inverted by U20C and the low level at the output holds the interlock relay driver U51A activated. Then, 0.75 second after tensioning, the single-shot output again goes to its stable (high) state (Plot 8) and resets flip-flop U21B via U3D, U9A and U15B.

With the inputs to INTLK (U13E) low and NSTAC (U13C) low, RST goes high (Plot 11).
Depressing the LOAD switch/indicator for the second time sets the LOAD control cleanup flip-flop (U5A, U5C) again. The output of U10B goes low, toggles flip-flop LOAD (U29A) and sets it. This is true because RST at the reset input of U29A is high at this point in the sequence.

If the LOAD switch/indicator is originally depressed twice, the supply arm again moves down, the takeup arm moves up, tape is tensioned, and the LOAD flip-flop is set. In this case, flip-flop U21A sets when the LOAD switch/indicator is depressed for the second time. After the Arm-Down-Stop switch NO contact is closed and the 0.75 second single-shot output returns to its stable (high) state, flip-flop U21B is reset and its $\overline{\mathrm{Q}}$ output goes high. This causes a negative-going transition at the output of U10C which toggles and sets U29A via delay network R56 and C20.

If power is applied to a transport which has a reel of tape mounted and threaded, and the tension arms are in the operating position, depressing the LOAD switch/indicator for the first time causes the interlock relay drive to be activated and tape to be tensioned. In this case the STAC output is high, since the Arm-Down-Stop switch NC contact is open, and enables one input of U14A. When tape is in the tape path, the TIP input to U14A is also high. At the moment the LOAD switch/indicator is depressed, all inputs to U14A become high. The negative-going output of U14A activates the interlock relay driver U51A. Once the interlock is made, RST at the reset input of flip-flop U29A becomes high; thus the LOAD flip-flop is enabled to respond to a toggle from the LOAD switch/indicator. The LOAD flip-flop will set when the switch is depressed for the second time.

At this point, the output of the LOAD flip-flop is high and flip-flop RW1 (U17B) is still reset (RW1 low). Therefore, NBUSY (U31B) goes low (Plot 13) and sets flip-flop FLR (Plot 14). The low level of NFLR at the input of U10B inhibits the possibility of further manual LOAD commands.

Should the tension arms move outside of their operating regions, the limit or interlock switch opens, INTLK and RST become low. Thus, flip-flops FLR and LOAD are reset and the interlock relay driver is deactivated. Relay K1 deenergizes and power is disconnected from the motors.

When LOAD becomes high, the Forward ramp generator is enabled by the output of NAND gate U35A. NRWR is high at the input of U35A because it is the output of U38C, one input of which is low (RW1). NBOTD is high at the input of U35A because when power is turned ON and transients have died out, the output of the BOT single-shot will be high. Therefore, when LOAD goes high, the output of U35A goes low and enables the Forward ramp generator. Tape is then accelerated to the specified velocity (Plot 15) and continues to move until either the BOT tab is detected by the BOT sensor or the RESET control switch is depressed. If BOT is detected, BOT goes high (Plot 16) and triggers the single-shot. NBOTD goes low and remains low for the duration of the single-shot period, approximately 0.5 second (Plot 17). The low level of NBOTD sets U35A high and the Forward ramp generator is disabled. The tape decelerates and stops with the BOT tab under the photosensor. With NRWR and LOAD high, when BOT goes high, RST (U7A) goes low, resetting flip-flop LOAD (U29A). This in turn sets NBUSY (U31B) and, after some delay, RST (U7A) high. With NBUSY, FLR, and BOT high, NLDP (U12C) goes low (Plot 18) enabling the lamp driver circuit of the LOAD switch/indicator, illuminating the lamp. The delay between the LOAD waveform and NAND gate U7A ensures that RST remains low for an appropriate length of time. After NBOTD returns to high, the ramp generator remains disabled by virtue of the low level of LOAD. Also, all inputs to U30A go high, thus NRDY goes low (Plot 19). If the RESET switch is depressed, cleanup flip-flop U4B, U4E is reset and RST (U13B) goes low. The LOAD flip-flop (U29A) is reset causing NBUSY and U35A to go high. The Forward ramp generator is disabled and tape comes to a stop. After the RESET switch is released, RST goes high and with NBOTD, FLR high, NRDY goes low.

### 4.3.5.2 Forward/Reverse Tape Motion - Manual Commands

Referring to Figure 4-15, if the On-line flip-flop (U27B) is reset and NRDY (U30A) is low, then RUN (U31C) is high and the transport will accept motion (Forward/Reverse) commands given via the Maintenance switch located on the Tape Control PCBA. If the On-line flip-flop (U27B) is set, then NONLINE is low, the lamp driver circuit of the ON LINE switch/indicator is enabled and the lamp is illuminated. Therefore, when either the RESET or ON LINE switch/indicator is depressed, the lamp will be extinguished indicating that the On-line flip-flop is reset.

When the Maintenance switch is set to pull tape in the forward direction and neither BOT nor EOT tabs are encountered, all inputs to NAND gate U35B are high and the Forward ramp generator is enabled. Tape will advance at the specified velocity. When the EOT tab is encountered, NEOT at the input of U35B goes low and tape motion ceases. When the BOT tab is encountered (this is not a normal situation), tape will come to a stop for approximately 0.5 second and then continue at the specified velocity (NBOTD, U18D, goes low setting NRDY, U30A, high and RUN, U31C, low for approximately 0.5 second).

When the Maintenance switch is set to pull tape in the reverse direction and the BOT tab is not encountered, all inputs to NAND gate U35C are high and the Reverse ramp generator is enabled. Tape will move in reverse at the specified speed. When the BOT tab is encountered, NBOT at the input of U35C goes low and tape motion ceases.

If the RESET switch is depressed while tape is in motion, NRDY (U30A) goes high, RUN goes low, and tape motion ceases. When the switch is released, RUN goes high and tape motion is resumed.

### 4.3.5.3 Forward/Reverse Tape Motion - External Commands

Referring to Figure $4-15$, if SRO output of gate U34A is high the transport will accept motion commands received via interface lines ISFC (U20A) and ISRC (U20B). SRO will be high when:
(1) NRDY at the input of U34D is low.
(2) NONLINE at the input of U34B is low, i.e., On-line flip-flop U27B is set.
(3) SLT at the input of U34C is high, i.e., interface line ISLT (U40B) is low.

When interface line ISFC (U20A) goes low and the BOT tab is not encountered, the output of U28A goes low and the Forward ramp generator is enabled. The tape advances at the specified velocity. When the BOT tab is encountered, NRDY (U3OA) will go high for approximately 0.5 second; during the time interval SRO will go low and tape motion will cease.

When interface line ISRC (U20B) goes low and the BOT tab is not encountered, U28D goes low and the Reverse ramp generator is enabled. Tape moves in reverse at the specified velocity. When the BOT tab is encountered, BOT at the input of U20E will go high and tape motion will cease. NRDY will also go high for approximately 0.5 second.

If the RESET switch is depressed during tape motion from external commands, the On-line flip-flop is reset and remains reset after the switch is released. SRO goes low and tape motion ceases until the On-line flip-flop is set again.

The following conditions must be met in order for the On-line flip-flop (U27B) to set in response to a toggle input.
(1) RESET switch should not be depressed (NSRST at the input of U19F should be low).
(2) Interface line IOFFC (U26A) should be high.
(3) Tape must not be unloading (UNL at the input of U19E should be low).

When the preceding conditions are met, the following will enable the transport to be placed in the On-line mode.
(1) Tape is tensioned (INTLK at the input of U26C is high) and the FLR flip-flop is set (LOAD switch/indicator has been depressed twice). Depressing the ON LINE switch/indicator will place the transport On-line.
(2) Tape is tensioned [LOAD switch has been depressed once and jumper W12 is removed (optional)]. Depressing the ON LINE switch/indicator will place the transport On-line.
(3) Tape is not tensioned, jumpers W12 and W18 are removed, and W19 is inserted, or jumpers W18 and W19 are inserted and W12 is removed and either the ISLT interface line is low or W17 is inserted (optional). When the first negative-going pulse of 1.0 second minimum width at interface line ILOL (U8A) is received, the output of U8C goes low and enables interlock relay driver U51B. Tape will now be tensioned and after a 1.0 second delay, when a second negative-going pulse is received, the output of U14B will go low, setting the On-line flip-flop.

NOTE
If tape is already tensioned, only one pulse must be received in order to set the flip-flop.

### 4.3.5.4 Rewind Sequence

The Rewind sequence can be initiated when the tape is not at Load Point, i.e., when BOT is low. BOT low enables gates U11A, U11B and disables gate U22A. Figure 4-17 shows the waveforms that occur during the operation. The transport will go into the Rewind mode from either a remote or a manual command. If the On-line flip-flop U27B is reset and the REWIND control switch/indcator is depressed (Plot 1), all inputs to NAND gate U11A become high (NUNL can go low only at Load Point). Or, if SRO (U34A) is high and a negative-going pulse appears at interface line IRWC (U6D, Plot 2), all inputs to NAND gate U11B go high. In either case, flip-flop RW1 (U17B) is set (Plot 3) enabling the lamp driver circuit of the REWIND switch/indicator, the lamp is illuminated and the Rewind sequence begins.

NAND gate U38C is enabled by the Q output of flip-flop RW1 and the $\bar{Q}$ output of flip-flop RW3 (U23A), and RW3 is reset at this time. NRWR at the output of U38C goes low (Plot 10). The Q output of flip-flop RW1 also triggers the 0.3 second single-shot and enables NAND gate U38A after the delay of the single-shot. The output of U38A, NRWRD, goes low (Plot 11) and the Rewind ramp generator is enabled. Tape accelerates to a reverse velocity of 200 ips (nominal) in approximately 1.0 second (Plot 14).

Additionally, when flip-flop RW1 is set, NBUSY (U31B) goes low and sets NRDY high. Thus, the output of gate U34D, RO, goes low, disables NAND gate U34C, and causes the SRO waveform to go low (Plot 13) for the situation where the REWIND sequence was initiated under remote command (ISLT was low).

When the BOT tab is detected (Plot 4) flip-flop RW2 (U17A) is set (Plot 6) and the 0.5 second single-shot NBOTD (U18D) is triggered (Plot 8) on the leading edge of the BOT waveform while flip-flop RW3 (U23A) is set on the trailing edge (Plot 7). The Q output of flip-flop RW3, NRW3, goes low, disabling NAND gates U38A and U38C. NRWR and NRWRD go high and the Rewind ramp generator is disabled. The tape decelerates to a stop.

At the end of the 0.5 second delay, the trailing edge of the NBOTD (U18D) waveform is differentiated by differentiator $\delta 2$ (U18E, U24D) generating a positive-going BOTDP pulse (Plot 9). Since the Q output of flip-flop RW3 is high at this time, flip-flop LOAD (U29A) is set (Plot 12) via gate U10A and the delay network. This enables the Forward ramp generator, and the Load sequence is initiated.

As the BOT tab overshoots the photosensor and returns, it is detected for the second time and triggers the 0.5 second single-shot NBOTD again. The Forward ramp generator is disabled and tape comes to a stop. Since LOAD was set high, NAND gate U7A is enabled and its output, RST, goes low, resetting the LOAD, RW1, RW2, and RW3 flip-flops. At the end of the 0.5 second delay, NBOTD waveform goes high setting NRDY (U3OA) low. Since the other inputs are high at this time, gate U34C is enabled and SRO goes high (if the sequence was initiated by remote command).

If at any point during the rewind sequence the RESET switch is depressed, RST (U13B) goes low and resets LOAD, RW1, RW2, and RW3 flip-flops. NRWRD (U38A), NRDY (U30A) go high and SRO (U34A), RUN (U31C) go low. Hence, either the Rewind ramp generator or Forward ramp generator is deactivated depending upon the time in the rewind sequence when the RESET switch was depressed. Tape comes to a stop. If the sequence was initiated under remote control, SRO goes high after the switch is released.


Figure 4-17. Rewind Sequence Waveforms

### 4.3.5.5 Unloading of Tape

If tape is at Load Point (BOT high) and the On-line flip-flop is reset, then in response to a manual REWIND command, all inputs to gate U22A become high and flip-flop UNL (U23B) is set. The Q output generates the AOS signal (U16D) which is used to position the tension arms close to the stops. NUNL also enables interlock relay driver U51A, the Rewind ramp generator, and switches the generator output to approximately one-tenth of the normal voltage. Thus, the tape moves in reverse at 20 ips (nominal).

When tape tension is lost, INTLK (U13A) goes low. As tape clears the head plate area, NTIP at the input of U16A goes high resetting the UNL flip-flop (U23B). Hence, the interlock relay driver and Rewind ramp generator are disabled.

With the Arm-Up-Stop switch NC contacts closed, the tape path cleared, the Interlock switch open, and flip-flop U21B reset, all inputs to gate U30B become high. The low output of U30B activates U47A, causing Q15 and Q16 to turn on. The arm actuator motor begins to move and positions the tension arms in the tape threading position. The Arm-Up-Stop switch NO contacts close causing the output of U30B to go high. Thus, U47A is deactivated and transistors Q15, Q16 are turned off. The arm actuator motor stops and the unloading cycle terminates.


## SECTION V <br> PRINTED CIRCUIT BOARDS THEORY OF OPERATION

### 5.1 INTRODUCTION

This section contains the theory of operation of the printed circuit boards used in the T8640A and T8660A Tape Transports. The schematics and assembly drawings for the PCBAs are at the end of Section VII.

A better understanding of the logic used in the tape transport can be gained when the operation of the J-K flip-flop is fully understood. The following paragraphs provide a summary of the operation of the $852 \mathrm{~J}-\mathrm{K}$ flip-flop, a type most commonly used in the system.

This flip-flop operates on a master-slave principle. A logic diagram of the flip-flop is shown in Figure 5-1. The flip-flop is designed so the threshold voltage of AND gates 101 and 102 is higher than the threshold voltage of AND gates 103 and 104. Since operation depends exclusively on voltage levels, any waveform of the proper voltage level can trigger the J-K flip-flop.

Assume that the trigger voltage is initially low. As the trigger voltage goes high, AND gates 103 and 104 are disabled. Subsequently, AND gates 101 and 102 are enabled by the trigger pulse, the J and K inputs, and the information previously stored at the output of the slave unit.

The $J$ and $K$ input information at this time is transferred to the input of the master unit. As the trigger voltage goes low, AND gates 101 and 102 are disabled. AND gates 103 and 104 are then enabled and the information stored in the master unit is transferred to the output of the slave unit.


Figure 5-1. Master-Slave Flip-Flop, Simplified Logic Diagram

### 5.2 DATA F PCBA (T8640A)

The following is a description of the Data F PCBA (refer to Schematic 101345 and Assembly 101346).

The Data F PCBA is approximately 419.1 mm ( 16.5 inches) long with edge connectors at each end along one edge. Figure 5-2 illustrates the placement of each connector and test point. J102 and J103 are the interface connectors and are slotted to mate with keys in the mating plugs. Three additional connectors are used on the Data F; J8 is for the power and control signals from the Tape Control PCBA; J1 and J2 are for the write and read head cables. (Table 7-6 lists all PCBA interconnections.)

### 5.2.1 CIRCUIT DESCRIPTION

The board operation is described with reference to Circuit 100 which is identical to Circuits 200 through 900. All interface signals relevant to writing data (nine Write Data signals, IWDO—IWD7, and Write Data Strobe, IWDS) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to Circuit 100, the Write Data Parity (IWDP) data line is terminated by resistors R101, R102, and inverter U6-E. IWDP and its complement are applied to the J and K inputs of write buffer flip-flop U8-A. At the trailing edge of IWDS (TP3), which is applied to the toggle input of U8-A from power gate U10-A, flip-flop U8-A copies in the inverse of IWDP.

The outputs of the write buffer flip-flop drive write amplifier transistors Q101 and Q102, whose emitters are taken to +5 v when the WRT POWER line (J8-4) is high. The transistor connected to the low (approximately 0 v ) output of the flip-flop will conduct and a current will flow in the associated half of the head winding. The center taps of all the windings are connected to the collector of Q3 which goes to -5 v when the NWRT signal is low (i.e., the transport is in the Write mode). When the WRT POWER line is low (approximately 0 v ) or the NWRT signal is high, writing is inhibited because the write amplifier transistors cannot turn on. Similarly, the erase current supplied by transistor Q1 is inhibited when the WRT POWER line is low or the NWRT signal is high. In operation, the write current is defined by resistors R107 and R108. R109 is the associated damping resistor.

To improve the writing characteristics at 3200 frpi, write compensation capacitors C101 and C102 are used to cause an overshoot of current on each leading edge.

The head windings are phased so that the output of the write buffer flip-flops, when reset, cause current to flow in the standard erase direction. The write buffer register is held reset unless the transport is in the Write mode (NWRT is low) and the tape is moving (MOTION, J8-6, is high).

The IWARS signal is received by resistors R22 and R23 but is not used on the Data PCBA. A jumper from J102-C (Data PCBA) to J101-15 (Tape Control PCBA) routes IWARS to the Overwrite circuitry on the Tape Control PCBA. IWARS is issued at the end of writing the postamble and is used in conjunction with IOVW to reset the WRT PWR ENABLE line on the Tape Control PCBA. This turns off the write and erase current so that the adjacent record will not be erased during an Overwrite operation.

When reading data from tape, signals from the read head are fed via connector J2 to the read amplifier (U16-B) which is one half of a dual operational amplifier IC. The amplifier output is maintained close to $0 v$ in the absence of an input signal by the feedback path of resistors R114 and R116. The cutoff frequency of the amplifier is determined by C104 and R114. The operating gain of the amplifier is defined by resistor network R114, R116, and R117. R117 is a variable resistor used in the initial setup to set the differentiator output peak-to-peak amplitude.


Figure 5-2. Data F PCBA Test Point and Connector Placement

Figure 5-3 illustrates typical read signal and timing relationships and should be referred to in the following discussion.

Amplifier U21-B is used as a differentiator so that a peak in the output voltage of U16-B (TP103) is changed to a zero crossing at the output of amplifier U21-B (TP104). The gain of U21-B is determined by R118, R119, and C105. Since the capacitive reactance of C105 decreases as frequency increases, the gain of U21-B increases with frequency until cut off by C106 and R119. Therefore, the amplitude of the envelope at TP104 is essentially independent of the data pattern. R117 should be adjusted so that the amplitude at TP104 is 4 v peak-to-peak.

The differentiated signal is fed to U30-A, a Schmitt Trigger (an amplifier with a small amount of positive feedback) which yields a square signal (TP105). The read data is then applied to the power NAND gate U35-A.

The output of the differentiator ( $\mathrm{U} 21-\mathrm{B}$ ) is also fed to the input of the Envelope Detector (U30-B). The envelope detector compares the positive halves of the differentiator signal (TP104) on Pin 9 of U30-B against the divided threshold level on Pin 8 of U30-B. The threshold level, when the transport is in the Write mode, is 45 percent of the nominal peak output and is determined by R18 and R19. Q4 and Q5 are cut off during a Write operation. During a normal Read operation, Q4 is conducting and the threshold is approximately 15 percent of the nominal peak output. If IRTH2 is low during a Read operation, Q5 also conducts and the threshold drops to 7.5 percent of the nominal peak output.

During the portion of the positive peak of the differentiated signal, the output at Pin 12 of U30-B goes to approximately - 2 v ; this also pulls C111 to approximately -1.3 v through CR104 and causes Q103 to cut off. When the peak falls below the threshold, the output of U30-B goes positive and C111 is charged by R131 unitl Q103 conducts. The charge time for C111 is $11 / 2$ to 2 times the period for a single character. While Q103 is cut off, C109 is charging through R132. When the voltage on C109 reaches approximately +2 v , emitter


Figure 5-3. Timing and Signal Relationships, One Channel Read Electronics
follower Q104 enables power NAND gate U35-A. Read data from U30-A is presented to the interface line when U35-A is enabled by the outputs of U30-B, and the MOTION signal being high. The charge time for C 109 is about four character times. If no positive peaks exceed the threshold for $11 / 2$ to 2 consecutive character periods, C 111 will charge to +0.7 v and cause Q103 to conduct. C109 will discharge, until Q104 turns off, and disables U35-A. Since C109 requires four character periods to enable U35-A, there must have been four continuous peaks of the differentiated signal before U35-A was enabled.

### 5.3 DATA G PCBA (T8660A)

The following is a description of the Data G PCBA (refer to Schematic 101375 and Assembly 101376).

The Data G PCBA is approximately 419.1 mm ( 16.5 inches) long with edge connectors at each end along one edge. Figure 5-4 illustrates the placement of each connector and test point. J102 and J013 are the interface connectors and are slotted to mate with keys in the mating plugs. Two additional connectors are used on the Data G; J8 is for the power and control signals from the Tape Control PCBA; J 1 is for the read/write head cable.

### 5.3.1 CIRCUIT DESCRIPTION

The board operation is described with reference to Circuit 100, which is identical to Circuits 200 through 900 . All interface signals relevant to writing data (nine Write Data signals, IWD0-IWD7, and Write Data Strobe, IWDS) enter via J102 and are terminated by a resistor combination and an IC inverter.

Referring to Circuit 100, the Write Data Parity (IWDP) data line is terminated by resistors R101, R102, and inverter U6-E. IWDP and its complement are applied to the J and K inputs of write buffer flip-flop U8-A. At the trailing edge of IWDS (TP3), which is applied to the toggle input of U8-A from power gate U10-A, flip-flop U8-A copies in the inverse of IWDP.

The outputs of the write buffer flip-flop drive write amplifier transistors Q101 and Q102, whose emitters are taken to +5 v when the WRT POWER line (J8-4) is high. The transistor connected to the low (approximately Ov ) output of the flip-flop will conduct and a current will flow in the associated half of the head winding. The center taps of all the windings are connected to the collector of Q3 which goes to -5v when the NWRT signal is low (i.e., the transport is in the Write mode). When the WRT POWER line is low (approximately Ov ) or the NWRT signal is high, writing is inhibited because the write amplifier transistors cannot conduct. Similarly, the erase current supplied by transistor Q1 is inhibited when the WRT POWER line is low or the NWRT signal is high. In operation, the write current is defined by resistors R107 and R108.

To improve the writing characteristics at 3200 frpi, the write compensation capacitors C101 and C102 are used to cause an overshoot of current on each leading edge.

The head windings are phased so that the output of the write buffer flip-flops, when reset, cause current to flow in the standard erase direction. The write buffer register is held reset unless the transport is in the Write mode (NWRT is low) and tape is moving (MOTION, J8-6, is high).

The IWARS signal is received by resistors R25 and R26 but is not used on the Data PCBA. A jumper from J102-C (Data PCBA) to J101-15 (Tape Control PCBA) routes IWARS to the Overwrite circuitry on the Tape Control PCBA. IWARS is issued at the end of writing the postamble and is used in conjunction with IOVW to reset the WRT flip-flop on the Tape Control PCBA. This turns off the write and erase current so that the adjacent record will not be erased during an Overwrite operation.


Figure 5-4. Data G PCBA Test Point and Connector Placement

When reading data from tape, signals from the read head are fed via connector J1 to the read amplifier (U16-B) which is one half of a dual operational amplifier IC. The amplifier output is maintained close to 0 v in the absence of an input signal by the feedback path of resistors R114 and R116. The cutoff frequency of the amplifier is determined by C104 and R114. The operating gain of the amplifier is defined by resistor network R114, R116, and R117. R117 is a variable resistor used in the initial setup to set the differentiator output peak-to-peak amplitude.

Figure 5-5 illustrates typical read signal and timing relationships and should be referred to in the following discussion.

Amplifier U21-B is used as a differentiator so that a peak in the output voltage of U16-B (TP103) is changed to a zero crossing at the output of amplifier U21-B (TP104). The gain of U21-B is determined by R118, R119, and C105. Since the capacitive reactance of C105 decreases as frequency increases, the gain of U21-B increases with frequency until cut off by C106 and R119. Therefore, the amplitude of the envelope at TP104 is essentially independent of the data pattern. R117 should be adjusted so that the amplitude at TP104 is 4v peak-to-peak.

The differentiated signal is fed to U30-A, a Schmitt trigger (an amplifier with a small amount of positive feedback) which yields a square signal (TP105). The read data is then applied to the power NAND gate U35-A.

The output of the differentiator (U21-B) is also fed to the input of the Envelope Detector ( $\mathrm{U} 30-\mathrm{B}$ ). The envelope detector compares the positive peaks of the differentiator signal (TP104) on Pin 9 of U30-B against the voltage-divided threshold level on Pin 8 of U30-B. During a normal Read operation, Q4 is conducting and the threshold is approximately 15 percent of the nominal peak output.


Figure 5-5. Timing and Signal Relationships, One Channel Read Electronics

If IRTH2 is low during a Read operation, Q5 also conducts and the threshold drops to approximately 7.5 percent of the nominal peak output. If IRTH1 is low, the threshold is 45 percent of the nominal peak output regardless of the condition of IRTH2.

During the portion of the positive peak of the differentiated signal, the output at Pin 12 of U30-B goes to approximately - 4 v ; this also pulls C111 to approximately -3 v through CR104 and causes Q103 to cut off. When the peak falls below the threshold, the output of U30-B goes positive and C111 is charged by R131 until Q103 conducts. The charge time for C111 is approximately $11 / 2$ to 2 times the period for a single character. While Q103 is cut off, C109 is charging through R132. When the voltage on C109 reaches approximately -2 v , emitter follower Q104 enables power NAND gate U35-A. Read data from U30-A is presented to the interface line when U35-A is enabled by the outputs of U30-B, and the MOTION signal becomes high. The charge time for C109 is about four character times. If no positive peaks exceed the threshold for $11 / 2$ to 2 consecutive character periods, C111 will charge to +0.7 v and cause Q103 to conduct. C109 will discharge, until Q104 turns off, and disables U35-A. Since C109 requires four character periods to enable U35-A, there must have been four continuous peaks of the differentiated signal before U35-A was enabled.

### 5.4 TAPE CONTROL J PCBA

The following is a description of the Tape Control J PCBA (refer to Schematic No. 102333 and Assembly No. 102334).

The Tape Control J PCBA is approximately 419.1 mm ( 16.5 inches) long and contains the tape control system, reel servo amplifiers, capstan servo amplifier, regulators, EOT/BOT amplifier, overwrite system, and necessary signals and switch electronics. Figure 5-6 illustrates the placement of the test points and connectors.

The power transistors associated with the circuits on this board are mounted on an external heatsink, illustrated in Figure 5-7, which is part of the power supply and is attached to the transport rear deck. Electrical connection between the Tape Control PCBA and the transistors is accomplished via jumper cables.

Connectors, located with respect to their associated circuitry, are used to connect all deck-mounted assemblies to the board, e.g., power supply, motors, tension arm sensors, photosensors, write lockout assembly, tension arm limit switch, EOT/BOT sensors, switch/indicators, as well as the interface lines and the Data PCBA. (Table 7-6 lists all PCBA interconnections.)

### 5.4.1 CIRCUIT DESCRIPTION

The Tape Control PCBA consists of seven functionally distinct sections which are described separately in the following paragraphs.
(1) Tape control system
(2) Reel servo amplifiers
(3) Capstan servo amplifier
(4) Regulated power supply
(5) EOT/BOT amplifier
(6) Overwrite system
(7) Status and control signals.


Figure 5-6. Tape Control J PCBA Test Point and Connector Placement


Figure 5-7. Heatsink Assembly

### 5.4.1.1 Tape Control System Circuit Description

A description of the logic sequences employed in the Tape Control System is detailed in Paragraph 4.3.5. The following paragraphs explain the operation of the Forward, Reverse, and Rewind ramp generators.

The Forward and Reverse ramp generator converts the digital signals to analog levels with controlled transition times, which are the inputs to the capstan servo. The ISFC, or ISRC, is fed via transistors Q19, or Q20, to the operational amplifier circuits (U48, U49) whose output levels are determined by the +5 v and -5 v lines, and the ratio of R82 to R74, R277 and R79, respectively. The circuit rise and fall times are determined by the +5 v and -5 v lines and R87, R88, R89, R90, and C24. Tape speed is a function of the current entering the capstan servo circuit; therefore, the proper current for the selected speed is provided by a voltage divider R94, R95, R96, and R97 and one of the series resistors R98, R99 at the output of U49.

Field Effect Transistor (FET) Q22 is used as a switching device to select one of the two specified speeds on dual speed models. Q21 selects the appropriate ramp times for the two speeds. Bias for the gates of Q21 and Q22 is provided by a polarity reversing network consisting of Q23 and Q24 which is controlled by the HIGH SPEED signal from the speed control circuit at the base of transistor Q23.

The NRWRD command activates the Rewind ramp generator which includes transistors Q25, Q26. The rewind speed is determined by the -5 v line to which transistor Q26 saturates when a rewind to BOT is in progress. Rewind from BOT (unloading of tape) is accomplished in the same manner except that Q27 is saturated by NUNL going low, thus decreasing the available driving voltage to the capstan drive amplifier.

The rise and fall times of the Rewind ramp are determined by resistors R118 and R119 in conjunction with capacitors C30 and C31.

### 5.4.1.2 Reel Servo Amplifiers Circuit Description

Two dc linear amplifiers drive the supply and takeup reel motors (refer to Schematic 102333). Relay K1 connects these amplifiers to the motors. When K1 is deenergized, contacts 5 and 11 connect the two reel motors to ground (supply side directly, takeup side via a resistor). This provides a dynamic braking effect when interlock is lost due to power failure, tape breaking or reaching the end of the tape leader.

Referring to the takeup reel amplifier circuit, the input (C36, C37, R158, R162) and feedback (C39, C40, R166, R167) circuits of the operational amplifier stage U50 provide lead-lag phase compensation. The dc gain of the amplifier is given by the ratio R166/(R158 + R162). Current limiting is provided by amplifying the voltage developed by the motor current across R183 and applying it in proper phase to the input of U50. Diodes CR34 and CR35 ensure that current limiting is not initiated at low levels. The offset voltage from the output of U44 provides for the 5.6 -inch swing of the takeup tension arm; the swing is adjusted by potentiometer R157. The offset voltage from potentiometer R159 adjusts the arm center position. Takeup reel power transistors Q42 and Q43 are located on the large vertical heatsink as shown in Figure 5-7.

The supply reel amplifier circuit is identical to the takeup reel circuit in all respects except for the offset voltage which provides for the 5.6 -inch swing of the supply tension arm. This voltage comes from the output of U43 and furnishes the necessary phase reversals for the supply reel servo. Supply reel power transistors Q48 and Q49 are located on the large vertical heatsink as shown in Figure 5-7.

In the Rewind Mode NRWRD (U38A) goes low and activates Rewind relay driver U51. Relay K 2 is energized and connects the return leads of the takeup and supply reel motors to +18 v and -18 v , respectively; it also connects the negative and positive inputs of the respective amplifiers to the -18 v and +18 v . This action allows the amplifiers to supply sufficient output voltage to enable the reel servos to follow tape speeds of 200 ips . Also, offset voltages being zero, the tension arms move only approximately 0.25 -inch.

After the BOT tab is detected, NRWRD goes high at the trailing edge of the BOT pulse; it deactivates K2 relay driver U51 and triggers single-shot U31, Q9, and associated circuitry. Transistors Q50, Q51, Q41, and Q42 turn on for the duration of the on-state condition of the single-shot. This raises the reel servo amplifier current limits and provides for the large deceleration required to bring the reels to a rapid halt.

In the Rewind-at-BOT mode (unloading of tape) AOS high (U16D) introduces 2-inch offsets in the tension arms, as the reels continue to rotate and the tape is completely rewound on the supply reel. When tension is lost, the arms move down a distance and impact on the stops. The ULOS offsets are then necessary to reduce the reel motor speed.

Diodes CR36, CR37, CR42, and CR43 prevent the contacts of relay K1 from arcing when they are opened; diodes CR38, CR39, CR44, and CR45 protect the contacts of relay K2.

### 5.4.1.3 Capstan Servo Amplifier Circuit Description

Relay K1 connects the capstan servo amplifier to the capstan motor (refer to Schematic 102333). The amplifier uses operational amplifier U54 as the input stage and discrete transistors Q32 and Q33 (located on vertical heatsink as shown in Figure 5-7) to drive the high currents in the motor. The overall dc gain of the amplifier is determined by the sum of R103 and R109 divided by the sum of R106 and R112 for high speed motor-tachometers. When the low speed motor-tachometer is employed, the overall gain of the amplifier is determined by the sum of R103 and R109 divided by the sum of R106 and R111. Diodes CR26 and CR27 prevent the contacts of relay K1 from arcing when they are opened. Potentiometer R101 adjusts the initial output offset of the operational amplifier to 0.

### 5.4.1.4 Regulated Power Supply Circuit Description

Transistors Q55, Q59, Q53, and Q57 (located on vertical heatsink as shown in Figure 5-7) provide regulated $+5 v,-5 v,+10 v$, and $-10 v$, respectively. The regulators are driven by the unregulated +18 v and -18 v from the power supply module (J6). Potentiometers R231 and R244 adjust the +5 v and -5 v levels. Zener diodes VR2 and VR5 provide the reference voltage for the positive and negative regulators, respectively. The currents to these diodes come from the regulated +10 v and -10 v lines via R229 and R241. This technique provides improved ripple characteristics for the regulators. CR46, CR47, CR52, and CR53 improve the temperature stability of the supplies. Jumpers W1, W2, W3, and W4 isolate the regulators from the remainder of the PCBA.

A crowbar over-voltage protection is provided and uses zener diode VR3 to detect an increase in the $+5 v$ level to $8 v$, in which case SCR1 fires. Firing SCR1 causes the +18 v fuse on the power supply module to blow, removing the +18 v supply. A similar protection is provided by VR6 and SCR2 for the $-5 v$ level.

### 5.4.1.5 EOT/BOT Amplifier Circuit Description

The EOT and BOT amplifiers utilize identical circuits, therefore, only the operation of the EOT amplifier will be detailed.

The EOT phototransistor is connected via J15 to the Tape Control PCBA. Network C1, R2, R3 in the emitter lead of the EOT phototransistor filters any spurious signals. R1 provides dc feedback between the base and emitter to reduce the current gain variation of the phototransistor. When the EOT tab reaches the EOT/BOT sensor assembly, the light reflected from the tab hits the base of the phototransistor, turning it on. The emitter voltage rises causing Q1 to turn on and Q3 to cut off. Thus, the EOT level goes high. Resistor R5 provides positive feedback, thus enabling the stability of the section.

### 5.4.1.6 Overwrite System Circuit Description

The logic operation of the overwrite circuit was described in Paragraphs 4.3.4.3 and 4.3.4.5 for T8640A and T8660A, respectively. The write power enable portion of the overwrite circuit is basically an R-C ramp utilizing a Darlington-pair transistor circuit (Q12, Q13). Write power is applied to the circuit from contacts 15 and 16 of K1 via the Write Lockout switch.

NOTE
A Write Enble ring must be installed on the supply reel to complete the Write Power Interlock circuit.

When an Overwrite operation is initiated, voltage at the output of power gate U42B drops sharply to Ov and the +5 v charge on capacitor C19 discharges toward Ov . (The R-C time of discharge is determined by the values of C19, R50.) Transistor Q12 conducts and causes transistor Q13 to conduct. The rate of conduction is determined by the discharge time of C19. The voltage at the collector of Q13 rises toward +5 v as determined by the current flow through R53 and Q13. The output voltage is supplied via J8 pin 4 to the Write logic on the Data PCBA

Termination of a Write or Overwrite operation causes the voltage at pin 8 of power gate U42B to rise sharply to +5 v . Conduction of transistors Q12 and Q13 decrease toward cutoff at a rate determined by (R49 + R50), Q19. The output voltage at the collector of Q13 ramps from $+5 v$ to $0 v$ as Q13 cuts off.

### 5.4.1.7 Status and Control Signals Circuit Description

The following paragraphs describe the generation techniques of the various status and control signals which were not explained in the preceding functional subsystems description of the Tape Control PCBA.

The low-true interface ISFC is received via J101 (pin C) inverted by U20A and passed to NAND gate U28A. ISFC is gated at U28A with the Selected, Ready, and On-line (SRO) signal (U34A) and fed to the Forwad ramp generator.

The output of U28A is also passed through NOR gate U28B. The output of U28B is the MOTION signal. Additionally, MOTION is delayed, inverted, differentiated, and fed to the base of transistor Q6. The negative-going signal on the base of Q6 causes the transistor to cut off, generating the positive-going GO pulse at the collector of transistor Q6. This pulse samples the status of the ISWS (J101-K) line. If ISWS is low, indicating that the Write mode is required, the Write/Read flip-flop U41B is set and NWRT goes low. If IOVW is high, then U41A is reset and U42B-8 goes low. In this case, WRT PWR at J8 pin 4 is high if Q12 and Q13 are provided with $+5 v$ to their emitters via the WLO switch.

Reverse commands are generated in the same manner as described for ISFC. The low-true ISRC is received via J101 (pin E) and operates in the same manner as the ISFC, with the exception that the inverted (high-true) ISRC is ANDed with the inverted BOTA signal. This is done to ensure that tape motion will stop upon encountering the BOT tab when the transport is operating in the synchronous reverse mode. The ISRC or the reverse command from the Maintenance switch is NORed by U28C to provide the REVERSE control signal for the Data PCBA.

The BOT single-shot consists of the components pertinent to Q5. The circuit is triggered by the leading edge (positive-going) of the BOT waveform, producing a pulse approximately 0.5 -second wide. This width is determined by capacitors C3 and C4 in conjunction with resistors R15 and R16. The single-shot pulse (NBOTD) is inverted and the trailing edge is differentiated by capacitor C5 in conjunction with resistors R18 and R19 and fed to inverter U24D. In this manner a narrow pulse (BOTDP) is generated whose width is determined by capacitor C5 and resistors R10 and R19.

Read Only transports employ the 9 TRACK switch/indicator to select the 7-track or 9-track head. The switch/indicator is not included in the Read/Write transports although the hardware is included on the PCBA. Table 5-1 illustrates the jumper placement for selection of either 7 - or 9 -track heads.

Table 5-1
Jumper Connections, FORMAT

| Transport Configuration | $\begin{gathered} \text { P22 } \\ (101897) \end{gathered}$ | Jumpers Used |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | W5 | W7 | W8 | W9 | W10 | W11 |
| 9 TRACK, PE, ROT | -01 |  |  |  | X | X |  |
| 9 TRACK, PE/NRZI, ROT | -02 |  | X |  | X |  |  |
| $7 / 9$ TRACK, PE/NRZI, ROT | -03 |  | X | x |  |  |  |
| 9 TRACK, NRZI, ROT. | -04 |  |  |  | X |  |  |
| 7 TRACK, NRZI, ROT/7 TRACK NRZI, READ AND WRITE, HI-DENSITY LOCAL | -05 |  | X |  |  |  |  |
| 7/9 TRACK, NRZI, ROT | -06 |  | X | x |  |  | X |
| 7 TRACK, NRZI, READ AND WRITE, HI DENSITY REMOTE | -07 | X |  |  |  |  |  |
| 9 TRACK, PE, READ AND WRITE | Not Used |  |  |  |  |  |  |
| 9 TRACK, NRZI, READ AND WRITE | Not Used |  |  |  |  |  |  |
| 9 TRACK, PE/NRZI, READ AND WRITE (HI-DEN LOCAL) | -02 |  | X |  | x |  |  |
| 9 TRACK, PE/NRZI, READ AND WRITE (HI-DEN REMOTE) | -08 | X |  |  | x |  |  |
| 7/9 TRACK PE/NRZI, ROT HI DENSITY REMOTE | -09 | x |  | $x$ |  |  |  |

NRZI models which are equipped to operate in the high density mode only, and all Phase Encoded models, utilize jumper W10. Jumper W7 is omitted in these transports, thereby forcing the input of inverter U1B low through jumper W10. The output of U1B is, therefore, permanently high. Since the output of U1B is coupled to the input of inverter U1C, the output of U1C (NHID) is forced low. Note that the switch/indicator contacts are disabled. In Phase Encoded transports the front panel is supplied with a 1600 CPI switch/indicator instead of the HI DEN (high density) switch/indicator and is permanently illuminated since the low output of U1C continuously enables the transistor of the lamp driver circuit.

In NRZI transports equipped to operate in only the low density mode, jumpers W5, W7, and W10 are omitted. The input of inverter U1B is, therefore, permanently high. Since the low output of U1B is directly coupled to the input of inverter U1C, the output of U1C is permanently high. The HI DEN switch/indicator switching contacts are permanently disabled and the lamp is extinguished.

NRZI transports configured to operate in the dual density mode have jumper W7 only installed. The data density and associated indicator are controlled by the HI DEN switch/indicator. When high density is selected via the HI DEN switch/indicator, the input of U1B is connected to 0 v via the contacts of the HI DEN switch/indicator. This causes NHID to be low and the transport is conditioned to operate in the high density mode. When the HI DEN switch/indicator is deactivated, NHID is high and the transport is conditioned to operate in the low density mode.

When jumper W11 is not used and the transport is in high density and 9-track mode (jumper W9 is used or jumper W8 is used and 9 TRACK switch/indicator is depressed), then HIGH SPEED (U3A-3) goes low. Otherwise, HIGH SPEED is high.

The interface Data Density Select (IDDS) operation provides for the external selection of the packing density on dual density transports. Jumper W5 provides the electrical connection to U1B necessary for this feature.

In 9-track transports the High Density mode of operation is automatically selected by installing a jumper to 0v on the Data PCBA which forces J8-5 (NHID) continuously low.

Certain options may be included on the transport to facilitate additional On-line and interface output capabilities. Table 5-2 illustrates the possible combinations of jumpers W12, W13, and W14.

Jumper W12 determines the On-line capabilities of the transport. Transports are normally equipped with jumper W12 which protects the transport from being placed On-line before FLR (First Load or Rewind) goes true. When jumper W12 is omitted, the transport can be placed On-line any time after the interlock has been completed, provided that IOFFC (Off-line Input command) is false.

Jumper W13 determines the relationship between the ISLT command and the SLTA command. SLT is generated by the inversion of ISLT through gate U40B. All interface inputs except IDDS are disabled when ISLT is low (false). SLTA is controlled by the output of U40B when jumper W13 is installed, or SLTA is permanently high (true) through R67 when jumper W13 is omitted. Interface outputs (IONLINE IEOT, IRDY, ILDP, IRWD, IDDI, and IFPT) are gated with SLTA and are disabled when SLTA is Iow.

The presence of jumper W14 causes the ON-LINE command to be wire ANDed with SLT, requiring the transport to be selected by the interface and On-line before SLT (and SLTA if W13 is installed) can go true. Transports are normally equipped with jumper W14.

If a reel of tape with a Write Enable ring is mounted on the supply reel hub, the Write Lockout switch closes, Q10 turns on, and the Write Lockout solenoid energizes. The solenoid in turn keeps the Write Lockout switch closed by retracting the Write Enable ring probe. In this case, +5 v reaches the emitter of Q10 through interlock relay K1 and WRT PWR goes high when the Write mode or Overwrite mode is selected.

In addition, if jumper W16 is used, the WRITE ENABLE lamp drive circuit is activated and the WRITE ENABLE indicator is lit. On the other hand, if jumper W15 is used, the WRITE ENABLE indicator turns off unless the write enable ring is removed from the reel of tape.

Table 5-2
Jumper Connections, OPTIONS

| Options Available |  |  |  | P21 | Jumpers Used |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| On Line At | Output Interface Line Enabled By | Input and Output Interface Lines Enabled By | WRTEN/FPT Indicator | $\begin{gathered} \text { P/N } \\ 102344 \end{gathered}$ | W12 | W13 | W14 | W15 | W16 |
| Middle of Tape | SLTA | SELECT | WRT EN | -01 |  |  |  |  | X |
|  |  |  | FPT | -02 |  |  |  | x |  |
|  |  | SELECT AND ON LINE | WRT EN | -03 |  |  | $x$ |  | X |
|  |  |  | FPT | -04 |  |  | X | X |  |
|  | SELECT | SELECT | WRT EN | -05 |  | X |  |  | X |
|  |  |  | FPT | -06 |  | X |  | X |  |
|  |  | SELECT AND ON LINE | WRT EN | -07 |  | $x$ | $x$ |  | X |
|  |  |  | FPT | -08 |  | X | X | X |  |
| $\begin{gathered} \text { Beginning } \\ \text { Of } \\ \text { Tape } \end{gathered}$ | SLTA | SELECT | WRT EN | -09 | X |  |  |  | X |
|  |  |  | FPT | -10 | $x$ |  |  | X |  |
|  |  | SELECT AND ON LINE | WRT EN | -11 | $x$ |  | $x$ |  | x |
|  |  |  | FPT | -12 | $x$ |  | x | X |  |
|  | SELECT | SELECT | WRT EN | -13 | x | x |  |  | X |
|  |  |  | FPT | -14 | X | x |  | X |  |
|  |  | SELECT AND ON LINE | WRT EN | -15 | $x$ | $x$ | X |  | X |
|  |  |  | FPT | -16 | X | x | X | X |  |

## SECTION VI <br> MAINTENANCE AND TROUBLESHOOTING

### 6.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments, parts replacement, and troubleshooting. Sections IV and V contain the theory of operation of components and circuits for reference.

### 6.2 FUSE IDENTIFICATION

Three fuses are located at the rear of the tape transport and are identified in Table 6-1.

### 6.3 SCHEDULED MAINTENANCE

The tape transport is designed to operate with a minimum of maintenance and adjustments. Parts replacement is planned to be as simple as possible. Repair equipment is kept to a minimum and only common tools are required in most cases. A list of hand tools required to service the tape transport is given in Paragraph 6.7.

To ensure reliable operation of the transport at its optimum design potential, and to assure high MTBF, a scheduled preventive maintenance program is recommended. This schedule is given in Table 6-2.

### 6.3.1 CLEANING THE TRANSPORT

The transport requires cleaning in these major areas: head and associated guides, roller guides, tape cleaner, and capstan.

To clean the head and head guides use a lint-free cloth or cotton swab moistened in $91 \%$ isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION
ROUTH OR ABRASIVE CLOTHS SHOULD NOT BE USED TO CLEAN THE HEAD AND HEAD GUIDES. USE ONLY 91\% ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH as carbon tetrachloride, may result in DAMAGE TO HEAD LAMINATION ADHESIVE.

To clean the capstan, use only a cotton swab moistened with $91 \%$ isopropyl alcohol to remove accumulated oxide and dirt.

To clean the roller guides, use a lint-free cloth or cotton swab moistened in $91 \%$ isopropyl alochol. Wipe the guide surfaces carefully to remove all accumulated oxide and dirt.

> CAUTION

> DO NOT SOAK THE GUIDES WITH EXCESSIVE SOLVENT. THE EXCESS MAY SEEP INTO THE PRECISION GUIDE BEARINGS CAUSING CONTAMINATION AND A BREAKDOWN OF THE BEARING LUBRICANT.

The tape cleaner must be removed from the transport for proper cleaning. Paragraph 6.6.25 details the procedure for removal, cleaning, and reinstallation of the tape cleaner.

Table 6-1
Fuse Identification

|  | Location | Function | Type |
| :---: | :---: | :---: | :---: |
| F1 | Power Supply Module | Line Fuse | $5 \mathrm{amp}, 3 \mathrm{AG}, \mathrm{SB}, 125 \mathrm{v}$ and below $3 \mathrm{amp}, 3 \mathrm{AG}, \mathrm{SB}, 190 \mathrm{v}$ and above |
| F2 |  | +18v | $10 \mathrm{amp}, 3 \mathrm{AG}, \mathrm{FB}$ |
| F3 |  | $-18 \mathrm{v}$ | $8 \mathrm{amp}, 3 \mathrm{AG}, \mathrm{FB}$ |

Table 6-2
Preventive Maintenance Schedule

| Maintenance <br> Operation | Frequency <br> (hours) | Quantity <br> to <br> Maintain | Time <br> Required <br> (minutes) | Manual <br> Paragraph <br> Reference |
| :--- | :---: | :---: | :---: | :---: |
| Clean Head, Head Guides, <br> Roller Guides, and Capstan | 8 (or start of <br> operating day) | - | 5 | 6.3 .1 |
| Check Skew, Tape Tracking. <br> and Speed | 500 | - | 15 | 6.6 .13 or 6.6.14, 6.5.6 |
| Check Head Wear | 2,500 | 1 | 3 | 6.6 .15 |
| Replace Reel Motors and <br> Capstan Motor | 10,000 | 3 | 30 | 6.6 .18 |
| Replace Tension Arm Springs | 10,000 | 2 | 15 | 6.6 .20 |
| Clean Tape Cleaner | 80 | 1 | 5 | 6.6 .25 |

### 6.4 PART REPLACEMENT ADJUSTMENTS

Tables 6-3 and 6-4 define the adjustments that may be necessary when a part is replaced for the T8640A and T8660A transports, respectively. Details are given in Paragraphs 6.5 and 6.6.

### 6.5 ELECTRICAL ADJUSTMENTS

In addition to the tools listed in Paragraph 6.7, the following equipment (or equivalent) will be required for electrical adjustments.
(1) Oscilloscope, Tektronix 561 (vertical and horizontal sensitivity specified to $\pm 3$ percent accuracy); a type 3A6 Dual Trace Amplifier is recommended for use with the Model 561 oscilloscope.
(2) Digital Volt Meter, Fairchild 7050 ( $\pm 0.1$ percent specified accuracy).
(3) Counter Timer, Monsanto Model 100B ( $\pm 0.1$ percent specified accuracy).
(4) Master Skew Tape, IBM No. 432640.
(5) Optical Encoder, 500-Line, PERTEC Part No. 512-1100.
(6) Exerciser, Hand Held, PERTEC Model No. TE-T02 (Part No. 895360-01).

Table 6-3
Part Replacement Adjustments, Model T8640A

| Part Replaced | Auxiliary Adjustments | Time Required (minutes) | Manual Paragraph Reference |
| :---: | :---: | :---: | :---: |
| Capstan | Capstan Height, Read Skew, Tape Path | 10 | 6.6.10, 6.6.13, 6.6.8 |
| Capstan Motor | *Capstan Servo Offset, Tape Speed, Ramp Timing and Rewind Speed on Tape Control PCBA, Read Skew, Tape Path | 35 | $\begin{aligned} & \text { 6.5.4, 6.5.6, } 6.5 .5, \\ & 6.5 .7,6.6 .13,6.6 .7 \end{aligned}$ |
| Control Switch | None | 2 | - |
| Data PCBA | Read Amplifier Gain, Threshold Write Deskew | 20 | 6.5.8, 6.5.9, 6.6.13 |
| Head | Write Deskew, Read Skew, Read Amplifier Gain, Flux Gate | 30 | 6.6.13, 6.5.8, 6.6.17 |
| Interlock Switch | Switch Adjustment | 10 | 6.6.2 |
| Photosensor | EOT/BOT Amplifier | 10 | 6.5.3 |
| Power Supply Assy | None | 20 | - |
| Reel Hub Assy | Reel Hub Assembly Height, Write Lockout Plunger | 10 | 6.6.21, 6.6.24 |
| Reel Motor Assy | Belt Tension, Tension Arm Position Sensor | 10 | 6.6.19, 6.6.7 |
| Reel Motor Drive Belt | Belt Tension | 5 | 6.6.19 |
| Roller Guide Assy | Read Skew, Tape Path | 25 | 6.6.13, 6.6.8 |
| Tape Control PCBA | *Ramp Timing, Tape Speed, Rewind Speed, Capstan Servo Offset, Tension Arm Position Sensor | 40 | $\begin{aligned} & 6.5 .5,6.5 .6,6.5 .7 \\ & 6.5 .4,6.6 .7 \end{aligned}$ |
| Tape-In-Position Sensor | EOT/BOT Amplifier | 10 | 6.5.3 |
| Tension Arm Position Sensor | Tension Arm Position Sensor | 20 | 6.6.6 |
| Tension Arm Spring | Tape Tension throughout Arm Travel | 30 | 6.6.20 |
| Write Lockout Assy | Plunger Height | 10 | 6.6.24 |
| Arm Retracted Limit Switch | Switch Adjustment | 10 | 6.6.5 |
| Arm Extended Limit Switch | Switch Adjustment | 10 | 6.6.4 |
| *The $+5 v$ and $-5 v$ regulators must be checked before attempting any electrical measurements or adjustments. |  |  |  |

Table 6-4
Part Replacement Adjustments, Model T8660A

| Part Replaced | Auxiliary Adjustments | Time Required (minutes) | Manual Paragraph Reference |
| :---: | :---: | :---: | :---: |
| Capstan | Capstan Height, Read Skew, Tape Path | 10 | 6.6.10, 6.6.13, 6.6 .8 |
| Capstan Motor | *Capstan Servo Offset, Tape Speed, Ramp Timing and Rewind Speed on Tape Control PCBA, Read Skew, Tape Path | 35 | $\begin{aligned} & \text { 6.5.4, 6.5.6, 6.5.5, } \\ & 6.5 .7,6.6 .13,6.6 .7 \end{aligned}$ |
| Control Switch | None | 2 | - |
| Data PCBA | Read Amplifier Gain, Threshold | 20 | 6.5.8,6.5.10 |
| Head | Read Skew, Read Amplifier Gain | 30 | 6.6.14, 6.5.8 |
| Interlock Switch | Switch Adjustment | 10 | 6.6.2 |
| Photosensor | EOT/BOT Amplifier | 10 | 6.5.3 |
| Power Supply Assy | None | 20 | - |
| Reel Hub Assy | Reel Hub Assembly Height, Write Lockout Plunger | 10 | 6.6.21, 6.6.24 |
| Reel Motor Assy | Belt Tension, Tension Arm Position Sensor | 10 | 6.6.19, 6.6.7 |
| Reel Motor Drive Belt | Belt Tension | 5 | 6.6.19 |
| Roller Guide Assy | Read Skew, Tape Path | 25 | 6.6.14, 6.6.8 |
| Tape Control PCBA | *Ramp Timing, Tape Speed, Rewind Speed, Capstan Servo Offset, Tension Arm Position Sensor | 40 | $\begin{aligned} & \text { 6.5.5, 6.5.6, 6.5.7, } \\ & \text { 6.5.4, 6.6.7 } \end{aligned}$ |
| Tape-In-Position Sensor | EOT/BOT Amplifier | 10 | 6.5.3 |
| Tension Arm Position Sensor | Tension Arm Position Sensor | 20 | 6.6.6 |
| Tension Arm Spring | Tape Tension throughout Arm Travel | 30 | 6.6.20 |
| Write Lockout Assy | Plunger Height | 10 | 6.6.24 |
| Arm Retracted Limit Switch | Switch Adjustment | 10 | 6.6.5 |
| Arm Extended Limit Switch | Switch Adjustment | 10 | 6.6.4 |
| *The $+5 v$ and $-5 v$ regulators must be checked before attempting any electrical measurements or adjustments. |  |  |  |

### 6.5.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.5.

When the measured value of any parameter is within the specified acceptable limits, NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustments should be made in accordance with the relevant procedure.

## NOTE

Some adjustments may require corresponding adjustments in other parameters. Ensure corresponding adjustments are made as specified in the individual procedures. The +5 and -5 regulator voltages must be checked prior to attempting any electrical adjustments.

When adjustments are made, the value set should be the exact value specified (to the best of the operator's ability).

CAUTION
PRIMARY POWER SHOULD BE REMOVED FROM THE TRANSPORT WHEN REAR ACCESS IS REQUIRED, EXCEPT IN CASES OF ELECTRICAL TESTING AND ADJUSTMENTS.

### 6.5.2 + 5V AND -5V REGULATORS

The $+5 v$ and $-5 v$ regulators are located on the Tape Control PCBA and are adjusted by means of variable resistors R231 and R244. The numerical value of the voltage difference, disregarding polarity, between the +5 v and -5 v lines must be less than 0.07 v since tape speed is dependent upon these voltages.

### 6.5.2.1 Test Configuration

(1) Apply power to the transport.
(2) Load a reel of tape on the transport.
(3) Depress and release the LOAD control twice to establish interlock and tension the tape, and to advance tape to the Load Point.
6.5.2.2 Test Procedure
(1) Using a Fairchild DVM Model 7050 (or equivalent), measure and note the voltage difference between TP23 ( +5 v ) and TP17 ( 0 v ) on the Tape Control PCBA.
(2) Measure and note the voltage difference between TP22 ( -5 v ) and TP17 ( 0 v ) on the Tape Control PCBA.
(3) Acceptable Limits
$\square+5 \mathrm{v}$ Regulator

- +4.95v minimum
- +5.05v maximum
$\square-5 \mathrm{v}$ Regulator
- -4.95 v minimum
- -5.05 v maximum
(4) Compare the voltage obtained in Steps (1) and (2). Voltages must fall within the acceptable limits and the absolute difference between the $+5 v$ and $-5 v$ lines must be less than 0.07 v .


### 6.5.2.3 Adjustment Procedure

When the acceptable limits are exceeded or the voltage difference between the +5 v and $-5 v$ lines exceeds 0.07 v , the following adjustments are performed.
(1) Adjust variable resistor R231 on the Tape Control PCBA to +5.0 v as observed at TP23 (using TP17 as the Ov reference).
(2) Adjust variable resistor R244 on the Tape Control PCBA to -5.0 v as observed at TP22 (using TP17 as the 0v reference).
(3) Verify that the voltage difference between TP23 and TP22 on the Tape Control PCBA falls within the acceptable limits and the absolute difference between the +5 v and -5 v lines is less than 0.07 v .

### 6.5.2.4 Related Adjustments

The EOT/BOT Amplifier, Capstan Servo Offset, Ramp Timing, Tape Speed, Rewind Speed, and Read Amplifier Gain (Paragraphs 6.5.3 through 6.5.8) must be checked and adjusted, if necessary, subsequent to adjusting the $+5 v$ and $-5 v$ regulators.

### 6.5.3 EOT/BOT AMPLIFIER

The EOT/BOT Amplifier circuit is located on the Tape Control PCBA.
NOTE
The 5 v regulators must be checked and adjusted, if necessary, prior to checking the EOT/BOT Amplifier system.

### 6.5.3.1 Test Configuration

(1) Apply power to the transport.
(2) Load a reel of tape on the transport.
(3) Depress and release the LOAD control twice to establish interlocks and tension the tape, and to advance tape to the Load Point.

### 6.5.3.2 Test Procedure

(1) Advance tape until the reflective BOT tab is past the photosensor.
(2) Using a Fairchild DVM Model 7050 (or equivalent), measure and note the off-tab voltage between TP4 (EOT) and TP17 (Ov) on the Tape Control PCBA.
(3) Measure and note the off-tab voltage between TP3 (BOT) and TP17 (Ov) on the Tape Control PCBA.
(4) Acceptable Limits (off-tab)

- +0.5 v maximum
(5) Position tape so that the reflective BOT tab is located under the photosensor.
(6) Measure and note the on-tab voltage between TP3 (BOT) and TP17 (Ov) on the Tape Control PCBA.
(7) Advance tape until the EOT tab is positioned under the photosensor.
(8) Measure and note the on-tab voltage between TP4 (EOT) and TP17 (Ov) on the Tape Control PCBA.
(9) Acceptable Limits (on-tab)
- +3.0v minimum
(10) Depress and release the REWIND control. Tape will rewind past the BOT tab, enter the Load sequence, return to the BOT tab and stop.
(11) Depress and release the REWIND control. Tape will reenter the Unload mode and remain until tape tension is lost.
(12) Remove the supply reel from the transport.
(13) Measure and note the voltage at TP4 (EOT) and TP3 (BOT) using TP17 (Ov) as reference.
(14) Acceptable Limits
- +3.0v minimum


### 6.5.3.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.
(1) Prepare transport by removing tape from tape path.
(2) Remove the head cover.
(3) Apply power to the transport.
(4) Set potentiometer R274, loated on the Tape Control PCBA, to the full counterclockwise position.
(5) Connect a Fairchild DVM Model 7050, or equivalent, between TP4 (EOT) and TP17 ( $0 v$ ) on the Tape Control PCBA.
(6) Adjust R274 in a clockwise direction until the voltage measured at TP4 switches from less than +0.5 v to greater than +3.0 v .
(7) Adjust R274 one-quarter turn in a clockwise direction.
(8) Set potentiometer R275, located on the Tape Control PCBA, to the full counterclockwise position.
(9) Connect the DVM between TP3 (BOT) and TP17 (Ov) on the Tape Control PCBA.
(10) Adjust R275 in a clockwise direction until the voltage measured at TP3 switches from less than +0.5 v to greater than +3.0 v .
(11) Adjust R275 one-quarter turn in a clockwise direction.
(12) Perform the EOT/BOT Amplifier Test Procedure detailed in Paragraph 6.5.3.2.

### 6.5.3.4 Related Adjustments

- None.


### 6.5.4 CAPSTAN SERVO OFFSET

The Capstan Servo Offset potentiometer, R101, is located on the Tape Control PCBA and should be checked and adjusted prior to adjusting tape speed.

## NOTE

The 5 v regulators must be checked and adjusted, if necessary, prior to adjusting the Capstan Servo Offset potentiometer.

### 6.5.4.1 Test Configuration

(1) Apply power to the transport.
(2) Load a reel of tape on the transport.
(3) Depress and release the LOAD control twice to establish interlocks and tension tape, and to advance tape to the Load Point.

### 6.5.4.2 Test Procedure

(1) Using a Fairchild DVM Model 7050 (or equivalent), measure and note the voltage between TP32 and TP17 on the Tape Control PCBA. Measured voltage is the output of the capstan motor amplifier.
(2) Acceptable Limits

- $+0.20 v$ maximum
- -0.20 v maximum


### 6.5.4.3 Adjustment Procedure

When the acceptable limits are exceeded, perform the following adjustment.
(1) Establish the test configuration described in Paragraph 6.5.4.1.
(2) Using a Fairchild DVM Model 7050 (or equivalent), measure the voltage between TP32 and TP17 on the Tape Control PCBA.
(3) Adjust variable resistor R101 to obtain Ov, nominal.

### 6.5.4.4 Related Adjustments

The Tape Speed and Read Amplifier Gain must be checked and adjusted after adjustments are made to the Capstan Servo Offset.

### 6.5.5 RAMP TIMING

The four tape acceleration and deceleration ramps (Forward and Reverse, Start and Stop) are controlled by a single potentiometer adjustment located on the Tape Control PCBA.

The adjustment controls the Start/Stop time and its value is chosen to ensure that the correct Start/Stop distance is obtained.

NOTE
The $5 v$ regulators must be checked and adjusted, if necessary, prior to adjusting the Ramp Timing.

### 6.5.5.1 Test Configuration

(1) Apply power to the transport.
(2) Load a reel of tape on the transport.
(3) Depress and release the LOAD control twice to establish interlocks and tension the tape, and to advance tape to the Load Point.

### 6.5.5.2 Test Procedure

(1) Connect a signal probe of a Tektronix Model 561 (or equivalent) oscilloscope to TP20 on the Tape Control PCBA.
(2) Connect the oscilloscope reference (ground) probe to TP17 ( $0 v$ ) on the Tape Control PCBA.
(3) Connect the transport ISLTO line to ground at J101 pin J and place the transport On-line.
(4) Apply a 5 Hz symmetrical square wave with a 3 v amplitude ( +3.0 v to Ov ) to the interface line ISFC (J101 pin C).
(5) Trigger the oscilloscope externally on the negative-going edge of the square wave input.
(6) Adjust the oscilloscope Vertical output control to display 0 to 100 percent of the ramp waveform over four large divisions of the oscilloscope graticule.
(7) Observe that the ramp time intersects the 90 percent of the ramp amplitude ( 18 small divisions of oscilloscope graticule). Figure 6-1 illustrates ramp levels and timing.
(8) Nominal values for ramp times are: 90 percent of actual speed.

| Speed <br> (ips) | Nominal Ramp Time <br> (msec) |
| :---: | :---: |
| 45.0 | 6.5 |
| 37.5 | 8.0 |
| 25 | 11.5 |
| 18.75 | 15.5 |
| 12.5 | 26.0 |

(9) Remove the square wave input from J101 pin C (ISFC) and apply the square wave input to ISRC line (J101 pin E).
(10) With the oscilloscope adjusted as specified in Step (6), observe that the reverse ramp timing is within the limits specified in Step (8).

NOTE
For reverse operation, the ramp is a negative-going waveform.


Figure 6-1. Ramp Levels and Timing

### 6.5.5.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.
(1) Establish test configuration described in Paragraph 6.5.5.1.
(2) Perform test procedure described in Paragraph 6.5.5.2, Steps (1) through (6).
(3) Adjust variable resistor R87 on the Tape Control PCBA to attain the ramp adjustment time specified in the Nominal Ramp Time Column in Paragraph 6.5.5.2, Step (8).

## NOTE

Specified time results in oscilloscope display illustrated in Figure 6-1. The ramp adjustment time intersects $90 \%$ of ramp amplitude when accelerating and $10 \%$ of ramp amplitude when decelerating.
(4) Remove the square wave input from ISFC line (J101 pin C) and apply the square wave input to the interface line ISRC (J101 pin E).
(5) Observe oscilloscope display of the reverse ramp. The ramp time should be as specified in Paragraph 6.5.5.2, Step (8).
6.5.5.4 Related Adjustments

- None.


### 6.5.6 TAPE SPEED

The synchronous forward and reverse speeds are independently adjustable.
NOTE
The +5 v and -5 v regulator voltages must be checked and adjusted prior to adjusting tape speed.

Two methods of tape speed adjustments are given. Paragraphs 6.5.6.1 through 6.5.6.3 describe the optical encoder method; Paragraphs 6.5.6.4 through 6.5.6.7 describe the strobe disk method.
6.5.6.1 Test Configuration — Optical Encoder Method
(1) Apply power to the transport.
(2) Load a reel of tape.
(3) Depress and release the LOAD control twice to establish interlocks and tension the tape, and to advance tape to the Load Point.
(4) Couple an Optical Encoder, PERTEC Part No. 512-1100, to the front of the capstan. Five volts dc must be applied to the optical encoder lamp input (pins 1 and 2). This voltage can be obtained between TP23 ( +5 v ) and TP17 ( 0 v ) on the Tape Control PCBA.
6.5.6.2 Test Procedure - Optical Encoder Method
(1) Connect input probes of Counter Timer, Monsanto Model 100B (or equivalent), to pins 6 and 7 of the Optical Encoder.
(2) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the forward direction.
(3) Adjust the sample interval of the counter timer to monitor the encoder output over a 1 second interval.
(4) Acceptable Limits45 ips

- 4545 Hz maximum
- 4455 Hz minimum37.5 ips
- 3788 Hz maximum
- 3713 Hz minimum25 ips
- 2550 Hz maximum
- 2450 Hz minimum
18.75 ips
- 1913 Hz maximum
- 1838 Hz minimum12.5 ips
- 1275 Hz maximum
- 1225 Hz minimum
(5) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the reverse direction.
(6) With the counter timer connected as specified in Step (1), monitor the output of the optical encoder.
(7) Acceptable Limits45 ips
- 4635 Hz maximum
- 4365 Hz minimum
37.5 ips
- 3863 Hz maximum
- 3638 Hz minimum

25 ips

- 2575 Hz maximum
- 2425 Hz minimum
$\square 18.75$ ips
- 1931 Hz maximum
- 1819 Hz minimum
12.5 ips
- 1288 Hz maximum
- 1213 Hz minimum


### 6.5.6.3 Adjustment Procedure - Optical Encoder Method

When the forward or reverse tape speed exceeds the specified limits, the following adjustments are performed.
(1) Establish the test configuration described in Paragraph 6.5.6.1.
(2) Perform the test procedure described in Paragraph 6.5.6.2, Steps (1) through (3).
(3) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the forward direction (or reverse direction when adjusting for reverse tape speeds).
(4) Adjust the variable resistor R96 (or R277 when adjusting for reverse tape speeds) on the Tape Control PCBA for a counter frequency as follows.

| Tape Speed (ips) | Counter Frequency (Hz) |
| :---: | :---: |
| 45 | 4500 |
| 37.5 | 3750 |
| 25 | 2500 |
| 18.75 | 1875 |
| 12.5 | 1250 |

(5) Monitor the counter timer to ensure that the forward and reverse speeds are within the limits established in Paragraph 6.5.6.2. Repeat Steps (2) through (6) as necessary.

### 6.5.6.4 Tape Speed — Strobe Disk Adjustment

Tape speed adjustments made using the strobe disk are accomplished by illuminating the capstan hub from a fluorescent light source and adjusting the capstan servo until the disk image, created by the pulsating light source, becomes stationary. Table 6-5 lists the available disks, synchronous tape speeds, and light source frequencies.

Some strobe disks have two or more concentric sets of strobe markings on each disk. The following rules apply to disks marked with multiple sets of strobe markings.
(1) Part No. 101744-02 (12.5/25 ips). The outer ring is used when the fluorescent light source is 60 Hz . The inner ring is used when the fluorescent light source is 50 Hz .
(2) Part No. 101744-03 ( $18.75 / 37.5 \mathrm{ips}$ ). There are three sets of strobe markings on this disk. The outer ring is used when checking and adjusting synchronous tape speeds of 18.75 or 37.5 ips from a 60 Hz light source. The middle ring is used at a tape speed of 37.5 ips from a 50 Hz light source. The inner ring is used at a tape speed of 18.75 ips from a 50 Hz light source.
(3) Part No. 101744-04 ( $20 / 40 \mathrm{ips}$ ). The outer ring is used when the light is from a 60 Hz source. The inner ring is used when the light source is from 50 Hz .
(4) Part No. 101744-05 (22.5/45 ips). The outer ring is used when checking and adjusting a tape speed of 45 ips from a 60 Hz light source. The middle ring is used at a tape speed of 22.5 ips from a 60 Hz light source. The inner ring is used at a tape speed of 22.5 ips from a 50 Hz light source.
(5) Part No. 101744-07 (30 ips). The outer ring is used when the light source is 60 Hz . The inner ring is used when the light source is 50 Hz .

The use of the capstan-mounted strobe disk should be limited to fine tape adjustments of the synchronous tape speed. When it is necessary to make gross speed adjustments (e.g., when replacing a Tape Control PCBA), refer to the test and adjustment procedures described in Paragraphs 6.5.6.1 through 6.5.6.3.

### 6.5.6.5 Test Configuration - Strobe Disk Method

(1) Apply power to the transport.
(2) Load a reel of tape.
(3) Depress and release the LOAD control twice to establish interlocks and tension the tape, and to advance tape to the Load Point.
(4) Illuminate the strobe disk located on the front of the capstan using a 60 Hz fluorescent light source.

Table 6-5
Strobe Disks

| PERTEC <br> Part No. | Tape Speed <br> (ips) | Light Source <br> Frequency (Hz) |
| :---: | :---: | :---: |
| $101744-02$ | $12.5 / 25$ | $60 / 50$ |
| $101744-03$ | $18.75 / 37.5$ | $60 / 50$ |
| $101744-04$ | $20 / 40$ | $60 / 50$ |
| $101744-05$ | $22.5 / 45$ | $60 / 50$ |
| $101744-06$ | 24 | 60 |
| $101744-07$ | 30 | $60 / 50$ |

### 6.5.6.6 Test Procedure - Strobe Disk Method

(1) Establish the test configuration described in Paragraph 6.5.6.5.
(2) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the forward direction.
(3) Observe the strobe disk image; the image should appear to be stationary.

### 6.5.6.7 Adjustment Procedure - Strobe Disk Method

(1) Establish the test configuration described in Paragraph 6.5.6.5.
(2) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the forward direction (or in the reverse direction when adjusting reverse tape speeds).
(3) Adjust variable resistor R96 (or R277 when adjusting for reverse tape speeds) on the Tape Control PCBA until the strobe disk image appears to be stationary.

### 6.5.6.8 Related Adjustments

The Read Amplifier Gain must be checked and adjusted after adjustments are made to the Tape Speed.

### 6.5.7 REWIND SPEED

The tape Rewind Speed should be between the following limits.

- 180 ips minimum
- 220 ips maximum


## NOTE

The +5 v and -5 v regulator voltages must be checked and adjusted prior to adjusting tape speed.

### 6.5.7.1 Test Configuration

(1) Apply power to the transport.
(2) Load a reel of tape.
(3) Depress and release the LOAD control twice to establish interlocks and tension the tape, and to advance tape to the Load Point.
(4) Couple an Optical Encoder, PERTEC Part No. 512-1100, to the front of the capstan. Five volts dc must be applied to the optical encoder lamp input (pins 1 and 2). This voltage can be obtained between TP23 ( +5 v ) and TP17 (0v) on the Tape Control PCBA.

### 6.5.7.2 Test Procedure

(1) Connect input probes of Counter Timer, Monsanto Model 100B (or equivalent), to pins 6 and 7 of the optical encoder.
(2) With a full reel of tape wound onto the takeup hub, depress and release the REWIND control.
(3) Adjust the sample interval of the counter timer to monitor the encoder output over a 1 second interval.
(4) Acceptable Limits

- $22,000 \mathrm{~Hz}$ maximum
- $18,000 \mathrm{~Hz}$ minimum
6.5.7.3 Adjustment Procedure
(1) Establish the test configuration described in Paragraph 6.5.7.1.
(2) Perform the test procedure described in Paragraph 6.5.7.2, Steps (1) through (3).
(3) Adjust the variable resistor R123 on the Tape Control PCBA to obtain a counter timer value of $20,000 \mathrm{~Hz}$. This corresponds to 200 ips rewind speed.


### 6.5.7.4 Related Adjustments

- None.


### 6.5.8 READ AMPLIFIER GAIN

The gain of each of the read amplifiers (located on the Data PCBA) is independently adjustable by means of variable resistors R117 through R917; gain is measured at the outputs of the Read Differentiators.

NOTE
The Tape Speed must be checked and adjusted prior to adjusting the Read Amplifier Gain.

Read amplifier gain may be determined by reading an all-ones tape ( 3200 frpi ) which was recorded on the transport. Paragraph 6.5.8.4 details a method for generating an all-ones tape.

### 6.5.8.1 Test Configuration

(1) Clean the head assembly and tape path as described in Paragraph 6.3.1.
(2) Load a prerecorded all-ones tape.
(3) Apply power to the transport.
(4) Depress and release the LOAD control to establish interlocks and tension tape.
(5) Depress and release the LOAD control a second time; tape will advance to the Load Point and stop.

### 6.5.8.2 Test Procedure

(1) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the forward direction.
(2) Using the signal probe of a Tektronix 561 oscilloscope (or equivalent), measure and record the peak-to-peak amplitude of the read amplifier waveforms viewed at the output of each differentiator (TP104 through TP904) on the Data PCBA.

NOTE
Oscilloscope vertical sensitivity should be set to display 2v per division.
(3) Acceptable limits (peak-to-peak when generating an all-ones tape).

- 4.75 v maximum
- $3.25 v$ minimum


### 6.5.8.3 Adjustment Procedure

When the acceptable limits are exceeded, the following adjustments are performed.
(1) Establish the test configuration described in Paragraph 6.5.8.1.
(2) Set the Maintenance switch on the Tape Control PCBA so that tape moves in the forward direction.
(3) Using the signal probe of a Tektronix 561 oscilloscope (or equivalent), observe TP104 through TP904 on the Data PCBA. Adjust potentiometers R117 through R917 associated with test points to 4.0 v peak-to-peak.

### 6.5.8.4 Generation of All-Ones Tape

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used. The read amplifier output should be adjusted as detailed in Paragraph 6.5.8.3. A read amplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to dropouts.

An all-ones tape may be generated as follows.
(1) Ensure that the head assembly and tape path are clean.
(2) Load a good quality work tape with a Write Enable ring in place, on the transport.
(3) Depress the LOAD switch twice to bring the transport to Load Point.
(4) Apply a ground to interface line ISWS (J101 pin K).
(5) Apply a ground to interface line ISLT ( J 101 pin J ).
(6) Apply a ground to interface line ISFC (J101 pin C).
(7) Apply a square wave to interface lines IWDP—IWD7 (J102 pins L, M, N, P, R, S, T, U , and V ).

(8) Apply negative-going pulses ( $+3 v$ to $0 v$ ) of $1-\mu \mathrm{sec}$ duration to the interface line IWDS (J102 pin A).

(9) Maintain the transport in this record mode for approximately 5 minutes.
(10) Remove the signal source from the interface line IWDS (J101 pin A).
(11) Remove the signal which was connected to the interface in Step (7).
(12) Remove the ground from the interface lines IWDP—IWD7 (J102 pins L, M, N, P, R, S, T, U, and V).
(13) Remove the ground from the interface line ISLT (J101 pin J).
(14) Depress and release the REWIND control; tape will rewind to the Load Point and stop.

### 6.5.9 THRESHOLDS (MODEL T8640A ONLY)

The output voltage of the threshold generator can be checked at TP6 on the Data F PCBA in the different modes of operation. The following values are included as a check only; no adjustment procedure is applicable. If the listed limits are exceeded, this is indicative of a fault in the threshold circuitry.
(1) Write Mode

- +5.0 v maximum
- +3.8 v minimum
(2) Read Mode

IRTH2 False

- +2.4 v maximum
- +1.8 v minimum

IRTH2 True

- +1.4 v maximum
- +0.8 v minimum


### 6.5.10 THRESHOLDS (MODEL T8660A ONLY)

The output voltage of the threshold generator can be checked at TP6 on the Data G PCBA in the different modes of operation. The following values are included as a check only; no adjustment procedure is applicable. If the listed limits are exceeded, this is indicative of a fault in the threshold circuitry.
(1) Write Mode. IRTH1 is used in the true condition when performing a read check immediately after writing data.

- +6.8 v maximum
- +5.6 v minimum
(2) Read Mode (IRTH1 must be false)
$\square$ IRTH2 False
- +3.0v maximum
- +2.4 v minimum

IRTH2 True

- +1.6v maximum
- +1.0v minimum


### 6.6 MECHANICAL ADJUSTMENTS

### 6.6.1 TENSION ARM LIMIT SWITCHES

There are three limit switches used in the transport; these are the tension arm interlock switch, the load limit switch, and the gear motor limit switch.

When adjusting these switches it will be necessary to move the tension arms up or down. The arms can be moved into the operating region only by applying power to the transport. Preliminary preparation of the transport is accomplished as follows.

CAUTION
NEVER EXERT PRESSURE ON A TENSION ARM ROLLER IN ATTEMPTING TO MOVE A TENSION ARM INTO THE OPERATING REGION FROM THE LOAD POSITION. DAMAGE TO THE ARM RETRACTOR ASSEMBLY OR THE ROLLER GUIDE SHAFT MAY RESULT.
(1) Remove both tape reels.
(2) Block the light path to the Tape In Path (TIP) reflector.
(3) Depress and release the LOAD control.
(4) Remove power from the transport when the arms have reached the end of their operating range.

### 6.6.2 TENSION ARM INTERLOCK SWITCH

### 6.6.2.1 Test Procedure

The tension arm interlock switch is located on the supply tension arm bearing housing and is actuated by the cam interlock on the tension arm shaft. Proper adjustment of the arm interlock is checked as follows.
(1) Prepare the transport as described in Paragraph 6.6.1.
(2) Disconnect connector P5 (supply reel motor) and connector P4 (takeup reel motor) from the Tape Control PCBA.
(3) Manually rotate the supply arm from its retracted position through its complete range to a position where the supply arm contacts the upper stop. Observe the following conditions.

- At rest, with the switch arm roller in contact with the low point of the cam, the switch contacts are open.
- When the center line of the supply arm is approximately 0.15 -inch past the first mark on the tape deck (visible through the arm slot), the switch arm roller should be contacting the high point of the cam. At this point, the switch contacts should close.
- When the supply arm approaches within 0.15 -inch of the third mark (uppermost) on the tape deck (visible through the arm slot), the switch arm roller should still be in contact with the high point of the cam. At this point, the switch contacts should be closed.

NOTE
The operating range of the interlock switch is between the first and third marks on the tape deck [while the switch arm is in contact with the high point of the cam].

### 6.6.2.2 Adjustment Procedure

If the test procedure performed in Paragraph 6.6.2.1 indicates that an adjustment is required, proceed as follows.
(1) Loosen the cam retaining setscrew located in the hub of the cam.
(2) Reposition the cam on its shaft until the switch arm is in contact with the low point of the cam and the switch contacts are open.
(3) Torque the cam retaining setscrew to 15 inch-pounds.

CAUTION
THE SETSCREW MUST BE TORQUED TO 15 INCHPOUNDS TO PREVENT ROTATION OF THE CAM WHEN the supply tension arm contacts either the UPPER OR LOWER STOP.
(4) If the adjustment in Step (2) cannot be made, loosen the two switch mounting screws and reposition the switch to a location where the requirements of Paragraph 6.6.6.1 Step (3) can be met.

### 6.6.2.3 Replacement Procedure

Replacement of the interlock switch is accomplished as follows.
(1) Remove power from the transport.
(2) Remove the two mounting screws which secure the limit switch to the mounting plate.
(3) Remove the switch and connectors; note the switch terminals and color coding of the wires.
(4) Install a new switch. Ensure the requirements of Paragraph 6.6.2.1 can be met.
(5) Connect the wiring to the new switch observing the proper connections noted in Step (3).

### 6.6.3 LOAD LIMIT SWITCH

The load limit switch is mounted on the tape deck and is accessible from the front. The load limit switch is actuated by the supply tension arm and is used to turn off the arm gear motor when the supply arm reaches the load position.

### 6.6.3.1 Adjustment Procedure

The load limit switch should be adjusted so the normally open switch contacts are closed when the supply arm is in the maximum extended load position. Adjustment of the switch is made by loosening the switch mounting screws and sliding the switch mounting bracket to the desired position and then retightening the screws.

### 6.6.3.2 Replacement Procedure

Replacement of the load limit switch is accomplished as follows.
(1) Remove power from the transport.
(2) Remove the load limit switch connector from the cable harness.
(3) Disconnect the leads and remove the switch assembly from the deck.
(4) Place the new switch near the center of the adjustment region.
(5) Connect the leads to the new switch.
(6) Check that the normally open switch contacts are closed when the arms are at the maximum extended load position. Readjust if necessary.
(7) Connect the cable harness.

### 6.6.4 GEAR MOTOR LIMIT SWITCH

The gear motor limit switch is attached to the gear motor mounting plate and is used to indicate to the relevant logic that the arm retractor has completed a full cycle. Refer to Figure 6-2 in conjunction with the following adjustment procedure.

### 6.6.4.1 Adjustment Procedure

The gear motor limit switch should be adjusted so that when the gear motor is cycling, the normally open switch contacts are closed when the switch roller is approximately at the center of the arm retractor cam. Adjustments are made by loosening the switch mounting screws and rotating the switch. Two holes in the rear of the mounting plate provide access to the screws.

## CAUTION

DO NOT ATtEMPT TO REMOVE OR INSTALL THE GEAR MOTOR ASSEMBLY WITH THE TENSION ARMS IN ANY POSITION EXCEPT THE FULLY RETRACTED POSITION. damage to the gear train or to the tension ARMS COULD RESULT.

### 6.6.4.2 Replacement Procedure

Replacement of the gear motor limit switch is accomplished as follows.
(1) Remove both tape reels and retract both tension arms as described in Paragraph 6.6.1.
(2) Remove power from the transport.
(3) Disconnect connector P29 from the cable harness.
(4) Remove the leads from the limit switch, noting terminal and wire colors; remove the old switch.
(5) Install the new switch and reconnect the leads to the switch.
(6) If adjustment is required, loosen and rotate the switch until the switch contact closes.
(7) Reconnect P29 to the cable harness.


Figure 6-2. Gear Motor Limit Switch Assembly, Rear View

### 6.6.5 GEAR MOTOR ASSEMBLY

The gear motor assembly (PERTEC Part No. 500-0002) is replaced as a complete assembly. The arm retractor actuator and the limit switch cable assembly need not be replaced unless damaged. Removal and replacement procedures are as follows (refer to Figure 6-2 for identification of parts).

### 6.6.5.1 Removal of Gear Motor Assembly

(1) Remove both tape reels and retract tension arms as indicated in Paragraph 6.6.1.
(2) Remove power from the transport.
(3) Disconnect connector P29 from the cable harness.
(4) Remove the spring-loaded wire linkage cables from the arm retractor actuator to each driver arm pulley.
(5) Disconnect the wires to the motor terminals; note polarity and color coding.
(6) Remove the four mounting screws securing the gear motor assembly to the mounting plate; remove the entire assembly.
(7) Remove the arm retractor actuator from the output shaft.

### 6.6.5.2 Replacement of Gear Motor Assembly

Replacement of the gear motor assembly is made as follows. When the new assembly is received, the flat on the output shaft of the gear motor may not be in the desired operating position relative to the retractor assembly.

CAUTION
do not attempt to rotate the output shaft by hand as damage to the gear train may result.
(1) Install the arm retractor actuator on the gear motor output shaft. Tighten the setscrew in the arm retractor to the flat on the output shaft; torque to 10 inch-pounds. (Disregard the position of the arm retractor relative to the switch actuating arm.)
(2) Install the gear motor assembly to the mounting plate.
(3) Connect the negative wire to the negative terminal of the motor.

NOTE
Do not connect the positive [red] wire at this time.
(4) Connect arm limit switch connector P29 to the cable harness connector.
(5) Insert a nonreflective card between the photosensor and the reflector.
(6) Apply power to the transport.
(7) Depress and release the LOAD switch.
(8) Momentarily connect the positive (red) wire to the motor. The arm actuator roller will rotate to the center of the cam lobe and the motor will stop. (The position of the arm actuator is illustrated in Figure 6-2.)
(9) If the gear motor limit switch fails to stop the gear motor, loosen the mounting screws and position the switch to a point that, when the switch actuating arm is depressed by the retractor actuator cam, power to the motor is removed.
(10) Tighten the switch mounting screws.
(11) Connect the positive (red) wire to the positive motor terminal. Allow the retractor actuator to again rotate until the switch roller is actuated by the cam lobe on the arm retractor actuator. At this position, power should be removed from the motor.
(12) Remove power from the transport.

### 6.6.5.3 Return Transport to Operational Status

(1) Reinstall the spring-loaded wire linkage cables to each tension arm pulley.
(2) Remove the nonreflective card from between the photosensor and reflector.
(3) Install the tape reels on the transport.
(4) Thread the tape along the tape path and onto the takeup reel.
(5) Apply power to the transport.
(6) Depress and release the LOAD switch one time. Observe that each tension arm is positioned at a point about three-quarters through its range.
(7) Depress and release the LOAD switch a second time. Observe forward tape motion until the BOT tab is reached.
(8) Depress and release the LOAD switch. There should be no movement of tape or tension arms.
(9) Make an overall inspection of the transport for foreign material; ensure that the cable harness routing does not interfere with moving parts.

### 6.6.6 TENSION ARM POSITION SENSOR

There are two tension arm position sensors; one on the takeup tension arm, and one on the supply tension arm. The sensor outputs are connected to the reel servo amplifier inputs on the Tape Control PCBA.

NOTE
Before adjusting either of the tension arm position sensors, ensure that the 5 v Regulators, Ramp Timing, and Tape Speed are correct as detailed in Paragraphs 6.5.2, 6.5.5, and 6.5.6, respectively.

### 6.6.6.1 Preliminary Adjustment

The tension arm position sensors on the supply reel and takeup reel are initially adjusted as follows.
(1) Remove both tape reels. Position both tension arms in their operating region as described in Paragraph 6.6.1.
(2) Remove power from the transport.
(3) Loosen the 10-32 self-locking nut that attaches the optical shutter. Ensure that there is sufficient friction to prevent the setting from changing when the screw is tightened.
(4) Apply power to the transport. Establish an environment which ensures that the tension sensors are shielded from high ambient light. Failure to do so might result in a shift in the arm operating region when the unit is rack-mounted.
(5) To place the shutters in the correct position, rotate each shutter with the tension arm placed over the center mark on the surface of the tape deck until +0.6 v is read at TP19 for the supply reel or TP24 for the takeup reel. Tighten the 10-32 selflocking nut to 20 inch-pounds. Take care not to disturb the shutter setting.
(6) Remove power from the transport.
(7) Load tape on the transport.
(8) Perform electrical adjustments detailed in Paragraphs 6.6.6.2 and 6.6.6.3.

### 6.6.6.2 Takeup Arm Adjustment

When the preliminary adjustments are completed, proceed as follows.
(1) Ensure that the takeup reel is nearly empty.
(2) Alternately toggle the Maintenance switch on the Tape Control PCBA to shuttle tape back and forth.
(3) If Step (2) causes loss of tape tension because the takeup arm exceeds its operating range, retension the tape by depressing the LOAD control. Adjust potentiometer R157 on the Tape Control PCBA five turns CCW to reduce the total takeup arm movement; repeat this step as required.
(4) Adjust potentiometer R157 on the Tape Control PCBA until the outside edge of the takeup arm is in line with the outside marks on the surface of the tape deck.

NOTE
The actual arc of the shutter movement may not coincide with that specified because the shutter may not be perfectly centered at this point in the procedure.
(5) Adjust R159 on the Tape Control PCBA so the arc of the arm movement is equidistant between the marks on both of the center marks.

NOTE
The arm position during Forward and Reverse motion should remain within the limits of the two outside marks on the tape deck.

### 6.6.6.3 Supply Arm Adjustment

When the preliminary adjustments are completed, proceed as follows.
(1) Ensure that the supply reel is nearly empty.
(2) Alternately toggle the Maintenance switch on the Tape Control PCBA to shuttle tape back and forth.
(3) If Step (2) causes loss of tape tension because the supply arm exceeds its operating range, retension tape by depressing the LOAD control. Adjust potentiometer R192 on the Tape Control PCBA five turns CCW to reduce the total supply arm movement; repeat this step as required.
(4) Adjust potentiometer R192 on the Tape Control PCBA until the outside edge of the supply arm is in line with the outside marks on the surface of the tape deck.

NOTE
The actual arc of movement may not coincide with that specified because the shutter may not be perfectly centered at this point in the procedure.
(5) Adjust R194 on the Tape Control PCBA so the arc of the arm movement is within the limits of the center mark.

NOTE
The arm position during Forward and Reverse motion should remain within the limits of the two outside marks on the tape deck.

### 6.6.6.4 Tension Arm Sensor Replacement

The tension arm optical sensors are replaced as follows.
(1) Rewind tape and remove the tape reel from the transport.
(2) Retract and position the tension arms in their operating regions as described in Paragraph 6.6.1.
(3) Remove power from the transport.
(4) Remove the harness connector at the arm sensor.
(5) Loosen the 10-32 self-locking nut which secures the optical shutter to the tension arm shaft.
(6) Rotate the shutter to clear the right-hand countersunk screw which retains the arm sensor PCBAs to the standoffs.
(7) Remove the right-hand screw. Manually rotate the tension arm to gain access to the left-hand screw.
(8) Remove the left-hand mounting screw and remove the sensor assembly.
(9) Mount the replacement assembly in the above (reverse) order. Torque the 10-32 self-locking nut on the tension arm shaft to 20 inch-pounds.

## NOTE

The F6 mark is visible when the supply arm shutter is correctly installed.
(10) Partially tighten the shutter in place.
(11) Plug the harness connector into the arm sensor connector.
(12) Perform the relevant adjustment procedures in Paragraphs 6.6.6.1, 6.6.6.2, and 6.6.6.3.

### 6.6.7 TAPE PATH ALIGNMENT

Paragraphs 6.6.8 through 6.6.12 detail the procedures for tape path alignment of the T8000A transports.

### 6.6.8 UNIVERSAL TAPE PATH ALIGNMENT TOOL

The PERTEC Universal Tape Alignment Tool, (Part No. 102382-01) is used for alignment of the supply and takeup guide rollers to the head guides. This tool is used to establish tension arm guide roller parallelism and tape reel positioning.

Since this tool can be used on all PERTEC tape transports, not all hole combinations or tool positions are used on any one transport for alignment. Only those holes required to accomplish tape path alignment on this model transport will be shown on the supporting figures.

CAUTION
the pertec alignment tool is a precision INSTRUMENT. CARE MUST BE TAKEN TO AVOID DAMAGE TO ALL CONTACTING SURFACES. STORE THE TOOL IN THE PROTECTIVE CONTAINER.

### 6.6.9 TAPE PATH ALIGNMENT - TAKEUP

Refer to Figure 6-3 in conjunction with the following takeup alignment procedures.


Figure 6-3. Takeup Tape Path Alignment

### 6.6.9.1 Transport Preparation

(1) With tape loaded and the transport operationally ready, perform an unload operation (refer to Paragraph 3.5).

## NOTE

Tension arms are now properly positioned for removal of the overlay.
(2) Remove the head covers which enclose the head, tape guides, and tape cleaner by firmly grasping each cover and pulling out and away from the transport.
(3) Remove the supply reel from the supply hub.
(4) Remove the takeup reel from the takeup hub by loosening the two Phillips-head screws on the face plate of the hub.
(5) Remove the overlay as follows.

- Disconnect the power source from the transport.
- Remove the door stop screws from the deck casting.
- Remove the eight 4-40 flathead screws.
- Free the switch housing from the tape deck by removing the four mounting screws; access is made from the rear of the deck.
- From the rear of the tape deck, extend the slack in the cable harness through the access hole so that the switch housing is free of the tape deck.
- Rotate the switch housing to a position where the overlay can pass over the switch housing; remove the overlay.
- Temporarily return the switch housing to its operating position and secure in place. Ensure that the green wire from the power switch is grounded to the tape deck.

NOTE
Check that wiring to all switches is in place and is securely connected before applying power to the transport.

- Reinstall the supply and takeup reels. Torque the Phillips-head screws on the takeup hub to 2 inch-pounds after the reel is firmly seated on the hub.
(6) Insert a card with a nonreflective surface between the reflecting surface and sensing elements of the photosensor.
(7) Apply power to the transport.
(8) Depress and release the LOAD control; the tension arms will move into their operating positions and stop.
(9) Remove power from the transport.
(10) Remove the head guide caps; prevent loosening of the guide post retaining screws (from the rear of the transport) by engaging and holding an Allen wrench in the socket heads.
(11) Install the U-frame to the head guides using the thumbscrews.
- Pass the thumbscrew through the U-frame clearance hole and thread into the upper head guide.
- Pass the thumbscrew through the U-frame clearance hole and thread into the lower head guide.

CAUTION
ENSURE THAT THE MAGNETIC HEAD CABLE IS NOT DAMAGED BY THE EDGE OF THE U-FRAME DURING INSTALLATION.

### 6.6.10 TAKEUP ARM GUIDE ROLLER

6.6.10.1 Takeup Arm Guide Roller Height Check
(1) Install the crossbar to the U-frame by passing the thumbscrew through the U-frame clearance hole and thread it into the crossbar hole.
(2) Swing the takeup arm away from its stop to the center mark on the deck.
(3) Position the crossbar so contact is made between the bottom of the guide roller and the upper surface of the crossbar. Tighten the thumbscrew finger tight.
(4) Determine that the crossbar contacts the center of the tape traction area of the guide roller. If the crossbar is not centered, a guide roller height adjustment is required.
(5) Return the takeup arm to its rest position.

### 6.6.10.2 Takeup Arm Guide Roller Height Adjustment

If the takeup arm guide roller height check performed in Paragraph 6.6.10.1 indicates a height adjustment is required, proceed as follows.
(1) Swing the takeup arm away from its stop to the center mark on the tape deck.
(2) Position the crossbar so contact is made between the bottom of the guide roller and the upper surface of the crossbar. Tighten the thumbscrew finger tight.
(3) With the crossbar in place, loosen the takeup arm guide roller Allen-head screw located near the end of the tension arm (refer to Figure 6-3, view A-A).
(4) Center the tape traction area of the guide roller on the crossbar when the guide roller is positioned at the center mark on the deck.
(5) When the correct height is established, tighten the takeup Allen-head screw.

### 6.6.10.3 Takeup Arm Guide Roller Parallelism Check

Check the takeup arm guide roller parallelism as follows.
(1) Swing the takeup arm away from its stop to the center mark on the deck.
(2) Position the crossbar so contact is made between the tape traction area of the guide roller and the upper surface of the crossbar. Tighten the thumbscrew finger tight.
(3) Sight along the upper surface of the crossbar that is now in contact with the tape traction area of the guide roller. Observe an equal contact between the tape traction area of the guide roller and the upper surface of the crossbar.
(4) If a light path is observed between the two surfaces, an adjustment is required.

### 6.6.10.4 Takeup arm Guide Roller Parallelism Adjustment

If the takeup arm roller parallelism check performed in Paragraph 6.6.10.3 indicates an adjustment is required, proceed as follows.
(1) Engage the right-angle end of an Allen wrench in the head of the Allen-head screw on the takeup arm hub to prevent the screw from turning. Loosen the nut using an 11/32 wrench.
(2) Swing the takeup arm to a position where contact is made between the upper surface of the crossbar and the tape traction area of the guide roller. Tighten the thumbscrew finger tight.
(3) Sight along the upper surface of the crossbar that is now in contact with the tape traction area of the guide roller.
(4) Rotate the tension arm by inserting a small diameter rod into the hole in the takeup arm near the guide roller until the face of the guide roller and the contacting surface of the crossbar are parallel.
(5) Test by sighting between the two surfaces. Observe a minimum amount of light between the parallel surfaces.
(6) Torque the nut on the tension arm Allen-head screw to 20 inch-pounds, nominal.
(7) Recheck parallelism of the guide roller.

### 6.6.10.5 Takeup Hub Height Check

(1) Install an empty takeup reel on the takeup hub. Torque the two Phillips-head screws on the face of the hub to 2 inch-pounds.
(2) Position the crossbar between the flanges of the takeup reel. Locate the crossbar so the upper surface of the crossbar is in the same plane as the center line of the hub. Tighten the thumbscrew finger tight.
(3) Rotate the takeup reel and determine that the reel flanges are parallel to the crossbar.
(4) While rotating the reel, observe an equal clearance between the crossbar and the reel flanges. If the clearances are not equal, ensure that the reel flanges are not warped or distorted; also determine that the takeup reel is fully seated on the hub.
(5) If one edge of the crossbar is closed to one reel flange, the height of the hub must be adjusted.

### 6.6.10.6 Takeup Hub Height Adjustment

From the rear of the transport, locate the takeup reel bearing assembly which encloses the takeup reel hub bearings. Note that there is an access hole provided between the front and rear hub bearings. Through this hole observe the collar which secures the hub shaft in place. Rotate the shaft until an Allen-head setscrew appears. This setscrew is used to clamp the collar to the shaft which, in turn, establishes the height of the hub.

To adjust the takeup hub height, proceed as follows.
(1) Loosen the Allen-head screw located on the collar.
(2) With the crossbar in place between the flanges on the reel, adjust the hub so the reel flanges are equally spaced on either side of the crossbar.
(3) Tighten the Allen-head screw on the shaft collar.
(4) Recheck the clearance between reel flanges and the crossbar to ensure the clearances are equal.
(5) Loosen the thumbscrew to allow the crossbar to clear the reel flanges and remove the tape reel.

### 6.6.10.7 Capstan Height Check and Adjustment

(1) Reposition the crossbar between the capstan and the takeup bridge guide roller; align, and thread the thumbscrew into the U-frame clearance hole and the crossbar hole.
(2) Position the crossbar so that the lower surface contacts the tape transporting area of the capstan. Tighten the thumbscrew.
(3) Observe the contacting area between the crossbar and the tape transporting area. Observe an equal display of tape traction area on each side of the crossbar.
(4) If the capstan does not run true, replace the capstan.
(5) If the capstan requires centering to the left or right side of the crossbar, loosen the setscrew in the capstan hub and adjust the height to conform to the requirements of Step (3).

### 6.6.10.8 Takeup Bridge Roller Height Check

(1) Loosen the crossbar thumbscrew.
(2) Swing the crossbar upward so that the upper surface of the crossbar contacts the tape transporting area of the takeup bridge roller. Tighten the thumbscrew finger tight.
(3) Determine that the crossbar contacts the center of the tape traction area of the roller. If the roller is not centered on the crossbar, a height adjustment is required.

### 6.6.10.9 Takeup Bridge Roller Height Adjustment

When a height adjustment is required, proceed as follows.
(1) Loosen the thumbscrew and free the crossbar from the roller.
(2) From the rear of the transport, gain access through the deck to the Phillips-head screw which secures the roller standoff to the bridge. Loosen the screw and remove the standoff. Retain all original shims.
(3) Utilizing shims, reinstall and adjust the standoff to the bridge until the tape traction area of the roller is centered on the crossbar when the crossbar is contacting the tape transporting area of the roller.

NOTE
Tighten the standoff screw each time shims are removed or added.
6.6.10.10 Takeup Bridge Roller Parallelism Check and Replacement
(1) With the crossbar positioned where the upper surface of the crossbar contacts the tape transporting area of the takeup bridge roller, tighten the thumbscrew finger tight.
(2) Sight along the crossbar in contact with the roller. Observe an equal contact between the two surfaces.
(3) If a light path is observed between the two surfaces, replace the bridge roller assembly.

## NOTE

If replacement of the bridge roller assembly is made, repeat the height check in Paragraph 6.6.10.8.
6.6.10.11 Return Transport to Operational Status
(1) Remove the crossbar and U-frame from the transport and store in the protective case while not in use.
(2) Replace the caps on the head guides.
(3) Install a reel of tape on the supply hub and thread tape along the tape path and onto the takeup reel.
(4) Apply power to the transport; tape is now tensioned with the tension arms in the operating position.
(5) Perform an unload operation (refer to Paragraph 3.5).

NOTE
The tension arms are now properly positioned for installation of the overlay.
(6) Remove the supply and takeup reels from the transport.
(7) Replace the overlay.

- Remove power from the transport.
- From the rear of the tape deck, remove the mounting screws to free the switch housing.
- From the rear of the tape deck, extend the slack in the cable harness through the access hole so the switch housing is free of the deck.
- Rotate the switch housing to a position where the overlay can be passed over the switch housing.
- Press the overlay firmly against the tape deck.

NOTE
Check that wiring to all switches is in place and is securely connected before applying power to the transport.
(8) Install the supply and takeup reels. After the takeup reel is firmly seated on the hub, torque the Phillips-head screws on the takeup hub face plate to 2 inchpounds.
(9) Remove the protective covering from the recording surface of the head.
(10) Perform a general inspection of the transport for the presence of foreign material and for the condition of belts, wiring, and all connections.
(11) Replace the head covers.

### 6.6.11 TAPE PATH ALIGNMENT — SUPPLY

Refer to Figure 6-4 in conjunction with the following supply alignment procedures.

### 6.6.11.1 Transport Preparation

(1) With tape loaded and the transport operationally ready, perform an unload operation (refer to Paragraph 3.5).

## NOTE

Tension arms are now properly positioned for removal of the overlay.
(2) Remove the head covers which enclose the head, tape guides, and tape cleaner by firmly grasping each cover and pulling out and away from the transport.

CAUTION
PROTECT THE HEAD RECORDING SURFACE BYTAPING a pad of soft nonabrasive material over the HEAD.
(3) Remove the supply reel from the supply hub.
(4) Remove the takeup reel from the takeup hub by loosening the two Phillips-head screws on the face plate of the hub.
(5) Remove the overlay as follows.

- Disconnect the power source from the transport.
- Remove the door stop screws from the deck casting.
- Remove the eight 4-40 flathead screws.


Figure 6-4. Supply Tape Path Alignment

- Free the switch housing from the tape deck by removing the four mounting screws; access is made from the rear of the tape deck.
- From the rear of the tape deck, extend the slack in the cable harness through the access hole so the switch housing is free of the tape deck.
- Rotate the switch housing to a position where the overlay can pass over the switch housing; remove the overlay.
- Temporarily return the switch housing to its operating position and secure in place. Ensure that the green wire from the power switch is grounded to the tape deck.


## NOTE

Check that wiring to all switches is in place and is securely connected before applying power to the transport.

- Reinstall the supply and takeup reels. Torque the Phillips-head screws on the hub to 2 inch-pounds after the reel is firmly seated on the hub.
- Reconnect the transport to the power source.
(6) Insert a card with a nonreflective surface between the reflecting surface and sensing elements of the photosensor.
(7) Apply power to the transport.
(8) Depress and release the LOAD control; the tension arms will move into their operating positions and stop.
(9) Remove power from the transport.
(10) Remove the caps from the head guide. Prevent loosening of the guide post retaining screws (from the rear of the transport) by engaging and holding an Allen wrench in the socket heads.
(11) Install the U-frame to the head guide using thumbscrews.
- Pass the thumbscrews through the U-frame clearance holes and thread into the upper head guide.
- Pass a thumbscrew through the U-frame clearance hole and thread into the lower head guide.


## CAUTION

ensure that the magnetic head cable is not damaged by the edge of the u-frame during INSTALLATION.

### 6.6.12 SUPPLY ARM GUIDE ROLLER

6.6.12.1 Supply Arm Guide Roller Height Check
(1) Install the crossbar to the U-frame by passing the thumbscrew through U-frame clearance hole and thread into crossbar hole.
(2) Swing the takeup arm away from its stop to center mark on the deck.
(3) Position the crossbar so contact is made between the bottom of the guide roller and the upper surface of the crossbar. Tighten the thumbscrew finger tight.
(4) Determine that the crossbar contacts the center of the tape traction area of the guide roller. If the crossbar is not centered, a guide roller height adjustment is required.
(5) Return the supply arm to its rest position.

### 6.6.12.2 Supply Arm Guide Roller Height Adjustment

If the supply arm guide roller height check performed in Paragraph 6.6.12.1 indicates a height adjustment is required, proceed as follows.
(1) Swing the supply arm away from its stop to the center mark on the tape deck.
(2) Position the crossbar so contact is made between the bottom of the guide roller and the upper surface of the crossbar. Tighten the thumbscrew finger tight.
(3) With the crossbar in place, loosen the supply arm guide roller Allen-head screw located near the end of the tension arm (refer to Figure 6-4, view A-A).
(4) Center the tape traction area of the guide roller on the crossbar when the guide roller is positioned at the center mark on the deck.
(5) When the correct height is established, tighten the supply guide roller Allen-head screw.

### 6.6.12.3 Supply Arm Guide Roller Parallelism Check

Check the supply arm guide roller parallelism as follows.
(1) Swing the supply arm away from its stop to the center mark on the deck.
(2) Position the crossbar so contact is made between the tape traction area of the guide roller and the upper surface of the crossbar. Tighten the thumbscrew finger tight.
(3) Sight along the upper surface of the crossbar that is now in contact with the tape traction area of the guide roller. Observe an equal contact between the tape traction area of the guide roller and the upper surface of the crossbar.
(4) If a light path is observed between the two surfaces, an adjustment is required.

### 6.6.12.4 Supply Arm Guide Roller Parallelism Adjustment

If the supply arm roller parallelism check performed in Paragraph 6.6.12.3 indicates an adjustment is required, proceed as follows.
(1) Engage the right-angle end of an Allen wrench in the head of the Allen-head screw on the supply arm hub to prevent the screw from turning. Loosen the nut using an 11/32 wrench.
(2) Swing the supply arm to a position where contact is made between the upper surface of the crossbar and the tape traction area of the guide roller. Tighten the thumbscrew finger tight.
(3) Sight along the upper surface of the crossbar that is now in contact with the tape traction area of the guide roller.
(4) Rotate the tension arm by inserting a small diameter rod into the hole in the supply arm near the guide roller until the face of the guide roller and the contacting surface of the crossbar are parallel.
(5) Test by sighting between the two surfaces. Observe a minimum amount of light between the parallel surfaces.
(6) Torque the nut on the tension arm Allen-head screw to 20 inch-pounds, nominal.
(7) Recheck parallelism of the guide roller.

### 6.6.12.5 Supply Hub Height Check

(1) Install and firmly seat an empty supply reel on the supply hub. Lock the reel in place.
(2) Position the crossbar between the flanges of the supply reel. Position the crossbar so the upper surface of the crossbar is in the same plane as the center line of the hub. Tighten the thumbscrew finger tight.
(3) Rotate the supply reel and determine that the reel flanges are parallel to the crossbar.
(4) While rotating the reel, observe an equal clearance between the crossbar and the reel flanges. If the clearances are not equal, ensure that the reel flanges are not warped or distorted; also determine that the supply reel is fully seated on the hub.
(5) If one edge of the crossbar is closer to one reel flange, the height of the supply hub must be adjusted.

### 6.6.12.6 Supply Hub Height Adjustment

From the rear of the transport, locate the supply reel bearing assembly which encloses the supply reel hub bearings. Note that there is an access hole provided between the front and rear hub bearings. Through this hole, observe the collar which secures the hub shaft in place. Rotate the shaft until an Allen-head setscrew appears. This setscrew is used to clamp the collar to the shaft which, in turn, establishes the height of the hub. Adjust the supply hub height as follows.
(1) Loosen the Allen-head screw located on the collar.
(2) With the crossbar in place between the flanges on the reel, adjust the hub so the reel flanges are equally spaced on either side of the crossbar.
(3) Tighten the Allen-head screw on the shaft collar.
(4) Recheck the clearance between the reel flanges and the crossbar to ensure the clearances are equal.
(5) Loosen the thumbscrew and allow the crossbar to clear the reel flanges. Remove the tape reel.

### 6.6.12.7 Supply Bridge Roller Height Check

(1) Relocate the crossbar. Pass the thumbscrew through the clearance hole and thread into the crossbar hole.
(2) Swing the crossbar to a position where the upper surface of the crossbar contacts the tape transporting area of the supply bridge roller. Tighten the thumbscrew finger tight.
(3) Determine that the crossbar contacts the center of the tape traction area of the roller. If the roller is not centered on the crossbar, a height adjustment is required.

### 6.6.12.8 Supply Bridge Roller Height Adjustment

When a height adjustment is required, proceed as follows.
(1) Loosen the thumbscrew and free the crossbar from the roller.
(2) From the rear of the transport, gain access through the deck to a Phillips-head screw which secures the bridge roller to the standoff; loosen the screw and remove the standoff. Retain the shims.
(3) Using shims, reinstall and adjust the standoff to the bridge until the tape traction area of the roller is centered on the crossbar when the crossbar is contacting the tape transporting area of the roller.

NOTE
Tighten the standoff screw each time shims are removed or added.

### 6.6.12.9 Supply Bridge Roller Parallelism Check and Replacement

(1) Position the crossbar where the upper surface of the crossbar contacts the tape transporting area of the supply bridge roller. Tighten the thumbscrew finger tight.
(2) Sight along the crossbar in contact with the roller. Observe an equal contact between the two surfaces.
(3) If a light path is observed between the two surfaces, replace the bridge roller assembly.

## NOTE

If replacement of the bridge roller assembly is made, repeat the height check in Paragraph 6.6.12.7.

### 6.6.12.10 Supply Guide Roller Height Check

(1) Reposition the crossbar so the right side of the crossbar contacts the tape transporting area of the supply guide roller. Pass the thumbscrew through the U-frame clearance hole and thread into the crossbar hole.
(2) With the crossbar contacting the tape transporting area of the roller, tighten the thumbscrew finger tight.
(3) Determine that the crossbar contacts the center of the tape traction area of the roller. If the roller is not centered on the crossbar, a supply guide roller height adjustment is required.

### 6.6.12.11 Supply Guide Roller Height Adjustment

(1) Loosen the thumbscrew and swing the crossbar free of the supply guide roller.
(2) From the rear of the transport, gain access through the hole in the deck to a Phillips-head screw which secures the roller guide standoff to the deck. Remove the standoff and retain all original shims.
(3) Using shims, reinstall and adjust the standoff to the deck until the tape traction area of the guide roller is centered on the crossbar when the crossbar is contacting the tape transporting area of the roller. Tighten the roller guide Allenhead screw in the bushing.

### 6.6.12.12 Supply Guide Roller Parallelism Check and Replacement

(1) With the right side of the crossbar contacting the tape transporting area of the supply guide roller, tighten the thumbscrew finger tight.
(2) Sight along the crossbar in contact with the guide roller. Observe an equal contact between the two surfaces.
(3) If a light path is observed between the two surfaces, replace the roller assembly.

NOTE
If replacement of the guide roller assembly is made, repeat the height check in Paragraph 6.6.12.10.

### 6.6.12.13 Return Transport to Operational Status

(1) Remove the crossbar and U-frame from the transport and store in the protective case while not in use.
(2) Replace the caps on the head guides.
(3) Install a reel of tape on the supply hub and thread tape along the tape path and onto the takeup reel.
(4) Apply power to the transport; tape is now tensioned with the tension arms in the operating position.
(5) Perform an unload operation (refer to Paragraph 3.2.2).

NOTE
The tension arms are now properly positioned for installation of the overlay.
(6) Remove the supply and takeup reels from the transport.
(7) Replace the overlay.

- Remove power from the transport.
- From the rear of the tape deck, remove the mounting screws to free the switch housing.
- From the rear of the tape deck, extend the slack in the cable harness through the access hole so the switch housing is free of the deck.
- Rotate the switch housing to a position where the overlay can be passed over the switch housing.
- Press the overlay firmly against the tape deck.

NOTE
Align the screw holes for the switch housing, overlay and door stop prior to installing screws.

- Install the four mounting screws on the switch housing. Ensure that the green ground wire from the power switch is grounded to the tape deck

NOTE
Before applying power to the transport, check that wiring to all switches is in place and is securely connected.
(8) Install the supply and takeup reels. After the takeup reel is firmly seated on the hub, torque the Phillips-head screws on the takeup face plate to 2 inch-pounds.
(9) Remove the protective covering from the recording surface of the head.
(10) Perform a general inspection of the transport for the presence of foreign material and for the condition of belts, wiring, and all connections.
(11) Replace the head covers.
(12) Return the transport to operating status.

### 6.6.13 SKEW MEASUREMENT AND ADJUSTMENT (MODEL T8640A)

Transport skew is adjusted by first checking and, if necessary, adjusting write skew, then checking the read skew. The requirements on PE read skew are not severe since the system uses a multiple buffer register per channel for read data recovery.

### 6.6.13.1 Write Skew Measurement

An indication of the write skew may be obtained by observing the algebraic sum of the peak detectors at TP10 on the Data F PCBA with the write head connector plugged into the read head receptacle (J2) on the Data F PCBA.

Figure 6-5 illustrates an example of correctly adjusted skew. This method of determining the system write skew is accomplished as follows.
(1) Disconnect the write head and read head connectors from J1 and J2, respectively, on the Data F PCBA.
(2) Plug the write head connector into the read head connector (J2) on the Data F PCBA.
(3) Set the vertical sensitivity on the oscilloscope to $1.0 \mathrm{v} / \mathrm{cm}$.
(4) Set the oscilloscope to trigger on Channel 1 negative slope, alternate mode.
(5) Load an 800 -cpi master tape on the transport, bring to BOT, and activate the Maintenance switch so that tape moves in the forward direction.
(6) Observe oscilloscope waveform and adjust the horizontal time/division fixed and variable controls to display one complete cycle.

NOTE
With an 800-cpi tape, a half cycle represents 1250 uinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 major divisions; therefore $2500 \mu$ inch $\div 50$ divisions $=50 \mu$ inches/division.


Figure 6-5. Skew Waveform (Typical)
(7) Observe and note the fall time of the waveform viewed at TP10. This measurement should be taken between the 95 - and 5 -percent points of the waveform.
(8) Disconnect the write head connector from the read head receptacle (J2). Connect the write and read head connectors to J1 and J2, respectively, on the Data PCBA.
(9) Acceptable skew limits

- The maximum displacement between any two bits of a character when reading an IBM master tape using the write head in the T8640A transport is $200 \mu$ inches.
- The maximum displacement between any two bits of a character on an all ones tape written with the write section of the read-after-write head, and read with the read section of the read-after-write head is $400 \mu$ inches.


### 6.6.13.2 Write Skew Adjustment

To reduce skew to within acceptable limits, the following procedure is performed.
(1) Perform skew measurement procedure described in Paragraph 6.6.13.1, Steps (1) through (5).
(2) While observing the waveform at TP10 on the Data PCBA with tape moving in the forward direction, ease the edge of the tape off the head guide cap toward the spring-loaded washer. This should be done on first one guide, then the other.

NOTE
Moving the tape one- to two-thousandths of an inch from one of the guides will reduce skew to within the specified range.
(3) Observe the waveform and determine which movement (left guide or right guide) improves the display. If moving the tape off the left guide improved the display, the right guide should be shimmed.

> NOTE

The shims are burr-free, etched, one-half of a thousandths inch thick berrylium copper.
(4) Observe and note the fall time of the waveform observed at TP10.
(5) Since the character spacing at 800 cpi is $1250 \mu$ inches, the actual skew can be calculated. The skew correction provided by the addition of one shim (each shim is $500 \mu$ inches thick) is $500 \div 12=42 \mu$ inches. The number of shims used must satisfy the following.

- Skew must be reduced to a minimum consistent with the maximum number of shims allowable.
- Maximum number of shims used must not exceed four.


### 6.6.13.3 Read Skew Measurement

Measurement of read skew is accomplished by reading an all-ones or all-zeros tape with the read head connector plugged into the read head receptacle (J2) on the Data PCBA. This measurement is accomplished as follows.
(1) Set the vertical sensitivity of a Tektronix 561 oscilloscope (or equivalent) to $1.0 \mathrm{v} / \mathrm{cm}$.
(2) Set the oscilloscope to trigger on Channel 1, negative slope, alternate mode.
(3) Load an 800-cpi master tape on the transport; bring to BOT.
(4) Activate the Maintenance switch so that tape moves in the forward direction.
(5) Observe oscilloscope waveform and adjust the horizontal time/division fixed and variable controls to display one complete cycle.

## NOTE

With an 800-cpi tape, a half cycle represents 1250 uinches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 major divisions; therefore $2500 \mu$ inches $\div 50$ divisions $=50 \mu$ inches $/$ division.
(6) Observe and note the fall time of the waveform viewed at TP2. This measurement should be taken between the 95 - and 5 -percent points of the waveform.

### 6.6.14 SKEW MEASUREMENT AND ADJUSTMENT (MODEL T8660A)

Transport skew is adjusted mechanically as outlined in the following paragraphs. The requirements on PE read skew are not severe since the PE system uses a multiple buffer register per channel for read data recovery.

### 6.6.14.1 Skew Measurement

An indication of skew may be obtained by observing the algebraic sum of the peak detectors at TP10 on the Data G PCBA.

Figure 6-6 illustrates an example of correctly adjusted skew. This method of determining the system write head skew is accomplished as follows.
(1) Set the vertical sensitivity on the oscilloscope to $1.0 \mathrm{v} / \mathrm{cm}$.
(2) Set the oscilloscope to trigger on Channel 1 negative slope, alternate mode.
(3) Load an 800-cpi master tape on the transport; bring to BOT.
(4) Activate the Maintenance switch so that tape moves in the forward direction.
(5) Observe oscilloscope waveform and adjust the horizontal time/division fixed and variable controls to display one complete cycle.

NOTE
With an 800-cpi tape, a half cycle represents $1250 \mu$ inches. The scope graticule is divided into 10 major divisions, each of which is divided into 5 major divisions; therefore $2500 \mu$ inches $\div 50$ divisions $=50 \mu$ inches $/$ division.


Figure 6-6. Skew Waveform (Typical)
(6) Observe that the fall time of the waveform viewed at TP10 is less than eight small divisions of the oscilloscope graticule, i.e., $200 \mu$ inches. This measurement should be taken between the 95 -and 5-percent points of the waveform.
(7) Acceptable skew limits

- The maximum displacement between any two bits of a character when reading an IBM master tape using the write head in the T8660A transport is $200 \mu$ inches.
- The maximum displacement between any two bits of a character on an all-ones tape written with the write section of the read-after-write head, and read with the read section of the read-after-write head is $400 \mu$ inches.


### 6.6.14.2 Skew Adjustment

Reduction of skew to within acceptable limits is accomplished as follows.
(1) Perform skew measurement procedure described in Paragraph 6.6.14.1.
(2) While observing the waveform at TP10 on the Data PCBA with tape moving in the forward direction, ease the edge of the tape off the head guide cap toward the spring-loaded washer. This should be done on first one guide, then the other.

NOTE
Moving the tape one- to two-thousandths of an inch from one of the guides will reduce skew to within the specified range.
(3) Observe the waveform and determine which movement (left guide or right guide) improves the display. If moving the tape off the left guide improved the display, the right guide should be shimmed.

NOTE
Moving the tape one- to two-thousandths of an inch from one of the guides will reduce skew to within the specified range.
(4) Observe and note the fall time of the waveform observed at TP10 with the oscilloscope set up as described in Paragraph 6.6.14.1, Step (5).
(5) Since the character spacing at 800 cpi is $1250 \mu$ inches, the actual skew can be calculated. The skew correction provided by the addition of one shim (each shim is $500 \mu$ inches thick) is $500 \div 12=42 \mu$ inches. The number of shims used must satisfy the following.

- Skew must be reduced to a minimum consistent with the maximum number of shims allowable.
- The maximum number of shims used must not exceed four.

Therefore, if, for example, the measured skew is 250 inches, four shims will yield a skew correction of $168 \mu$ inches (i.e., $4 \times 500 \div 12=168 \mu$ inches). This satisfies the requirements listed above.
(6) Move the Maintenance switch to the stop position.
(7) Remove the head guide retaining screw (accessible from the rear of the deck) and remove the guide.

NOTE
When removing the guide, care should be taken not to drop the spring and washer.
(8) Insert the required number of shims and replace the head guides.

## NOTE

Shim only one head guide.
(9) Recheck skew measurement as described in Paragraph 6.6.14.1.

### 6.6.15 HEAD REPLACEMENT

The head may require replacement because of internal faults, faulty cabling, or from wear. Internal faults can be verified by reading a master tape; wear can be verified by measuring the depth of the wear pattern on the head crown. On heads having guttering (grooves cut on the crown on either side of the tape path) the head should be replaced. Replacement should take place when the guttering is worn down to a depth in excess of 0.010 inch. In those heads showing guttering, the head wear should be measured with a brass shim that is ten-thousandths of an inch thick. The shim width should be less than the minimum tape width ( 0.496 inch). The shim is placed in the worn area of the head crown with one side butted against the worn step. When the upper surface of the shim is below the unworn surface of the head crown (i.e., the head has worn to a depth greater than 0.010 inch ) the head should be replaced.

When a head is installed it is adjusted to 12 degrees for a dual-stack head, or 9 degrees for a single-stack head. These angles are in respect to the tape path when the tape is at operating tension.

Positioning the head can easily be accomplished if a cardboard or plastic template with the appropriate angle is constructed as shown in Figure 6-7.

### 6.6.15.1 Head Removal

Removal of the head is accomplished as follows.
(1) Remove the head covers.
(2) Disconnect the head connector(s) from the Data PCBA.
(3) Remove the two screws that attach the head to the deck.
(4) Ease the head cable(s) through the deck.


Figure 6-7. Head Alignment Template

### 6.6.15.2 Head Replacement

(1) Check the replacement head for particles adhering to the mounting surface.

NOTE
The mounting surface must be free of all foreign substances or excessive skew will result.
(2) Route the head connector(s) and cable(s) through the deck.
(3) Install the head using the two screws removed in Step (3) of Paragraph 6.6.15.1; do not fully tighten the screws.

NOTE
Two sets of screw holes are provided for mounting the head. The set nearest the capstan is used for dual-stack heads [T8640A]; the other set is used for single-stack heads [T8660A].
(4) Load an all-ones tape on the transport.
(5) Bring tape to Load Point by depressing and releasing the LOAD control twice.
(6) Position the crown of the head so contact is made with the tape that is now under operating tension.

NOTE
Ensure the full width of the tape is in contact with the magnetic head laminations.
(7) Place the template (Figure 6-7) in the position shown in Figure 6-8 or 6-9 for single- or dual-stack transports, respectively.

NOTE
It will be necessary to remove the photosensor, the tape-in-path reflector, and the tape cleaner when a head is aligned.
(8) Rotate the head until the narrow surface of the template is in full contact with the tape.
(9) Tighten the head screws sufficiently to maintain head-to-tape alignment.
(10) Recheck the head-to-tape alignment and remove the template.
(11) Torque the headscrews to four inch-pounds.


Figure 6-8. Single-Stack (9-degree) Head-to-Tape Positioning


Figure 6-9. Dual-Stack (12-degree) Head-to-Tape Positioning
(12) Replace the photosensor, the tape-in-path reflector, and the tape cleaner.
(13) Replace the head connectors.

- For dual-stack transports, plug the write head connector into J1 and the read head connector into J2 on the Data PCBA.

NOTE
The read head is the one farthest from the erase head and nearest the takeup reel.

- For single-stack transports, plug the head connector into J1 on the Data PCBA.


### 6.6.15.3 Head Operation Test

(1) Set the all-ones tape in motion and set all read amplifier gains as described in Paragraph 6.5.8.
(2) Operate the transport in a shuttling mode, i.e., forward, then reverse, by actuating the Forward-Reverse switch on the Tape Control PCBA; observe the oscilloscope signal amplitude at the output of the read amplifiers. While operating in the shuttling mode, physically adjust the head assembly until the observed amplitude difference between forward and reverse operation is at a minimum.
(3) Check the read skew, write skew, and flux gate (T8640A only), as described in Paragraphs 6.6.13 or 6.6.14 and 6.6.17, respectively. Output waveforms should approach that shown in Figure 6-5.
(4) Torque the head screws to four inch-pounds.
(5) Rewind tape to the supply reel and remove the reel.
(6) Replace the head covers.

### 6.6.16 BOT/EOT SENSOR ASSEMBLY REPLACEMENT

Removal and replacement of the BOT/EOT sensor is accomplished as follows.
(1) Remove the head covers.
(2) From the rear of the transport, disconnect the wiring harness plug from the photosensor cable.
(3) Remove the screw that retains the sensor assembly.
(4) Remove the pins from the plug by using a Molex extractor tool; remove the cable through the hole in the deck.
(5) Insert the new photosensor cable through the deck.
(6) Replace the connector pins, using the Molex tool, as follows.

- Brown wire - pin 1
- Red wire - pin 2
- Orange wire - pin 3
- Yellow wire - pin 4
- Green wire - pin 5
- Blue wire - pin 6
(7) Measure the output of the BOT and EOT amplifiers as described in Paragraph 6.5.3.2.


### 6.6.17 FLUX GATE ADJUSTMENT (MODEL T8640A ONLY)

Crosstalk can be checked and, if necessary, reduced to within acceptable limits by mechanically positioning the flux gate. The check and adjustment procedure is accomplished as follows.
(1) Load a reel of tape with a write enable ring installed on the transport. Do not pass tape over the capstan.
(2) Apply power to the transport.
(3) Bring the transport to the Load Point by placing a white card between the tape and photosensor assembly and depressing the LOAD control.
(4) Place the transport on-line.
(5) Write a block of all-ones tape (refer to Paragraph 6.5.8.4 for generation of an allones tape).
(6) Observe waveform on any test points between TP104 and TP904 on the Data PCBA.

NOTE
Synchronize the oscilloscope with a suitable signal such as IWDS or SFC at the signal interface. Observe the crosstalk on the Read waveform by using the oscilloscope magnifier or delayed function.
(7) Observe that the waveforms viewed in Step (6) are approximately sinusoidal with no pronounced peaks. The crosstalk should be maintained at the lowest possible level and should not exceed $1.0 v$ peak-to-peak.

## NOTE

If the observed waveforms in Step [6] fall within the limit specified in Step [7], no adjustment should be attempted.
(8) Place a white card approximately 0.005 -inch thick (e.g., business card) between the flux gate and the magnetic head; press the flux gate assembly lightly against the head. Adjust the spacing screw on the base of the flux gate until a gap width of 0.005 -inch minimum is established.
(9) Figure 6-10 illustrates the correct relationship between the magnetic head and flux gate.

NOTE
It may be necessary to move or rotate the assembly slightly to achieve the best compromise between all tracks.
(10) Tighten the flux gate assembly screws and repeat Steps (1) through (7).

CAUTION
ensure adequate clearance between the FLUX GATE AND THE MAGNETIC HEAD [0.005 INCH MINIMUM]. FAILURE TO ALLOW CORRECT CLEARANCE WILL RESULT IN DAMAGE TO THE HEAD OR TAPE.

### 6.6.18 CAPSTAN MOTOR REPLACEMENT

Removal and replacement of the capstan motor is accomplished as follows.
(1) Disconnect the motor leads: if the motor has terminals, disconnect the leads at the motor and tachometer terminals; if the motor does not have terminals, disconnect the motor connector from the main cable assembly.
(2) Remove the capstan from the old motor.
(3) Remove the overlay; refer to Paragraph 6.6.9.1, Steps (1) through (5).


Figure 6-10. Flux Gate Adjustment
(4) Remove the screws holding the capstan motor to the deck. Note the presence of any shims as they may be reused to maintain the angularity of the motor shaft to the tape path.
(5) Mount the replacement motor.

NOTE
The mounting surface must be free of any foreign objects in order that perpendicularity of the capstan to the tape path can be accomplished.
Alternately tighten the three retaining screws and torque to 16 inch-pounds.
(6) Reinstall the motor leads and/or harness connector.

NOTE
To ensure effective filtering, the RFI filter must be firmly secured by the tie wrap or clamp to the frame of the motor.
(7) Reinstall the overlay (refer to Paragraph 6.6.9.11).
(8) Load takeup and supply reels with a work tape installed on the transport.
(9) Adjust the back edge of the capstan to approximately 0.25 -inch above the surface of the overlay.
(10) Establish capstan position on the motor shaft by moving tape first in the reverse and then in the forward direction. Observe the tape tracking around the periphery of the capstan. If tape skewing or capstan walk are observed, raise or lower the capstan on the shaft or adjust the shims on the motor mounting surfaces so that capstan walk is less than 0.005 -inch.
(11) Adjust the tape speed and rewind speed as described in Paragraphs 6.5.6 and 6.5.7, respectively.
(12) Perform a check of the read system skew as described in Paragraph 6.6.13, or 6.6.14.

### 6.6.19 REEL MOTOR BELT TENSION

The toothed belts that couple the reel motors to the hubs must have sufficient tension to prevent the teeth from skipping or servo instability due to backlash may result. However, the belts must not have excessive tension as this will overload the reel motors and reel shaft bearings.

### 6.6.19.1 Belt Tension Adjustment Procedure

The belt tension is adjusted as follows.
(1) Loosen the three screws that fasten the motor mounting plate to the deck standoffs.

NOTE
Slots in the motor mounting plate allow rotation of the motor to adjust belt tension.
(2) Adjust the motor mounting so the belt is snug. Note the last tooth of the belt that is completely seated in a slot on the large pulley (refer to Figure 6-11).


Figure 6-11. Reel Servo Belt Tension Adjustment
(3) Count two to three slots forward from the last engaged tooth. Hold the large pulley to ensure that it does not turn. Depress the belt at the point between the second and third teeth with sufficient force to deflect the belt flush against the pulley.

CAUTION
do not apply excessive force on the toothed $B E L T$.
(4) Adjust the motor assembly so the second tooth is firmly engaged in a slot on the large pulley but the third tooth of the belt is not engaged.
(5) Tighten the three screws on the reel motor mounting plate and recheck for the condition in Step (2).

### 6.6.20 TAPE TENSION

Tape tension around the tape path is controlled by individual springs connected to the tape deck and to the tension arms.

NOTE
When performing a tape tension check, it is not necessary to remove the overlay. If a tension adjustment is required, the overlay must be removed [refer to Paragraph 6.6.9.1].

### 6.6.20.1 Supply Tape Tension Check

When checking tape tension, it is necessary to move the tension arm through its operating range. The tension arm can be moved into the operating region only by applying power and bringing the transport to the load condition. Refer to Figure 6-12 in conjunction with the following procedure.

## CAUTION

NEVER EXERT PRESSURE ON A TENSION ARM ROLLER When attempting to move a tension arm into the operating region from the load position. dAMAGE TO THE ARM RETRACTOR ASSEMBLY OR TO the roller guide shaft may result.


Figure 6-12. Supply Tape Tension Adjustment
(1) Remove both tape reels.
(2) Block the light path to the Tape In Path (TIP) reflector.
(3) Depress and release the LOAD control.
(4) When the arms have reached the end of their operating range, remove power from the transport.
(5) Prepare a 6 -inch piece of $1 / 2$-inch magnetic recording tape with loops at each end.
(6) Thread tape about the guide rollers and the supply arm roller, as shown in Figure 6-12.
(7) Hold a calibrated 16-ounce force gauge in the position shown in Figure 6-12. Maintain the tape to supply reel hub distance as shown.
(8) With an even pull on the tape, exert enough force to bring the supply arm guide roller to the first operating mark on the tape deck. Verify that the force gauge indicates 7.5 ounces.
(9) Continue to pull on the tape until the supply arm reaches the end operating mark on the tape deck. Verify that the force gauge indicates 9.5 ounces.
(10) If the tape tensions required in Steps (8) and (9) cannot be met, perform the following adjustment.

### 6.6.20.2 Supply Tape Tension Adjustment

To adjust the tape tension, the overlay must be removed and the location of the spring adjusting bracket changed.
(1) Remove the overlay; refer to Paragraph 6.6.9.1, Steps (1) through (5).
(2) With the tape positioned as described in Paragraph 6.6.20.1, bring the supply arm roller from the rest position to the first operating mark on the tape deck. Holding the supply arm roller in this position, slightly loosen the anchor bracket screws and adjust the tape pull to 7.5 ounces and tighten the anchor bracket screws.
(3) Further extend the pull on the tape until the end operating mark is reached. Verify that the force gauge indicates 9.5 ounces.
(4) Repeat Steps (2) and (3), as required.
(5) Apply a slight amount of Bendix brake lubricant or Lubriplate to each end of the spring and clevis pin.
(6) Remove the tape loop and force gauge.
(7) Replace the overlay and return the transport to operating condition (refer to Paragraph 6.6.9.11).

### 6.6.20.3 Takeup Tape Tension Check

When checking tape tension, it is necessary to move the tension arm through its operating range. The tension arm can be moved into the operating region only by applying power and bringing the transport to the load condition. Refer to Figure 6-13 in conjunction with the following procedure.

## CAUTION

NEVER EXERT PRESSURE ON A TENSION ARM ROLLER WHEN ATtEMPTING TO MOVE A TENSION ARM INTO the operating region from the load position. DAMAGE TO THE ARM RETRACTOR ASSEMBLY OR TO the ROLLER GUIDE SHAFT MA Y RESULT.
(1) Remove both tape reels.
(2) Block the light path to the Tape In Path (TIP) reflector.
(3) Depress and release the LOAD control.
(4) When the arms have reached the end of their operating range, remove power from the transport.
(5) Prepare a 6 -inch piece of $1 / 2$-inch magnetic recording tape with loops at each end.
(6) Thread tape about the guide rollers and takeup arm roller as shown in Figure 6-13.


Figure 6-13. Takeup Tape Tension Adjustment
(7) Hold a calibrated 16-ounce force gauge in the position shown in Figure 6-13. Maintain the tape to takeup supply reel hub distance as shown.
(8) With an even pull on the tape, exert enough force to bring the takeup arm guide roller to the first operating mark on the tape deck. Verify that the force gauge indicates 7.5 ounces.
(9) Continue to pull on the tape until the takeup arm reaches the end operating mark on the tape deck. Verify that the force gauge indicates 9.5 ounces.
(10) If the tape tensions required in Steps (8) and (9) cannot be met, perform the following adjustment.

### 6.6.20.4 Takeup Tape Tension Adjustment

To adjust the tape tension, the overlay must be removed and the location of the spring adjusting bracket changed.
(1) Remove the overaly; refer to Paragraph 6.6.9.1, Steps (1) through (5).
(2) With the tape positioned as described in Paragraph 6.6.20.3, bring the takeup arm roller from the rest position to the first operating mark on the deck. Holding the takeup arm roller in this position, slightly loosen the anchor bracket screws and adjust the tape pull to 7.5 ounces and tighten the anchor bracket screws.
(3) Further extend the pull on the tape until the end operating mark is reached. Verify that the force gauge indicates 9.5 ounces.
(4) Repeat Steps (2) and (3) as required.
(5) Apply a slight amount of Bendix brake lubricant or Lubriplate to each end of the spring and clevis pin.
(6) Remove the tape loop and force gauge.
(7) Replace the overlay and return the transport to operating condition (refer to Paragraph 6.6.9.11).

### 6.6.21 SUPPLY REEL HUB REPLACEMENT

Removal and replacement of the supply reel hub is accomplished as follows.
(1) From the rear of the transport, loosen the two setscrews which hold the belt driven gear pulley on the shaft.
(2) Slide the gear pulley off the shaft; the toothed belt will disengage from the gear pulley.
(3) Loosen the setscrew on the shaft collar.
(4) Rotate the hub and align the setscrew with the access hole.
(5) From the front of the transport, withdraw the hub.
(6) Install the replacement hub assembly. Ensure the lineup of each setscrew to the flat surface on the hub shaft.
(7) Proper hub height must be ensured; refer to Paragraphs 6.6.12.5 and 6.6.16.6 for check and adjustment procedures.
(8) Proper write lockout plunger height must be ensured; refer to Paragraph 6.6.24.

### 6.6.22 TAKEUP REEL HUB REPLACEMENT

Removal and replacement of the takeup reel is accomplished as follows.
(1) Remove the takeup reel by loosening the two Phillips-head screws on the face plate of the hub.
(2) From the rear of the transport, loosen the two setscrews which hold the belt driven gear pulley on the shaft.
(3) Slide the gear pulley off the shaft; the toothed belts will disengage from the gear pulley.
(4) Loosen the setscrew on the shaft collar.
(5) Rotate the hub and align the setscrew with the access hole.
(6) From the front of the transport, withdraw the hub.
(7) Install the replacement hub assembly. Ensure the lineup of each setscrew to the flat surface on the hub shaft.
(8) Proper hub height must be ensured; refer to Paragraphs 6.6.10.5 and 6.6.10.6 for check and adjustment procedures.

### 6.6.23 SUPPLY REEL HUB EXPANSION RING ADJUSTMENT

Adjustment of the supply hub expansion ring is required when a supply reel hub is replaced, or when reel slippage is noted. Adjustment of the ring is accomplished as follows.
(1) Place the quick-release latch in the unload position.
(2) Load a reel of tape on the transport.
(3) Lock the quick-release latch by depressing the indented portion of the hub.
(4) Using a suitable force gauge, exert pressure at the center of the indented latch. If the force required to release the latch is less than 6 pounds, the expansion ring requires adjustment.
(5) Insert an Allen wrench into the adjustment hole located in the center of the hub and turn one-quarter turn clockwise.
(6) Repeat Steps (4) and (5) until the force required to release the latch is 6 pounds.

### 6.6.24 WRITE LOCKOUT ASSEMBLY

When the supply reel hub or the write lockout assembly are replaced, the write lockout plunger may require adjustment. The plunger height should be adjusted so that when the plunger is fully retracted, the plunger end is just flush with the back side of the reel hub flange. Adjustment may be accomplished by removing the write lockout assembly, loosening the safety nut and rotating the plunger adjusting screw to the desired position. The safety nut is then tightened.

### 6.6.25 TAPE CLEANER CLEANING AND REPLACEMENT

### 6.6.25.1 Removal of Tape Cleaner

(1) Remove the head covers to gain access to the tape cleaner.
(2) Remove the Allen-head screws securing the tape cleaner to the deck.

### 6.6.25.2 Cleaning Tape Cleaner

(1) Remove the two machine screws securing the perforated mesh to the tape cleaner mounting post.
(2) Gently push the perforated mesh forward and away from the body of the tape cleaner.
(3) Clean the cavity of the tape cleaner with a cotton swab moistened with $91 \%$ isopropyl alcohol. Clean the perforated mesh.
(4) Inspect the perforated mesh for excessive wear or rough areas that could cause tape damage. Ensure that all holes in the mesh are free of contamination.
(5) Replace the mesh on the body of the tape cleaner and ensure that it is fully seated. Replace the two machine screws.
(6) Perform the installation and alignment procedures in the following paragraphs.

### 6.6.25.3 Installation of Tape Cleaner

(1) Ensure all surface areas on the tape cleaner and deck casting are free of contamination.
(2) Insert the captive tape cleaner dowel pin into the dowel pin hole. Replace the retaining screws and secure the tape cleaner to the deck.

### 6.6.26 TAPE-IN-PATH (TIP) REFLECTOR ADJUSTMENT

It is important to note that the Tape-In-Path (TIP) reflector adjustment is to be performed after the head and the tape cleaner are aligned, and the BOT/EOT Sensor has been removed. Refer to Figure 6-14 in conjunction with the following procedure.
(1) Install the TIP refluctor in place; do not tighten the retaining screws.
(2) Position the TIP adjustment tool so that the step side contacts, and is parallel to both the head and the tape cleaner.
(3) With the adjustment tool held in place, slide the TIP reflector along the slots until the reflecting surface touches the step portion of the tool. Tighten the retaining screws.
(4) Remove the TIP adjustment tool and install the BOT/EOT Sensor Assembly as described in Paragraph 6.6.16.
(5) Align and check the BOT/EOT Sensor as described in Paragraph 6.5.3.


Figure 6-14. Tape-In-Path (TIP) Reflector Adjustment

### 6.7 MAINTENANCE TOOLS

The following list of tools is required to maintain the tape transport. All tools, except items 17 and 18, may be obtained from a local source.
(1) Hex socket key set 0.050 through $5 / 32$ sizes.
(2) Splined drive socket key for a 4-40 setscrew.
(3) Long-nose pliers.
(4) Phillips screwdriver set.
(5) Standard blade screwdriver set.
(6) Open-end wrenches, sizes $3 / 16,1 / 4,5 / 16$, and $3 / 8$.
(7) Soldering aid.
(8) Soldering iron.
(9) One-pound force gauge.
(10) Ten-pound force gauge.
(11) Lint-free cloth.
(12) Cotton swabs.
(13) $91 \%$ Isopropyl alcohol.
(14) Torque wrench, 0-35 in/lbs.
(15) Molex pin extractor (Mfg. Part No. HT2285).
(16) Loctite Sealant, Grade C.
(17) Tape Path Alignment Tool, PERTEC Part No. 102381-01.
(18) TIP Reflector Adjustment Tool, PERTEC Part No. 104830.

### 6.8 TROUBLESHOOTING

Table 6-6, System Troubleshooting chart, provides a means of isolating faults, possible causes, and remedies. The troubleshooting chart should be used in conjunction with the schematics and assembly drawings at the end of Section VII.

Table 6-6

## System Troubleshooting

| Symptom | Probable Cause | Remedy | Reference |
| :--- | :--- | :--- | :--- |
| Tape does not tension <br> and the capstan shaft <br> rotates freely when the <br> LOAD control is de- <br> pressed for the first <br> time after the arms <br> have moved down. | Interlock relay K1 does <br> not close. | LOAD control is not <br> operative. | Check relay operation. <br> Replace if necessary. |
| Relay driver defective. | Check control operation. <br> Replace if necessary. | Paragraph 5.4 |  |

Table 6-6
System Troubleshooting (Continued)

| Symptom | Probable Cause | Remedy | Reference |
| :---: | :---: | :---: | :---: |
| Tension arms hit interlock switches at rewind. | Relay K2 does not latch. | Check relay for faulty contacts. Check U51. | Paragraph 5.4.1.2 |
| At rewind after BOT, the arms do not move down 2 and 2-1/2 inches. | AOS and ULOS signals missing. | Check output of U16D and U16C on Tape Control PCBA. | Paragraph 5.4 |
| Tape runs past the BOT marker. | BOT tab is dirty or tarnished. | Replace tab. | Paragraph 6.6.16 |
|  | Photosensor does not operate. | Replace photosensor. | Paragraph 6.6.16 |
|  | Photosensor or amplifier defective. | Check for appropriate voltage levels in sensor systems with tab not over photosensor. Check for appropriate voltage levels in sensor systems with tab over photosensor. | Paragraph 6.5.3 |
|  | Logic fault (Load flipflop does not reset). | Replace or repair Tape Control PCBA. | Paragraph 5.4 |
| Transport does not move in response to SYNCHRONOUS FORWARD or SYNCHRONOUS REVERSE commands. | Interface cable or receiver faulty. | Check levels at outputs and inputs of receivers on Tape Control PCBA. Replace or repair cable or Tape Control PCBA. | Paragraph 5.4 |
|  | Transport is not Ready. | Replace or repair Tape Control PCBA. | Paragraph 5.4 |
|  | Fault in ramp generator or capstan servo amplifier. | Check TP20 on Tape Control PCBA. Replace or repair Tape Control PCBA. | Paragraph 5.4 |
| Transport responds to SYNCHRONOUS FORWARD command, but tape is not written. | Write current is not enabled. | Check for Write Enable ring on supply reel, WRT EN indicator should be lit. Check TP18 on Tape Control PCBA (should be $+5 v$ for writing). Replace Write Lockout assembly if faulty. Check that WRT POWER level is $+5 v$ on Data PCBA. | Paragraph 5.2 or 5.3, 5.4 |
|  | Write status or MOTION signal to Data PCBA is not correct. | Check receiver on Tape Control PCBA for WRITE status and on Data PCBA for WRITE status. |  |
|  |  | Check Data PCBA for MOTION signal. Replace or repair Data PCBA or Tape Control PCBA if faulty. |  |
|  | WRITE DATA or WRITE DATA STROBE is not received correctly on Data PCBA from interface. | Check for correct levels on Data PCBA. Replace or repair Data PCBA or interface cable if faulty. | Paragraph 5.2 or 5.3, 5.4 |
|  | Heads not plugged in correctly. | Check J1 or J2 on Data PCBA. |  |

Table 6-6
System Troubleshooting(Continued)

| Sympton | Probable Cause | Remedy | Reference |
| :---: | :---: | :---: | :---: |
| Data are incorrectly written. | Incorrect data format. | Use correct format. | IBM Form <br> A22-6589-3 <br> (729 or 727 Series) <br> IBM Form <br> A22-6866-3 <br> ( 2400 Series) |
|  | Write deskew circuit faulty. | Check TP10 on Data E71 E9 or TP8 on E17/E19 for sequence of 10 pulses for each WDS. Replace Data PCBA if necessary. | Paragraph 5.2 or 5.3 |
|  | Fault on one track due to failure in write circuits. | Check receiver and write amplifier on Data PCBA. Replace or repair Data PCBA if faulty. | Paragraph 5.4 |
|  | Signal intermittent on WRT POWER, WRITE, MOTION, or WARS. | Check the signals and replace or repair Tape Control PCBA or Write Lockout Assembly. | Paragraph 5.4 |
| Correct tape cannot be read. | Interface cable or transmitter faulty. | Replace or repair interface cable or Data PCBA. | Paragraph 5.2 or $5.3$ |
|  | Head is not plugged in. | Check J1 or J2 on Data PCBA. | - |
|  | Tape tracking on skew is badly adjusted. | Readjust according to description in Section VI. | Paragraph 6.6.13 or $6.6 .14$ |
|  | Head, guides, and tape cleaner need cleaning. | Clean head, guides, and tape cleaner. | $\begin{aligned} & \text { Paragraph 6.3.1, } \\ & 6.6 .25 \end{aligned}$ |
|  | Read amplifier gains are adjusted incorrectly. | Check and adjust amplifier gains. | Paragraph 6.5.8 |
|  | Faulty write amplifier causes current to be passed through head while reading. | Check write amplifier output test points and replace or repair Data PCBA if faulty. | Paragraph 5.2 or $5.3$ |
|  | Component fault in read channel. | Check test points on Data PCBA. Replace or repair Data PCBA. |  |
|  | Envelope detector delays are incorrect. | Check TP106-TP906 on Data PCBA for correct on and off times. Replace or repair Data PCBA. | Paragraph 5.2 or $5.3$ |
|  | Threshold level incorrect. | Check level at TP6 on Data PCBA. Replace or repair Data PCBA. | Paragraph 6.5.9 or 6.5.10 |

## SECTION VII PARTS LIST, LOGIC LEVELS AND WAVEFORMS, AND SCHEMATICS

### 7.1 INTRODUCTION

This section includes illustrated parts lists, logic level and waveform definitions, interconnect lists, and schematic and assembly drawings.

### 7.2 ILLUSTRATED PARTS BREAKDOWN (IPB)

Figures 7-1 through 7-3, used in conjunction with Tables 7-1 through 7-3, respectively, provide identification by PERTEC part number of the mechanical and electrical components of the T8000A Series Tape Transports.

When part numbers for a particular part differ due to a change in transport configuration, descriptions and part numbers for all configurations are listed.

### 7.3 RECOMMENDED SPARE PARTS

Table 7-4 provides a list of the recommended subassembly spare parts for the T8000A Series Tape Transports. The Customer should always furnish the model number and the serial number of the disk drive when ordering parts.

An additional recommended spare parts list containing the part number, description, current price for component parts, subassembly parts, and special tools is also available. This list can be obtained by providing the unit part number from the ID label on the drive to the Spares Product Management, PERTEC, 9600 Irondale Avenue, Chatsworth, CA 91311.

### 7.4 PART NUMBER CROSS REFERENCE

Table 7-5 provides a cross reference to the manufacturer's part number from typical PERTEC part numbers.

### 7.5 PCBA INTERCONNECTIONS

Interconnections between PCBAs installed in the transports are listed in Table 7-6.

### 7.6 LOGIC LEVELS AND WAVEFORMS

The transport control and interface logic uses the DTL800 series of logic elements. Logic levels are: +5.0 v - logical true; +0.4 v - logical false.

All basic waveform names are chosen to correspond to the logical true condition, e.g., SET WRITE STATUS (ISWS) enables the write circuits when it is logically true ( +5.0 v ), or disables the write circuits when it is logically false ( 0 v ).

The inverse of a waveform is denoted by the prefix ' N '. Therefore, NBOT will be 0.4 v when the BOT tab is under the photosensor head, or +5.0 v otherwise.

All interface lines connecting the transport to the controller are prefixed by 'l'. Each line must be terminated at the receiver end of the cable by a $220 / 330$-ohm divider chain between +5.0 v and 0 v .

All interface waveforms are low-true. Their logic levels are: +3.0v - logical false; +0.4 v - logical true. For example, ISFC (SYNCHRONOUS FORWARD command) will be +0.4 v when the transport is being driven in the forward direction, or +3.0 v otherwise.

The Glossary contains the waveform mnemonics referred to in this manual.


Figure 7-1. T8000A Series Transports, Photo Parts Index (Front View)

Table 7-1
T8000A Series Transports, Photo Parts Index

| Figure and Index No. | Part Number | Description |
| :---: | :---: | :---: |
| Figure 7-1 |  |  |
| -1 | 103347-01 | Tension Arm |
| -2 | 103544-01 | Tension Arm Spring |
| -3 | 102261-02 | Supply Reel Hub Assembly |
| -4 | 103382-02 | Deck Mounting Hinge |
| -5 | 103338-01 | Deck Mounting Hinge |
| -6 | 103384-01 | Spring Anchor Bracket |
| -7 | 667-0017 | Rubber Cushion |
| -8 | 100808-03 | Tension Arm Roller Guide Assembly |
| -9 | 103343-02 | Take-up Reel Hub Assembly |
| -10 | 103939-01 | Rear Head Cover |
| -11 | 103938-01 | Front Head Cover |
| -12 | 103351-01 | Bridge Plate |
| -13 | 101744-* | Strobe Disk |
| -14 | $\begin{aligned} & 103352-01 \\ & 103353-01 \end{aligned}$ | Capstan $\leq 25 \mathrm{ips}$ <br> Capstan >25ips |
| -15 | 101026-02 | Fixed Roller Guide Assembly |
| -16 | 100810-01 | Head Guide (Matched Pair) |
| -17 | 615-0460 | Stud (Midget Banana Plug) |
| -18 | 102581-01 | Flux Gate (Dual Stack Transports Only) |
| -19 | 510-* | Magnetic Head |
| -20 | 103542-01 | Door Latch Assembly |
| -21 | $\begin{aligned} & 102320-01 \\ & 103813-01 \end{aligned}$ | Photosensor <br> Photosensor Reflector |
| -22 | 103805-90 | Tape Cleaner Assembly |
| -23 | 101026-03 | Fixed Roller Guide Assembly |
| -24 | 506-1807 | ON/OFF Switch/Indicator |
| -25 | 102357-23 | RESET Switch/Indicator Assembly |
| -26 | $\begin{aligned} & 102357-20 \\ & 102357-21 \end{aligned}$ | HI DEN Indicator Assembly (NRZI Transports) 1600 CPI Indicator Assembly (PE Transports) |
| -27 | 102357-16 | LOAD Switch/Indicator Assembly |
| -28 | 102357-17 | ON LINE Switch/Indicator Assembly |
| -29 | $\begin{aligned} & 102357-19 \\ & 102357-22 \\ & 102357-24 \end{aligned}$ | WRT EN Indicator FPT Indicator 9 TRACK Indicator |
| -30 | 102357-18 | REWIND Switch/Indicator Assembly |
| -31 | 506-6360 | Load Limit Switch |
| Not Shown | 101761-01 | Overlay |
| Not Shown | 103357-01 | Door Assembly |

*Refer to Spare Parts List, Table 7-4, for specific part number.


Figure 7-2. T8000A Series Transports, Photo Parts Index (Rear View with PCBAs)

Table 7-2
T8000A Series Transports, Photo Parts Index

| Figure and <br> Index No. | Part <br> Number | Description |
| :--- | :--- | :--- |
| Figure 7-2 <br> -1 | $102410-02$ | Reel Motor Assembly |
| -2 | $102245-01$ | RFI Filter |
| -3 | $103375-01$ | Card Cage Assembly |
| -4 | $615-0114$ | Adjustable Clamp |
| -5 | $615-7500$ | Floating Captive Fastener Screw |
| -6 | $502-1243$ | Relay |
| -7 | $*$ | Capstan Motor Assembly |
| $-8^{* *}$ | $102262-01$ | Capacitor Pack Assembly |
| $-9^{* *}$ | $658-2038$ | Panel Fuse Holder |
| $-10^{* *}$ | $663-3550$ | Fuse, 5A, Slow Blow, 115v, 60 Hz <br> Fuse, 3A, Slow Blow, 240v, 50 Hz |
| $-11^{* *}$ | $660-0011$ | Strain Bushing |
| -12 | $104770-01$ | Power Cord Assembly, 125v <br> $104770-02$ <br> Power Cord Assembly, European <br> Power Cord Assembly, 250v |
|  | $104770-03$ |  |
| -13 | $102316-01$ | Heatsink Assembly |
| -14 | $102334-*$ | Tape Control J PCBA |

*Refer to Spare Parts List, Table 7-4, for specific part number. **Not required with 48 v converter.


Figure 7-3. T8000A Series Transports, Photo Parts Index (Rear View, PCBAs Removed)

Table 7-3
T8000A Series Transports, Photo Parts Index

| Figure and Index No. | Part Number | Description |
| :---: | :---: | :---: |
| Figure 7-3 |  |  |
| -1 | 610-0020 | Timing Belt, 80-tooth |
| -2 | $\begin{aligned} & 103541-01 \\ & 506-6360 \end{aligned}$ | Limit Switch Assembly Switch |
| -3 | 103547-01 | Cam Interlock |
| -4 | 100858-05 | Tension Arm Sensor Assembly |
| -5 | 100925-01 | Shutter |
| -6 | 615-4410 | Adjustable Pawl Fastener |
| -7 | $\begin{aligned} & 102258-01 \\ & 506-6360 \end{aligned}$ | Gear Motor Assembly. Switch |
| -8 | $\begin{aligned} & 103345-01 \\ & \text { or } \\ & 104700-* \end{aligned}$ | Power Supply Assembly 48 v Converter |
| -9 | 101083-01 | Pulley, 48-tooth |
| -10 | 102305-01 | Cable Arm Retractor Linkage |
| -11 | 102373-01 | Cable Arm Retractor Spring |
| -12 | $\begin{aligned} & 100817-02 \\ & 506-6360 \end{aligned}$ | Write Lockout Assembly Switch |
| *Refer to Drawing 104700 for specific part number. |  |  |

Table 7-4
T8000A Series Recommended Spare Parts List

| Item |  | Part No. |
| :---: | :---: | :---: |
| 1. | Data G PCBA (T8660A) | 101376-* |
|  | Data F PCBA (T8640A) | 101346-* |
|  | Data K1 PCBA (T8640A-98) | 102326-* |
|  | Data D1 PCBA (T8X60A) | 101721-* |
|  | Data E17 PCBA (T8X40A) 7-track | 101716-* |
|  | Data E19 PCBA (T8X40A) 9-track | 101711-* |
| 2. | PE/NRZI Write PCBA (T8640A-98) | 102308-* |
| 3. | Tape Control J PCBA | 102334-* |
| 4. | Tape Cleaner Assembly | 103805-90 |
| 5. | Photosensor Assembly | 102320-01 |
| 6. | Tension Arm Sensor Assembly | 100858-05 |
| 7. | Tension Arm Roller Guide Assembly | 100808-03 |
| 8. | Fixed Roller Guide Assembly | 101026-02 |
| 9. | Fixed Roller Guide Assembly | 101026-03 |
|  | Reel Motor Assembly | 102410-02 |
| 11. | Capstan Motor Assembly, $\leq 25$ ips | 102413-11 |
|  | Capstan Motor Assembly, >25 ips | 102386-11 |
| 12. | ON/OFF Switch/Indicator | 506-1807 |
| 13. | LOAD Indicator/Switch Assembly | 102357-16 |
| 14. | ON LINE Switch/Indicator Assembly | 102357-17 |
| 15. | REWIND Switch/Indicator Assembly | 102357-18 |
| 16. | WRT EN Indicator Assembly | 102357-19 |
|  | FPT Indicator Assembly | 102357-22 |
|  | 9 TRACK Indicator Assembly | 102357-24 |
| 17. | HI DEN Indicator Assembly | 102357-20 |
|  | 1600 CPI Indicator Assembly | 102357-21 |
|  | RESET Switch/Indicator Assembly | 102357-23 |
| 19. | Head, 7-track T8X40A, All Speeds | $510-6187$ |
|  | Head, 9-track 18X40A, All Speeds Head, 9 -track T8640A, All Speeds | $510-6189$ $510-6169$ |
|  | Head, 9-track T8640A-98, All Speeds | 510-6169 |
|  | Head, 7-track T8X60A, All Speeds | 510-5187 |
|  | Head, 9-track T8X60A, All Speeds | 510-5189 |
|  | Head, 9-track T8660A, 12.5 ips | 510-5169 |
|  | Head, 9-track T8660A, 18.75 ips | 510-5269 |
|  | Head, 9-track T8660A, 25-45 ips | 510-5369 |
| 20. | Head Guide Shim | 100298-01 |
| 21. | Strobe Disk, 12.5/25.0 ips | 101744-02 |
|  | Strobe Disk, 18.75/37.5 ips | 101744-03 |
|  | Strobe Disk, 20.0/40.0 ips | 101744-04 |
|  | Strobe Disk, 22.5/45.0 ips | 101744-05 |
|  | Strobe Disk, 24.0 ips | 101744-06 |
|  | Strobe Disk, 30.0 ips | 101744-07 |
| *Order as indicated on PCBA. |  |  |

Table 7-5
Part Number Cross Reference

| PERTEC Part No. | Manufacturer | Manufacturer Part No.*/Description |
| :---: | :---: | :---: |
| Composition Resistors | (Comply with MIL-R-11) |  |
| 100-0395 |  | 3.9 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-1005 |  | 10 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-1015 |  | 100 ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-1025 |  | 1.5 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-1055 |  | 1 meg ohm $\pm 5 \%, 1 / 4 w$ |
| 100-1235 |  | 150 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-1525 |  | 1.5 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-1535 |  | 15 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-1815 |  | 180 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-1825 |  | 1.8 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-1845 |  | 180k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-2215 |  | 220 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-2225 |  | $2.2 k$ ohms $\pm 5 \%, 1 / 4 w$ |
| 100-2235 |  | 22 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-2705 |  | 27 ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-2725 |  | 2.7 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-3305 |  | 33 ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-3315 |  | 390 ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-3325 |  | $3.3 \mathrm{kohms} \pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-3925 |  | $3.9 \mathrm{kohms} \pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-4705 |  | 47 ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-4715 |  | 470 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-4725 |  | 4.7 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-5625 |  | 5.6k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-6805 |  | 68 ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 100-6815 |  | 680 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-8215 |  | 820 ohms $\pm 5 \%, 1 / 4 w$ |
| 100-8235 |  | 82 k ohms $\pm 5 \%, 1 / 4 \mathrm{w}$ |
| 101-1025 |  | 1 k ohms $\pm 5 \%, 1 / 2 \mathrm{w}$ |
| 101-1505 | . | 15 ohms $\pm 5 \%, 1 / 2 \mathrm{w}$ |
| 101-1515 |  | 1.50 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-2205 |  | 22 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-2715 | - | 270 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-3305 |  | 33 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-3325 |  | 3.3k ohms $\pm 5 \%, 1 / 2 \mathrm{w}$ |
| 101-3915 |  | 390 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-4715 |  | 470 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-6805 |  | 68 ohms $\pm 5 \%, 1 / 2 w$ |
| 101-8205 |  | 82 ohms $\pm 5 \%, 1 / 2 w$ |
| 102-5615 |  | 560 ohms $\pm 5 \%, 1 \mathrm{w}$ |
| 102-8205 |  | 82 ohms $\pm 5 \%, 1 \mathrm{w}$ |
| 103-1215 |  | 120 ohms $\pm 5 \%$, 2 w |
| 103-1815 |  | 180 ohms $\pm 5 \%$, 2 w |
| 103-4705 |  | 47 ohms $\pm 5 \%, 2 w$ |

Table 7-5
Part Number Cross Reference (Continued)

| PERTEC Part No. | Manufacturer | Manufacturer Part No.*/Description |
| :---: | :---: | :---: |
| Precision Resistors | (Comply with MIL-R-11) |  |
| 104-1000 |  | 100 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1001 |  | 1 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1002 |  | 10 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1003 |  | 100 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1100 |  | 110 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1101 |  | 1.1 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1102 |  | 11 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1211 |  | 1.21 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1330 |  | 133 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1331 |  | 1.33 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1332 |  | 13.3 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1623 |  | 162 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1781 |  | 1.78 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1782 |  | 17.8 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1961 |  | 1.96k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-1962 |  | 19.6 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2151 |  | 2.15 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2152 |  | 21.5k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2370 |  | 237 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2610 |  | 261 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2611 |  | 2.61 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2612 |  | 26.1 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-2870 |  | 287 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-3481 |  | 3.48 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-3831 |  | 3.83 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-3832 |  | 38.3 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-3833 |  | 383 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-3482 |  | 34.8 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-3483 |  | 348 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-4220 |  | 422 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-4221 |  | 4.22 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-4222 |  | 42.2k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-4641 |  | 4.64k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-4753 |  | 475k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-5110 |  | 511 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-5111 | . | 5.11 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-5113 |  | 511 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-5620 |  | 562 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-5621 |  | 5.62k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-6192 |  | 61.9 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-6811 |  | 6.81 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-6812 |  | 68.1 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-7500 |  | 750 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-8252 |  | 82.5 k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-9090 |  | 909 ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |

Table 7-5
Part Number Cross Reference (Continued)

| PERTEC Part No. | Manufacturer | Manufacturer Part No.*/Description |
| :---: | :---: | :---: |
| Precision Resistors (Continued) |  |  |
| 104-9092 |  | 90.9k ohms $\pm 1 \%, 1 / 4 \mathrm{w}$ |
| 104-9093 |  | 909k ohms $\pm 1 \%, 1 / 4 w$ |
| 107-1000 |  | 100 ohms $\pm 1 \%, 1 / 8 w$ |
| 107-1001 |  | 1 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1002 |  | 10k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1003 |  | 100k ohms $\pm 1 \%, 1 / 8 w$ |
| 107-1101 |  | 1.1 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1102 |  | 11 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1211 |  | 1.21 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1332 |  | 13.3k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1471 |  | 1.47 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1781 |  | 1.78 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1782 |  | 17.8 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1961 |  | 1.96 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1962 |  | 19.6k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-1963 |  | 196k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-2152 |  | 21.5 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-2611 |  | 2.61 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-2612 |  | 26.1 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-2870 |  | 287 ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-3482 |  | 34.8 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-3483 |  | 348 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-3832 |  | 38.3 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-4221 |  | 4.22k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-4222 |  | 42.2 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-5110 |  | 511 ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-5111 |  | 5.11k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-5112 |  | 51.1 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-5113 |  | 511 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-5620 |  | 562 ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-6192 |  | 61.9 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-6811 |  | 6.81 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-6812 |  | 68.1 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-8252 |  | 82.5 k ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 107-9090 |  | 909 ohms $\pm 1 \%, 1 / 8 \mathrm{w}$ |
| 109-0003 |  | 0.10 ohms $\pm 3 \%$, 5 w |
| 113-0111 |  | 10 ohms $\pm 1 \%, 1 \mathrm{w}$ |
| Variable Resistors |  |  |
| 121-1020 | Beckman | 79PR1K, Variable, 1 k ohms $\pm 10 \%, 3 / 4 \mathrm{w}$ |
| 121-1030 | Beckman | 79PR10K, Variable, 10k ohms $\pm 10 \%, 3 / 4 \mathrm{w}$ |
| 121-5020 | Beckman | 79PR5K, Variable, 5 k ohms $\pm 10 \%, 3 / 4 \mathrm{w}$ |
| 123-5020 | Spectrol | 53-1-1-502, Variable, 5 k ohms $\pm 10 \%, 1 / 2 \mathrm{w}$ |

Table 7-5
Part Number Cross Reference (Continued)

| PERTEC Part No. | Manufacturer | Manufacturer Part No.*/Description |
| :---: | :---: | :---: |
| Dipped Mica Capacitors |  |  |
| 130-1005 | (Comply with MIL-C-5) | $10 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-1015 |  | $100 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-1515 |  | $150 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-2205 |  | $22 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-2215 |  | $220 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-3305 |  | $33 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-4705 |  | $47 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-4715 |  | $470 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-5605 |  | $56 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-6805 |  | $68 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| 130-7515 |  | $750 \mathrm{pf} \pm 5 \%, 500 \mathrm{vdc}$ |
| Mylar Film Capacitors |  |  |
| 131-1020 | TRW | 663uw series, $.001 \mu \mathrm{fd} \pm 10 \%, 100 \mathrm{vdc}$ |
| 131-1030 | TRW | 663uw series, $.01 \mu \mathrm{fg}+10 \%, 100 \mathrm{vdc}$ |
| 131-2220 | TRW | 663uw series, $.0022 \mu \mathrm{fd} \pm 10 \%, 100 \mathrm{vdc}$ |
| 131-4720 | TRW | 663uw series, $.0047 \mu \mathrm{fd} \pm 10 \%, 100 \mathrm{vdc}$ |
| Solid Tantalum Polarized Capacitors |  |  |
| 132-1062 | Mallory | TIM106M010POW, $10 \mu \mathrm{fd} \pm 20 \%, 10 \mathrm{vdc}$ |
| 132-2752 | Mallory | TIM275M035POW, $2.7 \mu \mathrm{fg} \pm 20 \%$, 35 v dc |
| 139-2244 | Kemet | T310A225M020AS, $2.2 \mu \mathrm{fd} \pm 20 \%$, 20v dc |
| 139-2262 | Kemet | T310B226M015AS, $22 \mu \mathrm{fd} \pm 20 \%, 15 \mathrm{vdc}$ |
| 139-3352 | Kemet | T310A335M015AS, $3.3 \mu \mathrm{fg} \pm 20 \%$, 15v dc |
| Aluminum Foil Polarized Capacitor |  |  |
| 134-2680 | Mallory | TOW282N025N1R3P, $2600 \mu \mathrm{fg}+100 \%-10 \%$, 20 vdc |
|  |  |  |
| 135-1002 | Centralab | DD-102, . $001 \mu \mathrm{fg} \pm 10 \%, 1000 \mathrm{vdc}$ |
| 135-1040 | TRW | 663uw series, $.10 \mu \mathrm{fd} \pm 10 \%, 100 \mathrm{vdc}$ |
| 135-4742 | Erie | $8131-050651-474 \mathrm{M}, .47 \mu \mathrm{fd} \pm 20 \%, 50 \mathrm{vdc}$ |
| Transistors |  |  |
| 200-3053 | RCA | 2N3053, NPN, Silicon Annular, T0-5 |
| 200-3251 | Motorola | 2N3251, PNP, Switching, T0-18 |
| 200-4123 | Motorola | 2N4123, NPN, Silicon, T0-92 |
| 200-4125 | Motorola | 2N4125, PNP, Silicon, T0-92 |
| 200-4400 | Motorola | 2N4400, NPN, Silicon, T0-92 |
| 200-4402 | Motorola | 2N4402, PNP, Silicon, T0-92 |
| 200-5321 | RCA | 2N5321, NPN, Silicon, T0-5 |
| 200-5323 | RCA | 2N5323, PNP, Silicon, T0-5 |
| 200-6051 | Motorola | 2N6051, PNP, Power Darlington, TO-3 |
| 200-6058 | Motorola | 2N6058, NPN, Power Darlington, T0-3 |
| 200-6282 | Motorola | 2N6282, NPN, Power Darlington, T0-3 |
| 200-6285 | Motorola | 2N6285, PNP, Power Darlington, T0-3 |

Table 7-5
Part Number Cross Reference (Continued)

| PERTEC Part No. | Manufacturer | Manufacturer Part No.* / Description |
| :---: | :---: | :---: |
| Field Effect Transistors 204-0074 | National |  |
| Diodes |  |  |
| 300-4002 | Motorola | IN4002, Rectifier, 1A, 100 PIV, D0-41 |
| 300-4446 | Components, Inc. | IN4446, Switching, 75PIV, D0-7 |
| Zener Diodes |  |  |
| 300-0475 | Motorola | IN4732A, Zener, 4.7v dc $\pm 5 \%$, 1w, D0-41 |
| 330-0515 | Motorola | IN4733A, Zener, 5.1v dc $\pm 5 \%$, 1w, D0-41 |
| 330-1005 | Motorola | IN4740A, Zener, $10 \mathrm{v} \pm 5 \%, 1 \mathrm{w}$, D0-41 |
| 330-1205 | Motorola | IN4742A, Zener, 12v $\pm 5 \%$, 1 w |
| 331-0275 | Motorola | IN5223B, Zener, 2.7v dc $\pm 5 \%$, 500mw, D0-7 |
| 331-0395 | Motorola | IN5228B, Zener, 3.9v dc $\pm 5 \%$, 500mw, D0-7 |
| 331-0515 | Motorola | W5231B, Zener, $5.1 \mathrm{vdc} \pm 5 \%, 500 \mathrm{mw}$, D0-7 |
| 331-0605 | Motorola | IN5233B, Zener, $6 \mathrm{vdc} \pm 5 \%, 500 \mathrm{mw}$, D0-7 |
| Light Emitting Diode 301-0055 | Optron | OR133W-3, Light Emitting, Infra Red, T0-46 |
| Operational Amplifiers |  |  |
| 400-0307 | National | LM307N, IC, Op Amp |
| 400-0319 | National | LM319N, IC, Dual Comparator |
| 400-0592 | Signetics | NE592A, IC, Op Amp |
| 400-5558 | National | LM1458N, IC, Dual Op Amp |
| Relays |  |  |
| 502-1205 | Amer Zett | AZ-535-11-1, 12 v dc, SPDT, Contract Rating $5 A$ at 26 v dc |
| 502-1242 | Allied Control | TF-154-4C-12v dc, $12 \mathrm{vdc}, 4 \mathrm{PDT}$, Contact Rating 5 A at 28 v dc |
| Inductors |  |  |
| 515-1015 | Delevan | 1537-76, $100 \mu \mathrm{H} \pm 5 \%, 4.5$ ohms |
| 515-3305 | Delevan | 1537-52, $33 \mu \mathrm{H} \pm 5 \%, 2.9$ ohms |
| 515-6805 | Delevan | 1537-68, $68 \mu \mathrm{H} \pm 5 \%, 3.3$ ohms |
| Crystals |  |  |
| 524-0002 | Northern Eng Lab | NE12, 10.00 MHz $\pm .005$ |
| * or equivalent |  |  |

Table 7-6
T8000A Series Transports PCBA Interconnections

| Tape Control PCBA |  |
| :---: | :---: |
| J1 | Supply Reel Tension Arm Sensor |
| J2 | Take-up Reel Tension Arm Sensor |
| J3 | Capstan Motor |
| J4 | Take-up Reel Motor |
| J5 | Supply Reel Motor |
| J6 | Power Supply Assembly |
| J7 | Tension Arm Interlock and WLO Switch |
| J8 | Data E17, E19, F, G, and D1 PCBAs (J8) <br> Data K1 PCBA (J8) <br> PE/NRZI PCBA (J26) |
| J9 | Heatsink Assembly |
| J10 | Not Used |
| J11 | Data K1 PCBA (J11) |
| $J 12$ | RESET Control |
| J13 | LOAD Control |
| J14 | REWIND Control |
| J15 | EOT/BOT Sensors |
| J16 | Address Select Control |
| J17 | ON LINE Control |
| J18 | 9 TRACK Control |
| J19 | HI DEN or 1600 CPI Control |
| J20 | WRT EN or FPT Indicator |
| J21 | Option Select Plug Assembly |
| J22 | Format Plug Assembly |
| J27 | Power Supply Assembly |
| J28 | Power Disconnect Plug |
| J29 | Gear Motor Limit Switch |
| J30 | Load Limit Switch |
| J31 | Arm Cocking Gear Motor |
| J32 | Heatsink Assembly |
| J33 | Heatsink Assembly |
| J34 | Heatsink Assembly |
| J35 | Heatsink Assembly |
| PE/NRZI Write PCBA |  |
| $\begin{aligned} & \mathrm{J} 23 \\ & \mathrm{~J} 25 \\ & \text { P104 } \end{aligned}$ | Data K1 PCBA (J4) (Read Configuration) <br> Data K1 PCBA (J8) (Read and Write Configuration) <br> Data K1 PCBA (J104) (Read and Write Configuration) |
| Data PCBA |  |
| J1 <br> J24 <br> J2 <br> J4 <br> J1 <br> J2 <br> J24 | Data E17, E19, and F PCBAs, Write and Erase Head PE/NRZI Write PCBA, Write and Erase Head Data E17, E19, and F PCBAs, Read Head Data K1 PCBA, Read Head Data D1 and G PCBAs, Read/Write and Erase Head Data D PCBA, Read/Write and Erase Head PE/NRZI Write PCBA, Read/Write and Erase Head |

APPENDIX A - GLOSSARY

| Symbol | Description | Symbol | Description |
| :---: | :---: | :---: | :---: |
| B1B | Buffer 1 Busy | EPNP | Encoder Pulse Narrow Powerful |
| BCD10 | Binary Coded Decimal | EPS | Erase Power Start |
| BOT | Beginning of Tape | EPW | Encoder Pulse Wide |
| BOTD | Beginning of Tape Delay | ERASE* | Erase |
| BOTDP | Beginning of Tape Delay Pulse | ES | Erase Winding Start |
| BOTI | Beginning of Tape Input | EWPC | Enable Write Power Control |
| вото | Beginning of Tape Output | EWRS | Enable Write/Read Status |
| BOV* | Buffer Overflow | FAD* | Formatter Address |
| CBY | Command Busy | FBY* | Formatter Busy |
| CCG* | Check Character Gate | FEN• | Formatter Enable |
| CCS | Check Character Strobe | FER* | Formatter Error |
| CER* | Correctable Error | FGC | File Gap Command |
| CHARDET* | Character Detect | FGL | File Gap Lamp |
| CLRNZDATA* | Clear NRZI Data | FGR | File Gap Ramp |
| CMP1,2 | Clamp Waveform 1, 2 | FLR | First Load - or Rewind |
| COPY* | Copy | FM | File Mark |
| CPI | Characters Per Inch | FMK* | File Mark |
| CRC0-CRC7 | Cyclic Redundancy Check, Ch 0-7 | FMKNZ* | File Mark NRZI |
| CRCC | Cyclic Redundancy Check Character | FMKPE* | File Mark PE |
| CRCP | Cyclic Redundancy Check Parity | FPT | File Protect |
| CTO-CT7 | Center Tap 0-7 | FWD | Forward |
| CTP | Center Tap Parity | GIP | Gap In Process |
| CT4 | Count 4 | GO | Motion signal delayed |
| CT8 | Count 8 | GO1* | Go |
| CUR | Clean-up Ramp | GRS | General Reset |
| CURLIM | Reel Servo Current Limit | HER* | Hard Error |
| D8CT | Disables 8 Count | HERNZ* | Hard Error NRZI |
| DBY | Data Busy | HID | Hi Density |
| DDI | Data Density Indicator | 10* | Identification |
| DDS | Data Density Select | IDGATE* | Identification Gate |
| DDSX | Data Density Select External | INTLK | Transport Interlock Signal |
| DEN* | Density | IRGC | Record Gap Command |
| DGATE* | Data Gate | K2ENERG | Relay K2 Energize |
| DI* | Data In | LD | Lamp Driver |
| DMC | Disable Manual Controls | LDCRC* | Load Cyclic Redundancy Check |
| DROPDET* | Drop Detected | LDFAIL | Load Fail |
| DUN | Done and Unload | LDLOOP | Load Loop |
| EAO | Encoder Amplifier Output | LDP | Load Point |
| ECC | Enable Check Character | LDWRTDATA* | Load Write Data |
| ECD | Echo Check Disable | LFC | Load Forward Command |
| ECE | Echo Check Error | LFR | Load Forward Ramp |
| ECLK* | Envelope Clock | LOCK | Interlock off pulse |
| ECO0-ECO7 | Echo Check Output, Ch 0-7 | LOCKA | Interlock A |
| ECOP | Echo Check Output Parity | LOCKB | Interlock B |
| ECR | Echo Check Reset | locktime | Locktime pulse |
| ECRC | Enable CRC | LOL* | Load-On-Line |
| EDIT* | Edit | LRCC | Longitudinal Redundancy Check Character |
| EEC | Enable Echo Check | LWD* | Last Word |
| EEP | Enable Encoder Pulse | MOTION | Tape Motion as result of SFC/SRC Command |
| EF | Erase Winding Finish | NRZ* | NRZI |
| EFM | Enable File Mark | OFC* | Off Line Command |
| ENV* | Envelope Detected | OFFC | Off-Line Input Command |
| EOT* | End of Tape | OFL* | Off Line |
| EOTI | End of Tape Input | OLUNL | Off-Line Unload |
| EOTO | End of Tape Output | ONEDET* | Ones Detected |
| NOTES: <br> 1. *Microformatter Only <br> 2. I Symbol Prefix = Interface Signal <br> 3. N Symbol Prefix = Low Active Signal |  |  |  |


| Symbol | Description | Symbol | Description |
| :---: | :---: | :---: | :---: |
| OOLL | On-Line/Off-Line Lamp | RWR | Rewind Ramp |
| ORD | ORed Data | RYC | Ready Command ... |
| OVW | Overwrite | SBY | Start Busy Delay . |
| PARC* | Parity Correcting | SFC | Synchronous Forward Command |
| PICKK1 | Pick K-1 Relay | SFCD | Synchronous Forward Command Delayed |
| POSTJUMP* | Postamble Jump | SFL1-SFL4 | Step Forward Level 1-4 |
| POSTEST* | Postamble Test | SGL* | Single |
| PR* | Parity | SHLCLK* | Shift Left Clock |
| PRESET* | Preset | SHRCLK* | Shift Right Clock |
| PSEN* | Power Supply Enable | SKLP | Seek Load Point |
| PSO0-PSO7 | Peak Sensor Output, Ch 0-7 | SKTO | Seek Time Out |
| PSOP | Peak Sensor Output Parity | SLT | Select Transport \% |
| PSP | Peak Sensor Parity | SPC* | Space Command |
| RA01, RA02 | Read Amplifier Track 0, Output 1, Output 2 | SPD* | Speed |
| RA11, etc. | Read Amplifier Track n, Output 1 or 2 | SRC | Synchronous Reverse Command |
| RAC | Read Amplifier Clamp | SRO/SRO1 | Selected-Ready-On Line |
| RACT | Read Amplifier Center Tap | SWS | Set Write Status |
| RAP1, RAP2 | Read Amplifier Parity, Output 1, Output 2 | TAD | Turnaround Delay |
| RCLK* | Read Clock | TADO, 1* | Transport Address |
| RD0-RD7 | Read Data, Ch 0-7 | TBY | Turnaround Busy |
| RDI | Relay Driver Input | TENCNT | Tension Control |
| RDNZ* | Read NRZI Data | THR* | Read Threshold - .al |
| RDP | Read Data Parity | TIP | Tape-In-Place |
| RDS | Read Data Strobe | TNT | Tape Not Tensioned |
| RDY | Ready | TRR | Transport Ready |
| REN* | Read Enable | WARS | Write Amplifier Reset |
| RENDNZ* | Read End NRZI | WCLK* | Write Clock |
| RENDPE* | Read End PE | WCN* | Write Control |
| REV | Reverse | WCRC | Write CRC |
| REW* | Rewind | WD* | Write Data |
| REW RAMP A | Rewind Ramp Output A | WD0-WD7 | Write Data, Ch 0-7 |
| REW RAMP B | Rewind Ramp Output B | WDP | Write Data Parity |
| REWRI | Rewind Ramp Initiate | WDS | Write Data Strobe |
| RF0-RF7 | Read Finish 0-7 | WDSN | Write Data Strobe Narrow |
| RFP | Read Finish Parity | WDSW | Write Data Strobe Wide |
| RGATENZ* | Read Gate NRZI | WF0-WF7 | Write Finish, Ch 0-7 |
| RGATEPE* | Read Gate PE | WFM | Write File Mark |
| RGC | Inter-Record Gap Command | WFP | Write Finish Parity |
| RGR | Inter-Record Gap Ramp | WLO | Write Lockout |
| RRS | Remote Reset | WDP | Write Power Control |
| RS1 | Rewind Step 1 | W/RF0-W/RF7 | Write/Read Head Winding Finish, Ch 0-7 |
| RSC* | Read Strobe Counter | W/RFP | Write/Read Heading Winding Finish Parity |
| RSP | Read Start Parity | WDO | Write/Read Output |
| RST | Reset | WDP | Write Pulse * |
| RSTR* | Read Strobe | WRS | Write/Read Status |
| RSTRNZ* | Read Strobe NRZI | W/RS0-W/RS7 | Write/Read Head Winding Start, Ch 0-7 |
| RSTRPE* | Read Strobe PE : | W/RSP | Write/Read Head Winding Start Parity |
| RTH | Read Threshold | WRT* | Write |
| RTN1 | Front Panel Switches Gnd Return 1 | WRT EN | Write Enable |
| RW1 | Rewind 1 FF | WS0-WS7 | Write Start, Ch 0-7 |
| RWC | Rewind Command | WSC | Write Step Command |
| RWD | Rewinding | WSP | Write Start Parity |
| RWFWD | Rewind Forward | WSTR* | Write Strobe |

## ADDENDUM A

DUAL FORMAT TAPE TRANSPORT

## ADDENDUM A

## TABLE OF CONTENTS

Paragraph Page
4.1 Functional Subsystems Description, Introduction ..... A-2
4.2 Data Electronics ..... A-2
4.3 Data Recording ..... A-8
4.3.1 NRZI Operation ..... A-8
4.3.2 PE Operation ..... A-11
4.4 Data Reproduction ..... A- 14
4.4.1 NRZI Operation ..... A-15
4.4.2 PE Operation. ..... A-18
5.1 PCBA Theory of Operation, Introduction ..... A-20
5.2 Data Kl Detailed Theory of Operation ..... A-20
5.3 PE/NRZI Write PCBA Detailed Theory of Operation ..... A-32
5.3.1 NRZI Operation ..... A-34
5.3.2 PE Operation ..... A-36
6.1 Adjustment Procedures, Introduction ..... A-38
6.2 Read Preamplifier Gain (NRZI Mode) ..... A-38
6.2.1 Test Configuration ..... A-38
6.2.2 Test Procedure (NRZI Mode) ..... A-39
6.2.3 Adjustment Procedure (NRZI Mode) ..... A-40
6.3 Read Preamplifier Gain (PE Mode) ..... A-40
6.3.1 Test Configuration ..... A-41
6.3.2 Test Procedure (PE Mode) ..... A-41
6.3.3 Adjustment Procedure ..... A-42
6.4 Threshold Generator ..... A-42
6.4.1 Test Configuration (PE) ..... A-43
6.4.2 Test Procedure ..... A-43
6.4.3 Adjustment Procedure ..... A-44
6.5 Character Gate ..... A- 44
6.5.1 Test Configuration ..... A-45
6.5.2 Test Procedure ..... A-45
6.5.3 Adjustment Procedure ..... A. 46

## ADDENDUM A <br> TABLE OF CONTENTS (continued)

Paragraph Page
6.6 Read Skew Measurement and Adjustment ..... A-46
6.6.1 Test Configuration ..... A-46
6.6.2 Test Procedure ..... A.47
6.6.3 Adjustment Procedure ..... A-48
6.7 Write Skew Adjustment ..... A-48
6.7.1 Test Configuration ..... A-48
6.7.2 Test and Adjustment Procedure ..... A-48

## ADDENDUM A <br> LIST OF ILLUSTRATIONS

Figure Page
A-1 PE and NRZI Recording Comparison ..... A-3
A-2 9-Track NRZI Allocation and Spacing ..... A- 4
A-3 7-Track NRZI Allocation and Spacing ..... A-4
A-4 9-Track PE Allocation and Format ..... A-5
A-5 NRZI Write and Read Waveforms ..... A-6
A-6 PE Write and Read Waveforms ..... A-6
A-7 PE/NRZI Write Logic ..... A-51
A- 8 NRZI Data Recording, Timing Diagram ..... A-53
A-9 PE Data Recording, Timing Diagram ..... A-55
A-10 Data Recovery, Functional Block Diagram ..... A-57
A-11 NRZI Data Reproduction, Timing Diagram ..... A-59
A-12 PE Data Reproduction, Timing Diagram ..... A-61
A-13 Data Kl Test Point and Connector Placement ..... A-21
A-14 Operational Amplifier ..... A-23
A-15 PE/NRZI Write PCBA Test Point and Connector Placement ..... A-33

ADDENDUM A<br>DUAL FORMAT TAPE TRANSPORT ADDENDUM

This Addendum provides a description of the NRZI and PE data encoding and decoding schemes employed in PERTEC Dual Format Tape Transports. A block diagram level discussion of the theory of operation of the PE/NRZI Write PCBA is included. Detailed theory of operation of the Data K1 PCBA (Schematic 102325 and Assembly 102326) and the PE/NRZI Write PCBA (Schematic 102307 and Assembly 102308) is also included and should be referred to in lieu of Data PCBA information contained in the companion documents.

Adjustment procedures are provided for NRZI gain, PE gain, threshold generator, and character gate; these procedures should be referred to in lieu of adjustment procedures for these items contained in Section VI of the companion document.

Two packing densities are available in dual density models. On models configured for dual speed operation the function of the data density select switch is altered. When the HI DEN control is illuminated, the transport read/write elctronics are conditioned to operate in the High Density mode and the transport operates at the lower speed.

Two additional interface lines are provided. The operation of these lines is as follows.
(1) NRZI Indicator (INRZ). This is a level which, when true, indicates that the transport is conditioned to read and/or write NRZI tape; when false, the transport is conditioned to read and/or write PE tape.
(2) Speed (ISPEED). This is a level which is true only when dual speed models are conditioned to read and/or write PE tape at the lower tape speed. When the level on this line is false, the dual speed transport is conditioned to read and/or write NRZI tape at the higher speed. The level on this line is maintained in the false state on all single speed models.

## 4.1 <br> FUNCTIONAL SUBSYSTEMS DESCRIPTION, INTRODUCTION

The information contained in this section pertains to the data recording and reproduction scheme employed in PERTEC dual format transports.

The customer should use the following information in lieu of the paragraphs in the companion document entitled "Data Electronics".

### 4.2 DATA ELECTRONICS

Information recorded in the NRZI mode is represented on tape by changes in direction of the magnetization between positive and negative saturation levels. A "one" bit is represented on tape by a flux polarity reversal, and a "zero" bit by no change of flux polarity. Two NRZI tape formats are in general use; they are the IBM 727/729 7-track format which can operate at 200,556 , and 800 cpi , and the IBM 2400 9-track format which operates at 800 cpi.

The PE method of recording distinguishes between one and zero bits on the tape by the direction of flux change. The PE system interprets a flux change toward the magnetization direction of the IBG as a one bit. A flux change in the opposite direction represents a zero bit. A phase flux reversal is written between successive one bits or between successive zero bits to establish proper polarity. Thus, up to two flux changes are required per bit for the PE method of data encoding.

The PE method of recording data differs from the NRZI method in that the NRZI employs only one flux change in either direction to represent a one bit, and the lack of a flux change to represent a zero bit.

Figure A-1 illustrates the basic recording waveform components of the NRZI and PE modes. Note that in the PE mode the direction of magnetic flux change on the tape at the center of the bit cell determines its value (one or zero).

Figures A-2 and A-3 illustrate the relevant 9- and 7-track NRZI allocation and spacing. Figure A-4 illustrates the relevant 9-track allocation, spacing, and format of 1600 cpi PE tapes.

Note that in the 9-track configuration, both NRZI and PE, consecutive data channels are not allocated to consecutive tracks. This organization increases tape system reliability because the most used data channels are located near the center of the tape. Consequently, they are least subject to errors caused by tape contamination.


NOTES:
NRZI - ANY CHANGE IN POLARITY IS A "1" BIT NO CHANGE IS A "0" BIT

Figure A-1. PE and NRZI Recording Comparison


Figure A-2. 9-Track NRZI Allocation and Spacing


Figure A-3. 7-Track NR ZI Allocation and Spacing


Figure A-4. 9-Track PE Allocation and Format

The PE data block is preceded by a preamble consisting of 40 bytes of all zeros and one byte of all ones. Note that the data block is followed by a postamble which is the mirror image of the preamble; i. e., one byte of all ones followed by 40 bytes of all zeros.

NOTE
The preamble and postamble bursts are configured so that during a Read Reverse operation their functions are interchangeable.

Figures A-5 and A-6 illustrate waveforms representative of data written on a channel along with the readback waveforms for NRZI and PE formats, respectively. Magnetization transitions recorded on the tape are not perfectly sharp due to the limited resolution of the magnetic recording process.

During a Read operation, as the tape passes over the Read head, any flux pattern recorded on the tape (one or zero) generates a waveform in its appropriate data track. It is important to note that during a Read Reverse operation the Read signal is inverted, i. e., a PE one bit is a negative transition and a PE zero bit is a positive transition.


Figure A-5. NRZI Write and Read Waveforms


Figure A-6. PE Write and Read Waveforms

Solid state switching is employed to accomplish format selection in the transport. All formats require a minimum signal level for accurate data reproduction. For NRZI tapes this level is approximately 20 percent of the peak voltage output at the read head; on PE tapes this level is approximately 10 percent. These threshold levels prevent tape noise and sporadic signals from appearing on data since these unwanted signals are usually lower than the 20 and 10 percent levels established.

In extreme cases when the PE data signal drops below the 10 percent threshold, an extra low read recovery threshold level is employed. This extra low threshold level can be selected through the interface and reduces the threshold level to approximately 50 percent of its original value, i. e., 5 percent. The lowest level set for the NRZI format is 20 percent.

The data electronics do not include provision for deskewing PE data. The customer must provide this function through use of an external formatter or similar device.

There are two types of skew associated with reproducing NRZI data; these are static and dynamic.

Static skew is caused by misalignment of the head azimuth and gap scatter. Azimuth misalignment is normally corrected by adjusting the tape path over the read head. Dual stack models employ electronic static deskew since the tape path cannot be simultaneously aligned for both stacks.

Dynamic skew is normally caused by imperfections in tape tracking and is corrected for by use of the transport character gate. The character gate is an electronic "window'" which opens upon receipt of the first data "one" bit from any track. The window stays open for nominally 46 percent of the bit-cell time. All other "ones" arriving during the time of this window are considered valid data for that byte.

Figure A-7* is a block diagram of the PE/NRZI Write PCBA. Figures A-8* and A-9* illustrate the timing for NRZI and PE data recording, respectively.

Assume that the transport is Selected, Ready, On-line, and has a supply reel with a Write Enable ring installed. The WRT PWR control line will therefore be at approximately +4.5 v , providing power for the head driver circuits.

When a SYNCHRONOUS FORWARD command is received, the MOTION signal generated on the Tape Control PCBA goes high, enabling one input to AND gate Ull. If the SET WRITE STATUS line on the Tape Control PCBA is true, the NWRT input to the Write PCBA will be low and the following actions take place.
(1) The output of U12 will go high, enabling the second input to U11 and one input to U19 and U20.
(2) The output of Ull will go high removing the reset applied to flip-flop U25. Since the IWARS input to U6 is also high, the reset applied to flip-flop U3 by U9 will also be removed.

### 4.3.1 NRZI OPERATION

Refer to Figures A-7 and A-8 for the following discussion. NRZI operation requires the NHID input to U7 to be high, causing the output of U 7 to go low and the output of U10 to go high. Additionally, the low output from U7 disables U21, enables U22, and conditions U2 to operate as a noninverting device. The output of U 2 will be of the same polarity as that of its input, i. e., output of U1. The high output from Ul0 enables U5, U8, U19, and disables Ul6 through Ul5.

[^1]Since Ul9 has both inputs high, its output goes low and disables one input to U20 and through the write heads center tap switch returns the center taps to approximately -9.5 v . The U 16 output is clamped to a high level by the low input from U15, disabling the PE write threshold generator (PE WTH) on the Data K1 PCBA. The RTH2 output is set high by NWRT by holding one input to U17 low via U13 and U14 and by holding one input to U18 high via U13. The high RTH2 level, sent to the Data K1 NRZI threshold generator, controls the read-while-write or high threshold. RTH2 will remain high, independent of the state of the IRTH2 input, as long as NWRT is low.

The SYNCHRONOUS FORWARD command (ISFC) (Plot l) shown on the timing diagram enables the ramp generator, which causes the tape to accelerate to the prescribed velocity (Plot 2). After a time (T1) determined by the required inter-record gap (IRG) displacement, the WRITE DATA inputs, together with the WRITE DATA STROBE (IWDS), are supplied to the interface connector. The WRITE DATA (IWD) input is received by interface receiver Ul, and when low, enables both the $J$ and K inputs to flip-flop U3 via Ul and U2. This input allows flip-flop U3 to toggle at the trailing edge of each WRITE DATA STROBE (WDSI). Each WDSl is also fed to a dual output single-shot (SSl) which generates pulses approximately $1 \mu \mathrm{sec}$ wide at the trailing edge of each WRITE DATA STROBE. The negative-going output pulse is applied to NOR gate U23 via AND gate U22. The output from U23, WDS2 (Plot 5), is applied to the write deskew single-shot which produces negative-going pulses of variable width (Plots 6 and 7). These pulses are fed through NOR gate U 24 to the clock input of flip-flop U25. The $J$ and $K$ inputs of $U 25$ are conditioned by the $Q$ and $\bar{Q}$ outputs of flip-flop $U 3$ to which they are respectively connected. Depending on the state of the $J$ and $K$ inputs of U25, its master section will load when the clock input goes high and the slave section will change state on the negative, or trailing edge. Since the pulse width into the clock input can be varied, the time at which each
flip-flop output will change state can be controlled to compensate for gap scatter and azimuth error in the particular head being used, thus providing write deskew.

Both outputs of flip-flop U25 are fed to head driver transistors Q1 and Q2 which cause current to flow in one half or the other of the center-tap head winding. Consequently, magnetization on the tape is maintained in the appropriate direction between changeovers and changes direction for each "l" bit to be recorded (as required by the IBM NRZI format). At the end of each record, check characters have to be recorded and an IRG inserted.

In a 9-track system, both CRCC and LRCC are written. The CRC character is supplied by the customer to the interface together with a single WRITE DATA STROBE signal whose trailing edge is separated by four character times from the trailing edge of the last WRITE DATA STROBE. The LRC character is written by resetting flip-flops U3 using the WRITE AMPLIFIER RESET signal (IWARS) received by interface receiver U6 and applied through U8 and U9 to the clear input of U3. The IWARS signal is also applied to U5, the output of which is differentiated by $\delta 1$. The output of $\delta 1$ is applied through NOR gate U23 to the write deskew single-shot. As previously stated, these single-shots compensate for the gap scatter and azimuth error in the head and write the LRC character in a deskewed manner. The timing of the U3 reset operation and the differentiated pulse into the deskew single-shot is controlled by the leading edge of the IWARS signal, which should be separated by eight character times from the trailing edge of the last WRITE DATA STROBE. The LRCC is written such that the total number of magnetization transitions in any track is even.

When the LRCC has been recorded, the SYNCHRONOUS FORWARD command goes false after a post-record delay time (T2), the ramp generator is disabled and the tape decelerates to zero velocity.

### 4.3.2 PE OPERATION

Refer to Figures A-7 and A-9 for the following discussion. When operating in the PE mode, the NHID input is set low. NHID low causes the output of U7 to go high and the output of Ul0 to go low. The high output from U7 enables U21, disables U22, and conditions U2 to operate as an inverting device. Thus, the output of U2 will be of the opposite polarity of that of its input, i.e., output of Ul.

The low output of U10:
(1) Disables U5 and U8 and inhibits the IWARS signal.
(2) Disables U19, the high output of which, together with the high output of U12, makes U20 switch the heads center taps to approximately -4.0 v .
(3) Disables Ul7 and, through U15, enables Ul6.

Since U16 has both inputs high, its output will be low (PE WTH). The low input to U17 will force its output high (RTH2). PE WTH low and RTH2 high are sent to the Data Kl PCBA and together generate the read-whilewrite or the highest of the read threshold levels. Note that to obtain this highest threshold the RTH2 must be high and the PE write threshold (PE WTH) must be low.

As the SYNCHRONOUS FOR WARD command (ISFC) (Plot 1 on the timing diagram) goes low, the ramp generator is enabled and causes the tape to accelerate to the prescribed velocity (Plot 2). After a time (Tl) determined by the required inter-record gap (IRG) displacement, the WRITE DATA inputs (Plot 3), together with the WDS (Plot 4), are supplied to the interface connector. Preamble, data block, and postamble are recorded.

The WRITE DATA (IWD) input is received by interface receiver Ul. The information presented to the $J$ and $K$ inputs of U3 is strobed into this flipflop at the trailing edge of the WRITE DATA STROBE, inverted (WDSI). The WDS1 is also fed to a dual output single-shot (SS1) which generates complementary pulses coincident with the trailing edge of the WDSl signal. The positive-going pulse from SSl is transmitted by U2l and U24 to the clock input of U25. The $Q$ and $\bar{Q}$ outputs of $U 3$ are presented to the $J$ and $K$ inputs of U25 and their levels are copied into U25 at the trailing edge of the positive pulse from U24. On the Write Data lines (IWDP - IWD7) a one is a positive-going edge at data flux reversal time and a zero is a negative-going edge. The phase edge can be positive- or negative-going. Both outputs of flip-flop U25 are fed to head driver transistors Q1 and Q2, which cause current to flow in one half or the other of the center tap head winding. Consequently, magnetization on tape is maintained in the appropriate direction between change-overs and changes direction in accordance with the input signal IWD.

At the completion of the postamble, ISFC goes false after the post-record delay time (T2). The ramp generator is disabled and the tape velocity decelerates to zero.

The threshold level control, performed by U13 through U18, has been discussed for the write mode of operation. It is important to note that the threshold level generators are not part of the PE/NRZI Write PCBA, but are an integral part of the Data Kl PCBA. Only the logic necessary to distinguish between the Write, Read, PE, and NRZI conditions has been built into the PE/NRZI Write PCBA. The output of this threshold level control logic, the RTH2 and the PE WTH, are in the form of standard logic levels of +5 v and 0 v , and are supplied to the Data K1, where the actual threshold levels are generated.

The threshold level control logic operates as follows.
(1) Write NRZI; IRTH1 high.

NHID is high which, through U7, U10, and U15, disables one input to U16, forcing its output to a high level which, in this case, is false.

NHID, through U7 and U10, enables one input to U17. NWRT (low) disables U18 through U13, and clamps one input of U17 permanently low through U13 and U14. Since one input to U18 at this time is high, its output releases the U17 output which also goes high. This high RTH2 level is interpreted by the Data Kl as the Write NRZI mode and the read-while-write threshold level is generated.
(2) Read NRZI; IRTH1 high.

NHID is high, performing the same functions as in
Step (1). NWRT (high), through U13 and U14, makes the second input to Ul7 go high. The Ul7 output goes low and the NRZI read only threshold is generated in the Data Kl PCBA.

Note that during the NRZI mode of operation, the threshold levels are independent of the state of the IRTH2 input line, since this condition is not defined for NRZI.
(3) Write PE; IRTHl high.

NHID (low), through U7 and U10, clamps one input to U17 to low, and through U7, U10, and U15 enables one input to Ul6.

NWRT (low), through U13, sets one input to U18 high, releasing the clamp from the U17 output and allows this line to set high. Ul3 also sets the second input to U16
high. The output of U16 goes low since both inputs are high. PE WTH low and RTH2 high are interpreted in the Data K1 PCBA as the PE read-while-write condition and the highest of the three PE read threshold is generated.
(4) Read PE; IRTH1 high. NHID (low, performs the same functions as in Step (4). NWRT (high), through U13, returns one input of U16 low, forcing U16 output high. U17 still has one input from U10 clamped low, tending to make its output high. IRTH2 high causes the output of U18 to go high. Therefore, PE WTH high and RTH2 high are interpreted by the Data K1 PCBA as the normal PE read-only condition and the intermediate or normal read threshold is generated. When IRTH2 is low, the output of Ul8 will go low. This condition of PE WTH high and RTH2 low, will generate the extra low read threshold level in the Data K1 PCBA or the lowest of the three PE read thresholds.

## 4.4

## DATA REPRODUCTION

The fundamentals of operation of the data recovery system (NRZI and PE) are described in the following paragraphs. Three reference figures are provided to be used in conjunction with this description. Figure A-10* is a functional block diagram of the data recovery system and is used throughout this description. The diagram is keyed only to the text and to the relevant waveform illustration.

Although the Data K1 PCBA is capable of reading 7- or 9-track NRZI tapes and 9-track PE tapes, the discussion in the following paragraphs is based on the 9-track, dual stack, PE/NRZI transport configuration. As an aid to understanding, the NRZI and PE formats will be addressed separately.

[^2]
### 4.4.1 NRZI OPERATION

Figure A-11* is a diagram (keyed to the text) illustrating the NRZI waveforms encountered when reading a NRZI tape. This diagram should be used in conjunction with Figure A-10*.

The 9-track magnetic head is connected to the read preamplifier through a solid-state head switching network Ul. The output of the preamplifier U 2 is an amplified replica of the read head output. The preamplifier gain and bandwidth is adjusted for the appropriate head and format by the Gain and Bandwidth Control block U3.

NOTE
Preamplifier bandwidth for PE operation is wider than for NRZI operation.

The output of the preamplifier is fed via the differentiator $U 4$ to the voltage comparators U5 and U6. In the NRZI mode of operation the reference input to U 5 and U 6 is 0 v . Therefore, U5 (non-inverting) and U6 (inverting) act as squaring circuits.

Operation may be more clearly understood by referring to Figure A-11*. As illustrated in the diagram, both the positive and negative going outputs of the preamplifier will result in sine wave outputs from the differentiator U4. The points at which the sine waves cross the $0 v$ point occur at the peaks of the preamplifier output (which correspond to the flux transitions on the tape).

The slope of the differentiator output at the zero crossing is determined by the polarity of the preamplifier output, which, in turn depends on the direction of the flux transition. The output voltage of the non-inverting amplifier (U5) changes from low to high whenever the differentiator output voltage changes from negative to positive (positive-going data signal peak) and vice versa. Similarly, the output voltage of the inverting amplifier

[^3](U6) changes from low to high whenever the differentiator output voltage changes from positive to negative (negative-going data signal peak).

A dc threshold voltage equal to 20 or 10 percent (depending on which threshold is selected) of the peak preamplifier output is generated in the NRZI threshold generator U26. This threshold reference voltage and its negative complement are fed to the reference inputs of voltage comparators U7 and U8. During NRZI operation the NRZI/PE line at NOR gates Ull and U12 is high, enabling the outputs of the voltage comparators.

When the positive-going portion of the data signal from the preamplifier output exceeds the positive threshold level of the voltage comparator (U7), the output of the comparator goes low. This causes the output of NOR gate Ull to go high.

The high output of gate U11 enables gate U9 to pass the valid data from U5 since the data amplitude was sufficient to exceed the pre-determined threshold. The same process is performed for the negative-going portion of the data signal through devices U8, U6, U12, and U10.

The outputs of NAND gates U9 and Ul0 are ORed by gate U13 and inverted by inverter U14. The resultant output waveform is a negative-going pulse for each data "one" read on that particular track.

The pulse train from inverter U14 contains all true displacement errors associated with azimuth error, gap scatter, and dynamic skew. The read head azimuth error is corrected by aligning the tape path, and the gap scatter (limited to tight tolerances) is absorbed by the character gate.

When the output of the staticiser flip-flop $U 20$ is set to the true state, $Q$ goes high and $\bar{Q}$ goes low. The flip-flop will remain in this state until reset via the Clear Direct (CD) input. The low output of $\bar{Q}$ is NORed with
that of all other channels by gate U23. The output of gate U23 is a positive level which remains high from the first data "l" input to the staticiser clear pulse. The output $(Q)$ of the staticiser is directly connected to the inverting output driver U2l which drives the interface line to a true (low) level when the staticiser is in the "l" state.

The high level of gate U23 output triggers a timing circuit in the character gate. The period of the character gate is approximately 50 percent of a bit cell period. At the end of this period a READ DATA STROBE (RDS) pulse is generated. This pulse strobes the data on the interface output lines into the formatter. Shortly after the RDS pulse the staticiser flipflops are cleared via the Staticiser Clear signal from the character gate.

Testpoint 6 is an algebraic summing point of the pulse trains from all channels and is used when setting and checking transport skew performance.

The control logic (U25) of the Data PCBA operates on inputs supplied from the Tape Control PCBA. The output of the logic controls such functions as:
(1) Preamplifier gain/bandwidth
(2) NRZI and PE threshold levels
(3) NRZI and PE mode controls

It should be noted that portions of the data channel are not utilized in NRZI reproduction. These portions are the PE envelope detector U15, NAND gate U18, inverter U19, and driver U22. The NRZI/PE control line into gate U18 was continuously low, thus disabling the gate and keeping erroneous data from reaching the interface driver U22.

### 4.4.2 PE OPERATION

Figure A-12* is a diagram (keyed to the text) illustrating the PE waveforms encountered when reading a PE tape. This diagram is to be used in conjunction with Figure A-10*. Functions common to both PE and NRZI which were previously discussed will not be detailed.

As in NRZI operation, not all portions of each data channel are used. For PE operation the NRZI/PE select signal into gates Ull and Ul2 is held low. This effectively disables voltage comparators U7 and U8, thus NAND gates U9 and U10 are always enabled. The staticiser clear line is held continuously low, disabling the staticiser flip-flop U20 so that no erroneous data can reach the interface driver U2l.

For the PE mode of operation, the 9-track head is connected to the preamplifier which, in turn, feeds the differentiator U4. In single speed transports, the frequency content of the data signal is considerably higher in the PE mode than in the NRZI mode. Therefore, it is necessary to switch the bandwidth (and therefore the gain) with a change of mode. This is accomplished by the Gain/Bandwidth zontrol signal.

In dual speed transports the tape speed is halved to maintain the same data rate in both PE and NRZI modes of operation. In this case no bandwidth (or gain) switching occurs with a mode change.

As in NRZI operation, the output of U 4 is fed to the two voltage comparator circuits U5 and U6. U5 acts as a squaring circuit whose edges correspond to the peaks of the read signal from the head. The output from U5 is thus a replica of the magnetization on the tape.

Before the data is sent to the interface, it is gated with a signal called PE ENVELOPE which is generated as follows.

[^4]In the PE mode, U6 acts as a voltage comparator whose reference (positive) input is set to a positive level equal to approximately 10 or 5 percent of the peak differentiator output (U4). The differentiator, rather than preamplifier output is used because the differentiator characteristics result in amplitude equalization of the 1600 and 3200 frpi signals and also remove base line distortion effects associated with high density operation.

When the differentiator output exceeds the positive threshold, the output of voltage comparator U6 goes low, causing the output of NAND gate Ul0 to go high (the other input to Ul0 is always high). Thus, a positive pulse appears at the input to the envelope detector (U15) for each half-wave portion of the PE signal whose amplitude is sufficient to exceed the threshold. The PE envelope detector utilizes two timing circuits designed so that they are insensitive to the duration of the input pulses. The characteristics of the timing circuits are such that four consecutive input pulses to the PE envelope detector (U15) yield a true output. The absence of two consecutive input pulses after Ul5 has been enabled will cause the output to return to the false state.

If, during a record, the output of the PE envelope detector goes low, gate U18 will be disabled and the data flow will be interrupted. The external formatter will detect this loss of signal and, if possible, correct for it by use of the parity information for reconstruction.

In contrast to NRZI operation, there is no clock (Read Strobe) or deskewing circuitry associated with PE reproduction. All channels are completely independent. On dual speed models, the tape speed is reduced to one-half the NRZI speed when operating in the PE mode to yield the same data transfer rate as 800 cpi NRZI.

### 5.1 PCBA THEORY OF OPERATION, INTRODUCTION

The information contained in this section pertains to the Data Kl PCBA and the PE/NRZI Write PCBA installed in PERTEC Dual Format Tape Transports.

The customer should use the following descriptions in lieu of the Data PCBA circuit descriptions contained in the companion document. Only those sections which apply to the 9-track, dual stack PE/NRZI configuration, will be described.

### 5.2 DATA K1 DETAILED THEORY OF OPERATION

The following is a description of the Data Kl PCBA (refer to Schematic 102325 and Assembly 102326).

Data Kl is a dual format Read PCBA which is approximately 16.5 inches long. Figure A-13 illustrates the placement of connectors and test points. Edge connectors J102 and Jl03 are located at each end along one edge. Jl02 is directly coupled to J104, and provides interface signals to the PE/NRZI Write PCBA. Connector J8 is employed to connect power and control signals from the Write PCBA; Jll is used to connect additional logic signals from the Tape Control PCBA; J4 connects the 9-track read head. J3 is omitted in the dual format model.

It is important to note that all read data electronics for the transport are contained on the Data Kl PCBA and all write data electronics are contained on the PE/NRZI Write PCBA.

NOTE
All components shown on Schematic 102325 are not included or used in all versions of the Data K1 PCBA.


Figure A-13. Data Kl Test Point and Connector Placement

The circuit board operation is described in reference to circuit 100. The operation of circuits 200 through 900 is identical to that described for circuit 100.

Since the PCBA is designed to operate in both NRZI and PE Read modes, each mode will be discussed individually. Circuits which are common to both NRZI and PE will be discussed under the NRZI portion.

Reference should also be made to the theory of operation and block diagram of Data Kl (Figure A-10) presented at the end of this Addendum.

The 9-track read head is connected to the Data K1 board via J4. Jumper wires W102 and Wl03 provide direct connections between J4 and the read preamplifier via input resistors R103 and R104. The center-taps of the 9 -track read heads are returned to $0 v$ through jumper wire W3. CR101-104, CR107-110, C101, C102, R101, R102, R109, R114, and Q102 are omitted in the PE/NRZI 9-track dual stack configuration.

R103 and R104 are the input resistors to the operational amplifier UllB. R103, in conjunction with the feedback network, determines the gain of the preamplifier. R104 and R105 are utilized to balance the input of the amplifier, which, in turn, determines the preamplifier common mode rejection ratio.

C42 and C43 are decoupling capacitors for the $\pm 10 \mathrm{v}$ power supplies. C103, R107, and Cl04 are compensating components for the operational amplifier. These components are required to control the open loop response of the preamplifier and to assure stability at all frequencies. The preamplifier features electrically selectable gain and bandwidth parameters. Consider the example in Figure A-14.


Figure A-14. Operational Amplifier

The gain of the system from input to output is determined by the ratio of feedback current (I2) to output voltage Vo. Because the operational amplifier has a very high open loop gain the input voltage required for a specified output (up to the supply voltage) is negligible. The voltage at node (1) is therefore nearly zero at all times. Furthermore, since the operational amplifier input impedance is high, its input current is negligible. Therefore, $I 1=I 2$, since $V(1=0$.

$$
\begin{aligned}
& \mathrm{I} 1=\frac{\mathrm{VI}}{\mathrm{RI}} \\
& \mathrm{I} 2=\frac{\mathrm{V} 2}{\mathrm{R} 2}
\end{aligned}
$$

Since

$$
\begin{aligned}
& R 2>R 3, \\
& V(2)=\text { Vo } \frac{R 3}{R 3+R 4} \text { (at low frequencies) }
\end{aligned}
$$

Thus

$$
\frac{\mathrm{VI}}{\mathrm{RI}}=\frac{\mathrm{V}(2)}{\mathrm{R} 2}=\operatorname{Vo} \frac{\left(\frac{\mathrm{R} 3}{\mathrm{R} 3+\mathrm{R} 4}\right)}{\mathrm{R} 2}
$$

Therefore

$$
\frac{\mathrm{VO}}{\mathrm{VI}}=\operatorname{gain}=\frac{\mathrm{R} 2}{\mathrm{R} 1} \frac{1}{\left(\frac{\mathrm{R} 3}{\mathrm{R} 3+\mathrm{R} 4}\right)}=\frac{\mathrm{R} 2}{\mathrm{R} 1} \quad\left(\frac{\mathrm{R} 3+\mathrm{R} 4}{\mathrm{R} 3}\right)
$$

It can therefore be said that the gain is equal to $\frac{\mathrm{R} 2}{\mathrm{R} 1} \times \frac{1}{\text { voltage divider ratio }}$ where the voltage divider is defined as R3 and R4. In the above example:

$$
\begin{aligned}
& R 1=R 103 \\
& R 2=R 106 \\
& R 3=\text { (set value of R108) } \\
& R 4=R 111
\end{aligned}
$$

The gain in the foregoing example was for the 9-track NRZI mode. Cl06 is a dc blocking capacitor and, because of it, there is no dc voltage divider action. The dc gain of the circuit is therefore lower than the ac gain, minimizing dc offset in the output.

Field effect transistor (FET) Q101 acts as a switch. When its gate is at -10 v , it appears as an open circuit (between drain and source). When the gate is forward-biased, it appears as a short circuit ( $\leq 100 \Omega$ ).

Turning Ql01 on places Rll2 in parallel with Rlll. This lowers the value of R 4 in the previous example, which decreases the gain for PE operation. The PE gain must be decreased to compensate for the 6 db per octave rise gain characteristic of differentiator U17B.

The high frequency response of the preamplifier is rolled off at approximately three times the highest data frequency. This is done to improve the signal-to-noise ratio while minimizing phase non-linearities. The breakpoint in NRZI operation is defined by

$$
\mathrm{f}=\frac{1}{2 \pi(\mathrm{R} 111)(\mathrm{C} 105}
$$

It is therefore independent of gain. The corner frequency in PE operation is higher than in NRZI due to the parallel combination of R111 and Rll2. The ratio of corner frequencies is, in fact, inversely proportional to the ratio of gains.

The gain of the preamplifier, as described, is raised for 9-track NRZI operation and lowered for PE operation. The bandwidth is extended for PE operation. R113 is gate current limiting resistor for Q101. Rllo provides an output current bias for UllB which reduces crossover distortion. The output of the preamplifier can be observed at TP101. Values for R103, R104, Rlll, Rll2, and Cl05 are a function of tape speeds and head outputs.

The output of UllB is connected to an active differentiator and a NRZI threshold detector. The function of these circuits was described in Section IV.

The differentiator is of classical design with the addition of two highfrequency poles (rolloffs). The first pole is defined by

$$
\mathrm{f}=\frac{1}{2 \pi(\mathrm{R} 115)(\mathrm{C} 107)},
$$

the second pole is defined by

$$
f=\frac{1}{2 \pi(\mathrm{R} 117)(\mathrm{C} 108)}
$$

These break points roll the high frequency response off to improve the signal-to-noise ratio. The overall gain is controlled by the equation: A = Rll7 (2 $\pi$ f) (Cl07) (low frequency). As in the preamplifier, Cl09, Rll8, and Cll0 are compensation components for the operational amplifier. R116 provides a 0v reference for the operational amplifier. C52 and C53 are power supply decoupling capacitors. The output of the differentiator can be observed at TP102.

U27 and U36 are employed as voltage comparators. Their outputs are coupled to two 3-input NAND gates. For ease in understanding their operation, the internal schematic has been depicted on Schematic 102325. Input polarities have been reversed with respect to those of the manufacturer, since the output considered will be the input of the NAND gate.

The voltage comparator output is true (high) when the positive (+) input voltage is more positive than the negative input voltage (-). The input resistor R122, in conjunction with the feedback resistor R126 and capacitor Cll4, provide positive feedback. This positive feedback is ac-only with a time constant considerably less than a bit-cell period. It provides hysteresis at the time of output change to prevent multiple edge transitions.

U46 performs the functions of "NOR" and 'INVERT". It is a standard DTL gate. TP105 is provided at the "OR" output of the NRZI peak detector. The output of the peak detector, a negative-going pulse for each "one" is connected through R130 to a skew test point for checking tape path alignment.

A jumper from Jl-12 to Jl-3 connects the peak detector output to the DTL J-K staticiser flip-flop U56B.

The operation of the staticiser flip-flop was explained in the companion document. Its output is connected to line driver U53A which is an open collector, high current, TTL inverter. U53A drives the interface line to a low level through its output transistor when the state of the staticiser flip-flop is a logical "l".

In PE operation, voltage comparator U27 is not used. Its common input (pin 6) is low, causing a logical "l" at both outputs, continuously enabling U36. PE data must be differentiated before threshold detection is possible. The output of voltage comparator U36 (pin 9) is used to drive the PE envelope detector (Q103, etc.). PE data are still passed through U46 but are stopped at the staticiser flip-flop since its clear input is held continuously low during PE operation.

The PE envelope detector (Q103 and associated circuitry) serves to make a steady signal out of the always pulsing threshold detector output U36 (pin 9). R127 increases the output voltage of U36 in the high state from approximately 3.5 v to 5 v . A high input to CR105 signifies the data is of sufficient amplitude for valid data output.

This high input charges Cll5 (through CR105) from its "no data" state of approximately +2.3 v to near +4.3 v . The emitter of Q 103 is connected to $\mathrm{a}+3 \mathrm{v}$ source. Since its base voltage (same as voltage across Cll15) is higher than its emitter voltage the transistor is cut off. When Q103 is cut off, R129 discharges C116 from +2.3 v toward -5 v . When the voltage across Cll6 passes through 0 v , the output of the voltage comparator within U41-B goes high. This enables the gate of U41-B. C116 continues discharging until CR106 clamps its voltage at -0.7 v . This improves recovery time at the end of the envelope.

As long as pulses continue to drive the envelope detector, Cll5 will remain charged, Q103 cut off, and the output of voltage comparator U41-B true.

After the last pulse has come through the threshold detector, Cll5 is allowed to discharge through R128 to +2.3 v . The voltage does not go below +2.3 v because the base emitter junction of Q 103 clamps the level at approximately one diode drop below the +3 v reference supply. This forward-biasing causes Q103 to conduct. When Q103 conducts, it charges Cll6 back to +2.3 v , thus disabling the output gate of U41-B (voltage comparator output goes low). The timing of the circuit is controlled by two time constants: R128-C115 and R129-C116. R128 and Cl15 determine the period after the receipt of the last threshold pulse until the envelope signal goes false. This period is typically set to two bit-cell periods. R129 and Cl16 determine the time from the receipt of the first threshold pulse to the transition to a true envelope state. This period is typically set to four bit-cell periods.

The gate of U41-B passes data (pin 8) when both the RPE and MOTION, and envelope signals are true. It also inverts the data which is corrected for by inverter U54-F. The output driver U53-F performs the line driver function.

In addition to the data and clock outputs, there are three status signals appearing on the output lines of Data Kl. They are INRZ, I7TR, ISPEED. All these outputs are gated with SLTA. U57-A, U12-A, and U12-B are the output driver gates for these status signals. SPEED is true only on dual speed models when the transport is operating at the low speed (PE mode). Jumper W1 is installed for all other models to keep ISPEED false (high).

U57-B serves as a NOR gate for all staticiser flip-flops. Any staticiser going to a true output state causes its $\bar{Q}$ output to go low, thus making U57-B (pin 8) true (high). This true level enables the character gate (dynamic deskew and clock generator). There are three adjustment potentiometers for the character gate circuit; R35 controls the 9-track period, R30 and R24 control the 7-track High and Low densities, respectively. Transistors Q5, Q6, and Q7 determine which of the potentiometers are connected to the timing circuit. Only one potentiometer is enabled at any one time. In the dual format, PE/NRZI 9-track, only R35, Q5, and the associated circuitry need to be considered. Q6 and Q7, and associated circuitry are omitted.

The period of the character gate is determined primarily by Cll and the setting of the R 35 potentiometer. When the output of the NOR gate (U57-B) is false (low), Q8 conducts. When Q8 is conducting, the voltage across Cll is pulled up to nearly $+5 v$ through R37. This high state raises the voltage on the base of Q10 until it conducts. The conduction of Q10 causes Q13 to cut off, making TP2 high (approximately +5 v ). The base voltage of Q11 determines the threshold voltage (switching point) of Q10.

When the output of NOR gate U57-B goes high, Q8 cuts off. Cll begins discharging to $-5 v$ through CR1, R17, and R35. When the voltage across C11 passes through the threshold voltage of Q10 (minus the drop of CR4), transistor Q13 conducts. This signifies the end of the character gate period. R44 and C14 provide a small amount of ac hysteresis to prevent multiple edge transitions.

As previously mentioned, Q11 controls the threshold of Q10. Its base voltage equals the base threshold voltage of Q10. The base voltage of Q11 is set to a value determined by transistor Q12 which is turned on through R51. This pulls the base voltage of $Q 11$ to +0.7 v as limited by CR5. R52 is the pull-up and collector current limiting resistor.

Read Data Strobe (RDS) pulses are required for NRZI operation. The pulse is negative-going as seen at TP15 (interface output J103 pin 2). It is generated by differentiating the output of the character gate through C 25 and R56 in parallel with R59. Its pulse width is approximately $2 \mu \mathrm{sec}$.

After each RDS pulse, the staticiser flip-flops must be reset. This requires a pulse after the trailing edge of RDS. The integrator circuit (RC delay) formed by R58, R71, and C26 perform this function. The input of U18-E and U18-F sees a true (high) level after RDS. This high signal causes the outputs of U18-F and U18-E to go low, thus clearing the staticiser flip-flops. When the flip-flops reset, the output of the "NOR" gate (U57-B) goes low, causing Q8 to conduct, charging C11 back to +5 v , and resetting the character gate for the next byte of data. It should be noted that when there is no tape motion or the system is in the PE mode (MOTION is low and the RPE level is high) U6-A and U6-B will hold the input of Ul-F low, thereby causing a continuous clear signal to all staticiser flip-flops.

Resistor R66 is a pull-up resistor for all unused inputs of voltage comparator U36 and its counterparts. U18-B and R64 form a high current driver which controls the mode of the NRZI threshold detectors.

Transistor Q15, in conjunction with resistors R60, R61, R62, and diode CR6 form a 3v source for the PE envelope detectors (e.g., Q103, Q104). C27 through C30 are decoupling capacitors.

Ull-A and its associated circuitry form the PE threshold generator. When operating in the NRZI mode, the output of U11-A is 0 v . In the PE Read mode the output voltage is one of two values, the nominal value is the highest. It is achieved by causing both $Q 3$ and $Q 4$ to conduct. This passes a current through R21, a voltage divider. The voltage at R21 is equal in sign and magnitude to the output voltage. The operational amplifier (Ull-A) has a closed loop gain of one, as determined by R22 and R28. R23 does not affect the gain but balances the dc input impedance to reduce dc offset errors in the output. When IRTH2 goes true (low), the lower threshold voltage is selected. This is half of the nominal value and is achieved by turning Q4 off, reducing the current through R21 to half of its previous value. In the PE/Write model, a third threshold, the highest of all is generated by turning Q16 on.

C5, R29, and C6 are compensation components for the operational amplifier Ull-A. Capacitors C21 through C24 are for decoupling.

The NRZI threshold generator is bi-polar (complementary voltages) and consists of U 2 and its associated circuitry. The output has one of two values; high during write, and low during read. The high value is determined by the ratio of R25 to the parallel combination of R13 and R14 times 5v. When RTH2 goes low, Q2 is turned off. This essentially raises the input resistance, thereby decreasing the output voltage. R20 provides a 0 v reference for the operational amplifier and minimizes dc
offset errors on the output. U2-B is a unity gain inverting amplifier employed to yield the inverse (positive voltage) of the output of U2-A. R32 and R39 are equal, thus yielding unity gain. R33 serves the same purpose as R20. W4 is omitted and RTH2 level, generated in the write card controls the threshold levels.

C3, R26, C4, C12, R40, and C13 are compensation components for both halves of operational amplifier U2. C17 through C20 and C7 through C10 are decoupling capacitors. All threshold voltages are available at test points (refer to Figure A-13 or Schematic 102325).

The 7/9-track head switching controller is made up of transistors Q1, Q9, and their associated circuitry.

In the PE/NRZI Read and Write Dual Format models, only the 9-track head is used for both modes of operation; the head switching controllers are not used. The same is true for CR101, CR102, CR103, CR104, C101, C102, R101, and R102 at the input of the preamplifier. These are left off the board and replaced by jumpers W102 and W103 to connect the head directly to R103 and R104.

The read head center taps are returned to ground by W3. Q14 and associated components control the PE gain switching FETs.

The following is a description of the PE/NRZI Write PCBA (refer to Schematic 102307 and Assembly 102308).

This PCBA is a dual format PE/NRZI Write which measures 7.0 inches by 10.25 inches. It is used in conjunction with the Data K1 PCBA and is hinge-mounted on the Data K1 PCBA to facilitate access to components on the Data K1 PCBA. The PE/NRZI Write PCBA contains all the circuitry necessary for writing PE or NRZI data.

Figure A-15 illustrates the placement of connectors and test points. Connector J26 receives power and control signals from the Tape Control PCBA, these signals are also routed to J25 which connects to the Data K1 PCBA. The write head cable connector is coupled to J24. J23 is omitted. Pl04 is a 34 -pin plug which connects into J104 on the Data Kl and receives all the interface write data signals plus the write data strobe and WARS, IRTH1 and IRTH2 supplied by the formatter. These interface signals are then supplied to the board at J105 via a 34 -conductor flat cable. This cable, J105 and Pl04 are an integral part of the Write PCBA.

The circuit board operation is described in reference to circuit 100 (Parity channel) since the operation of the remaining channels are virtually identical. The PE/NRZI Write PCBA is designed to operate in both PE and NRZI modes, therefore, each mode will be described separately. Circuits which are common to both NRZI and PE will be described under the NRZI portion.


Figure A-15. PE/NRZI Write PCBA Test Point and Connector Placement

### 5.3.1 NRZI OPERATION

All interface signals relevant to writing data (IWD0, etc.), WRITE DATA STROBE (IWDS), WRITE AMPLIFIER RESET (IWARS), IRTHl and IRTH2, enter via Pl04 which, in turn, receives the interface signals from Jl04, located on the Data K1, and coupled to J102 which receives the interface signals from the formatter. All these interface signals are terminated by a resistor combination and an IC inverter. The terminating resistors are part of a 14 -pin dual in-line resistor pack.

Referring to circuit 100 , and assuming NRZI operation, NHID is HIGH, the level at U4-2 is low. Under this condition, U4 acts as a non-inverting device and its output at pin 3 will be of the same polarity as that of the input at pin l. When IWDP is set to a low level in order to write a one, Ul-6 will be high, which will cause both the J and K inputs to U7-B to be high, therefore conditioning this J-K flip-flop to toggle at the trailing edge of the clock input pulse WDS from Ul4-B, which is an inversion of the IWDS presented at the interface inputs. The $Q$ and $\bar{Q}$ outputs from U7-B condition the $J$ and $K$ inputs of U7-A. U7-A receives its.clock pulse via NOR gate U8-C from a deskew single-shot associated with each channel. This single-shot, formed by $\mathrm{U} 5-\mathrm{B}$ and circuit l00A, receives a $1 \mu \mathrm{sec}$ positive-going pulse (WDS2) coincident with the trailing edge of the IWDS, and provides individual write deskew for its associated channel. The output from $\mathrm{U} 5-\mathrm{B}$ pin 4 is a negative-going pulse of variable width controlled by R103 and, since for NRZI operation the level to U8-10 is held high, the low going pulse at U8-9 will be inverted and fed to the clock input of U7-A. The outputs of flip-flop U7-A will change state at the trailing edge of the clock input pulse, and will drive the write amplifier transistors Q102 and Q103, whose emitters are taken to approximately +5 v when the WRT POWER line (J26-4) is high. The transistor connected to the low (approximately 0 v ) output of the flip-flop will conduct and a current will flow in the associated half of the head winding, causing a one to be written on tape. When the WRT POWER line is low (approximately 0v), writing is
inhibited because the write amplifier transistors cannot be turned on. In operation, the write current is defined by resistors R110 and Rlll; Rll2 is a damping resistor.

The write flip-flop U7-A is primed for writing by the WRT and MOTION lines which are ANDed and inverted by U25-A and U2l-C. Write flip-flop U7-B is primed for writing by the AND combination of WRT, MOT, and WARS. These signals are applied to the $C_{D}$ inputs, pins 4 and 10 , of the flip-flops. Thus, when NWRT is low and MOT is high, the low level applied to pins 4 and 10 of the flip-flops is removed and writing is possible whenever the WRT POWER line is high.

The IWARS pulse received by inverted Ul-D is used to reset the U7-B flip-flop, the outputs of which conditions U7-A to write the LRC character at the end of the record. C10, R13, and Rl4 differentiate the IWARS pulse and generate a pulse coincident with the leading edge of the IWARS and, through OR gate Ull-B, drive the deskew single-shots, and the LRC is written in a deskewed manner.

The WDS2 pulse is generated at the trailing edge of the IWDS pulse. The WDS2 pulse width is determined by the differentiator C8, R4, and R6, driving one input of U8-A to a low level which makes U8-3 go high. This high level is inverted by Ul2-D whose output goes low. This low-going transition at the output of U16-D is coupled back to U8-1 through C9. R4, $R 6$, and R5 then pull pin 1 of $U 8$ to $+3 v$ with a time constant equal to (R5) •C9. The negative pulse at the output of U12-D is inverted twice by Ul2-C and Ul2-E and fed to the write deskew single-shot through Ull-B as a positive-going pulse, (WDS2) which starts the single-shot delay time.

The heads center taps are returned to -10 v for NR ZI operation through Q2 and to $-5 v$ for PE operation through Q4. For NRZI operation, NHID is high which makes the output of U12-A remain high and enables U2-1.

When the NWRT goes low in order to perform a write operation, U23-8 goes high and forces U2-3 to a low state disabling U2-B and providing a base current drive for Q1. If a reel of tape with a write enable ring is mounted on the transport, the WRT POWER line will be high and Ql will conduct. Conduction of Q1 applies a positive drive to the base of Q2 which will, in turn, conduct, providing a return path to -10 v for the heads center taps. When in the PE mode, NHID goes low and, through Ul2-A, disables U2-1. U2-3 is forced to go high, turning Q1 off and enabling U2-B by holding pin 2 high. When NWRT goes low, U2-6 also will be set low driving Q 3 on which in turn drives Q 4 into conduction. Conduction of Q 4 provides a return path to -5 v for the heads center taps.

### 5.3.2 PE OPERATION

When operating in the PE mode, the NHID line is set low. This low level, inverted by Ul4-C and again inverted by U12-A disables U8-B, U2-D, U25-C, and U2-A. The high output from Ul4 pin 6 enables AND gate U11-A and, through U12-F, clamps U12C output to a permanently low level. With all inputs to Ull-A set permanently high, its output will remain low. This low output keeps WDS2 from changing state since there is no write deskewing in PE. The write clock pulses are passed by UllA as negative-going pulses $1 \mu \mathrm{sec}$ wide, WDS3.

The input to U4-2 is set to a permanently high state; this causes U 4 to act as an inverter and its output will be of opposite polarity as that applied to pin 1. Therefore, IWDP and its complement are applied to the J and K inputs of $\mathrm{U} 7-\mathrm{B}$. At the trailing edge of WDS1, which is applied to the toggle input of U7-B from Ul4-A, flip-flops U7-B copies the inverse of IWDP.

The complementary outputs from U7-B are presented to the $J$ and $K$ inputs of U7-A. When the clock pulse WDS3 drives U8-10 to 0 v for approximately $1 \mu \mathrm{sec}$, U8-8 applies a $1 \mu \mathrm{sec}$ positive-going pulse to the toggle input of

U7-A. At the trailing edge of this clock pulse, flip-flop U7-A copies the signals presented to its $J$ and $K$ inputs and drives the write amplifier transistors Q102 and Q103. The read threshold voltages generated and used on the Data Kl board are controlled by the levels at J104-29 (RTH2) and at J104-33 (PEWTH). These controlling levels are generated as follows.

While in the Write mode NWRT is low, forcing U25-B output high; thus, the outputs of U23-C and U23-E are low. The output of U23-E clamps the U23-F output to 0 v and inhibits the IRTH2 receiver. Since U25-10 is low, the collector ORed outputs of U25-C and U23-A will both go to a high state, making J104-29 (RTH2) high. This high level is supplied to the Data K1 PCBA to generate the NRZI read while write or high threshold voltage.

While in the Read mode, NWRT is high, forcing U25-6 low and U23-6 high. Since the NRZ line is also high, U25-8 goes to a low state which clamps the output of U23-A to 0 v , inhibiting again the IRTH2 input, and keeping J104-29 (RTH2) low. This low level supplied to the Data K1 defines the Read Only or lower threshold voltage.

In the PE mode, the NHID line is low which makes the NRZ line at U23-3 low and applies a high level to U25-13. In the Write mode, NWRT is low, U25-6 is high, which makes both inputs to U25-D high, and U25-11 goes low, which makes Jlo4-33 (PE WTH) low. At the same time, U23-10 is low which inhibits the IRTH2 input and forces U23-2 high, for cing J104-29 (RTH2) high. The combination of PE WTH low and RTH2 high is utilized in the Data Kl to generate the PE Read While Write, or the highest of the three threshold levels used in PE. If the NWRT line is high, which implies a Read mode, U25-6 is low. This forces U25-11 high. Also, the clamp exerted on U23-12 by U23-10 is removed and the PE read thresholds are then controlled solely by the IRTH2 line. When IRTH2
is high, a high level is present at J104-29 (RTH2) which dictates the normal read, or the higher of the two read threshold levels. When IRTH2 is low, a low level is present at J104-29 (RTH2) which is interpreted as the extra low read threshold level.
6.1 ADJUSTMENT PROCEDURES, INTRODUCTION

The information contained in this section pertains to the Data Kl PCBA and the PE/NRZI Write PCBA utilized in PERTEC Dual format transports.

The adjustment procedures contained in this section should be referred to in lieu of the corresponding procedures in the companion document.
6. 2 READ PREAMPLIFIER GAIN (NRZI MODE)

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i. e., new or used.

Additionally, a read preamplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to dropouts.
6.2.1 TEST CONFIGURATION
(1) Load a 1600 cpi , all-ones ( 3200 frpi ) reference level tape (125 percent saturation) on the transport.
(2) Apply power to the transport.
(3) Apply tension and advance tape to Load Point.

### 6.2.2 TEST PROCEDURE (PE MODE)

The gains of the read amplifiers are checked with the transport operating in the PE mode.
(1) Select PE format (high density).
(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.
(3) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the read differentiators as viewed at TP102 through TP902 on the Data PCBA. Use TP4 as zero dc ground reference. The oscilloscope vertical sensitivity should be set to display 1.0 v per division (including any probe attenuation).
(4) Acceptable limits:

- 3.25 v peak-to-peak (maximum)
- 2.75 v peak-to-peak (minimum)


### 6.2.3 ADJUSTMENT PROCEDURE

When the acceptable differentiator output limits are exceeded, repeat the test procedure detailed in Paragraph 6.2.2. If the acceptable differentiator limits are still exceeded, adjust variable resistors R108 through R908 to3.0v peak-to-peak.

### 6.3 READ PREAMPLIFIER GAIN (NRZI MODE)

In considering the overall gain of the read system, it is important to note that the output of the read head is particularly dependent upon the type of magnetic tape used and the condition of the tape, i.e., new or used.

A read preamplifier whose gain is adjusted too high will result in amplifier saturation; gain which is set too low will increase the susceptibility to data errors due to dropouts.
6.3.1 TEST CONFIGURATION (NRZI MODE)
(1) Load a 800 cpi , 9 -track, all ones (3200 frpi) reference level tape ( 125 percent saturation) on the transport.
(2) Apply power to the transport.
(3) Apply tension and advance tape to Load Point.

### 6.3.2 TEST PROCEDURE

The gain of the preamplifiers must be checked in NRZI modes with the density switched low (HIGH DEN extinguished).
(1) Select low density (NRZI) operation.
(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.
(3) Using the signal probe of an oscilloscope, measure and record the peak-to-peak output amplitude of the read preamplifiers as observed at TP101 through TP901 on the Data PCBA. Use TP4 as zero dc ground reference. The oscilloscope vertical sensitivity should be set to display lv per division (including any probe attenuation).
(4) Acceptable Limits

- 6.0 v peak-to-peak (maximum)
- 4.0v peak-to-peak (minimum)


### 6.3.3 ADJUSTMENT PROCEDURE (NRZI MODE)

When the acceptable limits are exceeded, perform the following adjustments.
(1) Establish the test configuration described in Paragraph 6.2. 1 of this addendum.
(2) Apply a manual FORWARD command; tape will move forward at the specified velocity.
(3) Using the signal probe of an oscilloscope, observe the PE differentiator outputs at TP102 through TE902 on the Data PCBA. Adjust variable resistors R 108 through R908 associated with test points 3.0 v peak-to-peak.

NOTE
It is allowable to vary the PE differentiator outputs within acceptable limits in order to bring the NRZI preamplifier outputs to within acceptable limits.

### 6.4 THRESHOLD GENERATOR

Only the PE threshold is adjustable. The NRZI threshold is not adjustable. The following data concerning NRZI threshold values are given only as an aid to troubleshooting. Use TP4 as ground zero reference when taking the following threshold generation dc voltage readings.
(1) WRITE True

- TP5
- +1.45 v (maximum)
- +1.2 v (minimum)

■ TP7

- -1.45 v (maximum)
- -1.2 v (minimum)
(2) WRITE False TP5
- +660 mv (maximum)
- +540 mv (minimum)
- TP7
- -660 mv (maximum)
- -540 mv (minimum)


### 6.4.1 TEST CONFIGURATION (PE)

(1) Load a 1600 cpi (3200 frpi) reference level tape (125 percent saturation) on the transport.
(2) Apply power to the transport.
(3) Apply tension and advance tape to Load Point.
(4) Activate the HI DEN switch. The switch will become illuminated.

### 6.4.2 TEST PROCEDURE

(1) With RTH2 false (high), measure and record the voltage at TP6.
(2) Set RTH2 true by applying a ground to pin 1 of Ul on the Data PCBA.
(3) Measure and record the voltage at TP6 on the Data PCBA.
(4) Acceptable limits

- RTH2 False
- $+250 \pm 20 \mathrm{mv}$, single-speed models
- $+125 \pm 10 \mathrm{mv}$, dual-speed models
- RTH2 True
- $+125 \mathrm{mv} \pm 10 \mathrm{mv}$, single-speed models
- $+60 \mathrm{mv} \pm 5 \mathrm{mv}$, dual speed models
(5) The voltage at TP6 must be $0 \pm 30 \mathrm{mv}$ in the NRZI mode. In PE; the Read While Write threshold level, Write true, must be
- $+750 \pm 30 \mathrm{mv}$, single-speed models


### 6.4.3 ADJUSTMENT PROCEDURE

When the acceptable limits are exceeded, the following adjustments are performed.
(1) With RTH2 false, observe the threshold output voltage at TP6. Adjust R2l on the Data PCBA to $+250 \pm 20 \mathrm{mv}$ for single-speed models or to $+125 \pm 10 \mathrm{mv}$ for dualspeed models.
(2) Set RTH2 true by applying a ground to pin 1 of Ul on the Data PCBA.
(3) Observe the threshold output voltage at TP6. The voltage must be $50 \pm 5$ percent of the value set in Step (1).
(4) Set the Write to true (low) and observe that the voltage at TP6 goes to $+750 \pm 30 \mathrm{mv}$ for single-speed models or to $+375 \pm 15 \mathrm{mv}$ for dual-speed models.

### 6.5 CHARACTER GATE

The character gate, located on the Data PCBA, is utilized during NRZI operation to set the period during which valid data are passed by the staticisers. The length of the gate is defined as the period from the rise (leading edge) of the waveform at TP1 to the rise (trailing edge) of the waveform at TP15. Potentiometer R35 sets the 9-track character gate length.

NOTE
Tape Speed and Preamplifier Gain must be checked and adjusted prior to adjusting the Character Gate.
6.5 .1 TEST CONFIGURATION
(1) Load an all-ones 800 cpi , 9-track tape, on the transport.
(2) Apply power to the transport.(3) Apply tension and advance tape to Load Point.
(4) Set the HI DEN switch to the appropriate mode.(5) Connect a 220-ohm resistor from TP15 of the Data PCBAto +5 v .
(6) Depress and release the ON LINE control.
(7) Apply a ground to J101-C (ISFC); tape will move forwardat the specified velocity.
6.5.2 TEST PROCEDURE
(1) Connect the Trace One probe of an oscilloscope to TPl and the Trace Two probe to TP15 of the Data PCBA.
(2) Trigger the oscilloscope on Trace One (ac positive).
(3) Measure and record the period between the waveform rise at TP1 (Trace One) to the waveform rise at TP15 (Trace Two).
(4) Calculate the bit-cell time of the recorded tape by the following equation.

$$
\begin{aligned}
\tau & =\frac{1}{\mathrm{DS}} \\
\mathrm{~T} & =0.46 \tau \\
\mathrm{~T}_{\mathrm{ul}} & =0.48 \tau \text { (upper limit) } \\
\mathrm{T}_{11} & =0.44 \tau \text { (lower limit) }
\end{aligned}
$$

where

$$
\begin{aligned}
\mathrm{D} & =\text { Density (cpi) } \\
\mathrm{S} & =\text { Speed (ips) } \\
\mathrm{T} & =\text { Character Gate Length } \\
T & =\text { Bit-Cell Period }
\end{aligned}
$$

(5) Acceptable limits

The value obtained in Step (3) is the actual character gate period. This value must be between $T_{u l}$ and $T_{11}$ as calculated in Step (4).

### 6.5.3 ADJUSTMENT PROCEDURE

(1) Establish the test configuration detailed in Paragraph 6.5.1.
(2) Perform test procedure detailed in Paragraph 6.5.2, Steps (1) through (5).
(3) Observe the character gate length and set variable resistor R35 to 46 percent of the bit-cell period ( $\tau$ ).
6. 6 READ SKEW MEASUREMENT AND ADJUSTMENT

### 6.6.1 TEST CONFIGURATION

(1) Perform the Read Amplifier checks and adjustments described in Paragraphs 6.2 and/or 6.3 of this Addendum.
(2) Load a 800 cpi IBM Master Skew Tape (IBM 432640) (or equivalent) on the transport.
(3) Apply power to the transport.
(4) Apply tension and advance tape to Load Point.
(5) Set the HI DEN switch off (extinguished).
6.6 .2 TEST PROCEDURE
(1) Using an oscilloscope, observe the falling edge of the waveform observed at TPll (SKEW) on the Data Kl PCBA.
(2) With the oscilloscope connected as in Step (1) measure and record the length (in $\mu \mathrm{sec}$ ) of the falling edge of the waveform at TP11. This measurement should be taken between the 95 - and 5 -percent points of the waveform.
(3) Multiply the time obtained in Step (2) by the tape speed in inches per second (ips) to determine the skew in $\mu$ inches.
NOTE
The observed waveform contains both the static and dynamic components of the total skew.
(4) If the total (dynamic and static) skew is less than 150 $\mu$ inches, no adjustment should be attempted.
(5) In the event that total skew is in excess of $150 \mu$ inches, determine if the dynamic skew exceeds $100 \mu$ inches.
NOTE
If dynamic skew is in excess of $100 \mu$ inches, the tape guiding system should be checked for dirt, wear, and alignment.
(6) If dynamic skew is less than $100 \mu$ inches and the total skew exceeds 150 inches, proceed with the adjustment procedure in Paragraph 6.6.3.
NOTE
This test procedure should be performed in both forward and reverse directions.

### 6.6.3 ADJUSTMENT PROCEDURE

(1) Establish test configuration described in Paragraph 6.6.1, Steps (1) through (5).
(2) Perform the adjustment procedure contained in Section VI of the companion document.

### 6.7 WRITE SKEW ADJUSTMENT

The following procedure is provided to allow adjustment of write deskew. This adjustment procedure is to be used in conjunction with the Read Skew Measurement contained in Paragraphs 6.6.1 and 6.6.2 of this Addendum, and the Adjustment Procedure contained in Section VI of the companion document.
6.7.1 TEST CONFIGURATION
(1) Establish the test configuration for Read Skew Measurement and Adjustment contained in the companion manual.
(2) Ensure that the HI DEN switch/indicator is extinguished.
6.7.2 TEST AND ADJUSTMENT PROCEDURE
(1) Perform the Read Skew Measurement contained in Paragraphs 6.6.1 and 6.6.2 of this Addendum, and the Adjustment procedure contained in the companion document.
(2) Remove the IBM master skew tape and load a reel of tape with a Write Enable ring installed.
(3) Set R103-R903 to their center positions. These resistors are located on the PE/NRZI Write PCBA. Refer to Assembly Drawing 102308 or Figure A- 15 for placement.
(4) Bring the transport to Load Point.
(5) Place the transport On-Line.
(6) Apply a ground to the interface ISLT line.
(7) Apply a ground to the interface ISFC line.
(8) Apply a ground to interface lines IWDP and IWD0 through IWD7 of the Data PCBA.
(9) Apply negative-going pulses ( +3 v to 0 v ) of $2 \mu \mathrm{sec}$ duration at the specified transfer rate to the interface line IWDS (J102 pin A) on the Data PCBA.

NOTE

$$
\begin{aligned}
& \text { Transfer Rate }=\mathrm{D} \times \mathrm{V} \\
& \text { where } D=\text { Density in cpi } \\
& \mathrm{V}=\text { Speed in ips } \\
& \text { i. e., } 20 \mathrm{Kc} \text { at } 800 \mathrm{cpi}, 25 \mathrm{ips}
\end{aligned}
$$

(10) Tape will move forward at the synchronous speed and a tape will be written with ones recorded in each track.
(11) Observe the waveform at TP1l of the Data Kl PCBA.
(12) Adjust variable resistors R103-R903 on the PE/NRZI Write PCBA for minimum skew. The total measured skew should be less than $200 \mu$ inches or one-sixth of the period of the waveform observed at TPll on the Data Kl PCBA.
(13) Rewind the tape to BOT and rewrite a section of all-ones tape. Do not make any adjustments of R103-R903 during this step.
(14) Apply a ground to the interface ISRC line. Tape will move in the reverse direction at the synchronous speed.
(15) Observe the waveform at TPll on the Data Kl PCBA. The total skew measured should be less than $200 \mu$ inches or one-sixth of the period of the waveform. If the skew is in excess of the specified limits, repeat this procedure.

THIS PAGE LEFT BLANK INTENTIONALLY


Figure A-7. PE/NRZI Write Logic


Figure A-8. NRZI Data Recording, Timing Diagram

(1) THIS DIRECTION OF CURRENT

IS SUCH AS TO MAGNETIZE
TAPE IN THE DIRECTION OF
THE IRG.

Figure A-9. PE Data Recording, Timing Diagram


Figure A-10. Data Recovery, Functional Block Diagram


POSITIVE NRZI THRESHOLD OUTPUT UII


NEGATIVE NRZI THRESHOLD OUTPUT U12

dIfferentiator output u4 NOTE INVERSION


Negative voltage comparator output us

positive voltage comparator output ub


ONE SHOT UI6


I///, OR NUN = INDETERMINATE STATE

Figure A-11. NRZI Data Reproduction, Timing Diagram


Figure A-12. PE Data Reproduction, Timing Diagram




TABLEII (2)

table I (1)

| PART NO. | REF DESIGNATION |
| :--- | :--- | | PARF N. | RLF DESTGNA |
| :--- | :--- |
| $100-1025$ | R4,9,12,20,24, |

 | $100-1525$ | R6 |
| :--- | :--- |
| $100-1825$ | R7,8,10,11,17,18, |

 \begin{tabular}{|l|l|}
\hline $100-3315$ \& R45 <br>
\hline $100-3225$ \& R4 <br>
\hline

 $100-3325$ 

\hline $100-3325$ \& R14 <br>
\hline $100-3915$ \& R3 <br>
\hline

 

\hline $100-4715$ \& R5,19,26 <br>
\hline
\end{tabular} 100-

$\begin{array}{r}100-8 \\ \hline \\ \hline\end{array}$

|  |  |
| :--- | :--- |
|  |  |
|  |  |


| $101-3915$ | R25 |
| :--- | :--- |
|  |  |
|  |  |
| $102-1815$ | R21 |


| $130-4715$ | $C 8$ |
| :--- | :--- |
|  |  |
| $131-1020$ | 9 |


| $131-1020$ | $\mathrm{C9}, 10$, |
| :--- | :--- |
|  |  |

table III

PART NO. REF DESIGNATION \begin{tabular}{|l|l|}
\hline $100-2725$ \& R105 THRU 905 <br>
\hline

 

$1223-1030$ \& R103 THRU 903 <br>
\hline 200

 

\hline $200-4123$ \& Q101 THRU 901 <br>
\hline $100373-02$ \& <br>
\hline

 

\hline $100373-02$ \& W1, ,101 THRU 901 <br>
\hline $100-1825$ \& RII2 THRU 912 <br>
\hline

 

\hline $100-1825$ \& R112 THRU 912 <br>
\hline $131-1020$ \& C102 THPL <br>
\hline

 

\hline $131-3320$ \& Clio3 THRU 903 <br>
\hline
\end{tabular}















[^0]:    *Foldout drawing, see end of this section.

[^1]:    Foldout drawing, see end of this Addendum.

[^2]:    ${ }^{\text {* }}$ Foldout drawing, see end of this Addendum.

[^3]:    Foldout drawing, see end of this Addendum.

[^4]:    *Foldout drawing, see end of this Addendum.

