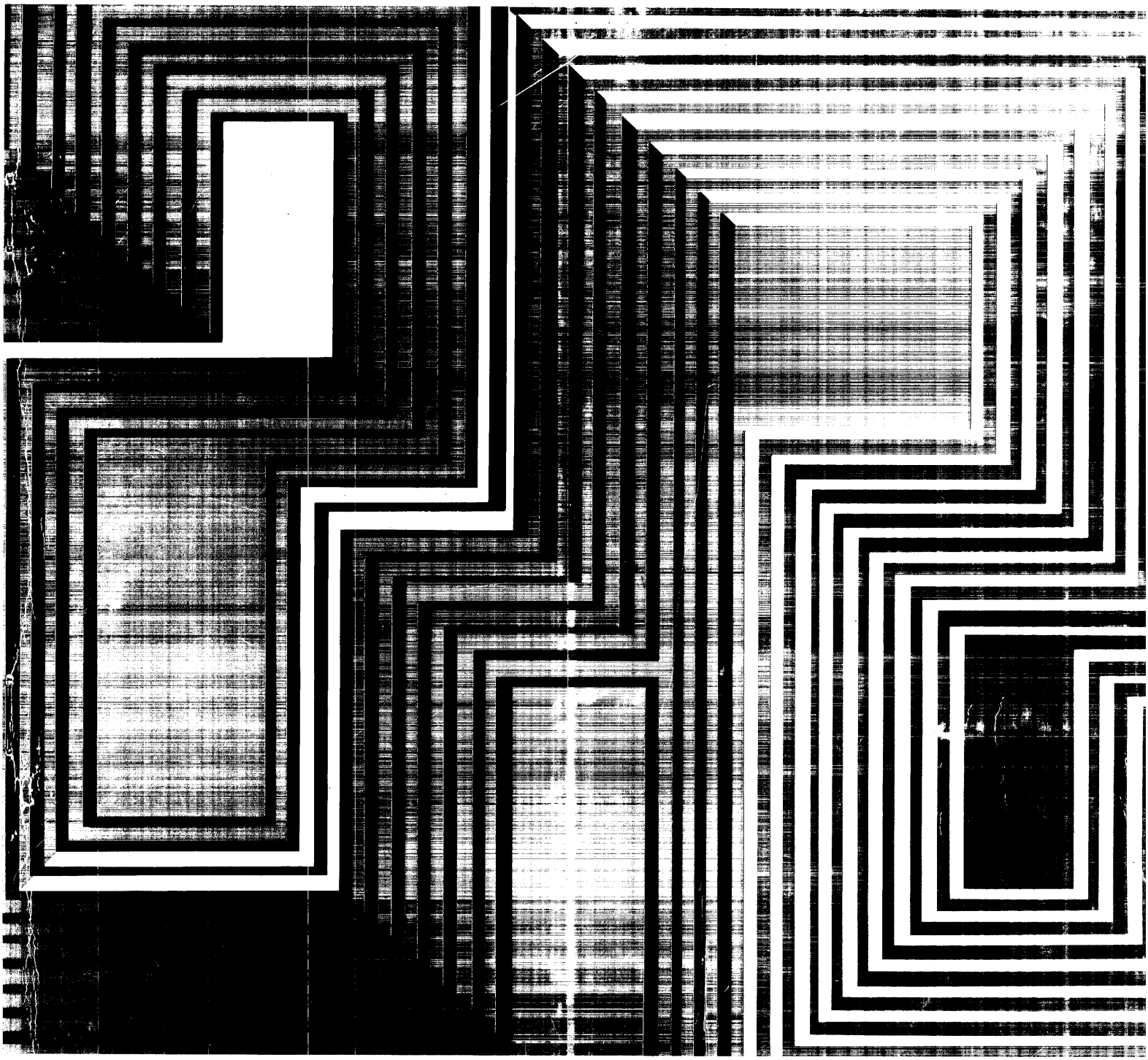


IM88-0428-00
HARDWARE INSTRUCTION MANUAL
ND 4410 DATA ACQUISITION AND
DISPLAY SYSTEM

NUCLEAR DATA INC

NUCLEAR DATA, INC.
Post Office Box 451
Palatine, Illinois 60067

March, 1972

Preliminary Edition

IM88-0428-00
HARDWARE INSTRUCTION MANUAL
ND 4410 DATA ACQUISITION AND DISPLAY SYSTEM

TABLE OF CONTENTS

SECTION	TITLE	PAGE
I	INTRODUCTION	1-1
	1-1. General Description	1-1
	1-6. Options	1-2
	1-8. Functional Description	1-3
	1-10. Analog to Digital Converter Module	1-3
	1-14. ND812 Central Processor	1-5
	1-16. Control Module	1-5
	1-18. Display Oscilloscope	1-5
	1-20. Power Supply	1-5
	1-22. Specifications	1-5
II	EQUIPMENT PREPARATION	2-1
	2-1. General	2-1
	2-3. Preparation for Use	2-1
	2-4. Unpacking and Inspection	2-1
	2-6. System Installation and Interconnections	2-1
	2-10. Preliminary Check-Out	2-3/2-4
	2-12. Initial Start-Up Procedure	2-8
III	OPERATING INSTRUCTIONS	3-1
	3-1. General	3-1
	3-3. Control and Indicator Functions	3-1
	3-5. Operational Considerations	3-10
	3-6. Specific Hardware Considerations	3-10
	3-7. Analog to Digital Converter Module	3-10
	3-16. Control Module	3-11
	3-18. Oscilloscope Calibration	3-12
	3-19. Pulse Height Analysis Experiment	3-13
	3-20. Specific Software Considerations	3-15
	3-21. ND4410 Instruction Repertoire	3-15

SECTION	TITLE	PAGE
IV	FUNCTIONAL DESCRIPTION	4-1
	4-1. General	4-1
	4-3. General Functional Description	4-1
	4-5. Functional Block Diagram Description	4-2
	4-24. Detailed Functional Description	4-5
	4-26. Control Circuit Description	4-5
	4-56. Control Timing For Acquisition Modes	4-12
	4-58. Program Control Mode	4-12
	4-59. DMA Increment Mode	4-12
	4-60. DMA List Mode	4-12
	4-61. Input/Output Signal Description	4-16
V	MAINTENANCE	5-1
	5-1. General	5-1
	5-3. Maintenance Philosophy	5-1
	5-6. Equipment Required For Maintenance	5-1
	5-8. Maintenance Controls, Indicators, and Test Points	5-2
	5-10. Preventive Maintenance	5-2
	5-11. Periodic Inspection	5-2
	5-12. Performance Standards Tests	5-2
	5-15. DC Voltages and Power Distribution Tests	5-2
	5-16. ND812 Computer Tests	5-3
	5-17. ND4410 Control Module Tests	5-3
	5-23. Corrective Maintenance	5-6
	5-24. Alignment and Adjustment	5-6
	5-27. Horizontal Display Position Adjustment	5-6
	5-28. Vertical Display Position Adjustment	5-6
	5-29. Display Marker Position Adjustment	5-7
VI	REPLACEABLE PARTS LIST	6-1
	6-1. General	6-1
VII	DIAGRAMS	7-1
	7-1. General	7-1

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
1-1	ND4410 System with Various Options	1-2
2-1	Series 4410 System Interconnection Diagram	2-5/2-6
3-1	Control Module Front Panel Controls and Indicators	3-2
3-2	Typical System Set-Up for Pulse Height Analysis Experiment	3-14
4-1	Signal Inversion	4-1
4-2	ND4410 Control Module Functional Block Diagram	4-3/4-4
4-3	Signal Reference	4-6
4-4	Program Control Mode Timing Diagram	4-13
4-5	DMA Increment Mode Timing Diagram	4-14
4-6	DMA List Mode Timing Diagram	4-15
5-1	NIM Bin Connector, Dc Voltage Requirements	5-3
5-2	ND4410 Control Module, Adjustment Locations	5-7

LIST OF TABLES

TABLE	TITLE	PAGE
1-1	Basic ND4410 System Components	1-3
1-2	ND4410 Options	1-4
1-3	ND4410 Control Module, Physical and Functional Characteristics	1-6
1-4	ND812 Computer, Physical and Functional Characteristics	1-8

TABLE	TITLE	PAGE
1-5	50 MHz ADC, Physical and Functional Characteristics. . . .	1-9
1-6	NIM Bin and Power Supply, Physical and Functional Characteristics	1-12
3-1	Control Module, Function of Controls and Indicators	3-3
4-1	Input/Output Signals, Printed Circuit Board	4-16
4-2	Input/Output Signals, Printed Circuit Board 112	4-20
4-3	Power Connector	4-22
5-1	Required Test Equipment	5-1
5-2	ND4410 Control Module Display Circuits Test	5-4
5-3	ND4410 Control Module Front Panel Switch	5-5
6-1	Replaceable Parts List	6-1
7-1	Diagram Index	7-1

SECTION I.
INTRODUCTION

1-1. GENERAL DESCRIPTION

1-2. This manual contains instructions necessary to operate and maintain the ND4410 system, part number 88-0428, manufactured by Nuclear Data, Incorporated. The ND4410 system (figure 1-1) is a single parameter data acquisition and display system used for measurement, storage, display, and processing of data obtained in physical science research.

1-3. The ND4410 basic system consists of a Function Control Module, a 50 MHz Analog to Digital Converter (ADC), a Dead Time Monitor, an ND812 Central Processor with 4K memory (expandable to 16K), a Teletype Interface with Auto Loading, NIM Bin with three connectors, Bin power supply, Tektronix 602 display Oscilloscope (option), and Teletype (option). The basic system can be expanded to include up to eight ADC's (with a digitizing rate of 50 or 100 MHz), and the selection of an 8K, 12K, or 16K ND812 Central Processor (Refer to table 1-1 for description, part number and quantity of basic ND4410 system components). Also, various basic system options and peripheral options are available.

1-4. Several software packages for the ND4410 system are available. Current packages include a Basic Physics Analyzer, a Basic X-Ray Analyzer, and a Floating Point Physics Analyzer. The Basic Physics Analyzer package requires only 2K, 12 bits of core storage, leaving 1K of 24 bits for data storage. The Basic X-Ray Analyzer requires 3K of 12 bits, and the Floating Point Physics Analyzer requires 4K of 12 bits. Information on these packages and packages presently in work are available on request.

1-5. The operation and maintenance instructions contained in this manual cover the basic ND4410 system and are primarily centered around the ND4410 Control Module. Refer to the appropriate instruction manual for specific instructions on the Analog to Digital Converter, Dead Time Monitor, ND812 Central Processor, Teletype Interface with Auto Loading, Bin Power Supply, Display Oscilloscope, Teletype, and all system and peripheral options. Also, refer to the ND4410 Single Parameter Data Acquisition and Display System Software Instruction Manual for specific information on system software.

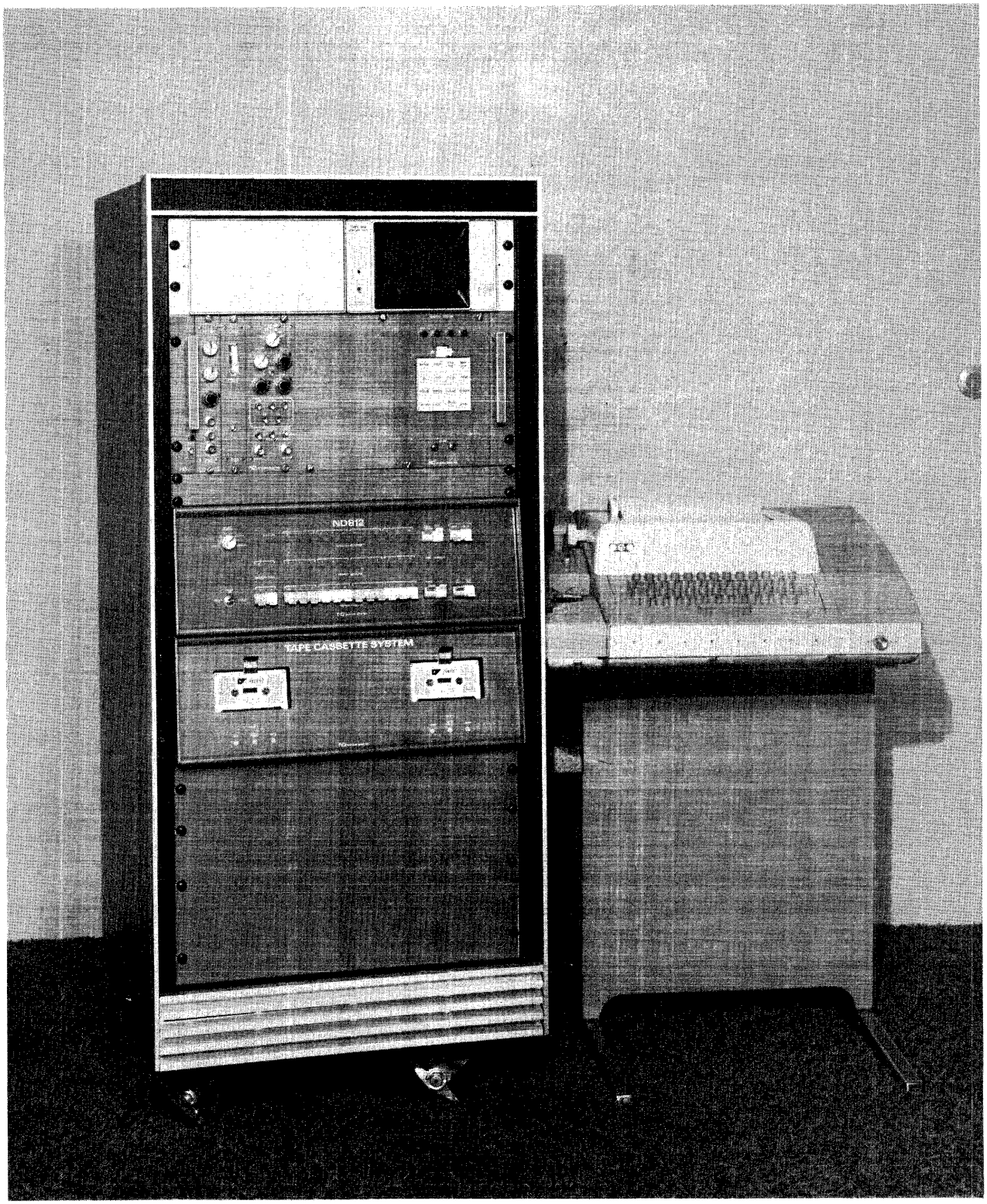


Figure 1-1. Typical ND4410 System with Various Options

Table 1-1. Basic ND4410 System Components

Description	Part Number	Quantity
ND4410 Function Control Module	88-0428	1
ND560 ADC, 4096, 50 MHz	88-0415	1
*ND565TM Dead Time Monitor	88-0435	1
ND812 Central Processor/4K x 12 Bit memory	88-0097/ 88-0096	1
Teletype Interface with Auto Loading	88-0481	1
NIM Bin with three connectors	88-0344	1
Bin Power Supply, +6 Vdc, 5A; +12 Vdc, 2.5A ±24 Vdc, 1A	88-0297	1

*Not required when optional 8192, 100 MHz ADC (part number 88-0426) is used.

1-6. OPTIONS

1-7. Basic ND4410 system options, peripheral options, and memory expansion options are given in table 1-2. Various bulk storage devices, magnetic tape I/O devices, paper tape I/O devices, hard copy devices, and miscellaneous ND812 options are also available. Information and price list on these devices and options are available on request.

1-8. FUNCTIONAL DESCRIPTION

1-9. There are three modes of software-controlled data acquisition. These are Program Control Mode, Buffer or List Mode, and Direct Memory Increment Mode. The Program Control Mode places restrictions on the digitized data following the selection of areas of interest. The 24-bit word transferred contains up to 15 bits of ADC data (32K channels), 3 bits to identify one ADC out of the possible eight, 1 bit for the clock, and 5 unassigned bits. The Buffer or List Mode transfers up to 24 bits directly into the computer memory. The number of ADC's used are initialized by software. The Direct Memory Increment Mode treats the ADC word as an address with the contents of the address being incremented creating a spectrum of counts versus channels.

1-10. ANALOG TO DIGITAL CONVERTER MODULE

1-11. The ND560 ADC is a highly versatile analog to digital converter designed for processing amplitude modulated signals, such as are encountered when measuring fast random phenomenon. It may also be used to sample dc or slowly varying voltages.

1-12. Data acquisition efficiency is enhanced by a 50 megahertz digitizing rate. The digitizing oscillator is crystal-controlled to ensure high, long term stability. In addition, all critical circuitry is temperature compensated to ensure drift free operation.

Table 1-2. ND4410 Options

Description	Part Number
Basic System Options	
ND4410 Digiplex - Two Function Control Module	88-0461
ND4410 Digiplex - Two Function Control/Digiplex - Four Option	88-0461/ 84-0152
Analog to Digital Converter, 8192, 100 MHz	88-0426
Digital Spectrum Stabilizer	88-0058
Two Input Zero Dead Time Multichannel Scaler	88-0477
Time of Flight	88-0145
Eight Input Router	88-0502
NIM Bin - 6 Connectors	88-0300
NIM Bin - 12 Connectors	88-0346
Basic System Peripherals	
Teletype Model TC33ASR Combination Punch Paper Tape and Page Printer	86-0085
Tektronix 602 Oscilloscope	86-0140
Rack Mount	86-0141
Filler Panel	86-0142
Hewlett Packard Model 1208B Oscilloscope	86-0199
Rear Terminal and Blanking Option	86-0200
Hewlett Packard Model 7004B XY Plotter	86-0149
Memory Expansion Options	
8K x 12 Bit Memory (4K to 8K Expansion)	84-0097
ND812 Memory Extension Unit with 4K x 12 Bit Memory (8K to 12K Expansion)	88-0431 84-0094
ND812 Memory Extension Unit with 8K x 12 Bit Memory (8K to 16K Expansion)	88-0431 84-0095
8K x 12 Bit Memory (12K to 16K Expansion)	84-0095

1-13. Conversion gain is selectable in binary increments from 128 to 4096 channels full scale. Front panel selection of group size in binary increments from 64 to 4096 allows resolution up to 4096 channels in a memory group of only 64 channel capacity. A digital zero shift selector is included which utilizes five toggle switches representing 256, 512, 1024, and 2048 channels. By placing these switches in the appropriate positions, the selected channel may be digitally moved to zero, automatically suppressing all previous channels. Any combination of switches may be used providing a maximum zero shift of 3968 channels.

1-14. ND812 CENTRAL PROCESSOR

1-15. The ND812 is a general purpose computer designed for the scientific researcher. The basic ND812 contains a 12-bit, 4K memory, with optional 8K, 12K or 16K memories available. This computer is extremely versatile, in that the entire core locations (up to 16K) are directly addressable by using two-word instructions. A total of 256 single-word or 4096 two-word I/O commands are possible. Other outstanding features are the 12 or 24-bit programmed I/O transfer, a four level priority interrupt, four micro-programmable pulses per I/O instruction, direct memory access, four arithmetic registers, hardware multiply and divide, and 100% integrated control logic circuitry.

1-16. CONTROL MODULE

1-17. The Control Module interfaces the ADC's and display scope with the ND812 Central Processor. Sixteen front panel pushbutton switches control the system, establish the number of channels displayed, increasing or decreasing the number of counts full scale, and the position of two data markers. Data contained between the markers can be totalized; read out by channel (with channel ID every eight channels); read out to an X-Y plotter; or altered by addition, subtraction, division and multiplication. A front panel pushbutton switch also initiates display of system parameters on the display oscilloscope.

1-18. DISPLAY OSCILLOSCOPE

1-19. The 602 display oscilloscope is a compact, solid state monitor with excellent resolution providing accurate displays of information from X, Y, and Z signal inputs. Display is provided on a 5-inch, flat-faced, rectangular cathode ray tube with an internal graticule. Signal inputs are via BNC connectors on the rear panel.

1-20. POWER SUPPLY

1-21. The bin mounted power supply is furnished with a 23-pin female bin interface connector for distributing power to the bin power connectors. The rear panel contains two line fuses, an ac line cord, and a switch for selection of 115 or 230 volt operation. This unit is also equipped with thermal cutouts which disconnect the ac line when the heat sink exceeds the preset temperature.

1-22. SPECIFICATIONS

1-23. Physical and functional characteristics for the ND4410 Control Module, ND812 Computer, 50 MHz ADC, and NIM Bin Power Supply are given in tables 1-3, 1-4, 1-5,

and 1-6 respectively. Refer to the appropriate instruction manual for specifications on all other modules and peripheral equipments.

Table 1-3. ND4410 Control Module, Physical and Functional Characteristics

Characteristic	Specification
Physical Characteristics	
Height	8.71 in
Width	5.36 in
Depth	9.7 in
NIM Compatible	four-wide module
Functional Characteristics	
Input/Output	Directly compatible with ND812 I/O Buss.
Accumulator Mode	Each event (24 bits) is transferred to the ND812 accumulators. The information contained in the 24 bits is then available for software processing. Communication via the interrupt, "trap" address is provided.
List Mode	Each event (24 bits) is transferred directly to the ND812 memory. The number of events contained in the list and the processing of the list is software selectable. Communication is via direct memory access, transmit.
Direct Memory Increment Mode	The ADC address for each event directly identifies a location in the ND812 memory and causes a read, add-1, write at that location. Communication is via direct memory access, increment.
Display Decoding	X-Axis: 10 bits Y-Axis: 10 bits
Display Output	Horizontal: 0 to 1V Vertical: 0 to 1V Blanking: +5V on, 0V blank

Table 1-3. ND4410 Control Module, Physical and Functional Characteristics (Cont'd)

Characteristic	Specification
Display Markers	Internal circuitry and software selection permit generation on the display scope of a marker (a full-scale vertical line) at any address.
Plotter Control	External connectors and software selection permit analog readout to a plotter, X-Y, incremental, or strip chart.
Function Control	16 software-selection pushbuttons provide control of analyzer functions.
Direction Control	Two-position switch selects direction of parameter movement.
Acquisition Control	An internal 100 MHz crystal-controlled time base permits software selection of acquisition time at 10 ms clock or live time gated intervals.
Data Erasure	Dual pushbuttons, which must be depressed simultaneously, prevent accidental erasure of stored data.
Mode Indication	Four front panel lamps provide indication of acquisition and display modes.
Power Requirements	+6 Vdc, 2A ±12 Vdc, 50mA

Table 1-4. ND812 Computer, Physical and Functional Characteristics

Characteristic	Specification
Physical Characteristics	
Height	7.00 in
Width	19.00 in
Depth	22.00 in
Functional Characteristics	
Memory	Magnetic core, 4096 words, 12 bits, 2 μS cycle time. Memory options: Minimum 4K, field expandable to 16K in 4K increments.
Addressing	Relative, indirect, and direct. Hardware multiple field control.
Arithmetic	Parallel, binary, fixed point, 2's complement. Hardware multiply and divide.
Instructions	Single and two-word instructions which include 25 memory reference instructions, three literals, and more than 50 arithmetic and register control instructions.
Input/Output	Interrupt: Programmable 4-level priority interrupt. Trap to any core location in first 4K of memory.
Programmed I/O Transfer	Transmit 12 or 24 bits. Receive 12 or 24 bits. Transmit 12 and receive 12 bits. Receive 12 and transmit 12 bits.
I/O Instruction	Includes four microprogrammable pulses for multi-function operation with single instruction.
Single-Word Instructions	256 possible I/O commands at 3 μS per instruction.
Two-Word Instructions	4096 possible I/O commands at 5 μS per instruction.

Table 1-4. ND812 Computer, Physical and Functional Characteristics (Cont'd)

Characteristic	Specification
Control, data, and sense lines	Total of 75 available on single connector.
Direct Memory Access (DMA)	6 megabits/s; read, load, increment or decrement on DMA with single cycle.
Accumulator	Dual accumulators with individual sub-accumulators.
Timing	16 MHz crystal-controlled clock assures absolute and drift-free timing.
Voltage Requirements	115/230 Vac ± 10%, 50/60 Hz, single phase.
Power Consumption	400W maximum

Table 1-5. 50 MHz ADC, Physical and Functional Characteristics

Characteristic	Specification	
Physical Characteristic		
Height	8.71 in	
Width	2.68 in	
Depth	9.70 in	
Functional Characteristics		
Conversion Gain	128, 256, 512, 1024, 2048 or 4096 channels full-scale.	
Digitizing Rate	50 MHz on all conversion ranges.	
ADC Conversion Time	Gain Setting	Conversion Time (μS)
	4096	6.0 μS + 0.02N
	2048	6.0 μS + 0.02N
	1024	6.0 μS + 0.02N
	512	6.0 μS + 0.02N

Table 1-5. 50 MHz ADC, Physical and Functional Characteristics (Cont'd)

Characteristic	Specification
	Gain Setting — Conversion Time (μS) 256 — 6.0 μS + 0.02N 128 — 6.0 μS + 0.02N N is equal to the number of address advances for a given input event. The fixed dead time includes initialization, pedestal rundown, delay line propagation, bad data flag ($\overline{ALT}$) check, etc.
Signal Inputs	Coupling: ac or dc, switch-selectable. Amplitude: 0 to +8V, nominal. Polarity: Positive monopolar or initially positive bipolar. Rise Time: 0.2 to 70 μS Duration: 1 μS, minimum. Internal Delay: 1 μS. Input Impedance: 1000 ohms.
Baseline Restoration	Type: Robinson. Input: Positive monopolar, operative in ac mode only.
Coincidence or Anticoincidence Input	Selection: Coincidence, anticoincidence or normal operation. Amplitude: 3 to 10V, ac or dc-coupled. Polarity: Positive from 0V reference. Duration: 1 μS minimum. Timing: Determined by internal modification which allows the coincidence or anticoincidence pulse to occur before or after the input event. Nominally set at 2 μS. Overlap of the input event is not necessary in either coincidence or anti-coincidence Input Impedance: 1000 ohms.
Strobe	Front-panel-switch-selectable for use in measuring slowly varying dc signals or rapidly determining the zero energy intercept.

Table 1-5. 50 MHz ADC, Physical and Functional Characteristics (Cont'd)

Characteristic	Specification
	Auto Position: Opens the linear gate for a pre-determined time, as selected by the LGT control. Rate is nominally 8,000 samples per second. An external 3 to 10V positive strobe pulse, 1 to 10 μS in duration, may be entered via rear panel BNC to open the linear gate for the pre-determined time. Pulse rate not to exceed 8,000 samples per second. Normal Position: Disables internal and external auto strobe.
Linearity	Integral: Better than 0.075% of full scale. Differential: Conservatively estimated at less than 1.0% deviation from mean channel width over 99% of full scale.
Stability	Time: Less than 0.5 channel per day at stable ambient temperature. Temperature: Less than ±0.01% zero drift and less than ±0.01% gain shift per 1°C from 15 to 40°C.
Power Requirements	+24 Vdc, 115mA -24 Vdc, 115mA +12 Vdc, 840mA -12 Vdc, 15mA When +6 Vdc supply is available, 800mA is automatically switched from the +12 Vdc to +6 Vdc.
LGT Control	Continuously variable from 7 to 70 nSec (must be set such that the linear gate line (LGT) exceeds the rise time of the input event).

Table 1-6. NIM Bin and Power Supply, Physical and Functional Characteristics

Characteristic	Specification
Physical Characteristics	
Height	9.71 in
Width	19.00 in
Depth	16.00 in
Functional Characteristics	
Voltage Requirement	115/230 Vac, 50/60 Hz, single phase
Power Requirement	500W maximum
Power Output	+6 Vdc, 5A +12 Vdc, 2.5A ±24 Vdc, 1A
Regulation	±0.1% (±12 and ±24 Vdc) and ±0.5% (±6 Vdc) for 100% load change or ±10% line variation.
Temperature Drift	Less than 0.02%/°C, 0 to 50°.
Ripple and Noise	Less than 10 mV peak to peak
Voltage Adjustment	±5% nominal
Recovery Time	Less than 100 µS (±12 and ±24 Vdc) and less than 250 µS (±6 Vdc) is required to return within ±0.1% of nominal output voltage after any change in input voltage or a 10 to 100% step change (1 µS rise time) in rated load.

SECTION II.
EQUIPMENT PREPARATION

2-1. GENERAL

2-2. This section contains instructions for preparation for use, system installation and interconnections, and preliminary check-out.

2-3. PREPARATION FOR USE

2-4. UNPACKING AND INSPECTION

2-5. Carefully unpack the units which make up the ND4410 System, saving the shipping cartons for possible reshipment. Thoroughly inspect the units for damage. If damage is apparent, notify the delivering carrier about damage incurred during transit and then notify the nearest Nuclear Data sales office or the Nuclear Data home office.

NOTE

The delivering carrier must be notified within 24 hours after receipt of the units to insure reimbursement for any damages incurred during transit.

2-6. SYSTEM INSTALLATION AND INTERCONNECTIONS

2-7. Normal heat generated by the ND4410 System will not hamper its operation. However, the system should not be located over radiators or systems using vacuum tubes, since the high ambient heat may adversely affect system operation.

2-8. The ND4410 System requires a 115 or 230-volt, 50/60 Hz, ac source which is free of excessive noise or fluctuations. A voltage stabilizing transformer can be inserted between the ac source and the system where available power is subject to large fluctuations. Noise produced by various types of electrical equipment can be eliminated or greatly reduced by connecting a suitable filter between the ac source and the interfering equipment.

2-9. Using the ND4410 System Interconnection Diagram (Figure 2-1) and the following step-by-step procedure, interconnect the units that make up the ND4410 system.

a. Interconnect the Control Module to the ND812 Computer using ribbon cable equipped with card connectors on both ends as follows:

(1) Insert card connector into location 111 on Control Module.

(2) Insert card connector on other end of ribbon cable into either of the two input/output printed circuit board connectors located on the rear of the ND812 Computer.

b. Interconnect the Control Module to the ADC Module using ribbon cable equipped with a card connector on one end and a 50-pin male connector on the other end as follows:

(1) Insert card connector into location 112 on Control Module.

(2) Insert 50-pin male connector on other end of ribbon cable into 50-pin female connector designated 50F on the ADC module.

NOTE

The card connectors referred to in steps (a) and (b) above are slotted to prevent inserting them the wrong way.

c. Interconnect the Control Module to the 602 Oscilloscope as follows using three 75Ω coaxial cables with BNC connectors on both ends:

(1) From the HORIZ BNC Connector (upper) on control module rear panel to the X input on the 602 oscilloscope.

(2) From the VERT BNC Connector (upper) on the Control Module rear panel to the Y input on the 602 oscilloscope.

(3) From the BLANK BNC Connector (upper) on the Control Module rear panel to the Z input on the 602 oscilloscope.

d. Connect ac line cords from the 602 Oscilloscope, Bin Power Supply, and ND812 Central Processor, to the Power Junction Box.

e. Connect ac line cord from the Power Junction Box to a nearby 115 volt ac source.

NOTE

Step f applies to ND4410 systems equipped with an optional X-Y plotter.

f. Connect the X-Y HP-7004B Plotter to the Control Module as follows:

(1) Plug BNC/dual banana adapters into X and Y inputs on the HP-7004B front panel. Ground negative side of each input with ground strap.

(2) Connect 75-ohm coaxial cable (with BNC connectors on both ends) from X input on HP-7004B front panel to the HORIZ BNC connector (lower) on rear of Control Module.

(3) Connect 75-ohm coaxial cable (with BNC connectors on both ends) from Y input on HP-7004B front panel to VERT BNC connector (lower) on rear of Control Module.

(4) Connect cable with 9-pin female connector on one end and blue and yellow banana jacks on other end as follows:

a. Plug blue and yellow banana jacks into blue (COMPLETE) and yellow (SEEK) receptacles respectively, on the Control Module rear panel.

b. Connect 9-pin female connector into 9-pin male receptacle of HP-17173 Null Detector Plug-in on bottom of the HP-7004B.

NOTE

Step g applies to ND4410 systems equipped with optional TC33ASR Teletype.

g. Connect the TC33ASR Teletype into the ND812 Computer as follows:

(1) Plug male integrated circuit connector (on grey ribbon cable) into female integrated receptacle (rear row, second from left) on ALT printed circuit board of the ND812 Computer.

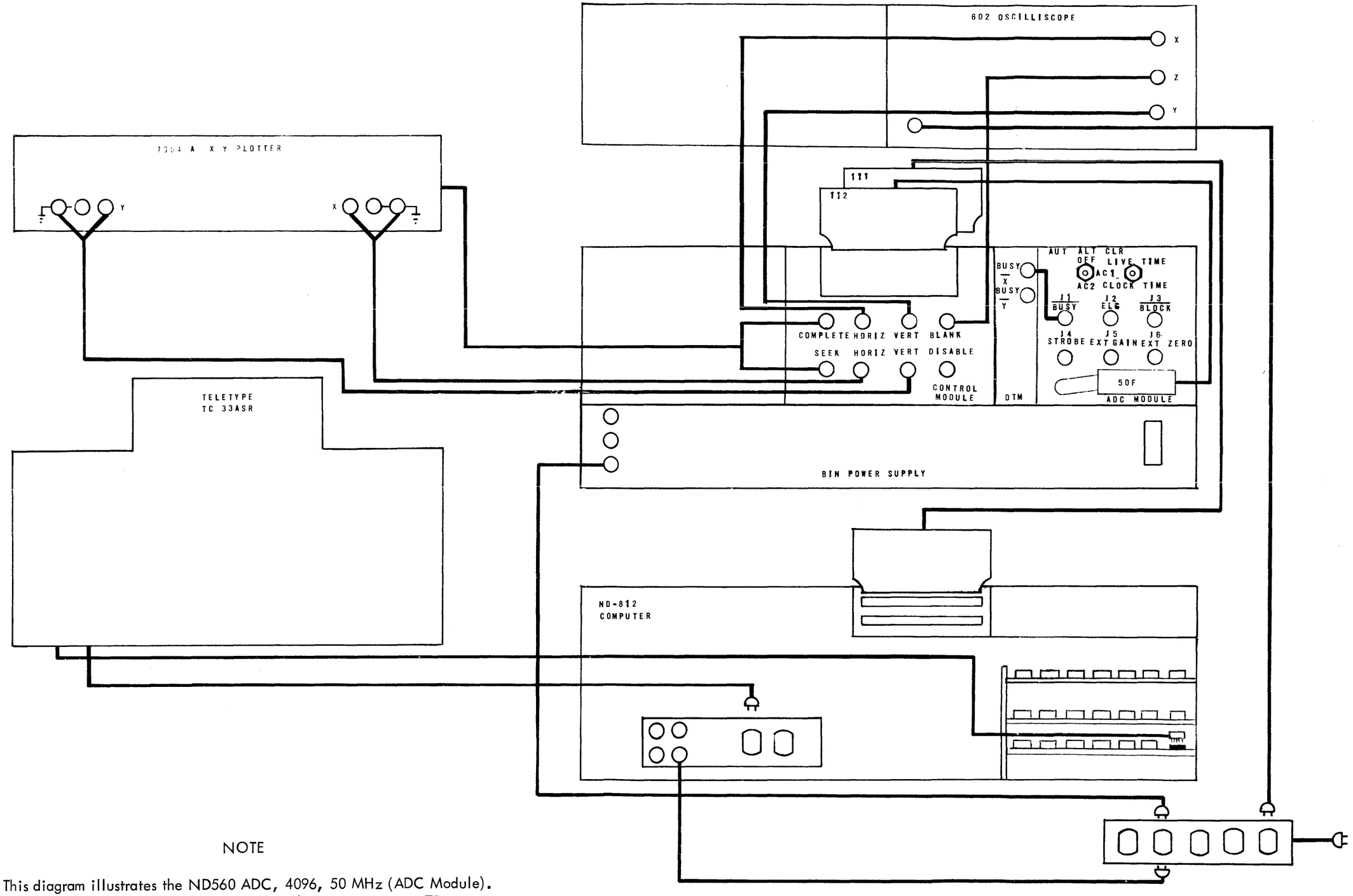
(2) Connect ac line cord from TC33ASR to one of two ac receptacles on the ND812 Computer.

2-10. PRELIMINARY CHECK-OUT

2-11. The following procedures provide step-by-step instructions to ensure the ND4410 System is ready for normal operation. These procedures should be performed as a matter of routine before operating the ND4410 System. Set front panel switches and controls as follows:

a. Analog to Digital Converter Module

(1) Front Panel



NOTE

This diagram illustrates the ND560 ADC, 4096, 50 MHz (ADC Module). If the ND 565 TM Dead Time Monitor (DTM) is used, connect 75Ω coaxial cable (with BNC connectors on both ends) from the J1 $\overline{\text{BUSY}}$ BNC on the ADC Module to the DTM BUSY $\overline{\text{X}}$ BNC on the DTM.

Figure 2-1. Series 4410 System Interconnection Diagram

Switch/Control	Initial Position
CONVERSION GAIN Switch	Equivalent to memory group size selected at external analyzer.
GROUP Switch	Equivalent to memory group size selected at external analyzer.
ULD Control	Fully clockwise (10.0)
LLD Control	Fully counter clockwise (0.0)
ZERO Trim Potentiometer	Fully counter clockwise
FINE ZERO Control	Fully counter clockwise (0.0)
ZERO SUPPRESSION Switches	All zero (0)
STROBE ON/STROBE OFF Switch	STROBE ON
DC/AC Switch	AC
COIN/NORM/ANTI Switch	NORM

(2) Rear panel

Switch/Control	Initial Position
AUT ALT CLR Switch	As desired
LGT Control	Set at a time greater than the rise time of the input event.
LIVE TIME/CLOCK TIME	As desired

b. ND812 Computer

Switch/Control	Initial Position
POWER OFF/POWER ON/ CONTROL OFF Switch	POWER ON
SINGLE STEP Switch	Down
SINGLE INSTR Switch	Down
SWITCH REGISTER Switches (0-11)	All Down
MEMORY FIELD Switches (0, 1)	Both Down
SELECT REGISTER Switch	EXTERNAL

c. Control Module

Switch/Control	Initial Position
Direction (⟷) Switch	Left (⟵)

d. 602 Oscilloscope

Switch/Control	Initial Position
ON Switch	Down
INTENSITY Control	Maximum Counterclockwise
FOCUS Control	Mid range
VERT POSITION Control	Mid range
HORIZ POSITION Control	Mid range
SCALE ILLUM	Maximum Counterclockwise

e. Bin Power Supply

Switch/Control	Initial Position
Power Switch	Down

f. Teletype ASR33

Switch/Control	Initial Position
LINE/OFF/LOCAL Switch	LINE
START/STOP/FREE Switch	FREE

2-12. INITIAL START-UP PROCEDURE

2-13. After all controls have been initially set, load the programs into the ND812 Computer in accordance with the procedures given in the ND4410 Single Parameter Data Acquisition and Display System Software Instruction Manual. After the programs have been loaded, start the ND4410 system as follows:

a. Place the POWER Switch on the Bin Power Supply in the "up" position. Power indicator lamp shall light.

b. Place the ON switch on the 602 Oscilloscope in the "up" position. Adjust INTENSITY control until a dot is visible on oscilloscope screen.

NOTE

If HP-1208B oscilloscope is used, refer to note on Figure 7-2, sheet 5 of 11 for proper blanking circuit hookup.

c. Turn the LINE/OFF/LOCAL Switch on the Teletype to the LINE position.

d. Set the SWITCH REGISTER Switches on the ND812 Computer to 0200_8.

e. Depress the STOP Key on the ND812 Computer.

f. Depress the LOAD AR Key on the ND812 Computer.

g. Depress the START Key on the ND812 Computer. The teletype should now perform a carriage return and line feed and type an asterisk (*). The system is now in operation.

h. Depress ACQUIRE pushbutton switch on Control Module. ACQ lamp shall light.

i. Adjust FINE ZERO control until storage is observed in channel zero.

j. Set STROBE ON/STROBE OFF switch to STROBE OFF.

k. Apply an appropriate signal to the front panel SIGNAL INPUT BNC.

l. Adjust the LLD control clockwise until storage of a spectrum is observed. The ADC is now operational and properly zeroed.

SECTION III.
OPERATING INSTRUCTIONS

3-1. GENERAL

3-2. Most of the actual operating instructions are governed by the specific program applications as defined by the various ND4410 System Software Manuals. However, in the following pages, certain manual operations which will facilitate experiment set-up will be discussed along with an example experiment. In addition, the 4410 Instruction Repertoire will be explained. This instruction repertoire, in conjunction with the "Principles of Programming the ND812 Computer", should provide an excellent guide for understanding the ND4410 Software.

3-3. CONTROL AND INDICATOR FUNCTION

3-4. The ND4410 control module provides the primary controls necessary for operation of the ND4410 system. The controls and indicators for the control module are illustrated in Figure 3-1. Table 3-1 lists the controls and indicators, and describes their functions. Refer to the appropriate instruction manual for controls and indicators information on all other system units and peripheral options.

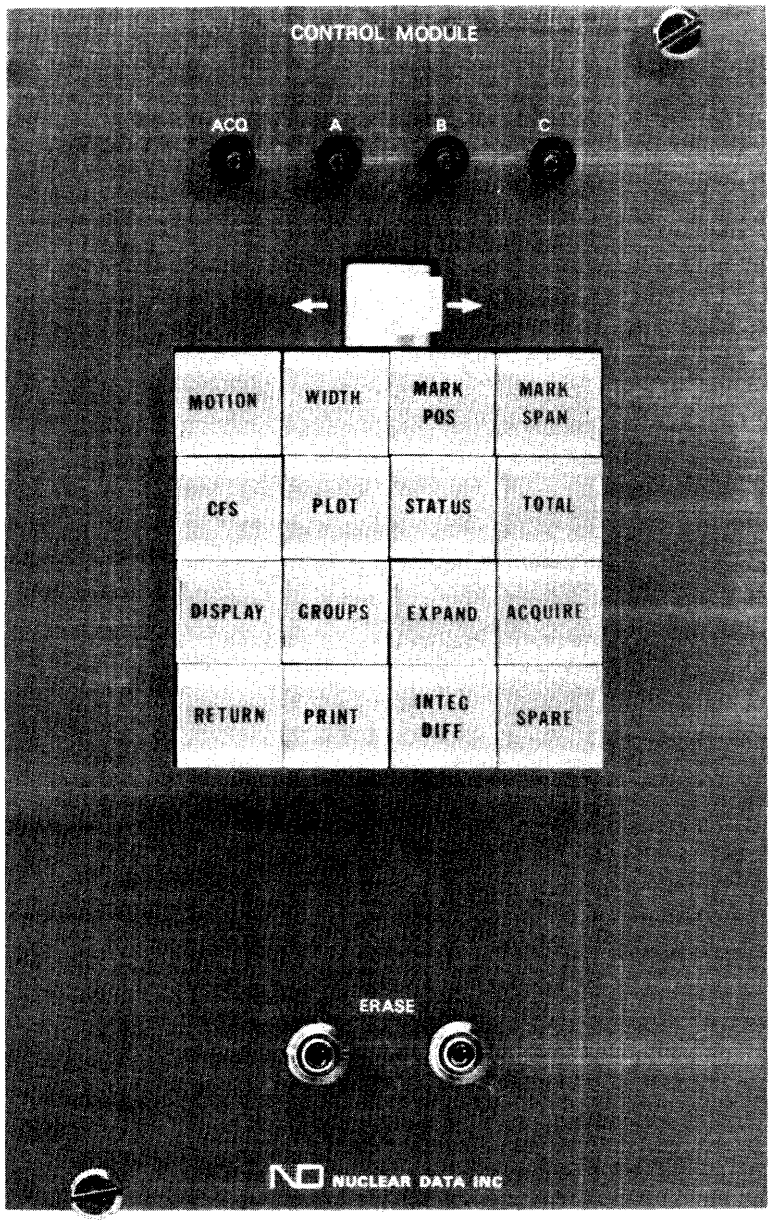


Figure 3-1. Control Module Front Panel Controls and Indicators

Table 3-1. Control Module, Function of Controls and Indicators

Control/Indicator	Description	Function
ACQ	Indicator lamp	Illuminates when the ND4410 System is in an Acquisition Mode.
A, B, C	Indicator lamps	illuminate when the ND4410 System is in the program selected A, B or C mode of operation.
Direction Switch ⟵ ⟶	Toggle switch	Determines the direction in which the display limit, marker, or group will move when the selected pushbutton is depressed.
MOTION Pushbutton	Pushbutton Switch S1	Holding the MOTION Pushbutton depressed causes the display to move horizontally in the direction selected by the setting of the Direction (⟷) Switch. The rate of movement is a function of the length of time the MOTION pushbutton is held depressed. A momentary switch depression will move the display one channel. Depressing the GROUPS pushbutton returns the display to the initial position.
WIDTH Pushbutton	Pushbutton Switch S2	Holding the WIDTH pushbutton depressed horizontally contracts the display when the Direction Switch is in the Left (⟵) position, or horizontally expands when the Direction Switch in the Right (⟶) position. Horizontal expansion increases the spacing between channels, causing the number of channels displayed to decrease, while horizontal contraction decreases the spacing between channels, causing the number of channels displayed to increase. The rate of expansion or contraction

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
		is a function of the length of time the WIDTH pushbutton is depressed. A momentary depression will only expand or contract the display by one channel.
MARK POS Pushbutton	Pushbutton Switch S3	Holding the MARK POS Pushbutton depressed, causes the left and right markers (full scale vertical lines imposed upon the spectrum) to move in the direction specified by the Direction (⟷) Switch. The rate of movement is a function of the length of time the MARK POS Pushbutton is held depressed. A momentary depression will move the markers one channel.
MARK SPAN Pushbutton	Pushbutton Switch S4	Holding the MARK SPAN pushbutton depressed, causes the right marker (a full scale vertical line imposed upon the spectrum) to move in the direction specified by the Direction (⟷) Switch increasing or decreasing the number of channels between the markers. The rate of movement is a function of the length of time the MARK SPAN pushbutton is held depressed. A momentary depression will only move the right marker one channel.

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
CFS Pushbutton	Pushbutton Switch S5	Depressing the CFS pushbutton increases the counts full scale value by a factor of two when the Direction Switch is in the Left (⟵) position or decreases the counts full scale value by a factor of two when the Direction Switch is in the Right (⟶) position. Each time the CFS pushbutton is depressed, the counts full scale value will be increased or decreased by a factor of two until it becomes zero. The range of counts full scale values is from 1 to $2^{24}-1$ in binary increments. Logarithmic display is selected by depressing the CFS pushbutton after the minimum counts full scale value (1) is reached with the Direction Switch in the Right (⟶) position or after the maximum counts full scale value ($2^{24}-1$) is reached with the Direction Switch in the Left (⟵) position. Display of the counts full scale value when selected by the STATUS pushbutton will appear as follows: Ø, 1, 2, . . . 8388607, -1, Ø. The counts full scale value displayed for $2^{24}-1$ is -1. The counts full scale value displayed for logarithmic display is zero (Ø).

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
PLOT Pushbutton	Pushbutton Switch S6	Depressing the PLOT pushbutton plots the current display (including the current STATUS selected display parameters and the content of the channels in the current group) at the X-Y Plotter. The X-Y plot operation can be terminated at any time by depressing the RETURN pushbutton. An asterisk (*) is typed at the teletype to indicate initiation and termination of the X-Y plot operation. NOTE Calibration of the X-Y plotter is described in Section IV of the ND4410 system software manual under OPERATIONAL PROCEDURE. When an X-Y plotter is not used, depressing the PLOT pushbutton causes an asterisk (*) to be typed.
STATUS Pushbutton	Pushbutton Switch S7	Depressing the STATUS pushbutton sequentially displays the following parameters: (1) Center pointer channel/content, and left marker channel-right marker channel, with the channels relative to the currently displayed group; (2) current group number/total groups, current group width, and counts full

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
		scale; (3) Elapsed time, and preset analysis time; or (4) Off (no parameters displayed). After the last parameter, display reverts back to the first parameter.
TOTAL Pushbutton	Pushbutton Switch S8	Depressing the TOTAL pushbutton prints the current group number, the channel locations of the left and right markers, the elapsed analysis time, totalizes the counts stored in the channels between the left and right markers, subtracts the background from the total and then prints the total and the net total (total minus background).
DISPLAY Pushbutton	Pushbutton Switch S9	Depressing the DISPLAY pushbutton alternately selects live or static display. Static display presents the data to the display oscilloscope continually while live display presents the data to the display oscilloscope only when the corresponding channel has been addressed by the ADC.
GROUPS Pushbutton	Pushbutton Switch S10	Depressing the GROUPS pushbutton sequentially selects the groups for data storage and display. The direction of selection is determined by the Direction (⟷) Switch. In the Left (⟵) position, the next lower group is selected.

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
		After the first group, selection reverts to the last group. In the Right (→) position, the next higher group is selected. After the last group, selection reverts back to the first group. Display of the current group, total groups and current group width can be selected using the STATUS pushbutton.
EXPAND Pushbutton	Pushbutton Switch S11	Depressing the EXPAND pushbutton expands the display between the left and right markers to full scale. The display can be returned to normal by depressing the GROUPS Pushbutton.
ACQUIRE Pushbutton	Pushbutton Switch S12	Depressing the ACQUIRE pushbutton alternately starts or stops data acquisition. Data acquisition stops automatically after the preset analysis time. The preset analysis time is entered using the Clock Set Command. NOTE Since data storage occurs in the group currently displayed at the start of analysis, the GROUPS Pushbutton should be used to select the desired storage group prior to starting analysis.

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
		The preset and elapsed acquisition time can be displayed using the STATUS pushbutton.
RETURN Pushbutton	Pushbutton Switch S13	Depressing the RETURN pushbutton terminates the routine in progress and returns the program to display.
PRINT Pushbutton	Pushbutton Switch S14	Depressing the PRINT pushbutton prints the current group number, the channel locations of the left and right markers, the elapsed analysis time in centiseconds (0.01 second), and the content of the channels between the markers with channel identification every eighth channel.
INTEG DIFF Pushbutton	Pushbutton Switch S15	Depressing the INTEG/DIFF pushbutton with the Direction Switch in the Right (→) position selects integration of the area defined by the left and right markers in the

Table 3-1. Control Module, Function of Controls and Indicators (Cont'd)

Control/Indicator	Description	Function
		currently displayed group with storage of the integral in the marker defined area. Depressing the INTEG/DIFF pushbutton with the Direction Switch in the Left (←) position selects differentiation of the area defined by the left and right markers in the currently displayed group with storage of the differential in the defined area.
SPARE Pushbutton	Pushbutton Switch S16	Available for future software operation.

3-5. OPERATIONAL CONSIDERATIONS

3-6. SPECIFIC HARDWARE CONSIDERATIONS

3-7. ANALOG TO DIGITAL CONVERTER MODULE. The storage capacity of the analyzer memory being used is an important consideration in the selection of the conversion gain. The number of address advance pulses for a full scale (8 volt) input signal corresponds to the conversion gain switch positions of 128, 256, 512, 1024, 2048, and 4096. Therefore, it would seem feasible to select the switch position corresponding to the memory size, i.e., for a 1024 channel memory, select switch setting of 1024; for a 2048 channel memory, select a switch setting of 2048; etc. In many experiments the above holds true, but in others, different factors require different settings. For example, if the energy of interest does not exceed 5 volts, it may be better to select a conversion gain of 1024 with a 2048 channel memory size. This allows the spectrum peaks to spread out over the full memory rather than half the memory.

3-8. Another factor to consider is resolution. With the conversion gain switch set at 1024, each channel represents 8 millivolts (horizontally on the display oscilloscope) for a full scale 8 volt input. This means the voltage levels can be resolved to within 8 millivolts of each other. The conversion gain is directly proportional to the resolution. Therefore, if the experiment requires high resolution, a higher conversion gain might be more advantageous.

3-9. Speed is another factor. The analysis time required for a full scale input with the conversion gain switch set at 1024 is twice as long as it would be with the switch set at 512. Therefore, a lower conversion gain may be desirable where speed is more important

than resolution. However, since the average analysis time rather than the maximum is usually used in evaluating the selection of proper conversion gain, the percentage of increase in speed is considerably less, and the loss in resolution may be enough to offset the advantages of increased speed. Therefore, the tradeoffs among these factors must be determined in evaluating the experiment to be performed, and then the selection of the proper conversion gain may be made.

3-10. In some experiments, intense noise or low energy radiation may be present. To reduce the effect of dead time, which is a result of noise analysis, the lower level discriminator control must be adjusted above the level of the noise. The lower level discriminator control provides a bias at the input of the ADC to reject any signal below the bias level. When a signal exceeds the bias level, the bias is removed. Therefore, signals which exceed the bias level are passed for analysis in their entirety.

3-11. When the analyzer is preoccupied with useless analysis of noise, most of the noise will fall at channel zero. However, since channel zero is reserved for storing of clock pulses, it is not always evident that the ADC is preoccupied with noise analysis.

3-12. A percent dead time meter, which can be connected to the rear panel Busy BNC, is a useful tool in determining whether or not the ADC is preoccupied with useless analysis of noise. This allows the user to determine whether or not the setting of the Lower Level Discriminator Control affects the indicated percent dead time.

3-13. When there is no appreciable noise mixed with the input signal, a minimum Lower Level Discriminator control setting of 0.3 is usually appropriate. For highest linearity in the lower energy regions, the control should be set at the minimum value. However, if there is an apparent increase in noise, which may be caused by increasing the amplifier gain, the minimum setting should be increased accordingly.

3-14. The upper level discriminator control setting selects the triggering level of the upper level discriminator circuit. Input pulses which exceed the bias setting imposed by this control will cause the linear gate of the ADC to close, prohibiting the analysis of the input pulse. For most experiments, this control is set at maximum (10.0), but can be set as desired depending upon experiment requirements.

3-15. When the Zero Suppression Switches are not used, the Analog Zero Control is used primarily for precise adjustment of energy zero to correspond to the lower boundary of channel zero. Alteration of the Conversion Gain Switch changes the energy zero position. It is recommended that the Analog Zero Control be properly set to locate the zero energy intercept for each of the six conversion gains in order to facilitate later experimental set-up operations. A calibration performance check once a month will probably be adequate for most applications. However, this must be determined by experience.

3-16. CONTROL MODULE. Primary control of all analyzer functions is provided by the pushbuttons on the Control Module. These include: acquisition, display and data manipulation, teletype print out, and data erasure.

3-17. Initiation and termination of any of the three acquisition modes is controlled by the ACQUIRE Pushbutton. Group selection for data storage and display is controlled by the GROUPS Pushbutton. Display manipulation is provided by the MOTION WIDTH, MARK POS, MARK SPAN Pushbuttons in conjunction with the Direction (⟷) Switch. Selection of live or static display is provided by the DISPLAY Pushbutton. Expansion of the marker defined area is provided by the EXPAND Pushbutton. Oscilloscope display of the various parameters is controlled by the STATUS Pushbutton. Data manipulation of the marker defined area is provided by the TOTAL, INTEG and DIFF Pushbuttons. Teletype print out of the counts stored in the channels between the markers is provided by the PRINT Pushbutton. Erasure of data stored in any group is provided by the ERASE Pushbuttons. Termination of any of the operations with return to display is provided by the RETURN Pushbutton.

3-18. OSCILLOSCOPE CALIBRATION. The following procedure is intended to assist the experimenter in calibrating the display oscilloscope. Although this method is arbitrary, it has been found useful in analyzing the data displayed.

a. Set controls on display oscilloscope as follows:

(1) Rotate the INTENSITY Control slowly clockwise until the display is visible.

CAUTION

If the INTENSITY Control is set too high, damage to the CRT phosphor may result.

(2) Adjust the FOCUS Control for a well-defined trace.

b. Set controls on the control module as follows:

(1) Depress DISPLAY Pushbutton and erase the group currently displayed by depressing both ERASE pushbuttons. The horizontal trace on the oscilloscope screen represents full scale horizontal deflection.

(2) Place the Direction Switch in the Left (⟵) position.

(3) Depress and hold the MARK POS Pushbutton until the left marker (a full scale vertical line on the left side of the display) reaches the extreme left of the oscilloscope screen and ceases to move.

(4) Place the Direction Switch in the Right (⟶) position.

(5) Depress and hold the MARK SPAN Pushbutton until the right marker (a full scale vertical line on the right side of the display) reaches the extreme right of the oscilloscope screen and ceases to move.

c. Set controls on the display oscilloscope as follows:

(1) Adjust the HORIZ POSITION Control so that the left marker coincides with the grid line on the left side of the oscilloscope screen.

(2) Adjust the VERT POSITION Control so that the horizontal trace coincides with the grid line at the bottom of the oscilloscope screen.

NOTE

The oscilloscope is now calibrated for 125 millivolts per horizontal and vertical divisions.

3-19. PULSE HEIGHT ANALYSIS EXPERIMENT. The following is a procedure for a sample experiment in Pulse Height Analysis involving spectrum storage and energy calibration. The experiment conditions are: energy calibration of 1 Kev/channel desired; Cesium 137 to be used as the calibration source; memory capacity to be 1024 channels.

a. Connect the source, detector, preamp, and ADC as shown in Figure 3-2. Connect the oscilloscope, ND812 computer, Power supply, and Teletype as shown in Figure 2-1.

b. Erase the group current displayed by depressing the Control Module ERASE pushbuttons.

c. Depress the STATUS Pushbutton until the center marker channel and the number of counts stored in that channel are displayed on the oscilloscope.

d. Place the Direction Switch in the Left (⟵) position.

e. Depress and hold the MARK SPAN pushbutton until the right marker reaches channel 646.

f. Place the Direction Switch in the Right (⟶) position.

g. Depress and hold the MARK POS pushbutton until the Left marker reaches channel 33 (0.32 Mev Cesium peak). The right marker should now be at channel 678 (0.662 Mev Cesium peak).

h. Depress the ACQUIRE Pushbutton. Accumulation of data in the memory can be observed on the oscilloscope. Allow data acquisition to continue until the 0.032 Mev and 0.662 Mev Cesium photopeaks are clearly visible (do not stop data acquisition).

i. Set preamp COARSE GAIN control in position 4, and adjust the FINE GAIN Control so that the 0.622 Mev Cesium photopeak coincides with the right marker, and the .032 Mev Cesium peak coincides with the left marker.

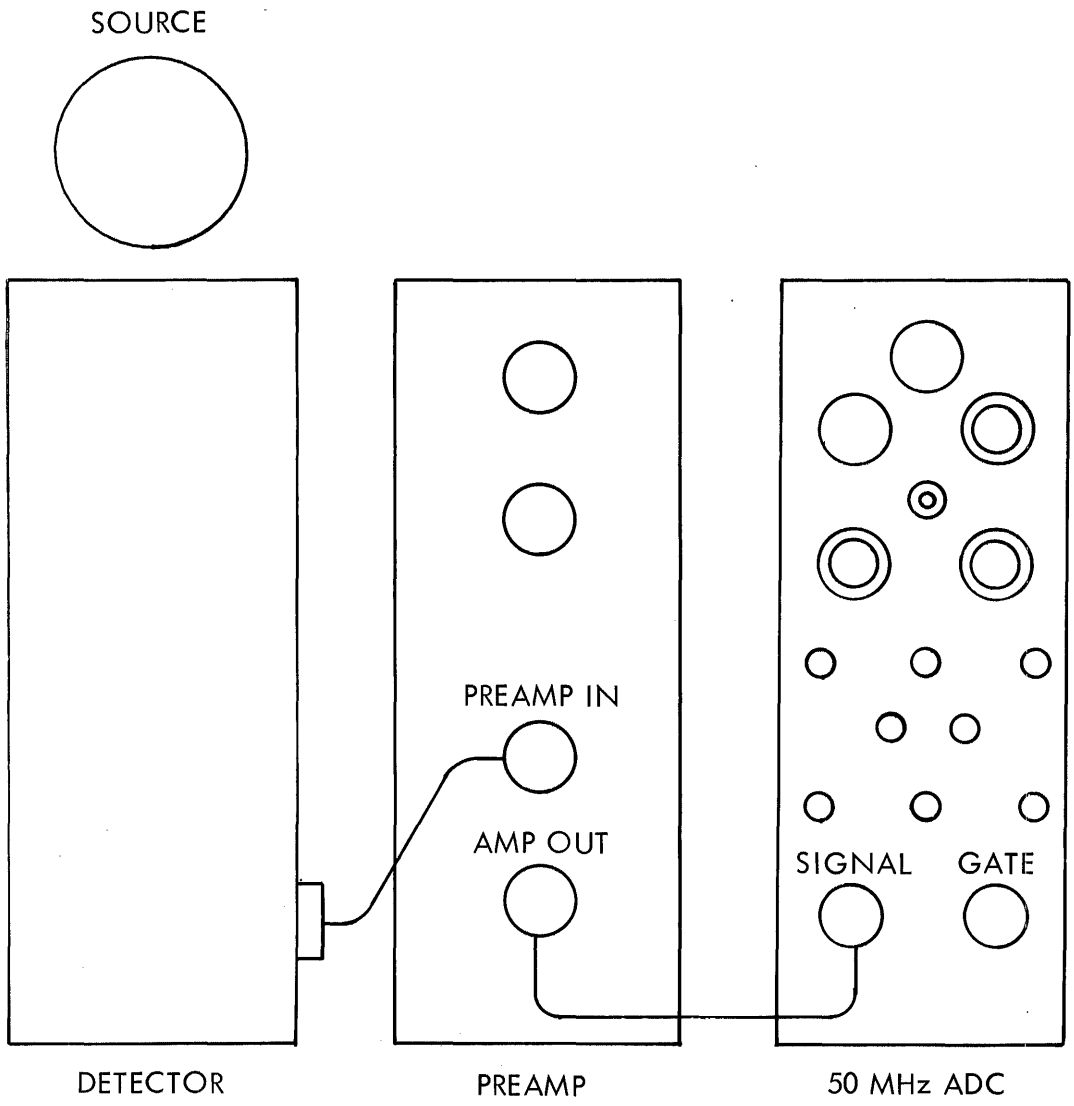


Figure 3-2. Typical System Set-Up for Pulse Height Analysis Experiment

j. Erase the Memory by depressing the two ERASE Pushbuttons. Again allow sufficient data accumulation so that the 0.032 Mev and 0.662 photopeaks are clearly visible.

k. Repeat steps i and j until satisfactory energy calibration is achieved.

l. After satisfactory energy calibration is achieved, depress the ACQUIRE Pushbuttons and record the setting of the ZERO COARSE and FINE Controls for future reference. The settings represents 1 Kev/channel energy calibration for a CONVERSION GAIN setting of 1024.

NOTE

Since alternation of the CONVERSION GAIN Switch changes the energy zero position, it is recommended that the proper setting of the ZERO COARSE and FINE Controls be determined for each of the CONVERSION GAIN Switch settings in order to facilitate later experimental set-up operations. A similar procedure to that described above can be followed for the other CONVERSION GAIN Settings.

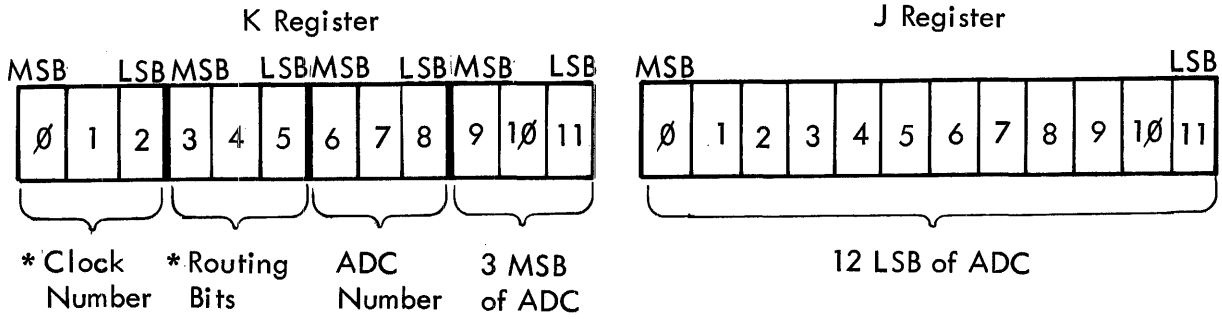
3-20. SPECIFIC SOFTWARE CONSIDERATIONS

3-21. ND4410 INSTRUCTION REPERTOIRE. The following ND4410 instruction repertoire is an extension of the basic ND812 I/O instructions. Refer to "Principles of Programming the ND812 Computer" for explanation of the ND812 I/O instructions.

a. Read ADC to JK accumulators

Octal Code

7524	Load K
7522	Load J
7521	Clear Device

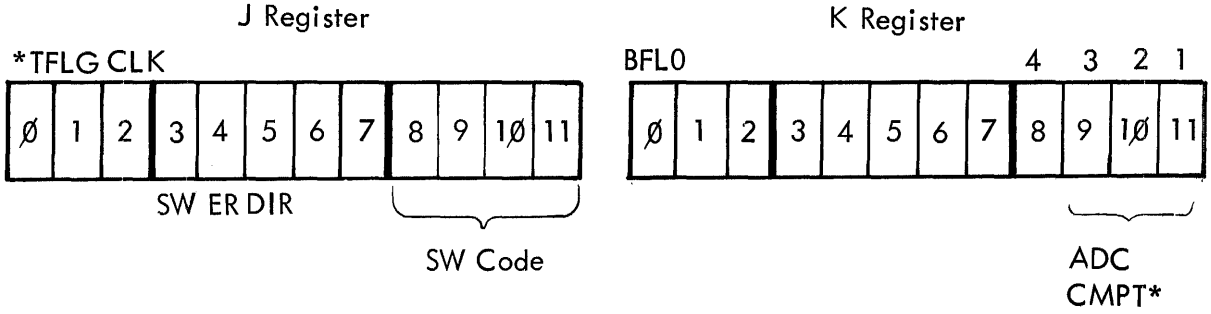


ADC operates on Interrupt facility and traps to $\emptyset 1\emptyset 1_8$ and stores the contents of the program counter. There is no skip flag.

b. Read 4410 Control Status to JK accumulators.

Octal Code

0740	0604	Load K
0740	0602	Load J



*Assigned but not currently used.

J Register Bit Assignment

Bit Ø	Unassigned
1	T flag. "1" = CTA time out
2	Real time clock. "1" occurs at 10 ms intervals
3	Switch. "1" when any of 16 controls or erase pushbutton engaged
4	Erase. "1" when erase pushbuttons are engaged
5	Direction. "1" when switch is in the left position
6,7	Unassigned, reserved for expanded switch field
8,9,10 & 11	Binary code for one of 16 control pushbutton switches: 8 is MSB. 11 is LSB.

K Register Bit Assignment

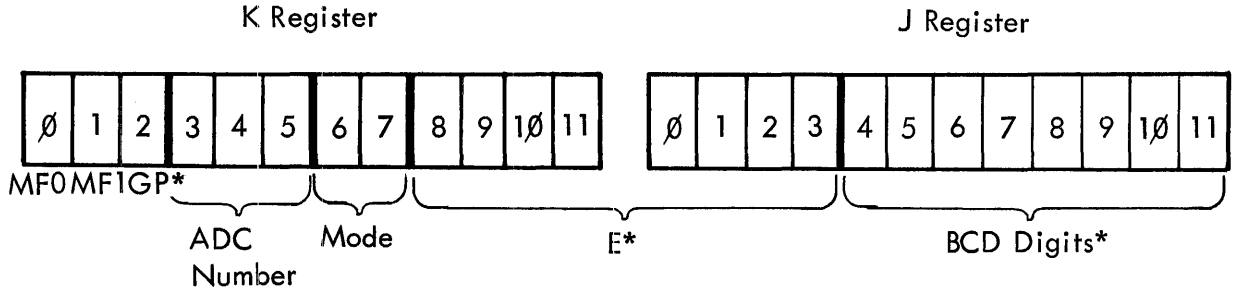
Bit Ø	Buffer overflow. "1" when list mode address counter overflows
1	Unassigned.

2 thru 7	Unassigned
8,9,10 & 11	Binary code for CTA time out. 8 is MSB. 11 is LSB.

c. Set acquire mode in 4410 control

Octal Code

0740	2024	Transfer K to 4410 Control
0740	2022	Transfer J to 4410 Control



*Assigned but not currently used.

K Register bit assignment

Bit Ø & 1	Memory field bits for storage and display
2	Hardware storage routing bit
3,4,& 5	Device address for enabling acquisition. 3 is MSB, 5 is LSB.
6,7	Mode bits 00 off state 01 accumulator 10 DMA Increment 11 List
8 thru 11	4 MSB's of term E for initializing CTA timer

J Register bit assignment

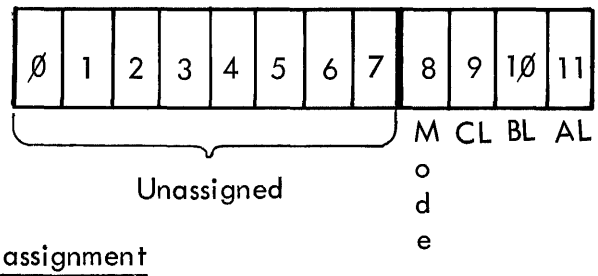
Bits Ø thru 3	4 LSB of E term for initializing CTA timer
4 thru 11	2 BCD digits for initializing CTA timer

d. Set mode lamps and clear

Octal Code

0740	0614	Load lamp and P.B. switch mode register
0740	0612	Clear real time clock interrupt
0740	0611	Clear switch interrupt

J Register



J Register bit assignment

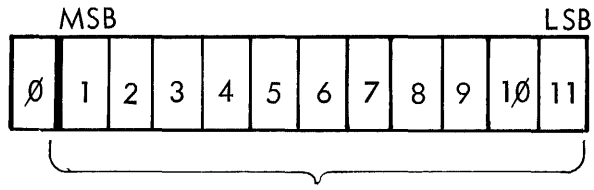
Bits Ø thru 7	Unassigned
8	"1" will allow upper 4 pushbuttons of 16 key array to operate One push allows one interrupt to ND812 Central Processor. "0" will allow upper 4 pushbuttons of 16 key array to operate. One push will allow multiple interrupts to ND812 Central Processor at rate not to exceed 50 interrupts per second.
Bit 9	"0" will light C mode lamp on front panel. "1" will extinguish C mode lamp on front panel.
10	"0" will light B mode lamp on front panel "1" will extinguish B mode lamp on front panel
11	"0" will light A mode lamp on front panel "1" will extinguish A mode lamp on front panel

e. Set List Mode Register

Octal Code

0740	0632	Load list register from J accumulator

J Register



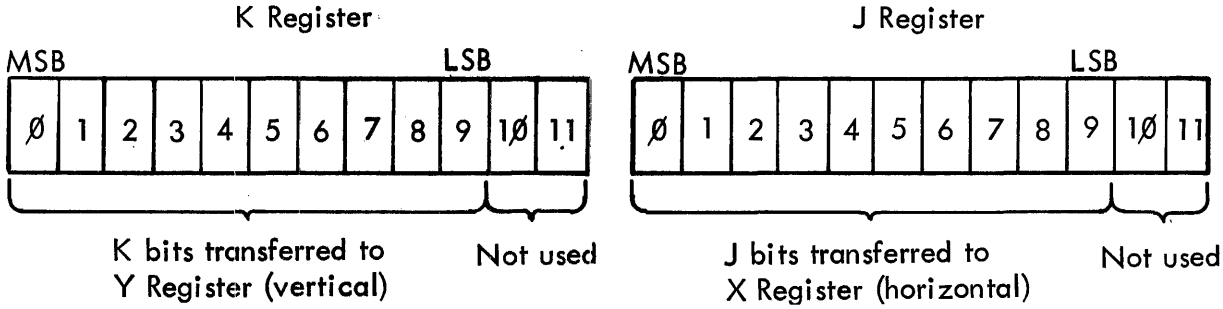
J Register bit assignment

Ø	Unassigned
1 thru 11	Bit 1 is MSB. Bit 11 is LSB. Each list event occupies two core locations. Example: If J = $ØØ77_8$ then the list will start at location $4096_{10} - 128_{10} = 3966_{10}$ in an ND812 4K field. When list area is filled an interrupt will occur and the BFR bit will be "1" when the read control status is issued.

f. Set Display Register and Plot

Octal Code

7514	Will skip if both plotter and marker are ready
7504	Will load Y from K accumulator
7502	Will load X from J accumulator
7501	Will generate a vertical mark
7500	Will dim scope
7511	Will plot last point loaded in XY display registers.



K Register bit assignment

Bit Ø	"1" produces 1/2 scale vertical deflection. Is MSB
Bits 1 thru 9	"1" produce 1/2 vertical deflection of the bits of higher order.

J Register bit assignment

Bits Ø thru 9	"1" produces 1/2 horizontal deflection. Is MSB "1" produces 1/2 horizontal deflection of the bits of higher order.

SECTION IV.
FUNCTIONAL DESCRIPTION

4-1. GENERAL

4-2. This section contains theory of operation for the ND4410 system. Theory of operation is presented as a general functional description and a detailed functional description.

4-3. GENERAL FUNCTIONAL DESCRIPTION

4-4. The 4410 Control Module is contained in a standard 4-wide Nuclear Instrumentation Module (NIM). All functions are generated either by software commands or by front panel pushbuttons. These decoded functions control the following events: data acquisition in one of three modes - Program Control, Buffer or List, or Direct Memory Increment; data display on the ancillary oscilloscope or X-Y plotter; interrupt enable or disable of the interrupt lines to the ND812 Central Processor; and print-out of group and/or channel information. This section provides a general functional description of the major circuits followed by a more detailed analysis. Signal names followed by an asterisk (*) signify the inversion of that signal (Figure 4-1).

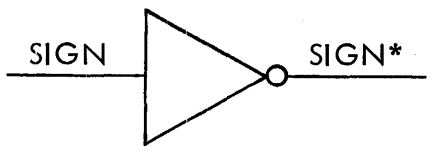


Figure 4-1. Signal Inversion

4-5. FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

4-6. Refer to Figure 4-2 for the ND4410 Control Module functional block diagram.

4-7. COMMAND DECODERS. The command decoders accept the Input/Output commands from the ND812 Central Processor and decodes them into control and timing signals. These signals in turn are propagated throughout the Control Module.

4-8. ADC DECODER. The ADC decoders select the ADC to be enabled for acquisition. They accept a three bit combination from the K accumulator in the ND812 Central Processor and produce signals ON1* thru ON4*. In this system, only signal ON1* is used.

4-9. MEMORY FIELD AND ACQUISITION MODE REGISTER. The memory field and acquisition mode registers decode the memory field to determine which field data will be stored, and which acquisition mode will be selected. The three modes of acquisition are Program Control, Buffer or List, or Direct Memory Increment. The OFF mode is the absence of the other three.

4-10. ADC CONTROL CIRCUITS. The ADC control circuits indicate when the ADC is in the ready state. They also provide control for transfer of data from the ADC.

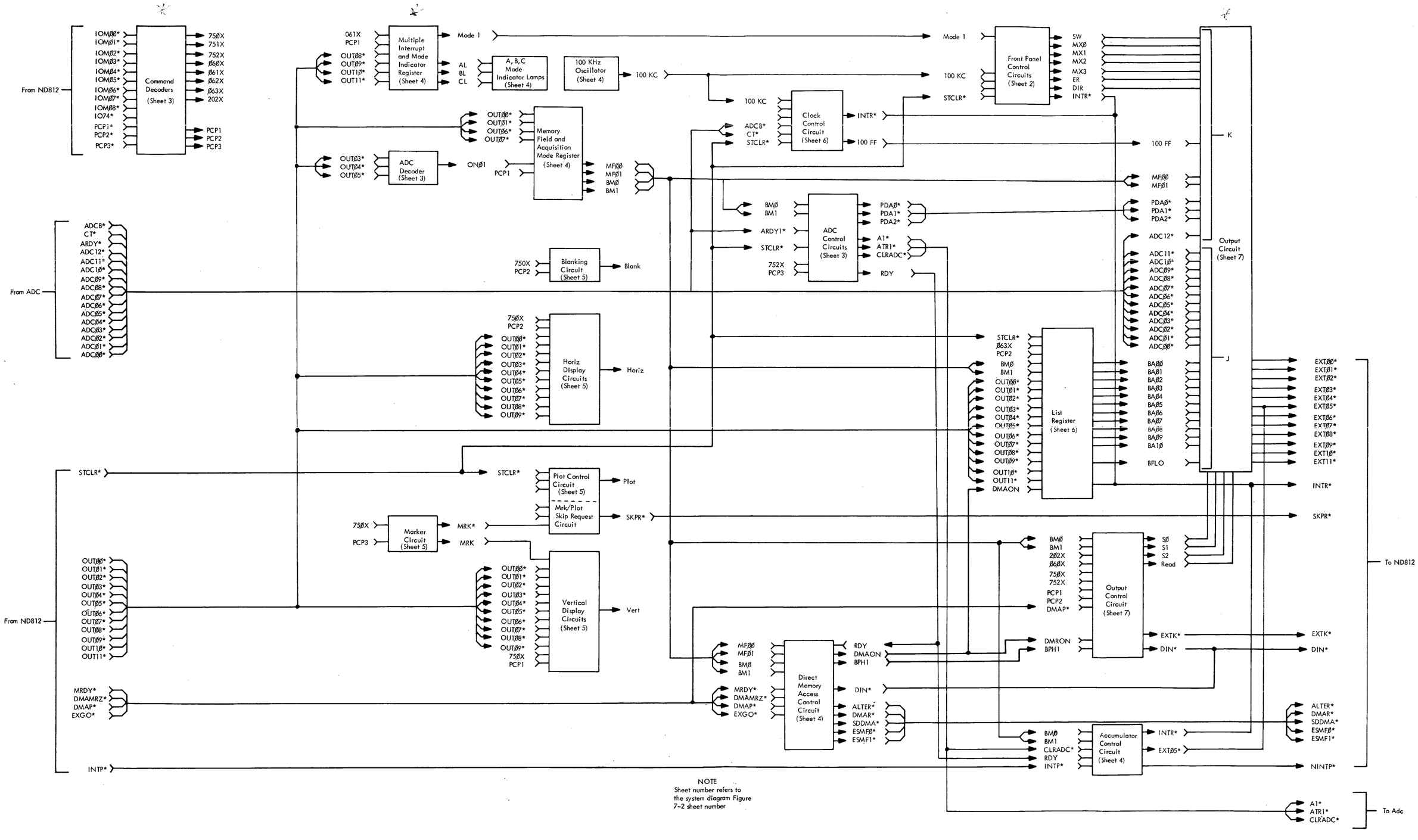
4-11. CLOCK CONTROL CIRCUIT. The clock control circuit provides the timing for data acquisition, and interrupts the ND812 Central Processor when acquisition is complete. The clock control circuit operates in either gated (live time) or ungated (clock time) mode.

4-12. MULTIPLE INTERRUPT AND MODE INDICATOR REGISTER. The multiple interrupt and mode indicator register decodes the program selected interrupt and indicator modes received from the J accumulator of the ND812 Central Processor. The multiple interrupt signal, Mode 1, goes to the Front Panel Control Circuits and the selected mode indicator signal will illuminate one of the three mode indicator lamps A, B, or C.

4-13. FRONT PANEL CONTROL CIRCUITS. The front panel control circuits decode the front panel pushbutton controls to select the software program stored in the ND812 Central Processor for specific assigned operation. These selected outputs go to the K accumulator of the ND812 Central Processor. The INTR* output interrupts the ND812 Central Processor.

4-14. LIST REGISTER. The list register contains the address of the list during the List Mode operation. It is initially set to the program selected address from the J accumulator in the ND812 Central Processor. As each 24 bits of data are stored in the ND812 memory, the address is incremented by one. When the list is complete, the List Register interrupts the ND812 and requests processing of the list.

4-15. DIRECT MEMORY ACCESS CONTROL CIRCUITS. The direct memory access control circuits control the initiation and timing of DMA cycles during Direct Memory Increment and List modes. In the List mode, a double DMA cycle provides for dual precision transfer of data.



NOTE
Sheet number refers to the system diagram Figure 7-2 sheet number

Figure 4-2. ND4410 Control Module Functional Block Diagram

4-16. ACCUMULATOR CONTROL CIRCUITS. The accumulator control circuits select the Program Control Mode and specifies a trap address in the ND812 memory which contains a sub-routine to place pre-storage restrictions on the data transferred to the ND812 Central Processor.

4-17. OUTPUT CONTROL CIRCUITS. The output control circuits select one of the eight differently formatted 12-bit words to be set into the J or K accumulators of the ND812 Central Processor.

4-18. VERTICAL DISPLAY CIRCUITS. The vertical display circuits control the positioning of the data point on the Y-coordinate for the oscilloscope display or the X-Y Plotter.

4-19. HORIZONTAL DISPLAY CIRCUITS. The horizontal display circuits control the positioning of the data point on the X-coordinate for the oscilloscope display or the X-Y Plotter.

4-20. BLANKING CIRCUIT. The blanking circuit blanks X-Y display of the selected point until both the horizontal and vertical display circuits have assimilated the information presented by the program.

4-21. MARKER CIRCUIT. The marker circuit allows display of a marker full scale vertical line at the program selected address.

4-22. PLOT CONTROL CIRCUIT. The plot control circuit enables the X-Y plotter to plot the program selected data point.

4-23. MARKER/PLOTTER SKIP REQUEST CIRCUIT. The marker/plotter skip request circuit allows a program skip request to the ND812 Central Processor when a marker or plotter operation has been completed.

4-24. DETAILED FUNCTIONAL DESCRIPTION

4-25. The following description provides a detailed analysis of the ND4410 Control Module and Control timing for each mode of acquisition including timing diagrams depicting relationships of certain signals. Also, input/output signal descriptions are provided in tabular form for reference.

4-26. CONTROL CIRCUIT DESCRIPTION

4-27. The following is a circuit description of the ND4410 Control Module. Parenthetical expressions following signal names refer to location coordinates of that signal on logic diagrams in section VII. For example, IOMØ8* (3A2) indicates that signal IOMØ8* can be found in section VII on logic diagram sheet 3, zone A2 (Refer to Figure 4-3). Refer to Figure 4-2 and the logic diagrams in section VII as necessary while reading the following description

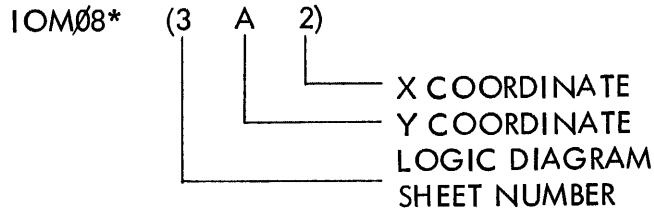


Figure 4-3. Signal Reference

4-28. COMMAND DECODERS. The command decoders circuit accepts signals from the ND812 Central Processor and converts them into control and timing signals. Signals IOMØØ* through IOMØ8* (3A1) are fed into a 9301 decoder to produce signals 750X, 751X, and 752X (3A2). Also, signals IOMØØ* through IOMØ8* in conjunction with signal IO74* are fed into another 9301 decoder (3A2) to produce signals Ø6ØX, Ø61X Ø62X, and Ø63X (3A3). Signals IOMØ* through IOM7* are added to produce signal 2Ø2X* (3A4). These decoded outputs in conjunction with Peripheral Control Pulses PCP1, PCP2, and PCP3 select program control operations within the Control Module.

4-29. ADC DECODER. The ADC decoder circuit accepts signals from the ND812 K accumulator and decodes them to determine which ADC will be enabled for acquisition. Signals OUT3*, OUT4*, and OUT5* at PCP1 time (3A3) will produce signals ON1* through ON4* (3A4). In this particular control module, only signal ON1* is utilized. When signals OUT3* through OUT5* are at +5 volts, signal ON1* will be at +5 volts, and the ADC will be enabled for acquisition.

4-30. MEMORY FIELD AND ACQUISITION MODE REGISTER. The memory field and acquisition mode register decodes the memory field for data transfer and the acquisition mode to be used. Signals OUTØØ* and OUTØ1* correspond to bits Ø and 1 respectively of the ND812 K register. They are fed into a shift register (4B2) which produces signals MFØ and MF1 which when added with signal DMAON produces signals ESMFØ* and ESMF1* (4B2). These signals indicate which memory field will be used for storage and display. The truth table is as follows:

OUTØØ*	OUTØ1	ESMFØ*	ESMF1	Memory Field
Ø	Ø	Ø	Ø	Ø
Ø	1	Ø	1	1
1	Ø	1	Ø	2
1	1	1	1	3

4-31. Signals OUTØ6* and OUTØ7* correspond to bits 6 and 7 respectively of the ND812 K register. They are fed into a shift register which produces signals BMØ* and BM1* to indicate which mode of acquisition will be used. The truth table is as follows:

OUTØ6*	OUTØ7*	BMØ*	BM1*	Acq. Mode
1	1	1	1	OFF
1	Ø	1	Ø	Accumulator
Ø	1	Ø	1	DMA Increment
Ø	Ø	Ø	Ø	DMA List

4-32. ADC CONTROL CIRCUITS. The ADC control circuits indicate that the ADC is in the ready state and controls the transfer of data from the ADC. Signal RDY1* (3B2) indicates that the ADC is in the ready state. This produces signal ATR1* which indicates that data is ready to be transferred from the ADC. This signal is sent to the ADC via Pin V, card connecor 112.

ATR1* (3B3) = 1 = not ready
ATR1* = Ø = ready

4-33. CLOCK CONTROL CIRCUIT. The clock control circuit provides the timing for data acquisition and interrupts. A 100 kHz crystal output (4A1) is gated with signal ADCB* (6B3) to provide signal G100KC (6B4). Signal ADCB* is gated with signal CT* (6B3). Signal CT* is from the ADC and indicates live or clock time selected on the ADC. When CT* is high, it indicates that live time was selected, and signal ADCB* is allowed to gate signal G100KC. If CT* is low, clock time is selected, and signal G100KC is effectively free-running. Signal C100KC is set into a times 100 decade scaler to produce signal 100FF (7A3) every 100 milliseconds which causes signal INTR* to interrupt the ND812 Central Processor if gated with signal IONL* (6A2).

4-34. Signal Ø61X at PCP2* time (6A2) clears the program interrupt. Signal STCLR* (6A2) clears the clock control circuit when the ND812 Central Processor START key is depressed. The 100 kHz crystal also provides an input to the front panel control circuits (2B4) for scanning of the 16 pushbuttons.

4-35. MULTIPLE INTERRUPT AND MODE INDICATOR REGISTER. The multiple interrupt and mode indicator register decodes OUTØ9* through OUT11* (4B3) to illuminate mode indicator lamps A, B, or C or any combination thereof. OUTØ8* (4B3) selects whether the top four pushbuttons on the Control Module front panel will interrupt the ND812 Central Processor once with each depression of the switch, or up to 50 times per second during the time the switch is held depressed. These four switches are marked: MOTION, WIDTH, MARK POS, and MARK SPAN. Signal Ø61X at PCP1* time will clear this circuit.

4-36. FRONT PANEL CONTROL CIRCUITS. The front panel control circuit generates signal SWFF (2A4) whenever any of the 16 control module front panel pushbuttons and the two ERASE pushbuttons are depressed. S1 thru S4 are gated with signal SCAN and MODE 1 to provide multiple signals SWFF. SWFF (4B1) gated with signal IONA generate signal INTR* which interrupts the ND812 Central Processor.

4-37. Signals MXØ thru MX3 indicate which pushbutton was depressed. Signal ER* is generated when both ERASE pushbuttons are depressed simultaneously (7B2). The Direction Switch (⟷) (7A2) controls the direction of the marker(s) for the MOTION,

WIDTH, MARK SPAN, and MARK SPAN functions. The truth tables for these switches are as follows:

OUTPUT SIGNAL				PUSHBUTTON DEPRESSED
SWFF				
Ø				NO
1				YES
MXØ	MX1	MX2	MX3	
Ø	Ø	Ø	Ø	S1 (MOTION)
1	Ø	Ø	Ø	S2 (WIDTH)
Ø	1	Ø	Ø	S3 (MARK POS)
1	1	Ø	Ø	S4 (MARK SPAN)
Ø	Ø	1	Ø	S5
1	Ø	1	Ø	S6
Ø	1	1	Ø	S7
1	1	1	Ø	S8
Ø	Ø	Ø	1	S9
1	Ø	Ø	1	S10
Ø	1	Ø	1	S11
1	1	Ø	1	S12
Ø	Ø	1	1	S13
1	Ø	1	1	S14
Ø	1	1	1	S15
1	1	1	1	S16
ER				ERASE
Ø				NO
1				YES
DIR				DIRECTION
Ø				RIGHT (→)
1				LEFT (←)

4-38. Signal Ø61X at PCP3* time generates signal SWCLR* (4B3) which clears Front Panel Control Circuits. Signal STCLR* (2B4) also clears this circuit when the computer START Key is depressed.

4-39. LIST REGISTER. The List Register contains the address of the list. It is set to the initial address of the list by signal Ø63X at PCP2 time (6B2) and then incremented for each DMA list mode cycle by signal DMAON (6B1). This initial address is transferred into the List register by signals OUTØ1* through OUT11* from the J Register to provide signals BAØØ through BA1Ø. Signals BAØØ through BA1Ø are then incremented to specify the address of the next storage location. Since the outputs are offset one bit from the inputs, the actual increment is by a factor of two. This is done to allow double precision storage during the list mode. When the last storage location of the list is filled, signal

BFLØ* is generated to provide signal INTR* (6A3). Signal INTR* interrupts the ND812 Central Processor so it may process the list. Signal STCLR* (6A2) clears signals BFLØ* and INTR* when the computer START Key is depressed.

4-40. DIRECT MEMORY ACCESS CONTROL CIRCUIT. The direct memory access control circuit controls the initiation and timing of Direct Memory Access cycles during the DMA Increment and DMA List modes. In the List mode, a double DMA cycle provides for dual precision transfer of data. When the ADC control circuits provide signal BLOCK (4B1) in the DMA Increment or DMA List mode, signal DMAR* is generated to request direct memory access to the ND812 Central Processor memory. The computer then provides signal DMAR* (4A4) to initiate a DMA cycle. Signal DMAP* clears signal DMAR* (4B1) and provides signal DMAON (4A4). The DMA Increment or DMA List mode is selected by signals BMØ and BM1* (4A4).

4-41. In the DMA increment mode, signal DMAP (7B4) sets the ADC address into the computer. Signal DMAON provides signals DIN* and ALTER* to initiate a read, Add-1, and write memory cycle (4A4) at the location in the computer memory addressed by the ADC.

4-42. Signal MRDY* (4B4) which controls the timing of the DMA cycle, provides signal TMRDY* which clears signal DMAON unless the memory has overflowed. An overflow condition is indicated by signal DAMRZ* (4B4) which provides signal TCSMRZ*. Signal TCSMRZ* provides signal SDDMA* (4A3) which initiates a new DMA cycle. At the completion of the second DMA cycle, signal MRDY((4B4) clears signal DMAON (4A4).

4-43. In the DMA List mode, signal DMAON increments the List register (6B1) and transfers the 12 bits of data into the output register (7A4). Signal DMAP* transfers this data into the computer. At the completion of the first DMA cycle, signal MRDY* provides signal BPH1* (4A4) to transfer the second 12 bits of data into the output register, and signal DMAON transfers the information into the computer. At the completion of the second DMA cycle, signal MRDY* clears signals DMAON and BPH1* (4A4). Signal EXGO* holds the DMA control circuits in a reset condition when the ND812 Central Processor is not in the run mode (4B2). Signals MFØ and MF1 in conjunction with signal DMAON provide signals ESMFØ* and ESMF1* (4B3) for selection of the memory field for DMA operation.

4-44. ACCUMULATOR CONTROL CIRCUIT. The accumulator control circuit selects the accumulator mode, and specifies a trap address in the ND812 Central Processor which contains a sub-routine to place pre-storage restrictions on the data presented to the computer.

4-45. Signals BMØ* and BM1 (4A3) select the accumulator mode. When the ADC is ready, signal BLOCK (4B4) provides signal INTR* (4A4) to request an interrupt for processing the ADC information. When the computer is ready to process the data, it provides signal INTP* (4B3) which sets the trap address ($Ø1ØØ_8$) into the accumulator via signal EXTØ5* (4B4). Signal CLRADC* clears the accumulator mode circuit (4B4).

4-46. OUTPUT CONTROL CIRCUIT. The output control circuit selects one of eight 12-bit words to be set into the J and K accumulators of the computer. Signals SØ, S1, and S2 (7A4) select one of the eight 12-bit words, and signal READ (7B4) sets the selected information into the computer.

4-47. Signal EXTK* stipulates the K accumulator for data input or output. Any of signals 752X, 2Ø2X, 75ØX, or Ø6ØX at PCP1 time will provide signal EXTK* (3A4). Either signal 752X at PCP1 or PCP2 time, or signals Ø6ØX and 1074 will provide signal DIN*. Signal DIN* stipulates data input to the computer.

4-48. Signals SØ, S1, and S2 are provided in varying logic configurations by signals PCP1, PCP2, 752X, DMAP*, BMØ, BM1, DMAON, Ø6ØX, BPH1, and DMAP (7A4). These inputs will select one bit of data from up to eight sources. The truth table is as follows:

SØ	S1	S2	Selected Source
Ø	Ø	Ø	1Ø
Ø	Ø	1	11
Ø	1	Ø	12
Ø	1	1	13
1	Ø	Ø	14
1	Ø	1	15
1	1	Ø	16
1	1	1	17

4-49. OUTPUT CIRCUITS. The output circuit consists of 12 eight-input multiplexers which select the data to be transferred into the J or K accumulators of the ND812 Central Processor. Selection of the inputs are controlled by signals SØ, S1, and S2 as detailed above. The 12 output signals are EXTØØ* through EXT11*. The eight inputs for each multiplexer in relation to their output signals are:

INPUT SELECTED								OUTPUT LINE
1Ø	11	12	13	14	15	16	17	
MXØ	--	ADCØØ*	ADC12*	--	PULL9	--	--	EXT11*
MX1	--	ADCØ1*	--	ADCØØ*	BAØ	--	--	EXT1Ø*
MX2	--	ADCØ2*	--	ADCØ1*	BAØ1	--	--	EXTØ9*
MX3	--	ADCØ3*	PDAØØ*	ADCØ2*	BA2	--	--	EXTØ8*
--	--	ADCØ4*	PDAØ1*	ADCØ3*	BA3	--	--	EXTØ7*
--	--	ADCØ5*	PDAØ2*	ADCØ4*	BA4	--	--	EXTØ6*
LFT	--	ADCØ6*	--	ADCØ5*	BA5	--	--	EXTØ5*
ER	--	ADCØ7*	--	ADCØ6*	BA6	--	--	EXTØ4*
SWFF	--	ADCØ8*	--	ADCØ7*	BA7	--	--	EXTØ3*
1ØØFF	--	ADCØ9*	--	ADCØ8*	BA8	--	--	EXTØ2*
--	--	ADC1Ø*	--	ADCØ9*	BA9	--	--	EXTØ1*
--	BFLØ	ADC11*	ALT'	ADC1Ø*	BA1Ø	--	--	EXTØØ*

NOTE

-- indicates not used.

4-50. VERTICAL DISPLAY CIRCUITS. The vertical display circuits contain the vertical display register, the vertical analog to digital converter, and the vertical deflection amplifier. Signals OUTØØ* through OUTØ9* are fed into the vertical display register by signal 750X at PCP1 time (5B3). These signals are the 10 most significant bits of the vertical or Y coordinate of the point selected by the program display. The outputs of the vertical display register are applied to the vertical digital to analog converter which converts these outputs to an analog current proportional to the value of the Y coordinate of the point to be displayed (5A4). This analog current is applied to the vertical deflection amplifier which changes the analog current to an analog voltage for application to the Y input of the display oscilloscope or X-Y plotter (5A4).

4-51. HORIZONTAL DISPLAY CIRCUITS. The horizontal display circuits contain the horizontal display register, horizontal digital to analog converter, and horizontal deflection amplifier. Signals OUTØØ* through OUTØ9* are fed into the horizontal display register by signal 75ØX at PCP2 time. These signals are the 10 most significant bits of the horizontal or X-coordinate of the point selected by the program for display (5A1). The outputs are applied to the horizontal digital to analog converters which convert these outputs to an analog current proportional to the value of the X-coordinate of the point to be displayed (5A2). This analog current is applied to the horizontal deflection amplifier which changes the analog current to an analog voltage for application to the X input of the display oscilloscope or X-Y plotter.

4-52. BLANKING CIRCUIT. The blanking circuit blanks the X-Y display of the selected point until both the horizontal and vertical display circuits have assimilated the information presented by the program. Signal 75ØX provides signal BLANK (5B2) which is applied to the display oscilloscope to blank the display. A predetermined time after PCP2 time, signal BLANK is removed to permit display of the selected point.

4-53. MARKER CIRCUIT. This circuit permits display of a marker (full scale vertical line) at the program selected address. Signal 75ØX at PCP3 time (5B4) provides signal MRK which is applied to the vertical display circuits (5A4) to cause display of a marker at the selected address.

4-54. PLOT ENABLE CIRCUIT. The plot enable circuit provides the plot signal to an X-Y plotter to enable plotting the program selected point. This is done by signal SEEK (5B3) which is provided by signal 751X at PCP3 time (5B2). After the X-Y plotter plots the selected point it provides signal CMPLT (5B2) which clears signal SEEK. Signal STCLR* clears the plot enable circuit to its initial state when the computer START key is depressed.

4-55. MARKER/PLOTTER SKIP REQUEST CIRCUIT. The marker/plotter skip request circuit provides a program skip request to the computer when a marker or plotter operation has been completed. Signal 751X at PCP1 time (5B3) provides signal ESKPR* which requests a program skip after a marker or plotter operation has been completed.

4-56. CONTROL TIMING FOR ACQUISITION MODES

4-57. The following discussion concerns control timing for the three modes of acquisition: Program Control Mode (Accumulator); DMA increment; and DMA List.

4-58. PROGRAM CONTROL MODE. When ADC has completed a conversion and is ready to transfer, data signal ADRY1* goes low and signal BLOCK goes high. Signal 1.5 μs later, transfer signal ATR1* goes low and signal BLOCK goes high. Signal BLOCK generates an interrupt to the Central Processor by forcing signal INTR* low. When the Central Processor is ready to process the interrupt, it responds with interrupt permit pulse INTP* going low. Pulse INTP* toggles signal EXTØ5* low and causes the Central Processor to trap to location $Ø1Ø1_8$. At PCP1* time, the K accumulator is loaded with ADC12* of the ADC address and with the ADC number, which in all cases will be ADC #1. Signal PCP1* causes data in signal DIN* to go low, and load K accumulator signal EXTK* to go low. Also at PCP1* time, signal READ is set high to gate the output data lines. On the trailing edge of PCP1*, signal EXTK* is reset high. At PCP2* time, the J accumulator is loaded with ADC11* through ADCØØ* of the ADC address. On the trailing edge of PCP2*, signal DIN* is reset high and signal READ is reset low. At PCP3* time, clear ADC signal CLADC* goes low, clearing the ADC in order to process another event. Signal CLADC* also resets signals ATR1* high, BLOCK low, and INTR* high. When the ADC is cleared, signal ADRY1* goes high.

4-59. DMA INCREMENT MODE. When the ADC has completed a conversion and is ready to transfer data, signal ADRY1* goes low (Figure 4-5). Approximately 1.Ø to 1.5 μs later, signal ATR1* goes low and signal BLOCK goes high. Signal BLOCK then generates an interrupt request to the Central Processor by causing signal DMAR* to go low. When the Central Processor is ready to process the DMA interrupt, it responds with DMA interrupt permit pulse DMAP* going low. The leading edge of DMAP* resets DMAR* high and the trailing edge of DMAP* triggers DMA active signal DMAON high. Signal DMAON causes data transfer signal DIN* to go low and signal ALTER* to go low. When signal ALTER* goes low, it initiates a read, add-1, and signals ESMFØ* and ESMF1*. During this DMA cycle, signal MRDY* from the Central Processor goes low. When the DMA cycle is complete, signal MRDY* goes high and causes signal DMAON to go low, which in turn, causes signals DIN* and ALTER* to go reset high. Signal CLADC* is set low by DMAON, clearing the ADC in order to process another event. Signal CLADC* also resets signals ATR1* high and Block low. When the ADC is cleared, signal ADRY1* goes high.

4-60. DMA LIST MODE. When the ADC has completed a conversion and is ready to transfer data, signal ADRY1* goes low (Figure 4-6). Approximately 1.Ø to 1.5 μs later, signal ATR1* goes low and signal BLOCK goes high. Signal BLOCK then generates a DMA interrupt to the Central Processor by causing DMA interrupt request signal DMAR* to go low. When the Central Processor is ready to process the interrupt, it responds with a DMA interrupt permit pulse DMAP* going low. The leading edge of DMAP* resets DMAR* high and the trailing edge of DMAP* sets DMA acting signal DMAON high. Signal DMAON loads the buffer address specified by the List Register into the ND812 memory via EXTØØ* through EXT1Ø* output gates. Signal DMAON also causes data

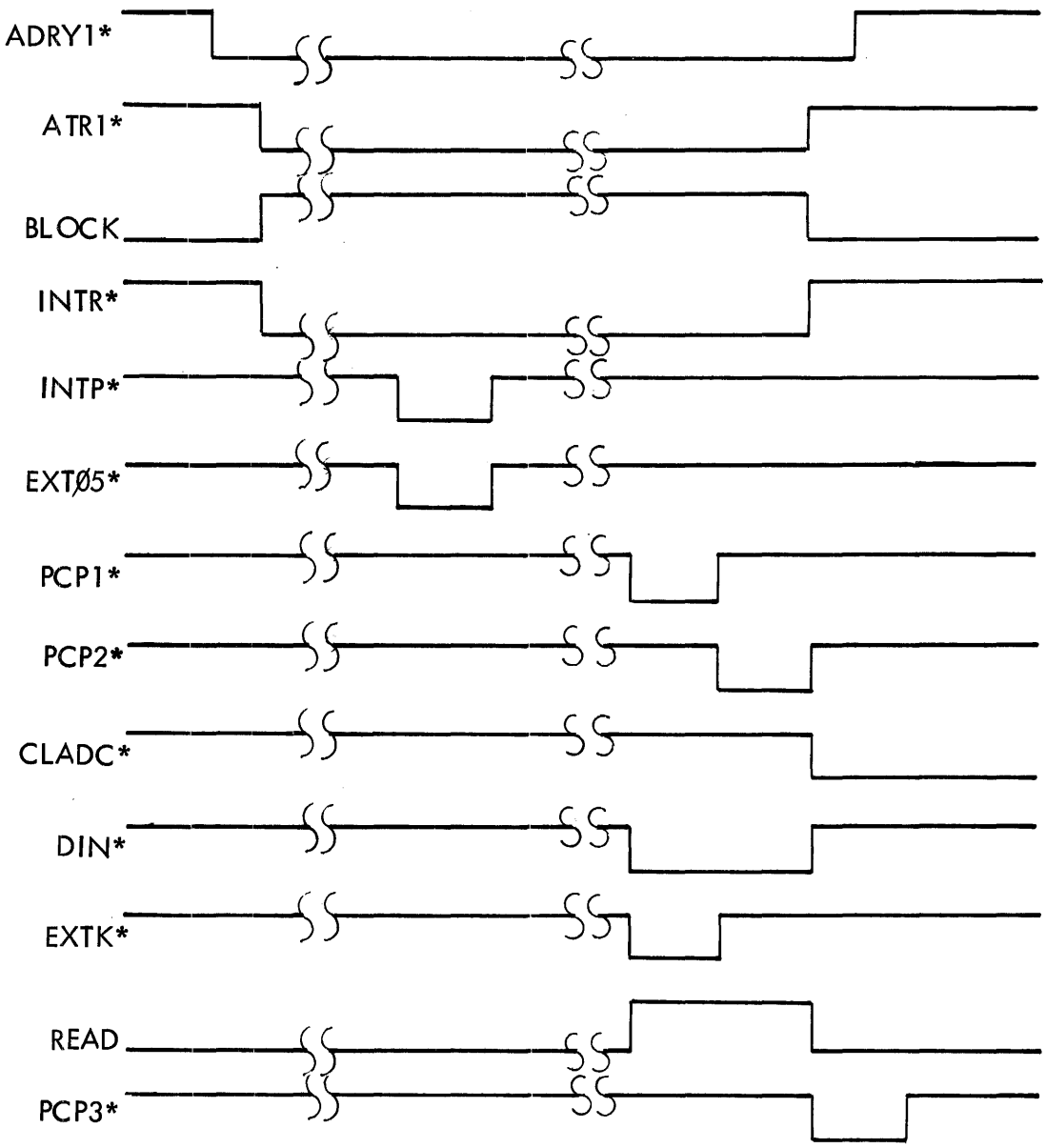
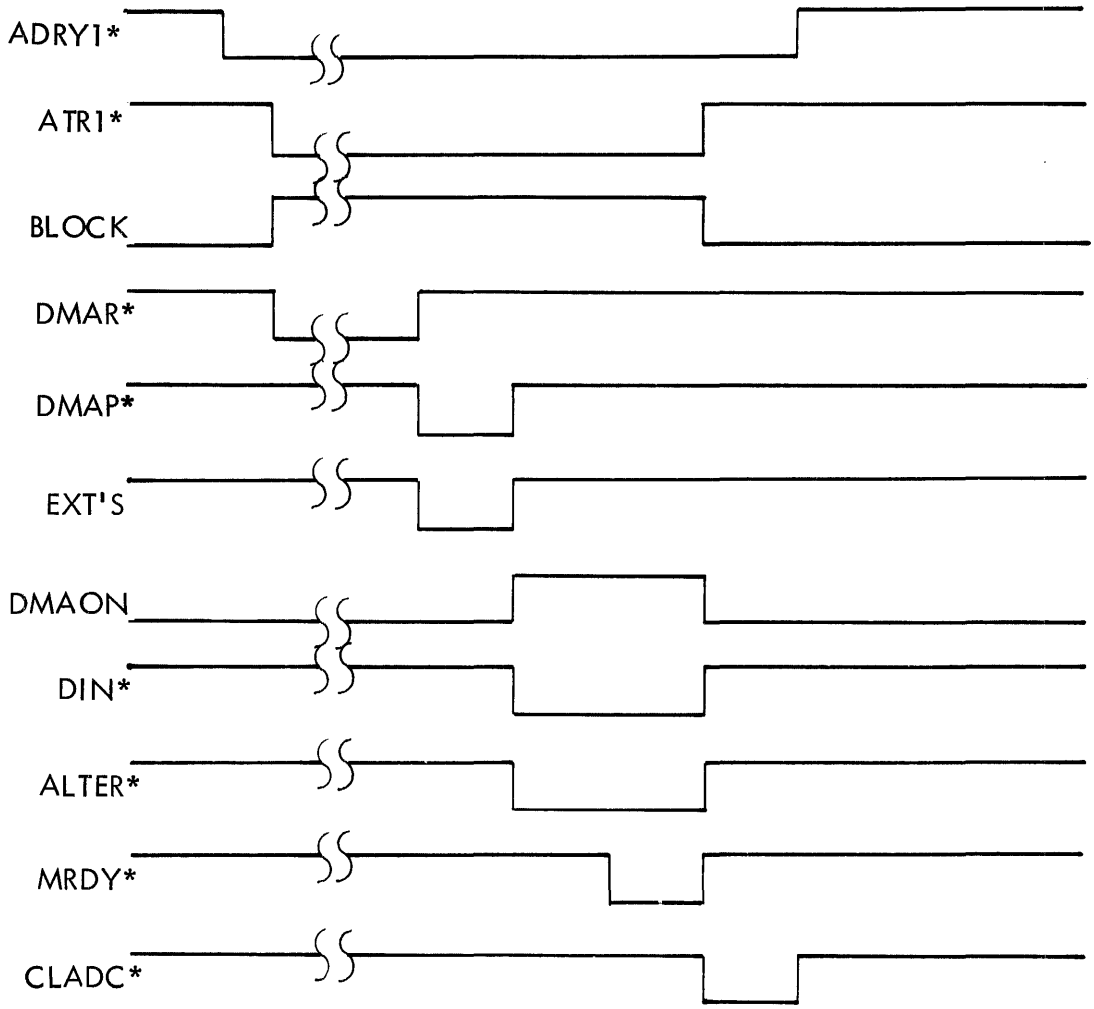
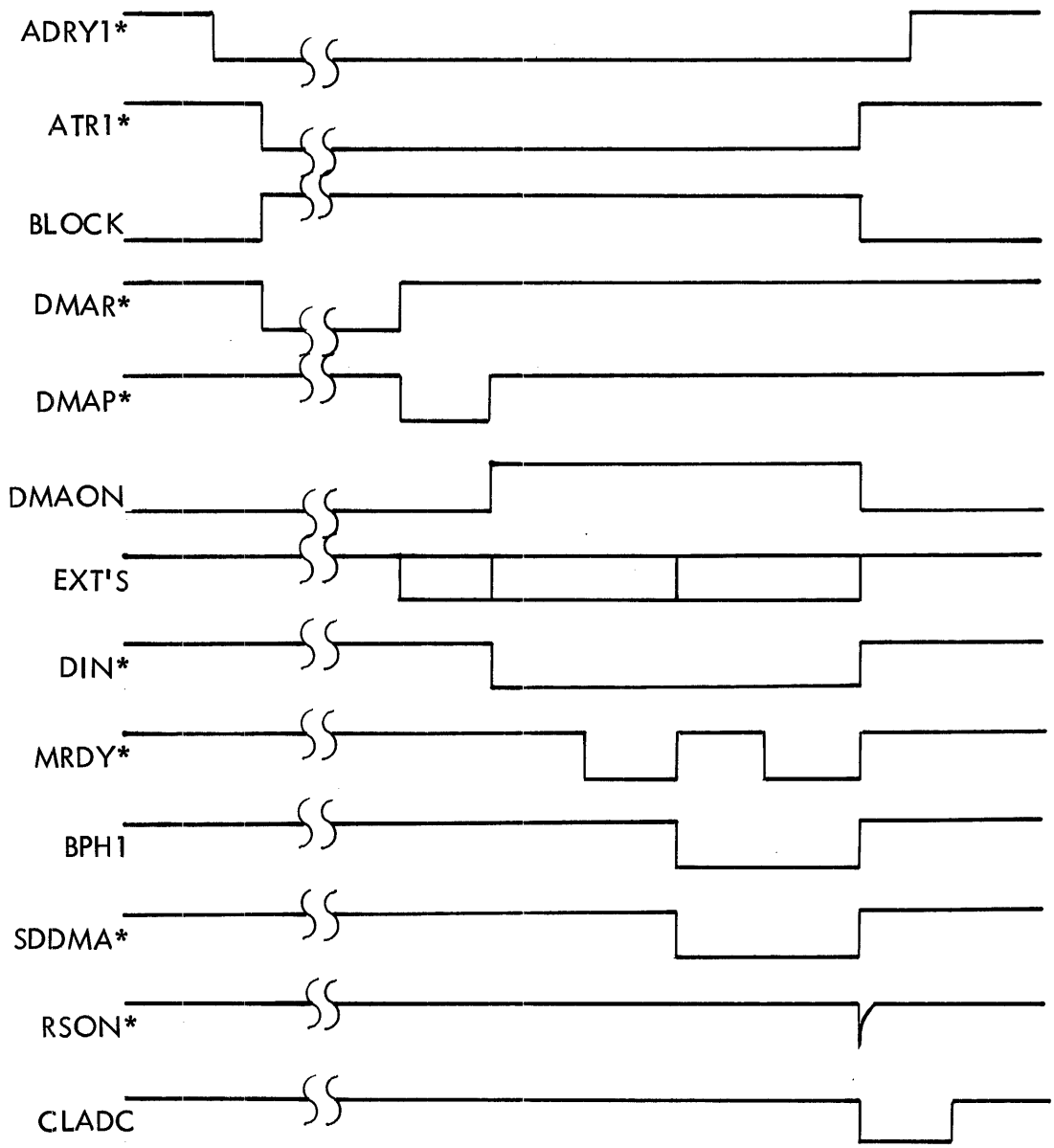


Figure 4-4. Program Control Mode Timing Diagram



NOTE: Signal EXT'S timing is data dependent.

Figure 4-5. DMA Increment Mode Timing Diagram



NOTE: Signal EXT'S timing is data dependent.

Figure 4-6. DMA List Mode Timing Diagram

input signal DIN* to go low. When signal DMAP* goes high and signal DMAON goes high, ADC12* and the ADC number (in this case, ADC #1) are transferred to the ND812 memory at the address previously specified by the contents of the List Register. During this time, memory ready signal MRDY* goes low. At the end of the memory cycle, signal MRDY* goes high causing buffer phase 1 signal BPH1 to go low. Signal BPH1 sets single/double DMA cycle signal SDDMA* low initializing a new memory cycle and updating the buffer address by one. During this memory cycle, signals ADCØØ* through ADC11* are loaded into the ND812 memory at the location specified by the updated buffer address.

Again during this memory cycle, signal MRDY* goes low, and at the end of the memory cycle, goes high causing signals BPH1 and SDDMA* to go high. This in turn triggers pulse RSON* low which resets signal DMAON low. Signal DMAON resets signal DIN* high and signal CLADC* low. Signal CLADC* resets signals BLOCK low and ATR1* high. Signal CLADC also clears the ADC in order to process another event. When the ADC is cleared, signal ARDY1* goes high.

4-61. INPUT/OUTPUT SIGNAL DESCRIPTION

4-62. Tables 4-1 and 4-2 lists the signal names, the associated pin locations, and provides a brief functional description of the input/output signals for printed circuit board connectors 111 and 112 respectively on the ND4410 Control Module.

Table 4-1. Input/Output Signals, Printed Circuit Board 111

SIGNAL	PIN	DESCRIPTION
DC COM	A, 1	Logic Signal common.
DIN*	C	Data In Output Signal DIN* selects the direction of data flow between the Control Module and the Computer. When signal DIN* is at +5 volts, data flow is from the Computer to the Control Module. When signal DIN* is at zero volts, data flow is from the Control Module to the Computer.
EXTØØ* EXTØ1* EXTØ2* EXTØ3* EXTØ4* EXTØ5* EXTØ6* EXTØ7* EXTØ8* EXTØ9* EXT1Ø* EXT11*	D E F H J K L M N P R S	External Output Bits Ø through 11 Signals EXTØØ* through EXT11* are the data output lines to the J and K Accumulators of the Computer. When an EXT signal is at +5 volts, the corresponding J or K Accumulator bit is set to the "Ø" state. When an EXT signal is at zero volts, the corresponding J or K Accumulator bit is set to the "1" state. The most significant bit is signal EXTØØ* and the least significant bit is signal EXT11*. Selection of the J or K Accumulator is controlled by signal EXTK*. Also puts address and data in ND812 memory during DMA modes.

Table 4-1. Input/Output Signals, Printed Circuit Board 111 (Cont'd)

SIGNAL	PIN	DESCRIPTION
EXTK*	T	External K Output/Input Signal EXTK* selects either the J or K Accumulator for data input from the Control Module. When signal EXTK* is at +5 volts, data is set into the J Accumulator. When signal EXTK* is at zero volts, data is set into the K Accumulator.
EINTR*	U	External Interrupt Request Output The steady state condition of signal EINTR* is +5 volts. When signal EINTR* is brought to zero volts, the computer is requested to interrupt the program.
INTP* (XINTP*)	V	Interrupt Permit Input The steady state condition of signal INTP* is +5 volts. When signal INTP* is brought to zero volts, it indicates the computer has accepted the interrupt requested by signal EINTR* and is asking for a trap address.
DMAR* (CSR*)	W	Direct Memory Access Request Output The steady state condition of signal DMAR* is +5 volts. When signal DMAR* is brought to zero volts, the computer is requested to enable direct access to the memory.
DMAP* (EXCSP*)	X	Direct Memory Access Permit Input The steady state condition of signal DMAP* is +5 volts. When signal DMAP* is brought to zero, it indicates the computer has enabled direct access to the memory and is asking for DMA address.
ALTER*	Y	Alter Data Output The steady state condition of signal ALTER* is +5 volts. When signal ALTER* is brought to zero volts, it initiates the alter of memory at the location selected during a DMA cycle.

Table 4-1. Input/Output Signals, Printed Circuit Board 111 (Cont'd)

SIGNAL	PIN	DESCRIPTION
SDDMA* (SDCS*)	Z	Single/Double Direct Memory Access Output Signal SDDMA* selects single or multiple direct memory access cycles. When signal SDDMA* is at +5 volts, it selects single DMA cycles. When signal SDDMA* is a zero volts, it selects double or repetitive DMA cycles.
DMAMRZ* (CSMRZ*)	AA	Direct Memory Access Memory Register Zero Input The steady state condition of signal DMAMRZ* is +5 volts. When the Computer Memory Register Count is zero during a DMA increment cycle, signal DMAMRZ* is brought to zero volts.
MRDY*	BB	Memory Ready Input The steady state condition of signal MRDY* is +5 volts. When signal MRDY* is brought to zero volts, it indicates the data is on the IOM's.
PCP1* PCP2* PCP3*	DD EE FF	Peripheral Control Pulses 1, 2 and 3 Signals PCP1*, PCP2* and PCP3* are timed sequenced zero to +5 volts pulses, 0.5 microseconds in duration, which controls the timing of program controlled operations. During PCP1* time, K Accumulator input/output functions are performed. During PCP2* time, J Accumulator input/output functions are performed. During PCP3* time, control functions are performed.
ESMFØ* (SMFØØ*) EXMF1* (SMFØ1*)	HH JJ	External Set Memory Field Bits Ø and 1. Signal EXMFØ* and ESMF1* select any one of the four 4K computer memory fields. ESMFØ — ESMF1* — Memory Field +5 volts — +5 volts — Ø (1st 4K) Ø volts — +5 volts — 1 (2nd 4K) +5 volts — Ø volts — 2 (3rd 4K) Ø volts — Ø volts — 3 (4th 4K)

Table 4-1. Input/Output Signals, Printed Circuit Board 111 (Cont'd)

SIGNAL	PIN	DESCRIPTION
ESKPR* (EXSKP*)	KK	External Skip Request Output The steady state condition of signal ESKPR* is +5 volts. When signal ESKPR* is brought to zero volts, the computer is requested to execute a program skip.
EXGO*	3	External Go Input Signal EXGO* is at zero volts when the computer is performing instructions, and at +5 volts when the computer program is halted.
OUTØØ* OUTØ1* OUTØ2* OUTØ3* OUTØ4* OUTØ5* OUTØ6* OUTØ7* OUTØ8* OUTØ9* OUT1Ø* OUT11*	4 5 6 7 8 9 10 11 12 13 14 15	Computer Output Bits Ø through 11 Signals OUTØØ* through OUT11* are the data input lines from the J and K Accumulators of the Computer. When an OUT signal is at +5 volts it represents the "Ø" state of the corresponding J or K Accumulator bit. When an OUT signal is at zero volts, it represents the "1" state of the corresponding J or K Accumulator bit. The most significant bit is signal OUTØØ* and the least significant bit is signal OUT11*.
IOMØØ* IOMØ1* IOMØ2* IOMØ3* IOMØ4* IOMØ5* IOMØ6* IOMØ7* IOMØ8*	16 17 18 10 20 21 22 23 24	Input/Output Memory Bits Ø through 8. Signals IOMØØ* through IOMØ8 contains the program input/output instructions. When an IOM signal is at +5 volts, it represents the "Ø's" state of the corresponding computer memory bit. When an IOM signal is at zero volts, it represents the "1's" state of the corresponding computer memory bit. The most significant bit is signal IOMØØ* and the least significant bit is signal IOMØ8*.
IO74*	28	Input/Output 0740_8 Signal IO74* at zero volts defines a single or two word input/output control instruction.

Table 4-1. Input/Output Signals, Printed Circuit Board 111 (Cont'd)

SIGNAL	PIN	DESCRIPTION
STCLR* (XSTCL*)	29	Start Clear Input Signal STCLR* is at +5 to zero volt pulse provided when the computer power is turned on, or when the computer START key is depressed to clear all main control circuits in preparation for a new instruction.
IONB*	30	Interrupt On B-Level The steady state condition of signal IONB* is +5 volts. When signal INOB* is brought to zero volts, it enables B-level or lower interrupts to interrupt the program.
IONL*	31	Interrupt On LOW-Level The steady state condition of signal IONL* is +5 volts. When signal IONL* is brought to zero volts, it enables Low-level interrupts to interrupt the program.

Table 4-2. Input/Output Signals, Printed Circuit Board 112

SIGNAL	PIN	DESCRIPTION
ADCØØ*	N	ADC Bits Ø through 12
ADCØ1*	M	
ADCØ2*	L	Signals ADCØØ* through ADC12* contain the address to be
ADCØ3*	K	transferred to the control module when signal ATR1* is
ADCØ4*	J	brought to zero volts. When an ADC signal is at +5 volts,
ADCØ5*	H	its corresponding address bit is a "Ø". When an ADC
ADCØ6*	F	signal is at zero volts, its corresponding address bit is a
ADCØ7*	E	"1". The most significant bit is ADC12* and the least
ADCØ8*	D	significant bit is ADCØØ*.
ADCØ9*	C	
ADC1Ø*	B	
ADC11*	A	
ADC12*	P	
A*	U	Acquire Output Signal A* is brought to zero volts to allow the ADC to acquire data, and to +5 volts to prohibit it from acquiring data.

Table 4-2. Input/Output Signals, Printed Circuit Board 112 (Cont'd)

SIGNAL	PIN	DESCRIPTION
ATR1*	V	ADC Transfer Output The steady state condition of signal ATR1* is +5 volts. When signal ATR1* is brought to zero volts, address data from the ADC is transferred to the Control Module.
ADCB*	X	ADC Busy Input Signal ADCB* is at +5 volts when the ADC is not busy and at zero volts when it is busy and cannot validly accept input pulses.
ADRY1*	DD	ADC Ready Input The steady state condition of signal ARDY* is +5 volts. Upon completion of a conversion by the ADC signal, ARDY* is brought to zero volts to indicate the ADC is ready to transfer data.
CT*	R	Clock Time Input Signal CT* is brought to zero volts when the clock time is selected at the ADC.
CLADC*	W	Clear ADC The steady state of signal CLADC* is +5 volts. When signal CLADC* is brought to Ø volts, it indicates a transfer of data from the ADC is completed and clears the ADC in order to process the next event.
ALT'	S	Alter Input The steady state of ALT' is Ø volts. When signal ALT' is brought to +5 volts, it indicates that the ADC data is invalid and a dummy transfer is executed. NOTE Signal ALT' is used only when an ADC without AUTO/ALT is connected to the ND4410.

Table 4-2. Input/Output Signals, Printed Circuit Board 112 (Cont'd)

SIGNAL	PIN	DESCRIPTION
Gnd	AA BB CC 15	Logic signal common
BIØØF	Z	Buffer 100 KHz output Gated timing signal for use with the optional Model 802 Biomation Recorder Interface. Its steady state is Ø volts. Its true state is +5 volts.

4-63. POWER CONNECTOR. Table 4-3 lists the voltages, associated pin locations and power requirements of the input power signals for the 42-pin male connector on the rear panel of the ND4410 Control Module.

Table 4-3. Power Connector

SIGNAL	PIN	DESCRIPTION
+6V	10	Power input, +6 volts D.C. at 1 ampere.
+12V	16	Power input, +12 volts D.C. at 50 milliamperes.
-12V	17	Power input, -12 volts D.C. at 50 milliamperes.
DC COM	34	Power return ground.

SECTION V.
MAINTENANCE

5-1. GENERAL

5-2. This section contains instructions required to maintain the ND4410 Data Acquisition and Display System. The instructions include preventive and corrective maintenance procedures. Preventive maintenance includes periodic inspection and performance standards tests of the equipment. Corrective maintenance includes alignment and adjustment, and repair.

5-3. MAINTENANCE PHILOSOPHY

5-4. The maintenance philosophy for the ND4410 system is to first locate the faulty module within the basic system - the Power Supply module, the ND812 Computer module, the ND4410 Control Module, or the ADC Module.

5-5. After locating the faulty unit, refer to the applicable module instruction manual for detailed testing and troubleshooting procedures. If a peripheral fault is suspected, refer to that peripheral instruction manual for testing procedures. Testing and troubleshooting steps for the Control Module are included in this manual.

5-6. EQUIPMENT REQUIRED FOR MAINTENANCE

5-7. Table 5-1 is a list of test equipment required for maintenance.

Table 5-1. Required Test Equipment

Nomenclature	Manufacturer's Model or Part No.	Manufacturer*
Multimeter	630-A	Triplett
Extender Card for Board 104	72-0219	Nuclear Data

* or equivalent

5-8. MAINTENANCE CONTROLS, INDICATORS, AND TEST POINTS

5-9. All maintenance controls are located on the ND812 Computer front panel, ND4410 Control Module front panel, or Teletype. Test points for dc voltage checks are shown in Figure 5-1. All other test results are oscilloscope displays or Teletype responses.

5-10. PREVENTIVE MAINTENANCE

5-11. Periodic inspection of the equipment is necessary to detect potential trouble before a malfunction occurs. Items such as condition of connectors and cables, proper operation of controls and indicators, and cleanliness of equipment, should be monitored and corrected as required prior to each use.

5-12. PERFORMANCE STANDARDS TESTS

5-13. The performance standards tests provide a means of determining if the equipment is operating properly. These procedures may be performed at regular intervals, before each normal operational use of the equipment, or if a malfunction is suspected.

5-14. Perform the procedures in the order given. If a malfunction is detected, refer to the indicated equipment manual and perform the testing and troubleshooting steps in that manual. Repair the fault and return to the beginning of the performance standards tests in this manual. Repeat all steps until another malfunction is detected or until all performance tests are completed.

5-15. DC VOLTAGES AND POWER DISTRIBUTION TESTS. Disconnect ac power and remove all plug in modules, except the power supply, from the NIM bin. Test for correct dc voltages and power distribution as follows:

a. Plug power supply into correct ac source and turn on front panel power switch.

b. Front panel power indicator should light. If not, check fuses and ac source.

CAUTION

If fuses are blown, determine cause of overcurrent and repair before power is reapplied.

c. Refer to Figure 5-1, and check for the indicated dc voltage at each connector in the bin. Dc voltages are shown with respect to chassis ground.

d. If any voltages are incorrect, refer to the power supply instruction manual for adjustment and/or testing procedures.

e. If all voltages are correct, turn off power, replace plug-in modules, and proceed to paragraph 5-16.

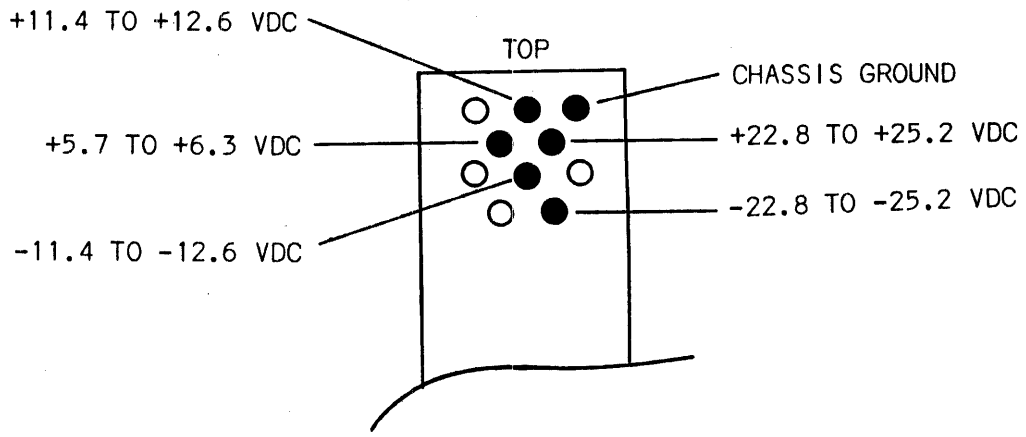


Figure 5-1. NIM Bin Connector, Dc Voltage Requirements

5-16. ND812 COMPUTER TESTS. Refer to ND812 Diagnostics manual and perform computer diagnostics as required. If the Computer fails any of the diagnostics, perform troubleshooting and repair as indicated. After repair, repeat the diagnostics to ensure normal operation has not been impaired by repair. When the Computer responds correctly to all diagnostic tests, proceed to paragraph 5-17.

5-17. ND4410 CONTROL MODULE TESTS. The ADC should be disconnected from the ND4410 system before Control Module tests are performed. Refer to Section II for Teletype, ND812 Computer and oscilloscope interconnections. The listing and flow diagrams for ND4410 Control Module Diagnostic Test Program, part number 41-8044, are shown in the ND4410 Diagnostic Software Manual. Load the diagnostic tape into the ND812 Computer as follows:

a. Depress ND812 STOP switch.

b. Load program into tape reader. Be sure leader is over read heads before continuing.

c. Simultaneously press ND812 LOAD AR and NEXT WORD switches.

d. Tape is automatically read into the ND812. After tape motion stops, check that J register is all zeroes. If not, reload tape.

e. Set SWITCH REGISTER switches to 2000_8.

f. Depress ND812 LOAD AR and START switches.

5-18. After loading the diagnostic program, refer to Table 5-2 and test the horizontal and vertical display circuits in the Control Module by setting ND812 Computer SWITCH REGISTER switches as indicated. Check for the required oscilloscope display for each switch setting. If any displays are incorrect, refer to paragraph 5-26 for alignment of display circuits. After adjustment, repeat the checks in Table 5-2. If displays are still incorrect, troubleshoot and repair, and repeat the tests in Table 5-2.

Table 5-2. ND4410 Control Module Display Circuits Test

ND812 SWITCH REGISTER Switch Positions	Required Oscilloscope Display
Switch 0 up, all others down	Horizontal display at Y = 0.
Switch 1 up, all others down	Vertical display at X = 0.
Switch 2 up, all others down	Positive ramp
Switch 3 up, all others down	Negative ramp
Switch 4 up, all others down	Positive and negative ramp
Switch 5 up, all others down	Horizontal display with markers at 1/4 and 3/4 scale deflection.
Switch 6 up, all others down	Horizontal display intensifies from 0 to 1/4 and 3/4 to full scale deflection, dims from 1/4 to 3/4 scale deflection.

5-19. Check the operation of ND4410 Control Module clock circuit by momentarily setting ND812 Computer SWITCH REGISTER switch 7 up and back down. (All other SWITCH REGISTER switches are down.) After approximately 10 seconds, Teletype should print 100.0 ± 0.04 cps. If printout is not correct, troubleshoot control module clock circuit and repair. After repair, repeat this test and check for proper Teletype response.

NOTE

If "2" is printed, status bit 2 (CLK INT) is missing.

5-20. Test the operation of ND4410 Control Module front panel lamps and switches as follows:

a. All lamps, except ACQUIRE, should be on.

b. Set ND812 SWITCH REGISTER switch 9 up and all others down. Front panel lamp C should go out. A and B should be on.

c. Set switch 10 up and all others down. Lamp B should go out. A and C should be on.

d. Set switch 11 up and all others down. Lamp A should go out. B and C should be on.

e. For this program, the front panel switches are assigned alphabetic references. The following matrix represents the front panel switch locations and assigned references:

A	B	C	D
E	F	G	H
I	J	K	L
M	N	O	P

f. Set ND812 SWITCH REGISTER switch 8 up and all others down. (This disables multiple interrupt on switches A, B, C, and D.) Refer to Table 5-3 and check for the required Teletype response as each front panel switch is depressed.

NOTE

If "3" is printed, status bit 3 (SWITCH INT) is missing.

g. Depress both front-panel ERASE pushbuttons. "Q" should be printed.

Table 5-3. ND4410 Control Module Front Panel Switch Test

Front Panel Switch Setting	Teletype Response
Left-Right switch Left and depress:	
A	AL
B	BL
C	CL
D	DL
Left-Right switch Right and depress:	
A	AR
B	BR
C	CR
D	DR
Depress remaining front panel switches E through P.	Assigned letter is printed for each switch E though P.

h. Set all ND812 SWITCH REGISTER switches down. Refer to Table 5-3 and repeat the tests for front panel switches A, B, C, and D. The Teletype response should be a multiple printout of the response shown in Table 5-3 with the number of printouts dependent upon the length of time the applicable switch is held depressed.

5-21. If the ND4410 Control Module fails any of the above diagnostic tests, troubleshoot the circuit area being tested by the diagnostic and repair. After repair, repeat the diagnostics. When the Control Module responds correctly to all diagnostic tests, proceed to paragraph 5-22.

5-22. ADC TESTS. Refer to the ADC instruction manual, part number IM88-0415 (50 MHz ADC) or IM88-0426 (100 MHz ADC), and perform the performance test procedures. If the ADC fails a test, troubleshoot and repair. After repair, repeat the performance tests until all test conditions are met.

5-23. CORRECTIVE MAINTENANCE

5-24. ALIGNMENT AND ADJUSTMENT

5-25. Reference to adjustment procedures is made primarily during performance testing when a test tolerance is not met. However, if repair is necessary in a circuit area containing an adjustable component, that component should be adjusted after repair is affected to assure optimum performance. Also, unless otherwise specified, all adjustable components on a replacement card should be adjusted after that card is installed in the Control Module.

5-26. Three ND4410 adjustable components are located on board 104. Refer to Figure 5-2 for adjustment locations. The following paragraphs list the adjustable components in the ND4410 Control Module, describe preferred adjustment methods, and specify tolerances. Extend board 104 using extender card, part number ND72-0219.

5-27. HORIZONTAL DISPLAY POSITION ADJUSTMENT. Adjust the position of the horizontal display as follows:

a. Be sure oscilloscope is aligned properly. Using diagnostic program, obtain horizontal display (paragraph 5-18).

b. Adjust vertical adjustment potentiometer (Figure 5-2) for proper positioning of horizontal display (Y = 0).

5-28. VERTICAL DISPLAY POSITION ADJUSTMENT. Adjust the position of the vertical display as follows:

a. Be sure oscilloscope is aligned properly. Using diagnostic program, obtain vertical display (paragraph 5-18).

b. Adjust horizontal adjustment potentiometer (Figure 5-2) for proper positioning of vertical display (X = 0).

5-29. DISPLAY MARKER POSITION ADJUSTMENT. Adjust the position of the display markers as follows:

a. Be sure oscilloscope is aligned properly and that the horizontal and vertical positioning is accurate. Using diagnostic program, obtain horizontal display with markers at 1/4 and 3/4 scale deflection (paragraph 5-18).

b. Adjust marker adjustment potentiometer (Figure 5-2) for proper positioning of markers.

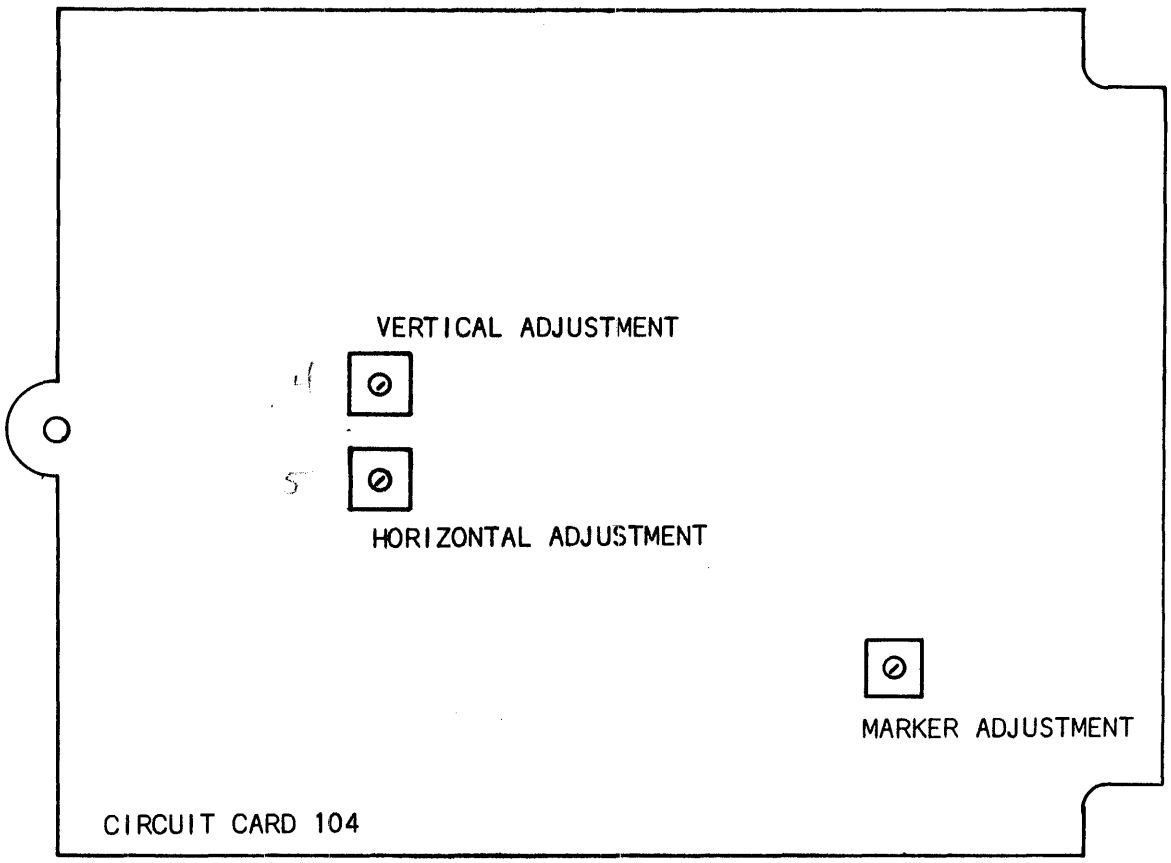


Figure 5-2. ND4410 Control Module, Adjustment Locations

SECTION VI.
REPLACEMENT PARTS LIST

6-1. GENERAL

6-2. Table 6-1 provides a non-illustrated list of replaceable parts for the ND4410 System Control Module.

Table 6-1. Replaceable Parts List

N.D. Part Number	Description
01-0132	Bracket clamp
01-0160	Angle Panduct
01-0161	Rod lock
01-0162	Panduct
01-0179	Strip Desig 101 112
01-0240	Bracket cable 50 50
01-0241	Shield 50 50 Mod
02-0512	Plate Guide
02-0515	Bus Bar
02-0705	P. P. CNT MOD.
02-0706	BRKT SW ASSY NTG
02-0707	Panel Rear
03-0043	Module
10-0047	CNN INDT CRTRG
10-0066	JAX BANA YEL
10-0068	JAZ BANA BL
10-0095	BNC JAX
10-0096	BNC PLUG CBL

Table 6-1. Replaceable Parts List (Cont'd)

N.D. Part Number	Description
10-0112	SKT PCBD MTG 14
10-0115	SKT WRP 14
10-0116	SKT WRP 16
10-0118	RECPT PC BD 62 PIN
10-0122	CNN PC 31/62 CTT
10-0156	PLG 16 PN DIP
10-0159	SKT IC 14 WRP .4CNTR
10-0160	SKT IC 16 WRP .4CNTR
10-5001	BLC PIN PH 50 CTT
10-5003	CNN SKT 50 CTT
10-5019	BLC PIN DP 42 POS
10-5020	SKT BLC 42 POS
11-0005	SHLD LNG STL 50 POS
11-5001	CRN GID PIN 34/50 PB
11-5002	CRN GID SKT 14/50 PB
11-5010	CRN GID SKT GOLD AEC
11-5011	GID PIN CRN GLD
12-0002	LKNG SP ASSY LG
12-5003	CTT PN GLD 16 18 GA
12-5005	SNP IN REC CTT
12-5007	CNT SKT SIZE 20
12-5008	CTT SIZE 20 PN
12-5013	TERM SOLDS RING
12-5020	CNTCT SKT GOLD 18 16
12-5026	GND LUG SLD
12-5037	Polarizing Key Plug
12-5042	PO WRP 1 INC
13-0013	SCR 6-32 X 1Q PNHD SEM
13-0016	SCR 6-32 X 1Q 100D FH
13-0021	SCR 6-32 X 14 PHPNHD
13-0038	SCR 6-32 X 3E PH
13-0039	SCR 6-32 X 1 PNHD EXT
13-1003	LOCK TERM LUG NO6
13-1010	DECORATIVE MTG NUT
13-1017	WASHER N04 9 320D
13-1023	LOCK TERM NO. 4 HOLE

Table 6-1. Replaceable Parts List (Cont'd)

N. D. Part Number	Description
13-1038	SLEEVE SOLDER
13-2009	Panel FSTNER SOUTHCO
13-2014	FSTN HEDLOCK BNS
13-3055	SPACER RD. 6-32 1 IN
13-4002	MTG CLIP TINNERMAN
14-1001	XT 100KC WIRE
14-2018	LMP IND INCD AMB
16-0113	WRE 22GA RED
16-0114	WRE 22GA ORG
16-0115	WRE 22GA YEL
16-0117	WRE 22GA BL
16-0118	WRE 22GA VIO
16-0119	WRE 22GA GR
16-0149	CBL COAX SUBMNX 24GA
16-0151	CBL RBN 61 CNDT
16-0175	CBL RIB 16 CNDT
21-0007	RSMG 10 OHM QW 5P
21-0024	RSMG 51 OHM QW 5P
21-0031	RSMG 100 OHM QW 5P
21-0034	RSMG 130 OHM QW 5P
21-0039	RSMG 220 OHM QW 5P
21-0042	RSMG 300 OHM QW 5P
21-0043	RSMG 330 OHM QW 5P
21-0047	RSMG 470 OHM QW 5P
21-0048	RSMG 510 OHM QW 5P
21-0055	RSMG 1K QW 5P
21-0059	RSMG 1.5K QW 5P
21-0062	RSMG 2.0K QW 5P
21-0063	RSMG 2.2K QW 5P
21-0065	RSMG 2.7K QW 5P
21-0072	RSMG 5.1K QW 5P
21-0077	RSMG 8.2K QW 5P
21-0079	RSMG 10K QW 5P
21-0083	RSMG 15K QW 5P
21-0089	RSMG 27K QW 5P
21-0099	RSMG 68K QW 5P

Table 6-1. Replaceable Parts List (Cont'd)

N.D. Part Number	Description
21-0108	RSMG 160K QW 5P
21-5016	RSMF 1K EW 1P
21-5027	RSMF 6.19K EW 1P
21-5028	RSMF 7.68K EW 1P
21-5036	RSMF 12.4K EW 1P
21-5045	RSMF 24.9K EW 1P
21-5053	RSMF 49.9K EW 1P
21-5058	RSMF 100K EW 1P
21-5062	RSMF 200K EW 1P
21-5076	RSMF 1.6MEG QW 1P
21-5079	RSMF 400K EW .25P
21-5030	RSMF 800K QW .5P
24-0096	RSVR 5K HW 5P
25-0001	RSNTW 2.2K 14 DIP
25-0002	RSNTW 220 330 16 DIP
26-0008	CPSM 150PF 500V
26-0010	CPSM 250PF 500V
26-0011	CPSM 330PF 500V 5P
26-0012	CPSM 500PF 500V 5P
26-0014	CPSM 1000PF 100V
26-1004	CPMY .01MFD 100V
26-1006	CPMY .1MFD 100V
26-2000	CPTM .22MFD 35V
26-2015	CPTM 4.7MFD 35V 20P
26-2020	CPTM 6.8MFD 35V 20P
26-2024	CPTM 22MFD 15V
26-4005	CPCR .01MFD 25V
26-4008	CPCR .1MFD 30V
26-4019	CPCR .1MFD 10V
31-0004	DO ZR 1N4728A
31-0005	DO ZR 1N4734A
31-0006	DO ZR 1N4736A
31-0013	DO SIL SIG 1N914B

Table 6-1. Replaceable Parts List (Cont'd)

N.D. Part Number	Description
32-0001	DO NTW 16DO 14 DIP
33-0036	TRSL PNP 2N3640
33-0086	TRSL NPN MJE 3055
35-0006	IC 944 DIP 14 PG
36-0008	DTL 946 DIP 14G
35-0009	IC 948 DIP 14FF
35-0010	DTL 962 DIP 14G
35-0017	IC 936 DIP 14HX IVT
35-0023	IC U5B77039X 8L OPA
35-0033	IC MC857P DIP 14 BG
35-0034	IC MC858P DIP 14PG
35-0039	MSI 9300 DIP 16 SR
35-0041	IC 9601 DIP 14 MONO
35-0053	IC SN7474N DIP 14FF
35-0058	IC 9002 DIP 14G
35-0059	IC 9003 DIP 14G
35-0060	IC 9004 DIP 14G
35-0063	IC 9007 DIP 14G
35-0066	IC 9016 DIP 14 HXVT
35-0068	MSI 9312 DIP 16 MLPX
35-0069	MSI 9301 DIP 16 DCDR
35-0072	IC 9022 DIP 16 DUJK
35-0077	MSI 9310 DIP 16 DCTR
35-0083	MSI 9316 DIP 16 CTR
35-0110	MSI 9318 DIP 16
37-4001	SW MTRY SPST 1 AMP
37-5017	SW SLD RK SPDT W DTN
37-8055	KBRD 16K SDST
37-8056	BNT LDG WH
42-0008	WRP 4400 CNT
42-0009	WRP 4409
42-0010	WRP 4407
42-0011	WRP 4405
42-0012	WRP 4402

Table 6-1. Replaceable Parts List (Cont'd)

N.D. Part Number	Description
50-0254	PCB EXB
50-0350	PCB DEC
50-0415	PCB CCS
50-0436	PCB TCC
50-0439	PCB WW1
50-0457	PCB NIT
50-0475	PCB ICS
54-0253	F.P. Control Mod.
55-0107	R.P. Control Mod.
70-0716	4409-A
70-0717	4407-A
70-0718	4405-A
70-0719	4402-A
70-1737	DEC-K
70-1814	NIT-A
70-1856	ICK-H, BT, BH, X, Q-A
71-0041	F.P. TO A6-102
71-0042	F.P. TO A7-102
72-0219	EXB 23
72-0795	R.P. Cont. Mod.
72-0796	MOD. Control
72-0797	F.P. Cont. Mod.
72-0815	ADC CNT. MOD. CONN.
72-0816	CMPTR86-62 STACK CONN
75-0180	2200 PWR CBL

SECTION VII.
DIAGRAMS

7-1. GENERAL

7-2. This section contains logic diagrams to be used for troubleshooting the ND4410 System Control Module. Table 7-1 provides an index for diagrams contained in this section. Figure 7-1 provides general notes which apply to logic diagrams in this section; and illustrates how to identify connectors, connector pins, integrated circuit types, printed circuit board name, and location of integrated circuits on printed circuit boards.

Table 7-1. Diagram Index

Figure No.	Description	Page No.
7-1	Logic Diagram Notes	7-2
7-2	ND4410 System Diagram, Signal Destinations (Sheet 1 of 11)	7-3/7-4
7-2	ND4410 System Diagram, Front Panel Control Circuits (Sheet 2 of 11)	7-5/7-6
7-2	ND4410 System Diagram (Sheet 3 of 11)	7-7/7-8
7-2	ND4410 System Diagram (Sheet 4 of 11)	7-9/7-10
7-2	ND4410 System Diagram (Sheet 5 of 11)	7-11/7-12
7-2	ND4410 System Diagram (Sheet 6 of 11)	7-13/7-14
7-2	ND4410 System Diagram (Sheet 7 of 11)	7-15/7-16
7-2	ND4410 System Diagram (Sheet 8 of 11)	7-17/7-18
7-2	ND4410 System Diagram (Sheet 9 of 11)	7-19/7-20
7-2	ND4410 System Diagram (Sheet 10 of 11)	7-21/7-22
7-2	ND4410 System Diagram (Sheet 11 of 11)	7-23/7-24

NOTES:

1 - ALL DIODES ARE G964 OR EQUIVALENT, EXCEPT AS NOTED.

2 - ALL RESISTORS ARE 1/4W, ±5%, EXCEPT AS NOTED.

3 - ALL CAPACITORS ARE pf, EXCEPT AS NOTED.

4 - I.C. VOLTAGES, EXCEPT AS NOTED:

14 PIN DIP, PIN (7) GND: PIN (14) +5V

16 PIN DIP, PIN (8) GND: PIN (16) +5V

24 PIN DIP, PIN (12) GND: PIN (24) +5V

5 - THE FOLLOWING SYMBOLS/NOTATIONS ARE USED ON THE DIAGRAM AND/OR PRINTED CIRCUIT BOARD ASSEMBLY.

IC - INTEGRATED CIRCUIT

Q - TRANSISTOR

( ) - IC PIN DESIGNATION

- CONNECTOR DESIGNATION

NC - NO CONNECTION

SAT - SELECT AT TEST

(P1) - PRECISION RESISTORS 100PPM 1/8W, ±1% METAL FILM

- DC COMMON

FB - FERRITE BEAD

- GERMANIUM DIODE

- SILICON DIODE

- ZENER DIODE

- TUNNEL DIODE

- SELENIUM DIODE

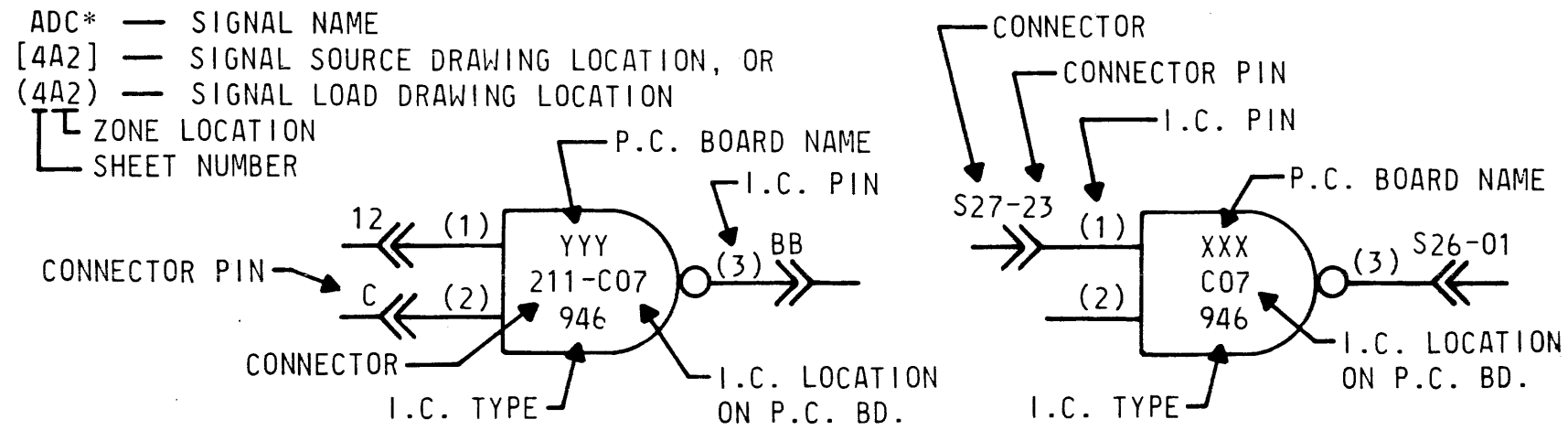


Figure 7-1. Logic Diagram General Notes

SIGNAL	DESTINATIONS		DESTINATIONS	SIGNAL	DESTINATIONS	SIGNAL	DESTINATIONS
A1*	[3A3] (4B1)	DMAMRZ*	(4B4)	IOMØ*	(3A1), (3A2), (3A4)	OUT1Ø*	(4B3), (6B1)
ADCB*	(3B2) (6B3)	DMAON	[4A4], (4A2), (7A4), (7B4) (6A4)	IOM1*	(3A1), (3A2)	OUT11*	(4B3), (6B1)
ADCRY*	(3B1)	DMAON*	[4A4], (3B3), (7A4), (7B4) (1B4)	IOM2*	(3A1), (3A2), (3A4)	060X	[3A3], (3A4), (7A4) (7B4)
ADCØØ*	(7A1)	DMAP	[4A4], (4B1), (7B4)(7B4)	IOM3*	(3A1), (3A4)	060X*	[3A2], (3A4)
ADCØ1*	(7A1)	DMAP*	[4A3] (7A4), (7A4) (1A4)	IOM4*	(3A2), (3A1), (3A4)	061X	[3A3] (4B3), (6A2)
ADCØ2*	(7B1)	DMAR*	[4B1]	IOM5*	(3A1), (3A2), (3A4)	063X	[3A3], (6B1), (6B1)
ADCØ3*	(7B1)	INTR*	[4B1], [6A3], [4A4]	IOM6*	(3A1), (3A4)	PCP1	[5B3], (3A4), (3B3), (4B3) (5B2), (7A4), (7A4)
ADCØ4*	(7A2)	ESKPR*	[5B3]	IOM7*	(3A1)	PCP1*	(7A4), (5B3), (4B2), (4B1)
ADCØ5*	(7A2)	ESMFØ*	[4A3] [1B4]	IOM8*	(3A1)	PCP2*	(5B1), (7A4)
ADCØ6*	(7B2)	ESMF1*	[4B3] [1B4]	IONA*	(4B1)	PCP3*	(5B2), (4B2)
ADCØ7*	(7B2)	EXGO*	(4B2)	IONL*	(6A2)	PCP3	[5B2], [4B3], (3B3) (5B3)
ADCØ8*	(7A3)	EXTK*	[3A4]	IO74*	(3A1)	PULL2	(4A2), (4B3), (6A1), (2B2) (2A4), (5B1), (5B3)
ADCØ9*	(7A3)	EXTØØ*	[7B4] (1A4)	MRDY*	(4B4)	PULL5	(5B2), (5B3), (7B3), (3B4)
ADC1Ø*	(7B3)	EXTØ1*	[7B4] (1A4)	MX0	[4A2], (2A3), (2A4), (7A1)	PULL7	(4A4), (4B1), (4A4), (6B2) (6A4), (6A4)
ADC11*	[7B3] (1B4)	EXTØ2*	[7A4]	MX1	[4A3], (2A3), (2A4), (7A1)	PULL9	(4B4) (3B2), (4B4), (6B1) (7A1), (6A4)
ADC12*	[7A1]	EXTØ3*	[7A4]	MX2	[4A3], (2A3), (7B1)	SCAN	[2B4], (4A1), (2A4), (2B2)
	[4A4]	EXTØ4*	[7B3]	MX3	[4A3], (2A3), (7B1)	SDDMA*	[4A3]
ATR1*	[3B2]	EXTØ5*	[7B3]	OUTØØ*	(4B2), (5A1), (5A3)	STCLR*	(2B4), (2A4), (6A1), (5B2) (3B1)
BMO	[4B3], (4B1), (4A2), (4A4), (4A3), (6B1), (7A4), (7B4) (7B4), (7B4),	EXTØ6*	[7A3]	OUTØ1*	(4B2), (5A1), (5A3), (6B2)	SWFF	[2A4], (4B1), (7A3)
BMØ*	[4B3], (3A2), (4A3), (7B4)	EXTØ7*	[7A3]	OUTØ2*	(5A1), (5A3), (6B2)	750X	[3A2], (5B1), (5B3)
BM1	[4B3], (4A3), (4A2), (6A4) (7A4), (7B4), (7B4)	EXTØ8*	[7B2]	OUTØ3*	(3A3), (5A1), (5A3), (6B2)	750X*	[3A1], (3A4), (5B1)
BM1*	[4B3], (3A2), (4A2), (4A4)	EXTØ9*	[7B2]	OUTØ4*	(3A3), (5A1), (5A3), (6B1)	751X	[3A2], (5B2), (5B3)
BPH1	[4A4], (7B4), (4A1)	EXT1Ø*	[7A2]	OUTØ5*	(3A3), (5A1), (5A3), (6B1)	752X	[3A2], (3A4), (3B3), (7A4) (7A4)
CLADC*	[3B4] (3B1), (4B4)	EXT11*	[7A2]	OUTØ6*	(4B2), (5A1), (5A3), (6B1)	752X*	[3A1], (3A4)
CT	(6B3)	INTP*	(4B3)	OUTØ7*	(4B2), (5A1), (5A3), (6B1)	100KC	[4A1], (6A3), (6B3)
DIN*	[3A4], (4A4)	INTR*	[4B1], [6A3], [4A4]	OUTØ8*	(4B3), (5B1), (5B3), (6B1)		
				OUTØ9*	(4B3), (5B1), (5B3), (6B1)		

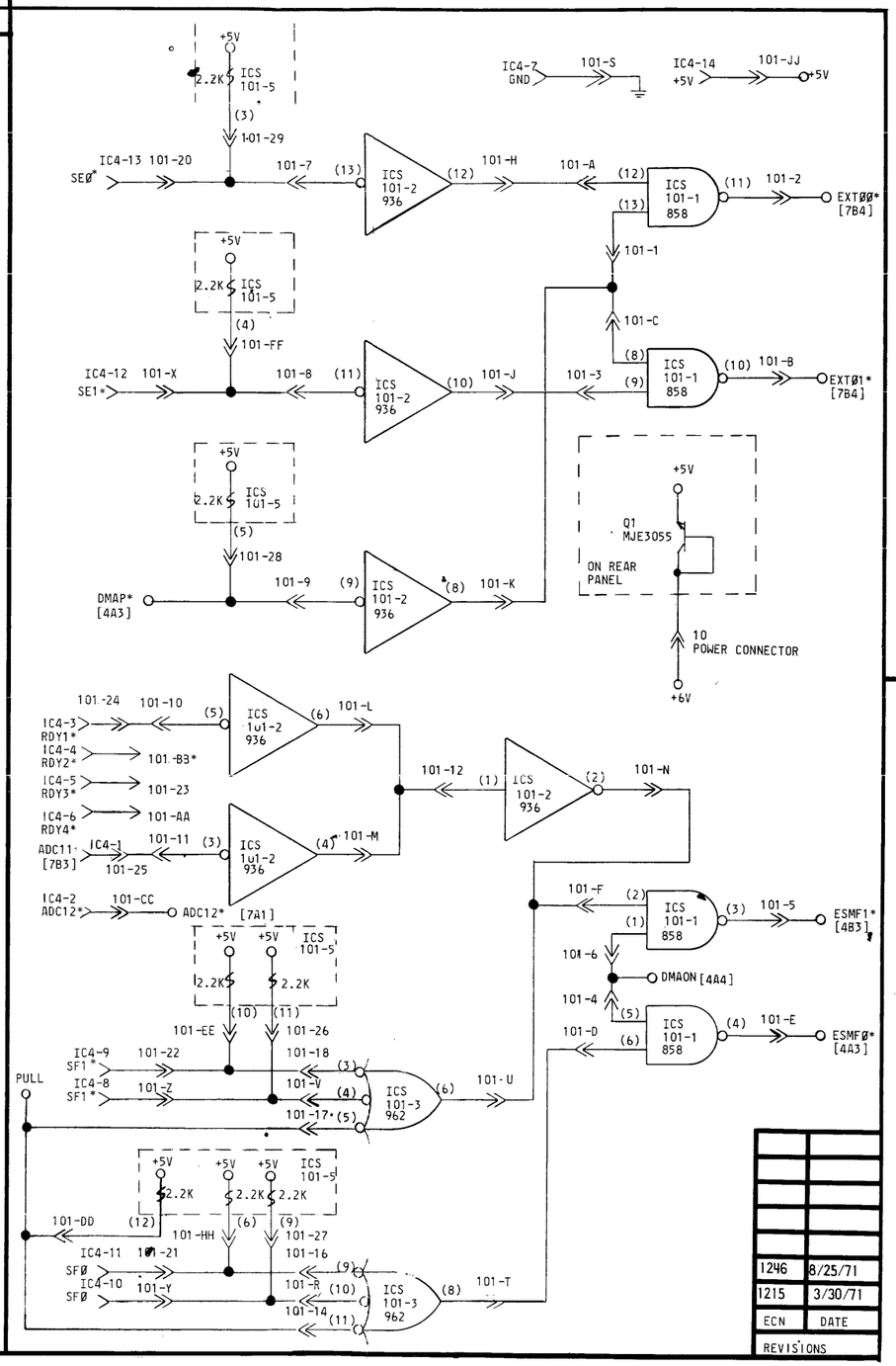


Figure 7-2. ND4410 System Diagram, Signal Destinations (Sheet 1 of 11)

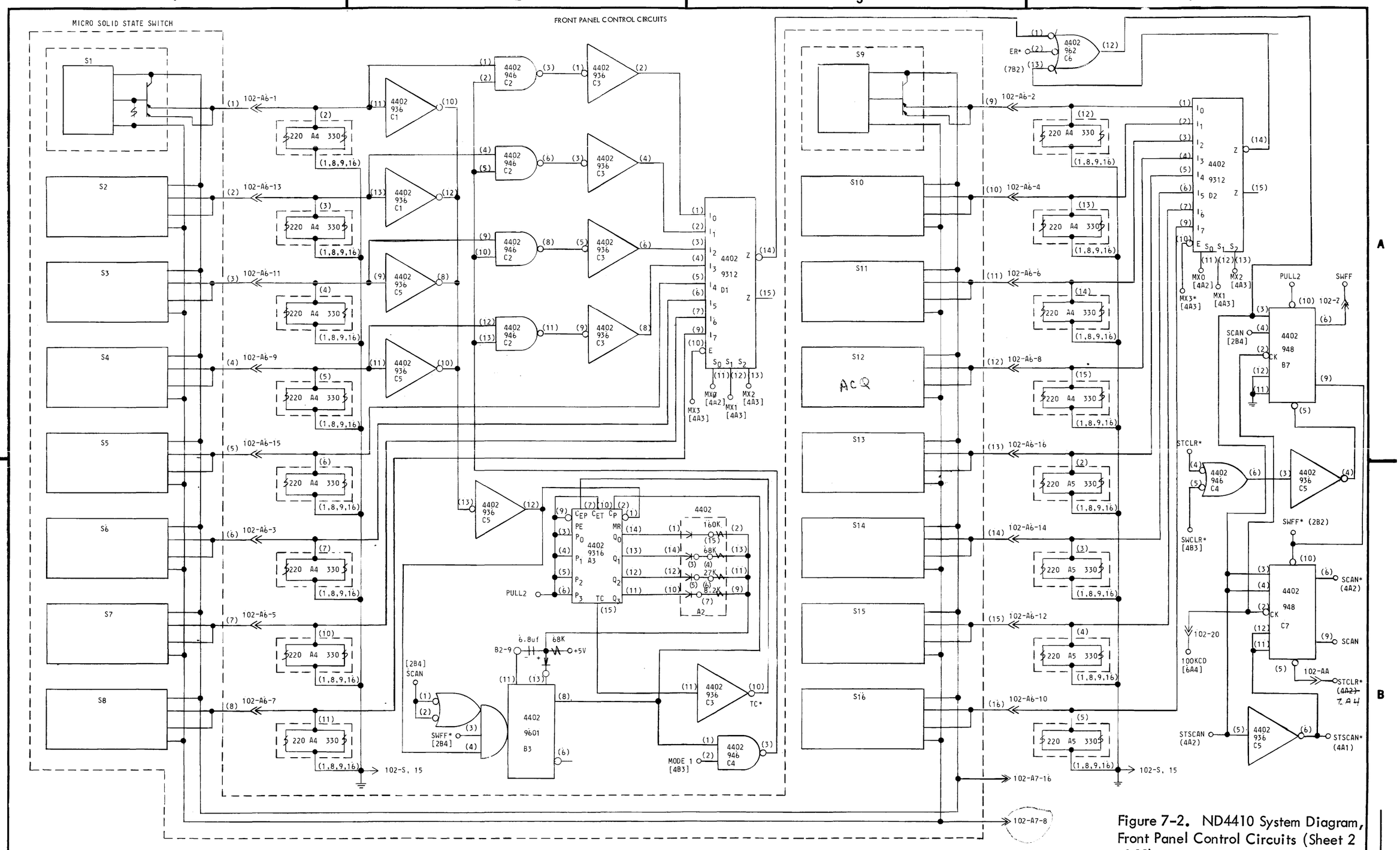


Figure 7-2. ND4410 System Diagram, Front Panel Control Circuits (Sheet 2 of 11)

7-5/7-6

PENDING ECN

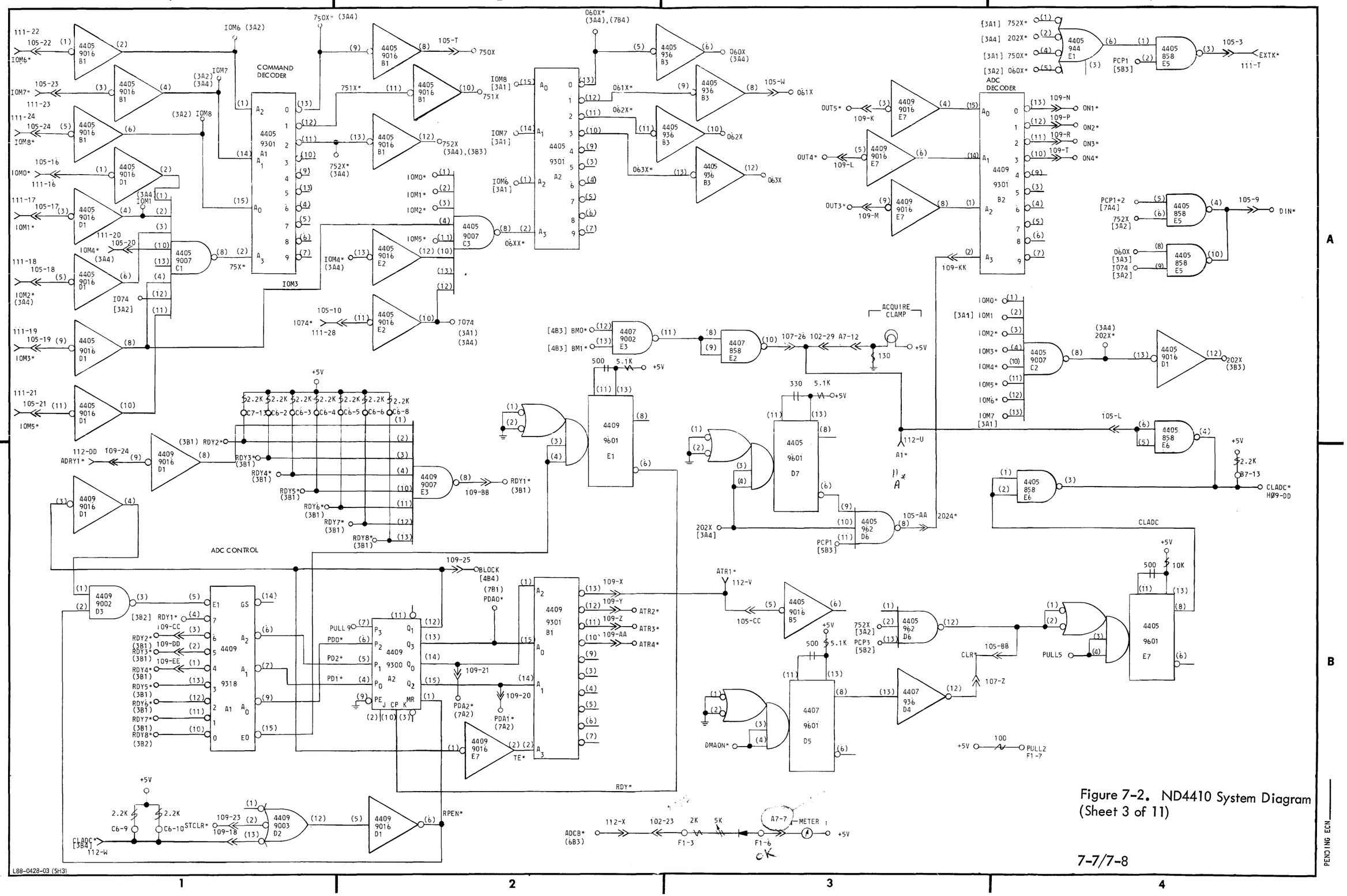


Figure 7-2. ND4410 System Diagram (Sheet 3 of 11)

7-7/7-8

L88-0428-03 (SH3)

PENDING ECN

PUSHBUTTON DECODE CIRCUITS

DIRECT MEMORY ACCESS CONTROL CIRCUITS

MULTIPLE INTERRUPT AND MODE INDICATOR REGISTER

MEMORY FIELD AND ACQUISITION MODE DECODER

Figure 7-2. ND4410 System Diagram (Sheet 4 of 11)

L88-0428-06 (SH4)

HORIZONTAL DISPLAY CIRCUITS

DEC-K 70-1737

VERTICAL DISPLAY CIRCUITS

DEC-K 70-1737

BLANKING CIRCUIT

NOTE:
FOR 1208B SCOPE
MOVE WIRE TO PIN 9
OF D4 AND DISCONNECT
WIRE FROM PIN 6 OF D4.

PLOT CONTROL CIRCUITS

MARKER CIRCUIT

MARKER/PLOTTER SKIP REQUEST CIRCUIT

Figure 7-2. ND4410 System Diagram (Sheet 5 of 11)

7-11/7-12

L88-0428-04 (SH5)

PENDING ECN 1223

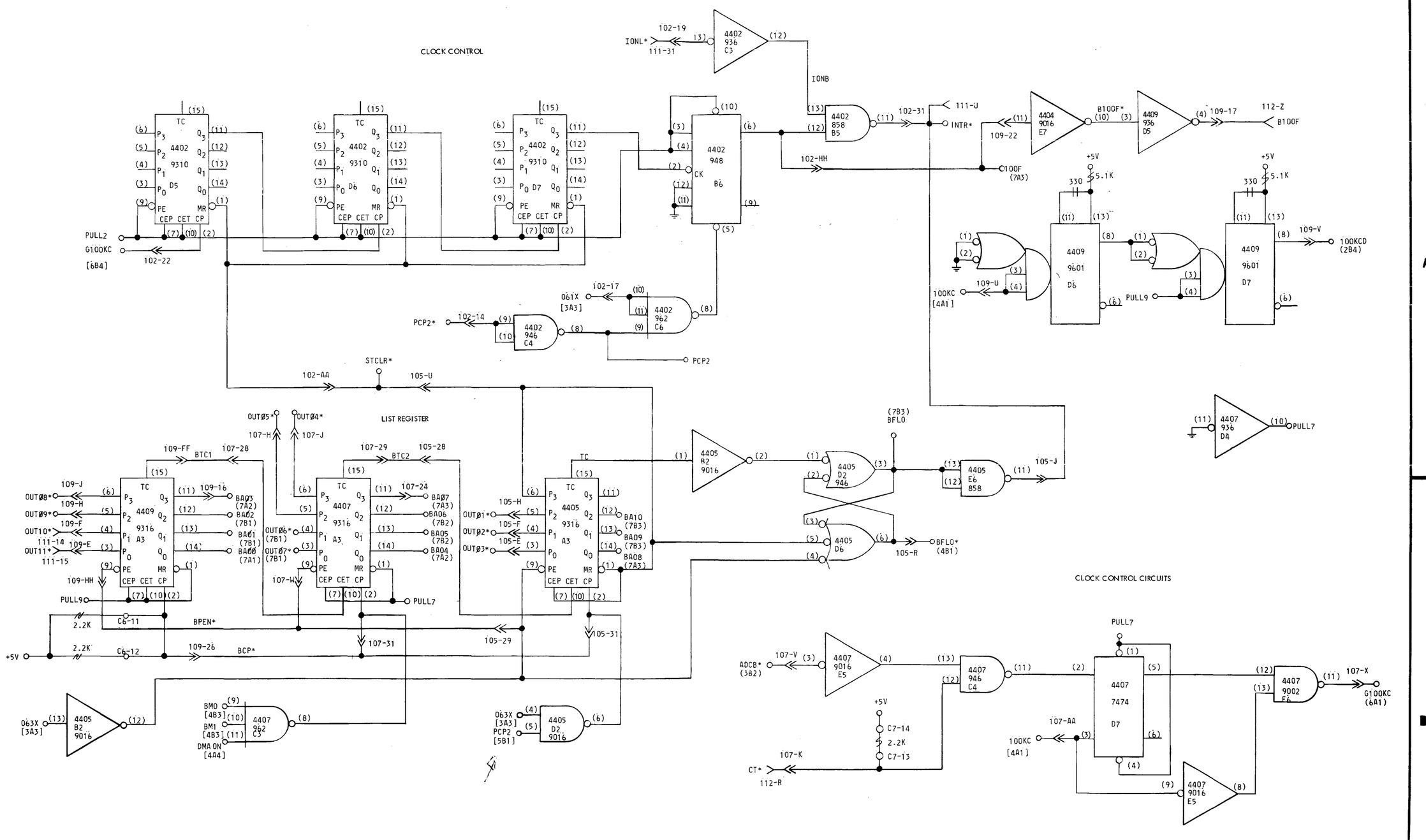


Figure 7-2. ND4410 System Diagram (Sheet 6 of 11)

L88-0428-03 (SH6)

PENDING ECN

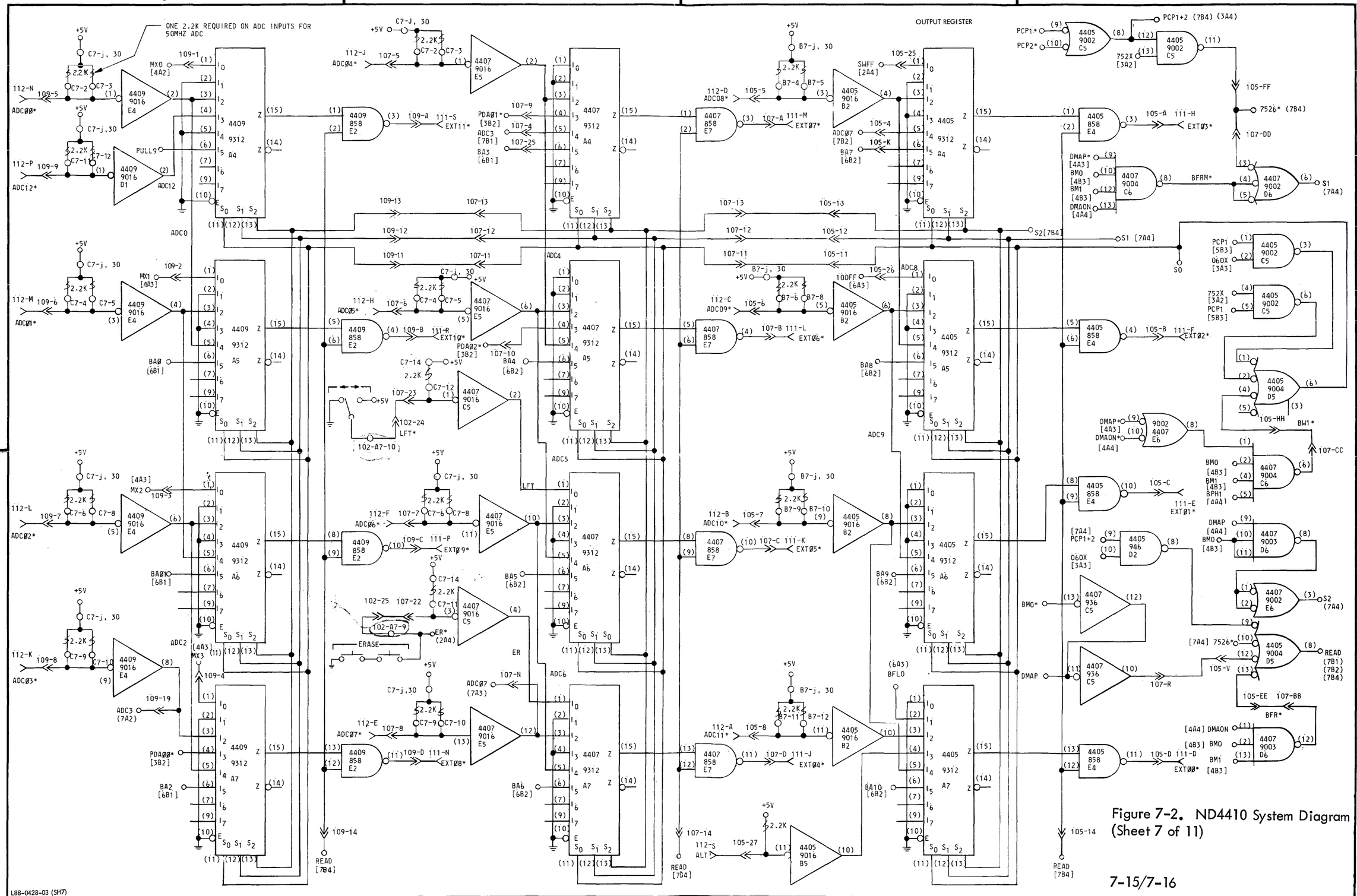
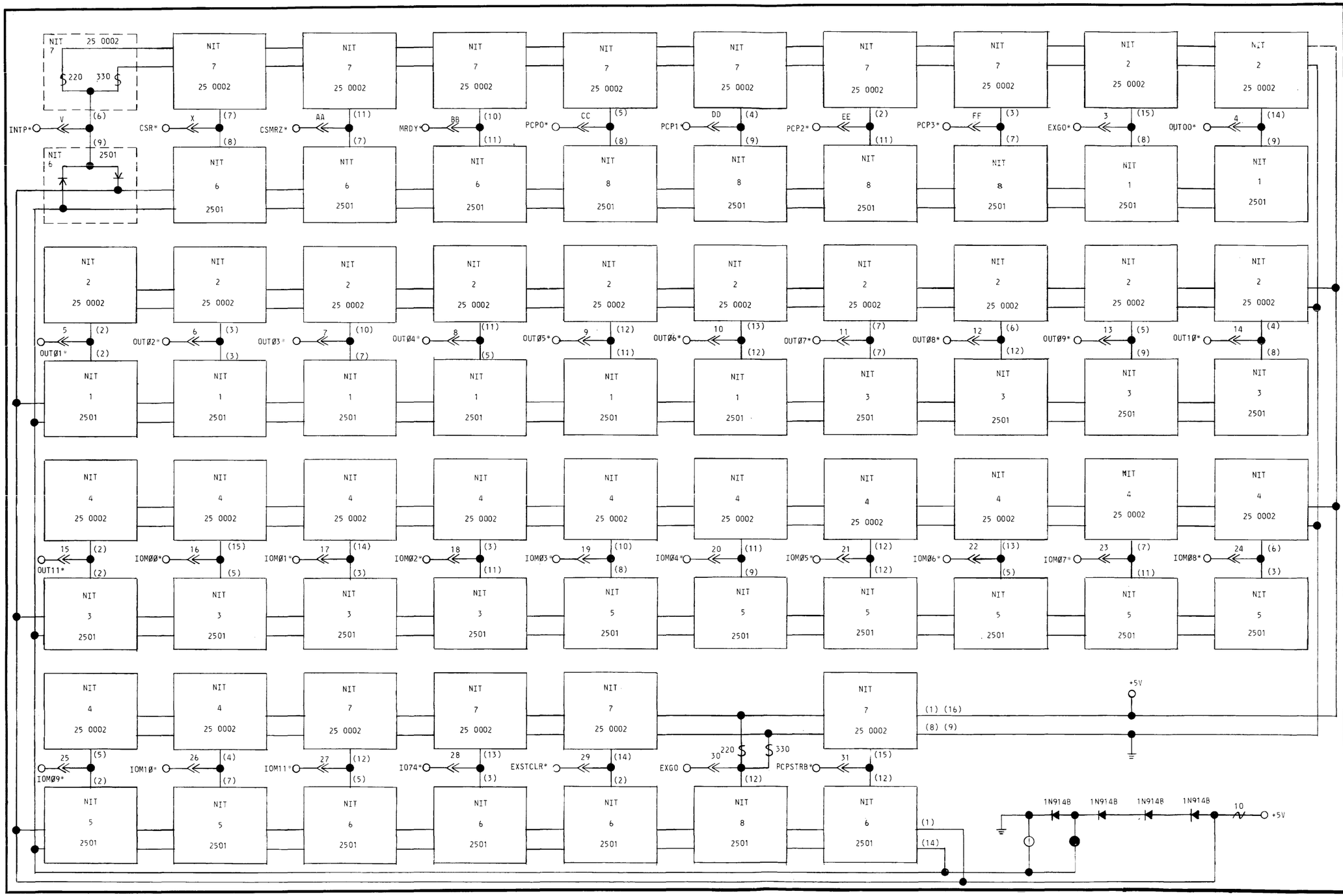


Figure 7-2. ND4410 System Diagram (Sheet 7 of 11)

7-15/7-16

L88-0428-03 (SH7)

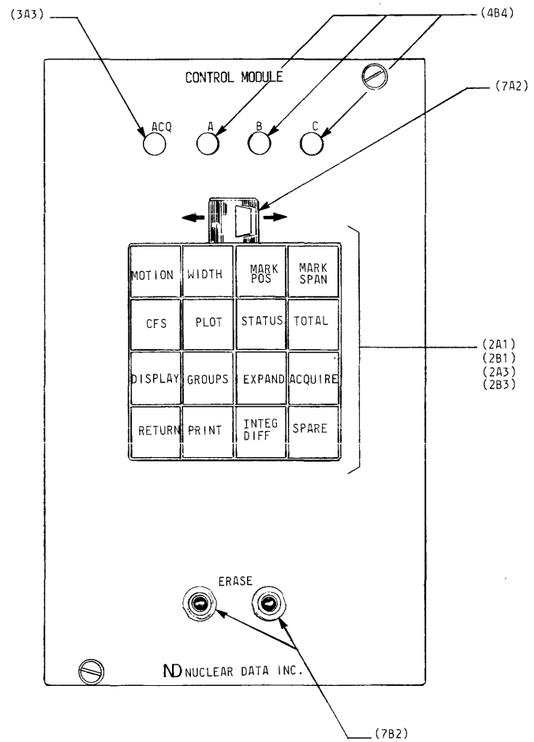
PENDING ECN

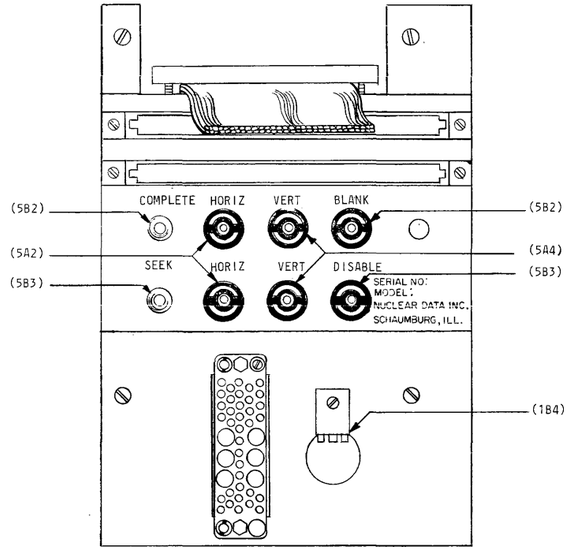


CONNECTOR	
PIN	SIGNAL
A	D.C. COMMON
B	+5V
C	
D	
E	
F	
H	
J	
K	
L	
M	
N	
P	
R	
S	
T	
U	
V	INTP*
W	
X	CSP*
Y	
Z	
a	CSMRZ*
b	MRDY*
c	PCPØ*
d	PCP1*
e	PCP2*
f	PCP3*
h	
j	
k	
1	D.C. COMMON
2	+5V
3	EXGO*
4	OUTØØ*
5	OUTØ1*
6	OUTØ2*
7	OUTØ3*
8	OUTØ4*
9	OUTØ5*
10	OUTØ6*
11	OUTØ7*
12	OUTØ8*
13	OUTØ9*
14	OUT1Ø*
15	OUT11*
16	IOMØØ*
17	IOMØ1*
18	IOMØ2*
19	IOMØ3*
20	IOMØ4*
21	IOMØ5*
22	IOMØ6*
23	IOMØ7*
24	IOMØ8*
25	IOMØ9*
26	IOM1Ø*
27	IOM11*
28	IO74*
29	EXSTCLR*
30	EXGO
31	PCPSTRB*

Figure 7-2. ND4410 System Diagram (Sheet 8 of 11)

PENDING ECN





ECN	DATE
1326	3-24-72
1246	9-7-71
1223	5-18-71
N/A	———

REVISIONS

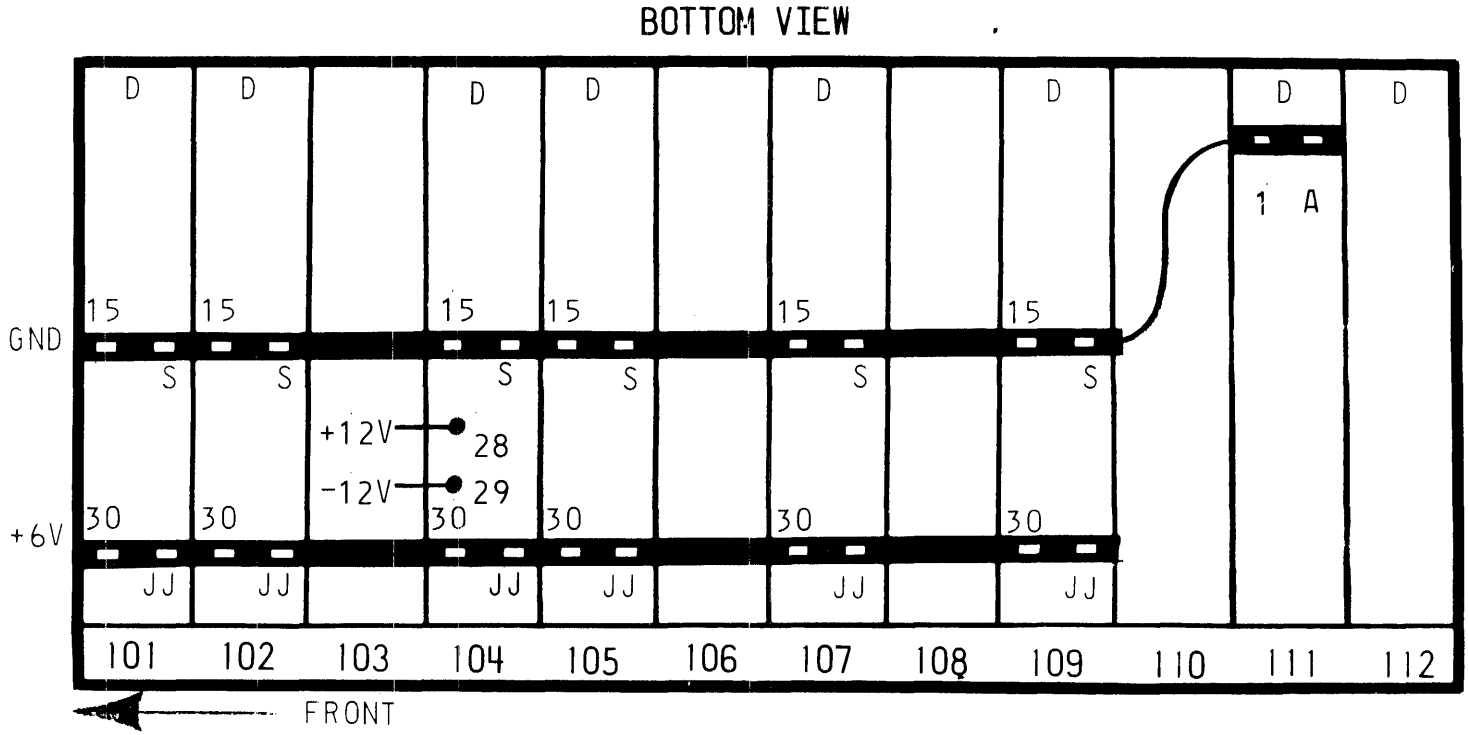
Figure 7-2. ND4410 System Diagram
(Sheet 9 of 11)

7-19/7-20

PENDING ECN

L88-0428-03 (SH9)

NOTES:
1 - "D" DENOTES DOUBLE CONNECTOR.
2 - "S" DENOTES SINGLE CONNECTOR.



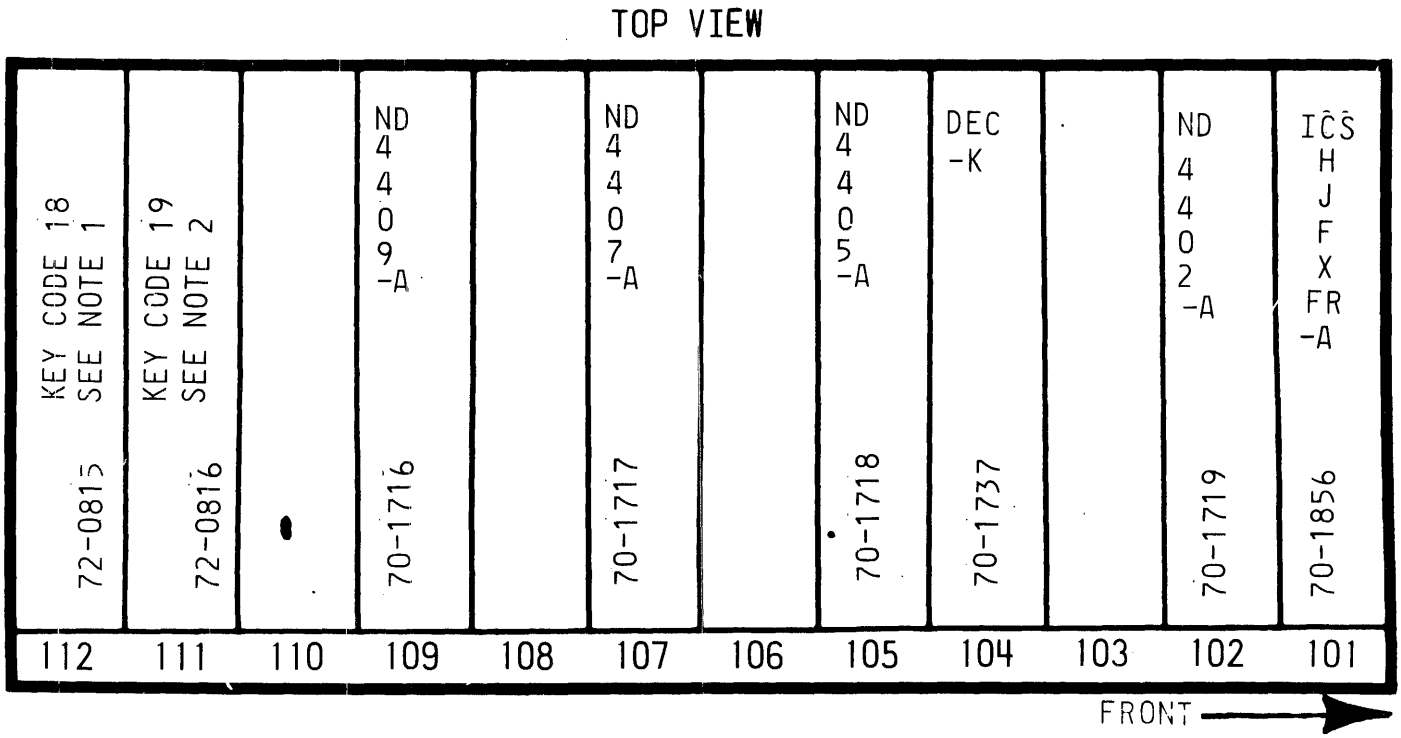
L88-0428-00 (SH10)

Figure 7-2. ND4410 System Control Bussing Diagram (Sheet 10 of 11)

NOTES:

1. 75-0009 CBL ADC CNT MODULE KEY AS REQ.

2. 75-0008 CBL COMPUTER 86-62 STACK KEY 62
   PIN CON. AS REQ.



L88-0428-02 (SH11)

Figure 7-2. ND4410 System Control Loading Diagram (Sheet 11 of 11)

NUCLEAR DATA INC.

Nuclear Data Inc.
P. O. Box 451
100 West Golf Road
Palatine, Illinois 60067
Tel: (312) 529-4600

Nuclear Data Inc.
103 Pincushion Road
Framingham, Massachusetts 01701
Tel: (617) 899-4927

Nuclear Data Inc.
P. O. Box 2192
14278 Wicks Boulevard
San Leandro, California 94577
Tel: (415) 483-9200

Nuclear Data Inc.
2335 Brannen Road, S.E.
Atlanta, Georgia 30316
Tel: (404) 241-3220

Nuclear Data, GmbH
Mainzerlandstrasse 29
6 Frankfurt/M, Germany
Tel: 23 11 44

Nuclear Data Inc. (U.K.)
Rose Industrial Estate
Cores End Road
Bourne End, Bucks., England
Tel: 22733

Nuclear Data (Ireland) Ltd.
Kinsale Road, Ballycurreen
P. O. Box #23
Cork, Ireland
Tel: 22137

Nuclear Data (Scandinavia)
Division of Selektronik A/S
Hammervej 3
2970 Hørsholm, Denmark
Tel: (01) 86 30 00