NCR 5385E/5386 SCSI Protocol Controller User's Guide

NCR

Microelectronics Division, Colorado Springs

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SECTION 1
GENERAL INFORMATION

The NCR SCSI Protocol Controller is capable of operating as either an Initiator or a Target, and can therefore be used in host adapter and control unit designs. The purpose of this manual is to assist the user in the design of these SCSI bus devices.

Sections 2 through 5 discuss the software required to control the device. Sample flowcharts and step-by-step walk-through's demonstrate the required routines for both the Initiator and Target roles. Additionally, the interrupt service routines presented in Section 5 cover all possible interrupting conditions for the Connected as Initiator, Connected as Target and Disconnected states.

Section 6 describes the inteface required between the NCR 5385E/86 and SCSI bus for both Single-Ended and Differential-Pair operation, and provides sample schematics for each.

This design manual is not an SCSI specification and assumes some prior knowledge of the SCSI proposed standard. Copies of the proposed standard may be obtained, with a pre-payment of $20, from:

X3 Secretariat, Computer and Business Equipment
Manufacturers Association
311 First Street, NW, Suite 500
Washington, D.C. 20001

Please include a self-addressed mailing label.

1.1 ADDITIONAL DOCUMENTATION

Other documents which may be useful are:

- NCR 5385 SCSI Protocol Controller Data Sheet (MC-704)
- NCR 5380 SCSI Interface Chip Design Manual
- SCSI Engineering Notebook

These documents may be obtained from your local NCR Microelectronics sales representative or from:

NCR Microelectronics
Logic Products Marketing
1635 Aeroplaza Drive
Colorado Springs, CO 80916
(800) 525-2252 or
(303) 596-5612

SECTION 2
INITIALIZATION

The three steps typically performed after the NCR SCSI Protocol Controller is reset are presented below. It is assumed that no errors occur.

1. Loop on reading the Diagnostic Status Register until the Self-Diagnostic Complete bit is on. (This should occur within 350 clock cycles after the reset pulse goes inactive or after the write pulse for a Chip Reset command.) Never attempt to read the Diagnostic Status Register while Reset is active, as the data bus is in an unknown state and the Self-Diagnostic Complete bit may appear asserted.

2. Check the Diagnostic Command Status and Self-Diagnostic Status bits of the Diagnostic Status Register for all zeros (no errors).

   (At this point, the user may wish to perform other tests such as loading an invalid command, performing the Diagnostic Data Turnaround, etc.)

3. Load the Control Register with the desired information (Parity Enable, Reselect Enable, Select Enable).

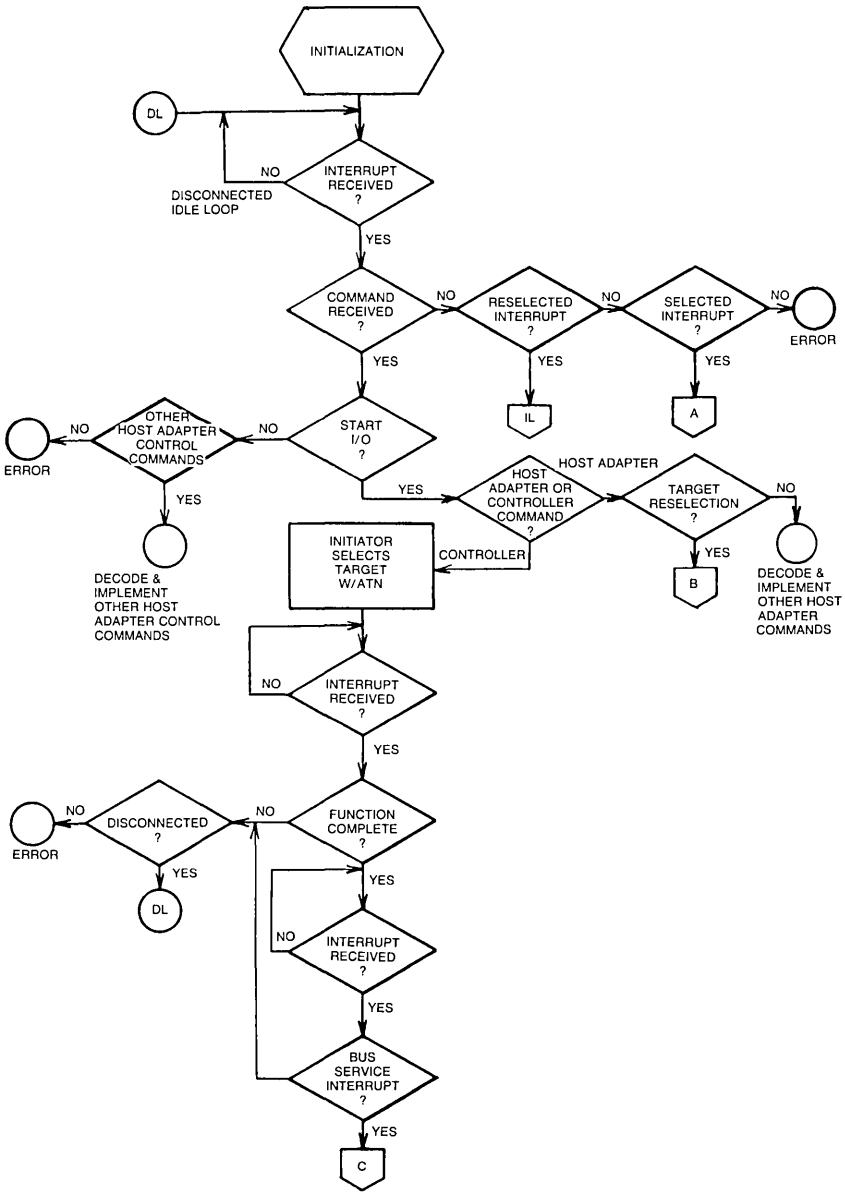
It should be noted that immediately following step 3, the chip is in the Disconnected state. If the Reselect Enable or Select Enable bits are enabled, an interrupt can occur prior to issuing any commands to the NCR SCSI Protocol Controller. A Reselection or Selection interrupt may also occur even after issuing a Select or Reselect command to the chip. In this case, a higher priority device wins arbitration and selects or reselects the chip, generating a Selected or Reselected interrupt rather than a Function Complete Interrupt. The user must wait until the chip is in the Disconnected state before reissuing the Select or Reselect command.

For more information concerning Initialization, please refer to Section 7 of the NCR 5385 SCSI Protocol Controller Data Sheet (Publication # MC-704), and to Section 7, Device Note 5 of this document.

SECTION 3
INITIATOR ROLE

The Initiator Role is normally associated with the host adapter, but may also be assumed by a tape controller performing a disk back-up operation. After selecting a Target device, the Initiator must respond to the Information Transfer Phases controlled by the Target. Please refer to the latest revision of the draft proposed SCSI standard for a complete description of the Initiator Role.

The following partial flowchart illustrates the role of the SCSI bus Initiator. (Note that the Target portion of this flowchart appears in Section 4, "Target Role," and that the flow chart is presented in its entirety in Appendix C.)



3.1 INITIATOR ROLE FLOWCHART

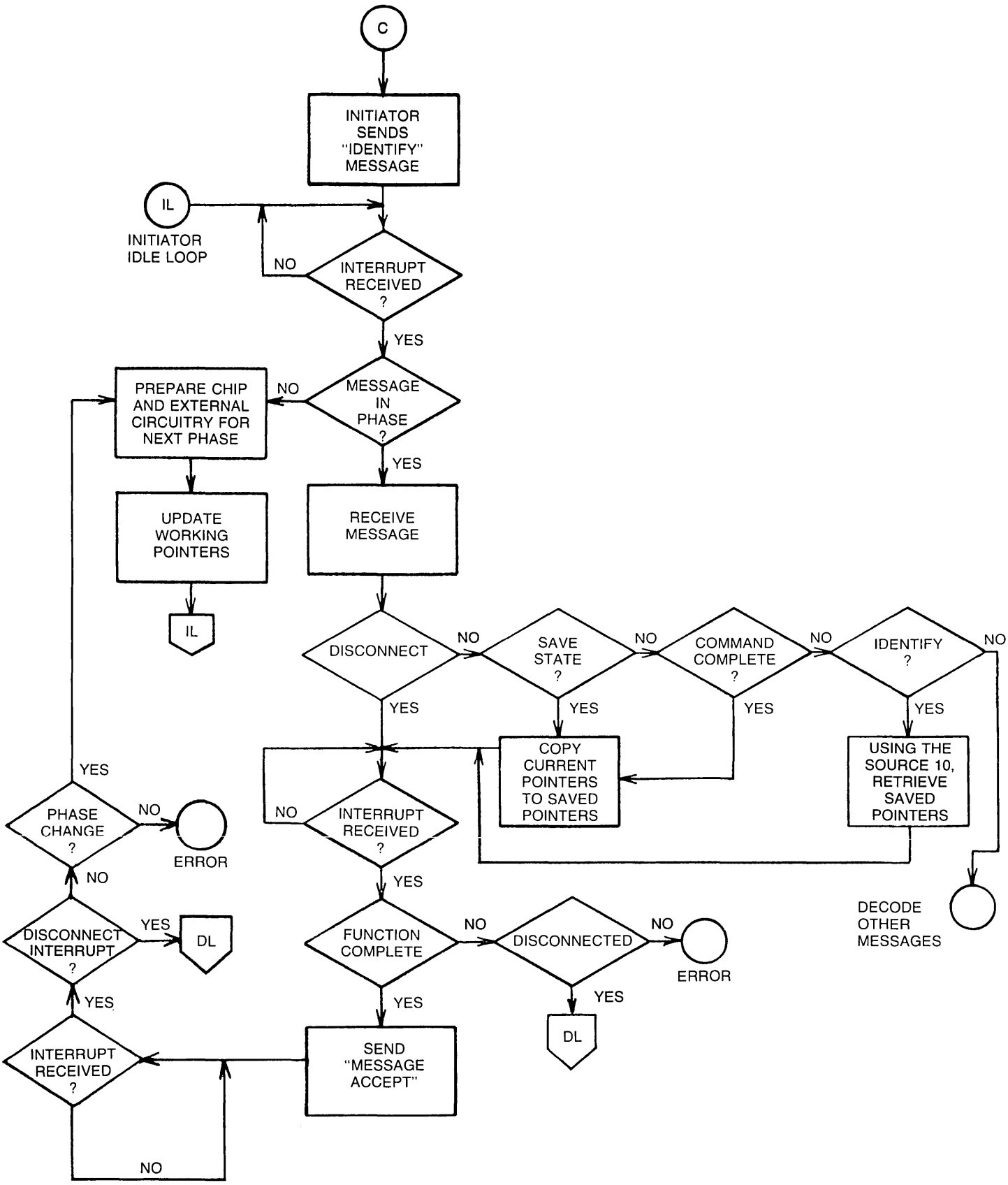


FIGURE 3.1 INITIATOR ROLE (Concluded)

3.1 INITIATOR ROLE WALKTHROUGH

This sample walkthough outlines the steps typically required to perform a complete I/O function as an Initiator. It is assumed that both the Initiator and Target can handle messages and are able to disconnect and reconnect during the function. To simplify this example, it is further assumed that no errors or exceptions occur during the entire operation.

Note that the steps are grouped under headings that describe the function each group accomplishes.

INITIATOR SELECTS TARGET

1. Load the Destination ID Register with the Target's ID.
2. Load the Transfer Counter to program the selection timeout. Write to each of the three 8-bit registers.
3. Load the Command Register with SELECT W/ATN.
4. Wait for an interrupt.
5. Read the Auxiliary Status Register.
6. Read the Interrupt Register.
7. Check for a Function Complete interrupt. (This indicates the SELECT W/ATN was successful.)

(The NCR 5385 SCSI Protocol Controller is now in the Connected as Initiator state.)

INITIATOR SENDS "IDENTIFY" MESSAGE

8. Wait for an interrupt.
9. Read the Auxiliary Status Register.
10. Read the Interrupt Register.
11. Check the interrupt. A Bus Service interrupt should have occurred, indicating that the Target has initiated an information transfer.
12. Check the I/O, C/D, and MSG bits read from the Auxiliary Status Register. The Target should be requesting a Message Out phase to receive the "Identify" message.
13. Load the Command Register with a Transfer Info command. Since the "Identify" message is a single byte, program the Single Byte Transfer bit ON ("1") and the DMA Mode bit OFF ("0").
14. Read the Auxiliary Status Register.
15. Check the Data Register Full bit.
16. Repeat steps (14) and (15) until Data Register Full is OFF ("0").
17. Write the "Identify" message into the Data Register.
18. Wait for an interrupt.
19. Read the Auxiliary Status Register.
20. Read the Interrupt Register.
21. Check the interrupt. Another Bus Service interrupt should have occurred, indicating that the Target has again changed the bus phase.

INITIATOR RECEIVES "DISCONNECT" MESSAGE

(Note that the Target is not required to send a "Disconnect" message and disconnect at this point. It may request the command before disconnecting, or not

disconnect at all. If the Target does not issue the message, proceed to step 65.

22. Check the I/O, C/D, and MSG bits read from the Auxiliary Status Register. The Target should be requesting a Message In phase.
23. Load the Command Register with a Transfer Info command. The Single Byte Transfer bit should be ON ("1"), and the DMA Mode bit OFF ("0").
24. Read the Auxiliary Status Register.
25. Check the Data Register Full bit.
26. Repeat 24 and 25 until Data Register Full is on.
27. Read the Data Register.
28. Check the message. The Target should have sent a "Disconnect" message, indicating that it will reconnect later to complete the I/O function.
29. Wait for an interrupt. (Note that a Function Complete interrupt may occur at any time after the Transfer Info command is loaded (step 23). To provide for its occurrence during steps 24 through 28, it is suggested that the user set an interrupt flag in the interrupt service routine, mask any other interrupts, and then complete steps 24 through 28.) If a Disconnect interrupt occurs, it must be serviced immediately.
30. Read the Auxiliary Status Register.
31. Read the Interrupt Register.
32. Check the interrupt. A Function Complete should have occurred, indicating that the last byte of the message has been received. ACK is left active so that ATN may be asserted if the message needs to be rejected.
33. Load the Command Register with a Message Accepted command.

INITIATOR AWAITS DISCONNECTION

34. Wait for an interrupt.
35. Read the Auxiliary Status Register.
36. Read the Interrupt Register.
37. Check the interrupt. The Target should have disconnected, causing a Disconnect interrupt.

(The NCR 5385 SCSI Protocol Controller is now in the Disconnected state and may start or handle I/O functions for any other logical unit. For this I/O function to continue, the user must wait until the chip is reselected by the Target while in the disconnected state. Step 38 continues the flow.)

INITIATOR IS RESELECTED

38. Wait for an interrupt.
39. Read Auxiliary Status Register.
40. Read Interrupt Register.
41. Check the interrupt. Assuming the Target has reselected the NCR SCSI Protocol Controller to continue the function, a Reselect Interrupt should have occurred.

(The user is now in the Connected as Initiator state.)

INITIATOR RECEIVES "IDENTIFY" MESSAGE

42. Wait for an interrupt.

43. Read the Auxiliary Status Register.
44. Read the Interrupt Register.
45. Check the interrupt. A Bus Service interrupt should have occurred, indicating that the Target has activated REQ for an information transfer.
46. Check the I/O, C/D, and MSG bits read from the Auxiliary Status Register. The Target should be requesting a Message In phase to identify the I/O.
47. Load the Command Register with a Transfer Info command (Single Byte Transfer = 1, DMA Mode = 0.)
48. Read the Auxiliary Status Register.
49. Check the Data Register Full bit.
50. Repeat 48 and 49 until Data Register Full is ON ("1").
51. Read the Data Register.
52. Check the message. The Target should have sent an "Identify" message which contains the logical unit number for the I/O.
53. Read the Source ID Register.
54. Check the contents of the Source ID Register to determine which device did the reselection.
55. Having identified the device and logical unit number, retrieve the command, data and status pointers for this I/O, and store them in a working pointer area outside the NCR 5385 chip.
56. Wait for an interrupt. (Note that a Function Complete interrupt may occur at any time after the Transfer Info command (step 47). To provide for its occurrence during steps 48 through 55, it is suggested that the user set an interrupt flag in the interrupt service routine, mask any further interrupts, and then complete steps 48 through 55.) If a Disconnect interrupt occurs, it must be serviced immediately.
57. Read the Auxiliary Status Register.
58. Read the Interrupt Register.
59. Check the interrupt. A Function Complete should have occurred, indicating that the last byte of the message has been received. ACK is left active so that ATN may be asserted if the message needs to be rejected.
60. Load the Command Register with a Message Accepted command.

INITIATOR TRANSFERS COMMAND, DATA, OR STATUS

61. Wait for an interrupt.
62. Read the Auxiliary Status Register.
63. Read the Interrupt Register.
64. Check the interrupt. A Bus Service interrupt should have occurred, indicating that the Target has initiated another information phase.
65. Check the I/O, C/D, and MSG bits read from the Auxiliary Status Register. The Target should be requesting a Command, Data, or Status phase.
66. Prepare circuitry external to the chip for the

requested transfer by using the appropriate working pointer.

67. Load the Transfer Counter for the maximum number of bytes to be transferred. Write to each of the three 8-bit registers. (This step is omitted for a Single Byte Transfer.)
68. Load the Command Register with a Transfer Info command. Normally, for command or data transfers, Single Byte Transfer = 0 and DMA Mode = 1. (For status, these bits might be 1 and 0, respectively.)
69. If Single Byte Transfer = 0, go to step 74.
70. Read the Auxiliary Status Register.
71. Check the Data Register Full bit.
72. Repeat 70 and 71 until the Data Register Full bit if OFF ("0").
73. Read the Data Register (with status byte).
74. Wait for an interrupt.
75. Read the Auxiliary Status Register.
76. Read the Interrupt Register.
77. Check the interrupt. A Bus Service interrupt should have occurred, indicating that the Target has initiated a different information phase.

INITIATOR UPDATES WORKING POINTER FOR LAST TRANSFER

78. If the last transfer was a single byte, go to step 82.
79. Check the Transfer Counter Zero bit in the Auxiliary Status Register.
80. If Transfer Counter = 0, go to step 82.
81. Read the Transfer Counter.
82. Update the *working* pointer for the last information phase. Note that the stored pointer is not updated at this time. Stored pointers are updated ONLY when a "Save State" or "Command Complete" message is received.

INITIATOR CHECKS NEW PHASE TYPE

83. Check the I/O, C/D, and MSG bits read from the Auxiliary Status Register.
84. If the Target is requesting a Command, Data or Status phase, go back to step 66.

INITIATOR RECEIVES MESSAGE

85. If the Target is requesting a Message In phase, load the Command Register with a Transfer Info command (Single Byte Transfer = 1, DMA Mode = 0).
86. Read the Auxiliary Status Register.
87. Check the Data Register Full bit.
88. Repeat steps 86 and 87 until the Data Register Full is set.
89. Read the message in the Data Register.
90. If the message is "Command Complete," go to step 113.
91. If the message is "Disconnect," go to step 103.

INITIATOR HANDLES "SAVE STATE" MESSAGE

92. In normal operation, the message referred to in step 89 should be "Save State." In this case, the user saves the state of the working pointers by moving them to the stored pointer area.

93. Wait for an interrupt. (Note that a Function Complete interrupt may occur at any time after step 85. To provide for its occurrence during steps 86 through 92, it is suggested that user set an interrupt flag in the interrupt service routine, mask any further interrupts, and proceed to complete steps 86 through 92.) If a Disconnect interrupt occurs, it must be serviced immediately.

94. Read the Auxiliary Status Register.

95. Read the Interrupt Register.

96. Check the interrupt. A Function Complete should have occurred, indicating that the last byte of the message was received. ACK is left active so that ATN may be asserted if the message needs to be rejected.

97. Load the Command Register with a Message Accepted command.

98. Wait for an interrupt.

99. Read the Auxiliary Status Register.

100. Read the Interrupt Register.

101. Check the interrupt. A Bus Service interrupt should have occurred, indicating that the Target has initiated another information phase.

102. Go to step 83.

INITIATOR HANDLES "DISCONNECT" MESSAGE

103. Wait for an interrupt. (Note that a Function Complete interrupt may occur at any time after step 85. To provide for its occurrence during steps 86 through 102, it is suggested that the user set an interrupt flag in the interrupt service routine, mask any further interrupts, and proceed to complete steps 86 through 102.) If a Disconnect interrupt occurs, it must be serviced immediately.

104. Read the Auxiliary Status Register.

105. Read the Interrupt Register.

106. Check the interrupt. A Function Complete should have occurred, indicating that the last byte of the message has been received. ACK is left active so that ATN may be asserted if the message needs to be rejected.

107. Load the Command Register with a Message Accepted command.

INITIATOR AWAITS DISCONNECTION

108. Wait for an interrupt.

109. Read the Auxiliary Status Register.

110. Read the Interrupt Register.

111. Check the interrupt. After sending the "Disconnect" message, the Target should have disconnected, resulting in a Disconnected interrupt.

112. Go to step 38. (The note prior to 38 applies.)

INITIATOR HANDLES "COMMAND COMPLETE" MESSAGE

113. Save the state of the working pointers by moving them to the stored pointer area.

114. Wait for an interrupt. (Note that a Function Complete interrupt may occur at any time after step 85. To provide for its occurrence during steps 86 through 113, it is suggested that the user set an interrupt flag in the interrupt service routine, mask any further interrupts, and complete steps 86 through 113.) If a Disconnect interrupt occurs, it must be serviced immediately.

115. Read the Auxiliary Status Register.

116. Read the Interrupt Register.

117. Check the interrupt. A Function Complete should have occurred, indicating that the last byte of the message has been received. ACK is left active so that ATN may be asserted if the message needs to be rejected.

118. Load the Command Register with a Message Accepted command.

INITIATOR AWAITS DISCONNECTION

119. Wait for an interrupt.

120. Read the Auxiliary Status Register.

121. Read the Interrupt Register.

122. Check the interrupt. After sending the "Command Complete" message, the Target should have disconnected, resulting in a Disconnected interrupt.

(The I/O function is now complete. The user is back in the Disconnected state.)

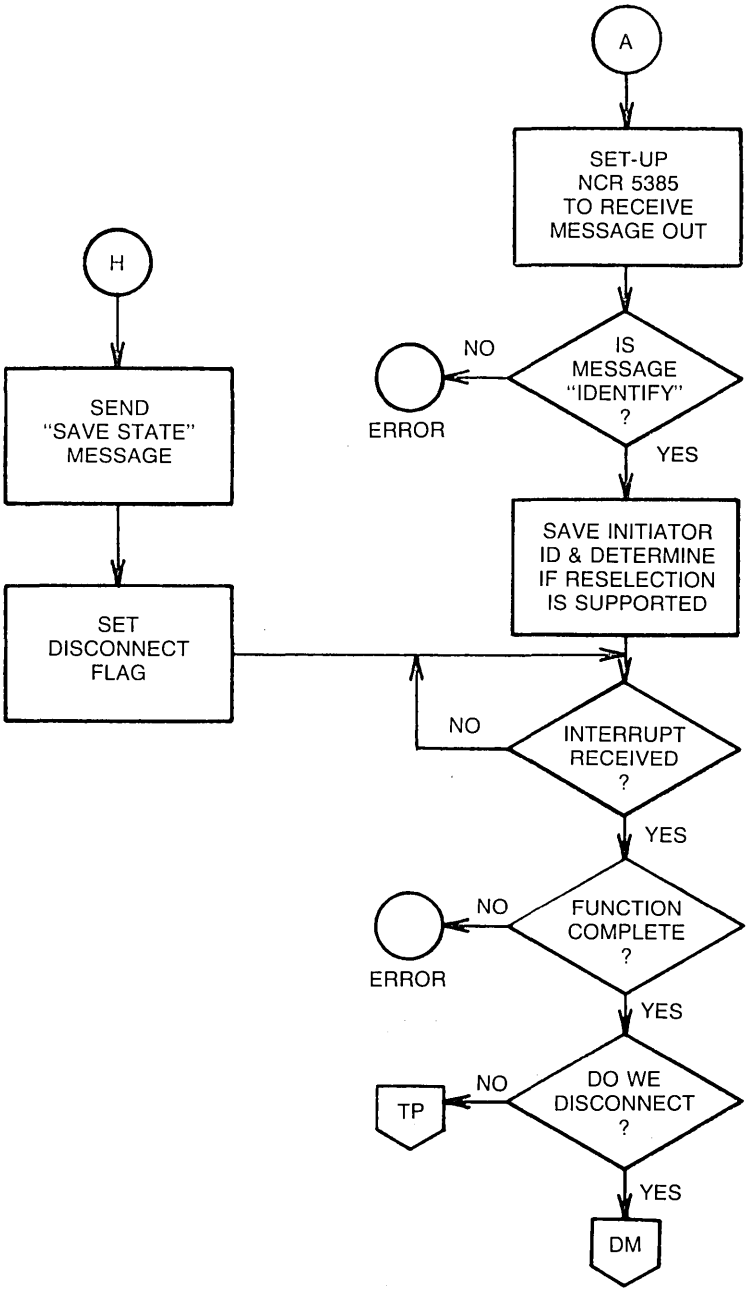
3.2 NOTES

1. Steps 14 through 16, and 70 through 72 can be omitted if the microprocessor guarantees that one full clock cycle elapses between loading the Command Register and loading the Data Register. The act of loading an Interrupting command resets the Data Register Full Status Bit in the Auxiliary Status Register. Therefore, when a command is issued that requires data to be put into the Data Register, data may not be loaded until the Data Register Full Status Bit is allowed to reset.
2. If a Disconnect Command is issued when connected as an Initiator, the Target is left hanging on the bus. A bus reset may be required to free the bus.

SECTION 4
TARGET ROLE

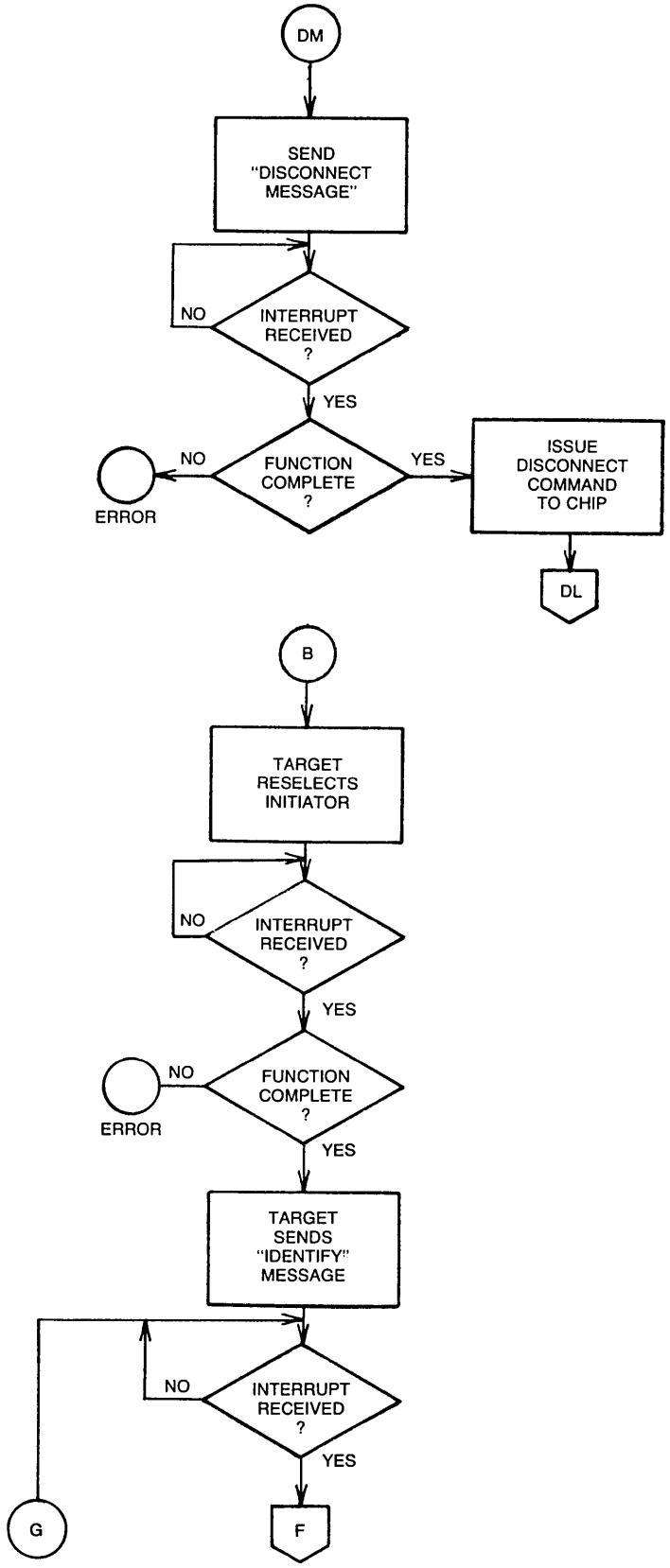
The Target Role, though normally performed by a peripheral, may also be assumed by the host adapter during host-to-host communications. When selected, the Target controls the bus activity by driving the C/D, I/O, and MSG signals. Please refer to the latest draft proposed SCSI standard for a complete description of the Target Role.

The following partial flowchart illustrates the role of the Target on the SCSI bus. The flowchart in Fig. 4.1 is a continuation of Fig. 3.1 and resumes after the target has been selected. The flowchart of the Initiator and Target Roles is shown in its entirety in Appendix C.

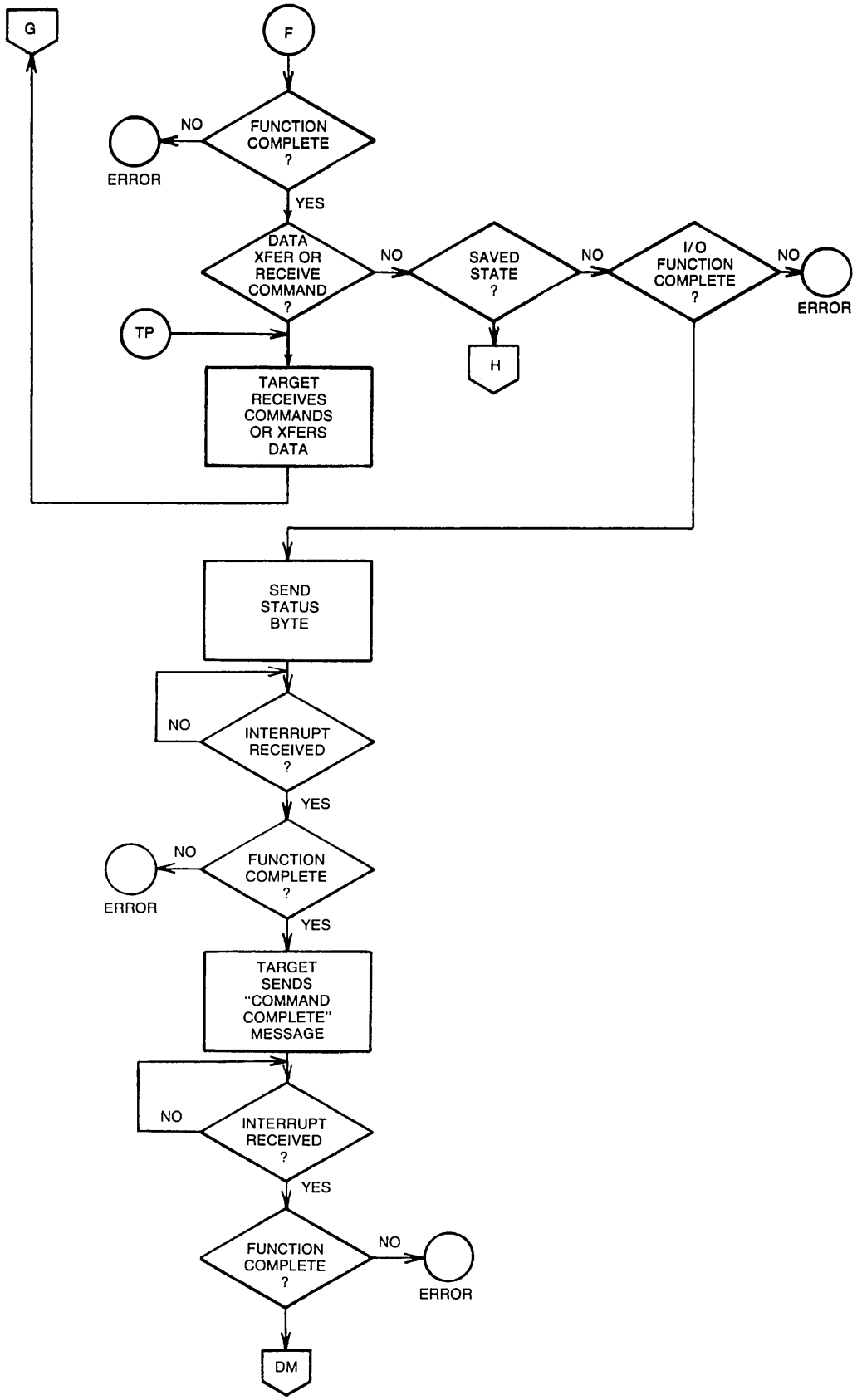


4.1 TARGET ROLE FLOWCHART

4.1 TARGET ROLE FLOWCHART (Continued)



4.1 TARGET ROLE FLOWCHART (Continued)



4.1 TARGET ROLE WALKTHROUGH

This sample walkthrough outlines the steps typically required to perform a complete I/O function as a Target. It is assumed that both the Target and Initiator can handle messages and are able to disconnect. It is also assumed that no errors or exceptions occur during the entire operation. The sequence of steps begins after the chip has been selected as a Target.

Note that the steps are grouped under headings that describe the function each group accomplishes.

TARGET IS SELECTED

1. Wait for an interrupt.
2. Read the Auxiliary Status Register.
3. Read the Interrupt Register.
4. Check the interrupt. Selected and Bus Service interrupts should have occurred, indicating that the chip has been selected as a Target, and the Initiator has asserted the ATN signal, respectively.

(The user is now in the Connected as Target state.)

TARGET RECEIVES "IDENTIFY MESSAGE"

5. Load the Command Register with a Receive Message Out command (Single Byte Transfer = 1, DMA Mode = 0).
6. Read the Auxiliary Status Register.
7. Check the Data Register Full bit.
8. Repeat steps 6 and 7 until Data Register Full bit is ON ("1").
9. Read the Data Register.
10. Check the message. The Initiator should have sent an "Identify" message which indicates whether he can disconnect. The message also contains the logical unit number for the I/O.
11. Read the Source ID Register.
12. Check the ID Valid bit. If the Initiator has the ability to disconnect, it will be ON. (The user now has the Initiator ID and the logical unit number, which uniquely defines an I/O. The user may record this information and disconnect.)
13. Wait for an interrupt. (Note that a Function Complete may occur at any time after step 9. To provide for its occurrence during steps 10 through 12, it is suggested that the user set an interrupt flag in the interrupt service routine, mask any further interrupts, and complete steps 10 through 12.) If a Disconnect interrupt occurs, it must be serviced immediately.
14. Read the Auxiliary Status Register.
15. Read the Interrupt Register.
16. Check the interrupt. A Function Complete should have occurred, indicating that the ID message has completed.

(The user is back in the Connected as Target state. If it is desired not to disconnect at this point, go to step 43.)

TARGET SENDS DISCONNECT MESSAGE AND DISCONNECTS

17. Load the Command Register with a Send

Message In command, (Single Byte Transfer = 1, DMA Mode = 0).

18. Read the Auxiliary Status Register.
19. Check the Data Register Full bit.
20. Repeat steps 18 and 19 until Data Register Full bit is OFF ("0").
21. Write the "Disconnect" message into the Data Register.
22. Wait for an interrupt.
23. Read the Auxiliary Status Register.
24. Read the Interrupt Register.
25. Check the interrupt. A Function Complete interrupt should have occurred, indicating the message was sent successfully.
26. Load the Command Register with a Disconnect command.

(DISCONNECT immediately breaks the connection, and the user is in the Disconnected state. When ready to continue the I/O operation, go to step 27.)

TARGET RESELECTS INITIATOR

27. Load the Destination ID Register with the Initiator's ID.
28. Load the Transfer Counter to program in the reselection timeout. Write to each of the three 8-bit registers.
29. Load the Command Register with a Reselect command.
30. Wait for an interrupt.
31. Read the Auxiliary Status Register.
32. Read the Interrupt Register.
33. Check the interrupt. A Function Complete interrupt should have occurred, indicating that the Reselect was successful.

(The user is now in the Connected as Target state. Note that SCSI protocol requires that the "Identify" Message be sent immediately following the reselection. Therefore, the user should continue with steps 34 through 42.)

TARGET SENDS "IDENTIFY" MESSAGE

34. Load the Command Register with a Send Message In command, (Single Byte Transfer = 1, DMA Mode = 0).
35. Read the Auxiliary Status Register.
36. Check the Data Register Full bit.
37. Repeat steps 35 and 36 until Data Register Full bit is OFF ("0").
38. Write the "Identify" message into the Data Register.
39. Wait for an interrupt.
40. Read the Auxiliary Status Register.
41. Read the Interrupt Register.
42. Check the interrupt. A Function Complete interrupt should have occurred, indicating that the message was sent successfully.

TARGET RECEIVES COMMAND OR TRANSFERS DATA

43. Load the Transfer Counter for a command or data transfer.

44. Load the Command Register with a Receive Command, Receive Data, or Send Data command (Single Byte Transfer = 0, DMA Mode = 1).
45. Wait for an interrupt.
46. Read the Auxiliary Status Register.
47. Read the Interrupt Register.
48. Check the interrupt. A Function Complete interrupt should have occurred, indicating that the transfer was successful.
49. To do a data transfer, go back to step 43.
50. If the I/O function is complete, go to step 62 and continue through step 80. Otherwise, proceed to steps 51 through 61 with the intent of reconnecting later.

TARGET SENDS "SAVE STATE" AND "DISCONNECT" MESSAGES, AND DISCONNECTS

51. Load the Command Register with a Send Message In command, (Single Byte Transfer = 1, DMA Mode = 0).
52. Read the Auxiliary Status Register.
53. Check the Data Register Full bit.
54. Repeat steps 52 and 53 until Data Register Full is OFF ("0").
55. Write the "Save State" message into the Data Register.
56. Wait for an interrupt.
57. Read the Auxiliary Status Register.
58. Read the Interrupt Register.
59. Check the interrupt. A Function Complete interrupt should have occurred, indicating the message was sent successfully.
60. Repeat steps 51 through 59 for a "Disconnect" message.
61. Load the Command Register with a Disconnect command.

(A Disconnect command immediately breaks the connection, and the NCR SCSI Protocol Controller is in the Disconnected state. When ready to continue I/O operation, go to step 27.)

TARGET SENDS STATUS BYTE

62. Load the Command Register with a Send Status command, (Single Byte Transfer = 1 and DMA Mode = 0).
63. Read the Auxiliary Status Register.
64. Check the Data Register Full bit.
65. Repeat steps 63 and 64 until Data Register Full bit is OFF ("0").
66. Write the status byte into the Data Register.
67. Wait for an interrupt.
68. Read the Auxiliary Status Register.
69. Read the Interrupt Register.
70. Check the interrupt. A Function Complete interrupt should have occurred, indicating that the status byte was sent successfully.

TARGET SENDS COMMAND COMPLETE MESSAGE

71. Load the Command Register with a Send Message in command, (Single Byte Transfer = 1, DMA Mode = 0).
72. Read the Auxiliary Status Register.
73. Check the Data Register Full bit.
74. Repeat steps 72 and 73 until Data Register Full bit is OFF ("0").
75. Write the "Command Complete" message into the Data Register.
76. Wait for an interrupt.
77. Read the Auxiliary Status Register.
78. Read the Interrupt Register.
79. Check the interrupt. A Function Complete interrupt should have occurred, indicating that the message was sent successfully.
80. Load the Command Register with a Disconnect command.

(The I/O function is now complete. The user is back in the disconnected state.)

4.2 NOTES

Steps 18 through 20, 35 through 37, 52 through 54, 63 through 65, and 72 through 74 can be omitted if the microprocessor guarantees that one full clock cycle elapses between loading the Command Register and loading the Data Register.

The act of loading an interrupting command resets the Data Register Full status bit in the Auxiliary Status Register. Therefore, when a command is issued that requires data to be put into the Data Register, the data may not be loaded until the Data Register Full bit is allowed to reset.

SECTION 5
INTERRUPT SERVICE ROUTINES (ISR)

This section defines all possible interrupt conditions, and provides suggested responses.

5.1 GENERAL

When interrupted by the NCR SCSI Protocol Controller, the users should read and save the Auxiliary Status Register and the Interrupt Register. (Note that this is not a requirement for servicing the interrupt for the Diagnostic command.)

Figures 5.1 and 5.2 depict the Auxiliary Status and Interrupt Registers.

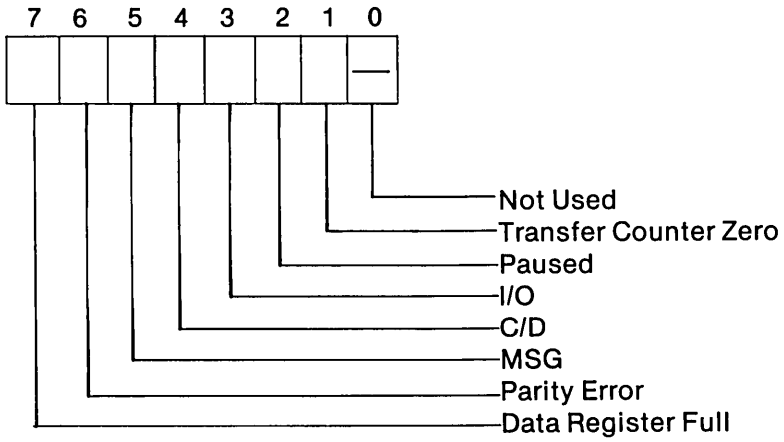


Figure 5.1 Auxiliary Status Register

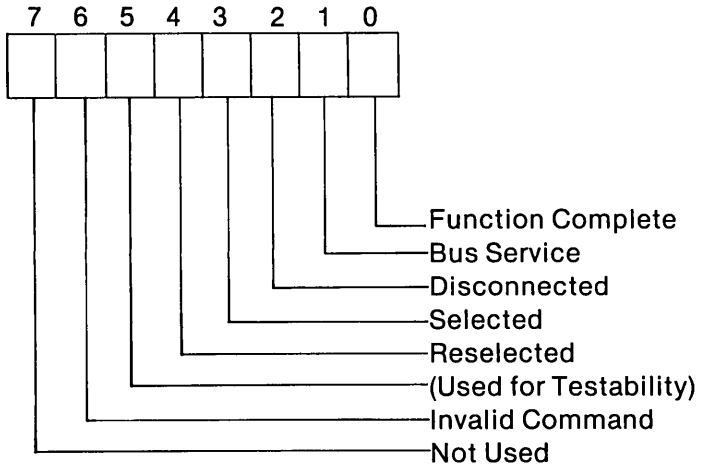


Figure 5.2 Interrupt Register

The act of reading the Interrupt Register disables the interrupt signal (INT), resets the Interrupt Register, and resets an internal flag that indicates an Interrupting command is in progress. For this reason, if a bus event which also causes an interrupt occurs at the same time an Interrupting command is loaded into the Command Register, the command in the Command Register is not executed. Rather, the bus event is honored.

The user must always know in which state the device is operating: Disconnected, Connected as Initiator, or Connected as Target. (This determines which commands are valid for that state and what the interrupt service routine should contain.) Interrupt information is summarized in Table 5.1. The paragraphs following the table describe the suggested interrupt service routines for each state.

5.2 USER DISCONNECTED ISR

In the Disconnected state, the user is either currently logically disconnected from the SCSI bus, or was disconnected at the time the last command to the chip was issued. Valid commands that may have been issued in this state are:

Interrupting	SELECT W/ATN SELECT W/O ATN RESELECT
Immediate	PAUSE CHIP RESET

The seven interrupts that may occur in the Disconnected state are numbered and described below.

1. Interrupt Register (7-0): 0000 1000

   Auxiliary Status Register (7-0): xxxx xxxx

   Reason for Interrupt: The user has been selected as the Target. ATN was not enabled by the Initiator; therefore, the Target is not capable of using messages (with the exception of "Command Complete"), and cannot disconnect prior to completing the function.

   Suggested Response: Set-up the Transfer Counter, issue a Receive command, and proceed with the function through status phase and "Command Complete" message.

2. Interrupt Register (7-0): 0000 1010

   Auxiliary Status Register (7-0): xxxx xxxx

   Reason For Interrupt: The user has been selected as the Target. ATN was asserted by the Initiator; therefore, the Target is capable of using messages.

   Suggested Response: Read the Source ID Register. If the ID Valid bit is not enabled, the Initiator cannot be disconnected until the function is completed. Set the Transfer Counter and issue a Receive Message Out command. The Identify message can be used to determine whether the Initiator can disconnect.

3. Interrupt Register (7-0): 0001 0000

   Auxiliary Status Register (7-0): xxxx xxxx

   Reason for Interrupt: The user has been reselected as the Initiator. It is implied that the Target has disconnect and control message capability.

   Suggested Response: Wait for another interrupt (either Bus Service or Disconnect).

Normally, a Bus Service interrupt is generated for a Message In phase, allowing an "Identify" message to be sent.

4. Interrupt Register (7-0): 0000 0001

   Auxiliary Status Register (7-0): XXXX XXXX

   Reason for Interrupt: The user command has been successfully completed. The Select commands (SELECT W/ATN, SELECT W/O ATN) imply that the user is connected to a Target and is acting as an Initiator, while the Reselect command implies reconnection to an Initiator and action is as a Target.

   Suggested Response: Proceed with intended command sequence. After either Select command, wait for a Bus Service or Disconnect interrupt. After a Reselect command, issue a Send Message In to transmit an "Identify" message.

5. Interrupt Register (7-0): 0000 0100

   Auxiliary Status Register (7-0): XXXX XXXX

   Reason For Interrupt: While executing a Select or Reselect command, no response (BSY) was received from the destination device within the specified timeout. The operation was aborted.

   Suggested Response: Retry a limited number of times.

6. Interrupt Register (7-0): 0100 0000

   Auxiliary Status Register (7-0): XXXX XXXX

   Reason For Interrupt: The user issued a command that is not valid in the Disconnected state.

   Suggested Response: If the command is valid, either retry or issue a Chip Reset command and retry.

7. Interrupt Register (7-0): All Others

   Auxiliary Status Register (7-0): XXXX XXXX

   Reason for Interrupt: Chip malfunction.

   Suggested Response: Issue chip reset and retry operation.

5.3 USER CONNECTED AS TARGET ISR

In this state, the user is logically connected on the SCSI bus in the Target role. Commands that may be issued in this state are:

Interrupting	RECEIVE COMMAND RECEIVE DATA RECEIVE MESSAGE OUT RECEIVE UNSPECIFIED OUTPUT SEND STATUS SEND DATA SEND MESSAGE IN SEND UNSPECIFIED INPUT
Immediate	PAUSE DISCONNECT CHIP RESET

In order to service an interrupt in the Connected as Target state, the user should know the current command and if the pending command will result in an interrupt.

The seven interrupts that may occur in this state are numbered and described below.

1. Interrupt Register (7-0): 0000 0010

   Auxiliary Status Register (7-0): XXXX XXXX

   Reason for Interrupt: ATN was received from the Initiator. If this interrupt was received after issuing an interrupting command, the command was not and will not be executed by the chip.

   Suggested Response: Issue a Receive Message Out command to determine why the Initiator enabled ATN. If a command was aborted, it should be reissued.

2. Interrupt Register (7-0): 0000 0001

   Auxiliary Status Register (7-0): X0XX XXXX

   Reason for Interrupt: A Send or Receive command completed successfully.

   Suggested Response: Proceed with function by issuing any other valid command.

3. Interrupt Register (0-7): 0000 0011

   Auxiliary Status Register (0-7): X0XX XXXX

   Reason for Interrupt: A Send or Receive command has completed. ATN was enabled by the Initiator during the transfer.

   Suggested Response: Issue a Receive Message Out to determine why the Initiator set ATN.

4. Interrupt Register (0-7): 0000 0001

   Auxiliary Status Register (0-7): X1XX XXXX

   Reason for Interrupt: A Receive command terminated due to a bus parity error. (ATN is not enabled.)

   Suggested Response: If the error occurred during a Receive Message Out command, issue a Send Message In, "Message Parity Error" followed by a Receive Message Out in order to retry the message. If the error occurred during another Receive command, issue a Send Message In, "Restore State," and retry the entire transmission. In either case, the number of retries should be limited.

5. Interrupt Register (7-0): 0000 0011

   Auxiliary Status Register (7-0): X1XX XXXX

   Reason for Interrupt: A Receive command terminated due to a bus parity error, and the Initiator is asserting ATN.

   Suggested Response: Similar to previous interrupt, with an exception: if the error did not occur on a message, the ATN should be serviced first by issuing a Receive Message Out.

6. Interrupt Register (7-0): 0100 0000

   Auxiliary Status Register (0-7): XXXX XXXX

   Reason for Interrupt: The user issued a command that is not valid in the Connected as Target state.

Suggested Response: If the command is valid, retry or issue CHIP RESET and retry the entire operation.

7. Interrupt Register (7-0): All Others

   Auxiliary Status Register (0-7): xxxx xxxx

   Reason for Interrupt: Chip malfunction.

   Suggested Response: Issue chip reset and retry operation.

5.4 USER CONNECTED AS INITIATOR ISR

In the Connected as Initiator state, the user is logically connected on the SCSI bus in the Initiator role. Commands that may be issued in this state are:

Interrupting	TRANSFER INFO TRANSFER PAD
Immediate	MESSAGE ACCEPTED SET ATN DISCONNECT CHIP RESET

In order to service an interrupt, the user should know the current command and if the pending command will result in an interrupt. The information phase during the last Transfer command should also be noted.

The seven interrupts that may occur in the Connected as Initiator state are numbered and described below.

1. Interrupt Register (7-0): 0000 0010

   Auxiliary Status Register (0-7): xxxx xxxx

   Reason for Interrupt: A REQ has been received from a Target that the chip cannot service automatically. This may occur prior to issuing a Transfer command when a REQ is received after TC = 0 during a Transfer command, or when an information phase change is detected by the chip during a Transfer command.

   Suggested Response: Compare I/O, C/D, and MSG in the Auxiliary Status Register with the previous information phase to determine if an information phase change has occurred. If the phase type changed, read the Transfer counter and update working pointers for the old phase, and proceed to set-up for the new transfer (Refer to section 5.41 Bus Service Interrupt.) If the phase did not change, a buffer overflow has occurred, and the Transfer Counter Zero bit will have been set.

2. Interrupt Register (0-7): 0000 0100

   Auxiliary Status Register (0-7): xxxx xxxx

   Reason for Interrupt: The Target disconnected from the bus. The disconnection may or may not be expected, depending upon the previous sequence of events.

   Suggested Response: Do housekeeping to complete Initiator role.

3. Interrupt Register (0-7): 0000 0001

   Auxiliary Status Register (0-7): xxxx xxxx

   Reason for Interrupt: A Transfer command for a Message In phase has completed. ACK is left active on the bus.

Suggested Response: Examine the message. To reject the message, issue a Set ATN followed by a Message Accepted command. To accept the message, issue only the Message Accepted command.

4. Interrupt Register (0-7): 0000 0100

   Auxiliary Status Register (0-7): X1XX XXXX

   Reason for Interrupt: The Target disconnected from the bus when ATN was on due to a parity error.

   Suggested Response: Consider this I/O invalid since the Target never sent a Message Out to check the parity error. Abort the I/O.

5. Interrupt Register (0-7): 0000 0010

   Auxiliary Status Register (0-7): X1XX XXXX

   Reason for Interrupt: A REQ from the Target cannot be serviced automatically by the chip. Also, a parity error occurred during the last Transfer Info command.

   The interrupt does not occur at the time of the parity error, but when TC = 0 or the Target changes information phases. The chip automatically sets ATN when the parity error occurs.

   Suggested Response: Use I/O, C/D, and MSG to determine if a phase change occurred. If so, and the new phase is a Message Out, send either a "Message Parity Error" or an "Initiator Detected Error" message. (The choice depends on whether the last phase was a message phase.) If the new phase is not a Message Out, service the new phase and issue a Transfer command. (The chip will keep ATN on until a Message Out is sent with TC = 0.)

   If the phase did not change and the TC = 0, a buffer overflow occurred in addition to the parity error.

6. Interrupt Register (7-0): 0100 0000

   Auxiliary Status Register (0-7): XXXX XXXX

   Reason for Interrupt: The user issued a command that is not valid in the Connected as Initiator state.

   Suggested Response: If the command is valid, retry or issue a Chip Reset command, and retry the entire operation.

7. Interrupt Register (7-0): All Others

   Auxiliary Status Register (7-0): XXXX XXXX

   Reason for Interrupt: Chip malfunction.

   Suggested Response: Issue a Chip Reset command, and retry the operation.

5.4.1 Bus Service Interrupt

The NCR 5385E is designed to interrupt the user for a detected phase change, even when REQ is not active. This offers two advantages:

1. Provides early notification to the Initiator for unbuffered target devices, allowing the Initiator to prepare for the next information phase before it occurs.

2. In high performance systems, this early notification allows the Initiator to prepare the chip

for a requested phase change and increases the overall system performance.

When a phase change is detected by the chip, the phase lines are monitored for 12 clock periods. If the phase lines have indeed changed, the chip monitors the BSY line for an additional 12 clock periods to determine if the chip is still connected. If so, a Bus Service interrupt occurs, indicating a phase change. The user must respond to this phase change by issuing either a Transfer Info or Transfer Pad Command even if this is an unexpected bus phase.

One possible way to handle an invalid or unexpected bus phase is to program the Transfer Counter to a value of "1", and program the Command Register with a Transfer Pad command. If the Target requests data, the Transfer Counter goes to zero and the user receives an interrupt indicating that a REQ has occurred. The important point is that the Initiator must respond to all Bus Service Interrupts by issuing either a Transfer Info or Transfer Pad command to the chip.

The NCR 5386 defaults to NCR 5385E type operation but may be optionally programmed to ignore phase changes except when REQ is active. This is accomplished by setting Bit 3 (phase valid on REQ) in the control register.

5.5 INTERRUPT SUMMARY

The information provided in this section is summarized in the following table.

Table 5.1 Interrupt Summary

User State	Interrupt Register (7-0)	Auxillary Status Register (7-0)	Event
Disconnected	0000 1000	XXXX XXXX	Selected as Target, ATN off.
	0000 1010	XXXX XXXX	Selected as Target, ATN on.
	0001 0000	XXXX XXXX	Reselected as Initiator.
	0000 0001	XXXX XXXX	Select W/ATN, Select W/O ATN, or Reselect command completed successfully.
	0000 0100	XXXX XXXX	No response from Destination while executing a Select or Reselect command.
	0100 0000	XXXX XXXX	Invalid command issued.
	All Others	XXXX XXXX	Hardware Error - should not occur.
Connected as Target	0000 0010	XXXX XXXX	ATN received.
	0000 0001	X0XX XXXX	Send or Receive command successfully completed.
	0000 0011	X0XX XXXX	Send or Receive command completed: ATN was turned on during the transfer.
	0000 0001	X1XX XXXX	Receive command terminated due to bus parity error.
	0000 0011	X1XX XXXX	Receive command terminated due to bus parity error. ATN is on.
	0100 0000	XXXX XXXX	Invalid command issued.
	All Others	XXXX XXXX	Hardware Error - should not occur.
Connected as Initiator	0000 0010	XXXX XXXX	Service Target request.
	0000 0100	X0XX XXXX	Message In transfer completed.
	0000 0001	XXXX XXXX	Transfer for Message In has completed.
	0000 0100	X1XX XXXX	Target disconnected from bus. Did not respond to ATN due to parity error.
	0000 0010	X1XX XXXX	Service Target request. A parity error was previously detected and ATN turned on.
	0100 0000	XXXX XXXX	Invalid command issued.
	All Others	XXXX XXXX	Hardware error - should not occur.

SECTION 6
SCSI BUS INTERFACE

The NCR SCSI Protocol Controller supports either differential pair or open-collector operation. Differential pair operation allows bus devices to be spaced up to 25 meters apart and offers better noise immunity than the more prominent open-collector interface.

The open-collector or single-ended interface is recommended for in cabinet use and limits bus device spacing to 6 meters.

Figure 6.1. shows the suggested interface between the SCSI Protocol Controller and the differential pair transceivers. A 3-to-8 decoder, gated by the ARB signal, is used to enable the driver for the device ID used during arbitration. At this time, all other data bit receivers are enabled for reading and the Protocol Controller drives the appropriate device ID data bit high.

The single-ended interface may be simply implemented using the NCR 8310 General Purpose 48 ma Driver/ Receiver Chip. The equivalent circuit for the NCR 8310 is shown in Figure 6.2. Aside from providing 48 ma sink capability for the SCSI bus, this device may be used with other common device interfaces that require 48 ma operation. The interface to the NCR SCSI Protocol Controller is shown in Figure 6.3.

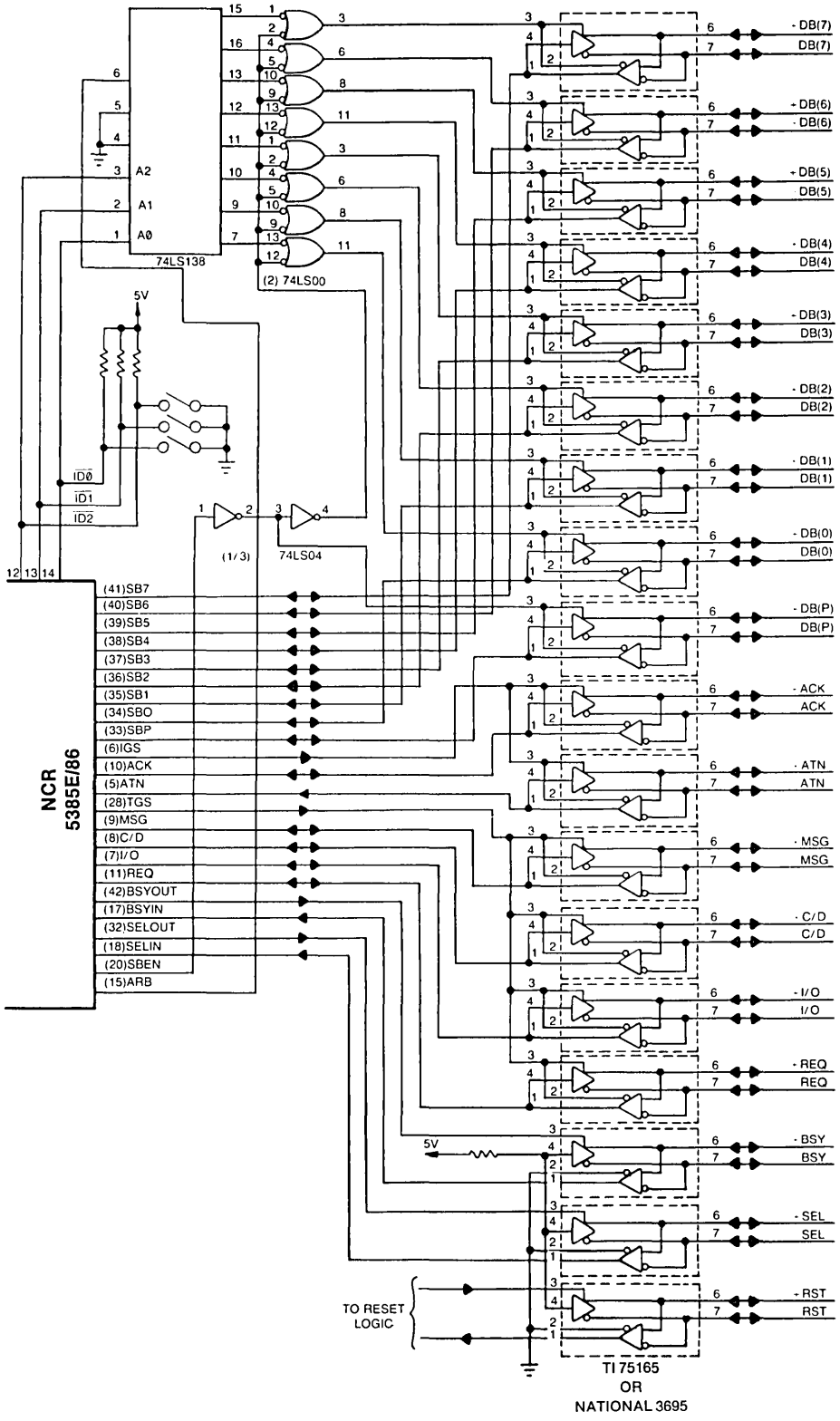


Figure 6.1 Suggested Interface to SCSI Differential Transceivers

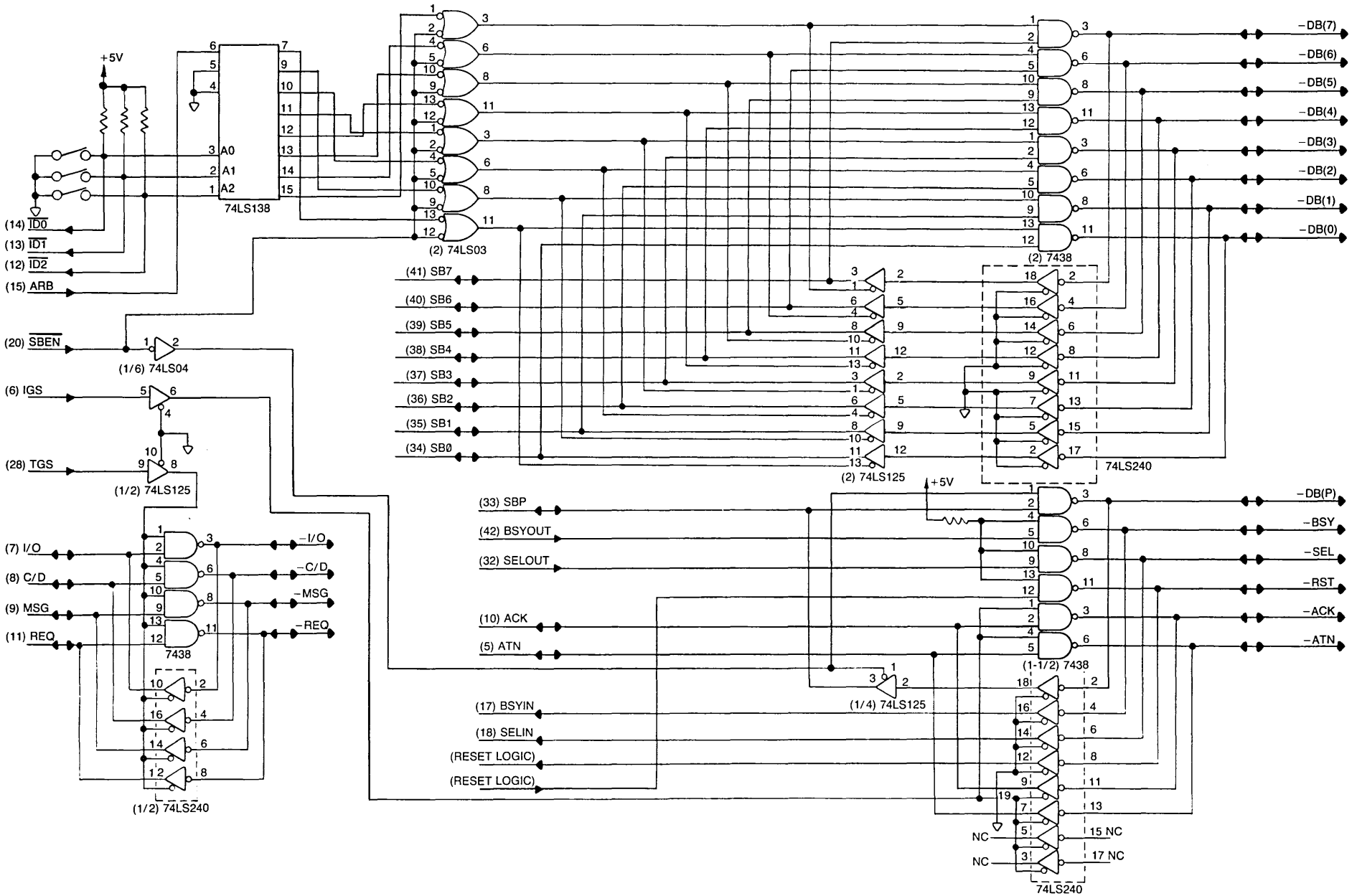


Figure 6.2 NCR 8310 Equivalent Circuit

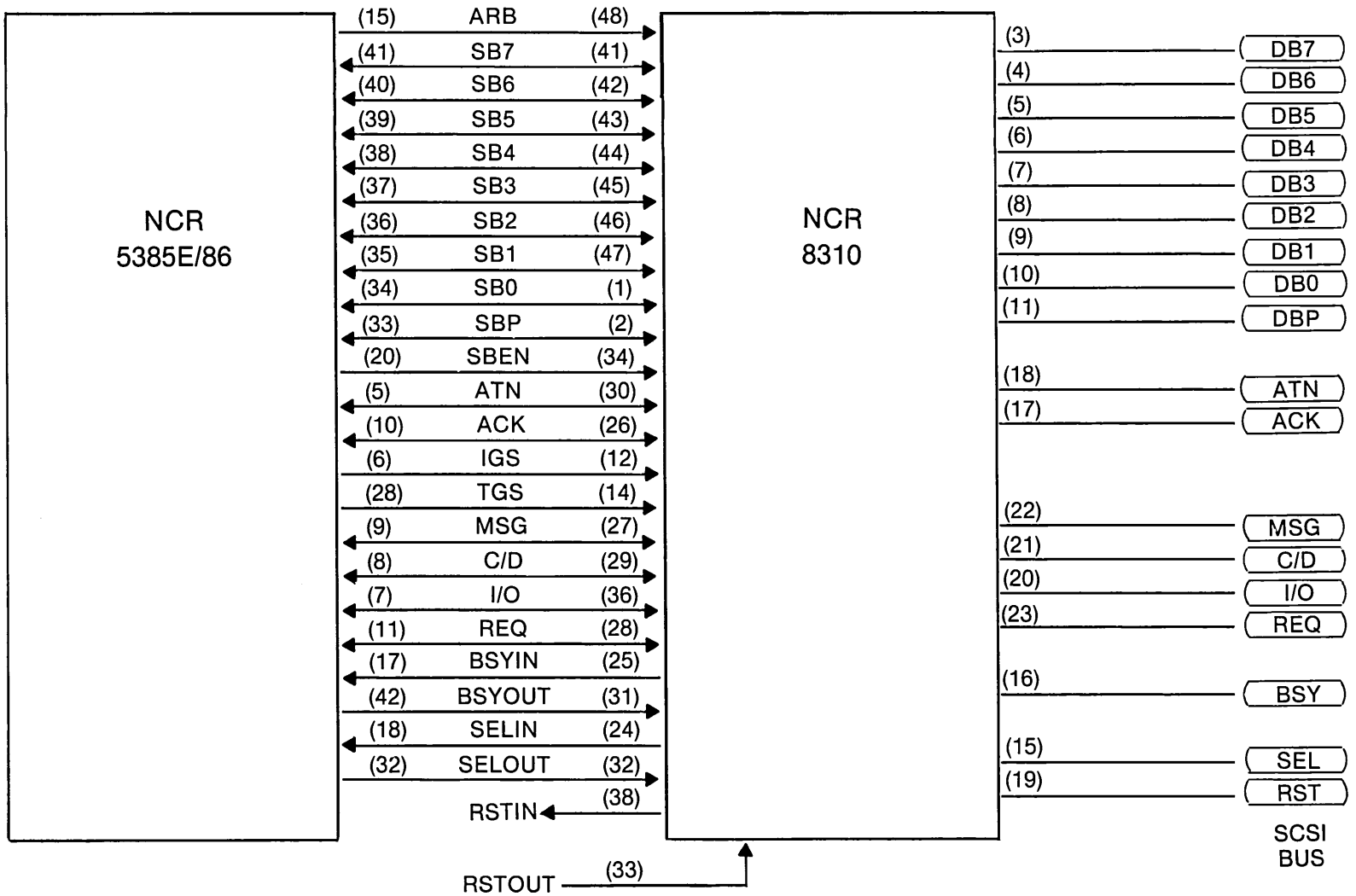


Figure 6.3 Single-Ended Interface Using the NCR 8310 Driver/Receiver Chip

APPENDIX A
NCR 5385E/86 SCSI PROTOCOL CONTROLLER REGISTER AND COMMAND SUMMARY

REGISTER SUMMARY

A3	A2	A1	A0	R/W	REGISTER NAME
0	0	0	0	R/W	Data Register I
0	0	0	1	R/W	Command Register
0	0	1	0	R/W	Control Register
0	0	1	1	R/W	Destination ID
0	1	0	0	R	Auxiliary Status
0	1	0	1	R	ID Register
0	1	1	0	R	Interrupt Register
0	1	1	1	R	Source ID
1	0	0	0	R	Data Register II*
1	0	0	1	R	Diagnostic Status
1	1	0	0	R/W	Transfer Counter (MSB)
1	1	0	1	R/W	Transfer Counter (2nd BYTE)
1	1	1	0	R/W	Transfer Counter (LSB)
1	1	1	1	R/W	Reserved for Testability

*NCR 5386 ONLY

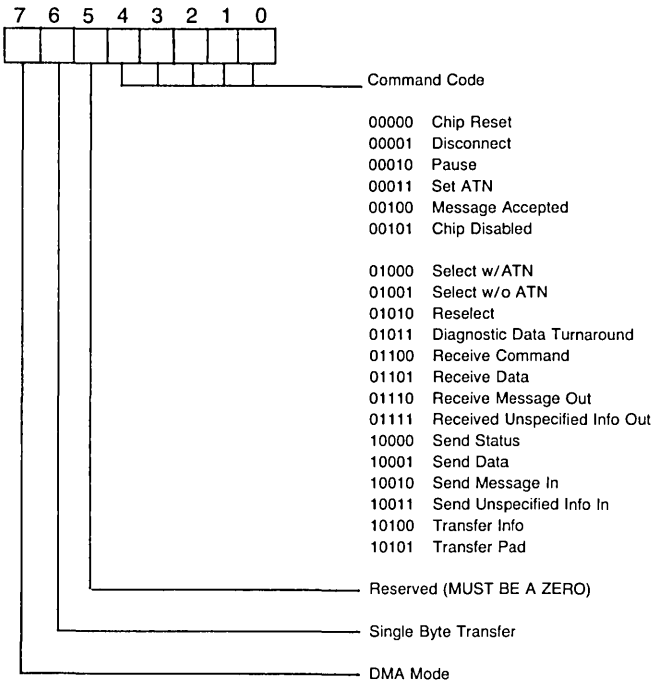
COMMAND SUMMARY

INT = INTERRUPTING
IMM = IMMEDIATE
D = DISCONNECTED
T = CONNECTED AS A TARGET
I = CONNECTED AS AN INITIATOR

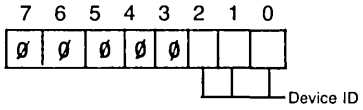
COMMAND CODE	COMMAND	TYPE	VALID STATES
00000	Chip Reset	IMM	D,I,T
00001	Disconnect	IMM	I,T
00010	Paused	IMM	D,T
00011	Set ATN	IMM	I
00100	Message Accepted	IMM	I
00101	Chip Disable	IMM	D,I,T
00110-00111	Reserved	IMM	
01000	Select w/ATN	INT	D
01001	Select w/o ATN	INT	D
01010	Reselect	INT	D
01011	Diagnostic	INT	D
01100	Receive Command	INT	T
01101	Receive Data	INT	T
01110	Receive Message Out	INT	T
01111	Receive Unspecified Info Out	INT	T
10000	Send Status	INT	T
10001	Send Data	INT	T
10010	Send Message Out	INT	T
10011	Send Unspecified Info In	INT	T
10100	Transfer Info	INT	I
10101	Transfer Pad	INT	I
10110-11111	Reserved	INT	

APPENDIX B
INTERNAL REGISTERS

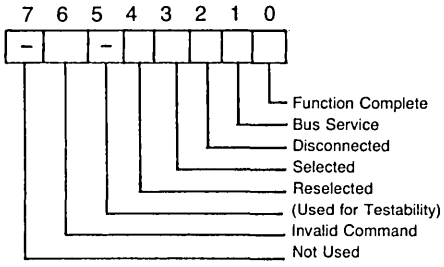
COMMAND REGISTER



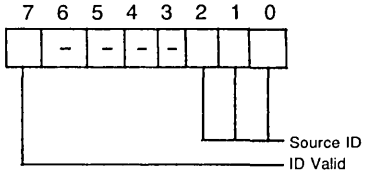
ID REGISTER



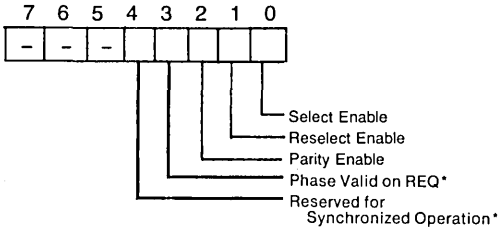
INTERRUPT REGISTER



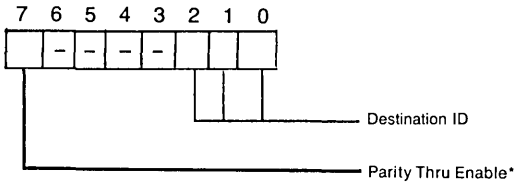
SOURCE ID REGISTER



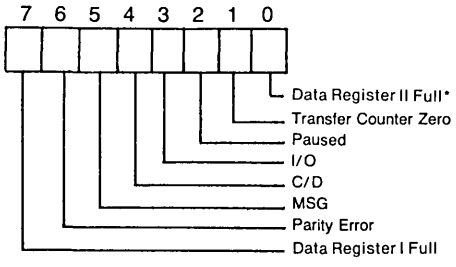
CONTROL REGISTER



DESTINATION ID REGISTER

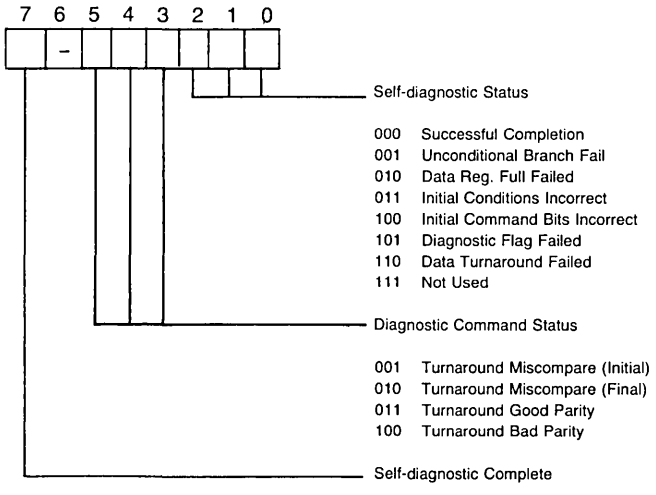


AUXILIARY STATUS REGISTER



*NCR 5386 ONLY

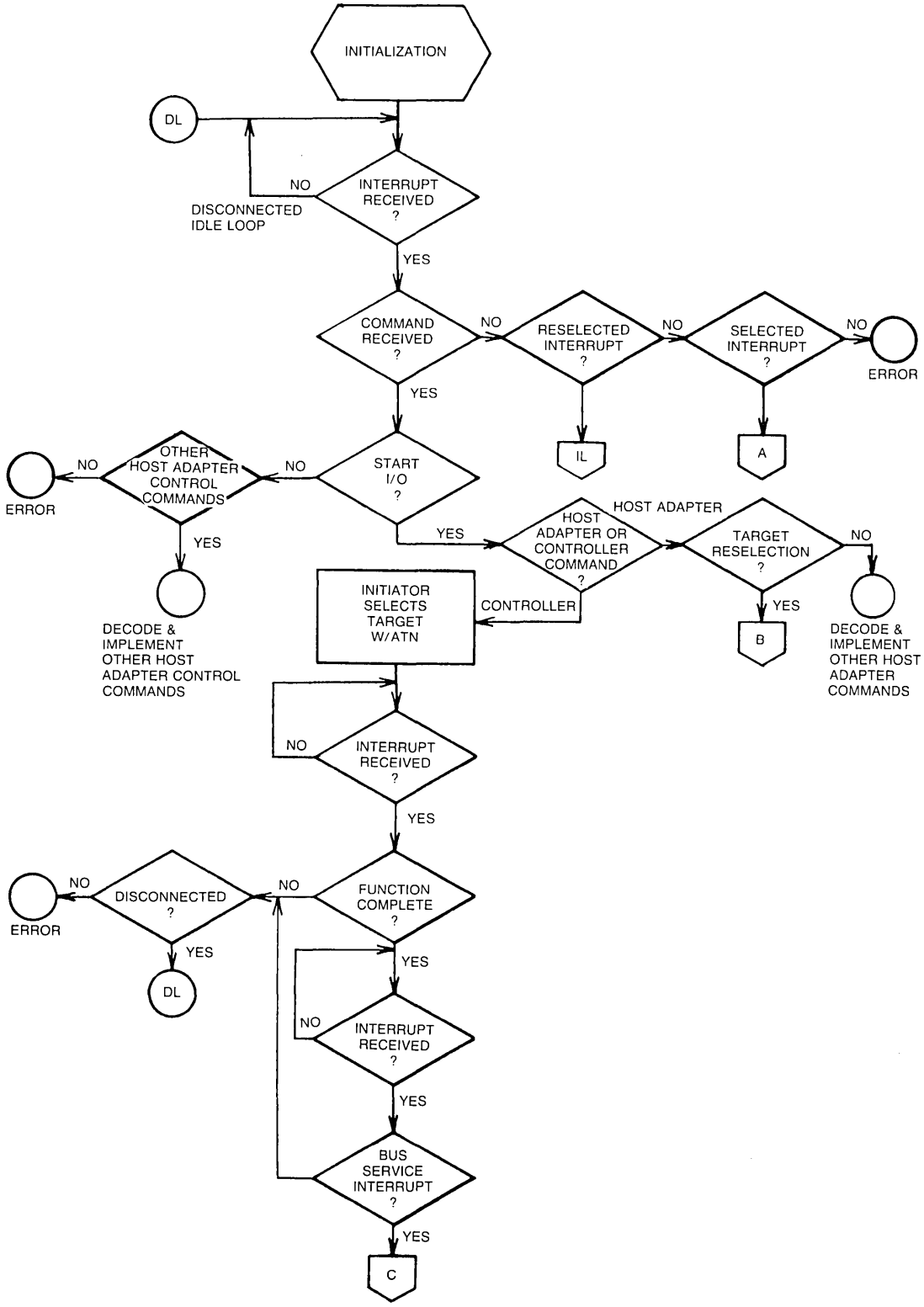
DIAGNOSTIC STATUS REGISTER



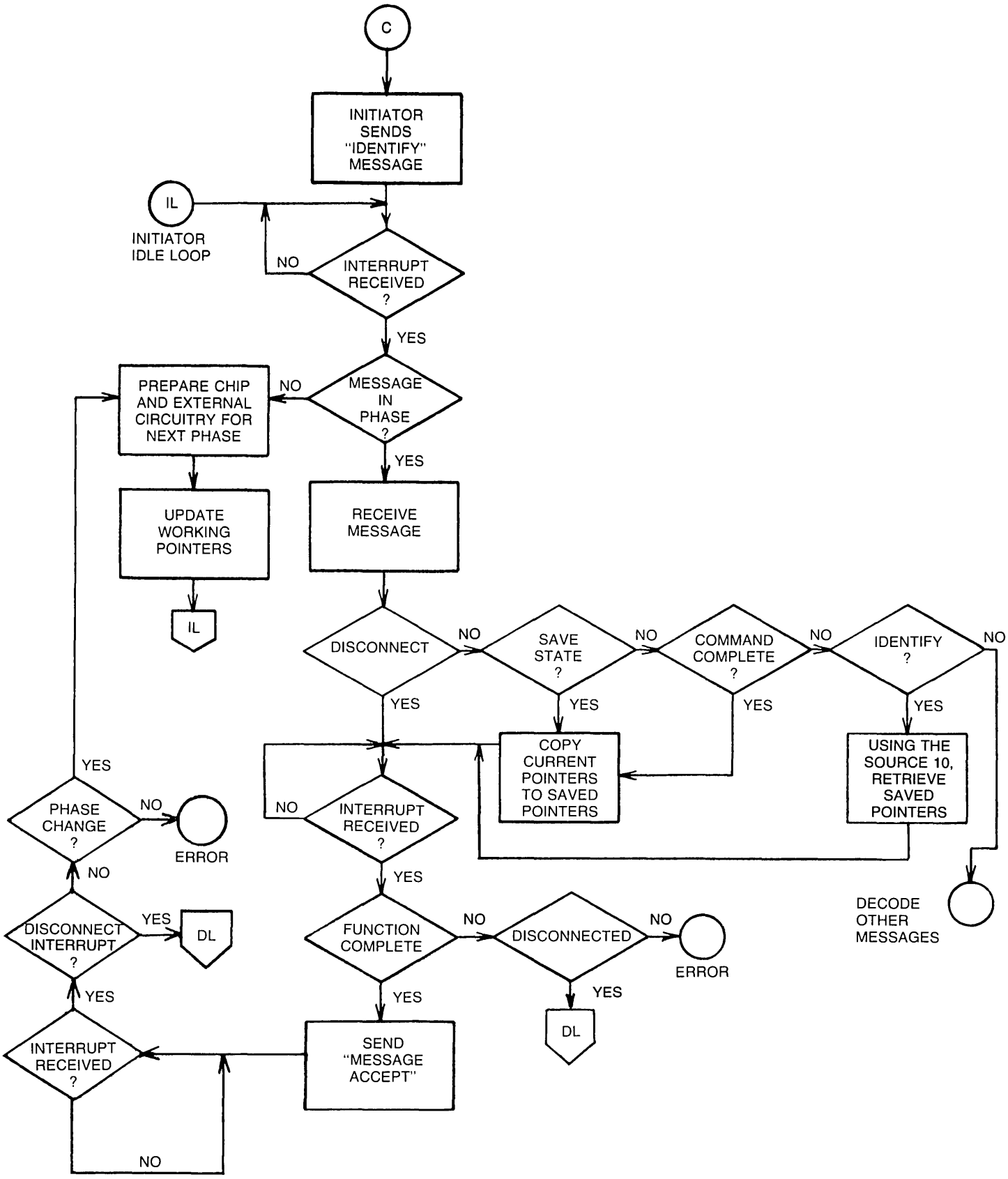
TRANSFER COUNTER

A3	A2	A1	A0	SELECTED BYTE
1	1	0	0	Most Significant Byte
1	1	0	1	Middle Byte
1	1	1	0	Least Significant Byte

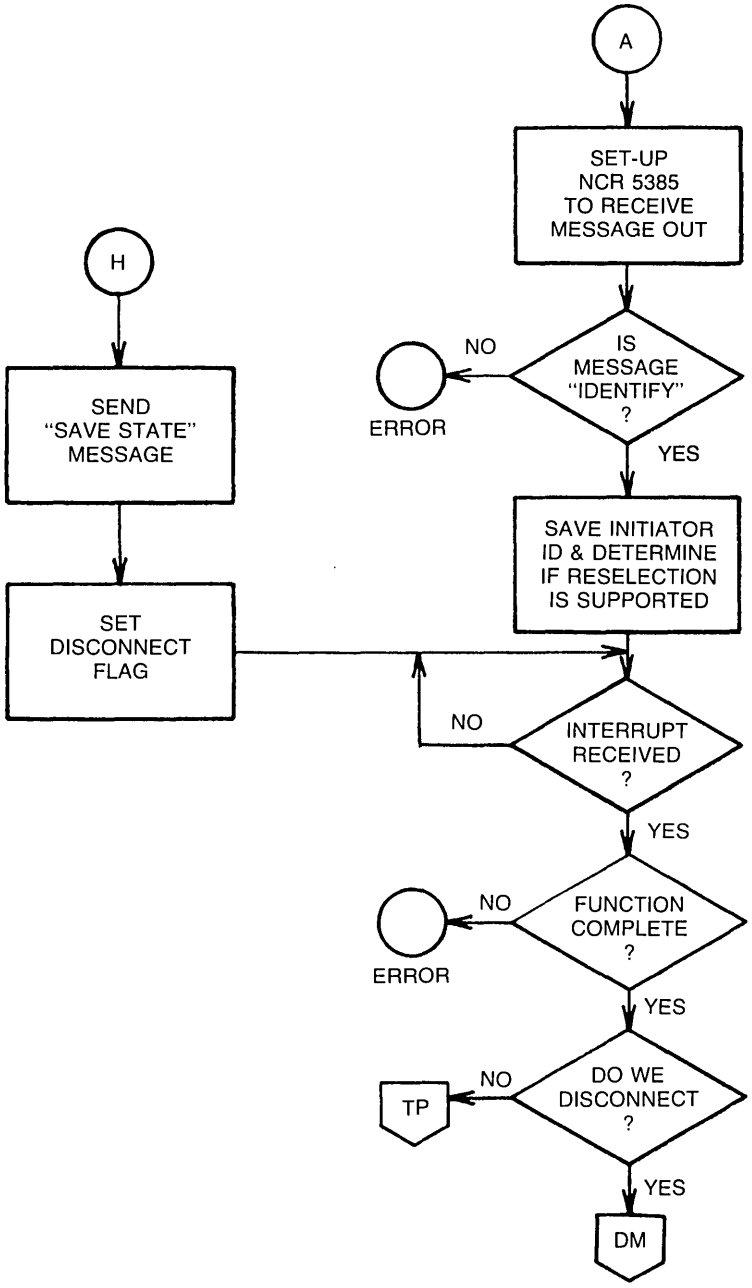
APPENDIX C
INITIATOR/TARGET ROLE FLOWCHART



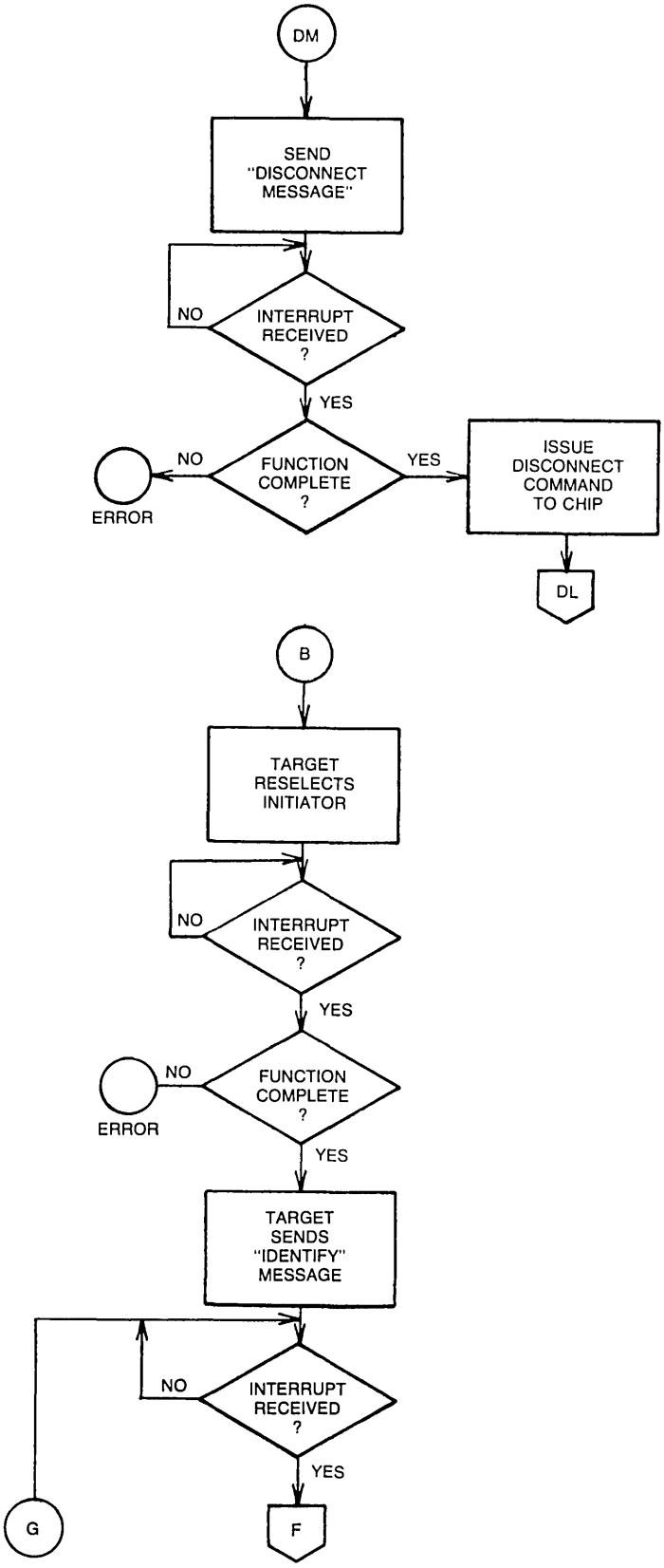
INITIATOR/TARGET ROLE FLOWCHART



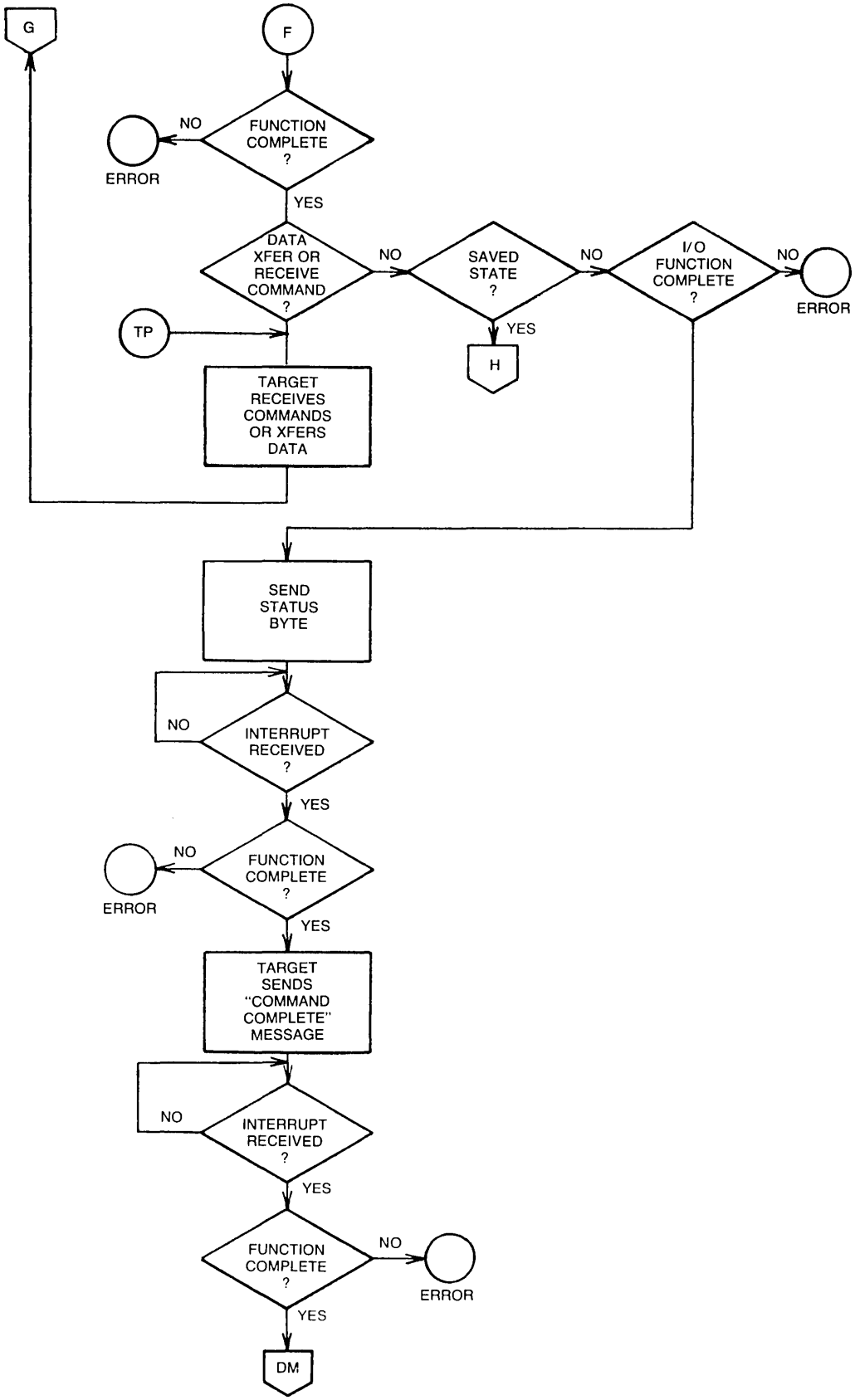
INITIATOR/TARGET ROLE FLOWCHART



INITIATOR/TARGET ROLE FLOWCHART (Continued)



INITIATOR/TARGET ROLE FLOWCHART (Continued)



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