NCR 53C300

SCSI BUFFER CONTROLLER

PRODUCT MANUAL

Microelectronics Division
Colorado Springs

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1. INTRODUCTION

1.1 General Description

The NCR 53C300 SCSI Dual-Ported Buffer Controller combines the functionality of the NCR 53C80 SCSI Interface Chip with a dual-ported buffer controller. The SCSI portion of the chip supports the 1986 ANSI X3.131 SCSI Standard and can be used in both the initiator and target roles. The 53C300 supports arbitration, including reselection. Special high current single-ended output drivers, capable of sinking 48mA at 0.5V, allow for direct connection to the SCSI Bus.

The 53C300 communicates with the system microprocessor as a peripheral device. The chip is controlled by reading and writing the internal registers which may be addressed as standard or memory-mapped I/O. Minimal processor intervention is required for DMA transfers because the chip controls the SCSI handshake signals. The 53C300 also interrupts the microprocessor when it detects a bus condition that requires attention.

The buffer controller portion of the chip is specifically designed to simplify buffering and increase the throughput of block-oriented high-performance peripheral controllers. The dual-ported buffer controller uses static RAM as a dual-ported circular FIFO. The controller supervises data transfers to the buffer which reduces the possibility of host overruns to the peripheral and allows for high-speed DMA transfers. The 53C300 also contains the necessary logic for resolving peripheral controller/SCSI transfer requests by giving priority to the peripheral controller with the SCSI request honored immediately afterward. The buffer controller can address buffer sizes from 256 bytes to 64K bytes.

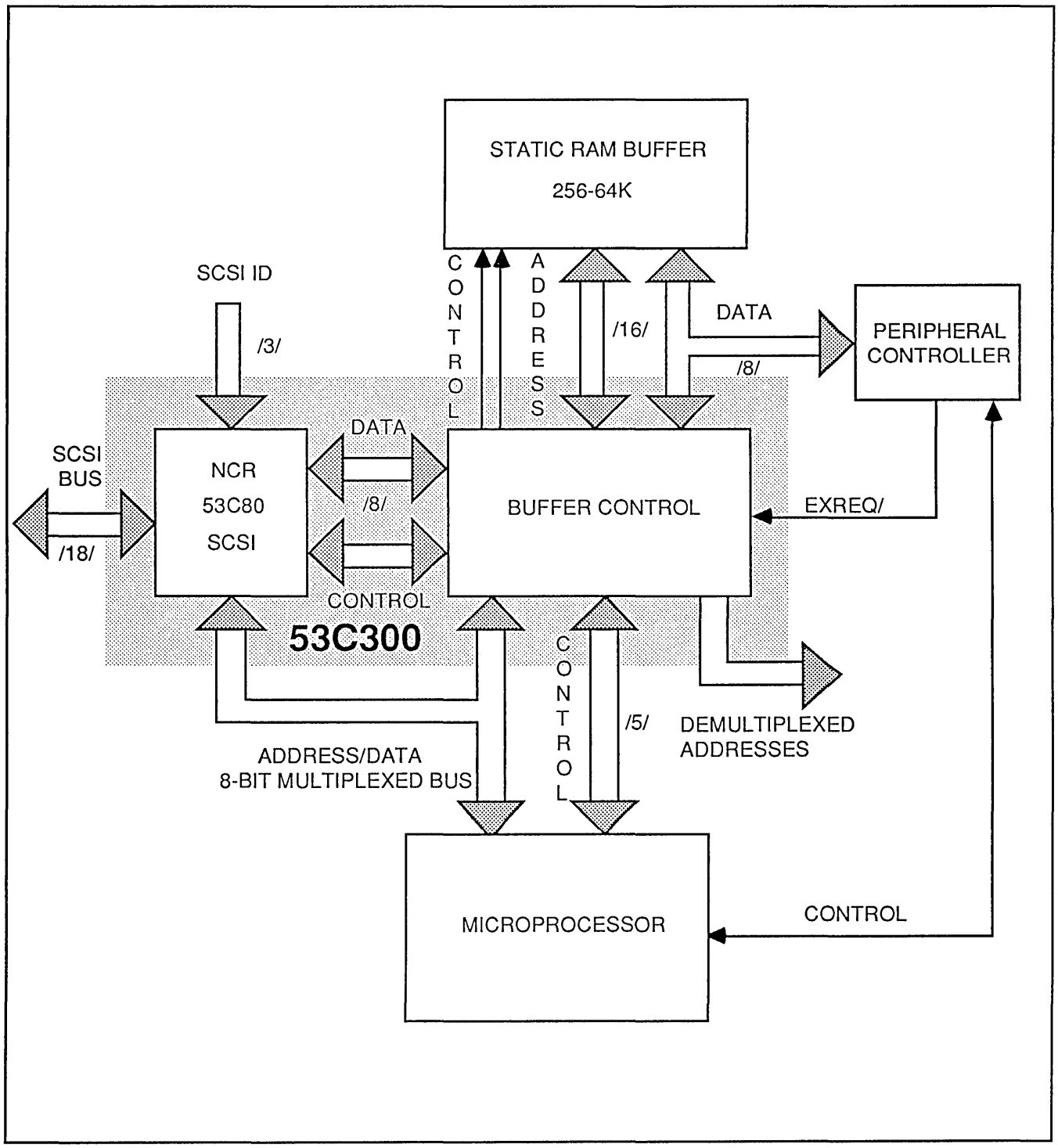
The 53C300 contains a general purpose 4-bit output port. It supports Intel's multiplexed address/data bus scheme and also provides a demultiplexed address bus for use by other peripherals. This chip is intended for use in intelligent controllers and is software configurable via the multiplexed microprocessor I/O bus and is also adaptable to other microprocessor I/O buses that are not multiplexed. The 53C300 provides three input signals with internal pull-ups for SCSI device identification.

Another document which may prove helpful in understanding the 53C300 is the NCR 5380/C80 Design Manual. This, and information on other NCR products, may be obtained by calling the NCR Hotline: 1-800-334-5454.

1.2 Features Summary

- Supports the 1986 ANSI X3.131 SCSI Standard
- Uses static RAM as a dual-ported circular FIFO
- Handles buffer sizes from 256 to 64K bytes in 256-byte increments
- Supports Intel's multiplexed address/data bus
- Provides demultiplexed address bus for use by other peripheral devices which reduces external logic
- Provides three input signals with internal pull-ups for SCSI device identification
- Functionally compatible with the NCR 5380 family
- On-chip single-ended bus transceivers
- Flexible SCSI protocol control
- Stop pointer eliminates possibility of host overruns
- Additional 4-bit output port for general purpose use
- Parity generation with optional checking
- Functions in both the initiator and target roles
- Additional grounding and controlled fall times reduce noise generated by SCSI Bus switching
- Presents no D.C. load to the SCSI Bus when powered down
- CMOS low power requirements
- 84-pin PLCC package

1.3 Block Diagram



2. PIN INFORMATION

(Note: A Slash "/" indicates an active low signal.)

2.1 Pin Description

2.1.1 Microprocessor Interface Signals

SYMBOL	PIN #	TYPE
ALE	21	Input

Address Latch Enable - The ALE Signal latches the address from the multiplexed Address/Data Bus (AD0-AD7). The falling edge of ALE latches the address onto the Address Bus (A0-A7).

PWR/	24	Input

Processor Write Request - The PWR/ Signal latches data from the multiplexed Address/Data Bus (AD0-AD7) to any selected internal register which can be written. The rising edge of PWR/ latches the data into the register. The address specified by the Address Bus (A0-A7) determines to which register the data is written.

PRD/	23	Input

Processor Read Request - The PRD/ Signal reads data from any selected internal register which is readable. The data will appear on the multiplexed Address/Data Bus (AD0-AD7). This data is valid on the rising edge of PRD/. The address specified by the Address Bus (A0-A7) determines from which register the data is read.

PCS	25	Input

Processor Chip Select - The PCS Signal enables the microprocessor access to all registers within the chip. If the chip is selected and the Address Bus (A0-A7) holds a valid internal register address, the PRD/ and PWR/ Signals can be enabled to read or write data. The ALE Signal can latch data onto the Address Bus (A0-A7) regardless of the logic state of this signal.

AD0-AD7	20-13	Input/Output

Address/Data Bus - The Address/Data Bus is an 8-bit bus multiplexed between address and data. ALE latches the address onto the Address Bus (A0-A7). During a read, (PRD/ active) these lines are driven by the chip; during a write, (PWR/ active) they are driven by the microprocessor.

IRQ/	41	Output

Interrupt Request - The IRQ/ Signal is sent to the microprocessor when an interrupt condition has occurred within the chip.

A0-A7	33-26	Output

Address Bus - The Address Bus holds the last valid address to have appeared on the multiplexed Address/Data Bus (AD0-AD7). The falling edge of ALE latches the address of AD0-AD7 onto this bus.

2.1.2 Peripheral Interface Signals

These signals are used to interface the peripheral controller to the chip.

SYMBOL	PIN #	TYPE
EXREQ/	11	Input

External Data Transfer Request - The EXREQ/ Signal is asserted when the peripheral controller requests the next available memory cycle to do a transfer between itself and the buffer memory. It has priority over data transfer requests from the SCSI Bus.

HSD0-HSD7	74-67	Input/Output

High-Speed Data Bus - The High-Speed Data Bus allows the 53C300 and the peripheral controller to transfer data to the buffer memory. This common data bus is used during transfers between the SCSI Bus and the buffer memory or the peripheral controller and the buffer memory.

2.1.3 Buffer Control and Interface Signals

These signals are used to interface the chip to the buffer memory.

SYMBOL	PIN #	TYPE
OE/	10	Output

Output Enable - The OE/ Signal enables the buffer memory for a read. It is asserted when the buffer is read by the 53C300. The peripheral controller can read the buffer when the 53C300 asserts this signal.

WR/	9	Output

Write Enable - The WR/ Signal enables the buffer memory for a write. It is asserted low when the 53C300 writes to the buffer. The peripheral controller can write to the buffer when the 53C300 asserts this signal.

MB0-MB15	7-1, 84-76	Output

Memory Buffer Address Bus - The Memory Buffer Address Bus selects the desired memory locations within the buffer memory. The value of the Read Address Pointer (RAP) appears on this bus during a buffer read, and the value of the Write Address Pointer (WAP) appears on the bus during a buffer write.

HSD0-HSD7	74-67	Input/Output

High-Speed Data Bus - The High-Speed Data Bus allows the chip and the peripheral controller to transfer data to the buffer memory. This common data bus is used during transfers with the SCSI Bus and the buffer memory or the peripheral controller and the buffer memory.

2.1.4 Miscellaneous Signals

SYMBOL	PIN #	TYPE
CLKA/	8	Input

Clock - The CLKA/ Signal synchronizes data transfers with the buffer memory and the peripheral controller.

PORST/	66	Input

Power On Chip Reset - The PORST/ Signal, when active, resets all registers in the 53C300. This signal will not assert the SCSI RST/ Signal.

D0-D2	36-34	Output

Data Output Pins - The Data Output Pins are general purpose output pins that can be controlled by accessing the D0-D2 Bits (Register 30, Bits 3-5). They can be used for general purpose control functions for external components. Outputs D0-D2 have 4mA source capability and 8mA sink capability.

LED/	64	Output

Light Emitting Diode Driver Output - The LED/ Signal can be used to drive an external light emitting diode. It can be controlled by accessing the LED/ Bit (Register 30, Bit 6). This output contains a special open-drain high-current output driver with 48mA sink capability.

ID0/-ID2/	38-40	Input

SCSI ID Input Pins - The SCSI ID Input Pins are three inputs which may be read by reading the ID0/-ID2/ Bits (Register 30, Bits 0-2). These pins have on-chip pull-up resistors. Before starting the arbitration process, the microprocessor should read these bits, decode their value, and set up the correct value in the Output Data Register (Register 20).

TP/	37	Input

Test Pin - The Test Pin is intended for device functionality tests only. This pin has an on-chip pull-up resistor and should be tied high for normal operation.

2.1.5 SCSI Interface Signals

The following signals are all bi-directional, active low, open-drain signals. With 48mA sink capability, all pins interface directly with the SCSI Bus.

SYMBOL	PIN #	TYPE
ACK/	55	Input/Output

Acknowledge - The ACK/ Signal, driven by an initiator, indicates an acknowledgment for a SCSI data transfer handshake. In the target role, ACK/ is received as a response to the REQ/ Signal.

ATN/	53	Input/Output

Attention - The ATN/ Signal, driven by an initiator, indicates an attention condition. In the target role, ATN/ is received.

BSY/	54	Input/Output

Busy - The BSY/ Signal indicates that the SCSI Bus is being used and can be driven by both the initiator and the target device.

C/D/	60	Input/Output

Control/Data - The C/D/ Signal, driven by a target, indicates that control or data information is on the SCSI Bus. This signal is received by the initiator.

I/O/	63	Input/Output

Input/Output - The I/O/ Signal, driven by a target, controls the direction of data transfer on the SCSI Bus. When active, this signal indicates input to the initiator. When inactive, this signal indicates output from the initiator. This signal is also used to distinguish between the Selection and Reselection Phases.

MSG/	58	Input/Output

Message - The MSG/ Signal is driven active by a target during the Message Phase. This signal is received by the initiator.

REQ/	61	Input/Output

Request - The REQ/ Signal, driven by a target, indicates a request for a SCSI data transfer handshake. This signal is received by the initiator.

RST/	57	Input/Output

Reset - The RST/ Signal indicates an SCSI Bus reset condition.

SDB0/-SDB7/	42-43, 45-49, 51	Input/Output
SDBP/	52	

SCSI Data Bits and Parity Bit - These eight Data Bits (SDB0/-SDB7/), plus a Parity Bit (SDBP/), form the SCSI Data Bus. SDB7/ is the most significant bit and has the highest priority ID during the Arbitration Phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.

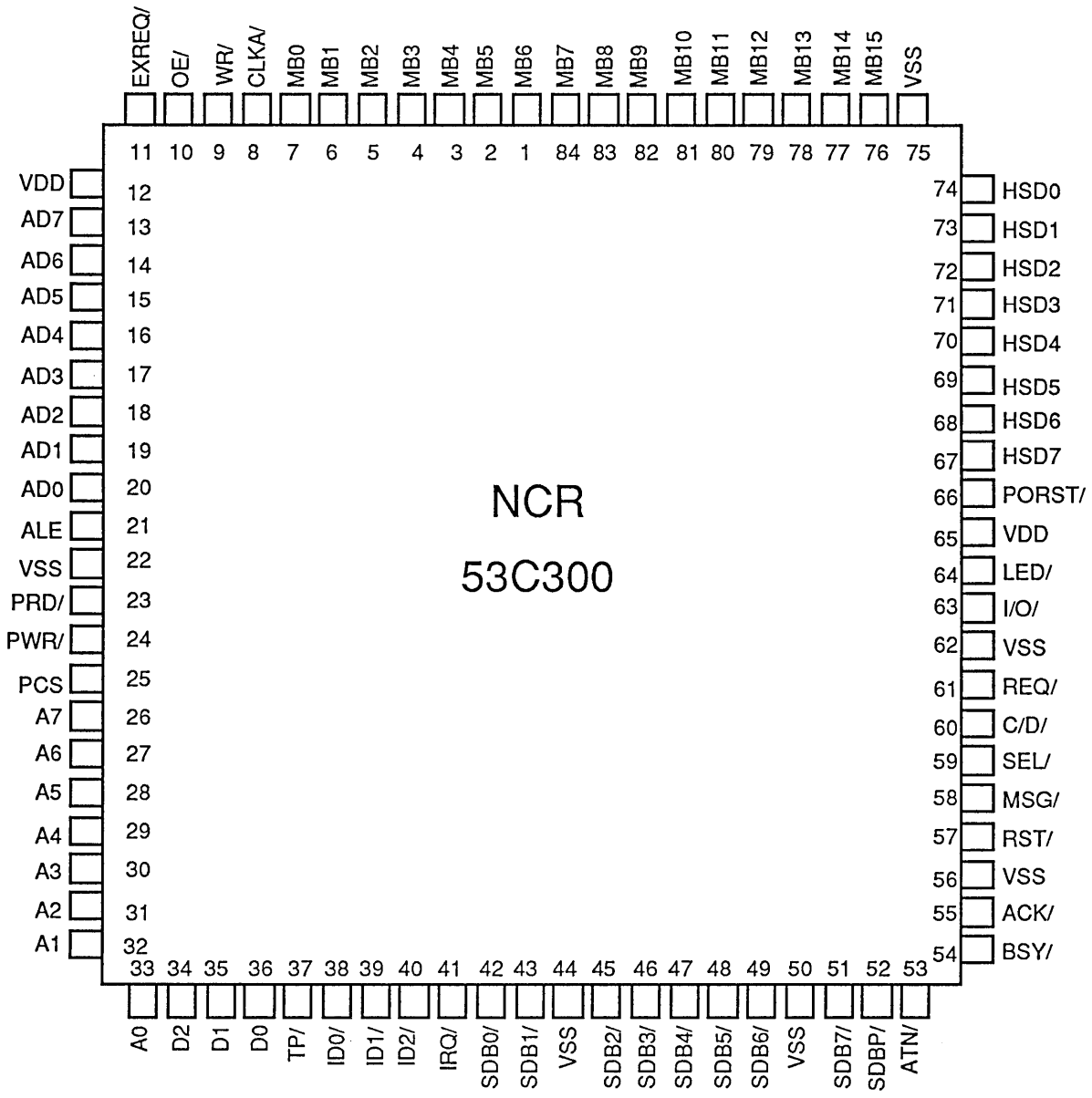
SEL/	59	Input/Output

Select - The SEL/ Signal is used by an initiator to select a target or by a target to reselect an initiator.

2.1.6 Power Signals

SYMBOL	PIN #	TYPE
VDD	12, 65	+5 Volts
VSS	22, 44, 50, 56, 62, 75	Ground

2.2 Pin Diagram



3. REGISTERS

3.1 53C80 Registers

3.1.1 Current SCSI Data Register - Address 20 (Read Only)

The Current SCSI Data Register is a read-only register which allows the microprocessor to monitor the active SCSI Data Bus. If parity checking is enabled, the SCSI Data Bus parity is checked at the beginning of the read cycle. This register is used during a programmed I/O data read or during arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during arbitration.

3.1.2 Output Data Register - Address 20 (Write Only)

The Output Data Register is a write-only register that sends data to the SCSI Data Bus. This register should contain the proper ID bits to drive the SCSI Data Bus during the Arbitration and Selection Phases.

3.1.3 Initiator Command Register - Address 21 (Read/Write)

The Initiator Command Register is a read/write register which asserts certain SCSI Bus signals, monitors those signals, and monitors the progress of SCSI Bus arbitration. Many of these bits are significant only when used as an initiator. However, most can be used during target role operation.

Bit 7 - Assert RST/ - Read/Write

When set, the RST/ Signal is asserted on the SCSI Bus. The RST/ Signal will remain asserted until this bit is reset or until PORST/ (Pin 66) is asserted. After this bit is set, IRQ/ goes active, all SCSI signals are removed except for RST/, and Registers 20 through 27 are reset.

Bit 6 - Arbitration In Progress - Read Only

This bit is used to determine if arbitration is in progress. For this bit to be active, the Arbitrate Bit (Register 22, Bit 0) must previously have been set. The Arbitration In Progress Bit indicates that a bus-free condition has been detected, and the chip has asserted BSY/ and the contents of the Output Data Register onto the SCSI Bus. Arbitration In Progress will remain set until the Arbitrate Bit is reset.

Bit 6 - Test Mode - Write Only

This bit may be set in a test environment to disable all output drivers. It should not be set for normal operation.

Bit 5 - Lost Arbitration - Read Only

When set, this bit indicates that the chip has detected a bus-free condition, arbitrated for use of the bus by asserting BSY/ and its ID on the SCSI Bus, and lost arbitration due to SEL/ being asserted by another bus device. For this bit to be set, the Arbitrate Bit (Register 22, Bit 0) must be set.

Bit 4 - Assert ACK/ - Read/Write

This bit is used by the initiator to assert ACK/ onto the SCSI Bus. In order to assert ACK/, the Target Mode Bit (Register 22, Bit 6) must not be set. Writing a zero to this bit de-asserts ACK/ on the SCSI Bus. Reading this register simply reflects the status of this bit.

Bit 3 - Assert BSY/ - Read/Write

When set, this bit asserts BSY/ onto the SCSI Bus. When reset, this bit de-asserts the BSY/ Signal. Asserting BSY/ indicates a successful attempt to gain control of the SCSI Bus. Resetting this bit creates a bus-disconnect condition, except during the Selection Phase. Reading this register simply reflects the status of this bit.

Bit 2 - Assert SEL/ - Read/Write

When set, this bit asserts SEL/ onto the SCSI Bus. SEL/ is normally asserted after arbitration has been successfully completed. When reset, this bit de-asserts the SEL/ Signal. Reading this register simply reflects the status of this bit.

Bit 1- Assert ATN/ - Read/Write

When set, this bit asserts ATN/ onto the SCSI Bus if the Target Mode Bit (Register 22, Bit 6) is not set. ATN/ is normally asserted by the initiator to request a Message Out Phase. When reset, this bit de-asserts the ATN/ Signal. Reading this register simply reflects the status of this bit.

Bit 0 - Assert Data Bus - Read/Write

When set, this bit allows the contents of the Output Data Register to be enabled as chip outputs on SCSI signals SDB0/ through SDB7/. Parity is also generated and asserted on SDBP/. When connected as an initiator, the outputs are only enabled if the Target Mode Bit (Register 22, Bit 6) is not set, and the phase signals C/D/, I/O/, and MSG/ match the contents of the Assert C/D/, Assert I/O, and Assert MSG/ in the Target Command Register. The Assert Data Bus Bit should also be set during DMA operations.

3.1.4 Mode Register - Address 22 (Read/Write)

The Mode Register is used to control the operation of the chip. This register determines whether the chip operates as an initiator or target, whether parity is checked, and whether interrupts are generated on various external conditions.

Bit 7 - Do Not Set

Bit 6 - Target Mode - Read/Write

When set, the chip operates as a SCSI Bus target device. When reset, the chip operates as a SCSI Bus initiator device. In order for the signals ATN/ and ACK/ to be asserted onto the SCSI Bus, the Target Mode Bit must not be set. In order for the signals C/D/, I/O/, MSG/, and REQ/ to be asserted onto the SCSI Bus, the Target Mode Bit must be set.

Bit 5 - Enable Parity Checking - Read/Write

This bit determines whether parity errors will be ignored or saved in the parity error latch. When set, parity errors are saved. When reset, parity errors are ignored.

Bit 4 - Enable Parity Interrupt - Read/Write

When set, this bit causes the IRQ/ Signal to be asserted if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking Bit is also set.

Bit 3 - Enable EOP Interrupt - Read/Write

When this bit and the REOP Bit (Register 28, Bit 3) are set, the IRQ/ Signal is asserted when the DMA transfer is completed. The DMA transfer is completed when the value of STP is equal to the value of RAP during a DMA send operation, or equal to the value of WAP during a DMA receive operation.

Bit 2 - Monitor Busy - Read/Write

When set, this bit causes the IRQ/ Signal to be asserted when BSY/ unexpectedly changes from active to inactive. When the interrupt is generated, the lower six bits of the Initiator Command Register are reset and all signals are de-asserted on the SCSI Bus. The Busy Error Bit (Register 25, Bit 2) will also be set when this condition occurs.

Bit 1 - DMA Mode - Read/Write

The DMA Mode Bit allows a DMA transfer to occur and must be set prior to writing Registers 25 through 27. Registers 25 through 27 are used to start DMA transfers. The Target Mode Bit (Register 22, Bit 6) must be set prior to a write to Register 26 and reset prior to a write to Register 27. The Assert Data Bus Bit (Register 21, Bit 0) must be set for all DMA send operations. In the DMA Mode, REQ/ and ACK/ are automatically controlled.

The DMA Mode Bit is not reset when an internal 53C80 core End of DMA Transfer Process Signal (EOP/) is received. That is, it is not reset when the STP equals RAP or WAP. Any DMA transfer may be stopped by writing a zero into this bit location. However, care must be taken not to access Registers 20 through 27 when the internal 53C80 core DACK/ Signal is active. For this reason, the DMA Enable Bit (Register 28, Bit 1) has to be reset first to stop any potential conflict with DACK/. The SCSI BSY/ Signal must be active in order to set the DMA Mode Bit.

Bit 0 - Arbitrate - Read/Write

When set, this bit starts the arbitration process. Prior to setting this bit the Output Data Register should contain the proper SCSI device ID value. One data bit should be active for SCSI Bus arbitration. The chip will wait for a bus-free condition before entering the Arbitration Phase. The status of the Arbitration Phase may be determined by reading the Lost Arbitration and Arbitration In Progress Bits (Register 21, Bits 5 and 6 respectively).

3.1.5 Target Command Register - Address 23 (Read/Write)

The Target Command Register allows the microprocessor to control the SCSI Bus Information Transfer Phase and/or to assert REQ/ simply by writing this register. The Target Mode Bit (Register 22, Bit 6) must be set for bus assertion to occur. If connected as an initiator with the DMA Mode Bit (Register 22, Bit 1) set, and the I/O/, C/D/, and MSG/ phase lines do not match the phase bits in the Target Command Register, a phase mismatch interrupt will be generated when REQ/ goes active. In order to send data as an initiator, the Assert I/O/, Assert C/D/, and Assert MSG/ bits must match the corresponding bits in the Current SCSI Bus Status Register (Register 24).

Bit 7 - Last Byte Sent - Read Only

This bit indicates that the last byte of the DMA send operation has been sent on the SCSI Bus. This flag is necessary since the End of DMA Transfer Bit (Register 25, Bit 7) only reflects when the last byte was received from the buffer memory.

Bit 3 - Assert REQ/ - Read/Write

When this bit is set, REQ/ is asserted.

Bit 2 - Assert MSG/ - Read/Write

When this bit is set, MSG/ is asserted.

Bit 1 - Assert C/D/ - Read/Write

When this bit is set, C/D/ is asserted.

Bit 0 - Assert I/O/ - Read/Write

When this bit is set, I/O/ is asserted.

3.1.6 Current SCSI Bus Status Register - Address 24 (Read Only)

The Current SCSI Bus Status Register is a read-only register which monitors seven SCSI Bus control signals plus the SCSI Data Bus Parity Bit. When a bit is set, it represents an active signal; when a bit is not set or reset, it represents an inactive signal.

Bit 7 - RST/

Bit 6 - BSY/

Bit 5 - REQ/

Bit 4 - MSG/

Bit 3 - C/D/

Bit 2 - I/O/

Bit 1 - SEL/

Bit 0 - SDBP/

3.1.7 Select Enable Register - Address 24 (Write Only)

The Select Enable Register is a write-only register which masks all but a single ID bit during a selection attempt of the 53C300 by another device. The SCSI ID of the chip is written as a one (1) to the bit that corresponds to the SCSI ID value. For example, if SCSI ID 7 is the ID of the chip, then Bit 7 must be set for the interrupt to be generated after the chip is successfully selected. The simultaneous occurrence of the correct SCSI ID, BSY/ inactive, and SEL/ active will cause an interrupt. This interrupt can be disabled by resetting all bits in this register, effectively disallowing the chip to be selected. If the Enable Parity Checking Bit (Register 22, Bit 5) is active, parity will be checked during selection.

3.1.8 Bus and Status Register - Address 25 (Read Only)

The Bus and Status Register is a read-only register which monitors six status bits and the two SCSI control signals (ATN/ and ACK/) which are not found in the Current SCSI Bus Status Register (Register 24).

Bit 7 - End of DMA Transfer

This bit is set if the Buffer Control logic has terminated the DMA process. Since the termination happens as the last byte is transferred to the chip, the Last Byte Sent Bit (Register 23, Bit 7) must be monitored to ensure that the last byte sent to the Output Data Register (Register 20) has been transferred to the SCSI Bus. This bit is reset when the DMA Mode Bit (Register 22, Bit 1) is reset .

Bit 6 - DMA Request

This bit allows the microprocessor to sample the internal 53C80 core DMA Request (DRQ) Signal. DRQ can be cleared by an internal 53C80 core DMA Acknowledge (DACK/) Signal from the Buffer Control logic or by resetting the DMA Mode Bit (Register 22, Bit 1). The DRQ Signal does not reset when a phase mismatch interrupt occurs.

Bit 5 - Parity Error

This bit is set if a parity error occurs when receiving data or during a device selection. It can only be set if the Enable Parity Checking Bit (Register 22, Bit 5) is set. This bit may be cleared by reading the Reset Parity/Interrupt Register (Register 27).

Bit 4 - Interrupt Request Active

This bit indicates whether an interrupt condition has been detected within the 53C300 core. When set, the IRQ/ Signal is active; when reset, IRQ/ is inactive. It can be cleared by reading the Reset Parity/Interrupt Register (Register 27).

Bit 3 - Phase Match

The SCSI MSG/, C/D/, and I/O/ Signals determine the current Information Transfer Phase. The Phase Match Bit indicates whether the current SCSI Bus phase matches the lower three bits of the Target Command Register (Register 23). The Phase Match Bit is continuously updated and is only significant when operating as a bus initiator. A phase match is required for data transfer to occur on the SCSI Bus.

Bit 2 - Busy Error

This bit is active if the BSY/ Signal is detected inactive for at least 400ns. The Busy Error Bit will disable any SCSI outputs and will reset the DMA Mode Bit (Register 22, Bit 1). This bit can be monitored to determine when the SCSI Bus is in a bus-free state.

Bit 1 - ATN/

This bit reflects the condition of the SCSI ATN/ Signal . When this bit is set, ATN/ is active. This signal is normally monitored by the target device. An active SCSI ATN/ can assert the IRQ/ by setting the Enable Attention Interrupt Bit (Register 28, Bit 4).

Bit 0 - ACK/

This bit reflects the condition of the SCSI Bus control signal ACK/. When this bit is set, ACK/ is active.

3.1.9 Start DMA Send Register - Address 25 (Write Only)

The Start DMA Send Register produces a strobe which starts a DMA send from the chip to the SCSI Data Bus. To initiate a DMA Send operation, the DMA Mode Bit (Register 22, Bit 1) and the DMA Enable Bit (Register 28, Bit 1) must be set. Any value written to this register will start the DMA send operation. The DMA Send operation can be initiated in either the initiator or the target mode.

3.1.10 Input Data Register - Address 26 (Read Only)

The Input Data Register is a read-only register that is used to receive data from the SCSI Data Bus during DMA transfers.

3.1.11 Start DMA Target Receive Register - Address 26 (Write Only)

The Start DMA Target Receive Register is written to initiate a DMA receive from the SCSI Data Bus to the chip for target operation only. To initiate a DMA Target Receive operation, the DMA Mode Bit (Register 22, Bit 1), the Target Mode Bit (Register 22, Bit 6), and the DMA Enable (Register 28, Bit 1) must all be set. Any value written to this register will start the DMA Target Receive Operation.

3.1.12 Reset Parity/Interrupt Register - Address 27 (Read Only)

The Reset Parity/Interrupt Register, when read, resets the Parity Error Bit, the Interrupt Request Bit, and the Busy Error Bit in the Bus and Status Register (Register 25).

3.1.13 Start DMA Initiator Receive Register - Address 27 (Write Only)

The Start DMA Initiator Receive Register is written to initiate a DMA Receive from the SCSI Data Bus to the chip for initiator operation only. To initiate a DMA Initiator Receive operation, the DMA Mode Bit (Register 22, Bit 1) and the DMA Enable Bit (Register 28, Bit 1) must be set, and the Target Mode Bit (Register 22, Bit 6) must not be set. Any value written to this register will start the DMA Initiator Receive Operation.

3.2 Buffer Control Registers

3.2.1 Memory Buffer Control Register - Address 28 (Read/Write)

The Memory Buffer Control Register controls SCSI DMA transfers. It also allows the microprocessor to access the buffer memory and contains the direction of transfer and end of DMA transfer information. Reading this register will strobe the contents of the RAP (Registers 2B and 2C) and WAP (Registers 2D and 2E) into their respective monitor registers.

Bit 7 - SCSI Transfer Started - Read Only

When set, this bit indicates that a SCSI transfer has started (at least one byte has been transferred). This bit is reset when either the STP (Registers 29 and 2A) is updated or the DMA Enable Bit is reset.

Bit 6 - Equal - Read Only

During DMA receive operations, this bit will be set when the STP is equal to the WAP. During DMA send operations, this bit will be set when the STP is equal to the RAP. This bit is reset when either the STP is updated or the DMA Enable Bit is reset.

Bit 5 - Status of SCSI ATN/ - Read Only

This bit reflects the status of the ATN/ Signal on the SCSI Bus. When this bit is set, ATN/ is active.

Bit 4 - Enable Attention Interrupt - Read/Write

When set, this bit enables the occurrence of an active SCSI ATN/ Signal to assert IRQ/. When reset, no IRQ/ will occur on the assertion of ATN/. This bit has no effect on the standard interrupt conditions detected within the 53C80 core.

Bit 3 - REOP - Read/Write

When set, this bit allows the Equal Bit to terminate a SCSI DMA operation by generating an internal 53C80 core End of DMA Transfer Process (EOP/) Signal. Resetting this bit will not generate an EOP/ when the Equal Bit is set. This bit can be used with the Enable EOP Interrupt Bit (Register 22, Bit 3) to signify the successful transfer of a block of data.

Bit 2 - Direction - Read/Write

This bit controls the direction of the data transfer. When set, the transfer direction is from the buffer to the 53C300. When reset, the transfer direction is from the 53C300 to the buffer. This bit should be set for DMA send operations and reset for DMA receive operations.

Bit 1 - DMA Enable - Read/Write

When set, this bit allows DMA transfers to occur. When reset, it prevents DMA transfers from occurring. When terminating a DMA transfer, this bit must be reset before resetting the DMA Mode Bit (Register 22, Bit 1).

Bit 0 - Access Memory - Read/Write

When set, this bit enables the microprocessor to access the buffer memory. The DMA Enable Bit must be reset, and the Direction Bit must be set when doing buffer memory reads and reset when doing buffer memory writes.

3.2.2 Stop Pointer (STP) Register - LSB - Address 29 (Read/Write)

The STP Registers contain the address of the last byte to be transferred to the buffer memory. This STP Register holds the LSB of the STP. This register must be written prior to writing the MSB (Register 2A).

3.2.3 STP Register - MSB - Address 2A (Read/Write)

This STP Register holds the MSB of the STP. Loading this location causes the STP (16 bit) to be updated to the new value now held within the STP Registers. When DMA is in progress, the value of the STP must not be incremented by less than two.

NOTE: Registers 2B to 2E have two parts. One part is the register itself , and the other part is a monitor register. When reading these registers, the value read is that of the monitor and not the register itself. In order to update the value in the monitor register to the present value of the actual register, a read of the Memory Buffer Control Register (Register 28) must be executed. This can be executed at any time while the DMA is in progress. Unlike the STP, either byte may be changed first, but the monitor register will not be changed until a read of Register 28 is performed.

3.2.4 Read Address Pointer (RAP) Register - LSB - Address 2B (Read/Write)

The RAP Registers contain the address in the buffer memory that will be read on the next read cycle. This RAP Register contains the LSB of the next buffer read address.

3.2.5 RAP Register - MSB - Address 2C (Read/Write)

This RAP Register contains the MSB of the next buffer read address.

3.2.6 Write Address Pointer (WAP) Register - LSB - Address 2D (Read/Write)

The WAP Registers contain the address in the buffer memory that will be written on the next write cycle. This WAP Register contains the LSB of the next buffer write address.

3.2.7 WAP Register - MSB - Address 2E (Read/Write)

This WAP Register contains the MSB of the next buffer write address.

3.2.8 Processor/Buffer Register - Address 2F (Read/Write)

The Processor/Buffer Register allows the microprocessor to access the buffer memory. It is important that the DMA Enable Bit (Register 28, Bit 1) is reset, and the Direction Bit (Register 28, Bit 2) is correctly written before accessing the memory. The procedure is as follows:

A. To read information from the buffer:

1. Stop all transfers from the peripheral controller and reset the DMA Enable Bit (Register 28, Bit 1).
2. Load the RAP (Registers 2B and 2C) with the buffer address to be read.
3. Set the Direction Bit (Register 28, Bit 2).
4. Set the Access Memory Bit (Register 28, Bit 0).
5. Read the byte from the Processor/Buffer Register (Register 2F). The RAP will automatically increment after the byte has been read.

B. To write information to the buffer:

1. Stop all transfers from the peripheral controller and reset the DMA Enable Bit (Register 28, Bit 1).
2. Load the WAP (Registers 2D and 2E) with the buffer address to be written.
3. Reset the Direction Bit (Register 28, Bit 2).

4. Set the Access Memory Bit (Register 28, Bit 0).
5. Write the byte to the Processor/Buffer Register (Register 2F). The WAP will automatically increment after the byte has been written to the buffer.

3.2.9 External Control Register - Address 30 (Read/Write)

The External Control Register monitors the status of three input pins and controls the status of four output pins on the chip.

Bit 7 - Not Used

Bit 6 - LED/ - Read/Write

When set, the open-drain LED/ Signal is driven low. Reading this bit reflects the status of this output.

Bit 5 - D2 - Read/Write

When set, the D2 Data Output Pin is driven high. Reading this bit reflects the status of this output.

Bit 4 - D1 - Read/Write

When set, the D1 Data Output Pin is driven high. Reading this bit reflects the status of this output.

Bit 3 - D0 - Read/Write

When set, the D0 Data Output Pin is driven high. Reading this bit reflects the status of this output.

Bit 2 - ID2/ - Read Only

This bit indicates the status of the SCSI ID2/ Input Pin. The SCSI ID0/-ID2/ Input Pins may contain the SCSI ID or can be general purpose input pins. When set, this bit indicates that ID2/ is active.

Bit 1 - ID1/ - Read Only

This bit indicates the status of the SCSI ID1/ Input Pin. When set, this bit indicates that ID1/ is active.

Bit 0 - ID0/ - Read Only

This bit indicates the status of the SCSI ID0/ Input Pin. When set, this bit indicates that ID0/ is active.

4. FUNCTIONAL DESCRIPTION

4.1 Reset Conditions

4.1.1 Hardware Chip Reset

The PORST/ Signal initializes the chip and clears all internal logic and control registers. This is a chip reset only and does not create a SCSI Bus reset condition.

4.1.2 SCSI Bus RST/ Received

When an active SCSI RST/ Signal is received, the IRQ/ Signal is asserted and the SCSI part of the chip is initialized. Registers 20 through 27 are cleared, but the Assert RST/ Bit (Register 21, Bit 7) remains unchanged.

4.1.3 SCSI Bus RST/ Issued

If the microprocessor sets the Assert RST/ Bit (Register 21, Bit 7), the RST/ Signal goes active on the SCSI Bus and an internal reset is performed. The SCSI part of the chip is initialized. Registers 20 through 27 are cleared, but the Assert RST/ Bit remains set. The RST/ Signal will continue to be active until the Assert RST/ Bit is reset or until a hardware reset occurs.

4.2 SCSI and Peripheral Request Prioritization

Both the SCSI interface and the peripheral controller can request a data transfer with the external buffer. When a DMA transfer is in operation, data is transferred to the buffer. If both a peripheral request and a SCSI interface request occur at the same time, the priority is given to the peripheral. The EXREQ/ Signal is sampled on the falling edge of CLKA/, and the internal 53C80 core DMA Request (DRQ) Signal is sampled on the rising edge of CLKA/. If the EXREQ/ Signal is active before DRQ becomes active, the EXREQ/ will be serviced first and the SCSI interface request is completed in the next available memory cycle. The DMA control interleaves SCSI and peripheral transfers. The peripheral requests are synchronous to the 53C300 clock (CLKA/, Pin 8), but the SCSI interface transfers are asynchronous.

4.3 Pointer Operation in Data Transfers

4.3.1 General Operation

Data transfers to the external buffer are controlled by three data transfer pointers: STP (Registers 29 and 2A), RAP (Registers 2B and 2C), and WAP (Registers 2D and 2E). The STP controls the number of data bytes being transferred. The RAP contains the read address of the buffer, and the WAP contains the write address of the buffer. When a DMA transfer occurs, one source will use the RAP and the other will use the WAP. The STP determines when the transfer will stop. For example, during a target receive operation, when the WAP is equal to the STP, the End of DMA Transfer Bit (Register 25, Bit 7) will be set indicating that all data received from the SCSI Data Bus has successfully been written to the buffer memory. Both the RAP and WAP are automatically advanced after a byte has been read/written into the buffer. The direction of the transfer is determined by the value of the Direction Bit (Register 28, Bit 2). If the Direction Bit is set, then data can be read from the buffer. If the Direction Bit is reset, then data can be written to the buffer.

During initiator or target DMA send operations, data is read from the buffer address as indicated by the current value of the RAP and latched in the Output Data Register (Register 20). During initiator or target DMA receive operations, data latched in the Input Data Register (Register 26) is written to the buffer address as indicated by the current value of the WAP.

4.3.2 SCSI Operation

When the SCSI Data Bus is ready to transfer data, an internal 53C80 core DMA Request (DRQ) Signal will become active. The data transfers from the SCSI Data Bus to the buffer can continue until the RAP or the WAP is equal to the STP. If the RAP or WAP is equal to the STP, then the Equal Bit (Register 28, Bit 6) will be set. The internal 53C80 core End of DMA Transfer Process (EOP/) Signal will be asserted if the REOP Bit (Register 28, Bit 3) is set. If the REOP Bit is set and the Equal Bit becomes set, then this condition will set the End of DMA Transfer Bit (Register 25, Bit 7) and assert IRQ/ if the Enable EOP Interrupt Bit (Register 22, Bit 3) is set. If the EXREQ/ Signal becomes active during a SCSI transfer, the peripheral controller request will be completed during the next available memory cycle.

4.3.3 Peripheral Operation

When the peripheral controller is ready to transfer data, it will assert EXREQ/. EXREQ/ must satisfy the setup time with respect to the CLKA/ Signal. Any current SCSI transfers will be completed. The peripheral controller request will be completed on the next available memory cycle. The buffer will be read/written at the current

address indicated by the RAP or the WAP. If the internal 53C80 core DMA Request (DRQ) Signal becomes active during a peripheral controller transfer, then the SCSI transfer will be completed on the next available memory cycle.

4.4 Microprocessor Access to Internal Registers

The microprocessor interface is compatible with Intel's 8-bit address/data multiplexed bus scheme. The microprocessor can read or write any of the internal registers to initiate SCSI Bus activity or to assert any one of the SCSI Bus signals. The microprocessor must write the desired register address to the Address/Data Bus (AD0-AD7, Pins 20-13), and then assert the PCS Signal. After the address has been latched on the falling edge of ALE, then a read or write can be executed by asserting the PRD/ Signal or the PWR/ Signal. For a register read, the data will appear on the Address/Data Bus after a read access time delay. For a register write, the data must satisfy the setup time before the rising edge of PWR/ to ensure that the data is properly written to the chip.

4.5 Microprocessor Access to the Buffer

The microprocessor can set up the buffer address pointers by accessing the internal registers as described above. Since the RAP, WAP, and STP Registers contain 16-bit addresses, the microprocessor must write to the chip twice to change the addresses. The microprocessor can monitor the DMA transfers by reading the RAP/WAP counters while the DMA is in progress. It can also advance the STP while a DMA transfer is taking place, but only by two or more. Access to the RAP/WAP/STP while a DMA transfer is in progress does not have an adverse effect on the DMA throughput rate.

The microprocessor can access a byte of data stored in the buffer by setting the Access Memory Bit (Register 28, Bit 0). The DMA Enable Bit (Register 28, Bit 1) must not be set. The RAP/WAP must be loaded with the correct address and the Direction Bit (Register 28, Bit 2) must be set for a read and not set for a write. The data can be obtained by reading/writing the Processor/Buffer Register (Register 2F). The RAP/WAP will automatically be incremented after each byte is read/written.

5. ELECTRICAL CHARACTERISTICS

5.1 D.C. Characteristics

5.1.1 Absolute Maximum Stress Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tstg	Storage Temperature	-55	150	°C
VDD	Supply Voltage	-0.5	7.0	V
VIN	Input Voltage	VSS - 0.5	VDD + 0.5	V
*ESD	Electrostatic Discharge (For all pads except SCSI)	-3000	3000	V
*ESD	Electrostatic Discharge (For all SCSI pads)	-4000	4000	V

*Tested using the human body model--100pF at 1.5kΩ

5.1.2 Operating Conditions

All timings and DC characteristics shall hold across the full range of temperature and voltage states below:

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply Voltage	4.75	5.25	V
IDD	Supply Current	0	25	mA
Ta	Operating Free-Air Temperature	0	70	°C
SRF	Signal Rise/Fall Time (SCSI pins)	8.0		ns

5.1.3 Microprocessor Interface Signals

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIL	Input Low Voltage	VSS - 0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VOL	Output Low Voltage	VSS	0.4	V	IOL = 3.20mA
VOH	Output High Voltage	2.4	VDD	V	IOH = -400uA
IOL	Output Low Current	4.0		mA	VOL = 0.4V
IOH	Output High Current	-2.0		mA	VOH = VDD - 0.5V
IIH	Input High Leakage	0	10	µA	VIN = VDD
IIL	Input Low Leakage	-10	0	µA	VIN = VSS

5.1.4 SCSI Signals

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIL	Input Low Voltage	VSS - 0.5	0.8	V	
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VOL	Output Low Voltage	VSS	0.5	V	IOL = 48mA
VHYS	Hysteresis	200		mV	
IOL	Output Low Current	48		mA	VOL = 0.5V
IIL	Input Low Leakage	-10	0	µA	VIN = VSS
IIH	Input High Leakage	0	10	µA	VIN = VDD

5.1.5 Address Lines A0-A7

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VOL	Output Low Voltage	VSS	0.4	V	IOL = 4.0mA
VOH	Output High Voltage	2.4	VDD	V	IOH = -400uA
IOL	Output Low Current	4.0		mA	VOUT = VSS
IOH	Output High Current	-2.0		mA	VOUT = VDD

5.1.6 Buffer Control and Address Lines

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VOL	Output Low Voltage	VSS	0.4	V	IOL = 4.0mA
VOH	Output High Voltage	2.4	VDD	V	IOH = -400uA
VIL	Input Low Voltage (HSD0-HSD7)	VSS - 0.5	0.8	V	
VIH	Input High Voltage (HSD0-HSD7)	2.0	VDD + 0.5	V	
IOL	Input Low Current	4.0		mA	VOL = 0.4V
IOH	Input High Current	-2.0		mA	VOH = VDD - 0.5V
IIH	Input High Leakage	0	10	µA	VIN = VDD
IIL	Input Low Leakage	-10	0	µA	VIN = VSS

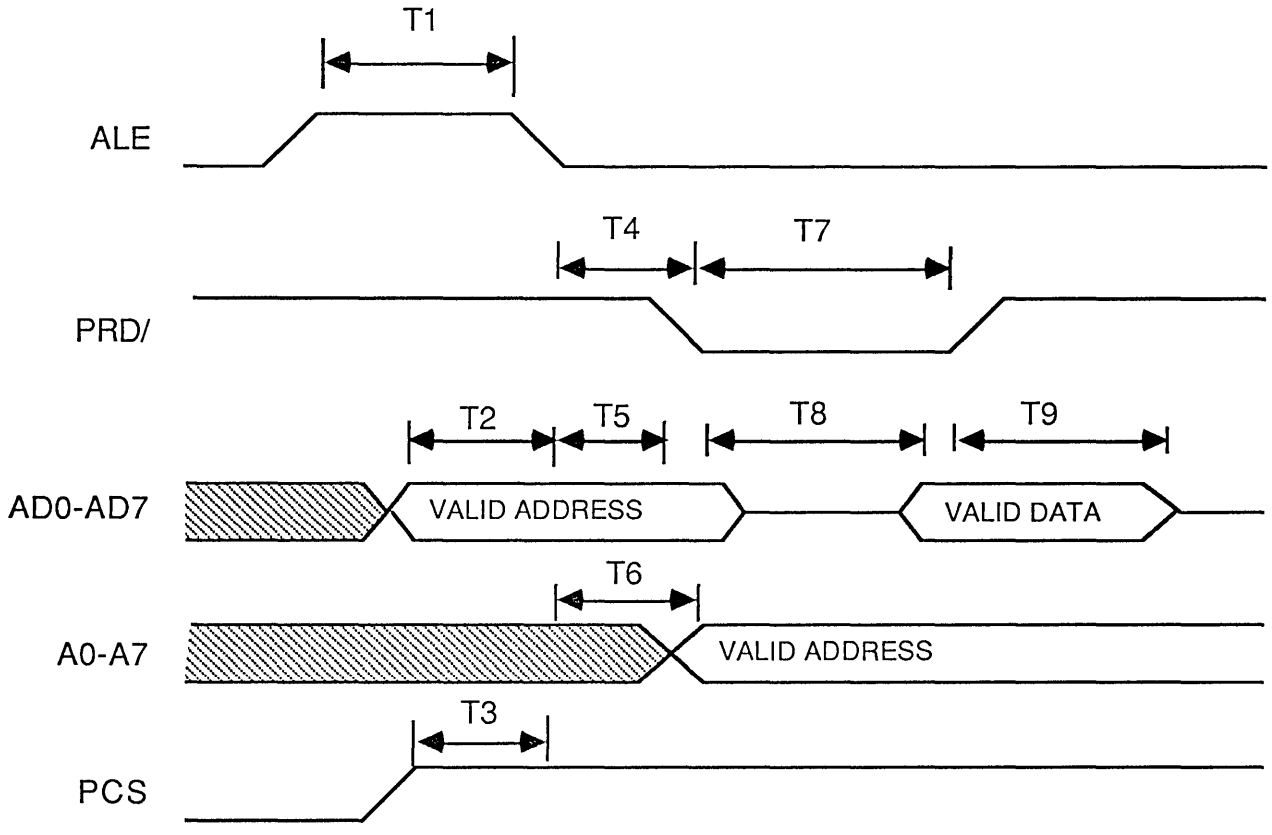
5.1.7 Miscellaneous Input and Output Pins

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
VIL	Input Low Voltage (PORST/, ID0-ID2/)	VSS - 0.5	0.8	V	
VIH	Input High Voltage (PORST/, ID0-ID2/)	2.0	VDD + 0.5	V	
VOL	Output Low Voltage (D0-D2)	VSS	0.4	V	IOL = 4mA
VOH	Output High Voltage (D0-D2)	2.4	VDD	V	IOH = -400uA
VOL	Output Low Voltage (LED/)	VSS	0.5	V	IOL = 48mA
IIH	Input High Leakage (PORST/, ID0/-ID2/, TP/)	0	10	µA	VIN = VDD
IIL	Input Low Leakage (Except ID0/-ID2/, TP/)	-10	0	µA	VIN = VSS
IIL	Input Low Leakage (ID0/-ID2/, TP/)	-800	-50	µA	VIN = VSS

5.2 A.C. Characteristics

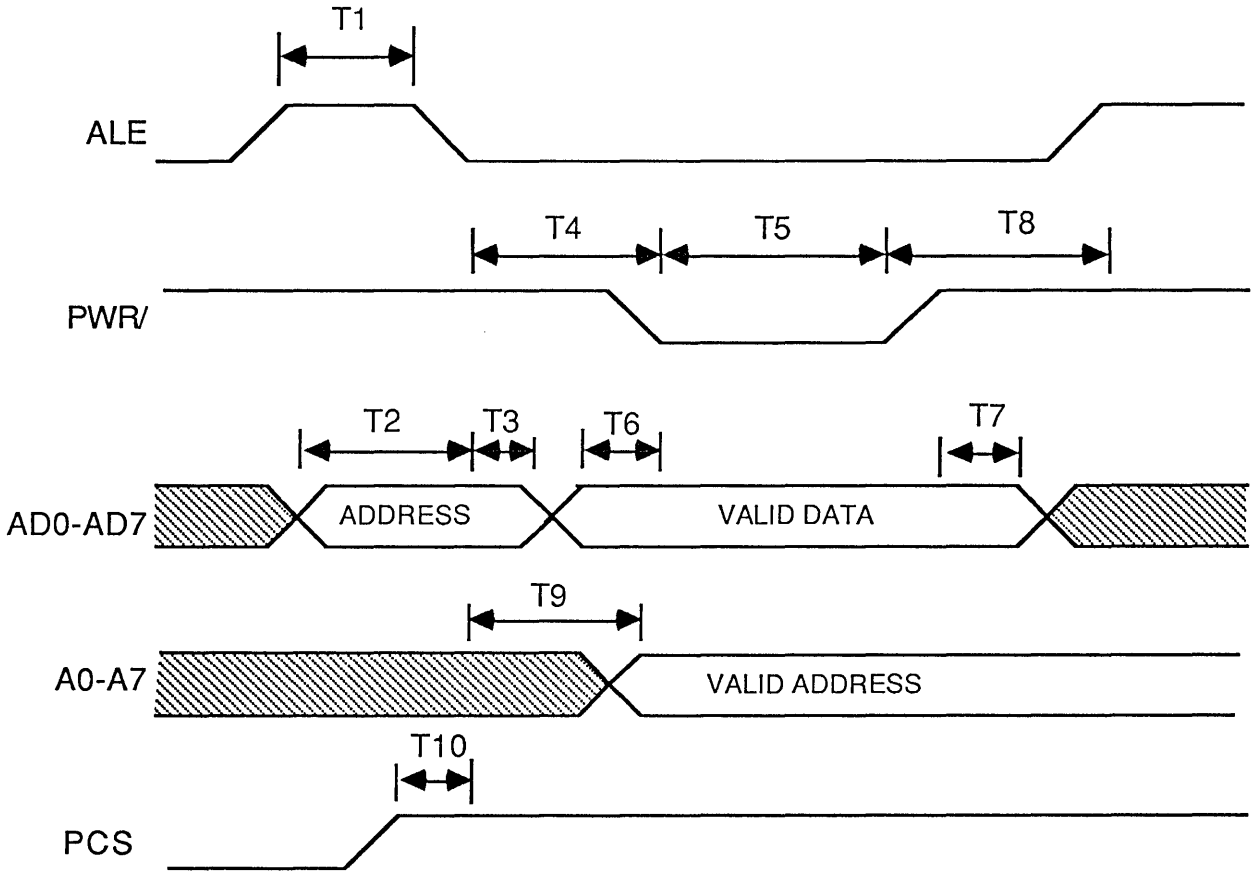
5.2.1 Microprocessor to Internal Register Read Timing

Symbol	Description	Min	Max	Unit
T1	ALE Pulse Width	60		ns
T2	Address Setup Time to ALE Low	5		ns
T3	PCS Setup Time to ALE Low	20		ns
T4	ALE Low to PRD/ or PWR/ Low	50		ns
T5	Address Hold after ALE Low	20		ns
T6	ALE Low to A0-A7 Address Valid		25	ns
T7	PRD/ Pulse Width	100		ns
T8	PRD/ Low to Valid Chip Data		100	ns
T9	Data Hold after PRD/	0	10	ns



5.2.2 Microprocessor to Internal Register Write Timing

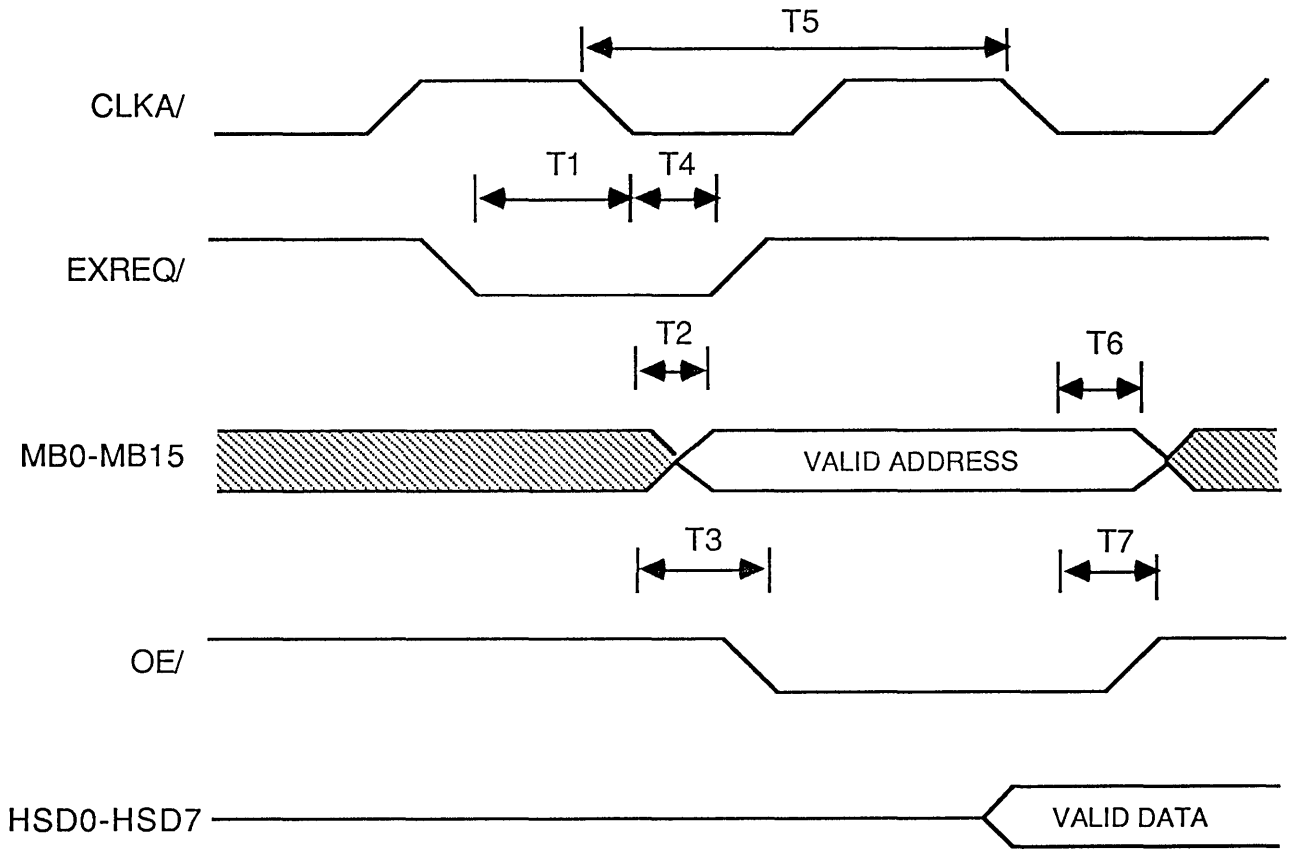
Symbol	Description	Min	Max	Unit
T1	ALE Pulse Width	60		ns
T2	Address Setup Time to ALE Low	5		ns
T3	Address Hold after ALE	20		ns
T4	ALE Low to PRD/ or PWR/ Low	50		ns
T5	PWR/ Pulse Width	100		ns
T6	Data Setup to PWR/ Transition	0		ns
T7	Data Hold after PWR/	12		ns
T8	PRD/ or PWR/ High to ALE High	20		ns
T9	ALE Low to A0-A7 Address Valid		25	ns
T10	PCS Setup Time to ALE Low	20		ns



5.2.3 Peripheral to Buffer Read Timing

Symbol	Description	Min	Max	Unit
T1	EXREQ/ Setup to CLKA/ Low	30		ns
T2	CLKA/ Low to New Address Valid		65	ns
T3	CLKA/ Low to OE/ Low		50	ns
T4	EXREQ/ Hold after CLKA/ Low	50	*	ns
T5	Period of CLKA/	200		ns
T6	CLKA/ Low to Address Invalid	15		ns
T7	CLKA/ Low to OE/ High	30	80	ns

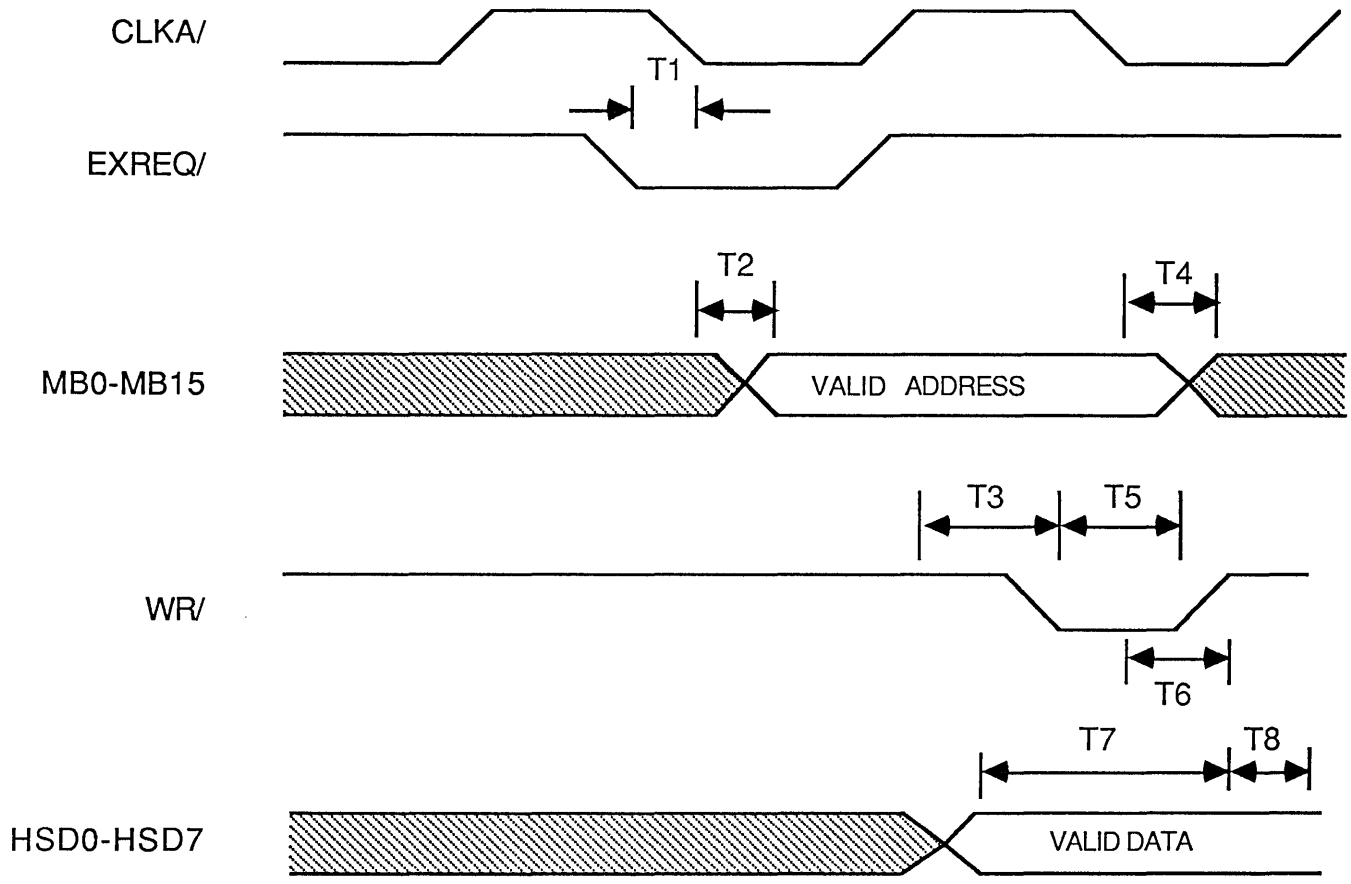
* (Period of CLKA/) - 30 ns



5.2.4 Peripheral to Buffer Write Timing

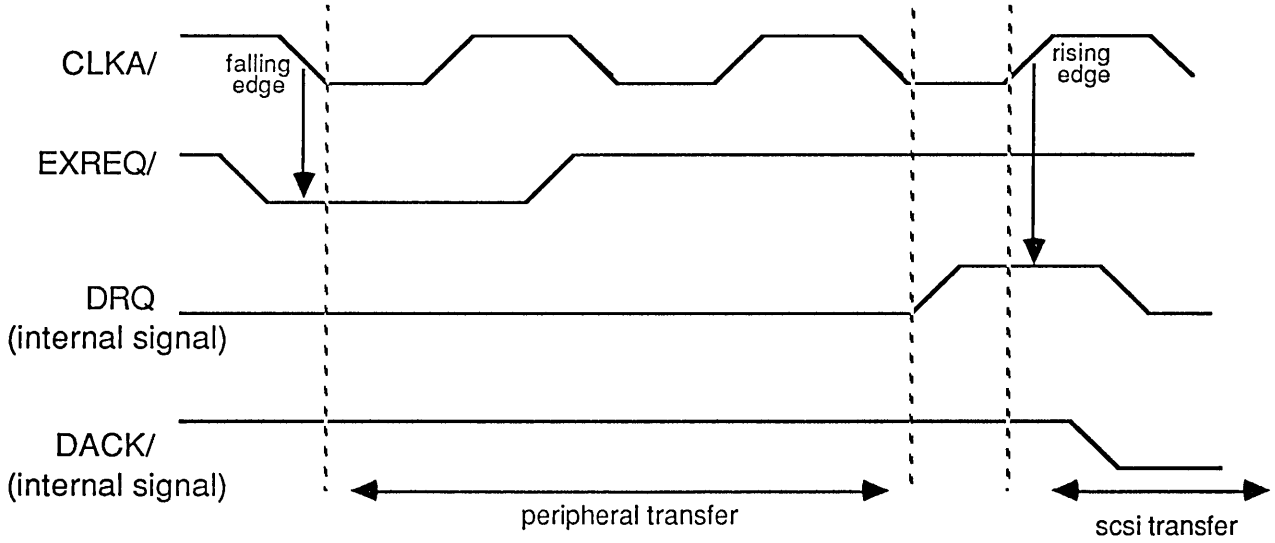
Symbol	Description	Min	Max	Unit
T1	EXREQ/ Setup Time to CLKA/ Low	30		ns
T2	CLKA/ Low to New Address Valid		65	ns
T3	CLKA/ High to WR/ Low		50	ns
T4	CLKA/ Low to Address Invalid	15		ns
T5	Width of WR/ Pulse	*	**	ns
T6	CLKA/ Low to WR/ High		50	ns
T7	Data Setup to WR/ High	***	***	ns
T8	Data Hold from WR/ High	***	***	ns

* (One-half of the period of CLKA/) - 10ns
** One half of the period of CLKA/
*** These timings depend on the characteristics of the memory device being used.

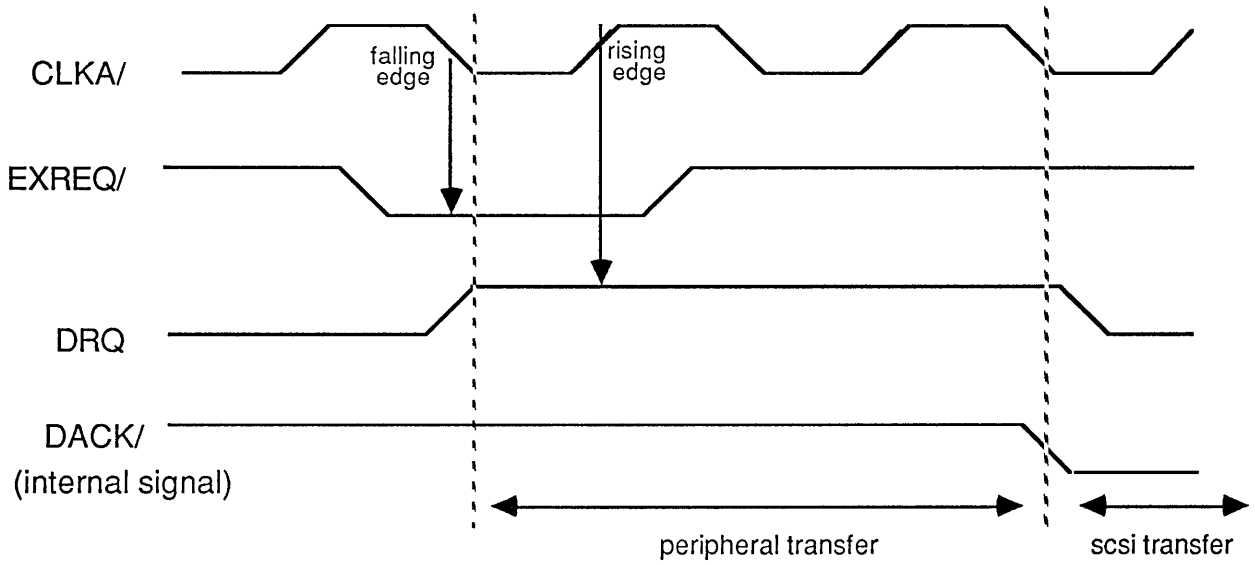


6. APPENDIX

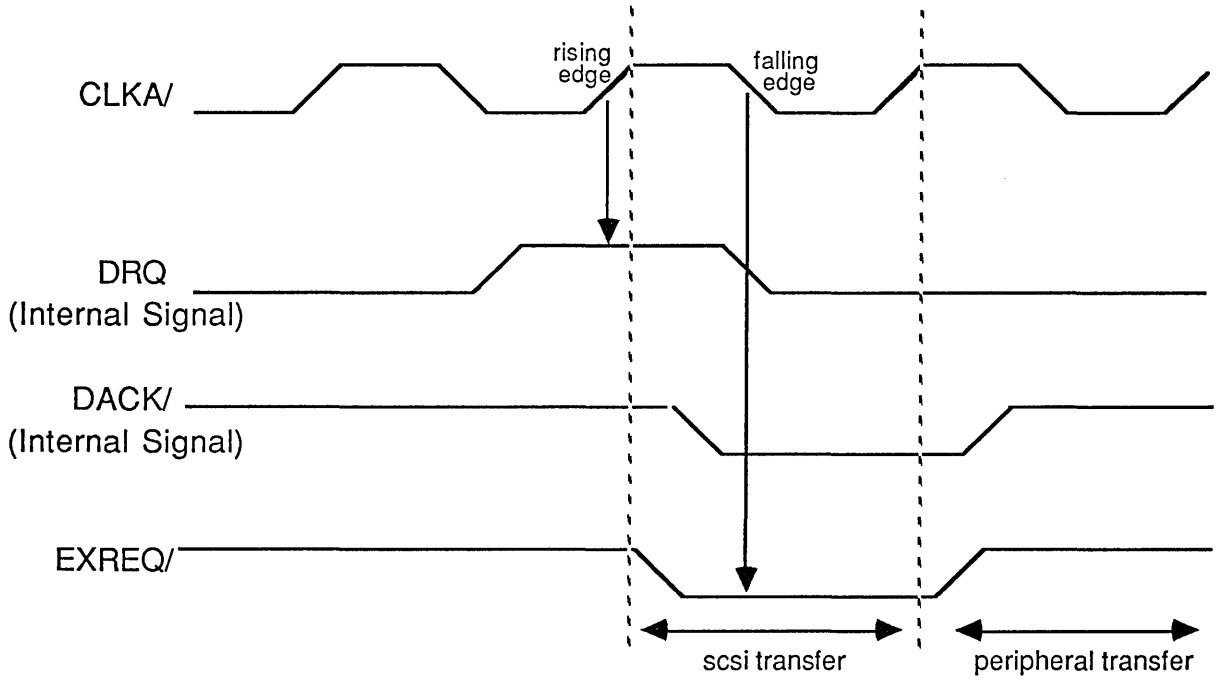
6.1 Data Transfer Request Prioritization



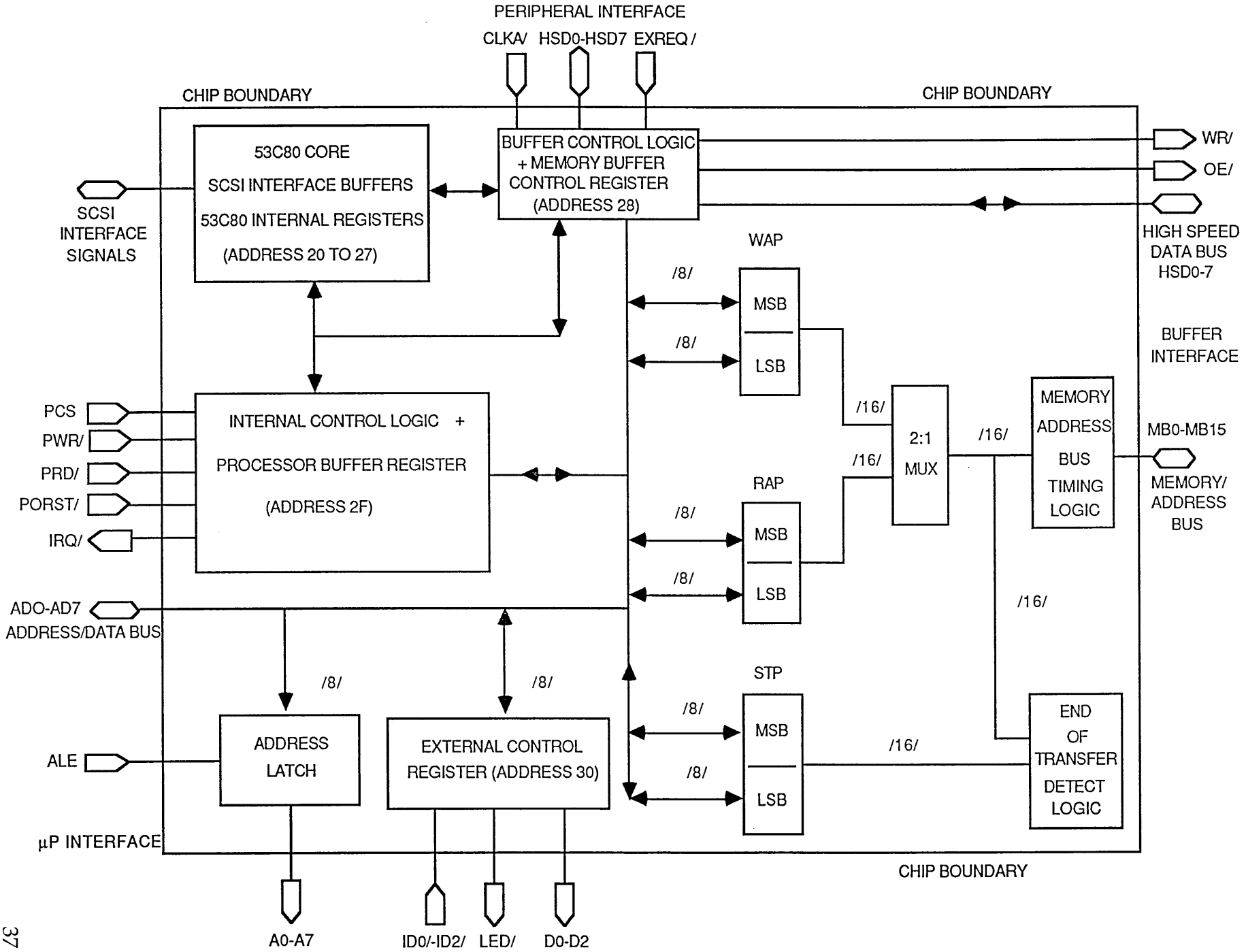
EXREQ/ is sampled on the falling edge of CLKA/. DRQ indicates an SCSI data transfer request. The DRQ Signal (internal to the chip) is sampled on the rising edge of CLKA/.



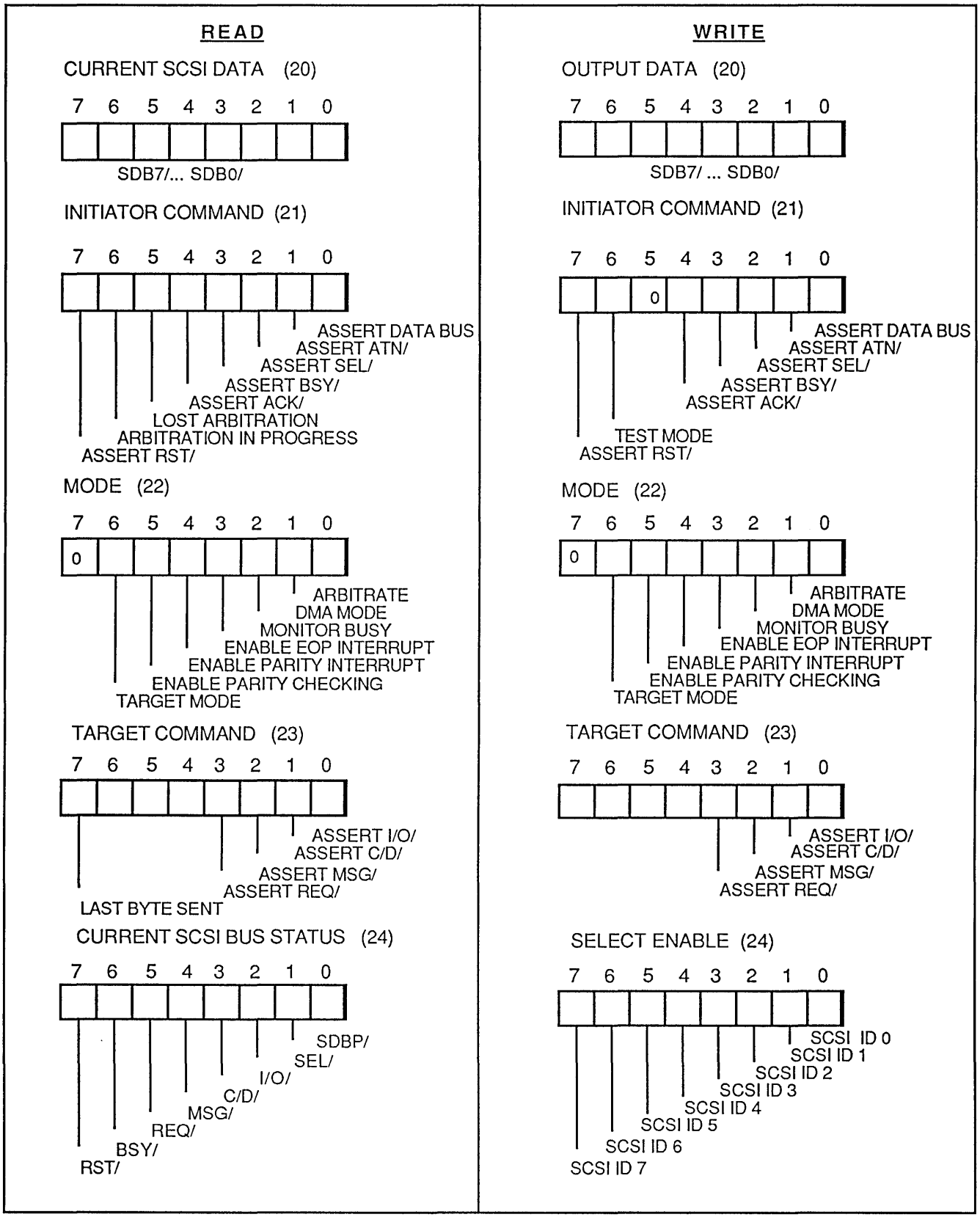
When an EXREQ/ is clocked on a falling edge of CLKA/ and a DRQ is clocked on the rising edge, priority is given to the signal that is detected first. When the EXREQ/ is given priority, the DRQ will be serviced after two clock cycles.



When a DRQ is clocked on a rising edge of CLKA/ and an EXREQ/ is clocked on the falling edge, priority is given to the signal that is detected first. When the DRQ is given priority, the EXREQ/ will be serviced after one clock cycle.

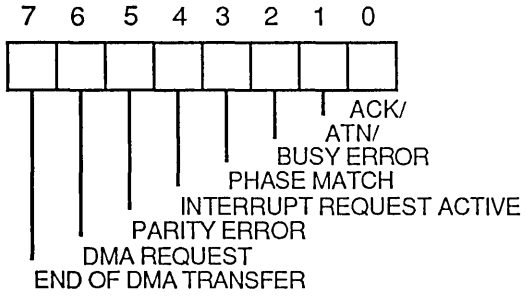

PERIPHERAL INTERFACE
CLKA/ HSD0-HSD7 EXREQ/
CHIP BOUNDARY
CHIP BOUNDARY
53C80 CORE
SCSI INTERFACE BUFFERS
53C80 INTERNAL REGISTERS
(ADDRESS 20 TO 27)
BUFFER CONTROL LOGIC
+ MEMORY BUFFER
CONTROL REGISTER
(ADDRESS 28)
SCSI
INTERFACE
SIGNALS
WR/
OE/
HIGH SPEED
DATA BUS
HSD0-7
BUFFER
INTERFACE
WAP
/8/
MSB
/8/
LSB
/16/
2:1
MUX
/16/
MEMORY
ADDRESS
BUS
TIMING
LOGIC
MB0-MB15
MEMORY/
ADDRESS
BUS
PCS
PWR/
PRD/
PORST/
IRQ/
INTERNAL CONTROL LOGIC +
PROCESSOR BUFFER REGISTER
(ADDRESS 2F)
RAP
/8/
MSB
/8/
LSB
/16/
ADO-AD7
ADDRESS/DATA BUS
/8/
/8/
STP
/8/
MSB
/8/
LSB
/16/
END
OF
TRANSFER
DETECT
LOGIC
ALE
ADDRESS
LATCH
EXTERNAL CONTROL
REGISTER (ADDRESS 30)
µP INTERFACE
CHIP BOUNDARY
A0-A7
ID0/-ID2/
LED/
D0-D2

6.3 Register Summary

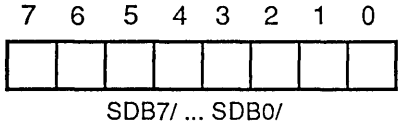


READ

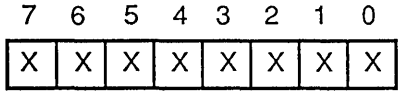
BUS AND STATUS (25)



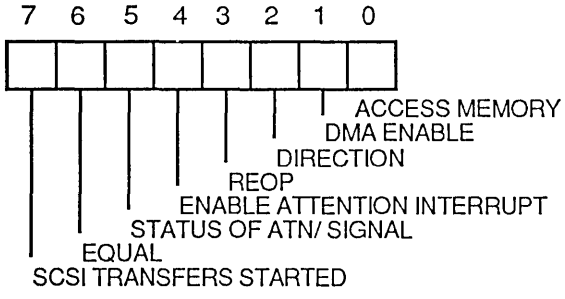
INPUT DATA (26)



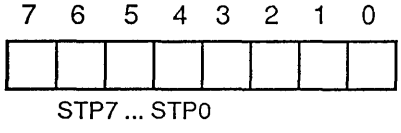
RESET PARITY / INTERRUPT (27)



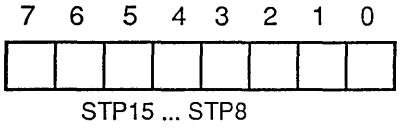
MEMORY BUFFER CONTROL (28)



STP (LSB) (29)

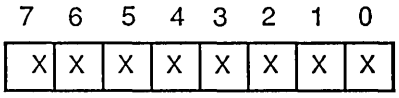


STP (MSB) (2A)

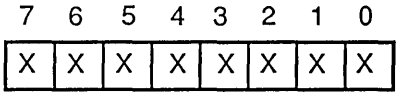


WRITE

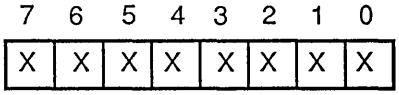
START DMA SEND (25)



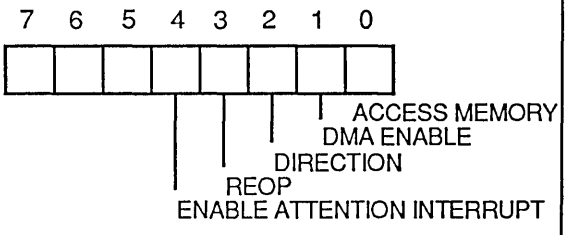
START DMA TARGET RECEIVE (26)



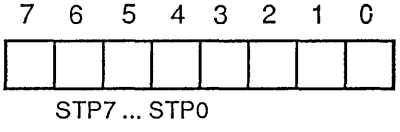
START DMA INITIATOR RECEIVE (27)



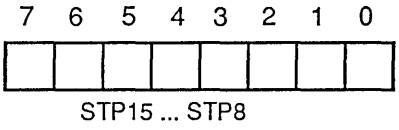
MEMORY BUFFER CONTROL (28)



STP (LSB) (29)



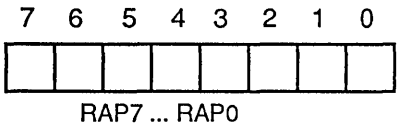
STP (MSB) (2A)



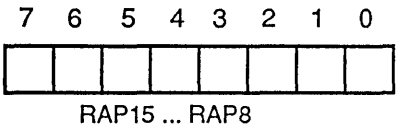
X = DON'T CARE

READ

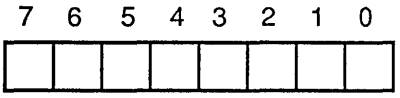
RAP (LSB) (2B)



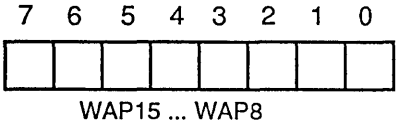
RAP (MSB) (2C)



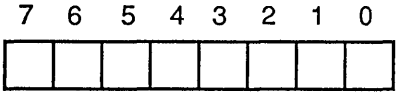
WAP (LSB) (2D)



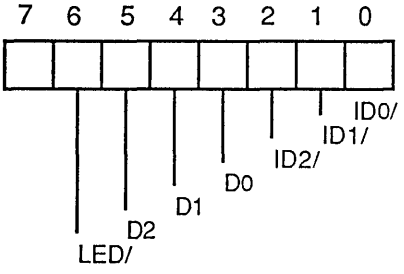
WAP (MSB) (2E)



PROCESSOR/BUFFER (2F)

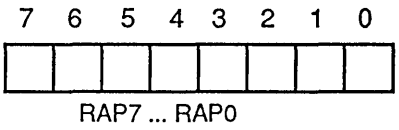


EXTERNAL CONTROL (30)

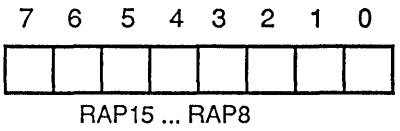


WRITE

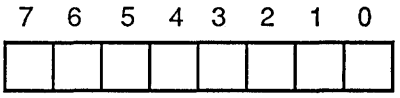
RAP (LSB) (2B)



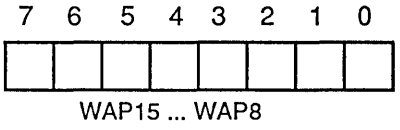
RAP (MSB) (2C)



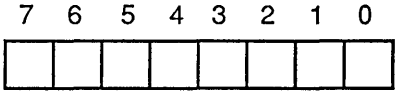
WAP (LSB) (2D)



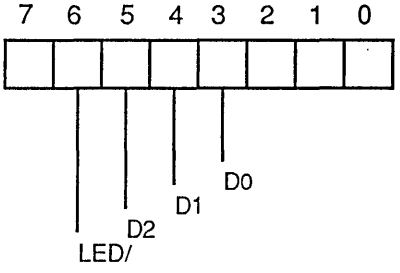
WAP (MSB) (2E)



PROCESSOR/BUFFER (2F)

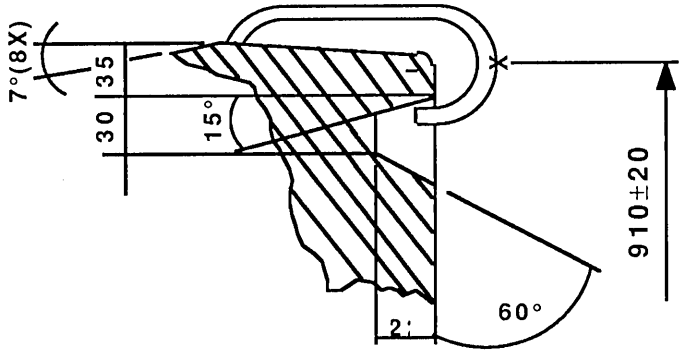


EXTERNAL CONTROL (30)



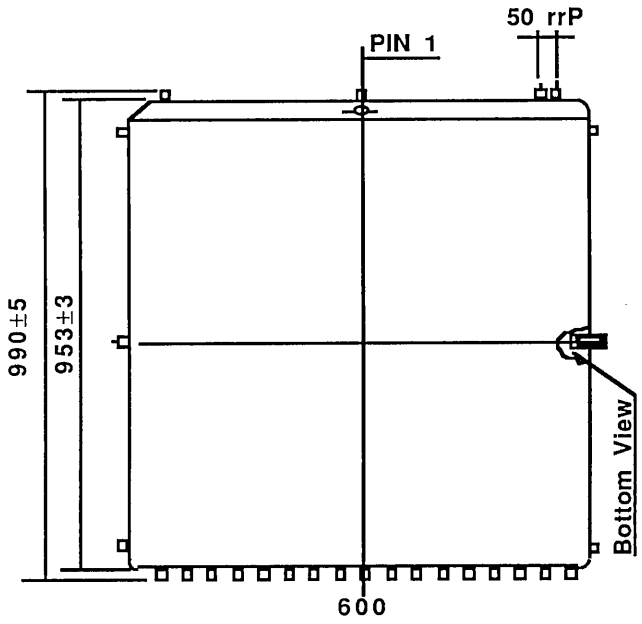
6.4 84 Pin PLCC Mechanical Drawing

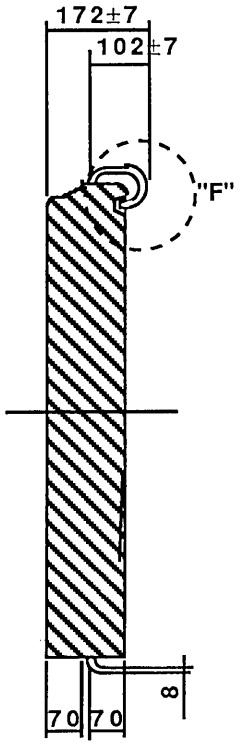
Note: All units are 1/1000 inches

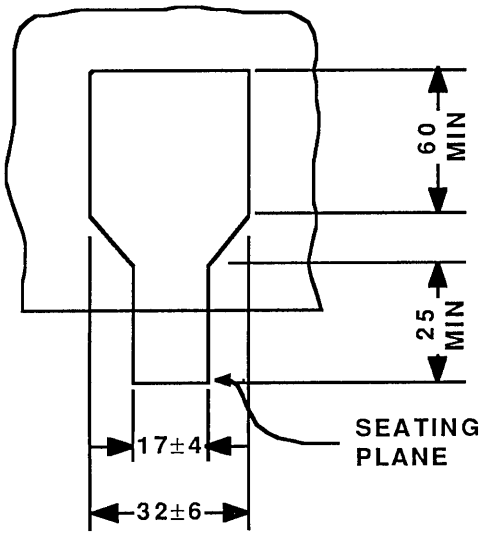


DETAIL OF "F"

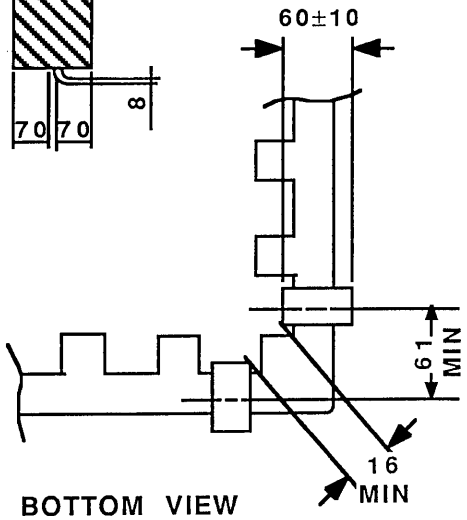
X: SURFACE MOUNT POINT







SIDE VIEW



BOTTOM VIEW

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