INS4001 ROM & I/O port, INS4002-1 RAM, INS4003 shift register INS4004 CPU, four-bit integrated processing system INS4008/INS4009 in a four-bit integrated processing system (FIPS)

general description

FIPS is a four-bit, general-purpose microprocessor chip set designed for application in intelligent terminals, traffic signals, measuring instruments, numeric control and process control systems. It interfaces easily with switches, keyboards, displays, and other peripheral devices; and it provides a compact and powerful replacement for random logic in many control systems.

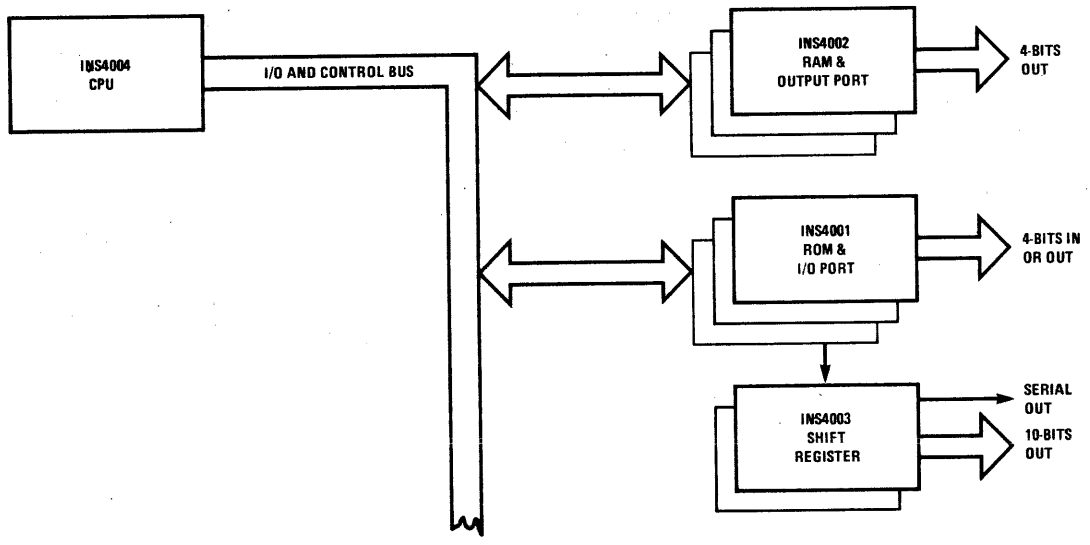
INS4002, INS4003, and INS4004 are standard building blocks for system control, I/O, and temporary data storage. The INS4001 ROM is mask-programmed to customer specifications and holds the application program for the FIPS controller. The FIPS microprocessor can interface directly with up to 4K x 8 of ROM, 1280 x 4 RAM, and 128 I/O lines. A small amount of additional logic will interface FIPS with up to 48 RAM or ROM packages in any combination, and 192 I/O lines. The minimum system configuration consists of one CPU and one ROM.

The National Semiconductor FIPS microprocessor is fabricated from PMOS, Silicon-gate technology for high reliability and producibility. Its powerful instruction set includes binary and decimal arithmetic, conditional branch, and indirect addressing instructions.

features

- General purpose programmable microprocessor
- 45 instructions, including:
  - Conditional Branch
  - Indirect Fetch
  - Binary/Decimal Arithmetic
- Easy memory expansion to 32K bits of ROM and 4K bits of RAM
- 16-pin dual in-line package allows compact designs
- Parallel operation for higher performance
- Simple memory and I/O interface for low system cost
- Second source for the MCS-4* microprocessor chips 4001, 4002-1, 4002-2, 4003, and 4004

block diagram-FIPS microprocessor chip set



*MCS-4 is a registered trademark of INTEL Corp.

INS4001 ROM &I/O port, INS4002-1 RAM, INS4003 shift register
INS4004 CPU, four-bit integrated processing system
INS4008/INS4009 in a four-bit integrated processing system (FIPS)

INS4001 256×8 bit mask-programmed ROM and 4-bit I/O port

The INS4001 is a 2K metal-mask ROM which interfaces directly to the INS4004 CPU and is used to store the control program for the FIPS system. Its address decoding capability is also used to control the selection of a built-in 4-bit I/O port. Data is transferred between the ROM and the CPU via a time-multiplexed, 4-bit Data Bus.

ROM OPERATION

During ROM access, 12-bit addresses and 8-bit data words are multiplexed onto the 4-bit Data Bus connecting the INS4001 with the CPU. (See FIPS Basic Instruction Cycle Timing Diagram). During the three address periods following a SYNC command from the CPU, addresses which select one of 256 words per ROM, and one of 16 ROM chips, are passed to the INS4001. During the next two time periods, 8 bits of instruction are transferred from the ROM to the CPU. A command signal (CM) is provided from the CPU, and is used to select a ROM bank (group of 16 ROMs).

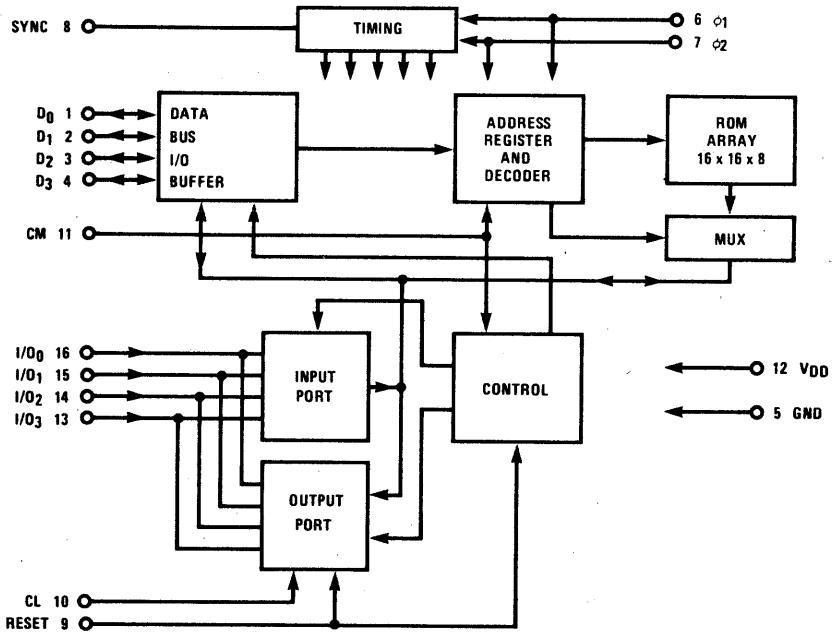
I/O PORT OPERATION

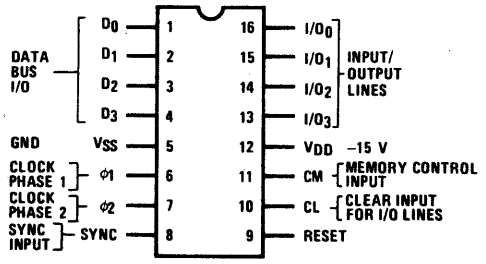
In this mode of operation, the chip routes data directly between the Data Bus and a 4-bit I/O port which is part of the chip. Each chip has the capability to identify itself for I/O operations, and to recognize and execute I/O commands from the CPU. An external signal (CL) may be applied to asynchronously clear the output register during normal operation.

All internal flip-flops will be reset when the RESET line goes low (negative voltage).

Each I/O pin can be selected as an input or output line by metal mask option. Inputs and outputs may be selected as direct or inverted. An on-chip resistor tying the inputs to either V_{DD} or V_{SS} is also optional.

block and connection diagrams





INS4002 320-bit RAM and 4-bit output port

The INS4002 combines the functions of 4-bit parallel read/write data storage and 4-bit output/control lines which facilitate data transfer between the CPU and a peripheral device.

RAM OPERATION

RAM storage in the INS4002 is organized as 4 registers of 20 4-bit characters each (16 main memory and 4 status characters). Main memory locations are selected during an SRC instruction, while status locations are selected during the actual I/O or RAM instruction.

When doing a RAM data transfer, the CPU first executes an SRC instruction, which sends out the contents of the designated index register pair (X_2 X_3) as an address to the RAM. These bits are decoded as shown in the diagram below.

X_2				X_3			
D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0
Chip # (0-3)		Register # (0-3)		Main Memory Character # (0-15)			

Selection of different RAM chips is based upon a metal-mask address option (INS4002-1 or INS4002-2) and an external pin, P_O, which may be wired to either V_{DD} or V_{SS}. Decoding is as shown below:

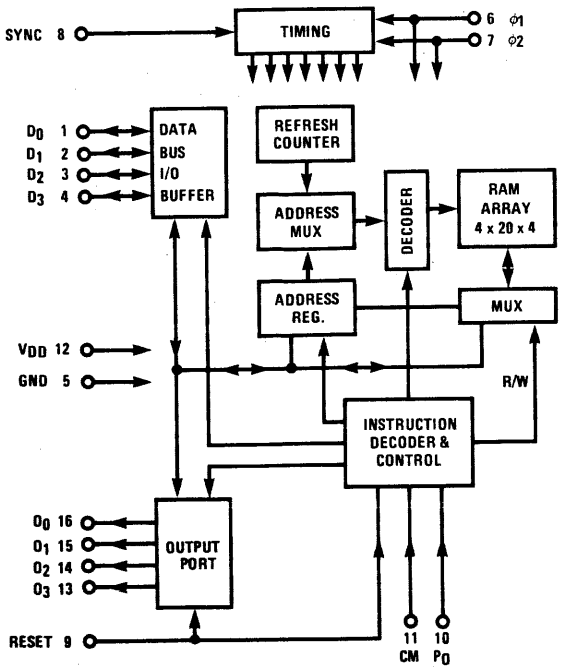
CHIP #	OPTION	P_O	D_3	D_2
0	INS4002-1	GND	0	0
1	INS4002-1	V_{DD}	0	1
2	INS4002-2	GND	1	0
3	INS4002-2	V_{DD}	1	1

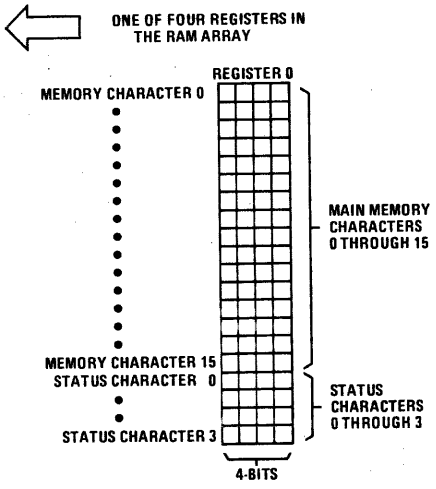
Timing is based upon two externally-supplied clock signals, and a SYNC signal provided by the CPU. Internal refresh circuitry maintains memory data in the cells of the chip.

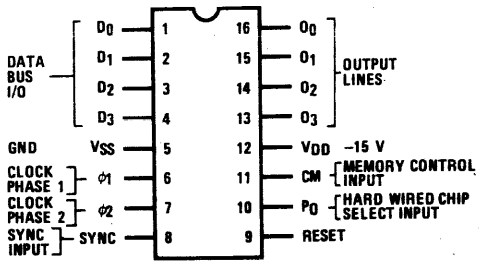
OUTPUT PORT OPERATION

The INS4002 has the capability to transfer data directly from the system Data Bus through a 4-bit Output Port to an external peripheral device. When the external RESET line goes low, the memory and all static flip-flops are cleared. To completely clear memory, the RESET line must be held low for at least 32 memory cycles (32 x 8 clock periods).

block and connection diagrams







INS4003 10-bit serial-in/parallel-out shift register

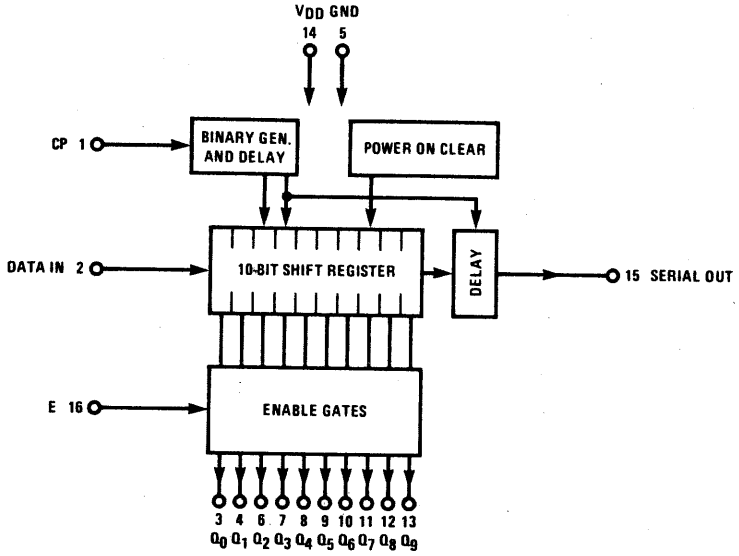
The INS4003 10-bit static shift register is used to increase the number of output lines available from the microprocessor system to interface with peripheral devices.

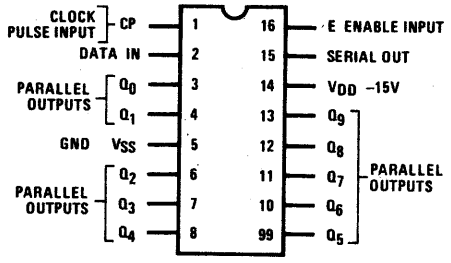
Data is loaded serially into the Shift Register, and is then available in parallel on 10 output lines which can be accessed through enable logic. When the ENABLE line (E) is low, shift register contents are available at pins Q_0 - Q_9. When E is high, these pins are at V_{SS}.

A Serial-Data-Out line is also available from the Shift Register, and it allows an indefinite number of Shift Registers to be cascaded together to provide any required number of output lines, in multiples of 10. This serial output line is not affected by the E line.

Data is clocked through the Shift Register by a signal on the CP line. An internal initialization circuit clears the shift register between the application of the supply voltage and the first CP signal.

block and connection diagrams





INS4004 4-bit central processing unit (CPU)

The INS4004 is the Central Processing Unit of the FIPS microprocessor system. It includes the necessary control logic to request program instructions from main memory (INS4001 ROMs), decode the instructions and execute them. It is designed to interface directly with the INS4001, INS4002, and INS4003 chips. Communication with the outside world is accomplished through I/O ports included in these chips.

The CPU itself consists of a 4-bit ALU, 16 4-bit index registers, a 12-bit program counter (PC), three levels of PC stack, an instruction register, and miscellaneous control logic. Communication with other chips is accomplished over a time-multiplexed 4-bit Data Bus.

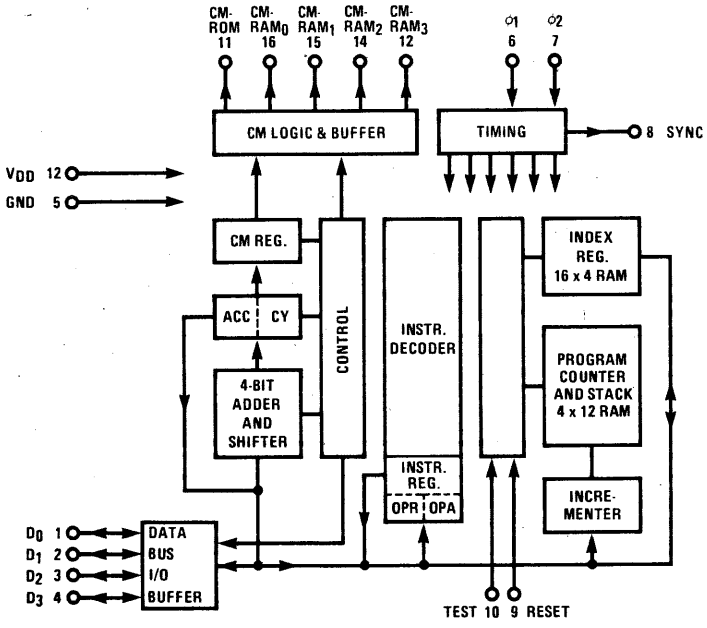
In operation, the CPU sends a SYNC signal to the ROMs and RAMs in the system, followed by 12 bits of address data (during the next three clock cycles), to select the next instruction to be executed. The selected ROM sends back 8 bits of instruction during the following two clock times, and this information is stored in the OPR and OPA registers within the CPU. The CPU executes the instruction during the next three clock times.

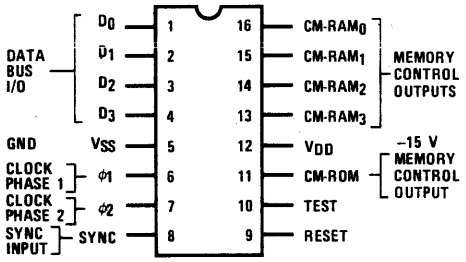
CPU instructions are drawn from the INS4001 ROMs, arranged in banks of 16 ROMs each. Bank switching is done under program control, with the CPU selectively enabling one bank of ROMs to fetch an instruction.

The CPU provides a Conditional Jump instruction which is used to test an external input pin. A RESET signal may be supplied to the CPU to clear all registers and flip-flops. After RESET, the program will start from step "0," executing program instructions.

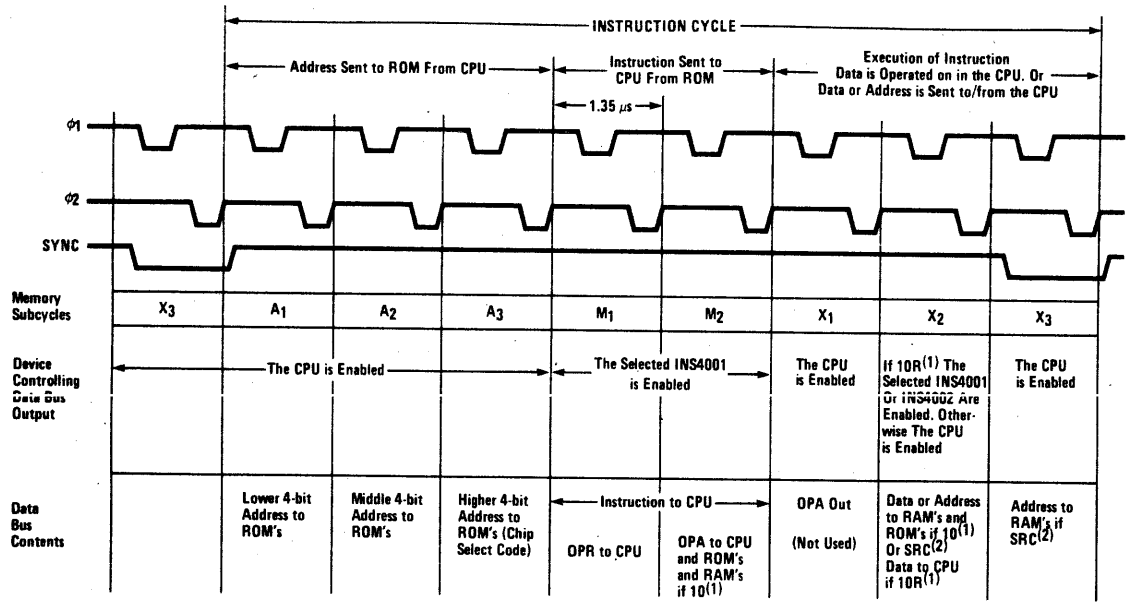
The INS4004 CPU provides a total of 45 program instructions, which are specified in the table on the following page.

block and connection diagrams





system timing



FIPS Basic Instruction Cycle

instruction set

[Those instructions preceded by an asterisk (*) are 2 word instructions that occupy 2 successive locations in ROM]

MACHINE INSTRUCTIONS

MNEMONIC	OPR	OPA	DESCRIPTION OF OPERATION
NOP	0 0 0 0	0 0 0 0	No operation.
*JCN	0 0 0 1 A_2 A_2 A_2 A_2	C_1 C_2 C_3 C_4 A_1 A_1 A_1 A_1	Jump to ROM address A_2 A_2 A_2 A_2, A_1 A_1 A_1 A_1 (within the same ROM that contains this JCN instruction) if condition C_1 C_2 C_3 C_4(1) is true, otherwise skip (go to the next Instruction in sequence).
*FIM	0 0 1 0 D_2 D_2 D_2 D_2	R R R 0 D_1 D_1 D_1 D_1	Fetch immediate (direct) from ROM Data D_2, D_1 to index register pair location RRR.(2)
SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the Instruction Cycle.
FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the Instruction Cycle.
*JUN	0 1 0 0 A_2 A_2 A_2 A_2	A_3 A_3 A_3 A_3 A_1 A_1 A_1 A_1	Jump unconditional to ROM address A_3, A_2, A_1.
*JMS	0 1 0 1 A_2 A_2 A_2 A_2	A_3 A_3 A_3 A_3 A A A A	Jump to subroutine ROM address A_3, A_2, A_1, save old address. (Up 1 level in stack.)
INC	0 1 1 0	R R R R	Increment contents of register RRRR.(3)
*ISZ	0 1 1 1 A_2 A_2 A_2 A_2	R R R R A_1 A_1 A_1 A_1	Increment contents of register RRRR. Go to ROM address A_2, A_1 (within the same ROM that contains this ISZ instruction) if result ≠ 0, otherwise skip (go to the next instruction in sequence).
ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.

input/output and RAM instructions

[The RAM's and ROM's operated on in the I/O and RAM instructions have been previously selected by the last SRC instruction executed.]

MNEMONIC	OPR	OPA	DESCRIPTION OF OPERATION
WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
WRϕ[4]	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
WR1[4]	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
WR2[4]	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
WR3[4]	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
RDϕ[4]	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
RD1[4]	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
RD2[4]	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
RD3[4]	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

accumulator group instructions

CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
CLC	1 1 1 1	0 0 0 1	Clear carry.
IAC	1 1 1 1	0 0 1 0	Increment accumulator.
CMC	1 1 1 1	0 0 1 1	Complement carry.
CMA	1 1 1 1	0 1 0 0	Complement accumulator.
RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
STC	1 1 1 1	1 0 1 0	Set carry.
DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
DCL	1 1 1 1	1 1 0 1	Designate command line.

NOTES: (1) The condition code is assigned as follows:

$C_1 = 1$ Invert jump condition
$C_1 = 0$ Not invert jump condition
$C_2 = 1$ Jump if accumulator is zero
$C_3 = 1$ Jump if carry/link is a 1
$C_4 = 1$ Jump if test signal is a 0

(2) RRR is the address of 1 of 8 index register pairs in the CPU.

(3) RRRR is the address of 1 of 16 index registers in the CPU.

(4) Each RAM chip has 4 registers, each with twenty 4-bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (OPA).

absolute maximum ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage with Respect to V_{SS}	+0.5 to −20 V
Power Dissipation	1.0 W

***Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

d.c. and operating characteristics

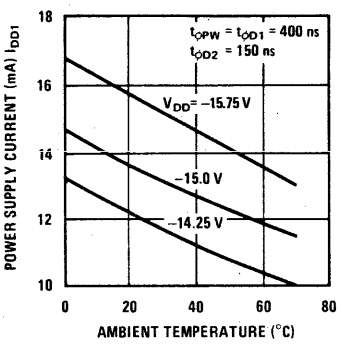
T_A = 0°C to +70°C; V_{DD} = −15 V ±5%, V_{SS} = GND, $t_{\phi PW} = t_{\phi D1}$ = 400 ns, $t_{\phi D2}$ = 150 ns, unless otherwise specified. Logic "0" is defined as the more positive voltage (V_{IH},V_{OH}), Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}).

PRODUCT	SYMBOL	PARAMETER	LIMIT MIN.	LIMIT TYP.(1)	LIMIT MAX.	UNIT	TEST CONDITIONS
SUPPLY CURRENT							
INS4001	I_{DD1}	Average Supply Current		15	30	mA	T_A = 25°C
INS4002	I_{DD2}	Average Supply Current		17	33	mA	T_A = 25°C
INS4003	I_{DD3}	Average Supply Current		5.0	8.5	mA	$t_{WL} = t_{WH}$ = 8 µsec; T_A = 25°C
INS4004	I_{DD4}	Average Supply Current		30	40	mA	T_A = 25°C
INPUT CHARACTERISTICS(ALL INPUTS EXCEPT I/O INPUT PINS)							
INS4001/2/4	I_{LI}	Input Leakage Current			10	µA	$V_{IL} = V_{DD}$
INS4001/2/4	V_{IH}	Input High Voltage (Except Clocks)	V_{SS}−1.5		V_{SS}+0.3	V	
INS4001/2/4	V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}−5.5	V	
INS4001/2/4	V_{ILC}	Clock Input Low Voltage	V_{DD}		V_{SS}−13.4	V	
INS4001/2/4	V_{IHC}	Clock Input High Voltage	V_{SS}−1.5		V_{SS}+0.3	V	
OUTPUT CHARACTERISTICS (ALL OUTPUTS EXCEPT I/O OUTPUT PINS)							
INS4001/2/4	I_{LO}	Data Bus Output Leakage Current			10	µA	V_{OUT} = −12V, Chip disabled
INS4001/2/4	V_{OH}	Output High Voltage		V_{SS}	V_{SS}−0.5	V	Driving 4000 Series loads only
INS4001/2/4	I_{OL1}	Data Lines Sinking Current "1" Level	10	18		mA	V_{OUT} = 0V
INS4004	I_{OL5}	CM-ROM Sinking Current "1" Level	6.5	12		mA	V_{OUT} = 0V
INS4004	I_{OL6}	CM-RAM Lines Sinking Current "1" Level	2.5	4		mA	V_{OUT} = 0V
INS4001/2/4	V_{OL1}	Data Lines, CM Lines, Sync Output Low Voltage	V_{SS}−12	V_{SS}−10	V_{SS}−6.5	V	I_{OL1} = 500 µA
INS4001/2/4	R_{OH1}	Output Resistance Data Data Lines "0" Level		150	250	Ω	V_{OUT} = 0.5 V
INS4004	R_{OH5}	CM-ROM Output Resistance "0" Level		320	600	Ω	V_{OUT} = −0.5 V
INS4004	R_{OH6}	CM-RAM Lines Output Resistance "0" Level		1.1	1.8	KΩ	V_{OUT} = −0.5 V
I/O INPUT CHARACTERISTICS							
INS4001/3	I_{LI}	Input Leakage Current			10	µA	$V_{IL} = V_{DD}$
INS4001/3	V_{IH}	Input High Voltage	V_{SS}−1.5		V_{SS}+0.3	V	
INS4001/3	V_{IL}(2)	Input Low Voltage	V_{DD}		V_{SS}−4.2	V	
INS4001	R_I	I/O Pins Input Resistance	10	18	35	KΩ	Internal input resistor is optional
I/O OUTPUT CHARACTERISTICS							
INS4001/2	I_{OL2}	I/O Output Line Sinking Current, "1" Level	2.5	5		mA	V_{OUT} = 0V. For T^2L compatibility a 12KΩ (±10%) resistor between output and V_{DD} should be added(3).
INS4003	I_{OL3}	Parallel Out Pins Sinking Current, "1" Level	0.6	1.0		mA	V_{OUT} = 0V. For T^2L compatibility a 5.6KΩ (±10%) resistor between output and V_{DD} should be added(3).
INS4003	I_{OL4}	Serial Out Sinking Current, "1" Level	1.0	2.0		mA	V_{OUT} = 0V
INS4001/2	V_{OL2}	I/O Output Lines Output Low Voltage	V_{SS}−12	V_{SS}−7.5	V_{SS}−6.5	V	I_{OL2} = 50 µA
INS4003	V_{OL3}	Output Low Voltage	V_{SS}−11	V_{SS}−7.5	V_{SS}−6.5	V	I_{OL3} = 10 µA
INS4001/2	R_{OH2}	Output Resistance I/O Lines "0" Level		1.2	1.8	KΩ	V_{OUT} = −0.5 V
INS4003	R_{OH3}	Parallel-Out Pins Output Resistance "0" Level		400	750	Ω	V_{OUT} = −0.5 V
INS4003	R_{OH4}	Serial Out Output Resistance "0" Level		650	1200	Ω	V_{OUT} = −0.5 V

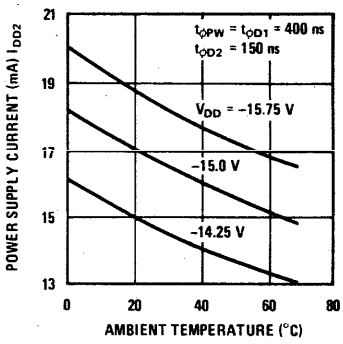
Note 1: Typical values are for T_A = 25°C and Nominal Voltages.
Note 2: If non-inverting input option is used, V_{IL} = −6.5 Volts maximum.
Note 3: For T^2L compatibility on the I/O lines the supply voltages should be V_{DD} = −10 V ±5%, V_{SS} = +5 V ±5%.

typical d.c. characteristics

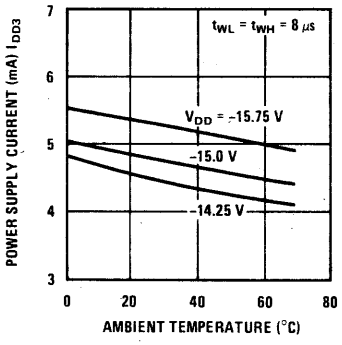
Power Supply Current vs Temperature (INS4001)



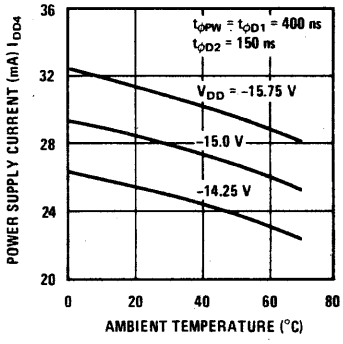
Power Supply Current vs Temperature (INS4002)



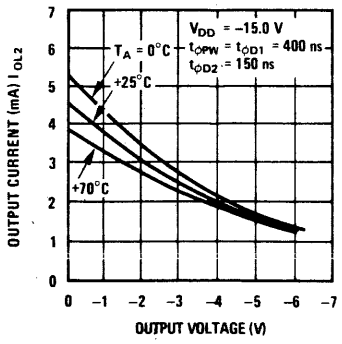
Power Supply Current vs Temperature (INS4003)



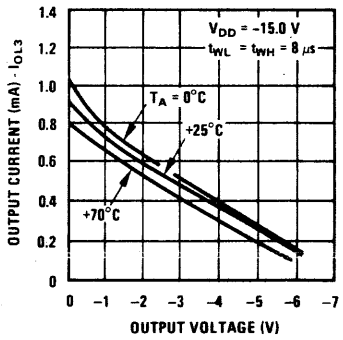
Power Supply Current vs Temperature (INS4004)



Output Current vs Output Voltage (INS4001, INS4002)



Output Current vs Output Voltage (INS4003)



system timing instruction set T_A = 0°C to +70°C; V_{DD} = −15 V ±5%, V_{SS} = GND

PRODUCT	SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
INS4001/2/4	t_{cy}	Clock Period	1.35	2	μs	
	$t_{\phi R}$ $t_{\phi F}$	Clock Rise and Fall Times		50	ns	
	$t_{\phi PW}$	Clock Width	380	480	ns	
	$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	400	550	ns	
	$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	150		ns	
	t_W	Data-In Write Time	350		ns	
	t_H	Data-In Hold Time	40		ns	
	t_{OS}(1)	Set Time for Data Out, SYNC, CM-ROM, (2)CM-RAM, (2)Lines	0		ns	C_{OUT} = 500 pF for data lines 500 pF for SYNC 160 pF for CM-ROM 50 pF for CM-RAM
	t_{OH}	Holdtime for Data Out, Sync, CM-ROM, CM-RAM Lines	50		ns	C_{OUT} = 20 pF
	$t_R t_F$	Rise and Fall Times for Data Out, SYNC, CM-ROM, CM-RAM Lines		500	ns	C_{OUT} = 500 pF for data lines 500 pF for SYNC 160 pF for CM-ROM 50 pF for CM-RAM
INS4001/2	t_D	I/O Output Lines Delay		600	ns	C_{OUT} = 20 pF
	t_{WC}	CM Write Time	350		ns	
	t_{HC}	CM Hold Time	10		ns	
INS4001	t_{IS}	I/O Input Lines Set Time	50		ns	
	t_{IH}	I/O Input Lines Hold Time	100			
	t_C(3)	I/O Output Lines Delay on Clear		200	ns	C_{OUT} = 20 pF

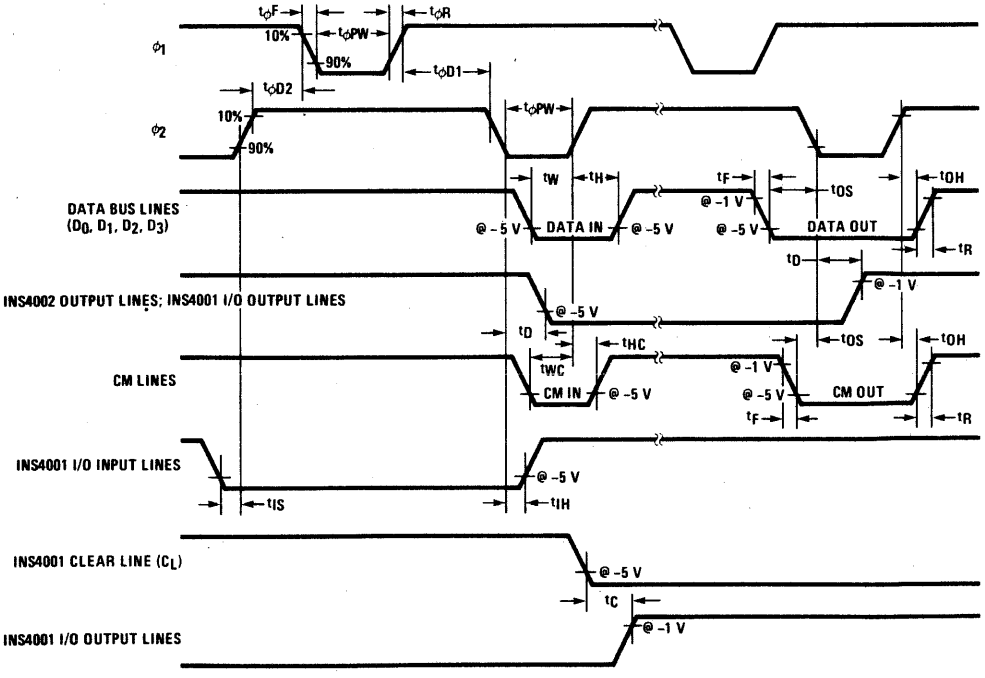
NOTES:

(1)Date out, SYNC, CM-ROM, and CM-RAM lines are clocked out with the trailing edge of the ϕ_2 clock.

(2)The CM-ROM and the selected CM-RAM lines are always activated during A_3 time. They are also activated during M_2 time if an I/O and RAM instruction was fetched by the CPU, and during X_2 time if an SRC instruction was fetched by the CPU;

(3)Pin C_L on INS4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.

INS4001,INS4002,INS4004 timing diagram

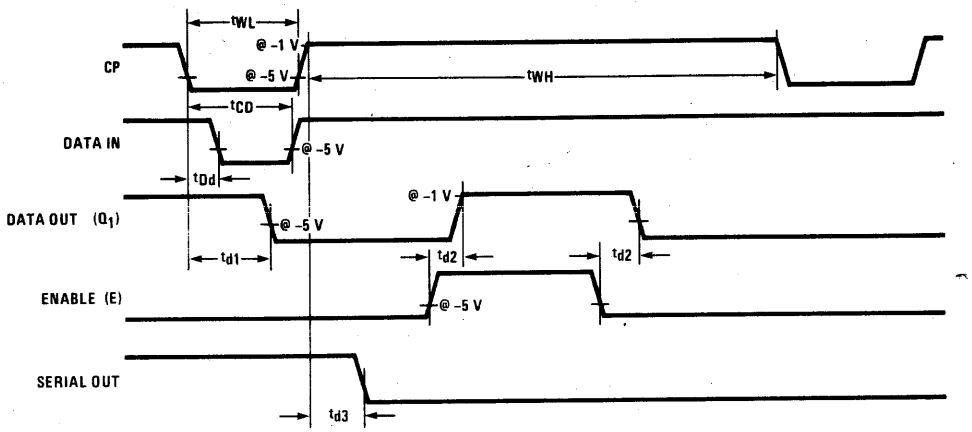


INS4003 a.c. characteristics $T_A = 0°C$ to $+70°C$; $V_{DD} = -15 \pm 5\%$, $V_{SS} = GND$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
t_{WL}	CP Low Width	6	10,000	μs	
t_{WH}	CP High Width	6	Note (1)	μs	
t_{CD}	Clock-On to Data-Off Time	3		μs	
t_{Dd}	CP to Data Set Delay	Note (2)	250	ns	
t_{d1}	CP to Data Out Delay	250	1,750	ns	
t_{d2}	Enable to Data Out Delay		350	ns	C_{OUT} = 20 pF
t_{d3}	CP to Serial Out Delay	200	1,250	ns	C_{OUT} = 20 pF

NOTES: (1) t_{WH} can be any time greater than 6 μsec.
(2) Data can occur prior to CP.

INS4003 timing diagram



capacitance f = 1 MHz; V_{IN} = 0 V; T_A = 25°C; Unmeasured Pins Grounded.

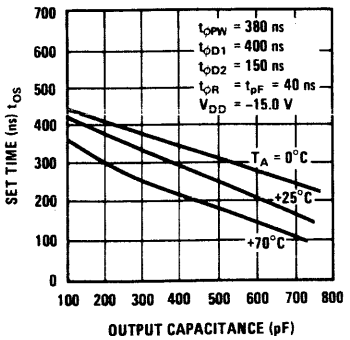
PRODUCT	SYMBOL	TEST	LIMIT (pF) TYP.	LIMIT (pF) MAX.
INS4001/2/3/4	C_{IN}	Input(1) Capacitance	5	10
INS4001/2	$C_{\phi1}$, $C_{\phi2}$	Clock Input Capacitance	8	15
INS4004	$C_{\phi1}$, $C_{\phi2}$	Clock Input Capacitance	14	20

PRODUCT	SYMBOL	TEST	LIMIT (pF) TYP.	LIMIT (pF) MAX.
INS4002/4	C_{D1}	Data Bus I/O Lines Capacitance	6.5	10
INS4001	C_{D2}	Data Bus I/O Lines Capacitance	9.5	15

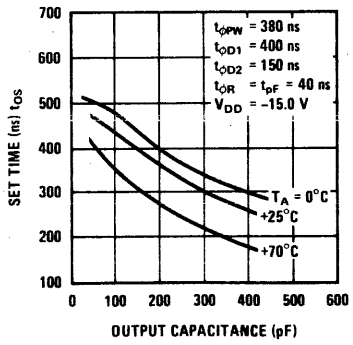
NOTE: (1) Refers to all input pins except data bus I/O and ϕ_1 and ϕ_2.

typical load characteristics

Set Time vs Output Capacitance (Data Lines for INS4001, INS4002, INS4004 & Sync for INS4004)



Set Time vs Output Capacitance (CM-ROM INS4004)



INS4008/INS4009 in a four-bit integrated processing system (FIPS)

The INS4008/4009 standard memory and I/O interface set provides the complete control functions performed by the INS4001. The INS4008/4009 are completely compatible with other members of the FIPS family. All activity is still under control of the INS4004 CPU. One set of INS4008/4009 and several TTL decoders are sufficient to interface to 4k words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

It should be noted that in any FIPS configuration the program memory is distinct from the read/write data storage (INS4002 RAM). Using the INS4008/4009, programs can now be stored and executed from RAM memory, but this RAM memory is distinct from the INS4002 read/write data storage. RAM program memory will be organized in eight bit words and 256 word pages, just like the memory array inside the INS4001. Any combination of PROM, ROM, and RAM will be referred to as program memory.

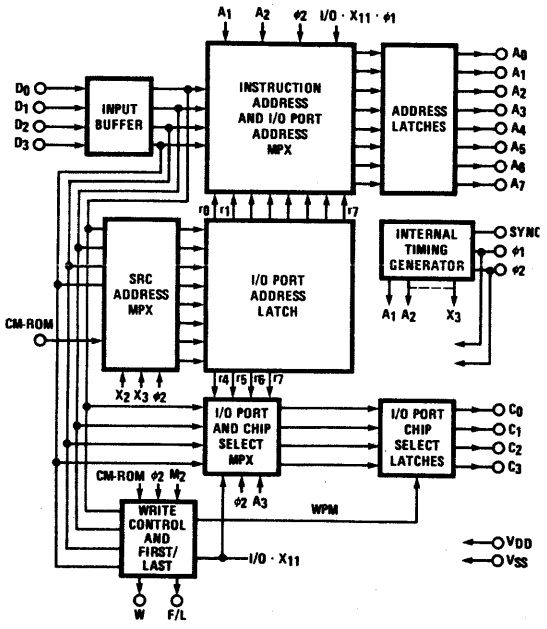
The accompanying diagrams show the internal organization of both the INS4008 and INS4009.

The INS4008 is the address latch chip which interfaces the INS4004 to standard PROMs, ROMs and RAMs used for program memory. The INS4008 latches the eight bit program address sent out by the CPU during A1 and A2 time. During A3 time it latches the ROM chip number from the INS4004. The eight bit program address is then presented at pins A0 through A7 and the four bit chip number (also referred to as page number) is presented at pins C0 through C3. These four bits must be decoded externally and one page of program memory is selected.

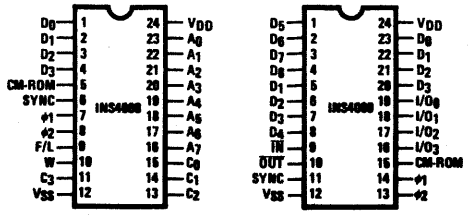
The INS4009 then transfers the eight bit instruction from program memory to the INS4004 four bits at a time at M1 and M2. The command signal sent by the CPU activates the INS4009 and initiates this transfer.

When the CPU executes an SRC (Send Register Control) instruction, the INS4008 responds by storing the I/O address in its eight bit SRC register. The content of this SRC register is always transferred to the address lines (A0 through A7) and the chip select lines (C0 through C3) at X1 time. The appropriate I/O port is then selected by decoding the chip select lines. The IN and OUT lines of the INS4009 indicate whether an input or output operation will occur.

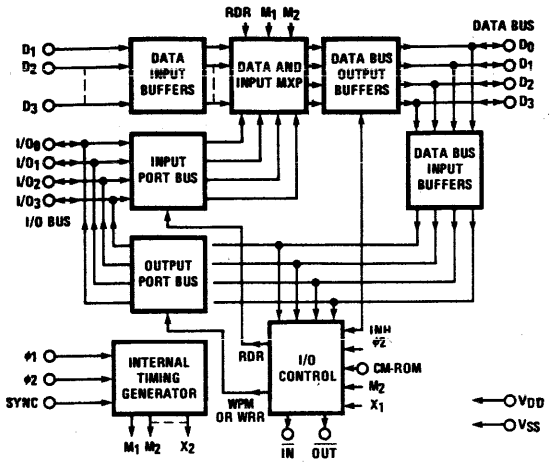
The INS4009 is primarily an instruction and I/O transfer device. When the CPU executes an RDR (Read ROM Port) instruction, the INS4009 will send an input strobe (pin 9) to enable the selected input port. It also enables I/O input buffers to transfer the input data from the I/O bus to the data bus. When the INS4009 interprets a WRR (Write ROM Port) instruction, it transfers output data from the CPU to the I/O bus and sends an output strobe (pin 10) to enable the selected output port. A formerly undefined instruction is now used in conjunction with the INS4008/4009 to write data into the RAM program memory. This new instruction is called WPM (Write Program Memory – 1110 0011). When an instruction is to be stored in RAM program memory, it is written in two four-bit segments. The F/L signal from the INS4008 keeps track of which half is being written. When the CPU executes a WPM instruction, the chip select lines of the INS4008 are jammed with "1111". In the system design this should be designated as the RAM channel. The W line on the INS4008 is also activated by the WPM instruction. The previously selected SRC address on line A0 through A7 of the INS4008 becomes the address of the RAM word being written. By appropriately decoding the chip select lines, the W line, and F/L, the write strobes can be generated for the memory. The F/L line is initially high when power comes on. It then pulses low when every second WPM is executed. A high on the F/L line means that the first four bits are being written, and a low means that the last four bits are being written. The INS4009 transfers the segment of the instruction to the I/O bus at X2 of the WPM instruction. The SRC address sent to RAM is only 8 bits. When more than one page of RAM (256 bytes) is being written, an output port must be used to supply additional address lines for higher order addresses.



INS4008 BLOCK DIAGRAM



PIN CONFIGURATIONS



INS4009 BLOCK DIAGRAM

DEFINITION OF WRITE PROGRAM MEMORY INSTRUCTION

Mnemonic: WPM

OPR OPA: 1111 0011

Symbolic: 1111 → $C_3C_2C_1C_0$ of INS4008
ACC → $I/O_3I/O_2I/O_1I/O_0$ of INS4009
SRC Address → A_0 - A_7 of INS4008

Description: The chip select lines of the INS4008 are forced to "1111" at X1 time and the content of the accumulator is available on the INS4009 I/O bus at X2. RAM program memory can be loaded four bits at a time. The previous SRC address is sent out on lines A0 through A7 of INS4008.

SYSTEM ILLUSTRATIONS USING THE 4008 AND 4009

Example 1: Four MM1702A PROMs and Four I/O Ports. Four MM1702As are used for program storage and four four-bit I/O ports are used. In this case D-type output latches are used and a one of eight decoder 3205 is used to decode both the input and output strobes. Note that the I/O bus is buffered from the outputs. Buffers are needed only when the current sinking requirement on the bus exceeds 1.6 mA. In small systems low power TTL could be used and buffers could be avoided.

Example 2: Read/Write Memory for Program Storage. This example shows only the RAM portion of a system when RAM is used for program memory. Note that the chip selects are tied together in groups of four. The chip selects are gated with the F/L control line for writing only four bits at a time when executing a WPM instruction. They are also gated with the decoding of the chip selects from the INS4008 for normal program execution. The MM1101 (256 words x 1 bit) is shown. A similar system using the MM2102 (1k words x 1 bit) could be developed.

Example 3: Seven MM1702A PROMs, One RAM Block, and Seven I/O Ports. This example uses a single page of RAM program memory shown in Example 2 in a complete system. In this case the input ports are 8:1 multiplexers which are buffered from the I/O bus by a quad tri-state buffer. The input port selection is then the function of the multiplexers. The output ports are latches and the port selection is done using a DM74155 decoder.

Example 4: Eight MM1702A PROMs, Eight RAM Blocks, and Eight I/O Ports. Program memory organized with 2k bytes in ROM and 2k bytes in RAM. Each basic RAM block can be organized as in Example 2. When more than one block of RAM is used, the write chip select (WCS) for each RAM block is generated by properly gating chip select 15 with special decoding for page selection. Output port eight is dedicated to this selection function. This is only necessary when the RAM program memory is being written. In this example standard TTL logic elements are used for I/O port selection rather than decoders as shown in previous examples. In this case all input ports are tri-state buffers.

The following differences exist between a FIPS system using INS4001 program memory and a system using INS4008/4009 program memory:

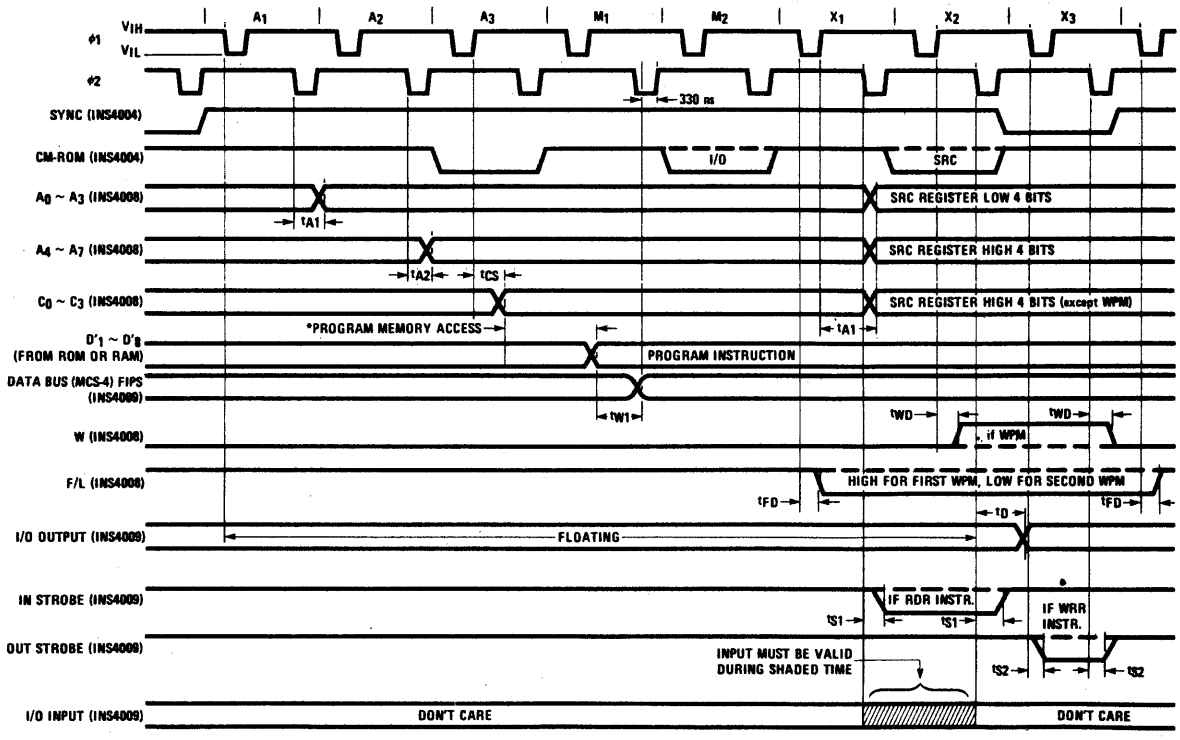
1. For normal operation, INS4001 ROMs cannot be used in the same system with INS4008/4009.
2. Memory address, memory data, I/O bus, and control lines from both INS4008 and INS4009 are defined with respect to positive logic. The FIPS data and control lines from the INS4004 are defined with respect to negative logic. As a result, in program memory used with the INS4009, programs should be coded with logic "1" = high level and logic "0" = low level (i.e., NOP = 0000 0000 = NNNN NNNN). Note that programs are defined for the INS4001 in terms of negative logic such that NOP = 0000 0000 = PPPP PPPP. Carefully check all tapes submitted for metal mask ROMs to be sure that the correct logic definitions are used.
3. Input and output data from the INS4009 I/O bus is defined in terms of positive logic. If these interface devices are used for prototyping an INS4001 program memory, care should be taken to be sure that the I/O ports for the INS4001s are defined consistent with the INS4008/4009 system.
4. An I/O port associated with the INS4009 can have lines with both input and output capability. On the INS4001 each I/O line may have only a single function, either input or output.
5. The RAM program memory cannot be used as a substitute for the INS4002 read/write data storage. They perform distinctly different functions.
6. CM-ROM and CM-RAM_0 cannot be used to control INS4002s when CM-ROM is used for INS4008/4009 and the WPM instruction is being used. The reason is that the WPM instruction is interpreted as a Write Memory (WRM) by INS4002s connected to the same CM line as INS4008/4009. CM-RAM_0 in absence of a DCL behaves exactly like CM-ROM.

a.c. characteristics

T_A = 0°C to +70°C, V_{SS} - V_{DD} = 15 V ± 5%. All clock, sync, CM-ROM, data bus, and I/O timing specifications are identical with the INS4001 and INS4004.

Symbol	Parameter	Product	Limit		Unit	Test Conditions
			Min.	Max.		
t_{CY}	Clock Period	INS4008/4009	1.35	2.0	μs	
$t_{\phi R}$, $t_{\phi F}$	Clock Rise and Fall Time	INS4008/4009		50	ns	
$t_{\phi PW}$	Clock Width	INS4008/4009	380	480	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	INS4008/4009	400	500	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	INS4008/4009	150		ns	
t_{A1}	Address to Output Delay at A_1, X_1	INS4008		1	μs	C_L = 250 pF
t_{A2}	Address to Output Delay at A_2	INS4008		580	μs	C_L = 250 pF
t_{CS}	Chip Select Output Delay at A_3	INS4008		300	ns	C_L = 50 pF
t_{WD}	W Output Delay	INS4008		600	ns	C_L = 100 pF
t_{FD}	F/L Output Delay	INS4008	0.1	1	μs	C_L = 100 pF
t_{WI}	Data In Write Time	INS4009	470		ns	C_L = 200 pF on data bus
t_D	I/O Output Delay	INS4009		1.0	μs	C_L = 300 pF
t_{S1}	IN Strobe Delay	INS4009		450	ns	C_L = 50 pF
t_{S2}	OUT Strobe Delay	INS4009		1.0	μs	C_L = 50 pF

timing diagram

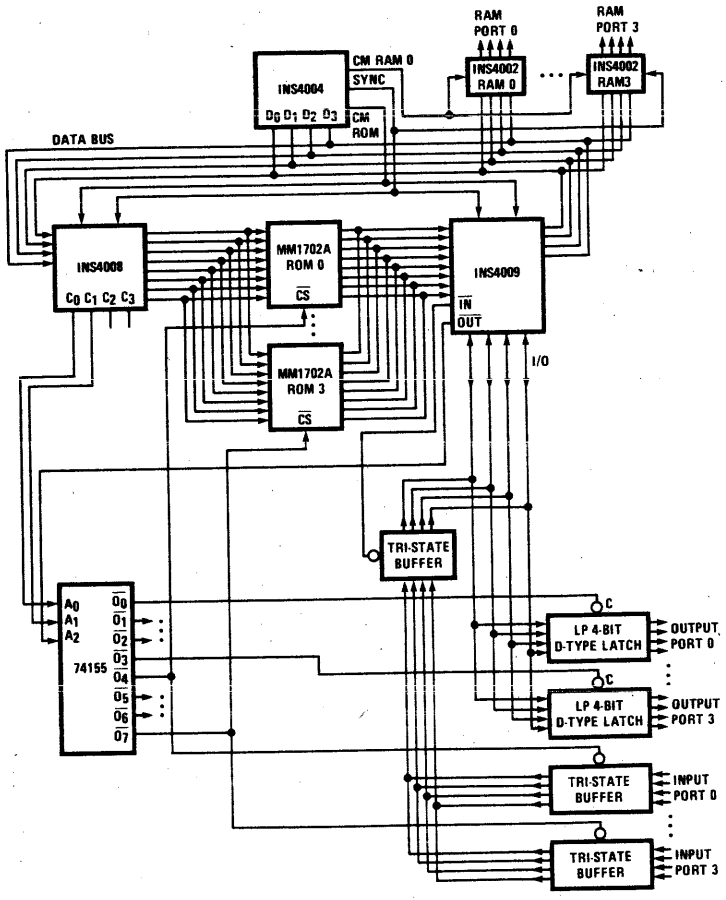


*PROGRAM MEMORY ACCESS TIME (CHIP SELECT TO DATA OUT) MUST BE LESS THAN OR EQUAL TO 900 ns.

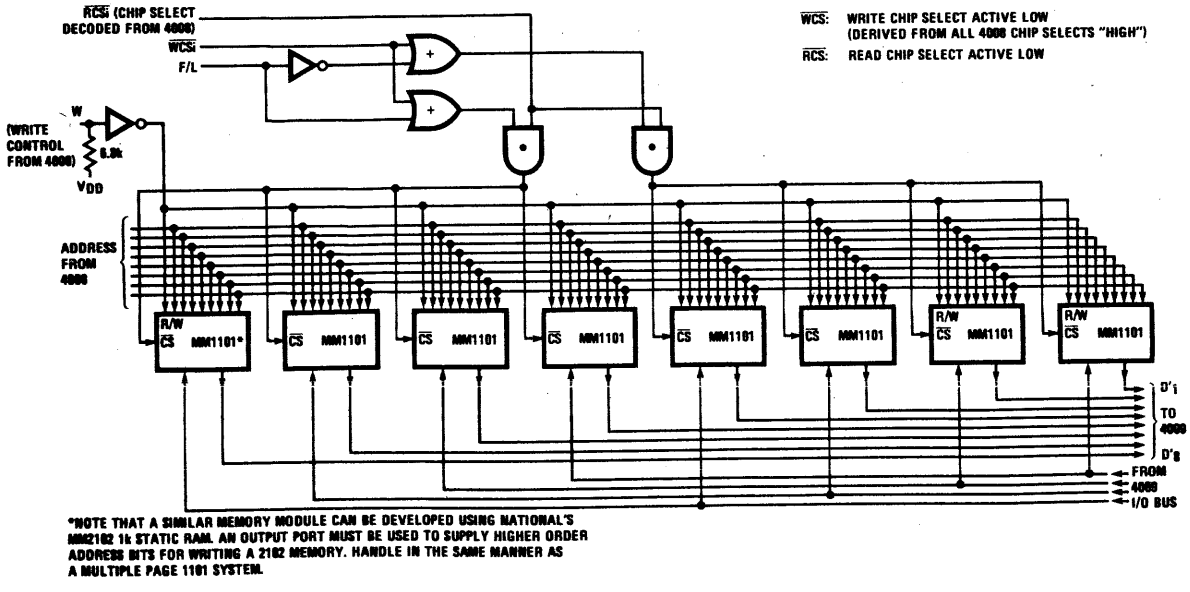
capacitance

f = 1 MHz, V_{IN} = V_{SS}, T_A = +25°C.

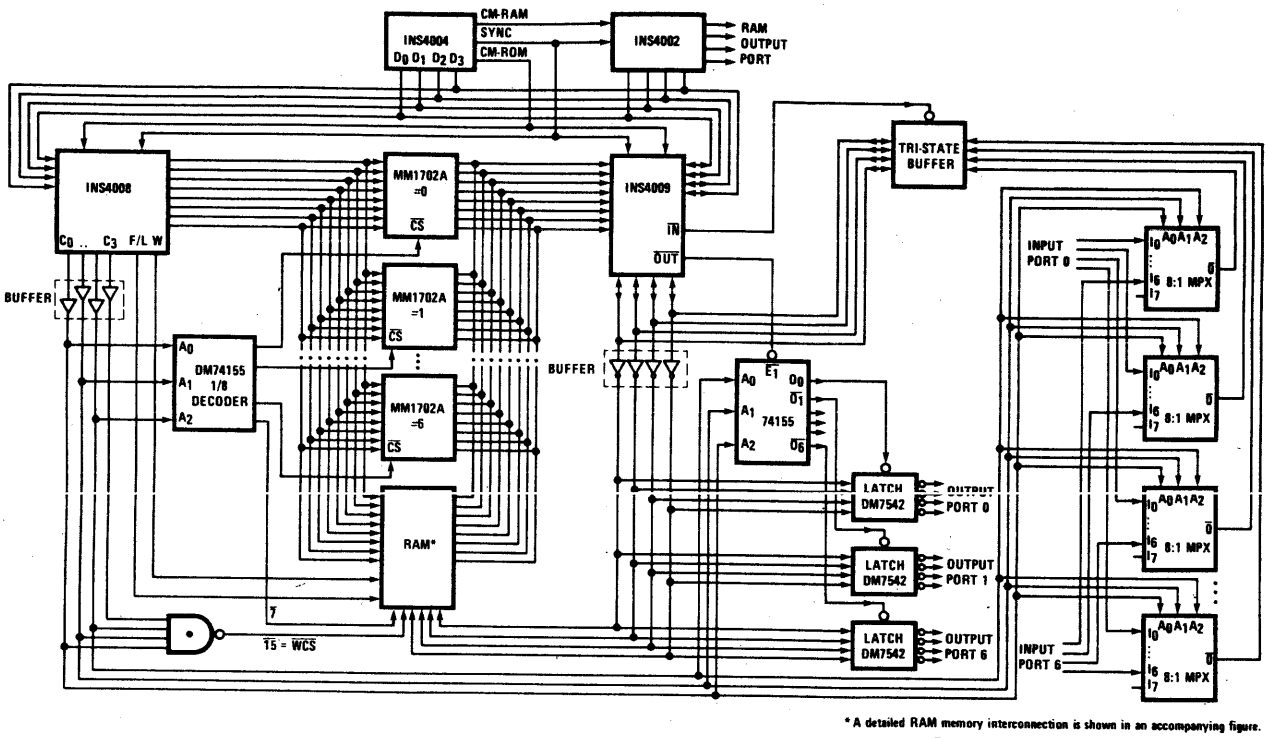
Symbol	Parameter	Product	Limit (pF)		Symbol	Parameter	Product	Limit (pF)	
			Typ.	Max.				Typ.	Max.
C_{IN}	Input Capacitance	INS4008	5	10	$C_{I/O}$	Data Bus and I/O Capacitance	INS4008/9	8	10
		INS4009	8	15					
C_{OUT}	Output Capacitance	INS4008/9	8	10	C_ϕ	Clock Capacitance	INS4008/9	12	20



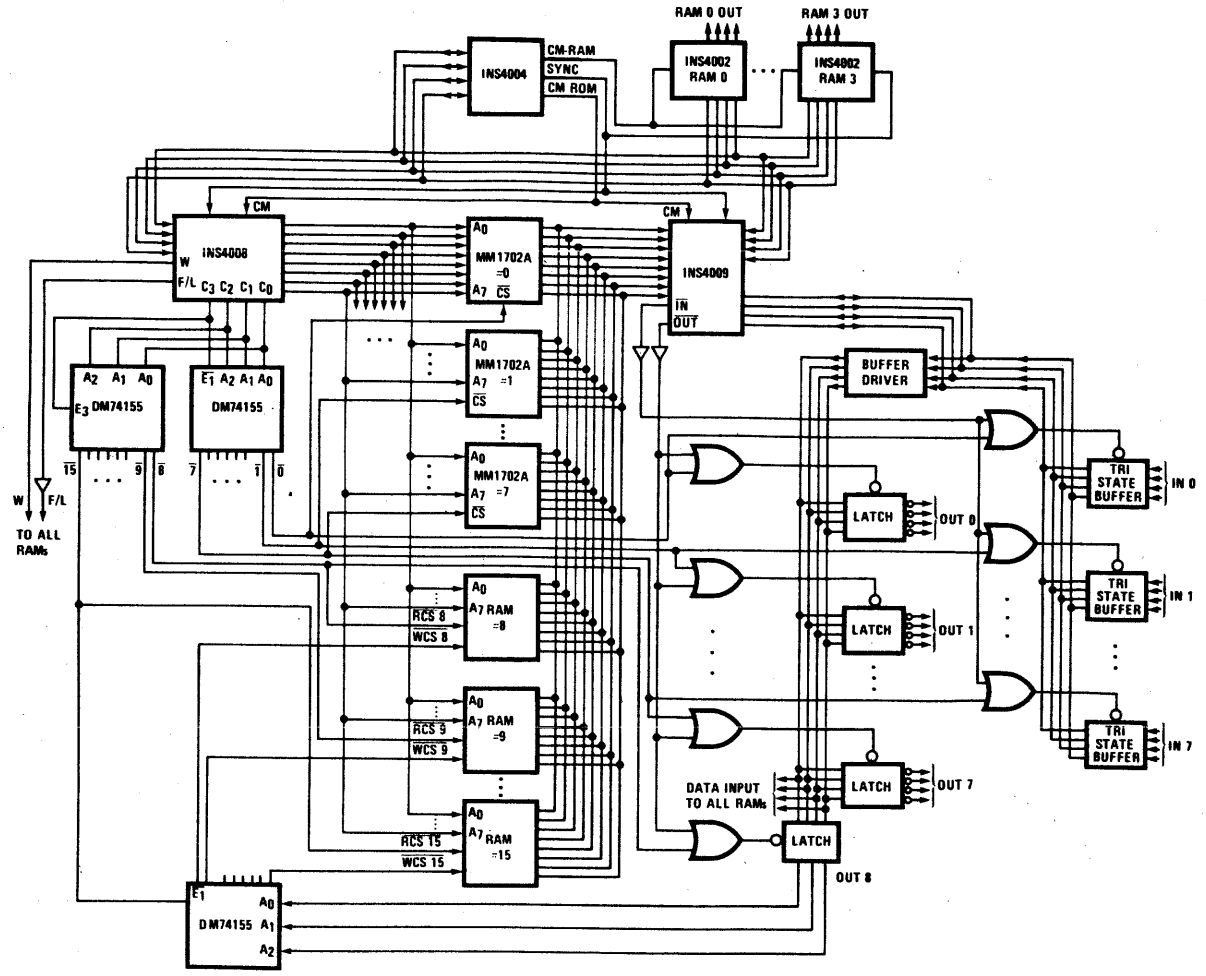
Example 1. Four MM 1702As and Four I/O Ports



Example 2. Read/Write Memory for Program Storage

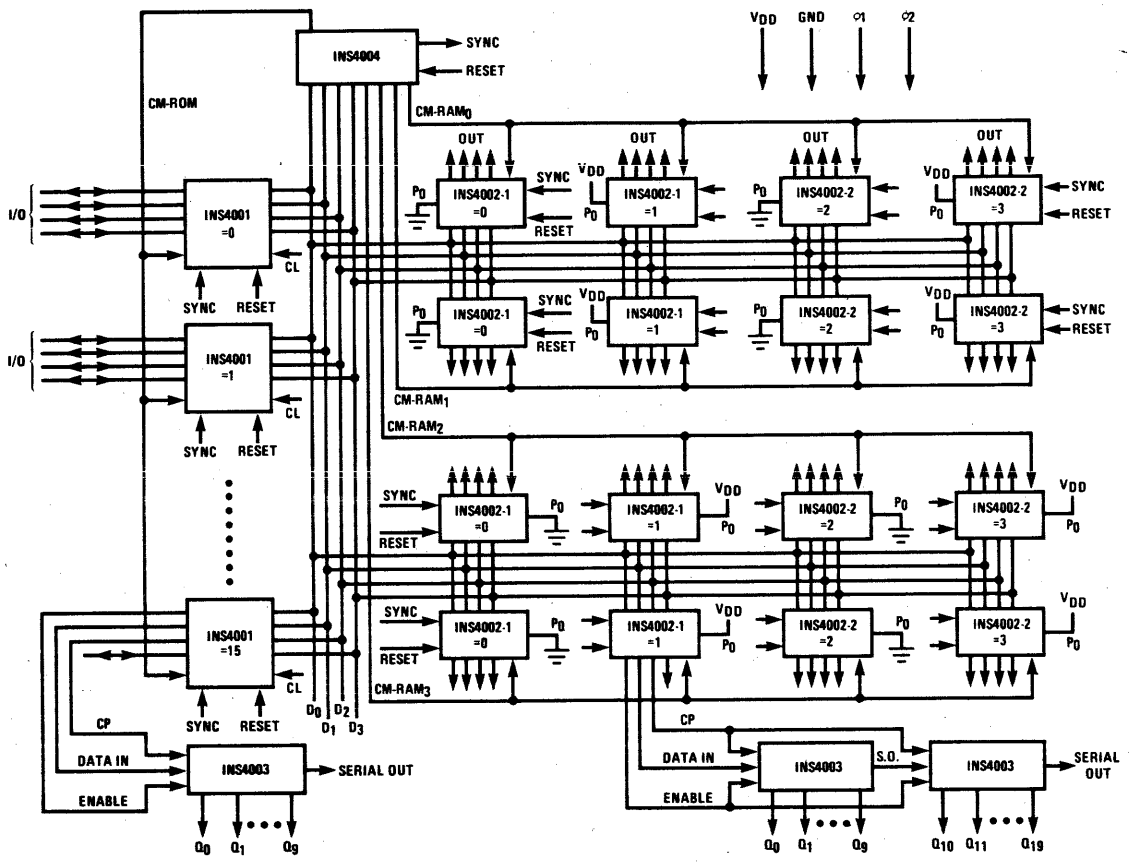


Example 3. Program Memory with Seven Pages of PROM and One Page of RAM



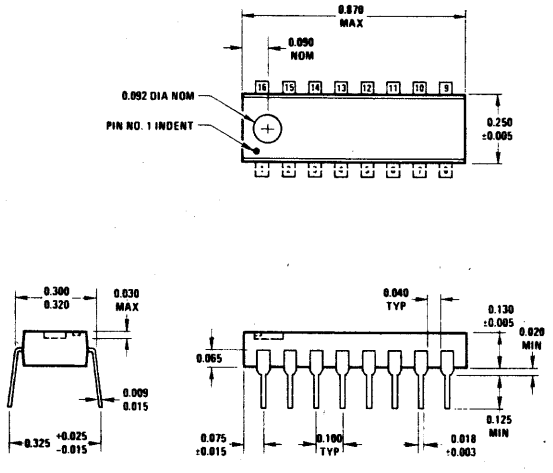
Example 4. Program Memory with Eight Pages of PROM and Eight Pages of RAM

FIPS system interconnection



INS4001 ROM & I/O port, INS4002-1 RAM, INS4003 shift register
INS4004 CPU, four-bit integrated processing system
INS4008/INS4009 in a four-bit integrated processing system (FIPS)

physical dimensions



Molded Dual-In-Line Package (N)

ordering information

NS PART NUMBER	EQUIVALENT INTEL™ PART	FUNCTION
INS4001	4001	256 x 8 ROM & 4-Bit I/O Port
INS4002-1	4002-1	320-Bit RAM & 4-Bit Output Port
INS4002-2	4002-2	
INS4003	4003	Shift Register
INS4004	4004	CPU
INS4008	4008	Standard Memory
INS4009	4009	I/O Interface Set

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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