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National Semiconductor

Linear Application Specific IC's Databook

- Audio Circuits
- Radio Circuits
- Video Circuits
- Display Drivers
- Clock Drivers
- Frequency Synthesis
- Special Automotive
- Special Functions

Linear Application Specific IC's Databook

1993

National Semiconductor

LINEAR APPLICATION SPECIFIC IC's

DATABOOK

1993 Edition

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ISE™
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LMCMOS™
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Macrobus™
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Starlink™
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SuperAT™
Super-Block™
SuperChip™
SuperScript™
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National Semiconductor

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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Additional Available Linear Devices

Additional Available Linear Devices (Continued)

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National Semiconductor

Cross Reference by Part Number

A complete interchangeability list of Linear IC's offered by most Integrated Circuit Manufacturers is listed in this section, and references the nearest National Semiconductor Corporation direct replacement or recommended replacement with either an improved or functional replacement.

The following companies are included in this cross reference:

Analog Devices	Harris (GE/RCA/Intersil)	Philips	Signetics
Burr Brown	Hitachi	Precision Monolithics Inc.	Siliconix
Cherry	Linear Technology Corp.	Raytheon	Texas Instruments
Elantec	Maxim	Samsung	Toshiba
Fairchild (NSC)	Motorola	SGS Thompson	Unitrode

Part Number	NSC Part Number		Part Number	NSC Part Number		Part Number	NSC Part Number	
ANALOG DEVICES								
AD0042	LH0042	I	AD590	LM135	S	AD7542	DAC1210	S
AD101A	LM101A	I	AD590	LM34	S	AD7545	DAC1208	S
AD201A	LM201A	I	AD590	LM35	S	AD7545	DAC1209	S
AD301A	LM301A	I	AD611	LF441	I	AD7545	DAC1210	S
AD5035	LH0042	S	AD624	LM363	S	AD7548	DAC1230	S
AD506	LH0022	S	AD650	LM331	S	AD7548	DAC1231	S
AD509	LH0003	S	AD651	LM331	S	AD7548	DAC1232	S
AD521	LH0036	S	AD654	LM331	S	AD7552	ADC1220	S
AD521	LM363	S	AD673	ADC0841	S	AD7552	ADC1225	S
AD522	LH0038	S	AD707	LM607	I	AD7575	ADC0820	S
AD524	LM363	S	AD711	LF411	S	AD7576	ADC0820	S
AD537	LM331	S	AD712	LF412	S	AD7578	ADC1205	S
AD546	LPC660	I	AD741	LM741	D	AD7578	ADC1225	S
AD546	LPC662	I	AD746	LM6218	I	AD7820	ADC0820	D
AD548	LF441	D	AD7502	LF13509	S	AD7821	ADC08061	I
AD549	LPC660	I	AD7523	DAC0830	S	AD7824	ADC08064	I
AD549	LPC662	I	AD7523	DAC0831	S	AD7828	ADC08068	I
AD562	DAC1266	S	AD7523	DAC0832	S	AD844	LM6181	I
AD563	DAC1265	S	AD7524	DAC0830	S	AD846	LM6181	I
AD565A	DAC1265	S	AD7524	DAC0831	S	AD847	LM6161	D
AD566A	DAC1266	S	AD7524	DAC0832	S	AD848	LM6164	D
AD567	DAC1230	S	AD7533	DAC1020	D	AD849	LM6165	D
AD573	ADC1005	S	AD7533	DAC1021	D	AD96685	LM6685	I
AD581	LH0070	I	AD7533	DAC1022	D	AD96687	LM6687	I
AD582	LF398	S	AD7541	DAC1218	S	ADDAC-08	DAC0800	D
AD583	LF398	S	AD7541	DAC1219	S	ADDAC-08	DAC0801	D
AD588	LM369	S	AD7541A	DAC1218	S	ADDAC-08	DAC0802	D
AD589M	LM385	I	AD7541A	DAC1219	S	ADOP07	LM607	I
AD589U	LM185	I	AD7542	DAC1208	S	HTC-0300	LH4860	S
AD590	LM134	S	AD7542	DAC1209	S			

The following notations are appended to assist you in finding the best option.
S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

Part Number	NSC Part Number	
BURR-BROWN		
3507	LH0003	S
3507	LM118	S
3507	LM6361	S
3507	LM709	S
3510	LM101	S
3510	LM107	S
3510	LM112	S
3510	LM725	S
3510	LM748	S
3533	LH0033	S
3542	LH0042	S
3550	LM6361	S
3551	LH0024	S
3551	LM6361	S
3553	LH0002	S
3553	LH0063	S
3554	LH0032	S
3571	LM675	S
3572	LH0021	S
3573	LM675	S
3580	LH0004	S
3580	LM143	S
3580	LM144	S
3606A6	LH0084	S
3606A6	LH0086	S
3626	LH0036	S
3629	LH0038	S
ADC80	ADC1280	S
DAC7541A	AD7521	S
DAC7541A	AD7531	S
DAC7541A	DAC1218	S
DAC7541A	DAC1219	S
DAC811	ADC1230	S
H0S-100	LH0033	S
HI-508	LF13508	S
HI-509	LF13509	S
INA101	LM163	S
INA101HP	LM363	S
INA102	LH0038	S
INA102	LM363	S

Part Number	NSC Part Number	
OPA111	LH0052	S
OPA121	LF441A	S
OPA121	LH0022	S
OPA121	LH0042	S
OPA156	LF156	S
OPA21	LM108A	S
OPA21	LM11	S
OPA2111	LF353	S
OPA2111	LF412A	S
OPA2111	LF442A	S
OPA2111	LH2011	S
OPA2111	LH2101A	S
OPA2111	LH2108A	S
OPA2111	LM1558	S
OPA2111	LM358	S
OPA2111	LM2904	S
OPA2111	LM747A	S
OPA27	LH0044	S
OPA27	LM627	S
OPA37	LM637	S
OPA404	LF444A	S
OPA404	LM837	S
OPA404	LMC660	S
OPA511	LM675	S
OPA541	LH0101	S
OPA541	LM12	S
OPA602	LF411	S
OPA605	LH0005	S
OPA605	LH0032	S
OPA633	LH0033	S
OPA633	LH4001	S
PGA100/102	LH0086	S
PGA200/201	LH0084	S
SHC298	LF298	D
SHC298	LH0043	S
SHC5320	LH0053	D
SHC80	LF398	S
SHC85	LF398	S
SHC85	LH0053	S
VFC32	LM131/331	S

Part Number	NSC Part Number	
CHERRY		
CS-189	LM1819	S
CS-2907	LM2907	D
CS-2917	LM2917	D
CS-925	LM2925	S
CS-935	LM2935	S
ELANTEC		
EHA2500	LM6161	S
EHA2502	LM6161	S
EHA2505	LM6361	S
EHA2510	LM6161	S
EHA2512	LM6161	S
EHA2515	LM6361	S
EHA2520	LM6164	S
EHA2522	LM6164	S
EHA2525	LM6364	S
EHA2600	LM6161	S
EHA2602	LM6161	S
EHA2605	LM6361	S
EHA2620	LM6164	S
EHA2622	LM6164	S
EHA2625	LM6364	S
EL2006	LM6161	S
EL2006C	LM6261	S
EL2020	LM6181	I
ELH0002	LH0002	D
ELH0021	LH0021	D
ELH0032	LH0032	D
ELH0033	LH0033	D
ELH0041	LH0041	D
ELH0101	LH0101	D

The following notations are appended to assist you in finding the best option.

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Part Number	NSC Part Number	
FAIRCHILD (NSC)		
μA101	LM101	D
μA105	LM105	D
μA108	LM108	D
μA108A	LM108A	D
μA110	LM110	D
μA111	LM111	D
μA117	LM117	D
μA124	LM124	D
μA139	LM139	D
μA1458	LM1458	D
μA1489	DS1489	D
μA1558	LM1558	D
μA201	LM201	D
μA208	LM208	D
μA208A	LM208A	D
μA2111	LH2111	D
μA224	LM224	D
μA239	LM239	D
μA26LS31	DS26LS31	D
μA26LS32	DS26LS32	D
μA2901	LM2901	D
μA301	LM301	D
μA301A	LM301A	D
μA305	LM305	D
μA3052	TP3052	D
μA305A	LM305A	D
μA308	LM308	D
μA3086	LM3086	D
μA30S54	TP3054	D
μA30S57	TP3057	D
μA30S64	TP3064	D
μA30S67	TP3067	D
μA311	LM311	D
μA317	LM317	D
μA324	LM324	D
μA3302	LM3302	D
μA348	LM348	D
μA3486	DS3486	D
μA350	LM350	D
μA5116	TP5116	D
μA5156	TP5156	D
μA555	LM555	D
μA556	LM556	D
μA5800	TP3204	D
μA709	LM709	D
μA710	LM710	D
μA711	LM711	D
μA723	LM723	D
μA725	LM725	D
μA741	LM741	D
μA747	LM747	D
μA748	LM748	D
μA75107	DS75107	D
μA75108	DS75108	D
μA75150	DS75150	D
μA75154	DS75154	D
μA75450	DS75450	D
μA75491	DS75491	D
μA760	LM760	D
μA771	LF351	D
μA772	LF353	D
μA774	LF347	D
μA7805	LM140	D
μA7805	LM340-5	D
μA7805	LM7805	D
μA7806	LM7806	D
μA7808	LM7808	D
μA7812	LM140	D
μA7812	LM340-12	D
μA7812	LM7812	D
μA7815	LM140	D
μA7815	LM340-15	D
μA7815	LM7815	D
μA7818	LM7818	D
μA7824	LM7824	D
μA78L05	LM78L05	D
μA78L12	LM78L12	D
μA78L15	LM78L15	D
μA78LXXA	LM78LXXA	D
μA78M05	LM78M05	D
μA78M12	LM78M12	D
μA78MXX	LM341-XX	D
μA78MXX	LM78MXX	D
μA78XX	LM140-XX	D
μA78XX	LM340-XX	D
μA78XX	LM78XX	D
μA7905	LM7905	D
μA7912	LM7912	D
μA7915	LM7915	D
μA79M05	LM79M05	D
μA79M12	LM79M12	D
μA79M15	LM79M15	D
μA79MXX	LM320-XX	D
μA79XX	LM320-XX	D
μA79XX	LM79LXX	D
μA79XX	LM79MXX	D
μA79XX	LM79XX	D
DAC1508	MC1508	D
SH0002	LH0002	D
SH1605	LH1605	D
HARRIS (GE/RCA/Intersil)		
μA748	LM748	D
AD7520	DAC1021	D
AD7520	DAC1022	D
AD7521	DAC1220	D
AD7521	DAC1221	D
AD7521	DAC1222	D
AD7530	DAC1020	S
AD7530	DAC1021	S
AD7530	DAC1022	S
AD7531	DAC1220	D
AD7531	DAC1221	D
AD7531	DAC1222	D
AD7533	DAC1020	D
AD7533	DAC1021	D
AD7533	DAC1022	D
AD7541	DAC1218	S
AD7541	DAC1219	S
ADC0801	ADC0801	D
ADC0802	ADC0802	D
ADC0803	ADC0803	D

The following notations are appended to assist you in finding the best option.

S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

HARRIS (GE/RCA/Intersil) (Continued)

Part Number	NSC Part Number	
ADC0804	ADC0804	D
CA081	LF411	S
CA081	TL081	D
CA082	LF412	S
CA082	TL082	D
CA084	LF147	S
CA084	LF347	S
CA124	LM124	D
CA139	LM139	D
CA139A	LM139A	D
CA1458	LM1458	D
CA1558	LM1558	D
CA158	LM158	D
CA158A	LM158A	D
CA224	LM224	D
CA239	LM239	D
CA239A	LM239A	D
CA258	LM258	D
CA258A	LM258A	D
CA301A	LM301A	D
CA307	LM307	D
CA3105	LM675	S
CA311	LM311	D
CA324	LM324	D
CA3290	LM393	S
CA339	LM339	D
CA339A	LM339A	D
CA3401	LM3401	D
CA358	LM358	D
CA358A	LM358A	D
CA741	LM741	D
CA747	LM747	D
CA748	LM748	D
DG201	LF13201	D
DG211	LF13201	D
DG212	LF13202	D
HA-OP07	LM607	I
HA2400	LM604	S
HA2404	LM604	S
HA2405	LM604	S
HA2406	LM604	S
HA2420	LH0023	S
HA2420	LH0043	S
HA2500	LM6161	S
HA2502	LM6161	S
HA2505	LM6361	S
HA2510	LM118	S
HA2510	LM318	S
HA2510	LM6161	S
HA2512	LM6161	S
HA2515	LM6361	S
HA2520	LM6164	S
HA2520	LM6113	S
HA2522	LM6164	S
HA2522	LM6113	S
HA2525	LM6364	S
HA2525	LM6313	S
HA2529	LM6313	S
HA2530	LH0024	S
HA2535	LH0024	S
HA2540	LH0032	S
HA2541-2	LM6161	S
HA2541-5	LM6361	S
HA2542	LH0032	S
HA2620	LH4104	S
HA2620	LM6164	S
HA2622	LM118	S
HA2625	LM318	S
HA2640	LH0004	S
HA2640	LM143	S
HA2640	LM144	S
HA2645	LM343	S
HA2645	LM344	S
HA4741	LM348	S
HA5002	LH0002	S
HA5033	LH0033	S
HA5020	LM6181	I
HA5102	LM833	S
HA5104	LM837	S
HA5135	LM637	S
HA5141	LM4250	S
HA5142	LF442	D
HA5144	LF444	D
HA5160	LF357	S
HA5160	LH0062	S
HA5162	LH0062	S
HA5170	LF151	S
HA5170	LF155	S
HA5170	LF156	S
HA5170	LF157	S
HA5170	LF355	S
HA5170	LF356	S
HA5180	LH0022	S
HA5180	LH0042	S
HA5180	LH0052	S
HF-10	MF10	D
HF-201	LF13201	D
HF-300	AH5020	S
HI-201	LF13201	D
HI-508	LF13508	S
HI-509	LF13509	S
HI-5618	DAC0800	S
HI-5618	DAC0806	S
HI-5618	DAC0807	S
HI-5618	DAC0808	S
HI-565A	DAC1265	D
HI-5660	DAC1266	D
HI-5680	DAC1280	S
HI-5685	DAC1200	S
HI-5685	DAC1285	S
HI-5687	DAC1201	S
HI-5687	DAC1285	S
HI-5690	DAC1280	S
HI-5695	DAC1285	S
HI-5697	DAC1285	S
HI-574	ADC1080	S
HI-574	ADC1210	S
HI-574	ADC1211	S
HI-574	ADC1280	S
HI-674	ADC1080	S

The following notations are appended to assist you in finding the best option.

S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

Part Number	NSC Part Number	
HARRIS (GE/RCA/Intersil) (Continued)		
HI-674	ADC1280	S
ICH8530	LH0101	S
ICL7114	ADC1205	S
ICL7114	ADC1225	S
ICL7660	LMC7660	D
ICL8069	LM313	D
ICL8069	LM385-1.2	D
IH5009	AH5009	D
IH5010	AH5010	D
IH5011	AH5011	D
IH5012	AH5012	D
IH6106	LF13508	D
IH6206	LF13509	D
LM741	LM741	D
HITACHI		
HA12012	LM833	S
HA12411	LM3089	D
HA12412	LM3189	S
HA12413	LM1868	S
HA12417	LM1863	S
HA13421A	LM18293	S
HA1374	LM2877	S
HA1389	LM384	S
HA1394	LM2879	S
HA1397	LM1875	S
HA17082	LF353	I
HA17082A	LF412	I
HA17084	LF347	I
HA17084A	LF347B	I
HA17094	LM2904	I
HA17301	LM3301	I
HA17324	LM324	I
HA17339	LM339	I
HA17358	LM358	I
HA17393	LM393	I
HA17458	LM458	I
HA17741	LM741	I
HA17747	LM747	I
HA17901	LM2901	I
HA17902	LM2902	I
HA17903	LM2903	I

Part Number	NSC Part Number	
LINEAR TECHNOLOGY CORP.		
LF155	LF155	D
LF155A	LF155A	D
LF156	LF156	D
LF156A	LF156A	D
LF198	LF198	D
LF198A	LF198A	D
LF355A	LF355A	D
LF356A	LF356A	D
LF398	LF398	D
LF398A	LF398A	D
LF412A	LF412A	D
LH0070	LH0070	D
LH2108	LH2108	D
LH2108A	LH2108A	D
LM10	LM10	D
LM101A	LM101A	D
LM107	LM107	D
LM108	LM108	D
LM108A	LM108A	D
LM111	LM111	D
LM117	LM117	D
LM117HV	LM117HV	D
LM118	LM118	D
LM119	LM119	D
LM123	LM123	D
LM129	LM129	D
LM129A	LM129A	D
LM134	LM134	D
LM136	LM136	D
LM137	LM137	D
LM137HV	LM137HV	D
LM138	LM138	D
LM150	LM150	D
LM185	LM185	D
LM199	LM199	D
LM234	LM234	D
LM308A	LM308A	D
LM311	LM311	D
LM317	LM317	D
LM317HV	LM317HV	D

Part Number	NSC Part Number	
LM318	LM318	D
LM319	LM319	D
LM323	LM323	D
LM329	LM329	D
LM329A	LM329A	D
LM334	LM334	D
LM336	LM336	D
LM337	LM337	D
LM337HV	LM337HV	D
LM338	LM338	D
LM350	LM350	D
LM385	LM385	D
LM399	LM399	D
LM399A	LM399A	D
LT1001	LH0044	D
LT1001	LM607	I
LT1003	LM123	S
LT1003	LM323	S
LT1003	LM337	D
LT1004	LM113	D
LT1004	LM185	D
LT1004	LM385	D
LT1005	LM2935	S
LT1008	LM108	D
LT1008	LM308	D
LT1009	LM136	D
LT1009	LM336	D
LT1010	LH0002	S
LT1011	LM311	D
LT1012	LM312	D
LT1013	LM358	D
LT1014	LM324	D
LT1014	LM348	D
LT1019	LM368	D
LT1020	LP2951	S
LT1021	LM369	I
LT1022	LF356	D
LT1029	LM336	D
LT1031	LH0070	D
LT1033	LM133	D

The following notations are appended to assist you in finding the best option.

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Part Number	NSC Part Number	
LINEAR TECHNOLOGY CORP. (Continued)		
LT1033	LM137	S
LT1033	LM333	D
LT1034	LM385	D
LT1038C	LM396	S
LT1038M	LM196	S
LT1055	LF355	D
LT1056	LF356	D
LT111	LM111	D
LM317HV	LM317HV	D
LT117	LM117	D
LT118	LM118	D
LT119	LM119	D
LT123	LM123	D
LT123A	LM123A	D
LT1223	LM6181	I
LT137	LM137	D
LT150	LM150	D
LT1524	LM1524D	D
LT311	LM311	D
LT317	LM317	D
LT317A	LM317A	D
LT318	LM318	D
LT319	LM319	D
LT323	LM323	D
LT323A	LM323A	D
LT337	LM337	D
LT338	LM338	D
LT338A	LM338A	D
LT350A	LM350A	D
LT3524	LM3524D	D
LTC1059	MF5	D
LTC1060	MF10	D
LTC1099	ADC0820	D
REF-01	LM368	S
SG1524	LM1524D	I
SG3524	LM3524D	I

Part Number	NSC Part Number	
MAXIM		
AD565	DAC1265	D
AD566	DAC1266	D
AD7523	DAC0830	S
AD7523	DAC0831	S
AD7523	DAC0832	S
AD7524	DAC0830	S
AD7524	DAC0831	S
AD7524	DAC0832	S
AD7533	DAC1020	D
AD7533	DAC1021	D
AD7533	DAC1022	D
AD7541	DAC1218	S
AD7541	DAC1219	S
AD7542	DAC1208	S
AD7542	DAC1209	S
AD7542	DAC1210	S
AD7545	DAC1208	S
AD7545	DAC1209	S
AD7545	DAC1210	S
AD7548	DAC1230	S
AD7548	DAC1231	S
AD7548	DAC1232	S
AD7820	ADC0820	D
ICL7642	LMC6044	S
MAX480	LMC6041	S
MOTOROLA		
AD562	DAC1266	S
AD563	DAC1265	S
DAC-08	DAC0800	D
DAC-08	DAC0801	D
DAC-08	DAC0802	D
LF347	LF347	D
LF351	LF351	D
LF353	LF353	D
LF355	LF355	D
LF356	LF356	D
LF357	LF357	D
LF411	LF411	D
LF412	LF412	D
LF441	LF441	D
LF442	LF442	D

Part Number	NSC Part Number	
LF444	LF444	D
LM101	LM101	D
LM108	LM108	D
LM109	LM109	D
LM11	LM11	D
LM111	LM111	D
LM117	LM117	D
LM123	LM123	D
LM124	LM124	D
LM137	LM137	D
LM139	LM139	D
LM140	LM140	D
LM148	LM148	D
LM150	LM150	D
LM158	LM158	D
LM193	LM193	D
LM201	LM201	D
LM208	LM208	D
LM209	LM109	D
LM211	LM211	D
LM217	LM117	D
LM223	LM123	D
LM224	LM224	D
LM237	LM137	D
LM239	LM239	D
LM248	LM248	D
LM250	LM150	D
LM258	LM258	D
LM285	LM285	D
LM2900	LM2900	D
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM2903	D
LM2904	LM2904	D
LM293	LM293	D
LM2931	LM2931	D
LM301	LM301	D
LM307	LM307	D
LM308	LM308	D
LM309	LM309	D

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Part Number	NSC Part Number	
MOTOROLA (Continued)		
LM311	LM311	D
LM317	LM317	D
LM323	LM323	D
LM324	LM324	D
LM337	LM337	D
LM339	LM339	D
LM340-XX	LM340-XX	D
LM348	LM348	D
LM350	LM350	D
LM358	LM358	D
LM385	LM385	D
LM3900	LM3900	D
LM393	LM393	D
LM833	LM833	D
MC1391	LM1391	D
MC1408	DAC0806	D
MC1408	DAC0807	D
MC1408	DAC0808	D
MC1414	LM1414	D
MC1436	LM343	I
MC1437	LH2301	S
MC14442	ADC0829	S
MC14444	ADC0830	S
MC145040	ADC0811	S
MC145041	ADC0811	D
MC1455	LM555	D
MC1456	LM212	S
MC1458	LM1458	D
MC1468	LM325	S
MC1488	DS1488	D
MC1489	DS1489	D
MC1496	LM1496	D
MC1508	DAC0808	D
MC1514	LM1514	D
MC1536	LM143	I
MC1537	LH2101	S
MC1537	LH2201	S
MC1556	LM112	S
MC1558	LM1558	D
MC1568	LM125	S
MC1596	LM1596	D
MC1709	LM709	D
MC1710	LM710	D
MC1723	LM723	D
MC1741	LM741	D
MC1747	LM747	D
MC1748	LM748	D
MC3301	LM3301	D
MC3302	LM3302	D
MC33078	LM833	S
MC33079	LM837	S
MC3346	LM3046	D
MC3346	LM3146	I
MC3356	LM3089	S
MC3356	LM3189	S
MC3361	LM3361A	I
MC34001	LF351	I
MC34001	LF353	I
MC34001	LF411	I
MC34002	LF412	I
MC34004	LF347	I
MC3401	LM3401	D
MC3410	DAC1020	D
MC3412	DAC1265	S
MC3456	LM556	D
MC35001	LF411	I
MC35002	LF412	I
MC3510	DAC1020	D
MC4741	LM348	D
MC7812	LM7812	D
MC7815	LM7815	D
MC7824	LM7824	D
MC78LXX	LM78LXX	D
MC78LXXA	LM78LXXA	D
MC78MXX	LM341-XX	D
MC78MXX	LM78MXX	D
MC78XX	LM78XX	D
MC78XXA	LM340A-XX	D
MC79LXX	LM320L-XX	D
MC79LXX	LM79LXXA	D
MC79MXXA	LM79MXX	I
MC79XX	LM320-XX	I
MC79XX	LM79XX	D
MC79XXA	LM320-XX	I
PHILIPS		
μA723	LM723	D
μA741	LM741	D
μA747	LM747	D
ADC0803	ADC0803	D
ADC0804	ADC0804	D
ADC0805	ADC0805	D
ADC0820	ADC0820	D
AM26LS30	DS3691	D
CA3089	LM3089	D
DAC-08	DAC0801	D
DAC-08	DAC0800	D
DAC-08	DAC0802	D
ICM7555	LMC555	D
LF198	LF198	D
LF224	LM224	D
LF298	LF298	D
LF398	LF398	D
LM111	LM111	D
LM119	LM119	D
LM124	LM124	D
LM139	LM139	D
LM139A	LM139A	D
LM158	LM158	D
LM193	LM193	D
LM193A	LM193A	D
LM211	LM211	D
LM219	LM219	D
LM224	LM224	D
LM239	LM239	D
LM239A	LM239A	D
LM258	LM258	D
LM2901	LM2901	D
LM2903	LM2903	D
LM293	LM293	D
LM293A	LM293A	D

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Part Number	NSC Part Number	
PHILIPS (Continued)		
LM311	LM311	D
LM319	LM319	D
LM324	LM324	D
LM324A	LM324A	D
LM339	LM339	D
LM339A	LM339A	D
LM358	LM358	D
LM393	LM393	D
LM393A	LM393A	D
MC1408	DAC0807	D
MC1408	DAC0808	D
MC1458	LM1458	D
MC1488	DS1488	D
MC1488	DS14C88	I
MC1489	DS1489	D
MC1489A	DS1489A	D
MC1489A	DS14C89A	I
MC1496	LM1496	D
MC1508	DAC0808	D
MC1596	LM1596	D
MC3302	LM3302	D
MC3403	LM3403	D
NE4558	LM833	S
NE5034	ADC0841	S
NE5118	DAC0830	S
NE5119	DAC0830	S
NE5410	DAC1020	S
NE5532	LM833	D
NE5532	LM833	D
NE555	LM555	D
NE556	LM556	D
NE565	LM565	D
NE566	LM566	D
NE567	LM567	D
SA532	LM2904	I
SA534	LM2902	I
SE529	LM161	S
SE5537	LF398	D
SE555	LM555	D
SE556	LM556	D
SE567	LM567	D
SG1532	LM1524	I
SG2524	LM2524	D
SG3524	LM3524	D
PRECISION MONOLITHICS INC.		
ADC-910	ADC1025	S
ADC-910	ADC1061	S
AMP-01	LH0038	S
AMP01	LM363	S
BUF-03	LH0033	I
BUF-03	LH0002	S
CMP-08	LM260	S
CMP-08	LM360	S
DAC-02	DAC1020	S
DAC-02	DAC1021	S
DAC-02	DAC1022	S
DAC-03	DAC1020	S
DAC-03	DAC1021	S
DAC-03	DAC1022	S
DAC-05	DAC1020	S
DAC-05	DAC1021	S
DAC-05	DAC1022	S
DAC-08	DAC0800	D
DAC-08	DAC0801	D
DAC-08	DAC0802	D
DAC-100	DAC1020	S
DAC-100	DAC1021	S
DAC-100	DAC1022	S
DAC-1408	DAC0806	S
DAC-1408	DAC0807	S
DAC-1408	DAC0808	S
DAC-312	DAC1266	D
DAC-888	DAC0830	S
DAC-888	DAC0831	S
DAC-888	DAC0832	S
MAT02	LM394	S
MAT02AH	LM194H	S
MUX-08E	LF13508	D
MUX-24E	LF13509	D
OP-05	LM607	S
OP-07	LM607	I
OP-07	OP07	D
OP-15	LF411	I
OP-215	LF412	I
OP-77	LM607	I
OP02	LM741	S
OP04	LM747	S
OP06	LM725	S
OP08	LM101	S
OP09	LM4136	S
OP11	LM324	S
OP11	LM348	S
OP14	LM1458	S
OP14	LM1558	S
OP14	LM358	S
OP15	LF351	S
OP15	LM301	S
OP15	LM310	S
OP160	LM6181	I
OP177	LM607	S
OP215	LF353	S
OP22	LM4250	S
OP221	LM2904	S
OP221	LM358	S
OP42	LH0062	S
OP42	LM318	S
OP421	LM2902	S
OP421	LM324	S
OP421	LM3303	S
OP421	L2902	S
OP421	LP324	S
OP43	LM348	S
OP43GP	LF441ACN	S
OP471	LM149	S
OP471	LM837	S
OP490	LMC6044	S
OP77	LM607	S
OP97	LM311	S
PM0820	ADC0820	D
PM1008	LM308	D

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Part Number	NSC Part Number	
PRECISION MONOLITHICS INC. (Continued)		
PM1012	LM312	S
PM111	LM111	D
PM119	LM119	D
PM139	LM139	D
PM139A	LM139A	D
PM148	LM148	D
PM155	LF155	D
PM155A	LF155A	D
PM156	LF156	D
PM156A	LF156A	D
PM157	LF157	D
PM157A	LF157A	D
PM208	LM208	D
PM208A	LM208A	D
PM211	LM211	D
PM219	LM219	D
PM248	LM248	D
PM308	LM308	D
PM308A	LM308A	D
PM319	LM319	D
PM339A	LM339A	D
PM355	LF355	D
PM355A	LF355A	D
PM356	LF356	D
PM356A	LF356A	D
PM357	LF357	D
PM357A	LF357A	D
PM725	LM725	D
PM741	LM741	D
PM747	LM747	D
PM7533	DAC1020	D
PM7533	DAC1021	D
PM7533	DAC1022	D
PM7541	DAC1218	S
PM7541	DAC1219	S
REF-01	LM368	S
REF-01	LM369	S
REF-02	LM368-5.0	S
REF-03	LM336	S
REF-03	LM385-2.5	S
REF-43	LM136	D
SMP10	LF398	S
SMP10	LH0043	S
SMP11	LF398	S
SMP11	LH0023	S
SSM2139	LM833	S
SSM2210	LM394	S
SW-06	LF13333	D
SW-201	LF13201	D
SW-202	LF13202	D
RAYTHEON		
DAC-08	DAC0800	S
DAC-10	DAC-1020	S
DAC-10	DAC-1021	S
DAC-6012	DAC-1220	S
DAC-6012	DAC-1221	S
LH2101A	LH2101A	D
LH2111	LH2111	D
LM101A	LM101A	D
LM111	LM111	D
LM124	LM124	D
LM139	LM139	D
LM148	LM148	D
LM2900	LM2900	D
LM301A	LM301A	D
LM324	LM324	D
LM339	LM339	D
LM348	LM348	D
LM3900	LM3900	D
LP365	LP365	D
RC1458	LM1458	D
RC1558	LM1558	D
RC4156	LM348	S
RC4157	LM348	S
RC4195	LM325	S
RC4195	LM326	S
RC714	LM607	I
RC741	LM741	D
RC747	LM747	D
REF-01	LH0070	S
REF-01	LM368	S
REF-01	LM369	I
REF-02	LM336-5.0	S
REF-02	LM368-5	S
REF-03	LM368-5	I
SAMSUNG		
KA219	LM219	D
KA2803	LM1851	S
KA2807	LM1851	S
KA301	LM301	D
KA319	LM319	D
KA331	LM331	D
KA3524	LM3524D	D
KA431	LM431	D
KA710	LM710	D
KA78S40	LM78S40	D
KF347	LF347	D
KF351	LF351	D
KF442	LF442	D
LM224A	LM224A	D
LM239	LM239	D
LM248	LM248	D
LM258A	LM258A	S
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM2903	D
LM2904	LM2904	D
LM293	LM293	D
LM311	LM311	D
LM324	LM324	D
LM324A	LM324A	D
LM3302	LM3302	D
LM339A	LM339A	D
LM348	LM348	D
LM358A	LM358A	D
LM393	LM393	D
LM393A	LM393A	D
LM741	LM741	D
MC1458	LM1458	D
MC78LXX	LM78LXX	D
MC78MXX	LM78MXX	D

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Part Number	NSC Part Number	
SAMSUMG (Continued)		
MC78XX	LM78XX	D
MC79MXX	LM79MXX	D
MC79XX	LM79XX	D
NE555	LM555	D
NE556	LM556	D
SGS THOMPSON		
μA741	LM741	D
μA748	LM748	D
L293	LM18293	D
L4940	LM2940	S
L4941	LM2940	S
L78MXX	LM78MXX	D
L78S05	LM323	I
L78XX	LM340-XX	D
L78XX	LM78XX	D
L7912	LM7912	D
L79XX	LM320-XX	D
L79XX	LM79XX	D
LF198	LF198	D
LF255	LF255	D
LF256	LF256	D
LF257	LF257	D
LF298	LF298	D
LF351	LF351	D
LF353	LF353	D
LF355	LF355	D
LF355A	LF355A	D
LF356	LF356	D
LF356A	LF356A	D
LF357	LF357	D
LF357A	LF357A	D
LF398	LF398	D
LM101A	LM101A	D
LM109	LM109	D
LM117	LM117	D
LM123	LM123	D
LM124	LM124	D
LM124A	LM124A	D
LM134	LM134	D
LM135	LM135	D
LM137	LM137	D
LM139	LM139	D
LM139A	LM139A	D
LM148	LM148	D
LM158	LM158	D
LM158A	LM158A	D
LM1837	LM1837	D
LM193	LM193	D
LM193A	LM193A	D
LM201A	LM201A	D
LM208	LM208	D
LM211	LM211	D
LM218	LM218	D
LM219	LM219	D
LM223	LM223	D
LM224	LM224	D
LM224A	LM224A	D
LM234	LM234	D
LM235	LM235	D
LM236	LM236	D
LM239	LM239	D
LM239A	LM239A	D
LM246	LM246	D
LM248	LM249	D
LM258	LM258	D
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM3903	D
LM2904	LM2904	D
LM293	LM293	D
LM2930	LM2930	D
LM2931A	LM2931A	D
LM301A	LM301A	D
LM308	LM308	D
LM308A	LM308A	D
LM311	LM311	D
LM318	LM318	D
LM319	LM319	D
LM323	LM323	D
LM324	LM324	D
LM324A	LM324A	D
LM334	LM334	D
LM335	LM335	D
LM336	LM336	D
LM336B	LM336B	D
LM339	LM339	D
LM339A	LM339A	D
LM346	LM346	D
LM348	LM348	D
LM358	LM358	D
LM358A	LM358A	D
LM393	LM393	D
LM393A	LM393A	D
NE555	LM555	D
NE556	LM556	D
SE555	LM555	D
SG556	LM556	D
SG2524	LM2524	D
SG3524	LM3524	D
SG3525	LM3525	D
SG3527	LM3527	D
TSA2040	LM1875	S
TS272	LMC662	S
TS274	LMC660	S
TS27L2	LPC662	S
TS27L4	LPC660	S
TS27M2	LMC662	S
TS27M4	LMC660	S
SIGNETICS		
μA723	LM723	D
μA741	LM741	D
μA747	LM747	D
ADC0801	ADC0801	D
ADC0802	ADC0802	D
ADC0803	ADC0803	D
ADC0804	ADC0804	D
ADC0805	ADC0805	D
ADC0820	ADC0820	D
CA3089N	LM3089	D

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Part Number	NSC Part Number	
SIGNETICS (Continued)		
DAC-08	DAC0800	D
DAC-08	DAC0801	D
DAC-08	DAC0802	D
ICM7555	LMC555	D
LF198	LF198	D
LF298	LF298	D
LF398	LF398	D
LM2901	LM2901	D
LM2903	LM2903	D
LM311	LM311	D
LM319	LM319	D
LM324	LM324	D
LM339	LM339	D
LM358	LM358	D
LM393	LM393	D
MC1408	DAC0807	D
MC1458	LM1458	D
MC1496	LM1496	D
NE5034	ADC0841	S
NE5118	DAC0830	S
NE529	LM361	S
NE532	LM358	D
NE5410	DAC1020	S
NE5517	LM13600	D
NE5537	LF398	D
NE555	LM555	D
NE565	LM565	D
NE566	LM566	D
NE567	LM567	D
SA532	LM2904	I
SA534	LM2902	I
SE5118	DAC0830	S
SE529	LM161	S
SE532	LM158	S
SE5410	DAC1020	S
SE566	LM566	D
SE567	LM567	D
SG3524	LM3524	D

Part Number	NSC Part Number	
SILICONIX		
DG201	LF13201	D
DG202	LF13202	D
DG211	LF13201	D
DG212	LF13202	D
DG508	LF13508	D
DG509	LF13509	D
TEXAS INSTRUMENTS		
UA2240	LM2240	D
μA709	LM709	D
μA723	LM723	D
μA741	LM741	D
μA747	LM747	D
μA748	LM748	D
μA78LXX	LM78LXX	D
μA78MXX	LM78MXX	D
μA78XX	LM78XX	D
μA79MXX	LM79MXX	D
μA79XX	LM79XX	D
ADC0803	ADC0803	D
ADC0804	ADC0804	D
ADC0805	ADC0805	D
ADC0808	ADC0808	D
ADC0809	ADC0809	D
ADC0820	ADC0820	D
ADC0831	ADC0831	D
ADC0832	ADC0832	D
ADC0834	ADC0834	D
ADC0838	ADC0838	D
LF198	LF198	D
LF347	LF347	D
LF351	LF351	D
LF353	LF353	D
LF398	LF398	D
LF411	LF411	D
LF412	LF412	D
LM101A	LM101A	D
LM107	LM107	D
LM108	LM108	D
LM111	LM111	D
LM124	LM124	D
LM139	LM139	D
LM148	LM148	D

Part Number	NSC Part Number	
LM158	LM158	D
LM185	LM185	D
LM193	LM193	D
LM201	LM201	D
LM207	LM207	D
LM211	LM211	D
LM217	LM217	D
LM218	LM218	D
LM224	LM224	D
LM237	LM137	D
LM239	LM239	D
LM248	LM248	D
LM258	LM258	D
LM2900	LM2900	D
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM2903	D
LM2904	LM2904	D
LM2907	LM2907	D
LM2917	LM2917	D
LM293	LM293	D
LM2930	LM2930	D
LM2931	LM2931	D
LM301	LM301	D
LM307	LM307	D
LM317	LM317	D
LM318	LM318	D
LM324	LM324	D
LM330	LM330	D
LM337	LM337	D
LM339	LM339	D
LM348	LM348	D
LM358	LM358	D
LM385	LM385	D
LM3900	LM3900	D
LM393	LM393	D
LP111	LP311	S
LP211	LP311	S
LP239	LP339	S
LP2901	LP339	S

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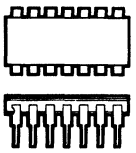
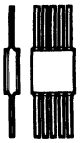
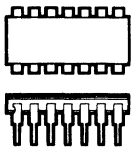
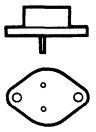
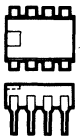
Part Number	NSC Part Number	
TEXAS INSTRUMENTS (Continued)		
LP311	LP311	D
LP339	LP339	D
LT1004	LM385	D
LT1009	LM336	D
MC1458	LM1458	D
MC155	LM1558	D
MC3303	LM3303	D
MC3403	LM3403	D
MC79LXX	LM79LXX	D
MF10	MF10	D
MF4	MF4	D
NE555	LM555	D
NE555	LM556	D
NE592	LM592	D
OP07	OP07	D
OP27	LM627	I
OP37	LM63	I
RC4136	LM4136	D
RC4558	LM833	D
SA555	LM555	D
SA556	LM556	D
SE2524	LM2524D	I
SE3524	LM3524D	I
SE555	LM555	D
SE556	LM556	D
SE592	LM592	D
TL061	LF441	I
TL062	LF442	I
TL064	LF444	I
TL071	LF351	I
TL071	LF411	I
TL072	LF353	I
TL072A	LF412	I
TL074	LF347	I
TL0808	ADC0808	D
TL0809	ADC0809	D
TL081	TL081	D
TL082	TL082	D
TL084	LF347	I
TL087	LF411	S
TL088	LF411	S
TL287	LF412	S
TL288	LF412	S
TL317	LM317	D
TL431	LM431	D
TL592	LM592	D
TLC04	MF4	D
TLC0820	ADC0820	D
TLC10	MF10	D
TLC1225	ADC1225	D
TLC14	MF4-100	D
TLC1541	ADC1031	S
TLC20	MF10	D
TLC252	LMC662	S
TLC254	LMC660	S
TLC25L2	LMC662	S
TLC25M2	LMC662	S
TLC25M4	LMC660	S
TLC27L2	LMC6042	I
TLC27L4	LMC6044	I
TLC27L7	LMC6062A	I
TLC27M2	LMC662	S
TLC27M4	LMC660	S
TLC271	LMC6041	I
TLC272	LMC6032	I
TLC274	LMC6034	I
TLC277	LMC6082A	I
TLC339	LP339	S
TLC532	ADC0829	S
TLC533	ADC0829	D
TLC540	ADC0811	S
TLC541	ADC0811	D
TLC545	ADC0819	S
TLC546	ADC0819	D
TLC549	ADC0831	S
TLC555	LMC555	D
TOSHIBA		
TA7133	LM1391	S
TA7140	LM386	S
TA7230	LM1877	S
TA7232	LM2896	S
TA7233	LM2877	S
TA7268	LM1875	S
TA7269	LM2878	S
TA7282	LM2896	S
TA7283	LM2896	S
TA7313	LM386	S
TA7336	LM390	S
TA7366	LM3914	S
TA7367	LM3914	S
TA7370	LM3361	S
TA7504	LM741	D
TA75061	LF441	I
TA75062	LF442	I
TA75064	LF444	I
TA75071	LF351	I
TA75072	LF353	I
TA75074	LF347	I
TA75092	LM2902	I
TA75092	LM324	S
TA75339	LM2901	D
TA75339	LM339	D
TA75358	LM2904	I
TA75358	LM358	D
TA75393	LM2903	I
TA75393	LM393	D
TA75458	LM1558	D
TA7555	LM555	D
TA7612	LM3914	S
TA7613	LM1868	S
TA7630	LM1036	S
TA7640	LM1868	S
TA76524	LM3624	S
TA7654	LM3914	S
TA7667	LM3915	S
TA7688	LM1896	S
TA7758	LM1868	S
TA7769	LM1896	S
TA78LXX	LM78LXX	D
TA78MXX	LM78MXX	D
TA78XXX	LM78XX	D
TA79LXXX	LM79LXX	D
TA79XXX	LM79XX	D
TA8117	LM1868	S
TA8119	LM1896	S
TA8202	LM1877	S
TA8211	LM2878	S
TC9154	LMC1982	S
UNITRODE		
L293	LM18293	D
UC117	LM117	D
UC137	LM137	D
UC150	LM150	D
UC1524	LM1524D	I
UC2524	LM2524D	I
UC317	LM317	D
UC337	LM337	D
UC350	LM350	D
UC3524	LM3524D	I
UC78XX	LM340-XX	D
UC78XX	LM78XX	D
UC79XX	LM320-XX	D
UC79XX	LM79XX	D

The following notations are appended to assist you in finding the best option.

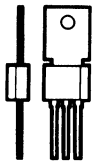
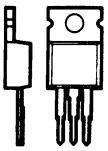
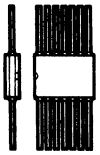
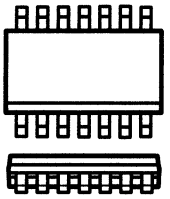
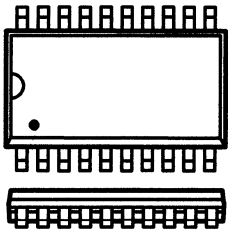
S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

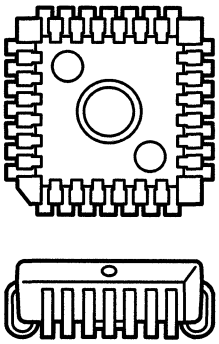
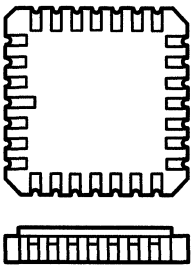
Industry Package Cross-Reference Guide

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Spraque
 4/16 Lead Glass/Metal DIP	D	D	I	L		D	R
 Glass/Metal Flat Pack	F	F	Q	F	F, S	F	
 TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	H	
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J	D	H
 TO-3 (Steel)	K			KS			
TO-3 (Aluminum)	KC	K	DA	K	K		
 8-, 14- and 16-Lead Plastic DIP	N	T, P	N, V	P	P, N	P	A, B, M

*With dual-in-line formed leads

**With radically formed leads

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
 TO-202 (D-40, Durawatt)	P						
 TO-220 3- & 5-Lead	T	U	U		KC		
TO-220 11-, 15- & 23-Lead	T						
 Low Temperature Glass Hermetic Flat Pack	W	F		F	W	F	
 TO-92 (Plastic)	Z	W	S	P	LP		
 SO (Narrow Body)	M	S	S, D	D	D		L
 (Wide Body)	WM				DW		LW

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Spraque
 PCC	V	Q	A	FN	FN	L	EP
 LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	L	EK

Section 1

Audio Circuits

Section 1 Contents

National Semiconductor

Audio Circuits Definition of Terms

Amplifier

Class A

A class A transistor audio amplifier refers to an amplifier with a single output device that has a collector flowing for the full 360° of the input cycle.

Class B

The most common type of audio amplifier that basically consists of two output devices each of which conducts for 180° of the input cycle.

Class C

In a class C amplifier the collector current flows for less than 180°. Although highly efficient, high distortion results and the load is frequently tuned to minimize this distortion (primarily used in R.F. power amplifiers).

Class D

A switching or sampling amplifier with extremely high efficiency (approaching 100%). The output devices are used as switches, voltage appearing across them only while they are off, and current flowing only when they are saturated.

Crossover Distortion

Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current allowing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for I/Cs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion for negative going transition through zero at the higher audio frequencies.

Dolby B

Dolby B is a simplified version of the Dolby A professional quality noise reduction system. The amplitude of low level signals over a selected frequency range is increased prior to recording to enhance them above tape noise. On playback the original levels are restored causing a corresponding reduction in the audible tape noise. The major difference with Dolby A which used four frequency bands, is the use of a single variable frequency band with a cut-off frequency that increases in the presence of high level high frequency signals.

Dolby Level

Because of the complementary nature of the Dolby B noise reduction system, the audio channel between the encoder and the decoder must have a fixed gain such that the decoding signal level is within 2 dB of the encoding signal level. Also if recordings are interchangeable the signals in the noise reduction system must be related to the levels in the audio channel. Dolby level provides this reference and corresponds to a specified tape flux density when recorded with a 400 Hz tone. For reel to reel and eight track cartridge tapes this is 185 nWb/m, and for cassettes Dolby level is 200 nWb/m.

Large-Signal Voltage Gain

The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Resistance

The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing

The peak output voltage swing, referred to zero, that can be obtained without clipping.

Power Bandwidth

The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated at 60 watts with $\leq$0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30 watts.

Power Supply Rejection

The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate

The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Thermal Resistance (R_{TH})

An analogy for heat transfer where the ability of a heat conductive system to transfer heat is described in similar terms to those used in an electrical system for power dissipated in a resistor with a given applied voltage. The thermal resistance is given by the temperature differential established when a given amount of power is being dissipated ($\theta = T1 - T2/P_D$) with units of °C/watt.

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Audio Circuits Selection Guide

Preamplifiers/Systems

	Application			Package	Voltage Range	Equivalent Input Noise	THD	PSR	Input Coupling	Notes
	Portable	Home	Auto							
LM833 (Note 1)		•	•	8 Pin DIP 8 Pin SO	±5V–±15V	0.5 μV	0.002%	100 dB	DC	Low Noise Dual Op Amp
LM837 (Note 1)		•	•	14 Pin DIP 14 Pin SO	±5V–±15V	0.5 μV	0.002%	100 dB	DC	Low Noise Quad Op Amp Drives 600Ω Load

Audio Power Amplifiers

	Application			Package	Power*			@ Voltage	Bridgeable	THD*	Input Noise*	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM380		•		8 Pin DIP 14 Pin DIP	2.5W			18V		0.2%		Single	See AN-69 Fixed Gain
LM383	•		•	5 Pin TO-220		5.5W	8.6W	14.4V	Yes	0.2%	2 μV	Single	Protected
LM384		•		14 Pin DIP	5.5W			22V	Yes	0.25%		Single	Fixed Gain
LM386	•	•		8 Pin DIP 8 Pin SO	0.33W			6V		0.2%		Single	4V Operation 20 mW Quiescent
LM388	•			14 Pin DIP	2.2W			12V	Yes	0.1%		Single	4V Operation Min Externals
LM389	•			18 Pin DIP	0.33W			6V		0.2%		Single	Includes Transistor Array
LM831	•	•		16 Pin DIP 16 Pin SOIC	0.44W			3V	Yes	0.25%	3 μV	Dual	1.8V-6V
LM390	•			14 Pin DIP		1W		6V	Yes	0.2%		Single	Battery Operation
LM391		•		16 Pin DIP	10–100W			60V–100V	Yes	0.01%	3 μV	Single	Shutdown Pin, Thermal Protected Power Driver
LM1877	•	•	•	14 Pin DIP	3W			20V		0.05%	2.5 μV	Dual	6V–24V
LM2877	•	•	•	11 Pin SIP	4.5W			20V		0.07%	2.5 μV	Dual	Flexible Application

Audio Power Amplifiers (Continued)

	Application			Package	Power*			@ Voltage	Bridgeable	THD*	Input Noise*	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM1896	•	•	•	14 Pin DIP		1.1W		6V	Yes	0.1%	1.4 μV	Dual	Low AM Radiation, 3V Op
LM2896	•	•	•	11 Pin SIP		2.5W		9V	Yes	0.1%	1.4 μV	Dual	No Pops, 3–15V Op
LM2878		•		11 Pin SIP	5.5W			22V	Yes	0.15%	2.5 μV	Dual	6V–32V
LM12		•		4-Pin TO-3	50W	85W		±30V	Yes	0.01%	9 μV	Single	Power Op Amp; See AN-446
LM1875		•		5 Pin TO-220	25W			±25V		0.015%	3 μV	Single	Low Distortion At H. Power
LM2879		•		11 Pin TO-220	8W			28V	Yes	0.05%	2.5 μV	Dual	6V–32V

*Note that all values shown are typical. Please refer to datasheets for test conditions.

Audio Controls

	Application			Package	Voltage Range	Volume Control Range	Signal to Noise	THD	Separation	Notes
	Portable	Home	Auto							
LM1035/ LM1036		•	•	20 Pin DIP	8V–18V	80 dB	80 dB	0.05%	75 dB	Dual DC Controlled Tone/Volume/Balance
LM1037	•	•	•	18 Pin DIP	5V–25V		100 dB	0.04%	100 dB	DC Audio Switch
LM13600 (Note 1)	•	•	•	16 Pin DIP 16 Pin SO	±2V–±18V			0.5%	100 dB	Dual Transconductance Amplifiers
LM13700	•	•	•	16 Pin DIP 16 Pin SO						
LM3080 (Note 1)	•	•	•	8 Pin DIP	±2V–±18V					Transconductance Amplifier
LM1040		•	•	24 Pin DIP	9V–16V	75 dB	80 dB	0.06%	75 dB	Dual DC Controlled Tone/Volume/Balance Stereo Enhancement
LMC835	•	•	•	28 Pin DIP	±2.5V–±8V	±12 dB/Band	114 dB	*		7 Band Stereo Graphic Equalizer MICROWIRE™ Controlled; See AN-435
LMC1982		•		28 Pin DIP	7V–15V	80 dB	95 dB	0.008%	80 dB	2 Stereo Inputs Volume/ Tone/Fade/Select Enhanced Stereo Loudness Comp. IM Controlled
LMC1983		•		28 Pin DIP	7V–15V	80 dB	95 dB	0.008%	80 dB	3 Stereo Inputs Volume/ Tone/Fade/Select Loudness Comp. IM Controlled
LMC1992		•	•	28 Pin DIP	7V–15V	80 dB	105 dB	0.03%	95 dB	4 Stereo Inputs Volume/ Tone/Fade/Select MICROWIRE™ Controlled

*Distortion determined by external op amps.

Note 1: Datasheet in Operational Amplifiers Databook.

Noise Reduction

	Application			Package	Voltage Range	NR Type	NR Effect*	Encoding Required	Single/ Dual/	Decode S/N*	Notes
	Portable	Home	Auto								
LM1131	•	•	•	18 Pin DIP	5V–20V	Dolby®	10 dB	Yes	Dual	90 dB	DC Switched
LM1894	•	•	•	14 Pin DIP, SO	4.5V–18V	DNR®	12 dB	No	Dual	76 dB	NSC System
LM832	•	•		14 Pin DIP, SO	1.5V–9V	DNR®	10 dB	No	Dual	72 dB	See AN-384, 386, 390

*Note that all values shown are typical. Please refer to datasheets for test conditions.

DNR® is a registered trademark of National Semiconductor Corporation.

Dolby® is a registered trademark of Dolby Laboratories Licensing Corporation.

National Semiconductor

LM380 Audio Power Amplifier

General Description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

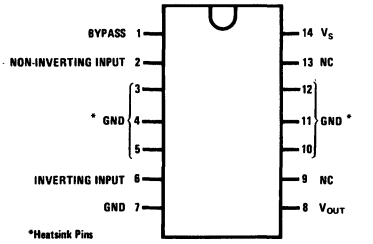
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters, etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

Features

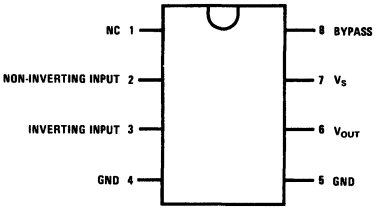
- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

Connection Diagrams (Dual-In-Line Packages, Top View)



TL/H/6977-1

Order Number LM380N
See NS Package Number N14A

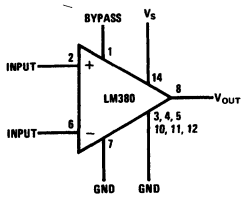


TL/H/6977-2

Order Number LM380N-8
See NS Package Number N08E

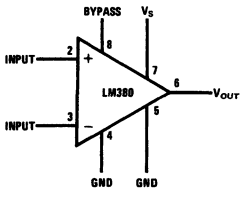
Block and Schematic Diagrams

LM380N

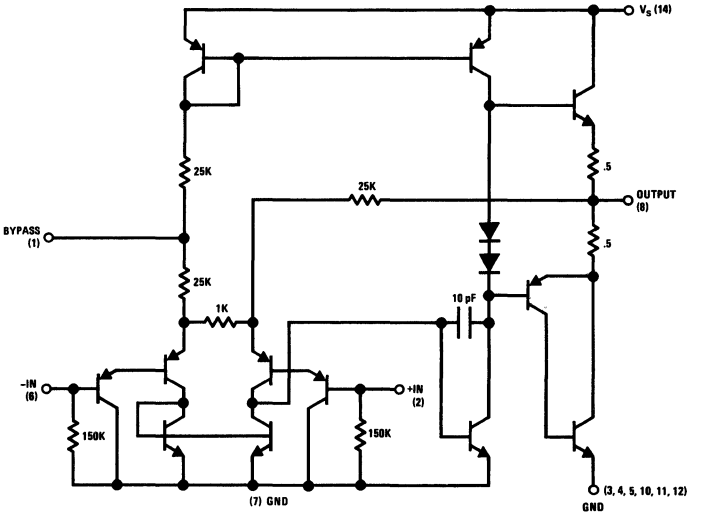


TL/H/6977-3

LM380N-8



TL/H/6977-4



TL/H/6977-5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	22V
Peak Current	1.3A
Package Dissipation 14-Pin DIP (Notes 6 and 7)	8.3W
Package Dissipation 8-Pin DIP (Notes 6 and 7)	1.67W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
ESD rating to be determined	

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$P_{OUT(RMS)}$	Output Power	$R_L = 8\Omega$, THD = 3% (Notes 3, 4)	2.5			W
A_V	Gain		40	50	60	V/V
V_{OUT}	Output Voltage Swing	$R_L = 8\Omega$		14		V_{p-p}
Z_{IN}	Input Resistance			150k		Ω
THD	Total Harmonic Distortion	(Notes 4, 5)		0.2		%
PSRR	Power Supply Rejection Ratio	(Note 2)		38		dB
V_S	Supply Voltage		10		22	V
BW	Bandwidth	$P_{OUT} = 2W$, $R_L = 8\Omega$		100k		Hz
I_Q	Quiescent Supply Current			7	25	mA
V_{OUTQ}	Quiescent Output Voltage		8	9.0	10	V
I_{BIAS}	Bias Current	Inputs Floating		100		nA
I_{SC}	Short Circuit Current			1.3		A

Note 1: V_S = 18V and T_A = 25°C unless otherwise specified.

Note 2: Rejection ratio referred to the output with C_{BYPASS} = 5 μF.

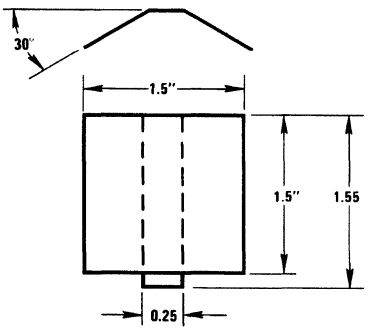
Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of 6 square inches.

Note 4: C_{BYPASS} = 0.47 μfd on Pin 1.

Note 5: The maximum junction temperature of the LM380 is 150°C.

Note 6: The package is to be derated at 15°C/W junction to heat sink pins for 14-pin pkg; 75°C/W for 8-pin.

Heat Sink Dimensions

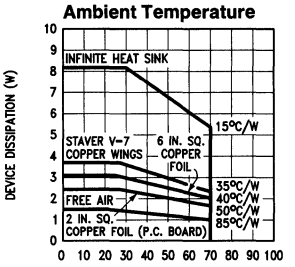


Staver Heat Sink #V-7
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bayshore, NY 11706
Tel: (516) 666-8000
Copper Wings
2 Required
Soldered to
Pins 3, 4, 5,
10, 11, 12
Thickness 0.04
Inches

TL/H/6977–6

Typical Performance Characteristics

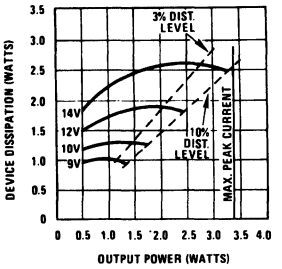
Maximum Device Dissipation vs Ambient Temperature



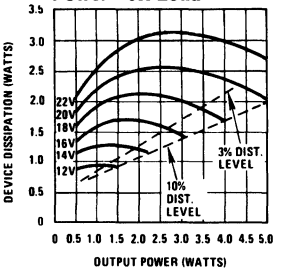
Note: 2 oz. copper foil, single-sided PC board.

TL/H/6977–12

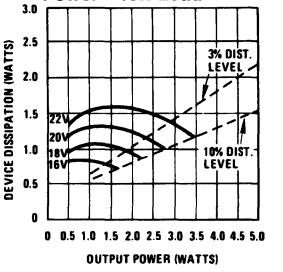
Device Dissipation vs Output Power—4Ω Load



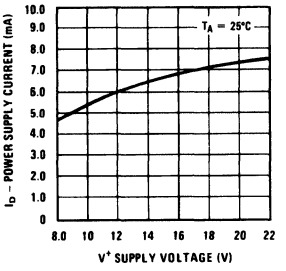
Device Dissipation vs Output Power—8Ω Load



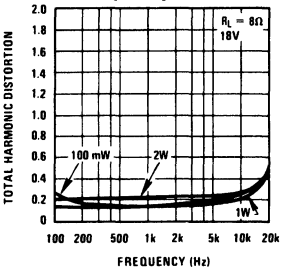
Device Dissipation vs Output Power—16Ω Load



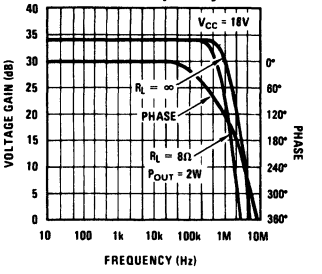
Power Supply Current vs Supply Voltage



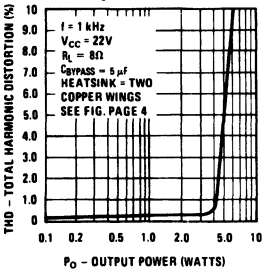
Total Harmonic Distortion vs Frequency



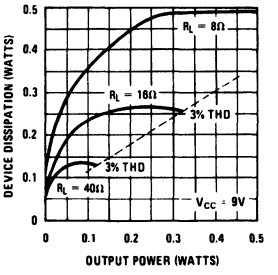
Output Voltage Gain and Phase vs Frequency



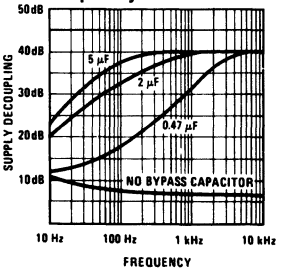
Total Harmonic Distortion vs Output Power



Device Dissipation vs Output Power



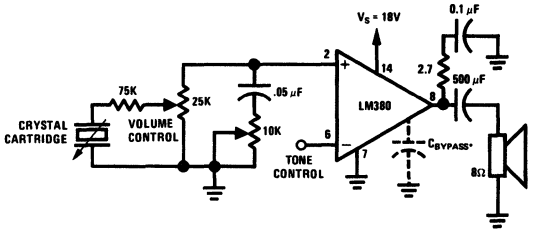
Supply Decoupling vs Frequency



TL/H/6977–7

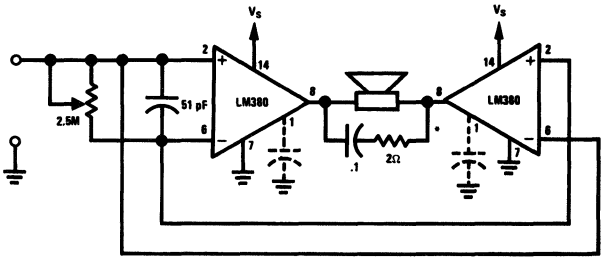
Typical Applications

Phono Amplifier



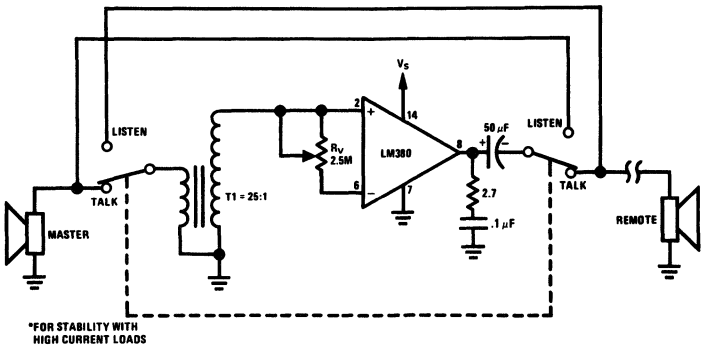
TL/H/6977–8

Bridge Amplifier



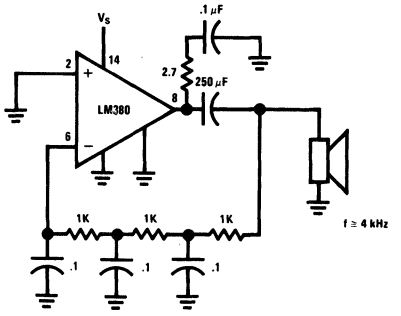
TL/H/6977–9

Intercom



TL/H/6977–10

Phase Shift Oscillator



TL/H/6977–11

National Semiconductor

LM383/LM383A 7 Watt Audio Power Amplifier

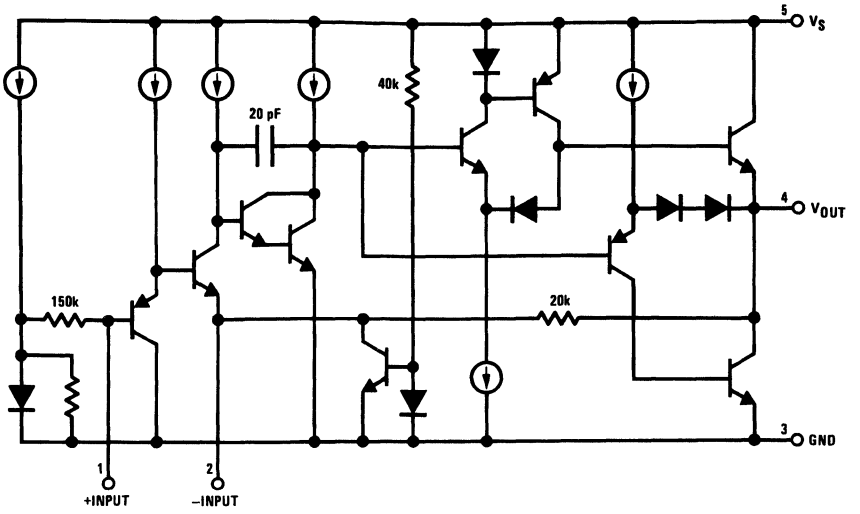
General Description

The LM383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM383 is current limited and thermally protected. High voltage protection is available (LM383A) which enables the amplifier to withstand 40V transients on its supply. The LM383 comes in a 5-pin TO-220 package.

Features

- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V–20V)
- Few external parts required
- Low distortion
- High input impedance
- No turn-on transients
- High voltage protection available (LM383A)
- Low noise
- AC short circuit protected

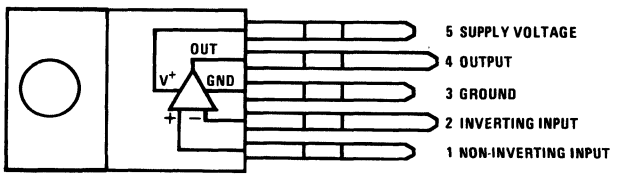
Equivalent Schematic



TL/H/7145–1

Connection Diagram

Plastic Package



TL/H/7145–2

Order Number LM383T or LM383AT
See NS Package Number T05B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Peak Supply Voltage (50 ms)	
LM383A (Note 2)	40V
LM383	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	±0.5V
Power Dissipation (Note 3)	15W
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $V_S = 14.4V$, $T_{TAB} = 25°C$, $A_V = 100$ (40 dB), $R_L = 4\Omega$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Output Level		6.4	7.2	8	V
Quiescent Supply Current	Excludes Current in Feedback Resistors		45	80	mA
Supply Voltage Range		5		20	V
Input Resistance			150		kΩ
Bandwidth	Gain = 40 dB		30		kHz
Output Power	$V_S = 13.2V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		4.7		W
	$R_L = 2\Omega$, THD = 10%		7.2		W
	$V_S = 13.8V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		5.1		W
	$R_L = 2\Omega$, THD = 10%		7.8		W
	$V_S = 14.4V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%	4.8	5.5		W
	$R_L = 2\Omega$, THD = 10%	7	8.6		W
	$R_L = 1.6\Omega$, THD = 10%		9.3		W
	$V_S = 16V$, f = 1 kHz				
	$R_L = 4\Omega$, THD = 10%		7		W
	$R_L = 2\Omega$, THD = 10%		10.5		W
	$R_L = 1.6\Omega$, THD = 10%		11		W
THD	$P_O = 2W$, $R_L = 4\Omega$, f = 1 kHz		0.2		%
	$P_O = 4W$, $R_L = 2\Omega$, f = 1 kHz		0.2		%
Ripple Rejection	$R_S = 50\Omega$, f = 100 Hz	30	40		dB
	$R_S = 50\Omega$, f = 1 kHz		44		dB
Input Noise Voltage	$R_S = 0$, 15 kHz Bandwidth		2		μV
Input Noise Current	$R_S = 100$ kΩ, 15 kHz Bandwidth		40		pA

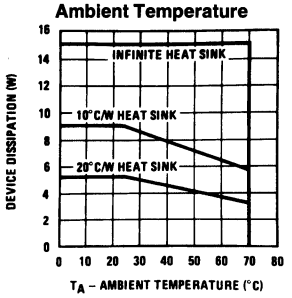
Note 1: A 0.2 μF capacitor in series with a 1Ω resistor should be placed as close as possible to pins 3 and 4 for stability.

Note 2: The LM383 shuts down above 25V.

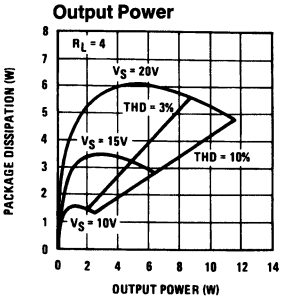
Note 3: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 4°C/W junction to case.

Typical Performance Characteristics

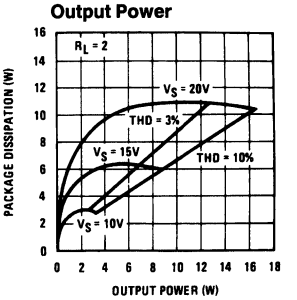
Device Dissipation vs Ambient Temperature



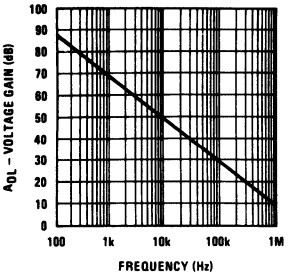
Power Dissipation vs Output Power



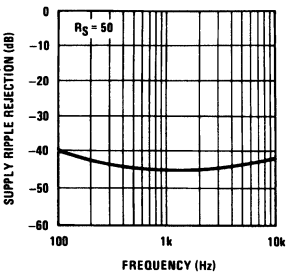
Power Dissipation vs Output Power



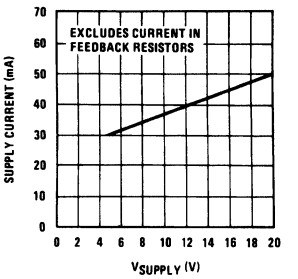
Open Loop Gain vs Frequency



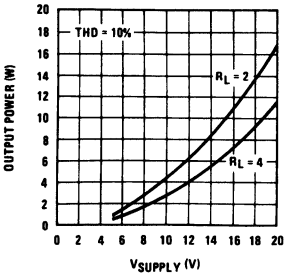
Supply Ripple Rejection vs Frequency



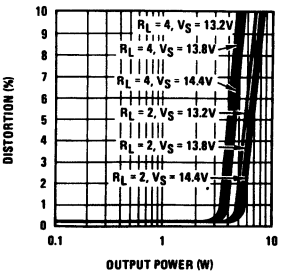
Supply Current vs Supply Voltage



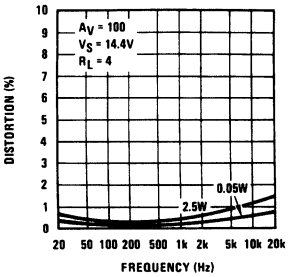
Output Power vs Supply Voltage



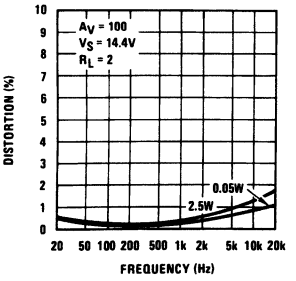
Distortion vs Output Power



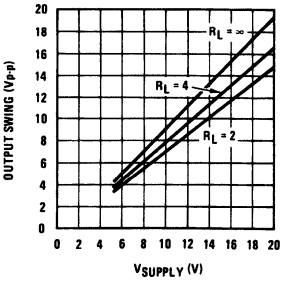
Distortion vs Frequency



Distortion vs Frequency



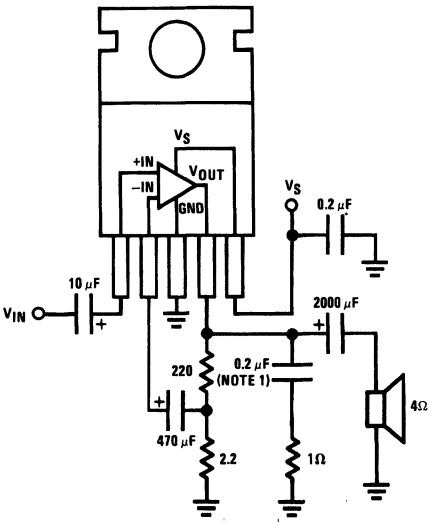
Output Swing vs Supply Voltage



TL/H/7145–4

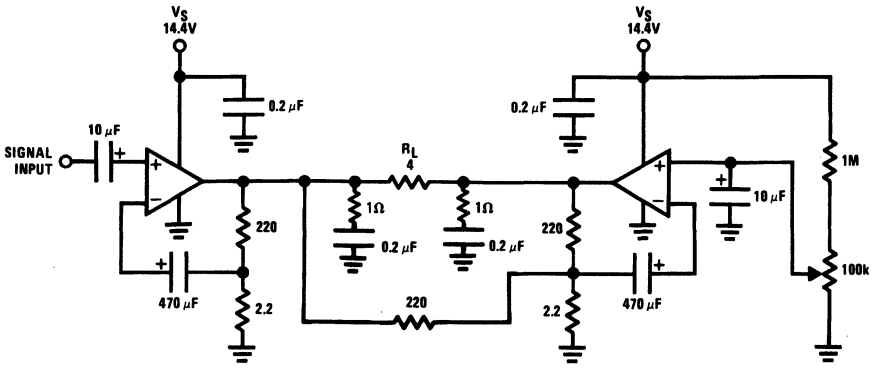
Typical Applications

Single Amplifier



TL/H/7145–3

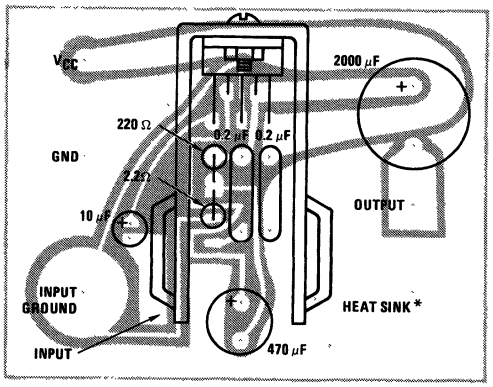
16W Bridge Amplifier



TL/H/7145–5

Component Layout

Single Amplifier
V_S = 20V
R_L = 4Ω



* Staver V-5

Heatsink from:
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bay Shore, NY 11706
Tel: (516) 666-8000

TL/H/7145–6

National Semiconductor

LM384 5 Watt Audio Power Amplifier

General Description

The LM384 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self-centering to one half the supply voltage.

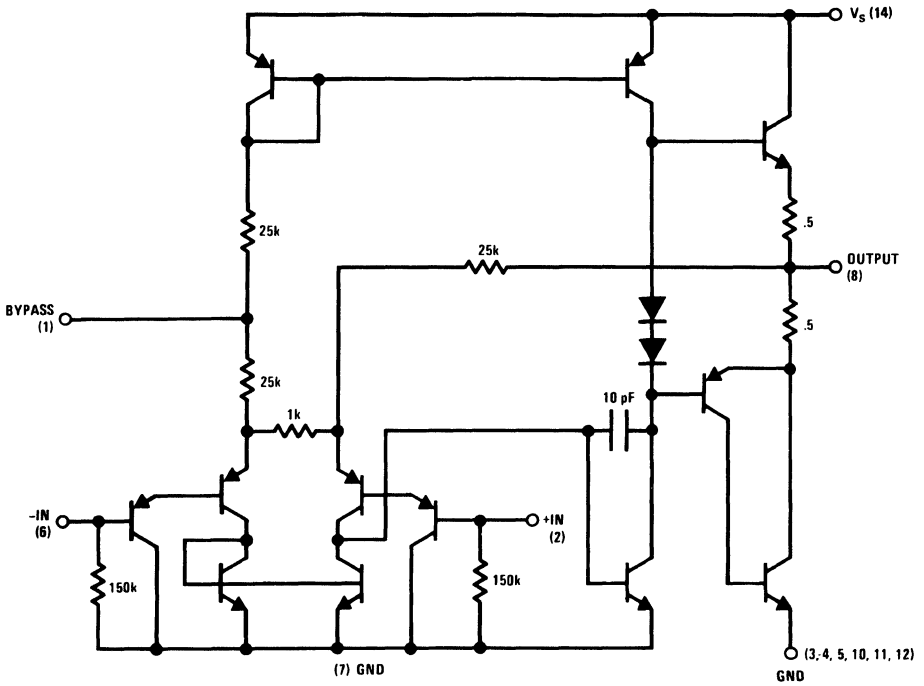
The output is short-circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, sound projector systems, etc. See AN-69 for circuit details.

Features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one half of the supply voltage
- Standard dual-in-line package

Schematic Diagram



TL/H/7843–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	28V
Peak Current	1.3A
Power Dissipation (See Notes 3 and 4)	1.67W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Z_{IN}	Input Resistance			150		kΩ
I_{BIAS}	Bias Current	Inputs Floating		100		nA
A_V	Gain		40	50	60	V/V
P_{OUT}	Output Power	THD = 10%, R_L = 8Ω	5	5.5		W
I_Q	Quiescent Supply Current			8.5	25	mA
$V_{OUT\,Q}$	Quiescent Output Voltage			11		V
BW	Bandwidth	P_{OUT} = 2W, R_L = 8Ω		450		kHz
V^+	Supply Voltage		12		26	V
I_{SC}	Short Circuit Current (Note 5)			1.3		A
$PSRR_{RTO}$	Power Supply Rejection Ratio (Note 2)			31		dB
THD	Total Harmonic Distortion	P_{OUT} = 4W, R_L = 8Ω		0.25	1.0	%

Note 1: V^+ = 22V and T_A = 25°C operating with a Staver V7 heat sink for 30 seconds.

Note 2: Rejection ratio referred to the output with C_{BYPASS} = 5 μF, freq = 120 Hz.

Note 3: The maximum junction temperature of the LM384 is 150°C.

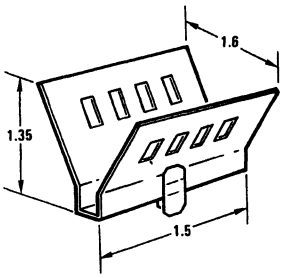
Note 4: The package is to be derated at 15°C/W junction to heat sink pins.

Note 5: Output is fully protected against a shorted speaker condition at all voltages up to 22V.

Heat Sink Dimensions

Staver Company
41 Saxon Ave.
P.O. Drawer H
Bay Shore, N.Y.
Tel: (516) 666-8000

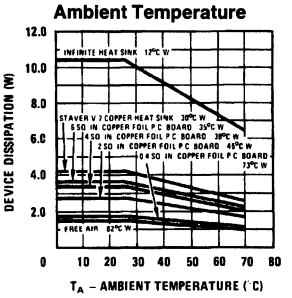
Staver "V7" Heat Sink



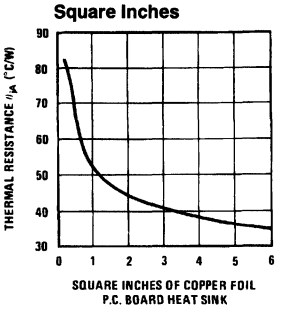
TL/H/7843–4

Typical Performance Characteristics

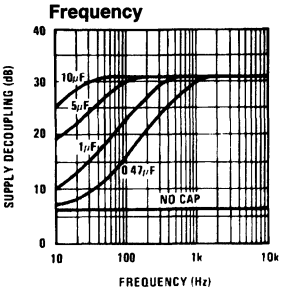
Device Dissipation vs Ambient Temperature



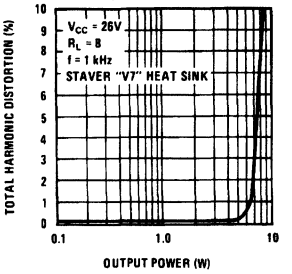
Thermal Resistance vs Square Inches



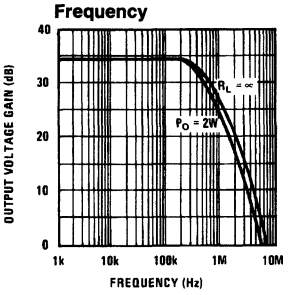
Supply Decoupling vs Frequency



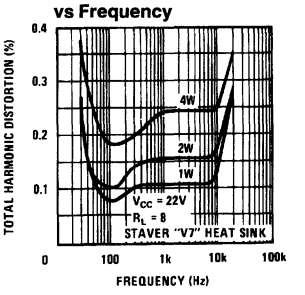
Total Harmonic Distortion vs Output Power



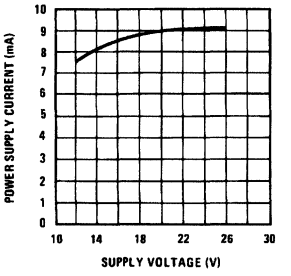
Output Voltage Gain vs Frequency



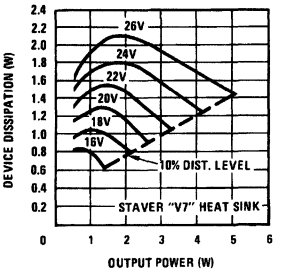
Total Harmonic Distortion vs Frequency



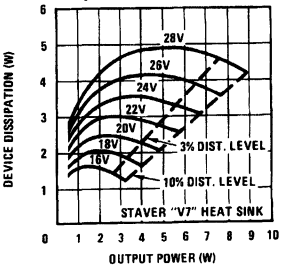
Power Supply Current vs Supply Voltage



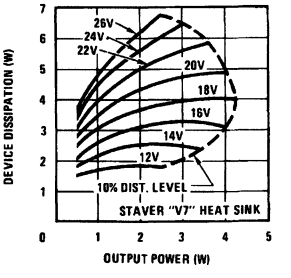
Device Dissipation vs Output Power—16Ω Load



Device Dissipation vs Output Power—8Ω Load

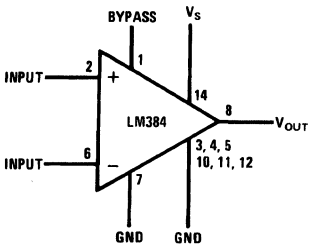


Device Dissipation vs Output Power—4Ω Load



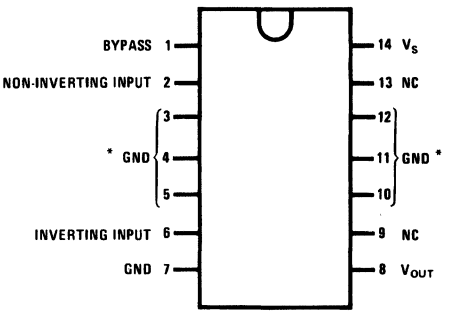
TL/H/7843–5

Block and Connection Diagrams



TL/H/7843–1

Dual-In-Line Package



*Heatsink Pins

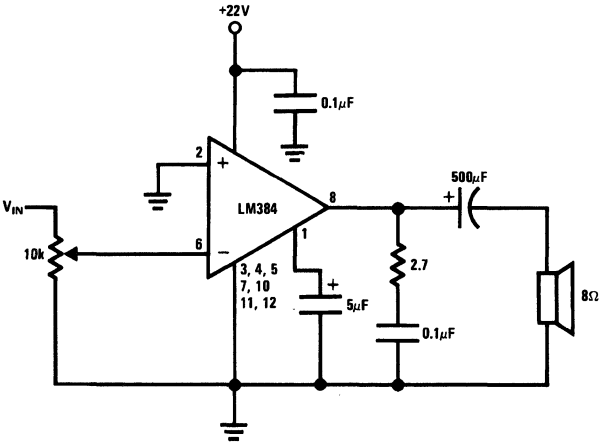
TL/H/7843–2

Top View

Order Number LM384N
See NS Package Number N14A

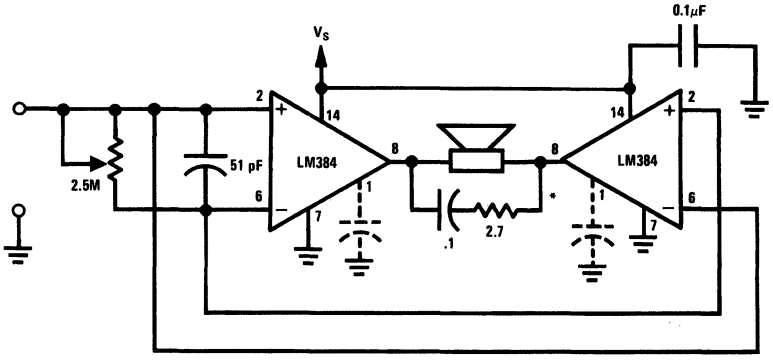
Typical Applications

Typical 5W Amplifier



TL/H/7843–6

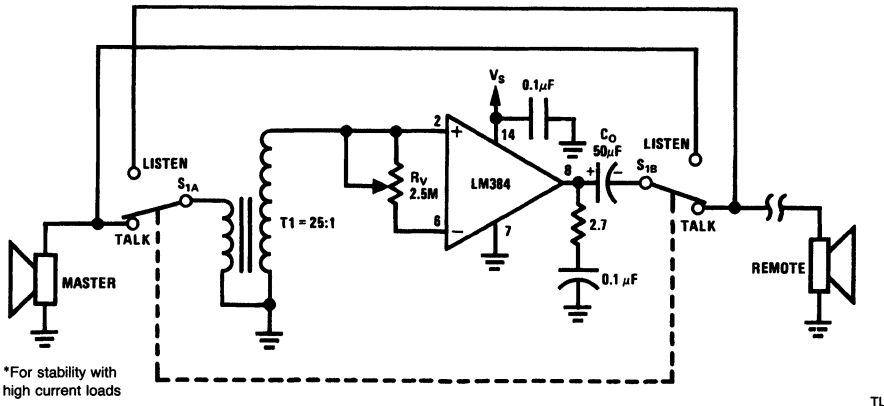
Bridge Amplifier



TL/H/7843–7

Typical Applications (Continued)

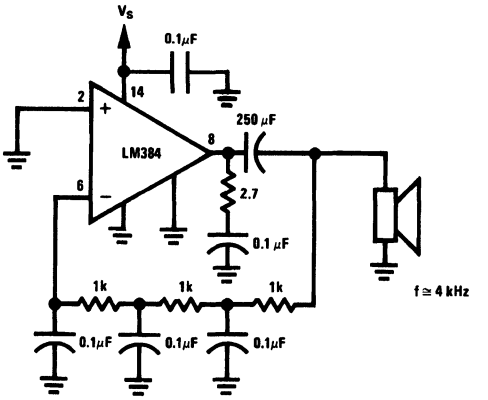
Intercom



*For stability with high current loads

TL/H/7843–8

Phase Shift Oscillator



TL/H/7843–9

National Semiconductor

LM386 Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

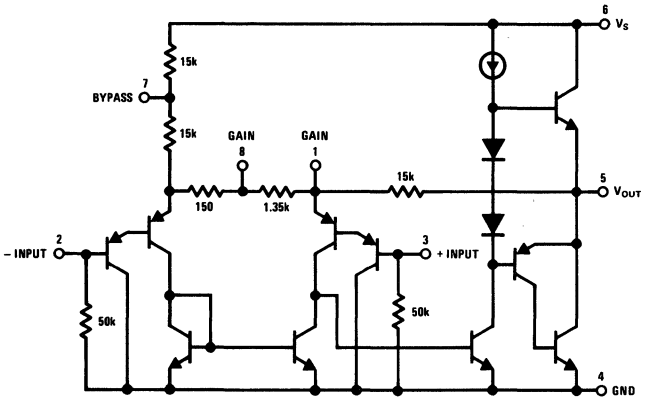
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range — 4V–12V or 5V–18V
- Low quiescent current drain — 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

Applications

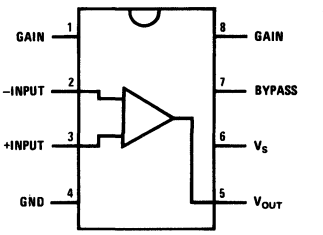
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/6976–1

Dual-In-Line and Small Outline Packages



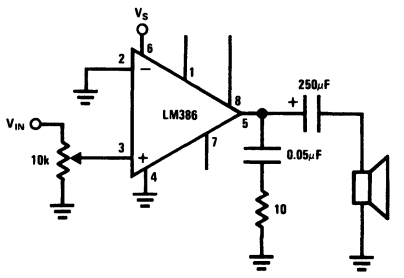
TL/H/6976–2

Top View

Order Number LM386M-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A or N08E

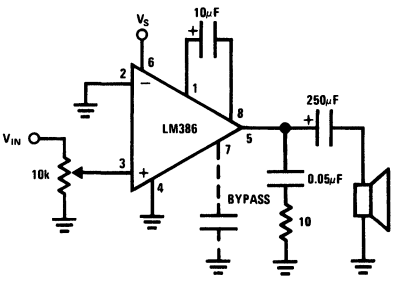
Typical Applications

Amplifier with Gain = 20
Minimum Parts



TL/H/6976–3

Amplifier with Gain = 200



TL/H/6976–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 1) (LM386N)	1.25W
(LM386M)	0.73W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 μF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 μF Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 80°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

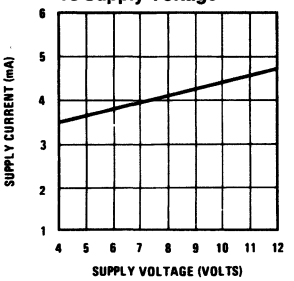
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

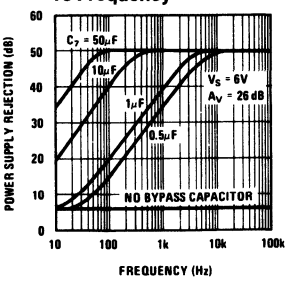
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

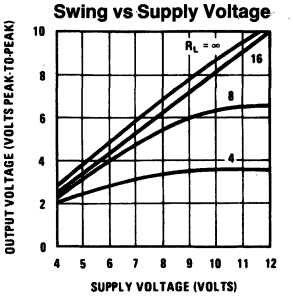
Quiescent Supply Current vs Supply Voltage



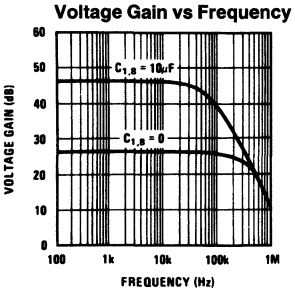
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



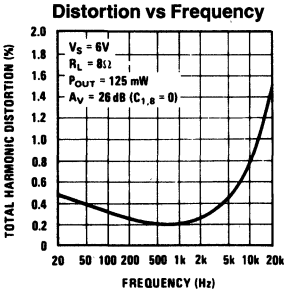
Peak-to-Peak Output Voltage Swing vs Supply Voltage



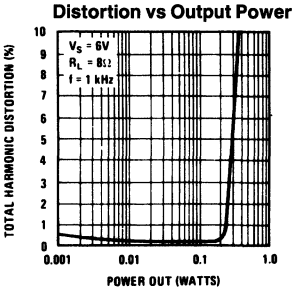
Voltage Gain vs Frequency



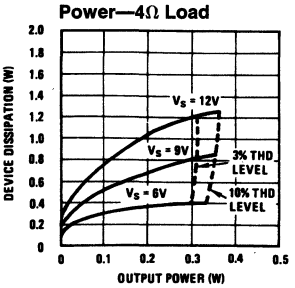
Distortion vs Frequency



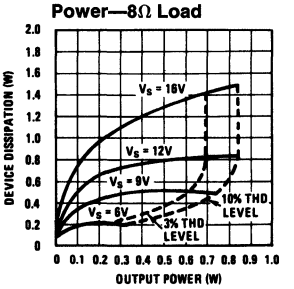
Distortion vs Output Power



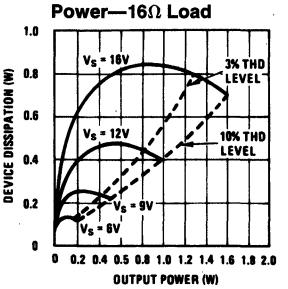
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



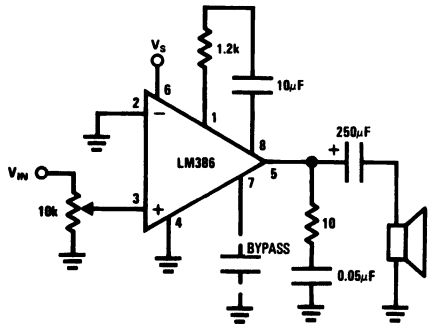
Device Dissipation vs Output Power—16Ω Load



TL/H/6976–5

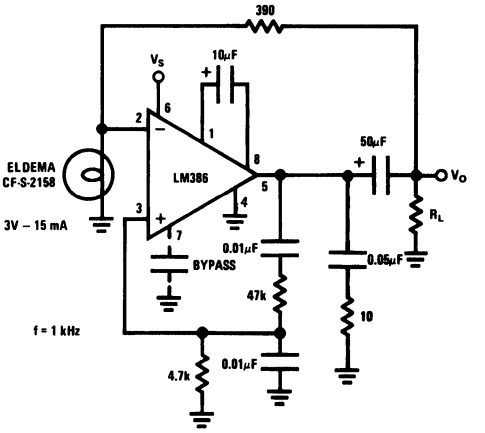
Typical Applications (Continued)

Amplifier with Gain = 50



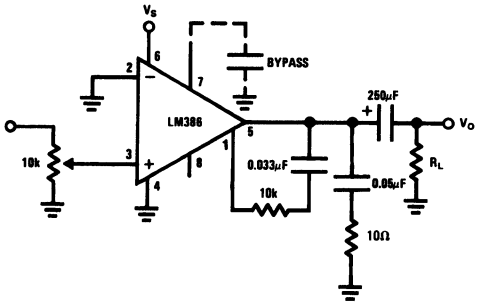
TL/H/6976–6

Low Distortion Power Wienbridge Oscillator



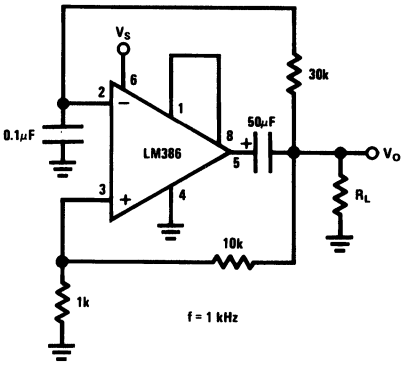
TL/H/6976–7

Amplifier with Bass Boost



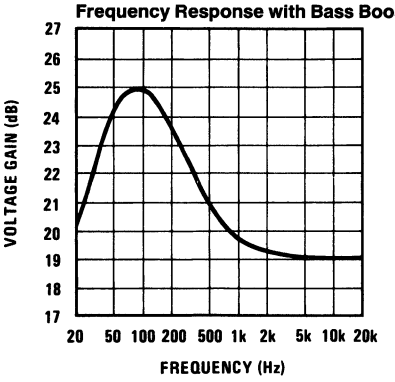
TL/H/6976–8

Square Wave Oscillator



TL/H/6976–9

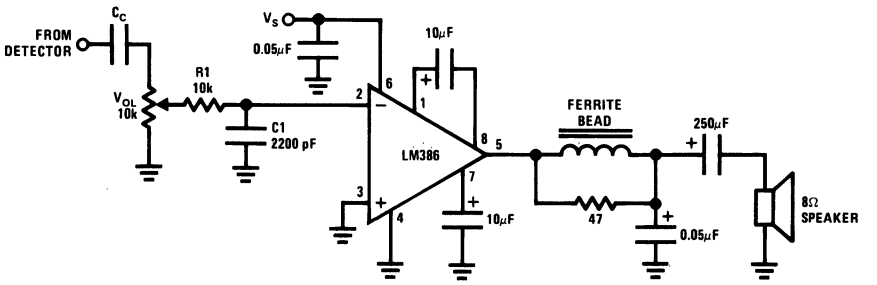
Frequency Response with Bass Boost



TL/H/6976–10

Typical Applications (Continued)

AM Radio Power Amplifier



TL/H/6976–11

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor

LM388 1.5 Watt Audio Power Amplifier

General Description

The LM388 is an audio amplifier designed for use in medium power consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

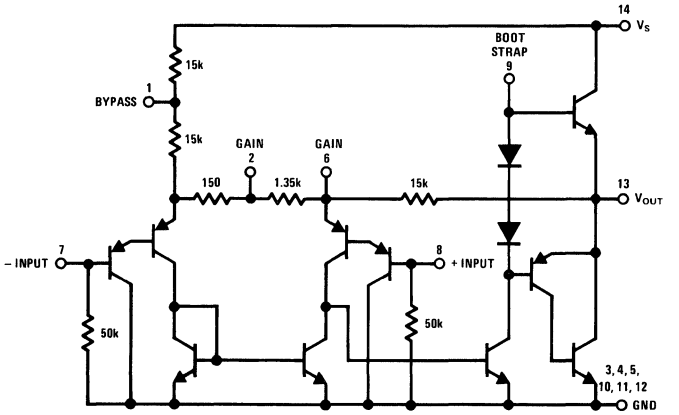
Features

- Minimum external parts
- Wide supply voltage range
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package
- Low voltage operation, 4V

Applications

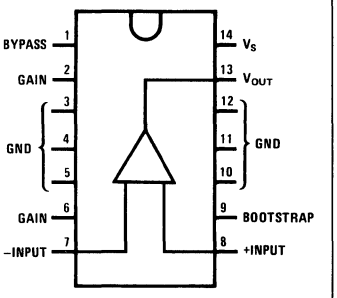
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/7846–1

Dual-In-Line Package



TL/H/7846–2

Top View

Order Number LM388N-1
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	15V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics T_A = 25°C, *(Figure 1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_S	Operating Supply Voltage LM388		4		12	V
I_Q	Quiescent Current LM388	V_{IN} = 0 V_S = 12V		16	23	mA
P_{OUT}	Output Power (Note 2) LM388N-1	R1 = R2 = 180Ω, THD = 10% V_S = 12V, R_L = 8Ω V_S = 6V, R_L = 4Ω	 1.5 0.6	 2.2 0.8		 W W
A_V	Voltage Gain	V_S = 12V, f = 1 kHz 10 μF from Pins 2 to 6	23	26 46	30	dB dB
BW	Bandwidth	V_S = 12V, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 12V, R_L = 8Ω, P_{OUT} = 500 mW, f = 1 kHz, Pins 2 and 6 Open		0.1	1	%
PSRR	Power Supply Rejection Ratio (Note 3)	V_S = 12V, f = 1 kHz, C_{BYPASS} = 10 μF, Pins 2 and 6 Open, Referred to Output		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	V_S = 12V, Pins 7 and 8 Open		250		nA

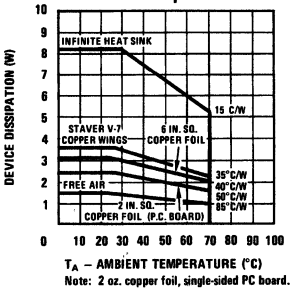
Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Derate at 15°C/W above 25°C case.

Note 2: The amplifier should be in high gain for full swing on higher supplies due to input voltage limitations.

Note 3: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

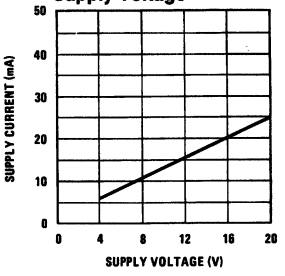
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

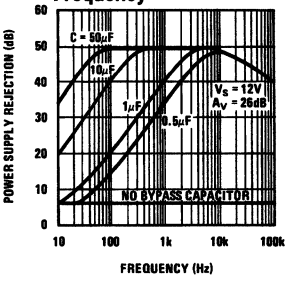


Note: 2 oz. copper foil, single-sided PC board.

Quiescent Supply Current vs Supply Voltage



Power Supply Rejection Ratio (Referred to the Output) vs Frequency



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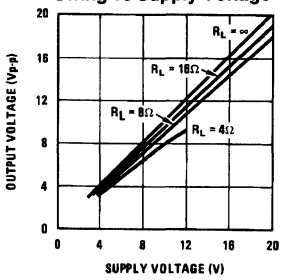
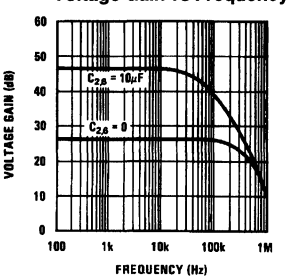
Typical Performance Characteristics (Continued)

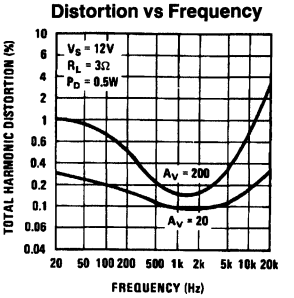
Peak-to-Peak Output Voltage Swing vs Supply Voltage



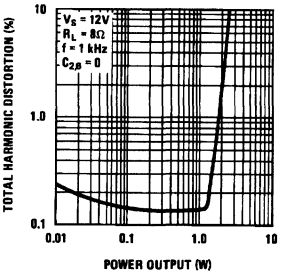
Voltage Gain vs Frequency



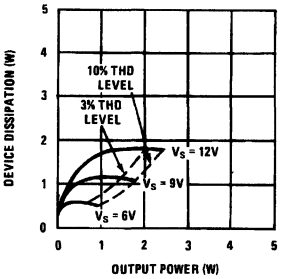
Distortion vs Frequency



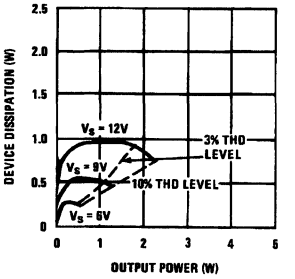
Distortion vs Output Power



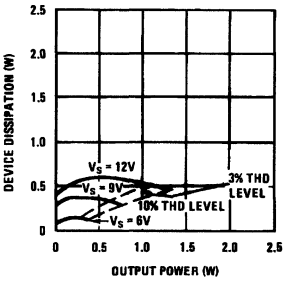
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



Device Dissipation vs Output Power—16Ω Load



TL/H/7846–6

Application Hints

GAIN CONTROL

To make the LM388 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pins 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pins 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2

Application Hints (Continued)

is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor . The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM388 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM388 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

BOOTSTRAPPING

The base of the output transistor of the LM388 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are $V_{BE} = 0.7V$ and $\beta_O = 100$.

Example: 1 watt into 8Ω load with $V_S = 12V$.

$$I_{O\,MAX} = \sqrt{\frac{2P_O}{R_L}} = 500\ mA$$

$$(R1 + R2) = 100\left(\frac{(12/2) - 0.7}{0.5}\right) = 1060\Omega$$

To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \cong \frac{4C_c}{\beta_O} \cong \frac{C_c}{25}$$

Example: for 100 Hz pole and $R_L = 8\Omega$; $C_c = 200\ \mu F$ and $C_B = 8\ \mu F$, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications

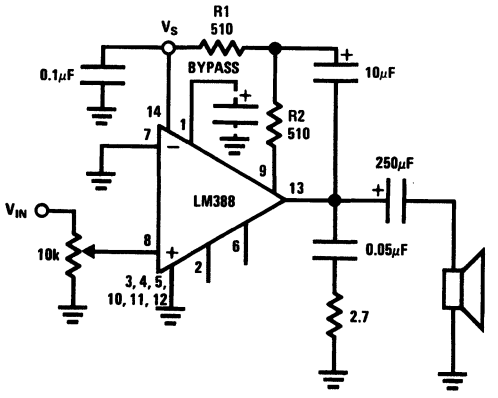


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FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)

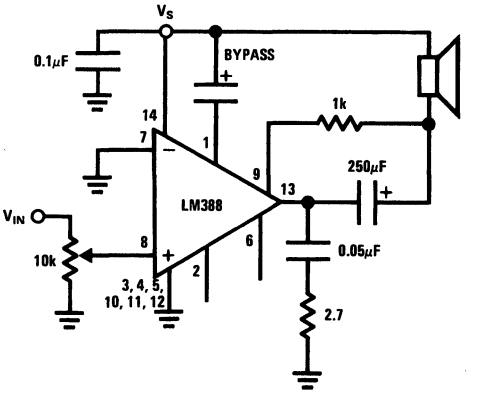

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FIGURE 2. Load Returned to V_S (Amplifier with Gain = 20)

Typical Applications (Continued)

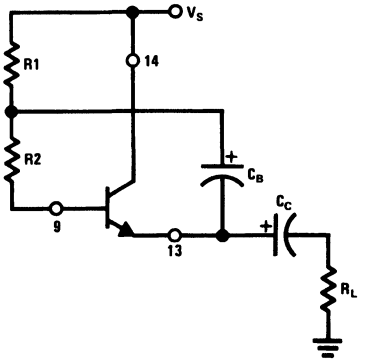

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FIGURE 3

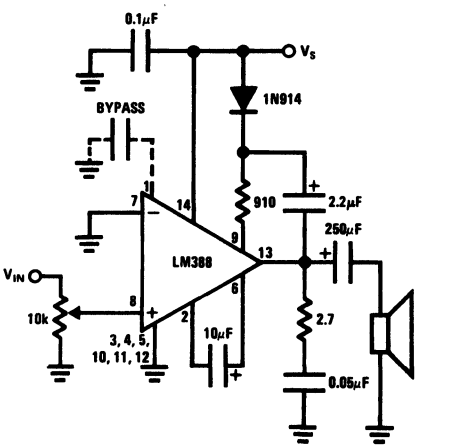

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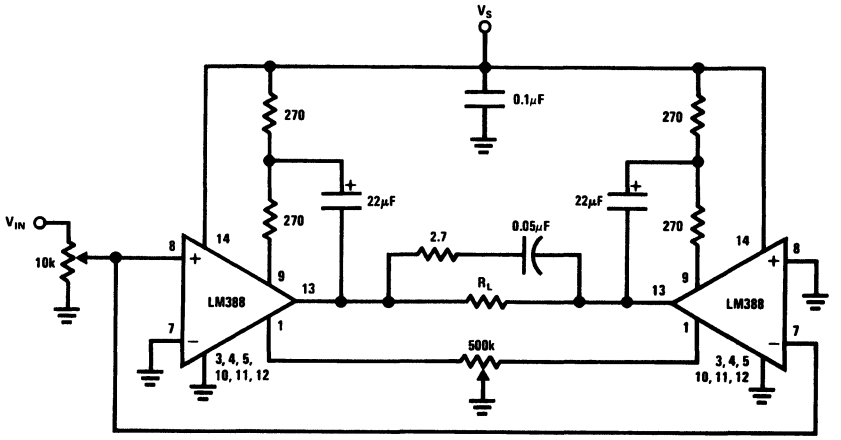
FIGURE 4. Amplifier with Gain = 200 and Minimum C_B



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V_S = 6V R_L = 4Ω P_O = 1.0W
V_S = 12V R_L = 8Ω P_O = 4W

FIGURE 5. Bridge Amp

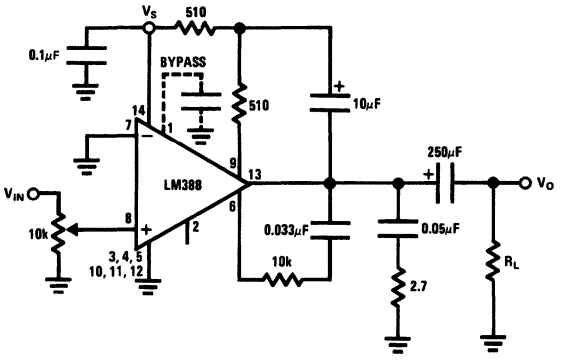

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FIGURE 6a. Amplifier with Bass Boost

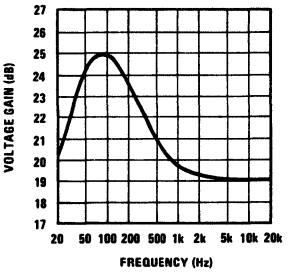

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FIGURE 6b. Frequency Response with Bass Boost

Typical Applications (Continued)

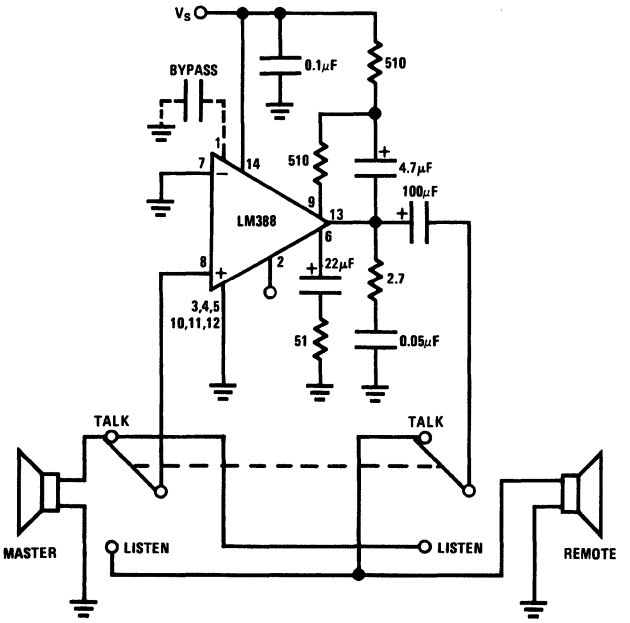

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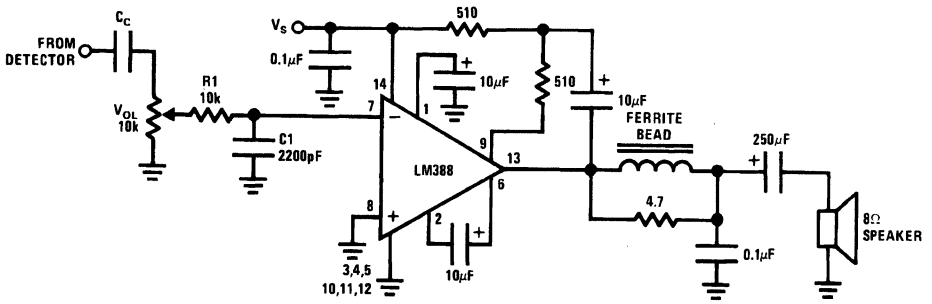
FIGURE 7. Intercom



TL/H/7846–13

FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor

LM389 Low Voltage Audio Power Amplifier with NPN Transistor Array

General Description

The LM389 is an array of three NPN transistors on the same substrate with an audio power amplifier similar to the LM386.

The amplifier inputs are ground referenced while the output is automatically biased to one half the supply voltage. The gain is internally set at 20 to minimize external parts, but the addition of an external resistor and capacitor between pins 4 and 12 will increase the gain to any value up to 200.

The three transistors have high gain and excellent matching characteristics. They are well suited to a wide variety of applications in DC through VHF systems.

Features

Amplifier

- Battery operation
- Minimum external parts
- Wide supply voltage range
- Low quiescent current drain
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion

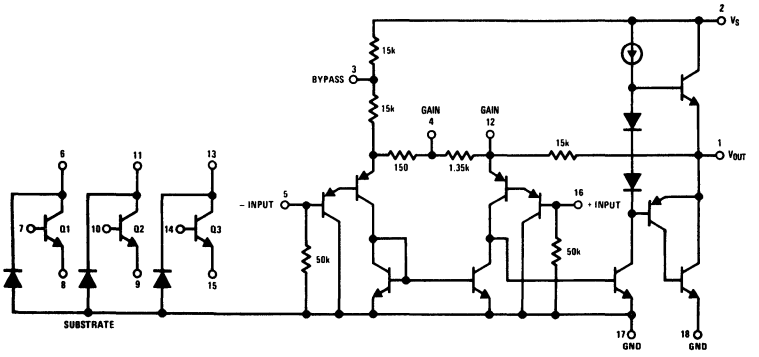
Transistors

- Operation from 1 μA to 25 mA
- Frequency range from DC to 100 MHz
- Excellent matching

Applications

- AM-FM radios
- Portable tape recorders
- Intercoms
- Toys and games
- Walkie-talkies
- Portable phonographs
- Power converters

Equivalent Schematic and Connection Diagrams



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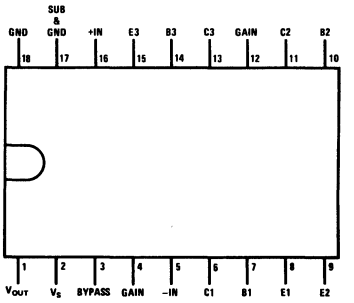
Dual-In-Line Package



TL/H/7847–2

Order Number LM389N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	15V
Package Dissipation (Note 1)	1.89W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Collector to Emitter Voltage, V_{CEO}	12V
Collector to Base Voltage, V_{CBO}	15V
Collector to Substrate Voltage, V_{CIO} (Note 2)	15V
Collector Current, I_C	25 mA
Emitter Current, I_E	25 mA
Base Current, I_B	5 mA
Power Dissipation (Each Transistor) $T_A \leq +70°C$	150 mW

Electrical Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLIFIER						
V_S	Operating Supply Voltage		4		12	V
I_Q	Quiescent Current	$V_S = 6V$, $V_{IN} = 0V$		6	12	mA
P_{OUT}	Output Power (Note 3)	THD = 10% $V_S = 6V$, $R_L = 8\Omega$ $V_S = 9V$, $R_L = 16\Omega$	250	325 500		mW mW
A_V	Voltage Gain	$V_S = 6V$, f = 1 kHz 10 μF from Pins 4 to 12	23	26 46	30	dB dB
BW	Bandwidth	$V_S = 6V$, Pins 4 and 12 Open		250		kHz
THD	Total Harmonic Distortion	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125$ mW, f = 1 kHz, Pins 4 and 12 Open		0.2	3.0	%
PSRR	Power Supply Rejection Ratio	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10$ μF, Pins 4 and 12 Open, Referred to Output	30	50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	$V_S = 6V$, Pins 5 and 16 Open		250		nA
TRANSISTORS						
V_{CEO}	Collector to Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	12	20		V
V_{CBO}	Collector to Base Breakdown Voltage	$I_C = 10$ μA, $I_E = 0$	15	40		V
V_{CIO}	Collector to Substrate Breakdown Voltage	$I_C = 10$ μA, $I_E = I_B = 0$	15	40		V
V_{EBO}	Emitter to Base Breakdown Voltage	$I_E = 10$ μA, $I_C = 0$	6.4	7.1	7.8	V
H_{FE}	Static Forward Current Transfer Ratio (Static Beta)	$I_C = 10$ μA $I_C = 1$ mA $I_C = 10$ mA	100	100 275 275		
h_{oe}	Open-Circuit Output Admittance	$I_C = 1$ mA, $V_{CE} = 5V$, f = 1.0 kHz		20		μmho
V_{BE}	Base to Emitter Voltage	$I_E = 1$ mA		0.7	0.85	V
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Offset	$I_E = 1$ mA		1	5	mV
V_{CESAT}	Collector to Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		0.15	0.5	V
C_{EB}	Emitter to Base Capacitance	$V_{EB} = 3V$		1.5		pF
C_{CB}	Collector to Base Capacitance	$V_{CB} = 3V$		2		pF
C_{CI}	Collector to Substrate Capacitance	$V_{CI} = 3V$		3.5		pF
h_{fe}	High Frequency Current Gain	$I_C = 10$ mA, $V_{CE} = 5V$, f = 100 MHz	1.5	5.5		

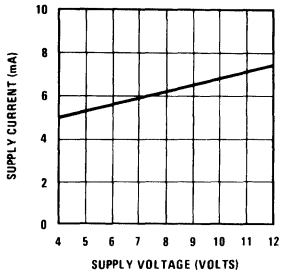
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 66°C/W junction to ambient.

Note 2: The collector of each transistor is isolated from the substrate by an integral diode. Therefore, the collector voltage should remain positive with respect to pin 17 at all times.

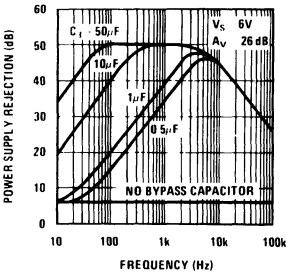
Note 3: If oscillation exists under some load conditions, add 2.7Ω and 0.05 μF series network from pin 1 to ground.

Typical Amplifier Performance Characteristics

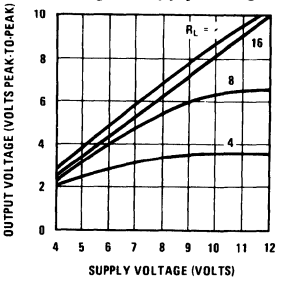
Quiescent Supply Current vs Supply Voltage



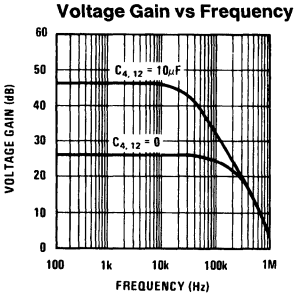
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



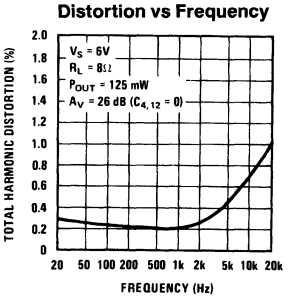
Peak-to-Peak Output Voltage Swing vs Supply Voltage



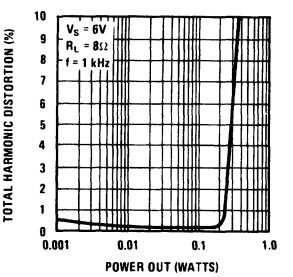
Voltage Gain vs Frequency



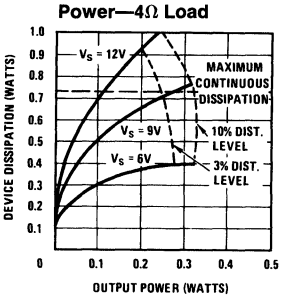
Distortion vs Frequency



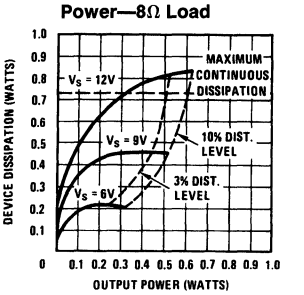
Distortion vs Output Power



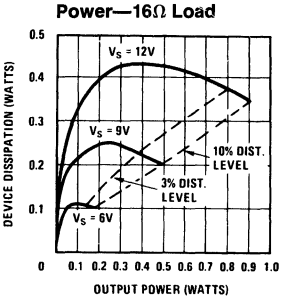
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



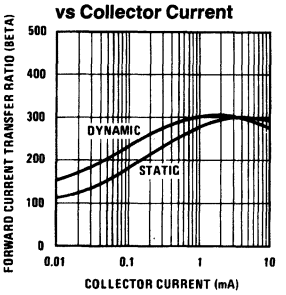
Device Dissipation vs Output Power—16Ω Load



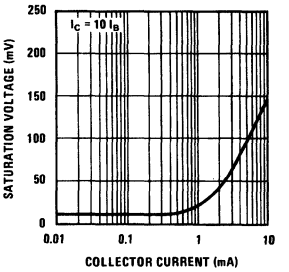
TL/H/7847–3

Typical Transistor Performance Characteristics

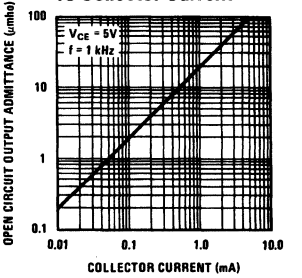
Forward Current Transfer Ratio vs Collector Current



Saturation Voltage vs Collector Current



Open Circuit Output Admittance vs Collector Current



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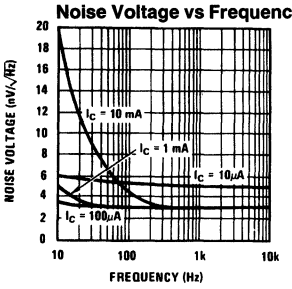
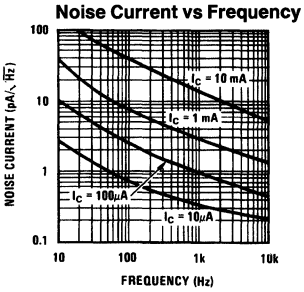
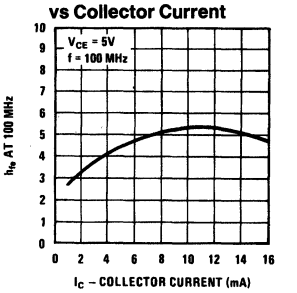
Noise Voltage vs Frequency



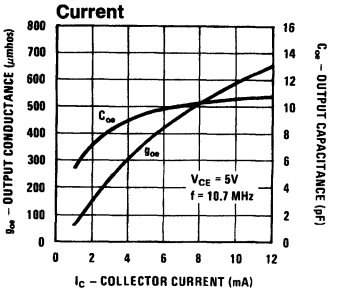
Noise Current vs Frequency



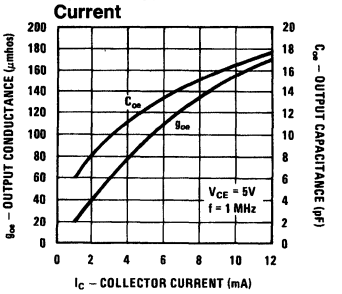
High Frequency Current Gain vs Collector Current



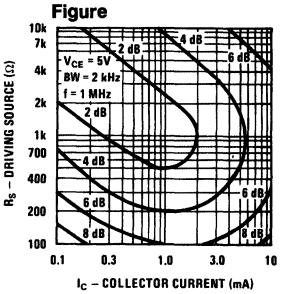
g_{oe} and C_{oe} vs Collector Current



g_{oe} and C_{oe} vs Collector Current



Contours of Constant Noise Figure



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Application Hints

Gain Control

To make the LM389 a more versatile amplifier, two pins (4 and 12) are provided for gain control. With pins 4 and 12 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 4 to 12, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 4 to 12, then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 12 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 12 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: $R \cong 15\ k\Omega$, the lowest value for good stable operation is $R = 10\ k\Omega$ if pin 4 is open. If pins 4 and 12 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM389 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM389 with higher gains (bypassing the 1.35 kΩ resistor between pins 4 and 12) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance of the driven input.

Supplies and Grounds

The LM389 has excellent supply rejection and does not require a well regulated supply. However, to eliminate possible high frequency stability problems, the supply should be decoupled to ground with a 0.1 μF capacitor. The high current ground of the output transistor, pin 18, is brought out separately from small signal ground, pin 17. If the two ground leads are returned separately to supply then the parasitic resistance in the power ground lead will not cause stability problems. The parasitic resistance in the signal ground can cause stability problems and it should be minimized. Care should also be taken to insure that the power dissipation does not exceed the maximum dissipation of the package for a given temperature. There are two ways to mute the LM389 amplifier. Shorting pin 3 to the supply voltage, or shorting pin 12 to ground will turn the amplifier off without affecting the input signal.

Transistors

The three transistors on the LM389 are general purpose devices that can be used the same as other small signal transistors. As long as the currents and voltages are kept within the absolute maximum limitations, and the collectors are never at a negative potential with respect to pin 17, there is no limit on the way they can be used.

For example, the emitter-base breakdown voltage of 7.1V can be used as a zener diode at currents from 1 μA to 5 mA. These transistors make good LED driver devices, V_{SAT} is only 150 mV when sinking 10 mA.

In the linear region, these transistors have been used in AM and FM radios, tape recorders, phonographs and many other applications. Using the characteristic curves on noise voltage and noise current, the level of the collector current can be set to optimize noise performance for a given source impedance. Some of the circuits that have been built are shown in *Figures 1–7*. This is by no means a complete list of applications, since that is limited only by the designers imagination.

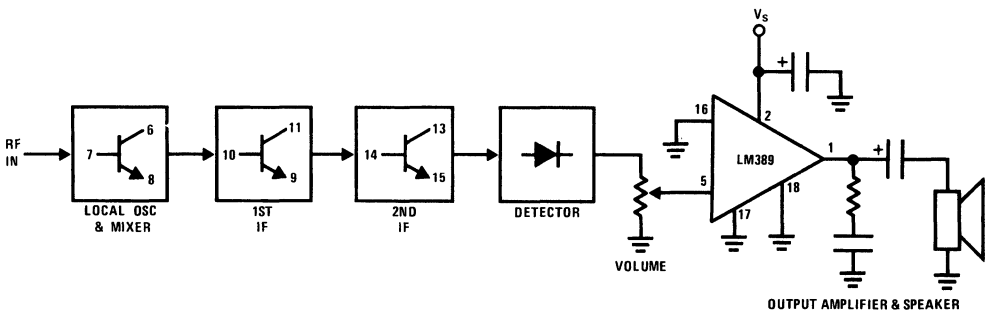

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FIGURE 1. AM Radio

Application Hints (Continued)

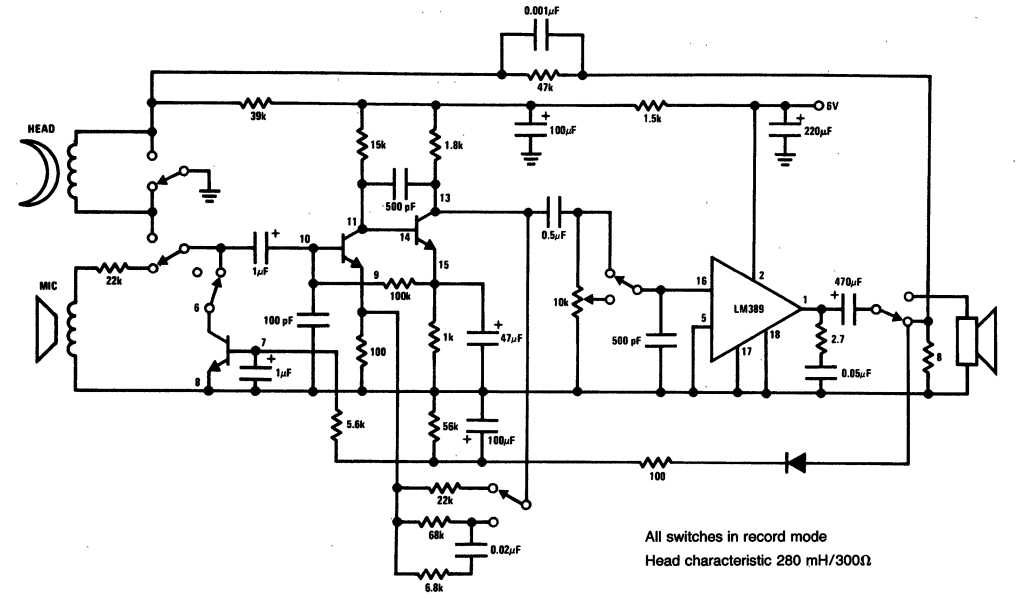

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FIGURE 2. Tape Recorder

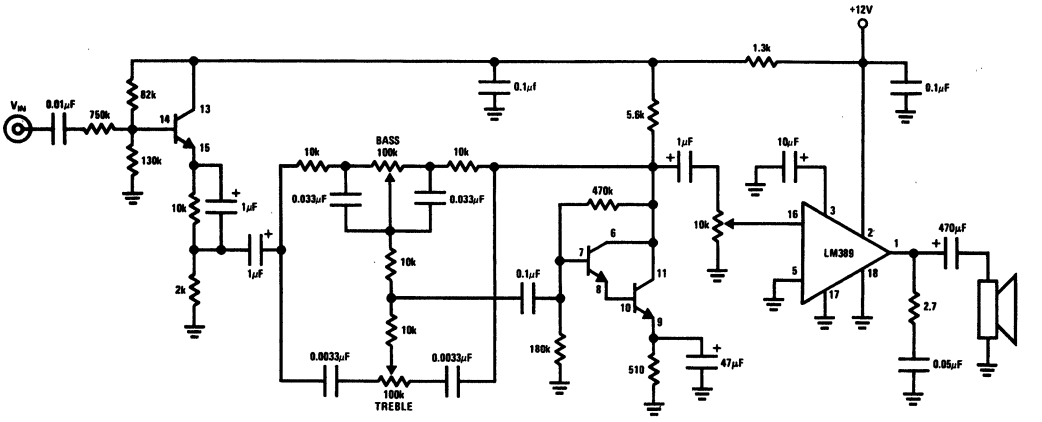

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FIGURE 3. Ceramic Phono Amplifier with Tone Controls

Application Hints (Continued)

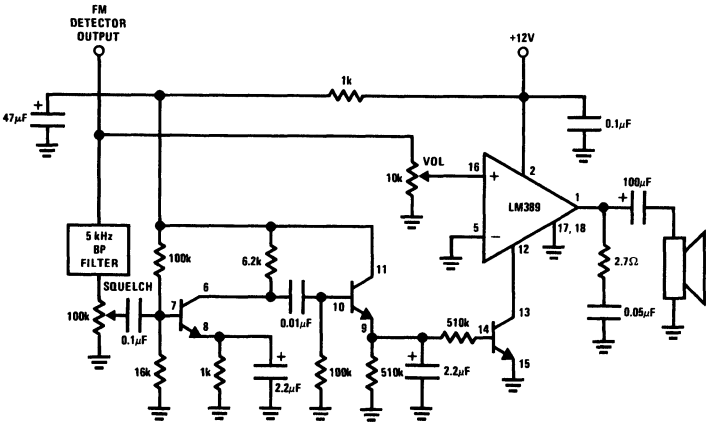

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FIGURE 4. FM Scanner Noise Squelch Circuit

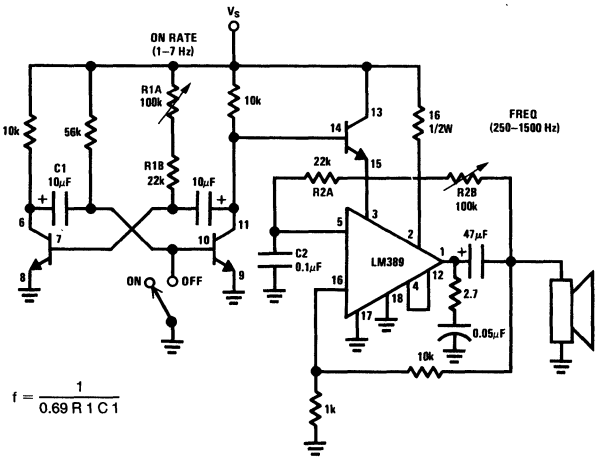

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FIGURE 5. Siren

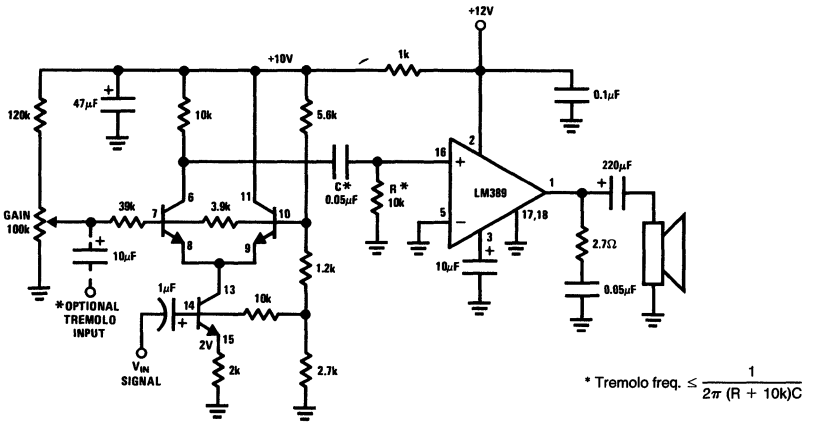

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FIGURE 6. Voltage-Controlled Amplifier or Tremolo Circuit

Application Hints (Continued)

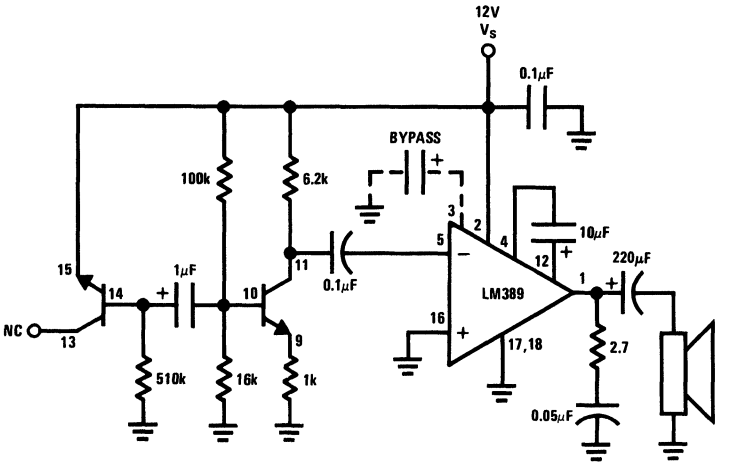

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FIGURE 7. Noise Generator Using Zener Diode

National Semiconductor

LM390 1 Watt Battery Operated Audio Power Amplifier

General Description

The LM390 Power Audio Amplifier is optimized for 6V, 7.5V, 9V operation into low impedance loads. The gain is internally set at 20 to keep the external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 wil increase the gain to any value up to 200. The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

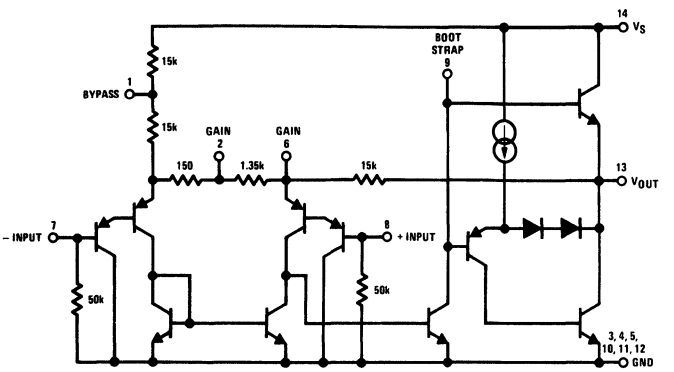
Features

- Battery operation
- 1W output power
- Minimum external parts
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package

Applications

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



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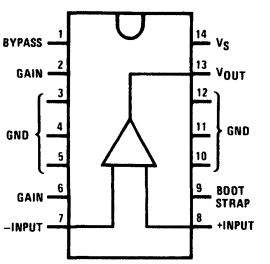
Dual-In-Line Package



TL/H/7848–2

Order Number LM390N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics T_A = 25°C, *(Figure 1)*

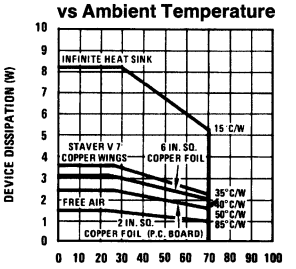
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_S	Operating Supply Voltage		4		9	V
I_Q	Quiescent Current	V_S = 6V, V_{IN} = 0		10	20	mA
P_{OUT}	Output Power	V_S = 6V, R_L = 4Ω, THD = 10%	0.8	1.0		W
A_V	Voltage Gain	V_S = 6V, f 1 kHz 10 μF from Pin 2 to 6	23	26 46	30	dB dB
BW	Bandwidth	V_S = 6V, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 6V, R_L = 4Ω, P_{OUT} = 500 mW f = 1 kHz, Pins 2 and 6 Open		0.2	1	%
PSRR	Power Supply Rejection Ratio	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 μF, Pins 2 and 6 Open, Referred to Output (Note 2)		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	V_S = 6V, Pins 7 and 8 Open		250		nA

Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Above 25°C case, derate at 15°C/W junction to case, or 85°C/W junction to ambient.

Note 2: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

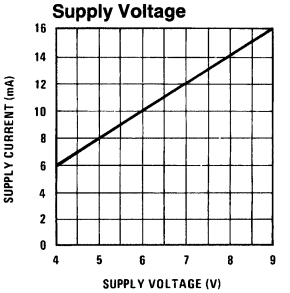
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

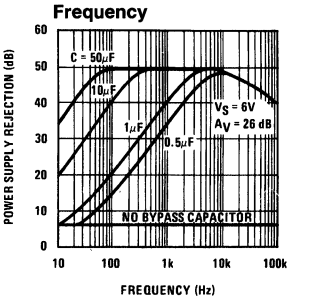


Note: 2 oz. copper foil, single-sided PC board.

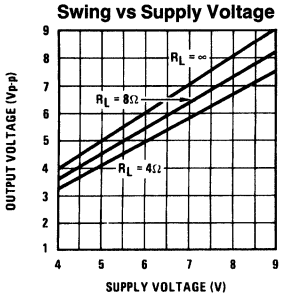
Quiescent Supply Current vs Supply Voltage



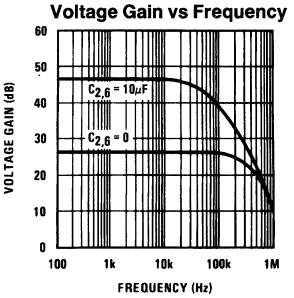
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



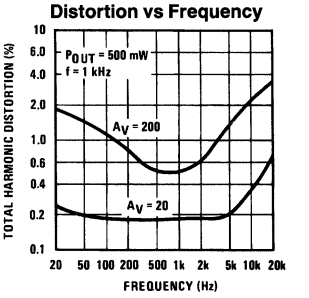
Peak-to-Peak Output Voltage Swing vs Supply Voltage



Voltage Gain vs Frequency



Distortion vs Frequency



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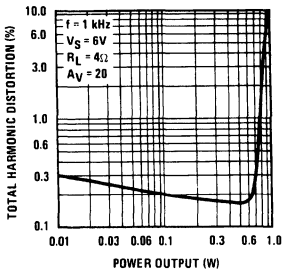
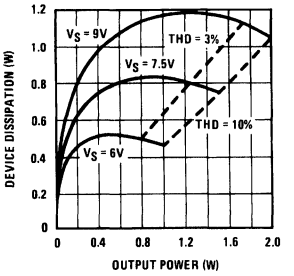
Typical Performance Characteristics (Continued)

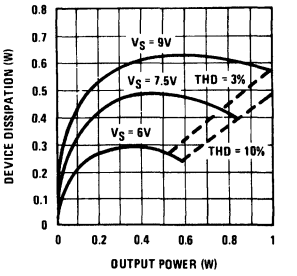
Distortion vs Output Power



Device Dissipation vs Output Power 4Ω Load



Device Dissipation vs Output Power 8Ω Load



TL/H/7848–6

Application Hints

Gain Control

To make the LM390 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2 is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM390 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM390 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Bootstrapping

The base of the output transistor of the LM390 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are $V_{BE} = 0.7V$ and $\beta_O = 100$.

Example 0.8 watt into 4Ω load with $V_S = 6V$.

$$I_{O\,MAX} = \sqrt{\frac{2\,P_O}{R_L}} = 632\ mA$$

$$(R1 + R2) = 100\left(\frac{(6/2) - 0.7}{0.632}\right) = 364\Omega$$

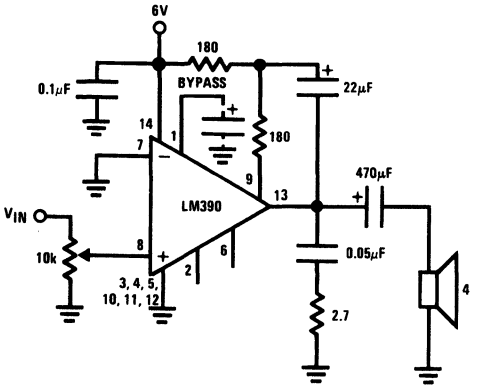
To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \cong \frac{4C_c}{\beta_O} \cong \frac{C_c}{25}$$

Example: for 100 Hz pole and $R_L = 4\Omega$; $C_c = 400\ \mu F$ and $C_B = 16\ \mu F$, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

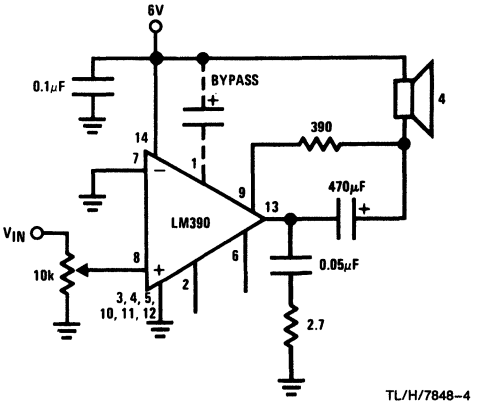
For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications



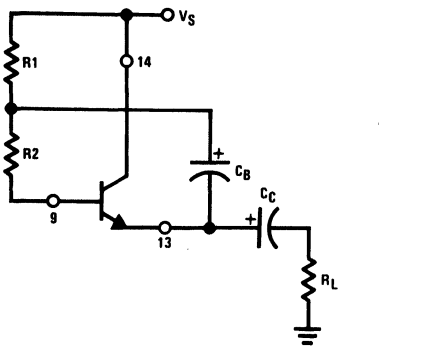
TL/H/7848–3

FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)



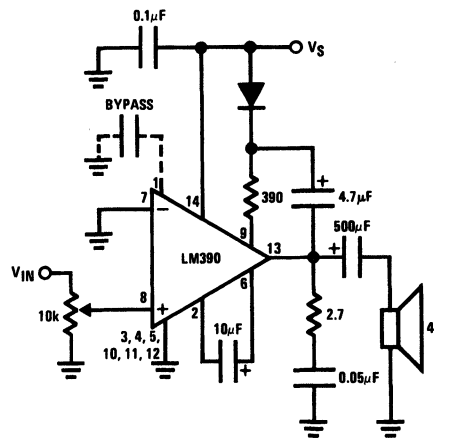
TL/H/7848–4

FIGURE 2. Load Returned to Supply (Amplifier with Gain = 20)



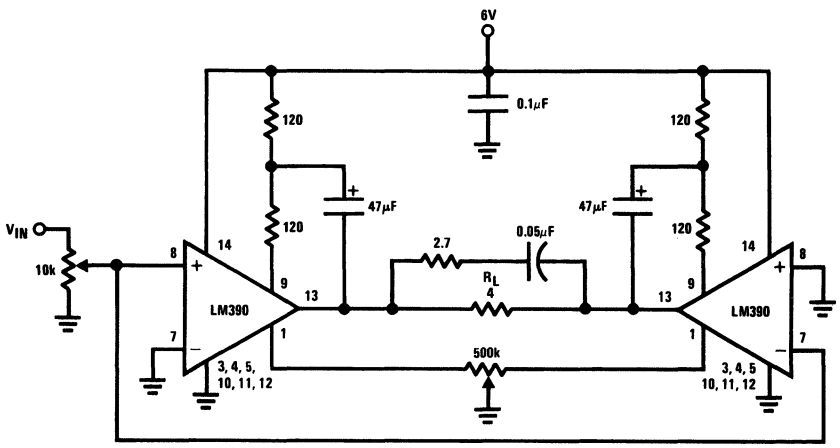
TL/H/7848–7

FIGURE 3



TL/H/7848–8

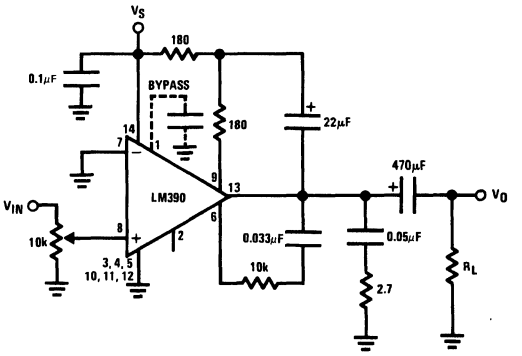
FIGURE 4. Amplifier with Gain = 200 and Minimum C_B



TL/H/7848–9

FIGURE 5. 2.5W Bridge Amplifier

Typical Applications (Continued)



TL/H/7848–10

FIGURE 6(a). Amplifier with Bass Boost

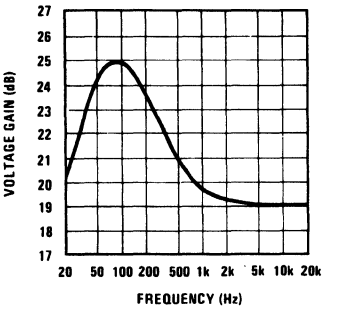


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FIGURE 6(b). Frequency Response with Bass Boost

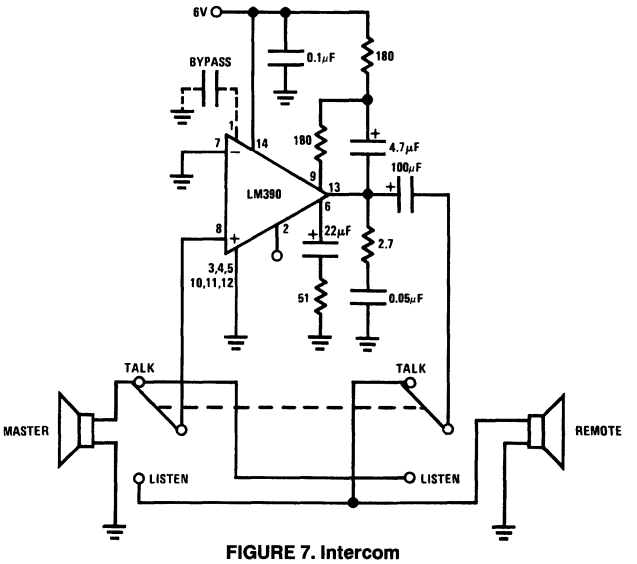

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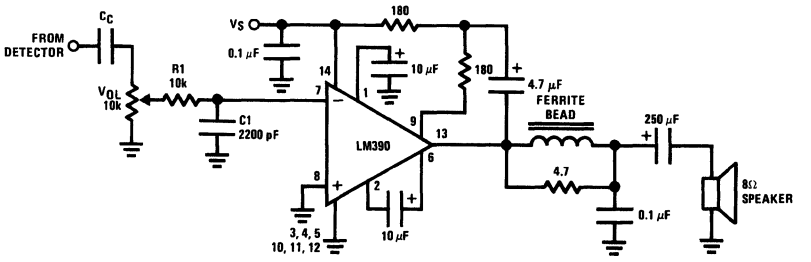
FIGURE 7. Intercom



TL/H/7848–13

FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor

LM391 Audio Power Driver

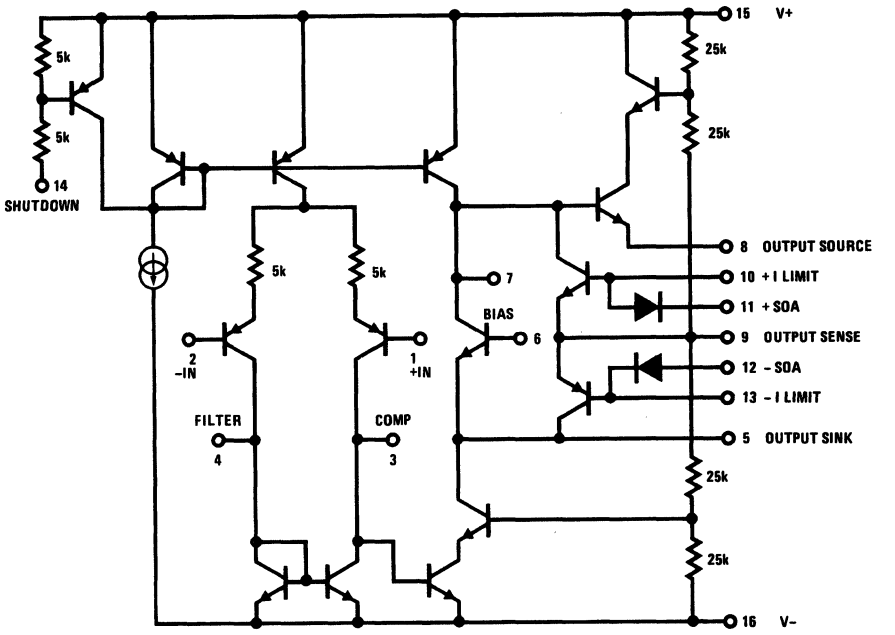
General Description

The LM391 audio power driver is designed to drive external power transistors in 10 to 100 watt power amplifier designs. High power supply voltage operation and true high fidelity performance distinguish this IC. The LM391 is internally protected for output faults and thermal overloads; circuitry providing output transistor protection is user programmable.

Features

■ High Supply Voltage	±50V max
■ Low Distortion	0.01%
■ Low Input Noise	3 μV
■ High Supply Rejection	90 dB
■ Gain and Bandwidth Selectable	
■ Dual Slope SOA Protection	
■ Shutdown Pin	

Equivalent Schematic and Connection Diagram



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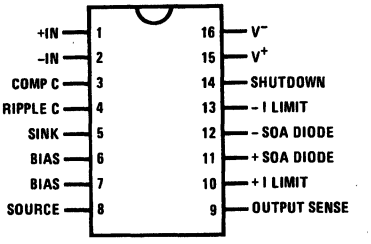
Dual-In-Line Package



TL/H/7146–2

Top View

Order Number LM391N-100
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
LM391N-100	±50V or +100V
Input Voltage	Supply Voltage less 5V
Shutdown Current (Pin 14)	1 mA
Package Dissipation (Note 1)	1.39W
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temp. (Soldering, 10 sec.)	260°C

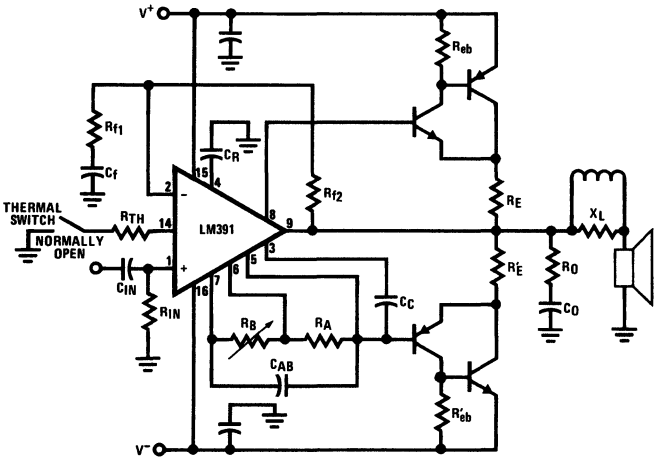
Electrical Characteristics T_A = 25°C (The following are for V^+ = 90% V^+_{MAX} and V^- = 90% V^-_{MAX}.)

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current LM391N-100	Current in Pin 15 V_{IN} = 0		 5	 6	mA
Output Swing	Positive Negative	$V^+ - 7$ $V^- + 7$	$V^+ - 5$ $V^- + 5$		V V
Drive Current	Source (Pin 8) Sink (Pin 5)	5 5			mA mA
Noise (20 Hz–20 kHz)	Input Referred		3		μV
Supply Rejection	Input Referred	70	90		dB
Total Harmonic Distortion	f = 1 kHz f = 20 kHz		0.01 0.10	 0.25	% %
Intermodulation Distortion	60 Hz, 7 kHz, 4:1		0.01		%
Open Loop Gain	f = 1 kHz	1000	5500		V/V
Input Bias Current			0.1	1.0	μA
Input Offset Voltage			5	20	mV
Positive Current Limit V_{BE}	Pin 10–9		650		mV
Negative Current Limit V_{BE}	Pin 9–13		650		mV
Positive Current Limit Bias Current	Pin 10		10	100	μA
Negative Current Limit Bias Current	Pin 13		10	100	μA

Pin 14 Current Comments
Minimum pin 14 current required for shutdown is 0.5 mA, and must not exceed 1 mA.
Maximum pin 14 current for amplifier not shut down is 0.05 mA.
The typical shutdown switch point current is 0.2 mA.

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Typical Applications

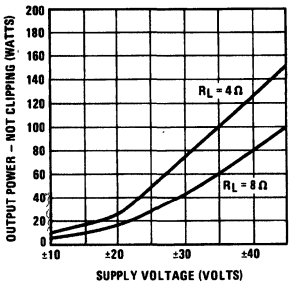


TL/H/7146–3

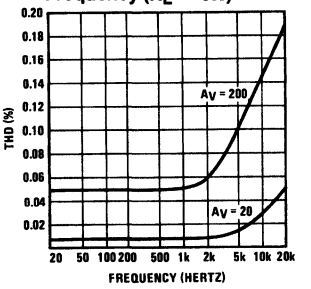
FIGURE 1. LM391 with External Components—Protection Circuitry Not Shown

Typical Performance Characteristics

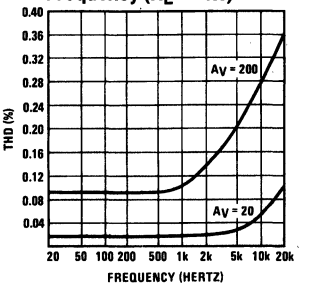
Output Power vs Supply Voltage



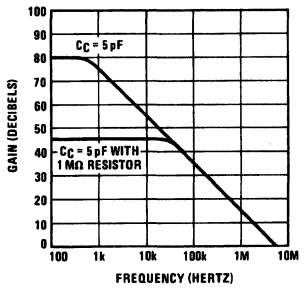
Total Harmonic Distortion vs Frequency ($R_L = 8\Omega$)



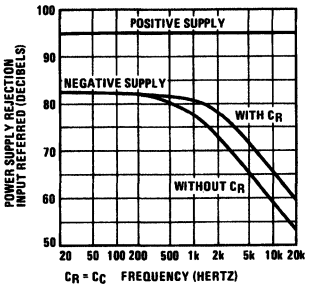
Total Harmonic Distortion vs Frequency ($R_L = 4\Omega$)



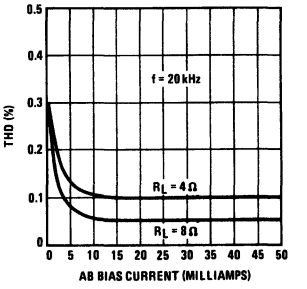
Open Loop Gain vs Frequency



Input Referred Power Supply Rejection vs Frequency



Total Harmonic Distortion vs AB Bias Current



TL/H/7146–4

Pin Descriptions

Pin No.	Pin Name	Comments
1	+ Input	Audio input
2	− Input	Feedback input
3	Compensation	Sets the dominant pole
4	Ripple Filter	Improves negative supply rejection
5	Sink Output	Drives output devices and is emitter of AB bias V_{BE} multiplier
6	BIAS	Base of V_{BE} multiplier
7	BIAS	Collector of V_{BE} multiplier
8	Source Output	Drives output devices
9	Output Sense	Biases the IC and is used in protection circuits
10	+ Current Limit	Base of positive side protection circuit transistor
11	+ SOA Diode	Diode used for dual slope SOA protection
12	− SOA Diode	Diode used for dual slope SOA protection
13	− Current Limit	Base of negative side protection circuit transistor
14	Shutdown	Shuts off amplifier when current is pulled out of pin
15	V+	Positive supply
16	V−	Negative supply

External Components (Figure 1)

Component	Typical Value	Comments
C_{IN}	1 μF	Input coupling capacitor sets a low frequency pole with R_{IN}. $f_L = \frac{1}{2\pi R_{IN} C_{IN}}$
R_{IN}	100k	Sets input impedance and DC bias to input.
R_{f_2}	100k	Feedback resistor; for minimum offset voltage at the output this should be equal to R_{IN}.
R_{f_1}	5.1k	Feedback resistor that works with R_{f_2} to set the voltage gain. $A_V = 1 + \frac{R_{f_2}}{R_{f_1}}$
C_f	10 μF	Feedback capacitor. This reduces the gain to unity at DC for minimum offset voltage at the output. Also sets a low frequency pole with R_{f_1}. $f_L = \frac{1}{2\pi R_{f_1} C_f}$
C_C	5 pF	Compensation capacitor. Sets gain bandwidth product and a high frequency pole. $GBW = \frac{1}{2\pi 5000 C_C}$, $f_h = \frac{GBW}{A_V}$ Max f_h for stable design ≈ 500 kHz.
R_A	3.9k	AB bias resistor.
R_B	10k	AB bias potentiometer. Adjust to set bias current in the output stage.
C_{AB}	0.1 μF	Bypass capacitor for bias. This improves high frequency distortion and transient response.
C_R	5 pF	Ripple capacitor. This improves negative supply rejection at midband and high frequencies. C_R, if used, must equal C_C.
R_{eb}	100Ω	Bleed resistor. This removes stored charge in output transistors.
R_O	2.7Ω	Output compensation resistor. This resistor and C_O compensate the output stage. This value will vary slightly for different output devices.
C_O	0.1 μF	Output compensation capacitor. This works with R_O to form a zero that cancels f_β of the output power transistors.
R_E	0.3Ω	Emitter degeneration resistor. This resistor gives thermal stability to the output stage quiescent current. IRC PW5 type.
R_{TH}	39k	Shutdown resistor. Sets the amount of current pulled out of pin 14 during shutdown.
C_2, C'_2	1000 pF	Compensation capacitors for protection circuitry.
X_L	10Ω‖5 μH	Used to isolate capacitive loads, usually 20 turns of wire wrapped around a 10Ω, 2W resistor.

Application Hints

GENERALIZED AUDIO POWER AMP DESIGN

Givens: Power Output
Load Impedance
Input Sensitivity
Input Impedance
Bandwidth

The power output and load impedance determine the power supply requirements. Output signal swing and current are found from:

$$V_{Opeak} = \sqrt{2\,R_L\,P_O} \quad (1)$$

$$I_{Opeak} = \sqrt{\frac{2\,P_O}{R_L}} \quad (2)$$

Add 5 volts to the peak output swing (V_{OP}) for transistor voltage to get the supplies, i.e., $\pm$ (V_{OP} + 5V) at a current of I_{peak}. The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions.

$$\text{max supplies} \approx \pm(V_{Opeak} + 5)\,(1 + \text{regulation})\,(1.1) \quad (3)$$

The input sensitivity and output power specs determine the required gain.

$$A_V \geq \frac{\sqrt{P_O\,R_L}}{V_{IN}} = \frac{V_{ORMS}}{V_{INRMS}} \quad (4)$$

Normally the gain is set between 20 and 200; for a 25 watt, 8 ohm amplifier this results in a sensitivity of 710 mV and 71 mV, respectively. The higher the gain, the higher the THD, as can be seen from the characteristics curves. Higher gain also results in more hum and noise at the output.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The bandwidth requirements determine the size of C_f and C_C as indicated in the external component listing.

The output transistors and drivers must have a breakdown voltage greater than the voltage determined by equation (3). The current gain of the drive and output device must be high enough to supply I_{Opeak} with 5 mA of drive from the LM391. The power transistors must be able to dissipate approximately 40% of the maximum output power; the drivers must dissipate this amount divided by the current gain of the outputs. See the output transistor selection guide, Table A.

To prevent thermal runaway of the AB bias current the following equation must be valid:

$$\theta_{JA} \leq \frac{R_E\,(\beta_{MIN} + 1)}{V_{CEQMAX}\,(K)} \quad (5)$$

where:

θ_{JA} is the thermal resistance of the driver transistor, junction to ambient, in °C/W.

R_E is the emitter degeneration resistance in ohms.

β_{min} is that of the output transistor.

V_{CEQMAX} is the highest possible value of one supply from equation (3).

K is the temperature coefficient of the driver base-emitter voltage, typically 2 mV/°C.

Often the value of R_E is to be determined and equation (5) is rearranged to be:

$$R_E \geq \frac{\theta_{JA}\,(V_{CEQMAX})\,K}{\beta_{MIN} + 1} \quad (6)$$

The maximum average power dissipation in each output transistor is:

$$\overline{P_{DMAX}} = 0.4\,P_{OMAX} \quad (7)$$

The power dissipation in the driver transistor is:

$$\overline{P_{DRIVER(MAX)}} = \frac{\overline{P_{DMAX}}}{\beta_{MIN}} \quad (8)$$

Heat sink requirements are found using the following formulas:

$$\theta_{JA} \leq \frac{T_{JMAX} - T_{AMAX}}{P_D} \quad (9)$$

$$\theta_{SA} \leq \theta_{JA} - \theta_{JC} - \theta_{CS} \quad (10)$$

where:

T_{jMAX} is the maximum transistor junction temperature.

T_{AMAX} is the maximum ambient temperature.

θ_{JA} is thermal resistance junction to ambient.

θ_{SA} is thermal resistance sink to ambient.

θ_{JC} is thermal resistance junction to case.

θ_{CS} is thermal resistance case to sink, typically 1°C/W for most mountings.

Application Hints (Continued)

PROTECTION CIRCUITRY

The protection circuits of the LM391 are very flexible and should be tailored to the output transistor's safe operating area. The protection V-I characteristics, circuitry, and resistor formulas are described below. The diodes from the output to each supply prevent the output voltage from exceeding the supplies and harming the output transistors. The output will do this if the protection circuitry is activated while driving an inductive load.

TURN-ON DELAY

It is often desirable to delay the turn-ON of the power amplifier. This is easily implemented by putting a resistor in series with a capacitor from pin 14 to ground. The value of the resistor is set to limit the current to less than 1 mA (the absolute maximum). This resistor with the capacitor gives a time constant of RC. The turn-ON delay is approximately 2 time constants.

Example:

Amplifier with maximum supply of 30V, like the 20W, 8Ω example in the data sheet, requiring a delay of 1 second.

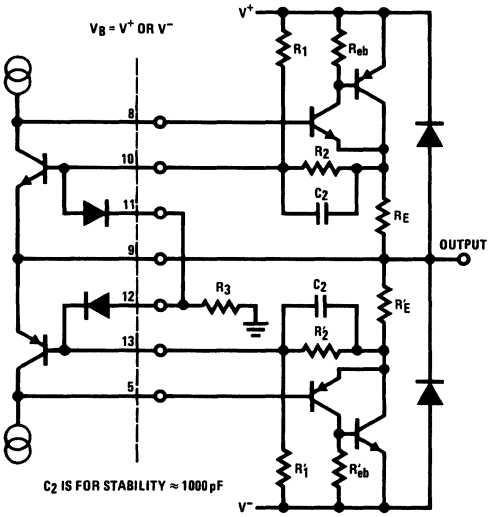
Time delay = 2 RC

$$R = \frac{\text{Max } V^+}{1\text{ mA}}$$

So:

R = 30k. Solving for C gives 16.7 μF. Use C = 20 μF with a 30V rating.

Protection Circuitry with External Components



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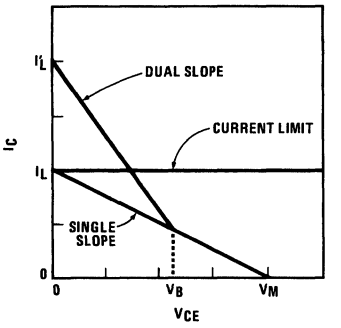
Protection Characteristics



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Protection Circuit Resistor Formulas ($V_B = V^+$)

Type of Protection	R_E, R'	R_1, R'_1	R_2, R'_2	R_3, R'_3
Current Limit	$R_E = \frac{\phi}{I_L}$	Not Required	Short	Not Required
Single Slope SOA Protection	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	Not Required
Dual Slope SOA Protection ($V_B = V^+$)	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	$R_3 = R_2\left[\frac{V^+}{I_L R_E - \phi} - 1\right]$

Note: ϕ is the current limit V_{BE} voltage, 650 mV. Assumptions: $V^+ >> \phi$, $V_M >> \phi$. V^+ is the load supply voltage. V_M is the maximum rated V_{CE} of the output transistors.

Application Hints (Continued)

TRANSIENT INTERMODULATION DISTORTION

There has been a lot of interest in recent years about transient intermodulation distortion. Matti Otala of University of Oulu, Oulu, Finland has published several papers on the subject. The results of these investigations show that the open loop pole of the power amplifier should be above 20 kHz.

To do this with the LM391 is easy. Put a 1 MΩ resistor from pin 3 to the output and the open loop gain is reduced to about 46 dB. Now the open loop pole is at 30 kHz. The current in this resistor causes an offset in the input stage that can be cancelled with a resistor from pin 4 to ground. The resistor from pin 4 to ground should be 910 kΩ rather than 1 MΩ to insure that the shutdown circuitry will operate correctly. The slight difference in resistors results in about 15 mV of offset. The 40W, 8Ω amplifier schematic shows the hookup of these two resistors.

BRIDGE AMPLIFIER

A switch can be added to convert a stereo amplifer to a single bridge amplifer. The diagram below shows where the switch and one resistor are added. When operating in the bridge mode the output load is connected between the two outputs, the input is V_{IN} #1, and V_{IN} #2 is disconnected.

OSCILLATIONS & GROUNDING

Most power amplifiers work the first time they are turned on. They also tend to oscillate and have excess THD. Most oscillation problems are due to inadequate supply bypassing and/or ground loops. A 10 μF, 50V electrolytic on each power supply will stop supply-related oscillations. However, if the signal ground is used for these bypass caps the THD is usually excessive. The signal ground must return to the power supply alone, as must the output load ground. All other grounds—bypass, output R-C, protection, etc., can tie together and then return to supply. This ground is called high frequency ground. On the 40W amplifier schematic all the grounds are labeled.

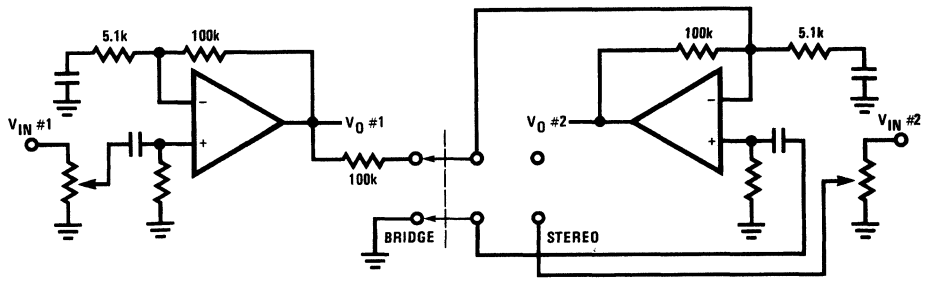
Capacitive loads can cause instabilities, so they are isolated from the amplifier with an inductor and resistor in the output lead.

AB BIAS CURRENT

To reduce distortion in the output stage, all the transistors are biased ON slightly. This results in class AB operation and reduces the crossover (notch) distortion of the class B stage to a low level, (see performance curve, THD vs AB bias). The potentiometer, R_B, from pins 6–7 is adjusted to give about 25 mA of current in the output stage. This current is usually monitored at the supply or by measuring the voltage across R_E.

Typical Applications (Continued)

Bridge Circuit Diagram



TL/H/7146–7

Output Transistors Selection Guide

Table A.

Power Output	Driver Transistor		Output Transistor	
	PNP	NPN	PNP	NPN
20W @ 8Ω 30W @ 4Ω	MJE711 MJE171 D43C8	MJE721 MJE181 D42C8	TIP42A 2N6490	TIP41A 2N6487
40W @ 8Ω 60W @ 4Ω	MJE712 MJE172 D43C11	MJE722 MJE182 D42C11	2N5882	2N5880

Application Hints (Continued)

A 20W, 8Ω; 30W, 4Ω AMPLIFIER

Givens:

Power Output	20W into 8Ω 30W into 4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

20W/8Ω V_{OP} = 17.9V I_{OP} = 2.24A

30W/4Ω V_{OP} = 15.5V I_{OP} = 3.87A

Therefore the supply required is:

±23V @ 2.24A, reducing to . . .

±21V @ 3.87A

With 15% regulation and high line we get ±29V from equation (3).

Sensitivity and equation (4) set minimum gain:

$$A_V \geq \frac{\sqrt{20 \times 8}}{1} = 12.65$$

We will use a gain of 20 with resulting sensitivity of 632 mV.

Letting R_{IN} equal 100k gives the required input impedance. For low DC offsets at the output we let R_{f_2} = 100k. Solving for R_{f_1} gives:

$$R_{f_2} = 100k$$

$$R_{f_1} = \frac{100k}{20 - 1} = 5.26k; \text{ use } 5.1k$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = \frac{20}{5} = 4 \text{ Hz}$$

$$f_h = 20k \times 5 = 100 \text{ kHz}$$

Solving for C_f:

$$C_f \geq \frac{1}{2\pi R_{f_1} f_L} = 7.8\ \mu\text{F; use } 10\ \mu\text{F}$$

The recommended value for C_C is 5 pF for gains of 20 or larger. This gives a gain-bandwidth product of 6.4 MHz and a resulting bandwidth of 320 kHz, better than required.

The breakdown voltage requirement is set by the maximum supply; we need a minimum of 58V and will use 60V. We must now select a 60V power transistor with reasonable beta at I_{Opeak}, 3.87A. The TIP42, TIP41 complementary pair are 60V, 60W transistors with a minimum beta of 30 at 4A. The driver transistor must supply the base drive given 5 mA drive from the LM391. The MJE711, MJE721 complementary driver transistors are 60V devices with a minimum beta of 40 at 200 mA. The driver transistors should be much faster (higher f_T) than the output transistors to insure that the R-C on the output will prevent instability.

To find the heat sink required for each output transistor we use equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(30) = 12\text{W} \quad (7)$$

$$\theta_{JA} \leq \frac{150°C - 55°C}{12} = 7.9°C/\text{W for } T_{AMAX} = 55°C \quad (9)$$

$$\theta_{SA} \leq 7.9 - 2.1 - 1.0 = 4.8°C/\text{W} \quad (10)$$

If both transistors are mounted on one heat sink the thermal resistance should be halved to 2.4°C/W.

The maximum average power dissipation in each driver is found using equation (8):

$$\overline{P_{DRIVER(MAX)}} = \frac{12}{30} = 400 \text{ mW}$$

Using equation (9):

$$\theta_{JA} \leq \frac{155 - 55}{0.4} = 237°C/\text{W}$$

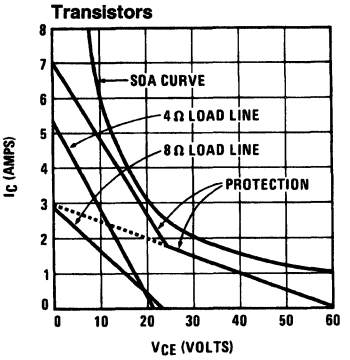
Application Hints (Continued)

Since the free air thermal resistance of the MJE711, MJE721 is 100°C/W, no heat sink is required. Using this information and equation (6) we can find the minimum value of R_E required to prevent thermal runaway.

$$R_E \geq \frac{100\,(30)\,(0.002)}{30+1} = 0.19\Omega \qquad (6)$$

We must now use the SOA data on the TIP42, TIP41 transistors to set up the protection circuit. Below is the SOA curve with the 4Ω and 8Ω load lines. Also shown are the desired protection lines. Note the value of V_B is equal to the supply voltage, so we use the formulas in the table.

D.C. SOA of TIP42, TIP41 Transistors



TL/H/7146–8

The data points from the curve are:

$$V_M = 60V,\ V_B = 23V,\ I_L = 3A,\ I_L' = 7A$$

Using the dual slope protection formulas:

$$R_E = \frac{0.65}{3} = 0.22\Omega$$

$$R_2 = 1k$$

$$R_1 = 1k\left(\frac{60-0.65}{0.65}\right) \approx 91k$$

$$R_3 = 1k\left(\frac{23}{7(0.22)-0.65} - 1\right) \approx 24k$$

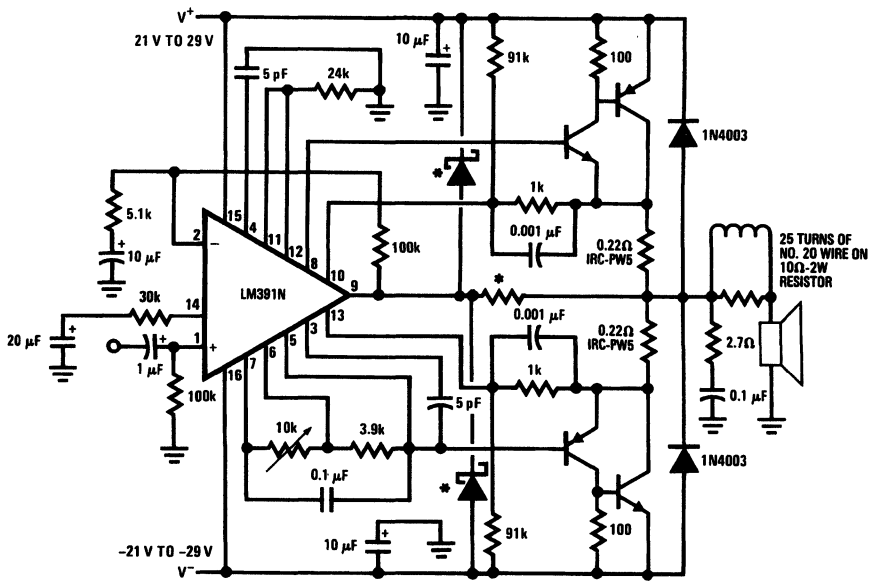
Note that an R_E of 0.22Ω satisfies equation (6). The final schematic of this amplifier is below. If the output is shorted the current will be 1.8A and V_{CE} is 23V. Since the input is AC, the average power is:

$$\text{short } \overline{P_D} = \tfrac{1}{2}(1.8)\,(23) \approx 21W$$

This power is greater than was used in the heat sink calculations, so the transistors will overheat for long-duration shorts unless a larger heat sink is used.

Typical Applications (Continued)

20W-8Ω, 30W-4Ω Amplifier with 1 Second Turn-ON Delay



TL/H/7146–9

*Additional protection for LM391N; Schottky diodes and R ≅ 100Ω.

Application Hints (Continued)

A 40W/8Ω, 60W/4Ω AMPLIFIER

Given:

Power Output	40W/8Ω 60W/4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

40W/8Ω $V_{OPeak} = 25.3V$ $I_{OPeak} = 3.16A$

60W/4Ω $V_{OPeak} = 21.9V$ $I_{OPeak} = 5.48A$

Therefore the supply required is:

±30.3V @ 3.16A, reducing to . . .

±26.9V @ 5.48A

With 15% regulation and high line we get ±38.3V using equation (3).

The minimum gain from equation (4) is:

$$A_V \geq 18$$

We select a gain of 20; resulting sensitivity is 900 mV.

The input impedance and bandwidth are the same as the 20 watt amplifier so the components are the same.

$R_{f_1} = 5.1k$ $R_{IN} = 100k$ $C_C = 5\ pF$

$R_{f_2} = 100k$ $C_f = 10\ \mu F$

The maximum supplies dictate using 80V devices. The 2N5882, 2N5880 pair are 80V, 160W transistors with a minimum beta of 40 at 2A and 20 at 6A. This corresponds to a minimum beta of 22.5 at 5.5A (I_{Opeak}). The MJE712, MJE722 driver pair are 80V transistors with a minimum beta of 50 at 250 mA. This output combination guarantees I_{Opeak} with 5 mA from the LM391.

Output transistor heat sink requirements are found using equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(60) = 24W \qquad (7)$$

$$\theta_{JA} \leq \frac{200 - 55}{24} = 6.0°C/W \text{ for } T_{AMAX} = 55°C \qquad (9)$$

$$\theta_{SA} \leq 6.0 - 1.1 - 1.0 = 3.9°C/W \qquad (10)$$

For both output transistors on one heat sink the thermal resistance should be 1.9°C/W.

Now using equation (8) we find the power dissipation in the driver:

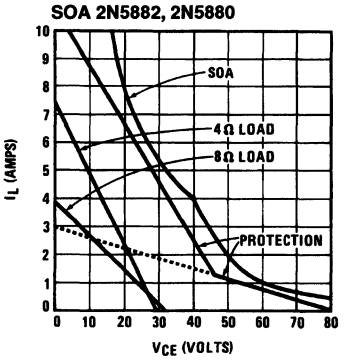
$$\overline{P_{DRIVER}} = \frac{24}{20} = 1.2W \qquad (8)$$

$$\theta_{JA} \leq \frac{150 - 55}{1.2} = 79°C/W \qquad (9)$$

Since a heat sink is required on the driver, we should investigate the output stage thermal stability at the same time to optimize the design. If we find a value of R_E that is good for the protection circuitry, we can then use equation (5) to find the heat sink required for the drivers.

The SOA characteristics of the 2N5882, 2N5880 transistors are shown in the following curve along with a desired protection line.

SOA 2N5882, 2N5880



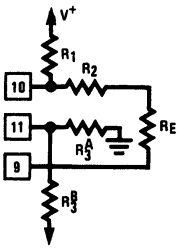
TL/H/7146–10

The desired data points are:

$V_M = 80V$ $V_B = 47V$ $I_L = 3A$ $I_L' = 11A$

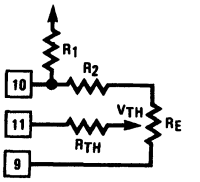
Since the break voltage is not equal to the supply, we will use two resistors to replace R_3 and move V_B.

Circuit Used



TL/H/7146–11

Thevenin Equivalent



Where: $R_{TH} = R_3^A \parallel R_3^B$

$$V_{TH} = V^- \left[\frac{R_3^A}{R_3^A + R_3^B}\right]$$

TL/H/7146–12

Application Hints (Continued)

The formulas for R_E, R_1, and R_2 do not change:

$$R_E = \frac{0.65}{3A} = 0.22\Omega$$

$$R_2 = 1k \qquad R_1 = 1k\frac{80 - 0.65}{0.65} = 120k$$

The formula for R_3 now gives R_{TH} when the V^+ in the formula becomes V_B.

$$R_{TH} = R_2\left[\frac{V_B}{I_L R_E - \phi} - 1\right]$$

$$= 1k\left[\frac{47}{11\,(0.22) - 0.65} - 1\right] = 25.55k$$

V_{TH} is the additional voltage added to the supply voltage to get V_B.

$$V_{TH} = -(V_B - V^+) = -(47 - 30) = -17V$$

Now we must find R_3^A and R_3^B using the Thevenin formulas. Putting V_{TH}, V^-, and R_{TH} into the appropriate formulas reduces to:

$$R_3^B = 0.76\,R_3^A \qquad \text{and} \qquad 25.55k = R_3^A \,||\, R_3^B$$

The easiest way to solve these equations is to iterate with standard values. If we guess $R_3^A = 62k$, then $R_3^B = 47.12k$; use 47k. The Thevenin impedance comes out 26.7k, which is close enough to 25.55k.

Now we will use equation (5) to determine the heat sinking requirements of the drivers to insure thermal stability:

$$\theta_{JA} \le \frac{0.22\,(20 + 1)}{40\,(0.002)} \approx 57°C/W \qquad (5)$$

This value is lower than we got with equation (9), so we will use it in equation (10):

$$\theta_{SA} \le 57 - 6 - 1 = 50°C/W \qquad (10)$$

This is the required heat sink for each driver. For low TIM we add the 1 MΩ resistor from pin 3 to the output and a 910k resistor from pin 4 to ground. The complete schematic is shown below.

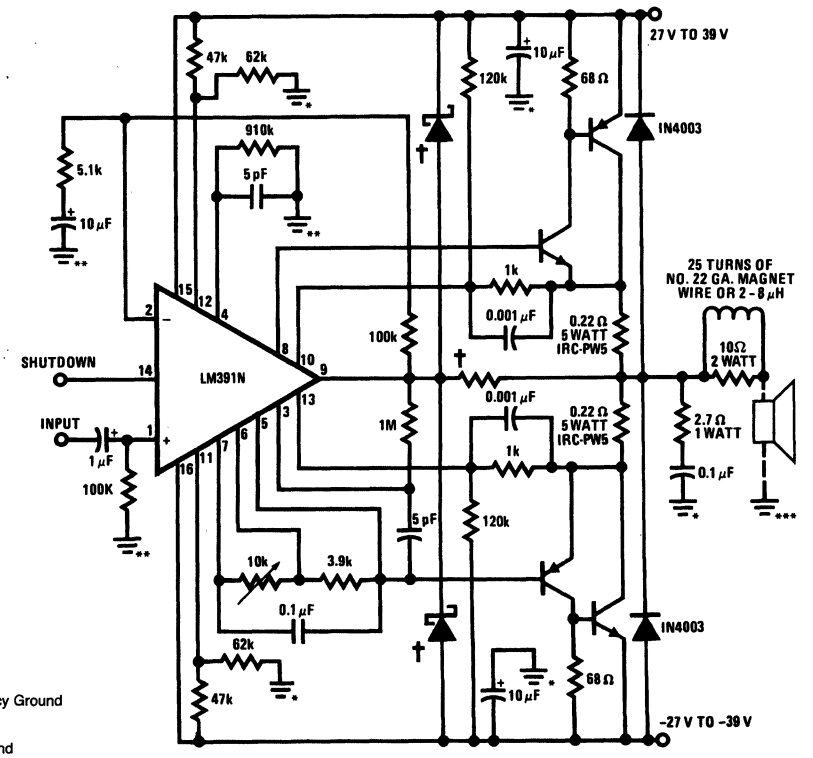
If the output is shorted, the transistor voltage is about 28V and the current is 5A. Therefore the average power is:

$$\text{short } \overline{PD} = \tfrac{1}{2}(28)\,5 = 70W$$

This is much larger than the power used to calculate the heat sinks and the output transistors will overheat if the output is shorted too long.

Typical Applications (Continued)

40W-8Ω, 60W-4Ω Amplifier



*High Frequency Ground

**Input Ground

***Speaker Ground

Note: All Grounds Should be Tied Together Only at Power Supply Ground.

†Additional protection for LM391N; Schottky diodes and R ≅ 100Ω.

TL/H/7146–13

National Semiconductor

LM831 Low Voltage Audio Power Amplifier

General Description

The LM831 is a dual audio power amplifier optimized for very low voltage operation. The LM831 has two independent amplifiers, giving stereo or higher power bridge (BTL) operation from two- or three-cell power supplies.

The LM831 uses a patented compensation technique to reduce high-frequency radiation for optimum performance in AM radio applications. This compensation also results in lower distortion and less wide-band noise.

The input is direct-coupled to the LM831, eliminating the usual coupling capacitor. Voltage gain is adjustable with a single resistor.

Features

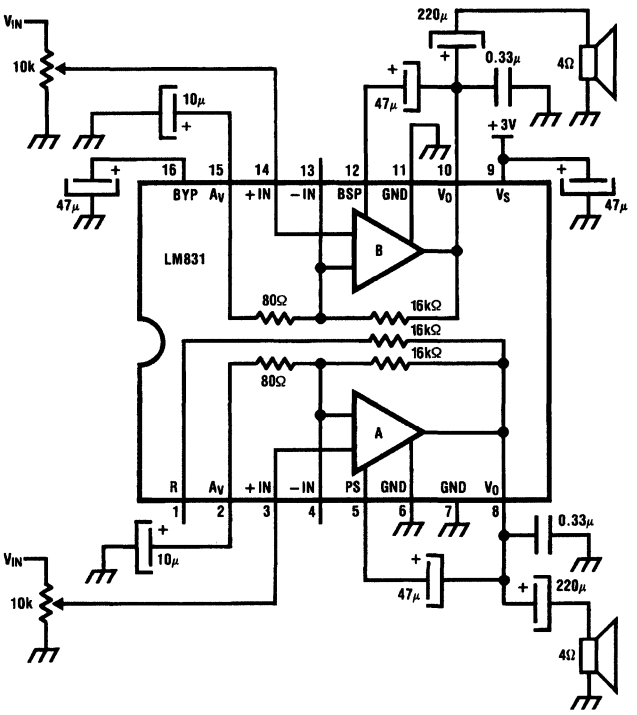
- Low voltage operation, 1.8V to 6.0V
- High power, 440 mW, 8Ω, BTL, 3V
- Low AM radiation
- Low noise
- Low THD

Applications

- Portable tape recorders
- Portable radios
- Headphone stereo
- Portable speakers

Typical Application

Dual Amplifier with Minimum Parts



TL/H/6754–1

A_V = 46 dB, BW = 250 Hz to 35 kHz

P_{OUT} = 220 mW/Ch, R_L = 4Ω

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	7.5V
Input Voltage, V_{IN}	±0.4V
Power Dissipation (Note 1), P_D	1.3W (M Package) 1.4W (N Package)
Operating Temperature (Note 1), T_{opr}	−40°C to +85°C
Storage Temperature, T_{stg}	−65°C to +150°C
Junction Temperature, T_j	+150°C
Lead Temp. (Soldering, 10 sec.), T_L	+260°C

Electrical Characteristics

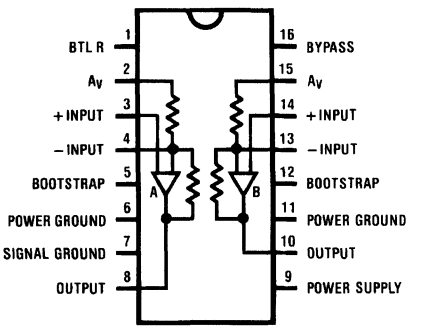
Unless otherwise specified, T_A = 25°C, V_S = 3V, f = 1 kHz, test circuit is dual or BTL amplifier with minimum parts.

Symbol	Parameter	Conditions	Typ	Tested Limit	Unit (Limit)
V_S	Operating Voltage		3 3	1.8 6	V(Min) V(Max)
I_Q	Supply Current	V_{IN} = 0, Dual Mode V_{IN} = 0, BTL Mode	5 6	10 15	mA (Max) mA (Max)
V_{OS}	Output DC Offset	V_{IN} = 0, BTL Mode	10	50	mV (Max)
R_{IN}	Input Resistance		25	15 35	k (Min) k (Max)
A_V	Voltage Gain	V_{IN} = 2.25 mV_{rms}, f = 1 kHz, Dual Mode	46	44 48	dB (Min) dB (Max)
PSRR	Supply Rejection	V_S = 3V + 200 mV_{rms} @ f = 1 kHz	46	30	dB (Min)
P_{OD}	Power Out	V_S = 3V, R_L = 4Ω, 10% THD, Dual Mode	220	150	mW (Min)
P_{ODL}	Power Out Low, V_S	V_S = 1.8V, R_L = 4Ω, 10% THD, Dual Mode	45	10	mW (Min)
P_{OB}	Power Out	V_S = 3V, R_L = 8Ω, 10% THD, BTL Mode	440	300	mW (Min)
P_{OBL}	Power Out Low, V_S	V_S = 1.8V, R_L = 8Ω, 10% THD, BTL Mode	90	20	mW (Min)
Sep	Channel Separation	Referenced to V_O = 200 mV_{rms}	52	40	dB (Min)
I_B	Input Bias Current		1	2	μA (Max)
E_{n0}	Output Noise	Wide Band (250 ~ 35 kHz)	250	500	μV (Max)
THD	Distortion	V_S = 3V, P_O = 50 mW, f = 1 kHz, Dual	0.25	1	% (Max)

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 98°C/W junction to ambient for the M package or 90°C/W junction to ambient for the N package.

Connection Diagram

Dual-In-Line Package



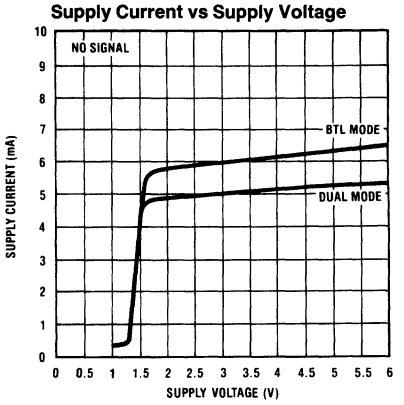
TL/H/6754–2

Top View

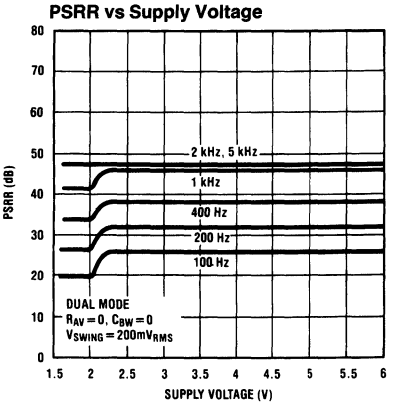
Order Number LM831M or N
See NS Package Number M16B or N16E

Typical Performance Characteristics

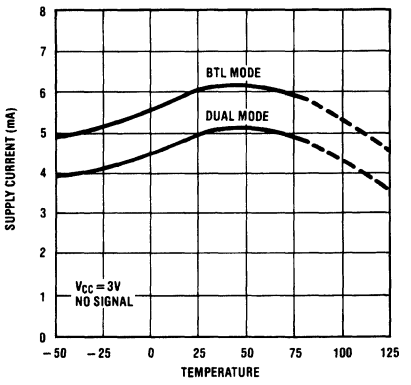
Supply Current vs Supply Voltage



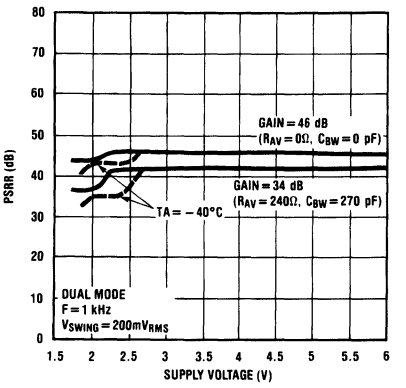
PSRR vs Supply Voltage



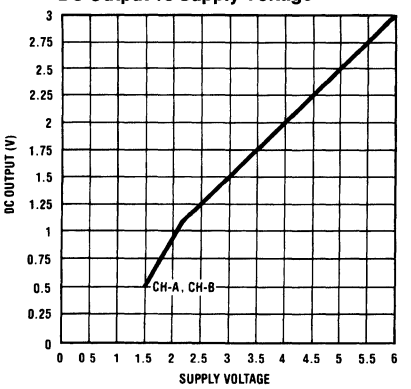
Supply Current vs Temperature



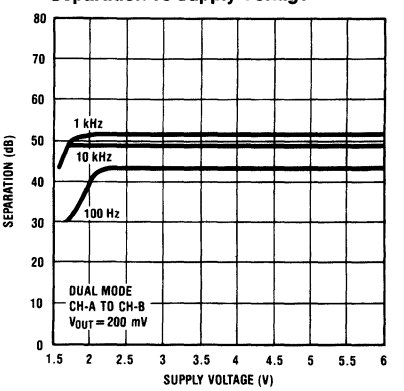
PSRR vs Supply Voltage



DC Output vs Supply Voltage



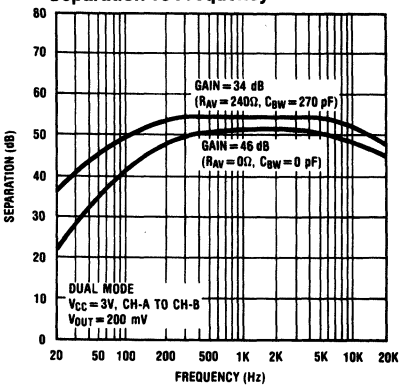
Separation vs Supply Voltage



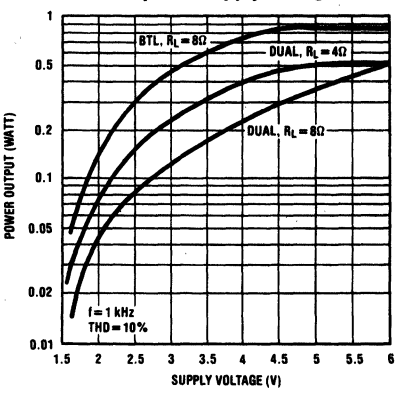
TL/H/6754–4

Typical Performance Characteristics (Continued)

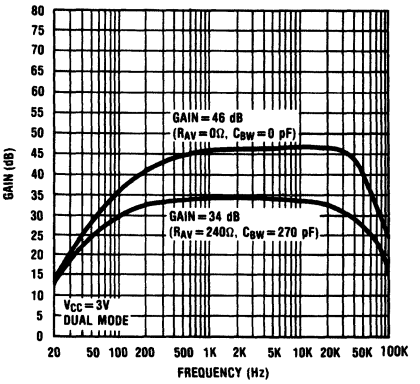
Separation vs Frequency



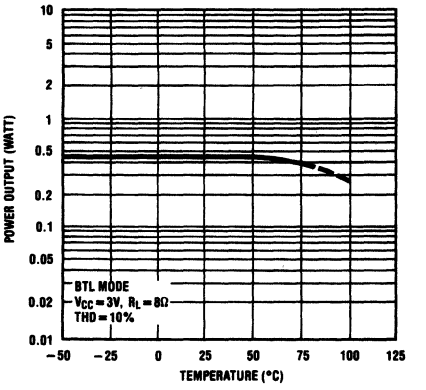
Power Output vs Supply Voltage



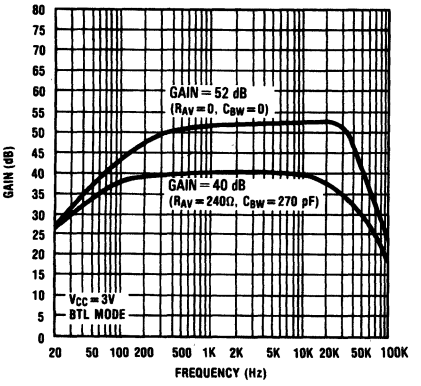
Gain vs Frequency



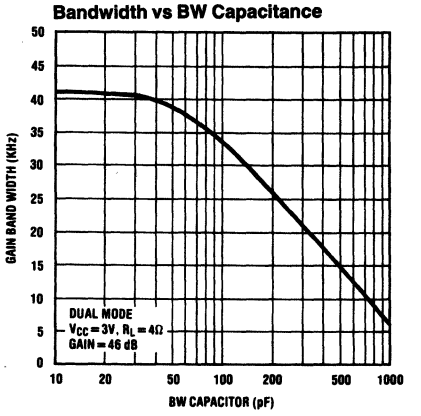
Power Output vs Temperature



Gain vs Frequency



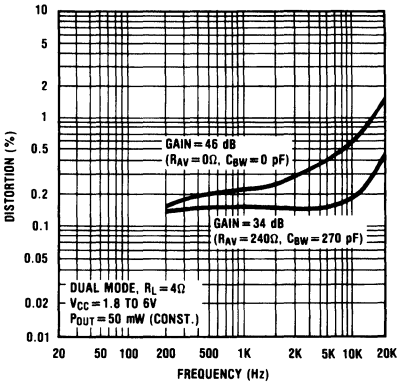
Bandwidth vs BW Capacitance



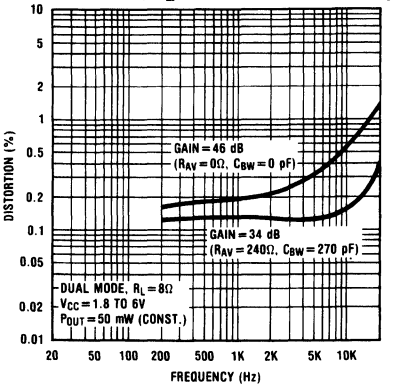
TL/H/6754–5

Typical Performance Characteristics (Continued)

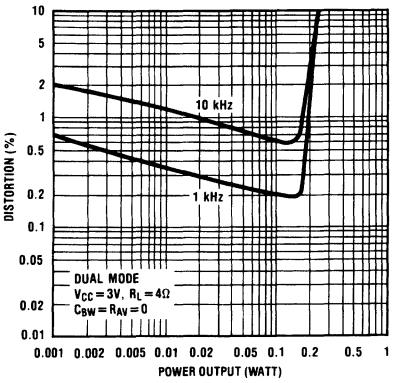
Dual Mode, $R_L = 4\Omega$ Distortion vs Frequency



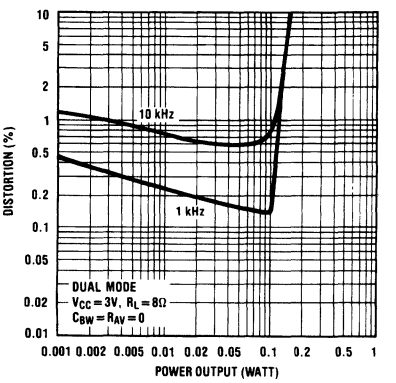
Dual Mode, $R_L = 8\Omega$ Distortion vs Frequency



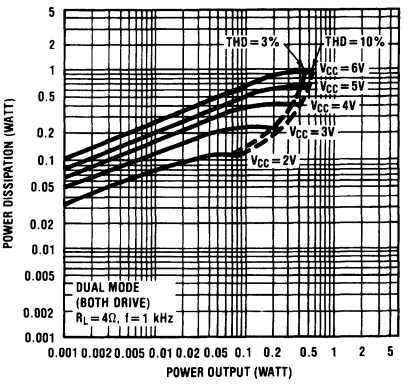
Distortion vs Power Output (Note 2)



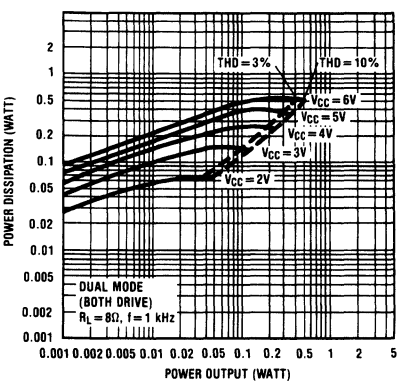
Distortion vs Power Output (Note 2)



Power Dissipation vs Power Output



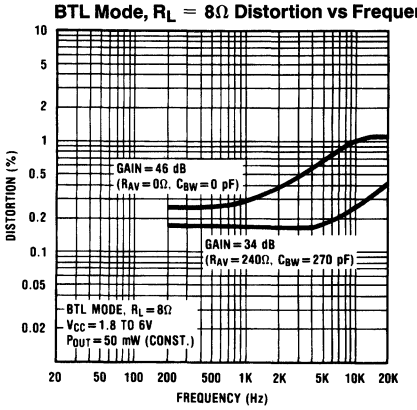
Power Dissipation vs Power Output



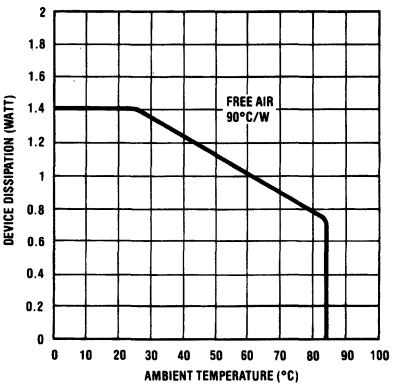
TL/H/6754–6

Typical Performance Characteristics (Continued)

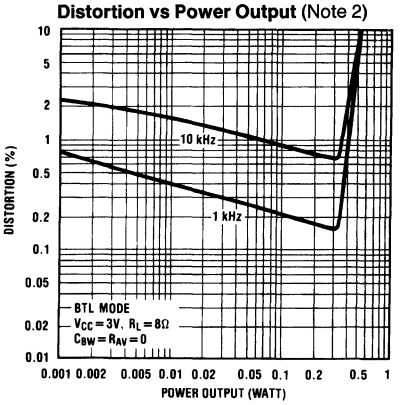
BTL Mode, $R_L = 8\Omega$ Distortion vs Frequency



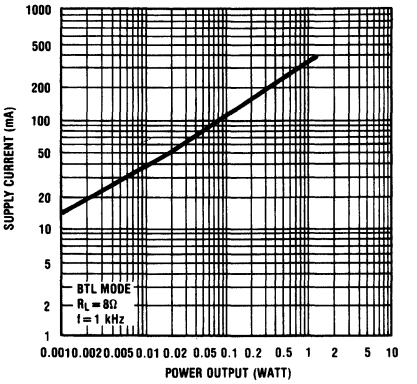
Device Dissipation vs Ambient Temperature



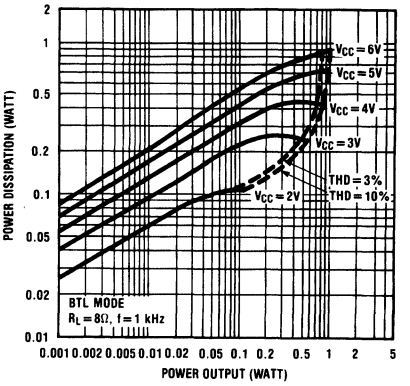
Distortion vs Power Output (Note 2)



Supply Current vs Power Output



Power Dissipation vs Power Output

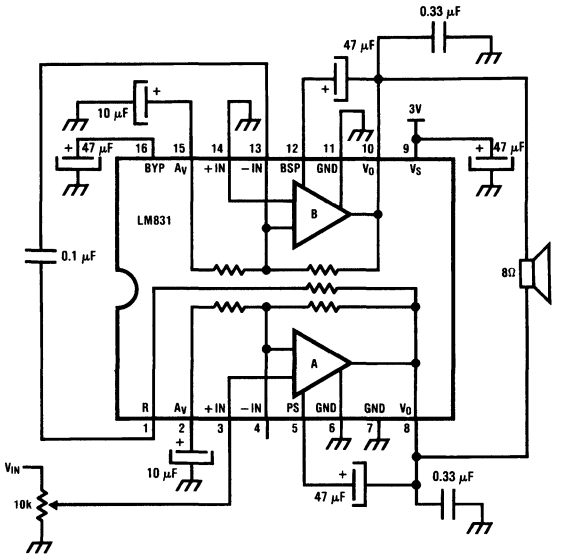


Note 2: 1 kHz curve is measured with 400 Hz–30 kHz Filter.

TL/H/6754–7

Typical Applications

BTL Amplifier with Minimum Parts

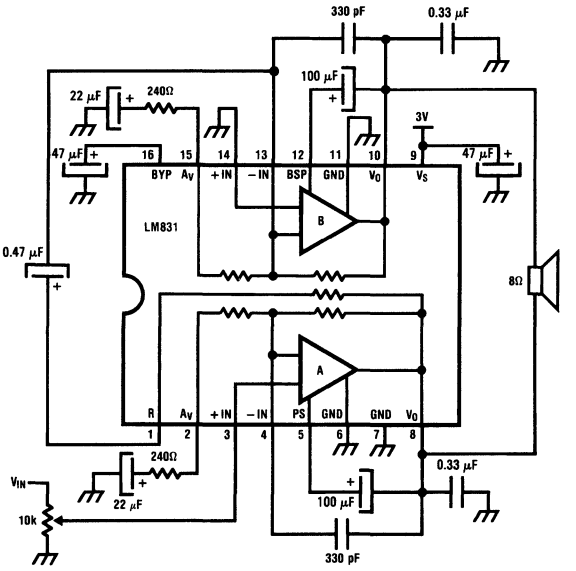


TL/H/6754–8

A_V = 52 dB, BW = 250 Hz to 25 kHz

P_{OUT} = 440 mW, R_L = 8Ω

BTL Amplifier for Hi-Fi Quality



TL/H/6754–9

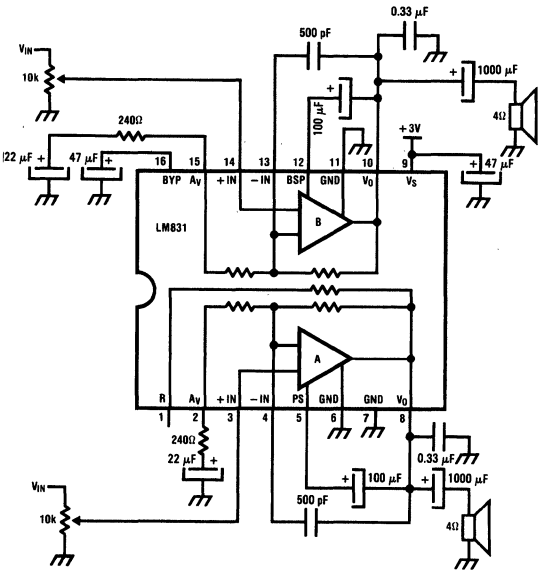
A_V = 40 dB, BW = 20 Hz to 20 kHz

P_{OUT} = 440 mW, R_L = 8Ω

(Dynamic Range Over 80 dB)

Typical Applications (Continued)

Dual Amplifier for Hi-Fi Quality



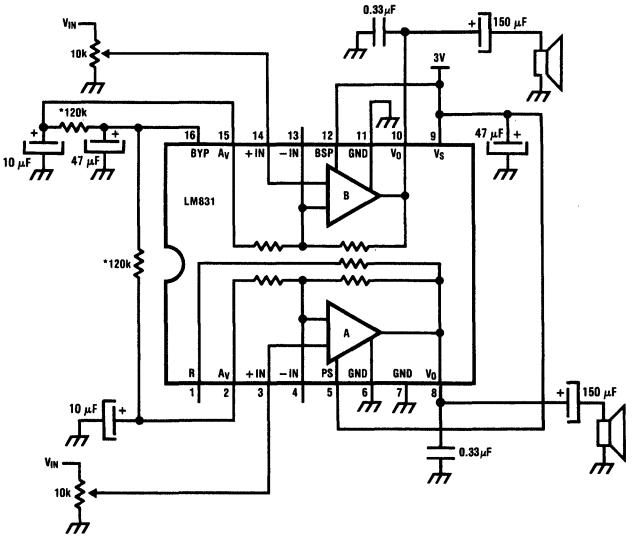
TL/H/6754–10

A_V = 34 dB, BW = 50 Hz to 20 kHz

P_{OUT} = 220 mW/Ch, R_L = 4Ω

(Dynamic Range Over 80 dB)

Low-Cost Power Amplifier (No Bootstrap)



TL/H/6754–11

P_{OUT} = 150 mW/Ch, BW = 300 Hz to 35 kHz

BTL Mode is also possible

*For 3-cell applications, the 120k resistor should be changed to 20K.

LM831 Circuit Description Refer to the external component diagram and equivalent schematic.

The power supply is applied to Pin 9 and is filtered by resistor R_1 and capacitor C_{BY} on Pin 16. This filtered voltage at Pin 16 is used to bias all of the LM831 circuits except the power output stage. Resistor R_0 generates a biasing current that sets the output DC voltage for optimum output power for any given supply voltage.

Feedback is provided to the input transistor Q_1 emitter by R_6 and R_7.

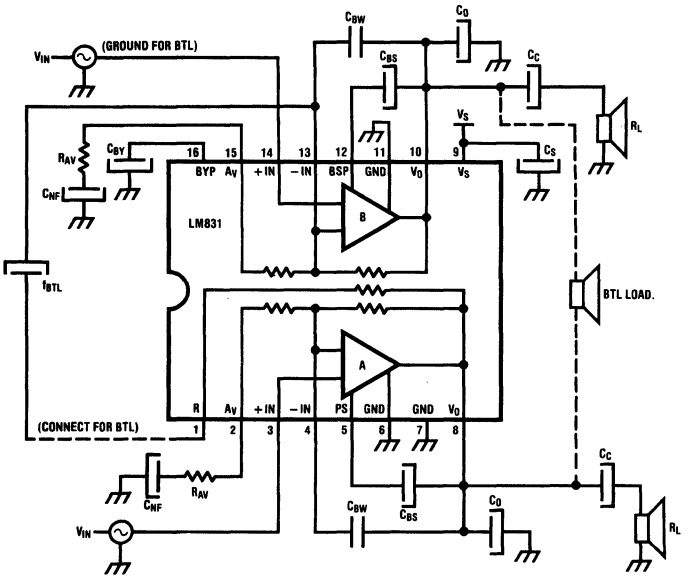
The capacitor C_{NF} on Pin 2 provides unity DC gain for maximum DC accuracy.

Q_2 provides voltage gain and the rest of the devices buffer the output load from Q_2's collector.

Bootstrapping of Pin 5 by C_{BS} allows maximum output swing and improved supply rejection.

R_5 is provided for bridge (BTL) operation.

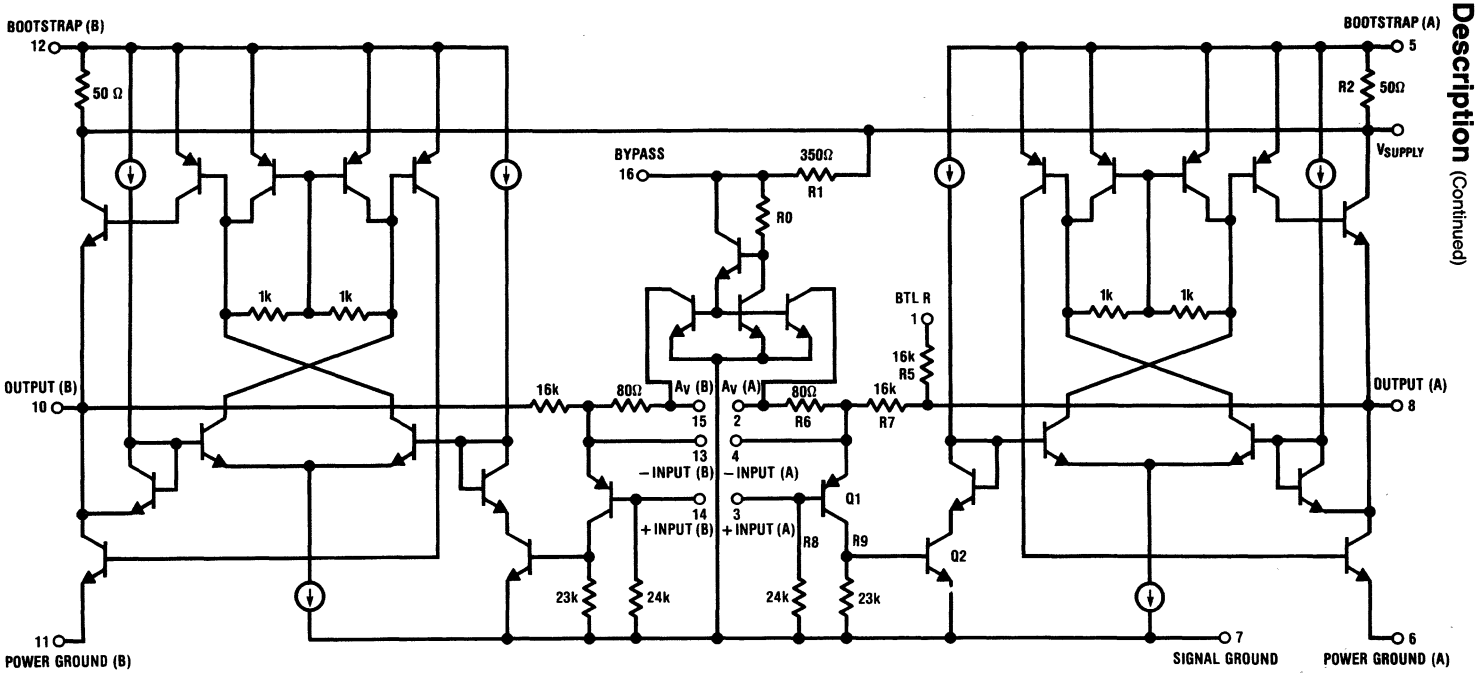
External Component Diagram



TL/H/6754–12

LM831 Circuit Description (Continued)

LM831 Equivalent Schematic



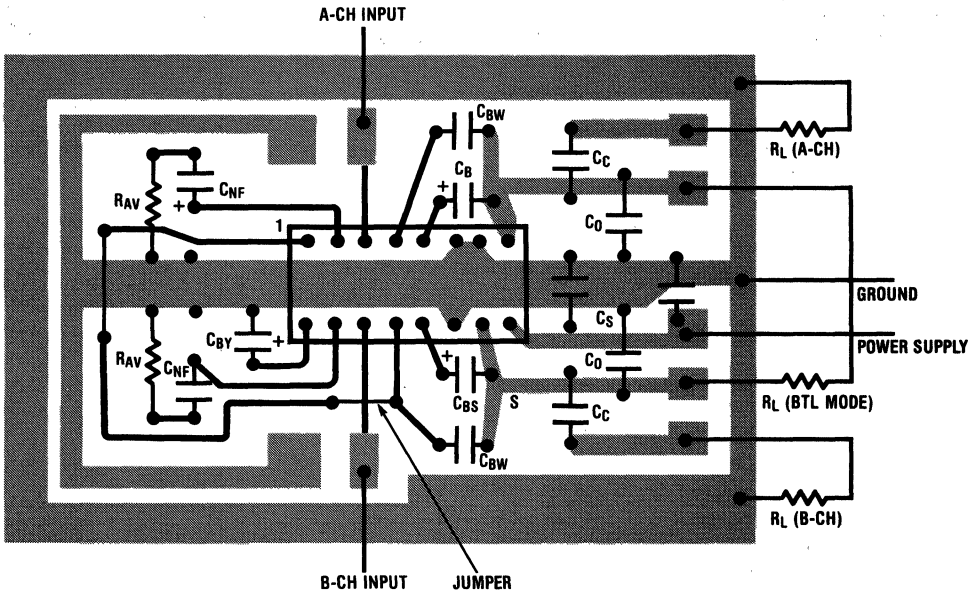
TL/H/6754–13

External Components (Refer to External Component Diagram)

Component	Comments	Min	Max
C_O	Required to stabilize output stage.	0.33 μF	1 μF
C_C	Output coupling capacitors for Dual Mode. Sets a low-frequency pole in the frequency response. $f_L = \frac{1}{2\pi C_C R_L}$	100 μF	10,000 μF
C_{BS}	Bootstrap capacitors. Sets a low-frequency pole in the power BW. Recommended value is $C_{BS} = \frac{1}{10 \bullet 2\pi \bullet f_L \bullet R_L}$	22 μF or (short Pins 4 & 12 to 9)	470 μF
C_S	Supply bypass. Larger values improve low-battery performance by reducing supply ripple.	47 μF	10,000 μF
C_{BY}	Filters the supply for improved low-voltage operation. Also sets turn-on delay.	47 μF	470 μF
C_{NF}	Sets a low-frequency response. Also affects turn-on delay. $f_L = \frac{1}{2\pi \bullet C_{NF} \bullet (R_{AV} + 80)}$ In BTL Mode, C_{NF} on Pin 15 can be reduced without affecting the frequency response. However, the turn-on "POP" will be worsened.	10 μF	100 μF
C_{BTL}	Used only in the Bridge Mode. Connects the output of the first amplifier to the inverting input of the other through an internal resistor. Sets a low-frequency pole in one-half the frequency response. $f_L = \frac{1}{2\pi \bullet C_{BTL} \bullet 16k}$	0.1 μF	1 μF
C_{BW}	Improves clipping waveform and sets the high-frequency bandwidth. Works with an internal 16k resistor. (This equation applies for $R_{AV} \neq 0$. For 46 dB application, see BW–C_{BW} curve.) $f_H = \frac{1}{2\pi \bullet C_{BW} \bullet 16k}$	See table below	
R_{AV}	Used to reduce the gain and improve the distortion and signal to noise. If this is desired, C_{BW} must also be used.	See table below	

Typical A_V	R_{AV}	C_{BW}	
		Min	Max
46 dB	Short	Open	4700 pF
40 dB	82	100 pF	4700 pF
34 dB	240	270 pF	4700 pF
28 dB	560	500 pF	4700 pF

Printed Circuit Layout for LM831N (Foil Side View) Refer to External Component Diagram



TL/H/6754–14

Note: Power ground pattern should be as wide as possible. Supply bypass capacitor should be as close to the IC as possible. Output compensation capacitors should also be close to the IC.

National Semiconductor

DNR® DYNAMIC NOISE REDUCTION SYSTEM

LM832 Dynamic Noise Reduction System DNR®

General Description

The LM832 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is noncomplementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

The LM832 is optimized for low voltage operation with input levels around 30 mVrms.

For higher input levels use the LM1894.

Features

- Low voltage battery operation
- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 1.5V to 9V
- 150 mVrms input overload
- No royalty requirements
- Cascade connection for 17 dB noise reduction

Applications

- Headphone stereo
- Microcassette players
- Radio cassette players
- Automotive radio/tape players

Application Circuit

Order Number LM832M See NS Package M14A
Order Number LM832N See NS Package N14A

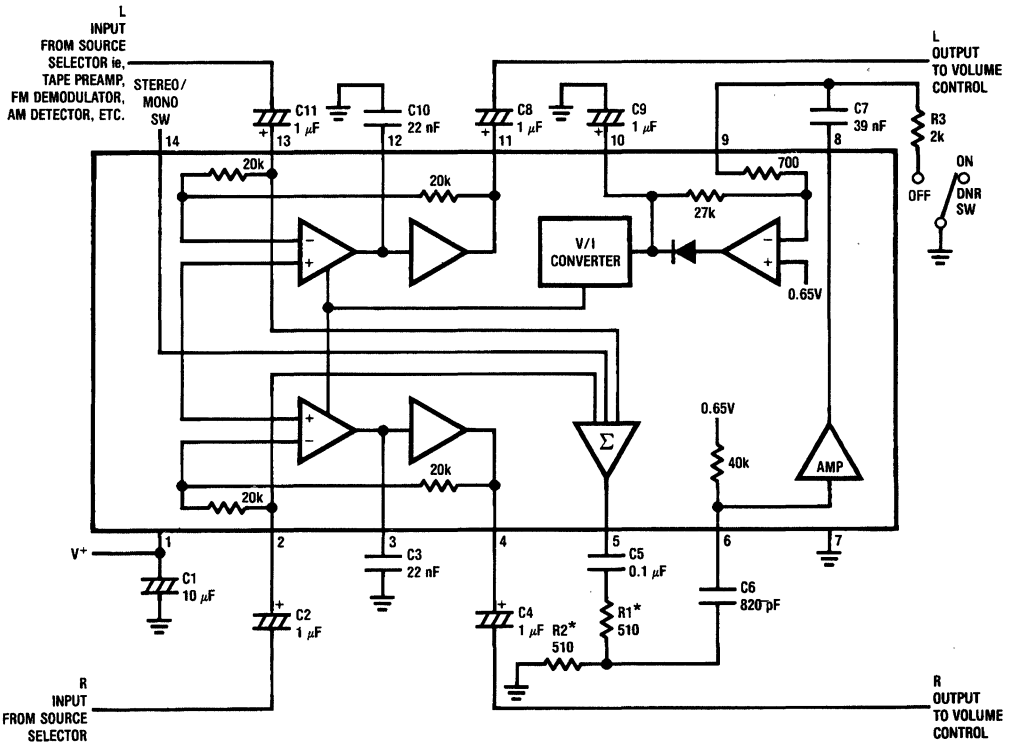


FIGURE 1. Component Hook-up for Stereo DNR System

TL/H/5176–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10V
Power Dissipation (Note 1)	1.2W
Input Voltage	1.7 Vpp
Storage Temperature	−65 to +150°C
Operating Temperature (Note 1)	−40 to +85°

Soldering Information

- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effects on Products Reliability" for other methods of soldering surface mount devices."

DC Electrical Characteristics T_A = 25°C V_{CC} = 3.0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OP}	Operating Voltage	Supply Voltage for Normal Operation	1.5	3.0	9.0	V
$I_{CC}(1)$	Supply Current (1)	Pin 9 to GND 0.1 μF, BW = Min, Note 2		2.5	4.0	mA
$I_{CC}(2)$	Supply Current (2)	DC GND Pin 9 with 2k, BW = Max, Note 2		5.0	8.0	mA
$V_{IN}(1)$	Input Voltage (1)	Pin 2, Pin 13	0.20	0.36	0.5	V
$V_{IN}(2)$	Input Voltage (2)	Pin 6	0.50	0.65	0.8	V
$V_{IN}(3)$	Input Voltage (3)	Pin 9	0.50	0.65	0.8	V
$V_{OUT}(1)$	Output Voltage (1)	Pin 4, Pin 11	0.20	0.35	0.50	V
$V_{OUT}(2)$	Output Voltage (2)	Pin 5 Stereo Mode	0.15	0.28	0.40	V
$V_{OUT}(3)$	Output Voltage (3)	Pin 5 Monaural Mode, DC Ground Pin 14	0.10	0.20	0.30	V
$V_{OUT}(4)$	Output Voltage (4)	Pin 8	0.25	0.40	0.60	V
$V_{OUT}(5)$	Output Voltage (5)	Pin 10 BW = Max, Note 2	1.00	1.27	1.50	V
$V_{OUT}(6)$	Output Voltage (6)	Pin 10 BW = Min, Note 2	0.50	0.65	0.75	V
V_{OS}	Output DC Shift	Pin 4, PIN 11; Change BW Min to Max		1.0	3.0	mV

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MAIN SIGNAL PATH (Note 3)						
A_V	Voltage Gain	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2	−1.0	0.0	+1.0	dB
C.B.	Channel Balance	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2	−1.0	0	+1.0	dB
f_{MIN}	Min Bandwidth	0.1 μF between Pin 9 - GND	600	1000	1500	Hz
f_{MAX}	Max Bandwidth	DC Ground Pin 9 with 2k	24	30	46	kHz
THD	Distortion	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2		0.07	0.5	%
MV_{IN}	Max Input Voltage	THD = 3%, f = 1 kHz, BW = Max Note 2	120	150		mVrms
S/N	Signal to Noise	REF = 30 mVrms, BW = Max, CCIR/ARM	60	68		dB
Z_{IN}	Input Impedance	Pin 2, Pin 13	14	20	26	kΩ
C.S.	Channel Separation	Ref = 30 mVrms, f = 1 kHz, BW = Max, Note 2	40	68		dB
P_{SRR}	P_{SRR}	V_{RIPPLE} = 50 mVrms, f = 100 Hz	40	55		dB
CONTROL PATH						
$A_V$sum(1)	Summing Amp Gain (1)	V_{IN} = 30 mVrms at R and L, f = 1 kHz	−3.0	−1.5	0.0	dB
$A_V$sum(2)	Summing Amp Gain (2)	DC Ground Pin 14, f = 1 kHz	−9.0	−6.0	−3.0	dB
A_V 1st	Gain Amp Gain	Pin 6 to Pin 8	25	30	35	dB
Z_{IN} 1st	Input Impedance	Pin 6	28	40	52	kΩ
A_{VPKD}	Peak Detector Gain	AC In, DC Out; Pin 9 to Pin 10	25	30	35	V/V
Z_{INPKD}	Input Impedance	Pin 9	500	800	1100	Ω
V_{RPKD}	Output DC Change	Pin 10, Change BW Min to Max	0.5	0.62	0.8	V

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance junction to ambient, as follows: LM832N −90° c/w, LM832M-115° c/w.

Note 2: To force the DNR system into maximum bandwidth, connect a 2k resistor from pin 9 to GND. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Application Hints.

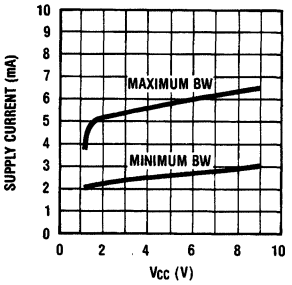
Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives 10 dB of noise reduction. See Application Hints.

External Component Guide (See *Figure 1*)

P/N	Recommended Value	Purpose	Effect		Remarks
			Smaller	Larger	
C1	10 μF	Power supply decoupling	Poor supply rejection	Better supply rejection	Do not use less than 10 μF
C2,C11	1 μF	Input coupling capacitor	Increases frequency of low-frequency roll-off	Reduces frequency of low-frequency roll-off	DC voltage at pin 2 and pin 13 is 0.35V $f=\frac{1}{2\pi C_2 R_{IN}}$
C3,C10	22 nF for Stereo, 15 nF for mono	Establishment of Min and Max Bandwidth	Bandwidth becomes wider	Bandwidth becomes narrower	See Note 4
C4,C8	1 μF	Output coupling capacitor	Increases frequency of low-frequency roll-off	Reduces frequency of low-frequency roll-off	DC voltage at pin 4 and pin 11 is 0.35V $f=\frac{1}{2\pi C_4 R_{LOAD}}$
C5	0.1 μF	Works with R1 and R2 to set one of the low-frequency corners in control path	Some high frequency program material may be attenuated	Bandwidth may increase due to low-frequency inputs, causing "Breathing"	$f=\frac{1}{2\pi C_5(R1+R2)}=1.6$ kHz See Note 4
C6	820 pF	Works with input resistance of pin 6 to set one of the low-frequency corners in the control path	Same as above	Same as above	$f=\frac{1}{2\pi C_6 R_{PIN6}}=4.8$ kHz See Note 4
C7	39 nF	Works with input resistance of pin 9 to form part of control path frequency weighing	Same as above	Same as above	$f=\frac{1}{2\pi C_7 R_{PIN7}}=4.8$ kHz See Note 4
C9	1 μF	Sets attack time	Reduces attack and decay time	Increases attack and decay time	See Note 4
R1,R2	$R_1+R_2=1$ kΩ	This voltage divider sets control path sensitivity	—	—	Sensitivity should be set for maximum noise reduction and minimum audible frequency program effect on high
R3	•2 kΩ	Sets gain amp load when DNR is OFF	Loads gain amp output, may cause distortion	Max bandwidth will be reduced	

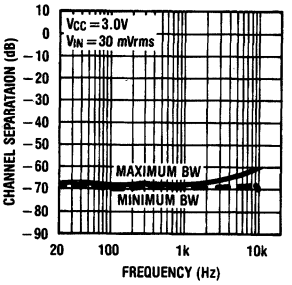
Note 4: The values of the control path filter components (C5, C6, C7, C9, R1, R2) and the integrating capacitors (C3, C10) should not be changed from the recommended values unless the characteristics of the noise or program material differ substantially from that of FM or tape sources. Failure to use the correct values may result in degraded performance, and therefore the application may not be approved for DNR trademark usage. Please contact National Semiconductor for more information and technical assistance.

Typical Performance Characteristics



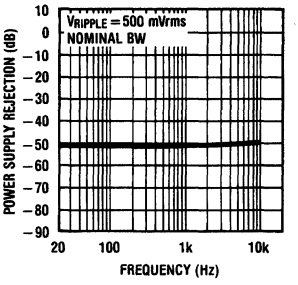
TL/H/5176–2

FIGURE 2. Supply current vs supply voltage



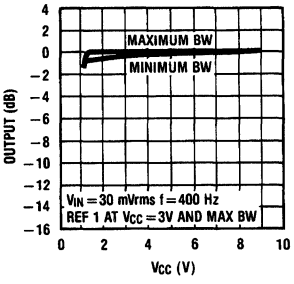
TL/H/5176–3

FIGURE 3. Channel separation vs frequency



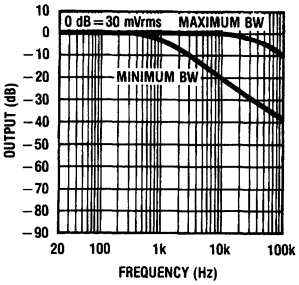
TL/H/5176–4

FIGURE 4. Power supply rejection ratio vs frequency



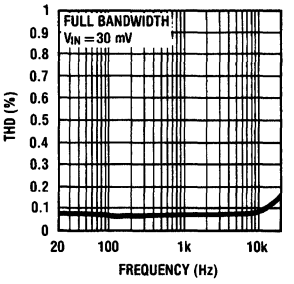
TL/H/5176–5

FIGURE 5. Output level change vs supply voltage



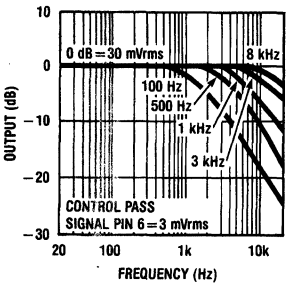
TL/H/5176–6

FIGURE 6. Output level vs frequency



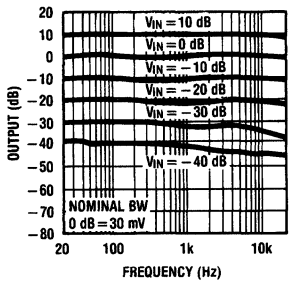
TL/H/5176–7

FIGURE 7. THD vs frequency



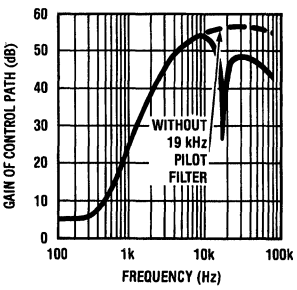
TL/H/5176–8

FIGURE 8. Output vs frequency and control path signal



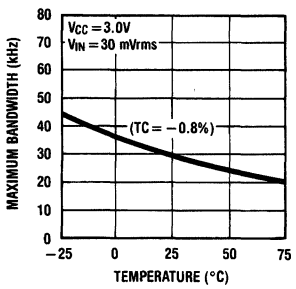
TL/H/5176–9

FIGURE 9. Frequency response for various input levels



TL/H/5176–10

FIGURE 10. Gain of control path vs frequency



TL/H/5176–11

FIGURE 11. Change in main signal path maximum bandwidth vs temperature

Circuit Operation

The LM832 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a g_m block with a variable current, and a unity gain buffer. As seen in *Figure 1*, DC feedback constrains the low frequency gain to $A_V = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.022 μF capacitor.

The purpose of the control path is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 1*. The R1, R2 resistor divider adjusts the incoming noise level to slightly open the bandwidth of the low pass filter. Control path gain is about 60dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 μF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the g_m blocks. The bandwidth sensitivity to g_m current is 70 Hz/μA. In FM stereo applications a 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 16*.

Normal methods of evaluating the frequency response of the LM 832 can be misleading if the input signal is also applied to the control path. Since the control path includes a frequency weighting network, a constant amplitude but varying frequency input signal will change the audio signal path bandwidth in a non-linear fashion. Measurements of the audio signal path frequency response will therefore be in error since the bandwidth will be changing during the measurement. See *Figure 9* for an example of the misleading results that can be obtained from this measurement approach. Although the frequency response is always flat below a single high-frequency pole, the lower curves do not resemble single pole responses at all.

A more accurate evaluation of the frequency response can be seen in *Figure 8*. In this case the main signal path is frequency swept while, the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

PSYCHOACOUSTIC BASICS

The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR system operates on three principles of psychoacoustics.

1. Music and speech can mask noise. In the absence of source material, background noise can be very audible. However, when music or speech is present, the human ear is less able to distinguish the noise—the source material is said to mask the noise. The degree of masking is dependent on the amplitude and spectral content (frequencies) of the source material, but in general multiple tones around 1 kHz are capable of providing excellent masking of noise over a very wide frequency range.

2. The ear cannot detect distortion for less than 1 ms. On a transient basis, if distortion occurs in less than 1 ms, the ear acts as an integrator and is unable to detect it. Because of this, signals of sufficient energy to mask noise open the bandwidth to 90% of the maximum value in less than 1 ms. Reducing the bandwidth to within 10% of its minimum value is done in about 60 ms: long enough to allow the ambience of the music to pass through, but not so long as to allow the noise floor to become audible.

3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR system low pass filters this noise. Low frequency music will not appreciably open the DNR bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Application Hints

The DNR system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to slightly open the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 12*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C10, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.022 μF capacitor to 0.015 μF will change the typical bandwidth from 1 kHz–30 kHz to 1.5 kHz–44 kHz. With C3 and C10 set at 0.022 μF, the maximum bandwidth is typically 30 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C9. Decay times can be decreased by paralleling a resistor with C9, and increased by increasing the value of C9.

When measuring the amount of noise reduction of DNR in a cassette tape system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 13*. The DNR system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.

Application Hints (Continued)

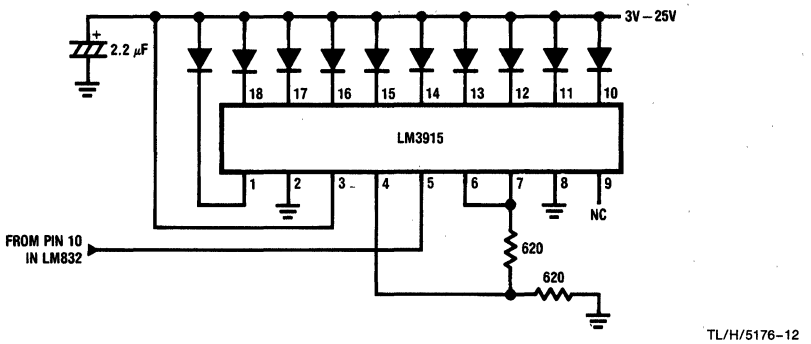


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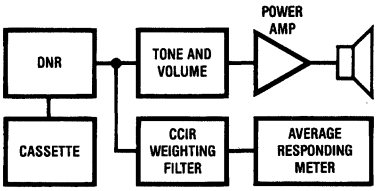
FIGURE 12. Bar Graph Display of Peak Detector Voltage



TL/H/5176–13

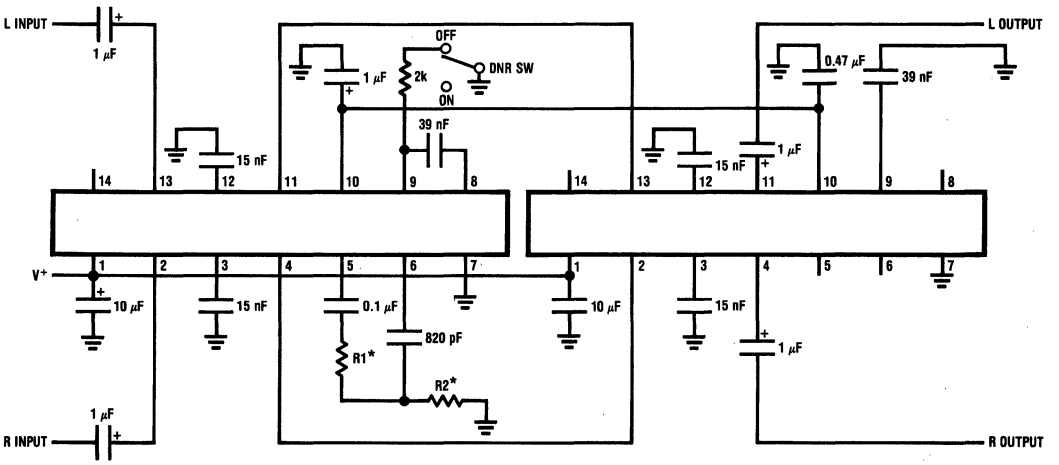
FIGURE 13. Technique for Measuring S/N Improvement of the DNR System

CASCADE CONNECTION

Additional noise reduction can be obtained by cascading the DNR filters. With two filters cascaded the rolloff is 12 dB per octave. For proper operating bandwidth the capacitors on pin 3 and 12 are changed to 15 nF. The resulting noise reduction is about 17 dB.

Figure 15 shows the monaural cascade connection. Note that pin 14 is grounded so only the pin 2 input is fed to the summing amp and therefore the control path.

Figure 14 shows the stereo cascade connection. Note that pin 14 is open circuit as in normal stereo operation.

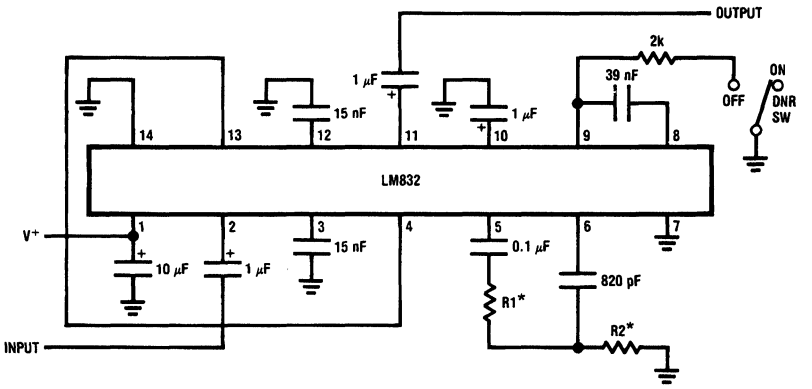


*R1 + R2 = 1 kΩ (refer to application hints)

TL/H/5176–14

FIGURE 14. Stereo Cascade Connection

Application Hints (Continued)



*R1 + R2 = 1 kΩ (refer to application hints)

TL/H/5176–15

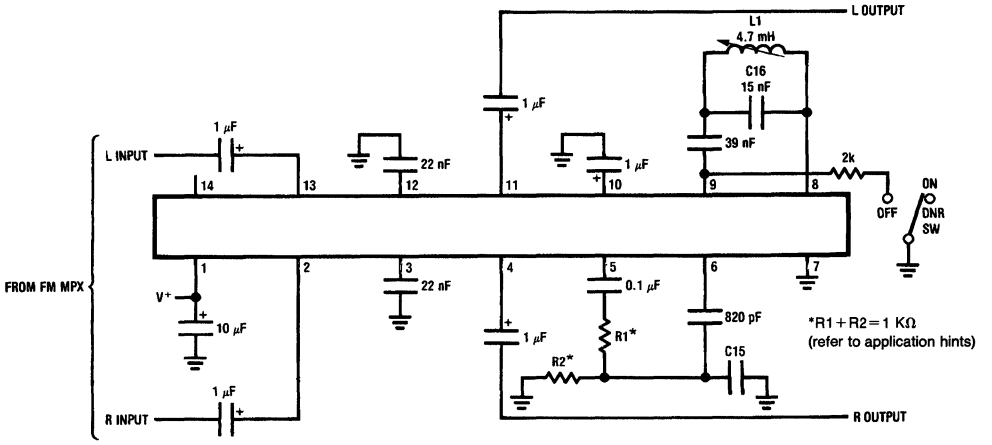
FIGURE 15. Monaural Cascade Connection

FM STEREO

When using the DNR system with FM stereo as the audio source, it is important to eliminate the ultrasonic frequencies that accompany the audio. If the radio has a multiplex filter to remove the ultrasonics there will be no problem.

This filtering can be done at the output of the demodulator, before the DNR system, or in the DNR system control path.

Standard audio multiplex filters are available for use at the output of the demodulator from several filter companies. *Figure 16* shows the additional components L1, C15 and C16 that are added to the control path for FM stereo applications. The coil must be tuned to 19 kHz, the FM pilot frequency.



TL/H/5176–16

FIGURE 16. FM Stereo Application

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System" Blackmer, 'dB' Magazine, August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, Sert Journal, May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, Audioscene Canada, April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, JAES, 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, JAES, Volume 39, #4, 1966.

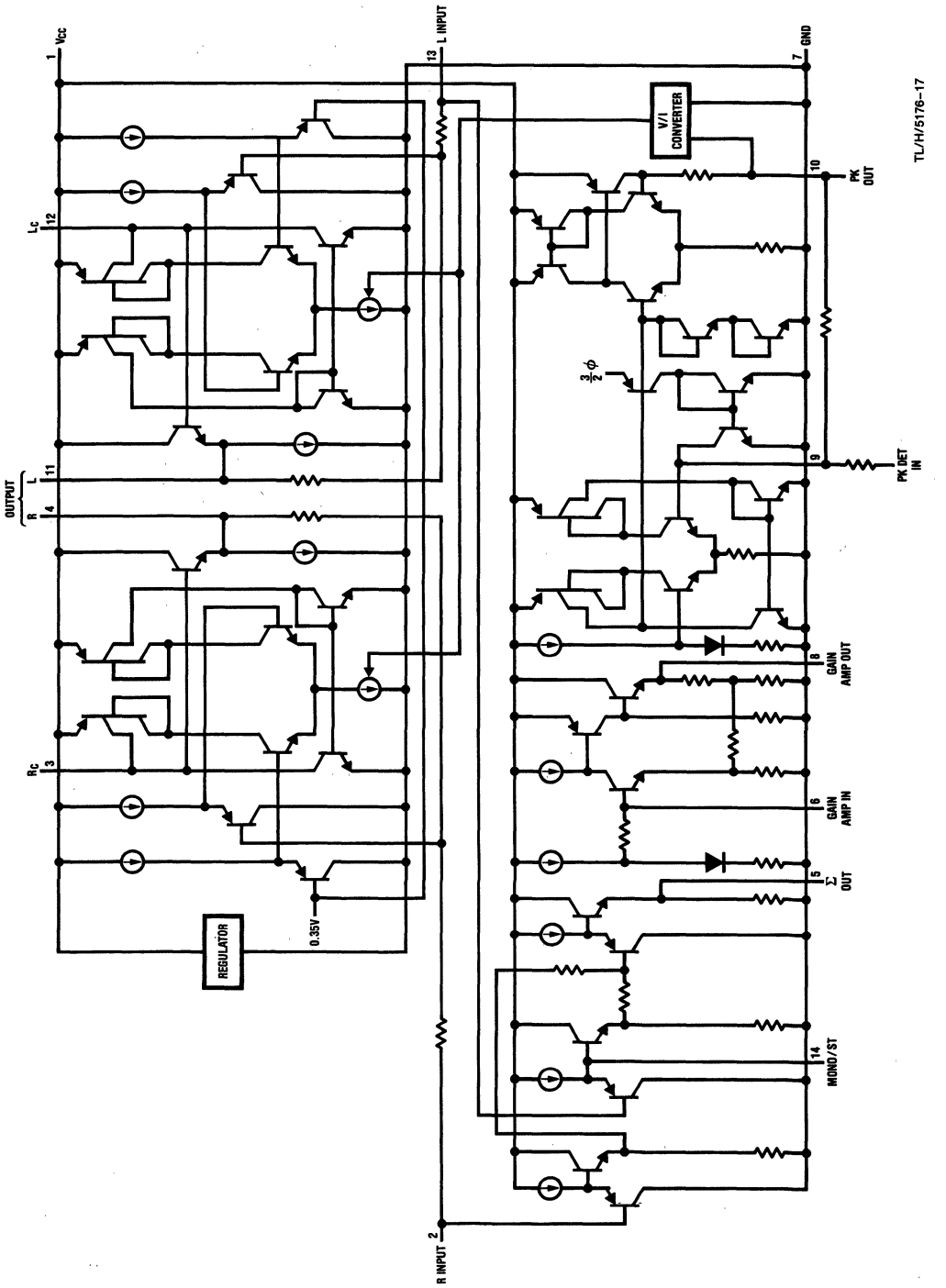
2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, JAES, Volume 22, #1, 1950.

3. "Sound System Engineering", Davis, Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

LM832 Simple Circuit Schematic



National Semiconductor

LM833 Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

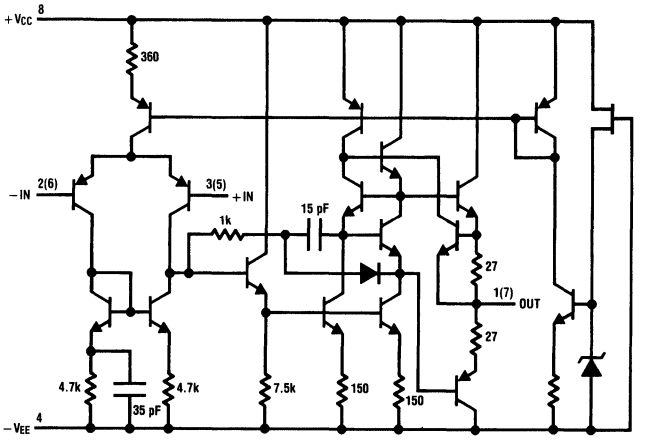
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

Features

■ Wide dynamic range	>140 dB
■ Low input noise voltage	4.5 nV/√Hz
■ High slew rate	7 V/μs (typ) 5 V/μs (min)
■ High gain bandwidth product	15 MHz (typ) 10 MHz (min)
■ Wide power bandwidth	120 kHz
■ Low distortion	0.002%
■ Low offset voltage	0.3 mV
■ Large phase margin	60°

Schematic Diagram (1/2 LM833)



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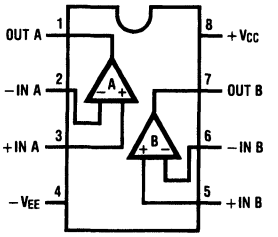
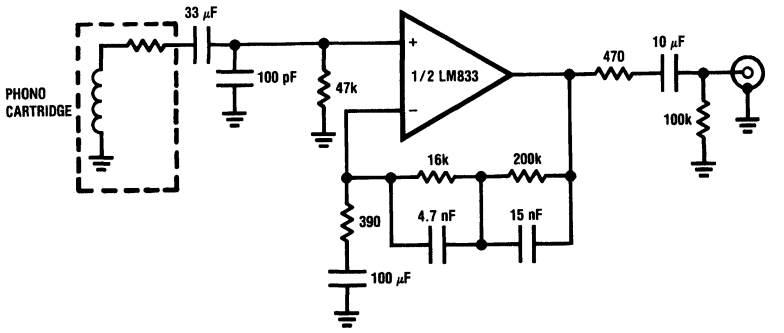
Connection Diagram



TL/H/5218–2

Order Number LM833M or LM833N
See NS Package Number
M08A or N08E

Typical Application RIAA Preamp



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A_v = 35 dB — f = 1 kHz
E_n = 0.33 μV — A Weighted
S/N = 90 dB — A Weighted, V_{IN} = 10 mV @ f = 1 kHz

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	$V_{CC}-V_{EE}$	36V
Differential Input Voltage (Note 1)	V_{ID}	±30V
Input Voltage Range (Note 1)	V_{IC}	±15V
Power Dissipation (Note 2)	P_D	500 mW
Operating Temperature Range	T_{OPR}	−40 ~ 85°C
Storage Temperature Range	T_{STG}	−60 ~ 150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 1600V

DC Electrical Characteristics (T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ R_L = 2 kΩ	±12 ±10	±13.5 ±13.4		V V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics (T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz

Design Electrical Characteristics (T_A = 25°C, V_S = ±15V)

The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	nV/$\sqrt{Hz}$
i_n	Input Referred Noise Current	f = 1 kHz	0.7	pA/$\sqrt{Hz}$
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

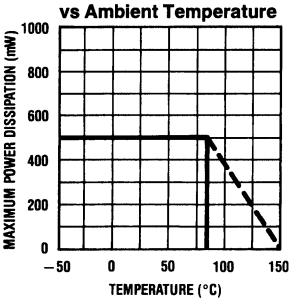
Note 1: If supply voltage is less than ±15V, it is equal to supply voltage.

Note 2: This is the permissible value at $T_A \leq 85°C$.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

Maximum Power Dissipation vs Ambient Temperature



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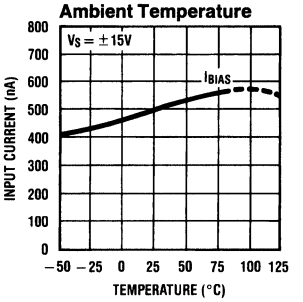
Input Bias Current vs Ambient Temperature



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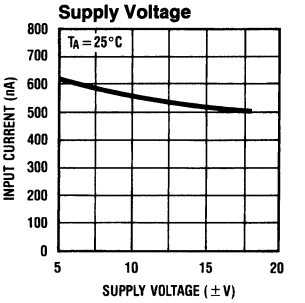
Input Bias Current vs Supply Voltage



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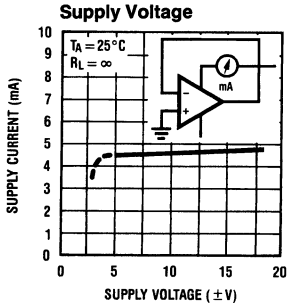
Supply Current vs Supply Voltage



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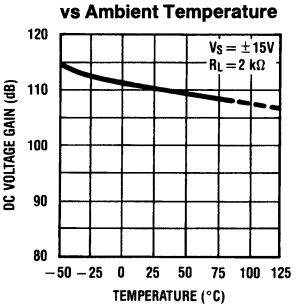
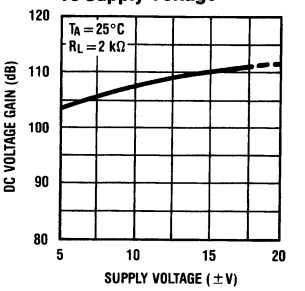
DC Voltage Gain vs Ambient Temperature



TL/H/5218–8

DC Voltage Gain vs Supply Voltage



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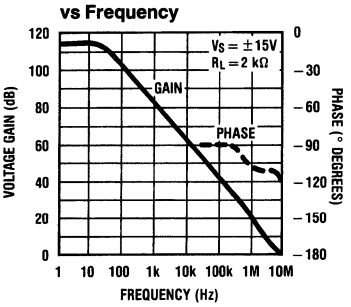
Voltage Gain & Phase vs Frequency



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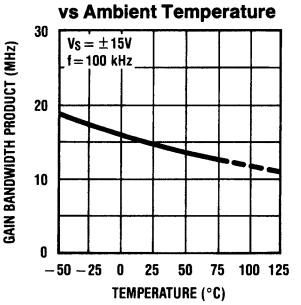
Gain Bandwidth Product vs Ambient Temperature



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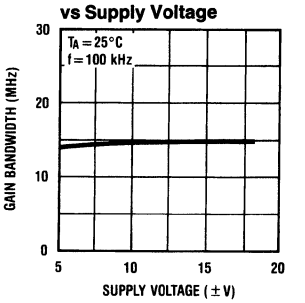
Gain Bandwidth vs Supply Voltage



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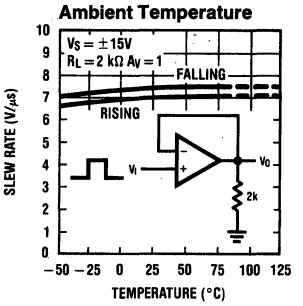
Typical Performance Characteristics (Continued)

Slew Rate vs Ambient Temperature



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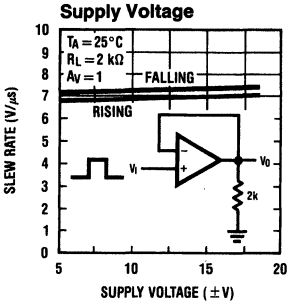
Slew Rate vs Supply Voltage



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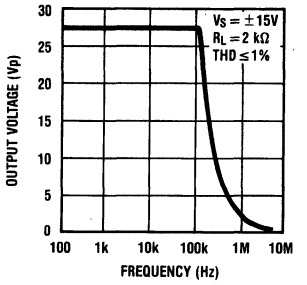
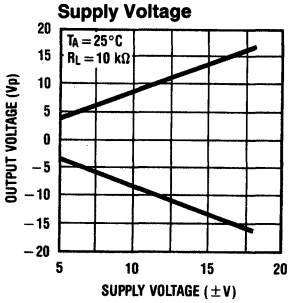
Power Bandwidth



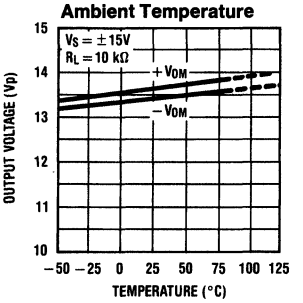
TL/H/5218–15

Maximum Output Voltage vs Supply Voltage



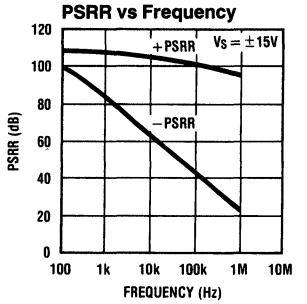
TL/H/5218–16

Maximum Output Voltage vs Ambient Temperature



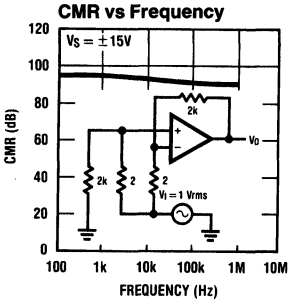
TL/H/5218–17

PSRR vs Frequency



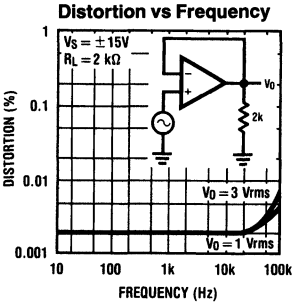
TL/H/5218–18

CMR vs Frequency



TL/H/5218–19

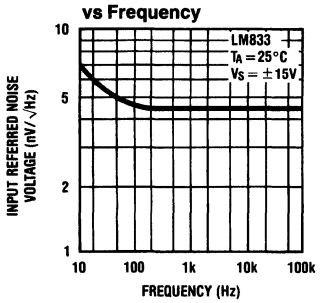
Distortion vs Frequency



TL/H/5218–20

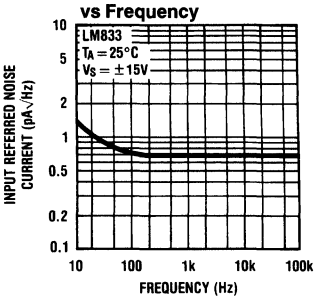
Typical Performance Characteristics (Continued)

Spot Noise Voltage vs Frequency



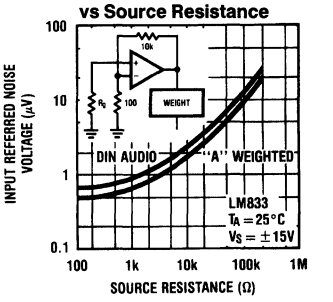
TL/H/5218–21

Spot Noise Current vs Frequency



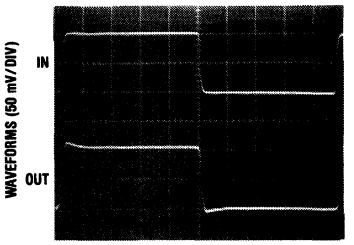
TL/H/5218–22

Input Referred Noise Voltage vs Source Resistance



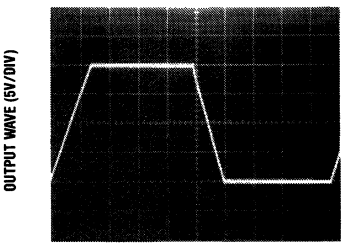
TL/H/5218–23

Noninverting Amp



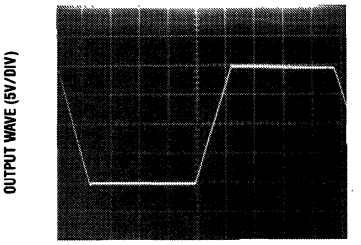
TL/H/5218–24

Noninverting Amp



TL/H/5218–25

Inverting Amp



TL/H/5218–26

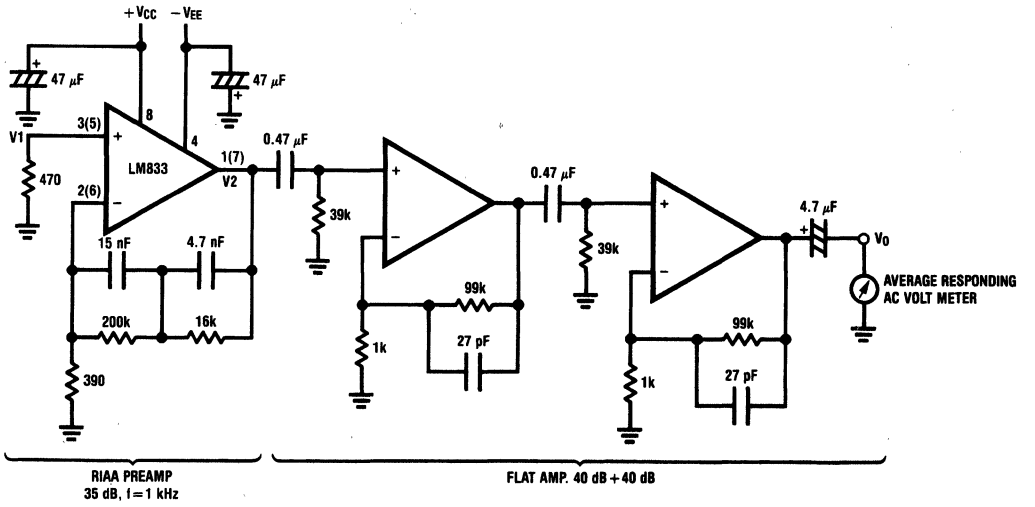
Application Hints

The LM833 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

Noise Measurement Circuit

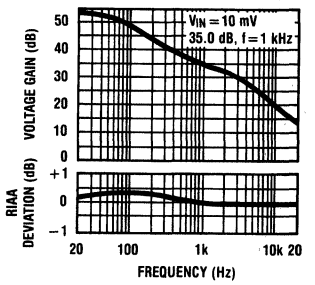
Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.



TL/H/5218–27

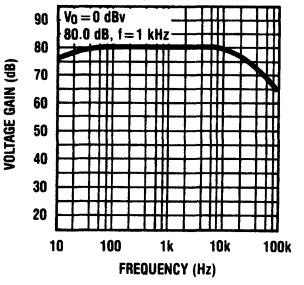
Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: e_n = V0/560,000 (V)

RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency



TL/H/5218–28

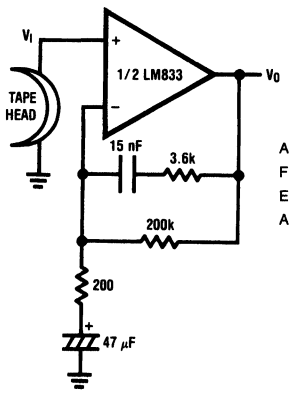
Flat Amp Voltage Gain vs Frequency



TL/H/5218–29

Typical Applications

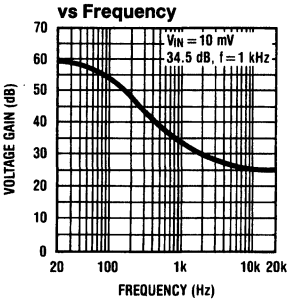
NAB Preamp



A_V = 34.5
F = 1 kHz
E_n = 0.38 µV
A Weighted

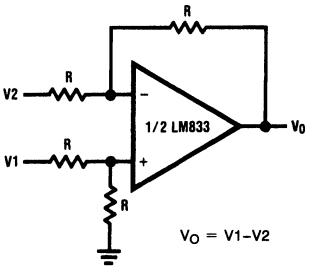
TL/H/5218-30

NAB Preamp Voltage Gain vs Frequency



TL/H/5218-31

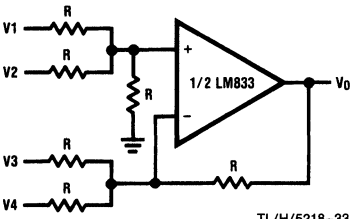
Balanced to Single Ended Converter



$V_O = V1 - V2$

TL/H/5218-32

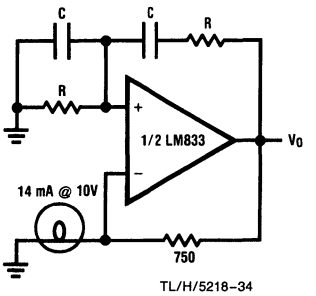
Adder/Subtracter



$V_O = V1 + V2 - V3 - V4$

TL/H/5218-33

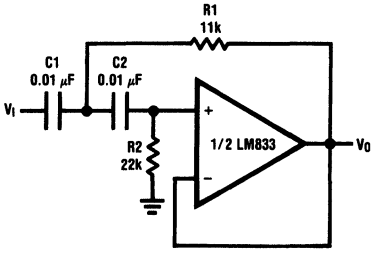
Sine Wave Oscillator



TL/H/5218-34

$$f_o = \frac{1}{2\pi RC}$$

Second Order High Pass Filter (Butterworth)



TL/H/5218-35

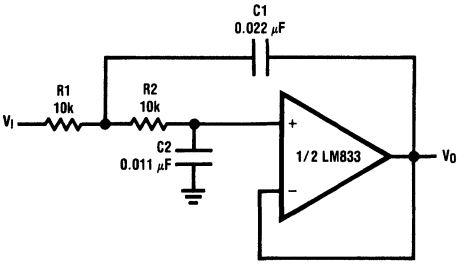
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Second Order Low Pass Filter (Butterworth)



TL/H/5218-36

if R1 = R2 = R

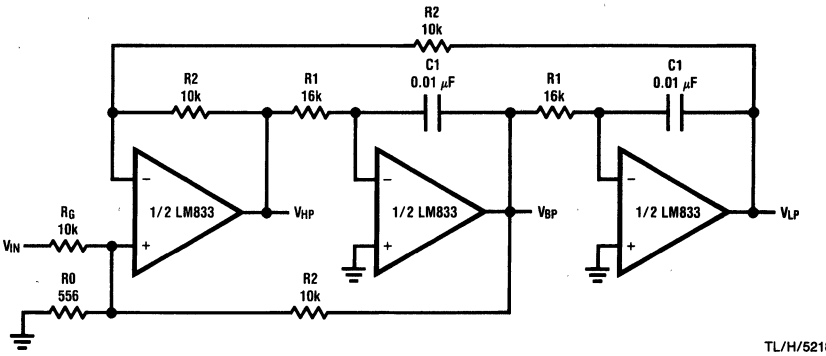
$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Typical Applications (Continued)

State Variable Filter

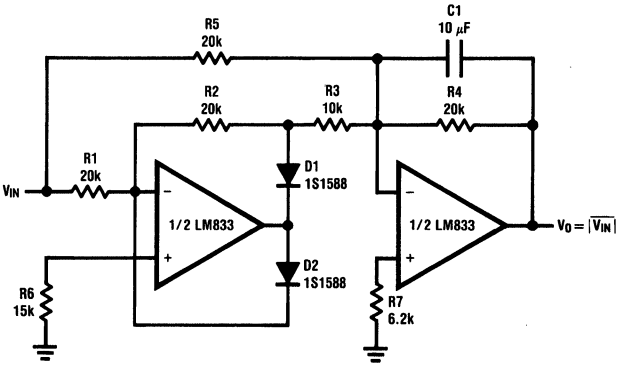


TL/H/5218–37

$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

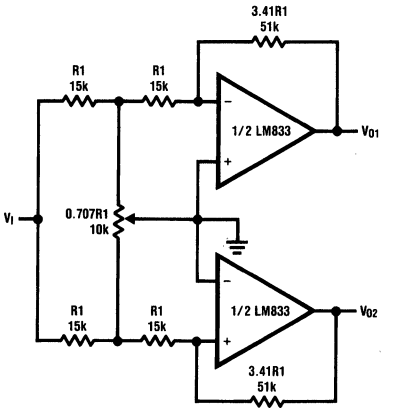
Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

AC/DC Converter



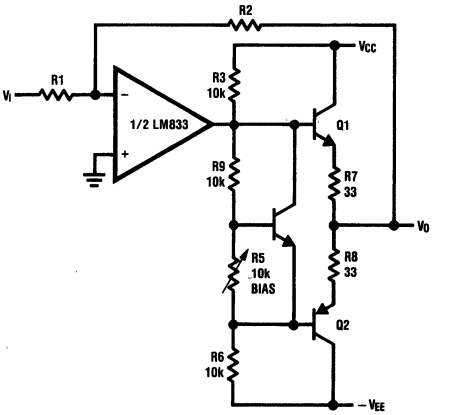
TL/H/5218–38

2 Channel Panning Circuit (Pan Pot)



TL/H/5218–39

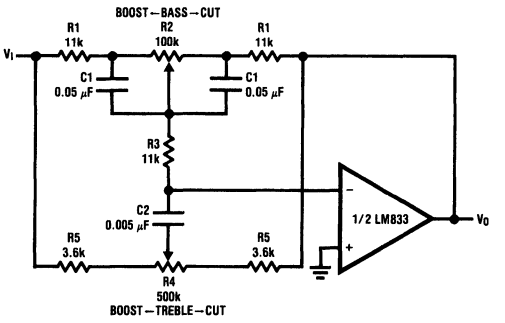
Line Driver



TL/H/5218–40

Typical Application (Continued)

Tone Control



TL/H/5218–41

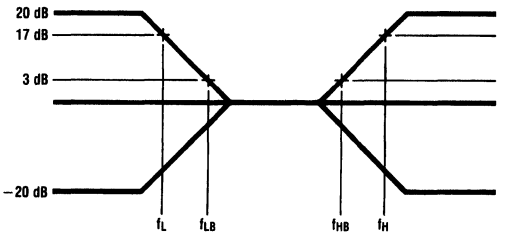
$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2},\ f_{HB} = \frac{1}{2\pi(R1 + R5 + 2R3)C2}$$

Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H = 11 kHz, f_{HB} = 1.1 kHz



TL/H/5218–42

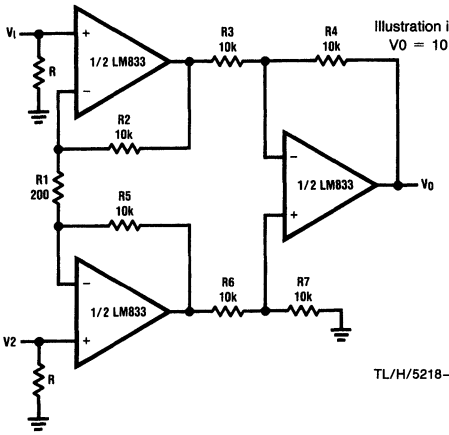
Balanced Input Mic Amp

If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

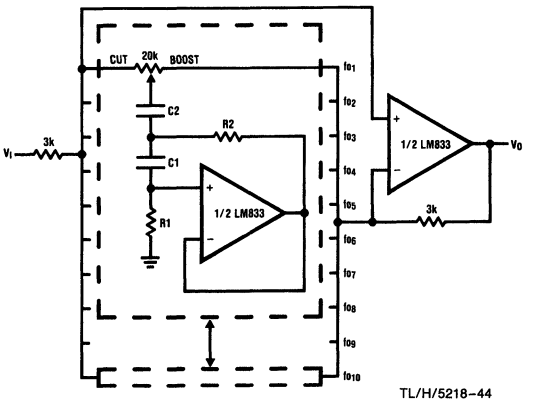
Illustration is:

V0 = 101(V2 − V1)



TL/H/5218–43

10 Band Graphic Equalizer



TL/H/5218–44

fo(Hz)	C_1	C_2	R_1	R_2
32	0.12µF	4.7µF	75kΩ	500Ω
64	0.056µF	3.3µF	68kΩ	510Ω
125	0.033µF	1.5µF	62kΩ	510Ω
250	0.015µF	0.82µF	68kΩ	470Ω
500	8200pF	0.39µF	62kΩ	470Ω
1k	3900pF	0.22µF	68kΩ	470Ω
2k	2000pF	0.1µF	68kΩ	470Ω
4k	1100pF	0.056µF	62kΩ	470Ω
8k	510pF	0.022µF	68kΩ	510Ω
16k	330pF	0.012µF	51kΩ	510Ω

At volume of change = ±12 dB

Q = 1.7

Reference: "AUDIO/RADIO HANDBOOK", National Semiconductor, 1980, Page 2–61

National Semiconductor

LM837 Low Noise Quad Operational Amplifier

General Description

The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

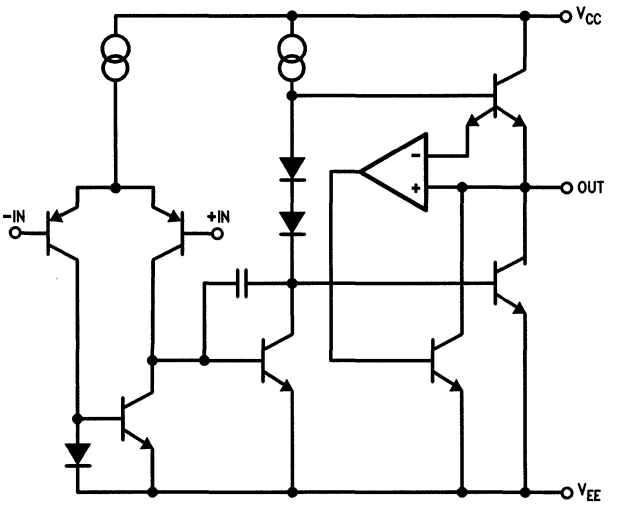
The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and can therefore be used to upgrade existing systems with little or no change.

Features

■ High slew rate	10 V/μs (typ)
	8 V/μs (min)
■ Wide gain bandwidth product	25 MHz (typ)
	15 MHz (min)
■ Power bandwidth	200 kHz (typ)
■ High output current	±40 mA
■ Excellent output drive performance	>600Ω
■ Low input noise voltage	4.5 nV/√Hz
■ Low total harmonic distortion	0.0015%
■ Low offset voltage	0.3 mV

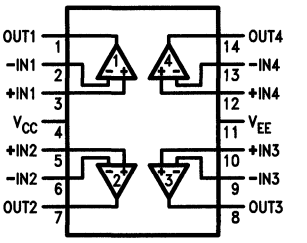
Schematic and Connection Diagrams

1/4 Quad



TL/H/9047–1

Dual-In-Line Package



TL/H/9047–2

Top View

Order Number LM837M or LM837N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	V_{CC}/V_{EE}	±18V
Differential Input Voltage (Note 1)	V_{ID}	±30V
Common Mode Input Voltage (Note 1)	V_{IC}	±15V
Power Dissipation (Note 2)	P_D	1.2W (N) 830 mW (M)
Operating Temperature Range	T_{OPR}	−40°C to +85°C
Storage Temperature Range	T_{STG}	−60°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Large Signal Voltage Gain	$R_L = 2 k\Omega, V_{OUT} = \pm 10V$	90	110		dB
V_{OM}	Output Voltage Swing	$R_L = 2 k\Omega$	±12	±13.5		V
		$R_L = 600\Omega$	±10	±12.5		V
V_{CM}	Common Mode Input Voltage		±12	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{IN} = \pm 12V$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 15 \sim 5, -15 \sim -5$	80	100		dB
I_S	Power Supply Current	$R_L = \infty$, Four Amps		10	15	mA

AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
SR	Slew Rate	$R_L = 600\Omega$	8	10		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz, $R_L = 600\Omega$	15	25		MHz

Design Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$ (Note 3)

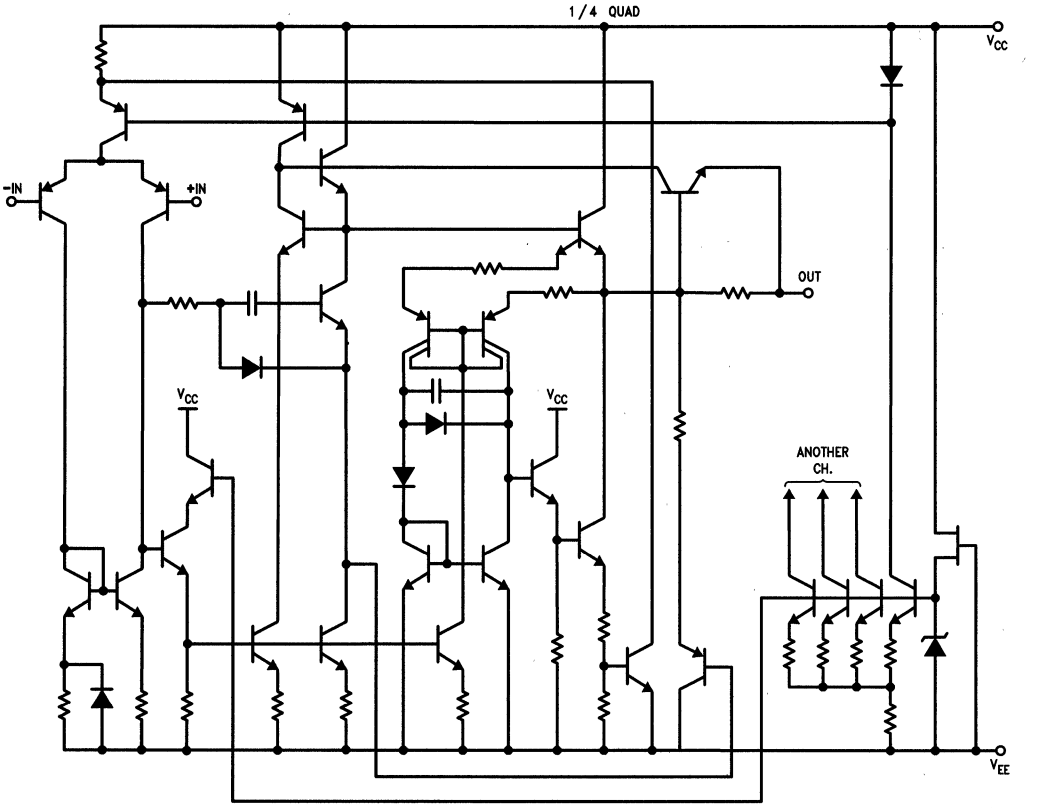
Symbol	Parameter	Condition	Min	Typ	Max	Units
PBW	Power Bandwidth	$V_O = 25 V_{P-P}, R_L = 600\Omega$, THD < 1%		200		kHz
e_{n1}	Equivalent Input Noise Voltage	JIS A, $R_S = 100\Omega$		0.5		μV
e_{n2}	Equivalent Input Noise Voltage	f = 1 kHz		4.5		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 1 kHz		0.7		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	$A_V = 1, V_{OUT} = 3$ Vrms, f = 20 ~ 20 kHz, $R_L = 600\Omega$		0.0015		%
f_U	Zero Cross Frequency	Open Loop		12		MHz
ϕ_m	Phase Margin	Open Loop		45		deg
	Input-Referred Crosstalk	f = 20 ~ 20 kHz		−120		dB
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage			2		μV/°C

Note 1: Unless otherwise specified the absolute maximum input voltage is equal to the power supply voltage.

Note 2: For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM837N, 90°C/W; LM837M, 150°C/W.

Note 3: The following parameters are not tested or guaranteed.

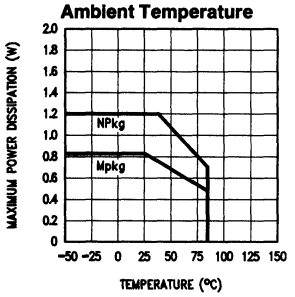
Detailed Schematic



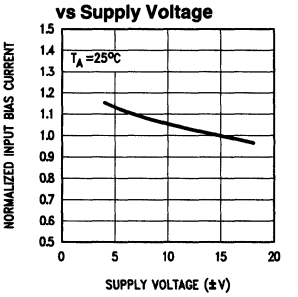
TL/H/9047–3

Typical Performance Characteristics

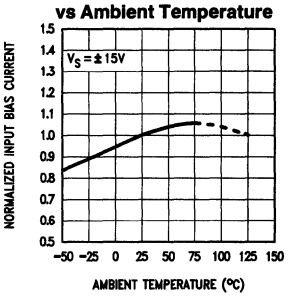
Maximum Power Dissipation vs Ambient Temperature



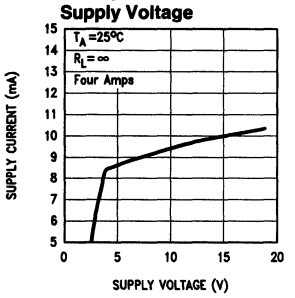
Normalized Input Bias Current vs Supply Voltage



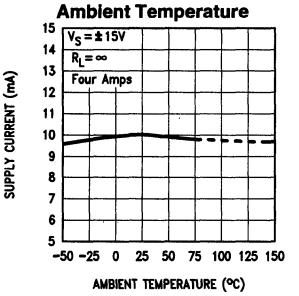
Normalized Input Bias Current vs Ambient Temperature



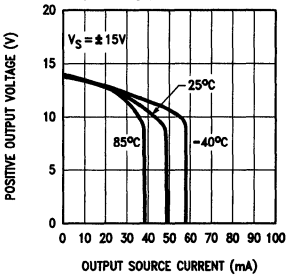
Supply Current vs Supply Voltage



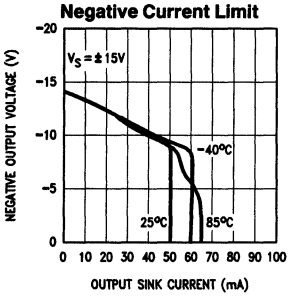
Supply Current vs Ambient Temperature



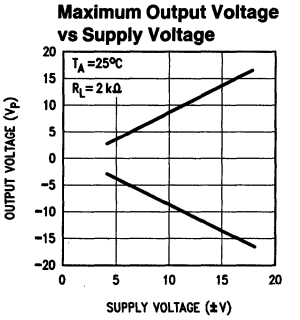
Positive Current Limit



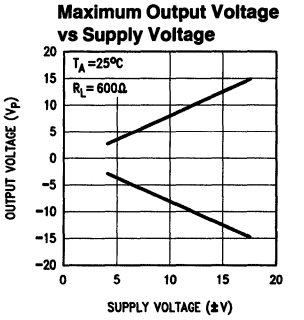
Negative Current Limit



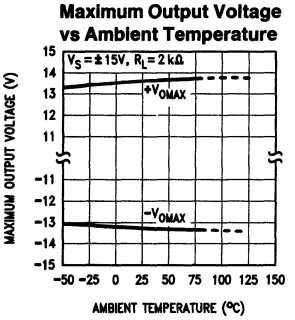
Maximum Output Voltage vs Supply Voltage



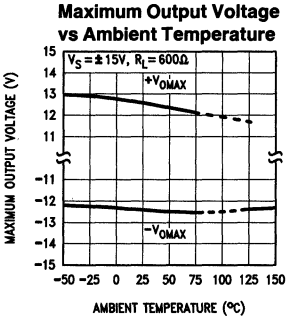
Maximum Output Voltage vs Supply Voltage



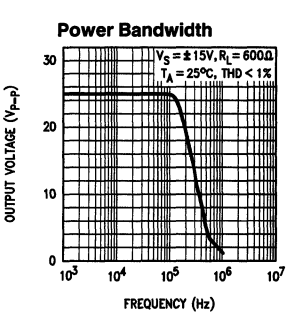
Maximum Output Voltage vs Ambient Temperature



Maximum Output Voltage vs Ambient Temperature



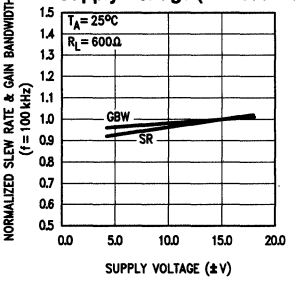
Power Bandwidth



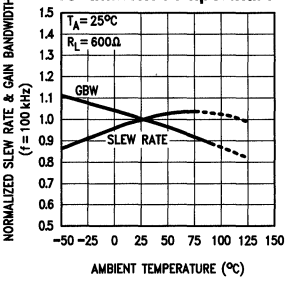
TL/H/9047–4

Typical Performance Characteristics (Continued)

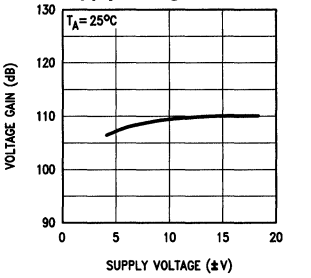
Normalized Slew Rate & Gain Bandwidth vs Supply Voltage (f = 100 kHz)



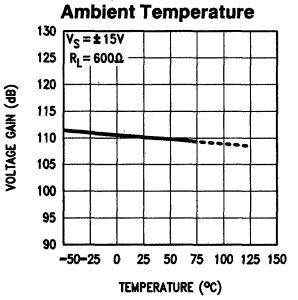
Normalized Slew Rate & Gain Bandwidth (f = 100 kHz) vs Ambient Temperature



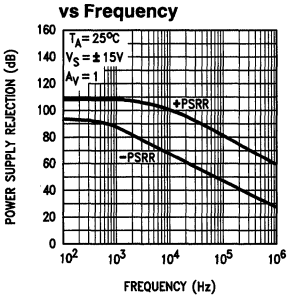
Voltage Gain vs Supply Voltage



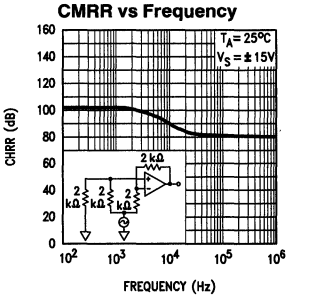
Voltage Gain vs Ambient Temperature



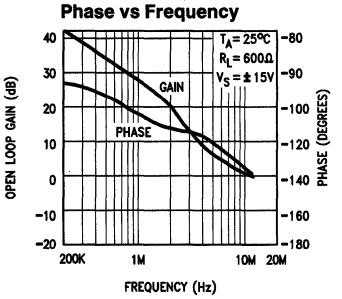
Power Supply Rejection vs Frequency



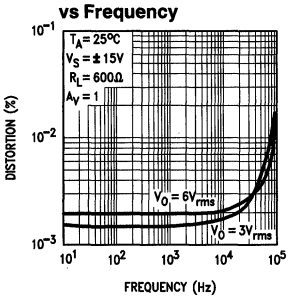
CMRR vs Frequency



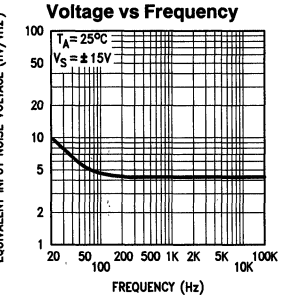
Open Loop Gain & Phase vs Frequency



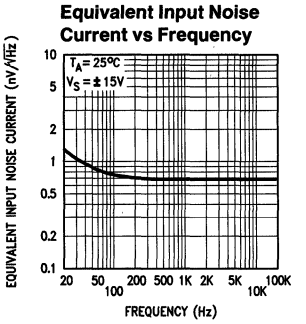
Total Harmonic Distortion vs Frequency



Equivalent Input Noise Voltage vs Frequency



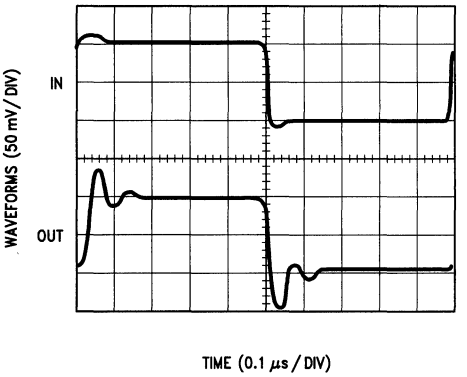
Equivalent Input Noise Current vs Frequency



TL/H/9047–5

Typical Performance Characteristics (Continued)

Small Signal, Non-Inverting
$T_A = 25°C, A_V = 1, R_L = 600\Omega, V_S = \pm 15V$



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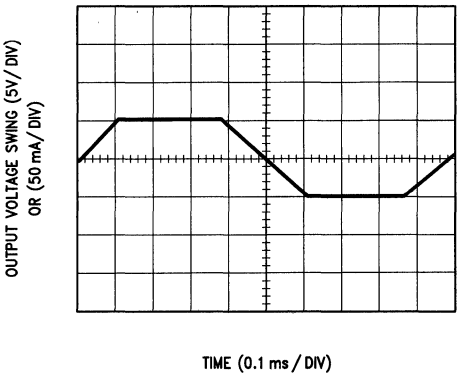
Current Limit
$T_A = 25°C, V_S = \pm 15V, R_L = 100\Omega, A_V = 1$



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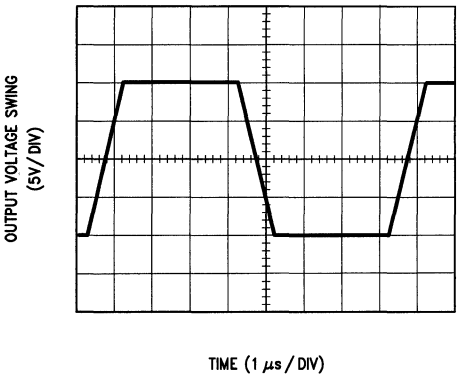
Large Signal Non-Inverting
$T_A = 25°C, R_L = 600\Omega, V_S = \pm 15V$



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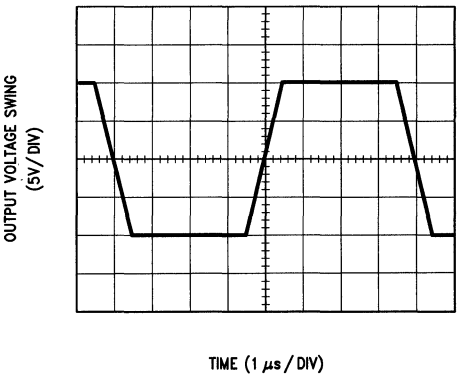
Large Signal Inverting
$T_A = 25°C, R_L = 600\Omega, V_S = \pm 15V$



TL/H/9047-9

National Semiconductor

LM1035/LM1036 Dual DC Operated Tone/Volume/Balance Circuits

General Description

The LM1035/LM1036 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

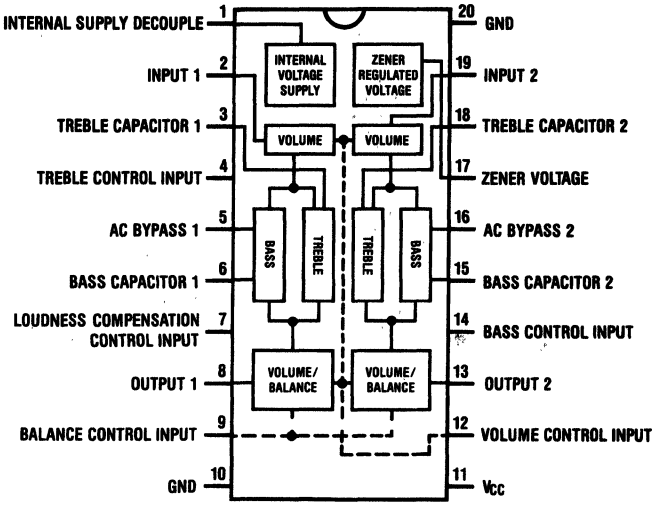
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 8V to 18V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 1 Vrms (0.3 Vrms for LM1036)
- High signal to noise, 80 dB typical for an input level of 1 Vrms (0.3 Vrms for LM1036)
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5142–1

Order Number LM1035N or LM1036N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- LM1036 16V
- LM1035 20V

Control Pin Voltage (Pins 4, 7, 9, 12, 14) V_{CC}

Operating Temperature Range 0°C to +70°C
Storage Temperature Range −65°C to +150°C
Power Dissipation 1W
Lead Temp. (Soldering, 10 seconds) 260°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions		Min	Typ	Max	Units
Supply Voltage Range	Pin 11	LM1036	9		16	V
		LM1035	8		18	V
Supply Current				35	45	mA
Zener Regulated Output Voltage Current	Pin 17			 5.4	 5	 V mA
Maximum Output Voltage LM1036	Pins 8, 13; f=1 kHz $V_{CC}=9V$, Maximum Gain $V_{CC}=12V$		 0.8	 0.8 1.0	 	 Vrms Vrms
Maximum Output Voltage LM1035	Pins 8, 13; f=1 kHz $V_{CC}=8V$ $V_{CC}=12V$ $V_{CC}=18V$		 2	 1.3 2.5 3.5	 	 Vrms Vrms Vrms
Maximum Input Voltage LM1036 (Note 1)	Pins 2, 19; f=1 kHz, $V_{CC}=9V$ Flat Response, $V_{CC}=12V$ Gain=−10 dB		 1.3	1.1 1.6		Vrms Vrms
Maximum Input Voltage LM1035 (Note 1)	Pins 2, 19; f=1 kHz Flat Response		2	2.5		Vrms
Input Resistance	Pins 2, 19; f=1 kHz		20	30		kΩ
Output Resistance	Pins 8, 13;f=1 kHz			20		Ω
Maximum Gain	V(Pin 12)=V(Pin 17); f=1 kHz		−2	0	2	dB
Volume Control Range	f=1 kHz	LM1036	70	75		dB
		LM1035	70	80		dB
Gain Tracking Channel 1−Channel 2	f=1 kHz 0 dB through −40 dB −40 dB through −60 dB			 1 2	 3 	 dB dB
Balance Control Range	Pins 8, 13; f=1 kHz			1 −26	 −20	dB dB
Bass Control Range (Note 2)	f=40 Hz, $C_b=0.39\ \mu F$ V(Pin 14)=V(Pin 17) V(Pin 14)=0V		 12 −12	 15 −15	 18 −18	 dB dB
Treble Control Range (Note 2)	f= 16 kHz, $C_t=0.01\ \mu F$ V(Pin 4)=V(Pin 17) V(Pin 4)=0V		 12 −12	 15 −15	 18 −18	 dB dB
Total Harmonic Distortion LM1036	f=1 kHz, $V_{IN}=0.3$ Vrms Gain=0 dB Gain=−30 dB			 0.06 0.03	 0.3 	 % %
Total Harmonic Distortion LM1035	f=1 kHz, $V_{IN}=1$ Vrms Maximum Gain			0.05	0.2	%

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated) (Continued)

Parameter	Conditions		Min	Typ	Max	Units
Channel Separation	f = 1 kHz, Maximum Gain	LM1036	60	75		dB
		LM1035		75		dB
Signal/Noise Ratio LM1036	Unweighted 100 Hz–20 kHz Maximum Gain, 0 dB = 0.3 Vrms CCIR/ARM (Note 3)			80		dB
	Gain = 0 dB, $V_{IN}=0.3$ Vrms		75	79		dB
	Gain = −20 dB, $V_{IN}=1.0$ Vrms			72		dB
Signal/Noise Ratio LM1035	Unweighted 100 Hz–20 kHz Maximum Gain, 0 dB = 1 Vrms CCIR/ARM (Note 3)			80		dB
	Gain = 0 dB		76	80		dB
	Gain = −20 dB			64		dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)	LM1036		10	16	μV
		LM1035		25	35	μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	LM1036	35	50		dB
		LM1035		40		dB
Control Input Currents	Pins 4, 7, 9, 12, 14 (V = 0V)			−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz–16 kHz)			250		kHz

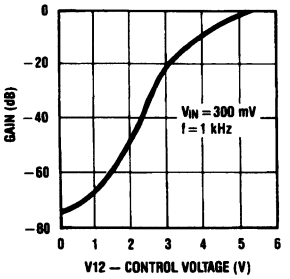
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

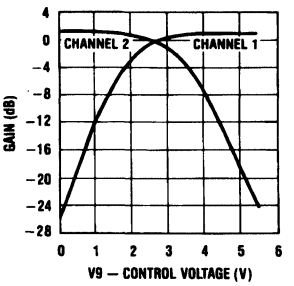
Note 3: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

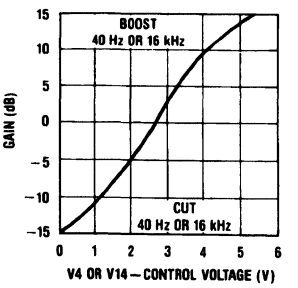
Volume Control Characteristics



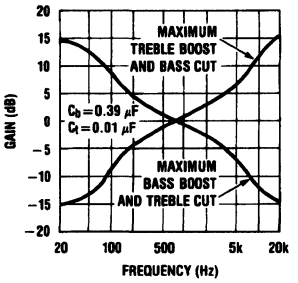
Balance Control Characteristic



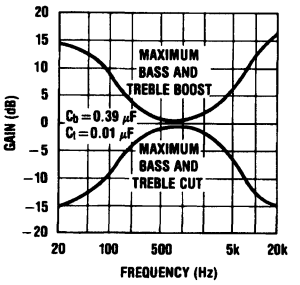
Tone Control Characteristic



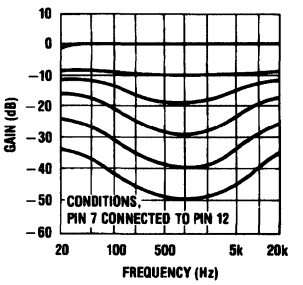
Tone Characteristic (Gain vs Frequency)



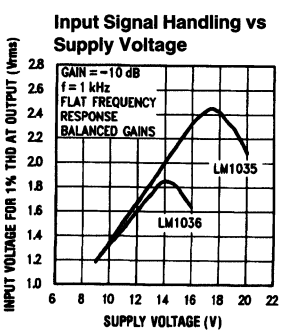
Tone Characteristic (Gain vs Frequency)



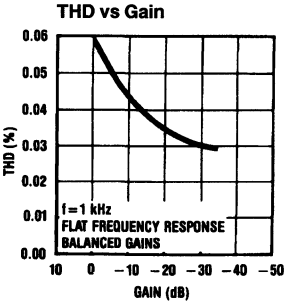
Loudness Compensated Volume Characteristic



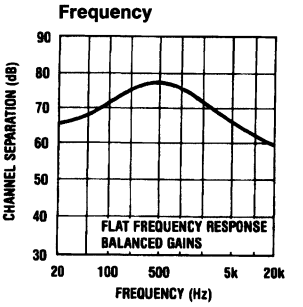
Input Signal Handling vs Supply Voltage



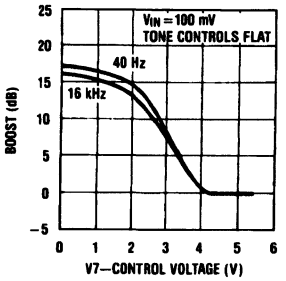
THD vs Gain



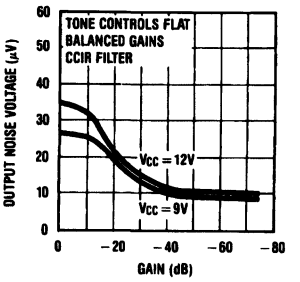
Channel Separation vs Frequency



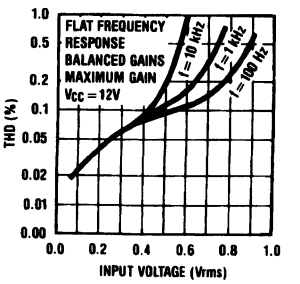
Loudness Control Characteristic



Output Noise Voltage vs Gain—LM1036



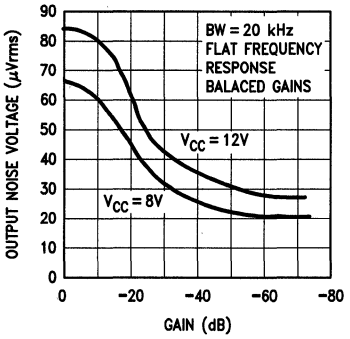
THD vs Input Voltage—LM1036



TL/H/5142–2

Typical Performance Characteristics (Continued)

Output Noise Voltage vs Gain—LM1035



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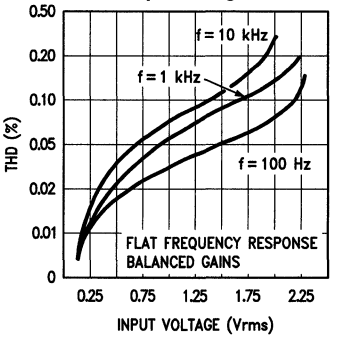
THD vs Input Voltage—LM1035



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Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1+\frac{0.00065(1-a_b)}{j\omega C_b}}{1+\frac{0.00065a_b}{j\omega C_b}}$$

$$\text{Treble Response} = \frac{1+j\omega 5500(1-a_t)C_t}{1+j\omega 5500a_tC_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

ZENER VOLTAGE

A zener voltage (pin 17 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 4, 9, and 14, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

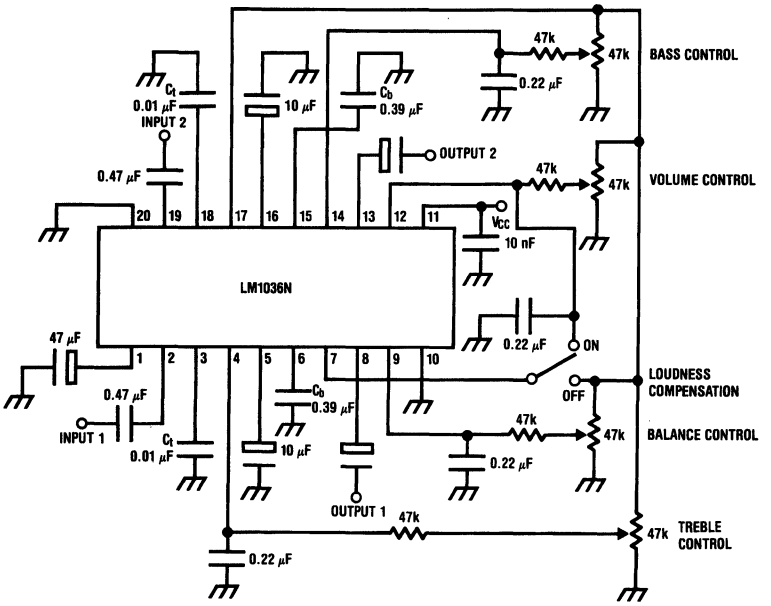
LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 7. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 7 is connected to pin 17. Pin 7 can be connected to pin 12 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 7 and 12 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1036 is carried out in two stages, controlled by the DC voltage on pin 12, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, $V_{CC} = 12V$ (0.8 Vrms, $V_{CC} = 9V$). At reduced gain (< -6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, $V_{CC} = 12V$ (1.1 Vrms, $V_{CC} = 9V$). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Application Circuit



TL/H/5142-3

Applications Information

OBTAINING MODIFIED RESPONSE CURVES

The LM1036 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1036 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

Figure 1 shows the typical tone response obtained in the standard application circuit. (C_t=0.01 μF, C_b=0.39 μF). Response curves are given for various amounts of boost and cut.

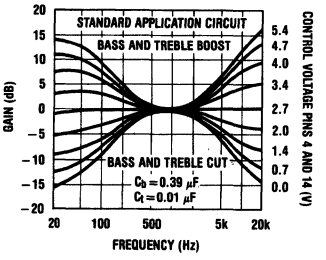


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FIGURE 1. Tone Characteristic (Gain vs Frequency)

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, $C_b/2$ and $4C_t$, $C_b/4$ respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.

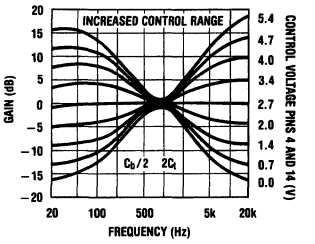

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FIGURE 2. Tone Characteristic (Gain vs Frequency)

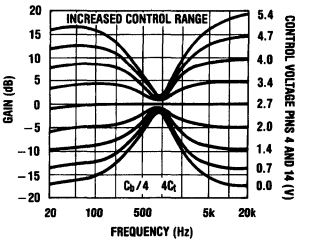

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FIGURE 3. Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5*.

Restriction of Tone Control Action at High or Low Frequencies

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequence noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 5 (channel 1) and 16 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6*. The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

Other Advantages of DC Controls

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition, to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

The loudness control is achieved through control of the tone sections by the voltage applied to pin 7; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz–16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).

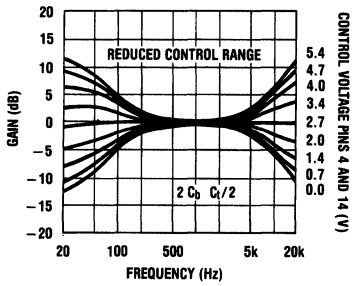

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FIGURE 4. Tone Characteristic (Gain vs Frequency)

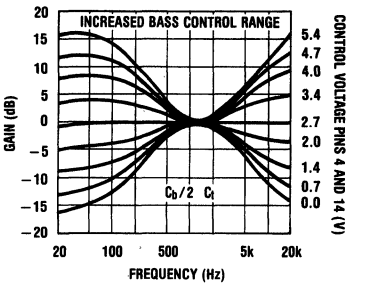

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FIGURE 5. Tone Characteristic (Gain vs Frequency)

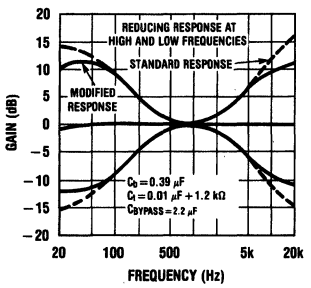

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FIGURE 6. Tone Characteristic (Gain vs Frequency)

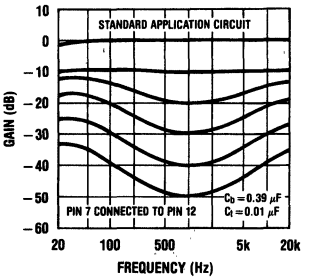

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FIGURE 7. Loudness Compensated Volume Characteristic

Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3*.

With pins 7 (loudness) and 12 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 7 towards the control reference voltage (pin 17). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 7 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12*, With a suitable level shifting network between pins 12 and 7, the onset of loudness control and its rate of change may be readily modified.

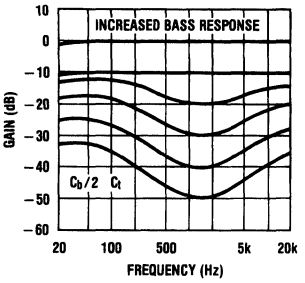

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FIGURE 8. Loudness Compensated Volume Characteristic

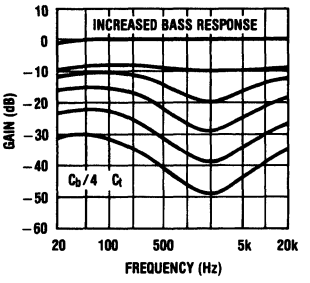

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FIGURE 9. Loudness Compensated Volume Characteristic

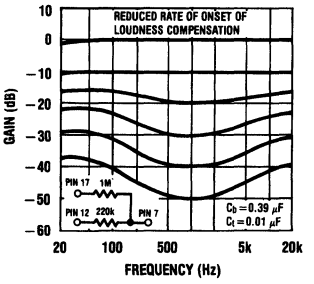

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FIGURE 10. Loudness Compensated Volume Characteristic

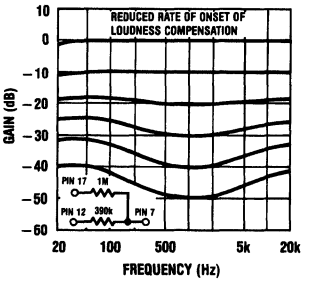

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FIGURE 11. Loudness Compensated Volume Characteristic

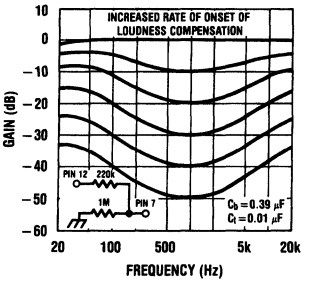

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FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM1036 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13*. The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

USE OF THE LM1036 ABOVE AUDIO FREQUENCIES

The LM1036 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.

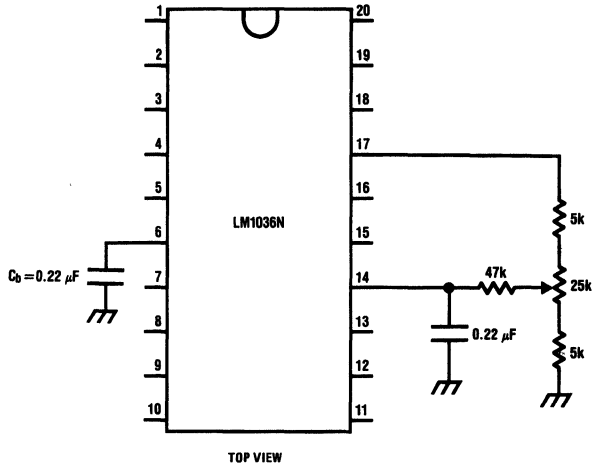

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FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control

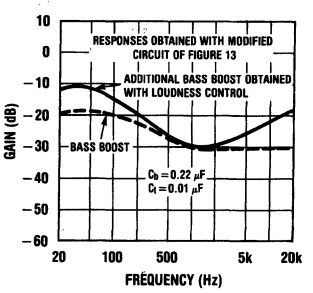

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FIGURE 14. Loudness Compensated Volume Characteristic

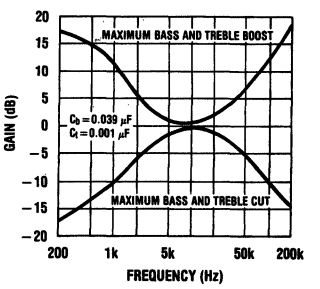

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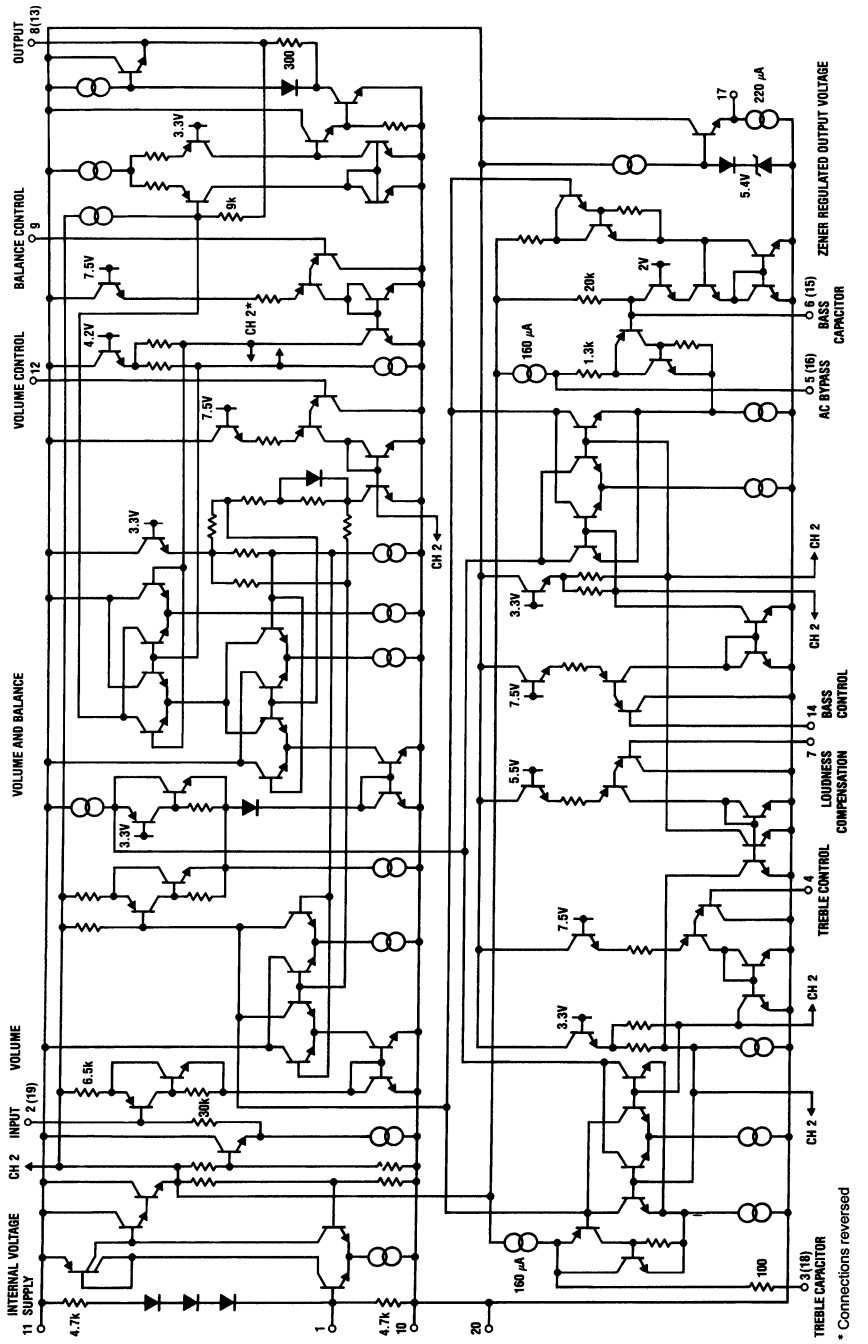
FIGURE 15. Tone Characteristic (Gain vs Frequency)

Simplified Schematic Diagram (One Channel)



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National Semiconductor

LM1037 Dual Four-Channel Analog Switch

General Description

The LM1037 is a dual, electronically controlled, analog switch with an internal muting facility. Any one of four stereo signal sources may be selected by means of four control inputs.

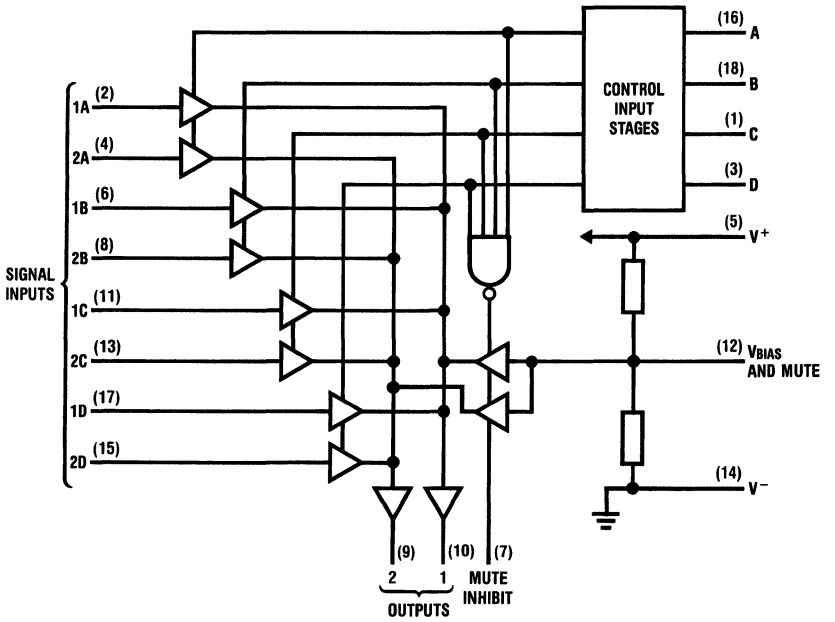
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

An additional pin is included to allow parallel connection of two or more integrated circuits.

Features

- Wide supply voltage range, 5V–28V
- Low distortion, 0.04% typical
- Low noise, typically 5 μV
- High input impedance
- Low output impedance
- TTL compatible control inputs
- Very low control current

Block Diagram



TL/H/5199–1

Order Package Number LM1037N
See NS Package N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

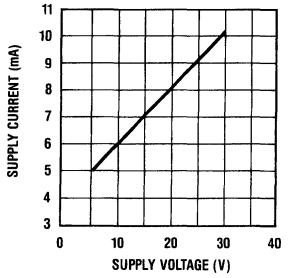
Supply Voltage	28V
Pin 7 Input Current	5 mA
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	1.3W
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$

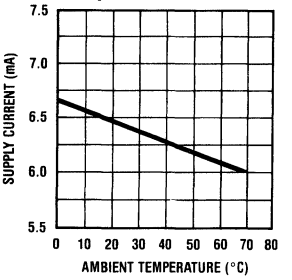
Parameter	Conditions	Typical	Tested Limit (Note 7)	Design Limit (Note 8)	Units (Limits)
Supply Voltage			28		$V_{(max)}$
Supply Voltage				5	$V_{(min)}$
Supply Current	$V_{SUPPLY} = 12V$	6.4	8.5		$mA_{(max)}$
	$V_{SUPPLY} = 28V$	10	14		$mA_{(max)}$
Voltage Gain		0	±0.7		dB
Signal Handling (Notes 2, 6)	$V_{SUPPLY} = 12V$	3.0	2.8		$Vrms_{(min)}$
Small-Signal Bandwidth		300			kHz
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	0.04	0.1		$\%_{(max)}$
Noise Voltage at Output (Note 3)	CCIR/ARM $R_S = 0\Omega$	5		20	$\mu V_{(max)}$
Channel Separation (Note 4)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−95		−70	$dB_{(min)}$
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−90	−70		$dB_{(min)}$
Output Impedance		10			Ω
Signal Input Impedance		30			MΩ
Logic Low Input Level				0.8	$V_{(max)}$
Logic High Input Level				2.0	$V_{(min)}$
Logic High Input Level				V_{SUPPLY}	$V_{(max)}$

Typical Performance Characteristics ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

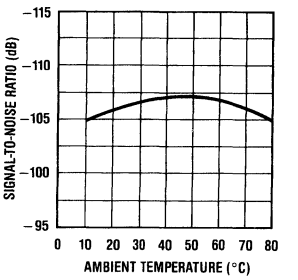
Supply Current vs Supply Voltage



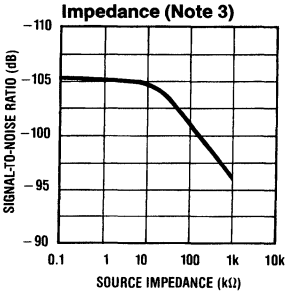
Supply Current vs Temperature



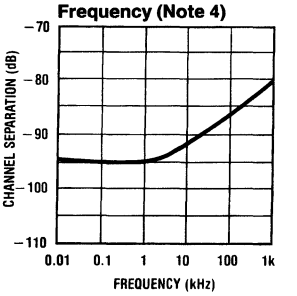
Signal-to-Noise vs Temperature (Note 3)



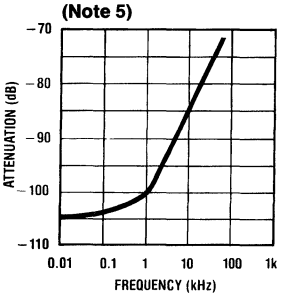
Signal-to-Noise vs Source Impedance (Note 3)



Channel Separation vs Frequency (Note 4)



Attenuation of Unselected Inputs vs Frequency (Note 5)



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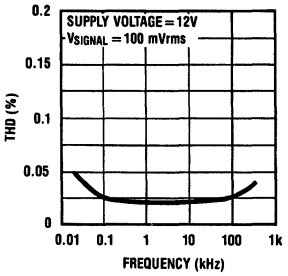
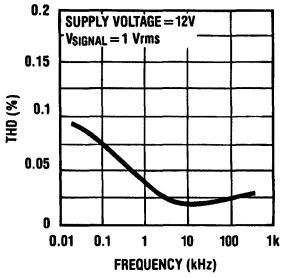
Typical Performance Characteristics (Continued) (V_S = 12V, T_A = 25°C unless otherwise noted)

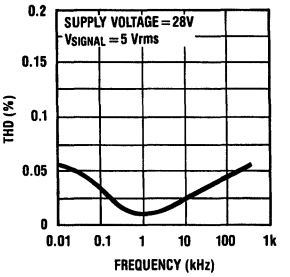
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



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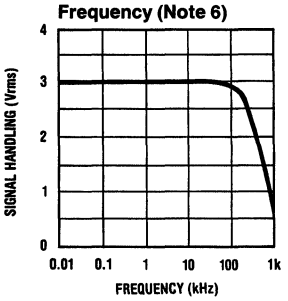
Signal Handling vs Frequency (Note 6)



TL/H/5199–4

Note 1: Above T_A = 25°C derate based on T_J max = 150°C and θ_{JA} = 90°C/W.

Note 2: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

Note 3: Gaussian noise, monitored over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz, and an average-responding meter. Signal to noise ratios are referenced to 1V rms input signal.

Note 4: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

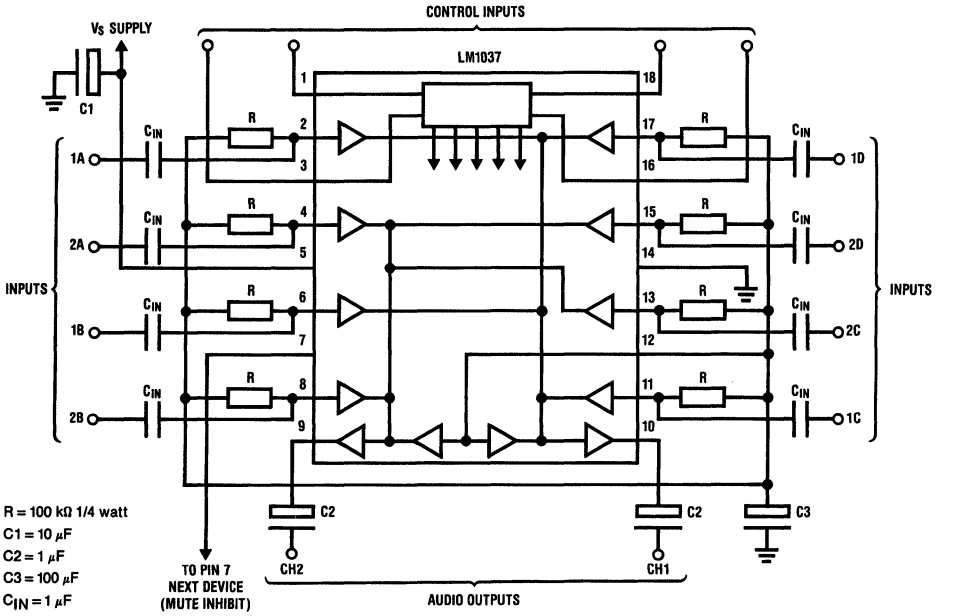
Note 5: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 6: Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Application



TL/H/5199–5

Truth Tables

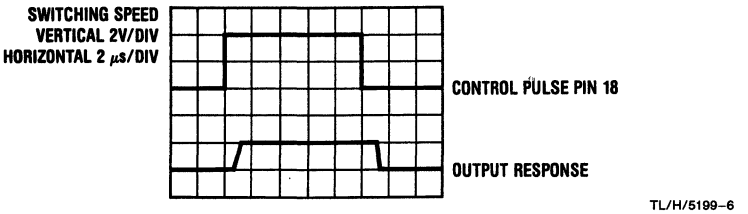
LM1037

Channel selection is achieved by the application of DC voltages to the control pins. Unselected control pins should be held low.

DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10, 9)	
16	A	(2,4)
18	B	(6,8)
1	C	(11,13)
3	D	(17,15)
None	Mute	(12)

Low switching level (V_L) < 0.8V

High switching level (V_H) > 2.0V and up to V_{SUPPLY}



TL/H/5199–6

2 DEVICES CONNECTED IN PARALLEL

To increase the channel switching capacity, two or more devices can be connected together by the direct coupling of the mute inhibit pin 7 and the output pins 9 and 10. Only one output capacitor is required for each common output.

	DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10,9)	
Device Number 1	16	A	(2,4)
	18	B	(6,8)
	1	C	(11,13)
	3	D	(17,15)
Device Number 2	16	A	(2,4)
	18	B	(6,8)
	1	C	(11,13)
	3	D	(17,15)
	None	Mute	(12)

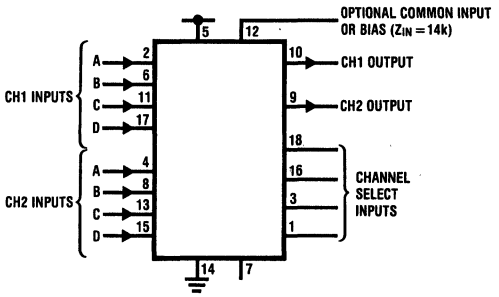
Pin Function Description

Device Pins	Description
Pin 16—Inputs A Select Pin 18—Inputs B Select Pin 1—Inputs C Select Pin 3—Inputs D Select	A high input level selects the corresponding channel. Only one channel should be selected at a time. Unselected channels should have their select inputs at a low level. Open circuit pins represent a high input level.
Pins 2, 6, 11, 17— Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15— Inputs for Output 2 (Pin 9)	Two sets of four high impedance channel inputs for the connection of signals to be switched.
Pin 12—Mute Bias Level	The DC level at this pin is applied to the outputs when no input is selected and pin 7 is open. The level is internally set by a 25 kΩ and 33 kΩ potential divider at 0.6 V_S. This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common input in which case this signal is present on both outputs when no control input is applied.
Pin 7—Mute Inhibit Input	With this pin unconnected and no channel selection input is present; the mute level at pin 12 is applied to the outputs. With pin 7 grounded and no channel selection input present, the device output emitter-followers are disabled allowing parallel connection to other device outputs. This pin is a current input and any current applied should be limited to 5 mA maximum. Pin 7 of several devices may be directly connected for parallel operation.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 kΩ pull-down resistors to ground.
Pin 5	Positive supply voltage.
Pin 14	Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

For switching between signal sources in stereo systems the LM1037 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.



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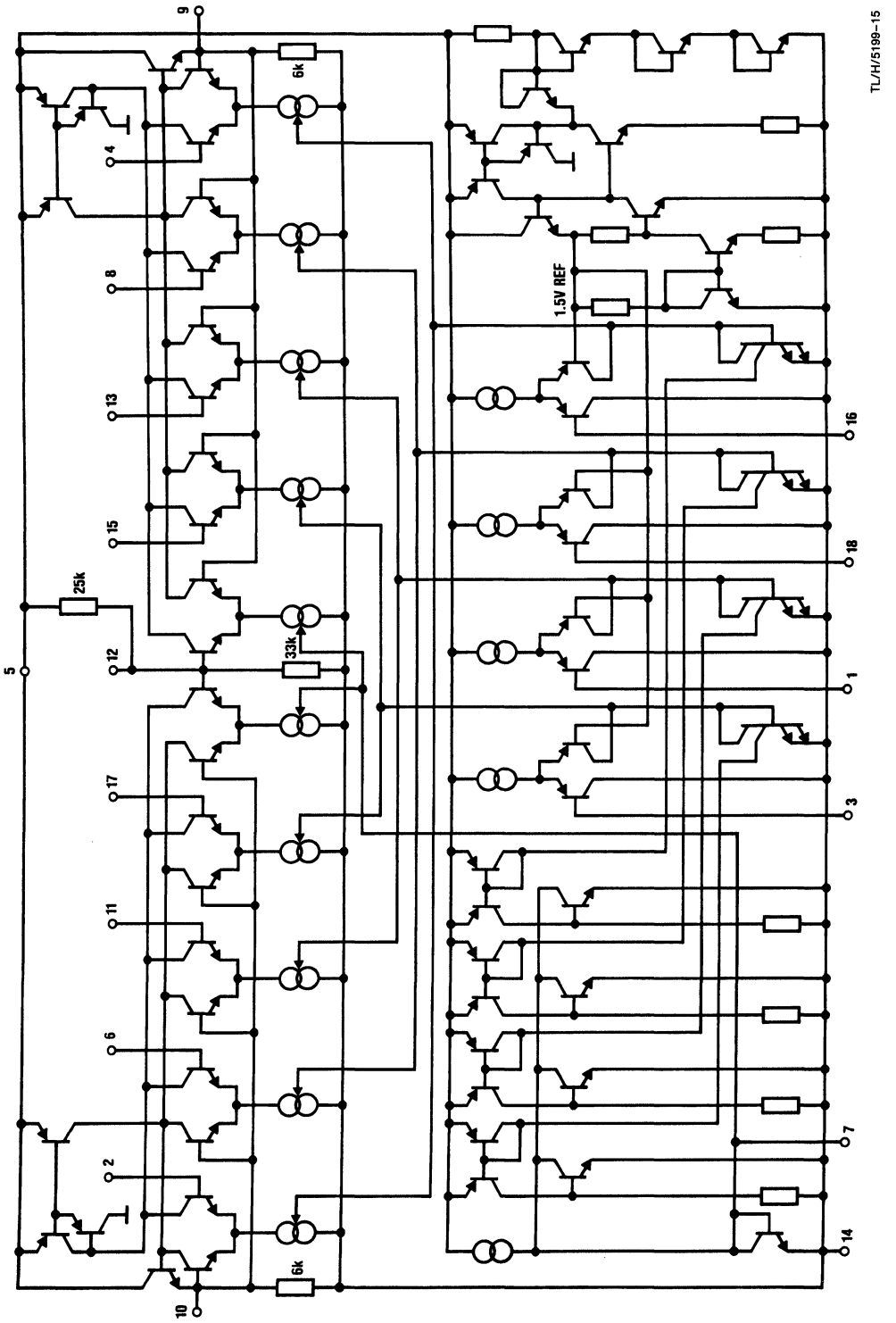
DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Simplified Circuit Schematic (All signal and control inputs are Darlington connected)



TL/H/5199–15

National Semiconductor

LM1040 Dual DC Operated Tone/Volume/Balance Circuit with Stereo Enhancement Facility

General Description

The LM1040 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. A stereo enhancement facility is included whereby the apparent stereo separation of systems requiring closely spaced speakers may be improved. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

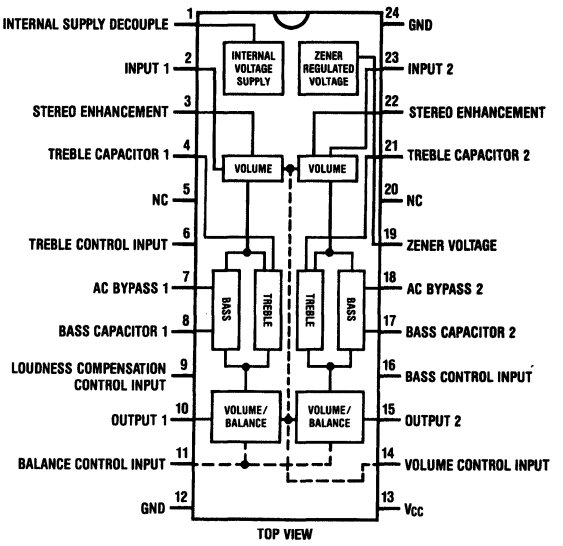
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagrams

Dual-in-Line Package



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Order Number LM1040N
See NS Package Number N24A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	16V
Control Pin Voltage (Pins 6, 9, 11, 14, 16)	V_{CC}
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	Pin 13	9		16	V
Supply Current			35	45	mA
Zener Regulated Output Voltage Current	Pin 19		 5.4	 5	 V mA
Maximum Output Voltage	Pins 10, 15; f=1 kHz V_{CC}=9V, Maximum Gain V_{CC}=12V	 0.8	 0.8 1.0		 Vrms Vrms
Maximum Input Voltage (Note 1)	Pins 2, 23; f=1 kHz, V_{CC}=9V Flat Response, V_{CC}=12V Gain=−10 dB	 1.3	 1.1 1.6		 Vrms Vrms
Input Resistance	Pins 2, 23; f=1 kHz	20	30		kΩ
Output Resistance	Pins 10, 15; f=1 kHz		20		Ω
Maximum Gain	V(Pin 14)= V(Pin 19); f=1 kHz	−2	0	2	dB
Volume Control Range	f=1 kHz	70	75		dB
Gain Tracking Channel 1-Channel 2	f=1 kHz 0 dB through −40 dB −40 dB through −60 dB	 	 1 2	 3 	 dB dB
Balance Control Range	Pins 10, 15; f=1 kHz		1 −26	 −20	dB dB
Bass Control Range (Note 2)	f=40 Hz, C_b=0.39 μF V(Pin 16)=V(Pin 19) V(Pin 16)=0V	 12 −12	 15 −15	 18 −18	 dB dB
Treble Control Range (Note 2)	f=16 kHz, C_t=0.01 μF V(Pin 6)=V(Pin 19) V(Pin 6)=0V	 12 −12	 15 −15	 18 −18	 dB dB
Total Harmonic Distortion	f=1 kHz, V_{IN}=0.3 Vrms Gain=0 dB Gain=−30 dB	 	 0.06 0.03	 0.3 	 % %
Channel Separation	f=1 kHz, Maximum Gain	60	75		dB
Signal/Noise Ratio	Unweighted 100 Hz-20 kHz Maximum Gain, 0 dB=0.3 Vrms CCIR/ARM (Note 3) Gain=0 dB, V_{IN}=0.3 Vrms Gain=−20 dB, V_{IN}=1.0 Vrms	 75 	80 79 72	 	dB dB dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)		10		μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	35	−50		dB
Control Input Currents	Pins 6, 9, 11, 14, 16 (V=0V)		−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz−16 kHz)		250		kHz

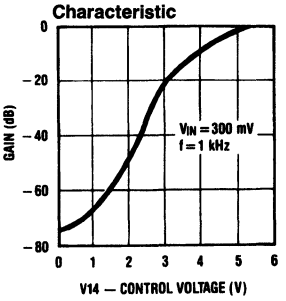
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

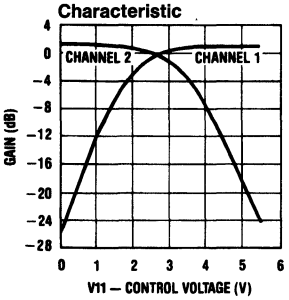
Note 3: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

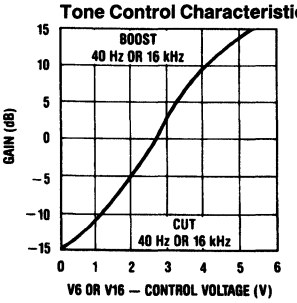
Volume Control Characteristic



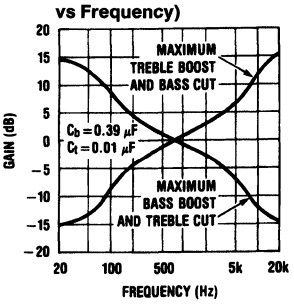
Balance Control Characteristic



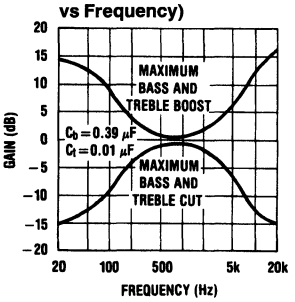
Tone Control Characteristic



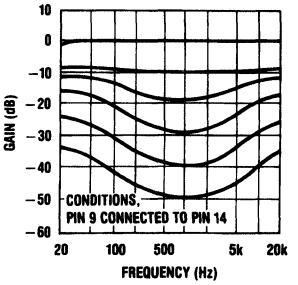
Tone Characteristic (Gain vs Frequency)



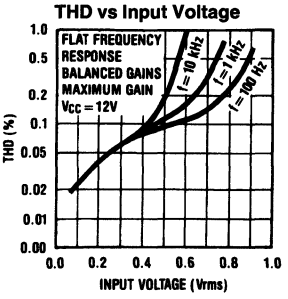
Tone Characteristic (Gain vs Frequency)



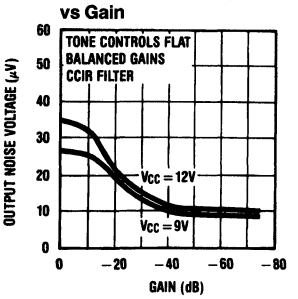
Loudness Compensated Volume Characteristic



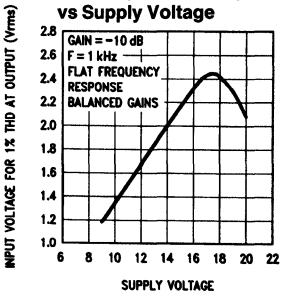
THD vs Input Voltage



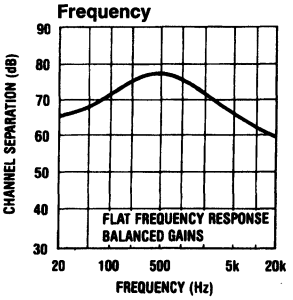
Output Noise Voltage vs Gain



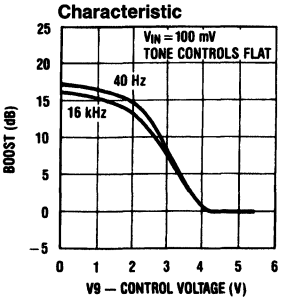
Input Signal Handling vs Supply Voltage



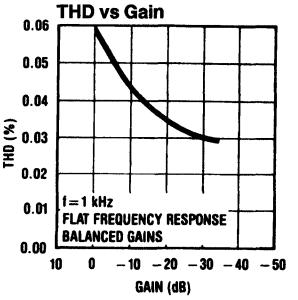
Channel Separation vs Frequency



Loudness Control Characteristic



THD vs Gain



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Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1 + \dfrac{0.00065(1 - a_b)}{j\omega C_b}}{1 + \dfrac{0.00065a_b}{j\omega C_b}}$$

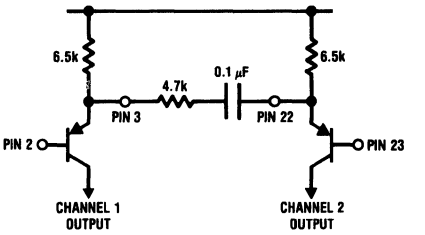
$$\text{Treble Response} = \frac{1 + j\omega 5500(1 - a_t)C_t}{1 + j\omega 5500a_tC_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

STEREO ENHANCEMENT

When stereo system speakers need to be closer than optimum because of equipment/cabinet limitations, an improved stereo effect can be obtained using a modest amount of phase—reversed interchannel cross-coupling. In the LM1040 the input stage transistor emitters are brought out to facilitate this. The arrangement is shown below in basic form.



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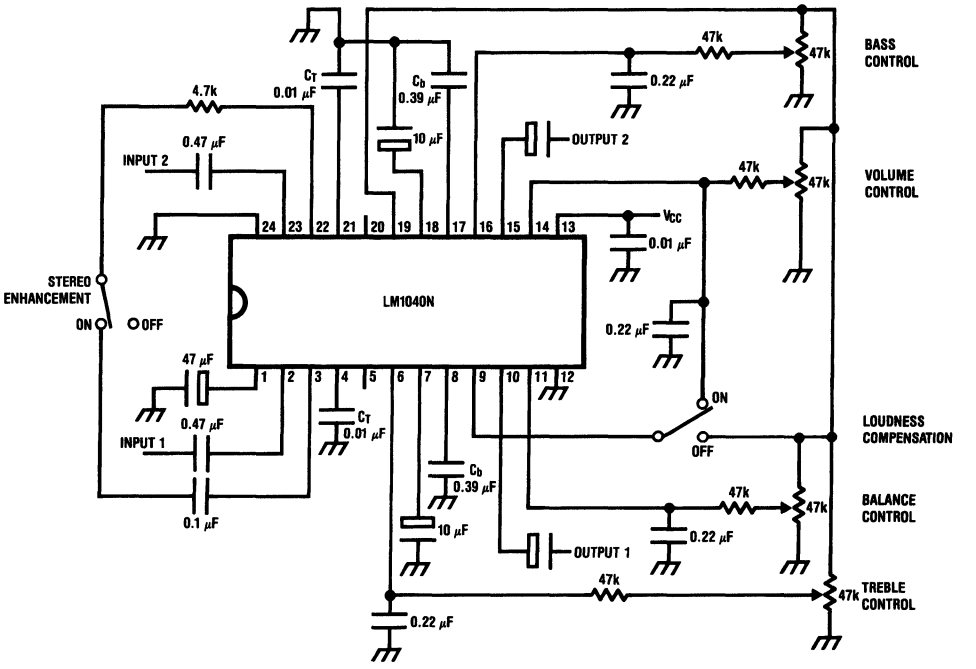
With a monophonic source, the emitters have the same signal and the resistor and capacitor connected between them have no effect. With a stereo signal each transistor works in the grounded base mode for stereo components, generating an in-phase signal from the opposite channel. As the normal signals are inverted at this point, the appropriate phase-reversed cross-coupling is achieved. An effective level of coupling of 60% can be obtained using 4.7k in conjunction with the internal 6.5k emitter resistors. At low frequencies, speakers become less directional and it becomes desirable to reduce the enhancement effect. With a 0.1 μF coupling capacitor, as shown, roll-off occurs below 330 Hz. The coupling components may be varied for alternative responses.

Application Circuit



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Application Notes (Continued)

ZENER VOLTAGE

A zener voltage (pin 19 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 6, 11, and 16, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 9. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 9 is connected to pin 19. Pin 9 can be connected to pin 14 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 9 and 14 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1040 is carried out in two stages, controlled by the DC voltage on pin 14, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, V_{CC} = 12V(0.7 Vrms, V_{CC} = 9V). At reduced gain (< −6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, V_{CC} = 12V (1.1 Vrms, V_{CC} = 9V). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Applications Information

OBTAINING MODIFIED RESPONSE CURVES

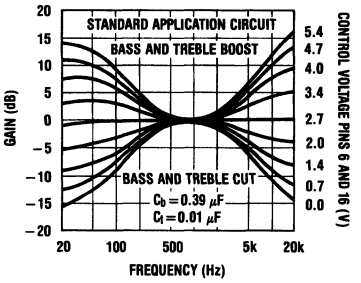
The LM1040 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1040 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

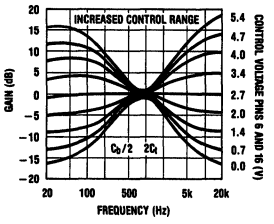
Figure 1 shows the typical tone response obtained in the standard application circuit. (C_t = 0.01 µF, C_b = 0.39 µF). Response curves are given for various amounts of boost and cut.



TL/H/5147–5

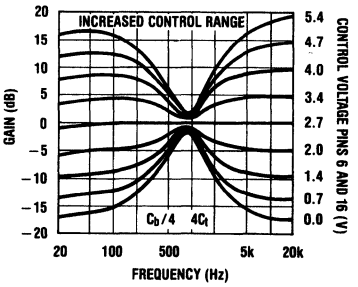
FIGURE 1. Tone Characteristic (Gain vs Frequency)

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, C_b/2 and 4C_t, C_b/4 respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.



TL/H/5147–6

FIGURE 2: Tone Characteristic (Gain vs Frequency)



TL/H/5147–7

FIGURE 3: Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5.*

RESTRICTION OF TONE CONTROL ACTION AT HIGH OR LOW FREQUENCIES

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequency noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 7 (channel 1) and 18 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6.* The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

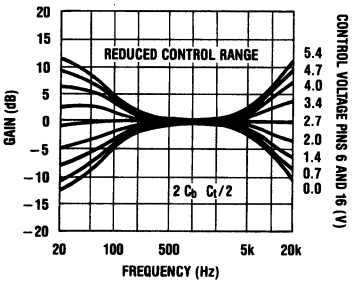
OTHER ADVANTAGES OF DC CONTROLS

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition; to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

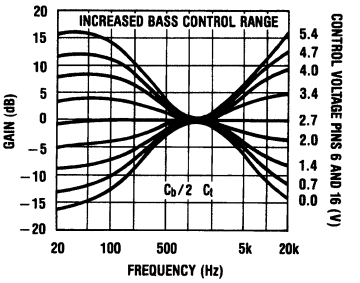
The loudness control is achieved through control of the tone sections by the voltage applied to pin 9; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz−16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).



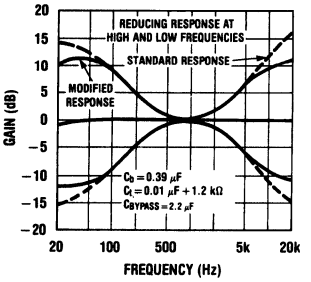
TL/H/5147–8

FIGURE 4. Tone Characteristic (Gain vs Frequency)



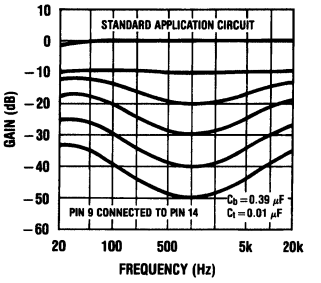
TL/H/5147–9

FIGURE 5. Tone Characteristic (Gain vs Frequency)



TL/H/5147–10

FIGURE 6. Tone Characteristic (Gain vs Frequency)



TL/H/5147–11

FIGURE 7. Loudness Compensated Volume Characteristic

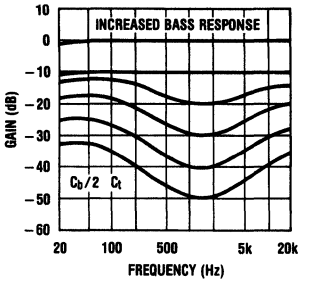
Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3*.

With pins 9 (loudness) and 14 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

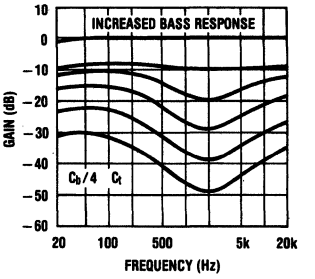
Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 9 towards the control reference voltage (pin 19). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 9 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12*. With a suitable level shifting network between pins 14 and 9, the onset of loudness control and its rate of change may be readily modified.



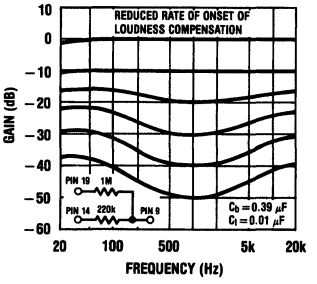
TL/H/5147–12

FIGURE 8. Loudness Compensated Volume Characteristic



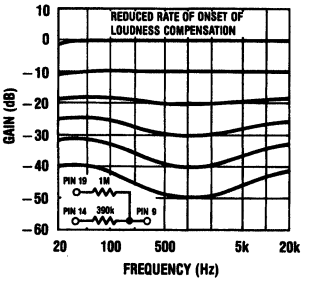
TL/H/5147–13

FIGURE 9. Loudness Compensated Volume Characteristic



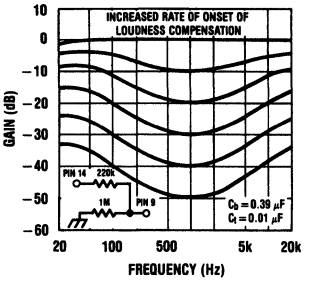
TL/H/5147–14

FIGURE 10. Loudness Compensated Volume Characteristic



TL/H/5147–15

FIGURE 11. Loudness Compensated Volume Characteristic



TL/H/5147–16

FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM-1040 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13.* The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

USE OF THE LM1040 ABOVE AUDIO FREQUENCIES

The LM1040 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.

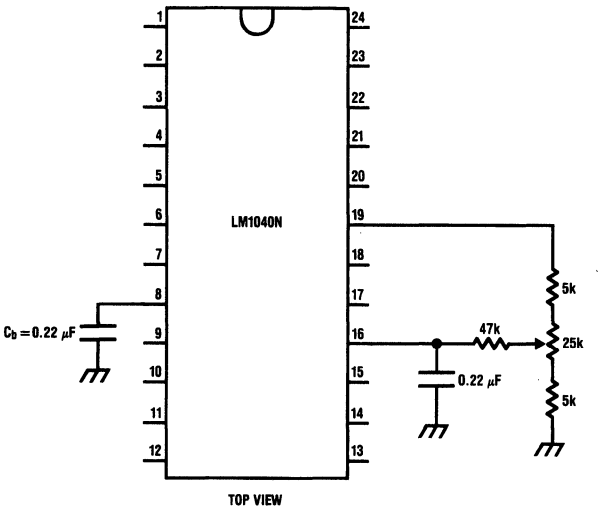


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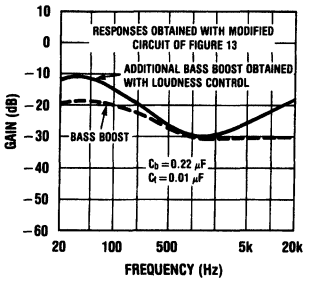
FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control



TL/H/5147–18

FIGURE 14. Loudness Compensated Volume Characteristic

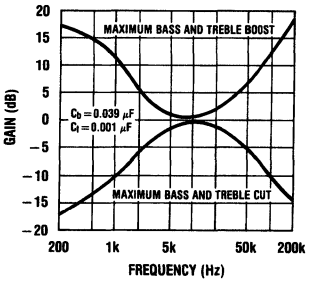


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FIGURE 15. Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

DC CONTROL OF STEREO ENHANCEMENT AND LOUDNESS CONTROL

Figure 16 shows a possible circuit if electronic control of these functions is required. the typical DC level at pins 3 and 22 is 7.5V (V_{CC} = 12V), with the input signal superimposed, and this can be used to bias a FET switch as shown to save components. For switching with a 0V−5V signal a low-threshhold FET is required when using a 12V supply. With larger switching levels this is less critical.

The high impedance PNP base input of the loudness control pin 9 is readily switched with a general purpose NPN transistor.

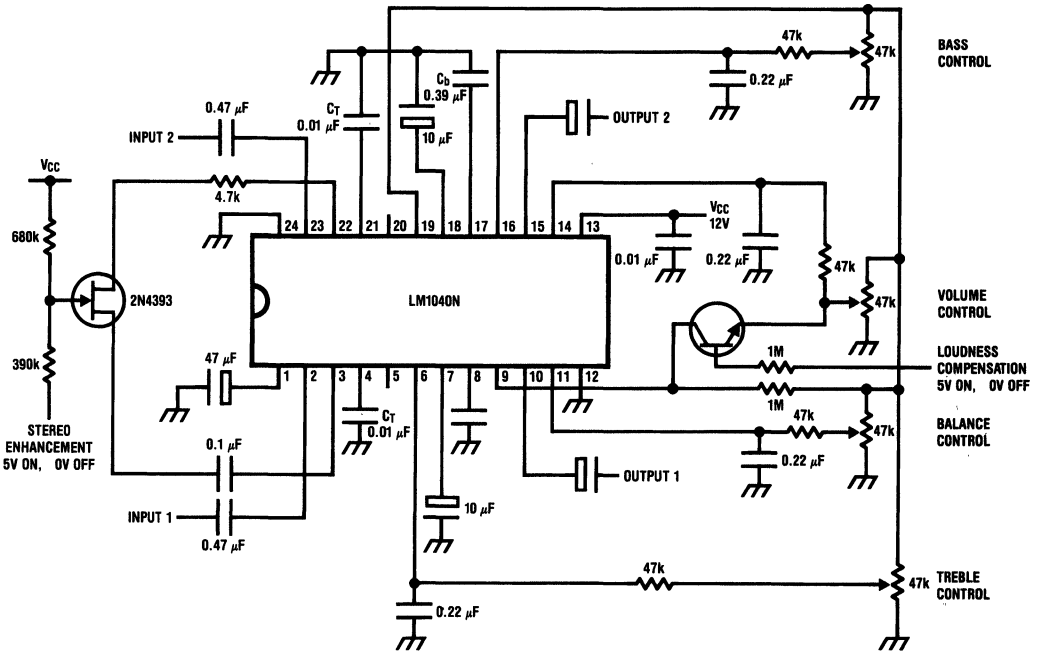

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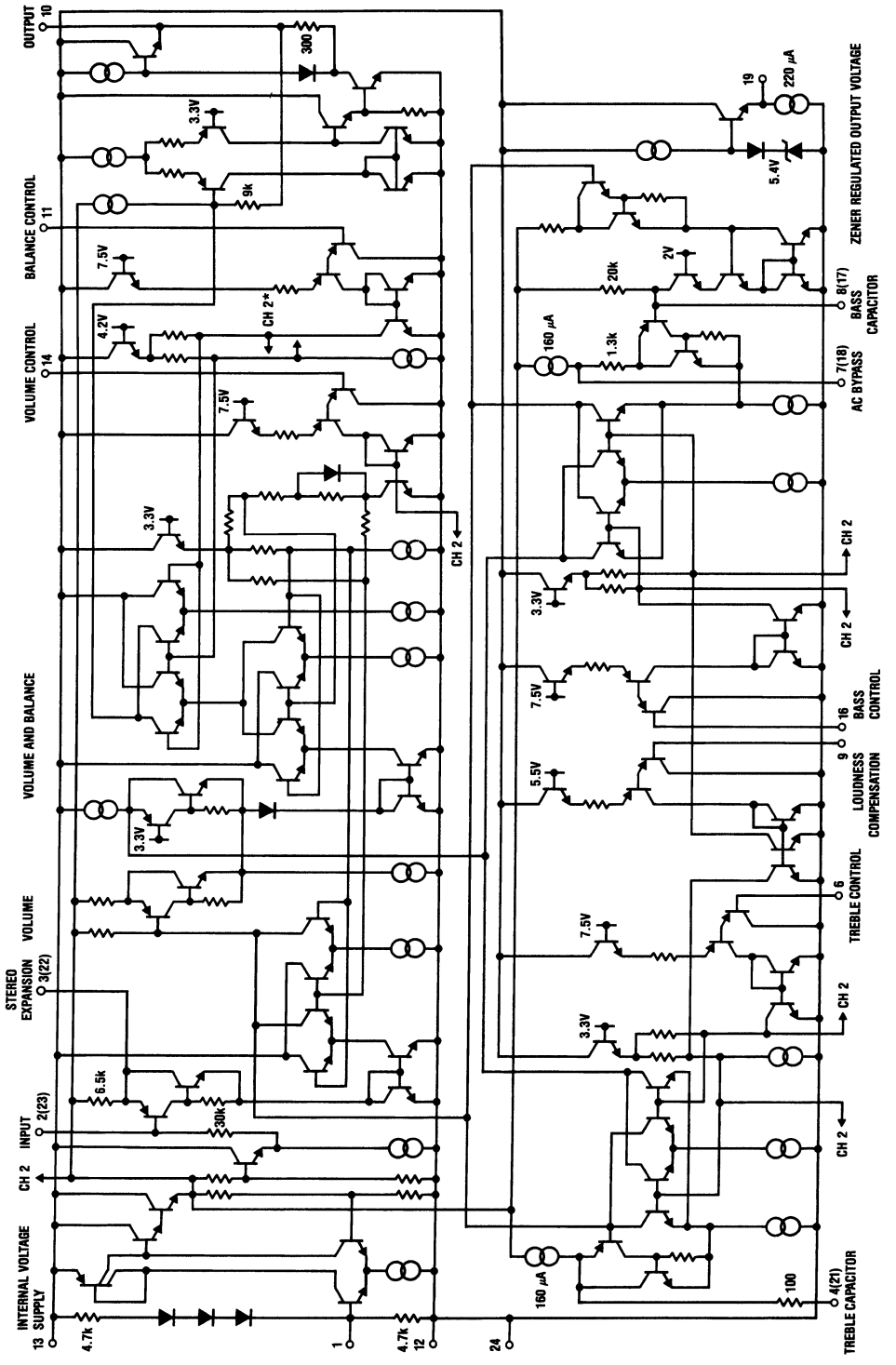
FIGURE 16. Application Circuit with Electronic Switching

Simplified Schematic Diagram (One Channel)



National Semiconductor

LM1131A/LM1131B/LM1131C
Dual Dolby® B-Type Noise Reduction Processor

General Description

The LM1131 is a monolithic integrated circuit specifically designed to realize the Dolby B-Type noise reduction system.

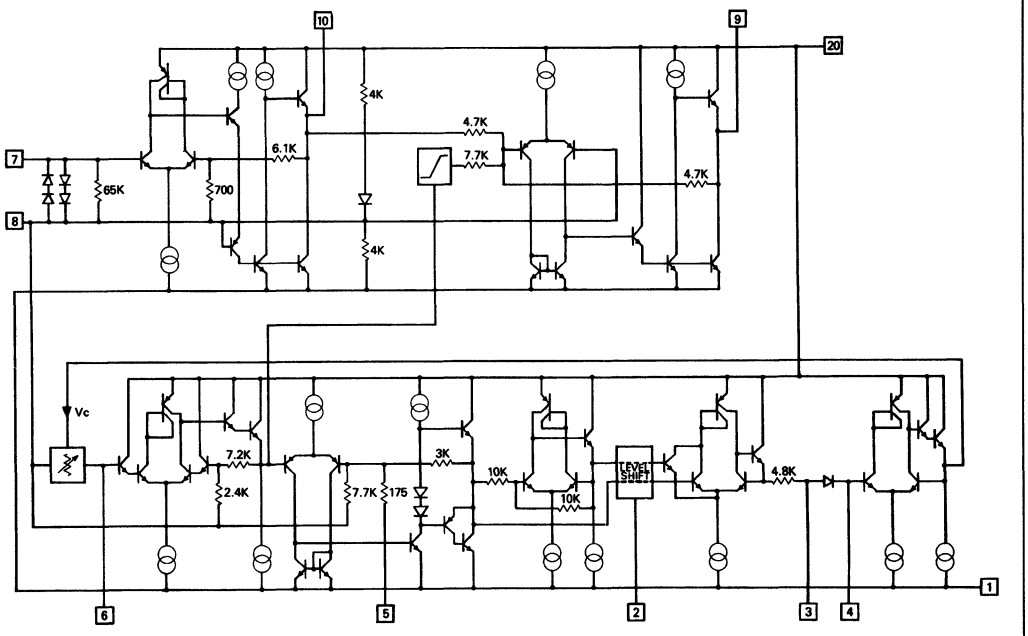
The circuit includes two completely separate noise reduction processors and will operate in both encode and decode modes. It is ideal for stereo applications in compact equipment or for mono applications in 3-head equipment where two processors with very closely matched internal gains are required.

Features

- Stereo Dolby noise reduction with one IC
- Wide supply voltage range, 5V–20V
- Very high signal/noise ratio, 79 dB encode, 90 dB decode (CCIR/ARM)
- Very close gain matching for 3-head recorders
- Close matching to standard Dolby characteristics
- Very low temperature drift of Dolby characteristics
- High signal handling capability, $> +20$ dB ($V_S = 20V$)
- Full-wave rectifier in both channels
- Operates with both single and split supply voltages
- Excellent transient response characteristics
- Minimal input switch-on transients
- Reduced number of external components per channel
- Improved input protection

Available to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

Schematic Diagram (1 channel shown only)



TL/H/6858–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	24V
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

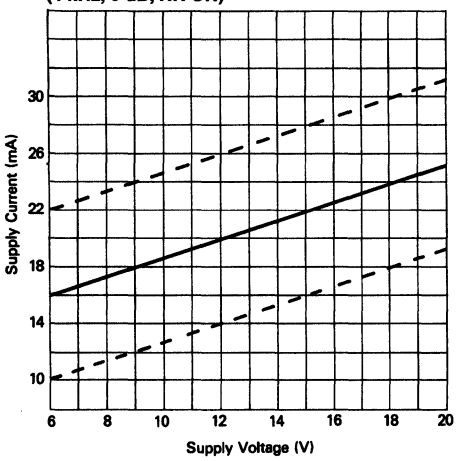
V_S = 12V, T_A = 25°C unless otherwise specified. 0 dB refers to Dolby level and is 580 mV, measured at TP1 and TP2.

Parameter	Conditions	LM1131A			LM1131B			LM1131C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		5		20	5		20	5		20	V
Supply Current			20			20		20			mA
Voltage Gain											
(Pins 7-10 and 14-11)	1 kHz Decode	19.2	19.7	20.2	18.7	19.7	20.7	18.2	19.7	21.2	dB
(Pins 10-9 and 11-12)	1 kHz Decode	−0.5	0	0.5	−0.5	0	0.5	−1.0	0	1.0	dB
Difference in Voltage	1 kHz Noise	−0.2	0	0.2	−0.5	0	0.5	−1.0	0	1.0	dB
Gain between Channels	Reduction OFF										
Crosstalk between Channels	1 kHz, 0 dB	−60	−90		−60	−90		−60	−90		dB
Signal/Noise Ratio at Pins 9 and 12	(Note 1)										
Encode	R_S = 10 kΩ	77	79		75.5	79		74	79		dB
	R_S = 1 kΩ		82			82			82		dB
Decode	R_S = 10 kΩ		90			90			90		dB
	R_S = 1 kΩ		92			92			92		dB
Encode Characteristics	10 kHz, 0 dB	0	0.5	1.0	0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−23.0	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Variation in Encode Characteristics											
Temperature	0°C–70°C		< ±0.5			< ±0.5			< ±0.5		dB
Voltage	5V–20V		< ±0.2			< ±0.2			< ±0.2		dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.2	%
	10 kHz, 10 dB		0.2			0.2			0.2		%
Signal Handling	1 kHz, Dist = 0.3%										
	V_S = 5V		6.5			6.5			6.5		dB
	V_S = 7V		10.5			10.5			10.5		dB
	V_S = 12V	14.0	16.0		14.0	16.0		14.0	16.0		dB
	V_S = 20V		21.0			21.0			21.0		dB
Input Resistance	Pins 7 and 14	45	65	80	45	65	80	45	65	80	kΩ
Output Resistance	Pins 9 and 12		30	55		30	55		30	55	Ω
	Pins 10 and 11		30	55		30	55		30	55	Ω

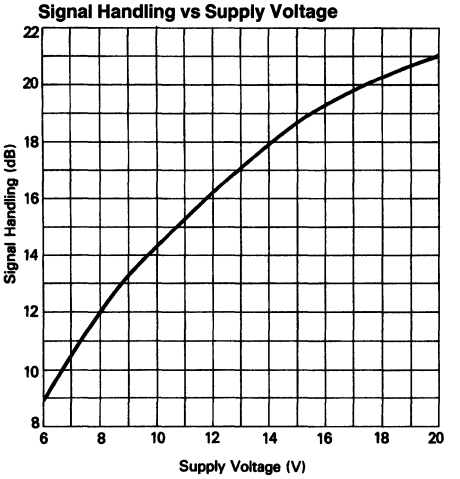
Note 1: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

Supply Current vs Supply Voltage (1 kHz, 0 dB; NR ON)



Signal Handling vs Supply Voltage



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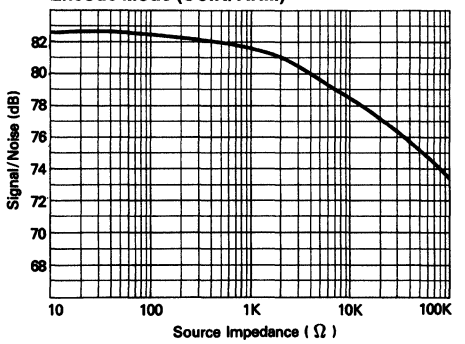
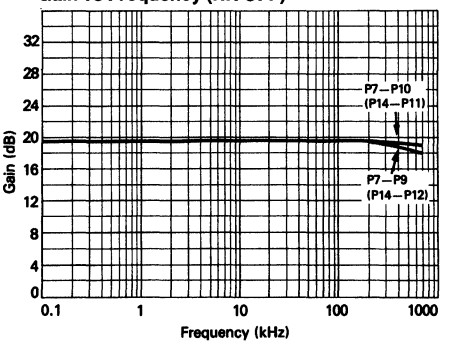
Signal to Noise Ratio vs Source Impedance Encode Mode (CCIR/ARM)

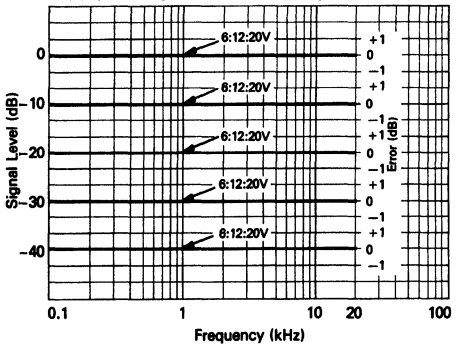


Gain vs Frequency (NR OFF)

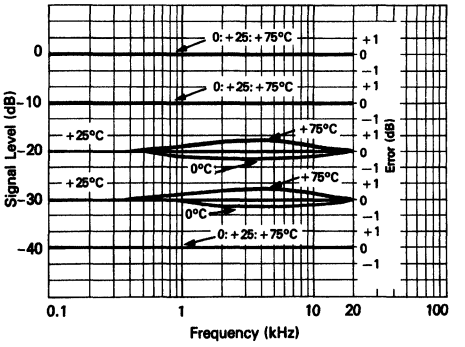


TL/H/6858–3

Back to Back Response Error vs Frequency and Supply Voltage (Standard Dolby Encoder)



Back to Back Response Error vs Frequency and Temperature (Encode Temperature + 25°C)



TL/H/6858–4

Application Notes

SUPPLY VOLTAGE

LM1131 may operate with either single or split supply voltages.

Single Supply Voltage

Pin 1 is connected to ground, pin 20 to V_S.

Pins 8 and 13 are internally generated reference voltages set to approximately half-supply. They should be connected together externally.

A 220 μF capacitor must be connected between pins 8 and 13 and ground. Device turn-on time is delayed by the rise time of pins 8 and 13.

Split Supply Voltages

Pin 1 is connected to the negative supply, pin 20 to the positive supply. Pins 8 and 13 are connected to 0V and no capacitor is required. Device turn-on time is delayed only by the rise times of the supply voltages.

SIGNAL GAIN AND FILTERING

It should be noted that LM1131 has only one internal preamplifier, AB, with no provision for interconnection of a low pass filter to remove bias or multiplex tones. In addition, main chain gain has been reduced by 6 dB in comparison with LM1112/LM1011.

If a low pass filter is required it should be connected at the input of the LM1131. Pre-adjustment of Dolby input level may then be performed, at the input of LM1131 if required.

NOISE REDUCTION SWITCH

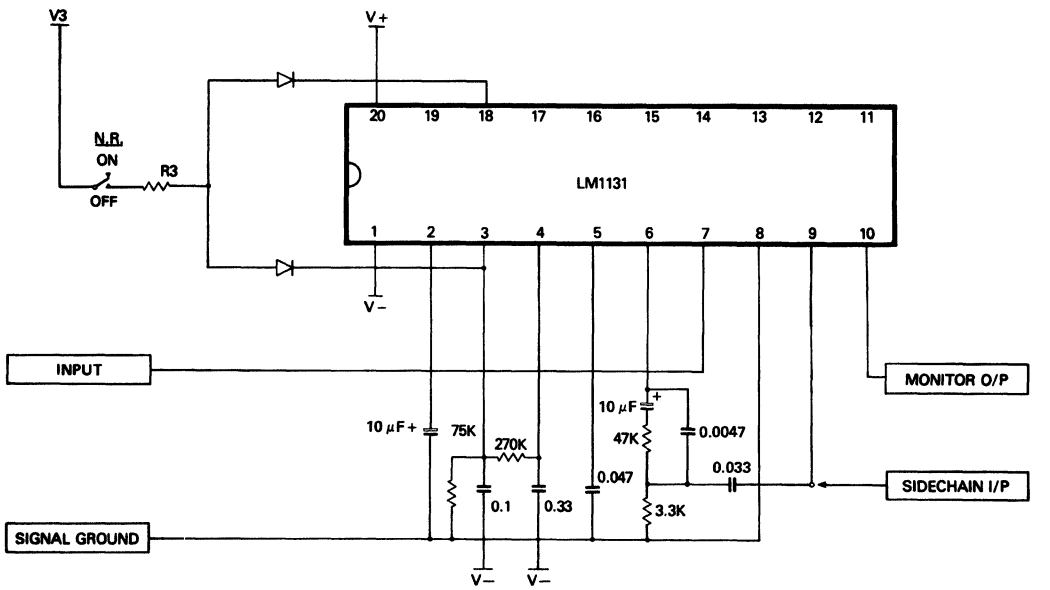
Noise reduction OFF is normally effected by means of a mechanical switch which open-circuits the sidechain input.

An alternative method which permits the control of NR OFF by means of a DC voltage is shown in *Figure 1*. The DC control voltage forces the internal impedance to a minimum value and heavily attenuates the sidechain input. When using this circuit the following points should be noted:

a) Signal boost in encode mode (signal cut in decode) is reduced by increasing DC voltages on pins 3 and 18. A voltage of approximately 3V above signal ground is adequate to achieve NR OFF.

b) Supply current may be increased significantly by high pin 3/18 forcing voltages. Thus, values for V3 and R3 should ideally be chosen such that pin 3/18 forced voltage is only 3V–5V greater than signal ground. Maximum permissible voltage on pin 3/18 is equal to supply voltage.

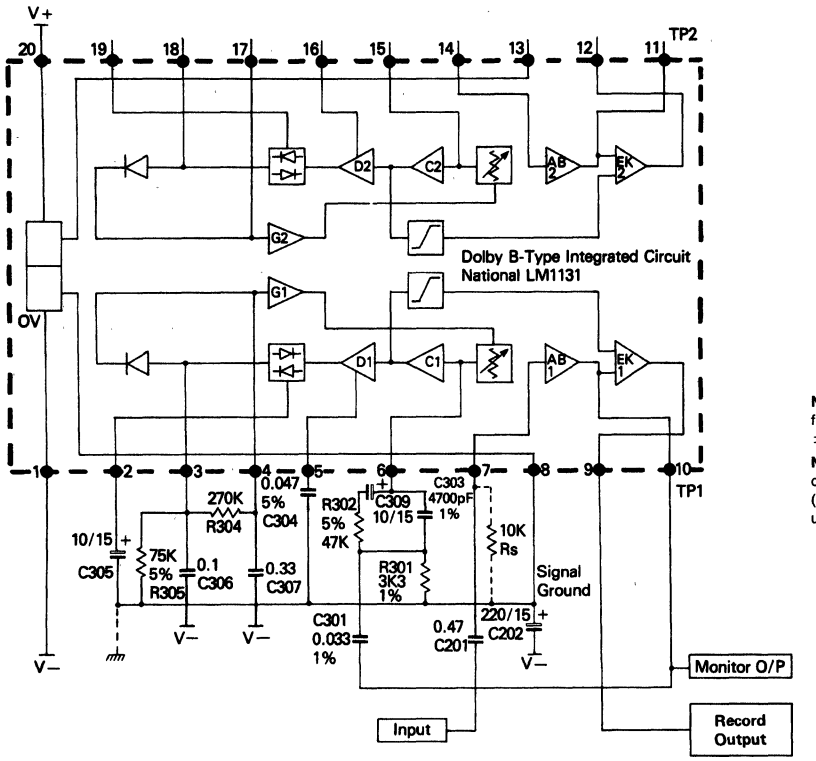
c) When electrical NR switching is used in this way, NR OFF signal level is slightly affected by the restriction that the internal variable impedance cannot achieve zero impedance. Thus, at 10 kHz–10 dB, a residual boost in encode (or cut in decode) of approximately 0.4 dB remains. At low frequencies this value reduces to insignificant levels. This is not the case for mechanical NR switching.



TL/H/6858–5

FIGURE 1. LM1131 Decode Processor with Electrical NR Switch (1 Channel Shown)

Test Circuit Encode Mode (components shown for channel 1 only)



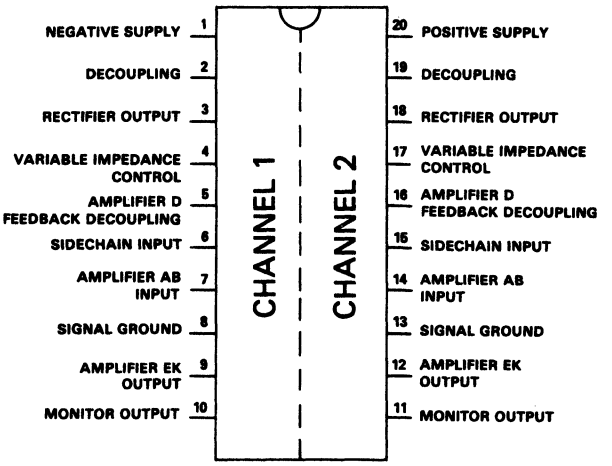
Note 1: Where not otherwise specified component tolerances are ±10%

Note 2: For LM1131AN use 2% components for C304, R303, R305. (5% components may cause errors up to ± 0.3 dB).

TL/H/6858–6

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/6858–7

Order Number LM1131AN, LM1131BN, LM1131CM or LM1131CN
See NS Package Number M20B or N20A

National Semiconductor

PRELIMINARY

LM1151
Dolby® B-Type Noise Reduction System

General Description

The LM1l151 is a two-channel encode/decode switchable Dolby B-type noise reduction processor.

The circuit includes two completely separate noise reduction processors and will operate in both encode and decode modes.

Electronic switching simplifies switching from record to playback modes of operation and turn on/off of noise reduction.

Applications

- Compact stereo audio equipment
- Dubbing cassette decks

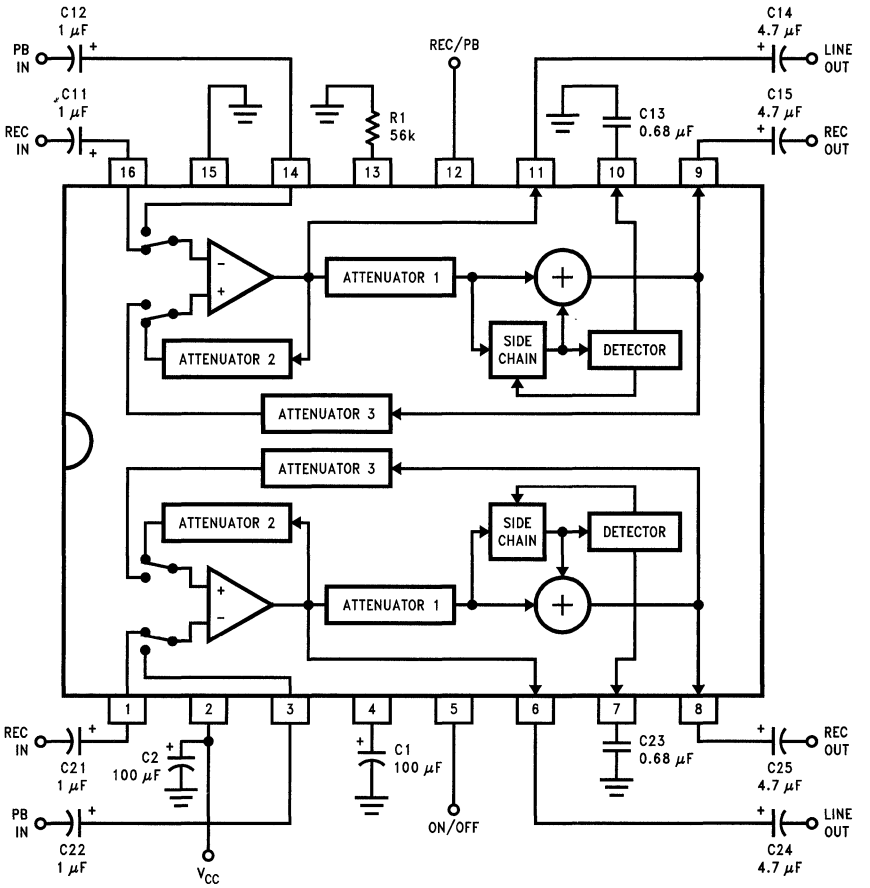
Features

- Minimum number of external components
- Electronic NR ON/OFF and REC/PB switching
- Small surface mount package
- Two channel processors on one chip
- Operates with both single and split supply voltages

Key Specifications

■ Supply Voltage Range	6.5V to 15V
■ LINE OUT Level	387.5 mV (−6 dBm)
■ Signal Handling	≥ +14 dB

Block Diagram and Typical Application



TL/H/11439–1

National Semiconductor

LM1875 20 Watt Power Audio Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

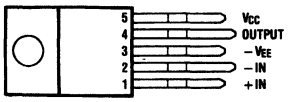
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion: 0.015%, 1 kHz, 20 W
- Wide power bandwidth: 70 kHz
- Protection for AC and DC short circuits to ground
- Thermal protection with parole circuit
- High current capability: 4A
- Wide supply range 16V-60V
- Internal output protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram



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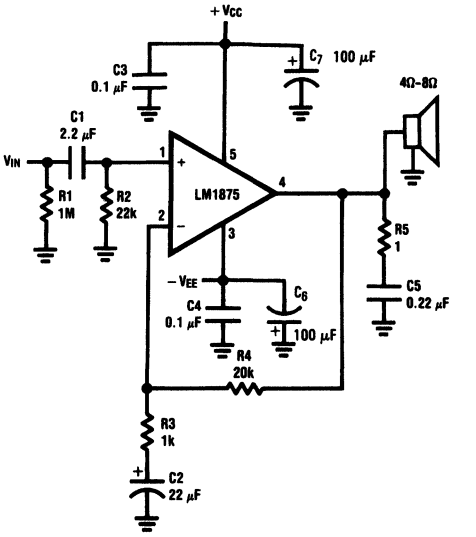
Front View

Order Number LM1875T
See NS Package Number T05B

Typical Applications



TL/H/5030–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	60V
Input Voltage	$-V_{EE}$ to V_{CC}
Storage Temperature	−65°C to + 150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

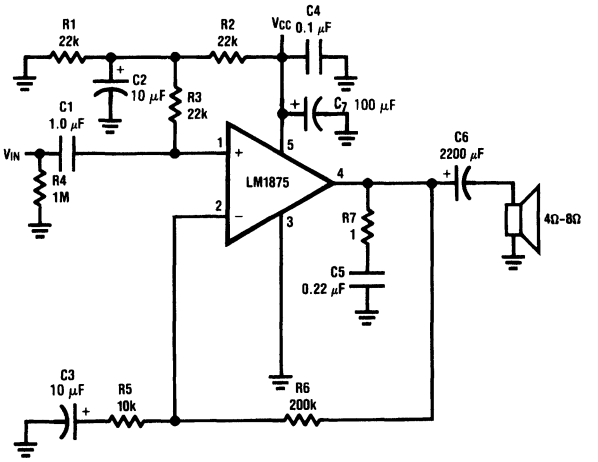
V_{CC} = +25V, $-V_{EE}$ = −25V, $T_{AMBIENT}$ = 25°C, R_L = 8Ω, A_V = 20 (26 dB), f_o = 1 kHz, unless otherwise specified.

Parameter	Conditions	Typical	Tested Limits	Units
Supply Current	P_{OUT} = 0W	70	100	mA
Output Power (Note 1)	THD = 1%	25		W
THD (Note 1)	P_{OUT} = 20W, f_o = 1 kHz	0.015		%
	P_{OUT} = 20W, f_o = 20 kHz	0.05	0.4	%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 1 kHz	0.022		%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 20 kHz	0.07	0.6	%
Offset Voltage		±1	±15	mV
Input Bias Current		±0.2	±2	μA
Input Offset Current		0	±0.5	μA
Gain-Bandwidth Product	f_o = 20 kHz	5.5		MHz
Open Loop Gain	DC	90		dB
PSRR	V_{CC}, 1 kHz, 1 Vrms	95	52	dB
	V_{EE}, 1 kHz, 1 Vrms	83	52	dB
Max Slew Rate	20W, 8Ω, 70 kHz BW	8		V/μs
Current Limit	V_{OUT} = V_{SUPPLY} −10V	4	3	A
Equivalent Input Noise Voltage	R_S = 600Ω, CCIR	3		μVrms

Note 1: Assumes the use of a heat sink having a thermal resistance of 1°C/W and no insulator with an ambient temperature of 25°C. Because the output limiting circuitry has a negative temperature coefficient, the maximum output power delivered to a 4Ω load may be slightly reduced when the tab temperature exceeds 55°C.

Typical Applications (Continued)

Typical Single Supply Operation



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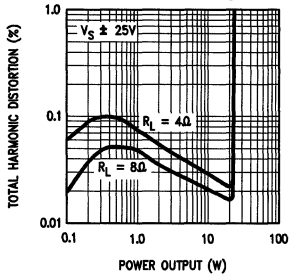
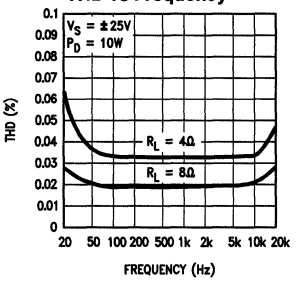
Typical Performance Characteristics

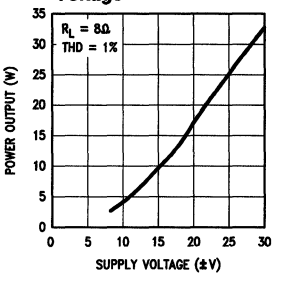
THD vs Power Output



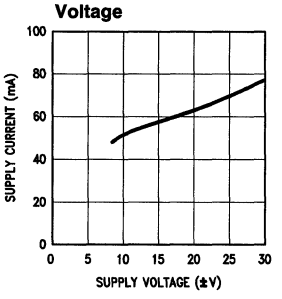
THD vs Frequency



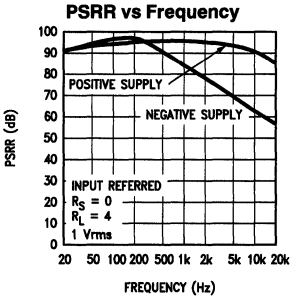
Power Output vs Supply Voltage



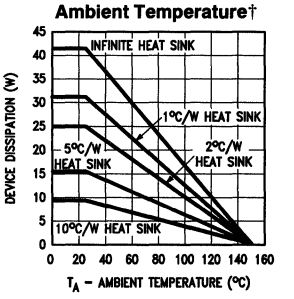
Supply Current vs Supply Voltage



PSRR vs Frequency

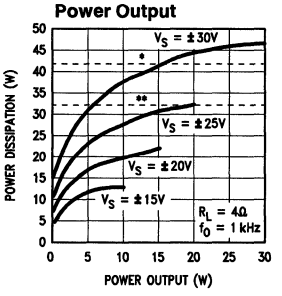


Device Dissipation vs Ambient Temperature†

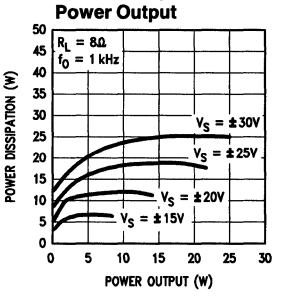


†ϕINTERFACE = 1°C/W.
See Application Hints.

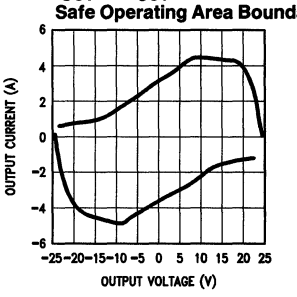
Power Dissipation vs Power Output



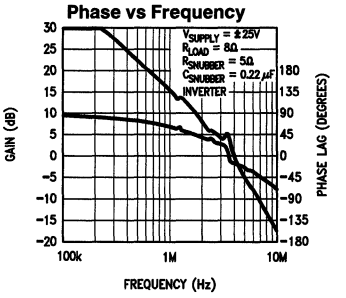
Power Dissipation vs Power Output



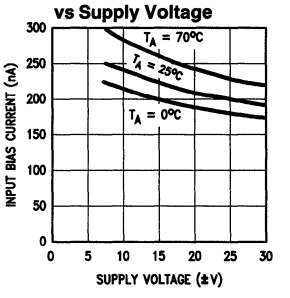
I_{OUT} vs V_{OUT}-Current Limit/ Safe Operating Area Boundary



Open Loop Gain and Phase vs Frequency



Input Bias Current vs Supply Voltage



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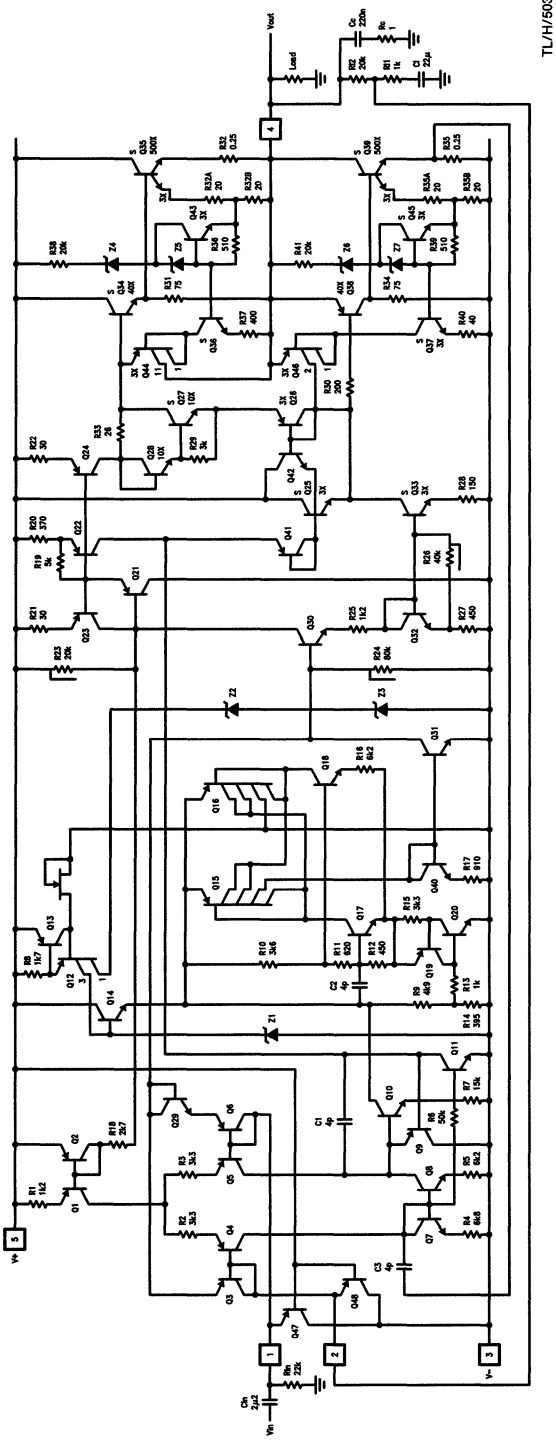
*Thermal shutdown with infinite heat sink

**Thermal shutdown with 1°C/W heat sink

Schematic Diagram



TL/H/5030–5

Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JC} = 2°C/W$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry.

If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

4.2°C/W − 2°C/W − 1.6°C/W = 0.6°C/W.

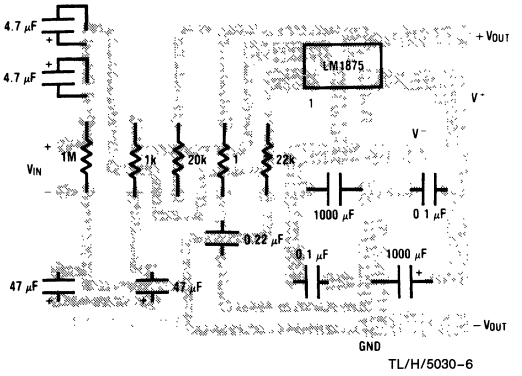
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



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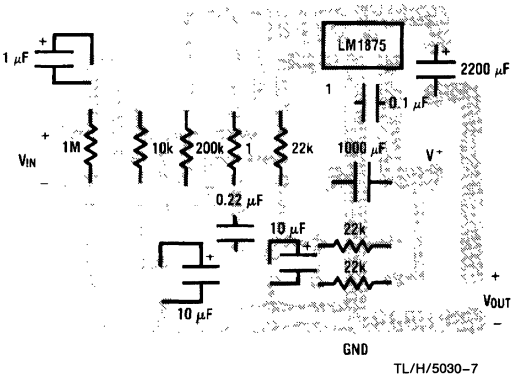
Single Supply



TL/H/5030–7

National Semiconductor

LM1877 Dual Power Audio Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

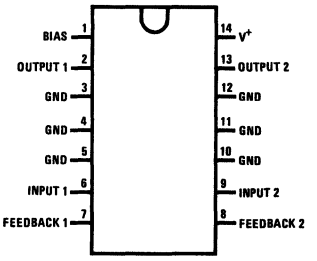
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred
- Wide supply range, 6V–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

Dual-In-Line Package
or Surface Mount Package



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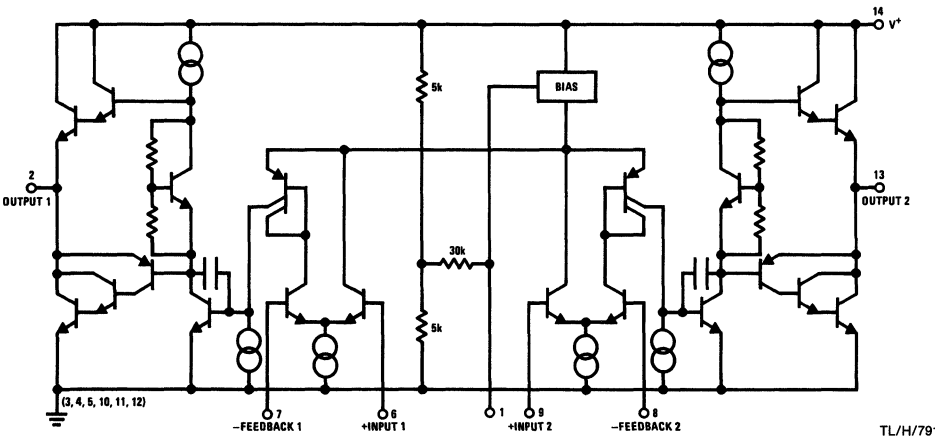
Top View

Order Number LM1877M-9 or LM1877N-9
See NS Package Number M14B or N14A

Equivalent Schematic Diagram



TL/H/7913–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C

Lead Temperature	
N-Package Soldering (10 sec.)	260°C
M-Package Infared (15 sec.)	220°C
M-Package Vapor Phase (60 sec.)	215°C
Thermal Resistance, θ_{JA}	
M-Package	106°C/W
N-Package	76°C/W

Electrical Characteristics

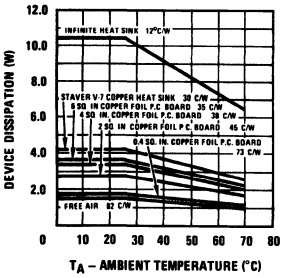
V_S = 20V, T_A = 25°C, (See Note 1) R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Output Power LM1877	THD = 10% V_S = 20V, R_L = 8Ω	2.0			W/Ch
Total Harmonic Distortion LM1877	f = 1 kHz, V_S = 14V				
	P_O = 50 mW/Channel		0.075		%
	P_O = 500 mW/Channel		0.045		%
	P_O = 1 W/Channel		0.055		%
Output Swing	R_L = 8Ω		V_S −6		Vp-p
Channel Separation	C_F = 50 μF, C_{IN} = 0.1 μF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply Rejection Ratio	C_F = 50 μF, C_{IN} = 0.1 μF, f = 120 Hz, Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−65		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 μF, BW = 20 Hz–20 kHz, Output Noise Wideband		2.5		μV
	R_S = 0, C_N = 0.1 μF, A_V 200		0.80		mV
Open Loop Gain	R_S = 0, f = 100 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

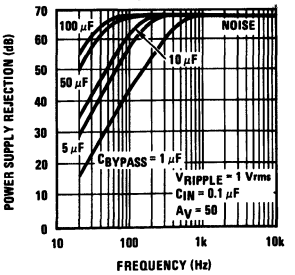
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature.

Typical Performance Characteristics

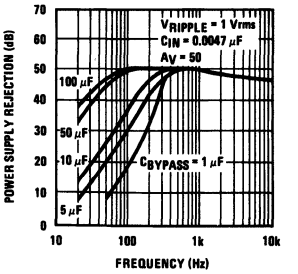
Device Dissipation vs Ambient Temperature



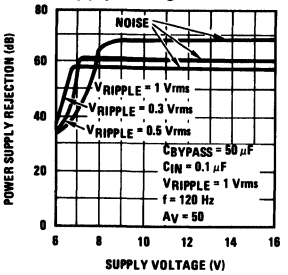
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



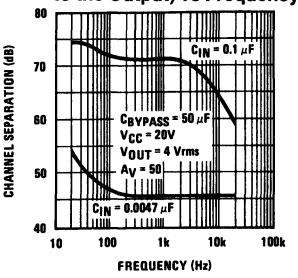
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



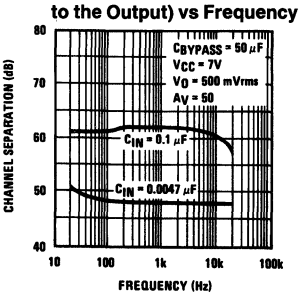
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



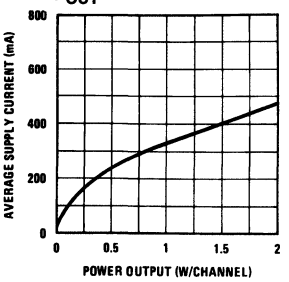
Channel Separation (Referred to the Output) vs Frequency



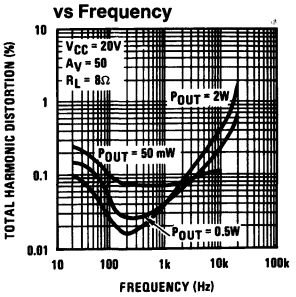
Channel Separation (Referred to the Output) vs Frequency



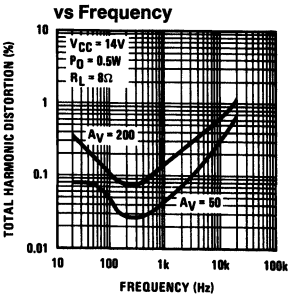
Average Supply Current vs P_{OUT}



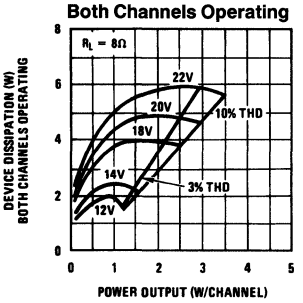
Total Harmonic Distortion vs Frequency



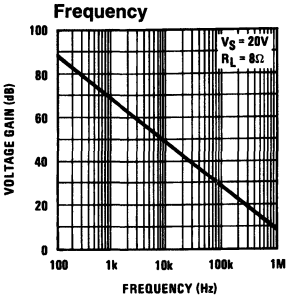
Total Harmonic Distortion vs Frequency



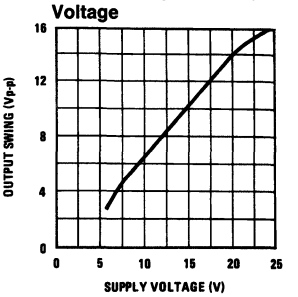
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency



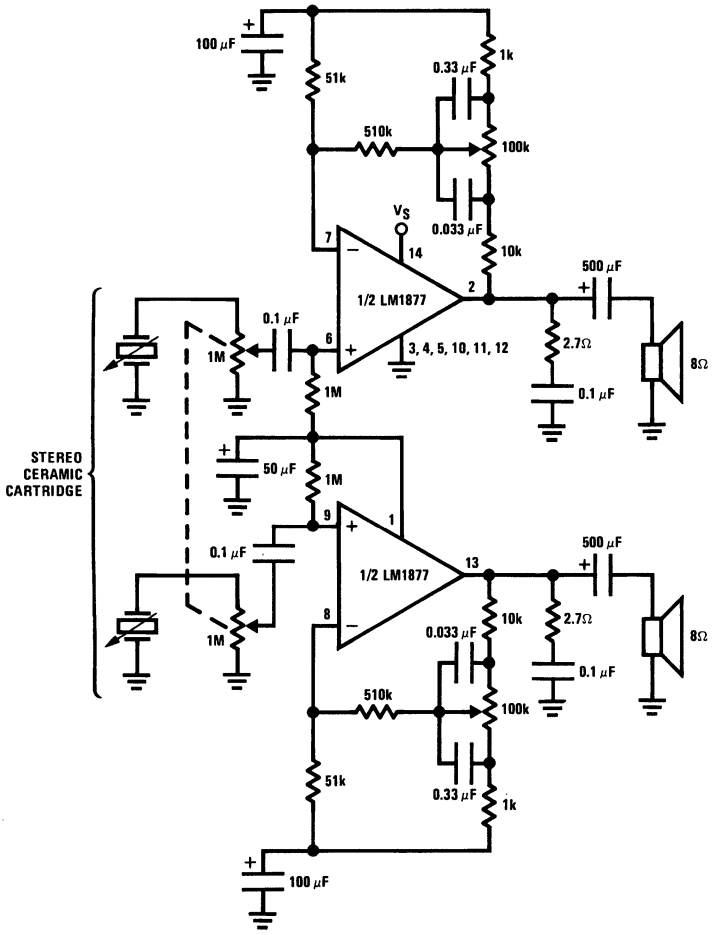
Output Swing vs Supply Voltage



TL/H/7913–3

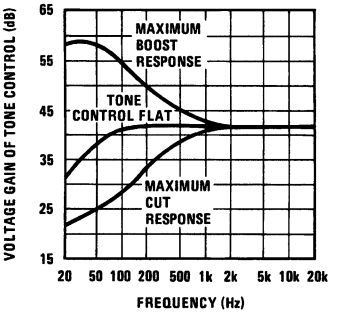
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



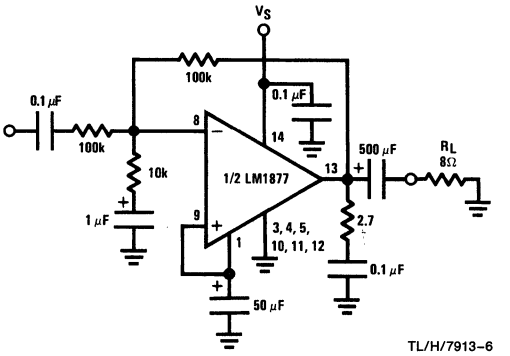
TL/H/7913–4

Frequency Response of Bass Tone Control



TL/H/7913–5

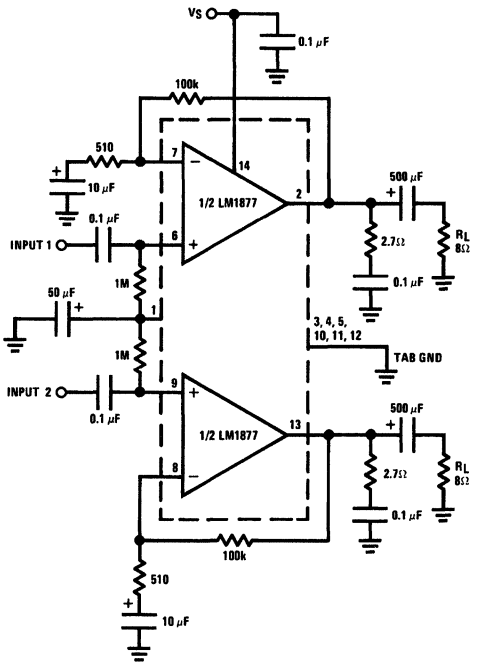
Inverting Unity Gain Amplifier



TL/H/7913–6

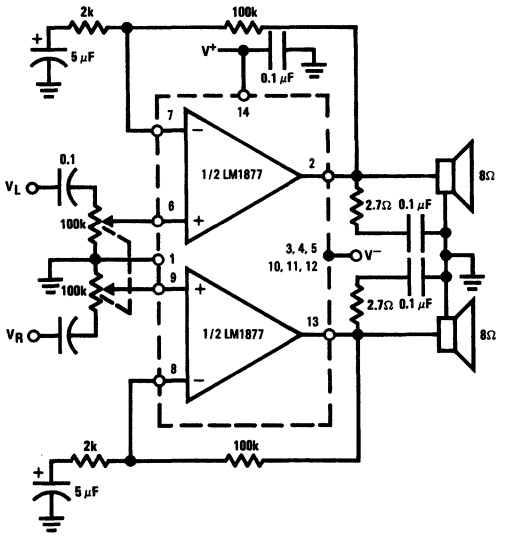
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$



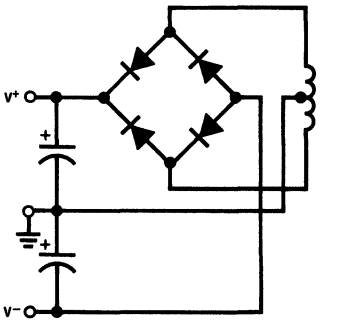
TL/H/7913–7

Non-Inverting Amplifier Using Split Supply



TL/H/7913–8

Typical Split Supply



TL/H/7913–9

National Semiconductor

DNR® DYNAMIC NOISE REDUCTION SYSTEM

LM1894 Dynamic Noise Reduction System DNR®

General Description

The LM1894 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is non-complementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

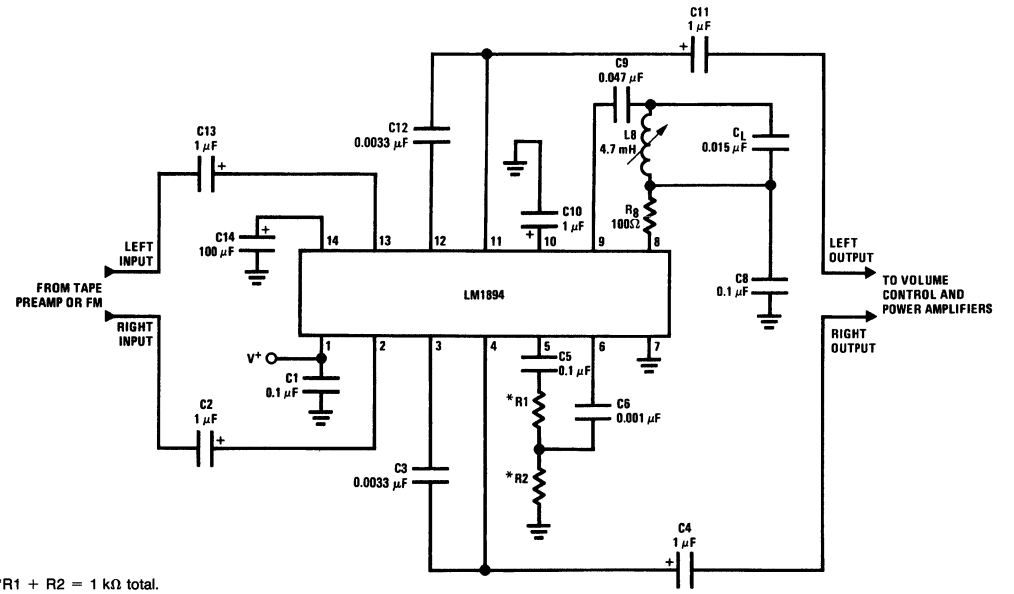
Features

- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 4.5V to 18V
- 1 Vrms input overload

Applications

- Automotive radio/tape players
- Compact portable tape players
- Quality HI-FI tape systems
- VCR playback noise reduction
- Video disc playback noise reduction

Typical Application



*R1 + R2 = 1 kΩ total.
See Application Hints.

TL/H/7918–1

FIGURE 1. Component Hook-Up for Stereo DNR System

Order Number LM1894M or LM1894N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	20V
Input Voltage Range, V_{pk}	$V_S/2$
Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_S = 8V, T_A = 25°C, V_{IN} = 300 mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Range		4.5	8	18	V
Supply Current	V_S = 8V		17	30	mA
MAIN SIGNAL PATH					
Voltage Gain	DC Ground Pin 9, Note 2	−0.9	−1	−1.1	V/V
DC Output Voltage		3.7	4.0	4.3	V
Channel Balance	DC Ground Pin 9	−1.0		1.0	dB
Minimum Balance	AC Ground Pin 9 with 0.1 μF Capacitor, Note 2	675	965	1400	Hz
Maximum Bandwidth	DC Ground Pin 9, Note 2	27	34	46	kHz
Effective Noise Reduction	CCIR/ARM Weighted, Note 3		−10	−14	dB
Total Harmonic Distortion	DC Ground Pin 9		0.05	0.1	%
Input Headroom	Maximum V_{IN} for 3% THD AC Ground Pin 9		1.0		Vrms
Output Headroom	Maximum V_{OUT} for 3% THD DC Ground Pin 9		V_S − 1.5		Vp-p
Signal to Noise	BW = 20 Hz–20 kHz, re 300 mV				
	AC Ground Pin 9		79		dB
	DC Ground Pin 9		77		dB
	CCIR/ARM Weighted re 300 mV Note 4				
	AC Ground Pin 9	82	88		dB
	DC Ground Pin 9	70	76		dB
	CCIR Peak, re 300 mV, Note 5				
	AC Ground Pin 9		77		dB
	DC Ground Pin 9		64		dB
Input Impedance	Pin 2 and Pin 13	14	20	26	kΩ
Channel Separation	DC Ground Pin 9	−50	−70		dB
Power Supply Rejection	C14 = 100 μF, V_{RIPPLE} = 500 mVrms, f = 1 kHz	−40	−56		dB
Output DC Shift	Reference DVM to Pin 14 and Measuree Output DC Shift from Minimum to Maximum Bandwidth, Note 6.		4.0	20	mV

Electrical Characteristics

V_S = 8V, T_A = 25°C, V_{IN} = 300 mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
CONTROL SIGNAL PATH					
Summing Amplifier Voltage Gain	Both Channels Driven	0.9	1	1.1	V/V
Gain Amplifier Input Impedance	Pin 6	24	30	39	kΩ
Voltage Gain	Pin 6 to Pin 8	21.5	24	26.5	V/V
Peak Detector Input Impedance	Pin 9	560	700	840	Ω
Voltage Gain	Pin 9 to Pin 10	30	33	36	V/V
Attack Time	Measured to 90% of Final Value with 10 kHz Tone Burst	300	500	700	μs
Decay Time	Measured to 90% of Final Value with 10 kHz Tone Burst	45	60	75	ms
DC Voltage Range	Minimum Bandwidth to Maximum Bandwidth	1.1		3.8	V

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 1) 80°C/W junction to ambient for the dual-in-line package, and 2) 105°C/W junction to ambient for the small outline package.

Note 2: To force the DNR system into maximum bandwidth, DC ground the input to the peak detector, pin 9. A negative temperature coefficient of −0.5%/°C on the bandwidth, reduces the maximum bandwidth at increased ambient temperature or higher package dissipation. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Appliction Hints.

Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives −10 dB of noise reduction. See Application Hints.

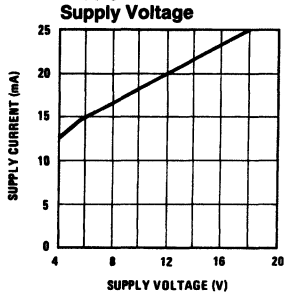
Note 4: The CCIR/ARM weighted noise is measured with a 40 dB gain amplifier between the DNR system and the CCIR weighting filter; it is then input referred.

Note 5: Measured using the Rhode-Schwartz psophometer.

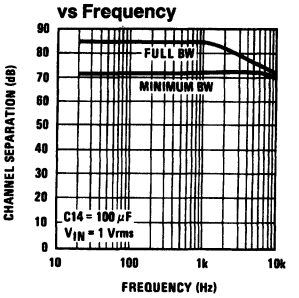
Note 6: Pin 10 is DC forced half way between the maximum bandwidth DC level and minimum bandwidth DC level. An AC 1 kHz signal is then applied to pin 10. Its peak-to-peak amplitude is V_{DC} (max BW) − V_{DC} (min BW).

Typical Performance Characteristics

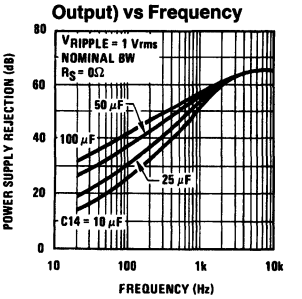
Supply Current vs Supply Voltage



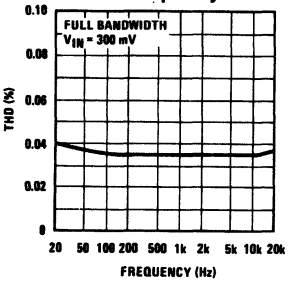
Channel Separation (Referred to the Output) vs Frequency



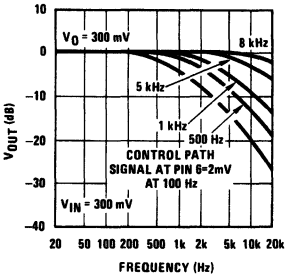
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



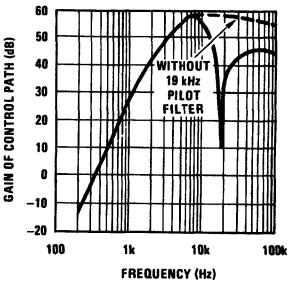
THD vs Frequency



−3 dB Bandwidth vs Frequency and Control Signal



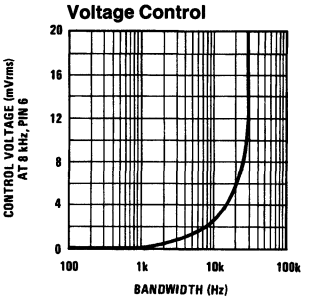
Gain of Control Path vs Frequency (with 10 kHz FM Pilot Filter)



TL/H/7918–2

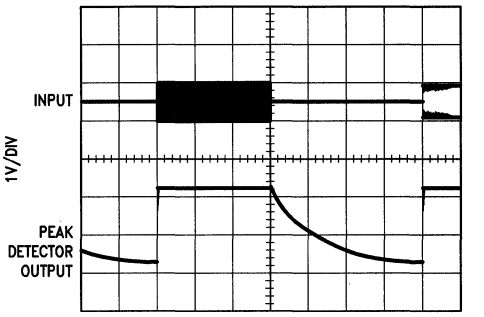
Typical Performance Characteristics (Continued)

Main Signal Path Bandwidth vs Voltage Control



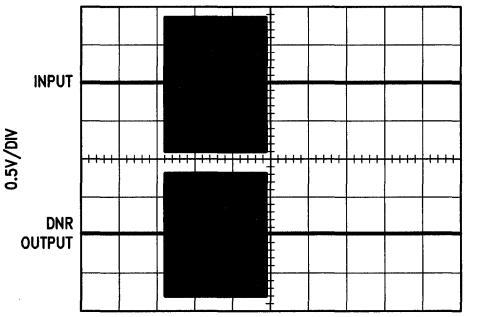
TL/H/7918–3

Peak Detector Response



TL/H/7918–4

Output Response



TL/H/7918–5

External Component Guide *(Figure 1)*

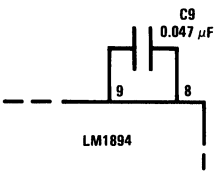
Component	Value	Purpose
C1	0.1 μF–100 μF	May be part of power supply, or may be added to suppress power supply oscillation.
C2, C13	1 μF	Blocks DC, pin 2 and pin 13 are at DC potential of $V_S/2$. C2, C13 form a low frequency pole with 20k R_{IN}. $f_L = \frac{1}{2\pi\ C2\ R_{IN}}$
C14	25 μF–100 μF	Improves power supply rejection.
C3, C12	0.0033 μF	Forms integrator with internal gm block and op amp. Sets bandwidth conversion gain of 33 Hz/μA of gm current.
C4, C11	1 μF	Output coupling capacitor. Output is at DC potential of $V_S/2$.
C5	0.1 μF	Works with R1 and R2 to attenuate low frequency transients which could disturb control path operation. $f_5 = \frac{1}{2\pi\ C5\ (R1 + R2)} = 1.6\ kHz$
C6	0.001 μF	Works with input resistance of pin 6 to form part of control path frequency weighting. $f_6 = \frac{1}{2\pi\ C6\ R1_{PIN\ 6}} = 5.3\ kHz$
C8	0.1 μF	Combined with L8 and C_L forms 19 kHz filter for FM pilot. This is only required in FM applications (Note 1).

External Component Guide (Figure 1)
(Continued)

Component	Value	Purpose
L8, C_L	4.7 mH, 0.015 μF	Forms 19 kHz filter for FM pilot. L8 is Toko coil CAN-1A185HM* (Note 1).
C9	0.047 μF	Works with input resistance of pin 9 to form part of control path frequency weighting. $f_9 = \frac{1}{2\pi\ C9\ R_{PIN\ 9}} = 4.8$ kHz
C10	1 μF	Set attack and decay time of peak detector.
R1, R2	1 kΩ	Sensitivity resistors set the noise threshold. Reducing attentuation causes larger signals to be peak detected and larger bandwidth in main signal path. Total value of R1 + R2 should equal 1 kΩ.
R8	100Ω	Forms RC roll-off with C8. This is only required in FM applications.

* Toko America Inc., 1250 Feehanville Drive, Mt. Prospect IL 60056

Note 1: When FM applications are not required, pin 8 and pin 9 hook-up as follows:



TL/H/7918–6

Circuit Operation

The LM1894 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a gm block with a variable current, and an op amp configured as an integrator. As seen in *Figure 2*, DC feedback constrains the low frequency gain to $A_V = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.0033 μF capacitor.

The purpose of the control paths is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 2*. The R1, R2 resistor divider adjusts the incoming noise level to open slightly the bandwidth of the low pass filter. Control path gain is about 60 dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 μF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the gm blocks. The bandwidth sensitivity to gm current is 33 Hz/μA. In FM stereo applications at 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 1*.

Figure 3 is an interesting curve and deserves some discussion. Although the output of the DNR system is a linear function of input signal, the −3 dB bandwidth is not. This is due to the non-linear nature of the control path. The DNR system has a uniform frequency response, but looking at the −3 dB bandwidth on a steady state basis with a single frequency input can be misleading. It must be remembered that a single input frequency can only give a single −3 dB bandwidth and the roll-off from this point must be a smooth −6 dB/oct.

A more accurate evaluation of the frequency response can be seen in *Figure 4*. In this case the main signal path is frequency swept, while the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

Psychoacoustic Basics

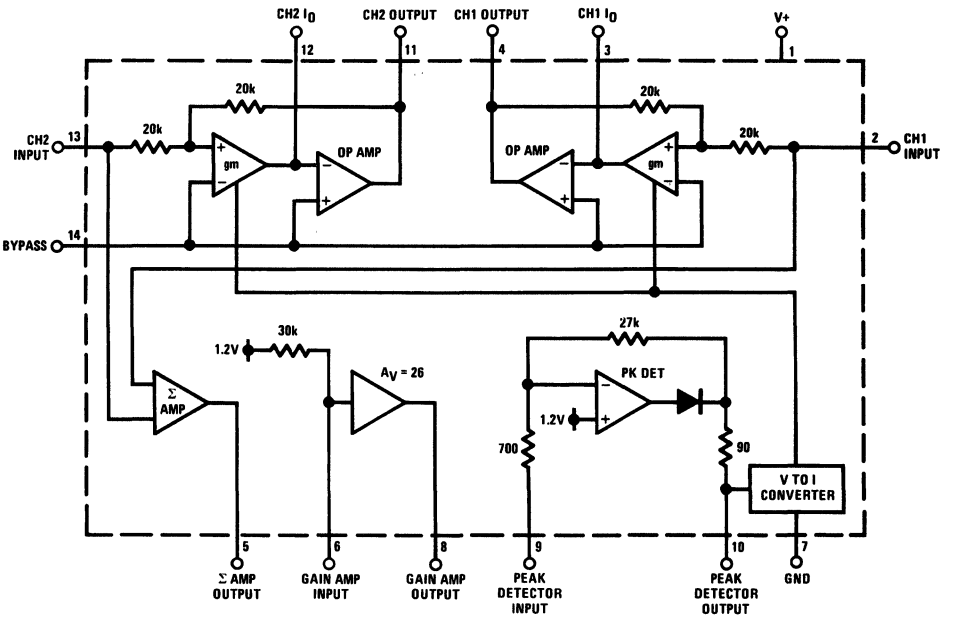
The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR system operates on three principles of psychoacoustics.

1. White noise can mask pure tones. The total noise energy required to mask a pure tone must equal the energy of the tone itself. Within certain limits, the wider the band of masking noise about the tone, the lower the noise amplitude need be. As long as the total energy of the noise is equal to or greater than the energy of the tone, the tone will be inaudible. This principle may be turned around; when music is present, it is capable of masking noise in the same bandwidth.

2. The ear cannot detect distortion for less than 1 ms. On a transient basis, if distortion occurs in less than 1 ms, the ear acts as an integrator and is unable to detect it. Because of this, signals of sufficient energy to mask noise open bandwidth to 90% of the maximum value in less than 1 ms. Reducing the bandwidth to within 10% of its minimum value is done in about 60 ms: long enough to allow the ambience of the music to pass through, but not so long as to allow the noise floor to become audible.

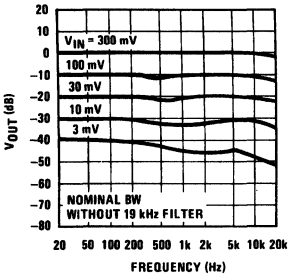
3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR system low pass filters this noise. Low frequency music will not appreciably open the DNR bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Block Diagram



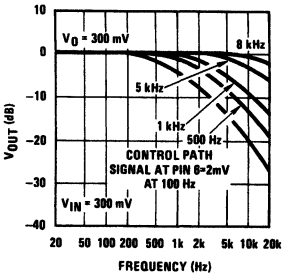
TL/H/7918–7

FIGURE 2



TL/H/7918–8

FIGURE 3. Output vs Frequency



TL/H/7918–9

FIGURE 4. −3 dB Bandwidth vs Frequency and Control Signal

Application Hints

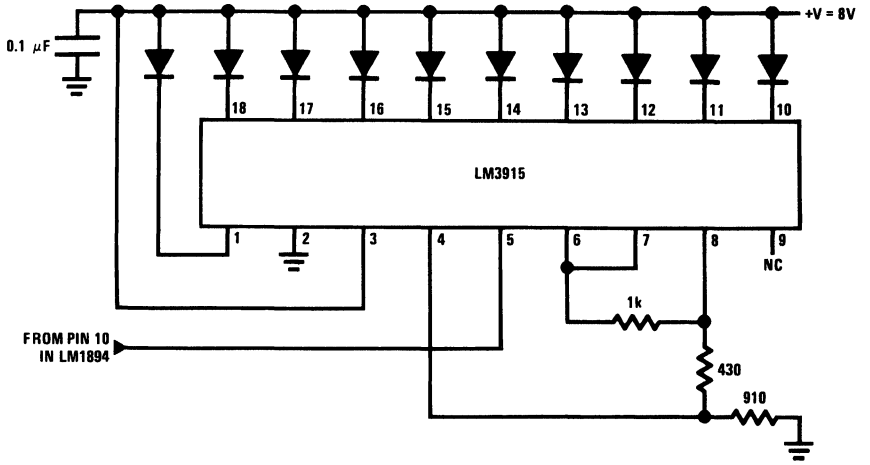
The DNR system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to open slightly the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 5*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C12, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.0039 μF capacitor to 0.0033 μF will change the typical bandwidth from 965 Hz–34 kHz to 1.1 kHz–40 kHz. With C3 and C12 set at 0.0033 μF, the maximum bandwidth is typically 34 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C10. Decay times can be decreased by paralleling a resistor with C10, and increased by increasing the value of C10.

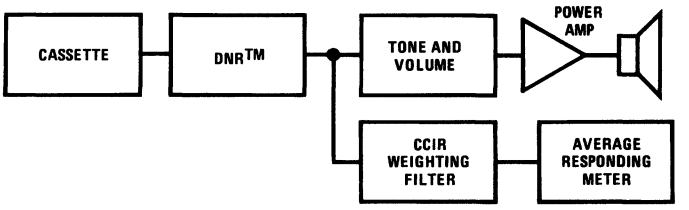
Application Hints (Continued)

When measuring the amount of noise reduction of the DNR system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 6*. The DNR system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.



TL/H/7918–10

FIGURE 5. Bar Graph Display of Peak Detector Voltage



TL/H/7918–11

FIGURE 6. Technique for Measuring S/N Improvement of the DNR System

Application Hints (Continued)

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System", Blackmer, *'dB' Magazine,* August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, *Sert Journal,* May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, *Audioscene Canada,* April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, *JAES,* 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, *JAES,* Volume 39, #4, 1966.

2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, *JAES,* Volume 22, #1, 1950.

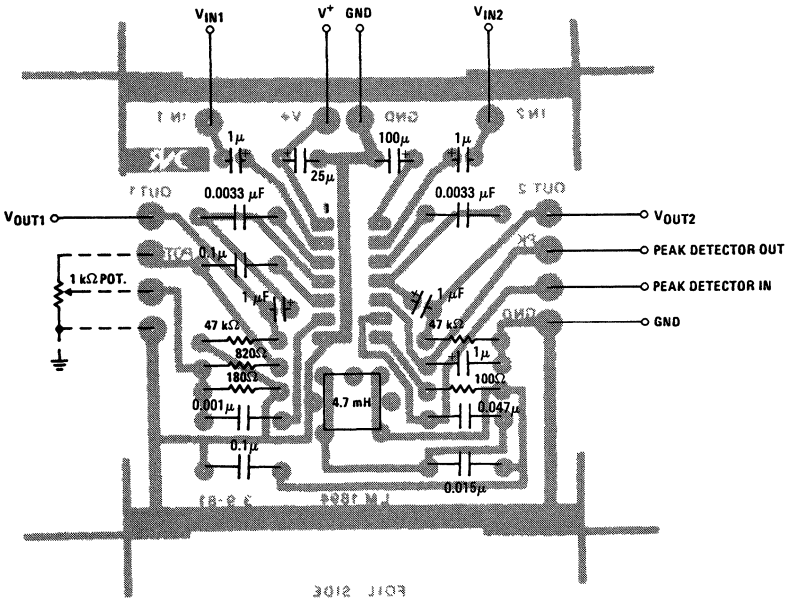
3. "Sound System Engineering", Davis Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

Printed Circuit Layout

DNR Component Diagram



TL/H/7918–12

National Semiconductor

LM1896/LM2896 Dual Power Audio Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies (V_S > 9V) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

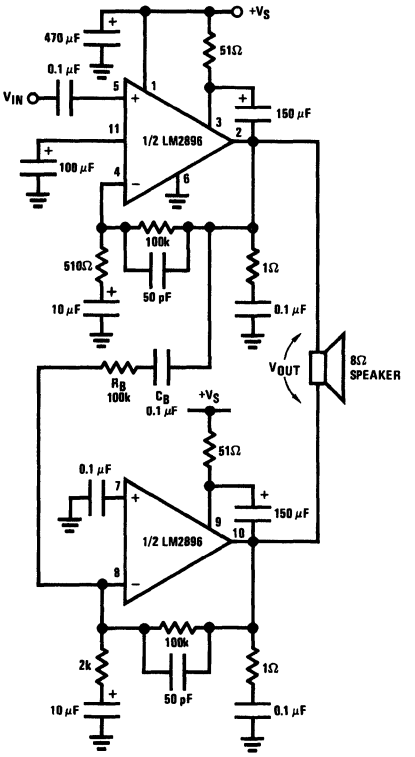
Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo P_O = 250 mW
- Wide supply operation 3V–15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- P_O = 9W bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications



TL/H/7920–1

FIGURE 1. LM2896 in Bridge Configuration (A_V = 400, BW = 20 kHz)

Order Number LM1896N **Order Number LM2896P**

See NS Package Number N14A **See NS Package Number P11A**

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- LM1896 V_S = 12V
- LM2896 V_S = 18V

Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

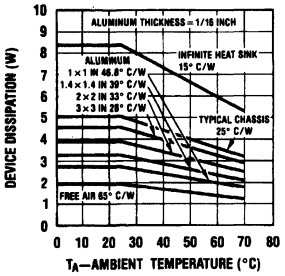
Unless otherwise specified, T_A = 25°C, A_V = 200 (46 dB). For the LM1896; V_S = 6V and R_L = 4Ω. For LM2896, T_{TAB} = 25°C, V_S = 12V and R_L = 8Ω. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1896			LM2896			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	P_O = 0W, Dual Mode		15	25		25	40	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1896N-1	V_S = 6V, R_L = 4Ω Dual Mode, T_A = 25°C	0.9	1.1					W/ch
LM1896N-2	V_S = 6V, R_L = 8Ω Bridge Mode, T_A = 25°C		1.8	2.1				W
	V_S = 9V, R_L = 8Ω Dual Mode, T_A = 25°C		1.3					W/ch
LM2896P-1	V_S = 12V, R_L = 8Ω Dual Mode, T_{TAB} = 25°C				2.0	2.5		W/ch
LM2896P-2	V_S = 12V, R_L = 8Ω Bridge Mode, T_{TAB} = 25°C				7.2	9.0		W
	V_S = 9V, R_L = 4Ω Bridge Mode, T_{TAB} = 25°C					7.8		W
	V_S = 9V, R_L = 4Ω Dual Mode, T_{TAB} = 25°C					2.5		W/ch
Distortion	f = 1 kHz							
	P_O = 50 mW		0.09			0.09		%
	P_O = 0.5W		0.11			0.11		%
	P_O = 1W					0.14		%
Power Supply Rejection Ratio (PSRR)	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred, V_{RIPPLE} = 250 mV	−40	−54		−40	−54		dB
Channel Separation	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred	−50	−64		−50	−64		dB
Noise	Equivalent Input Noise R_S = 0,							
	C_{IN} = 0.1 μF, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3	3.2	5.6	6	6.4	V
Input Impedance		50	100	350	50	100	350	kΩ
Input Offset Voltage			5			5		mV
Voltage Difference between Outputs	LM1896N-2, LM2896P-2		10	20		10	20	mV
Input Bias Current			120			120		nA

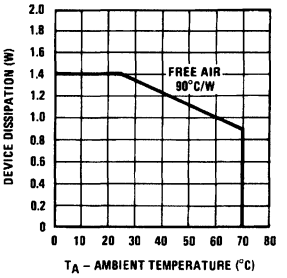
Note 1: For operation at ambient temperature greater than 25°C, the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves

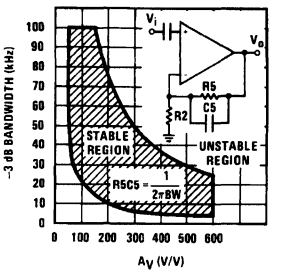
LM2896 Device Dissipation vs Ambient Temperature



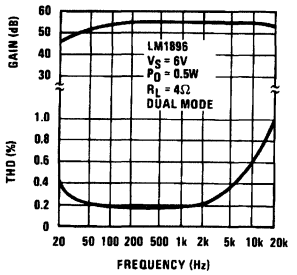
LM1896 Maximum Device Dissipation vs Ambient Temperature



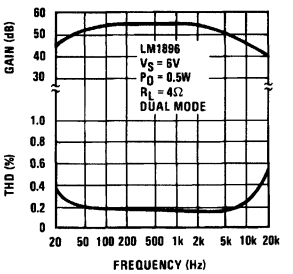
−3 dB Bandwidth vs Voltage Gain for Stable Operation



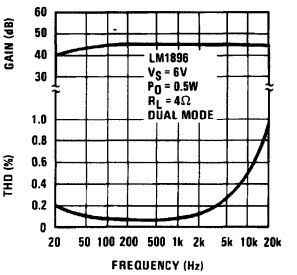
THD and Gain vs Frequency A_V = 54 dB, BW = 30 kHz



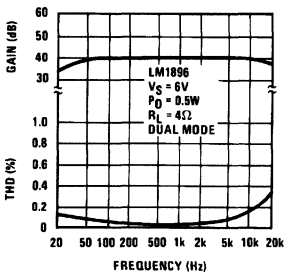
THD and Gain vs Frequency A_V = 54 dB, BW = 5 kHz



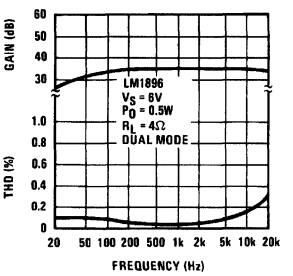
THD and Gain vs Frequency A_V = 46 dB, BW = 50 kHz



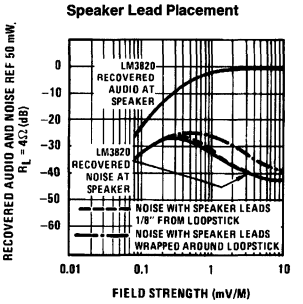
THD and Gain vs Frequency A_V = 40 dB, BW = 20 kHz



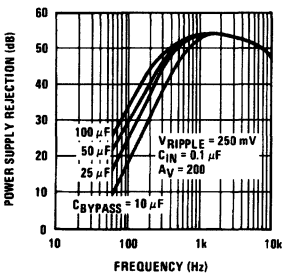
THD and Gain vs Frequency A_V = 34 dB, BW = 50 kHz



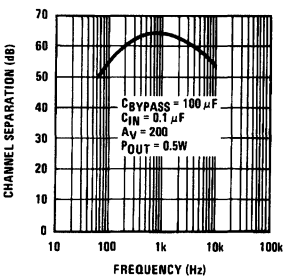
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



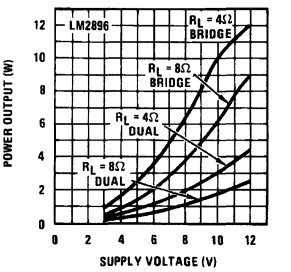
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



Power Output vs Supply Voltage



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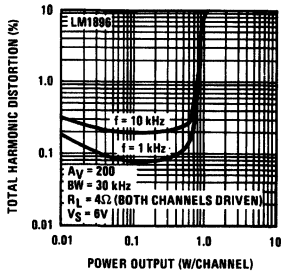
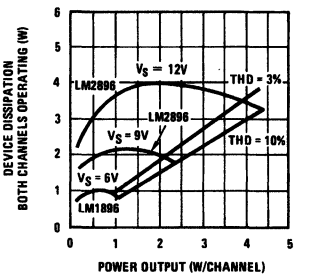
Typical Performance Curves (Continued)

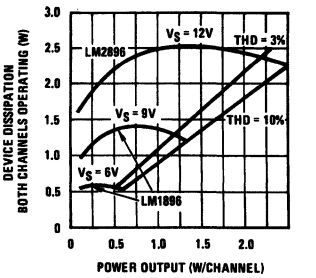
Total Harmonic Distortion vs Power Output



Power Dissipation vs Power Output R_L = 4Ω

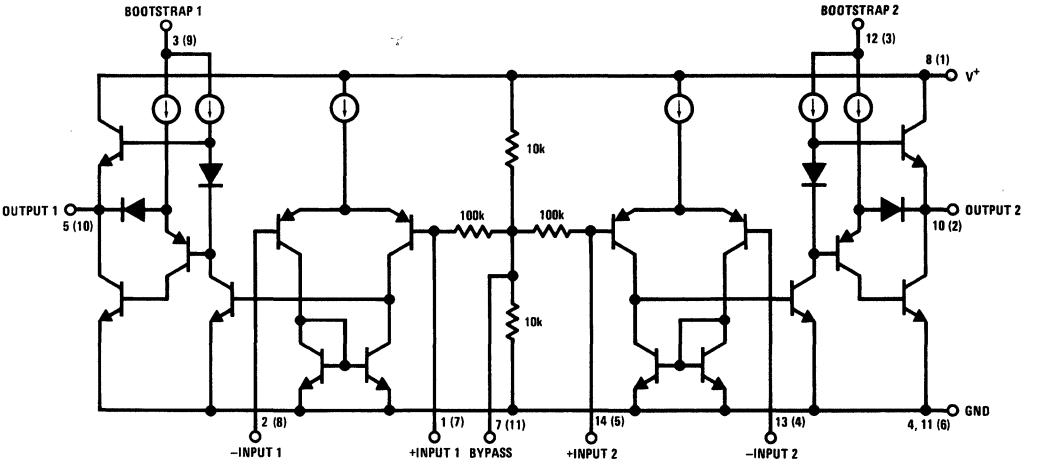


Power Dissipation vs Power Output R_L = 8Ω



TL/H/7920–3

Equivalent Schematic



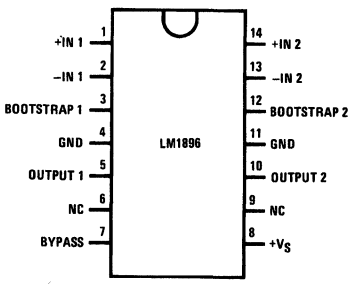
6, 9 No connection on LM1896

( ) indicates pin number for LM2896

TL/H/7920–4

Connection Diagrams

Dual-In-Line Package



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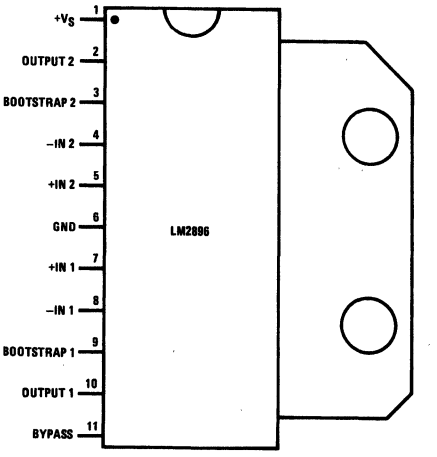
Top View

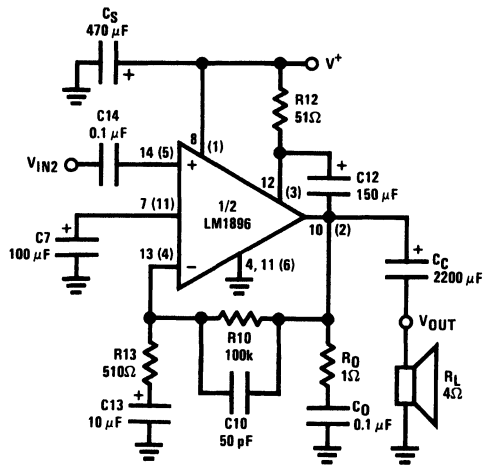
Single-In-Line Package



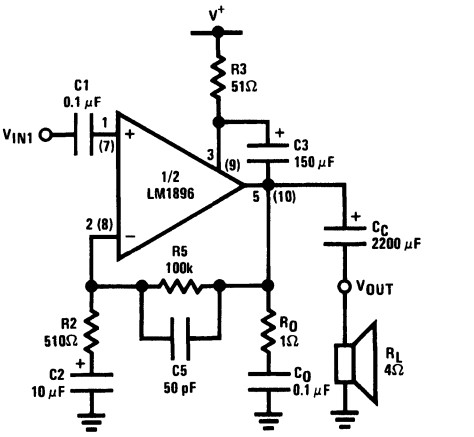
TL/H/7920–6

Top View

Typical Applications (Continued)



TL/H/7920-7



TL/H/7920-8

6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with A_V = 200, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R2, R5, R10, R13	Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.
2. R3, R12	Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S.
3. R_O	Works with C_O to stabilize output stage.
4. C1, C14	Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R_{IN} C1}$
5. C2, C13	Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at: $f_L = \frac{1}{2\pi R2C2}$
6. C3, C12	Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by: $f_L = \frac{1}{2\pi R3C3}$
7. C5, C10	Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.
8. C7	Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.
9. C_C	Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by: $f_L = \frac{1}{2\pi C_C R_L}$
10. C_O	Works with R_O to stabilize output stage.
11. C_S	Provides power supply filtering.

Application Hints

AM Radios

The LM1896/LM2896 has been designed fo fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifer. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V\,\omega_o}{S + \omega_o}$$

$$\text{where } A_V = \frac{R2 + R5}{R2}, \quad \omega_o = \frac{1}{R5C5}$$

A curve of -3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in *Figure 4*.

Amp 1 has a voltage gain set by 1 + R5/R2. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referenced to V_i. The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2\left(1 + \frac{R5}{R2}\right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi\, R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if V_S = 6V and R_L = 8Ω bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20\,R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

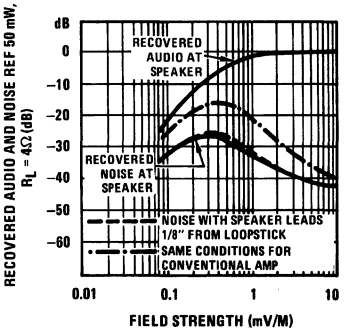
When adjusting the frequency response in the bridge configuration, R5C5 and R10C10 form a 2 pole cascade and the -3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

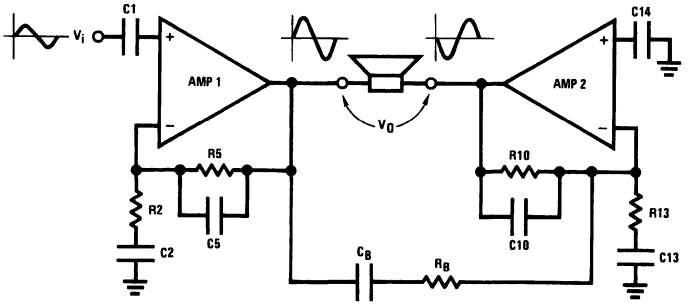
To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. *Figure 1* shows the complete bridge amplifier.



TL/H/7920–9

FIGURE 3. Improved AM Sensitivity over Conventional Design

Application Hints (Continued)



TL/H/7920–10

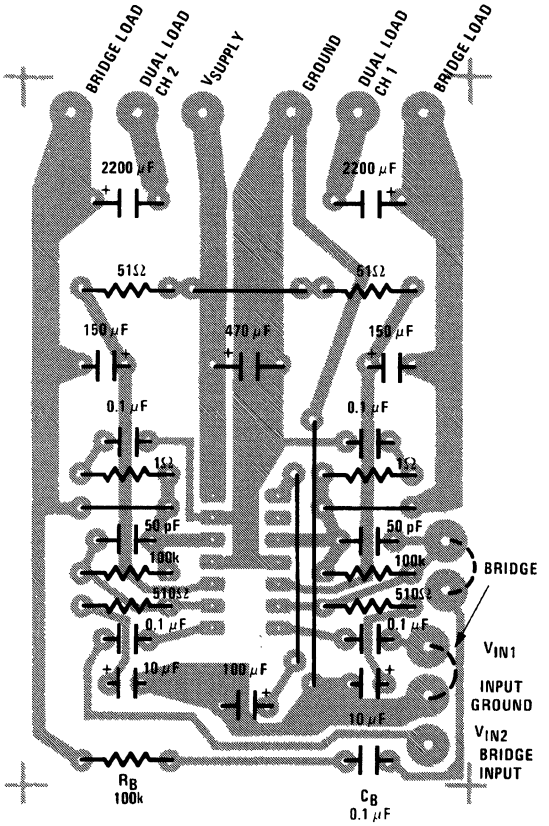
Figure 4. Bridge Amplifier Connection

Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and *Figure 6* show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in less than 50 kΩ to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B, C_B into the PCB.

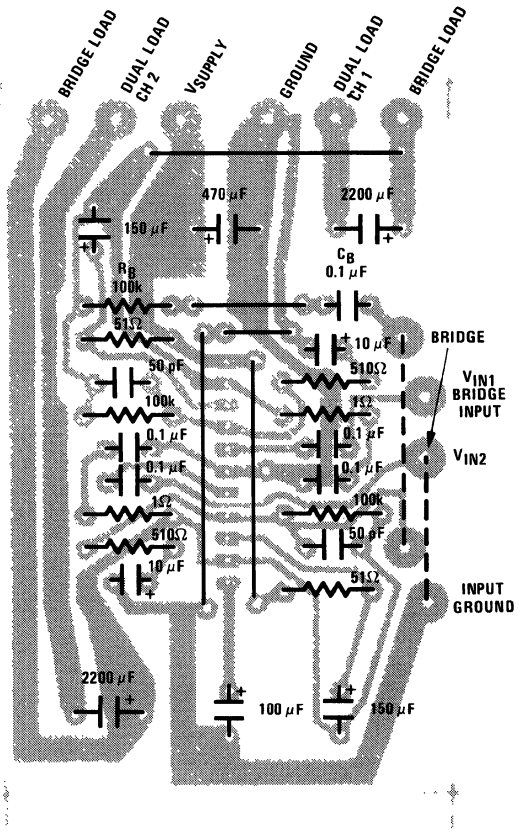
To wire the amplifer into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).



TL/H/7920–11

FIGURE 5. Printed Circuit Board Layout for the LM1896

Printed Circuit Layout (Continued)



TL/H/7920–12

FIGURE 6. Printed Circuit Board Layout for the LM2896

National Semiconductor

LM2877 Dual 4-Watt Power Audio Amplifier

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package.

Features

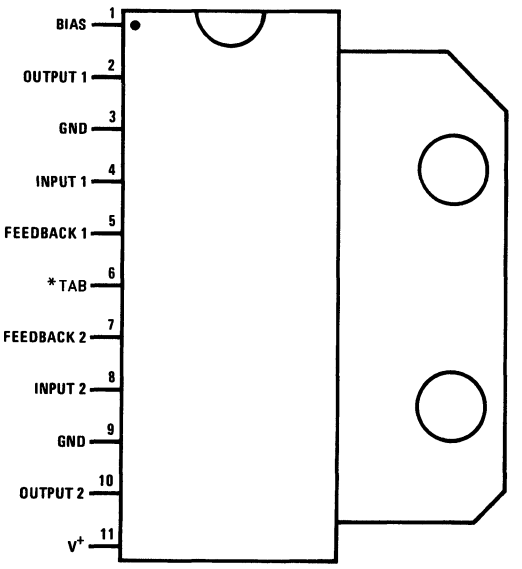
- 4W/channel
- −68 dB ripple rejection, output referred
- −70 dB channel separation, output referred
- Wide supply range, 6-24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

(Single-In-Line Package)



TL/H/7933-1

Top View

Order Number LM2877P
See NS Package Number P11A

*Pin 6 must be connected to GND.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

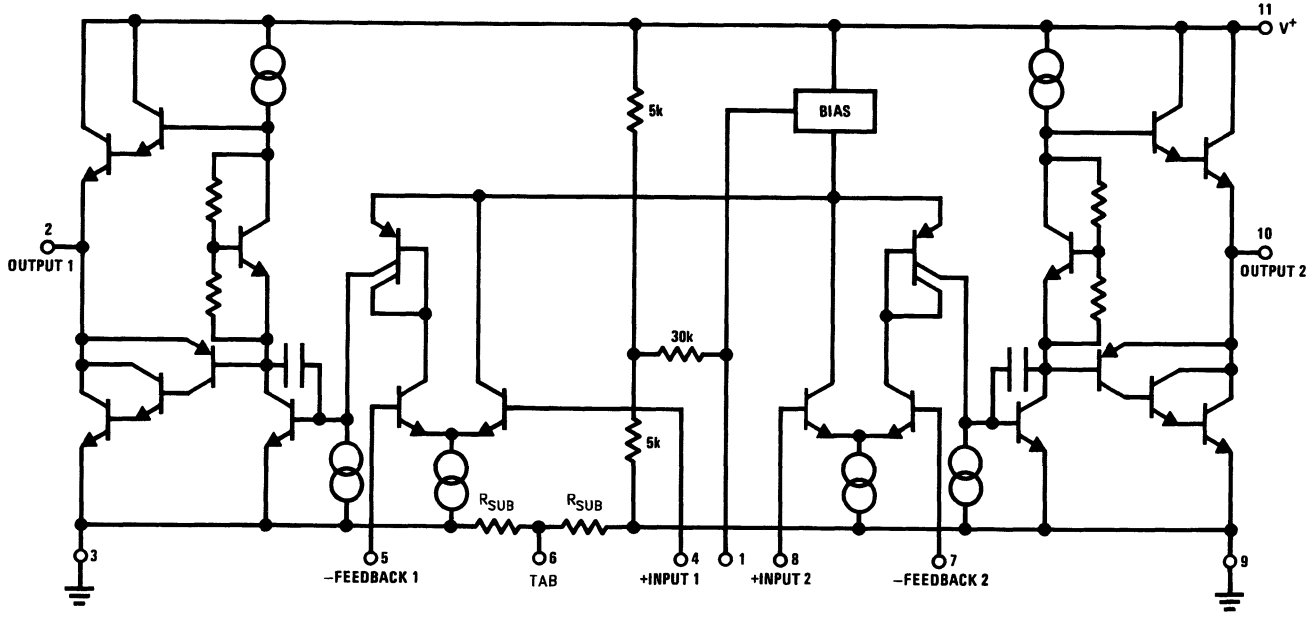
Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics V_S = 20V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Operating Supply Voltage		6		24	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C				
	V_S = 20V	4.0	4.5		W
	V_S = 18V		3.6		W
	V_S = 12V, R_L = 4Ω	1.5	1.9		W
Distortion, THD	f = 1 kHz, V_S = 20V				
	P_O = 50 mW/Channel		0.1		%
	P_O = 1W/Channel		0.07	1	%
	P_O = 2W/Channel		0.07		%
	f = 1 kHz, V_S = 12V, R_L = 4Ω				
	P_O = 50 mW/Channel		0.25		%
	P_O = 500 mW/Channel		0.20		%
	P_O = 1W/Channel		0.15	1	%
Output Swing	R_L = 8Ω		V_S−4		V_{p-p}
Channel Separation	C_F = 50 μF, C_{IN} = 0.1 μF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply	C_F = 50 μF, C_{IN} = 0.1 μF, f = 120 Hz				
Rejection Ratio	Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−68		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 μF, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.80		mV
Open Loop Gain	R_S = 0, f = 1 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

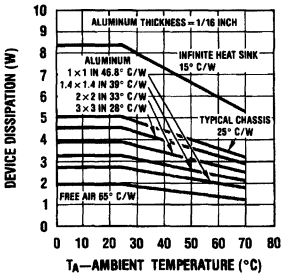
Equivalent Schematic Diagram



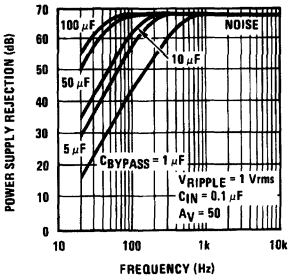
TL/H/7933–2

Typical Performance Characteristics

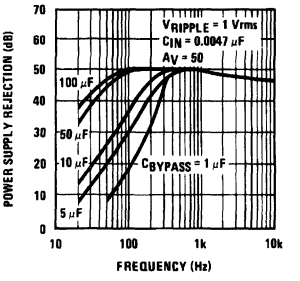
Device Dissipation vs Ambient Temperature



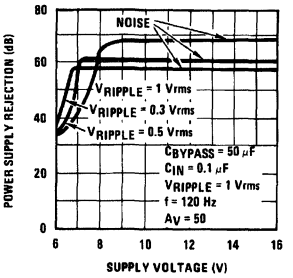
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



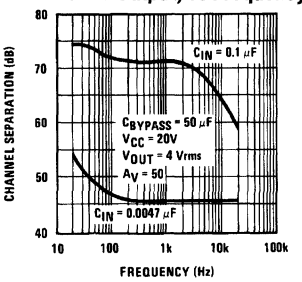
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



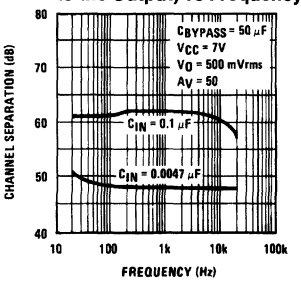
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



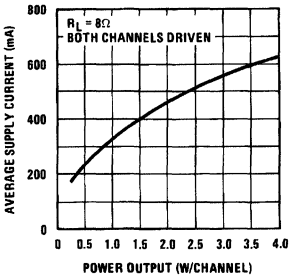
Channel Separation (Referred) to the Output) vs Frequency



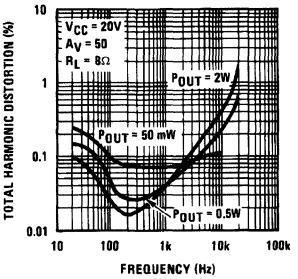
Channel Separation (Referred) to the Output) vs Frequency



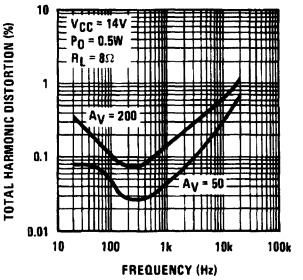
Average Supply Current vs Power Output



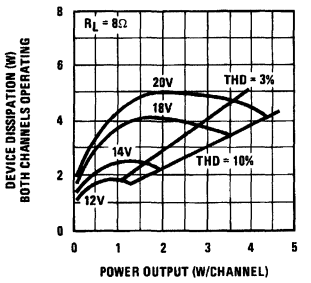
Total Harmonic Distortion vs Frequency



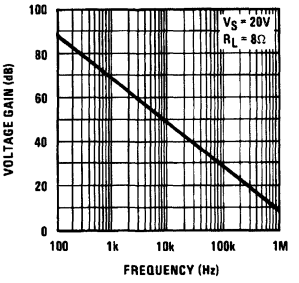
Total Harmonic Distortion vs Frequency



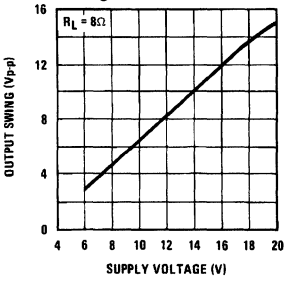
Power Dissipation vs Power Output



Open Loop Gain vs Frequency



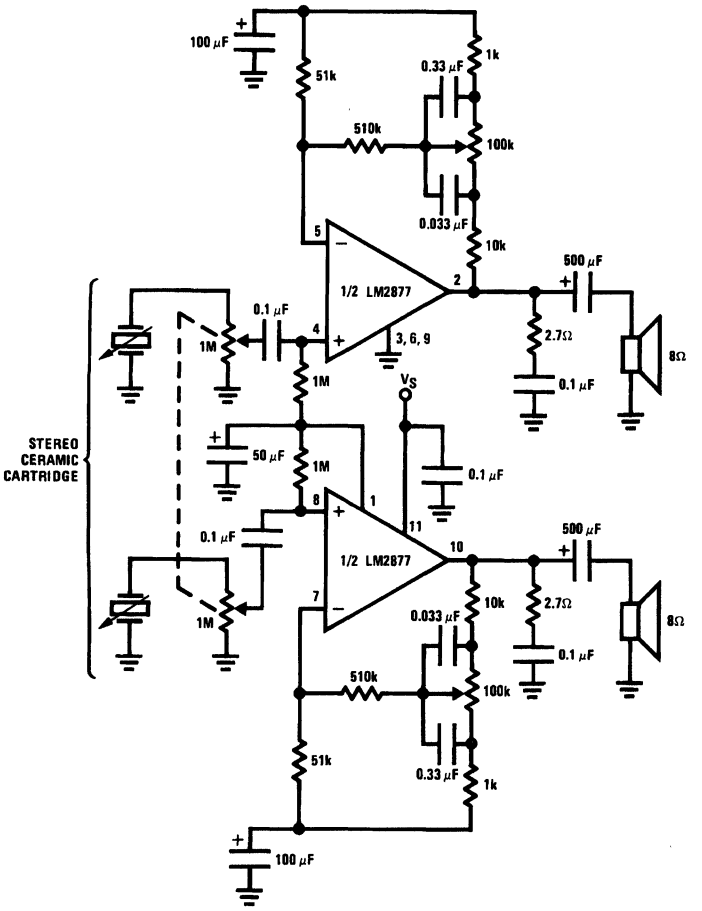
Output Swing vs Supply Voltage



TL/H/7933–3

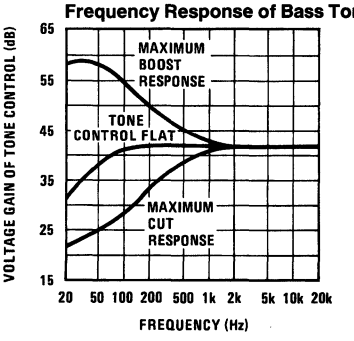
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/7933–4

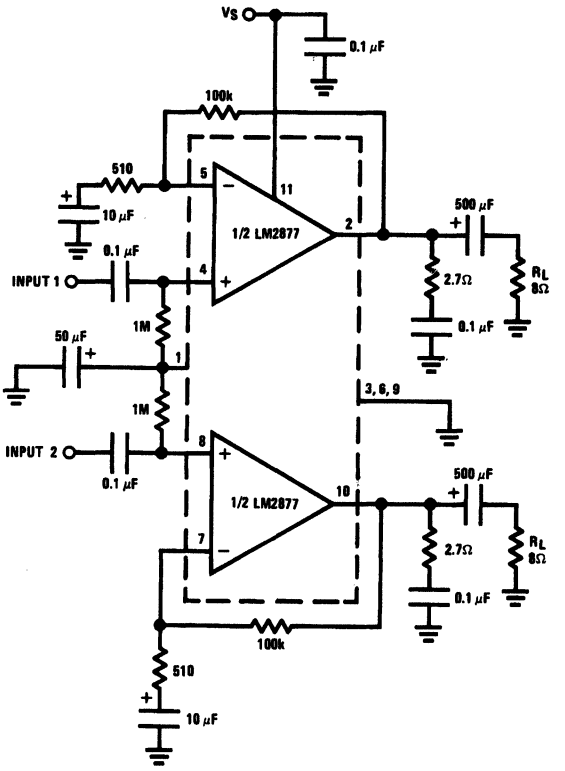
Frequency Response of Bass Tone Control



TL/H/7933–5

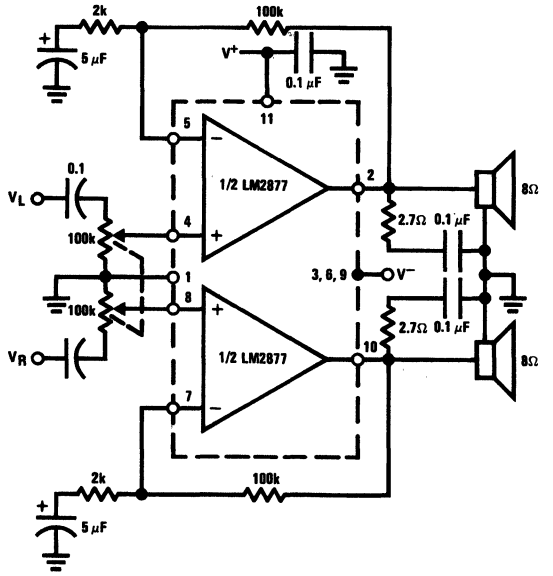
Typical Applications (Continued)

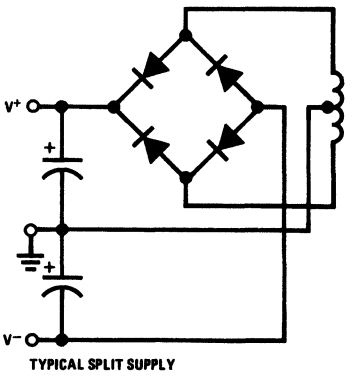
Stereo Amplifier with $A_V = 200$



TL/H/7933-6

Non-Inverting Amplifier Using Split Supply



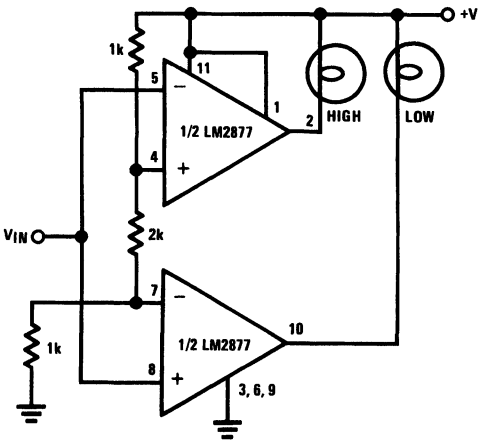


TYPICAL SPLIT SUPPLY

TL/H/7933-7

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TL/H/7933–8

Truth Table

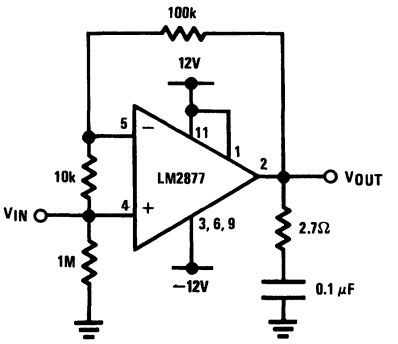
V_{IN}	High	Low
$<1/4\ V^+$	Off	On
$1/4\ V^+$ to $3/4\ V^+$	Off	Off
$>3/4\ V^+$	On	Off

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless, the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.



TL/H/7933–9

FIGURE 1

National Semiconductor

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

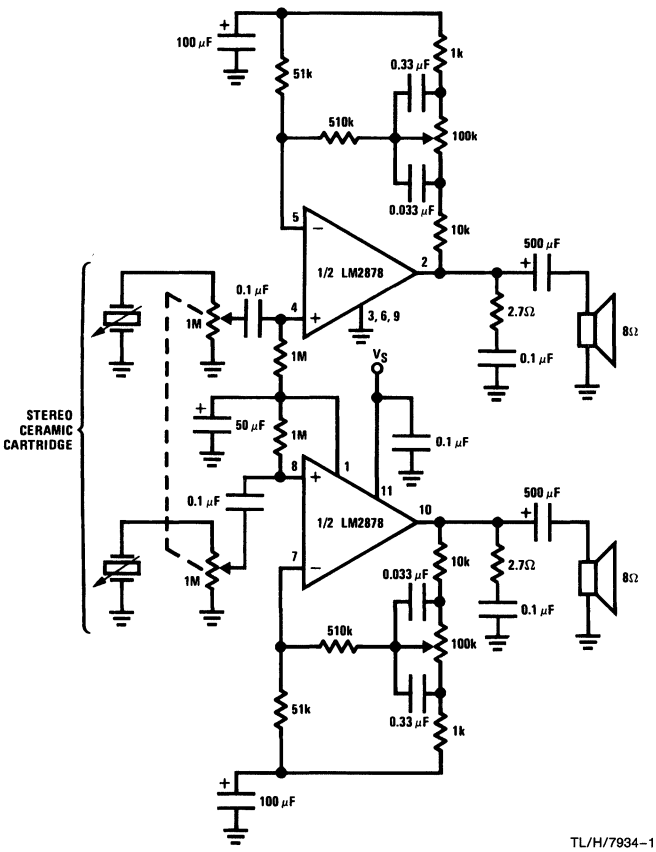
Features

- Wide operating range 6V–32V
- 5W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

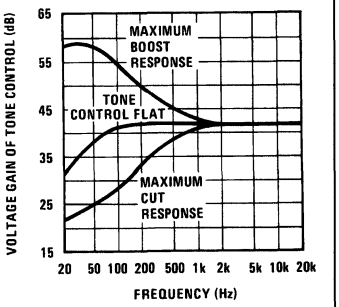
Typical Applications



TL/H/7934–1

FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Frequency Response of Bass Tone Control



TL/H/7934–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics V_S = 22V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

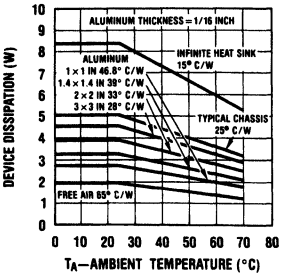
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		10	50	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C	5	5.5		W
Distortion	f = 1 kHz, R_L = 8Ω P_O = 50 mW		0.20		%
	P_O = 0.5W		0.15		%
	P_O = 2W		0.14		%
Output Swing	R_L = 8Ω		V_S − 6V		Vp-p
Channel Separation	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 1 kHz, Output Referred V_O = 4 Vrms	−50	−70		dB
PSRR Power Supply Rejection Ratio	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 120 Hz, Output Referred V_{ripple} = 1 Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise R_S = 0, C_{IN} = 0.1 μF BW = 20 − 20 kHz		2.5		μV
	CCIR•ARM		3.0		μV
	Output Noise Wideband R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.8		mV
Open Loop Gain	R_S = 51Ω, f = 1 kHz, R_L = 8Ω		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	V_S = 22V	10	11	12	V
Slew Rate			2		V/μS
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: ±0.7V applies to audio applications; for extended range, see Application Hints.

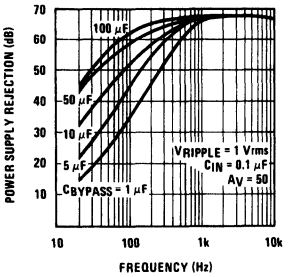
Note 2: For operation at ambient temperature greater than 25°C, the LM2878 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

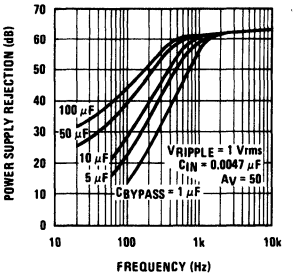
Device Dissipation vs Ambient Temperature



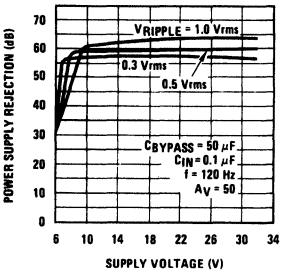
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



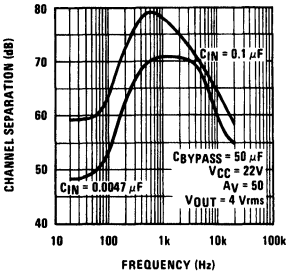
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



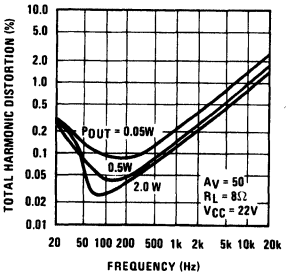
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



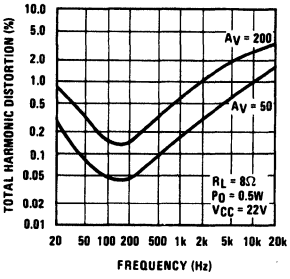
Channel Separation (Referred to the Output) vs Frequency



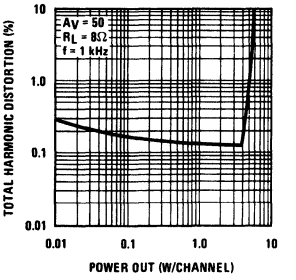
Total Harmonic Distortion vs Frequency



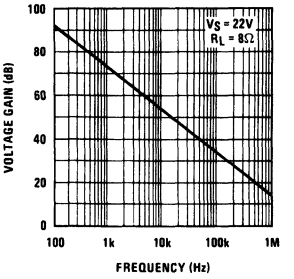
Total Harmonic Distortion vs Frequency



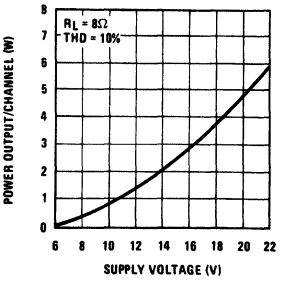
Total Harmonic Distortion vs Power Out



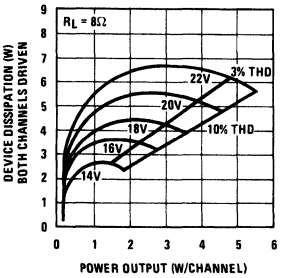
Open Loop Gain vs Frequency



Power Output/Channel vs Supply Voltage

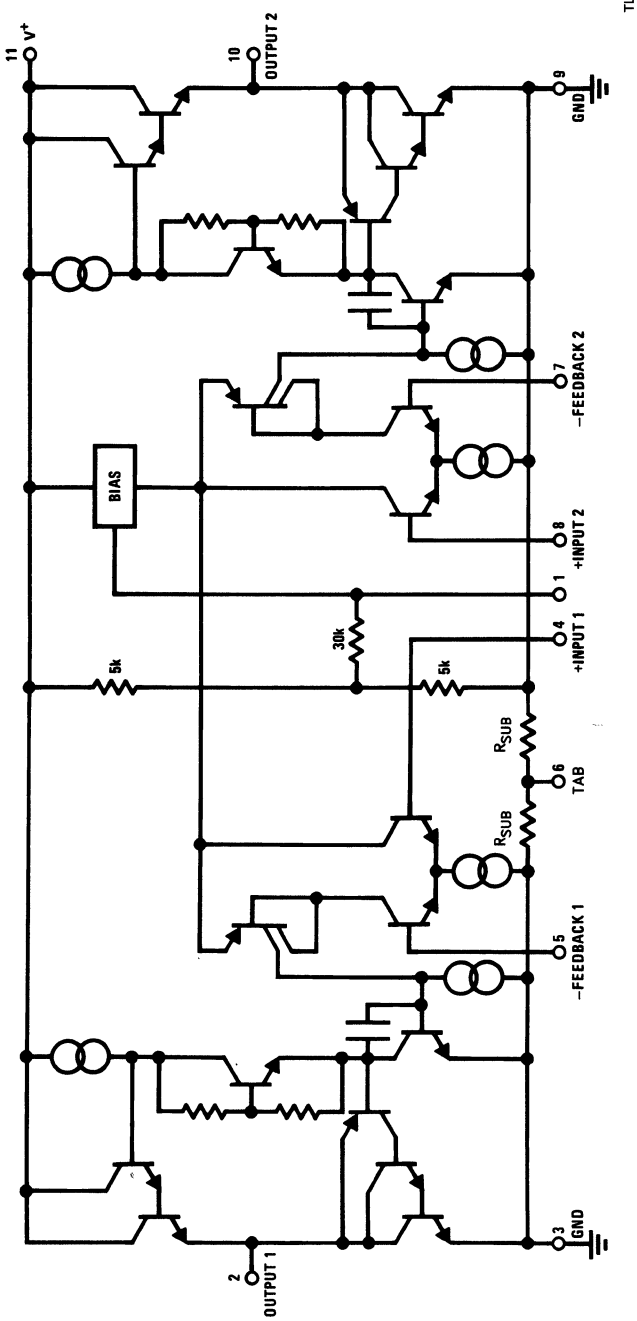


Power Dissipation vs Power Out



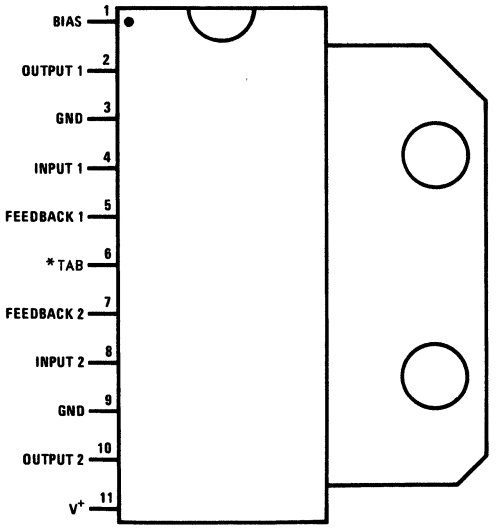
TL/H/7934–3

Equivalent Schematic Diagram



Connection Diagram

Single-In-Line Package



TL/H/7934–5

Top View

*Pin 6 must be connected to GND.

Order Number LM2878P
See NS Package Number P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.

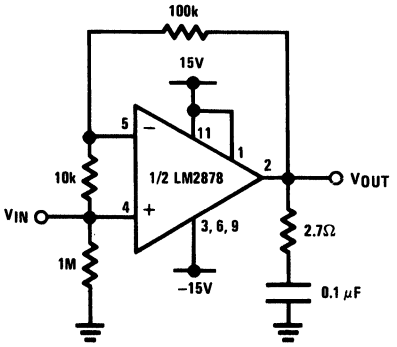


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FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components *(Figure 3)*

1. R2, R5, R7, R10 Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2. R4, R8 Resistors set input impedance and supply bias current for the positive input.
3. R_O Works with C_O to stabilize output stage.
4. C1 Improves power supply rejection (see Typical Performance Characteristics).
5. C11 Stabilizes amplifier, may need to be larger depending on power supply filtering.
6. C4, C8 Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R4C4}$$

7. C5, C7 Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at:

$$f_L = \frac{1}{2\pi R5C5}$$

8. C_O Works with R_O to stabilize output stage.
9. C2, C10 Output coupling capacitor. Low frequency pole given by:

$$f_L = \frac{1}{R\pi RLC2}$$

Typical Applications (Continued)

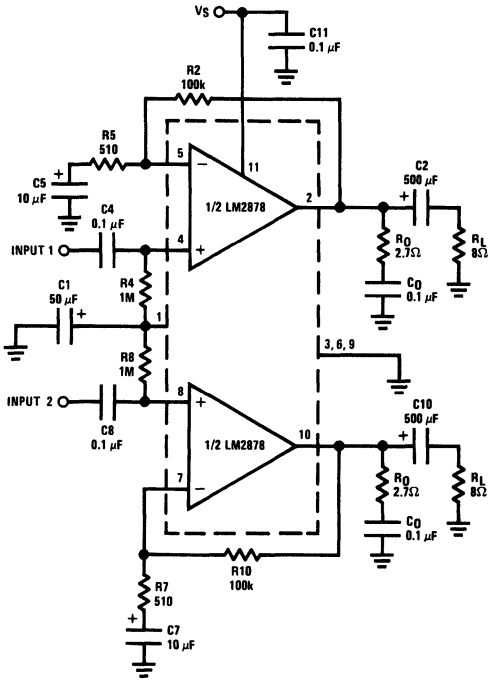

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FIGURE 3. Stereo Amplifier with $A_V = 200$

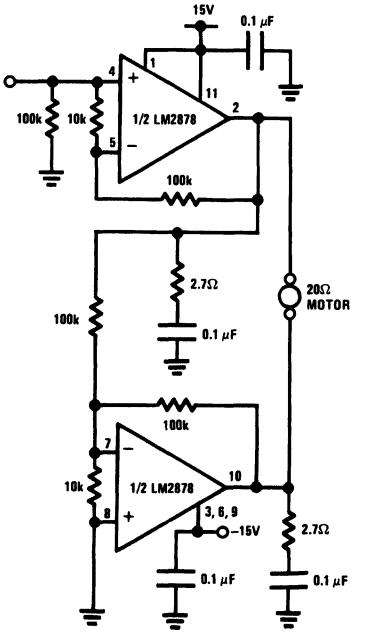

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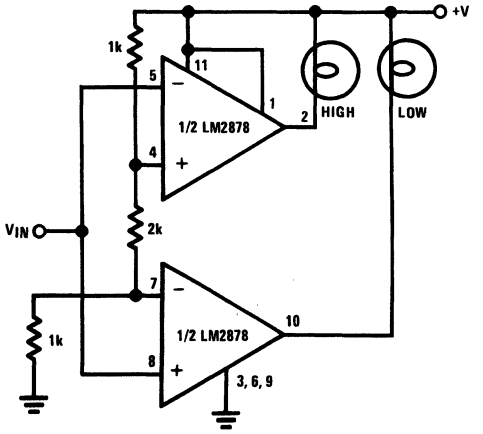
FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

Typical Applications (Continued)



Truth Table

V_{IN}	High	Low
$<\frac{1}{4}V^+$	Off	On
$\frac{1}{4}V^+$ to $\frac{3}{4}V^+$	Off	Off
$>\frac{3}{4}V^+$	On	Off

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FIGURE 5. Window Comparator Driving High, Low Lamps

National Semiconductor

LM2879 Dual 8-Watt Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 8W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown.

Features

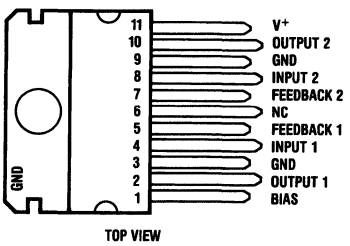
- A_{VO} typical 90 dB
- 9W per channel (typical)
- 60 dB ripple rejection
- 70 dB channel separation
- Self-centering biasing
- 4 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram and Typical Application

Plastic Package

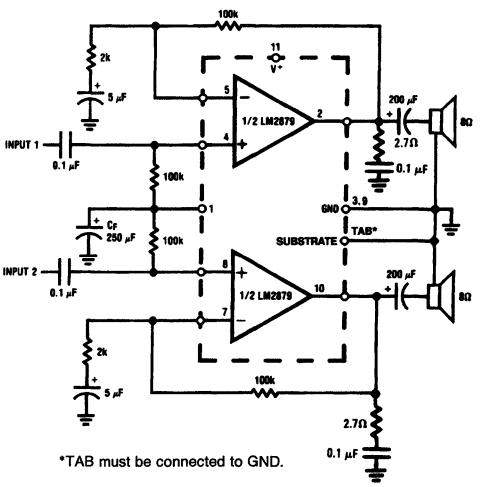


TOP VIEW

TL/H/5291–1

Order Number LM2879T
See NS Package Number TA11B

Stereo Amplifier



*TAB must be connected to GND.

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FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to + 70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

Electrical Characteristics $V_S = 28V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

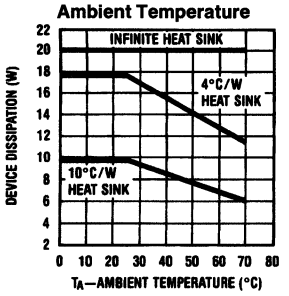
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		12	65	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	6	8		W
Distortion	f = 1 kHz, $R_L = 8\Omega$ $P_O = 1$ W/Channel		0.05	1	%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred $V_O = 4$ Vrms	−50	−70		dB
PSRR Positive Supply	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred $V_{ripple} = 1$ Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$ BW = 20 − 20 kHz CCIR•ARM Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		 2.5 3.0 0.8		 μV μV mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 28V$		14		V
Slew Rate			2		V/μs
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: The input voltage range is normally limited to ±0.7V with respect to pin 1. This range may be extended by shorting pin 1 to the positive supply.

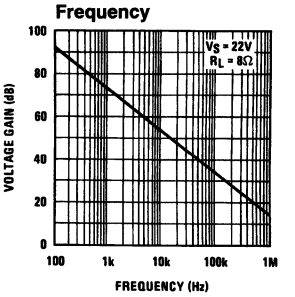
Note 2: For operation at ambient temperature greater than 25°C, the LM2879 must be derated based on a maximum 150°C junction temperature. Thermal resistance, junction to case, is 3°C/W. Thermal resistance, case to ambient, is 40°C/W.

Typical Performance Characteristics

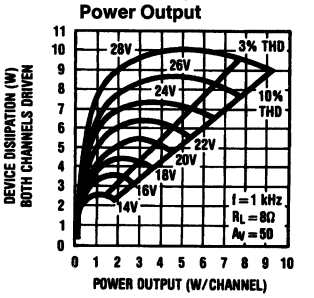
Device Dissipation vs Ambient Temperature



Open Loop Gain vs Frequency



Power Dissipation vs Power Output



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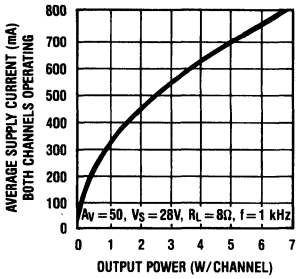
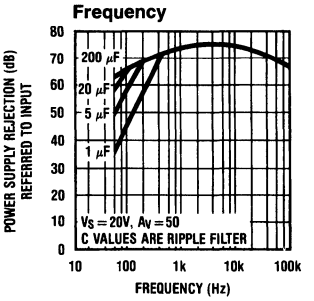
Typical Performance Characteristics (Continued)

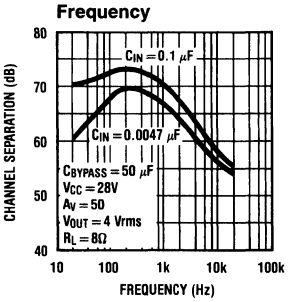
Supply Current vs Output Power



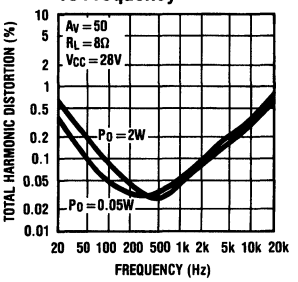
Supply Rejection vs Frequency



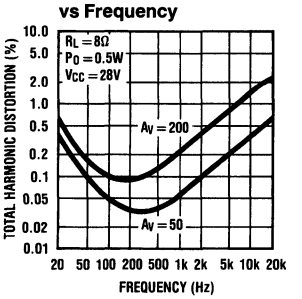
Channel Separation (Referred to the Output) Frequency



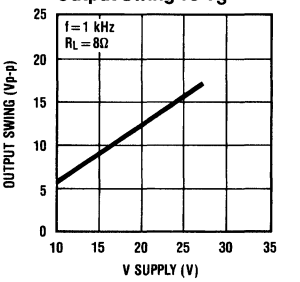
Total Harmonic Distortion vs Frequency



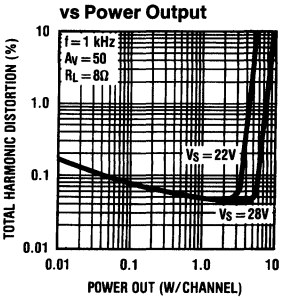
Total Harmonic Distortion vs Frequency



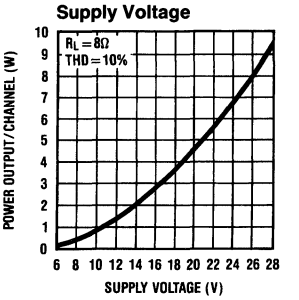
Output Swing vs V_S



Total Harmonic Distortion vs Power Output

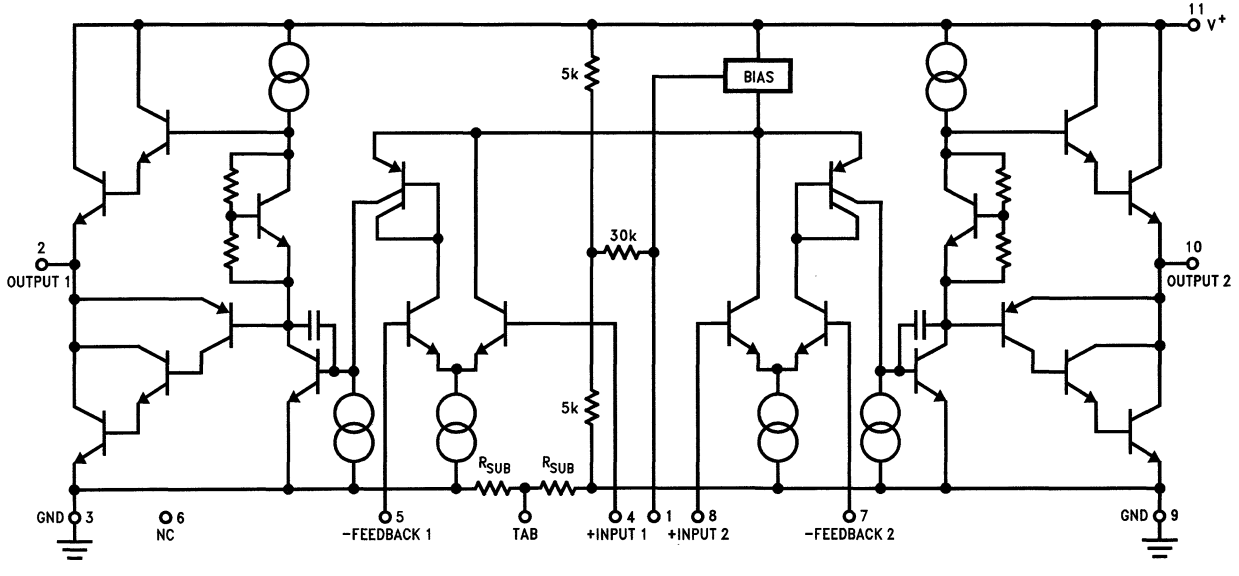


Power Output/Channel vs Supply Voltage



TL/H/5291–4

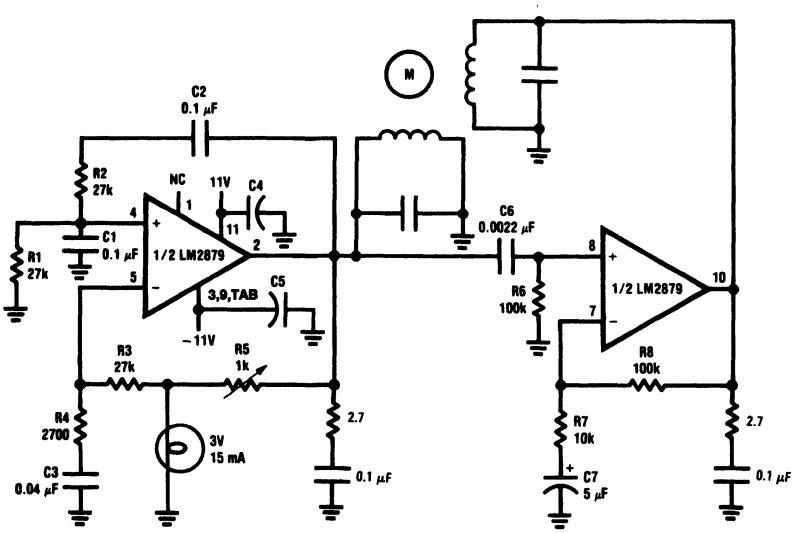
Equivalent Schematic Diagram



TL/H/5291–5

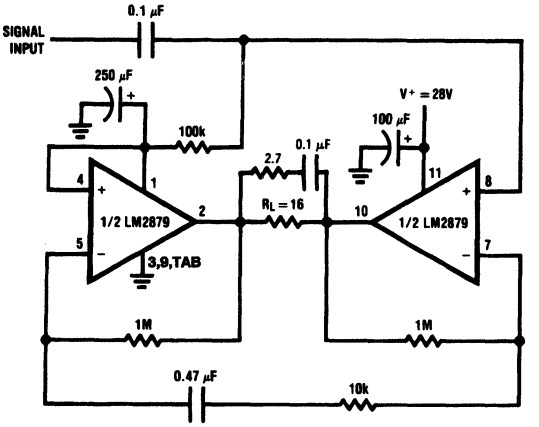
Typical Applications

Two-Phase Motor Drive



TL/H/5291–6

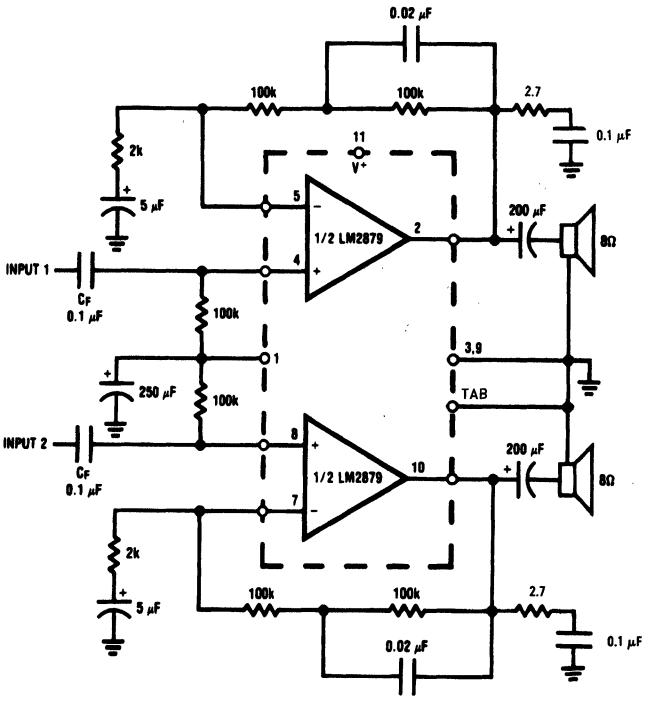
12W Bridge Amplifier



TL/H/5291–7

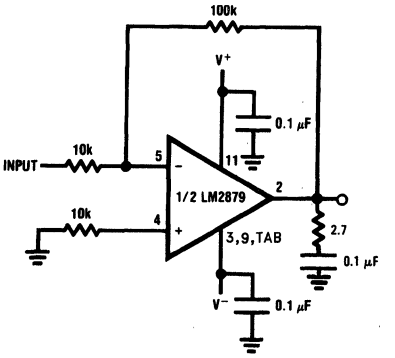
Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost



TL/H/5291–8

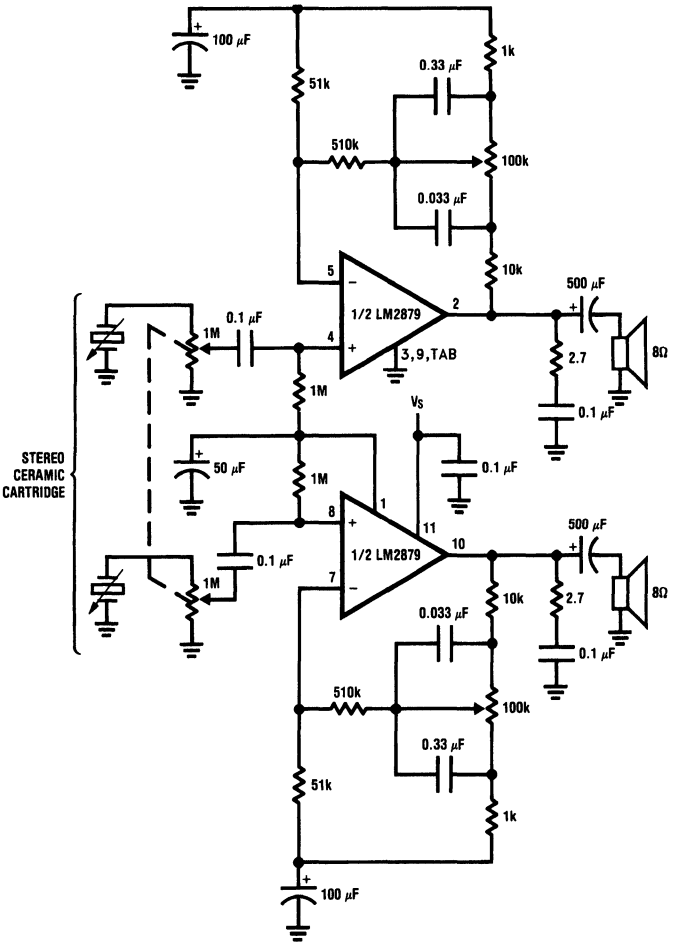
Power Op Amp (Using Split Supplies)



TL/H/5291–9

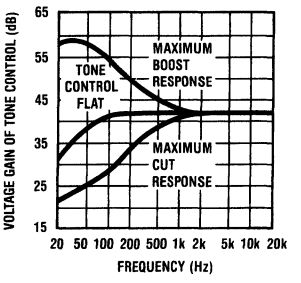
Typical Applications (Continued)

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/5291–10

Frequency Response of Bass Tone Control



TL/H/5291–11

National Semiconductor

ADVANCE INFORMATION

LM3875
High Performance 40W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier. It is capable of delivering 40W to an 8Ω load. It is fully protected using circuit techniques similar to those found in the LM12.

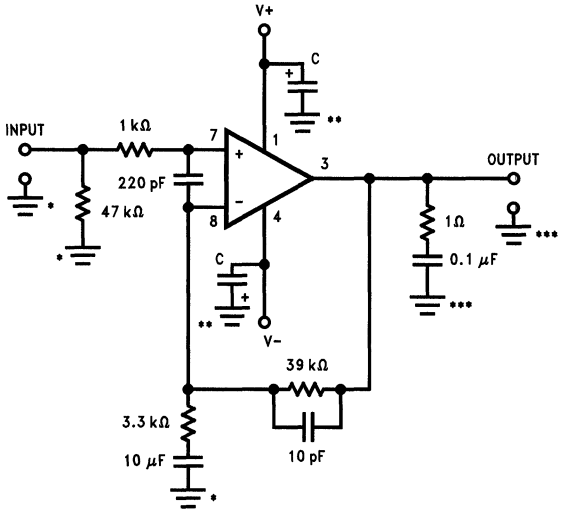
The output stage is protected from a short to ground or to the supplies. Protection against transients from inductive loads is provided at the output stage via internal clamp diodes. The LM3875 also contains thermal shutdown protection against operation outside its operating temperature range.

The LM3875 is internally compensated and stable for gains ≥10.

Features

- 40W output power into 8Ω
- Over-voltage protection
- Dynamic Safe Area Protection
- Fully protected from AC and DC short-circuits
- 11-lead TO-220 package
- Under-voltage shutdown

Typical Application



TL/H/11449–1

C—Power supply bypass using low ESR 680 μF electrolytic, 10 μF electrolytic, and 0.1 ceramic chip capacitor.

Ground Connections

*Input signal ground.

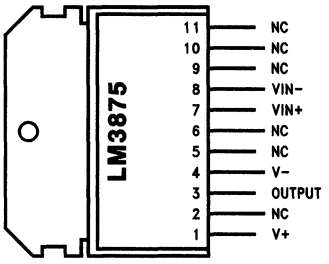
**Power supply bypass ground.

***Output signal ground.

These three ground connections should have separate return paths to the power supply ground ("star ground").

Connection Diagram

Plastic Package



TL/H/11449–2

Top View

Order Number LM3875CCT
See NS Package Number T11A

National Semiconductor

ADVANCE INFORMATION

LM3876
High Performance 40W Audio Power Amplifier

General Description

The LM3876 is a high-performance audio power amplifier with an output mute that eliminates turn-on and turn-off transients. It is capable of delivering 40W to an 8Ω load. It is fully protected using circuit techniques similar to those found in the LM12.

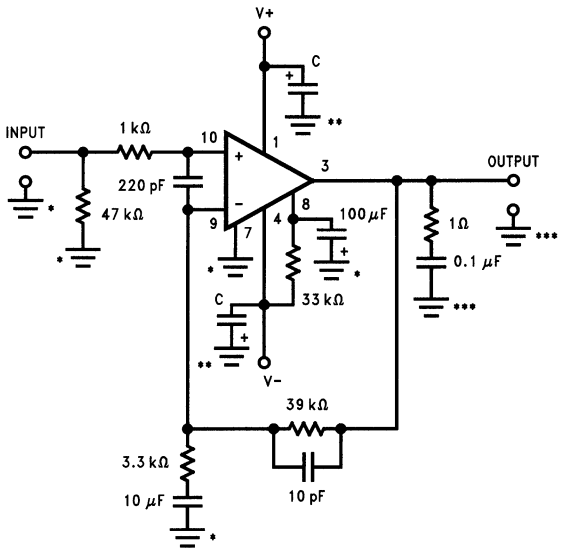
The output stage is protected from a short to ground or to the supplies. Protection against transients from inductive loads is provided at the output stage via internal clamp diodes. The LM3876 also contains thermal shutdown protection against operation outside its operating temperature range.

The LM3876 is internally compensated and stable for gains ≥10.

Features

- 40W continuous output power into 8Ω
- Turn-on and turn-off mute
- Over-voltage protection
- Dynamic Safe Area Protection
- Fully protected from AC and DC short-circuits
- 11-lead TO-220 package
- Under-voltage shutdown

Typical Application



TL/H/11450–1

C—Power supply bypass using low ESR 680 μF electrolytic, 10 μF electrolytic, and 0.1 ceramic chip capacitor.

Mute—In this example, the mute pin is tied high

Ground Connections

*Input signal ground.

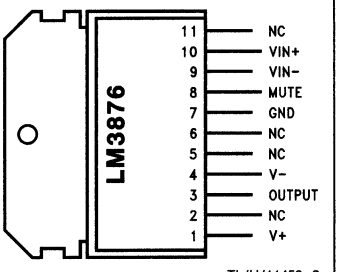
**Power Supply bypass ground.

***Output signal ground.

These three ground connections should have separate return paths to the power supply ground ("star ground").

Connection Diagram

Plastic Package



TL/H/11450–2

Top View

Order Number LM3876CCT
See NS Package Number T11A

National Semiconductor

LMC835 Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ±12 dB or ±6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μP-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

Features

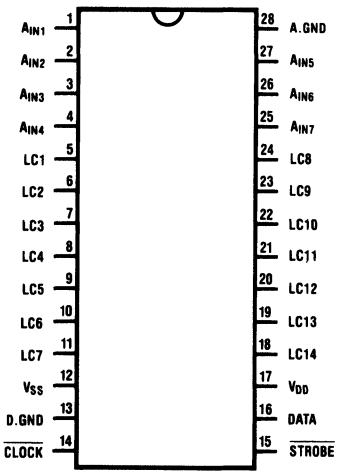
- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ±12 dB or ±6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

Connection Diagrams

Dual-In-Line Package

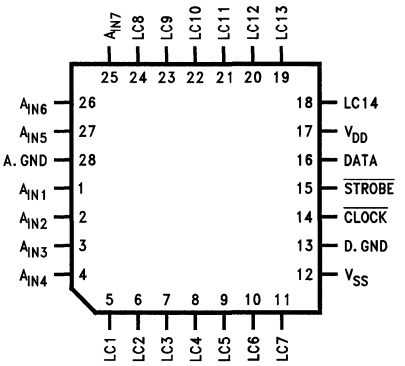


TL/H/6753-1

Top View

Order Number LMC835N
See NS Package N28B

Molded Chip Carrier Package

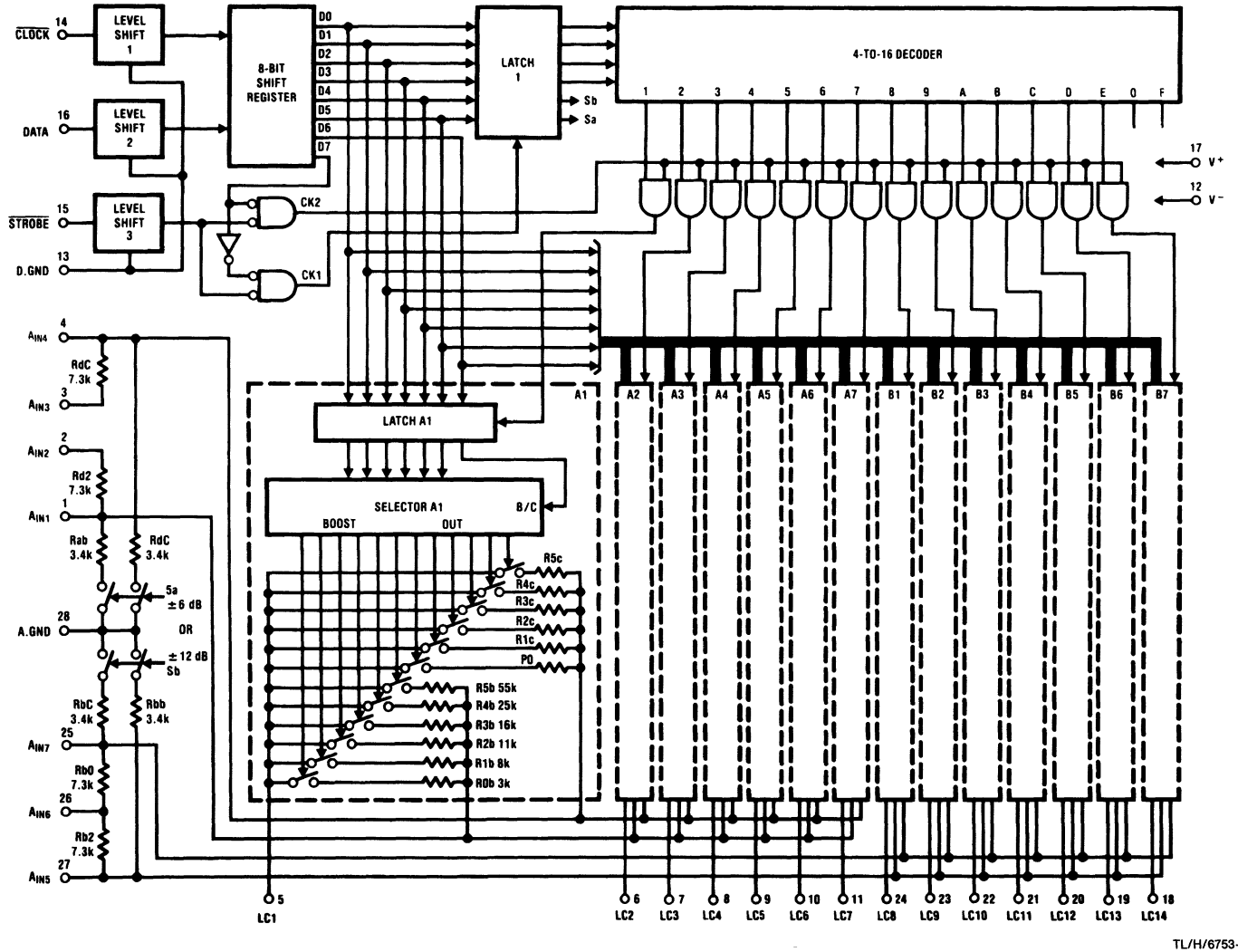


TL/H/6753-26

Top View

Order Number LMC835V
See NS Package V28A

Block Diagram



TL/H/6753–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_{DD}-V_{SS}$	18V
Allowable Input Voltage (Note 1)	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{stg}	−60°C to +150°C
Lead Temperature (Soldering, 10 sec), N Pkg	+260°C
Lead Temperature, V Pkg	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

Operating Ratings

Supply Voltage, $V_{DD}-V_{SS}$	5V to 16V
Digital Ground (Pin 13)	V_{SS} to V_{DD}
Digital Input (Pins 14, 15, 16)	V_{SS} to V_{DD}
Analog Input (Pins 1, 2, 3, 4, 25, 26, 27) (Note 1)	V_{SS} to V_{DD}
Operating Temperature, T_{opr}	−40°C to +85°C

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, A.GND=0V

LOGIC SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
I_{DDL}	Supply Current	Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{SSL}		Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{DDH}		Pins 14, 15, 16 are 5V	1.3	5	**5**	mA (Max)
I_{SSH}		Pins 14, 15, 16 are 5V	0.9	5	**5**	mA (Max)
V_{IH}	High-Level Input Voltage	@Pins 14, 15, 16	1.8	2.3	**2.5**	V (Min)
V_{IL}	Low-Level Input Voltage	@Pins 14, 15, 16	0.9	0.6	**0.4**	V (Max)
f_o	Clock Frequency	@Pin 14	2000	500	**500**	kHz (Max)
$t_{w(\overline{STB})}$	Width of $\overline{STB}$ Input	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{setup}	Data Setup Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{hold}	Data Hold Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{cs}	Delay from Rising Edge of $\overline{CLOCK}$ to $\overline{STB}$	See *Figure 1*	0.25	1	**1**	μs (Min)
I_{IN}	Input Current	@Pins 14, 15, 16 $0V<V_{IN}<5V$	±0.01	±1		μA (Max)
C_{IN}	Input Capacitance	@Pins 14, 15, 16 f=1 MHz	5			pF

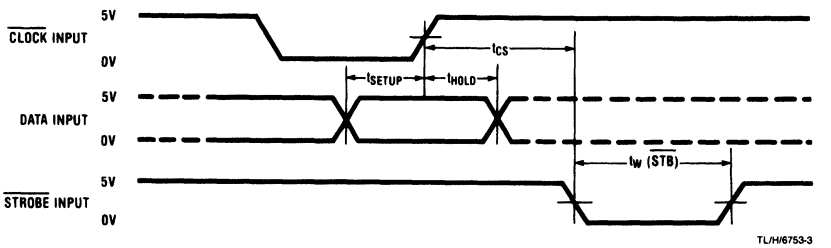
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Bold numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagram



TL/H/6753-3

Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 1

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V

SIGNAL PATH SECTION

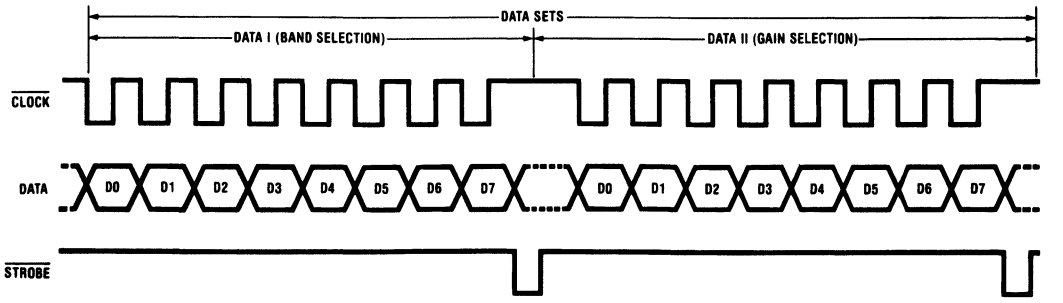
Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
E_A	Gain Error	$A_V=0$ dB @ ± 12 dB Range	0.1	0.5	**0.5**	dB (Max)
		$A_V=0$ dB @ ± 6 dB Range	0.1	1	**1**	dB (Max)
		$A_V=\pm1$ dB @ ± dB Range (R_{5b} or R_{5c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm2$ dB @± 12 dB Range (R_{4b} or R_{4c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm3$ dB @± 12 dB Range (R_{3b} or R_{3c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm4$ dB @± 12 dB Range (R_{2b} or R_{2c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm5$ dB @±12 dB Range (R_{1b} or R_{1c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm9$ dB @± 12 dB Range (R_{0b} or R_{0c} is ON)	0.2	1	**1.3**	dB (Max)
THD	Total Harmonic Distortion	$A_V=0$ dB @±12 dB Range $V_{IN}=4V_{rms}$, f=1 kHz	0.0015			%
		$A_V=12$ dB @ ± 12 dB Range				
		$V_{IN}=1V_{rms}$, f=1 kHz	0.01	0.1		% (Max)
		$V_{IN}=1V_{rms}$, f=20 kHz	0.1	0.5		% (Max)
		$A_V=-12$ dB @ ±12 dB Range				
		$V_{IN}=4V_{rms}$, f=1 kHz	0.01	0.1		% (Max)
		$V_{IN}=4V_{rms}$, f=20 kHz	0.1	0.5		% (Max)
$V_{O\ Max}$	Maximum Output Voltage	$A_V=0$ dB @ ±12 dB Range THD <1%, f=1 kHz	5.5	5.1	**5**	V_{rms} (Min)
S/N	Signal to Noise Ratio	$A_V=0$ dB @ ±12 dB Range $V_{ref}=1\ V_{rms}$	114			dB
		$A_V=12$ dB @ ±12 dB Range $V_{ref}=1V_{rms}$	106			dB
		$A_V=-12$ dB @ ±12 dB Range $V_{ref}=1V_{rms}$	116			dB
I_{LEAK}	Leakage Current	$A_V=0$ dB @ ±12 dB Range (All internal switches are OFF)				
		Pin 2+3, Pin 26		500		nA (Max)
		Pin 5~Pin 11, Pin 18~Pin 24		50		nA (Max)

Note 2; Boldface numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagrams



TL/H/6753–4

Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 2

Truth Tables

DATA I (Band Selection)

D7	D6	D5	D4	D3	D2	D1	D0	
H	X	L	L	L	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	L	L	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 1
H	X	L	L	L	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 2
H	X	L	L	L	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 3
H	X	L	L	L	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 4
H	X	L	L	L	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 5
H	X	L	L	L	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 6
H	X	L	L	L	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 7
H	X	L	L	H	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 8
H	X	L	L	H	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 9
H	X	L	L	H	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 10
H	X	L	L	H	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 11
H	X	L	L	H	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 12
H	X	L	L	H	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 13
H	X	L	L	H	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 14
H	X	L	L	H	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	H	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
H	X	H	L	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 12 dB Range, Band 1 ~ 14
H	X	H	H	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
↑ ①	↑ ②	↑ ③	↑ ④	← Band Code →				

(Ch A: Band 1 ~ 7, Ch B: Band 8 ~ 14)

① DATA 1
② Don't Care
③ Ch A ±6 dB/±12 dB Range
④ Ch B ±6 dB/±12 dB Range

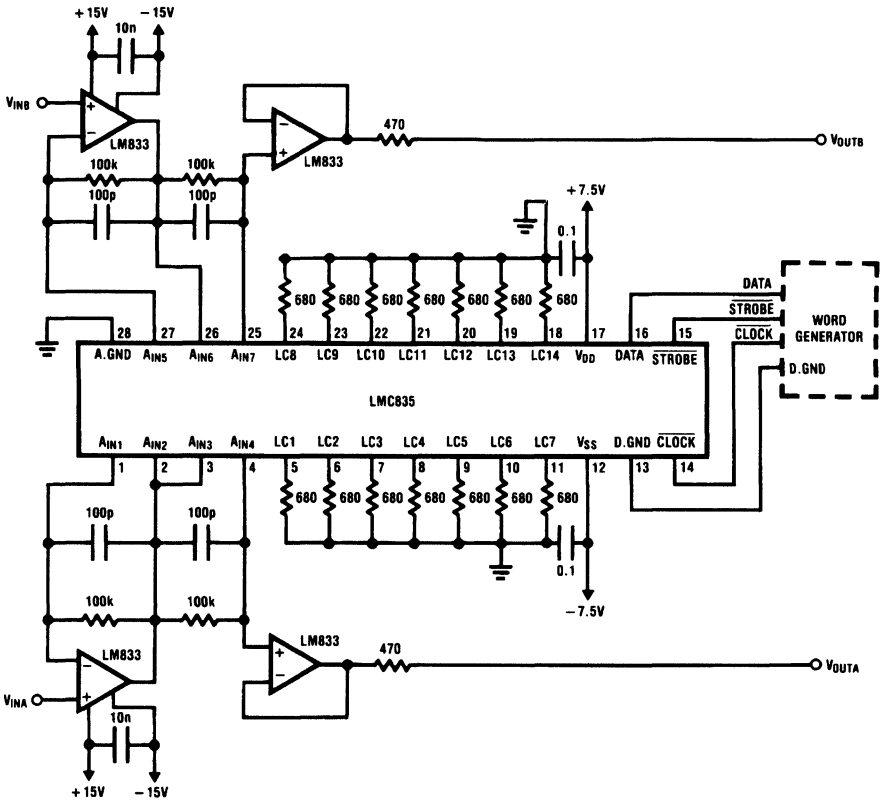
DATA II (Gain Selection)

	D7	D6	D5	D4	D3	D2	D1	D0
Flat	L	X	L	L	L	L	L	L
1 dB Boost	L	H	H	L	L	L	L	L
2 dB Boost	L	H	L	H	L	L	L	L
3 dB Boost	L	H	L	L	H	L	L	L
4 dB Boost	L	H	L	L	L	H	L	L
5 dB Boost	L	H	L	L	L	L	H	L
6 dB Boost	L	H	L	H	L	L	H	L
7 dB Boost	L	H	H	L	H	L	H	L
8 dB Boost	L	H	L	H	L	H	H	L
9 dB Boost	L	H	L	L	L	L	L	H
10 dB Boost	L	H	H	L	H	L	L	H
11 dB Boost	L	H	H	L	H	H	L	H
12 dB Boost	L	H	H	L	H	H	H	H
1 dB ~ 12 dB Cut	L	L	Valid Above Input					
	↑ ⑤	↑ ⑥	← Gain Code →					

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved. See the characteristics curves for more exact data.

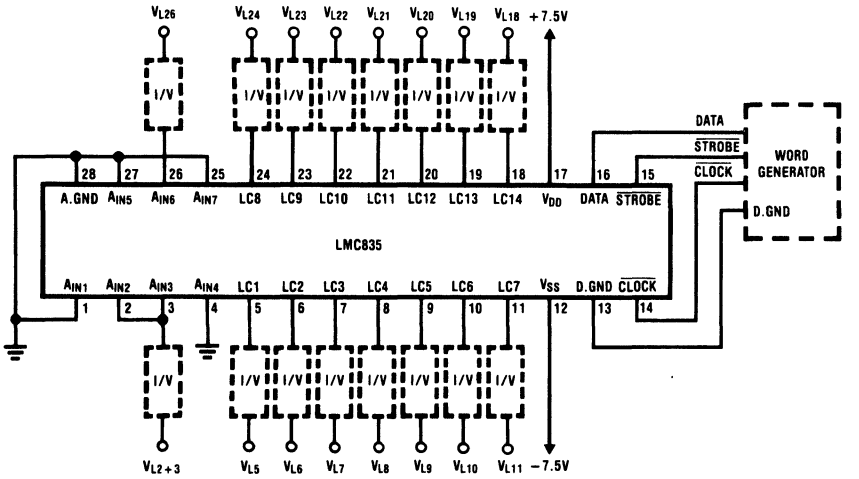
⑤ DATA II
⑥ Boost/Cut

Test Circuits



TL/H/6753–5

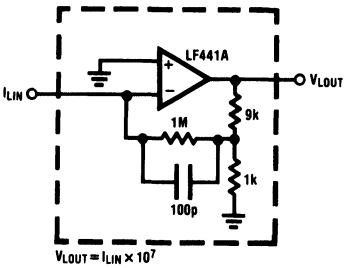
FIGURE 3. Test Circuit for AC Measurement



TL/H/6753–6

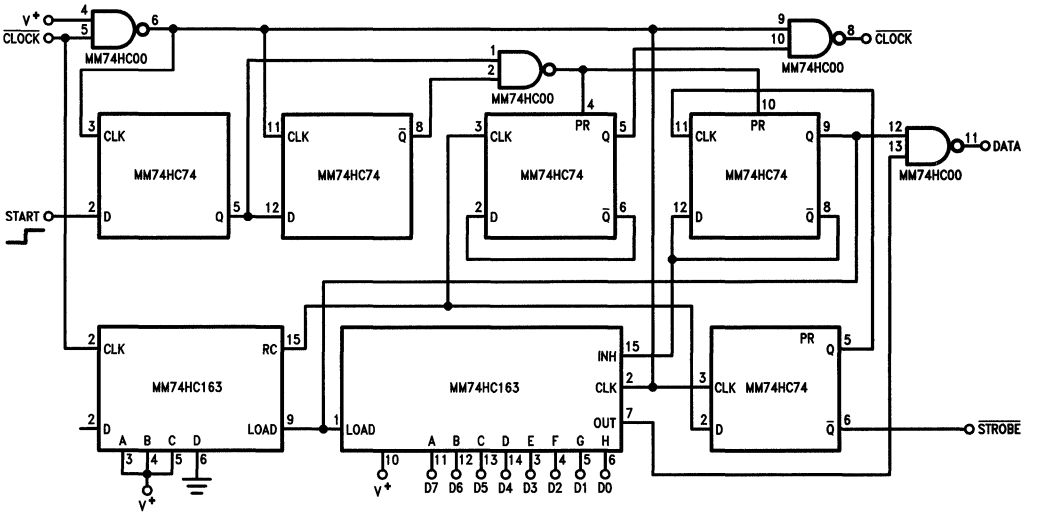
FIGURE 4. Test Circuit for Leakage Current Measurement

Test Circuits (Continued)



TL/H/6753–7

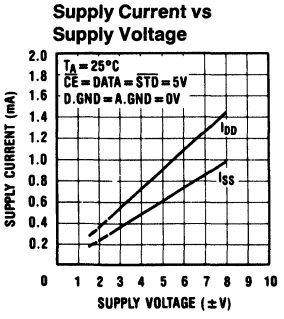
FIGURE 5. I to V Converter

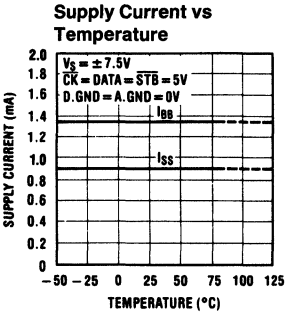


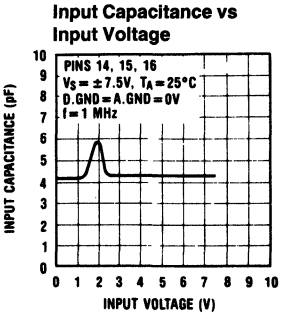
TL/H/6753–8

FIGURE 6. Simple Word Generator

Typical Performance Characteristics



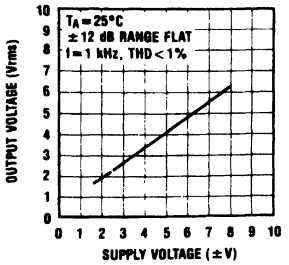




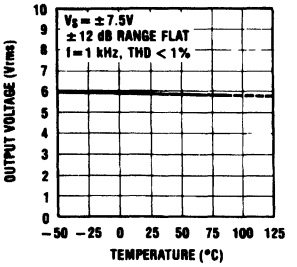
TL/H/6753–9

Typical Performance Characteristics (Continued)

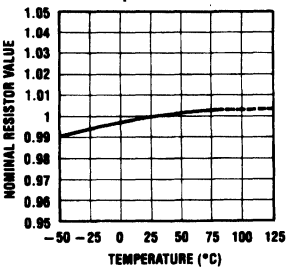
Maximum Output Voltage vs Supply Voltage



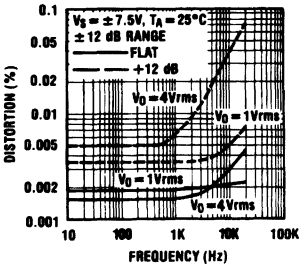
Maximum Output Voltage vs Temperature



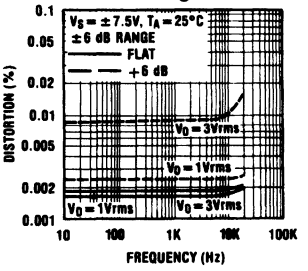
Nominal Resistor vs Temperature



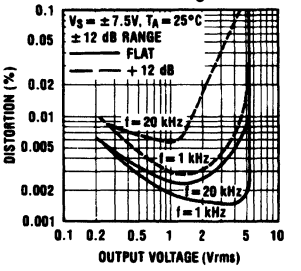
Distortion vs Frequency @ ± 12 dB Range



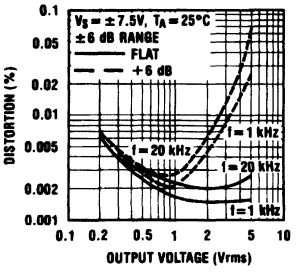
Distortion vs Frequency @ ±6 dB Range



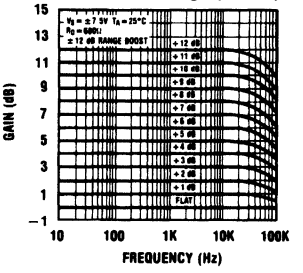
Distortion vs Output Voltage @ ± 12 dB Range



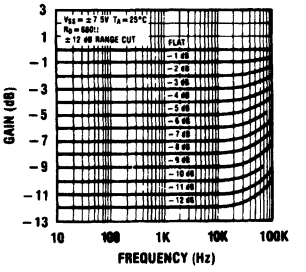
Distortion vs Output Voltage @ ±6 dB Range



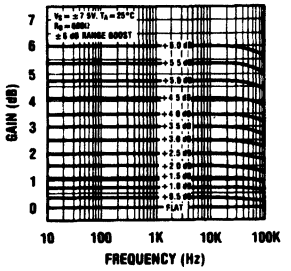
Gain vs Frequency @ ± 12 dB Range (Boost)



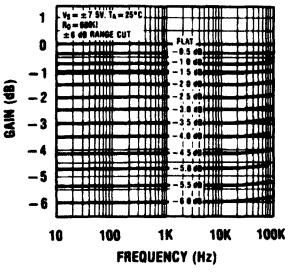
Gain vs Frequency @ ± 12 dB Range (Cut)



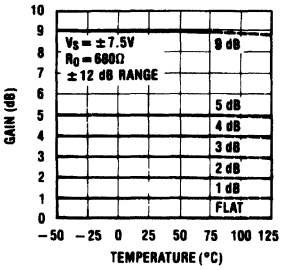
Gain vs Frequency @ ±6 dB Range (Boost)



Gain vs Frequency @ ±6 dB Range (Cut)



Gain vs Temperature



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Typical Applications

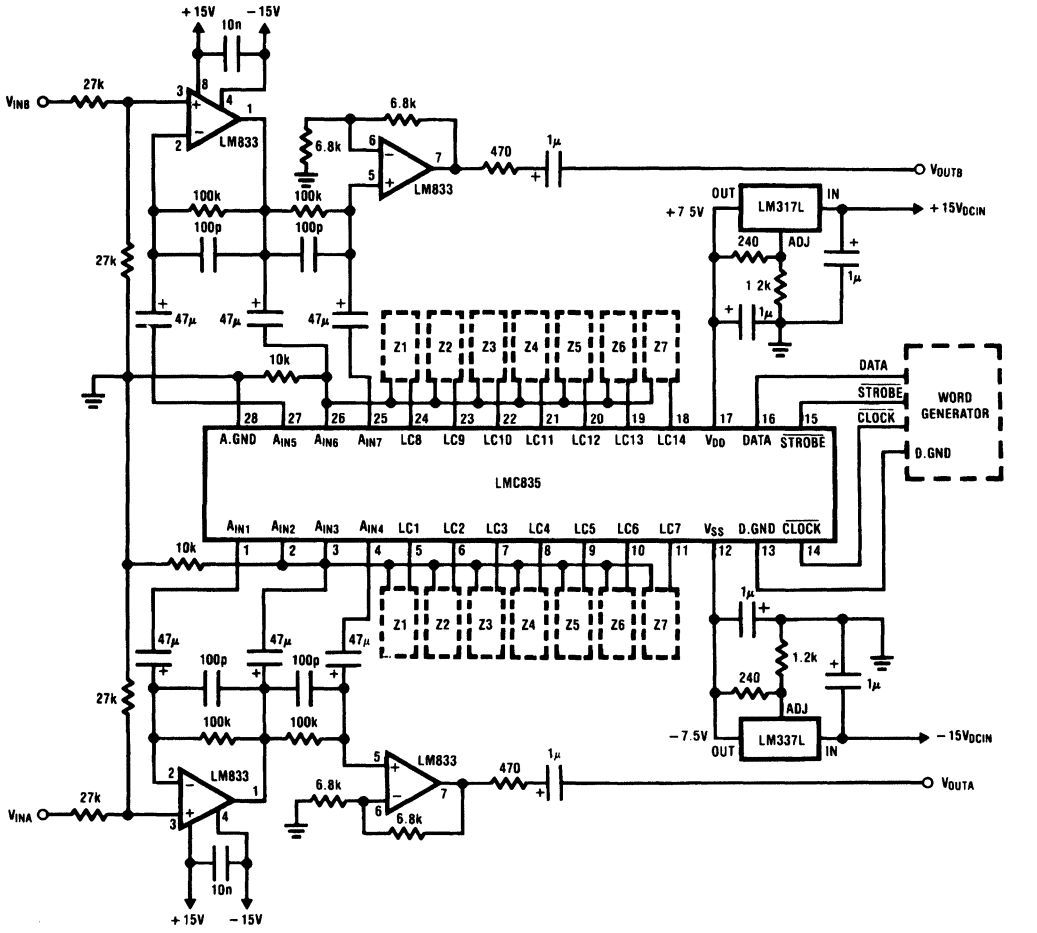

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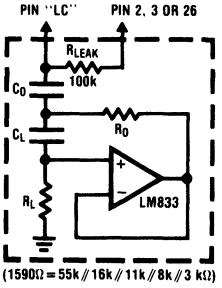
FIGURE 7. Stereo 7-Band Equalizer

TABLE I: Tuned Circuit Elements

$Q_0 = 3.5, Q_{12dB} = 1.05$					
Z1	**f_o (Hz)**	**C_O (F)**	**C_L (F)**	**R_L (Ω)**	**R_O (Ω)**
Z1	63	1µ	0.1µ	100k	680
Z2	160	0.47µ	0.033µ	100k	680
Z3	400	0.15µ	0.015µ	100k	680
Z4	1k	0.068µ	0.0068µ	82k	680
Z5	2.5k	0.022µ	0.0033µ	82k	680
Z6	6.3k	0.01µ	0.0015µ	62k	680
Z7	16k	0.0047µ	680p	47k	680



$$L_O = C_L R_L R_O$$

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

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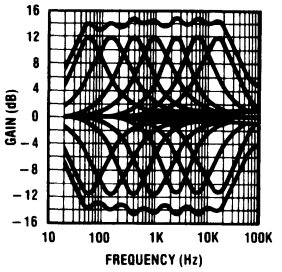
FIGURE 8. Tuned Circuit for Stereo 7-Band Equalizer (*Figure 7*)

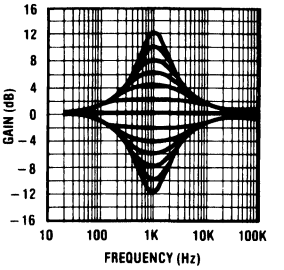
Typical Applications (Continued)

Performance Characteristics (Circuit of *Figure 7*)

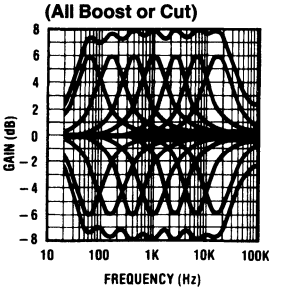
LMC835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)



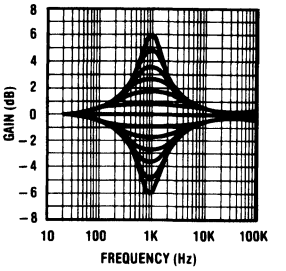
LMC835 Gain vs Frequency @ ± 12 dB Range (1 kHz Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (1 kHz Boost or Cut)



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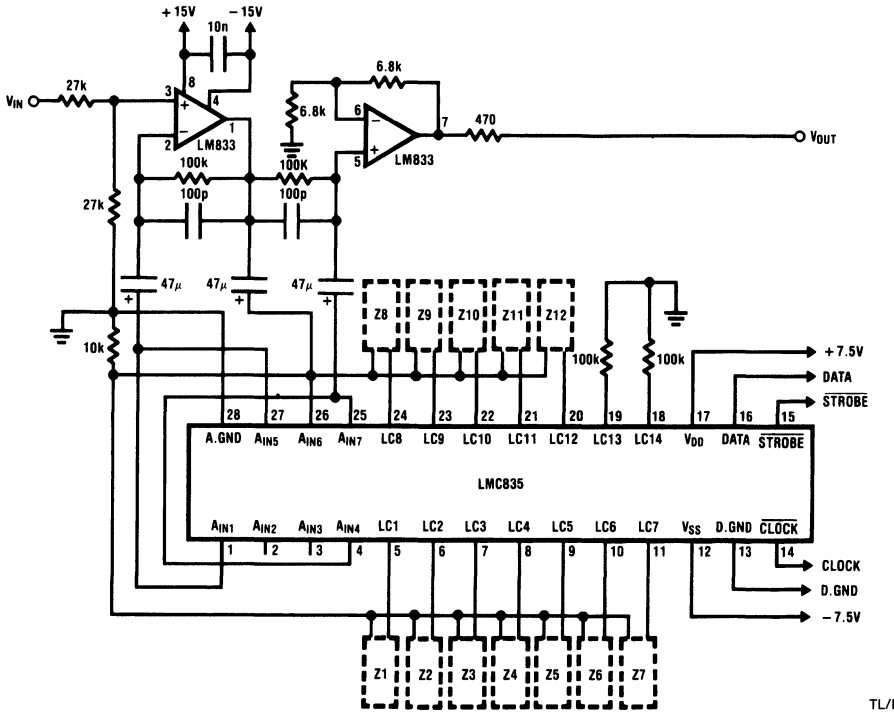

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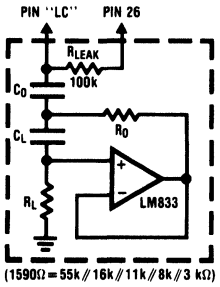
FIGURE 9. 12-Band Equalizer

Typical Applications (Continued)

TABLE II. Tuned Circuit Elements

$Q_0 = 4.7, Q_{12\,dB} = 1.4$					
	f_o (Hz)	C_o (F)	C_L (F)	R_L (Ω)	R_o (Ω)
Z1	16	3.3μ	0.47μ	100k	680
Z2	31.5	15μ	0.22μ	110k	680
Z3	63	1μ	0.1μ	100k	680
Z4	125	0.39μ	0.068μ	91k	680
Z5	250	0.22μ	0.033μ	82k	680
Z6	500	0.1μ	0.015μ	100k	680
Z7	1k	0.047μ	0.01μ	82k	680
Z8	2k	0.022μ	0.0047μ	91k	680
Z9	4k	0.01μ	0.0022μ	110k	680
Z10	8k	0.0068μ	0.001μ	82k	680
Z11	16k	0.0033μ	680p	62k	680
Z12	32k	0.0015μ	470p	68k	510



$$L_O = C_L R_L R_O$$

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

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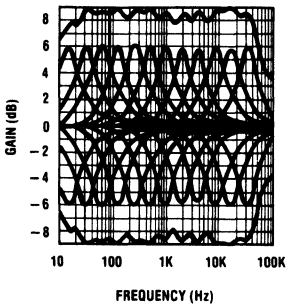
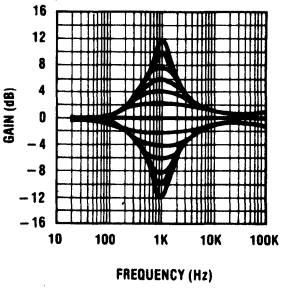
FIGURE 10. Tuned Circuit for 12-Band Equalizer (*Figure 9*)

Performance Characteristics (Circuit of Figure 9)

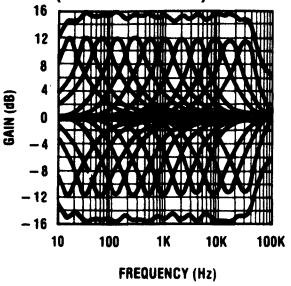
12 Band Equalizer Application
LMC835 Gain vs Frequency
@ ±6 dB Range
(All Boost or Cut)



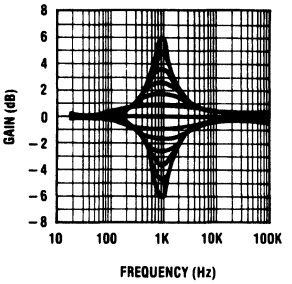
LMC835 12 Band E.Q. Application
Gain vs Frequency
@ ±12 dB Range
(1 kHz Boost or Cut)



12 Band Equalizer Application
LMC835 Gain vs Frequency
@ ± 12 dB Range
(All Boost or Cut)



LMC835 12 Band E.Q. Application
Gain vs Frequency
@ ±6dB Range
(1 kHz Boost or Cut)



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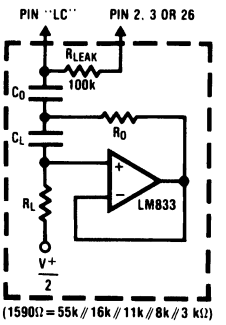
Typical Applications (Continued)



$L_o = C_L, R_L, R_O$

$F_o = \frac{1}{2\pi\sqrt{L_O C_O}}$

$Q_O = \sqrt{C_O R_O^2}$

$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 15°C}$

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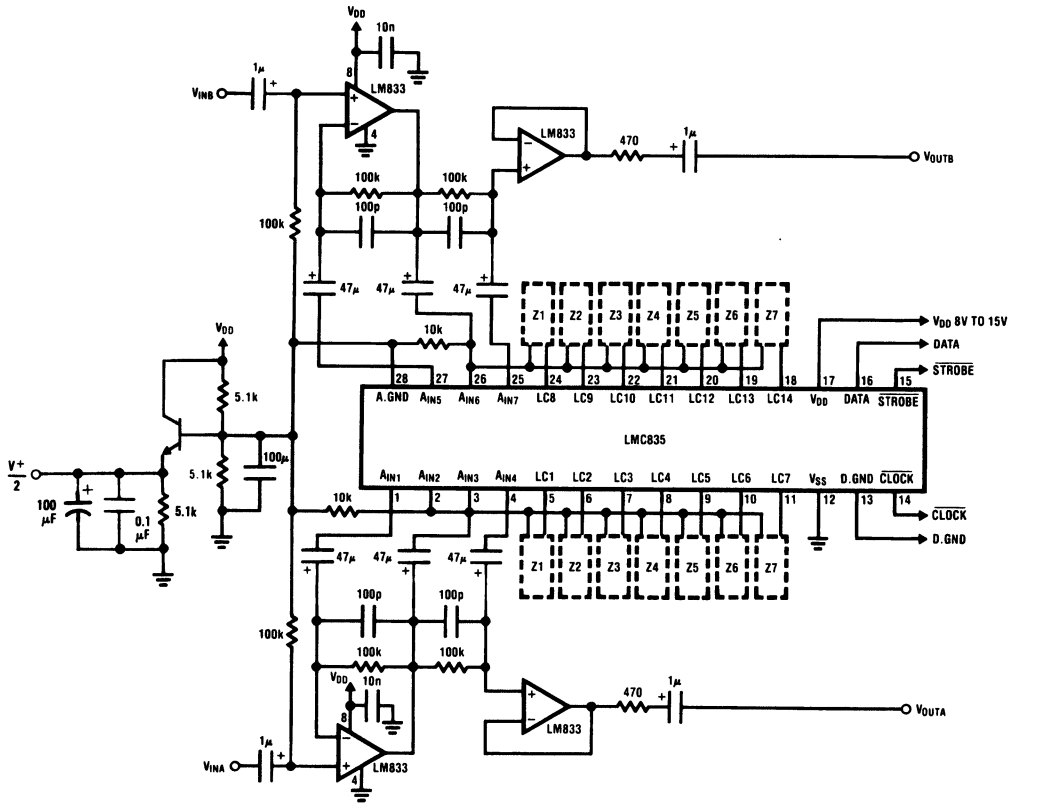

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The $\frac{V^+}{2}$ output is used to bias the gyrators

FIGURE 11. Single Supply Stereo Equalizer

Typical Applications (Continued)

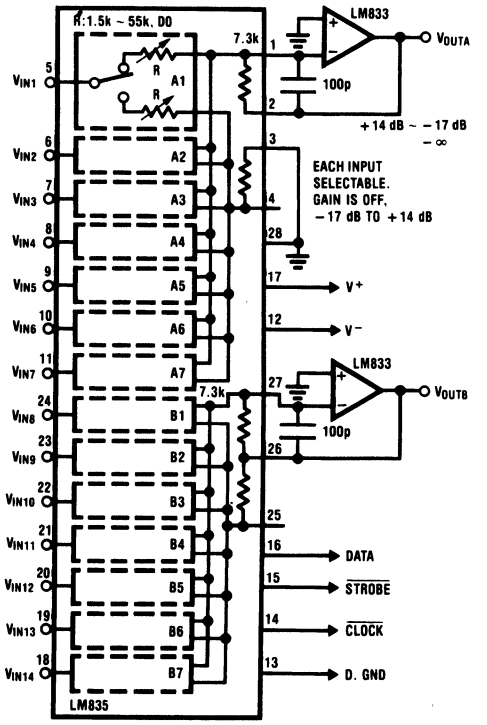

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FIGURE 12. Stereo 7-Input/1-Output Mixers (THD is not as low as equalizer circuit)

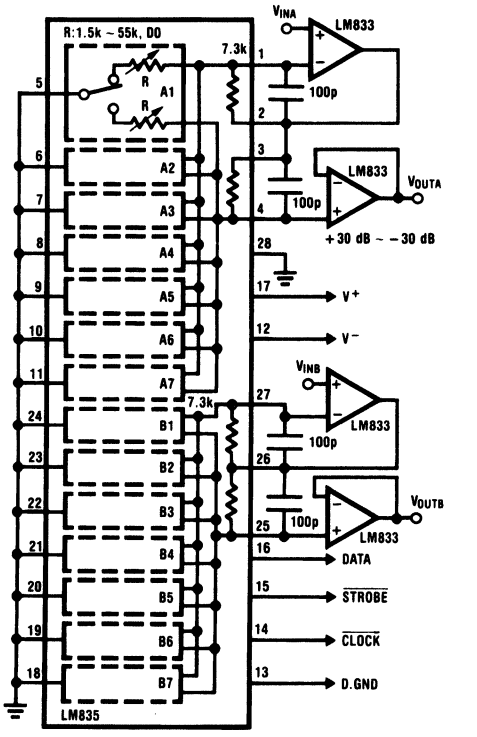

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FIGURE 13. Stereo Volume Control, Very Low THD

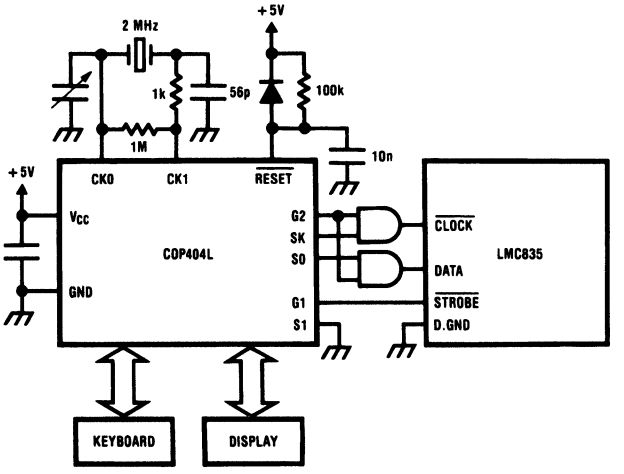

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FIGURE 14. LMC835-COP404L CPU Interface

Typical Applications (Continued)

Sample Subroutine Program for *Figure 14*, LMC835-COP404L CPU Interface

```
HEX
CODE      LABEL       MNEMONICS                          COMMENTS
3F        LMC835:     LBI       3F       ;POINT TO RAMADDRESS 3F
05        SEND        LD                 ;RAMDATA TO A
22                    SC                 ; SET CARRY
335F                  OGI                ;SET PORT G= 1111, OPEN THE AND GATES
4F                    XAS                ;SWAP A AND SIO, CLOCK START
05                    LD                 ;RAMDATA TO A, MAKE SURE A = DATA
07                    XDS                ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
05                    LD                 ;RAMDATA TO A
4F                    XAS                ;SWAP A AND SIO
05                    LD                 ;RAMDATA TO A, MAKE SURE A=NEWDATA
07                    XDS                ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
32                    RC                 ;RESET CARRY
4F                    XAS                ;SWAP A AND SIO, CLOCK STOP
335D                  OGJ       13       ;SET PORT G=1101, MAKE STROBE LOW
335B                  OGI       11       ;SET PORT G=1011, MAKE STROBE HIGH, CLOSE THE
                                                                          GATES
4E                    CBA                ;BD TO A
43                    AISC      3        ;RAMADDRESS<3C THEN RETURN
48                    RET
80                    JP        SEND
```

```
      RAM
   ADDRESS          COMMENTS
3C        DATA   ;GAIN DATA D4-D7
3D        DATA   ;GAIN DATA D0-D3
3E        DATA   ;BAND DATA D4-D7
3F        DATA   ;BAND DATA D0-D3
```

Application Hints

SWITCHING NOISE

The LMC835 uses CMOS analog switches that have small leakages (less than 50 nA). When a band is selected for flat gain, all the switches in that band are open and the resonator circuit is not connected to the LMC835 resistor network. It is only in the flat mode that the small leakage currents can cause problems. The input to the resonator circuit is usually a capacitor and the leakage currents will slowly charge up this capacitor to a large voltage if there is no resistive path to limit it. When the band is set to any value other than flat, the charge on the capacitor will be discharged by the resistor network and there will be a transient at the output. To limit the size of this transient, R_{LEAK} is necessary.

HOW TO AVOID SWITCHING NOISE DUE TO LEAKAGE CURRENT (Refer to *Figures 7* and *8*)

To avoid switching noise due to leakage currents when changing the gain, it is recommended to put R_{LEAK} = 100 kΩ between Pin 3 and Pin 5—11 each, Pin 26 and Pin 12—24 each. The resistor limits the voltage that the capacitor can charge to, with minimal effects on the equalization. The frequency response change due to R_{LEAK} are shown in *Figure 15*. The gain error is only 0.2 dB and Q error is only 5% at 12 dB boost or cut.

SIMPLE WORD GENERATOR *(Figure 6)*

Circuit operation revolves around an MM74HC165 parallel-in/serial-out shift register. Data bits D0 through D7 are applied to the parallel of the MM74HC165 from 8 toggle switches. The bits are shifted out to the DATA input of the LMC835 in sync with the clock. When all data bits have been loaded, CLOCK is inhibited and a STROBE pulse is generated: this sequence is initiated by a START pulse.

LMC835-COP404L CPU INTERFACE (Refer to *Figure 14*)

The diagram shows AND gates between the COP and the LMC835. These permit G2 to inhibit the CLOCK and DATA lines (SK and SO) during a STROBE (G1) pulse. This function may also be implemented in software. As shown in *Figure 2*, the data groups are shifted in D0 first. Data is loaded on positive clock edges.

POWER SUPPLIES

These applications show LM317/337 regulators for the ±7.5V supplies for the LMC835. Since the latter draws only 5 mA max., 1k series dropping resistors from the ±15V op amp supply and a pair of 7.5V zeners and bypass caps will also suffice.

Application Hints (Continued)

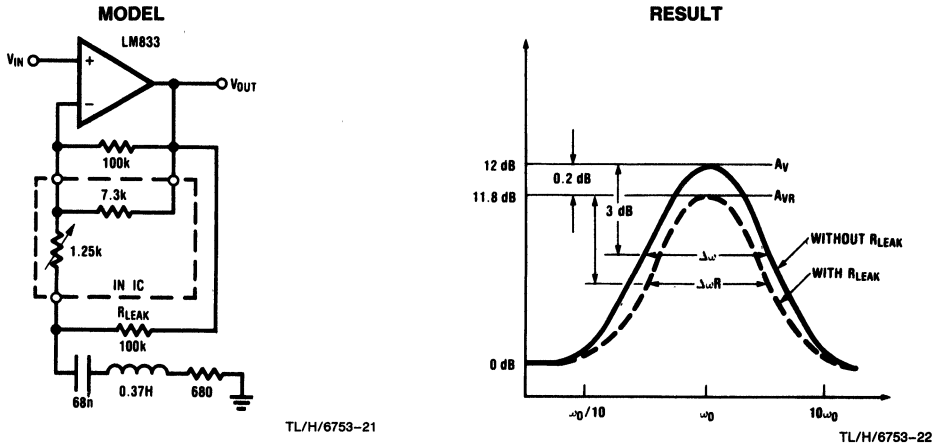


FIGURE 15. Effect of R_{LEAK}

REDUCING EXTERNAL COMPONENTS

The typical application shown in *Figure 7* is switching noise free. The DC-coupled circuit in *Figure 16* is also switching noise free, except at 12 dB/6 dB switch turn ON/OFF. This switching noise is caused by the I_{bias} and V_{offset} of the op amps. Selecting a low I_{bias} and V_{offset} op amp can minimize the switching noise due to the 12 dB/6 dB switch. The DC-coupled application can also eliminate the R_F = 100k resistors with only a 0.5 dB gain error at 12 dB boost or cut.

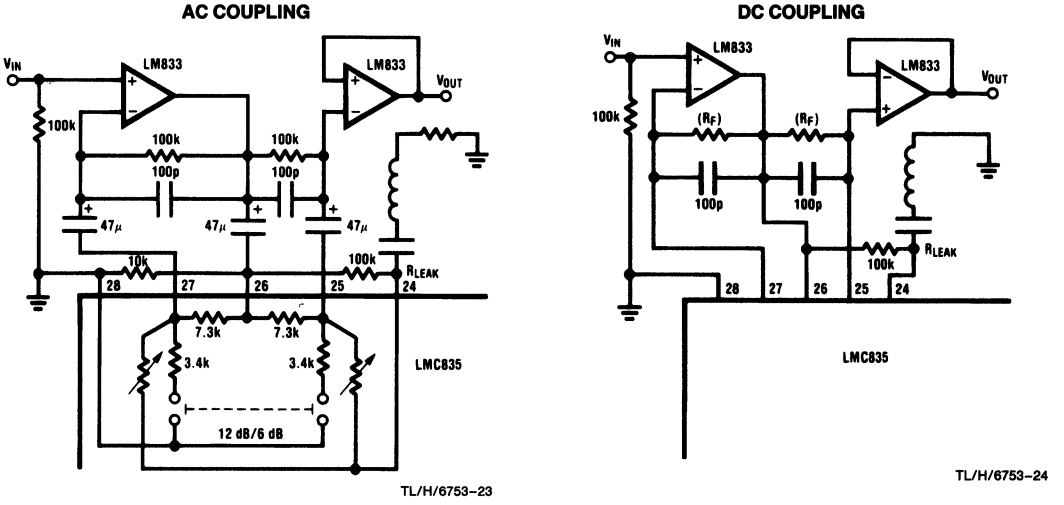


FIGURE 16. Reducing External Components

National Semiconductor

LMC1982
Digitally-Controlled Stereo Tone and Volume Circuit with Two Selectable Stereo Inputs

General Description

The LMC1982 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), enhanced stereo, and loudness controls and selection between two pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1982 is designed for line level input signals (300 mV–2V) and has a maximum gain of −0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1982's SELECT OUT/SELECT IN external processor loop.

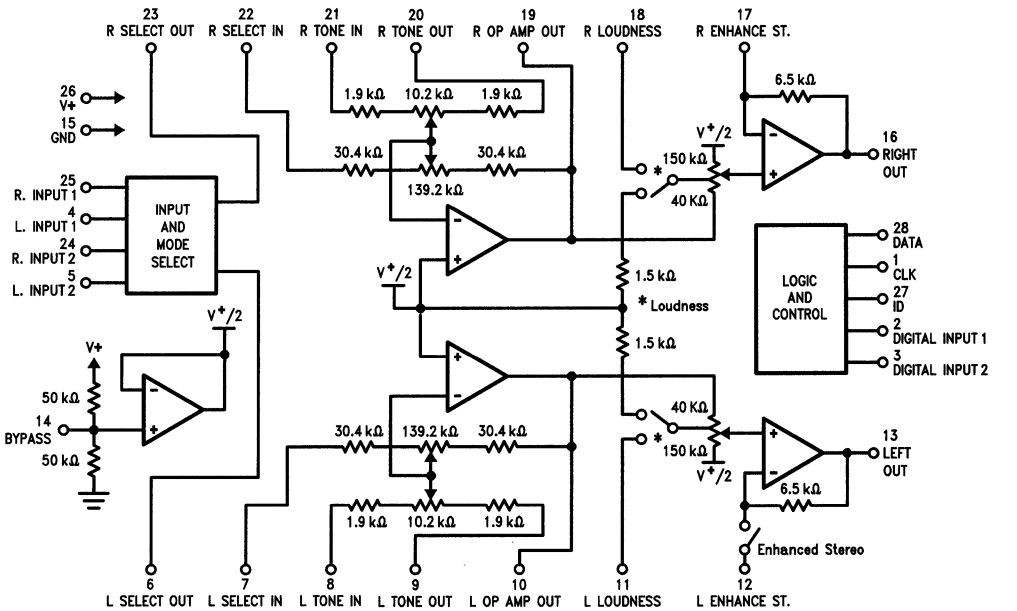
Features

- Low noise and distortion
- Two pairs of stereo inputs
- Enhanced stereo function
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block and Connection Diagrams



TL/H/11028–1

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, (Soldering, 10 Seconds)	+260°C
V Package, (Vapor Phase, 60 Seconds)	215°C
Infrared, (15 Seconds)	220°C
ESD Susceptability (Note 5)	2 kV

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1982CIN, LMC1982CIV	$-40°C \le T_A \le +85°C$
Supply Voltage ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, enhanced stereo is off, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
I_S	Supply Current		15	25	mA (max)
V_{IN}	Input Voltage	Clipping Level (1,.0% THD), Select Out (Pins 6, 23)	2.3	2.0	V_{rms} (min)
THD	Total Harmonic Distortion	Left and Right channels; Output Pins 13, 16			
		V_{IN} = 0.3 V_{rms}; f_{IN} = 100 Hz, 1 kHz, 10 kHz	0.008	0.1	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 100 Hz, 1 kHz	0.4	1.0	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 10 kHz	0.5	1.0	% (max)
		V_{IN} = 0.5 V_{rms}; Bass and Treble Tone Controls Set at Maximum	0.07	0.5	% (max)
		V_{IN} = 0.3 V_{rms}; Volume Attenuator at −20 dB, Bass and Treble Tone Controls Set at Maximum	0.06	0.15	% (max)
	DC Shifts	V_{IN} = 0.3 V_{rms}; Between Any Two Adjacent Control Settings	2.0	4.0	mV (max)
		V_{IN} = 0.3 V_{rms}; All Mode and Input Positions	18	20	mV (max)
R_{OUT}	AC Output Impedance	Pins 6, 23, (470Ω to Ground at Input)	150	200	Ω (max)
		Pins 13, 16	26	40	Ω (max)
R_{IN}	AC Input Impedance	Pins 4, 5, 24, 25	50	72	kΩ (max)
				35	kΩ (min)
	Volume Attenuator Range	Pins 13, 16; Volume Attenuation at 0100010XXX000000 (0 dB)	0.5	1.5	dB (max)
		0100010XXX101XXX (80 dB); (Relative to Attenuation at the 0 dB Setting)	80	78	dB (min)
				82	dB (max)
	Volume Step Size	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB) (Note 9)	2.0	1.5	dB (min)
				2.5	dB (min)
	Channel-to-Channel Volume Tracking Error	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB)	±0.1	±1.5	dB (min)
	Mute Attenuation	V_{IN} = 1.0 V_{rms}	105	86	dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, enhanced stereo is off, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 13, 16	±0.1	±1.5	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 13, 16	±0.1	±1.5	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Enhanced Stereo Cross Coupling	(Note 10)	−4.4	−2.5 −6.9	dB (min) dB (max)
	Frequency Response	V_{IN} Applied to Input 1 and Input 2; f_{IN} = 20 Hz − 20 kHz (Relative to Signal Amplitude at 1 kHz)	±0.1	±1.0	dB (max)
	Loudness	Volume Attenuator = 40 dB, Loudness on (See *Figure 5*) Gain at 100 Hz (Referenced to Gain at 1 kHz) Gain at 10 kHz (Referenced to Gain at 1 kHz)	 11.5 6.5	 13.5 9.5 8.5 4.5	 dB (max) dB (min) dB (max) dB (min)
	Signal-to-Noise Ratio	V_{IN} = 1.0 V_{rms}, A Weighted, Measured at 1 kHz, R_S = 470Ω	95	90	dB (min)
	Channel Balance	All Volume Settings	0.2	1.0	dB (max)
	Channel Separation	Input Pins 4, 25: Output Pins 13, 16; V_{IN} = 1.0 V_{rms} (Note 8)	80	60	dB (min)
	Input-Input Isolation	470Ω to AC Ground on Unused Input	95	60	dB (min)
PSSR	Power Supply Rejection Ratio	V^+ = 9 V_{DC}; 200 mV_{rms}, 100 Hz Sinewave Applied to Pin 26	32	28	dB (min)
f_{CLK}	Clock Frequency		5.0	1.0	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	1.3 2.9	2.0 5.5	V (min) V (min)
$V_{IN(0)}$	Logic "0" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	0.4 1.2	0.8 3.5	V (max) V (max)
$V_{OUT(1)}$	Logic "1" Output Voltage	Pin 28 (IM Bus)		2.0	V (min)
$V_{OUT(0)}$	Logic "0" Output Voltage	Pin 28 (IM Bus)	0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the deivce may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1982CIN, T_{JMAX} = +125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_J = +25°C$ and represent the most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

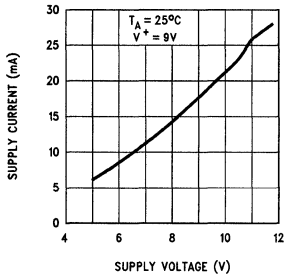
Note 8: The Input-Input Isolation is tested by driving one input and measuring the output when the undriven input are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

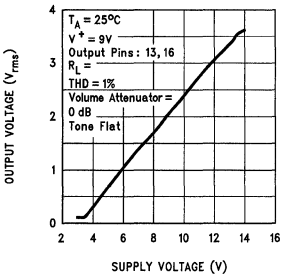
Note 10: Enhanced Stereo Cross Coupling is a measure of the ratio between the undriven right channel output signal and the driven left channel output signal. It is measured by driving the left inputs with a 300 mV_{rms} signal while the right inputs are grounded.

Typical Performance Characteristics

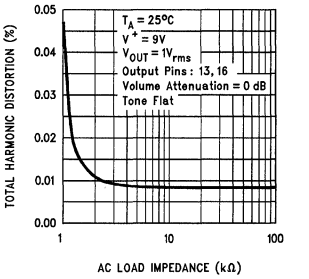
Supply Current vs Supply Voltage



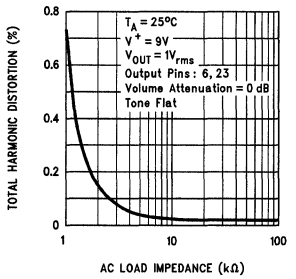
Output Voltage vs Supply Voltage



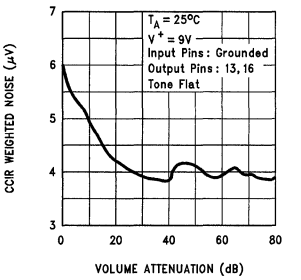
THD vs Load Impedance



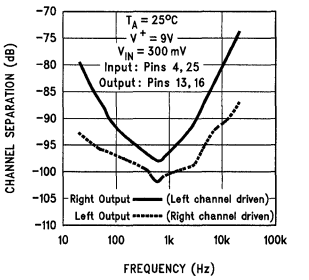
THD vs Load Impedance



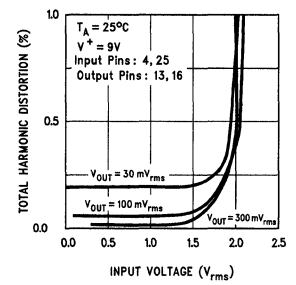
CCIR Output Noise vs Volume Setting



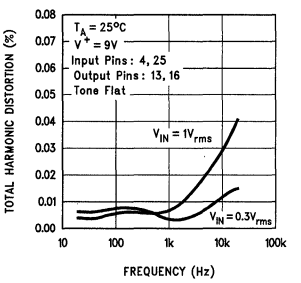
Channel Separation vs Frequency



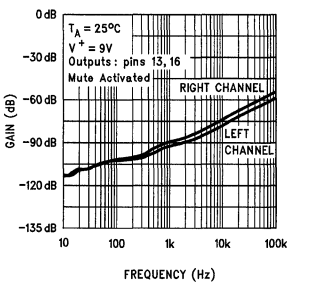
THD vs V_{IN} (V_{OUT} Constant)



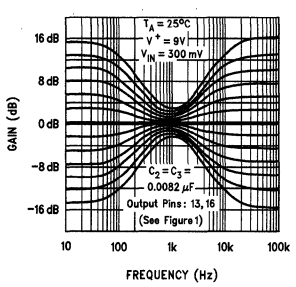
THD vs Frequency



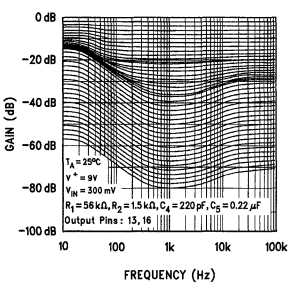
Mute Gain vs Frequency



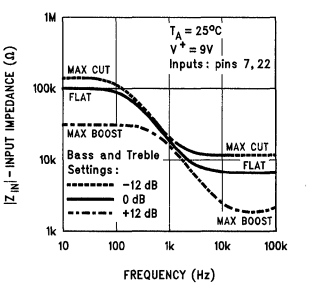
Tone Control Response with Equal Bass and Treble Control Settings



Loudness Response vs Frequency



Select Input Impedance vs Frequency



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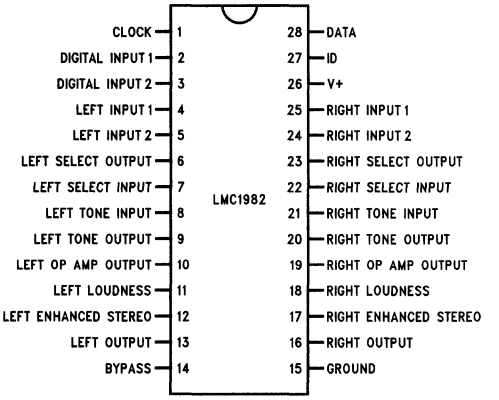
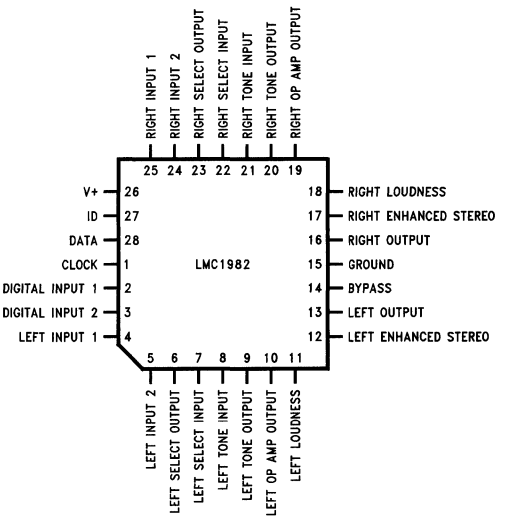
Connection Diagram



TL/H/11028–2

Top View

Order Number LMC1982CIN
See NS Package Number N28B



TL/H/11028–12

Top View

Order Number LMC1982CIV
See NS Package Number V28A

Pin Description

CLK (1) — The INTERMETAL (IM) Bus clock is applied to the CLOCK pin. This input accepts a TTL or CMOS level signal. The input is used to clock the DATA signal. A data bit must be valid on the rising clock edge.

DIGITAL INPUT 1 & 2 (2, 3) — Internally tied high to V^+ through a 30 kΩ pull-up resistor, these inputs allow a peripheral device to place any single-bit, active low digital information onto the IM Bus. It is then sent out to the controlling device through the DATA pin. Examples of such information could include indication of the presence of a Second Audio Program (SAP) or an FM stereo carrier.

INPUTS 1 & 2 (4, 25; 5, 24) — These are the LMC1982's two stereo input pairs.

SELECT OUT (6, 23) — The selected INPUT signal is available at this output. This feature allows external signal processors such as noise reduction or graphic equalizers to be used. This output can typically sink 1 mA. These pins should be capacitively coupled to pins 7 and 22, respectively, if no external processor is used.

SELECT IN (7, 22) — These are the inputs that an external signal processor uses to return a signal to the LMC1982. These pins should be capacitively coupled to pins 6 and 23, respectively, if no external processor is used.

TONE IN (8, 21) — These are the inputs to the tone control amplifier. See the Application Information section titled "Tone Control Response".

TONE OUT (9, 20) — Tone control amplifier output. See the Application Information section titled "Tone Control Response".

OP AMP OUT (10, 19) — These outputs are used with external tone control capacitors. Internally, this output is applied to the volume attenuators.

LOUDNESS (11, 18) — The output signal on these pins is a voltage taken from the volume attenuator's −40 dB tap point. An external R–C network is connected to these pins.

ENHANCED STEREO (12, 17) — An external R–C network is connected across these pins. This provides left-right channel cross-coupling and cancellation to create an enhanced stereo channel separation effect.

MAIN OUTPUT (13, 16) — The output signal from these pins drives a stereo power amplifier. The output can typically sink 1 mA.

BYPASS (14) — A 10 μF capacitor is connected between this pin and ground to provide an AC ground for the internal half-supply voltage reference.

GROUND (15) — This pin is connected to analog ground.

V^+ (26) — This is the power supply connection. The LMC1982 is operational with supply voltages from 6V to 12V. This pin should be bypassed to ground through a 1.0 μF capacitor.

Pin Description (Continued)

ID (27) This is the IDENTITY digital input that, when low, signals the LMC1982 to receive, from a controlling device, a device address (40_H–47_H), present on the DATA line.

DATA (28) This is the serial data input for communications sent by a controller. The controller must have open drain outputs used with external pull-up resistors. The data rate has a maximum frequency of 1 MHz. The LMC1982 requires 16 bits of data to control or change a function: the first 8 bits select the LMC1982 and one of eight functions. The final eight bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

TABLE I. IM Bus Programming Codes for LMC1982

Address (A7–A0)	Function	Data	Function Selected
01000000	Input Select + Mute	XXXXXX00	INPUT1
		XXXXXX01	INPUT2
		XXXXXX10	N/A
		XXXXXX11	MUTE
01000001	Loudness, Enhanced Stereo	XXXXXX00	Loudness OFF Enhanced Stereo OFF
		XXXXXX01	Loudness ON Enhanced Stereo OFF
		XXXXXX10	Loudness OFF Enhanced Stereo ON
		XXXXXX11	Loudness ON Enhanced Stereo ON
01000010	Bass	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000011	Treble	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000100	Left Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000101	Right Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000110	Mode Select	XXXXX100	Left Mono
		XXXXX101	Stereo
		XXXXX11X	Right Mono
01000111	Read Digital Input 1 or Digital Input 2 on IM Bus	XXXXXXD1D0	D0 = Digital Input 1 D1 = Digital Input 2

General Information

The LMC1982 is a CMOS/bipolar building block intended for high fidelity audio signal processing. It is designed for line level inputs signals (300 mV − 2V) and has a maximum gain of −0.5 dB. While the LMC1982 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and poly-silicon resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment. Internal circuits set the volume to minimum, tone controls to flat, the mute to on, and all other functions off when power is first applied. Individual left and right volume controls are software programmed to achieve the stereo balance function. *Figure 1* shows the connection diagram of a typical LMC1982 application.

The LMC1982 has internal decoding logic that allows a microprocessor (μP) or microcontroller (μC) to communicate directly to the audio control circuitry through an INTERMETAL (IM) Bus interface. This three-wire interface consists of a bi-directional DATA line, a Clock (CLK) input line, and an Identity (ID) line. Address and function selection data (8 bits) are serially shifted from the controller to the LMC1982. This is followed by 8 bits of function value data. Data present in the internal shift register is latched and the instruction is executed.

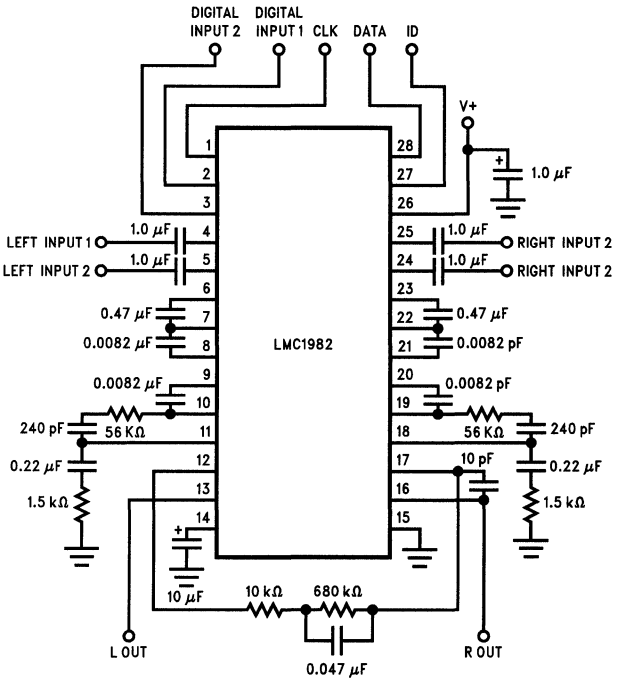


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FIGURE 1. Typical Application

Application Information

INPUT SELECTOR

The LMC1982's input selector and mode control are shown in *Figure 2*. The input selector selects one of two stereo signal sources or a mute function with typical attenuation of 100 dB. The selected signals are then sent to a mode control matrix. As shown in Table I, the matrix provides normal stereo or can direct either channel to both LEFT or RIGHT SELECT OUTPUTs. The third matrix mode is normal stereo. The control matrix output is buffered and appears on each channel's respective SELECT OUT pin (6, 23). Switching noise is kept to a minimum when mute is selected by using a 50 kΩ bias resistor.

Noise performance is optimized through the use of emitter followers in the mode control matrix's output. Internal 50 kΩ resistors are connected to each input selector pin to provide the proper bias point for the emitter follower buffers. Each internal 50 kΩ bias resistor is connected to a common half-supply ($V^+/2$) source. This produces a voltage at pins 6 and 23 (SELECT OUT) that is 1.4V below $V^+/2$ (typically 3.1V with $V^+ = 9V$). Since a DC voltage is present at the input pins (4, 5, 24, and 25), input signal should be AC coupled through a 1 μF capacitor.

The output signal at pins 6 and 23 can be used to drive exteral audio processing circuits such as noise reduction (LM1894–DNR or Dolby) or graphic equalizers (LMC835). It is important that if any noise reduction is used it be placed ahead of any tone controls or equalizers in the external circuit path to preserve the frequency spectrum of the selected input signal. Otherwise, any frequency equalization could prevent the proper operation of the noise reduction circuit. If no external processor is used, a capacitor should be used to couple the SELECT OUT signals directly to pins 7 and 22, respetively.

MINIMUM LOAD IMPEDANCE

The LMC1982 employs emitter-followers to buffer the selected stereo channels. The buffered signals are available at pins 6 and 23 (SELECT OUT). The SELECT OUT buffers operate with a typical bias current 1 mA.

The Electrical Specifications table lists a maximum input signal of 2.0 V_{rms} (2.5 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum AC load impedance seen by the SELECT OUT pins is 2.5 kΩ (2.5V/1 mA). Using lower load impedances results in clipping at lower output levels. If the load impedance is DC-coupled, an increased quiescent current can flow. Latch-up may occur if the total emitter current exceeds 5 mA. Thus, maximum output voltage can be increased and much lower distortion levels can be achieved using load impedances of at least 25 kΩ.

INPUT IMPEDANCE

The input impedance of pins 4, 5, 24 and 25 is defined by internal bias resistors and is typically 50 kΩ.

The SELECT IN pins have an input impedance that varies with the BASE and TREBLE control settings. The input impedance is 100 kΩ at DC and 19 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 30.4 kΩ at DC and 16 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 6.8 kΩ and, with the tone controls at maximum boost, is 2.5 kΩ.

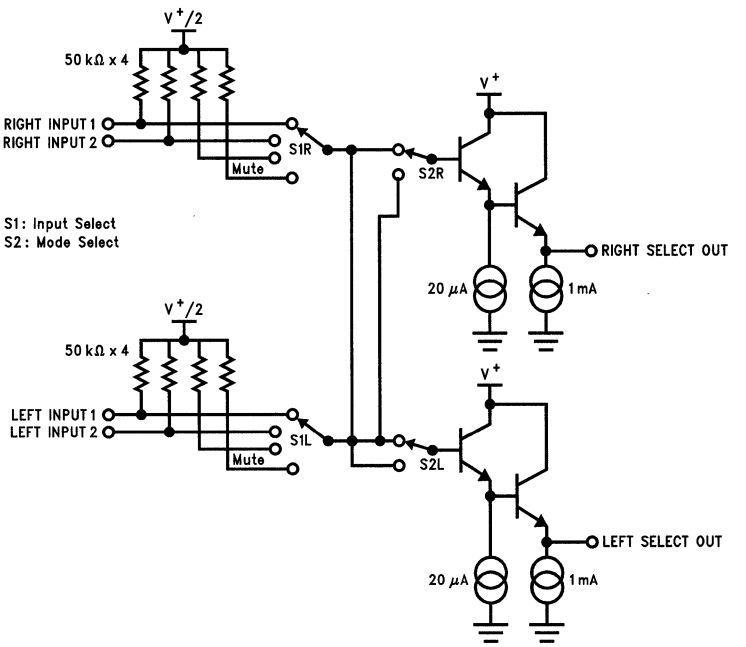

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FIGURE 2. Input and Mode Select Circuitry

Application Information (Continued)

EXTERNAL SIGNAL PROCESSING

The SELECT OUT pins (6 and 23) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or multi-band graphic equalizers (LMC835). If both are used, it is important to ensure that the noise reduction circuitry precede the equalization circuits. Failure to do so results in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the LMC1982. The tone controls used just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see *Figure 4*) and internal resistors in the feedback loop of the internal tone amplifier. The maximum-boost or cut is determined by the data sent to the LMC1982 (see Table I).

The typical tone control response shown in Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response is referred to as the turn-over frequency. With C = C2 = C3, the LMC1982's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14\ k\Omega)}$$

The bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(30.4\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(1.9\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(169.6\ k\Omega)}$$

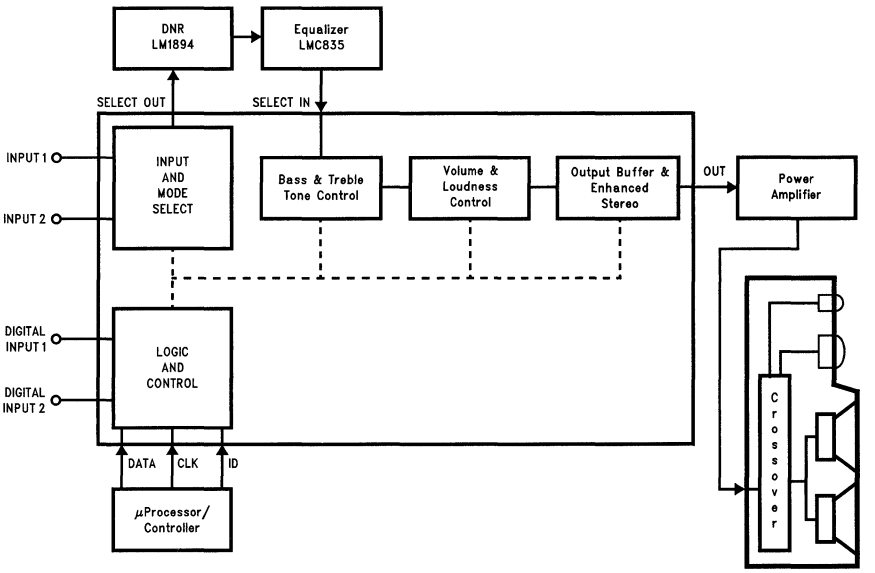

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FIGURE 3. System Block Diagram Utilizing the External Processing Loop (One Channel Shown)

Application Information (Continued)

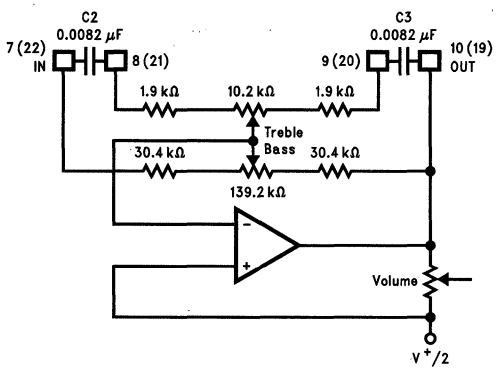

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FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082 μF, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 μF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors size is decreased these frequencies will increase. With C2 = C3 = 0.0068 μF the 2 dB steps take place at 130 Hz and 11.2 kHz.

LOUDNESS

The human ear has less sensitivity to high and low frequencies relative to its sensitivity to mid-range frequencies between 2 kHz and 6 kHz for any given acoustic level. The low and high frequency sensitivity decreases faster than the sensitivity to the mid-range frequencies as the acoustic level drops. The LMC1982's loudness function can be used to help compensate for the decreased sensitivity by boosting the gain at low and high frequencies as the volume control attenuation increases (see the curve labeled "Gain vs Frequency with Loudness Active").

The LMC1982's loudness function uses external components R1, R2, C4 and C5, as shown in *Figure 5*, to select the frequencies where bass and treble boost begin. The amount of boost is dependent on the volume attenuator's setting. The loudness characteristic, with the volume attenuator set at 40 dB, has a transfer function of

$$\frac{V_O}{V_I} = \frac{(sC5R2 + 1)[sC4(R1 + 156k) + 1]}{(s^2)C4C5R2(163k) + s[C4(156k) + C5(4.9R2 + 156k)] + 1}$$

The external components R1 and C4 can be eliminated and pin 10(19) left open if bass boost is the only desired loudness characteristic.

As shown in Table I, loudness and enhanced stereo are controlled through the same address. It is important to remember to set both functions to the correct value any time either of these functions is updated.

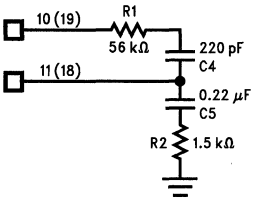

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FIGURE 5. Loudness Control Circuit

ENHANCED STEREO

The LMC1982 has an enhanced stereo effect that can be achieved by cross-coupling reverse phase information between the left and right stereo channels. This feature can help improve the apparent stereo channel separation when, because of cabinet or equipment limitations, the left and right speakers are closer to each other than optimum.

Enhanced stereo is created by connecting an external frequency shaping RC network between the OUTPUT operational amplifiers' inverting inputs through an internal CMOS switch (see *Figure 6*). The external network couples 60% of each channel's output to the opposite channel's inverting input. This cancels a portion of the signal common to both channels.

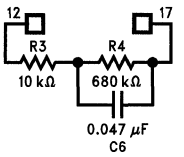

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FIGURE 6. Enhanced Stereo Circuit

The desired 60% cross-coupling is accomplished through the internal 6.5 kΩ feedback resistor and an external 10 kΩ resistor. Bass frequency cancellation is prevented by using a 0.047 μF coupling capacitor to couple only frequencies above 330 Hz. Switching noise is eliminated by using a 680 kΩ resistor across the 0.047 μF. R3, R4 and C6 can be eliminated if enhanced stereo is not desired.

As shown in Table I, enhanced stereo and loudness are controlled through the same address. It is important to remember to set both functions to the correct value any time either of these functions is updated.

Application Information (Continued)

SERIAL DATA COMMUNICATION

The LMC1982 uses the INTERMETAL serial bus (IM Bus) standard. Serial data information is sent to the LMC1982 over a three wire IM Bus consisting of Clock (CLK), Data (DATA), and Identity (ID). The DATA line is bidirectional and the CLK and ID lines are unidirectional from the microprocessor or micontroller to the LMC1982. The LMC1982's bidirectional capability is accomplished by using an open drain output on the DATA line and an external 1 kΩ pull-up resistor.

The LMC1982 responds to address values from 01000000 (40_H) through 01000111 (47_H). The addresses select one of the eight available functions (see Table I). The IM Bus' lines have a logic high standby state when using TTL logic levels. As shown in *Figure 7*, data transmission is initiated by low levels on CLK and ID. Next, eight address bits are sent. This address information includes the code to select one of the LMC1982's desired functions. Each address bit is clocked in on the rising edge of CLK. The ID line is taken high after the eight bits of address data are received by the LMC1982. The controlling system continues toggling the CLK line eight more times. Data that determines the selected function's operating point is written into, or single bit information on DIGITAL INPUT 1 or DIGITAL INPUT 2 is read from, the LMC1982. Finally, the end of transmission is signalled by pulsing the ID line low for a minimum of 1 μs. The transmitted function data is latched and the function changes to its new setting.

Table I also details the serial data structure, range, and bit assignments that sets each function's operating point. The volume and tone controls' function control data binarily increments from zero to maximum as the function's operating point changes from 80 dB attenuation to 0 dB attenuation (volume) or −12 dB to +12 dB (tone controls). Note that not all data bits are needed by each function. The extra bits shown as "X"s ("don't cares") are position holders and have no affect on a respective function. They are necessary to properly position the data in the LMC1982's internal data shift register. Unexpected results may take place if these bits are not sent.

The LMC1982's internal data shift register can handle either a 16-bit word or two 8-bit serial data transmissions. It is the final 8 bits of data received before the ID line goes high that are used as the LMC1982 selection and function addresses. The final eight bits after the ID line returns high are used to change a function's operating point. CLK must be stopped when the final 8 data bits are received. The data stored in the internal data latch remains unchanged until the ID is pulsed, signifying the end of data transmission. When ID is pulsed, the new data in the data shift register is latched into the data latch and the selected function takes on a new operating point.

A complete description and more information concerning the IM Bus is given in the appendix of ITT's CCU2000 datasheet.

DIGITAL I/O

The LMC1982's two Digital Input pins, 2 and 3, provide single-bit communication between a peripheral device and the controller over the IM Bus. Each pin has an internal 30 kΩ pull-up resistor. Therefore, these pins should be connected to open collector/drain outputs. The type of information that could be received on these lines and retrieved by a controller include FM stereo pilot indication, power on/off, Secondary Audio Program (SAP), etc.

According to Table I, the logic state of DIGITAL INPUT 1 and DIGITAL INPUT 2 is latched and can be retrieved over the IM Bus using the read command (47_H). The single-bit information sent on the IM Bus is active low since these lines are internally pulled high.

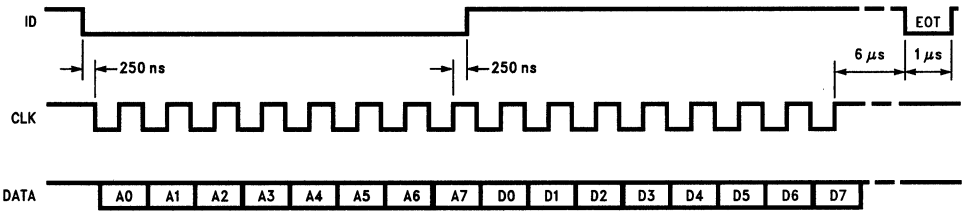

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FIGURE 7. LMC1982's INTERMETAL Serial Bus Timing

National Semiconductor

LMC1983
Digitally-Controlled Stereo Tone and Volume Circuit with Three Selectable Stereo Inputs

General Description

The LMC1983 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), loudness controls and selection between three pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1983 is designed for line level input signals (300 mV–2V) and has a maximum gain of −0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1983's SELECT OUT/SELECT IN external processor loop.

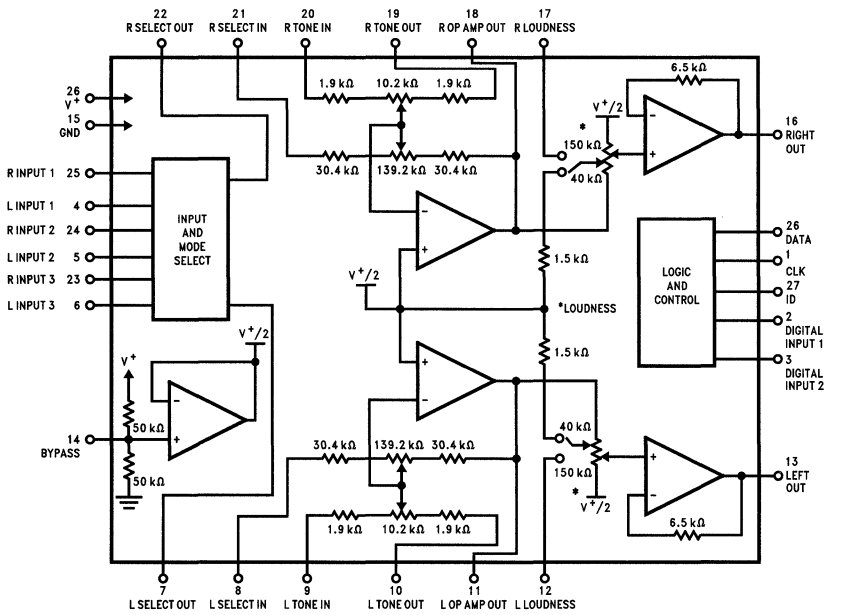
Features

- Low noise and distortion
- Three pairs of stereo inputs
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC Package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block Diagram



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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, (Soldering, 10 Seconds)	+260°C
V Package, (Vapor Phase, 60 Seconds)	215°C
Infrared, (15 Seconds)	220°C
ESD Susceptability (Note 5)	2 kV

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1983CIN, LMC1983CIV	$-40°C \le T_A \le +85°C$
Supply Voltage ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
I_S	Supply Current		15	25	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 7, 22)	2.3	2.0	V_{rms} (min)
THD	Total Harmonic Distortion	Left and Right channels; Output Pins 13, 16			
		V_{IN} = 0.3 V_{rms}; f_{IN} = 100 Hz, 1 kHz, 10 kHz	0.008	0.1	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 100 Hz, 1 kHz	0.4	1.0	% (max)
		V_{IN} = 2.0 V_{rms}; f_{IN} = 10 kHz	0.5	1.0	% (max)
		V_{IN} = 0.5 V_{rms}; Bass and Treble Tone Controls Set at Maximum	0.07	0.5	% (max)
		V_{IN} = 0.3 V_{rms}; Volume Attenuator at −20 dB, Bass and Treble Tone Controls Set at Maximum	0.06	0.15	% (max)
	DC Shifts	V_{IN} = 0.3 V_{rms}; between Any Two Adjacent Control Settings	2.0	4.0	mV (max)
		V_{IN} = 0.3 V_{rms}; All Mode and Input Positions	18	20	mV (max)
R_{OUT}	AC Output Impedance	Pins 7, 22, (470Ω to Ground at Input)	150	200	Ω (max)
		Pins 13, 16	26	40	Ω (max)
R_{IN}	AC Input Impedance	Pins 4, 5, 23, 24, 25	50	72 35	kΩ (max) kΩ (min)
	Volume Attenuator Range	Pins 13, 16; Volume Attenuation at 0100010XXX000000 (0 dB)	0.5	1.5	dB (max)
		0100010XXX101XXX (80 dB); (Relative to Attenuation at the 0 dB Setting)	80	78 82	dB (min) dB (max)
	Volume Step Size	All Volume Attenuation Settings from 0100010XXX101XXX (80 dB) to 0100010XXX000000 (0 dB) (Note 9)	2.0	1.5 2.5	dB (min) dB (min)
	Channel-to-Channel Tracking Error	All Volume Attenuation Settings from 0100010XXX100110 (76 dB) to 0100010XXX000000 (0 dB)	±0.1	±1.5	dB (min)
		from 0100010XXX101XXX (80 dB) to 0100010XXX100111 (78 dB)		±2.0	dB (min)
	Mute Attenuation	V_{IN} = 1.0 V_{rms}	105	86	dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 9V$, $f_{IN} = 1$ kHz, input signal (300 mV) applied to INPUT 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and loudness is off unless otherwise specified. All limits apply for $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Unit (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 13, 16	±0.1	±1.5	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 13, 16	±12	±10.0 ±14.0	dB (min) dB (max)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 13, 16	±0.1	±1.5	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 13, 16 (Relative to Previous Level)	2.0	1.5 2.5	dB (min) dB (max)
	Frequency Response	V_{IN} Applied to Input 1 and Input 2; f_{IN} = 20 Hz − 20 kHz (Relative to Signal Amplitude at 1 kHz)	±0.1	±1.0	dB (max)
	Loudness	Volume Attenuator = 40 dB, Loudness on (See *Figure 5*) Gain at 100 Hz (Referenced to Gain at 1 kHz) Gain at 10 kHz (Referenced to Gain at 1 kHz)	 11.5 6.5	 13.5 9.5 8.5 4.5	 dB (max) dB (min) dB (max) dB (min)
	Signal-to-Noise Ratio	V_{IN} = 1.0 V_{rms}, A Weighted, Measured at 1 kHz, R_S = 470Ω	95	90	dB (min)
	Channel Balance	All Volume Settings	0.2	1.0	dB (max)
	Channel Separation	Input Pins 4, 25: Output Pins 13, 16; V_{IN} = 1.0 V_{rms} (Note 8)	80	60	dB (min)
	Input-Input Isolation	470Ω to AC Ground on Unused Input	95	60	dB (min)
PSSR	Power Supply Rejection Ratio	V^+ = 9 V_{DC}; 200 mV_{rms}, 100 Hz Sinewave Applied to Pin 26	32	28	dB (min)
f_{CLK}	Clock Frequency		5.0	1.0	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	1.3 2.9	2.0 5.5	V (min) V (min)
$V_{IN(0)}$	Logic "0" Input Voltage	Pins 1, 27, 28 (IM Bus) Pins 2, 3	0.4 1.2	0.8 3.5	V (max) V (max)
$V_{OUT(1)}$	Logic "1" Output Voltage	Pin 28 (IM Bus)		2.0	V (min)
$V_{OUT(0)}$	Logic "0" Output Voltage	Pin 28 (IM Bus)	0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the deivce may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1983CIN, T_{JMAX} = +125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at $T_J = +25°C$ and represent the most likely parametric norm.

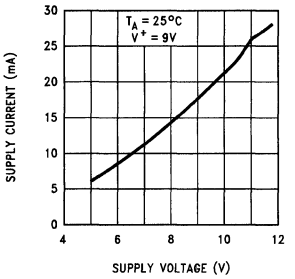
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The Input-Input Isolation is tested by driving one input and measuring the output when the undriven input are selected.

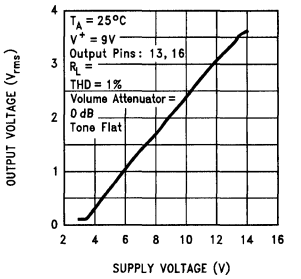
Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

Typical Performance Characteristics

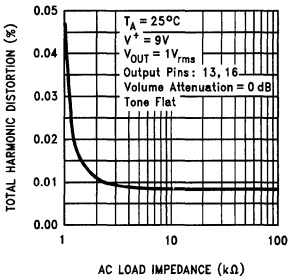
Supply Current vs Supply Voltage



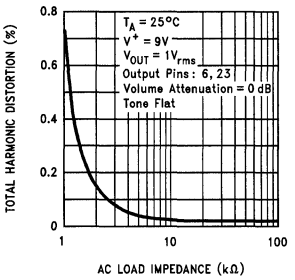
Output Voltage vs Supply Voltage



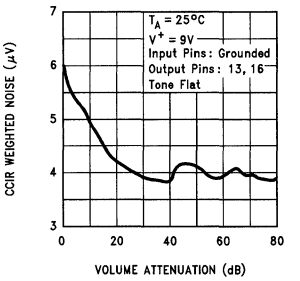
THD vs Load Impedance



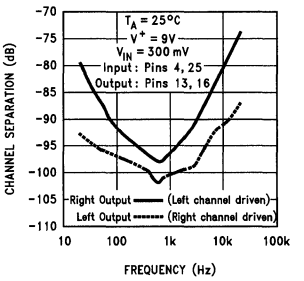
THD vs Load Impedance



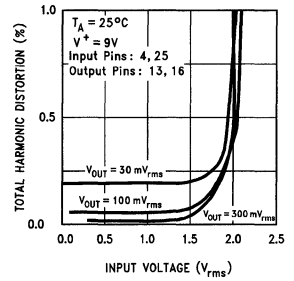
CCIR Output Noise vs Volume Setting



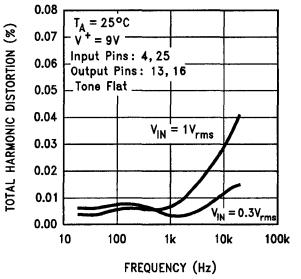
Channel Separation vs Frequency



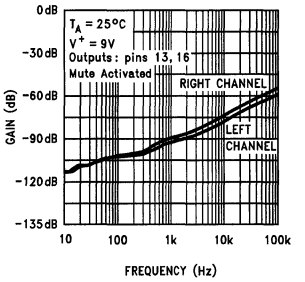
THD vs V_{IN} (V_{OUT} Constant)



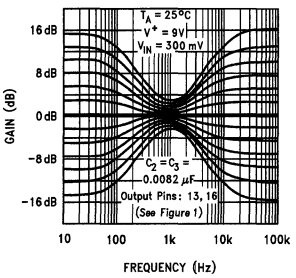
THD vs Frequency



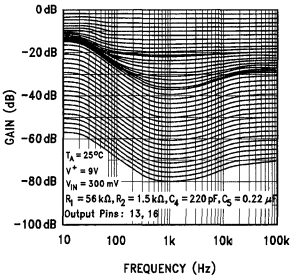
Mute Gain vs Frequency



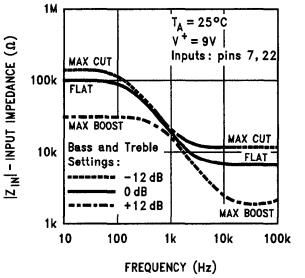
Tone Control Response with Equal Bass and Treble Control Settings



Loudness Response vs Frequency

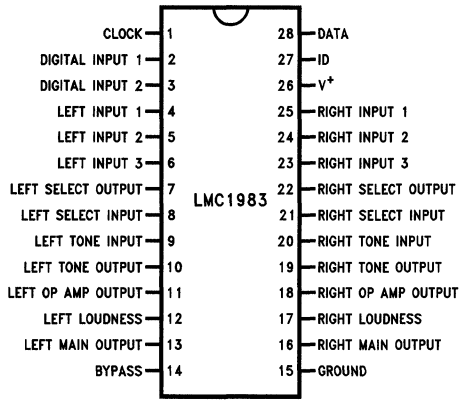


Select Input Impedance vs Frequency



TL/H/11279–9

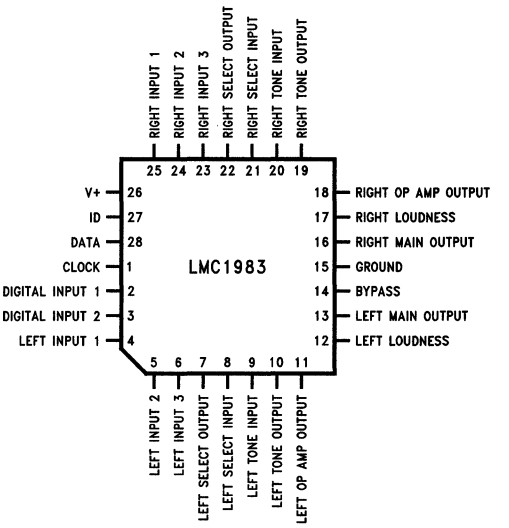
Connection Diagram



TL/H/11279–2

Top View

Order Number LMC1983CIN
See NS Package Number N28B



TL/H/11279–10

Top View

Order Number LMC1983CIV
See NS Package Number V28A

Pin Description

CLK (1)	The INTERMETAL (IM) Bus clock is applied to the CLOCK pin. This input accepts a TTL or CMOS level signal. The input is used to clock the DATA signal. A data bit must be valid on the rising clock edge.
DIGITAL INPUT 1 & 2 (2, 3)	Internally tied high to V^+ through a 30 kΩ pull-up resistor, these inputs allow a peripheral device to place any single-bit, active low digital information onto the IM Bus. It is then sent out to the controlling device through the DATA pin. Examples of such information could include indication of the presence of a Second Audio Program (SAP) or an FM stereo carrier.
INPUTS 1, 2 & 3 (4, 25; 5, 24; 6, 23)	These are the LMC1983's three stereo input pairs.
SELECT OUT (7, 22)	The selected INPUT signal is available at this output. This feature allows external signal processors such as noise reduction or graphic equalizers to be used. This output can typically sink 1 mA. These pins should be capacitively coupled to pins 8 and 21, respectively, if no external processor is used.
SELECT IN (8, 21)	These are the inputs that an external signal processor uses to return a signal to the LMC1983. These pins should be capacitively coupled to pins 7 and 22, respectively, if no external processor is used.
TONE IN (9, 20)	These are the inputs to the tone control amplifier. See the Application Information section titled "Tone Control Response".
TONE OUT (10, 19)	Tone control amplifier output. See the Application Information section titled "Tone Control Response".
OP AMP OUT (11, 18)	These outputs are used with external tone control capacitors. Internally, this output is applied to the volume attenuators.
LOUDNESS (12, 17)	The output signal on these pins is a voltage taken from the volume attenuator's −40 dB tap point. An external R–C network is connected to these pins.
MAIN OUTPUT (13, 16)	The output signal from these pins drives a stereo power amplifier. The output can typically sink 1 mA.
BYPASS (14)	A 10 μF capacitor is connected between this pin and ground to provide an AC ground for the internal half-supply voltage reference.
GROUND (15)	This pin is connected to analog ground.
V^+ (26)	This is the power supply connection. The LMC1983 is operational with supply voltages from 6V to 12V. This pin should be bypassed to ground through a 1.0 μF capacitor.
ID (27)	This is the IDENTITY digital input that, when low, signals the LMC1983 to receive, from a controlling device, a device address (40_H–47_H), present on the DATA line.

Pin Description (Continued)

DATA (28) This is the serial data input for communications sent by a controller. The controller must have open drain outputs used with external pull-up resistors. The data rate has a maximum frequency of 1 MHz. The LMC1983 requires 16 bits of data to control or change a function: the first 8 bits select the LMC1983 and one of eight functions. The final eight bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

General Information

The LMC1983 is a CMOS/bipolar building block intended for high fidelity audio signal processing. It is designed for line level inputs signals (300 mV – 2V) and has a maximum gain of −0.5 dB. While the LMC1983 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and poly-silicon resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment. Internal circuits set the volume to minimum, tone controls to flat, the mute to on, and all other functions off when power is first applied. Individual left and right volume controls are software programmed to achieve the stereo balance function. *Figure 1* shows the connection diagram of a typical LMC1983 application.

The LMC1983 has internal decoding logic that allows a microprocessor (μP) or microcontroller (μC) to communicate directly to the audio control circuitry through an INTERMETAL (IM) Bus interface. This three-wire interface consists of a bi-directional DATA line, a Clock (CLK) input line, and an Identity (ID) line. Address and function selection data (8 bits) are serially shifted from the controller to the LMC1983. This is followed by 8 bits of function value data. Data present in the internal shift register is latched and the instruction is executed.

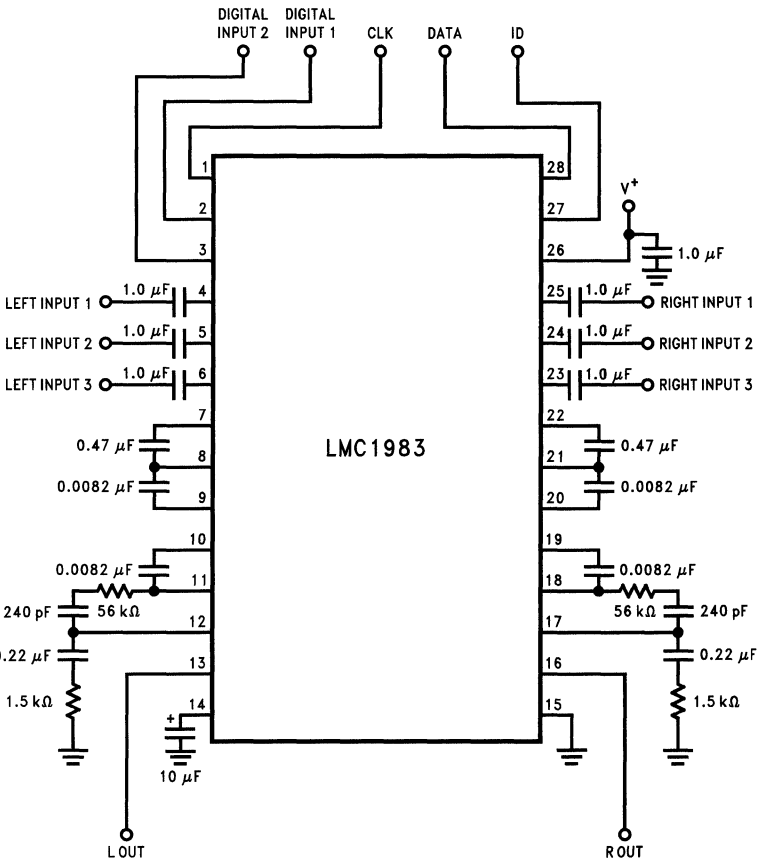


FIGURE 1. Typical Application

Application Information

INPUT SELECTOR

The LMC1983's input selector and mode control are shown in *Figure 2*. The input selector selects one of three stereo signal sources or a mute function with typical attenuation of 100 dB. The selected signals are then sent to a mode control matrix. As shown in Table I, the matrix provides normal stereo or can direct any given channel to both LEFT or RIGHT SELECT OUTPUTs. The third matrix mode is normal stereo. The control matrix output is buffered and appears on each channel's respective SELECT OUT pin (7, 22). Switching noise is kept to a minimum when mute is selected by using a 50 kΩ bias resistor.

Noise performance is optimized through the use of emitter followers in the mode control matrix's output. Internal 50 kΩ resistors are connected to each input selector pin to provide the proper bias point for the emitter follower buffers. Each internal 50 kΩ bias resistor is connected to a common half-supply ($V^+/2$) source. This produces a voltage at pins 7 and 22 (SELECT OUT) that is 1.4V below $V^+/2$ (typically 3.1V with $V^+ = 9V$). Since a DC voltage is present at the input pins (4, 5, 6, 23, 24, and 25), input signals should be AC coupled through a 1 μF capacitor.

The output signal at pins 7 and 22 can be used to drive exteral audio processing circuits such as noise reduction (LM1894–DNR or Dolby) or graphic equalizers (LMC835). It is important that if any noise reduction is used it be placed ahead of any tone controls or equalizers in the external circuit path to preserve the frequency spectrum of the selected input signal. Otherwise, any frequency equalization could prevent the proper operation of the noise reduction circuit. If no external processor is used, a capacitor should be used to couple the SELECT OUT signals directly to pins 8 and 21, respectively.

MINIMUM LOAD IMPEDANCE

The LMC1983 employs emitter-followers to buffer the selected stereo channels. The buffered signals are available at pins 7 and 22 (SELECT OUT). The SELECT OUT buffers operate with a typical bias current of 1 mA.

The Electrical Specifications table lists a maximum input signal of 2.0 V_{rms} (2.8 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum AC load impedance seen by the SELECT OUT pins is 2.5 kΩ (2.5V/1 mA). Using lower load impedances results in clipping at lower output levels. If the load impedance is DC-coupled, an increased quiescent current can flow. Latch-up may occur if the total emitter current exceeds 5 mA. Thus, maximum output voltage can be increased and much lower distortion levels can be achieved using load impedances of at least 25 kΩ.

INPUT IMPEDANCE

The input impedance of pins 4, 5, 6, 23, 24 and 25 is defined by internal bias resistors and is typically 50 kΩ.

The SELECT IN pins have an input impedance that varies with the BASS and TREBLE control settings. The input impedance is 100 kΩ at DC and 19 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 30.4 kΩ at DC and 16 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 6.8 kΩ and, with the tone controls at maximum boost, is 2.5 kΩ.

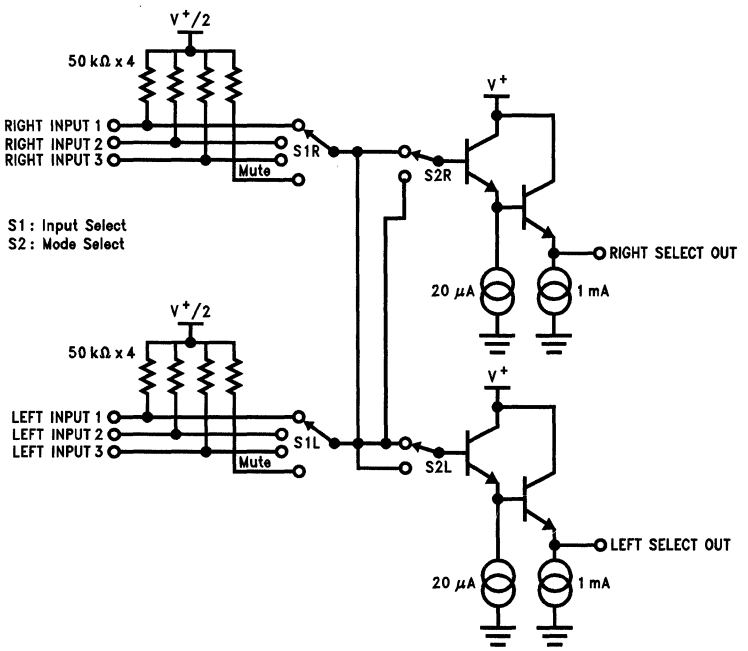


FIGURE 2. Input and Mode Select Circuitry

Application Information (Continued)

TABLE I. IM Bus Programming Codes for LMC1983

Address (A7–A0)	Function	Data	Function Selected
01000000	Input Select + Mute	XXXXXX00	INPUT1
		XXXXXX01	INPUT2
		XXXXXX10	INPUT3
		XXXXXX11	MUTE
01000001	Loudness	XXXXXXX0	Loudness **OFF**
		XXXXXXX1	Loudness **ON**
01000010	Bass	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000011	Treble	XXXX0000	−12 dB
		XXXX0011	−6 dB
		XXXX0110	FLAT
		XXXX1001	+6 dB
		XXXX11XX	+12 dB
01000100	Left Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000101	Right Volume	XX000000	0 dB
		XX010100	−40 dB
		XX101XXX	−80 dB
		XX11XXXX	−80 dB
01000110	Mode Select	XXXXX100	Left Mono
		XXXXX101	Stereo
		XXXXX11X	Right Mono
01000111	Read Digital Input 1 or Digital Input 2 on IM Bus	XXXXXXD1D0	D0 = Digital Input 1 D1 = Digital Input 2

Application Information (Continued)

EXTERNAL SIGNAL PROCESSING

The SELECT OUT pins (7 and 22) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or multi-band graphic equalizers (LMC835). If both are used, it is important to ensure that the noise reduction circuitry precede the equalization circuits. Failure to do so results in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the LMC1983. The tone controls use just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 (see *Figure 4*) and internal resistors in the feedback loop of the internal tone amplifier. The maximum-boost or cut is determined by the data sent to the LMC1983 (see Table I).

The typical tone control response shown in Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response is referred to as the turn-over frequency. With C = C2 = C3, the LMC1983's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14\ k\Omega)}$$

The bass turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(30.4\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(1.9\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(169.6\ k\Omega)}$$

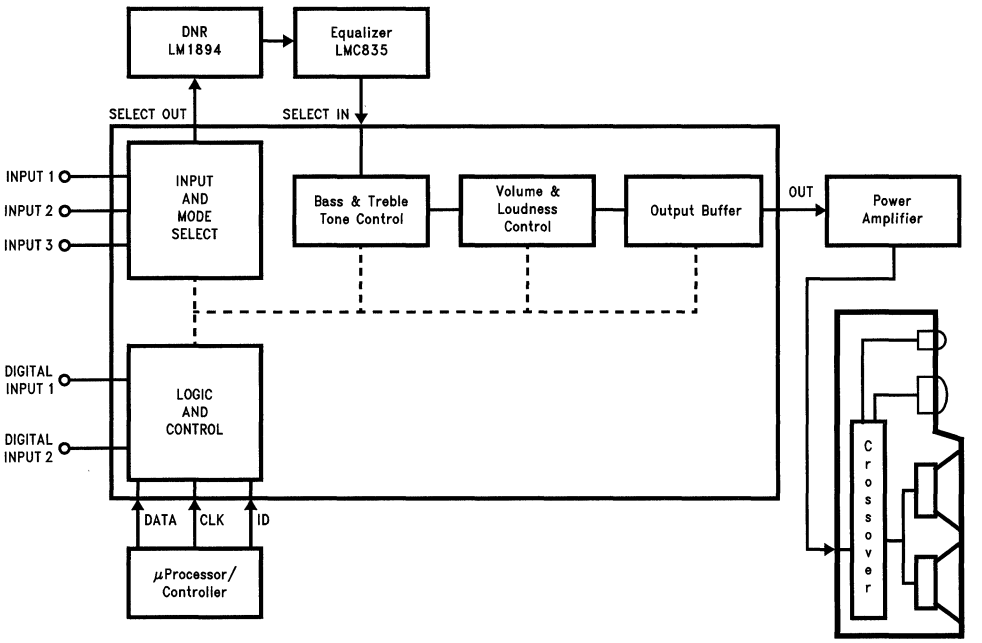


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FIGURE 3. System Block Diagram Utilizing the External Processing Loop (One Channel Shown)

Application Information (Continued)

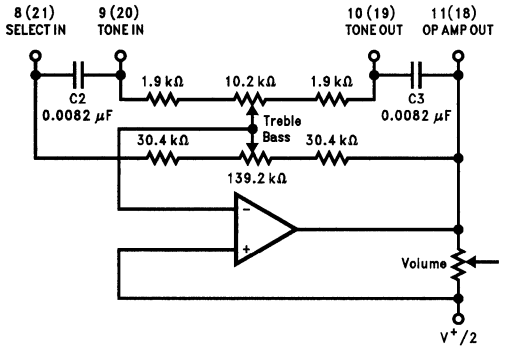

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FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 μF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C2 = C3 = 0.0068 μF the 2 dB steps take place at 130 Hz and 11.2 kHz.

LOUDNESS

The human ear has less sensitivity to high and low frequencies relative to its sensitivity to mid-range frequencies between 2 kHz and 6 kHz for any given acoustic level. The low and high frequency sensitivity decreases faster than the sensitivity to the mid-range frequencies as the acoustic level drops. The LMC1983's loudness function can be used to help compensate for the decreased sensitivity by boosting the gain at low and high frequencies as the volume control attenuation increases (see the curve labeled "Gain vs Frequency with Loudness Active").

The LMC1983's loudness function uses external components R1, R2, C4 and C5, as shown in *Figure 5*, to select the frequencies where bass and treble boost begin. The amount of boost is dependent on the volume attenuator's setting. The loudness characteristic, with the volume attenuator set at 40 dB, has a transfer function of

$$\frac{V_O}{V_I} = \frac{(sC5R2 + 1)[sC4(R1 + 156k) + 1]}{(s^2)C4C5R2(163k) + s[C4(156k) + C5(4.9R2 + 156k)] + 1}$$

The external components R1 and C4 can be eliminated and pin 11(18) left open if bass boost is the only desired loudness characteristic.

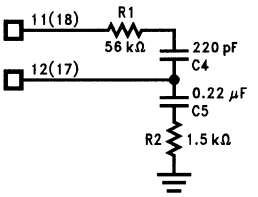

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FIGURE 5. Loudness Control Circuit

SERIAL DATA COMMUNICATION

The LMC1983 uses the INTERMETAL serial bus (IM Bus) standard. Serial data information is sent to the LMC1983 over a three wire IM Bus consisting of Clock (CLK), Data (DATA), and Identity (ID). The DATA line is bidirectional and the CLK and ID lines are unidirectional from the microprocessor or micontroller to the LMC1983. The LMC1983's bidirectional capability is accomplished by using an open drain output on the DATA line and an external 1 kΩ pull-up resistor.

The LMC1983 responds to address values from 01000000 (40_H) through 01000111 (47_H). The addresses select one of the eight available functions (see Table I). The IM Bus' lines have a logic high standby state when using TTL logic levels. As shown in *Figure 6*, data transmission is initiated by low levels on CLK and ID. Next, eight address bits are sent. This address information includes the code to select one of the LMC1983's desired functions. Each address bit is clocked in on the rising edge of CLK. The ID line is taken high after the eight bits of address data are received by the LMC1983.

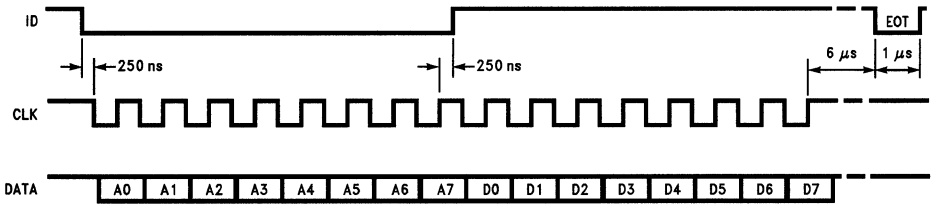

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FIGURE 6. LMC1983's INTERMETAL Serial Bus Timing

Application Information (Continued)

The controlling system continues toggling the CLK line eight more times. Data that determines the selected function's operating point is written into, or single bit information on DIGITAL INPUT 1 or DIGITAL INPUT 2 is read from, the LMC1983. Finally, the end of transmission is signaled by pulsing the ID line low for a minimum of 3 μs. The transmitted function data is latched and the function changes to its new setting.

Table I also details the serial data structure, range, and bit assignments that sets each function's operating point. The volume and tone controls' function control data binarily increments from zero to maximum as the function's operating point changes from 80 dB attenuation to 0 dB attenuation (volume) or −12 dB to +12 dB (tone controls). Note that not all data bits are needed by each function. The extra bits shown as "X"s ("don't cares") are position holders and have no affect on a respective control. They are necessary to properly position the data in the LMC1983's internal data shift register. Unexpected results may take place if these bits are not sent.

The LMC1983's internal data shift register can handle either a 16-bit word or two 8-bit serial data transmissions. It is the final 8 bits of data received before the ID line goes high that are used as the LMC1983 selection and function addresses. The final eight bits after the ID line returns high are used to change a function's operating point. CLK must be stopped when the final 8 data bits are received. The data stored in the internal data latch remains unchanged until the ID is pulsed, signifying the end of data transmission. When ID is pulsed, the new data in the data shift register is latched into the data latch and the selected function takes on a new operating point.

A complete description and more information concerning the IM Bus is given in the appendix of ITT's CCU2000 datasheet.

DIGITAL I/O

The LMC1983's two Digital Input pins, 2 and 3, provide single-bit communication between a peripheral device and the controller over the IM Bus. Each pin has an internal 30 kΩ pull-up resistor. Therefore, these pins should be connected to open collector/drain outputs. The type of information that could be received on these lines and retrieved by a controller include FM stereo pilot indication, power on/off, Secondary Audio Program (SAP), etc.

According to Table I, the logic state of DIGITAL INPUT 1 and DIGITAL INPUT 2 is latched and can be retrieved over the IM Bus using the read command (47_H). The single-bit information sent on the IM Bus is active low since these lines are internally pulled high.

National Semiconductor

LMC1992 Digitally-Controlled Stereo Tone and Volume Circuit with Four-Channel Input-Selector

General Description

The LMC1992 is a monolithic integrated circuit that provides four stereo inputs, bass and treble tone controls, and volume, balance, and front-rear fader controls. These functions are digitally controlled through a three-wire communication interface. All of the LMC1992s functions are achieved with only three external capacitors per channel. It is designed for line level input signals (300 mV − 2V) and has a maximum gain of 0 dB.

The internal design is optimized for external capacitors having values of 0.1 μF or less. This allows the use of chip capacitors for coupling and tone control functions.

Low noise and distortion result from using analog switches and thin-film silicon-chromium resistor networks in the signal path.

Volume and fader are at minimum and tone controls are flat when supply voltage is first applied.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1992's select-out/select-in external processor loop.

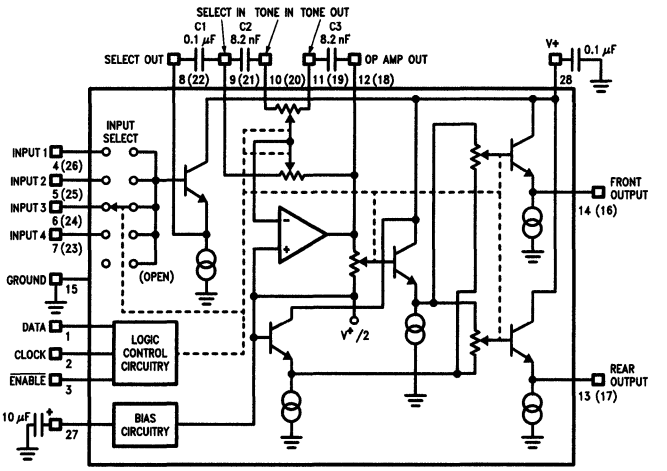
Features

- Low noise and distortion
- Four stereo inputs
- 40 volume levels including mute
- 20 fader levels
- All attenuators have a 2 dB of attenuation per step
- Front/back fade control
- External processor loop
- Only three external components per channel
- Serial programmable: standard MICROWIRE™ interface
- Single supply operation: 6V to 12V supply voltage
- Protection address (similar to DS8906)
- DC-coupled inputs
- Single supply operation

Applications

- Automotive audio systems
- Sound reinforcement systems
- Home entertainment—stereo television and music reproduction systems
- Electronic music (MIDI)

Block and Connection Diagrams



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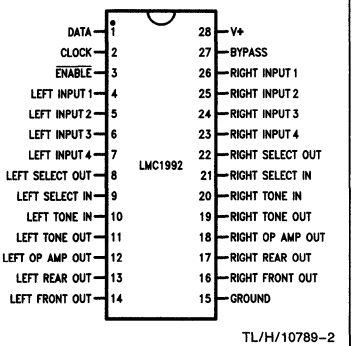
Left channel shown. Pin numbers in parentheses are for the right channel.



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Order Number LMC1992CCN
See NS Package Number N28B

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - GND$)	15V
Voltage at Any Pin	GND − 0.2V to V^+ + 0.2V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Junction Temperature	125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, Soldering, 10 sec.	+260°C
ESD Susceptibility (Note 5)	2000V
Pins 9, 10, 11, 19, 20, 21	850V

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC1992CCN	$0°C \le T_A \le 70°C$
Supply Voltage ($V^+ - V^-$)	6V to 12V

Electrical Characteristics

The following specifications apply for $V^+ = 8V$, $f_{IN} = 1$ kHz, input signal applied to channel 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and faders = 0 dB unless otherwise specified. All limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
I_S	Supply Current			27.0	mA (max)
V_{IN}	Input Voltage	Clipping Level (1.0% THD), Select Out (Pins 8, 22)	2.3	2.0	V_{rms}(min)
V_{OUT}	Output Voltage	Clipping Level (1.0% THD), Outputs (Pins 13, 14, 16, 17)	1.2	0.65	V_{rms}(min)
THD	Total Harmonic Distortion	All Four Channels			
		Volume Attenuator at 0 dB, Input Level 0.3 V_{rms}	0.15	0.3	% (max)
		Volume Attenuator at −20 dB, Input Level 0.6 V_{rms}	0.03	0.1	% (max)
E_{nOUT}	Output Noise	All Four Channels CCIR/ARM Filter, $R_S = 0\Omega$	6.5	30.0	μV_{rms} (max)
E_{nOUT}	Output Noise	All Four Channels CCIR/ARM Filter, $R_S = 0\Omega$ Volume Attenuator = −80 dB	5.0	20.0	μV_{rms} (max)
R_{OUT}	DC Output Impedance	Pins 8, 22	100	150	Ω (max)
		Pins 13, 14, 16, 17	80	120	Ω (max)
R_{IN}	DC Input Impedance	Pins 4, 5, 6, 7, 23, 24, 25, 26	2		MΩ
	Volume Attenuator Range	Pins 16, 17; Volume Attenuation at 0101110100X (0 dB); (Absolute Gain)	−1.0	−1.5	dB (max)
		01011000000 (80 dB); (Relative to Attenuation at the 0 dB setting)	80.0	75.0	dB (min)
	Volume Step Size	All Volume Attenuation Settings from 01011001010 (60 dB) to 0101110100X (0 dB) (Note 9)	2.0	0.7 4.3	dB (min) dB (max)
	Channel-to-Channel Volume Tracking Error	Fader Attenuation from 1XXX000000 (40 dB) to 1XXX1010X (0 dB)	±0.5	±1.0	dB (max)
	Fader Attenuation Range	Pins 16, 17; Fader Attenuation at 011XXX1010X (0 dB); (Absolute Gain)	−1.0	−1.5	dB (max)
		011XXX00000 (40 dB); (Relative to Attenuation at the 0 dB setting)	40	38.0	dB (min)
	Fader Step Size	All Fader Attenuation Settings from 011XXX00000 (40 dB) to 011XXX1010X (0 dB) (Note 10)	2.0	1.0 4.5	dB (min) dB (max)

Electrical Characteristics The following specifications apply for $V^+ = 8V$, $f_{IN} = 1$ kHz, input signal applied to channel 1, volume = 0 dB, bass = 0 dB, treble = 0 dB, and faders = 0 dB unless otherwise specified. All limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 6)	Limit (Note 7)	Units (Limit)
	Bass Gain Range	f_{IN} = 100 Hz, Pins 14, 16	±12	±10.0	dB (min)
	Bass Tracking Error	f_{IN} = 100 Hz, Pins 14, 16	±0.1	±1.0	dB (max)
	Bass Step Size	f_{IN} = 100 Hz, Pins 14, 16 (Relative to Previous Level)	2.0	1.0 3.0	dB (min) dB (max)
	Treble Gain Range	f_{IN} = 10 kHz, Pins 14, 16	±12	±10.0	dB (min)
	Treble Tracking Error	f_{IN} = 10 kHz, Pins 14, 16	±0.1	±1.0	dB (max)
	Treble Step Size	f_{IN} = 10 kHz, Pins 14, 16 (Relative to Previous Level)	2.0	1.0 3.0	dB (min) dB (max)
	Frequency Response	−3 dB −0.3 dB (Relative to Signal Amplitude at 1 kHz)	450	 20	kHz kHz (min)
	Channel Separation	V_{IN} = 1.0 V_{rms}	97	70	dB (min)
	Input-Input Isolation	V_{IN} = 1.0 V_{rms} (Note 8)	90	70	dB (min)
PSRR	Power Supply Rejection Ratio	V^+ = 8 V_{DC}; 100 mV_{P-P}, 100 Hz Sinewave Applied to Pin 28	40	31	dB (min)
f_{CLK}	Clock Frequency		1.0	0.5	MHz (max)
$V_{IN(1)}$	Logic "1" Input Voltage		1.3	2.0	V (min)
$V_{IN(0)}$	Logic "0" Input Voltage		0.4	0.8	V (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are specified with respect to ground.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 4: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, ϕ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMC1992CCN, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W.

Note 5: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

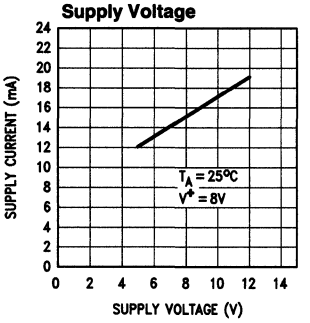
Note 8: The Input-Input Isolation is tested by driving one input and measuring the front outputs when the undriven inputs are selected.

Note 9: The Volume Step Size is defined as the change in attenuation between any two adjacent volume attenuation settings. The nominal Volume Step Size is 2 dB.

Note 10: The Fader Step Size is defined as the change in attenuation between any two adjacent fader attenuation settings. The nominal Volume Step Size is 2 dB.

Typical Performance Characteristics

Quiescent Current vs Supply Voltage



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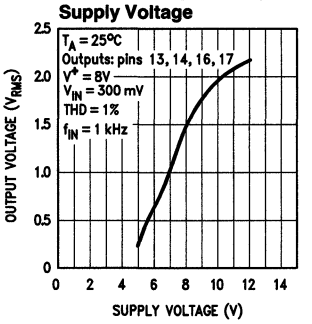
Maximum Output Swing vs Supply Voltage



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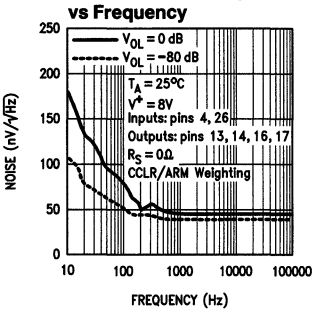
Output Noise Voltage vs Frequency



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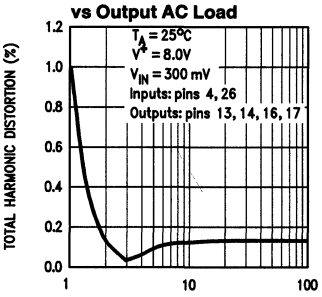
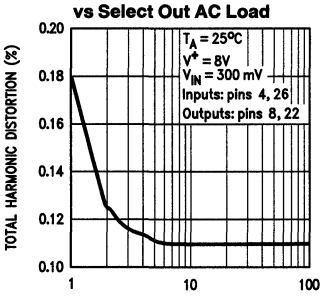
Total Harmonic Distortion vs Output AC Load



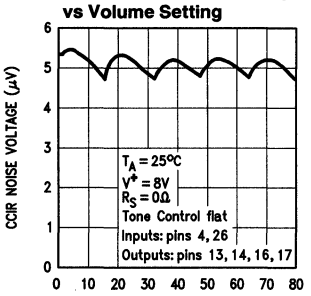
TL/H/10789–6

Total Harmonic Distortion vs Select Out AC Load



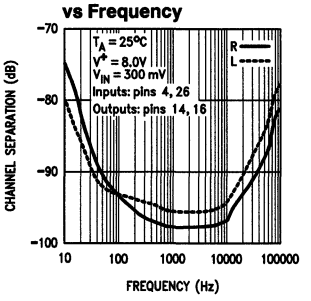
TL/H/10789–7

CCIR Output Noise Voltage vs Volume Setting



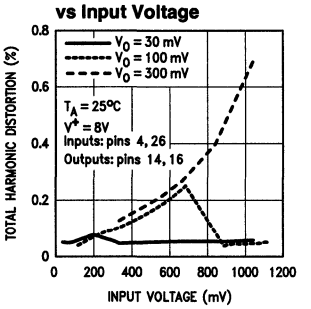
TL/H/10789–8

Channel Separation vs Frequency



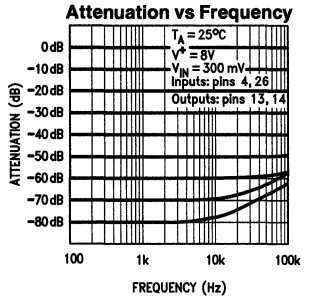
TL/H/10789–9

Total Harmonic Distortion vs Input Voltage



TL/H/10789–10

Attenuation vs Frequency



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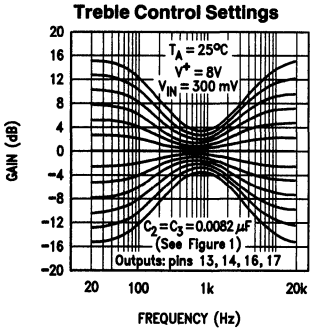
Typical Performance Characteristics (Continued)

Tone Control Response with Equal Bass and Treble Control Settings



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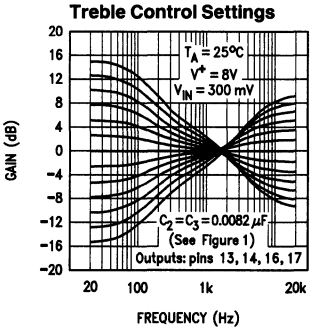
Tone Control Response with Reciprocal Bass and Treble Control Settings



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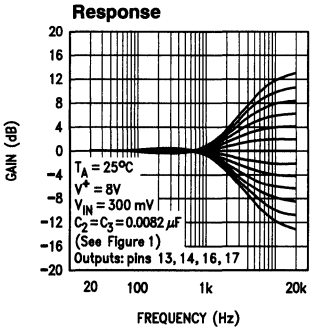
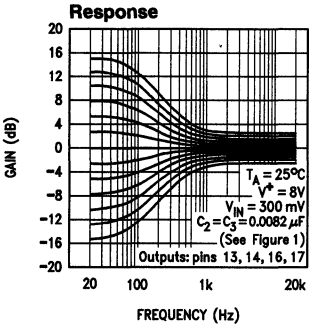
Treble Tone Control Response



TL/H/10789–14

Bass Tone Control Response



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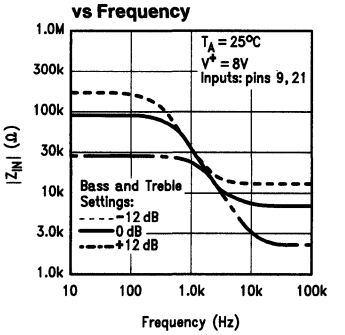
Select In Impedance vs Frequency



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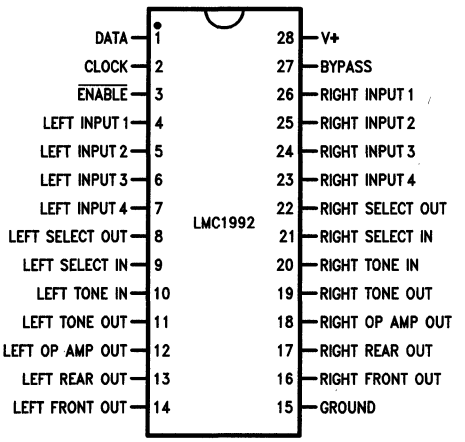
Connection Diagram



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Pin Description

DATA(1) This is the serial data input for communications sent by a controller. The data rate has a maximum frequency of 500 kHz. The LMC1992 requires 11 bits of data to control or change a function: the first two bits, a 1 and 0, select the LMC1992, the next three bits select a function, and the final six bits set the function to a desired value. The data must be valid on the rising edge of the CLOCK input signal.

CLOCK(2) The CLOCK input accepts a TTL or CMOS level clocking signal. The input is used to clock the DATA input signal and determines when a data bit is valid.

$\overline{\text{ENABLE}}$(3) This input accepts a logic low signal when a controller is addressing the LMC1992. When $\overline{\text{ENABLE}}$ is active, the LMC1992 responds to input signals present on the DATA and CLOCK inputs.

INPUT 1–4 (4–7, 23–26) Four two-channel analog inputs are available on the LMC1992. These pins should be dc-biased to mid-supply.

SELECT OUT (8, 22) The selected INPUT signal is available at this output. This feature allows the use of external signal processing such as noise reduction or graphic equalizers. This output can typically sink 1 mA.

SELECT IN (9, 21) This is the input that an external signal processor uses to return a signal to the LMC1992.

TONE IN (10, 20) This is the input to the tone control amplifier. See the Application Information section titled "Tone Control Response".

TONE OUT (11, 19) Tone control amplifier output. See the Application Information section titled "Tone Control Response".

OP AMP OUT (12, 18) This output is used externally with the tone control capacitors. Internally, this output is applied to the volume attenuators.

REAR OUT (13, 17) This pin's output signal is intended for the rear amplifiers in a four speaker stereo system. The output can typically sink 350 μA.

FRONT OUT (14, 16) This pin's output signal is intended for the front amplifiers in a four speaker stereo system. The output can typically sink 350 μA.

GROUND (15) This is the system ground connection.

V^+ (28) This is the power supply connection. The LMC1992 is operational with supply voltages from 6V to 12V. It is recommended that this pin is bypassed with 0.1 μF capacitor.

BYPASS (27) A 10 μF capacitor is connected between this pin and ground.

General Information

The LMC1992 is a CMOS/bipolar high quality building block intended for high fidelity audio signal processing. It is designed for line level input signals (300 mV − 2V) and has a maximum gain of −1 dB. While the LMC1992 is manufactured with CMOS processing, NPN transistors are used to build low noise op amps. The combination of CMOS switches, bipolar op amps, and SiCr resistors make it possible to achieve an order of magnitude quality improvement over other bipolar circuits that use analog multipliers to accomplish gain adjustment.

The LMC1992 has internal decoding logic that allows a computer (μP) to communicate directly to the audio control circuitry through a standard MICROWIRE interface. This three-wire interface consists of a DATA input line, a CLOCK input line, and an $\overline{\text{ENABLE}}$ line. When the $\overline{\text{ENABLE}}$ line is low, data can be serially shifted from the controller to the LMC1992. As the $\overline{\text{ENABLE}}$ line goes through the low-to-high transition, any additional data is ignored. Data present in the internal shift register is latched and the instruction is executed.

Figure 1 shows the connection diagram of a typical LMC1992 application.

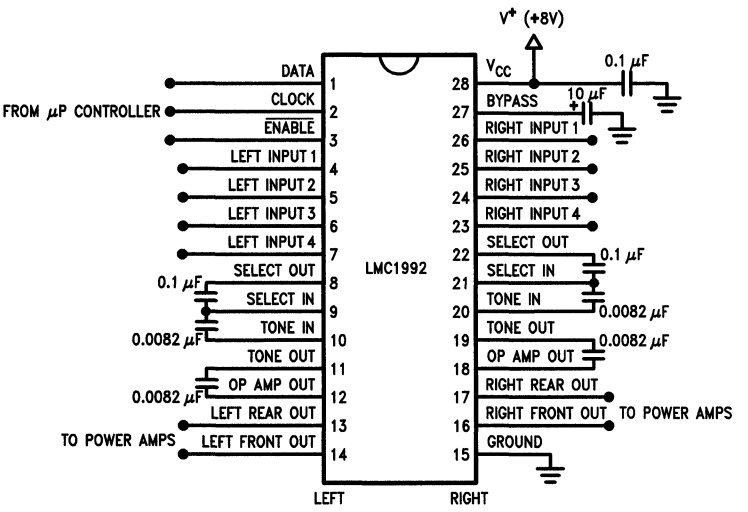

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FIGURE 1. Typical Connection Diagram

Applications Information

MINIMUM LOAD IMPEDANCE

The LMC1992 employs emitter-follower buffers at pins 8 and 22 (SELECT OUT), 13 and 14 (LEFT FRONT and REAR OUTPUTs), and 16 and 17 (RIGHT FRONT-and-REAR OUTPUTs) that buffer output signals. Typical bias current of 1 mA is used for the SELECT OUTPUT buffers and 350 μA for the LEFT-and-RIGHT, FRONT-and-REAR OUTPUT buffers.

The Electrical Specifications table lists a maximum input signal of 2.3 V_{rms} (3.25 V_{peak}) for 1% THD at the SELECT OUT pins. This distortion level is achieved when the minimum ac load impedance seen by the SELECT OUT pin is 3.25 kΩ (3.25V/1 mA). For the LEFT-and-RIGHT, FRONT-and-REAR OUTPUTs, the typical maximum output is 1.2 V_{rms} (1.55 V_{peak}). Therefore, the minimum load impedance is 4.43 kΩ (1.55 V/0.35 mA). Trying to use a lower impedance results in a clipped output signal. Therefore, *the chance of clipping can be greatly reduced and much lower distortion levels can be achieved by using load impedances that are an order of magnitude higher than shown here.*

For applications that require dc coupling and the INPUTs biased to $V^+/2$, the minimum load impedance will differ from that detailed in the above discussion. The emitter followers may be potentially operating at high currents because there is a dc voltage $V^+/2 - 0.7V$ at the SELECT OUT pins; dc resistance to ground will result in increased current flow. Latch-up may occur if the total emitter current exceeds 5 mA. This current is a combination of the emitter follower's 1 mA current source and 4 mA drawn by the external load. Therefore, to prevent this possibility, the minimum dc load impedance should be

$$\frac{V_{peak} + (V^+/2 - 0.7V)}{4\ mA} = 1638\Omega$$

$V_{peak} = 3.25V$

$V^+ = 8V$

To allow for variations and part tolerances, 2.0 kΩ is a good choice for this minimum dc load impedance.

When dc coupling is used at the LEFT-and-RIGHT, FRONT-and-REAR OUTPUTs, the output emitter followers will be operating at a nominal dc voltage of $V^+/2 - 2(0.7V)$. Latch-up may occur if the total emitter current exceeds 1 mA. This current is a combination of the emitter follower's 0.35 mA current source and 0.65 mA drawn by the external load. Therefore, to prevent this possibility, the minimum dc load impedance should be

$$\frac{V_{peak} + (V^+/2 - 2(0.7V))}{0.65\ mA} = 9\ k\Omega$$

$V_{peak} = 3.25V$

$V^+ = 8V$

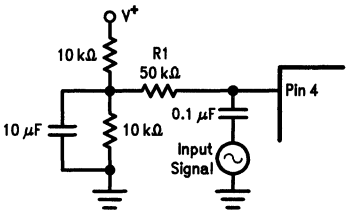

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FIGURE 2. Input Bias Network

To allow for variations and part tolerances, 10 kΩ is a good choice for this minimum dc load impedance.

INPUT IMPEDANCE

For ac coupled input signals the input impedance value is determined by bias resistor R1, as shown in *Figure 2.* A directly coupled input signal will see an emitter follower's nominal input impedance of 2 MΩ.

The SELECT IN pins have an input impedance that varies with the BASS and TREBLE control settings. The input impedance is 96 kΩ at dc and 27 kΩ at 1 kHz when the controls are set at 0 dB. Minimum input impedance of 28 kΩ at dc and 24 kΩ at 1 kHz occurs when maximum boost is selected. At 10 kHz the minimum input impedance, with the tone controls flat, is 8 kΩ and, with the tone controls at maximum boost, is 3 kΩ.

STEREO SIGNAL INPUTS

When operating with a single supply voltage, the stereo signal inputs must be dc biased to one-half of the supply voltage, as shown in *Figure 2.* As an example, with a supply voltage of 8V, all signal sources should have a dc bias of 4V. The maximum input signal level of 6.5 V_{p-p} (for 1% THD) would then swing from 0.75V to 7.25V. Input-to-input crosstalk can be minimized by using a separate dc bias circuit for each stereo input pair.

EXTERNAL SIGNAL PROCESSING

The signal present at the selected input will be available at the SELECT OUT pins 8 (left) and 22 (right). The dc bias voltage at those pins will be one base-emitter voltage, approximately 0.7 V_{dc}, below the source because of the internal emitter follower. Therefore, if the selected input has a bias of 4.0 V_{dc} the dc component at pins 8 and 22 will be about 3.3 V_{dc}.

The LMC1992's SELECT OUT emitter followers allow additional signal sources using emitter follower outputs (such as multiple LMC1992s) to be "wired-ORed" together. When this feature is in use, the input channel of the LMC1992 not in use should be set to "open" input codes 01000XX0000 or 01000XX011X.

Applications Information (Continued)

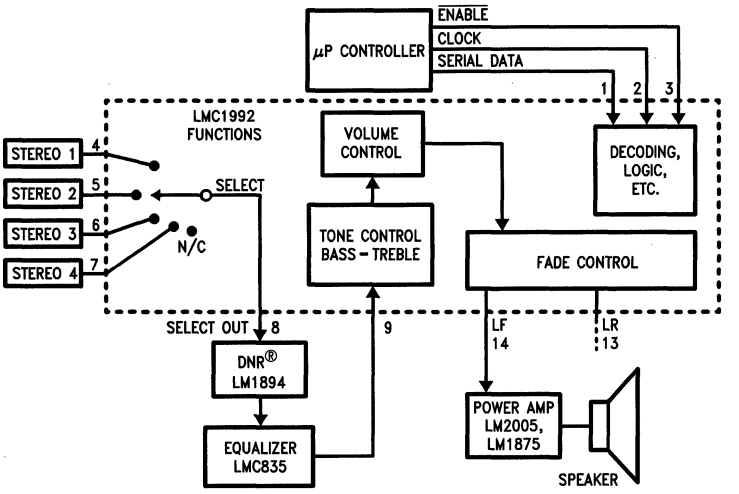

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FIGURE 3. System Block Diagram Showing Inclusion of DNR® Noise Reduction (LM1894) and Equalizer (LMC835) (One Channel Only—LMC1992)

The SELECT OUT pins (8 and 22) enable greater system design flexibility by providing a means to implement an external processing loop. This loop can be used for noise reduction circuits such as DNR (LM1894) or mulit-band graphic equalizers (LMC835). It is important to ensure that if both are used, the noise reduction circuitry precede the equalization circuits. Failure to do so will result in improper operation of the noise reduction circuits. The system shown in *Figure 3* utilizes the external loop to include DNR and a multi-band equalizer.

AUDIO MUTE

A mute function with attenuation of 100 dB is possible with the volume control set to −80 dB and the INPUT select code set to 01000XX0000 (open circuit).

TONE CONTROL RESPONSE

Base and treble tone controls are included in the LMC1992. The tone controls use just two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C2 and C3 *(Figure 4)* and internal resistors in the feedback loop of the internal tone amplifier. The maximum amplitude boost or cut is determined by the data sent to the LMC1992 (see Table I).

The typical tone control response shown in the Typical Performance Curves were generated with C2 = C3 = 0.0082 μF and show the response for each step. When modifying the tone control response it is important to note that the ratio of C3 and C2 sets the mid-frequency gain. Symmetrical tone response is achieved when C2 = C3. However, with C2 = 2(C3) and the tone controls set to "flat", the frequency response will be flat at 20 Hz and 20 kHz, and +6 dB at 1 kHz.

The frequency where a tone control begins to deviate from a flat response will be referred to as the turn-over frequency. With C = C2 = C3, the LMC1992's treble turn-over frequency is nominally

$$f_{TT} = \frac{1}{2\pi C(14.2\ k\Omega)}$$

The base turn-over frequency is nominally

$$f_{BT} = \frac{1}{2\pi C(27.7\ k\Omega)}$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3 dB of the final value) are for treble and bass

$$f_{TI} = \frac{1}{2\pi C(2.3\ k\Omega)}$$

$$f_{BI} = \frac{1}{2\pi C(164.1\ k\Omega)}$$

Applications Information (Continued)

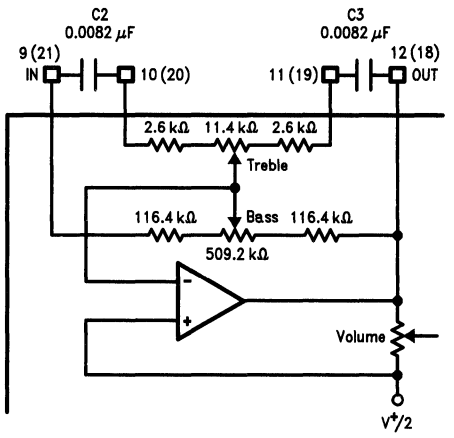

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FIGURE 4. The Tone Control Amplifier

Increasing the values of C2 and C3 decreases the turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Curves will shift left when C2 and C3 are increased and shift right when C2 and C3 are decreased. With C2 = C3 = 0.0082, 2 dB steps are achieved at 100 Hz and 10 kHz. Changing C2 and C3 to 0.01 µF shifts the 2 dB per step frequency to 72 Hz and 8.3 kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C2 = C3 = 0.0068 µF the 2 dB steps take place at 130 Hz and 11.2 kHz.

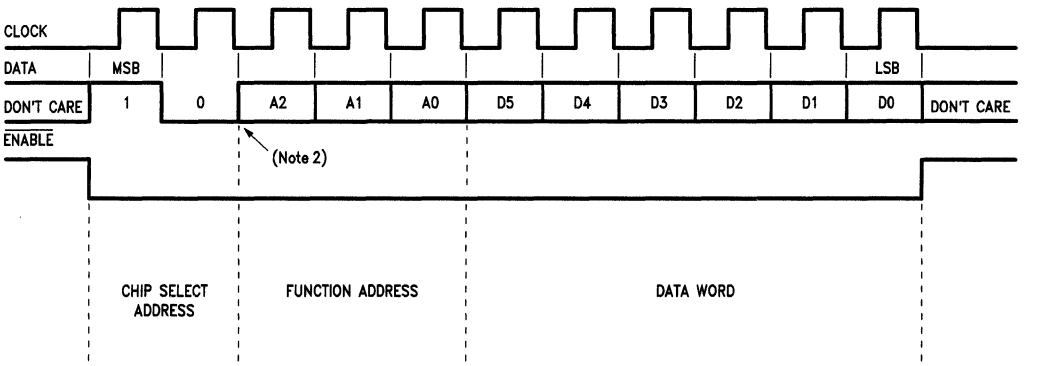
FADER FUNCTION

The four fader functions are all independently adjustable and therefore no balance control is needed. Emulating a balance control is accomplished through software by simultaneously changing a channel's front and rear faders by equal amounts. To satisfy normal balance requirements the faders have an attenuation range of 40 dB.

SERIAL COMMUNICATION INTERFACE

Figure 5 shows the LMC1992's timing diagram for its three wire MICROWIRE interface. A controller's data stream can be any length; once the correct device address is received by the LMC1992, any number of data bits can be sent; the last nine bits occurring before $\overline{\text{ENABLE}}$ goes high are used by the LMC1992. The first two bits in a valid data stream are decoded and used as device address bits. The LMC1992 uses a unique address of 1,0. The LMC1992 will not respond to information on the DATA line if any other address is used. This allows other MICROWIRE serially programmable devices to share the same three-wire communication bus. When $\overline{\text{ENABLE}}$ goes high, any further serial data is ignored and the contents of the shift register is transferred to the data latches. Only when information is received by the data latches do any function or setting changes take place. The first three of nine bits select one of the LMC1992s functions. The remaining six bits set the selected function to the desired value or position.

A data bit is accepted as valid and clocked into an internal shift register on each rising edge of the signal appearing at the LMC1992s CLOCK input pin. Proper data interpretation and operation is ensured when $\overline{\text{ENABLE}}$ makes its falling transition during the time when CLOCK is low. Erroneous operation will result if the $\overline{\text{ENABLE}}$ signal makes its falling transition at any other time.



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Note 1: Negative transition on $\overline{\text{ENABLE}}$ clears previous address. Clock must be low during transition.

Note 2: Additional don't care states may be inserted here for ease of programming. (Optional.)

Note 3: Positive transition on $\overline{\text{ENABLE}}$ latches in new data if the LMC1992 has been addressed. Clock can either be high or low during transition.

FIGURE 5. Clocking Data into the Standard MICROWIRE Interface (Minimum Number of Bits in Data Stream)

Applications Information (Continued)

TABLE I. Programming Codes for LMC1992

Address			Function	Data						Values
A2	A1	A0		D5	D4	D3	D2	D1	D0	
1	1	1	Left Rear Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
1	1	0	Right Rear Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
1	0	1	Left Front Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 − 20 dB = X01010 0 dB = X1010X
1	0	0	Right Front Fader	X	MSB	N	N	N	LSB	−40 dB = X00000 −20 dB = X01010 0 dB = X1010X
0	1	1	Volume	MSB	N	N	N	N	LSB	−80 dB = 000000 −40 dB = 010100 0 dB = 10100X
0	1	0	Treble	X	X	MSB	N	N	LSB	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	1	Bass	X	X	MSB	N	N	LSB	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	0	Input Select	X	X	0	MSB	N	LSB	OPEN = XX0000 INPUT1 = XX0001 INPUT2 = XX0010 INPUT3 = XX0011 INPUT4 = XX0100

Note 1: All attenuators 2 dB/step.

Note 2: Tone controls 2 dB/step @ 100 Hz and 10 kHz.

Note 3: Use of data that deviates from the values shown in the table may result in erroneous results.

SERIAL DATA FORMAT

Table I displays the required data format needed by the LMC1992. Not shown is the 2-bit device address (10). These two bits of information must precede the final nine-bits used as the data word. The first three of these nine bits is the function address.

The VOLUME, TONE, and FADER controls are designed to increment their settings (in 2 dB steps) as the control data is incremented by one LSB. Disregarding the device address and the function address, the VOLUME input code increases from 000000 (−80 dB) to 10100X (0 dB). The TONE controls' input code increases from XX0000 (−12 dB) to XX0110 (0 dB) to XX1100 (+12 dB). The code for the FADERs starts from X00000 (−40 dB) and goes to X1010X (0 dB).

The table shows that VOLUME is the only function that uses all six bits to choose that function's setting. The remaining functions use less than six bits; the unused bits are shown as "X"s ("don't care"). While these "don't care" bits have no effect on their respective function, the LMC1992 must receive them for proper operation. If neglected, erroneous or unknown results will occur.

Applications Information (Continued)

DATA TRANSFER EXAMPLE

The following routines, based on the flowchart shown in *Figure 6,* are examples of COPS™ microcontroller instruction code that can be used to control the LMC1992 (see National Semiconductor's COPS Microcontrollers Databook for more information). These routines arbitrarily select COPS register 0 for I/O purposes. When these routines are entered, it is assumed that chip select is high, SK (clock) is low, and SO (data) is low. These routines exit with chip select high and SK and SO low. Output port G0 is arbitrarily chosen to send the chip select signal to the LMC1992.

The 11 data bits needed to control the LMC1992 are assumed to be in the 4-bit registers, 13–15, with the 4 MSBs in register 13. With this configuration there is an extra bit for a data stream that is 12 bits long. As previously mentioned, there can be any number of extra bits between the device address and the function address.

DATA TRANSFER ROUTINE 1

This general purpose routine handles all the overhead except loading data into registers 13–15. It sends the data according to the conditions discussed above. The data will be lost at the conclusion of the routine. This routine consumes only 17 ROM memory locations.

```
OUT1:  LBI   0,13   ;POINT TO START OF DATA
                    ;WORD
       SC           ;SET C TO ENABLE SK CLOCK
       OGI   14     ;SELECT EXTERNAL DEVICE G0
                    ;= 0
       LEI   8      ;ENABLE SHIFT REGISTER
                    ;OUTPUT
SEND:  LD
       XAS          ;DATA TRANSMISSION LOOP
       XIS          ;TURN-ON CLOCK
       JP    SEND
       RC
       OGI   15     ;DE-SELECT EXTERNAL
                     DEVICE
       LEI   0      ;SET SO TO 0
       RET
```

DATA TRANSFER ROUTINE 2

This routine performs the same function as routine 1 while preserving the contents of the data registers. This routine takes only 21 ROM memory locations.

```
OUT1:  LBI   0,13   ;POINT TO START OF DATA
                    ;WORD
       SC           ;SET C TO ENABLE SK CLOCK
       OGI   14     ;SELECT EXTERNAL DEVICE
                    G0 ;=0
       LEI   8      ;ENABLE SHIFT REGISTER
                    ;OUTPUT
       JP    SEND2
SEND1: XAS
SEND2: LD           ;DATA TRANSMISSION LOOP
       XIS          ;TURN-ON CLOCK
       JP    SEND1
       XAS          ;SEND LAST DATA
       RC           ;WAIT 4 CYCLES - DATA
                    ;GOING OUT
       CLRA
       NOP
       XAS          ;TURN SK CLOCK OFF
       OGI   15     ;DE-SELECT DEVICE
       LEI   0      ;SET SO TO 0
       RET
```

Applications Information (Continued)

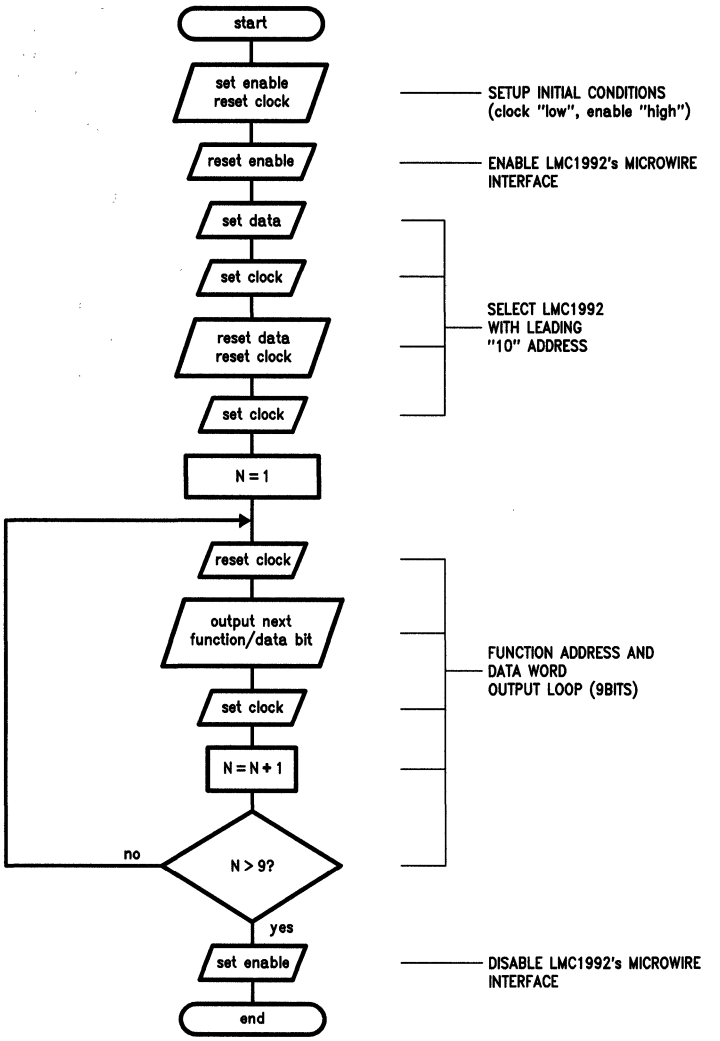

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FIGURE 6. General Data Transmission Flowchart to Send Serial Data to the LMC1992's MICROWIRE Compatible Digital Inputs

Section 2

Radio Circuits

Section 2 Contents

National Semiconductor

Radio Circuits
Definition of Terms

AGC dc Output Shift: The shift of the quiescent IC output voltage of the AGC section for a given change in AGC central voltage.

AGC Figure of Merit: The widest possible range of input signal level required to make the output signal drop by a specified amount from the specified maximum output level. Typical F.O.M. numbers are from 40 dB to 50 dB, for domestic radios and about 60 dB for automotive radios (for −10 dB output level change).

AGC Input Current: The current required to bias the central voltage input of the AGC section.

AM Rejection Ratio: The ratio of the recovered audio output produced by a desired FM signal of specified level and deviation to the recovered audio output produced by an unwanted AM signal of specified amplitude and modulating index.

Channel Separation: The level of output signal of an undriven amplifier with respect to the output level of an adjacent driven amplifier.

Detection Bandwidth: That frequency range about the free running frequency of the tone decoder/phase locked loop where a signal above a specified level will cause a detected signal condition at the output.

Detection Bandwidth Skew: The measure of how well the detection bandwidth is centered about the free running frequency. It is equal to the maximum detection bandwidth frequency plus the minimum detection bandwidth frequency minus twice the free running frequency.

Hold In Range: That range of frequencies about the free running frequency for which the phase locked loop will stay in lock if initially starting out in lock.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Sensitivity: The minimum level of input signal at a specified frequency required to produce a specified signal-to-noise ratio at the recovered audio output.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

−3 dB Limiting Sensitivity: In FM the input signal level which causes the recovered audio output level to drop 3 dB from the output level with a specified large signal input.

Lock In Range: That range of frequencies about the free running frequency for which the phase locked loop will come into lock if initially starting out of lock.

Maximum Sweep Rate: The maximum rate that the VCO may be made to vary its oscillating frequency over its Sweep Range.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Phase Detector Sensitivity: The change in the output voltage of the phase detector for a given change in phase between the two input signals to the phase detector.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated a 60W with $\leq$0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Sweep Range: That ratio of maximum oscillating frequency to minimum operating frequency produced by varying the central voltage of the VCO from its maximum value to its minimum value with fixed values of timing resistance and capacitance.

VCO Sensitivity: The change in operating frequency for a given change in VCO central voltage.

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Radio Circuits Selection Guide

AM RF/IF Detector

Device	Portable	Home	Auto	Synthesized	Pin Count (Dip Package)	Supply Range	Max Input Sensitivity for 20 dB S/N Ratio	AM and FM IF	Audio Power Amplifier	Internal Detector	Meter Output
LM1868	•	•			20	4.5-15V	12 μV	•	•	•	

*SO Surface Mount Package Only

Stereo Decoder

Device	Portable	Home	Auto	Pin Count Dip Package	Supply Range	THD	Separation	Blend	High Cut	Lamp Driver	Output Buffer	ARI Interference Rejection
LM4500A	•	•	•	16	8-16V	0.1%	40 dB			•	•	•

Modulators & Demodulators Selection Guide

	LM1211	LM1496
Typical Application	Broadband Demodulator	Balanced Modulator-Demodulator
Key Features	• Configurable for AM or FM Based Signals • 20 MHz–80 MHz Operating Frequency Range • 25 MHz Detector Output Bandwidth • Linear Output Phase Response	• Wide Frequency Response to 100 MHz • Fully Balanced Inputs and Outputs • Adjustable Gain and Signal Handling

FM IF/Detector

	Portable	Home	Auto	Synthesized	Pin Count Dip	Pin Count S.O.	Supply Range	−3 dB Limiting Sensitivity	THD	Mute	AGC Outputs	AFC	Meter Output	AM/ FM IF
LM1865		•	•	•	20	20	7.3-16V	60 μV*	0.1%	•	Reverse	•	•	
LM1868	•	•			20		4.5-15V	15 μV	1.1%					•
LM3089		•	•		16		8-16V	12 μV	0.5%	•	•	•	•	
LM3189		•	•		16		8-16V	12 μV	0.5%	•	•	•	•	
LM3361A**	•		•		16	16	2-9V	2 μV	-		•			

*Exclusive of 22 dB Buffer

**Narrow-Band FM-IF

National Semiconductor

LM1211 Broadband Demodulator System

General Description

The LM1211 is a high performance IF amplifier and product detection system for operation in the 20–80 MHz frequency range. It is suitable for data or video recovery from broadband local area networks and other communications systems.

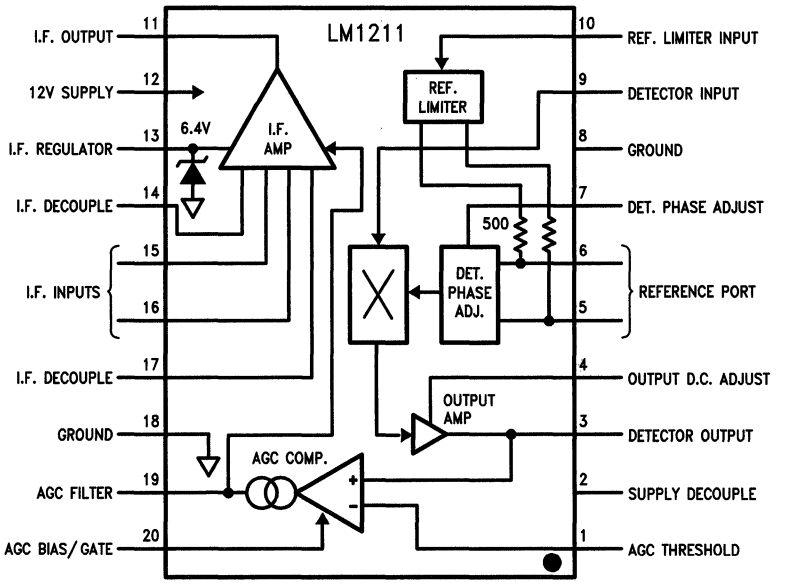
The high gain IF amplifier has a SAW filter compatible input and can be gain-controlled in excess of 40 dB. A flexible product detector is used in which the input signal is multiplied by a reference derived from limiting and phase-shifting the input. The signal input is separate from the reference path, which has a port for external connections. A DC-operated phase control is provided for detection phase adjustment.

The detector is followed by a 25 MHz bandwidth amplifier which has a symmetric output swing capability around 0V. A fast attack, peak-following AGC detector is also provided for use in AM systems.

Features

- Configurable for AM or FM based signals
- 20–80 MHz operating frequency range
- IF input SAW filter compatible
- >40 dB IF gain control range
- 25 MHz detector output bandwidth
- Linear output phase response
- Output swings ±3.5V referenced to ground
- Gateable peak-following AGC detector
- DC-adjustable detection phase
- DC-adjustable 0 carrier output level

Connection Diagram



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Order Number LM1211N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V12	15V
IF Supply Current, I13	40 mA
Detector Output Current, I3	15 mA
Detector Input Signal, V9	1 Vrms
Ref. Limiter Input Signal, V10	1 Vrms
AGC Bias/Gate Current, I20	3 mA
Power Dissipation	1.67W
Thermal Resistance	60°C/W
Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
ESD Susceptibility (Note 1)	3000V

DC Electrical Characteristics

T_A = 25°C, Test Circuit, $V_{IF} = V_{Det} = 0$, $V_{AGC} = 0$, $V_{PH} = 4V$, $V_{OC} = 6V$, all switches open unless noted.

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
I_S	Supply Current	SW 3 closed, $V_{AGC} = 3V$	67	80		mA (max)
V_{13}	IF Regulator Voltage	SW 3 closed, $V_{AGC} = 3V$	6.5	5.8 7.0		V (min) V (max)
$V_{15/16}$	IF Input Voltage	SW 2, 3 closed	3.9	3.4 4.4		V (min) V (max)
$V_{14}-V_{17}$	IF Decouple V_{OS}	SW 2, 3 closed, measure $V_{14}-V_{17}$	0	±50		mV (max)
I_{11}	IF Output Current	SW 2, 3 closed, $V_{AGC} = 6V$, $I_{11} = \frac{12V - V_{11}}{50}$	4.0	2.5 5.0		mA (min) mA (max)
V_{10}	Limiter Input Bias	SW 1, 2, 3 closed	5.1	4.5 5.5		V (min) V (max)
V_9	Detector Input Bias	SW 1, 2, 3 closed	5.1	4.5 5.5		V (min) V (max)
$V_{5/6}$	Reference DC Voltage	SW 1, 2, 3 closed	4.6	4.0 5.2		V (min) V (max)
V_3	O Carrier Output Voltage	SW 1, 2, 3 closed	0	±0.5		V (max)
V_{OC}	O Carrier Adjust Voltage	SW 1, 2, 3 closed, adjust V_{OC} for $V_3 = OV$	6.0	1.0 11.0		V (min) V (max)
$I_{19(D)}$	AGC Discharge Current	SW 1, 3 closed, $V_{AGC} = 2V$	−11	−7 −16		μA (min) μA (max)
$I_{19(C)}$	AGC Charge Current	SW 1, 4 closed, $V_{AGC} = 6V$	1.0	0.7 1.3		mA (min) mA (max)
$I_{19(L)}$	AGC Leakage Current	SW 1, 2, 4 closed, $V_{AGC} = 4V$	−25	±200		nA (max)

Note 1: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Detector AC Set-up Procedure

T_A = 25°C, Test Circuit, Sw 1, 2, 3 closed, V_{AGC} = 0, V_{PH} = 4V.

1. With no input (V_{Det} = 0), adjust V_{0C} for V3 = 0V.
2. Apply V_{Det} = 100 mVrms, 60 MHz CW at the input. Tune L2 for maximum DC voltage at output Pin 3.

AC Electrical Characteristics

T_A = 25°C, Test Circuit, Follow AC set-up procedure, f = 60 MHz, V_{AGC} = 0, V_{PH} = 4V, V_{0C} as per set-up, all switches open unless noted.

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limit)
Z15/16	IF Input Impedance	Measure Differential Impedance between Pins 15 and 16.	60		40 80	Ω (min) Ω (max)
Av(IF)	Maximum IF Gain (Note 3)	SW 2 Closed, V_{IF} = 0.5 mVrms, Measure V_{out}. Av(IF) = $20 \log \left(\frac{V_{out}}{5 \times 10^{-4}}\right)$	30	20		dB (min)
V_{AGC20}	20 dB Gain Reduction	SW 2 Closed, V_{IF} = 5 mVrms, Adjust V_{AGC} for Same V_{out} as in Av(IF) Test.	2.6	2.2 3.0		V (min) V (max)
V_{AGC40}	40 dB Gain Reduction	SW 2 Closed, V_{IF} = 50 mVrms, Adjust V_{AGC} for Same V_{out} as in Av(IF) Test.	3.8	3.3 4.3		V (min) V (max)
IM	IF Intermodulation (Note 3)	SW 2 Closed, f_1 = 60 MHz, f_2 = 65 MHz, V_{IF} = 10 mVrms Ea, Adjust V_{AGC} for V_{out} = 10 mVrms Ea, Measure IM Products Relative to V_{out}.	−40		−30	dB (min)
Z9	Detector Input Impedance	Measure Impedance into Pin 9	3.0		2.0 5.0	KΩ (min) pF (max)
Z10	Reference Limiter Input Impedance	Measure Impedance into Pin 10	2.0		1.3 5.0	KΩ (min) pF (max)
Av(D)	Detector Conversion Gain	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure V_{3DC}. Av(D) = $20 \log \left(\frac{V_3}{0.1}\right)$	24	20 30		dB (min) dB (max)
LIN	Detector-6dB Linearity	SW 1, 3 Closed, V_{Det} = 50 mVrms, Measure V_3'. LIN = $20 \log \left(\frac{V_3'}{V_3}\right)$	−6	−5 −7		dB (min) dB (max)
$V_{3(Th)}$	AGC Threshold	SW 1, 3 Closed, Increase V_{Det} until I19 = 100 μA, Measure V_3.	2.8		2.6 3.0	V (min) V (max)
$V_{3(OL)}$	Detector Overload Capability	SW 1, 2, 3 Closed, V_{Det} = 1 Vrms, Measure V_3.	4.1	3.5		V (min)
PHA(+)	DC Phase Adjust (+)	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure Ratio of V_3 with V_{PH} = 6V to V_3 with V_{PH} = 4V.	0.65	0.95		V/V (max)
PHA(−)	DC Phase Adjust (−)	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure Ratio of V_3 with V_{PH} = 2V to V_3 with V_{PH} = 4V.	0.30	0.60		V/V (max)
$V_{3(-)}$	Negative Output Swing	SW 1, 2, 3 Closed, f = 70 MHz, V_{Det} = 300 mVrms, V_{PH} = 6V, Measure V_3.	−3.7	−3.0		V (min)
DBW	Detector Output Bandwidth	SW 1, 2, 3 Closed, Modulate V_{Det} with 30% AM Modulation. Increase Modulation Frequency Until Pin 3 Signal Drops 3 dB.	25		20	MHz (min)
DHL	Detector Harmonic Levels	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure 60 MHz and 120 MHz Levels Relative to V_3	−35		−20	dB (min)

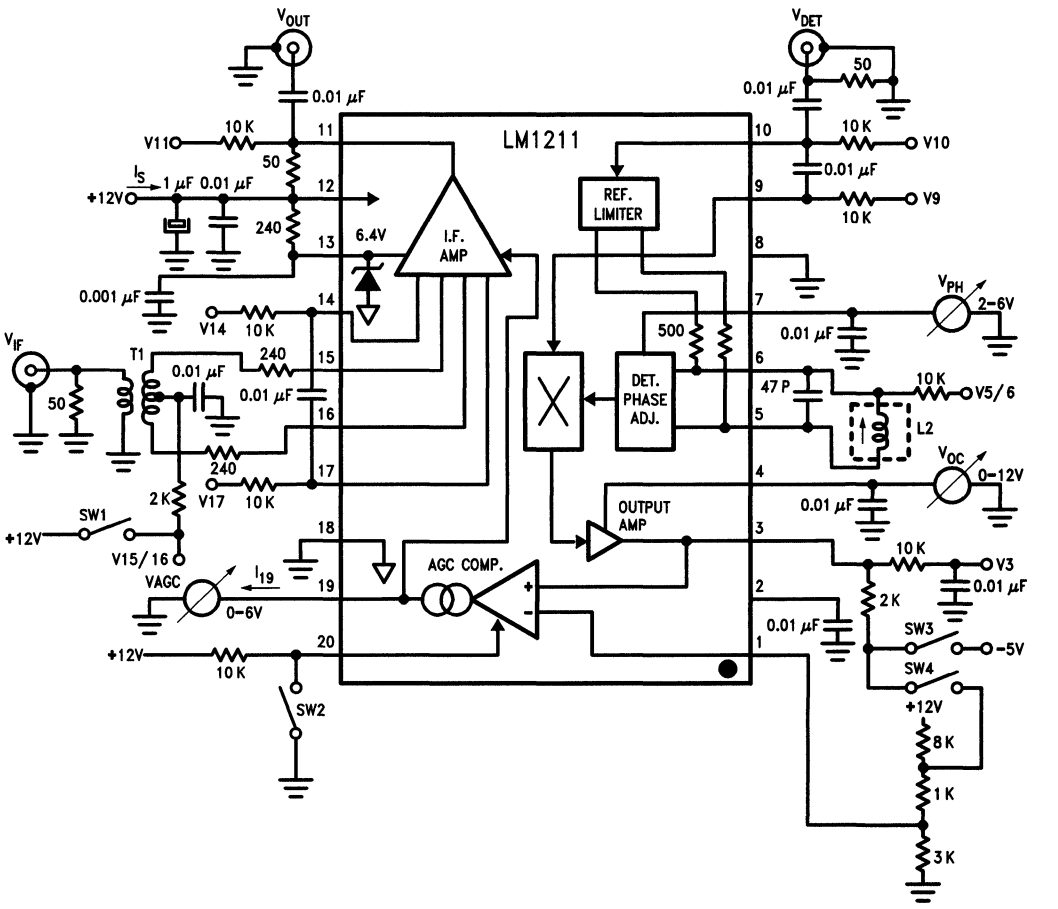
Note 1: Tested limits are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Note 3: The IF amplifier output is measured with the IF output connected to a 50Ω measurement system resulting in a 25Ω loaded impedance. The gain in an actual application will typically be 20 dB higher.

Test Circuit

Measure Parameters at Indicated Test Points



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T1 = 50Ω unbal. to bal. Mini-circuits Lab TM01T-1T

L2 = 4½ T #22 wire on 3/16" form with HF core, shielded

Typical Performance Characteristics

(All characteristics apply to the typical application circuit. Figure numbers are referenced in the applications information.)

FIGURE 1
IF Amplifier Gain Reduction Characteristic

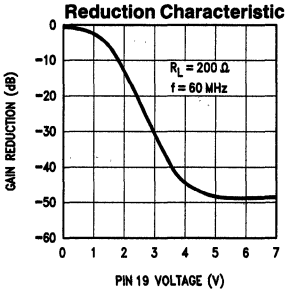


FIGURE 2
IF Amplifier Frequency Response

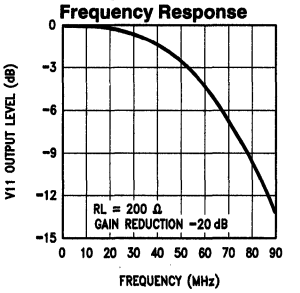


FIGURE 3
IF Amplifier Noise Figure vs. AGC

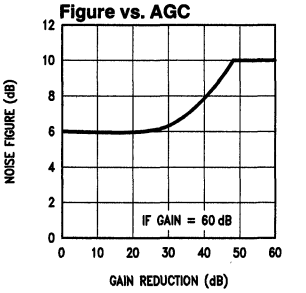


FIGURE 4
LM1211 Detection Phase

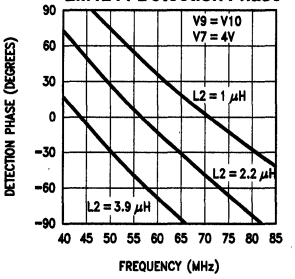


FIGURE 5
Detector Phase Adjust Characteristic

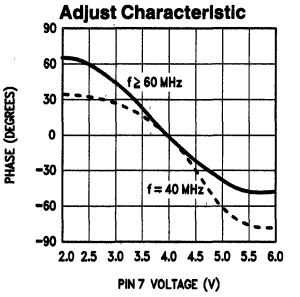
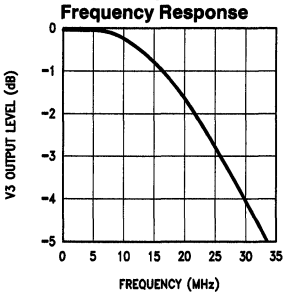


FIGURE 6
Output Amplifier Frequency Response



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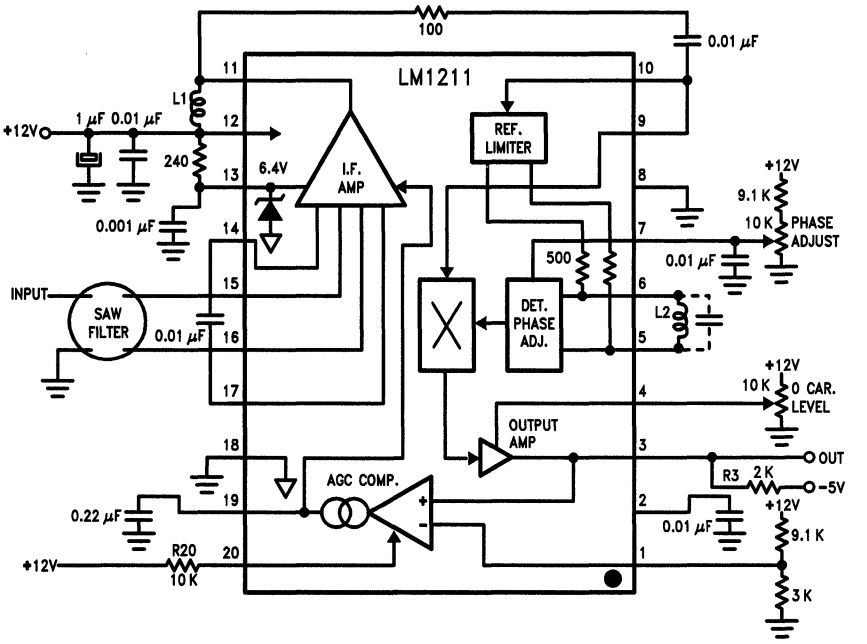
Typical Application Circuit



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Applications Information (Refer to Typical Performance Characteristics and Application Circuit.)

The LM1211 broadband demodulator system provides essentially independent IF amplifier and wideband detector blocks on the same integrated circuit. The IF amplifier consists of 5 differential stages, 3 of which have gain control capability. The detector is a highly flexible product detector with separate signal and reference input pins and a wideband output amplifier. An AGC comparator operating from the detector output is also provided. The operation of each of these blocks will now be described.

IF AMPLIFIER

The IF amplifier is powered from an internal shunt regulator between IF supply Pin 13 and IF ground Pin 18. The regulator has a nominal value of 6.5V and the IF amplifier current is delivered through a dropping resistor from the 12V rail supplying the remainder of the LM1211. The 0.001 μF ceramic RF decoupling capacitor at Pin 13 should be grounded through very short leads—preferably on the copper side of the PCB. A nominal current level into Pin 13 is 23 mA, set by a 240Ω resistor. This current should not exceed 40 mA and the minimum current is about 16 mA, below which the IF amplifier will start to lose gain as the Pin 13 voltage drops below the regulated level.

IF Amplifier Input Configuration

Circuit detail for the IF amplifier input Pins 14–17 is shown in *Figure 7.* The input stage is a common-base differential amplifier designed to give good rejection of unwanted IF output and detector reference signals that may be radiated back to the input.

The low differential input impedance of 60Ω ensures that SAW filters are terminated sufficiently to keep the triple transit echo (TTE) more than 40 dB below the signal level, even with low impedance SAW filters. Because it is a common base stage, the input stage gain is inversely proportional to the source impedance Zs presented to the input. A normal range for differential Zs is from 100Ω to 1 KΩ. As an example, a typical high impedance SAW filter has an output impedance that can be modeled as a 2 KΩ resistor in parallel with 6 pF capacitance, yielding Zs = 372Ω at 70 MHz. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained.

A balanced input is extremely important since the input leads to Pins 14–17 are the most sensitive points in the system to unwanted IF coupling. For example, if the IF output or detector reference signals couple into these pins it can cause changes in the frequency response and can easily promote oscillation. A spectrum analyzer is invaluable for helping determine the system susceptibility to this phenomenon. With the input terminated by the IF filter (or an equivalent resistor), the IF amplifier output noise spectrum will show if oscillation is likely to occur at maximum gain. A good layout will have symmetrical input leads placed as close together as possible, shielded input coils (where used), and external components mounted as close to the I.C. as possible. The DC feedback decoupling capacitor connected between Pins 14 and 17 should be right against the pins.

Gain Control Stages

The second through fourth differential stages of the IF amplifier are gain controlled by the voltage at the AGC Filter Pin 19. 0V corresponds to maximum IF gain, while increasing the Pin 19 voltage results in the gain reduction curve shown in *Figure 1.*

In most AM applications, the Pin 19 voltage will be under control of the AGC detector (to be described later) in a closed feedback loop. If Pin 20 of the AGC detector is grounded, Pin 19 is tri-stated, allowing it to be externally controlled. In the tri-stated condition the typical input bias current at Pin 19 is only 25 nA, allowing small filter capacitors to be used in gated AGC systems. The *Figure 1* characteristics has a temperature dependence of approximately −0.1 dB/°C. While this has no bearing in a closed loop system, it precludes setting a temperature stable fixed gain via a resistive divider at Pin 19.

For FM applications, the IF amplifier may be locked at maximum gain by grounding Pin 19. Under these conditions none of the 5 stages saturate when overdriven, allowing the amplifier to function as a basic wideband limiter.

IF Amplifier Output

The fifth and final IF amplifier stage has a single-ended output, with no internal connection to the detector block. The output Pin 11 is an open collector NPN transistor which must be returned to Pin 12 via a DC path. Pin 11 is also a point at which any additional signal filtering may be applied. A resistive load connected to Pin 12 can be used, but the maximum value is limited in practice to less than 500Ω at intermediate frequencies because of stray capacitance and the loading of the detector stage input impedance.

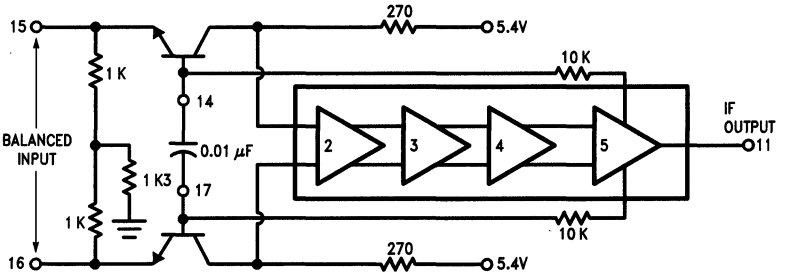

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FIGURE 7. Low Impedance Common Base Input Stage

Applications Information (Refer to Typical Performance Characteristics and Application Circuit.) (Continued)

The frequency response for the IF amplifier with a 200Ω load is shown in *Figure 2*. The high frequency rolloff gives rise to a potential problem called "tilt." This occurs in wide bandwidth signals when the upper frequency components are attenuated relative to the lower frequency components, which can cause amplitude distortion following demodulation. Tilt can be easily compensated at Pin 11 by using an inductive load to provide an increasing impedance with frequency. The impedance of inductive load L1, including the effects of stray capacitance, is given by:

$$|Z_L| = \frac{\omega L_1}{1 - \omega^2 L_1 C_S}$$

For example, a 0.33 μH coil with 8 pF stray capacitance at Pin 11 has an impedance of 300Ω at 70 MHz, and this impedance is on a frequency dependent slope of 0.4 dB/MHz. As the inductance is increased, the slope becomes steeper until resonance with the stray capacitance is reached. By using this technique, a flat IF response can be obtained over the frequency range of interest.

IF Amplifier Gain and Noise Figure

As described earlier, the maximum IF amplifier gain in the LM1211 is externally determined by the input source impedance, Zs, in conjunction with the output load impedance, Z_L. This gain is approximately given by:

$$A_V = \frac{(1000)|Z_L|}{|Z_S| + 60}$$

The IF amplifier noise figure (NF) as a function of gain reduction is shown in *Figure 3*. The contribution of IF NF to the overall system NF depends on the amount of gain ahead of the IF in the mixer and IF filter.

The SAW filter output mistermination, determined by the IF amplifier input impedance, is desirable from the viewpoint of keeping the TTE more than 40 dB below the signal. However, the mismatch at the input to the SAW filter is not so desirable as it simply increases the filter losses. Therefore a preferable solution is to use a low impedance SAW filter which will reduce losses, or to provide a pre-amplifier stage such as shown in *Figure 8* between the mixer and SAW filter. Since this stage can also be used to match the mixer output to the SAW filter input, the filter losses can be reduced.

To illustrate the effectiveness of this approach, a 10 dB gain pre-amp with a 4 dB NF will put the NF after the mixer stage at 23 dB, and the increase in NF with AGC action (by about 4 dB) will not contribute significantly to the system NF. A useful rule of thumb is that the total NF of the stages following the mixer should not exceed the mixer gain.

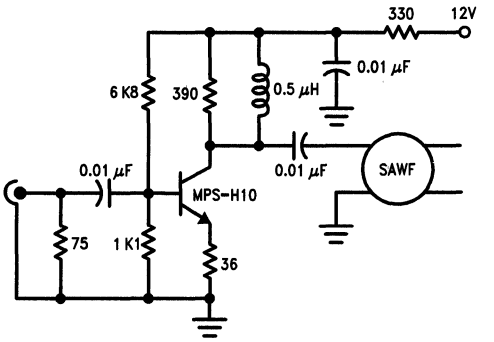

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FIGURE 8. SAW Filter Gain Stage

Detector

The detector section operates from a 12V supply between Pin 12 and ground Pin 8. The LM1211 uses a product detector comprised of a multiplier, reference limiter, detector phase adjuster, and wideband output amplifier (see block diagram). The demodulation process of multiplying the detector input by a limited version of the input is called quasi-synchronous detection. This process provides a wider reference bandwidth but reduced efficiency in carrier nulls relative to a true synchronous detector.

While the following description will apply to quasi-synchronous detection, the LM1211 can be made to function as a true synchronous detector if an external phase-locked loop (PLL) is used. In this mode, the reference limiter input Pin 10 is decoupled and the voltage-controlled oscillator (VCO) signal from the PLL is coupled into the reference port at Pins 5 and 6. Differential coupling of any external signal into the reference port is critical to minimize feedback to the IF amplifier inputs.

Multiplier

The heart of the product detector is the 6 transistor balanced multiplier shown in *Figure 9*. The detector input Vs(t) at Pin 9 is coupled to the linear differential pair, while the reference input Vr(t) switches the upper quad devices at the carrier rate.

If Vs(t) is an amplitude modulated carrier Fm(t)coswt and Vr(t) is a square wave of the same frequency w and relative phase ϕ, then the filtered output is given by:

$$V_{OUT} = \frac{2}{\pi}\frac{RL}{Re} Fm(t)\cos\phi$$

The output depends on the amplitude of Vs(t) and relative phase ϕ between Vs(t) and Vr(t). If ϕ is made 0 degrees so cosϕ is 1, then the multiplier acts as an amplitude detector and can be used to detect the amplitude modulation Fm(t) on the IF carrier. Note that around 0 degrees cos ϕ changes very little with phase. The multiplier can also be used as a

Detector (Continued)

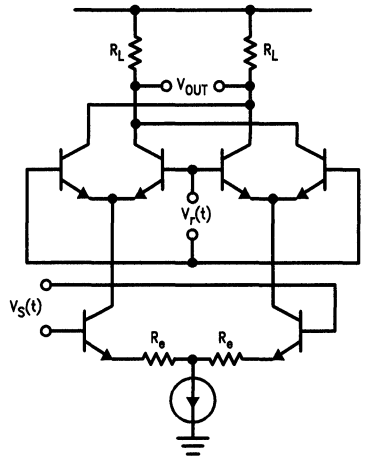

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FIGURE 9. Balanced Multiplier Circuit

phase or frequency detector if Vs(t) is limited to remove amplitude information and ϕ is centered at 90 degrees, where cosϕ produces the largest change in output for a given change in phase.

Thus a vital part of setting up the detector will be to obtain the correct relative phase for the type of demodulation desired.

Reference Limiter

The purpose of the reference limiter is to create the reference signal required for product detection by stripping AM modulation off the input signal. This should not be confused with the limiter required in an FM system, which is in the main signal path. FM limiting would be performed by locking the IF amplifier at maximum gain as previously described, in which case the reference limiter becomes redundant.

A single differential limiter stage is provided between Pin 10 and the reference port at Pins 5 and 6. Pin 10 is internally biased from a 5.1V source through a 3.3 KΩ resistor; the detector input Pin 9 is biased from the same source through 5 KΩ. By sharing a common bias point Pins 9 and 10 can be directly shorted together when fed from the same signal, thus saving a coupling capacitor. Alternatively, Pins 9 and 10 may be fed separately allowing phase and/or amplitude differences to be introduced.

The reference limiter output is a differential signal across the reference port Pins 5 and 6. Pins 5 and 6 are internally biased at 4.6V and have a 1 KΩ differential impedance. Limiting begins with 20 mVrms at Pin 10 and heavy limiting occurs above 100 mVrms input. The maximum limited output voltage is 350 mVrms.

Detector Phasing

As we have seen, the relative phase between the detector and reference inputs of the multiplier determines the LM1211 demodulation characteristic. The detector input phase is known since it connects directly to Pin 9. However, the reference phase depends on several factors: The external components at Pins 10, 5, and 6, the phase shift through the reference limiter, and lastly the setting of the detector phase adjust control at Pin 7. The general approach for phasing the detector is to first select the external components which produce the desired detection phase when the phase adjust control is in the center of its range (V7 = 4V), and then use the control to trim part-to-part and external component variations.

The curves of *Figure 4* give the multiplier detection phase versus frequency for different values of L2 with Pins 9 and 10 shorted together. These curves can be used to select the L2 value and to determine whether additional phase shift between Pins 9 and 10 is required. The detection phase versus temperature is approximately −0.25 degrees/°C.

A detection phase of ϕ = 0 degrees corresponds to maximum (+) amplitude detection efficiency, i.e. the detector output voltage increasing with Pin 9 input level. In the simplest case this can be obtained by choosing the L2 for which the *Figure 4* curve passes through 0 degrees at or near the IF frequency. When the proper phasing cannot be obtained by this means, phase lead or lag must be introduced at Pin 10 relative to Pin 9. A simple RC lead-lag network which can provide up to ±90 degrees phase shift is shown in *Figure 10.*

When XC1 = XC2 = 240Ω in the *Figure 10* circuit, approximately 90 degrees of phase difference between Pins 9 and 10 is produced with 3 dB additional attenuation. Pin 10 is shown lagging Pin 9, but the two pins could be reversed to produce phase lead. If C1 is increased or C2 is decreased, the phase difference is reduced.

A wideband FM quadrature detector is implemented in *Figure 11* by configuring the IF Amplifier for maximum gain and replacing L2 with an LC tank tuned to the IF frequency. Since the IF Amplifier performs the limiting function, the reference limiter is not used; rather, the quadrature signal is fed directly to the reference port via an RC phasing network. The DC offset at Pin 10 (13 KΩ to 12V) prevents signal leakage through the reference limiter to Pins 5 and 6.

The FM detector sensitivity depends on the phase slope of the LC tank, which is determined by the Q. For example, the tank in *Figure 11* is resonant around 70 MHz and has a Q ≅ 2 defined by the internal 1 KΩ resistance across Pins 5 and 6 in parallel with the external resistor. Deviating the input frequency produces an output characteristic given by:

$$V3 = V_{pk}[\cos(90 \pm \Delta 0)]$$

where V_{pk} is the theoretical peak output level set by the IF Pin 11 load impedance, and Δ0 is the combined phase swing produced by the tank and detector. For the *Figure 11* circuit, V_{pk} = 6V and Δ 0 ≅ 5 degrees/MHz, yielding an output swing of ±0.5 V/MHz.

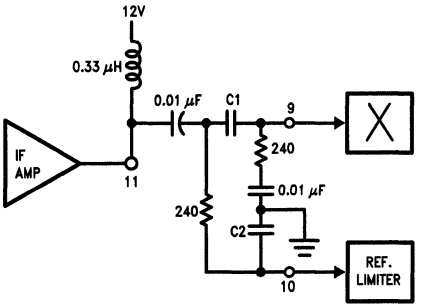

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FIGURE 10. Detector Input Phasing Network

Detector (Continued)

Phase Adjust Control

Once the external components have been selected for the correct nominal phasing, the detector phase adjust is used to perform the final set-up by monitoring the detector output either for maximum output in the case of AM detection or for 0V average level for FM detection. The phase adjust control Pin 7 is externally biased via a potentiometer and resistor from 12V and requires a 2V to 6V minimum range at Pin 7. The amount of phase lead or lag added to the reference path as a function of V_7 is given in *Figure 5.* For example, at 70 MHz a cumulative phase error of ±50 degrees could be compensated for by the phase adjust control.

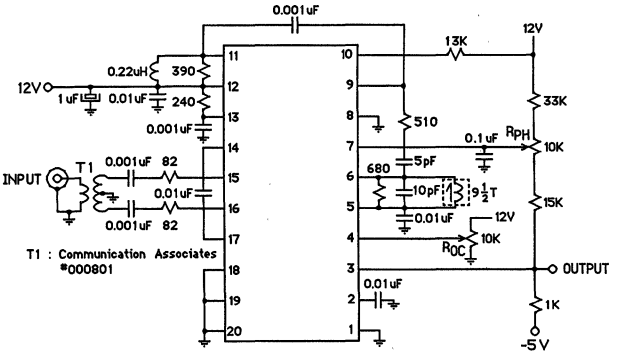
While the previously cited −0.25 degrees/°C detection phase temperature dependence is not noticeable in AM detection applications, it can cause the average DC level of the FM detector output to drift. This can be reduced by using the phase adjust control in a feedback loop as shown in *Figure 11.* Finally, it should be re-emphasized that the Pin 7 adjustment is intended as a trim rather than a substitute for correct detector phasing.

Detector Output

The LM1211 output amplifier has an NPN emitter follower driving Pin 3 through a 50Ω damping resistor as shown in *Figure 12.* The nominal 0 carrier (no input signal) output voltage is 0V, and a negative supply is required as a return point for the external load resistor R3. The output may be biased at up to 5 mA in order to maintain the (−) slew rate into capacitive loads.

The 0 carrier output voltage is adjusted by the control voltage on a potentiometer at Pin 4. The center of the Pin 4 range is ½ supply with an adjustment sensitivity of approximately 0.1 V/V. Thus on a 12V supply up to ±0.6V part-to-part output variation can be trimmed out. The Pin 3 output is capable of swinging up to ±4V; however, in certain AM detector applications the output will always remain above 0V. In these cases it may be possible to omit the negative supply and return the Pin 3 load resistor directly to ground. This will result in some degradation in linearity at low output voltages which can be minimized by pre-biasing the 0 carrier level high (V4 = 12V).

The output amplifier frequency response is shown in *Figure 6.* The output exhibits a linear phase response of approximately −5.5 degrees/MHz out to 30 MHz. The first 70 MHz carrier harmonic is approximately −46 dB and the second harmonic −40 dB referenced to a 3V peak output.



ALIGNMENT SEQUENCE:

1. With no input, adjust R_{OC} for V3 = 0V.
2. Apply $V_{in} \geq 10$ mVrms, Fo = 70 MHz ±5 MHz Dev, Fm = 100 kHz; Tune Quadrature coil for best output linearity.
3. Adjust R_{PH} for output DC centering.

FIGURE 11. 70 MHz FM Detector Application

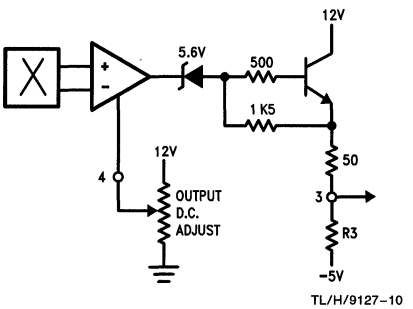


FIGURE 12. Detector Output Amplifier

Detector (Continued)

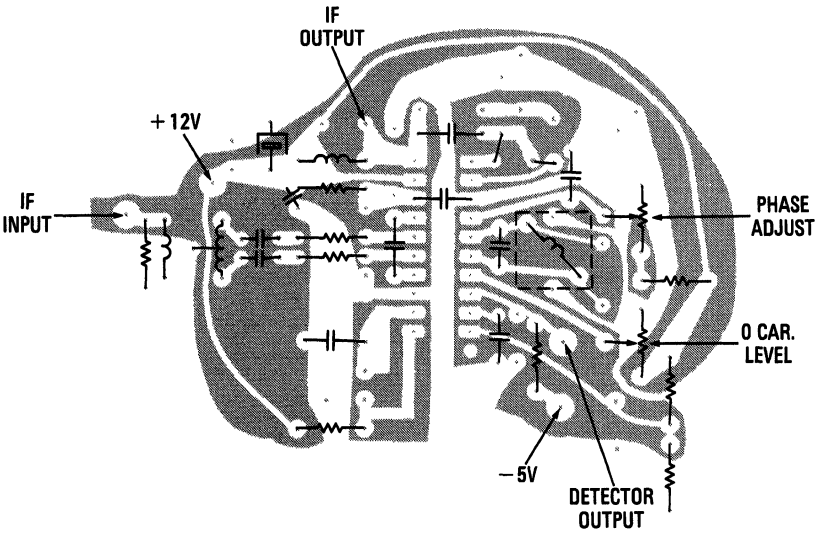
AGC Comparator

An AGC comparator is provided for use in AM systems. The (+) input is internally connected to the detector output Pin 3 while the (−) input is biased from an external resistive divider at AGC threshold Pin 1. An output current charges and discharges the AGC filter capacitor at Pin 19 to control the IF amplifier gain. The comparator is biased by a current into bias/gate Pin 20. Internally, Pin 20 has a diode in series with 1 KΩ to ground so that the current level from an external resistor R20 to 12V is given by:

$$I20 = \frac{11.3}{R20 + 1000}$$

Whenever the detector output exceeds the AGC threshold, a current equal to the Pin 20 bias current is delivered to Pin 19 to charge the AGC filter capacitor. When the detector output is below the AGC threshold, approximately 11 μA discharge current flows into Pin 19. Thus the charge to discharge current ratio at Pin 19 is given by I20/11 μA, or 90:1 for I20 = 1 mA. This large ratio creates a peak-detecting action in which the AGC loop holds the detector (+) output peaks at the AGC threshold voltage, typically 1-3V. Because of the large ratio of charge to discharge current, the LM1211 AGC has inherently faster recovery from a step increase in signal than from a decrease. The overall speed is inversely proportional to the AGC filter capacitor, with 0.05 μF being a practical lower limit for I20 = 1 mA. It is important to use a quality (low Rs) capacitor at Pin 19 to prevent AGC oscillation.

The AGC detector can be used at lower charge/discharge ratios by reducing I20 which has a direct effect on the charge current but only a second order effect on the discharge current. For I20 = 100 μA a 15:1 ratio is produced and a 0.01 μF minimum capacitor can be used. As the charge/discharge ratio is reduced, peak detection no longer occurs and gating of Pin 20 may be necessary. This requires an external gate pulse generator to turn on the Pin 20 bias current only during the time the detector output is to be sampled. In between gate pulses the Pin 19 output will be tri-stated and the filter capacitor will hold the previous voltage until the next gate pulse. Permanently grounding Pin 20 turns off the AGC comparator, allowing an external AGC signal at Pin 19 to control the IF amplifier gain.



TL/H/9127–11

Printed Circuit Layout (component side)

National Semiconductor

LM1596/LM1496 Balanced Modulator-Demodulator

General Description

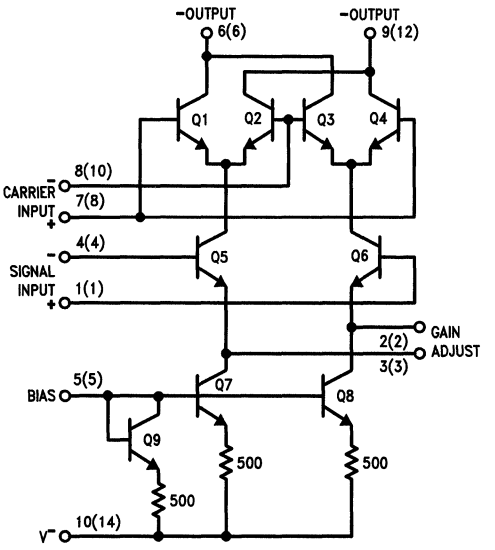
The LM1596/LM1496 are doubled balanced modulator-demodulators which produce an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection, broadband frequency doubling and chopping.

The LM1596 is specified for operation over the −55°C to +125°C military temperature range. The LM1496 is specified for operation over the 0°C to +70°C temperature range.

Features

- Excellent carrier suppression
  - 65 dB typical at 0.5 MHz
  - 50 dB typical at 10 MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- Low offset and drift
- Wide frequency response up to 100 MHz

Schematic and Connection Diagrams



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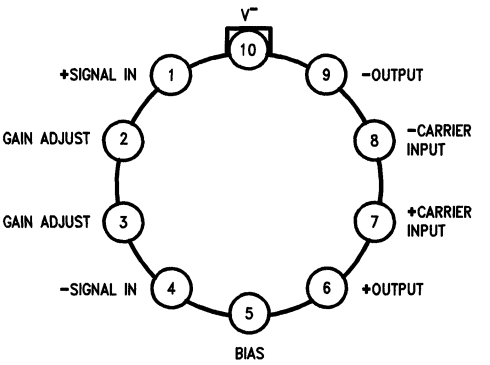
Numbers in parentheses show DIP connections.

Metal Can Package



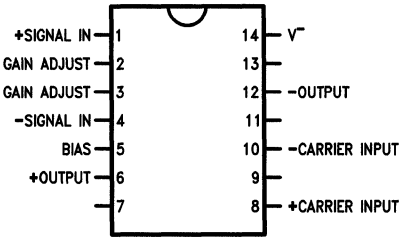
TL/H/7887–2

Top View

Note: Pin 10 is connected electrically to the case through the device substrate.

Order Number LM1496H or LM1596H
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/7887–3

Order Number LM1496M or LM1496N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$\pm(5 + I_5R_0)$V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	12 mA
Operating Temperature Range LM1596	−55°C to +125°C
LM1496	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and their effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit)

Parameter	Conditions	LM1596			LM1496			Units
		Min	Typ	Max	Min	Typ	Max	
Carrier Feedthrough	V_C = 60 mVrms sine wave f_C = 1.0 kHz, offset adjusted		40			40		μVrms
	V_C = 60 mVrms sine wave f_C = 10 kHz, offset adjusted		140			140		μVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2		0.04	0.2	mVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, not offset adjusted		20	100		20	150	mVrms
Carrier Suppression	f_S = 10 kHz, 300 mVrms f_C = 500 kHz, 60 mVrms sine wave offset adjusted	50	65		50	65		dB
	f_S = 10 kHz, 300 mVrms f_C = 10 MHz, 60 mVrms sine wave offset adjusted		50			50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mVrms sine wave		300			300		MHz
	f_S = 1.0 kHz, 300 mVrms sine wave Signal Input Port, V_S = 300 mVrms sine wave $V_7 - V_8$ = 0.5Vdc		80			80		MHz
Voltage Gain, Signal Channel	V_S = 100 mVrms, f = 1.0 kHz $V_7 - V_8$ = 0.5 Vdc	2.5	3.5		2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		200			200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		2.0			2.0		pF
Single Ended Output Resistance	f = 10 MHz		40			40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0			5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25		12	30	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0		5.0	5.0	μA
Average Temperature Coefficient of Input Offset Current	(−55°C < T_A < +125°C) (0°C < T_A < +70°C)		2.0			2.0		nA/°C nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50		14	60	μA
Average Temperature Coefficient of Output Offset Current	(−55°C < T_A < +125°C) (0°C < T_A < +70°C)		90			90		nA/°C nA/°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit) (Continued)

Parameter	Conditions	LM1596			LM1496			Units
		Min	Typ	Max	Min	Typ	Max	
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0			5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 Vdc		−85			−85		dB
Common Mode Quiescent Output Voltage			8.0			8.0		Vdc
Differential Output Swing Capability			8.0			8.0		V_{p-p}
Positive Supply Current	(I_6 + I_8)		2.0	3.0		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0		3.0	4.0	mA
Power Dissipation			33			33		mW

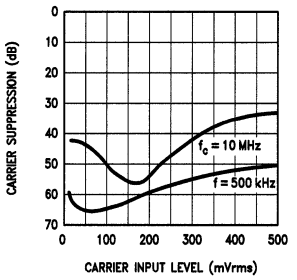
Note 1: LM1596 rating applies to case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperature above 75°C. LM1496 rating applies to case temperatures to +70°C.

Note 2: Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

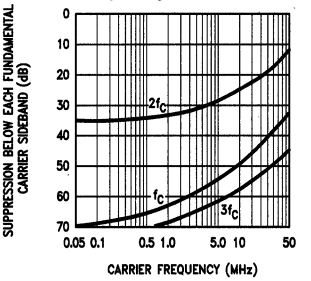
Note 3: Refer to rets1596x drawing for specifications of military LM1596H versions.

Typical Performance Characteristics

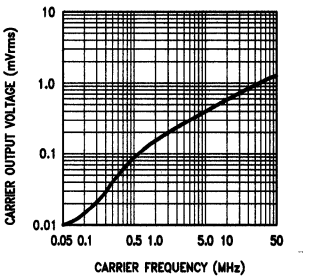
Carrier Suppression vs Carrier Input Level



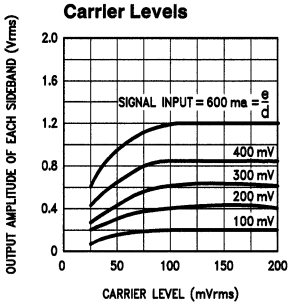
Carrier Suppression vs Frequency



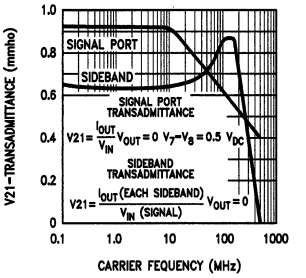
Carrier Feedthrough vs Frequency



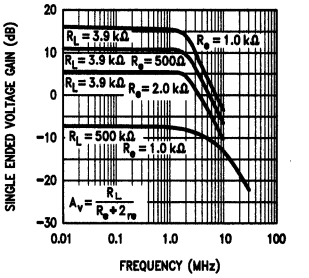
Sideband Output vs Carrier Levels



Sideband and Signal Port Transadmittances vs Frequency



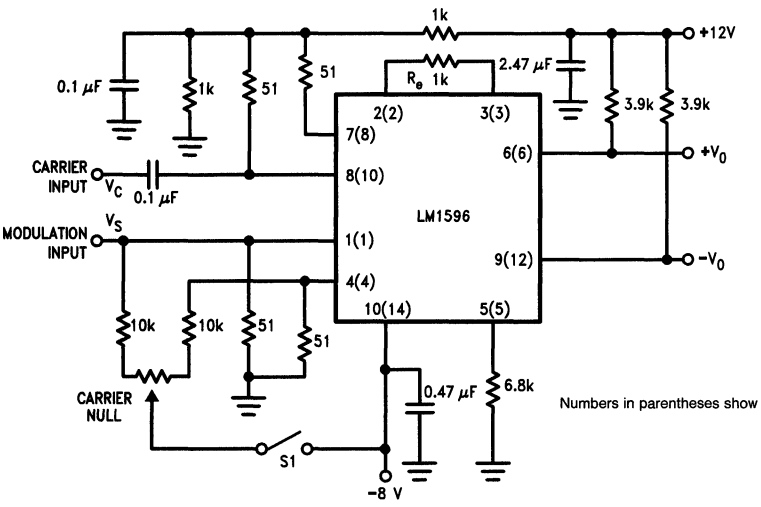
Signal-Port Frequency Response



TL/H/7887–5

Typical Application and Test Circuit

Suppressed Carrier Modulator

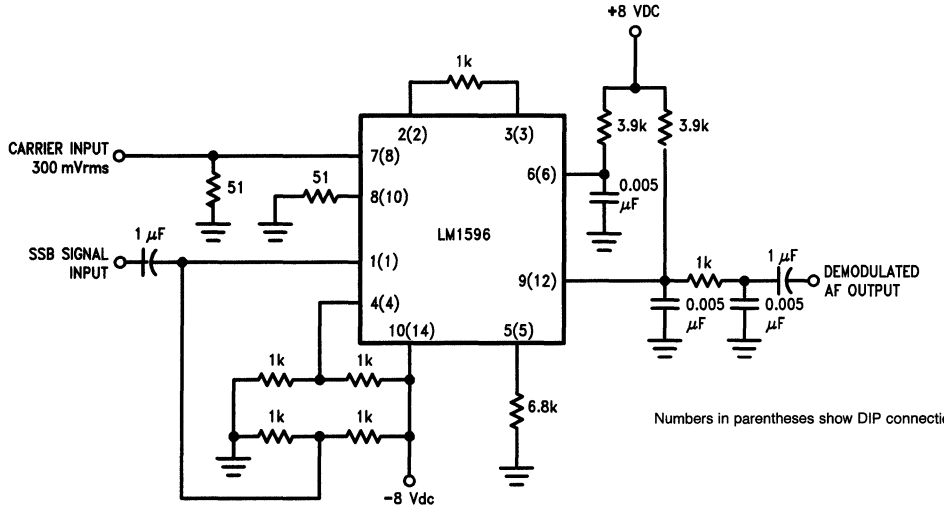


Numbers in parentheses show DIP connections.

Note: S_1 is closed for "adjusted" measurements.

TL/H/7887–4

SSB Product Detector



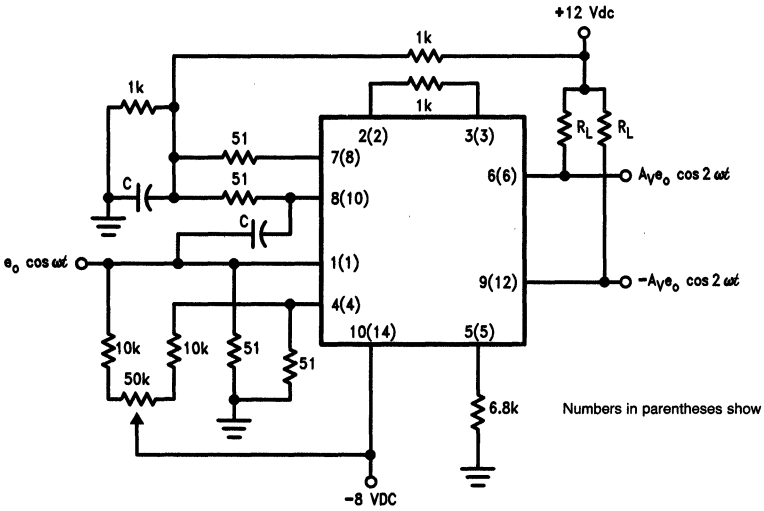
Numbers in parentheses show DIP connections.

TL/H/7887–6

This figure shows the LM1596 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mVrms is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mVrms. All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Typical Applications (Continued)

Broadband Frequency Doubler



Numbers in parentheses show DIP connections.

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The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

National Semiconductor

LM1865 Advanced FM IF System

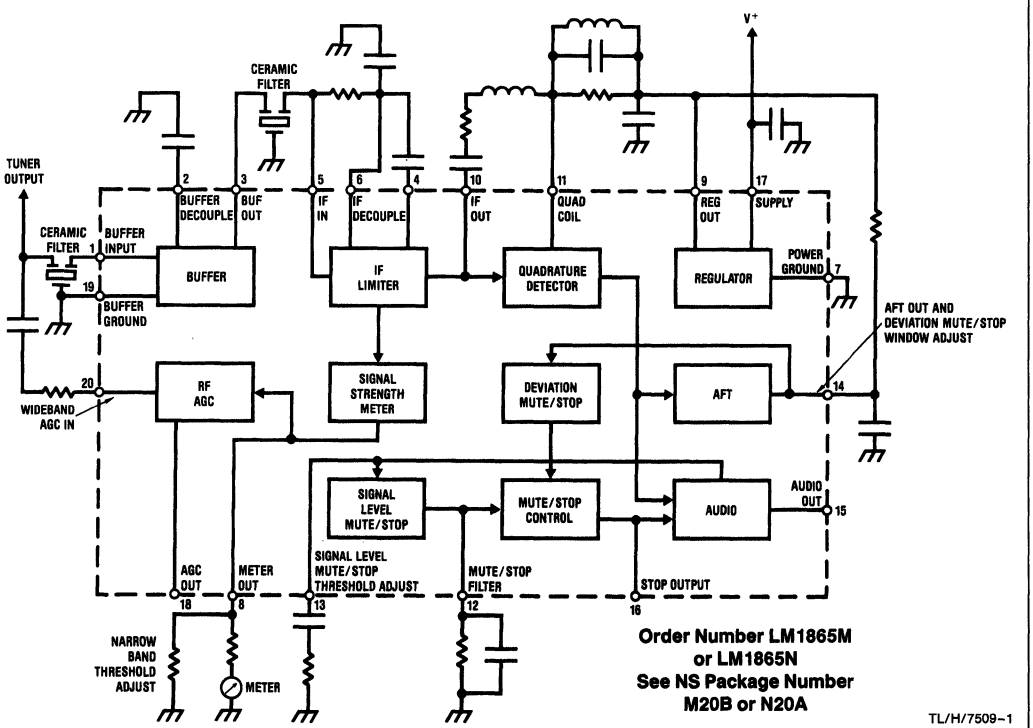
General Description

Reduced external component cost, improved performance, and additonal functions are key features to the LM1865 FM IF system. The LM1865 is designed for use in electronically tuned radio applications. It contains both deviation and signal level stop circuitry in addition to an open-collector stop output. The LM1865 generates a reverse AGC voltage (ie: decreasing AGC voltage with increasing signal).

Features

- On-chip buffer to provide gain and terminate two ceramic filters
- Low distortion 0.1% typical with a single tuned quadrature coil for 100% modulation.
- Broad off frequency distortion characteristic
- Low THD at minimum AFT offset
- Meter output proportional to signal level
- Stop detector with open-collector output
- Adjustable signal level mute/stop threshold, controlled either by ultrasonic noise in the recovered audio or by the meter output
- Adjustable deviation mute/stop threshold
- Separate time constants for signal level and deviation mute/stop
- Dual threshold AGC eliminates need for local/distance switch and offers improved immunity from third order intermodulation products due to tuner overload
- User control of both AGC thresholds
- Excellent signal to noise ratio, AM rejection and system limiting sensitivity

Block Diagram



Order Number LM1865M or LM1865N
See NS Package Number M20B or N20A

TL/H/7509–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, Pin 17	16V
Package Dissipation (Note 1)	2.0W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−20°C to +85°C
Max Voltage on Pin 16 (Stop Output)	16V

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V^+ = 12V; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise

Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS					
Supply Current			33	45	mA
Pin 9, Regulator Voltage			5.7		V
Operating Voltage Range	(See Note 2)	7.3		16	V
Pin 18, Output Leakage Current	Pin 20 Open, V_{IF} = 0, S3 in Position 1		0.1		μA
Pin 16, Stop Low Output Voltage	S1 in Position 1, S2 in Position 3		0.3		V
Pin 16, Stop High Output Leakage Current	S2 in Position 2, V14 = V9		0.1		μA
Pin 15, Audio Output Resistance			4.7		kΩ
Pin 1, Buffer Input Resistance	Measured at DC		350		Ω
Pin 3, Buffer Output Resistance	Measured at DC		350		Ω
Pin 20, Wide Band Input Resistance	Measured at DC		2		Ω
Pin 8, Meter Output Resistance			1		kΩ
DYNAMIC CHARACTERISTICS f_{MOD} = 400 Hz, f_o = 10.7 MHz, Deviation = ±75 kHz					
−3 dB Limiting Sensitivity	IF Only (See Note 3)		60	120	μVrms
Buffer Voltage Gain	V_{IN} Pin 1 = 10 mVrms at 10.7 MHz	19	22	25	dB
Recovered Audio	V_{IF} = 10 mVrms, V14 = V9	275	320	470	mVrms
Signal-to-Noise	V_{IF} = 10 mVrms, V14 = V9 (See Note 4)	70	84		dB
AM Rejection	V14 = V9 V_{IF} = 1 mV, 30% AM Mod V_{IF} = 10 mV, 30% AM Mod	 50 50	 60 60		 dB dB
Minimum Total Harmonic Distortion	V_{IF} = 10 mV		0.1	0.35	%
THD at Frequency where V14 = V9 (Zero AFT Offset)	V_{IF} = 10 mV, Tune until V14 = V9		0.1	0.45	%
THD ± 10 kHz from Frequency where V14 = V9	V_{IF} = 10 mV		0.15		%
AFT Offset Frequency for Low Stop Output at Pin 16	V_{IF} = 10 mV, S2 in Position 3, f_{MOD} = 0 Offset = (Frequency for Pin 16 Low) − (Frequency where V14 = V9)		±50		kHz
Ultrasonic Mute/Stop Level Threshold	V14 = V9, S1 in Position 3 (See Note 5) V_{IF} = 10 mV f_{MOD} = 100 kHz S2 in Position 3 Amount of Deviation where V16 → Low		60		kHz

Electrical Characteristics Test Circuit, T_A = 25°C, V^+ = 12V; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise (Continued)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC CHARACTERISTICS f_{MOD} = 400 Hz, f_o = 10.7 MHz, Deviation = ±75 kHz (Continued)					
Pin 13 Mute/Stop Threshold Voltage	V14 = V9, S1 in Position 4 S2 in Position 3 V13 where V16 → Low		220		mV
Amount of Muting (LM1965 Only)	S2 in Position 4, S1 in Position 1, V_{IF} = 10 mV		66		dB
Amount of Muting with Pin 13 and Pin 16 Grounded	S1 in Position 1 V14, = V9, V_{IF} = 10 mV		0		dB
Narrow Band AGC Threshold	Increase IF Input until I_{AGC} = 0.1 mA Pin 20 = 30 mVrms	100	210	300	μVrms
Wide Band AGC Threshold	V_{IF} = 100 mVrms Increase Signal to Pin 20 until I_{AGC} = 0.1 mA	5	12	22	mVrms
Pin 18, Low Output Voltage (LM1865 and LM1965 only)	V_{IN} Pin 20 = 100 mV, V_{IF} = 100 mVrms		0.2	0.5	V
Pin 18, High Output Voltage (LM2065 only)	V_{IN} Pin 20 = 100 mV, V_{IF} = 100 mVrms, (See Note 6)		11.7		V
Pin 8, Meter Output Voltage	V_{IF} = 10 μV V_{IF} = 300 μV V_{IF} = 3 mV		0.1 1.1 2.6		V V V

Note 1: Above T_A = 25°C derate based on $T_{J(max)}$ = 150°C and θ_{JA} = 60°C/W.

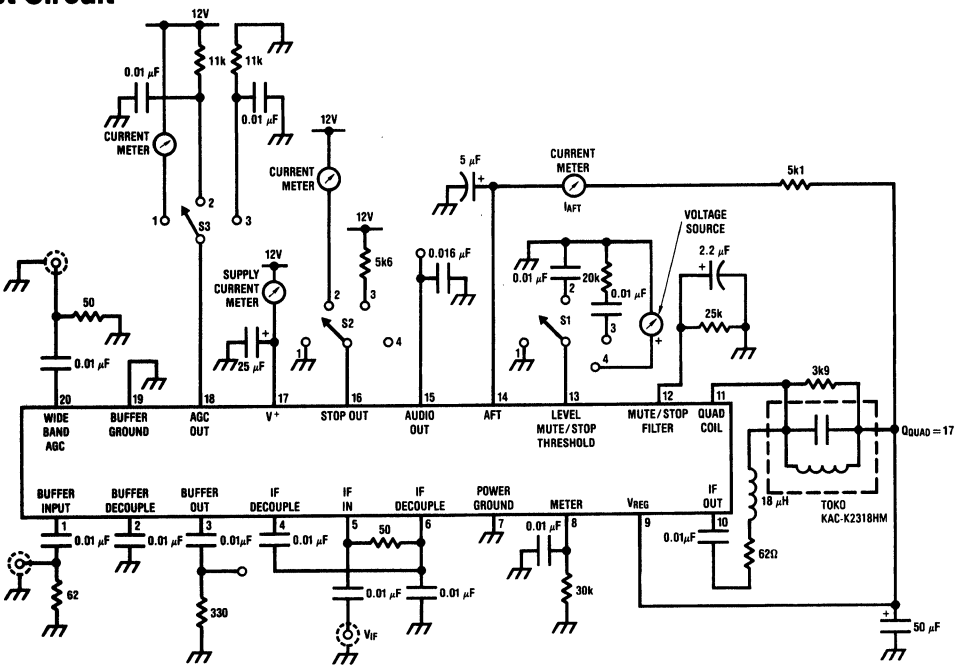
Note 2: All data sheet specifications are for V^+ = 12V may change slightly with supply.

Note 3: When the IF is preceded by 22 dB gain in the buffer, excellent system sensitivity is achieved.

Note 4: Measured with a notch at 60 Hz and 20 Hz to 100 kHz bandwidth.

Note 5: FM modulate RF source with a 100 kHz audio signal and find what modulation level, expressed as kHz deviation, results in V16 → 12V.

Test Circuit

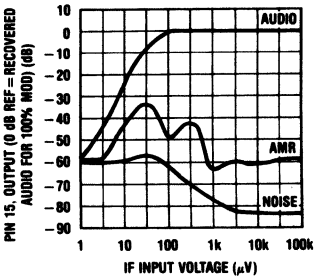


TL/H/7509–2

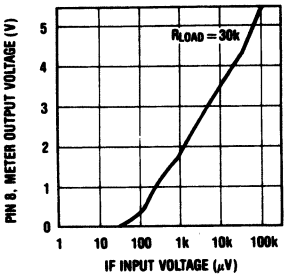
FIGURE 2

Typical Performance Characteristics (from Test Circuit)

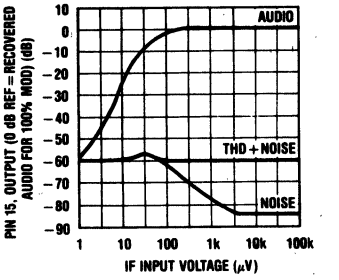
FM Limiting Characteristics and AM Rejection



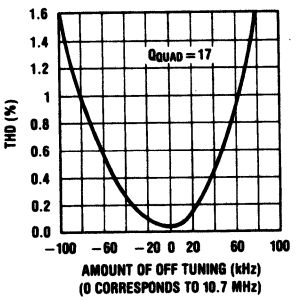
Pin 8, Meter Output Voltage vs IF Input Level



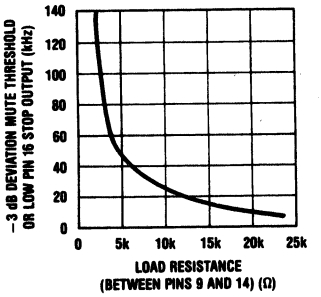
FM Limiting Characteristics + THD



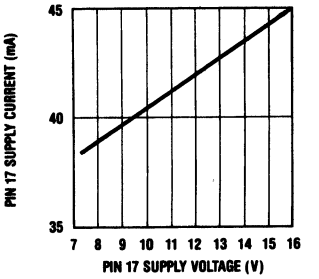
% THD vs OFF Tuning (Single Tuned Quadrature Coil)



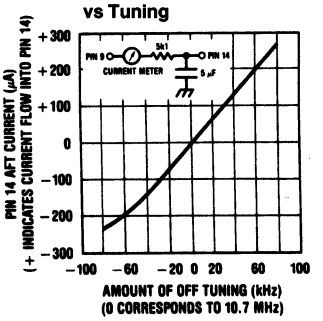
Deviation Mute/Stop Threshold as a Function of AFT Load Resistor



Supply Current vs Supply Voltage



Pin 14, AFT Current vs Tuning



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Coils and ceramic filters are available from:

Toko America	Murata
1250 Feehanville Drive	2200 Lake Park Drive
Mount Prospect, IL 60056	Smyrna, GA 30080
(312) 297-0070	(404) 436-1300

Application Circuit

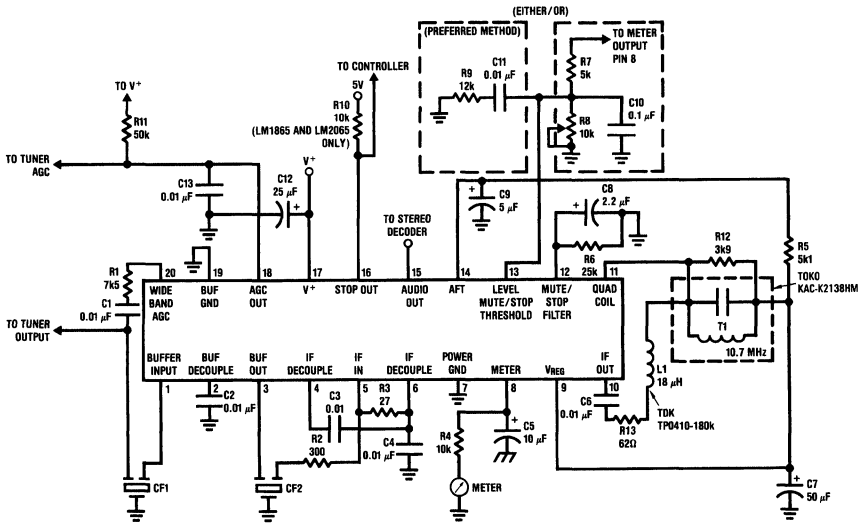

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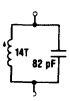
FIGURE 3

IC External Components (See Application Circuit)

Component	Typical Value	Comments
C1	0.01 µF	AC coupling for wide band AGC input
C2	0.01 µF	Buffer and AGC supply decoupling
C3, C4	0.01 µF	IF decoupling capacitors
C5	10 µF	Meter decoupling capacitor
C6	0.01 µF	AC coupling for IF output
C7	50 µF	Regulator decoupling capacitor, affects S/N floor
C8	2.2 µF	Level mute/stop time constant
C9	5 µF	AFT decoupling, affects stop time
C10	0.1 µF	Disables noise mute/stop
C11	0.01 µF	AC coupling for noise mute/stop threshold adjust
C12	25 µF	Supply decoupling
C13	0.01 µF	AGC output decoupling capacitor
R1	Tuner Dependent	Wide band AGC threshold adjust
R2, R3	Tuner Dependent	Gain set and bias for IF; R2 + R3 = 330Ω to terminate ceramic filter
R4	Meter Dependent	Sets full-scale on meter
R5	5k1	Deviation mute/stop window adjustment
R6	25k	Mute/stop filter, affects stop time
R7	5k	Level mute/stop threshold adjustment
R8	10k Pot	Level mute/stop threshold adjustment
R9	12k	Noise mute/stop threshold adjustment, decrease resistor for lower S/N at threshold, for optimum performance over temp. and gain variation, set this resistor value so that the signal level mute/stop threshold occurs in the radio at 45dB S/N (±3 dB) in mono.
R10	10k	Load for open-collector stop output
R11	50k	AGC output load resistor for open-collector output
R12	3k9	Sets Q of quadrature coil affecting THD, S/N and recovered audio
R13	62Ω	Optimises minimum THD
L1	18 µH Q_u>50 @ 10.7 MHz TDK Electronics TPO410-180K or equivalent	Sets signal swing across quadrature coil, High Q is important to minimize effect variation of Q has on both minimum THD and AFT offset.
T1	 Q_u>70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz TOKO KAC-K2318HM or equivalent	10.7 MHz quadrature coil: Q_{UL} > 70
CF1, CF2	Murata SFE10.7ML or equivalent	10.7 MHz ceramic resonators provide selectivity; good group delay characteristics important for low THD of system

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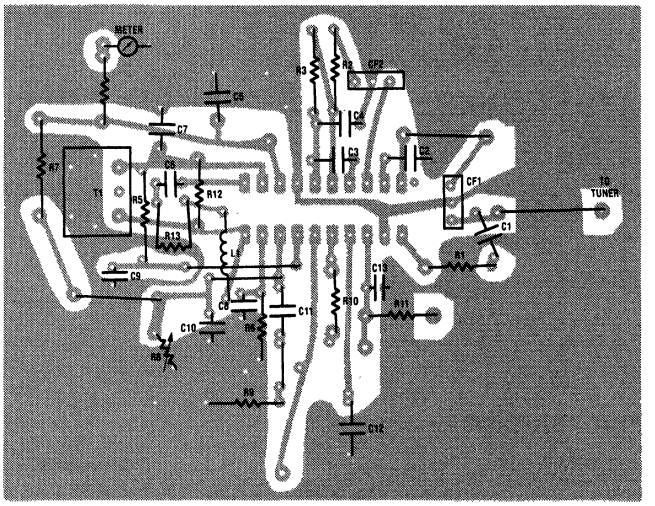
Typical Application

LAYOUT CONSIDERATIONS

Although the pinout of the LM1865 has been chosen to minimize layout problems, some care is required to insure stability. The ground terminal on CF1 should return to both the input signal ground and the buffer ground, pin 19. The ground terminal on CF2 should return to the ground side of C4. The quadrature coil T1 and inductor L1 should be separated from the input circuitry as far as possible.

PC Layout (Component Side)



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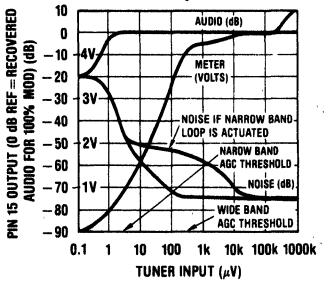
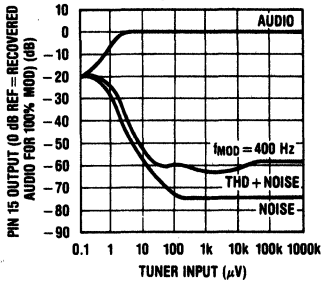
PERFORMANCE CHARACTERISTICS OF TYPICAL APPLICATION WITH TUNER

The following data was taken using the typical application circuit in conjunction with an FM tuner with 43 dB of gain, a 5.5 dB noise figure, and 30 dB of AGC range. The tuner was driven from a 50Ω source. 75 μs of de-emphasis was used on the audio output, pin 15. The 0 dB reference is for ±75 kHz deviation at 400 Hz modulation.

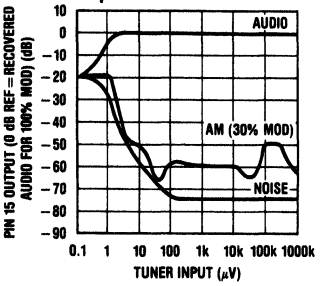
Meter Output and Signal-to-Noise vs Tuner Input



Total Harmonic Distortion vs Tuner Input



AM Rejection vs Tuner Input



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−3 dB limiting = 0.9 μV

30 dB quieting = 1.4 μV

Level stop/mute threshold = 1.4 μV

Deviation mute window (−3 dB) = ±45 kHz

Application Notes

ADJUSTABLE MUTE/STOP THRESHOLD

The threshold adjustments for the mute and stop functions are controlled by the same pins. Thus, the term mute/stop will be used to designate either function.

The adjustable mute/stop threshold in the LM1865 allows for user programming of the signal level at which muting or stop indication takes place. The adjustment can be made in two mutually exclusive ways. The first way is to take a voltage divider from the meter output (pin 8) to the off channel mute input (pin 13). When the voltage at pin 13 falls below 0.22V, an internal comparator is tripped causing muted or causing the stop output to go low. Adjustment of the voltage divider ratio changes the signal level at which this happens.

The second method of mute/stop detection as a function of signal level is to use the presence of ultrasonic noise in the recovered audio to trip the internal comparator. As the signal level at the antenna of the radio drops, the amount of noise in the recovered audio, both audible and ultrasonic, increases.

The recovered audio is internally coupled through a high pass filter to pin 13 which is internally biased above the comparator trip point. Large negative-going noise spikes will drive pin 13 below the comparator trip point and cause mute/stop action. A simplified circuit is shown in *Figure 4*.

Since the input to the comparator is noise, the output of the comparator is noise. Consequently, a mute/stop filter on pin 12 is required to convert output noise spikes to an average DC value. This filter is not necessary if pin 13 is driven from the meter.

Adjustment of the mute/stop threshold in the noise mode is accomplished by adjusting the pole of the high pass filter coupled to the comparator input. This is done with a series capacitor/resistor combination, R9 C11, from pin 13 to ground. As the pole is moved higher in frequency (i.e., R9 gets smaller) more ultrasonic noise is required in the recovered audio in order to initiate mute/stop action. This corresponds to a weaker signal at the antenna of the radio. In choosing the correct value for R9 it is important to make sure that recovered audio below 75 kHz is not sufficient to cause mute/stop action. This is because stereo and SCA information are contained in the audio signal up to 75 kHz. Also note that the ultrasonic mute/stop circuit will not operate properly unless a tuner is connected to the IF. This is because, at low signal levels, the noise at the tuner output dominates any noise sources in the IC. Consequently, driving the IC directly with a 50Ω generator is much less noisy than driving the IC with a tuner and therefore not realistic. The RC filter on pin 12 not only filters out noise from the comparator output but controls the "feel" when manually tuning. For example, a very long time constant will cause the mute to remain active if you rapidly tune through valid strong stations and will only release the mute if you slowly tune to a valid station. Conversely, a short time constant will allow the mute to kick in and out as one tunes rapidly through valid stations.

The advantage in using the noise mute/stop approach versus the meter driven approach is that the point at which mute/stop action occurs is directly related to the signal-to-noise ratio in the recovered audio. Furthermore, the mute/stop threshold is not subject to production and temperature variations in the meter output voltage at low signal levels, and thus might be able to be set without a production adjustment of the radio. The noise mute/stop threshold is very insensitive to temperature and gain variations. Proper operation of this circuit requires that the signal level mute/stop threshold be set at a signal level that achieves 45 dB S/N (±3 dB) in mono. in a radio. In an electronically tuned radio, the signal level stop threshold can be set to a much larger level by gain reducing the tuner (ie. pulling the AGC line) in scan mode and then releasing the AGC once the radio stops on a station. In an environment where temperature variations are minimal and manual adjustment of the signal level mute/stop threshold is desired, then the meter driven approach is the best alternative.

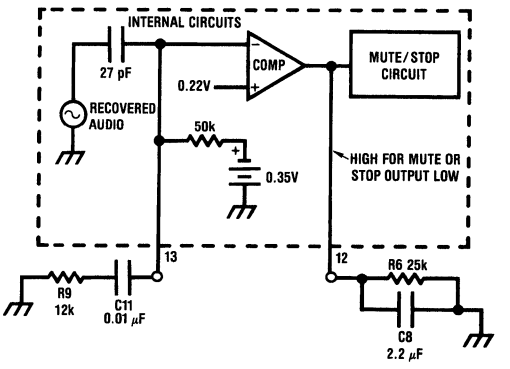

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FIGURE 4. Simplified Level Mute/Stop Circuit

Application Notes (Continued)

STOP TIME

An electronically tuned radio (ETR) pauses at fixed intervals across the FM band and awaits the stop indication from the LM1865. If within a predetermined period of time, no stop indication is forthcoming, the controller circuit concludes that there is no valid station at that frequency and will tune to the next interval. There are several time constants that can affect the amount of time it takes the LM1865 to output a valid stop indication on pin 16. In this section each time constant will be discussed.

Deviation Stop Time Constant

An offset voltage is generated by the AFT if the LM1865 is tuned to either side of a station. Since deviation stop detection in the LM1865 is detected by the voltage at pin 14, it is important that this voltage move fast enough to make the deviation stop decision within the time allowed by the controller. The speed at which the voltage at pin 14 moves is governed by the RC time constant, R5 C9. This time constant must be chosen long enough to remove recovered audio from pin 14 and short enough to allow for reasonable stop detection time.

Signal Level Stop Using Ultrasonic Noise Detection

As previously mentioned, the R6 C8 time constant on pin 12 is necessary to filter the noise spikes on the output of the internal comparator in the LM1865. This time constant also determines the level stop time. When the voltage at pin 12 is above a threshold voltage of about 0.6V, the stop output is low. The maximum voltage at pin 12 is about 0.8V. The level stop time is dominated by the amount of time it takes the voltage at pin 12 to fall from 0.8V to 0.6V. The voltage at pin 12 follows an exponential decay with RC time constant given by R6 C8. For example if R6 = 25k and C8 = 2.2 μF the stop time is given by

$$t = -(24k)\,(2.2\ \mu F)\ \ell n \left(\frac{0.6}{0.8}\right)$$

which yields t = 15 ms. It should be noted that the 0.6V threshold at pin 12 has a high temperature dependence and can move as much as 100 mV in either direction.

Signal Level Stop Using the Meter Output, Pin 8

As mentioned previously, R6 C8 is not necessary when the meter output is used to drive pin 13. Consequently, this time constant is not a factor in determining the stop time. However, the speed at which the meter voltage can move may become important in this regard. This speed is a function of the resistive load on pin 8 and filter capacitance, C5.

AGC Time Constant

In tuning from a strong station to a weaker station above the level stop threshold, the AGC voltage will move in order to try to maintain a constant tuner output. The AGC voltage must move sufficiently fast so that the tuner is gain increased to the point that the level stop indicates a valid station. This time constant is controlled by R11 and C13.

DISTORTION COMPENSATION CIRCUIT

The quadrature detector of the LM1865 has been designed with a special circuit that compensates for distortion generated by the non-linear phase characteristic of the quadrature coil. This circuit not only has the effect of reducing distortion, but also desensitizes the distortion as a function of tuning characteristic. As a result, low distortion is achieved with a single tuned quad coil without the need for a double tuned coil which is costly and difficult to adjust on a production basis. The lower distortion has been achieved without any degradation of the noise floor of the audio output. Futhermore, the compensation circuit first-order cancels the effect of quadrature coil Q on distortion.

When measuring the total harmonic distortion (THD) of the LM1865, it is imperative that a low distortion RF generator be used. In the past it has been possible to cancel out distortion in the generator by adjustment of the quadrature coil. This is because centering the quadrature coil at other than the point of inflection on the S-curve introduces 2nd harmonic distortion which can cancel 2nd harmonic distortion in the generator. Thus low THD numbers may have been obtained wrongly. Large AFT offsets asymmetrical off tuning characteristic, and less than minimum THD will be observed if alignment of the quadrature coil is done with a high distortion RF generator.

Care must also be taken in choosing ceramic filters for the LM1865. It is important to use filters with good group delay characteristics and wide enough bandwidth to pass enough FM sidebands to achieve low distortion.

Application Notes (Continued)

The LM1865 has been carefully designed to insure low AFT offset current at the point of minimum THD. AFT offset current will cause a non-symmetric deviation mute/stop window about the point of minimum THD. No external AFT offset adjustment should be necessary with the LM1865. The amount of resistance in series with the 18 μH quadrature coil drive inductor, L1, has a significant effect on the minimum THD. This series resistance is contributed not only by R13 but also by the Q of L1. The Q of L1 should be as high as possible (ie: Q>50) in order to avoid production problems with the Q variation of L1. Once R13 has been optimized for minimum THD, adjustment on a radio by radio basis should be un-necessary.

DUAL THRESHOLD AGC (AUTOMATIC LOCAL/DISTANCE SWITCH)

There is a well recognized need in the field for gain reducing (AGCing) the front end (tuner) of an FM receiver. This gain reduction is important in preventing overload of the front end which might occur for large signal inputs. Overloading the front end with two out-of-band signals, one channel spacing apart and one channel spacing from center frequency, or, two channel spacings apart and two channel spacings from center frequency, will produce a third order intermodulation product (IM_3) which falls inband. This IM_3 product can completely block out a weaker desired station. The AGC in the LM1865 has been specially designed to deal with the problem of IM_3.

With the LM1865 system, a low AGC threshold is achieved whenever there are strong out-of-band signals that might generate an interfering IM_3 product, and a high AGC threshold is achieved if there are no strong out-of-band signals. The high AGC threshold allows the receiver to obtain its best signal-to-noise performance when there is no possibility of an IM_3 product. The low AGC threshold allows for weaker desired stations to be received without gain-reducing the tuner. It should be noted that when the AGC threshold is set low, there will be a signal-to-noise compromise, but is assumed that it is more desirable to listen to a slightly noisy station than to listen to an undesired IM_3 product. The simplified circuit diagram (*Figure 5*) of the AGC system shows how the dual AGC thresholds are achieved.

V_m = 1V corresponds to a fixed in-band signal level (defined as V_{NB}) at the tuner output. V_{NB} will be referred to as the "narrow band threshold". V_{WB} also corresponds to a fixed tuner output which can either be an in-band or out-of-band signal. This fixed tuner output will be called the "wide band threshold". Always $V_{WB} > V_{NB}$. R11 and C13 define the AGC time constant. A reverse AGC system is shown. This means that V_{AGC} decreases to gain-reduce the tuner. The LM1865 AGC output is an open-collector current source capable of sinking at least 1 mA.

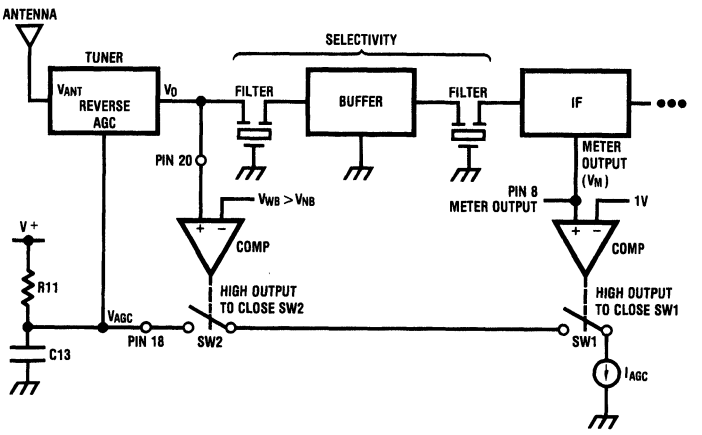

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FIGURE 5. Dual Threshold AGC

$I_1 = GM_1 V_m$ only if $V_m > 1V$
otherwise $I_1 = 0$

Gm_1, V_{WB} = constants

$I_{AGC} = Gm_2 V_o$ where $Gm_2 = I_1/26$ mV *and*
$V_o > V_{WB}$ otherwise $I_{AGC} = 0$

Application Notes (Continued)

First examine what happens with a single in-band signal as we vary the strength of this signal. *Figures 6 and 7* illustrate what happens at the tuner and AGC outputs.

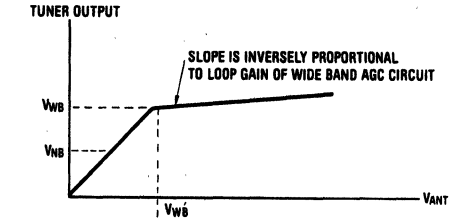


FIGURE 6

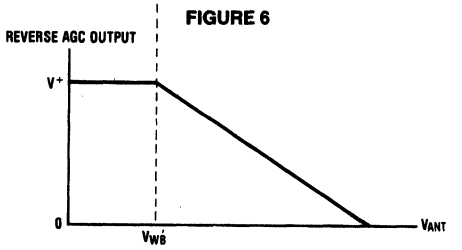


FIGURE 7 TL/H/7509–10

In *Figure 7* there is no AGC output until the tuner output equals the wide band threshold. At this point both SW2 and SW1 are closed and the AGC holds the tuner output in *Figure 6* relatively constant.

Another simple case to examine is that of the single out-of-band signal. Here there is no AGC output even if the signal exceeds V_{WB}. There is no output because the ceramic filters prevent the out-of-band signal from getting to the input of the IF. With no signal at the IF input there is no meter output and SW1 is open, which means No AGC.

Figures 8 and 9 illustrate what happens at the tuner and AGC outputs when the strength of an in-band signal is varied in the presence of a strong out-of-band signal (i.e., greater than V_{WB}) which is held constant at the tuner input. For this example, the in-band signal at the tuner output will be referred to as V_D (desired signal), and the out-of-band signal as V_{UD} (undesired signal).

In *Figure 9*, we see that there is no AGC output until the tuner output exceeds the narrow band threshold, V_{NB}. At this point $V_m > 1V$ and SW1 closes. Further increase of the desired signal at the tuner input results in an AGC current that tries to hold the desired signal at the tuner output constant. This gain reduction of the tuner forces the undesired signal at the tuner output to fall. At the point that V_{UD} reaches the wide band threshold, no further gain reduction can occur as V_O would fall below V_{WB} (refer to *Figure 5*). At this point, control of the AGC shifts from the meter output (narrow band loop) to the out-of-band signal (wide band loop). Here V_{UD} is held constant along with the AGC

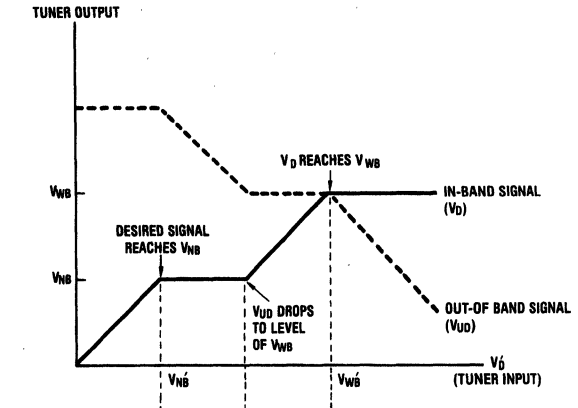
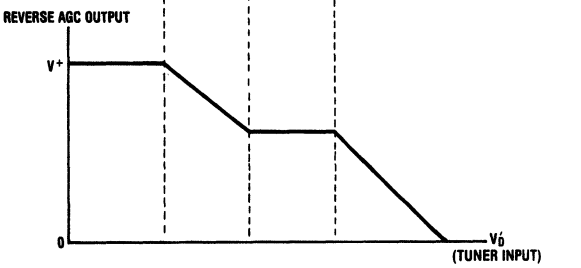


FIGURE 8



TL/H/7509–11

Prime indicates referenced to tuner input

FIGURE 9

Application Notes (Continued)

voltage, while V_D is allowed to increase. V_D will increase until it reaches the level of the wide band threshold at the tuner output. When this occurs V_{UD} is no longer needed to keep $V_o > V_{WB}$ as V_D takes over the job. Thus V_{UD} will drop as the amount of AGC increases, while V_D is held constant by the AGC.

When compared to the simple case of a single in-band signal, we see that because of the presence of a strong out-of-band signal, AGC action has occurred earlier. For the simple case, AGC started when $V_D \geq V_{WB}$. For the two signal case above, AGC started when $V_D \geq V_{NB}$. Thus, the LM1865 achieves an early AGC when there are strong adjacent channels that might cause IM_3, and a later AGC when these signals aren't present.

For the range of signal levels that the tuner was gain-reduced and $V_D < V_{WB}$ there was loss in signal-to-noise in the recovered audio as compared to the case where there was no gain reduction in this interval. *Note, however, that the tuner is not desensitized by the AGC to weak desired stations below the narrow band threshold.*

NARROW BAND AGC THRESHOLD ADJUSTMENT

Both the narrow band and wide band AGC thresholds are user adjustable. This allows the user to optimize the AGC response to a given tuner. Referring to *Figure 5*, when the meter output exceeds 1V a comparator closes SW1. A simplified circuit diagram of this comparator is shown in *Figure 10*.

The 1K resistor in series with pin 8 allows for an upward adjustment of the narrow band threshold. This is accomplished by externally loading pin 8 with a resistor. *Figure 11* illustrates how this adjustment takes place.

From *Figure 11* it is apparent that loading the meter output not only moves the narrow band threshold, but also decreases the meter output for a given input.

In general one chooses the narrow band threshold based on what signal-to-noise compromise is considered acceptable.

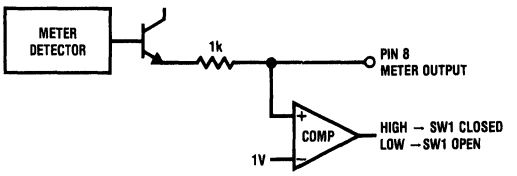


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FIGURE 10. Narrow Band Threshold Circuit

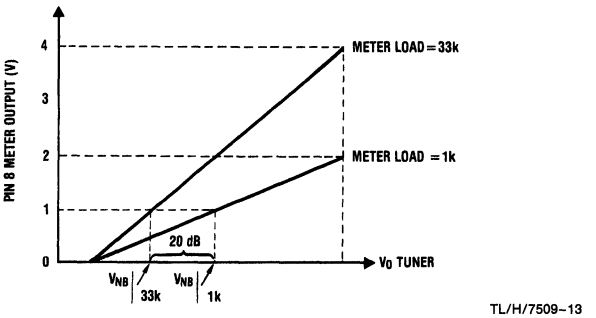

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FIGURE 11. Affect of Meter Load on Narrow Band Threshold

Application Notes (Continued)

WIDE BAND AGC THRESHOLD ADJUSTMENT

There are a number of criteria that determine where the wide band threshold should be set. If the threshold is set too high, protection against IM_3 will be lost. If the threshold is set too low, the front end, under certain input conditions, may be needlessly gain-reduced, sacrificing signal-to-noise performance. Ideally, the wide band threshold should be set to a level that will insure AGC operation whenever there are out-of-band signals strong enough to generate an IM_3 product of sufficient magnitude to exceed the narrow band threshold. Ideally, this level should be high enough to allow for a single in-band desired station to AGC the tuner, only after the maximum signal-to-noise has been achieved.

In order to insure that the wide band loop is activated whenever the IM_3 exceeds the narrow band threshold, V_{NB}, determine the minimum signal levels for two out-of-band signals necessary to produce an IM_3 equal to V_{NB}. Then, arrange for the wide band loop to be activated whenever the tuner output exceeds the rms sum of these signals. There are many combinations of two out-of-band signals that will produce an IM_3 of a given level. However, there is only one combination whose rms sum is a minimum at the tuner output. IM_3 at the tuner output is given according to the equation:

$IM_3 = aV_{UD1}{}^2 V_{UD2}$ (assuming no gain reduction) (1)

where a = constant dependent on the tuner;

V_{UD1} = out-of-band signal 400 kHz from center frequency, applied to tuner input;

V_{UD2} = out-of-band signal 800 kHz from center frequency and 400 kHz away from V_{UD1}, applied to tuner input.

In general, due to tuned circuits within the tuner, the tuner gain is not constant with frequency. Thus, if the tuner is kept fixed at one frequency while the input frequency is changed, the output level will not remain constant. *Figure 12* illustrates this.

It can be shown that for a given IM_3, the combination of V_{UD1} and V_{UD2} that produces the smallest rms sum at the tuner output is given by the equations:

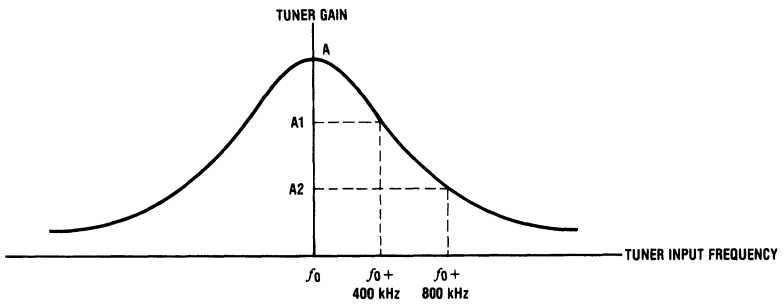
$$V_{UD1} = 1.12 \left(\frac{A2}{A1}\frac{IM_3}{a}\right)^{1/3} \quad (2)$$

$$V_{UD2} = 0.794 \left(\frac{A1^2}{A2^2}\frac{IM_3}{a}\right)^{1/3} \quad (3)$$

Therefore, in order to guarantee that the AGC will be keyed for an $IM_3 = V_{NB}$ we need only satisfy the condition:

$$V_{WB} \leq \sqrt{V_{NB}^2 + \left[(A1)(1.12)\left(\frac{A2}{A1}\frac{V_{NB}}{a}\right)^{1/3}\right]^2 + \left[A2\,(0.794)\left(\frac{A1^2}{A2^2}\frac{V_{NB}}{a}\right)^{1/3}\right]^2} \quad (4)$$

The right hand term of equation (4) defines an upper limit for V_{WB} called V_{WBUL}. V_{WBUL} is the rms sum of all the signals at the tuner output for two out-of-band signals, V_{UD1} and V_{UD2} [as expressed in equations (2) and (3)], applied to the tuner input.



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Define A = tuner gain at center frequency

A1 = tuner gain at f_0 + 400 kHz

A2 = tuner gain at f_0 + 800 kHz

FIGURE 12

Application Notes (Continued)

In order to make the calculation in equation (4), the constants a, A1, A2 must first be determined. This is done by the following procedure:

1. Connect together two RF generators and apply them to the tuner input. Since the generators will terminate each other, remove the 50Ω termination at the tuner input.
2. Connect a spectrum analyzer to the tuner output. Most spectrum analyzers have 50Ω input impedances. To make sure that this impedance does not load the tuner output use a FET probe connected to the spectrum analyzer. The tuner output should be terminated with a ceramic filter.
3. Disconnect the AGC line to the tuner. Make sure that the tuner is not gain-reduced.
4. Adjust the two RF generators for about 1 mV input and to frequencies 400 kHz and 800 kHz away from center frequency (*Figure 13*).
5. Note the three output levels in volts.
6. Knowing the tuner input levels for V_{UD1} and V_{UD2} and the resulting IM_3 just measured, "a" is calculated from the formula:

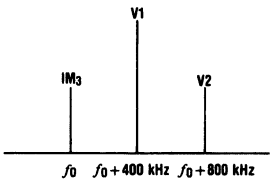
$$a = \frac{IM_3}{V_{UD1}^2 V_{UD2}} \quad (5)$$

where all levels are in volts rms. A typical value for "a" might be 2×10^6.

7. A1 and A2 are calculated according to the following formulas

$$A1 = \frac{V1}{V_{IN}\big|_{f_o + 400\ kHz}} \quad (6)$$

$$A2 = \frac{V2}{V_{IN}\big|_{f_o + 800\ kHz}} \quad (7)$$



$f_o = 10.7$ MHz

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FIGURE 13. Spectrum Analyzer Display of Tuner Output

If the wide band threshold was set to V_{WBUL}, then when a single in-band station reached the level V_{WBUL} at the tuner output, AGC action would start to take place. For this reason it is hoped that V_{WBUL} is above the level that will allow for maximum signal-to-noise. If, however, this is not the case, consideration might be given to improving the intermodulation performance of the tuner.

The lower limit for V_{WB} is the minimum tuner output that achieves the best possible signal-to-noise ratio in the recovered audio. In general, it is desirable to set V_{WB} closer to the upper limit rather than the lower limit. This is done to prevent AGC action within the narrow band loop except when there is a possibility of an IM_3 greater than V_{NB}.

The wide band threshold at the pin 20 input to the LM1865 is fixed at 12 mVrms. Generally speaking, if pin 20 were driven directly from the tuner output. V_{WB} would be too low. Therefore, in general, pin 20 is not connected directly to the tuner output. Instead the tuner output is attenuated and then applied to pin 20. Increasing attenuation increases the wide band threshold, V_{WB}.

Pin 20 has an input impedance at 10.7 MHz that can be modeled as a 500Ω resistor in series with a 19 pF capacitor, giving a total impedance of 940Ω ∠−58°. Thus an easy way to attenuate the input to pin 20 is with the arrangement shown in *Figure 14*.

Notice that pin 20 must be AC coupled to the tuner output and that C1 is a bypass capacitor. R1 adjusts the amount of attenuation to pin 20. The wide band threshold will roughly increase by a factor of (R1 + 940Ω)/940Ω.

AGC CIRCUIT USED AS A CONVENTIONAL AGC

If for some reason the dual AGC thresholds are not desired, it is easy to use the LM1865 as a more conventional LM3189 type of AGC. This is accomplished by AC coupling the pin 20 input after the ceramic filters rather than before the filters. Thus, as with the LM3189, only in-band signals will be able to activate the AGC.

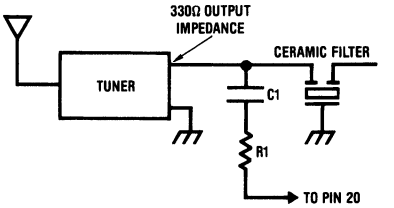

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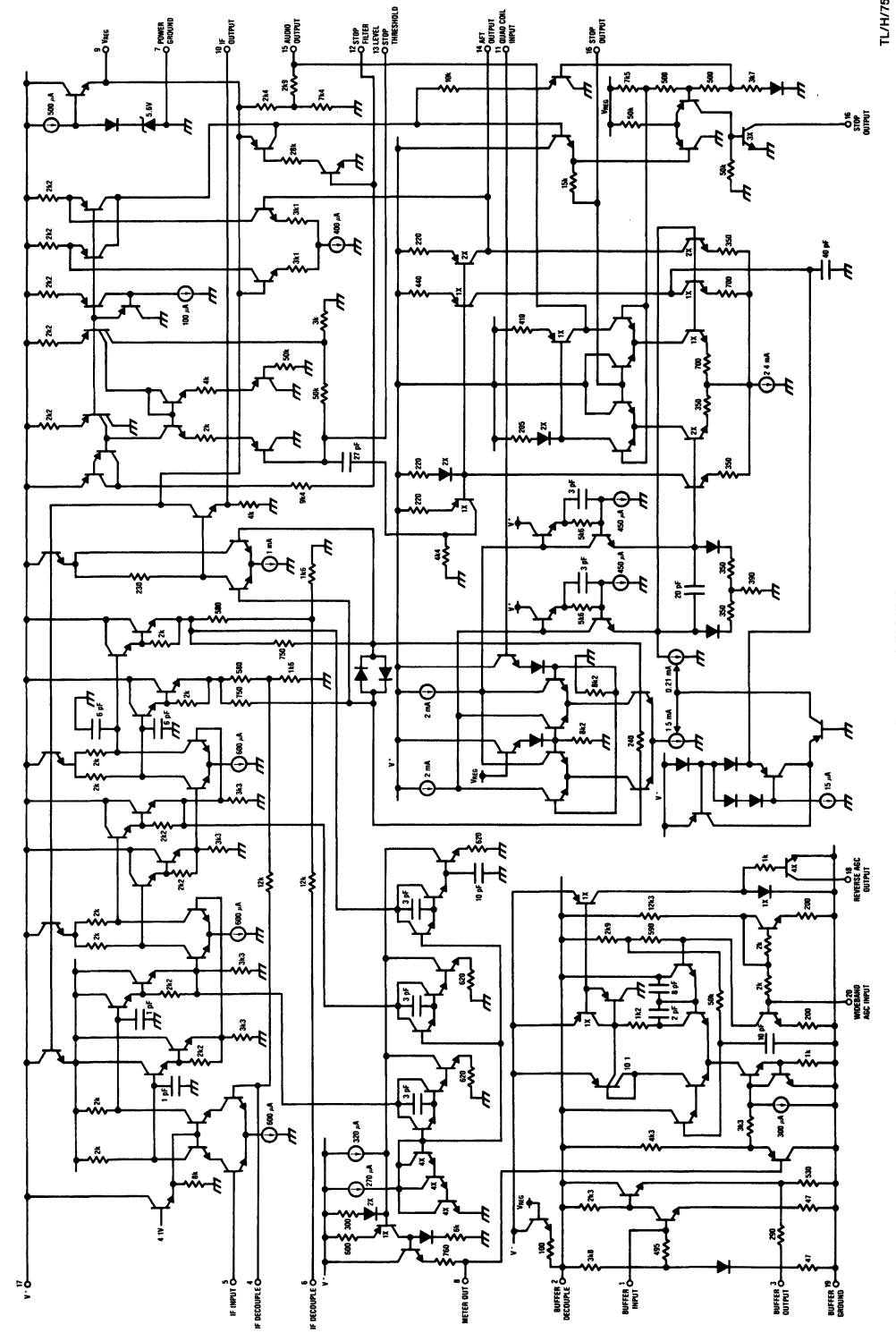
FIGURE 14. Wide Band Threshold Adjustment

Simplified Diagram



TL/H/7509–17

Advanced FM IF System

National Semiconductor

LM1868 AM/FM Radio System

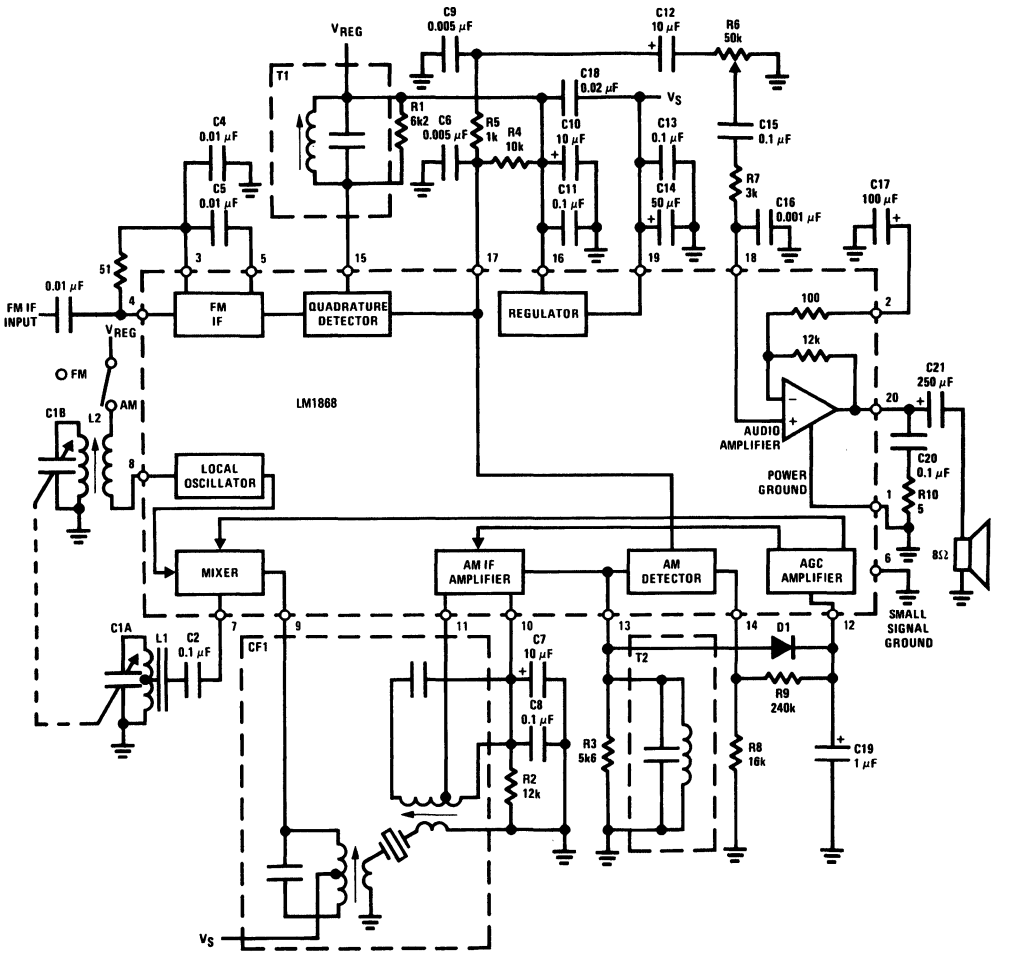
General Description

The combination of the LM1868 and an FM tuner will provide all the necessary functions for a 0.5 watt AM/FM radio. Included in the LM 1868 are the audio power amplifier, FM IF and detector, and the AM converter, IF, and detector. The device is suitable for both line operated and 9V battery applications.

Features

- DC selection of AM/FM mode
- Regulated supply
- Audio amplifier bandwidth decreased in AM mode, reducing amplifier noise in the AM band
- AM converter AGC for excellent overload characteristics
- Low current internal AM detector for low tweet radiation

Block Diagram



TL/H/7909–1

Order Number LM1868N
See NS Package Number N20A

Note: See table for coil data

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

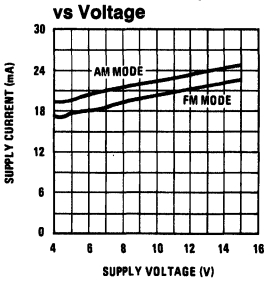
Supply Voltage (Pin 19)	15V
Package Dissipation	2.0W
Above T_A = 25°C, Derate Based on $T_{J(MAX)}$ = 150°C and θ_{JA} = 60°C/W	
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics Test Circuit, T_A = 25°C, V_S = 9V, R_L = 8Ω (unless otherwise noted)

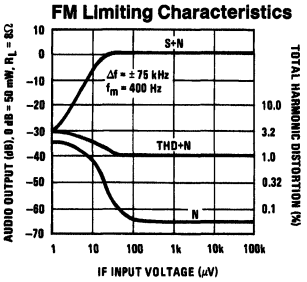
Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS e_{AM} = 0, e_{FM} = 0					
Supply Current	AM Mode, S1 in Position 1		22	30	mA
Regulator Output Voltage (Pin 16)		3.5	3.9	4.8	V
Operating Voltage Range		4.5		15	
DYNAMIC CHARACTERISTICS—AM MODE f_{AM} = 1 MHz, f_{mod} = 1 kHz, 30% Modulation, S1 in Position 1, P_O = 50 mW unless noted					
Maximum Sensitivity	Measure e_{AM} for P_O = 50 mW, Maximum Volume	8		16	μV
Signal-to-Noise	e_{AM} = 10 mV	40	50		dB
Detector Output	e_{AM} = 1 mV Measure at Top of Volume Control	40	60	85	mV
Overload Distortion	e_{AM} = 50 mV, 80% Modulation		2	10	%
Total Harmonic Distortion (THD)	e_{AM} = 10 mV		1.1	2	%
DYNAMIC CHARACTERISTICS—FM MODE f_{FM} = 10.7 MHz, f_{mod} = 400 Hz, Δf = ±75 kHz, P_O = 50 mW, S1 in Position 1					
−3 dB Limiting Sensitivity			15	45	μV
Signal-to-Noise Ratio	e_{FM} = 10 mV	50	64		dB
Detector Output	e_{FM} = 10 mV, Δf = ±22.5 kHz Measure at Top of Volume Control	40	60	85	mV
AM Rejection	e_{FM} = 10 mV, 30% AM Modulation	40	50		dB
Total Harmonic Distortion (THD)	e_{FM} = 10 mV		1.1	2	%
DYNAMIC CHARACTERISTICS—AUDIO AMPLIFIER ONLY f = 1 kHz, e_{AM} = 0, e_{FM} = 0, S1 in Position 2					
Power Output	THD = 10%, R_L 8Ω V_S = 6V V_S = 9V	 250 500	 325 700		 mW mW
Bandwidth	AM Mode, P_O = 50 mW FM Mode, P_O = 50 mW		11 22		kHz kHz
Total Harmonic Distortion (THD)	P_O = 50 mW, FM Mode		0.2		%
Voltage Gain			41		dB

Typical Performance Characteristics (Test Circuit) All curves are measured at audio output

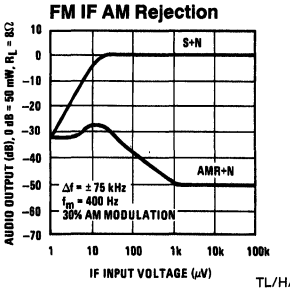
Quiescent Supply Current vs Voltage



FM Limiting Characteristics



FM IF AM Rejection

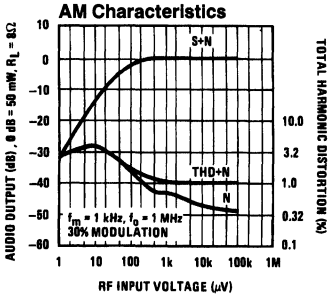


TL/H/7909–2

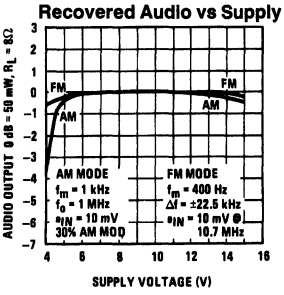
Typical Performance Characteristics (Continued)

All curves are measured at audio output (Test Circuit)

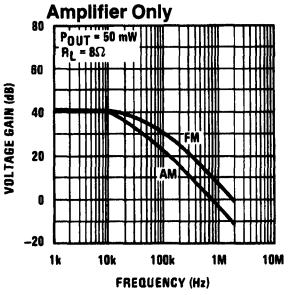
AM Characteristics



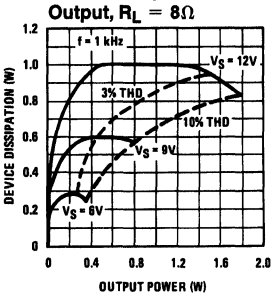
Recovered Audio vs Supply



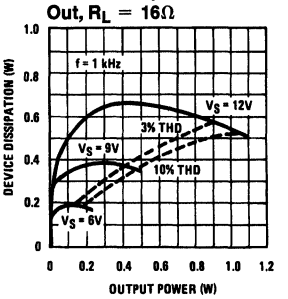
Gain vs Frequency Audio Amplifier Only



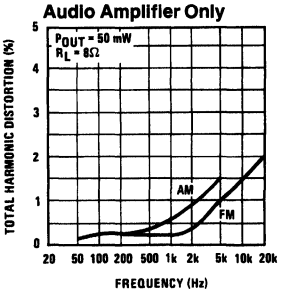
Power Dissipation vs Power Output, $R_L = 8\Omega$



Power Dissipation vs Power Out, $R_L = 16\Omega$

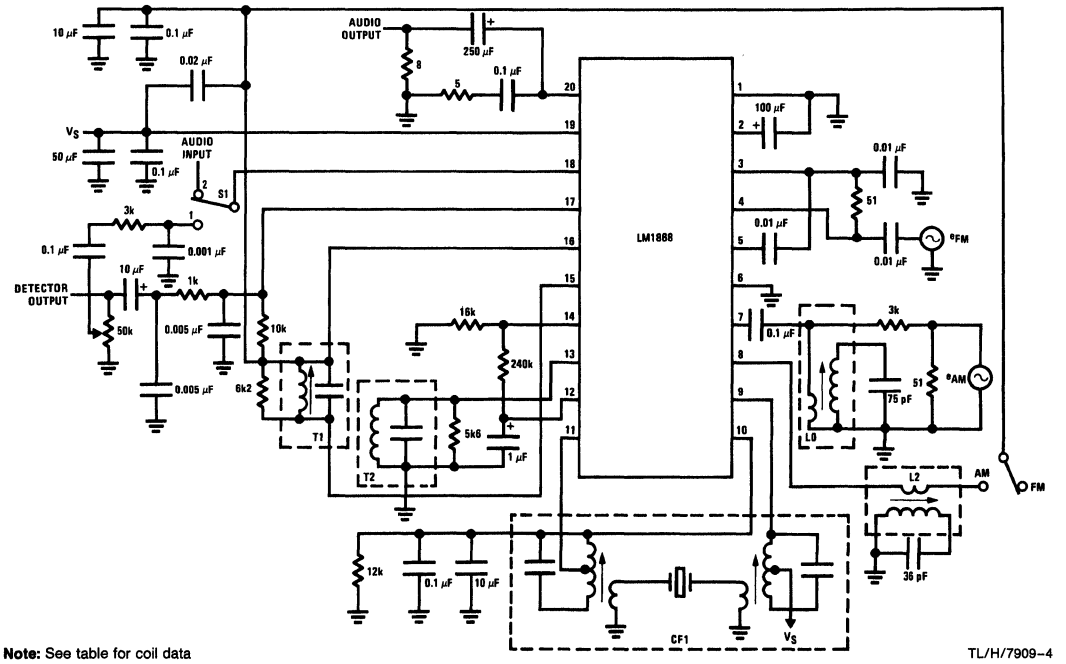


Distortion vs Frequency Audio Amplifier Only



TL/H/7909–3

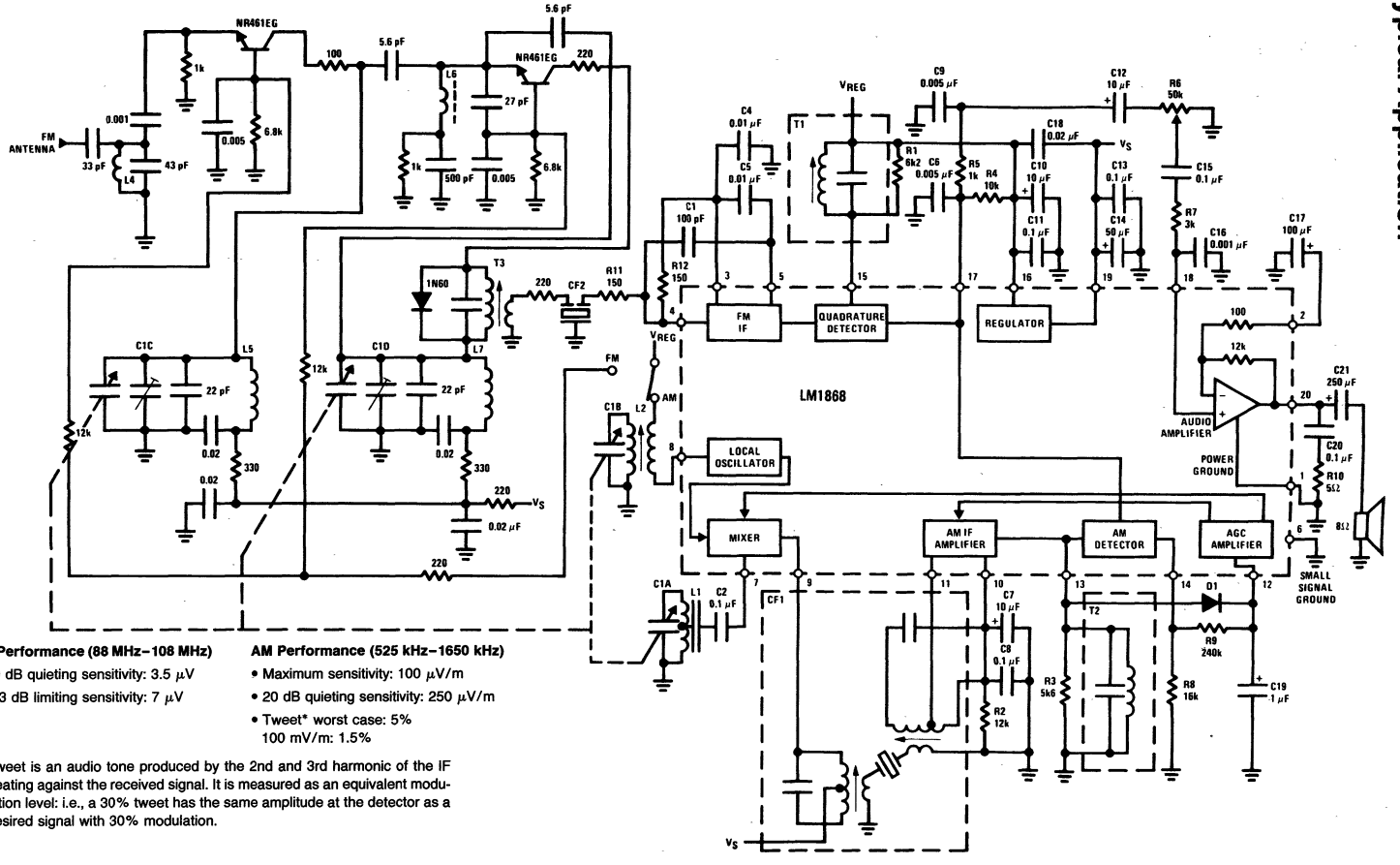
Test Circuit



Note: See table for coil data

TL/H/7909–4

Typical Application



FM Performance (88 MHz–108 MHz)

- 30 dB quieting sensitivity: 3.5 µV
- −3 dB limiting sensitivity: 7 µV

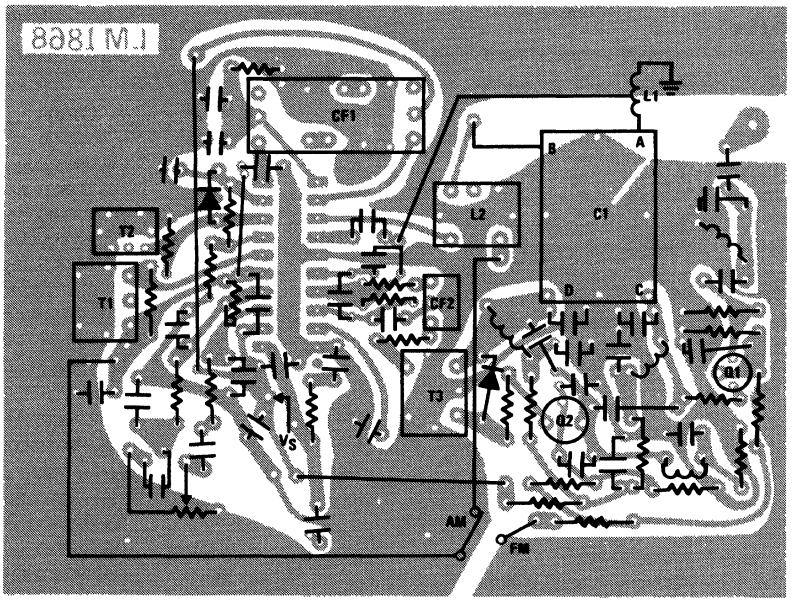
AM Performance (525 kHz–1650 kHz)

- Maximum sensitivity: 100 µV/m
- 20 dB quieting sensitivity: 250 µV/m
- Tweet* worst case: 5%
  100 mV/m: 1.5%

*Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: i.e., a 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

TL/H/7909–5

PC Board Layout

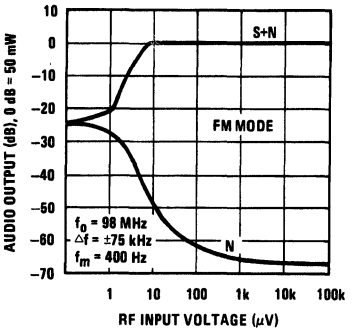


TL/H/7909–6

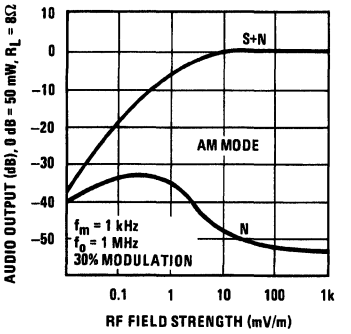
Component Side

Typical Performance Characteristics Typical Application

All curves are measured at audio output



TL/H/7909–7



TL/H/7909–8

IC External Components (Application Circuit)

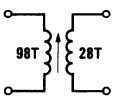
Component	Typical Value	Comments
C1	100 pF	Removes tuner LO from IF input
C2	0.1 μF	Antenna coupling capacitor
C4, C5	0.01 μF	FM IF decoupling capacitors
C6, C9	0.005 μF	AM smoothing/FM de-emphasis network, de-emphasis pole is given by. $f1 \cong \frac{1}{2\pi\,(C6 + C9)\left(\frac{R4\ \ R6}{R4 + R6}\right)}$
R5	1k	
C10	10 μF	Regulator decoupling capacitor
C11	0.1 μF	Regulator decoupling capacitor
C12	10μF	AC coupling to volume control
C13	0.1 μF	Power supply decoupling
C14	50 μF	Power supply decoupling
C15	0.1 μF	Audio amplifier input coupling
R7	3k	Roll off signals from detector in the AM band to prevent radiation
C16	0.001 μF	
C17	100 μF	Power amplifier feedback decoupling, sets low frequency supply rejection
R8	16k	AM detector bias resistor
R9	240k	Set AGC time constant
C19	1 μF	
C7	10 μF	IF coupling
C8	0.1 μF	IF coupling
C20	0.1 μF	High frequency load for audio amplifier, required to stabilize audio amplifier
R10	5Ω	
C21	250 μF	Output coupling capacitor
R1	6k2	Sets Q of quadrature coil, determining FM THD and recovered audio
R2	12k	IF amplifier bias R
R3	5k6	Sets gain of AM IF and Q of AM IF output tank
R4	10k	Detector load resistor
R6	50k	Volume control
C18	0.02 μF	Power supply decoupling
R11, R12	150Ω	Terminates the ceramic filter, biases FM IF input stage
D1	1N4148	Optional. Quickens the AGC response during turn on

Coil and Tuning Capacitor Specifications

C1 — AM ANT 140 pF max 5.0 pF min
AM OSC 82 pF max 5.0 pF min
Trimmers 5 pF
FM 20 pF max 4.5 pF min
TOKO CY2-22124PT

L1 — 640 μH, Q_u = 200
R_P = 3k5 @ F = 796 kHz
(At secondary)
AM antenna
1 mV/meter induces approximately 100 μV open circuit at the secondary

L0, L2 — 360 μH, Q_U > 80 @ F = 796 kHz
TOKO RWO-6A5105 or equivalent



TL/H/7909–9

Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

L4 — SWG #20, N = 3½T, inner diameter = 5 mm

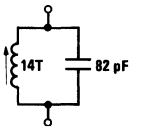
L5 — SWG #20, N = 3½T, inner diameter = 5 mm

L6 — L = 0.44 μH, N = 4 ½T, Qu = 70

L7 — SWG #20, N = 2 ½T, inner diameter = 5 mm

CF2 — 10.7 MHz ceramic filter
MURATA SFE 10.7 mA or equivalent
Murata
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

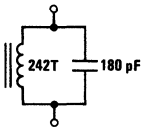
T1



TL/H/7909–10

Q_u > 70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz
TOKO KAC-K2318 or equivalent

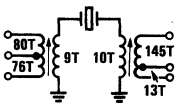
T2



TL/H/7909–11

Q_u > 14 @ 455 kHz, L to resonate w/180 pF @ 455 kHz
TOKO 159GC-A3785 or equivalent

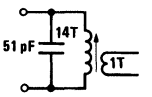
CF1



TL/H/7909–12

TOKO CFU-090D or equivalent
BW > 4.8 kHz @ 455 kHz

T3



TL/H/7909–13

Apollo Electronics NS-107C or equivalent

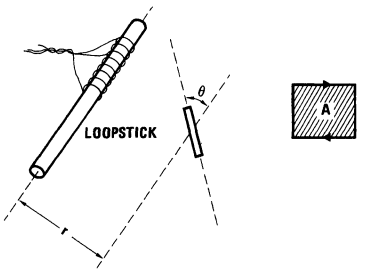
Layout Considerations

AM SECTION

Most problems in an AM radio design are associated with radiation of undesired signals to the loopstick. Depending on the source, this radiation can cause a variety of problems including tweet, poor signal-to-noise, and low frequency oscillation (motor boating). Although the level of radiation from the LM1868 is low, the overall radio performance can be degraded by improper PCB layout. Listed below are layout considerations association with common problems.

1. **Tweet:** Locate the loopstick as far as possible from detector components C6, C9, R4, and R5. Orient C6, C9, R4, and R5 parallel to the axis of the loopstick. Return R8, C6, C9, and C19 to a separate ground run (see Typical Application PCB).

2. **Poor Signal-to-Noise/Low Frequency Oscillation:** Twist speaker leads. Orient R10 and C20 parallel to the axis of the loopstick. Locate C11 away from the loopstick.



TL/H/7909–14

In general, radiation results from current flowing in a loop. In case 1 this current loop results from decoupling detector harmonics at pin 17; while in case 2, the current loop results from decoupling noise at the output of the audio amplifier and the output of the regulator. The level of radiation picked up by the loopstick is approximately proportional to: 1) $1/r^3$; where r is the distance from the center of the loopstick to the center of the current loop; 2) SIN θ, where θ is the angle between the plane of the current loop and the axis of the loopstick; 3) I, the current flowing in the loop; and 4) A, the cross-sectional area of the current loop.

Pickup is kept low by short leads (low A), proper orientation ($\theta \cong 0$ so SIN $\theta \cong 0$), maximizing distance from sources to loopstick, and keeping current levels low.

FM SECTION

The pinout of the LM1868 has been chosen to minimize layout problems, however some care in layout is required to insure stability. The input source ground should return to C4 ground. Capacitors C13 and C18 form the return path for signal currents flowing in the quadrature coil. They should connect directly to the proper pins with short PC traces (see Typical Application PCB). The quadrature coil and input circuitry should be separated from each other as far as possible.

AUDIO AMPLIFIER

The standard layout considerations for audio amplifiers apply to the LM1868, that is: positive and negative inputs should be returned to the same ground point, and leads to the high frequency load should be kept short. In the case of the LM1868 this means returning the volume control ground (R6) to the same ground point as C17, and keeping the leads to C20 and R10 short.

Circuit Description (See Equivalent Schematic)

AM SECTION

The AM section consists of a mixer stage, a separate local oscillator, an IF gain block, an envelope detector, AGC circuits for controlling the IF and mixer gains, and a switching circuit which disables the AM section in the FM mode.

Signals from the antenna are AC-coupled into pin 7, the mixer input. This stage consists of a common-emitter amplifier driving a differential amp which is switched by the local oscillator. With no mixer AGC, the current in the mixer is 330 μA; as the AGC is applied, the mixer current drops, decreasing the gain, and also the input impedance drops, reducing the signal at the input. The differential amp connected to pin 8 forms the local oscillator. Bias resistors are arranged to present a negative impedance at pin 8. The frequency of oscillation is determined by the tank circuit, the peak-to-peak amplitude is approximately 300 μA times the impedance at pin 8 in parallel with 8k2.

After passing through the ceramic filter, the IF signals are applied to the IF input. Signals at pin 11 are amplified by two AGC controlled common-emitter stages and then applied to the PNP output stage connected to pin 13. Biasing is arranged so that the current in the first two stages is set by the difference between a 250 μA current source and the Darlington device connected to pin 12.

When the AGC threshold is exceeded, the Darlington device turns ON, steering current away from the IF into ground, reducing the IF gain. Current in the IF is monitored by the mixer AGC circuit. When the current in the IF has dropped to 30 μA, corresponding to 30 dB gain reduction in the IF, the mixer AGC line begins to draw current. This causes the mixer current and input impedance to drop, as previously described.

The IF output is level shifted and then peak detected at detector cap C1. By loading C1 with only the base current of the following device, detector currents are kept low. Drive from the AGC is taken at pin 14, while the AM detector output is summed with the FM detector output at pin 17.

FM SECTION

The FM section is composed of a 6-stage limiting IF driving a quadrature detector. The IF stages are identical with the exceptions of the input stage, which is run at higher current to reduce noise, and the last stage, which is switched OFF in the AM mode. The quadrature detector collectors drive a level shift arrangement which allows the detector output load to be connected to the regulated supply.

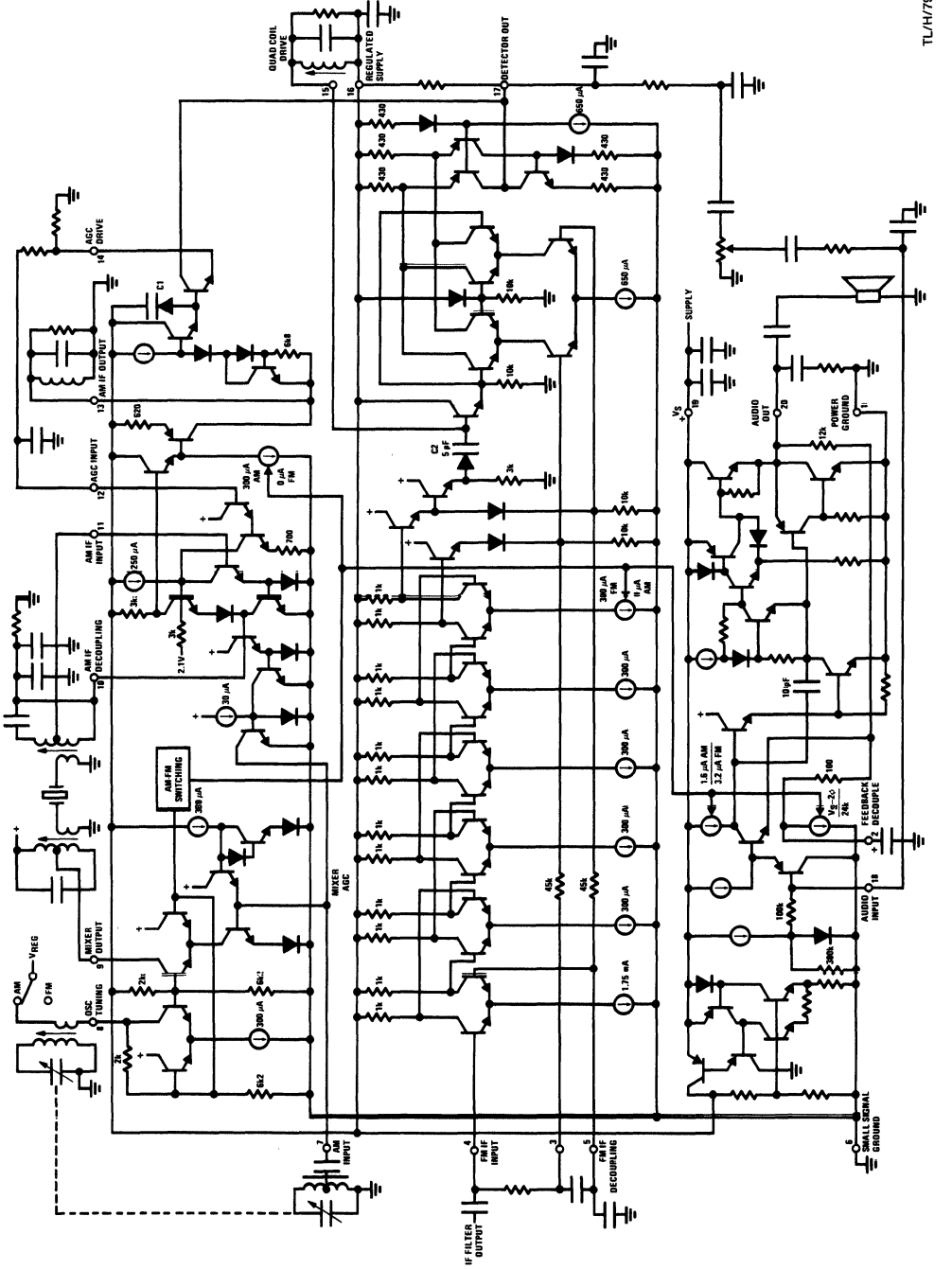
AUDIO AMPLIFIER

The audio amplifier has an internally set voltage gain of 120. The bandwidth of the audio amplifier is reduced in the AM mode so as to reduce the output noise falling in the AM band. The bandwidth reduction is accomplished by reducing the current in the input stage.

REGULATOR

A series pass regulator provides biasing for the AM and FM sections. Use of a PNP pass device allows the supply to drop to within a few hundred millivolts of the regulator output and still be in regulation.

Equivalent Schematic



TL/H/7909–15

National Semiconductor

LM3089 FM Receiver IF System

General Description

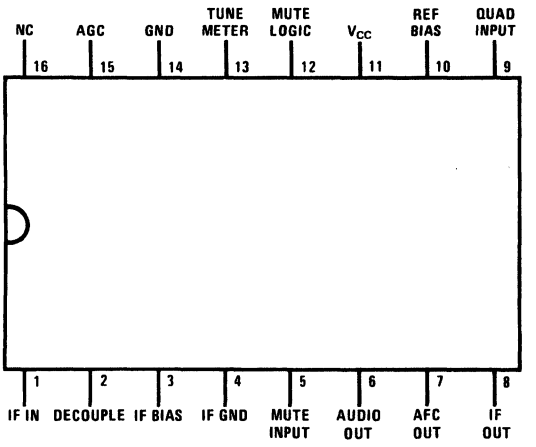
The LM3089 has been designed to provide all the major functions required for modern FM IF designs of automotive, high-fidelity and communications receivers.

Features

- Three stage IF amplifier/limiter provides 12 μV (typ) −3 dB limiting sensitivity
- Balanced product detector and audio amplifier provide 400 mV (typ) of recovered audio with distortion as low as 0.1% with proper external coil designs.
- Four internal carrier level detectors provide delayed AGC signal to tuner, IF level meter drive current and interchannel mute control
- AFC amplifier provides AFC current for tuner and/or center tuning meters
- Improved operating and temperature performance, especially when using high Q quadrature coils in narrow band FM communications receivers
- No mute circuit latchup problems
- A direct replacement for CA3089E

Connection Diagram

Dual-In-Line Package

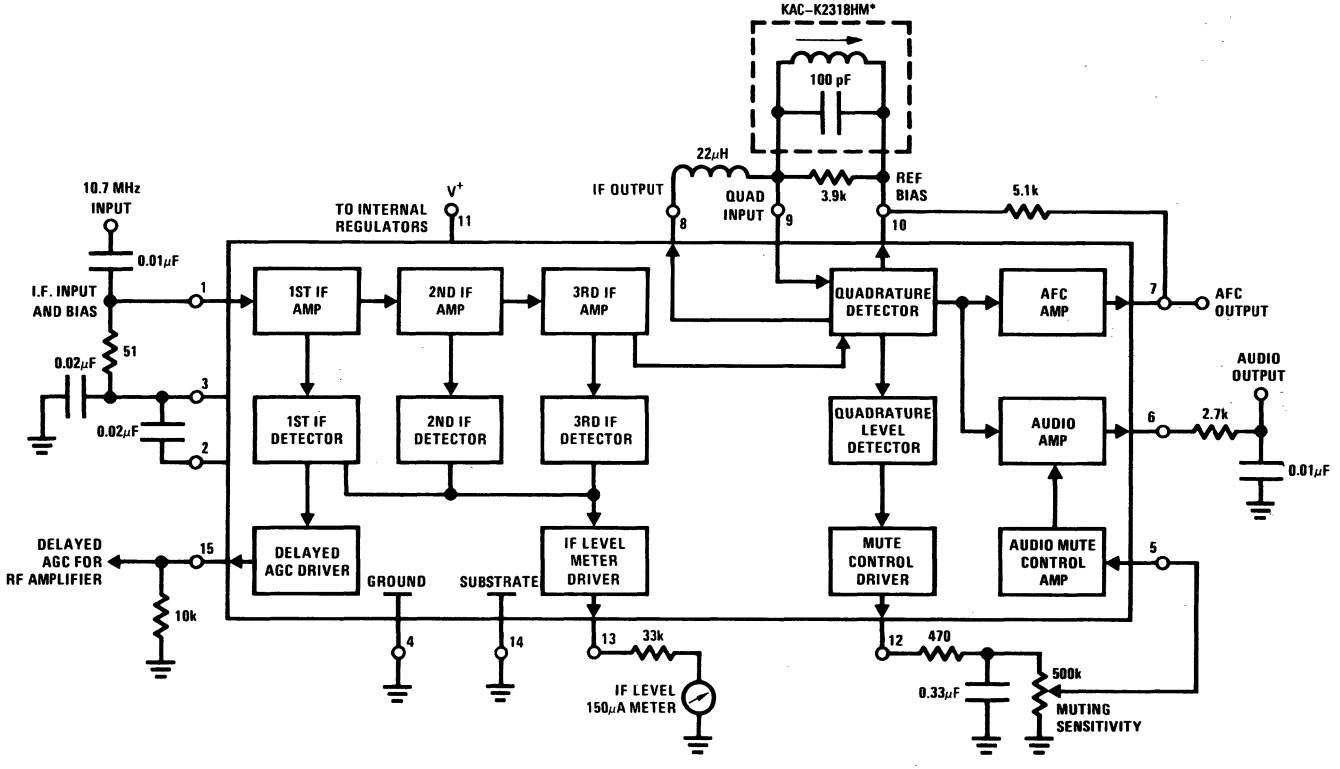


TL/H/7149–2

Top View

Order Number LM3089N
See NS Package Number N16E

Block Diagram



TL/H/7149–1

Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Between Pin 11 and Pins 4, 14	+16V
DC Current Out of Pin 12	5 mA
DC Current Out of Pin 13	5 mA
DC Current Out of Pin 15	2 mA
Power Dissipation (Note 2)	1500 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +12V, see Test Circuit)

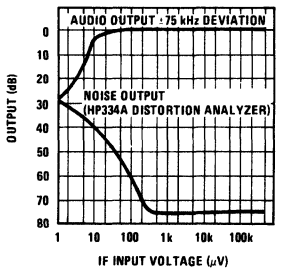
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS (V_{IN} = 0, NOT MUTED)						
I_{11}	Supply Current		16	23	30	mA
V1, 2, 3	IF Input and Bias		1.2	1.9	2.4	V
V6	Audio Output		5.0	5.6	6.0	V
V7	AFC Output		5.0	5.6	6.0	V
V10	Reference Bias		5.0	5.6	6.0	V
V12	Mute Control		5.0	5.4	6.0	V
V13	IF Level			0	0.5	V
V15	Delayed AGC		4.2	4.7	5.3	V
DYNAMIC CHARACTERISTICS f_o = 10.7 MHZ, Δf = ±75 kHz @ 400 Hz						
V_{IN}(LIM)	Input Limiting −3 dB			12	25	μV
AMR	AM Rejection	V_{IN} = 100 mV, AM: 30%	45	55		−dB
V_O(AF)	Recovered Audio	V_{IN} = 10 mV	300	400	500	mVrms
THD	Total Harmonic Distortion					
	Single Tuned (Note 1)	V_{IN} = 100 mV		0.5	1.0	%
	Double Tuned (Note 1)	V_{IN} = 100 mV		0.1	0.3	%
S+N/N	Signal to Noise Ratio	V_{IN} = 100 mV	60	70		dB
V12	Mute Control	V_{IN} = 100 mV		0	0.5	V
V13	IF Level	V_{IN} = 100 mV	4.0	5.0	6.0	V
V13	IF Level	V_{IN} = 500 μV	1.0	1.5	2.0	V
V15	Delayed AGC	V_{IN} = 100 mV		0.1	0.5	V
V15	Delayed AGC	V_{IN} = 30 mV		2.5		V
V_O(AF)	Audio Muted	V_{IN} = 100 mV, V5 = +2.5V		60		−dB

Note 1: Distortion is a function of quadrature coil used.

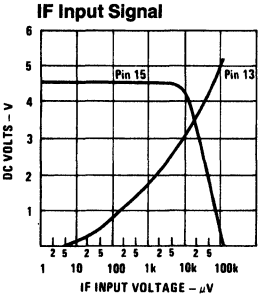
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Typical Performance Characteristics

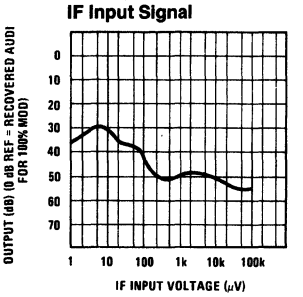
Typical S + N/N and IF Limiting Sensitivity vs IF Input Signal



Typical AGC (Pin 15) and Meter Output (Pin 13) vs IF Input Signal

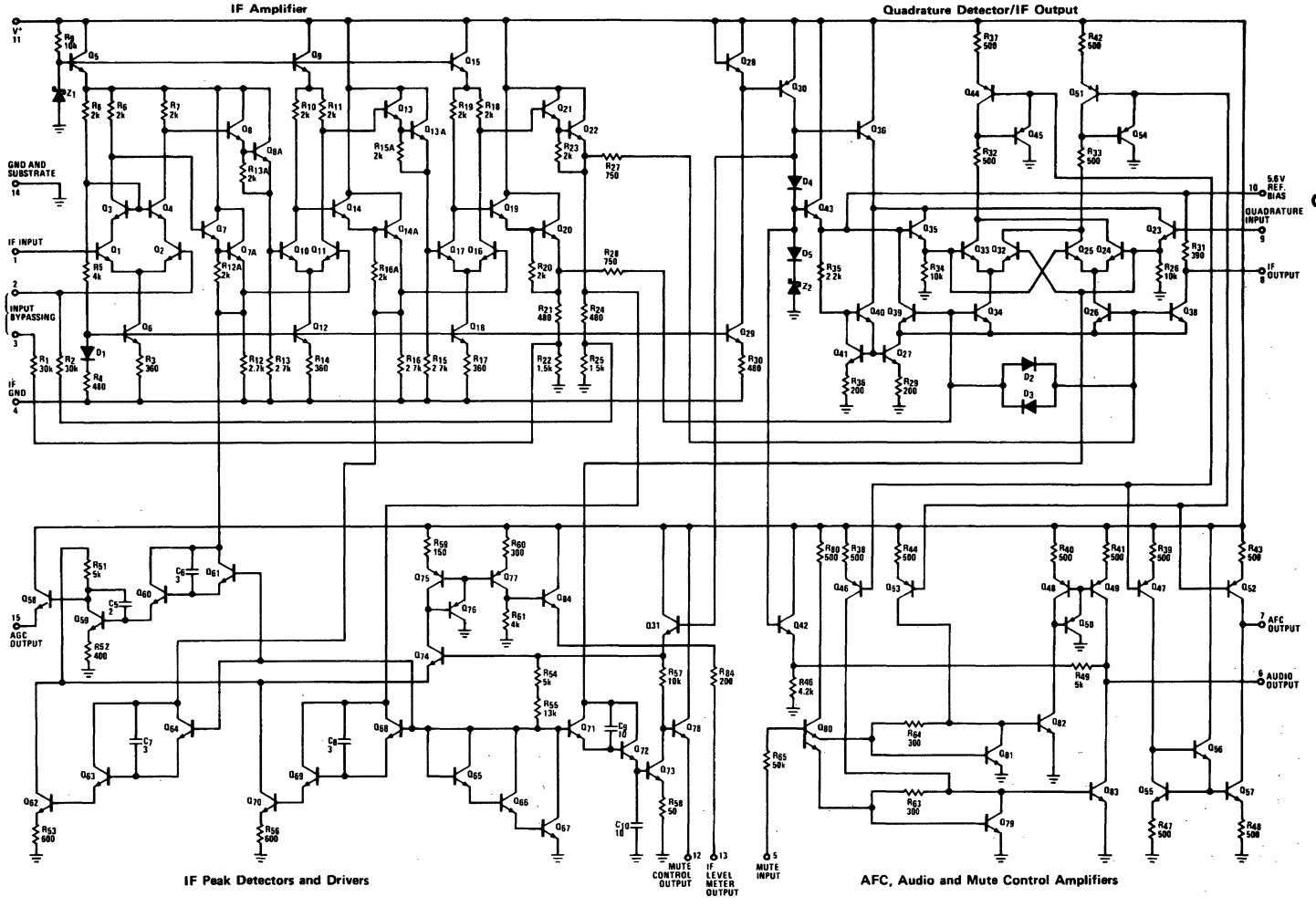


AM Rejection (30% Mod) vs IF Input Signal



TL/H/7149–3

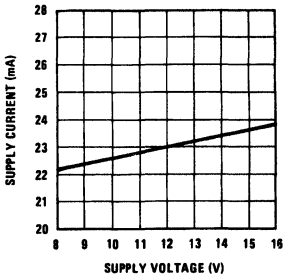
Schematic Diagram



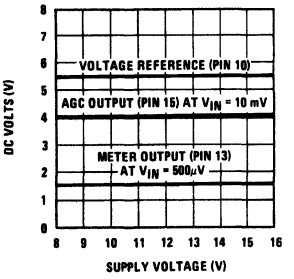
TL/H/7149–4

Typical Performance Characteristics

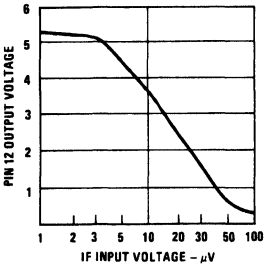
Supply Current (I_{11}) vs Supply Voltage (V11)



Reference Voltage, AGC and Meter Output vs Supply Voltage

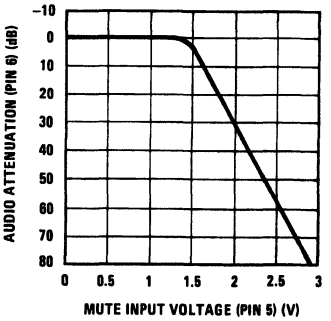


Mute Control Output (Pin 12) vs IF Input Signal



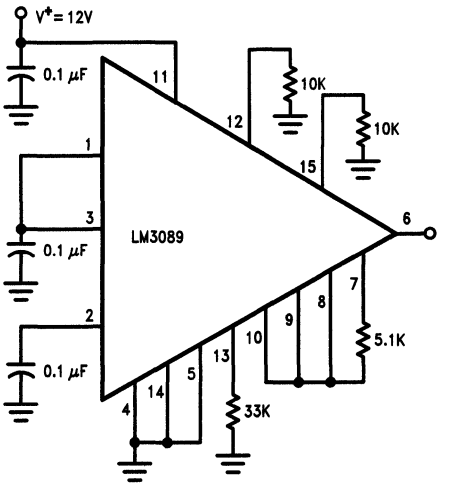
TL/H/7149–5

Typical Audio Attenuation (Pin 6) vs Mute Input Voltage (Pin 5)



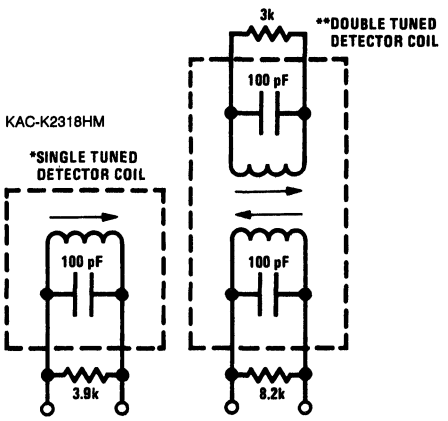
TL/H/7149–6

DC Test Circuit



TL/H/7149–7

AC Test Circuit



TL/H/7149–8

*For single tuned dectector coil:
L_O tunes with 100 pF at 10.7 MHz
Q_{UL} (unloaded) ≅ 75
Q_L (loaded) ≅ 13 for V9 ≅ 150 mVrms

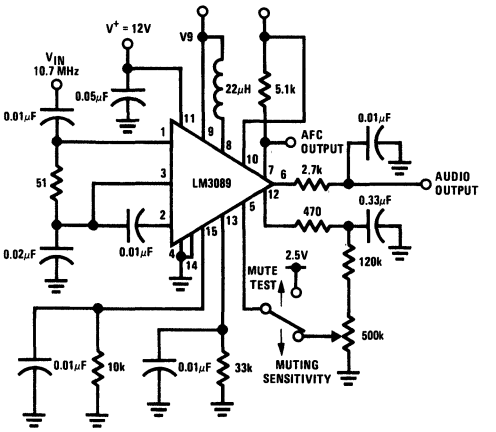
**For double tuned detector coil:
Q_{ULPRI} = QULSEC ≅ 75
kQ ≅ 0.7 for V9 ≅ 150 mVrms

Note:

The recovered audio output voltage will be approximately 0.5 dB less when using the double tuned detector coil.

For proper operation of the mute circuit, the RF voltage at pin 9 should be 150 mVrms ±30 mV.

AC Test Circuit (Continued)



TL/H/7149–9

National Semiconductor

LM3189 FM IF System

General Description

The LM3189N is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram of the LM3189N includes a three stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

The LM3189N is ideal for high fidelity operation. Distortion in an LM3189N FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

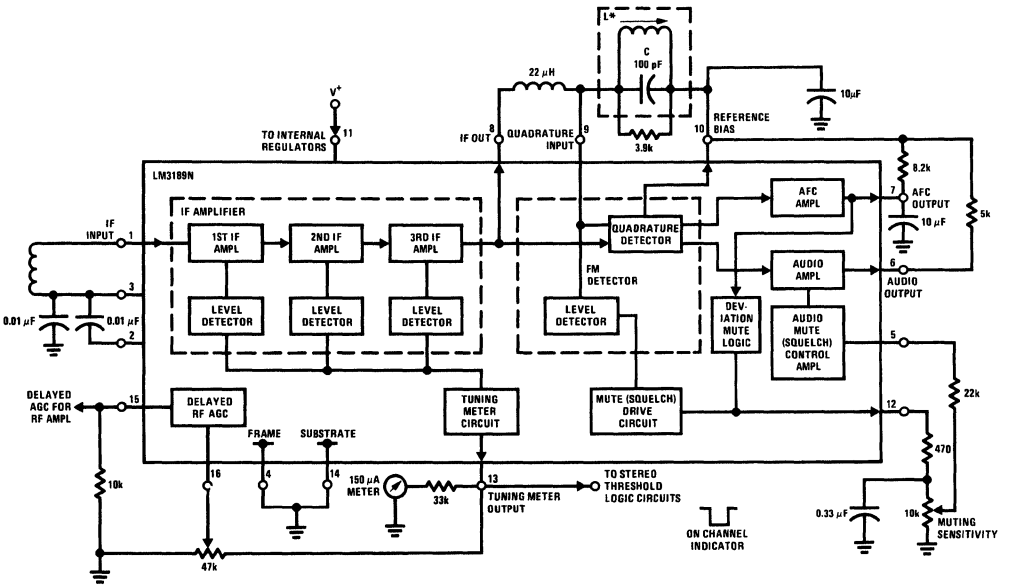
The LM3189N has all the features of the LM3089N plus additions.

The LM3189N utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

Features

- Exceptional limiting sensitivity: 12 μV typ at −3 dB point
- Low distortion: 0.1% typ (with double-tuned coil)
- Single-coil tuning capability
- Improved (S + N)/N ratio
- Externally programmable recovered audio level
- Provides specific signal for control of inter-channel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- On channel step for search control
- Provides programmable AGC voltage for RF amplifier
- Provides a specific circuit for flexible audio output
- Internal supply voltage regulators
- Externally programmable ON channel step width, and deviation at which muting occurs

Block Diagram



TL/H/7960–1

All resistance values are in Ω

*L tunes with 100 pF (C) at 10.7 MHz, $Q_0 \cong 75$
(Toko No. KACS K586HM or equivalent)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Between Pin 11 and Pins 4, 14	16V
DC Current Out of Pin 12	5 mA
DC Current Out of Pin 13	5 mA
DC Current Out of Pin 15	2 mA
Power Dissipation (Note 2)	1500 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $T_A = 25°C, V^+ = 12V$

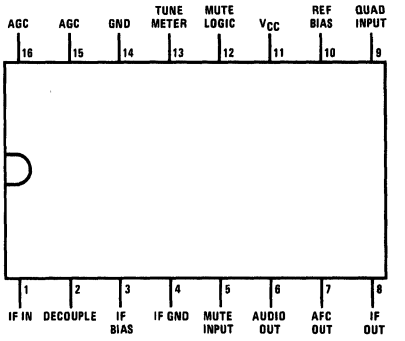
Symbol	Parameter	Conditions (See Single-Tuned Test Circuit)		Min	Typ	Max	Units
STATIC (DC) CHARACTERISTICS							
I_{11}	Quiescent Circuit Current	No Signal Input, Non Muted		20	31	44	mA
	DC Voltages:						
V1	Terminal 1 (IF Input)			1.2	2.0	2.4	V
V2	Terminal 2 (AC Return to Input)			1.2	2.0	2.4	V
V3	Terminal 3 (DC Bias to Input)			1.2	2.0	2.4	V
V15	Terminal 15 (RF AGC)			7.5	9.5	11	V
V10	Terminal 10 (DC Reference)			5	5.75	6	V
DYNAMIC CHARACTERISTICS							
V_I(lim)	Input Limiting Voltage (−3 dB Point)				12	25	μV
AMR	AM Rejection (Term. 6)	V_{IN} = 0.1V	f_o = 10.7 MHz, f_{mod} = 400 Hz, Deviation ±75 kHz	45	55		dB
V_O(AF)	Recovered AF Voltage (Term. 6)	AM Mod. = 30%		325	500	650	mV
THD	Total Harmonic Distortion (Note 1)						
	Single Tuned (Term. 6)	V_{IN} = 0.1V			0.5	1	%
	Double Tuned (Term. 6)				0.1		%
S + N/N	Signal Plus Noise to Noise Ratio (Term. 6)			65	80		dB
f_{DEV}	Deviation Mute Frequency		f_{mod} = 0		±40		kHz
V16	RF AGC Threshold				1.25		V
V12	On Channel Step	V_{IN} = 0.1V	f_{DEV} < ±40 kHz f_{DEV} > ±40 kHz		0 5.6		V

Note 1: THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Connection Diagram

Dual-In-Line Package



TL/H/7960–2

Top View

Order Number LM3189N
See NS Package Number N16E

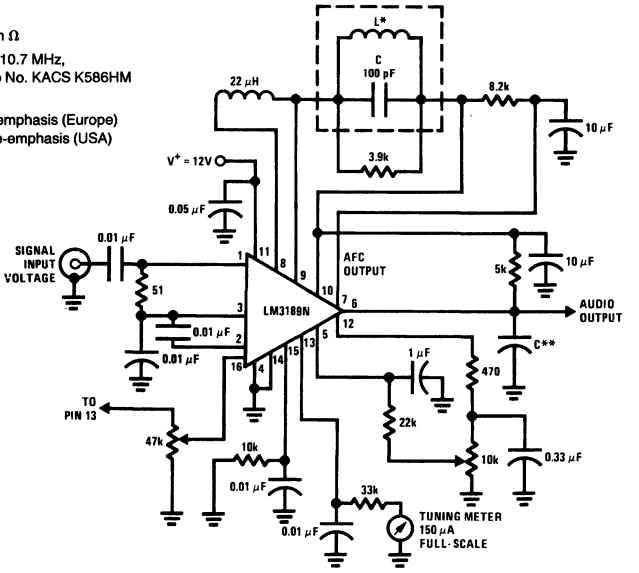
Test Circuits

Test Circuit for LM3189N Using a Single-Tuned Detector Coil

All resistance values are in Ω

*L tunes with 100 pF (C) at 10.7 MHz, Q_o(unloaded) ≅ 75 (Toko No. KACS K586HM or equivalent)

**C = 0.01 μF for 50 μs de-emphasis (Europe)
= 0.015 μF for 75 μs de-emphasis (USA)



TL/H/7960–3

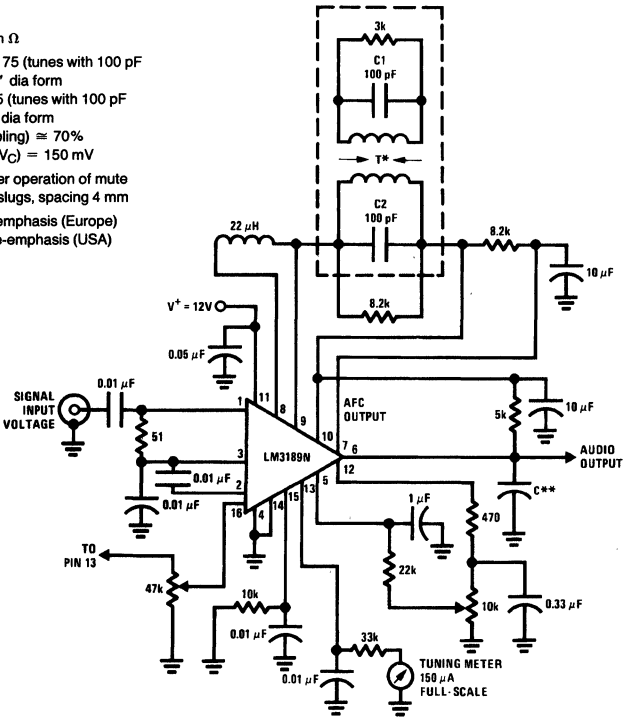
Test Circuit for LM3189N Using a Double-Tuned Detector Coil

All resistance values are in Ω

*T:PRI—Q_o(unloaded— ≅ 75 (tunes with 100 pF (C12)) 20t of 34e on 7/32" dia form
SEC—Q_o(unloaded) ≅ 75 (tunes with 100 pF (C2)) 20t of 34e on 7/32" dia form
kQ(percent of critical coupling) ≅ 70%
(adjusted for coil voltage (V_C) = 150 mV

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4 mm

**C = 0.01 μF for 50 μs de-emphasis (Europe)
= 0.015 μF for 75 μs de-emphasis (USA)

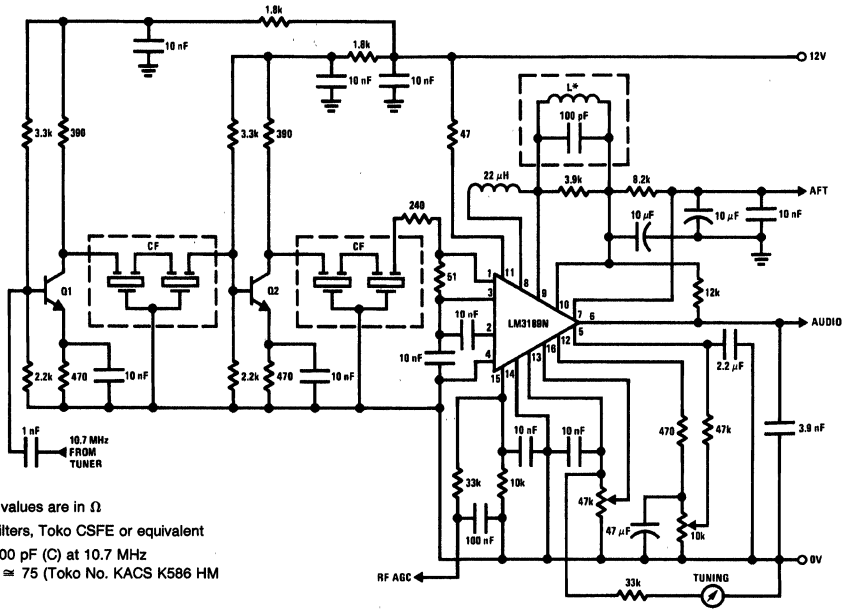


TL/H/7960–4

Complete FM IF System for High Quality Tuners

The circuit provides a complete FM IF system for a high quality receiver. Either one or two stages of amplification and bandpass filtering may be desired, depening on the receiver requirements. See graph for Typical Limiting and Noise Characteristics for each circuit configuration which can be compared to the LM3189N alone.

Complete FM IF System for High Quality Receivers



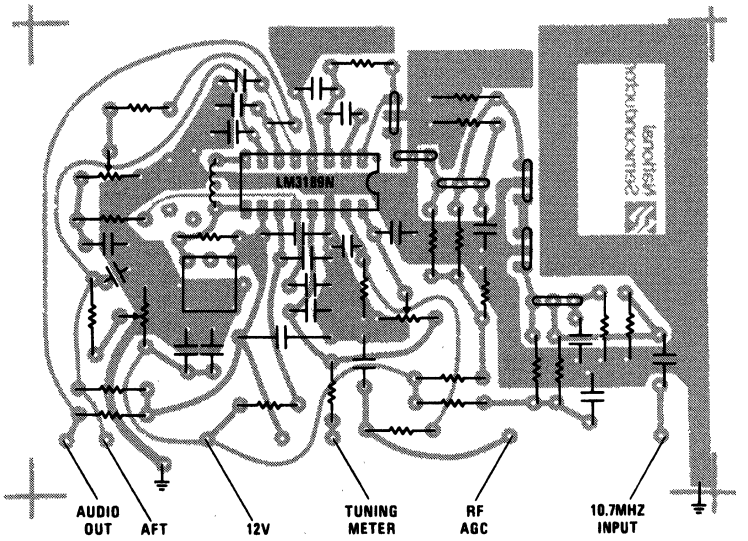
All resistance values are in Ω

CF: Ceramic filters, Toko CSFE or equivalent

*L tunes with 100 pF (C) at 10.7 MHz
Q_o(unloaded) ≅ 75 (Toko No. KACS K586 HM or equivalent)

TL/H/7960–5

Printed Circuit Board and Component Layout

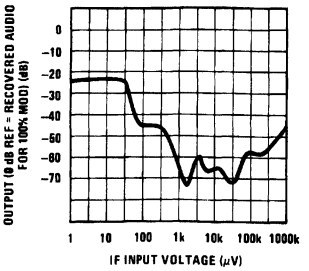


TL/H/7960–6

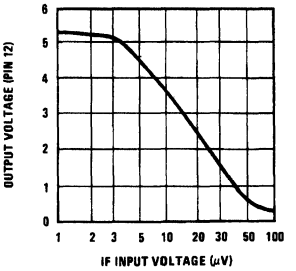
Component Side

Typical Performance Characteristics

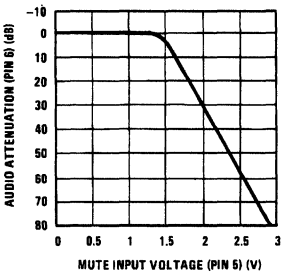
AM Rejection (30% Mod) vs IF Input Signal



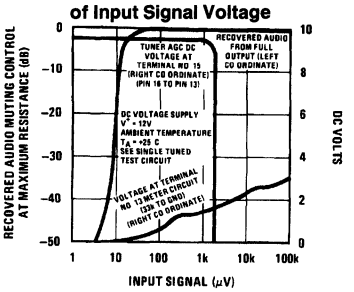
Mute Control Output (Pin 12) vs IF Input Signal



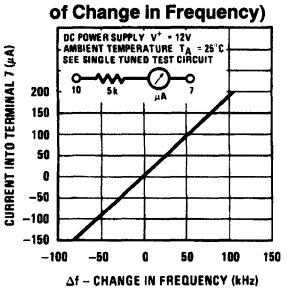
Typical Audio Attenuation (Pin 6) vs Mute Input Voltage (Pin 5)



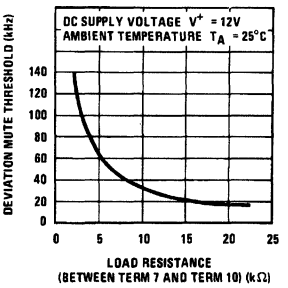
Muting Action, Tuner AGC, and Tuning Meter Output as a Function of Input Signal Voltage



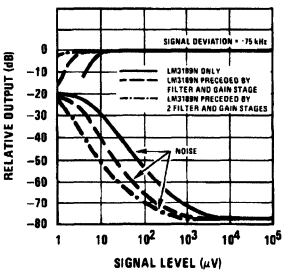
AFC Characteristics (Current at Term 7 as a Function of Change in Frequency)



Deviation Mute Threshold as a Function of Load Resistance (Between Term 7 and Term 10)

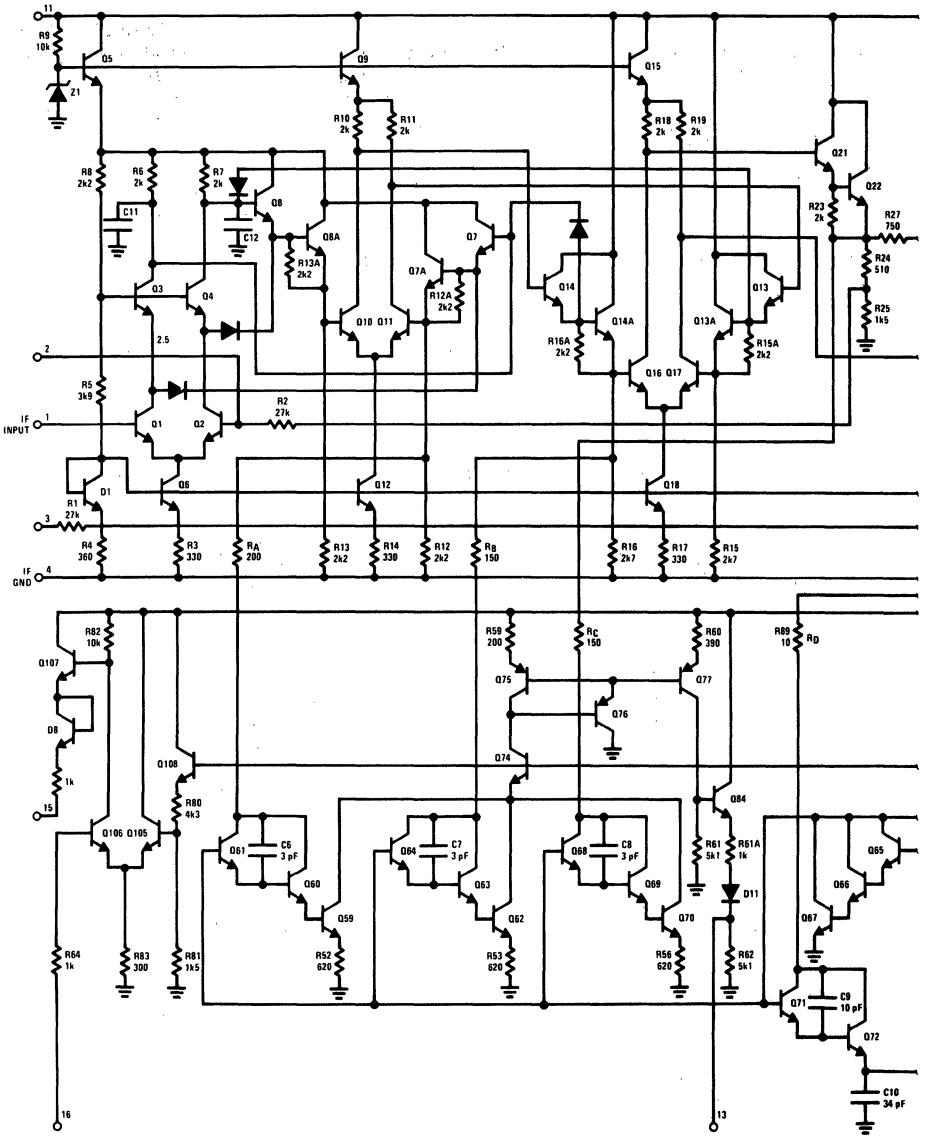


Typical Limiting and Noise Characteristics



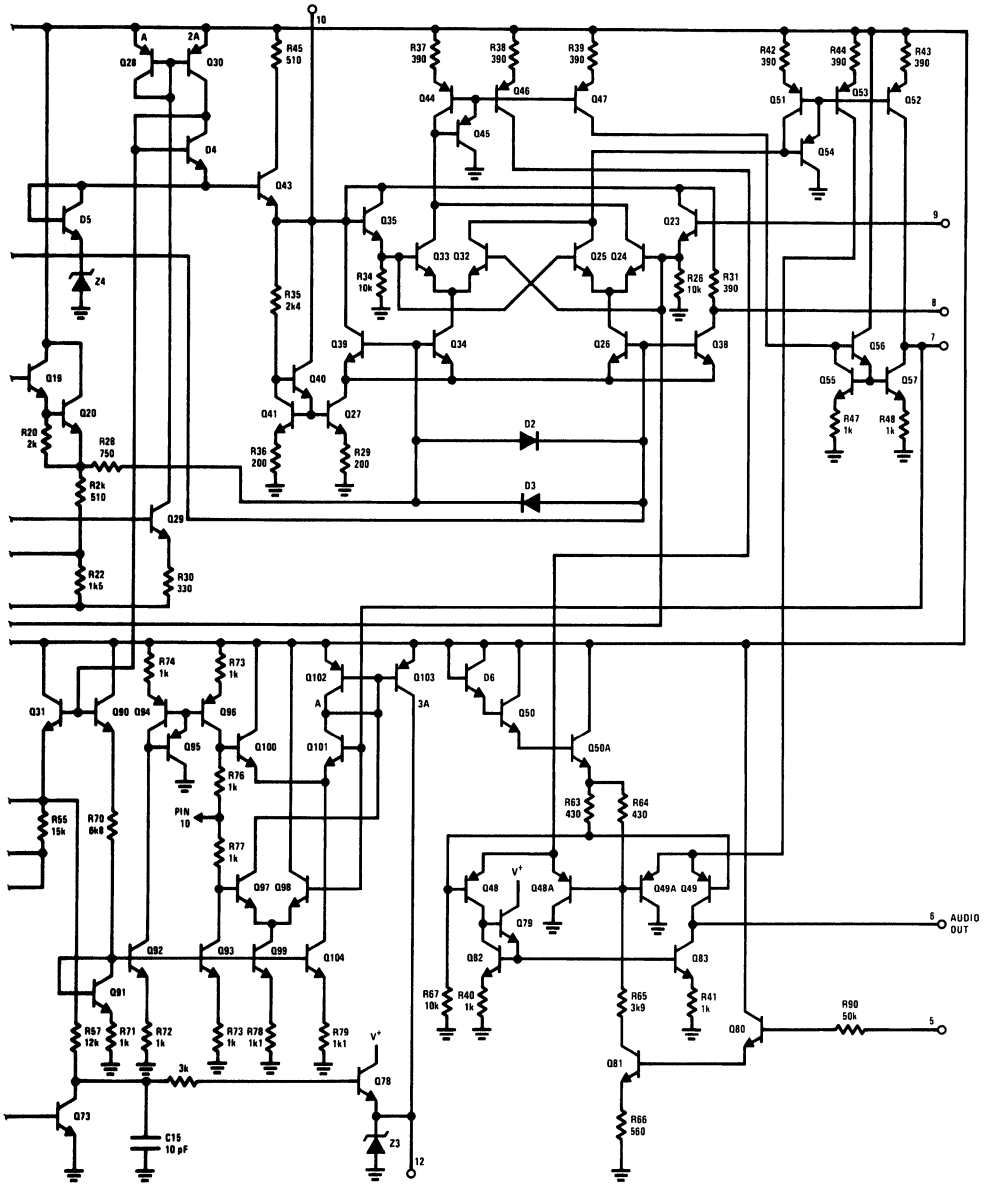
TL/H/7960–7

Schematic Diagram



TL/H/7960–8

Schematic Diagram (Continued)



TL/H/7960–9

National Semiconductor

LM3361A Low Voltage/Power Narrow Band FM IF System

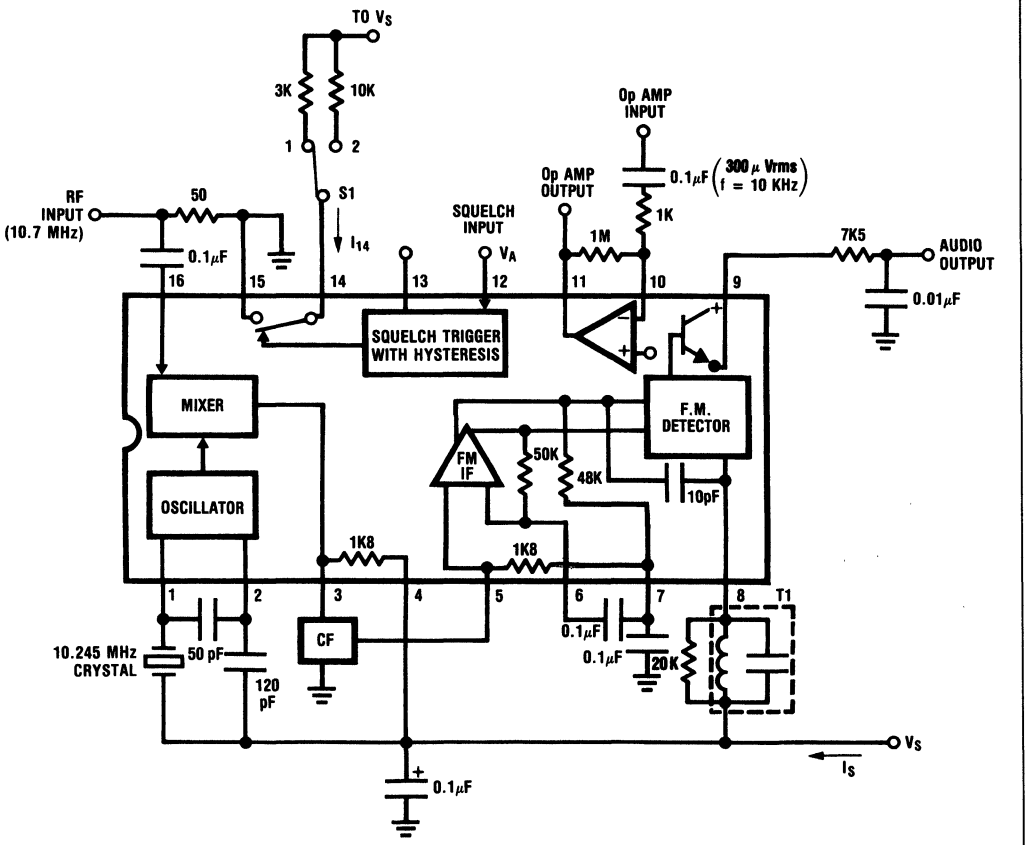
General Description

The LM3361A contains a complete narrow band FM demodulation system operable to less than 2V supply voltage. Blocks within the device include an oscillator, mixer, FM IF limiting amplifier, FM demodulator, op amp, scan control, and mute switch. The LM3361A is similar to the MC3361 with the following improvements: the LM3361A has higher voltage swing both at the op amp and audio outputs. It also has lower nominal drain current and a squelch circuit that draws significantly less current than the MC3361. Device pinout functions are identical with some slightly different operating characteristics.

Features

- Functions at low supply voltage (less than 2V)
- Highly sensitive (−3 dB limiting at 2.0 μV input typical)
- High audio output (increased 6 dB over MC3361)
- Low drain current (2.8 mA typ., V_{CC} = 3.6V)
- Minimal drain current increase when squelched
- Low external parts count

Block Diagram and Test Circuit



TL/H/5586–1

Order Number LM3661AM or LM3361AN
See NS Package Number M16A or N16E

T1-TOKO RMC-2A6597HM
CF-MURATA CFU 455E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Package Dissipation (Note 1)	1500 mW
Power Supply Voltage (V_S)	12 V
RF Input Voltage ($V_S > 3.6V$)	1 Vrms
Mute Function (pin 14)	−0.7 to 5 Vp
Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Parameters Guaranteed By Electrical Testing

(Test ckt., $T_A = 25°C$, $V_S = 3.6V$, $f_O = 10.7$ MHz, $\Delta f = \pm 3$ kHz, $f_{MOD} = 1$ kHz, 50Ω source)

Parameter	Measure	Min	Typ	Max	Units
Supply Voltage Range	V_S	2.0	3.6	9.0	V
Supply Current					
Squelch Off	I_S		2.8	5.0	mA
Squelch On	I_S		3.6	6.0	mA
RF Input for −3 dB Limiting	RF Input		2.0	6.0	μV
Recovered Audio at Audio Output	Audio Output	200	350		mV_{RMS}
Audio Out DC	V_9	1.2	1.5	1.8	V_{DC}
Op Amp Gain	V_{11}/V_{IN}	40	55		dB
Op Amp Output DC	V_{10}	0.4	0.7		V_{DC}
Op Amp Input Bias Current	$(V_{10} - V_{11})/1M\Omega$		20	75	nA
Scan Voltage					
Pin 12 high (2V)	V_{13}		0	0.5	V_{DC}
Pin 12 Low (0V)	V_{13}	3.0	3.4		V_{DC}
Mute Switch Impedance, Pin 12 = 0V Switch S1 from pos.1 to pos.2	$\Delta V_{14}/\Delta I_{14}$		15	30	Ω

Design Parameters Not Tested or Guaranteed

	Typ	
Mixer Conversion Gain (Note 2)	46	V/V
Mixer Input Resistance	3.6	kΩ
Mixer Input Capacitance	2.2	pF
Detector Output Impedance	500	Ω
Squelch Hysterisis	100	mV
Mute Off Impedance (measure pin 14 with pin 12 @ 2V)	10	MΩ
Squelch Threshold	0.65	V_{DC}
Detector Center Frequency Slope	0.15	V/kHz

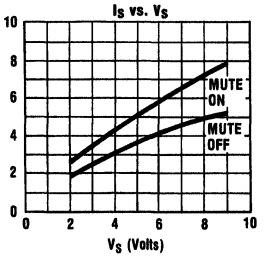
Note 1. For operation above 25°C ambient temperature, the device must be derated based on 150°C maximum junction temperature and a thermal resistance θ_{JA} of 80°C/W.

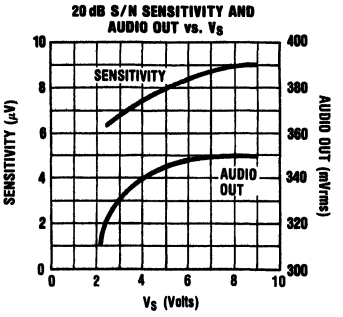
Note 2. Mixer gain is supply dependent and effects overall sensitivity accordingly (See Typical Performance Characteristics).

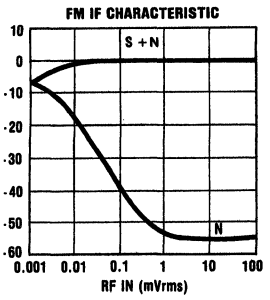
Coils:
Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

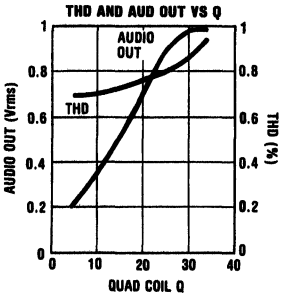
Filters:
Murata
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

Typical Performance Characteristics (Test Circuits)

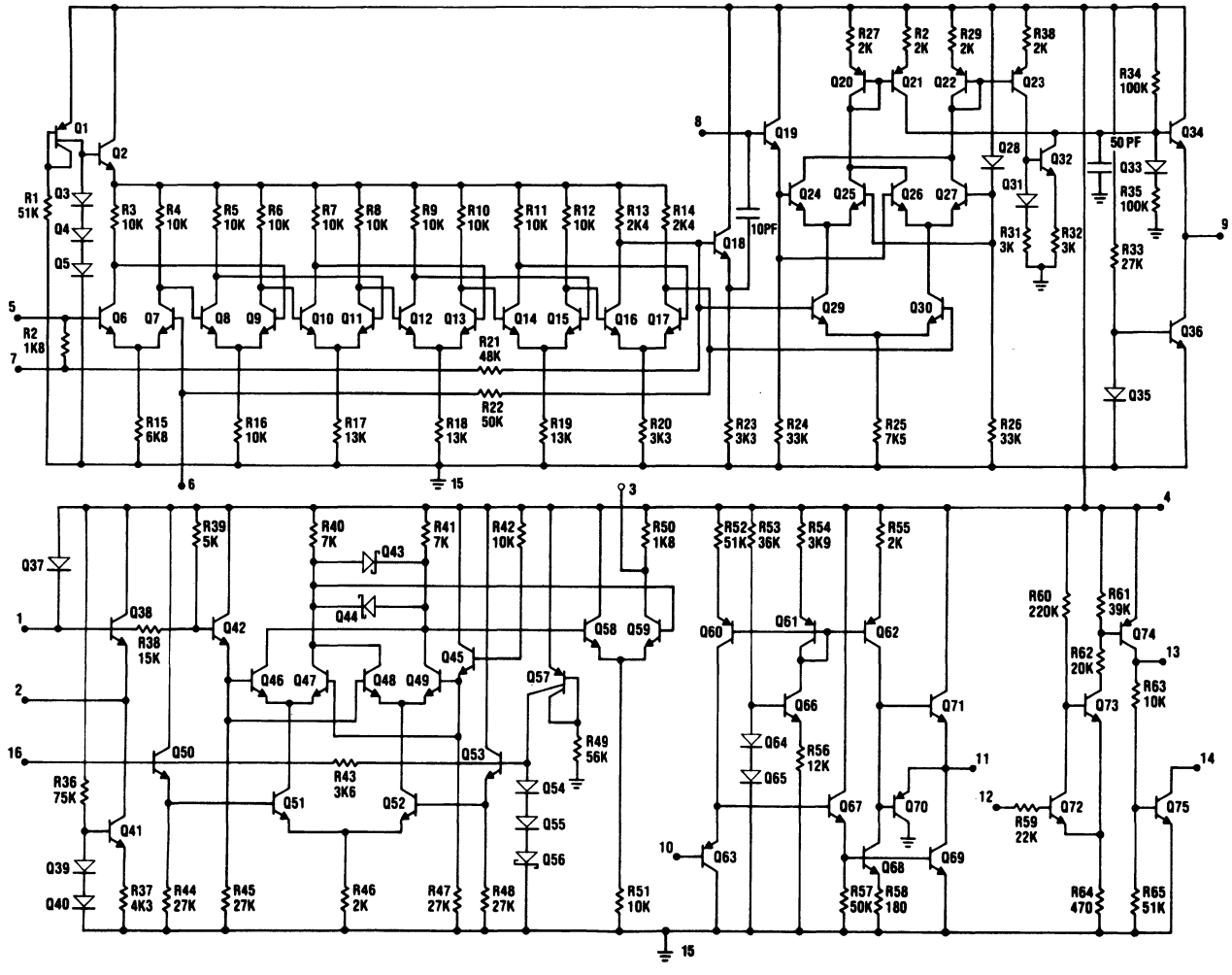








TL/H/5586–2


R1 51K
R2 1K8
R3 10K
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
R10 10K
R11 10K
R12 10K
R13 2K4
R14 2K4
R15 6K8
R16 10K
R17 13K
R18 13K
R19 13K
R20 3K3
R21 48K
R22 50K
R23 3K3
R24 33K
R25 7K5
R26 33K
R27 2K
R28 2K
R29 2K
R31 3K
R32 3K
R33 27K
R34 100K
R35 100K
R36 75K
R37 4K3
R38 15K
R39 5K
R40 7K
R41 7K
R42 10K
R43 3K6
R44 27K
R45 27K
R46 2K
R47 27K
R48 27K
R49 56K
R50 1K8
R51 10K
R52 51K
R53 36K
R54 3K9
R55 2K
R56 12K
R57 50K
R58 180
R59 22K
R60 220K
R61 39K
R62 20K
R63 10K
R64 470
R65 51K
10PF
50 PF
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q47 Q48 Q49 Q50 Q51 Q52 Q53 Q54 Q55 Q56 Q57 Q58 Q59 Q60 Q61 Q62 Q63 Q64 Q65 Q66 Q67 Q68 Q69 Q70 Q71 Q72 Q73 Q74 Q75
1
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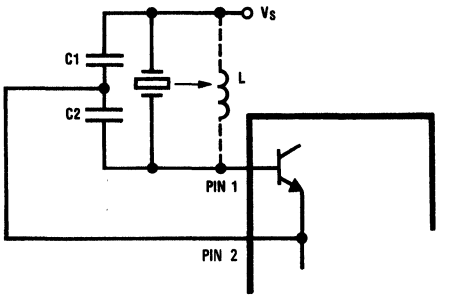
16

TL/H/5586-3

Applications Information (See Internal Schematic)

OSCILLATOR

The Colpitts type oscillator is internally biased with a regulated current source which assures proper operation over a wide supply range. The collector, base, and emitter terminals are at pins 4, 1, and 2 respectively. The crystal, which is used in the parallel resonant mode, may be replaced with an appropriate inductor if the application does not require the stability of a crystal oscillator. In this case, the resonant frequency will be determined by the inductor in parallel with the series combination of C1 and C2.



TL/H/5586–4

so $Ct = (C1)(C2)/(C1 + C2)$

and $f_O = .159/\sqrt{L(Ct)}$

MIXER

The mixer is double balanced to reduce spurious responses. The upper pairs are switched by the oscillator while the RF input is applied to the lower pair (pin 16). R43 sets the mixer input impedance at 3.6 kΩ. The mixer output impedance of 1.8 kΩ will properly match the input impedance of a ceramic filter which is used as a bandpass filter coupling the mixer output to the IF limiting amplifier.

IF LIMITER

The IF amplifier consists of six differential gain stages, with the input impedance set by R2 at 1.8 kΩ to properly terminate the ceramic filter driving the IF. The IF alone (without mixer) has a −3 dB limiting sensitivity of approximately 50 μV. The system bandwidth is limited to about 5 MHz due to high impedances in the IF which are necessary to meet low power requirements. The IF output is connected to the external quad coil at pin 8 via an internal 10 pF capacitor.

FM DEMOD AUDIO OUT

A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple effects on the audio output. Increasing the Q increases output level but because of nonlinearities in the tank phase characteristic, also increases distortion (see Typical Performance Characteristics). For proper operation, the voltage swing on pin 8 should be adequate to drive the upper rank of the multiplier into switching (about 100 mVrms). This voltage level is dependent on the internal 10 pF capacitor and the tank R_p voltage divider network. After detection and de-emphasis, the audio output at pin 9 is buffered by an emitter follower.

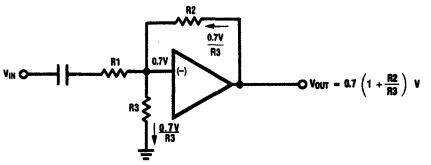
OP AMP

The op amp inverting input (pin 10) which is internally referenced to 0.7V, receives dc bias from the output at pin 11 through the external feedback network. Because of the low D.C. bias, maximum swing on the op amp output with 10% distortion is 500 mVrms. This can be increased when operating on supplies over 2.3V by adding a resistor from the op amp input to ground which raises the quiescent D.C. at the output allowing more swing (see figure below for selection of added resistor). The op amp is normally utilized as either a bandpass filter to extract a specific frequency from the audio output, such as a ring or dial tone, or as a high pass filter to detect noise due to no input at the mixer. The latter condition will generate a signal at the op amp output, which when applied to pin 12 can mute the external audio amp.

For max swing: $V_{OUT} = (V_S - V_{BE})/2$ (from internal circuit)

$$\text{so } (V_S - V_{BE})/2 = 0.7\left(1 + \frac{R2}{R3}\right)$$

$$\text{therefore } \frac{R2}{R3} = \left(\frac{V_S - V_{BE}}{1.4}\right) - 1$$



TL/H/5586–5

Increasing OP Amp Swing

SQUELCH TRIGGER CIRCUIT

The squelch trigger circuit is configured such that a low bias on the input (pin 12) will force pin 13 high (200 mV below supply), where it can support at least a 1 mA load, and pin 14 to be a low impedance, typically 15Ω to ground. Connecting pin 14 to a high impedance ground reference point in the audio path between pin 9 and the audio amp will mute the audio output. Pulling pin 12 above mute threshold (0.65V) will force pin 13 to an impedance of about 60 kΩ to ground and pin 14 will be an open circuit. There is 100 mV of hysterisis at pin 12 which effectively prevents jitter.

Section 3

Video Circuits

Section 3 Contents

National Semiconductor

Video
Definition of Terms

Aspect Ratio: The ratio of picture width to picture height. For the NTSC system this is 4:3.

Back Porch: The section of the composite video signal between the trailing edge of the line (horizontal) sync pulse and the end of the blanking pulse period (when picture information begins). For a monochrome signal the back porch is simply at the blanking level. For a color signal, the color burst is added within this section.

Black Level: The DC voltage level in the picture signal which corresponds to beam cut-off on the display tube. It can be at the blanking level (given by the back porch) or slightly higher (7.5% to 10% of the peak white signal above the blanking level).

Blacker-than-Black: The amplitude region in the composite video signal that extends below the reference black level in the direction of the synchronizing pulses.

Blanking: A portion of the composite video signal whose instantaneous amplitude makes the vertical and horizontal scan retrace not visible on the display tube.

Blanking Level: The level of the front and back porches of the composite video signal.

Blanking Period: The period in the composite video signal where the level is reduced to the blanking level, below which the display electron beam is cut-off. This allows non-visible retrace of the beam from the right side of the display to the left side at the end of each scan line (horizontal blanking) and non-visible return of the electron beam from the bottom of the display to the top. Horizontal blanking occurs for approximately 11 μs between each scan line and vertical blanking for 1.2 ms between each field.

Blooming: Defocussing of the picture in regions where the brightness is too high.

Breezeway: The section in the signal blanking period between the end of the sync pulse and the start of the color burst.

C.C.I.R.: International Radio Consultative Committee—a worldwide standards organization.

Chrominance Signal: That part of the NTSC signal that contains the color information.

Clamping: A process that established a fixed DC voltage level for the picture signal. This is important for proper RF modulation and for maintaining the correct picture black level.

Color: An attribute of an object being scanned that distinguishes it from other objects, apart from shape, texture, and brightness. In television systems the color of an object is further subdivided into hue (tint) and saturation. The hue or tint refers to the dominant wavelength of a spectral color, i.e., light red is the same hue as deep red and dark red. Deep red has more vividness or saturation (less white), whereas dark red has less brightness. Similar terms are used to describe non-spectral colors (a mixture of hues).

Color Burst: Normally refers to approximately 9 cycles of the 3.58 MHz subcarrier superimposed on the back porch of the composite video signal. The phase of this burst establishes the reference color phase for tint or hue, and the amplitude provides a reference for the color saturation level.

Color Subcarrier: A subcarrier at 3.579545 MHz (NTSC) whose modulation sidebands are added to a monochrome video signal to convey the color information. Similar subcarriers are used for SECAM and PAL.

Composite Video Signal: The complete video signal. For monochrome, it consists of blanking and synchronizing signals, with a picture signal representing the scene brightness. For color, an additional subcarrier is added for color synchronization and picture color content.

Compression: An undesired decrease in amplitude of one portion of the composite video signal relative to another portion.

Contrast: The range of dark and light values in a picture.

Cross-talk: An undesired signal interfering with a desired signal.

Definition: See resolution.

Differential Gain: The amplitude change in the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level. This is the result of system non-linearities and is measured in percent change.

Differential Phase: The phase change, measured in degrees, of the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level.

Equalizing Pulses: Pulses of one half the width of the line (horizontal) sync pulses, transmitted at twice the line rate for the three line periods before and after the field (vertical) sync pulse. They are used to help the vertical sync system of the receiver accommodate the half line difference in the number of scan lines on successive fields.

Field: One half of a complete picture interval. A field will contain either all the odd numbered scanning lines or all the even numbered scanning lines in the picture.

Field Frequency: The rate at which a complete field is scanned. For NTSC color signals this is nominally 59.94 Hz.

Fly-back: See Horizontal Retrace.

Frame: A complete picture consisting of two interlocking fields.

Frame Frequency: The rate at which a complete frame is scanned. In the U.S. this is nominally 30 frames or pictures per second.

Front Porch: The section of the composite video signal between the end of the picture information on a scan line (start of blanking) and the start of the line synchronization pulse.

Horizontal Blanking: The blanking signal at the end of each scan line that prevents the retrace of the display tube electron beam from being visible.

Horizontal Retrace: The rapid return of the scanning electron beam from the right side of the raster to the left side.

Horizontal Hum Bars: Relatively broad horizontal bars drifting slowly up the screen as a result of interference from the 60 Hz main frequency.

Hue (Tint): Describes the color that is being represented on the screen, i.e., red, blue, magenta, green, orange, etc.

Interlace: A scanning process in which each adjacent line belongs to the alternate field.

I.R.E.: Institute of Radio Engineers. Now combined with the AIEE to form the IEEE.

I.R.E. Scale: An oscilloscope scale calibrated for composite video and divided vertically into 140 units. The picture signal occupies the range from 0 to 100 with syncs in the range 0 to −40.

Luminance: The monochrome or brightness part of the color signal, composed of specific proportions of the three primary colors, red, blue, and green.

N.T.S.C.: National Television System Committee, used in reference to the system adopted for color television broadcasting in the U.S. at the end of 1953.

Noise: In a television picture, 'noise' refers to random interference producing a salt and pepper pattern over the picture. Heavy noise totally obscuring the picture is called "snow".

Overshoot: An (excessive) response to a unidirectional signal change. Overshoot is often used deliberately to enhance the luminance portion of a signal.

Pairing: A partial or complete failure of interlace in which scan lines of alternate fields fall in pairs, one on top of the other.

Pedestal Level: See Blanking Level.

Percentage Sync:

Video: The ratio in percent of the amplitude of the synchronizing pulse to the peak amplitude of the picture signal between blanking and reference white level. For a properly constituted composite video signal this is 40%.

RF: The ratio is a percent of the amplitude of the synchronizing pulse to the peak amplitude of the modulated RF signal. For correct modulation this is 25%.

P.A.L.: Phase Alternation Line. A variation of the NTSC system involving phase reversal of one of the color difference signals on a line by line basis, introduced into the U.K. and Germany in 1967.

Picture Signal: That portion of the composite video signal which is above the blanking level and contains the picture information.

Pre-emphasis: An increase in the level of a band of frequency components with respect to the remainder of the signal. For U.S. television, the audio signal is increased at a 6 db/octave rate above 2.1 kHz.

Raster: The area on the face of the display tube that is scanned by the electron beam. This is not always entirely visible since commercial receivers employ overscan so that the edges of the raster are hidden by the faceplate.

Reference Signals: See V.I.T.S. and V.I.R.S.

Resolution (Horizontal): The amount of resolvable detail in the horizontal direction of the picture. This depends on the high frequency and phase response of the transmission system and the receiver.

Resolution (Vertical): The amount of resolvable detail in the vertical direction of the picture. This depends primarily on the number of scan lines that are used and secondarily on the size (shape) of the electron scanning beam.

Saturation (Color): The amplitude of the chrominance signal. Increased saturation means increased chrominance signal level. Visibly, this refers to a color increasing from pale or pastel to deep.

S.E.C.A.M.: Sequential Couleur Avec Memoire. The color broadcasting system used predominantly in France which utilizes sequential transmission of the color difference signals, which are FM modulated on two separate subcarriers (1967).

Setup: The difference in level between the blanking level and the reference black level expressed as a percent of the reference white level.

Smear: Smear describes a picture condition where objects appear extended in the horizontal direction producing an ill-defined, blurry picture. This often occurs when the receiver is tuned slightly above the proper pix carrier frequency.

Sync: Abbreviation for synchronizing or synchronization.

Sync Level: The level of the synchronizing pulse tips.

Vertical Blanking: The blanking signal at the end of each field starting three lines before the vertical sync pulse.

Vertical Retrace: The return of the electron beam from the bottom of the display to the top after a complete field has been scanned.

V.I.R.S.: Vertical Interval Reference Signal. A quality control signal added to a horizontal scan line during the vertical blanking period. It is used to provide a chrominance, luminance and black level reference.

V.I.T.S.: Vertical Interval Test Signals. A series of test signals that are added to horizontal lines during the vertical blanking for in-service testing of the transmission equipment. They can be deleted or added at various points in the transmission link, unlike the VIRS, which is added at program origination and stays with the program material.

Vestigal Sideband Transmission: A broadcast transmission technique wherein only one side band of an amplitude modulated carrier is fully transmitted with the other sideband (usually lower) truncated.

Video: The visible portion of the transmitted signal representing the picture.

National Semiconductor

Video Circuits Selection Guide

Video Amplifiers

	Bandwidth	Gain	Package	Supply Voltage	Comments
LM1201	200 MHz	4–10	16 Pin DIP	+12V	Single Amplifier with Black Level and Contrast Control
LM1203	70 MHz	4–10	28 Pin DIP	+12V	Triple Amplifier System with Black Level and Balanced Contrast Control
LM1204	150 MHz	1–10	44 Pin PLCC	12V	Triple Amplifier System with DC Controls and Sync Detector. Provides Blanking at CRT Cathode.
LM2416	45 MHz	−13	11 Pin TO220	80V	• Triple CRT Driver • 50 V_{PP} Output Swing with 10 ns t_r/t_f
LM2418	30 MHz	−19	11 Pin TO220	90V	• Triple CRT Driver • 50 V_{PP} Output Swing with 10 ns t_r/t_f

Video Timing

	Function	Package	Supply Voltage	Comments
LM1391	Low-Freq PLL	8 Pin DIP	Internally Regulated	For Horizontal Section
LM1881	Sync Separator	8 Pin DIP 8 Pin SO	5V–12V	Outputs Provided: Composite Sync Vertical Burst Gate Odd/Even Field
LM1882	Sync Generator	20 Pin DIP 20 Pin LCC	5V	130 MHz Max Clock Frequency. Both Interlaced and Non-Interlaced Formats. Control Via Register Programming with NTSC Default Values.

Video Circuits (Continued)

Video IFs

	Application	Package	Comments
LM1211	Broadband Demodulator Date or Video Recovery from LANs, Other Comm. Systems	20 Pin DIP	Operating Range 20 MHz–80 MHz Quasi-Synchronous Detector 25 MHz Output Amplifier
LM1823	Video IF Signal Processing	28 Pin DIP	Operating Range 20 MHz–70 MHz Synchronous Detector using PLL 9 MHz Output Amplifier

Other Video Products

	Function	Package	Supply Voltage	Comments
LM1044	Video Switch	24 Pin DIP	8V–16V	• DC Switch between 3 Composite Video Channels or 2 RGB Channels • 60 dB Channel Separation
LH4266	SPDT rf Switch	24 Pin Hermetic	±8V–±18V	• DC to 150 MHz Switch • Break-before-Make • TTL Control Input • Low Insertion Loss 1.5 dB (50Ω)

National Semiconductor

LH4266 SPDT RF Switch

General Description

The LH4266 is a single pole double throw switch intended for RF and video switching applications. The device has a TTL compatible control signal and can be configured as a multiplexer or demultiplexer which will fulfill most switching needs.

The non-selected input may be terminated to provide a match to the source driving that port and prevent spurious oscillations that might occur from an unterminated transmission line.

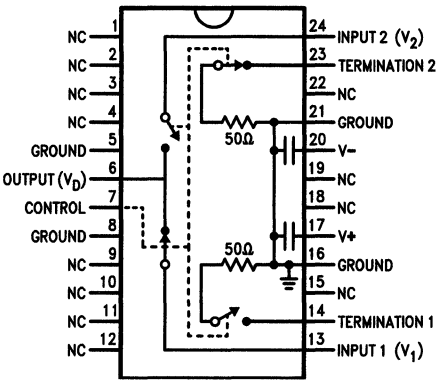
Features

- Single pole double throw (SPDT)
- DC to 150 MHz
- +27.5 dBm maximum signal (50Ω)
- Low insertion loss 1.5 dB (50Ω)
- Non-selected input terminated
- Break before make
- TTL compatible control signal
- Internal power supply bypassing

Applications

- ATE pin driver switch
- Computer RF switch
- Tester switching matrix
- RF voltage multiplexer

Connection Diagram



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Top View

Note: NC means no internal connection.

Order Number LH4266CD or LH4266D
See NS Package Number D24I

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_S)	±18V
Power Dissipation, (P_D)(See Curve)	2.0W
Input Signal, (V_{IN})	$\pm V_S$
ESD	TBD
Control Voltage, (V_C)	V_S-2V
Storage Temperature Range, (T_{STG})	−65°C to +150°C
Operating Temperature Range, (T_A)	
LH4266CD	−25°C to +85°C
LH4266D	−55°C to +125°C
Lead Temperature (T_L) (Soldering, < 10 seconds)	300°C

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	LH4266C			Units (Max. unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
I_S	Supply Current	V^+	4.8	7		mA
		V^-	−47	−60		
V_{TH}	Logic High		1.5	2.0		V (Min)
V_{TL}	Logic Low		0.5	0.8		V
I_{IN}	Control Input Current	V_{IN} = 0V to 5V	2.0	3.0		μA
R_{ON}	On Resistance	$V_1 = V_2$ = 0V, I_D = 1 mA	15	18		Ω
Δ_r	Resistance Match			4		
	Leakage Current	$V_{1-2} = V_D$ = ±5V, Switch On, Note 4		100		nA
		$V_{1-2} = V_D$ = ±5V, Switch Off, Note 4		100		
		$V_{1-2} = V_D$ = ±5V, Input to Input		100		

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 50Ω, T_A = 25°C unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4266			Units (Max. unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
I_S	Supply Current	V^+	4.8	**7**		mA
		V^-	−47	**−60**		
V_{TH}	Logic High		1.5	**1.8**		V (Min)
V_{TL}	Logic Low		0.5	**0.8**		V
I_{IN}	Control Input Current	V_{IN} = 0V to 5V	2.0	**3.0**		μA
R_{ON}	On Resistance	$V_1 = V_2$ = 0V, I_D = 1 mA	15		**30**	Ω
Δ_r	Resistance Match			**6**		
	Leakage Current	$V_{1-2} = V_D$ = ±5V, Switch On, Note 4		**1**		μA
		$V_{1-2} = V_D$ = ±5V, Switch Off, Note 4		**1**		
		$V_{1-2} = V_D$ = ±5V, Input to Input		**1**		

AC Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$, $T_A = 25°C$, unless otherwise noted.

Symbol	Parameter	Conditions	LH4266C/LH4266			Units (Max. unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
	Insertion Loss	10 MHz	1.0	1.5		dB
		100 MHz	2.0	2.3		
	Isolation Input to Output See Test Circuit	10 MHz	90	75		dB (Min)
		100 MHz	75	60		
	Isolation Input1 to Input2	10 MHz	90			
		100 MHz	60			
	Distortion	$V_{OUT} = 10\ V_{p-p}$	1.0			%
V_{SWR}		Unselected Input	1.5 : 1			Ratio
T_{SW}	Switching Speed		500			ns

Note 1: Boldface limits are guaranteed over full temperature range.

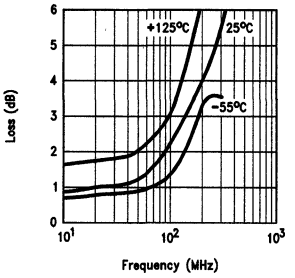
Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality level.

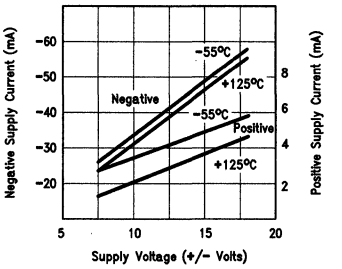
Note 4: Leakage current is measured with signal applied to each input. See test circuit.

Typical Performance Characteristics

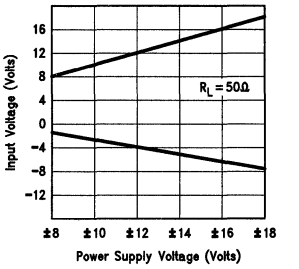
Insertion Loss



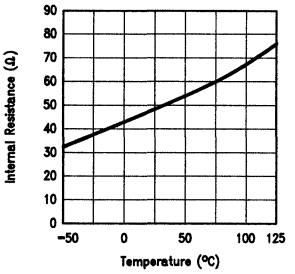
Supply Current



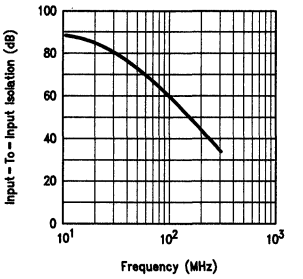
Allowable Input Signal



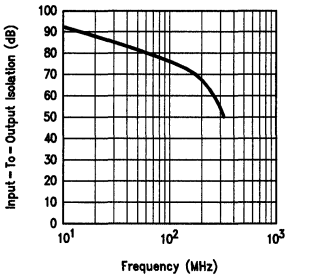
Internal Termination Resistance



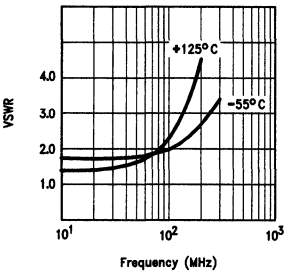
Input to Input Isolation



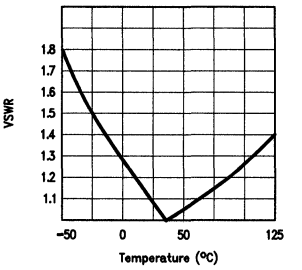
Input to Output Isolation



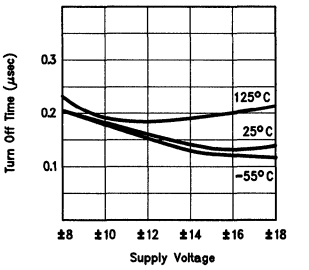
Termination VSWR



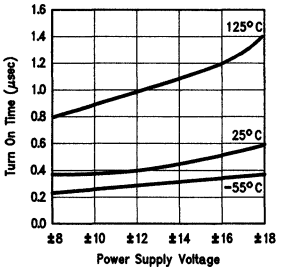
Termination VSWR



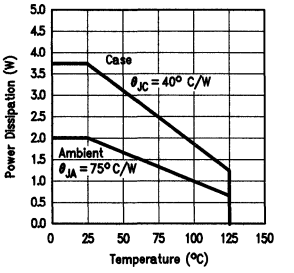
Turn Off Time



Turn On Time



Maximum Power Dissipation



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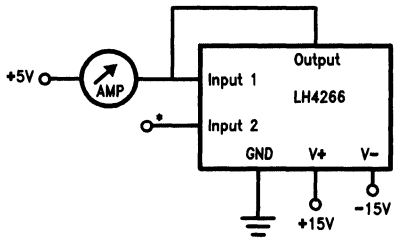
Leakage Current Equivalent Test Circuit



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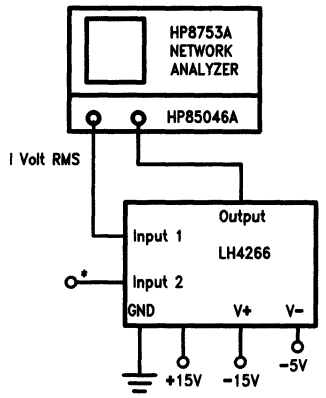
*Same test for Input 2.

Test Circuit for Isolation Input to Output



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Applications Information, LH4266

The LH4266 uses hybrid technology to give increased circuit performance. In order to maintain its excellent cross talk and feedthru specifications, proper RF grounding and shielding should be incorporated in the printed circuit board layout. For example; the input traces should not run next to output traces and grounds should be provided by a ground plane under the device (see *Figure 1a, b* for suggested PC board layout).

The device contains two internal termination resistors and switches. If termination of the non-selected input is desired, connect the termination pin to the adjacement input pin and the deselected input will be terminated with approximately 50Ω.

Note that the internal termination resistors are internally connected to the device's ground pin. Thus if the internal termination resistors are used then the input ground planes should remain isolated from the output ground plane (as in *Figure 1*) so as not to form a ground loop. When using external termination resistors at the input, the resistors should be connected to their respective ground planes, and, pin 16 should be tied to input1's ground plane while pin 21 is tied to input2's ground plane. Since pins 16 and 21 are internally connected to the device ground pin, the input and output ground planes should remain isolated. LH4266's power supplies are internally bypassed with high frequency capacitors for ease of use. Thus for high frequency applications bypass capacitors are not required, however, at low frequencies (10 MHz or less) a 4.7 μF bypass capacitor for each supply is recommended.

Due to the unique design of the LH4266 it can easily be used as a multiplexer or demultiplexer. In fact several units can be connected to give a 1 to 4 multiplexer or a 4 to 1 demultiplexer by simply adding the required units as shown in *Figures 2* to *5*.

The action of the switches can be seen in the following truth table.

LH4266 Truth Table

Control	Pin 24 Input 2	Pin 13 Input 1
Low = 0	On	Off
High = 1	Off	On

Double Sided Board, Bottom Side

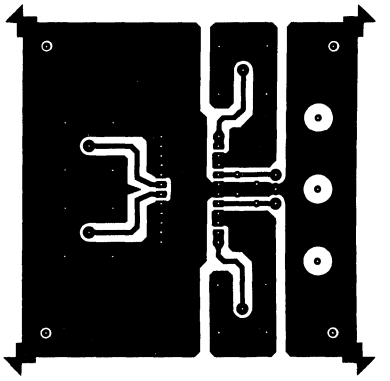

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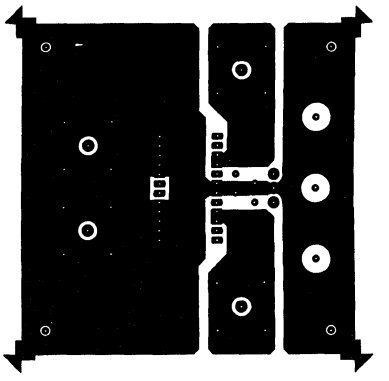
FIGURE 1a. LH4266, Recommended Printed Circuit Board Layout

Double Sided Board, Top Side



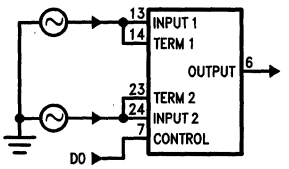
TL/K/9404–13

FIGURE 1b. LH4266, Recommended Printed Circuit Board Layout

Video Switch

The LH4266 is ideally suited for video signal switching applications. *Figure 7* shows how the LH4266 may be used to select one of two video input signals while the LH4006 buffer allows driving four doubly terminated 75Ω cables. R1 biases the buffer's output to 0V and prevents the output stage from saturating when both switches are momentarily open. Meanwhile, R2 eliminates the offset voltage caused by the buffer's input bias current, and, a 10 pF capacitor across R2 prevents undesirable oscillations caused by stray capacitance at the buffers's inverting input. The circuit is capable of producing ±1V at the terminated ends of the 75Ω cables. To maintain LH4266's excellent input to output isolation and input to input crosstalk specifications, extreme care should be exercised while laying out the printed circuit board. From *Figure 1*'s recommended printed circuit board layout it can be observed that there are three separate ground planes. Each input signal should be referenced to it's respective ground plane while the output signal, control signal and power supplies are referenced to the output ground plane. Note that LH4266's internal termination resistors are internally connected to the device's ground pin. Consequently, if LH4266's internal termination resistors are used then the input and output ground planes should remain isolated (as in *Figure 1*) so as to prevent a ground loop from occurring. When an external termination resistor is used as in *Figure 7*, the resistor should be connected to its respective ground plane, while pin 16 is tied to input1's ground plane and pin 21 is tied to input2's ground plane. Moreover, all ground planes should remain isolated because pins 16 and 21 are internally connected to the device ground pin.

Application Circuits, LH4266



TL/K/9404-3

FIGURE 2. 2 to 1 Multiplexer

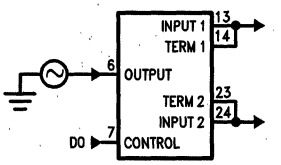


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FIGURE 3. 1 to 2 Demultiplexer

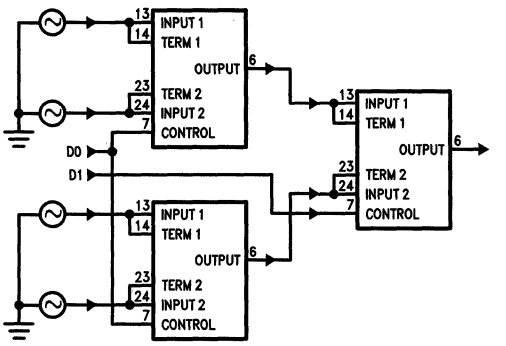

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FIGURE 4. 4 to 1 Multiplexer

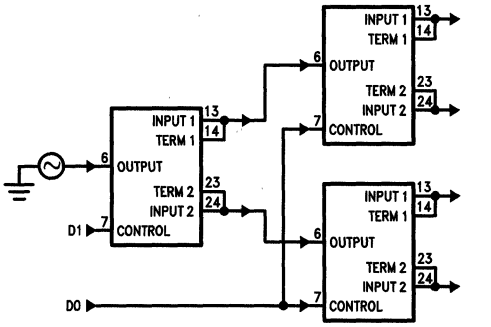

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FIGURE 5. 1 to 4 Demultiplexer

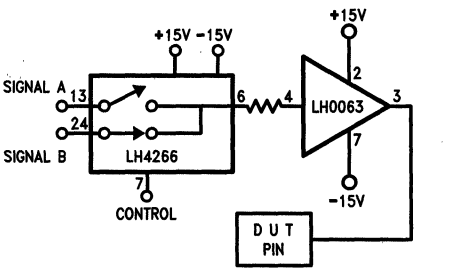

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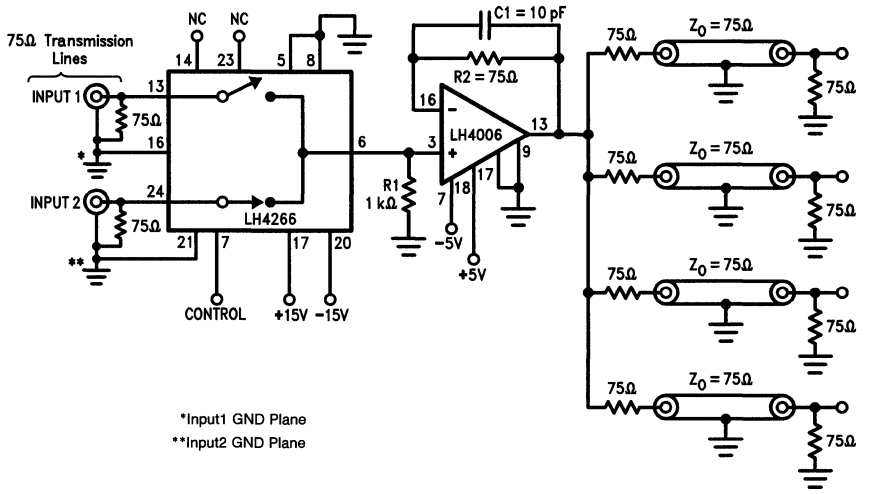
FIGURE 6. ATE Pin Driver Switch



TL/K/9404–10

FIGURE 7. Video Switch

National Semiconductor

LM1044 Analog Video Switch

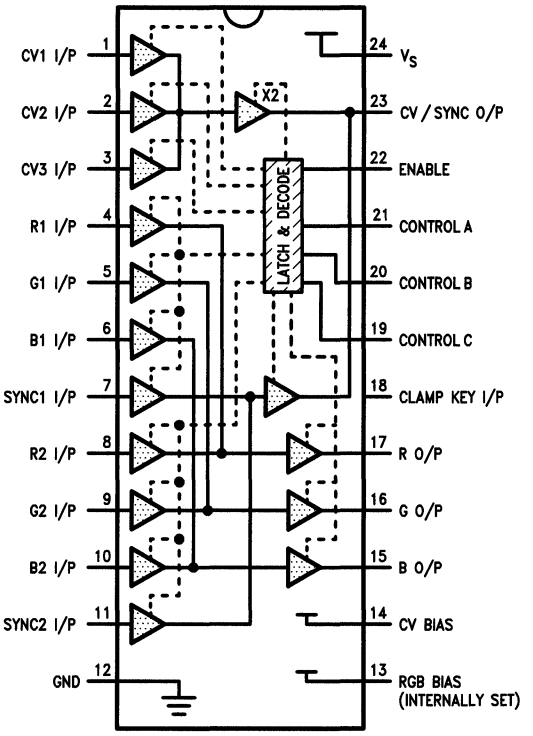
General Description

Primarily intended for, but not restricted to, the switching of video signals, the LM1044 is a monolithic DC controlled analog switch with buffered outputs, allowing the selection of three 5 MHz bandwidth, 6 dB gain channels, or two RGB + Sync, 30 MHz bandwidth, 0 dB gain channels. Channel selection is achieved via latched, TTL compatible, logic inputs which may be controlled by microprocessor derived signals. The device is supplied in a 24 pin dual in line plastic package.

Features

- Wide RGB bandwidth, typically 30 MHz
- High signal to noise ratio, typically 60 dB
- Excellent channel isolation typically −60 dB @ 5 MHz
- High RGB output currents; typically 4 mA peak
- RGB channels may be DC restored or clamped
- Logically compatible with the LM1038 stereo audio switch IC

Block Diagram



TL/H/9252–1

Order Number LM1044N
See NS Package Number N24A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_S)	17V
Package Dissipation at T_A = 25°C (Note 8)	2.0W
Voltage at Control and Signal Inputs	−0.2V to Vs +0.2V
Output Current, I_{23}, I_{17}, I_{16}, I_{15}	10 mA
ESD Susceptibility (Note 5)	2000V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C
Junction Temperature	150°C

Electrical Characteristics V_S = 12V, R_L = 600Ω, C_L = 20 pF, T_A = 25°C unless otherwise stated

Parameter	Conditions	Test Limit (Note 6)		Design Limit (Note 7)			Units
		Min	Max	Min	Typ	Max	
Supply Voltage, Vs		8	16	8	12	16	V
Supply Current	RGB1 Channel Selected with No Input Signals Applied		60		42	60	mA
Control Inputs Logic High Level Control Inputs Logic Low Level	Control Inputs A, B, C and Enable Input	2.0	 0.8	2.0		 0.8	V V
Enable Input Current, Pin 22	0V to Vs				2	10	μA
Control Input Current	0V Logic Level 5V Logic Level				20 250	50 500	μA μA
Enable Pulse Width				5			μs
Channel Select Time					5	7	μs
COMPOSITE VIDEO CHANNELS	Inputs—Pins 1, 2, 3 Output—Pin 23						
Maximum Input Voltage Swing	For Output THD = 1% @ 1 kHz			1.2			V_{p-p}
Input Impedance				1.2	1.5	1.7	kΩ
Dynamic Output Impedance					10		Ω
Voltage Gain	Input Signal = 0.5 V_{p-p} @ 100 kHz	5.3		5.3	5.8	6.3	dB
Bandwidth	Input Signal = 0.5 V_{p-p}, −3 dB,	4.0		4.0	5.0		MHz
Signal to Noise Ratio	Bandwidth = 5 MHz				60		dB
Channel Isolation (Note 1)	Input Signal = 0.5 V_{p-p} @ 3 MHz				60		dB
Crosstalk (Note 2)	Input Signal = 0.5 V_{p-p} @ 3 MHz				−60		dB
Load Resistance (Note 3)	AC Coupled DC Coupled to GND			600 2			Ω kΩ
Power Supply Rejection Ratio	V_S Modulated 1 V_{p-p} @ 1 kHz	40			50		dB
CV Bias (Pin 14) Input Impedance					1.0		kΩ

Electrical Characteristics

V_S = 12V, R_L = 600Ω, C_L = 20 pF, T_A = 25°C unless otherwise stated (Continued)

Parameter	Conditions	Test Limit (Note 6)		Design Limit (Note 7)			Units
		Min	Max	Min	Typ	Max	
RGB CHANNELS	Inputs—Pins 4, 5, 6, 8, 9, 10 Outputs—Pins 15, 16, 17						
CLAMP INPUT-Pin 18 Minimum Input Voltage Maximum Input Voltage	 For Clamp on For Clamp off			 9		 5	 V V
Input Current	Pin 18 = 0V					10	μA
Clamp Pulse Delay (Note 4)						0.2	μs
Maximum Input Voltage Swing	for Output THD = 1% @ 1 kHz			3.0			V_{p-p}
Input Bias Current	Clamp off, Channel Selected				20		μA
Dynamic Output Impedance					20		Ω
Voltage Gain	Input Signal = 1 V_{p-p} @ 100 kHz	−0.5		−0.5	0	+0.5	dB
Bandwidth	Input Signal = 1 V_{p-p}, −3 dB	6.0		24	30		MHz
Signal to Noise Ratio	R_{IN} = 50Ω, Bandwidth = 10 MHz				60		dB
Load Resistance (Note 3)	AC Coupled 3 V_{p-p} DC Coupled to GND			600 2			Ω kΩ
Channel Isolation (Note 1)	Input Signal = 1 V_{p-p} @ 5 MHz				60		dB
Crosstalk (Note 2)	Input Signal = 1 V_{p-p} @ 5 MHz				−50		dB
Power Supply Rejection Ratio	V_S Modulated 1 V_{p-p} @ 1 kHz				50		dB
Pin 13 Output Impedance					60		Ω
SYNC CHANNELS	Inputs—Pins 7, 11 Outputs—Pin 23						
Maximum Input Voltage Swing	for Output THD = 1% @ 1 kHz			3.0			V_{p-p}
Input Impedance				1.8	2.3	2.8	kΩ
Dynamic Output Impedance					40		Ω
Voltage Gain	Input Signal = 1 V_{p-p} @ 100 kHz	−1.0		−1.0	−0.4	+0.2	dB
Bandwidth	Input Signal = 1 V_{p-p}, −3 dB,	6.0		18	24		MHz
Signal to Noise Ratio	R_{IN} = 50Ω, Bandwidth = 10 MHz				60		dB

Note 1: CV channels defined with a CV mute condition set up (ABC = 001) and all CV inputs driven. Isolation is the output measured with respect to the input level for R_L of 600Ω. Channel isolation for RGB channels is measured in the same way with signals applied to the R, G or B inputs while a RGB mute condition is selected.

Note 2: CV crosstalk measured with selected channel input AC grounded and with signal applied to the other CV inputs. Resulting output voltage is measured with R_L of 600Ω. RGB crosstalk is measured similarly with signals applied to unselected channel inputs and measuring the selected channel output. Note that high frequency crosstalk measurements are very dependent on board layout. An effective ground plane and input to input shielding are required.

Note 3: DC output current sourced from device to load should not exceed 10 mA, care should be taken to avoid shorting outputs to GND.

Note 4: Delay between clamp pulse input at Pin 18 and resulting clamping action as seen at RGB inputs.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

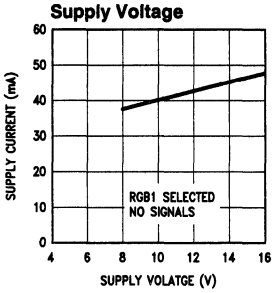
Note 6: Guaranteed and 100% production tested.

Note 7: Design limits are guaranteed to National's AOQL, but are not 100% production tested.

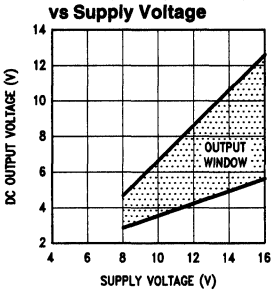
Note 8: When operating at elevated temperatures, the maximum power dissipation must be derated based on a maximum junction temperature of 150°C and θ_{JA} = 60°C/W.

Typical Performance Characteristics

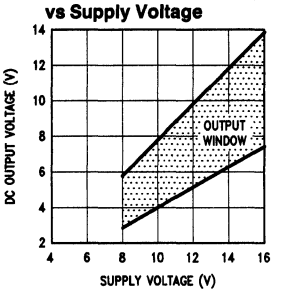
Supply Current vs Supply Voltage



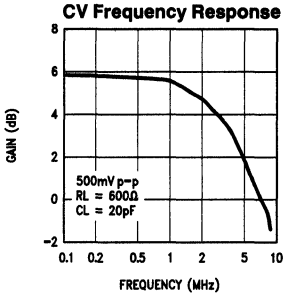
CV Output Signal Range vs Supply Voltage



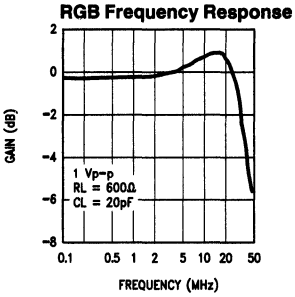
RGB Output Signal Range vs Supply Voltage



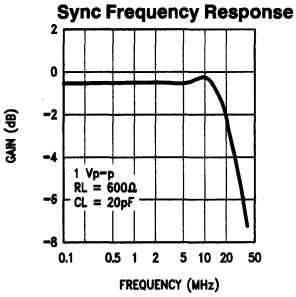
CV Frequency Response



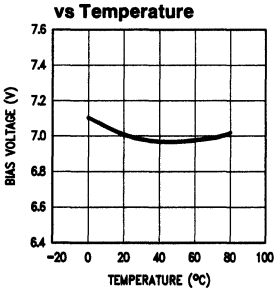
RGB Frequency Response



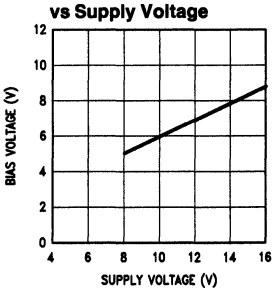
Sync Frequency Response



CV and RGB Bias vs Temperature



CV and RGB Bias vs Supply Voltage



TL/H/9252-2

Pin Description

Note: The pin designations CV, R, G, B, and Sync are assigned for the convenience of description and are not intended to be a limitation. For example RGB could be YUV, or they could all be independent signal sources.

Pin 1	Composite video input 1 (CV1), biased internally via 1.8 kΩ to $\frac{V_S}{2}$ + 1V.
Pin 2	Composite video input 2 (CV2), biased as for pin 1 (CV1) above.
Pin 3	Composite video input 3 (CV3), biased as for pin 1 (CV1) above.
Pin 4	RGB input R1. This pin is internally biased via a clamp circuit to $\frac{V_S}{2}$ + 1V and should be AC coupled to a low impedance source. The input coupling capacitor also acts as a clamp capacitor, see application notes.
Pin 5	RGB input G1, biased as for pin 4 (R1) above.
Pin 6	RGB input B1, biased as for pin 4 (R1) above.
Pin 7	Sync input S1, biased internally via 2.5k to $\frac{V_S}{2}$ + 1V.
Pin 8	RGB input R2, biased as for pin 4 (R1) above.
Pin 9	RGB input G2, biased as for pin 4 (R1) above.
Pin 10	RGB input B2, biased as for pin 4 (R1) above.
Pin 11	Sync input S2, biased as for pin 7 (S1) above.
Pin 12	Negative supply (GND)
Pin 13	Connect a capacitor to GND to decouple the internal bias of the RGB amplifiers.
Pin 14	Internal bias for the CV and Sync Amplifiers, decouple with a capacitor to GND.
Pin 15	B Output.
Pin 16	G Output.
Pin 17	R Output.
Pin 18	This is the clamp pulse input pin. A positive going pulse activates the RGB input bias clamps. See application notes.
Pin 19	Channel select input, control C.
Pin 20	Channel select input, control B.
Pin 21	Channel select input, control A.
Pin 22	Enable input for control latches. Channel selection is locked while this input is low and is updated when high. The minimum enable pulse width is 5 μs.
Pin 23	CV output or Sync output when an RGB channel is selected.
Pin 24	Supply pin (V_S). This pin should be well decoupled at high frequencies, a 100 nF capacitor connected close to the supply pins is normally adequate.

Application Notes

DEVICE DESCRIPTION

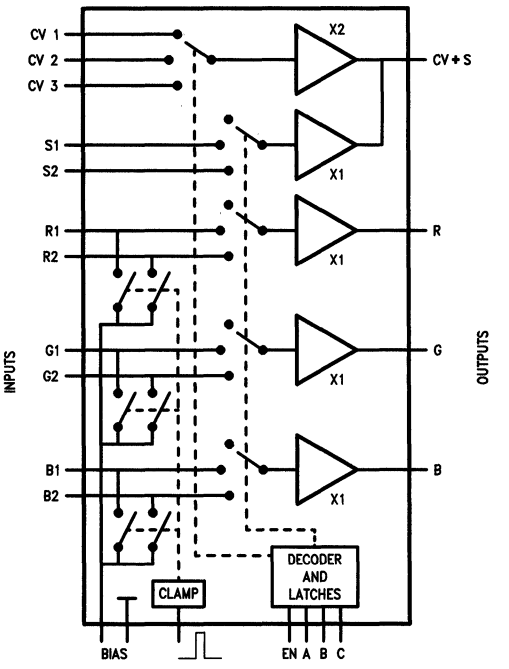
The LM1044 video switch circuit has a configuration as illustrated in *Figure 1* and consists of a 3 input to 1 output, 5 MHz switch with 6 dB gain, three 2 input to 1 output, 30 MHz, 0 dB gain switches, coupled together with a 2 input to 1 output switch sharing the 3 way switch output. All switch stages are current switched differential amplifers with feedback, providing low impedance buffered outputs. Latched logic inputs with control decoding are provided for switch control and a DC clamp facility is available on the 30 MHz channels.

The principle application of this device is the selection between various composite video (CV) or Red, Green, and Blue (RGB) sources now found in video systems using various signal sources, e.g., VCR's, satellite receivers, home computers and video games. Other possible application examples, for example security camera switching, are shown towards the end of these notes.

The 5 MHz channels are ideally suited for the switching of composite video sources and have a gain of 6 dB to allow amplification from terminated inputs back up to internal signal levels. The 30 MHz channels are suitable for direct RGB inputs to display high quality graphics and will also handle high quality linear signals. The fourth switch channel shares the CV output pin and is ideal for routing synchronization signals from the RGB/YUV sources into the path to the sync separator and timebase circuits.

CHANNEL SELECTION

The switch selections are made via the enable and 3 logic control inputs, according to the truth table shown on the following page. This gives a choice of 3 CV video signal sources or 2 RGB plus Sync signals on the video display.



TL/H/9252–3

FIGURE 1

Application Notes (Continued)

Truth Table

Control Logic				Channel Selected
EN 22	C 19	B 20	A 21	
1	0	0	0	CV1, RGB Outputs Muted
1	0	0	1	CV2, RGB Outputs Muted
1	0	1	0	CV3, RGB Outputs Muted
1	0	1	1	RGB1 with Sync1
1	1	1	1	RGB2 with Sync2
1	1	1	0	Mute
1	1	0	1	Mute
1	1	0	0	Mute
0	X	X	X	Previous selection retained

The shaded section of the truth table indicates selection compatible with the LM1038 four channel stereo audio switch logic to give a possible selection of CV1 + Audio1, CV2 + Audio2, CV3 + Audio3, RGB1 + Audio4 and RGB2 + Mute or Audio4; see *Figure 3.*

The mute conditions in the table correspond to disabled CV/Sync (output pulled low) and high impedance RGB outputs which may be connected in parallel with other device outputs for further expansion of the switch system. If all the RGB inputs are being used to switch composite video signals then the RGB outputs can be connected into the CV inputs to allow multiplexing down to 1 output from a large number of input signals.

LOGIC AND ENABLE INPUTS

If undriven the enable input will assume a high impedance logic 1 condition and should be defined externally. The Logic selection inputs have internal pulldowns, typically 20 kΩ, which will define logic low levels if unconnected, giving CV1 in default of any other control input.

INPUT BIAS FOR CV CHANNELS

The CV and Sync inputs are biased via internal 1.5 kΩ and 2.3 kΩ resistors, respectively, to the internally generated 7V bias (V_S = 12V) level at pin 14. Input coupling capacitors need to be chosen to give an adequate low frequency response when driving the 1.5 kΩ input impedance, for example, for less than 2% tilt on a frame rate waveform 330 μF will be required. Depending on the effectiveness of any following clamp circuitry the input coupling capacitors may be reduced in value. These inputs may also be driven with DC coupled signals, provided the standing DC level is sufficiently near to 7V to maintain the output within the output signal range (4.5 to 8.5V for V_S = 12V).

The bias at pin 14 has a DC output resistance typically of 1 kΩ and requires a decoupling capacitor to properly define the gain and crosstalk. To ensure an adequate low frequency response this capacitor should be 100 μF or more. This pin may also be biased from an external voltage source provided the output remains within the output window. Note this bias will also affect the voltage at pin 13.

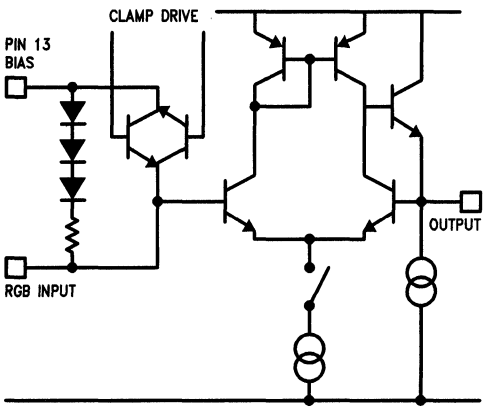
INPUT BIAS FOR RGB CHANNELS

The 6 RGB inputs may be biased in one of three ways;

1) DC restored above an internal 4.5V level
2) Clamped to an internal 7V bias level
3) Driven directly with DC coupled signals

With an AC coupled input signal and the clamp pulse held low the negative going peaks will DC restore to a level greater than 3 diode drops below the reference bias level at pin 13, typically 4.5V for V_S = 12V. The source resistance of the diode restoring path is 1 kΩ for currents below 200 μA.

Simplified Schematic of RGB Stage



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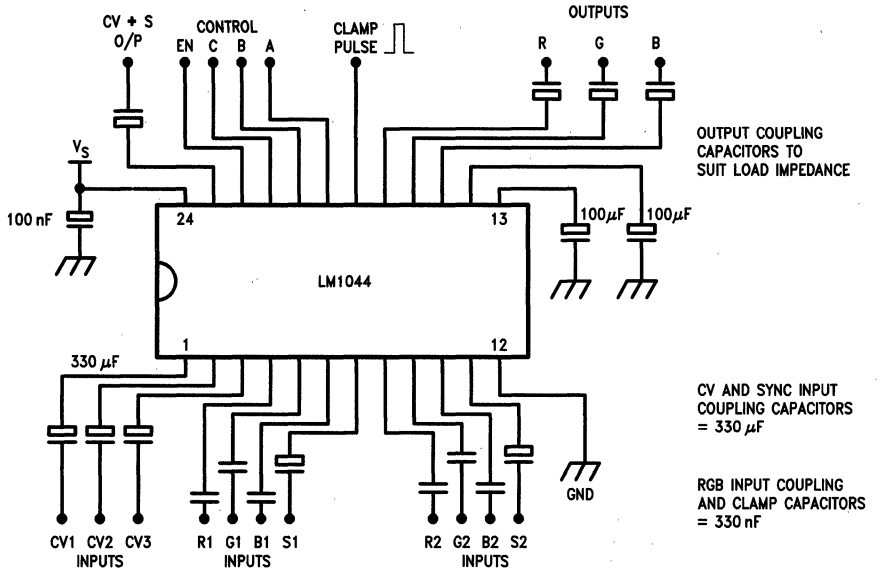
The simplified schematic of the CV stage is virtually identical to the RGB stage except that the CV stage does not incorporate the clamp circuitry.

Clamping to the internal 7V bias is arranged by applying a positive going clamp pulse to pin 18 during a time when the input signals are at a black reference level. This is usually during the back porch or during the blanking period of signals without syncs. The clamp pulse width should not be less than 3 μs. During the time pin 18 is high all six inputs R1, R2, G1, G2, B1 and B2 are connected to the RGB bias voltage developed at pin 13, charging the input coupling capacitors to this level. These coupling capacitors are chosen to optimize value versus tilt introduced during the active line period. A value of 330 μF gives less than 1% tilt for input currents less than 20 μA. The effective impedance of the clamp path when conducting is 300Ω. The voltage at pin 13 is a low impedance, 60Ω, buffered version of the CV bias voltage at pin 14 and decoupling is required to remove high frequencies and maintain channel separation. The voltage at pin 13 may be changed by driving pin 14 as described for CV bias.

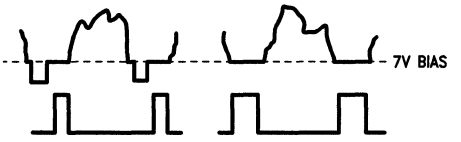
Application Notes (Continued)



TL/H/9252–7

FIGURE 2. LM1044 Basic Application Circuit

Relation of Clamp Pulse to Video



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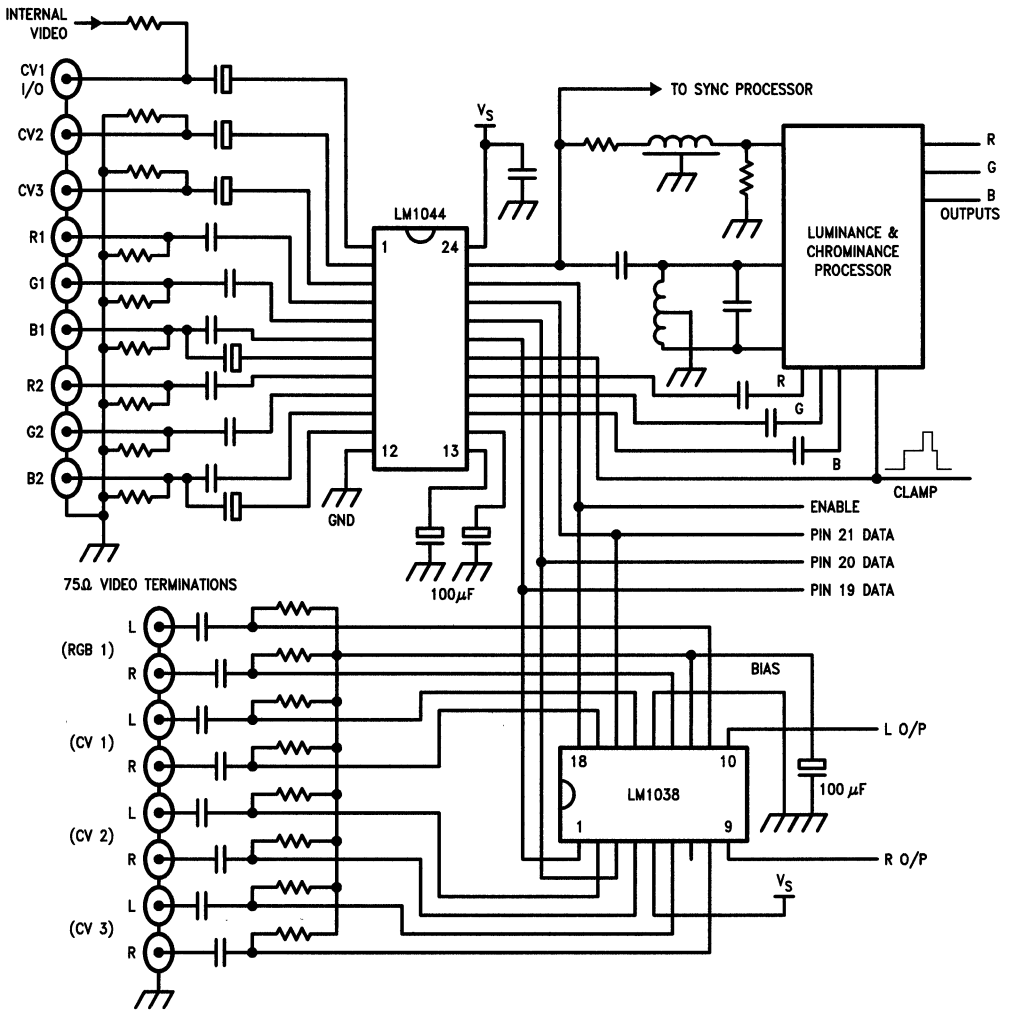
If the clamp pulse input is held low the RGB inputs may be driven directly with DC coupled signals provided the levels are such as to remain within the output window. Such signals could be directly coupled from the RGB outputs of a preceeding LM1044, avoiding the need for coupling capacitors when expanding the switching capability. External resistive biasing to the bias voltage available at pin 13 may also be used for a mean level bias with AC coupled signals not having reference levels.

OPERATION AT SUPPLIES OTHER THAN 12V

The LM1044 may be operated at supply voltages between 8V and 16V. Note that the CV and RGB bias voltages, together with the clamp pulse threshold, will track with supply variations whilst the logic input thresholds will remain essentially constant. At lower supply voltages the signal handling may be optimized with an external bias voltage to pin 14.

Application Notes (Continued)



TL/H/9252–5

FIGURE 3. LM1044 Application Circuit Showing System Interfacing and LM1038

OPERATION WITH SPLIT SUPPLIES

The LM1044 may be operated with split supplies with due regard to the maximum supply voltage (16V) and output signal range. An example of operation in this way is illustrated below. With ±5V and pin 14 held at 0V the RGB outputs can swing +2V, −1.5V and the CV and Sync output can swing +1.3V, −1.3V. Similarly with +10V, −5V supplies, pin 14 to 0V, RGB output swings of +5.5V, −1.5V and CV/Sync swings of +4.5V and −1.5V can be obtained. This supply configuration has the advantage that pin 14 can be grounded and all signals may be DC coupled avoiding the need for coupling capacitors. Offsets introduced are typically −30 mV for CV and RGB channels, and −140 mV for Sync channels.

OTHER APPLICATIONS

The LM1044 can be used in other than the standard CV with RGB circuit and an example is given below of a dual 6 input to 1 output multiplexer for video or indeed any kind of signals up to 2 V_{p-p}. In this particular example the RGB outputs are cross-coupled into the CV inputs of the other channel to complete the multiplexing down to 2 outputs. The clamp circuits are disabled to allow direct drive on the inputs. Such circuits are ideal for security cameras and other multiple video source monitoring systems.

Application Notes (Continued)

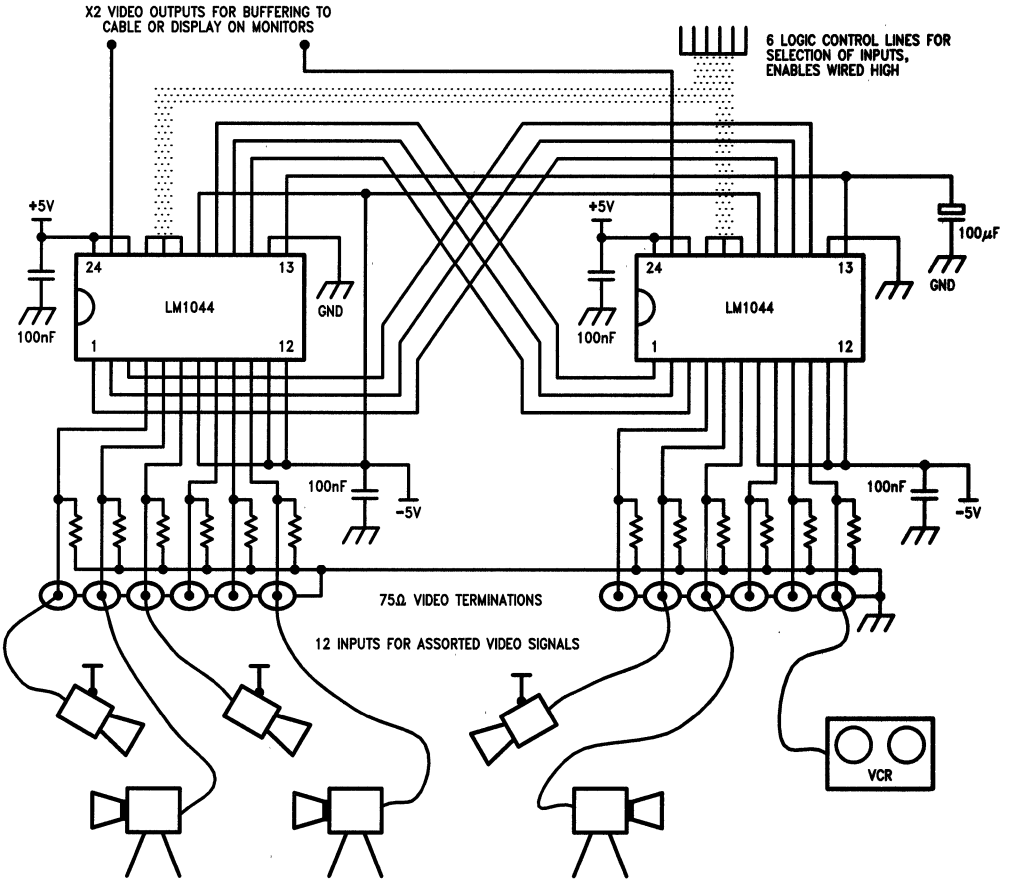


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FIGURE 4. Application Circuit Example Using Two LM1044 Devices as a Dual 6 Channel Multiplexer and Illustrating Use of Split Supplies

National Semiconductor

LM1201 Video Amplifier System

General Description

The LM1201 is a wideband video amplifier system intended for high resolution monochrome or RGB monitor applications. In addition to the wideband video amplifier the LM1201 contains a gated differential input black level clamp comparator for brightness control and an attenuator circuit for contrast control. The LM1201 also contains a voltage reference for the video input. For medium resolution RGB color monitor applications also see the LM1203 Video Amplifier System data sheet.

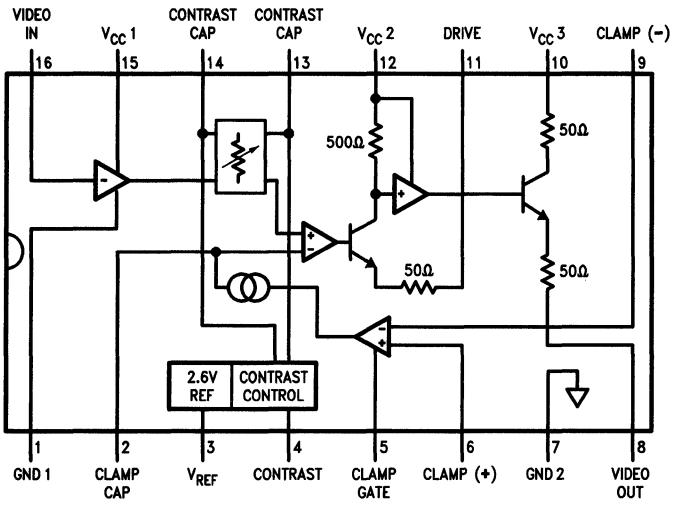
Features

- Wideband video amplifier (200 MHz @ −3 dB)
- Attenuator circuit for contrast control (>40 dB range)
- Externally gated comparator for brightness control
- Provisions for external gain set and peaking of video amplifier
- Video input voltage reference
- Low impedance output driver

Typical Applications

- CRT video amplifiers
- Video switches
- High frequency video preamplifiers
- Wideband gain controls
- PC monitors
- Workstations
- Facsimile machines
- Printers

Block and Connection Diagram



TL/H/10006–1

FIGURE 1

Order Number LM1201M or LM1201N
See NS Package Number M16A or N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 10, 12, 15 to Ground Pins, 1, 7 — 13.5V

Voltage at Any Input Pin (V_{IN}) — $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current (I_8) — 28 mA

Package Power Dissipation at $T_A = 25°C$ (Above 25°C derate based on (θ_{JA} and T_J) — 1.56W

Package Thermal Resistance (θ_{JA}) N16E — 80°C/W

Package Thermal Resistance (θ_{JA}) M16A — 100°C/W

Junction Temperature (T_J) — 150°C

Operating Temperature Range (T_A) — 0°C to +70°C

Storage Temperature Range (T_{STG}) — −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) — 265°C

ESD Susceptibility — 2 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics

See Test Circuit (Figure 2), $T_A = 25°C$; $V_{CC1} = V_{CC2} = V_{CC3} = 12V$

DC Static Tests

S9 Open; V4 = 6V; V5 = 0V; V6 = 2.0V unless otherwise stated

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
I_S	Supply Current	V_{CC} Pins 12, 15 Only	45	57		mA(max)
V_3	Video Input Reference Voltage		2.65	2.4		V(min)
				2.95		V(max)
I_{16}	Video Input Bias Current	$(V_3-V_{16})/10\ k\Omega$	5.0	20		μA(max)
V_{5L}	Clamp Gate Low Input Voltage	Clamp Comparator On	1.2	0.8		V(min)
V_{5H}	Clamp Gate High Input Voltage	Clamp Comparator Off	1.6	2.0		V(max)
I_{5L}	Clamp Gate Low Input Current	$V_5 = 0V$	−0.5	−5.0		μA(max)
I_{5H}	Clamp Gate High Input Current	$V_5 = 12V$	0.005	1		μA(max)
I_{2+}	Clamp Cap Charge Current	$V_2 = 0V$	1	0.55		mA(min)
I_{2-}	Clamp Cap Discharge Current	$V_2 = 5V$	−1	−0.55		mA(min)
V_{8L}	Video Output Low Voltage	$V_2 = 0V$	0.5	0.9		V(max)
V_{8H}	Video Output High Voltage	$V_2 = 5V$	8.5	8.0		V(min)
V_{OS}	Comparator Input Offset Voltage	V_6-V_9	±0.5	±25		mV(max)

AC Dynamic Tests

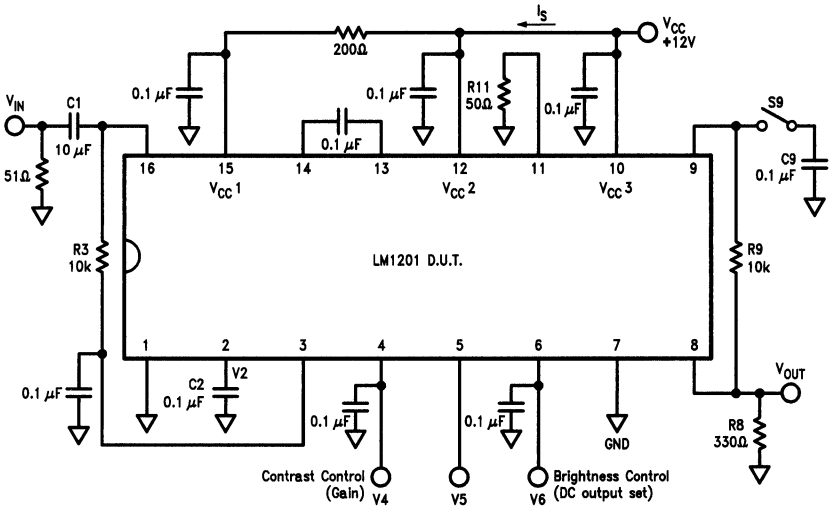
S9 Closed, $V_5 = 0V$, $V_6 = 4V$

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
Av max	Video Amplifier Gain	$V_4 = 12V$	8	5.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, $V_4 = 5V$	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, $V_4 = 2V$	−45			dB
THD	Video Amplifier Distortion	$V_4 = 5V$, $V_O = 1\ V_{p-p}$	0.3			%
f (−3dB)	Video Amplifier Bandwidth (Note 3)	$V_4 = 12V$, $V_O = 100\ mV_{rms}$	200		170	MHz(min)
t_r	Output Rise Time (Note 3)	$V_O = 4\ V_{p-p}$	2.5			ns
t_f	Output Fall Time (Note 3)	$V_O = 4\ V_{p-p}$	3			ns

Note 1: These parameters are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

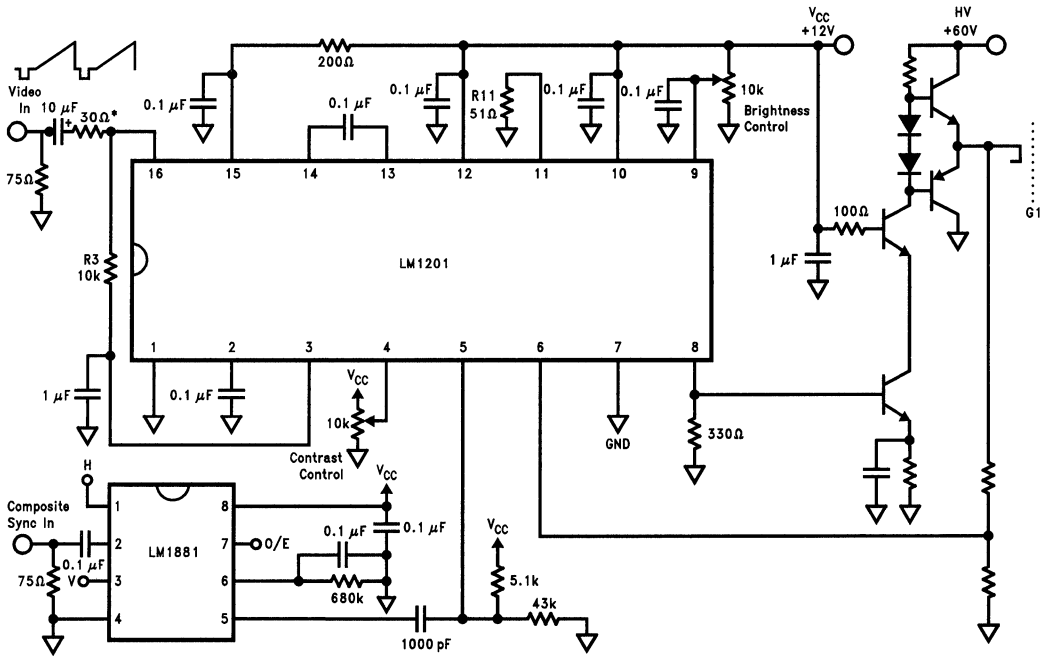
Note 3: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended.



TL/H/10006–2

FIGURE 2. LM1201 AC/DC Test Circuit

Note: When $V_5 \leq 0.8V$ and S9 is closed, DC feedback around the Video Amplifier is provided by the clamp comparator. Under these conditions sine wave or 50% duty cycle square waves can be used for test purposes. The low frequency dominant pole is determined by C2 at Pin 2. Capacitor C9 at pin 9 prevents overloading the clamp comparator inverting input. See applications section for additional information.



TL/H/10006–3

FIGURE 3. Typical Application of the LM1201

* 30Ω resistor is added to the input pin for protection against current surges coming from the 10 μF input capacitor. By increasing this resistor to well over 100Ω the rise and fall times of the LM1201 can be increased for EMI considerations.

APPLICATIONS INFORMATION

Figure 4 shows the block diagram of a typical analog monochrome monitor. The monitor is used with CAD/CAM work stations, PCs, arcade games and in a wide range of other applications that benefit from the use of high resolution display terminals. Monitor characteristics may differ in such ways as sweep rates, screen size, or in video amplifier speed but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained as a composite signal in the video input signal. The video input signal is usually supplied by coaxial cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifier. The input signal is approximately 1V peak-to-peak in amplitude and at the input of the high voltage video section, approximately 6V peak-to-peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. The block in *Figure 4* labeled "Video Amplification with DC Controlled Gain/Black Level" contains the function of the LM1201 video amplifier system.

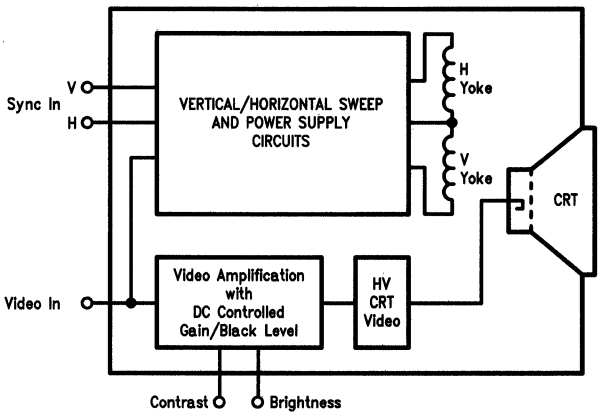


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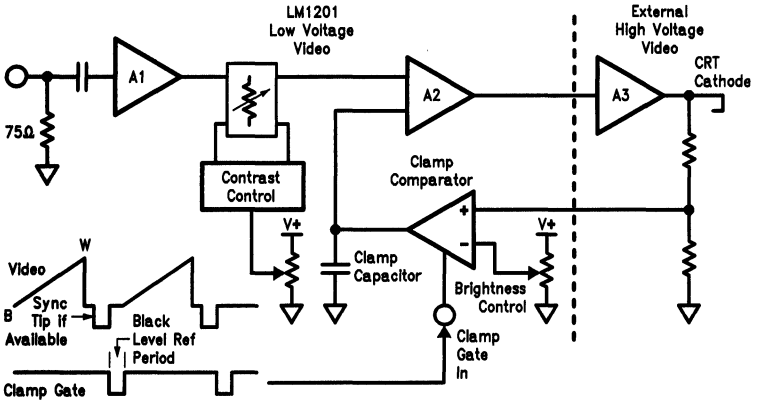
FIGURE 4. Typical Monochrome Monitor Block Diagram

Circuit Description

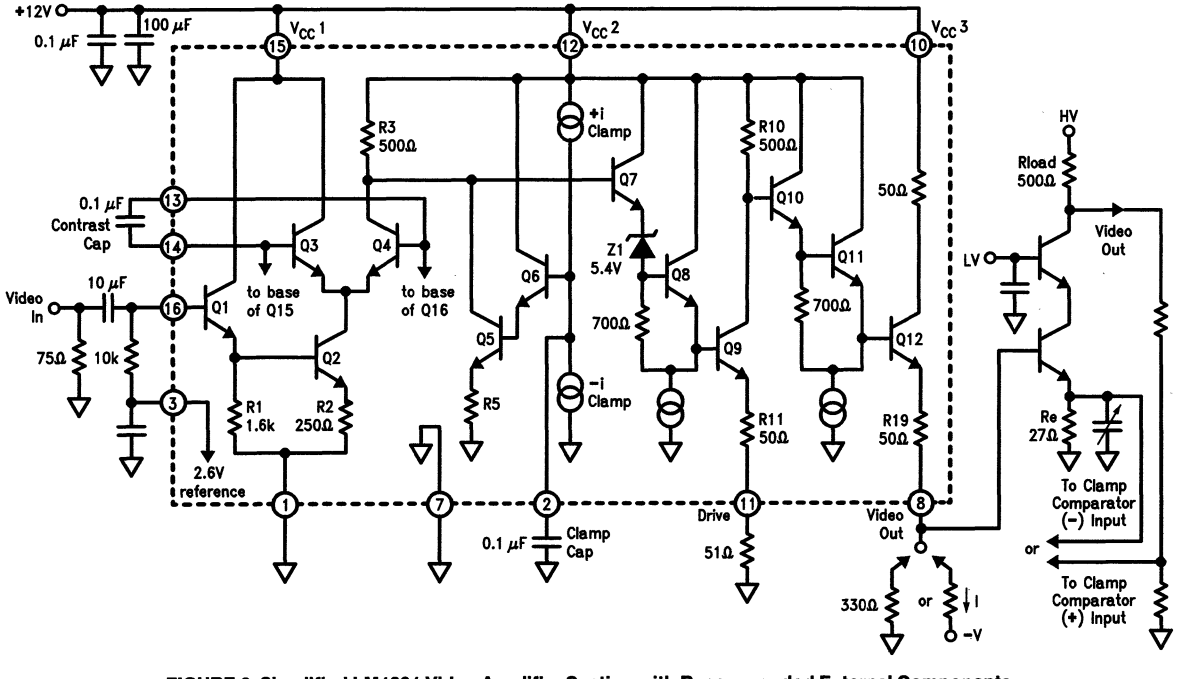
Figure 5 is a block diagram of the LM1201 along with the contrast and brightness controls. The contrast control is a DC operated attenuator which varies the AC gain of the amplifier without introducing any signal distortions or DC output shift. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifier and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the non-inverting input of the clamp comparator matches that of the inverting input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of the LM1201 video amplifier along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 16 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.6V reference at pin 3. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC1} supply through Q3 or to V_{CC2} through Q4 and the 500Ω load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. The black level DC voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.



TL/H/10006–5

FIGURE 5. Block Diagram of LM201 Video Amplifier with Contrast and Black Level Control



TL/H/10006–6

FIGURE 6. Simplified LM1201 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to set the maximum gain of the amplifier based on the range of input video signal levels and the CRT stage gain if it is fixed or limited. When using three LM1201 devices for high resolution RGB applications, the "Drive" pin allows the user to trim the gain of each channel to correct for differences in the three CRT cathodes. A small capacitor (12 pF) in shunt with a 51Ω drive resistor at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. The 51Ω resistor will set the system gain to approximately 8 or 18 dB. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 50Ω resistor which is included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 330Ω, otherwise package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V, and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 50Ω resistor. Precautions must be taken to prevent the video output pin from going below ground since IC substrate currents may cause erratic operation. The collector current from the video output transistor is returned to the power supply at V_{CC3}, pin 10. When making power dissipation calculations note that the datasheet specifies only the V_{CC1} and V_{CC2} supply currents at 12V. The IC power dissipation contribution of V_{CC3} is dependent upon the video output emitter pull down load.

In normal operation the minimum black level voltage that can be set at the video output pin is approximately 2V at maximum contrast setting. In applications that require a lower black level voltage, a resistor (approximately 16 kΩ) can be added from pin 3 to ground. This has the effect of raising the DC voltage at the collector of Q4 which will extend the range of the black level clamp by allowing Q5 to remain active. In applications that require video amplifier shutdown due to fault conditions detected by monitor protection circuits, pin 3 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control potentiometers and V_{CC}.

Figure 7 shows the internal construction of the pin 3 2.6V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier input. The value of the external DC biasing resistors should not be larger than 10 kΩ when using more than one LM1201 (e.g. in RGB systems) because minor differences in input bias currents on the individual video amplifiers may cause offsets in gain.

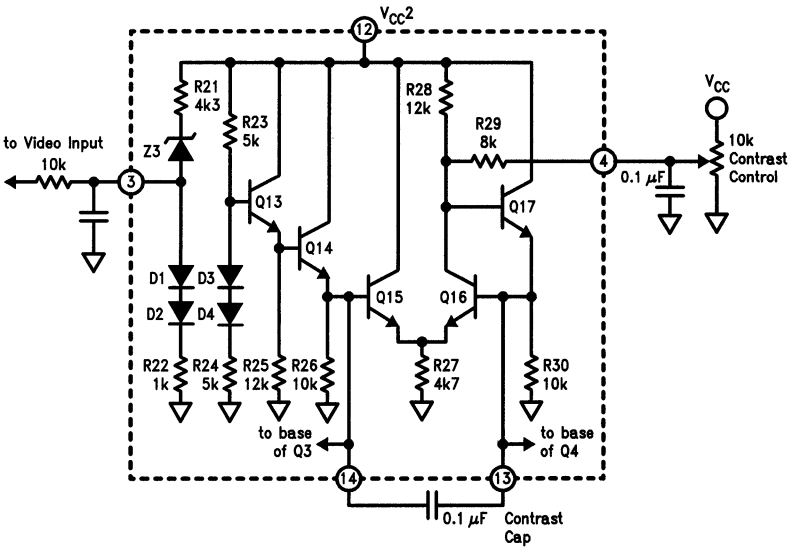


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FIGURE 7. LM1201 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, R24, diodes D3, D4, and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, Q16 and feedback transistor Q17 along with resistors R27, R28 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 4. A capacitor should be added from pin 4 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator section of the LM1201. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, Q20) and an output switch (Q21). When the clamp gate input at pin 5 is high (>1.5V), the Q21 switch is on and shunts the I1 1mA current to ground. When pin 5 is low (<1.3V), the Q21 switch is off and the I1 1mA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 1mA current source for the clamp comparator. The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitor at pin 2. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter-base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, resistor R34 with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, Q25 to approximately 350 mV. The clamp comparator common mode range extends from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

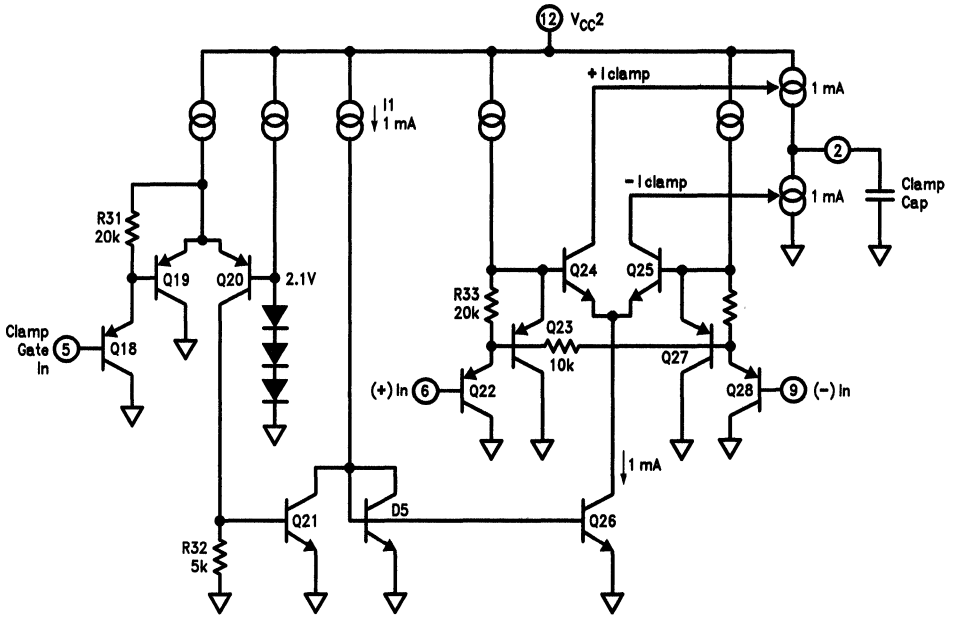

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FIGURE 8. Simplified Schematic of LM1201 Clamp Gate and Clamp Comparator Circuits

Applications Information

Figure 9 shows the configuration of a high frequency amplifier with non-gated DC feedback. Pin 5 is tied low to turn on the clamp comparator (feedback amplifier). The inverting input (pin 9) is connected to the amplifier output from a low pass filter. Additional low frequency filtering is provided by the clamp capacitor. The Drive pin is grounded to allow for the widest range of output signals. Maximum output swing is achieved when the DC output is set to approximately 4.5V.

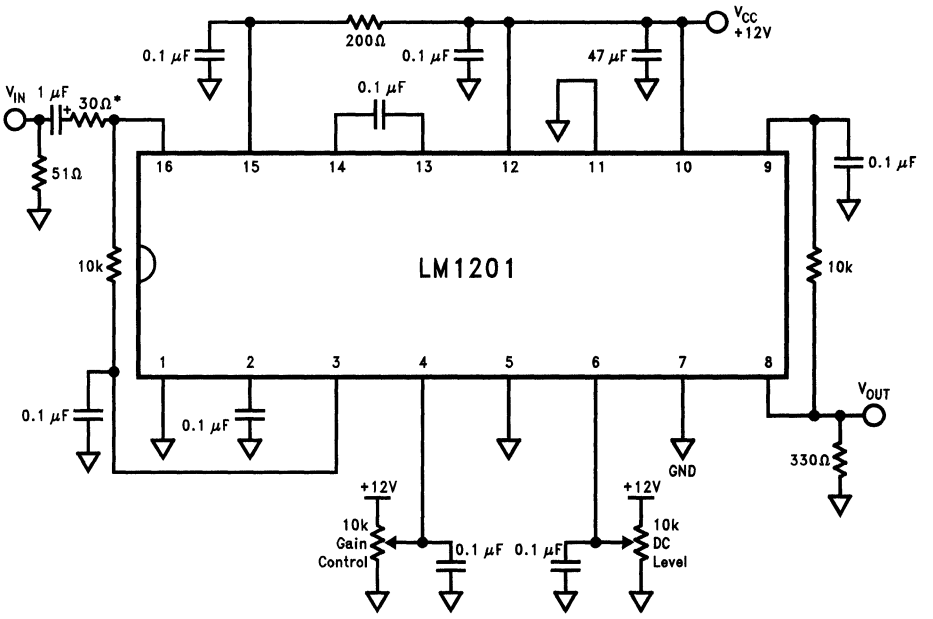

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FIGURE 9. High Frequency Amplifier/Attenuator Circuit with Non-Gated DC Feedback (Non-Video Applications)

Applications Information (Continued)

Figure 10 shows the LM1201 set up as a video amplifier with biphase outputs. Because the collector of output transistor Q12 is the only internal connection to V_{CC3}, a 75Ω termination to the power supply voltage allows one to obtain inverted video at pin 10. Black level on the non-inverted video output (pin 8) is set to 1.5V by the voltage divider on pin 6.

Figure 11 shows how a high frequency video switch may be designed using multiple LM1201 devices. All outputs can be OR'ed together assuming no more than one channel is selected at any given time. Channel selection is accomplished by keeping the appropriate SELECT SWITCH open. Closing the SELECT SWITCH on a given channel disables that channel's output (pin 8) leaving it in a high impedance state. A single pair of contrast and brightness potentiometers control the selected channel's gain and output DC level.

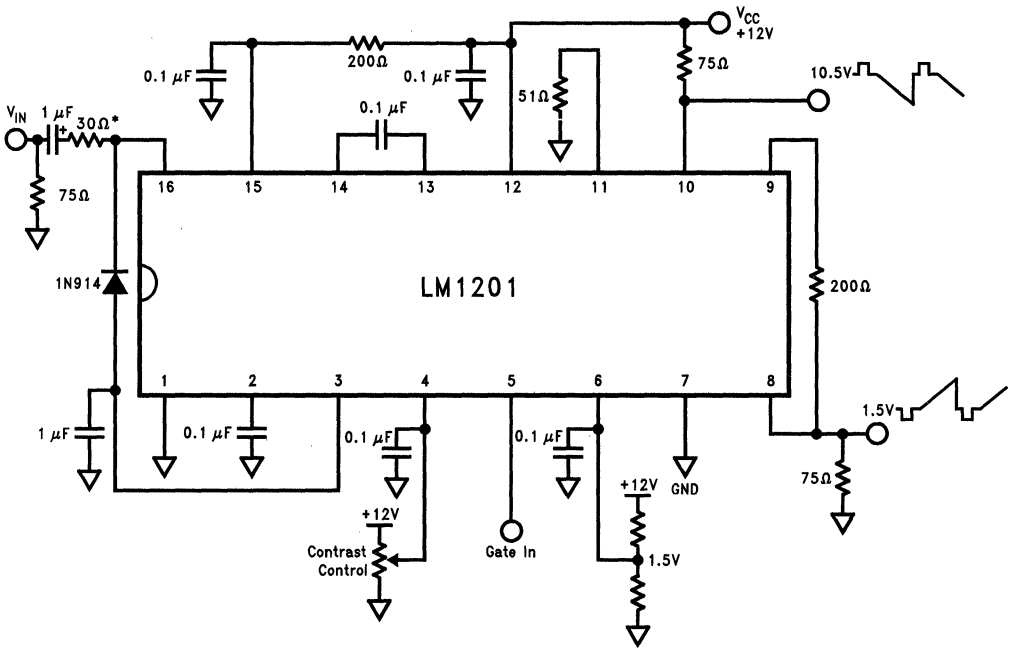

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FIGURE 10. Preclamped Video Amplifier with Biphase Outputs

Applications Information (Continued)

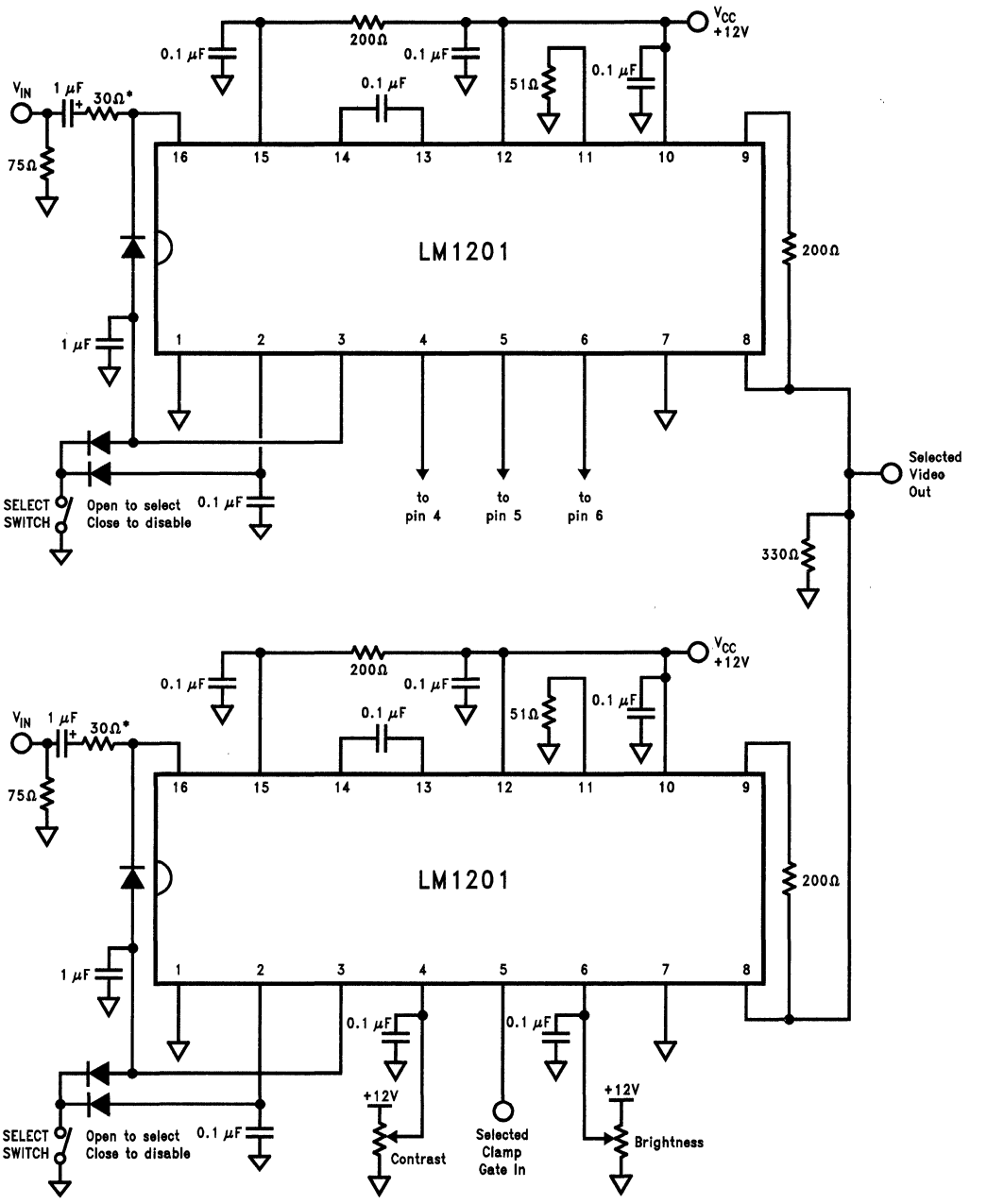

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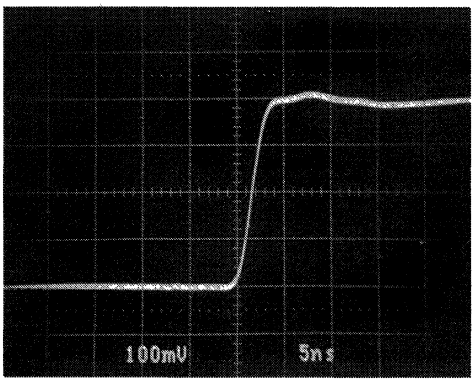
FIGURE 11. High Frequency Video Switch with Common Contrast and Brightness Controls

Rise Time No Socket



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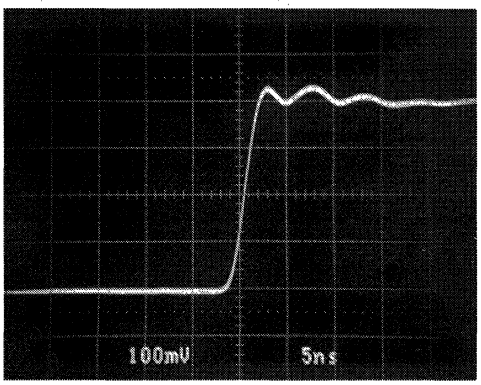
Rise Time In Socket



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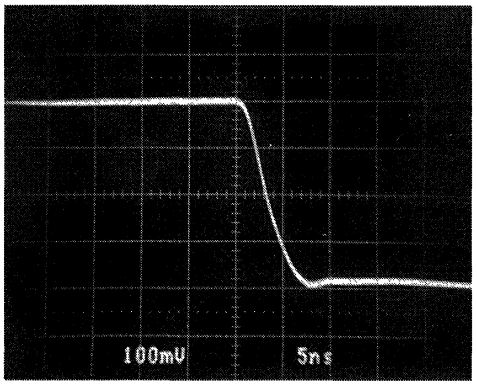
Fall Time No Socket



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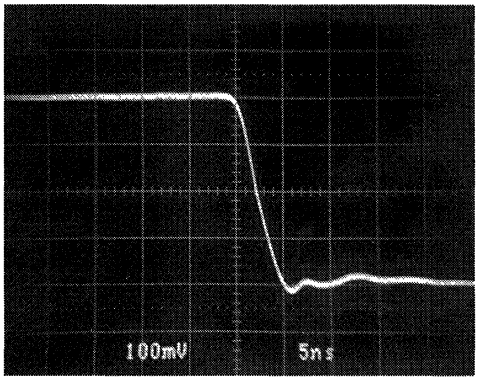
Fall Time In Socket

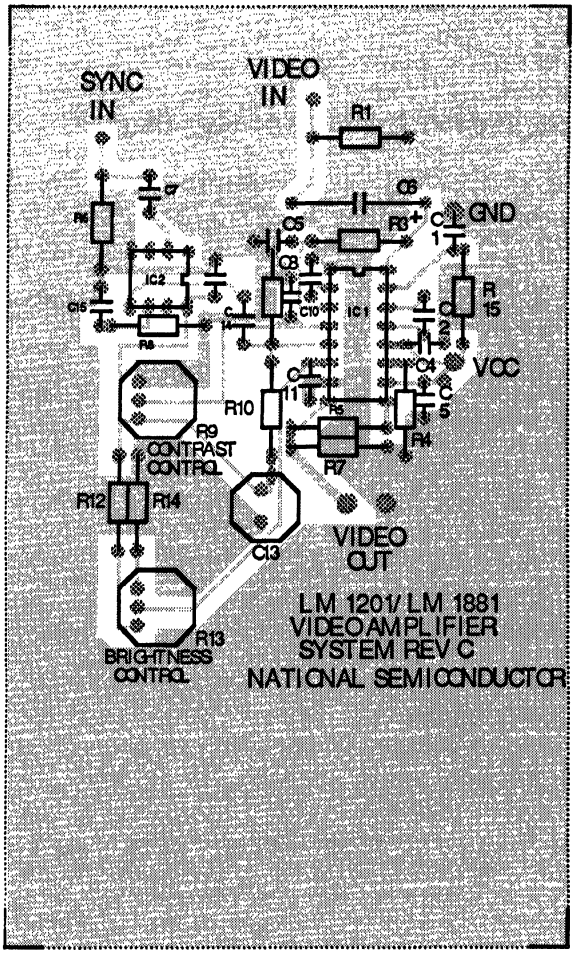


TL/H/10006–15

HP8082 pulse generator
HP10241A 10:1 voltage divider
HP1120A 500 MHz FET probe
Tektronix 2465A 350 MHz scope

Scale for All Photos—Vert: 1V/Div
Horiz: 5 ns/Div

- Actual output signal swings 4 V_{p-p} (10:1 divider is used)
- Contrast is set to maximum
- V_{IN} = 500 mV_{p-p}
- R_{DRIVE} = 50Ω
- Vertical scale is actually 1V/div and not 100 mV/div due to 10:1 attenuator used.
- Outputs are centered at 4V DC.



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Note: The p.c.b. layout shown above is suitable for evaluating the performance of the LM1201. Although it is similar to the typical application circuit of Figure 3, there is no c.r.t. driver stage. Instead, a feedback resistor is connected between Pins 8 and 9 and the brightness control is connected to Pin 6. Again, for best results, a socket should not be used for the LM1201.

COMPONENT VALUES:

R1	75Ω, 5%, 1/4 watt, carbon composition	C1	0.1 μF, ceramic
R3	10 kΩ, 5%, 1/4 watt, carbon composition	C2	0.1 μF, ceramic
R4	50Ω, 5%, 1/4 watt, carbon composition	C4	0.1 μF, ceramic
R5	200Ω, 5%, 1/4 watt, carbon composition	C5	0.1 μF, ceramic
R6	75Ω, 5%, 1/4 watt, carbon composition	C6	10 μF/6V, electrolytic
R7	330Ω, 5%, 1/4 watt, carbon composition	C7	0.1 μF, ceramic
R8	680 kΩ, 5%, 1/4 watt, carbon composition	C8	0.1 μF, ceramic
R9	10 kΩ, trim pot, helitrim model 91	C9	0.1 μF, ceramic
R10	5.1 kΩ, 5%, 1/4 watt, carbon composition	C10	0.1 μF, ceramic
R11	43 kΩ, 5%, 1/4 watt, carbon composition	C11	0.1 μF, ceramic
R12	12 kΩ, 5%, 1/4 watt, carbon composition	C12	0.1 μF, ceramic
R13	10 kΩ, trim pot, helitrim model 91	C13	100 μF/15V, electrolytic
R14	2 kΩ, 5%, 1/4 watt, carbon composition	C14	0.001 μF, mica
R15	200Ω, 5%, 1/4 watt, carbon composition	C15	0.1 μF, ceramic
IC1	LM1201		
IC2	LM1881		

National Semiconductor

LM1202 230 MHz Video Amplifier System

General Description

The LM1202 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications. In addition to the wideband video amplifier the LM1202 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0V to 4V range for easy interface to bus controlled alignment systems. The LM1202 operates from a nominal 12V supply but can be operated with supply voltages down to 8V for applications that require reduced IC package power dissipation characteristics.

Features

- Wideband video amplifier (f_{-3dB} = 230 MHz at V_O = 4 V_{PP})
- t_r, t_f = 1.5 ns at V_O = 4 V_{PP}
- Externally gated comparator for brightness control
- 0V to 4V high input impedance DC contrast control (>40 dB range)
- 0V to 4V high input impedance DC drive control (±3 dB range)
- Easy to parallel three LM1202s for optimum color tracking in RGB systems
- Output stage clamps to 0.65V and provides up to 9V output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

Applications

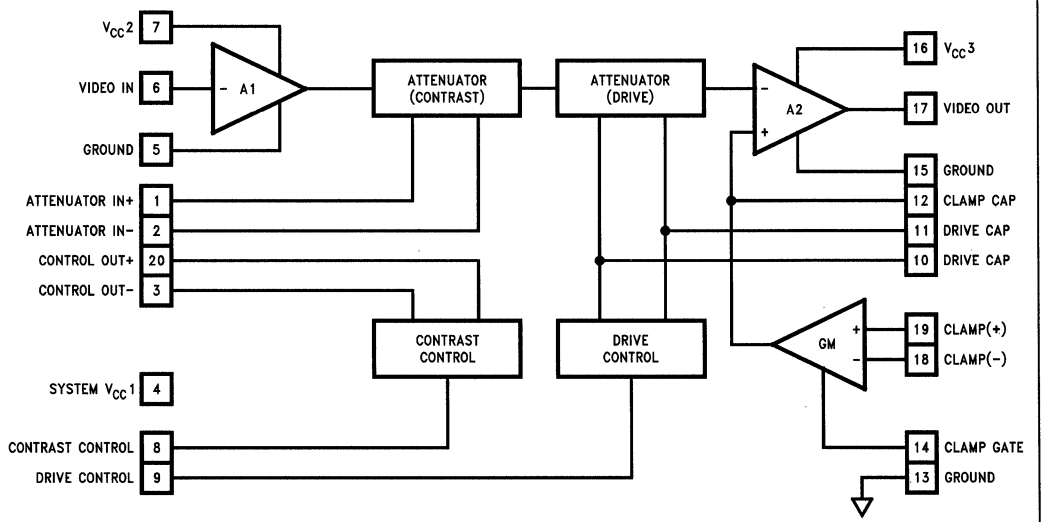
High resolution CRT monitors

Video switches

Video AGC amplifier

Wideband amplifier with gain and DC offset control

Block and Connection Diagram



TL/H/11440–1

Order Number LM1202N or LM1202M
See NS Package Number N20A or M20B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 4, 7, 16 to Ground Pins 5, 13, 15 — 13.5V

Voltage at Any Input Pin (V_{IN}) — $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current (I_{17}) — 28 mA

Package Power Dissipation at $T_A = 25°C$ (Above 25°C Derate Based θ_{JA} and T_J) — 1.56W

Package Thermal Resistance (θ_{JA})
- N20A — 68°C/W
- M20B — 90°C/W

Junction Temperature (T_J) — 150°C

Storage Temperature Range (T_{stg}) — −65°C to +150°C

Lead Temperature
- N Package (Soldering, 10 sec.) — 265°C

ESD Susceptibility
- Human Body Model: 100 pF Discharged through a 1.5k Resistor — 1.5 kV

Operating Ratings (Note 2)

Temperature Range — −20°C to +80°C

Supply Voltage (V_{CC}) — $8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Open, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
I_S 4, 7, 16	Total Supply Current	$R_{Load} = \infty$ (Note 5)	48	60	mA (max)
V_6	Video Input Bias Voltage		2.4	2	V (min)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparator On		0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparator Off		2	V (min)
I_{14L}	Clamp Gate Low Input Current	$V_{14} = 0V$	−0.5		μA
I_{14H}	Clamp Gate High Input Current	$V_{14} = 12V$	0.005		μA
I_{12+}	Clamp Cap Charge Current	$V_{12} = 0V$	800	500	μA (min)
I_{12-}	Clamp Cap Discharge Current	$V_{12} = 5V$	−800	−500	μA (min)
V_{17L}	Video Output Low Voltage	$V_{12} = 0V$	0.2	0.65	V (max)
V_{17H}	Video Output High Voltage	$V_{12} = 6V$	10	9	V (min)
V_{OS}	Comparator Input Offset Voltage	$V_{18} - V_{19}$	15	±50	mV (max)

AC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Closed, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
R_{IN}	Video Amplifier Input Resistance	$f_{IN} = 12$ kHz	20		kΩ
A_V max	Video Amplifier Gain	$V_8 = 4V$, $V_9 = 4V$	20	16	V/V (min)
ΔA_V 2V	Attenuation at 2V	Ref: A_V max, $V_8 = 2V$	−6		dB
ΔA_V 0.5V	Attenuation at 0.5V	Ref: A_V max, $V_8 = 0.5V$	−38	−23	dB (min)
Δ Drive	Δ Gain Range	$V_9 = 0V$ to 4V	6	5	dB (min)
THD	Video Amplifier Distortion	$V_O = 4\ V_{PP}$, $f_{IN} = 12$ kHz	0.5	1	% (max)
$f_{-3\ dB}$	Video Amplifier Bandwidth (Note 6)	$V_O = 4\ V_{PP}$	230		MHz
t_r	Output Rise Time (Note 6)	$V_O = 4\ V_{PP}$	1.5	2	ns (max)
t_f	Output Fall Time (Note 6)	$V_O = 4\ V_{PP}$	1.5	2	ns (max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

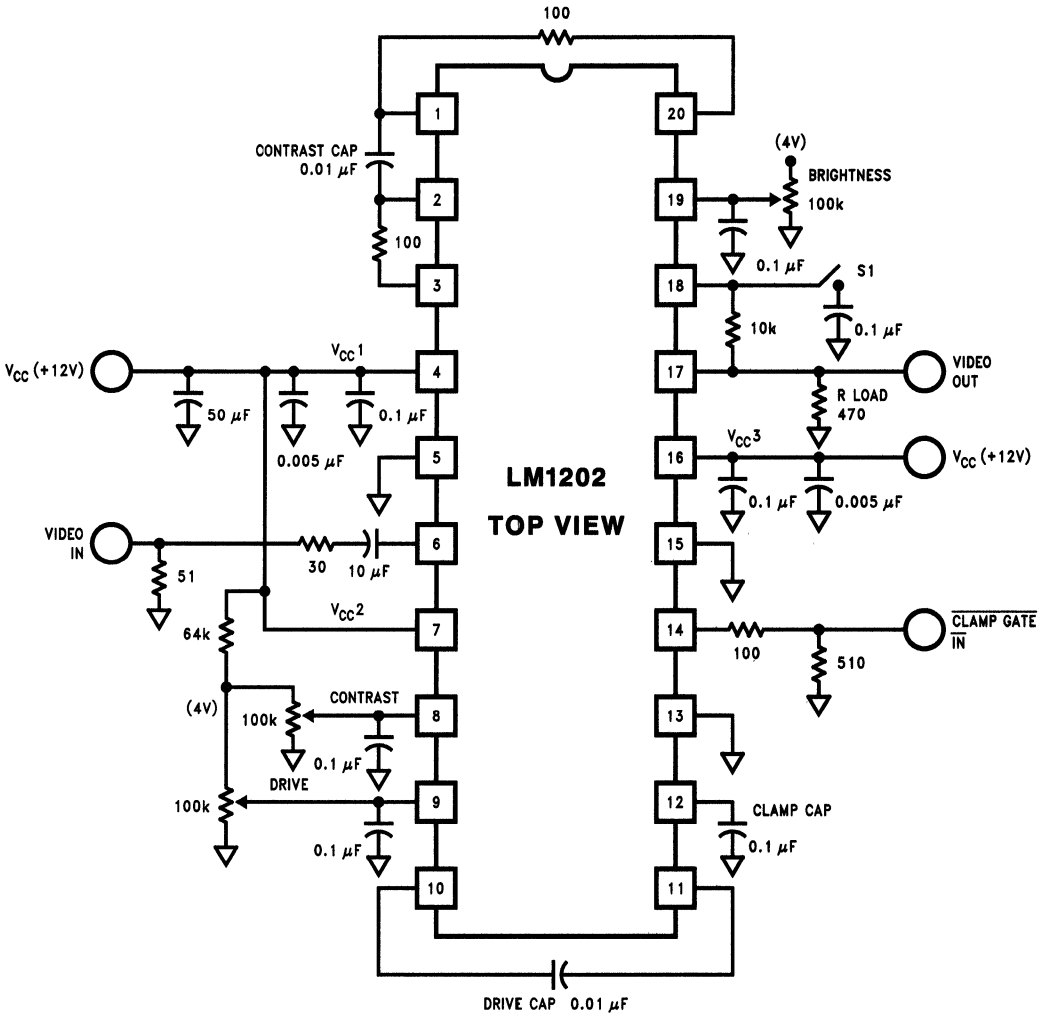
Note 3: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 4: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 5: The supply current specified is the quiescent current for V_{CC1}, V_{CC2} and V_{CC3} with $R_{Load} = \infty$, see *Figure 1's* test circuit. The total supply current also depends on the output load, R_{Load}. The increase in device power dissipation due to R_{Load} must be taken into account when operating the device at the maximum ambient temperature.

Note 6: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator and the oscilloscope.

Test Circuit

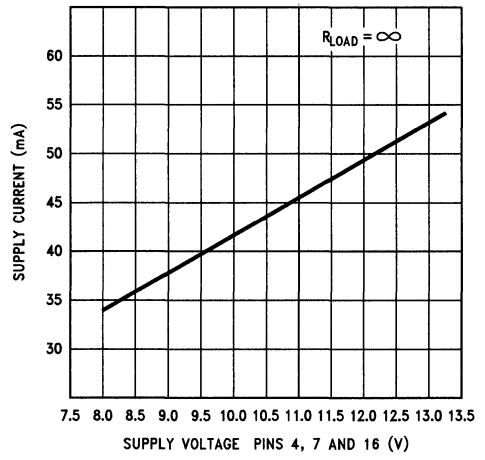


TL/H/11440–2

FIGURE 1. LM1202 Test Circuit

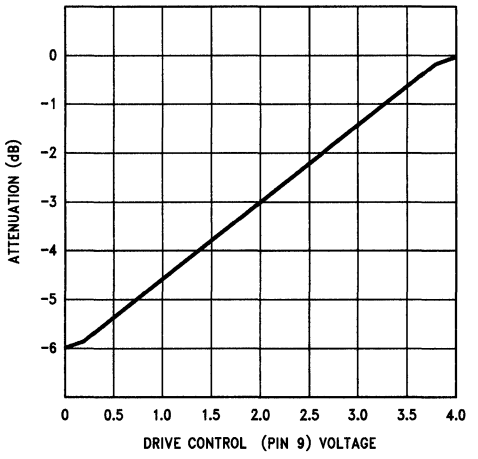
Typical Performance Characteristics (V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Quiescent Supply Current vs Supply Voltage



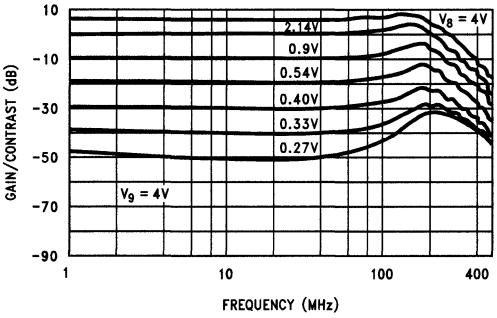
TL/H/11440–12

Attenuation vs Drive Control Voltage



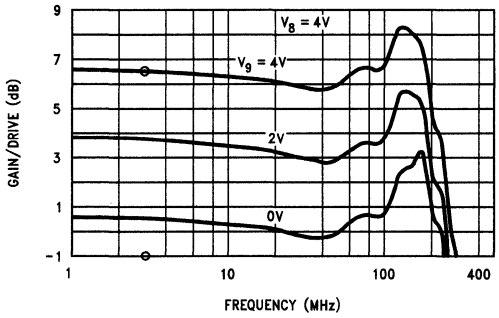
TL/H/11440–13

Contrast vs Frequency



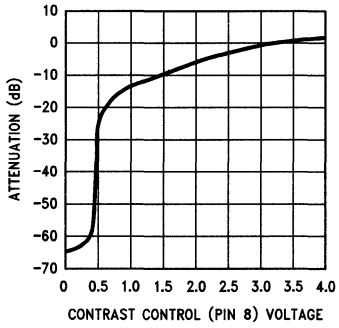
TL/H/11440–14

Drive vs Frequency



TL/H/11440–15

Attenuation vs Contrast Control Voltage



TL/H/11440–16

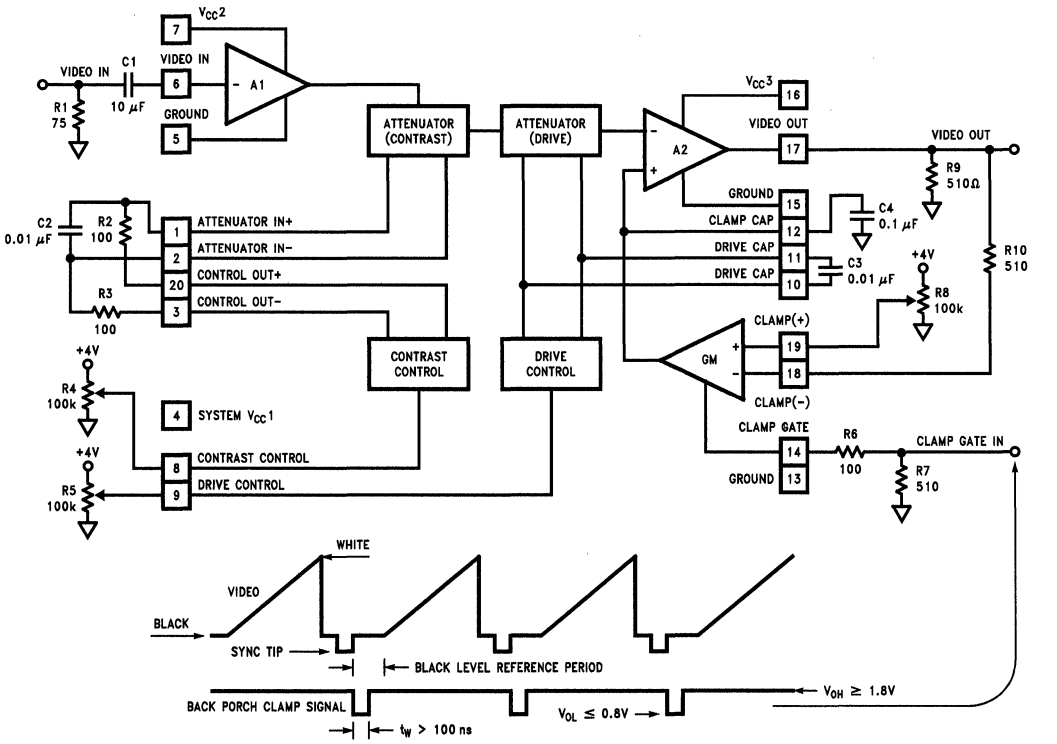
Circuit Description

Figure 2 shows a block diagram of the LM1202 video amplifier along with contrast and brightness (black level) control. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. As shown in *Figure 2*, pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independent gain adjustment of each channel is required.

The brightness or black level clamping requires a "sample and hold" circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration, is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period (see *Figure 2*). When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width (t_W in *Figure 2*) must be greater than 100 ns for proper operation.

VIDEO AMPLIFIER SECTION (Input Stage)

A simplified schematic of LM1202's video amplifier input stage is shown in *Figure 3*. The 5.4V zener diode, Q1, Q6 and R2 bias the base of Q7 at 2.6V. The AC coupled video signal applied to pin 6 is referenced to the 2.6V bias voltage. Transistor Q7 buffers the video signal, V_{IN}, and Q8 converts the voltage to current. The AC collector current through Q8 is $I_{C8} = V_{IN}/R9$. Under maximum gain condition, transistors Q9 and Q11 are off and all of I_{C8} flows through the load resistors R10 and R11. The maximum signal gain at the base of Q13 is, $A_{V1} = -(R10 + R11)/R9 = -2$. Signal attenuation is achieved by varying the base drive to the differential pairs Q9, Q10 and Q11, Q12 thereby unbalancing the collector currents through the transistor pairs. Base of Q10 is biased at 5.3V by externally connecting pin 1 to pin 20 through a 100Ω resistor. Pin 2 is connected to pin 3 through a 100Ω resistor. Adjusting the contrast voltage at



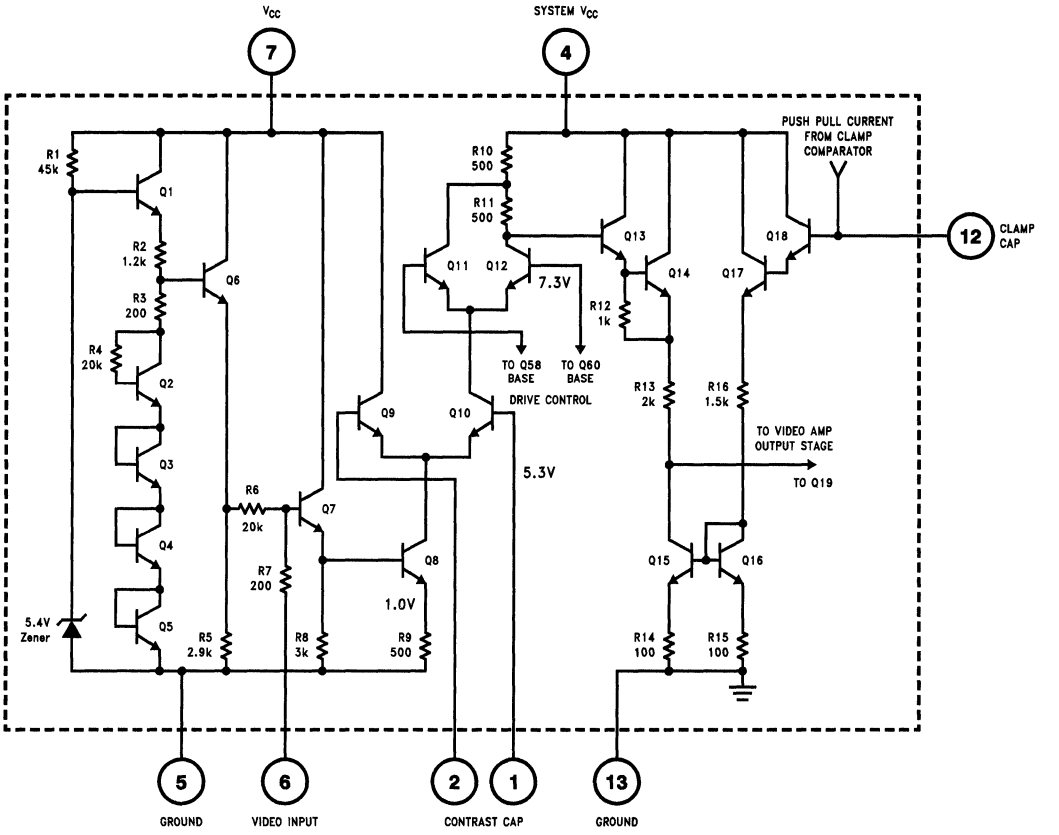
TL/H/11440–3

FIGURE 2. Block Diagram of the LM1202 Video Amplifier with Contrast and Brightness (Black Level) Control

Circuit Description (Continued)

pin 8 produces a control voltage at pin 3 which drives the base of Q9. By varying the voltage at the base of Q9, Q8's collector current (I_{C8}) is diverted away from the load resistors R10 and R11, thereby providing signal attenuation. Maximum attenuation is achieved when all of I_{C8} flows through Q9 and no current flows through the load resistors.

The differential pair Q11 and Q12 provide drive control. Q12's base is internally biased at 7.3V. Adjusting the voltage at the drive control input (pin 9) produces a control voltage at the base of Q11. With Q9 off and Q12 off, all of I_{C8} flows through R10, thus providing a gain of $A_{V1} = -(R10/R9) \times V_{IN} = -1$. Drive control thus provides a 6 dB attenuation range.



TL/H/11440–4

FIGURE 3. Simplified Schematic of the LM1202 Video Amplifier Input Stage

Circuit Description (Continued)

VIDEO AMPLIFIER SECTION (Output Stage)

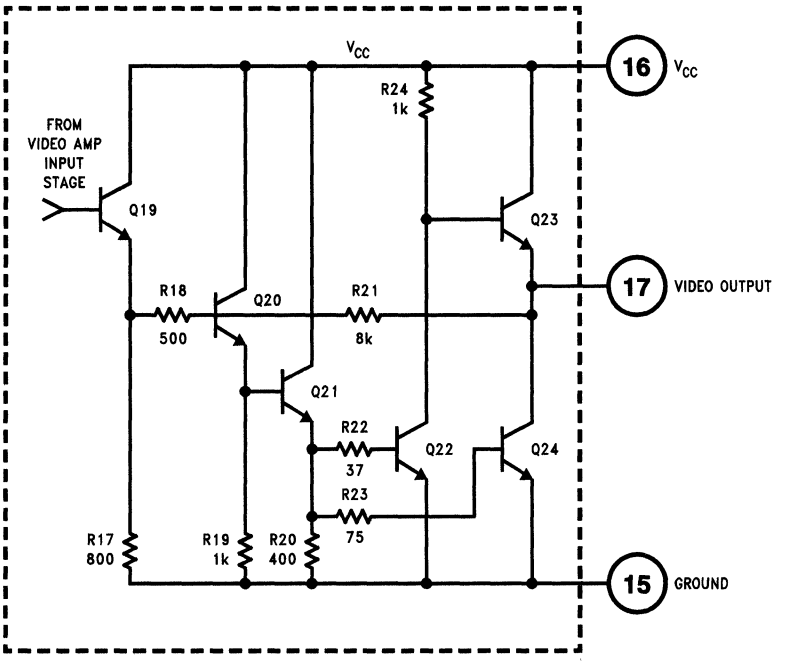
A simplified schematic of LM1202's video amplifier output stage is shown in *Figure 4*. The output stage is the second gain stage. Ideally the gain of the second gain stage would be $A_{V2} = -R21/R18 = -16$. Because of the output stage's low open loop gain, the gain is approximately $A_{V2} = -10$. Thus the maximum gain of the video amplifier is $A_V = A_{V1} \times A_{V2} = 20$. Transistors Q23 and Q24 provide a push-pull drive to the load. The output voltage can swing from 0.2V to 10V.

CONTRAST CONTROL SECTION

A simplified schematic of LM1202's contrast control section is shown in *Figure 5*. A 0V to 4V DC voltage is applied at the contrast input (pin 8). Transistors Q29, Q30 and Q34 buffer and level shift the contrast voltage to the base of Q36. The voltage at the emitter of Q36 equals the contrast voltage (V_{cont}) and the current through Q36's collector is given by $I_{C36} = V_{cont}/R28$.

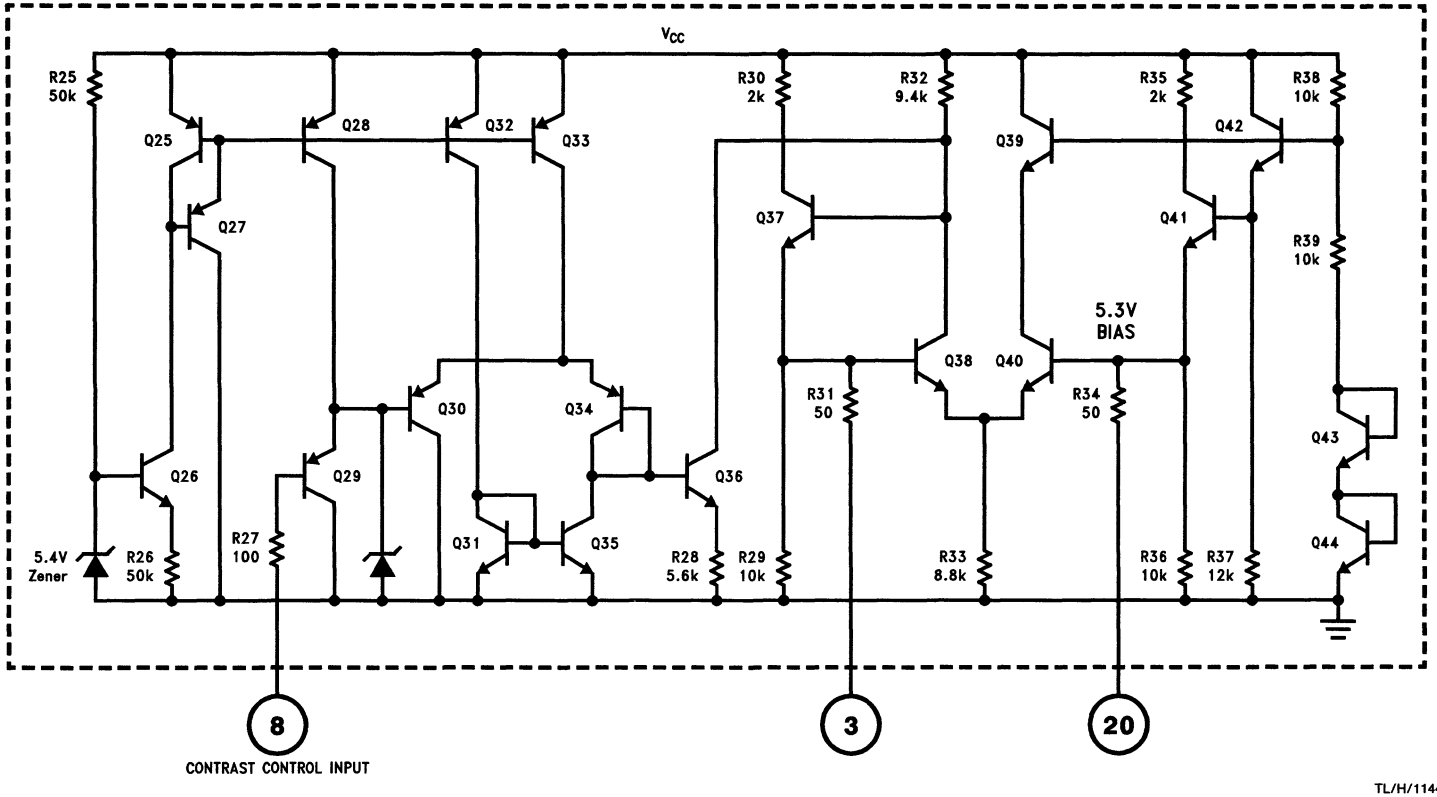
Transistor Q36's collector current is used to unbalance the current through the differential pair comprised of Q38 and Q40. Q40's base is internally biased at 5.3V and made available at pin 20. Pin 20 is externally connected to pin 1 through a 100Ω resistor (see *Figures 2* and *3*). The base of Q38 (pin 3) is externally connected to pin 2 through a 100Ω resistor (see *Figures 2* and *3*). With $V_{cont} = 2V$, the differential pair (Q38, Q40) is balanced and the voltage at pins 1 and 2 is 5.3V. Under this condition, Q8's collector current is equally split between Q9 and Q10 (see *Figure 3*) and the amplifier's gain is half the maximum gain. If contrast voltage at pin 8 is greater than 2V then Q36's collector current increases, thus pulling Q38's collector node lower and consequently moving Q38's base below 5.3V. With pin 2 at a lower voltage than pin 1, current through Q10 (see *Figure 3*) increases and the amplifier's gain increases. With $V_{cont} = 4V$, the amplifier's gain is maximum.

If the contrast voltage at pin 8 is less than 2V then Q36's collector current decreases and Q38's base is pulled above 5.3V. With pin 2 voltage greater than pin 1 voltage, less current flows through Q10 (see *Figure 3*), consequently the amplifier's gain decreases. With $V_{cont} = 0V$, the amplifier's gain is minimum (i.e., maximum attenuation).



TL/H/11440–5

FIGURE 4. Simplified Schematic of LM1202 Video Amplifier Output Stage



TL/H/11440–6

FIGURE 5. Simplified Schematic of LM1202 Contrast Control

Circuit Description (Continued)

DRIVE CONTROL SECTION

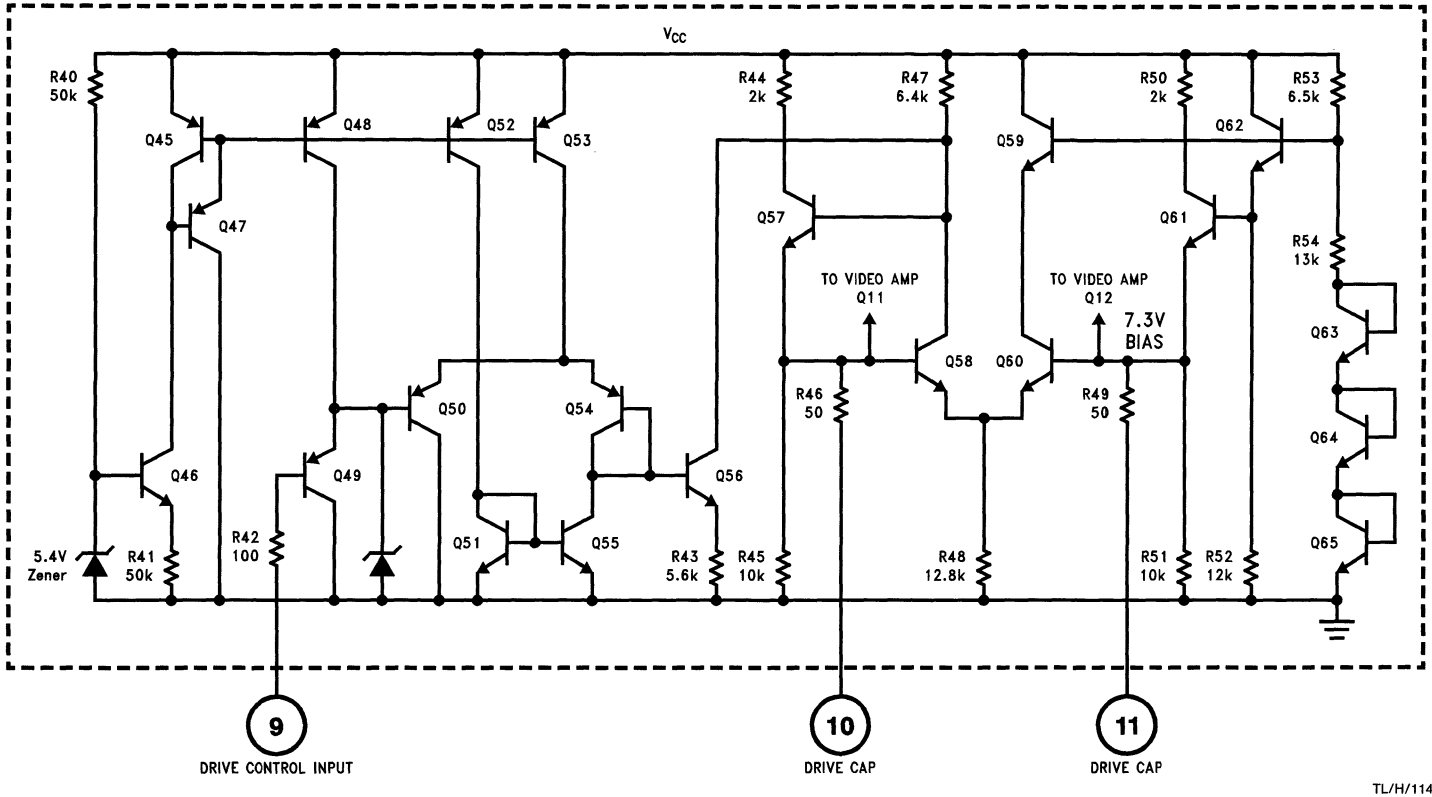
A simplified schematic of the LM1202's drive control section is shown in *Figure 6*. A 0V to 4V DC voltage is applied at the drive control input (pin 9). Transistors Q49, Q50 and Q54 buffer and level shift the contrast voltage to the base of Q56. The voltage at the emitter of Q56 equals the drive voltage, V_{drive} and the current through Q56's collector is given by $I_{C56} = V_{drive}/R43$.

Transistor Q56's collector current is used to unbalance the current through the differential pair comprised of Q58 and Q60. Q60's base is internally biased at 7.3V and connected to the base of Q12 (see *Figure 3*). Q58's base is internally connected to the base of Q11 (see *Figure 3*). With V_{cont} = 2V, the differential pair (Q58, Q60) is balanced and the voltage at the bases of Q11 and Q12 is 7.3V. Under this condition, Q10's collector current is equally split between Q11 and Q12 (see *Figure 3*). If the drive voltage at pin 9 is greater than 2V then Q56's collector current increases, thus pulling Q58's collector node lower and consequently moving Q58's base below 7.3V. With base of Q11 below 7.3V, current through Q12 (see *Figure 3*) increases and the amplifier's gain increases. With V_{drive} = 4V, the amplifier's gain is maximum under maximum contrast condition (i.e., V_{cont} = 4V).

If the drive voltage at pin 8 is less than 2V then Q56's collector current decreases and Q58's base is pulled above 7.3V. With base of Q11 greater than 7.3V, less current flows through Q12 (see *Figure 3*), consequently the amplifier's gain decreases. With V_{drive} = 0V, the amplifier's gain is 6 dB less than the maximum gain.

CLAMP GATE AND CLAMP COMPARATOR SECTION

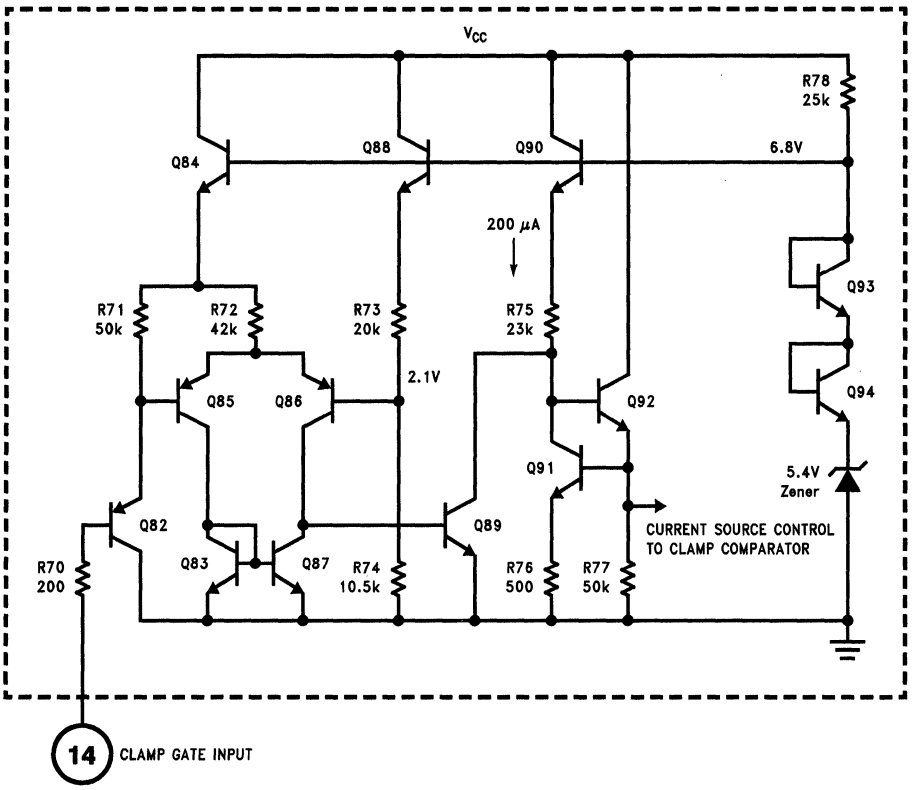
Figures 7 and *8* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 7)* consists of a PNP input buffer transistor (Q82), a PNP emitter coupled pair (Q85 and Q86) referenced on one side to 2.1V and an output switch transistor Q89. When the clamp gate input at pin 14 is high (> 1.5V) the Q89 switch is on and shunts the 200 μA current from current source Q90 to ground. When pin 14 is low (< 1.3V) the Q89 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q91 and Q75 (see *Figure 8*). Consequently the clamp comparator comprised of the differential pair Q74 and Q77 is enabled. The input of the clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitor externally connected from pin 12 to ground. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R63) with a value one half that of R60 or R68 is connected between the bases of Q71 and Q79. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC}.



TL/H/11440–7

FIGURE 6. Simplified Schematic of the LM1202 Drive Control

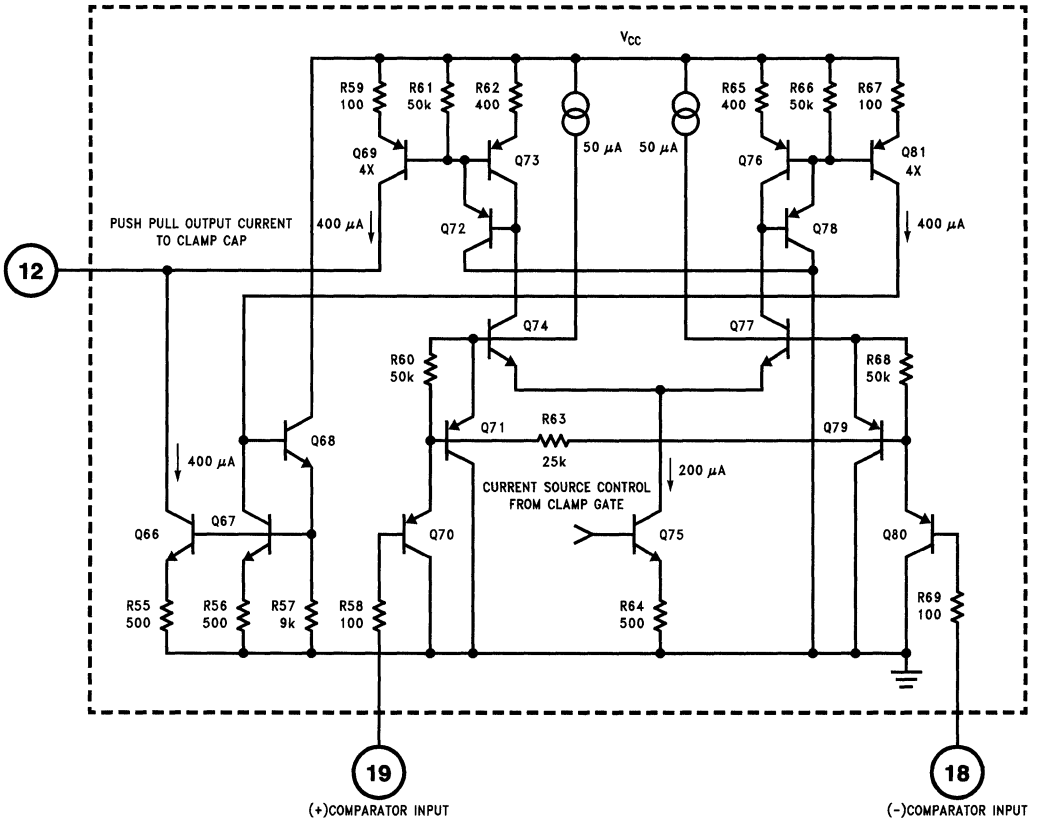
Circuit Description (Continued)



TL/H/11440–8

FIGURE 7. Simplified Schematic of the LM1202 Clamp Gate Circuit

Circuit Description (Continued)



TL/H/11440–9

FIGURE 8. Simplified Schematic of the LM1202 Clamp Comparator Circuit

Applications of the LM1202

SINGLE VIDEO CHANNEL

A typical application for a single video channel is shown in *Figure 9*. The video signal is AC coupled to pin 6. The LM1202 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifier's gain is minimum (i.e., maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval (see *Figure 2*). The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A 510Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510Ω.

RGB VIDEO PREAMPLIFIER

Figure 10 shows an RGB video preamplifier circuit using three LM1202s. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC-coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC-coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 to the black level voltage by using a voltage divider at pin 19.

Applications of the LM1202 (Continued)

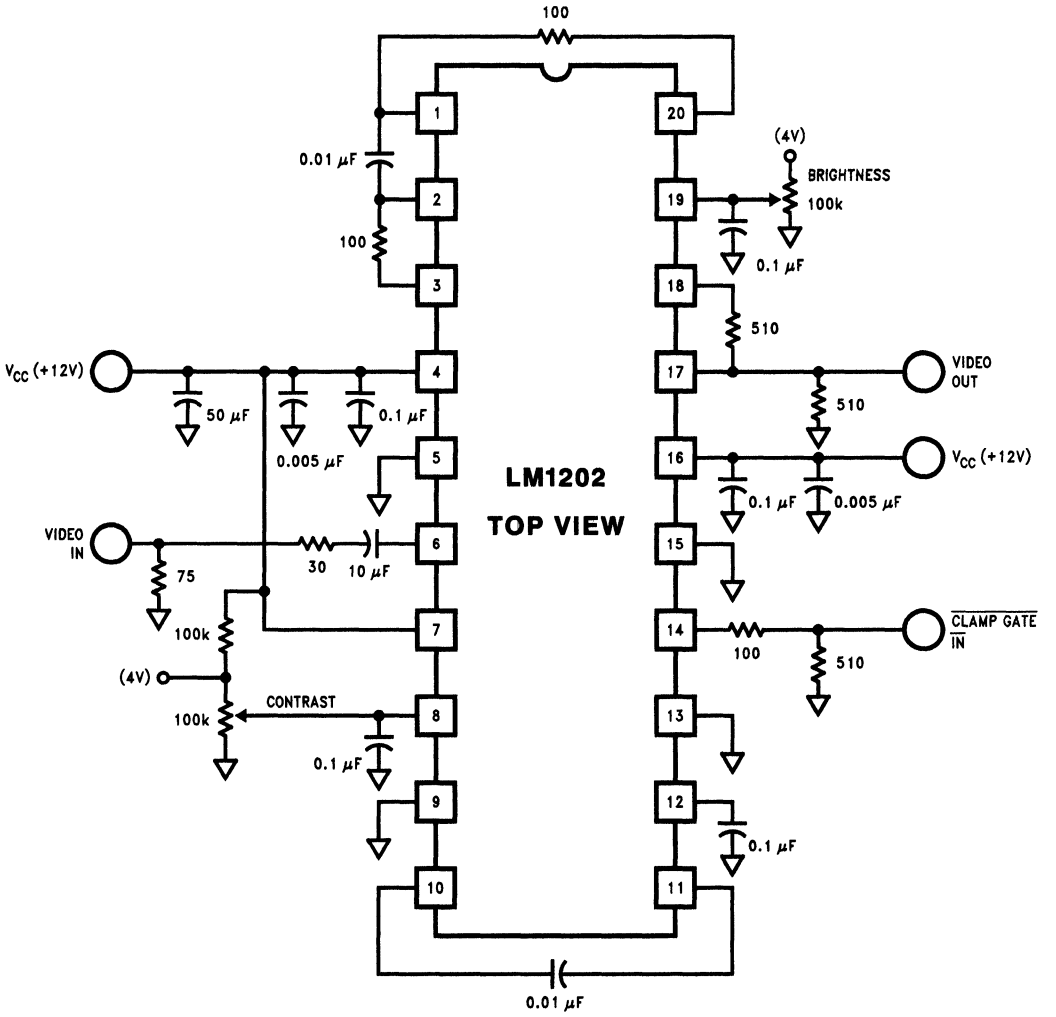


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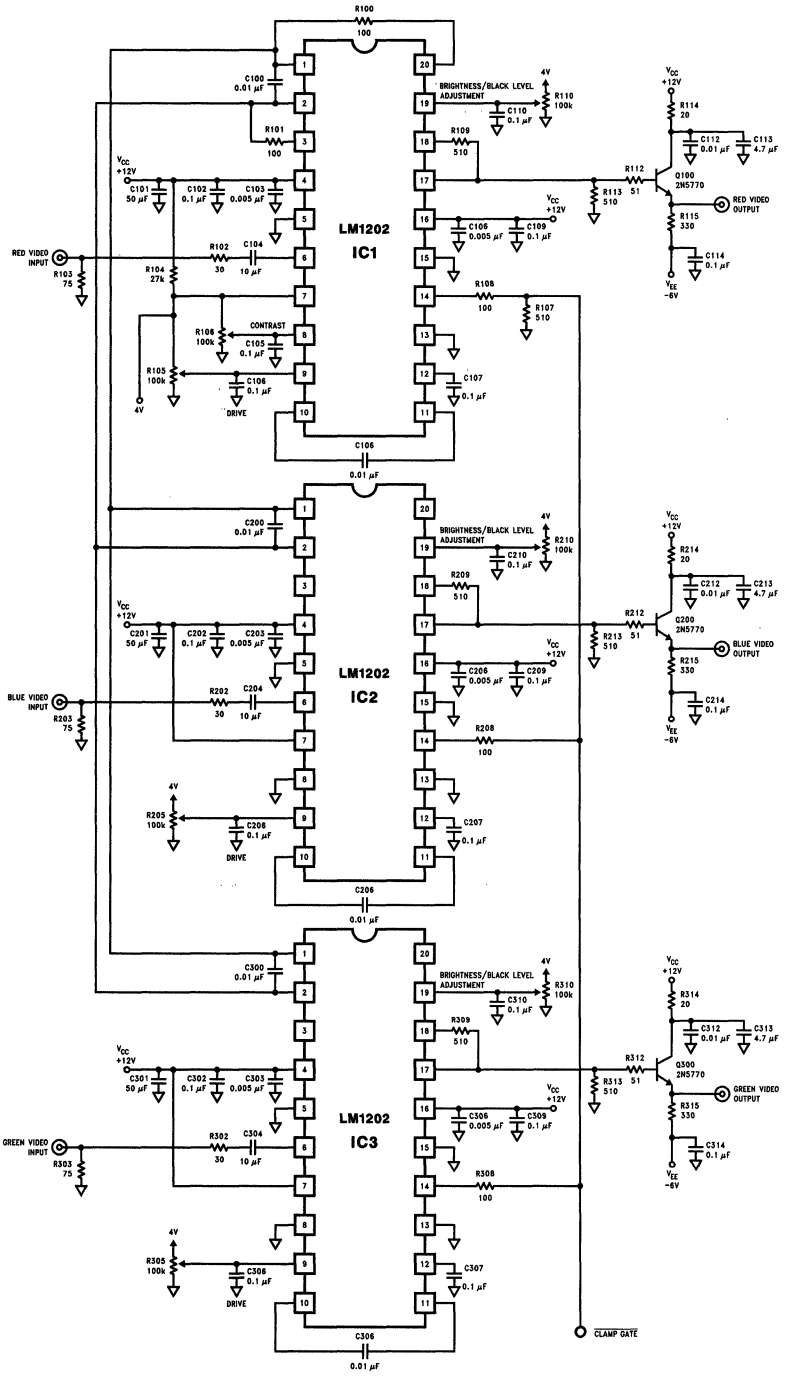
FIGURE 9. Typical LM1202 Application (Single Video Channel)

Applications of the LM1202 (Continued)



TL/H/11440–11

FIGURE 10. Typical RGB Application with Contrast, Drive and Black Level (Cutoff) Control

Power Down Characteristics

The LM1202 includes a built-in power down spot killer to prevent a flash on the screen upon power down. The LM1202's output voltage decreases as the device is being powered down, thus preventing a flash on the screen. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter-than-white level at the output of the CRT driver, thus causing a flash on the screen.

PC Board Layout Considerations

For optimum performance and stable operation, a double-sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. For suggestions on optimum PC board layout, please see the reference section below.

Reference

Ott, Henry W, *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, New York, 1976.

National Semiconductor

LM1203 RGB Video Amplifier System

General Description

The LM1203 is a wideband video amplifier system intended for high resolution RGB color monitor applications. In addition to three matched video amplifiers, the LM1203 contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain (Av = 4 to 10) as well as providing trim capability. The LM1203 also contains a voltage reference for the video inputs. For high resolution monochrome monitor applications see the LM1201 Video Amplifier System datasheet.

Features

- Three wideband video amplifiers (70 MHz @ −3dB)
- Inherently matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for independent gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram

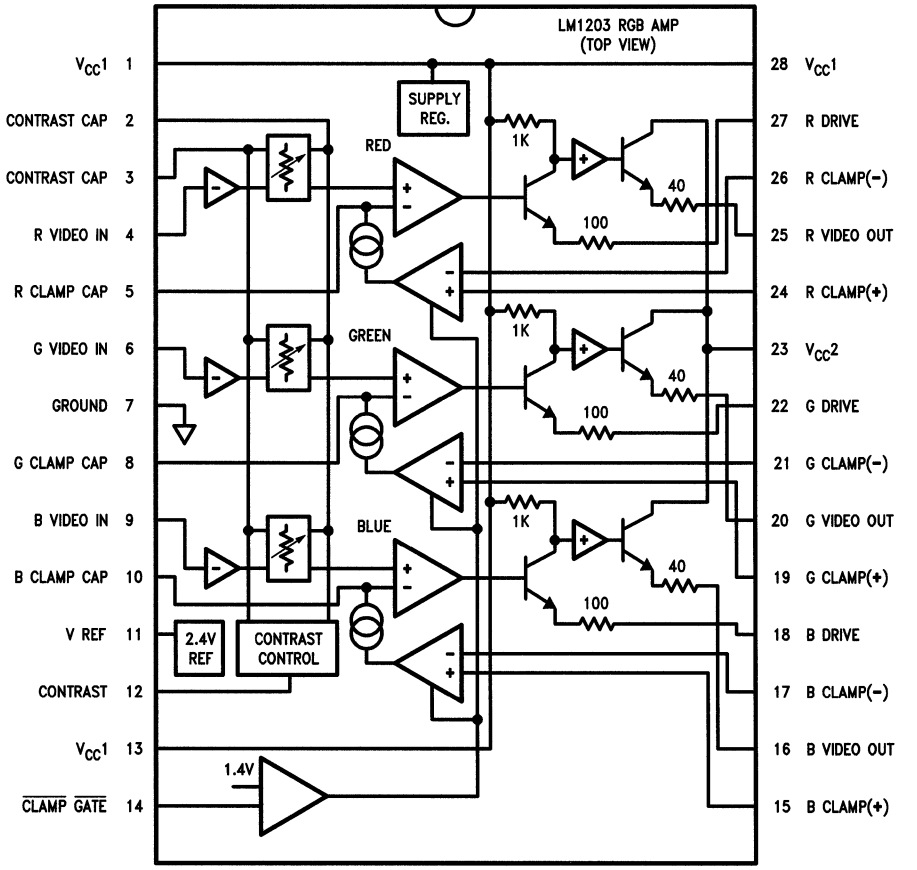


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FIGURE 1
Order Number LM1203N
See NS Package Number N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 1, 13, 23, 28 (Note 1) 13.5V

Voltage at Any Input Pin, V_{IN} $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current, I16, 20 or 25 28 mA

Power Dissipation, P_D 2.5W

(Above 25°C) Derate Based on θ_{JA} and T_J

Thermal Resistance, θ_{JA} 50°C/W

Junction Temperature, T_J 150°C

Operating Temperature Range, T_A 0°C to +70°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Lead Temperature, (Soldering, 10 sec.) 265°C

ESD susceptibility 1 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics

See Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$

DC Static Tests

S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Label	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Is	Supply Current	V_{CC} 1 only	73	90.0		mA(max)
V11	Video Input Reference Voltage		2.4	2.2		V(min)
				2.6		V(max)
Ib	Video Input Bias Current	Any One Amplifier	5.0	20		μA(max)
V14 l	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8		V(max)
V14 h	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0		V(min)
I14 l	Clamp Gate Low Input Current	V14 = 0V	−0.5	−5.0		μA(max)
I14 h	Clamp Gate High Input Current	V14 = 12V	0.005	1		μA(max)
Iclamp+	Clamp Cap Charge Current	V5, 8 or 10 = 0V	850	500		μA(min)
Iclamp−	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−850	−500		μA(min)
Vol	Video Output Low Voltage	V5, 8 or 10 = 0V	0.9	1.25		V(max)
Voh	Video Output High Voltage	V5, 8 or 10 = 5V	8.9	8.2		V(min)
ΔVo(2V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 2V	±0.5	±50		mV(max)
ΔVo(4V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 4V	±0.5	±50		mV(max)

AC Dynamic Tests

S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Av max	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mVp-p	6.0	4.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, V12 = 5V	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, V12 = 2V	−40			dB
Av match	Absolute gain match @ Av max	V12 = 12V (Note 5)	±0.5			dB
ΔAv track1	Gain change between amplifiers	V12 = 5V (Notes 5, 8)	±0.1		±0.5	dB(max)
ΔAv track2	Gain change between amplifiers	V12 = 2V (Notes 5, 8)	±0.3		±0.7	dB(max)
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 Vp-p	0.5			%
f (−3 dB)	Video Amplifier Bandwidth (Notes 4, 6)	V12 = 12V, V_O = 100 mV_{rms}	70			MHz
t_r	Output Rise Time (Note 4)	V_O = 4 Vp-p	5			ns
t_f	Output Fall Time (Note 4)	V_O = 4 Vp-p	7			ns

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated (Continued)

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Vsep 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 7)	−65			dB
Vsep 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 4, 7)	−46			dB

Note 1: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

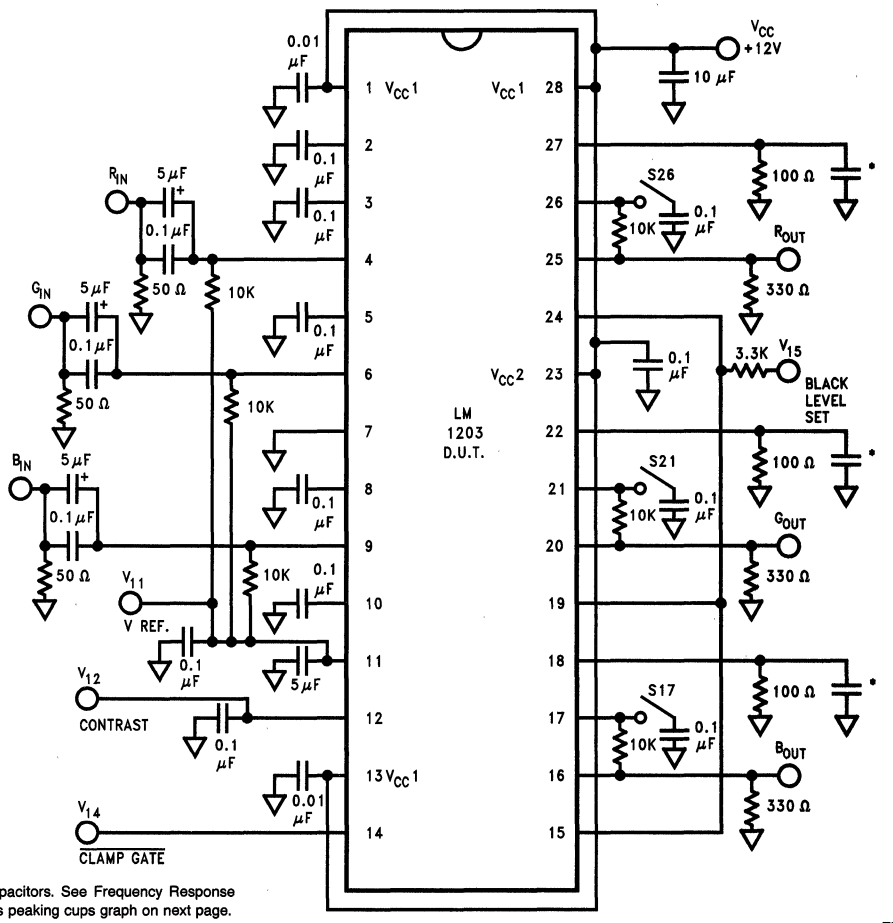
Note 4: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video Amplifier 10 MHz isolation test also requires this printed circuit board.

Note 5: Measure gain difference between any two amplifiers. V_{IN} = 1 Vp-p.

Note 6: Adjust input frequency from 10 kHz (Av_{max} ref level) to the −3 dB corner frequency (f −3 dB).

Note 7: Measure output levels of the other two undriven amplifiers relative to driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for Vsep = 10 MHz.

Note 8: ΔAv track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the Contrast Voltage V12 at either 5V or 2V measured relative to an Av max condition V12 = 12V. For example, at Av max the three amplifiers gains might be 17.4 dB, 16.9 dB, and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.



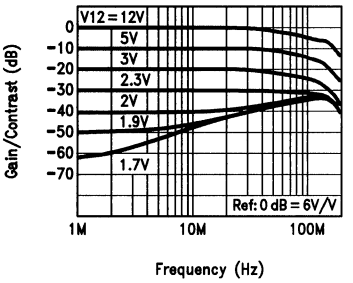
*Peaking capacitors. See Frequency Response using various peaking cups graph on next page.

TL/H/9178–2

FIGURE 2. LM1203 Test Circuit

Typical Performance Characteristics

Contrast vs Frequency



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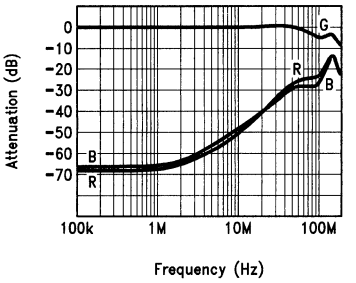
Crosstalk vs Frequency



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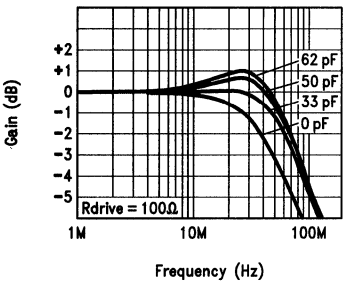
Frequency Response Using Various Peaking Caps



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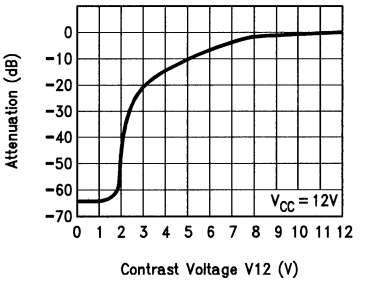
Attenuation vs Contrast Voltage



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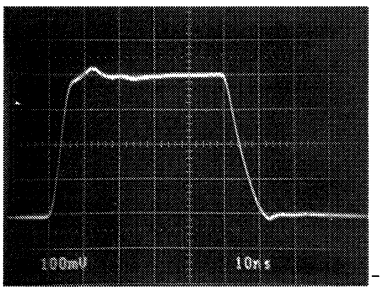
Pulse Response



Rise & Fall Times
Vert. = 1V/Div.
Horiz. = 10 ns/Div.

– – GND

TL/H/9178–15

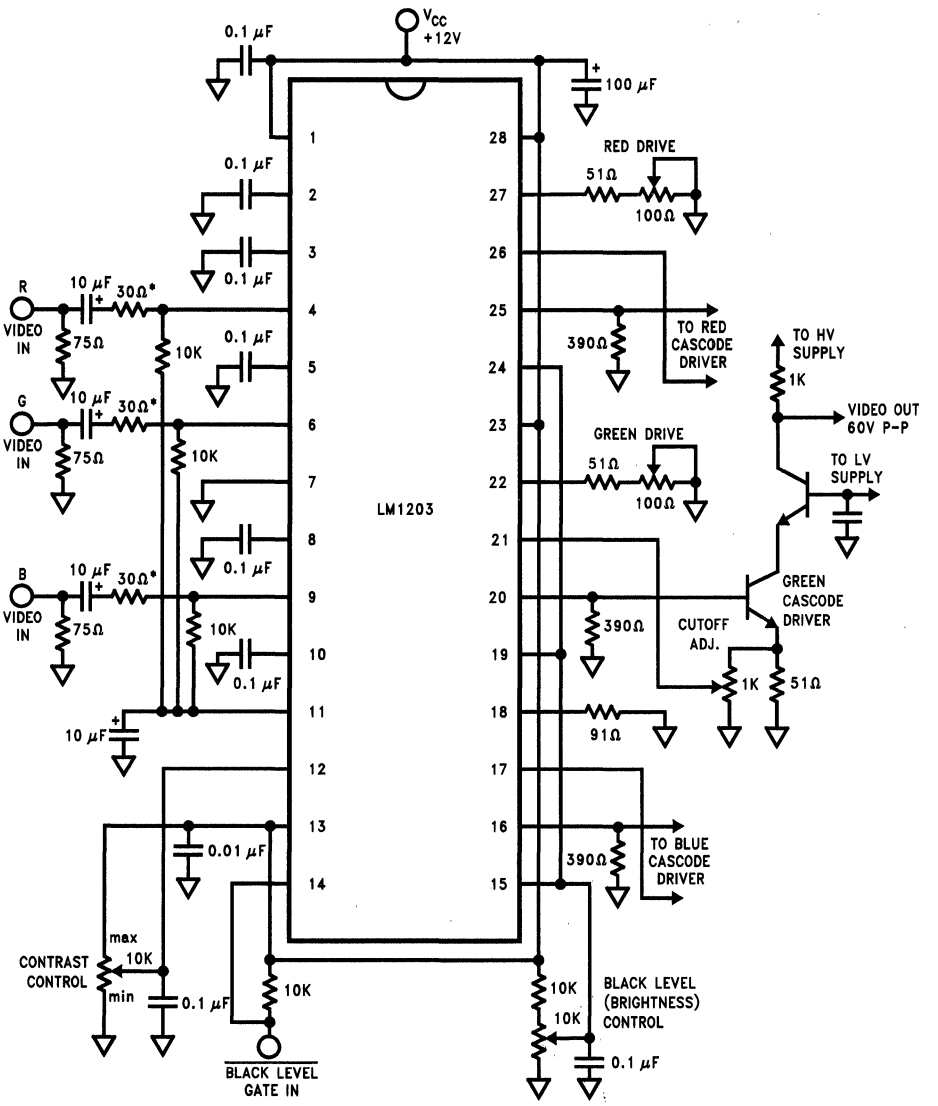


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FIGURE 3. LM1203 Typical Application

* 30Ω resistors are added to the input pins for protection against current surges coming through the 10 μF input capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203 can be increased for EMI considerations.

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac coupled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

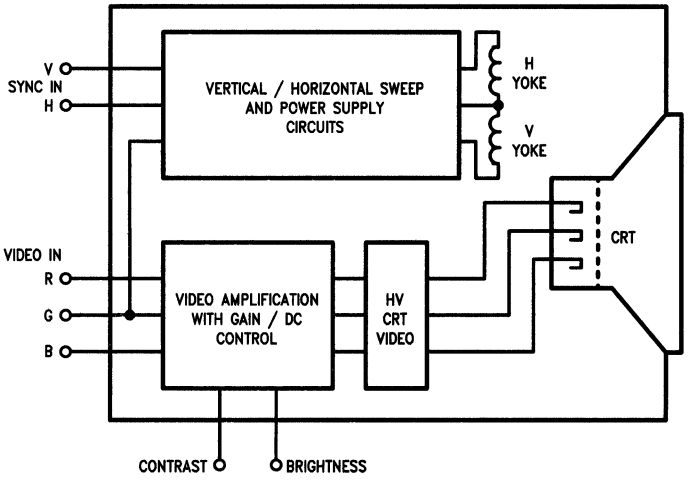

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FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 6 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.4V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC} 1 supply directly or through the 1k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. RF decoupling capacitors are required at pins 2 and 3 to insure high frequency isolation between the three video amplifiers which share these common connections. The black level dc voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

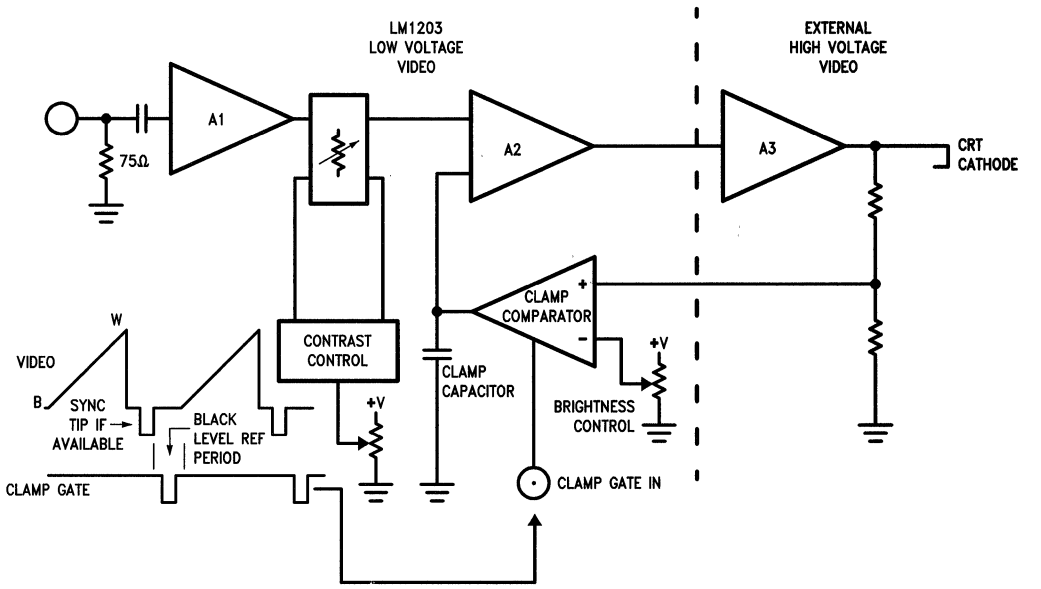

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FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

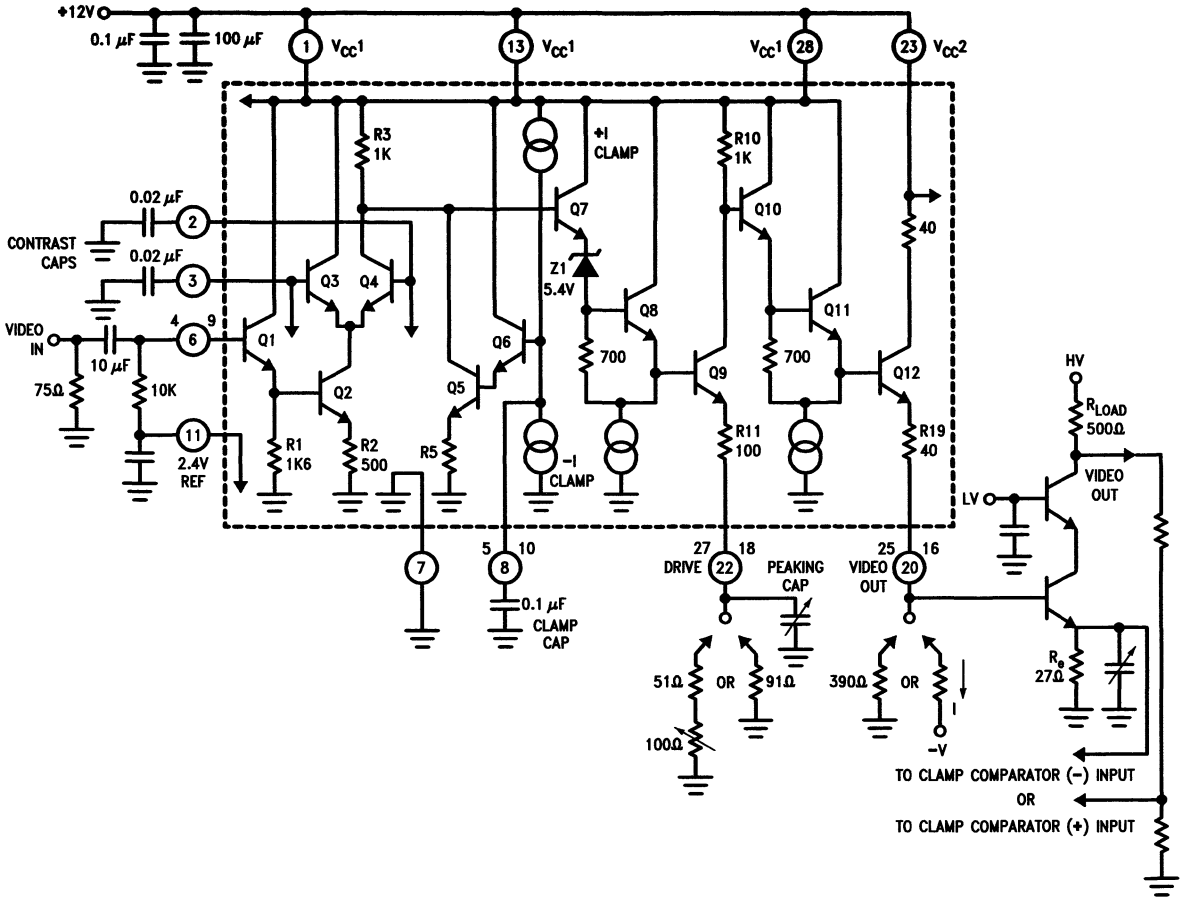

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FIGURE 6. Simplified LM1203 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to trim the Q9 gain of each amplifier to correct for differences in the CRT and high voltage cathode driver gain stages. A small capacitor (33 pF) at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. To use this capacitor and still provide variable gain adjustment, the 51Ω and series 100Ω pot should be used with the red and green drive pins. The 91Ω resistor used with the blue drive pin will set the system gain to approximately 6.2 and allow adjustment of the red and green gains to 6.2 plus or minus 25%. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 40Ω resistor which was included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 390Ω or package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 40Ω resistor. Precautions must be taken to prevent the video output pin from going below ground because IC substrate currents may cause erratic operation. The collector currents from the video output transistors are returned to the power supply at V_{CC} 2 pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC} 1 supply current at 12V. The IC power dissipation contribution of V_{CC} 2 is dependent upon the video output emitter pull down load.

In applications that require video amplifier shut down because of fault conditions detected by monitor protection circuits, pin 11 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control pots and V_{CC}.

Figure 7 shows the internal construction of the pin 11 2.4V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier inputs. The value of the external DC biasing resistors should not be larger than 10 kΩ because minor differences in input bias currents to the individual video amplifiers may cause offsets in gain.

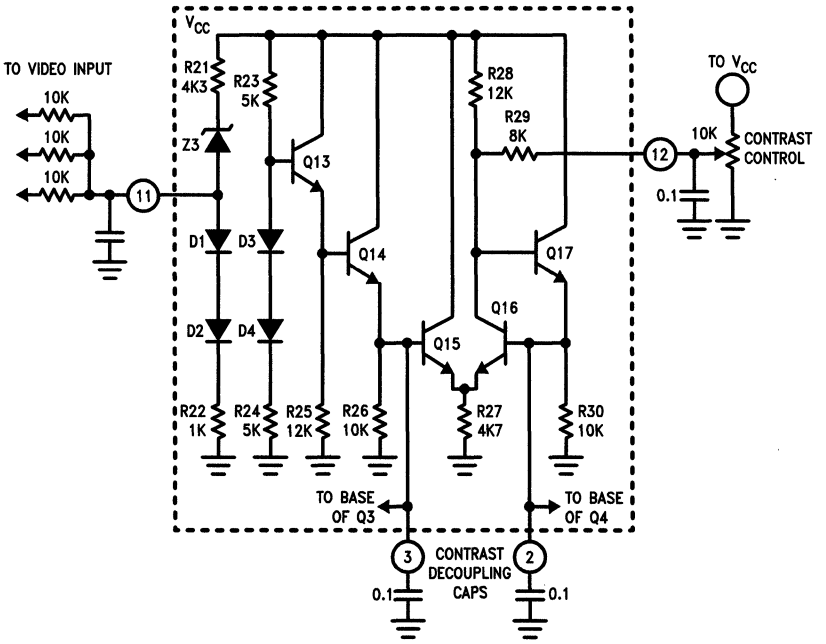

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FIGURE 7. LM1203 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, 24, diodes D3, 4 and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, 16 and feedback transistor Q17 along with resistors R27, 28 establish a diferential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 12. A capacitor should be added from pin 12 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator sections of the LM1203. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, 20) and an output switch (Q21). When the clamp gate input at pin 14 is high (>1.5V) the Q21 switch is on and shunts the I1 850 μA current to ground. When pin 14 is low (<1.3V) the Q21 switch is off and the I1 850 μA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 850 μA current source for the clamp comparator(s). The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitors at pins 5, 8, or 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R34) with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, 25 to approximately 350 mV. The clamp comparator common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

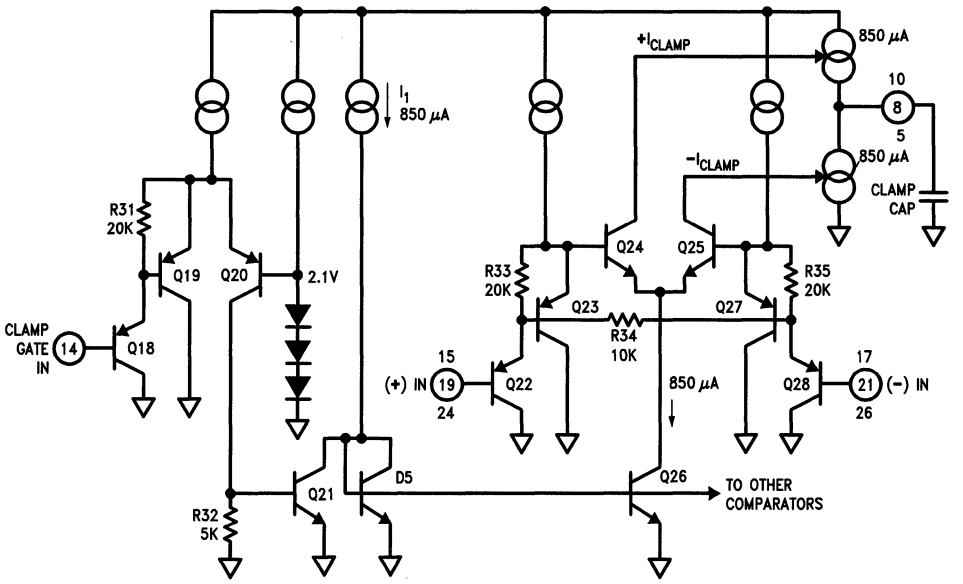

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FIGURE 8. Simplified Schematic of LM1203 Clamp Gate and Clamp Comparator Circuits

Additional Applications of the LM1203

Figure 9 shows how the LM1203 can be set up as a video buffer which could be used in low cost video switcher applications. Pin 14 is tied high to turn off the clamp comparators. The comparator input pins should be grounded as shown. Sync tip (black level if sync is not included) clamping is provided by diodes at the amplifier inputs. Note that the clamp cap pins are tied to the Pin 11 2.4V reference. This was done, along with the choice of 200Ω for the drive pin resistor, to establish an optimum DC output voltage. The contrast control (Pin 12) will provide the necessary gain or attenuation required for channel balancing. Changing the contrast control setting will cause minor DC shifts at the amplifier output which will not be objectionable as the output is AC coupled to the load. The dual NPN/PNP emitter follower will provide a low impedance output drive to the AC coupled 75Ω output impedance setting resistor. The dual 500 μF capacitors will set the low frequency response to approximately 4 Hz.

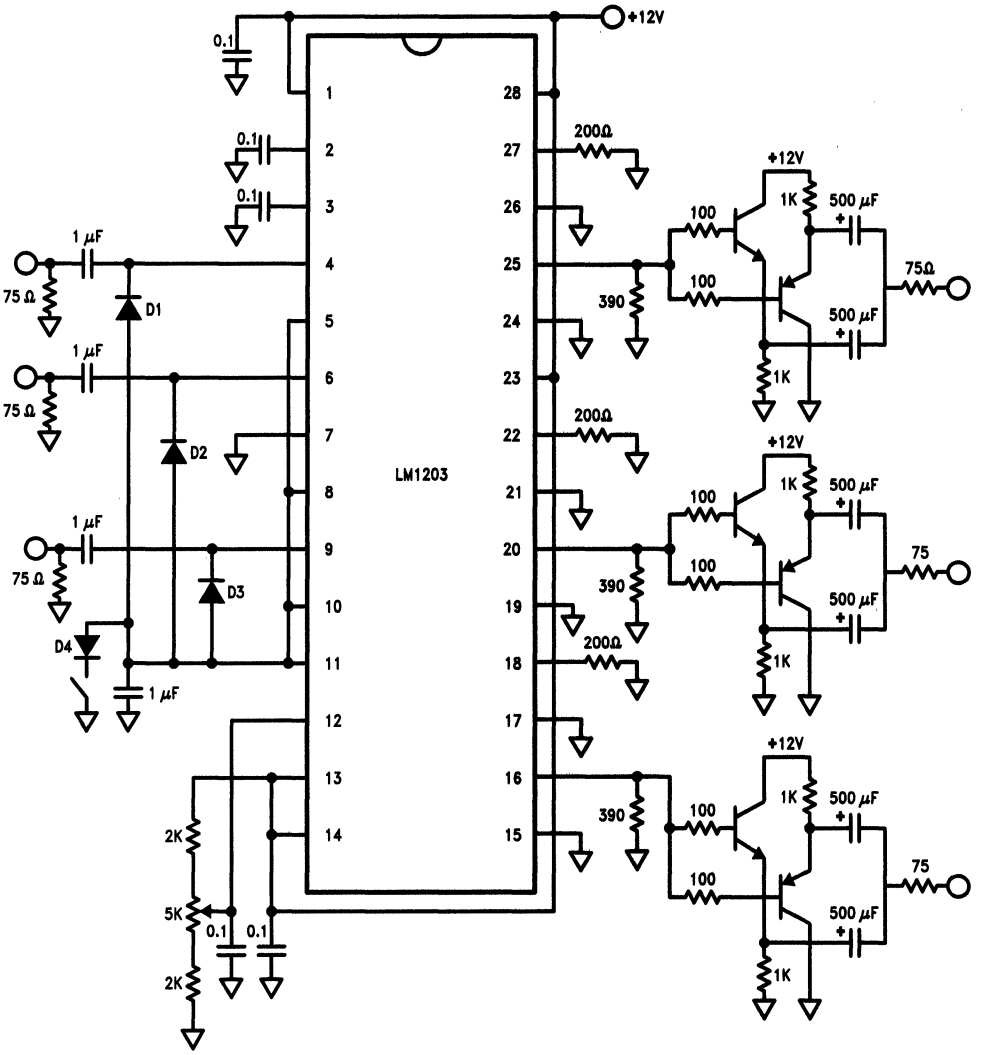

FIGURE 9. RGB Video Buffer with Diode Sync Tip Clamps and 75Ω Cable Driver

Additional Applications of the LM1203 (Continued)

When diode D4 at Pin 11 is switched to ground the input video signals will be DC shifted down and clamped at a voltage near ground (approximately 250 mV). This will disable the video amplifiers and force the output DC level low. The DC outputs from other similarly configured LM1203s could overide this lower DC level and provide the output signals to the 75Ω cable drivers. In this case any additional LM1203s would share the same 390Ω output resistor. The maximum DC plus peak white output voltage should not be allowed to exceed 7V because the "off" amplifier output stage could suffer internal zener damage. See *Figure 3* and text for a description of the internal configuration of the video amplifier.

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

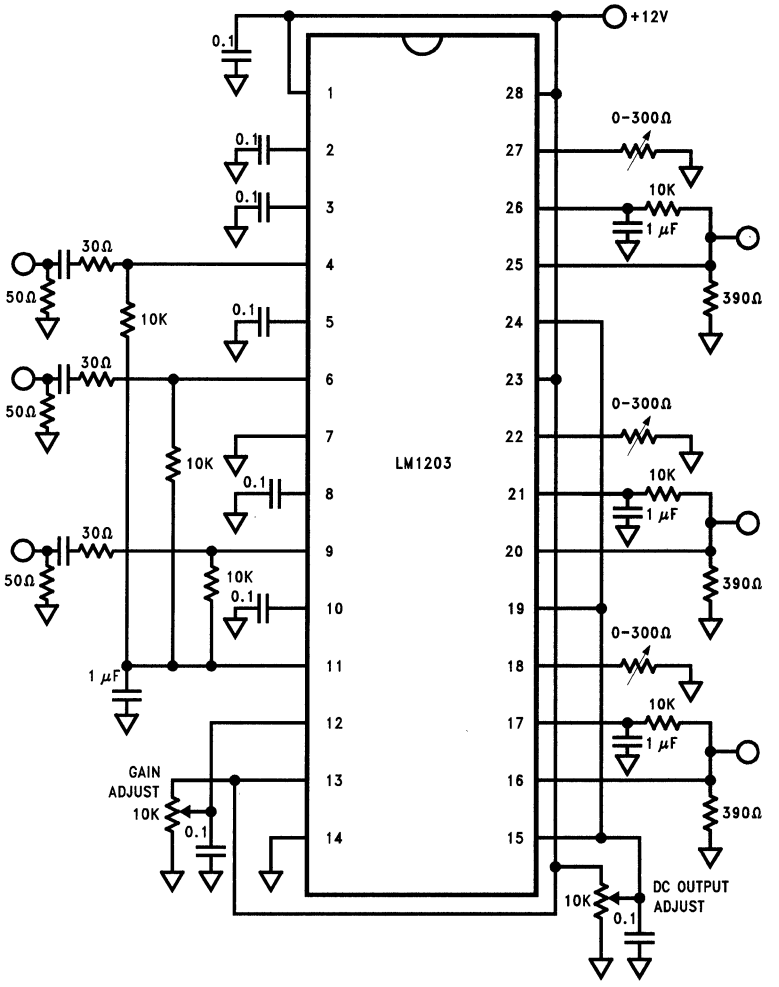

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

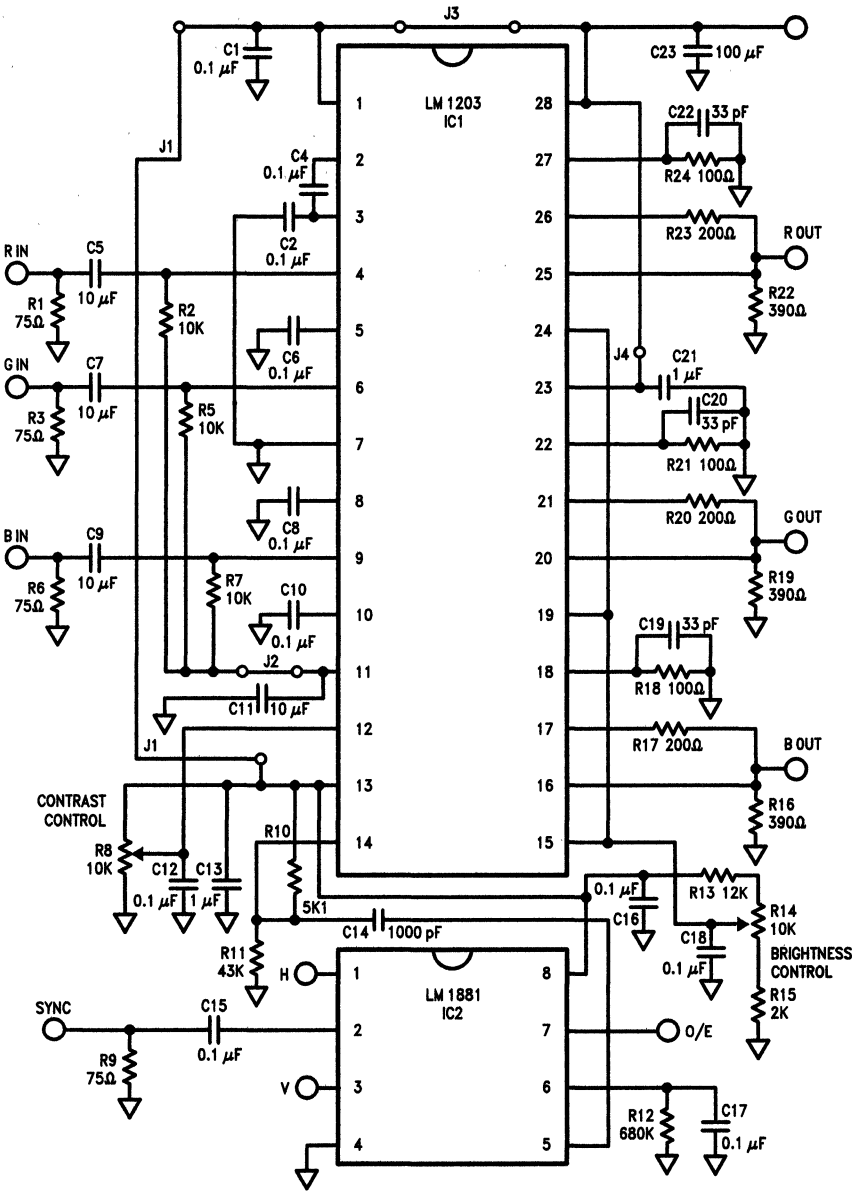

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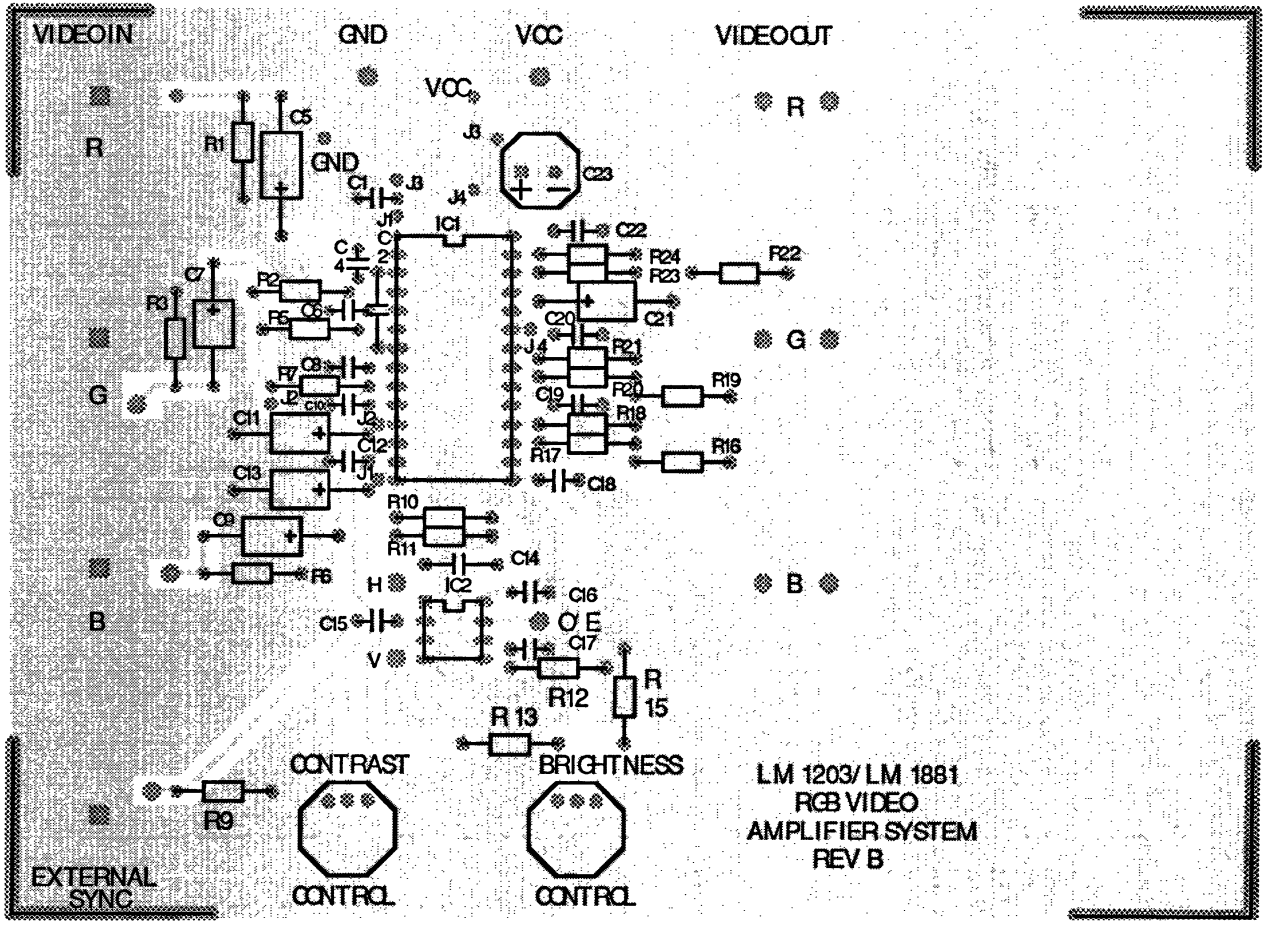
FIGURE 11. LM1203/LM1881 Application Circuit for PC Board

PC Board with Components



TL/H/9178–17

National Semiconductor

LM1203A
150 MHz RGB Video Amplifier System

General Description

The LM1203A is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203A contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203A also contains a voltage reference for the video inputs. The LM1203A is pin and function compatible with the LM1203.

Features

- Three wideband video amplifiers 150 MHz @ −3 dB
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Improvements over LM1203

- 150 MHz vs 70 MHz bandwidth
- V_{OUT} low: 0.15V vs 0.9V
- t_r, t_f: 4 ns vs 7 ns
- Built in power down spot killer

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls

Block and Connection Diagrams

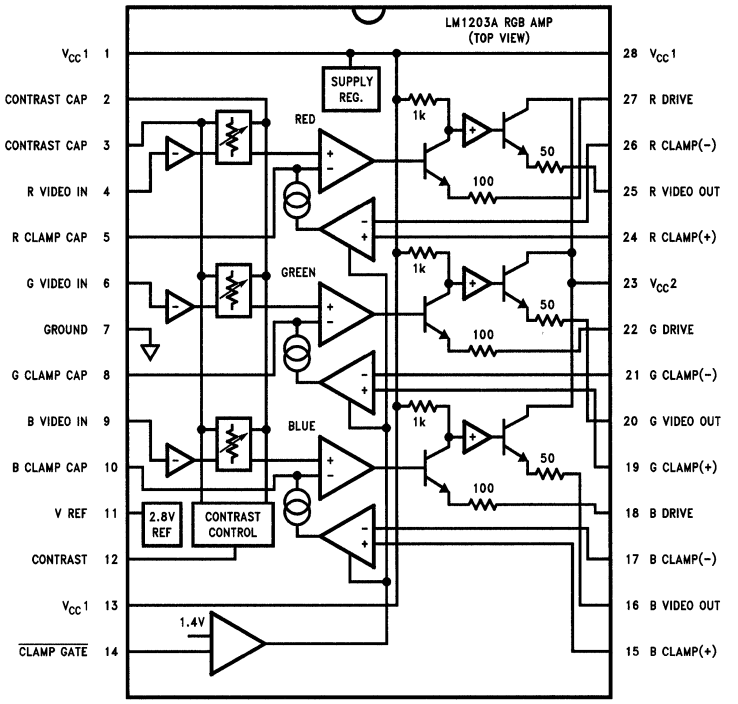


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FIGURE 1

Order Number LM1203AN
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})
Pins 1, 13, 23, 28 (Note 3) 13.5V

Peak Video Output Source Current
(Any One Amp) Pins 16, 20 or 25 28 mA

Voltage at Any Input Pin (V_{IN}) $V_{CC} \geq V_{IN} \geq GND$

Power Dissipation, (P_D) (Above 25°C derate based on θ_{JA} and T_J) 2.5W

Thermal Resistance (θ_{JA}) 50°C/W

Junction Temperature (T_J) 150°C

ESD Susceptibility (Note 4) 2 kV

Storage Temperature −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) 265°C

Operating Ratings (Note 2)

Temperature Range −20°C to +80°C

Supply Voltage (V_{CC}) $10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	$V_{CC1} + V_{CC2}$, $R_L = \infty$ (Note 7)	70	95	mA (max)
V11	Video Input Reference Voltage		2.8	2.5	V (min)
				3.1	V (max)
I_B	Video Input Bias Current	Any One Amplifier	7	20	μA (max)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V (min)
I_{14L}	Clamp Gate Low Input Current	V14 = 0V	−1	−5.0	μA (max)
I_{14H}	Clamp Gate High Input Current	V14 = 12V	0.07	0.2	μA (max)
I_{CLAMP+}	Clamp Cap Charge Current	V5, 8 or 10 = 0V	750	500	μA (min)
I_{CLAMP-}	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−750	−500	μA (min)
V_{OL}	Video Output Low Voltage	V5, 8 or 10 = 0V	0.15	0.5	V (max)
V_{OH}	Video Output High Voltage	V5, 8 or 10 = 5V	7.5	7	V (min)
$\Delta V_{O(2V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 2V	2	±25	mV (max)
$\Delta V_{O(4V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 4V	2	±25	mV (max)

AC Electrical Characteristics

See Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. S17, 21, 26 Closed; V14 = 0V; V15 = 4V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mV_{PP}	6.5	4.5	V/V (min)
$\Delta A_{V\ 5V}$	Attenuation @ 5V	Ref: A_V max, V12 = 5V	−8		dB
$\Delta A_{V\ 2V}$	Attenuation @ 2V	Ref: A_V max, V12 = 2V	−30		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 12V (Note 8)	±0.3		dB
$\Delta A_{V\ track\ 1}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.1		dB
$\Delta A_{V\ track\ 2}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.3		dB
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 V_{PP}	1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} (No External Peaking Capacitor)	100		MHz
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} With 18 pF Peaking Cap from Pins 18, 22 and 27 to GND	150		MHz
t_r	Output Rise Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	3		ns
t_f	Output Fall Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	4		ns
$V_{sep\ 10\ kHz}$	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 12)	−70		dB
$V_{sep\ 10\ MHz}$	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 10, 12)	−50		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with $R_L = \infty$, see *Figure 2's* test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 2V DC, the additional current through V_{CC2} is 18 mA for *Figure 2's* test circuit.

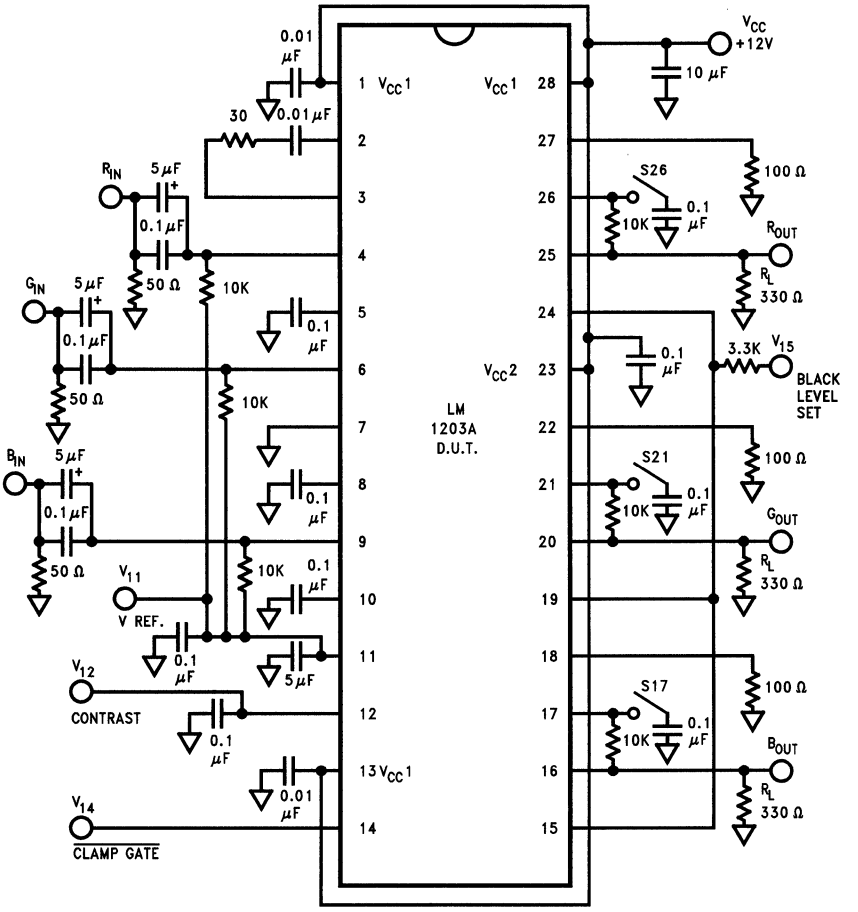
Note 8: Measure gain difference between any two amplifiers. V_{IN} = 1 V_{PP}.

Note 9: $\Delta A_{V\ track}$ is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 5V or 2V measured relative to an A_V max condition, V12 = 12V. For example, at A_V max the three amplifiers' gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

Note 10: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board.

Note 11: Adjust input frequency from 10 kHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

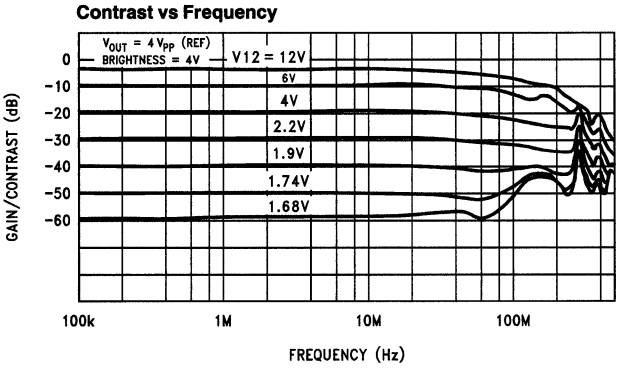
Note 12: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{sep} = 10 MHz.



TL/H/11441–2

FIGURE 2. LM1203A Test Circuit

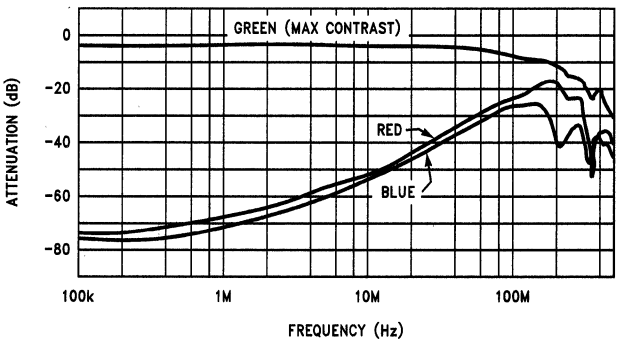
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified



TL/H/11441–3

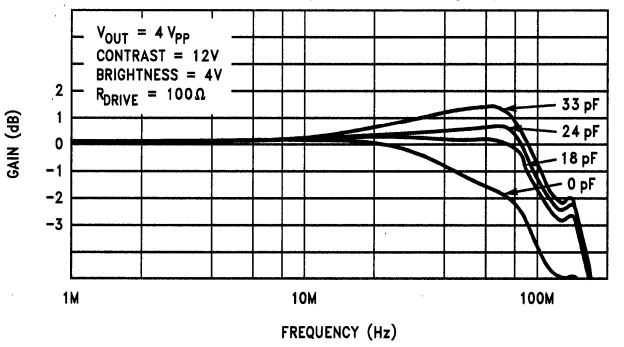
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified (Continued)

Crosstalk vs Frequency



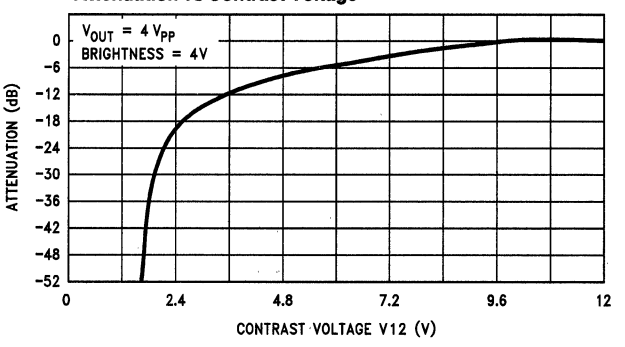
TL/H/11441–4

Frequency Response Using Various Peaking Caps

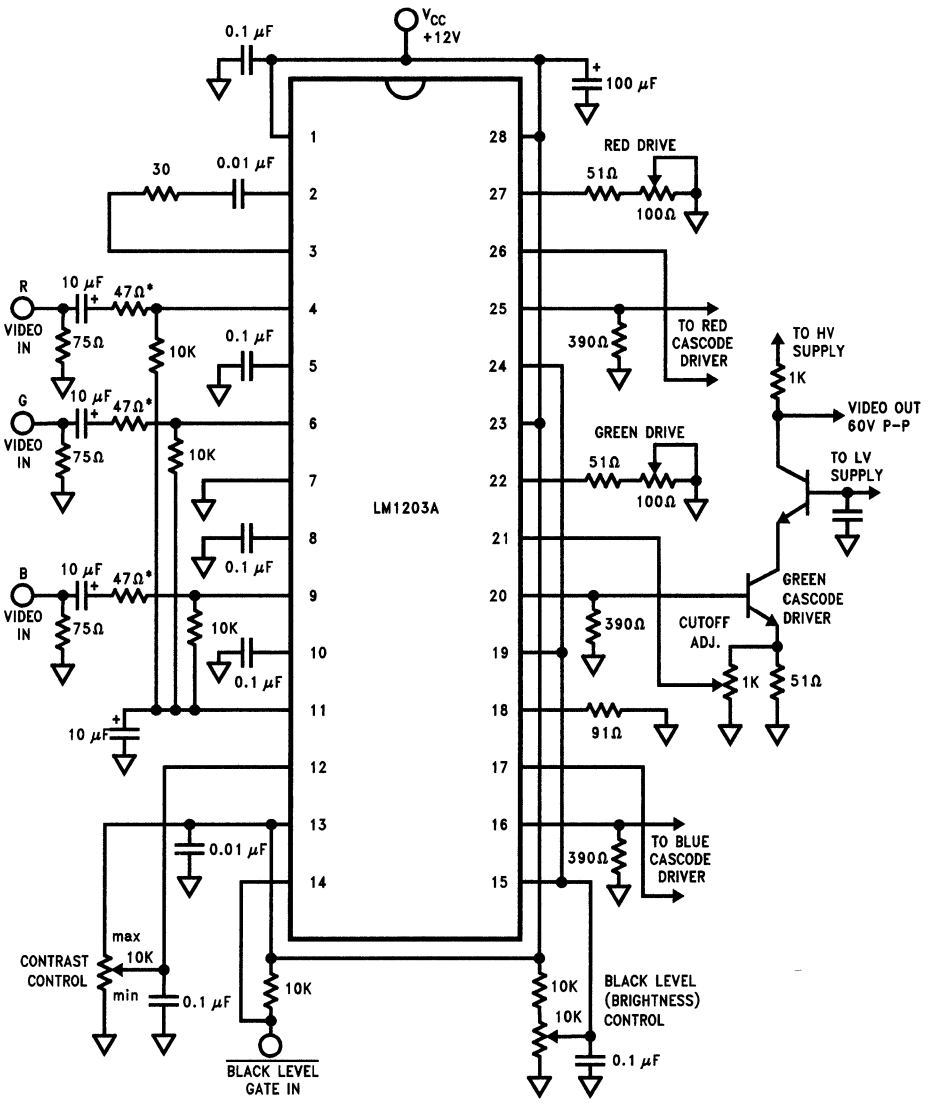


TL/H/11441–5

Attenuation vs Contrast Voltage



TL/H/11441–6



TL/H/11441–7

*47Ω resistors are added to the input pins for protection against current surges coming from the 10 μF capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203A can be increased for EMI considerations.

FIGURE 3. LM1203A Typical Application

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203A which contains the three matched video amplifiers, contrast control and brightness control.

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a DC-operated attenuator which varies the AC gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

VIDEO AMPLIFIER SECTION

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor. DC bias for the video input is through the 10k resistor connected to the 2.8V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. Q2's collector current is then directed to the V_{CC1} supply directly or through the 2k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. This differential DC voltage is generated by the contrast control circuit which is described in the following sections. A 0.01 μF decoupling capacitor in series with a 30Ω resistor is required between pins 2 and 3 to ensure high frequency isolation between the three video amplifiers which share these common connections. The video signal is buffered by Q5 and Q6 and DC level shifted by the voltage drop across R5. The magnitude of the current through R5 is determined by the voltage at pin 8. The voltage at pin 8 is set by the clamp comparator output current which charges or discharges the clamp hold capacitor during the black level period of the video waveform. Transistors Q9 and Q10 are Darlington connected to ensure a minimum discharge of the clamp hold capacitor during the time that the clamp capacitor is gated off. Q7, Q8 and R6 form a current mirror which sets a voltage at the base of Q11. Q11 buffers the video signal to the base of Q12 which provides additional signal gain. The "Drive" pin allows the user to trim the Q12 gain of each amplifier to correct for gain differences in the CRT and high voltage cathode driver gain stages. A small capacitor (several pico-Farads) from the "Drive" pin to ground will cause high frequency peaking and slightly improve the amplifier's bandwidth.

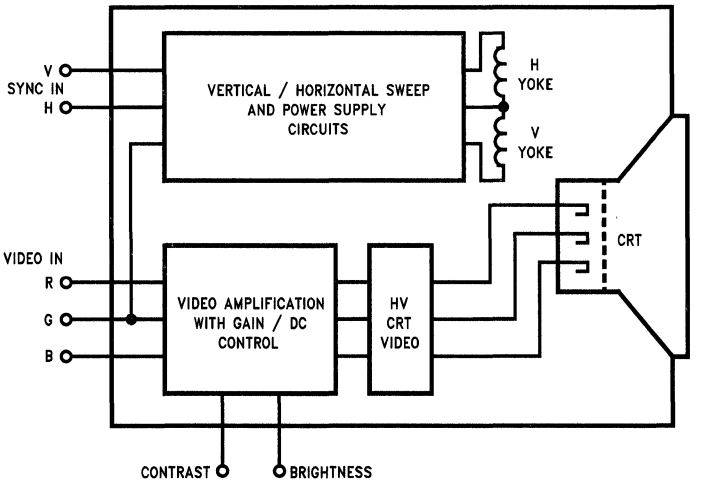
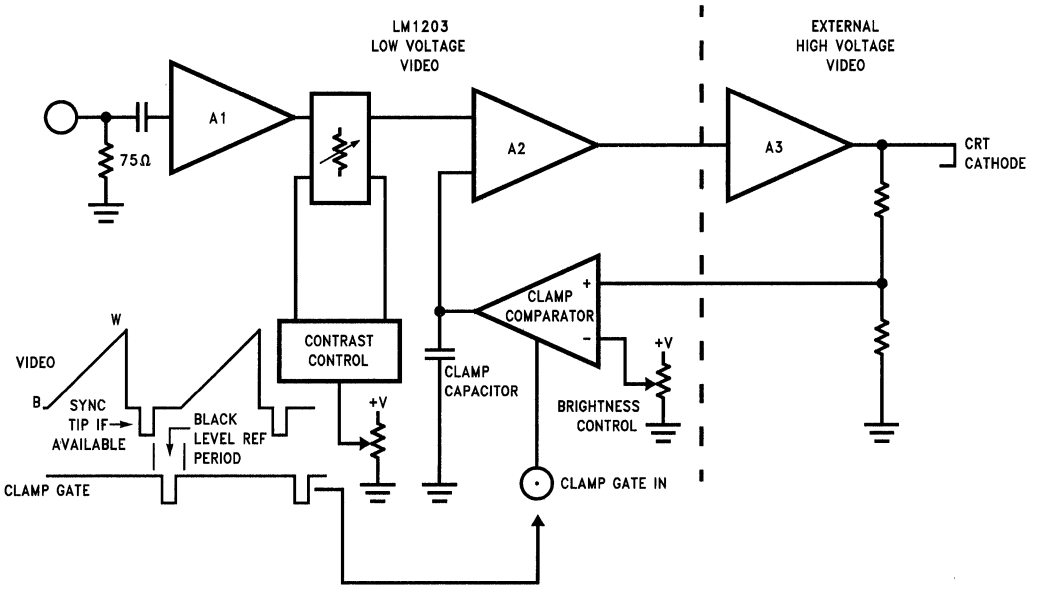


FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description (Continued)

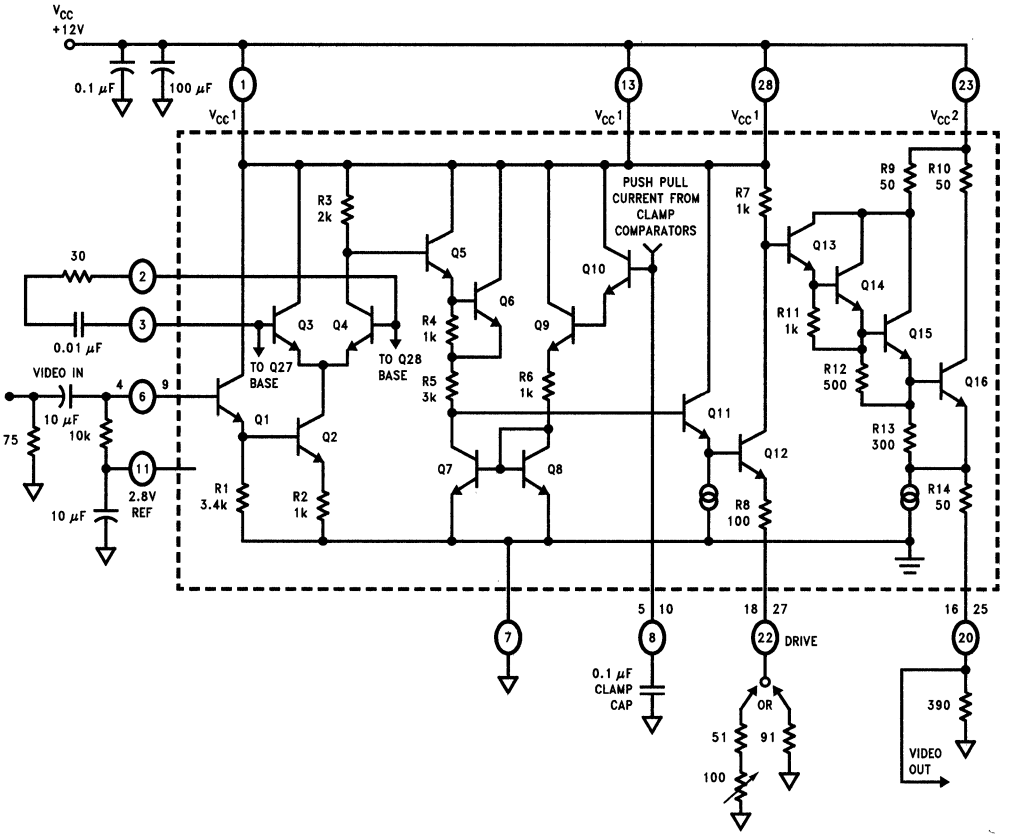
For individual gain adjustment of each video channel, a 51Ω resistor in series with a 100Ω potentiometer should be used with the red and green channel drive pins. A 91Ω resistor used with the blue channel drive pin sets the blue channel amplifier gain at approximately 6.2. The 100Ω potentiometer at the red and green channel drive pins allow a gain of 6.2 with ±25% gain adjustment. The video signal at the collector of Q12 is buffered and level shifted down by Q13, Q14 and Q15 to the base of the output emitter follower Q16. A 50Ω decoupling resistor is included in series with the emitter of Q16 and the video output pin so as to prevent oscillations when driving capacitive loads. An external resistor should be connected between the video output pin and ground. The value of this resistor should not be less than 390Ω or else package power limitations may be exceeded under worst case conditions (high supply voltage, maximum current, maximum temperature). The collector current from the video output transistor of each video channel is returned to the power supply at V_{CC2}, pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC1} and V_{CC2} supply current at 12V supply voltage with no pull down resistor at the output (i.e., $R_L = \infty$, see test circuit *Figure 2*). The IC power dissipation due to V_{CC2} is dependant upon the external video output pull down resistor.



TL/H/11441–9

FIGURE 5. Block Diagram of LM1203A Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)



TL/H/11441–10

FIGURE 6. Simplified Schematic of LM1203A Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

INPUT REFERENCE AND CONTRAST CONTROL SECTION

Figure 7 shows the input reference and contrast control circuitry. A temperature compensated 2.8V reference voltage is made available at pin 11. The external DC biasing resistors shown should not be larger than 10k because minor differences in input bias currents of the individual video amplifiers may cause offsets in gain. *Figure 7* also shows how the contrast control circuit is configured. R21, R22, Q22, Q23 and Q24 establish a low impedance zero TC half supply voltage reference at the base of Q25. The differential amplifier formed by Q27, Q28 and feedback transistor Q29 along with R28 and R29 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q28, a new differential voltage is generated that reflects the change in the ratio of currents in Q27 and Q28. To allow voltage control of the current through Q28, resistor R27 is added between the collector Q28 and pin 12. A capacitor should be connected from pin 12 to ground to prevent noise from the contrast control potentiometer from entering the IC.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 8 and *9* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 8)* consists of a PNP input buffer transistor (Q46), a PNP emitter coupled pair (Q47 and Q49) referenced on one side to 2.1V and an output switch transistor Q53. When the clamp gate input at pin 14 is high (>1.5V) the Q53 switch is on and shunts the 200 μA current from current source Q54 to ground. When pin 14 is low (<1.3V) the Q53 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q55 and Q36 (see *Figure 9*). Consequently the clamp comparator comprised of the differential pair Q35 and Q37 is enabled. The input of each clamp comparator is similar to the clamp gate except than an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitors at pins 5, 8 and 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R37) with a value one half that of R36 or R39 is connected between the bases of Q34 and Q38. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

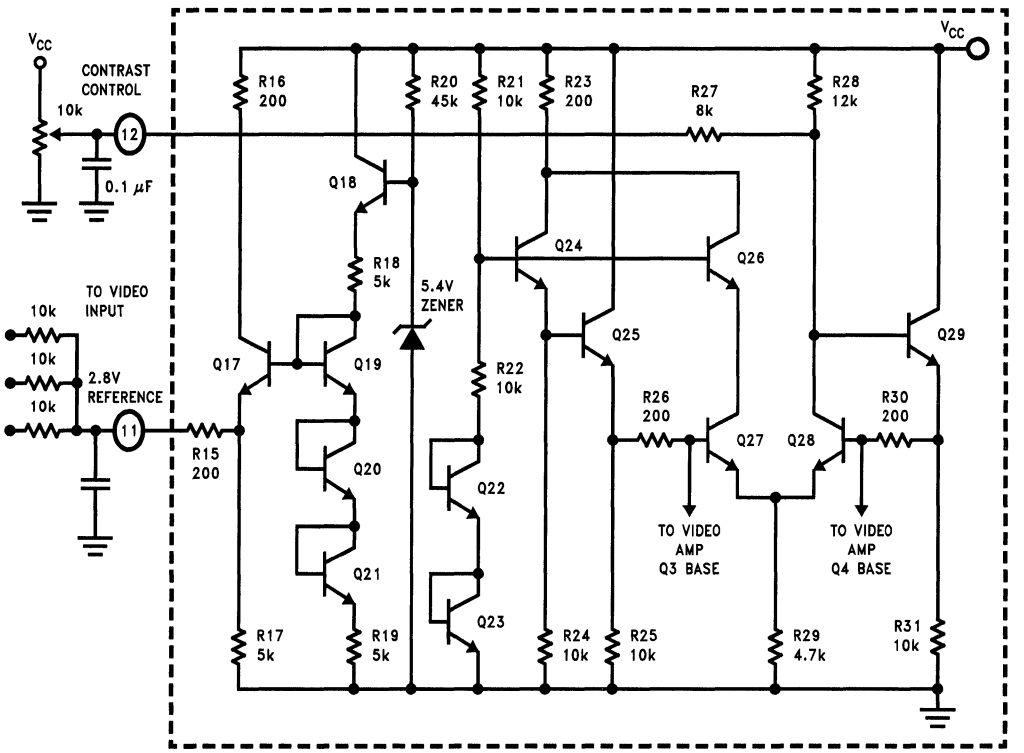


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FIGURE 7. Simplified Schematic of LM1203A Video Input Reference and Contrast Control Circuits

Circuit Description (Continued)

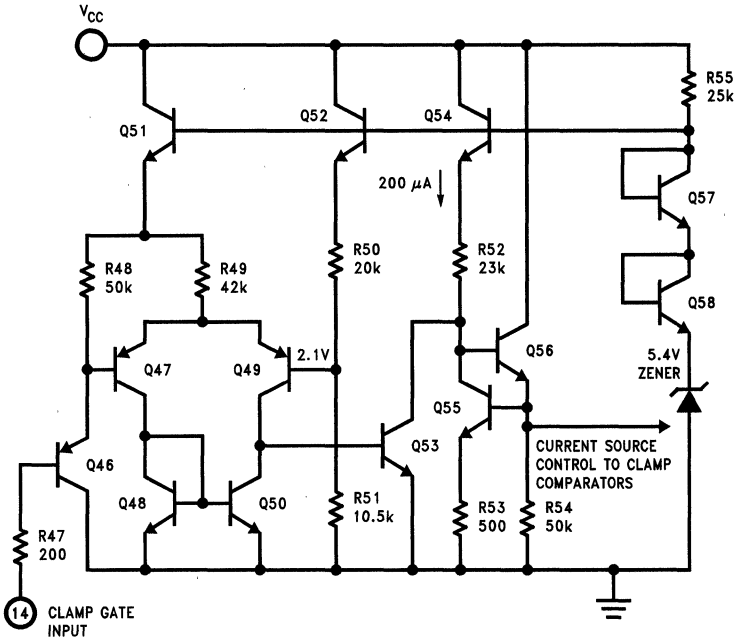

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FIGURE 8. Simplified Schematic of LM1203A Clamp Gate Circuit

Circuit Description (Continued)

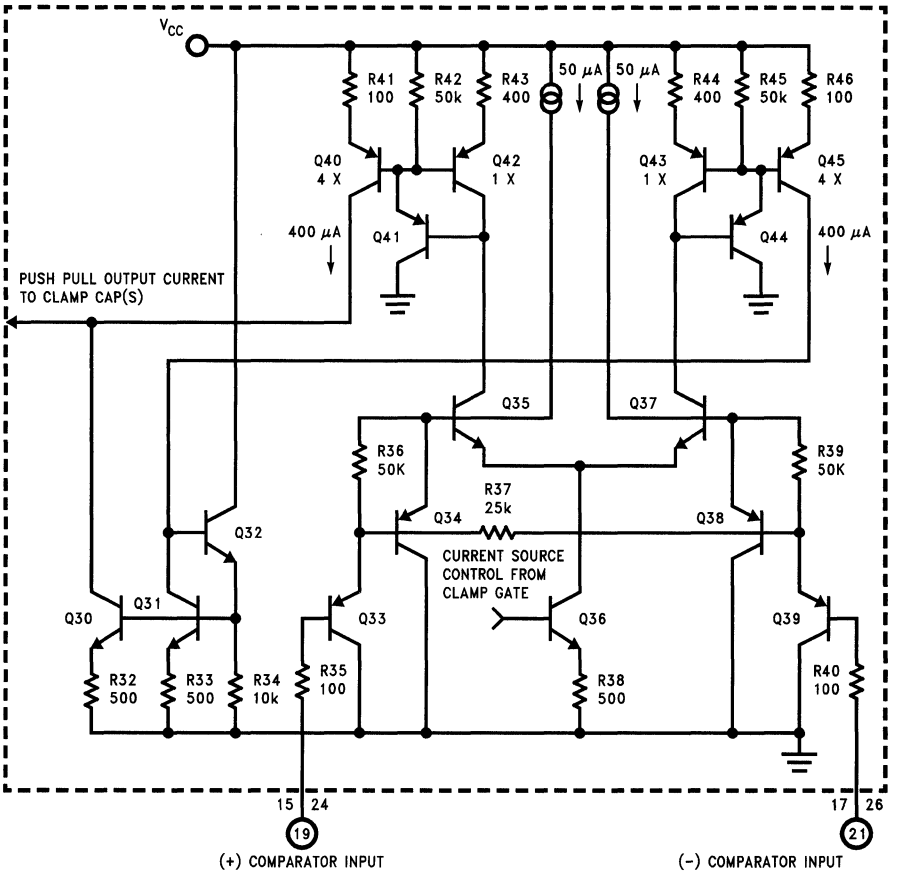

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FIGURE 9. Simplified Schematic of LM1203A Clamp Comparator Circuits

3

Additional Applications of the LM1203A

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0Ω and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

Figure 11 shows a complete RGB video preamplifier circuit using the LM1203A. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite sync input signal. The composite H Sync input signal may have either polarity. The back porch clamp signal applied to LM1203A's pin 14 allows clamping the video output signals to the black reference level, thereby providing DC restoration. The back porch clamp pulse width is determined by the time constant due to the product of R11 and C15. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R11 or C15 or both. Note that an MM74C86 Exclusive-OR gate may also be used, however, the pin out is different than that of the MM74HC86.

For optimum performance and maximum bandwidth, high speed buffer transistors (Q1, Q2 and Q3 in *Figure 11*) are recommended. The 2N5770 NPN transistors maintain high speed at high currents when driving the inputs of high voltage CRT drivers.

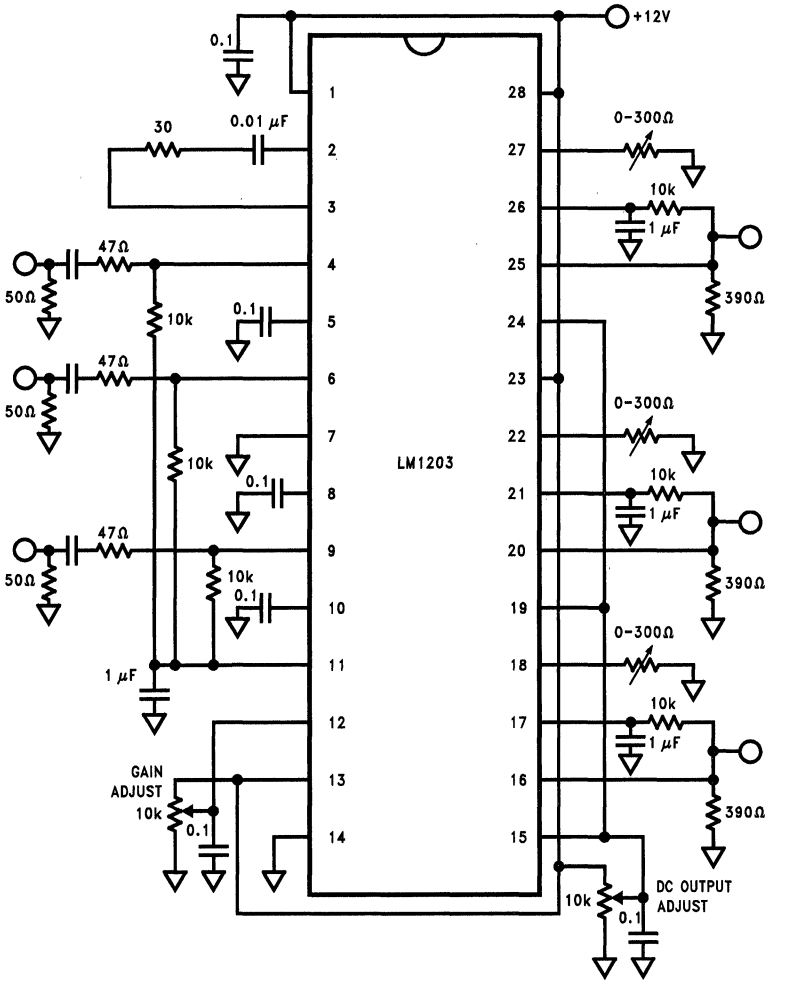

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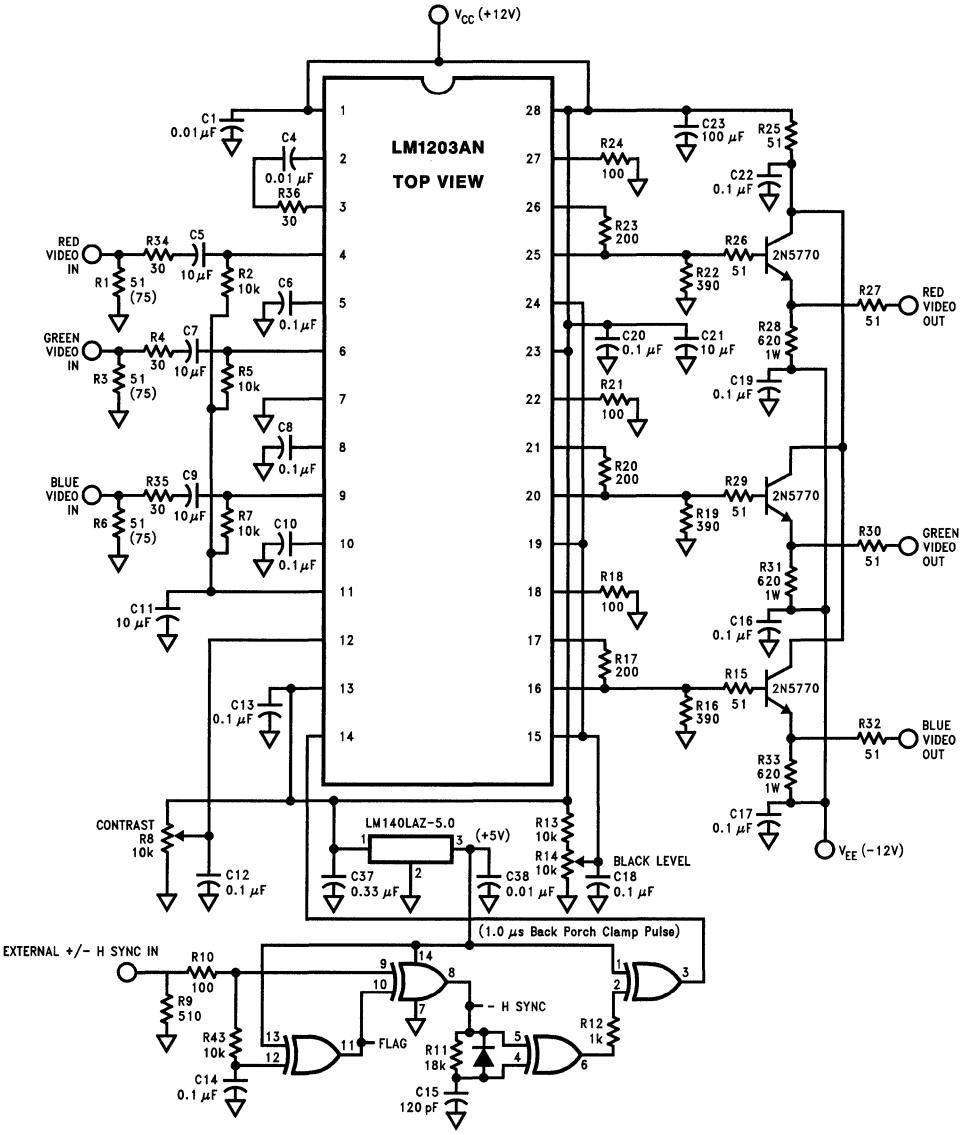
FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Application)

Additional Applications of the LM1203A (Continued)



TL/H/11441–18

FIGURE 11. LM1203A Applications Circuit

LM1203A vs LM1203

LM1203A is an improved version of the LM1203 RGB video amplifier system and is pin and function compatible with the LM1203. LM1203A's output voltage can swing as low as 0.15V as opposed to 0.9V for the LM1203. This eliminates the need for a level shift stage between the preamplifier and the CRT driver in most applications.

The LM1203A also offers faster rise and fall times of 4 ns vs 7 ns for the LM1203 and 100 MHz bandwidth vs 70 MHz for LM1203. With a peaking capacitor across the drive resistor, LM1203A's bandwidth can be extended to 150 MHz. Because of LM1203A's wide bandwidth, the device may oscillate if plugged directly into an existing LM1203 board. For optimum performance and stable operation, a double sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. *Figure 12* shows the layout of the PC board for *Figure 11's* circuit. For suggestions on optimum PC board layout, please see the reference section below.

The LM1203A also includes a built-in power down spot killer to prevent a flash on the screen upon power down. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter than white level at the output of the CRT driver, thus causing a flash on the screen.

REFERENCE

Ott, Henry W. *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1976.

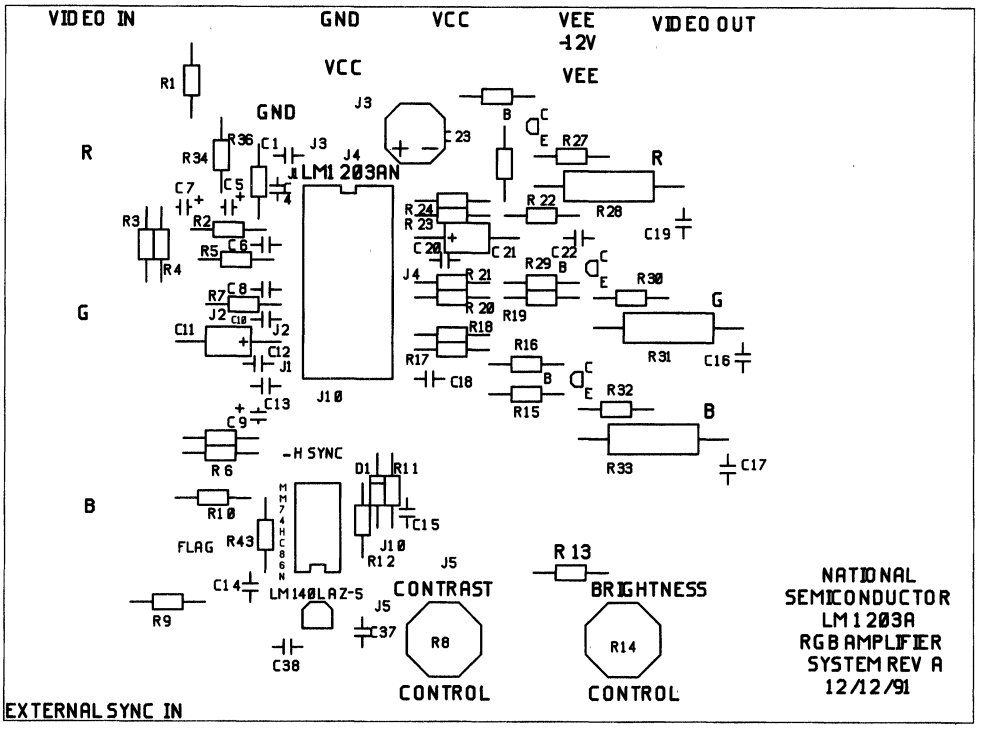


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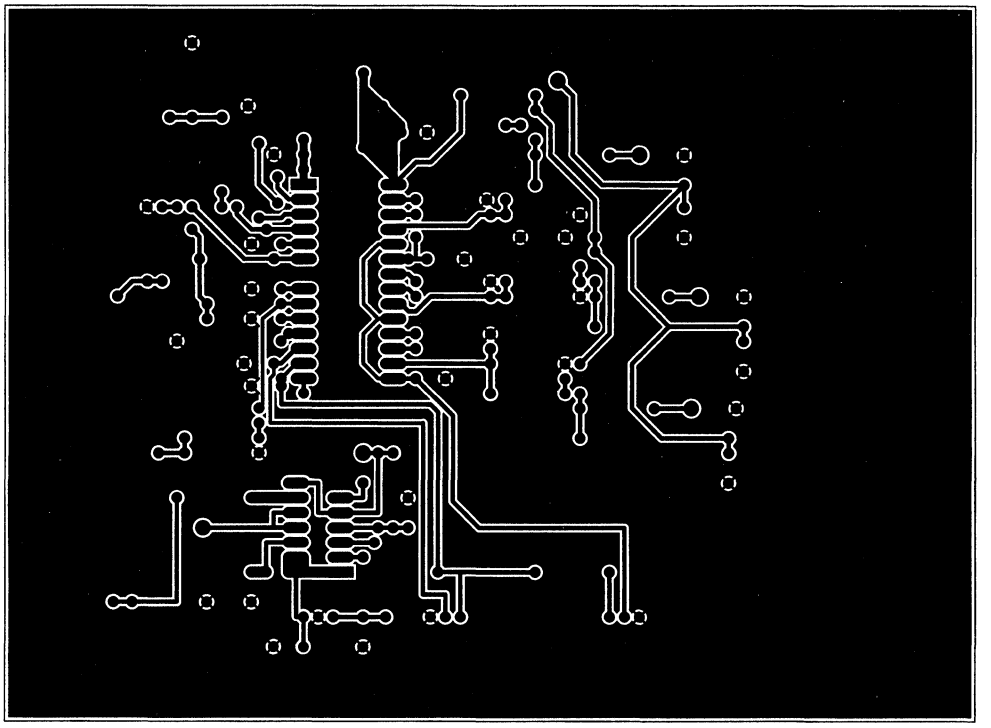
FIGURE 12(a). PC Board Silk Screen

Additional Applications of the LM1203A (Continued)



TL/H/11441–17

FIGURE 12(b). PC board layout of bottom side. Top side of PC board (not shown) is full ground plane.

National Semiconductor

PRELIMINARY

LM1203B
100 MHz RGB Video Amplifier System

General Description

The LM1203B is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203B contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203B also contains a voltage reference for the video inputs. The LM1203B is pin and function compatible with the LM1203.

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls

Features

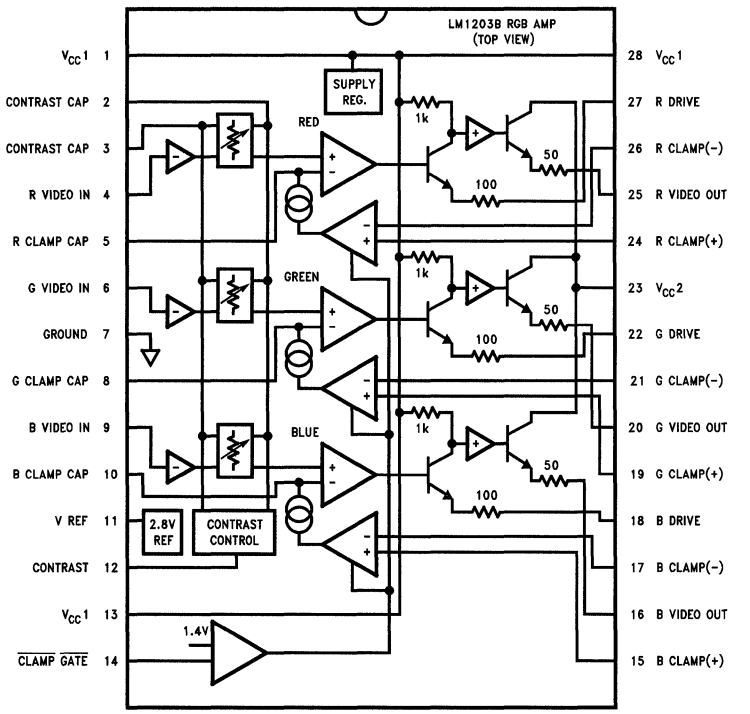
- Three wideband video amplifiers (100 MHz @ −3 dB)
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver
- Stable on a single sided board

Improvements over LM1203

- 100 MHz vs 70 MHz bandwidth
- V_{OUT} low: 0.15V vs 0.9V
- t_r, t_f: 3.7 ns vs 5 ns
- Built in power down spot killer

Block and Connection Diagrams

28-Lead Molded DIP



TL/H/11489–1

Order Number LM1203BN
See NS Package Number N28B

National Semiconductor

LM1204 150 MHz RGB Video Amplifier System

General Description

The LM1204 is a triple 150 MHz video amplifier system designed specifically for high resolution RGB video display applications. In addition to three matched video amplifiers, the LM1204 contains a DC operated contrast control, a DC operated drive control for each amplifier, and a dual clamping system for both brightness control and video blanking. The LM1204 also contains a back porch clamp pulse generator which is activated by an externally supplied ±H/HV sync signal or by an external composite video signal. The ±H/HV sync input will have priority over the composite video input. A single −H/HV sync output is provided for the automatically selected sync input signal. The back porch clamp pulse width is user adjustable from 0.3 μs to 4 μs.

The LM1204 video output stage will directly drive most Hybrid or discrete CRT amplfier input stages without the need for an external buffer transistor. The device has been designed to operate from a 12V supply with all DC controls operating over a 0V to 4V range providing for an easy interface to serial digital buss controlled monitors.

Features

- Built-in video blanking function
- Built-in sync separator for composite video input
- Includes DC restoration of video signals
- Back porch clamp pulse width user adjustable
- DC control of brightness, contrast, blanking level, drive and cutoff
- DC controls are 0V to 4V for easy interfacing to a digitally controlled system

Key Specifications

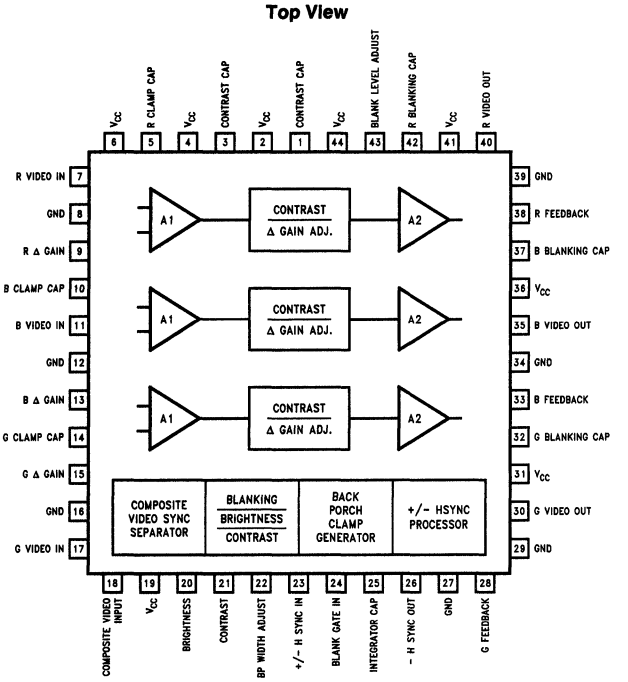
- 150 MHz large signal bandwidth (typ)
- 2.6 ns rise/fall times (typ)
- 0.1 dB contrast tracking (typ)
- ±3 dB drive (Δ gain) adjustments on R, G, B channels (typ)

Applications

- High resolution CRT monitors
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

Block Diagram and Connection Diagram

Top View



TL/H/11238–1

Ordering Information

Order Number LM1204V
See NS Package Number V44A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 2, 4, 6, 19, 31, 41, 44 (Note 3)	13.5V
Peak Video Output Source Current (Any One Amplifier) Pins 30, 35 or 39	30 mA
Voltage at Any Input Pin, V_{IN}	GND ≤ V_{IN} ≤ V_{CC}
Maximum ±H Sync Input Voltage	5.5 V_{PP}
Power Dissipation, PD (Above 25°C	
Derate Based on θ_{JA} and T_J)	2.4W
Thermal Resistance, θ_{JA}	52 °C/W
Junction Temperature, T_J	150°C
ESD Susceptibility (Note 4)	2.5 kV
Storage Temperature	−65°C to 150°C
Lead Temperature	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings (Note 2)

Temperature Range	0°C to 70°C
Supply Voltage, V_{CC}	10.8V ≤ V_{CC} ≤ 13.2V

DC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V unless otherwise specified; see test circuit, *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	No Video or Sync Input Signals, S1 = A	100	125	mA (Max)
I_B	Input Bias Current (Pin 9, 13, 15, 20, 21 or 22)	S1 = A	0.3	2	μA (Max)
I_{24h}	Blank Gate Input High Current	V24 = 4V	0.01	2	μA (Max)
I_{24l}	Blank Gate Input Low Current	V24 = 0V	2	5	μA (Max)
I_{FB}	Feedback Input Current (Pin 28, 33 or 38)		150		nA
I_{Blank+}	Blank Cap Charge Current	$V_{32,37,42}$ = 0V	185	75	μA (Min)
I_{Blank-}	Blank Cap Discharge Current	$V_{32,37,42}$ = 5V	−185	−75	μA (Min)
I_{BB}	Blank Cap Bias Current (Pins 32, 37, 42)		20		nA
I_{Clamp+}	Clamp Cap Charge Current	$V_{5,10,14}$ = 0V	185	75	μA (Min)
I_{Clamp-}	Blank Cap Discharge Current	$V_{5,10,14}$ = 5V	−185	−75	μA (Min)
I_{CB}	Clamp Cap Bias Current (Pins 5, 10, 14)		20		nA
V_{24h}	Blank Gate High Input Voltage	Input Signal is Not Blanked		2	V (Min)
V_{24l}	Blank Gate Low Input Voltage	Input Signal is Blanked		0.8	V (Max)
	Blank Comparator Offset Voltage	Voltage between V43 and Any One Video Output	2	50	mV (Max)
V_H	Video Output High Voltage (Pins 30, 35, 40)	R_L = 350Ω V28, 33, 38 = 0V	8.7	7	V(Min)
V_L	Video Output Low Voltage (Pins 30, 35, 40)	R_L = 350Ω V28, 33, 38 = 4V	0.1	0.5	V(Max)
V_{CM43}	Common Mode Range of Blank Comparator (Pins 43, 28, 33, 38)			0.5 4	V(Min) V(Max)

DC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V, unless otherwise specified; see Test Circuit *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$-H\ V_{OH}$	−H Sync Output Logic High (Pin 26)		4.2	2.4	V(Min)
$-H\ V_{OL}$	−H Sync Output Logic Low (Pin 26)		0.1	0.4	V(Max)
V_{23}	Quiescent DC Voltage at ±H Sync Input		3		V

AC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15, 21, 24, 43 = 4V, V20 = 2V, unless otherwise specified; see Test Circuit *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
R_{IN}	Video Amplifier Input Resistance		20		kΩ
A_{Vmax}	Maximum Video Amplifier Gain	f_{IN} = 12 kHz	10	5.5	V/V(Min)
ΔA_{Vtrack}	Amplifier Gain (Contrast) Tracking (Note 7)		0.1		dB
ΔA_{V2V}	Attenuation at 2V	Ref: $A_{V_{max}}$ V21 = 2V	6		dB
$\Delta A_{V0.5V}$	Attenuation at 0.5V	Ref: $A_{V_{max}}$ V21 = 0.5V	28	20	dB(Min)
ΔGain	Δ Gain Range (Pins 9, 13, 15)	V9, 13, 15 = 0V to 4V	±3		dB
ΔV_O	Max Brightness Tracking Error (Note 8)		100		mV
$f_{-3\ dB}$	Video Amplifier Bandwidth (Note 9)	V_{OUT} = 3.5 V_{PP}	150		MHz
THD	Video Amplifier Distortion	V_{OUT} = 1 V_{PP}, f = 12 kHz	0.3		%
t_R	Video Output Rise Time (Note 9)	Square Wave Input V_{OUT} = 3.5 V_{PP}, R_L = 350Ω	2.6		ns
t_F	Video Output Fall Time (Note 9)	Square Wave Input V_{OUT} = 3.5 V_{PP}, R_L = 350Ω	2.6		ns
$V_{ISO\ (1\ MHz)}$	Video Amplifier 1 MHz Isolation (Notes 9, 10)		−50		dB
$V_{ISO\ (130\ MHz)}$	Video Amplifier 130 MHz Isolation (Notes 9, 10)		−10		dB

AC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = A, S2 = B, S3, 4, 5 closed, V9, 13, 15, 20, 21, 43 = 2V, unless otherwise specified; see Test Circuit *Figure 1* and Timing Diagram for input waveform.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$V_{18(Min)}$	Composite Video Input Voltage (Pin 18)	S2 = A, Input = 10% Duty Cycle, Test for Loss of BP Pulse at Pin 26		0.15	V_{PP} (Min)
$V_{18(Max)}$	Composite Video Input Voltage (Pin 18)			2	V_{PP} (Max)
V_{23}	±H Sync Input Voltage (Pin 23)	Input = 10% Duty Cycle		1.6	V_{PP} (Min)
	Back Porch Clamp Pulse Width at V_{24} = 1V	S2 = A, Pin 26 = BP Output	1	1.4	µs (Max)
	Back Porch Clamp Pulse Width at V_{24} = 4V		300	600	ns (Max)
	Maximum ±H Sync Input Frequency		600		KHz
D_{HI}	Max Duty Cycle of Active High H Sync (Pin 23)	Test for Loss of Sync at Pin 26	22		%
D_{LO}	Max Duty Cycle of Active Low H Sync (Pin 23)		22		%
t_{pdl1}	±H Sync Input to −H Sync Output Low Delay	Input = 10% Duty Cycle	100		ns
t_{pdh1}	±H Sync Input to −H Sync Output High Delay	Input = 10% Duty Cycle	65		ns
t_{pd1}	±H Sync Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle, S2 = A	70		ns
t_{pdl2}	Composite Video Input to −H Sync Output Low Delay	Input = 10% Duty Cycle	106		ns
t_{pdh2}	Composite Video Input to −H Sync Output High Delay	Input = 10% Duty Cycle	68		ns
t_{pd2}	Composite Video Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle S2 = A	78		ns
$t_{pdl2}-t_{pdl1}$	Composite Video and ±H Sync Input to −H Sync Output Delta Delay	Input = 10% Duty Cycle	6		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 2, 4, 6, 19, 31, 36, 41 and 44 must be externally wired together to prevent internal damage during V_{CC} power on/off cycle.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: ΔA_V tracking is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage, V21, at either 4V or 2V measured relative to an A_V max condition V21 = 4V. For example, at A_V max, the three amplifier gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB and 6.5 dB respectively for V21 = 2V. This yields the measured typical ±0.1 dB channel tracking.

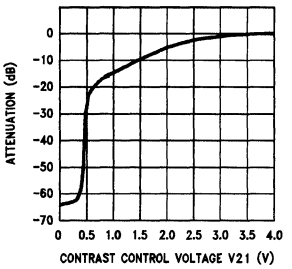
Note 8: Brightness tracking error is measured with all three video channels set for equal gain. The measured value is limited by the resolution of the measurement equipment.

Note 9: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. Video amplifier isolation tests also require this printed circuit board. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator.

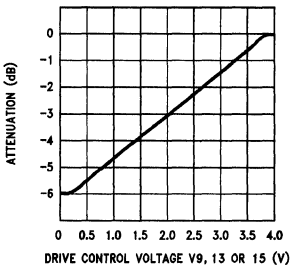
Note 10: Measure output levels of either undriven amplifier relative to the driven amplifier to determine channel isolation. Terminate the undriven amplifier inputs.

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

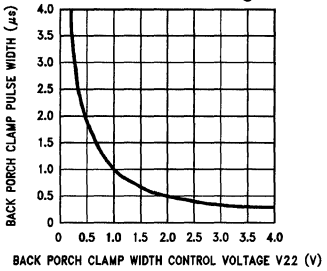
Attenuation vs Contrast Control Voltage (f = 12 kHz)



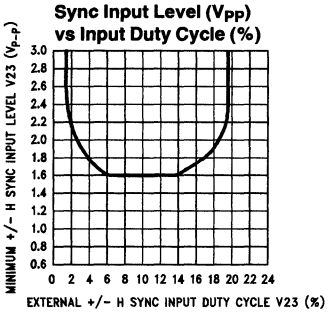
Attenuation vs Drive Control Voltage (f = 12 kHz)



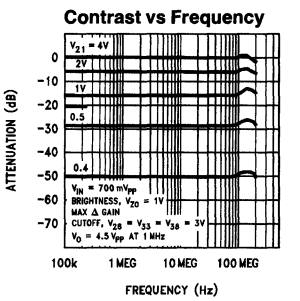
Back Porch Clamp Pulse Width vs Pin 22 Voltage



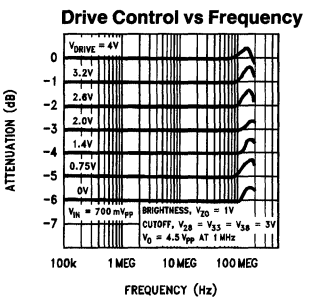
Minimum External ±H Sync Input Level (V_{PP}) vs Input Duty Cycle (%)



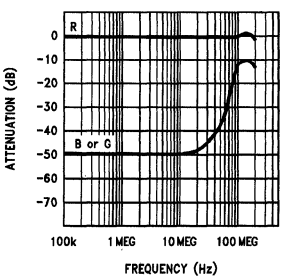
Contrast vs Frequency



Drive Control vs Frequency



Crosstalk vs Frequency



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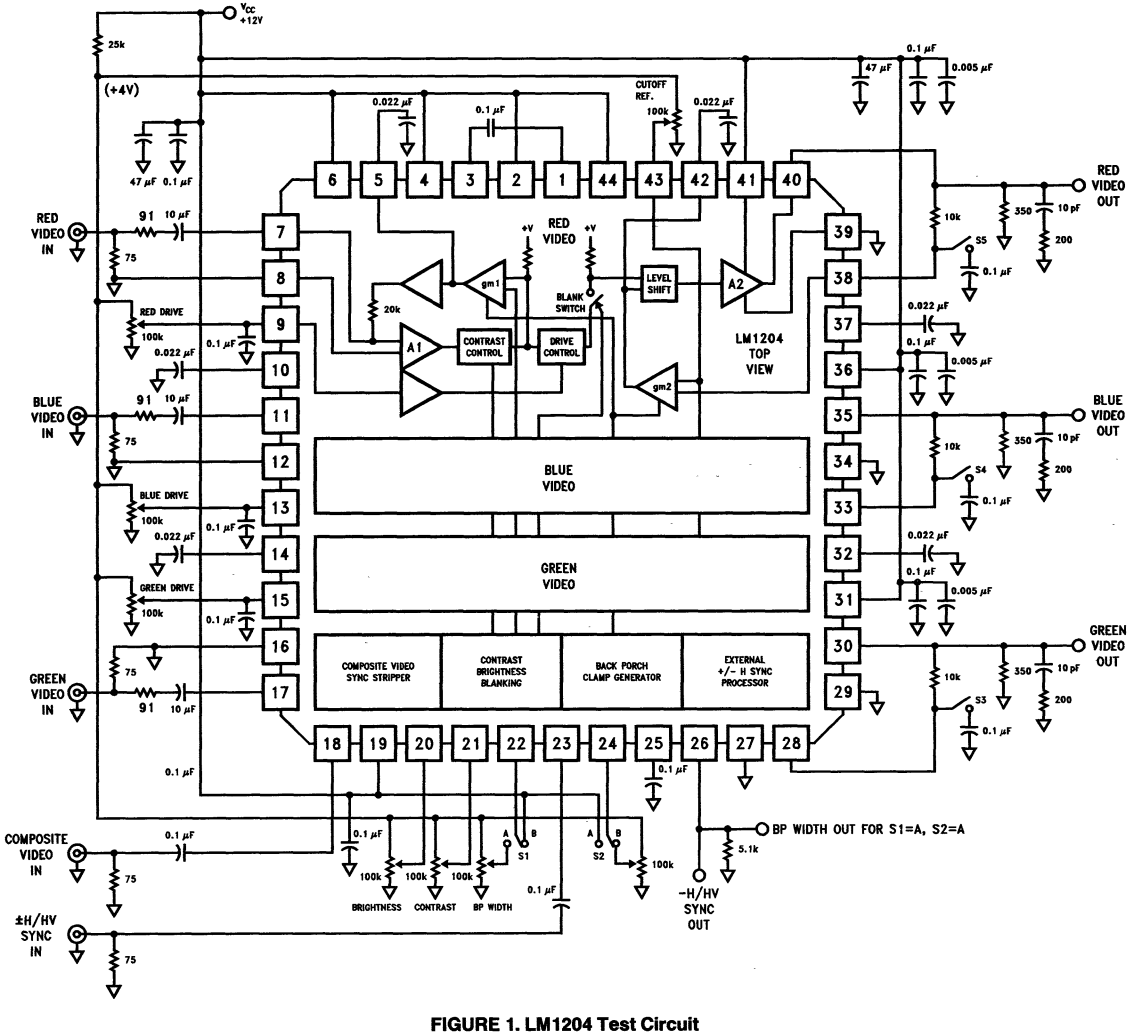

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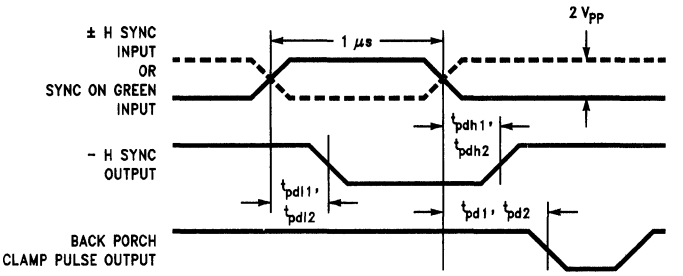
FIGURE 1. LM1204 Test Circuit

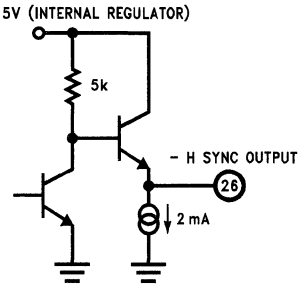
Timing Diagram



TL/H/11238–4

Input/Output Stages

–H Sync Output Stage



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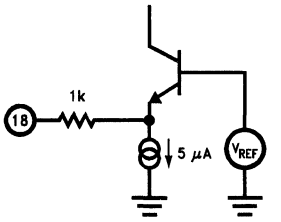
Composite Video Input



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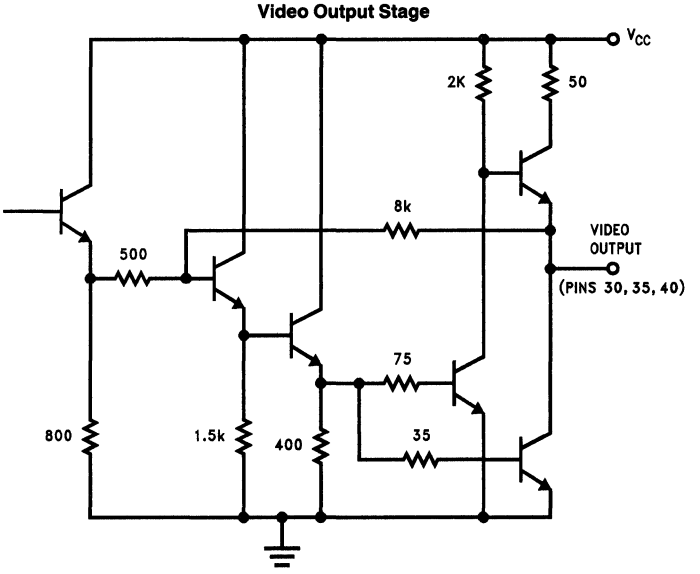
Video Output Stage



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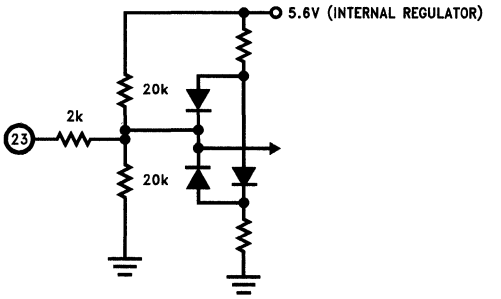
Input/Output Stages (Continued)

±H/HV Sync Input



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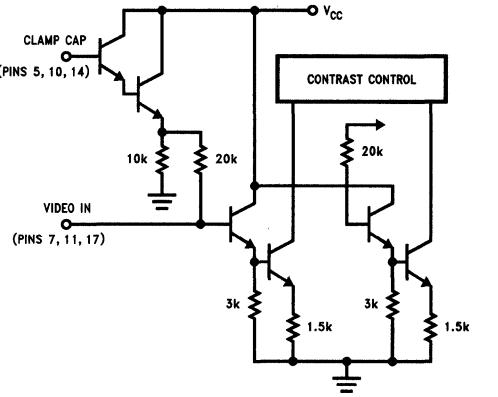
Video Input Stage



TL/H/11238–8

Pin Descriptions

V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41, 44)	All V_{CC} pins must be externally wired together. For stable operation, each supply pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.
Contrast Cap (Pins 1, 3)	An external decoupling capacitor of value 0.1 μF should be connected between pins 1 and 3 for contrast control.
R Clamp Cap (Pin 5)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the red channel video signal to the reference black level.
B Clamp Cap (Pin 10)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the blue channel video signal to the reference black level.
G Clamp Cap (Pin 14)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the green channel video signal to the reference black level.
R Video In (Pin 7)	This is the input for the red channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
B Video In (Pin 11)	This is the input for the blue channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
G Video In (Pin 17)	This is the input for the green channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
R Δ Gain (Pin 9)	This is the gain adjustment pin for the red video channel. A 0V to $4V_{DC}$ voltage is applied to this pin to vary the gain of the red channel. Usually, the red channel is set for maximum gain and the gains of the blue and green channels are reduced relative to the red channel until white balance is achieved on the CRT screen.
B Δ Gain (Pin 13)	This is the gain adjustment pin for the blue video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the blue channel.
G Δ Gain (Pin 15)	This is the gain adjustment pin for the green video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the green channel.
Compose Video Input (Pin 18)	This is the sync separator input pin. For Sync on Green systems, the green channel video signal should be AC coupled to pin 18 through a 0.1 μF capacitor.
Brightness Control (Pin 20)	If the LM1204 is used without blanking then this pin should be biased at 2.0 V_{DC}. Brightness control for all three video channels is now controlled by pin 43 (blank level adjust pin). See *Figure 4*. If the LM1204 is used with blanking then this pin allows the user to simultaneously DC offset the video portion of the output signals of all three channels thus allowing brightness control (See *Figure 5*).
Contrast Control (Pin 21)	This pin simultaneously controls the gain of all three video channels. A 0V to 4 V_{DC} input voltage is applied to this pin, with 0V corresponding to minimum gain (i.e., maximum attenuation of video signal) and 4V corresponding to maximum gain (i.e., minimum attenuation of the video signal).

Pin Descriptions (Continued)

Back Porch Clamp Width Adjust (Pin 22)
The LM1204 provides DC restoration or clamping during the back porch interval of the video signal. The width of LM1204's internally generated back porch clamp signal can be varied by applying a 0V to 4 V_{DC} voltage to this pin. The back porch clamp signal width can be varied from approximately 0.3 μs to 4.0 μs by applying 4V to 0.5V respectively. By connecting the blank gate input pin (pin 24) to V_{CC}, the back porch clamp pulse can be monitored on the −H Sync output pin (pin 26). See *Figures 4* and *5*. By connecting pin 22 to V_{CC}, the LM1204 functions as a non-gated amplifier requiring no clamping. See Section 4 under application hints for further information.

±H Sync In (Pin 23)
This is the external sync input pin, it accepts a negative or positive polarity signal, either horizontal sync or a composite sync (1.2 V_{PP} minimum amplitude). The LM1204 also provides a negative polarity (TTL compatible) horizontal sync or composite sync output on pin 26. If the composite video input (pin 18) is not used then an H Sync signal should be AC coupled to this pin through a 0.1 μF capacitor. The ±H Sync input has priority over the composite video input if both signals are present.

Blank Gate In (Pin 24)
This is the blank gate input pin. The LM1204 allows video blanking at the preamplifier. If blanking is desired then a TTL compatible, negative polarity blanking signal should be applied to this pin. During the blanking interval, all three video outputs are level shifted to the blank level set by the voltage at pin 43. If blanking is not required then, pin 24 should be biased at 4V.

Connecting pin 24 to V_{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch width as the potential at pin 22 is varied (see *Figures 4* and *5*).

Integrator Cap (Pin 25)
A 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows the LM1204 to integrate the ±H Sync input signal and genreate the proper polarity switch for −H Sync output.

−H Sync Out (Pin 26)
This output pin provides a negative polarity horizontal sync signal for other system uses. There is approximately 100 ns delay between the ±H Sync input signal at pin 23 and the −H Sync output signal at pin 26.

Connecting pin 24 to V_{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch clamp pulse width as the potential at pin 22 is varied (See *Figures 4* and *5*).

G Feedback (Pin 28)
This is the cutoff adjustment input for the green video channel. The green video output signal from pin 30 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.

B Feedback (Pin 33)
This is the cutoff adjustment input for the blue video channel. The blue video output signal from pin 35 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.

R Feedback (Pin 38)
This is the cutoff adjustment input for the red video channel. The red video output signal from pin 40 is fed back to this input through a potentiometer thus allowing the user to individualy adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.

G Video Output (Pin 30)
This is the green channel video output.

B Video Output (Pin 35)
This is the blue channel video output.

R Video Output (Pin 40)
This is the red channel video output.

G Blank Clamp Cap (Pin 32)
A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the green video channel.

B Blank Clamp Cap (Pin 37)
A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the blue video channel.

R Blank Clamp Cap (Pin 42)
A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows blanking for the red video channel.

Blank Level Adjust (Pin 43)
This pin serves two functions depending on whether the LM1204 is used with blanking or without blanking. If blanking is not selected then pin 20 should be biased at 2.0 V_{DC} and pin 43 assumes the role of brightness control. Varying the potential at pin 43 will simultaneously DC offset the video output signals of all three channels (See *Figure 4*). If the LM1204 is used with blanking then during the blanking interval, all three video output signals will be level shifted to the blank level. The desired blank level can be set by adjusting the potential at pin 43. Brightness control is now made possible by varying the potential at pin 20. Adjusting the brightness control DC offsets the video portion of the signal relative to the fixed blank level (all channels are affected simultaneously). See *Figure 5*.

GND (Pins 8, 12 16, 27, 29, 34, 39)
Ground. All ground pins must be connected to the ground plane.

Applications Hints

The LM1204 is a wideband video amplifier system designed specifically for high resolution RGB CRT monitors. The device includes circuitry for DC restoration of video signals and also allows contrast and brightness control. DC restoration is done during the back porch interval of the video signal. An internal sync separator generates a back porch clamp signal either from a "Sync on Green" signal applied to the composite video input (pin 18) or from an externally supplied ±H Sync signal . The LM1204 first looks at the ±H Sync input (pin 23), if an external horizontal sync signal is not present then the device syncs off the composite video input. The internally generated back porch clamp pulse width is user adjustable.

A blanking function is also included. This allows the user to cutoff the beam current in the CRT's guns during the blanking interval thereby preventing horizontal retrace lines from being visible. Normally blanking is done by applying a high voltage pulse at the grid. However, blanking at the cathode using the LM1204 leads to ease of design and lowered cost.

Figure 2 shows the block diagram of the green video channel and the control logic. The two modes of operation, with and without blanking, are described below in detail.

1.0 Operation without Blanking

For operation without blanking, the blank gate input (pin 24) should be connected to +4V. This causes the blank comparator to connect switch S2 to position Y (See *Figure 2*).

Furthermore, the brightness control input pin (pin 20) should be biased at a potential between 1V (Min) and 3.8V (Max), it is best to bias this pin at 2V. The video signal is AC coupled to the input of the LM1204 as shown for the green channel in *Figure 2*. During the back porch interval of the video signal (See *Figure 3*), the internally generated back porch clamping pulse goes low, causing switches S1A and S1B to be closed. The closure of S1A causes g_m1 to charge capacitor C2 to a potential determined by the DC voltage at pin 20. This allows g_m1 to set up an average DC bias for the AC coupled video signal at the input of A1. When the back porch clamping pulse is high, S1A and S1B are opened. With S1A open, g_m1 is effectively disconnected from C2, C2 now holds the DC bias voltage. The transconductance stage g_m1 therefore functions as a sample and hold device and holds the input of A1 at the desired DC bias.

The LM1204 uses black level clamping at the back porch of the video signal to accomplish DC restoration. The transconductance stage g_m2 is enabled during the back porch clamp period to provide a sample and hold function. During the back porch clamp period, DC feedback from LM1204's video output is compared with the voltage set by potentiometer R9. Depending on A2's output voltage, C6 is either charged or discharged so that the feedback loop consisting of g_m2 and A2 is stabilized and the output is clamped to the black level. All this occurs during the back porch clamp period. During the video portion of the signal, g_m2 is disabled and C6 holds the fixed black level reference voltage. The beginning of each new line on the raster always starts from a fixed reference black level thus restoring the DC component of each line.

A2 is a summing amplifier that adds a DC offset component from g_m2 to the video signal from the multiplier. Adjusting R9 will DC offset the output signals of all three channels thus providing brightness control. Individual cutoff adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (Pins 38, 28 and 33). For example, cutoff adjustment for the green channel is done by potentiometer R8 shown in *Figure 2*.

Adjusting the contrast control (potentiometer R3 in *Figure 2*) varies the peak to peak amplitude (includes sync tip if present) of all three video output signals relative to their black reference level. The Δ Gain adjust (pins 9, 15 and 13 for R, G, and B channels respectively) allows the user to individually adjust the AC gain of each channel. For example the AC gain of the green channel is adjusted using potentiometer R5 as shown in *Figure 2*. Normally the red channel is set for maximum gain and the gains of the blue and green channels are reduced until white balance is achieved on the CRT monitor's screen. *Figure 4* shows the adjustments for operation without blanking.

2.0 Operation with Blanking

Much of what was discussed in Section 1.0 also applies when the LM1204 is used with the blanking function. However, there are notable differences as described herein. For operation with blanking, a TTL compatible blanking signal must be applied to the blank gate input (pin 24).

During the blanking period, the blanking comparator connects switch S2 to position X (See *Figure 2*). This causes the LM1204 to level shift the video output signal to the blank level. Adjusting R9 will adjust the blank level of all three channels. Individual blank level adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (pin 38, 28 and 33). In *Figure 2* this is done by adjusting potentiometer R8 for the green channel.

During the video portion of the video signal, S2 is connected to position Y. Brightness control is now accomplished by varying the potential at the brightness control pin (pin 20). Adjusting R6 offsets the video portion of all three output signals relative to the fixed blank level, restoring the DC level of the video signal. *Figure 5* shows the adjustments for operation with blanking.

3.0 Stability Considerations

For optimum performance and stable operation, a double sided PC board with adequate ground plane is essential. Moreover, soldering the LM1204 on to the PC board will yield best results. Each supply pin (pins 2, 4, 6, 19, 31, 36, 41 and 44) should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the supply pin as is possible.

When driving the LM1204 from a 75Ω video source, the cable is terminated with 75Ω to minimize reflections caused by transmission line effects. However, the input impedance of LM1204 is capacitive and is also affected by the stray capacitance of the PC board. Thus the input impedance is a function of frequency. This changes the impedance of the cable termination. This can introduce overshoot and ringing in LM1204's pulse response. A 100Ω resistor in series with the blocking capacitor at the video input will minimize overshoot and ringing (see *Figure 8*). The value of the resistor is empirically determined. 100Ω is a good starting value.

Since the LM1204 is a wide bandwidth amplifier with high gain at high frequencies, the device may oscillate when driving a large capacitive/inductive load. To prevent oscillation, the amplifier's gain is rolled off at high frequencies. This is accomplished by an RC network comprised of a resistor in

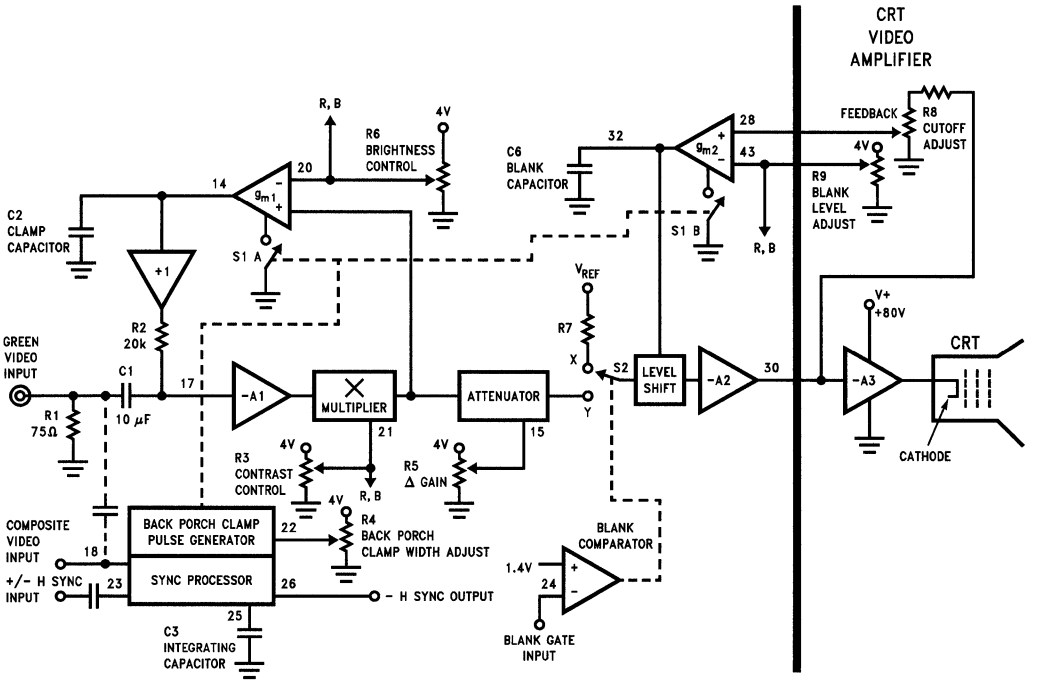
3.0 Stability Considerations (Continued)

series with a capacitor connected from the video output pin to ground (see Test Circuit, *Figure 1*). A 110Ω to 200Ω resistor in series with 10 pF is quite adequate for most applications. However, if oscillations don't cease then the value of the resistor should be decreased or the value of the capacitor should be increased or a combination of the two.

Non-Gated High Frequency Application

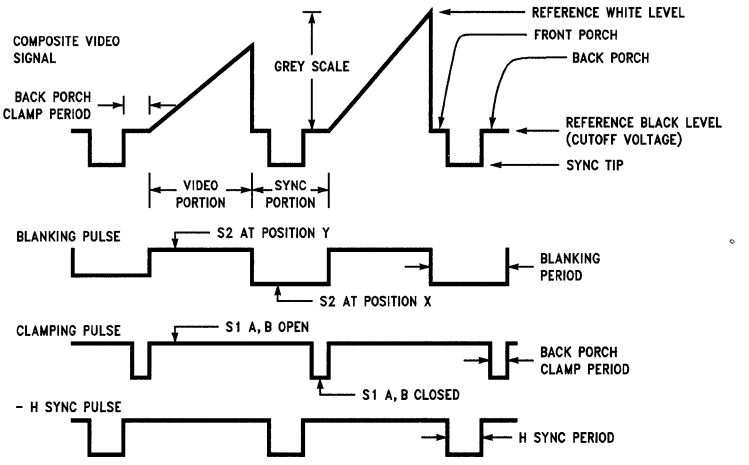
By connecting the back porch width adjust pin (pin 22) to V_{CC}, the LM1204 functions as a non-gated amplifier requiring no sync or blanking signals. *Figure 9* shows a triple high frequency amplifier with variable gain and DC offset control. In this mode of operation, filtered DC feedback must be provided to pins 28, 33 and 38 as shown in *Figure 9*.

LM1204



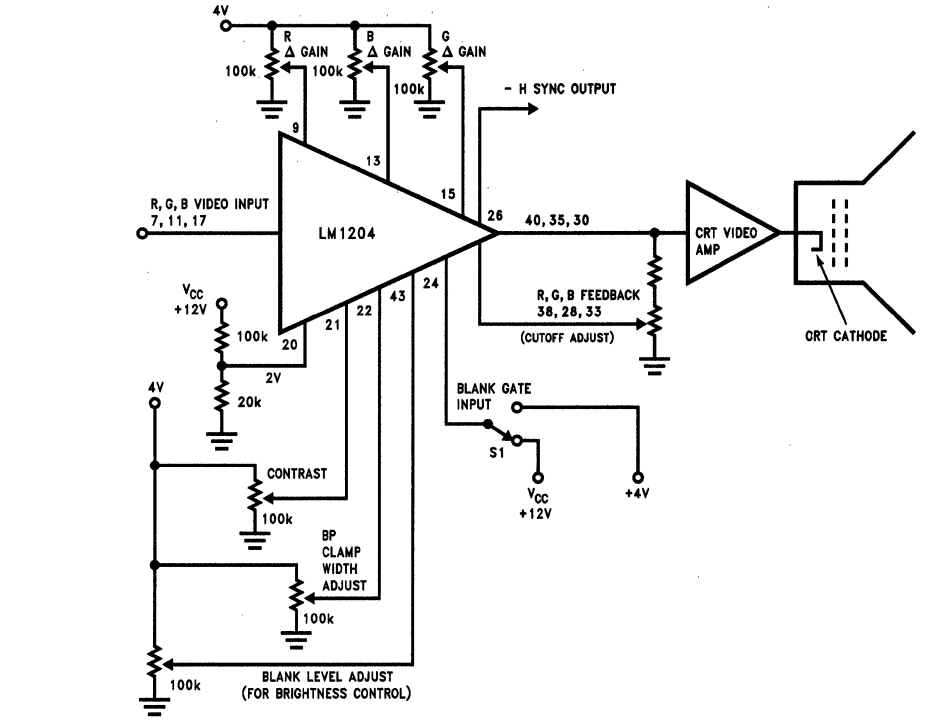
TL/H/11238–9

FIGURE 2. Block Diagram Showing Timing Circuitry and Green Video Channel

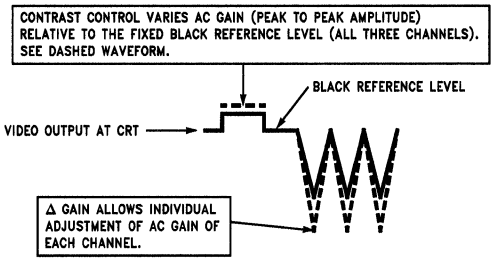


TL/H/11238–10

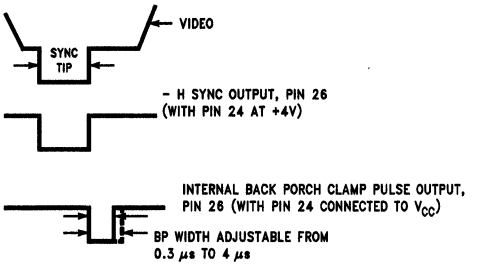
FIGURE 3. Composite Video and Timing Signals



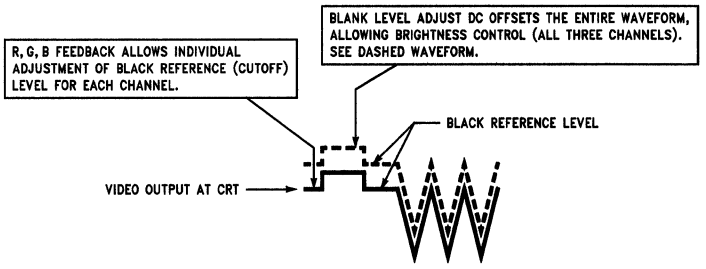
TL/H/11238–11



TL/H/11238–12

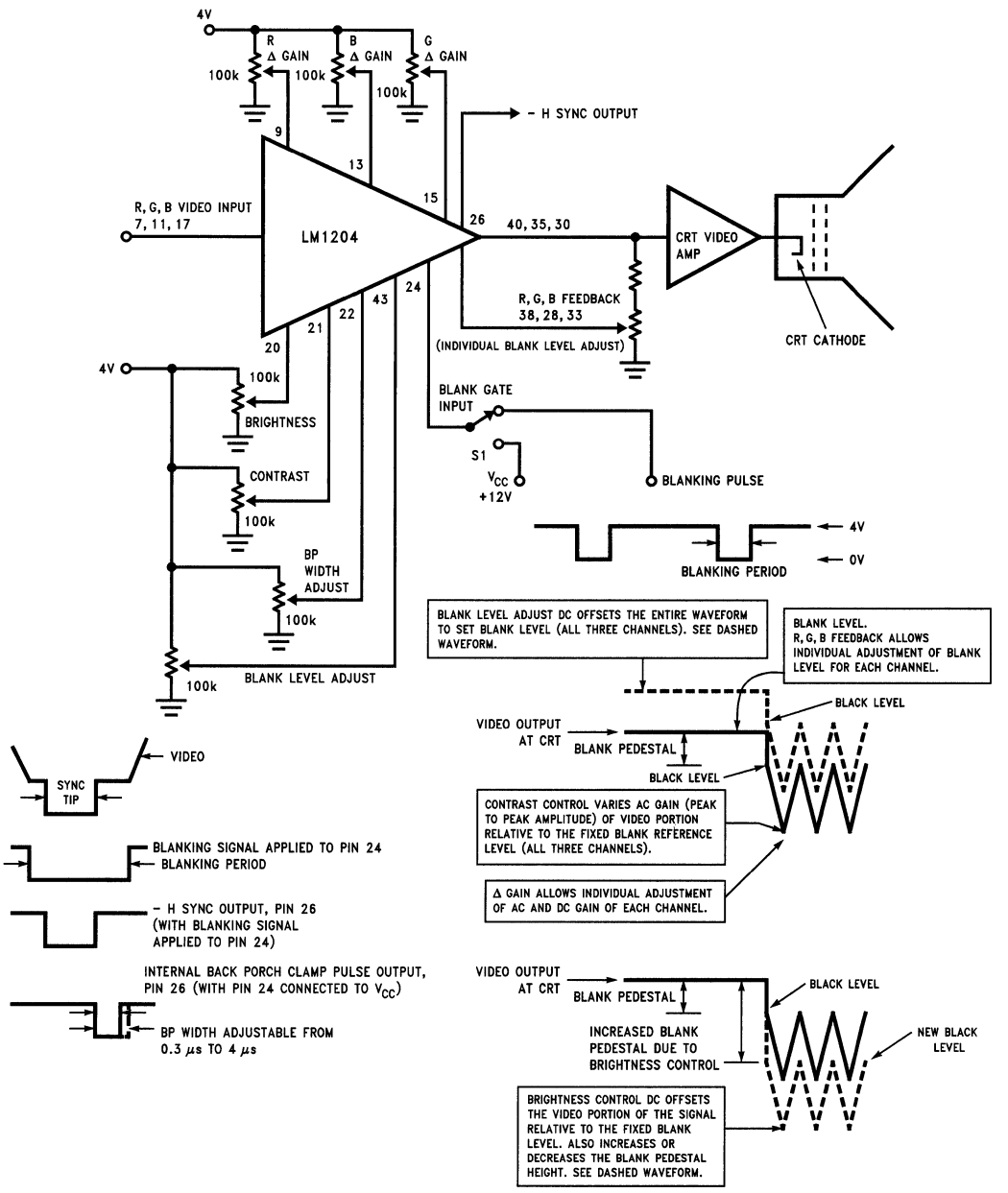


TL/H/11238–13



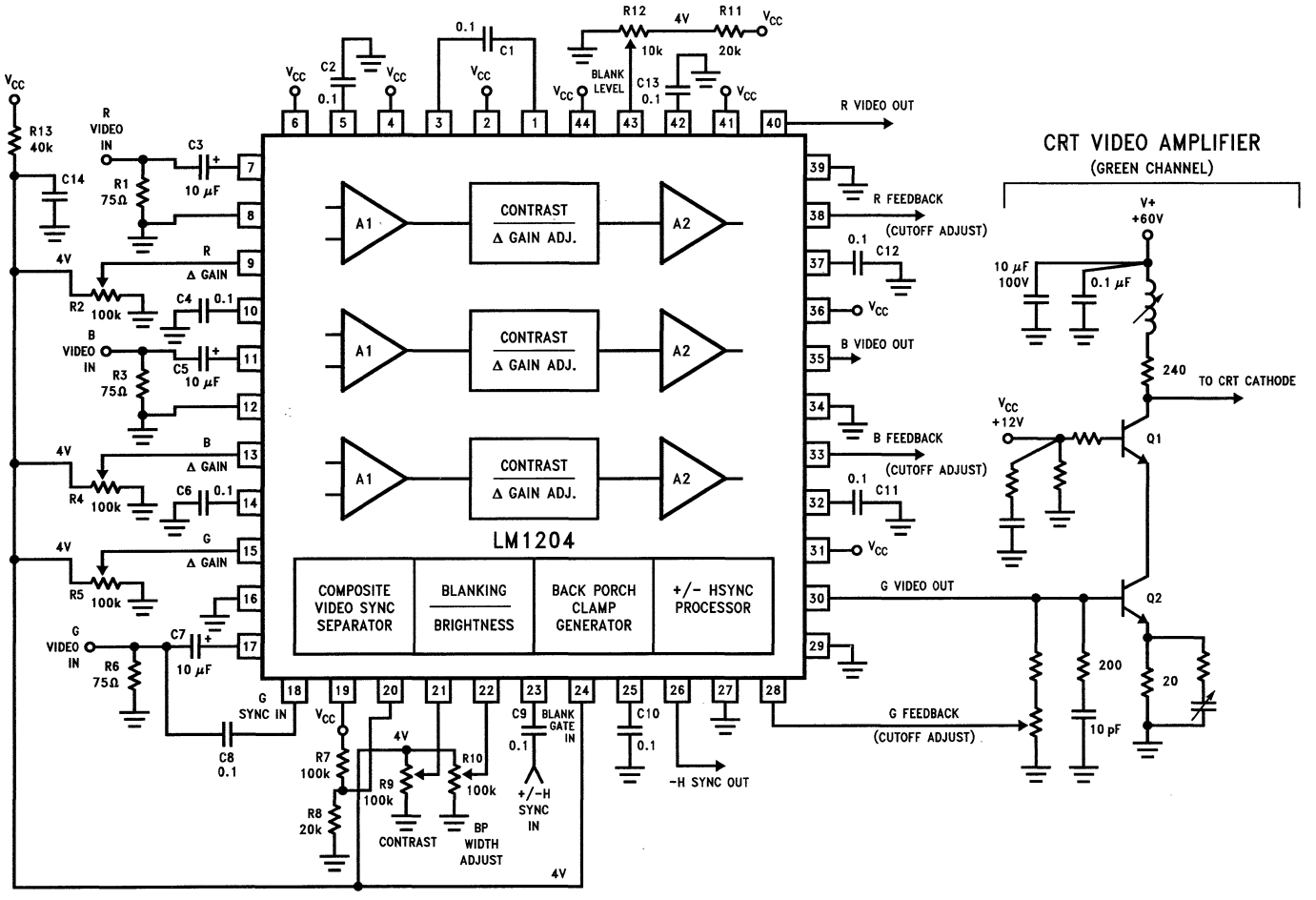
TL/H/11238–14

FIGURE 4. LM1204 Adjustments without Blanking



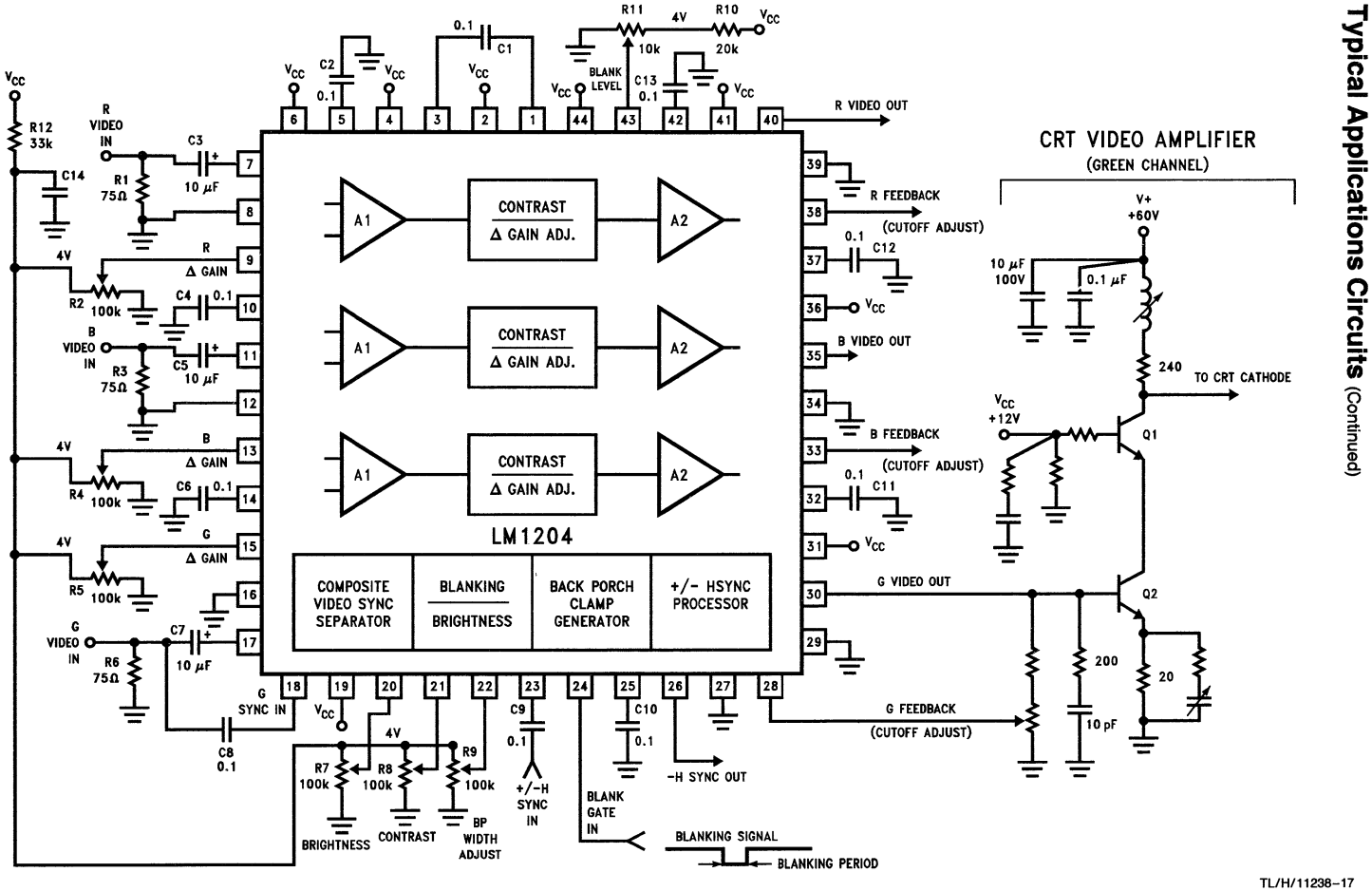
TL/H/11238–15

FIGURE 5. LM1204 Adjustments with Blanking



TL/H/11238–16

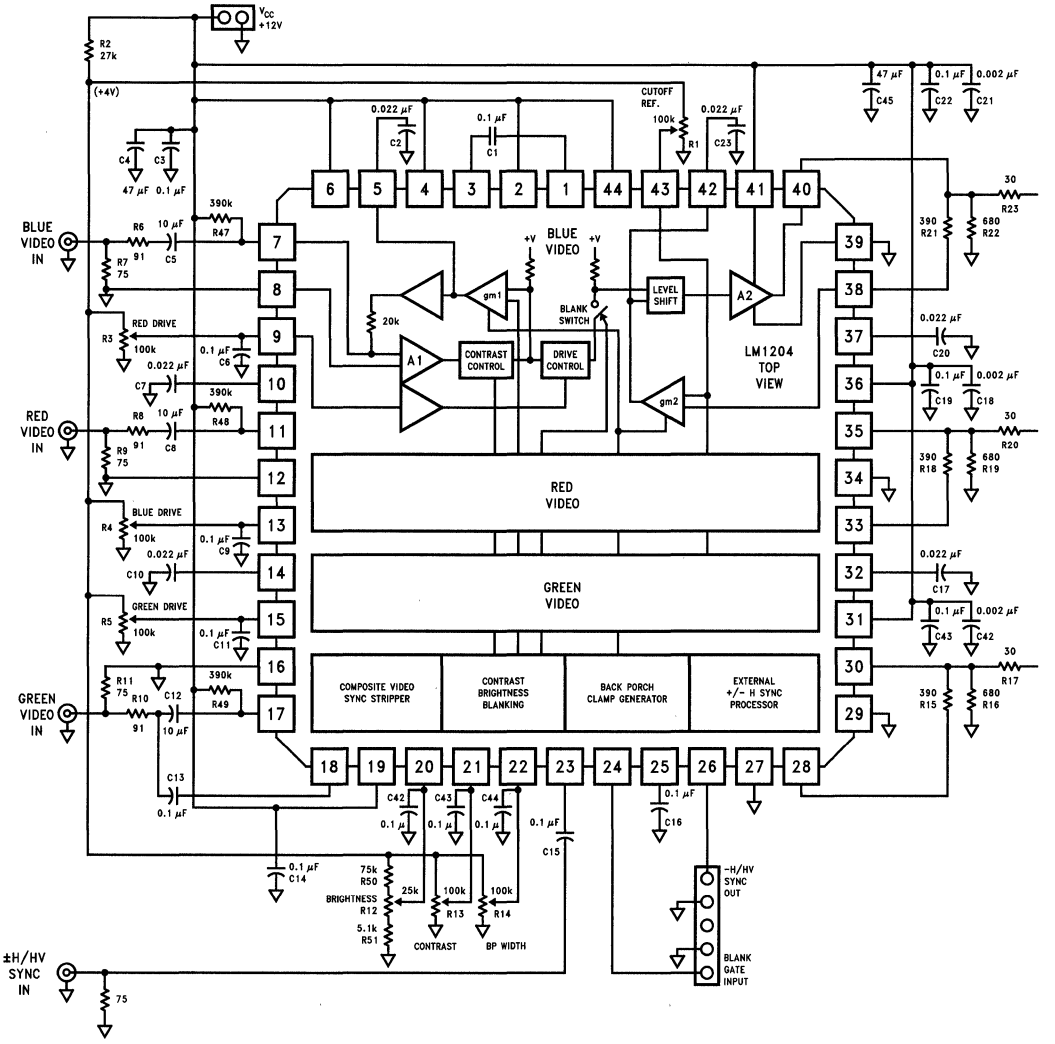
FIGURE 6. The LM1204 driving cascode CRT video amplifiers and operating without blanking. Brightness control is accomplished by potentiometer R12 (See *Figure 4* for explanation of adjustments). Each V_{CC} pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.



TL/H/11238–17

FIGURE 7. The LM1204 driving cascode CRT video amplifiers and operating with blanking. The video signal is level shifted to the user adjustable blank level during the blanking period. Brightness control DC offsets the video signal relative to the fixed blank level and is accomplished by potentiometer R7. See *Figure 5* for explanation of adjustments. Each V_{CC} pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.

Typical Applications Circuits (Continued)



TL/H/11238–18

FIGURE 8. Complete circuitry for an RGB CRT video board using the LM1204 and LH2426AS. The video output signals from LH2426AS are AC coupled and diode clamped to greater than 80V.

Typical Applications Circuits (Continued)

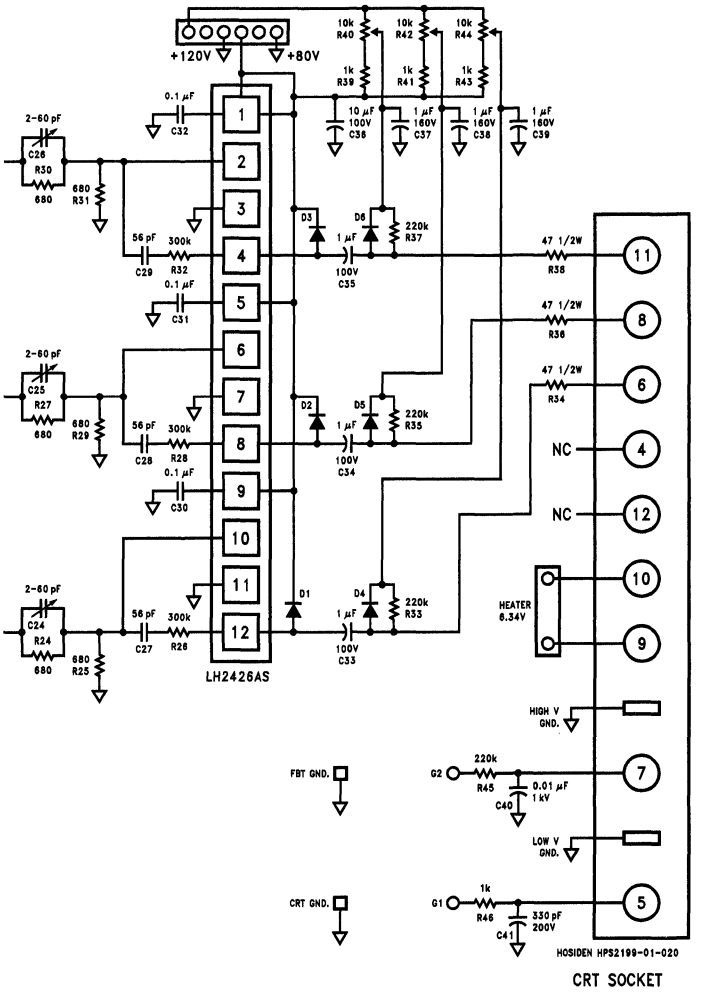


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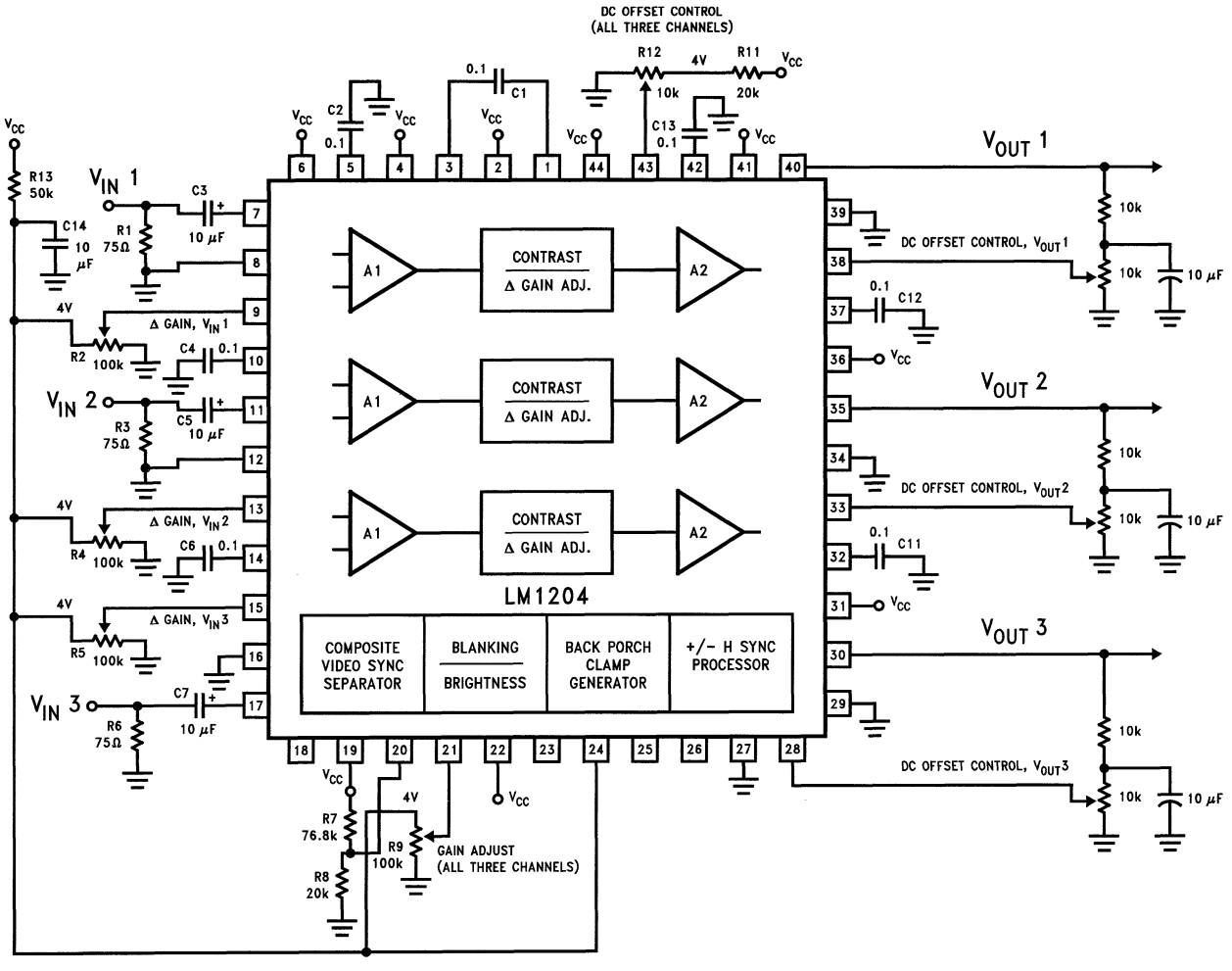
FIGURE 8. (Continued)



TL/H/11238–19

FIGURE 9. Three channel high frequency amplifier with gain and DC offset control (non-video application). Each V_{CC} pin should be bypassed with a 0.01 µF and a 0.1 µF capacitor connected as close to the pin as is possible.

National Semiconductor

LM1391 Phase-Locked Loop

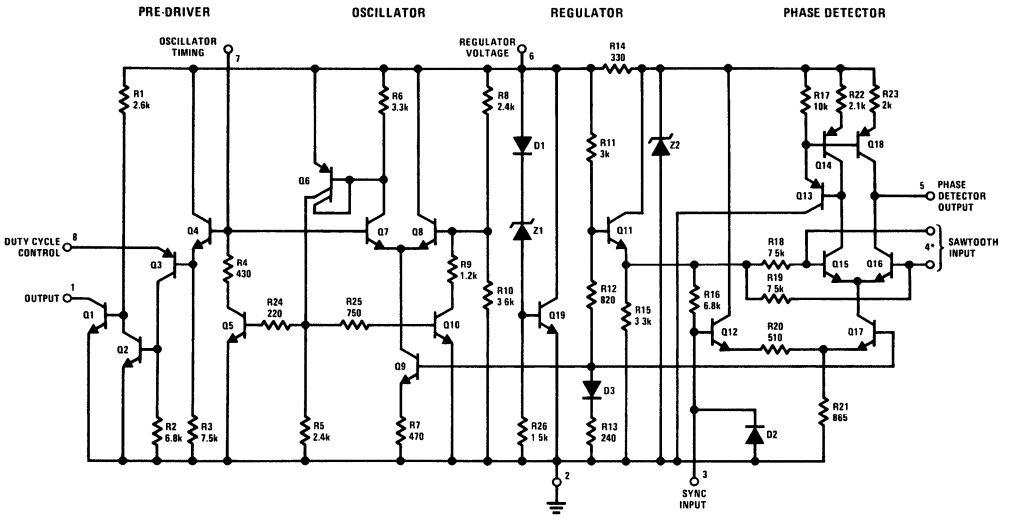
General Description

The LM1391 integrated circuit has been designed primarily for use in the horizontal section of TV receivers, but may find use in other low frequency signal processing applications. It includes a stable VCO, linear pulse phase detector, and variable duty cycle output driver.

Features

- Internal active regulator for improved supply rejection
- Uncommitted collector of output transistor
- Output transistor with low saturation and high voltage swing
- APC of the oscillator with a synchronizing signal
- DC controlled output duty cycle
- ±300 Hz typical pull-in
- Linear balanced phase detector
- Low thermal frequency drift
- Small static phase error
- Adjustable DC loop gain

Schematic Diagram



TL/H/7889–1

(*) Pin 4 Base of Q16 (LM1391) for use with (+) flyback pulse

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current	40 mA_{DC}
Output Voltage	40 V_{DC}
Output Current	30 mA_{DC}
Sync Input Voltage (Pin 3)	5.0 Vp-p
Flyback Input Voltage (Pin 4)	5.0 Vp-p
Power Dissipation (Package Limitation) Plastic Package (Note 1)	1000 mW
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

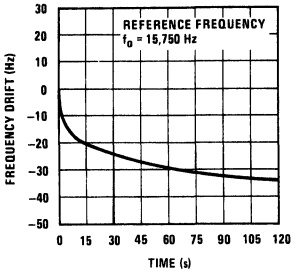
Electrical Characteristics T_A = 25°C (see test circuit, all switches in position 1)

Parameter	Conditions	Min	Typ	Max	Units
Regulated Voltage (Pin 6)	I_6 = 22 mA_{DC}	8.0	8.6	9.2	V_{DC}
Supply Current (Pin 6)			20		mA_{DC}
Collector-Emitter Saturation Voltage of Output Transistor (Pin 1)	I_{C1} = 20 mA		0.30	0.40	V_{DC}
Pin 4 Voltage			2.0		V_{DC}
Oscillator Pull-in Range	Adjust R_H		±300		Hz
Oscillator Hold-in Range	Adjust R_H		±900		Hz
Static Phase Error	Δf = 300 Hz		0.5		μs
Free-running Frequency Supply Dependance	S1 in position 2		±3.0		Hz/V_{DC}
Phase Detector Leakage (Pin 5)	All switches in position 2			±1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	Vp-p
Sawtooth Input Voltage (Pin 4)		1.0		3.0	Vp-p
Maximum Oscillator Frequency			500		kHz

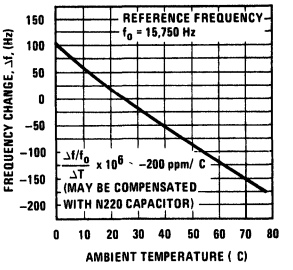
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 120°C/W junction to ambient.

Typical Performance Characteristics

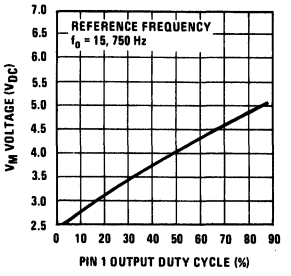
Frequency Drift vs Warm-Up Time



Frequency vs Temperature



Output Duty Cycle vs V_M Voltage



TL/H/7889–3

Application Information

The following equations may be considered when using the LM1391 in a particular application.

$$R201 = R301 = \frac{V_{CC} - 8.6}{0.02}\ \Omega$$

$$f_O \cong \frac{1}{0.6\ R_O C_O}\ \text{Hz}\quad 1.5k \le R_O < 51k$$

$$R204 \cong 10\ R_O$$

$$C203 = C204 \cong \frac{1}{600\ f_O(\text{Hz})}\ \text{F}$$

DC Loop Gain $\mu\beta \cong 3.2 \times 10^{-5}\ R_O f_O$ Hz/rad

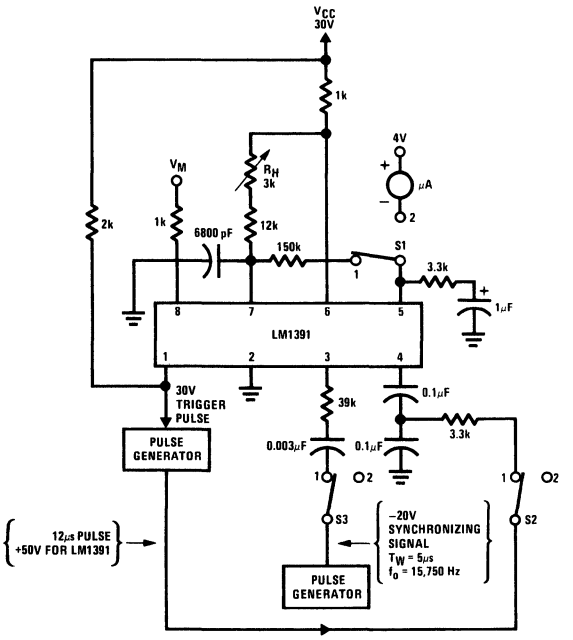
Noise Bandwidth

$$f_{nn} \cong \frac{1 + 2\pi \frac{R_X^2}{R_Y} C_C\ \mu\beta}{4 R_X C_C}\ \text{Hz}$$

Damping Factor

$$K \cong \frac{\pi}{2} \frac{R_X^2}{R_Y} C_C\ \mu\beta$$

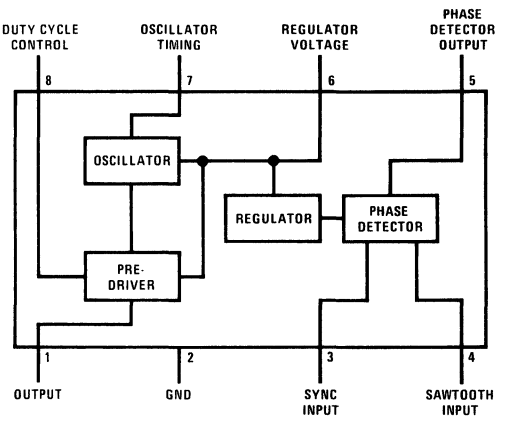
Test Circuit



TL/H/7889-4

Connection Diagram

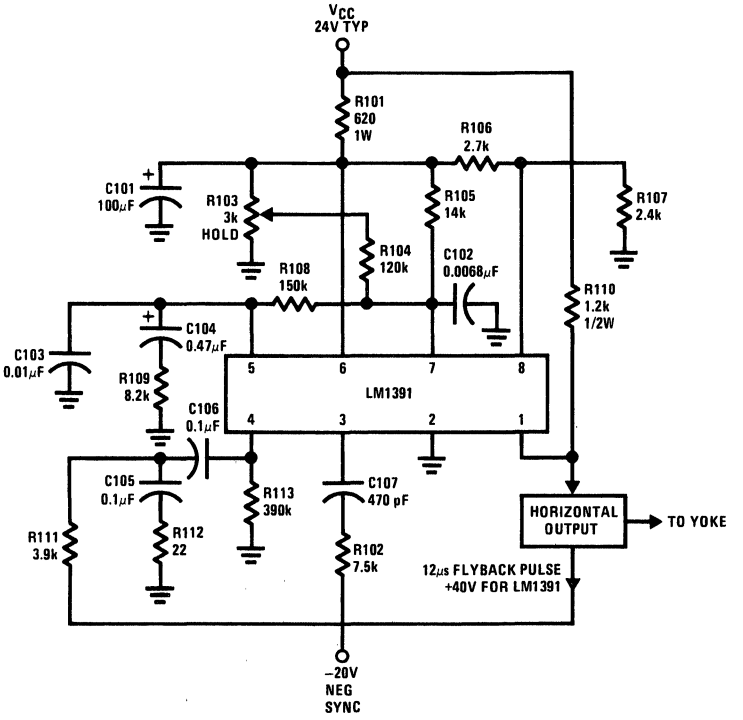
Dual-In-Line Package



TL/H/7889-2

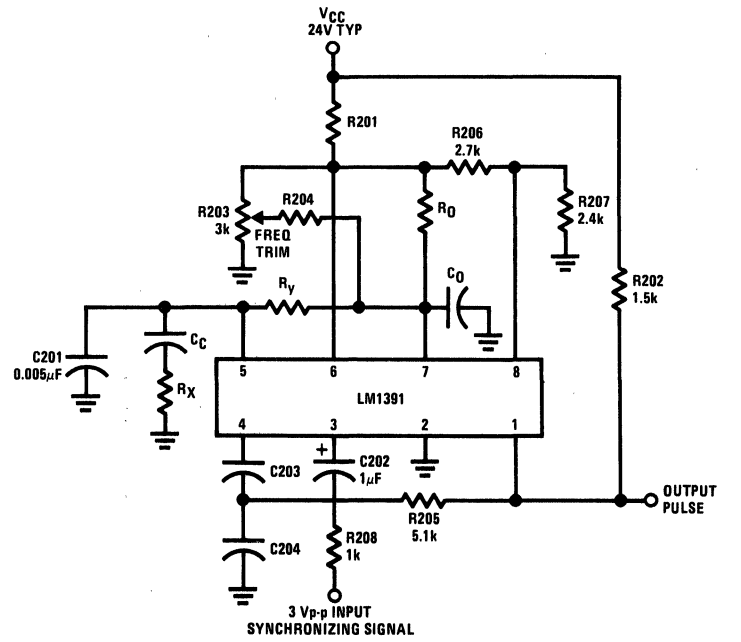
Top View
Order Number LM1391N
See NS Package Number N08E

Typical Applications



TL/H/7889–5

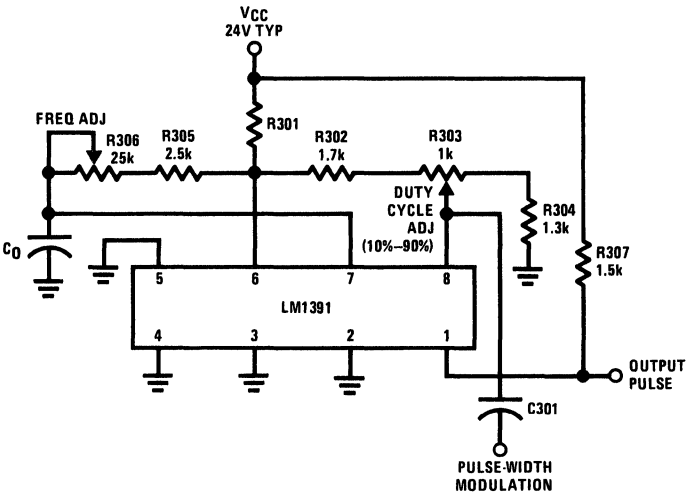
FIGURE 1. TV Horizontal Processor



TL/H/7889–6

FIGURE 2. General Purpose Phase-Lock Loop
(See Applications Information)

Typical Applications (Continued)



TL/H/7889–7

FIGURE 3. Variable Duty Cycle Oscillator (See Applications Information)

National Semiconductor

LM1823 Video IF Amplifier/PLL Detector System

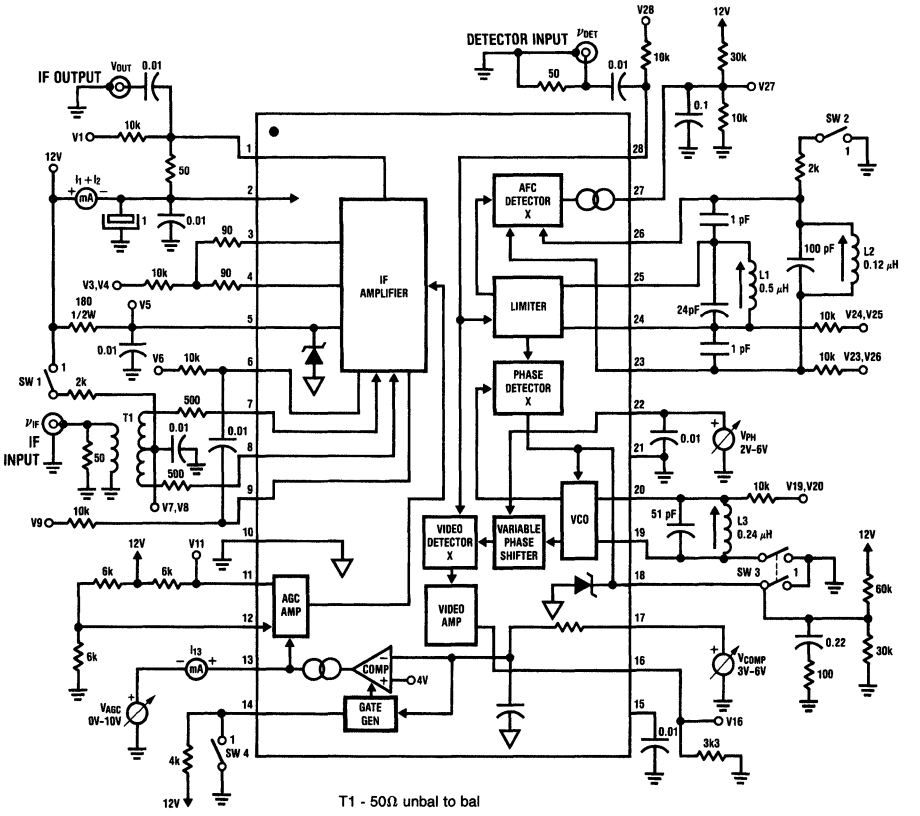
General Description

The LM1823 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous amplitude detector, self-contained gated AGC, and a switchable AFC detector. The increased flexibility of the LM1823 makes it suitable for a wide variety of television applications where high quality video or sound carrier recovery is required. These include home receiver video IFs, cable and subscription TV decoders, and parallel sound IF/intercarrier detector systems. Typical operating frequencies are 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Low differential gain and phase
- IF and detector pin compatible with LM1822
- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Uncommitted AGC comparator input
- Internal AGC gate generator
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- 9 MHz video bandwidth
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 - 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 - 9½T
L2 - 4½T
L3 - 6½T
#22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

TL/H/5222–1

Order Number LM1823N
See NS Package N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V2	15V
IF Supply Current, I_5	60mA
AGC Gate Voltage, V14	±5V
Video Output Current, I_{16}	10 mA
PLL Filter Current, I_{18}	5 mA
Detector Input Signal, v_{DET}	1 Vrms
Power Dissipation	2W
Thermal Resistance, θ_{JA}	50° C/W
Junction Temperature	125°C
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

DC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

$T_A = 25°C$, Test Circuit, $v_{IF} = v_{DET} = 0$, $V_{PH} = 4V$, $V_{COMP} = 4V$, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
12V Supply Current, $I_1 + I_2$	$V_{AGC} = 6.7V$. $V_{COMP} = 6V$	35	60	80	mA
IF Regulator Voltage, V5	$V_{AGC} = 6.7V$, SW4 Position 1	5.8	6.4	7.0	V
IF Input Voltage, V7, V8	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	3.2	3.7	4.1	V
IF Decouple Offset, V6–V9	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1		0	±30	mV
IF Peaker Voltage (Max Gain), V3, V4	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	2.3	3.0	3.6	V
IF Output Current, I1	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1, Measure V1, $I_1 = (12 - V1)/50$	3.1	5.5	7.8	mA
IF Peaker Voltage (Min Gain), V3, V4	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1	5.5	6.2		V
Detector Input Voltage, V28	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
Limiter Tank Voltage, V24, V25	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	6.4	7.0	7.6	V
AFC Tank Voltage, V23, V26	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
VCO Tank Voltage, V19, V20	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.7	5.2	5.7	V
AGC Sync Threshold, V17	SW 1, 2 Position 1, Adjust V_{COMP} for $I_{13} = 0$	3.8	4.0	4.2	V
AGC Filter Leakage Current, I_{13}	SW 1, 2, 4 Position 1		0	±5	μA
AGC Filter Charge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 3.5V$	1.6	2.2	2.8	mA
AGC Filter Discharge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 4.5V$	−0.45	−0.70	−0.90	mA
RF AGC Leakage current, I_{11}	$V_{AGC} = 2V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$		0	20	μA
RF AGC Output Current, I_{11}	$V_{AGC} = 10V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$	1.5	1.8		mA

Detector AC Set-Up Procedure SW 1, 4 position 1, $V_{AGC}=0V$

1. Apply $v_{DET}=10$ mVrms, 45.75 MHz CW at the detector input. Tune L1 for maximum AC signal at pin 25, measured with a 10x FET probe or through a 1 pF capacitor to prevent loading of the limiter tank.
2. Increase v_{DET} to 60 mVrms. Adjust L3 until the PLL locks, as indicated by a DC voltage at the video output pin 16.
3. With the detector locked, adjust L3 for 4.0V at pin 18.
4. Adjust V_{PH} for maximum detector efficiency by monitoring pin 16 for a minimum DC voltage.
5. Adjust L2 for 3.0V at pin 27 (on sensitive slope of AFC curve).

AC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

T_A = 25°C, Test Circuit, detector set-up as above, f = 45.75 MHz, V_{AGC} = 6.7V, V_{COMP} = 4V, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
IF Amplifier Gain, v_{OUT}/v_{IF} (Note 1)	$V_{AGC}=2V$, SW 2, 3, 4 Position 1, $v_{IF}=500\ \mu$Vrms	25	35		dB
V_{AGC} for 15 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF}=2.8$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	4.2	4.6	5.0	V
V_{AGC} for 45 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF}=89$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	5.1	5.5	6.1	V
Zero Carrier Level, V16	SW 1, 2, 4 Position 1, $v_{DET}=0$	6.6	7.4	8.4	V
Detected Output Level, ΔV16	SW 1, 2, 4 Position 1, $v_{DET}=60$ m/Vrms, Measure Change in V16 from Zero Carrier Test	2	3	4.3	V
Overload Output Voltage, V16	SW 1, 2, 4 Position 1, $v_{DET}=600$ mVrms		2	3	V
AFC Output Voltage (OFF), V27	SW 1, 2, 4 Position 1, $v_{DET}=0$	2.8	3.0	3.2	V
AFC Minimum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, 46.75 MHz		0.5	1.0	V
AFC Maximum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, 44.75 MHz	9	10		V
PLL Pull-In Range, Δf	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, Vary Frequency and Measure the Difference between Lock Points	2	3		MHz

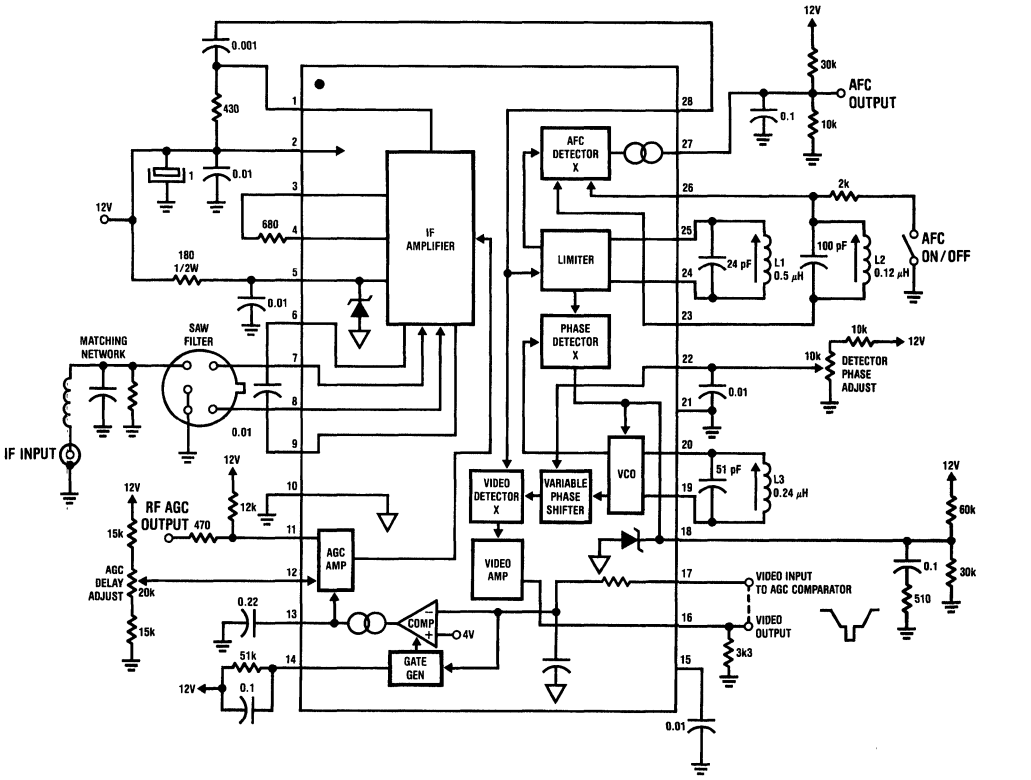
Note 1: The IF amplifier gain is specified with the IF output connected to a 50Ω measurement system which results in a 25Ω loaded impedance. The gain in an actual application will typically be 26 dB higher.

Design Parameters NOT TESTED OR GUARANTEED Typical Application Circuit

Parameter	Typ	Units
Maximum System Operating Frequency	70	MHz
IF Input Impedance (Differential Pin 7–8), 45 MHz	60	Ω
IF Output Impedance, 45 MHz	10	kΩ
IF Gain Control Range	55	dB
Detector Input Impedance, 45 MHz	2	kΩ
Detector Output Bandwidth, −3 dB	9	MHz
Detector Differential Gain (Note 2)	3	%
Detector Differential Phase (Note 2)	1	deg
Detector Output Harmonic Levels below 3 Vp-p Video	−40	dB
VCO Temperature Coefficient	−150	ppm/°C

Note: 2: Differential gain and phase measured with the limiter tank adjusted for minimum differential phase.

Typical Application 45.75 MHz (see Application Notes)



TL/H/5222–2

SAW Filter - MuRata SAF45MC/MA

L1 - 9½T
L2 - 4½T
L3 - 6½T
#22 wire on 3.16" form with HF core, shielded

All caps in µF unless noted

Application Notes Refer to Typical Application Circuit

COMMENTS ON RF Coupling

The LM1823 is a high gain RF system which is critically dependent on the ground plane and positioning of the external components. For this reason, it is suggested that the printed circuit layout shown in *Figure 3* be strictly adhered to.

The most sensitive points in the system to unwanted RF coupling are the IF input pins 6–9. There are two different signals which can cause different problems when coupling into the IF inputs. If the IF output is coupling to the input, it can cause bandpass tilting, peaking, and in extreme cases, oscillation. The other signal which can couple to the IF inputs is the PLL detector VCO. This VCO coupling can cause AFC skewing, non-symmetrical detector pull-in, and failure of the detector to acquire lock at weak signal levels. These input coupling problems will be most acute at maximum gain and will decrease as the IF is gain reduced by AGC action.

The differential IF inputs offer a large amount of inherent rejection to unwanted RF coupling. Therefore, A FULLY BALANCED INPUT SOURCE IS MANDATORY. The input leads must be routed together and socketless operation is recommended above 50 MHz. However, residual coupling may still dictate the maximum IF amplifier gain which can be taken (see Pin Descriptions).

PIN DESCRIPTIONS

Pin 1-IF Amplifier Output: Pin 1 is connected to an open-collector NPN device. The load on pin 1 must be returned to the 12V supply as close as possible to pin 2. The IF output load may be either resistive as shown in the Typical Application, or an LC tank. The tank need only be used if a tunable bandpass characteristic is desired, or in conjunction with a sound trap.

Pin 2–12V Supply: The LM1823 requires a nominal 12V supply but can accept a ±10% variation. Pin 2 must be RF decoupled to a good ground as close as possible to the IC.

Pins 3, 4-IF Gain Adjustment: Pins 3 and 4 are connected to the two emitters of the 4th IF differential amplifier such that the gain of the stage is set by the impedance between the pins. There is an internal 1360Ω resistor to set the minimum gain when the pins are left open. Adding an external resistor increases the gain by the ratio of the parallel impedance to the original 1360Ω. The pin 3 to 4 external resistor primarily affects the maximum IF gain; the relative gain increase goes away over the first 20 dB of AGC.

Pin 5-IF Supply: The IF supply employs an internal 6.4V shunt regulator which is fed by an external dropping resistor from pin 2 to pin 5. RF decoupling from pin 5 to the pin 10 ground plane is critical.

Pins 6–9-IF Input and Decouple Pins: The LM1823 uses a common-base differential input stage as shown in *Figure 1*. Pins 7 and 8 connect directly to the emitters of the input devices, while pins 6 and 9 decouple the DC feedback loop at the bases.

The gain of a common-base amplifier depends inversely on the source impedance. The LM1823 is designed to operate from differential impedances in the 500Ω to 2000Ω range, which is typical for surface acoustic wave (SAW) filters. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained. In all cases a balanced source must be used.

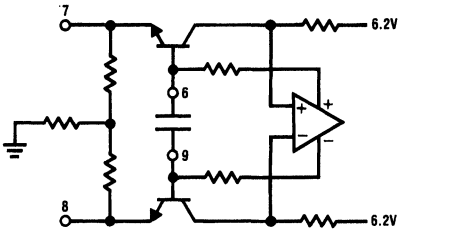


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FIGURE 1. IF Input Stage

Both the input network to pins 7 and 8 and decoupling capacitor between pin 6 and pin 9 must be as close to the device as is physically possible to minimize RF coupling.

Pin 10-IF Ground: Pin 10 grounds the IF and AGC circuits in the LM1823. It is separate from the detector and chip substrate grounds to prevent internal coupling.

Pin 11-RF AGC Output: Pin 11 is connected to an open-collector NPN device. It begins to conduct current when the voltage on the AGC filter capacitor at pin 13 exceeds the voltage set at the takeover pin 12 by approximately 0.6V. When connected to a resistor to 12V, this produces a falling voltage at pin 11 suitable for reverse tuner AGC inputs.

Pin 12-RF AGC Takeover Adjust: The voltage preset at pin 12 determines when the IF stops gain reducing and the tuner begins gain reducing as the pin 13 AGC filter capacitor voltage increases with signal level. A higher voltage at pin 12 delays the RF AGC takeover until more IF gain reduction has been taken (higher signal levels), while a lower voltage limits the IF gain reduction before RF takeover.

When the LM1823 is being used without a tuner, pin 12 may be connected to supply.

Pin 13-AGC Filter: Pin 13 is a push-pull current source output from the AGC comparator. The comparator compares the negative sync tips of noise-averaged pin 17 video with an internal 4V reference. Increases in signal produce a current out of pin 13 which charges the filter capacitor, while decreases discharge the capacitor. The resulting change in voltage at pin 13 controls the IF and tuner gains to maintain the pin 17 sync tip level at 4V. An optional capacitor between pin 13 and the takeover pin 12 couples the ripple produced by a rapidly varying signal into the takeover pin to enhance the AGC loop response.

Pin 14-AGC Gate Generator Time Constant: The AGC comparator is gated on during sync time by a pulse from an internal gate generator. The gate pulse which activates the comparator is derived from the sync pulse in the same video which feeds the comparator input (see pin 17 description). An RC time constant on pin 14 determines the slice level on the leading edge of the sync pulse at which the comparator is gated on. This level is approximately $V_{SLICE} = 1/(2RC)$ in millivolts above the sync tip, and should be set at ≤25% of the sync amplitude. Note that V_{SLICE} only determines when the AGC comparator turns on, and is unrelated to the comparator reference.

In the Typical Application, $V_{SLICE} = 100$ mV, or 10% of a 1V sync pulse. Increasing V_{SLICE} improves the AGC recovery from step changes in signal level but increases the risk of video interaction. When modifying the time constant, change the capacitor value only.

Application Notes (Continued) Refer to Typical Application Circuit

Pin 15-Supply Decouple: Pin 15 is an additional connection to the 12V supply to allow RF decoupling on the detector side of the chip.

Pin 16-Video Output: Pin 16 is a Darlington NPN emitter-follower output supplying negative sync video. With no detector input signal the pin 16 voltage sits at the zero carrier level, representing peak white. As the input signal level increases, the pin 16 voltage decreases towards black. The sync pulses are normally the most negative portion of the recovered video.

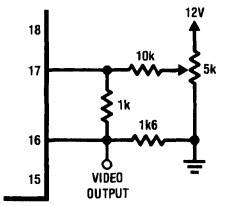

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FIGURE 2. Adjustable Recovered Video Level

Pin 17-AGC Comparator Input: External negative sync video is fed to the AGC comparator and gate generator via pin 17. An internal low pass filter removes high frequency noise and transients. The peak-to-peak video level with the AGC loop active is determined by the difference between the zero carrier level at pin 17 and the 4V sync tip level being held by the AGC comparator (see pin 13 description).

When the LM1823 is being used to recover normal video, pin 17 may simply be returned to pin 16. This results in a nominal 3 Vp-p video level, but which is subject to variations in the pin 16 zero carrier level. The network shown in *Figure 2* can be used to change the zero carrier at pin 17, thus providing an adjustable recovered video level. The pin 16 video level should be maintained at between 1 Vp-p minimum and 4 Vp-p maximum.

In suppressed sync systems, the recovered video at pin 16 may require processing to restore normal sync amplitude before being fed to pin 17. In this case, it is mandatory that a DC path be maintained for the zero carrier level through any external circuitry. Any DC level shift between pins 16 and 17 will have the effect of changing the video level as previously described.

Pin 18-PLL Filter: Pin 18 is connected to both the output of the phase detector and the control input of the VCO. The polarity of the VCO control characteristic is such that increasing the pin 18 voltage increases the VCO frequency. An external resistive divider at pin 18 serves two functions. The divider parallel impedance sets the gain of the phase detector, while the divider ratio places the quiescent voltage at the center of the VCO control characteristic. The 20 kΩ impedance, ⅓ supply divider shown in the Typical Application has been chosen to provide optimum performance. The series capacitor and resistor to ground complete the PLL filter.

An internal zener clamp to ground at pin 18 prevents the phase detector output from pulling the VCO control input over 5.6V. For this reason, external voltages should not be forced at pin 18 to avoid damaging the clamp.

Pins 19, 20-VCO Tank: A parallel LC tank between pins 19 and 20 sets the VCO center frequency. The tank Q is RpL/Xc, where RpL is the coil Rp loaded by an internal 1500Ω resistor. Increasing the Q (larger C) improves stability but reduces the VCO control range. The tank shown in the Typical Application will yield a loaded Q of around 15, providing stable operation with a control range in excess of 2 MHz.

Pin 21-Substrate Ground: Pin 21 grounds the chip substrate along with all of the AFC and PLL detector grounds.

Pin 22-Detector Phase Adjust: The video detector requires a reference signal in phase with the input signal carrier for maximum detection efficiency. However, the action of the PLL inherently sets the VCO phase in quadrature (at 90 degrees) with the limiter output. Therefore a variable phase shift network, controlled by pin 22, is used internally between the VCO and video detector to insure proper phasing. Pin 22 requires an adjustment voltage centered at ⅓ supply with ±2V of control range.

The pin 22 adjustment procedure described in the Detector AC Set-Up Procedure is an open loop approach where the voltage is adjusted for maximum detected output with a fixed detector input signal. In the Typical Application, with the detector input being fed from the IF amplifier and the AGC loop active, the pin 22 adjustment is made by maximizing the AGC filter voltage at pin 13. In all cases the detector phase adjustment must be performed after the limiter is tuned.

Pins 23, 26-AFC Tank: A parallel LC tank between pins 23 and 26 sets the center of the AFC characteristic. The internal resistance is typically 20 kΩ, so that Q will be dominated by the coil Rp. The L/C ratio shown in the Typical Application maximizes Q to provide a steep AFC output slope.

A quadrature input signal is required at the AFC tank to operate the AFC detector. This signal is derived by light capacitive coupling from the limiter tank. For applications at 45 MHz and above, the stray printed circuit capacitance from the adjacent limiter tank couples sufficient signal for proper operation. However, at lower IF frequencies, small (1 pF–5 pF) capacitors may be required between the adjacent pins as shown in the Test Circuit.

A second function of pins 23 and 26 allows turning the AFC detector OFF by grounding either side of the AFC tank. Up to 2 kΩ may be placed in series with the switch connection to prevent unbalancing the tank.

Pins 24, 25-Limiter Tank: A parallel LC tank between pins 24 and 25 forms the tuned load for a single stage limiting amplifier which strips amplitude information from the signals feeding the AFC and phase detectors. The amplifier has a small signal gain of approximately 50, with internal Schottky diodes across the tank to limit the output amplitude to 500 mVp-p.

The linearity of the detector video outputs depends directly on limiter tuning. Making the limiter adjustment based on maximum signal level at pins 24, 25 as outlined in the Detector AC Set-Up Procedure results in nearly optimum output linearity. However, to completely null the output differential phase the limiter should be adjusted while monitoring this parameter.

Pin 27-AFC Detector Output: Pin 27 is push-pull current source output from the AFC detector. The polarity is such that pin 27 sources current when the input signal is below the center frequency, and sinks current above the center frequency. An external resistive divider sets both the gain and quiescent output voltage of the AFC. Although the net-

Application Notes (Continued) Refer to Typical Application Circuit

work shown in the Typical Application sets up the output at ¼ supply, it could easily be changed to ½ supply by using equal-valued resistors. When setting up the AFC detector, the tank should always be tuned so the output is at the quiescent divider voltage with the desired center frequency applied.

Pin 28-Detector Input: Pin 28 is internally DC-biased and requires an AC-coupled input signal. The network between pins 1 and 28 should not allow over 1 Vrms at the input during signal transients to prevent overloading the detector. When a tank is being used for the IF output load, a capacitive divider may be used from pin 1 to pin 28 in which the series equivalent capacitance resonates with the coil.

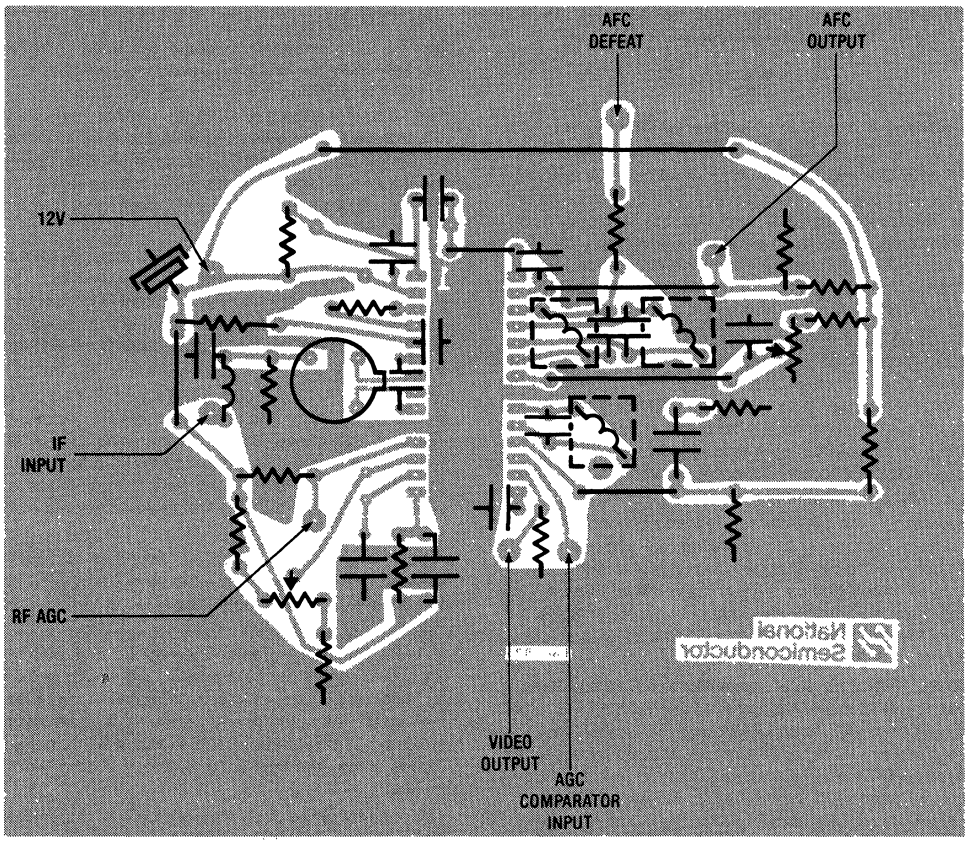

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FIGURE 3. Printed Circuit Layout (Component Side).

National Semiconductor

LM1881 Video Sync Separator

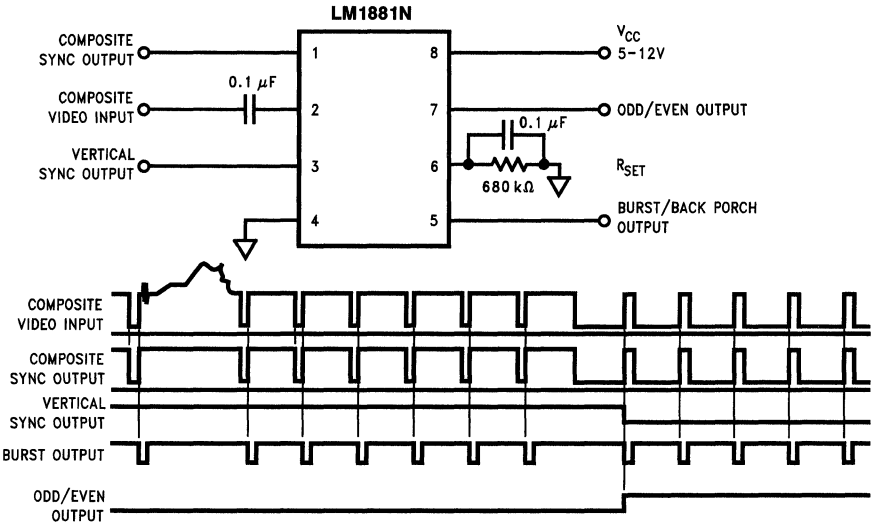
General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL*, and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 kΩ input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Horizontal scan rates to 150 kHz
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

Connection Diagram



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Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

*PAL in this datasheet refers to European broadcast TV standard "Phase Alternating Line", and not to Programmable Array Logic.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	13.2V
Input Voltage	3 Vpp (V_{CC} = 5V) 6 Vpp ($V_{CC} \geq$ 8V)
Output Sink Currents; Pins 1, 3, 5	5 mA
Output Sink Current; Pin 7	2 mA
Package Dissipation (Note 1)	1100 mW
Operating Temperature Range	0°C − 70°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 2)	2 kV
Soldering Information	
Dual-in-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_{CC} = 5V; Rset = 680 kΩ; T_A = 25°C; Unless otherwise specified

Parameter	Conditions		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Limits)
Supply Current	Outputs at Logic 1	V_{CC} = 5V	5.2	10		mAmax
		V_{CC} = 12V	5.5	12		mAmax
DC Input Voltage	Pin 2		1.5	1.3		Vmin
				1.8		Vmax
Input Threshold Voltage	Note 5		70	55		mVmin
				85		mVmax
Input Discharge Current	Pin 2; V_{IN} = 2V		11	6		μAmin
				16		μAmax
Input Clamp Charge Current	Pin 2; V_{IN} = 1V		0.8	0.2		mAmin
R_{SET} Pin Reference Voltage	Pin 6; Note 6		1.22	1.10		Vmin
				1.35		Vmax
Composite Sync. & Vertical Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V	4.5	4.0		Vmin
		V_{CC} = 12V		11.0		Vmin
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5V	3.6	2.4		Vmin
		V_{CC} = 12V		10.0		Vmin
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 μA; Logic 1	V_{CC} = 5V	4.5	4.0		Vmin
		V_{CC} = 12V		11.0		Vmin
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1		0.2	0.8		Vmax
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3		0.2	0.8		Vmax
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5		0.2	0.8		Vmax
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7		0.2	0.8		Vmax
Vertical Sync Width			230	190		μsmin
				300		μsmax
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		4	2.5		μsmin
				4.7		μsmax
Vertical Default Time	Note 7		65	32		μsmin
				90		μsmax

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110° C/W, junction to ambient.

Note 2: ESD susceptibility test uses the "human body model, 100 pF discharged through a 1.5 kΩ resistor".

Note 3: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 4: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

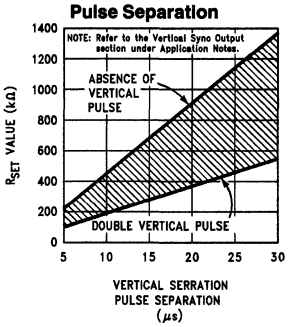
Note 5: Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 6: Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the R_{SET} pin (Pin 6).

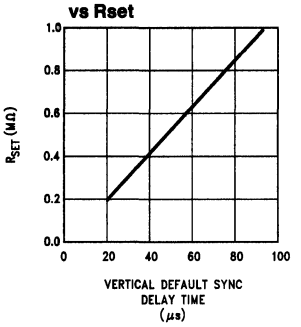
Note 7: Delay time between the start of vertical sync (at input) and the vertical output pulse.

Typical Performance Characteristics

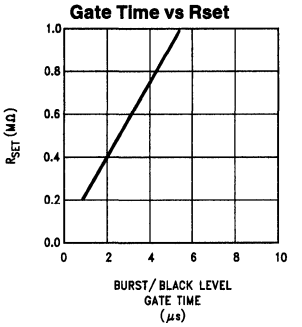
R_{set} Value Selection vs Vertical Serration Pulse Separation



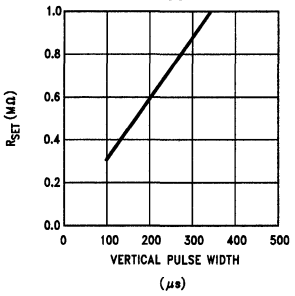
Vertical Default Sync Delay Time vs Rset



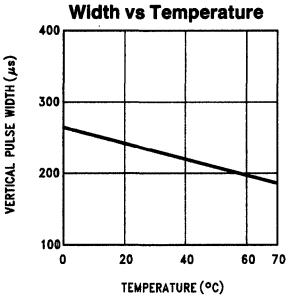
Burst/Black Level Gate Time vs Rset



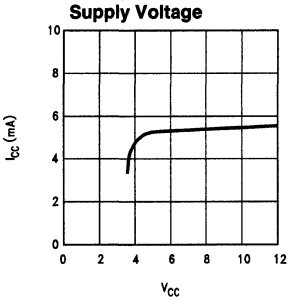
Vertical Pulse Width vs Rset



Vertical Pulse Width vs Temperature



Supply Current vs Supply Voltage



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Application Notes

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components beside power supply and set current decoupling are the input coupling capacitor and a single resistor that sets internal current levels, allowing the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C: composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the LM1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the LM1881 timing information and the type of signals that are used, refer to *Figure 2(a–e)* which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

COMPOSITE SYNC OUTPUT

The composite sync output, *Figure 2(b)*, is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on *Figure 2(a)*). This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA, whereas the discharge current is only 11 μA, typically. This allows relatively small capacitor values to be used—0.1 μF is generally recommended.

Normally the signal source for the LM1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform *(Figure 3)*. To understand the generation of the vertical sync pulse, refer to the lower left hand section *Figure 3*. Note that there are two comparators in the section. One comparator has an internally generated voltage reference called V_1 going to one of its inputs. The other comparator has an internally generated voltage reference called V_2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are **positive** going sync pulses. The capacitor to the integrator is internal to the LM1881. The capacitor charge current is set by the value of the external resistor R_{set}. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V_1. During the vertical sync period the narrow going positive pulses shown in *Figure 2* is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first Serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration pulse the integrator output should be between V_1 and V_2. This would give a high level at the output of the comparator with V_1 as one of its inputs. This high is clocked into the "D" flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the LM1881). The "Q" output of the "D" flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN "D" flip-flop. The ODD/EVEN field pulse operation is covered in the next section. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external R_{set}. The "$\overline{Q}$" output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the LM1881. By clocking the "D" flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the internal oscillator as shown in *Figure 2*.

How R_{set} affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is "R_{set} Value Selection vs Vertical Serration Pulse Separation". For this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal

Application Notes (Continued)

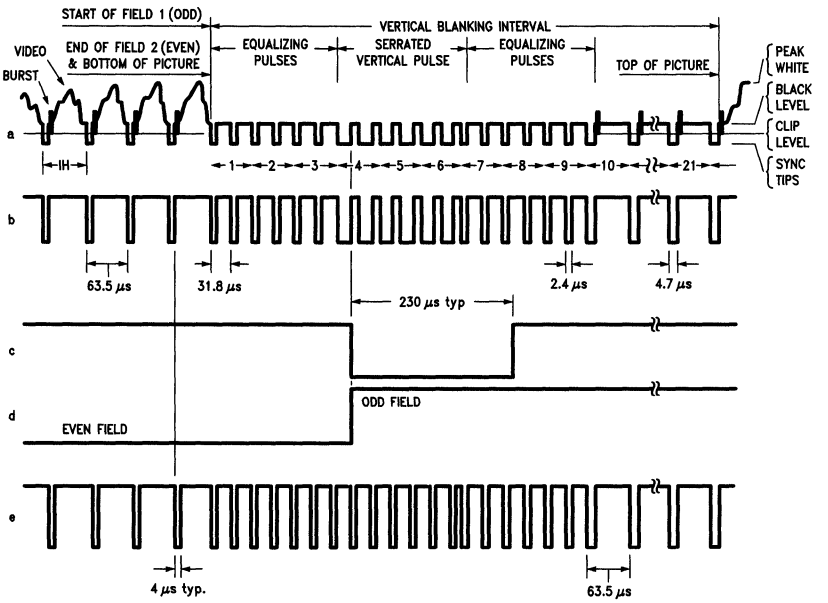

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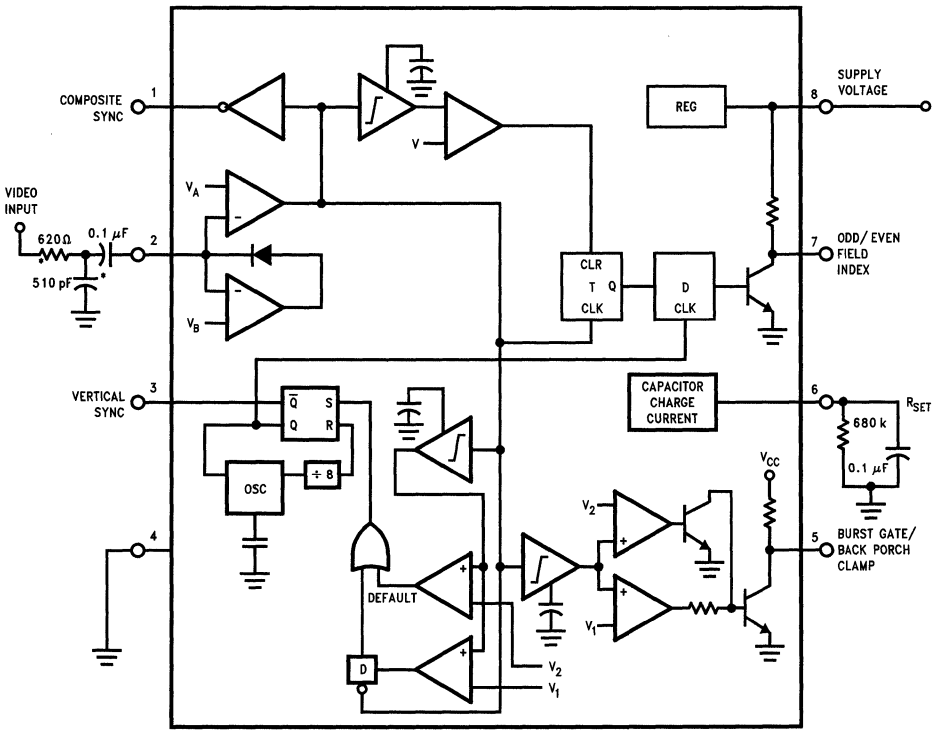
FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp



*Components Optional, See Text

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FIGURE 3

Application Notes (Continued)

half line). Remember this pulse is a positive pulse at the integrator but negative in *Figure 2*. This graph shows how long it takes the integrator to charge its internal capacitor above V_1.

WITH R_{set} too large the charging current of the integrator will be too small to charge the capacitor above V_1, thus there will be no vertical synch output pulse. As mentioned above, R_{set} also sets the frequency of the internal oscillator. If the oscillator runs too fast its eight cycles will be shorter than the vertical sync portion of the composite sync. Under this condition another vertical sync pulse can be generated on one of the later serration pulses after the divide by 8 circuit resets the R/S flip-flop. The first graph also shows the minimum R_{set} necessary to prevent a double vertical pulse, assuming that the serration pulses last for only three full horizontal line periods (six serration pulses for NTSC). The actual pulse width of the vertical sync pulse is shown in the "Vertical Pulse Width vs R_{set}" graph. Using NTSC as an example, lets see how these two graphs relate to each other. The Horizontal line is 64 μs long, or 32 μs for a horizontal half line. Now round this off to 30 μs. In the "R_{set} Value Selection vs Vertical Serration Pulse Separation" graph the minimum resistor value for 30 μs serration pulse separation is about 550 kΩ. Going to the "Vertical Pulse Width vs R_{set}" graph one can see that 550 kΩ gives a vertical pulse width of about 180 μs, the total time for the vertical sync period of NTSC (3 horizontal lines). A 550 kΩ will set the internal oscillator to a frequency such that eight cycles gives a time of 180 μs, just long enough to prevent a double vertical sync pulse at the vertical sync output of the LM1881.

The LM1881 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V_2. Since there is no falling edge at the end of a serration pulse to clock the "D" flip-flop, the only high signal going to the OR gate is from the default comparator when output of the integrator reaches V_2. At this time the R/S flip-flop is toggled by the default comparator, starting the vertical sync pulse at pin 3 of the LM1881. If the default vertical sync period ends before the end of the input vertical sync period, then the falling edge of the vertical sync (positive pulse at the "D" flip-flop) will clock the high output from the comparator with V_1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The "Vertical Default Sync Delay Time vs R_{set}" graph shows the relationship between the R_{set} value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again the smallest resistor for R_{set} is 500 kΩ. The vertical default time delay is about 50 μs, much longer than the 30 μs serration pulse spacing.

A common question is how can one calculate the required R_{set} with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the "Vertical Default Sync Delay Time vs R_{set}" graph to select the necessary R_{set} to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the "Vertical Pulse Width vs R_{set}" graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard a horizontal line is 32 μs long. The vertical sync period is two horizontal lines long, or 64 μs. The vertical default sync delay time **must be longer** than the vertical sync period of 64 μs. In this case R_{set} must be larger than 680 kΩ. R_{set} must still be small enough for the output of the integrator to reach V_1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that R_{set} is small enough for the integrator. Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 μs in this example. This graph is linear, meaning that a value as large as 2.7 MΩ can be used for R_{set} (twice the value as the maximum at 30 μs). Due to leakage currents it is advisable to keep the value of R_{set} under 2.0 MΩ. In this example a value of 1.0 MΩ is selected, well above the minimum of 680 kΩ. With this value for R_{set} the pulse width of the vertical sync output pulse of the LM1881 is about 340 μs.

ODD/EVEN FIELD PULSE

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur only in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the "odd field" or "field 1". The "even field" or "field 2" has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. *Figure 2(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the LM1881 again integrates the composite sync waveform *(Figure 3)*. A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flipflop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this

Application Notes (Continued)

threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60–120 Hz) vertical scan rates.

APPLICATIONS

Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field level allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR

The circuit in *Figure 4* puts out a single video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION

The circuit in *Figure 5* will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.

Typical Applications

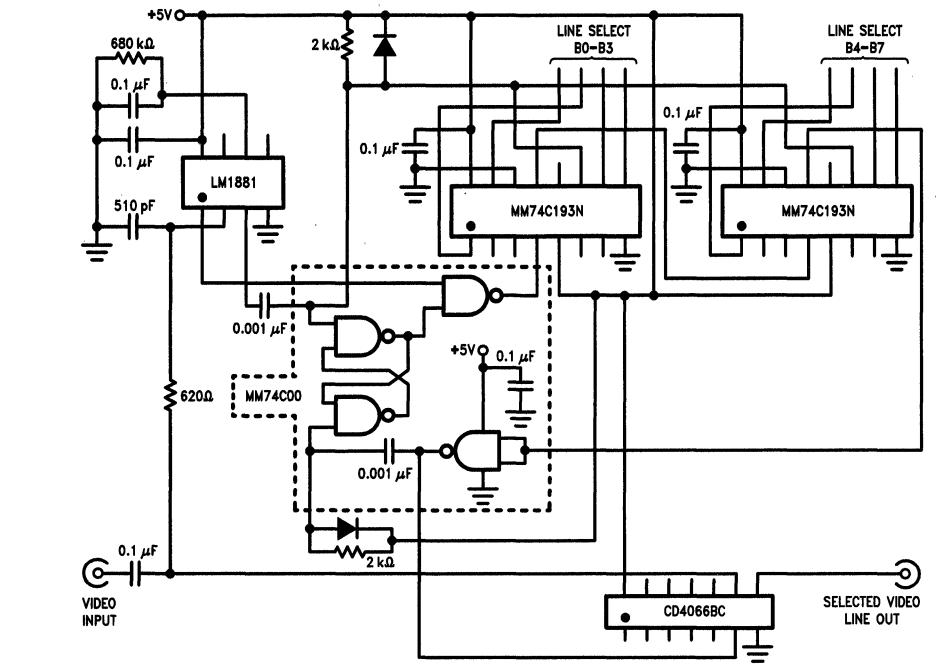

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FIGURE 4. Video Line Selector

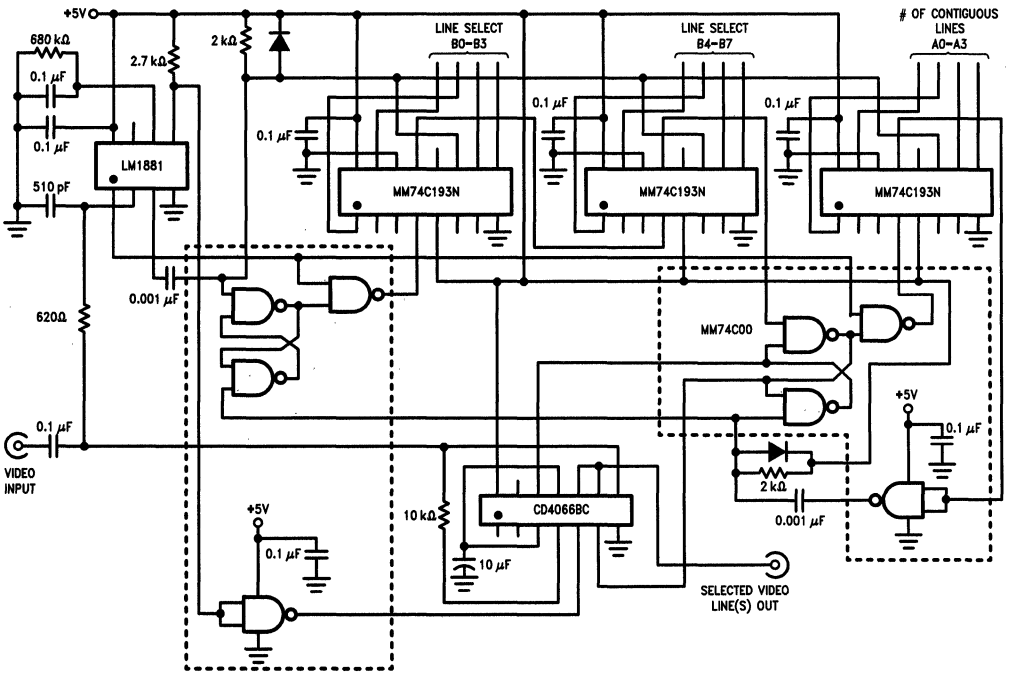

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FIGURE 5. Multiple Contiguous Video Line Selector With Black Level Restoration

National Semiconductor

54ACT/74ACT715•LM1882
54ACT/74ACT715-R•LM1882-R
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R are 20-pin TTL-input compatible devices capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The devices are capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

These devices make no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

The 'ACT715/LM1882 is mask programmed to default to a Clock Disable state. Bit 10 of the Status Register, Register 0, defaults to a logic "0". This facilitates (re)programming before operation.

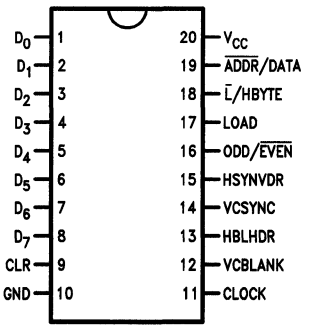
The 'ACT715-R/LM1882-R is the same as the 'ACT715/LM1882 in all respects except that the 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enabled state. Bit 10 of the Status Register defaults to a logic "1". Although completely (re)programmable, the 'ACT715-R/LM1882-R version is better suited for applications using the default 14.31818 MHz RS-170 register values. This feature allows power-up directly into operation, following a single CLEAR pulse.

Features

- Maximum Input Clock Frequency > 130 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- 4 KV minimum ESD immunity
- 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enable state for easier start-up into 14.31818 MHz RS170 timing

Connection Diagrams

Pin Assignment for DIP and SOIC



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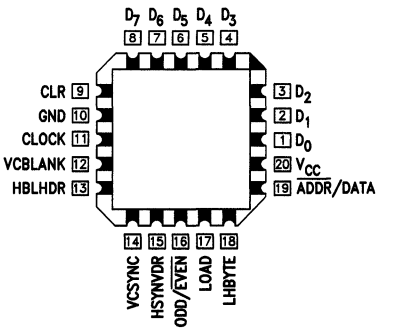
Order Number LM1882CN or LM1882CM
For Default RS-170, Order Number LM1882-RCN or LM1882-RCM

Pin Assignment for LCC



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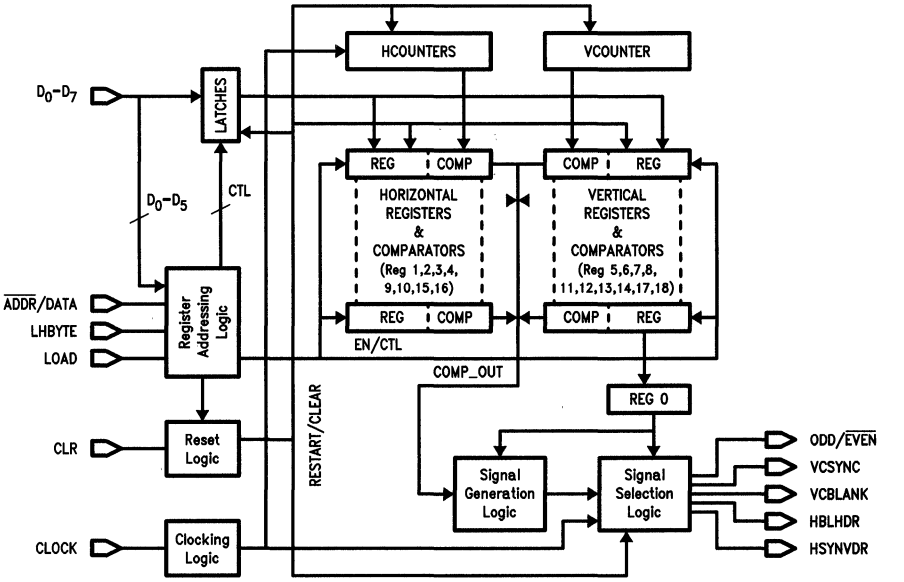
Logic Block Diagram



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Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0–D7: The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

L/HBYTE: The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The LOAD control pin loads data into the Address or Data Registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the LOAD. The LOAD pin has been implemented as a Schmitt trigger input for better noise immunity.

CLOCK: System CLOCK input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity. The CLOCK and the LOAD signal are asynchronous and independent. Output state changes occur on the falling edge of CLOCK.

CLR: The CLEAR pin is an asynchronous input that initializes the device when it is HIGH. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The CLEAR pin has been implemented as a Schmitt trigger for better noise immunity. A CLEAR pulse should be asserted by the user immediately after power-up to ensure proper initialization of the registers—even if the user plans to (re)program the device.

Note: A CLEAR pulse will disable the CLOCK on the 'ACT715/LM1882 and will enable the CLOCK on the 'ACT715-R/LM1882-R.

ODD/EVEN: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this output is always HIGH. Data can be serially scanned out on this pin during Scan Mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register. Equalization and Serration pulses will (if enabled) be output on the VCSYNC signal in composite mode only.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or Cursor Position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs. The default value for the Status Register is 0 (000 Hex) for the 'ACT715/LM1882 and is "512" (200 Hex) for the 'ACT715-R/LM1882-R.

Register Description (Continued)

Bits 0–2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0	CBLANK	CSYNC	HGATE	VGATE
(DEFAULT)						
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Bits 3–4

B_4	B_3	Mode of Operation
0	0	Interlaced Double Serration and Equalization
(DEFAULT)		
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Double Equalization and Serration mode will output equalization and serration pulses at twice the HSYNC frequency (i.e., 2 equalization or serration pulses for every HSYNC pulse). Single Equalization and Serration mode will output an equalization or serration pulse for every HSYNC pulse. In Interlaced mode equalization and serration pulses will be output during the VBLANK period of every odd and even field. Interlaced Single Equalization and Serration mode is not possible with this part.

Bits 5–8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates an output pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9–11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

Default values for B10 are "0" in the 'ACT715/LM1882 and "1" in the 'ACT715-R/LM1882-R.

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

This bit is not intended for the user but is for internal testing only.

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. All values of the horizontal timing registers are referenced to the falling edge of the Horizontal Blank signal (see *Figure 1*). Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Horizontal Blank reference pulse, edges referenced to this first Horizontal edge are n + 1 CLOCKs away, where "n" is the width of the timing in question. Registers 1, 2, and 3 are programmed in this manner. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This

Signal Specification (Continued)

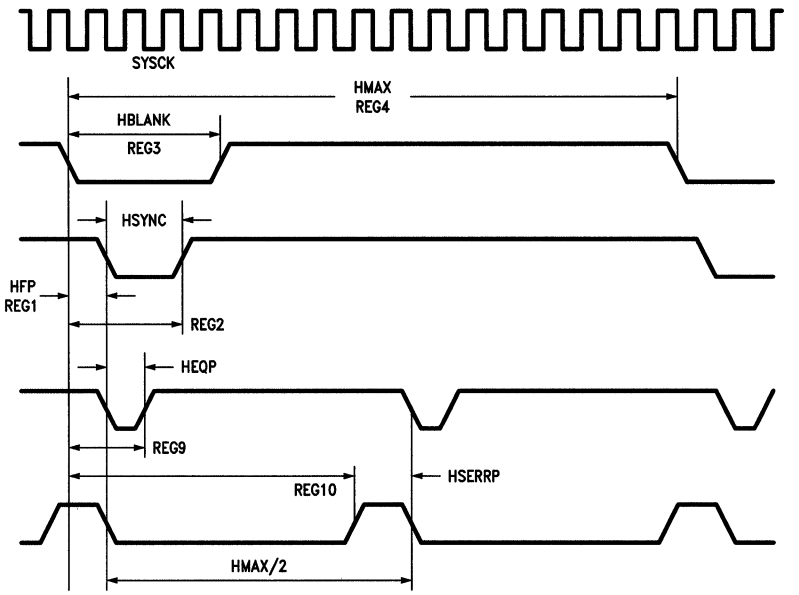

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FIGURE 1. Horizontal Waveform Specification

limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4) × ckper

Horizontal Blanking Width = [REG(3) − 1] × ckper

Horizontal Sync Width = [REG(2) − REG(1)] × ckper

Horizontal Front Porch = [REG(1) − 1] × ckper

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Vertical Blank (first Horizontal Blank) reference pulse, edges referenced to this first edge are n + 1 lines away, where "n" is the width of the timing in question. Registers 5, 6, and 7 are programmed in this manner. Also, in the interlaced mode, vertical timing is based on half-lines. Therefore registers 5, 6, and 7 must contain a value twice the total horizontal (odd and even) plus 1 (as described above). In non-interlaced mode, all vertical timing is based on whole-lines. Register 8 is always based on whole-lines and does not add 1 for the first clock. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC. (See *Figure 2A*.)

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width = [REG(7) − 1] × hper/n

Vertical Syncing Width = [REG(6) − REG(5)] × hper/n

Vertical Front Porch = [REG(5) − 1] × hper/n

where n = 1 for noninterlaced
n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The Serration pulse interval occurs in place of the Vertical Sync interval. Equalization pulses occur preceding and/or following the Serration pulses. The width and location of these pulses can be programmed through the registers shown below. (See *Figure 2B*.)

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper
REG 9 = (HFP) + (HEQP) + 1

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper
REG 10 = (HFP) + (HPER/2) − (HSERR) + 1

Where n = 1 for noninterlaced single serration/equalization
n = 2 for noninterlaced double serration/equalization
n = 2 for interlaced operation

Signal Specification (Continued)

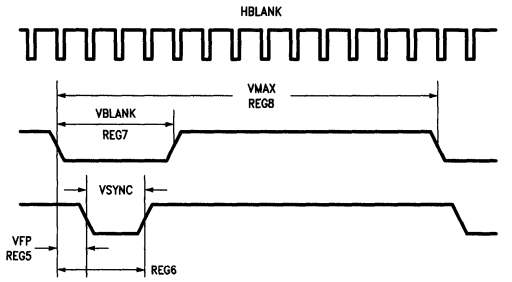

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FIGURE 2A. Vertical Waveform Specification

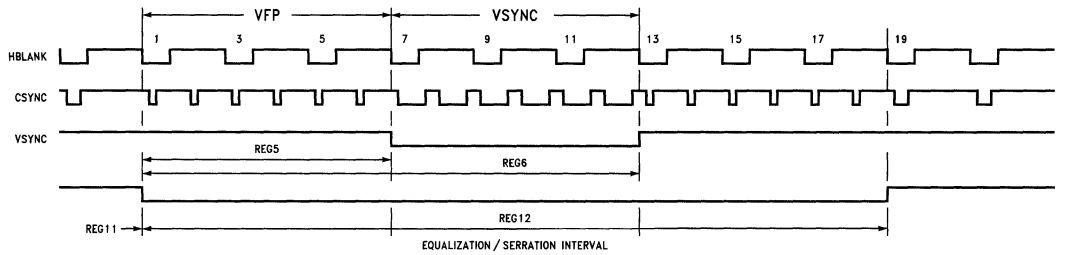

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FIGURE 2B. Equalization/Serration Interval Programming

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal Drive and Vertical Drive outputs can be utilized as general purpose Gating Signals. Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of Bit 2 of the Status Register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and Bit 2 of the Status Register is set to the value of 1. The Cursor Position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

Vertical Interrupt Width = [REG(14) − REG(13)] × hper

Addressing Logic

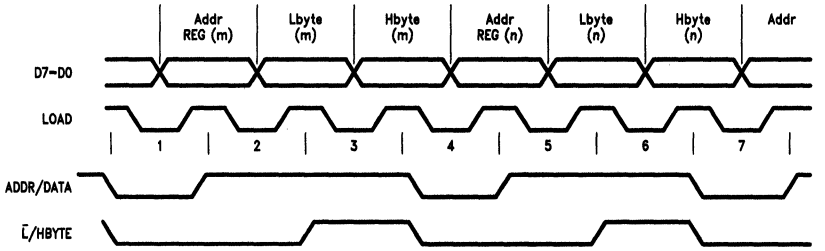
The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 load cycles (19 address and 38 data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 load cycles to completely program all registers (1 address and 38 data cycles). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of LOAD when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of LOAD after ADDRDATA and LHBYTE goes low.

Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n



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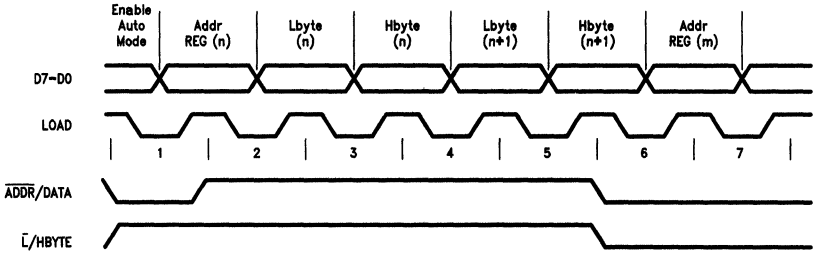
Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n+1)
5	Enable Hbyte Data Load	Load Hbyte (n+1); Inc Counter
6	Enable Manual Addressing	Load Address



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Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Two types of ADDRDEC logic is enabled by 2 pair of addresses, Addresses 22 or 54 (Vectored Restart logic) and Addresses 23 or 55 (Vectored Clear logic). Loading these addresses will enable the appropriate logic and put the part into either a Restart (all counter registers are reinitialized with preprogrammed data) or Clear (all registers are cleared to zero) state. Reloading the same ADDRDEC address will not cause any change in the state of the part. The outputs during these states are frozen and the internal CLOCK is disabled. Clocking the part during a Vectored Restart or Vectored Clear state will have no effect on the part. To resume operation in the new state, or disable the Vectored Restart or Vectored Clear state, another non-ADDRDEC address must be loaded. Operation will begin in the new state on the rising edge of the non-ADDRDEC load pulse. It is recommended that an unused address be loaded following an ADDRDEC operation to prevent data registers from accidentally being corrupted. The following Addresses are used by the device.

Address 0	Status Register REG0
Address 1–18	Data Registers REG1–REG18
Address 19–21	Unused
Address 22/54	Restart Vector (Restarts Device)
Address 23/55	Clear Vector (Zeros All Registers)
Address 24–31	Unused
Address 32–50	Register Scan Addresses
Address 51–53	Counter Scan Addresses
Address 56–63	Unused

At any given time only one register at most is selected. It is possible to have no registers selected.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the preprogramming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers to zero simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

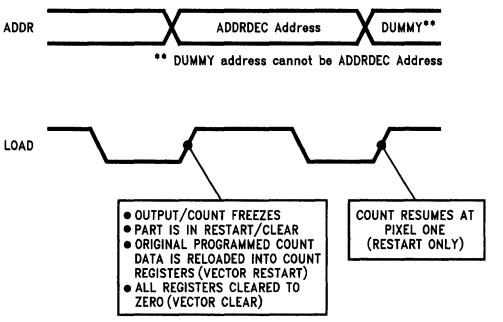

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FIGURE 3. ADDRDEC Timing

GEN LOCKING

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R is designed for master SYNC and BLANK signal generation. However, the devices can be synchronized (slaved) to an external timing signal in a limited sense. Using Vectored Restart, the user can reset the counting sequence to a given location, the beginning, at a given time, the rising edge of the LOAD that removes Vector Restart. At this time the next CLOCK pulse will be CLOCK 1 and the count will restart at the beginning of the first odd line.

Preconditioning the part during normal operation, before the desired synchronizing pulse, is necesasry. However, since LOAD and CLOCK are asynchronous and independent, this is possible without interruption or data and performance corruption. If the defaulted 14.31818 MHz RS-170 values are being used, preconditioning and restarting can be minimized by using the CLEAR pulse instead of the Vectored Restart operation. The 'ACT715-R/LM1882-R is better suited for this application because it eliminates the need to program a 1 into Bit 10 of the Status Register to enable the CLOCK. Gen Locking to another count location other than the very beginning or separate horizontal/vertical resetting is not possible with the 'ACT715/LM1882 nor the 'ACT715-R/LM1882-R.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The LSB will be scanned out first. Since each register is 12 bits wide, completely scanning out data of the addressed register will require 12 CLOCK pulses. More than 12 CLOCK pulses on the same register will only cause the MSB to repeat on the output. Re-scanning the same register will require that register to be reloaded. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51–53. Note that before the part will scan out the data, the LOAD signal must be brought back HIGH.

Addressing Logic (Continued)

Normal device operation can be resumed by loading in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the RS170 Format (using a 14.31818 MHz clock signal) and how they compare against the actual EIA RS170 Specifications. The default signals that will be output are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected so that a pulse indicating the active lines would be output.

Reg	D Value	H	Register Description
REG0	0	000	Status Register (715/LM1882)
REG0	512	200	Status Register (715-R/LM1882-R)
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	038	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 μs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

RS170 Horizontal Data

Signal	Width	μs	%H	Specification (μs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER iod	910 Clocks	63.556	100	
RS170 Vertical Data				
VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERiod (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERiod (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±15 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±20 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
Ceramic	175°C
Plastic	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
54ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	ACT/LM1882		54ACT/LM1882	74ACT/LM1882	Units	Conditions
			T_A = +25°C, C_L = 50 pF		T_A = −55°C to +125°C, C_L = 50 pF	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4	V	
		4.5		3.86	3.7	3.76	V	*V_{IN} = V_{IL}/V_{IH}
		5.5		4.86	4.7	4.76	V	I_{OH} = −8 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1	V	
		4.5		0.36	0.5	0.44	V	*V_{IN} = V_{IL}/V_{IH}
		5.5		0.36	0.5	0.44	V	I_{OH} = +8 mA
I_{OLD}	Minimum Dynamic Output Current	5.5			32.0	32.0	mA	V_{OLD} = 1.65V
I_{OHD}	Minimum Dynamic Output Current	5.5			−32.0	−32.0	mA	V_{OHD} = 3.85V
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CC}	Supply Current Quiescent	5.5		8.0	160	80	μA	V_{IN} = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_{IN} = V_{CC} − 2.1V

*All outputs loaded; thresholds on input associated with input under test.

Note 1: Test Load 50 pF, 500Ω to Ground.

3

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF			54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT/LM1882 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190		130		150		MHz
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220		145		175		MHz
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5	3.5	19.5	3.5	18.5	ns
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0	3.5	22.0	3.5	20.5	ns
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0	3.0	20.0	3.0	19.5	ns

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	ACT/LM1882 $T_A = +25°C$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimums			
t_{sc}	Control Setup Time ADDR/DATA to LOAD−	5.0	3.0	4.0	4.5	4.5	ns
t_{sc}	L/HBYTE to LOAD−	5.0	3.0	4.0	4.5	4.5	ns
t_{sd}	Data Setup Time D7–D0 to LOAD+	5.0	2.0	4.0	4.5	4.5	ns
t_{hc}	Control Hold Time LOAD− to ADDR/DATA	5.0	0	1.0	1.0	1.0	ns
	LOAD− to L/HBYTE	5.0	0	1.0	1.0	1.0	ns
t_{hd}	Data Hold Time LOAD+ to D7–D0	5.0	1.0	2.0	2.0	2.0	ns
t_{rec}	LOAD+ to CLK (Note 1)	5.0	5.5	7.0	8.0	8.0	ns
t_{wld-}	Load Pulse Width LOW	5.0	3.0	5.5	5.5	5.5	ns
t_{wld+}	HIGH	5.0	3.0	5.0	7.5	7.5	ns
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5	9.5	9.5	ns
t_{wck}	CLOCK Pulse Width (HIGH or LOW)	5.0	2.5	3.0	4.0	3.5	ns

Note 1: Removal of Vectored Reset or Restart to Clock.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

AC Operating Requirements (Continued)

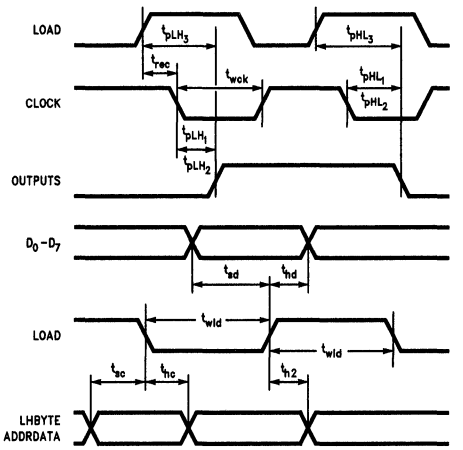

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FIGURE 4. AC Specifications

Additional Applications Information

POWERING UP

The 'ACT715/LM1882 default value for Bit 10 of the Status Register is 0. This means that when the CLEAR pulse is applied and the registers are initialized by loading the default values the CLOCK is disabled. Before operation can begin, Bit 10 must be changed to a 1 to enable CLOCK. If the default values are needed (no other programming is required) then *Figure 5* illustrates a hardwired solution to facilitate the enabling of the CLOCK after power-up. Should control signals be difficult to obtain, *Figure 6* illustrates a possible solution to automatically enable the CLOCK upon power-up. Use of the 'ACT715-R/LM1882-R eliminates the need for most of this circuitry. Modifications of the *Figure 6* circuit can be made to obtain the lone CLEAR pulse still needed upon power-up.

Note that, although during a Vectored Restart none of the preprogrammed registers are affected, some signals are affected for the duration of one frame only. These signals are the Horizontal and Vertical Drive signals. After a Vectored Restart the beginning of these signals will occur at the first CLK. The end of the signals will occur as programmed. At the completion of the first frame, the signals will resume to their programmed start and end time.

PREPROGRAMMING "ON-THE-FLY"

Although the 'ACT715/LM1882 and 'ACT715-R/LM1882-R are completely programmable, certain limitations must be set as to when and how the parts can be reprogrammed. Care must be taken when reprogramming any End Time registers to a new value that is lower than the current value. Should the reprogramming occur when the counters are at a count after the new value but before the old value, then the counters will continue to count up to 4096 before rolling over.

For this reason one of the following two precautions are recommended when reprogramming "on-the-fly". The first recommendation is to reprogram horizontal values during the horizontal blank interval only and/or vertical values during the vertical blank interval only. Since this would require delicate timing requirements the second recommendation may be more appropriate.

The second recommendation is to program a Vectored Restart as the final step of reprogramming. This will ensure that all registers are set to the newly programmed values and that all counters restart at the first CLK position. This will avoid overrunning the counter end times and will maintain the video integrity.

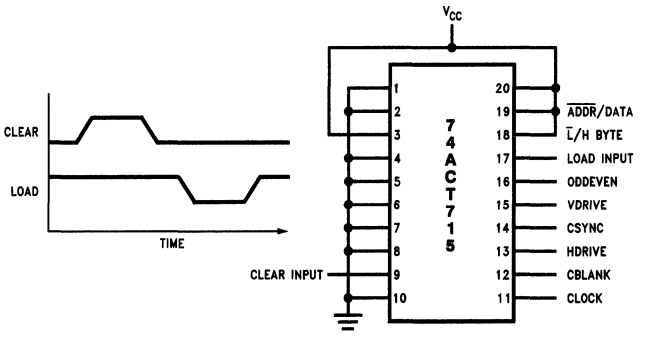

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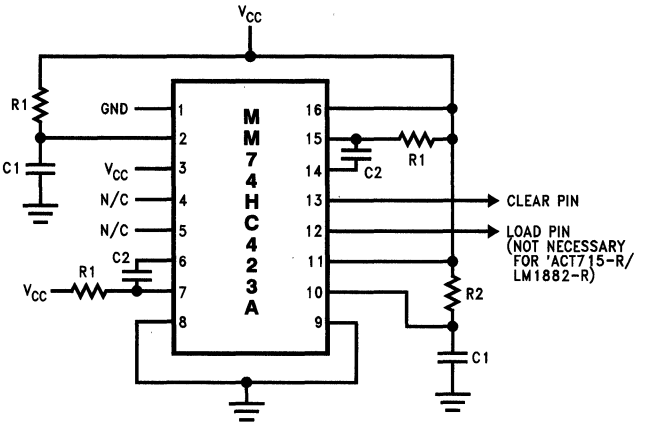
FIGURE 5. Default RS170 Hardwire Configuration

Additional Applications Information (Continued)



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Note: A 74HC221A may be substituted for the 74HC423A Pin 6 and Pin 14 must be hardwired to GND

Components

R1: 4.7k C1: 10 μF
R2: 10k C2: 50 pF

FIGURE 6. Circuit for Clear and Load Pulse Generation

National Semiconductor

LM2416/LM2416C Triple 50 MHz CRT Driver

General Description

The LM2416 contains three wide bandwidth, large signal amplifiers designed for large voltage swings. The amplifiers have a gain of 13. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to VGA, Super VGA and the IBM® 8514 graphics standard.

The part is housed in the industry standard 11-lead TO-220 molded power package. The heat sink is floating and may be grounded for ease of manufacturing and RFI shielding.

Features

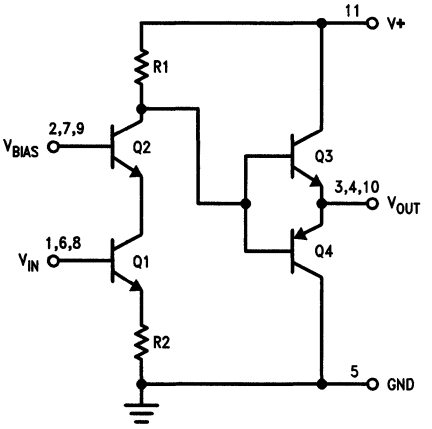
- 50 Vpp output at 45 MHz drives CRT directly
- Rise/fall time typically 10 ns with 8 pF load
- 65V output swing capability

Applications

- CRT driver for RGB monitors
- High voltage amplifiers

Schematic and Connection Diagram

(One Section)



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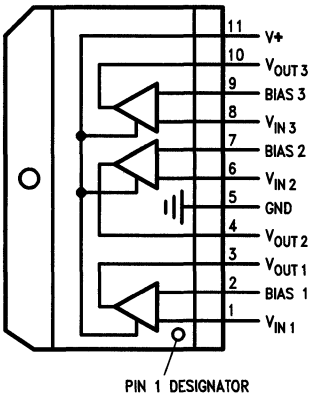


TL/K/10738–2

Top View

Order Number LM2416T or LM2416CT
See NS Package Number TA11B

Absolute Maximum Ratings

Supply Voltage, V^+	+85V
Power Dissipation, P_D	10W
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +90°C
Lead Temperature (Soldering, <10 sec.)	300°C
ESD Tolerance	4 kV

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Electrical Characteristics

V^+ = 80V, C_L = 8 pF, DC input bias, V_{IN} = 3.6 V_{DC}. 50 V_{PP} output swing, V_{BIAS} = +12V. See *Figure 1*. T_A = 25°C unless otherwise noted.

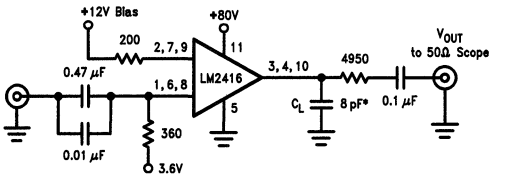
Symbol	Parameter	Conditions	LM2416			LM2416C			Units
			Min	Typical	Max	Min	Typ	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load	18	22	26	16	22	28	mA
V_{OUT}	Output Offset Voltage	V_{IN} = 3.6V	38	42	46	35	42	48	V_{DC}
t_r	Rise Time	10% to 90% (Note 3)		8	13		12	16	ns
t_f	Fall Time	10% to 90% (Note 3)		10	13		12	16	ns
BW	Bandwidth	−3 dB		42			35		MHz
A_V	Voltage Gain		−11	−13	−15	−10	−13	−16	V/V
OS	Overshoot	*Figure 1*		0			0		%
LE	Linearity Error	(Note 1)		8			10		%
ΔA_V	Gain Matching	(Note 2)		0.2			0.5		dB

Note 1: Linearity Error is defined as the variation in small signal gain from +20V to +70V output with a 100 mV AC, 1 MHz, input signal.

Note 2: Calculated value from Voltage Gain test on each channel.

Note 3: Guaranteed parameter, not tested.

Test Circuit



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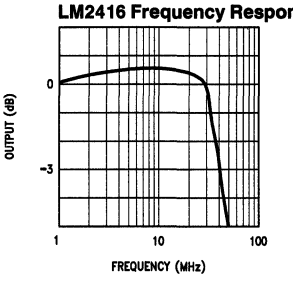
* 8 pF is total load capacitance. It includes all parasitic capacitance.

FIGURE 1. Test Circuit (One Section)

Figure 1 shows a typical test circuit for evaluation of the LM2416. This circuit is designed to allow testing of the LM2416 in a 50Ω environment such as a pulse generator, oscilloscope or network analyzer.

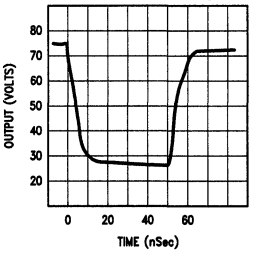
Typical Performance Characteristics

LM2416 Frequency Response



TL/K/10738–4

LM2416 Pulse Response

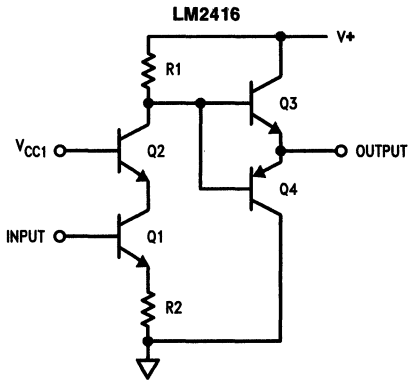


TL/K/10738–5

LM2416—Theory of Operation

The LM2416 is a high voltage triple CRT driver suitable for VGA, Super VGA, IBM 8514 and 1K by 768 non-interlaced display applications. The LM2416 features 80 volt operation and low power dissipation. The part is housed in the industry standard 11 lead TO-220 molded power package. The heat sink is floating and may be grounded for ease of manufacturing and RFI shielding.

The circuit diagram of the LM2416 is shown in *Figure 2*. Q1 and R2 provides a conversion of input voltage to current, while Q2 acts as a common base or cascode amplifier stage to drive the load resistor R1. Emitter followers Q3 and Q4 isolate the impedance of R1 from the capacitance of the CRT cathode, and make the circuit relatively insensitive to load capacitance. The gain of this circuit is −R1/R2 and is fixed at −13. The bandwidth of the circuit is set by the collector time constant formed by the load resistor R1 and associated capacitance of Q2, Q3, Q4, and stray layout capacitance. Proprietary transistor design allows for high bandwidth with low operating power.



TL/K/10738–6

FIGURE 2. LM2416 CRT Driver (One Section)

Thermal Considerations

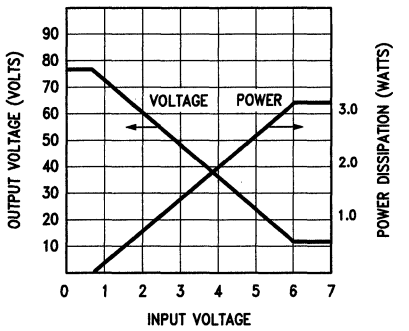
The transfer characteristics of the amplifier are shown in *Figure 3*. Power supply current increases as the input signal increases and consequently power dissipation also increases.

The LM2416 cannot be used without heat sinking. *Figure 3* shows the power dissipated in each channel over the operating voltage range of the device. Typical "average" power dissipation with the device output voltage at one half the supply voltage is 1.8W per channel for a total dissipation of 5.4W package dissipation. Under white screen conditions, i.e.: 15V output, dissipation increases to 3W per channel or 9W total. The LM2416 case temperature must be maintained below 90°C. If the maximum expected ambient temperature is 50°C, then a heat sink is needed with thermal resistance equal to or less than:

$$R_{th} = \frac{(90 - 50°C)}{9W} = 4.4°C/W$$

The Thermalloy #6400 is one example of a heatsink that meets this requirement.

WARNING: THE LM2416 IS NOT PROTECTED AGAINST OUTPUT SHORT CIRCUITS. The minimum resistance the LM2416 can drive is 600Ω to ground or V+.



TL/K/10738–7

FIGURE 3. LM2416 DC Characteristics

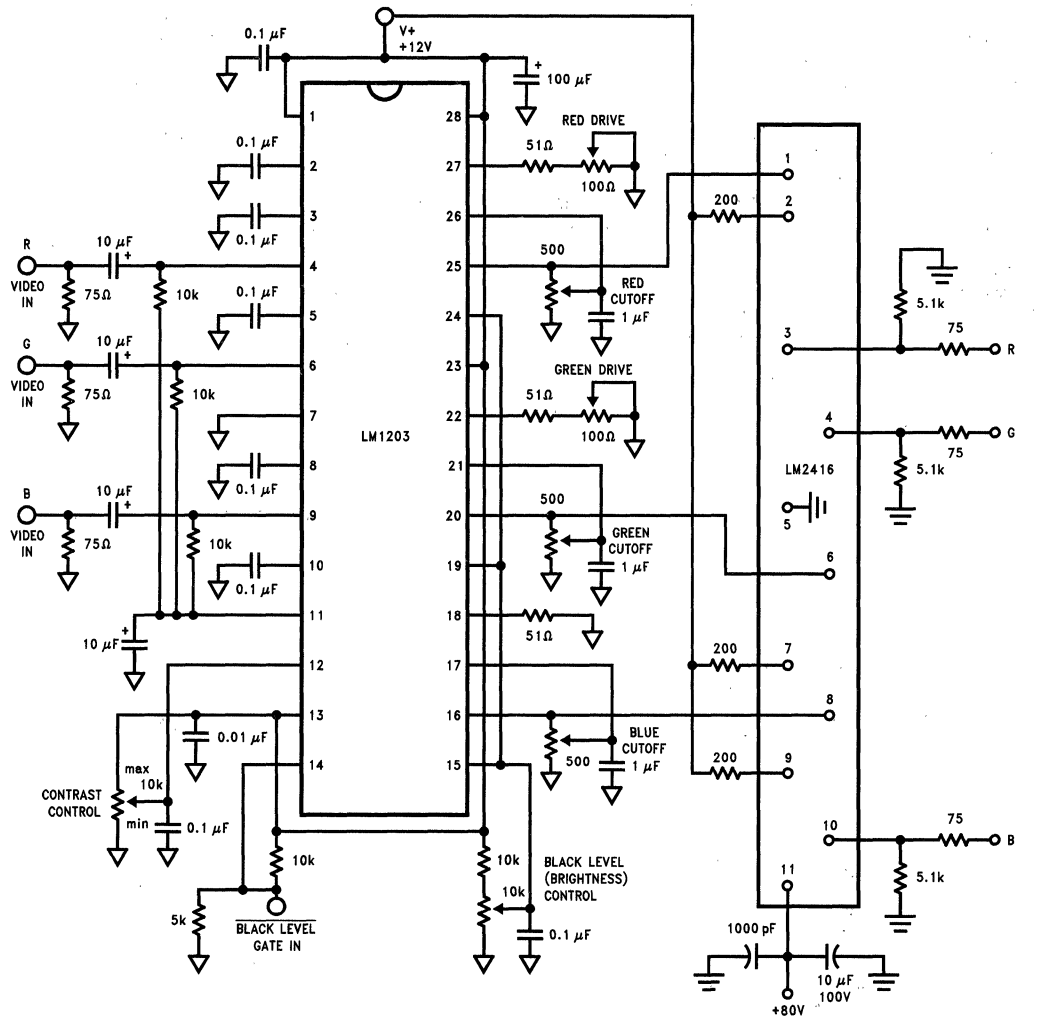


FIGURE 4. Typical Application LM1203-LM2416 Application

A typical application of the LM2416 is shown in *Figure 4*. Used in conjunction with a LM1203, a complete video channel from monitor input to CRT cathode is shown. Performance is satisfactory for all applications to 1k by 768 non-interlaced. Typical rise-fall times are 12 ns, with better than 50V p-p drive signals available to an 8 pF load. In this application, feedback is local to the LM1203. An alternative scheme would be feedback from the output of the LM2416 to the positive clamp inputs of the LM1203. This would provide slightly better black level control of the system.

National Semiconductor

LM2418 Triple 30 MHz CRT Driver

General Description

The LM2418 contains three large signal voltage amplifiers designed to directly drive CRT cathodes for VGA Color Graphics Displays. Output swings greater than 50 V_{PP} are achieved with a 90V power supply. The nominal voltage gain of each amplifier is 18 with gain matching of 1.0 dB between amplifiers.

Packaging is the industry standard molded 11 lead TO-220. The heatsink tab is isolated and may be grounded to improve RFI shielding and simplify assembly.

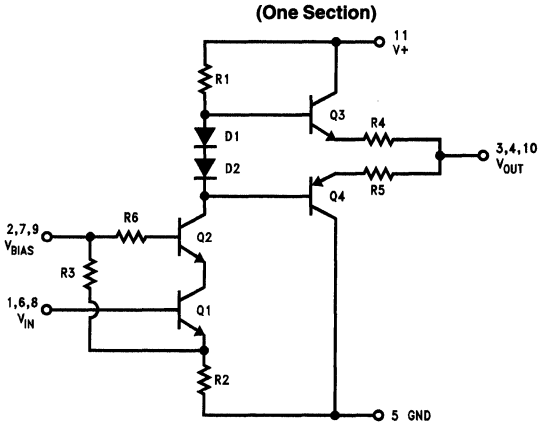
Features

- 50 Vpp output at 30 MHz drives CRT directly
- Rise/fall time typically 12 ns with 8 pF load
- 65V output swing capability
- Optimized output stage for low crossover distortion
- Gain matching of 1 dB
- Voltage gain of −19
- Includes oscillation supression resistors

Applications

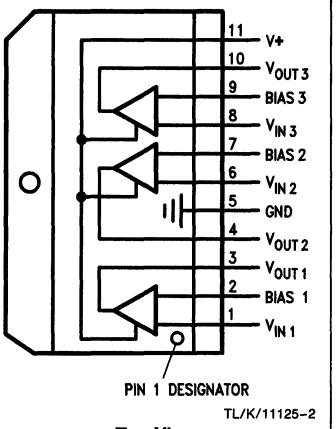
- CRT driver for RGB monitors
- High voltage amplifiers

Schematic and Connection Diagram



TL/K/11125–1

FIGURE 1



TL/K/11125–2

Top View

Order Number LM2418T
See NS Package Number TA11B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+	+95V
Storage Temperature Range, T_{STG}	−25°C to +100°C
Operating Temperature Range, T_{CASE}	−20°C to +100°C
Lead Temperature (Soldering, <10 sec.)	300°C
ESD Tolerance	tbd

Electrical Characteristics

$V^+ = 90V$, $C_L = 8$ pF, DC input bias, $V_{IN} = 3.6\ V_{DC}$. 50 V_{PP} output swing, $V_{BIAS} = +12V$. $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	LM2418			Units
			Min	Typ	Max	
I_{CC}	Supply Current (per Amplifier)	No Input or Output Load		18	26	mA
V_{OUT}	Output Offset Voltage	$V_{IN} = 3.6V$	46	53	60	V_{DC}
t_r	Rise Time	10% to 90% (Note 3)		12	20	ns
t_f	Fall Time	10% to 90% (Note 3)		12	20	ns
BW	Bandwidth	−3 dB		30		MHz
A_V	Voltage Gain		−17	−19	−23	V/V
OS	Overshoot			5		%
LE	Linearity Error	(Note 1)		8		%
ΔA_V	Gain Matching	(Note 2)		1.0		dB

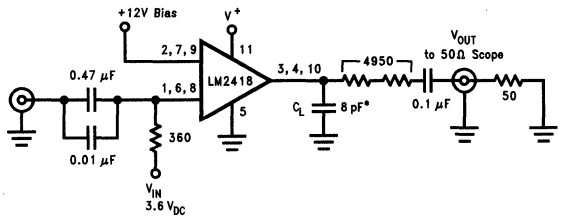
Note 1: Linearity Error is defined as the variation in small signal gain from +20V to +70V output with a 100 mV AC, 1 MHz, input signal.

Note 2: Calculated value from Voltage Gain test on each channel.

Note 3: Guaranteed parameter, not tested.

AC Test Circuit

Figure 2 shows a typical test circuit for evaluation of the LM2418. This circuit is designed to allow testing of the LM2418 in a 50Ω environment such as a pulse generator, oscilloscope or network analyzer.



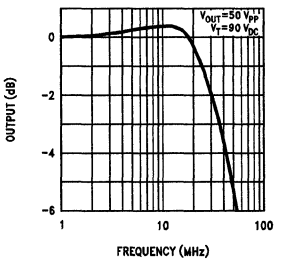
TL/K/11125–3

*8 pF is total load capacitance. It includes all parasitic capacitance.

FIGURE 2. Test Circuit (One Section)

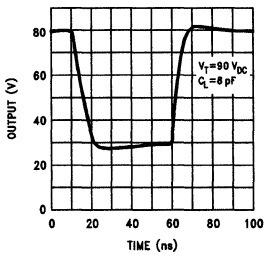
Typical Performance Characteristics

LM2418 Frequency Response



TL/K/11125–4

LM2418 Pulse Response



TL/K/11125–5

FIGURE 3

LM2418—Theory of Operation

The LM2418 is a high voltage triple CRT driver suitable for VGA display applications. The LM2418 features 90V operation and low power dissipation. The part is housed in the industry standard 11-lead TO-220 molded power package. The heat sink is electrically isolated from the circuitry and may be grounded for ease of manufacturing and RFI shielding.

The circuit diagram of the LM2418 is shown in *Figure 1*. Q1 and R2 provide a conversion of input voltage to current, while Q2 acts as a common base or cascode amplifier stage to drive the load resistor R1. Emitter followers Q3 and Q4 isolate the impedance of R1 from the capacitance of the CRT cathode, and make the circuit relatively insensitive to load capacitance. The gain of this circuit is $-R1/R2$ and is fixed at -19. The bandwidth of the circuit is set by the collector time constant formed by the load resistor R1 and associated capacitance of Q2, Q3, Q4, and stray layout capacitance. Diodes D1 and D2 provide forward bias to the output stage to reduce crossover distortion at low signal levels, while R3 provides a DC bias offset to match the output level characteristics of the LM1203 RGB Video Amplifier System. Proprietary transistor design allows for high bandwidth with low operating power.

Figure 2 shows a typical test circuit for evaluation of the LM2418. This circuit is designed to allow testing of the LM2418 in a 50Ω environment such as a pulse generator and a scope, or a network analyzer. In this test circuit, two resistors in series totaling 4.95 kΩ form a wideband low capacitance probe to match the output of the LM2418 to a 50Ω cable and load. Typical AC performance of the circuit is shown in *Figure 3*. The input signal is AC coupled to the base of Q1, while a DC bias of 12V is applied to the base of Q2 (See *Figure 2*).

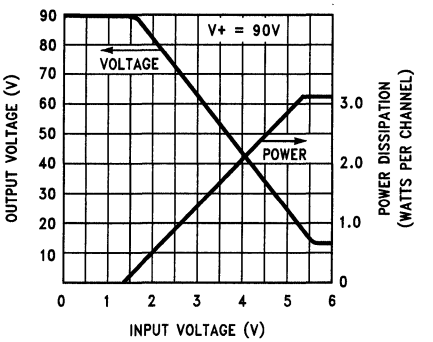
Thermal Considerations

The transfer characteristics of the amplifier are shown in *Figures 4* and *5*. Power supply current increases as the input signal increases and consequently power dissipation also increases.

The LM2418 cannot be used without heat sinking. *Figure 5* shows the power dissipated in each channel over the operating voltage range of the device. Typical "average" power dissipation with the device output voltage at one half the supply voltage is 1.8W per channel for a total dissipation of 5.4W package dissipation. Under white screen conditions, i.e., 20V output, dissipation increases to 3.0W per channel or 9W total. The LM2418 case temperature must be maintained below 100°C. If the maximum expected ambient temperature is 60°C, then a maximum heat sink thermal resistance can be calculated:

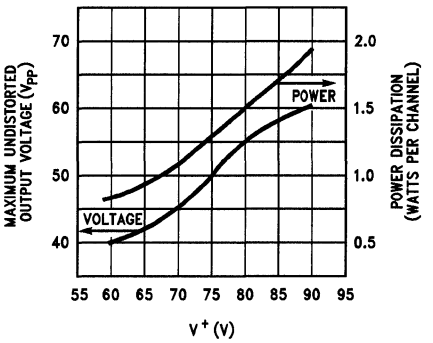
$$R_{th} = \frac{(100°C - 60°C)}{9W} = 4.4°C/W$$

PRECAUTION: THE LM2418 IS NOT PROTECTED AGAINST OUTPUT SHORT CIRCUITS. The minimum resistance the LM2418 can drive is 800Ω to ground or V^+.



TL/K/11125–7

FIGURE 4. LM2418 DC Characteristics

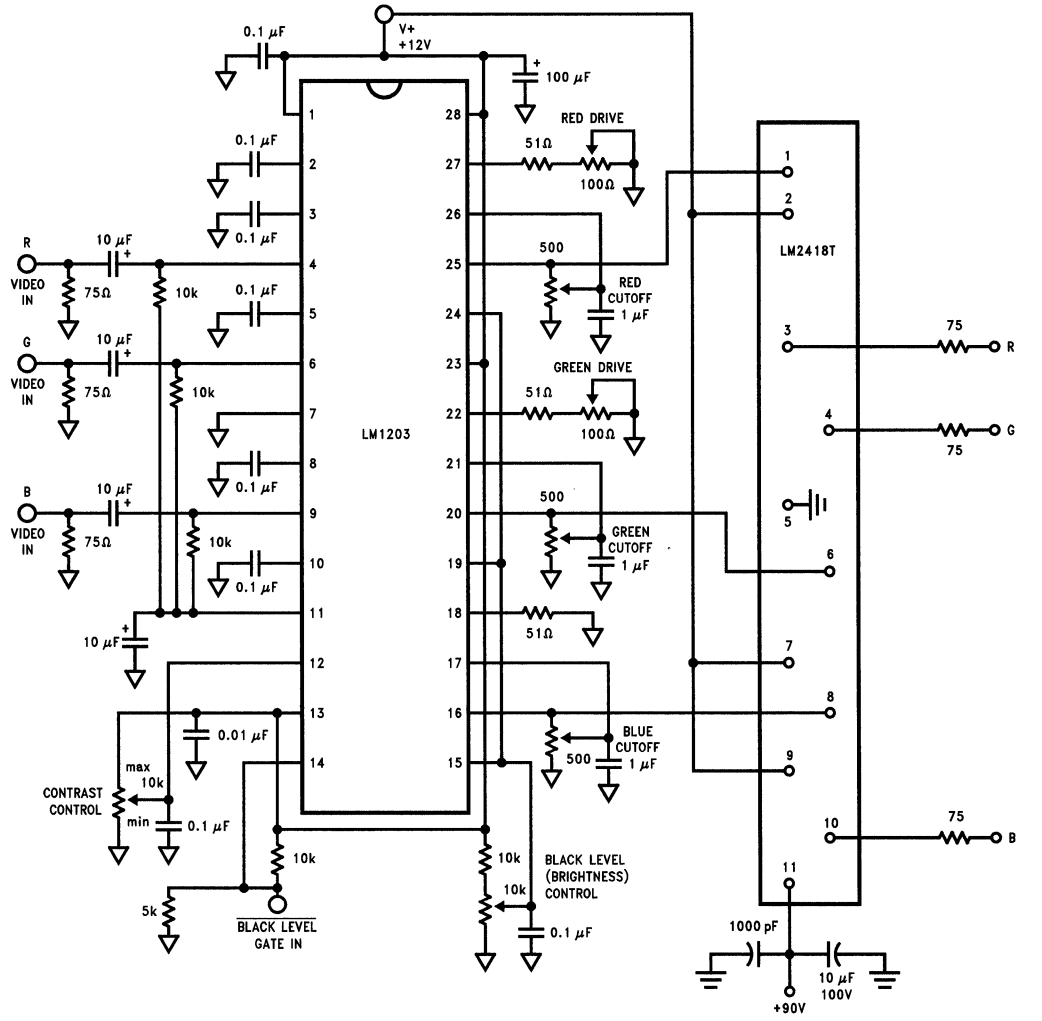


TL/K/11125–9

FIGURE 5. LM2418 Output Swing and Power Characteristics

Typical Application

A typical application of the LM2418 is shown in *Figure 6.* Used in conjunction with an LM1203, a complete video channel from monitor input to CRT cathode is shown. Performance is satisfactory for all applications up to 640 by 480 lines. Typical rise/fall times of this circuit are 15 ns, with better than 50 V_{PP} drive signals available to a 10 pF load. In this application, feedback is local to the LM1203, an alternative scheme would feed back from the output of the LM2418 to the positive clamp inputs of the LM1203. This would provide better black level control of the system.



TL/K/11125–10

FIGURE 6. Typical Application LM1203-LM2418 Application

National Semiconductor

PRELIMINARY

LM2419
Triple 65 MHz CRT Driver

General Description

The LM2419 contains three wide bandwidth, large signal amplifiers designed for large voltage swings. The amplifiers have a gain of −15. The device is intended for use in color CRT monitors and is a low cost solution to designs conforming to 1024 x 768 display resolution.

The device is mounted in the industry standard 11-lead TO-220 molded power package. The heat sink is electrically isolated and may be grounded for ease of manufacturing and EMI/RFI shielding.

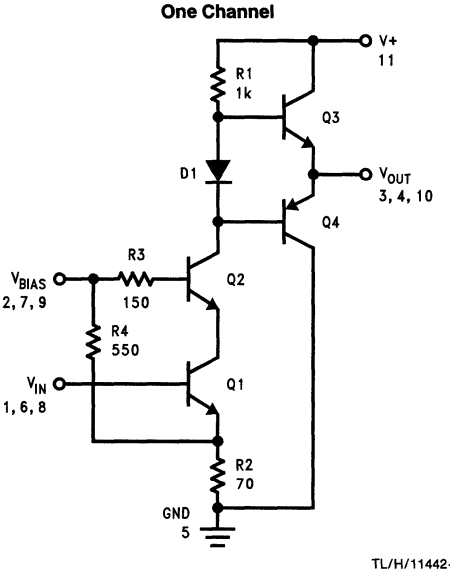
Features

- 50 V_{PP} output swing at 65 MHz
- Rise/Fall time < 7 ns with 12 pF load
- 60 V_{PP} output swing capability
- Pin and function compatible with LM2416
- No low frequency tilt

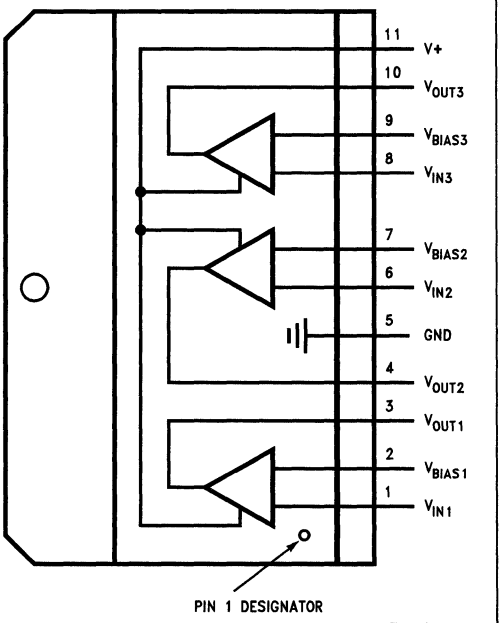
Applications

- CRT driver for SVGA, IBM 8514 and 1024 x 768 display resolution RGB monitors

Schematic and Connection Diagrams



TL/H/11442–1



TL/H/11442–2

Order Number LM2419T
See NS Package Number TA11B

Section 4

Display Drivers

Section 4 Contents

National Semiconductor

Display Drivers

MOS/LSI DISPLAY DRIVERS

National's comprehensive family of display drivers provides direct interface to all of the common display technologies—light-emitting diode (LED), liquid crystal display (LCD), and vacuum fluorescent (VF).

FUNCTION SIMILAR FAMILY

Each driver utilizes a simple serial-data input channel, on-chip shift register, latches and buffer/driver outputs. The serial input channel allows direct interface to most microprocessors, including COPS™, NSC800™, 8080 series, and TMS1000 series. Besides a serial-data input, each driver requires a clock input. Some offer a latch (data) input and/or data output for easy cascade interconnect of additional drivers.

Once loaded, the shift register data can be transferred to the on-chip latches, which then output to the buffer/driver and respective display. This buffer/driver is where each provides the unique driver interface desired by the particular display technology—LED, LCD, or VF.

THE MM58241 SERIES—VF

Each of the products in the MM58241 series provides high-voltage (several up to 60V) drive of VF displays. All are ideal for direct or multiplexed interface to large complex VF panel arrays or 5 × 7 (or larger) dot-matrix character strings. Each of the drivers are cascadable for further expansion. Application note AN-371 provides further details and other application information.

THE MM5450 SERIES—LED

National's MM5450 series of LED display drivers rounds out this comprehensive product family. This popular series offers direct drive of LED displays by providing up to 25 mA of current drive per LED segment.

CMOS/LSI

Many of the products in the display driver family utilize CMOS technology and are further evidence of National's capabilities and commitment to CMOS/LSI—the technology of the '80s.

In addition, National offers a line of bipolar segment and digit drivers with a broad range of output sink and source currents.

Detailed features/functions of the 16-member display driver family are high-lighted in the following product guide.

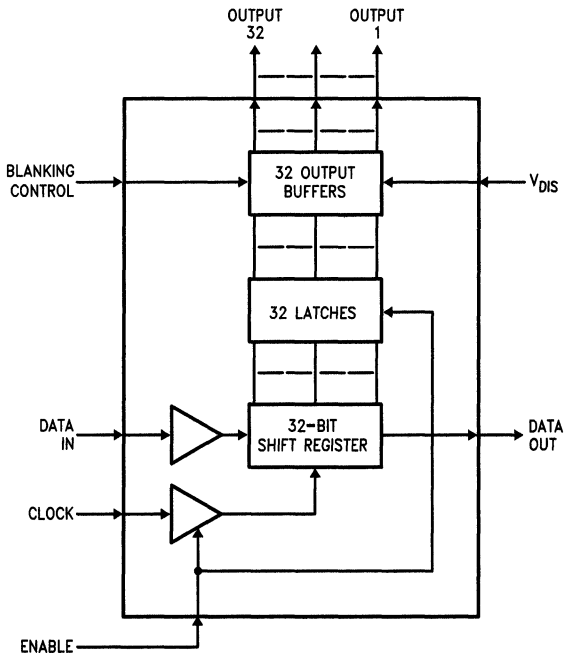


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FIGURE 1. Typical Block Diagram

National Semiconductor

LSI Display Driver Selection Guide

Display Technology	Product Number	Features
Vacuum Fluorescent (VF)	MM58241	32-segment, direct/multiplexed drive to 60V, data enable, brightness control, cascadable, 40-pin DIP or 44-pin PCC package.
VF	MM58242	20-digit, direct/multiplexed drive to 60V, data enable, brightness control, cascadable, 28-pin DIP or PCC package.
VF	MM58248	35-segment, direct/multiplexed drive to 60V, pin-compatible to MM5448, 40-pin DIP or 44-pin PCC package.
VF	MM58341	32-segment, direct/multiplexed drive to 35V, data enable, brightness control, cascadable, 40-pin DIP or 44-pin PCC package.
VF	MM58342	20-digit, direct/multiplexed drive to 35V, data enable, brightness control, cascadable, 28-pin DIP or PCC package.
VF	MM58348	35-segment, direct/multiplexed drive to 35V, pin-compatible to MM5448, 40-pin DIP or 44-pin PCC package.
Liquid Crystal (LCD)	MM5452	32-segment, direct drive, serial-data input, data enable, on-chip backplane (B/P) oscillator, 40-pin DIP or 44-pin PCC package.
LCD	MM5453	33-segment, direct drive, serial-data input, B/P oscillator, 40-pin DIP or 44-pin PCC package.
LCD	MM5483	31-segment, direct drive, serial-data input/output, latch (data) control, 40-pin DIP or 44-pin PCC package.
LCD	MM58201	Multiplexed drive, 192 segments (8 backplanes, 24 segments), 192-bit RAM, cascadable, R/C oscillator, serial-data input/output, 40-pin DIP or 44-pin PCC package.
Light-Emitting Diode (LED)	MM5450	34-segment, direct drive up to 25 mA, brightness control, data enable, 40-pin DIP or 44-pin PCC package.
LED	MM5451	35-segment, direct drive up to 25 mA, brightness control, 40-pin DIP or 44-pin PCC package.
LED	MM5480	23-segment, direct drive up to 25 mA, serial-data input, brightness control, 28-pin DIP package.
LED	MM5481	14-segment, direct drive up to 25 mA, serial-data input, brightness control, 20-pin DIP package.
LED	MM5484	16-segment, direct drive up to 10 mA, serial-data input/output, cascadable, 22-pin DIP package.
LED	MM5486	33-segment, direct drive up to 25 mA, serial-data input/output, brightness control, latch (data) control, 40-pin DIP package.

National Semiconductor

Bipolar Display Driver Selection Guide

Device Number and Temperature Range		Drivers/ Package	I_O/Digit (mA)		V_{MAX} (V)		Comments
0°C to +70°C	−55°C to +125°C		Sink (Common Anode)	Source (Common Cathode)	Input	Supply	
DS75491		4		50	10	10	
DS75494	DS55494	6	150		10	10	Enable Control
DS75492		6	250		10	10	
LM3909		1	45	45	2.1	6.4	LED Flasher/ Oscillator
LM3914		10	0	30*	35	25	Dot/Bar Driver Linear Scale
LM3915		10	0	30*	35	25	Dot/Bar Driver Log Scale
LM3916		10	0	30*	35	25	Dot/Bar Driver VU Meter Scale

*Per segment, use common external supply for anodes

National Semiconductor

DS8187 Vacuum Fluorescent Display Driver

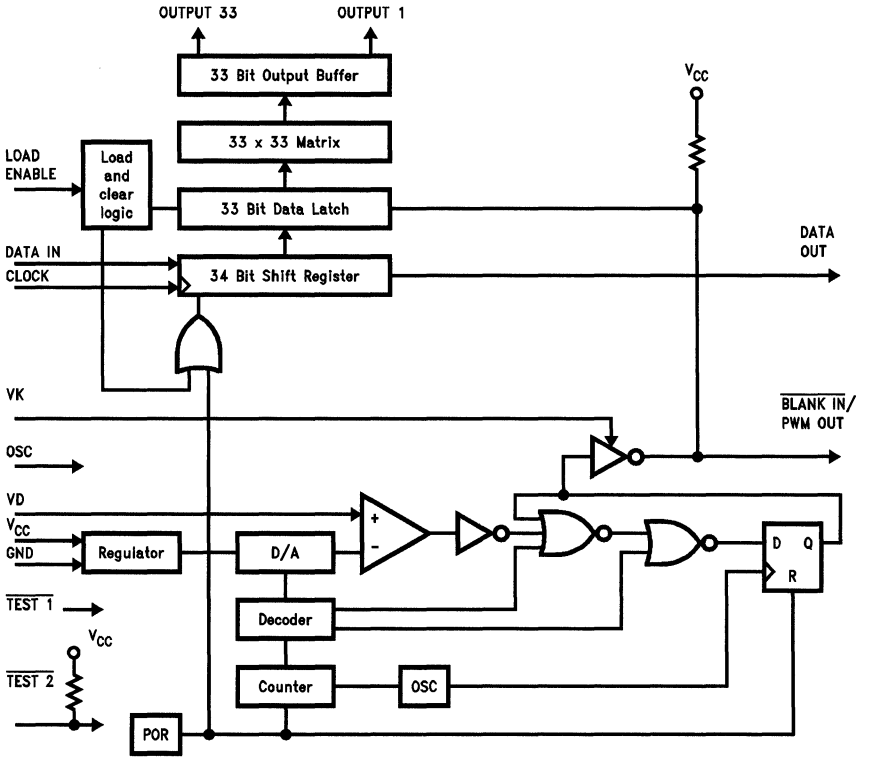
General Description

The DS8187 is a vacuum fluorescent display tube driver. This device is implemented in CMOS technology, to provide high voltage output drivers and low power. Dimming may be accomplished by either analog or digital input. Autoload capability is accomplished by connecting the DATA OUT pin to the LOAD ENABLE input pin, with the addition of a start bit to the input data stream.

Features

- 33 Segment Direct Drive 25 − 0.8 mA and 8 − 2 mA output drivers
- 49 steps of dimming, mask programmable
- Analog or digital input dimming control
- DATA OUT pin for cascading
- Mask options allow reconfiguring of outputs with respect to shift register bit position
- Autoload or external load capability

Block Diagram



TL/F/11220–4

FIGURE 1.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Volltage (V_{CC})	−0.3 to +20V
DC Input Voltage (V_{IN})	−0.3 to VCC+0.3V
DC Output Voltage (V_{OUT})	
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Power Dissipation (PD) at 25°C	
DIP Board Mount	TBD
DIP Socket Mount	TBD
Typical Values	
θJA DIP Board Mount	TBD °C/W
θJA DIP Socket Mount	TBD °C/W

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	8	18	V
DC Input or Output Voltage	0	V_{CC}	V
Temperature Range	−40	+85	°C
Electro-Static Discharge (ESD)		2K	V

DC Electrical Characteristics

V_{CC} = 8V to 18V, All voltages referenced to GND, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		3.8	6	V
V_{IL}	Low Level Input Voltage		0	0.8	V
I_{IH1}	High Level Input Current (Clock, Data In, Load, VK)	V_{IH1} = 5.0V	−5	5	μA
I_{IH2}	High Level Input Current (Blank)	V_{IH2} = 5.0V, T = 25°C	−20	10	μA
I_{IH3}	High Level Input Current ($\overline{TEST2}$)	V_{IH3} = %.0V, T = 25°C	−100	20	μA
I_{IL1}	Low Level Input Current (Clock, Data In, Load, VK)	V_{IL1} = 0V	−5	5	μA
I_{IL2}	Low Level Input Current ($\overline{BLANK\ IN}$)	V_{IL2} = 0V, T = 25°C	−125	−5	μA
I_{IL3}	Low Level Input Current ($\overline{TEST2}$)	V_{IL3} = 0V, T = 25°C	−700	−100	μA
I_{LI}	Input Leak Current (VD)	V_{IN} 0V to 6V	−5	5	μA
V_{OH1}	High Level Output Voltage (Low Current Driver)	V_{CC} = 9.5V, I_{OH1} = −0.8 mA	V_{CC}−0.8		V
V_{OH2}	High Level Output Voltage (High Current Drive)	V_{CC} = 9.5V, I_{OH2} = −2 mA	V_{CC}−0.8		V
V_{OH3}	High Level Output Voltage (DATA OUT, PWM OUT)	V_{CC} = 9.5V, I_{OH3} = −200 μA I_{OH3} = −20 μA	4 4.5	6 6	V V
V_{OL1}	Low Level Output Voltage (All Drivers)	V_{CC} = 9.5V, I_{OL1} = 500 μA I_{OL1} = 200 μA I_{OL1} = 2 μA		2 1 0.3	V V V
V_{OL2}	Low Level Output Voltage (DATA OUT,PWM OUT)	V_{CC} = 9.5V, I_{OL2} = 200 μA		0.8	V
I_{CC}	Supply Current	No Load		20	mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
f_C	Clock Frequency			250	kHz
PW_C	Clock Pulse Width		1.3		μs
t_S	Data Set-Up Time		1		μs
t_H	Data Hold Time		200		ns
PW_L	Load Pulse Width		1.3		μs
to_{DB}	Output Delay from Blank	C_L = 100 pF		7	μs
to_{DL}	Output Delay from Load	C_L = 100 pF		8	μs
t_r	Rise Time (All Driver Outputs)	C_L = 100 pF, t = 20% to 80% of V_{CC}		5	μs
t_f	Fall Time (All Driver Outputs)	CL = 100 pF, t = 80% to 20% of V_{CC}		5	μs

Dimming Characteristics

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
V_D Offset Voltage (Note 2)	$\pm V_D$ (3% + 6%)			±10	mV

AC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Pulse Width Error	No Load (Note 3)			±100	ns
PWM OUT Frequency		150	250	400	Hz
OSC Frequency		307.2	512	819.2	kHz

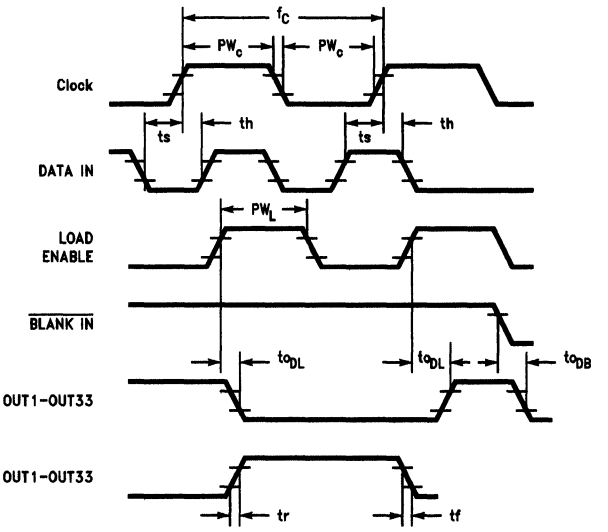
Note 2: Reference voltage is 6.1V typical.

Note 3: Under the ideal condition of DC parameters.

AC Test Conditions

Input Pulse Levels	0.5V to 3.5V
Input Rise and Fall Times	6 ns (10% to 90%)
Propagation Delays Measured at 20% and 80% points of respective waveforms	

Timing Waveforms



TL/F/11220–3

FIGURE 2.

Functional Description

SHIFT REGISTER OPERATION

Refer to block diagram *Figure 1* while LOAD ENABLE is low, data is entered into the shift register on the rising edge of the clock. The first data bit entered is stored in position #0, the last data bit entered is stored in position #33. A high voltage level applied to the LOAD ENABLE input transfers the data from the shift register to the data latch. The data is presented to the output drivers through a 33 x 33 matrix. This matrix determines shift register output designation. The DS8187 has 34 shift register positions, 33 data latches, and 33 output drivers.

AUTO LOAD MODE

In this mode, the DATA OUT pin is connected to the LOAD ENABLE pin. The data word consists of 34 bits including a leading start bit(logic 1). On the positive-going-edge of the 34th clock (LOAD ENABLE goes High), data is transferred to the data latches and the shift register is cleared.

DIRECT LOAD MODE

In this mode the DATA OUT pin is not connected to the LOAD ENABLE pin. The LOAD ENABLE pin is controlled directly by the user. When LOAD ENABLE goes High, the contents of the shift register are latched, presented to the output drivers through the 33 x 33 PLA matrix, and the shift register is cleared.

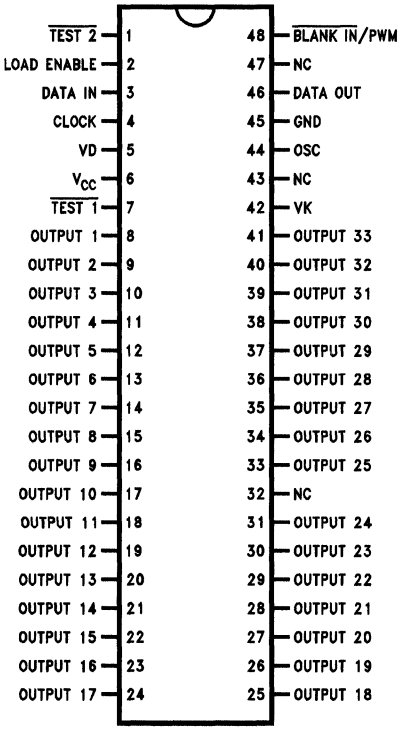
DIMMING FUNCTION

When VK is Low, the $\overline{\text{BLANK IN}}$/PWM OUT pin functions as an input blanking signal. When $\overline{\text{BLANK IN}}$/PWM is High, the output duty cycle is 100%. The duty cycle of a user supplied signal to this pin will determine the brightness of the output.

When VK is High, the duty cycle of the output drivers is controlled by an analog voltage applied to the VD pin. Table I indicates the duty cycle of the output drivers with respect to the analog voltage applied to VD pin.

Connection Diagram

Dual-In-Line Package



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Top View
Order Number DS8187N
See NS Package Number N48A

Analog Dimming and V_D Offset Description

When using analog dimming, the brightness attainable is 10.2% of maximum brightness. The voltage (V_{REF}) is the external voltage from which V_D is developed (usually from a variable resistor). This voltage should be in the range of 5.7V to V_{CC} so that the maximum 10.2% PWM duty cycle is achieved easily.

The V_D offset error represents the difference between the actual analog input voltage when using analog dimming and the internal analog voltage created by the D/A converter. Table III indicates the PWM duty cycle with respect to voltage at the V_D pin over 49 steps of dimming. To determine the Min/Max PWM, V_D offset must be subtracted from/added to the threshold voltage of Table III. The Dimming Curves *(Figure 6)* are a graphical representation of Table III showing the V_D offset.

Load Enable Description

The positive going edge of the Load Enable input signal latches data from the shifter and resets the shifter. While Load Enable is "high", the shifter will not accept data. The Load Enable should be driven high during the low level of the clock.

Output Circuit Description

The segment output drivers are push-pull active high. There are 25 low current drivers (0.8 mA) and 8 high current drivers (2 mA). These outputs nominally swing from 0.3V to (V_{CC} − 0.8V) and are designed to drive the anodes of low voltage (about 13V) vacuum fluorescent displays. The digital outputs (DATA OUT and PWM OUT) typically swing form 0.5V to 5V and are designed to drive other logic devices. For example, referring to *(Figure 3)*, if DS8187 devices are cascaded, then DATA OUT and PWM OUT of the first are connected respectively to DATA IN and $\overline{\text{BLANK IN}}$ of the second.

Figures 3, 4 and *5* are typical applications of the DS8187.

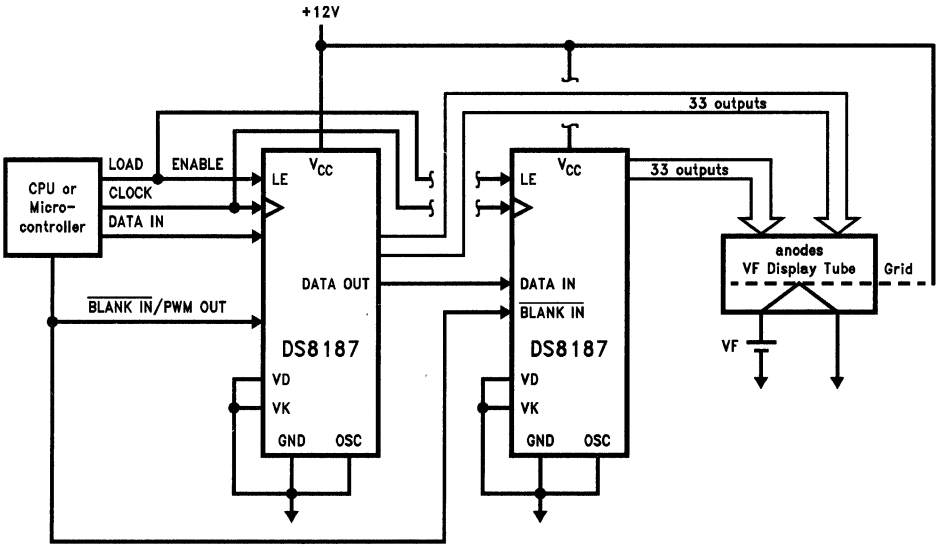

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FIGURE 3. Cascading Two Drivers with Digital Dimming

Pin Description

Pin No.	Pin Name	I/O	Description
1	$\overline{\text{TEST2}}$	I	This pin is used to select TEST MODE. (Factory Test)
2	LOAD ENABLE	I	While Low, data is enabled into the shift register. When this pin goes High, the contents of the shift register are loaded into the latch circuit and the shift register is reset to 0.
3	DATA IN	I	This pin inputs data to the shift register. When data is High, the output is ON. When data is Low, the output is OFF.
4	CLOCK	I	This pin is the clock for the shift register. Data is input to the shift register on the positive-going-edge of the clock.
5	VD	I	This analog voltage input pin specifies the output duty cycle per Table I.
6	V_{CC}		This is the power supply pin.
7	$\overline{\text{TEST1}}$		This pin is used to select TEST MODE. (Factory Test)
8–14	OUTPUT 1 to OUTPUT 7	O	These are low current output pins.
15–22	OUTPUT 8 to OUTPUT 15	O	These are high current output pins.
23–31	OUTPUT 16 to OUTPUT 24	O	These are low current output pins.
32	No Connect (NC)		Free pin, no connection to the chip.
33–41	OUTPUT 25 to OUTPUT 33	O	These are low current output pins.
42	VK	I	VK input terminal. This pin selects between analog dimming and digital dimming (duty cycle). When a Logic 0 is applied to VK, the $\overline{\text{BLANK IN}}$/PWM OUT pin functions as an input blanking signal. When a Logic 1 is applied to VK, the dimming is controlled by an analog voltage applied to the VD pin.
43	No Connect (NC)		Free pin, no connection to the chip.
44	OSC	I	This pin generates an oscillation of 500 kHz with an external capacitor of 47 pF connected between the OSC pin and GND.
45	GND		This is the GND pin.
46	DATA OUT	I/O	This pin outputs the data from the 34-bit shift register. Connecting the pin to the DATA IN pin on the next stage provides a cascade connection. Connecting the pin to the LOAD ENABLE pin causes the contents of the shift register to be latched on the leading edge of the signal at the DATA OUT pin. (Auto load function). In the Test Mode, this pin functions as an input.
47	No Connect (NC)		Free pin, no connection to the chip.
48	$\overline{\text{BLANK IN}}$/PWM OUT	I/O	When the internal dimming function is not used (VK = Low), this pin receives an external blank signal and controls the output duty cycle. This pin functions as an output when the internal dimming function is used (VK = High), and in Test Mode.

Typical Application

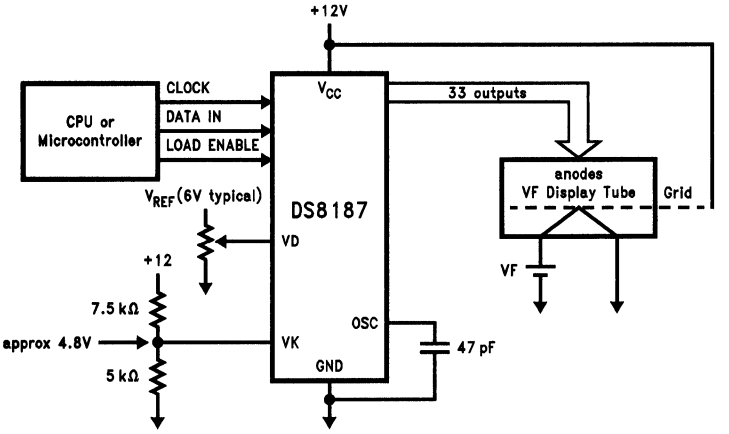

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FIGURE 4. Analog Dimming Control Using the V_D Pin

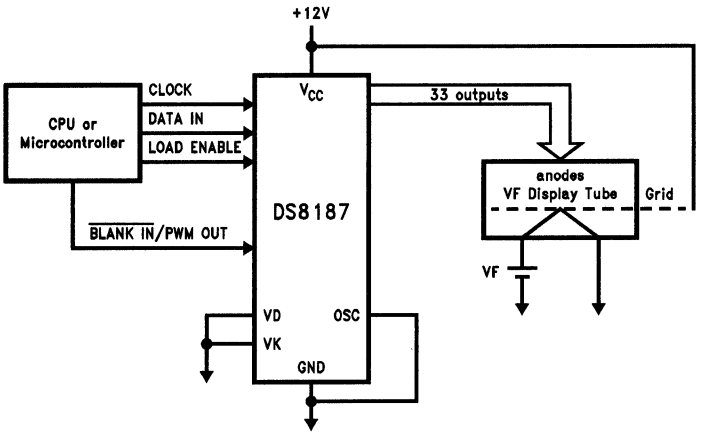

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FIGURE 5. Digital Dimming Using the $\overline{\text{BLANK IN}}$/PWM OUT Pin

TABLE I. Output Pin to Shift Register Conversion for Pattern "AA"

Pin Name	Shift Register	Pin Name	Shift Register	Pin Name	Shift Register
OUTPUT 1	BIT 14	OUTPUT 12	BIT 2	OUTPUT 23	BIT 12
OUTPUT 2	BIT 15	OUTPUT 13	BIT 10	OUTPUT 24	BIT 19
OUTPUT 3	BIT 1	OUTPUT 14	BIT 26	OUTPUT 25	BIT 24
OUTPUT 4	BIT 33	OUTPUT 15	BIT 29	OUTPUT 26	BIT 25
OUTPUT 5	BIT 5	OUTPUT 16	BIT 8	OUTPUT 27	BIT 20
OUTPUT 6	BIT 6	OUTPUT 17	BIT 3	OUTPUT 28	BIT 32
OUTPUT 7	BIT 7	OUTPUT 18	BIT 9	OUTPUT 29	BIT 21
OUTPUT 8	BIT 28	OUTPUT 19	BIT 4	OUTPUT 30	BIT 22
OUTPUT 9	BIT 27	OUTPUT 20	BIT 11	OUTPUT 31	BIT 23
OUTPUT 10	BIT 31	OUTPUT 21	BIT 16	OUTPUT 32	BIT 30
OUTPUT 11	BIT 18	OUTPUT 22	BIT 17	OUTPUT 33	BIT 13

PLA Code Chart

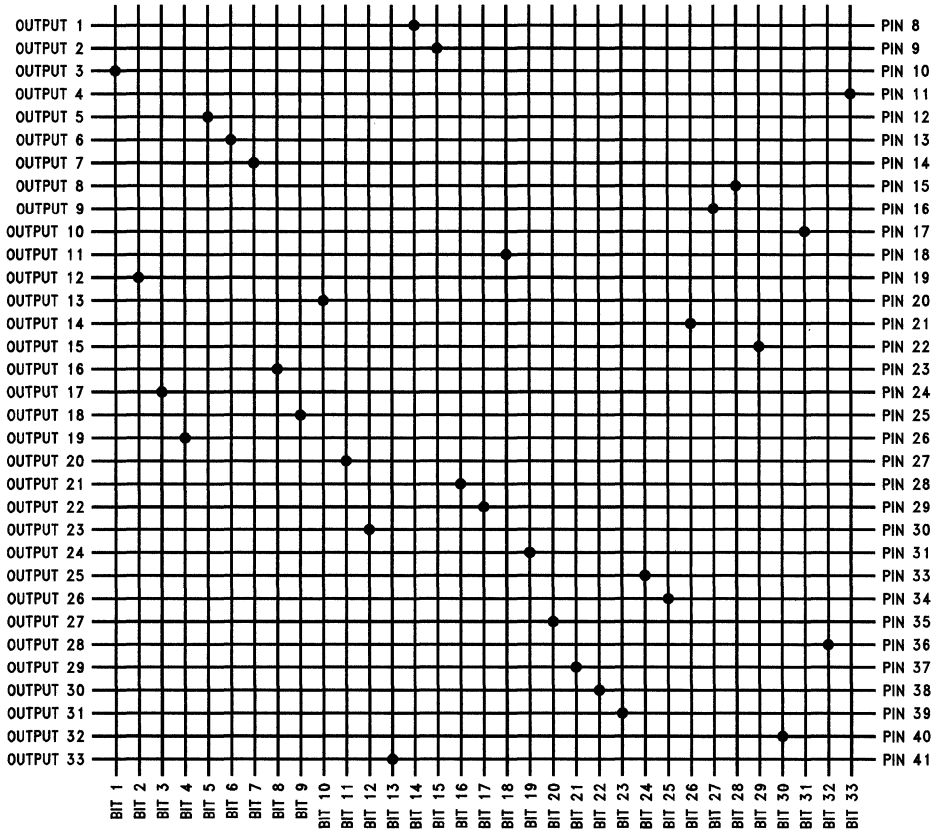

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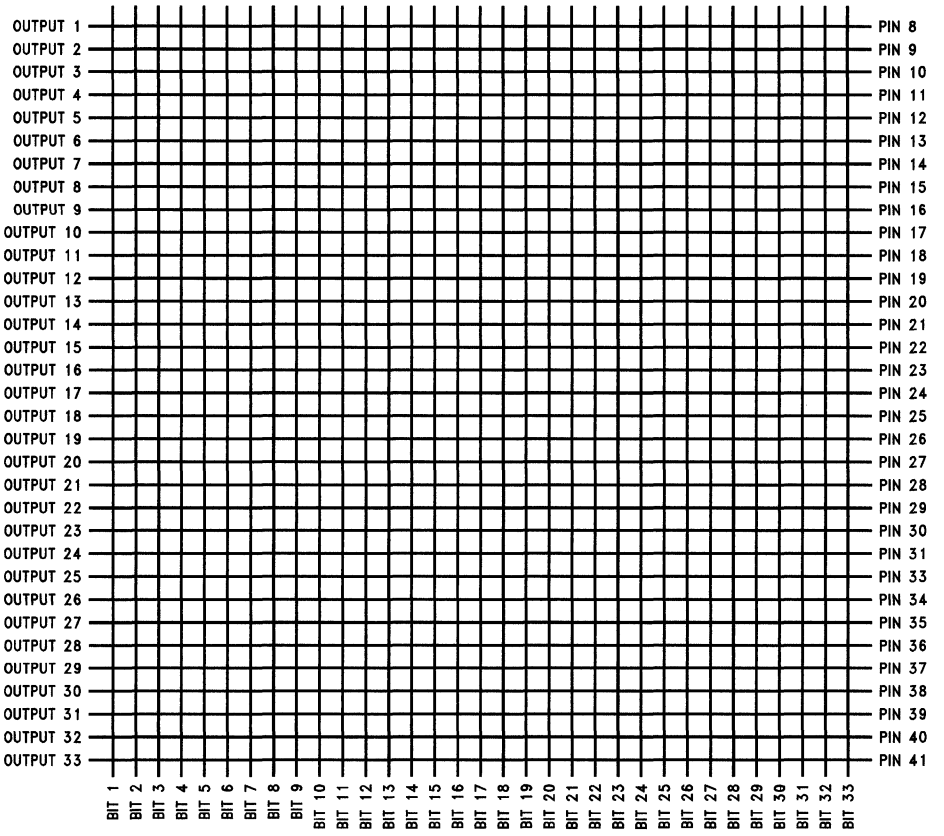
TABLE II. Customer Fill In, Output Pin to Shift Register Conversion

Pin Name	Shift Register	Pin Name	Shift Register	Pin Name	Shift Register
OUTPUT 1	BIT	OUTPUT 12	BIT	OUTPUT 23	BIT
OUTPUT 2	BIT	OUTPUT 13	BIT	OUTPUT 24	BIT
OUTPUT 3	BIT	OUTPUT 14	BIT	OUTPUT 25	BIT
OUTPUT 4	BIT	OUTPUT 15	BIT	OUTPUT 26	BIT
OUTPUT 5	BIT	OUTPUT 16	BIT	OUTPUT 27	BIT
OUTPUT 6	BIT	OUTPUT 17	BIT	OUTPUT 28	BIT
OUTPUT 7	BIT	OUTPUT 18	BIT	OUTPUT 29	BIT
OUTPUT 8	BIT	OUTPUT 19	BIT	OUTPUT 30	BIT
OUTPUT 9	BIT	OUTPUT 20	BIT	OUTPUT 31	BIT
OUTPUT 10	BIT	OUTPUT 21	BIT	OUTPUT 32	BIT
OUTPUT 11	BIT	OUTPUT 22	BIT	OUTPUT 33	BIT



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4

TABLE III. VD Threshold Dimming Voltage V.S. PWM Duty Cycle (Typical Value at V_{CC} = 12.8V)
10.2% PWM Maximum

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
			V_{REF}	26	56/2048	2.73	3.385
			V_{REF}	25	52/2048	2.54	3.323
			V_{REF}	24	48/2048	2.34	3.263
49	208/2048	10.2	V_{REF}	23	46/2048	2.25	3.204
48	192/2048	9.38	4.621	22	44/2048	2.15	3.155
47	184/2048	8.98	4.541	21	42/2048	2.05	3.118
46	176/2048	8.59	4.488	20	40/2048	1.95	3.076
45	168/2048	8.20	4.434	19	38/2048	1.86	3.027
44	160/2048	7.81	4.381	18	36/2048	1.76	2.983
43	152/2048	7.42	4.333	17	34/2048	1.66	2.941
42	144/2048	7.03	4.286	16	32/2048	1.56	2.898
41	136/2048	6.64	4.231	15	30/2048	1.46	2.860
40	128/2048	6.25	4.170	14	28/2048	1.37	2.822
39	120/2048	5.86	4.106	13	26/2048	1.27	2.785
38	112/2048	5.47	4.043	12	24/2048	1.17	2.744
37	104/2048	5.08	3.980	11	23/2048	1.12	2.692
36	96/2048	4.69	3.914	10	22/2048	1.07	2.650
35	92/2048	4.49	3.831	9	21/2048	1.03	2.622
34	88/2048	4.30	3.766	8	20/2048	0.98	2.597
33	84/2048	4.10	3.719	7	19/2048	0.93	2.569
32	80/2048	3.91	3.673	6	18/2048	0.88	2.539
31	76/2048	3.71	3.631	5	17/2048	0.83	2.511
30	72/2048	3.52	3.594	4	16/2048	0.78	2.478
29	68/2048	3.32	3.551	3	15/2048	0.73	2.455
28	64/2048	3.13	3.501	2	14/2048	0.68	2.425
27	60/2048	2.93	3.444	1	13/2048	0.63	2.392
							0.000

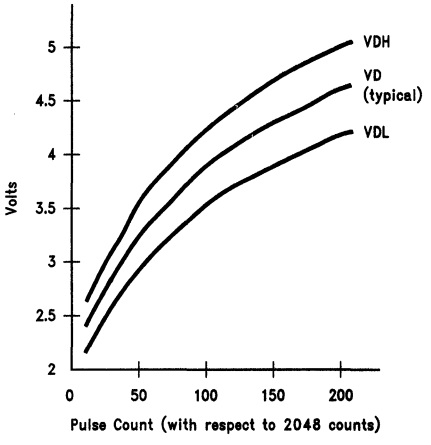

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FIGURE 6. Dimming Curve
(Graphical Representation of Table III)

National Semiconductor

DS75491 MOS-to-LED Quad Segment Driver
DS75492 MOS-to-LED Hex Digit Driver

General Description

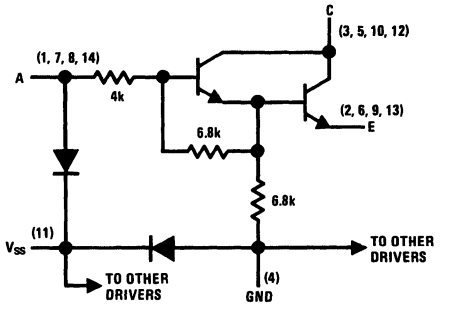
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LEDs in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492)
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

Schematic and Connection Diagrams

DS75491 (each driver)



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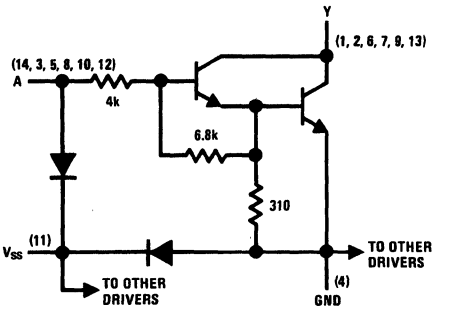
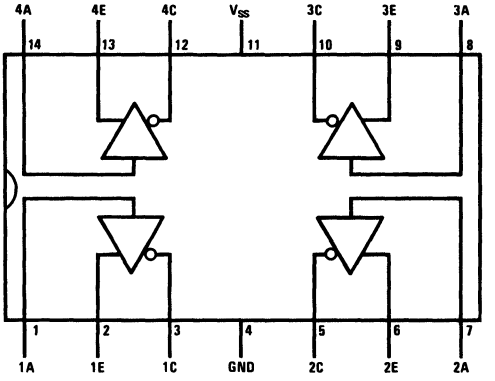
DS75492 (each driver)



TL/F/5830–2

DS75491 Dual-In-Line Package



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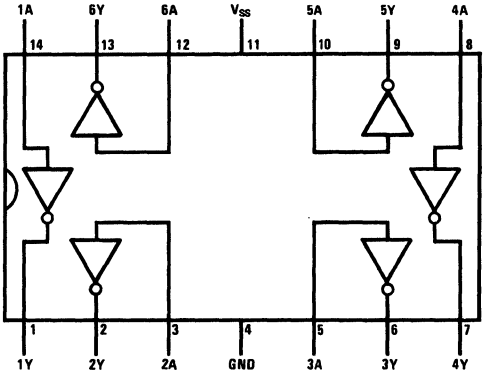
Top View

DS75492 Dual-In-Line Package



TL/F/5830–4

Top View

Order Number DS75491N or DS75492N
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	DS75491	DS75492
Input Voltage Range (Note 4)	−5V to V_{SS}	
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal with Respect to any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA

	DS75491	DS75492
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temp. (Soldering, 10 sec)	300°C	300°C
Maximum Power Dissipation at 25°C		
Molded Package	1207 mW*	1280 mW†

*Derate molded package 9.66 mW/°C above 25°C.

†Derate molded package 10.24 mW/°C above 25°C.

Electrical Characteristics V_{SS} = 10V (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS75491							
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	V_C = 10V, V_E = 0V	I_{IN} = 40 μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0V, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0V, V_E = 5V, I_C = 0 mA				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA
DS75492							
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 250 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
I_{OH}	High Level Output Current	V_{OH} = 10V	I_{IN} = 40 μA			200	μA
			V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

Switching Characteristics V_{SS} = 7.5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DS75491						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0V, R_L = 200Ω, C_L = 15 pF		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)			20		ns
DS75492						
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

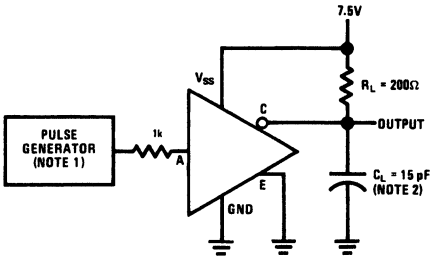
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

AC Test Circuits and Switching Time Waveforms

DS75491



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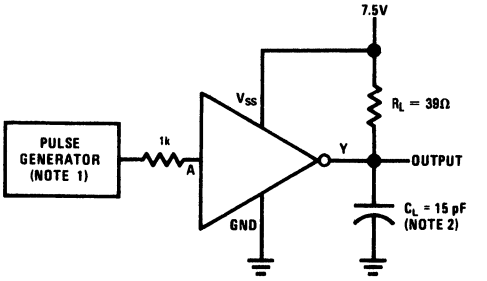
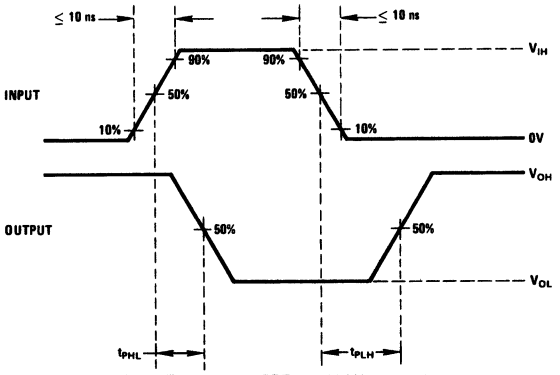
DS75492



TL/F/5830–6



TL/F/5830–7

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1 μs.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS55494/DS75494 Hex Digit Driver

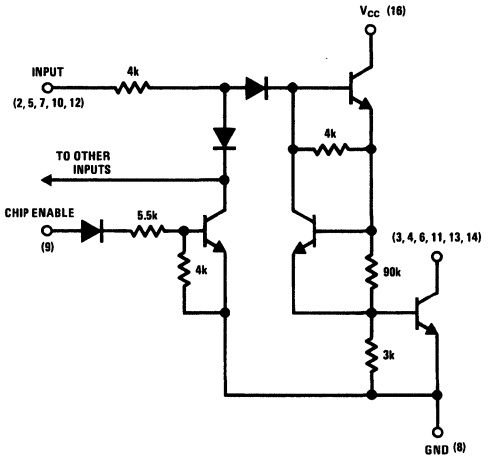
General Description

The DS55494/DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

Features

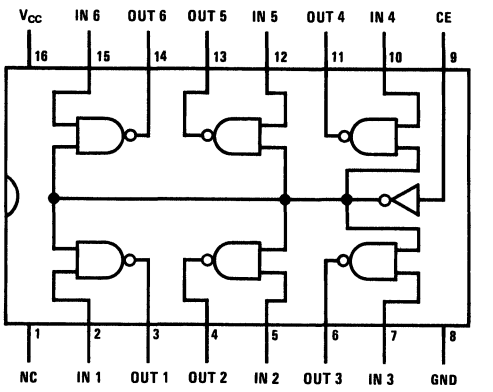
- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

Schematic and Connection Diagrams



TL/F/5832–1

Dual-In-Line Package



TL/F/5832–2

Top View
Order Number DS55494J
or DS75494N
See NS Package Number J16A or N16A

Truth Table

Enable	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering 4 seconds)	260°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A			
DS75494	0	+70	°C
DS55494	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

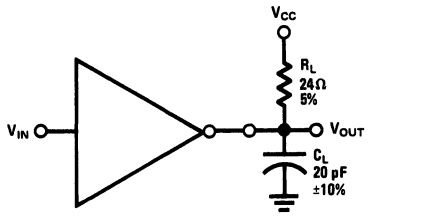
Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V	V_{CE} = 8.8V through 100k				2.0	mA
			V_{CE} = 8.8V				2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V					−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V	V_{IN} = 8.8V through 100k, V_{CE} = 0V				400	μA
			V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k				400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k		DS75494		0.25	0.35	V
				DS55494		0.25	0.4	V
I_{CC}	Supply Currents	V_{CC} = Max	One Driver "ON", V_{IN} = 8.8V	DS75474			8.0	mA
				DS55494			10.0	mA
			All Other Pins to GND	V_{CE} = 6.5V through 1.0k			100	μA
				V_{IN} = 8.8V through 100k			100	μA
			All Other Pins to GND				40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits				0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits				13	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

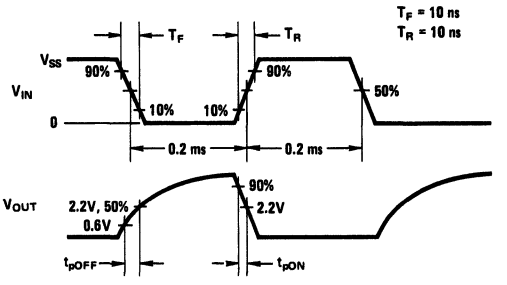
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494 and across the −55°C to +125°C range for the DS55494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



TL/F/5832-3



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National Semiconductor

MM5450/MM5451 LED Display Drivers

General Description

The MM5450 and MM5451 are monolithic MOS integrated circuits utilizing N-channel metal-gate low threshold, enhancement mode, and ion-implanted depletion mode devices. They are available in 40-pin molded or cavity dual-in-line packages. The MM5450/MM5451 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

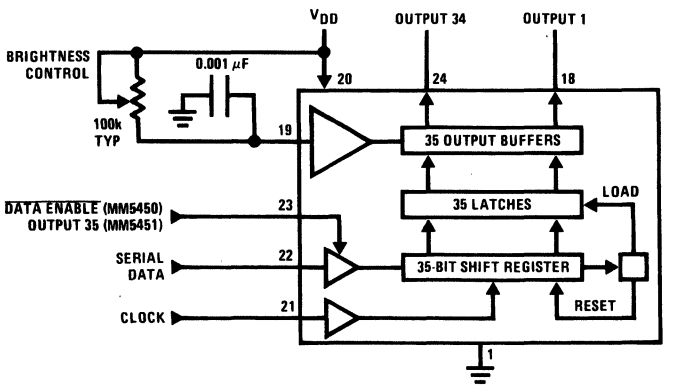
Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA sink capability
- Alphanumeric capability
- θ_{JA} DIP — Board = 49°C/W, Socket = 54°C/W

Block Diagram



TL/F/6136–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} − 0.3V to V_{SS} + 12V
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Power Dissipation at +25°C

Molded DIP Package, Board Mount	2.5W*
Molded DIP Package, Socket Mount	2.3W**

*Molded DIP Package board mount, θ_{JA} = 49°C/W, Derate 20.4 mW/°C above 25°C.

**Molded DIP Package, socket mount, θ_{JA} = 54°C/W, Derate 18.5 mW/°C above 25°C.

Electrical Characteristics T_A within operating range, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		4.75		11	V
Power Supply Current	Excluding Output Loads			7	mA
Input Voltages					
Logical "0" Level (V_L)	±10 μA Input Bias	−0.3		0.8	V
Logical "1" Level (V_H)	4.75V ≤ V_{DD} ≤ 5.25V	2.2		V_{DD}	V
	V_{DD} > 5.25V	V_{DD} − 2V		V_{DD}	V
Brightness Input (Note 2)		0		0.75	mA
Output Sink Current					
Segment OFF	V_{OUT} = 3.0V			10	μA
Segment ON	V_{OUT} = 1V (Note 3)				
	Brightness Input = 0 μA	0		10	μA
	Brightness Input = 100 μA	2.0	2.7	4	mA
	Brightness Input = 750 μA	15		25	mA
Brightness Input Voltage (Pin 19)	Input Current 750 μA	3.0		4.3	V
Output Matching (Note 1)				±20	%
Clock Input	(Notes 5 and 6)				
Frequency, f_C				500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input					
Set-Up Time, t_{DES}		100			ns

Note 1: Output matching is calculated as the percent variation (I_{MAX} + I_{MIN})/2.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: See *Figures 5, 6,* and *7* for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

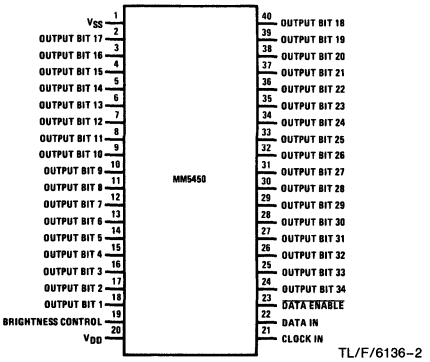
Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6* and *7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: t_r ≤ 20 ns, t_f ≤ 20 ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

Dual-In-Line Package



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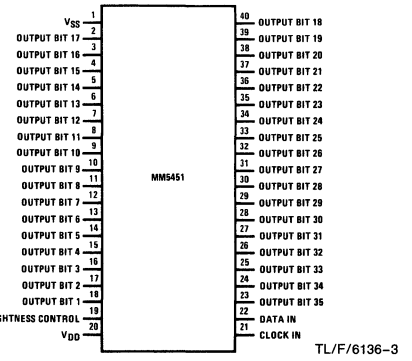
Top View

FIGURE 2a

Dual-In-Line Package



TL/F/6136–3

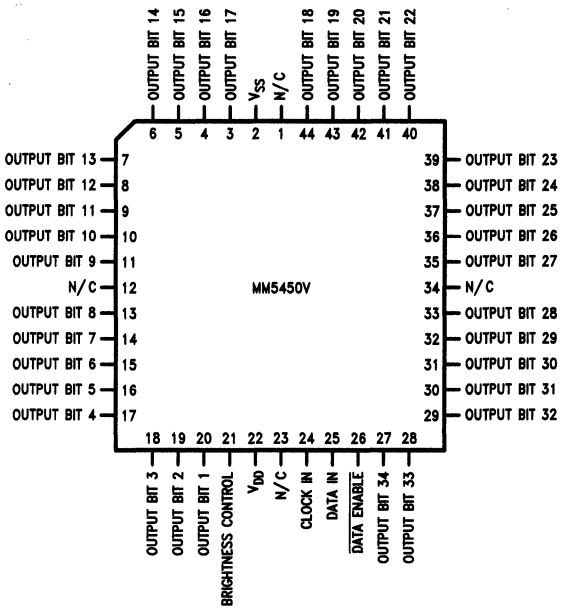
Top View

FIGURE 2b

Order Number MM5450N, MM5451N, MM5450V or MM5451V
See NS Package Number N40A or V44A

Connection Diagrams (Continued)

Plastic Chip Carrier



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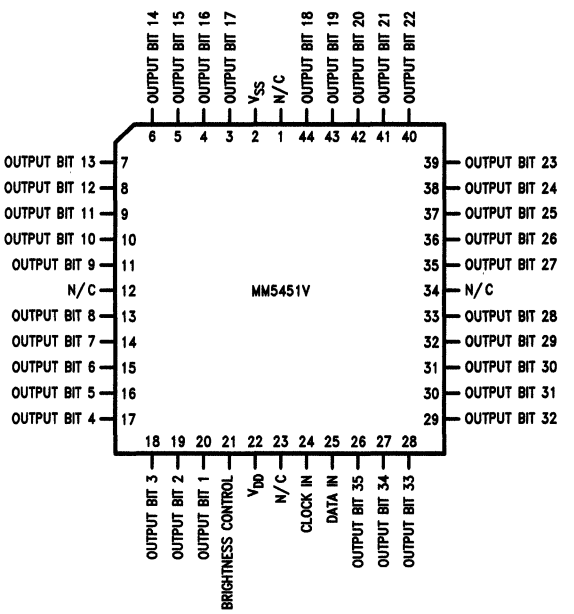
Top View

Plastic Chip Carrier



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Top View

Functional Description

Both the MM5450 and the MM5451 are specifically designed to operate 4- or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in *Figure 1.* For the MM5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the MM5450. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 2 shows the pin-out of the MM5450 and MM5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$T_j = (V_{OUT})\,(I_{LED})$ (No. of segments)$(\theta_{JA}) + T_A$

where:

T_j = junction temperature, 150°C max

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

θ_{JA} = thermal coefficient of the package

T_A = ambient temperature

θ_{JA} (Socket Mount) = 54°C/W

θ_{JA} (Board Mount) = 49°C/W

The above equation was used to plot *Figure 5, Figure 6* and *Figure 7.*

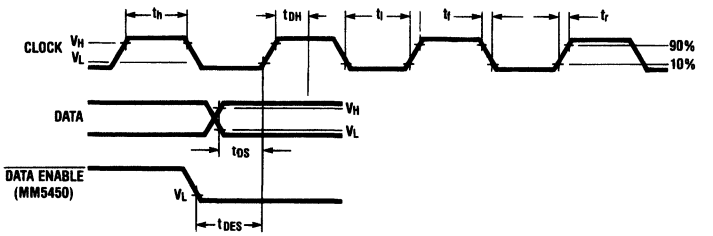

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FIGURE 3

Functional Description (Continued)

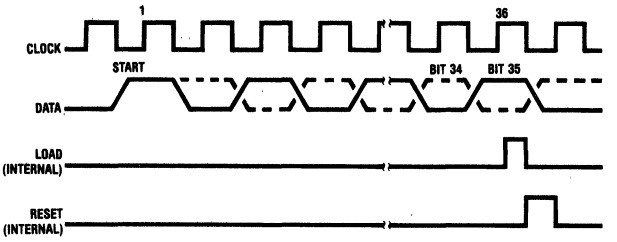

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FIGURE 4. Input Data Format

Typical Performance Characteristics

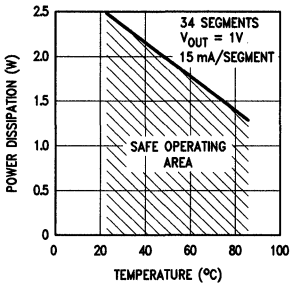

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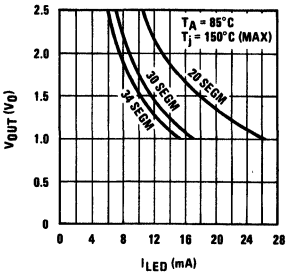
FIGURE 5



TL/F/6136–7

FIGURE 6

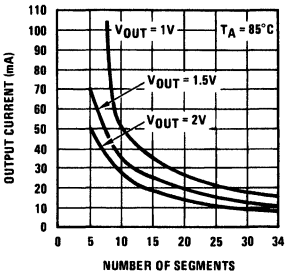


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FIGURE 7

Typical Applications

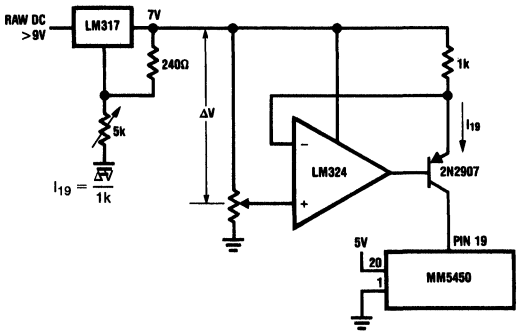

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FIGURE 8. Typical Application of Constant Current Brightness Control

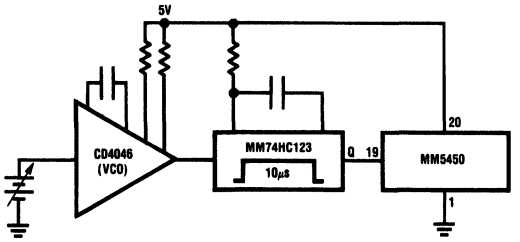

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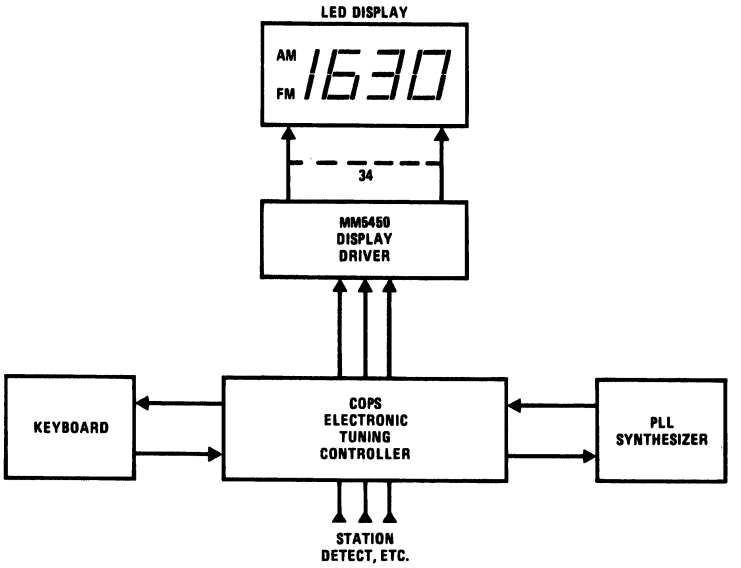
FIGURE 9. Brightness Control Varying the Duty Cycle

Typical Applications (Continued)

Basic Electronically Tuned Radio System



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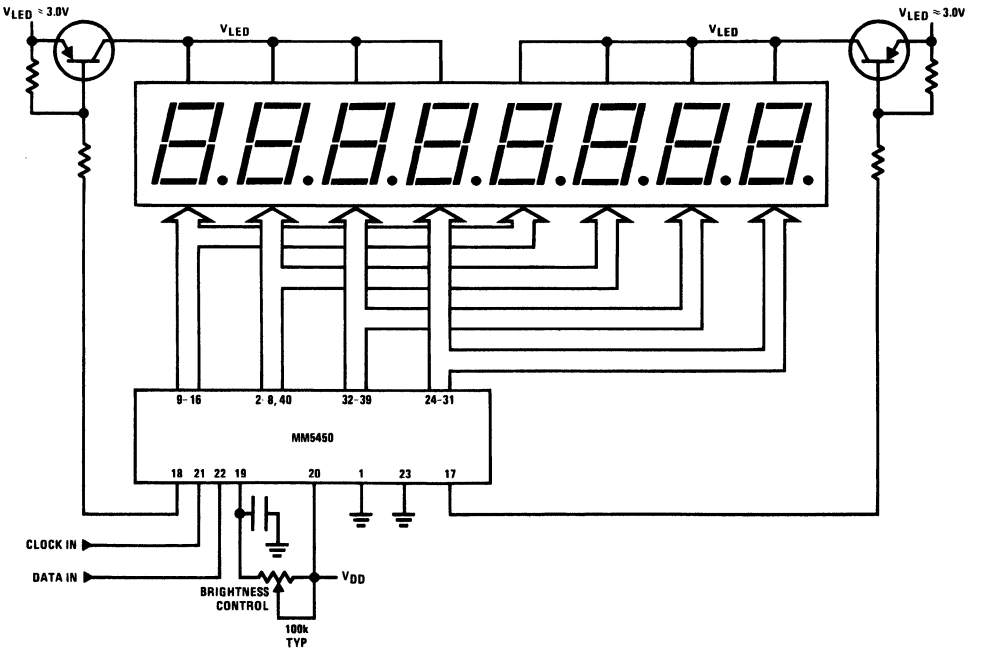
Duplexing 8 Digits with One MM5450



TL/F/6136–12

National Semiconductor

MM5452/MM5453 Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4 ½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

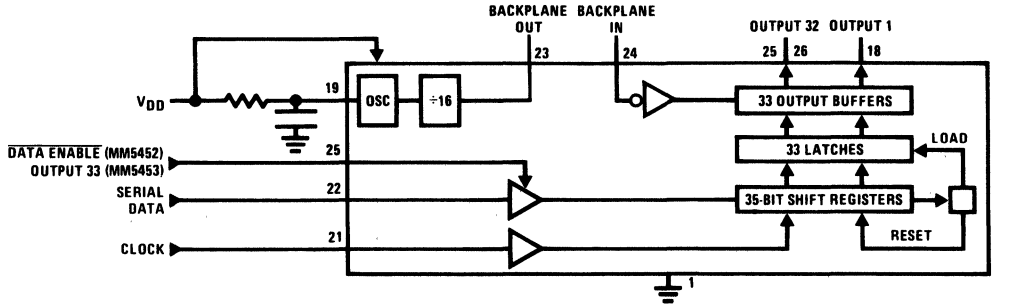
Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block Diagram



TL/F/6137–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +70°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3		10	V
Power Supply Current	Excluding Outputs				
	OSC = V_{SS}, BP IN @ 32 Hz			40	μA
	V_{DD} = 5V, Open Outputs, No Clock			10	μA
Clock Frequency				500	kHz
Input Voltages					
Logical '0' Level	V_{DD} < 4.75	−0.3		0.1 V_{DD}	V
	V_{DD} ≥ 4.75	−0.3		0.8	V
Logical '1' Level	V_{DD} > 5.25	0.8 V_{DD}		V_{DD}	V
	V_{DD} ≤ 5.25	2.0		V_{DD}	V
Output Current Levels					
Segments					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−20	μA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	20			μA
Backplane					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−320	μA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	320			μA
Output Offset Voltage	Segment Load 250 pF Backplane Load 8750 pF (Note 1)			±50	mV
Clock Input Frequency, f_C	(Notes 2 and 3)			500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input Set-Up Time, t_{DES}		100			ns

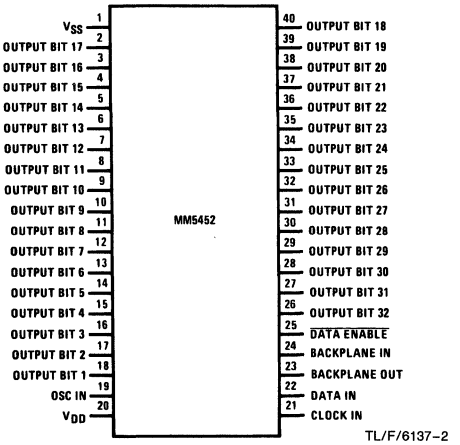
Note 1: This parameter is guaranteed (not 100% production tested) over operating temperature and supply voltage ranges. Not to be used in Q.A. testing.

Note 2: AC input waveform for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

Dual-In-Line Package



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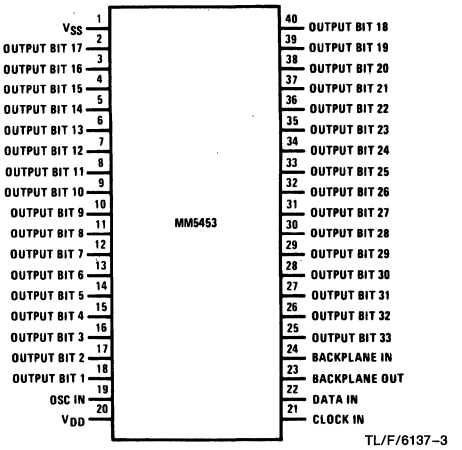
Top View
FIGURE 2a

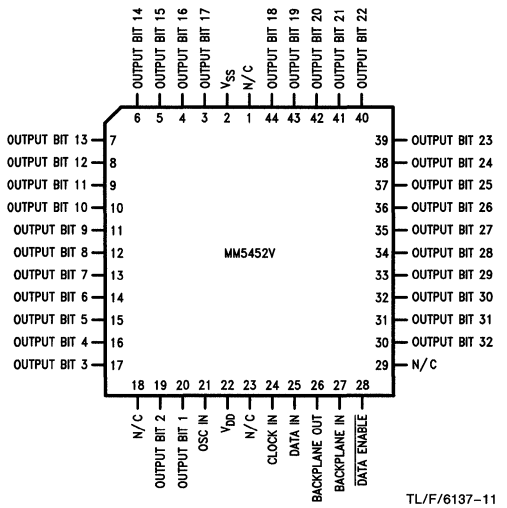
Dual-In-Line Package



TL/F/6137–3

Top View
FIGURE 2b

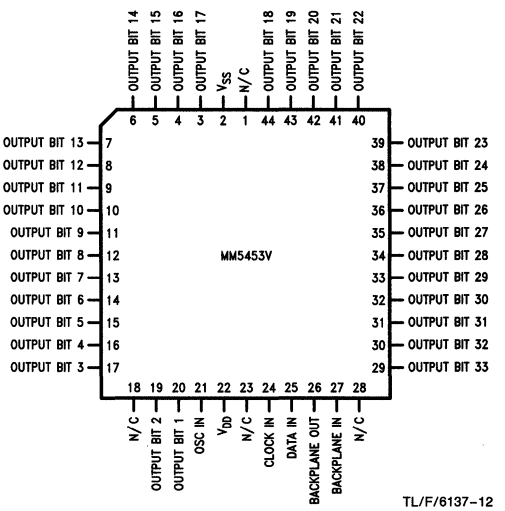
Plastic Chip Carrier



TL/F/6137–11

Top View

Plastic Chip Carrier



TL/F/6137–12

Top View

Order Number MM5452N, MM5453N,
MM5452V or MM5453V
See NS Package Number N40A or V44A

Functional Description

The MM5452 is specifically designed to operate 4 ½-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading "1" followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in *Figure 1.* For the MM5452 a $\overline{\text{DATA ENABLE}}$ is used instead of the 33rd output. If the $\overline{\text{DATA ENABLE}}$ signal is not required, the 33rd output can be brought out. This is the MM5453 device.

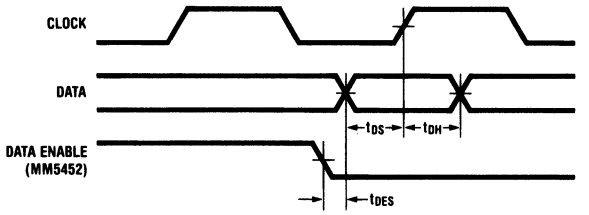
Functional Description (Continued)

Figure 4 shows the input data format. A start bit of logical "1" precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be a complete set of 36 clocks otherwise the shift registers will not clear.

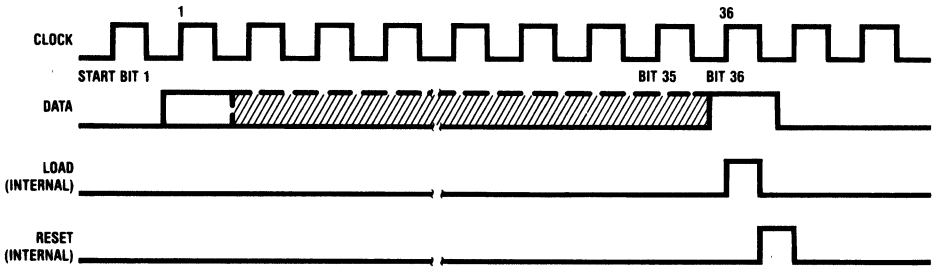
Figure 2a shows the pin-out of the MM5452. Bit 1 is the first bit following the start bit and it will appear on pin 18.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$.



TL/F/6137–4

FIGURE 3

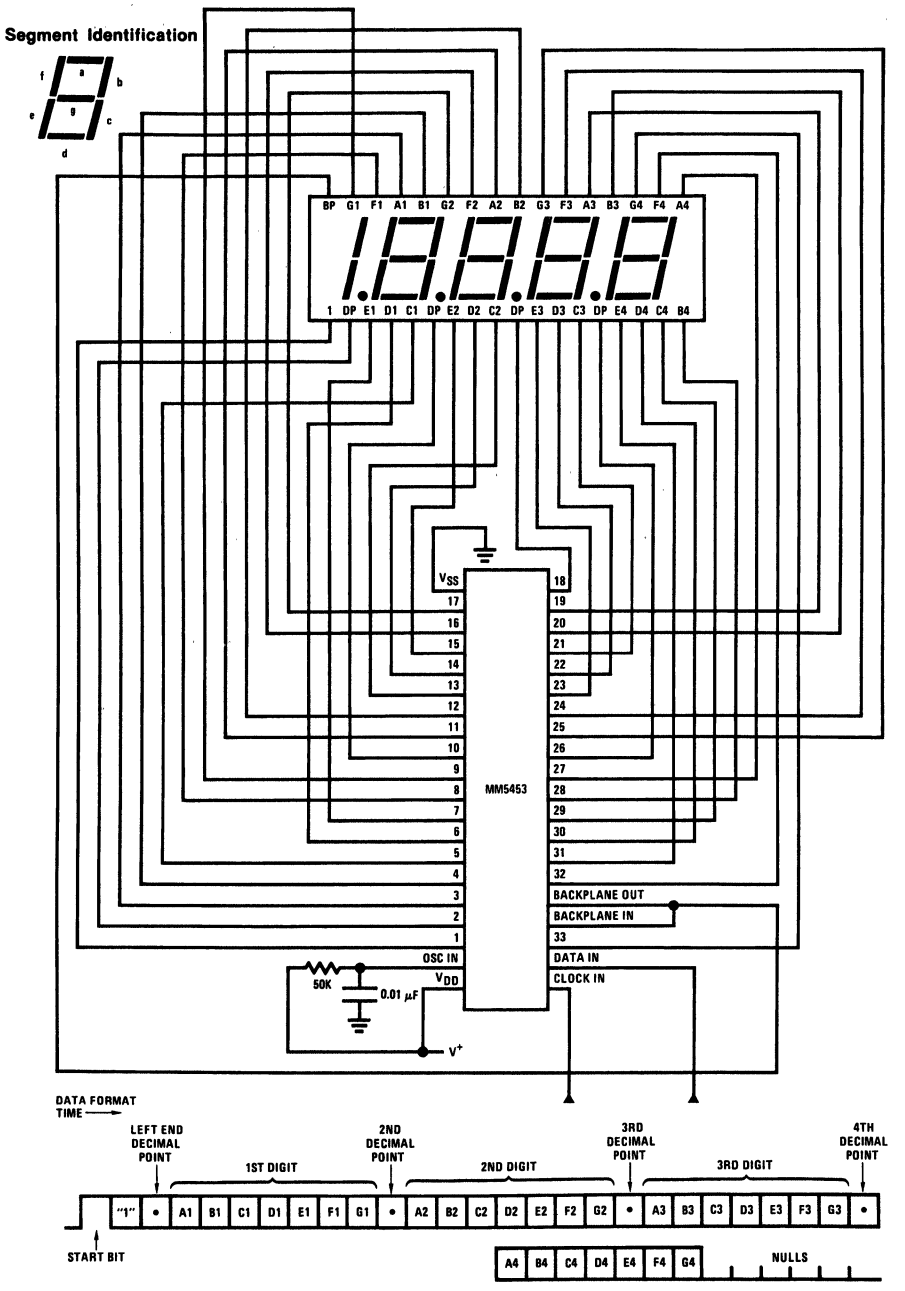


TL/F/6137–5

FIGURE 4. Input Data Format

Functional Description (Continued)

Figure 5 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. This application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.

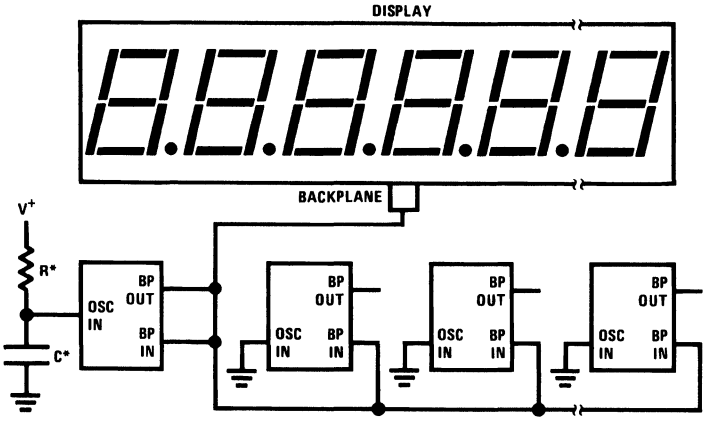


TL/F/6137–6

Consult LCD manufacturer's data sheet for specific pinouts.

FIGURE 5. Typical 4½-Digit Display Application

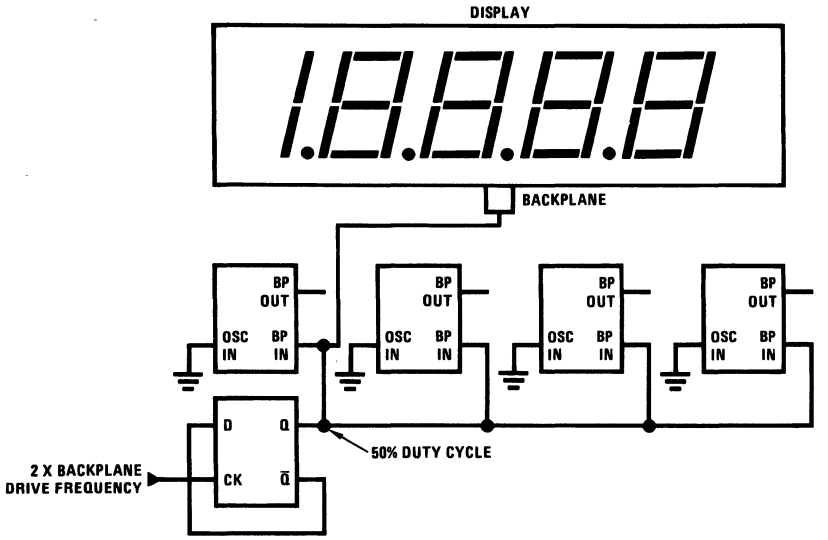
Functional Description (Continued)



TL/F/6137–7

*The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately 4.91×10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 6. Parallel Backplane Outputs



TL/F/6137–8

FIGURE 7. External Backplane Clock

Figure 8 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

USING AN EXTERNAL CLOCK

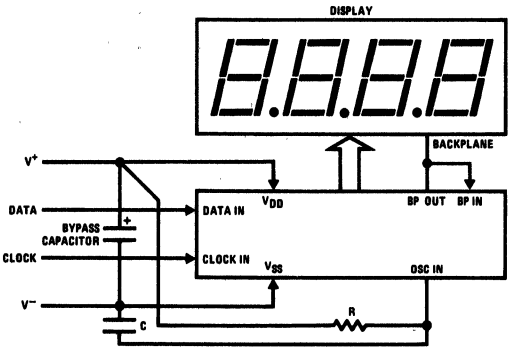
The MM5452/MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In *Figure 7,* a flip-flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumptions in the chips. The oscillator is not used.

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 9 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

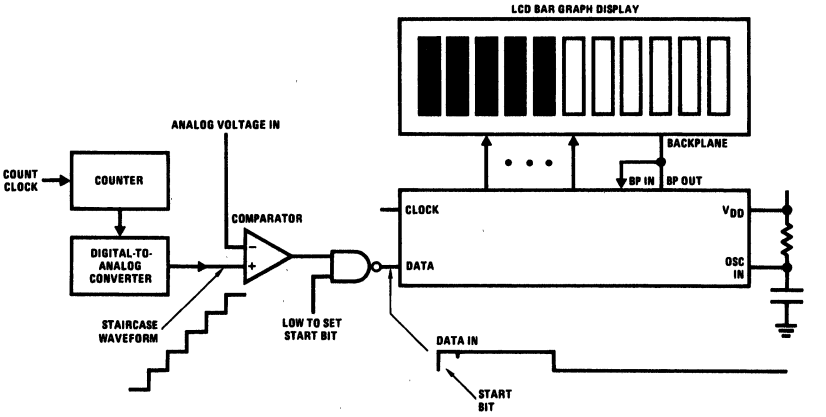
With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.

Functional Description (Continued)



TL/F/6137–9

FIGURE 8. Four Wire Remote Display



TL/F/6137–10

Data is high until staircase > input

FIGURE 9. Analog Display

National Semiconductor

MM5480 LED Display Driver

General Description

The MM5480 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5451 die packaged in a 28-pin package making it ideal for a 3½ digit display. The MM5480 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

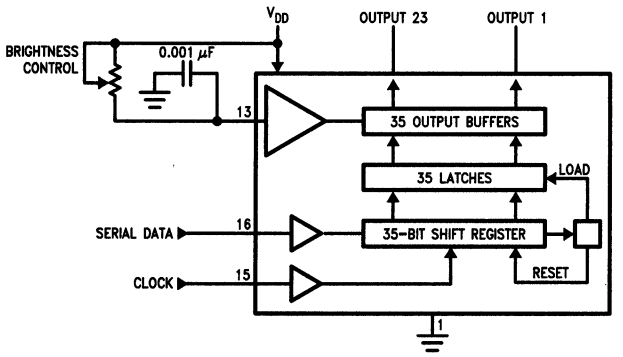
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 3½ digit displays

Applications

- COPS™ microcontrollers or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

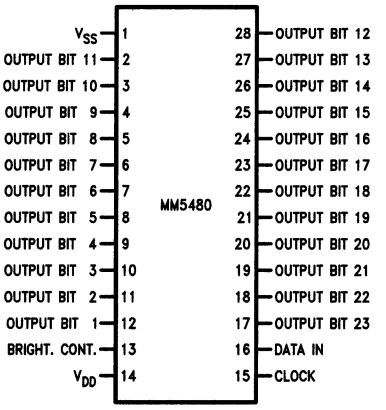


TL/F/6138–1

FIGURE 1

Connection Diagram

Dual-In-Line Package



Order Number MM5480N
See NS Package Number N28B

TL/F/6138–2

Top View
FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{SS} + 12V$
Storage Temperature	−65°C to +150°C

Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.4W*
Molded DIP Package, Socket Mount	2.1W**
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Molded DIP Package, Board Mount, θ_{JA} = 52°C/W, Derate 19.2 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 58°C/W, Derate 17.2 mW/°C above 25°C.

Electrical Characteristics

T_A = −25°C to +85°C, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
V_{IL}	Input Voltage Logical "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Input Voltage Logical "1" Level	4.75V ≤ V_{DD} ≤ 5.25V	2.2		V_{DD}	V
		V_{DD} > 5.25V	V_{DD} − 2		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
I_{OH}	Output Sink Current (Note 3) Segment OFF	V_{OUT} = 3.0V			10.0	μA
I_{OL}	Output Sink Current (Note 3) Segment ON	V_{OUT} = 1V				
		Brightness Input = 0 μA	0		10.0	μA
		Brightness Input = 100 μA	2.0	2.7	4.0	mA
		Brightness Input = 750 μA	15.0		25.0	mA
V_{IBR}	Brightness Input Voltage (Pin 13)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics T_A = −25°C to +85°C, V_{DD} = 5V ±0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
t_{DS}	Data Input Set-Up Time		300			ns
t_{DH}	Data Input Hold Time		300			ns

Note 1: Output matching is calculated as the percent variation from $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5480 is specifically designed to operate 3½-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF ceramic or mica disc capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are 'Don't Cares'.

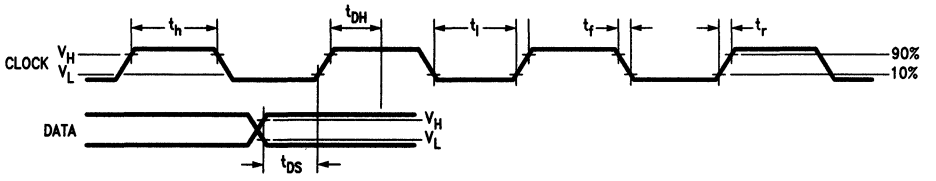
Figure 3 shows the timing relationships between data and clock. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(\theta_{JA}) + T_A$$

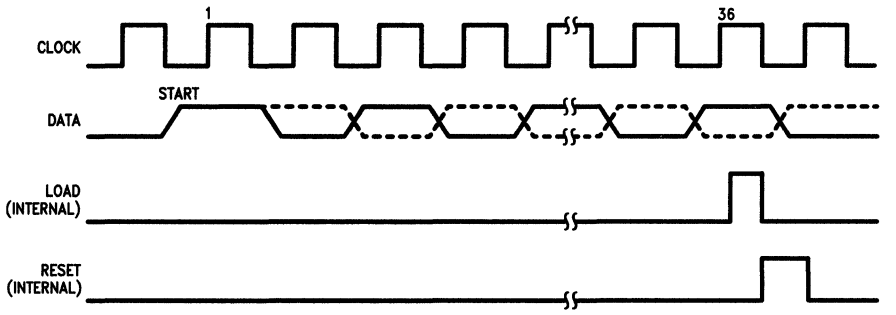
where:

T_j = junction temperature, 150°C max.
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
θ_{JA} = thermal coefficient of the package
T_A = ambient temperature
θ_{JA} (Socket Mount) = 58°C/W
θ_{JA} (Board Mount) = 52°C/W



TL/F/6138–3

FIGURE 3



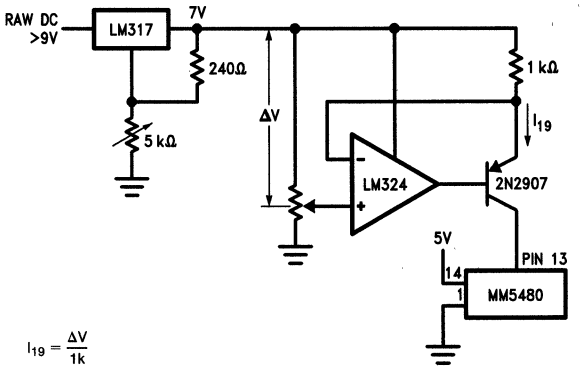
TL/F/6138–4

FIGURE 4. Input Data Format

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	5451
START	X	1	2	3	4	5	6	7	X	X	X	8	9	10	11	X	X	X	X	12	13	14	15	16	17	X	18	X	X	19	20	21	22	23	X	5480

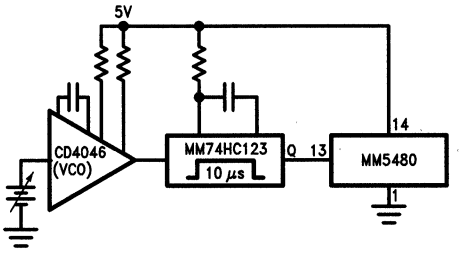
FIGURE 5. Output Data Format

Functional Description (Continued)



TL/F/6138–5

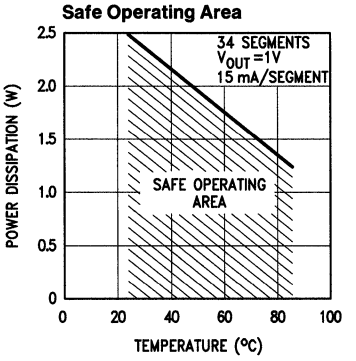
FIGURE 6. Typical Application of Constant Current Brightness Control



TL/F/6138–6

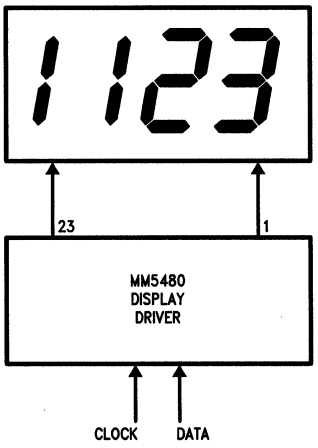
FIGURE 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



TL/F/6138–7

Basic 3½-Digit Interface



TL/F/6138–8

National Semiconductor

MM5481 LED Display Driver

General Description

The 5481 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5450 die packaged in a 20-pin package making it ideal for a 2 digit display. The MM5481 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

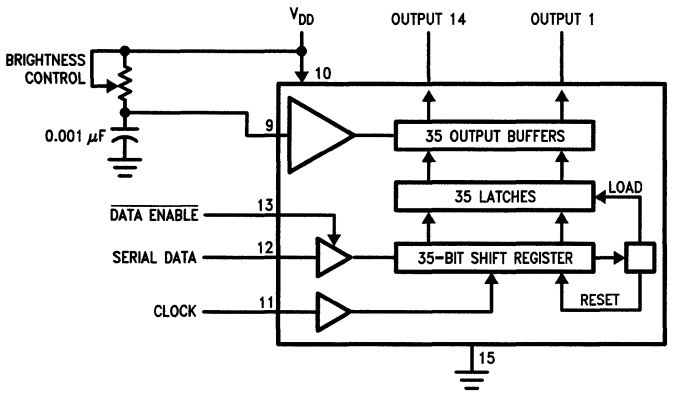
Features

- Continuous brightness control
- Serial data input
- No load signal required
- Data enable
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 2 digit LED driver

Applications

- COPS or microprocessor displays
- Industrial control indicator
- Relay driver
- Instrumentation readouts

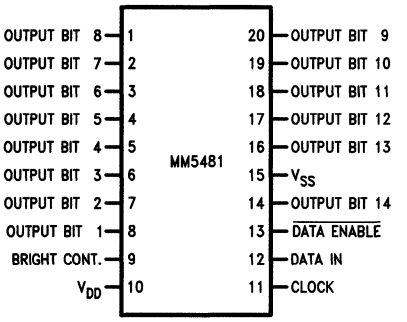
Block and Connection Diagrams



TL/F/6139–1

FIGURE 1

Dual-In-Line Package



TL/F/6139–2

Top View
FIGURE 2

Order Number MM5481N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 12V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2W*
Molded DIP Package, Socket Mount	1.8W**
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Molded DIP Package, Board Mount, θ_{JA} = 61°C/W, Derate 16.4 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 67°C/W, Derate 14.9 mW/°C above 25°C.

Electrical Characteristics

T_A = −25°C to +85°C, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
V_{IL}	Input Voltages Logical "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logical "1" Level	4.75 ≤ V_{DD} ≤ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD} − 2		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
I_{OH}	Output Sink Current (Note 3) Segment OFF	V_{OUT} = 3.0V			10.0	μA
I_{OL}	Segment ON	V_{OUT} = 1V (Note 4) Brightness Input = 0 μA Brightness Input = 100 μA Brightness Input = 750 μA	 0 2.0 15.0	 2.7 	 10.0 4.0 25.0	 μA mA mA
V_{IBR}	Brightness Input Voltage (Pin 9)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics T_A = −25°C to +85°C, V_{DD} = 5V ± 0.5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns
t_{DES}	Data Enable Input Set-Up Time		100			ns

Note 1: Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are compiled with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: t_r ≤ 20 ns, t_f ≤ 20 ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5481 uses the MM5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interference to the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the positive-going-edge of the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are a static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continous operation.

There must be a complete set of 36 clocks (high/low edges) or the shift registers will not clear.

Data Enable

This active low signal enables the data input pin. If high, the shift register sees zeroes clocked in.

To blank the display at any time, (i.e., power on), clock in 36 or more zeroes, followed by a 'one' (start bit), followed by 36 or more zeroes.

Figure 5 shows the Output Data Format for the MM5481. Because it uses only 14 of the possible 34 outputs, 20 of the bits are 'Don't Cares'. Note that only alternate groups of 4 outputs are used.

Figure 3 shows the timing relationships between data, clock, and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$T_j = (V_{OUT})(I_{LED})(\text{No. of segments})(\theta_{JA}) + T_A$

where:

T_j = junction temperature, 150°C max.

V_{OUT} = the voltage at the LED driver outputs

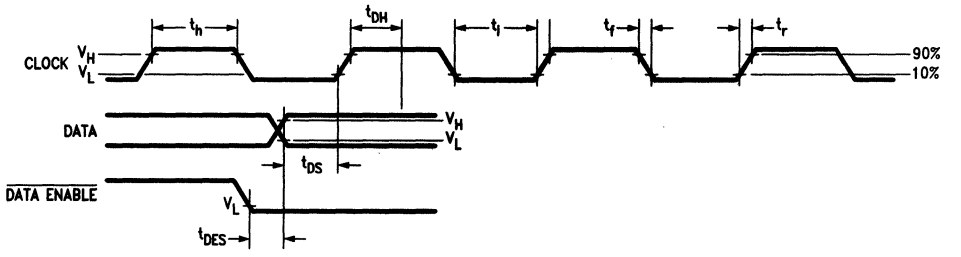
I_{LED} = the LED current

θ_{JA} = thermal coefficient of the package

T_A = ambient temperature

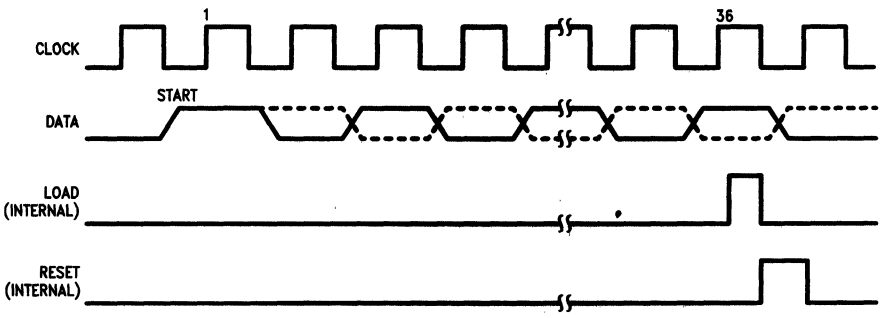
θ_{JA} (Socket Mount) = 67°C/W

θ_{JA} (Board Mount) = 61°C/W



TL/F/6139–3

FIGURE 3. Timing



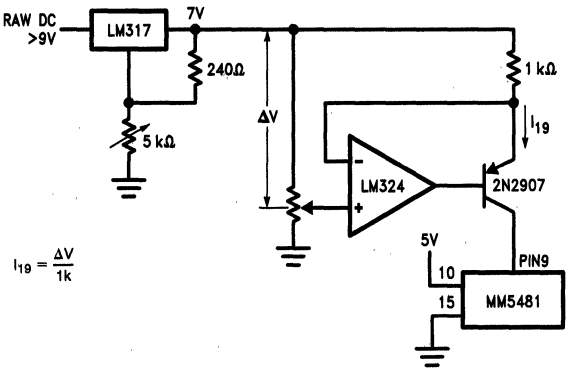
TL/F/6139–4

FIGURE 4. Input Data Format

Functional Description (Continued)

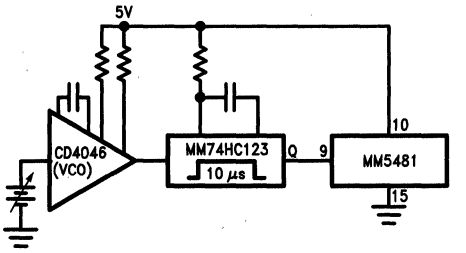
START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	5450
START	X	X	X	X	1	2	3	4	X	X	X	X	5	6	7	8	X	X	X	X	9	10	11	12	X	X	X	X	13	14	X	X	X	X	5481

FIGURE 5. Output Data Format



TL/F/6139–5

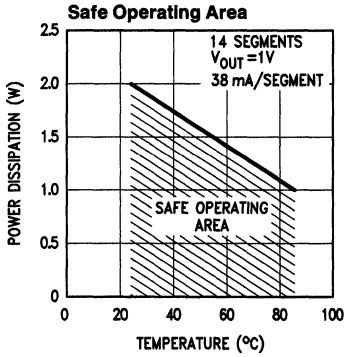
FIGURE 6. Typical Application of Constant Current Brightness Control



TL/F/6139–6

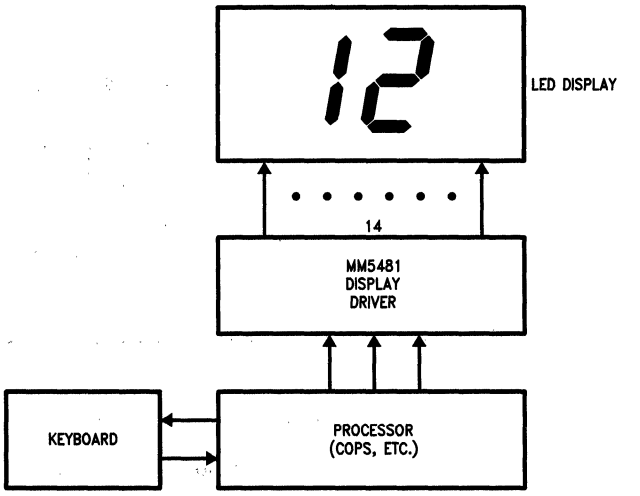
FIGURE 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



TL/F/6139–7

Basic Electronically Tuned Television System



TL/F/6139–8

National Semiconductor

MM5483 Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a $4\frac{1}{2}$-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received

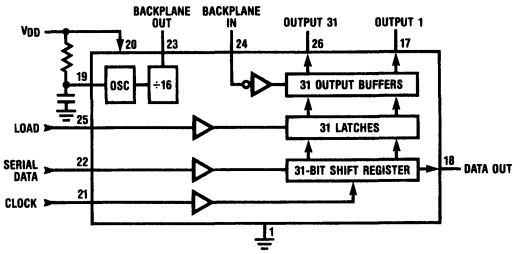
Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

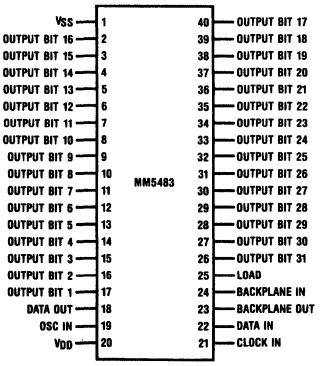
Block and Connection Diagrams



TL/F/6140–1

FIGURE 1

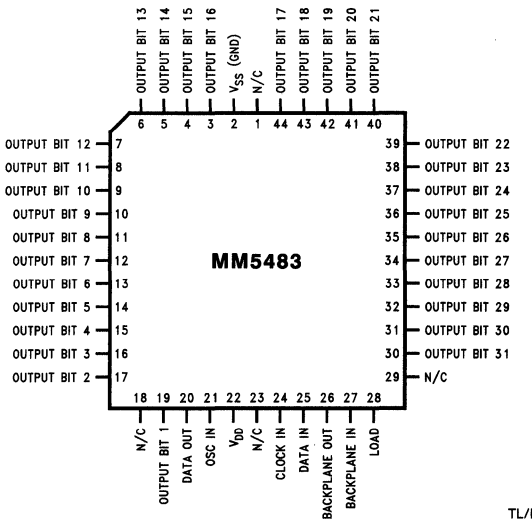
Dual-In-Line Package



TL/F/6140–2

Top View

FIGURE 2
Order Number MM5483N
See NS Package Number N40A



TL/F/6140–7

Order Number MM5483V
See NS Package Number V44A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +85°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3.0		10	V
Power Supply Current	R = 1M, C = 470 pF, Outputs Open				
	V_{DD} = 3.0V		9	15	μA
	V_{DD} = 5.0V		17	25	μA
	V_{DD} = 10.0V		35	45	μA
	OSC = 0V, Outputs Open, BPIN = 32 Hz, V_{DD} = 3.0V		1.5	2.5	μA
Input Voltage Levels	Load, Clock, Data				
Logic "0"	V_{DD} = 5.0V			0.9	V
Logic "1"	V_{DD} = 5.0V	2.4			V
Logic "0"	V_{DD} = 3.0V			0.4	V
Logic "1"	V_{DD} = 3.0V	2.0			V
Output Current Levels Segments and Data Out					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	20			μA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	20			μA
BP OUT					
Sink	V_{DD} = 3.0V, V_{OUT} = 0.3V	320			μA
Source	V_{DD} = 3.0V, V_{OUT} = 2.7V	320			μA

AC Electrical Characteristics $V_{DD} \geq 4.7V$, V_{SS} = 0V unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
f_C	Clock Frequency, V_{DD} = 3V				500	kHz
t_{CH}	Clock Period High	(Notes 1, 2)	500			ns
t_{CL}	Clock Period Low		500			ns
t_{DS}	Data Set-Up before Clock		300			ns
t_{DH}	Data Hold Time after Clock		100			ns
t_{LW}	Minimum Load Pulse Width		500			ns
t_{LTC}	Load to Clock		400			ns
t_{CDO}	Clock to Data Valid			400	750	ns

Note 1: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

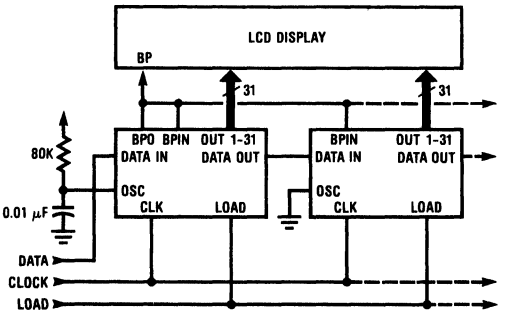
Note 2: Clock input rise and fall times must not exceed 300 ns.

Note 3: Output offset voltage is ±50 mV with $C_{SEGMENT}$ = 250 pF, C_{BP} = 8750 pF.

Functional Description

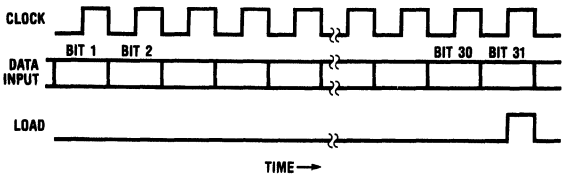
A block diagram for the MM5483 is shown in *Figure 1* and a package pinout is shown in *Figure 2*. *Figure 3* shows a possible 3-wire connection system with a typical signal format for *Figure 3*. Shown in *Figure 4*, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in *Figure 5*. In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to "walk" across the display in the 2-wire mode. An AC timing diagram can be seen in *Figure 6*. It should be noted that data out is not a TTL-compatible output.

Functional Description (Continued)



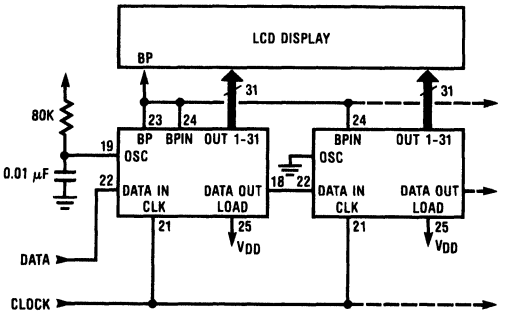
TL/F/6140–3

FIGURE 3. Three-Wire Control Mode



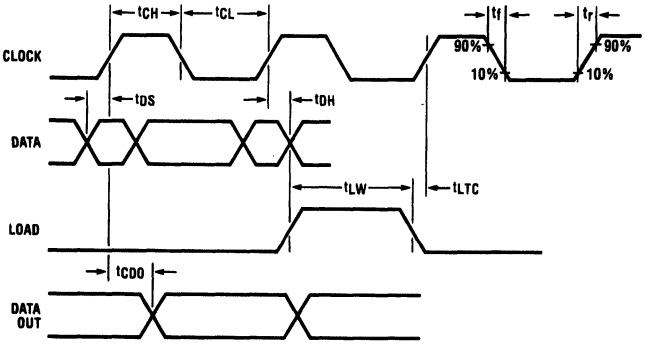
TL/F/6140–4

FIGURE 4. Data Format Diagram



TL/F/6140–5

FIGURE 5. Two-Wire Control Mode



TL/F/6140–6

FIGURE 6. Timing Diagram

National Semiconductor

MM5484 16-Segment LED Display Driver

General Description

The MM5484 is a low threshold N-channel metal gate circuit using low threshold enhancement and ion implanted depletion devices. The MM5484 is available in a 22-pin molded package and is capable of driving 16 LED segments. The MM5484 is designed to drive common anode separate cathode LED displays.

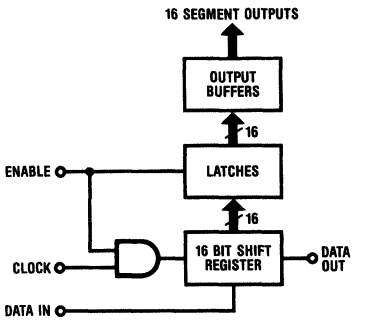
Features

- Serial data input
- Wide power supply operation
- 16 output, 15 mA sink capability
- MM5484 is cascadeable
- TTL compatibility
- No load signal required
- Non multiplex display
- 2½ digit capability—MM5484

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Industrial control indicator
- Relay driver

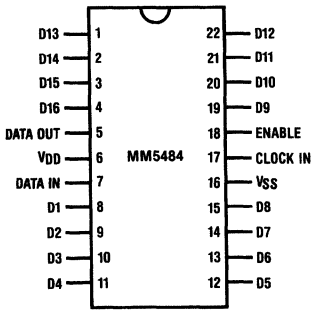
Block and Connection Diagrams



TL/F/6141–1

FIGURE 1. MM5484

Dual-In-Line Package

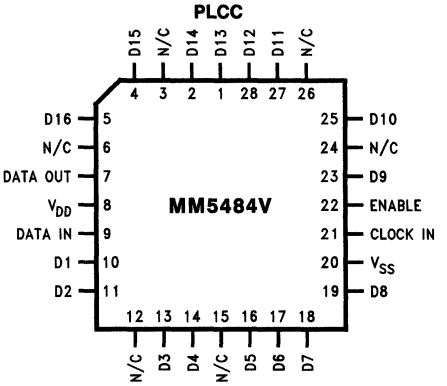


TL/F/6141–3

Top View

Order Number MM5484N
See NS Package Number N22A

PLCC



TL/F/6141–6

Top View

Order Number MM5484V
See NS Package Number V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at LED Outputs	V_{SS} − 0.5V to V_{SS} + 12V
Voltage at Other Pins	V_{SS} − 0.5V to V_{SS} + 10V
Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, board mount	2W*
Molded DIP Package, socket mount	1.8W**

*Molded DIP Package, board mount, derate 15.8m W/°C above 25°C. θ_{JA} = 63°C/W,

**Molded DIP Package, socket mount, derate 14.5m W/°C above 25°C. θ_{JA} = 69°C/W,

Lead Temperature (Soldering, 10 sec.) 300°C

DC Electrical Characteristics V_{DD} = 4.5V to 9V, T_A = −40°C to +85°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		4.5		9	V
Supply Current			5	10	mA
Logic One					
Input High Level V_{IH}		2.4		V_{DD} + 0.5	V
Logic Zero					
Input Low Level V_{IL}		0		0.8	V
Input Current	High or Low Level			±1	μA
Input Capacitance				7.5	pF
OUTPUTS					
Data Output Voltage					
High Level V_{OH}	I_{OUT} = 0.1 mA	V_{DD} − 0.5			V
Low Level V_{OL}	I_{OUT} = −0.1 mA			0.5	V
Segment Off	V_{OUT} = 12V			50	μA
(Logic Zero on Input)	R_{EXT} = 400Ω				
Output Current Segment On					
(Logic One on Input)	I_{OUT} = 15 mA		0.5	1.0	V
Output Voltage	V_{DD} ≥ 6V				

AC Electrical Characteristics

(See *Figure 3.*) V_{DD} = 4.5V to 9V, T_A = −40°C to +85°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Frequency				0.5	MHz
t_h	High Time		0.95			μs
t_l	Low Time		0.95			μs
t_{S1}	Data Setup Time		0.5			μs
t_{H1}	Data Hold Time		0.5			μs
t_{S2}	Enable Setup Time		0.5			μs
t_{H2}	Enable Hold Time		0.5			μs
t_{pd}	Data Out Delay				0.5	μs

Note 1: Under no condition should the power dissipated by the segment driver exceed 50 mW nor the entire chip power dissipation exceed 500 mW.

Note 2: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 500 ns.

Functional Description

The MM5484 is designed to drive LED displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, DATA IN, CLOCK and ENABLE. The signal ENABLE acts as an envelope and only while this signal is at a logic '1' do the circuits recognize the clock signal.

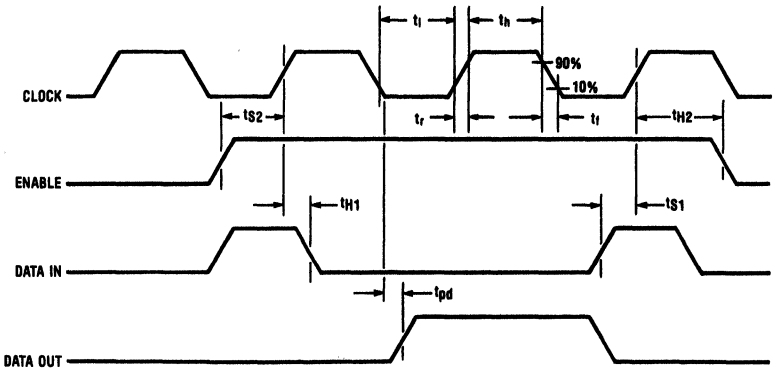
While ENABLE is high, data on the serial data input is transferred and shifted in the internal shift register on the rising clock edge, i.e. a logic '0' to logic '1' transition.

When the ENABLE signal goes to a low (logic zero state), the contents of the shift register is latched and the display will show the new data. While new data is being loaded into the SR the display will continue to show the old data.

For the MM5484, data is output from the serial DATA OUT pin on the falling edge of clock so cascading is made simple with race hazards eliminated.

When the chip first powers on, an internal power on reset signal is generated which resets the SR and latches to zero so that the display will be off.

Timing Diagram



TL/F/6141–5

FIGURE 3

National Semiconductor

MM5486 LED Display Driver

General Description

The MM5486 is a monolithic MOS integrated circuit utilizing N-channel metal-gate low-threshold, enhancement mode and ion-implanted depletion mode devices. It is available in a 40-pin molded dual-in-line package. The MM5486 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

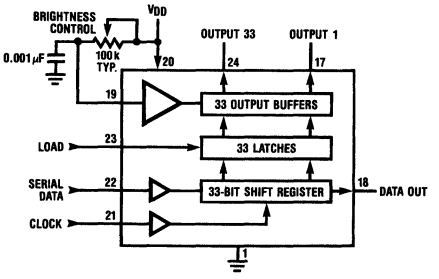
Features

- Continuous brightness control
- Serial data input/outut
- External load input
- Cascaded operation capability
- Wide power supply operation
- TTL compatibility
- 33 outputs, 15 mA sink capability
- Alphanumeric capability

Applications

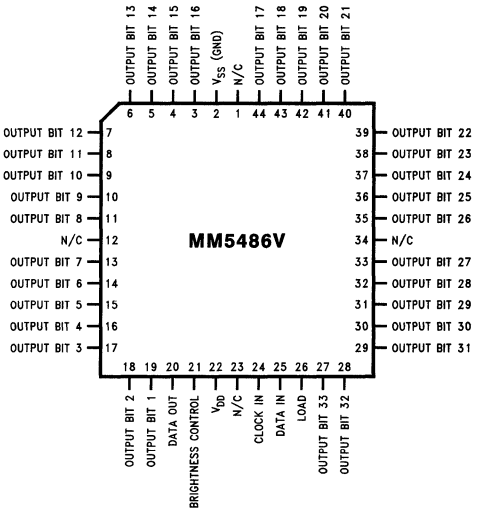
- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block and Connection Diagrams



TL/F/6142–1

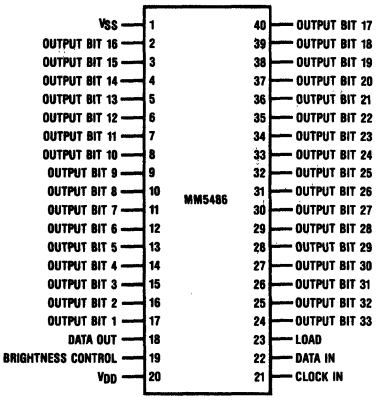
FIGURE 1



TL/F/6142–13

Order Number MM5486V
See NS Package Number V44A

Dual-In-Line Package



TL/F/6142–2

Top View

Order Number MM5486N
See NS Package Number N40A

FIGURE 2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} +12V
Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C

Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.5W*
Molded DIP Package, Socket Mount	2.3W**
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Molded DIP Package, Board Mount, θ_{JA} = 49°C/W, Derate 20.4 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 54°C/W, Derate 18.5 mW/°C above 25°C.

Electrical Characteristics

T_A within operating range, V_{DD} = 4.75V to 11.0V, V_{SS} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
	Input Voltages					
V_{IL}	Logic "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logic "1" Level	4.75 ≤ V_{DD} ≤ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD}−2		V_{DD}	V
I_{BR}	Brightness Input (Note 2)		0		0.75	mA
	Output Sink Current (Note 3)					
I_{OH}	Segment OFF	V_{OUT} = 3.0V			10	μA
I_{OL}	Segment ON	V_{OUT} = 1V (Note 4)				
		Brightness Input = 0 μA	0		10	μA
		Brightness Input = 100 μA	2.0	2.7	4	mA
		Brightness Input = 750 μA	15		25	mA
I_O	Maximum Segment Current				40	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%
	Data Output					
V_{OL}	Logical "0" Level	I_{OUT} = 0.5 mA	V_{SS}		0.4	V
V_{OH}	Logical "1" Level	I_{OUT} = 100 μA	2.4		V_{DD}	V
	Clock Input	(Notes 5 and 6)				
f_C	Frequency				500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6* and *7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5486 is specifically designed to operate four-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 3 signals, serial data, clock, and load. The data bits are latched by a positive-level load signal, thus providing non-multiplexed, direct drive to the display. When load is high, the data in the shift registers is displayed on the output drivers. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

A block diagram is shown in *Figure 1*.

Figure 4 shows the input data format. Bit "1" is the first bit into the data input pin and it will appear on pin 17. A logical "1" at the input will turn on the appropriate LED. The load signal latches the 33 bits of the shift register into the latches. The data out pin allows for cascading the shift registers for more than 33 output drivers.

When the chip first powers ON, an internal power ON reset signal is generated which resets all registers and latches. The leading clock returns the chip to its normal operation.

Figure 3 shows the timing relationship between data, clock and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations:

$$T_J = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(\theta_{JA}) + T_A$$

where:

T_J = junction temperature, 150°C max.

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

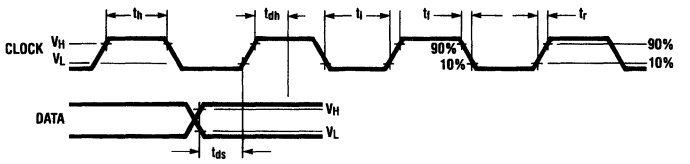
θ_{JA} = thermal coefficient of the package

T_A = ambient temperature

θ_{JA} (Socket Mount) = 54°C/W

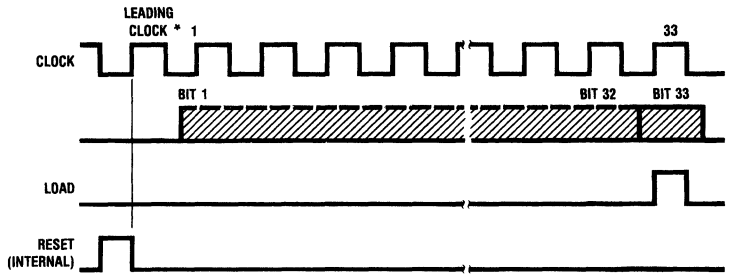
θ_{JA} (Board Mount) = 49°C/W

The above equation was used to plot *Figure 6, Figure 7,* and *Figure 8*.



TL/F/6142–3

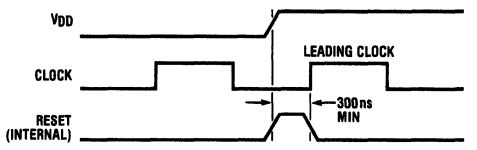
FIGURE 3



TL/F/6142–4

*This leading clock is necessary only after power ON.

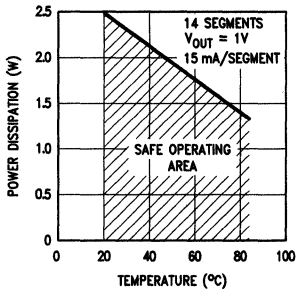
FIGURE 4. Input Data Format



TL/F/6142–5

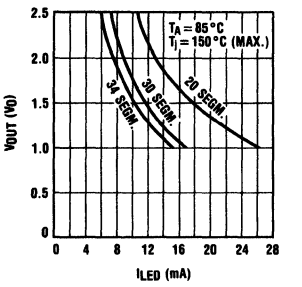
FIGURE 5

Typical Applications



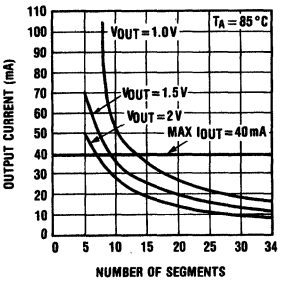
TL/F/6142–6

FIGURE 6



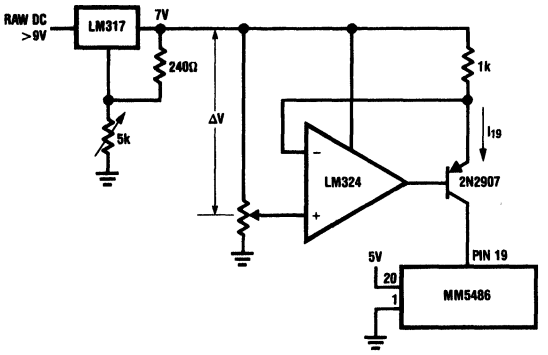
TL/F/6142–7

FIGURE 7



TL/F/6142–8

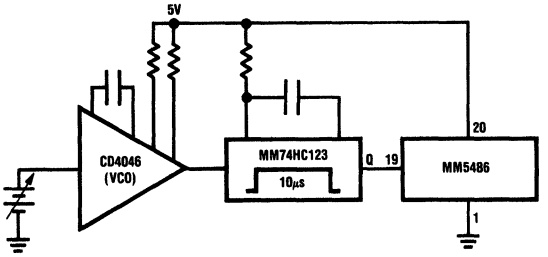
FIGURE 8



TL/F/6142–9

$$I_{19} = \frac{\Delta V}{1k}$$

FIGURE 9. Constant Current Brightness Control

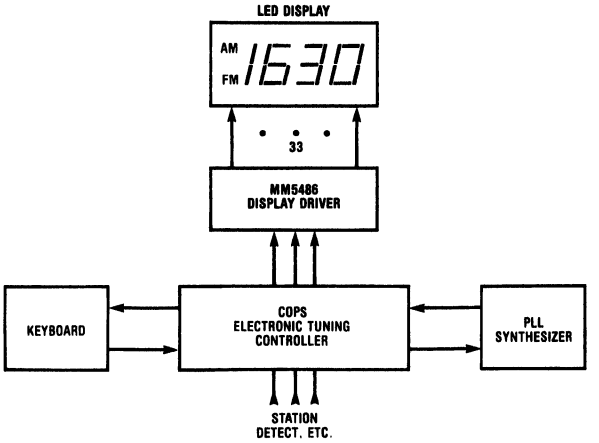


TL/F/6142–10

FIGURE 10. Brightness Control Varying the Duty Cycle

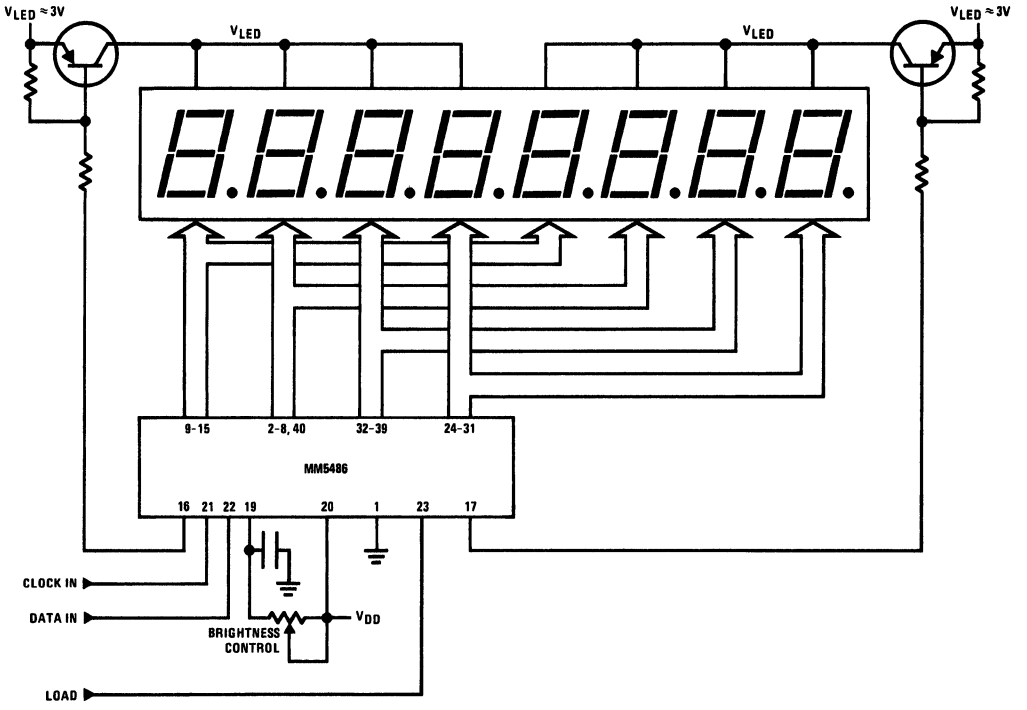
Typical Applications (Continued)

Basic Electronically Tuned Radio System



TL/F/6142–11

Duplexing 8 Digits with One MM5486



TL/F/6142–12

*This driver has 7 segments only.

National Semiconductor

MM58201 Multiplexed LCD Driver

General Description

The MM58201 is a monolithic CMOS LCD driver capable of driving up to 8 backplanes and 24 segments. A 192-bit RAM stores the data for the display. Serial input and output pins are provided to interface with a controller. An RC oscillator generates the timing necessary to refresh the display. The magnitude of the driving waveforms can be adjusted with the V_{TC} input to optimize display contrast. Four additional bits of RAM allow the user to program the number of backplanes being driven, and to designate the driver as either a master or slave for cascading purposes. When two or more drivers are cascaded, the master chip drives the backplane lines, and the master and each slave chip drive 24 segment lines. Synchronizing the cascaded drivers is accomplished by tying the RC OSC pins together and the BP1 pins together.

The MM58201 is packaged in a 40-lead dual-in-line package, or 44 lead plastic chip carrier package.

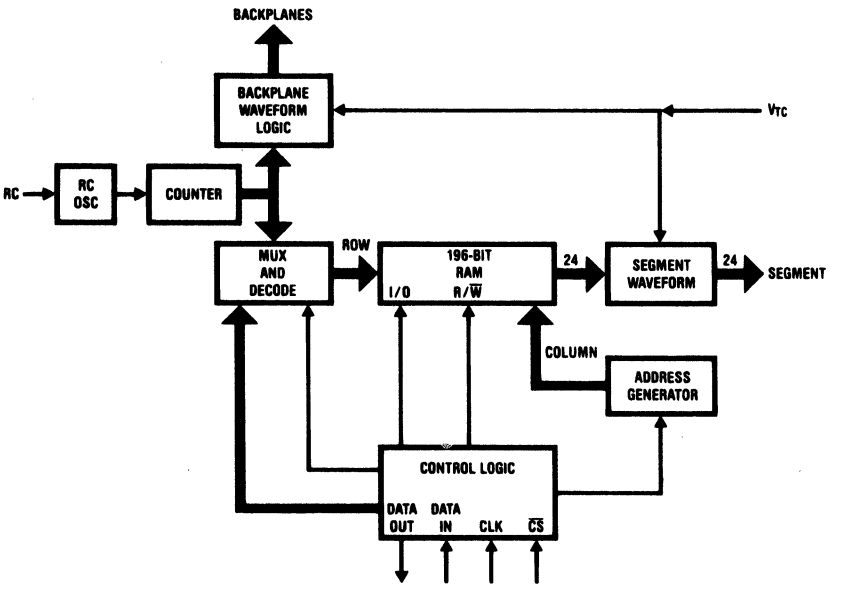
Features

- Drives up to 8 backplanes and 24 segment lines
- Stores data for display
- Cascadable
- Low power
- Fully static operation

Applications

- Dot matrix LCD driver
- Multiplexed 7-segment LCD driver
- Serial in/Serial out memory

Block Diagram



TL/F/6146–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin V_{SS} −0.3V to V_{SS} +18V

Operating Temperature Range 0°C to 70°C

Storage Temperature Range −65°C to +150°C

Power Dissipation at 25°C

Molded DIP Package, board mount 2.9W*

Molded DIP Package, socket mount 2.6W**

*Molded DIP Package, board mount, derate 23.3m W/°C above 25°C θ_{JA} = 43°C/W,

**Molded DIP Package, socket mount, derate 21.3m W/°C above 25°C θ_{JA} = 47°C/W,

Operating V_{DD} Range V_{SS} +7.0V to V_{SS} +18.0V

Lead Temperature (Soldering, 10 seconds) 300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Supply Current				0.3	mA
$V_{IN(1)}$	Logical "1" Input Voltage		0.45 V_{DD}		V_{DD} +0.3	V
$V_{IN(0)}$	Logical "0" Input Voltage		V_{SS}−0.3		1.0	V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{SINK} = 0.6 mA			0.4	V
$I_{OUT(1)}$	Logical "1" Output Leakage Current	V_{OUT} = V_{DD}	0		±10	μA
$I_{IN(1)}$	Logical "1" Input Leakage Current	V_{IN} = V_{DD}	0		1.0	μA
$I_{IN(0)}$	Logical "0" Input Leakage Current	V_{IN} = V_{SS}	−1.0		0	μA
V_{TC}	Input Voltage		4.5		V_{DD}+0.3	V
V_{TC}	Input Impedance		10		30	kΩ
Z_{OUT}	Output Impedance	Backplane and Segment Outputs			10	kΩ
Z_{OUT}	DC Offset Voltage	Between Any Backplane and Segment Output	0		±10	mV

AC Electrical Characteristics

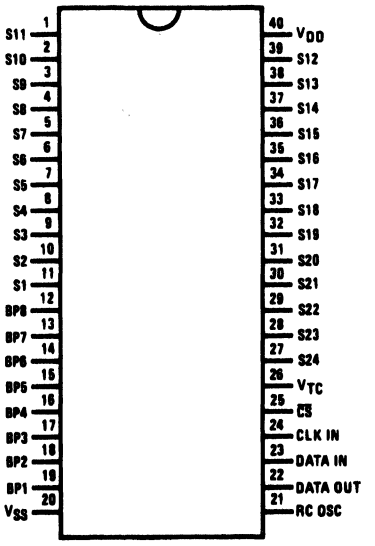
T_A and V_{DD} within operating range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator Frequency*		128η		400η	Hz
$f_{CLK\ IN}$	Clock Frequency		DC		100	kHz
t_{ON}	Clock Pulse Width		5.0			μs
t_{OFF}	Clock OFF Time		5.0			μs
t_S	Input Data Set-Up Time		2.0			μs
t_H	Input Data Hold Time		1.0			μs
t_{ACC}	Access Time		5.0			μs
t_r	Rise Time	Backplane, Segment Outputs C_L = 2000 pF			60	μs
t_f	Fall Time	Backplane, Segment Outputs C_L = 2000 pF			60	μs

* η is the number of backplanes programmed.

Connection Diagrams

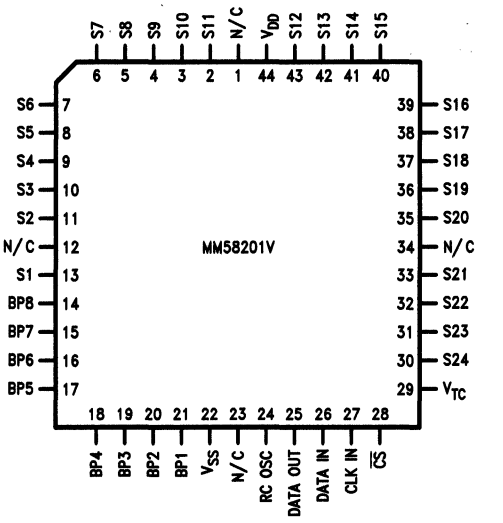
Dual-In-Line Package



TL/F/6146-2

Top View

Plastic Chip Carrier



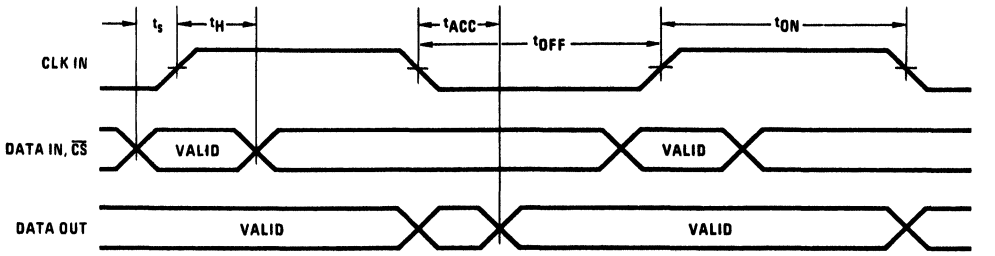
TL/F/6146-10

Top View

FIGURE 2

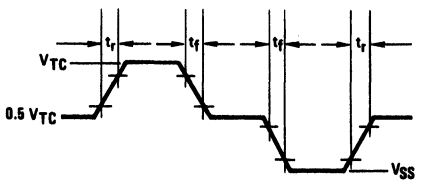
Order Number MM58201N or MM58201V
See NS Package Number N40A or V44A

Switching Time Waveforms



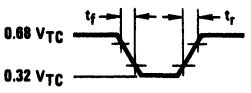
TL/F/6146-3

Backplane Output



TL/F/6146-4

Segment Output



TL/F/6146-5

Functional Description

A functional diagram of the MM58201 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

SERIAL INPUTS AND OUTPUTS

A negative-going edge on the $\overline{CS}$ input initiates a frame. The $\overline{CS}$ input must then stay low for at least one rising edge of CLK IN, and may not be pulsed low again for the next 31 clocks. At least one clock must occur while $\overline{CS}$ is high. If CLK IN is held at a logic "1", $\overline{CS}$ is disabled. This allows the signal that drives $\overline{CS}$ to be used for other purposes when the MM58201 is not being addressed.

CLK IN latches data from the DATA IN input on its rising edge. Data from the DATA OUT pin changes on the falling edge of CLK IN and is valid before the next rising edge.

The first five bits of data following $\overline{CS}$ are the address bits *(Figure 3)*. The address selects the column where the operation is to start. Bit 1 is the MSB and bit 5 is the LSB. The sixth bit is the read/write bit. A logic "1" specifies a read operation and a logic "0" specifies a write operation. The next 24 bits are the data bits. The first data bit corresponds to the BP1 row of the display, the second data bit to the BP2 row, and so on. After the eighth and sixteenth data bits, the column pointer is incremented. When starting address 10110 or 10111 is specified, the column pointer increments from 10111 to 00000.

During a read or write cycle, the LCD segment outputs do not reflect the data in the RAM. To avoid disrupting the pattern viewed on the display, the read or write cycle time should be kept short. Since the LCD turn-on time can be as little as 30 ms, a clock rate of at least 10 kHz would be required in order to address the entire contents of the RAM within that time interval. The formula below can be used to estimate the minimum clock rate:

$$f_{CLK\ IN} = \frac{30}{(t_{LCD} - 7t_s)}$$

where t_s is the processor's set-up time between each read or write cycle, and t_{LCD} is the minimum turn-on or turn-off time of the LCD as specified by the LCD manufacturer.

The DATA OUT output is an open drain N-channel device to V_{SS} *(Figure 4)*. With an external pull-up this configuration allows the controller to operate at a lower supply voltage, and also permits the DATA OUT output to be wired in parallel with the DATA OUT outputs from any other drivers in the system.

To program the number of backplanes being driven and the M/$\overline{S}$ bit, load address 11000, a write bit, three bits for the number of backplanes (Table I), and the M/$\overline{S}$ bit. The remaining 20 data bits will be ignored but it is necessary to provide 21 more clocks before initiating another frame.

TABLE I. Backplane Select

Number of Backplanes	B2	B1	B0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

RC OSC Pin

This oscillator generates the timing required for multiplexing the liquid crystal display. The oscillator operates at a frequency that is 4η times the refresh rate of the display, where η is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency must be:

$$128\eta \leq f_{OSC} \leq 400\eta$$

The frequency of oscillation is related to the external R and C components in the following way:

$$f_{OSC} = \frac{1}{1.25\,RC} \pm 30\%$$

The value used for the external resistor should be in the range from 10 kΩ to 1 MΩ.

The value used for the external capacitor should be less than 0.005 μF.

V_{TC} Pin

The V_{TC} pin is an analog input that controls the contrast of the segments on the LCD. If eight backplanes are being driven (η = 8), a voltage of typically 8V is required at 25°C. The voltage for optimum contrast will vary from display to display. It also has a significant negative temperature coefficient.

The voltage source on the V_{TC} input must be of relatively low impedance since the input impedance of V_{TC} ranges from 10 kΩ to 30 kΩ. A suitable circuit is shown in *Figure 5*.

In a standby mode, the V_{TC} input can be set to V_{SS}. This reduces the supply current to less than 300 μA per driver.

BACKPLANE AND SEGMENT OUTPUTS

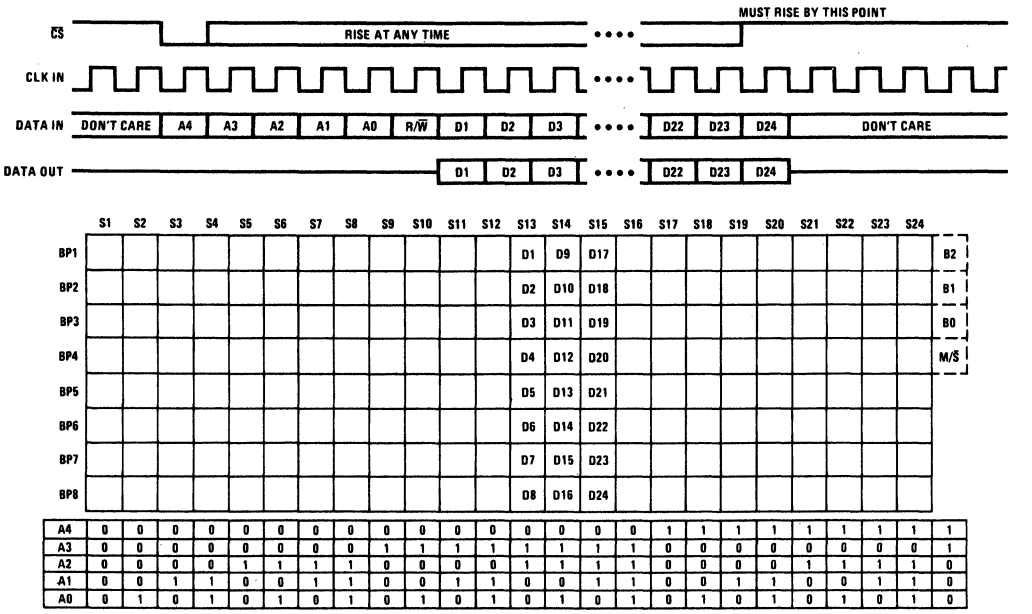
Connect the backplane and segment outputs directly to the LCD row and column lines. The outputs are designed to drive a display with a total ON capacitance of up to 2000 pF.

The output structure consists of transmission gates tapped off of a resistor string driven by V_{TC} *(Figure 6)*.

A critical factor in the lifetime of an LCD is the amount of DC offset between a backplane and segment signal. Typically, 50 mV of offset is acceptable. The MM58201 guarantees an offset of less than 10 mV.

The BP1 output is disabled when the M/$\overline{S}$ bit is set to zero. This allows the BP1 output from the master chip to be connected directly to it so that synchronizing signals can be generated. Synchronization occurs once each refresh cycle, so the cascaded chips are assured of remaining synchronized.

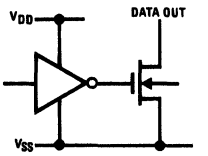
Functional Description (Continued)



TL/F/6146–6

Diagram above shows where data will appear on display if starting address 01100 is specified in data format.

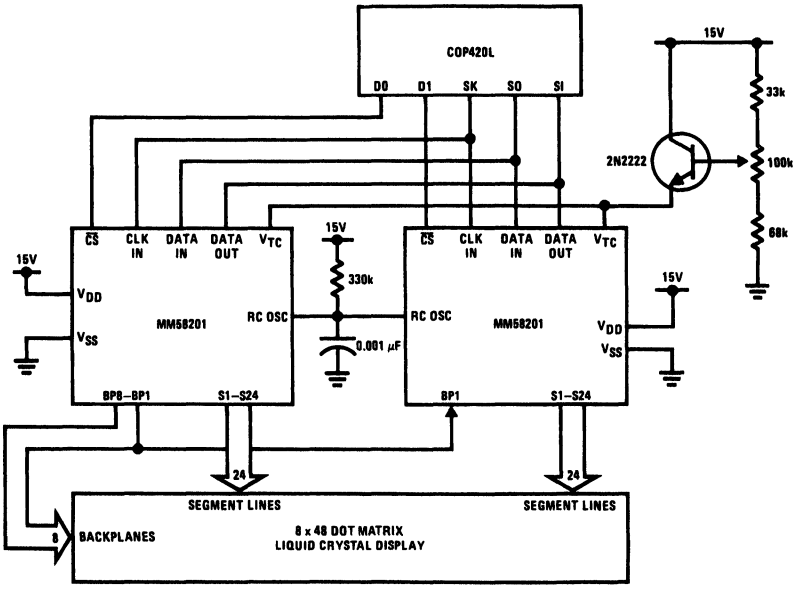
FIGURE 3. Data Format



TL/F/6146–7

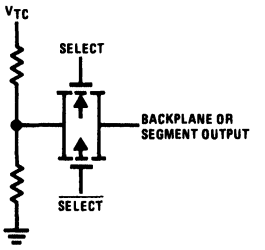
FIGURE 4. DATA OUT Structure

Functional Description (Continued)



TL/F/6146–8

FIGURE 5. Typical Application



TL/F/6146–9

FIGURE 6. Structure of LCD Outputs

National Semiconductor

MM58241 High Voltage Display Driver

General Description

The MM58241 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58241 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 32-digit alphanumeric or dot matrix display).

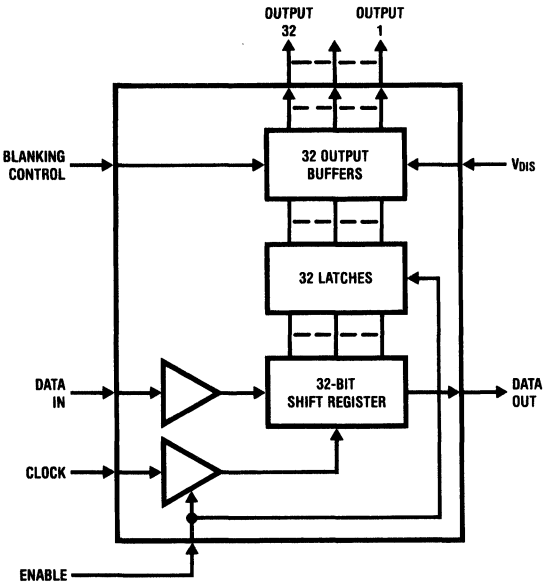
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



TL/F/5600–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 62.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at +25°C	
Molded DIP Package, Board Mount	2.28W*
Molded DIP Package, Socket Mount	2.05W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, θ_{JA} = 46°C/W, Derate 21.7 mW/°C above +25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 51°C/W, Derate 19.6 mW/°C above +25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, V_{SS} = 0V,				
I_{DD}		V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −55V All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	I_{OUT} = 400 μA			0.4	V
V_{OH}	Logic '1'	I_{OUT} = −10 μA	$V_{DD} - 0.5$			V
V_{OH}	Logic '1'	I_{OUT} = −500 μA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	V_{DD} = 5.5V, V_{SS} = 0V				
R_{OFF}	Output Off *(Figure 3a)*	V_{DIS} = −25V	60		400	kΩ
		V_{DIS} = −40V	70		550	kΩ
		V_{DIS} = −55V	80		650	kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −25V		3.0	4.0	kΩ
		V_{DIS} = −40V		2.6	3.7	kΩ
		V_{DIS} = −55V		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, $-55V \le V_{DIS} \le -25V$	V_{DIS}		$V_{DIS} + 4$	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

4

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input					
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output	$C_L = 50$ pF				
	CLOCK Low to Data Out				500	ns
t_{CDO}	Time					

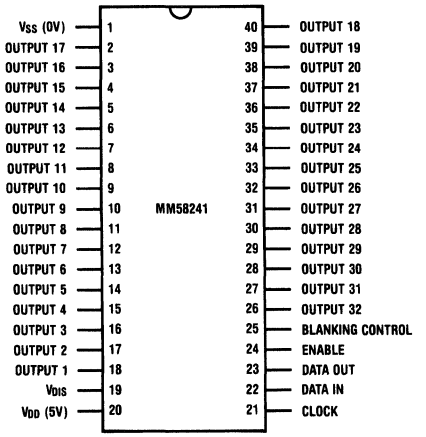
Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

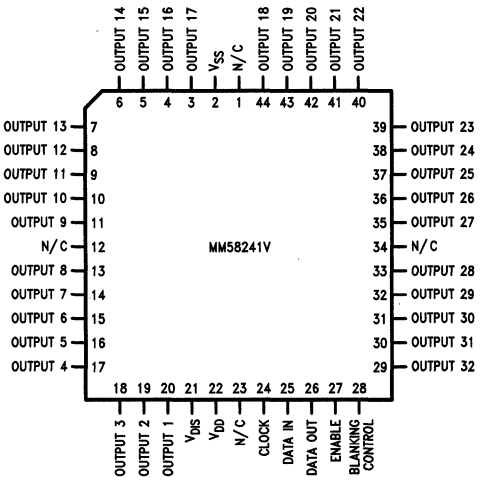
Dual-In-Line Package



TL/F/5600–2

Top View

Plastic Chip Carrier



TL/F/5600–8

Top View

FIGURE 2

Order Number MM58241N or MM58241V
See NS Package Number N40A or V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58421 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58241 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58241 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following ENABLE high. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58241, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

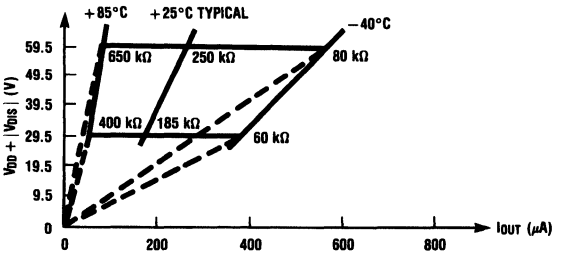
Functional Description (Continued)

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58241.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 32 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

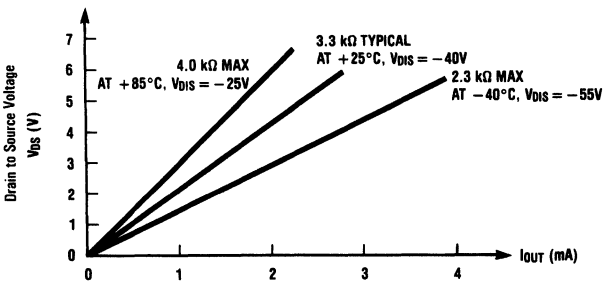
In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58241, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58241 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vaccum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.



TL/F/5600–3

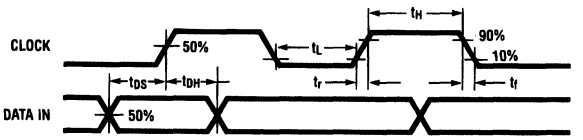
FIGURE 3a. Output Impedance Off



TL/F/5600–4

FIGURE 3b. Output Impedance On

Timing Diagrams

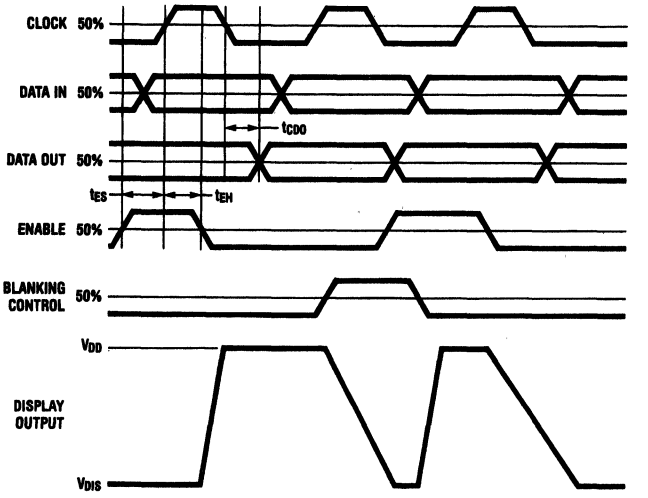


TL/F/5600–5

For the purposes of AC measurements, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

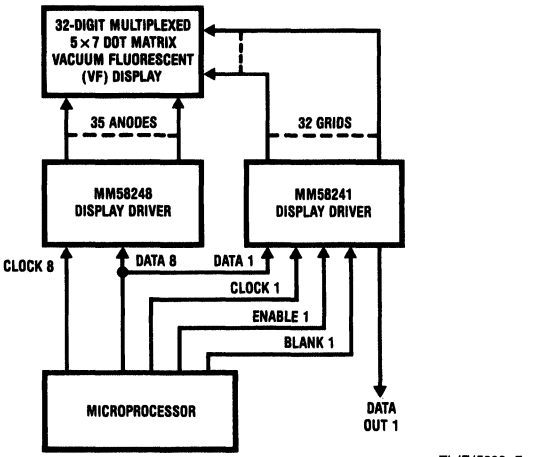
Timing Diagrams (Continued)



TL/F/5600–6

FIGURE 5. MM58241 Timings (Data Format)

Typical Application



TL/F/5600–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58242 High Voltage Display Driver

General Description

The MM58242 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58242 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

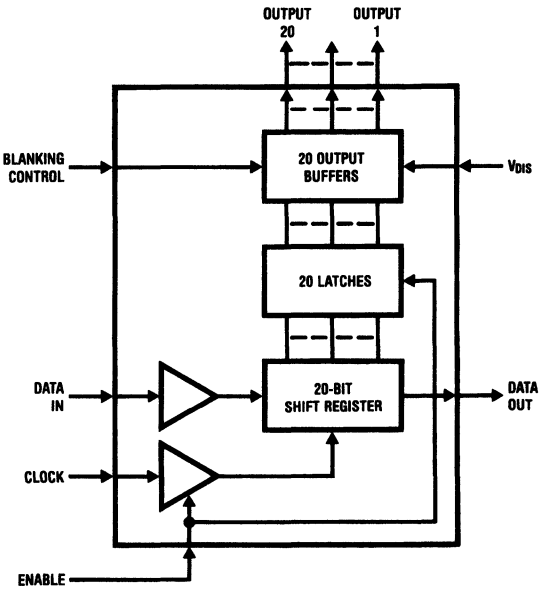
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



TL/F/7924–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} −0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} −62.5V
$V_{DD} + \lvert V_{DIS} \rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at +25°C	
Molded DIP Package, Board Mount	2.03W*
Molded DIP Package, Socket Mount	1.83W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, θ_{JA} = 52°C/W, Derate 19.2 mW/°C above +25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 58°C/W, Derate 17.2 mW/°C above +25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	V_{IN} = V_{SS} or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = 55V All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	I_{OUT} = 400 μA			0.4	V
V_{OH}	Logic '1'	I_{OUT} = −10 μA	V_{DD}−0.5			V
V_{OH}	Logic '1'	I_{OUT} = −500 μA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	V_{DD} = 5.5V, V_{SS} = 0V				
R_{OFF}	Output Off *(Figure 3a)*	V_{DIS} = −25V	60		400	kΩ
		V_{DIS} = −40V	70		550	kΩ
		V_{DIS} = −55V	80		650	kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −25V		3.0	4.0	kΩ
		V_{DIS} = 40V		2.6	3.7	kΩ
		V_{DIS} = −55V		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −55V ≤ V_{DIS} ≤ −25V	V_{DIS}		V_{DIS}+4	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 3 and 4)				
Frequency, f_C				800	kHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input	(Note 2)				
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output	$C_L = 50$ pF				
CLOCK Low to Data Out Time, t_{CDO}				500	ns

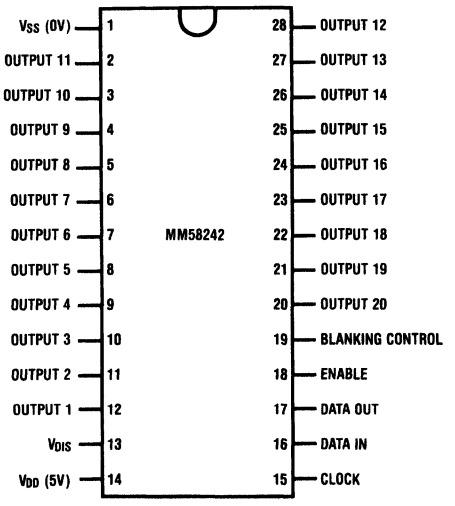
Note 2: For timimg purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package

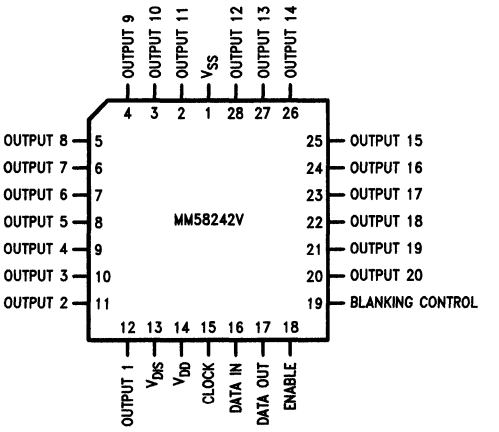


TL/F/7924-2

Top View
FIGURE 2

Order Number MM58242N
See NS Package Number N28B

Plastic Chip Carrier



TL/F/7924-8

Top View
Order Number MM58242V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58242 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58242 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58242 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

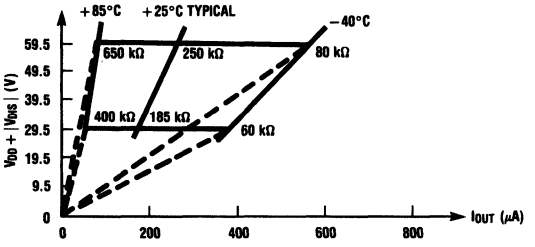
A significant reduction in discrete board components can be achieved by use of the MM58242, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied, However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58242.

To clear (reset) the display driver at "power on" or any time, the following flushing routine may be used. With the enable signal high, clock in 20 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

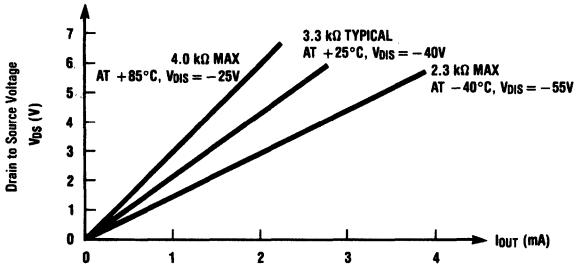
In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58242 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58242 is used to provide the grid drive for a 40-digit 2 line 5 × 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.



TL/F/7924–3

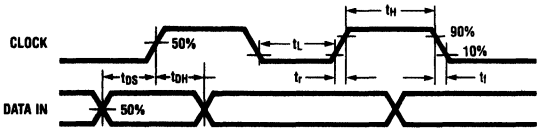
FIGURE 3a. Output Impedance Off



TL/F/7924–4

FIGURE 3b. Output Impedance On

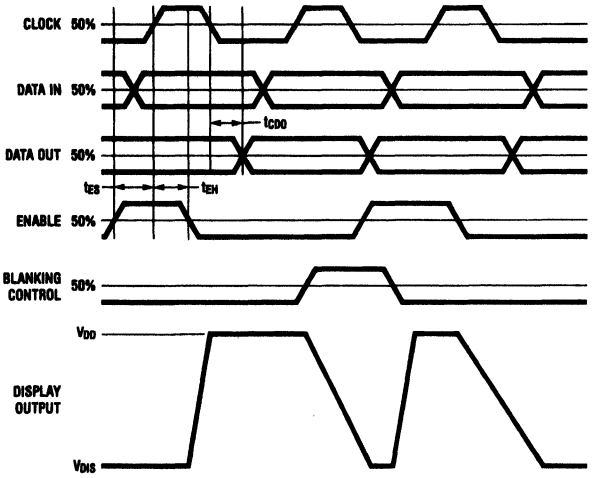
Timing Diagrams



TL/F/7924–5

For the purposes of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V.

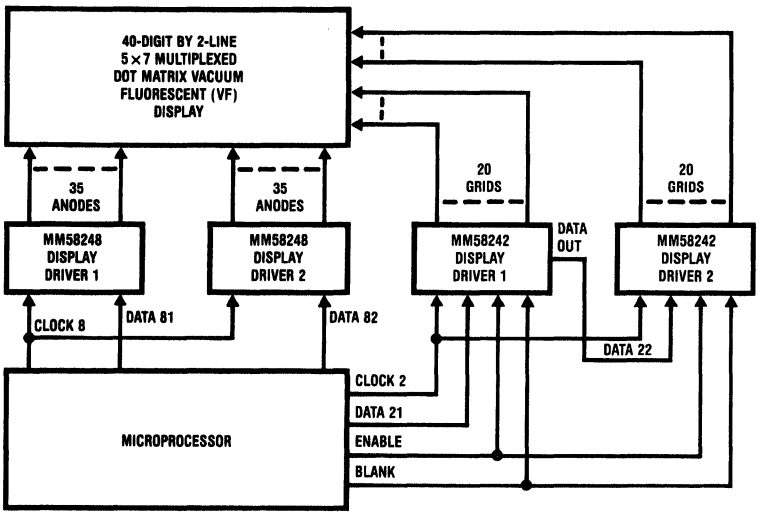
FIGURE 4. Clock and Data Timings



TL/F/7924–6

FIGURE 5. MM58242 Timings (Data Format)

Typical Application



TL/F/7924–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58248 High Voltage Display Driver

General Description

The MM58248 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58248 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 5 x 7 dot matrix display).

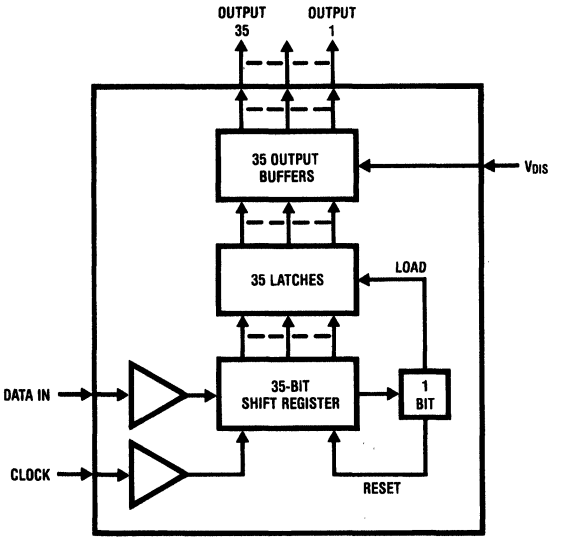
Applications

- COPS™ or microprocessor-driven display
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

Block Diagram



TL/F/5599–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 62.5V
V_{DD} + $\|V_{DIS}\|$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at +25°C	
Molded DIP Package, Board Mount	2.28W*
Molded DIP Package, Socket Mount	2.05W**

*Molded DIP Package, Board Mount θ_{JA} = 46°C/W, Derate 21.7 mW/°C above +25°C.

**Molded DIP Package, Socket Mount, θ_{JA} = 51°C/W, Derate 19.6 mW/°C above +25°C.

Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	V_{IN} = V_{SS} or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −55V, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK Logic '0'				0.8	V
V_{IH}	Input Logic Levels DATA IN, CLOCK Logic '1'	(Note 1)	2.4			V
I_{IN}	Input Currents, DATA IN, CLOCK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance, DATA IN, CLOCK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	V_{DD} = 5.5V, V_{SS} = 0V V_{DIS} = −25V V_{DIS} = −40V V_{DIS} = −55V	 60 70 80		 400 550 650	 kΩ kΩ kΩ
R_{ON}	Display Output Impedances Output on *(Figure 3b)*	V_{DD} = 5.5V, V_{SS} = 0V V_{DIS} = −25V V_{DIS} = −40V V_{DIS} = −55V		 3.0 2.6 2.3	 4.0 3.7 3.4	 kΩ kΩ kΩ
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −55V ≤ V_{DIS} ≤ −25V	V_{DIS}		V_{DIS} + 4	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristics T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V

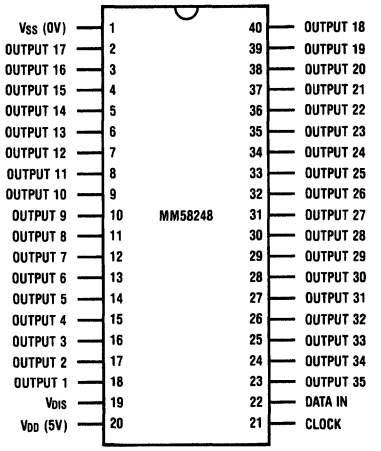
Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 2, 3)			1.0	MHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Setup Time	C_L = 50 pF	100			ns
t_{DH}	Data Input Hold Time		100			ns

Note 2: AC input waveform specification for test purposes: t_r, t_f ≤ 20 ns, f = 1 MHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package

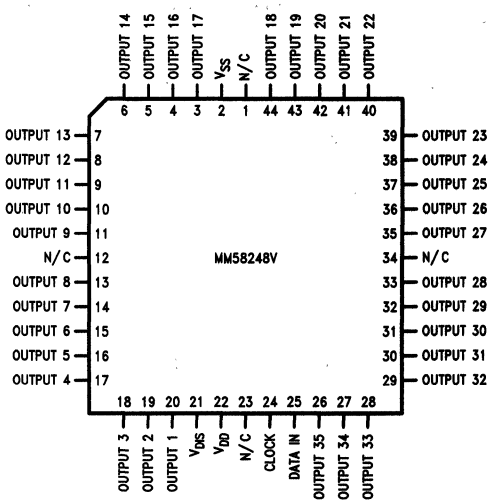


TL/F/5599–2

Top View

Order Number MM58248N
See NS Package Number N40A

Plastic Chip Carrier



TL/F/5599–8

Top View

Order Number MM58248V
See NS Package Number V44A

FIGURE 2

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58248 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58248 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58248 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following the start bit. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

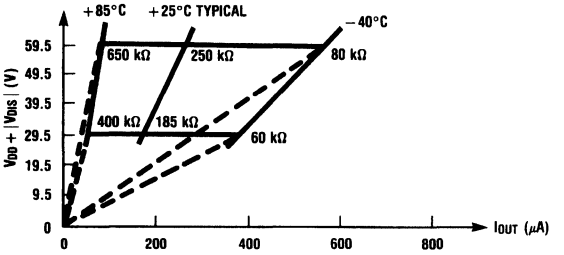
A significant reduction in discrete board components can be achieved by the use of the MM58248, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58248.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'–'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58248, or the shift register will not clear. To clear (reset) the display driver at 'power on' or any time, the following flushing routine may be used. Clock in 36 "zeroes", followed by a "one" (start bit), followed by 35 "zeroes". This procedure will completely blank the display. It is recommended to clear the driver at power on.

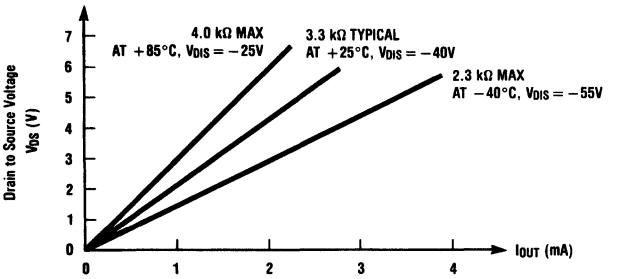
Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58248 is used to provide the anode drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58241, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

Functional Description (Continued)



TL/F/5599–3

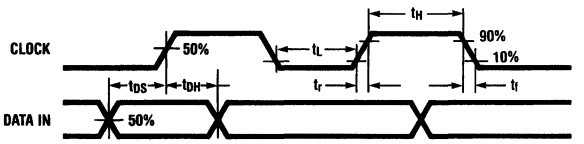
FIGURE 3a. Output Impedance Off



TL/F/5599–4

FIGURE 3b. Output Impedance On

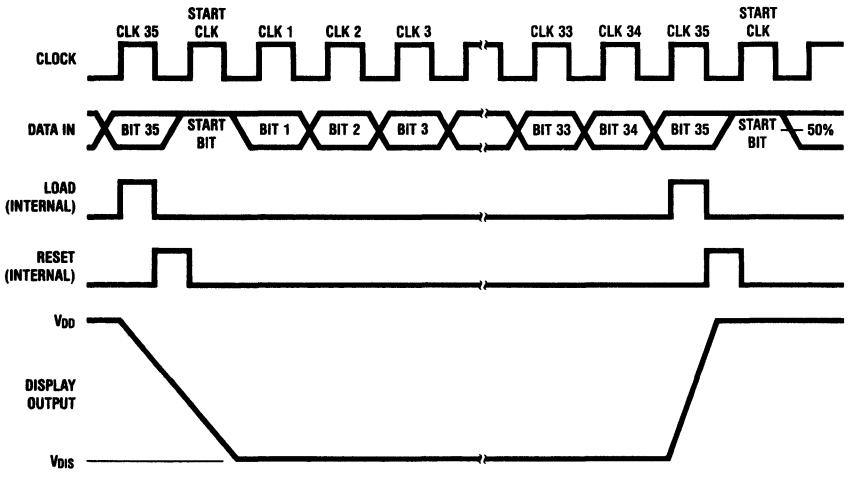
Timing Diagrams



TL/F/5599–5

For the purposes of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V.

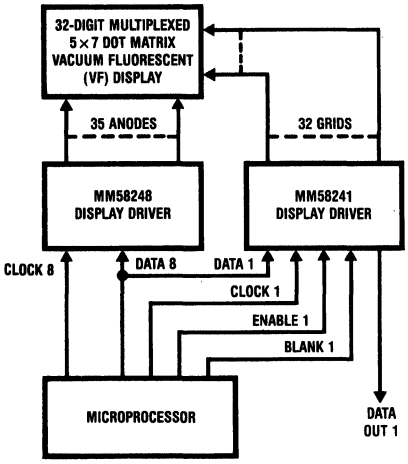
FIGURE 4. Clock and Data Timings



TL/F/5599–6

FIGURE 5. MM58248 Timings (Data Format)

Typical Applications



TL/F/5599–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display).

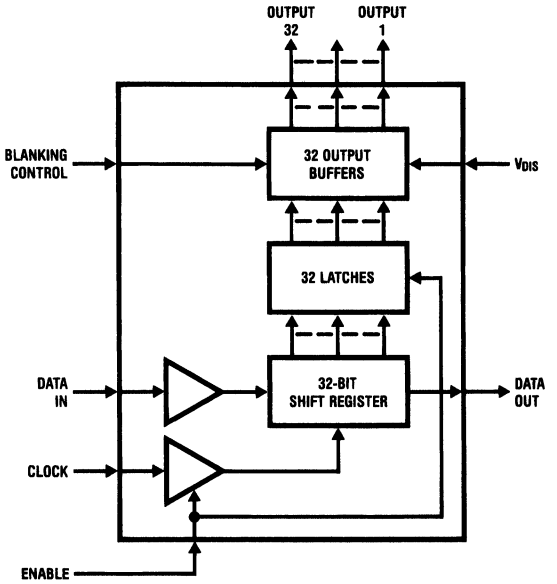
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



TL/F/5603–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 36.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.28W*
Molded DIP Package, Socket Mount	2.05W**
*Molded DIP Package, Board Mount, Derate 21.7 mW°C Above 25°C	θ_{JA} = 46°C/W
**Molded DIP Package, Socket Mount, Derate 19.6 mW/°C Above 25°C	θ_{JA} = 51°C/W
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −30V, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '0'				0.8	V
V_{IH}	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK Logic '1'	(Note 1)	2.4			V
V_{OH}	Data Output Logic Levels Logic '0'	I_{OUT} = 400 μA			0.4	V
V_{OH}	Data Output Logic Levels Logic '1'	I_{OUT} = −10 μA	$V_{DD} - 0.5$			V
V_{OH}	Data Output Logic Levels Logic '1'	I_{OUT} = −500 μA	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	V_{DD} = 5.5V, V_{SS} = 0V V_{DIS} = −10V V_{DIS} = −20V V_{DIS} = −30V	 55 60 65		 250 300 400	 kΩ kΩ kΩ
R_{ON}	Display Output Impedances Output On *(Figure 3b)*	 V_{DIS} = −10V V_{DIS} = −20V V_{DIS} = −30V		 700 600 500	 800 750 680	 Ω Ω Ω
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, $-30V \le V_{DIS} \le -10V$	V_{DIS}		V_{DIS} + 2	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 3, 4)			800	kHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Setup Time		100			ns
t_{DH}	Data Input Hold Time		100			ns
t_{ES}	Enable Input Setup Time		100			ns
t_{EH}	Enable Input Hold Time		100			ns
t_{CDO}	Data Output Clock Low to Data Out Time	$C_L = 50$ pF			500	ns

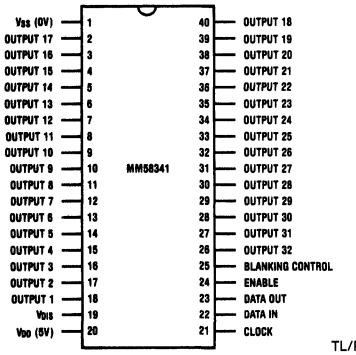
Note 2: Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package

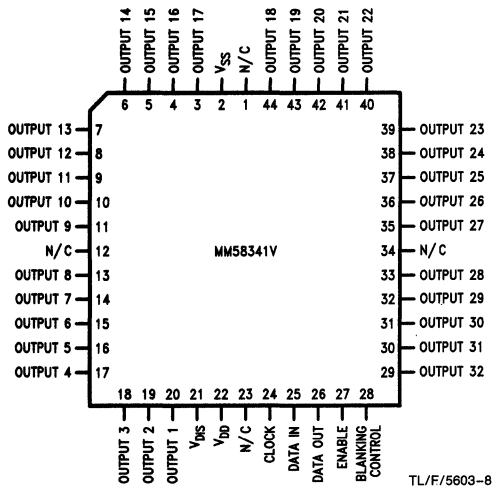


TL/F/5603-2

Top View

Order Number MM58341N
See NS Package Number N40A

Plastic Chip Carrier



TL/F/5603-8

Top View

Order Number MM58341V
See NS Package Number V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58341 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58341 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58341 device, where output 1 (pin 18) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58341, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

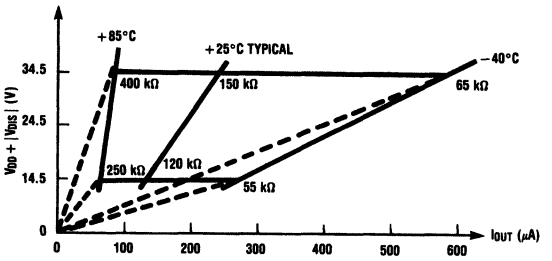
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58341.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 32 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58341, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

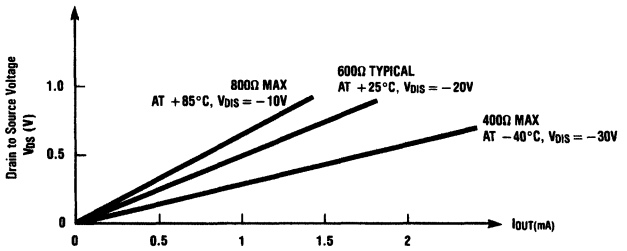
Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58341 is used to provide the grid drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

Functional Decription (Continued)



TL/F/5603–3

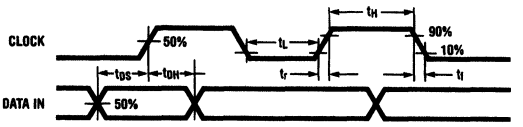
FIGURE 3a. Output Impedance Off



TL/F/5603–4

FIGURE 3b. Output Impedance On

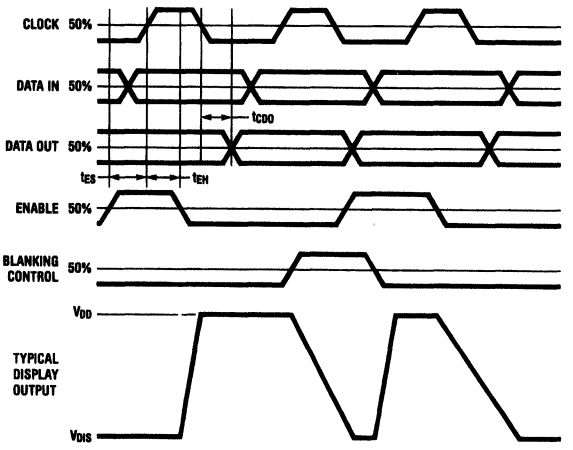
Timing Diagrams



TL/F/5603–5

For the purposes of AC measurements, V_{IH} = 2.4V, V_{IL} = 0.8V.

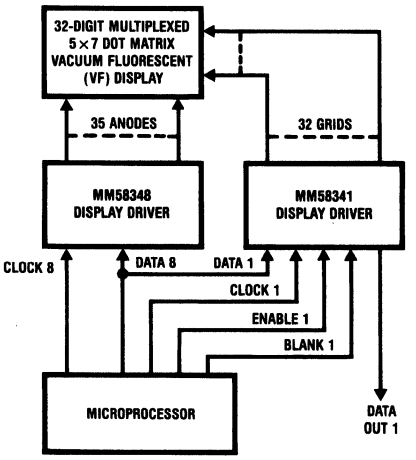
FIGURE 4. Clock and Data Timings



TL/F/5603–6

FIGURE 5. MM58341 Timings (Data Format)

Typical Application



TL/F/5603–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58342 High Voltage Display Driver

General Description

The MM58342 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58342 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

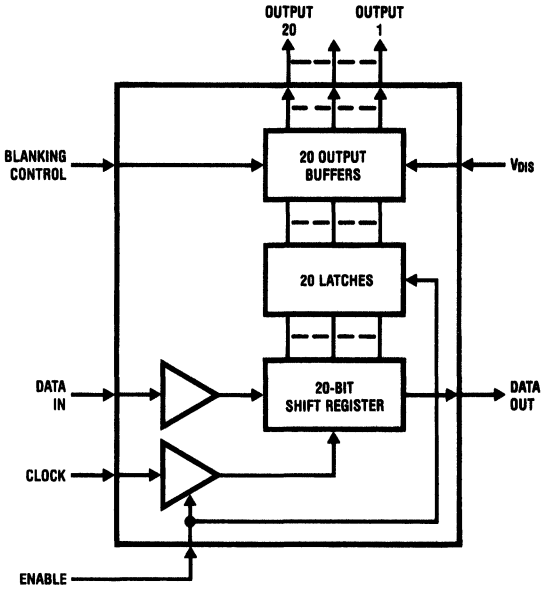
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram



TL/F/7925–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 36.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.03W*
Molded DIP Package, Socket Mount	1.83W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, $\theta_{JA} = 52°C/W$, derate 19.2 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, $\theta_{JA} = 58°C/W$, derate 17.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS} = 0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN} = V_{SS}$ or V_{DD}, $V_{SS} = 0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = -30V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT} = 400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT} = -10\ \mu A$	$V_{DD} - 0.5$			V
V_{OH}	Logic '1'	$I_{OUT} = -500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN} = 0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD} = 5.5V$, $V_{SS} = 0V$				
R_{OFF}	Output Off *(Figure 3a)*	$V_{DIS} = -10V$	55		250	kΩ
		$V_{DIS} = -20V$	60		300	kΩ
		$V_{DIS} = -30V$	65		400	kΩ
R_{ON}	Output On *(Figure 3b)*	$V_{DIS} = -10V$		700	800	Ω
		$V_{DIS} = -20V$		600	750	Ω
		$V_{DIS} = -30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V$, I_{OUT} = Open Circuit, $-30V \le V_{DIS} \le -10V$	V_{DIS}		$V_{DIS} + 2$	V

Note 1: 74LSTTL $V_{OH} = 2.7V$ @ $I_{OUT} = -400\ \mu A$, TTL $V_{OH} = 2.4V$ @ $I_{OUT} = -400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input	(Note 2)				
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output CLOCK Low to Data Out Time	$C_L = 50$ pF			500	ns
t_{CDO}						

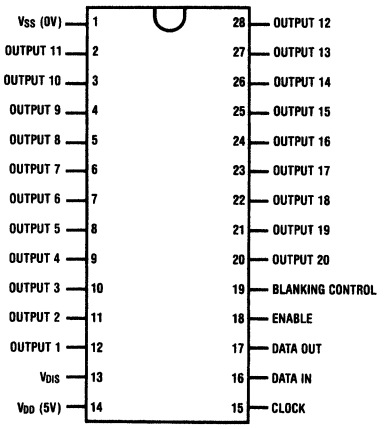
Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package



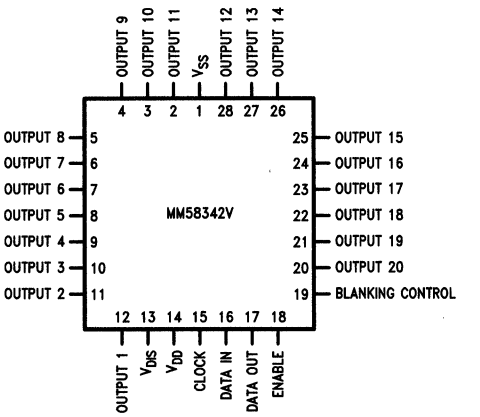
TL/F/7925-2

Top View

FIGURE 2

Order Number MM58342N
See NS Package Number N28B

Plastic Chip Carrier



TL/F/7925-8

Top View
Order Number MM58342V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58342 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58342 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58342 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58342, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a*

Functional Description (Continued)

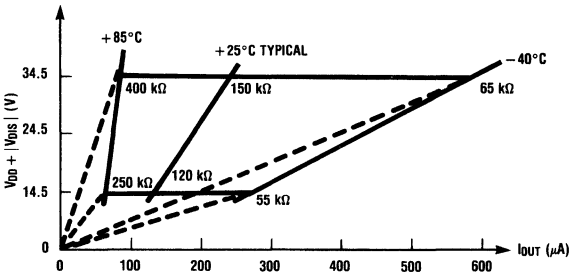
and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58342.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 20 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

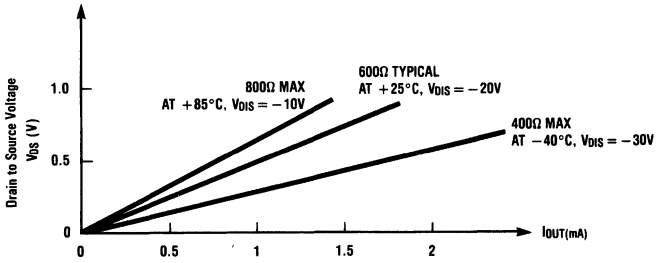
In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58342 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58342 is used to provide the grid drive for a 40-digit 2 line 5 x 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.



TL/F/7925–3

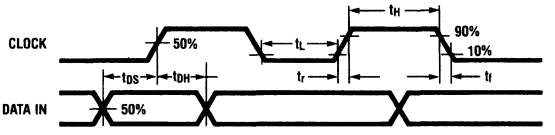
FIGURE 3a. Output Impedance Off



TL/F/7925–4

FIGURE 3b. Output Impedance On

Timing Diagrams

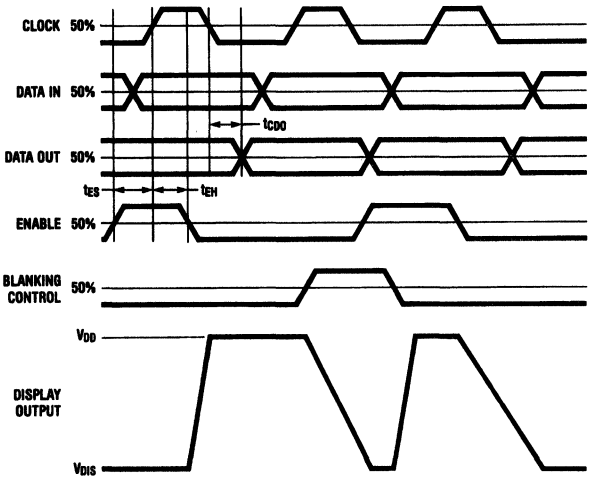


TL/F/7925–5

For the purposes of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

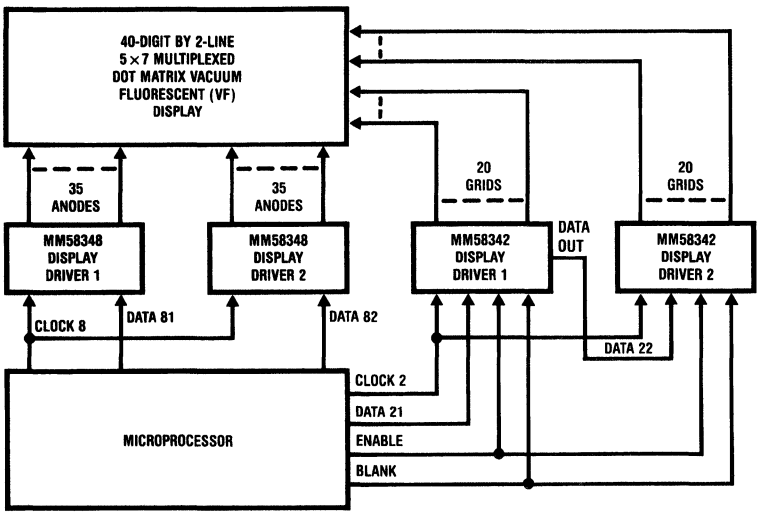
Timing Diagrams (Continued)



TL/F/7925–6

FIGURE 5. Timings (Data Format)

Typical Application



TL/F/7925–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58348 High Voltage Display Driver

General Description

The MM58348 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58348 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 5 x 7 dot matrix display).

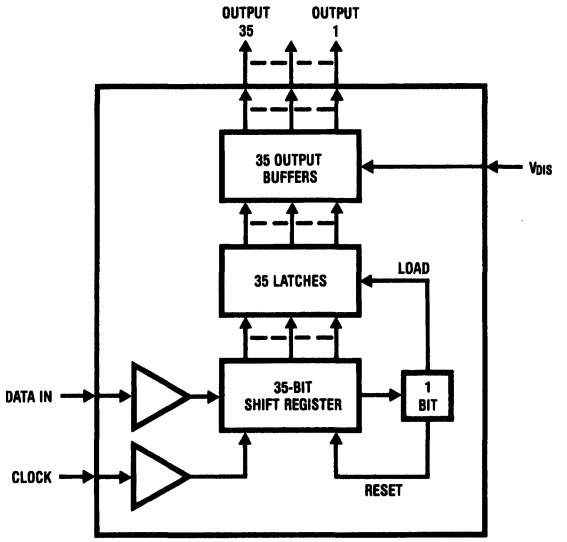
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

Block Diagram



TL/F/5601–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at Any Display Pin	V_{DD} to V_{DD} − 36.5V
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to + 150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.28W*
Molded DIP Package, Socket Mount	2.05W**
*Molded DIP Package, Board Mount, Derate 21.7 mW°C Above 25°C	θ_{JA} = 46°C/W
**Molded DIP Package, Socket Mount, Derate 19.6 mW/°C Above 25°C	θ_{JA} = 51°C/W
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) V_{SS} = 0V	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V, V_{SS} = 0V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Currents	$V_{IN} = V_{SS}$ or V_{DD}, V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} Disconnected			150	μA
I_{DIS}		V_{DD} = 5.5V, V_{SS} = 0V, V_{DIS} = −30V, All Outputs Low			10	mA
V_{IL}	Input Logic Levels DATA IN, CLOCK Logic '0'				0.8	V
V_{IH}	Logic '1'		2.4			V
I_{IN}	Input Currents DATA IN, CLOCK	V_{IN} = 0V or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK				15	pF
R_{OFF}	Display Output Impedances Output Off *(Figure 3a)*	V_{DD} = 5.5V, V_{SS} = 0V				
		V_{DIS} = −10V	55		250	kΩ
		V_{DIS} = −20V	60		300	kΩ
		V_{DIS} = −30V	65		400	kΩ
R_{ON}	Output On *(Figure 3b)*	V_{DIS} = −10V		700	800	Ω
		V_{DIS} = −20V		600	750	Ω
		V_{DIS} = −30V		500	680	Ω
V_{DOL}	Display Output Low Voltage	V_{DD} = 5.5V, I_{OUT} = Open Circuit, −30V ≤ V_{DIS} ≤ −10V	V_{DIS}		V_{DIS} + 2	V

Note 1: 74LSTTL V_{OH} = 2.7V @ I_{OUT} = −400 μA, TTL V_{OH} = 2.4V @ I_{OUT} = −400 μA.

AC Electrical Characteristic T_A = −40°C to +85°C, V_{DD} = 5V ±0.5V

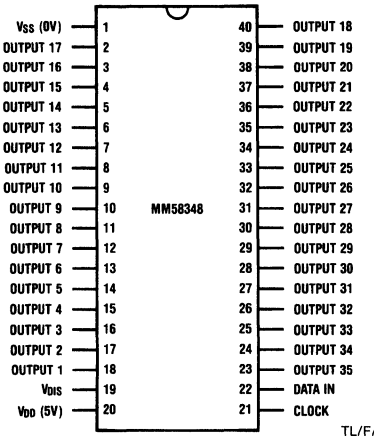
Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	*(Notes 2 and 3)*			1.0	MHz
t_H	Clock Input High Time		300			ns
t_L	Clock Input Low Time		300			ns
t_{DS}	Data Input Set-Up Time		100			ns
t_{DH}	Data Input Hold Time		100			ns

Note 2: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 1 MHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package



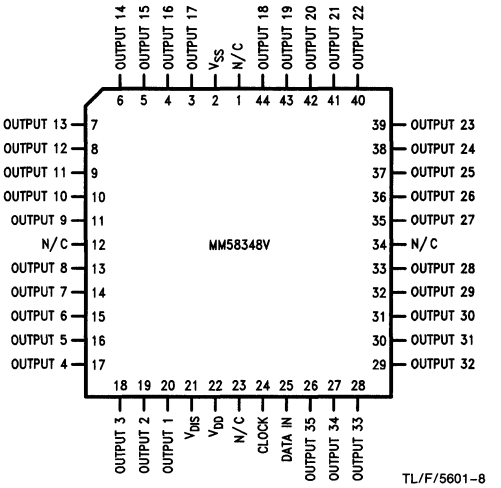
TL/F/5601–2

Top View

FIGURE 2

Order Number MM58348N
See NS Package Number N40A

Plastic Chip Carrier



TL/F/5601–8

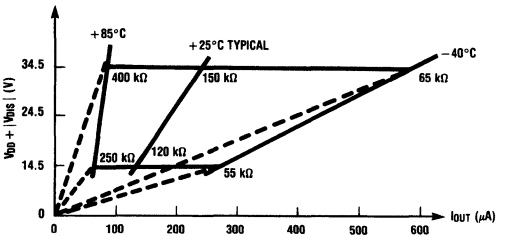
Top View
Order Number MM58348V
See NS Package Number V44A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58348 uses two signals, DATA IN and CLOCK, with a format of a leading "1" followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58348 is shown in *Figure 1.*

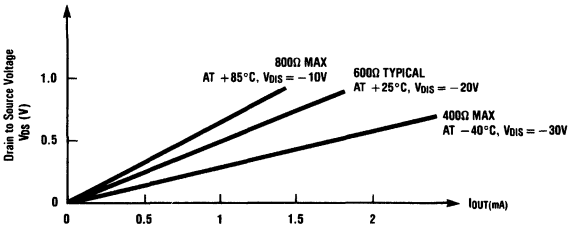
Figure 2 shows the pinout of the MM58348 device, where output 1 (pin 18) is equivalent to bit 1, (i.e., the first bit of data to be loaded into the shift register following the start bit). A logic "1" at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58348, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figure 3a* and *3b* show that this output impedance will remain constant for a fixed value of display voltage.



TL/F/5601–3

FIGURE 3a. Output Impedance Off



TL/F/5601–4

FIGURE 3b. Output Impedance On

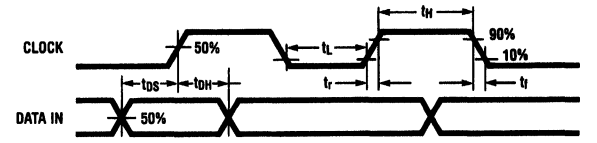
Functional Description (Continued)

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58348.

In *Figure 5,* a start bit of logic "1" precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a "0"–"1" transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed to clear (reset) the display driver at "power on" or any time, the following flushing routine may be used. Clock in 36 "zeroes", followed by a "one" (start bit), followed by 35 "zeroes". This procedure will completely blank the display. It is recommended to clear the driver at power on.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58348 is used to provide the anode drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58341, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

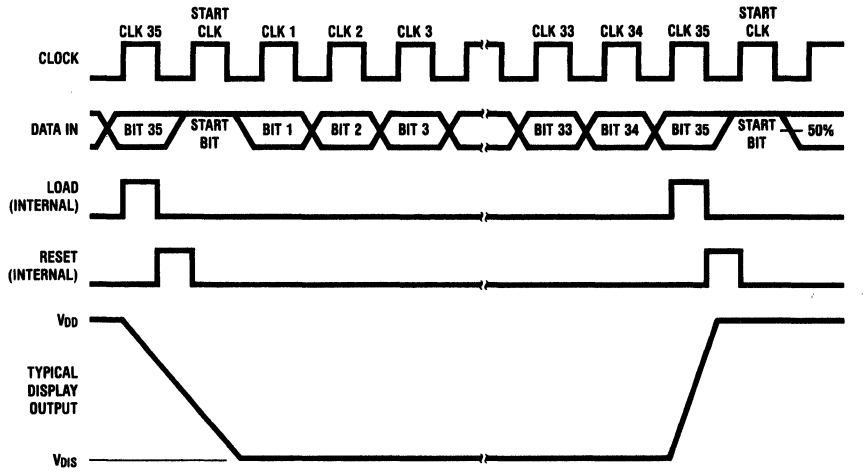
Timing Diagrams



TL/F/5601–5

For the purpose of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V

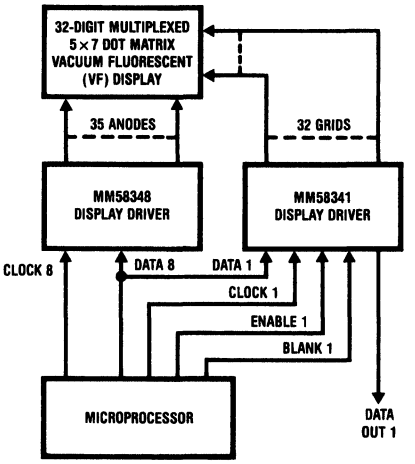
FIGURE 4. Clock and Data Timings



TL/F/5601–6

FIGURE 5. MM58348 Timings (Data Format)

Typical Application



TL/F/5601–7

FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

LM3909 LED Flasher/Oscillator

General Description

The LM3909 is a monolithic oscillator specifically designed to flash Light Emitting Diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as an LED flasher.

Packaged in an 8-lead plastic mini-DIP, the LM3909 will operate over the extended consumer temperature range of −25°C to +70°C. It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor. As shown in the first two application circuits, the timing resistors supplied are optimized for nominal flashing rates and minimum power drain at 1.5V and 3V.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example −20% to +100%.

Features

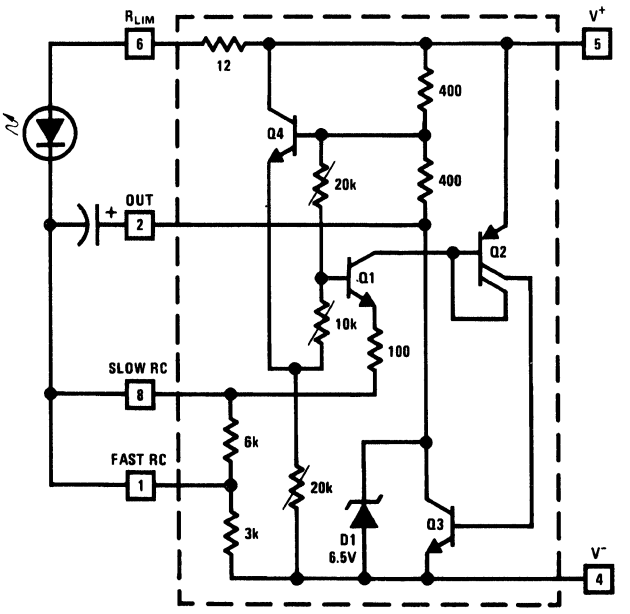
- Operation over one year from one C size flashlight cell
- Bright, high current LED pulse
- Minimum external parts
- Low cost
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker
- Wide temperature range

Applications

- Finding flashlights in the dark, or locating boat mooring floats
- Sales and advertising gimmicks
- Emergency locators, for instance on fire extinguishers
- Toys and novelties
- Electronic applications such as trigger and sawtooth generators
- Siren for toy fire engine, (combined oscillator, speaker driver)
- Warning indicators powered by 1.4V to 200V

Schematic Diagram

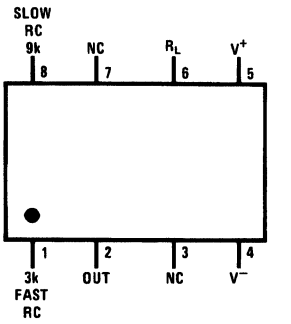
Typical 1.5V Flasher



TL/H/7969–1

Connection Diagram

Dual-In-Line Package



TL/H/7969–2

Top View

Order Number LM3909N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

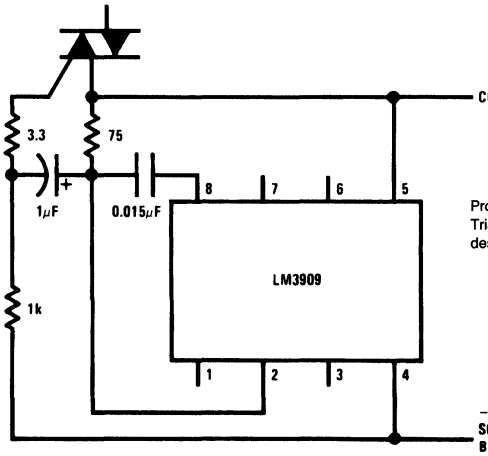
Power Dissipation	500 mW
V^+ Voltage	6.4V
Operating Temperature Range	−25°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

Parameter	Conditions (Applications Note 3)	Min	Typ	Max	Units
Supply Voltage	(In Oscillation)	1.15		6.0	V
Operating Current			0.55	0.75	mA
Flash Frequency	300 μF, 5% Capacitor	0.65	1.0	1.3	Hz
High Flash Frequency	0.30 μF, 5% Capacitor		1.1		kHz
Compatible LED Forward Drop	1 mA Forward Current	1.35		2.1	V
Peak LED Current	350 μF Capacitor		45		mA
Pulse Width	350 μF Capacitors at ½ Amplitude		6.0		ms

Typical Applications (See applications notes on following page)

Triac Trigger

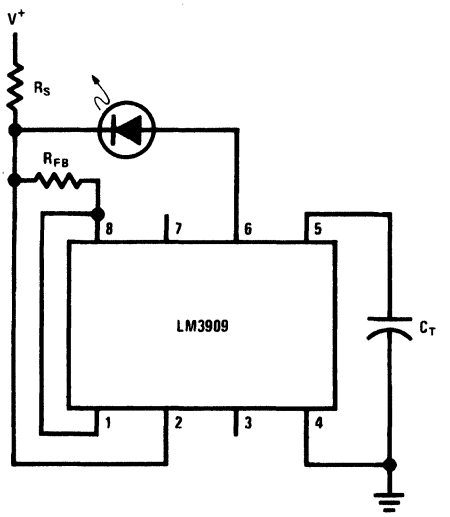


Provides 40 mA. 10 μs pulses at about 8 kHz. Triac gate may be pulse transformer isolated if desired.

TL/H/7969–3

Typical Applications (Continued)(See applications notes below)

Warning Flasher High Voltage Powered

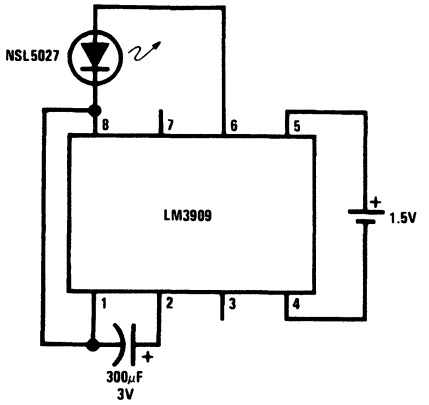


TL/H/7969–4

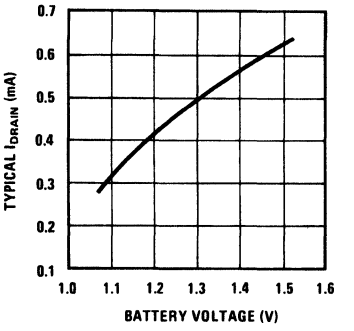
Typical Operating Conditions

V^+	Nominal Flash Hz	C_T	R_S	R_{FB}	V^+_{RANGE}
6V	2	400 μF	1k	1.5k	5V–25V
15V	2	180 μF	3.9k	1k	13V–50V
100V	1.7	180 μF	43k 1W	1k	85V–200V

1.5V Flasher



TL/H/7969–5



TL/H/7969–6

Note: Nominal flash rate: 1 Hz.

Estimated Battery Life (Continuous 1.5V Flasher Operation)

Size Cell	Type	
	Standard	Alkaline
AA	3 months	6 months
C	7 months	15 months
D	1.3 years	2.6 years

Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended for any application of five months or more. Nickel Cadmium cells are not recommended.

APPLICATIONS NOTES

Note 1: All capacitors shown are electrolytic unless marked otherwise.

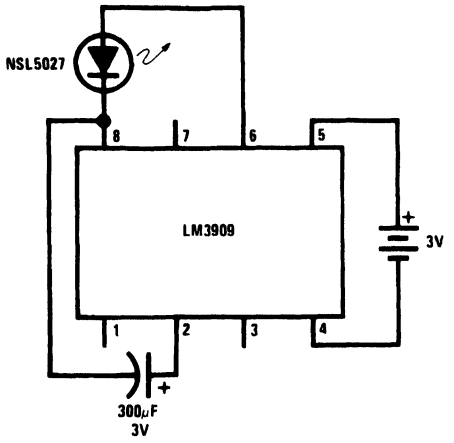
Note 2: Flash rates and frequencies assume a ±5% capacitor tolerance. Electrolytics may vary −20% to +100% of their stated value.

Note 3: Unless noted, measurements above are made with a 1.4V supply, a 25°C ambient temperature, and an LED with a forward drop of 1.5V to 1.7V at 1 mA forward current.

Note 4: Occasionally a flasher circuit will fail to oscillate due to an LED defect that may be missed because it only reduces light output 10% or so. Such LEDs can be identified by a large increase in conduction between 0.9V and 1.2V.

Typical Applications (Continued) (See applications notes on previous page)

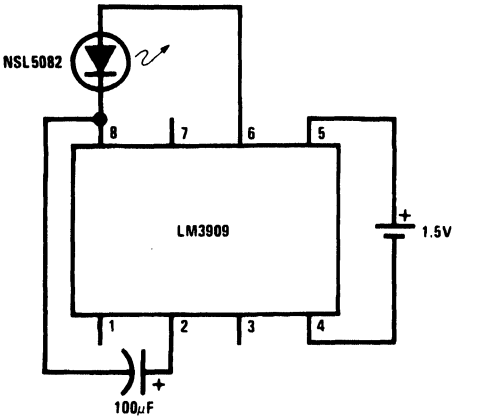
3V Flasher



TL/H/7969-7

Note: Nominal flash rate: 1 Hz. Average I_{DRAIN} = 0.77 mA.

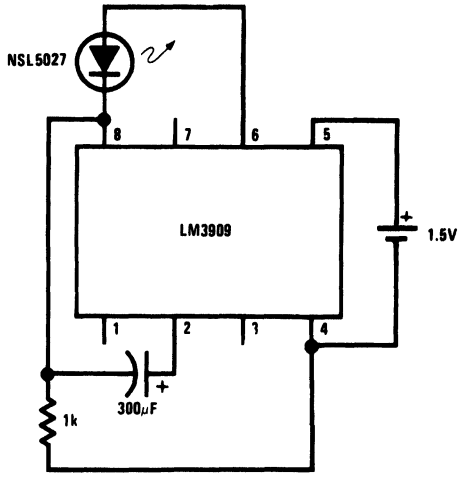
Minimum Power at 1.5V



TL/H/7969-8

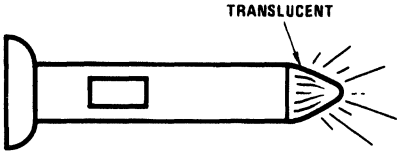
Note: Nominal flash rate: 1.1 Hz. Average I_{DRAIN} = 0.32 mA.

Fast Blinker



TL/H/7969-9

Note: Nominal flash rate: 2.6 Hz. Average I_{DRAIN} = 1.2 mA.

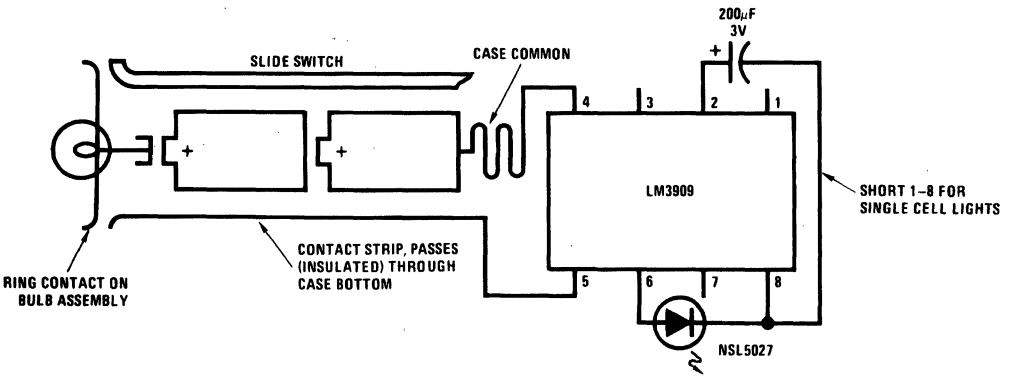


TL/H/7969-11

Note: Winking LED inside, locates light in total darkness.

Typical Applications (Continued) (See applications notes above)

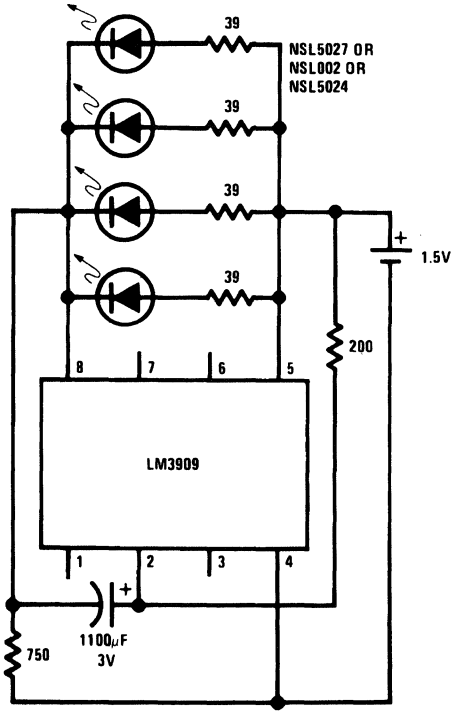
Flashlight Finder



TL/H/7969–10

Note: LM3909, capacitor, and LED are installed in a white translucent cap on the flashlight's back end. Only one contact strip (in addition to the case connection) is needed for flasher power. Drawing current through the bulb simplifies wiring and causes negligible loss since bulb resistance cold is typically less than 2Ω.

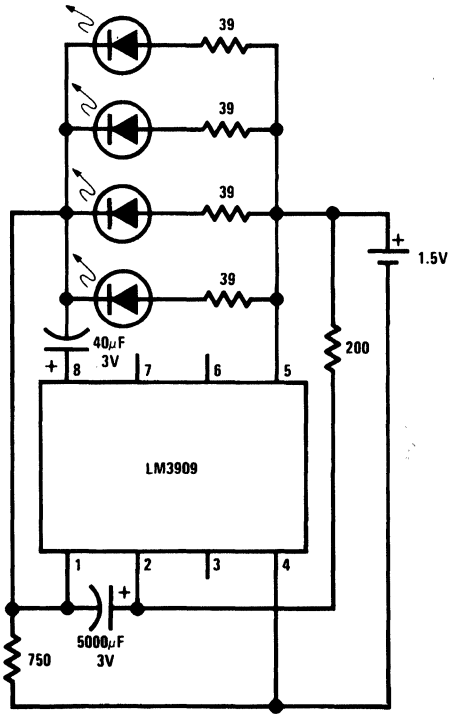
4 Parallel LEDs



TL/H/7969–12

Note: Nominal flash rate: 1.3 Hz. Average I_{DRAIN} = 2 mA.

High Efficiency Parallel Circuit

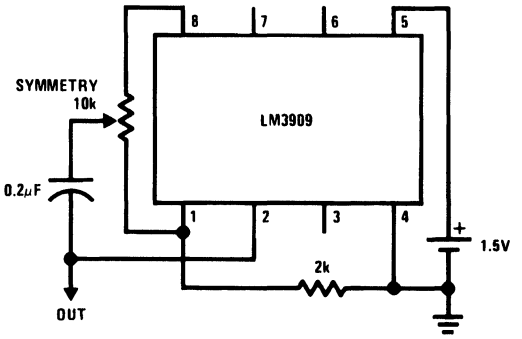


TL/H/7969–13

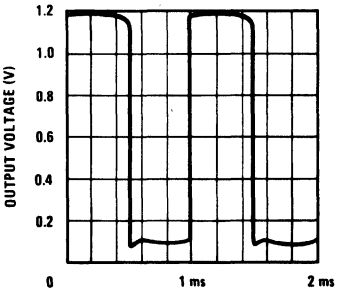
Note: Nominal flash rate: 1.5 Hz. Average I_{DRAIN} = 1.5 mA.

Typical Applications (Continued) (See applications notes above)

1 kHz Square Wave



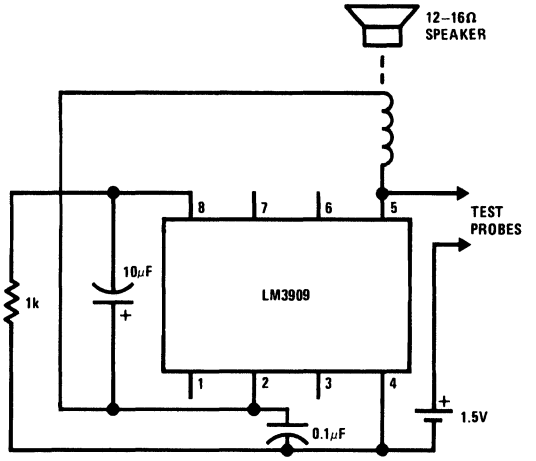
TL/H/7969–14



TL/H/7969–15

Note: Output voltage through a 10k load to ground.

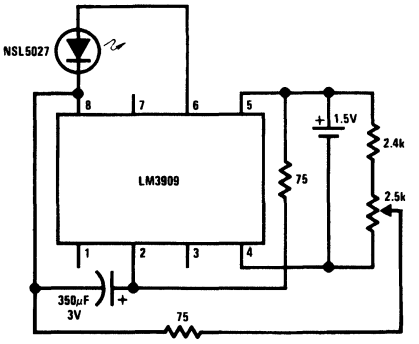
"Buzz Box" Continuity and Coil Checker



TL/H/7969–16

Note: Differences between shorts, coils, and a few ohms of resistance can be heard.

Variable Flasher

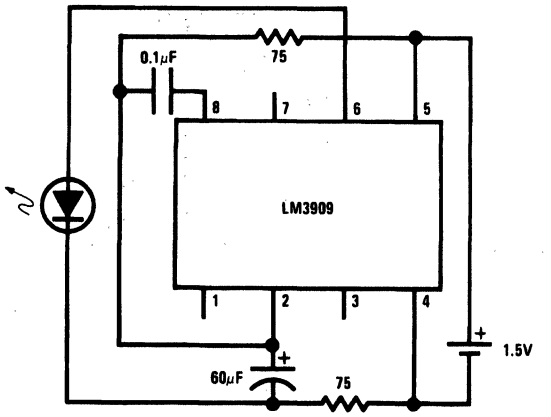


TL/H/7969–17

Note: Flash rate: 0 Hz–20 Hz.

Typical Applications (Continued) (See applications notes above)

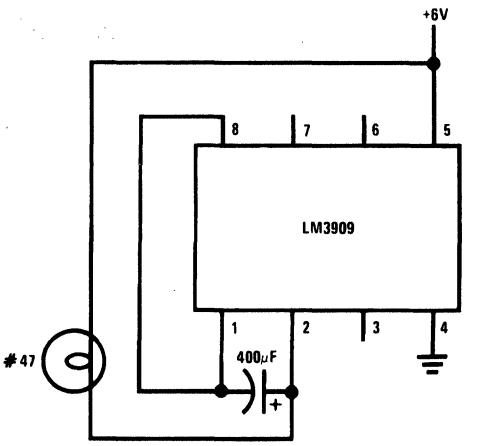
LED Booster



TL/H/7969–18

Note: High efficiency, 4 mA drain. Continuous appearing light obtained by supplying short, high current, pulses (2 kHz) to LEDs with higher than battery voltage available.

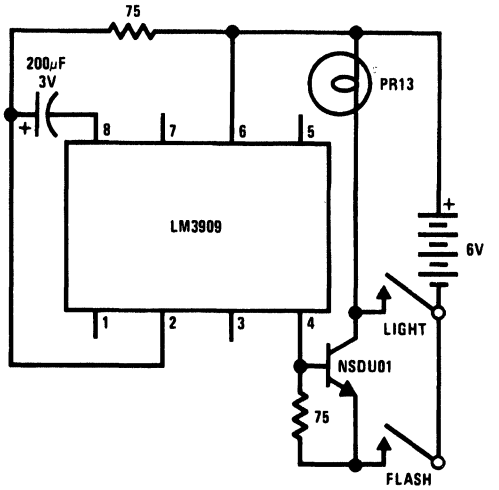
Incandescent Bulb Flasher



TL/H/7969–19

Note: Flash rate: 1.5 Hz.

Emergency Lantern/Flasher



TL/H/7969–20

Note: Nominal flash rate: 1.5 Hz.

National Semiconductor

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package.

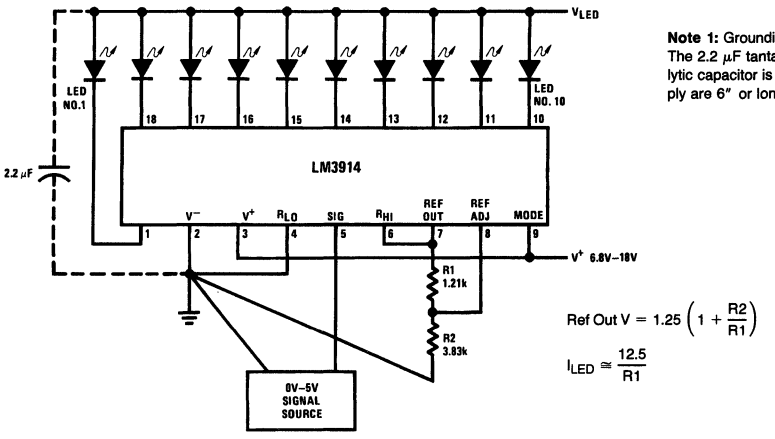
The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 mA to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \cong \frac{12.5}{R1}$$

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
COMPARATOR						
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA			3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA			3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA		3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$			25	100	nA
Input Signal Overvoltage	No Change in Display		−35		35	V
VOLTAGE-DIVIDER						
Divider Resistance	Total, Pin 6 to 4		8	12	17	kΩ
Accuracy	(Note 2)			0.5	2	%
VOLTAGE REFERENCE						
Output Voltage	0.1 mA $\le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$			0.01	0.03	%/V
Load Regulation	0.1 mA $\le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$			0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = 5V$			1		%
Adjust Pin Current				75	120	μA
OUTPUT DRIVERS						
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA		7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$	$I_{LED} = 2$ mA		0.12	0.4	mA
		$I_{LED} = 20$ mA		1.2	3	
LED Current Regulation	$2V \le V_{LED} \le 17V$	$I_{LED} = 2$ mA		0.1	0.25	mA
		$I_{LED} = 20$ mA		1	3	
Dropout Voltage	$I_{LED(ON)} = 20$ mA, $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA				1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA			0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)			0.1	10	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
OUTPUT DRIVERS (Continued)						
Output Leakage	(Dot Mode) (Note 4)	Pins 10–18		0.1	10	μA
		Pin 1	60	150	450	μA
SUPPLY CURRENT						
Standby Supply Current (All Outputs Off)	$V^+ = 5V$, $I_{L(REF)} = 0.2$ mA			2.4	4.2	mA
	$V^+ = 20V$, $I_{L(REF)} = 1.0$ mA			6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:
$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$
$3\ V_{DC} \le V_{LED} \le V^+$ $0V \le V_{IN} \le V^+ - 1.5V$
$-0.015V \le V_{RLO} \le 12\ V_{DC}$ $T_A = +25°C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Bar Mode).
$-0.015V \le V_{RHI} \le 12\ V_{DC}$
For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to $+10.000\ V_{DC}$ at pin 6, with $0.000\ V_{DC}$ at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

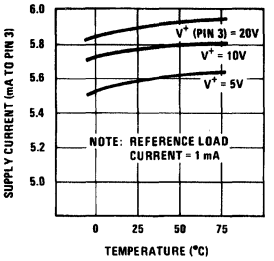
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

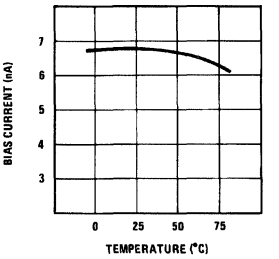
Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Typical Performance Characteristics

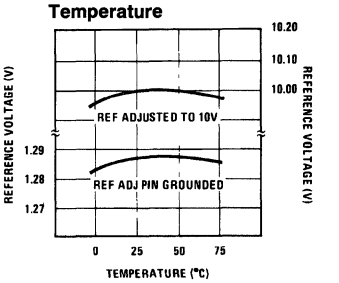
Supply Current vs Temperature



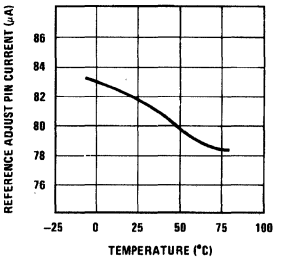
Operating Input Bias Current vs Temperature



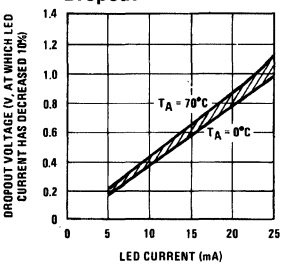
Reference Voltage vs Temperature



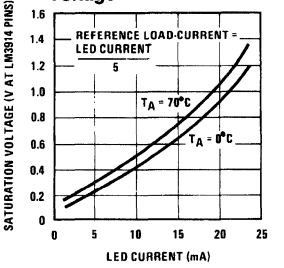
Reference Adjust Pin Current vs Temperature



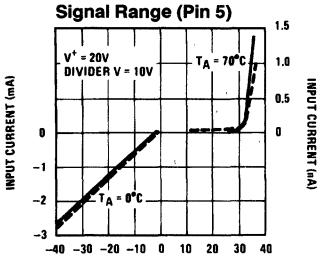
LED Current-Regulation Dropout



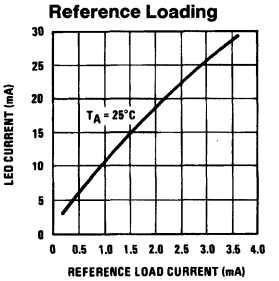
LED Driver Saturation Voltage



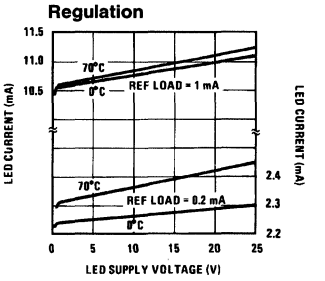
Input Current Beyond Signal Range (Pin 5)



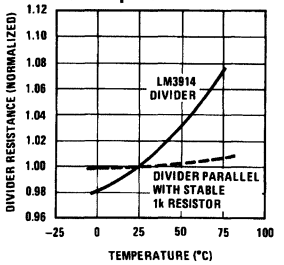
LED Current vs Reference Loading



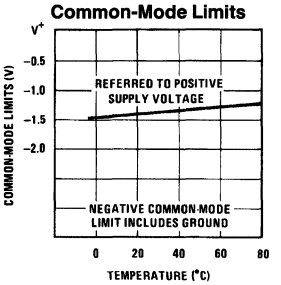
LED Driver Current Regulation



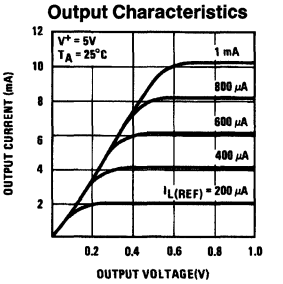
Total Divider Resistance vs Temperature



Common-Mode Limits



Output Characteristics



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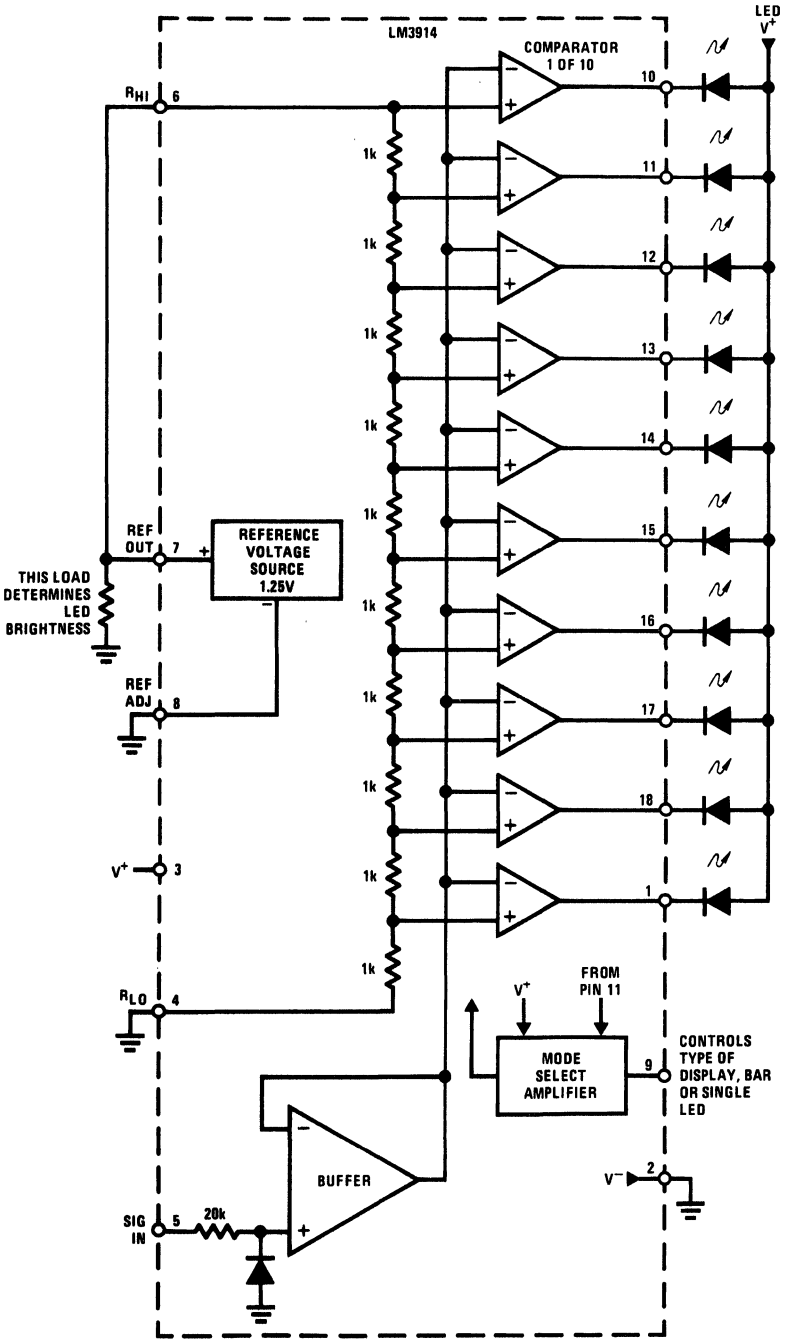
Block Diagram (Showing Simplest Application)



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Functional Description

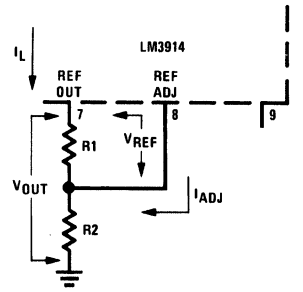
The simplifed LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



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Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

MODE PIN USE

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

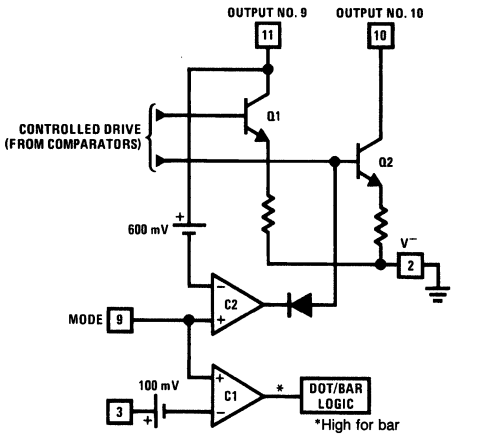
Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



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Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

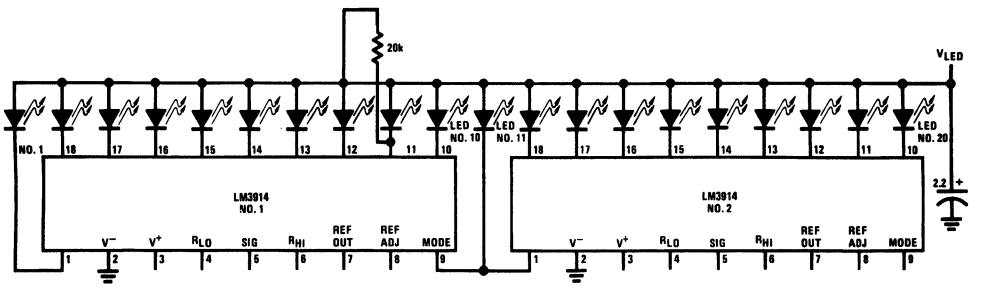
OTHER DEVICE CHARACTERISTICS

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 2). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 μF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

Cascading LM3914s in Dot Mode



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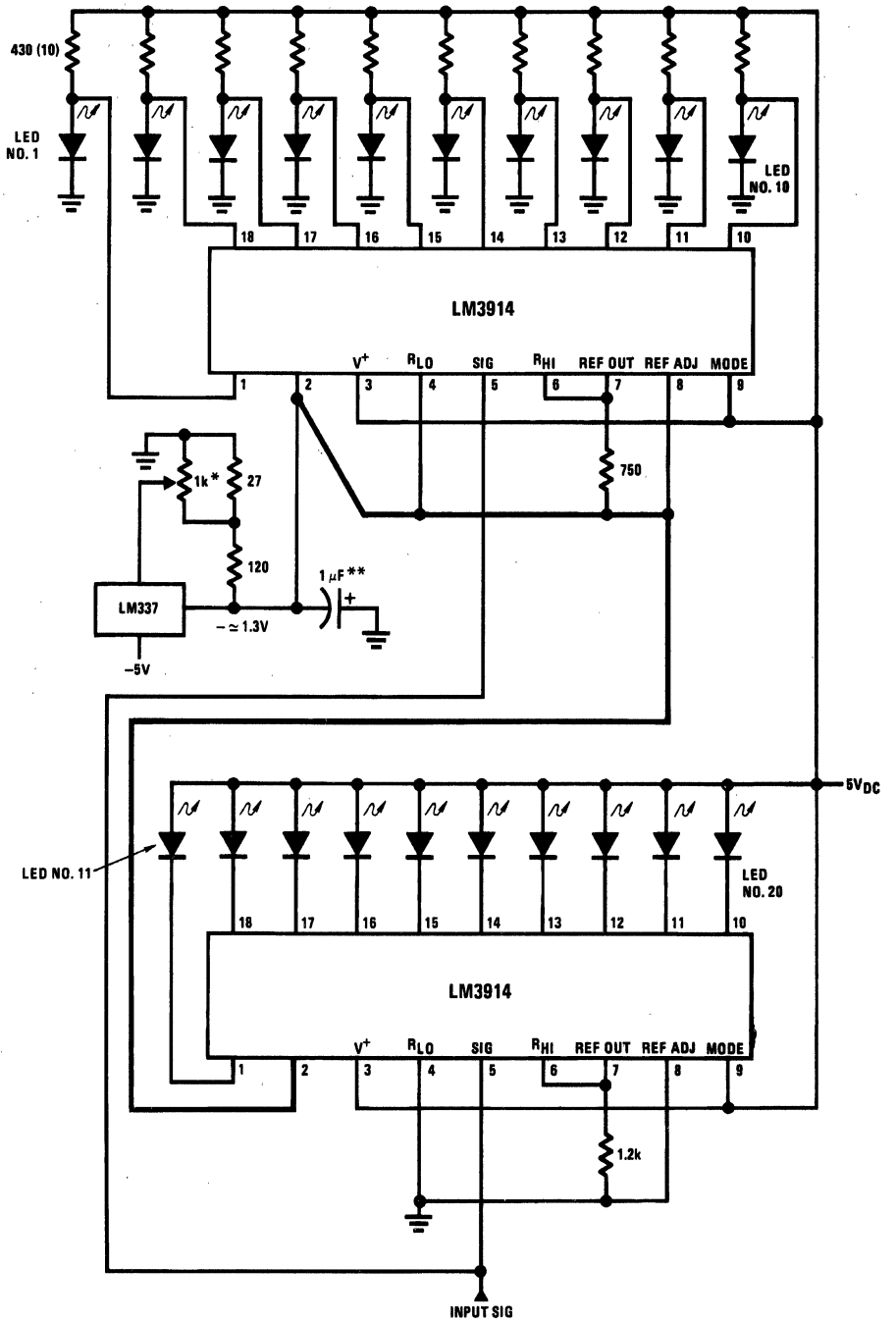
Typical Applications (Continued)

Zero-Center Meter, 20-Segment



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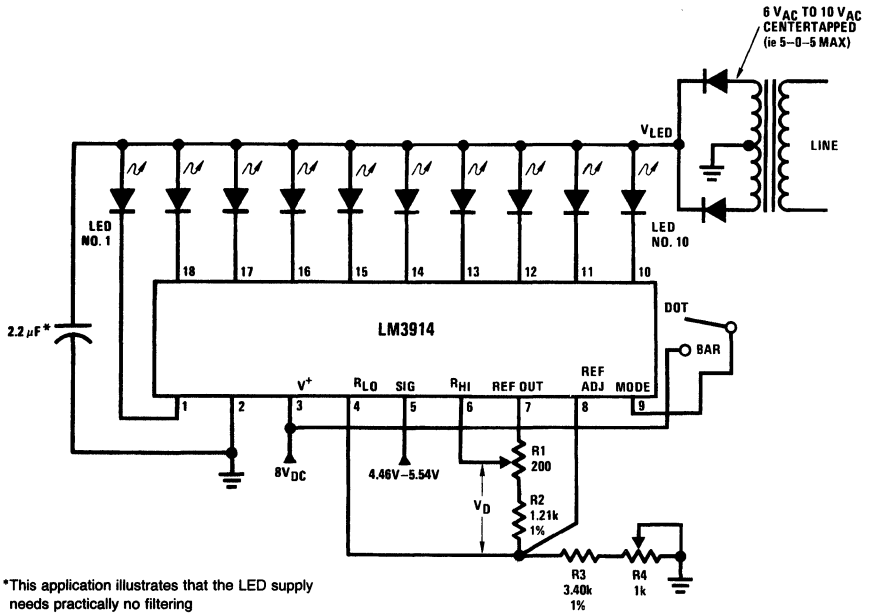
Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



*This application illustrates that the LED supply needs practically no filtering

Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.94V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

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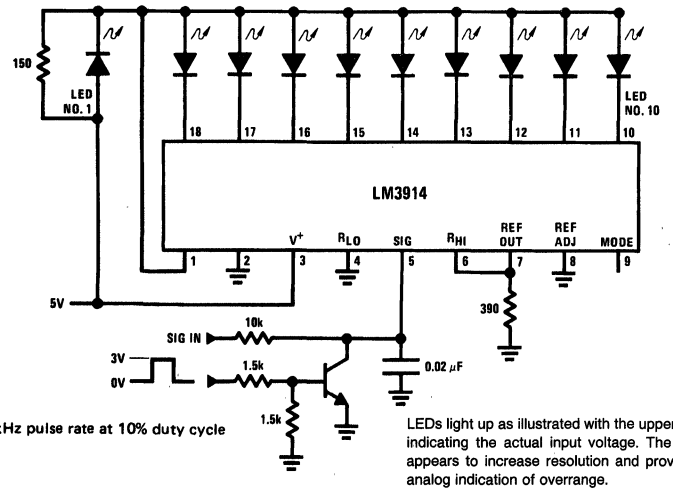
Application Example: Grading 5V Regulators

Highest No. LED on	Color	$V_{OUT(MIN)}$
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
5V		
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

Typical Applications (Continued)

"Exclamation Point" Display

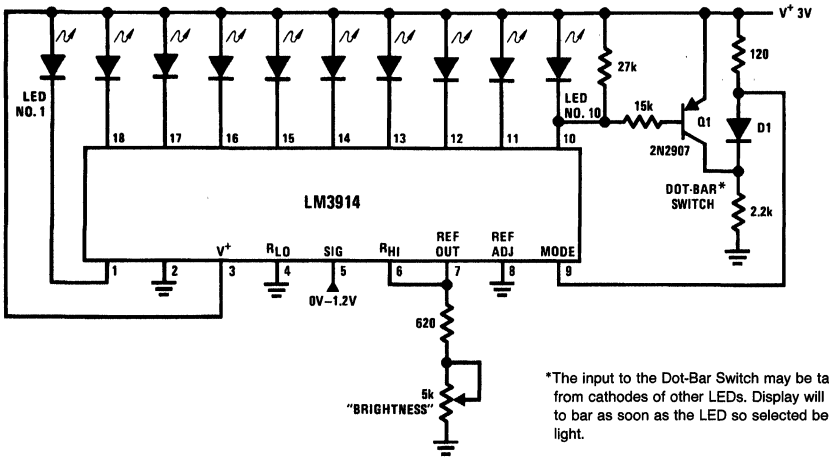


1 kHz pulse rate at 10% duty cycle

LEDs light up as illustrated with the upper lit LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

TL/H/7970–9

Indicator and Alarm, Full-Scale Changes Display from Dot to Bar

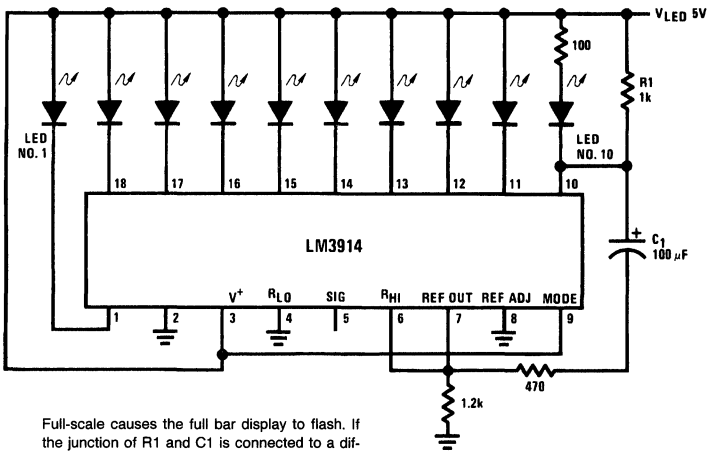


*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

TL/H/7970–10

Typical Applications (Continued)

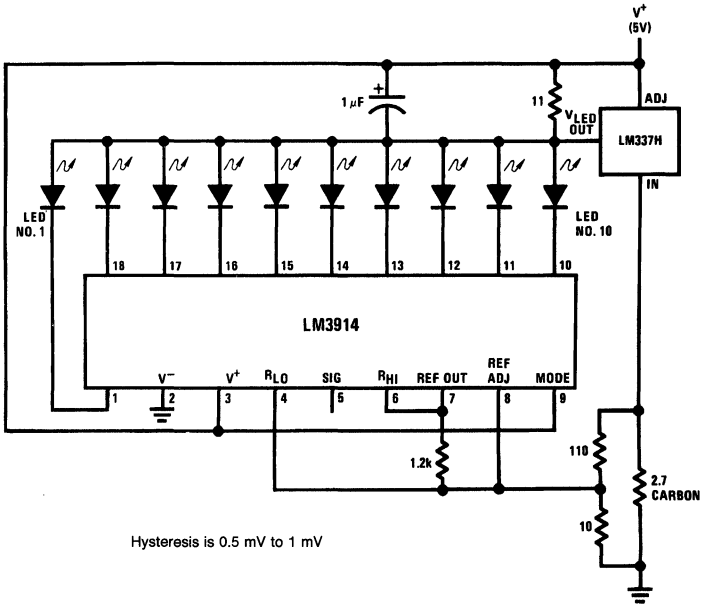
Bar Display wih Alarm Flasher



Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7970–11

Adding Hysteresis (Single Supply, Bar Mode Only)

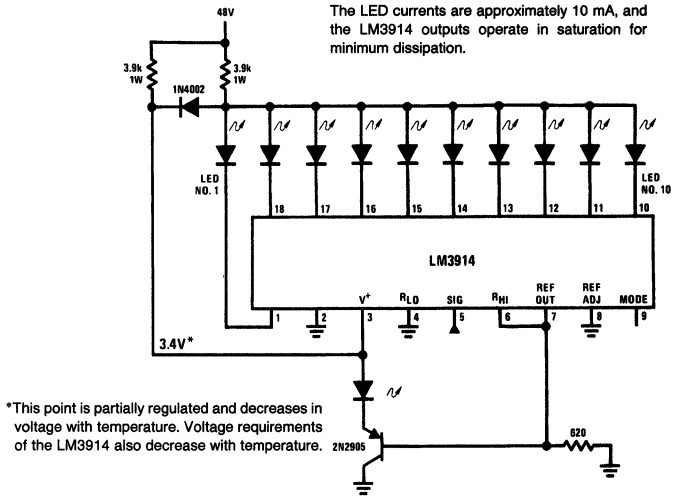


Hysteresis is 0.5 mV to 1 mV

TL/H/7970–12

Typical Application (Continued)

Operating with a High Voltage Supply (Dot Mode Only)

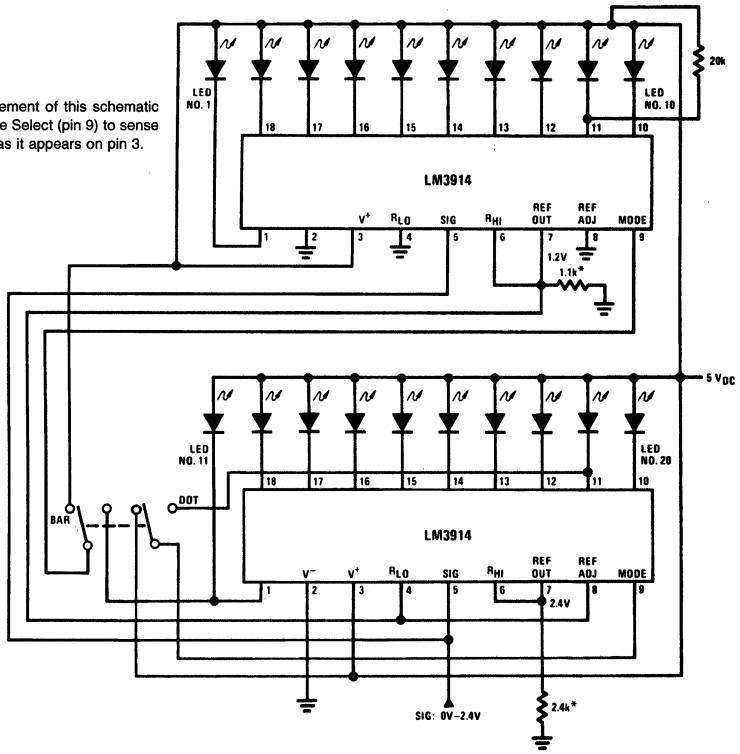


The LED currents are approximately 10 mA, and the LM3914 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3914 also decrease with temperature.

TL/H/7970–13

20-Segment Meter with Mode Switch



*The exact wiring arrangement of this schematic shows the need for Mode Select (pin 9) to sense the V^+ voltage exactly as it appears on pin 3.

*Programs LEDs to 10 mA

TL/H/7970–14

Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing (see page 9-108) showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits (see Note 2, page 9-108). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 μA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called "Application Tips for the LM3914 Adjustable Reference" has been included with these schematics.

APPLICATION TIPS FOR THE LM3914 ADJUSTABLE REFERENCE

GREATLY EXPANDED SCALE (BAR MODE ONLY)

Placing the LM3914 internal resistor divider in parallel with a section (≅230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

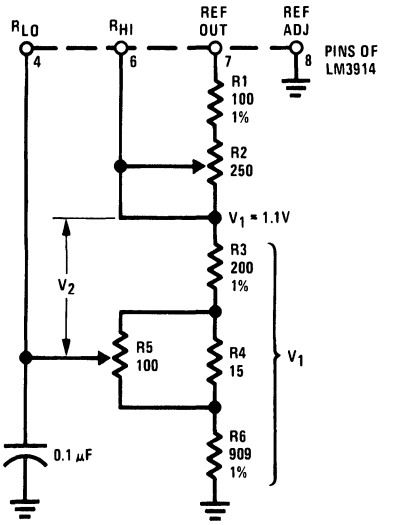
NON-INTERACTING ADJUSTMENTS FOR EXPANDED SCALE METER (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made.

Greatly Expanded Scale (Bar Mode Only)



TL/H/7970–15

ADJUSTING LINEARITY OF SEVERAL STACKED DIVIDERS

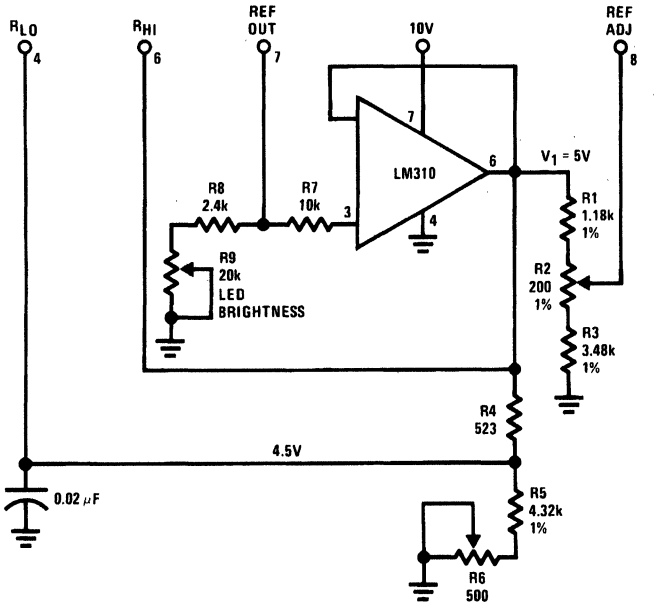
Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

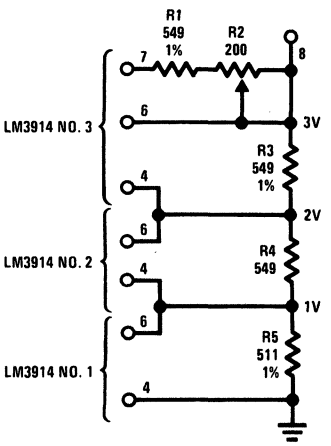
Application Hints (Continued)

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)



TL/H/7970–16

Adjusting Linearity of Several Stacked Dividers



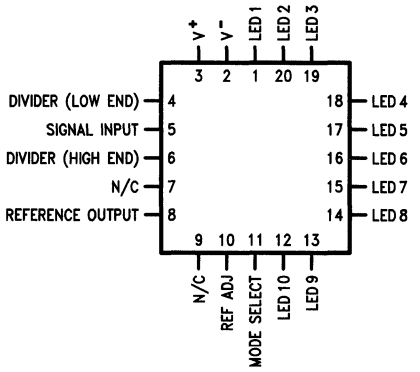
TL/H/7970–17

Other Applications

- "Slow"—fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"—display could be circle or semi-circle
- Moving "hole" display—indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagrams

Plastic Chip Carrier Package

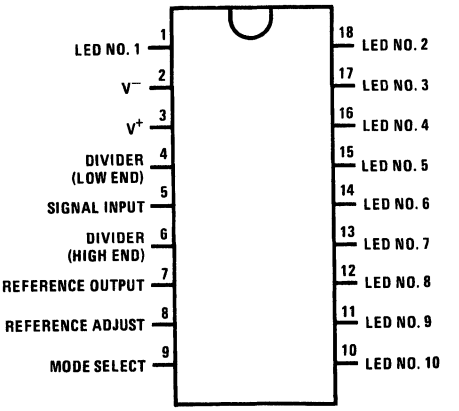


TL/H/7970–18

Top View

Order Number LM3914V
See NS Package Number V20A

Dual-In-Line Package



TL/H/7970–19

Top View

Order Number LM3914N
See NS Package Number N18A

4

National Semiconductor

LM3915 Dot/Bar Display Driver

General Description

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

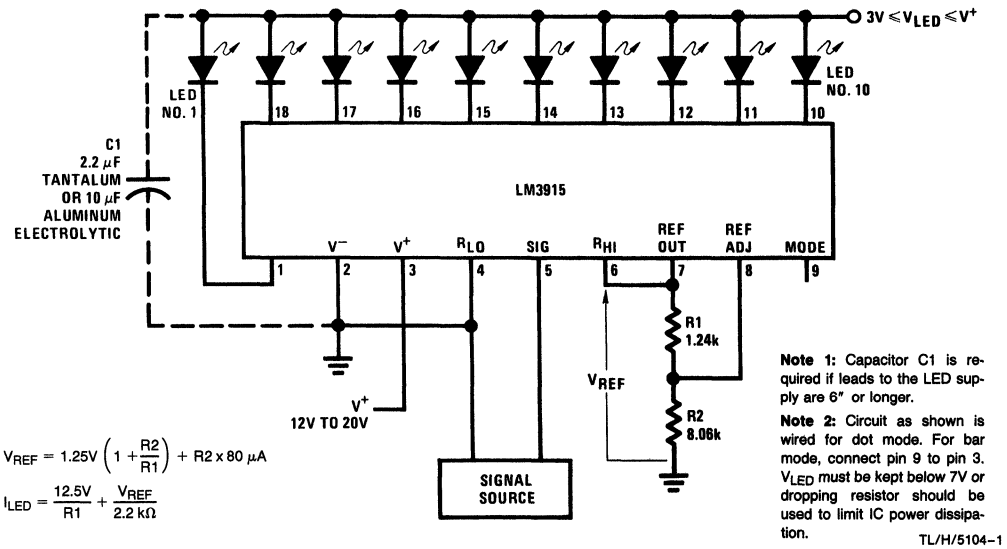
Features

- 3 dB/step, 30 dB range
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 90 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3915 is rated for operation from 0°C to +70°C. The LM3915N is available in an 18-lead molded DIP package.

Typical Applications

0V to 10V Log Display



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\ \mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\ k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

TL/H/5104–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP(N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Comparators					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
Voltage-Divider					
Divider Resistance	Total, Pin 6 to 4	16	28	36	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2)	2.0	3.0	4.0	dB
Absolute Accuracy at Each Threshold Point	(Note 2)				
	$V_{IN} = -3, -6$ dB	−0.5		+0.5	dB
	$V_{IN} = -9$ dB	−0.5		+0.65	dB
	$V_{IN} = -12, -15, -18$ dB	−0.5		+1.0	dB
	$V_{IH} = -21, -24, -27$ dB	−0.5		+1.5	dB
Voltage Reference					
Output Voltage	$0.1 \text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	$0.1 \text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED}$ 5V		1		%
Adjust Pin Current			75	120	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Output Drivers					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA		0.12	0.4	mA
	$V_{LED} = 5V$, I_{LED} 20 mA		1.2	3	mA
LED Current Regulation	$2V \le V_{LED} \le 17V$, $I_{LED} = 2$ mA		0.1	0.25	mA
	$I_{LED} = 20$ mA		1	3	mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	10	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10-18			0.1	10	μA
Pin 1		60	150	450	μA
Supply Current					
Standby Supply Current (All Outputs Off)	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to 0 dB = + 10.000 V_{DC} at pin 5, with + 10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

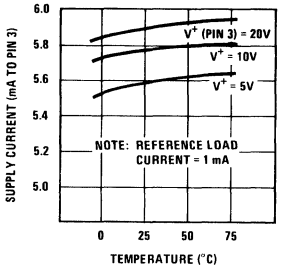
Note 5: The maximum junction temperature of the LM3915 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

THRESHOLD VOLTAGE (Note 2)

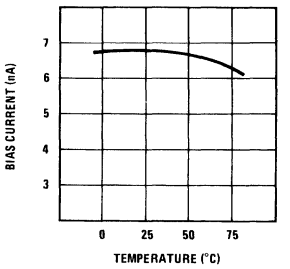
Output	dB	Min	Typ	Max	Output	dB	Min	Typ	Max
1	−27	0.422	0.447	0.531	6	−12	2.372	2.512	2.819
2	−24	0.596	0.631	0.750	7	−9	3.350	3.548	3.825
3	−21	0.841	0.891	1.059	8	−6	4.732	5.012	5.309
4	−18	1.189	1.259	1.413	9	−3	6.683	7.079	7.498
5	−15	1.679	1.778	1.995	10	0	9.985	10	10.015

Typical Performance Characteristics

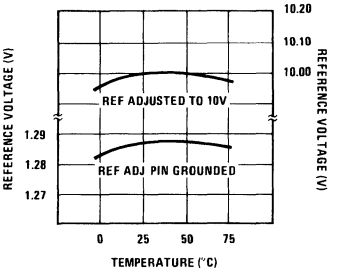
Supply Current vs Temperature



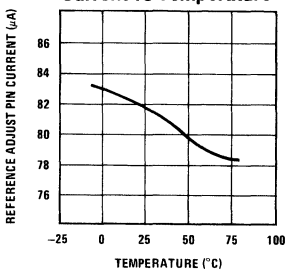
Operating Input Bias Current vs Temperature



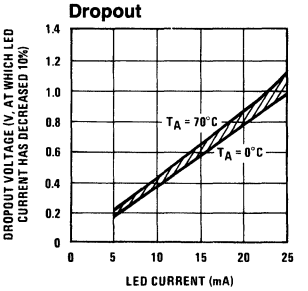
Reference Voltage vs Temperature



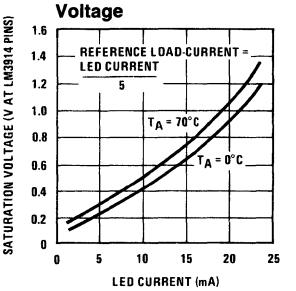
Reference Adjust Pin Current vs Temperature



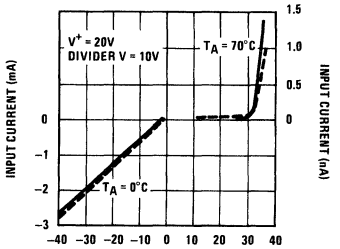
LED Current-Regulation Dropout



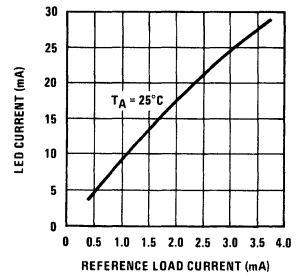
LED Driver Saturation Voltage



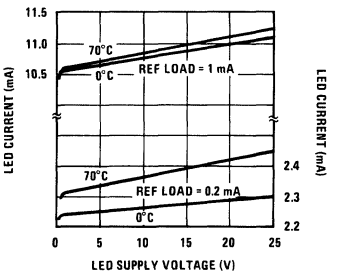
Input Current Beyond Signal Range (Pin 5)



LED Current vs Reference Loading

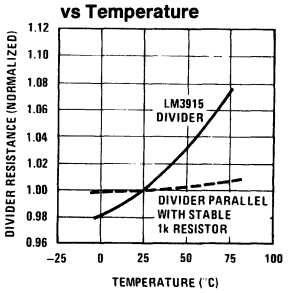


LED Driver Current Regulation

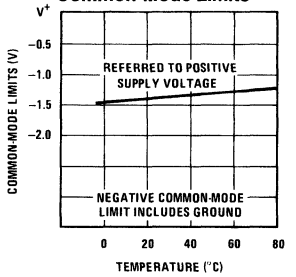


TL/H/5104–2

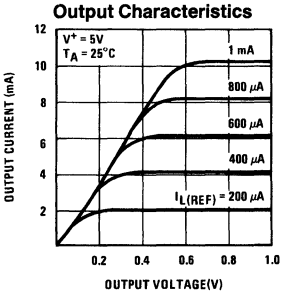
Total Divider Resistance vs Temperature



Common-Mode Limits

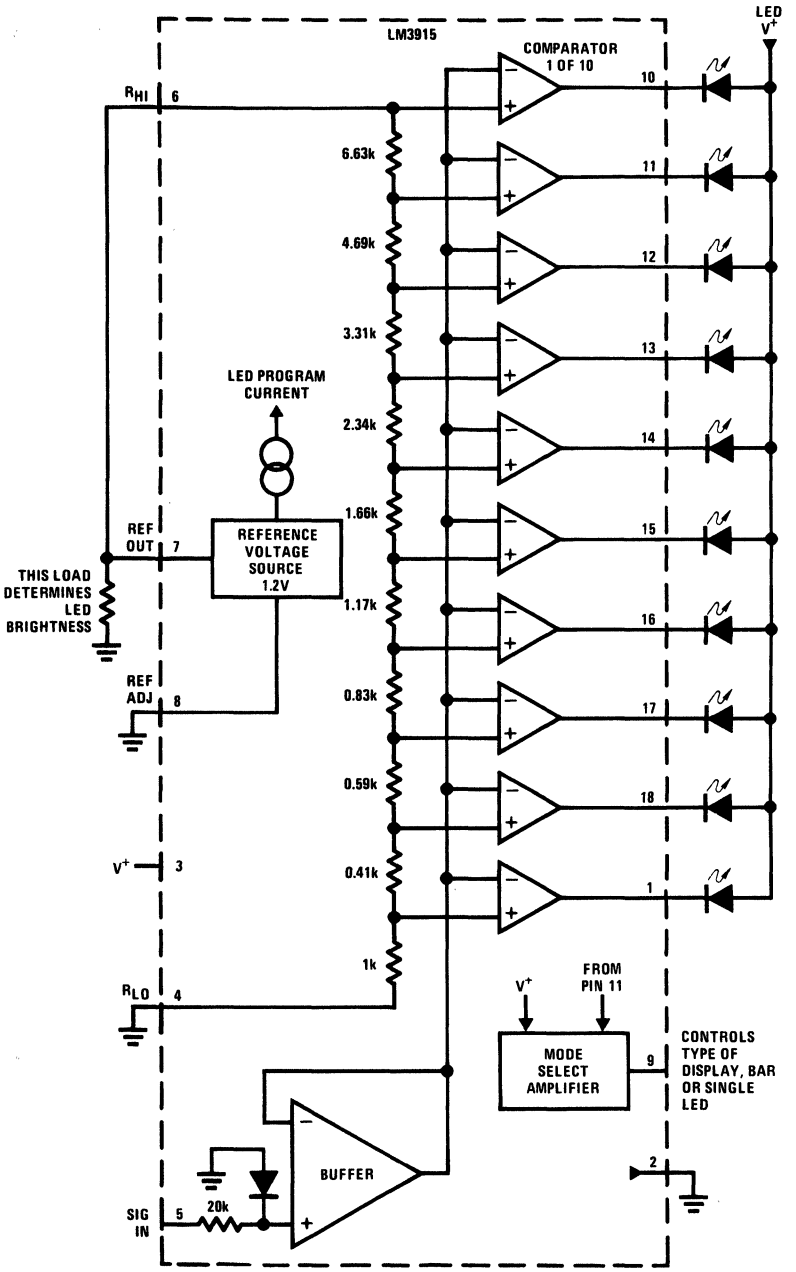


Output Characteristics



TL/H/5104–3

Block Diagram (Showing Simplest Application)



TL/H/5104–4

Functional Description

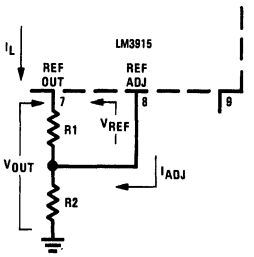
The simplified LM3915 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 3 dB that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



TL/H/5104–5

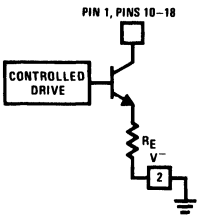
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3915 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3915 Output Circuit



TL/H/5104–6

Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple LM3915s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

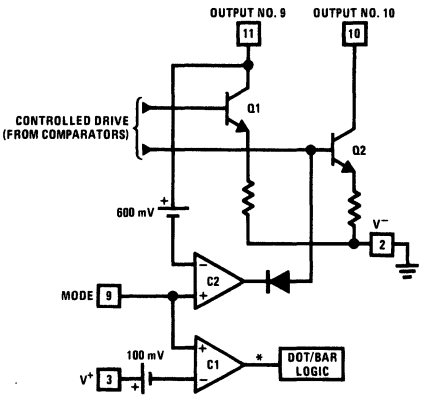
Dot Display, Single LM3915 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3915 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3915 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



*High for bar

TL/H/5104–7

Mode Pin Functional Description

(Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3915s are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3915, LED #11 is off. Pin 9 of LM3915 #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of LM3915 #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3915 #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

OTHER DEVICE CHARACTERISTICS

The LM3916 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3916 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device "chained" to the first.

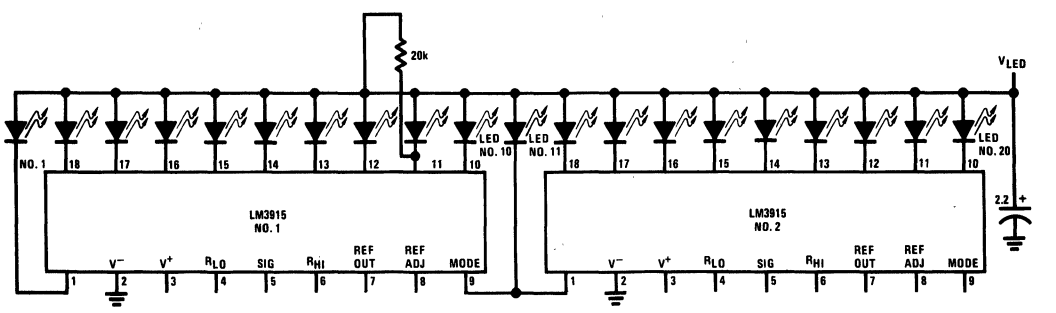
Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Cascading LM3915s in Dot Mode



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Application Hints (Continued)

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

The simplest way to display an AC signal using the LM3915 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3915 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). It's recommended to use dot mode and to run the LEDs at 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3915 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 1* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3915 is used for a 30 dB display.

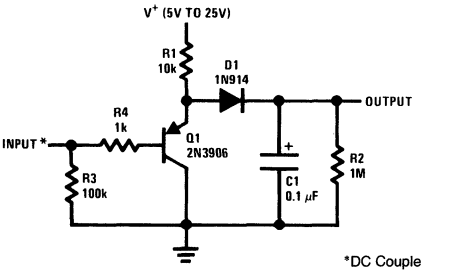
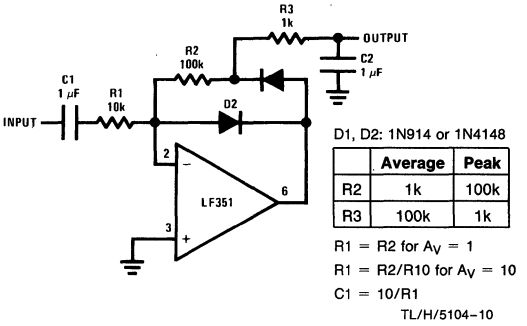


FIGURE 1. Half-Wave Peak Detector

Display circuits using two or more LM3915s for a dynamic range of 60 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 2* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353, or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

For precision full-wave averaging use the circuit in *Figure 3*. Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5–C2. A simple modification results in the precision full-wave detector of *Figure 4*. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3915.



	Average	Peak
R2	1k	100k
R3	100k	1k

FIGURE 2. Precision Half-Wave Rectifier

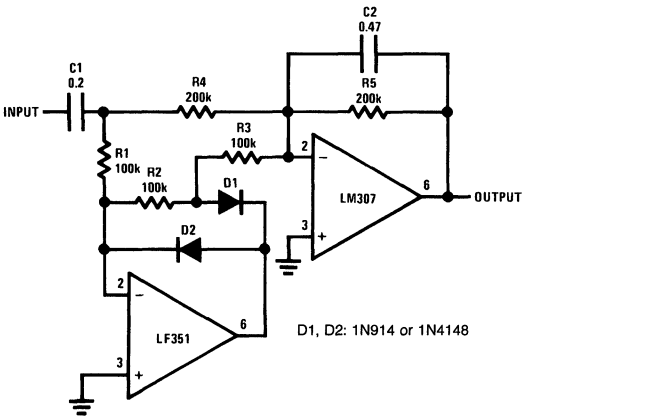


FIGURE 3. Precision Full-Wave Average Detector

Application Hints (Continued)

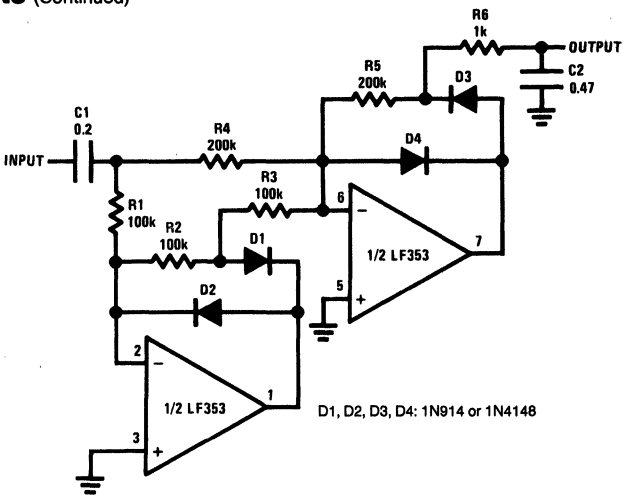


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FIGURE 4. Precision Full-Wave Peak Detector

CASCADING THE LM3915

To display signals of 60 or 90 dB dynamic range, multiple LM3915s can be easily cascaded. Alternatively, it is possible to cascade an LM3915 with LM3914s for a log/linear display or with an LM3916 to get an extended range VU meter.

A simple, low cost approach to cascading two LM3915s is to set the reference voltages of the two chips 30 dB apart as in *Figure 5*. Potentiometer R1 is used to adjust the full scale voltage of LM3915 #1 to 316 mV nominally while the second IC's reference is set at 10V by R4. The drawback of this method is that the threshold of LED #1 is only 14 mV and, since the LM3915 can have an offset voltage as high as 10 mV, large errors can occur. This technique is not recommended for 60 dB displays requiring good accuracy at the first few display thresholds.

A better approach shown in *Figure 6* is to keep the reference at 10V for both LM3915s and amplify the input signal to the lower LM3915 by 30 dB. Since two 1% resistors can set the amplifier gain within ±0.2 dB, a gain trim is unnecessary. However, an op amp offset voltage of 5 mV will shift the first LED threshold as much as 4 dB, so that an offset trim may be required. Note that a single adjustment can null out offset in both the precision rectifier and the 30 dB gain stage. Alternatively, instead of amplifying, input signals of sufficient amplitude can be fed directly to the lower LM3915 and *attenuated* by 30 dB to drive the second LM3915.

To extend this approach to get a 90 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 0.5 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

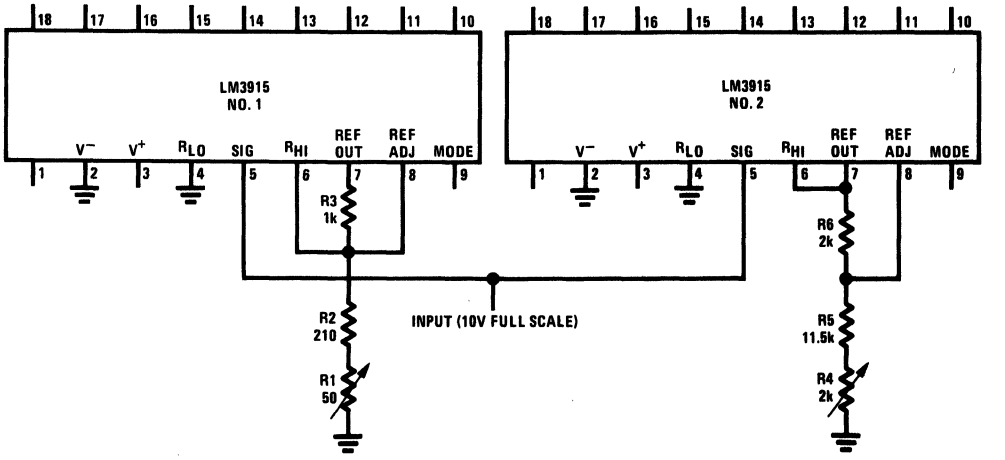

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FIGURE 5. Low Cost Circuit for 60 dB Display

Application Hints (Continued)

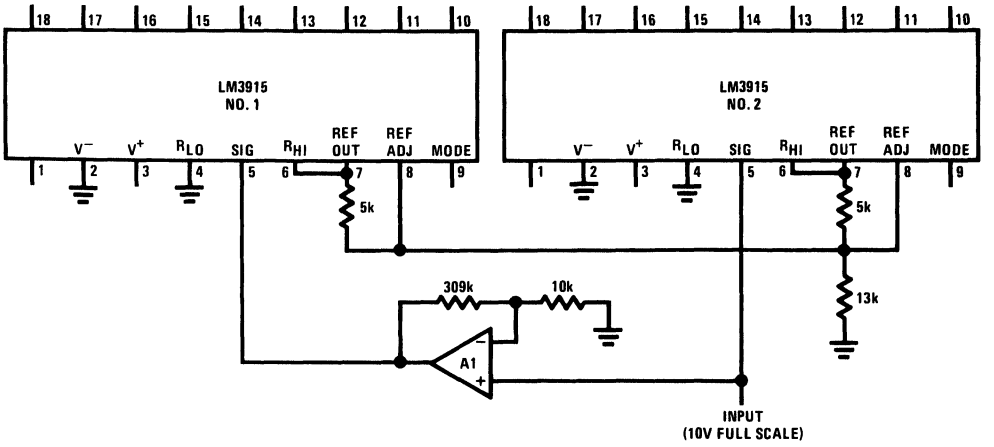

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FIGURE 6. Improved Circuit for 60 dB Display

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

SINGLE LM3915

The equations in *Figure 7* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 450 μA to flow from pin 7 into the divider which means that the LED current will be at least 5 mA. R1 will typically be between 1 kΩ and 2 kΩ. To trim the reference voltage, vary R2.

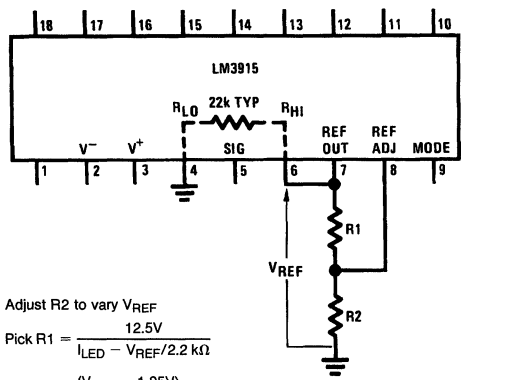

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FIGURE 7. Design Equations for Fixed LED Intensity

The circuit in *Figure 8* shows how to add a LED intensity control which can vary LED current from 9 mA to 28 mA. The reference adjustment has some effect on LED intensity but the reverse is not true.

MULTIPLE LM3915s

Figure 9 shows how to obtain a common reference trim and intensity control for two LM3915s. The two ICs may be connected in cascade for a 60 dB display or may be handling separate channels for stereo. This technique can be extended for larger numbers of LM3915s by varying the values of R1, R2 and R3 in inverse proportion to the number of devices tied in. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.1 dB for V_{REF} = 10V.

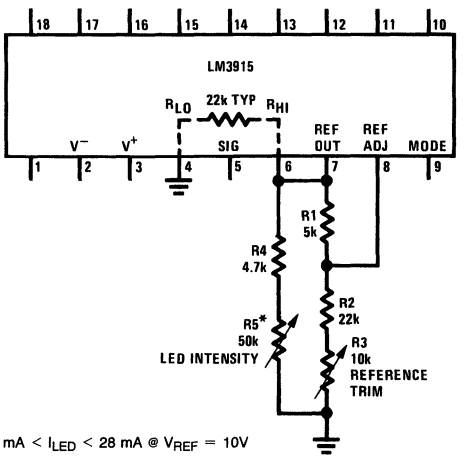

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FIGURE 8. Varying LED Intensity

Application Hints (Continued)

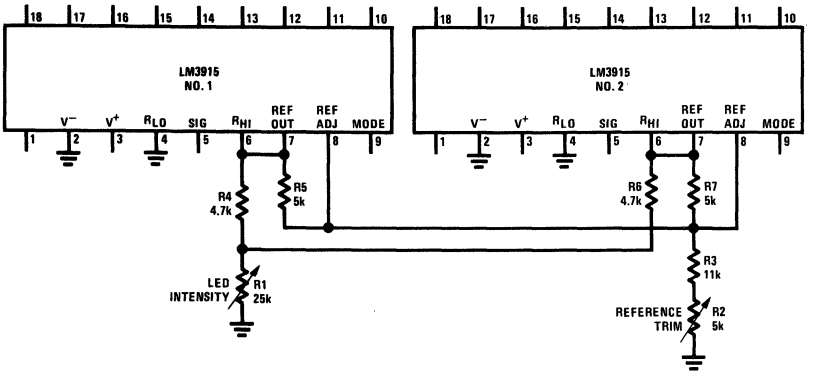

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FIGURE 9. Independent Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

The scheme in *Figure 10* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 20 mA.

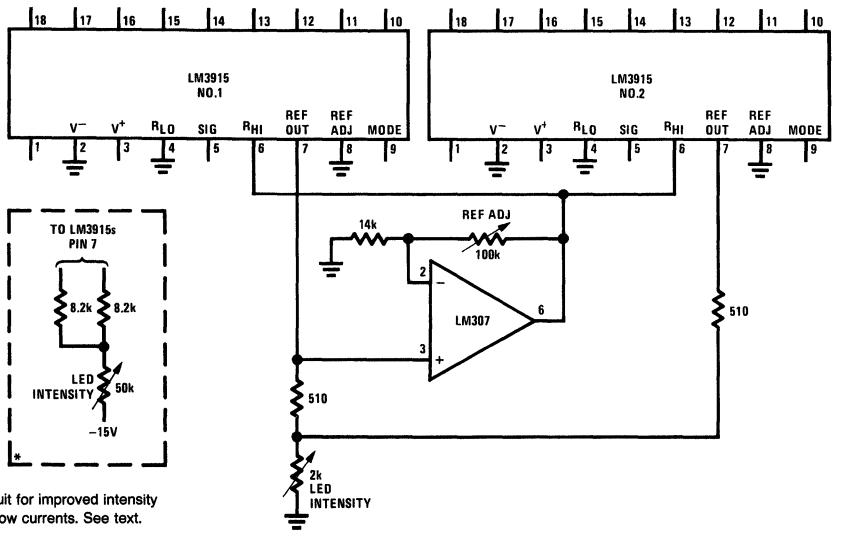
At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by varying the reference level at pin 6 by 3 dBp-p as shown in *Figure 11*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.

When an exponentially decaying RC discharge waveform is applied to pin 5, the LM3915's outputs will switch at equal intervals. This makes a simple timer or sequencer. Each time interval is equal to RC/3. The output may be used to drive logic, opto-couplers, relays or PNP transistors, for example.

Typical Applications



*Optional circuit for improved intensity matching at low currents. See text.

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FIGURE 10. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

Typical Applications (Continued)

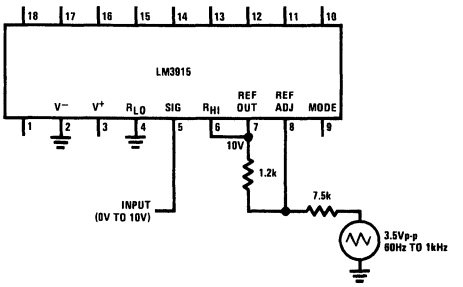

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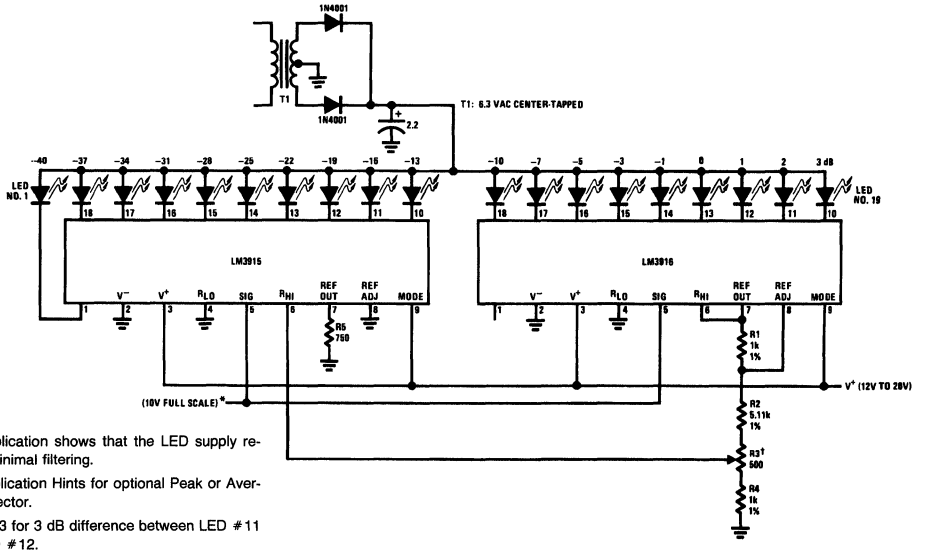
FIGURE 11. 0V to 10V Log Display with Smooth Transitions

Extended Range VU Meter



This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12.

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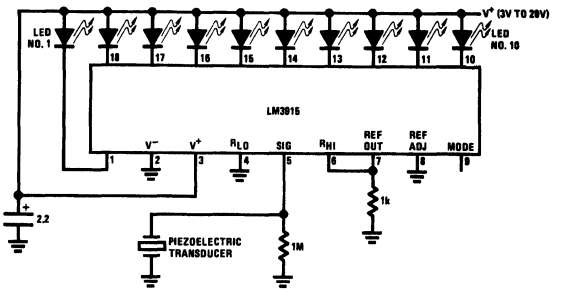
Vibration Meter



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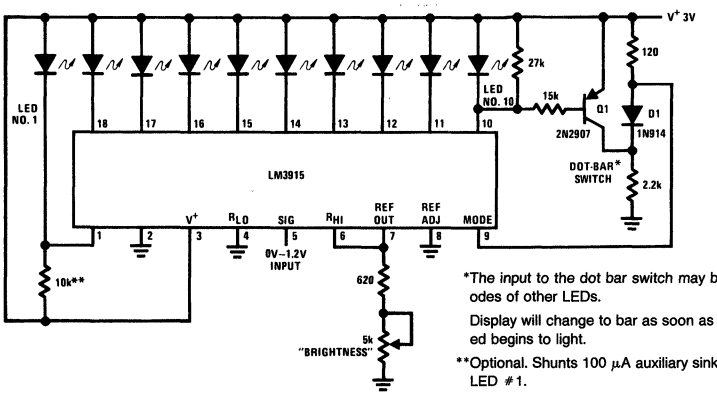
LED	Threshold
1	60 mV
2	80 mV
3	110 mV
4	160 mV
5	220 mV
6	320 mV
7	440 mV
8	630 mV
9	890 mV
10	1.25V

Typical Applications (Continued)

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



*The input to the dot bar switch may be taken from cathodes of other LEDs.

Display will change to bar as soon as the LED so selected begins to light.

**Optional. Shunts 100 μA auxiliary sink current away from LED #1.

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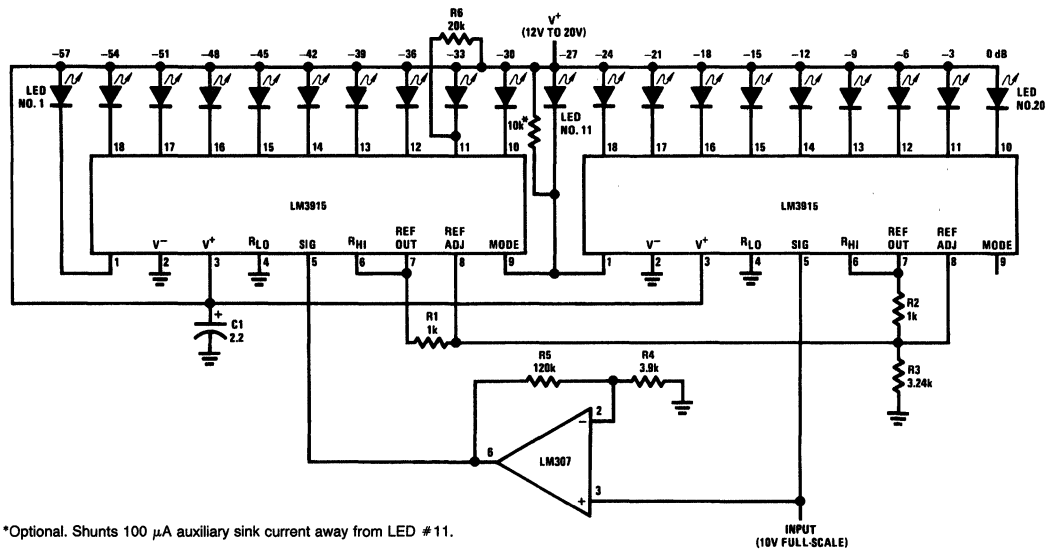
60 dB Dot Mode Display



*Optional. Shunts 100 μA auxiliary sink current away from LED #11.

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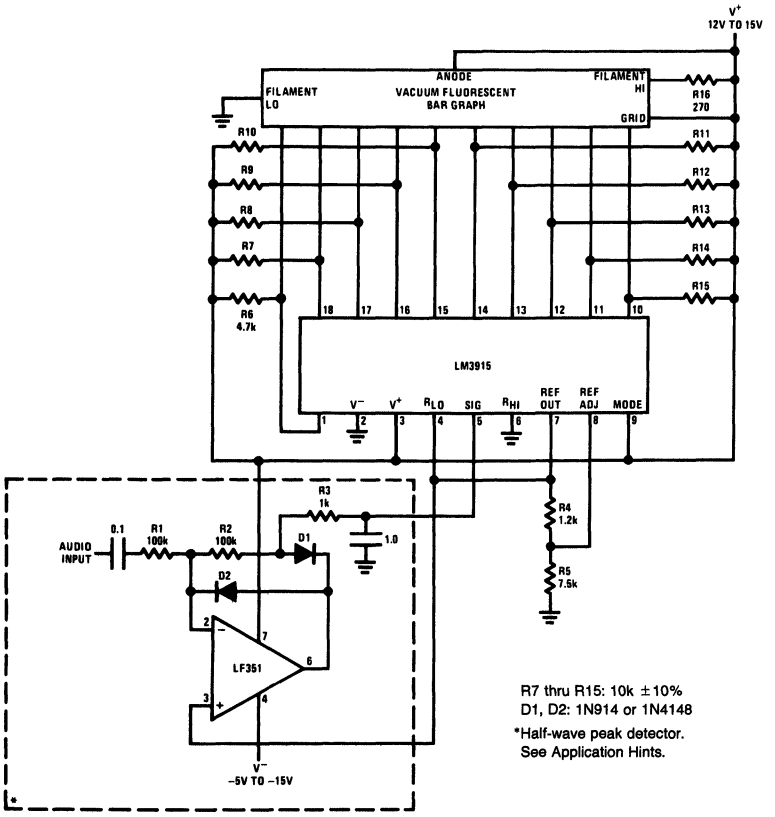
Typical Applications (Continued)

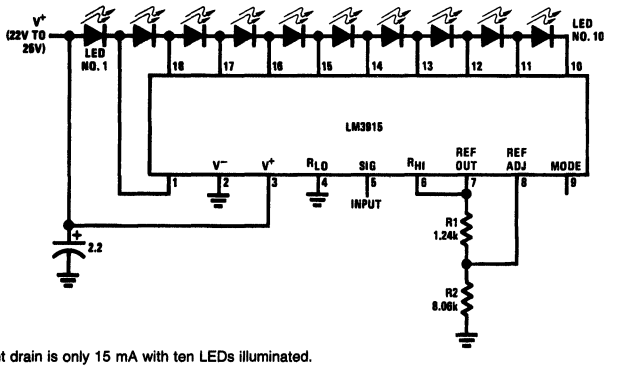
Driving Vacuum Fluorescent Display



R7 thru R15: 10k ±10%
D1, D2: 1N914 or 1N4148
*Half-wave peak detector.
See Application Hints.

TL/H/5104–24

Low Current Bar Mode Display

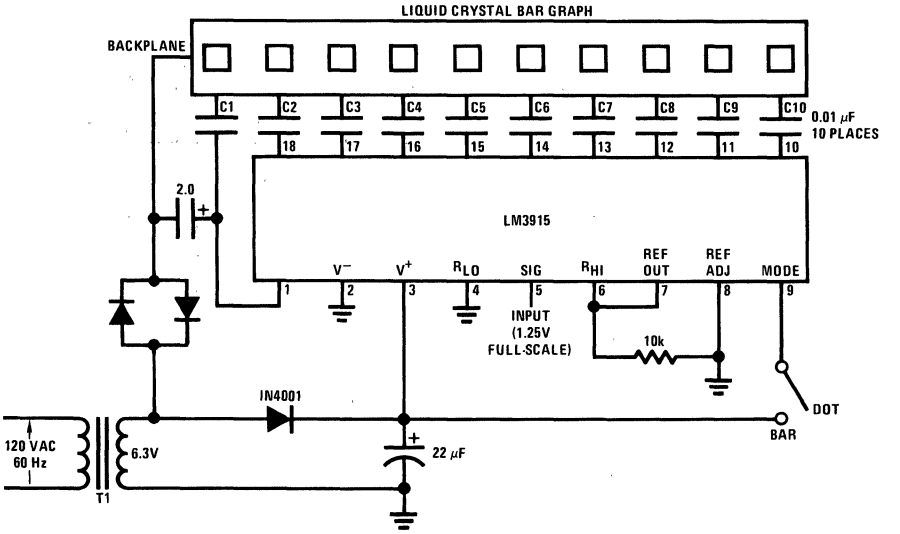


Supply current drain is only 15 mA with ten LEDs illuminated.

TL/H/5104–25

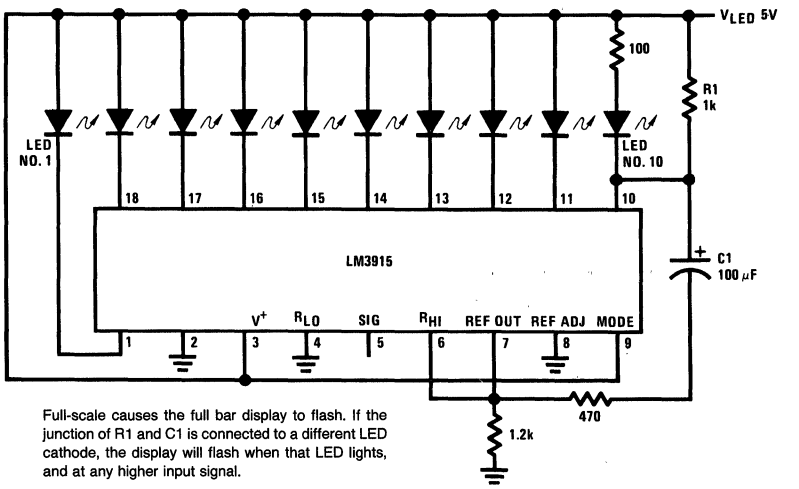
Typical Applications (Continued)

Driving Liquid Crystal Display



TL/H/5104–26

Bar Display with Alarm Flasher

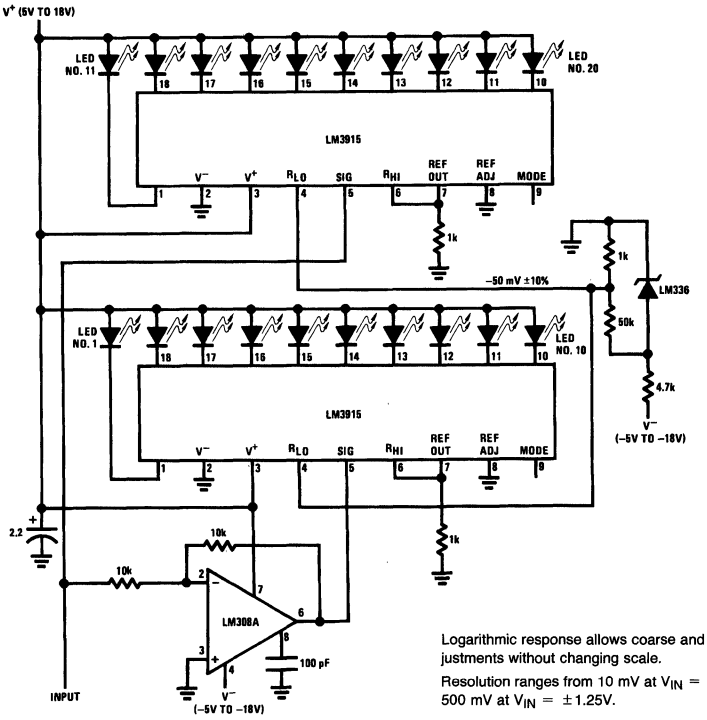


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/5104–27

Typical Applications (Continued)

Precision Null Meter

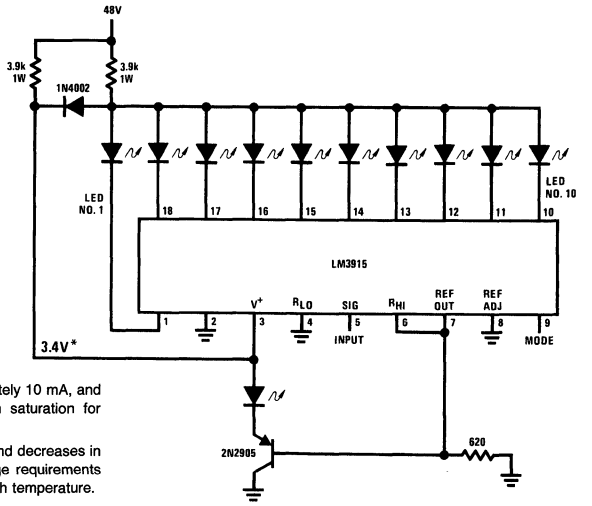


Logarithmic response allows coarse and fine adjustments without changing scale.

Resolution ranges from 10 mV at V_{IN} = 0 mV to 500 mV at V_{IN} = ±1.25V.

TL/H/5104–28

Operating with a High Voltage Supply (Dot Mode Only)



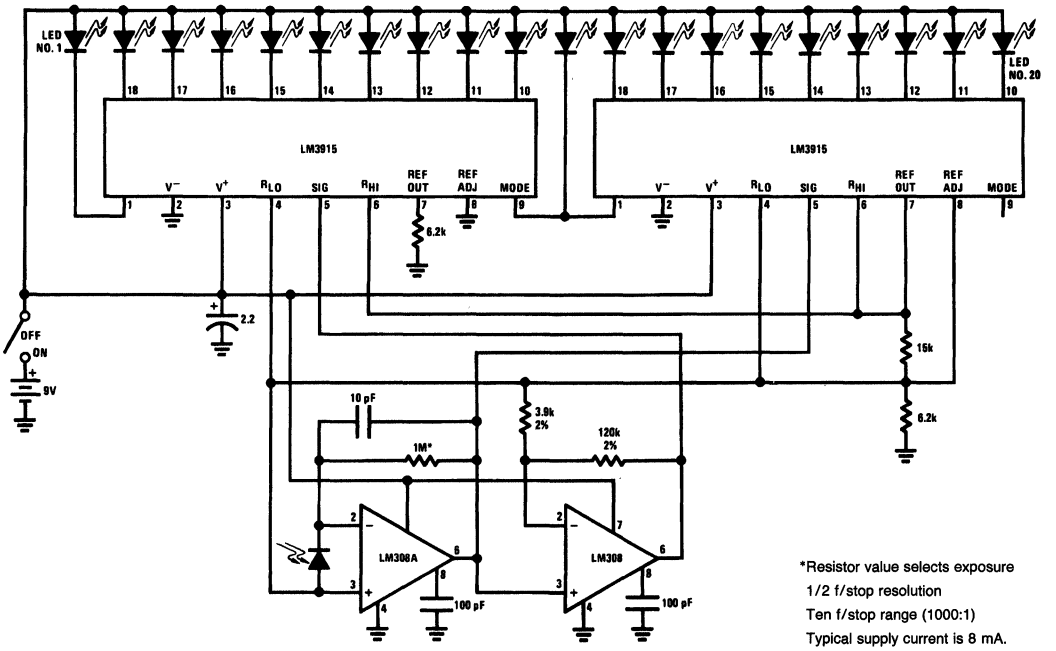
The LED currents are approximately 10 mA, and the LM3915 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3915 also decrease with temperature.

TL/H/5104–29

Typical Applications (Continued)

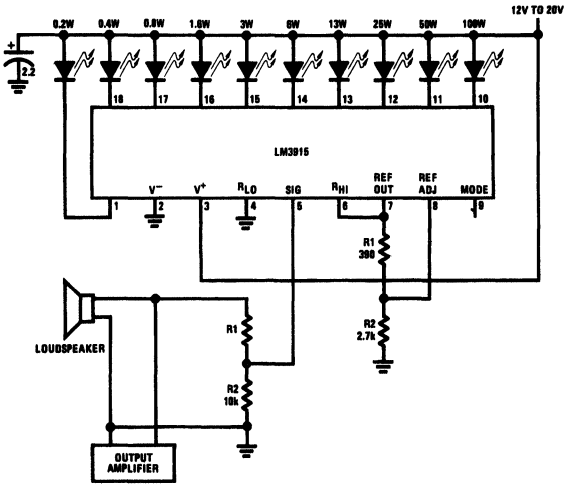
Light Meter



*Resistor value selects exposure
1/2 f/stop resolution
Ten f/stop range (1000:1)
Typical supply current is 8 mA.

TL/H/5104–30

Audio Power Meter



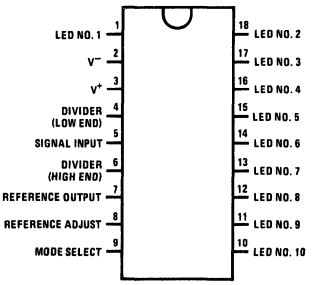
TL/H/5104–31

Load Impedance	R1
4Ω	10k
8Ω	18k
16Ω	30k

See Application Hints for optional Peak or Average Detector

Connection Diagram

Dual-In-Line Package



TL/H/5104–32

Top View

Order Number LM3915N
See NS Package Number N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage

National Semiconductor

LM3916 Dot/Bar Display Driver

General Description

The LM3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3916 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display for increased range and/or resolution. Useful in other applications are the linear LM3914 and the logarithmic LM3915.

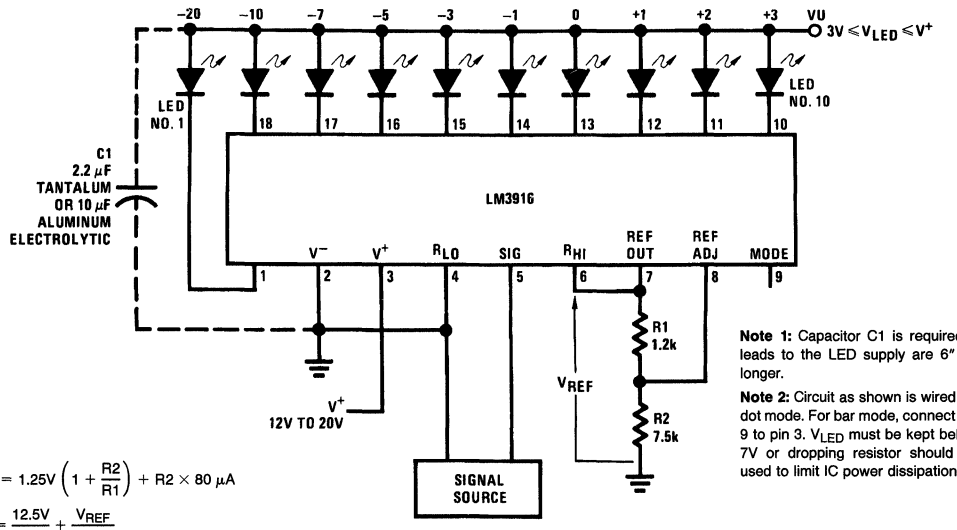
Features

- Fast responding electonic VU meter
- Drivers LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3916 is rated for operation from 0°C to +70°C. The LM3916N is available in an 18-lead molded DIP package.

Typical Applications

0V TO 10V VU Meter



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\,\mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\,k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

TL/H/7971–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
COMPARATORS					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE DIVIDER					
Divider Resistance	Total, Pin 6 to 4	8	12	17	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2) -1 dB $\le V_{IN} \le 3$ dB -7 dB $\le V_{IN} \le -1$ dB -10 dB $\le V_{IN} \le -7$ dB	 0.75 1.5 2.5	 1.0 2.0 3.0	 1.25 2.5 2.5	 dB dB dB
Absolute Accuracy	(Note 2) $V_{IN} = 2, 1, 0, -1$ dB $V_{IN} = -3, -5$ dB $V_{IN} = -7, -10, -20$ dB	 −0.25 −0.5 −1		 +0.25 +0.5 +1	 dB dB dB
VOLTAGE REFERENCE					
Output Voltage	0.1 mA$\le I_{L(REF)} \le 4$mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	0.1 mA $\le I_{L(REF)} \le 4$mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED} = 5V$		1		%
Adjust Pin Current			75	120	μA
OUTPUT DRIVERS					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA $V_{LED} = 5V$, $I_{LED} = 20$ mA		0.12 1.2	0.4 3	mA mA
LED Current Regulation	$2V \le V_{LED} \le 17V$ $I_{LED} = 2$ mA $I_{LED} = 20$ mA		0.1 1	0.25 3	mA mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	100	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10–18			0.1	100	μA
Pin 1		60	150	450	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
SUPPLY CURRENT					
Standby Supply Current	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
(All Outputs Off)	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to +3 dB = +10.000 V_{DC} at pin 5, with +10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

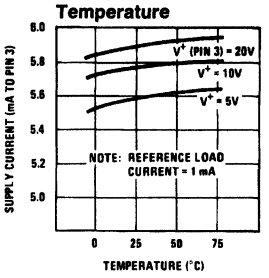
Note 5: The maximum junction temperature of the LM3916 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

LM3916 Threshold Voltage (Note 2)

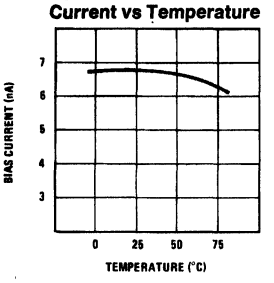
dB	Volts			dB	Volts		
	Min	Typ	Max		Min	Typ	Max
3	9.985	10.000	10.015	−3 ± ½	4.732	5.012	5.309
2 ± ¼	8.660	8.913	9.173	−5 ± ½	3.548	3.981	4.467
1 ± ¼	7.718	7.943	8.175	−7 ± 1	2.818	3.162	3.548
0 ± ¼	6.879	7.079	7.286	−10 ± 1	1.995	2.239	2.512
−1 ± ½	5.957	6.310	6.683	−20 ± 1	0.631	0.708	0.794

Typical Performance Characteristics

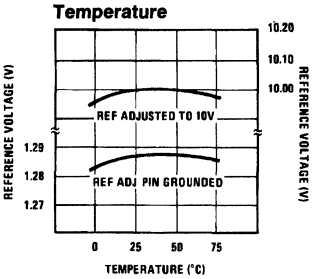
Supply Current vs Temperature



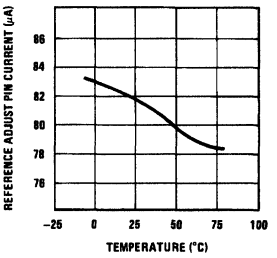
Operating Input Bias Current vs Temperature



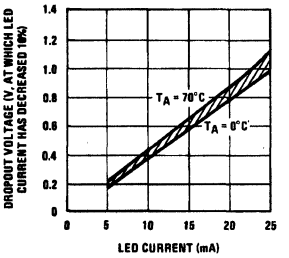
Reference Voltage vs Temperature



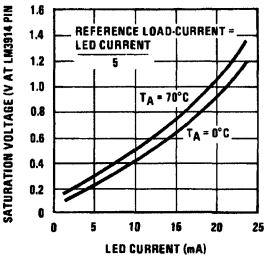
Reference Adjust Pin Current vs Temperature



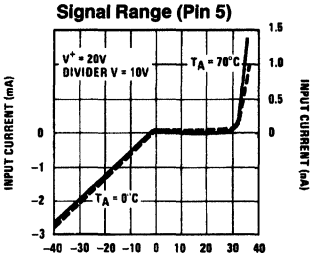
LED Current-Regulation Dropout



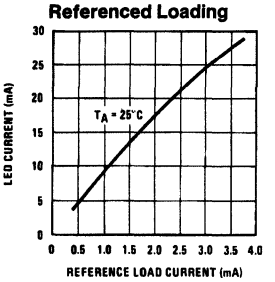
LED Driver Saturation Voltage



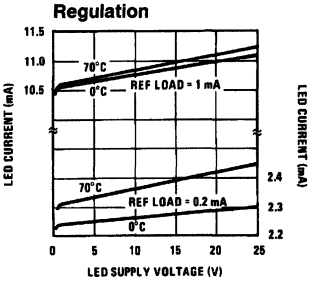
Input Current Beyond Signal Range (Pin 5)



LED Current vs Referenced Loading

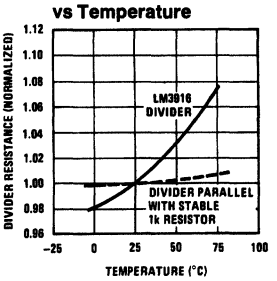


LED Driver Current Regulation

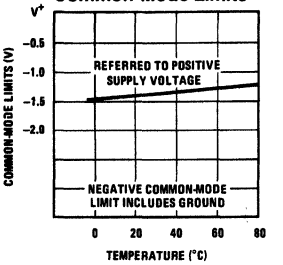


TL/H/7971–2

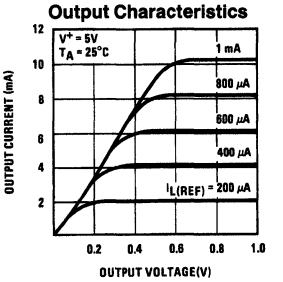
Total Divider Resistance vs Temperature



Common-Mode Limits

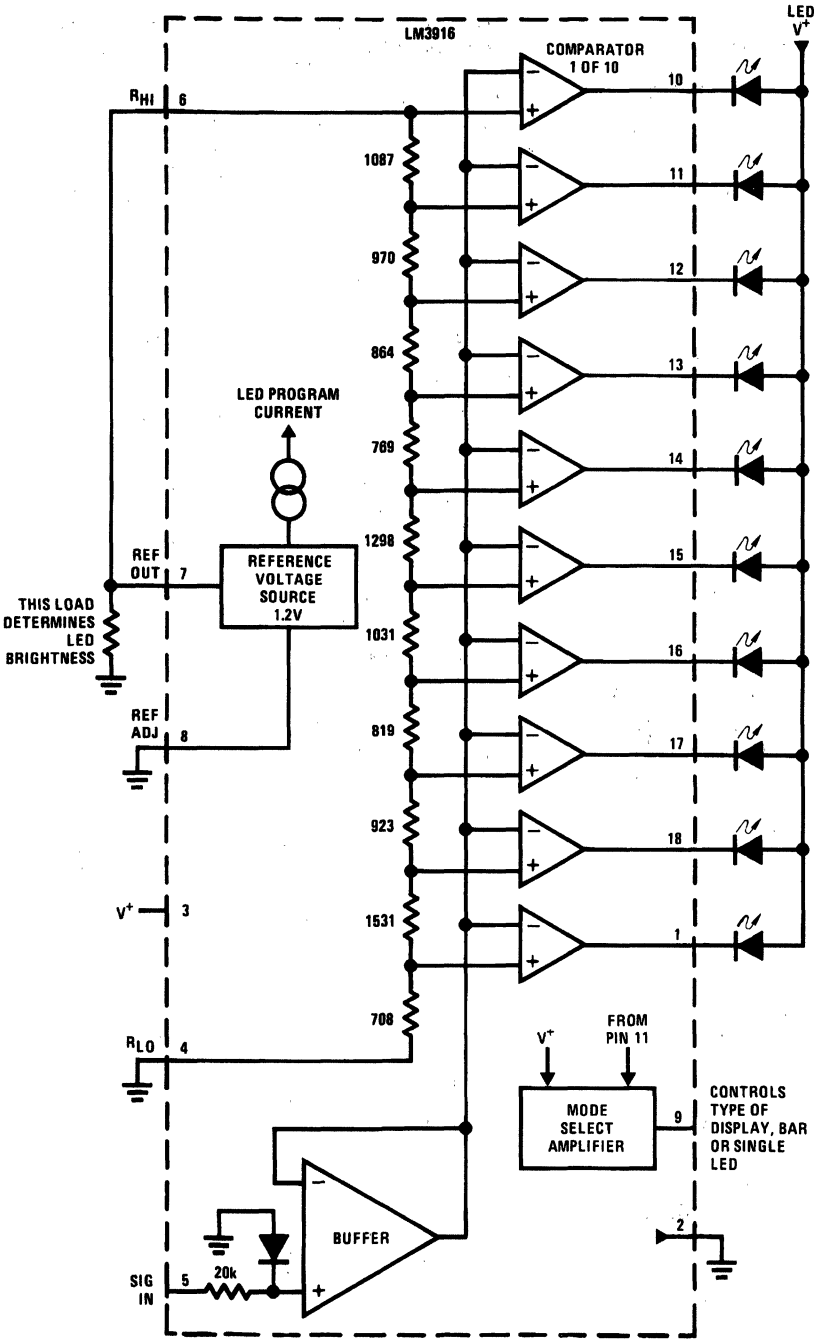


Output Characteristics



TL/H/7971–3

Block Diagram (Showing Simplest Application)



TL/H/7971–4

Functional Description

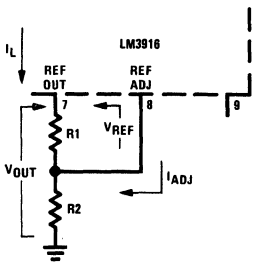
The simplified LM3916 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. As the input voltage varies from 0 to 1.25, the comparator outputs are driven low one by one, switching on the LED indicators. The resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



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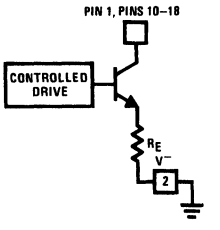
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3916 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3916 Output Circuit



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Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple devices, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

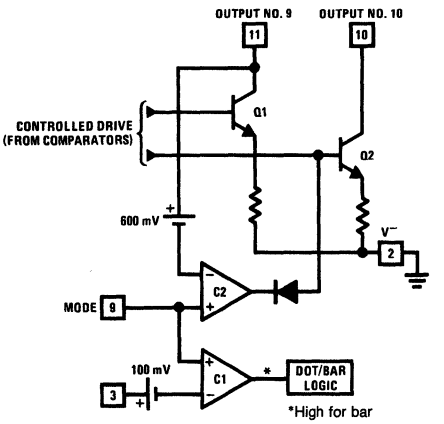
Dot Display, Single LM3916 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* drivers in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3916 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3916 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



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Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for display to make sense when multiple drivers are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted in *Figure 1.*

As long as the input signal voltage is below the threshold of the second driver, LED #11 is off. Pin 9 of driver #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of driver #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of driver #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 (and LED #1) with a 10k resistor. The 1V 1R drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

In some circuits a number of outputs on the higher device are not used. Examples include the high resolution VU meter and the expanded range VU meter circuits (see Typical Applications). To provide the proper carry sense voltage in dot mode, the LEDs of the higher driver IC are tied to V_{LED} through two series-connected diodes as shown in *Figure 2.* Shunting the diodes with a 1k resistor provides a path for driver leakage current.

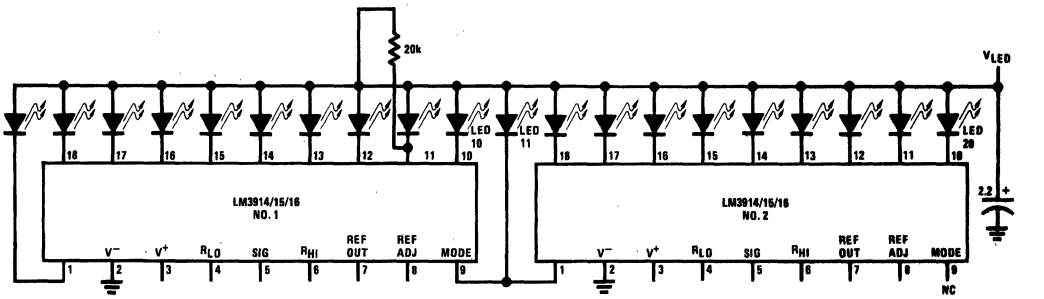

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FIGURE 1. Cascading LM3914/15/16 Series in Dot Mode

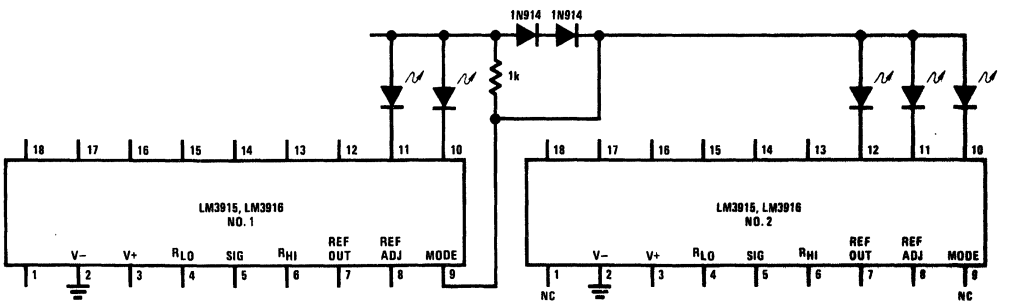

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FIGURE 2. Cascading Drivers in Dot Mode with Pin 1 of Driver #2 Unused

Mode Pin Functional Description (Continued)

OTHER DEVICE CHARACTERISTICS

The LM3915 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3915 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off the dot mode. Generally one LED fades in while the other fades out over a 1 mV range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device cascaded.

Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. The usual cure is bypassing the LED anodes with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor. If the LEd anode line wiring is inaccessible, often a 0.1 μF capacitor from pin 1 to pin 2 will be sufficient.

If there is a large amount of LED overlap in the bar mode, oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. When several LEDs are lit in dot mode, the problem is usually an AC component of the input signal which should be filtered out. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with 0.1 μF.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum or 10 μF aluminum electrolytic capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

The simplest way to display an AC signal using the LM3916 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3916 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). A smear or bar type display results even though the LM3916 is connected for dot mode. The LEDs should be run at 20 mA to 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3916 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 3* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3916 is used for a 23 dB display.

Display circuits such as the extended range VU meter using two or more drivers for a dynamic range of 40 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 4* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353 or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

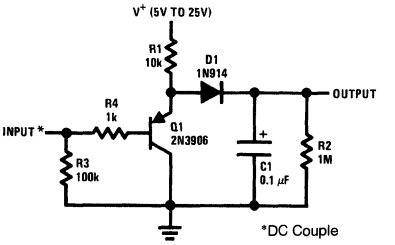

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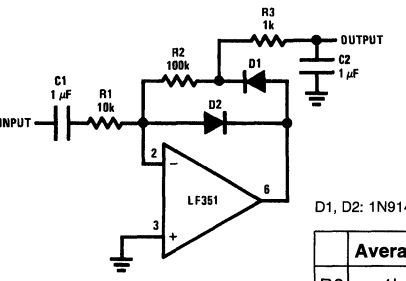
FIGURE 3. Half-Wave Peak Detector



D1, D2: 1N914 or 1N4148

	Average	Peak
R2	1k	100k
R3	100k	1k

R1 = R2 for A_V = 1
R1 = R2/10 for A_V = 10
C1 = 10/R1

TL/H/7971–11

FIGURE 4. Precision Half-Wave Rectifier

Application Hints (Continued)

For precision full-wave averaging use the circuit in *Figure 5.* Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5•C2. A simple modification results in the precision full-wave detector of *Figure 6.* Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3916.

AUDIO METER STANDARDS

VU Meter

The audio level meter most frequently encountered is the VU meter. Its characteristics are defined as the ANSI specification C165. The LM3916's outputs correspond to the meter indications specified with the omission of the −2 VU indication. The VU scale divisions differ slightly from a linear scale in order to obtain whole numbers in dB.

Some of the most important specifications for an AC meter are its dynamic characteristics. These define how the meter responds to transients and how fast the reading decays. The VU meter is a relatively slow full-wave averaging type, specified to reach 99% deflection in 300 ms and overshoot by 1 to 1.5%. In engineering terms this means a slightly underdamped second order response with a resonant frequency of 2.1 Hz and a Q of 0.62. *Figure 7* depicts a simple rectifier/filter circuit that meets these criteria.

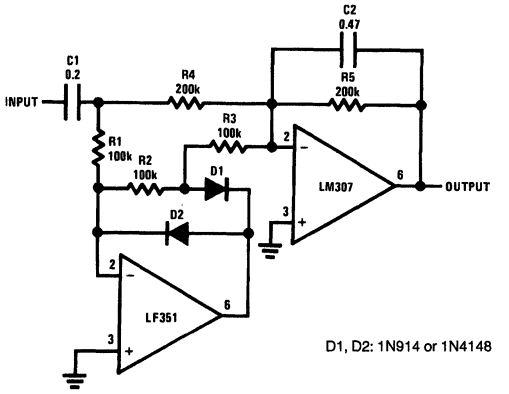


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FIGURE 5. Precision Full-Wave Average Detector

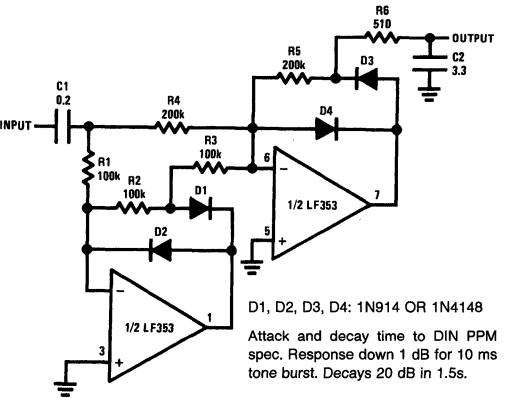

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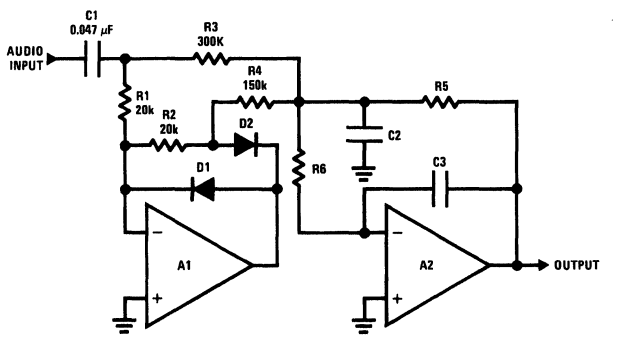
FIGURE 6. Precision Full-Wave Peak Detector



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GAIN	R5	R6	C2	C3
1	100k	43k	2.0	0.56 μF
10	1M	100k	1.0	0.056 μF

Design Equations

$$\frac{1}{R5 \bullet R6 \bullet C2 \bullet C3} = \omega_0^2 = 177 \text{ sec}^{-2}$$

$$\frac{1}{C2}\left(\frac{1}{R3}+\frac{1}{R4}+\frac{1}{R5}+\frac{1}{R6}\right) = \frac{\omega_0}{Q} = 21.5 \text{ sec}^{-1}$$

$R3 = 2R4$

$R1 = R2 \ll R4$

A1, A2: ½ LF353

D1, D2: 1N914 OR 1N4148

*Reaches 99% level at 300 ms after applied tone burst and overshoots 1.2%.

FIGURE 7. Full-Wave Average Detector to VU Meter Specifications*

Application Hints (Continued)

Peak Program Meter

The VU meter, originally intended for signals sent via telephone lines, has shortcomings when used in high fidelity systems. Due to its slow response time, a VU meter will not accurately display transients that can saturate a magnetic tape or drive an amplifier into clipping. The fast-attack peak program meter (PPM) which does not have this problem is becoming increasingly popular.

While several European organizations have specifications for peak program meters, the German DIN specification 45406 is becoming a de facto standard. Rather than respond instantaneously to peak, however, PPM specifications require a finite "integration time" so that only peaks wide enough to be audible are displayed. DIN 45406 calls for a response of 1 dB down from steady-state for a 10 ms tone burst and 4 dB down for a 3 ms tone burst. These requirements are consistent with the other frequently encountered spec of 2 dB down for a 5 ms burst and are met by an attack time constant of 1.7 ms.

The specified return time of 1.5s to −20 dB requires a 650 ms decay time constant. The full-wave peak detector of *FIGURE 6* satisfies both the attack and decay time criteria.

Cascading The LM3916

The LM3916 by itself covers the 23 dB range of the conventional VU meter. To display signals of 40 dB or 70 dB dynamic range, the LM3916 may be cascaded with the 3 dB/step LM3915s. Alternatively, two LM3916s may be cascaded for increased resolution over a 28 dB range. Refer to the Extended Range VU Meter and High Resolution VU Meter in the Typical Applications section for the complete circuits for both dot and bar mode displays.

To obtain a display that makes sense when an LM3915 and an LM3916 are cascaded, the −20 dB output from the LM3916 is dropped. The full-scale display for the LM3915 is set at 3 dB below the LM3916's −10 dB output and the rest of the thresholds continue the 3 dB/step spacing. A simple, low cost approach is to set the reference voltage of the two chips 16 dB apart as in *Figure 5*. The LM3915, with pin 8 grounded, runs at 1.25V full-scale. R1 and R2 set the LM3916's reference 16 dB higher or 7.89V. Variation in the two on-chip references and resistor tolerance may cause a ± 1 dB error in the −10 dB to −13 dB transition. If this is objectionable, R2 can be trimmed.

The drawback of the aforementioned approach is that the threshold of LED #1 on the LM3915 is only 56 mV. Since comparator offset voltage may be as high as 10 mV, large errors can occur at the first few thresholds. A better approach, as shown in *Figure 9,* is to keep the reference the same for both drivers (10V in the example) and *amplify* the input signal by 16 dB ahead of the LM3915. Alternatively,

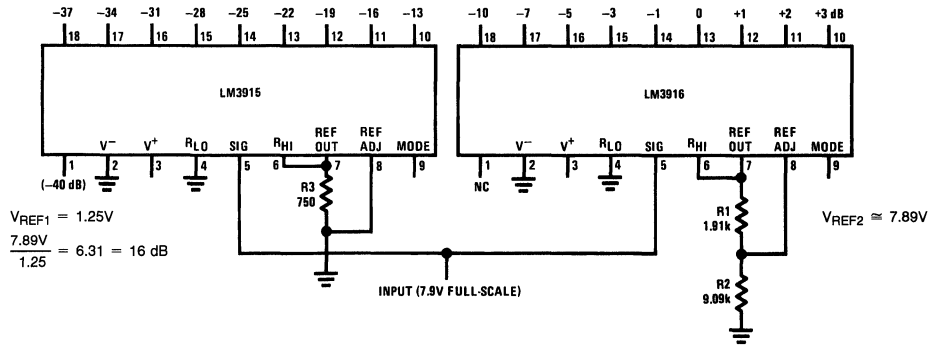

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FIGURE 8. Low Cost Circuit for 40 dB Display

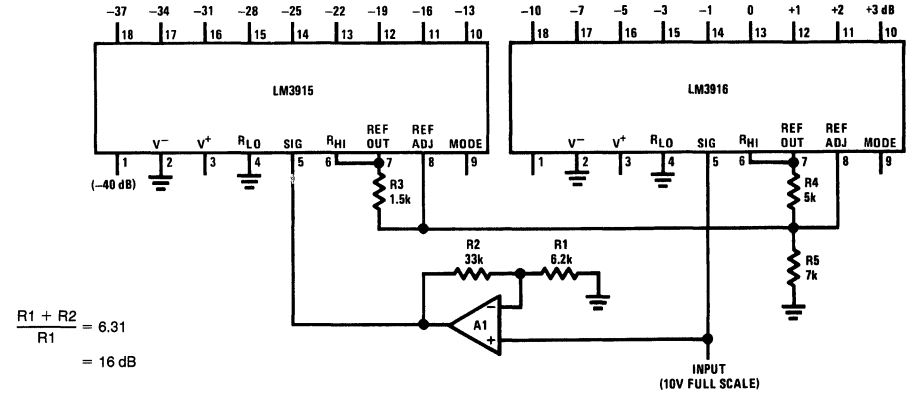

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FIGURE 9. Improved Circuit for 40 dB Display

Application Hints (Continued)

instead of amplifying, input signals of sufficient amplitude can be fed directly to the LM3916 and *attenuated* by 16 dB to drive the LM3915.

To extend this approach to get a 70 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 2 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

Single Driver

The equations in *Figure 10* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 1 mA to flow from pin 7 into the divider which means that the LED current will be at least 10 mA. R1 will typically be between 1 kΩ and 5 kΩ. To trim the reference voltage, vary R2.

The current in *Figure 11* shows how to add a LED intensity control which can vary LED current from 5 mA to 28 mA. Choosing V_{REF} = 5V lowers the current drawn by the ladder, increasing the intensity adjustment range. The reference adjustment has some effect on LED intensity but the reverse is not true.

Multiple Drivers

Figure 12 shows how to obtain a common reference trim and intensity control for two drivers. The two ICs may be connected in cascade or may be handling separate channels for stereo. This technique can be extended for larger numbers of drivers by varying the values of R1, R2 and R3. Because the LM3915 has a greater ladder resistance, R5 was picked less than R7 in such a way as to provide equal reference load currents. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.2 dB for V_{REF} = 5V.

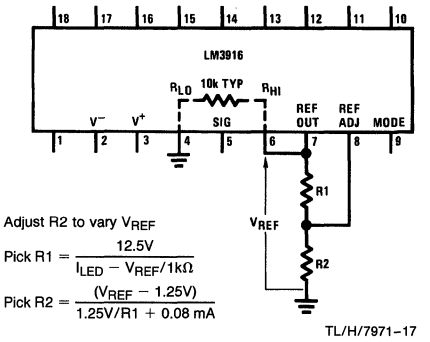


FIGURE 10. Design Equations for Fixed LED Intensity

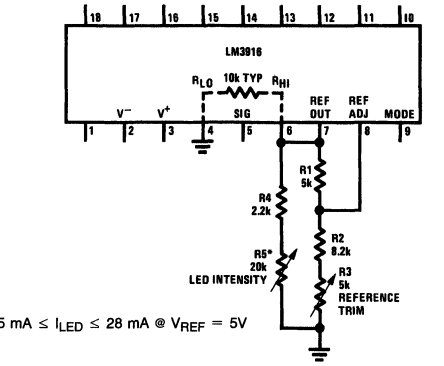


FIGURE 11. Varying LED Intensity

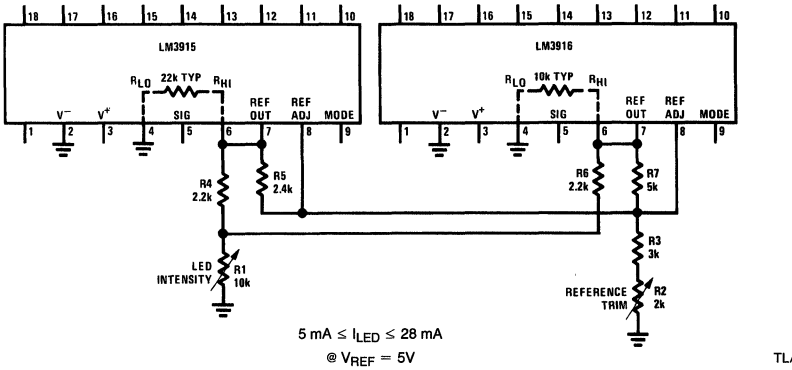


FIGURE 12. Independent Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

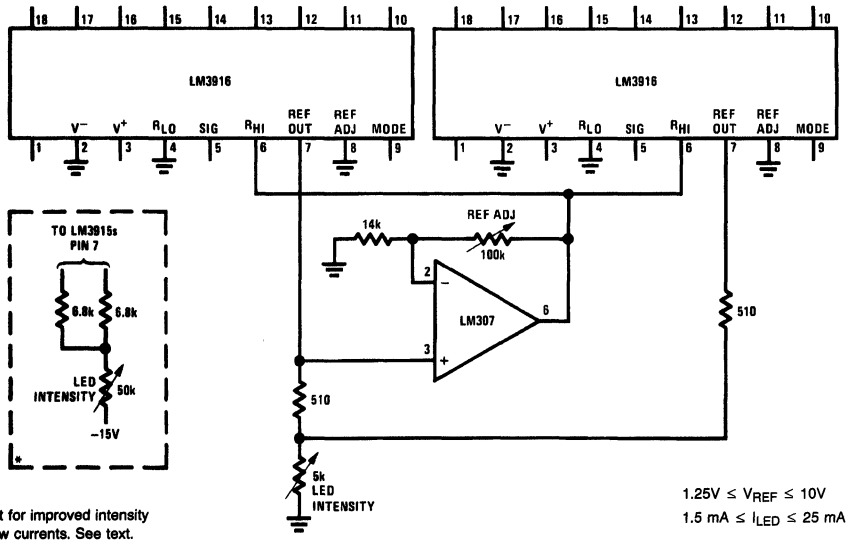
Application Hints (Continued)

The scheme in *Figure 13* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 25 mA.

At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by superimposing an AC waveform on top of the input level as shown in *Figure 14*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.



*Optional circuit for improved intensity matching at low currents. See text.

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FIGURE 13. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

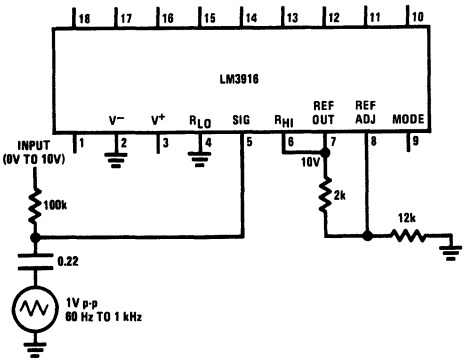

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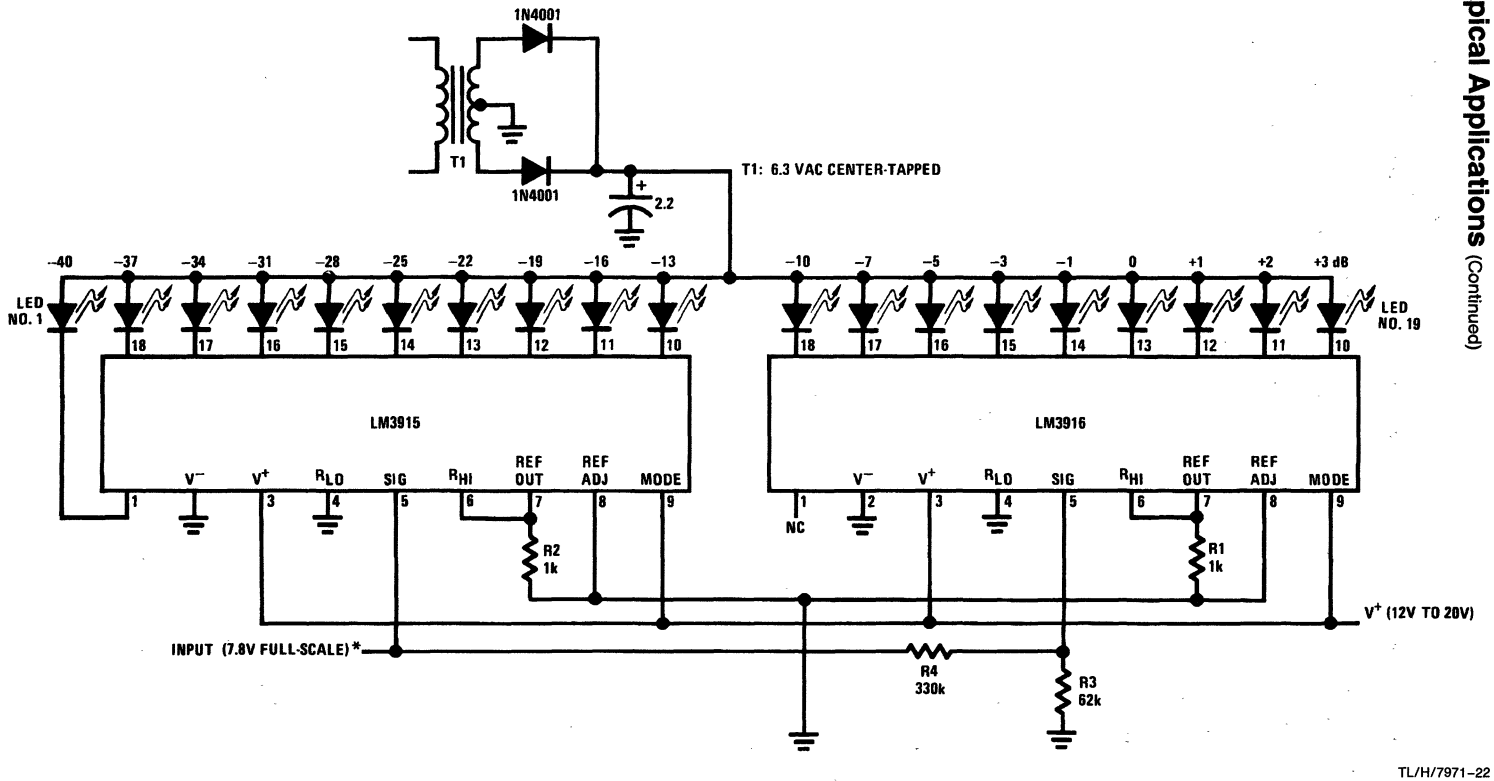
FIGURE 14. 0V to 10V VU Meter with Smooth Transitions

Typical Applications (Continued)

Extended Range VU Meter (Bar Mode)



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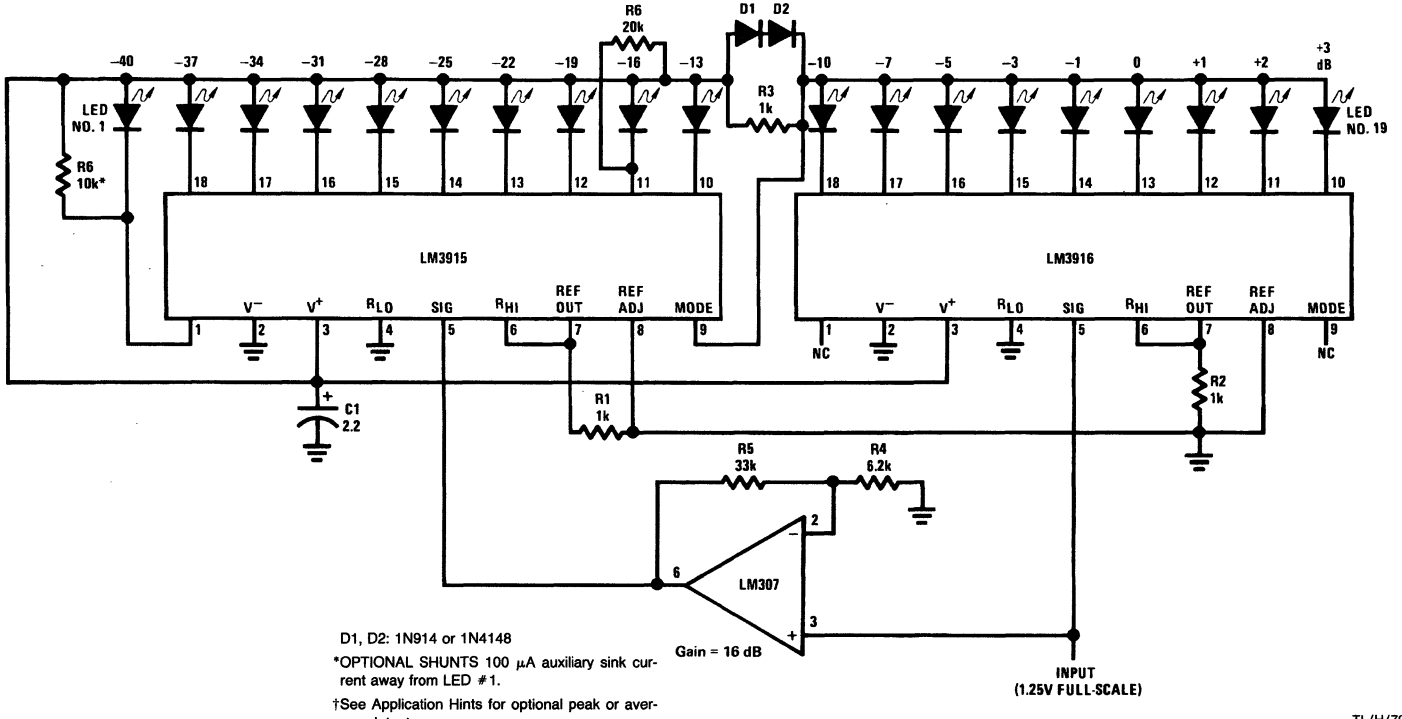
This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12

$$\frac{R3}{R3 + R4} = 0.158 = -16\ dB$$

Extended Range VU Meter (Dot Mode)



D1, D2: 1N914 or 1N4148

*OPTIONAL SHUNTS 100 μA auxiliary sink current away from LED #1.

†See Application Hints for optional peak or average detector.

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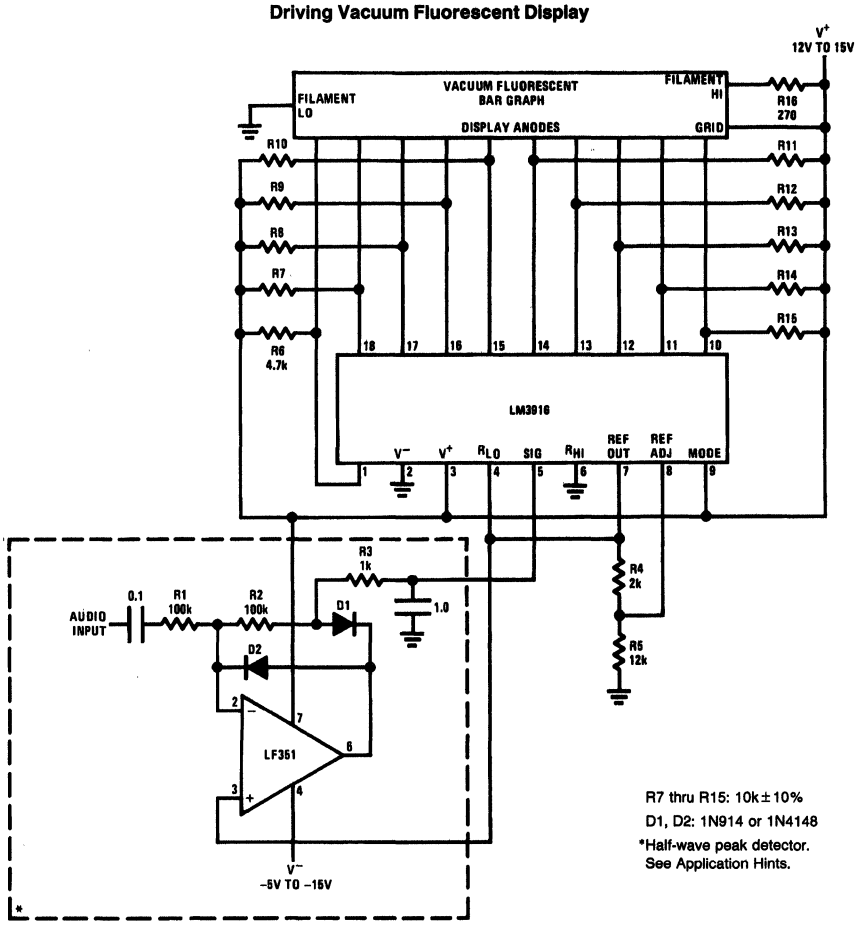
Typical Applications (Continued)

Driving Vacuum Fluorescent Display



R7 thru R15: 10k±10%

D1, D2: 1N914 or 1N4148

*Half-wave peak detector. See Application Hints.

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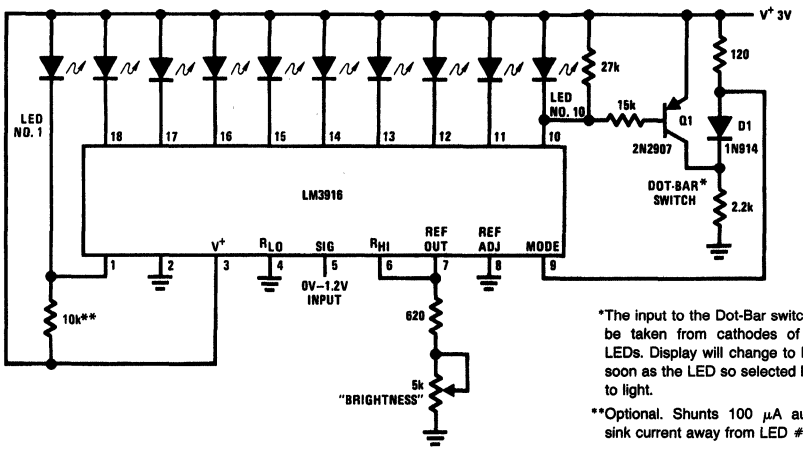
Indicator and Alarm, Full-Scale Changes Display From Dot to Bar

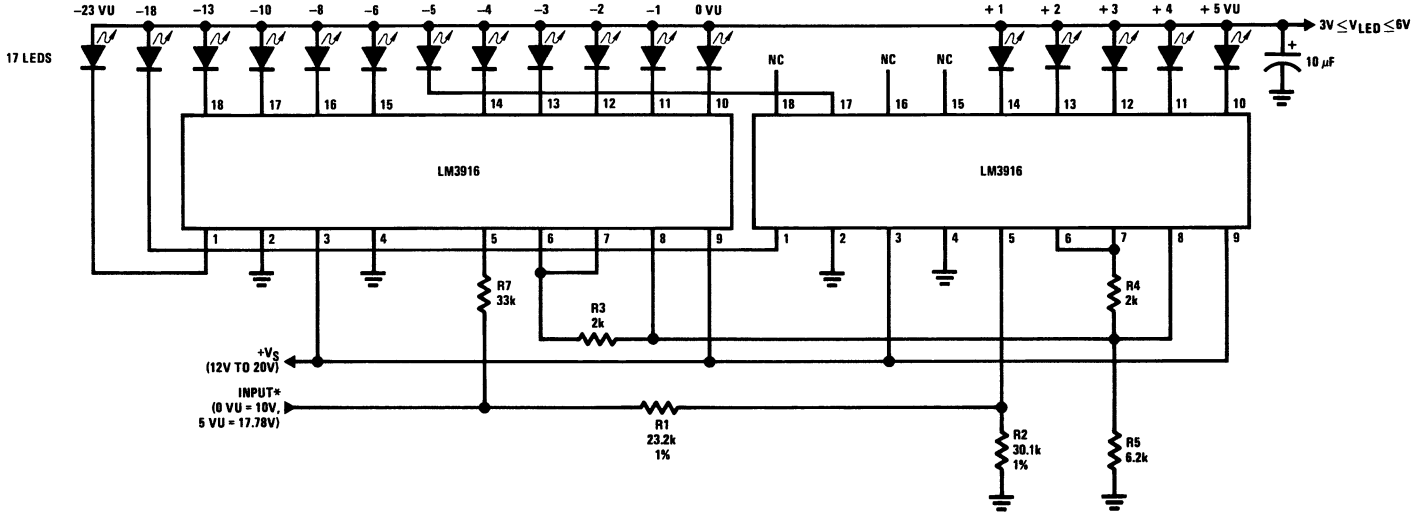


*The input to the Dot-Bar switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

**Optional. Shunts 100 μA auxiliary sink current away from LED #1.

TL/H/7971–25

High Resolution VU Meter (Bar Mode)



TL/H/7971–26

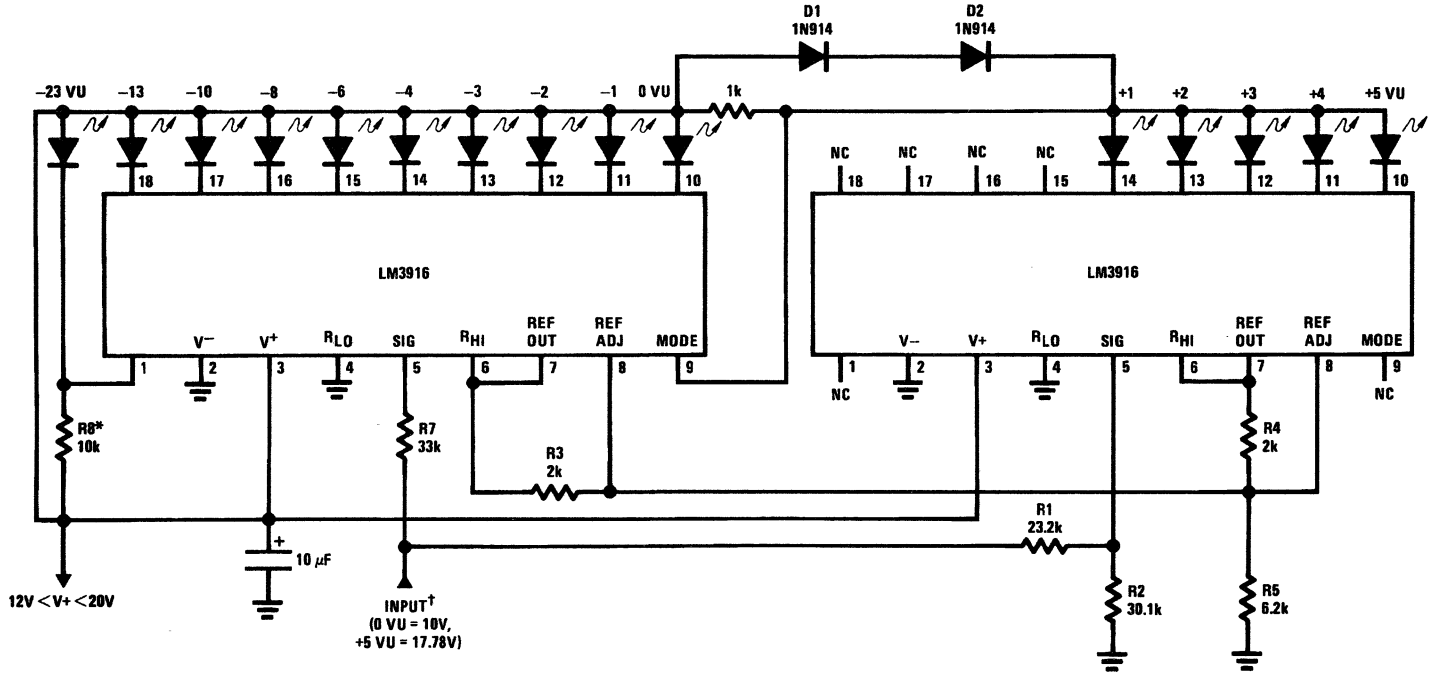
*See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ dB$$

or $R1 \cong 0.788 \bullet R2$

Typical Applications (Continued)

High Resolution VU Meter (Dot Mode)



TL/H/7971–27

*Optional shunts 100 µA auxiliary sink current away from LED #1.

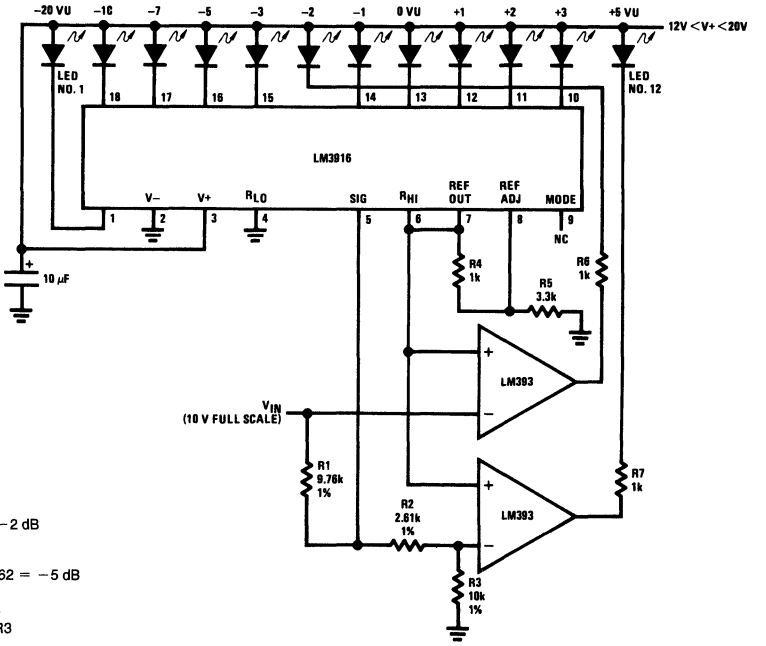
†See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ dB$$

$$\text{or } R1 \cong 0.788 \bullet R2$$

Typical Applications (Continued)

Displaying Additional Levels



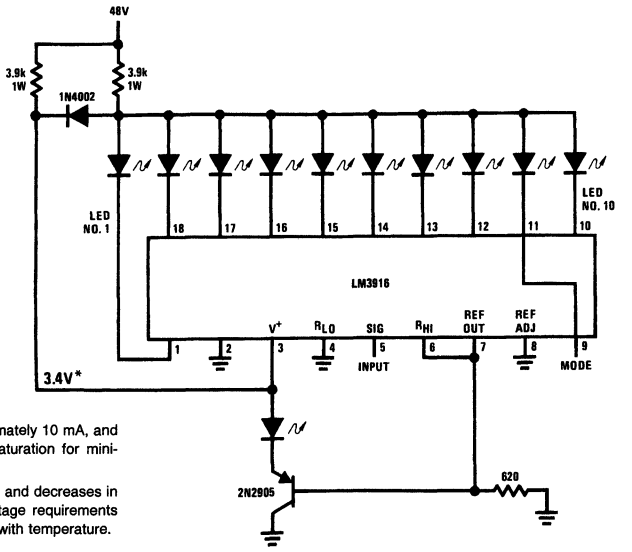
$$\frac{R3}{R2 + R3} \cong 0.794 = -2\ dB$$

$$\frac{R2 + R3}{R1 + R2 + R3} \cong 0.562 = -5\ dB$$

or R2 = 0.259 • R3
and R1 = 0.979 • R3

TL/H/7971–28

Operating with a High Voltage Supply (Dot Mode Only)



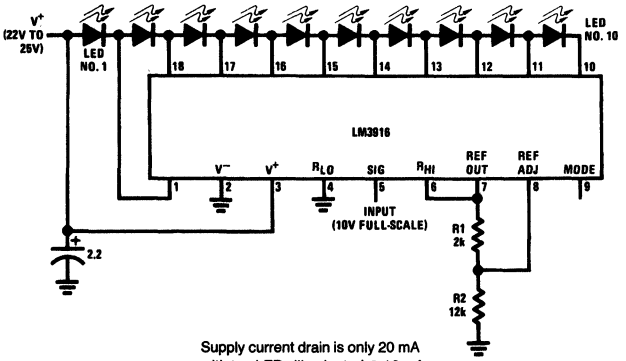
The LED currents are approximately 10 mA, and LM3916 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3916 also decrease with temperature.

TL/H/7971–29

Typical Applications (Continued)

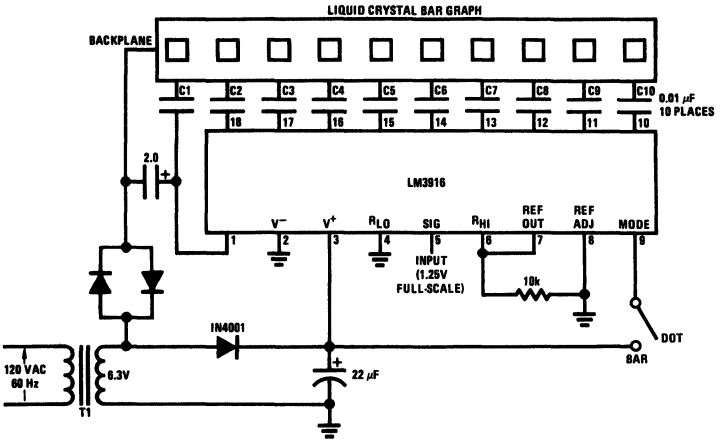
Low Current Bar Mode Display



Supply current drain is only 20 mA with ten LEDs illuminated @ 16 mA.

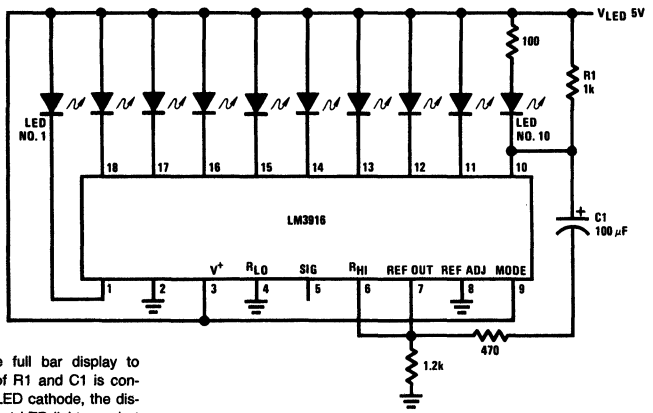
TL/H/7971–30

Driving Liquid Crystal Display



TL/H/7971–31

Bar Display with Alarm Flasher

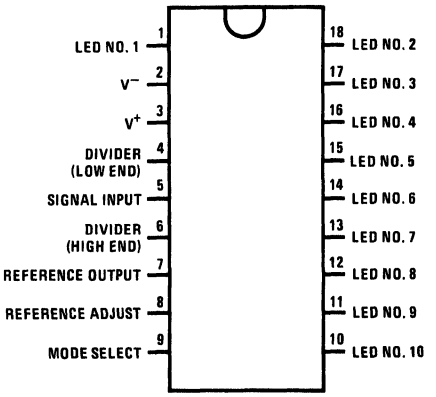


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7971–32

Connection Diagram

Dual-In-Line Package



TL/H/7971–33

Top View

Order Number LM3916N
See NS Package Number N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference amplifier pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Section 5

Clock Drivers

Section 5 Contents

National Semiconductor

Clock Drivers

Temperature Range		Driver/ Package	TRI-STATE®/ Strobed	Output High Voltage (V)	Propagation Delay Typ. (ns)	Capacitive Load (PS)	Supply Current (mA)
0°C to +70°C	−55°C to +125°C						
DS0026C	DS0026	2		20	7.5	1000	80
DS0056C	DS0056	2		20	7.5	1000	80
DS75325	DS55325	4		24	25	25	70
DS75361		2	STROBED	24	11	390	24
DS75365		4	STROBED	24	31	200	47

National Semiconductor

DS0025C Two Phase MOS Clock Driver

General Description

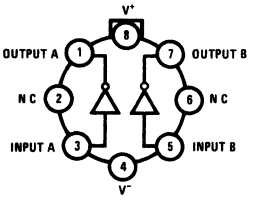
The DS0025C is a monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL line drivers or buffers such as the DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse width may be set by selection of the input capacitor eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead or 14-lead dual-in-line package
- High Output Voltage Swings—up to 25V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DS8830, DM7440
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package



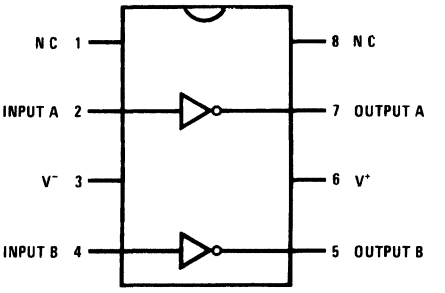
TL/F/5852–1

Note: Pin 4 connected to case.

Top View

Order Number DS0025CH
See NS Package Number H08C

Dual-In-Line Package

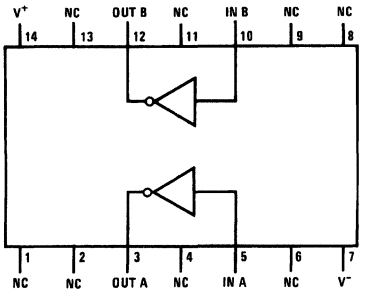


TL/F/5852–2

Top View

Order Number DS0025CJ-8
or DS0025CN
See NS Package Number J08A or N08E

Dual-In-Line Package



TL/F/5852–3

Top View

Order Number DS0025CJ
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$(V^+ - V^-)$Voltage Differential	25V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Recommended Operating Conditions

V^+ V^- Differential Voltage 20V

	Min	Max
Temperature	0	70

Maximum Power Dissipation* at 25°C

8-Pin Cavity Package	1150 mW
14-Pin Cavity Package	1410 mW
Molded Package	1080 mW
Metal Can (TO-5) Package	670 mW

* Derate 8-pin cavity package 7.8 mW/°C above 25°C; derate 14-pin cavity package 9.5 mW/°C above 25°C; derate molded package 8.7 mW/°C above 25°C; derate metal can (TO-5) package 4.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) See test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{d\,ON}$	Turn-On Delay Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF			25	50	ns
$t_{d\,OFF}$	Turn-Off Delay Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF	(Note 4)	60	90	120	ns
			(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001 μF, R_{IN} = 0Ω, C_L = 0.001 μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA		$V^+ - 1.0$	$V^+ - 0.7V$		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			$V^- + 0.7V$	$V^- + 1.5V$	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

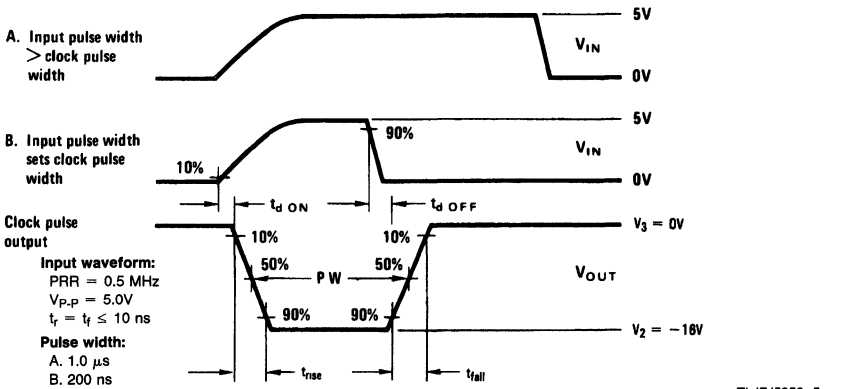
Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C range for the DS0025C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

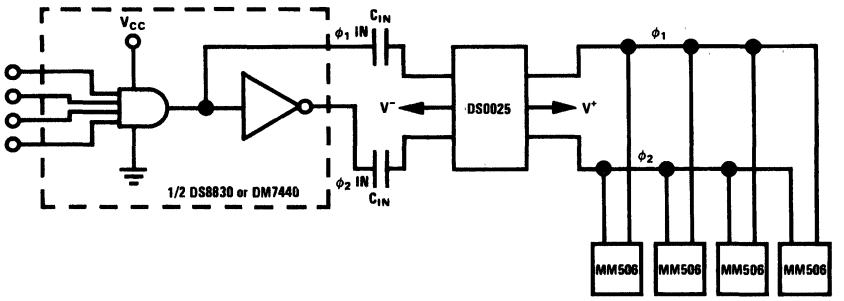
Note 5: Parameter values for input width greater than output clock pulse width.

Timing Diagram



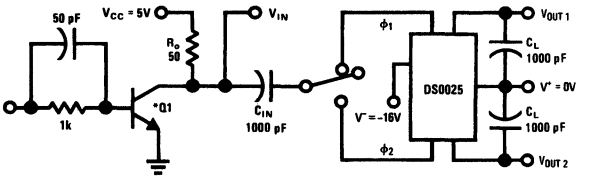
TL/F/5852–5

Typical Application



TL/F/5852–4

AC Test Circuit

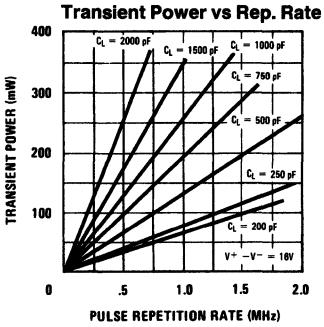


TL/F/5852–6

*Q1 is selected high speed NPN switching transistor.

Typical Performance

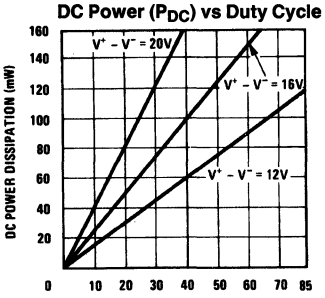
Transient Power vs Rep. Rate



TL/F/5852–7

$$P_{AC} = (V^+ - V^-)^2 f C_L$$

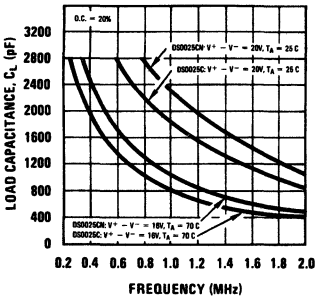
DC Power (P_{DC}) vs Duty Cycle



TL/F/5852–8

$$P_{DC} = \frac{V^+ - V^-)^2\ (DC)}{1k}$$

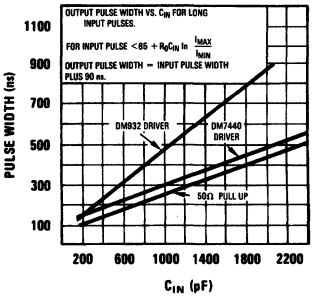
Maximum Load Capacitance



TL/F/5852–9

$$C_L < \frac{(P_{MAX})\ (1k) - (V^+ - V^-)^2\ (DC)}{(f)\ (1k)\ (V^+ - V^-)^2} < \frac{(I_{pk})\ (t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



TL/F/5852–10

I_{MAX} = Peak Current delivered by driver

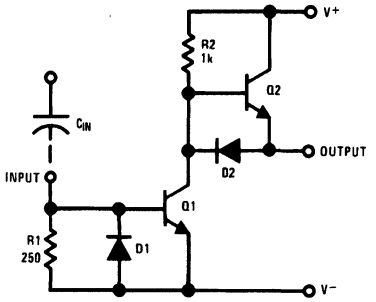
$$I_{MIN} \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

Applications Information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.



TL/F/5852–11

FIGURE 1. DS0025 Schematic (One-Half Circuit)

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \quad (1)$$

Typical rise times into 1000 pF load is 25 ns. For $V^+ - V^- = 20V$, $I = 0.8A$.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \quad (2)$$

For $V^+ - V^- = 20V$, $f = 1.0$ MHz, $C_L = 1000$ pF, $P_{AC} = 400$ mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \quad (3)$$

$= 80$ mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power.

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30–50 ns and 16V amplitude over the temperature range 0°–70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power.

385 mW = transient output power.

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

For further information please refer to National Semiconductors Application Note AN-76.

National Semiconductor

DS0026/DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to ($V^+ - 0.1V$) in the off state.

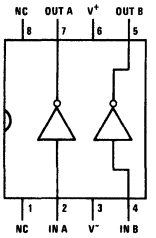
For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagrams (Top Views)

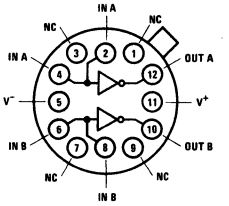
Dual-In-Line Package



TL/F/5853-2

Order Number DS0026CJ-8, DS0026CL or DS0026CN See NS Package Number J08A or N08E

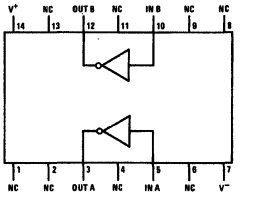
TO-8 Package



TL/F/5853-3

Order Number DS0026G or DS0026CG See NS Package Number G12B

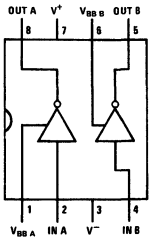
Dual-In-Line Package



TL/F/5853-4

Order Number DS0026J or DS0026CJ See NS Package Number J14A

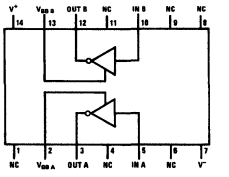
Dual-In-Line Package



TL/F/5853-6

Order Number DS0056CN See NS Package Number N08E

Dual-In-Line Package



TL/F/5853-7

Order Number DS0056J or DS0056CJ See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
EIAJ SO Package	800 mW
Operating Temperature Range	
DS0026, DS0056	−55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

* Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C; derate EIAJ SO package 5.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_{OL} = 1$ mA			$V^- + 0.7$	$V^- + 1.0$	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{SS} \geq V^+ + 1.0V$, $I_{OH} = -1$ mA	DS0026	$V^+ - 1.0$	$V^+ - 0.8$		V
			DS0056	$V^+ - 0.3$	$V^+ - 0.1$		V
$I_{CC(ON)}$	"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$	DS0026		30	40	mA
	(one side on)	(Note 6)	DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics ($T_A = 25°C$) (Notes 5 and 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{ON}	Turn-On Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-Off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		15	18	ns
			$C_L = 1000$ pF		20	35	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		30	40	ns
			$C_L = 1000$ pF		36	50	ns
t_f	Fall Time	*(Figure 1)*, (Note 5)	$C_L = 500$ pF		12	16	ns
			$C_L = 1000$ pF		17	25	ns
		(Figure 2), (Note 5)	$C_L = 500$ pF		28	35	ns
			$C_L = 1000$ pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

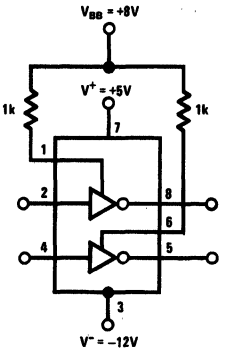
Note 4: All typical values for $T_A = 25°C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1$ kΩ (for one side) when output is low.

Note 7: The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Typical V_{BB} Connection



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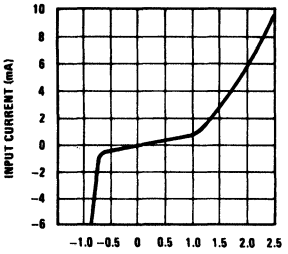
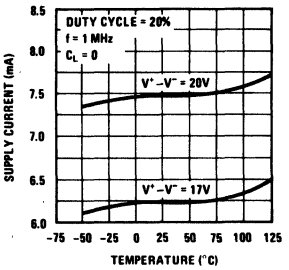
Typical Performance Characteristics

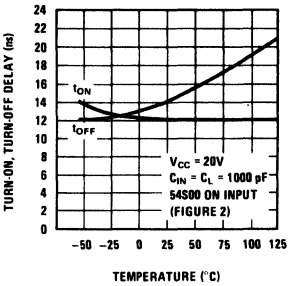
Input Current vs Input Voltage



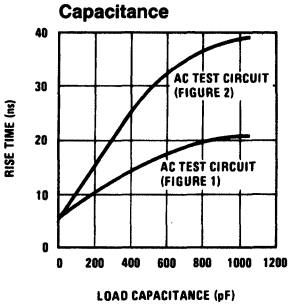
Supply Current vs Temperature



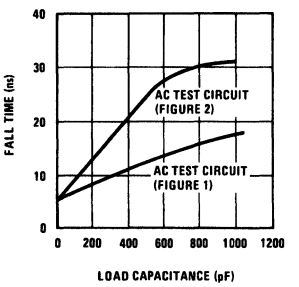
Turn-On and Turn-Off Delay vs Temperature



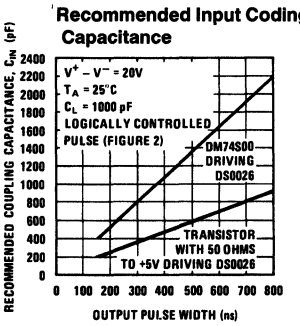
Rise Time vs Load Capacitance



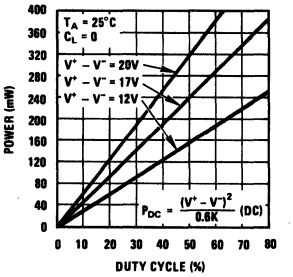
Fall Time vs Load Capacitance



Recommended Input Coding Capacitance



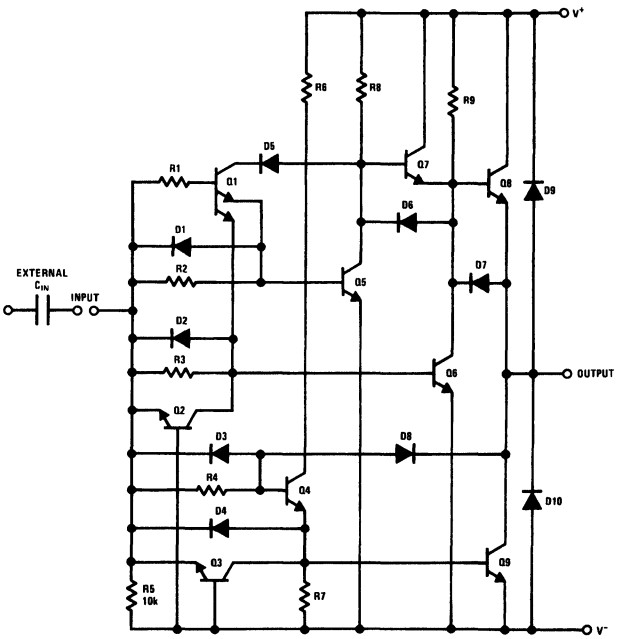
DC Power (P_{DC}) vs Duty Cycle



TL/F/5853–9

Schematic Diagrams

1/2 DS0026



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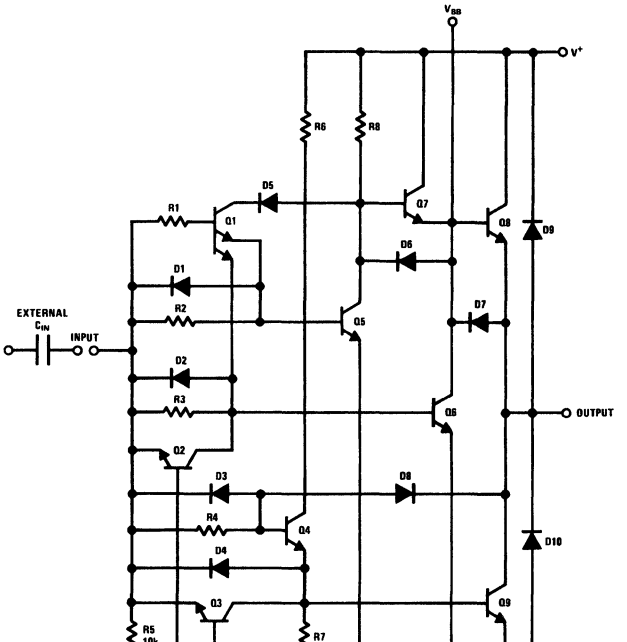
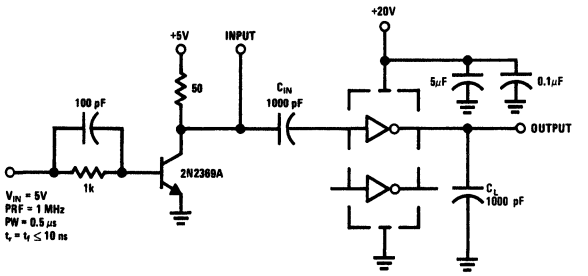
1/2 DS0056



TL/F/5853–11

AC Test Circuits and Switching Time Waveforms



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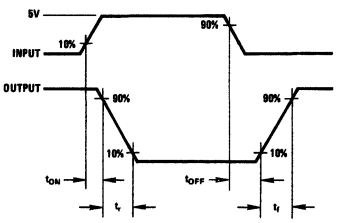

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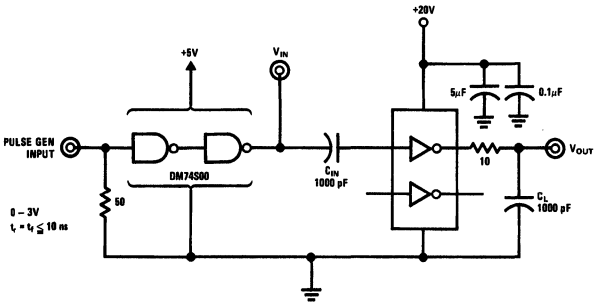
FIGURE 1



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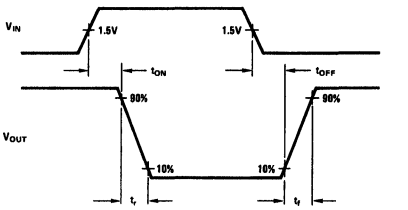

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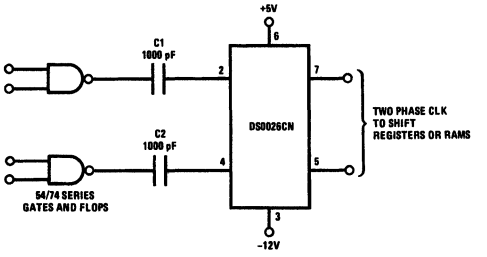
FIGURE 2

Typical Applications

AC Coupled MOS Clock Driver



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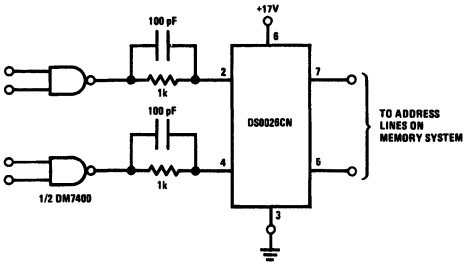
DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



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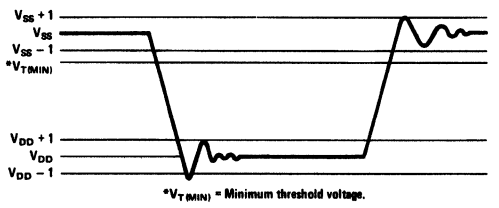
Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Application Hints (Continued)

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock specification, in diagram form, with idealized ringing sketched in. The



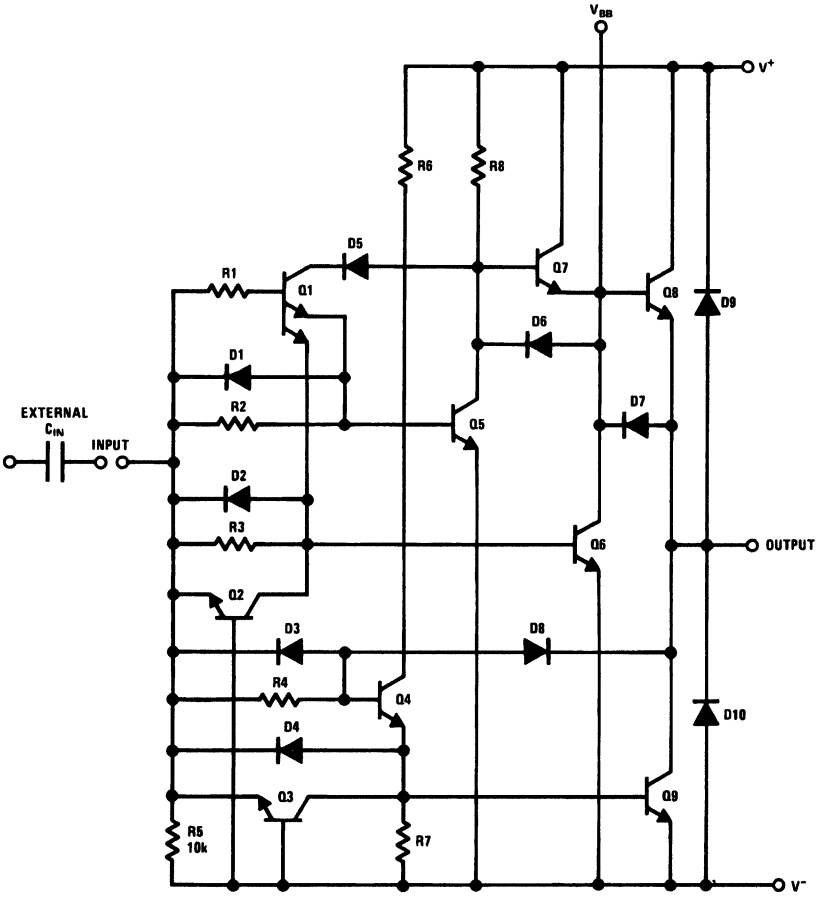
TL/F/5853–18

FIGURE 6. Clock Waveform

ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damp-



TL/F/5853–11

FIGURE 7. Schematic of 1/2 DS0056

Application Hints (Continued)

ing resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

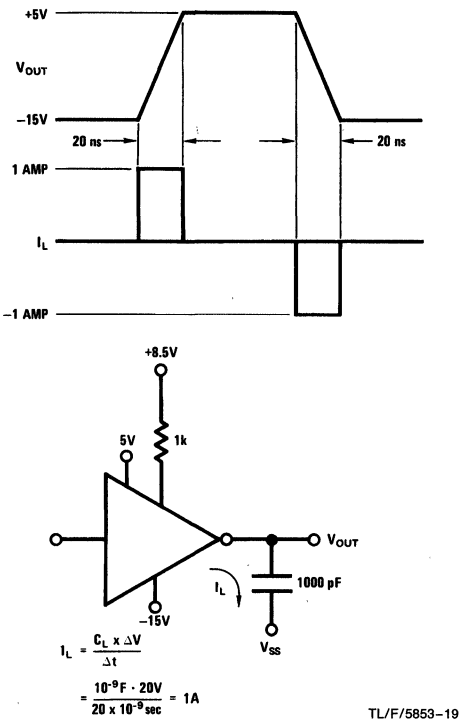
In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q8 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the V_{SS} − 1.0V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q8 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin on this line to zero.

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L.



TL/F/5853–19

FIGURE 8. Clock Waveforms (Voltage and Current)

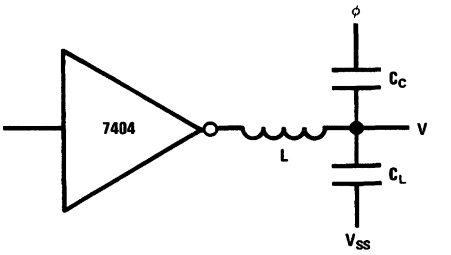


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FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of

Application Hints (Continued)

noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

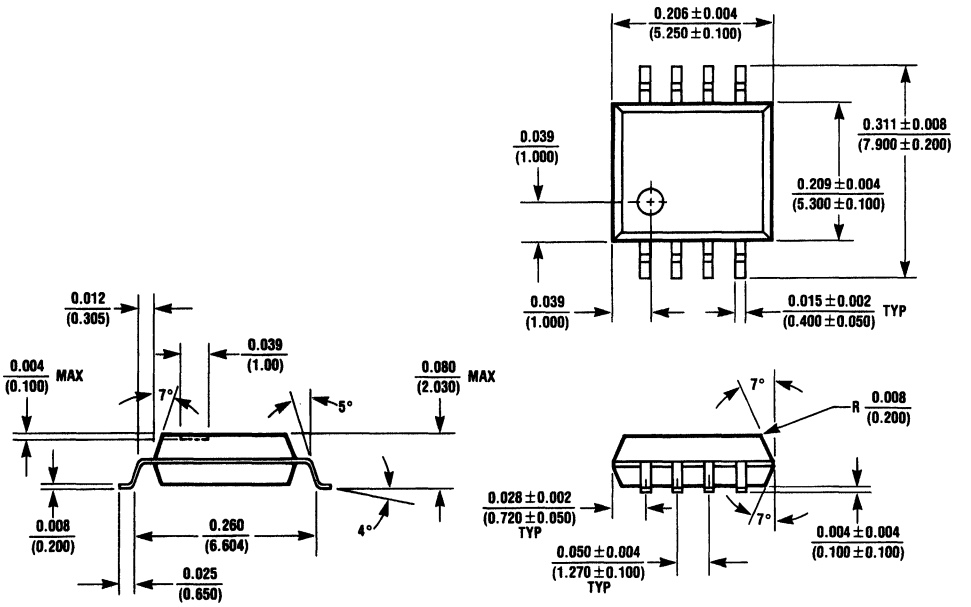
$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

Packaging Information



TL/F/5853–21

8-Lead Surface Mount Package
Order Number DS0026CL

National Semiconductor

DS75325
Memory Drivers

General Description

The DS75325 is a monolithic memory driver which features high current outputs as well as internal decoding of logic inputs. This circuit is designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

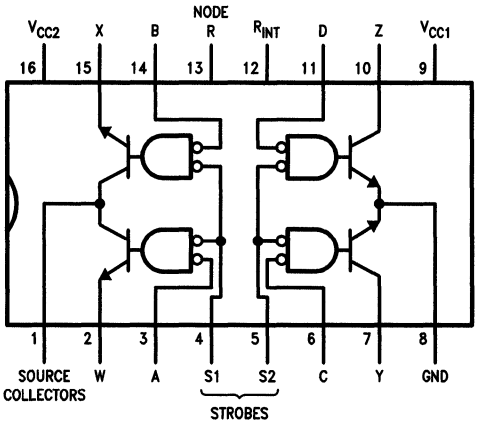
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally, activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

Features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- TTL compatible

Connection Diagram

Dual-In-Line Package



TL/F/9755–2

Top View

Order Number DS75325N
See NS Package Number N14A

Truth Table

Address Inputs				Strobe Inputs		Outputs			
Source		Sink		Source	Sink	Source		Sink	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = High Level, L = Low Level, X = Irrelevant

Note: Not more than one output is to be on at any one time.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC1} (Note 5)	7V
Supply Voltage V_{CC2} (Note 5)	25V
Input Voltage (Any Address or Strobe Input)	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate Cavity Package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Temperature (T_A)			
DS75325	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	*(Figures 1 and 2)*			2			V
V_{IL}	Low Level Input Voltage	*(Figures 3 and 4)*					0.8	V
V_I	Input Clamp Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C *(Figure 5)*				−1.3	−1.7	V
I_{OFF}	Source Collectors Terminal "Off" State Current	V_{CC1} = 4.5V, V_{CC2} = 24V *(Figure 1)*	Full Range	DS55325			500	μA
				DS75325			200	μA
			T_A = 25°C	DS55325		3	150	μA
				DS75325		3	200	μA
V_{OH}	High Level Sink Output Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0 mA *(Figure 2)*			19	23		V
V_{SAT}	Saturation Voltage Source Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA *(Figure 3)* (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
V_{SAT}	Saturation Voltage Sink Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA *(Figure 4)* (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
I_I	Input Current at Maximum Input Voltage	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V *(Figure 5)*	Address Inputs				1	mA
			Strobe Inputs				2	mA
I_{IH}	High Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V *(Figure 5)*	Address Inputs			3	40	μA
			Strobe Inputs			6	80	μA
I_{IL}	Low Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V *(Figure 5)*	Address Inputs			−1	−1.6	mA
			Strobe Inputs			−2	−3.2	mA
$I_{CC\ OFF}$	Supply Current, All Sources and Sinks "Off"	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C *(Figure 6)*	V_{CC1}			14	22	mA
			V_{CC2}			7.5	20	mA
I_{CC1}	Supply Current from V_{CC1}, Either Sink "On"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C *(Figure 7)*				55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source "On"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C *(Figure 8)*				32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55325 and across the 0°C to +70°C range for the DS75325. All typical values are at T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

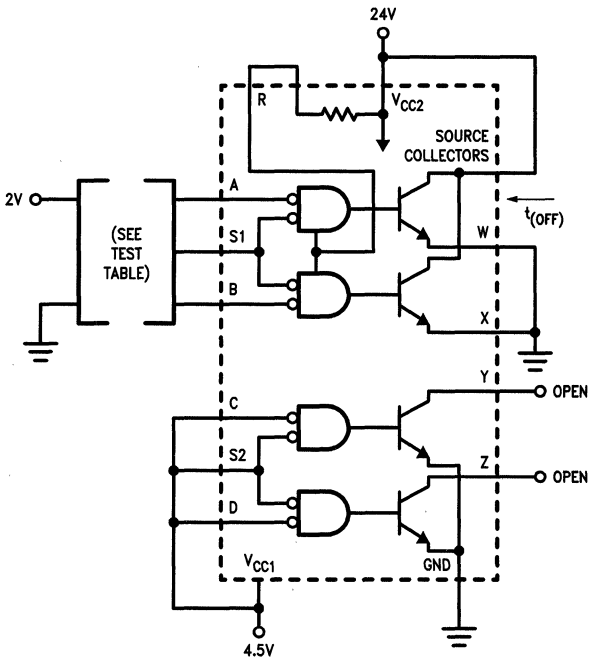
Note 5: Voltage values are with respect to network ground terminal.

Note 6: These parameters must be measured using pulse techniques. t_W = 200 μs, duty cycle ≤2%.

Switching Characteristics V_{CC1} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ *(Figure 10)*		55		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω *(Figure 9)*		7	15	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ *(Figure 10)*		7		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω *(Figure 9)*		9	20	ns
t_S	Storage Time, Sink Outputs	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF *(Figure 9)*			15	30	ns

DC Test Circuits



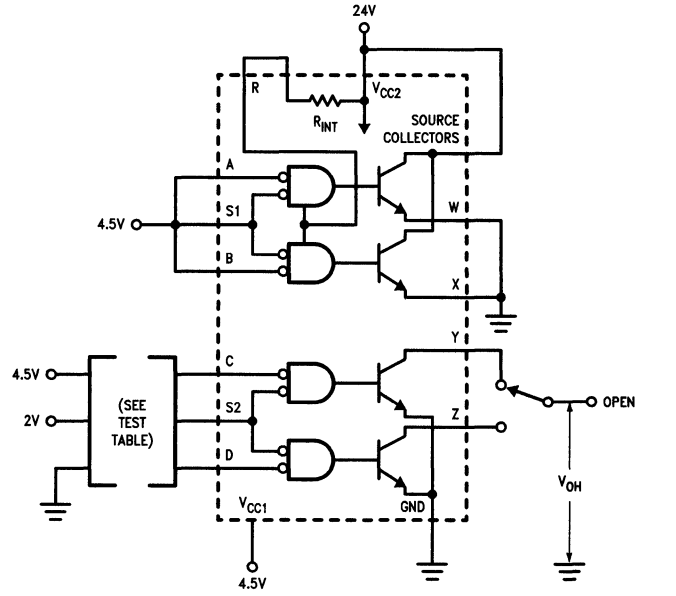
TL/F/9755–3

Test Table

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

DC Test Circuits (Continued)

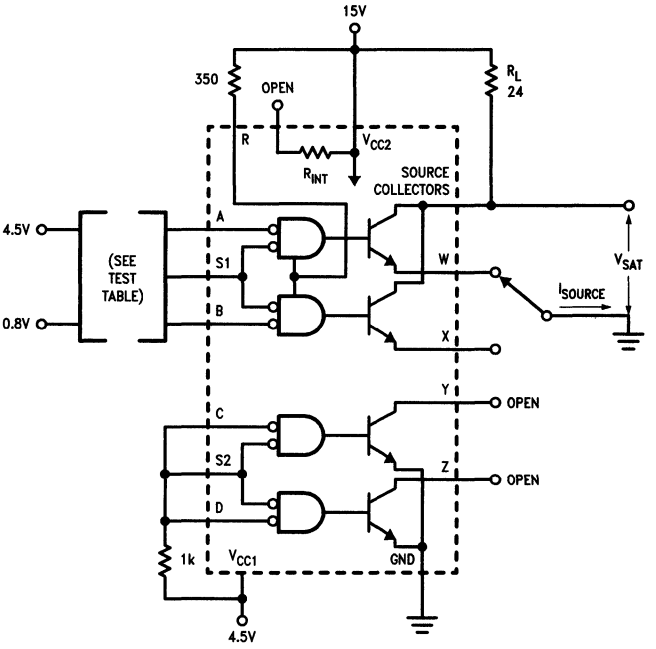


TL/F/9755–4

FIGURE 2. V_{IH} and V_{OH}

Test Table

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}



TL/F/9755–5

Test Table

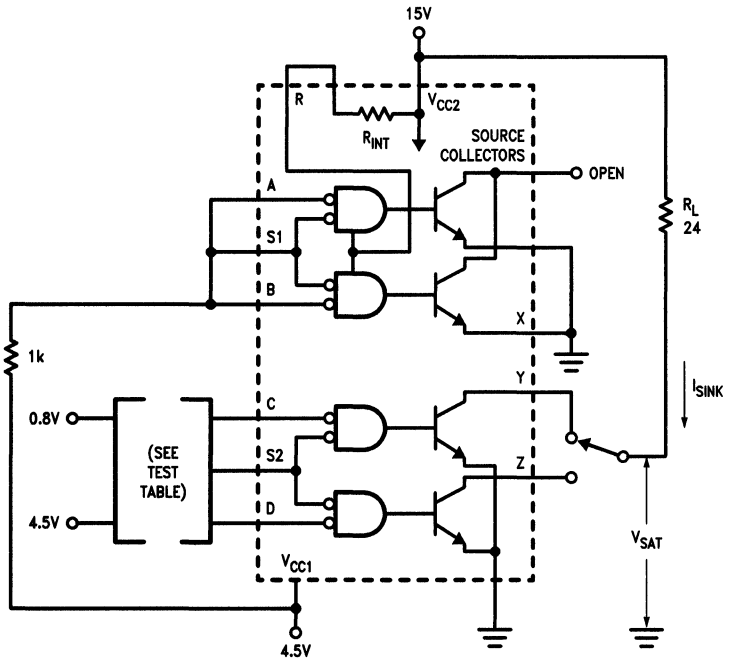
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

Note 1: *Figure 3* and *4* parameters must be measured using pulse techniques, t_W = 200 μs, duty cycle ≤2%.

FIGURE 3. V_{IL} and Source V_{SAT}

5

DC Test Circuits (Continued)



TL/F/9755–6

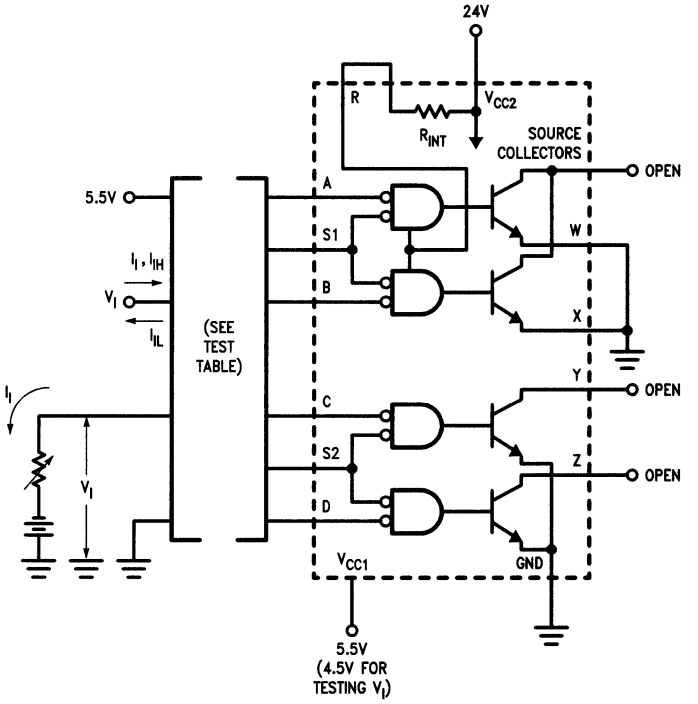
Note 1: *Figure 3* and *4* parameters must be measured using pulse techniques, $t_W = 200\ \mu s$, duty cycle $\leq 2\%$.

Test Table

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}

DC Test Circuits (Continued)



TL/F/9755–7

Test Tables

I_I, I_{IH}

Apply V_I = 5.5V Measure I_I / Apply V_I = 2.4V Measure I_{IH}	Ground	Apply 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

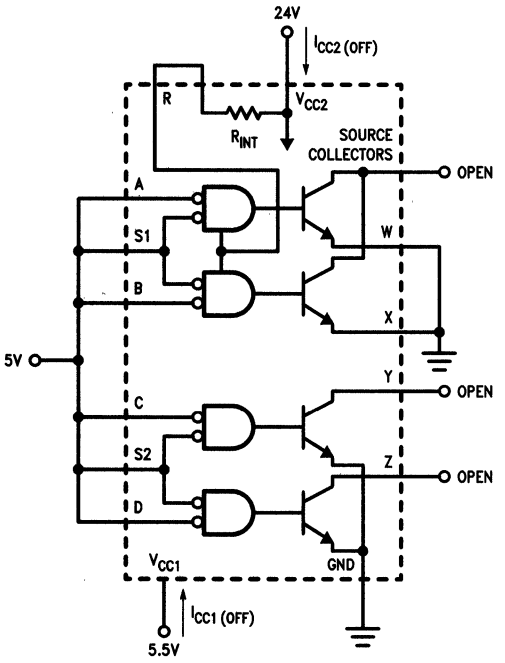
V_I, I_{IL}

Apply V_I = 0.4V Measure I_{IL} / Apply I_I = −10 mA Measure V_I	Apply 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH} and I_{IL}

5

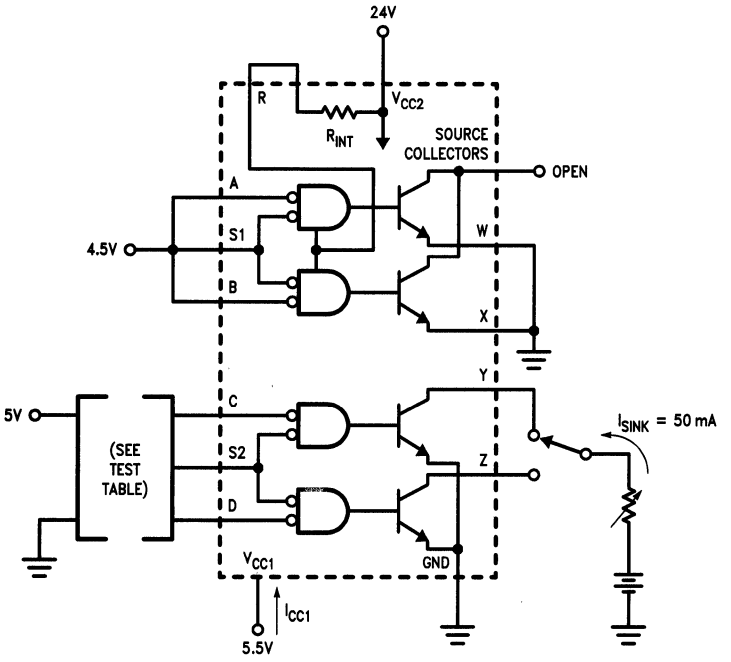
DC Test Circuits (Continued)



TL/F/9755–8

FIGURE 6. $I_{CC1\ (OFF)}$ and $I_{CC2\ (OFF)}$

DC Test Circuits (Continued)



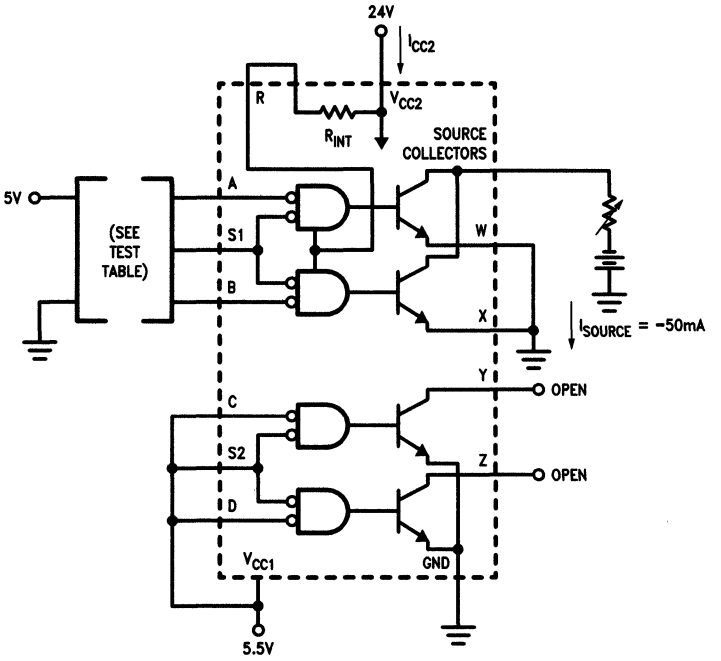
TL/F/9755–9

Test Table

C	D	S2	Y	Z
GND	5V	GND	I_{SINK}	OPEN
5V	GND	GND	OPEN	I_{SINK}

FIGURE 7. I_{CC1}, Either Sink On

DC Test Circuits (Continued)



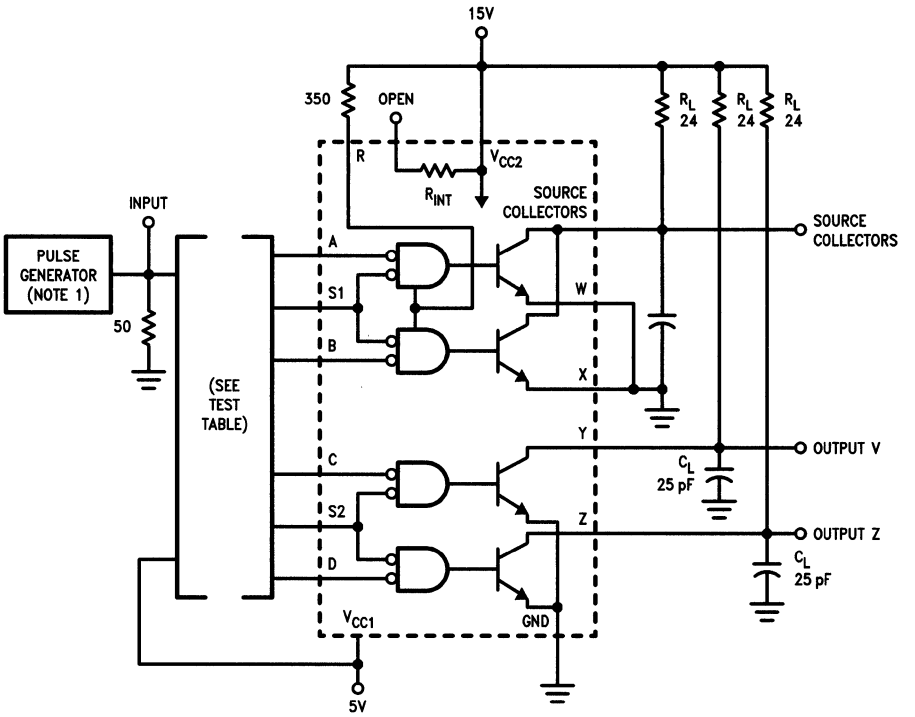
TL/F/9755–10

Test Table

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

DC Test Circuits (Continued)

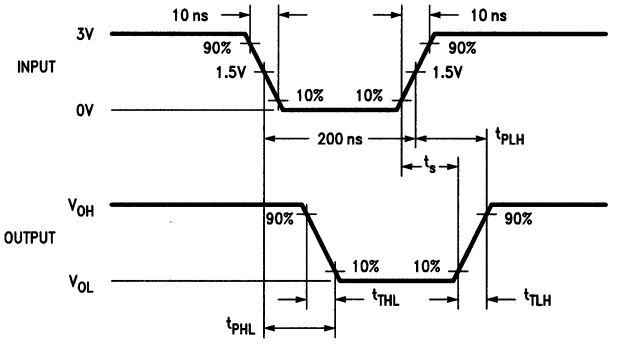


TL/F/9755–11

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤1%.

Note 2: C_L includes probe and jig capacitance.

Voltage Waveforms



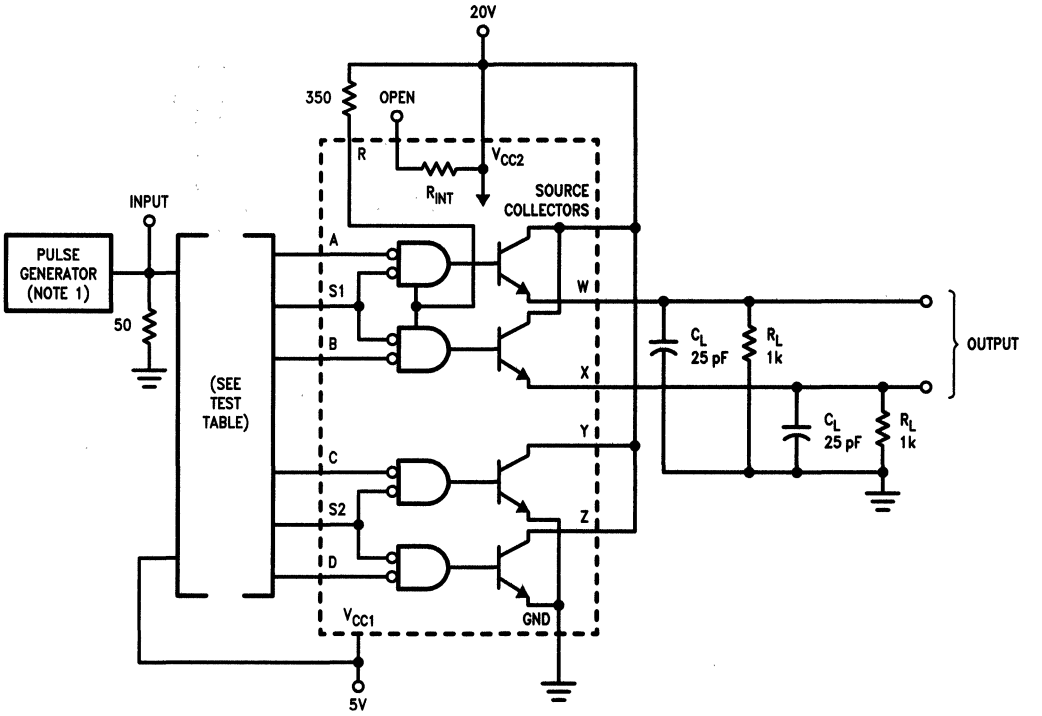
TL/F/9755–12

Test Table

Parameter	Output Under Test	Input	Connect to 5V
t_{PLH} and t_{PHL}	Source Collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} and t_S	Sink Output Y	C and S2	A, B, D and S1
	Sink Output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times

DC Test Circuits (Continued)

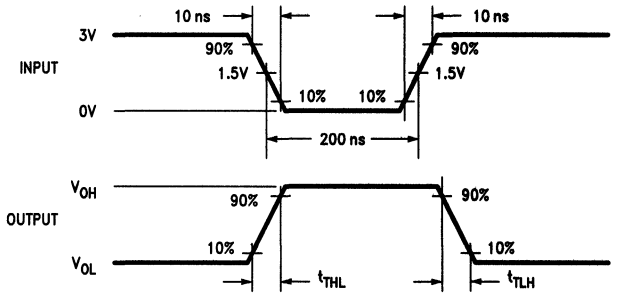


TL/F/9755–13

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

Note 2: C_L includes probe and jig capacitance.

Voltage Waveforms



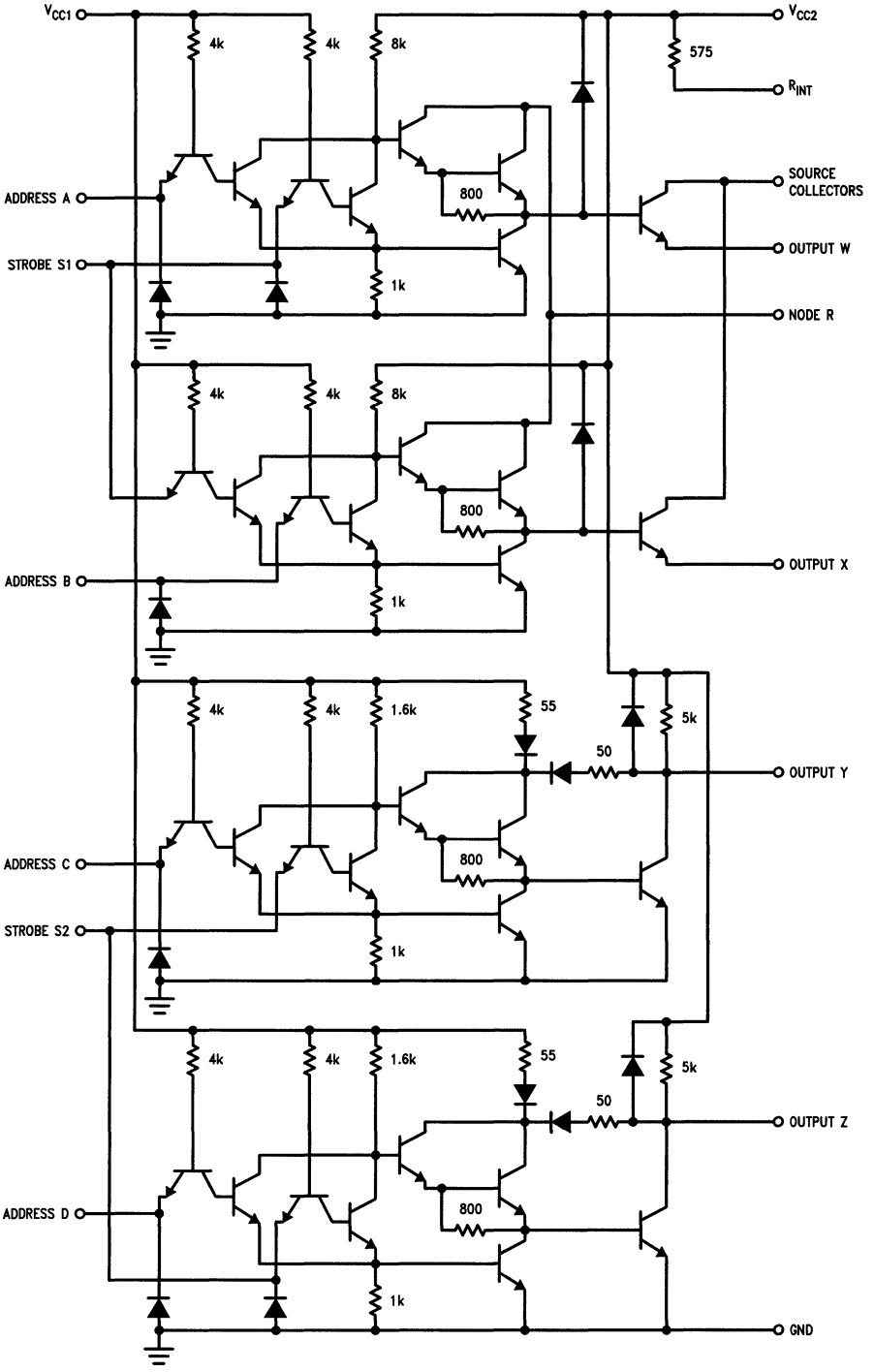
TL/F/9755–14

Test Table

Parameter	Output Under Test	Input	Connect to 5V
t_{TLH} and t_{THL}	Source Output W	A and S1	B, C, D and S2
	Source Output X	B and S1	A, C, D and S2

FIGURE 10. Transition Times of Source Outputs

Schematic Diagram



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Applications

EXTERNAL RESISTOR CALCULATION

A typical magnetic-memory word drive requirement is shown in *Figure 11*. A source-output transistor of one DS75325 delivers load current (I_L). The sink-output transistor of another DS75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(Min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(Min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(Min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(Min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\,I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(Min)} = 20V$ and $V_L = 3V$ while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\,k\Omega$$

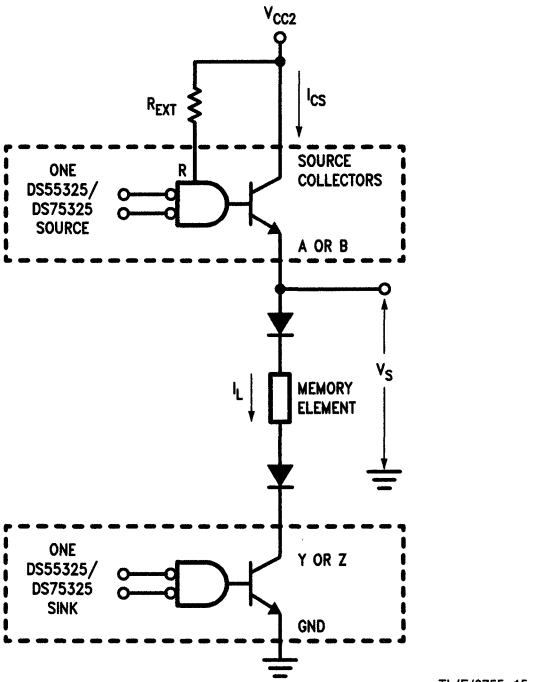
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\,mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\,mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



TL/F/9755–15

Note 1: For clarity, partial logic diagrams of two DS55325s are shown.

Note 2: Source and sink shown are in different packages.

FIGURE 11. Typical Application Data

National Semiconductor

DS75361 Dual TTL-to-MOS Driver

General Description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

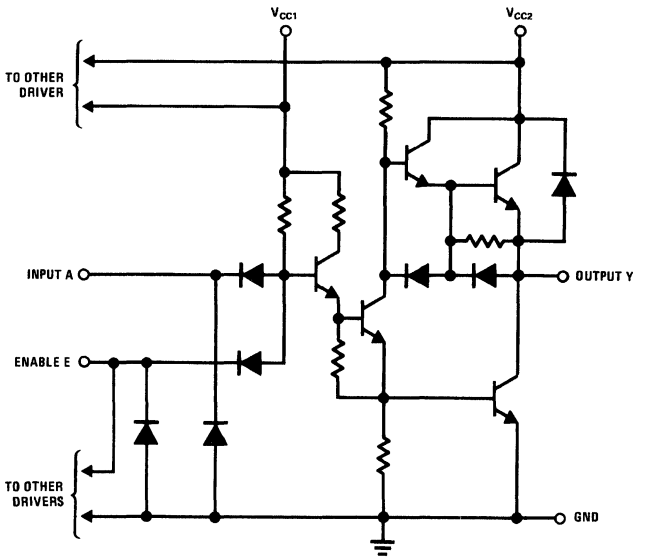
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

Features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

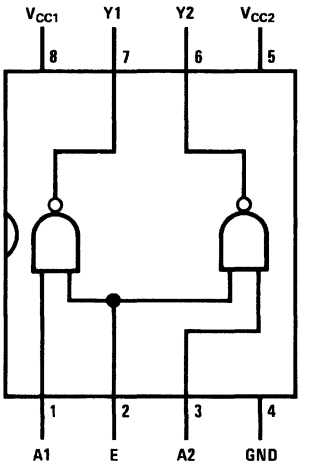
Schematic and Connection Diagrams

(1/2 shown)



TL/F/7557–3

Dual-In-Line Package



TL/F/7557–1

Top View

Order Number DS75361N
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Range of V_{CC1} (Note 1)	−0.5 to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1022 mW
Lead Temperature 1/16 inch from Case for 10 Seconds: N or P Package	200°C

*Derate molded package 8.2 mW/° above about 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC2} = 15V$ to 24V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	$V_{CC1} = 5.25V$, All Inputs at 0V,	$V_{CC2} = 24V$, No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	$V_{CC1} = 5.25V$, All Inputs at 5V,	$V_{CC2} = 24V$, No Load		16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, All Inputs at 5V,	$V_{CC2} = 24V$, No Load			0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$.

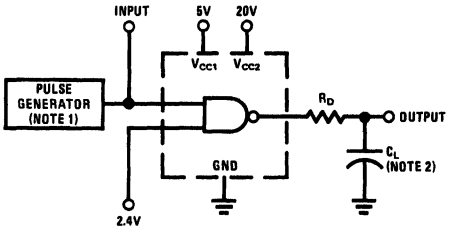
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between the A input of either driver and the common E input.

Switching Characteristics V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω *(Figure 1)*		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
tPLH	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

AC Test Circuit and Switching Time Waveforms



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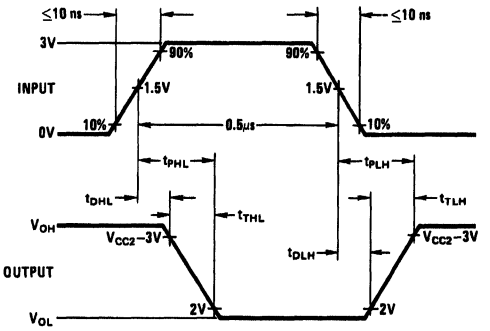


TL/F/7557–5

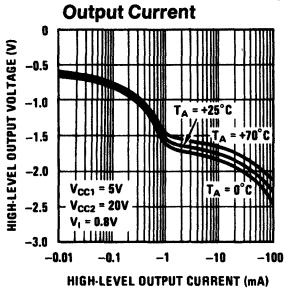
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

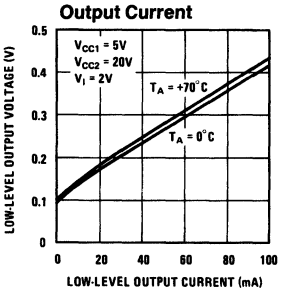
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

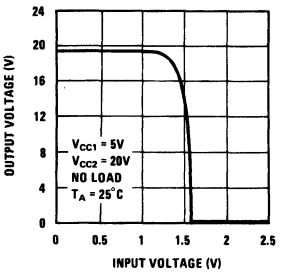
High-Level Output Voltage vs Output Current



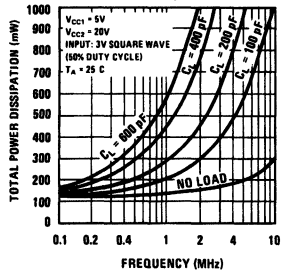
Low-Level Output Voltage vs Output Current



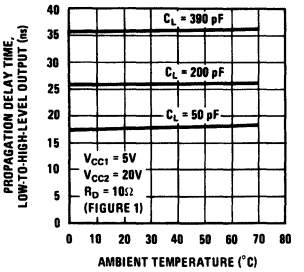
Voltage Transfer Characteristics



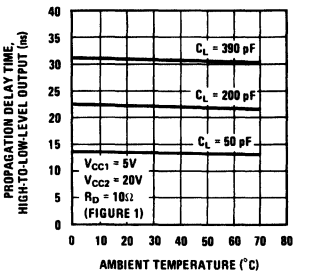
Total Dissipation (Both Drivers) vs Frequency



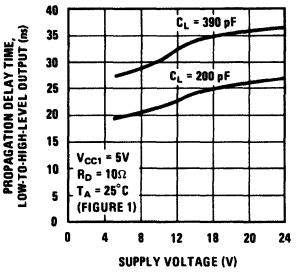
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



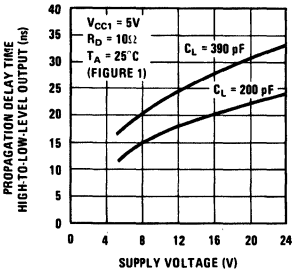
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



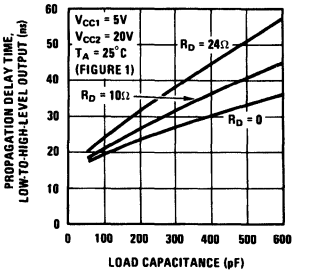
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



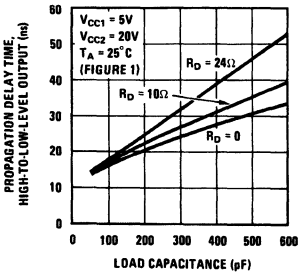
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



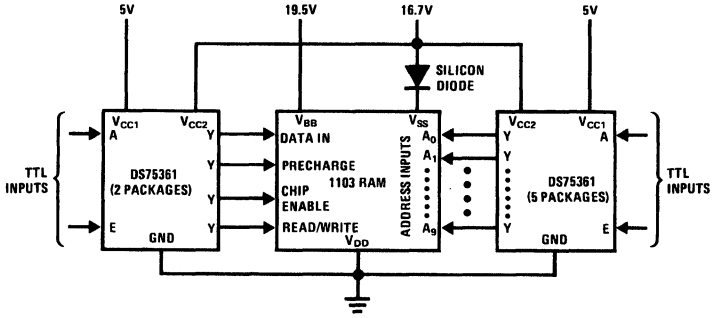
Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



TL/F/7557–2

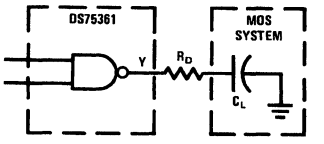
Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.



TL/F/7557–6

FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM



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Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high ($t_H/T = 0.6$). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\,mA}{2}\right) + (20V)\left(\frac{0\,mA}{2}\right) \right](0.6) + \left[(5V)\left(\frac{16\,mA}{2}\right) + (20V)\left(\frac{7\,mA}{2}\right) \right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx$ (200 pF) (19.2V)^2 (2 MHz)

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\,(47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.

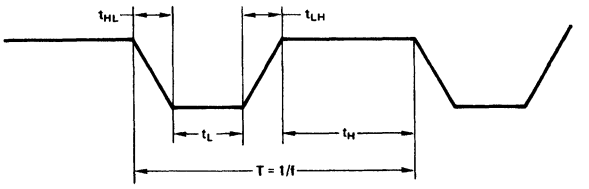

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FIGURE 4. Output Voltage Waveform

National Semiconductor

DS75365 Quad TTL-to-MOS Driver

General Description

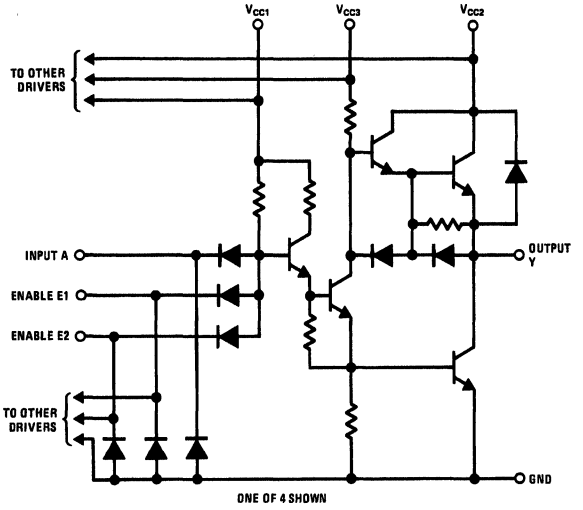
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} to the V_{CC2} pin.

Features

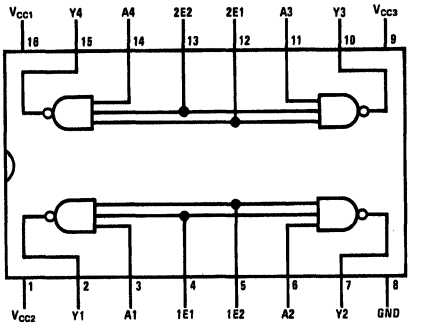
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over side range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



TL/F/7560–1

Dual-In-Line Package



TL/F/7560–2

Top View
Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365N or DS75365WM
See NS Package Number M16B or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
nput Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
SO Package	1488 mW
Lead Temperature (Soldering, 10 sec)	300°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C, derate SO package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\ \mu A$		$V_{CC2} - 0.3$	$V_{CC2} - 0.1$		V
		$V_{CC3} = V_{CC2} + 3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 1.2$	$V_{CC2} - 0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\ \mu A$		$V_{CC2} - 1$	$V_{CC2} - 0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2} - 2.3$	$V_{CC2} - 1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2} + 1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$ $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA

Electrical Characteristics (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-By Condition	V_{CC1} = 0V, V_{CC2} = 24V V_{CC3} = 24V, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-By Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for T_A = 25°C and V_{CC1} = 5V and V_{CC2} = 20V and V_{CC3} = 24V.

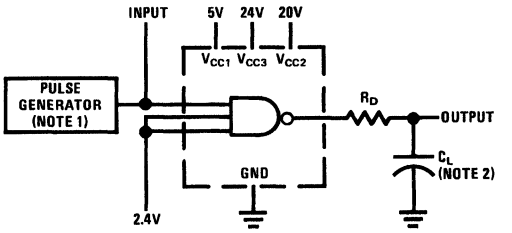
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

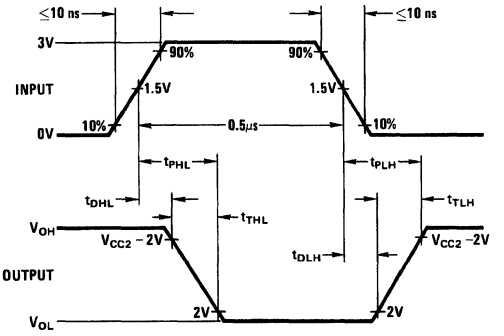
Switching Characteristics V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF R_D = 24Ω (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms



TL/F/7560–3



TL/F/7560–4

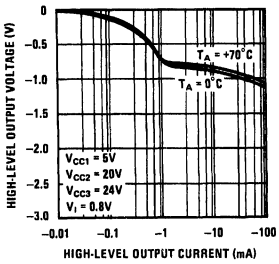
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} = 58Ω.

Note 2: C_L includes probe and jig capacitance.

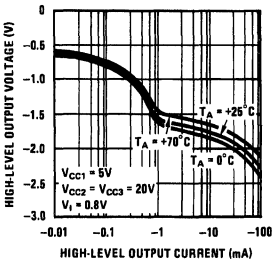
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

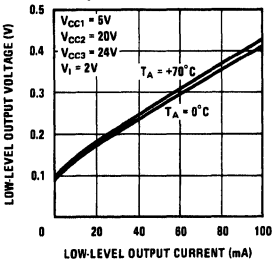
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

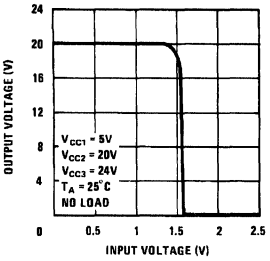


Low-Level Output Voltage Output Current

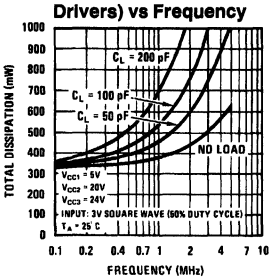


TL/F/7560–5

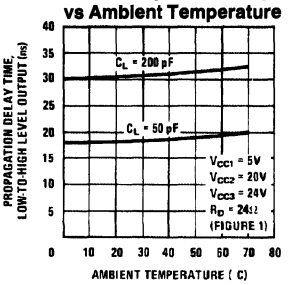
Voltage Transfer Characteristics



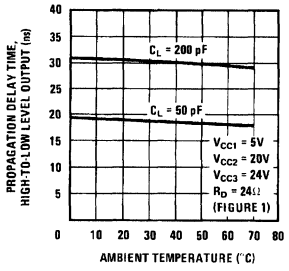
Total Dissipation (All Four Drivers) vs Frequency



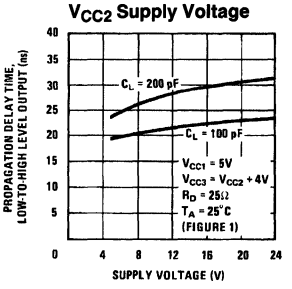
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



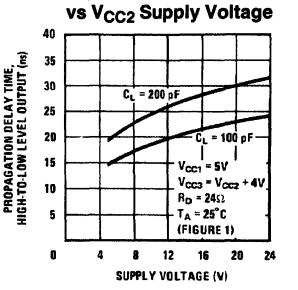
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



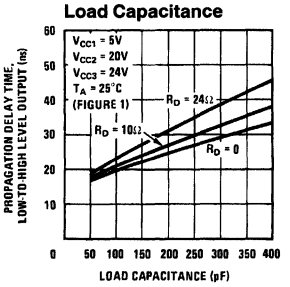
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



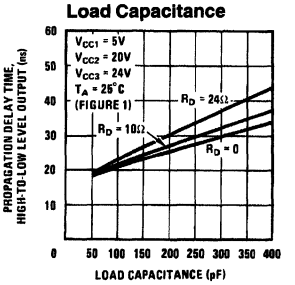
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



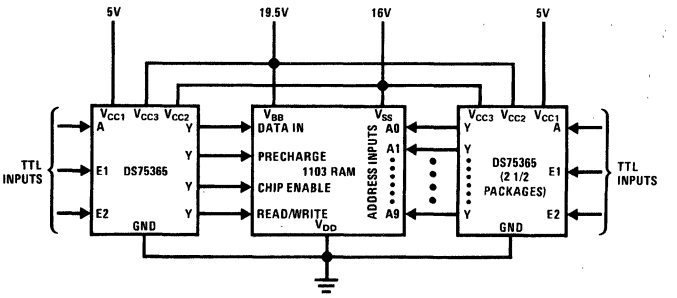
Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



TL/F/7560–6

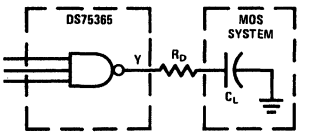


TL/F/7560–7

FIGURE 2. Interconnection of DS75365 Devices with 1103-Type Silicon-Gate MOS RAM

Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω (*Figure 3*).



Note: $R_D \cong$ 10Ω to 30Ω (Optional)

TL/F/7560–8

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75365 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \cong C\,V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

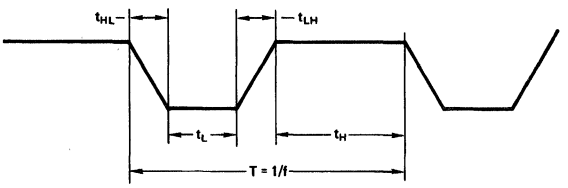
$P_{C(AV)} \cong$ (100 pF) (19.9V)^2 (2 MHz)

$P_{C(AV)} \cong$ 79 mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \cong 4\,(58 + 79)$

$P_{T(AV)} \cong$ 548 mW typical for total package.



TL/F/7560–9

FIGURE 4. Output Voltage Waveform

Section 6

Frequency Synthesis

Section 6 Contents

National Semiconductor

Frequency Synthesis

Frequency synthesis is the process of generating a multitude of different frequencies from one reference frequency. A common application where the frequency synthesis concept is used is in electronically tuned radios and televisions.

Digital tuning systems are fast replacing the conventional mechanical systems in AM, FM and television receivers. The digital approach encompasses the following operational features:

- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station "search" (stop on next active station)
- Power-on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large-scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive.

The heart of any digital tuning system is, of course, the phase locked loop (PLL) synthesizer. The basic subcomponents of a digital system are: a voltage controlled oscillator (VCO), a phase comparator and some programmable and fixed dividers. The PLL's basic function is to take two input signals and match them as illustrated in *Figure 1.* The output of the phase comparator of the PLL is an error signal which is filtered and fed back to the VCO as a DC control voltage. The DC control voltage adjusts the VCO until it causes the phase comparator's two inputs to match one another.

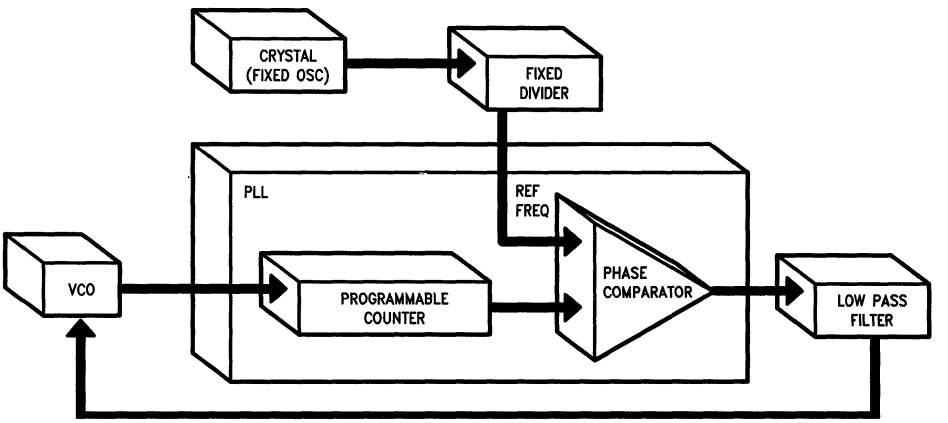
The weak point of this simple illustration is that many PLLs are fabricated using MOS processes which make them relatively incapable of receiving high frequency signals. In fact, state-of-the-art microCMOS devices are usually limited to 100 MHz operation. Even the FM band exceeds this limitation. As a result, a prescaler is almost always used in PLL tuning applications such as FM radios, police scanning radios, aircraft radios, etc. The prescaler is specifically designed to divide high frequency AC input signals down to a usable frequency for the PLL. The prescaler becomes an extension of the PLL's programmable counter as illustrated in *Figure 2.*

For less sophisticated tuning applications, a fixed division prescaler will make the VCO signal palatable to the PLL and be sufficient for general tuning characteristics. However, in some applications, a fixed division prescaler can cause significant undesirable side effects such as:

1. Increased channel spacing (step size) at the output of the PLL's counter; or
2. A forced decrease of the fixed oscillator reference frequency in order to obtain specific channel spacing which can lead to
   A. increased lock-on time,
   B. decreased scanning rates, and
   C. sidebands at undesirable frequencies.

AN-335 in this section explains in detail how these two shortcomings of fixed division prescaling are alleviated by using a dual modulus prescaler. A dual modulus prescaler is substituted for the fixed prescaler and is controlled by programmable counters in the dual modulus PLL, as illustrated by the dotted line in *Figure 2.*

In order to address the requirements of digital frequency synthesis applications, National has introduced a growing family of PLL synthesizers and prescalers. The DS8906, DS8907 and DS8908 are complete PLL synthesizers with features that go beyond those illustrated in *Figure 2.*

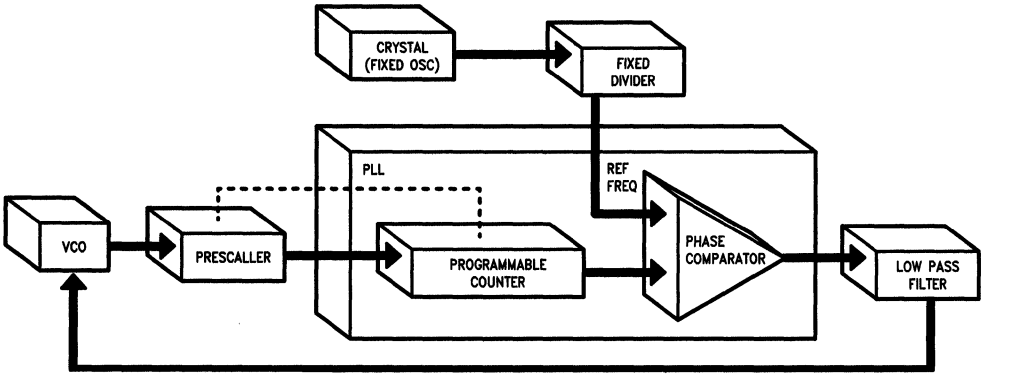


TL/XX/0108–1

FIGURE 1

Highlights

- The DS8908 integrates a reference oscillator, phase comparator, charge pump, operational amplifier, 120 MHz ECL/I^2L dual modulus programmable divider, and a shift register/latch for serial data entry.
- The DS8614, DS8615, DS8616, DS8617, DS8627, and DS8628 represent a broad family of single and dual modulus prescalers for use in conjunction with other manufacturers' NMOS or CMOS PLLs. These low-power/high-speed prescalers are available with division ratios ranging from a fixed ÷20 up to a dual modulus ÷64/65. This array of products allows for the choice of a division ratio which is virtually tailored to the speed and tuning requirements of a particular frequency synthesis application.



TL/XX/0108–2

FIGURE 2

National Semiconductor

Frequency Synthesizers Selection Guide

PLL FREQUENCY SYNTHESIZERS

Product Type	Frequency Bands	Power (mA)	Tuning Resolution
DS8908	AM/FM	160	1 kHz,9 kHz,10 kHz, 20 kHz
DS8911/13	AM/FM/VHF TV	35	FM; 10, 12.5, 25, 100 kHz AM; 1, 1.25, 2.5, 10 kHz

HIGH FREQUENCY PRESCALERS

Product Type	Divide Modulus	Power (mA)	f_{MAX}
Single (Fixed) Modulus Dividers			
DS8673	÷64	25	1 GHz
DS8674	÷256	25	1 GHz
Dual-Modulus Dividers			
DS8615	÷32/33	7/10	130/225 MHz
DS8616	÷40/41	7/10	130/225 MHz

OSCILLATOR DIVIDER CIRCUITS

Product Type	Crystal Frequency	Output Frequency	Power (mA)
MM5368	32,768 Hz	50/60 Hz, 10 Hz, 1 kHz	1.5
MM5369AA	3,579545 MHz	60 Hz, Crystal Frequency	1.2

National Semiconductor

DS8615/DS8616 130/225 MHz Low Power Dual Modulus Prescalers

General Description

The DS8615 series products are low power dual modulus prescalers which divide by 32/33 and 40/41 respectively. The modulus control (MC) input selects division by N when at a high TTL level and division by N + 1 when at a low TTL level. The clock inputs are buffered, providing 40/100 mVrms input sensitivity. The two outputs provide the user the option to wire either a totem-pole or open-collector output structure. Additionally, the user can wire a resistor between the two output pins to minimize edge transition emissions. The outputs are designed to drive positive edge triggered PLLs. These products can be operated from either an unregulated 5.5V to 13.5V source or regulated 5V ±10% source. Unregulated operation is obtained by connecting V_S to the source with V_{REG} open. Regulated operation is obtained by connecting both V_S and V_{REG} to the supply source.

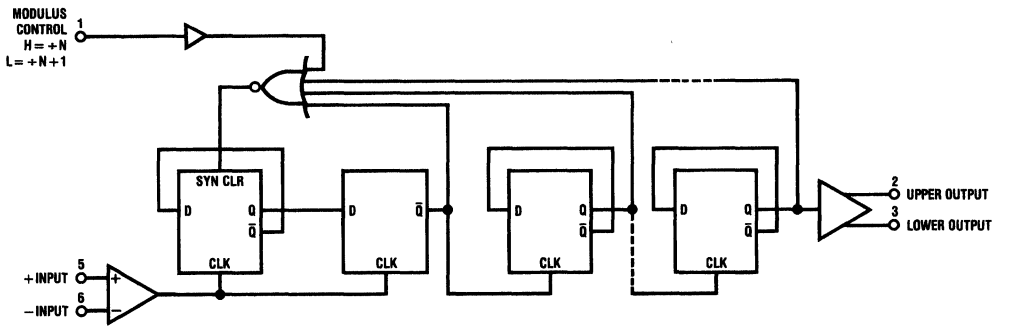
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4); 225 MHz (-2)
- Low power: 10 mA (-4, -2)
- Input sensitivity: 100 mVrms (-4); 40 mVrms (-2)
- Pin compatible with Motorola MC12015-16 prescalers
- Unregulated/regulated power supply option

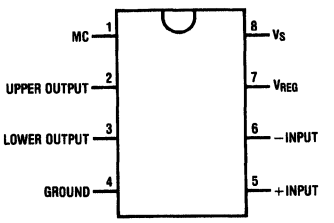
Logic and Connection Diagrams

Generalized ÷ N/N + 1



TL/F/5240–1

Dual-In-Line Package



TL/F/5240–2

Top View

Order Number DS8615N or DS8616N (-4, -2)
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_S, Unregulated Supply Voltage	15V
V_{REG}, Regulated Supply Voltage	7V
Modulus Control Input Voltage	7V
Open-Collector Output Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8615-4 DS8616-4		DS8615-2 DS8616-2		Units
			Min	Max	Min	Max	
V_S	Unregulated Supply Voltage	V_{REG} = Open	6.8	13.5	5.5	13.5	V
V_{REG}	Regulated Supply Voltage	V_S and V_{REG} Shorted	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130		225	MHz
V_{IN}	Input Signal Amplitude		100	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		V/μs
I_{OH}	High Level Output Current			−400		−400	μA
I_{OL}	Low Level Output Current			2.0		2.0	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8615-4 DS8616-4		DS8615-2 DS8616-2		Units
			Min	Max	Min	Max	
V_{IH}	High Level MC Input Voltage	V_S = 13.5V, V_{REG} = Open	2.0		2.0		V
V_{IL}	Low Level MC Input Voltage	V_{REG} = V_S = 4.5V		0.8		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, Pins 2 and 3 Shorted	V_{REG} −2		V_{REG} −2		V
I_{CEX}	Open-Collector High Level Output	Lower Output = 5.5V		100		100	μA
V_{OL}	Low Level Output Voltage	V_{REG} = 4.5V, I_{OL} = 2 mA		0.5		0.5	V
I_I	Max MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IH} = 7V		100		100	μA
I_{IH}	High Level MC Input Current	V_{REG} = 4.5V, V_{IH} = 2.7V		20		20	μA
I_{IL}	Low Level MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IL} = 0.4V		−200		−200	μA
I_S	Supply Current, Unregulated Mode	V_S = 13.5V, V_{REG} = Open		10		10	mA
I_{REG}	Supply Current, Regulated Mode	V_S = V_{REG} = 5.5V		10		10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −30°C to +70°C range.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as Max or Min on absolute value basis.

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = −30°C to +70°C

Symbol	Parameter		Conditions	Min	Max	Units
$t_{MODULUS}$	Modulus Set-Up Time (Notes 4 and 5)	DS8615, DS8616			65	ns
R_{IN}	AC Input Resistance		V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		V_{IN} = 100 MHz and 50 mVrms	3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

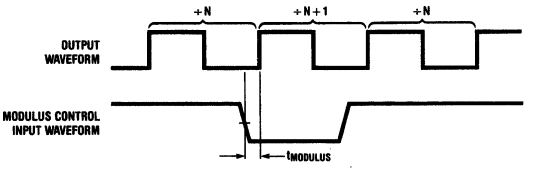
Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: $t_{MODULUS}$ = the period of time the modulus control level must be defined prior to the positive transition of the prescaler output to ensure proper modulus selection.

Note 5: See Timing Diagrams.

Timing Diagram



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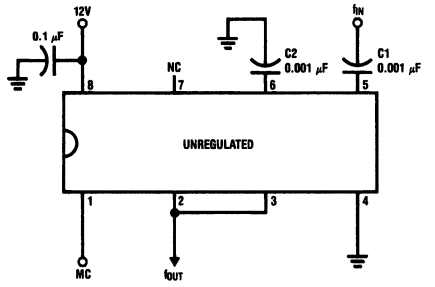
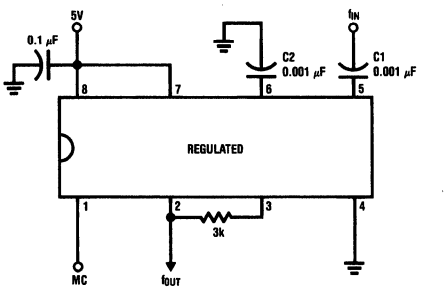
The logical state of the modulus control input just prior to the output's rising edge will determine the modulus ratio of the device immediately following that rising edge. The pulse width difference of N and N + 1 operation occurs during the output = HI conditions.

Typical Applications

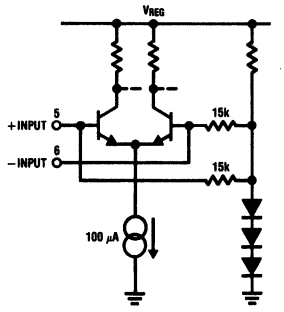


TL/F/5240–4

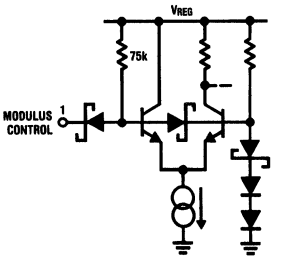


TL/F/5240–5

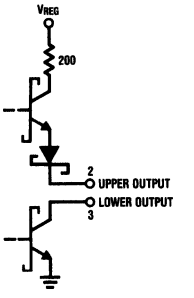
Schematic Diagrams



TL/F/5240–6



TL/F/5240–7



TL/F/5240–8

Application Hints

OPERATING NOTES

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pulldown resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

For regulated mode operation connect V_S to V_{REG} to ensure proper operation (see Typical Application diagram).

National Semiconductor

DS8673/DS8674 Low Power VHF/UHF Prescalers

General Description

The DS8673 and DS8674 products are low power prescalers which divide by 64 and 256 respectively. The devices are used in frequency synthesis applications such as TV/CATV, cellular phone, and instrumentation to divide a very high frequency down to a frequency usable by low power MOS PLL's.

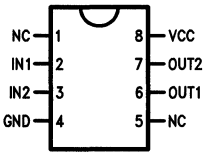
The devices have differential buffered inputs and complementary ECL outputs. The inputs provide high input sensitivity and good isolation. The DS8673 is pin compatible with Plessey's SP4531, SP4632, and Motorola's MC12073 products. The DS8674 is pin compatible with Plessey's SP4653 and Motorola's MC12074 products.

Features

- 1.0 GHz operating frequency
- 25 mA typical supply current
- 20 mV rms input sensitivity
- 0.8V complementary ECL outputs
- Low output radiation

Block and Connection Diagrams

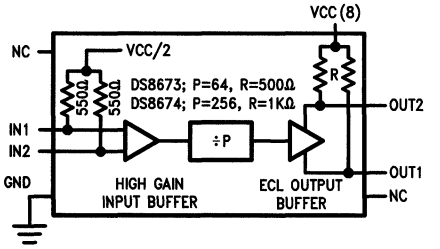
Dual-In-Line Package



TL/F/9340–1

Top View

Order Number DS8673N or DS8674N
See NS Package Number N08E



TL/F/9340–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	V_{CC} + 0.5V
Operating Free Air Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

ESD rating is to be determined.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		4.5		5.5	V
F_{IN}	Input Frequency Range	V_{IN} Min	80		1,000	MHz
V_{IN}	Input Sensitivity into 50Ω	80 MHz	20		200	mV rms
		300 MHz	20		200	
		500 MHz	20		200	
		700 MHz	20		200	
		1 GHz	20		200	

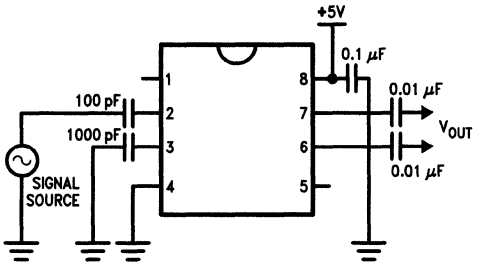
DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = 5.5V		25	35	mA
V_{OUT}	Output Voltage Swing	Peak-to-Peak (no load)	0.8	1.2	1.6	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Typical Applications

Typical Wiring Configuration

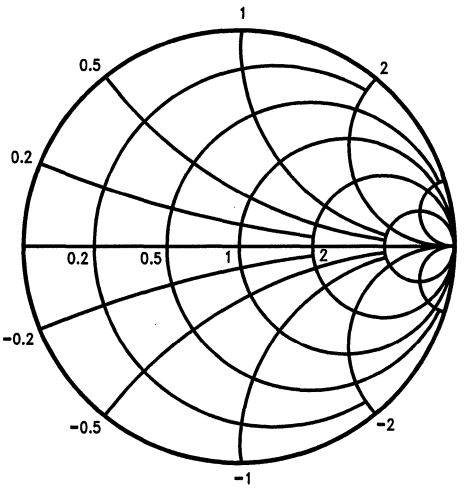


TL/F/9340–3

Typical Applications (Continued)

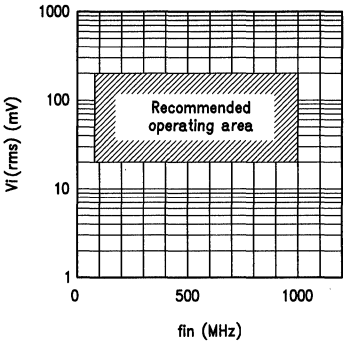
Typical Input Impedance

Reference value = 50Ω
Vi (rms) = 25 mV
V_{CC} = 5V
Waveshape is TBD



TL/F/9340–4

Typical Sensitivity Curve Under Nominal Conditions



TL/F/9340–5

National Semiconductor

DS8908B AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8908B is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necesary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and a 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data steram is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL(N+1) divide code. The 15th bit is used internally to select the AM or FM local oscillator input. A high level on this bit enables the FM input and a low level enables the AM input. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, FM, or charge pump current source levels.

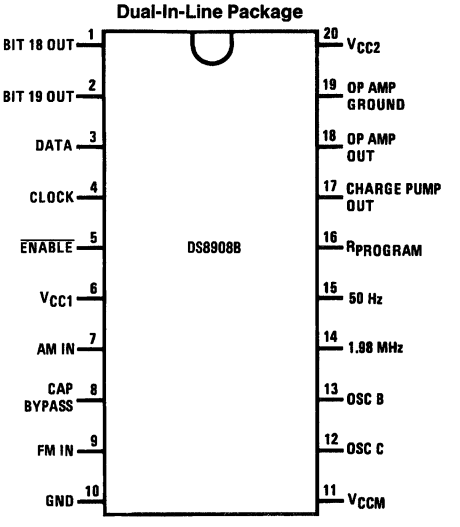
The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p +1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N+1), N being the number loaded into the shift register. The programmable divider is clocked through a $\div 7/8$ prescaler by the AM input or through a $\div 63/64$ prescaler by the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μA to 750 μA of constant current by connection of an external resistor from pin $R_{PROGRAM}$ to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier provided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of either 10 kHz or 20 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- Separate AM and FM inputs; AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram

Dual-In-Line Package



TL/F/5111–1

Top View
Order Number DS8908BN
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
(V_{CC1}) (V_{CCM})	7V
(V_{CC2})	17V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
V_{CC1}	4.5	5.5	V
V_{CC2}	V_{CC1} + 1.5	15.0	V
V_{CCM}	3.5	5.5	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, V_{IN} = 0V			−5	−25	μA
I_{OH}	Logical "1" Output Current All Bit Outputs, 50 Hz Output	V_{OH} = 5.5V				50	μA
	1.98 MHz Output	V_{OH} = 2.4V, V_{CCM} = 4.5V				−250	μA
V_{OL}	Logical "0" Output Voltage All Bit Outputs	I_{OL} = 5 mA				0.5	V
	50 Hz Output, 1.98 MHz Output	I_{OL} = 250 μA				0.5	V
	1.98 MHz Output	I_{OL} = 20 μA, T_A > 70°C I_{OL} = 20 μA, T_A ≤ 70°C				0.3 0.4	V V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High				160	mA
I_{CCM}	V_{CCM} Supply Current	V_{CCM} = 5.5V, All Other Pins Open			2.5	4.0	mA
I_{OUT}	Charge Pump Ougtput Current	3.33k ≤ R_{PROG} ≤ 33.3k I_{OUT} Measured between Pin 17 and Pin 18 I_{PROG} = V_{CC1}/2 R_{PROG}	Pump Up	−20	I_{PROG}	+20	%
			Pump Down	−20	I_{PROG}	+20	%
			TRI-STATE®		0	11	nA
I_{CC2}	V_{CC2} Supply Current	V_{CCM} = 5V, V_{CC1} = 5.5V, V_{CC2} = 15V All Other Pins Open			6.7	11	mA
OP_{VOH}	Op Amp Minimum High Level	V_{CC1} = 4.5V, I_{OH} = −750 μA		V_{CC2} −0.4			V
OP_{VOL}	Op Amp Maximum Low Level	V_{CC1} = 5.5V, I_{OL} = 750 μA				0.6	V
CPO_{BIAS}	Charge Pump Bias Voltage Delta	CPO Shorted to Op Amp Output CPO = TRI-STATE Op Amp I_{OL}: 750 μA vs −750 μA				100	mV

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, t_r ≤ 10 ns, t_f ≤ 10 ns

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C			20	100	mV(rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, −40°C ≤ T_A ≤ 85°C		1000	1500		mV(rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms −40°C ≤ T_A ≤ 85°C	AM	0.5		15	MHz
			FM	80		120	MHz
$R_{IN}(FM)$	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		600			Ω
$R_{IN}(AM)$	AC Input Resistance, AM	15 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz (FM), 15 MHz (AM)		3	6	10	pF
t_{EN1}	Minimum ENABLE High Pulse Width				625	1250	ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, $t_r \leq 10$ ns, $t_f \leq 10$ ns (Continued)

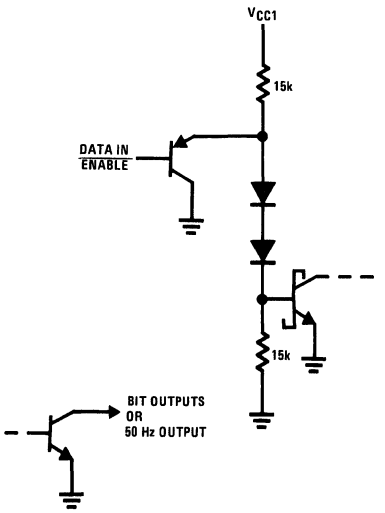
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width			375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Be Low			−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes Low That CLOCK Must Remain Low			275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time before $\overline{\text{ENABLE}}$ Goes High That Last Positive CLOCK Edge May Occur			300	600	ns
$t_{\overline{EN}1CLK}$	Minimum Time after $\overline{\text{ENABLE}}$ Goes High before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Set-Up Time, Minimum Time before CLOCK That DATA Must Be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time after CLOCK That DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

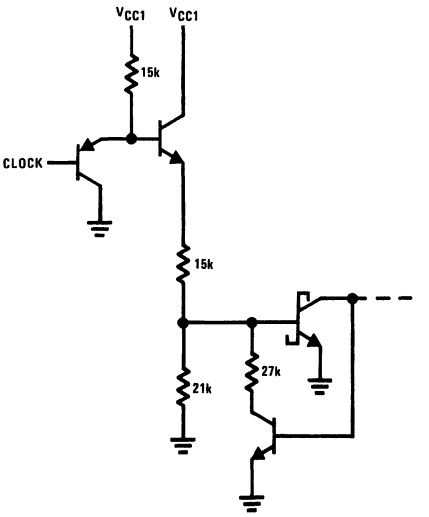
Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8908B.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagrams (DS8908B AM/FM PLL Typical Input/Output Schematics)



TL/F/5111–2



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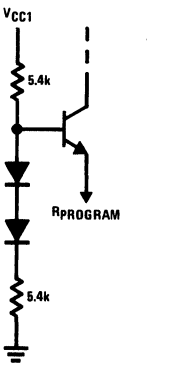
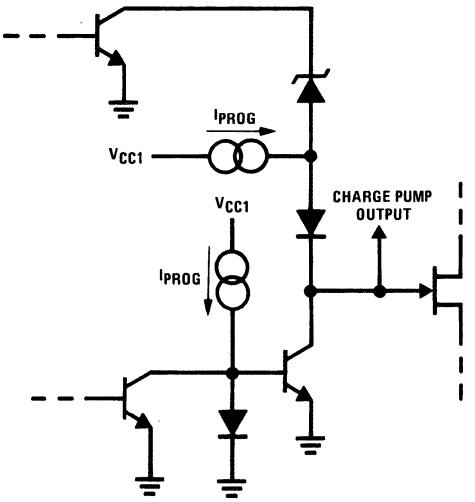
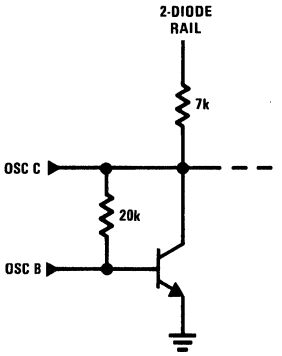


TL/F/5111–4

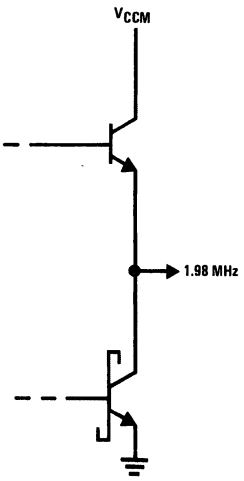
Schematic Diagrams (Continued)



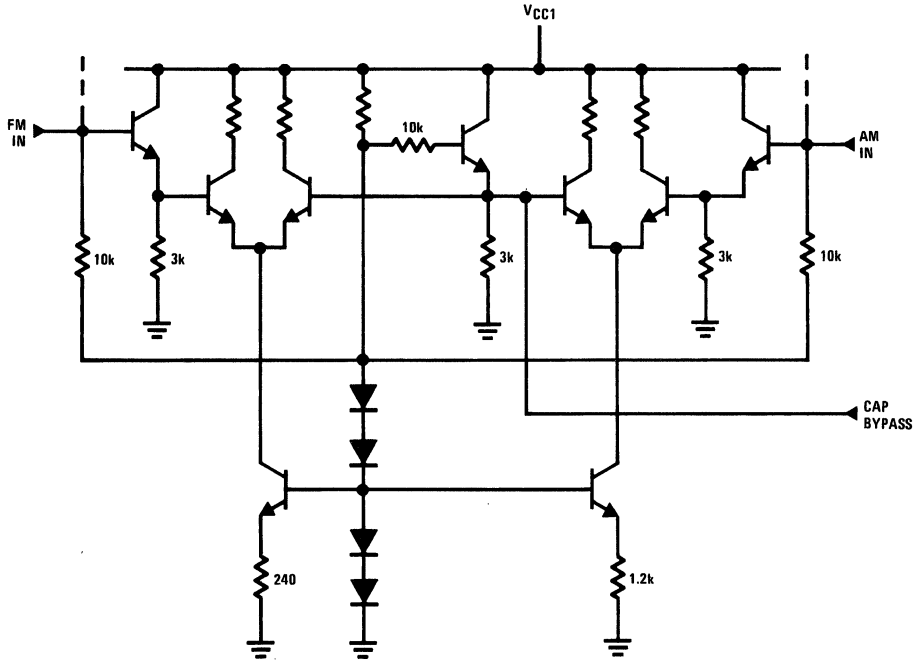
TL/F/5111–5



TL/F/5111–6

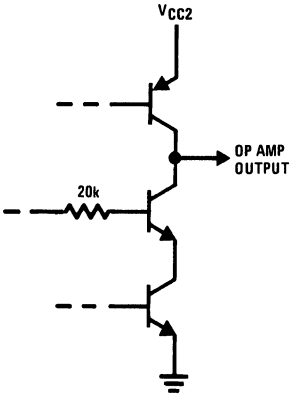


TL/F/5111–7



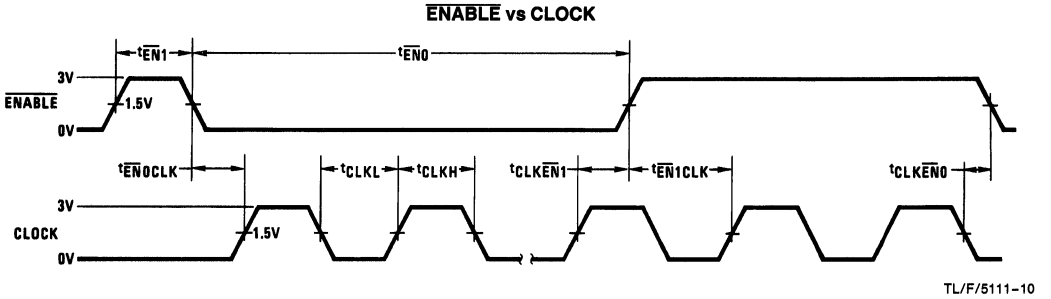
TL/F/5111–8

Schematic Diagrams (Continued)

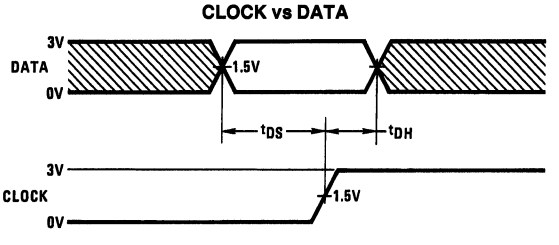


TL/F/5111–9

Timing Diagrams*



TL/F/5111–10

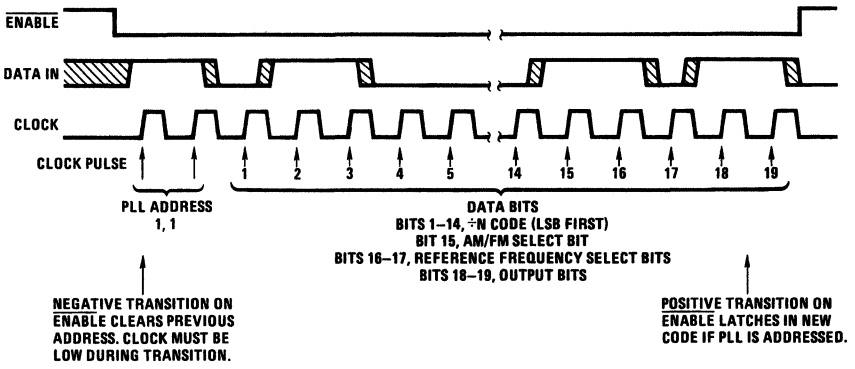


TL/F/5111–11

6

Timing Diagrams* (Continued)

AM/FM Frequency Synthesizer (Scan Mode)



TL/F/5111–12

*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8908B

Serial information entry into the DS8908B is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1 *no* further information will be accepted fromt he DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any data bits preceding the 19th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the $\overline{\text{ENABLE}}$ low. When the $\overline{\text{ENABLE}}$ input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

These data bits are interpreted as follows:

Data Bit Position	Data Interpretation
Last	Bit 19 Output (Pin 2)
2nd to Last	Bit 18 Output (Pin 1)
3rd to Last	Ref. Freq. Select Bit(1)17
4th to Last	Ref. Freq. Select Bit(1)16
5th to Last	AM/FM Select Bit 15
6th to Last	(2^{13})
7th to Last	(2^{12})
8th to Last	(2^{11})
9th to Last	(2^{10})
10th to Last	(2^{9})
11th to Last	(2^{8})
12th to Last	(2^{7})
13th to Last	(2^{6})
14th to Last	(2^{5})
15th to Last	(2^{4})
16th to Last	(2^{3})
17th to Last	(2^{2})
18th to Last	(2^{1})
19th to Last	LSB of $\div N(2^{0})$

$\div N(2)$

Note 1: See Reference Frequency Select Truth Table.

Note 2: The actual divide code is N+1, ie., the number loaded plus 1.

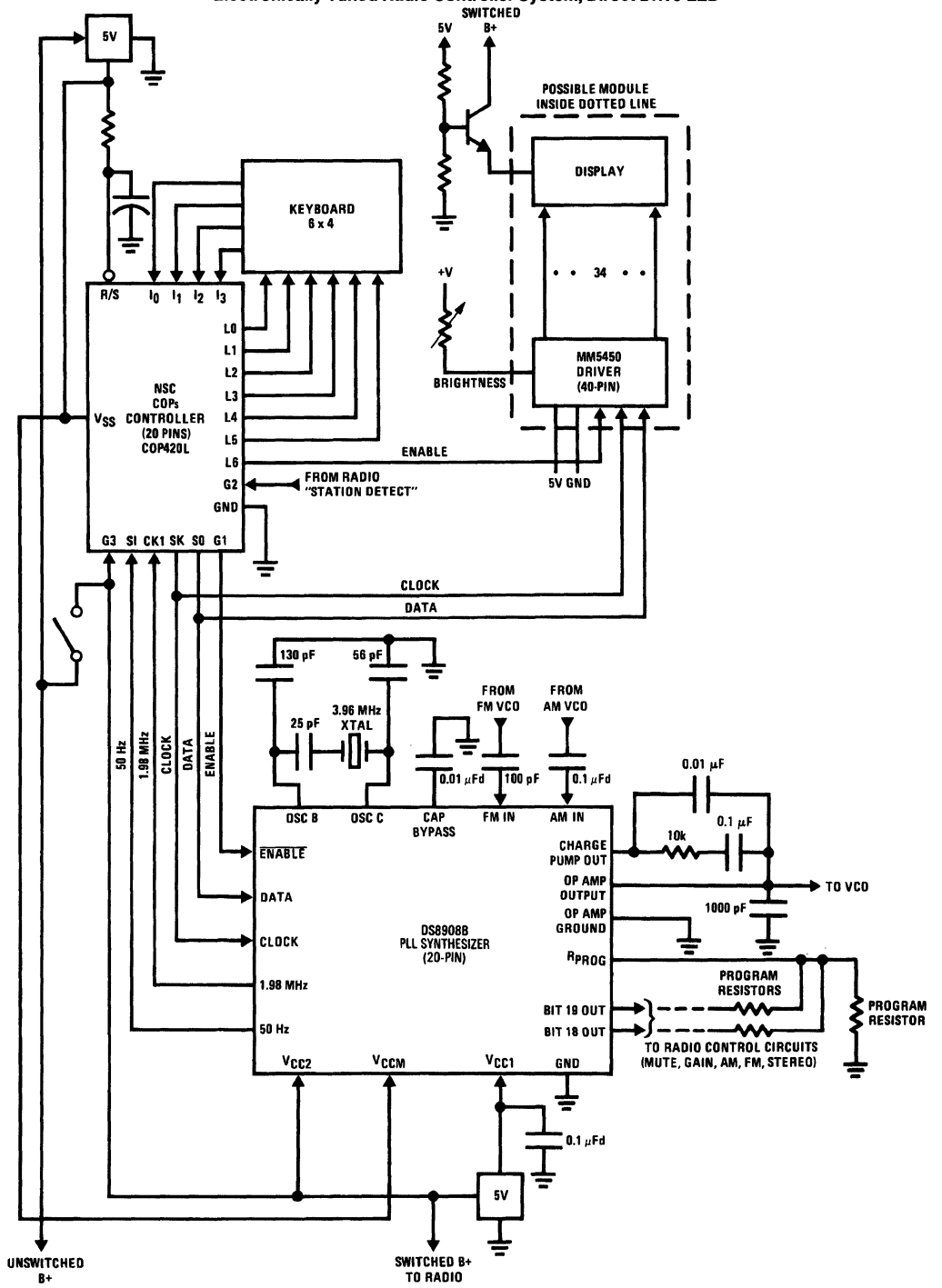
Truth Table

Reference Frequency Selection Truth Table

Serial Data		Reference Frequency
Bit 16	Bit 17	(kHz)
1	1	20
1	0	10
0	1	9
0	0	1

Typical Application Additional application notes are located at the back of section 11.

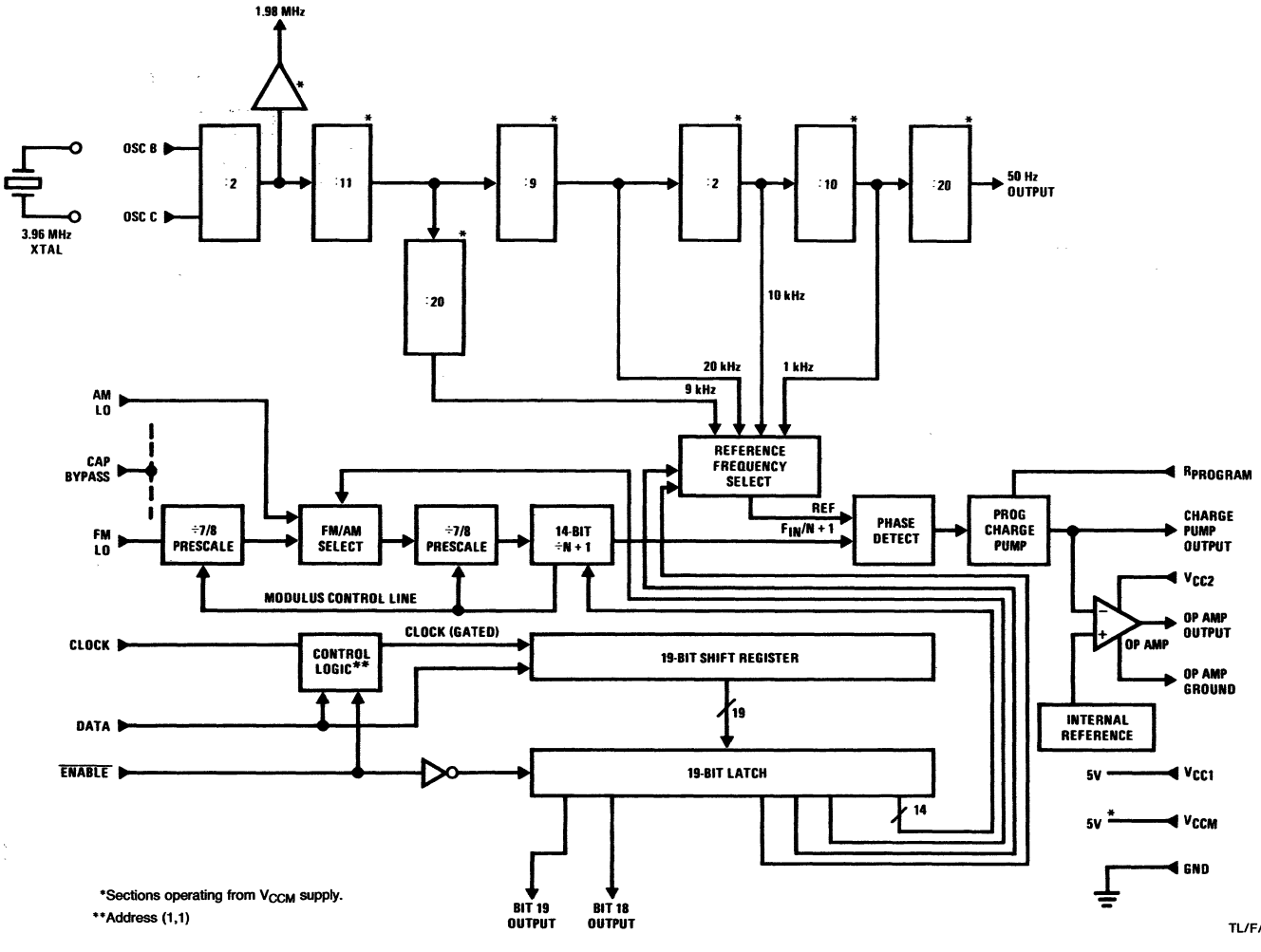
Electronically Tuned Radio Controller System; Direct Drive LED



TL/F/5111–13

Logic Diagram

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)



*Sections operating from V_{CCM} supply.

**Address (1,1)

TL/F/5111–14

National Semiconductor

DS8911/DS8913 AM/FM/TV Sound Up-Conversion Frequency Synthesizer

General Description

The DS8911 is a digital Phase-Locked Loop (PLL) frequency synthesizer intended for use as a Local Oscillator (LO) in electronically tuned radios. The device is used in conjunction with a serial data controller, a loop filter, some varactor diodes and several passive elements to provide the local oscillator function for both AM and FM tuning.

The conventional superheterodyne AM receiver utilizes a low IF or down conversion tuning approach whereby the IF is chosen to be below the frequencies to be received. The DS8911 PLL on the other hand, utilizes an up-conversion technique in the AM mode whereby the first IF frequency is chosen to be well above the RF frequency range to be tuned. This approach eliminates the need for tuned circuits in the AM frontend since the image, half IF, and other spurious responses occur far beyond the range of frequencies to be tuned. Sufficient selectivity and second IF image protection is provided by a crystal filter at the output of the first mixer.

A significant cost savings can be realized utilizing this up-conversion approach to tuning. Removal of the AM tuned circuits eliminates the cost of expensive matched varactor diodes and reduces the amount of labor required for alignment down from 6 adjustments to 2. Additional cost savings are realized because up-conversion enables both the AM and FM bands to be tuned using a single Voltage Controlled Oscillator (VCO) operating between 98 and 120 MHz. (The 2 to 1 LO tuning range found in conventional AM down conversion radios is reduced to a 10% tuning range; 9.94 MHz to 11.02 MHz).

Up-conversion AM tuning is accomplished by first dividing the VCO signal down by a modulus 10 to obtain the LO signal. This LO in turn is mixed on chip with the RF signal to obtain a first IF at the MIXER output pins. This first IF after crystal filtering is mixed (externally) with a reference frequency provided by the PLL to obtain a 450 kHz second IF frequency. The DS8911 derives the 450 kHz second IF by mixing an 11.55 MHz first IF with a 12.00 MHz reference frequency.

FM and WB (weather band) tuning is done using the conventional down conversion approach. Here the VCO signal is buffered to produce the LO signal and then mixed on chip with the RF signal to obtain an IF frequency at the MIXER output pins. This IF frequency is typically chosen to be 10.7 MHz although placement at 11.50 MHz can further enhance AM mode performance and minimize IF circuitry.

The PLL provides phase comparator reference frequencies of 10, 12.5, 25, and 100 kHz. The tuning resolutions resulting from these reference frequencies are determined by dividing the reference by the premix modulus. Table II shows the tuning resolutions possible.

The DS8911 contains the following logic elements: a voltage controlled oscillator, a reference oscillator, a 14-bit programmable dual-modulus counter, a reference frequency divider chain, a premix divider, a mixer, a phase comparator, a charge pump, an operational amplifier, and control circuitry for latched serial data entry.

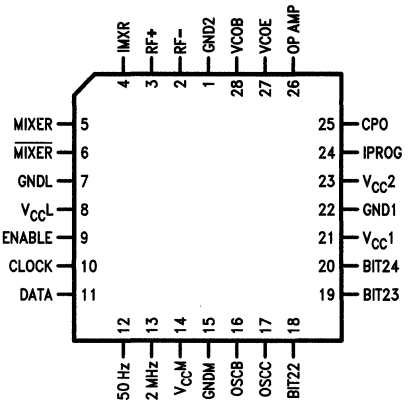
The DS8913 includes all the above logic elements except that it requires a 10 MHz reference frequency instead of 12 MHz.

Features

- Direct synthesis of LW, MW, SW, FM, and WB frequencies
- Serial data entry for simplified processor control
- 10, 12.5, 25, and 100 kHz reference frequencies
- 8 possible tuning resolutions (see Table II)
- An op amp with high impedance inputs for loop filtering
- Programmable mixer with high dynamic range

Connection Diagram

Plastic Chip Carrier



TL/F/7398–8

Top View

Order Number DS8911V/DS8913V
See NS Package Number V28A

Pin Descriptions

V_{CC1}: The V_{CC1} pin provides a 5V supply source for all circuitry except the reference divider chain, op amp and mixer sections of the die.

V_{CC2}: The V_{CC2} pin provides a 12V supply source for the Op amp.

V_{CCL}: The V_{CCL} pin provides an isolated 5V supply source for the premix divider and mixer functions.

V_{CCM}: The V_{CCM} pin provides a 5V supply source for the reference oscillator and divider chain down through the 50 Hz output, thus enabling low standby current for time-of-day clock applications.

GND1, GND2, GNDL and GNDM: Provide isolated circuit ground for the various sections of the device.

DATA and CLOCK: The DATA and CLOCK inputs are for serial data entry from a controller. They are CMOS inputs with TTL logic thresholds. The 24-bit data stream is loaded into the PLL on the positive transition of the CLOCK. The first 14 bits of the data stream select PLL divide code in binary form MSB first. The 15th through 24th bits select the premix modulus, the reference frequency, the bit output status, and the test/operate modes as shown in Tables I through V.

ENABLE: The ENABLE input is a CMOS input with a TTL logic threshold. The ENABLE input enables data when at a logic "one" and latches data on the transition to a logic "zero".

BIT Outputs: The open-collector BIT outputs provide either the status of shift register bits 22, 23, and 24 or enable access to key internal circuit test nodes. The mode for the bit outputs is controlled by shift register bits 20 and 21. In operation, the bit outputs are intended to drive radio functions such as gain, mute, and AM/FM status. These outputs can also be used to program the loop gain by connection of an external resistor to IPROG. Bit 24 output can also be used as a 300 millisecond timer under control of shift register bit 19. During service testing, these pins can be used for the purpose of either monitoring or driving internal logic points as indicated in the TEST MODES description under Table V.

VCOb and VCOe: The Voltage Controlled Oscillator inputs drive the 14-bit programmable counter and the premix divider. These inputs are the base and emitter leads of a transistor which require connection of a coil, varactor, and several capacitors to function as a Colpitts oscillator. The VCO is designed to operate up to 225 MHz. The VCO's minimum operating frequency may be limited by the choice of reference frequency and the 961 minimum modulus constraint of the 31/32 dual modulus counter.

RF+ and RF−: The Radio Frequency inputs are fed differentially into the mixer.

IMXR: The bias current for the mixer is programmed by connection of an external resistor to this pin. The total mixer output current equals 4 times the current entering this pin.

MIXER and $\overline{\text{MIXER}}$: The MIXER outputs are the collectors of the double balanced pair mixer transistors. They are intended to operate at voltages greater than V_{CC1}.

OSCb and OSCc: The Reference Oscillator inputs are part of an on-chip Pierce oscillator designed to work in conjunction with 2 capacitors and a crystal resonator. The DS8911 requires a 12 MHz crystal to derive the reference frequencies shown in Table II. The DS8913 requires 10 MHz crystal.

The 12 MHz OSC signal is also used externally as the 2nd AM LO to obtain a 450 kHz 2nd IF frequency in the AM mode.

2 MHz: The 2 MHz output is provided to drive a controller's clock input.

50 Hz: The 50 Hz output is provided as a time reference for radios with time-of-day clocks.

IPROG: The IPROG pin enables the charge pump to be programmed from 0.25 mA to 1.0 mA by connection of an external resistor to ground.

CPO: The Charge Pump Output circuit sources current if the VCO frequency is high and sinks current if the VCO frequency is low. The CPO is wired directly to the negative input of the loop filter op amp.

OP AMP: The OP AMP output is provided for loop filtering. The op amp has high impedance PMOS gate inputs and is wired as a transconductance amplifier/filter. The op amp's positive input is internally referenced while its negative input is common with the CPO output.

Reference Tables

TABLE I

Bit 15	Premix Modulus
0	÷1
1	÷10

TABLE II

Bit		Reference Frequency	Tuning Resolution	
16	17		÷1 Premix	÷10 Premix
0	0	10 kHz	10 kHz	1 kHz
0	1	12.5 kHz	12.5 kHz	1.25 kHz
1	0	25 kHz	25 kHz	2.5 kHz
1	1	100 kHz	100 kHz	10 kHz

TABLE III

Bit 18	Mode
0	Normal Operation*
1	Production Test Mode Only

*The user should always load Bit 18 low.

TABLE IV

Bit 19	Timer
0	Bit 24 Status
1	$\overline{\text{Bit 24}}$ for 300 ms

TIMER OPERATION

The timer function is provided for use as a retriggerable "one shot" to enable muting for approximately 300 milliseconds after station changes. The timer is enabled at bit 24's output if the normal operating mode is selected (shift register bits 20 and 21 = "LOW") and shift register bit 19 data is latched as a "HI". The timer's output state will invert immediately upon latching bit 19 "HI" and remain inverted for approximately 300 milliseconds. If the user readdresses the device with bit 19 data "LOW" before the timer finishes its cycle the timer's BIT 24 output will finish out the 300 ms pulse. Readdressing the device with bit 19 "HI" before the timer finishes its cycle will extend the BIT 24 output pulse width by 300 ms. Addressing should be performed immediately after the 50 Hz output transitions "HI". BIT 24's output state is not guaranteed during the first 300 ms after V_{CC_1} power up as a result of a timer reset in progress.

TABLE V

Bit		FUNCTION OF PINS 3, 4, & 5
20	21	
0	0	Status of Bits 22-24
0	1	Test mode 1
1	0	Test mode 2
1	1	Test mode 3

TEST MODE OPERATION

Test Mode 1: Enables the BIT output pins to edge trigger the phase comparator inputs and monitor an internal lock detector. BIT 22 negative edge triggers the reference divider input of the phase comparator if the reference divider state is low. BIT 23 provides the open collector ORing of the phase comparator's pump up and down outputs. BIT 24 negative edge triggers the N counter input of the phase comparator if the N counter state is preconditioned low.

Test Mode 2: Enables the BIT outputs to clock the programmable N counter, monitor its output, and force either its load or count condition. BIT 22 provides the N counter output which negative edge triggers the phase comparator and which appears low one N counter clock pulse before it reloads. BIT 23 positive edge triggers the N counter's clock input if the prescaler's output is preconditioned HI. BIT 24 clears the N counter output so that loading will occur on the next N counter clock edge.

Test Mode 3: Enables the BIT outputs to clock the 50 Hz and 10 kHz reference dividers and monitor the reference divider input to the phase comparator. BIT 22 positive edge clocks the 10 kHz reference divider chain if the 10 kHz output is preconditioned HI. BIT 23 positive edge clocks the 50 Hz divider chain. BIT 24 is the reference divider negative edge trigger input to the phase comparator.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CCM}	7V
V_{CC1}	7V
V_{CC2}	15V
Input Voltage	7V
Output Voltage	
Logic	7V
Op Amp and Mixer Outputs	15V
ESD Sensitivity	1000V
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CCM}	3.5	5.5	V
V_{CC1}	4.5	5.5	V
V_{CC2}	7.0	12.0	V
Temperature, T_A	−40	+85	°C
Mixer I_{BIAS} (Mixer + $\overline{\text{Mixer}}$ Current)	1	20	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Test Conditions		Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage				2.0			V
V_{IL}	Logic "0" Input Voltage						0.8	V
I_{IH}	Logic "1" Input Current		V_{IN} = 5.5V				10	μA
I_I	Logic "1" Input Current		Data, Clock and Enable Inputs, V_{IN} = 7V				100	μA
I_{IL}	Logic "0" Input Current		Data, Clock and Enable Inputs, V_{IN} = 0V				−10	μA
V_{OH}	Logic "1" Output Voltage	2 MHz	I_{OH} = −20 μA		V_{CCM}−0.3			V
			I_{OH} = −400 μA		V_{CCM}−2			V
		Op Amp	I_{OH} = −1.0 mA		V_{CC2}−1.5			V
V_{OL}	Logic "0" Output Voltage	2 MHz	I_{OL} = 20 μA				0.3	V
			I_{OL} = 400 μA				0.4	V
		50 Hz	I_{OL} = 250 μA				0.3	V
		Bit Outputs	I_{OL} = 1 mA				0.3	V
		Op Amp	I_{OL} = 1.0 mA				1.5	V
V_{BIAS}	Op Amp Input VΔ		Op Amp I/O Shorted, V_{CC1} = 5.5V, V_{CC2} = 12V, CPO = TRI-STATE®, Op Amp I_{OH} vs. I_{OL} Applied				200	mV
I_{CEX}	High Level Output Current	Bit Outputs	V_{CC1} = 4.5V, V_O = 8.8V				100	μA
		50 Hz	V_{CCM} = 3.5V, V_O = 5.5V				10	μA
		Mixers	V_{CCL} = V_{CC1} = 4.5V, V_O = 12V				100	μA
I_{CPO}	Charge Pump Program Current		0.25 mA < I_{CPO} < 1.0 mA, 2 I_{PROG} = V_{CC1}/R_{PROG}, Measured I_{PROG} to CPO	Pump-up	−30	2 I_{PROG}	+30	%
				Pump-down	−30	2 I_{PROG}	+30	%
				TRI-STATE		0	100	nA
I_{CCM}	V_{CCM} Supply Current (Static)		V_{CCM} = 5.5V, OSCC = High			0.5	1.0	mA
I_{CC1} + I_{CCL}	V_{CC1} + V_{CCL} Supply Current		V_{CC} = 5.5V, Bits Hi, I_{MXR} and I_{PROG} Open			25	35	mA
I_{CC2}	V_{CC2} Supply Current		V_{CC2} = 12V			1.5	2.5	mA
Mixer I_{BIAS}	Mixer + $\overline{\text{Mixer}}$ Current (Note 4)		V_{CC1} = V_{CCL} = 5.5V, Mixer = $\overline{\text{Mixer}}$ = 12V		−25	4 I_{MXR}	+25	%
RF_{IN}	Mixer Input Max Signal Level		Mixer I_{BIAS} = 20 mA, RF+ or RF− Signal Level			300		mVrms

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits.

Note 2: Unless otherwise specified, min/max limits apply across the −40°C to +85°C temperature range.

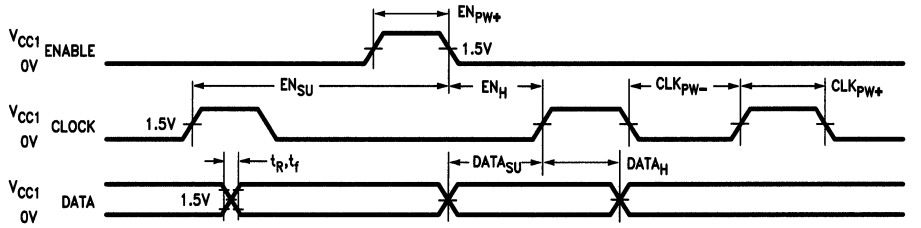
Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

Note 4: Total mixer output current (Mixer + $\overline{\text{Mixer}}$) ≅ 4 times the current into the I_{MXR} pin.

AC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	20%–80% Rise Time	V_{CC1} = 4.5V to 5.5V		200		ns
t_f	80%–20% Fall Time			200		ns
$DATA_{SU}$	Data Setup Time		100			ns
$DATA_H$	Data Hold Time		100			ns
EN_{SU}	Enable Setup Time		100			ns
EN_H	Enable Hold Time		100			ns
EN_{PW+}	Enable Positive Pulse Width		200			ns
CLK_{PW+}	Clock Positive Pulse Width		200			ns
CLK_{PW-}	Clock Negative Pulse Width		200			ns
VCO f_{max}	VCO Max Frequency	See Typical Wiring Diagram	20		225	MHz
OSC f_{max}	Reference Oscillator Max Frequency	V_{CCM} = 3.5V		12		MHz

Timing Diagram



TL/F/7398–10

MICROWIRE™ Bus Format

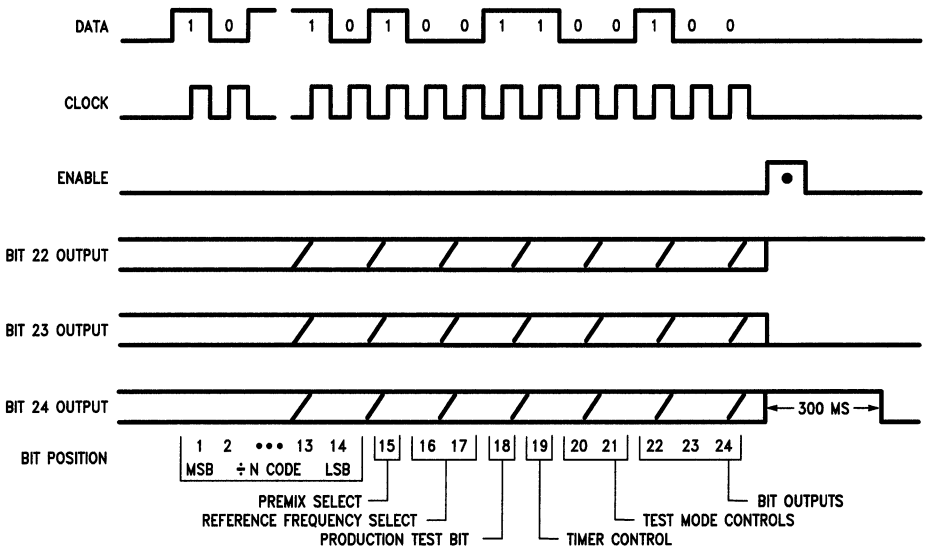


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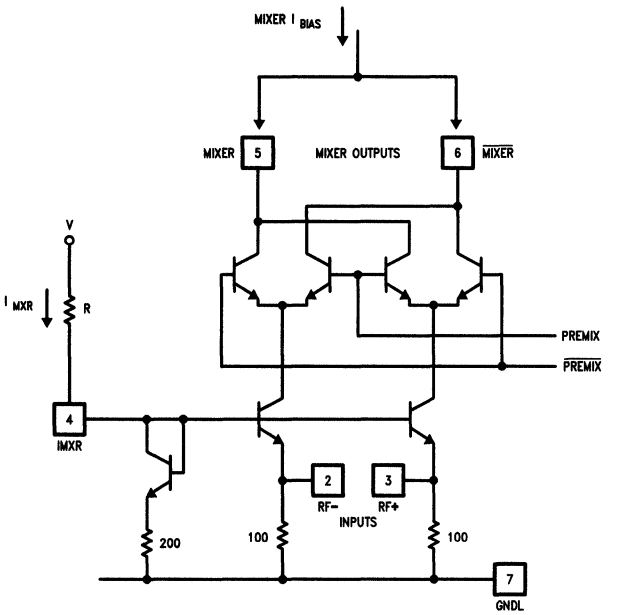
TABLE VI. DS8911 Tuning Characteristics

Mode	IF Frequency (MHz)	Tuning Range (MHz)	VCO Range (MHz)	Premix Modulus	Reference Frequency (kHz)	Tuning Resolution (kHz)	Image (MHz)
LW	11.55/.450	.145–.290	112.4–114.1	10	10	1	22–23
MW	11.55/.450	.515–1.61	99.4–110.2	10	10, 12.5, 25, 100	1, 1.25, 2.5, 10	21–23
SW	11.55/.450	5.94–6.2	53.5 to 56.1	10	10, 12.5, 25	1, 1.25, 2.5	28–30
FM	10.7	87.4–108.1	98.1–118.8	1	10, 12.5, 25, 100	10, 12.5, 25, 100	109–130
WB	10.7	162.4–162.6	151–152	1	12.5, 25	12.5, 25	140–142
TV_1	10.7	59.75–87.75	70.45–98.45	1	25	25	81–109
TV_2	10.7	179.75–215.75	169.1–205.1	1	25	25	158–194

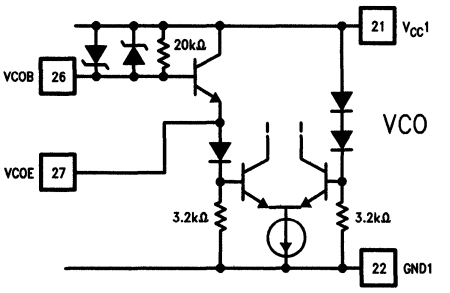
Input and Output Schematics



$$R \cong \frac{4\,(V - 0.8)}{\text{MIXER } I_{BIAS}} - 200\Omega$$

I_{MXR} RESISTOR CALCULATION

TL/F/7398–11



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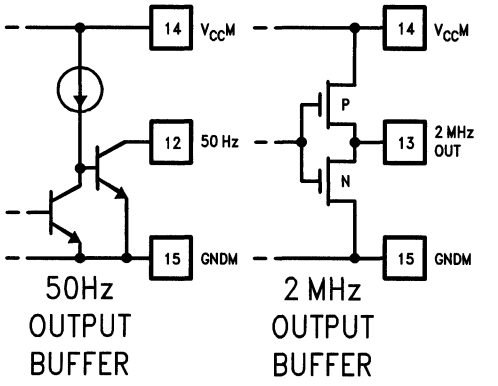
Input and Output Schematics (Continued)



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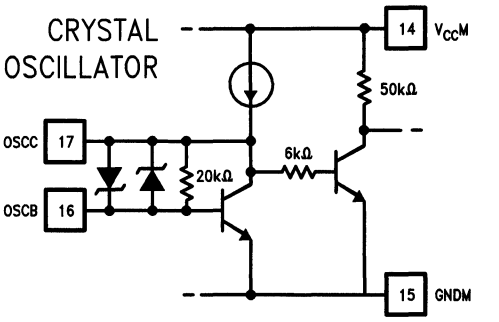

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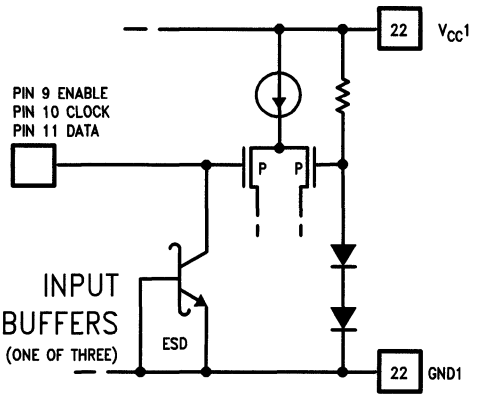

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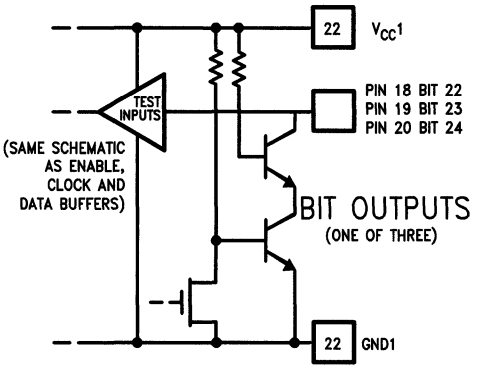
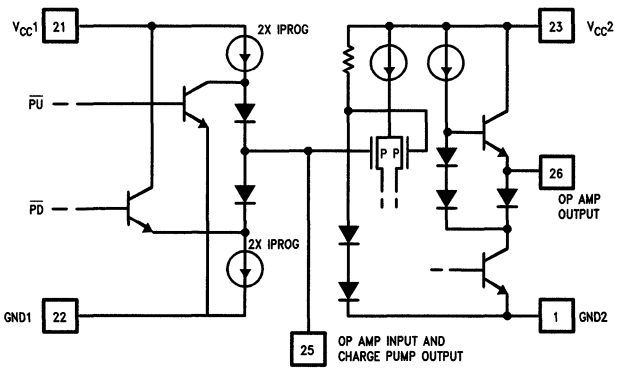
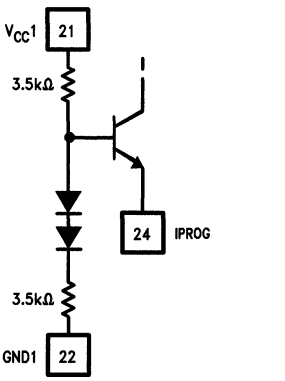


TL/F/7398–16



TL/F/7398–17



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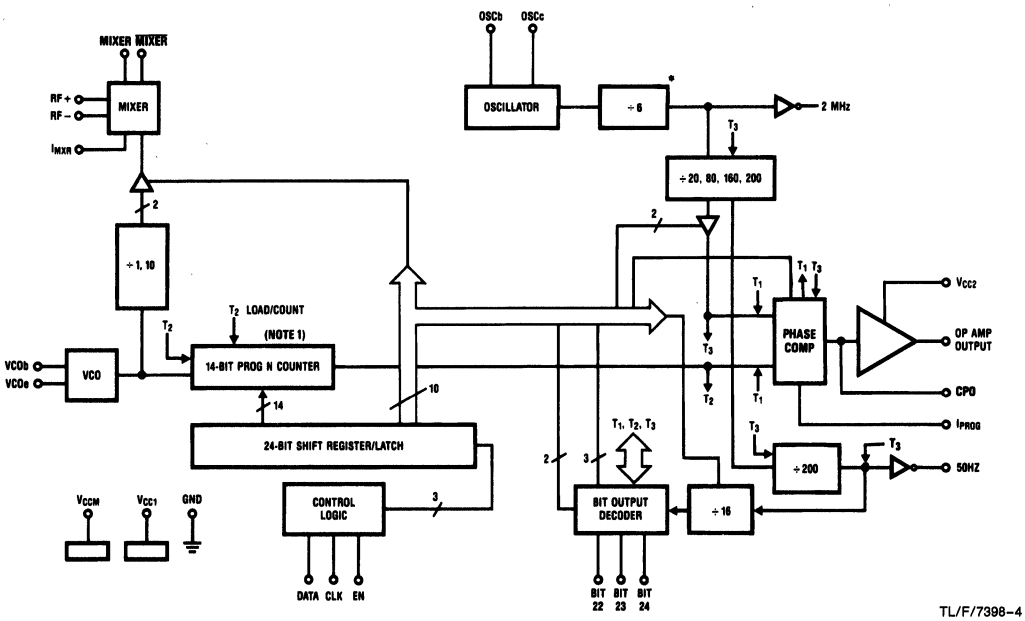
6

Logic Diagram

DS8911/DS8913 PLL Synthesizer



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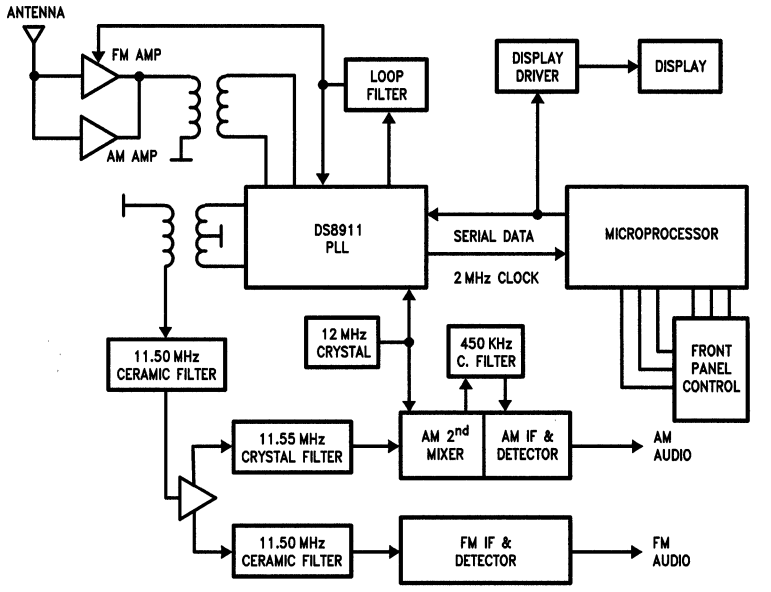
Note 1: The 14 bit programmable N counter is a dual modulus counter with 31/32 prescaler. The minimum continuous modulus of the N counter is 961. (There are a limited number of valid modulus codes below 961.)

*The DS8913 has ÷ 5

Typical Application Diagram

AM/FM ETR Radio Application



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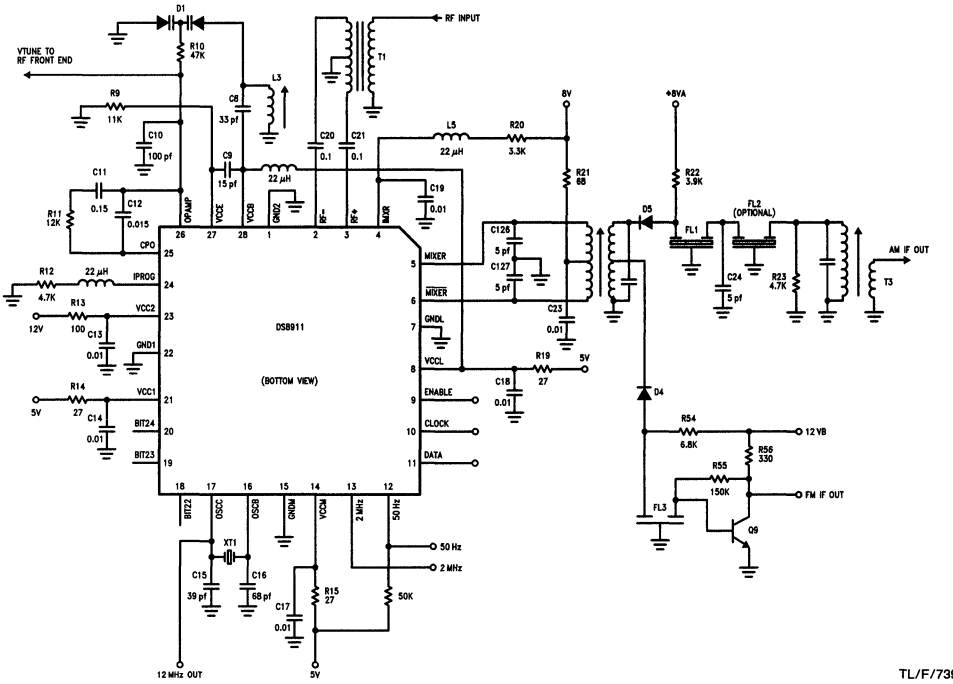
Wiring Diagrams

Configuration Using PLL and First Mixer Functions



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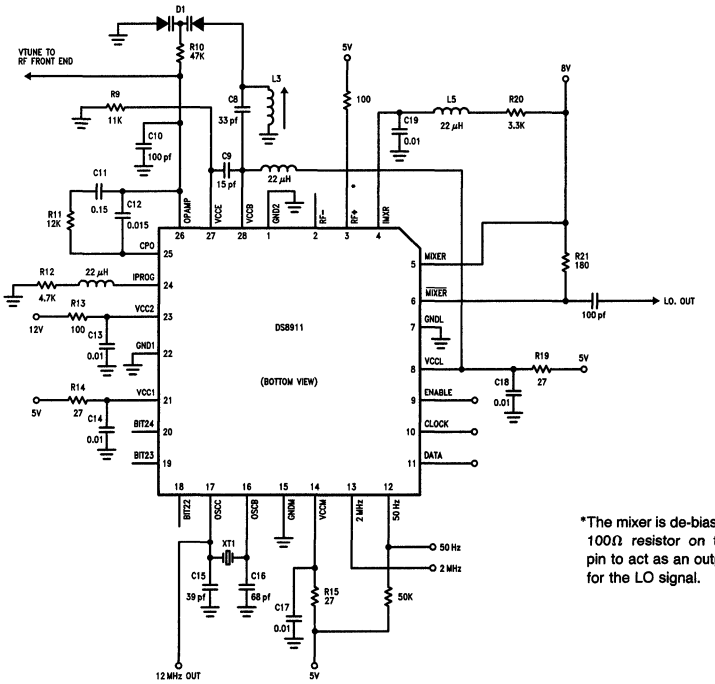
Configuration Using PLL with LO Bypassing Mixer



*The mixer is de-biased by the 100Ω resistor on the RF+ pin to act as an output buffer for the LO signal.

TL/F/7398–21

National Semiconductor

MM5368 CMOS Oscillator Divider Circuit

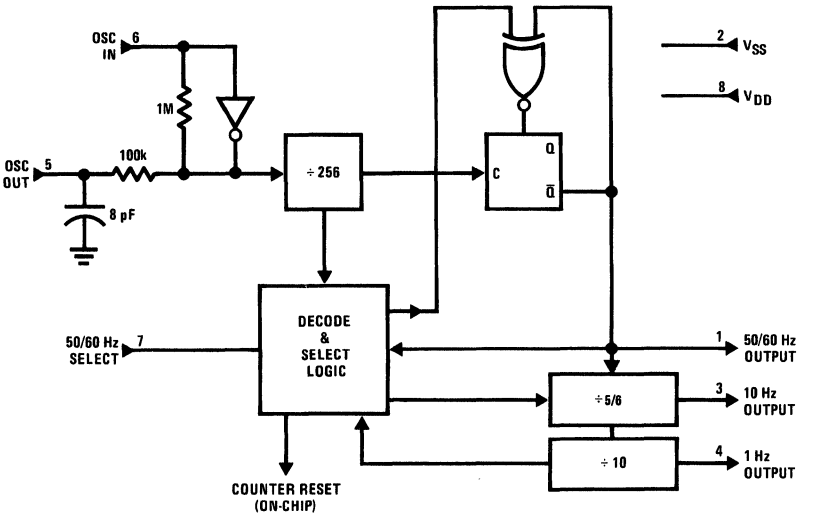
General Description

The MM5368 is a CMOS integrated circuit generating 50 or 60 Hz, 10 Hz, and 1 Hz outputs from a 32 kHz crystal (32,768 Hz). For the 60 Hz selected output the input time base is divided by 546.133, for the 50 Hz mode it is divided by 655.36. The 50/60 Hz output is then divided by 5 or 6 to obtain a 10 Hz output which is further divided to obtain a 1 Hz output. The 50/60 Hz select input can be floated for a counter reset.

Features

- 50/60 Hz output
- 1 Hz output
- 10 Hz output
- Low power dissipation
- Fully static operation
- Counter reset
- 3.5V–15V supply range
- On-chip oscillator—tuning and load capacitors are the only required external components besides the crystal. (For operation below 5V it may be necessary to use an ~ 1 MΩ pullup on the oscillator output to insure start-up.)

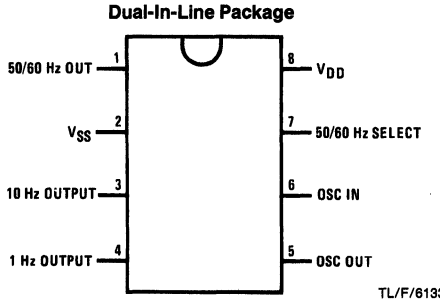
Block and Connection Diagrams



TL/F/6133–1

FIGURE 1

Dual-In-Line Package



TL/F/6133–2

Top View

FIGURE 2

Order Number MM5368N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Maximum V_{DD} Voltage	16V
Operating V_{DD} Range	$3.5V \leq V_{DD} \leq 15V$
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics T_A within operating range, $V_{SS} = 0V$

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current Drain	$V_{DD} = 15V$; 50/60 Select Floating			10	μA
Operating Current Drain	$f_{IN} = 32$ kHz, $V_{DD} = 3.5V$			60	μA
	$f_{IN} = 32$ kHz, $V_{DD} = 15V$			1500	μA
Maximum Input Frequency	$V_{DD} = 3.5V$			64	kHz
	$V_{DD} = 15V$			500	kHz
Output Current Levels	$V_{DD} = 5V$				
Logical "1", Source	$V_{OH} = V_{SS} + 2.7V$			−400	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	400			μA
	$V_{DD} = 9V$				
Logical "1", Source	$V_{OH} = V_{SS} + 6.7V$			−1500	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	1500			μA
Input Current Levels	50/60 Select Input (Note 1)				
Logical "1" (I_{IH})	$V_{DD} = 3.5V$, $V_{IN} \geq 0.9\ V_{DD}$			50	μA
Logical "1" (I_{IH})	$V_{DD} = 15V$, $V_{IN} \geq 0.9\ V_{DD}$			3	mA
Logical "0" (I_{IL})	$V_{DD} = 3.5V$, $V_{IN} \geq 0.1\ V_{DD}$			20	μA
Logical "0" (I_{IL})	$V_{DD} = 15V$, $V_{IN} \geq 0.1\ V_{DD}$			1	mA

Note 1: The input current level test is performed by first measuring the open circuit voltage at the 50/60 Hz select pin. If the voltage is "high", make the I_{IH} test. If the voltage is "low", make the I_{IL} test. The state of the 50/60 Hz select pin may be changed by applying a pulse to OSC IN (pin 6) while the 50/60 Hz pin is open circuit.

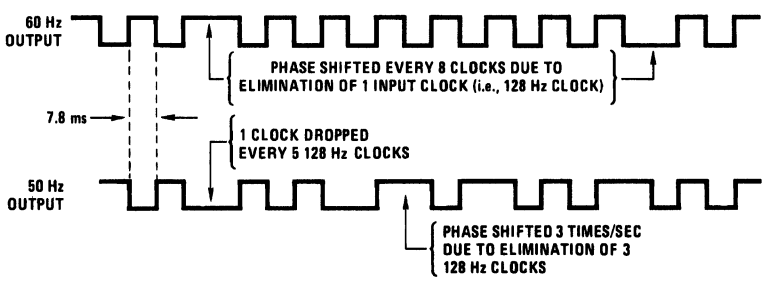
Functional Description *(Figure 1)*

The MM5368 initially divides the input time base by 256. From the resulting frequency (128 Hz for 32 kHz crystal) 8 clock periods are dropped or eliminated during 60 Hz operation and 28 clock periods are eliminated during 50 Hz operation. This frequency is then divided by 2 to obtain a 50 or 60 Hz output. This output is not periodic from cycle to cycle; however, the waveform repeats itself every second. Straight divide by 5 or 6 and 10 are used to obtain the 10 Hz output and the 1 Hz outputs.

The 60 Hz mode is obtained by tying pin 7 to V_{DD}. The 60 Hz output waveform can be seen in *Figure 3*. The 10 Hz and 1 Hz outputs have an approximate 50% duty cycle. In the 50 Hz mode the 50/60 select input is tied to V_{SS}. The 50 Hz output waveform can be seen in *Figure 3*. The 10 Hz output has an approximate 40% duty cycle and the 1 Hz output has an approximate 50% duty cycle.

For the 50/60 Hz select input floating, the counter chain is held reset, except for the initial toggle flip-flop which is needed for the reset function. A reset may also occur when the input is switched *(Figure 4)*. To insure the floating state, current sourced from the input must be limited to 1.0 μA and current sunk by the input must be limited to 1.0 μA for $V_{DD} = 3.5V$.

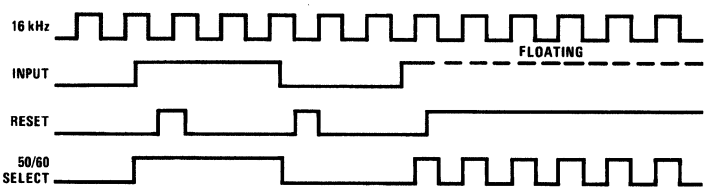
Timing Diagrams



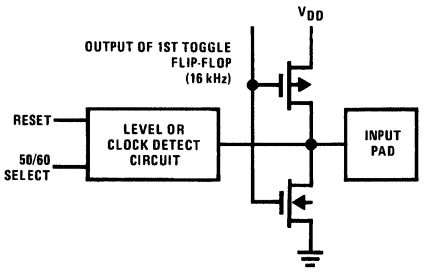
TL/F/6133–3

FIGURE 3. 50/60 Hz Output

Timing Diagrams (Continued)



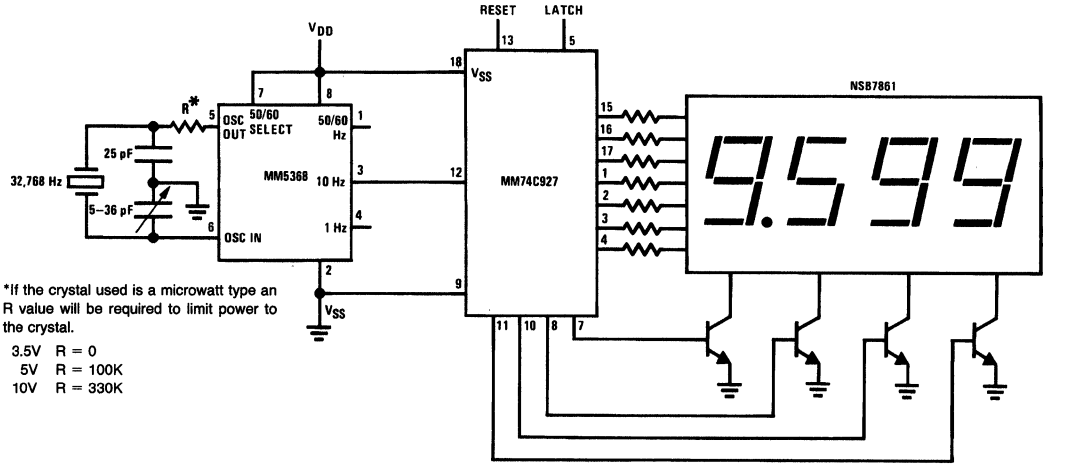
TL/F/6133–4



TL/F/6133–5

FIGURE 4. 50/60 Select and Reset

Typical Applications



*If the crystal used is a microwatt type an R value will be required to limit power to the crystal.

3.5V R = 0
5V R = 100K
10V R = 330K

TL/F/6133–6

FIGURE 5. 10 Minute (9:59.9) Timer

National Semiconductor

MM5369 17 Stage Oscillator/Divider

General Description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the cyrstal frequency for tuning purposes and the 17th stage output. The MM5369 is available in an 8-lead dual-in-line epoxy package.

Features

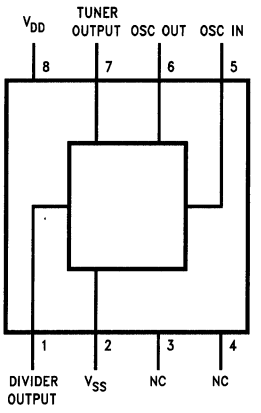
- Crystal oscillator
- Two buffered outputs
  - Output 1 crystal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10V)
- Wide supply range 3V–15V
- Low power
- Fully static operation
- 8-lead dual-in-line package
- Low Current

Option

- MM5369AA — 3.58 MHz to 60 Hz

Connection and Block Diagrams

Dual-In-Line Package



TL/F/10820–1

Top View

Order Number MM5369AA/N
See NS Package Number N08E

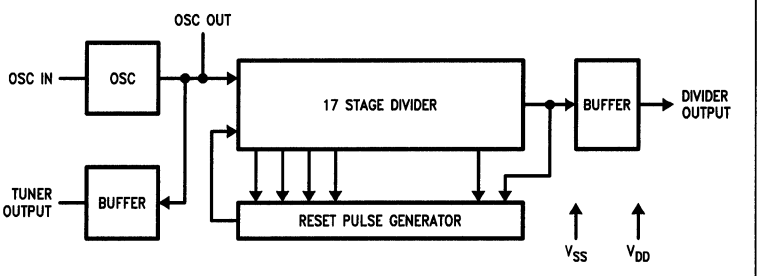


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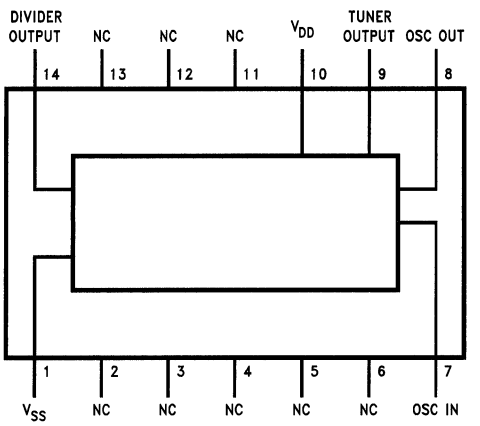
FIGURE 2



TL/F/10820–8

Order Number MM5369AA/M
See NS Package Number M14A

6

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	16V
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = GND, $3V \leq V_{DD} \leq 15V$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current Drain	V_{DD} = 15V			10	μA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V V_{DD} = 6V	DC DC		4.5 2	MHz MHz
Output Current Levels	V_{DD} = 10V V_O = 5V				
Logical "1" Source		500			μA
Logical "0" Sink		500			μA
Output Voltage Levels	V_{DD} = 10V I_O = 10 μA				
Logical "1"		9.0			V
Logical "0"				1.0	V

Note: For 3.58 MHz operation, V_{DD} must be ≥ 10V.

Functional Description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2.*

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

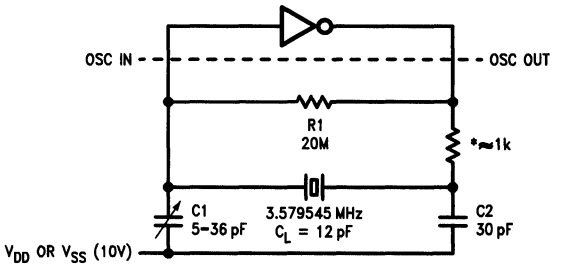
DIVIDER

A pulse is genertaed when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs.

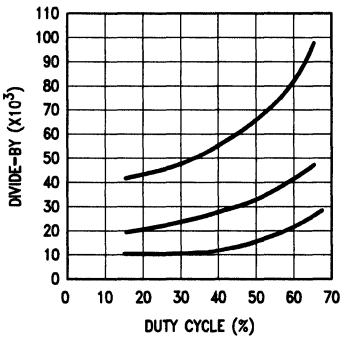
Functional Description (Continued)



TL/F/10820–3

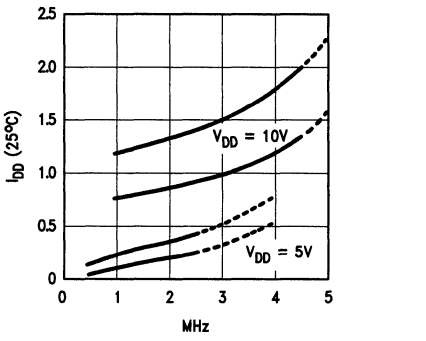
*To be selected based on xtal used

FIGURE 3. Crystal Oscillator Network



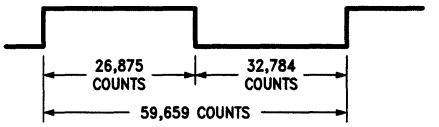
TL/F/10820–4

FIGURE 4. Plot of Divide-By vs Duty Cycle



TL/F/10820–5

FIGURE 5. Typical Current Drain vs Oscillator Frequency



TL/F/10820–6

FIGURE 6. Output Waveform for the MM5369AA

National Semiconductor

MM5437 Digital Noise Source

General Description

The MM5437 device is a monolithic metal gate NMOS integrated circuit which may be used as a digital noise source or a pseudo-random number generator. The part is designed to produce a broadband white noise signal with uniform noise quality and output amplitude. Two outputs are provided. The first, OUT 1, is sequence-limited to reduce "thumps." The other output, OUT 2, is the last stage of the shift register when $\overline{\text{CONTROL 2}}$ is left floating or is pulled up. Typical cycle time is one minute. Data is clocked in and out on the rising edge of the clock.

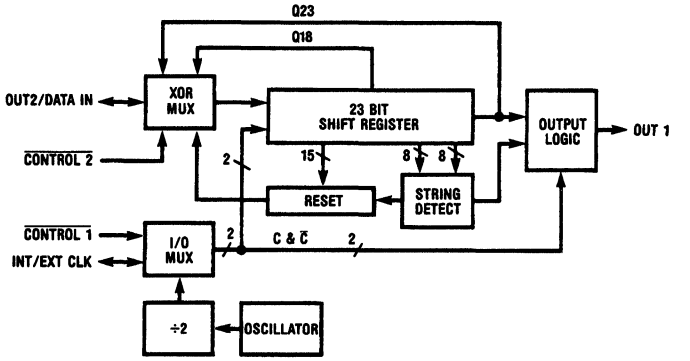
Applications

- Electronic musical rhythm instrument sound generators
- Music synthesizer white and pink noise generators
- Room acoustics testing/equalization
- Pseudo-random number generator

Features

- Internal self-contained oscillator
- Single supply voltage range of 4.5V to 11V
- TTL compatible at 5V
- Normal and sequence-limited outputs
- Low power consumption
- One minute cycle time
- External loading and clocking capability
- Automatic reset for all-zeros state
- Uniform noise quality
- Uniform noise amplitude
- Eliminate noise preamps
- Single component insertion

Block and Connection Diagrams



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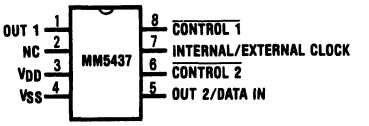


TL/F/5260–2

Top View

Order Number MM5437N
See NS Package Number N08E

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Operating Supply Voltage, V_{DD}	12V
Storage Temperature, T_S	−65°C to +150°C
Operating Temperature, T_A	−40°C to +85°C
DC Output Current, per pin	±12 mA
Lead Temp. (Soldering, 10 seconds)	+300°C

DC Electrical Characteristics T_A within operating range, V_{SS} = 0V, V_{DD} = 11V, unless specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (V_{DD})		4.5		11	V
Supply Current (I_{DD})	V_{DD} = 4.5V (No load) V_{DD} = 11V (No load)			4 5	mA mA
Output Voltage Levels Logic '0' Logic '1'	 I_{OL} = +1.6 mA, V_{DD} = 4.5V I_{OH} = −400 μA, V_{DD} = 4.5V	 V_{SS} 2.4		 0.4 V_{DD}	 V V
Input Voltage Levels Logic '0' Logic '1'		 2.0		 0.8 	 V
Input Currents Logic '0' Logic '1'	 V_{IN} = 0.4V V_{IN} = 2.4V			 200 200	 μA μA
Half Power Point*		30		140	kHz
Cycle Time		25		110	sec.

*Half Power Point = 0.45 (Shift Register Clock Frequency)

AC Timing $-40°C \le T_A \le +85°C$, $4.5V \le V_{DD} \le 11V$

Symbol	Parameter	Min	Max	Units
t_S	Data Set Up Time Prior to Clock	100		ns
t_H	Data Hold Time After Clock	100		ns
t_{C2DV}	$\overline{\text{CONTROL 2}}$ to Data Out Valid		100	ns
t_{CLKDV}	Clock to Data Out Valid		700	ns
t_{PH}	Clock Pulse Width High	1.5		μs
t_{PL}	Clock Pulse Width Low	1.5		μs
t_r, t_f	Input Rise and Fall Times		220	ns

Inputs/Outputs

$\overline{\text{CONTROL 1}}$: A mode switch input, which when held at a logic "1" or left floating, gates the internal oscillator onto the INT/EXT CLK pin. When $\overline{\text{CONTROL 1}}$ is at a logic "0", the shift register can be driven externally through the INT/EXT CLK pin.

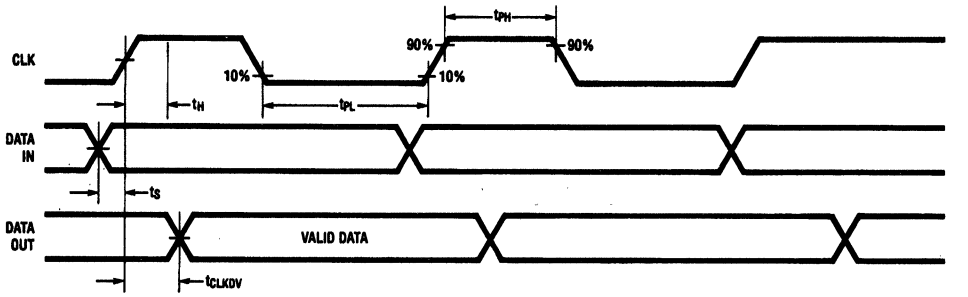
$\overline{\text{CONTROL 2}}$: A mode switch input, which when held at a logic "1" or left floating, gates the last stage of the shift register onto the OUT 2/DATA IN pin. When $\overline{\text{CONTROL 2}}$ is at a logic "0", the shift register can be loaded externally through the OUT 2/DATA IN pin.

OUT 1: An output pin for the sequence-limited output from the shift register.

INT/EXT CLK: An input/output pin. See $\overline{\text{CONTROL 1}}$ for description.

OUT 2/DATA IN: An input/output pin. See $\overline{\text{CONTROL 2}}$ for description.

Timing Diagrams



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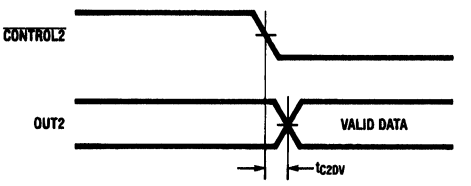
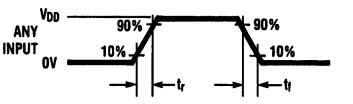
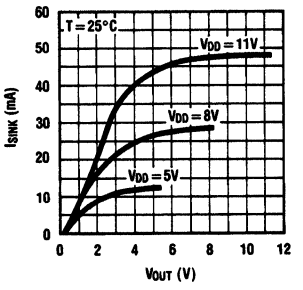


TL/F/5260–4



TL/F/5260–5



TL/F/5260–6

FIGURE 1. I_{SINK} vs V_{OUT}

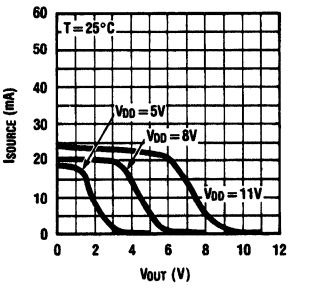


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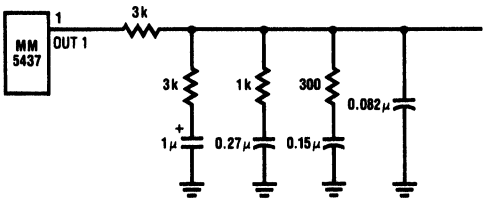
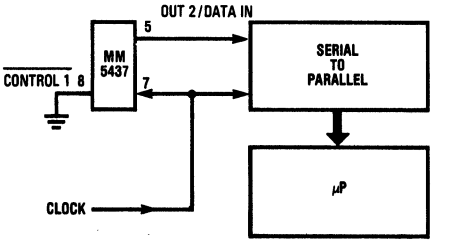
FIGURE 2. I_{SOURCE} vs V_{OUT}

Typical Applications



TL/F/5260–8

FIGURE 3. Pink Noise Generator



TL/F/5260–9

FIGURE 4. Pseudo-Random Number Generator

Section 7

Special Automotive

Section 7 Contents

National Semiconductor

Automotive Standard Products

High Current Switch Selection Guide

Device	Drivers/ Package	Continuous Current	Peak Current	Input Voltage Range	Diagnostics
LM1921*	1	1.0A	2.0A	4.5V to 26V	none
LM1950*	1	750 mA	1.4A	4.75V to 26V	none
LM1951*	1	1.0A	2.5A	4.5V to 26V	Error Flag
LMD18400*	4	1.0A	3.0A	6V to 28V	Error Flag Thermal Shutdown Flag Data Output provides switch status feedback, output load fault conditions and thermal and overvoltage shut-down status.

*All incorporate Automotive transient protection.

Liquid Level Sensor Selection Guide

Output Type	LM903	LM1042	LM1830
	Digital HI/LO	Analog	Digital HI/LO
Operation Method	Thermoresistive Probe	Thermoresistive Probe	Conductive Liquid

Special Amplifiers Selection Guide

	LM1815	LM1964
Typical Application	Adaptive Sense Amplifier	Sensor Interface Amplifier
Sensor	Inductive Pickup	Lambda Sensor
Key Features	• Operates from 2.5V to 12V Supply • Adaptive Hysteresis • True Zero Crossing Timing Reference	• Normal Operation Guaranteed with inputs up to 3V below Ground on a Single Supply • Fully Protected Inputs • Input Open Circuit Detection

National Semiconductor

LM903 Fluid Level Detector

General Description

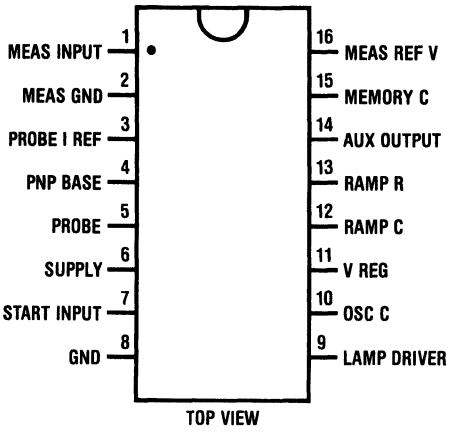
The LM903 uses the thermal-resistive probe technique to measure the level of nonflammable fluids. A low fluid level is indicated by a warning lamp operating in continuous or flashing mode. All supervisory requirements to control the thermal-resistive probe, including short and open circuit probe detection, are incorporated within the device. The circuit has possible applications in the detection of hydraulic fluid, oil level, etc., and may be used with partially conducting fluids.

Features

- Flashing or continuous warning indication
- Warning threshold externally adjustable
- Control circuitry for thermal-resistive probe
- Switch on reset and delay to avoid transients
- 600 mA flashing lamp drive capability
- Short and open circuit probe detection
- 70V transient protection on supply and control input
- 7V–18V supply range
- Internally regulated supply
- −40°C to +80°C operation

Connection Diagram

Dual-In-Line Package



TL/H/5699–1

Order Number LM903N
See NS Package Number N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	18V
Control Input Voltage (Pin 7)	18V
Transient Voltage (Pins, 6, 7, 9) 10 ms (Note 1)	70V
Output Current (Pin 4) I_4 (Sink)	10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature	−55°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

V_{CC} = 12V, C_T = 33 μF, R_T = 7.5 kΩ, T_A within operating range except where stated otherwise

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		7.0	18	7.0	13	18	V
I_S	Supply Current			50			50	mA
V_{REG}	Regulated Voltage		5.5	6.2	5.3	5.8	6.3	V
	Regulation Temperature Drift	V_{CC} = 7.2V–18V		105		500		mV μV/°C
V_6–V_3	Probe Current Reference Voltage		2.0	2.35	1.95	2.20	2.40	V
V_{REF}	Measurement Reference Voltage		790	900	780	850	910	mV
R_{REF}	Reference Input Resistor					1.2		kΩ
V_7	Start Input Logic High Level				1.6			V
V_7	Start Input Logic Low Level						1.0	V
I_7	High Input Current	Latch Off					100	nA
I_7	Latch Holding Current	Latch On				2.5		nA
R_7	Resistance Pin 7	Latch On				22		kΩ
I_{12}	Ramp Current	See Timing Diagram						
	Charging	V_{12} = 0V–1V	600	1100	590		1100	μA
		V_{12} = 1V–4V	53	93	50		96	μA
	Discharging	V_{12} = 4.1V	−700	−450	−710		−440	μA
		V_{12} = 0.5V	−650	−400	−660		−390	μA
V_{12}	Ramp Threshold	See Timing Diagram						
	Probe Current Start		570	850	550	710	870	mV
	First Measurement		910	1200	890	1055	1220	mV
	Second Measurement		910	1240	890	1080	1270	mV
V_1	Probe Input Voltage Range	V_{CC} = 7.5V–18V			1		V_{REG}−1.0	V
V_5	Probe Open-Circuit Threshold	At Pin 5			V_{REG}−0.85	V_{REG}−0.6		V
V_5	Probe Short-Circuit Threshold					0.6	0.85	V
I_1	Pin 1 Input Leakage Current	Pin 1 = 300 mV	−3.5	+3.5			+5.0	nA
I_{15}	Pin 15 Leakage Current	V_{15} = 2V, V_7 = 12V	−3.5	3.5				μA
	Pin 15 Charging Current	V_{15} = 4V, V_7 = 12V	60					μA
f_9	Lamp Oscillation Frequency	C_L = 3.3 μF			0.5	1.5	2.5	Hz
I_9	Lamp Driver Current	Flashing Mode					600	mA
V_9	Lamp Driver Saturation	I_9 = 200 mA		200			250	mA

Electrical Characteristics (Continued)

V_{CC} = 12V, C_T = 33 μF, R_T = 7.5 kΩ, T_A within operating range except where stated otherwise

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{14}	Auxiliary Output Voltage	Lamp OFF			5.0			V
		Lamp ON					1.2	V
V_1	Alarm Level	(Difference Between First and Second Measurement)			230	280	330	mV

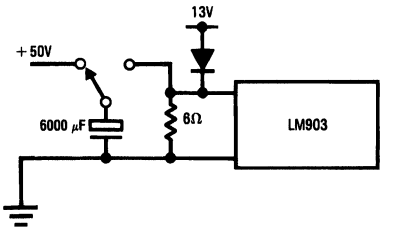
Sensitivity to Electrostatic Discharge: Pins 7, 10, 13, and 14 will withstand greater than 1500V when tested using 100 pF and 1500Ω in accordance with National Semiconductor standard ESD test procedures. All other pins will withstand in excess of 2 kV.

Note 1: Test circuit for overvoltage capability at pins 3, 6, 7.

Note 2: Guaranteed 100% production tested at 25°C. These limits are used to calculate outgoing quality levels.

Note 3: Limits guaranteed to include parametric variations. T_A = −40°C to +80°C and from V_{CC} = 7.5V–18V. These limits are not used to calculate AOQL figures.

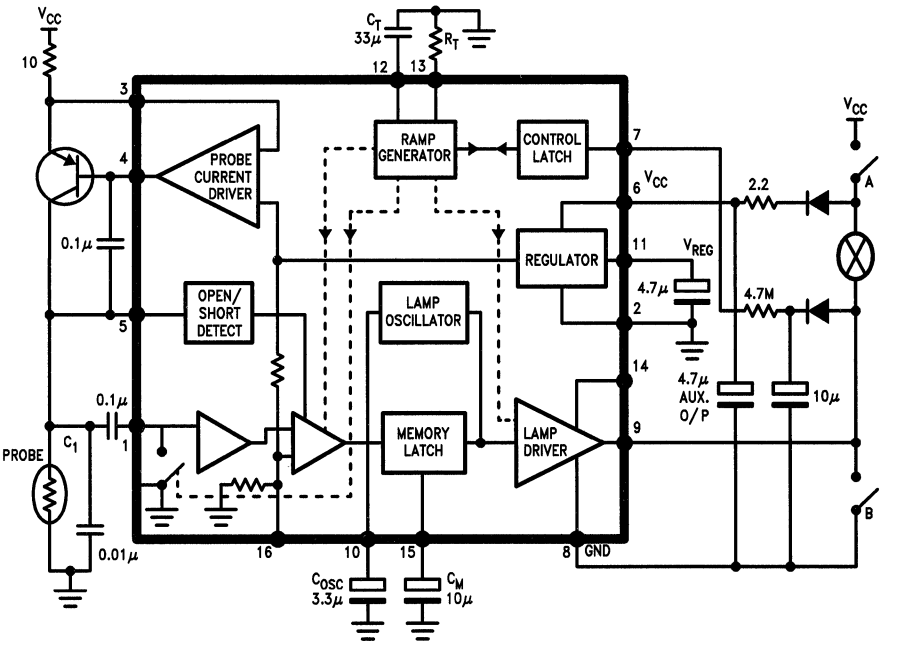
Note 4: Variations over temperature range are not production tested.



TL/H/5699–2

In Lamp ON condition, I_9 should be limited to 600 mA.

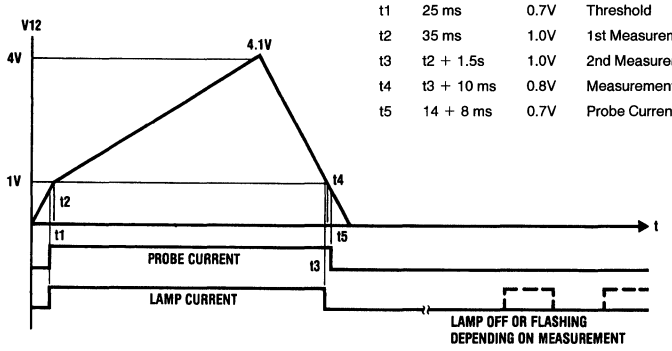
Block and Application Circuit



TL/H/5699–3

Memory capacitor on pin 15 is set
High—Lamp off
Low—Lamp on

Circuit Timing Diagram



t1	25 ms	0.7V	Threshold
t2	35 ms	1.0V	1st Measurement
t3	t2 + 1.5s	1.0V	2nd Measurement
t4	t3 + 10 ms	0.8V	Measurement Latched
t5	14 + 8 ms	0.7V	Probe Current Off

TL/H/5699–4

Circuit Operation

A measurement is initiated when the supply is applied, provided the control input pin 7 is low. Once a measurement is commenced, pin 7 is latched low and the ramp capacitor on pin 12 begins to charge. After 25 ms when switch-on transients have subsided, a constant current is applied to the thermo-resistive probe. The value of probe current, which is supplied by an external PNP transistor, is set by an external resistor across an internally generated 21V reference. The lamp current is applied at the start of probe current.

35 ms after switch-on, the voltage across the probe is sampled and held on external capacitor C1 (leakage current at pin 1 less than 1 nA). After a further 1.5 seconds the difference between the present probe voltage and the initial probe voltage is measured, multiplied by 3 and compared with a reference voltage of 850 mV (externally adjustable via pin 16). If the amplified voltage difference is less than the reference voltage the lamp is switched off, otherwise the lamp commences flashing at 1 Hz to 2 Hz. 10 ms later the measurement latch operates to store the result and after a further 8 ms the probe current is switched off.

A second measurement can only be initiated by interrupting the supply. An external CR can be arranged on pin 7 to prevent a second measurement attempt for 1 minute. The measurement condition stored in the latch will control the lamp.

PROBES

The circuit effectively measures the thermal resistance of the probe. This varies depending on the surrounding medium (*Figure 1*). It is necessary to be able to heat the probe with the current applied and, for there to be sufficient change in resistance with the temperature change, to provide the voltage to be measured.

Probes require resistance wire with a high resistivity and temperature coefficient. Nickel cobalt alloy resistance wires are available with resistivity of 50 $\mu\Omega$cm and temperature coefficient of 3300 ppm which can be made into suitable probes. Wires used in probes for use in liquids must be designed to drain freely to avoid clogging. A possible arrangement is shown in *Figure 2*.

The probe voltage has to be greater than 0.7V to prevent short circuit probe detection less than 5V to avoid open circuit detection. With a 200 mA probe current this gives a probe resistance range of 4Ω to 25Ω. This low value makes it possible to use the probe in partially conducting fluids.

Using resistance wire of 50 $\mu\Omega$cm resistivity, 8 cm of 0.08 mm (40 AWG) give approximately 8Ω at 25°C. Such a probe will give about 500 mV change between first and second measurements in air, and 100 mV change with oil, hydraulic fluid, etc., in the application circuit. With an alarm threshold of 280 mV (typ) lack of fluid can readily be detected. As the probe current, measurement reference and measurement period are all externally adjustable, there is freedom to use different probes and fluids.

Another possibility is the use of high temperature coefficient resistors made for special applications and positive temperature coefficient thermistors. The encapsulation must have a sufficiently low thermal resistance so as not to mask the change due to the different surrounding mediums, and the thermal time constant must be quick enough to enable the temperature change to take place between the two measurements. The ramp timing could be adjusted to assist this. Probes in liquids must be able to drain freely.

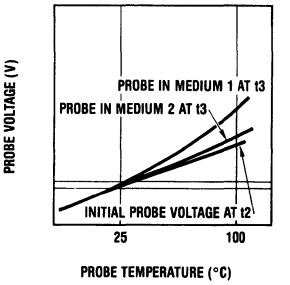


FIGURE 1. Typical Thermo-Resistive Probe

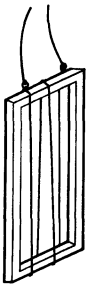


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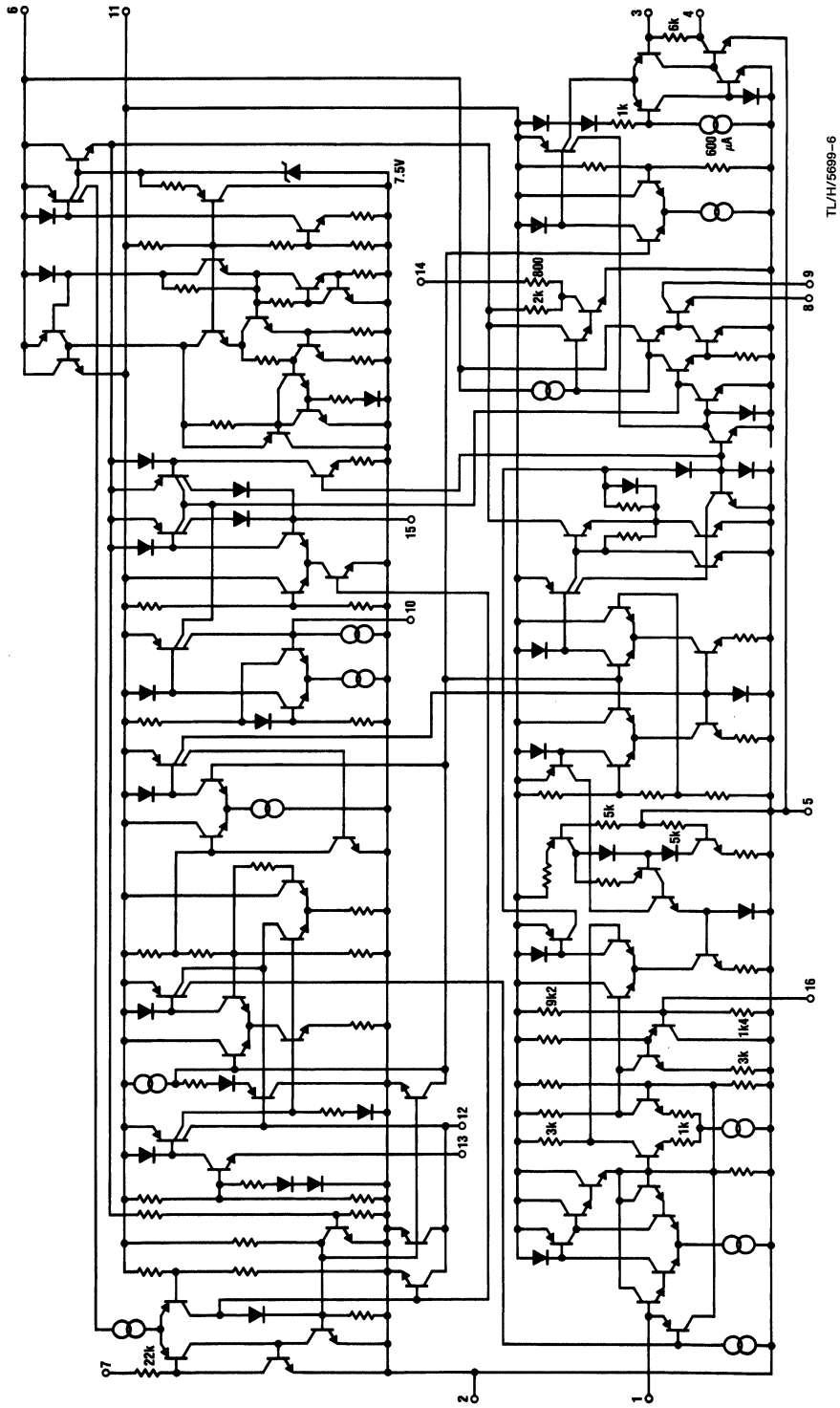
FIGURE 2

Equivalent Schematic Diagram



Application Hints

INTERNAL COMBUSTION ENGINE OIL LEVEL

The basic system provides a single shot measurement when the supply is applied and has a primary application in automotive oil, hydraulic fluid and coolant monitoring. Particularly in the case of the oil level, a valid measurement is only possible before the oil is disturbed. The application circuit shown is arranged such that the measurement is made when the ignition is switched on via switch A. Switch B is the oil pressure sensor and is closed before the engine starts, keeping pin 7 low and enabling the measurement.

STALLING AND RESTART PROTECTION

The 4M7 resistor and 10 μF capacitor connected to pin 7 provide the restart protection. When oil pressure builds up, switch B opens and the 10 μF capacitor charges through the bulb. At switch-off, the capacitor discharges slowly and is capable of preventing a low state on pin 7 for 1 minute. Unless pin 7 is low, a new measurement can not be made and the previous measurement result stored in the memory capacitor on pin 15 is used to control the output.

MEMORY

The pin 15 memory output goes high if a correct measurement is made (lamp off). If the power is removed, pin 15 leakage is less than 3 μA and the memory status is retained for some time. Provided pin 15 voltage does not fall below 3V, the memory capacitor will be refreshed on powering up again. There is no internal pull down on detecting an incorrect measurement. If it is required to use pin 15 as an output indicating the measurement result, an external pull down resistor and buffer will be required.

CONTINUOUS WARNING LAMP

The lamp can be arranged to light continuously by disabling the oscillator with a resistor of 150k or less, connected between pins 10 and 11.

REPETITIVE MEASUREMENTS

Measurements may be repeated by strobing the supply to pin 6. The probe current regulator transistor must have the same supply as pin 6, but the warning lamp can be permanently powered. The lamp will light during each measurement and will flash in between measurements when incorrect conditions are detected.

ALTERNATIVE APPLICATIONS

Gas flow detection: The cooling effect of gas flowing over a probe could be used to provide a warning signal from the LM903 in the event of gas failure.

Automatic top up: With the LM903 strobed continuously, the output may be stored, buffered, and used to drive solenoid valves to correct a fluid level as required.

National Semiconductor

LM1042 Fluid Level Detector

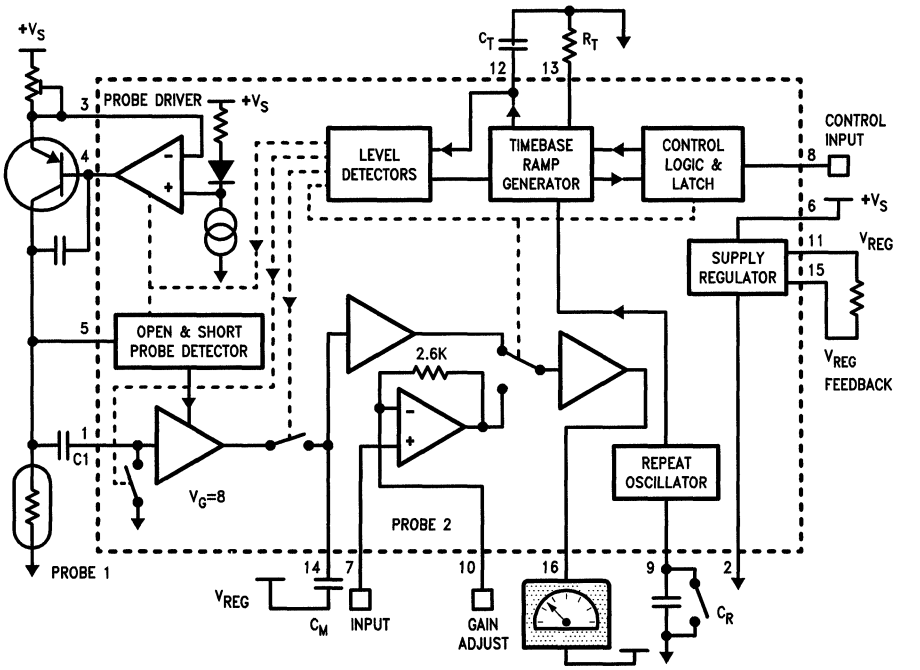
General Description

The LM1042 uses the thermal-resistive probe technique to measure the level of non-flammable fluids. An output is provided proportional to fluid level and single shot or repeating measurements may be made. All supervisory requirements to control the thermal-resistive probe, including short and open circuit probe detection, are incorporated within the device. A second linear input for alternative sensor signals may also be selected.

Features

- Selectable thermal-resistance or linear probe inputs
- Control circuitry for thermal-resistive probe
- Single-shot or repeating measurements
- Switch on reset and delay to avoid transients
- Output amplifier with 10 mA source and sink capability
- Short or open probe detection
- +50V transient protection on supply and control input
- 7.5V to 18V supply range
- Internally regulated supply
- −40°C to +80°C operation

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	32V
Voltage at Pin 8	32V
Positive Peak Voltage (Pins 6, 8, 3) (Note 1) 10 ms 2A	50V
Output Current Pin 4, (I_4)(sink)	10 mA
Output Current Pin 11 (source)	25 mA
Output Current Pin 16	±10 mA
Operating Temperature Range	−40°C to +80°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering 10 sec.)	260°C
Package Power Dissipation T_A = 25°C (Note 8)	1.8W
Device Power Dissipation	0.9W

Electrical Characteristics

V_{CC} = 13V, T_A within operating range except where stated otherwise. C_T = 22 μF, R_T = 12k

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		7.5	18	7.5	13	18	V
I_S	Supply Current			35			35	mA
V_{REG}	Regulated Voltage	Pins 15 and 11 connected	5.7	6.15	5.65	5.9	6.2	V
	Stability Over V_{CC} Range	Referred to value at V_{CC} = 13V (Note 4)		±0.5			±0.5	%
V_6-V_3	Probe Current Reference Voltage		2.15	2.35	2.10	2.25	2.40	V
	Probe Current Regulation Over V_{CC} Range	(Note 4)		±0.5			±0.8	%
T_1	Ramp Timing	See *Figure 5*	20	37	15	31	42	ms
T_2-T_1					3		16	ms
T_4-T_1	Ramp Timing		1.4	2.1	1.4	1.75	2.1	s
T_{STAB}	Ramp Timing Stability	Over V_{CC} Range		+5			±5	%
R_T	Ramp Resistor Range		3	15	3		15.0	kΩ
V_8	Start Input Logic High Level		1.7		1.7			V
V_8	Start Input Logic Low Level			0.5			0.5	V
I_8	Start Input Current	$V_8 = V_{CC}$		100			100	nA
I_8	Start Input Current	V_8 = 0V		300			300	nA
V_{16}	Maximum Output Voltage	R_L = 600Ω from Pin 16 to V_{REG}	$V_{REG}-0.3$		$V_{REG}-0.3$			V
	Minimum Output Voltage			0.5		0.2	0.6	V
	PROBE 1							
G_1	Probe 1 Gain	Pin 1 80 mV to 520 mV (Notes 6, 7)	9.9	10.4		10.15		
	Non-linearity of G_1	Pin 1 80 mV to 520 mV (Note 7)	−1	+1	−2	0	2	%
OS_1	Pin 1 Offset	(Note 7)				±5		mV
	PROBE 2							
G_2	Probe 2 Gain	Pin 7 240 mV to 1.562V (Note 7)	3.31	3.49		3.4		
	Non-linearity of G_2	Pin 7 240 mV to 1.562V (Note 7)	−1	+1	−2	0.2	2	%
OS_7	Pin 7 Offset	(Note 7)				±5		mV
R_7	Input impedance					5		MΩ

Electrical Characteristics

V_{CC} = 13V, T_A within operating range except where stated otherwise. C_T = 22 μF, R_T = 12k (Continued)

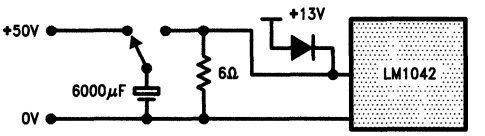
Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_1	Probe 1 Input Voltage Range	V_{CC} = 9V to 18V V_{CC} = 7.5V, I_4 < 2.5 mA (V_{REG} = 6.0V)	1	5	1 1		5 3.5	V V
V_5	Probe 1 Open Circuit Threshold	At Pin 5	$V_{REG}-0.7$	$V_{REG}-0.5$	$V_{REG}-0.85$	$V_{REG}-0.6$	$V_{REG}-0.35$	V
V_5	Probe 1 Short Circuit Threshold		0.5	0.7	0.35	0.6	0.85	V
I_{14}	Pin 14 Input Leakage Current	Pin 14 = 4V	−2.0	2.0			2.0	nA
I_1	Pin 1 Input Leakage Current	Pin 1 = 300 mV	−5.0	5.0		1.5	5.0	nA
T_R	Repeat Period	C_R = 22 μF (Note 5)	12	28	9.1	17	36	s
	C_R Discharge Time	C_R = 22 μF				70	135	ms
C_M	Memory Capacitor Value						0.47	μF
C_1	Input Capacitor Value						0.47	μF

Sensitivity fo Electrostatic Discharge—

Pins 7, 10, 13, and 14 will withstand greater than 1500V when tested using 100 pF and 1500Ω in accordance with National Semiconductor standard ESD test procedures.

All other pins will withstand in excess of 2 kV.

Note 1: Test circuit for over voltage capability at pins 3, 6, 8.



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Note 2: Guaranteed and 100% production tested at 25°C. These limits are used to calculate outgoing quality levels.

Note 3: Limits guardbanded to include parametric variations. T_A = −40°C to +80°C and from V_{CC} = 7.5V to 18V. These limits are not used to calculate AOQL figures.

Note 4: Variations over temperature range are not production tested.

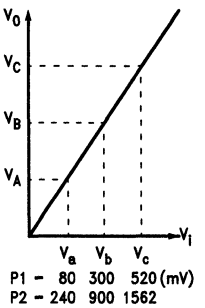
Note 5: Time for first repeat period, see *Figure 6*.

Note 6: Probe 1 amplifier tests are measured with pin 12 ramp voltage held between the T_3 and T_4 conditions (pin 12 ≈ 1.1V) having previously been held above 4.1V to simulate ramp action. See Figure 5.

Note 7: When measuring gain separate ground wire sensing is required at pin 2 to ensure sufficiently accurate results.

Linearity is defined as the difference between the predicted value of V_B (V_B*) and the measured value.

Note 8: Above T_A = 25°C derate with θ_{jA} = 70°C/W.



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For probe 1 and probe 2—Gain (G) = $\frac{V_C - V_A}{V_c - V_a}$

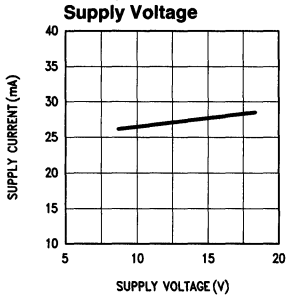
Input offset = $\left[\frac{V_C}{G} - V_c\right]$

Linearity = $\left[\frac{V_B^*}{V_B} - 1\right] \times 100\%$

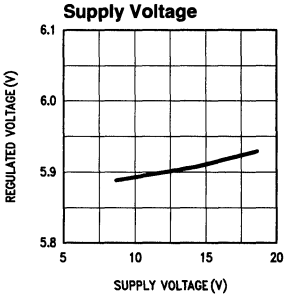
$V_B^* = V_A + G(V_b - V_a)$

Typical Performance Characteristics

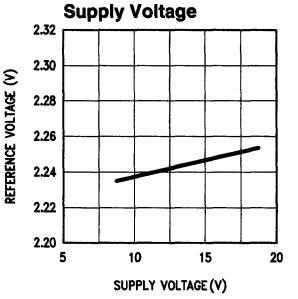
Supply Current vs Supply Voltage



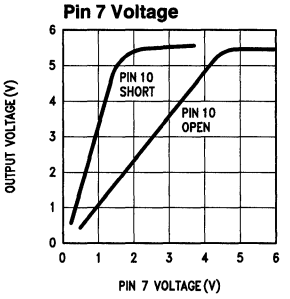
Regulated Voltage vs Supply Voltage



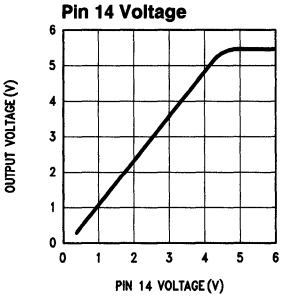
Probe Reference V vs Supply Voltage



Output Voltage vs Pin 7 Voltage



Output Voltage vs Pin 14 Voltage



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Pin Function Description

Pin 1 Input amplifier for thermo-resistive probe with 5 nA maximum leakage. Clamped to ground at the start of a probe 1 measurement.

Pin 2 Device ground — 0V.

Pin 3 This pin is connected to the emitter of an external PNP transistor to supply a 200 mA constant current to the thermo-resistive probe. An internal reference maintains this pin at $V_{SUPPLY} - 2V$.

Pin 4 Base connection for the external PNP transistor.

Pin 5 This pin is connected to the thermo-resistive probe for short and open circuit probe detection.

Pin 6 Supply pin, +7.5V to +18V, protected against +50V transients.

Pin 7 High Impedance input for second linear voltage probe with an input range from 1V to 5V. The gain may be set externally using pin 10.

Pin 8 Probe select and control input. If this pin is taken to a logic low level, probe 1 is selected and the timing cycle is initiated. The selection logic is subsequently latched low until the end of the measurement. If kept at a low level one shot or repeating probe 1 measurements will be made depending upon pin 9 conditions. A high input level selects probe 2 except during a probe 1 measurement period.

Pin 9 The repeat oscillator timing capacitor is connected from this pin to ground. A 2 μA current charges up the capacitor towards 4.3V when the probe 1 measurement cycle is restarted. If this pin is grounded the repeat oscillator is disabled and only one probe 1 measurement will be made when pin 8 goes low.

Pin 10 A resistor may be connected to ground to vary the gain of the probe 2 input amplifier. Nominal gain when open circuit is 1.2 and when shorted to ground 3.4. DC conditions may be adjusted by means of a resistor divider network to V_{REG} and ground.

Pin 11 Regulated voltage output. Requires to be connected to pin 15 to complete the supply regulator control loop.

Pin 12 The capacitor connected from this pin to ground sets the timing cycle for probe 1 measurements.

Pin 13 The resistor connected between this pin and ground defines the charging current at pin 12. Typically 12k, the value should be within the range 3k to 15k.

Pin 14 A low leakage capacitor, typical value 0.1 μF and not greater than 0.47 μF, should be connected from this pin to the regulated supply at pin 11 to act as a memory capacitor for the probe 1 measurement. The internal leakage at this pin is 2 nA max for a long memory retention time.

Pin 15 Feedback input for the internal supply regulator, normally connected to V_{REG} at pin 11. A resistor may be connected in series to adjust the regulated output voltage by an amount corresponding to the 1 mA current into pin 15.

Pin 16 Linear voltage output for probe 1 and probe 2 capable of driving up to ±10 mA. May be connected with a 600Ω meter to V_{REG}.

Application Notes

THERMO-RESISTIVE PROBES — OPERATION AND CONSTRUCTION

These probes work on the principle that when power is dissipated within the probe, the rise in probe temperature is dependent on the thermal resistance of the surrounding material and as air and other gases are much less efficient conductors of heat than liquids such as water and oil it is possible to obtain a measurement of the depth of immersion of such a probe in a liquid medium. This principle is illustrated in *Figure 1*.

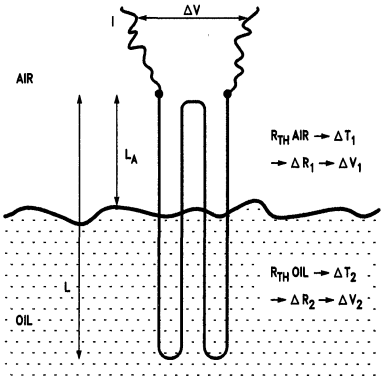

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FIGURE 1

During the measurement period a constant current drive I is applied to the probe and the voltage across the probe is sampled both at the start and just before the end of the measurement period to give ΔV. R_{TH} Air and R_{TH} Oil represent the different thermal resistances from probe to ambient in air or oil giving rise fo temperature changes ΔT_1 and ΔT_2 respectively. As a result of these temperature changes the probe resistance will change by ΔR_1 or ΔR_2 and give corresponding voltage changes ΔV_1 or ΔV_2 per unit length.

Hence

$$\Delta V = \frac{L_A}{L}\Delta V_1 + \frac{(L - L_A)}{L}\Delta V_2$$

and for $\Delta V_1 > \Delta V_2$, R_{TH} Air > R_{TH} Oil, ΔV will increase as the probe length in air increases. For best results the probe needs to have a high temperature coefficient and low thermal time constant. One way to achieve this is to make use of resistance wires held in a suitable support frame allowing free liquid access. Nickel cobalt iron alloy resistance wires are available with resistivity 50 μΩcm and 3300 ppm temperature coefficient which when made up into a probe with 4 × 2 cm 0.08 mm diameter strands between supports (10 cm total) can give the voltage vs time curve shown in *Figure 2* for 200 mA probe current. The effect of varying the probe current is shown in *Figure 3*. To avoid triggering the probe failure detection circuits the probe voltage must be between 0.7V and 5.3V (V_{REG} − 6V), hence for 200 mA the permissible probe resistance range is from 3.5Ω to 24Ω. The example given has a resistance at room temperature of 9Ω which leaves plenty of room for increase during measurements and changes in ambient temperature.

Various arrangements of probe wire are possible for any given wire gauge and probe current to suit the measurement range required, some examples are illustrated schematically in *Figure 4*. Naturally it is necessary to reduce the probe

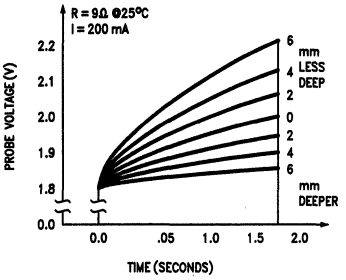

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FIGURE 2

current with very fine wires to avoid excessive heating and this current may be optimized to suit a particular type of wire. The temperature changes involved will give rise to noticeable length changes in the wire used and more sophisticated holders with tensioning devices may be devised to allow for this.

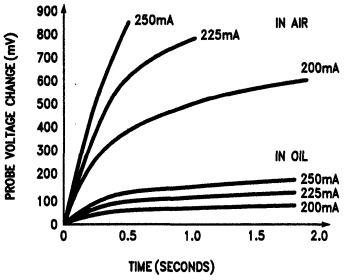

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FIGURE 3

Probes need not be limited to resistance wire types as any device with a positive temperature coefficient and sufficiently low thermal resistance to the encapsulation so as not to mask the change due to the different surrounding mediums, could be used. Positive temperature coefficient thermistors are a possibility and while their thermal time constant is likely to be longer than wire the measurement time may be increased by changing C_T to suit.

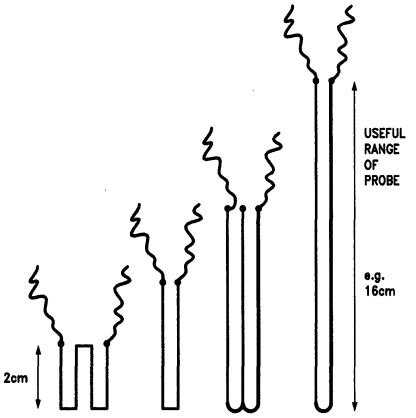

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FIGURE 4

Application Notes (Continued)

CIRCUIT OPERATION

1) Thermo-Resistive Probes

These probes require measurements to be made of their resistance before and after power has been dissipated in them. With a probe connected as probe 1 in the connection diagram the LM1042 will start a measurement when pin 8 is taken to a logic low level ($V_8 < 0.5V$) and the internal time-base ramp generator will start to generate the waveform shown in *Figure 5*. At 0.7V, T_1, the probe current drive is switched on supplying a constant 200 mA via the external PNP transistor and the probe failure circuit is enabled. At 1V pin 1 is unclamped and C_1 stores the probe voltage corresponding to this time, T_2. The ramp charge rate is now reduced as C_T charges toward 4V. As the 4.1V threshold is passed a current sink is enabled and C_T now discharges. Between 1.3V and 1.0V, T_3 and T_4, the amplified pin 1 voltage, representing the change in probe voltage since T_2 (and as the current is constant this is proportional to the resistance change) is gated onto the memory capacitor at pin 14. At 0.7V, T_5, the probe current is switched off and the measurement cycle is complete. In the event of a faulty probe being detected the memory capacitor is connected to the regulated supply during the gate period. The device leakage at pin 14 is a maximum of 2 nA to give a long memory retention time. The voltage present on pin 14 is amplifed by 1.2 to drive pin 16 with a low impedance, ±10 mA capability, between 0.5V and 4.7V. A new measurement can only be started by taking pin 8 to a low level again or by means of the repeat oscillator.

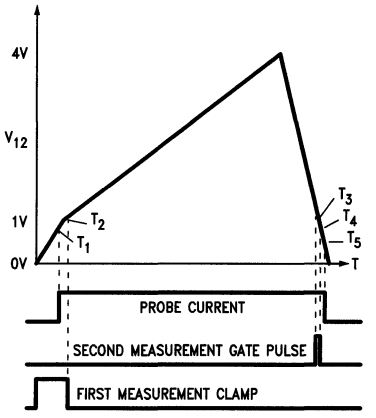

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FIGURE 5

2) Repetitive Measurement

With a capacitor connected between pin 9 and ground the repeat oscillator will run with a waveform as shown in *Figure 6* and a thermo-resistive probe measurement will be triggered each time pin 9 reaches a threshold of 4.3V, provided pin 8 is at a logic low level. The repeat oscillator runs independently of the pin 8 control logic.

As the repetition rate is increased localized heating of the probe and liquid being measured will be the main consideration in determining the minimum acceptable measurement intervals. Measurements will tend to become more dependent on the amount of fluid movement changing the rate of heat transfer away from the probe. The typical repeat time versus timing capacitor value is shown in *Figure 7*.

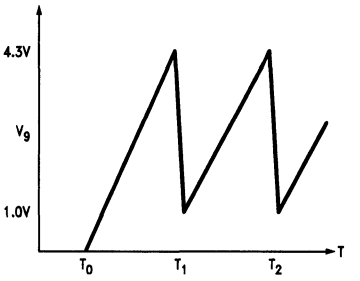

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FIGURE 6

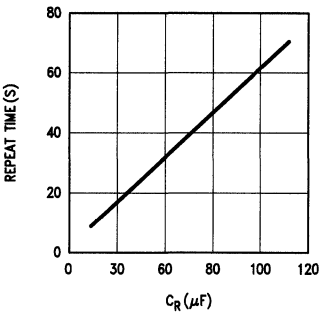

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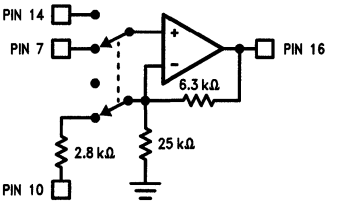
FIGURE 7

3) Second Probe Input

A high impedance input for an alternative sensor is available at pin 7. The voltage applied to this input is amplified and output at pin 16 when the input is selected with a high level on pin 8. The gain is defined by the feedback arrangement shown in *Figure 8* with adjustment possible at pin 10. With pin 10 open the gain is set at a nominal value of 1.2, and this may be increased by connecting a resistor between pin 10 and ground up to a maximum of 3.4 with pin 10 directly grounded. A variable resistor may be used to calibrate for the variations in sensitivity of the sensor used for probe 2.



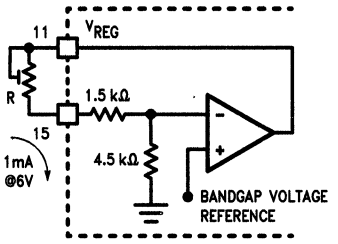
TL/H/8709–11

FIGURE 8

POWER SUPPLY REGULATOR

The arrangement of the feedback for the supply regulator is shown in *Figure 9*. The circuit acts to maintain pin 15 at a constant 6V and when directly connected to pin 11 the regulated output is held at 6V. If required a resistor R may be connected between pins 15 and 11 to increase the output voltage by an amount corresponding typically to 1 mA flowing in R. In this way a variable resistor may be used to trim out the production tolerance of the regulator by adjusting for $V_{REG} \geq 6.2V$.

Application Notes (Continued)

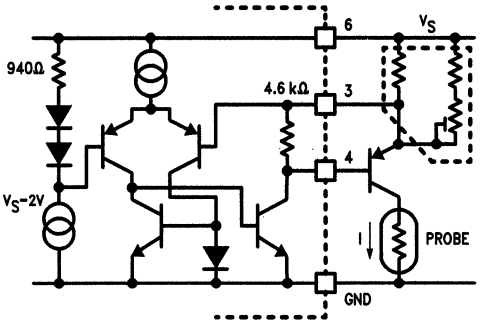


TL/H/8709–12

FIGURE 9

PROBE CURRENT REFERENCE CIRCUIT

The circuit defining the probe circuit is given in *Figure 10.* A reference voltage is obtained from a bandgap regulator derived current flowing in a diode resistor chain to set up a voltage 2 volts below the supply. This is applied to an amplifier driving an external PNP transistor to maintain pin 3 at 2V below supply. The emitter resistance from pin 3 to supply defines the current which, less the base current, flows in the probe. Because of the sensitivity of the measurement to probe current evident in *Figure 3* the current should be adjusted by means of a variable resistor to the desired value. This adjustment may also be used to take out probe tolerances.

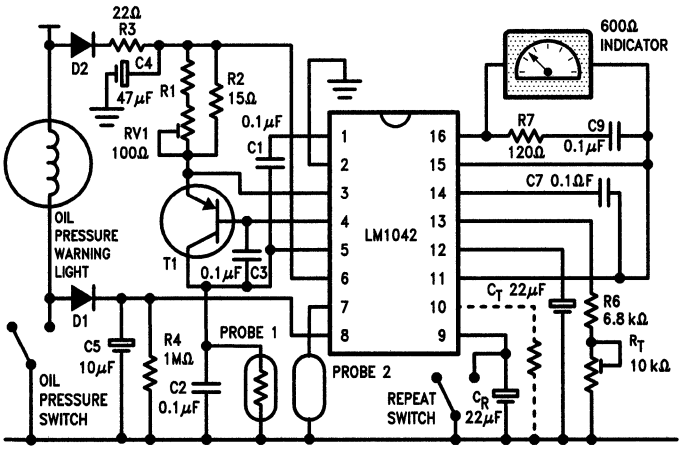


TL/H/8709–13

FIGURE 10

TYPICAL APPLICATIONS CIRCUIT

A typical automotive application circuit is shown in *Figure 11* where the probe selection signal is obtained from the oil pressure switch. At power up (ignition on) the oil pressure switch is closed and pin 8 is held low by R4 causing a probe 1 (oil level) measurement to be made. Once the engine has started the oil pressure switch opens and D1 pulls pin 8 high changing over to the second auxiliary probe input. The capacitor C_5 holds pin 8 high in the event of a stalled engine so that a second probe 1 measurement can not occur in disturbed oil. Non-automotive applications may drive pin 8 directly with a logic signal.



TL/H/8709–14

FIGURE 11. Typical Application Circuit

National Semiconductor

LM1815 Adaptive Sense Amplifier

General Description

The LM1815 is an adaptive sense amplifier and default gating circuit for motor control applications. The sense amplifier provides a one-shot pulse output whose leading edge coincides with the negative-going zero crossing of a ground referenced input signal such as from a variable reluctance magnetic pick-up coil.

In normal operation, this timing reference signal is processed (delayed) externally and returned to the LM1815. A logic input is then able to select either the timing reference or the processed signal for transmission to the output driver stage.

The adaptive sense amplifier operates with a positive-going threshold which is derived by peak detecting the incoming signal and dividing this down. Thus the input hysteresis varies with input signal amplitude. This enables the circuit to sense in situations where the high speed noise is greater than the low speed signal amplitude. Minimum input signal is 100 mVp-p.

Features

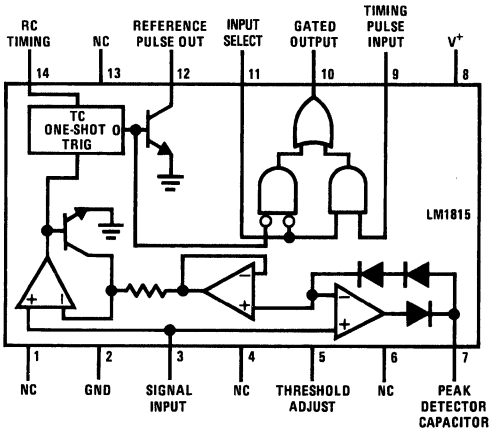
- Adaptive hysteresis
- Single supply operation
- Ground referenced input
- True zero crossing timing reference
- Operates from 2V to 12V supply voltage
- Handles inputs from 100 mV to over 120V with external resistor
- CMOS compatible logic

Applications

- Position sensing with notched wheels
- Zero crossing switch
- Motor speed control
- Tachometer
- Engine testing

Connection Diagram

Dual-In-Line Package



TL/H/7893–1

Top View

Order Number LM1815N
See NS Package Number N14A

Truth Table

Signal Input	Input Select	Timing Input	Gated Output
Pulses	L	X	Pulses
X	H	Pulses	Pulses

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	12V
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 2)	+125°C
Input Current	±30 mA
Lead Temperature (Soldering, 10 sec.)	260°C

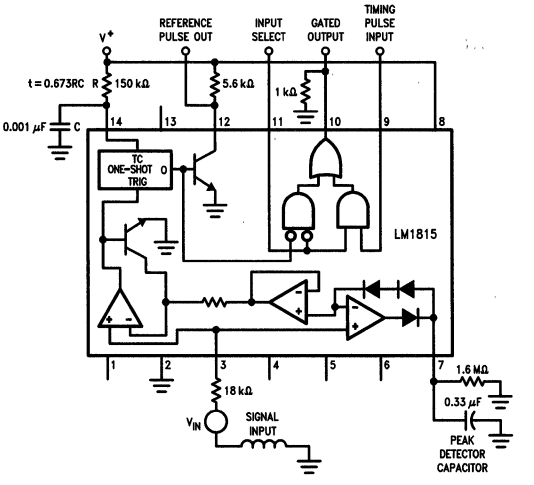
Electrical Characteristics (T_A = 25°C, V_{CC} = 10V, unless otherwise specified, see *Figure 1*)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage		2.5	10	12	V
Supply Current	f_{IN} = 500 Hz, Pin 9 = 2V, Pin 11 = 0.8V		3.6	6	mA
Reference Pulse Width	f_{IN} = 1 Hz to 2 kHz	70	100	130	μs
Input Bias Current	V_{IN} = 2V, (Pin 9 and Pin 11)			5	μA
Input Bias Current	V_{IN} = 0V dc, (Pin 3)		200		nA
Input Impedance	V_{IN} = 5 Vrms, (Note 3)	12	20	28	kΩ
Zero Crossing Threshold	V_{IN} = 100 mVp-p, (Pin 3)			25	mV
Logic Threshold	(Pin 9 and Pin 11)	0.8	1.1	2.0	V
V_{OUT} High	R_L = 1 kΩ, (Pin 10)	7.5	8.6		V
V_{OUT} Low	I_{SINK} = 0.1 mA, (Pin 10)		0.3	0.4	V
Input Arming Threshold	Pin 5 Open, $V_{IN} \leq$ 135 mVp-p	30	45	60	mV
	Pin 5 Open, $V_{IN} \geq$ 230 mVp-p	40	80	90	% of V_3 Pk
	Pin 5 to V^+	200			mV
	Pin 5 to Gnd	−25		25	mV
Output Leakage Pin 12	V_{12} = 11V		0.01	10	μA
Saturation Voltage P12	I_{12} = 2 mA		0.2	0.4	V

Note 1: For operation at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 2: Temporary excursions to 150°C can be tolerated.

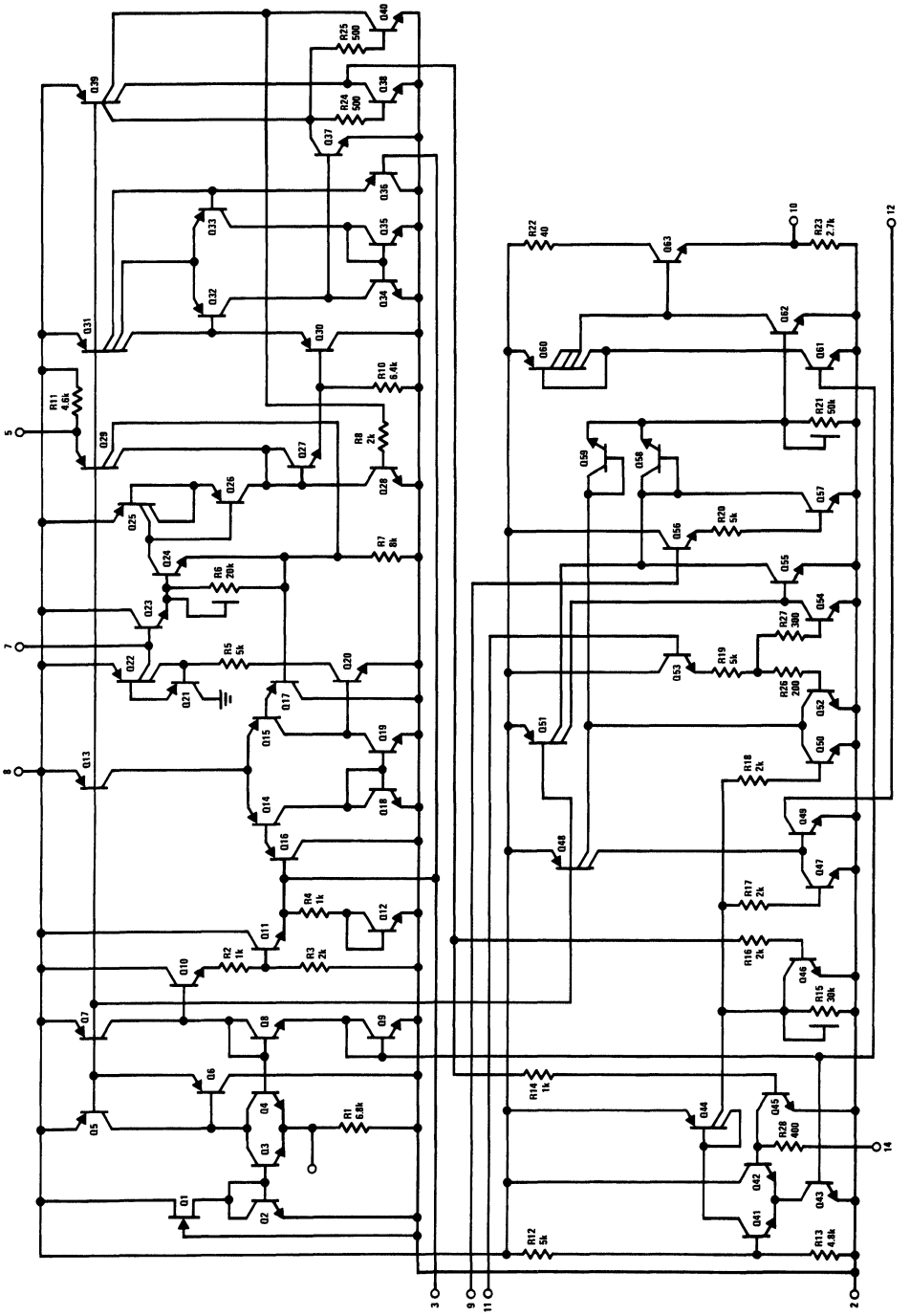
Note 3: Measured at input to external 18 kΩ resistor. IC contains 1 kΩ in series with a diode to attenuate the input signal.



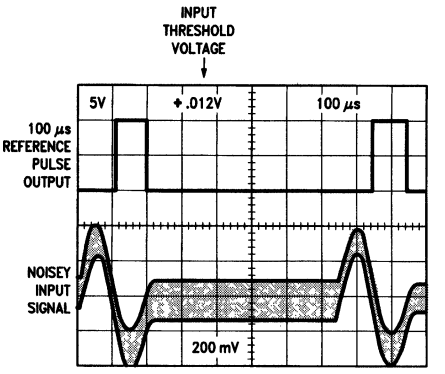
TL/H/7893–2

FIGURE 1. LM1815 Adaptive Sense Amplifier

Schematic Diagram



TL/H/7893–4



TL/H/7893–3

FIGURE 2. LM1815 Oscillograms

Application Hints

Input Clamp

The signal input at pin 3 is internally clamped. Current limit is provided by an external resistor which should be selected to allow a peak current of 3 mA in normal operation. Positive inputs are clamped by a 1 kΩ resistor and series diode, while an active clamp limits pin 3 to −350 mV for negative inputs (see R4, Q12, Q11 in internal schematic diagram).

Operation of Zero Crossing Detector

The LM1815 is designed to operate as a zero crossing detector, triggering an internal one shot on the negative-going edge of the input signal. Unlike other zero crossing detectors, the LM1815 cannot be triggered until the input signal has crossed an "arming" threshold on the positive-going portion of the waveform. The arming circuit is reset when the chip is triggered, and subsequent zero crossings are ignored until the arming threshold is exceeded again. This threshold varies depending on the connection at pin 5. Three different modes of operation are possible:

MODE 1, Pin 5 open. The adaptive mode is selected by leaving pin 5 open circuit. For input signals of less than 135 mVp-p, the input arming threshold is typically 45 mV. Under these conditions the input signal must first cross the 45 mV threshold in the positive direction to arm the zero crossing detector, and then cross zero in the negative direction to trigger it. If the signal is less than 30 mV peak (minimum rating in Electrical Characteristics), the one shot is guaranteed to not trigger.

Input signals of greater than 230 mVp-p cause the arming threshold to track at 80% of the peak input voltage. A peak detector (pin 7) stores a value relative to the positive input peaks to establish the arming threshold. Input signals must exceed this threshold in the positive direction to arm the zero crossing detector, which can then be triggered by a negative-going zero crossing. The peak detector tracks rapidly as the input signal amplitude increases, and decays by virtue of the resistor connected externally at pin 7 to track decreases in the input signal.

Note that since the input is clamped, the waveform observed at pin 3 is not identical to the waveform observed at the variable reluctance sensor. Similarly, the voltage stored at pin 7 is not identical to the peak voltage appearing at pin 3.

MODE 2, Pin 5 connected to V+. The input arming threshold is fixed at 200 mV minimum when pin 5 is connected to the positive supply. The chip has no output for signals of less than 200 mV peak, and triggers on the next negative-going zero crossing when the threshold is exceeded.

MODE 3, Pin 5 grounded. With pin 5 grounded, the input arming threshold is set to 0V (±25 mV maximum). Positive-going zero crossings arm the chip, and the next negative zero crossing triggers it.

The one shot timing is set by a resistor and capacitor connected to pin 14. The output pulse width is

$$\text{pulse width} = 0.673\ RC \qquad (1)$$

In some systems it is necessary to externally generate pulses, such as during stall conditions when the variable reluctance sensor has no output. External pulse inputs at pin 9 are gated through to pin 10 when Input Select (pin 11) is pulled high. Pin 12 is a direct output for the one shot and is unaffected by the status of pin 11.

Input/output pins 9, 11, 10 and 12 are all CMOS logic compatible. In addition, pins 9, 11 and 12 are TTL compatible. Pin 10 is not guaranteed to drive a TTL load.

Pins 1, 4, 6 and 13 have no internal connections and can be grounded.

National Semiconductor

LM1819 Air-Core Meter Driver

General Description

The LM1819 is a function generator/driver for air-core (moving-magnet) meter movements. A Norton amplifier and an NPN transistor are included on chip for signal conditioning as required. Driver outputs are self-centering and develop ±4.5V swing at 20 mA. Better than 2% linearity is guaranteed over a full 305-degree operating range.

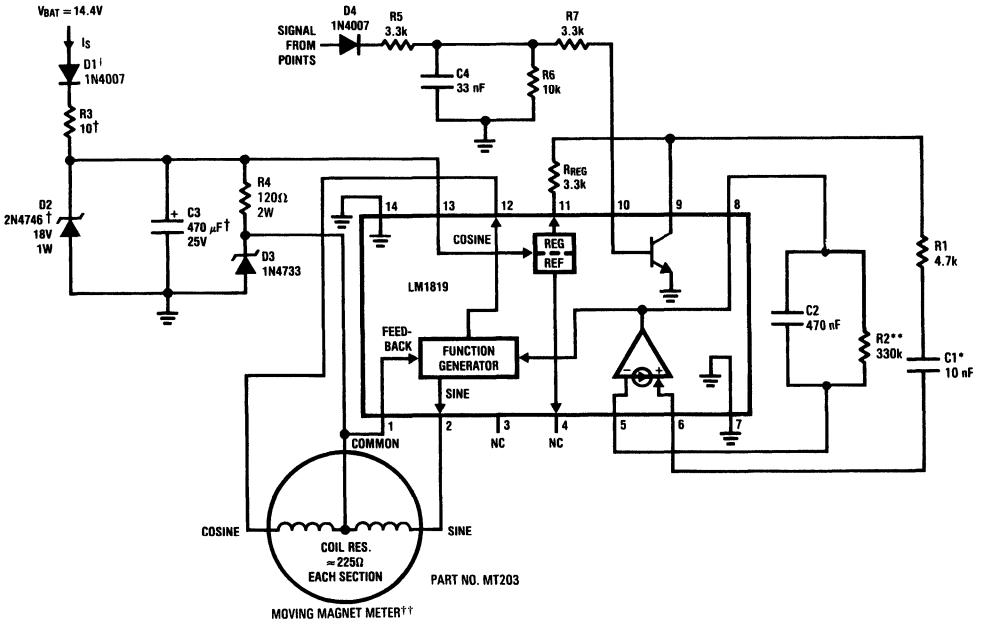
Features

- Self-centering 20 mA outputs
- 12V operation
- Norton amplifier
- Function generator

Applications

- Air-core meter driver
- Tachometers
- Ruggedized instruments

Typical Application



TL/H/5263–1

FIGURE 1. Automotive Tachometer Application. Circuit shown operates with 4 cylinder engine and deflects meter pointer (270°) at 6000 RPM.

Order Number LM1819N
See NS Package Number N14A

*TRW Type X463UW Polycarbonate Capacitor

**RN60D Low TC Resistor (±100 ppm)

†Components Required for Automotive Load Dump Protection

††Available from FARIA Co.
P O Box 983, Uncasville, CT 06382
Tel. 203-848-9271

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+ (pin 13)	20V
Power Dissipation (note 1)	1300 mW
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to −150°C
Lead Temp. (Soldering, 10 seconds)	260°C
BV_{CEO}	$20V_{MIN}$

Electrical Characteristics V_S = 13.1V T_A = 25°C unless otherwise specified

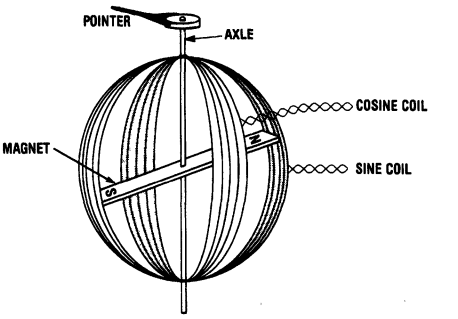
Symbol	Parameter	Pin(s)	Conditions	Min	Typ	Max	Units
I_S	Supply Current	13	Zero Input Frequency (See *Figure 1*)			65	mA
V_{REG}	Regulator Voltage	11	I_{REG} = 0 mA	8.1	8.5	8.9	V
	Regulator Output Resistance	11	I_{REG} = 0 mA to 3 mA		13.5		Ω
V_{REF}	Reference Voltage	4	I_{REF} = 0 mA	1.9	2.1	2.3	V
	Reference Output Resistance	4	I_{REF} = 0 μA to 50 μA		5.3		kΩ
	Norton Amplifier Mirror Gain	5, 6	$I_{BIAS} \cong$ 20 μA	0.9	1.0	1.1	
h_{FE}	NPN Transistor DC Gain	9, 10			125		
	Function Generator Feedback Bias Current	1	V_1 = 5.1V		1.0		mA
	Drive Voltage Extremes, Sine and Cosine	2, 12	I_{LOAD} = 20 mA	±4	±4.5		V
	Sine Output Voltage with Zero Input	2	$V_8 = V_{REF}$	−350	0	+350	mV
	Function Generator Linearity		FSD = 305°			±1.7	%FSD
k	Function Generator Gain		Meter Deflection/ΔV_8	50.75	53.75	56.75	°/V

Note 1: For operation above 25°C, the LM1819 must be derated based upon a 125°C maximum junction temperature and a thermal resistance of 76°C/W which applies for the device soldered in a printed circuit board and operating in a still-air ambient.

Application Hints

AIR-CORE METER MOVEMENTS

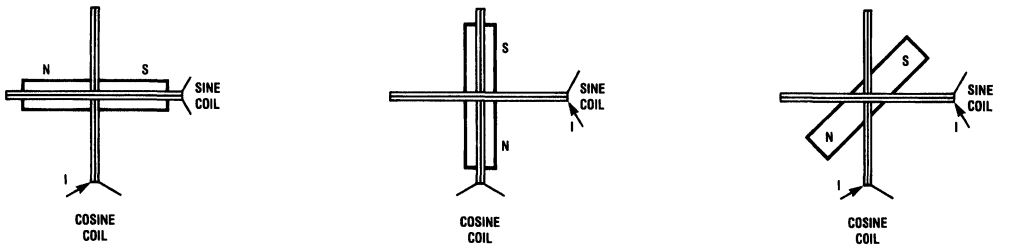
Air-core meters are often favored over other movements as a result of their mechanical ruggedness and their independence of calibration with age. A simplified diagram of an air-core meter is shown in *Figure 2*. There are three basic pieces: a magnet and pointer attached to a freely rotating axle, and two coils, each oriented at a right angle with respect to the other. The only moving part in this meter is the axle assembly. The magnet will tend to align itself with the vector sum of **H** fields of each coil, where **H** is the magnetic field strength vector. If, for instance, a current passes through the cosine coil (the reason for this nomenclature will become apparent later) as shown in *Figure 3(a)*, the magnet will align its magnetic axis with the coil's **H** field. Similarly, a current in the sine coil (*Figure 3(b)*) causes the magnet to align itself with the sine **H** field. If currents are applied simultaneously to both sine and cosine coils, the magnet will turn to the direction of the vector sum of the two **H** fields *(Figure 3(c))*. **H** is proportional to the voltage applied to a coil. Therefore, by varying both the polarity and magnitude of the coil voltages the axle assembly can be made to rotate a full 360°. The LM1819 is designed to drive the meter through a minimum of 305°.



TL/H/5263–2

FIGURE 2. Simplified Diagram of an Air Core Meter.

Application Hints (Continued)



TL/H/5263–3

(a) (b) (c)

FIGURE 3. Magnet and pointer position are controlled by the H field generated by the two drive coils.

In an air-core meter the axle assembly is supported by two nylon bushings. The torque exerted on the pointer is much greater than that found in a typical d'Arsonval movement. In contrast to a d'Arsonval movement, where calibration is a function of spring and magnet characteristics, air-core meter calibration is only affected by the mechanical alignment of the drive coils. Mechanical calibration, once set at manufacture, can not change.

Making pointer position a linear function of some input is a matter of properly ratioing the drive to each coil. The **H** field contributed by each coil is a function of the applied current, and the current is a function of the coil voltage. Our desired result is to have θ (pointer deflection, measured in degrees) proportional to an input voltage:

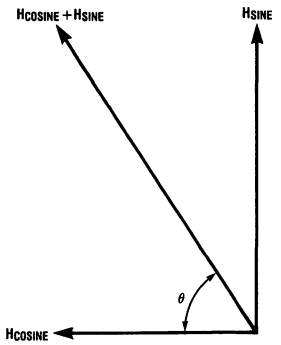
$$\theta = kV_{IN} \qquad [1]$$

where k is a constant of proportionality, with units of degrees/volt. The vector sum of each coils' **H** field must follow the deflection angle θ. We know that the axle assembly always points in the direction of the vector sum of $\mathbf{H}_{SINE}$ and $\mathbf{H}_{COSINE}$. This direction (see *Figure 4*) is found from the formula:

$$(\theta) = \arctan \{ | \mathbf{H}_{SINE} | / | \mathbf{H}_{COSINE} | \} \qquad [2]$$

Recalling some basic trigonometry,

$$(\theta) = \arctan(\sin(\theta) / \cos(\theta)) \qquad [3]$$



TL/H/5263–4

FIGURE 4. The vector sum of $\mathbf{H}_{COSINE}$ and $\mathbf{H}_{SINE}$ points in a direction θ measured in a clockwise direction from $\mathbf{H}_{COSINE}$.

Comparing [3] to [2] we see that if $\mathbf{H}_{SINE}$ varies as the sine of θ, and $\mathbf{H}_{COSINE}$ varies as the cosine of θ, we will generate a net **H** field whose direction is the same as θ. And since the axle assembly aligns itself with the net **H** field, the pointer will always point in the direction of θ.

THE LM1819

Included in the LM1819 is a function generator whose two outputs are designed to vary approximately as the sine and cosine of an input. A minimum drive of ±20 mA at ±4V is available at pins 2 (sine) and 12 (cosine). The common side of each coil is returned to a 5.1V zener diode reference and fed back to pin 1.

For the function generator, $k \cong 54°/V$ (in equation 1). The input (pin 8) is internally connected to the Norton amplifier's output. V_{IN} as considered in equation [1] is actually the difference of the voltages at pins 8 (Norton output/function generator input) and 4. Typically the reference voltage at pin 4 is 2.1V. Therefore,

$$\theta = k(V_8 - V_{REF}) = 54\ (V_8 - 2.1) \qquad [4]$$

As V_8 varies from 2.1V to 7.75V, the function generator will drive the meter through the chip's rated 305° range.

Air-core meters are mechanically zeroed during manufacture such that when only the cosine coil is driven, the pointer indicates zero degrees deflection. However, in some applications a slight trim or offset may be required. This is accomplished by sourcing or sinking a DC current of a few microamperes at pin 4.

A Norton amplifier is available for conditioning various input signals and driving the function generator. A Norton amplifier was chosen since it makes a simple frequency to voltage converter. While the non-inverting input (pin 6) bias is at one diode drop above ground, the inverting input (5) is at 2.1V, equal to the pin 4 reference. Mirror gain remains essentially flat to $I_{MIRROR} = 5$ mA. The Norton amplifier's output (8) is designed to source current into its load. To bypass the Norton amplifier simply ground the non-inverting input, tie the inverting input to the reference, and drive pin 8 (Norton output/function generator input) directly.

An NPN transistor is included on chip for buffering and squaring input signals. Its usefulness is exemplified in *Figures 1 & 6* where an ignition pulse is converted to a rectangular waveform by an RC network and the transistor. The emitter is internally connected to ground. It is important not to allow the base to drop below $-5V_{dc}$, as damage may occur. The 2.1V reference previously described is derived from an 8.5V regulator at pin 11. Pin 11 is used as a stable supply for collector loads, and currents of up to 5 mA are easily accommodated.

Application Hints (Continued)

TACHOMETER APPLICATION

A measure of the operating level of any motor or engine is the rotational velocity of its output shaft. In the case of an automotive engine the crankshaft speed is measured using the units "revolutions per minute" (RPM). It is possible to indirectly measure the speed of the crankshaft by using the signal present on the engine's ignition coil. The fundamental frequency of this signal is a function of engine speed and the number of cylinders and is calculated (for a four-stroke engine) from the formula:

$$f = n\omega/120 \quad \text{(Hz)} \quad (5)$$

where n = number of cylinders, and ω = rotational velocity of the crankshaft in RPM. From this formula the maximum frequency normally expected (for an 8 cylinder engine turning 4500RPM) is 300 Hz. In certain specialized ignition systems (motorcycles and some automobiles) where the coil waveform is operated at twice this frequency ($f = \omega/60$). These systems are identified by the fact that multiple coils are used in lieu of a single coil and distributor. Also, the coils have two outputs instead of one.

A typical automotive tachometer application is shown in *Figure 1*. The coil waveform is filtered, squared and limited by the RC network and NPN transistor. The frequency of the pulse train at pin 9 is converted to a proportional voltage by the Norton amplifier's charge pump configuration. The ignition circuit shown in *Figure 5* is typical of automotive systems. The switching element "S" is opened and closed in synchronism with engine rotation. When "S" is closed, energy is stored in Lp. When opened, the current in Lp diverts from "S" into C. The high voltage produced in Ls when "S" is opened is responsible for the arcing at the spark plug. The coil voltage (see *Figure 6*) can be used as an input to the LM1819 tachometer circuit. This waveform is essentially constant *duty cycle*. D4 rectifies this waveform thereby preventing negative voltages from reaching the chip. C4 and R5 form a low pass filter which attenuates the high frequency ringing, and R7 limits the input current to about 2.5mA. R6 acts as a base bleed to shut the transistor OFF when "S" is closed. The collector is pulled up to the internal regulator by R_{REG}. The output at pin 9 is a clean rectangular pulse.

Many ignition systems use magnetic, hall effect or optical sensors to trigger a solid state switching element at "S." These systems (see the LM1815) typically generate pulses of constant *width* and amplitude suitable for driving the charge pump directly.

The charge pump circuit in *Figure 7* can be operated in two modes: constant input pulse width (C1 acts as a coupling capacitor) and constant input duty cycle (C1 acts as a differentiating capacitor). The transfer functions for these two modes are quite diverse. However, deflection is always directly proportional to R2 and ripple is proportional to C2.

The following variables are used in the calculation of meter deflection:

symbol	description
n	number of cylinders
ω, ω_{IDLE}	engine speed at redline and idle, RPM
θ	pointer deflection at redline, degrees
δ	charge pump input pulse width, seconds
V_{IN}	peak to peak input voltages, volts
$\Delta\theta$	maximum desired ripple, degrees
k	function generator gain, degrees/volt
f, f_{IDLE}	input frequency at redline and idle, Hz

Where the NPN transistor and regulator are used to create a pulse $V_{IN} = 8.5V$. Acceptable ripple ranges from 3 to 10 degrees (a typical pointer is about 3 degrees wide) depending on meter damping and the input frequency.

The constant pulse width circuit is designed using the following equations:

(1) $$100\ \mu A < \frac{V_{IN}}{R1} < 3\ mA$$

(2) $$C_1 \geq \frac{10\delta}{R_1}$$

(3) $$R_2 = \frac{R_1\theta}{V_{IN}\delta k f} = \frac{120R_1\theta}{V_{IN}n\omega\delta k}$$

(4) $$C_2 = \frac{1}{R_2\Delta\theta f_{IDLE}} = \frac{1}{R_2\Delta\theta n\omega_{IDLE}}$$

The constant duty cycle equations are as follows:

$R_{REG} \geq 3\ k\Omega$

$R_1 \leq V_{IN} \times 10^4 - R_{REG}$

$C_1 \leq \delta/10(R_{REG} + R_1)$

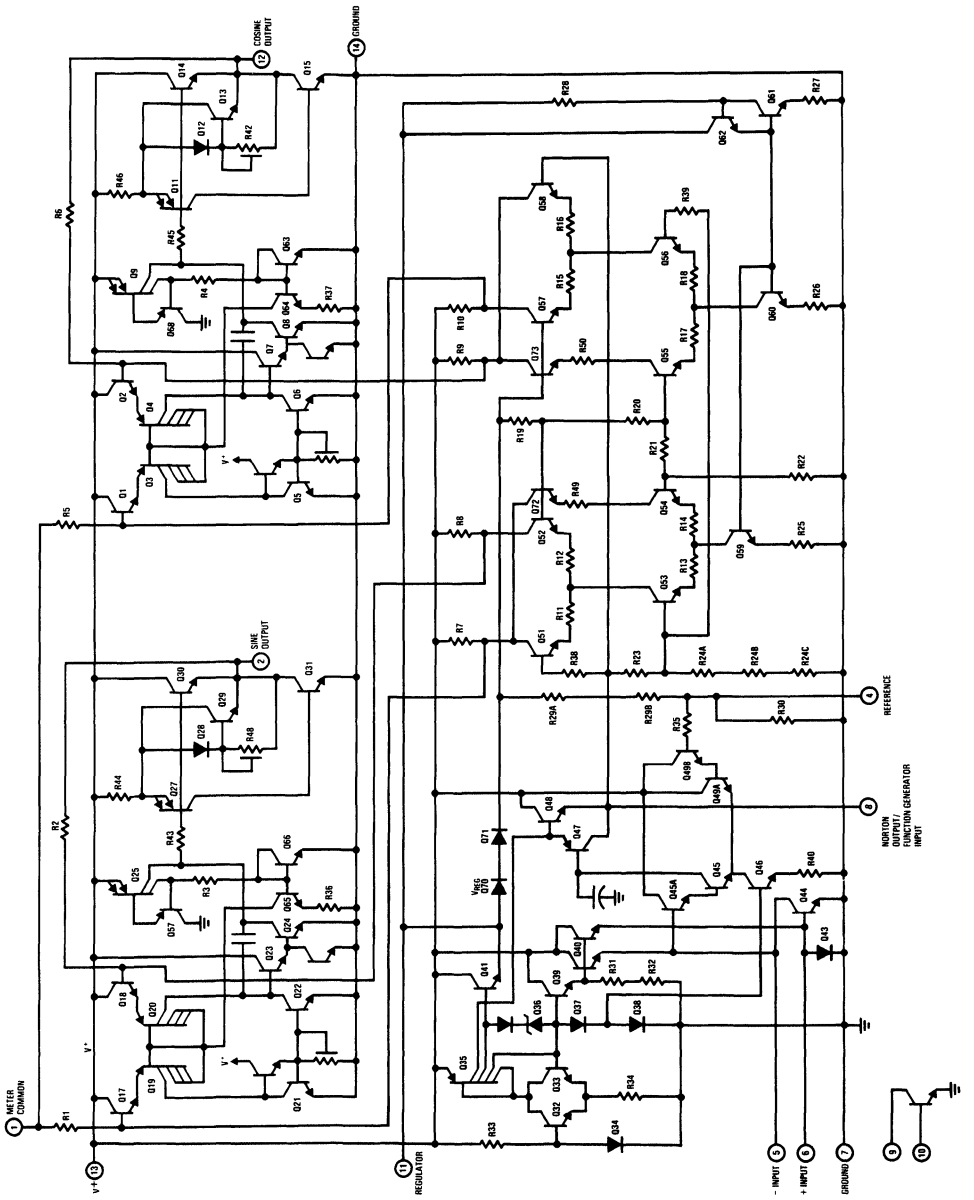
$R_Z = \theta/3.54n\omega C_1 = \theta/425fC_1$

$C_2 = 425C_1/\Delta\theta$

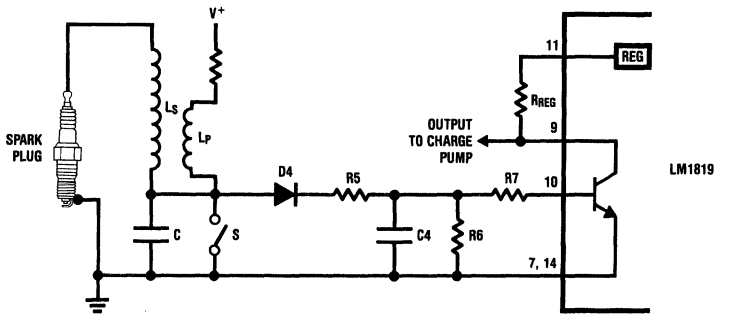
The values in *Figure 1* were calculated with n = 4, ω = 6000RPM, θ = 270 degrees, δ = 1 ms, V_{IN} is $V_{REG} - 0.7V$, and $\Delta\theta = 3$ degrees in the constant duty cycle mode. For distributorless ignitions these same equations will apply if $\omega/60$ is substituted for f.

Equivalent Schematic

TL/H/5263–12

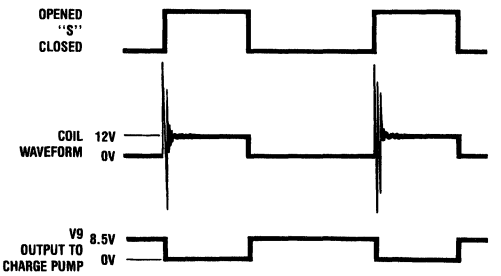


Typical Applications



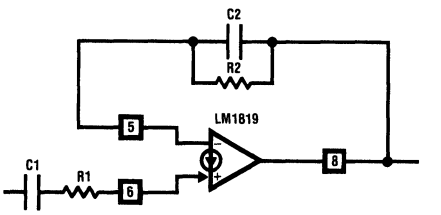
TL/H/5263–9

FIGURE 5. Typical Pulse-Squaring Circuit for Automotive Tachometers.



TL/H/5263–10

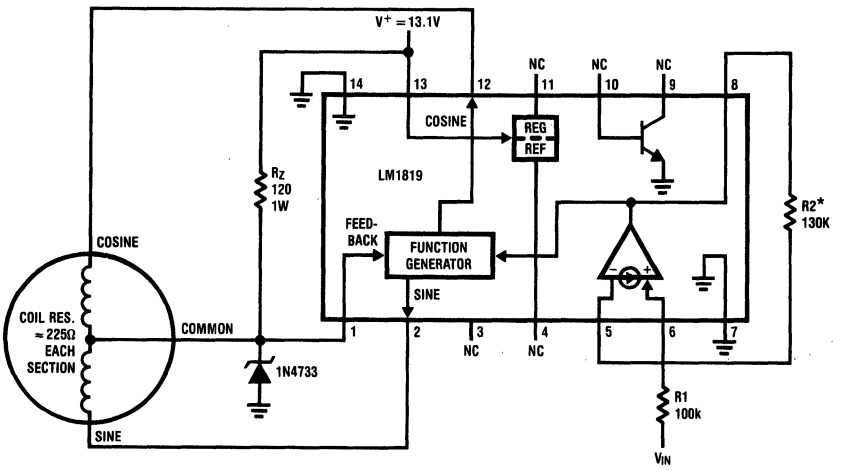
FIGURE 6. Waveforms Encountered in Automotive Tachometer Circuit.



TL/H/5263–11

FIGURE 7. Tachometer Charge Pump.

Voltage Driven Meter with Norton Amplifier Buffer



TL/H/5263–5

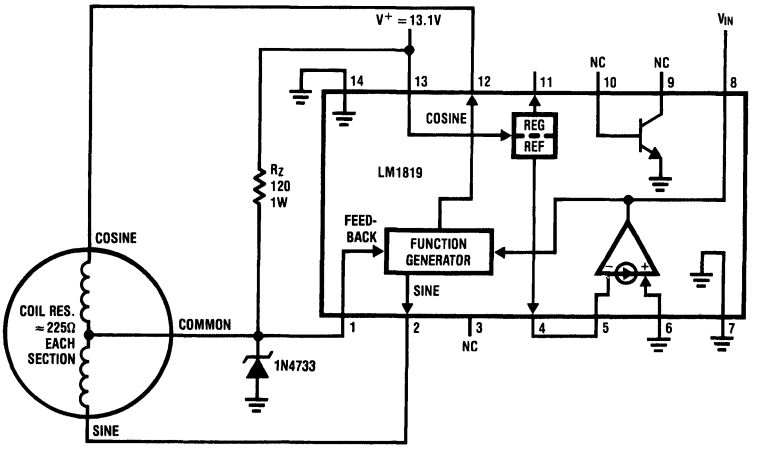
Deflection = 54 $(V_{IN} - .7)R_2/R_1$ (degrees)

0 to 305° deflection is obtained with .7 to 5V input.

*Full scale deflection is adjusted by trimming R_2.

Typical Applications (Continued)

Unbuffered Voltage Driven Meter



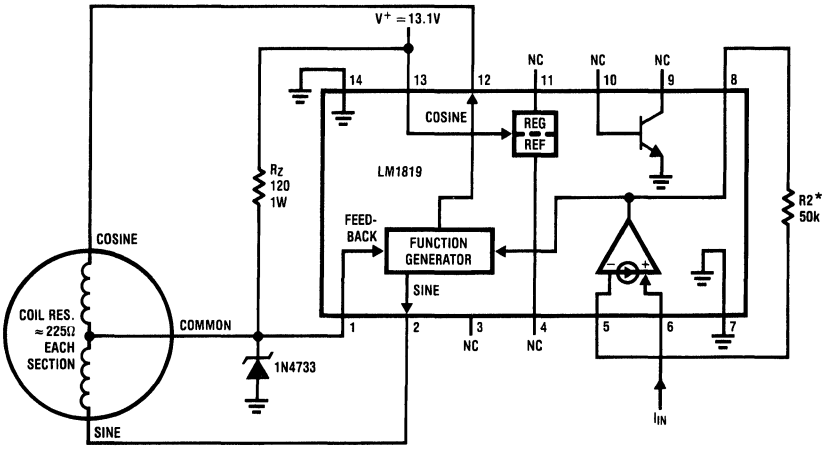
TL/H/5263–6

Deflection = $54(V_{IN} - 2.1)$ (degrees)

0 to 305° deflection is obtained for inputs of 2.1 to 7.75V.

Full scale deflection is adjusted by trimming the input voltage.

Current Driven Meter



TL/H/5263–7

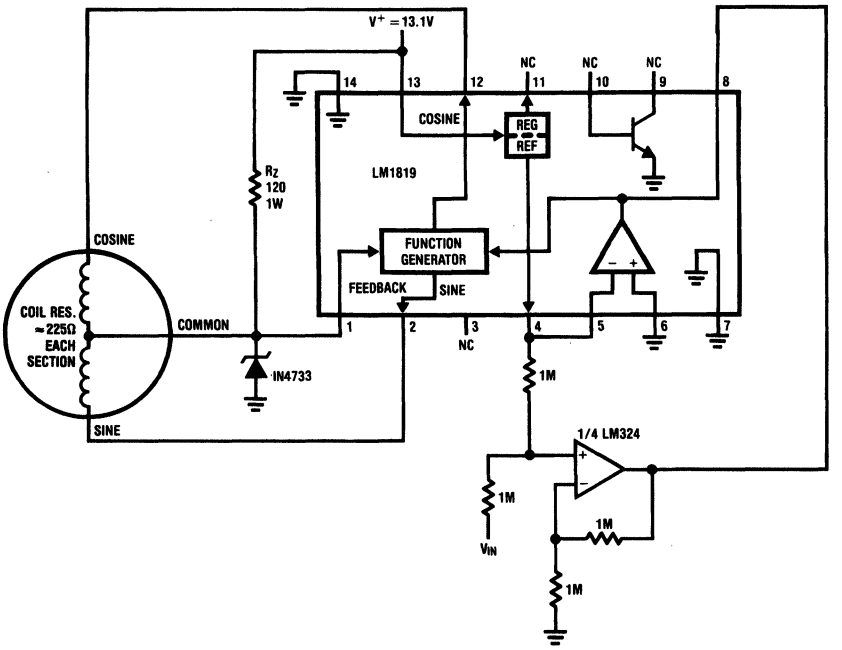
Deflection = $54R_2I_{IN}$ (degrees)

Inputs of 0 to 100 μA deflect the meter 0 to 270°.

*Full scale deflection is adjusted by trimming R_2.

Typical Applications (Continued)

Level Shifted Voltage Driven Meter



TL/H/5263–8

Deflection = $54V_{IN}$ (degrees)

Inputs of 0 to 5.65V deflect the meter through a range of 0 to 305°.

Full scale deflection is adjusted by trimming the input voltage.

National Semiconductor

LM1830 Fluid Detector

General Description

The LM1830 is a monolithic bipolar integrated circuit designed for use in fluid detection systems. The circuit is ideal for detecting the presence, absence, or level of water, or other polar liquids. An AC signal is passed through two probes within the fluid. A detector determines the presence or absence of the fluid by comparing the resistance of the fluid between the probes with the resistance internal to the integrated circuit. An AC signal is used to overcome plating problems incurred by using a DC source. A pin is available for connecting an external resistance in cases where the fluid impedance is of a different magnitude than that of the internal resistor. When the probe resistance increases above the preset value, the oscillator signal is coupled to the base of the open-collector output transistor. In a typical application, the output could be used to drive a LED, loud speaker or a low current relay.

Features

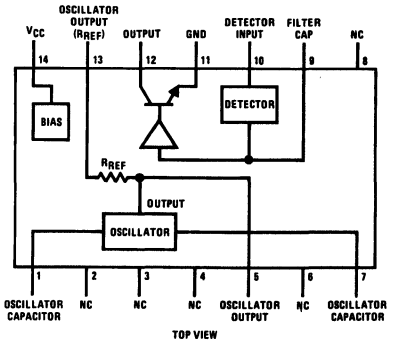
- Low external parts count
- Wide supply operating range
- One side of probe input can be grounded
- AC coupling to probe to prevent plating
- Internally regulated supply
- AC or DC output

Applications

- Beverage dispensers
- Water softeners
- Irrigation
- Sump pumps
- Aquaria
- Radiators
- Washing machines
- Reservoirs
- Boilers

Logic and Connection Diagram

Dual-In-Line Package



TL/H/5700–1

Order Number LM1830N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

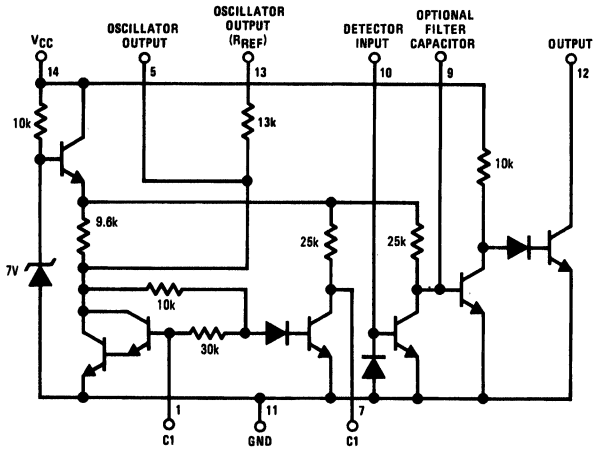
Supply Voltage	28V
Power Dissipation (Note 1)	1400 mW
Output Sink Current	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics ($V^+ = 16V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current			5.5	10	mA
Oscillator Output Voltage					
Low			1.1		V
High			4.2		V
Internal Reference Resistor		8	13	25	kΩ
Detector Threshold Voltage			680		mV
Detector Threshold Resistance		5	10	15	kΩ
Output Saturation Voltage	$I_O = 10$ mA		0.5	2.0	V
Output Leakage	$V_{PIN\ 12} = 16V$			10	μA
Oscillator Frequency	C1 = 0.00 1μF	4	7	12	kHz

Note 1: The maximum junction temperature rating of the LM1830N is 150°C. For operation at elevated temperatures, devices in the dual-in-line plastic package must be derated based on a thermal resistance of 89°C/W.

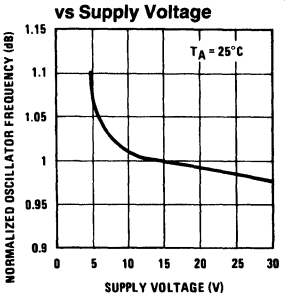
Schematic Diagram



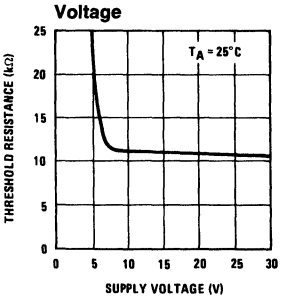
TL/H/5700–2

Typical Performance Characteristics

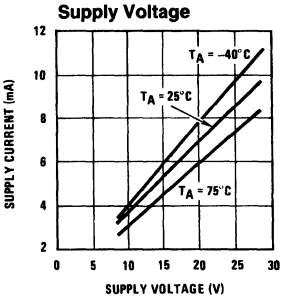
Normalized Oscillator Frequency vs Supply Voltage



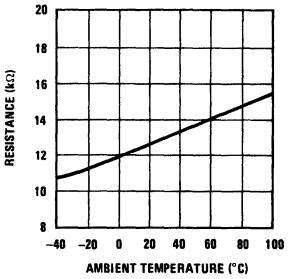
Threshold Resistance vs Supply Voltage



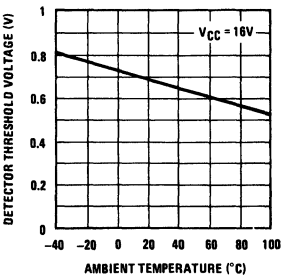
Power Supply Current vs Supply Voltage



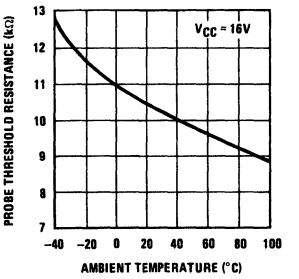
Reference Resistor vs Ambient Temperature



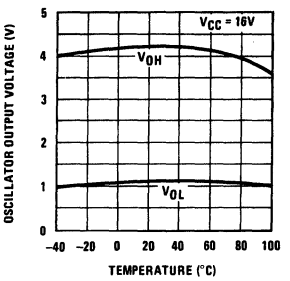
Detector Threshold Voltage vs Temperature



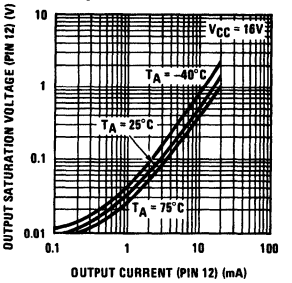
Probe Threshold Resistance vs Temperature



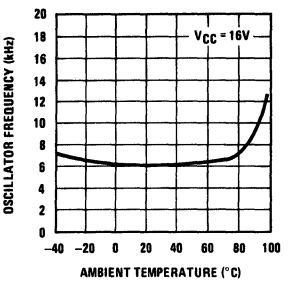
Oscillator V_{OH} and V_{OL} vs Ambient Temperature



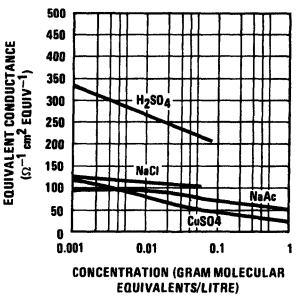
Output Saturation Voltage vs Output Current



Oscillator Frequency vs Ambient Temperature



Equivalent Resistance vs Concentration of Several Solutions



TL/H/5700–3

Application Hints

The LM1830 requires only an external capacitor to complete the oscillator circuit. The frequency of oscillation is inversely proportional to the external capacitor value. Using 0.001μF capacitor, the output frequency is approximately 6 kHz. The output from the oscillator is available at pin 5. In normal applications, the output is taken from pin 13 so that the internal 13k resistor can be used to compare with the probe resistance. Pin 13 is coupled to the probe by a blocking capacitor so that there is no net dc on the probe.

Since the output amplitude from the oscillator is approximately 4 V_{BE}, the detector (which is an emitter base junction) will be turned "ON" when the probe resistance to ground is equal to the internal 13 kΩ resistor. An internal diode across the detector emitter base junction provides symmetrical limiting of the detector input signal so that the probe is excited with ±2 V_{BE} from a 13 kΩ source. In cases where the 13 kΩ resistor is not compatible with the probe resistance range, an external resistor may be added by coupling the probe to pin 5 through the external resistor as shown in *Figure 2*. The collector of the detecting transistor is brought out to pin 9 enabling a filter capacitor to be connected so that the output will switch "ON" or "OFF" depending on the probe resistance. If this capacitor is omitted, the output will be switched at approximately 50% duty cycle when the probe resistance exceeds the reference resistance. This can be useful when an audio output is required and the output transistor can be used to directly drive a loud speaker. In addition, LED indicators do not require dc excitation. Therefore, the cost of a capacitor for filtering can be saved.

In the case of inductive loads or incandescent lamp loads, it is recommended that a filter capacitor be employed.

In a typical application where the device is employed for sensing low water level in a tank, a simple steel probe may be inserted in the top of the tank with the tank grounded. Then when the water level drops below the tip of the probe, the resistance will rise between the probe and the tank and the alarm will be operated. This is illustrated in *Figure 3*. In situations where a non-conductive container is used, the probe may be designed in a number of ways. In some cases a simple phono plug can be employed. Other probe designs include conductive parallel strips on printed circuit boards.

It is possible to calculate the resistance of any aqueous solution of an electrolyte for different concentrations, provided the dimensions of the electrodes and their spacing is known.

The resistance of a simple parallel plate probe is given by:

$$R = \frac{1000}{c.p} \bullet \frac{d}{A}\ \Omega$$

where A = area of plates (cm^2)
d = separation of plates (cm)
c = concentration (gm. mol. equivalent/litre)
p = equivalent conductance
(Ω^{-1} cm^2 equiv. $^{-1}$)

(An equivalent is the number of moles of a substance that gives one mole of positive charge and one mole of negative charge. For example, one mole of NaCl gives $Na^+ + Cl^-$ so the equivalent is 1. One mole of $CaCl_2$ gives $Ca^{++} + 2Cl^-$ so the equivalent is 1/2.)

Usually the probe dimensions are not measured physically, but the ratio d/A is determined by measuring the resistance of a cell of known concentration c and equivalent conductance of 1. A graph of common solutions and their equivalent conductances is shown for reference. The data was derived from D.A. MacInnes, "The Principles of Electrochemistry," Reinhold Publishing Corp., New York., 1939.

In automotive and other applications where the power source is known to contain significant transient voltages, the internal regulator on the LM1830 allows protection to be provided by the simple means of using a series resistor in the power supply line as illustrated in *Figure 4*. If the output load is required to be returned directly to the power supply because of the high current required, it will be necessary to provide protection for the output transistor if the voltages are expected to exceed the data sheet limits.

Although the LM1830 is designed primarily for use in sensing conductive fluids, it can be used with any variable resistance device, such as light dependent resistor or thermistor or resistive position transducer.

The following table lists some common fluids which may and may not be detected by resistive probe techniques.

Conductive Fluids	Non-Conductive Fluids
City water	Pure water
Sea water	Gasoline
Copper sulphate solution	Oil
Weak acid	Brake fluid
Weak base	Alcohol
Household ammonia	Ethylene glycol
Water and glycol mixture	Paraffin
Wet soil	Dry soil
Coffee	Whiskey

Typical Applications V_{CC} = 16V

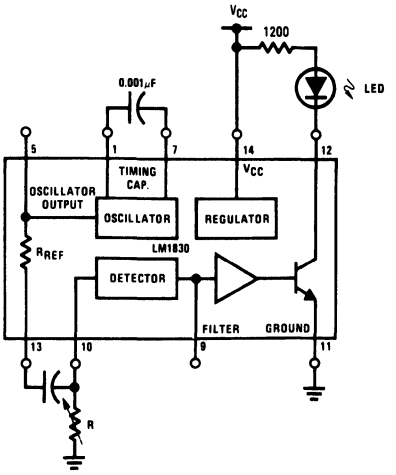


FIGURE 1. Test Circuit

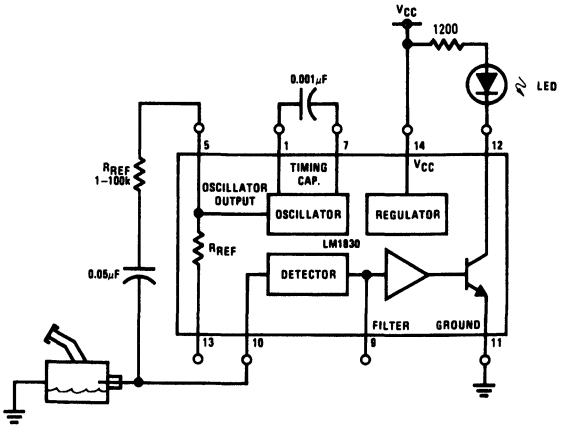


FIGURE 2. Application Using External Reference Resistor

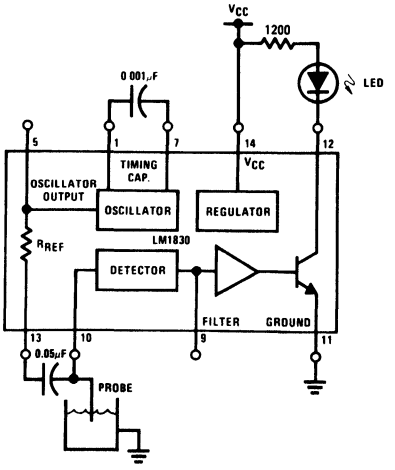
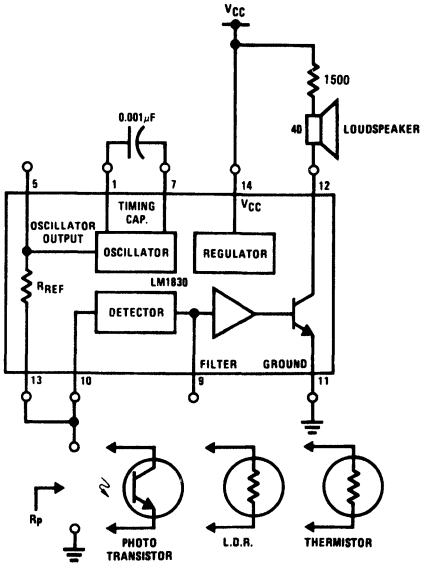


FIGURE 3. Basic Low Level Warning Device with LED Indication



TL/H/5700–4

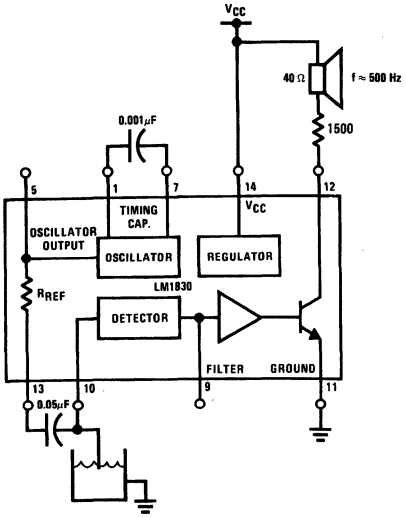
Output is activated when R_P is approximately greater than ⅓ R_{REF}

FIGURE 4. Direct Coupled Applications

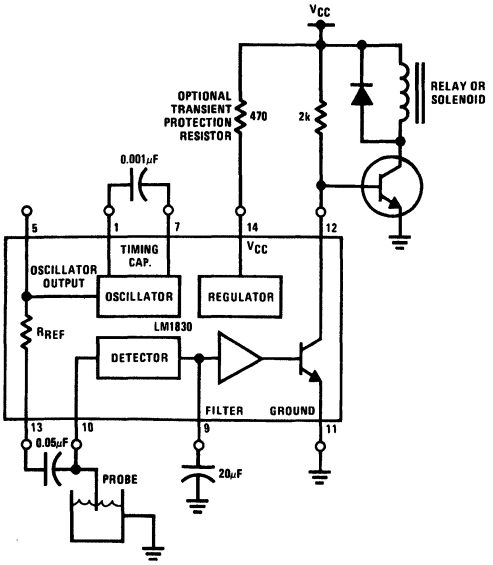
7

Typical Applications V_{CC} = 16V (Continued)

Low Level Warning with Audio Output



High Level Warning Device



TL/H/5700–5

The Output is suitable for driving a sump pump or opening a drain valve, etc.

National Semiconductor

LM1921 1 Amp Industrial Switch

General Description

The LM1921 Relay Driver incorporates an integrated power PNP transistor as the main driving element. The advantages of this over previous integrated circuits employing NPN power elements are several. Greater output voltages are available off the same supply for driving grounded loads; typically 4.5 volts for a 500 mA load from a 5.0 volt supply. The output can swing below ground potential up to 57 volts negative with respect to the positive power supply. This can be used to facilitate rapid decay times in inductive loads. Also, the IC is immune to negative supply voltages or transients. The inherent Safe Operating Area of the lateral PNP allows use of the IC as a bulb driver or for capacitive loads.

Familiar integrated circuit features such as short circuit protection and thermal shutdown are also provided. The input voltage threshold levels are designed to be TTL, CMOS, and LSTTL compatible over the entire operating temperature range. If several drivers are used in a system, their inputs and/or outputs may be combined and wired together if their supply voltages are also common.

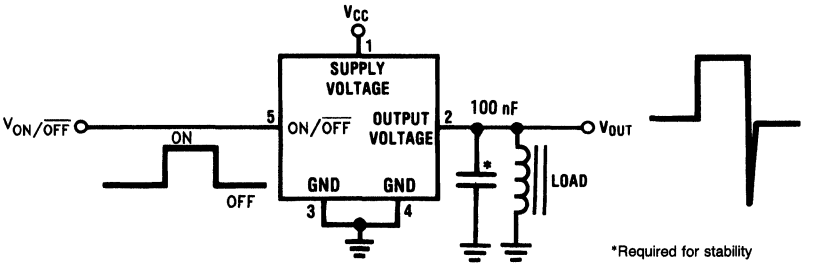
Features

- 1 Amp output drive
- Load connected to ground
- Low input-output voltage differential
- +60 volt positive transient protection
- −50 volt negative transient protection
- Automotive reverse battery protection
- Short circuit proof
- Internal thermal overload protection
- Unclamped output for fast decay times
- TTL, LSTTL, CMOS compatible input
- Plastic TO-220 package
- 100% electrical burn-in

Applications

- Relays
- Solenoids
- Valves
- Motors
- Lamps
- Heaters

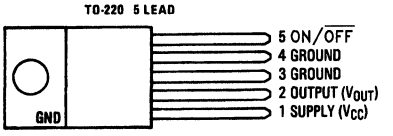
Typical Application Circuit



TL/H/5271–1

FIGURE 1. Test and Application Circuit

Connection Diagram



TL/H/5271–2

Front View
Order Number LM1921T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
Operating Range	4.75V to 26V
Overvoltage Protection (100 ms)	−50V to +60V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics (V_{CC} = 12V, I_{OUT} = 500 mA, T_J = 25°C, $V_{ON/\overline{OFF}}$ = 2V, unless otherwise specified.)

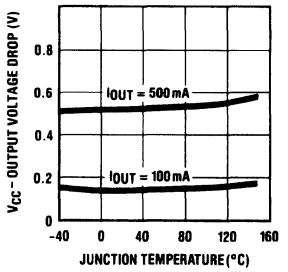
Parameter	Conditions	Typ	Tested Limits (Note 1)		Design Limits (Note 2)		Units
			Min	Max	Min	Max	
Supply Voltage							
Operational			4.75	26	6	24	V
Survival			−15	60			V_{DC}
Transient	100 ms, 1% Duty Cycle		−50				V
Supply Current							
$V_{ON/\overline{OFF}}$ = 0		0.6				1.5	mA
$V_{ON/\overline{OFF}}$ = 2V	I_{OUT} = 0 mA	6		10			mA
	I_{OUT} = 250 mA	285		350			mA
	I_{OUT} = 500 mA	575		700			mA
	I_{OUT} = 1A	1.3		1.5			A
Input to Output Voltage Drop	I_{OUT} = 500 mA	0.5		0.8			V
	I_{OUT} = 1A	1.0					V
Short Circuit Current		1.4	1.0	2.0			A
	6V ≤ V_{CC} ≤ 24V				.75	3.0	A
Output Leakage Current	$V_{ON/\overline{OFF}}$ = 0	0.1				50	μA
ON/$\overline{OFF}$ Voltage		1.3	0.8	2.0			V
Threshhold	6V ≤ V_{CC} ≤ 24V				0.8	2.0	V
ON/$\overline{OFF}$ Current		15	10	30			μA
Overvoltage Shutdown		32			26	36	V
Thermal Resistance							
junction-case	θjc	3					°C/W
case-ambient	θca	50					°C/W
Inductive Clamp							
Output Voltage	$V_{ON/\overline{OFF}}$ = 0, I_{OUT} = 100 mA	−60			−120	−45	V
Fault Conditions							
Output Current							
ON/$\overline{OFF}$ Floating	Pin 5 Open	0.1				50	μA
Ground Floating	Pin 3 & Pin 4 Open	0.1				50	μA
Reverse Voltage	V_{CC} = −15V	−0.01			−1		mA
Reverse Transient	V_{CC} = −50V	−100					mA
Overvoltage	V_{CC} = +60V	0.01				1	mA
Supply Current	Pin 1 & Pin 2 Short, No load	10				40	mA

Note 1: Guaranteed and 100% production tested.

Note 2: Guaranteed, not necessarily 100% production tested. Not used to calculate outgoing AQL. Limits are for the temperature range of −40°C ≤ T_j ≤ 150°C.

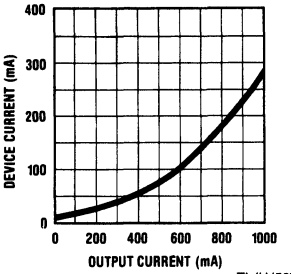
Typical Performance Characteristics

Output Voltage Drop



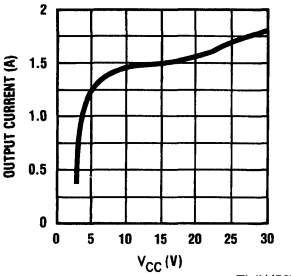
TL/H/5271–3

Device Operating Current



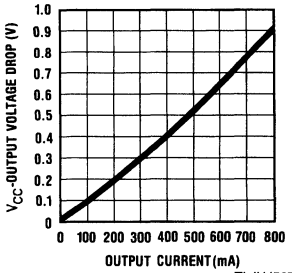
TL/H/5271–4

Peak Output Current (V_{OUT})



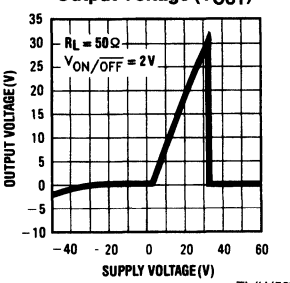
TL/H/5271–5

Output Voltage Drop



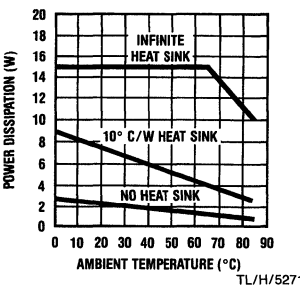
TL/H/5271–6

Output Voltage (V_{OUT})



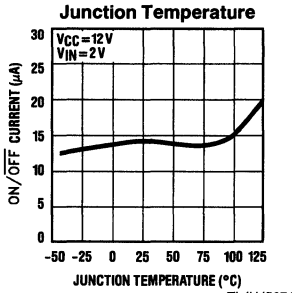
TL/H/5271–7

Maximum Power Dissipation (TO-220)



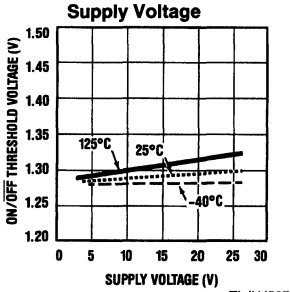
TL/H/5271–8

ON/$\overline{OFF}$ Current vs. Junction Temperature



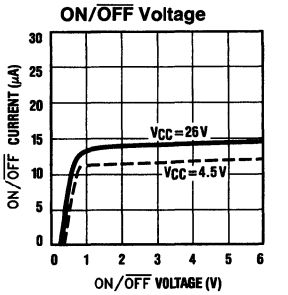
TL/H/5271–13

Threshold Voltage vs. Supply Voltage



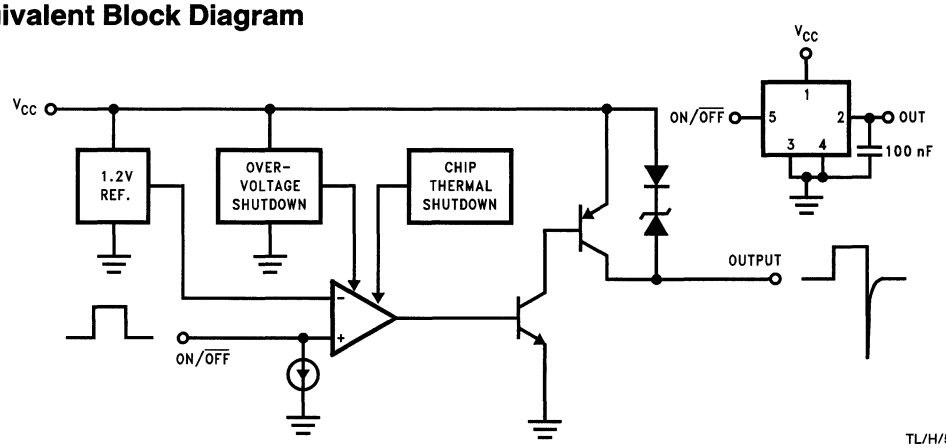
TL/H/5271–14

ON/$\overline{OFF}$ Current vs. ON/$\overline{OFF}$ Voltage



TL/H/5271–15

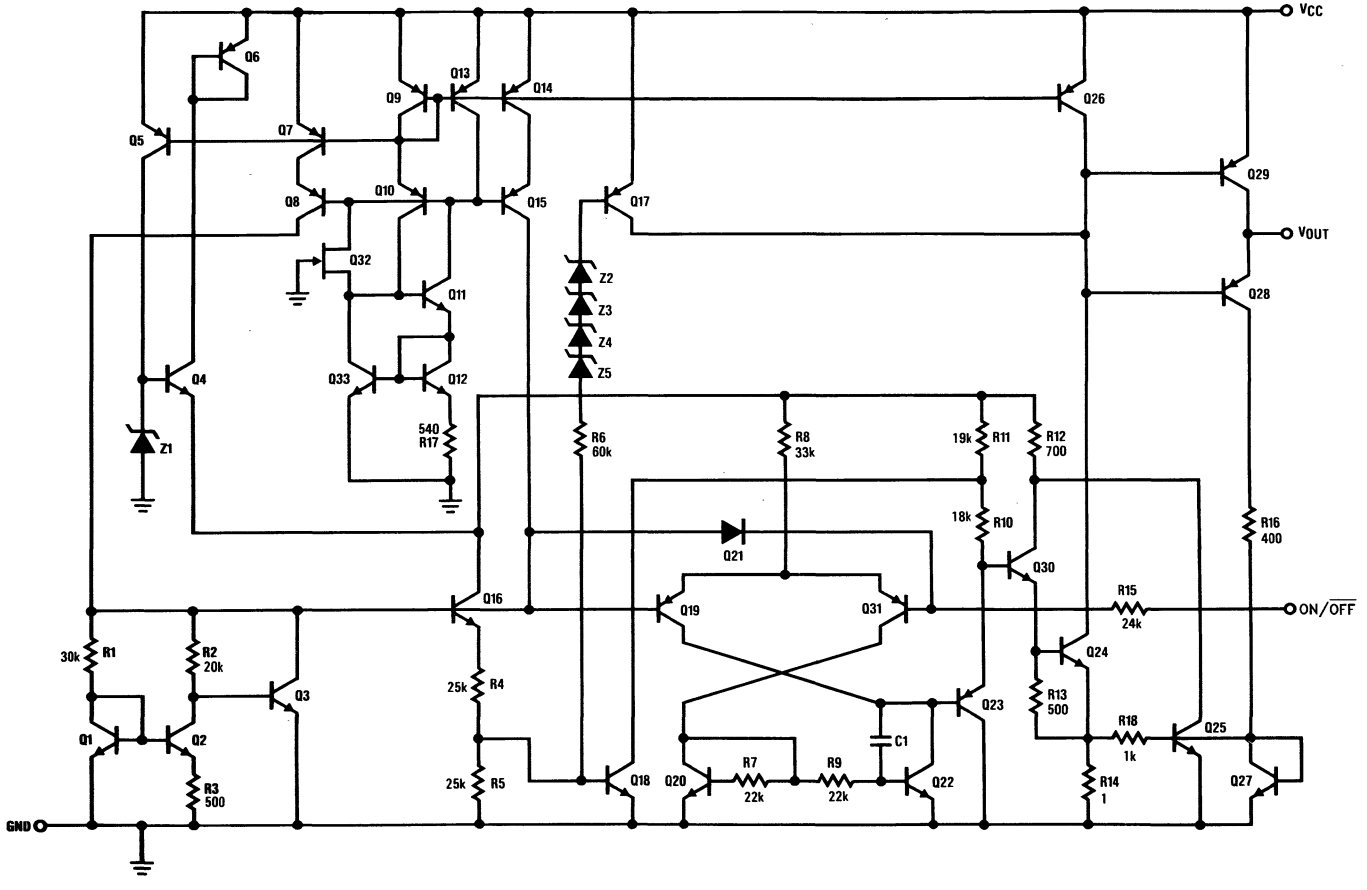
Equivalent Block Diagram



TL/H/5271–12

FIGURE 1

Circuit Schematic



TL/H/5271–9

Application Hints

HIGH CURRENT OUTPUT

The 1 Amp output is fault protected against overvoltage. If the supply voltage rises above approximately 30 volts, the output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. The 1921 will survive transients and DC voltages up to 60 volts on the supply. The output remains off during this time, independent of the state of the input logic voltage. This protects the load. The high current output is also protected against short circuits to either ground or supply voltage. Standard thermal shutdown circuits are employed to protect the 1921 from over heating.

FLYBACK RESPONSE

Since the 1921 is designed to drive inductive as well as any other type of load, inductive kickback can be expected whenever the output changes state from on to off (see waveforms on *Figure 1*). The driver output was left unclamped since it is often desirable in many systems to achieve a very rapid decay in the load current. In applications where this is not true, such as in *Figure 2*, a simple external diode clamp will suffice. In this application, the integrated current in the inductive load is controlled by varying the duty cycle of the input to the driver IC. This technique achieves response characteristics that are desirable for certain automotive transmission solenoids, for example.

For applications requiring a rapid controlled decay in the solenoid current, such as fuel injector drivers, an external zener and diode can be used as in *Figure 3*. The voltage rating of the zener should be such that it breaks down before the output of the LM1921. The minimum output breakdown voltage of the IC output is rated at −57 volts with respect to the supply voltage. Thus, on a 12 volt supply, the combined zener and diode breakdown should be less than 45 volts.

The LM1921 can be used alone as a simple relay or solenoid driver where a rapid decay of the load current is desired, but the exact rate of decay is not critical to the system. If the output is unclamped as in *Figure 1*, and the load is inductive enough, the negative flyback transient will cause the output of the IC to breakdown and behave similarly to a zener clamp. Relying upon the IC breakdown is practical, and will not damage or degrade the IC in any way. There are two considerations that must be accounted for when the driver is operated in this mode. The IC breakdown voltage is process and lot dependent. Clamp voltages ranging from −60 to −120 volts (with respect to the supply voltage) will be encountered over time on different devices. This is not at all critical in most applications. An important consideration, however, is the additional heat dissipated in the IC as a result. This must be added to normal device dissipation when considering junction temperatures and heat sinking requirements. Worst case for the additional dissipation can be approximated as:

$$\text{Additional } P_D = I^2 \times L \times f \text{ (Watts)}$$

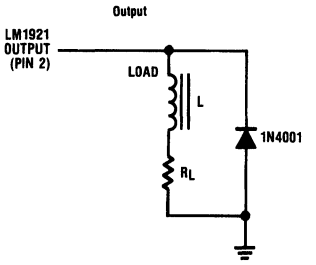
where: I = peak solenoid current (Amps)

L = solenoid inductance (Henries)

f = maximum frequency input signal (Hz)

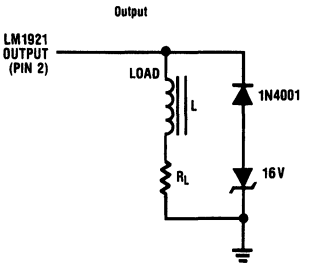
For solenoids where the inductance is less than ten millihenries, the additional power dissipation can be ignored.

Overshoot, undershoot, and ringing can occur on certain loads. The simple solution is to lower the Q of the load by the addition of a resistor in parallel or series with the load. A value that draws one tenth of the current or DC voltage of the load is usually sufficient.



TL/H/5271–10

FIGURE 2. Diode Clamp



TL/H/5271–11

FIGURE 3

Zener clamp for rapid controlled current decay

National Semiconductor

LM1946 Over/Under Current Limit Diagnostic Circuit

General Description

The LM1946 provides the industrial or automotive system designer with over or under current limit detection superior to that of ordinary transistor or comparator-based circuits.

Each of the five independent comparators can be used to monitor a separate load as either an over current or under current limit detector. Two comparators monitoring a single load can function as a current window monitor.

Current is sensed by monitoring the voltage drop across the wiring harness, pc board trace, or external sense resistor that feeds the load.

Provisions for compensating the user set limits for wiring harness resistance variations over temperature and supply voltage variations are also available.

When a limit is reached in one of the comparators, it turns on its output which can drive an external LED or microprocessor.

One side of the load can be grounded (not possible with ordinary comparator designs), which is important for automotive systems.

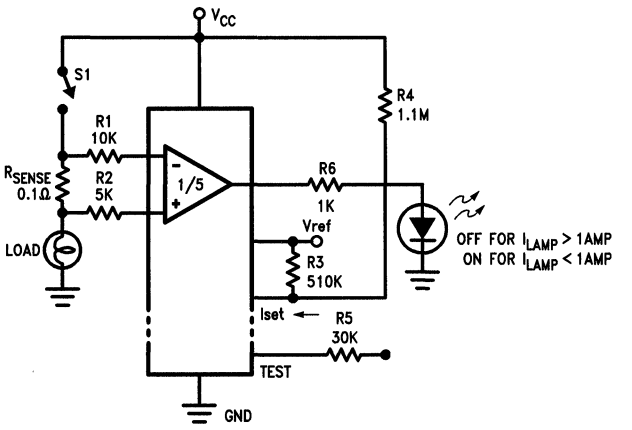
Features

- Five independent comparators
- Capable of 30 mA per output
- Low power drain
- User set input threshold voltages
- Reverse battery protection
- 60V load dump protection on supply and all inputs
- Input common mode range exceeds V_{CC}
- Short circuit protection
- Thermal overload protection
- Prove-out test pin
- Available in plastic DIP and SO packages

Applications

- Lamp fault detector
- Motor stall detector
- Power supply bus monitoring

Typical Application Circuit—Lamp Fault Detector (I_L > 1A)



TL/H/8707–2

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} and Input Pins)	
Survival Voltage ($T \leq 100$ ms)	−50V to +60V
Operational Voltage	9V to 26V
Internal Power Dissipation (Note 1)	Internally Limited
Output Short Circuit to Ground or V_{CC}	Continuous
Operating Temperature Range (T_A)	−40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
ESD Susceptibility (Note 3)	600V

Electrical Characteristics

$9V \leq V_{CC} \leq 16V$, Iset = 20 μA, T_j = 25°C (unless otherwise specified)

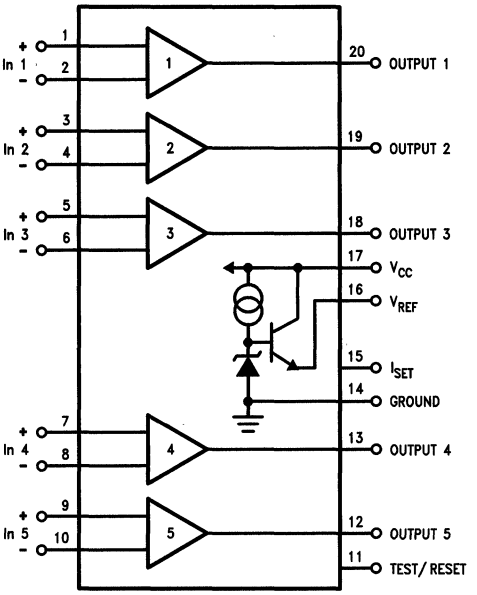
Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current	All Outputs "Off"		1.40	3.00	mA_{dc}
Reference Voltage	I_{ref} = 10 μA	5.8	6.4	7.0	V_{dc}
Reference Voltage Line Regulation	$9V \leq V_{CC} \leq 16V$, I_{ref} = 10 μA		±5	±50	mV_{dc}
Iset Voltage	Iset = 20 μA	1.20	1.40	1.60	V_{dc}
Input Offset Voltage	At Output Switch Point. V_O = 2V $9V \leq V_{CM} \leq 16V$		±1.0	±5.0	mV_{dc}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $9V \leq V_{CM} \leq 16V$		±0.10	±1.00	μA_{dc}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $9V \leq V_{CM} \leq 16V$	18.00	20.00	22.00	μA_{dc}
Input Common Mode Voltage Range		4.00		26.0	V_{dc}
Maximum Positive Input Transient	Either Input. T ≤ 100 ms	60	70		V
Maximum Negative Input Transient	Either Input. T ≤ 100 ms	−50	−60		V
Output Saturation Voltage	I_O = 2 mA, $5V \leq V_{CC} \leq 16V$		0.80	1.00	V_{dc}
	I_O = 10 mA, $5V \leq V_{CC} \leq 16V$		1.00	1.20	V_{dc}
Output Short Circuit Current	$V_O = 0V_{dc}$, Comparator "ON"	30	45	120.0	mA_{dc}
Output Leakage Current	$V_O = 0V_{dc}$. Comparator "Off"		0.01	1.00	μA_{dc}
Test Threshold Voltage	At Switch Point on Any Output V_O = 2V (Note 2)	0.80	1.25	2.00	V_{dc}
Test Threshold Current			0.2		μA_{dc}

Note 1: Thermal resistance from junction to ambient is typically 53°C/W (board mounted).

Note 2: The test pin is an active high input, i.e. all five will be forced high when this pin is driven high.

Note 3: C_{ESD} = 100 pF, R_{ESD} = 1.5k

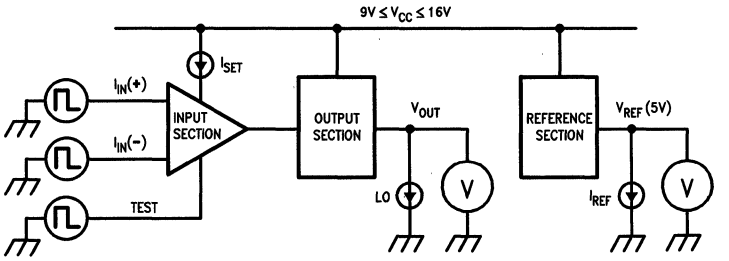
Connection Diagram



TL/H/8707–20

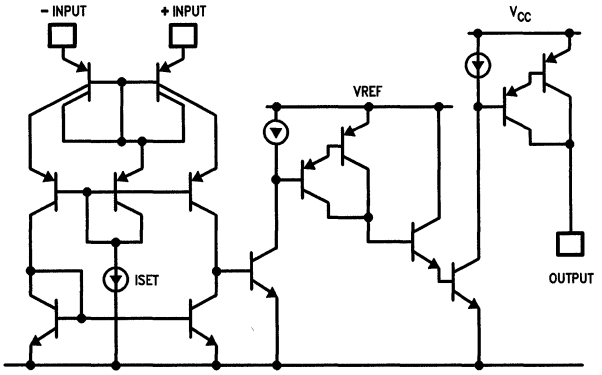
Order Number LM1946N or LM1946M
See NS Package Number M20B or N20A

Typical Test Circuit



TL/H/8707–23

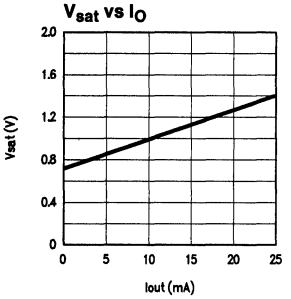
Simplified Comparator Schematic



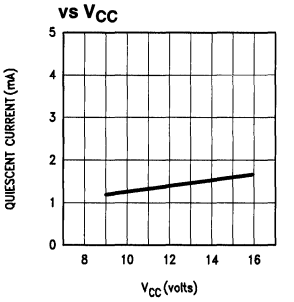
TL/H/8707–24

Typical Performance Characteristics

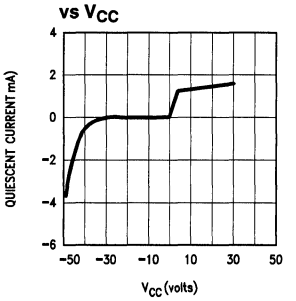
V_{sat} vs I_O



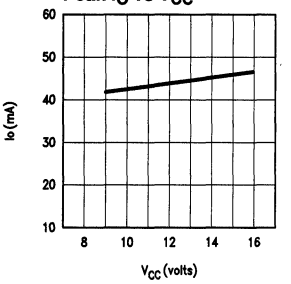
Quiescent Current vs V_{CC}



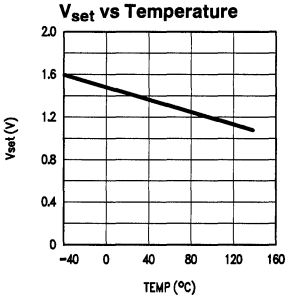
Quiescent Current vs V_{CC}



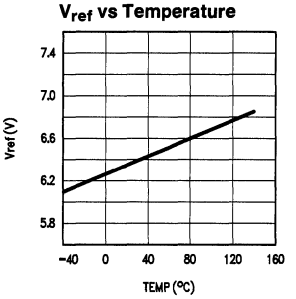
Peak I_O vs V_{CC}



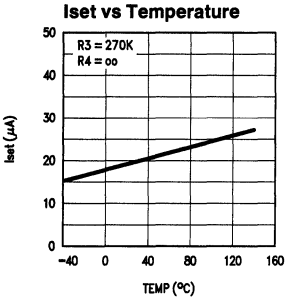
V_{set} vs Temperature



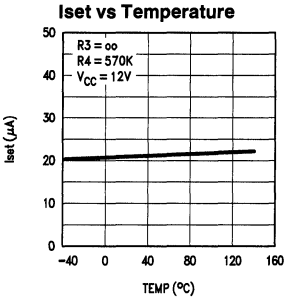
V_{ref} vs Temperature



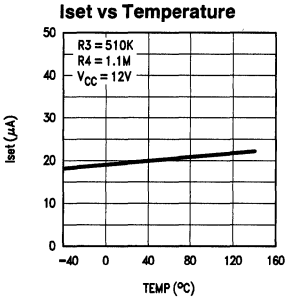
Iset vs Temperature



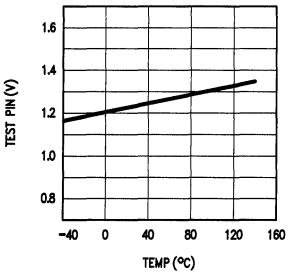
Iset vs Temperature



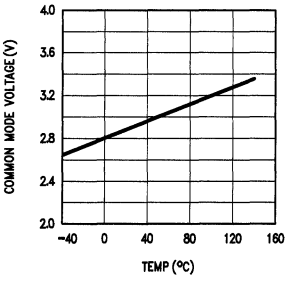
Iset vs Temperature



Test Threshold



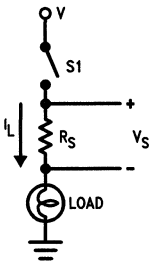
Common Mode Lower Limit



TL/H/8707–4

Application Hints

THEORY OF OPERATION: UNDER-CURRENT LIMIT DETECTOR



TL/H/8707–6

Lamp Fault Detector

FIGURE 3. Equivalent Automotive Lamp Circuit

The diagram of *Figure 3* represents the typical lamp circuit found in most automobiles. Switch S1 represents a dashboard switch, discrete power device, relay and/or flasher circuit used for turn signals. Sense resistor R_S can be an actual circuit component (such as a 0.1Ω 1W carbon resistor) or it can represent the resistance of some or all of the wiring harness. The load, represented here as a single bulb, can just as easily be two or more bulbs in parallel, such as front and rear parking lights, or left and right highbeams, etc.

One of the easiest methods to electronically monitor proper bulb operation is to sense the voltage developed across R_S by the bulb current I_L. If a fault occurs due to an open bulb filament, the load current, and sense voltage V_S, drop to zero (or to half their former values in the case of two bulbs wired in parallel). A comparator circuit can then monitor this sense voltage, and alert the system or system user (e.g. power an LED) if this sense voltage drops below a predetermined level (defined as the threshold voltage).

Typical sense voltages range from tens to hundreds of millivolts. Not only does this sense voltage vary nonlinearly with the battery voltage, it may vary significantly with ambient temperature depending on the temperature coefficient (TC) of the sense resistor or wiring harness. Since these nonlinear characteristics can vary from system to system, and sometimes even within a single system, provisions must be made to accommodate them. There are two general methodologies to accomplish this.

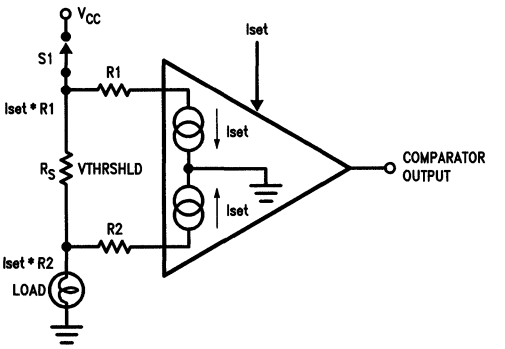
The first method uses only one bulb per monitoring circuit. A sense resistor is selected to give 50–100 mV of sense voltage in an operational circuit, and a comparator threshold detecting voltage of approximately 10 mV is set. Even if component tolerances, battery line variations, and temperature coefficients cause the sense voltage to vary 3:1 or more, circuit operation will not be affected.

The second method must be used if two or more bulbs are wired in parallel and it is necessary to detect if any single lamp fails. This is often desirable as it reduces the number of comparators and displays and system cost by at least a factor of two. In this case, the sense voltage will drop by only half (or less) of it's original value. For example, a nominal 100 mV drop across the sense resistor will drop to 50 mV if one of two bulbs fail. Therefore, a threshold detection voltage between 50 and 100 mV is required (since a 10 mV threshold would alert the system only if **both** bulbs failed). Yet a fixed threshold of 75 mV may not work if the nominal 100 mV sense voltage can vary 3:1 due to the factors mentioned earlier. What is required is a comparator with a threshold-detecting voltage that tracks the nominal sense voltage as battery line and ambient temperature change. Thus, while the sense voltage may nominally be anywhere from 50 to 150 mV, the threshold voltage will always be roughly 75% of it, or 37 mV to 112 mV, and will detect the failure of either of two bulbs.

The LM1946 integrated circuit contains five comparators especially designed for lamp monitoring requirements. Since all lamps in a system share the same battery voltage and ambient temperature, accommodations for these variations need to be made only once at the IC, and each threshold of the five comparators then tracks these variations.

SETTING THE COMPARATOR THRESHOLD VOLTAGE

The threshold voltage at which the comparator output changes state is user-set in order to accommodate the many possible system designs. The input bias currents are purposely high to accomplish this, and are each equal to the user-set current into the Iset pin (more on this later). Typically around 20 μA, the effect of this across the sense resistor R_S compared to a typical load measured in amps is negligible and can be ignored. However, when resistors R1 and R2 *(Figure 4)* are added to the circuit, a shift in the threshold voltage is effected. This occurs since each input has been affected by different IR drops. The LM1946 behaves like any other comparator in that the output switches when the input voltage at the IC pins is zero millivolts (ignoring offset voltage for the moment). If the output therefore has just switched states due to just the right threshold voltage across the sense resistor, then the sum of voltages around the resistor loop should equal zero:



TL/H/8707–9

Vthrshld = Iset (R1 − R2)

FIGURE 4. Input Bias Current

$$V_{thrshld} + I_{set} \bullet R2 - V_{offset} - I_{set} \bullet R1 = 0$$

Assuming $V_{offset} \ll V_{thrshld}$:

$$V_{thrshld} = I_{set} \bullet R1 - I_{set} \bullet R2$$

$$V_{thrshld} = I_{set} (R1 - R2)$$

Application Hints (Continued)

Typical values are:

R1 = 6.2k ±5%

R2 = 1.2k ±5%

Iset = 20 μA @ 25°C

Vthrshld = 20 μA (6.2k − 1.2k) = 100 mV

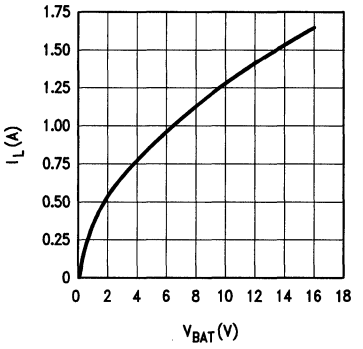
For values of sense voltages greater than 100 mV, the comparator output is off (low). Sense voltages less than 100 mV turn the output on (high).

It's also important that the output of the comparator be in the "off" state when the inputs are taken to ground, i.e. S1 is opened and the lamp is turned "off". The input section of LM1946 has been designed to turn "off" when the inputs are grounded and therefore not deliver an erroneous bulb out indication. The comparator is only activated when the inputs are above ground by at least 3V.

R1 and R2 are necessary for another reason. These resistors protect the input terminals of the IC from the many transients in an automobile found on the battery line, some of which can exceed a thousand volts for a few microseconds. A minimum value of approximately 1 kΩ is therefore recommended.

COMPENSATING FOR BATTERY VOLTAGE

The current through a typical automotive lamp, whether a headlight or dashboard illumination lamp, will vary as battery voltage changes. The change, however, is nonlinear. Doubling the battery voltage does not double the lamp current.

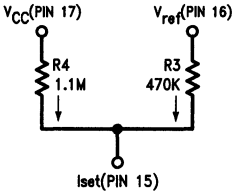


TL/H/8707–21

FIGURE 5

This occurs since a higher voltage will heat the filament more, increasing its resistance and allowing less current to flow than expected. *Figure 5* shows this effect. A best fit straight line over the normal battery range of 9V to 16V for this particular example can be given by:

$$I_L \text{ (Amps)} = 0.62 + 0.069 \bullet \text{Vbattery}$$



TL/H/8707–10

$$\text{Iset} = \frac{V_{CC} - 1.4}{R4} + \frac{\text{Vref} - 1.4}{R3}$$

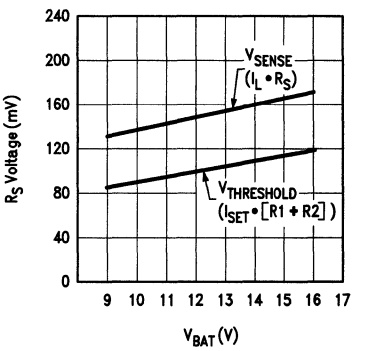
$$\text{Iset} = \frac{V_{CC}}{R4} + \frac{\text{Vref}}{R3} - 1.4\left(\frac{1}{R3} + \frac{1}{R4}\right)$$

FIGURE 6

Thus, in actual use, the LM1946 threshold voltage should track the variations in bulb current with respect to battery voltage. To accomplish this, Iset should have a component that varies with the battery. As shown in the LM1946 circuit schematic of *Figure 18*, the Iset pin is two diode drops above ground, or approximately 1.4V. A resistor from this pin to the 6.4V reference sets the fixed component of Iset; a resistor to the battery line sets the variable component. Thus, the best fit straight line in *Figure 5* can be realized exactly with only two resistors. The result is shown in *Figure 6*, giving a nominal Iset of 20 μA that tracks the bulb current as supply varies from 9V to 16V. The graph of *Figure 7* shows the final result comparing a typical sense voltage across Rs with the comparator threshold voltage as the supply varies.

COMPENSATING FOR AMBIENT TEMPERATURE VARIATION

If the sense resistors used in a system are perfect components with no temperature coefficient, then the compensation to be subsequently detailed here is unnecessary. However, resistors of the very small values usually required in a lamp monitoring system are sometimes difficult or expensive to acquire. A convenient alternative is the wiring harness, a length of wire, or even a trace on a printed circuit board. All of these are of copper material and therefore can vary by as much as 3900 ppm/°C. The LM1946 has been designed to accommodate a wide range of temperature compensation techniques. If the Iset current is designed to increase or decrease with temperature, nearly any temperature coefficient can be produced in the threshold voltage of the five input pairs.



TL/H/8707–22

FIGURE 7

Application Hints (Continued)

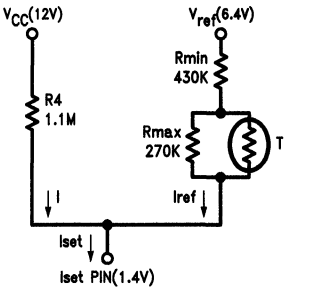
One solution is to use a low cost thermistor in conjunction with some low-TC resistors (see *Figure 8*).

There are three fixed resistors and one thermistor. This is an NTC thermistor, since it has a **negative** temperature coefficient. This is what is required in order to have Iset **increase** as the temperature rises. The data sheet with the thermistor described a number of ways to establish different final TC's. The thermistor itself has a very large TC which is somewhat difficult to describe mathematically. But, if it is used with some other fixed resistors, such as Rmin and Rmax, definite end point limits can be established and an approximate staight line TC generated. See *Figure 9* for a graphic representation of the ideal calculated values of Iset and the actual measured values generated. Notice that there is very close agreement between the two graphs. The circuit actually creates an S-shaped curve around the ideal.

The low-cost thermistor is available from Keystone and is listed as follows: RL2008-52.3K-155-D1.

OVER-CURRENT LIMIT DETECTOR

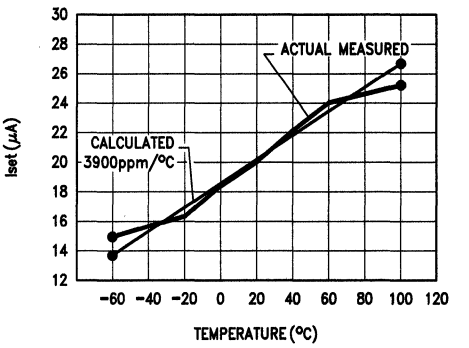
Other applications include an over-current detector, as shown in *Figure 10*. The load represented here can be either a single component or an entire system. Resistors R3



Thermistor
Keystone:
RL2008-52.3K-155-D1
100k @ 25°C

TL/H/8707–11

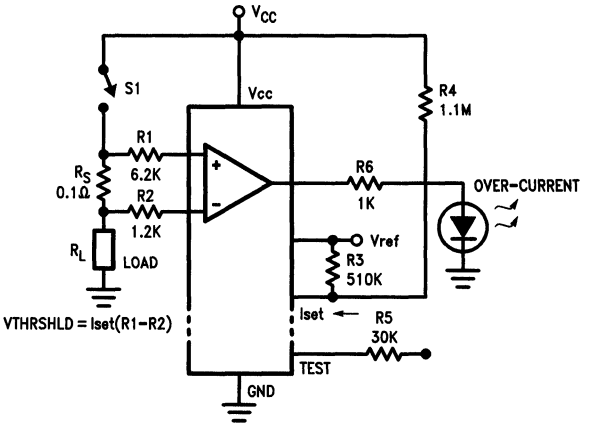
FIGURE 8. Thermistor/Resistor Network



TL/H/8707–12

FIGURE 9. Iset vs Temperature with *Figure 8* Circuit

Application Hints (Continued)



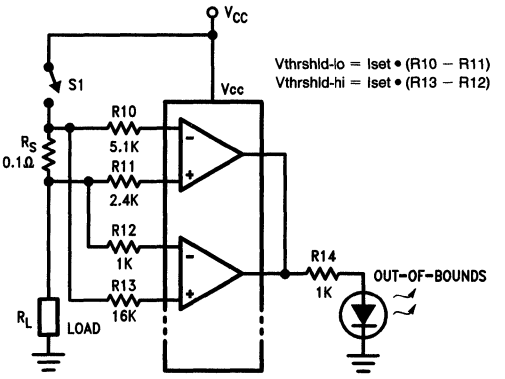
TL/H/8707–7

FIGURE 10. Using the LM1946 as an Over-Current Limit Detector

and R4 again allow the system designer to tailor the threshold limit to the V/I characteristics of each particular system. The input threshold voltage is determined by, and directly proportional to, Iset into pin 20. R3, from the on-chip reference voltage, provides a current and threshold that is independent of the supply voltage, V_{CC}. R4 provides a current directly proportional to supply. These resistors allow thresholds to be either independent of, or directly proportional to supply voltage, or anything in between. For example, the values in *Figure 10* are tailored to match the V/I characteristics of the bulb filament used in earlier examples. However, if the load had purely resistive characteristics, Iset and the threshold would be set with R4 only, eliminating R3. Likewise, if the load current was independent of supply, such as in many systems powered by a voltage regulator, Iset would be better set by R3 only, eliminating R4. Further details on this and how to handle variations with ambient temperature with resistor and thermistor combinations are discussed in detail in previous sections. Compensation for temperature variations, however, is rarely necessary since short circuit or over-current values are usually much greater than the nominal value. For example, if the load in *Figure 10* represented a DC motor, the circuit could be used to detect the motor stall condition. Stall current through the sense resistor, Rs, would typically be five times the nominal running current. By setting the threshold at three times the nominal current value, enough margin exists that minor variations due to temperature can be ignored. The variation in stall current due to battery or supply voltage can be significant, however. Being approximately proportional, Iset would best be set in this case by R4 only.

WINDOW DETECTOR

The availability of more than one comparator per IC allows many other applications. One is the current sense window detector. Many times it is useful to know that a certain current is within both an upper and lower limit. Using two of the LM1946 comparators and the circuit of *Figure 11* will accomplish this. In this particular case, high and low limits are approximately 3A and 1A respectively. The outputs can be kept separate or wired-or, as shown, to a single output load as a simple out-of-bounds detector.



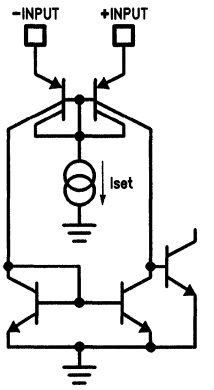
TL/H/8707–8

FIGURE 11. Current Limit Window Detector

COMPARATOR INPUT STAGE

The LM1946 IC consists of five specially designed comparator input circuits to monitor the IR drop across the wiring harness or the sense resistor between the battery and the light bulb. These comparators have been designed to accommodate a wide range of input signals without damage to the IC or the load circuitry. The inputs can easily withstand a common mode voltage above the positive supply since the inputs are the emitters of two matched PNP devices (see *Figure 12*). This is vital in a system which must operate in the conditions present under the hood of an automobile. The inputs can also survive when taken well below ground. If a negative voltage is present at the inputs of the comparator, the two emitter-base PNP junctions become reverse biased and block any current flow in or out of the device.

Application Hints (Continued)



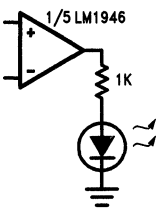
TL/H/8707–13

FIGURE 12. Comparator Input Stage

THE OUTPUT SECTION

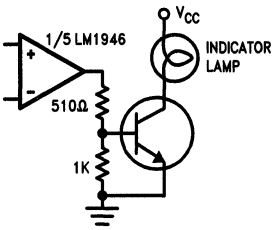
The output section of the LM1946 is different from most automotive comparators as it employs high beta proprietary PNP transistors which are very rugged and capable of higher output currents. Each of the five comparator outputs is capable of about 25 mA of drive and are internally current limited and protected against supply overvoltage. The LM1946 is therefore capable of driving LED's directly and larger bulbs via an external grounded base NPN (see *Figures 13* and *14*). The outputs can also be wired-or together without harm.

For use in systems with a microprocessor flag instead of a dashboard indicator, the LM1946 can be powered by a standard 5V logic supply. This prevents the LM1946 output from swinging above the microprocessor supply which might cause latch problems. Since the input common mode range is independent of supply, the inputs can still operate at any level up to 26V. Since the outputs can source current only, pull-down resistors as in *Figure 15* are required, their value depending on the input drive requirements of the particular microprocessor used.



TL/H/8707–19

FIGURE 13



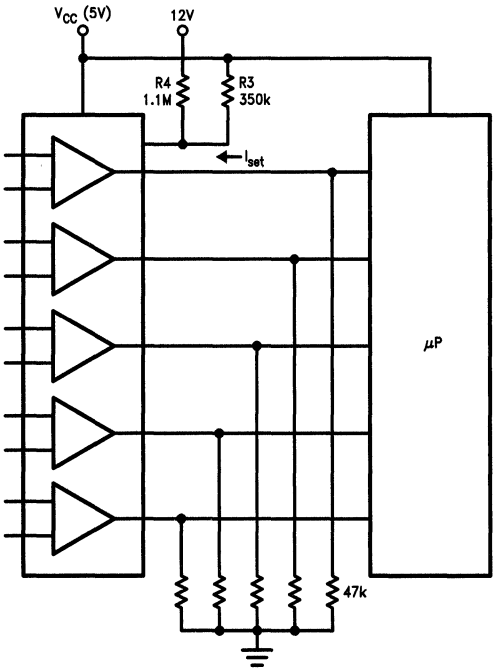
TL/H/8707–14

FIGURE 14

TEST PIN

The test pin is a high impedance logic input. Forcing this pin high (≥ 2V) forces all five comparator outputs on. This is used to test the indicator LED display (or other output load). The usual application circuit connects this pin to the ignition crank line. During engine crank, therefore, the LM1946 output display will light, similar to the usual dashboard indicators. The test pin was designed to operate with the usual transient voltages found on the crank line as long as a limiting resistor (e.g. 30k) separates them *(Figure 1)*.

Minimum pulse width (ms) ≈ 0.01 + 1.5 • C1 (μF)



TL/H/8707–15

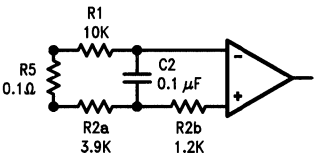
FIGURE 15

Application Hints (Continued)

MORE NOISE FILTERING

The current flowing through the sense resistor and certain loads can sometimes be very noisy, particularly when the load is a DC motor, or switching supply. Large amounts of noise on the supply line can also cause problems when threshold voltages are set to very small values. In these cases, while the average current level may remain well below the threshold trip point, noise peaks may exceed it. A LED display could then flicker or appear dimly lit, or excessive software routines and processor time may be required for a μP to disregard such noise. Often such noise must be filtered directly at the inputs, using the input resistors R1 and R2 and a capacitor. Care must be taken, however, that such a filter will not cause an erroneous output state upon power-up or whenever switch S1 is closed. The most effective general methodology to achieve this is to split the resistor in the positive input lead into two resistor values and connect a capacitor from here to the negative input. For example, the 1.2k resistor R2 of *Figure 10* could be replaced with 3.9k and 1.2k resistors as shown in *Figure 16a* (R1 increasing from 6.2k to 10k to compensate). The value of capacitor C2 depends upon the degree of filtering required, the amount of noise present, and the response times desired. The choice of values for the new resistors is almost arbitrary. Generally the larger value is attached to the sense resistor for better decoupling. The smaller value must be large enough so that the DC voltage across it upon power-up exceeds the maximum offset voltage expected of the comparator (i.e. Iset*R2b > 5.0mV). It is this requirement that guarantees that the output will not be in an erroneous high state upon power-up or whenever S1 is closed. (Should this feature be unnecessary to a particular application circuit, the methodology described can be replaced with a simple capacitor across the comparator input pins).

For extremely severe cases, additional filter stages can be cascaded at the inputs (see *Figure 17*). Since the input bias currents of the comparator are equal at the input threshold level, the voltage drops across the 1k resistors cancel and do not affect the DC operation of the circuit (ignoring resistor match tolerance and Ios). If an application circuit is noisy enough to require such an elaborate filter, then ferrite beads, shown here as L1 and L2, will also probably help.



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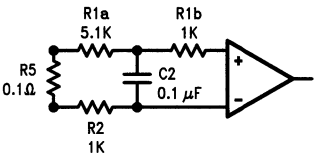
a. Open-Circuit Detector



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b. Over-Current Limit Detector

FIGURE 16. Input Noise Filters for Various Application Circuits

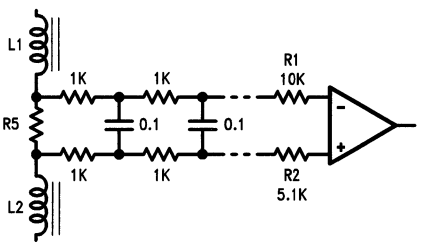

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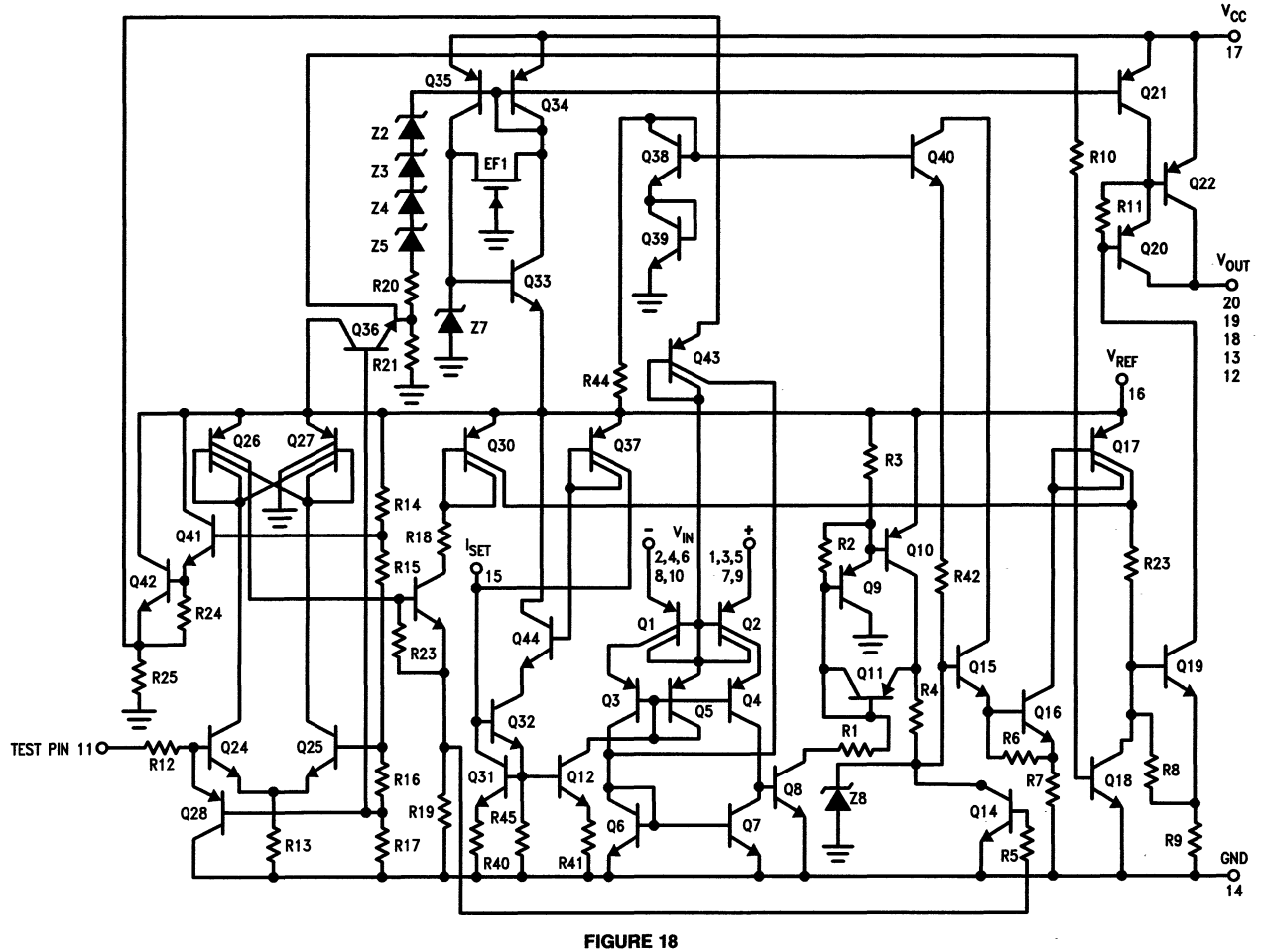
FIGURE 17. Additional Noise Filters

Circuit Schematic



TL/H/8707–3

FIGURE 18

National Semiconductor

LM1949 Injector Drive Controller

General Description

The LM1949 linear integrated circuit serves as an excellent control of fuel injector drive circuitry in modern automotive systems. The IC is designed to control an external power NPN Darlington transistor that drives the high current injector solenoid. The current required to open a solenoid is several times greater than the current necessary to merely hold it open; therefore, the LM1949, by directly sensing the actual solenoid current, initially saturates the driver until the "peak" injector current is four times that of the idle or "holding" current *(Figure 3-Figure 7)*. This guarantees opening of the injector. The current is then automatically reduced to the sufficient holding level for the duration of the input pulse. In this way, the total power consumed by the system is dramatically reduced. Also, a higher degree of correlation of fuel to the input voltage pulse (or duty cycle) is achieved, since opening and closing delays of the solenoid will be reduced.

Normally powered from a 5V ±10% supply, the IC is typically operable over the entire temperature range (−55°C to +125°C ambient) with supplies as low as 3 volts. This is particularly useful under "cold crank" conditions when the battery voltage may drop low enough to deregulate the 5-volt power supply.

The LM1949 is available in the plastic miniDIP, (contact factory for other package options).

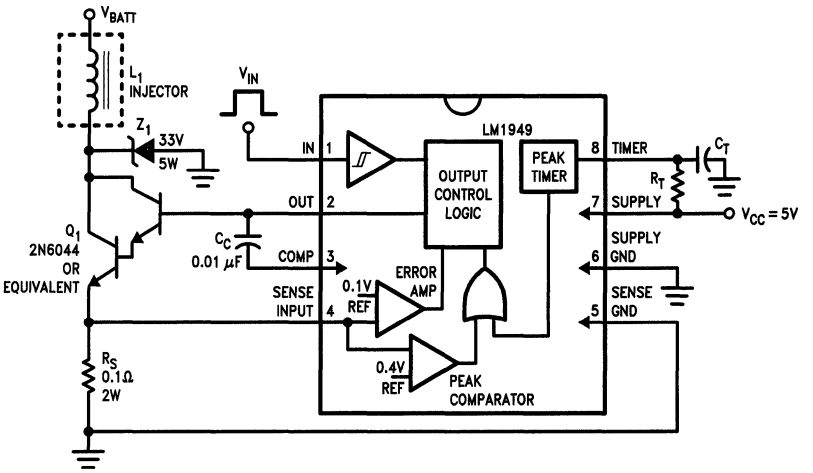
Features

- Low voltage supply (3V-5.5V)
- 22 mA output drive current
- No RFI radiation
- Adaptable to all injector current levels
- Highly accurate operation
- TTL/CMOS compatible input logic levels
- Short circuit protection
- High impedance input
- Externally set holding current, I_H
- Internally set peak current ($4 \times I_H$)
- Externally set time-out
- Can be modified for full switching operation
- Available in plastic 8-pin miniDIP

Applications

- Fuel injection
- Throttle body injection
- Solenoid controls
- Air and fluid valves
- DC motor drives

Typical Application Circuit



TL/H/5062–1

FIGURE 1. Typical Application and Test Circuit

Order Number LM1949N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

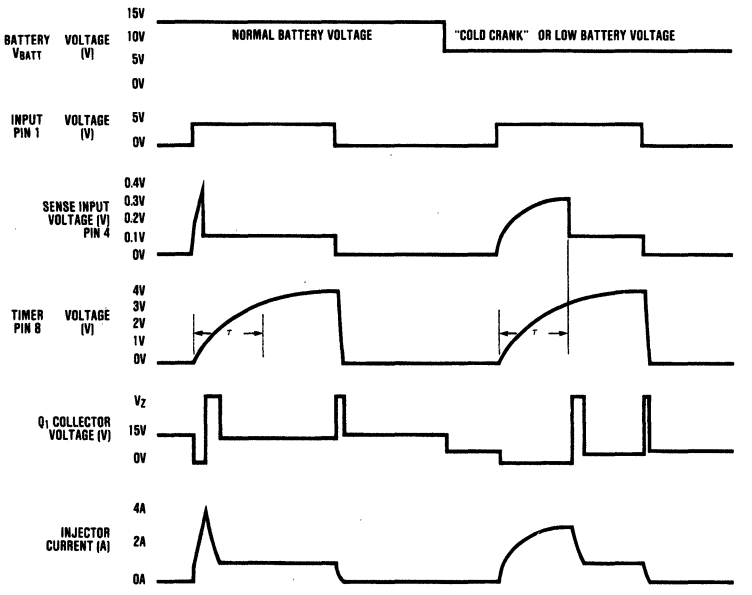
Supply Voltage	8V
Power Dissipation (Note 1)	1235 mW
Input Voltage Range	−0.3V to V_{CC}
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering 10 sec.)	260°C

Electrical Characteristics (V_{CC} = 5.5V, V_{IN} = 2.4V, T_j = 25°C, *Figure 1*, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current					
	Off	V_{IN} = 0V		11	23	mA
	Peak	Pin 8 = 0V		28	54	mA
	Hold	Pin 8 Open		16	26	mA
V_{OH}	Input On Level	V_{CC} = 5.5V		1.4	2.4	V
		V_{CC} = 3.0V		1.2	1.6	V
V_{OL}	Input Off Level	V_{CC} = 5.5V	1.0	1.35		V
		V_{CC} = 3.0V	0.7	1.15		V
I_B	Input Current		−25	3	+25	μA
I_{OP}	Output Current					
	Peak	Pin 8 = 0V	−10	−22		mA
	Hold	Pin 8 Open	−1.5	−5		mA
V_S	Output Saturation Voltage	10 mA, V_{IN} = 0V		0.2	0.4	V
	Sense Input					
V_P	Peak Threshold	V_{CC} = 4.75V	350	386	415	mV
V_H	Hold Reference		88	94	102	mV
t	Time-out, t	$t \div R_T C_T$	90	100	110	%

NOTE 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Typical Circuit Waveforms



TL/H/5062–2

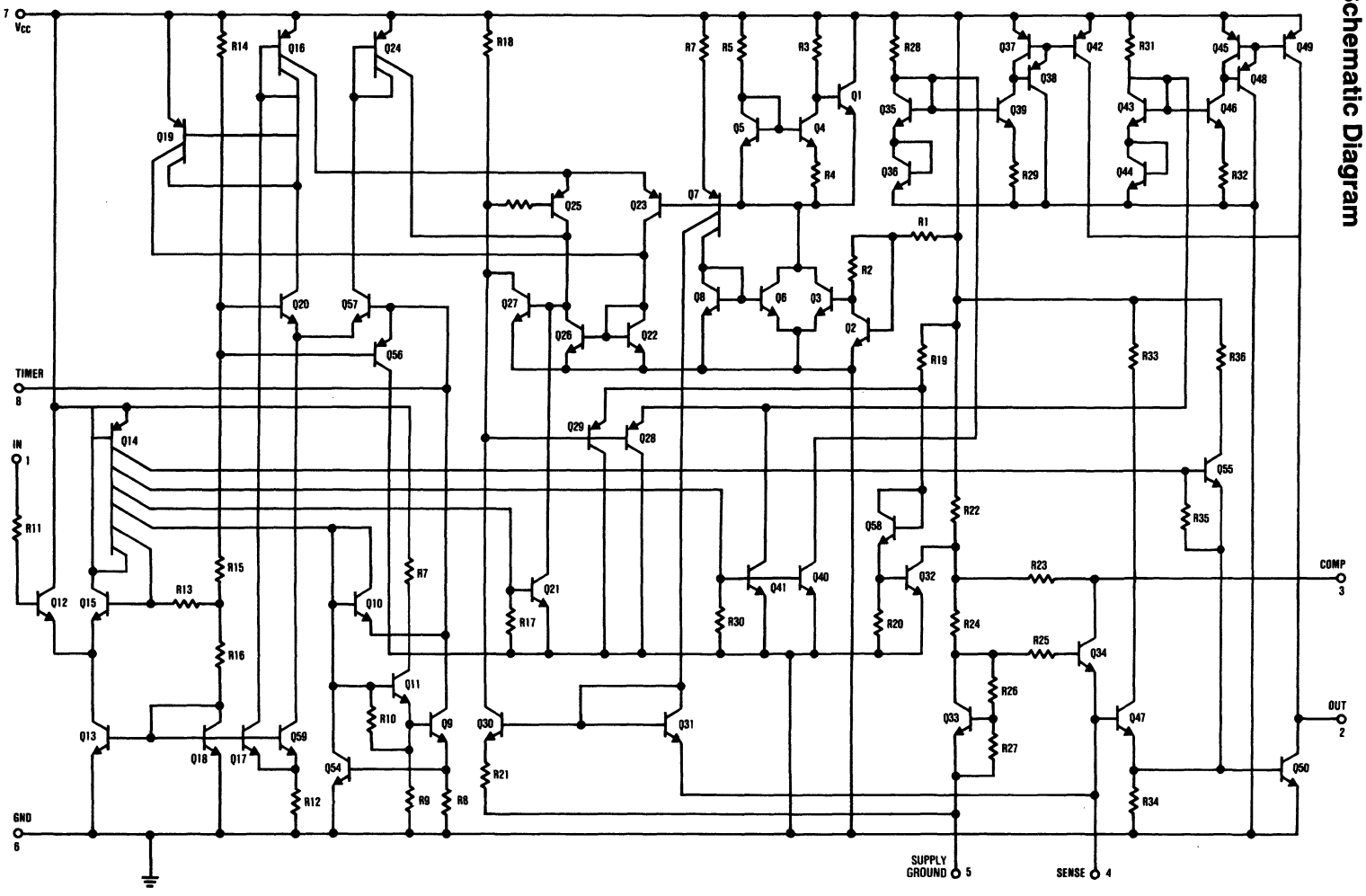


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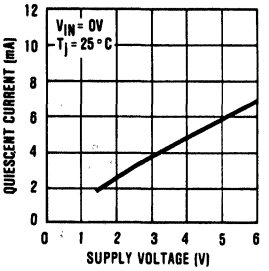
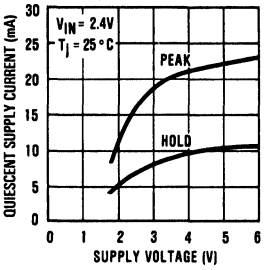
FIGURE 2. LM1949 Circuit

Typical Performance Characteristics

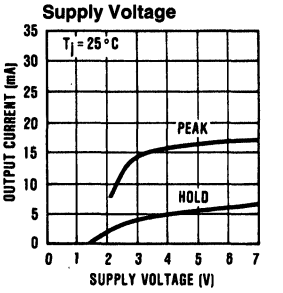
Quiescent Current vs Supply Voltage



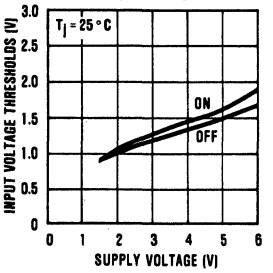
Supply Current vs Supply Voltage



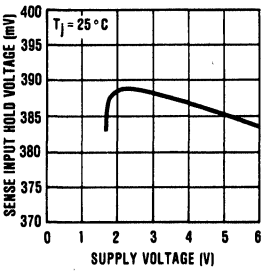
Output Current vs Supply Voltage



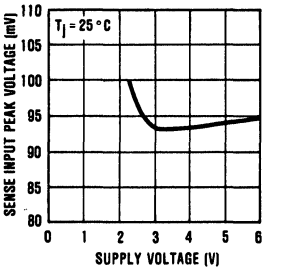
Input Voltage Thresholds vs Supply Voltage



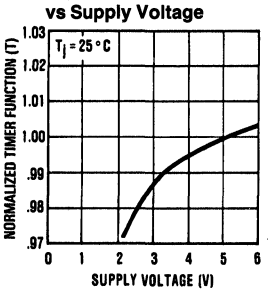
Sense Input Peak Voltage vs Supply Voltage



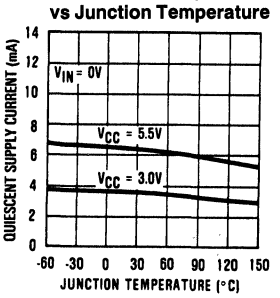
Sense Input Hold Voltage vs Supply Voltage



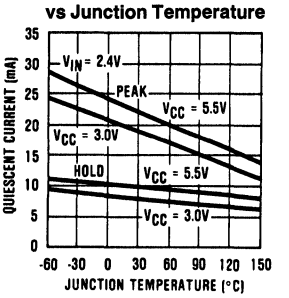
Normalized Timer Function vs Supply Voltage



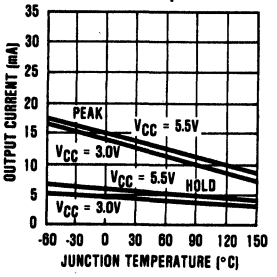
Quiescent Supply Current vs Junction Temperature



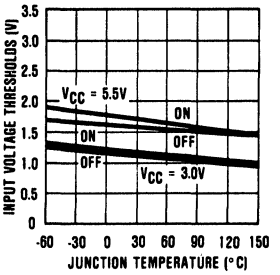
Quiescent Supply Current vs Junction Temperature



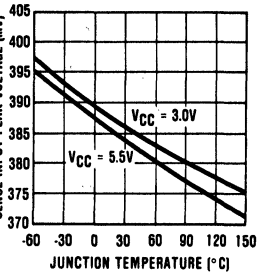
Output Current vs Junction Temperature



Input Voltage Thresholds vs Junction Temperature



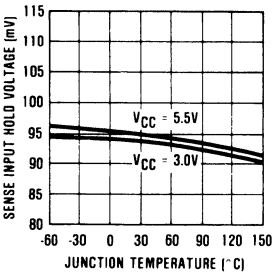
Sense Input Peak Voltage vs Junction Temperature



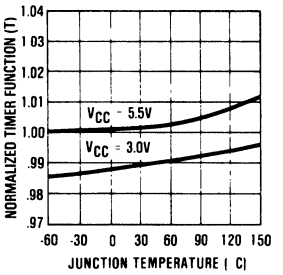
TL/H/5062–4

Typical Performance Characteristics (Continued)

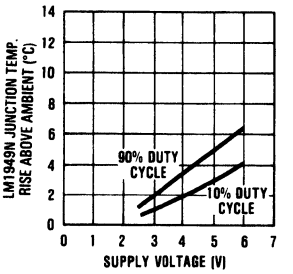
Sense Input Hold Voltage vs Junction Temperature



Normalized Timer Function vs Junction Temperature



LM1949N Junction Temperature Rise Above Ambient vs Supply Voltage



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Application Hints

The injector driver integrated circuits were designed to be used in conjunction with an external controller. The LM1949 derives its input signal from either a control oriented processor (COPS™), microprocessor, or some other system. This input signal, in the form of a square wave with a variable duty cycle and/or variable frequency, is applied to Pin 1. In a typical system, input frequency is proportional to engine RPM. Duty cycle is proportional to the engine load. The circuits discussed are suitable for use in either open or closed loop systems. In closed loop systems, the engine exhaust is monitored and the air-to-fuel mixture is varied (via the duty cycle) to maintain a perfect, or stochiometric, ratio.

INJECTORS

Injectors and solenoids are available in a vast array of sizes and characteristics. Therefore, it is necessary to be able to design a drive system to suit each type of solenoid. The purpose of this section is to enable any system designer to use and modify the LM1949 and associated circuitry to meet the system specifications.

Fuel injectors can usually be modeled by a simple RL circuit. *Figure 3* shows such a model for a typical fuel injector. In actual operation, the value of L_1 will depend upon the status of the solenoid. In other words, L_1 will change depending

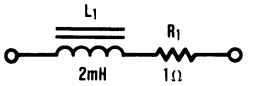

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FIGURE 3. Model of a Typical Fuel Injector

upon whether the solenoid is open or closed. This effect, if pronounced enough, can be a valuable aid in determining the current necessary to open a particular type of injector. The change in inductance manifests itself as a breakpoint in the initial rise of solenoid current. The waveforms on Page 2 at the sense input show this occurring at approximately 130 mV. Thus, the current necessary to overcome the constrictive forces of that particular injector is 1.3 amperes.

PEAK AND HOLD CURRENTS

The peak and hold currents are determined by the value of the sense resistor R_S. The driver IC, when initiated by a logic 1 signal at Pin 1, initially drives Darlington transistor Q_1 into saturation. The injector current will rise exponentially from zero at a rate dependent upon L_1, R_1, the battery voltage and the saturation voltage of Q_1. The drop across the sense resistor is created by the solenoid current, and when this drop reaches the peak threshold level, typically 385 mV, the IC is tripped from the peak state into the hold state. The IC now behaves more as an op amp and drives Q_1 within a closed loop system to maintain the hold reference voltage, typically 94 mV, across R_S. Once the injector current drops from the peak level to the hold level, it remains there for the duration of the input signal at Pin 1. This mode of operation is preferable when working with solenoids, since the current required to overcome kinetic and constriction forces is often a factor of four or more times the current necessary to hold the injector open. By holding the injector current at one fourth of the peak current, power dissipation in the solenoids and Q_1 is reduced by at least the same factor.

In the circuit of *Figure 1*, it was known that the type of injector shown opens when the current exceeds 1.3 amps and closes when the current then falls below 0.3 amps. In order to guarantee injector operation over the life and temperature range of the system, a peak current of approximately 4 amps was chosen. This led to a value of R_S of 0.1Ω. Dividing the peak and hold thresholds by this factor gives peak and hold currents through the solenoid of 3.85 amps and 0.94 amps respectively.

Different types of solenoids may require different values of current. The sense resistor R_S may be changed accordingly. An 8-amp peak injector would use R_S equal to .05Ω, etc. Note that for large currents above one amp, IR drops within the component leads or printed circuit board may create substantial errors unless appropriate care is taken. The sense input and sense ground leads (Pins 4 and 5 respectively), should be Kelvin connected to R_S. High current should not be allowed to flow through any part of these traces or connections. An easy solution to this problem on double-sided PC boards (without plated-through holes) is to have the high current trace and sense trace attach to the R_S lead from opposite sides of the board.

TIMER FUNCTION

The purpose of the timer function is to limit the power dissipated by the injector or solenoid under certain conditions. Specifically, when the battery voltage is low due to engine cranking, or just undercharged, there may not be sufficient voltage available for the injector to achieve the peak current. In the *Figure 2* waveforms under the low battery condition, the injector current can be seen to be leveling out at 3

Timer Function (Continued)

amps, or 1 amp below the normal threshold. Since continuous operation at 3 amps may overheat the injectors, the timer function on the IC will force the transition into the hold state after one time constant (the time constant is equal to R_TC_T). The timer is reset at the end of each input pulse. For systems where the timer function is not needed, it can be disabled by grounding Pin 8. For systems where the initial peak state is not required, (i.e., where the solenoid current rises immediately to the hold level), the timer can be used to disable the peak function. This is done by setting the time constant equal to zero, (i.e., $C_T = 0$). Leaving R_T in place is recommended. The timer will then complete its time-out and disable the peak condition before the solenoid current has had a chance to rise above the hold level.

The actual range of the timer in injection systems will probably never vary much from the 3.9 milliseconds shown in *Figure 1*. However, the actual useful range of the timer extends from microseconds to seconds, depending on the component values chosen. The useful range of R_T is approximately 1k to 240k. The capacitor C_T is limited only by stray capacitances for low values and by leakages for large values.

The capacitor reset time at the end of each controller pulse is determined by the supply voltage and the capacitor value. The IC resets the capacitor to an initial voltage (V_{BE}) by discharging it with a current of approximately 15 mA. Thus, a 0.1 μF cap is reset in approximately 25 μs.

COMPENSATION

Compensation of the error amplifier provides stability for the circuit during the hold state. External compensation (from Pin 2 to Pin 3) allows each design to be tailored for the characteristics of the system and/or type of Darlington power device used. In the vast majority of designs, the value or type of the compensation capacitor is not critical. Values of 100 pF to 0.1 μF work well with the circuit of *Figure 1*. The value shown of .01 μF (disc) provides a close optimum in choice between economy, speed, and noise immunity. In some systems, increased phase and gain margin may be acquired by bypassing the collector of Q_1 to ground with an appropriately rated 0.1 μF capacitor. This is, however, rarely necessary.

FLYBACK ZENER

The purpose of zener Z_1 is twofold. Since the load is inductive, a voltage spike is produced at the collector of Q_1 anytime the injector current is reduced. This occurs at the peak-to-hold transition, (when the current is reduced to one fourth of its peak value), and also at the end of each input pulse, (when the current is reduced to zero). The zener provides a current path for the inductive kickback, limiting the voltage spike to the zener value and preventing Q_1 from damaging voltage levels. Thus, the rated zener voltage at the system peak current must be less than the guaranteed minimum breakdown of Q_1. Also, even while Z_1 is conducting the majority of the injector current during the peak-to-hold transition (see *Figure 4*), Q_1 is operating at the hold current level. This fact is easily overlooked and, as described in the following text, can be corrected if necessary. Since the error amplifier in the IC demands 94 mV across R_S, Q_1 will be biased to provide exactly that. Thus, the safe operating area (SOA) of Q_1 must include the hold current with a V_{CE} of Z_1 volts. For systems where this is not desired, the zener anode may be reconnected to the top of R_S as shown in *Figure 5*. Since the voltage across the sense resistor now accurately portrays the injector current at all times, the error

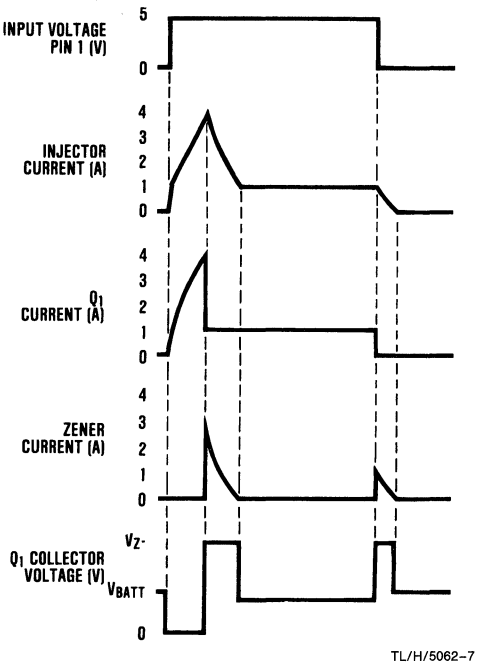

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FIGURE 4. Circuit Waveforms

amplifier keeps Q_1 off until the injector current has decayed to the proper value. The disadvantage of this particular configuration is that the ungrounded zener is more difficult to heat sink if that becomes necessary.

The second purpose of Z_1 is to provide system transient protection. Automotive systems are susceptible to a vast array of voltage transients on the battery line. Though their duration is usually only milliseconds long, Q_1 could suffer permanent damage unless buffered by the injector and Z_1. This is one reason why a zener is preferred over a clamp diode back to the battery line, the other reason being long decay times.

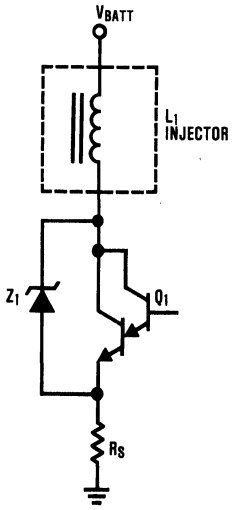

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FIGURE 5. Alternate Configuration for Zener Z_1

POWER DISSIPATION

The power dissipation of the system shown in *Figure 1* is dependent upon several external factors, including the frequency and duty cycle of the input waveform to Pin 1. Calculations are made more difficult since there are many discontinuities and breakpoints in the power waveforms of the various components, most notably at the peak-to-hold transition. Some generalizations can be made for normal operation. For example, in a typical cycle of operation, the majority of dissipation occurs during the hold state. The hold state is usually much longer than the peak state, and in the peak state nearly all power is stored as energy in the magnetic field of the injector, later to be dumped mostly through the zener. While this assumption is less accurate in the case of low battery voltage, it nevertheless gives an unexpectedly accurate set of approximations for general operation.

The following nomenclature refers to *Figure 1*. Typical values are given in parentheses:

R_S = Sense Resistor (0.1Ω)
V_H = Sense Input Hold Voltage (.094V)
V_p = Sense Input Peak Voltage (.385V)
V_Z = Z_1 Zener Breakdown Voltage (33V)
V_{BATT} = Battery Voltage (14V)
L_1 = Injector Inductance (.002H)
R_1 = Injector Resistance (1Ω)
n = Duty Cycle of Input Voltage of Pin 1 (0 to 1)
f = Frequency of Input (10Hz to 200Hz)

Q_1 Power Dissipation:

$$P_Q \approx n \bullet V_{BATT} \bullet \frac{V_H}{R_S} \text{ Watts}$$

Zener Dissipation:

$$P_Z \approx V_Z \bullet L_1 \bullet f \bullet \frac{(V_P^2 + V_H^2)}{((V_Z - V_{BATT}) \bullet R_S^2)} \text{ Watts}$$

Injector Dissipation:

$$P_I \approx n \bullet R_1 \bullet \frac{V_H^2}{R_S^2} \text{ Watts}$$

Sense Resistor:

$$P_R \approx n \frac{V_H^2}{R_S^2} \text{ Watts}$$

$$P_R \text{ (worst case)} \approx n \frac{V_P^2}{R_S^2} \text{ Watts}$$

SWITCHING INJECTOR DRIVER CIRCUIT

The power dissipation of the system, and especially of Q_1, can be reduced by employing a switching injector driver circuit. Since the injector load is mainly inductive, transistor Q_1 can be rapidly switched on and off in a manner similar to switching regulators. The solenoid inductance will naturally integrate the voltage to produce the required injector current, while the power consumed by Q_1 will be reduced. A note of caution: The large amplitude switching voltages that are present on the injector can and do generate a tremendous amount of radio frequency interference (RFI). Because of this, switching circuits are not recommended. The extra cost of shielding can easily exceed the savings of reduced power. In systems where switching circuits are mandatory, extensive field testing is required to guarantee that RFI cannot create problems with engine control or entertainment equipment within the vicinity.

The LM1949 can be easily modified to function as a switcher. Accomplished with the circuit of *Figure 7*, the only additional components required are two external resistors, R_A and R_B. Additionally, the zener needs to be reconnected, as shown, to R_S. The amount of ripple on the hold current is easily controlled by the resistor ratio of R_A to R_B. R_B is kept small so that sense input bias current (typically 0.3 mA) has negligible effect on V_H. Duty cycle and frequency of oscillation during the hold state are dependent on the injector characteristics, R_A, R_B, and the zener voltage as shown in the following equations.

$$\text{Hold Current} \approx \frac{V_H}{R_S}$$

$$\text{Minimum Hold Current} \approx \frac{\left(V_H - \frac{R_B}{R_A} \bullet V_Z\right)}{R_S}$$

$$\text{Ripple or } \Delta I \text{ Hold} \approx \frac{R_B}{R_A} \bullet V_Z \bullet \frac{1}{R_S}$$

$$f_o \approx \frac{R_S}{L_1} \bullet \frac{R_A}{R_B} \bullet \frac{V_{BATT}}{V_Z} \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right)$$

f_o = Hold State Oscillation Frequency

$$\text{Duty Cycle of } f_o \approx \frac{V_{BATT}}{V_Z}$$

Component Power Dissipation

$$P_Q \approx n \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right) \bullet \frac{V_{SAT}}{R_S} \bullet V_H$$

V_{SAT} = Q_1 Saturation Volt @ ~ 1 Amp (1.5V)

$$P_Z \approx n \bullet \frac{V_{BATT} \bullet V_H}{R_S}$$

$$P_{RA} \approx \frac{V_B \bullet V_Z}{R_1}$$

As shown, the power dissipation by Q_1 in this manner is substantially reduced. Measurements made with a thermocouple on the bench indicated better than a fourfold reduction in power in Q_1. However, the power dissipation of the zener (which is independent of the zener voltage chosen) is increased over the circuit of *Figure 1*.

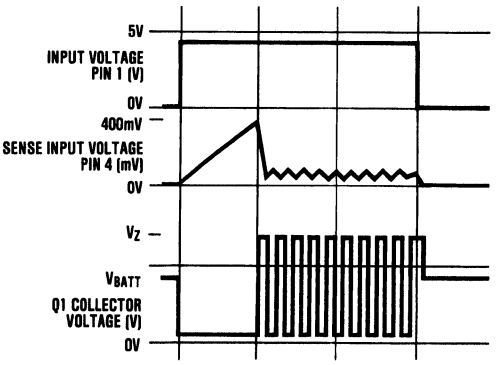

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FIGURE 6. Switching Waveforms

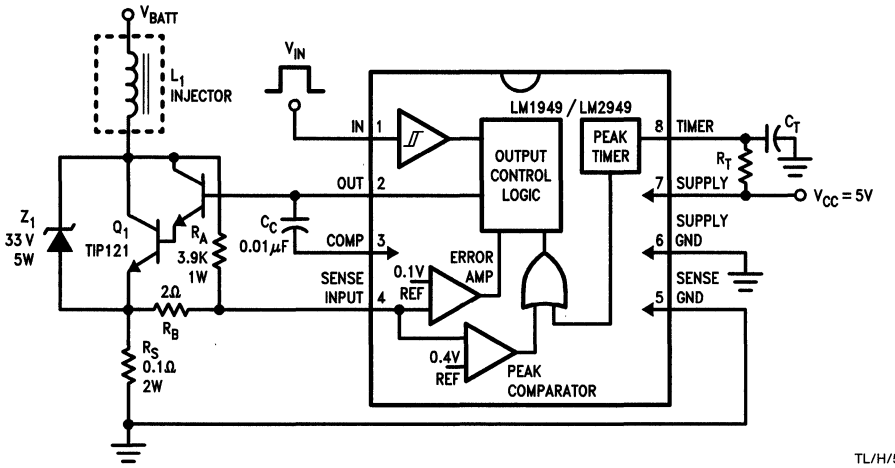

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FIGURE 7. Switching Application Circuit

National Semiconductor

LM1950 750 mA High Side Switch

General Description

The LM1950 is a high current, high side (PNP) power switch for driving ground referenced loads. Intended for industrial and automotive applications the LM1950 is guaranteed to deliver 750 mA continuous load current (with typically 1.4 Amps peak) and can withstand supply voltage transients up to +60V and −50V. When switched OFF the quiescent current drain from the input power supply is less than 100 μA which can allow continuous connection to a battery power source.

The LM1950 will drive all types of resistive or reactive loads. To obtain a rapid decay time of the energy in inductive loads, the output is internally protected but not clamped and can swing below ground to at least 54V negative with respect to the input power supply voltage.

The ON/OFF input can be driven with standard 5V TTL or CMOS compatible logic levels independent of the V_{CC} supply voltage used. Built in protection features include short circuit protection, thermal shutdown, over-voltage shutdown to protect load circuits and protection against reverse polarity input connections. The LM1950 is available in a 5-lead power TO-220 package and specified over a wide −40°C to 125°C operating temperature range.

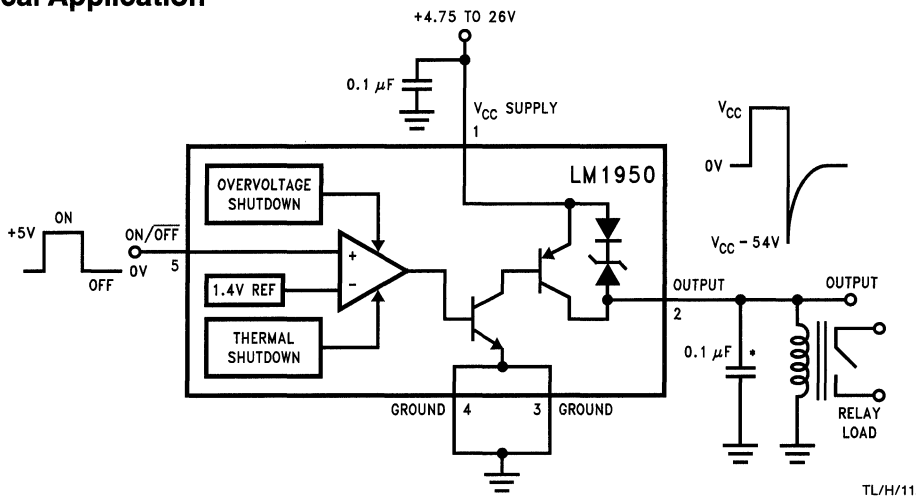
Features

- 750 mA continuous output drive current
- Less than 100 μA quiescent current in OFF state
- Low input/output voltage drop
- +60V/−50V transient protection
- Drives resistive or reactive loads
- Unclamped output for fast inductive decay tmies
- Reverse battery protected
- Short circuit proof
- Overvoltage shutdown to protect loads
- TTL/CMOS compatible control input
- Thermal overload protection

Applications

- Relay driver
- Solenoid/Valve driver
- Lamp driver
- Load circuit switching
- Motor driver

Typical Application



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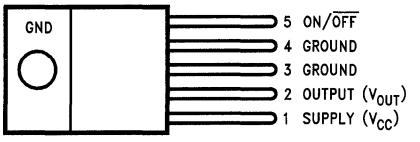
*Required for stability

Connection Diagram

TO 220, 5 Lead



TL/H/11237–2

Front View
Order Number LM1950T
See NS Package Number T05A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
Continuous	26V
Transient ($\tau \leq$ 100 ms)	−50V to +60V
Reverse Polarity (continuous)	−15V
On/$\overline{\text{Off}}$ Voltage	−0.3V to +6.0V
Power Dissipation	Internally Limited
Load Inductance	150 mH
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	230°C
ESD Susceptibility (Note 2)	2000V

Operating Ratings (Note 1)

Temperature Range (T_A)	−40°C to +125°C
Supply Voltage Range	4.75V to 26V
Thermal Resistances:	
Junction to Case ($\theta_{j\text{-}c}$)	3°C/W
Case to Ambient ($\theta_{c\text{-}a}$)	50°C/W

Electrical Characteristics

V_{CC} = 14V, I_{OUT} = 150 mA unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ 125°C, all other specifications are for $T_A = T_J$ = 25°C

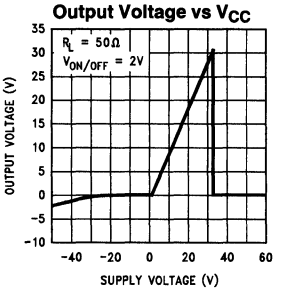
Parameter	Conditions	Typical	Limit	Units (Limit)
Supply Voltage				
Operational			4.75/**4.75**	V (Min)
			26/**26**	V (Max)
Survival			−15/−**15**	V_{DC} (Min)
Transient	t = 1 ms, τ = 100 ms, 1% dutycycle		60/**60**	V (Max)
			−50/−**50**	V (Min)
Supply Current	$V_{ON/\overline{OFF}}$ = 0.8V	20	100/**100**	μA(Max)
	$V_{ON/\overline{OFF}}$ = 2.0V			
	I_{OUT} = 0 mA	5	10/**10**	mA (Max)
	I_{OUT} = 250 mA	275	350/**350**	mA (Max)
	I_{OUT} = 500 mA	550	700/**700**	mA (Max)
	I_{OUT} = 750 mA	825	950/**950**	mA (Max)
Input to Output Voltage Drop	I_{OUT} = 250 mA	0.30	0.5/**0.6**	V (Max)
	I_{OUT} = 500 mA	0.50	0.7/**1.0**	V (Max)
	I_{OUT} = 750 mA	0.75	1.1/**1.4**	V (Max)
Short Circuit Current		1.5	1.0/**0.75**	A (Min)
			2.0/**2.0**	A (Max)
Output Leakage Current	$V_{ON/\overline{OFF}}$ = 0.8V	10	50/**50**	μA (Max)
ON/$\overline{\text{OFF}}$ Input Threshold Voltage		1.4	0.8/**0.8**	V (Min)
			2.0/**2.0**	V (Max)
ON/$\overline{\text{OFF}}$ Input Current	$V_{ON/\overline{OFF}}$ = 0.8V	0.1	5/**10**	μA (Max)
	$V_{ON/\overline{OFF}}$ = 2.0V	1	10/**20**	μA (Max)
	$V_{ON/\overline{OFF}}$ = 5.25V	50	100/**100**	μA (Max)
Overvoltage Shutdown Threshold		33	27/**27**	V (Min)
			37/**37**	V (Max)
Inductive Clamp Output Voltage	$V_{ON/\overline{OFF}}$ = 2V to 0.8V, I_{OUT} = 100 mA	−45	−120/−**120**	V (Max)
			−40/−**40**	V (Min)
Output Turn-On Delay	$V_{ON/\overline{OFF}}$ 0.8V to 2V	4.2	**20**	μs
Output Turn-Off Delay	$V_{ON/\overline{OFF}}$ 2V to 0.8V	4.5	**20**	μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

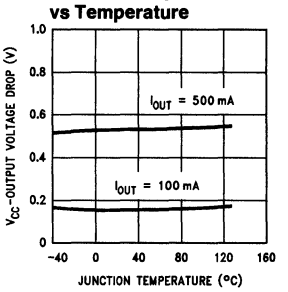
Note 2: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

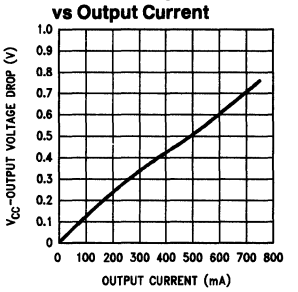
Output Voltage vs V_{CC}



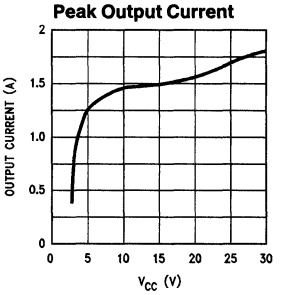
Output Voltage Drop vs Temperature



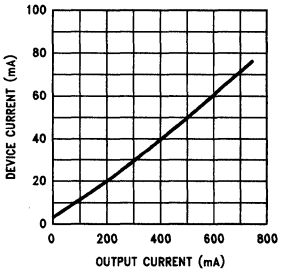
Output Voltage Drop vs Output Current



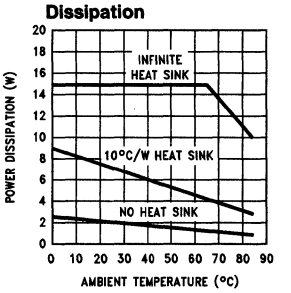
Peak Output Current



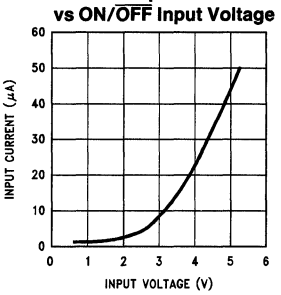
Operating Current vs Load Current



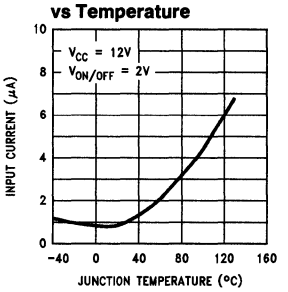
Maximum Power Dissipation



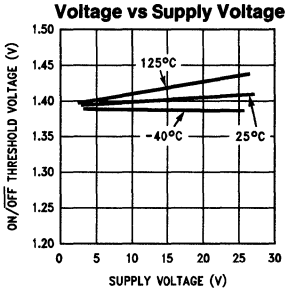
ON/$\overline{OFF}$ Input Current vs ON/$\overline{OFF}$ Input Voltage



ON/$\overline{OFF}$ Input Current vs Temperature

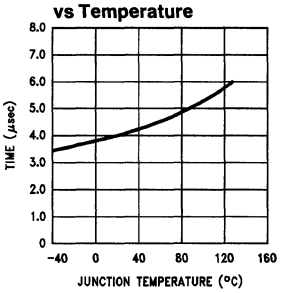


On/$\overline{OFF}$ Input Threshold Voltage vs Supply Voltage



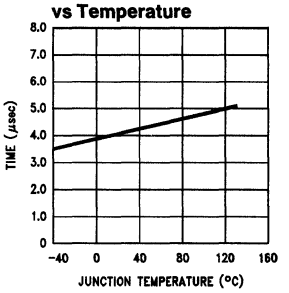
TL/H/11237–3

Turn-On Delay Time vs Temperature



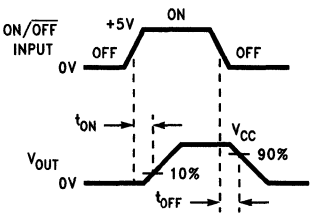
TL/H/11237–11

Turn-Off Delay Time vs Temperature



TL/H/11237–12

Delay Time Definitions



TL/H/11237–10

Application Hints

HIGH CURRENT OUTPUT

The 750 mA output is fault protected against overvoltage. If the supply voltage rises above approximately 30V, the output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. The LM1950 will survive transients and DC voltages up to 60V on the supply. The output remains off during this time, independent of the state of the input logic voltage. This protects the load. The high current output is also protected against short circuits to either ground or supply voltage. Standard thermal shutdown circuits are employed to protect the LM1950 from over heating.

FLYBACK RESPONSE

Since the LM1950 is designed to drive inductive as well as any other type of load, inductive kickback can be expected whenever the output changes state from ON to OFF (See Waveform on *Figure 1*). The driver output was left unclamped since it is often desirable in many systems to achieve a very rapid decay in the load current. In applications where this is not true, such as in *Figure 2*, a simple external diode clamp will suffice. In this application, the integrated current in the inductive load is controlled by varying the duty cycle of the input to the drive IC. This technique achieves response characteristics that are desirable for certain automotive transmission solenoids, for example.

For applications requiring a rapid controlled decay in the solenoid current, such as fuel injector drivers, an external zener and diode can be used as in *Figure 3*. The voltage rating of the zener should be such that it breaks down before the output of the LM1950. The minimum output breakdown voltage of the IC output is rated at −54V with respect to the supply voltage.

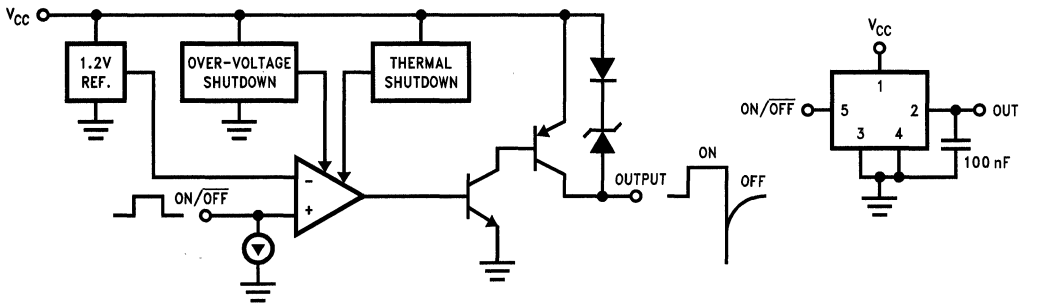
The LM1950 can be used alone as a simple relay or solenoid driver where a rapid decay of the load current is desired, but the exact rate of decay is not critical to the system. If the output is unclamped as in *Figure 1*, and the load is inductive enough, the negative flyback transient will cause the output of the IC to breakdown and behave similarly to a zener clamp. Relying upon the IC breakdown is practical and will not damage or degrade the IC in any way. There are two considerations that must be accounted for when the driver is operated in this mode. The IC breakdown voltage is process and lot dependent. Output clamp voltages ranging from −40V to −120V (with V_{CC} supply of 14V) will be encountered over time on different devices. This is not at all critical in most applications. An important consideration, however, is the additional heat dissipated in the IC as a result. This must be added to normal device dissipation when considering junction temperatures and heat sinking requirements. Worst case for the additional dissipation can be approximated as:

$$\text{Additional } P_D = I^2 \times L \times f(\text{Watts})$$

Where: I = Peak Solenoid Current (Amps)
L = Solenoid Inductance (Henries)
f = Maximum Frequency Input Signal (Hz)

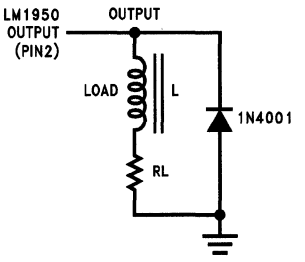
For solenoids where the inductance is less than ten millihenries, the additional power dissipation can be ignored. Overshoot, undershoot, and ringing can occur on certain loads. The simple solution is to lower the Q of the load by the addition of a resistor in parallel or series with the load. A value that draws one tenth of the current or DC voltage of the load is usually sufficient.

For frequency stability of the switch, a 0.1 μF or larger output bypass capacitor is required.



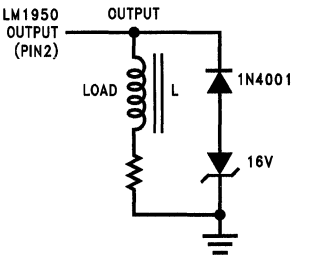
TL/H/11237–4

FIGURE 1



TL/H/11237–5

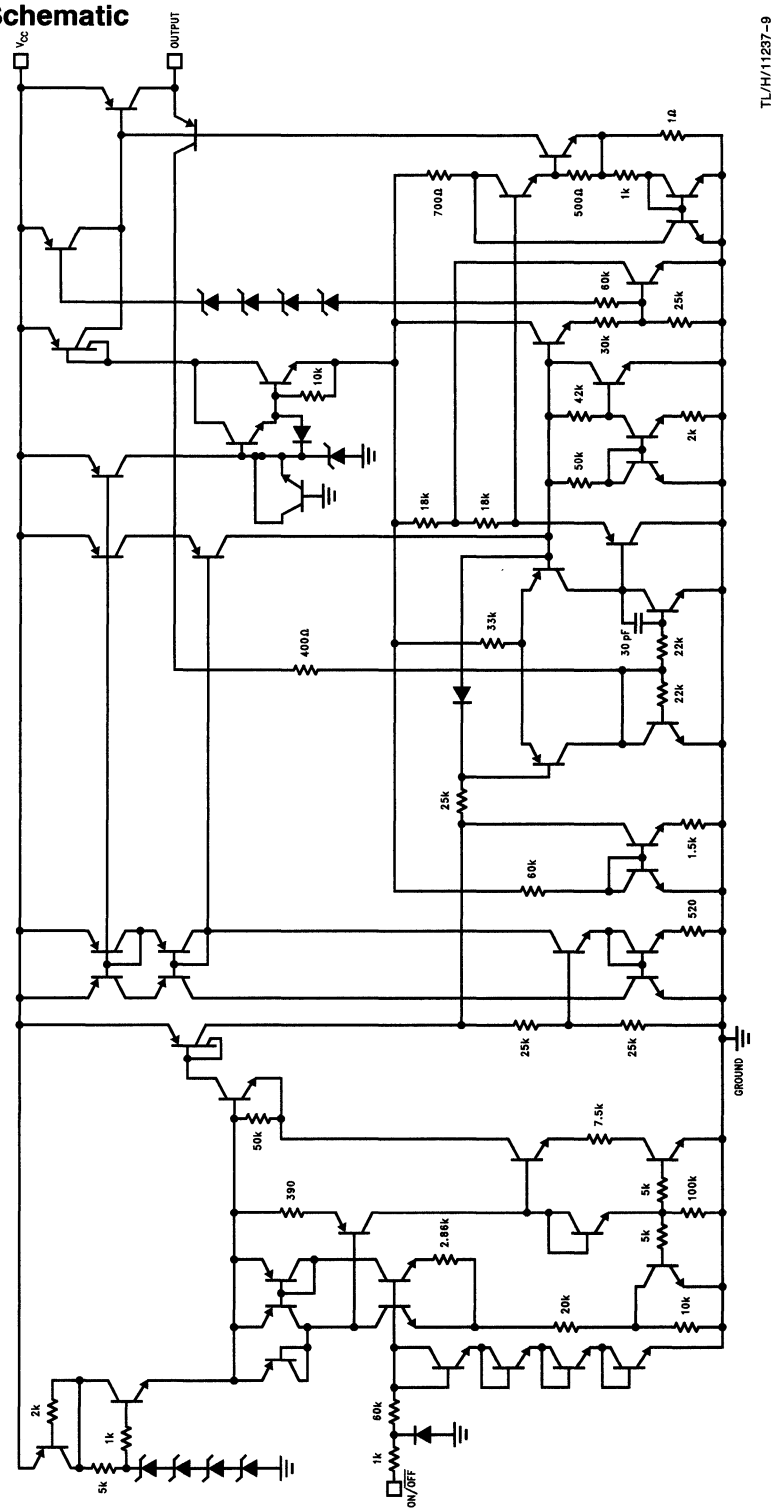
FIGURE 2. Diode Clamp



TL/H/11237–6

FIGURE 3. Zener Clamp for Rapid Controlled Current Decay

Circuit Schematic



National Semiconductor

LM1951 Solid State 1 Amp Switch

General Description

The LM1951 is a high current, high voltage, high side (PNP) switch with a built-in error detection circuit.

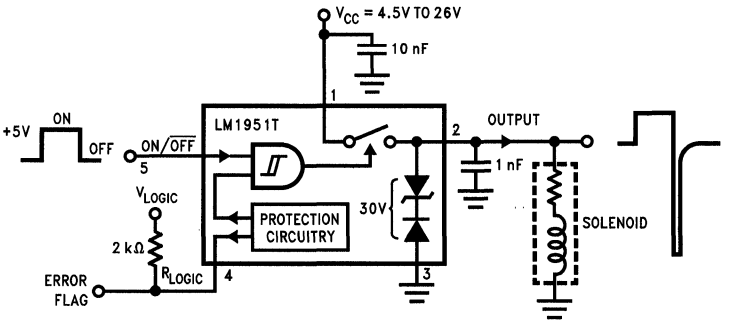
The LM1951 is guaranteed to deliver 1 Amp output current and is capable of withstanding up to ±85V transients. The built-in error detection provides an error flag output under the following fault conditions: output short to ground or supply, open load, current limit, overvoltage or thermal shutdown. The LM1951 will drive all types of resistive or inductive loads. The output has a built-in negative voltage clamp (≈ −30V) to provide a quick energy discharge path for inductive loads. The LM1951 features TTL and CMOS compatible logic input with hysteresis. Switching times, both turn on and turn off, are 2 μs (C_{load} < 0.005 μF). In addition, its quiescent current in the OFF state is typically less than 0.1 μA at room temperature and less than 10 μA over the entire operating temperature and voltage range.

The LM1951 features make it well suited for industrial and automotive applications.

Features

- 0.1 μA typical quiescent current (OFF state)
- 1 Amp output current guaranteed
- ±85V transient protection
- Reverse voltage protection
- Negative output voltage clamp
- Error flag output
- Internal overvoltage shutdown
- Internal thermal shutdown
- Short circuit proof
- High speed switching (up to 50 kHz)
- Inductive or resistive loads
- Low ON resistance (1Ω maximum)
- TTL, CMOS compatible input with hysteresis
- Plastic TO-220 5-lead package
- ESD protected
- 4.5V to 26V operation

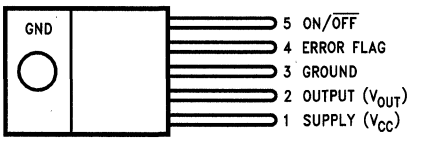
Typical Application Circuit and Connection Diagram



TL/H/9133–1

V_{IN}	Output
0	OFF
1	ON

TO-220, 5-Lead



TL/H/9133–2

Front View
Order Number LM1951T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- Operational Voltage: 26 V_{DC}
- Sustained Voltage: $-40\ V_{DC} \geq V_{CC} \leq 85\ V_{DC}$
- Transient Voltage Protection: ±85V
  (τ = 100 ms, 1% Duty Cycle, $R_S \geq 10\Omega$)
- Pins 4, 5: 26 V_{DC}

Power Dissipation (Note 1)	Internally Limited
Load Inductance	1H
Operating Temperature Range (T_A)	−40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Tolerance (Note 4):	2000V

Electrical Characteristics

V_{CC} = 12V, I_{out} = 500 mA, C_{out} = 0.001 µF, T_A = 25°C unless otherwise specified

Parameter	Conditions		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Supply Voltage, V_{CC}				4.5		V_{min}
Operational				26		V_{max}
Transient	τ = 100 ms, 1% Duty Cycle, $R_{CC} \geq 10\Omega$			−85		V
				85		V
Supply Current	I_{out} = 0 mA, $V_{ON/\overline{OFF}}$ = 0.8V		0.1	10	100	μA_{max}
	I_{out} = 250 mA, $V_{ON/\overline{OFF}}$ = 2.0V		260	270		mA_{max}
	I_{out} = 600 mA, $V_{ON/\overline{OFF}}$ = 2.0V		630	650		mA_{max}
	I_{out} = 1A, $V_{ON/\overline{OFF}}$ = 2.0V		1.06	1.2		A_{max}
Voltage Drop ($V_{CC} - V_{OUT}$)	I_{out} = 600 mA, $V_{ON/\overline{OFF}}$ = 2.0V		400	600		mV_{max}
	I_{out} = 1A, $V_{ON/\overline{OFF}}$ = 2.0V		0.7	1.0		V_{max}
Short Circuit Current	V_{OUT} = 0V, $V_{ON/\overline{OFF}}$ = 2V		1.3	1.0		A_{min}
				2.5		A_{max}
Input Threshold, Pin 5	4.5V ≤ V_{CC} ≤ 26V	Turn ON	1.4	2.0	2.0	V_{max}
		Turn OFF	1.2	0.8	0.8	V_{min}
Input Current, Pin 5	0.8V ≤ $V_{ON/\overline{OFF}}$ ≤ 5.5V		25	50		μA_{max}
				10		μA_{min}
Output Clamp	I_{out} ≤ 600 mA		−30	−40		V_{min}
				−24		V_{max}
Delay t_d, ON	R_{load} = 20Ω, C_{load} = 0.001 µF		1	3		μs_{max}
Time t_d, OFF			1	3		μs_{max}
Rise Time			1	3		μs_{max}
Fall Time			1	3		μs_{max}
Error Flag Characteristics: Output Voltage	Error Condition, Pin 4 Low, Sinking 10 mA		0.3	0.8		V_{max}
Sink Current	Error Condition, Pin 4 = 0.3V		10	3		mA_{min}
Output Leakage Current	No Error, Pin 4 = 26V		0.01	1		μA_{max}
Response Time	V_{LOGIC} = 5V, R_{LOGIC} = 2 kΩ, C_{LOGIC} = 0 µF		1			µs

Note 1: Thermal resistance junction-to-case is 3°C/W. Thermal resistance case-to-ambient is 50°C/W.

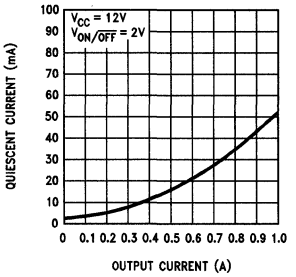
Note 2: Tested Limits are guaranteed and 100% production tested.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

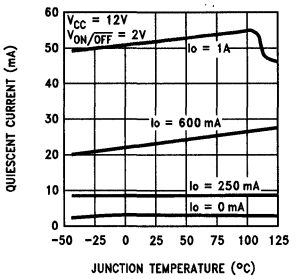
Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

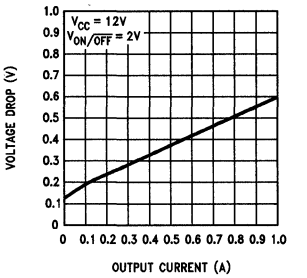
Quiescent Current



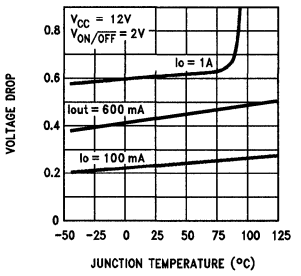
Quiescent Current



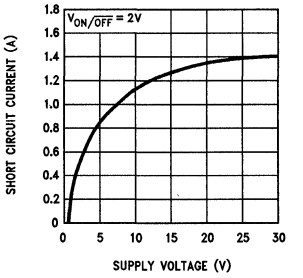
Voltage Drop



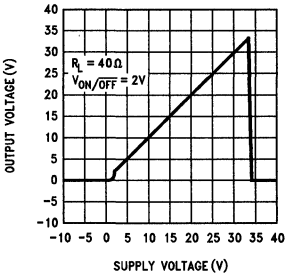
Voltage Drop



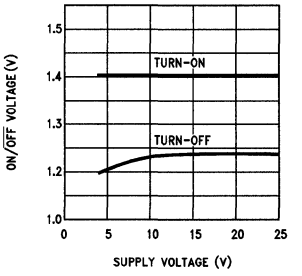
Short Circuit Current



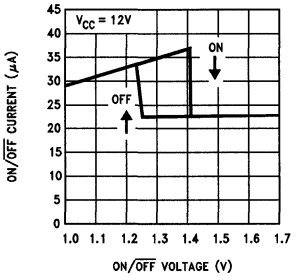
High Voltage Behavior



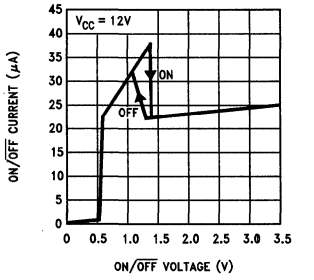
ON/$\overline{\text{OFF}}$ Threshold (Pin 5)



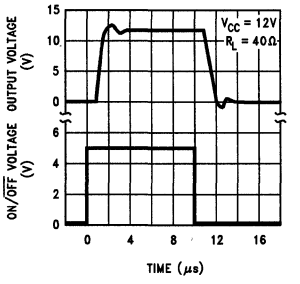
ON/$\overline{\text{OFF}}$ Current (Pin 5)



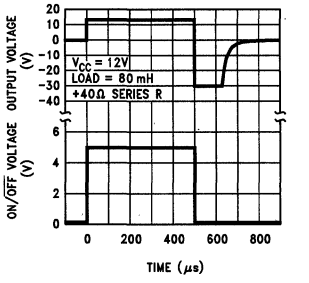
ON/$\overline{\text{OFF}}$ Current (Pin 5)



Output Voltage
Resistive Load

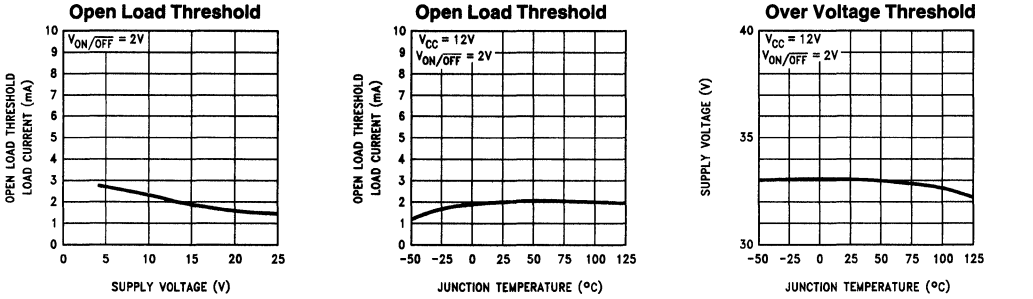


Output Voltage
Inductive Load



TL/H/9133–3

Error Flag Output Characteristics



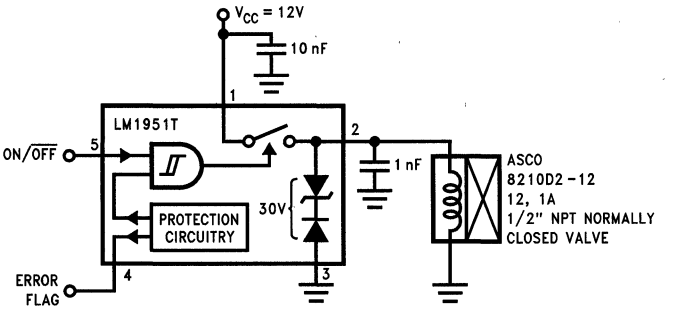
TL/H/9133–13

Truth Table

Fault Condition	$V_{ON/\overline{OFF}}$*	V_{out}	Error Flag
Normal	L	L	H
	H	H	H
Overvoltage	L	L	L
	H	L	L
Thermal Shutdown	L	L	L
	H	L	L
V_{OUT} Short to GND	L	L	H
	H	L	L
V_{OUT} Short to V_{supply}	L	H	L
	H	H	L
Open Load	L	L	H
	H	H	L
Current Limit	L	L	H
	H	H	L

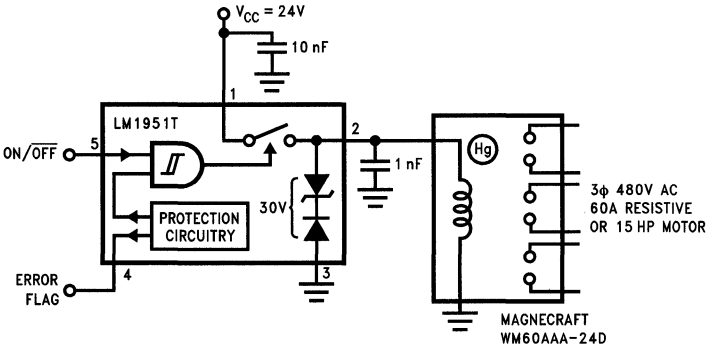
* L ≅ $0 \leq V_{ON/\overline{OFF}} \leq 0.8V$ H ≅ $2V \leq V_{ON/\overline{OFF}} \leq 26V$

Typical Applications



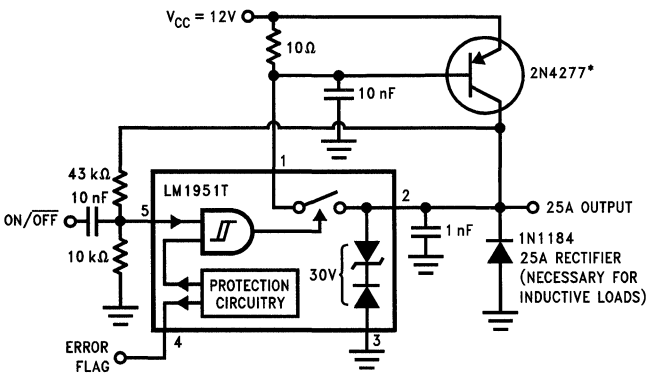
TL/H/9133–4

FIGURE 1. Solenoid Actuated Valve



TL/H/9133–5

FIGURE 2. 60A 3-Phase Mercury Displacement Relay

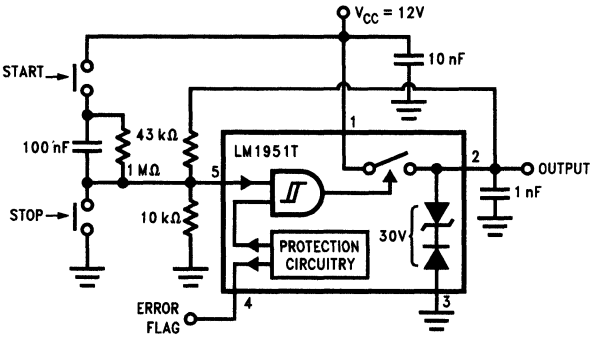


TL/H/9133–6

*Available from Germanium Power Devices, Andover, MA, Tel. (617) 475-5982

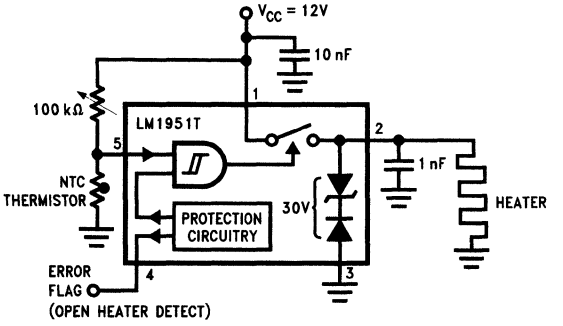
FIGURE 3. 25A Switch with Short Circuit Foldback

Typical Applications (Continued)



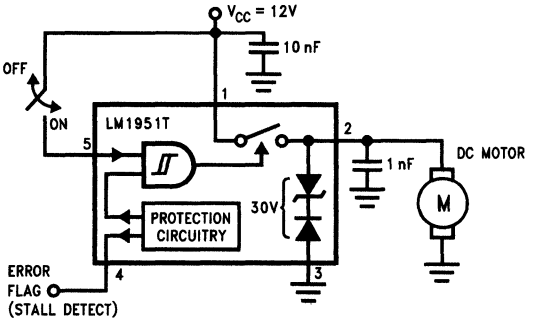
TL/H/9133–7

FIGURE 4. Latching Switch



TL/H/9133–8

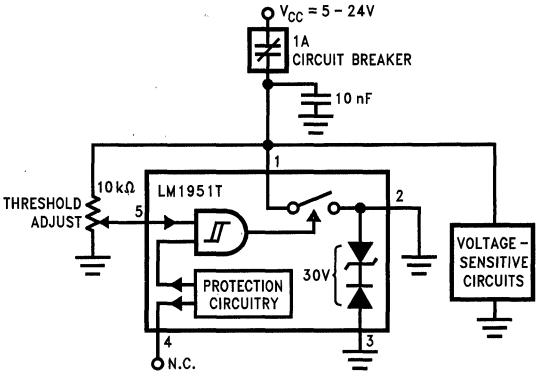
FIGURE 5. Temperature Controller with Hysteresis



TL/H/9133–9

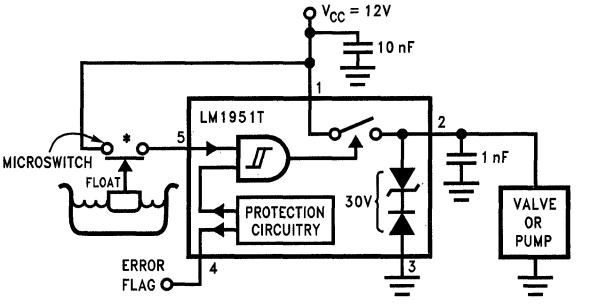
FIGURE 6. DC Motor Driver

Typical Applications (Continued)



TL/H/9133–10

FIGURE 7. Over-Voltage Crowbar



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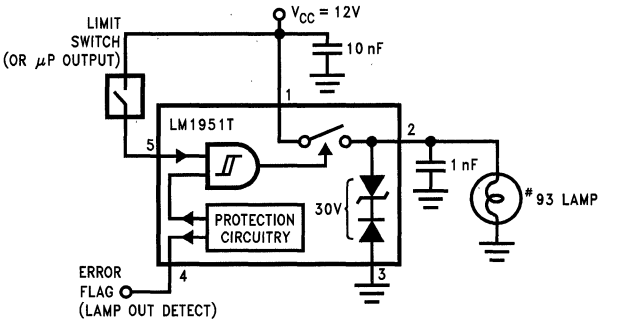
*

Operation	Switch Type
Empty	Normally Open
Fill	Normally Closed

FIGURE 8. Fluid Level Controller



TL/H/9133–12

FIGURE 9. Indicator Lamp Driver

Application Hints

When inductive loads are turned OFF, they produce a negative voltage spike. The LM1951 contains a voltage clamp that limits these spikes to approximately −30V, thus an external clamp is not necessary in most applications.

Loads with an inductance of greater than 1H, driven to full output current, may damage the clamp simply by exceeding the power capabilities of the LM1951. An LM1951 can dissipate 25W continuous at 25°C ambient when mounted on a large heatsink. If the load current is limited to 800 mA, the sustained spike from an infinitely large inductance can be handled. Sustained spikes produced by higher currents and high inductances will exceed the 25W limit.

For inductances above 1H, care should be taken to see that the output current does not exceed a value that could damage the clamp. While 800 mA is acceptable for the device running at 25°C ambient on a heatsink, derate this current for smaller heatsinks or higher ambient temperatures to limit the junction temperature to 150°C. Alternatively, an external clamp or resonating capacitor can be added to handle any combination of load inductance, load current, and device temperature. This is especially important if the output current is boosted, such as the application shown in *Figure 3*. A peak power of 750W could be developed in the internal clamp if an inductive load is switched without external clamping.

Another case where the clamp's power capability may be exceeded is when driving a solenoid. The inductance of a solenoid is greatest when energized, with the plunger pulled in. As the plunger is pulled out of the solenoid, the inductance goes down. Under certain conditions of high solenoid inductance and fast mechanical time constants, the current may actually **increase** when the solenoid is turned OFF. Since the energy stored in an inductor cannot change instantaneously, the current must increase to conserve energy when the inductance decreases. This condition is traced by observing the load current with a current probe and storage oscilloscope.

Load capacitances larger than 1 nF will slow rise and fall times. Inductive loads having a capacitive component larger than 1 nF will also exhibit overshoot. Furthermore, ringing may be evident in a combination inductive/capacitive load, or in an inductive load with supply decoupling capacitors in the range of 100 nF to 1 μF. For fast rise and fall times and minimum ringing with inductive loads, a supply decoupling capacitor of 10 nF and an output capacitor of 1 nF is recommended. These should be located as close to the IC pins as possible.

The error flag is an open collector output that pulls low under certain fault conditions. These errors include overvoltage (V_{CC} > 26V), overcurrent (I_{OUT} > 1.3A), undercurrent (I_{OUT} < 2 mA), output short circuit to ground, output short circuit to supply, and junction temperature greater than 150°C. By connecting a 2 kΩ resistor from the error flag output to a 5V supply a logic output to a microprocessor is provided.

The error flag can give seemingly false indications in a number of situations. Slewing large capacitive loads (>100 nF) can drive the LM1951 into temporary current limit, producing a momentary error indication. Incandescent lamps and DC motors require an inrush current that will also cause a temporary current limit and error indication. Large inductive loads (>50 mH) initially appear as open circuits, falsing the error flag. The error flag pulses for about 1 μs when any load is turned ON since the output is initially at ground. In microprocessor systems these false indications are easily ignored in software. In discrete logic circuits utilizing a latch at the error flag output, some filtering may be required.

An internal current sink (10 μA minimum) is connected to the input, pin 5. If this pin is left open it is guaranteed to pull low, switching the LM1951 OFF. This characteristic is important under certain fault conditions such as when the control line fails open cirucit.

Although the input threshold has hysteresis, the switch points are derived from a very stable band-gap reference. In many applications, such as *Figures 5* and *7*, the LM1951 input can replace an extenal reference and comparator.

The input (pin 5) is clamped at −0.7V and includes a series resistance of approximately 30 kΩ. This pin tolerates negative inputs of up to 1 mA without affecting the performance of the chip.

National Semiconductor

LM1964 Sensor Interface Amplifier

General Description

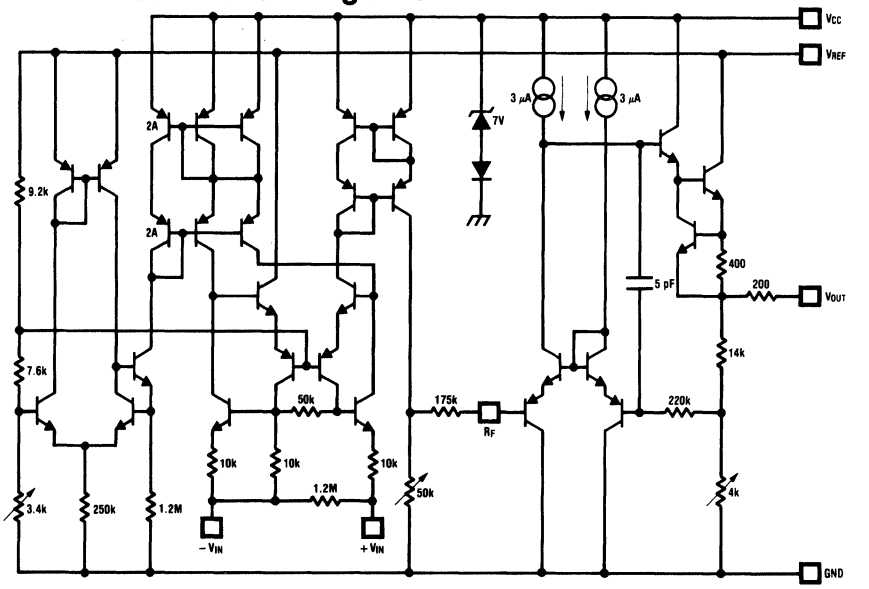
The LM1964 is a precision differential amplifier specifically designed for operation in the automotive environment. Gain accuracy is guaranteed over the entire automotive temperature range (−40°C to +125°C) and is factory trimmed prior to package assembly. The input circuitry has been specifically designed to reject common-mode signals as much as 3V below ground on a single positive power supply. This facilitates the use of sensors which are grounded at the engine block while the LM1964 itself is grounded at chassis potential. An external capacitor sets the maximum operating frequency of the amplifier, thereby filtering high frequency transients. Both inputs are protected against accidental shorting to the battery and against load dump transients. The input impedance is typically 1 MΩ.

The output op amp is capable of driving capacitive loads and is fully protected. Also, internal circuitry has been provided to detect open circuit conditions on either or both inputs and force the output to a "home" position (a ratio of the external reference voltage).

Features

- Normal circuit operation guaranteed with inputs up to 3V below ground on a single supply
- Gain factory trimmed and guaranteed over temperature (±3% of full-scale from −40°C to +125°C)
- Low power consumption (typically 1 mA)
- Fully protected inputs
- Input open circuit detection
- Operation guaranteed over the entire automotive temperature range (−40°C to +125°C)
- Single supply operation

Schematic and Connection Diagrams



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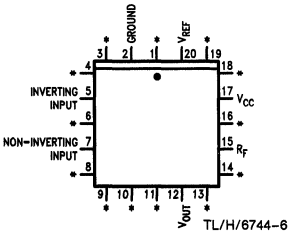
Plastic Chip Carrier Package



TL/H/6744–6

Top View

Order Number LM1964V
See NS Package Number V20A

*Pins 1, 3, 4, 6, 8, 9, 10, 11, 13, 14, 16, 18, 19 are trim pins and should be left floating.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage (RV_{CC} = 15 kΩ)	±60V
V_{REF} Supply Voltage	−0.3V to +6V
DC Input Voltage (Either Input)	−3V to +16V
Input Transients (Note 1)	±60V
Power Dissipation (see Note 6)	1350 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12V, V_{REF} = 5V, T_A = 25°C unless otherwise noted

Parameter	Conditions	(Note 2)			(Note 3)			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	V_{DIF} = 0.5V −1V ≤ V_{CM} ≤ +1V	4.41	4.50	4.59				V/V
	V_{DIF} = 0.5V, −40°C ≤ T_A ≤ 125°C −3V ≤ V_{CM} ≤ +1V				4.36	4.50	4.64	V/V
Gain Error (Note 5)	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	−2	0	2				%/FS
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C				−3	0	3	%/FS
Differential Input Resistance	o ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	1.00	1.20					MΩ
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A + 125°C				0.70	1.20		MΩ
Non-Inverting Input Bias Current	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V		0.3	1.0				μA
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C					0.3	1.5	μA
Inverting Input Bias Current	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V		45	100				μA
	0V ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C					45	150	μA
V_{CC} Supply Current	V_{CC} = 12V, RV_{CC} = 15k		300	500				μA
V_{REF} Supply Current	4.75V ≤ V_{REF} ≤ 5.5V		0.5	1.0				mA
Common-Mode Voltage Range (Note 4)	−40°C ≤ T_A ≤ +125°C	−1		1	−3		1	V
DC Common-Mode Rejection Ratio	Input Referred −1V ≤ V_{CM} ≤ +1V V_{DIF} = 0.5V	50	60					dB
Open Circuit Output Voltage	One or Both Inputs Open, −1V ≤ V_{CM} ≤ +1V	0.371	0.397	0.423				XV_{REF}
	−3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C				0.365	0.397	0.429	XV_{REF}
Short Circuit Output Current	Output Grounded	1.0	2.7	5.0				mA
V_{CC} Power Supply Rejection Ratio	V_{CC} = 12V, RV_{CC} = 15K V_{DIF} = 0.5V	50	65					dB
V_{REF} Power Supply Rejection Ratio	V_{REF} = 5 V_{DC} V_{DIF} = 0.5V	60	74					dB

Note 1: This test is performed with a 1000Ω source impedance.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: These parameters will be guaranteed but not 100% production tested.

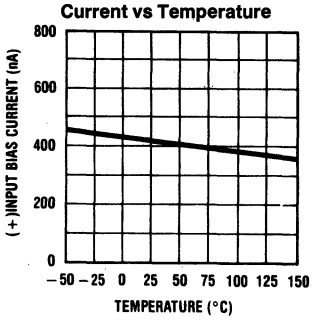
Note 4: The LM1964 has been designed to common-mode to −3V, but production testing is only performed at ±1V.

Note 5: Gain error is given as a percent of full-scale. Full-scale is defined as 1V at the input and 4.5V at the output.

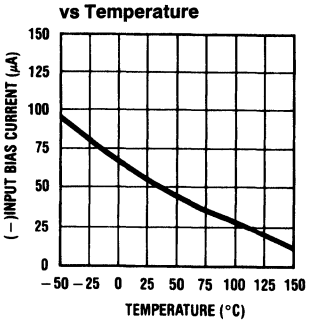
Note 6: For operation in ambient temperatures above 25°C the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 93°C/W junction to ambient.

Typical Performance Characteristics

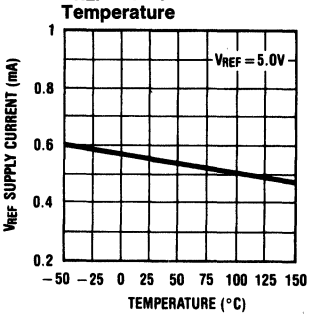
Non-Inverting Input Bias Current vs Temperature



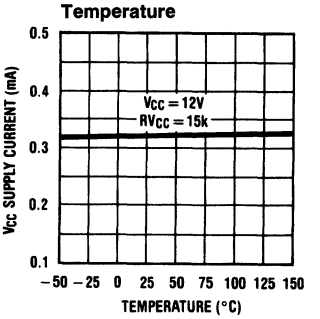
Inverting Input Bias Current vs Temperature



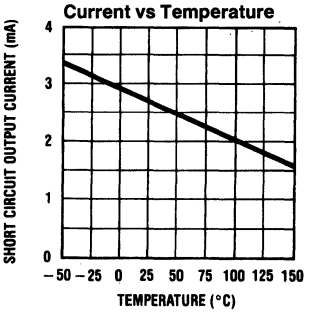
V_{REF} Supply Current vs Temperature



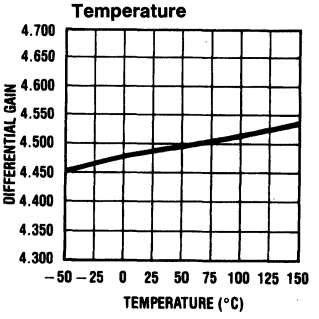
V_{CC} Supply Current vs Temperature



Short Circuit Output Current vs Temperature



Differential Gain vs Temperature



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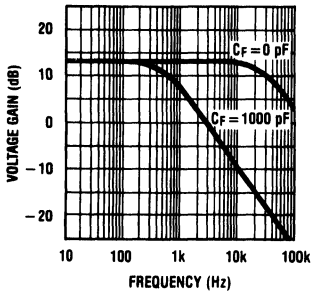
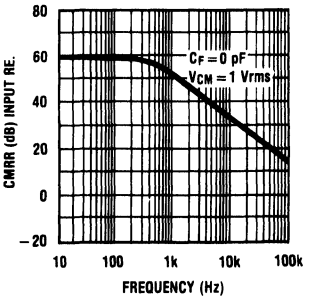
Typical Performance Characteristics (Continued)

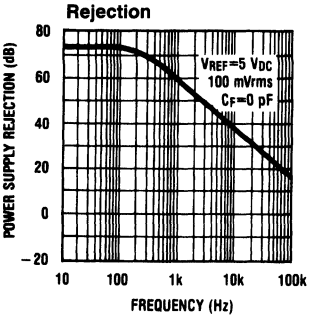
Voltage Gain vs Frequency



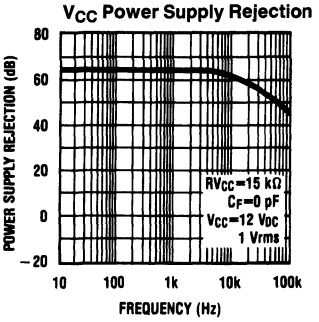
CMRR vs Frequency



V_{REF} Power Supply Rejection



V_{CC} Power Supply Rejection



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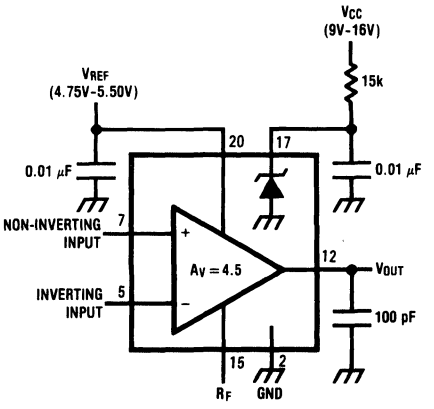
Test Circuit



TL/H/6744–5

National Semiconductor

LMD18400
Quad High Side Driver

General Description

The LMD18400 is a fully protected quad high side driver. It contains four common-drain DMOS N-channel power switches, each capable of switching a continuous 1 Amp load (>3 Amps transient) to a common positive power supply. The switches are fully protected from excessive voltage, current and temperature. An instantaneous power sensing circuit calculates the product of the voltage across and the current through each DMOS switch and limits the power to a safe level. The device can be disabled to produce a "sleep" condition reducing the supply current to less than 10 μA. Separate ON/OFF control of each switch is provided through standard LSTLL/CMOS logic compatible inputs.

A MICROWIRE™ compatible serial data interface is built in to provide extensive diagnostic information. This information includes switch status readback, output load fault conditions and thermal and overvoltage shutdown status. There are also two direct-output error flags to provide an immediate indication of a general system fault and an indication of excessive operating temperature.

The LMD18400 is packaged in a special power dissipating leadframe that reduces the junction to case thermal resistance to approximately 20°C/W.

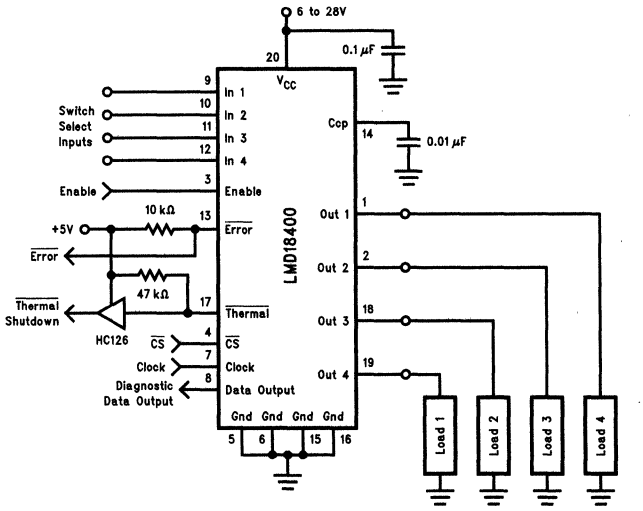
Features

- Four independent outputs with >3A peak, 1A continuous current capability
- 1.3Ω maximum ON resistance over temperature
- True instantaneous power limit for each switch
- High survival voltage (60 V_{DC}, 80V transient)
- Shorted load (to ground and supply) protection
- Overvoltage shutdown at V_{CC} > 35V
- LS TTL/CMOS compatible logic inputs and outputs
- <10 μA supply current in "sleep" mode
- −5V output clamp for discharging inductive loads
- Serial data interface for 11 diagnostic checks:
  - — Switch ON/OFF status
  - — Open or shorted load
  - — Operating temperature
  - — Excessive supply voltage
- Two direct-output error flags

Applications

- Relay and solenoid drivers
- High impedance automotive fuel injector drivers
- Lamp drivers
- Power supply switching
- Motor drivers

Typical Application



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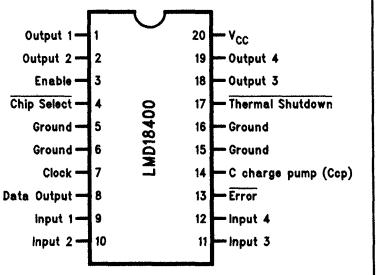
Connection Diagram



TL/H/11026–2

Order Number LMD18400N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Survival Voltage (Pin 20)	
Transient (t = 10 ms)	80V
Continuous	−0.5V to +60V
Output Transient Current (Each Switch)	3.75A
Output Transient Current (Total, All Switches)	6A
Output Steady State Current (Each Switch)	1A
Logic Input Voltage (Pins 3, 9, 10, 11, 12)	−0.3V to +16V
Logic Input Voltage (Pins 4, 7)	−0.3V to +6V
Error Flag Voltage	16V
ESD Susceptibility (Note 2)	2000V
Power Dissipation (Note 3)	5W
	Internally Limited
Junction Temperature ($T_{J_{Max}}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

Operating Ratings (Note 1)

Ambient Temperature Range (T_A)	−40°C to +125°C
Supply Voltage Range	6V to 28V

Electrical Characteristics

V_{CC} = 12V, C_{CP} = 0.01 μFd, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_J = +25°C.

Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units (Limit)
DC CHARACTERISTICS				
Supply Current	Enable Input = 0V	0.04	10	μA (Max)
	Enable Input = 5V, Inputs = 0V	7.5	15	mA (Max)
	Enable Input = 5V, Inputs = 5V Open Loads	7.5	15	mA (Max)
Output Leakage	Enable Input = 0V, Inputs = 0V (Pins 1, 2, 18, 19)	0.01	10	μA (Max)
Rds ON	I_{OUT} = 1A, (Note 6)	0.8	**1.3**	Ω (Max)
Short Circuit Current	V_{CC} = 12V, (Note 6)	1.2	0.8	A (Min)
	V_{CC} = 6V, (Note 6)	2.4		A
	V_{CC} = 28V, (Note 6)	0.6		A
Maximum Output Current	$V_{CC} - V_O$ = 4V, (Note 6)	3.75		A
Load Error Threshold Voltage	Pins 1, 2, 18, 19	4.1		V
Open Load Detection Current	Pins 1, 2, 18, 19	150		μA
Negative Clamp Output Voltage	I_O = 1A, (Note 6)	−5		V
Overvoltage Shutdown Threshold		35	40	V (Max)
Overvoltage Shutdown Hysteresis		0.75		V
Error Output Leakage Current	$V_{Pin\ 13}$ = 12V	0.001	10	μA (Max)
Thermal Warning Temperature	$V_{Pin\ 13}$ < 0.8V	145		°C
Thermal Shutdown Temperature	$V_{Pin\ 17}$ < 0.8V	170		°C

Electrical Characteristics V_{CC} = 12V, C_{CP} = 0.01 µF, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for T_A = T_J = +25°C. (Continued)

Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units (Limit)
AC CHARACTERISTICS				
Switch Turn-On Delay ($t_{d(ON)}$)	Enable (Pin 3) = 5V, I_{OUT} = 1A	5	10	µs (Max)
Switch Turn-On Rise Time (t_{ON})	I_{OUT} = 1A	7	15	µs (Max)
Switch Turn-Off Delay (t_{dOFF})	Enable (Pin 3) = 5V, I_{OUT} = 1A	0.5	2	µs (Max)
Switch Turn-Off Fall Time (t_{OFF})	I_{OUT} = 1A	0.15	1	µs (Max)
Enable Time (t_{EN})	Measured with Switch 1, Pin 9 = 5V	30	50	µs (Max)
Error Reporting Delay (t_{Error})	Enable (Pin 3) = 5V, Switch 1 Load Opened	75	150	µs (Max)
Data Setup Time (t_{DS})	C_L = 30 pF	200	500	ns (Min)
TRI-STATE® Control (t_{1H}, t_{OH})	Pin 8, Hi-Z Enable Time	2		µs
Data Clock Frequency		3	1	MHz (Max)
DIGITAL CHARACTERISTICS				
Logic "1" Input Voltage	Pins 3, 4, 7, 9, 10, 11, 12		**2.0**	V (Min)
Logic "0" Input Voltage	Pins 3, 4, 7, 9, 10, 11, 12		**0.8**	V (Max)
Logic "1" Input Current	Pins 4, 7	0.001	**1**	µA (Max)
Logic "0" Input Current	Pins 4, 7	−0.001	**−1**	µA (Max)
TRI-STATE Output Current	Pin 8, Pin 4 = 5V Pin 8 = 0V	0.05 −0.05	10 −10	µA (Max) µA (Max)
Enable Input Current	Pin 3 = 2.4V	12	**25**	µA (Max)
Channel Input Resistance	Pins 9, 10, 11, 12	75	**25**	kΩ (Min)
Error Output Sink Current	Pin 13 = 0.8V	4	**1.6**	mA (Min)
Logic "1" Output Voltage	Pin 8 I_{OUT} = −360 µA I_{OUT} = −10 µA I_{OUT} = −10 µA	 4.4 5.1	 **2.4** **4.5** **5.5**	 V (Min) V (Min) V (Max)
Logic "0" Output Voltage	Pin 8 I_{OUT} = 100 µA		**0.4**	V (Max)
Thermal Shutdown Output Source Current	Pin 17 = 2.4V	5	3	µA (Min)
Thermal Shutdown Output Sink Current	Pin 17 = 0.8V	360	250	µA (Min)

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model; 100 pF discharge through a 1.5 kΩ resistor. All pins except pins 8 and 13 which are protected to 1000V and pins 1, 2, 18 and 19 which are protected to 500V.

Note 3: The maximum power dissipation is a function of $T_{J_{Max}}$, θ_{JA}, and T_A and is limited by thermal shutdown. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J_{Max}} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will eventually go into thermal shutdown. For the LMD18400 the junction-to-ambient thermal resistance, θ_{JA}, is 60°C/W. With sufficient heatsinking the maximum continuous power dissipation for the package will be, $I_{DC_{Max}}{}^2 \times R_{ON(Max)} \times 4$ switches ($1A^2 \times 1.3\Omega \times 4 = 5.2W$).

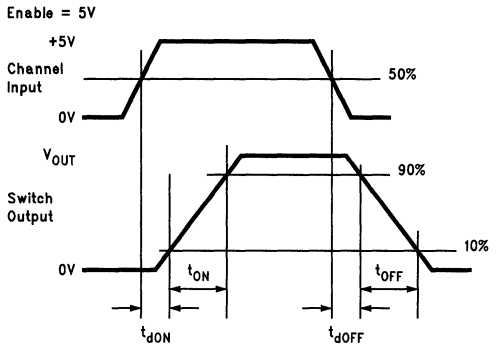
Note 4: Typical values are at $T_J = +25°C$ and represent the most likely parametric norm.

Note 5: All limits are 100% production tested at +25°C. Limits at temperature extremes are guaranteed through correlation and accepted Statistical Quality Control (SQC) methods.

Note 6: Pulse Testing techniques used. Pulse width is < 5 ms with a duty cycle < 1 %.

Timing Specification Definitions

Switching Turn ON/OFF



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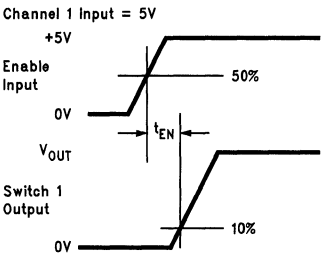
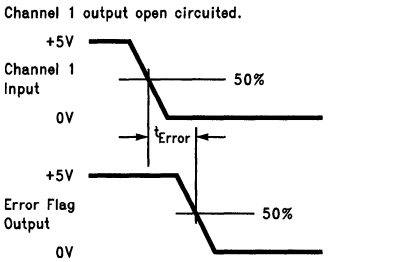
Enable Turn-ON



TL/H/11026–4

Error Reporting Delay



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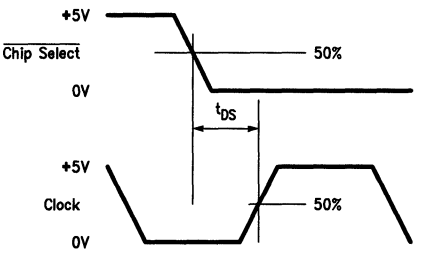
Data Setup Time



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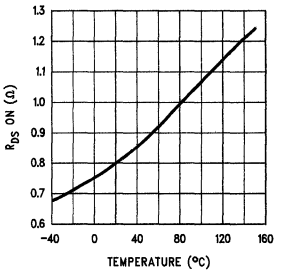
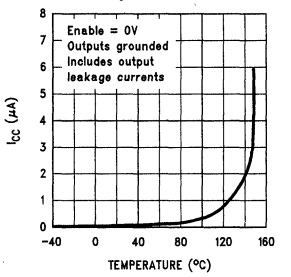
Typical Performance Characteristics

For all curves, V_{CC} = 12V, Temperature is the junction temperature unless otherwise noted.

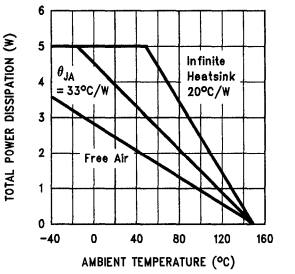
Switch ON Resistance vs Temperature



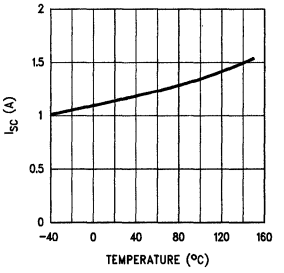
"Sleep" Mode Supply Current vs Temperature



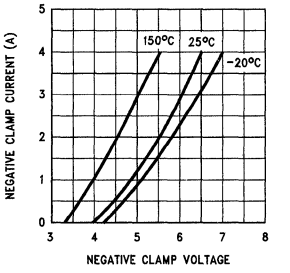
Maximum Power Dissipation vs Ambient Temperature



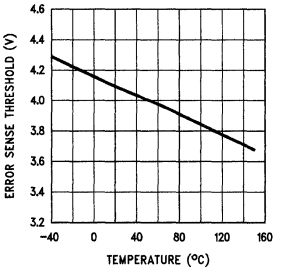
Short Circuit Current vs Temperature



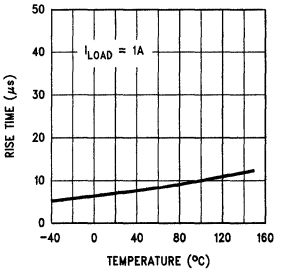
Clamp Characteristics vs Temperature



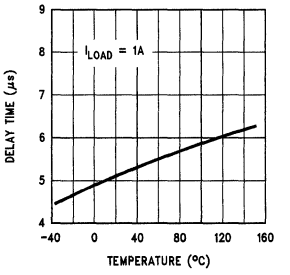
Error Sense Threshold Voltage vs Temperature



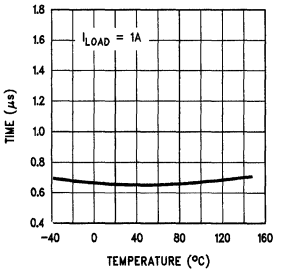
Turn ON Rise Time vs Temperature



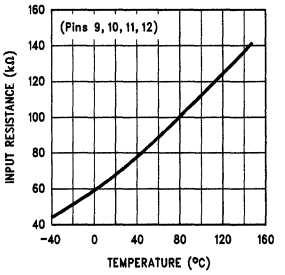
Turn ON Delay Time vs Temperature



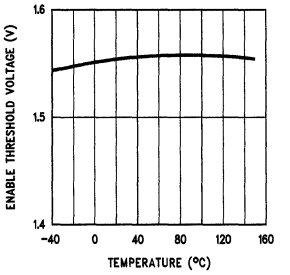
Turn OFF Time vs Temperature



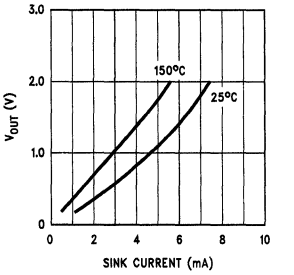
Switch Select Logic Input Resistance vs Temperature



Enable Threshold Voltage vs Temperature



Error Output Voltage vs Sink Current



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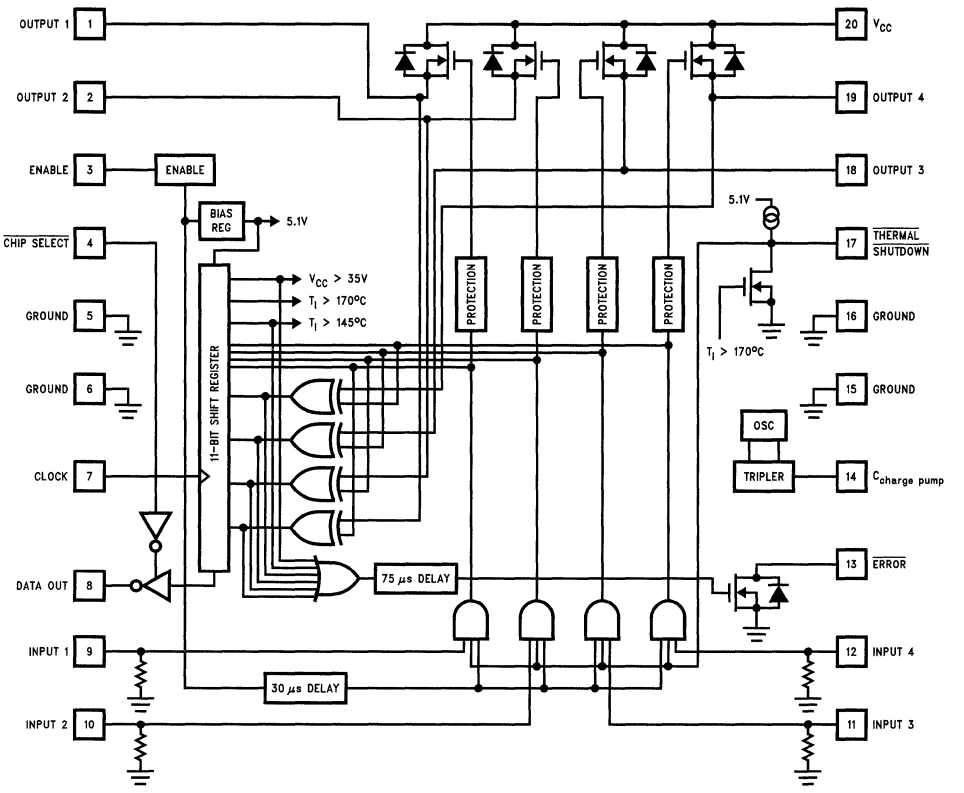
Functional Block Diagram



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Truth Table

Enable Input (Pin 3)	Chip Select Input (Pin 4)	Switch Control Input (Pins 8, 9, 10, 11)	Error Output (Pin 13)	Thermal SD Output (Pin 17)	Conditions
0	X	X	0	0	"Sleep" Mode, $I_{Supply} < 10\ \mu A$
1	X	0	1	1	Selected Switch is OFF
1	X	1	1	1	Selected Switch is ON, Normal Operation
1	X	0	0	1	Switch is OFF but: a. Load is Open Circuited, or b. Load is Shorted to V_{CC}, or c. $T_J > +145°C$, or d. $V_{CC} > +35V$
1	X	1	0	1	Switch is ON, but; a. Load is Shorted to Ground, or b. Switch is in Power Limit, or c. $T_J > +145°C$, or d. $V_{CC} > +35V$ and Switch is Actually OFF
1	X	1	0	0	$T_J > +170°C$, All Switches are OFF
1	1	X	X	X	Data Output Pin is TRI-STATE
1	0	X	X	X	Data Output Pin is Enabled and Ready to Output Diagnostic Information

Applications Information

BASIC OPERATION

High-side drivers are used extensively in automotive and industrial applications to switch power to ground referred loads. The major advantage of using high-side drive, as opposed to low-side drive, is to protect the load from being energized in the event that the load drive wire is inadvertently shorted to ground as shown in *Figure 1*. A high-side driver can sense a shorted condition and open the power switch to disable the load and eliminate the excessive current drain on the power supply. The LMD18400 can control and protect up to four separate ground referenced loads.

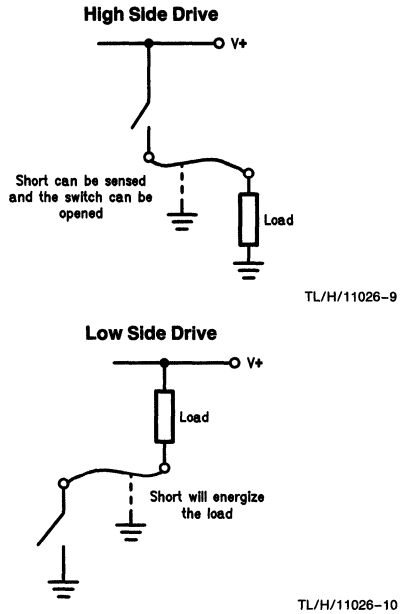

FIGURE 1. High-Side vs Low-Side Drive

The LMD18400 combines low voltage CMOS logic control circuitry with a high voltage DMOS process. Each DMOS power switch has an individual ON/OFF control input. When commanded ON, the output of the switch will connect the load to the V_{CC} supply through a maximum resistance of 1.3Ω (the ON resistance of the DMOS switch). The voltage applied to the load will depend upon the load current and the designed current capability of the LMD18400. When a switch is commanded OFF, the load will be disconnected from the supply except for a small leakage current of typically less than 0.01 μA.

The LMD18400 can be continually connected to a live power source, a car battery for example, while drawing less than 10 μA from the power source when put into a "sleep" condition. This "sleep" mode is enacted by taking the Enable Input (pin 3) low. During this mode the supply current for the device is typically only 0.04 μA. Special low current consumption standby circuitry is used to hold the DMOS switches OFF to eliminate the possibility of supply voltage transients from turning on any of the loads (a common problem with MOS power devices). When in the "sleep" mode, all diagnostic and logic circuitry is inactive. When the Enable Input is taken to a logic 1, the switches become "armed" and ready to respond to their control input after a short, 30 μs, enable delay time. This delay interval prevents the switches from transient turn-on. *Figure 2* shows the switch control logic.

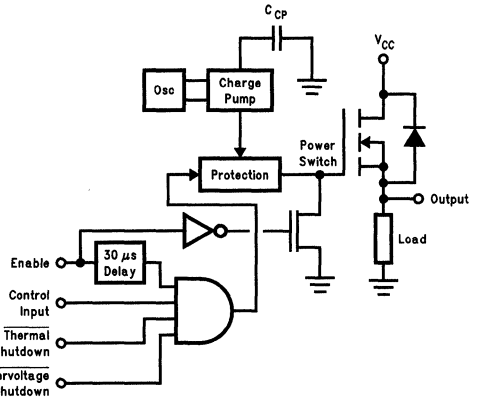

FIGURE 2. Control Logic for Each Power Switch

Each DMOS switch is turned ON when its gate is driven approximately 3.5V more positive than its source voltage. Because the source of the switch is the output terminal to the load it can be taken to a voltage very near the V_{CC} supply potential. To ensure that there is sufficient voltage available to drive the gates of the DMOS device a charge pump circuit is built in. This circuit is controlled by an internal 300 kHz oscillator and using an external 10 nF capacitor connected from pin 14 to ground generates a voltage that is approximately 20V greater than the V_{CC} supply voltage. This provides sufficient gate voltage drive for each of the switches which is applied under command of standard 5V logic input levels.

The turn-on time for each switch is approximately 12 μs when driving a 1A load current. This relatively slow switching time is beneficial in minimizing electromagnetic interference (EMI) related problems created from switching high current levels.

Applications Information (Continued)

PROTECTION CIRCUITRY

The LMD18400 has extensive protection circuitry built in. With any power device, protection against excessive voltage, current and temperature conditions is essential. To achieve a "fail-safe" system implementation, the loads are deactivated automatically by the LMD18400 in the event of any detected overvoltage or over-temperature fault conditions.

Voltage Protection

The V_{CC} supply can range from $-0.5V$ to $+60$ V_{DC} without any damage to the LMD18400. The CMOS logic circuitry is biased from an internal 5.1V regulator which protects these lower voltage transistors from the higher V_{CC} potentials. In order to protect the loads connected to the switch outputs however, an overvoltage shutdown circuit is employed. Should the V_{CC} potential exceed 35V all of the switches are turned OFF thereby disconnecting the loads. This 35V threshold has 750 mV of hysteresis to prevent potential oscillations.

Additionally, there is an undervoltage lockout feature built in. With V_{CC} less than 5V it becomes uncertain whether the logic circuitry can hold the switches in their commanded state. To avoid this uncertainty, all of the switches are turned OFF when V_{CC} drops below approximately 5V. *Figure 3* illustrates the shutoff of an output during a 0V to 80V V_{CC} supply transient.

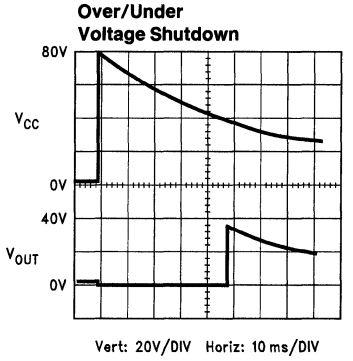

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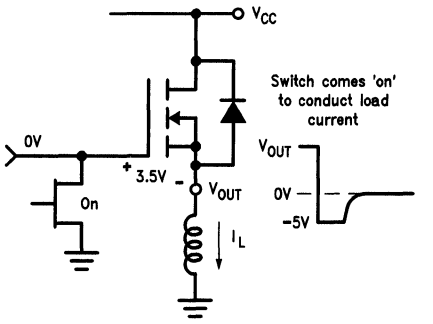
FIGURE 3. Overvoltage/Undervoltage Shutdown

The LMD18400 has been designed to drive all types of loads. When driving a ground referenced inductive load such as a relay or solenoid, the voltage across the load will reverse in polarity as the field in the inductor collapses when the power switch is turned OFF. This will pull the output pin of the LMD18400 below ground. This negative transient voltage is clamped at approximately $-5V$ to protect the IC. This clamping action is not done with diodes but rather the power DMOS switch turning back on momentarily to conduct the inductor current as it de-energizes as shown in *Figure 4.*



TL/H/11026–13

FIGURE 4. Turn-OFF Conditions with an Inductive Load

When the output inductance produces a negative voltage, the gate of the DMOS transistor is clamped at 0V. At $-3.5V$, the source of the power device is less than the gate by enough to cause the switch to turn ON again. During this negative transient condition the power limiting circuitry to protect the switch is disabled due to the gate being held at 0V. The maximum current during this clamping interval, which is equal to the steady state ON current through the inductor, should be kept less than 1A. Another concern during this interval has to do with the size of an inductive load and the amount of time required to de-energize it. With larger inductors it may be possible for the additional power dissipation to cause the die temperaure to exceed the thermal shutdown limit. If this occurs all of the other switches will turn OFF momentarily (see section on Thermal Management).

Power Limiting

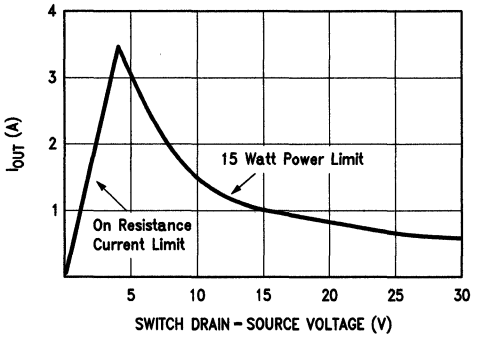
The LMD18400 utilizes a true instantaneous power limit circuit rather than simple current limiting to protect each switch. This provides a higher transient current capability while still maintaining a safe power dissipation level. The power dissipation in each switch (the product of the Drain-to Source voltage and the output current, $V_{ds} \times I_{OUT}$) is con-

Applications Information (Continued)

tinually monitored and limited to 15W by varying the gate voltage and therefore the ON resistance of the switch. Basically the ON resistance will be as low as possible until 15W is being dissipated. To maintain 15W, the ON resistance increases to reduce the load current. This results in a decrease of the output voltage. For resistive loads, the output voltage when in power limit will be:

$$V_{OUT}\ (\text{in Power Limit}) = \frac{V_{CC} - \sqrt{V_{CC}^2 - 60\,R_L}}{2}$$

This provides a maximum transient current and drain-to-source voltage characteristic as shown in *Figure 5*.



TL/H/11026–14

FIGURE 5. Maximum Output Current with Instantaneous Power Limiting

Driving a Lamp

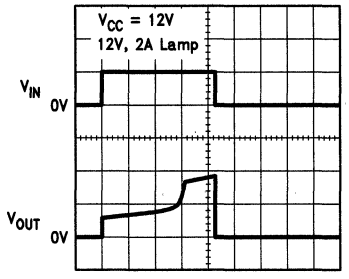


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FIGURE 6. Soft Turn-On of a Lamp Load

The steady state current to the load is limited by the package power dissipation, ambient temperature and the ON resistance of the switch which has a positive temperature coefficient as shown in the Typical Performance Characteristics.

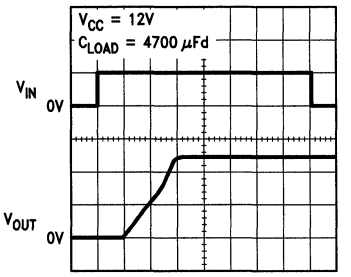
This dynamic current limiting of the switches is beneficial when driving lamp and large capacitive loads. Lamps require a large inrush current, on the order of 10 times the normal operating current, when first switched on with a cold filament. The LMD18400 will limit this initial current to the level where 15W is dissipated in the switch. As the filament warms up the voltage across the lamp increases thereby decreasing the voltage across the switch which permits more current to fully light the lamp. With limited inrush current the lifetime of a lamp load is increased significantly. *Figure 6* illustrates the soft turn-on of a lamp load.

The same principle of increasing output current as the voltage across the load increases allows large capacitive loads to be charged more quickly by an LMD18400 driver than as opposed to a driver with a fixed 1A current limit protection scheme. *Figure 7* shows the output response while driving a large capacitive load.

Thermal Protection

The die temperature of the LMD18400 is continually monitored. Should any conditions cause the die temperature to rise to +170°C, all of the power switches are turned OFF automatically to reduce the power dissipation. It is important to realize that the thermal shutdown affects all four of the switches together. That is, if just one switch load is enough to heat the die to the thermal shutdown threshold, all of the other switches, regardless of their power dissipation conditions, will be switched OFF. All of the switches will be re-enabled when the die temperature has cooled to approximately +160°C. Until the high temperature forcing conditions have been removed the switches will cycle ON and OFF thus maintaining an average die temperature of +165°C. The LMD18400 will signal that excessive temperatures exist through several diagnostic output signals (see Diagnostics).

Driving a Large Capacitive Load



TL/H/11026–16

FIGURE 7. Driving a Large Capacitive Load

Applications Information (Continued)

DIAGNOSTICS

The LMD18400 has extensive circuit diagnostic information reporting capability. Use of this information can produce systems with intelligent feedback of switch status as well as load fault conditions for troubelshooting purposes. All of the diagnostic information is contained in an 11-bit word. This data can be clocked out of the LMD18400 in a serial fashion as shown in *Figure 8*. The shift register is parallel loaded with the diagnostic data whenever the Chip Select Input is at a Logic 1 and changes to the serial shift mode when Chip Select is taken to a Logic 0. The Data Output line (pin 8) is biased internally from a 5.1V regulator which sets the Logic 1 output voltage. This pin has low current sourcing capability so any load on this pin will reduce the Logic 1 output level which is guaranteed to be at least 2.4V with a 360 μA load.

The data interface is MICROWIRE compatible in that data is clocked out of the LMD18400 on the falling edge of the clock, to be clocked into the controlling microprocessor on the rising edge. Any number of devices can share a common data output line because the data output pin is held in a high impedance (TRI-STATE) condition until the device is selected by taking its Chip Select Input low. Following Chip Select going low there is a short data setup time interval (500 ns Min) required. This is necessary to allow the first data bit of information to be established on the data output line prior to the first rising clock edge which will input the data bit into the controller. When all 11 bits of diagnostic data have been shifted out the data output goes to a Logic 1 level until the Chip Select line is returned high.

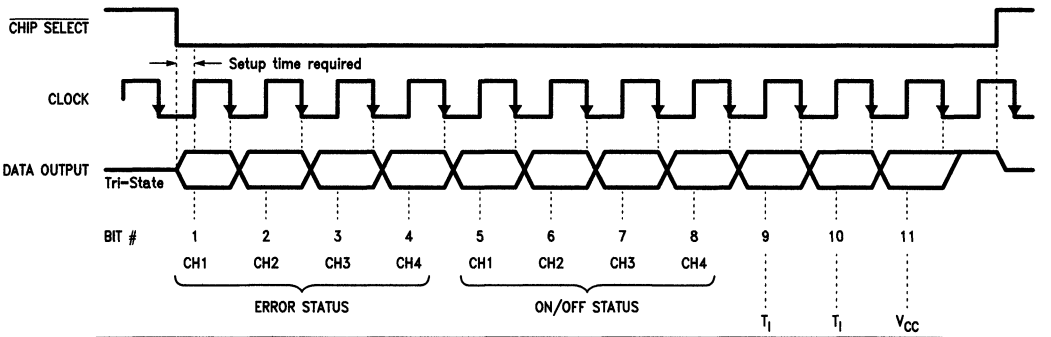
Figure 8 also indicates the significance of the diagnostic data bits. The first 4 bits indicate an output load error condition, one for each channel in succession (see Load Error Detection).

Bits 5 through 8 provide a readback of the commanded ON/OFF status of each switch.

A unique feature of the LMD18400 is that it provides an early warning of excessive operating temperature. Should the die temperature exceed +145°C, bit 9 will be set to a Logic 0. Acting on this information a system can be programmed to take corrective action, shutting OFF specific loads perhaps, while the LMD18400 is still operating normally (not yet in thermal shutdown). If this early warning is ignored and the device continues to rise in temperature, the thermal shutdown circuitry will come into action at a die temperature of +170°C. Should this occur bit 10 of the diagnostic data stream will be set to a Logic 0 indicating that the device is in thermal shutdown and all of the outputs have been shut OFF.

The final data bit, bit 11, indicates an overvoltage condition on the V_{CC} supply (V_{CC} is greater than 35V) and again indicates that all of the drivers are OFF.

The diagnostic data can be read periodically by a controller or only in the event of a general system error indication to determine the cause of any system problem. This general indication of a fault is provided by an Error Flag output (pin 13). This pin goes low whenever any type of error is detected. There is a built-in delay of approximately 75 μs from the time an error is detected until pin 13 is taken low. This is to help mask short duration error conditions such as may be caused by driving highly capacitive loads (>2 μF). A lamp load may generate a shorted load error for several hundred milliseconds as it turns on which should be ignored.



LOGIC 1	LOAD OK	SWITCH OFF	<145°C	<170°C	<35V
LOGIC 0	LOAD ERROR	SWITCH ON	>145°C	>170°C	>35V

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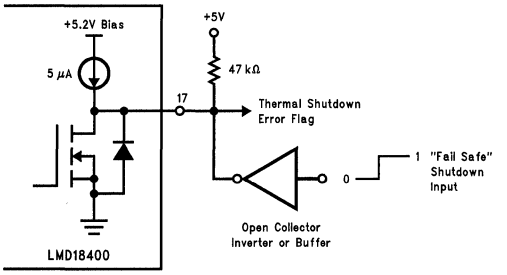
FIGURE 8. Serial Diagnostic Data Assignments

Applications Information (Continued)

The Error Flag output pin is an open drain transistor which requires a pull-up resistor to a positive voltage of up to 16V. Typically this pull-up is to the same 5V supply which is biasing the Enable input and any other external logic circuitry. The Error Flag pins of several LMD18400 packages can be connected together with just one pull-up resistor to provide an all-encompassing general system error indication. Upon detection of an error, each device could then be polled for diagnostic information to determine the source of the fault condition.

A second direct output error flag is for an indication of Thermal Shutdown (pin 17). This active low flag provides an immediate indication that the die temperature has reached +170°C and that the drive to all four switches has been removed. This output is pulled up to the internal 5.1V logic regulator through a small (5 μA) current source so use of a buffer on this pin is recommended.



TL/H/11026–18

FIGURE 9. Thermal Shutdown Flag and Shutdown Input

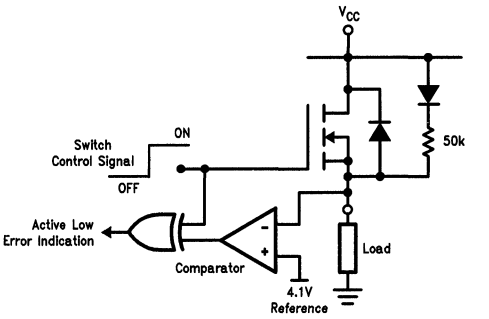
A useful feature of pin 17 is that it can also be used as a shutdown input. Driving this pin low immediately switches all of the drivers OFF, just the same as if thermal shutdown temperatures has been reached, yet all of the control logic and diagnostic circuits remain active. This is useful in designing "fail-safe" systems where the loads can be disabled under any sort of externally detected system fault condition. The diagnostic logic however does not distinguish between normal thermal shutdown or the fact that pin 17 has been driven low. As such, various switch errors and an over-temperature indication will be reported in the diagnostic data stream.

Figure 9 illustrates the use of pin 17 as both an output thermal shutdown flag and as an input to shut down only the switches. Directly tying pin 17 to +5V will prevent the internal thermal shutdown circuitry from disabling the switches. For reliability purposes however this is not recommended as there will then be no limit to the maximum die temperature.

Refer to the Truth Table for a summary of the action of these direct-output error flags.

LOAD ERROR DETECTION

An important feature of the LMD18400 is the ability to detect open or shorted load connections. *Figure 10* illustrates the detection circuit used with each of the drivers.



TL/H/11026–19

FIGURE 10. Detection Circuitry for Open/Shorted Loads

A voltage comparator monitors the voltage to the load and compares it to a fixed 4.1V reference level. When a switch is OFF, the ground referenced load should have no voltage across it. Under this condition, an internal 50 kΩ resistor connected to V_{CC} will provide a small amount of current to the load. If the load resistance is large enough to create a voltage greater than 4.1V an Open Load Error will be indicated for that switch. The maximum load resistance that will not generate an Open Load Error when a switch is OFF can be found by:

$$R_{Max} = \frac{4.1V}{V_{CC} - 4.6V} \times 50\ k\Omega;\ \text{for no Open Load Indication}$$

To make this Open Load Error threshold more sensitive, an external pull-up resistor can be added from the output to the V_{CC} supply.

Also when a switch is commanded OFF, should the load be shorted to the V_{CC} supply, this same circuitry will again indicate an error.

When a switch is commanded ON, the load is expected to have a voltage across it that approaches the V_{CC} potential. If the output voltage is less than the 4.1V threshold an error will again be reported, indicating that the load is either shorted to ground or that the driver is in power limit and not able to pull the output voltage any closer to V_{CC}. The minimum load resistance that will not generate a Shorted Load Error when a switch is ON can be found by:

$$R_{Min} = \frac{4.1V\ (V_{CC} - 4.1V)}{15W};\ \text{for no Shorted Load Error}$$

Applications Information (Continued)

Figure 11 indicates the range of load resistance for normal operation, open load, and shorted load or power limit indication.

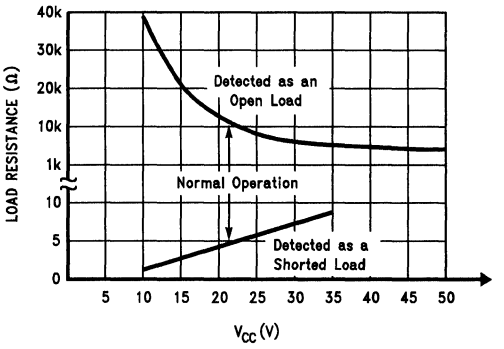


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FIGURE 11. Load Resistance Detected as Errors

THERMAL MANAGEMENT

It is particularly important to consider the total amount of power being dissipated by all four switches in the LMD18400 at all times. Any combination of the switches driving loads will cause an increase in the die temperature. Should the die temperature reach the thermal shutdown threshold of +170°C, all of the switches will be disabled. Careful calculation of the worst case total power dissipation required at any point in time, together with providing sufficient heatsinking will prevent this from occurring.

The LMD18400 is packaged with a special leadframe that helps dissipate heat through the two ground pins on each side of the package. The thermal resistance from junction-to-case (θ_{JC}) for this package is approximately 20°C/W. The thermal resistance from junction-to-ambient (θ_{JA}), without any heatsinking, is approximately 60°C/W. *Figure 12* illustrates how the copper foil of a printed circuit board can be designed to provide heatsinking and reduce the overall junction-to-ambient thermal resistance.

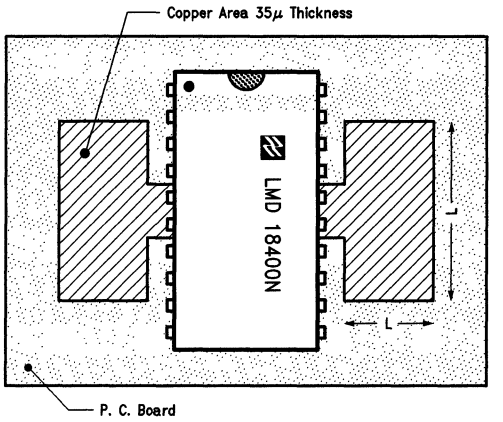
The power dissipation in each switch is equal to:

$$P_{D\ (Each\ Switch)} = I_{Load}^2 \times R_{ON} \quad or \quad \frac{(V_{CC} - V_{OUT})^2}{R_{ON}}$$

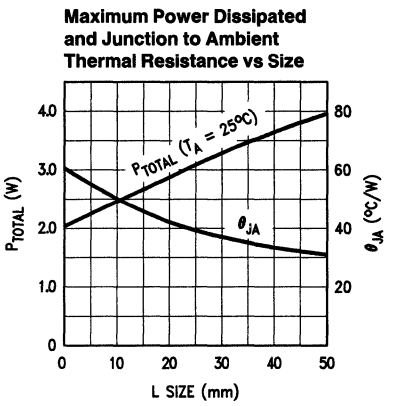
where R_{ON} is the ON resistance of the switch (1.3Ω maximum). These equations hold true until the power dissipation reaches the maximum limit of 15W. With resistive loads, the 15W power limit threshold will be reached when:

$$R_L \leq \frac{V_{CC}^2}{60W}$$

Inductive loads will create additional power dissipation when switched OFF. *Figure 13* shows the idealized voltage and current waveforms for an inductive load.



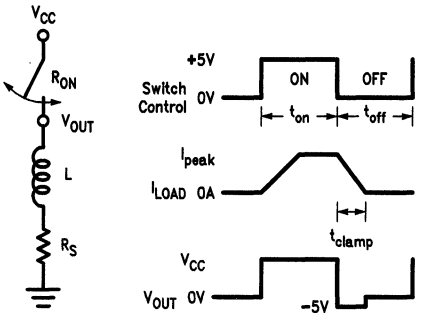
TL/H/11026–21



TL/H/11026–22

FIGURE 12. Recommended PC Board Layout to Reduce the Thermal Resistance from Junction-to-Ambient

Applications Information (Continued)



TL/H/11026–23

FIGURE 13. Switching an Inductive Load

When switched ON, the worst case power dissipation is:

$$P_{D(ON)} = I_{Peak}^2 \times R_{ON}; \text{ where } I_{Peak} = \frac{V_{CC}}{R_{ON} + R_S}$$

The steady-state ON current of the inductor should be kept less than 1A per power switch.

The additional power dissipation during turn-off, as the inductor is de-energized and the voltage across the inductor is clamped to −5V, can be found by:

$$P_{D(OFF)} = \frac{(V_{CC} + 5V) \times I_{Peak}}{2}$$

for the time interval, t_{Clamp}, which is the time required for the inductor current to fall to zero;

$$t_{Clamp} = \frac{I_{Peak} \times L}{5V}$$

The size of the inductor will determine the time duration for this additional power dissipation interval. Even though the peak current is kept less than 1A, the switch during this interval will see a voltage across it of V_{CC} + 5V with no power limit protection. If the inductor is too large, the time interval may be long enough to heat the die temperature to +170°C thereby shutting OFF all other loads on the package.

The total average power dissipation during a full ON/OFF switching cycle of an inductive load will be:

$$P_{D(tot)} = \left[I_{Peak}^2 R_{ON} t_{ON} + \frac{I_{Peak}^2 L (V_{CC} + 5V)}{10} \right] \frac{1}{t_{ON} + t_{OFF}}$$

Due to the common cut-off of all loads forced by thermal shutdown, the thermal time constants of the package become a concern. *Figure 14* provides an indication of the time it takes to heat the die to thermal shutdown with a step increase in package power dissipation from an initial junction temperature of +25°C. This data was measured using a PC board layout providing a thermal resistance from junction to ambient of approximately 35°C/W. Less heatsinking will, of course, result in faster thermal shutdown of the power switches.

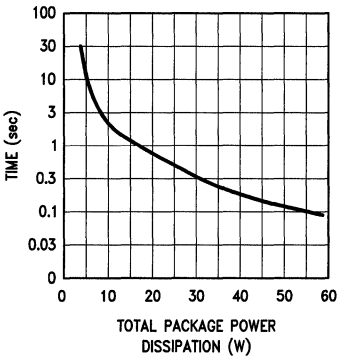


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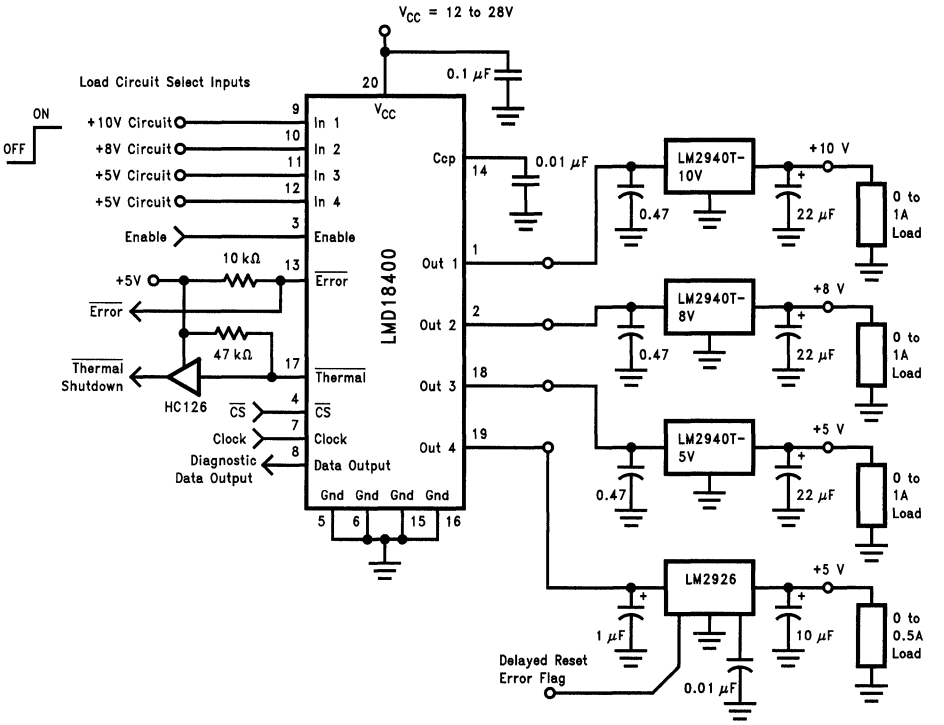
FIGURE 14. Approximate time required for the die to reach the 170°C thermal shutdown point from 25°C for different total package power dissipation levels.

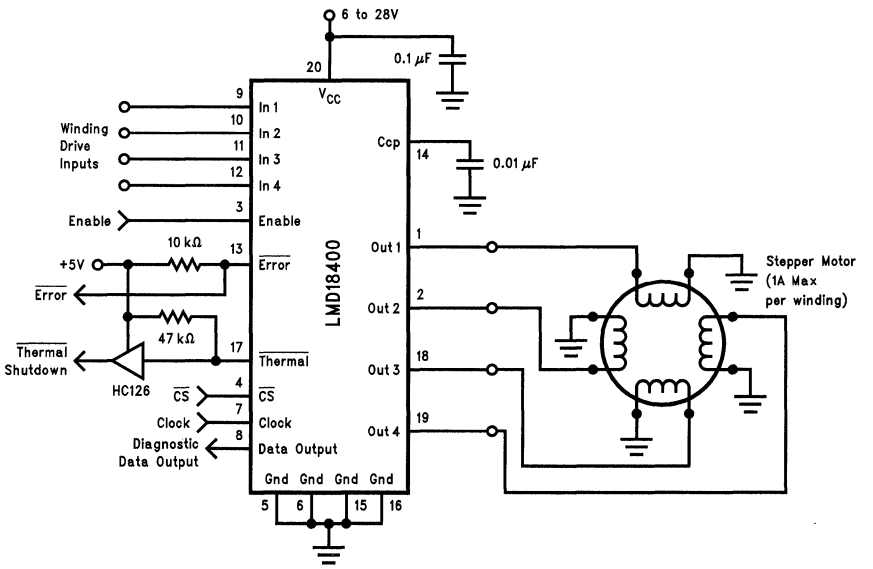
Applications

ON/OFF Switching of multiple voltage regulated circuit loads. Reset flag feedback from the LM2926 as shown connected to Output 4 can make the LMD18400 act as an electronic fuse for load faults.



TL/H/11026–25

Unipolar Drive for a 4-Phase Stepper Motor



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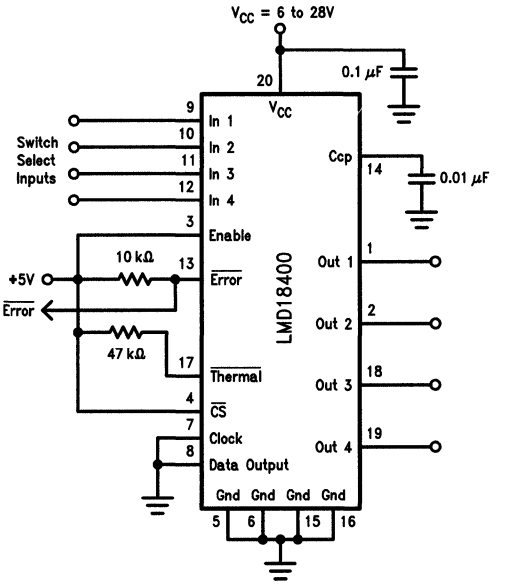
Applications (Continued)

Recommended Connection if No Diagnostics are Required



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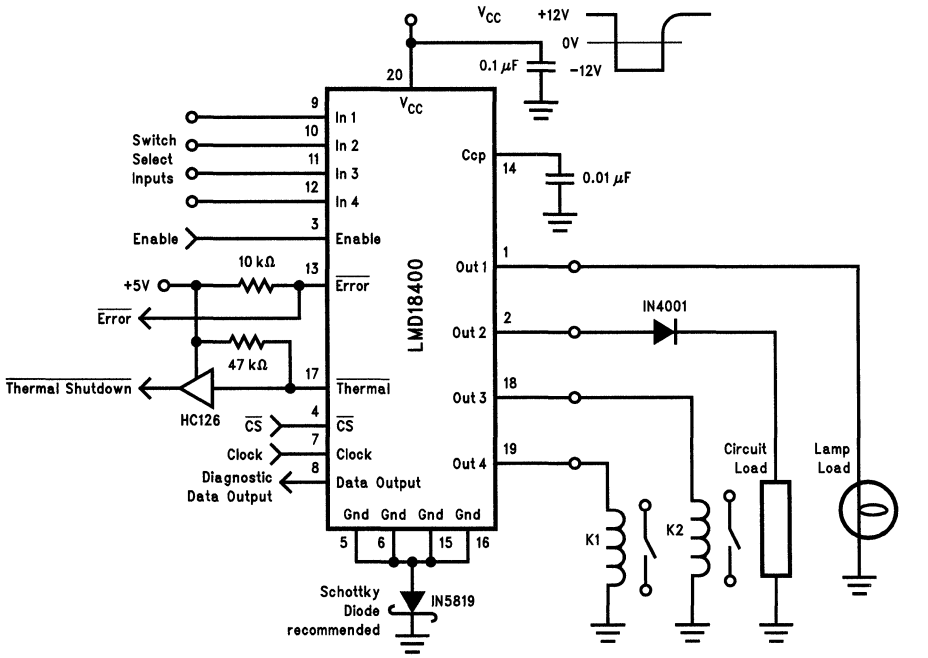
Simple protection of the LMD18400 against supply voltage reversal. Loads will be energized through the intrinsic diodes in parallel with the power switches. The Schottky diode will add approximately 0.2V to the logic input switching thresholds and the logic output low levels.



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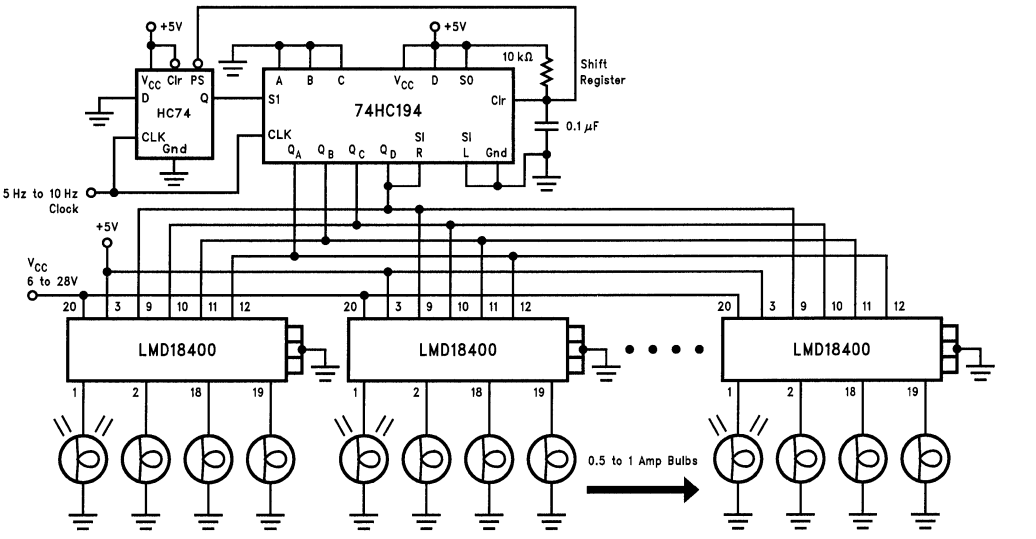
Applications (Continued)

Simple Light "Chaser"



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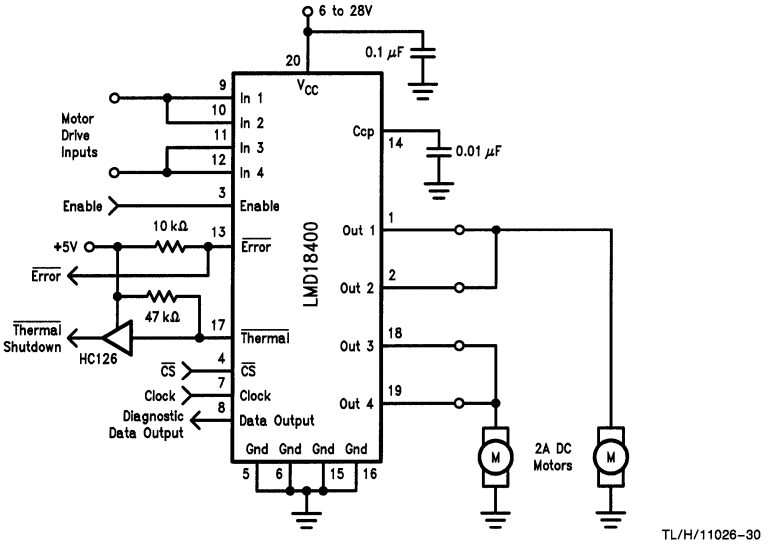
Parallelling switches for higher current capability. Positive temperature coefficient of the switch ON resistance provides ballasting to evenly share the load current between the switches. Any combination of switches can be paralleled. Required peak load current will depend upon the motor load. Motor speed control can be provided by a PWM signal of up to 20 kHz applied to the motor drive input lines.



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Section 8

Special Functions

Section 8 Contents

National Semiconductor

Special Function Circuits Selection Guide

Communications-Related Building Blocks

PLL's AND TONE DECODERS

General purpose PLL's and tone decoders are available for applications that include FSK demodulation, tone decoding, SAP and SCA demodulation, and telemetry reception. Both bipolar and CMOS devices are offered. Special purpose PLL's for TV synchronization and FM stereo demodulation are also available for use in other low frequency signal processing applications.

PLL and Tone Decoder Selection Guide

	†LM567	LMC567* (CMOS LM567)	LMC568
Typical Application	Tone Decoder	Tone Decoder	PLL
Center Frequency Range	0.01 Hz–500 kHz	0.01 Hz–500 kHz	0.01 Hz–500 kHz
VCO Control Range	±7%	±7%	±30%
Supply Voltage	4.75V–9V	2V–9V	2V–9V
Supply Current (Typ)	12 mA	0.8 mA	1.2 mA

*The CMOS LMC567 oscillator runs at twice the frequency of the bipolar LM567 oscillator. Refer to the datasheets for additional information.

† Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

TIMERS

General purpose timers are available for generating accurate time delays or oscillation. Both bipolar and CMOS devices are offered.

Timer Selection Guide

	†LM555	LMC555* (CMOS LM555)	†LM556 (Dual LM555)	LM2240
Trigger Pulse Relative to Output Pulse	Must Be Shorter	Must Be Shorter	Must Be Shorter	Can Be Longer
Typical Application	Astable	Astable	Astable	Programmable Monostable/ Astable
Supply Voltage	4.5V–15V	1.2V–12V	4.5V–15V	4.0V–15.0V
Supply Current (Typical)	10 mA	0.15 mA	10 mA (Each Timer Section)	4 mA – 13 mA (Depends on V_S)

*The CMOS LMC555 can handle −10 mA to +50 mA of output current and the bipolar LM555 can handle up to ±200 mA of output current.

† Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

Communications-Related Building Blocks (Continued)

VCO AND FUNCTION GENERATOR

The LM566 is a general purpose voltage controlled oscillator which may be used to generate square and triangle waves. Typical applications include FM modulation, signal generation, function generation, frequency shift keying, and tone generation. The LM566 has very linear modulation characteristics.

Precision-Related Building Blocks

TRANSISTOR ARRAYS

A variety of matched and power transistors are offered.

Transistor Array Selection Guide

	†LM394	LM195/†LM395/LP395	LM3046	LM3146
Description	NPN Transistor Pair	Power Transistor	5 NPN Transistors	5 NPN Transistors
Key Features	• Emitter-Base Voltage Matched to 50 μV • Current Gain Matched to 2%	• Collector Current: 1A • Quiescent Current: 10 mA • Switching Time: 2 μs • Current Limit • Thermal Limit • Safe Area Protection	• Emitter-Base Voltage Matched to ±5 mV • Breakdown Voltages —$V_{(BR)(CBO)}$: 20V —$V_{(BR)(CEO)}$: 15V —$V_{(BR)(CIO)}$: 20V —$V_{(BR)(EBO)}$: 5V • DC—120 MHz	• Emitter-Base Voltage Matched to ±5 mV • Breakdown Voltages —$V_{(BR)(CBO)}$: 40V —$V_{(BR)(CEO)}$: 30V —$V_{(BR)(CIO)}$: 40V —$V_{(BR)(EBO)}$: 5V • DC—120 MHz

† Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

Special Converters

A variety of special converters for signal transformation applications are offered.

Special Converters Selection Guide

	LH0091	LH0094	†LM331 (Note 1)	LM2907, LM2917
Converter Type	True RMS-to-DC	Multifunction	Voltage-to-Frequency	Frequency-to-Voltage
Key Features	• 0.05% Accuracy with External Trim • Uncommitted Amplifier for Filtering, Gain or High Crest Factor Configuration • True RMS Conversion	• $V_{OUT} = V_y\left(\frac{V_Z}{V_X}\right)^m$, $0.1 \leq m \leq 10$, m Continuously Adjustable • Applications —Precision Divider, Multiplier —Square Root —Square —Trigonometric Function Generator —Companding —Linearization —Control Systems —Log Amp	• 1 Hz to 100 kHz Frequency Range • Split or Single Supply Operation	• Operates Relay, Lamp or Other Load when Input Exceeds a Selected Rate • Ground Referenced Tachometer Fully Protected from Damage Due to Swings Above Supply or Below Ground

Note 1: See the Data Acquisition Linear Devices Databook for datasheet.

†Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

National Semiconductor

DH0006/DH0006C* Current Drivers

General Description

The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28V. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

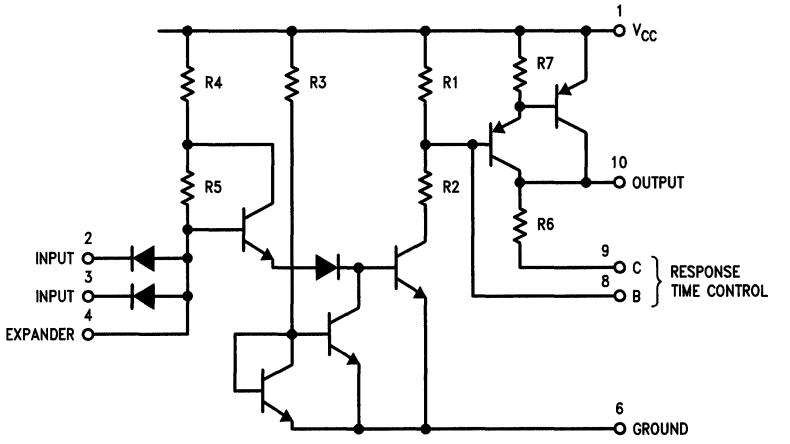
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

Features

- Operation from a Single +10V to +45 Power Supply
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply
- 1.5A, 50 ms, Pulse Current Capability

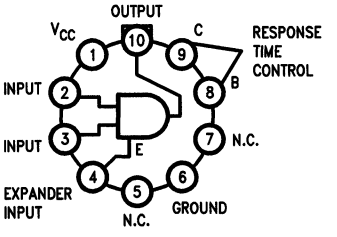
*Previously called NH0006/NH0006C

Schematic and Connection Diagrams



TL/K/10120–1

Metal Can Package



TL/K/10120–2

Top View

Order Number DH0006H or DH0006CH
See NS Package Number H10F

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
DH0006	−55°C to +125°C
DH0006C	0°C to +70°C
Storage Temperature	−65°C to +150°C

Electrical Characteristics (Note 1)

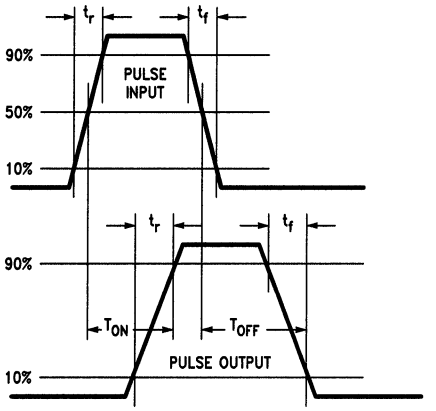
Parameter	Conditions	Min	Typ (Note 2)	Max	Units
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1k		0.001	0.01	
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9.2		
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V V_{CC} = 45V, V_{IN} = 5.5V		0.5	5.0 100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		μs
Fall Time			0.8		
T_{on}			0.26		
T_{off}			2.2		

Note 1: Unless otherwise specified, limits shown apply from −55°C to +125°C for DH0006 and 0°C to +70°C for DH0006C.

Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and θ_{JA} of 210°C/W.

Switching Time Waveforms

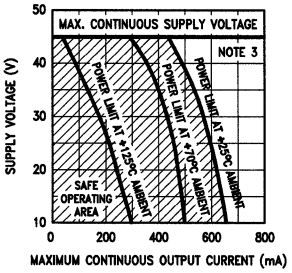


TL/K/10120–6

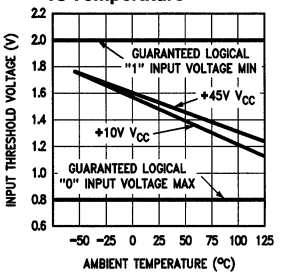
8

Typical Performance Characteristics

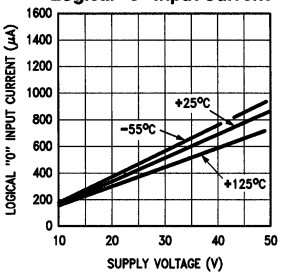
Maximum Continuous Output Current for TO-5



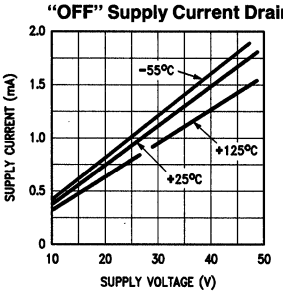
Input Threshold Voltage vs Temperature



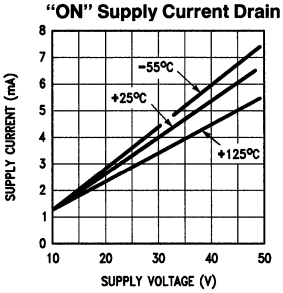
Logical "0" Input Current



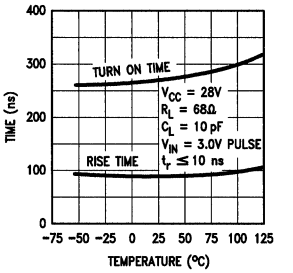
"OFF" Supply Current Drain



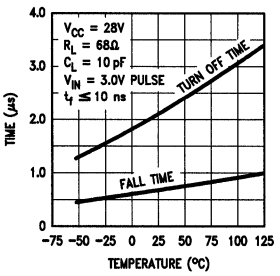
"ON" Supply Current Drain



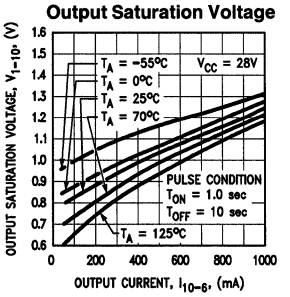
Turn On and Rise Time



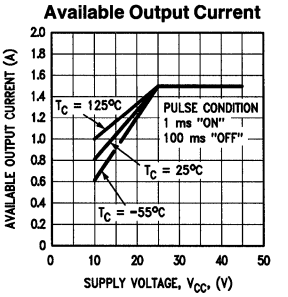
Turn Off and Fall Time



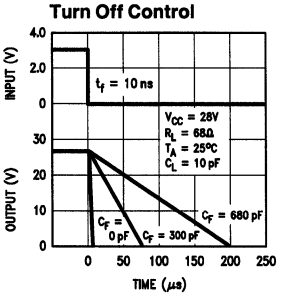
Output Saturation Voltage



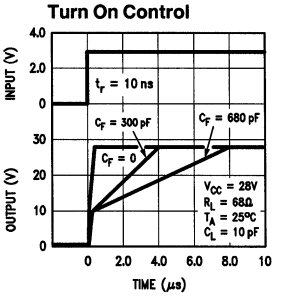
Available Output Current



Turn Off Control



Turn On Control



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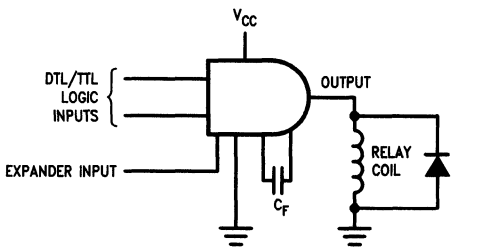
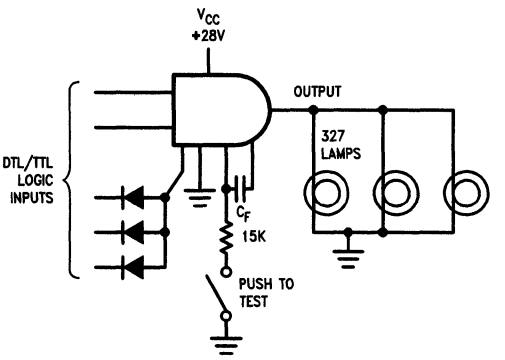
Typical Applications

Relay Driver



TL/K/10120–4

Lamp Driver with Expanded Inputs



TL/K/10120–5

8

National Semiconductor

DH0008
High Voltage, High Current Driver

General Description

The DH0008 is an integrated high voltage, high current driver, designed to accept standard DTL or TTL input levels and provide a pulsed load of up to 3A from a continuous supply voltage up to 45V. AND inputs are provided with an EXPANDER connection, should additional gating be required.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

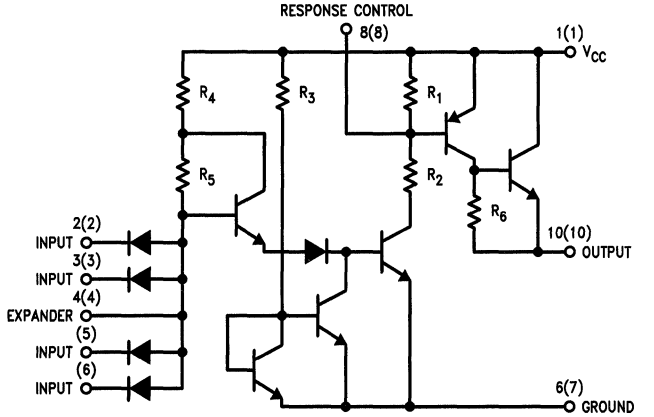
The high pulse current capability makes the DH0008 ideal for driving nonlinear resistive loads such as incandescent lamps. The circuit also requires only one power supply for circuit functional operation.

*Previously called NH0008/NH0008C

Features

- Operation from a single +10V to +45V power supply
- Low standby power dissipation of only 35 mW for 28V power supply
- 3.0A, 50 ms, pulse current capability

Schematic and Connection Diagrams



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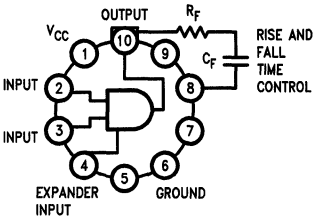
Numbers in parentheses are pin numbers for N package only

Metal Can Package



TL/K/10121-2

Top View

Order Number DH0008H
See NS Package Number H10F

Switching Sequence

Step	A	B	C	D
1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

To reverse the direction use a 4, 3, 2, 1 sequence.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Peak Power Supply Voltage (for 0.1s)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1s Off)	3.0A
Operating Temperature DH0008	−55°C to +125°C
Storage Temperature	−65°C to +150°C

Electrical Characteristics (Note 1)

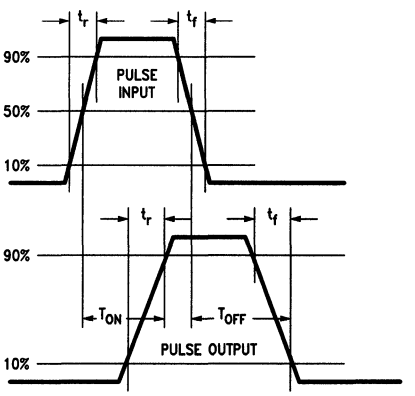
Parameter	Conditions	Min.	Typ. (Note 2)	Max.	Units
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A 50 ms On/1 s Off	43	43.5		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1 kΩ		0.02	0.1	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 0.8A 50 ms On/1 s Off	26.5	27.1		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V V_{CC} = 45V, V_{IN} = 5.5V		0.5	5.0 100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8.0	mA
Rise Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.2		μs
Fall Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		3.0		μs
T_{ON}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.4		μs
T_{OFF}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		7.0		μs

Note 1: Unless otherwise specified limits shown apply from −55°C to +125°C for DH0008 and 0°C to +70°C for DH0008C.

Note 2: Typical values are 25°C.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a θ_{JA} of 210°C/W.

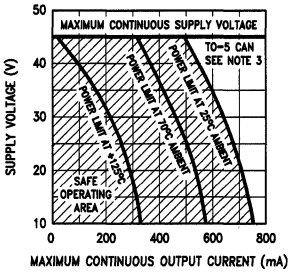
Switching Time Waveforms



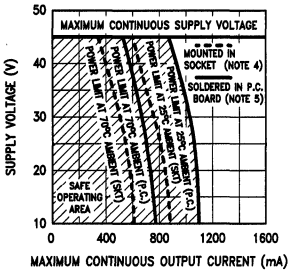
TL/K/10121–5

Typical Performance Characteristics

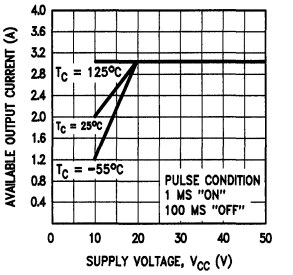
Maximum Continuous Output Current for TO-5 Package



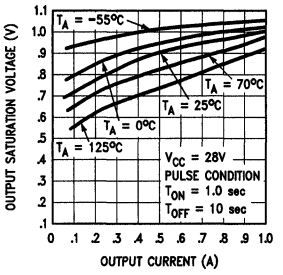
Maximum Continuous Output Current for Molded DIP



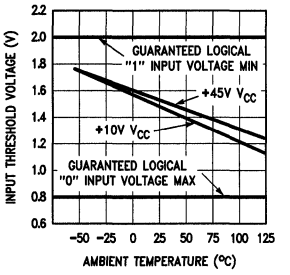
Available Output Current



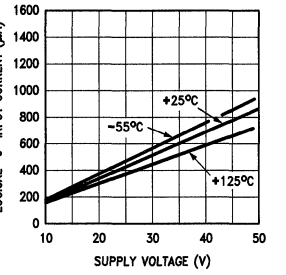
Output Saturation Voltage



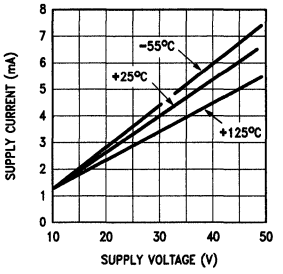
Input Threshold Voltage vs Temperature



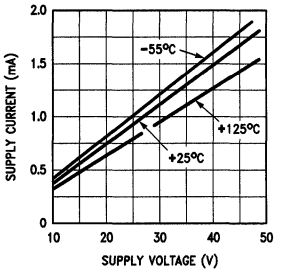
Logical "0" Input Current



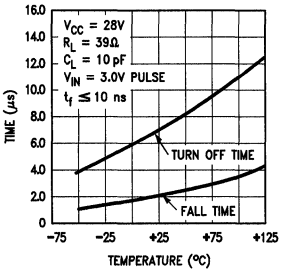
ON Supply Current Drain



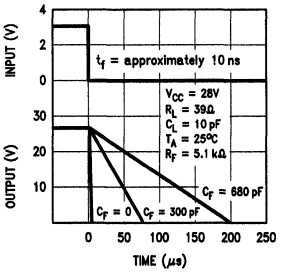
OFF Supply Current Drain



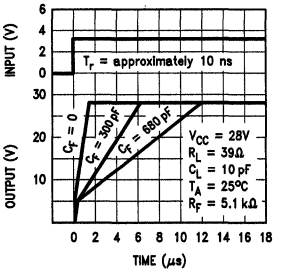
Turn OFF and Fall Times



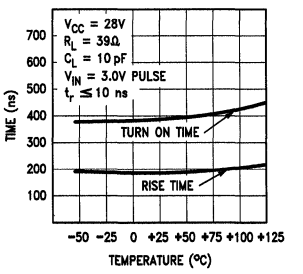
Turn ON Control



Turn OFF Control



Turn ON and Rise Time



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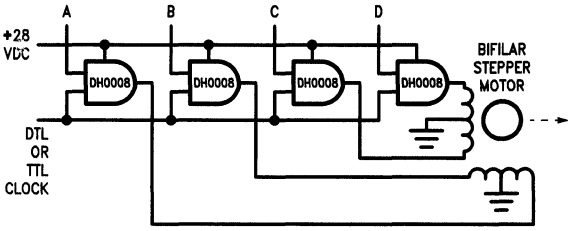
Typical Applications

Controller for Closed Loop Stepper Motor



TL/K/10121–4

National Semiconductor

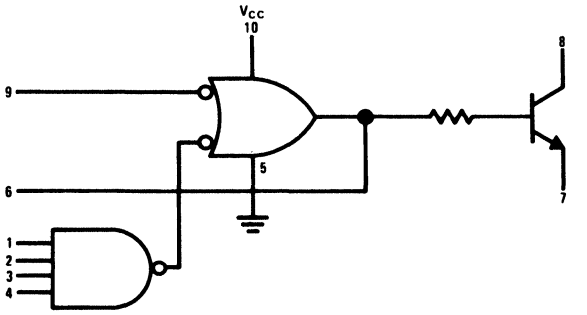
DH0011A High Voltage High Current Driver

General Description

The DH0011A High Voltage, High Current Driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 50V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

Logic Diagram



TL/K/6863–1

Ordering Information

NSC Designation	Package	Temperature Range	Output Capability
DH0011AH	H10C	−55°C to +125°C	500mA

Absolute Maximum Ratings

V_{CC}	8V	Power Dissipation	800 mW
Collector Voltage (Output)	50V	Operating Temperature Range	−55°C to +125°C
Input Reverse Current	1.0 mA	Storage Temperature	−65°C to +150°C

Electrical Characteristics

Test Pin	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Sense	Min	Max
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
12					GND				V_R	V_{CC}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
17				GND	GND				V_F	V_{CC}	I_9		$-I_F$
18					GND		GND			V_{CC}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CC}	I_8		I_{OX}
20					GND					V_{PD}	I_{10}		I_{PD}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms

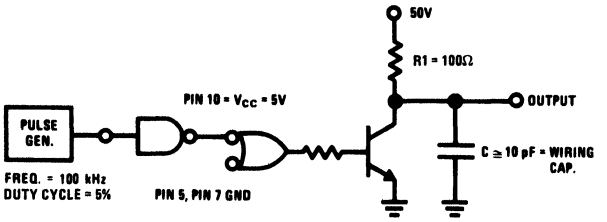
Forcing Functions

Parameter	−55°C	+25°C	+125°C	Units
				V
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
I_{OL1}	400	400	400	mA
I_{OL2}	20	20	20	mA
V_{OX}	50.0	50.0	50.0	V

Limits

Parameter	−55°C		+25°C		+125°C		Units
	Min	Max	Min	Max	Min	Max	
V_{OL1}		0.6		0.6		0.6	V
V_{OL2}		0.45		0.45		0.45	V
V_{OH}	1.95		1.85		1.65		V
I_R				60		60	μA
$-I_F$		1.6		1.6		1.6	mA
I_{OX}				5.0		200	μA
I_{PD}				12.2			mA
I_{MAX}				10			mA
t_{ON}				160			ns
t_{OFF}				220			ns

Switching Time Test Circuit



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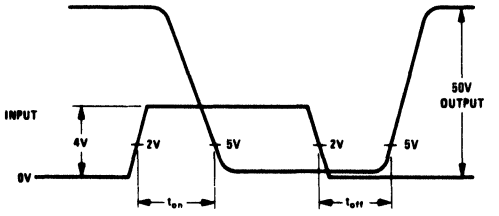
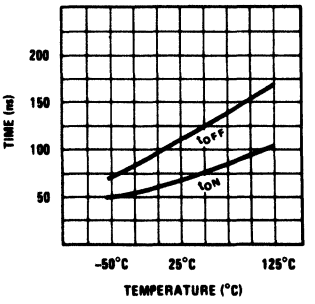
Switching Time Waveforms



TL/K/6863–3

Typical Switching Times



TL/K/6863–4

National Semiconductor

DH0035/DH0035C PIN Diode Driver

General Description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

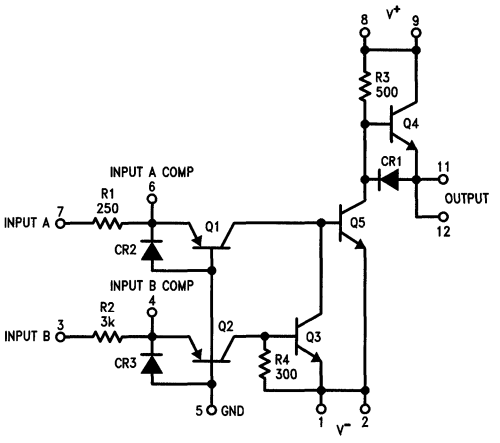
Features

- Large output voltage swing—30V
- Peak output current in excess of 1A
- Inputs TTL/DTL compatible
- Short propagation delay—10 ns
- High repetition rate—5 MHz

The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers.*

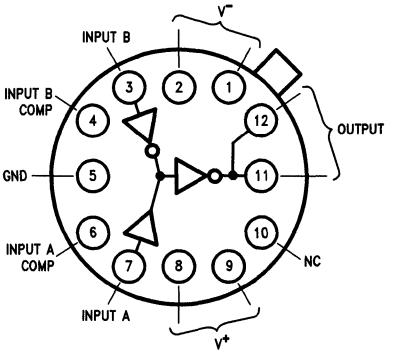
The DH0035 is guaranteed over the temperature range −55°C to +125°C whereas the DH0035C is guaranteed from 0°C to +85°C.

Schematic and Connection Diagrams



TL/K/10124–1

Metal Can Package



TL/K/10124–2

Top View

Order Number DH0035G-MIL or DH0035CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V
Input Current (Pin 3 or 7)	±75 mA
Peak Output Current	±1.0A
Power Dissipation (Note 3)	1.5W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DH0035	−55°C to +125°C
DH0035C	0°C to +85°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Input Logic "1" Threshold	V_{OUT} = −8V, R_L = 100Ω		1.0	2.0	V
Input Logic "0" Threshold	V_{OUT} = +8V, R_L = 100Ω	0.4	0.6		V
Positive Output Swing	I_{OUT} = 100 mA	7.0	+8.0		V
Negative Output Swing	I_{OUT} = 100 mA		−8.0	−7.0	V
Positive Short Circuit Current	V_{IN} = 0V, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	400	800		mA
Negative Short Circuit Current	V_{IN} = 1.5V, I_{IN} = 50 mA, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	800	1000		mA
Turn-On Delay	V_{IN} = 1.5V, V_{OUT} = −3V		10	15	ns
Turn-Off Delay	V_{IN} = 1.5V, V_{OUT} = +3V		15	30	ns
On Supply Current	V_{IN} = 1.5V		45	60	mA

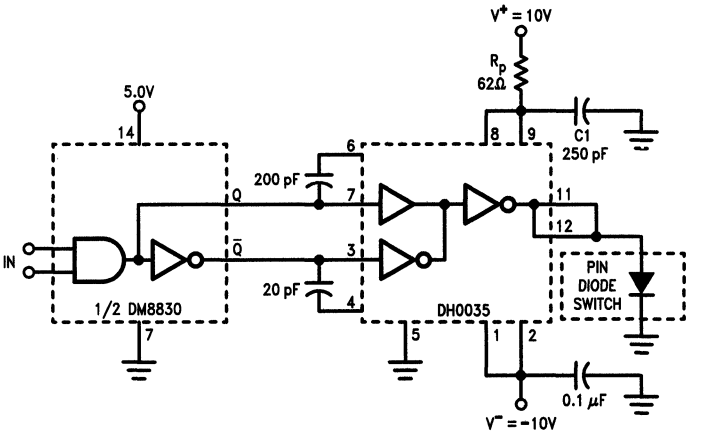
Note 1: Unless otherwise specified, these specifications apply for V^+ = 10.0V, V^- = − 10.0V, pin 5 grounded, over the temperature range −55°C to +125°C for the DH0035, and 0°C to +85°C for the DH0035C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 10 mW/°C for ambient temperatures above 25°C.

Typical Applications

Grounded Cathode Design

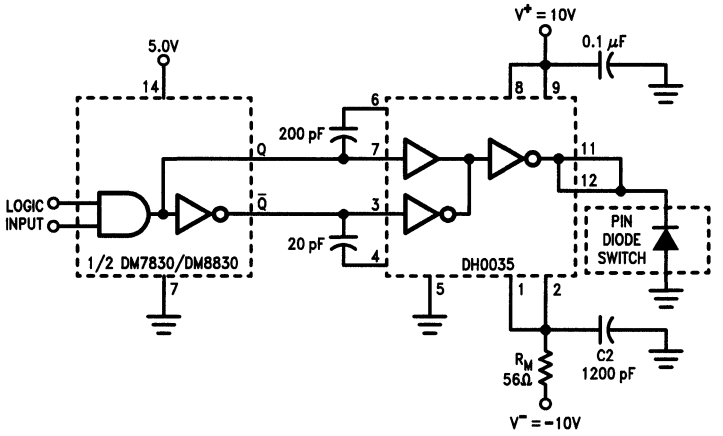


TL/K/10124–3

Note: Cathode grounded PIN diode: R_p = 62Ω limits diode forward current to 100 mA. Typical switching for HP33604A, RF turn-on 25 ns, turn-off 5 ns. C2 = 250 pF, R_p = 0Ω, C1 = 0.1F.

Typical Applications (Continued)

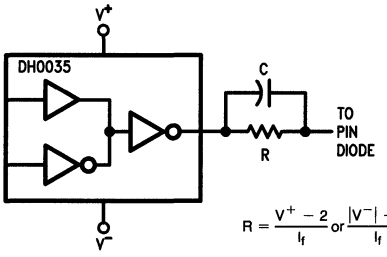
Grounded Anode Design



TL/K/10124–4

Note: Anode Grounded PIN diode: $R_M = 56\Omega$ limits diode forward current to 100 mA. Typical switching for HP33622A, RF turn-on 5 ns; turn-off 4 ns. C1 = 470 pF, C2 = 0.1 μF, $R_M = 0\Omega$.

Alternate Current Limiting



$$R = \frac{V^+ - 2}{I_f} \text{ or } \frac{|V^-| - 2}{I_f}$$

TL/K/10124–5

National Semiconductor

DH0034
High Speed Dual Level Translator

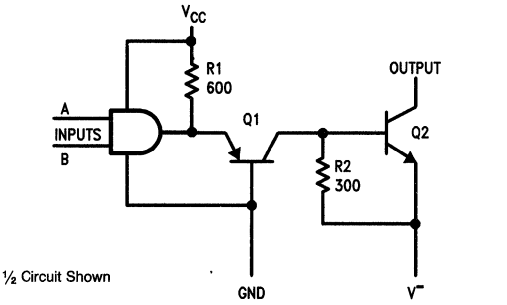
General Description

The DH0034 is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

Features

- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA

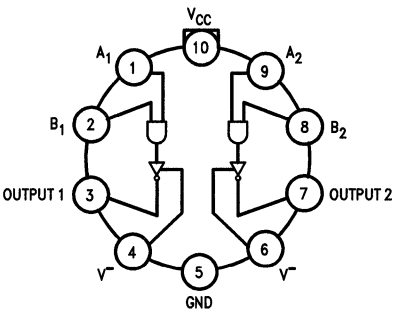
Schematic and Connection Diagrams



½ Circuit Shown

TL/K/10122-1

Metal Can Package

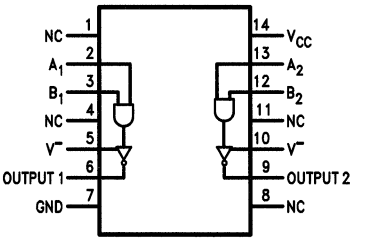


TL/K/10122-2

Top View

Order Number DH0034H-MIL
See NS Package Number H10F

Dual-In-Line Package



TL/K/10122-3

Top View

Order Number DH0034D
See NS Package Number D14D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage	7.0V
Negative Supply Voltage	−30V
Positive Supply Voltage	+25V
Differential Supply Voltage	25V
Maximum Output Current	100 mA
Input Voltage	+5.5V
Operating Temperature Range DH0034	−55°C to +125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (See Notes 1 and 2)

Parameter	Conditions	DH0034			Units
		Min	Typ	Max	
Logical "1" Input Voltage	V_{CC} = 4.5V V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 5.5V V_{CC} = 5.25V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V V_{CC} = 5.25V, V_{IN} = 5.5V			1.0	mA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Power Supply Current Logic "0"	V_{CC} = 5.5V, V_{IN} = 4.5V V_{CC} = 5.25V, V_{IN} = 4.5V (Note 3)		30	38	mA
Power Supply Current Logic "1"	V_{CC} = 5.5V, V_{IN} = 0V V_{CC} = 5.25V, V_{IN} = 0V (Note 3)		37	48	mA
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 100 mA V_{CC} = 4.5V, I_{OUT} = 50 mA		V^- + 0.50 V^- + 0.3	V^- + 0.50	V
Output Leakage Current	V_{CC} = 5.5V, V_{IN} = 0.8V $V^+ - V^-$ = 25V		0.1	5.0	μA
Transition Time to Logical "0"	V_{CC} = 5.0V, V_3 = 0V, T_A = 25°C V^- = 25V, R_L = 510Ω		15	25	ns
Transition Time to Logical "1"	V_{CC} = 5.0V, T_A = 25°C V^- = −25V, R_L = 510Ω		35	75	ns

Note 1: The specifications apply over the temperature range −55°C to +125°C for the DH0034 with a 510Ω resistor connected between output and ground, and V^- connected to −25V, unless otherwise specified.

Note 2: All typical values are for T_A = 25°C.

Note 3: Current measured is total drawn from V_{CC} supply.

Note 4: Power rating for the TO-5 metal can based on a maximum junction temperature of 175°C and θ_{JA} = 210°C/W.

Note 5: Power rating for the Cavity DIP based on a maximum junction temperature of 175°C and θ_{JA} = 180°C/W.

Theory of Operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by

$$\frac{V_{CC} - V_{BE}}{R1}$$

Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0", the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

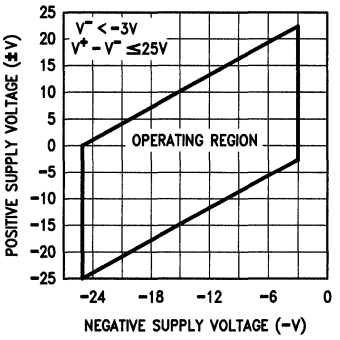
Applications Information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2Ω/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

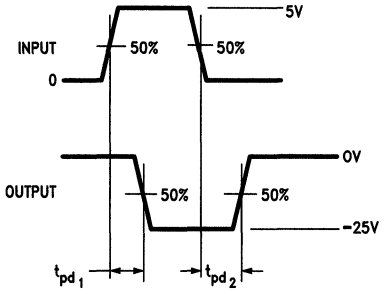
2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. **The range of operation for the negative supply is shown on the X axis and must be between −3V and −25V.** The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to −6V would dictate values of V^+ between −5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.



TL/K/10122-6

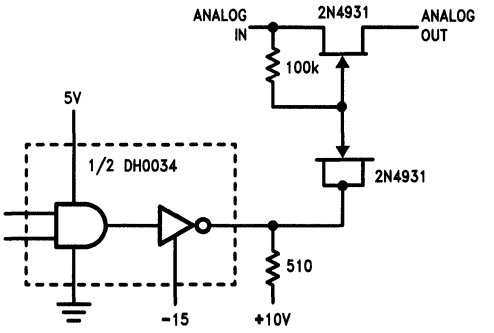
Switching Time Waveforms



TL/K/10122-7

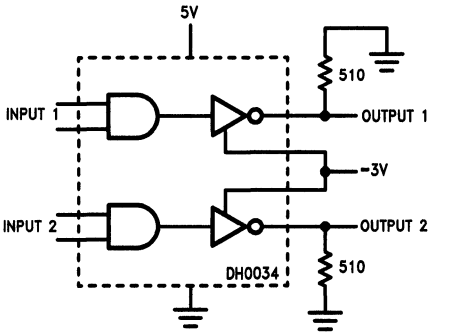
Typical Applications

5 MHz Analog Switch



TL/K/10122–4

TTL to IBM (SLT) Logic Levels



TL/K/10122–5

National Semiconductor

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_O = V_y \left(\frac{V_Z}{V_X}\right)^m, \; 0.1 \leq m \leq 10, \; m \text{ continuously adjustable}$$

m is set by 2 resistors.

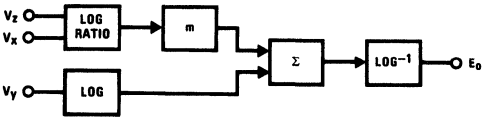
Features

- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range—±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m=2 and m=0.5

Applications

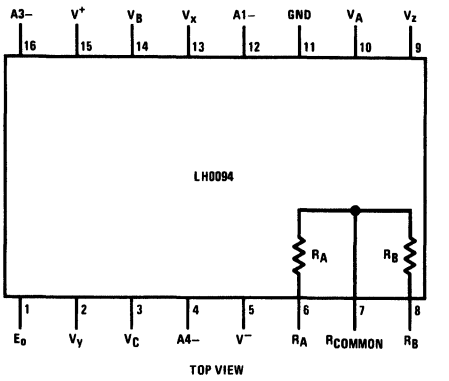
- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams



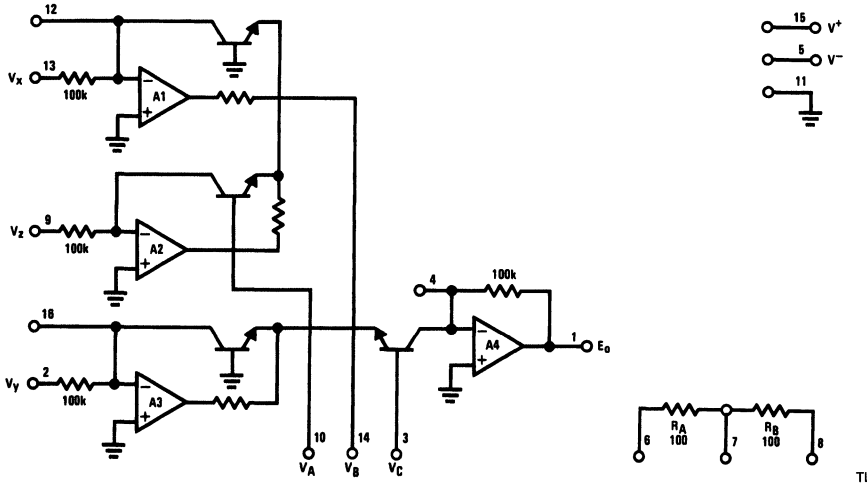
Order Number LH0094CD
See NS Package Number D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



TL/H/5695–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Input Voltage	±22V
Output Short-Circuit Duration	Continuous
Operating Temperature Range LH0094CD	−25°C to +85°C
Storage Temperature Range LH0094CD	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_Y \frac{V_Z^m}{V_X}$; $0.1 \le m \le 10$; $OV \le V_X, V_Y, V_Z \le 10V$

Parameter	Conditions	LH0094C			Units
		Min	Typ	Max	
ACCURACY					
Multiply	$E_O = V_Z V_Y$ ($0.03 \le V_Y \le 10V$; $0.01 \le V_Z \le 10V$)				% F.S.
Untrimmed	*(Figure 2)*		0.45	0.9	(10V)
External Trim	*(Figure 3)*		0.1		% F.S.
	vs. Temperature		0.2		mV/°C
Divide	$E_O = 10V_Z/V_X$				
Untrimmed	*(Figure 4)*, $0.5 \le V_X \le 10$; $0.01 \le V_Z \le 10$)		0.45	0.9	% F.S.
External Trim	*(Figure 5)*, ($0.1 \le V_X \le 10$; $0.01 \le V_Z \le 10$)		0.1		% F.S.
	vs. Temperature		0.2		mV/°C
Square Root	$E_O = 10\sqrt{V_Z/10}$				
Untrimmed	*(Figure 8)*, ($0.03 \le V_Z \le 10$		0.45	0.9	% F.S.
External Trim	*(Figure 9)*, ($0.01 \le V_Z \le 10$		0.15		% F.S.
Square	$E_O = 10\ (V_Z/10)^2$ ($0.1 \le V_Z \le 10$)				
Untrimmed	*(Figure 6)*	1.0	2.0	% F.S.	
External Trim	*(Figure 7)*	0.15		% F.S.	
Low Level	$E_O = \sqrt{10V_Z}$; $5.0mV \le V_Z \le 10V$, *(Figure 10)*		0.05		% F.S.
Square Root					
Exponential	$m = 0.2$, $E_O = 10\ (V_Z/10)^2$ *(Figure 11)*, ($0.1 \le V_Z \le 10$)		0.08		% F.S.
Circuits	$m = 5.0$, $E_O = 10\ (V_Z/10)^5$ *(Figure 11)*, ($1.0 \le V_Z \le 10$)		0.08		% F.S.
OUTPUT OFFSET					
	$V_X = 10V$, $V_{\ } = V_Z = 0$		5.0	10	mV
AC CHARACTERISTICS					
3 dB Bandwidth	$m = 1.0$, $V_X = 10V$, $V_Y = 0.1\ V_{rms}$		10		kHz
Noise	10 Hz to 1.0 kHz, $m = 1.0$, $V_Y = V_Z = OV$				
	$V_X = 10V$		100		μV/rms
	$V_X = 0.1V$		300		μV/rms
EXPONENT					
m		0.2 to 5.0	0.1 to 10		
INPUT CHARACTERISTICS					
Input Voltage	(For Rated Performance)	0		10	V
Input Impedance	(All Inputs)	98	100		kΩ
OUTPUT CHARACTERISTICS					
Output Swing	($R_L \le 10k$)	10	12		V
Output Impedance			1.0		Ω
Supply Current	($V_S = \pm 15V$) (Note 1)		3.0	5.0	mA

Note 1: Refer to RETS0094D drawing for specifications of the military LH00940 version.

8

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode (*Figure 1*) is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

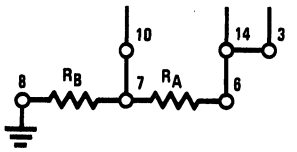
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

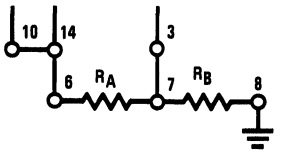
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ± 10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*



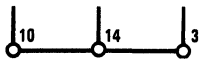
TL/H/5695-2

*No external resistors required, strap as indicated

External Resistors

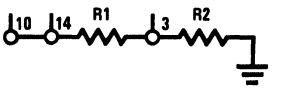
The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 ≤ 500Ω.

(a) m = 1



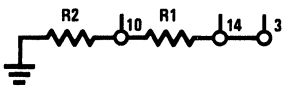
TL/H/5695-3

(b) m < 1



$$m = \frac{R2}{R1+R2} \quad R1+R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1+R2}{R2}$$

TL/H/5695-4

ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈ 25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

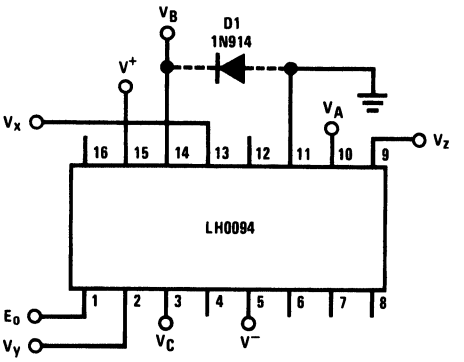
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponent—otherwise, results may be misinterpreted. For example, consider the $1/_{10}$th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION



$$E_O = V_y \left(\frac{V_Z}{V_X}\right)^m$$

$0.1 \leq m \leq 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

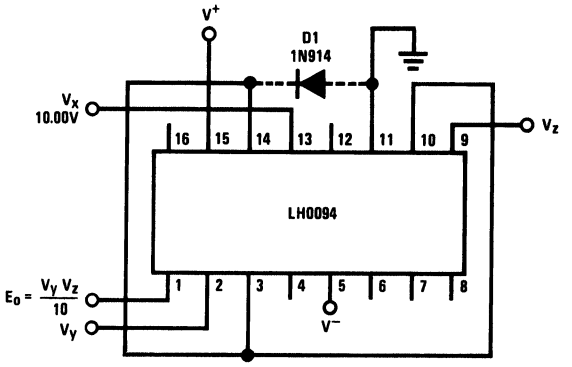


FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

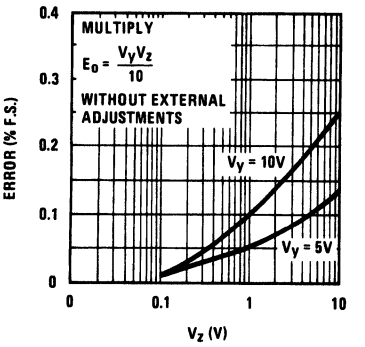
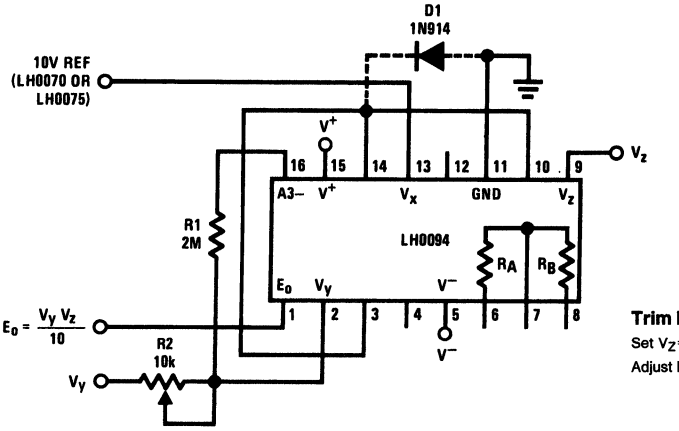


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment



$$E_O = \frac{V_Y V_Z}{10} \qquad m = 1$$

Trim Procedure

Set $V_Z = V_Y = 10V$

Adjust R2 until output = 10.000V

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FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

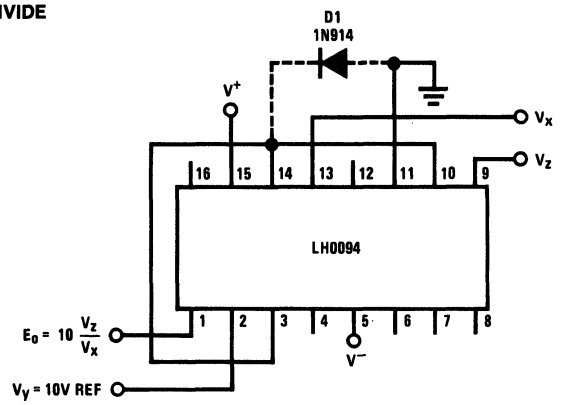

FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

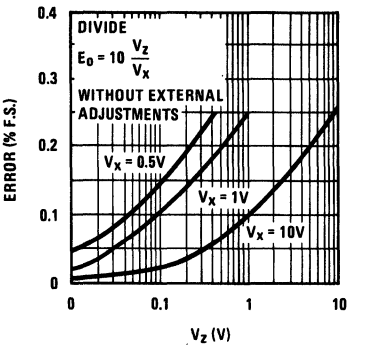

FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_Y, 0.1V to V_X and V_Z.
Adjust R3 until $E_O = 10.000V$.

Apply 10.000V to all inputs.
Adjust R2 until $E_O = 10.000V$

Repeat procedure.

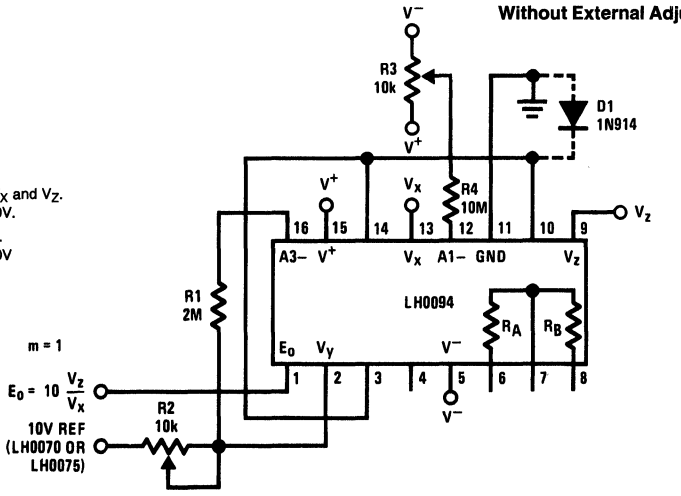

FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

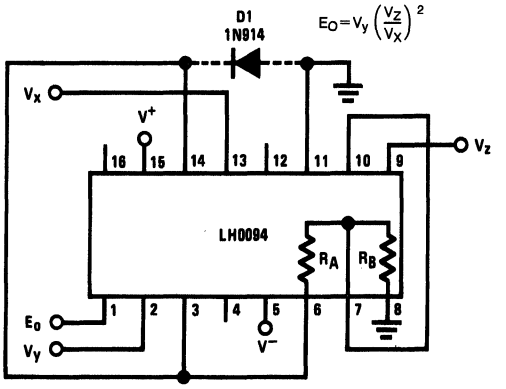

FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

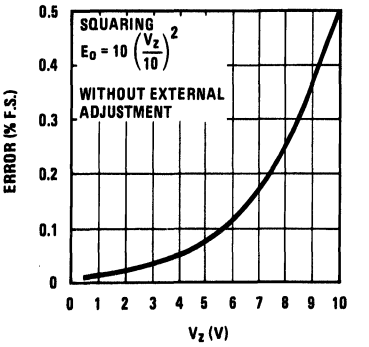

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FIGURE 6b. Squaring Mode without External Adjustment

Applications Information (Continued)

4. SQUARE (Continued)

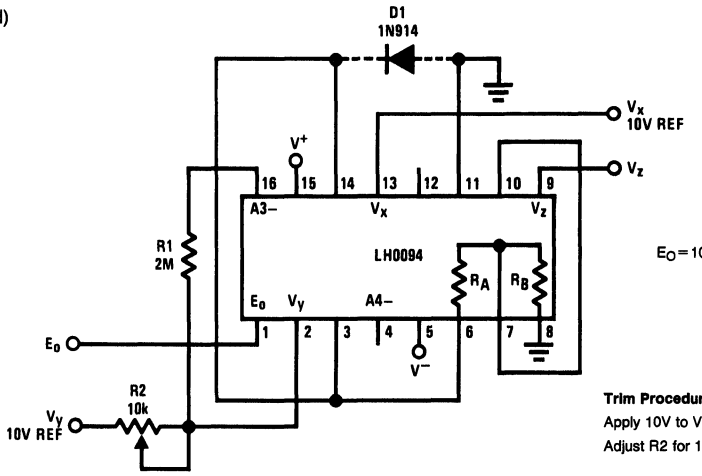

FIGURE 7. Precision Squaring Circuit (0. 15% Typ)

5. SQUARE ROOT

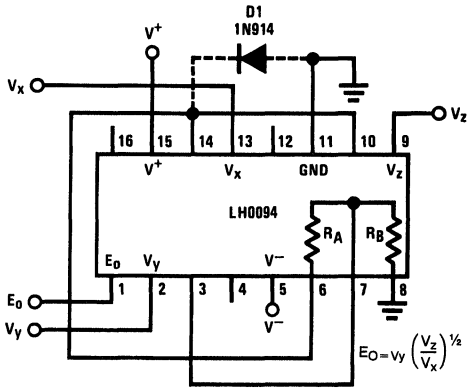

FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

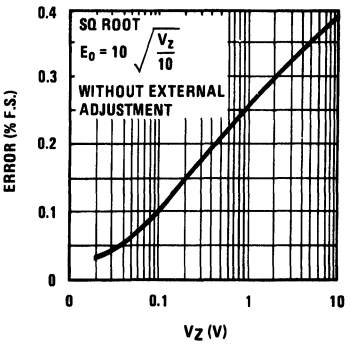

FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment

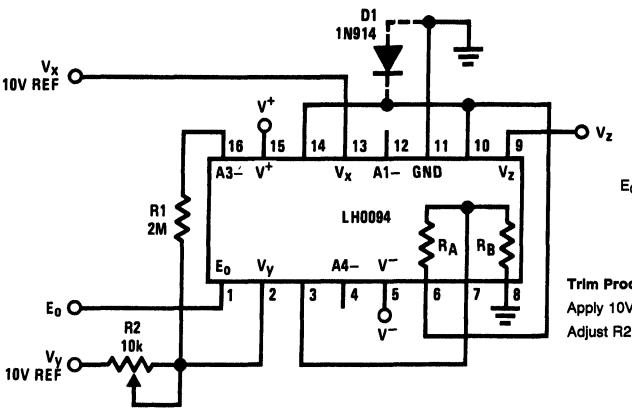

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FIGURE 9. Precision Square Rooter (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT

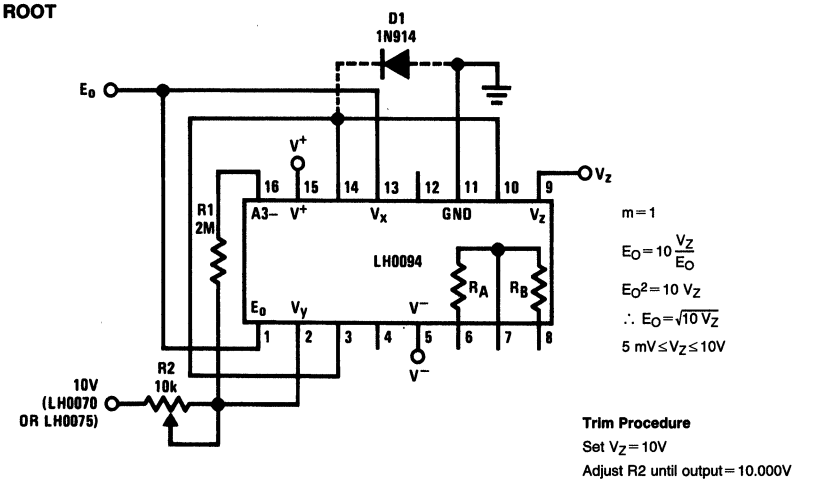
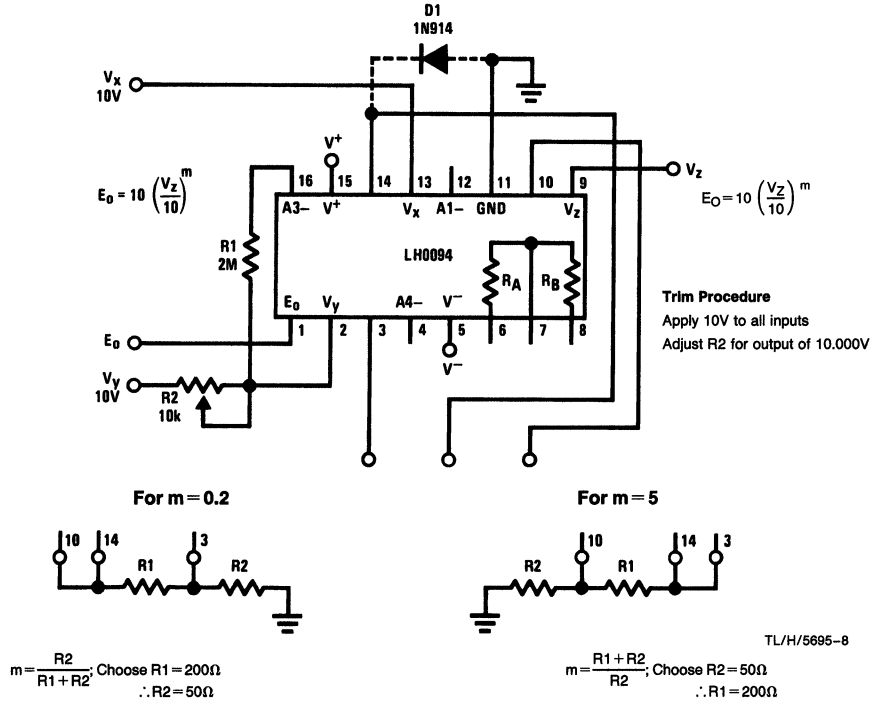


FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications

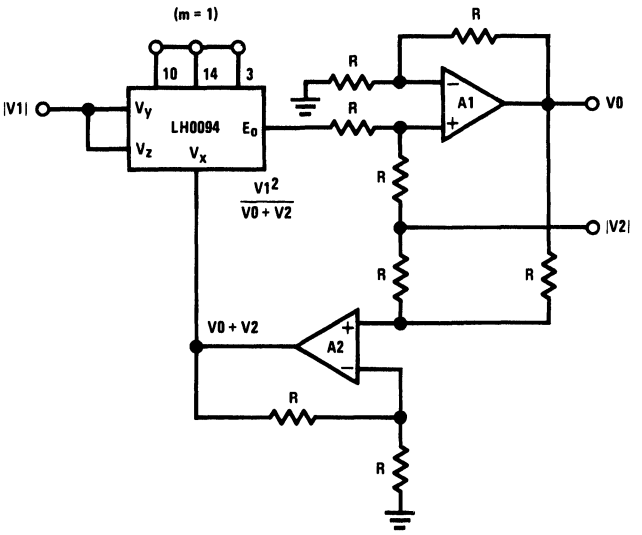


$m = \frac{R2}{R1 + R2}$; Choose R1 = 200Ω
$\therefore$ R2 = 50Ω

$m = \frac{R1 + R2}{R2}$; Choose R2 = 50Ω
$\therefore$ R1 = 200Ω

FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)



Note. The LH0094 may be used to generate a voltage equivalent to:

$V0=\sqrt{V1^2+V2^2}$

$V0=V2+\frac{V1^2}{V0+V2}$

$V0^2+V0\ V2=V2\ V0+V2^2+V1^2$

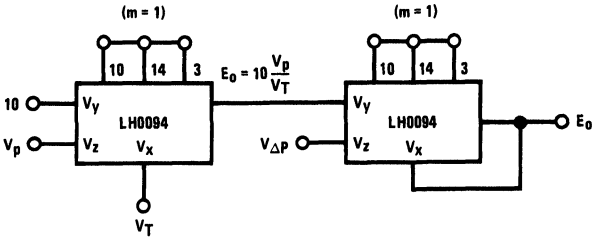
$V0^2=V1^2+V2^2$

$\therefore\ V0=\sqrt{V1^2+V2^2}$ V1, V2 0 ⟶ 10V

R ≈ 10k

National Semiconductor resistor array RA08—10k is recommended

FIGURE 12. Vector Magnitude Function



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Note. The LH0094 may be used in direct measurement of gas flow.

$\text{Flow}=k\sqrt{\frac{P\Delta P}{T}}$

$E_O=10\frac{V_P}{V_T}\times\frac{V_{\Delta P}}{E_O}$

$E_O^2=10\frac{V_P\,V_{\Delta P}}{VT}$

$E_O=\sqrt{10\frac{VP\,V_{\Delta P}}{VT}}$

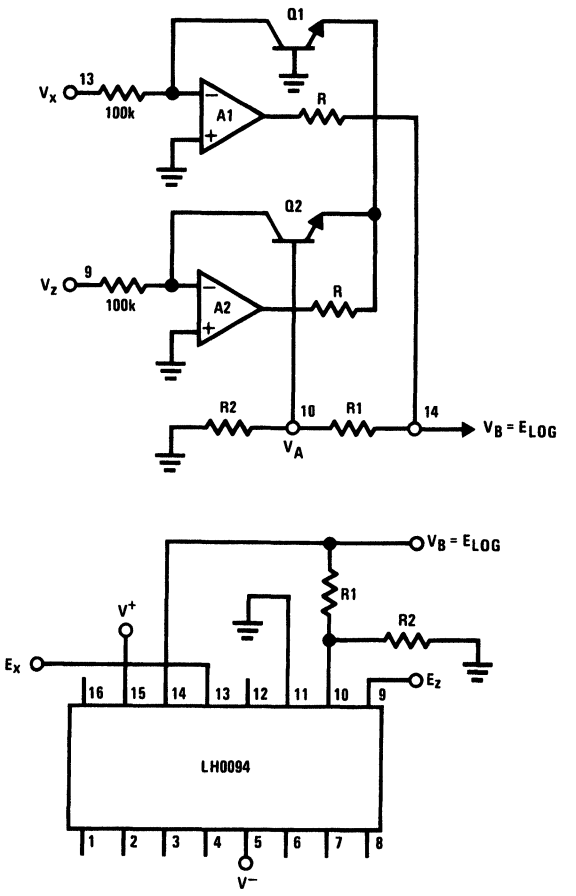
P = Absolute pressure

T = Absolute temperature

ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

Typical Applications (Continued)



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Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ell n \frac{V_Z}{V_X}$$

where $K1 = \frac{R1 + R2}{R2}$

If $K1 = \frac{1}{KT/q \ell n 10}$

then $E_{LOG} = \text{Log}_{10} \frac{V_Z}{V_X}$

$R1 = 15.9\ R2$

$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of $\approx$ 0.33%/°C to be compensated over temperature.

FIGURE 14. Log Amp Application

National Semiconductor

LM122/LM322/LM3905 Precision Timers

General Description

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A "logic reverse" circuit can be programmed by the user to make the output transistor either "on" or "off" during the timing period.

The **trigger** input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V—even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high gain PNP input transistors to achieve 300 pA typical input bias current over a common mode range of 0V to 3V. A **boost** terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3 μs to multi-hour timing range with excellent repeatability.

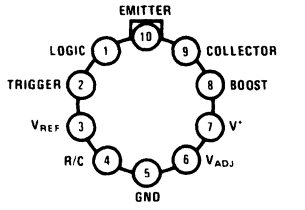
The LM122 operates over a temperature range of −55°C to +125°C. An electrically identical LM322 is specified from 0°C to +70°C. The LM3905 is identical to the LM122 series except that the **boost** and V_{ADJ} pin options are not available, limiting minimum timing period to 1 ms.

Features

- Immune to changes in trigger voltage during timing interval
- Timing periods from microseconds to hours
- Internal logic reversal
- Immune to power supply ripple during the timing interval
- Operates from 4.5V to 40V supplies
- Input protected to ±40V
- Floating transistor output with internal current limiting
- Internal regulated reference
- Timing period can be voltage controlled
- TTL compatible input and output

Connection Diagrams

Metal Can Package



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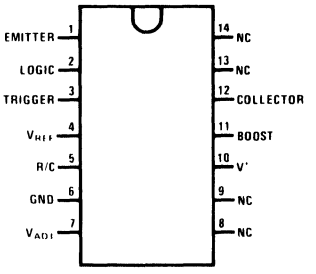
Top View
Order Number LM122H
See NS Package Number H10C

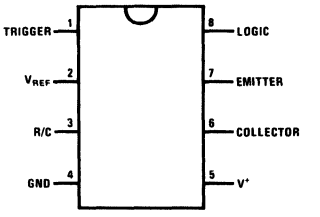
Dual-In-Line Package



TL/H/7768–7

Top View
Order Number LM322N
See NS Package Number N14A

Dual-In-Line Package



TL/H/7768–8

Top View
Order Number LM3905N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	500 mW
V^+ Voltage	40V
Collector Output Voltage	40V
V_{REF} Current	5 mA
Trigger Voltage	±40V
V_{ADJ} Voltage (Forced)	5V
Logic Reverse Voltage	5.5V
Output Short Circuit Duration (Note 1)	
Lead Temperature (Soldering, 10 sec.)	260°C
Operating Temperature Range	
LM122	$-55°C \le T_A \le +125°C$
LM322	$0°C \le T_A \le +70°C$
LM3905	$0°C \le T_A \le +70°C$

Electrical Characteristics (Note 2)

Parameter	Conditions	LM122			LM322			LM3905			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Timing Ratio	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	0.626	0.632	0.638	0.620	0.632	0.644	0.620	0.632	0.644	
	Boost Tied to V^+, (Note 3)	0.620	0.632	0.644	0.620	0.632	0.644				
Comparator Input Current	$T_A = 25°C$, $4.5V \le V^+ \le 40V$		0.3	1.0		0.3	1.5		0.5	1.5	nA
	Boost Tied to V^+		30	100		30	100				nA
Trigger Voltage	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	1.2	1.6	2	1.2	1.6	2	1.2	1.6	2	V
Trigger Current	$T_A = 25°C$, $V_{TRIG} = 2V$		25			25			25		μA
Supply Current	$T_A \ge 25°C$, $4.5V \le V^+ \le 40V$		2.5	4		2.5	4.5		2.5	4.5	mA
Timing Ratio	$4.5V \le V^+ \le 40V$	0.62		0.644	0.61		0.654	0.61		0.654	
	Boost Tied to V^+	0.62		0.644	0.61		0.654				
Comparator Input Current	$4.5V \le V^+ \le 40V$	−5		5	−2		2	−2.5		2.5	nA
	Boost Tied to V^+, (Note 4)			100			150				nA
Trigger Voltage	$4.5V \le V^+ \le 40V$	0.8		2.5	0.8		2.5	0.8		2.5	V
Trigger Current	$V_{TRIG} = 2.5V$			200			200			200	μA
Output Leakage Current	$V_{CE} = 40V$			1			5			5	μA
Capacitor Saturation Voltage	$R_t \ge 1\ M\Omega$		2.5			2.5			2.5		mV
	$R_t = 10\ k\Omega$		25			25			25		mV
Reset Resistance			150			150			150		Ω
Reference Voltage	$T_A = 25°C$	3	3.15	3.3	3	3.15	3.3	3	3.15	3.3	V
Reference Regulation	$0 \le I_{OUT} \le 3\ mA$		20	50		20	50		20	50	mV
	$4.5V \le V^+ \le 40V$		6	25		6	25		6	25	mV
Collector Saturation Voltage	$I_L = 8\ mA$		0.25	0.4		0.25	0.4		0.25	0.4	V
	$I_L = 50\ mA$		0.7	1.4		0.7	1.4		0.7	1.4	V
Emitter Saturation Voltage	$T_A = 25°C$, $I_L = 3\ mA$		1.8	2.2		1.8	2.2		1.8	2.2	V
	$T_A = 25°C$, $I_L = 50\ mA$		2.1	3		2.1	3		2.1	3	V
Average Temperature Coefficient of Timing Ratio			0.003			0.003			0.003		%/°C
Minimum Trigger Width	$V_{TRIG} = 3V$		0.25			0.25			0.25		μs

Note 1: Continuous output shorts are not allowed. Short circuit duration at ambient temperatures up to 40°C may be calculated from $t = 120/V_{CE}$ seconds, where V_{CE} is the collector to emitter voltage across the output transistor during the short.

Note 2: These specifications apply for $T_{AMIN} \le T_A \le T_{AMAX}$ unless otherwise noted.

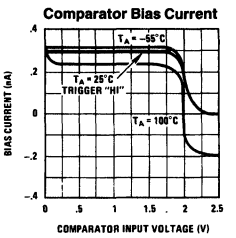
Note 3: Output pulse width can be calculated from the following equation: $t = (R_t)(C_t)[1 - 2(0.632 - r) - V_C/V_{REF})$ where r is timing ratio and V_C is capacitor saturation voltage. This reduces to $t = (R_t)(C_t)$ for all but the most critical applications.

Note 4: Sign reversal may occur at high temperatures (> 100°C) where comparator input current is predominately leakage. See typcial curves.

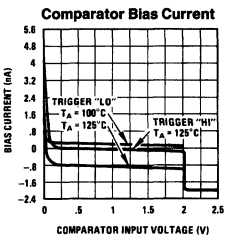
Note 5: Refer to RETS122X drawing of military LM122H version for specifications.

Typical Performance Characteristics

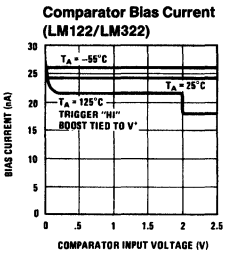
Comparator Bias Current



Comparator Bias Current



Comparator Bias Current (LM122/LM322)



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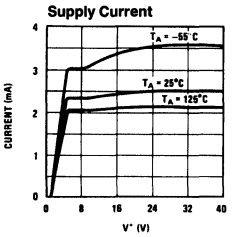
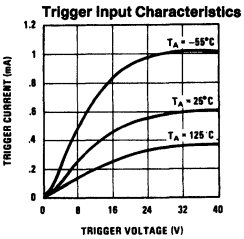
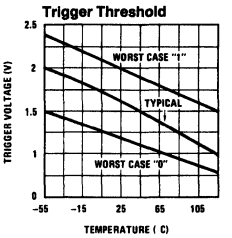
Supply Current



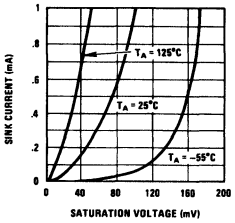
Trigger Input Characteristics



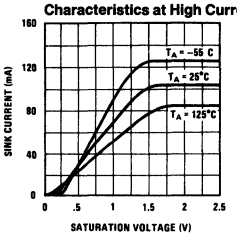
Trigger Threshold



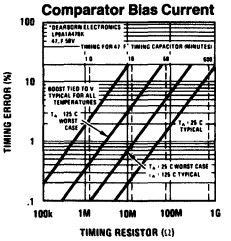
Output Transistor Saturation Characteristics at Low Currents



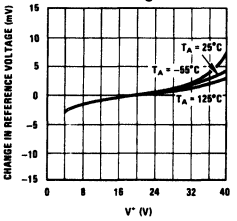
Collector Output Saturation Characteristics at High Current



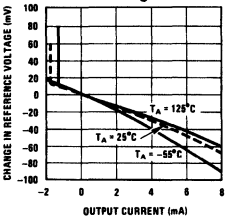
Timing Error Due to Comparator Bias Current



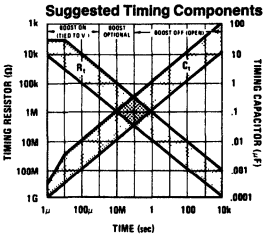
Reference Regulation



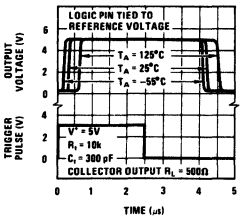
Reference Regulation



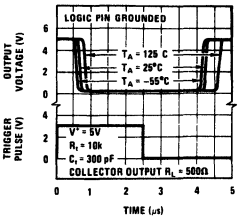
Suggested Timing Components



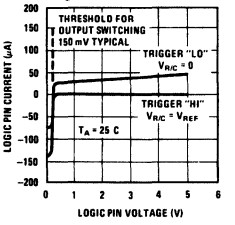
Short Output Pulse (LM122/LM322)



Short Output Pulse (LM122/LM322)



Logic Pin Characteristics



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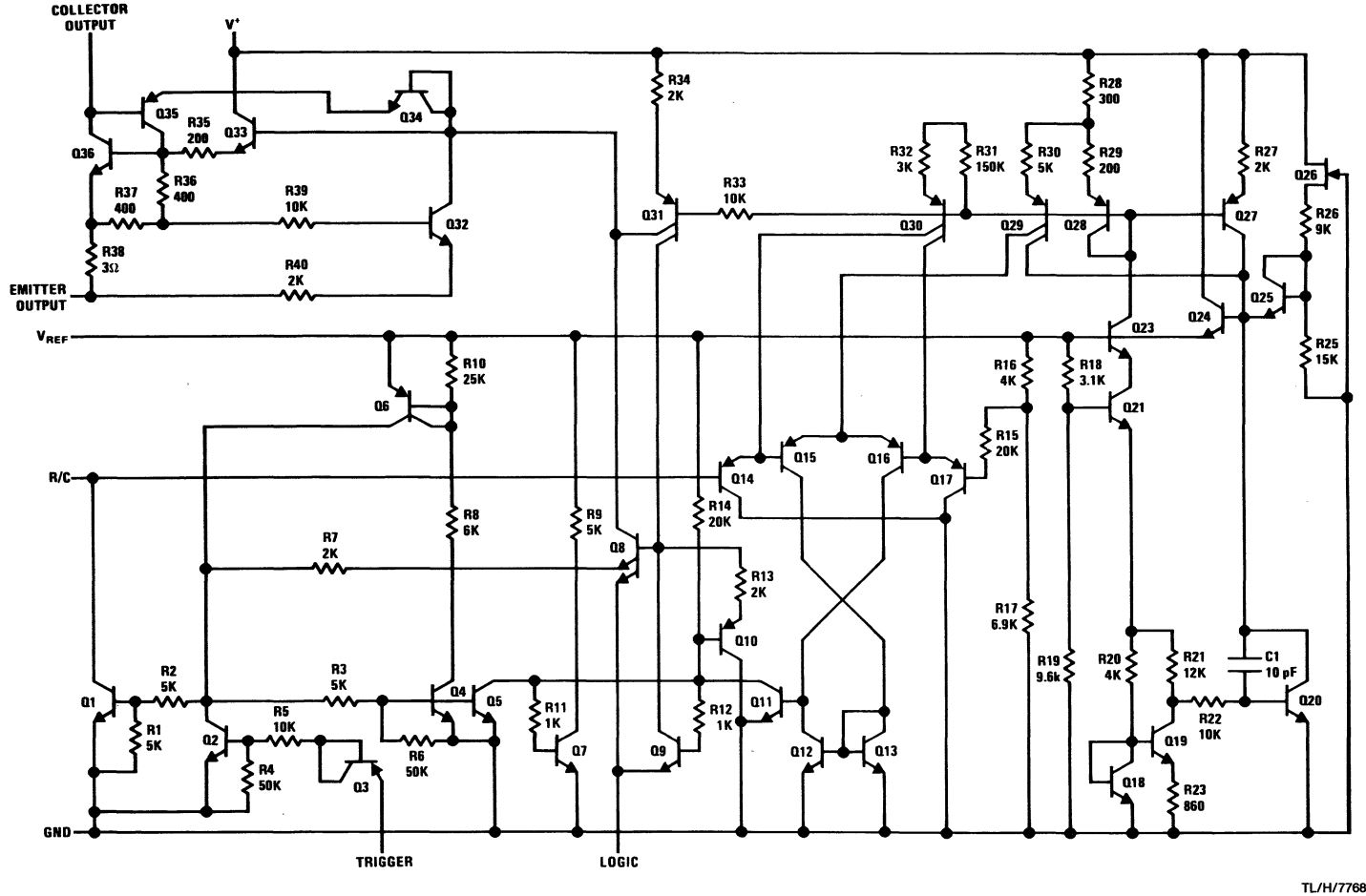
Schematic Diagram



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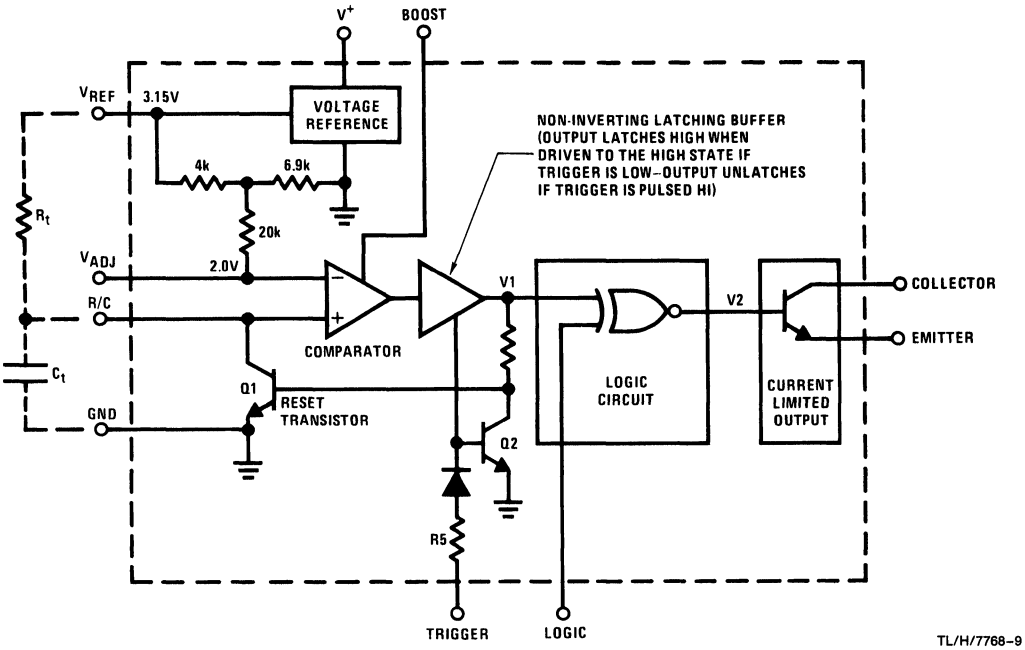
Functional Diagram



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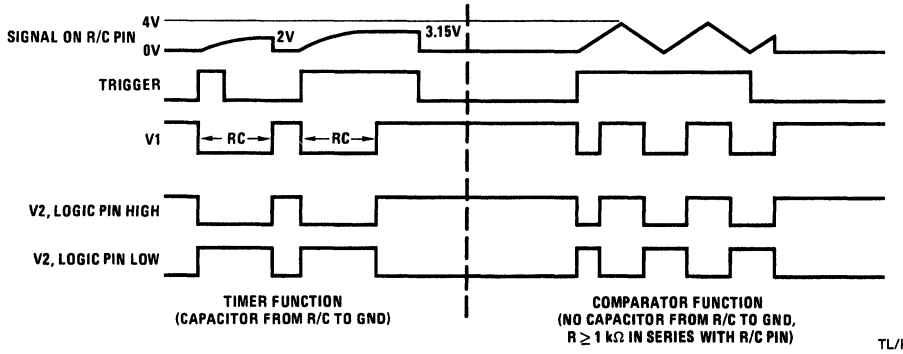
Timing Diagram



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Pin Function Description

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on V^+ is not generally needed but may be necessary when driving highly reactive loads.

Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature con-

Pin Function Description (Continued)

trollers. Typical temperature drift of the reference is less than 0.01%/°C.

The **trigger** terminal is used to start a timing cycle (see functional diagram). Initially, Q1 is saturated, C_t is discharged and the latching buffer output (V1) is latched high. A trigger pulse unlatches the buffer, V1 goes low and turns Q1 off. The timing capacitor C_t connected from R/C to GND will begin to charge. When the voltage at the R/C terminal reaches the 2.0V threshold of the comparator, the comparator toggles, latching the buffer output (V1) in the high state. This turns on Q1, discharges the capacitor C_t and the cycle is ready to begin again.

If the **trigger** is held high as the timing period ends, the comparator will toggle and V1 will go high exactly as before. However, V1 will not be latched and the capacitor will not discharge until the trigger again goes low. When the trigger goes low, V1 remains high but is now latched.

Trigger threshold is typically 1.6V at 25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the **trigger** source is typically 20 μA at threshold, rising to 600 μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region. The **trigger** can be driven from supplies as high as ±40V, even when device supply voltage is only 5V.

The **R/C** pin is tied to the non-inverting side of the comparator and to the collector of Q1. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). Q1 turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the **R/C** pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Current from the **R/C** pin is typically 300 pA when the voltage is negative with respect to the $\mathbf{V_{ADJ}}$ terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is typically 30 nA. Gain of the comparator is very high, 200,000 or more, depending on the state of the logic reverse pin and the connection of the output transistor.

The **ground** pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the $\mathbf{V^+}$ terminal. Level shifting may be necessary for the input **trigger** if the **trigger** voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the **ground** terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the **ground** pin of the LM122 was tied to a negative supply.

The terminal labled $\mathbf{V_{ADJ}}$ is tied to one side of the comparator and to a voltage divider between $\mathbf{V_{REF}}$ and **ground**. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to $\mathbf{V_{ADJ}}$. This resistor is a pinched type with a typical variation in nominal value of −50%, +100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between $\mathbf{V_{REF}}$ and **ground**) connected to $\mathbf{V_{ADJ}}$ should have a source resistance as low as possible. For small changes in $\mathbf{V_{ADJ}}$, up to several kΩ is all right, but for large variations, 250Ω or less should be maintained. This can be accomplished with a 1k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on $\mathbf{V_{ADJ}}$ from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The $\mathbf{V_{ADJ}}$ pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high, when the $\mathbf{V_{ADJ}}$ pin is grounded. In this case, the output changes state, but the capacitor does not discharge.

If the trigger drops while $\mathbf{V_{ADJ}}$ is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when $\mathbf{V_{ADJ}}$ is released, the output may or may not change state, depending on the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output. This pin is not available on the LM2905/LM3905.

In noisy environments or in comparator-type applications, a bypass capacitor on the $\mathbf{V_{ADJ}}$ terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1 μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The **emitter** and the **collector** outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the **emitter** is tied to the **ground** pin and the signal is taken from the **collector**, or the **collector** is tied to $\mathbf{V^+}$ and the signal is taken from the **emitter**. Variations on these basic connections are possible. The **collector** can be tied to any positive voltage up to 40V when the signal is taken from the **emitter**. However, the **emitter** will not be pulled higher than the supply voltage on the $\mathbf{V^+}$ pin. Connecting the **collector** to a voltage less than the $\mathbf{V^+}$ voltage is allowed. The **emitter** should not be connected to a low impedance load other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with **collector-emitter** voltages up to 40V. The power x time product, however, must not exceed 15 watt-seconds for power levels above the maximum rating of the package. A short to 30V,

Pin Function Description (Continued)

for instance, cannot be held for more than 4 seconds. These levels are based on 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A **boost** pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current.

For timing periods less than 1 ms, where low input current is not needed, comparator operating current can be increased several orders of magnitude. Shorting the boost terminal to **V**+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5 μA. This pin is not available on the LM3905.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used. The 800 ns error is relatively insensitive to temperature, so temperature coefficient of pulse width is still good.

The **Logic** pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the **logic** pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the **logic** pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the **logic** pin is typically 100 mV with 150 μA flowing out of the terminal. If an active drive to the **logic** pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 25 mV at 200 μA is required. Minimum and maximum voltages that may appear on the **logic** pin are 0 and +5.0, respectively.

Typical Applications

Basic Timers

Figure 1 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch along side *Figure 1*. Note that the trigger pulse may be either shorter or longer than the output pulse width.

Figure 2 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

Simulating a Thermal Delay Relay

Figure 3 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 4* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.

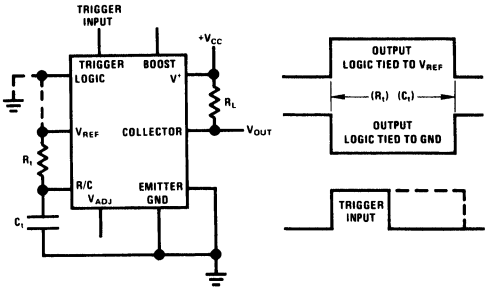

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FIGURE 1. Basic Timer-Collector Output and Timing Chart

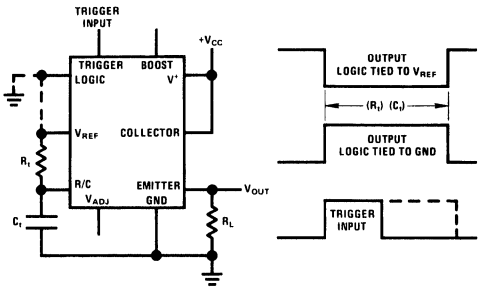

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FIGURE 2. Basic Timer-Emitter Output and Timing Chart

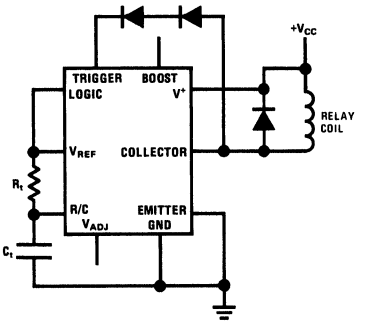

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FIGURE 3. Time Out on Power Up (Relay Energized R_t C_t Seconds after V_{CC} is Applied)

+5V Supply Driving 28V Relay

Figure 5 shows the timer interfacing 5V logic to a high voltage relay. Although the V+ terminal could be tied to the +28V supply, this may be an unnecessary waste of power in the IC or require extra wiring if the LM122 is on a logic card. In either case, the threshold for the trigger is 1.6V.

Typical Applications (Continued)

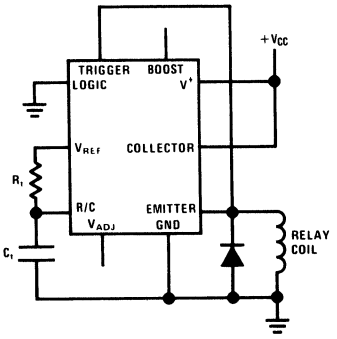

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FIGURE 4. Time Out on Power Up (Relay Energized *Until* R_t C_t Seconds After V_{CC} is Applied)

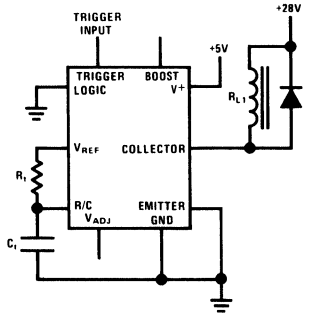

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FIGURE 5. 5V Logic Supply Driving 28V Relay

30V Supply Interfacing with 5V Logic

Figure 6 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL. If the logic is sensitive to rise/fall time of the trailing edge of the output pulse, the trigger pin should be low at that time.

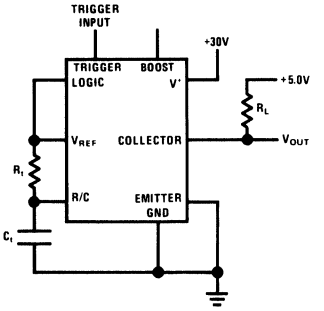

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FIGURE 6. 30V Supply Interfacing with 5V Logic

Astable Operation

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in *Figure 7*. Operating frequency is $1/(R_t + R_1)(C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2$ C_f. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t \geq 500k$.

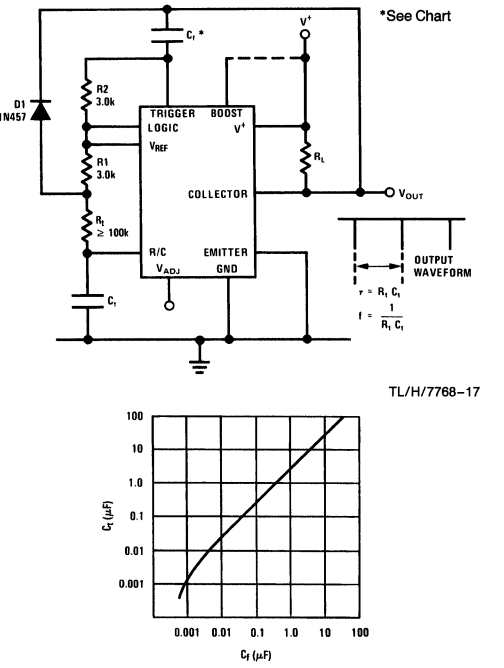

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FIGURE 7. Oscillator

One Hour Timer with Reset and Manual Cycle End

Figure 8 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released.

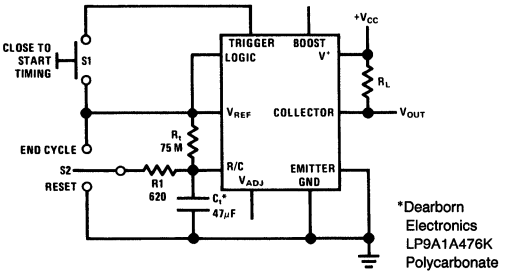

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FIGURE 8. One Hour Timer with Reset and Manual Cycle End

Typical Applications (Continued)

The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

Two Terminal Time Delay Switch

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In *Figure 9*, the timer is used to drive a relay "on" $R_t \bullet C_t$ seconds after application of power. "Off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

Zero Power Dissipation Between Timing Intervals

In some applications it is desirable to reduce supply current drain to zero between timing cycles. In *Figure 10* this is accomplished by using an external PNP as a latch to drive the V^+ pin of the timer.

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents the step on the V^+ pin from coupling back into the trigger pin. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.

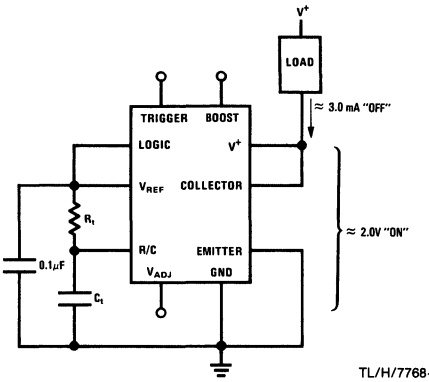

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FIGURE 9. 2-Terminal Time Delay Switch

Frequency to Voltage Converter

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 11*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

Pulse Width Detector

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made *(Figure 12)*.

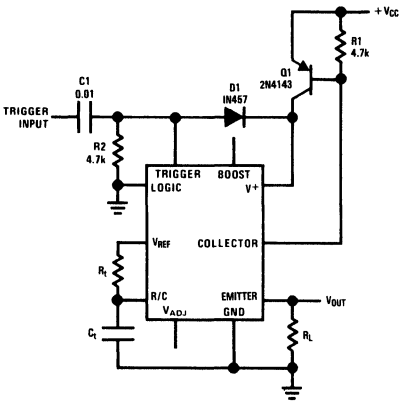

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FIGURE 10. Zero Power Dissipation Between Timing Intervals

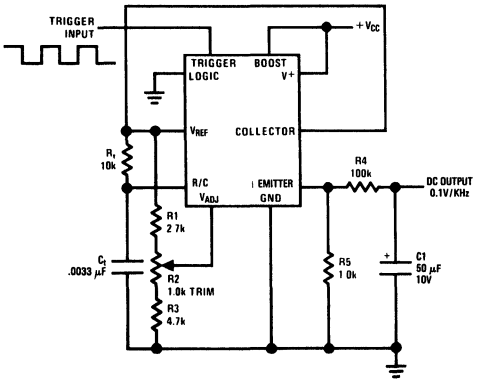

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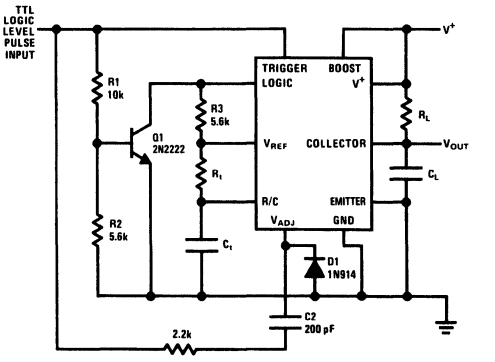
FIGURE 11. Frequency to Voltage Converter. (Tachometer) Output Independent of Supply Voltage.



TL/H/7768–23

*V_{OUT} = 0 for W R_1 C_1

Pulse Out = W − R_1 C_1 for W R_1 C_1

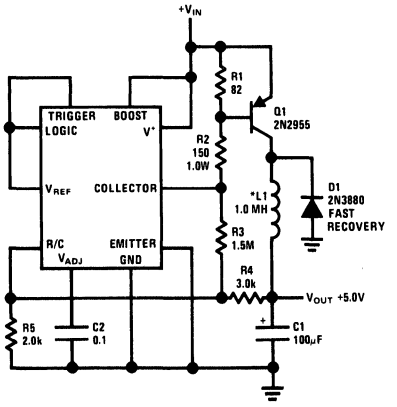
FIGURE 12. Pulse Width Detector

Typical Applications (Continued)

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \bullet C_t$. C2 insures no output pulse for short (<RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to propagation delays during switching.

5V Switching Regulator

Figure 13 is an application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP transistor switch. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.



*No. 22 Wire Wound on Molybdenum Permalloy Core TL/H/7768–24

FIGURE 13. 5V Switching Regulator with 1 Amp Output and 5.5V Minimum Input

Application Hints

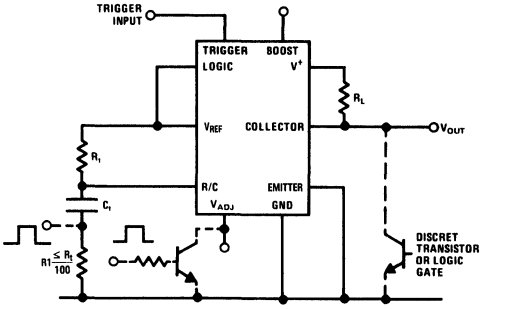
Aborting a Timing Cycle

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300 μA.

A timing cycle may also be ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.



TL/H/7768–25

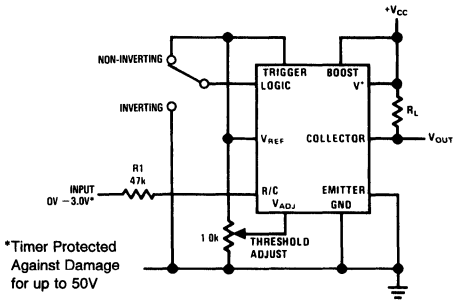
FIGURE 14. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25 μV/°C in the boosted mode and 50 μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in *Figure 15*. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply with internal reference should make this comparator very useful.

Application Hints (Continued)

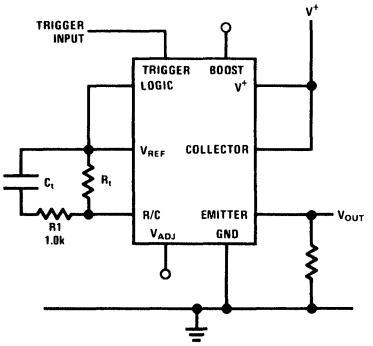


TL/H/7768–26

FIGURE 15. Comparator with 0V to 3V Threshold

Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will normally start a timing cycle (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 16*. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

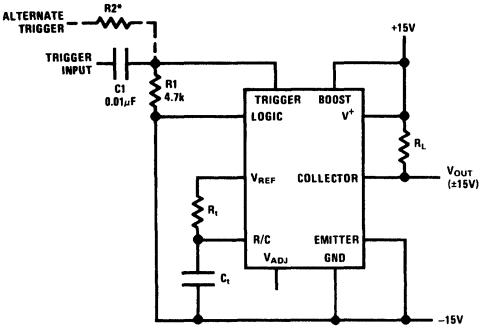


TL/H/7768–27

FIGURE 16. Eliminating Initial Timing Cycle

Using Dual Supplies

The LM122 can be operated off dual supplies as shown in *Figure 17*. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



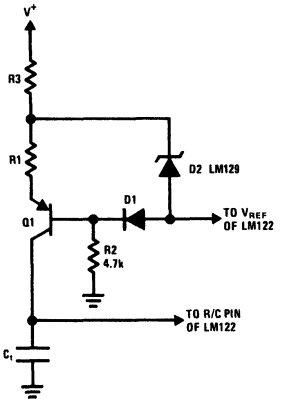
TL/H/7768–28

*Select for Proper Level Shift
Emitter Terminal or Emitter Load must be Tied to GND Pin of Timer

FIGURE 17. Operating Off Dual Supplies

Linearizing the Charging Sweep

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in *Figure 18*.



TL/H/7768–29

FIGURE 18. Temperature Compensated Linear Charging Sweep

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability is not critical. With D1, D2, R2 and R3 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

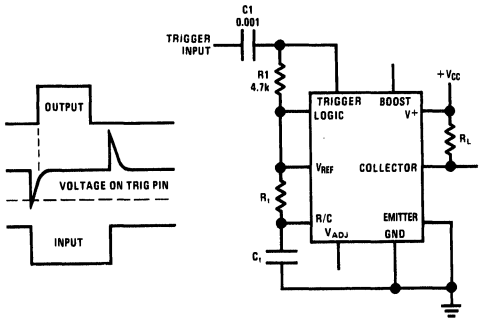
8

Application Hints (Continued)

Triggering with Negative Edge

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In *Figure 19*, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with *Figure 21* shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately (0.5 to 1.5) (R1 • C1) depending on the trigger amplitude, or about 2.5 to 7.5 μs with the values shown. This time will have to be increased for C_t larger than 0.01 μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

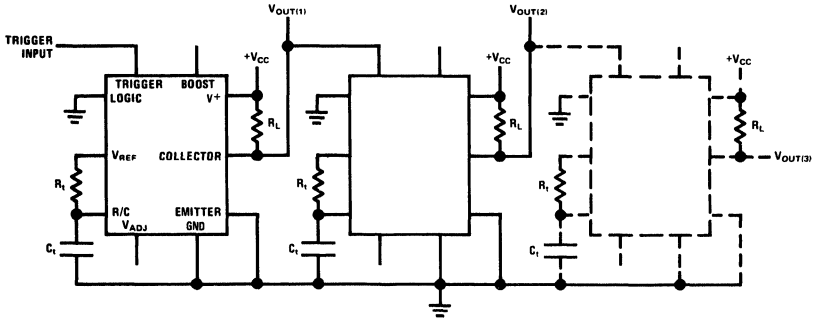


TL/H/7768–30

FIGURE 19. Timer Triggered by Negative Edge of Input Pulse

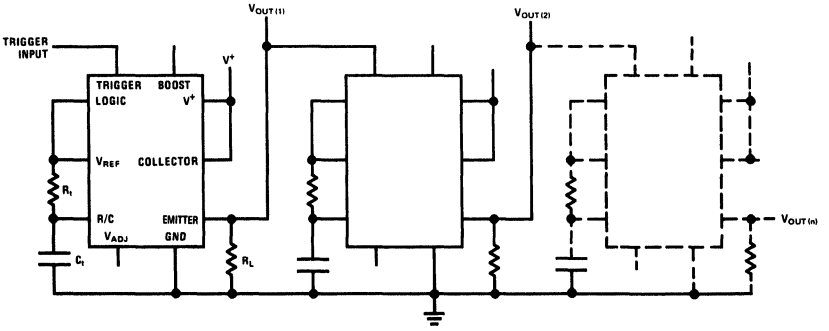
Chain of Timers

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 20A* and *20B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of the timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.

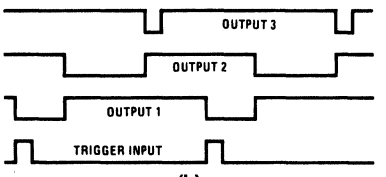


TL/H/7768–31

(a)



TL/H/7768–32



TL/H/7768–33

(b)

FIGURE 20. Chain of Timers

National Semiconductor

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1 μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM394/LM394B/LM394C are available in an 8-pin plastic dual-in-line package. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

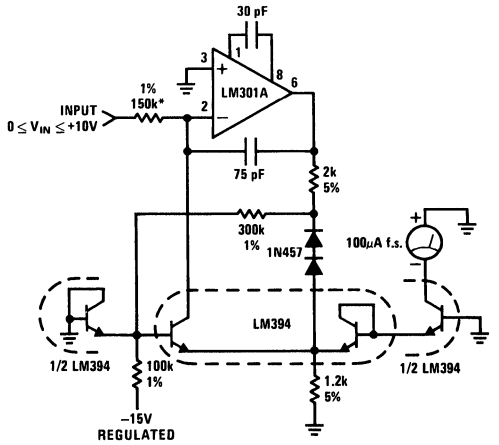
Features

- Emitter-base voltage matched to 50 μV
- Offset voltage drift less than 0.1 μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1 μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

Typical Applications

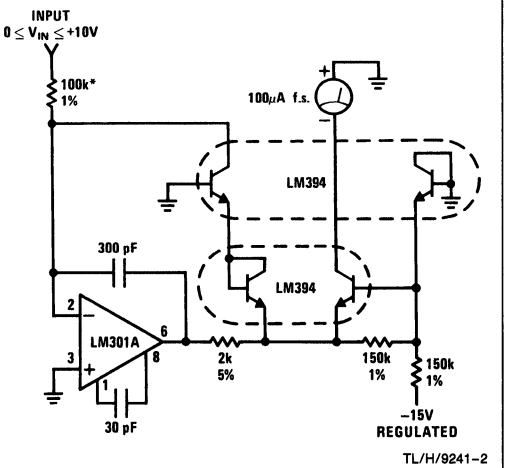
Low Cost Accurate Square Root Circuit

$I_{OUT} = 10^{-5} \cdot \sqrt{10\ V_{IN}}$



Low Cost Accurate Squaring Circuit

$I_{OUT} = 10^{-6} (V_{IN})^2$



TL/H/9241–1

*Trim for full scale accuracy

TL/H/9241–2

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Collector Current	20 mA
Collector-Emitter Voltage	V_{MAX}
Collector-Emitter Voltage	35V
LM394C	20V
Collector-Base Voltage	35V
LM394C	20V
Collector-Substrate Voltage	35V
LM394C	20V
Collector-Collector Voltage	35V
LM394C	20V
Base-Emitter Current	±10 mA
Power Dissipation	500 mW
Junction Temperature	
LM194	−55°C to +125°C
LM394/LM394B/LM394C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Metal Can Package (10 sec.)	260°C
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_J = 25°C)

Parameter	Conditions	LM194			LM394			LM394B/394C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Current Gain (h_{FE})	V_{CB} = 0V to V_{MAX} (Note 1)										
	I_C = 1 mA	350	700		300	700		225	500		
	I_C = 100 μA	350	550		250	550		200	400		
	I_C = 10 μA	300	450		200	450		150	300		
	I_C = 1 μA	200	300		150	300		100	200		
Current Gain Match, (h_{FE} Match) $= \frac{100\ [\Delta I_B]\ [h_{FE(MIN)}]}{I_C}$	V_{CB} = 0V to V_{MAX}										
	I_C = 10 μA to 1 mA		0.5	2		0.5	4		1.0	5	%
	I_C = 1 μA		1.0			1.0			2.0		%
Emitter-Base Offset Voltage	V_{CB} = 0 I_C = 1 μA to 1 mA		25	100		25	150		50	200	μV
Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR)	(Note 1) I_C = 1 μA to 1 mA, V_{CB} = 0V to V_{MAX}		10	25		10	50		10	100	μV
Change in Emitter-Base Offset Voltage vs Collector Current	V_{CB} = 0V, I_C = 1 μA to 0.3 mA		5	25		5	50		5	50	μV
Emitter-Base Offset Voltage Temperature Drift	I_C = 10 μA to 1 mA (Note 2)		0.08	0.3		0.08	1.0		0.2	1.5	μV/°C
	$I_{C1} = I_{C2}$ V_{OS} Trimmed to 0 at 25°C		0.03	0.1		0.03	0.3		0.03	0.5	μV/°C
Logging Conformity	I_C = 3 nA to 300 μA, V_{CB} = 0, (Note 3)		150			150			150		μV
Collector-Base Leakage	$V_{CB} = V_{MAX}$		0.05	0.25		0.05	0.5		0.05	0.5	nA
Collector-Collector Leakage	$V_{CC} = V_{MAX}$		0.1	2.0		0.1	5.0		0.1	5.0	nA
Input Voltage Noise	I_C = 100 μA, V_{CB} = 0V, f = 100 Hz to 100 kHz		1.8			1.8			1.8		nV/$\sqrt{Hz}$
Collector to Emitter Saturation Voltage	I_C = 1 mA, I_B = 10 μA		0.2			0.2			0.2		V
	I_C = 1 mA, I_B = 100 μA		0.1			0.1			0.1		V

Note 1: Collector-base voltage is swept from 0 to V_{MAX} at a collector current of 1 μA, 10 μA, 100 μA, and 1 mA.

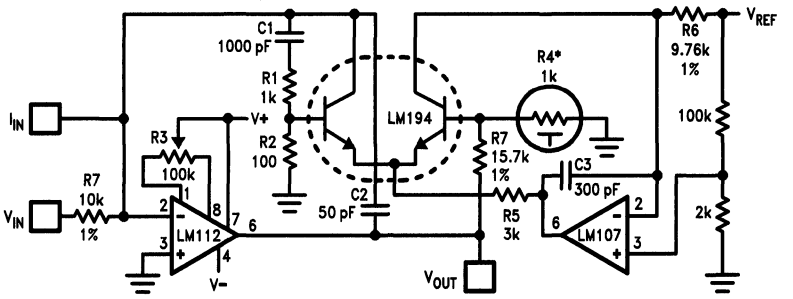
Note 2: Offset voltage drift with V_{OS} = 0 at T_A = 25°C is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at +25°C and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

Note 4: Refer to RETS194X drawing of military LM194H version for specifications.

Typical Applications (Continued)

Fast, Accurate Logging Amplifier, V_{IN} = 10V to 0.1 mV or I_{IN} = 1 mA to 10 nA

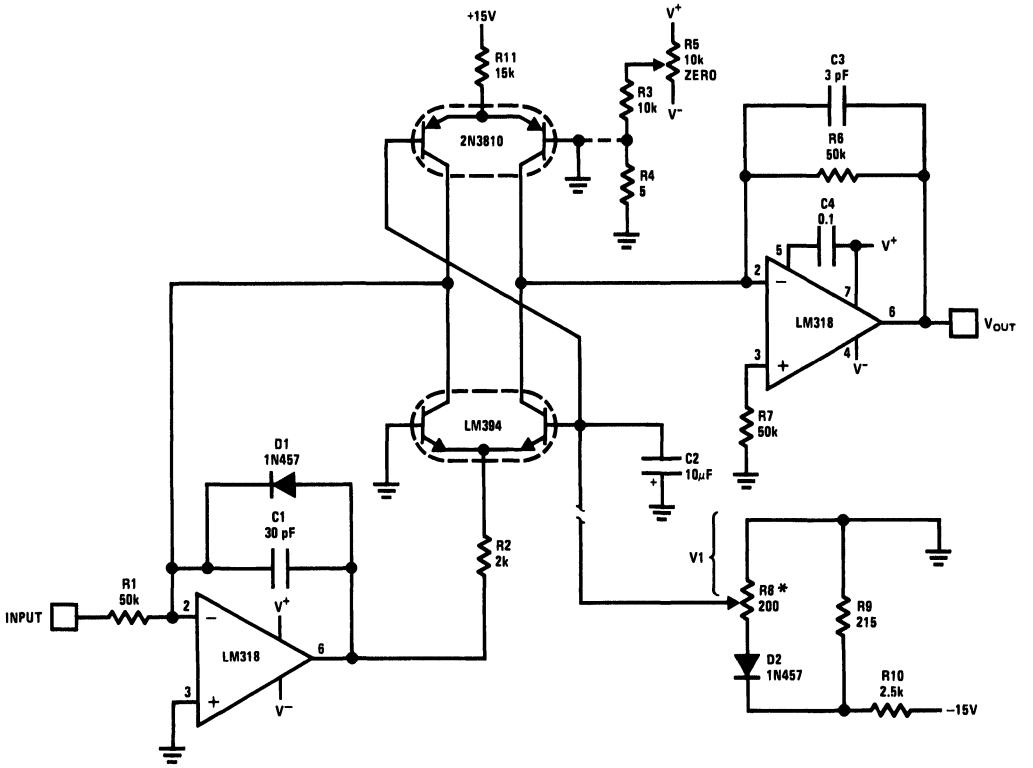


TL/H/9241–3

*1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

$$V_{OUT} = -\log_{10}\left(\frac{V_{IN}}{V_{REF}}\right)$$

Voltage Controlled Variable Gain Amplifier



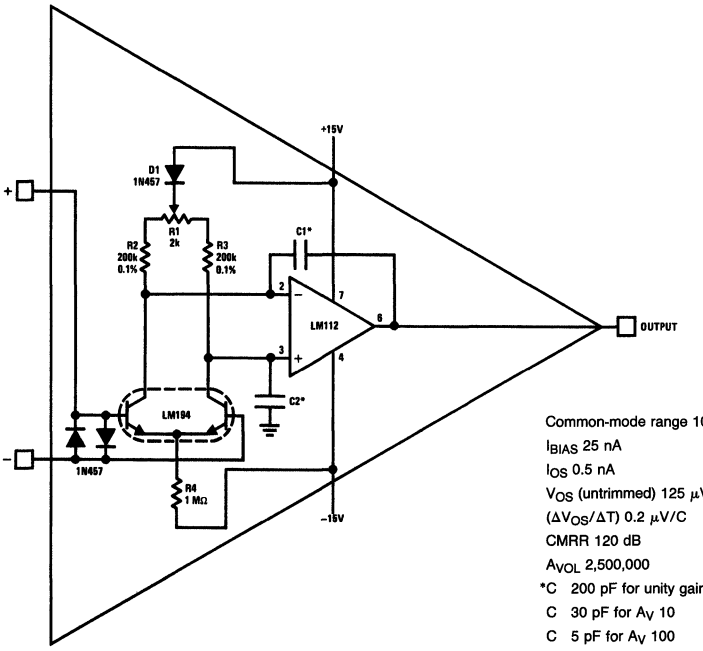
TL/H/9241–4

*R8–R10 and D2 provide a temperature independent gain control.
G = −336 V1 (dB)

Distortion < 0.1%
Bandwidth > 1 MHz
100 dB gain range

Typical Applications (Continued)

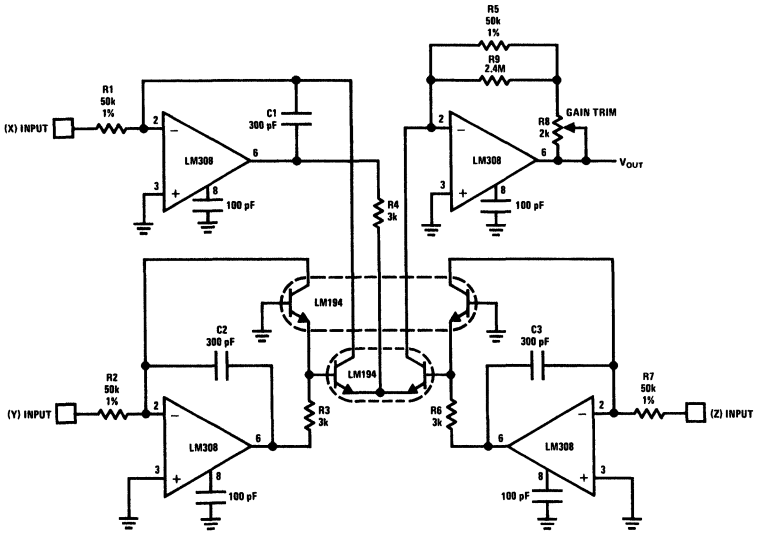
Precision Low Drift Operational Amplifier



Common-mode range 10V
I_{BIAS} 25 nA
I_{OS} 0.5 nA
V_{OS} (untrimmed) 125 μV
$(\Delta V_{OS}/\Delta T)$ 0.2 μV/C
CMRR 120 dB
A_{VOL} 2,500,000
*C 200 pF for unity gain
C 30 pF for A_V 10
C 5 pF for A_V 100
C 0 pF for A_V 1000

TL/H/9241–5

High Accuracy One Quadrant Multiplier/Divider



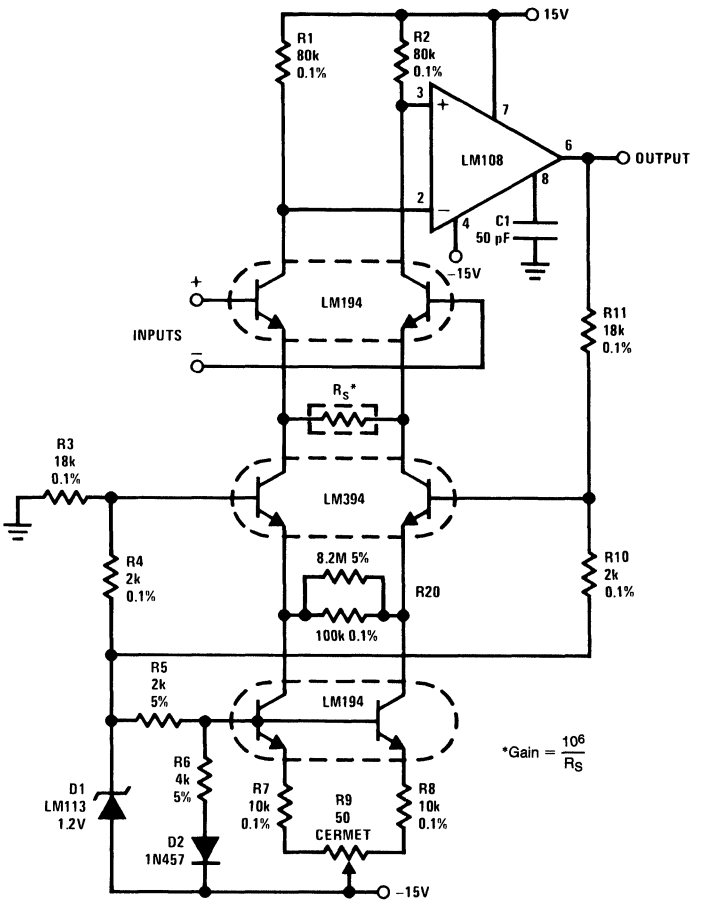
TL/H/9241–6

$V_{OUT} = \frac{(X)(Y)}{(Z)}$; positive inputs only.

*Typical linearity 0.1%

Typical Applications (Continued)

High Performance Instrumentation Amplifier



TL/H/9241–7

Performance Characteristics

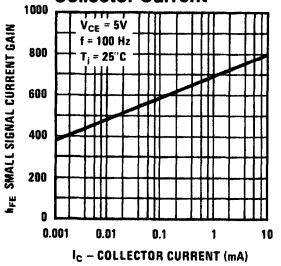
	G = 10,000	G = 1,000	G = 100	G = 10	
Linearity of Gain (±10V Output)	≤0.01	≤0.01	≤0.02	≤0.05	%
Common-Mode Rejection Ratio (60 Hz)	≥120	≥120	≥110	≥90	dB
Common-Mode Rejection Ratio (1 kHz)	≥110	≥110	≥90	≥70	dB
Power Supply Rejection Ratio					
+Supply	>110	>110	>110	>110	dB
−Supply	>110	>110	>90	>70	dB
Bandwidth (−3 dB)	50	50	50	50	kHz
Slew Rate	0.3	0.3	0.3	0.3	V/μs
Offset Voltage Drift**	≤0.25	≤0.4	2	≤10	μV/°C
Common-Mode Input Resistance	$>10^9$	$>10^9$	$>10^9$	$>10^9$	Ω
Differential Input Resistance	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	Ω
Input Referred Noise (100 Hz ≤ f ≤ 10 kHz)	5	6	12	70	$\frac{nV}{\sqrt{Hz}}$
Input Bias Current	75	75	75	75	nA
Input Offset Current	1.5	1.5	1.5	1.5	nA
Common-Mode Range	±11	±11	±11	±10	V
Output Swing (R_L = 10 kΩ)	±13	±13	±13	±13	V

**Assumes ≤ 5 ppm/°C tracking of resistors

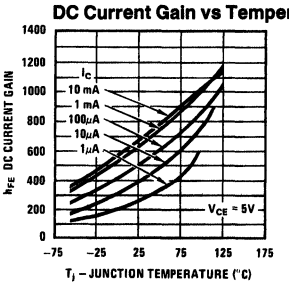
8

Typical Performance Characteristics

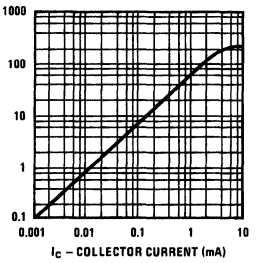
Small Signal Current Gain vs Collector Current



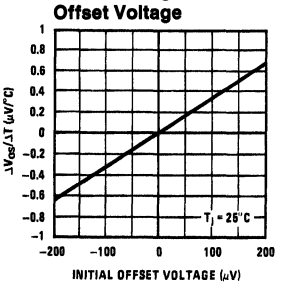
DC Current Gain vs Temperature



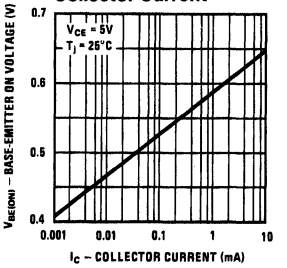
Unity Gain Frequency (f_t) vs Collector Current



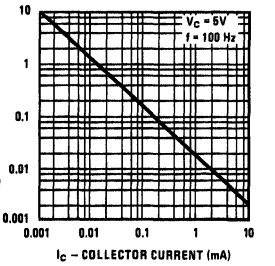
Offset Voltage Drift vs Initial Offset Voltage



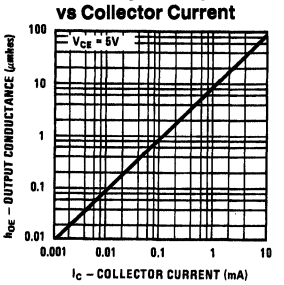
Base-Emitter On Voltage vs Collector Current



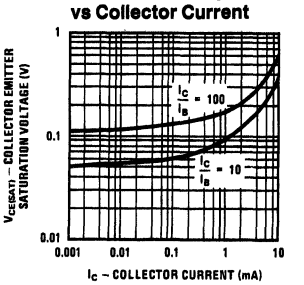
Small Signal Input Resistance (h_{ie}) vs Collector Current



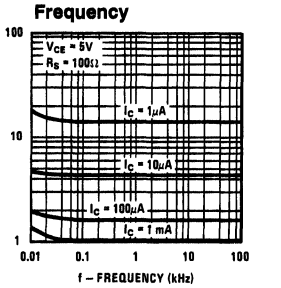
Small Signal Output Conductance vs Collector Current



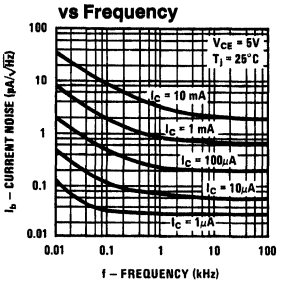
Collector-Emitter Saturation Voltage vs Collector Current



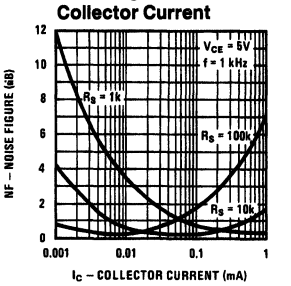
Input Voltage Noise vs Frequency



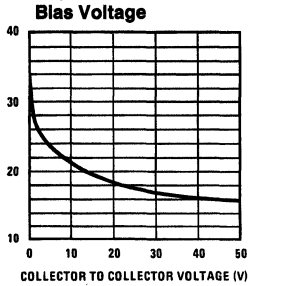
Base Current Noise vs Frequency



Noise Figure vs Collector Current



Collector to Collector Capacitance vs Reverse Bias Voltage



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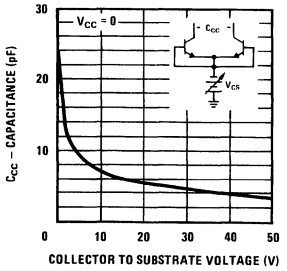
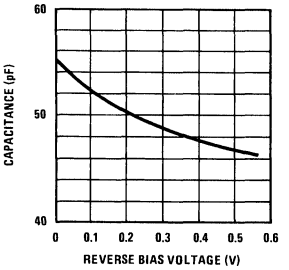
Typical Performance Characteristics (Continued)

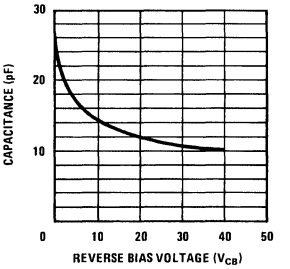
Collector to Collector Capacitance vs Collector-Substrate Voltage



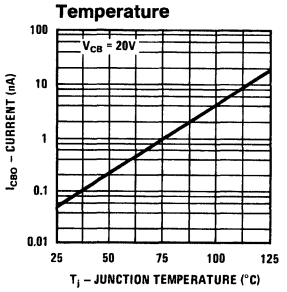
Emitter-Base Capacitance vs Reverse Bias Voltage



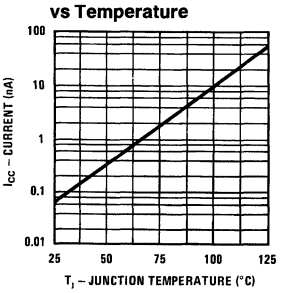
Collector-Base Capacitance vs Reverse Bias Voltage



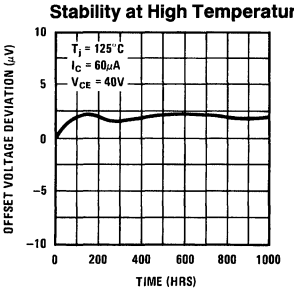
Collector-Base Leakage vs Temperature



Collector to Collector Leakage vs Temperature



Offset Voltage Long Term Stability at High Temperature



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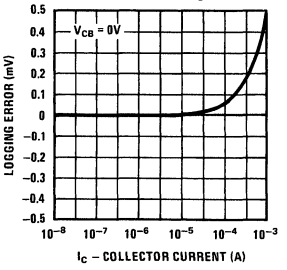
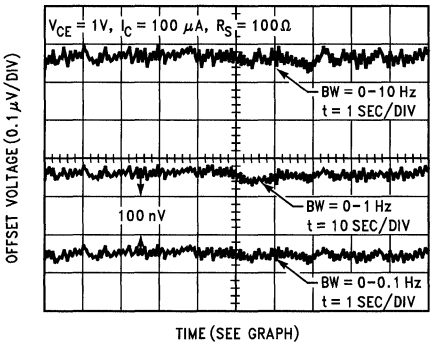
Emitter-Base Log Conformity



TL/H/9241–10

Low Frequency Noise of Differential Pair*



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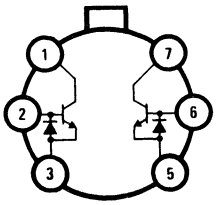
*Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

Connection Diagrams

Metal Can Package



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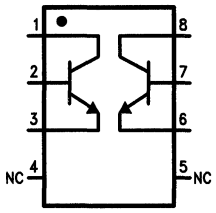
Top View

Order Number LM194H, LM194H/883*, LM394H, LM394BH or LM394CH
See NS Package Number H06C

Dual-In-Line and Small Outline Packages



TL/H/9241–13

Top View

Order Number LM394N or LM394CN
See NS Package Number N08E

*Available per SMD #5962-8777701

National Semiconductor

LM195/LM295/LM395 Ultra Reliable Power Transistors

General Description

The LM195/LM295/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

For low-power applications (under 100 mA), refer to the LP395 Ultra Reliable Power Transistor.

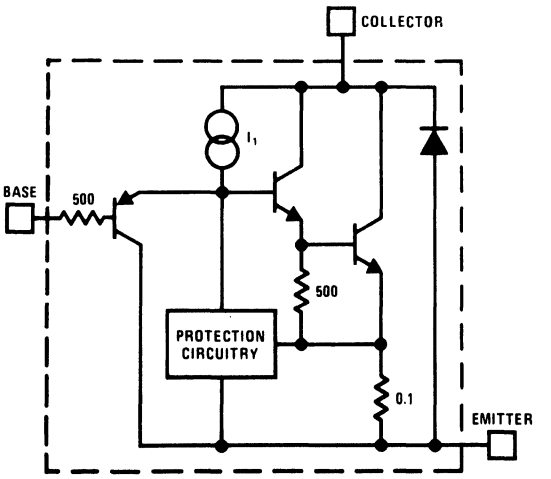
The LM195/LM295/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from −55°C to +150°C, the LM295 from −25°C to +150°C and the LM395 from 0°C to +125°C.

Features

- Internal thermal limiting
- Greater than 1.0A output current
- 3.0 μA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

Simplified Circuit

Simplified Circuit of the LM195



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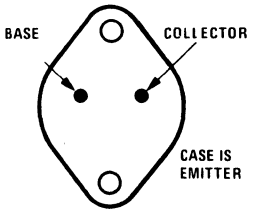
Connection Diagrams

TO-3 Metal Can Package

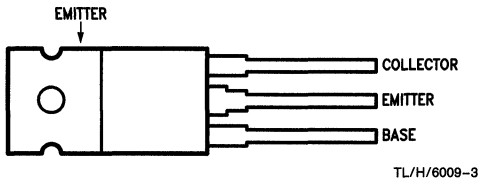


TL/H/6009-2

Bottom View

**Order Number LM195K,
LM295K or LM395K
See NS Package Number K02A**

TO-220 Plastic Package



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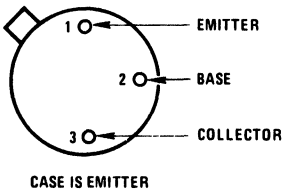
Case is Emitter

Top View

**Order Number LM395T
See NS Package Number T03B**

TO-5 Metal Can Package

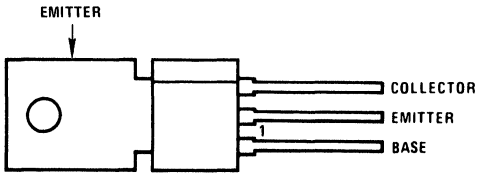


TL/H/6009-4

Bottom View

**Order Number LM195H,
LM295H or LM395H
See NS Package Number H03B**

TO-202 Plastic Package



TL/H/6009-5

Top View

**Order Number LM395P
See NS Package Number P03A**

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Collector to Emitter Voltage
- LM195, LM295 — 42V
- LM395 — 36V

Collector to Base Voltage
- LM195, LM295 — 42V
- LM395 — 36V

Base to Emitter Voltage (Forward)
- LM195, LM295 — 42V
- LM395 — 36V

Base to Emitter Voltage (Reverse) — 20V

Collector Current — Internally Limited

Power Dissipation — Internally Limited

Operating Temperature Range
- LM195 — −55°C to +150°C
- LM295 — −25°C to +150°C
- LM395 — 0°C to +125°C

Storage Temperature Range — −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) — 260°C

Preconditioning

100% Burn-In In Thermal Limit

Electrical Characteristics (Note 1)

Parameter	Conditions	LM195, LM295			LM395			Units
		Min	Typ	Max	Min	Typ	Max	
Collector-Emitter Operating Voltage (Note 3)	$I_Q \le I_C \le I_{MAX}$			42			36	V
Base to Emitter Breakdown Voltage	$0 \le V_{CE} \le V_{CEMAX}$	42			36	60		V
Collector Current								
TO-3, TO-220	$V_{CE} \le 15V$	1.2	2.2		1.0	2.2		A
TO-5, TO-202	$V_{CE} \le 7.0V$	1.2	1.8		1.0	1.8		A
Saturation Voltage	$I_C \le 1.0A$, $T_A = 25°C$		1.8	2.0		1.8	2.2	V
Base Current	$0 \le I_C \le I_{MAX}$ $0 \le V_{CE} \le V_{CEMAX}$		3.0	5.0		3.0	10	μA
Quiescent Current (I_Q)	$V_{be} = 0$ $0 \le V_{CE} \le V_{CEMAX}$		2.0	5.0		2.0	10	mA
Base to Emitter Voltage	$I_C = 1.0A$, $T_A = +25°C$		0.9			0.9		V
Switching Time	$V_{CE} = 36V$, $R_L = 36\Omega$, $T_A = 25°C$		500			500		ns
Thermal Resistance Junction to Case (Note 2)	TO-3 Package (K)		2.3	3.0		2.3	3.0	°C/W
	TO-5 Package (H)		12	15		12	15	°C/W
	TO-220 Package (T)					4	6	°C/W
	TO-202 Package (P)					12	15	°C/W

Note 1: Unless otherwise specified, these specifications apply for $-55°C \le T_j \le +150°C$ for the LM195, $-25°C \le T_j \le +150°C$ for the LM295 and $0°C \le +125°C$ for the LM395.

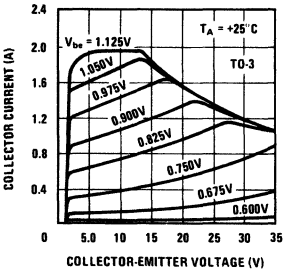
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about +150°C/W, while that of the TO-3 package is +35°C/W.

Note 3: Selected devices with higher breakdown available.

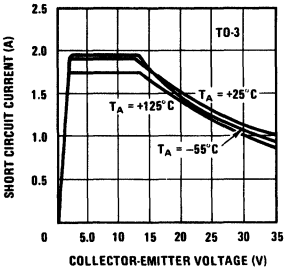
Note 4: Refer to RETS195H and RETS195K drawings of military LM195H and LM195K versions for specifications.

Typical Performance Characteristics (for K and T Packages)

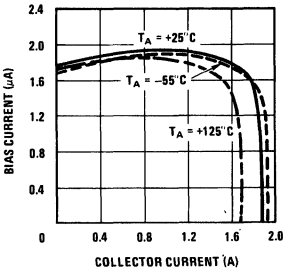
Collector Characteristics



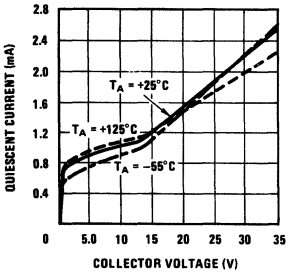
Short Circuit Current



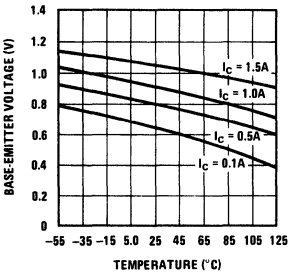
Bias Current



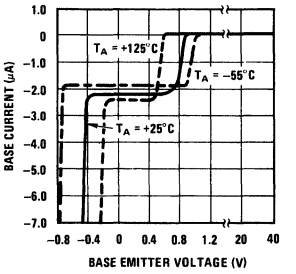
Quiescent Current



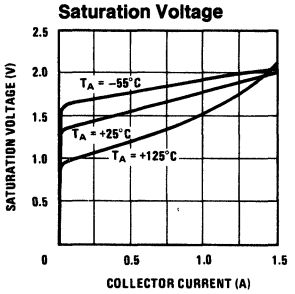
Base Emitter Voltage



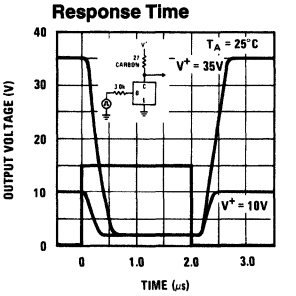
Base Current



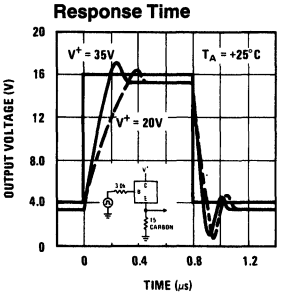
Saturation Voltage



Response Time



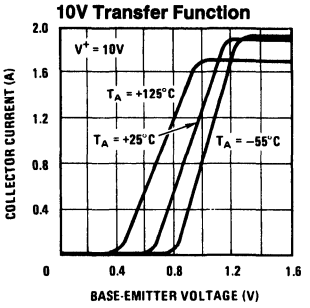
Response Time



TL/H/6009–6

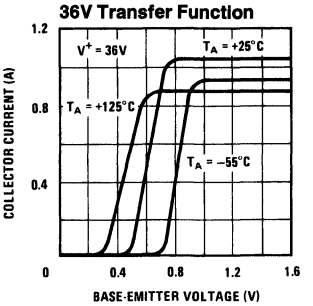
Typical Performance Characteristics (for K and T Packages) (Continued)

10V Transfer Function



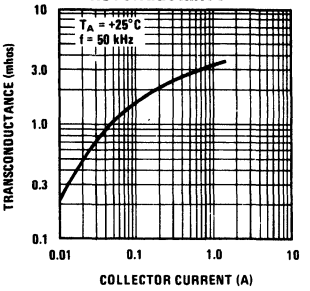
TL/H/6009–7

36V Transfer Function



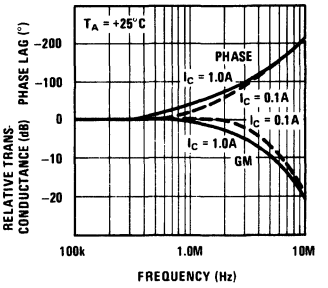
TL/H/6009–8

Transconductance



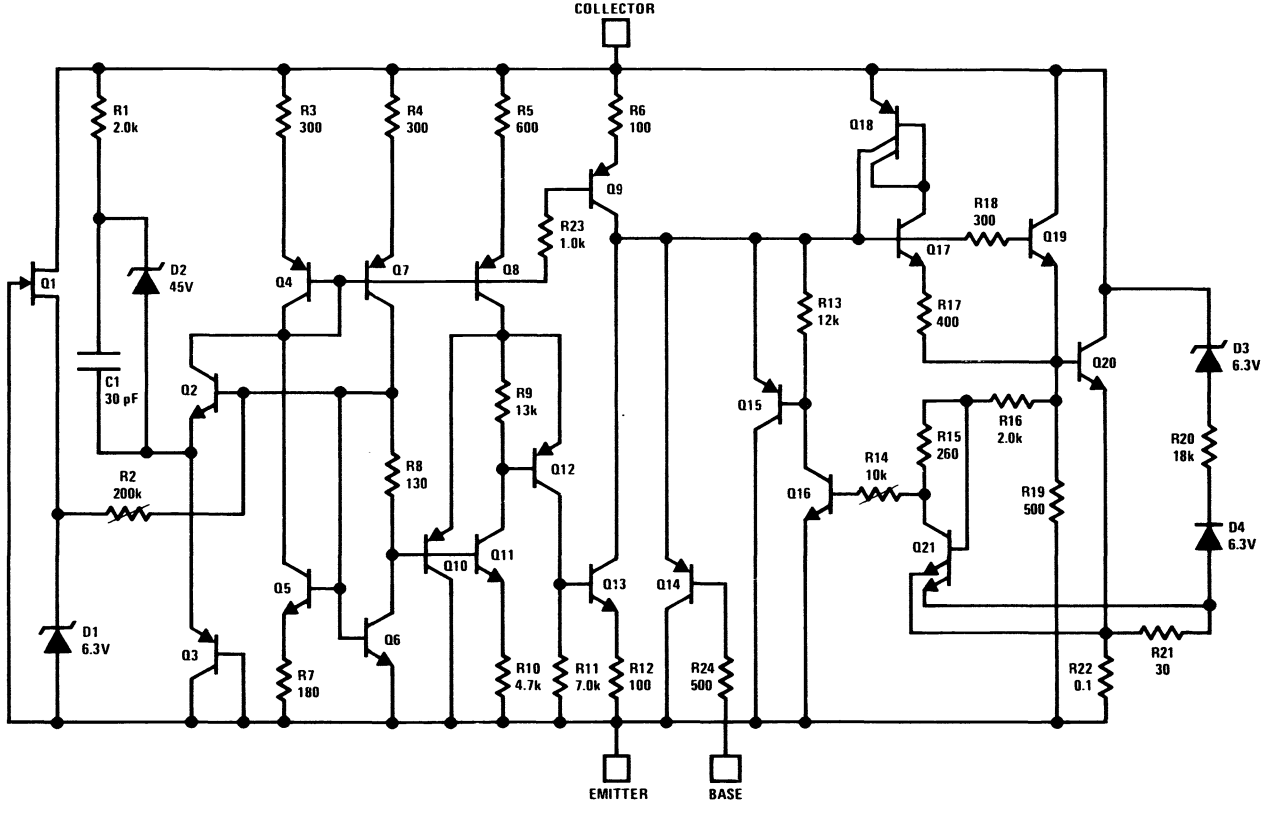
TL/H/6009–9

Small Signal Frequency Response



TL/H/6009–10

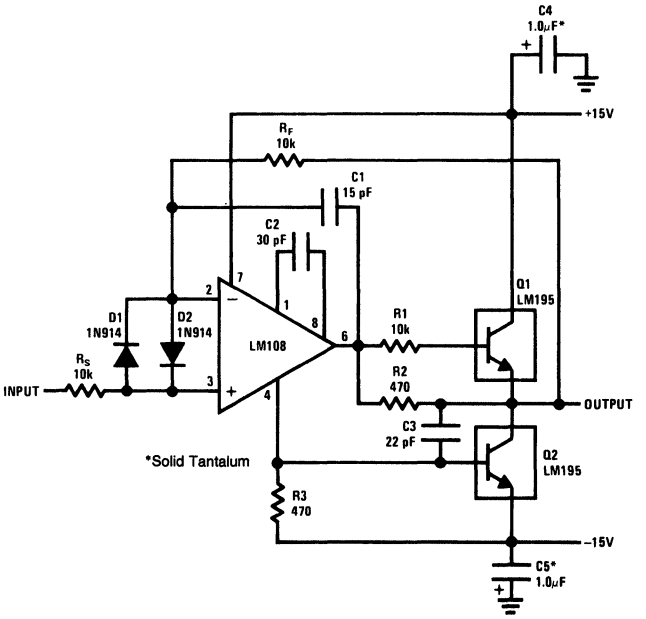
Schematic Diagram



TL/H/6009–11

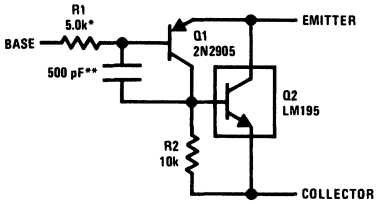
Typical Applications

1.0 Amp Voltage Follower



TL/H/6009-12

Power PNP

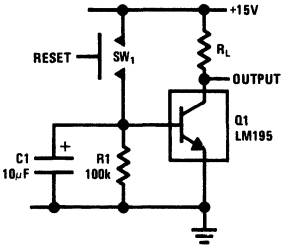


TL/H/6009-13

*Protects against excessive base drive

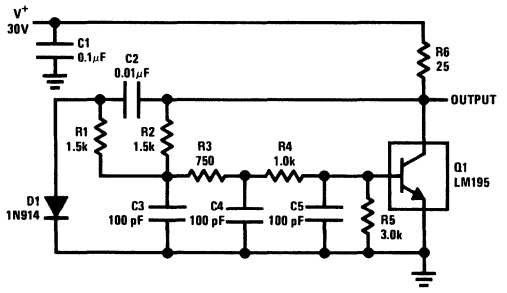
**Needed for stability

Time Delay



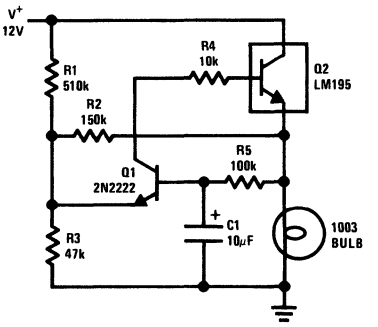
TL/H/6009-14

1.0 MHz Oscillator



TL/H/6009-15

1.0 Amp Lamp Flasher

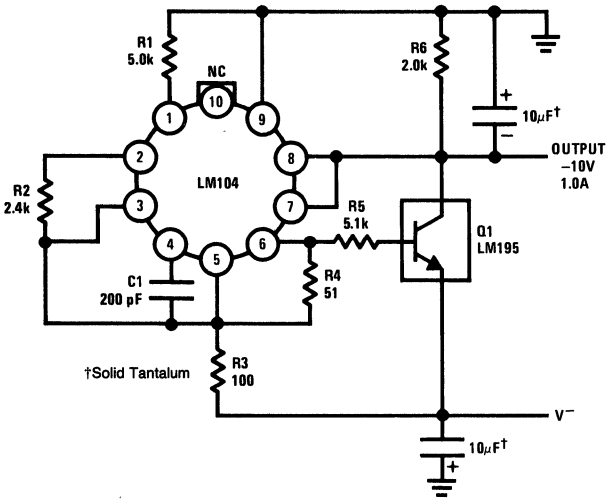


TL/H/6009-16

8

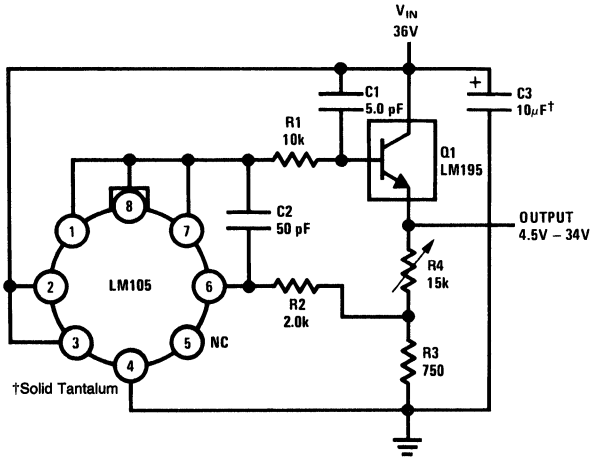
Typical Applications (Continued)

1.0 Amp Negative Regulator



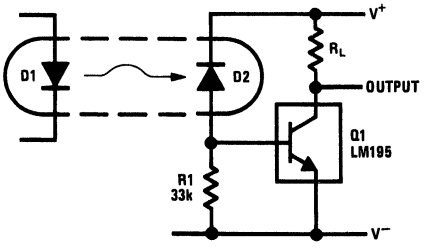
TL/H/6009–17

1.0 Amp Positive Voltage Regulator



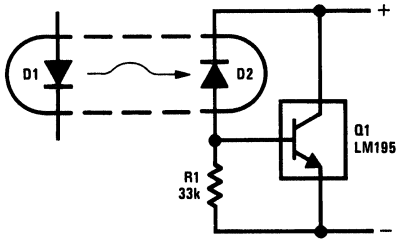
TL/H/6009–18

Fast Optically Isolated Switch



TL/H/6009–19

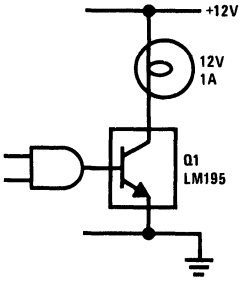
Optically Isolated Power Transistor



TL/H/6009–20

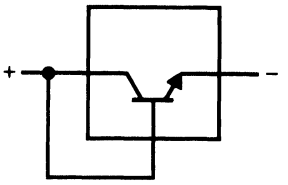
Typical Applications (Continued)

CMOS or TTL Lamp Interface



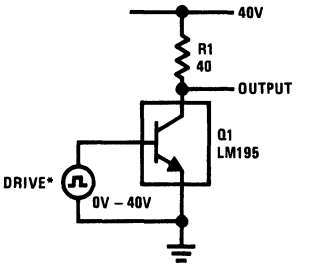
TL/H/6009-21

Two Terminal Current Limiter



TL/H/6009-22

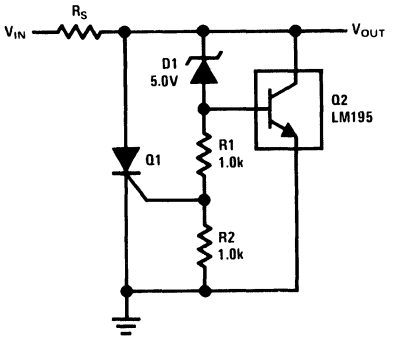
40V Switch



TL/H/6009-23

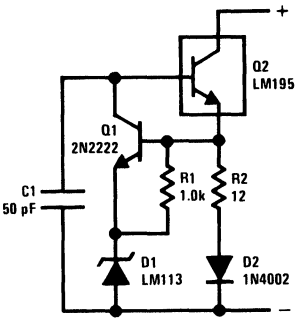
*Drive Voltage 0V to ≥ 10V ≤ 42V

6.0V Shunt Regulator with Crowbar



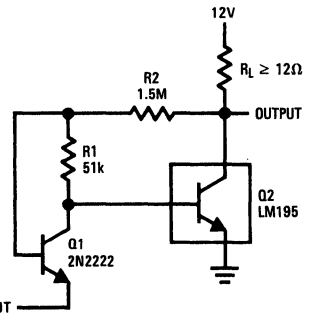
TL/H/6009-24

Two Terminal 100 mA Current Regulator



TL/H/6009-25

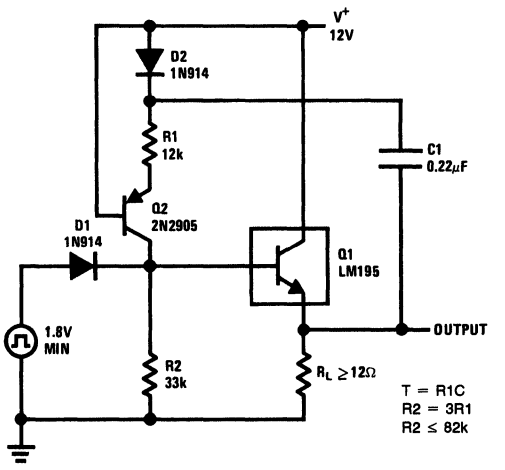
Low Level Power Switch



Turn ON = 350 mV
Turn OFF = 200 mV

TL/H/6009-26

Power One-Shot

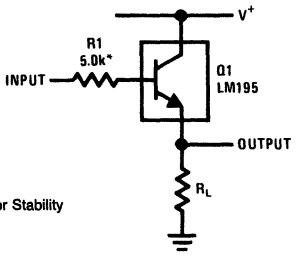


T = R1C
R2 = 3R1
R2 ≤ 82k

TL/H/6009-27

Typical Applications (Continued)

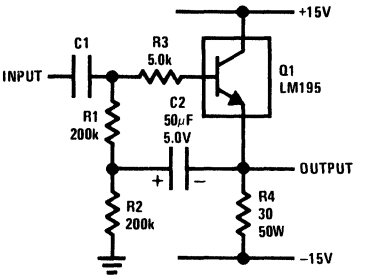
Emitter Follower



*Need for Stability

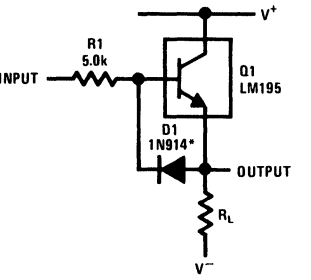
TL/H/6009–28

High Input Impedance AC Emitter Follower



TL/H/6009–29

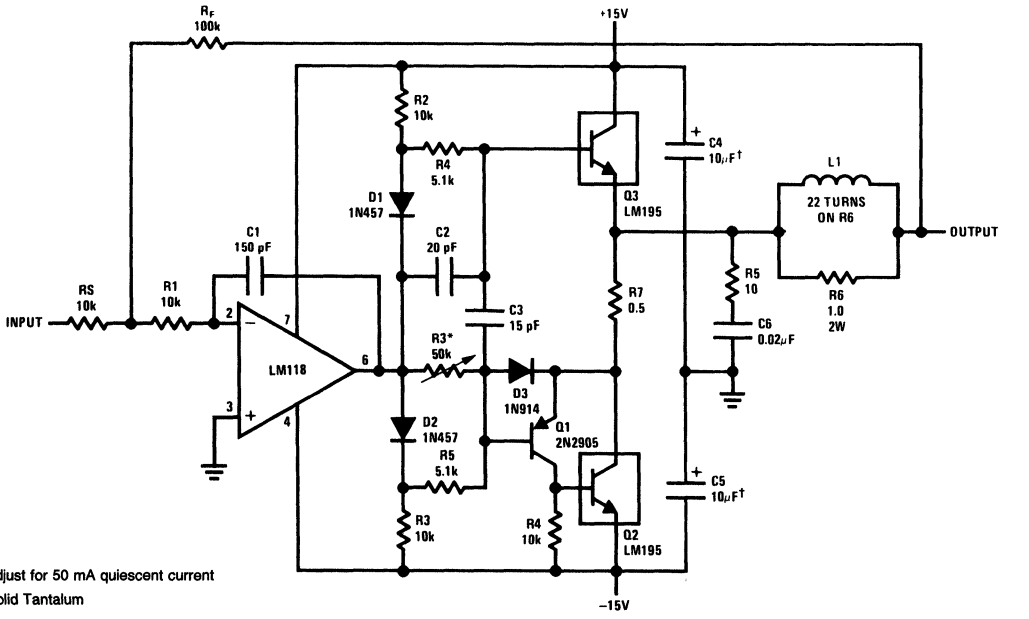
Fast Follower



TL/H/6009–30

*Prevents storage with fast fall time square wave drive

Power Op Amp

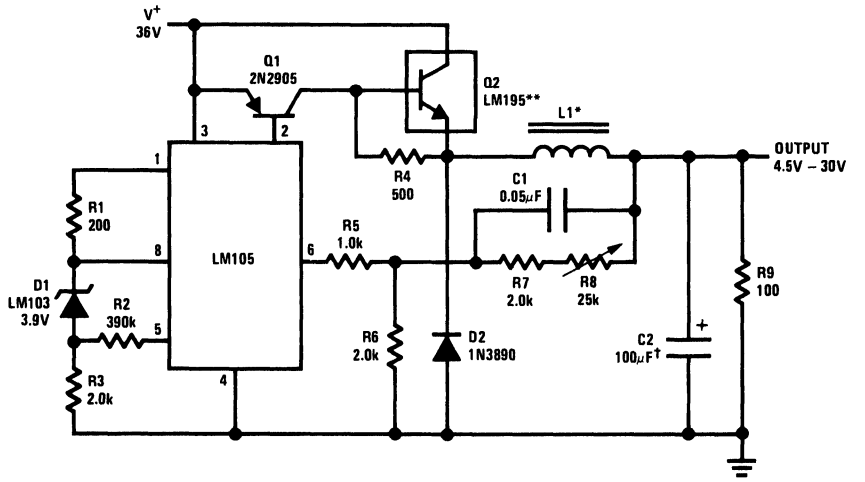


*Adjust for 50 mA quiescent current
†Solid Tantalum

TL/H/6009–31

Typical Applications (Continued)

6.0 Amp Variable Output Switching Regulator



TL/H/6009–32

*Sixty turns wound on Arnold Type A-083081-2 core.

**Four devices in parallel

†Solid tantalum

National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

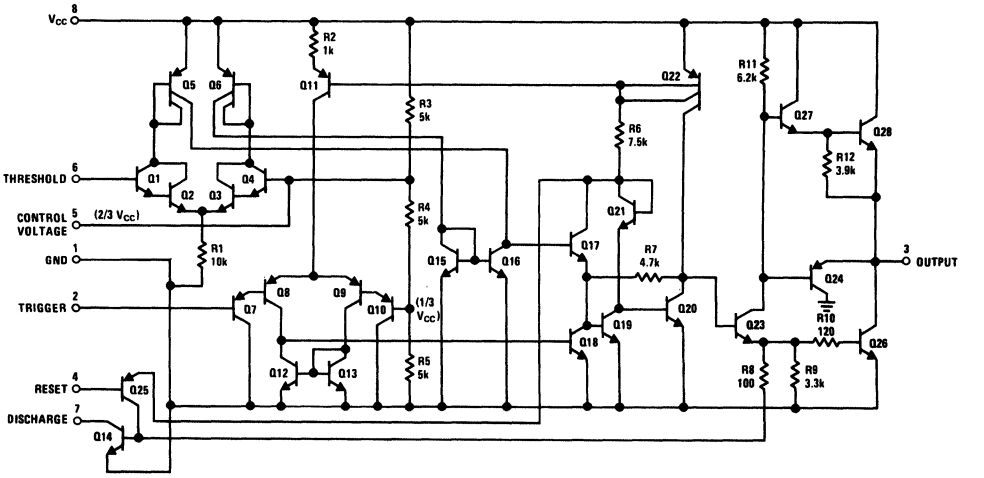
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM555H, LM555CH 760 mW
- LM555, LM555CN 1180 mW

Operating Temperature Ranges
- LM555C 0°C to +70°C
- LM555 −55°C to + 125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 Seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 Seconds) 215°C
  - Infrared (15 Seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		3 10	5 12		3 10	6 15	mA mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V	4.8 1.45	5 1.67	5.2 1.9		5 1.67		V V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, (unless othewise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15V$							
	$I_{SINK} = 10$ mA		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100$ mA		2	2.2		2	2.5	V
	$I_{SINK} = 200$ mA		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8$ mA		0.1	0.25				V
	$I_{SINK} = 5$ mA					0.25	0.35	V
Output Voltage Drop (High)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15V$		12.5			12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15V$	13	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°c/w (T0-5), 106°c/w (DIP) and 170°c/w (S0-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at $V_{CC} = 5V$.

Note 3: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.

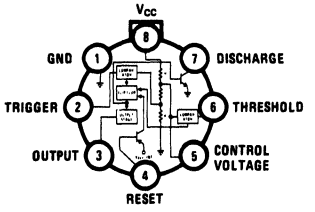
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package

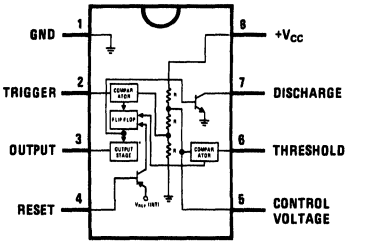


TL/H/7851-2

Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



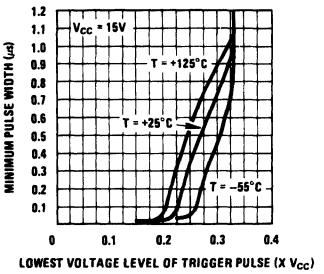
TL/H/7851-3

Top View

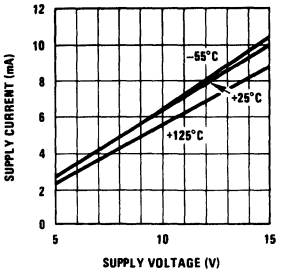
Order Number LM555J, LM555CJ,
LM555CM or LM555CN
See NS Package Number J08A, M08A or N08E

Typical Performance Characteristics

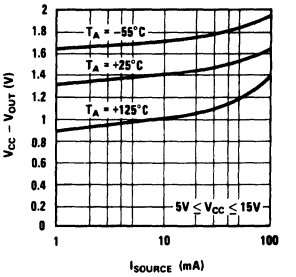
Minimuim Pulse Width Required for Triggering



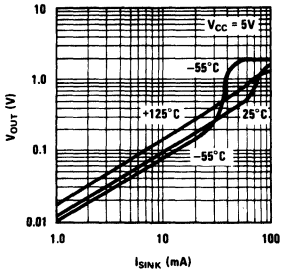
Supply Current vs Supply Voltage



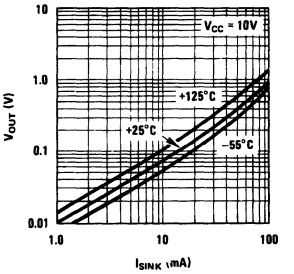
High Output Voltage vs Output Source Current



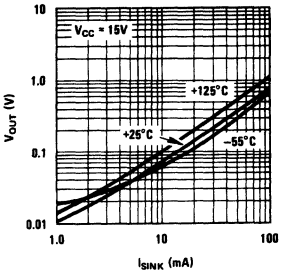
Low Output Voltage vs Output Sink Current



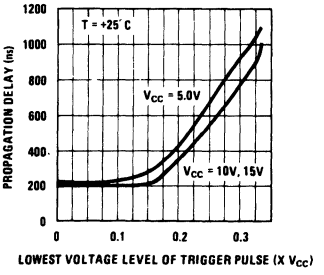
Low Output Voltage vs Output Sink Current



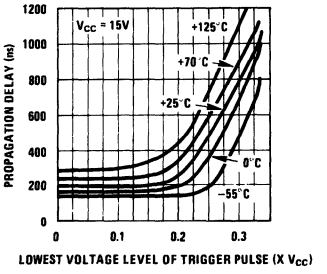
Low Output Voltage vs Output Sink Current



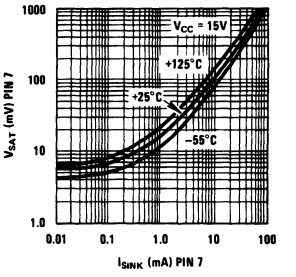
Output Propagation Delay vs Voltage Level of Trigger Pulse



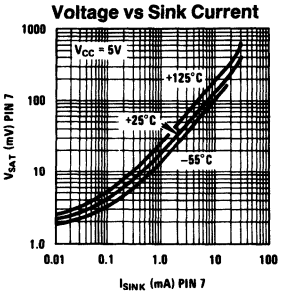
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



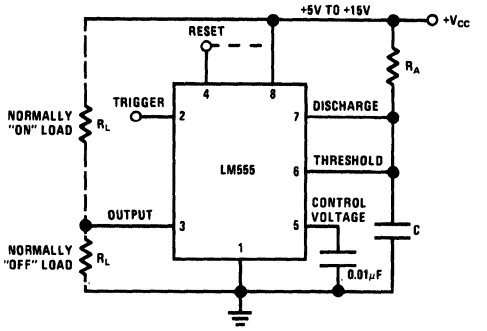
TL/H/7851–4

8

Applications Information

MONOSTABLE OPERATION

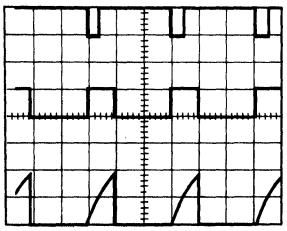
In this mode of operation, the timer functions as a one-shot *(Figure 1)*. The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



TL/H/7851–5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



TL/H/7851–6

V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

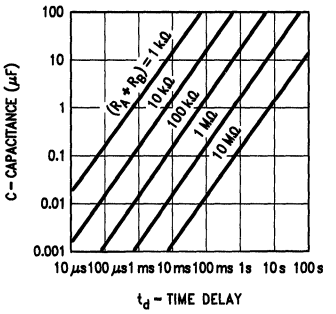
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

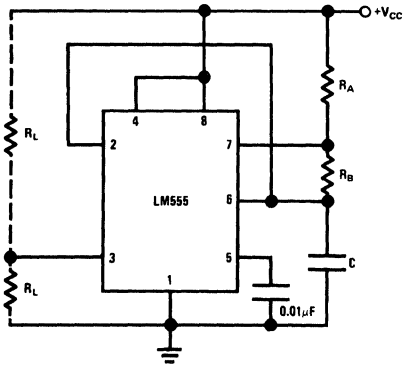


TL/H/7851–7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



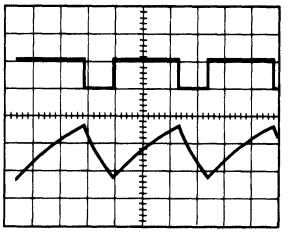
TL/H/7851–8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



TL/H/7851–9

V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

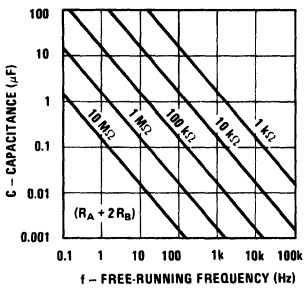
$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \frac{R_B}{R_A + 2R_B}$

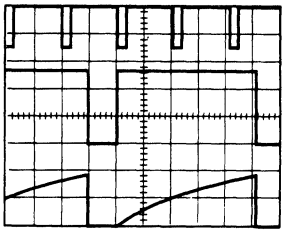


TL/H/7851–10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



TL/H/7851–11

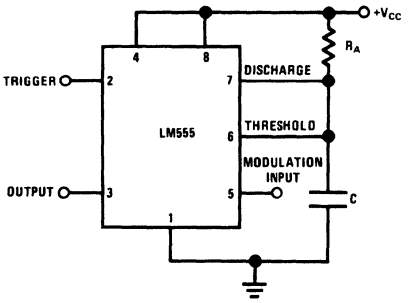
V_{CC} = 5V
TIME = 20 μs/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

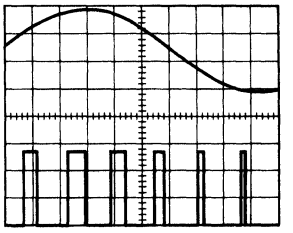
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



TL/H/7851–12

FIGURE 8. Pulse Width Modulator



TL/H/7851–13

V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

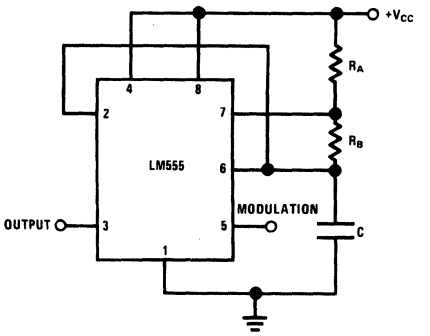
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

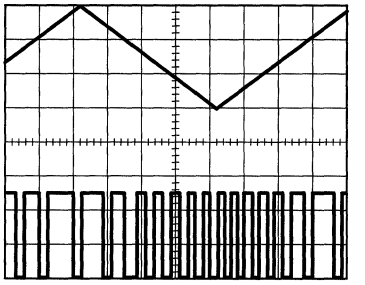
This application uses the timer connected for astable operation, as in *Figure 10,* with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)



TL/H/7851–14

FIGURE 10. Pulse Position Modulator



TL/H/7851–15

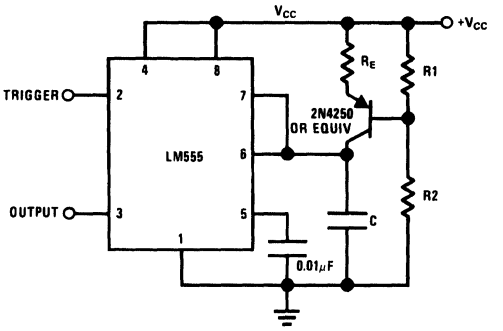
V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



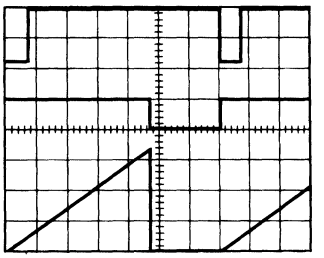
TL/H/7851–16

FIGURE 12

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$



TL/H/7851–17

V_{CC} = 5V
TIME = 20 μs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

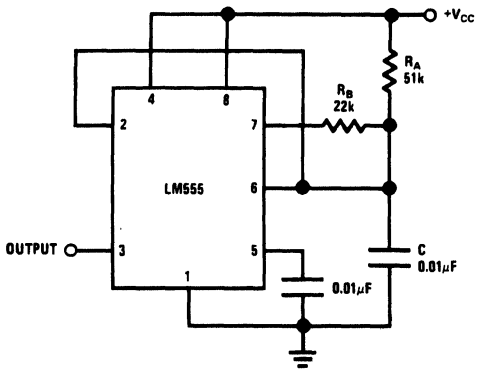
For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14.* The time period for the out-

Applications Information (Continued)

put high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \dfrac{1}{t_1 + t_2}$



TL/H/7851–18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 μF in parallel with 1 μF electrolytic.

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

National Semiconductor

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

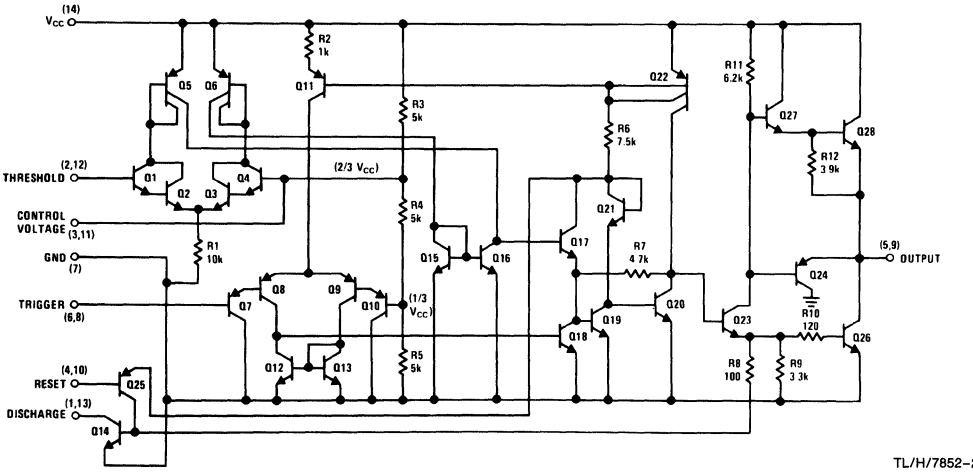
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

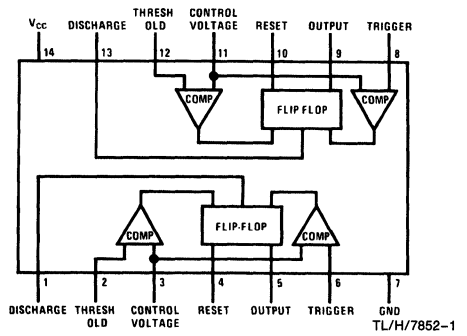
Schematic Diagram



TL/H/7852–2

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7852–1

Top View

Order Number LM556J or LM556CJ
See NS Package Number J14A

Order Number LM556CM
See NS Package Number M14A

Order Number LM556CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM556J, LM556CJ 1785 mW
- LM556CN 1620 mW

Operating Temperature Ranges
- LM556C 0°C to +70°C
- LM556 −55°C to +125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	LM556			LM556C			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current (Each Timer Section)	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		3 10	5 11		3 10	6 14	mA mA
Timing Error, Monostable Initial Accuracy Drift with Temperature Accuracy over Temperature Drift with Supply	 R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		 0.5 30 1.5 0.05			 0.75 50 1.5 0.1		 % ppm/°C % %/V
Timing Error, Astable Initial Accuracy Drift with Temperature Accuracy over Temperature Drift with Supply	 R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		 1.5 90 2.5 0.15			 2.25 150 3.0 0.30		 % ppm/°C % %/V
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V	4.8 1.45	5 1.67	5.2 1.9	4.5 1.25	5 1.67	5.5 2.0	V V
Trigger Current			0.1	0.5		0.2	1.0	μA
Reset Voltage	(Note 4)	0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.6	mA
Threshold Current	V_{TH} = V-Control (Note 5) V_{TH} = 11.2V		0.03	0.1 250		0.03	0.1 250	μA nA
Control Voltage Level and Threshold Voltage	V_{CC} = 15V V_{CC} = 5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V V
Pin 1, 13 Leakage Output High			1	100		1	100	nA
Pin 1, 13 Sat Output Low Output Low	(Note 6) V_{CC} = 15V, I = 15 mA V_{CC} = 4.5V, I = 4.5 mA		 150 70	 240 100		 180 80	 300 200	 mV mV

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified) (Continued)

Parameter	Conditions	LM556			LM556C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.25		2	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics	(Note 7)							
Initial Timing Accuracy			0.05	0.2		0.1	2.0	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/V

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 70°C/W (Ceramic), 77°C/W (Plastic DIP) and 110°C/W (SO-14 Narrow).

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: As reset voltage lowers, timing is inhibited and then the output goes low.

Note 5: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

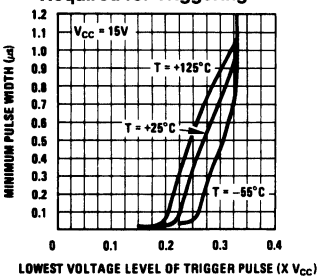
Note 6: No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.

Note 7: Matching characteristics refer to the difference between performance characteristics of each timer section.

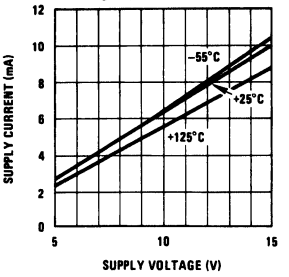
Note 8: Refer to RETS556X drawing for specifications of military LM556J version.

Typical Performance Characteristics

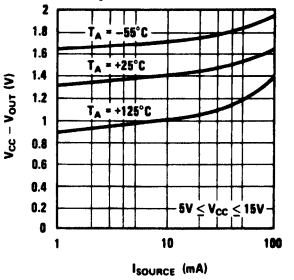
Minimum Pulse Width Required for Triggering



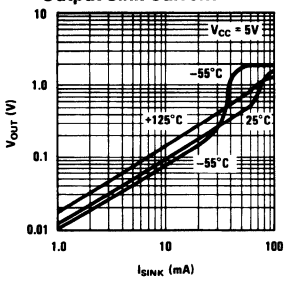
Supply Current vs Supply Voltage (Each Section)



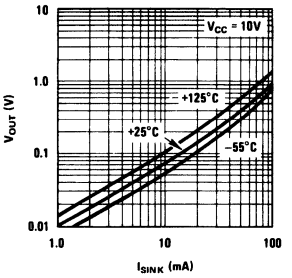
High Output Voltage vs Output Source Current



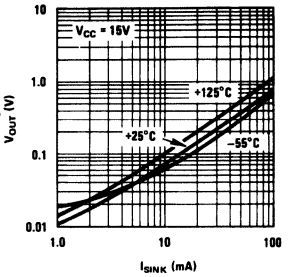
Low Output Voltage vs Output Sink Current



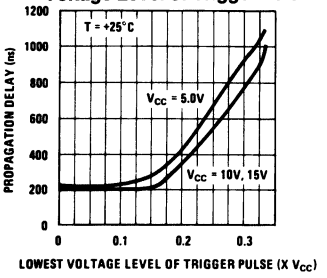
Low Output Voltage vs Output Sink Current



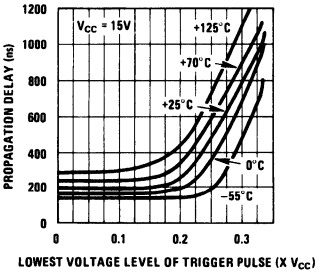
Low Output Voltage vs Output Sink Current



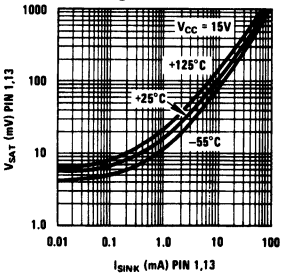
Output Propagation Delay vs Voltage Level of Trigger Pulse



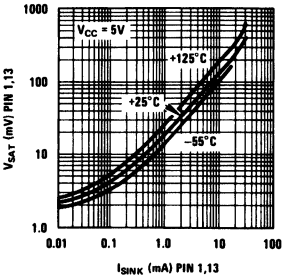
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 1, 13) Voltage vs Sink Current



Discharge Transistor (Pin 1, 13) Voltage vs Sink Current



TL/H/7852–3

8

National Semiconductor

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

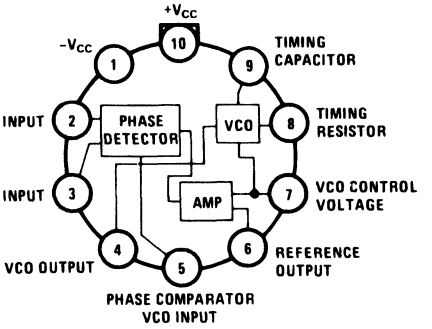
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

Connection Diagrams

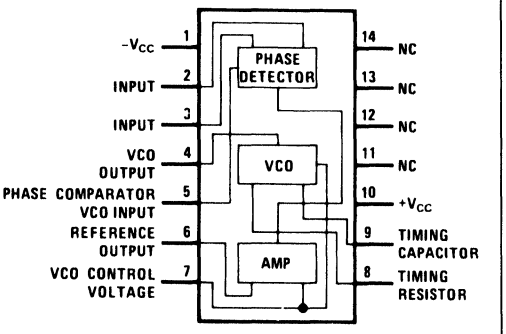
Metal Can Package



TL/H/7853–2

Order Number LM565H
See NS Package Number H10C

Dual-In-Line Package



TL/H/7853–3

Order Number LM565CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 1)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

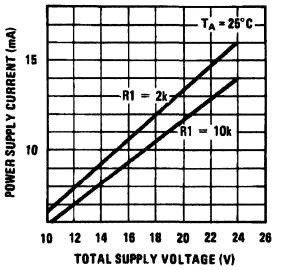
Electrical Characteristics AC Test Circuit, T_A = 25°C, V_{CC} = ±6V

Parameter	Conditions	LM565			LM565C			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	C_o = 2.7 pF	300	500		250	500		kHz
VCO Free-Running Frequency	C_o = 1.5 nF R_o = 20 kΩ f_o = 10 kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	f_o = 10 kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			.68			.68		V/radian

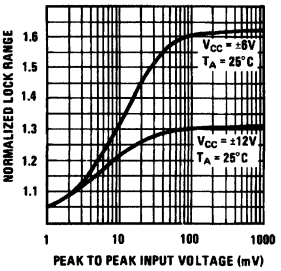
Note 1: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

Typical Performance Characteristics

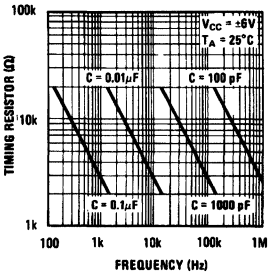
Power Supply Current as a Function of Supply Voltage



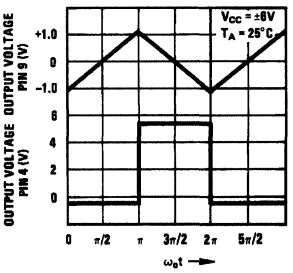
Lock Range as a Function of Input Voltage



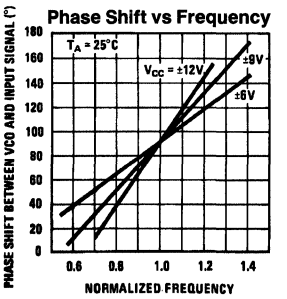
VCO Frequency



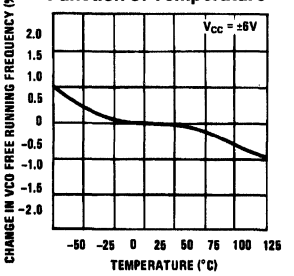
Oscillator Output Waveforms



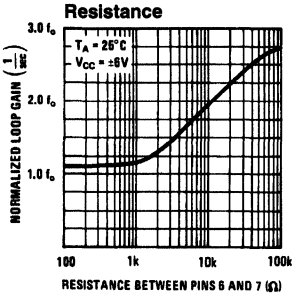
Phase Shift vs Frequency



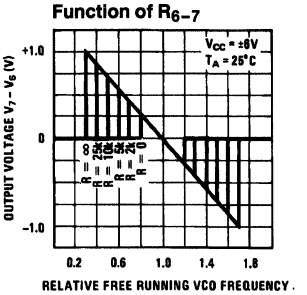
VCO Frequency as a Function of Temperature



Loop Gain vs Load Resistance

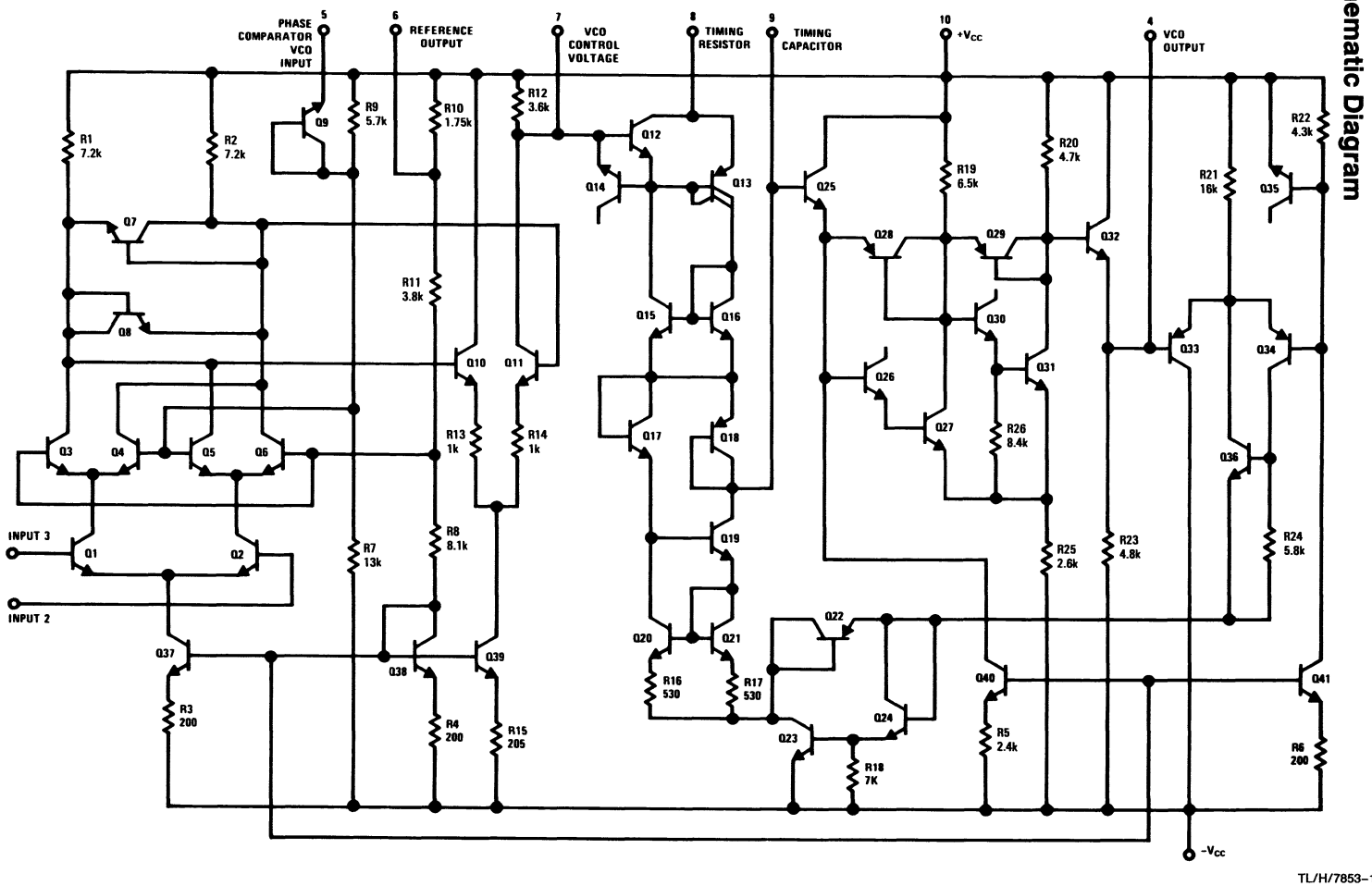


Hold in Range as a Function of R_{6-7}



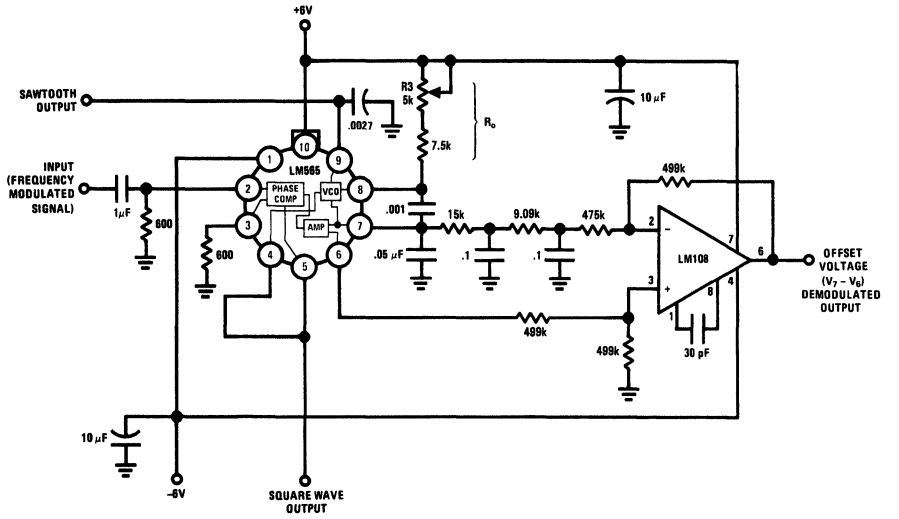
TL/H/7853–4

Schematic Diagram



TL/H/7853–1

AC Test Circuit

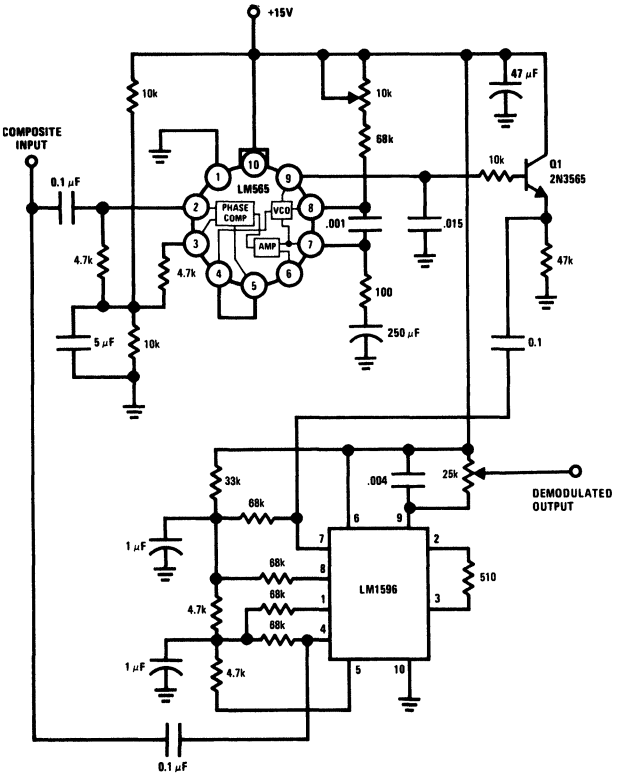


TL/H/7853–5

Note: S_1 open for output offset voltage ($V_7 - V_6$) measurement.

Typical Applications

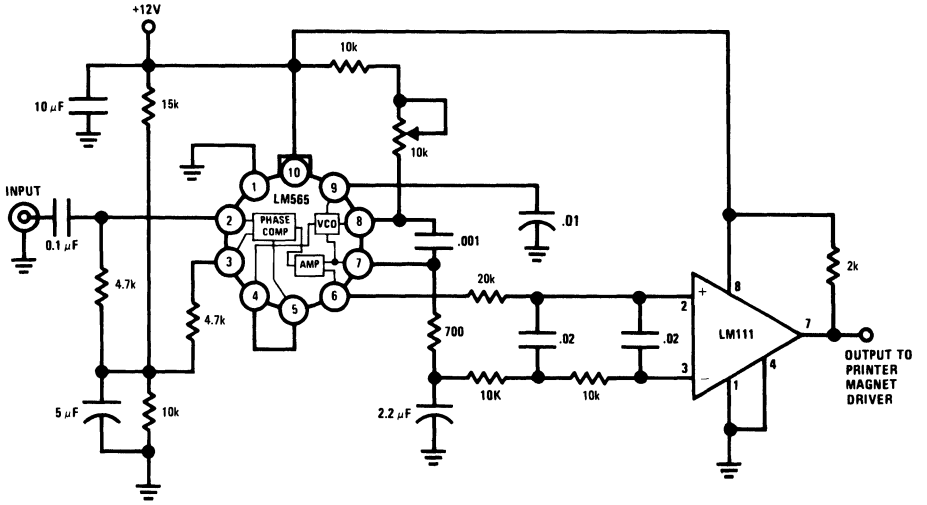
2400 Hz Synchronous AM Demodulator



TL/H/7853–6

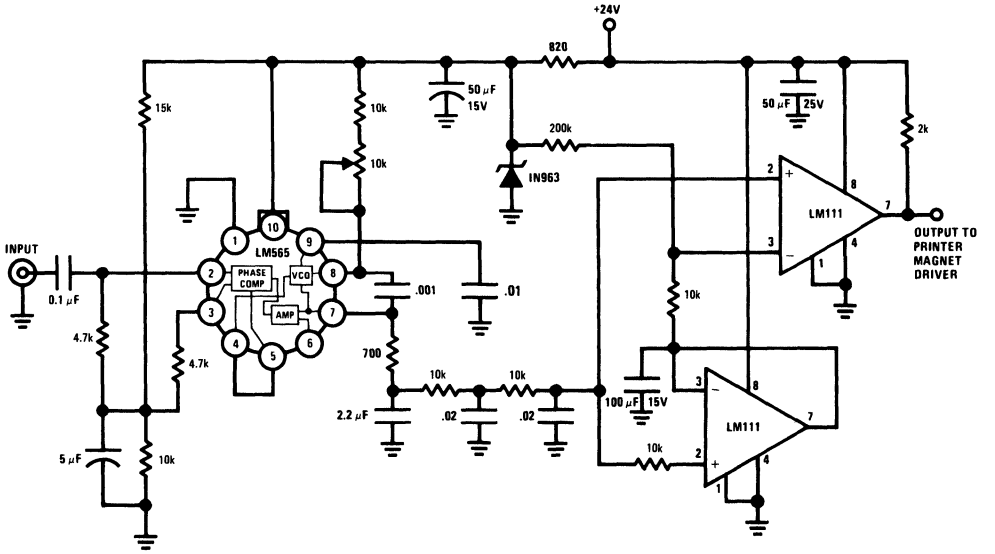
Typical Applications (Continued)

FSK Demodulator (2025–2225 cps)



TL/H/7853–7

FSK Demodulator with DC Restoration

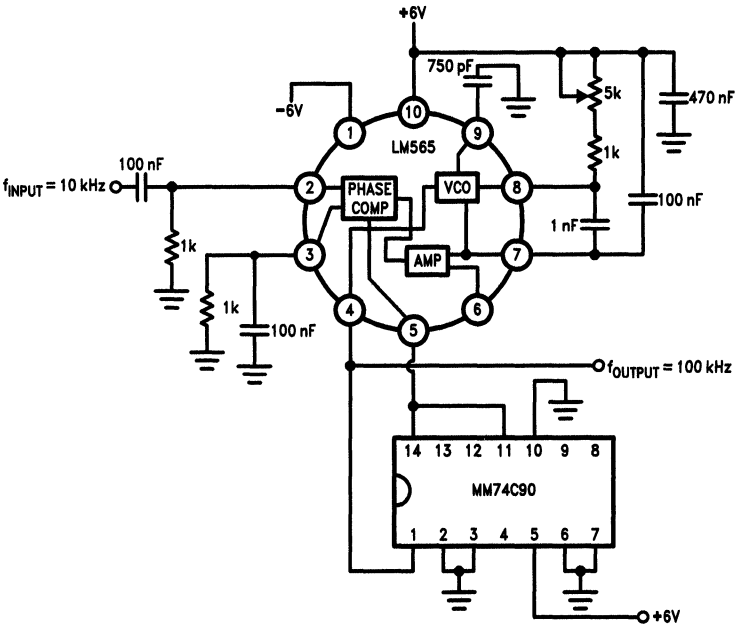


TL/H/7853–8

8

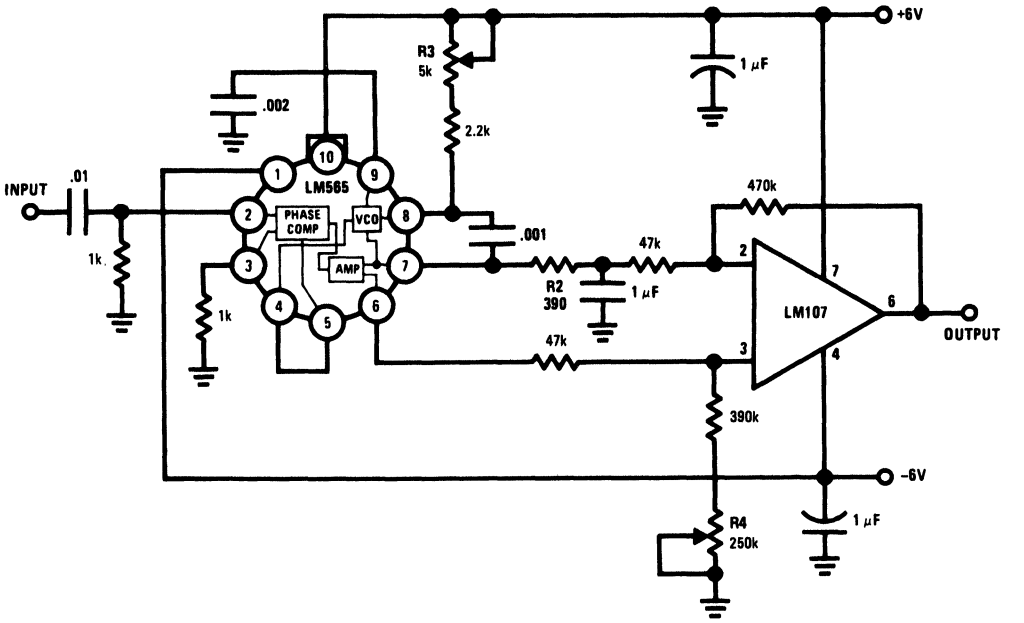
Typical Applications (Continued)

Frequency Multiplier (×10)



TL/H/7853–9

IRIG Channel 13 Demodulator



TL/H/7853–10

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{0.3}{R_o C_o}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient."

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

K_o = oscillator sensitivity $\left(\frac{\text{radians/sec}}{\text{volt}}\right)$

K_D = phase detector sensitivity $\left(\frac{\text{volts}}{\text{radian}}\right)$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm\frac{8\, f_o}{V_c}$$

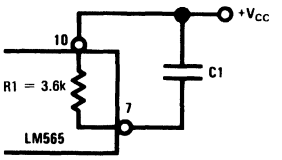
f_o = free running frequency of VCO

V_c = total supply voltage to the circuit

THE LOOP FILTER

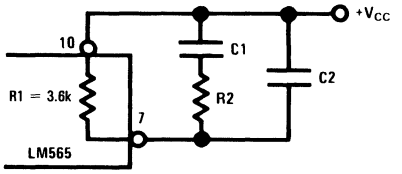
In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

Simple Lag Filter



TL/H/7853–11

Lag-Lead Filter



TL/H/7853–12

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

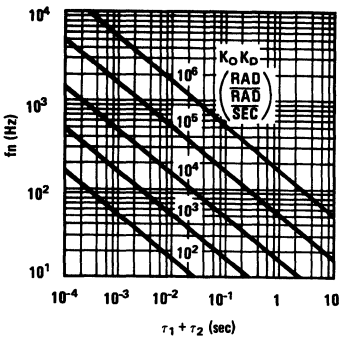
$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \approx \pi\, \tau_2 f_n$$

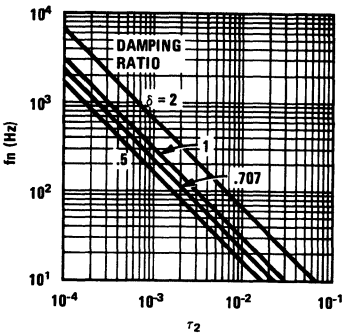
These two equations are plotted for convenience.

Filter Time Constant vs Natural Frequency



TL/H/7853–13

Damping Time Constant vs Natural Frequency



TL/H/7853–14

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\, C_1$.

National Semiconductor

LM566C Voltage Controlled Oscillator

General Description

The LM566CN is a general purpose voltage controlled oscillator which may be used to generate square and triangular waves, the frequency of which is a very linear function of a control voltage. The frequency is also a function of an external resistor and capacitor.

The LM566CN is specified for operation over the 0°C to +70°C temperature range.

Features

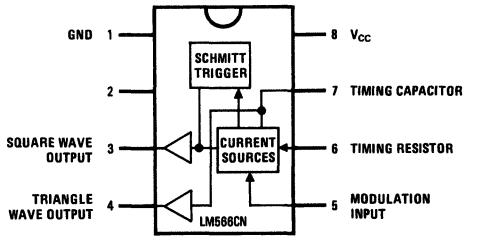
- Wide supply voltage range: 10V to 24V
- Very linear modulation characteristics
- High temperature stability
- Excellent supply voltage rejection
- 10 to 1 frequency range with fixed capacitor
- Frequency programmable by means of current, voltage, resistor or capacitor

Applications

- FM modulation
- Signal generation
- Function generation
- Frequency shift keying
- Tone generation

Connection Diagram

Dual-In-Line Package

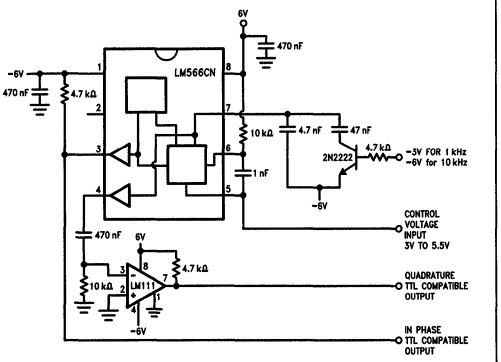


TL/H/7854–2

Order Number LM566CN
See NS Package Number N08E

Typical Application

1 kHz and 10 kHz TTL Compatible Voltage Controlled Oscillator



TL/H/7854–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	26V
Power Dissipation (Note 1)	1000 mW
Operating Temperature Range, LM566CN	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics V_{CC} = 12V, T_A = 25°C, AC Test Circuit

Parameter	Conditions	LM566C			Units
		Min	Typ	Max	
Maximum Operating Frequency	R0 = 2k C0 = 2.7 pF	0.5	1		MHz
VCO Free-Running Frequency	C_O = 1.5 nF R_O = 20k f_O = 10 kHz	−30	0	+30	%
Input Voltage Range Pin 5		¾ V_{CC}		V_{CC}	
Average Temperature Coefficient of Operating Frequency			200		ppm/°C
Supply Voltage Rejection	10–20V		0.1	2	%/V
Input Impedance Pin 5		0.5	1		MΩ
VCO Sensitivity	For Pin 5, From 8–10V, f_O = 10 kHz	6.0	6.6	7.2	kHz/V
FM Distortion	±10% Deviation		0.2	1.5	%
Maximum Sweep Rate			1		MHz
Sweep Range			10:1		
Output Impedance Pin 3			50		Ω
Pin 4			50		Ω
Square Wave Output Level	R_{L1} = 10k	5.0	5.4		Vp-p
Triangle Wave Output Level	R_{L2} = 10k	2.0	2.4		Vp-p
Square Wave Duty Cycle		40	50	60	%
Square Wave Rise Time			20		ns
Square Wave Fall Time			50		ns
Triangle Wave Linearity	+1V Segment at ½ V_{CC}		0.5		%

Note 1: The maximum junction temperature of the LM566CN is 150°C. For operation at elevated junction temperatures, maximum power dissipation must be derated based on a thermal resistance of 115°C/W, junction to ambient.

Applications Information

The LM566CN may be operated from either a single supply as shown in this test circuit, or from a split (±) power supply. When operating from a split supply, the square wave output (pin 3) is TTL compatible (2 mA current sink) with the addition of a 4.7 kΩ resistor from pin 3 to ground.

A 0.001 μF capacitor is connected between pins 5 and 6 to prevent parasitic oscillations that may occur during VCO switching.

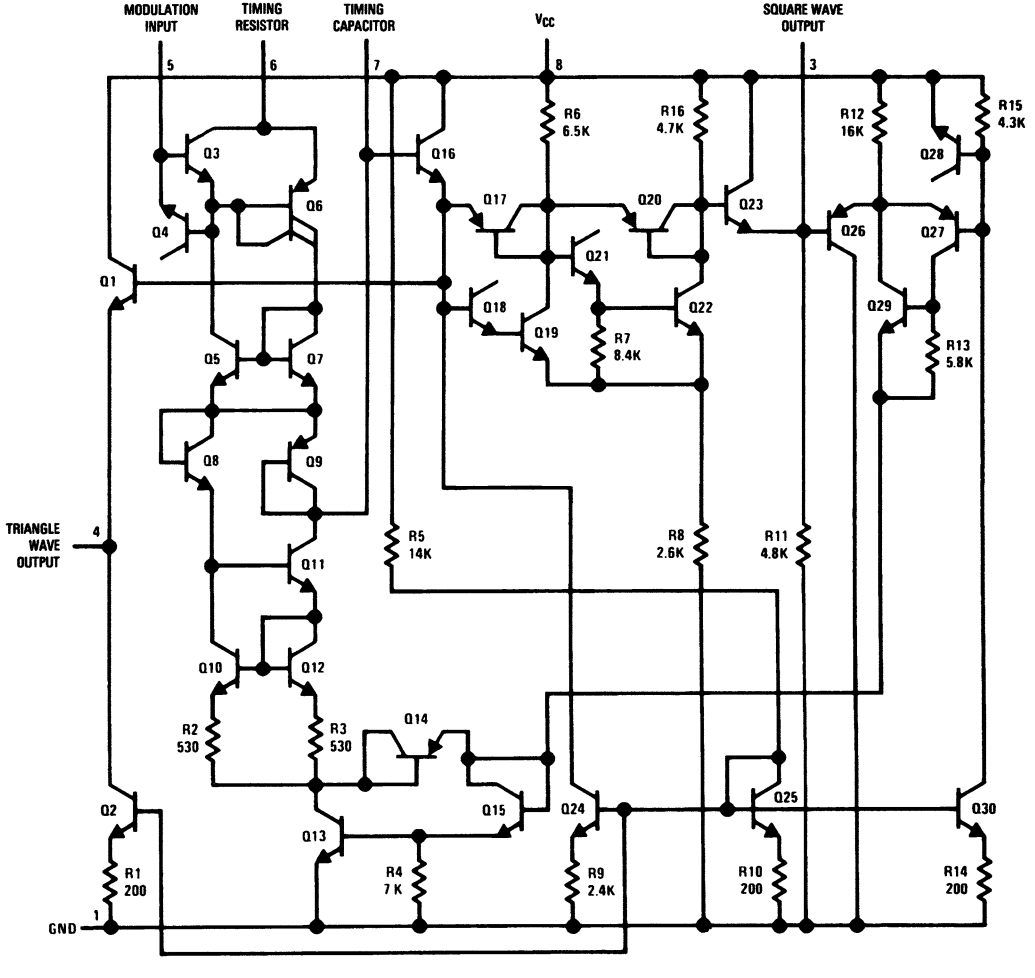
$$f_O = \frac{2.4(V^+ - V_5)}{R_O C_O V^+}$$

where

$2K < R_O < 20K$

and V_5 is voltage between pin 5 and pin 1.

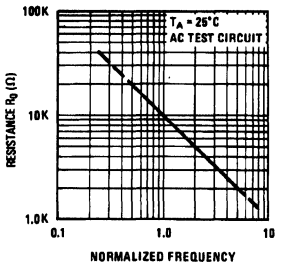
Schematic Diagram



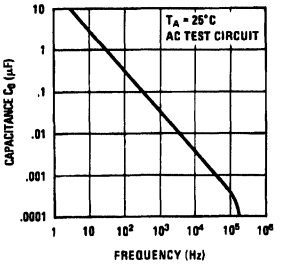
TL/H/7854–1

Typical Performance Characteristics

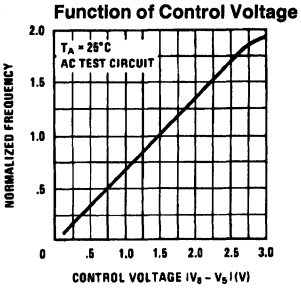
Operating Frequency as a Function of Timing Resistor



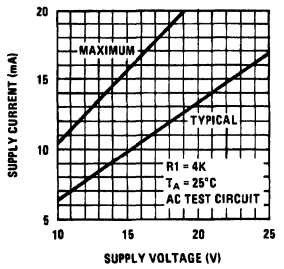
Operating Frequency as a Function of Timing Capacitor



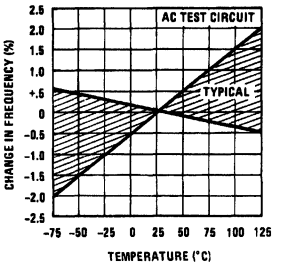
Normalized Frequency as a Function of Control Voltage



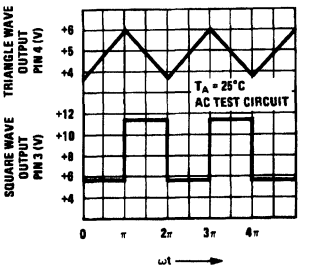
Power Supply Current



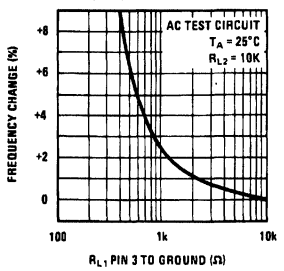
Temperature Stability



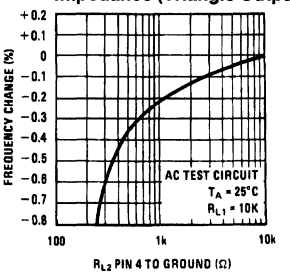
VCO Waveforms



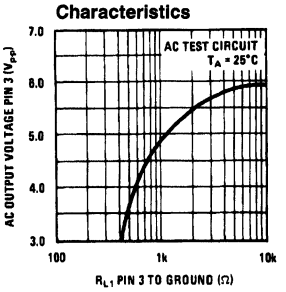
Frequency Stability vs Load Resistance (Square Wave Output)



Frequency Stability vs Load Impedance (Triangle Output)

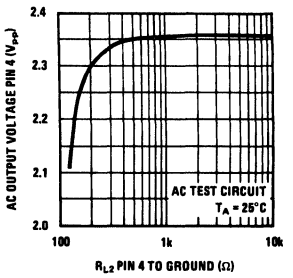


Square Wave Output Characteristics



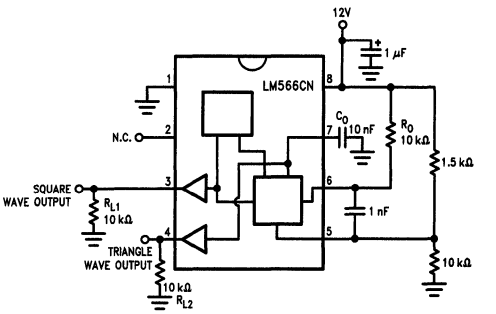
TL/H/7854–4

Triangle Wave Output Characteristics



TL/H/7854–5

AC Test Circuit



TL/H/7854–6

National Semiconductor

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

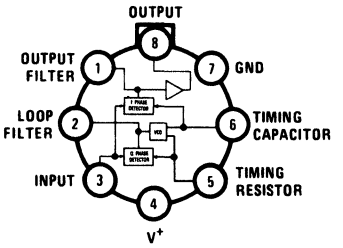
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

Metal Can Package

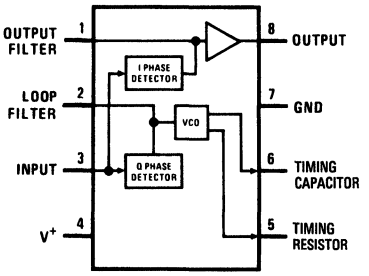


TL/H/6975–1

Top View

Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/6975–2

Top View

Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 1)	1100 mW
V_8	15V
V_3	−10V
V_3	V_4 + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM567H	−55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

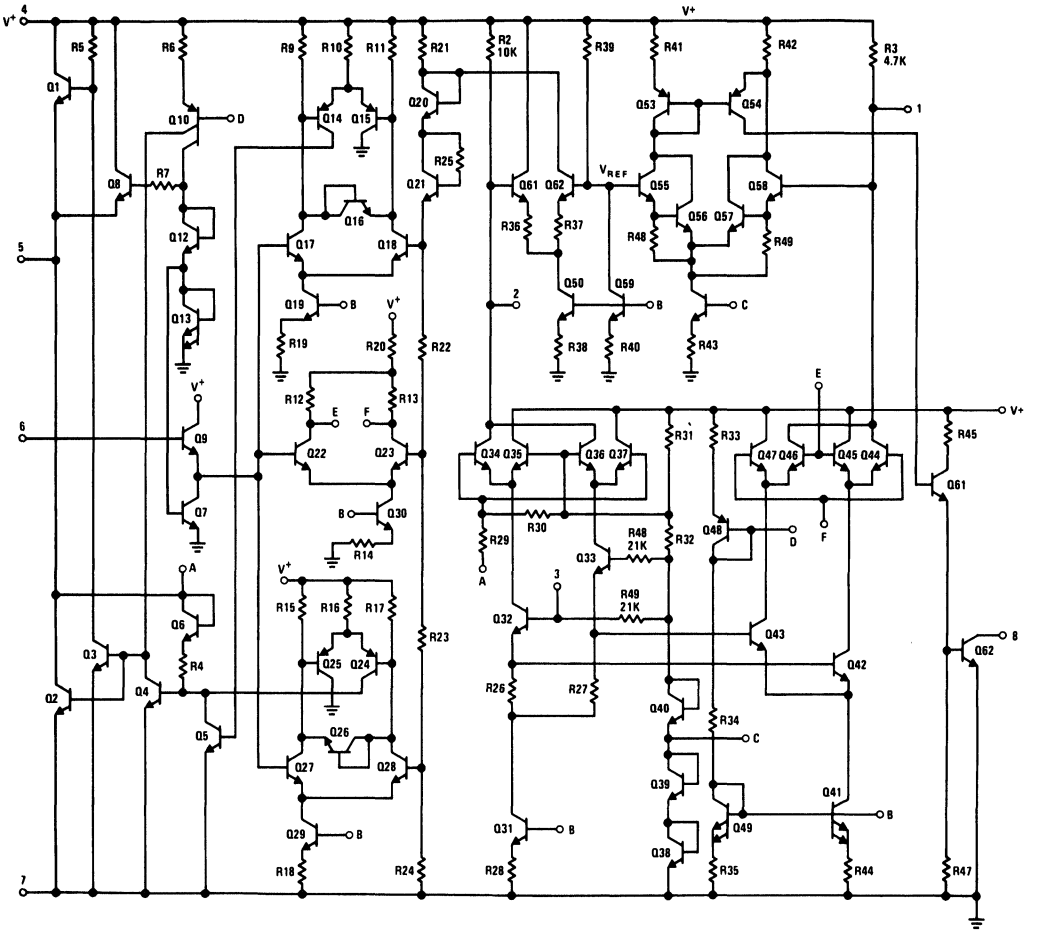
Electrical Characteristics AC Test Circuit, T_A = 25°C, V^+ = 5V

Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 − 6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75–5.75V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ±60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V − 6.75V 4.75V − 9V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 2: Refer to RETS567X drawing for specifications of military LM567H version.

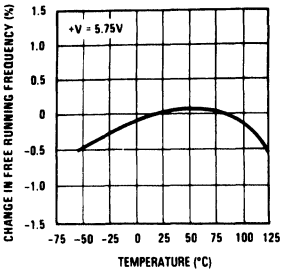
Schematic Diagram



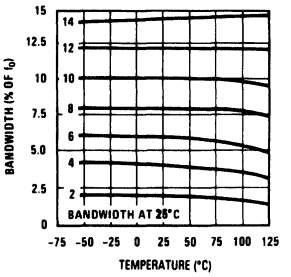
TL/H/6975-3

Typical Performance Characteristics

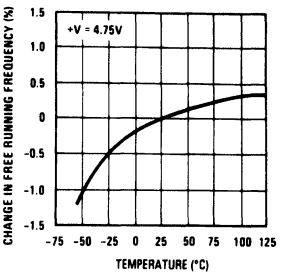
Typical Frequency Drift



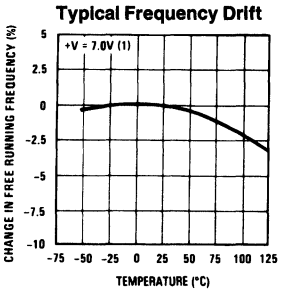
Typical Bandwidth Variation



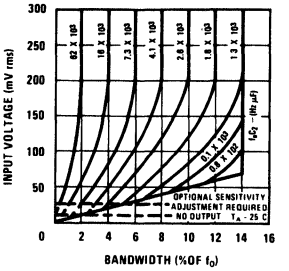
Typical Frequency Drift



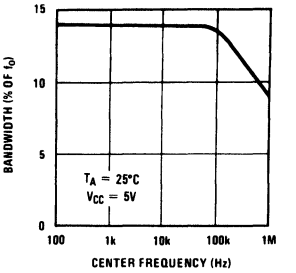
Typical Frequency Drift



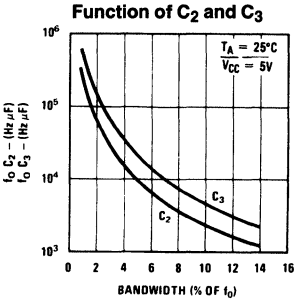
Bandwidth vs Input Signal Amplitude



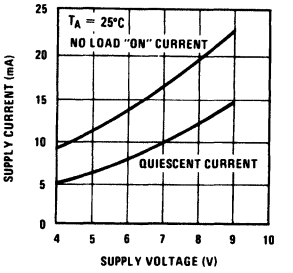
Largest Detection Bandwidth



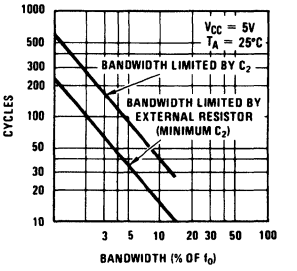
Detection Bandwidth as a Function of C_2 and C_3



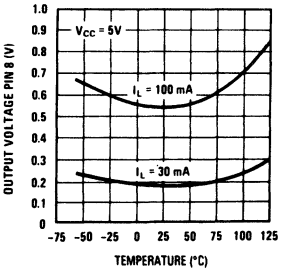
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output



Typical Output Voltage vs Temperature



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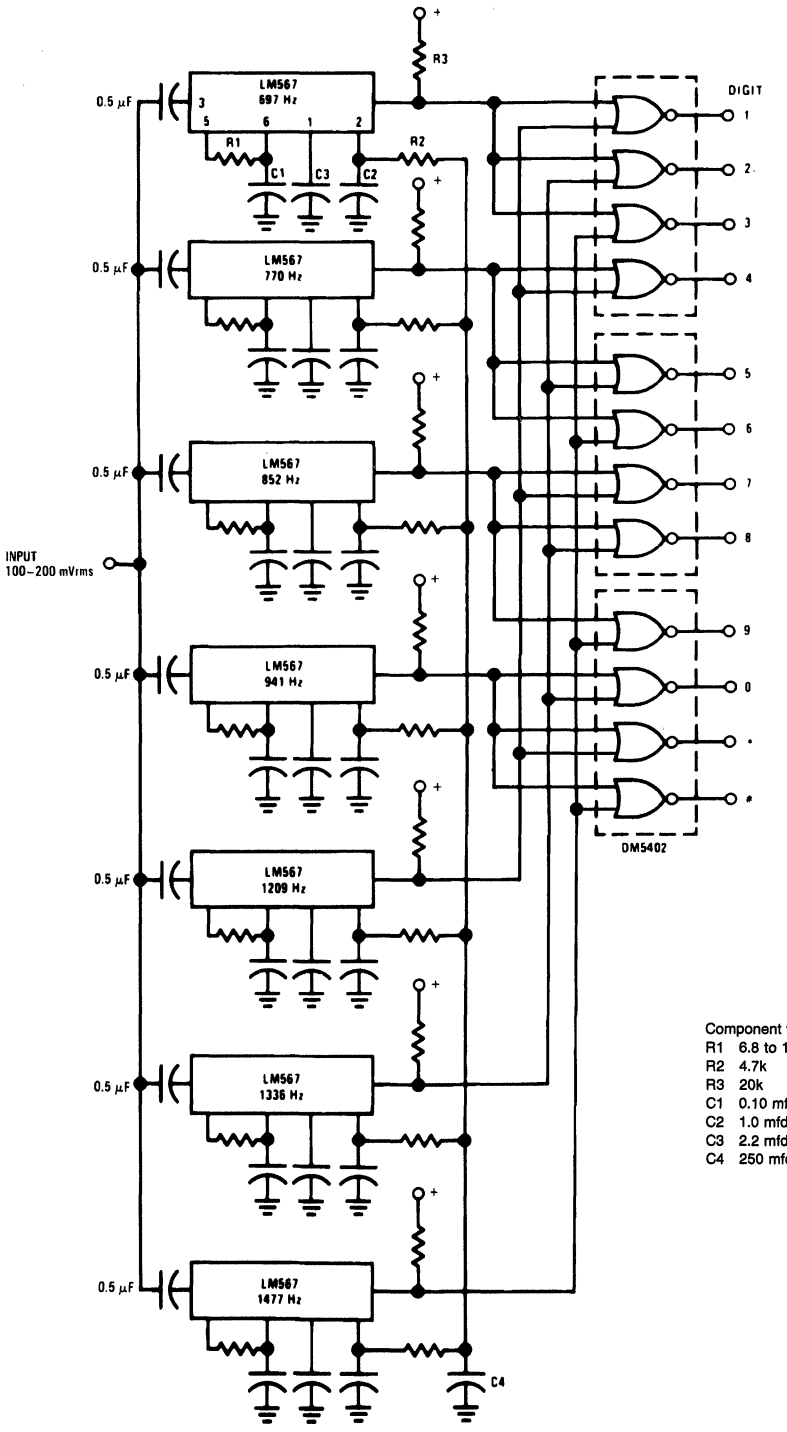
8

Typical Applications

Touch-Tone Decoder



Component values (typ)

R1	6.8 to 15k
R2	4.7k
R3	20k
C1	0.10 mfd
C2	1.0 mfd 6V
C3	2.2 mfd 6V
C4	250 mfd 6V

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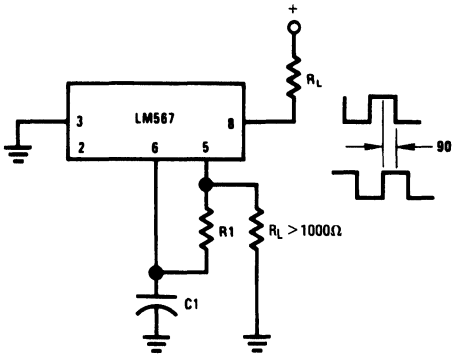
Typical Applications (Continued)

Oscillator with Quadrature Output



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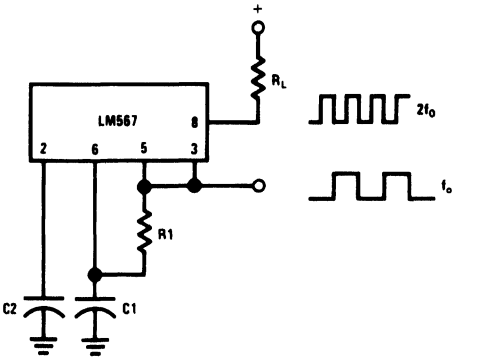
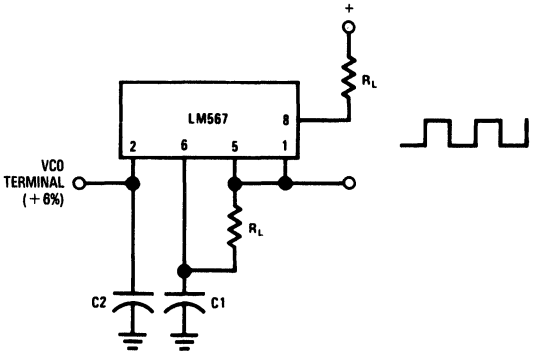
Connect Pin 3 to 2.8V to Invert Output

Oscillator with Double Frequency Output



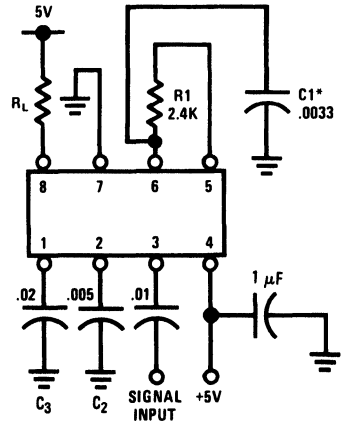
TL/H/6975–7

Precision Oscillator Drive 100 mA Loads



TL/H/6975–8

AC Test Circuit



TL/H/6975–9

f_i = 100 kHz + 5V

***Note:** Adjust for f_o = 100 kHz.

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \cong \frac{1}{1.1\, R_1 C_1}$$

The bandwidth of the filter may be found from the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

Where:

V_i = Input voltage (volts rms), $V_i \leq 200$ mV

C_2 = Capacitance at Pin 2 (μF)

8

National Semiconductor

LM1851 Ground Fault Interrupter

General Description

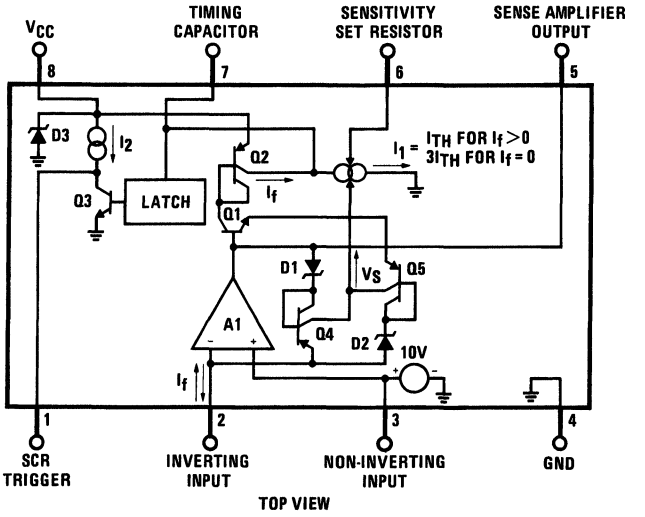
The LM1851 is designed to provide ground fault protection for AC power outlets in consumer and industrial environments. Ground fault currents greater than a presettable threshold value will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. In addition to detection of conventional hot wire to ground faults, the neutral fault condition is also detected.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise. Special features include circuitry that rapidly resets the timing capacitor in the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used.

Features

- Internal power supply shunt regulator
- Externally programmable fault current threshold
- Externally programmable fault current integration time
- Direct interface to SCR
- Operates under line reversal; both load vs line and hot vs neutral
- Detects neutral line faults

Block and Connection Diagram



TL/H/5177–1

Order Number LM1851M or LM1851N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current	19 mA
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−55°C to +150°C

Soldering Information

Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and Their Effects on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1, Without Fault, $V_{pin\ 1}$ Held to 0.3V (Note 4)	2.0	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

AC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

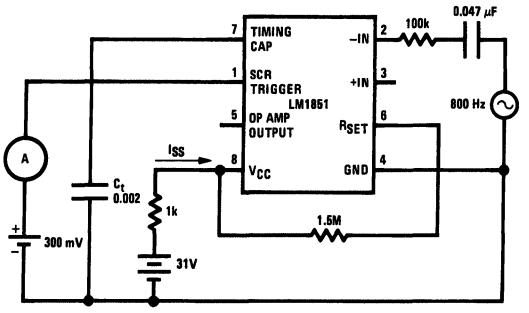
Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	*Figure 1* (Note 3)	3	5	7	mA
Normal Fault Trip Time	500Ω Fault, *Figure 2* (Note 2)		18		ms
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, *Figure 2* (Note 2)		18		ms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient for the DIP and 162°C/W for the SO Package.

Note 2: Average of 10 trials.

Note 3: Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.

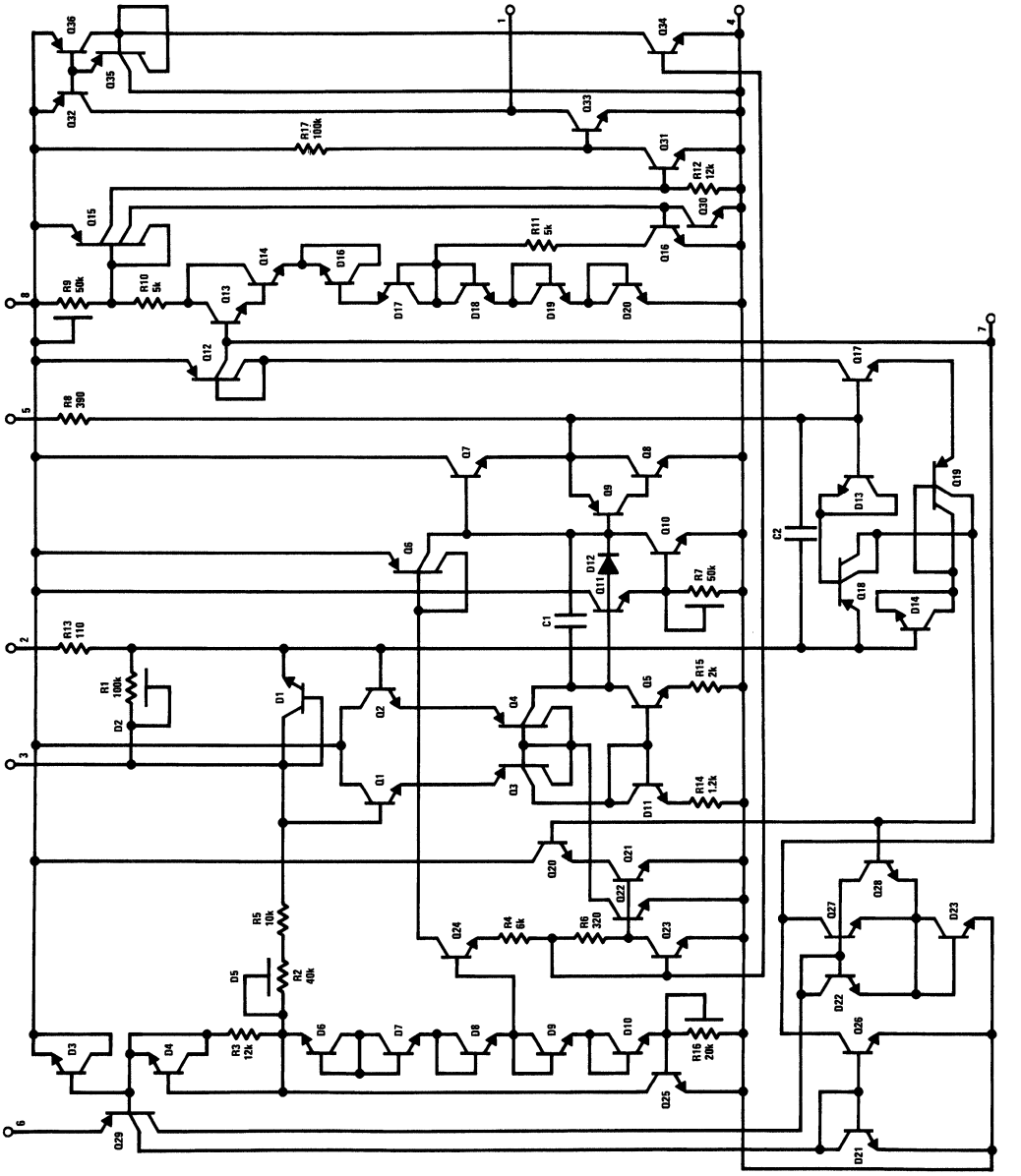
Note 4: This externally applied current is in addition to the internal "output drive current" source.



TL/H/5177–2

FIGURE 1. Normal Fault Sensitivity Test Circuit

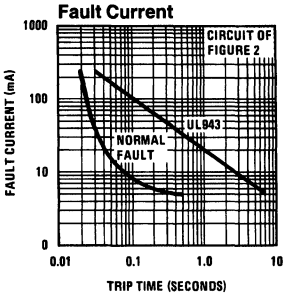
Internal Schematic Diagram



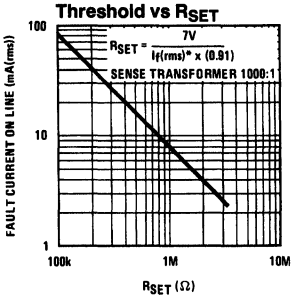
TL/H/5177–3

Typical Performance Characteristics

Average Trip Time vs Fault Current

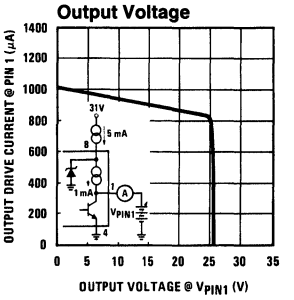


Normal Fault Current Threshold vs R_{SET}

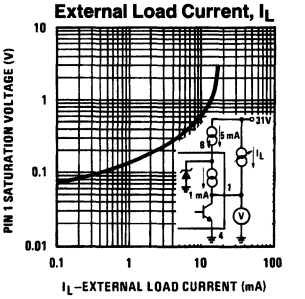


* See Block Diagram

Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I_L



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Circuit Description

(Refer to Block and Connection Diagram)

The LM1851 operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault ($I_f = 0$) the feedback path status signal (V_S) is correspondingly zero. Under these conditions the capacitor discharge current, I_1, sits quiescently at three times its threshold value, I_{TH}, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, I_f, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts I_f. The presence of I_f during either half-cycle will cause V_S to go high, which in turn changes I_1 from $3I_{TH}$ to I_{TH}. Although I_{TH} discharges the timing capacitor during both half-cycles of the line, I_f only charges the capacitor during the half-cycle in which I_f exits pin 2. Thus during one half-cycle $I_f - I_{TH}$ charges the timing capacitor, while during the other half-cycle I_{TH} discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I_2 to drive the gate of an SCR.

Application Circuits

A typical ground fault interrupter circuit is shown in *Figure 2*. It is designed to operate on 120 V_{AC} line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1 μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the IC discharge current increases from I_{TH} to $3I_{TH}$ (see Circuit Description and Block Diagram). This quickly resets both the timing capacitor and the output latch. At this time the circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH}=\frac{7V}{R_{SET}}\div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH}=\frac{I_{f(rms)}}{2}\times 0.91 \qquad (2)$$

where $I_{f(rms)}$ is the rms input fault current to the operational amp and the factor of 2 is due to the fact that I_f charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET}=\frac{7V}{I_{f(rms)}\times 0.91} \qquad (3)$$

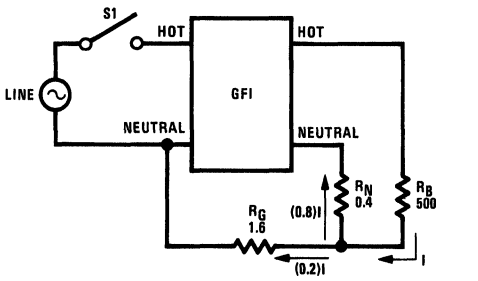
For example, to obtain 5 mA(rms) sensitivity for the circuit in *Figure 2* we have:

$$R_{SET}=\frac{7V}{\frac{5\text{ mA}\times 0.91}{1000}}=1.5\text{M }\Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA–6 mA, provision should be made to adjust R_{SET} on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_t. Due to the large number of variables involved, proper selection of C_t is best done empirically. The following design example, then should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GF1 start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



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UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms Specification

−3 ms GFI turn-on time (15k and 1 μF)

−8 ms Potential loss of one half-cycle due to fault current sense of half-cycles only

−4 ms Time required to open a sluggish circuit breaker

≤10 ms Maximum integration time that could be allowed

8 ms Value of integration time that accommodates component tolerances and other variables

$$C_t=\frac{I\times T}{V} \qquad (5)$$

where T = integration time

V = threshold voltage

I = average fault current into C_t

$$I=\underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\substack{\text{heavy fault current generated (swamps } I_{TH})}}\times\underbrace{\left(\frac{R_N}{R_G+R_N}\right)}_{\substack{\text{portion of fault current shunted around GFI}}}$$

$$\times\underbrace{\left(\frac{1\text{ turn}}{1000\text{ turns}}\right)}_{\substack{\text{current division of input sense transformer}}}\times\underbrace{\left(\frac{1}{2}\right)}_{\substack{C_t\text{ charging on half-cycles only}}}\times\underbrace{(0.91)}_{\substack{\text{rms to average conversion}}} \qquad (6)$$

therefore:

$$C_t=\frac{\left[\left(\frac{120}{500}\right)\times\left(\frac{0.4}{1.6+0.4}\right)\times\left(\frac{1}{1000}\right)\times\left(\frac{1}{2}\right)\times(0.91)\right]\times 0.0008}{17.5} \qquad (7)$$

$C_t=$ 0.01 μF

Application Circuits (Continued)

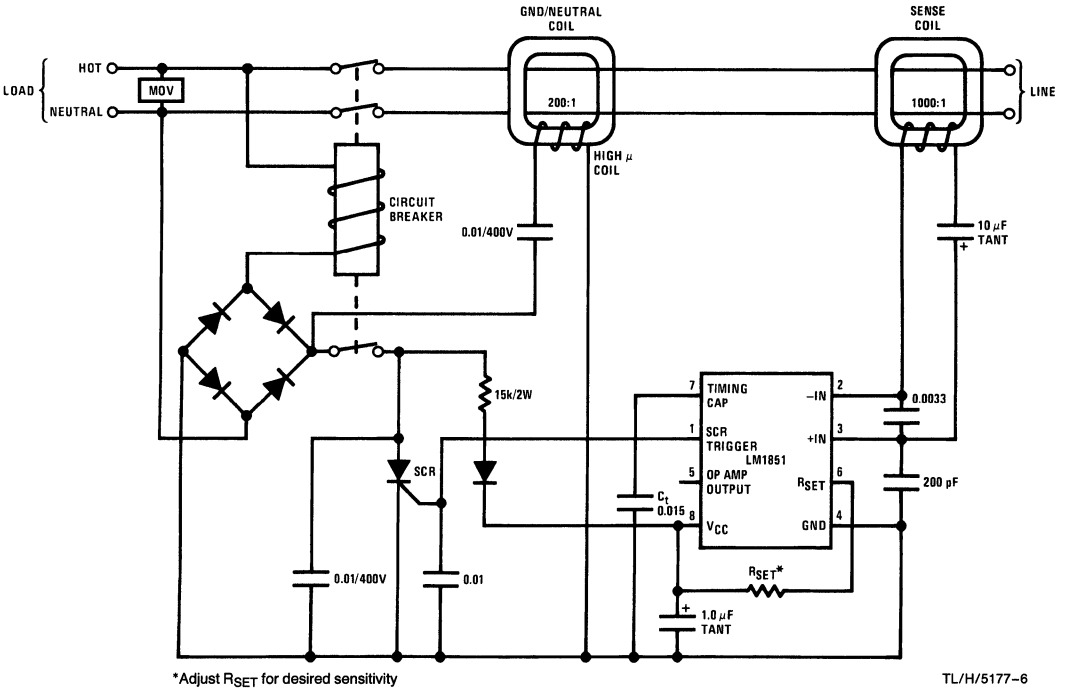
in practice, the actual value of C1 will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C1.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In *Figure 2*, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Typical Application



*Adjust R_{SET} for desired sensitivity

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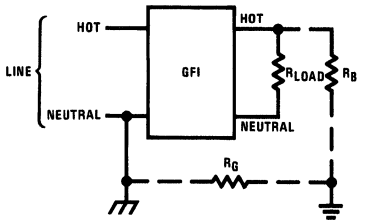
FIGURE 2. 120 Hz Neutral Transformer Approach

Definition of Terms

Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



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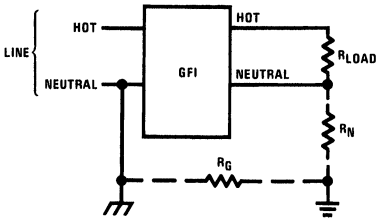
Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



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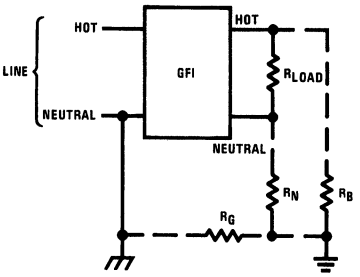
Normal Fault plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



TL/H/5177–9

National Semiconductor

LM2240
Programmable Timer/Counter

General Description

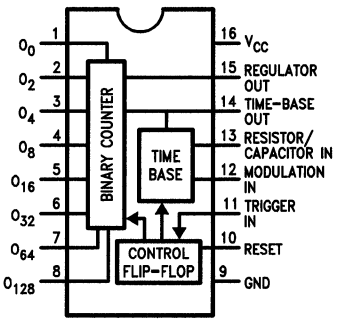
The LM2240 Programmable Timer/Counter is a monolithic controller capable of both monostable and astable operation. Monostable operation allows accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor-capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, a single RC network sets the base frequency. The frequencies of the squarewaves at the 8 outputs are each at different factors of 2 from the base frequency. If 2 or more of the outputs are shorted together, various pulse patterns can be generated. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and CMOS compatible for easy interface with digital systems. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

Features

- Accurate timing from microseconds to days
- Programmable delays from 1 RC to 255 RC
- TTL and CMOS compatible outputs
- Timing directly proportional to RC time constant
- High accuracy
- External sync and modulation capability
- Wide supply voltage range
- Excellent supply voltage rejection

Connection Diagram

16-Lead Molded DIP



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Top View

See NS Package Number N16E
Order Number LM2240N

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Molded DIP	−65°C to +150°C
Lead Temperature	
Molded DIP (Soldering, 10 Sec.)	265°C
Power Dissipation (Note 2)	1.8W
Junction Temperature	150°C
Supply Voltage	18V
Output Current	10 mA
Output Voltage	18V
Regulator Output Current	5.0 mA
ESD Tolerance (Note 3)	2000V

Operating Ratings

Temperature Range	0°C to 70°C
Supply Range (Note 4)	4V to 15V

LM2240

Electrical Characteristics

T_A = +25°C, V_{CC} = +5.0V, R = 10 kΩ, C = 0.1 μF, unless otherwise specified. See Block Diagram.

Symbol	Characteristic		Conditions		Min	Typ	Max	Units
GENERAL CHARACTERISTIC								
I_{CC}	Supply Current	Total Circuit	V_{CC} = 5.0V, V_{TR} = 0V, V_{RS} = 5.0V			4.0	7.0	mA
			V_{CC} = 15V, V_{TR} = 0V, V_{RS} = 5.0V			13	18	
		Counter Only				1.5		
V_{REG}	Regulator Output		Measured at Pin 15	V_{CC} = 5.0V	3.9	4.4		V
				V_{CC} = 15V	5.8	6.3	6.8	
TIME-BASE								
t_{ACC}	Timing Accuracy (Note 5)		V_{RS} = 0, V_{TR} = 5.0V			3.5	5.0	%
Δt/ΔT	Timing Shift with Temperature		0°C ≤ T_J ≤ 70°C	V_{CC} = 5.0V		200		ppm/°C
				V_{CC} = 15V		80		
Δt/ΔV	Timing Shift with Supply		V_{CC} ≥ 8.0V			0.08	0.3	%/V
f_{MAX}	Max Frequency		R = 1.0 kΩ, C = 0.007 μF			130		kHz
V_{MOD}	Modulation Voltage Level		Measured at Pin 12	V_{CC} = 5.0V	2.80	3.50	4.20	V
				V_{CC} = 15V		10.5		
R_T	Recommended Range of Timing Resistor				0.001		10	MΩ
C_T	Recommended Range of Timing Capacitor (Note 6)				0.01		1000	μF

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur.

Note 2: Rating applies to ambient temperature at 25°C. Above this temperature, derate at 15 mW/°C.

Note 3: Human body model, C = 100 pF, R_S = 1500Ω.

Note 4: For operation below 4.5 VDC, short pin 15 to pin 16.

Note 5: Timing error solely introduced by LM2240 measured as % of ideal time-base period of T = RC.

Note 6: Under the conditions of high supply voltages (V_{CC} > 7.0V) and low values of timing capacitor (C_T < 0.1 μF), a 600 pF capacitor may need to be connected from pin 14 to ground to ensure proper operation.

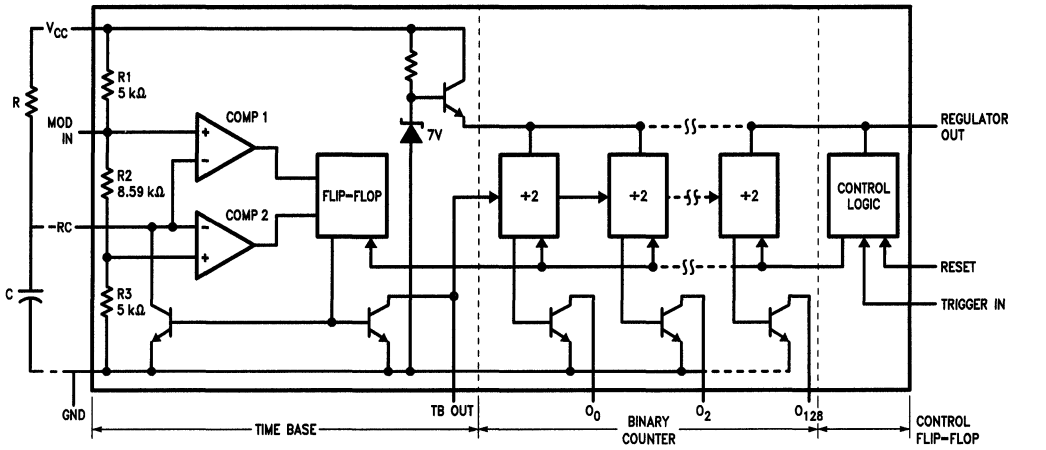
Electrical Characteristics

$T_A = +25°C$, $V_{CC} = +5.0V$, R = 10 kΩ, C = 0.1 μF, unless otherwise specified. See Block Diagram.

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
TRIGGER/RESET CONTROLS						
V_{TR}	Trigger Threshold	Measured at Pin 11, $V_{RS} = 0V$		1.4	2.0	V
I_{TR}	Trigger Current	$V_{RS} = 0V$, $V_{TR} = 2.0V$		10		μA
Z_T	Trigger Impedance			25		kΩ
t_{RSPT}	Trigger Response Time (Note 7)			1.0		μs
V_{RS}	Reset Threshold	Measured at Pin 10, $V_{TR} = 0V$		1.4	2.0	V
I_R	Reset Current	$V_{TR} = 0V$, $V_{RS} = 2.0V$		10		μA
Z_R	Reset Impedance			25		kΩ
t_{RSPT}	Reset Response Time (Note 7)			0.8		μs
COUNTER						
TR_{MAX}	Max Toggle Rate	Measured at Pin 14 $V_{RS} = 0V$, $V_{TR} = 5.0V$		1.5		MHz
Z_I	Input Impedance			20		kΩ
V_{TH}	Input Threshold		1.0	1.4		V
t_r	Output Rise Time	Measured at Pins 1 through 8 $R_L = 3.0$ kΩ, $C_L = 10$ pF		180		ns
t_f	Output Fall Time			180		
I_{O-}	Sink Current	$V_{OL} \leq 0.4V$	2.0	4.0		mA
I_{CEX}	Leakage Current	$V_{OH} = 15V$		0.01	15	μA

Note 7: Propagation delay from application of trigger or reset input to corresponding state change in counter output at Pin 1.

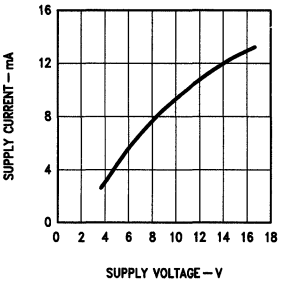
Block Diagram



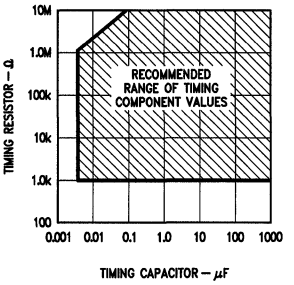
TL/H/10837–2

Typical Performance Characteristics

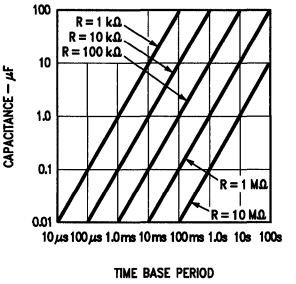
Supply Current vs Supply Voltage in Reset Condition



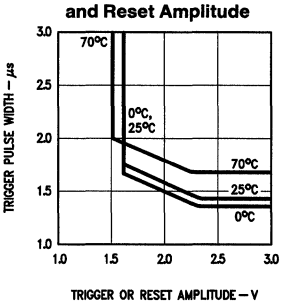
Recommended Range of Timing Component Values (Note 7)



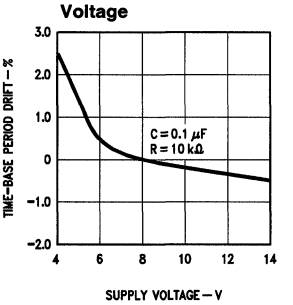
Time-Base Period vs External RC



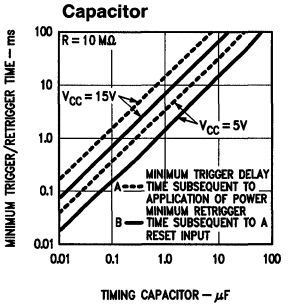
Minimum Trigger and Reset Pulse Widths vs Trigger and Reset Amplitude



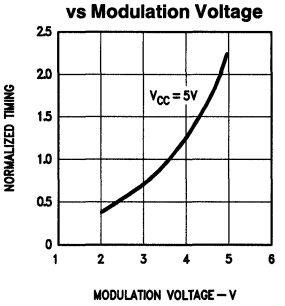
Time-Base Period Drift vs Supply Voltage



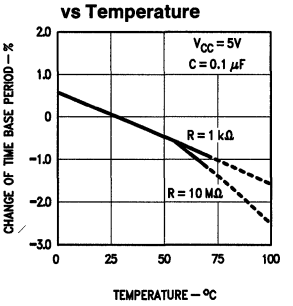
Minimum Trigger/Retrigger Timing vs Timing Capacitor



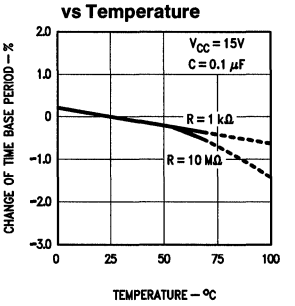
Normalized Change in Time-Base Period vs Modulation Voltage



Time-Base Period vs Temperature

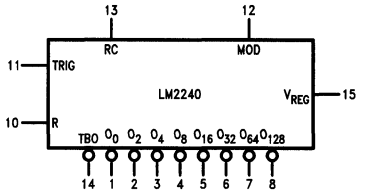


Time-Base Period vs Temperature



TL/H/10837–3

Functional Description



TL/H/10837–4

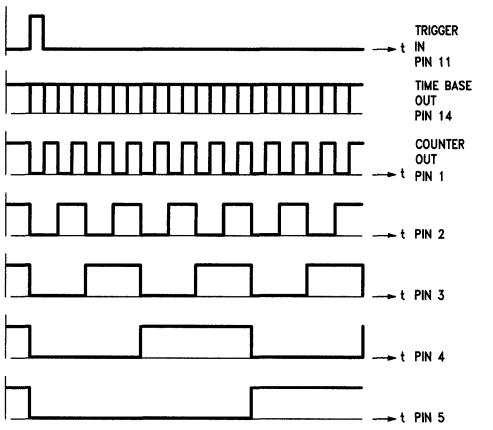
V_{CC} = Pin 16
GND = Pin 9

FIGURE 1. Logic Symbol

When power is applied to the LM2240 with no trigger or reset inputs activated, the circuit starts with all outputs HIGH. Application of a positive going trigger pulse to the trigger pin initiates the timing cycle. The trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC; this is the period of the waveform appearing at pin 14. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive going reset pulse is applied to the Reset pin.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

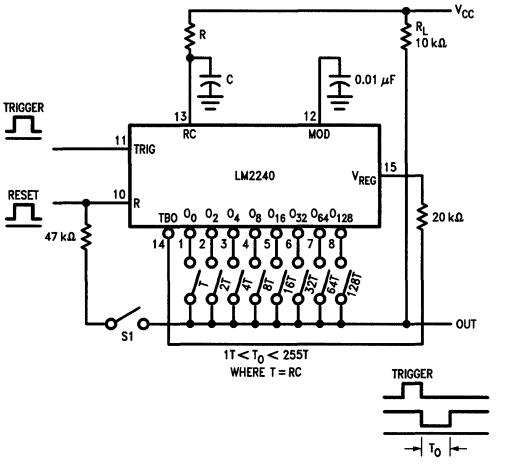
Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.



TL/H/10837–5

FIGURE 2. Timing Diagram of Output Waveforms

In monostable applications, one or more of the counter outputs are connected to the reset terminal with S1 closed *(Figure 3)*. The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. Each of the various multiples of T shown at the LM2240's outputs in *Figure 3* represent the duration of time, after a trigger pulse, that that particular output is low (it's *not* the period of the waveform) if the output is not tied to any other outputs. T_O represents the duration of time that the circuit output, which is the common point of all the counter outputs which are shorted together, is low. If none of the counter outputs are connected back to the reset terminal (switch S1 open), the circuit operates in an astable or free running mode, following a trigger input.



TL/H/10837–6

FIGURE 3. Basic Circuit Connection for Timing Applications (Monostable: S1 Closed; Astable: S1 Open)

Important Operating Information

Ground connection is pin 9.

Reset (R) (pin 10) sets all outputs HIGH.

Trigger (TRIG) (pin 11) sets all outputs LOW.

Time-base output (TBO) (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1.0 kΩ resistor.

Normal TBO (pin 14) is a negative going pulse greater than 500 ns.

NOTE: Under the conditions of high supply voltages (V_{CC} > 7.0V) and low values of timing capacitor (C_T < 0.1 μF), the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from TBO (pin 14) to ground (pin 9).

Reset (pin 10) stops the time-base oscillator.

Outputs (O_0 . . . O_{128}) (pins 1–8) sink 2.0 mA current with $V_{OL} \leq 0.4V$.

For use with external clock, minimum clock pulse amplitude should be 3.0V, with greater than 1.0 μs pulse duration.

Circuit Controls

Counter Outputs ($O_0 \ldots O_{128}$, Pins1 thru 8)

The binary counter outputs are buffered open collector type stages, as shown in the block diagram. Each output is capable of sinking 2.0 mA at 0.4V V_{OL}. In the reset condition, all the counter outputs are HIGH or in the nonconducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the programming segment of this datasheet.

Reset and Trigger Inputs (R and TRIG, Pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops ($\approx$ 1.4V) above ground. Minimum pulse widths for reset and trigger inputs are shown in the Performance Curves. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, Pin 12)

The oscillator time-base period (T) can be modulated by applying a DC voltage to MOD, pin 12 (see Performance Curves). Also, the time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12 as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

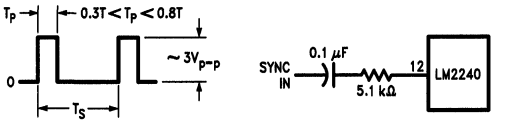


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FIGURE 4. Operation with External Sync Signal

The time-base can be synchronized by setting the sync pulse period (T_S) to be an integer multiple of T. This can be done by choosing the timing components R and C at pin 13 such that:

$T = RC = (T_S/m)$

where:

m is an integer, $1 \leq m \leq 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of the time-base frequency.

RC Terminal (Pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period $T = 1$ RC.

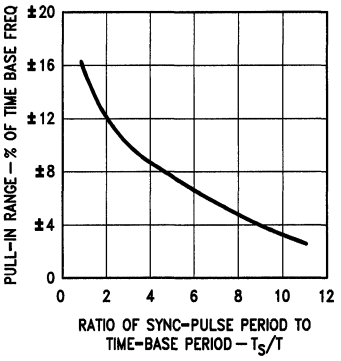

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FIGURE 5. Typical Pull-in Range for Harmonic Synchronization

Time-Base Output (TBO, Pin 14)

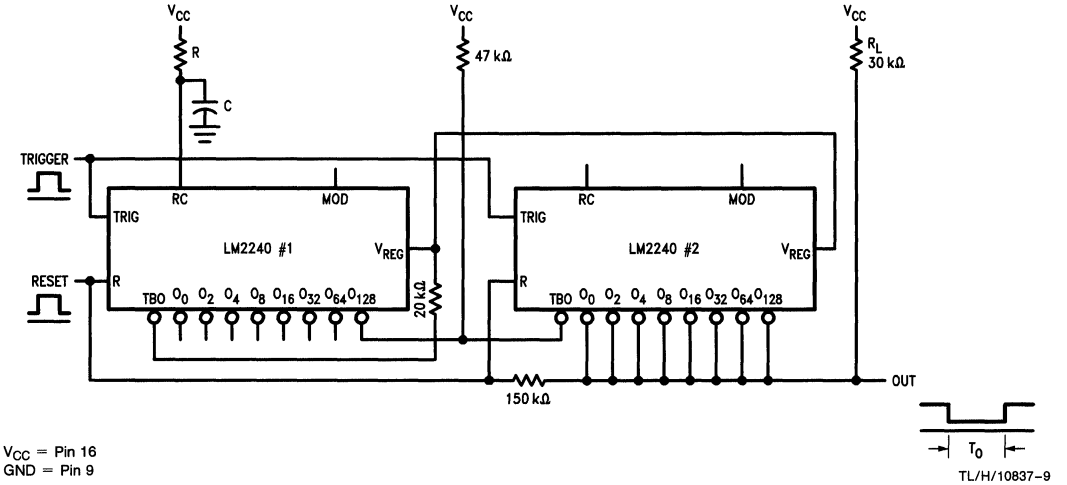
The time-base output is an open-collector type stage as shown in the block diagram, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is $\approx +1.4$V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltage ($V_{CC} > 7.0$V) and a small value timing capacitor ($C_T < 0.1$ μF), the pulse width at TBO pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from pin 14 to ground.

Regulator Output (V_{REG}, Pin 15)

The regulator output V_{REG} is used internally to power the binary counter and the control logic. This terminal can also be used as a supply to additional LM2240 circuits when several timer circuits are cascaded (see *Figure 6*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal so that the internal time-base circuitry is not powered, thus reducing power dissipation. When supply voltages less than 4.5V are used with the internal time-base, pin 15 should be shorted to pin 16.

Circuit Controls (Continued)



V_{CC} = Pin 16
GND = Pin 9

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FIGURE 6. Low Power Operation of Cascaded Timers

Monostable Operation

Precision Timing

In precision timing applications, the LM2240 is used in its monostable, or self-resetting, mode. The generalized circuit connection for this application is shown in *Figure 3* (S1 closed). The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration (T_O) and then returns to a HIGH state. The duration of the timing cycle T_O is given as:

$T_O = nT = NRC$

where T = RC is the time-base period as set by the choice of timing components at RC pin 13 (see Performance Curves) and n is an integer in the range of $1 \leq n \leq 255$ as determined by the combination of counter outputs ($O_0 \ldots O_{128}$), pins 1 through 8 connected to the output bus.

Counter Output Programming

The binary counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW The time delays associated with each counter output can thus be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1T \leq T_O \leq 255T$.

Ultra Long Time Delay Application

Two LM2240 units can be cascaded as shown in *Figure 7* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}280$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the reset and the trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of 256 (255) or 65,280 cycles of the time-base oscillator.

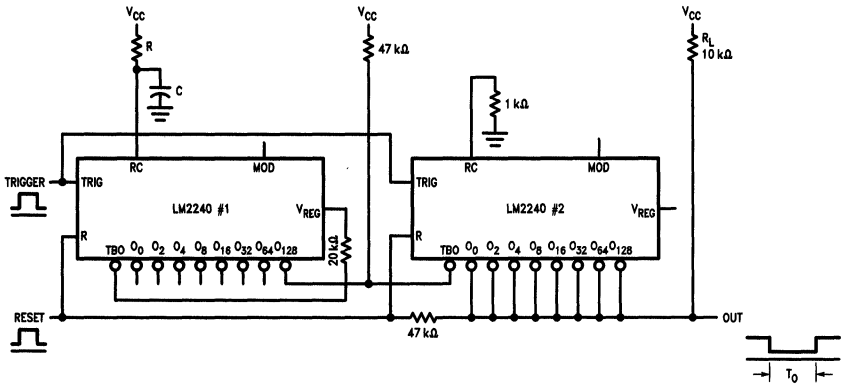
In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 6*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pin 15) of both units together.

Astable Operation

The LM2240 can be operated in its astable or free running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive going reset signal to pin 10, the circuit reverts back to its reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self triggers automatically when the power supply is turned on, and continues to operate in its free running mode indefinitely. In astable or free running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Astable Operation (Continued)



VCC = Pin 16
GND = Pin 9

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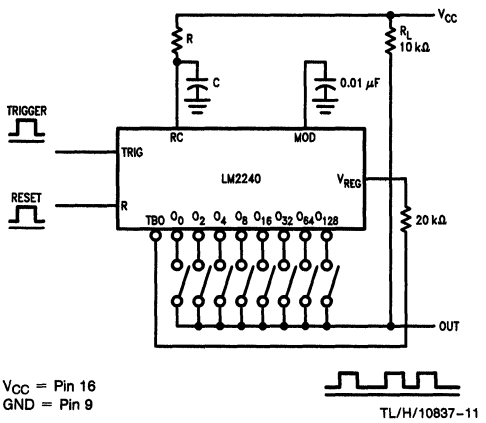
FIGURE 7. Cascaded Operation for Long Delays

Binary Pattern Generation

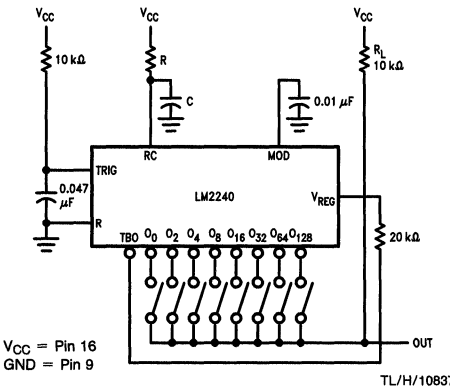
In astable operation, as shown in *Figures 8* and *9*, the output of the LM2240 appears as a complex pulse pattern if more than one of its switches is closed. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2*, which shows the phase relations between the counter outputs. *Figures 10* and *11* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.



VCC = Pin 16
GND = Pin 9

TL/H/10837–11

FIGURE 8. Astable Operation with Trigger and Reset Inputs



VCC = Pin 16
GND = Pin 9

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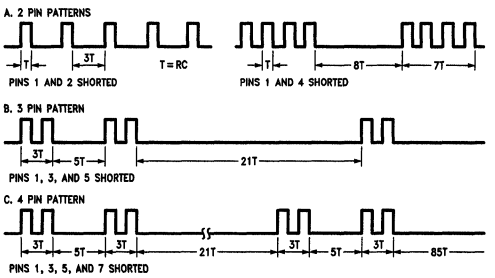
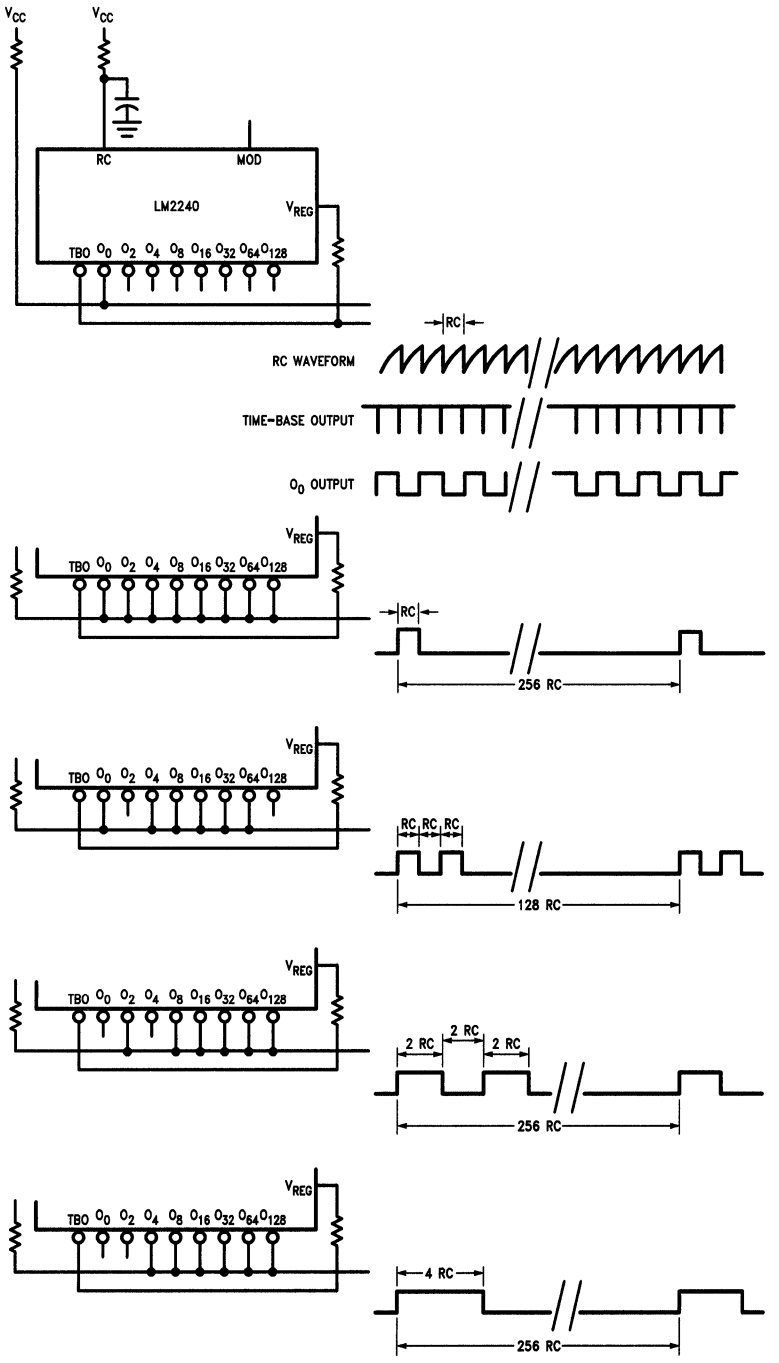
FIGURE 9. Free Running Astable Operation



TL/H/10837–13

FIGURE 10. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

Astable Operation (Continued)



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VCC = Pin 16
GND = Pin 9

FIGURE 11. Astable Operation Examples of Output

National Semiconductor

LM2907/LM2917 Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

Features

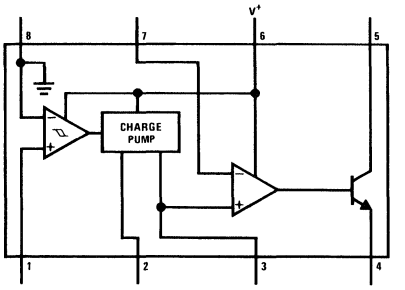
- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

Applications

- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

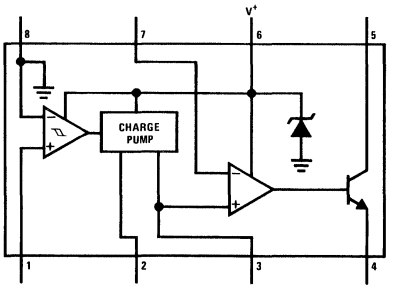
Block and Connection Diagrams

Dual-In-Line and Small Outline Packages, Top Views



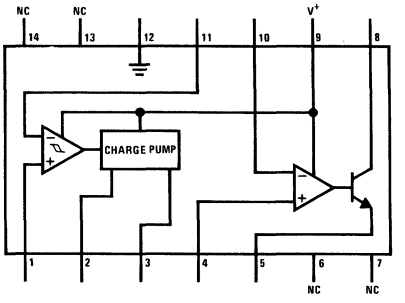
TL/H/7942-1

Order Number LM2907N-8
See NS Package Number N08E



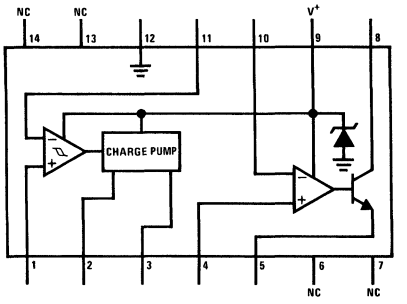
TL/H/7942-2

Order Number LM2917N-8
See NS Package Number N08E



TL/H/7942-3

Order Number LM2907N
See NS Package Number N14A



TL/H/7942-4

Order Number LM2917M or LM2917N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	28V
Supply Current (Zener Options)	25 mA
Collector Voltage	28V
Differential Input Voltage	
Tachometer	28V
Op Amp/Comparator	28V
Input Voltage Range	
Tachometer LM2907-8, LM2917-8	±28V
LM2907, LM2917	0.0V to +28V
Op Amp/Comparator	0.0V to +28V
Power Dissipation	
LM2907-8, LM2917-8	1200 mW
LM2907-14, LM2917-14 (See Note 1)	1580 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TACHOMETER						
	Input Thresholds	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)	±10	±25	±40	mV
	Hysteresis	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)		30		mV
	Offset Voltage	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)				
	LM2907/LM2917			3.5	10	mV
	LM2907-8/LM2917-8			5	15	mV
	Input Bias Current	V_{IN} = ±50 mV_{DC}		0.1	1	μA
V_{OH}	Pin 2	V_{IN} = +125 mV_{DC} (Note 3)		8.3		V
V_{OL}	Pin 2	V_{IN} = −125 mV_{DC} (Note 3)		2.3		V
I_2, I_3	Output Current	V2 = V3 = 6.0V (Note 4)	140	180	240	μA
I_3	Leakage Current	I2 = 0, V3 = 0			0.1	μA
K	Gain Constant	(Note 3)	0.9	1.0	1.1	
	Linearity	f_{IN} = 1 kHz, 5 kHz, 10 kHz (Note 5)	−1.0	0.3	+1.0	%
OP/AMP COMPARATOR						
V_{OS}		V_{IN} = 6.0V		3	10	mV
I_{BIAS}		V_{IN} = 6.0V		50	500	nA
	Input Common-Mode Voltage		0		V_{CC}−1.5V	V
	Voltage Gain			200		V/mV
	Output Sink Current	V_C = 1.0	40	50		mA
	Output Source Current	V_E = V_{CC} −2.0		10		mA
	Saturation Voltage	I_{SINK} = 5 mA		0.1	0.5	V
		I_{SINK} = 20 mA			1.0	V
		I_{SINK} = 50 mA		1.0	1.5	V

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Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZENER REGULATOR						
	Regulator Voltage	R_{DROP} = 470Ω		7.56		V
	Series Resistance			10.5	15	Ω
	Temperature Stability			+1		mV/°C
	TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 101°C/W junction to ambient for LM2907-8 and LM2917-8, and 79°C/W junction to ambient for LM2907-14 and LM2917-14.

Note 2: Hysteresis is the sum $+V_{TH} - (-V_{TH})$, offset voltage is their difference. See test circuit.

Note 3: V_{OH} is equal to $\frac{3}{4} \times V_{CC} - 1\ V_{BE}$, V_{OL} is equal to $\frac{1}{4} \times V_{CC} - 1\ V_{BE}$ therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

Note 4: Be sure when choosing the time constant R1 × C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with $I_3 \times$ R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10 MΩ typically.

Note 5: Nonlinearity is defined as the deviation of V_{OUT} (@ pin 3) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10 kHz. C1 = 1000 pF, R1 = 68k and C2 = 0.22 mFd.

General Description (Continued)

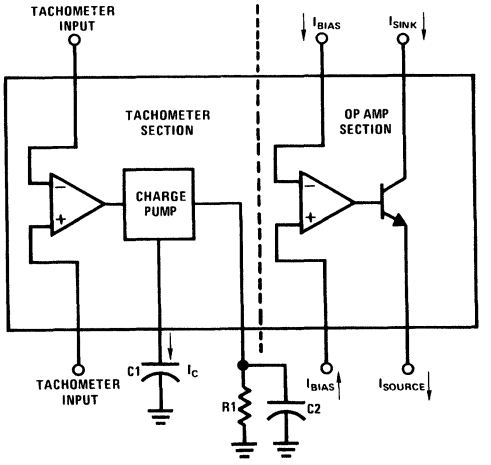
The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Test Circuit and Waveform



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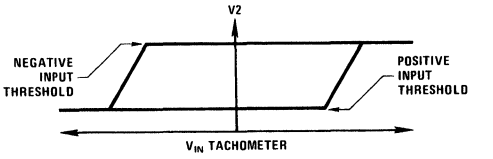
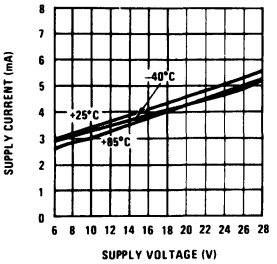
Tachometer Input Threshold Measurement



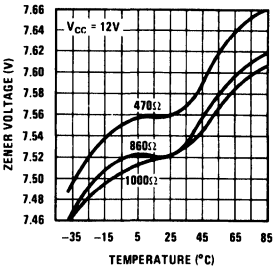
TL/H/7942–7

Typical Performance Characteristics

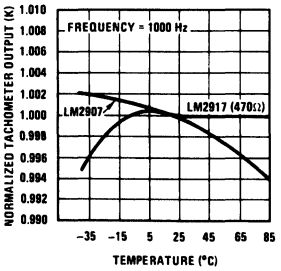
Total Supply Current



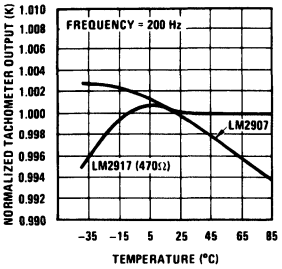
Zener Voltage vs Temperature



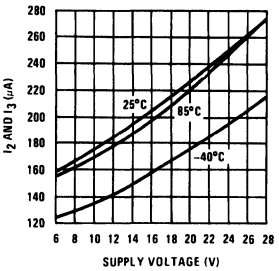
Normalized Tachometer Output vs Temperature



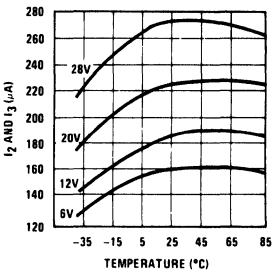
Normalized Tachometer Output vs Temperature



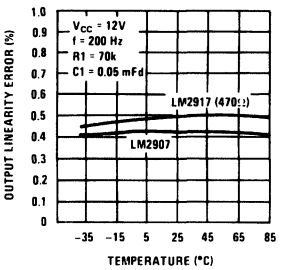
Tachometer Currents I_2 and I_3 vs Supply Voltage



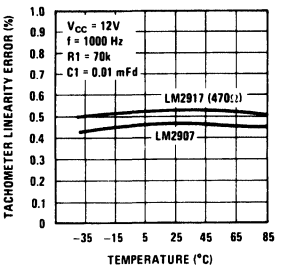
Tachometer Currents I_2 and I_3 vs Temperature



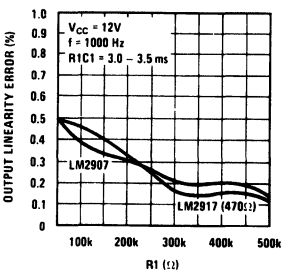
Tachometer Linearity vs Temperature



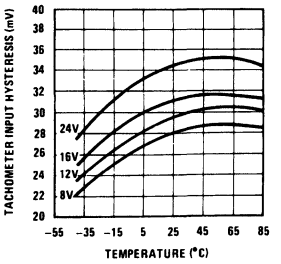
Tachometer Linearity vs Temperature



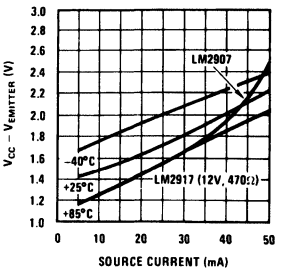
Tachometer Linearity vs R1



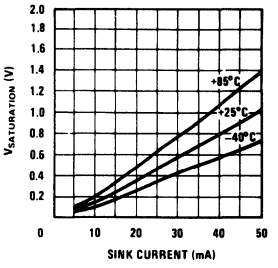
Tachometer Input Hysteresis vs Temperature



Op Amp Output Transistor Characteristics



Op Amp Output Transistor Characteristics



TL/H/7942–5

Applications Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. In order to fully exploit its features and advantages let's examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (LM2907-8, LM2917-8) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended ac output. This single input is also fully protected against voltage swings to ±28V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course in order to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a dc voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to $1/2\ f_{IN}$ the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor then is:

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2f_{IN}) = V_{CC} \times f_{IN} \times C1$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor, then $V_O = i_c \times R1$, and the total conversion equation becomes:

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K$$

Where K is the gain constant—typically 1.0.

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

CHOOSING R1 AND C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 500 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{ pk-pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1 and I_2:

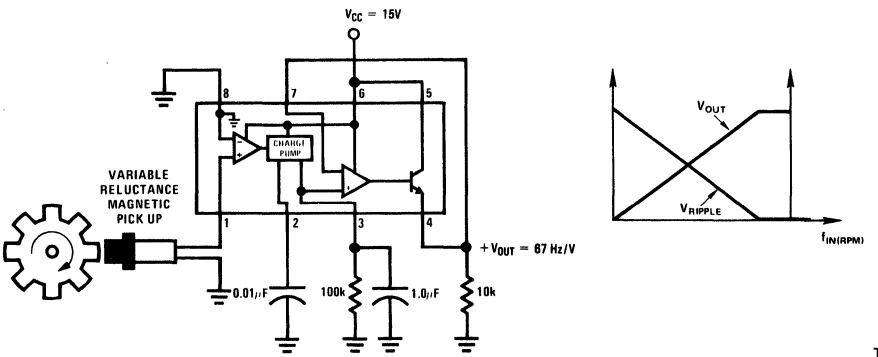
$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}}$$

USING ZENER REGULATED OPTIONS (LM2917)

For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize the zener voltage variation to 160 mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation.

Typical Applications

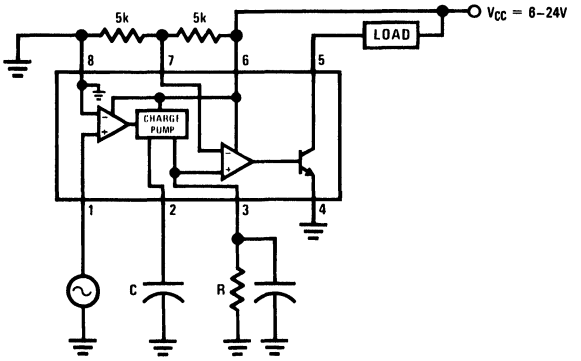
Minimum Component Tachometer



TL/H/7942–8

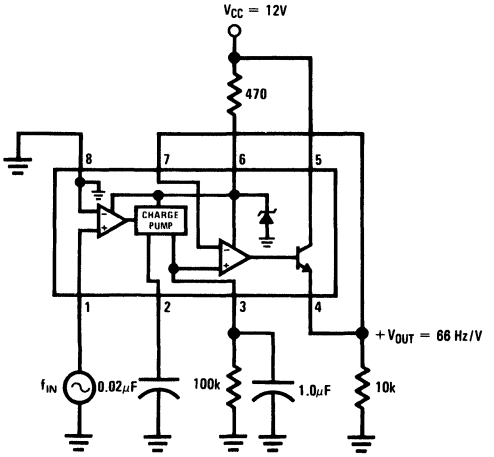
Typical Applications (Continued)

"Speed Switch" Load is Energized When $f_{IN} \geq \frac{1}{2RC}$



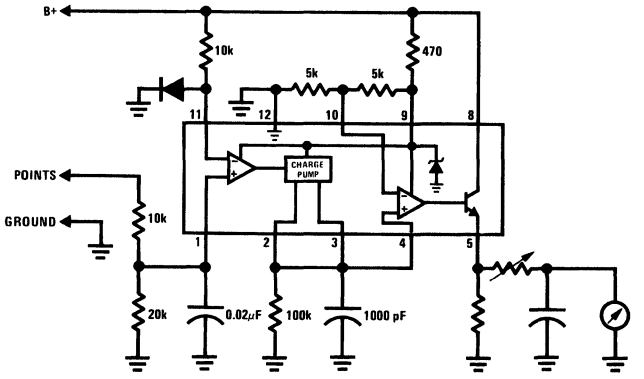
TL/H/7942–9

Zener Regulated Frequency to Voltage Converter



TL/H/7942–10

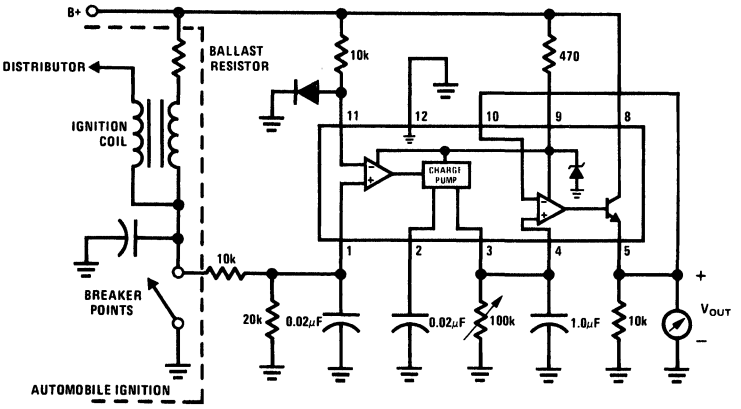
Breaker Point Dwell Meter



TL/H/7942–11

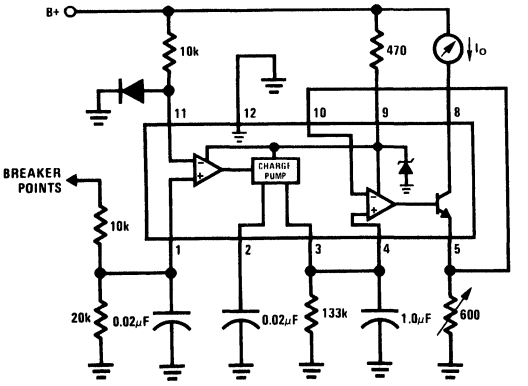
Typical Applications (Continued)

Voltage Driven Meter Indicating Engine RPM
V_O = 6V @ 400 Hz or 6000 ERPM (8 Cylinder Engine)



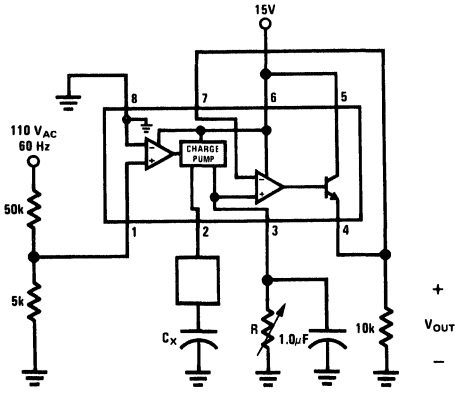
TL/H/7942–12

Current Driven Meter Indicating Engine RPM
I_O = 10 mA @ 300 Hz or 6000 ERPM (6 Cylinder Engine)



TL/H/7942–13

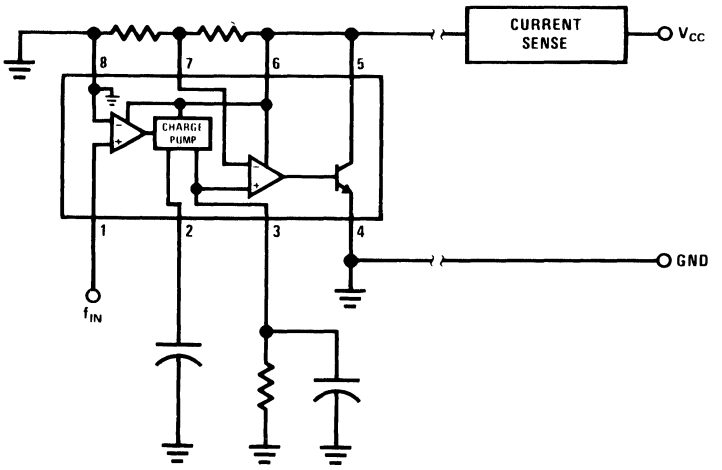
Capacitance Meter
V_{OUT} = 1V–10V for C_X = 0.01 to 0.1 mFd
(R = 111k)



TL/H/7942–14

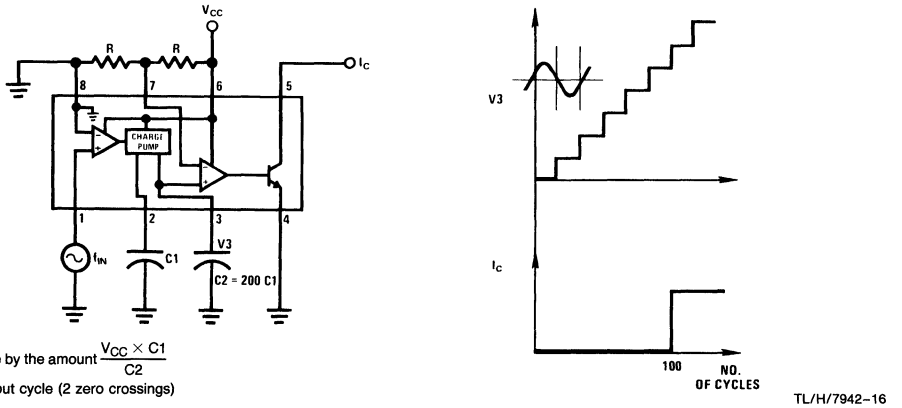
Typical Applications (Continued)

Two-Wire Remote Speed Switch



TL/H/7942–15

100 Cycle Delay Switch



TL/H/7942–16

V3 steps up in voltage by the amount $\frac{V_{CC} \times C1}{C2}$

for each complete input cycle (2 zero crossings)

Example:

If C2 = 200 C1 after 100 consecutive input cycles.

V3 = 1/2 V_{CC}

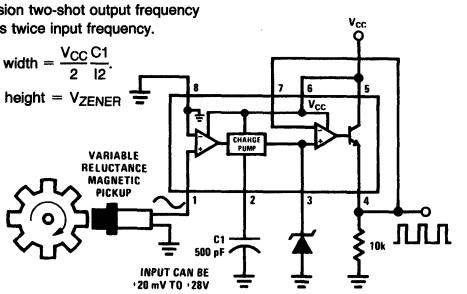
Typical Applications (Continued)

Variable Reluctance Magnetic Pickup Buffer Circuits

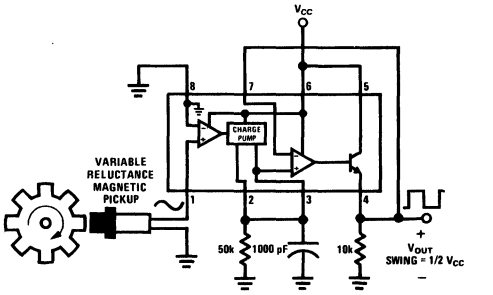
Precision two-shot output frequency equals twice input frequency.

Pulse width = $\frac{V_{CC}}{2} \frac{C1}{I2}$.

Pulse height = V_{ZENER}

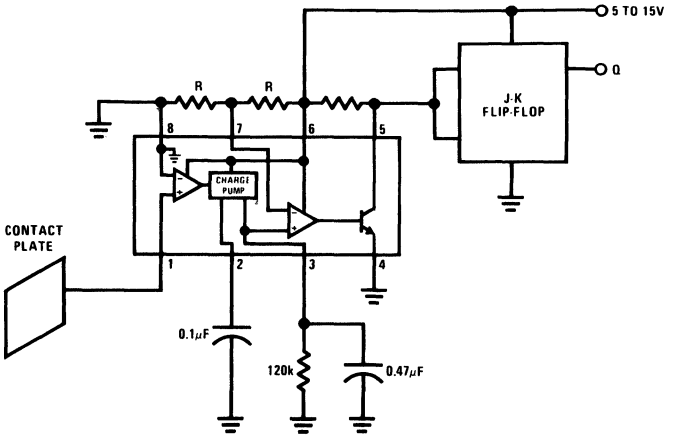


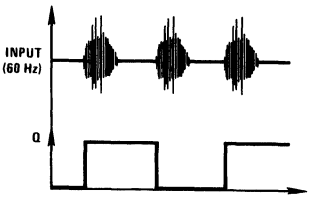
TL/H/7942-39



TL/H/7942-17

Finger Touch or Contact Switch

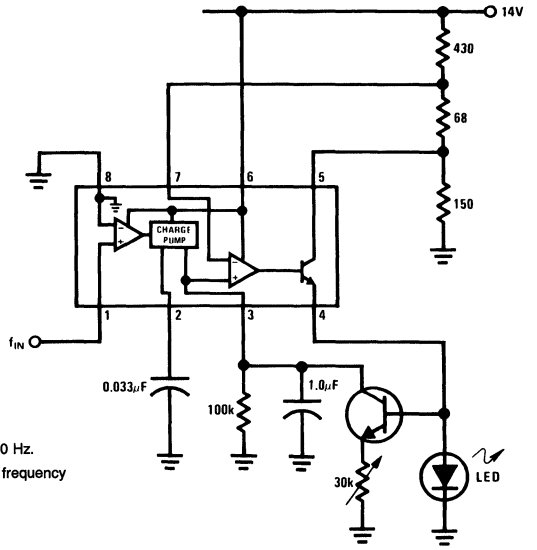




TL/H/7942-19

TL/H/7942-18

Flashing LED Indicates Overspeed



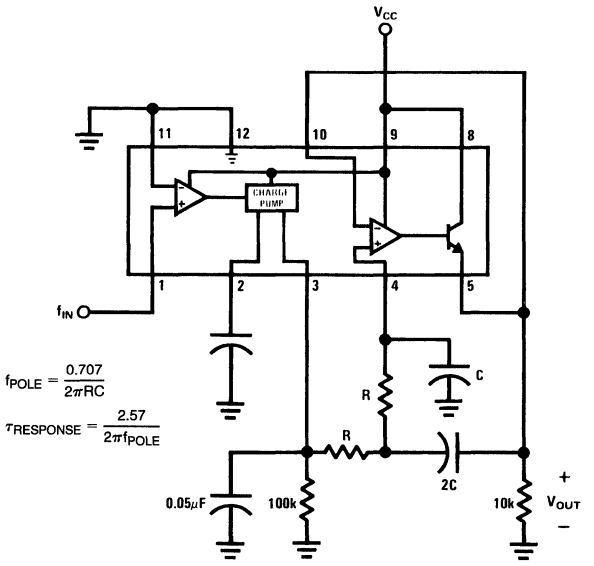
Flashing begins when $f_{IN} \geq 100$ Hz.

Flash rate increases with input frequency increase beyond trip point.

TL/H/7942-20

Typical Applications (Continued)

Frequency to Voltage Converter with 2 Pole Butterworth Filter to Reduce Ripple

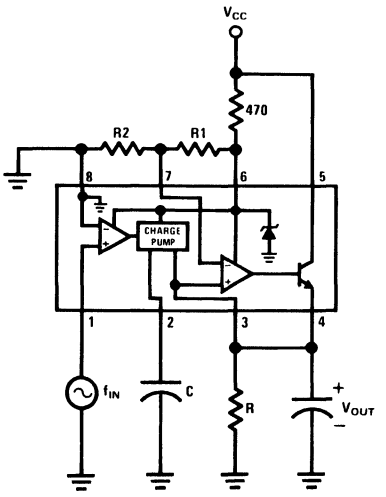


$$f_{POLE} = \frac{0.707}{2\pi RC}$$

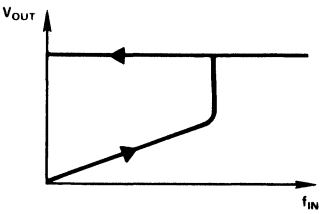
$$\tau_{RESPONSE} = \frac{2.57}{2\pi f_{POLE}}$$

TL/H/7942-21

Overspeed Latch



TL/H/7942-22



TL/H/7942-23

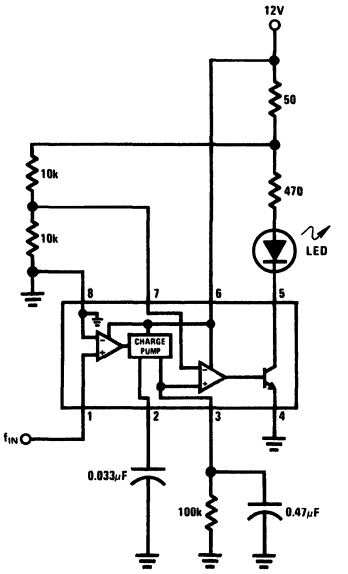
Output latches when

$$f_{IN} = \frac{R2}{R1 + R2} \frac{1}{RC}$$

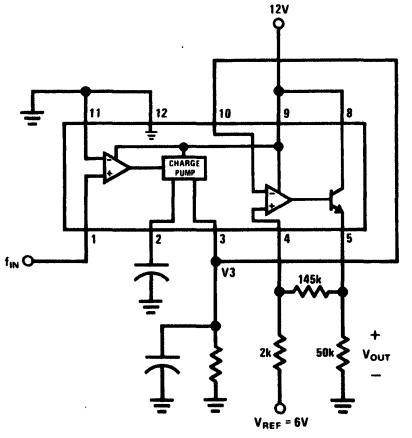
Reset by removing V_{CC}.

Typical Applications (Continued)

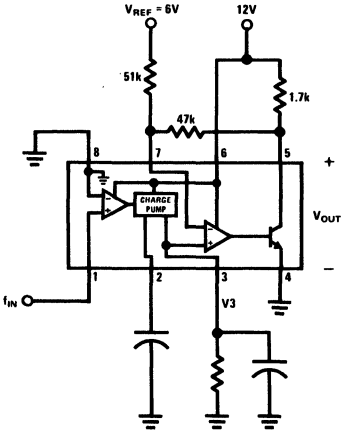
Some Frequency Switch Applications May Require Hysteresis in the Comparator Function Which can be Implemented in Several Ways:



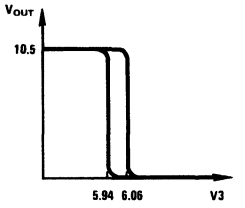
TL/H/7942–24



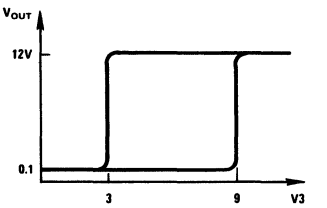
TL/H/7942–25



TL/H/7942–26



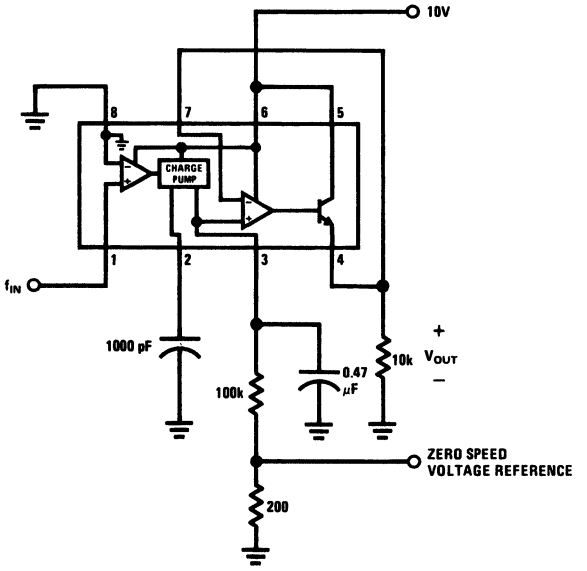
TL/H/7942–27

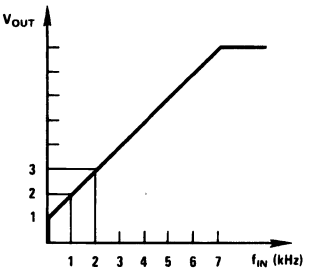


TL/H/7942–28

Typical Applications (Continued)

Changing the Output Voltage for an Input Frequency of Zero

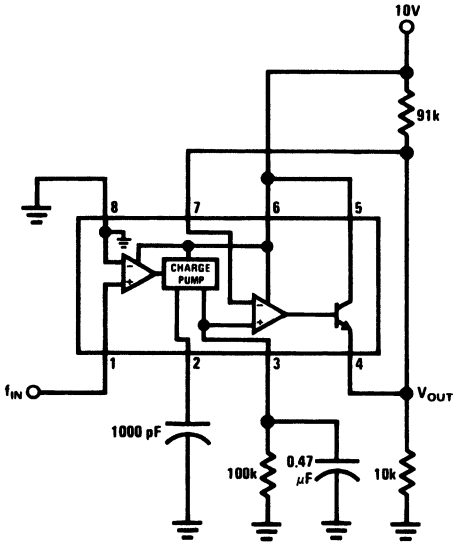


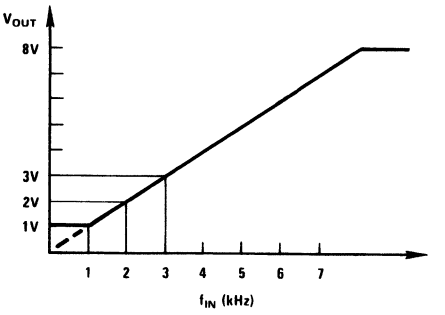


TL/H/7942–30

TL/H/7942–29

Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage





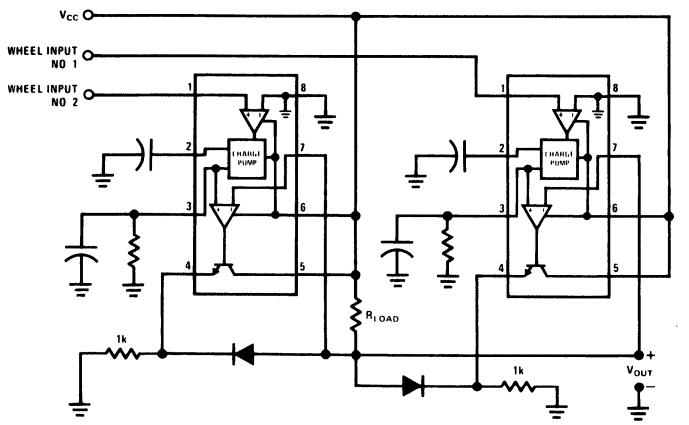
TL/H/7942–32

TL/H/7942–31

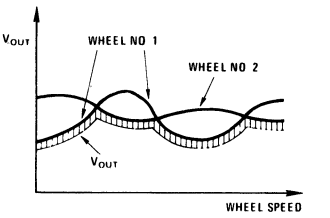
8

Anti-Skid Circuit Functions

"Select-Low" Circuit



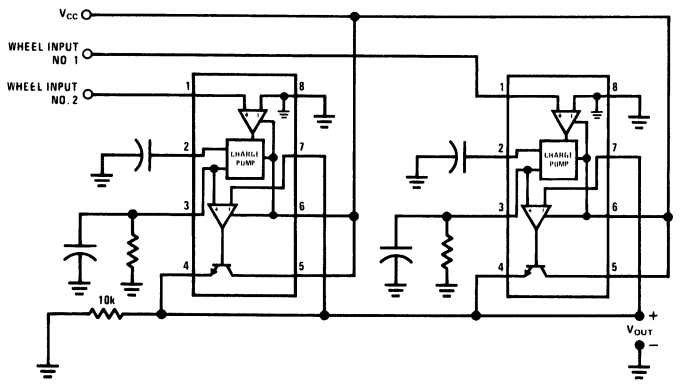
TL/H/7942–33



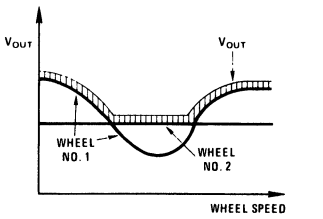
TL/H/7942–34

V_{OUT} is proportional to the lower of the two input wheel speeds.

"Select-High" Circuit



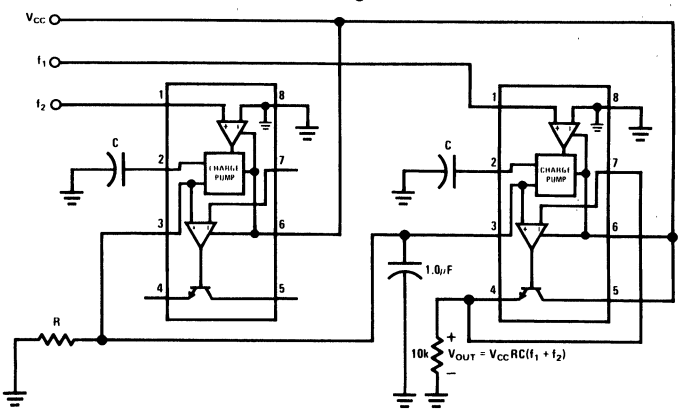
TL/H/7942–35



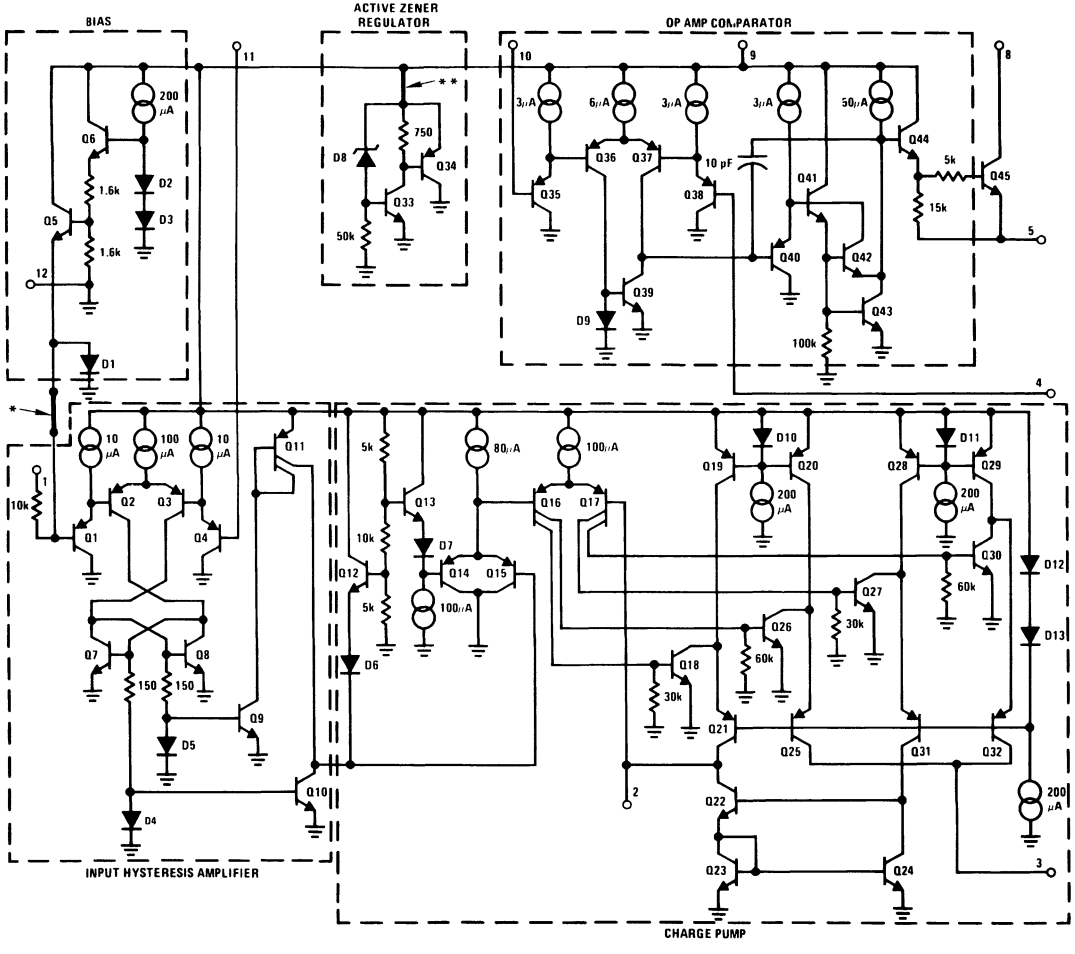
TL/H/7942–36

V_{OUT} is proportional to the higher of the two input wheel speeds.

"Select-Average" Circuit



TL/H/7942–37



TL/H/7942–38

*This connection made on LM2907-8 and LM2917-8 only.

**This connection made on LM2917 and LM2917-8 only.

National Semiconductor

LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

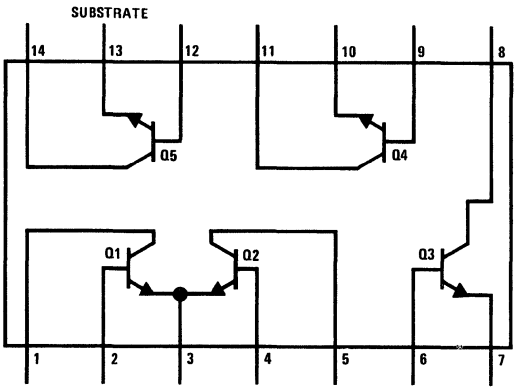
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) −55°C to +125°C

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7950–1

Top View

Order Number LM3045J, LM3046M, LM3086M, LM3046N or LM3086N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (T_A = 25°C)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM3045		LM3046/LM3086		Units
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
T_A > 55°C			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
T_A > 75°C	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	−55°C to +125°C		−40°C to +85°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +85°C		
Soldering Information					
Dual-In-Line Package Soldering (10 Sec.)	260°C		260°C		
Small Outline Package					
Vapor Phase (60 Seconds)			215°C		
Infrared (15 Seconds)			220°C		

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Conditions	Limits LM3045, LM3046			Limits LM3086			Units
		Min	Typ	Max	Min	Typ	Max	
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10 μA, I_E = 0	20	60		20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10 μA, I_{CI} = 0	20	60		20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E 10 μA, I_C = 0	5	7		5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0.002	40		0.002	100	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			0.5			5	μA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V, I_C = 10 mA		100			100		
	I_C = 1 mA	40	100		40	100		
	I_C = 10 μA		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{IO2}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.3	2				μA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1 mA		0.715			0.715		V
	I_E = 10 mA		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4}\rvert$, $\lvert V_{BE4} - V_{BE5}\rvert$, $\lvert V_{BE5} - V_{BE3}\rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		−1.9			−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		0.23			0.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		1.1					μV/°C

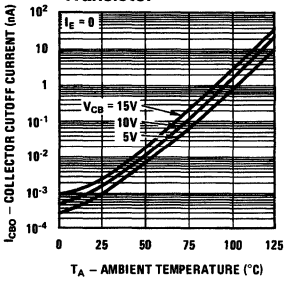
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

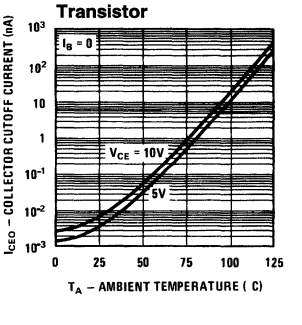
Parameter	Conditions	Min	Typ	Max	Units
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110 (LM3045, LM3046) (LM3086)		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3 + J 0.04		
Output Admittance (Y_{oe})			0.001 + j 0.03		
Reverse Transfer Admittance (Y_{re})			See Curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

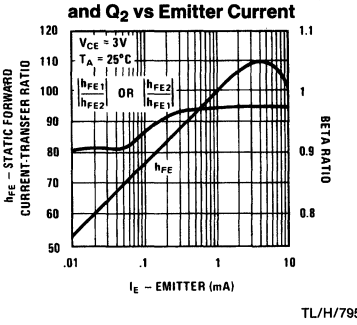
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor



Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current



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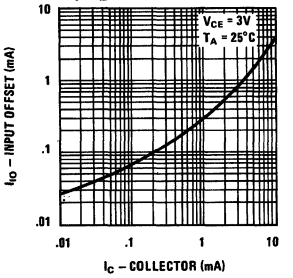
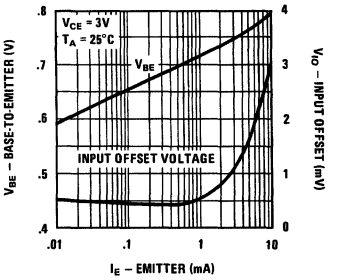
Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current



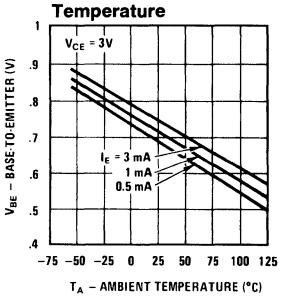
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



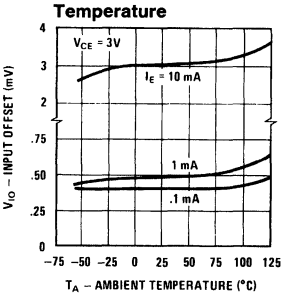
TL/H/7950–3

Typical Performance Characteristics (Continued)

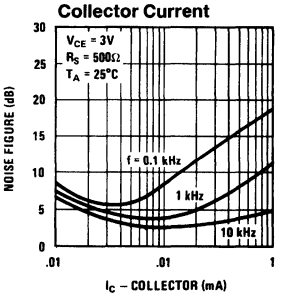
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

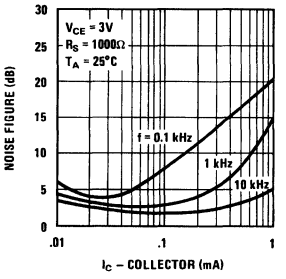


Typical Noise Figure vs Collector Current

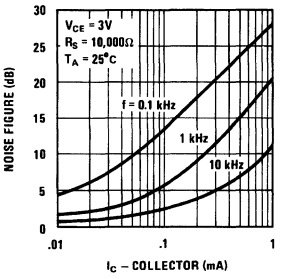


TL/H/7950–4

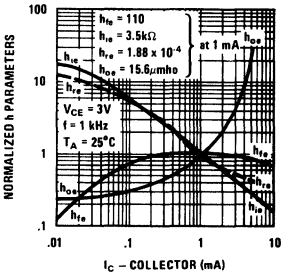
Typical Noise Figure vs Collector Current



Typical Noise Figure vs Collector Current

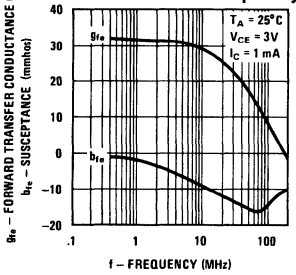


Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

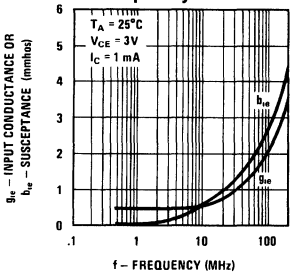


TL/H/7950–5

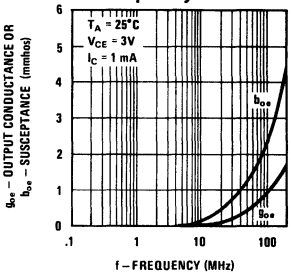
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency



Typical Output Admittance vs Frequency



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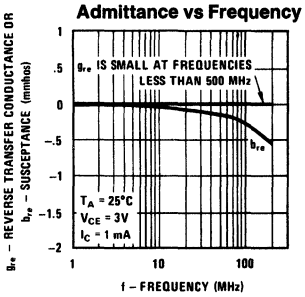
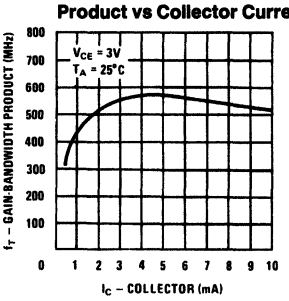
8

Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



TL/H/7950–7

National Semiconductor

LM3146 High Voltage Transistor Array

General Description

The LM3146 consists of five high voltage general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3146 is supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

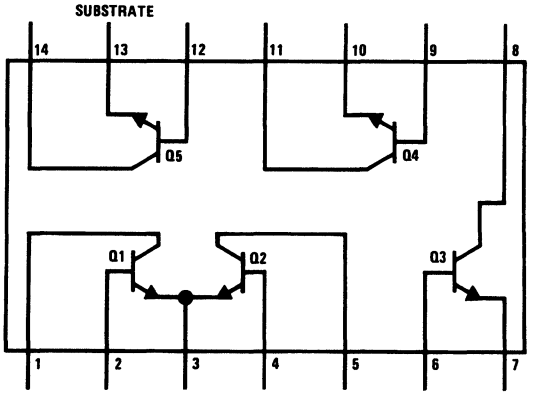
- High voltage matched pairs of transistors, V_{BE} matched ±5 mV, input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from dc to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from dc to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7959–1

Top View

Order Number LM3146M or LM3146N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM3146	Units
Power Dissipation: Each transistor		
T_A = 25°C to 55°C	300	mW
T_A > 55°C	Derate at 6.67	mW/°C
Power Dissipation: Total Package		
T_A = 25°C	500	mW
T_A > 25°C	Derate at 6.67	mW/°C
Collector to Emitter Voltage, V_{CEO}	30	V
Collector to Base Voltage, V_{CBO}	40	V
Collector to Substrate Voltage, V_{CIO} (Note 1)	40	V
Emitter to Base Voltage, V_{EBO} (Note 2)	5	V
Collector to Current, I_C	50	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics T_A = 25°C

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 10 μA, I_E = 0	40	72		V
$V_{(BR)CEO}$	Collector to Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	30	56		V
$V_{(BR)CIO}$	Collector to Substrate Breakdown Voltage	I_{CI} = 10 μA, I_B = 0, I_E = 0	40	72		V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage (Note 2)	I_C = 0, I_E = 10 μA	5	7		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 10V, I_E = 0		0.002	100	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10V, I_B = 0		(Note 3)	5	μA
h_{FE}	Static Forward Current Transfer Ratio (Static Beta)	I_C = 10 mA, V_{CE} = 5V I_C = 1 mA, V_{CE} = 5V I_C = 10 μA, V_{CE} = 5V	30	85 100 90		
$I_{B1}-I_{B2}$	Input Offset Current for Matched Pair Q1 and Q2	I_{C1} = I_{C2} = 1 mA, V_{CE} = 5V		0.3	2	μA
V_{BE}	Base to Emitter Voltage	I_C = 1 mA, V_{CE} = 3V	0.63	0.73	0.83	V
$V_{BE1}-V_{BE2}$	Magnitude of Input Offset Voltage for Differential Pair	V_{CE} = 5V, I_E = 1 mA		0.48	5	mV
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base to Emitter Voltage	V_{CE} = 5V, I_E = 1 mA		−1.9		mV/°C
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 10 mA, I_B = 1 mA		0.33		V
$\Delta V_{10}/\Delta T$	Temperature Coefficient of Input Offset Voltage	I_C = 1 mA, V_{CE} = 5V		1.1		μV/°C

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 5V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
f_T	Gain Bandwidth Product	V_{CE} = 5V, I_C = 3 mA	300	500		MHz
C_{EB}	Emitter to Base Capacitance	V_{EB} = 5V, I_E = 0		0.70		pF
C_{CB}	Collector to Base Capacitance	V_{CB} = 5V, I_C = 0		0.37		pF
C_{CI}	Collector to Substrate Capacitance	V_{CI} = 5V, I_C = 0		2.2		pF
Low Frequency, Small Signal Equivalent Circuit Characteristics						
h_{fe}	Forward Current Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		100		
h_{ie}	Short Circuit Input Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		3.5		kΩ
h_{oe}	Open Circuit Output Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		15.6		μmho
h_{re}	Open Circuit Reverse Voltage Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		1.8×10^{-4}		
Admittance Characteristics						
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.3 + j 0.04		mmho
Y_{oe}	Output Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		(Note 3)		mmho

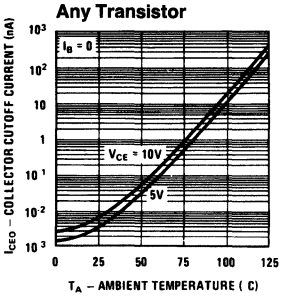
Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

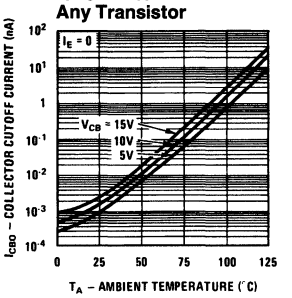
Note 3: See curve.

Typical Performance Characteristics

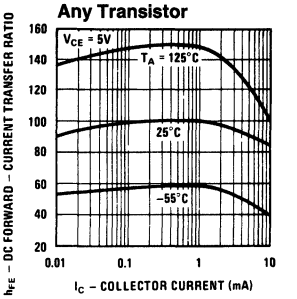
I_{CEO} vs T_A for Any Transistor



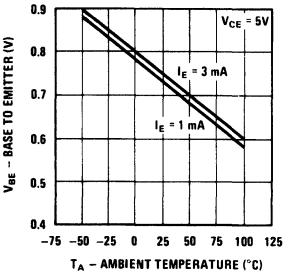
I_{CBO} vs T_A for Any Transistor



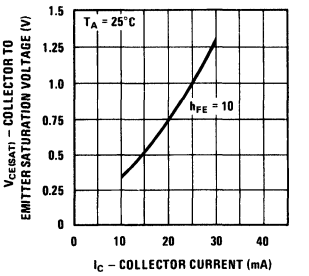
h_{FE} vs I_C for Any Transistor



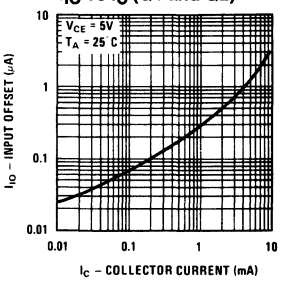
V_{BE} vs T_A for Any Transistor



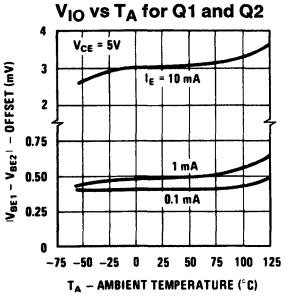
$V_{CE(SAT)}$ vs I_C for Any Transistor



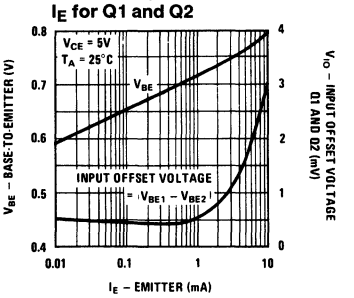
I_{IO} vs I_C (Q1 and Q2)



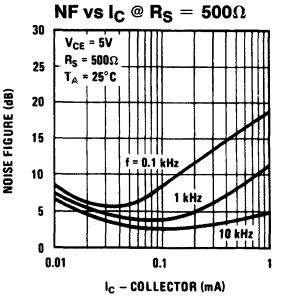
V_{IO} vs T_A for Q1 and Q2



V_{BE} and V_{IO} vs I_E for Q1 and Q2



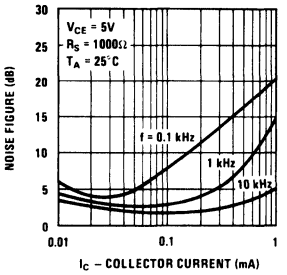
NF vs I_C @ $R_S = 500\Omega$



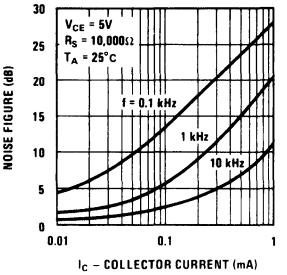
TL/H/7959–2

Typical Performance Characteristics (Continued)

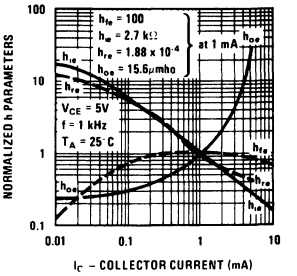
NF vs I_C @ R_S = 1 kΩ



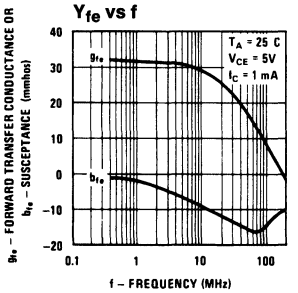
NF vs I_C = R_S = 10 kΩ



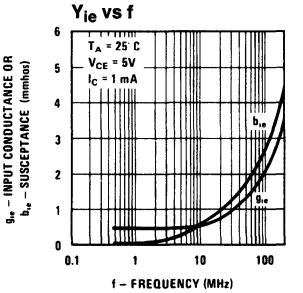
h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C



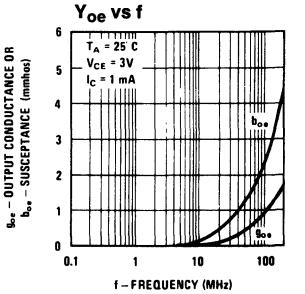
Y_{fe} vs f



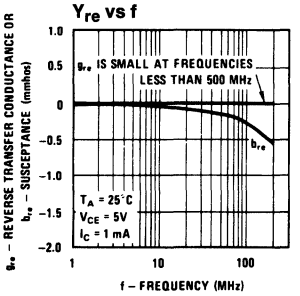
Y_{ie} vs f



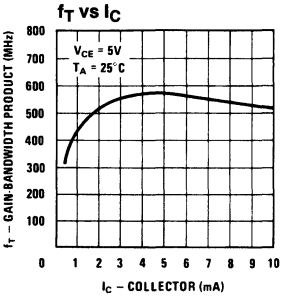
Y_{oe} vs f



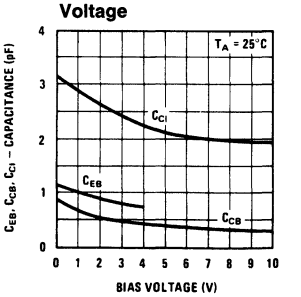
Y_{re} vs f



f_T vs I_C



C_{EB}, C_{CB}, C_{CI} vs Bias Voltage



TL/H/7959–3

8

National Semiconductor

PRELIMINARY

LMC555 CMOS Timer

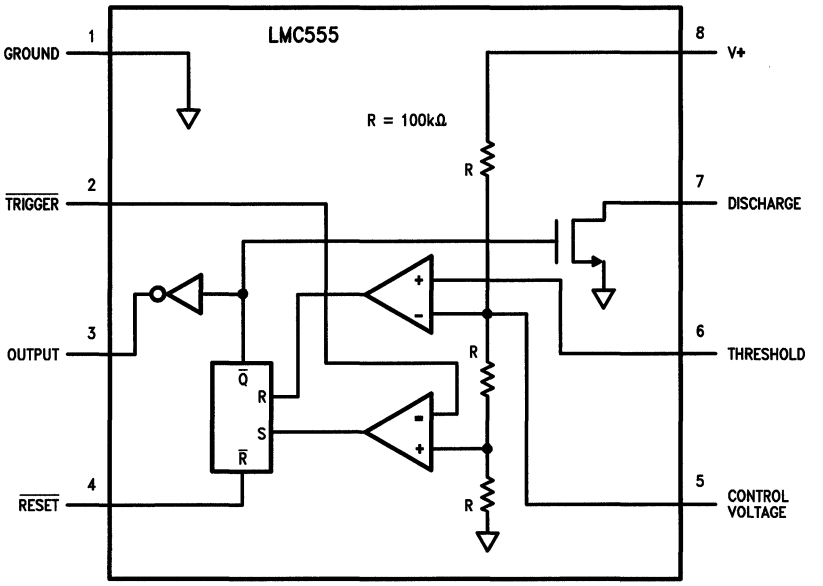
General Description

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. It offers the same capability of generating accurate time delays and frequencies but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers

Block and Connection Diagrams



TL/H/8669–1

(Pinouts for Molded and Metal Can Packages are identical)

Order Number LMC555CH, LMC555CM or LMC555CN
See NS Package Number H08C, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V8	15V
Input Voltages, V2, V4, V5, V6	−0.3V to V_S + 0.3V
Output Voltages, V3, V7	15V
Output Current I3, I7	100 mA
Operating Temperature Range (Note 1)	−40°C to +85°C*
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted

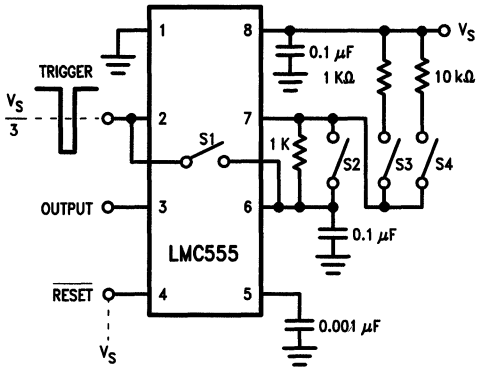
Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
I8	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	μA
V5	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V7	Discharge Saturation Voltage	V_S = 1.5V, I_7 = 1 mA V_S = 5V, I_7 = 10 mA		75 150	150 300	mV
$V3_L$	Output Voltage (Low)	V_S = 1.5V, I_3 = 1 mA V_S = 5V, I_3 = 8 mA V_S = 12V, I_3 = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
$V3_H$	Output Voltage (High)	V_S = 1.5V, I_3 = −0.25 mA V_S = 5V, I_3 = −2 mA V_S = 12V, I_3 = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V2	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I2	Trigger Current	V_S = 5V		10		pA
V4	Reset Voltage	V_S = 1.5V (Note 2) V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I4	Reset Current	V_S = 5V		10		pA
I6	Threshold Current	V_S = 5V		10		pA
I7	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
Δt/ΔVs	Timing Shift with Supply	V_S = 5V ±1V		0.3		%/V
Δt/ΔT	Timing Shift with Temperature	V_S = 5V −40°C ≤ T ≤ +85°C		75		ppm/°C
f_A	Astable Frequency	SW 1, 3 Closed V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

* Refer to RETSC555X drawing for specifications of military LMC555H version.

Note 1: For operation at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 111°C/W for the LMC555CN, 167°C/W for the LMC555CH, and 169°C/W for the LMC555CM. Maximum allowable dissipation at 25°C is 1126 mW for the LMC555CN, 755 mW for the LMC555CH, and 740 mW for the LMC555CM.

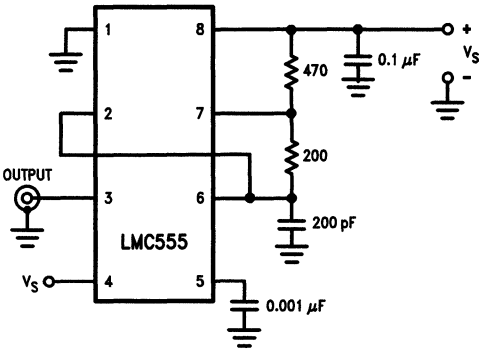
Note 2: If the $\overline{\text{RESET}}$ pin is to be used at temperatures of −20°C and below V_S is required to be 2.0V or greater.

Test Circuit



TL/H/8669-2

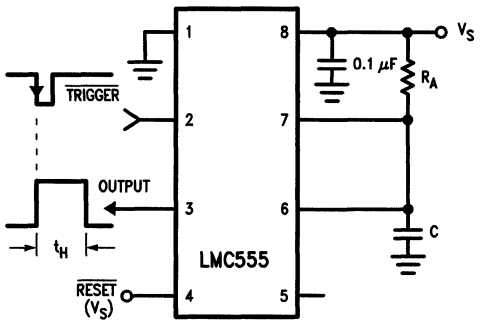
Maximum Frequency Test Circuit



TL/H/8669-3

Typical Applications

Monostable (One-Shot)



TL/H/8669-4

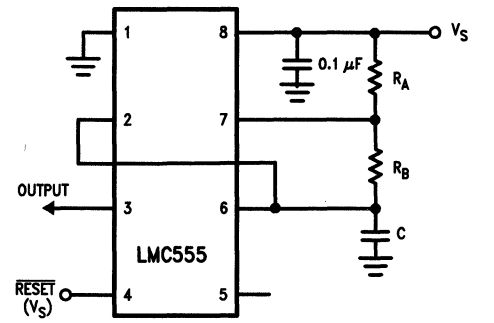
t_H = 1.1 R_AC (Gives time that output is high following trigger)

$\overline{\text{RESET}}$ overrides $\overline{\text{TRIGGER}}$, which can override THRESHOLD. Therefore, the trigger pulse must be shorter than the desired t_H.

The minimum trigger pulse width is 20 ns.

The minimum reset pulse width is 400 ns.

Variable Duty Cycle Oscillator

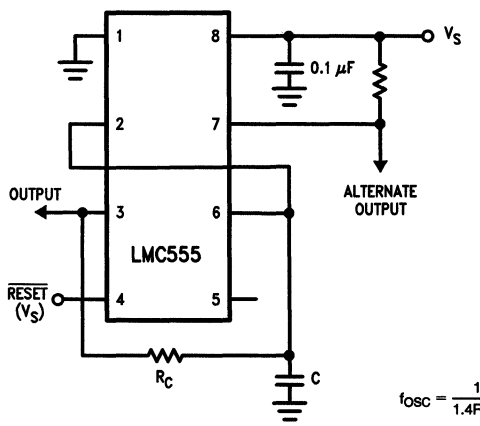


TL/H/8669-5

$$f_{OSC.} = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty Cycle} = \frac{R_B}{R_A + 2R_B}$$ (Gives fraction of total period that output is low)

50% Duty Cycle Oscillator



$$f_{OSC} = \frac{1}{1.4R_CC}$$

TL/H/8669-6

National Semiconductor

LMC567 Low Power Tone Decoder

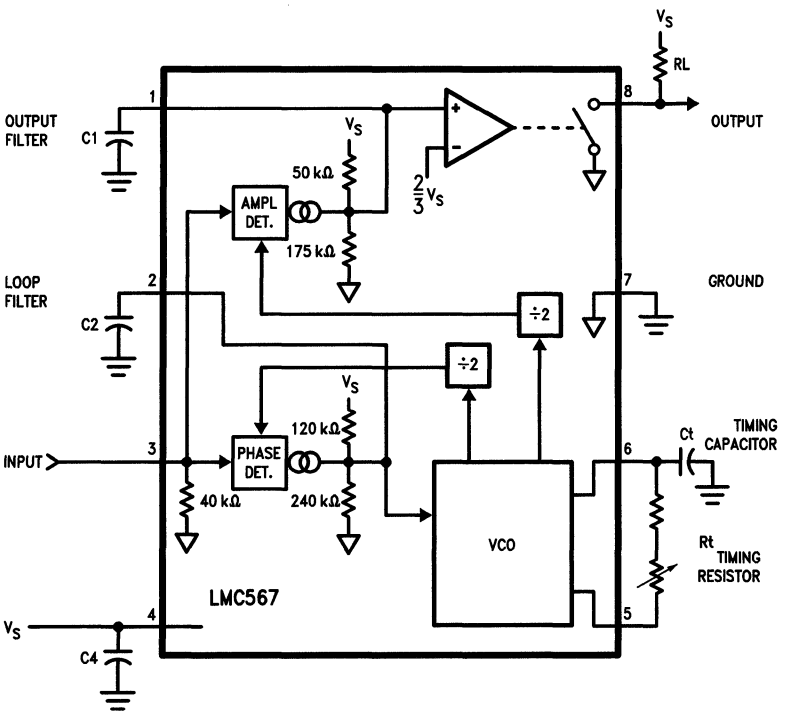
General Description

The LMC567 is a low power general purpose LMCMOS™ tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

Features

- Functionally similar to LM567
- 2V to 9V supply voltage range
- Low supply current drain
- No increase in current with output activated
- Operates to 500 kHz input frequency
- High oscillator stability
- Ground-referenced input
- Hysteresis added to amplitude comparator
- Out-of-band signals and noise rejected
- 20 mA output current capability

Block Diagram (with External Components)



TL/H/8670–1

Order Number LMC567CM or LMC567CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	$2\ V_{p-p}$
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	Vs to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

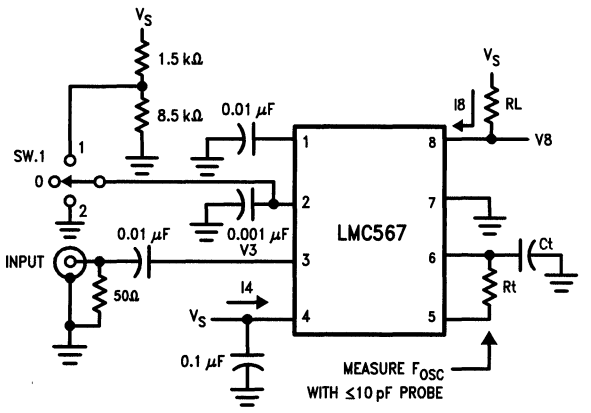
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, $T_A = 25°C$, $V_s = 5V$, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	$V_s = 2V$		0.3		mAdc
			$V_s = 5V$		0.5	0.8	
			$V_s = 9V$		0.8	1.3	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency, $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	$V_s = 2V$		98		kHz
			$V_s = 5V$	92	103	113	
			$V_s = 9V$		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\ f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level Until Pin 8 Goes Low.	$V_s = 2V$	11	20	27	mVrms
			$V_s = 5V$	17	30	45	
			$V_s = 9V$		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level Until Pin 8 goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; $\text{L.D.B.W} = \frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	$V_s = 2V$	7	11	15	%
			$V_s = 5V$	11	14	17	
			$V_s = 9V$		15		
ΔBW	Bandwidth Skew	$\text{Skew} = \left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\ F_{osc}\|_{P0}} - 1\right) \times 100$			0	±1.0	%
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz
V_{in}	Input Threshold at f_{max}	Set Input Frequency Equal to f_{max} measured Above, Increase Input Level Until Pin 8 goes Low.			35		mVrms

Test Circuit

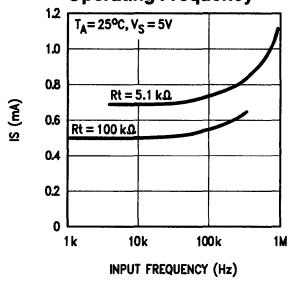


TL/H/8670–2

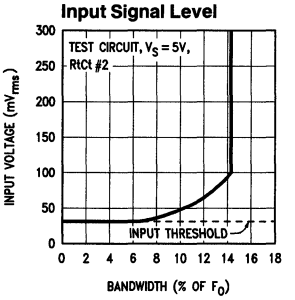
RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

Typical Performance Characteristics

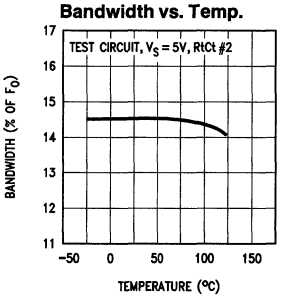
Supply Current vs. Operating Frequency



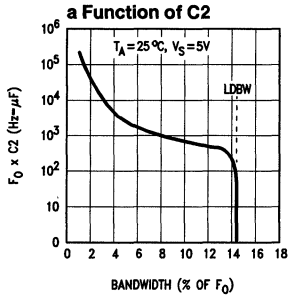
Bandwidth vs. Input Signal Level



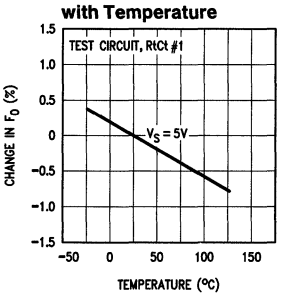
Largest Detection Bandwidth vs. Temp.



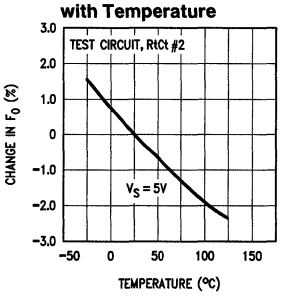
Bandwidth as a Function of C2



Frequency Drift with Temperature



Frequency Drift with Temperature



TL/H/8670–3

Applications Information (refer to Block Diagram)

GENERAL

The LMC567 low power tone decoder can be operated at supply voltages of 2V to 9V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (See OSCILLATOR TIMING COMPONENTS).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor Rt and timing capacitor Ct connected to pins 5 and 6 of the IC. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct} Hz$$

Since this will cause an input tone of half F_{osc} to be decoded,

$$F_{input} \cong \frac{1}{2.8\ Rt\ Ct} Hz$$

This equation is accurate at low frequencies; however, above 50 kHz (F_{osc} = 100 kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of Rt and Ct will be a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced due to Rt being switched to V_S every half cycle to charge Ct:

$$I_S \text{ due to } Rt = V_S/(4Rt)$$

Thus the supply current can be minimized by keeping Rt as large as possible (see supply current vs. operating frequency curves). However, the desired frequency will dictate an RtCt product such that increasing Rt will require a smaller Ct. Below Ct = 100 pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum Ct.

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close as possible to pin 4.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals which are already centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual d.c. isolation.

LOOP FILTER

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80 kΩ pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will begin to become narrower than the LDBW (see Bandwidth as a Function of C2 curve). However, the maximum hold-in range will always equal the LDBW.

OUTPUT FILTER

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches 2/3 V_S the output is activated (see OUTPUT PIN).

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

OUTPUT PIN

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The on resistance of the switch is inversely proportional to supply; thus the 'sat' voltage for a given output current will increase at lower supplies.

National Semiconductor

LMC568 Low Power Phase-Locked Loop

General Description

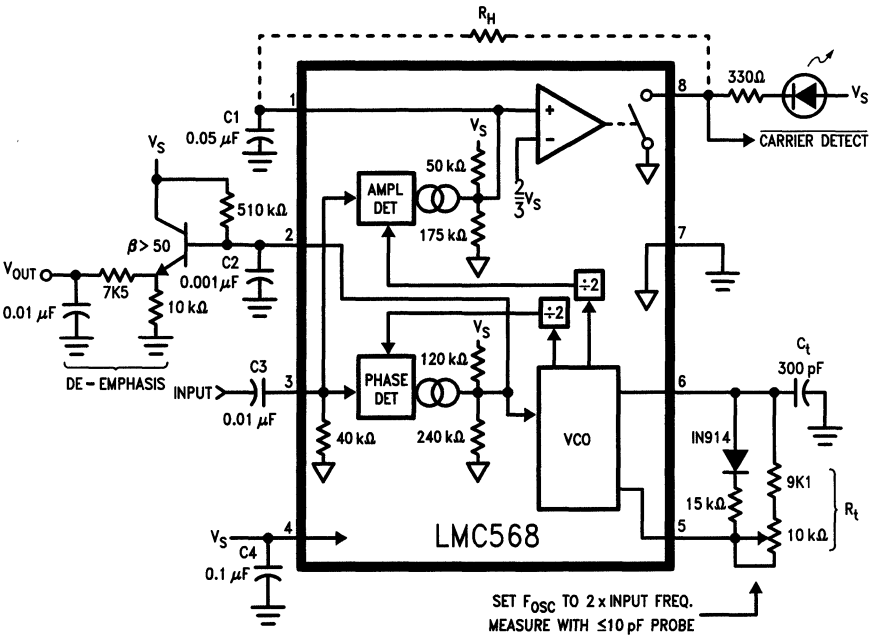
The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMCMOS™ technology is employed for high performance with low power consumption.

The VCO has a linearized control range of ±30% to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Features

- Demodulates ±15% deviation FM/FSK signals
- Carrier Detect Output with hysteresis
- Operation to 500 kHz input frequency
- Low THD—0.5% typ. for ±10% deviation
- 2V to 9V supply voltage range
- Low supply current drain

Typical Application (100 kHz input frequency, refer to notes pg. 3)



TL/H/9135–1

Order Number LMC568CM or LMC568CN
See NS Package Number M08A or N08E

8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage, Pin 3	2 V_{p-p}
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	V_S to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

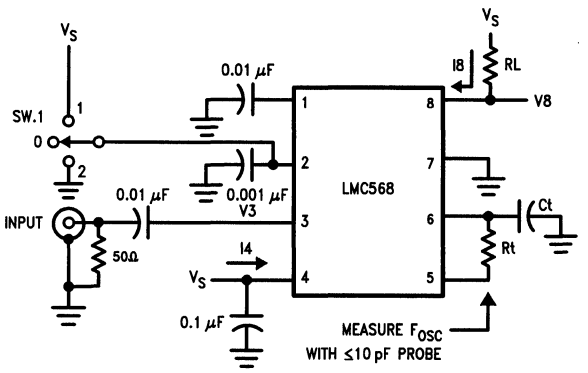
See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V_S = 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_S = 2V		0.35		mAdc
			V_S = 5V		0.75	1.5	
			V_S = 9V		1.2	2.4	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_S = 2V		98		kHz
			V_S = 5V	90	103	115	
			V_S = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level until Pin 8 Goes Low.	V_S = 2V	8	16	25	mVrms
			V_S = 5V	15	26	42	
			V_S = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W. $= \frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	V_S = 2V		30		%
			V_S = 5V	40	55		
			V_S = 9V		60		
ΔBW	Bandwidth Skew	Skew $= \left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\, F_{osc}\|_{P0}} - 1\right) \times 100$			1	±5	%
V_{out}	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F_{mod} = 400 Hz, ±10 kHz Dev.	V_S = 2V		170		mVrms
			V_S = 5V		270		
			V_S = 9V		400		
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V_{out} Distortion.			0.5		%
$\frac{S+N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V_n $(S + N)/N = 20 \log (V_{out}/V_n)$.			65		dB
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz

Test Circuit



TL/H/9135–3

RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

Notes to Typical Application

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for F_{osc} = 200 kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase V_{out} by approximately 2 dB with THD = 2% typical. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

To allow for I.C. and component value tolerences, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 kΩ, requiring the use of an external buffer transistor to drive nominal loads.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

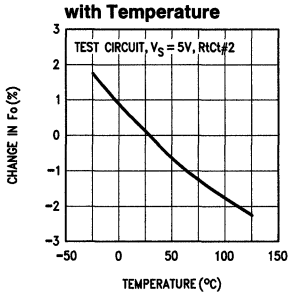
CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

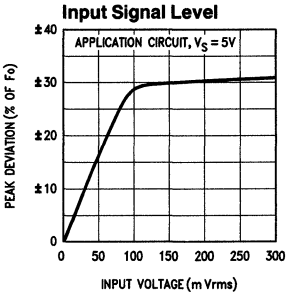
Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor R_H increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for R_H is 330 kΩ.

LMC568 Typical Performance Characteristics

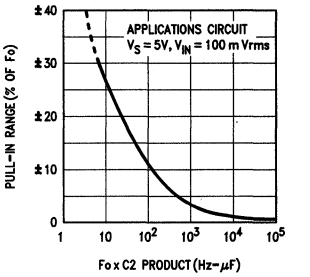
Frequency Drift with Temperature



Peak Deviation vs Input Signal Level



Pull-In Range as a Function of C2



TL/H/9135–2

National Semiconductor

LP395 Ultra Reliable Power Transistor

General Description

The LP395 is a fast monolithic transistor with complete overload protection. This very high gain transistor has included on the chip, current limiting, power limiting, and thermal overload protection, making it difficult to destroy from almost any type of overload. Available in an epoxy TO-92 transistor package this device is guaranteed to deliver 100 mA.

Thermal limiting at the chip level, a feature not available in discrete designs, provides comprehensive protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive die temperature.

The LP395 offers a significant increase in reliability while simplifying protection circuitry. It is especially attractive as a small incandescent lamp or solenoid driver because of its low drive requirements and blowout-proof design.

The LP395 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LP395 as with any transistor. When the device is used as an emitter follower with a low source impedance, it is necessary to insert a 4.7 kΩ resistor in series with the base lead to prevent possible emitter follower oscillations. Also since it has good high frequency response, supply bypassing is recommended.

Areas where the LP395 differs from a standard NPN transistor are in saturation voltage, leakage (quiescent) current and in base current. Since the internal protection circuitry requires voltage and current to function, the minimum voltage across the device in the on condition (saturated) is typically 1.6 Volts, while in the off condition the quiescent (leakage) current is typically 200 μA. Base current in this device flows out of the base lead, rather than into the base as is the case with conventional NPN transistors. Also the base can be driven positive up to 36 Volts without damage, but will draw current if driven negative more than 0.6 Volts. Additionally, if the base lead is left open, the LP395 will turn on.

The LP395 is a low-power version of the 1-Amp LM195/LM295/LM395 Ultra Reliable Power Transistor.

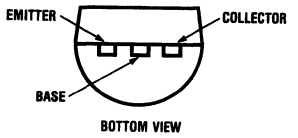
The LP395 is rated for operation over a −40°C to +125°C range.

Features

- Internal thermal limiting
- Internal current and power limiting
- Guaranteed 100 mA output current
- 0.5 μA typical base current
- Directly interfaces with TTL or CMOS
- +36 Volts on base causes no damage
- 2 μs switching time

Connection Diagram

TO-92 Package

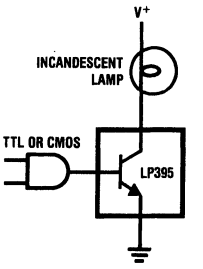


TL/H/5525–1

Order Number LP395Z
See NS Package Z03A

Typical Applications

Fully Protected Lamp Driver



TL/H/5525–3

Absolute Maximum Ratings

Collector to Emitter Voltage	36V	Collector Current Limit	Internally Limited
Collector to Base Voltage	36V	Power Dissipation	Internally Limited
Base to Emitter Voltage (Forward)	36V	Operating Temperature Range	−40°C to +125°C
Base to Emitter Voltage (Reverse)	10V	Storage Temperature Range	−65°C to +150°C
Base to Emitter Current (Reverse)	20 mA	Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
V_{CE}	Collector to Emitter Operating Voltage	0.5 mA ≤ I_C ≤ 100 mA		36	**36** (Note 1)	V(Max)
I_{CL}	Collector Current Limit (Note 4)	V_{BE} = 2V, V_{CE} = 36V V_{BE} = 2V, V_{CE} = 15V V_{BE} = 2V, 2V ≤ V_{CE} ≤ 6V	45 90 130	25 60 100	**20** **50** **100**	mA(Min) mA(Min) mA(Min)
I_B	Base Current	0 ≤ I_C ≤ 100 mA	−0.3	−2.0	**−2.5**	μA(Max)
I_Q	Quiescent Current	V_{BE} = 0V, 0 ≤ V_{CE} ≤ 36V	0.24	0.50	**0.60**	mA(Max)
$V_{CE(SAT)}$	Saturation Voltage	V_{BE} = 2V, I_C = 100 mA	1.82	2.00	**2.10**	V(Max)
BV_{BE}	Base to Emitter Breakdown Voltage (Note 4)	0 ≤ V_{CE} ≤ 36V, I_B = 2 μA		36	**36**	V(Min)
V_{BE}	Base to Emitter Voltage (Note 5)	I_C = 5 mA	0.69	0.79	**0.90**	V(Max)
		I_C = 100 mA (Note 4)	1.02		**1.40**	V (Max)
t_S	Switching Time	V_{CE} = 20V, R_L = 200Ω V_{BE} = 0V, +2V, 0V	2			μs
θ_{JA}	Thermal Resistance Junction to Ambient	0.4″ leads soldered to printed circuit board	150		**180**	°C/W (Max)
		0.125″ leads soldered to printed circuit board	130		**160**	°C/W (Max)

Note 1: Parameters identified with **boldface type** apply at temp. extremes. All other numbers, unless noted apply at +25°C.

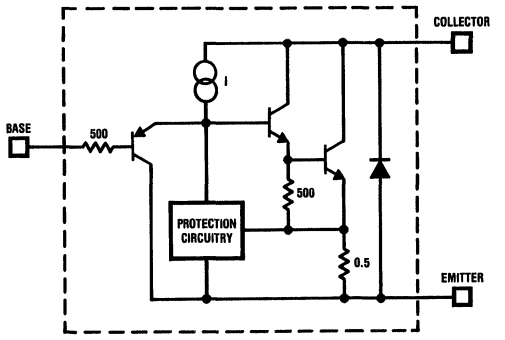
Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: These numbers apply for pulse testing with a low duty cycle.

Note 5: Base positive with respect to emitter.

Simplified Circuit



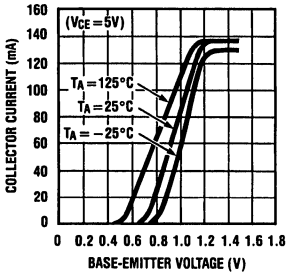
TL/H/5525–5

Applications Information

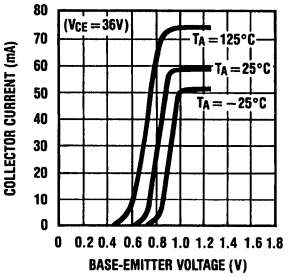
One failure mode incandescent lamps may experience is one in which the filament resistance drops to a very low value before it actually blows out. This is especially rough on most solid-state lamp drivers and in most cases a lamp failure of this type will also cause the lamp driver to fail. Because of its high gain and blowout-proof design, the LP395 is an ideal candidate for reliably driving small incandescent lamps. Additionally, the current limiting characteristics of the LP395 are advantageous as it serves to limit the cold filament inrush current, thus increasing lamp life.

Typical Performance Characteristics

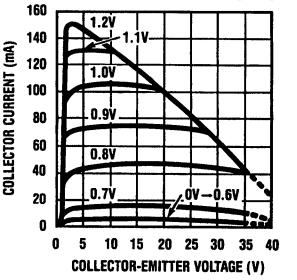
5 Volt Transfer Function



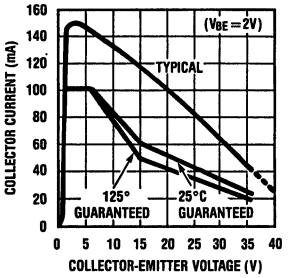
36 Volt Transfer Function



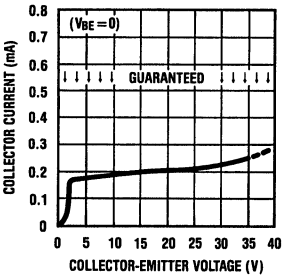
Collector Characteristics



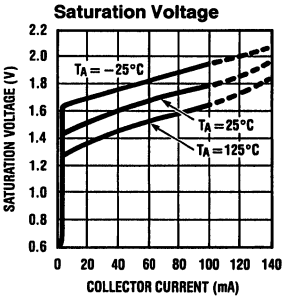
Available Collector Current



Quiescent Collector Current

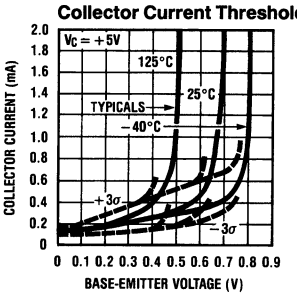


Saturation Voltage



TL/H/5525–4

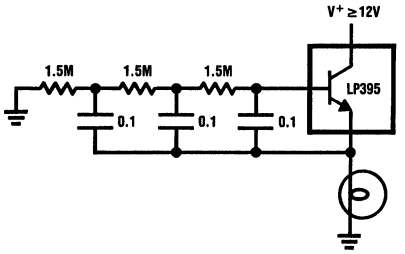
Collector Current Threshold



TL/H/5525–9

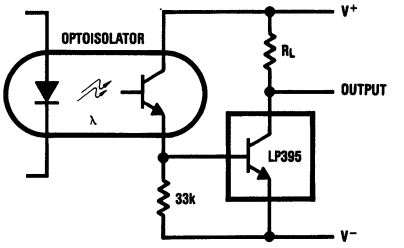
Typical Applications (Continued)

Lamp Flasher (Short Circuit Proof)



TL/H/5525–6

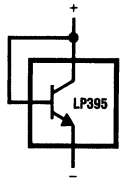
Optically Isolated Switch



TL/H/5525–7

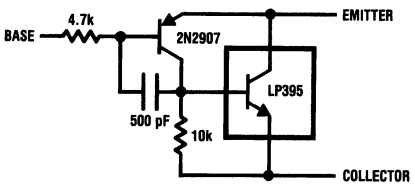
Typical Applications (Continued)

Two Terminal Current Limiter



TL/H/5525–8

Composite PNP



TL/H/5525–2

Section 9

Surface Mount

Section 9 Contents

National Semiconductor

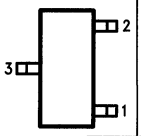
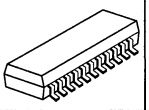
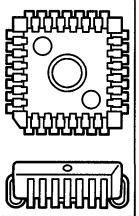
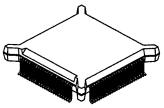
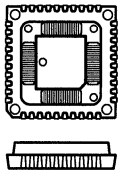
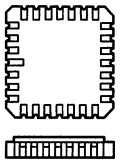
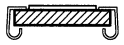
Surface Mount

SURFACE MOUNT PACKAGING AT NATIONAL

To meet the growing demand for smaller packaging, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK®) will have a lead center spacing of only 12–20 mils.

TABLE I. Surface Mount Packages from National

Package Type	Small Outline Transistor (SOT)	Small Outline IC (SOIC)	Plastic Chip Carrier (PCC)	Plastic Quad Flat Pack (PQFP)	TAPEPAK® (TP)	Leadless Chip Carrier (LCC) (LDCC)	Leaded Chip Carrier
							
Package Material	Plastic	Plastic	Plastic	Plastic	Plastic	Ceramic	Ceramic
Lead Bend	Gull Wing	Gull Wing	J-Bend	Gull Wing	Gull Wing	—	Gull Wing
Lead Center Spacing	50 Mils	50 Mils	50 Mils	25 Mils	20, 15, 12 Mils	50 Mils	50 Mils
Tape & Reel Option	Yes	Yes	Yes	tbd	tbd	No	No
Lead Counts	SOT-23 High Profile SOT-23 Low Profile	SO-8(*) SO-14(*) SO-14 Wide(*) SO-16(*) SO-16 Wide(*) SO-20(*) SO-24(*) SO-28(*)	PCC-20(*) PCC-28(*) PCC-44(*) PCC-68 PCC-84 PCC-124	PQFP-84 PQFP-100 PQFP-132 PQFP-196(*) PQFP-244	TP-40 (*) TP-68 TP-84 TP-132 TP-172 TP-220 TP-284 TP-360	LCC-18 LCC-20(*) LCC-28 LCC-32 LCC-44 (*) LCC-48 LCC-52 LCC-68 LCC-84 LCC-124	LDCC-44 LDCC-68 LDCC-84 LDCC-124

*In production (or planned) for linear products.

LINEAR PRODUCTS IN SURFACE MOUNT

Linear functions available in surface mount include:

- Op amps
- Comparators
- Regulators
- References
- Data conversion
- Industrial
- Consumer
- Automotive

A representative list of linear part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National has other products and is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for linear products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature (check the datasheet for the rare exception). Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 70°C and an industrial temperature range device will only be specified for a max ambient temperature of 85°C). See AN-336, "Understanding Integrated Circuit Package Power Capabilities", (reprinted in the appendix of each linear databook volume) for more information.

TABLE II: Surface Mount Package Thermal Resistance Range*

Package	Thermal Resistance** (θ_{jA}, °C/W)
SO-8	120–175
SO-14	100–140
SO-14 Wide	70–110
SO-16	90–130
SO-16 Wide	70–100
SO-20	60–90
SO-24	55–85
SO-28	TBD
PCC-20	70–100
PCC-28	60–90
PCC-44	40–60

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual θ_{jA} value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. This factor must be taken into account for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

TABLE III. Linear Surface Mount Selected Device Listing

Amplifiers and Comparators

Part Number	Part Number
LF451CM	LMC6022IM
LF453CM	LMC6024IM
LM10CWM	LMC6032IM
LM10CLWM	LMC6034IM
LM318M	LMC6041IM
LM3080M	LMC6042IM
LM4250M	LMC6044IM
LM611CM	LMC6084IM
LM612IM	LMC6064IM
LM613CWM	LMC6061IM
LM614CWM	LMC6081IM
LM615IWM	LMC6062IM
LM6181IM	LMC6082IM
LM6218WM	LMC6484IM
LM6321M	LMC6482IM
LM6361M	LPC660IM
LM6362M	LPC661IM
LM6364M	LPC662IM
LM6365M	
LMC660CM	
LMC662CM	

Peripheral Drivers

Part Number	Part Number
DS2001CM	DS2004TM
DS2001TM	DS3680M
DS2002CM	DS75451M
DS2002TM	DS75452M
DS2003CM	DS75453M
DS2003TM	DS75454M
DS2004CM	

Regulators and References

Part Number	Part Number
LM317LM	LM2577M—12
LM337LM	LM2577M—15
LM431ACM	LM2577M—ADJ
LM723CM	LM2578AM
LM2574M—3.3	LM2931AM—5.0
LM2574M—5.0	LM2931M—5.0
LM2574M—12	LM2931CM
LM2574M—15	LM2936M—5.0
LM2574M—ADJ	LM3524DM
LM2574HVM—3.3	LM3578AM
LM2574HVM—5.0	LM78L05ACM
LM2574HVM—12	LM78L12ACM
LM2574HVM—15	LM78L15ACM
LM2574HVM—ADJ	LM79L05ACM
LM2575M—5.0	LM79L12ACM
LM2575M—12	LM79L15ACM
LM2575M—15	LP2951ACM
LM2575M—ADJ	LP2951CM
LM2575HVM—5.0	LP2952AIM
LM2575HVM—12	LP2952IM
LM2575HVM—15	LP2953AIM
LM2575HVM—ADJ	LP2953IM

Data Acquisition Products

Part Number	Part Number
ADC08061/2/4/8	DAC0854
ADC08161/4/8	LM12454/8
ADC08031/2/4/8	LM34
ADC08131/4/8	LM35
ADC08231/4/8	LM4040
ADC0851/58	LM4041
ADC10061/2/4	LM4431
ADC10154/8	LMF100
ADC1034/8	LMF380
ADC10461/2/4	LMF40
ADC1061	LMF60
ADC10662/4	LMF90
ADC12030/2/4/8	

Industrial Functions

Part Number	Part Number
AH5012CM	LM13600M
LF13331M	LM13700M
LF13509M	LMC555CM
LF13333M	LM567CM
LM555CM	MF4CWM-50
LM556CM	MF4CWM-100
LM567CM	MF6CWM-50
LM1496M	MF10CCWM
LM2917M	MF6CWM-100
LM3046M	MF5CWM
LM3086M	LMC568CM
LM3146M	LMC567CM

Commercial and Automotive

Part Number	Part Number
LM386M-1	LM1851M
LM831M	LM1865M
LM832M	LM1877M
LM833M	LM1894M
LM837M	LM1882CM
LMC835V	LM1964V
LM1201M	LMC1982CIV
LM1204V	LMC1983CIV
	LM3361AM
	LM1881M
	LM3914V

A FINAL WORD

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

Ordering and Shipping Information

When you order a surface mount semiconductor, it will be in one of the several available surface mount package types. Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

When ordering bulk S.O.—specify "M".

When ordering S.O. Tape & Reel—specify "MX".

Package	Package Designator	Max/Rail	Per Reel*
SO-8	M	100	2500
SO-14	M	50	2500
SO-14 Wide	WM	50	1000
SO-16	M	50	2500
SO-16 Wide	WM	50	1000
SO-20	M	40	1000
SO-24	M	30	1000
SO-28	M	26	1000
PCL-20	V	50	1000
PCL-28	V	40	1000
PCL-44	V	25	500
PQFP-196	VF	TBD	—
TP-40	TP	100	TBD
LCC-20	E	50	—
LCC-44	E	25	—

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

Example: You order 5,000 LM324MXICs shipped in Tape-and-Reel.

- Case 1: All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs
- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 LM324MXICs with date code A

    Pack #2 has 500 LM324MXICs with date code A

    Pack #3 has 2,000 LM324MXICs with date code B

Short-Form Procurement Specification

TAPE FORMAT

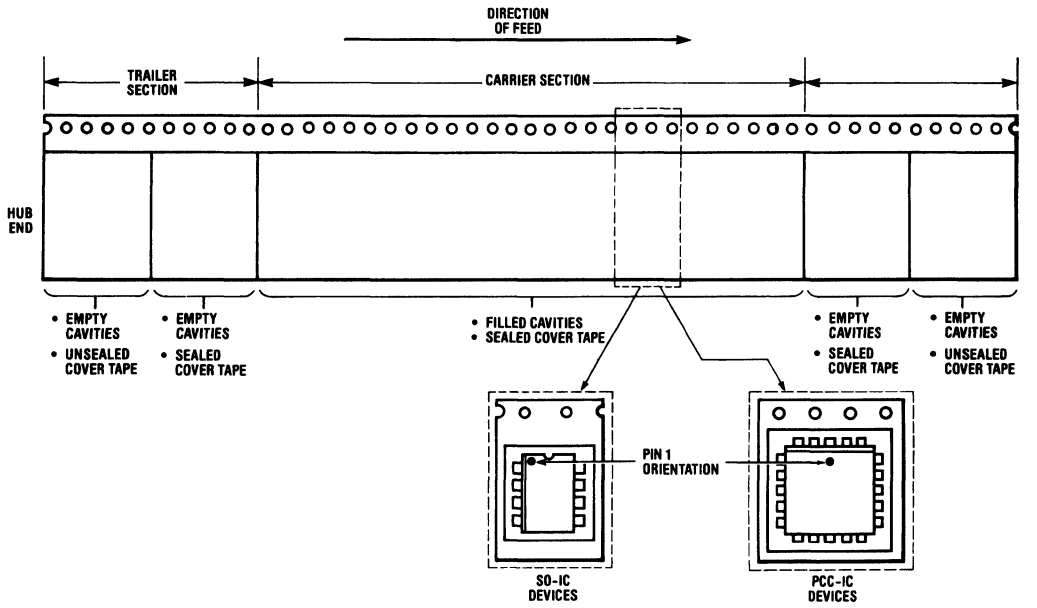
→ Direction of Feed

	Trailer (Hub End)*		Carrier*	Leader (Start End)*	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
Small Outline IC					
SO-8 (Narrow)	2	2	2500	5	5
SO-14 (Narrow)	2	2	2500	5	5
SO-14 (Wide)	2	2	1000	5	5
SO-16 (Narrow)	2	2	2500	5	5
SO-16 (Wide)	2	2	1000	5	5
SO-20 (Wide)	2	2	1000	5	5
SO-24 (Wide)	2	2	1000	5	5
SO-28 (Wide)	0	25	1000	42	0
Plastic Chip Carrier IC					
PCC-20	2	2	1000	5	5
PCC-28	2	2	750	5	5
PCC-44	2	2	500	5	5

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

Short-Form Procurement Specification (Continued)

DEVICE ORIENTATION



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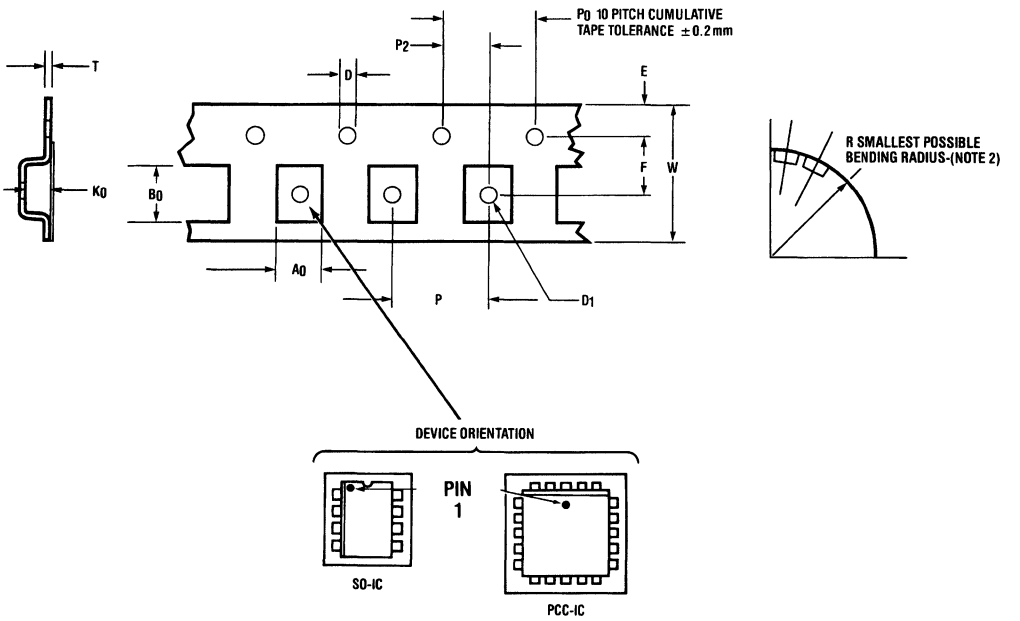
MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ohms/Sq)
- Cover Tape: Polyester
  - (1) Conductive cover available
- Reel:
  - (1) Solid 80 pt fibreboard (standard)
  - (2) Conductive fibreboard available
  - (3) Conductive plastic (PVC) available

TAPE DIMENSIONS (24 Millimeter Tape or Less)



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Short-Form Procurement Specification (Continued)

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
Small Outline IC													
SO-8 (Narrow)	12±.30	8.0±.10	5.5±.05	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.4±.10	5.2±.10	2.1±.10	1.55±.05	30
SO-14 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	9.0±.10	2.1±.10	1.55±.05	40
SO-14 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	9.5±.10	3.0±.10	1.55±.05	40
SO-16 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	10.3±.10	2.1±.10	1.55±.05	40
SO-16 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	10.76±.10	3.0±.10	1.55±.05	40
SO-20 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	13.3±.10	3.0±.10	2.05±.05	50
SO-24 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	15.85±.10	3.0±.10	2.05±.05	50
Plastic Chip Carrier IC													
PCC-20	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	9.3±.10	9.3±.10	4.9±.10	1.55±.05	40
PCC-28	24±.30	16.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	13.0±.10	13.0±.10	4.9±.10	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

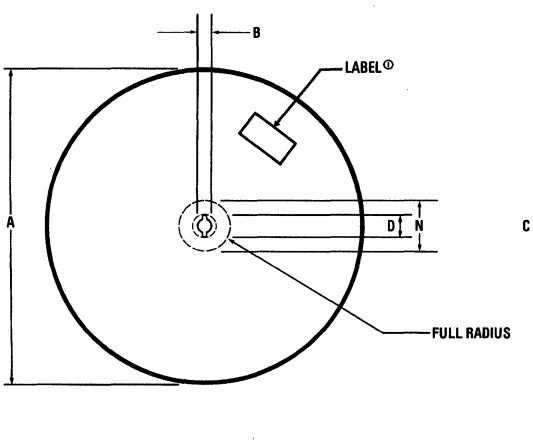
Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ohms/Sq).

Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

REEL DIMENSIONS



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START™* Surface Mount Tape and Reel

Short-Form Procurement Specifications (Continued)

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.488^{+.078}_{-.000}$ 12.4^{+2}_{-0}	.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PCC-20	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.646^{+.078}_{-.000}$ 16.4^{+2}_{-0}	.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PCC-28	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.960^{+.078}_{-.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PCC-44	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$1.276^{+.078}_{-.000}$ 32.4^{+2}_{-0}	1.512 38.4

Units: Inches / Millimeters

Material: Paperboard (Non-Flaking)

LABEL

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

FIELD

Lot Number

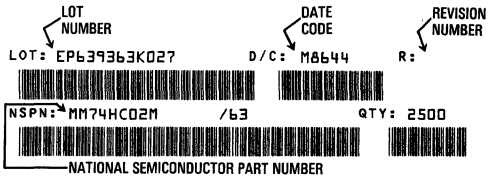
Date Code

Revision Level

National Part No. I.D.

Qty.

EXAMPLE



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Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

National Semiconductor will also offer additional labels containing information per your specific specification.

Wave Soldering of Surface Mount Components

ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.
b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.
   1. Components on the same side of PW Board.
      Lead insert standard DIPS onto PW Board Wave solder (conventional)
      Wash and lead trim
      Dispense solder paste on SMD pads
      Pick and place SMDs onto PW Board
      Bake
      Vapor phase/IR reflow
      Clean
   2. Components on opposite side of PW Board.
      Lead insert standard DIPs onto PW Board
      Wave Solder (conventional)
      Clean and lead trim
      Invert PW Board
      Dispense solder paste on SMD pads
      Dispense drop of adhesive on SMD sites (optional for smaller components)
      Pick and place SMDs onto board
      Bake/Cure
      Invert board to rest on raised fixture
      Vapor/IR reflow soldering
      Clean

B) Vapor/IR reflow solder then Wave Solder.
   1. Components on the same side of PW Board.
      Solder paste screened on SMD side of Printed Wire Board
      Pick and place SMDs
      Bake
      Vapor/IR reflow
      Lead insert on same side as SMDs
      Wave solder
      Clean and trim underside of PCB

C) Vapor/IR reflow only.
   1. Components on the same side of PW Board.
      Trim and form standard DIPs in "gull wing" configuration
      Solder paste screened on PW Board
      Pick and place SMDs and DIPs
      Bake
      Vapor/IR reflow
      Clean
   2. Components on opposite sides of PW Board.
      Solder paste screened on SMD-side of Printed Wire Board
      Adhesive dispensed at central location of each component
      Pick and place SMDs
      Bake
      Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads
      Lead insert DIPs
      Vapor/IR reflow
      Clean and lead trim

D) Wave Soldering Only
   1. Components on opposite sides of PW Board.
      Adhesive dispense on SMD side of PW Board
      Pick and place SMDs
      Cure adhesive
      Lead insert top side with DIPs
      Wave solder with SMDs down and into solder bath
      Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Wave Soldering of Surface Mount Components (Continued)

THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. Howerver, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

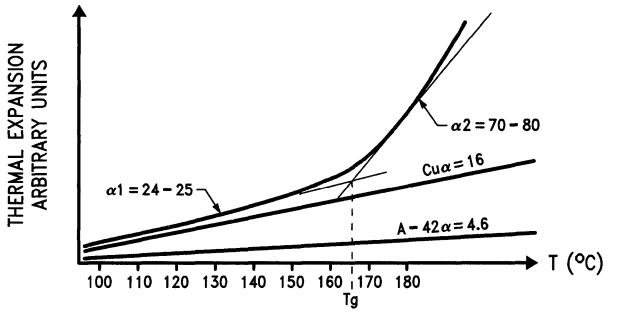

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FIGURE 1. Thermal Expansion and Glass Transition Temperature

Wave Soldering of Surface Mount Components (Continued)

85% relative humidity. Once cycle of approximately 100 hours has been shown to be equivalent to 2000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 2 sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 sec @ 260°C	—	0/83
Solder Dip 6 sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0.30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	0/30	12/30*	14/30*	2/30*
Manuf E	1/30**	0/30	0/30	0/30	0/30
Manuf F	0/30	0/30	0/30	0/30	0/30
Manuf G	0/30	0/30	0/30	0/30	0/30

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

SUMMARY

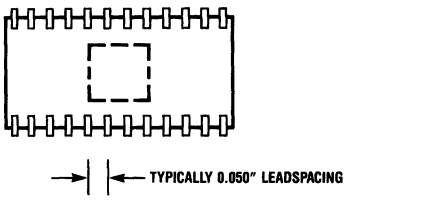
Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

Small Outline (SO) Package Surface Mounting Methods— Parameters and Their Effect on Product Reliability

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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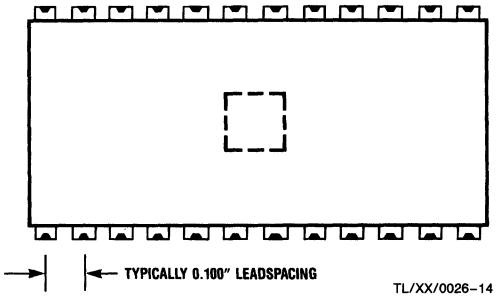
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelerated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

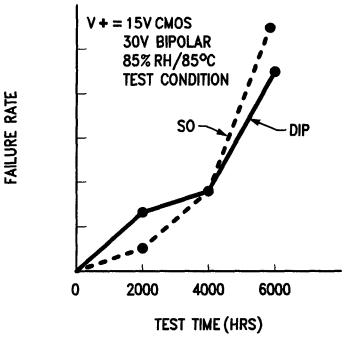

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

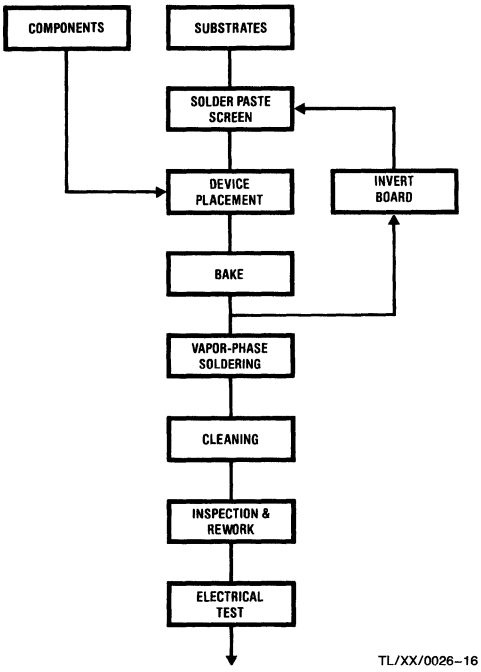
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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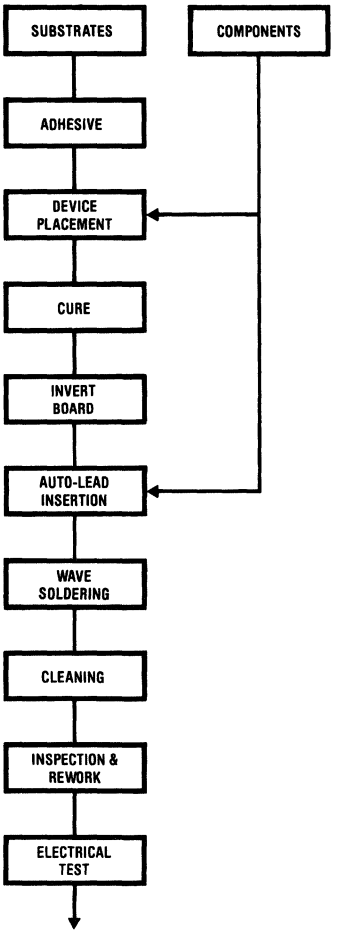
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

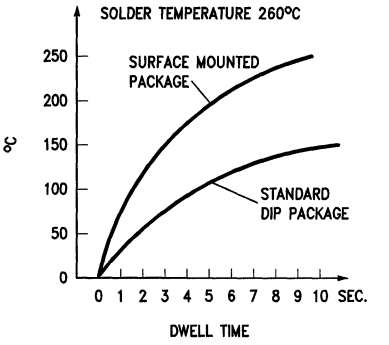

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

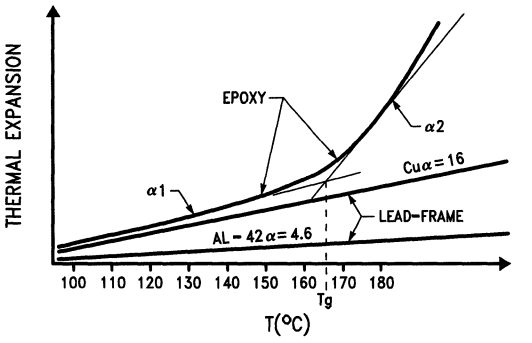

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

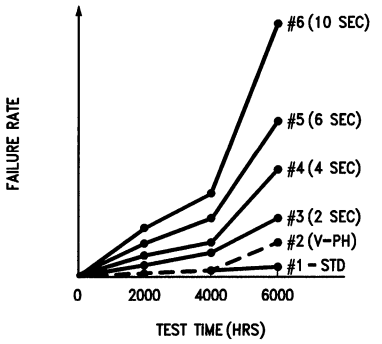

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

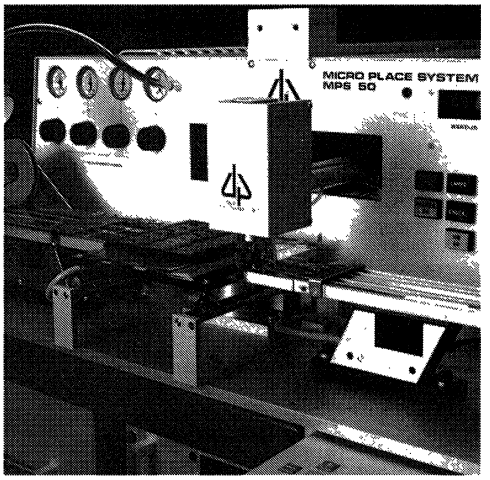
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

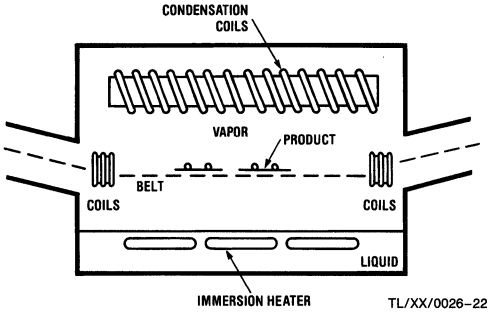
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

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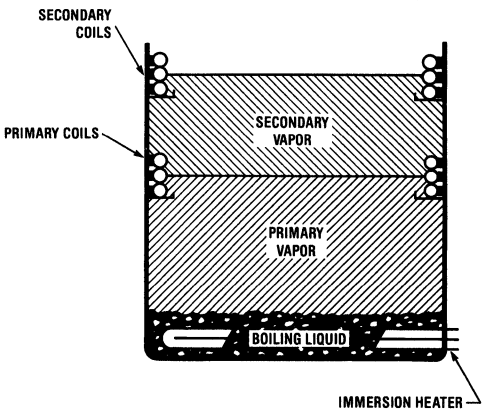
Batch-Fed Production Vapor-Phase Soldering Unit



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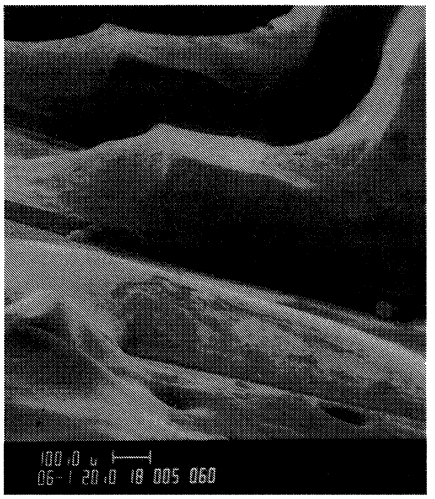
Solder Joints on a SO-14 Package on PCB



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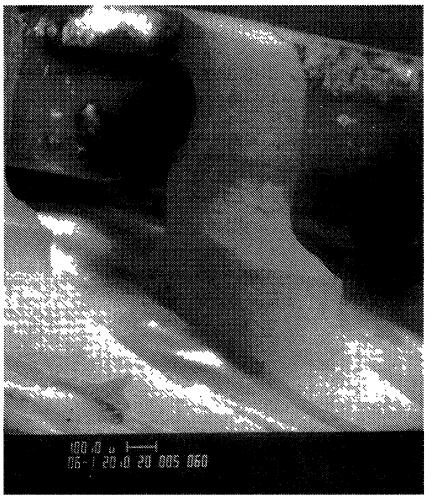
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed 1/8″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

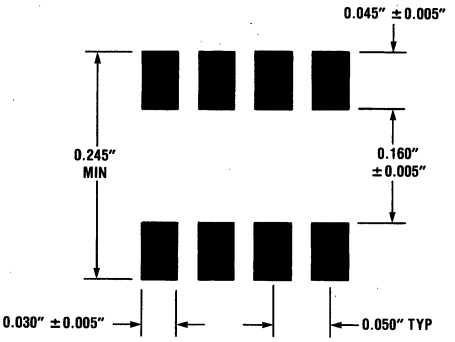
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

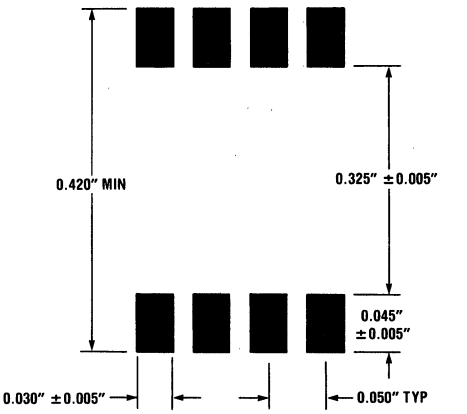
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



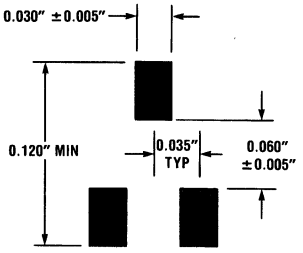
TL/XX/0026–27

SO-16L, SO-20



TL/XX/0026–28

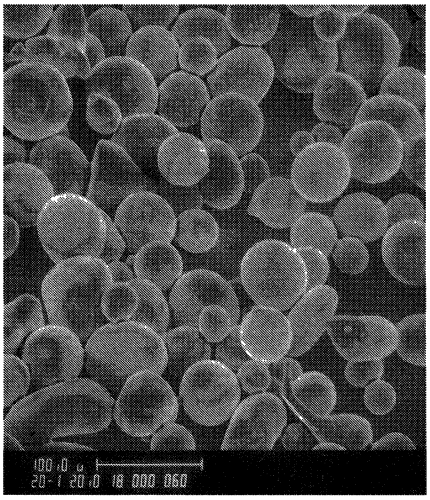
SOT-23



TL/XX/0026–29

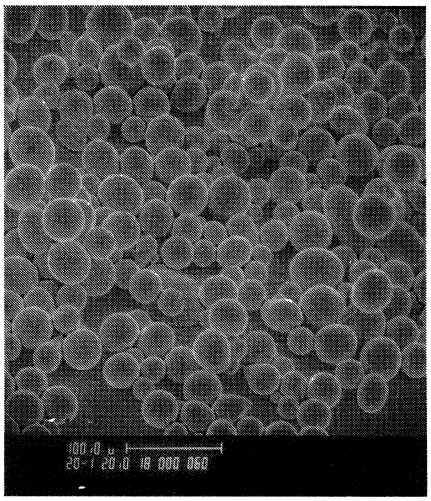
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



TL/XX/0026–30

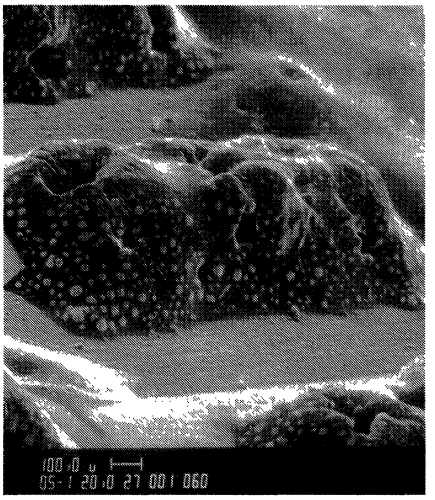
200 × Kester (63/37)



TL/XX/0026–31

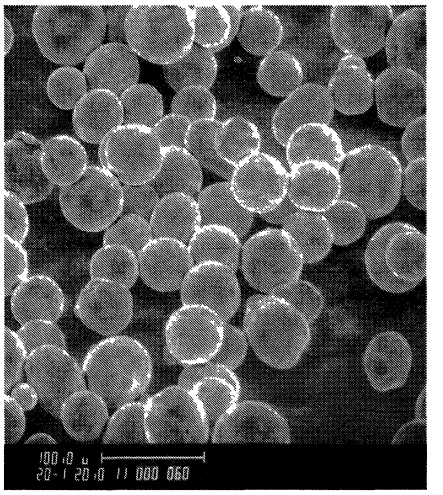
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



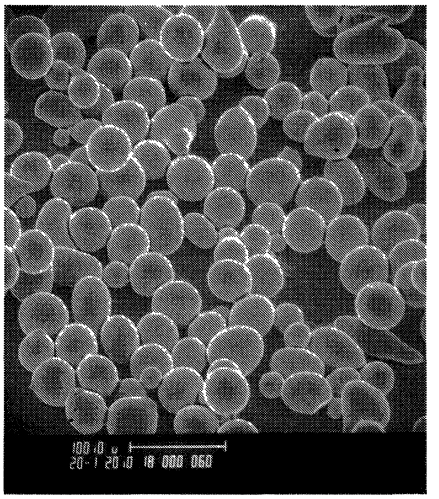
TL/XX/0026-32

200 × Fry Metal (63/37)



TL/XX/0026-33

200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

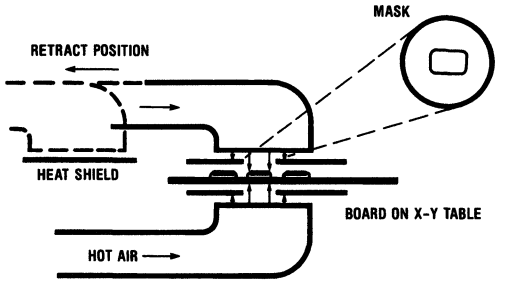
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

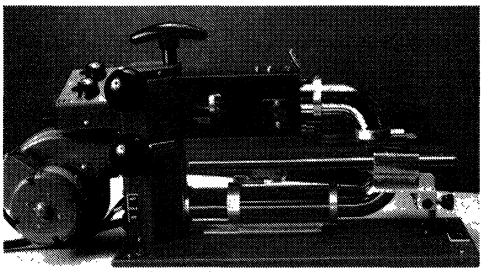
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/XX/0026–35

Hot-Air Rework Machine



TL/XX/0026–36

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

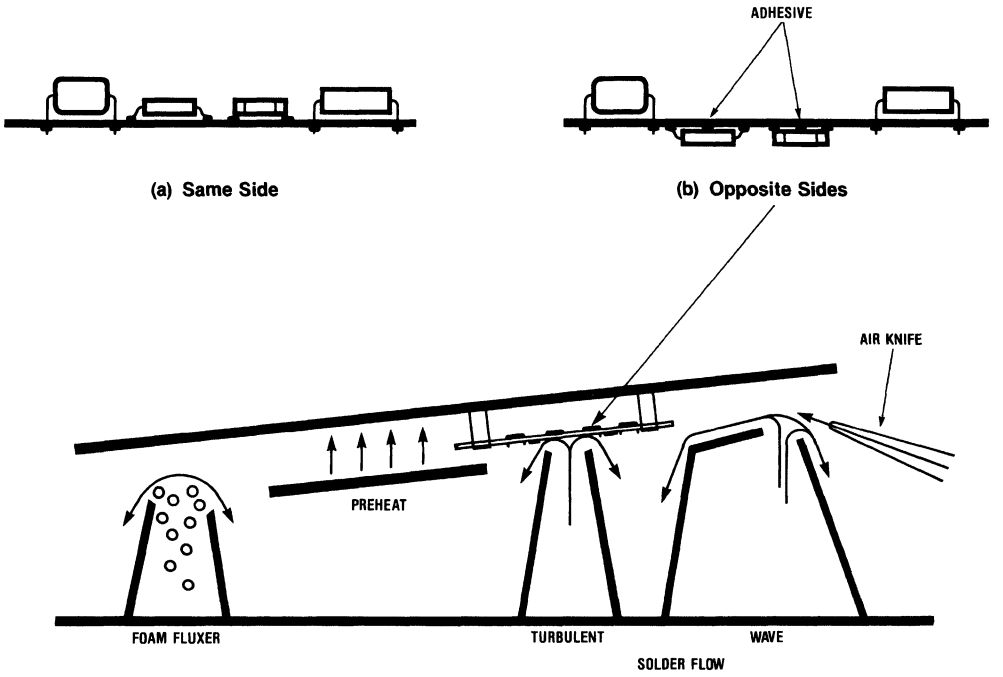
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050" vs 0.100" for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



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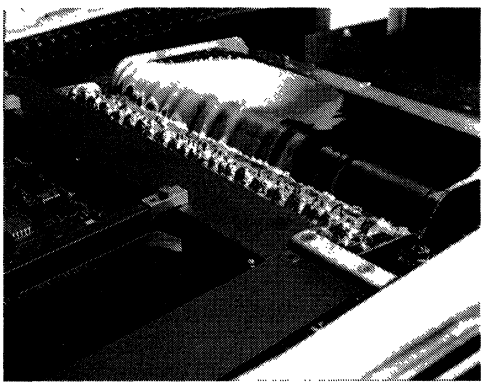
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



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CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

Section 10

Appendices/ Physical Dimensions

Section 10 Contents

National Semiconductor

Appendix A
General Product Marking & Code Explanation

LF 356 N /A+

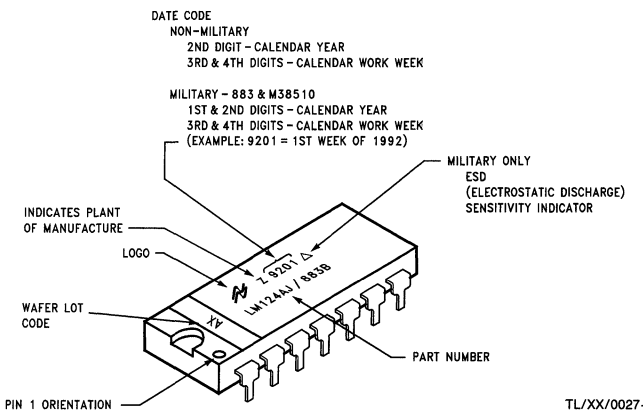
- /A+ — Reliability Program (Optional) (Refer to Appendix C)
- N — Package Type (See Right)
- 356 — Device Number (Generic Type) and Suffix Letter (Optional)
  - A or B: Improved Electrical Specification
  - C, I, E or M: Temperature Range
- LF — Device Family (See Below)

Device Family

ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (Bifet)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LP	Linear (Low Power)
LPC	Linear CMOS (Low Power)
MF	Linear (Monolithic Filter)
LMF	Linear Monolithic Filter

Package Type

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (1/4" x 1/4")
G	12 Lead TO-8 Metal Can (M/C)
H	Multi-Lead Metal Can (M/C)
H-05	4 Lead M/C (TO-5) } Shipped with
H-46	4 Lead M/C (TO-46) } Thermal Shield
J	Lo-Temp Ceramic DIP
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
M3	3-Lead Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 Power Pkg
Q	Cerdip with UV Window
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package



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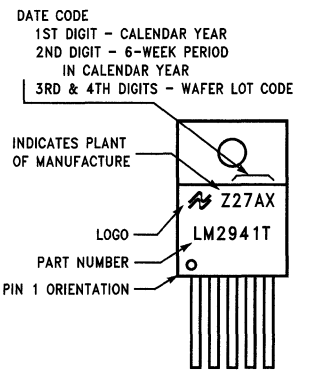

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National Semiconductor

Appendix B
Device/Application Literature Cross-Reference

Device Number	Application Literature
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN-274, AN-280, AN-281, LB-53
ADC08031	AN-460
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC10461	AN-769
ADC10462	AN-769
ADC10464	AN-769
ADC10662	AN-769
ADC10664	AN-769
ADC1210	AN-245
ADC12441	AN-769
ADC12451	AN-769
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ADC3511	AN-200
ADC3701	AN-200
ADC3711	AN-200
AH0014	AN-38
AH0019	AN-38
CD4016	AB-10
DACXXXX	AN-156
DAC0800	AN-693
DAC0830	AN-284
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1000	AN-271, AN-275, AN-277, AN-284
DAC1001	AN-271, AN-275, AN-277, AN-284
DAC1002	AN-271, AN-275, AN-277, AN-284

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-2293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1219	AN-693
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
Digitalker	AN-252, LB-54
DM8890	Appendix B
DS8606	AN-381, AN-382
DS8608	AN-382
DT1058	AN-287
DT1060	AN-287
DTSW250E2	AN-287
DTSW250GI	AN-287
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-262, AN-263, AN-264, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693
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LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LF13508	AN-289, AN-360, AN-447
LF13509	AN-289, AN-295, AN-447

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LH0002	AN-13, AN-63, AN-227, AN-244, AN-263, AN-272, AN-301
LH0005	AN-13
LH0022	AN-63, AN-75
LH0023	AN-245, AN-360
LH0024	AN–253
LH0032	AN-242, AN-244, AN-253
LH0033	AN-48, AN-115, AN-227, AN-253
LH0042	AN-63
LH0043	AN-245
LH0052	AN-63
LH0053	AN-245
LH0062	AN-75
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0082	AN-244, AN-266
LH0086	AN-245, AN-360
LH0091	AN-180
LH0094	AN-301
LH0101	AN-261
LH1605	AN-343
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693
LM11	AN-241, AN-242, AN-260, AN-266, AN-271
LM12	AN-446, AN-693, AN-706
LM101	AN-4, AN-13, AN-20, AN-24, AN-75, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241 AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM104	AN-21, LB-3, LB-7, LB-10, LB-40
LM105	AN-21, AN-23, AN-110, LB-3, LB-7, LB-10
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-63, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	AN-63, LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	AN-115, LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM129	AN-173, AN-178, AN-262, AN-266
LM131	AN-210, AN-460, Appendix D
LM131A	AN-210
LM134	LB-41, AN-460
LM135	AN-225, AN-262, AN-292, AN-298, AN-460
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260, AN-360
LM199A	AN-161
LM211	LB-39
LM216A	LB-37
LM231	AN-210
LM231A	AN-210
LM235	AN-225
LM239	AN-74
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM34	AN-460
LM35	AN-460
LM301A	AN-178, AN-181, AN-222
LM304	LB-40
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-115, AN-299, LB-21
LM319	AN-115, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D
LM331A	AN-210, Appendix C

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM381	AN-64, AN-104
LM382	AN-147
LM385	AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777
LM386	LB-54
LM389	AN-256, AN-263, AN-264, AN-274
LM391	AN-272
LM392	AN-274, AN-286
LM393	AN-271, AN-274, AN-293, AN-694
LM394	AN-262, AN-263, AN-264, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28
LM399	AN-184
LM555	AN-694, AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM604	AN-460
LM628	AN-693, AN-706
LM629	AN-693, AN-694, AN-706
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-75, AN-79, LB-19, LB-22
LM832	AN-386, AN-390
LM833	AN-346
LM1036	AN-390
LM1310	AN-81
LM1458	AN-116
LM1524	AN-272, AN-288, AN-292, AN-293
LM1558	AN-116
LM1578A	AB-30
LM1807	Appendix B

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM1808	Appendix B
LM1820	LB-29
LM1828	Appendix B
LM1830	AB-10
LM1845	Appendix B
LM1865	AN-382, AN-390
LM1894	AN-384, AN-386, AN-390
LM2577	AN-776, AN-777
LM2878	AN-147
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11
LM3045	AN-286
LM3046	AN-146, AN-299
LM3064	Appendix B
LM3065	Appendix B
LM3070	Appendix B
LM3071	Appendix B
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3525A	AN-694
LM3578A	AB-30
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3911	LB-27, AN-460
LM3914	AN-460, LB-48, AB-25
LM3915	AN-386
LM3999	AN-161
LM4250	AN-88, LB-34
LM7800	AN-178
LM78L12	AN-146
LM78S40	AN-711
LMC555	AN-460
LMC835	AN-435
LMD18200	AN-694
LM18293	AN-706
LP324	AN-284
LP395	AN-460

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
MF10	AN-307
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74LS138	LB-54
MM53200	AN-290
2N4339	AN-32

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Appendix C
Summary of Commercial Reliability Programs

General

National Semiconductor Commercial Reliability Programs provide a broad range of off-the-shelf enhanced semiconductor products that supply an extra measure of quality and reliability needed in high-stress or difficult to service applications.

National's A+ and B+ programs allow each individual customer to:

- Minimize the need for incoming electrical inspection
- Eliminate the need and associated costs of using independent testing laboratories
- Reduction in infant mortality rate
- Reduction in reworked board costs
- Reduction in warranty and service costs

A+ Product Enhancement

The A+ Product Enhancement incorporates the benefits of the Multiple-Pass and Elevated Temperature along with "BURN-IN."

The A+ Program provides:

- 100% Temperature Cycling
- 100% Electrical Testing at Room and High Temperature
- 100% Burn-In Testing Combining Increased Temperature with Applied Voltage
- Acceptable Quality Levels Greater than Industry Norm

Typical A+ Flow is:

- SEM
- Assembly and Seal
- Four Hour 150°C Bake
- Five Temperature Cycles (0°C to +100°C)
- High Temperature Electrical Test
- Electrical Test
- Burn-In (160 hours at a minimum junction temperature of 125°C)
- DC Parametric and Function Tests
- Tightened Quality Control Inspection Plans

Note: Certain products may follow slightly different process flows dictated by specific capabilities and device characteristics, consult NSC.

P+ Product Enhancement

The P+ product enhancement program applies to power devices and offers an added advantage. P+ involves dynamic tests that screen out assembly related and silicon defects that can lead to infant mortality and/or reduce the survivability of the device under high stress conditions. This includes but is not limited to the following devices:

Device	Package Types					
	TO-3 K STEEL	TO-39 (H)	TO-220 (T)	TO-202 (P)	DIP (N)	SO (M)
LM12	X					
LM109/309	X	X				
LM117/317	X	X	X	X		
LM117HV/317HV	X	X				
LM120/320	X	X	X	X		
LM123/323	X					
LM133/333	X		X			
LM137/337	X	X	X	X		
LM137HV/337HV	X	X				
LM138/338	X		X			
LM140/340	X		X			
LM145/345	X					
LM150/350	X		X			
LM195/395	X	X	X	X		
LM196/396	X					
LM2930/2935/2984			X			
LM2937			X			
LM2940/2941			X			
LM2990/2991			X			
LM2575/2575HV			X		X	X
LM2576			X			
LM2577			X		X	X
LMD18200/18201			X			
LM18298			X			

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Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our 1987 Reliability Handbook.

National Semiconductor's Military/Aerospace Program is founded on dedication to excellence. National offers complete support across the broadest range of products with the widest selection of qualification levels and screening flows. These flows include:

Process Flows (Integrated Circuits)	Description
JAN S	QPL products processed to MIL-M-38510 Level S for space level applications.
JAN B	QPL products processed to MIL-M-38510 Level B for military applications.
SMD	Standard Military Drawing products processed to Level B with Table I Electricals controlled by DESC. (Formally called DESC Drawing.)
883	Products processed to MIL-STD-883 Level B for military applications.
MLP	Products processed on the Monitored Line (Program) developed by the Air Force for space level applications.
MIL S	Non-JAN products processed to Level S to negotiated electrical specifications for space level applications.
-MIL	Similar to MIL-STD-883 with exceptions noted on Certificate of Conformance.
MSP	Military Screening Program for initial release of advanced products.

- **MIL-M-38510:** The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

  There are two processing levels specified within MIL-M-38510: Class S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft, naval and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

  Tables I and II explain the JAN device marking system.

  Copies of MIL-M-38510, the QPL and other related documents may be obtained from:

  Naval Publications and Forms Center
  5801 Tabor Avenue
  Philadelphia, PA 19120
  (212) 697-2179

- **Standard Military Drawings (SMD):** SMD's are issued to provide standardized versions of devices which are not available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's SMD offerings can be obtained from our authorized distributors, sales offices or DESC. DESC is located in Dayton, Ohio.

- **MIL-STD-883:** Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision D of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

  National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

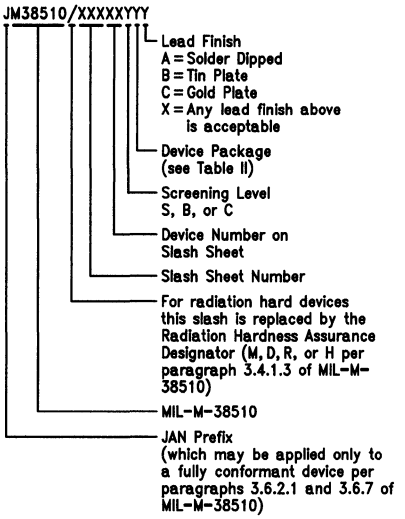
  As with SMDs a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits and test temperatures must be clearly documented. At National Semiconductor, this information is available via our Table I (formerly RETS, Reliability Electrical Test Specification Program). The Table I document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

  Some of National's products are produced on a flow similar to MIL-STD-883. These devices are screened to the same stringent requirements as 883 product, but are marked as **-MIL**; specific reasons for prevention of compliancy are clearly defined in the Certificate of Conformance (C of C) shipped with the product.

- **Monitored Line Program (MLP):** is a non JAN Level S program developed by the Air Force. Monitored Line product usually provides the shortest cycle time, and is acceptable for application in several space level programs. Lockheed Missiles and Space Company in Sunnyvale, California, under an Air Force contract, provides "on-site" monitoring of product processing, and as appropriate, program management. Monitored Line orders generally do not allow "customizing", and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company.

- **Military Screening Program (MSP):** National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking



TL/XX/0030–1

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-pin 1/4" x 1/4" (Metal) Flatpak
B	14-pin 3/16" x 1/4" (Metal) Flatpak
C	14-pin 1/4" x 3/4" Dual-In-Line
D	14-pin 1/4" x 3/8" (Ceramic) Flatpak
E	16-pin 1/4" x 7/8" Dual-In-Line
F	16-pin 1/4" x 3/8" (Metal or Ceramic) Flatpak
G	8-pin TO-99 Can or Header
H	10-pin 1/4" x 1/4" (Metal) Flatpak
I	10-pin TO-100 Can or Header
J	24-pin 1/2" x 1 1/4" Dual-In-Line
K	24-pin 3/8" x 5/8" Flatpak
L	24-pin 1/4" x 1 1/4" Dual-In-Line
M	12-pin TO-101 Can or Header
N	(Note 1)
P	8-pin 1/4" x 3/8" Dual-In-Line
Q	40-pin 3/16" x 2 1/16" Dual-In-Line
R	20-pin 1/4" x 1 1/16" Dual-In-Line
S	20-pin 1/4" x 1/2" Flatpak
T	(Note 1)
U	(Note 1)
V	18-pin 3/8" x 15/16" Dual-In-Line
W	22-pin 3/8" x 1 1/8" Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350" x 0.350" Chip Carrier
3	28-terminal 0.450" x 0.450" Chip Carrier

Note 1: These letters are assigned to packages by individual MIL-M-38510 detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
1.	Wafer Lot Acceptance	5007	All Lots		
2.	Nondestructive Bond Pull (Note 14)	2023	100%		
3.	Internal Visual (Note 1)	2020, Condition A	100%	2010, Condition B	100%
4.	Stabilization Bake (Note 16)	1008, Condition C, Min 24 Hrs. Min	100%	1008, Condition C, Min 24 Hrs. Min	100%
5.	Temperature Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E Min Y_1 Orientation Only	100%	2001, Condition E Min Y_1 Orientation Only	100%
7.	Visual Inspection (Note 3)		100%		100%
8.	Particle Impact Noise Detection (PIND)	2010, Condition A (Note 4)	100%		
9.	Serialization	(Note 5)	100%		
10.	Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	

TABLE III. 100% Screening Requirements (Continued)

	Screen	Class S		Class B	
		Method	**Reqmt**	**Method**	**Reqmt**
11.	Burn-In Test	1015 240 Hrs. @ 125°C Min (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min	100%
12.	Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 3)	100%		
13.	Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min (Cond. F Not Allowed)	100%		
14.	Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15.	PDA Calculation	5% Parametric (Note 14), 3% Functional	All Lots	5% Parametric (Note 14)	All Lots
16.	Final Electrical Test (Note 15) a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005) b) Dynamic Tests or Functional Tests 1) 25°C (Subgroup 4 or 7) 2) Max and Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005) c) Switching Tests 25°C (Subgroup 9, Table I, 5005)	Per Applicable Device Specification	 100% 100% 100% 100% 100%	Per Applicable Device Specification	 100% 100% 100% 100% 100%
17.	Seal Fine, Gross	1014	100% (Note 8)	1014	100% (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock Method 1011, Test Condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpaks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

Military Analog Products Available from National Semiconductor

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
HIGH PERFORMANCE AMPLIFIERS AND BUFFERS				
LF147	D, J	Wide BW Quad JFET Op Amp	SMD/JAN	/11906
LF155	J, W, H	JFET Input Op Amp	883/JAN	/11401
LF155A	H	JFET Input Op Amp	883	—
LF156	J, W, H	JFET Input Op Amp	883/JAN	/11402
LF156A	H	JFET Input Op Amp	883	—
LF157	H	JFET Input Op Amp	883	—
LF157A	H	JFET Input Op Amp	883	—
LF411M	H, J	Low Offset, Low Drift JFET Input	883/JAN	/11904
LF412M	H, J	Low Offset, Low Drift JFET Input-Dual	883/JAN	/11905
LF441M	H	Low Power JFET Input	883	—
LF442M	H	Low Power JFET Input-Dual	883	—
LF444M	D	Low Power JFET Input-Quad	883	—
LH0002	H	Buffer Amp	883/MIL	7801301
LH0021	K	1.0 Amp Power Op Amp	883/SMD	85088
LH0024	H	High Slew Rate Op Amp	"-MIL"	—
LH0032	G	Ultra Fast FET-Input Op Amp	883/SMD	80013
LH0041	G	0.2 Amp Power Op Amp	883/SMD	85087
LH0061	K	0.5 Amp Wide Bandwidth Op Amp	"-MIL"	—
LH0101	K	Power Op Amp	883/SMD	85089
LH4118	G	Low Gain Wide Band RF Amp	"-MIL"	—
LH4161	H	Trimmed LM6161 VIP Amp	"-MIL"	—
LH4162	H	Dual LH4161	"-MIL"	—
LM10	H	Super-Block™ Micropower Op Amp/Ref	883/SMD	5962-87604
LM101A	J, H, W	General Purpose Op Amp	883/JAN	/10103
LM108A	J, H, W	Precision Op Amp	883/JAN	/10104
LM118	J, H, W	Fast Op Amp	883/JAN	/10107
LM124	J, E, W	Low Power Quad Op Amp	883/JAN	/11005
LM124A	J, W	Low Power Quad	883/JAN	/11006
LM146	J	Quad Programmable Op Amp	883	—
LM148	J, E, W	Quad 741 Op amp	883/JAN	/11001
LM158A	J, H	Low Power Dual Op Amp	883/SMD	5962-8771002
LM158	J, H	Low Power Dual Op Amp	883/SMD	5962-8771001
LM604AM	J	Super-Block 4 Channel Mux Amp	883/SMD	5962-89639
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	TBD
LM613AM	J, E	Super-Block Dual Op Amp/Dual Comp/Ref	883/SMD	TBD
LM614AM	J	Super-Block Quad Op Amp/Ref	883/SMD	TBD
LM709A	H, J, W	General Purpose Op Amp	883/SMD	7800701
LM741	J, H, W	General Purpose Op Amp	883/JAN	/10101
LM747	J, H, W	General Purpose Dual Op Amp	883/JAN	/10102
LM6118	J, E	VIP Dual Op Amp	883/SMD	5962-91565
LM6121	H	VIP Buffer	883/SMD	5962-90812
LM6125	H	VIP Buffer with Error Flag	883/SMD	5962-90815
LM6161	J, E, W	VIP Op Amp (Unity Gain)	883/SMD	5962-89621
LM6164	J, E, W	VIP Op Amp ($A_V > 5$)	883/SMD	5962-89624
LM6165	J, E, W	VIP Op Amp ($A_V > 25$)	883/SMD	5962-89625
LM6162	J, E, W	VIP Op Amp ($A_V > 2, -1$)	883/SMD	5962-92165
LMC660AM	J	Low Power CMOS Quad Op Amp	883/SMD	TBD
LMC662AM	J	Low Power CMOS Dual Op Amp	883/SMD	TBD
LPC660AM	J	Micropower CMOS Quad Op Amp	883/SMD	TBD
LPC662AM	J	Micropower CMOS Dual Op Amp	883/SMD	TBD
OP07	H	Precision Op Amp	SMD/JAN	/13502

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
COMPARATORS				
LF111	H	Voltage Comparator	"-MIL"	—
LH2111	J, W	Dual Voltage Comparator	883/JAN	/10305
LM106	H, W	Voltage Comparator	883/SMD	8003701
LM111	J, H, E, W	Voltage Comparator	883/JAN	/10304
LM119	J, H, E, W	High Speed Dual Comparator	883/JAN	/10306
LM139	J, E, W	Quad Comparator	883/JAN	/11201
LM139A	J	Precision Quad Comparator	883/SMD	5962-87739
LM160	J, H	High Speed Differential Comparator	883/SMD	8767401
LM161	J, H	High Speed Differential Comparator	883/SMD	5962-87572
LM193A	J, H	Dual Comparator	883/JAN	/11202
LM612AM	J	Dual-Channel Comparator/Reference	883/SMD	TBD
LM613AM	J, E	Super-Block Dual Comparator/ Dual Op Amp/Adj Reference	883/SMD	TBD
LM615AM	J	Quad Comparator/Adjustable Reference	883/SMD	TBD
LM710A*	J, H, W	Voltage Comparator	883/JAN	/10301
LM711A*	J, H, W	Dual LM710	883/JAN	/10302
LM760	J, H	High Speed Differential Comparator	883/JAN	5962-87545
*Formerly manufactured by Fairchild Semiconductor as part numbers μA710 and μA711.				
LINEAR REGULATORS				
Positive Voltage Regulators				
LH0075	G	Precision Voltage Regulator	"-MIL"	—
LM105	H	Adjustable Voltage Regulator	883/SMD	5962-89588
LM109	H	5V Regulator, I_O = 20 mA	883/JAN	/10701BXA
LM109	K	5V Regulator, I_O = 1A	883/JAN	/10701BYA
LM117	H, E, K	Adjustable Regulator	883/JAN	/11703, /11704
LM117A	H	Precision Adjustable Regulator, I_O = 0.5A	883/SMD	7703405XA
LM117A	K	Precision Adjustable Regulator, I_O = 1.5A	883/SMD	7703405YA
LM117HV	H	Adjustable Regulator, I_O = 0.5A	883/SMD	7703402XA
LM117HV	K	Adjustable Regulator, I_O = 1.5A	883/SMD	7703402YA
LM123	K	3A Voltage Regulator	883	—
LM138	K	5A Adjustable Regulator	"-MIL"	—
LM140H-5.0	H	0.5A Fixed 5V Regulator	883/JAN	/10702
LM140H-6.0	H	0.5A Fixed 6V Regulator	883	—
LM140H-8.0	H	0.5A Fixed 8V Regulator	883	—
LM140H-12	H	0.5A Fixed 12V Regulator	883/JAN	/10703
LM140H-15	H	0.5A Fixed 15V Regulator	883/JAN	/10704
LM140H-24	H	0.5A Fixed 24V Regulator	883	—
LM140AK-5.0	K	1.0A Fixed 5V Regulator	883	—
LM140AK-12	K	1.0A Fixed 12V Regulator	883	—
LM140AK-15	K	1.0A Fixed 15V Regulator	883	—
LM140K-5.0	K	1.0A Fixed 5V Regulator	883/JAN	/10706
LM140K-12	K	1.0A Fixed 12V Regulator	883/JAN	/10707
LM140K-15	K	1.0A Fixed 15V Regulator	883/JAN	/10708
LM140K-24	K	1.2A Fixed 24V Regulator	883/JAN	/10709
LM140LAH-5.0	H	100 mA Fixed 5V Regulator	883	—
LM140LAH-12	H	100 mA Fixed 12V Regulator	883	—
LM140LAH-15	H	100 mA Fixed 15V Regulator	883	—
LM150	K	3A Adjustable Power Regulator	883	—
LM2940K-5.0	K	5V Low Dropout Regulator	883/SMD	5962-89587
LM2940K-8.0	K	8V Low Dropout Regulator	883/SMD	5962-90883
LM2940K-12	K	12V Low Dropout Regulator	883/SMD	5962-90884
LM2940K-15	K	15V Low Dropout Regulator	883/SMD	5962-90885
LM2941K	K	Adjustable Low Dropout Regulator	883/SMD	TBD
LM723	H, J, E	Precision Adjustable Regulator	883/JAN	/10201
LM78MG	H	Adjustable Regulator	883	—
LP2951	H, E, J	Adjustable Micropower LDO	883/SMD	5962-38705
LP2953AM	J	250 mA Adj. Micropower LDO	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
LINEAR REGULATORS (Continued)				
Negative Voltage Regulators				
LH0076	G	Precision Programmable Regulator	"-MIL"	—
LM104	H	Precision Negative Regulator	883/SMD	5962-87605
LM120H-5.0	H	Fixed 0.5A Regulator, $V_{OUT} = -5V$	883/JAN	/11501
LM120H-8.0	H	Fixed 0.5A Regulator, $V_{OUT} = -8V$	883	—
LM120H-12	H	Fixed 0.5A Regulator, $V_{OUT} = -12V$	883/JAN	/11502
LM120H-15	H	Fixed 0.5A Regulator, $V_{OUT} = -15V$	883/JAN	/11503
LM120K-5.0	K	Fixed 1.0A Regulator, $V_{OUT} = -5V$	883/JAN	/11505
LM120K-12	K	Fixed 1.0A Regulator, $V_{OUT} = -12V$	883/JAN	/11506
LM120K-15	K	Fixed 1.0A Regulator, $V_{OUT} = -15V$	883/JAN	/11507
LM137A	H	Precision Adjustable Regulator	883/SMD	7703406XA
LM137A	K	Precision Adjustable Regulator	883/SMD	7703406YA
LM137	H, K	Adjustable Regulator	883/JAN	/11803, /11804
LM137HV	H	Adjustable (High Voltage) Regulator	883/SMD	7703404XA
LM137HV	K	Adjustable (High Voltage) Regulator	883/SMD	7703404YA
LM145K-5.0	K	Negative 3 Amp Regulator	883/SMD	5962-90645
LM145K-5.2	K	Negative 3 Amp Regulator	883	—
LM79MG	H	Adjustable Regulator	883	—
SWITCHING REGULATORS				
LM1575-5	K	Simple Switcher™ Step-Down, $V_{OUT} = 5V$	883/SMD	TBD
LM1575-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	TBD
LM1575-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	TBD
LM1575-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	TBD
LM1575HV-5	K	Simple Switcher Step-Down, $V_{OUT} = 5V$	883/SMD	TBD
LM1575HV-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	TBD
LM1575HV-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	TBD
LM1575HV-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	TBD
LM1577-12	K	Simple Switcher Step-Up, $V_{OUT} = 12V$	883/SMD	TBD
LM1577-15	K	Simple Switcher Step-Up, $V_{OUT} = 15V$	883/SMD	TBD
LM1577-ADJ	K	Simple Switcher Step-Up, Adj V_{OUT}	883/SMD	TBD
LM1578	H	750 mA Switching Regulator	883/SMD	5962-89586
LM78S40*	J	Universal Switching Regulator Subsystem	883/SMD	5962-88761

*Formerly manufactured by Fairchild Semiconductor as the μA78S40DMQB.

VOLTAGE REFERENCES				
LM103-3.0	H	Reference Diode, BV = 3.0V	883/SMD	7702806
LM103-3.3	H	Reference Diode, BV = 3.3V	883/SMD	7702807
LM103-3.6	H	Reference Diode, BV = 3.6V	883/SMD	7702808
LM103-3.9	H	Reference Diode, BV = 3.9V	883/SMD	7702809
LM113	H	Reference Diode with 5% Tolerance	883/SMD	5962-8671101
LM113-1	H	Reference Diode with 1% Tolerance	883/SMD	5962-8671102
LM113-2	H	Reference Diode with 2% Tolerance	883/SMD	5962-8671103
LM129A	H	Precision Reference, 10 ppm/°C Drift	883/SMD	5962-8992101XA
LM129B	H	Precision Reference, 20 ppm/°C Drift	883/SMD	5962-8992102XA
LM136A-2.5	H	2.5V Reference Diode, 1% V_{OUT} Tolerance	883	—
LM136A-5.0	H	5V Reference Diode, 1% V_{OUT} Tolerance	883/SMD	8418001
LM136-2.5	H	2.5V Reference Diode, 2% V_{OUT} Tolerance	883	—
LM136-5.0	H	5V Reference Diode, 2% V_{OUT} Tolerance	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
VOLTAGE REFERENCES (Continued)				
LM169	H	10V Precision Reference, Low Tempco 0.05% Tolerance	883/SMD	TBD
LM185	H, E	Adjustable Micropower Voltage Reference	883	—
LM185BXH2.5	H	2.5V Micropower Reference Diode, Ultralow Drift	883/SMD	5962-8759404
LM185BY	H	Adjustable Micropower Voltage Reference	883	—
LM185BYH1.2	H	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759405
LM185BYH2.5	H	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759406
LM185-1.2	H, E	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759401
LM185-2.5	H, E	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759402
LM199	H	Precision Reference, Low Tempco	883/SMD	5962-8856102
LM199A	H	Precision Reference, Ultralow Tempco	883/SMD	5962-8856101
LM199A-20	H	Precision Reference, Ultralow Tempco	883	—
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	TBD
LM612AM	J	Super-Block Dual-Channel Comparator/Reference	883/SMD	TBD
LM613AM	J, E	Super-Block Dual Op Amp/DualComp/Dual Ref	883/SMD	TBD
LM614AM	J	Super-Block Quad Op Amp/Reference	883/SMD	TBD
LM615AM	J	Super-Block Quad Comparator/Reference	883/SMD	TBD
LH0070-0	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-1	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-2	H	Precision BCD Buffered Reference	"-MIL"	—
DATA ACQUISITION				
ADC08020L	J	8-Bit μP-Compatible	883/SMD	5962-90966
ADC0851	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC0858	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC1241CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	TBD
ADC12441CM	J	Dynamically-Tested ADC1241	883/SMD	TBD
ADC1251CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	TBD
ADC12451CM	J	Dynamically-Tested ADC1251	883/SMD	TBD
ADC10061CM	J	10-Bit Multistep ADC	883/SMD	TBD
ADC10062CM	J	10-Bit Multistep ADC w/Dual Input Multiplexer	883/SMD	TBD
ADC10064CM	J	10-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC08061CM	J	8-Bit Multistep ADC	883/SMD	TBD
ADC08062CM	J	8-Bit Multistep ADC w/Dual Input Multiplexer	883/SMD	TBD
ADC08064CM	J	8-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC08068CM	J	8-Bit Multistep ADC w/Octal Input Multiplexer	883/SMD	TBD

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
DATA ACQUISITION SUPPORT				
Switched Capacitor Filters				
LMF60CMJ50	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF60CMJ100	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF90CM	J	4th Order Elliptic Notch	883/SMD	5962-90968
LMF100A	J, E	Dual 2nd Order General Purpose	883/SMD	TBD
Sample and Hold				
LF198	H	Monolithic Sample and Hold	SMD/JA	5962-87608 /12501

Note 1: D: Side-Brazed DIP
E: Leadless Ceramic Chip Carrier
G: Metal Can (TO-8)
H: Metal Can (TO-39, TO-5, TO-99, TO-100)
J: Ceramic DIP
K: Metal Can (TO-3)
W: Flatpak

Note 2: Process Flows
JAN = JM38510, Level B
SMD = Standard Military Drawing
883 = MIL-STD-883 Rev C
-MIL = Exceptions to 883C noted on Certificate of Conformance

Note 3: Please call your local sales office to determine price and availability of space-level products. All "LM" prefix products in this guide are availble with space-level processing.

National Semiconductor

Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

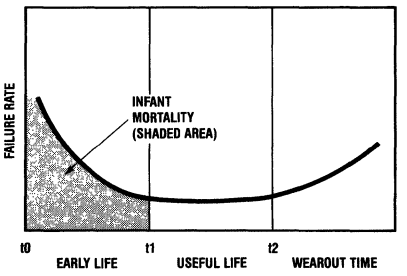


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

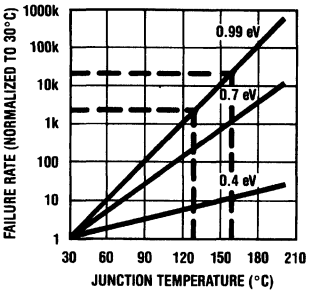

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

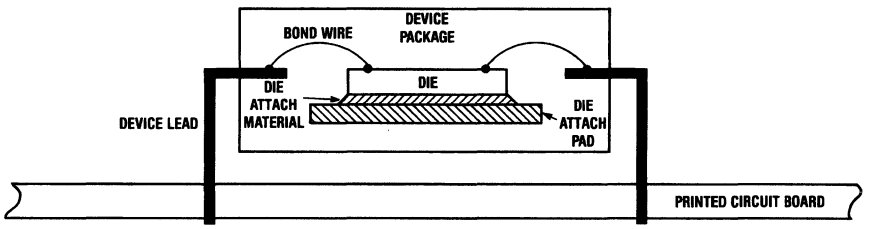

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

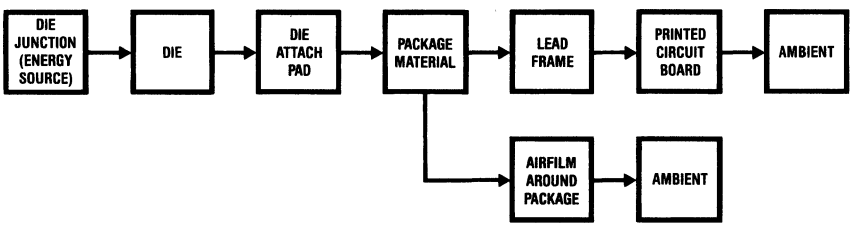

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

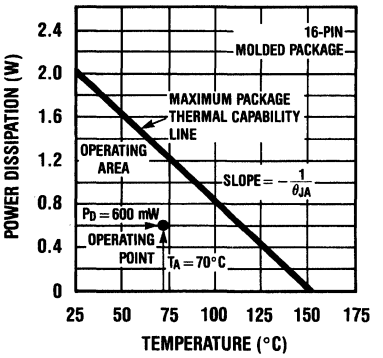

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

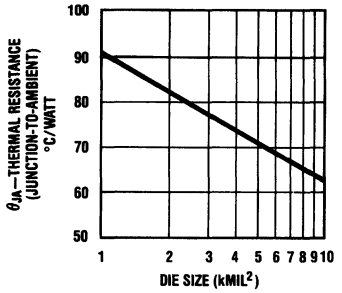

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

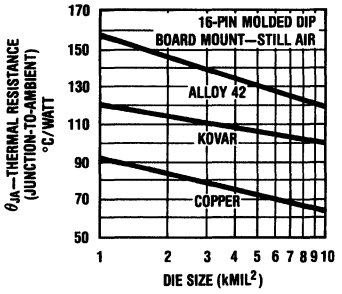

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

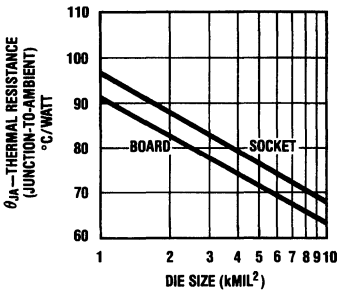

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

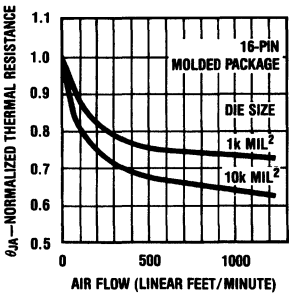

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

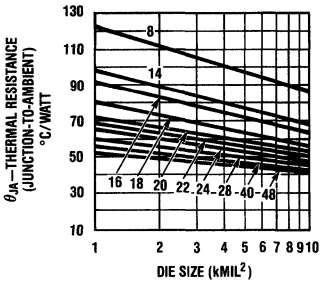
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70°C = 1476\ mW - (11.8\ mW/°C) \times (70°C - 25°C)$$
$$= 945\ mW$$

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air

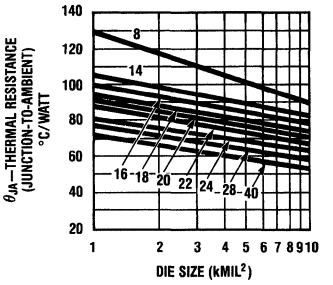


*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

TL/H/9312–10

FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

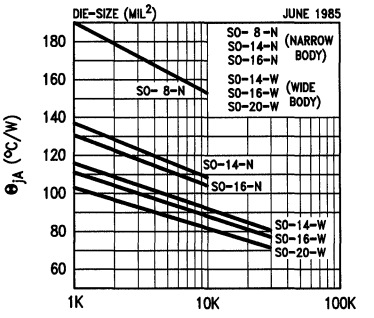
Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/H/9312–11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)



Θ_{JA} - THERMAL RESISTANCE FOR "SO" PACKAGES (BOARD MOUNT)

TL/H/9312–12

FIGURE 12

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APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, **Note 6**)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	2.0		0.5	2.0		µA
	$5V \le V_S \le 30V$	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	$T_j = T_{MAX}$ for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \le T_j \le +300°F$ for the LM34 and LM34A; $-40°F \le T_j \le +230°F$ for the LM34C and LM34CA; and $+32°F \le T_j \le +212°F$ for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \le T_j \le 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1.*

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1.*

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

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Appendix G
Obsolete Product Replacement Guide

Some device types, individual temperature grades and package options have been discontinued. This guide is provided to help design engineers select and specify an appropriate alternative.

NSC Part Number	Replacement	Note
ADB1200	ADC3711	2
AF100	None	
AF121	None	
AF134	None	
DAC1200/1201	DAC1265	2
DH3467	None	
DH3725	None	
DS8627	None	
DS8628	None	
LF352	LM3631	2
LF400	None	
LF401	None	
LF13300	ADC3711	2
LF13741	None	
LH0001	LM4250	2
LH0005/LH0005A	LH0003	2
LH0020	LH0101	2
LH0022	AD506	2
LH0023	AD585	2
LH0037	LH0036	3
LH0038	None	
LH0043	AD583	2
LH0044	OP07	2
LH0045	None	
LH0052	OP100	2
LH0053	None	
LH0061	None	
LH0062	HA5162	2
LH0075	None	
LH0076	None	
LH0082	None	
LH0084	None	
LH0086	None	
LH0091	None	
LH0132	LH0032	2
LH2011	LM11	2
LH2101	LM101	2
LH2108	LM108	2
LH2110	LM110	2
LH2201A	LM201A	2

NSC Part Number	Replacement	Note
LH2208	LM208	2
LH2208A	LM208A	2
LH2301	LM301	2
LH2308	LM308	2
LH2310	LM310	2
LH4003	EL2031	2
LH4006	CLC110	2
LH4008	BB3553	2
LH4009	BB3553	2
LH4010	EL2004	2
LH4011	None	
LH4012	None	
LH4033	LH0033	2
LH4063	LH0063	2
LH4101	LM6313	2
LH4105	LM6218	2
LH4106	LM6313	2
LH4117	LM6181	2
LH4124	LM6181	2
LH4141	OPA654	2
LH4161	LM6361	2
LH4162	LM6361	2
LH4200	CLC104	2
LH4201	CLC104	2
LH4266	None	
LH4267	None	
LH4810	None	
LH4860	None	
LH7001	None	
LH7070	LH0070	2
LH24250	LM11	2
LM170/270/370	LM13600N	2
LM171/271/371	None	
LM172/272/372	None	
LM173/273/373	None	
LM174/274/374	None	
LM175/275/375	None	
LM216/316	LM11	2
LM363	None	
LM388N-2/N-3	LM388N-1	2
LM377N	LM2877P	3

Note 1: Pin for Pin replacement.

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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NSC Part Number	Replacement	Note
LM378N	LM2878P	3
LM379	LM2879T	3
LM322H	LM122H	2
LM565CH	LM565H	2
LM567CH	LM567H	2
LM592	None	
LM733	None	
LM776	None	
LM1014	None	
LM1017	None	
LM1019	None	
LM1800	None	
LM1801	None	
LM1822	LM1823	3
LM1812	None	
LM1837	None	
LM1863	LM1868	3
LM1866	None	
LM1870	None	
LM1871	None	
LM1872	None	

NSC Part Number	Replacement	Note
LM1877N-1/N-2/N-3	LM1877N-9	2
LM1880	None	
LM1884	None	
LM1889	None	
LM1895	LM1896	3
LM1897	None	
LM1965	LM1865	3
LM2002	None	
LM2005	None	
LM2065	LM1865	3
LM2895	LM2896	3
LM2905N	LM3905N	2
LM3011	None	
LM3064	None	
LM3075	None	
LM3820	None	
LM4500	None	
LM776	None	
LMC669	None	
MH0007	CTS0007	1
MM54240	None	

Note 1: Pin for Pin replacement

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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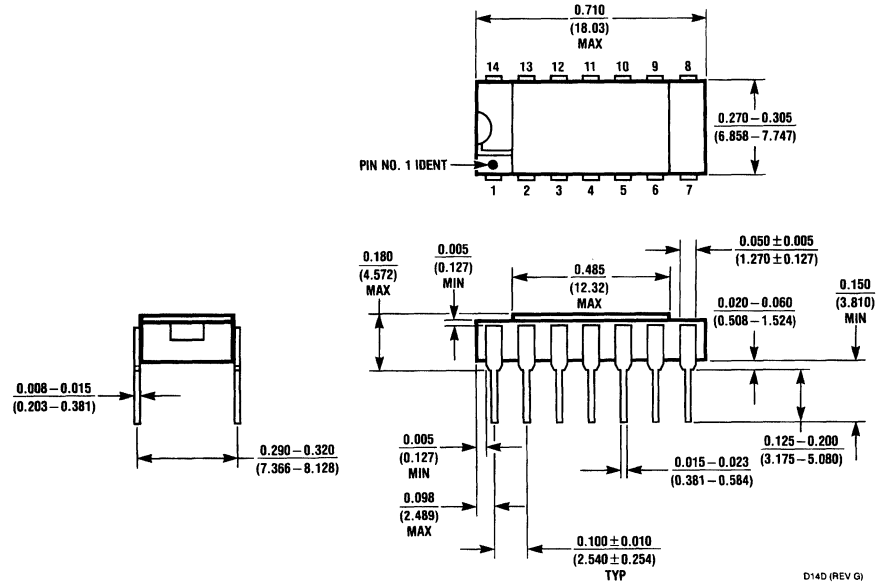
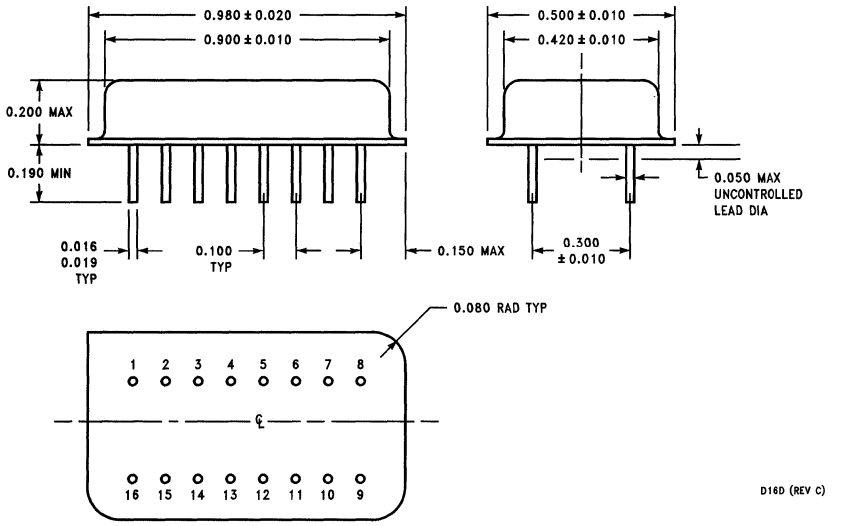
All dimensions are in inches (millimeters)

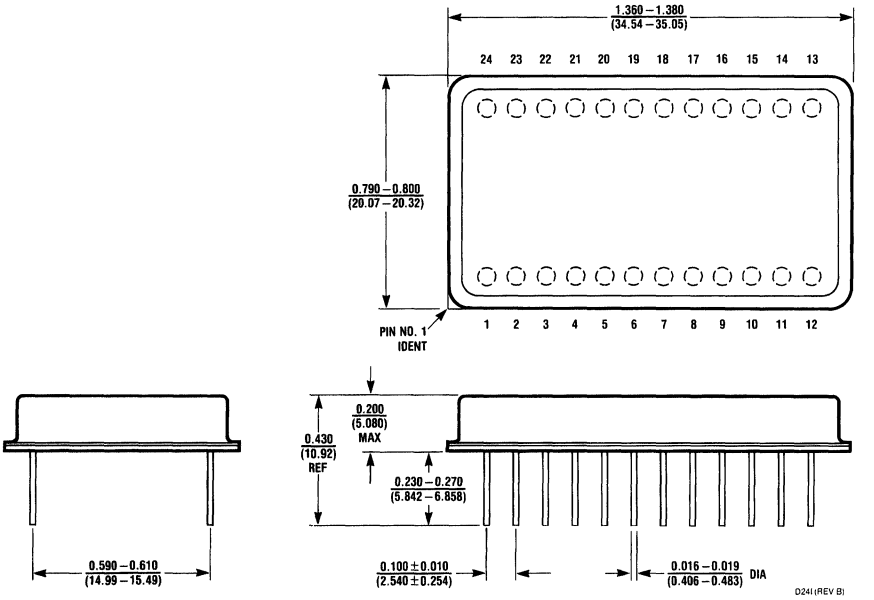
14 Lead Hermetic Dual In-Line Package (D)
NS Package Number D14D



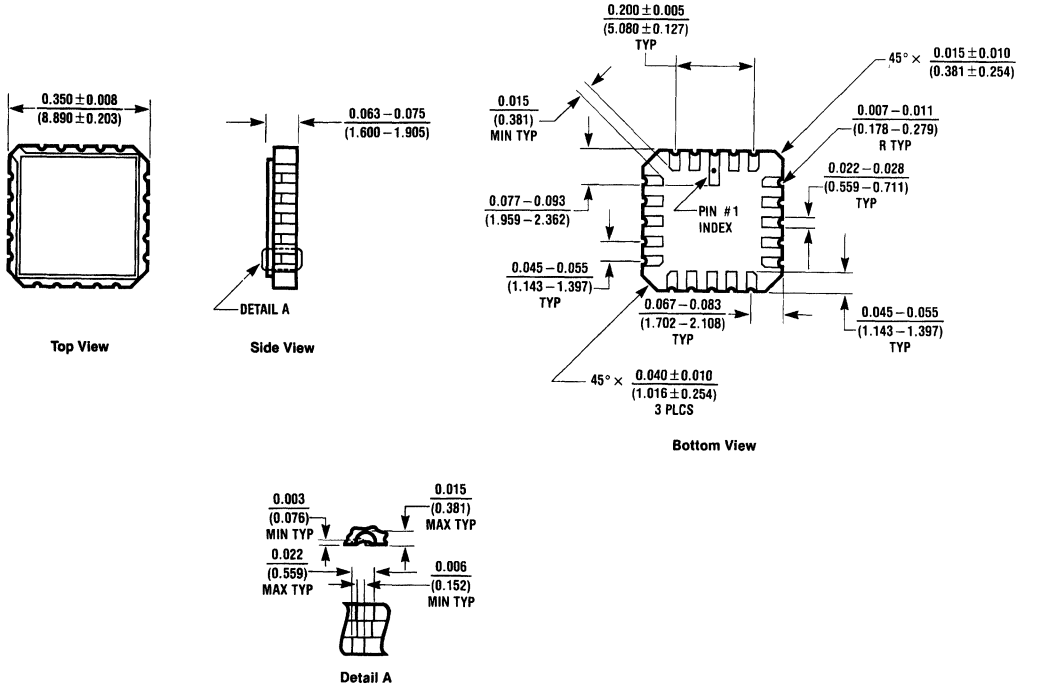
16 Lead Hybrid Metal Can Dual In-Line Package (D)
NS Package Number D16D



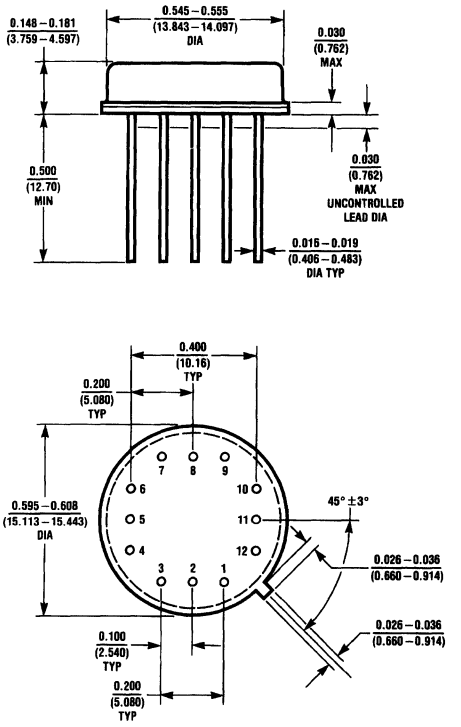
24 Lead (0.600" Wide) Dual In-Line Metal Package (D)
NS Package Number D24I



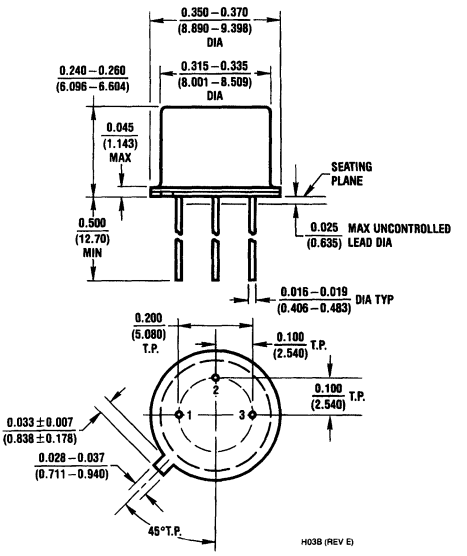
20 Terminal Ceramic Leadless Chip Carrier (LCC)
NS Package Number E20A



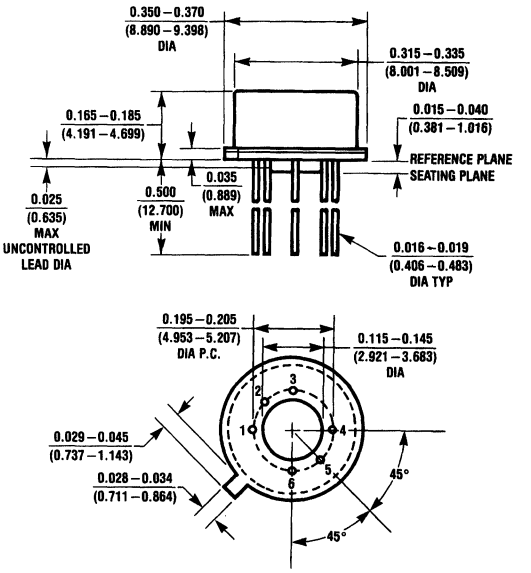
12 Lead (0.400" Square Pattern) Metal Can Package (G)
NS Package Number G12B



3 Lead (0.200" Diameter P.C.) TO-39 Metal Can Package (H)
NS Package Number H03B

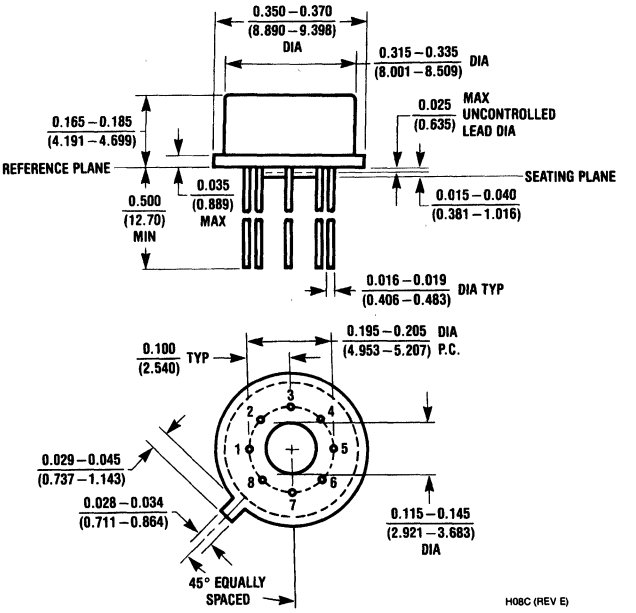


6 Lead (0.200" Diameter P.C.) TO-99 Metal Can Package (H)
NS Package Number H06C



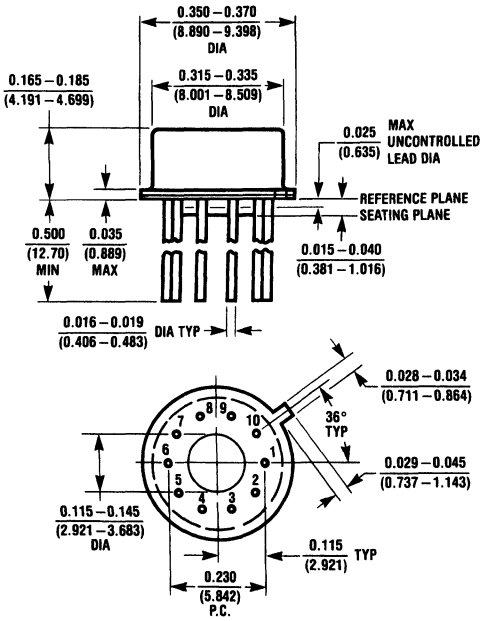
H06C (REV D)

8 Lead (0.200" Diameter P.C.) TO-99 Metal Can Package (H)
NS Package Number H08C



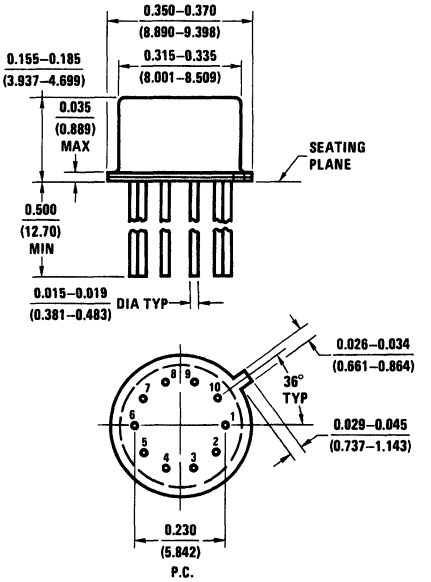
H08C (REV E)

10 Lead (0.230" Diameter P.C.) TO-100 Metal Can Package (H)
NS Package Number H10C



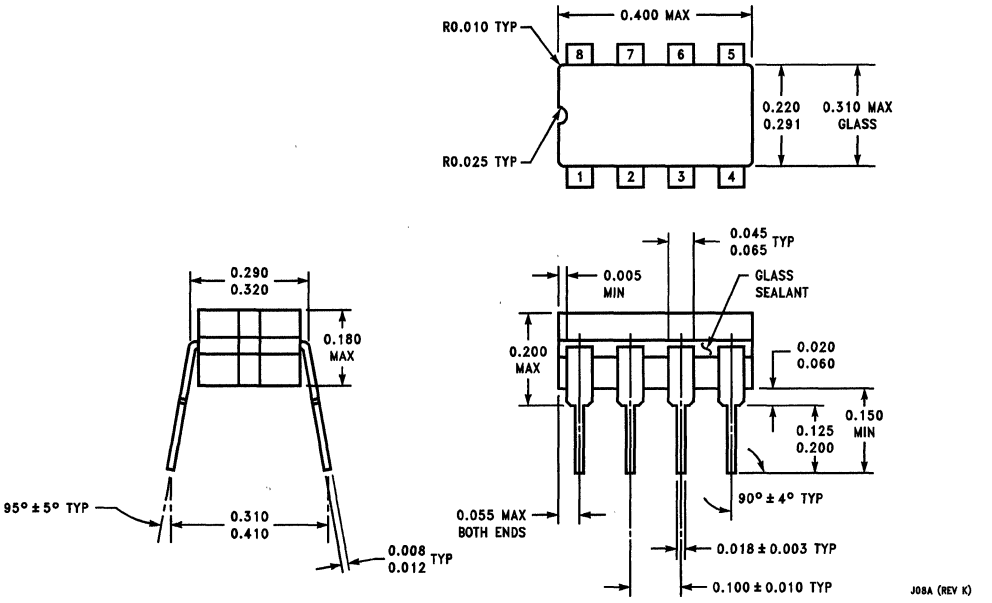
H10C (REV E)

10 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H10F

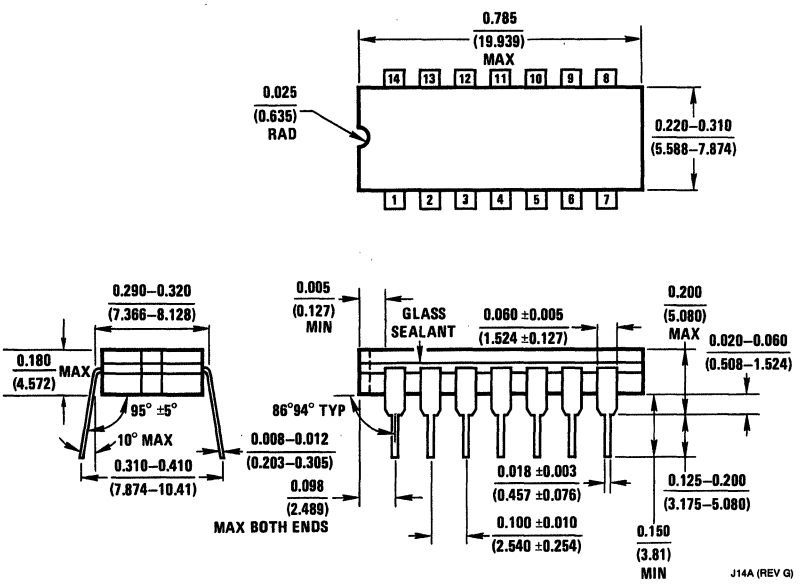


H10F (REV A)

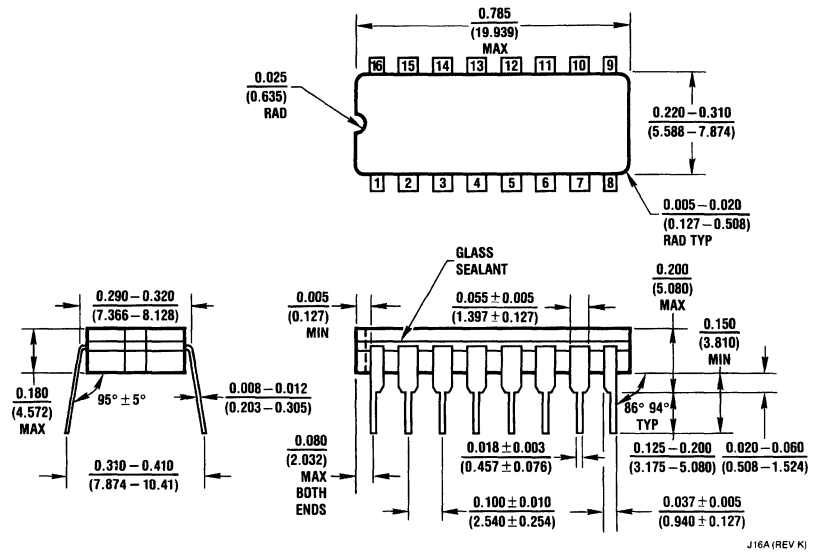
8 Lead Ceramic Dual In-Line Package (J)
NS Package Number J08A



14 Lead Ceramic Dual In-Line Package (J)
NS Package Number J14A

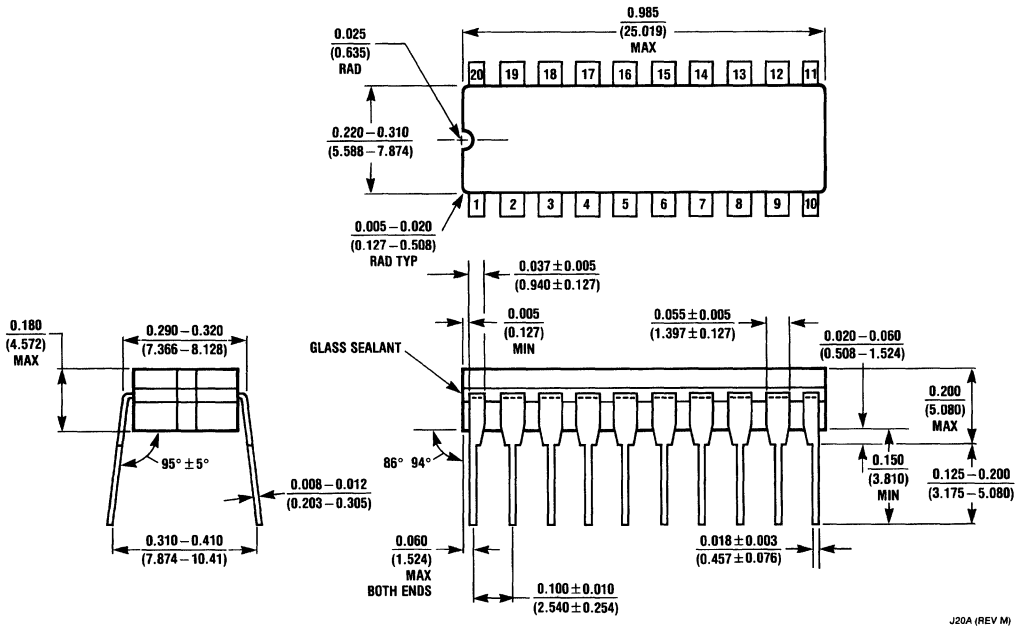


16 Lead Ceramic Dual In-Line Package (J)
NS Package Number J16A



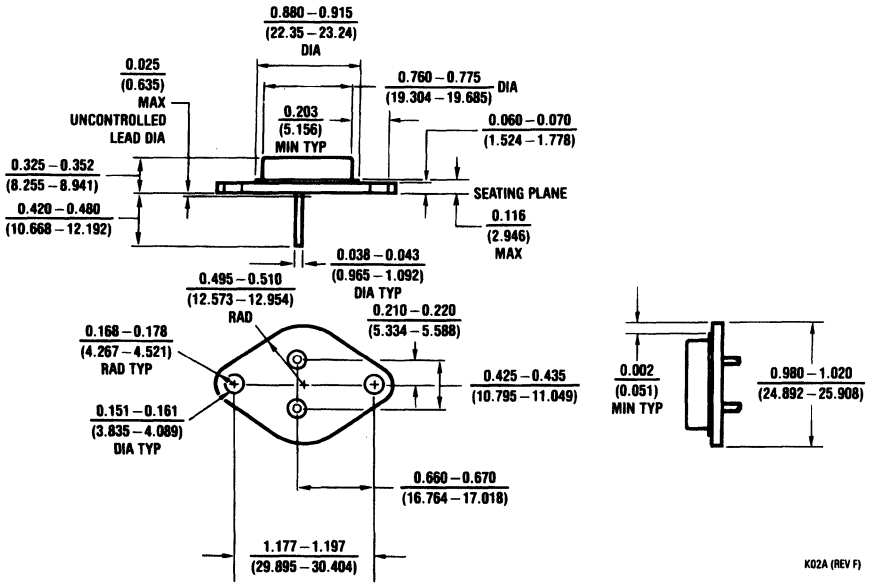
J16A (REV K)

20 Lead Ceramic Dual In-Line Package (J)
NS Package Number J20A

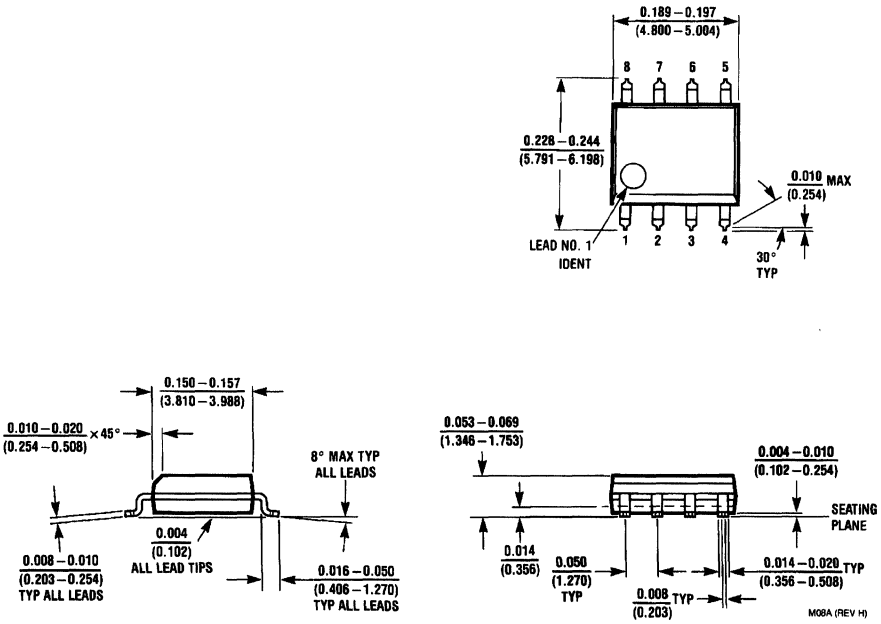


J20A (REV M)

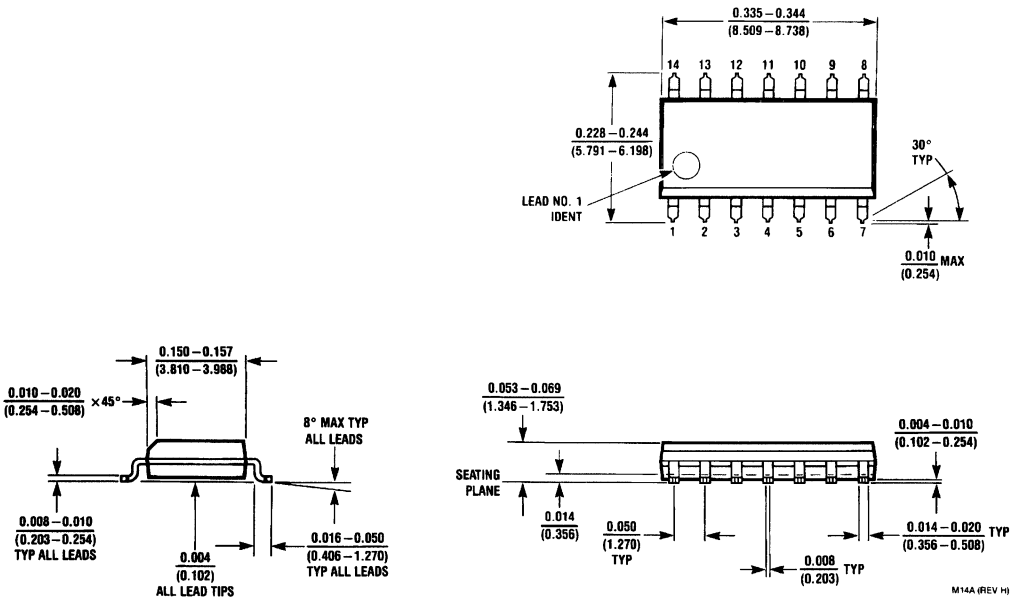
2 Lead TO-3 Metal Can Package (K)
NS Package Number K02A



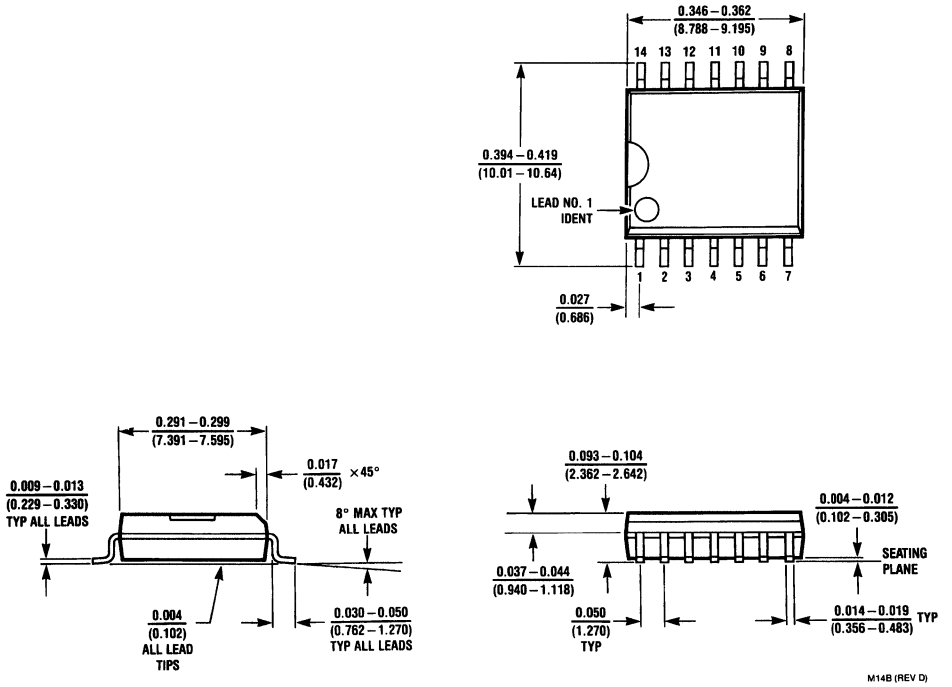
8 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M08A



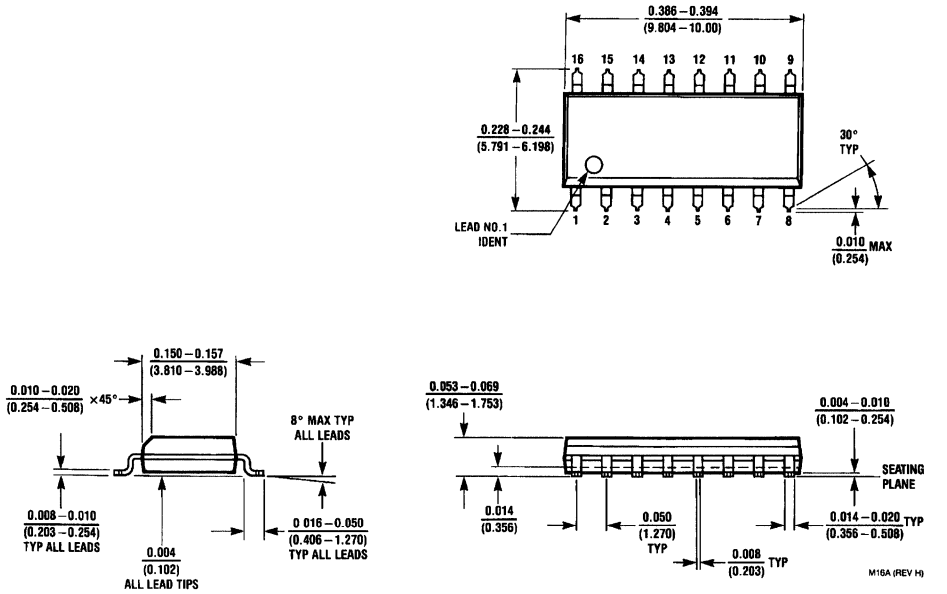
14 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M14A



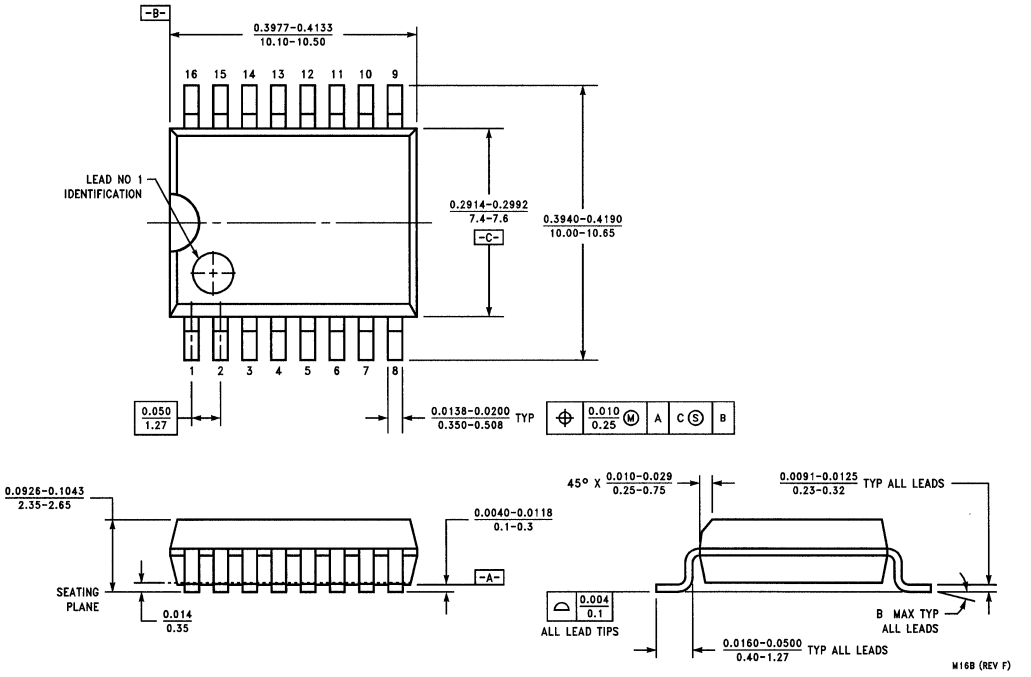
14 Lead (0.300" Wide) Small Outline Molded Package (M)
NS Package Number M14B



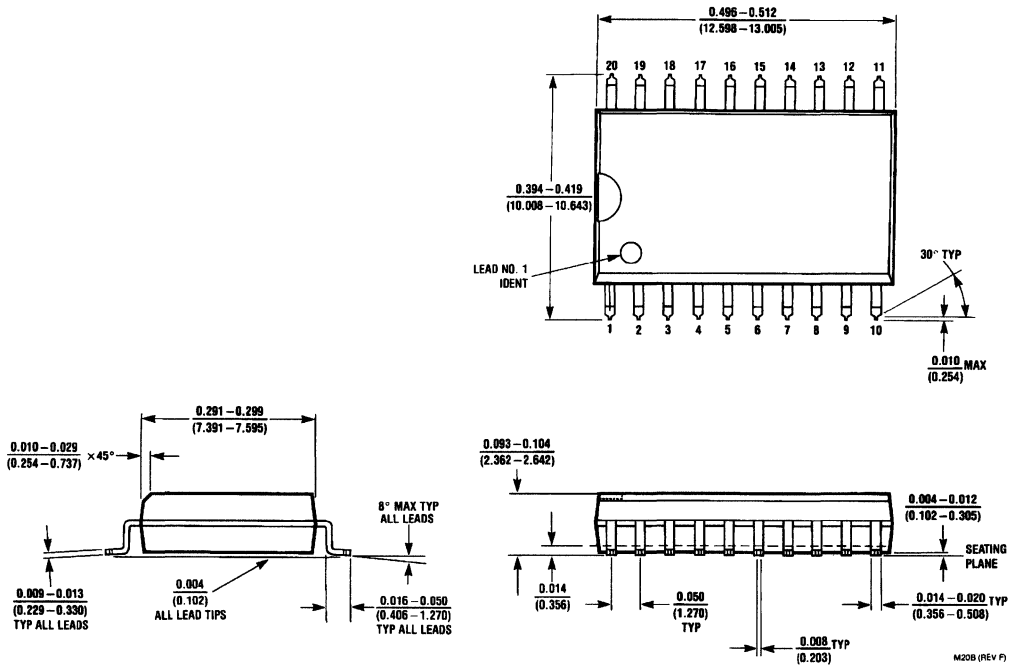
16 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M16A



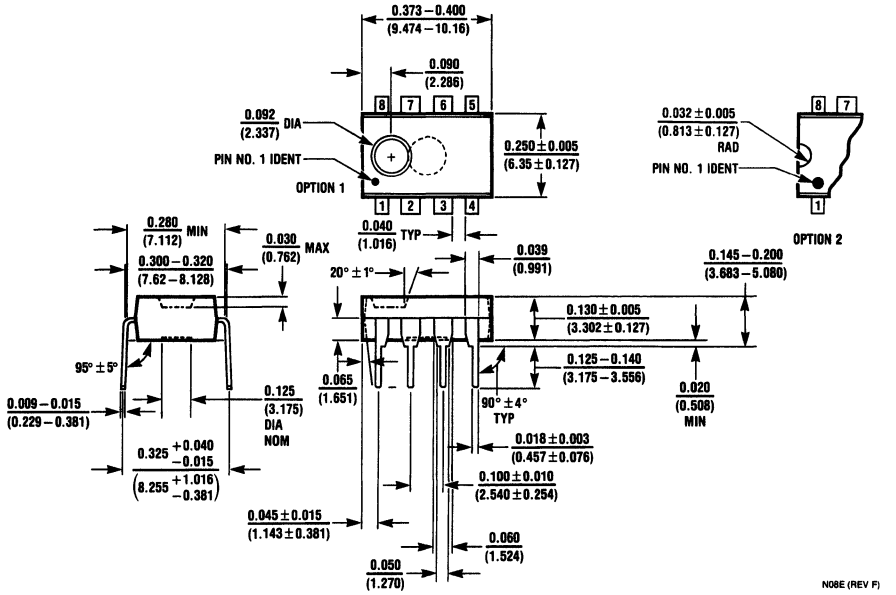
16 Lead (0.300" Wide) Small Outline Molded Package (M)
NS Package Number M16B



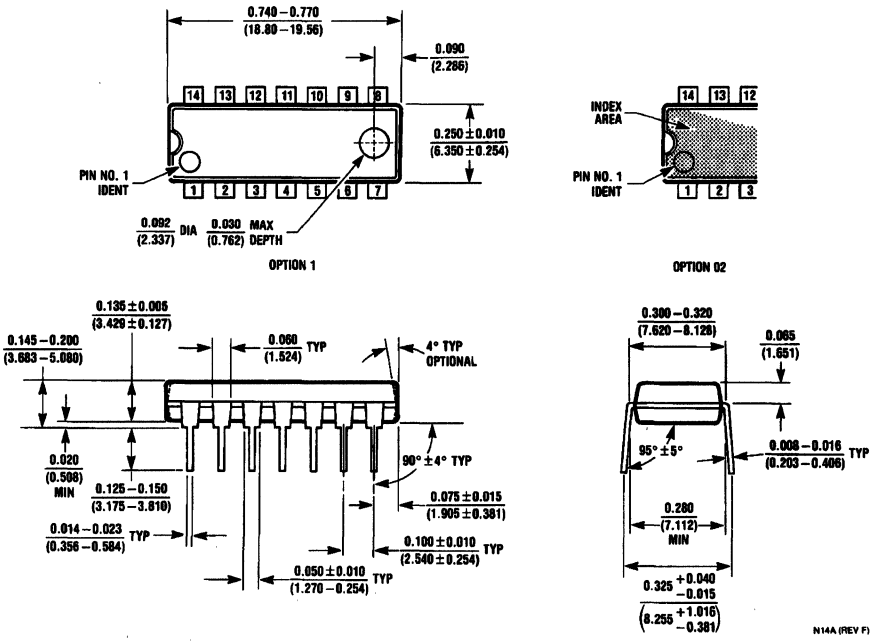
20 Lead (0.300" Wide) Small Outline Molded Package (M)
NS Package Number M20B



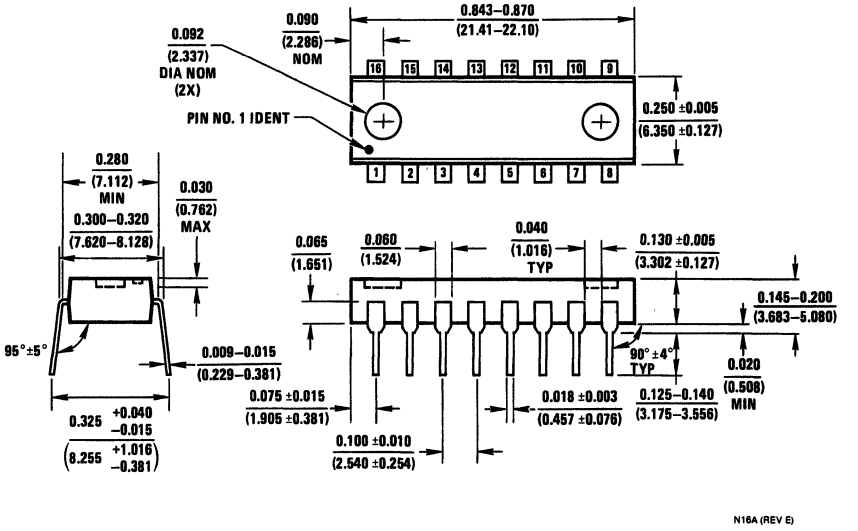
8 Lead Molded Dual In-Line Package (N)
NS Package Number N08E



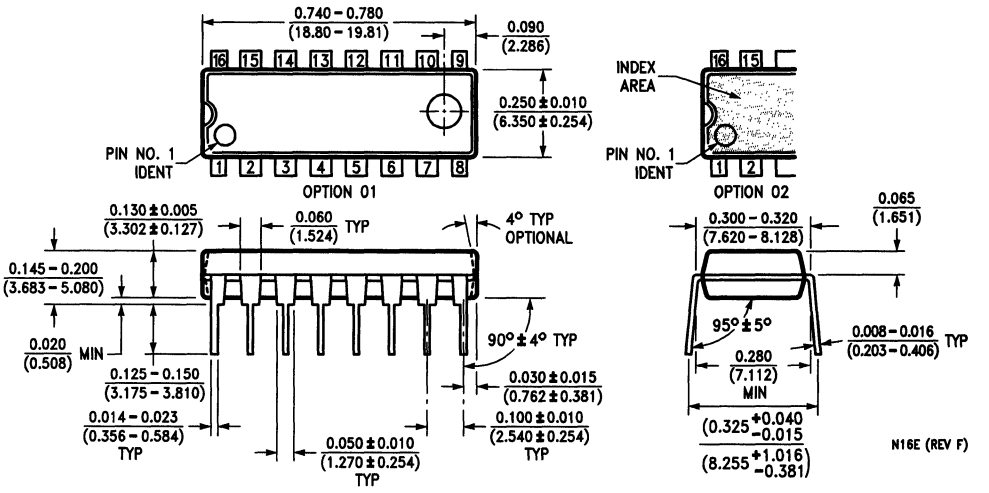
14 Lead Molded Dual In-Line Package (N)
NS Package Number N14A



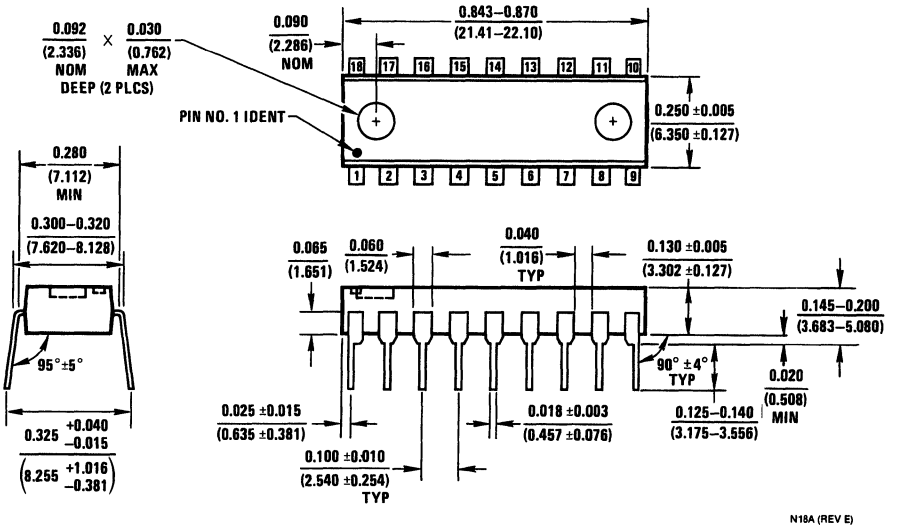
16 Lead Molded Dual In-Line Package (N)
NS Package Number N16A



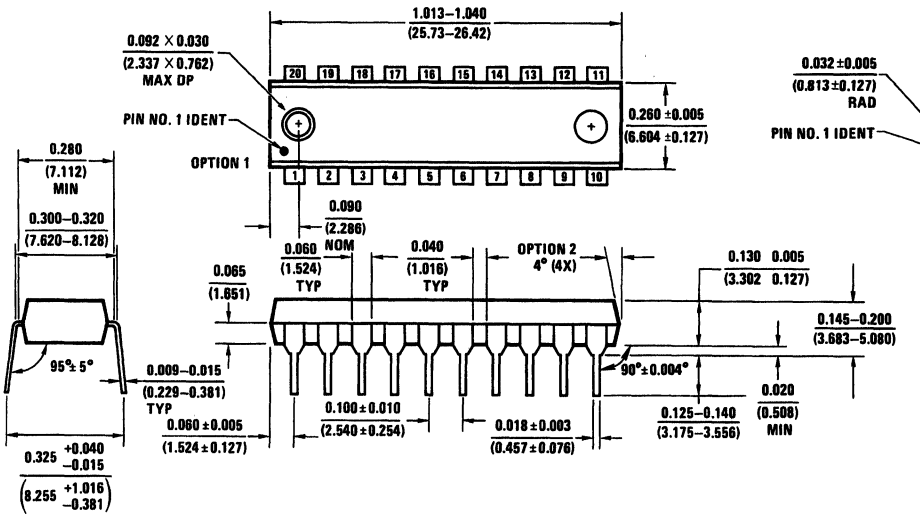
16 Lead Molded Dual In-Line Package (N)
NS Package Number N16E



18 Lead Molded Dual In-Line Package (N)
NS Package Number N18A

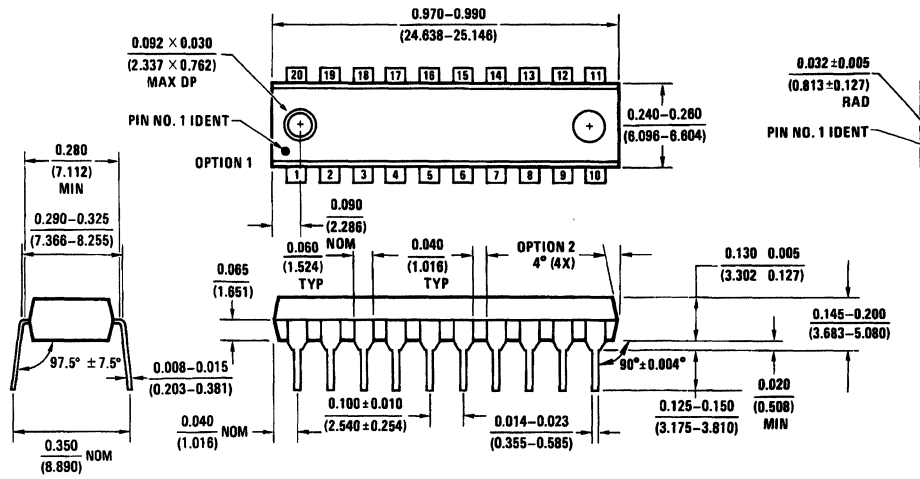


20 Lead Molded Dual In-Line Package (N)
NS Package Number N20A



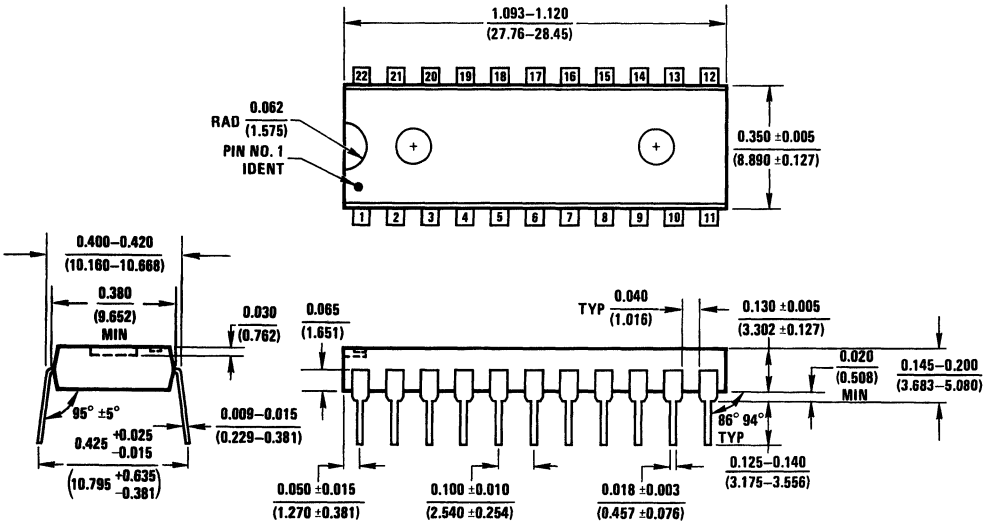
N20A (REV G)

20 Lead Molded Dual In-Line Package (N)
NS Package Number N20B



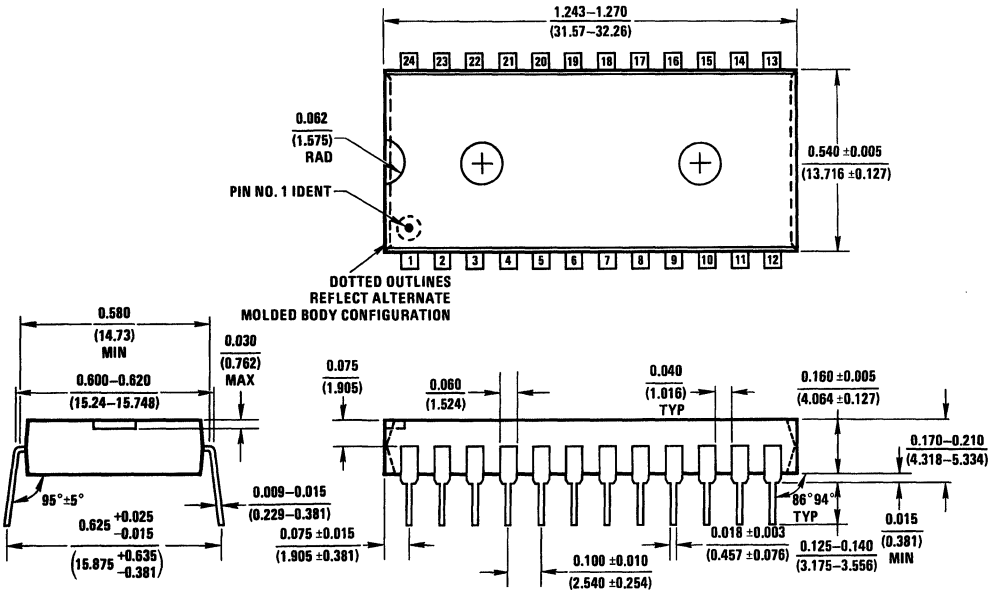
N20B (REV A)

22 Lead Molded Dual In-Line Package (N)
NS Package Number N22A



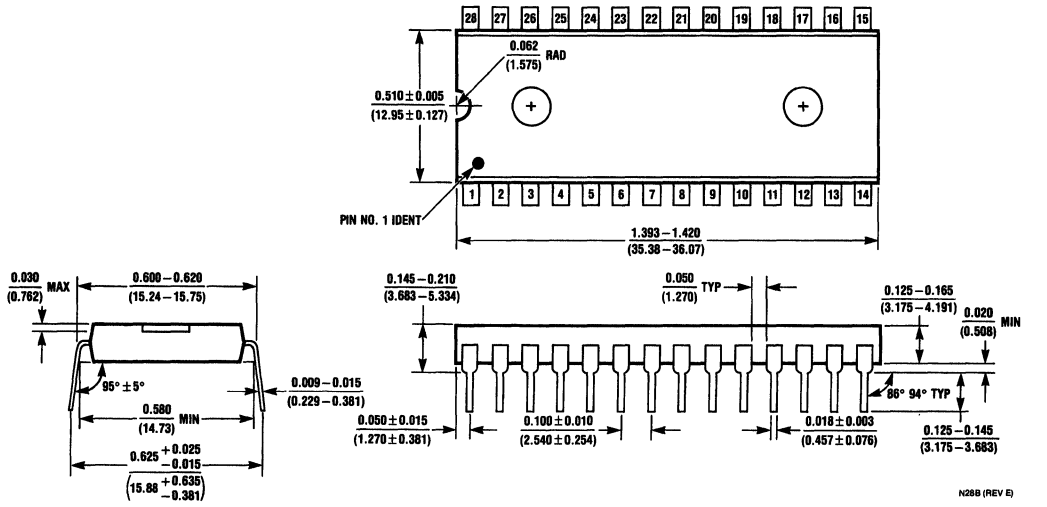
N22A (REV D)

24 Lead Molded Dual In-Line Package (N)
NS Package Number N24A

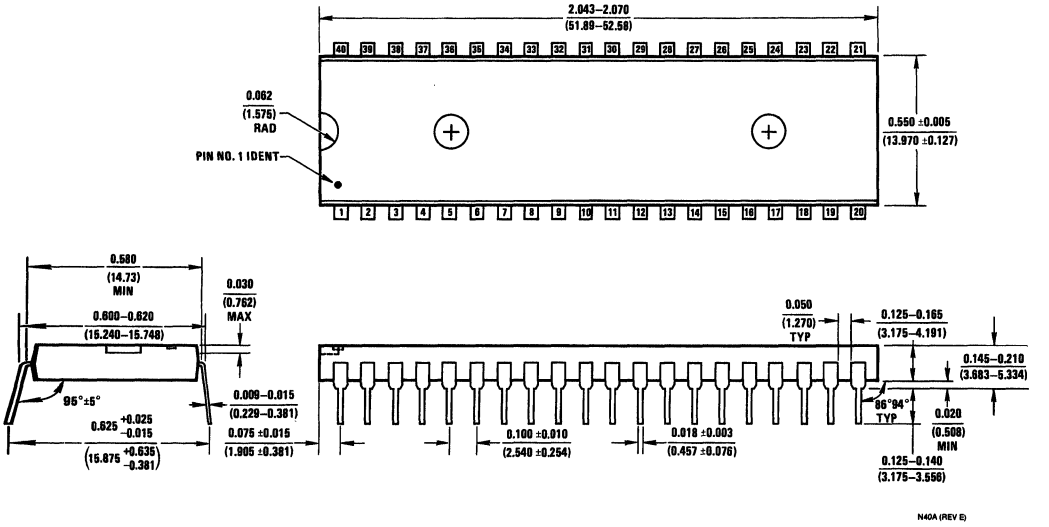


N24A (REV E)

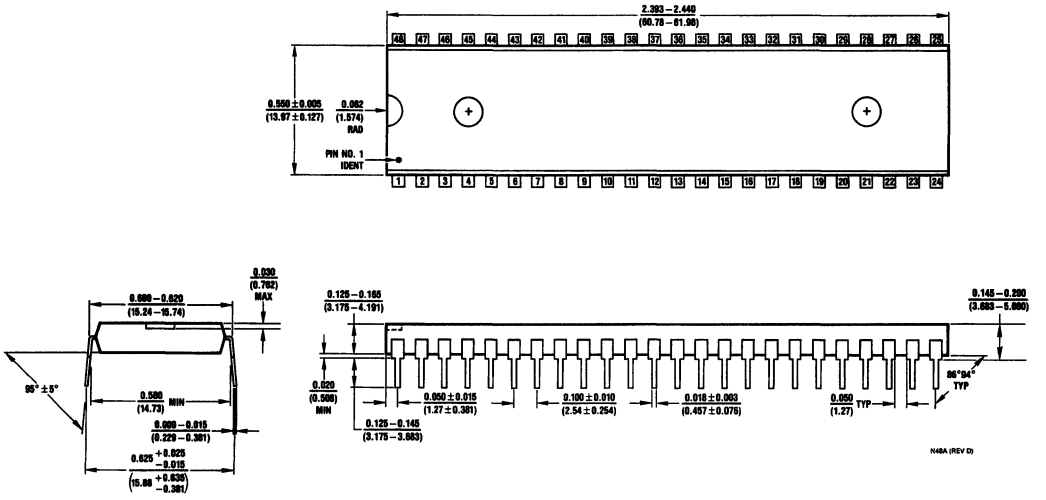
28 Lead Molded Dual In-Line Package (N)
NS Package Number N28B



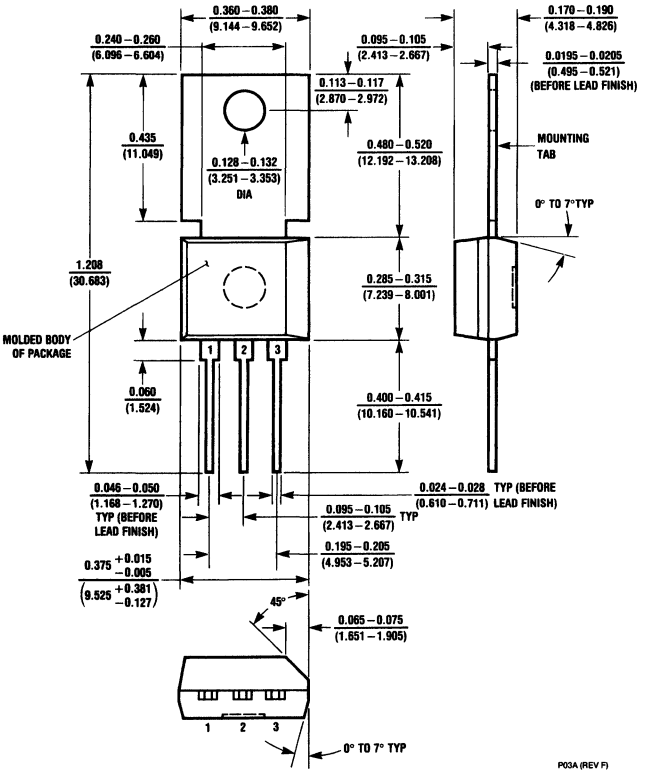
40 Lead Molded Dual In-Line Package (N)
NS Package Number N40A



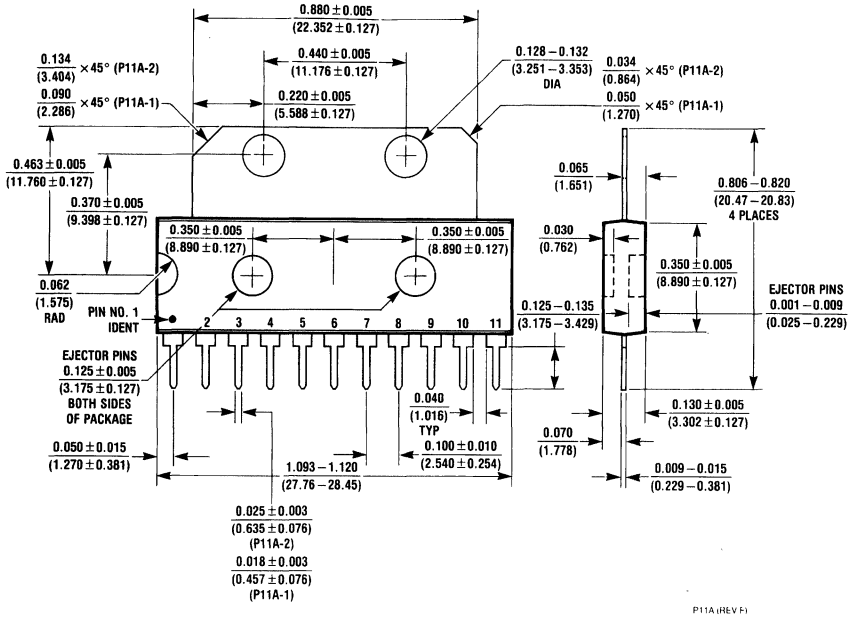
48 Lead Molded Dual In-Line Package (N)
NS Package Number N48A



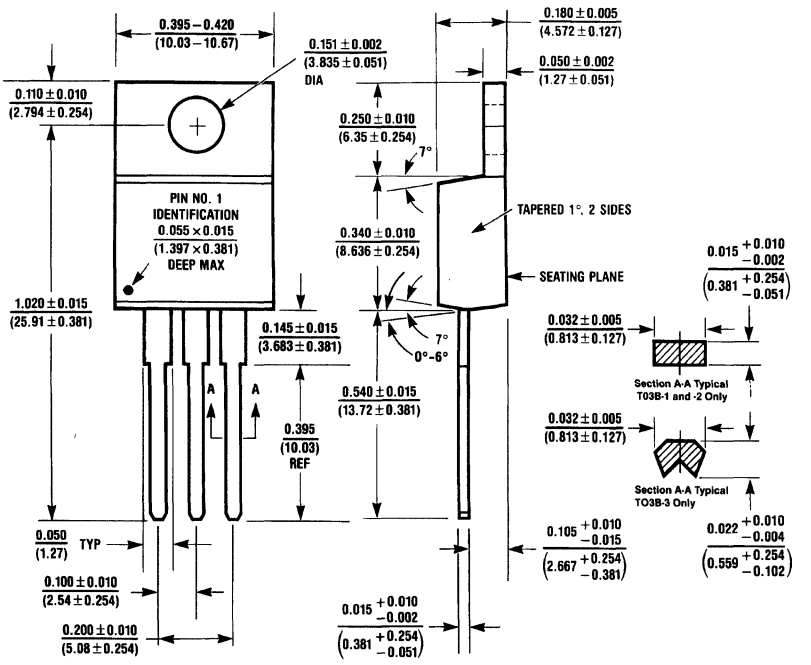
3 Lead TO-202 Molded Package (P)
NS Package Number P03A



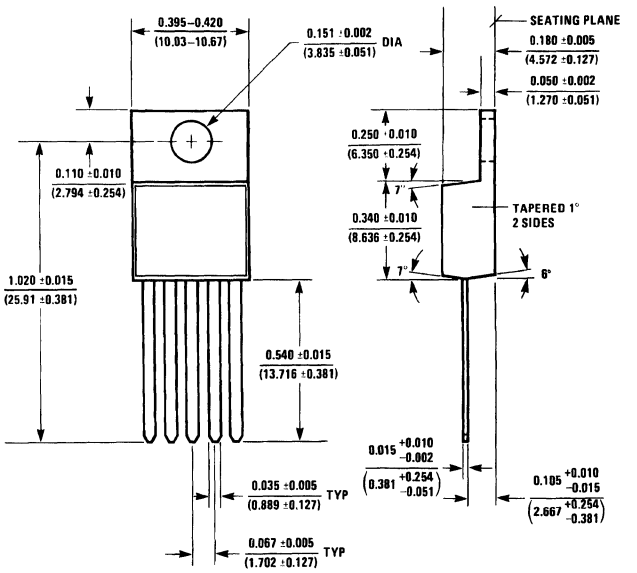
11 Lead Molded Single In-Line Package (P)
NS Package Number P11A



3 Lead TO-220 Molded Package (T)
NS Package Number T03B

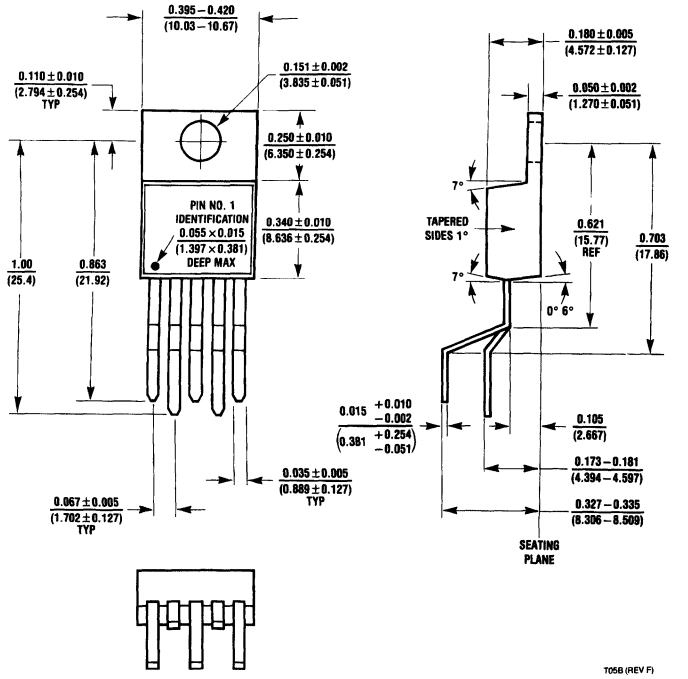


5 Lead TO-220 Molded Package (T)
NS Package Number T05A



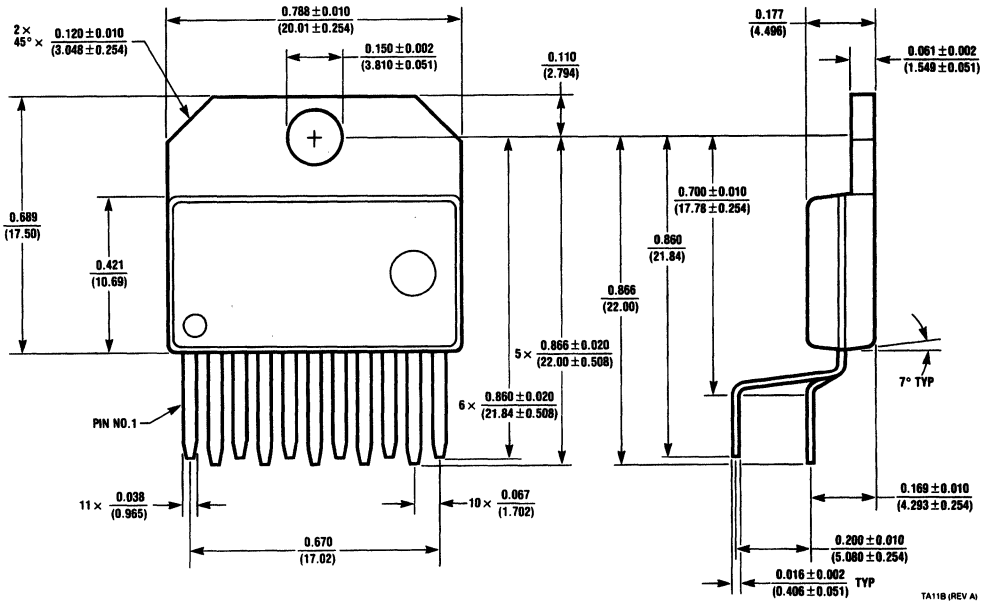
T05A (REV H)

5 Lead TO-220 Molded Package (T)
NS Package Number T05B

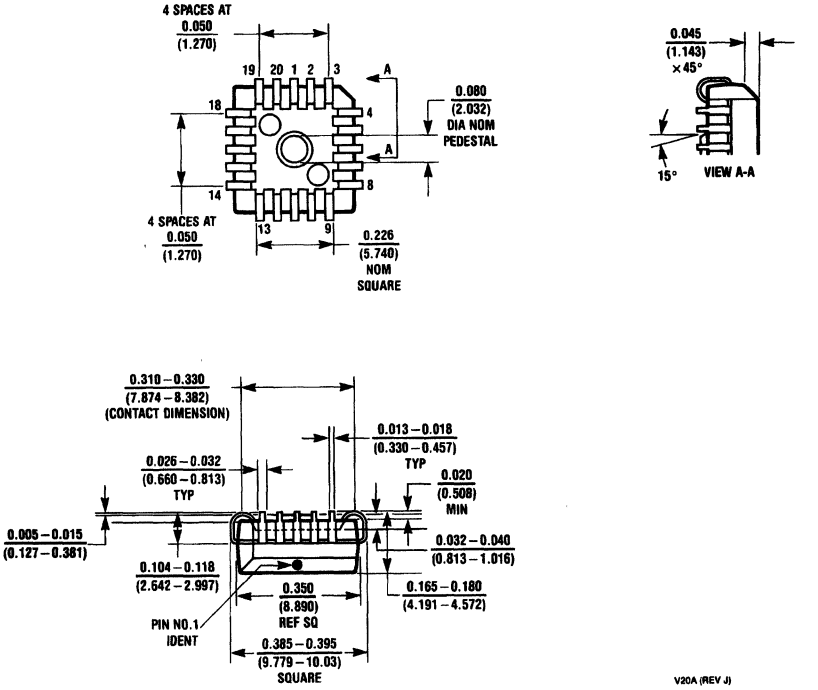


T05B (REV F)

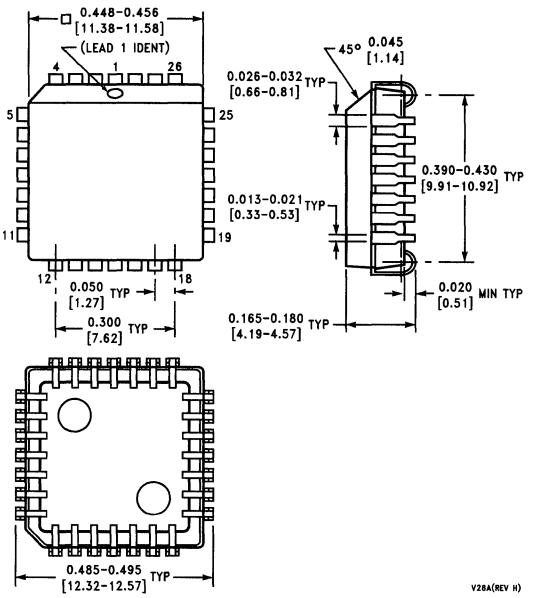
11 Lead TO-220 Molded Package (T)
NS Package Number TA11B



20 Lead Plastic Chip Carrier (PCC)
NS Package Number V20A

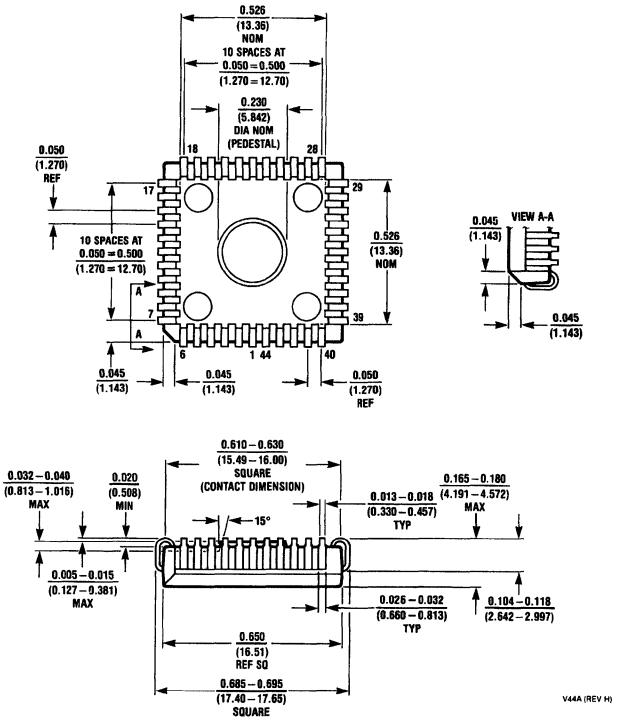


28 Lead Plastic Chip Carrier (PCC)
NS Package Number V28A



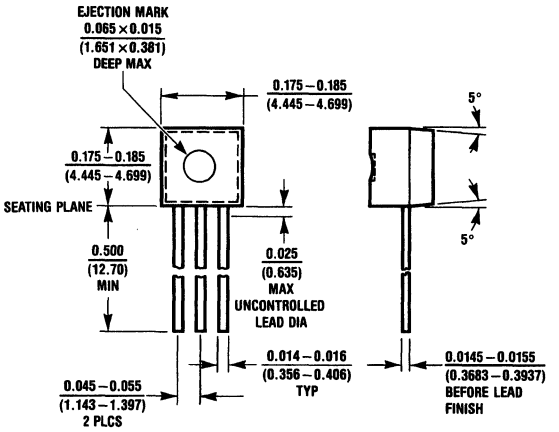
V28A(REV H)

44 Lead Plastic Chip Carrier (PCC)
NS Package Number V44A



V44A (REV H)

3 Lead TO-92 Molded Package (Z)
NS Package Number Z03A



Z03A (REV E)

NOTES

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LINEAR APPLICATIONS HANDBOOK—1991

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

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