580320

National Semiconductor

Clock Generation and Support (CGS™) Design Handbook

CLOCK GENERATION AND SUPPORT

HANDBOOK

1992 Edition

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Clock Generation & Support (CGS™) Family

Introduction

National Semiconductor has developed this handbook to help customers with the design of high-speed clock applications. It contains complete and comprehensive device performance data to assist designers and component engineers in their unique clock distribution applications. Included are skew performance specifications developed by National Semiconductor and discussion of the significance of these specifications as they relate to the end system. Also shown are the Clock Generation and Support (CGS) product's typical and maximum specifications and product functionality and additional characterization data such as power vs frequency, skew performance for unbalanced loads, and derating curves which show the skew performance for balanced output loads across frequency and load. A discussion on clock modeling and its importance in system design along with the required information for modeling is also provided. Finally, criteria for selection is presented with data sheets for National's currently available CGS products.

Clock Generation and Support has become one of the key design areas enabling today's CISC and RISC based systems to obtain maximum operating frequencies. The primary goal of the system clock is to deliver a clock signal to each component's input pins which meets the system's requirements for: signal skew; acceptable waveshape (rise and fall time, overshoot, undershoot, voltage swings), and stability (cycle-to-cycle). The components of clock skew include both intrinsic skew (pin-to-pin skew within a single chip) and extrinsic skew (clock skew generated from trace routing and loading).

National's CGS product strategy is to develop devices to meet customer needs for high speed clock generation and support applications. What CGS offers today is a series of optimal solutions for clock distribution applications requiring devices with high fanout and with guaranteed skew specifications.

For any additional information on device performance or future product availability please contact the National Customer Response Center at 1-800-CRC-9959 or your local sales office.

Table of Contents

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Section 1

Definitions and Test Philosophy

Section 1 Contents

National Semiconductor

Definitions and Test Philosophy

Test Philosophy

Minimizing output skew is a key design criteria in today's high-speed clocking schemes. National has incorporated new skew specifications into the CGS family of devices. National's test philosophy is to fully test guarantee all the available skew specifications in order to help clock designers optimize their clock budgets. In addition to these specifications, National's CGS family also provides extensive bench performance data for skew, rise and fall times, and duty cycle over various output and input conditions in order to provide designers *real-life* performance data.

This section provides general definitions and examples of skew and then discusses National's CGS bench performance methods and examples. The actual performance data can be found in Section 3.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s).

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

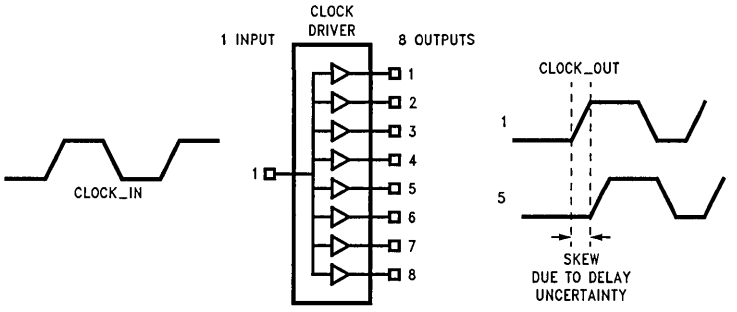

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FIGURE 1-1. Clock Output Skew

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

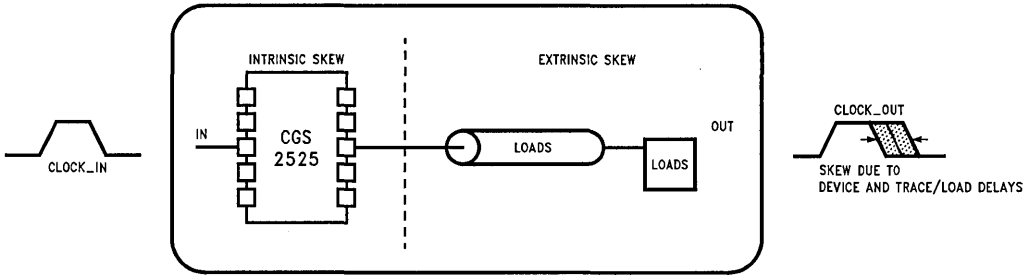

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FIGURE 1-2. Sources of Clock Skew

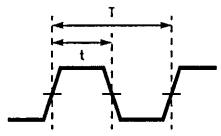
Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles
Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns
If extrinsic skew = 1 ns → − 1 ns
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



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Duty Cycle = t/T * 100%

FIGURE 1-3. Duty Cycle Calculation

Clock Signal

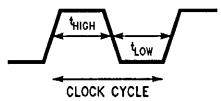

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FIGURE 1-4. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

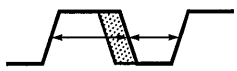

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FIGURE 1-5. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE 1-I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

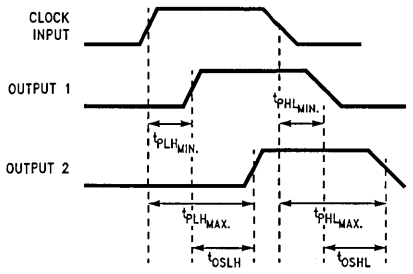

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FIGURE 1-6. t_{OSLH}, t_{OSHL}

TABLE 1-II. Guaranteed Specifications. Useful in applications requiring high fanout drivers with synchronous outputs.

Device	t_{OSHL} or t_{OSLH}	Conditions
CGS74B2525	1 ns	50 pF, 500Ω, 0°C to +70°C, V_{CC} 4.5V to 5.5V
CGS74C2525	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74CT2525	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74C2526	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74CT2526	700 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
100115	75 ps	50Ω, 0°C to +70°C, V_{EE} −4.2V to −4.8V

Definition of Parameters (Continued)

t_{PS} (Pin Skew or Transition Skew)

t_{PS}, describes opposite edge skews, i.e., the difference between the delay of the low-to-high transition and the high-to-low transition on the same pin. This parameter is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. Ideally this number needs to be 0 ns. Effectively, 0 ns means that there is no degradation of the input signal's Duty Cycle.

Many of today's microprocessors require a minimum of a 45:55 percent Duty Cycle. System clock designers typically achieve this in one of two ways. The first method is with an expensive crystal oscillator which meets the 45:55 percent Duty Cycle requirement. An alternative approach is to use a less expensive crystal oscillator and implement a divide by two function. Some microprocessors have addressed this by internally performing the divide by two.

Since Duty Cycle is defined as a percentage, the room for error becomes tighter as the system clock frequency increases. For example in a 25 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 4 ns (t_{PLH} of 18 ns and t_{PLH} of 22 ns) and still meet the Duty Cycle requirement. However for a 50 MHz system clock with a 45:55 percent Duty Cycle requirement, t_{PS} cannot exceed a maximum of 2 ns (t_{PLH} of 9 ns and t_{PHL} of 11 ns) and still meet the Duty Cycle requirement. This analysis assumes a perfect 50:50 percent Duty Cycle input signal.

Definition

t_{PS} (Pin Skew or Transition Skew):

$t_{PS} = |t_{PHL} - t_{PLH}|$

Both high-to-low and low-to-high propagation delays are measured at each output pin across the given device.

Example

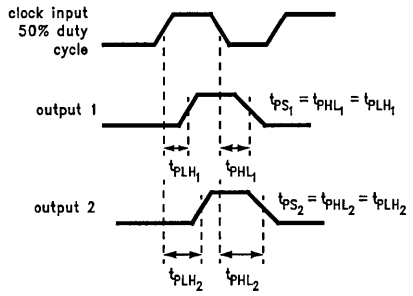

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FIGURE 1-7. t_{PS}

Example: A 33 MHz, 50/50% duty cycle input signal would be degraded by 2.6% due to a t_{PS} = 0.8 ns. (See Table and Illustration below.)

Note: Output symmetry degradation also depends on input duty cycle.

TABLE 1-III. Duty Cycle Degradation of 33 MHz

f (MHz)	Input			Device	Output			% Δ DC Input to Output
	DC Input	t_{IN} (ns)	T_{IN} (ns)	t_{PS} (ns)	t_{OUT} (ns)	T_{OUT} (ns)	DC Output	
33	**50%/50%**	15.15/15.15	30.3	**0.8**	14.35/15.95	30.3	47.4%/52.6%	**2.6%**
	45%/55%	13.6/16.6	30.3	**1.5**	12.1/18.1	30.3	39.9%/60.1%	**5.1%**

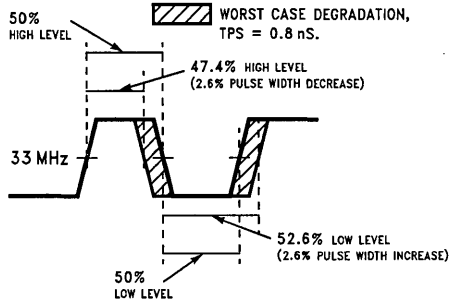

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FIGURE 1-8. Pulse Width Degradation

Definition of Parameters (Continued)

t_{OST} (Opposite Edge Skew)

t_{OST} defines the difference between the fastest and the slowest of both transitions within a given chip. Given a specific system with two components, one being positive-edge triggered and one being negative-edge triggered, t_{OST} helps to calculate the required delay elements if synchronization of the positive- and negative-clock edges is required.

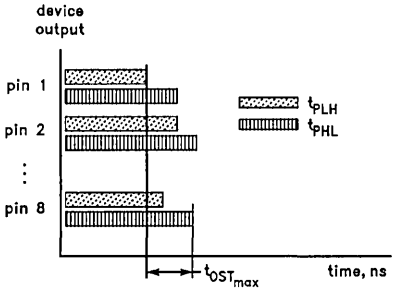

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FIGURE 1-9. t_{OST}

Definition

t_{OST} (Opposite Edge Skew):

$t_{OST} = |t_{P\varphi m} - t_{P\varphi n}|$

where φ is any edge transition (high-to-low or low-to-high) measured between any two outputs (m or n) within any given device.

Example

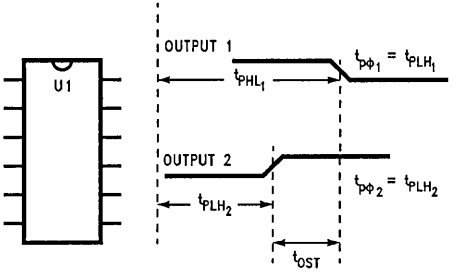

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FIGURE 1-10. t_{OST}

Definition of Parameters (Continued)

t_{PV} (Part Variation Skew)

t_{PV} illustrates the distribution of propagation delays between the outputs of any two devices.

Part-to-part skew, t_{PV}, becomes a critical parameter as the driving scheme becomes more complicated. This usually applies to higher-end systems which go from single clock drivers to distributed clock trees to increase fanout (shown below). In a distributed clock tree, part-to-part skew between U2 and U3 must be minimized to optimize system clock frequency. In the case of the clock tree, the total skew becomes a function of $t_{OSLH/HL}$ of U1 plus t_{PV} of U2 and U3.

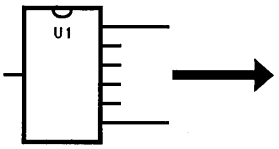

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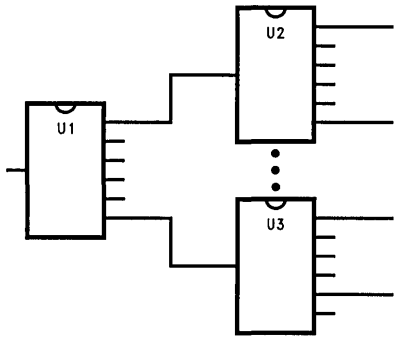
FIGURE 1-11. Clock Distribution

Case 1: Single Clock Driver

Total Skew = Pin-to-Pin Skew U1
= t_{OSLH} or t_{OSHL} of U1



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Case 2: Distributed Clock Tree

Total Skew (U2, U3) = Pin-to-Pin Skew (U1) + Part-to-Part Skew (U2, U3)

Definition

t_{PV} (Part Variation Skew):

$t_{PV} = |t_{P\varphi u,v} - t_{P\varphi x,y}|$

where φ is any edge transition (high-to-low or low-to-high) measured from the outputs of any two devices.

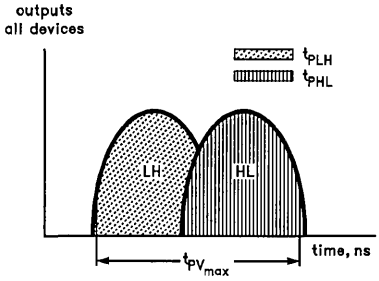

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FIGURE 1-12. t_{PV}

Example

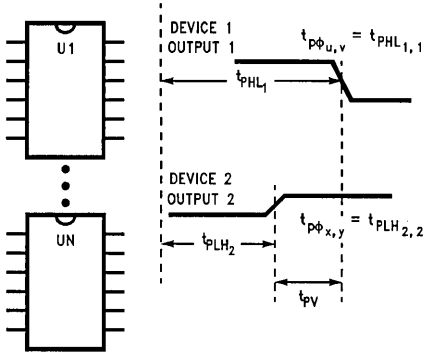

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FIGURE 1-13. t_{PV}

TABLE 1-IV. Guaranteed Specifications

Device	t_{PV}	Conditions
CGS74B2525	1.75 ns	50 pF, 500Ω, 0°C to +70°C, V_{CC} 4.5V to 5.5V
CGS74C2525	3.5 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74CT2525	3.5 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74C2526	3.5 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
CGS74CT2526	3.5 ps	50 pF, 500Ω, 0°C to +85°C, V_{CC} 4.5V to 5.5V
100115	Not Available	50Ω, 0°C to +70°C, V_{EE} −4.2V to −4.8V

The skew specifications offered on National's CGS products were chosen based on system performance demands. The parameters t_{OSHL}, t_{OSLH}, t_{OST}, t_{PS}, and t_{PV} each relate to a specific system requirement which helps designers compensate for pin-to-pin skew, duty cycle degradation, and part-to-part variation.

Section 2

Performance Data

Section 2 Contents

Product Performance Specifications

CGS products are available today in FACT™ (CMOS and TTL compatible CMOS, C2525/26, CT2525/26) and FAST™ LSI (B2525), and F100K Series ECL (100115) technologies. Below is a summary of AC/DC and skew specifications for these CGS products.

DC (STATIC) CHARACTERISTICS

TABLE 2-I. DC Characteristics of CGS Products

V_{CC} Range Oper. Temp.	'B2525 4.5–5.5 0°C–70°C		'C2525 2.0–6.0 0°C–70°C		'CT2525 2.0–6.0 0°C–70°C		100115 −5.7, −4.2 0°C–85°C	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max
V_{IH} (V)	2.0	−1.165	2.75	3.85	1.5	2.0		−1.165
V_{IL} (V)	0.8	−1.810	2.75	1.65	1.5	0.8		−1.810
V_{OH} (V)	2.4	−1.025	5.49	4.86	5.49	4.86		−1.025
V_{OL} (V)	0.5	−1.620	0.01	0.36	0.01	0.36		−1.620
I_{OH} (V)	48	−20.0		24.0		24.0		−20.0
I_{OL} (V)	−64	−6.0		−24.0		−24.0		−6.0

Refer to datasheets for actual conditions.

AC (DYNAMIC) CHARACTERISTICS

TABLE 2-II. AC Characteristics of CGS Products

AC Parameter	'B2525			'C2525			'CT2525			100115		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
t_{PLH} (ns)	2.0	2.9	4.8	2.9	5.0	8.1	4.0	8.5	10.1			0.83
t_{PHL} (ns)	2.0	2.9	4.8	2.9	5.0	8.1	4.0	8.5	10.1			0.83
t_{rise} (ns)		1.3	TBD		1.1			1.1				0.075
t_{fall} (ns)		0.8	TBD		1.1			1.1				0.075

Refer to datasheets for actual conditions.

SKEW PERFORMANCE CHARACTERISTICS

TABLE 2-III. Skew Specification of CGS Products

Skew Parameter	'B2525		'C2525		'CT2525		100115	
	Min	Max	Typ	Max	Typ	Max	Typ	Max
t_{OSLH} (ns)	0.15	1.0	0.2	0.7	0.2	0.7		0.075
t_{OSHL} (ns)	0.15	1.0	0.2	0.7	0.2	0.7		0.075
t_{PS} (ns)	0.6	1.5						
t_{OST} (ns)	0.7	1.5	0.4	1.0	0.4	1.0		
t_{PV} (ns)		1.75		3.5		3.5		0.2

Refer to datasheets for actual conditions.

Characterization Data

Each design has unique characteristics across load and frequency. To help the system designers use National's CGS parts, several derating curves were collected. Data was collected across load and frequency to determine the CMOS and TTL skew performance. This data allows one to compensate for any variations due to loading and frequency on a given product.

The setup used for the data collection included a 3-layer board, using separate layers for ground and V_{CC} to reduce any crosstalk and noise. The signal paths on the PC board were all the same length to minimize any propagation delay differences due to trace lengths. Standard TTL and CMOS loads and inputs were used. Data was collected at room temperature (+25°C) and 5.0V V_{CC}. Below is a simplified diagram of the test jig schematic.

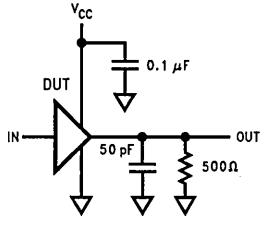

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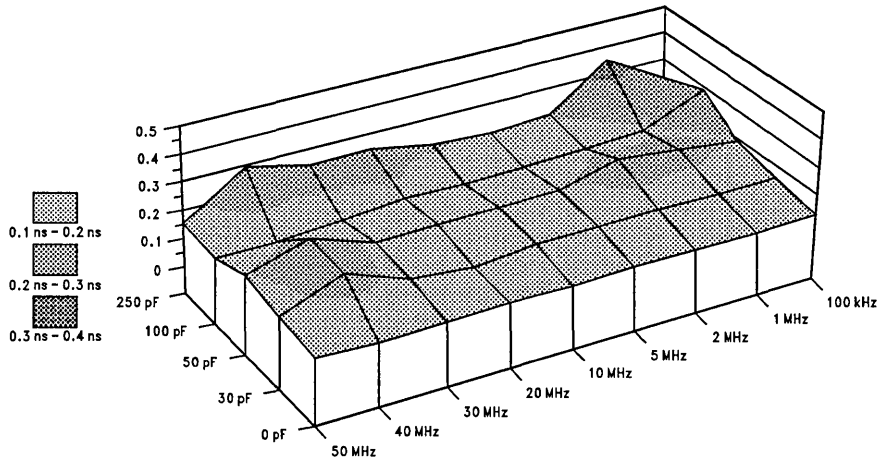
FIGURE 2-1. Test Jig Schematic

EXAMPLE OF A TYPICAL DERATING CURVE

Feature: Pin-to-Pin Output Skew Specification, t_{OSHL}



TL/F/10942–16

FIGURE 2-2. Max t_{OSHL} (ns)

For example, for the CGS74C2525 1 to 8 Clock driver, t_{OSHL} skew performance is observed over frequency (100 kHz to 50 MHz) and capacitive loading (0 pF to 250 pF):

Contour Curve Reading:		**Output Skew:**
at 50 MHz and 30 pF	→	t_{OSHL} is 0.1 ns to 0.2 ns (100 ps to 200 ps)

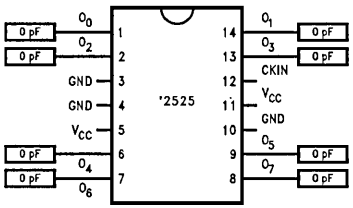
Skew Performance Studies

The performance studies to be described are designed to help system designers use National's CGS devices by providing derating curves observing skew across load and frequency. Data was collected across load and frequency to determine the CMOS and TTL skew performance. This data allows one to compensate for any variations due to loading and frequency on a given CGS product.

Study #1: Skew performance for balanced (matched) loads from 0 pF to 250 pF over 100 kHz to 50 MHz.

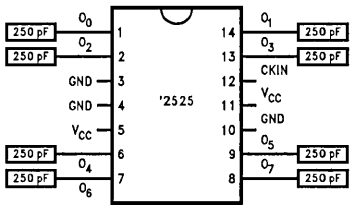
Other conditions: room temperature and 500Ω resistance loads.

This study is intended to observe skew variation with matched capacitive loading across all outputs of the clock driver during multiple output switching at high frequencies. To ensure the integrity of the bench performance study, the data was taken over various sample lots to account for process variations. The data collected is the worst case (maximum skew) performance measured for each of the various skew specifications over balanced loads.



TL/F/10942–72

FIGURE 2-3. Balanced Load 0 pF



TL/F/10942–73

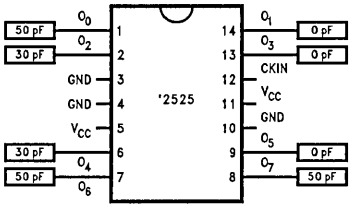
FIGURE 2-4. Balanced Load 250 pF

Refer to the Balanced Load Performance graphs.

Study #2: Skew performance for unbalanced (unmatched) loads from 0 pF to 50 pF over 100 kHz to 50 MHz.

Other conditions: room temperature and 500Ω resistive loads.

This study is indended to observe skew variation with unmatched capacitive loading across all outputs of the clock driver during multiple output switching at high frequencies. To ensure the integrity of the bench performance study, the data was taken over various sample lots to account for process variations. This data is useful to compensate for applications where achieving matched loads is not possible. The data collected is the worst case (maximum skew) performance measured for each of the various skew specifications over unbalanced loads.



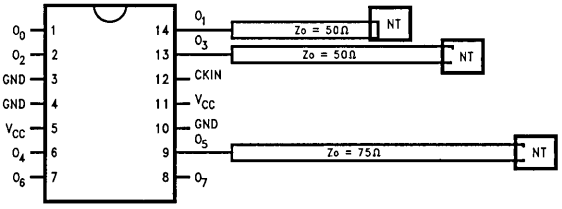
TL/F/10942–74

FIGURE 2-5. Unbalanced Load 0 pF to 50 pF

Refer to the Unbalanced Load Performance graphs.

Study #3: Skew performance for Distributive Loads (Transmission Lines)

This study is intended to provide device information required to perform transmission line simulation of the CGS drivers. Many simulation tools are available today and each has a unique set of information required to perform simulation. In order to create a model for the driver one must know how the driver behaves as its medium changes. That is how parameters such as t_{rise}, t_{fall} along with the output impedance change when board parameters such as length and/or the line's impedance change.

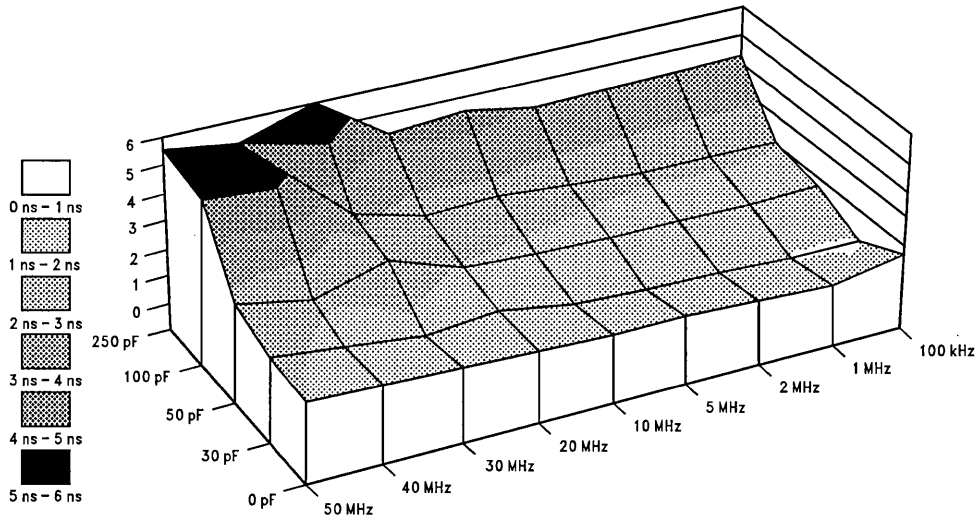


TL/F/10942–75

FIGURE 2-6. Distributive Loads

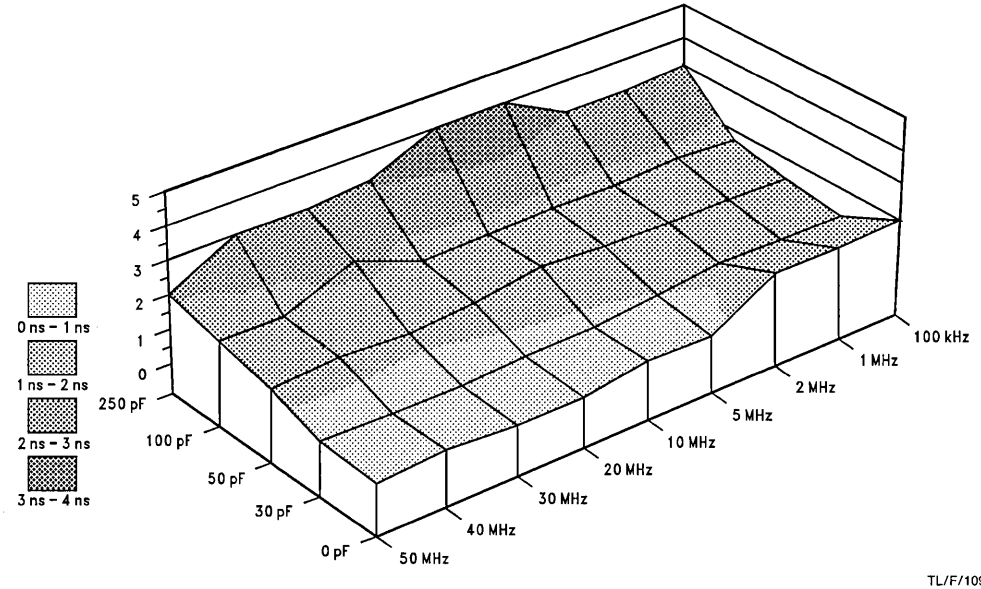
Refer to the Transmission Line graphs.

Balanced Load Performance



TL/F/10942–1

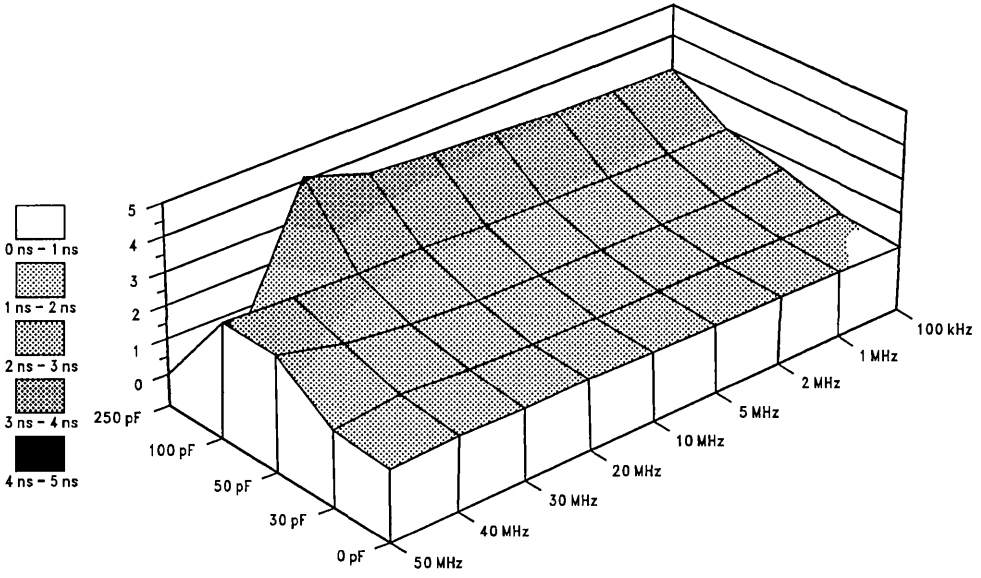
FIGURE 2-7. CGS74B2525 Max t_{rise} (ns)



TL/F/10942–2

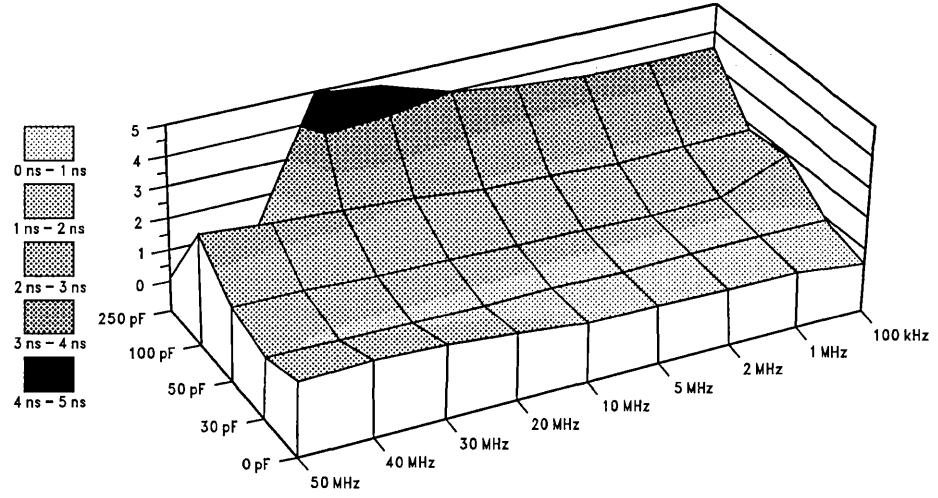
FIGURE 2-8. CGS74B2525 Max t_{fall} (ns)

Balanced Load Performance (Continued)



TL/F/10942–7

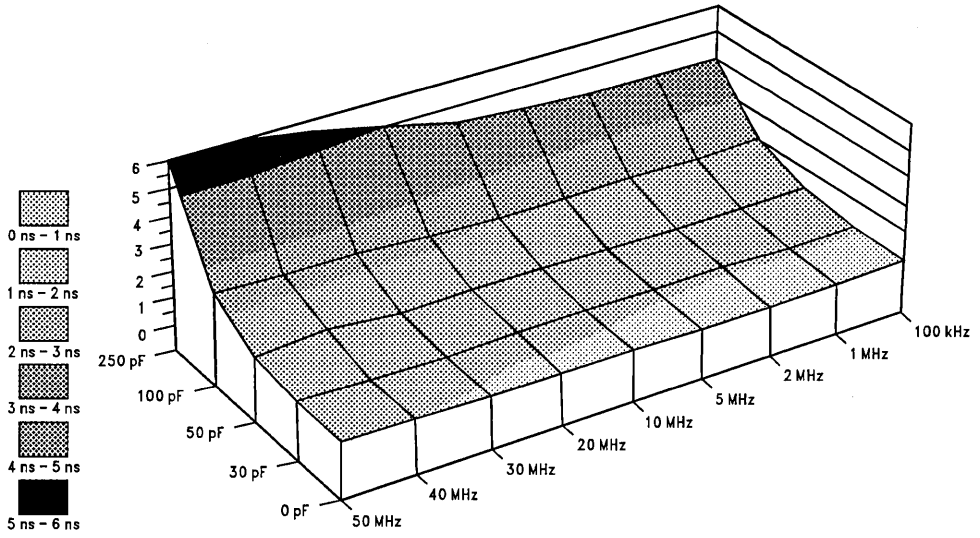
FIGURE 2-9. CGS74CT2525 Max t_{rise} (ns)



TL/F/10942–8

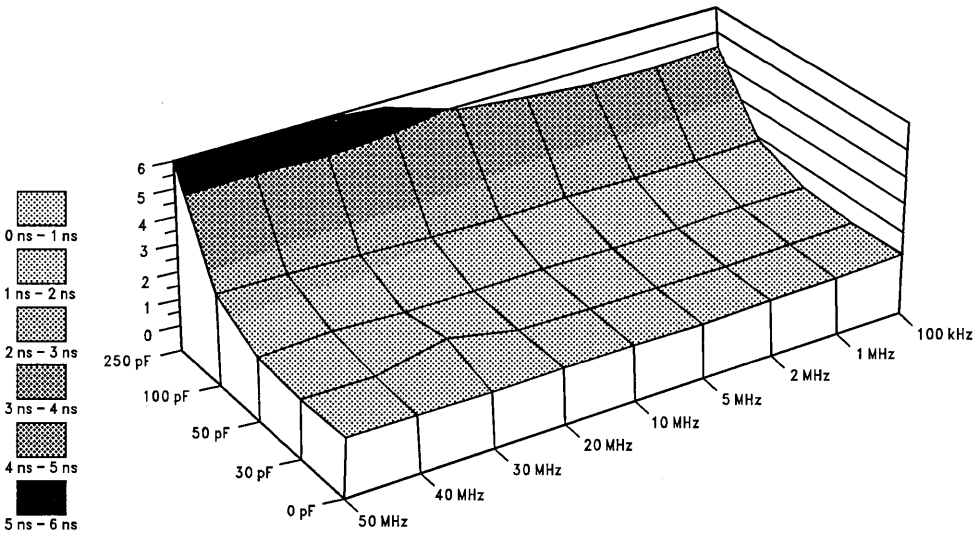
FIGURE 2-10. CGS74CT2525 Max t_{fall} (ns)

Balanced Load Performance (Continued)



TL/F/10942–13

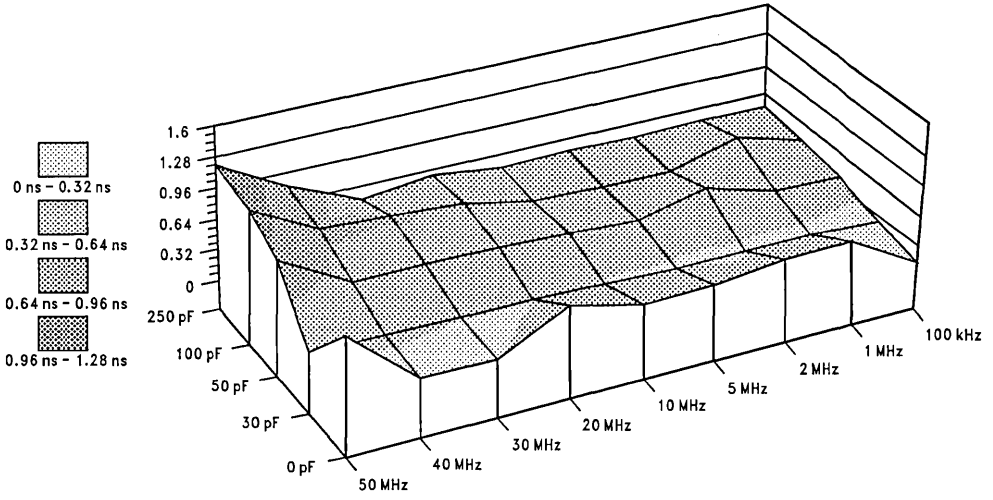
FIGURE 2-11. CGS74C2525 Max t_{rise} (ns)



TL/F/10942–14

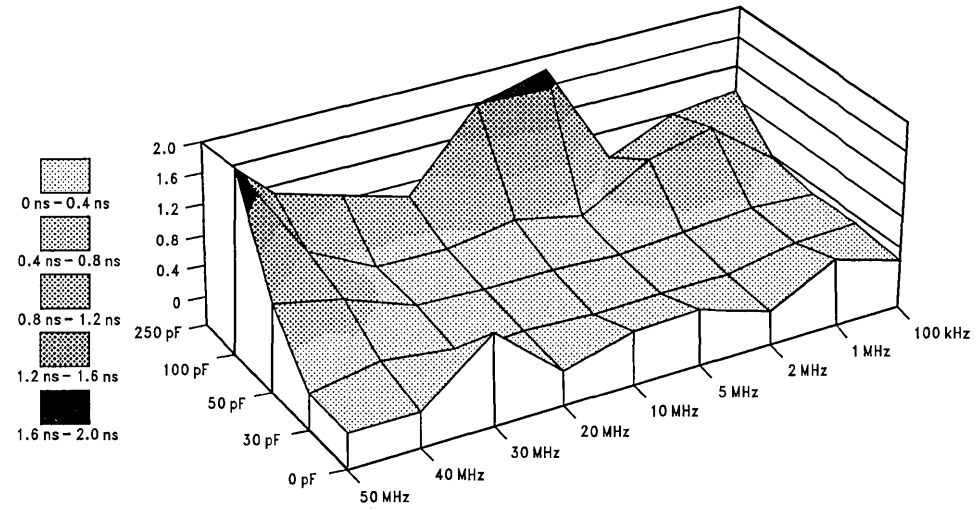
FIGURE 2-12. CGS74C2525 Max t_{fall} (ns)

Balanced Load Performance (Continued)



TL/F/10942–3

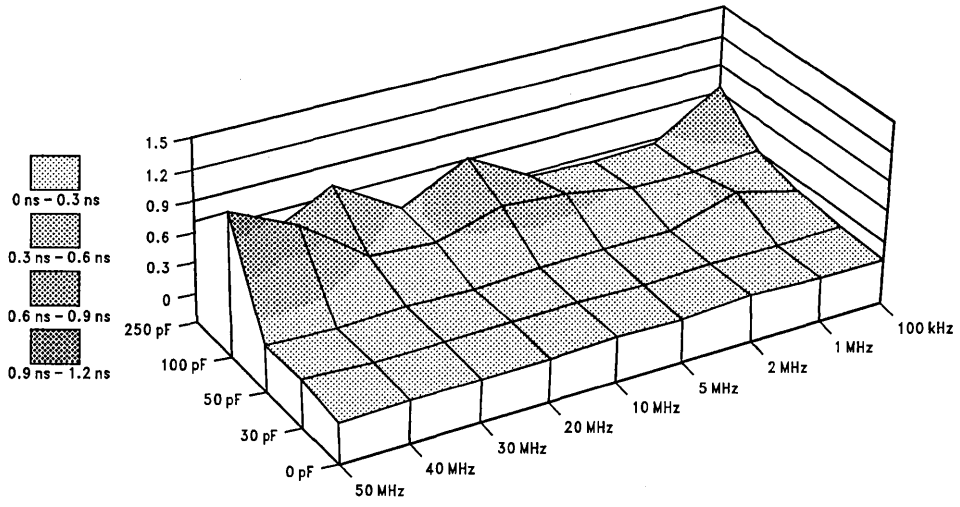
FIGURE 2-13. CGS74B2525 Max t_{OSLH} (ns)



TL/F/10942–4

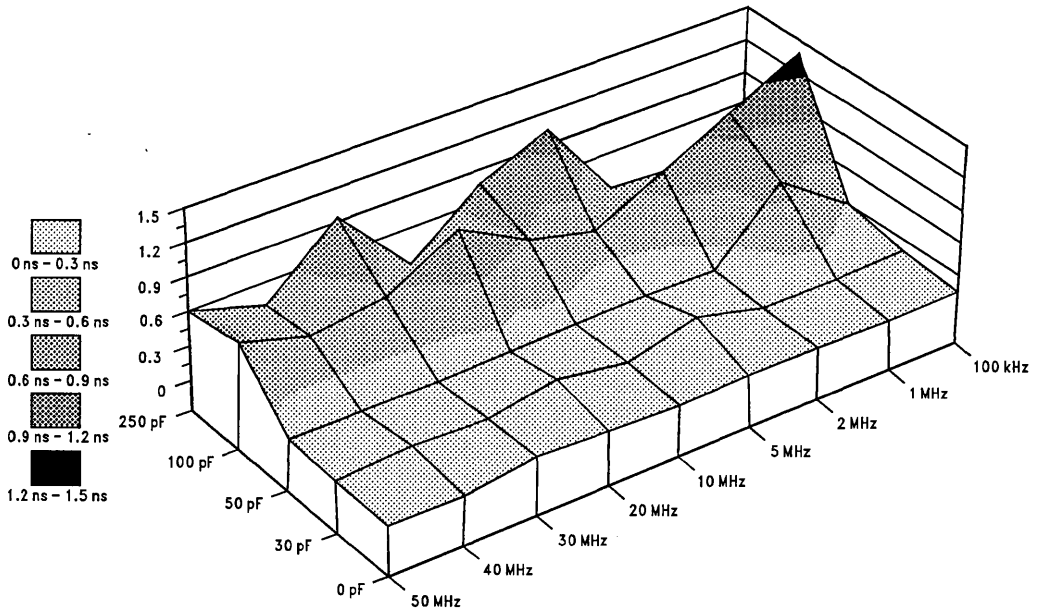
FIGURE 2-14. CGS74B2525 Max t_{OSHL} (ns)

Balanced Load Performance (Continued)



TL/F/10942–9

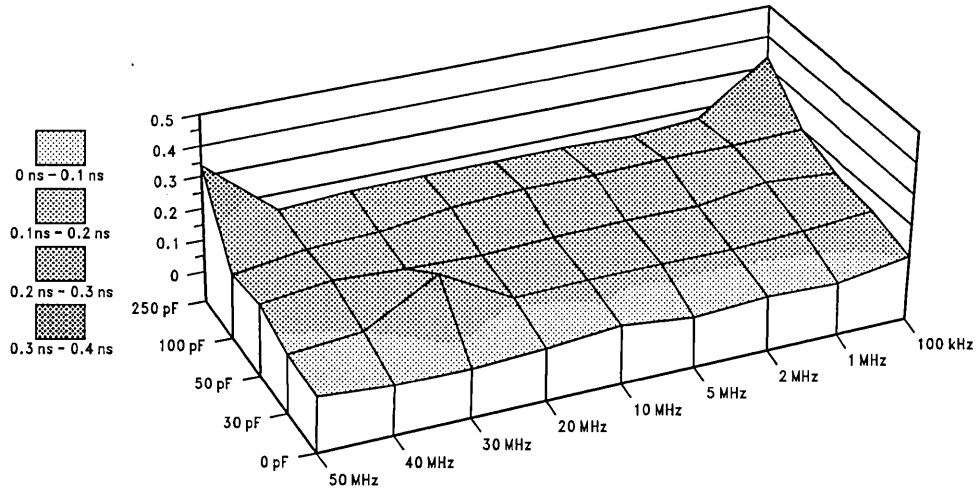
FIGURE 2-15. CGS74CT2525 Max t_{OSLH} (ns)



TL/F/10942–10

FIGURE 2-16. CGS74CT2525 Max t_{OSHL} (ns)

Balanced Load Performance (Continued)



TL/F/10942–15

FIGURE 2-17. CGS74C2525 Max t_{OSLH} (ns)

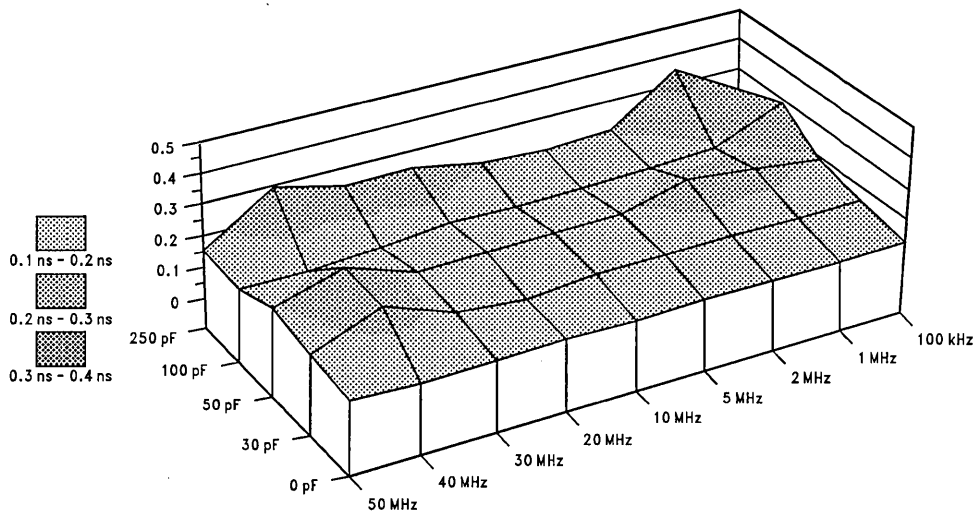


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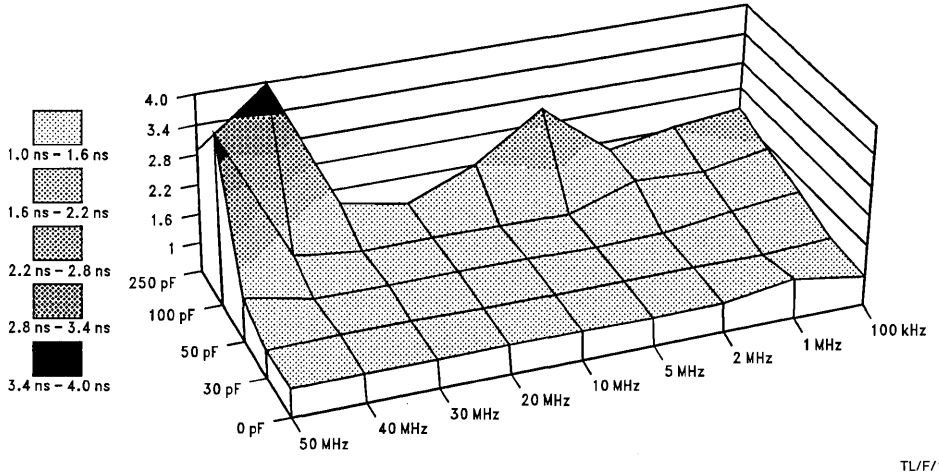
FIGURE 2-18. CGS74C2525 Max t_{OSHL} (ns)

Balanced Load Performance (Continued)



TL/F/10942–5

FIGURE 2-19. CGS74B2525 Max t_{OST} (ns)

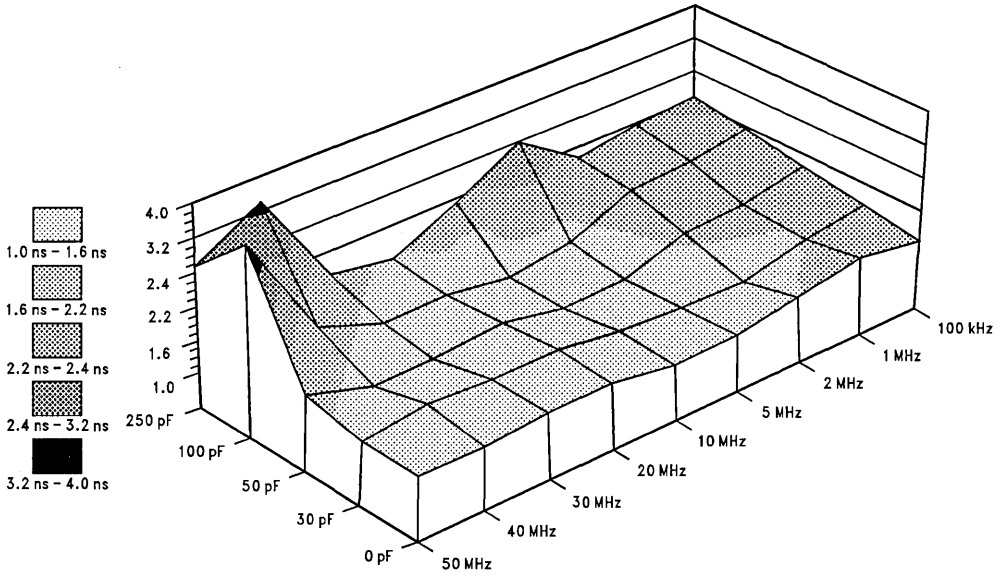


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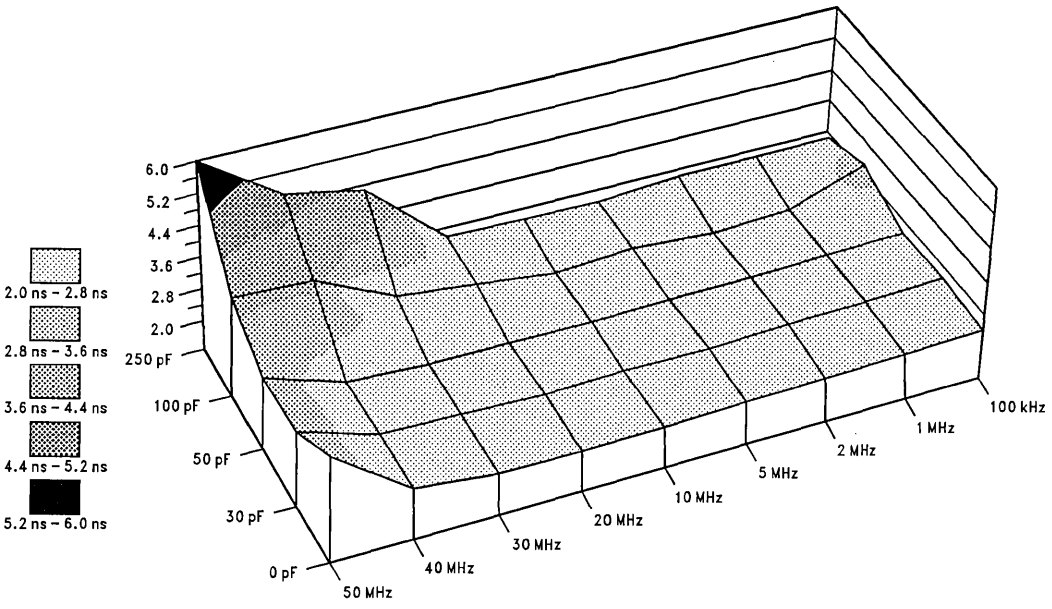
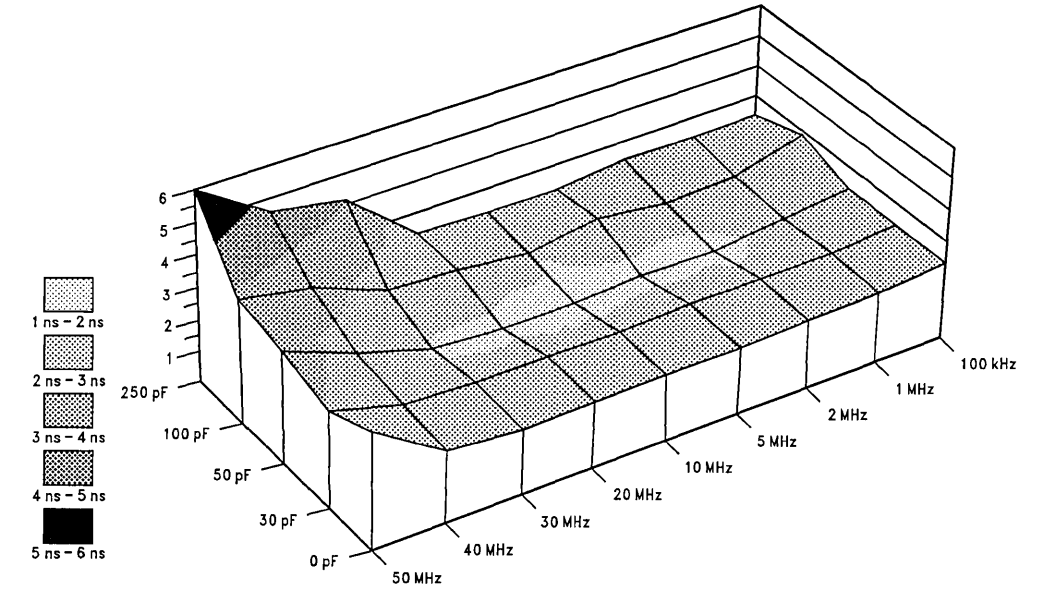
FIGURE 2-20. CGS74B2525 Max t_{PS} (ns)

Balanced Load Performance (Continued)



TL/F/10942–11

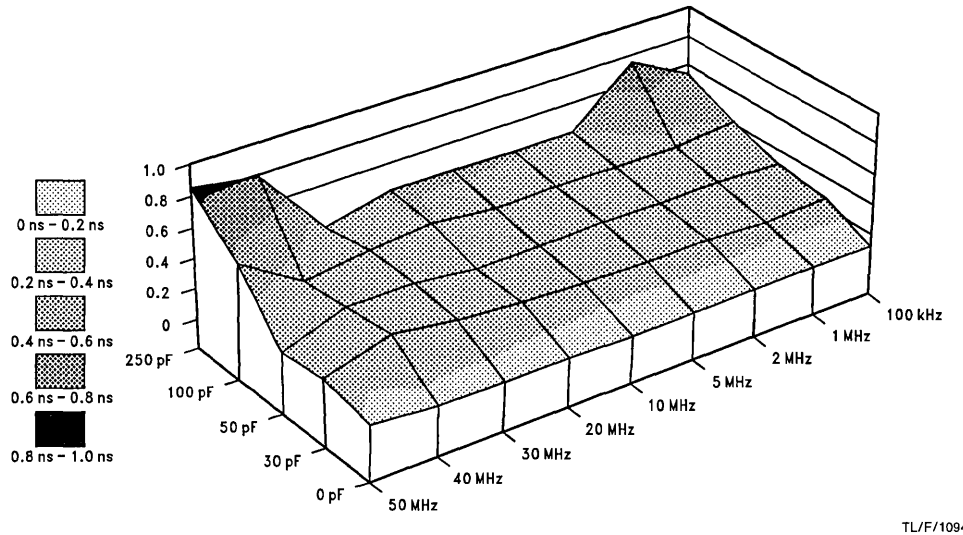
FIGURE 2-21. CGS74CT2525 Max t_{OST} (ns)



TL/F/10942–12

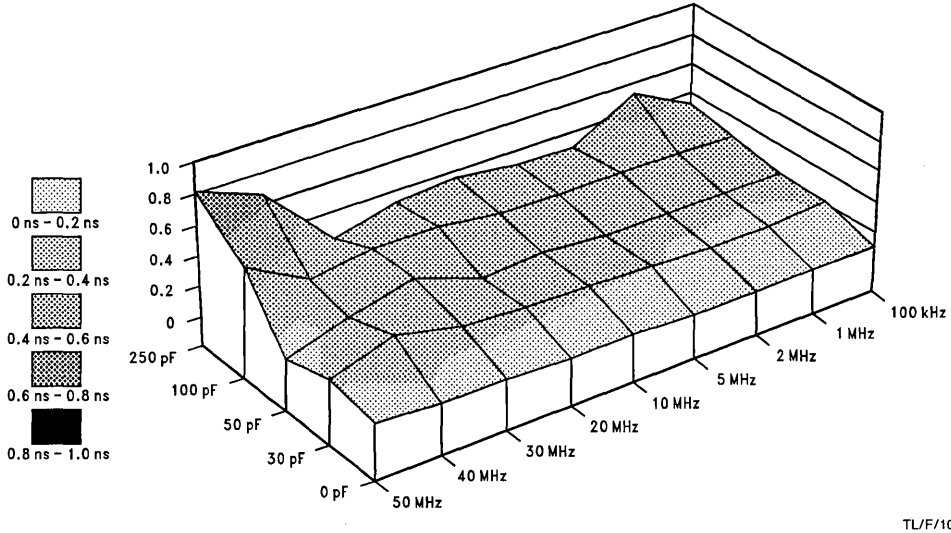
FIGURE 2-22. CGS74CT2525 Max t_{PS} (ns)

Balanced Load Performance (Continued)



TL/F/10942–17

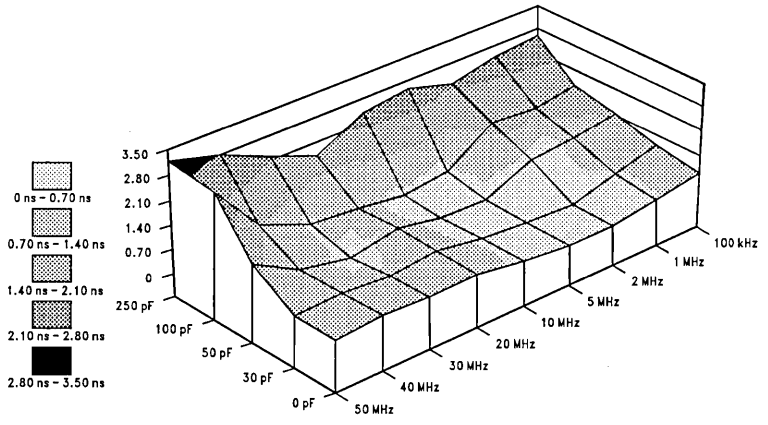
FIGURE 2-23. CGS74C2525 Max t_{OST} (ns)



TL/F/10942–18

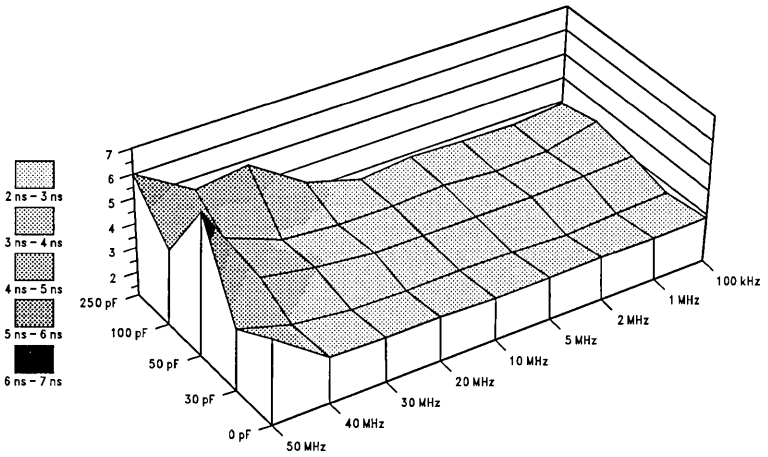
FIGURE 2-24. CGS74C2525 Max t_{PS} (ns)

Balanced Load Performance (Continued)



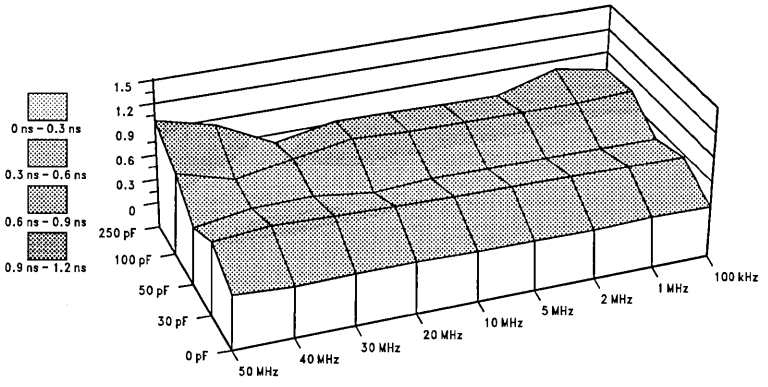
TL/F/10942–19

FIGURE 2-25. CGS74B2525 Max t_{PV} (ns)



TL/F/10942–20

FIGURE 2-26. CGS74CT2525 Max t_{PV} (ns)



TL/F/10942–21

FIGURE 2-27. CGS74C2525 Max t_{PV} (ns)

Unbalanced Load Performance

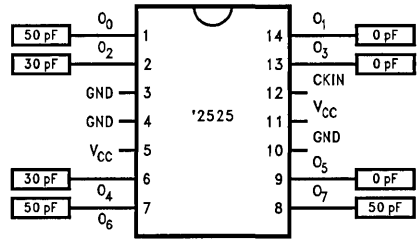
In many instances, no matter how much one tries to balance the loads across the outputs of the driver, there will be a slight imbalance. This imbalance will impact output rise/fall and propagation delay times which, in turn, impacts skew across the outputs. The graphs below show worst-case skew, given unbalanced loads of 0 pF to 50 pF across all eight outputs. This data was collected by placing the least amount of load on the fastest output (0 pF) and the heaviest load on the slowest output (50 pF). Data was collected at 5.0V supply voltage and at room temperature (+25°C).

Feature: Skew Performance Data over unbalanced (unmatched) loads.

Example: Unbalanced Load Performance

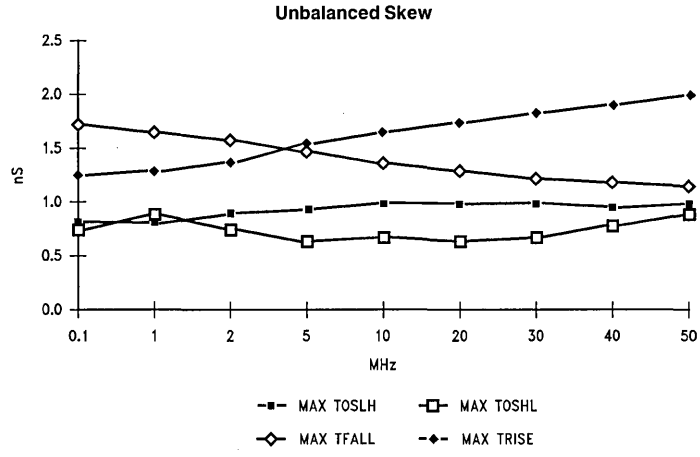
0 pF to 50 pF unmatched loads placed on driver outputs, 5V, room temp, 3 process lots.

Note: The following example is for illustration only. It is not the actual loading configuration for worst case conditions.

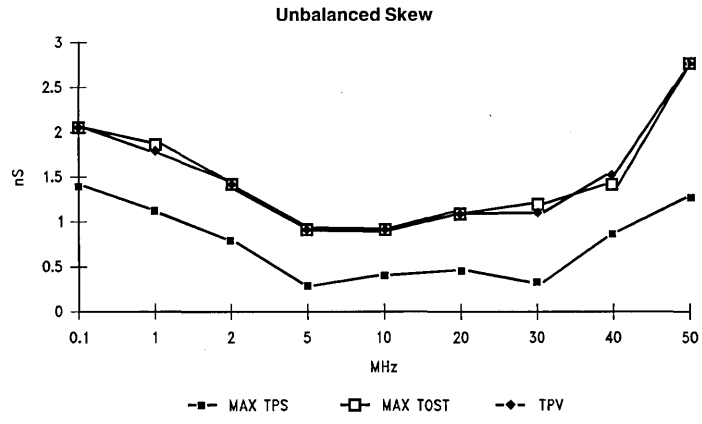


TL/F/10942–82

FIGURE 2-28. Unbalanced Loads



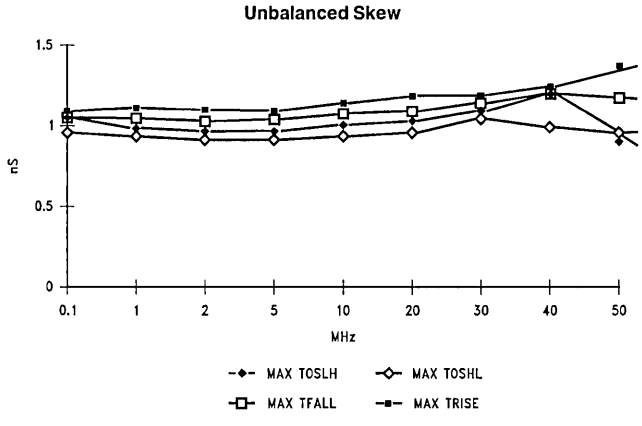
TL/F/10942–76



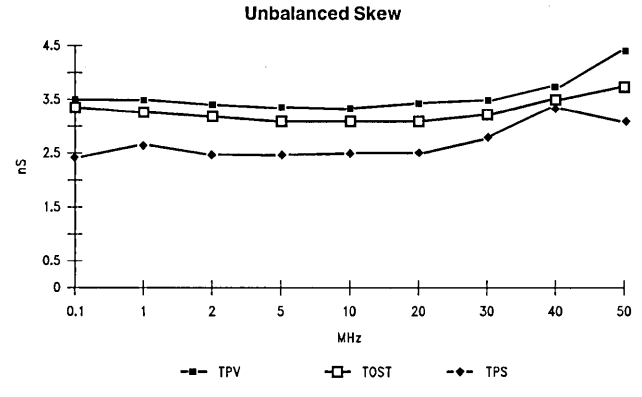
TL/F/10942–77

FIGURE 2-29. 'B2525 Unbalanced Load Skew Performance

Unbalanced Load Performance (Continued)

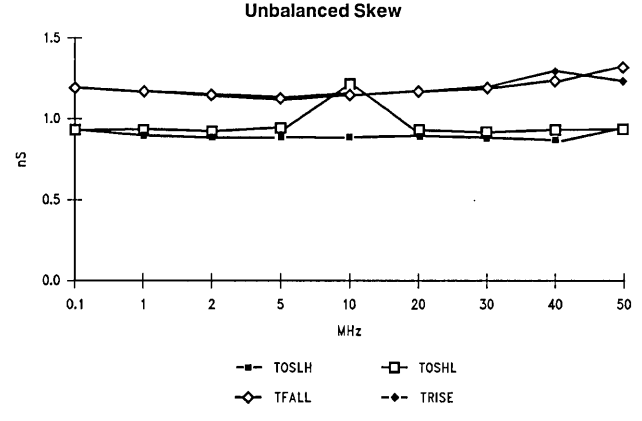


TL/F/10942–78



TL/F/10942–79

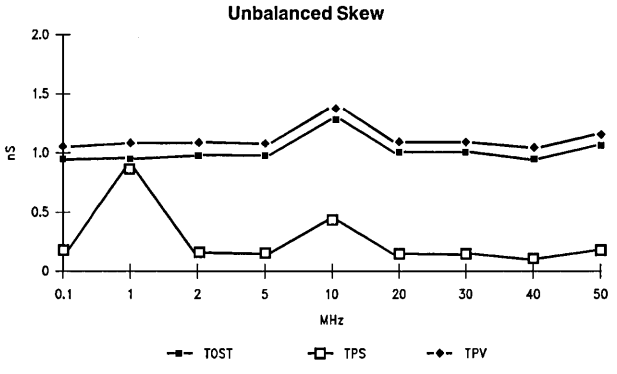
FIGURE 2-30. 'CT2525 Unbalanced Load Skew Performance



TL/F/10942–80

FIGURE 2-31. 'C2525 Unbalanced Load Skew Performance

Unbalanced Load Performance (Continued)



TL/F/10942–81

FIGURE 2-31. 'C2525 Unbalanced Load Skew Performance (Continued)

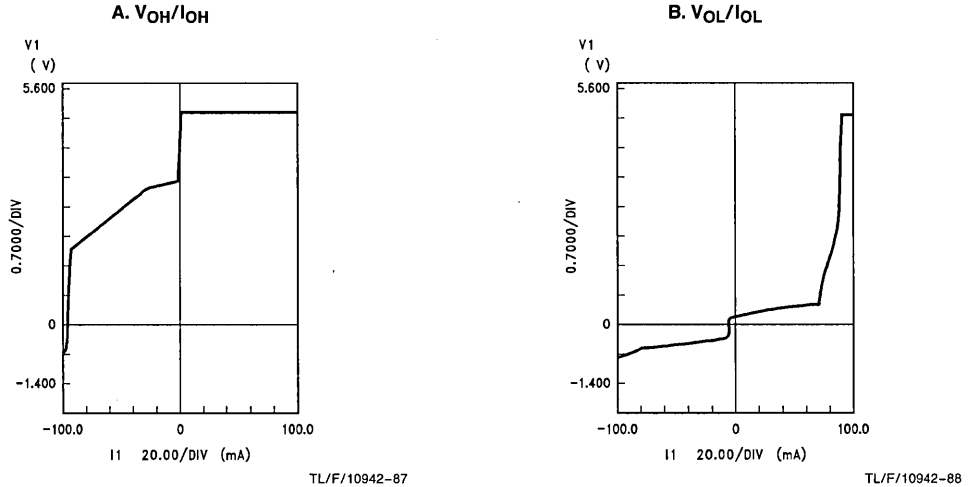
Clock Modeling: Transmission Line Characteristics (TLC)

As the speed of the clock signals increase, system designers must account for transmission lines effects. As a general rule of thumb, if the rise or fall time of any signal is more than twice the propagation delay of the signal's path, the path (trace) behaves as a transmission line. Clocks today operate in the 50 MHz region with the rise and fall time approaching sub-nanosecond transition performance. Also the length of traces are not getting any shorter and the need to distribute the clock to many components at different locations has actually increased. This results in the need to evaluate and simulate the board for transmission line and cross-talk effects caused in high frequency.

Many simulation tools are available today and each has a unique set of information required to perform simulation. Given a set of conditions and characteristics, most of these tools simulate the effects of transmission lines and crosstalk on any path. They usually require information such as the driver's and receiver's input and output characteristics along with information from PC board manufactures regarding the board's layout and impedance characteristics.

In order to create a model for the driver one must know how the driver behaves as its medium changes. That is how parameters such as t_{rise}, t_{fall} along with the output impedance change when board parameters such as length and/or the line's impedance change. For this reason many simulators such as QUAD DESIGN's XNS/TLC require models of the drivers and receivers. These models can be obtained either from the manufacturers or can be measured. t_{rise} and t_{fall} times can be measured from plots of the output driving purely resistive loads. I-V plots (i.e., plots of V_{OH}/I_{OH} and V_{OL}/I_{OL}) can be extrapolated from the load lines and the effective impedance of the output. The output's pin capacitance is also needed since it adds to the total load.

Below are the I-V plots for CGS74B2525, CGS74C2525 and CGS74CT2525 *(Figures 2-32, 2-33, 2-34)*. They reflect a typical output's (pin 14, Q8) performance. The load lines can be obtained by calculating the slopes of V_{OH} and V_{OL}. t_{rise} and t_{fall} graphs *(Figures 2-35, 2-36, 2-37)* will provide the signal transition times needed for analysis of the transmission line.



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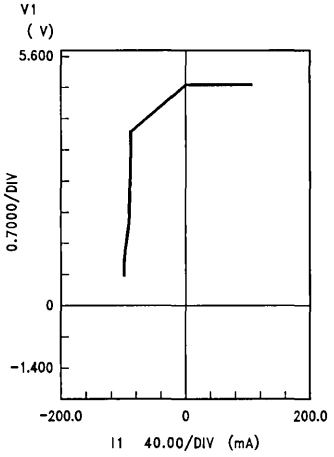
TL/F/10942–88

FIGURE 2-32. I-V Plots for CGS74B2525

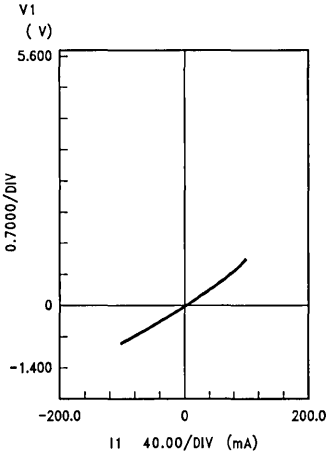
Clock Modeling: Transmission Line Characteristics (TLC) (Continued)

A. V_{OH}/I_{OH}



TL/F/10942–89

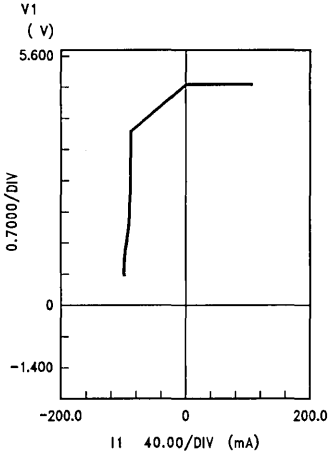
B. V_{OL}/I_{OL}



TL/F/10942–90

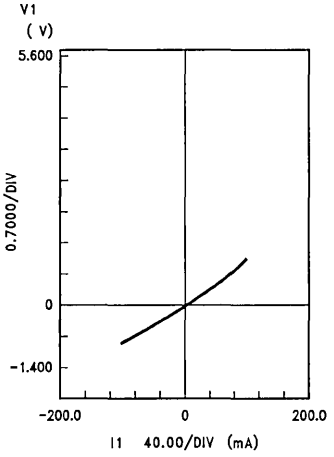
FIGURE 2-33. I-V Plots for CGS74C2525

A. V_{OH}/I_{OH}



TL/F/10942–91

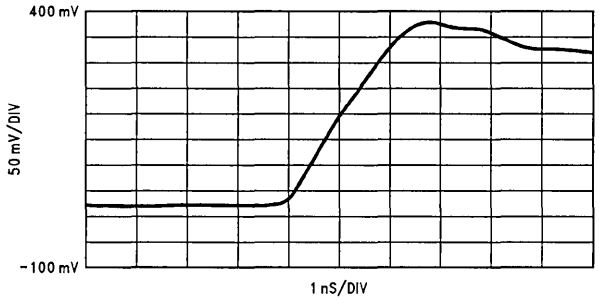
B. V_{OL}/I_{OL}



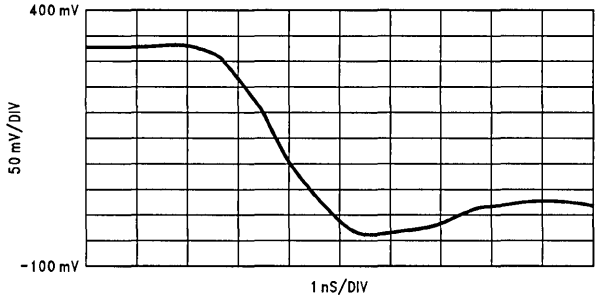
TL/F/10942–92

FIGURE 2-34. I-V Plots for CGS74C2525

Clock Modeling: Transmission Line Characteristics (TLC) (Continued)

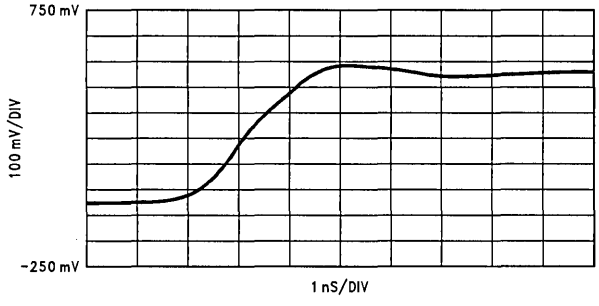


TL/F/10942–93

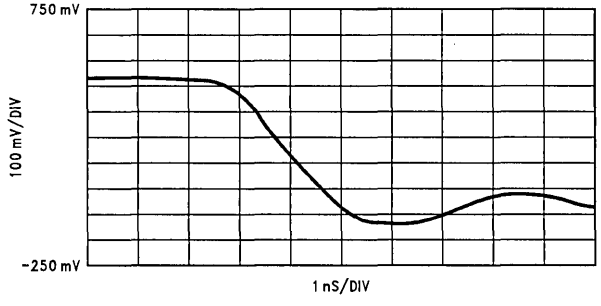


TL/F/10942–94

FIGURE 2-35. t_{rise} and t_{fall} Plots for CGS74B2525



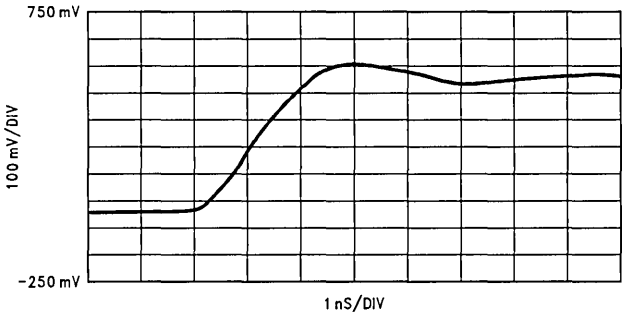
TL/F/10942–95



TL/F/10942–96

FIGURE 2-36. t_{rise} and t_{fall} Plots for CGS74CT2525

Clock Modeling: Transmission Line Characteristics (TLC) (Continued)



TL/F/10942–98

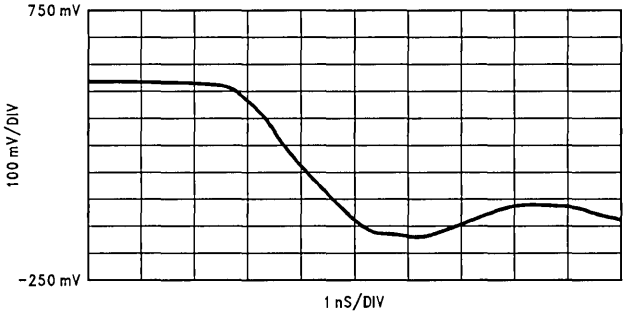


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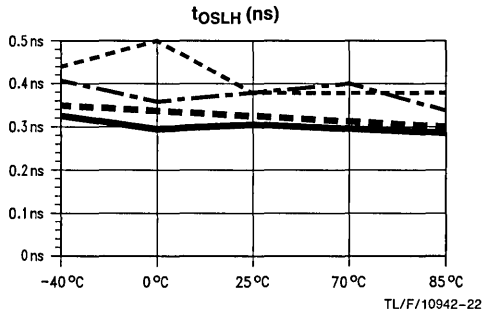
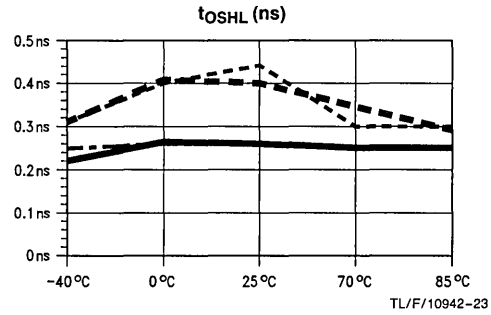
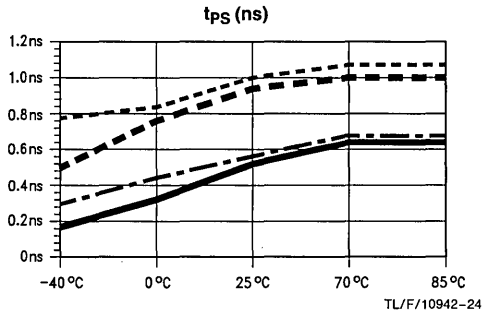
FIGURE 2-37. t_{rise} and t_{fall} Plots for CGS74C2525

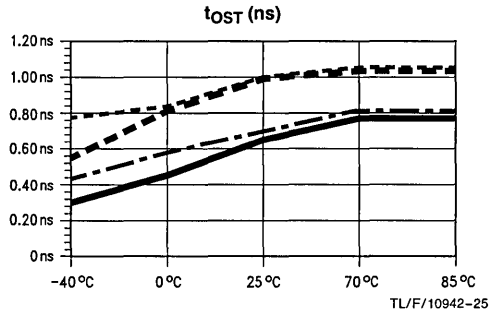
Temperature vs V_{CC} Derating Curves

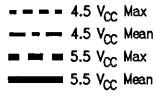
The following graphs show the performance of the B2525 across V_{CC} and temperature. The data was collected for 50 pF, 500Ω loads.











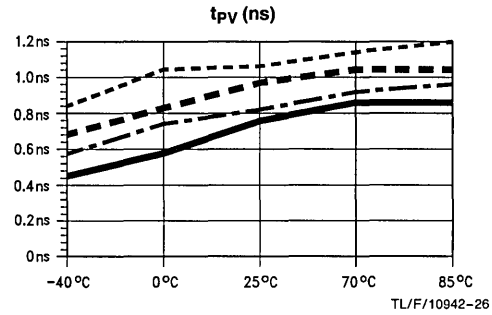
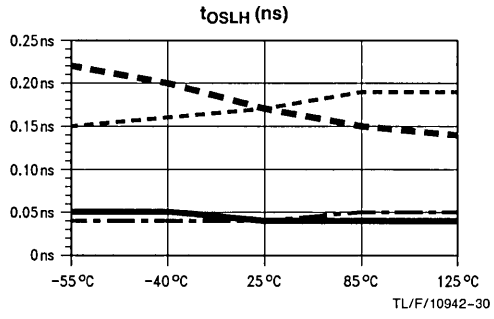
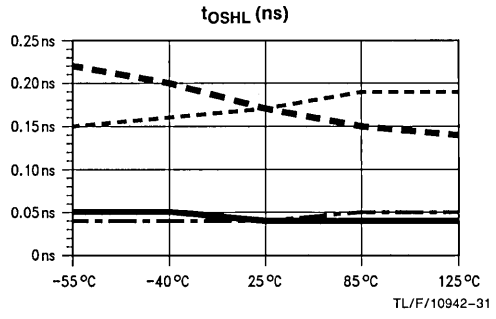


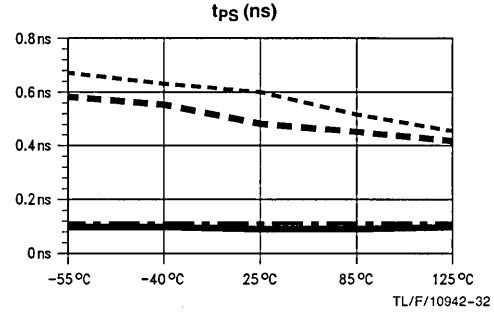
FIGURE 2-38. CGS74B2525 Performance Data

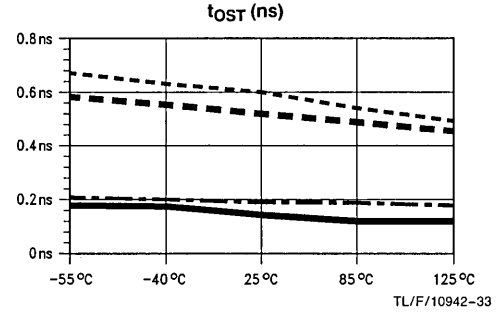
Temperature vs V_{CC} Derating Curves (Continued)

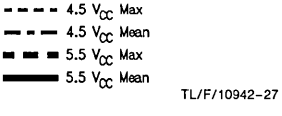
The following graphs show the performance of the C2525 across V_{CC} and temperature. The data was collected for 50 pF, 500Ω loads.











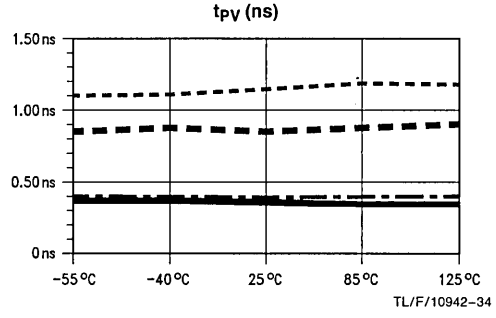


FIGURE 2-39. CGS74C2525 Performance Data

Temperature vs V_{CC} Derating Curves (Continued)

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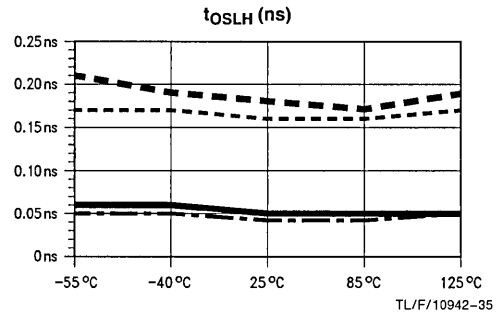

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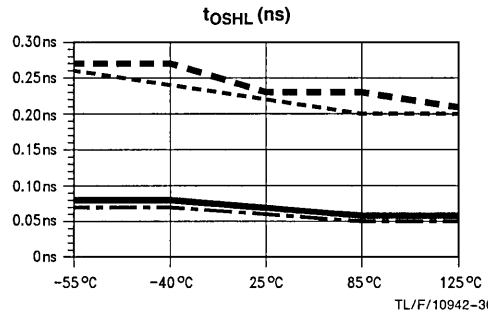
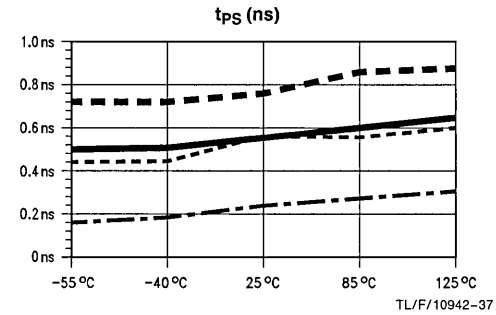
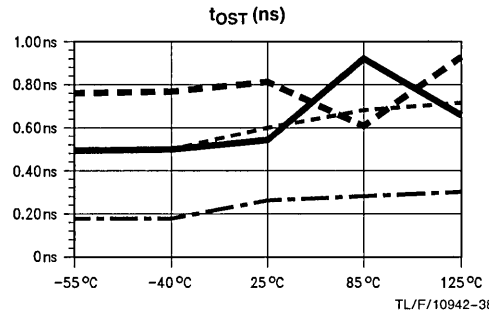


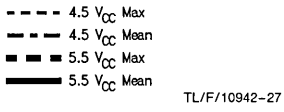
TL/F/10942–36



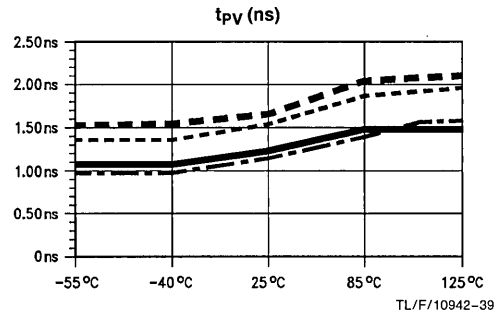
TL/F/10942–37



TL/F/10942–38



TL/F/10942–27



TL/F/10942–39

FIGURE 2-40. CGS74CT2525 Performance Data

Temperature vs V_{CC} Derating Curves (Continued)

The following graphs show the performance of the B2525 and C2525 across V_{CC} and temperature. The data was collected for 50 pF, 500Ω loads.

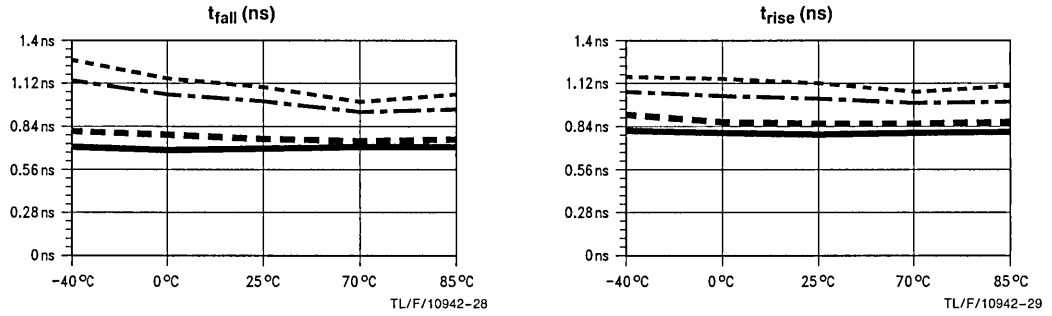


FIGURE 2-41. CGS74B2525 t_{rise} and t_{fall}

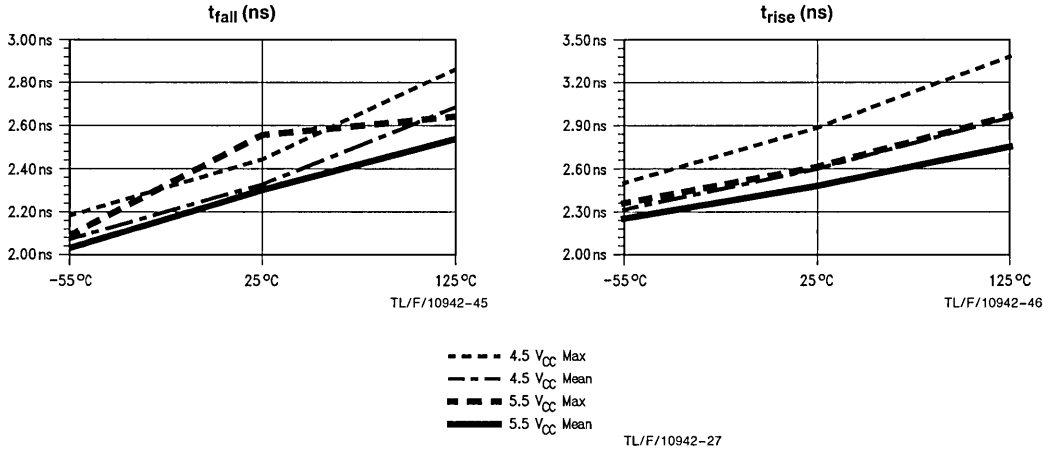


FIGURE 2-42. CGS74C2525 t_{rise} and t_{fall}

Power Performance vs Process Technology

For synchronous systems to operate, the clock must always be functioning. In the higher performance systems for which National's CGS products are targeted, the system clock is typically operating at very high frequencies, driving large loads, and is rarely if ever turned off (TRI-STATED). Historically the process technology of choice to meet the low power constraints would be CMOS due to its low quiescent power consumption. However, as the frequency of the clock increases, the benefits of CMOS low quiescent power consumption disappear and dynamic I_{CC} becomes a key concern. This is due to the fact that the P-channel and N-channel transistors do not have time to completely turn off (discharge) which results in a low resistive path from V_{CC} to ground.

The graph below presents empirical data comparing CMOS, Bipolar, and ECL power consumption for the CGS devices with no load. Given a standard load, the cross-over frequency of TTL and CMOS moves to the right somewhat (increases to about 25 MHz). This is because, for the Bipolar device I_{CC} increases more across frequency than for the CMOS device. As the internal impedance of the Bipolar device is more than CMOS, external loads added in parallel will reduce the total load (impedance). This affects Bipolar more than CMOS. This holds true until the load impedance becomes more than the internal impedance of the Bipolar device.

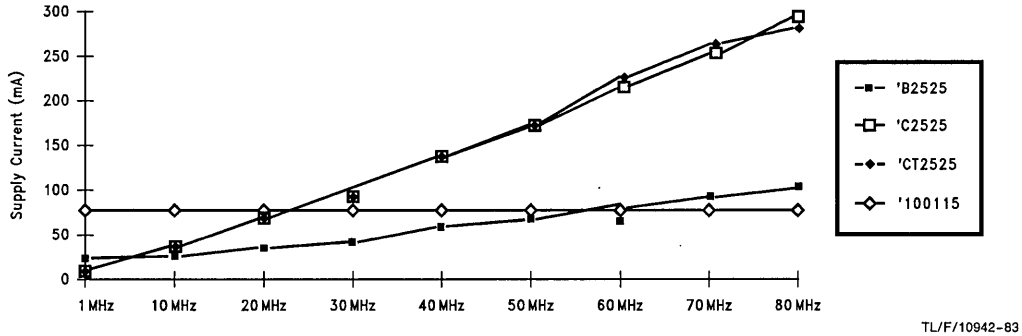


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FIGURE 2-43. Dynamic Power Comparison

Note: This graph reflects dynamic conditions only, no loading. The power supply (V_{CC}) for the '2525 devices is +5.0V; and for the 100115, V_{EE} = −4.8V. The 100115 device, as with all ECL devices, demonstrates constant current over frequency. All these clocked devices' power supply current will increase proportionately as their outputs are connected to a load.

In conjunction with the dynamic I_{CC}, the output loading will affect the f_{MAX} (Maximum operating frequency). The graphs below show how maximum operating frequency of the device is limited by system airflow. These charts provide the recommended airflow to maintain +150°C junction temperature. The maximum power consumed by the chip is calculated given the output load and frequency. Balanced loads are assumed across all outputs.

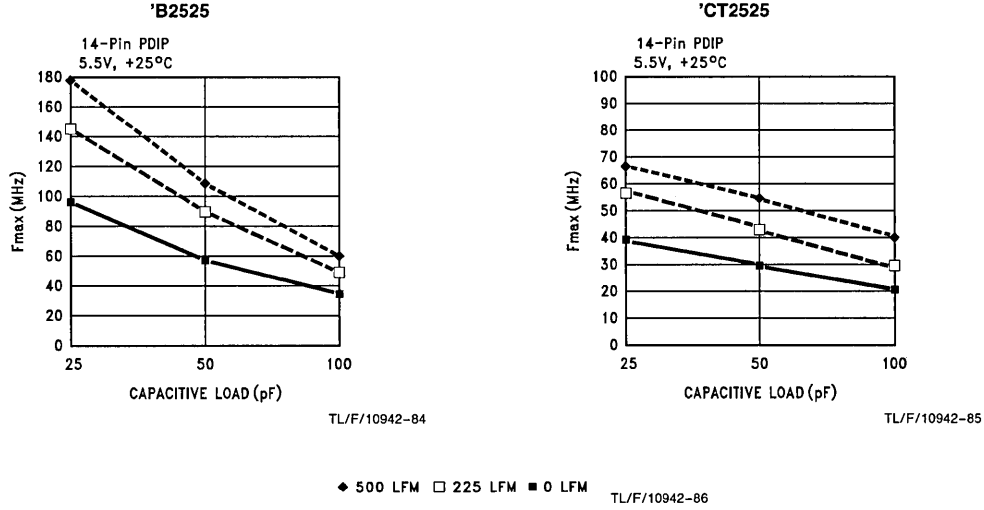

FIGURE 2-44. Airflow vs Frequency a) 'B2525, b) 'CT2525

Section 3

Selection Criteria and Datasheets

Section 3 Contents

Clock Generation and Support (CGS™)

APPLICATIONS

Selecting the Correct Clock-Generation-and-Support (CGS™) Product for your High Speed Application

INTRODUCTION

Clock generation and support is a key design area that enables today's CISC- and RISC-based systems to optimize maximum operating frequencies. The primary goal of the system clock is to deliver a clock signal to each component's input pins while meeting the system's requirements for skew, acceptable wave shape (rise and fall time, overshoot, undershoot, voltage swings), stability (cycle to cycle), and avoiding setup and hold time violations. The components of clock skew include intrinsic skew (pin to pin skew within a single chip) and extrinsic skew (clock skew generated from trace routing and loading).

This section presents input clock requirements for some of today's popular processors and defines each requirement. A typical memory caching scheme is presented and analyzed for the need of a minimum skew clock driver. A decision tree presents a guide for selecting from National Semiconductor's CGS products that are available on different process technologies.

SUMMARY OF INPUT CLOCK REQUIREMENTS

Each microprocessor has unique input clock requirements. These requirements are based on factors such as operating frequency (MHz) and the structure of the input clock (i.e., CMOS or Bipolar). This is true for the CPU, FPU, and/or any peripherals (controllers). Almost every device which requires a clock for its operation has common parameters shown in Table 3-I, which presents a summary of popular microprocessor's input clock requirements. Among these parameters the most common ones are t_{rise}, t_{fall}, and the duration of the high and low pulses, namely pulse width high and low.

t_{rise} and t_{fall} parameters require that the driver make a transition from low to high state (t_{rise}) and vice versa (t_{fall}) during a set amount of time. The actual specification has voltages as reference points such as 0.8V to 2.0V for bipolar and typically 20% to 80% of the V_{CC} for CMOS devices. The trend in the microprocessor t_{rise} and t_{fall} is toward faster edge rates, driven by the shorter period of the higher-frequency CPU's. The downside is that faster edge rates cause unwanted noise such as overshoot and undershoot which may cause glitches that can change the internal thresholds and cause erroneous triggering.

TABLE 3-I. Input Clock Requirements of Some Popular Microprocessors

Processor	Input CLK Frequency		t_{rise}		t_{fall}		High Width		Low Width		Swing	Fig.
			ns Max	Volts a, b	ns Max	Volts c, d	ns Min	Volts b, c	ns Min	Volts a, d		
Intel 386DX	CLK2	*66 MHz	4.0	3.7, 0.8	4.0	0.8, 3.7	4.5	3.7, 3.7	4.5	0.8, 0.8	CMOS	1
Intel 387DX	CLK2	*66 MHz	4.0	3.7, 0.8	4.0	0.8, 3.7	4.5	3.7, 3.7	4.5	0.8, 0.8	CMOS	1
Intel i486	CLK	50 MHz	2.0	2.0, 0.8	2.0	0.8, 2.0	7.0	2.0, 2.0	7.0	0.8, 0.8	TTL	1
Mot 68040	PCLK	*50 MHz	1.7	2.0, 0.8	1.7	0.8, 2.0	10.5	1.5, 1.5	10.5	1.5, 1.5	TTL	2
NSC32532	CLK	*66 MHz	3.0	2.0, 0.8	3.0	0.8, 2.0	4.3	2.0, 2.0	4.3	0.8, 0.8	TTL	1
AMD29000	CLK	*50 MHz	5.0	2.0, 0.8	5.0	0.8, 2.0	10.5	1.5, 1.5	10.5	1.5, 1.5	TTL	2
LSI 64901	CLK	25 MHz	3.0	2.0, 0.8	3.0	0.8, 2.0	15.0	1.5, 1.5	15.0	1.5, 1.5	TTL	2
Intel i860	CLK	50 MHz	6.0	3.0, 0.8	6.0	0.8, 3.0	3.0	3.0, 3.0	5.0	0.8, 0.8	CMOS	1
Intel I960ca	CLK	40 MHz	6.0	2.0, 0.8	6.0	0.8, 2.0	5.0	2.0, 2.0	5.0	0.8, 0.8	TTL	1
Mot 88100	CLK	25 MHz	4.0	4.0, 1.0	4.0	1.0, 4.0	19.0	0.8, 0.8 V_{CC}	19.0	0.2, 0.2 V_{CC}	CMOS	1
MIP R3001	CLK2 (xsys)	*66 MHz	5.0	2.0, 0.8	5.0	0.8, 2.0	6.0	1.5, 1.5	6.0	1.5, 1.5	TTL	2

*Divide by two is done internally.

CGS (Continued)

$$t_{(period)} = t_{rise} + t_{fall} + \text{High Width} + \text{Low Width}$$

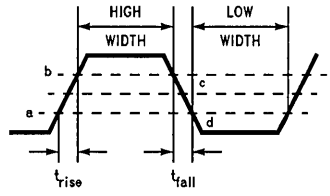

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FIGURE 3-1. Input Clock Period

The high and low pulse durations are required specifications of the input clocks. These parameters guarantee that there is enough time for the processor to recognize the transition. This may also be looked at as a hold-time equivalent of the input clock for any internal transitions. Again these parameters are specified at reference voltages and vary from processor to processor.

The combination of t_{rise} and t_{fall} along with pulse width high and low determine the operating frequency of the system. If the t_{rise} and t_{fall} are equal and all of the reference points are the same (see *Figure 3-1*), frequency is the reciprocal of the clock period, and the clock period can be determined from the addition of the low and high pulse widths along with t_{rise} and t_{fall} transitions.

As the speed of the microprocessors increases, the input clock specifications become more stringent (see Table 3-I). As an example t_{rise} and t_{fall} are required to be under 2 ns for Motorola's 68040 microprocessor running at 50 MHz. Pulse width durations are also required to be shorter since the total clock period is reduced. These requirements affect systems that are synchronized using various distribution methods. The rise and fall times along with the skew of the outputs become critical design considerations.

The Minimum Skew Clock Design Problem

Example: i386™-33 MHz caching restriction.

A typical cache scheme using an Intel's 386 microprocessor is shown in *Figure 3-2*. This example, described below, illustrates the need for a minimum skew clock driver providing the clock input to the CPU and the cache controller. The cache controller used is Intel's 80395™.

In *Figure 3-2* the CPU's address bus is connected directly to the Tag memory (Tag RAM) which is an SRAM. Depending on the scheme used, all or some of the address bits (A00 thru A31) may be connected from the CPU to the cache tag (direct mapped system or associative set mapping). The function of the tag RAM is to indicate to the controller by means of its MATCH output signal whether the address requested by the processor exists within the cache RAM.

Also connected from CPU directly to the cache memory is the data bus. Again all or some bits could be directly connected depending on the size of the data bus. The cache controller requires many inputs from the CPU as its control signals, among which are the W/R# and ADS#. The W/R# is a read/write signal generated by the CPU indicating if the current cycle is a read or a write operation. The ADS# status signal also generated from the CPU and it indicates if the address bus is valid or not. The cache controller also provides control signals of its own, some of which are inputs to the CPU and some are for controlling the status of the SRAMs. The Ready# signal supplied to the CPU indicates whether or not the contents of the SRAMs have been accessed (case of hit). WE# and OE are outputs from the controller to the memory arrays. WE# indicates if the current cycle is a read or write cycle, OE enables or disables the output of the cache RAM. Finally provided to both units are the CLK2 signals which are twice the operating frequency of the system (66 MHz), hence each unit performs the divide-by-two function internally to obtain the required duty cycle. Both of these clocks are supplied from an oscillator and are distributed by a driver. The function typically used as the driver was the '244 or '1004 with all inputs hard wired together. National's CGS products replace the '244, '1004 function, provide the benefits of tighter skew, and also minimize impedance mismatches in the '244, '1004 implementation due to the multiple inputs being tied together.

CGS (Continued)

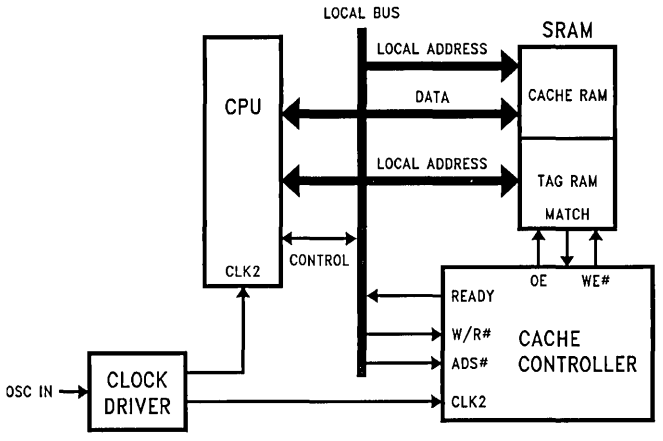
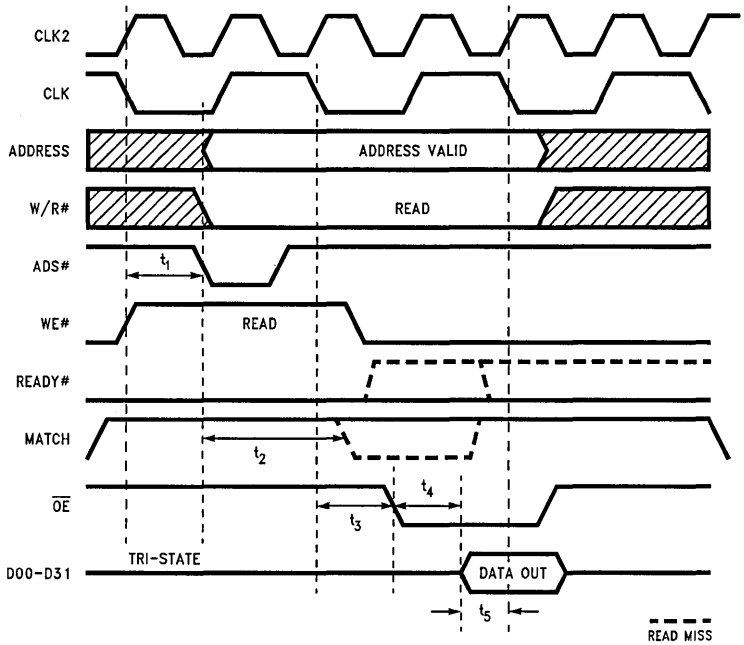


FIGURE 3-2. Cache Module for Intel's 386DX™

Figure 3-3 is the timing cycle for the *Figure 3-2* cache controller. This timing diagram shows a cache memory hit cycle. During this cycle the CPU issues the read command by activating a low on W/R# status line. When this line is low it indicates that the following cycle is a read cycle from memory. Next, the Address output pins of the CPU become valid (i.e., they correspond to a readable address). This time is indicated by the ADS# status signal transitioning from a high to a low, which is the Address Valid Delay time of the CPU. For the i386DX operating at 33 MHz this is 15 ns (T1). Notice that W/R# and ADS# are activated on a low transition of the CLK signal, which is the internal clock of the CPU and the controller, and is obtained by performing a divide-by-two function of the CLK2. Also an assumption has been made by the controller that this cycle will be a read cycle. This assumption allows the controller to provide a high on the W/E# status input signal to the cache arrays. At this time the memory starts its address access cycle. This time with current cache technologies is no less than 20 ns (T2). The addition of these two times (address valid delay T1, plus memory access time T2) equals 35 ns which is longer than the period of the internal CLK (30 ns). The second assumption by the controller is now made, that is, there will be a cache hit. If the assumption is invalid and there is not a cache hit the CPU will have to wait for the data to be accessed from the main memory (normally DRAM arrays). However, this "HIT" assumption can be made since the amount of time for the controller to reverse this operation by activating the Ready# signal is 4 ns, and therefore less than the OE enable time (T3). The "HIT" assumption is actually made at the second negative transition of the CLK, where the controller enables the cache outputs by driving the OE signal low. Enabling the OE pin on the SRAMSs allows the data to be released to the local data bus. The amount of time for this operation is 15 ns (T3) for the 395 module operating at 33 MHz plus the SRAMs output enable time from TRI-STATE to active (T4) which is 10 ns. Another timing requirement is the CPU's data set-up time. This time is 5 ns and is the amount of time that the data has to be on the local bus before the next negative transition of the CLK (T5). The sum of these three timing requirements (T3 + T4 + T5) equals 30 ns which is coincident with the CLK's total period. This indicates the amount of tolerance between the two clocks supplied to the CPU and the cache controller can not exceed 0 ns! However, in reality this time can vary somewhat since the timing specifications are at absolute maximum.

In this typical configuration it is assumed that the clocks to the CPU and controller are identical. In most applications the source of these clocks (CLK2) are supplied by an oscillator feeding into a clock driver. Ideally all outputs of the driver are identical, however, in reality there is a difference between the propagation delays of each output pin. This delay difference is known as skew. Therefore the CLK2 signals to the CPU and controller are not identical and the skew between them needs to be accounted in the timing diagram of *Figure 3-3*. National's CGS devices, with guaranteed skew specifications, enable designers to optimize system operating frequencies.

CGS (Continued)



TL/F/10942-A2

FIGURE 3-3. Read Hit Cycle

CGS Selection Criteria

The decision tree provides a summarized method for choosing the appropriate CGS technology based on system application requirements.

The first decision must be made knowing the power supply and maximum clock frequency. Dynamic I_{CC} graphs demonstrates that CMOS provides the best power/frequency performance below 20 MHz, TTL is the optimal choice between 20 MHz–70 MHz, and ECL above 70 MHz. Propagation delay is a concern in applications such as clock trees where the maximum operating frequency is a reciprocal function of the sum of the propagation delays through the tree. t_{rise} and t_{fall} requirements are driven by CPU demands which require the transitions to be less than 2 ns between 0.8V and 2.0V.

The Skew parameters are somewhat less flexible in terms of system designs. For most cases less than 1.0 ns of skew for t_{PLH} and t_{PHL} are required in order to preserve synchronization and less than 2.0 ns of t_{PS} (example at 50 MHz) to preserve the duty cycle. Part-to-part skew is critical when the system design incorporates clock trees as previously described.

The amount of drive is mainly a function of system bus requirements and loading. Additional concerns are items such as symmetric outputs to optimize termination schemes and whether or not the CPU or ASIC requires CMOS rail-to-rail input swings.

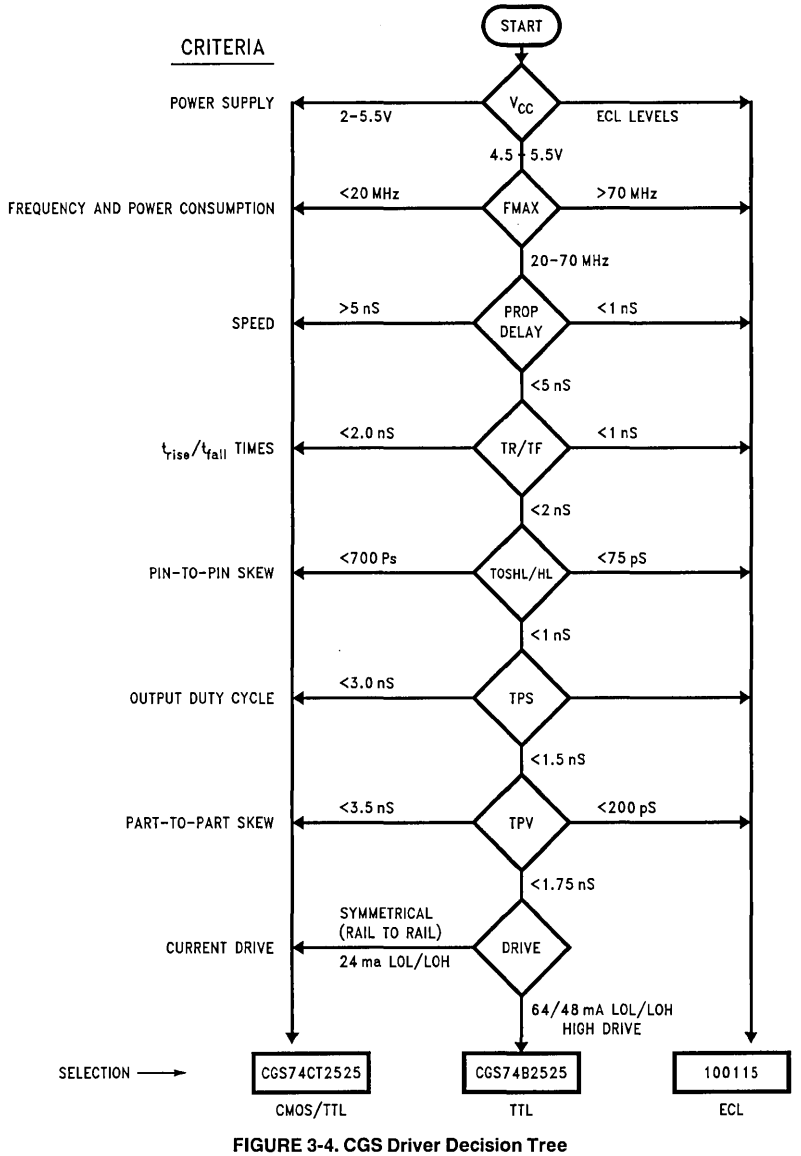


FIGURE 3-4. CGS Driver Decision Tree

Selection Criteria for CGS Drivers

TABLE 3-II

Customer Decision Driver	Significance	Performance Comment	Device Selection		
			Bipolar CGS74B2525	CMOS/TTL CGS74C2525 CGS74CT2525	ECL 100115
			Values	Values	Values
Skew (ns) Pin-to-Pin Skew, $T_{OSH/LH}$ (T_{SG-G} in ECL)	Meets skew requirements of microprocessor clock designs by reducing timing guardbands.	In most systems, 1 ns or less of output skew is acceptable. All CGS drivers meet this need.	1 ns	700 ps	75 ps
Part-to-Part Skew, T_{PV}	Part-to-Part skew is critical in multi-level tree and parallel driving applications.	Best in ECL then Bipolar then CMOS.	1.75 ns	3.5 ns	TBD
Pin Signal Skew, t_{PS} (Duty Cycle Degradation)	Meets duty cycle requirement of microprocessors (45/55%)	Output signal symmetry is best in bipolar then CMOS.	1.5 ns	3.0 ns	TBD
$t_{rise/fall}$ Time (ns)	Many microprocessor specs (50 MHz–80 MHz) require 2 ns or less $t_{rise/fall}$ times.	All CGS drivers have 2 ns or less $t_{rise/fall}$ performance.	< 2 ns	< 2 ns	0.75 ns
Unbalanced Load Skew Performance	Helpful in designing skew devices for unmatched loads and PCB routing discontinuities.	Overall CMOS/TTL part has better unmatched load skew performance than Bipolar. ECL data not available.	See CGS Performance Feature		Not Evaluated
Speed t_{PLH} t_{PHL}	May be a limiting factor in high speed system designs.	Technology performance shows ECL best then bipolar (FAST™LSI) and then CMOS (FACT™).	4.8 ns	12.4 ns	0.85 ns
Current Drive I_{OL} I_{OH}	Depends on applications, e.g., standard TTL or CMOS loads or backplane driving.	Bipolar has highest drive. CMOS has symmetric drive.	64 mA 48 mA	24 mA 24 mA	20 mA 6 mA
Power Dynamic I_{CC} (mA)	Dynamic Power Performance is significant in clock driving applications where drivers are continuously switching; and where TRI-STATE is not common.	Bipolar has best dynamic performance from 20 MHz to 80 MHz. CMOS is good below 20 MHz due to simultaneous conduction (no load conditions).	50 mA @ 50 MHz	160 mA @ 50 MHz	100 mA @ 50 MHz

References

1. NSC/Intel/Motorola/AMD/LSI Logic/MIPs microprocessors Datasheets for specifications on input clocks.
2. XNS/TLC technical manual. QUAD DESIGN, Camarillo, CA.
3. 33 MHz 386 system design considerations. AP-442 Intel microprocessors volume 2 data book.
4. Rich Jolly, Clock Design in 50 MHz i486™ Systems. AP-453 Intel.

National Semiconductor

ADVANCE INFORMATION

CGS74B303/CGS74B304/CGS74B305
Octal Divide-by-2 Circuits/Clock Drivers

General Description

These minimum skew clock drivers are designed for Clock Generation & Support (CGS) applications. The devices guarantee minimum output skew across the outputs of a given device and also from device-to-device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. These octal dividers contain eight flip-flops designed to have minimum skews between the outputs. The '303 is a minimum skew clock driver with six in-phase with CLK and two out-of-phase outputs. The '304 is a minimum skew clock driver with eight in-phase with CLK outputs. The '305 is a minimum skew clock driver with four in-phase with CLK and four out-of-phase outputs.

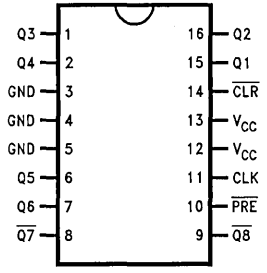
Features

- Functionality compatible to industry standard AS303, AS304 and AS305
- Maximum output skew of less than 1 ns to meet the tight skew budget required in hi-speed clocking schemes
- Specifications for device-to-device variation of output skew to ensure tight skew over process variations
- Specification for transition skew to meet near-50% output duty cycle requirements
- Center pin V_{CC} and GND configuration to minimize high speed switching noise
- Capability of current sourcing 48 mA and current sinking of 64 mA
- Lowest dynamic power consumption at high frequencies

Connection Diagrams

Pin Assignment for DIP and SOIC

'303



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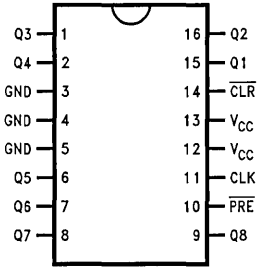
'304



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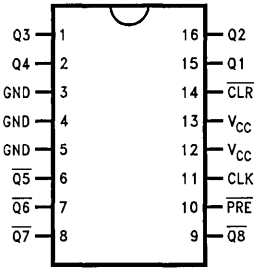
'305



TL/F/10966–3

National Semiconductor

CGS74B2525
1-to-8 Minimum Skew Clock Driver

General Description

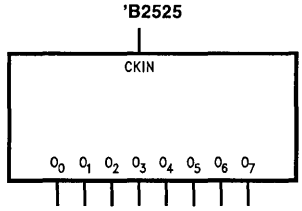
This minimum skew clock driver is designed for Clock Generation and Support (CGS) applications operating well above 20 MHz (33 MHz, 50 MHz). The device guarantees minimum output skew across the outputs of a given device and also from device-to-device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The 'B2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications.

Features

- Clock Generation and Support (CGS) Device—Ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST® LSI process
- 1-to-8 low skew clock distribution
- Sub 1 ns pin-to-pin output skew
- Specifications for device-to-device variation of propagation delay
- Specification for transition skew to meet duty cycle requirements
- Center pin V_{CC} and GND configuration to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 4

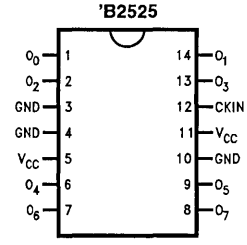
Logic Symbol



TL/F/10907–1

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10907–2

Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when the ('B2525) clock distribution chip is selected.

Pin Description

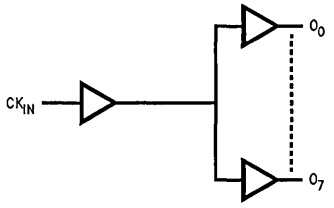
Pin Names	Description
CK_{IN}	Clock Input ('B2525)
O_0–O_7	Outputs

Truth Table

'B2525

Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'B2525



TL/F/10907–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V	
Input Voltage (V_I)	7.0V	
Operating Free Air Temperature	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	
Typical θ_{JA}		
Plastic (N) Package	104	°C/W
JEDEC SOIC (M) Package	120	°C/W

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage—High (V_{IH})	2.0V
Input Voltage—Low (V_{IL})	0.8V
High Level Output Current (I_{OH})	−48 mA
Low Level Output Current (I_{OL})	+64 mA
Free Air Operating Temperature (T_A)	0°C to +70°C

DC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = −48 mA, V_{CC} = 4.5V		2.0			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 64 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IH} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		8	15	mA
			Outputs Low		32	42	mA
C_{IN}	Input Capacitance	V_{CC} = 5V			5		pF

AC Electrical Characteristics

Symbol	Parameter	CGS74B			Units
		V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF			
		Min	Typ	Max	
t_{PLH}	Propagation Delay	2	2.9	4.8	ns
t_{PHL}	CK to O_n ('2525)	2	3.0	4.8	

Extended AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74B $R_L = 500\Omega$, $C_L = 50$ pF, $T_A = 0°C$ to $70°C$			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		0.15	1	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation (Note 1)	5.0		0.7	1.5	ns
t_{PV}	Maximum Skew Part-to-Part Variation Skew (Note 2)	5.0			1.75	ns
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6	1.5	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (from 0.5/2.4V to 2.4/0.5V at 33 MHz, $T_A = 25°C$)	5.0 5.0		1.90 1.15		ns ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

National Semiconductor

CGS54C/74C2525 • CGS54CT/74CT2525
CGS54C/74C2526 • CGS54CT/74CT2526
1-to-8 Minimum Skew Clock Driver

The CGS 'C/CT2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The '2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions. The '2526 is similar to the '2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

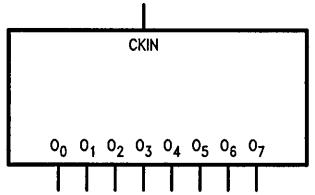
Features

- These CGS devices implement National's FACT™ family
- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- Symmetric output current drive of 24 mA for I_{OL}/I_{OH}
- 'CT has TTL-compatible inputs
- These products identical to 74AC/ACT2525 and 2526

Ordering Code: See Ordering Information

Logic Symbols

'2525



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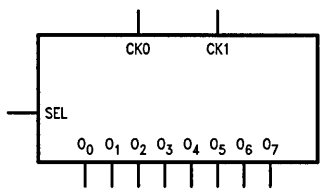
'2526



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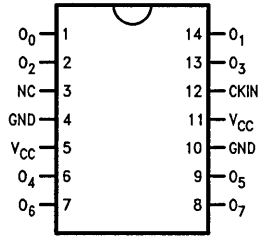
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC

'2525



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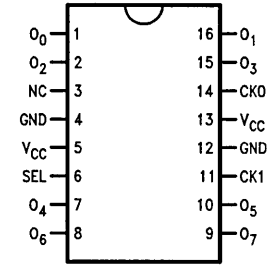
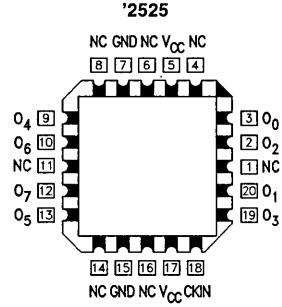
'2526



TL/F/10684–4

Pin Assignment for LCC

'2525



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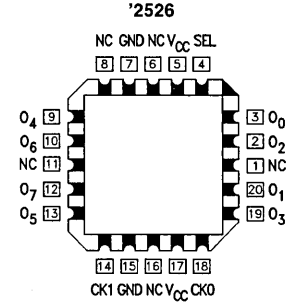
'2526



TL/F/10684–6

Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CK_n input will have an active effect on the outputs of the circuit. When SEL = 1, the CK_1 input is selected and when SEL = 0, the CK_0 input is selected. The non-selected CK_n input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK_{IN} or CK_1/CK_0 pins when either the multiplexed ('2526) or the straight ('2525) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK_{IN}	Clock Input ('2525)
CK_0, CK_1	Clock Inputs ('2526)
O_0–O_7	Outputs
SEL	Clock Select ('2526)

Truth Tables

'2525

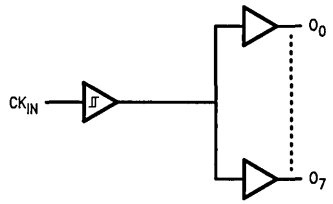
Inputs	Outputs
CK_{IN}	O_1–O_7
L	L
H	H

'2526

Inputs			Outputs
CK_0	CK_1	SEL	O_1–O_7
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

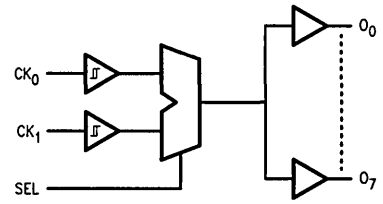
L = Low Voltage Level
H = High Voltage Level
X = Immaterial

'2525



TL/F/10684–7

'2526



TL/F/10684–8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+0.2 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = 0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 MA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of CGS circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'C	2.0V to 6.0V
'CT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
CGS74C/CT	−40°C to +85°C
CGS54C/CT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'C Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'CT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for CGS54C/74C Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74C T_A = +25°C	CGS74C	CGS54C T_A = −55°C to +125°C	CGS74C T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.40	0.44		12 mA
		4.5		0.36	0.50	0.44	V	24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for CGS54C/74C Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	CGS74C $T_A = +25°C$	CGS54C $T_A = -55°C$ to $+125°C$	CGS74C $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for CGS54C @ 25°C is identical to CGS74C @ 25°C.

DC Electrical Characteristics for CGS54CT/74CT Family Devices

Symbol	Parameter	V_{CC} (V)	CGS74CT $T_A = +25°C$	CGS54CT $T_A = -55°C$ to $+125°C$	CGS74CT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for CGS54CT @ 25°C is identical to CGS74CT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter		V_{CC}* (V)	CGS74C $T_A = +25°C$ $C_L = 50$ pF			CGS54C $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74C $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)		3.3 5.0	3.0 3.2	6.5 5.0	11.0 7.8	3.0 2.5	11.0 8.2	3.0 2.9		12.5 8.1	ns
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)		3.3 5.0	3.0 3.6	7.0 5.5	13.0 7.8			3.0 3.3		14.0 8.6	ns
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		3.3 5.0	3.0 4.0	8.0 6.5	14.0 8.5			3.0 3.5		15.0 9.5	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3 5.0		0.3 0.2	1.0 0.7		1.5 1.0			1.0 0.7	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		3.3 5.0		0.3 0.2	1.0 0.7		1.5 1.0			1.0 0.7	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0		1.5 1.0			1.0	ns
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	'C2525 'CT2525 'C2526	5.0			3.5		4.0				ns
		'CT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0		4.0			3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the CLK to Q propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay CK to O_n ('2525)	5.0	4.6	6.5	9.0			4.0	10.1	ns
t_{PLH}, t_{PHL}	Propagation Delay CK(n) to O_n ('2526)	5.0	5.8	8.5	11.1			5.1	12.4	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}* (V)	CGS74CT $T_A = +25°C$ $C_L = 50$ pF			CGS54CT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		CGS74CT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			Units
				Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2526)		5.0	5.1	8.5	12.4			4.4		14.1	ns
t_{OSHL}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OSLH}	Maximum Skew Common Edge Output-to-Output (Note 1) Variation		5.0		0.2	0.7					0.7	ns
t_{OST}	Maximum Skew Opposite Edge Output-to-Output (Note 1) Variation		5.0		0.4	1.0					1.0	ns
t_{PV}	Maximum Skew Part-to-Part Variation (Note 2)	AC2525 ACT2525 AC2526	5.0			3.5						ns
		ACT2526	5.0			5.0						ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (20% to 80% V_{CC})		5.0			3.0					3.75	ns
t_{rise}, t_{fall}	Maximum Rise/Fall Time (0.8V/2.0V and 2.0V/0.8V)				0.9					1.1		ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}).

Note 2: Part-to-part skew is defined as the absolute value of the difference between the propagation delay for any outputs from device to device. The parameter is specified for a given set of conditions (i.e., capacitive load, V_{CC}, temperature, # of outputs switching, etc.). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance ('2525)	820 pF−1.2 x 10^{-18} (f)*	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance ('2526)	820 pF−1.2 x 10^{-18} (f)*	pF	$V_{CC} = 5.0V$

*f = frequency

Recommended Maximum Power Dissipation (W)

LFPM	$T_A = 25°C$		$T_A = 85°C$	
	PDIP	SOIC	PDIP	SOIC
0	1.105	0.858	0.528	0.41
225	1.493	1.055	0.714	0.504
500	1.71	1.210	0.820	0.578

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100115
Low-Skew Quad Clock Driver

General Description

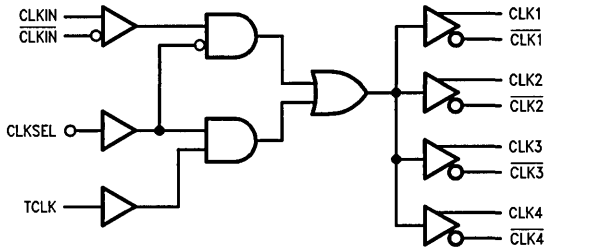
The 100115 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing.

Features

- Low output to output skew (≤75 ps)
- Differential inputs and outputs
- Small outline package
- Ideal for applications which require the low skew distribution of a clock signal to multiple outputs
- Secondary clock available for system level testing

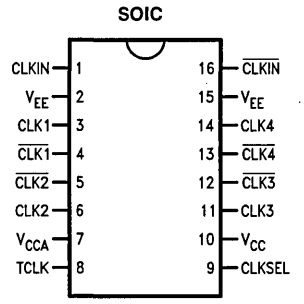
Ordering Code: See Section 4

Logic Diagram



TL/F/9842–2

Connection Diagram



TL/F/9842–1

Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input†
CLKSEL	Clock Input Select†

†TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{\text{CLKIN}}$	TCLK	CLK_N	$\overline{CLK_N}$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Single-Ended Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

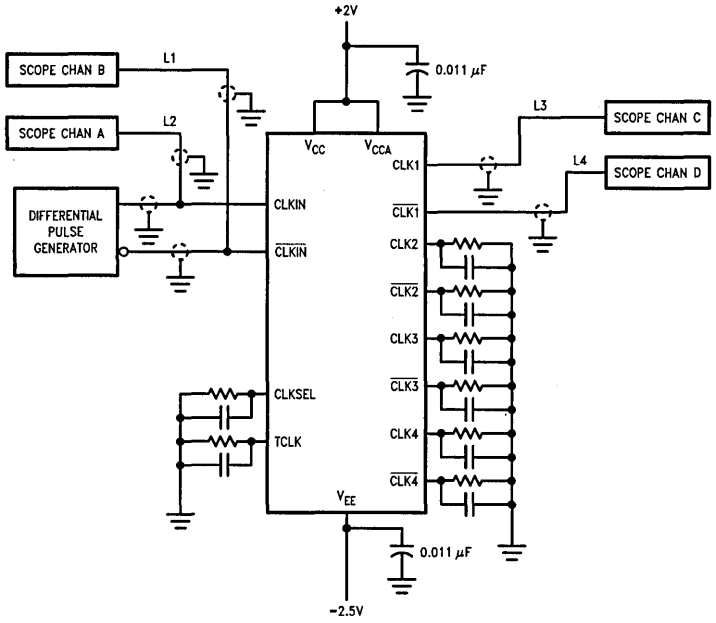
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V	V	
I_{IH}	Input High Current CLKIN, $\overline{CLKIN}$ TCLK CLKSEL			 107 300 260	 μA μA μA	V_{IN} = $V_{IH(Max)}$
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−70		−30	mA	

AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.63	0.83	0.65	0.85	0.70	0.93	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.60	1.40	0.60	1.40	0.60	1.40	ns	*Figures 1, 2*
t_{SG-G}	Skew Gate to Gate (Note 1)		75		75		75	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	0.80	0.30	0.75	0.25	0.75	ns	*Figures 1, 4*

Note 1: Maximum output skew for any one device.



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Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit

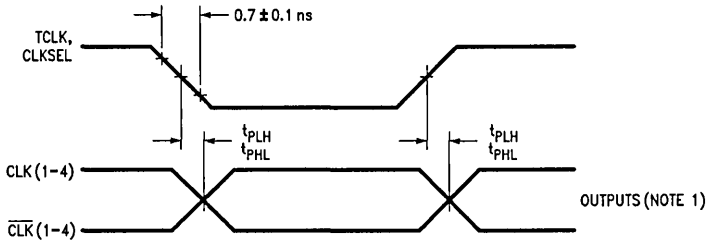

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FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs

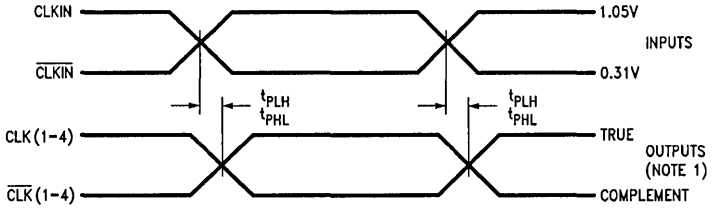

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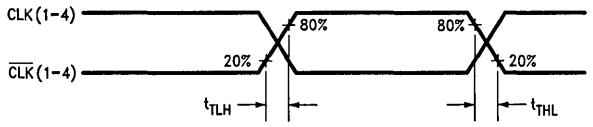
FIGURE 3. Propagation Delay, CLKIN/$\overline{CLKIN}$ to Outputs



TL/F/9842-6

FIGURE 4. Transition Times

Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

National Semiconductor

ADVANCE INFORMATION

100310
Low Skew 2:8 Differential Clock Driver

General Description

The 100310 is a low skew 8-bit differential clock driver which is designed to select between two separate differential clock inputs. The low output to output skew (< 50 ps) is maintained for either clock input. A LOW on the select pin (SEL) selects CLKINA, $\overline{\text{CLKINA}}$ and a HIGH on the SEL pin selects the CLKINB, $\overline{\text{CLKINB}}$ inputs.

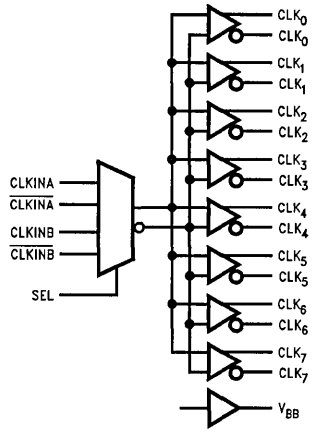
The 100310 is ideal for those applications that need the ability to freely select between two clocks, or to maintain the ability to switch to an alternate or backup clock should a problem arise with the primary clock source.

A V_{BB} output is provided for single-ended operation.

Features

- Low output to output skew (≤ 50 ps)
- Differential inputs and outputs
- Allows multiplexing between two clock inputs
- Voltage compensated operating range: −4.2V to −5.7V

Logic Symbol



TL/F/10943–1

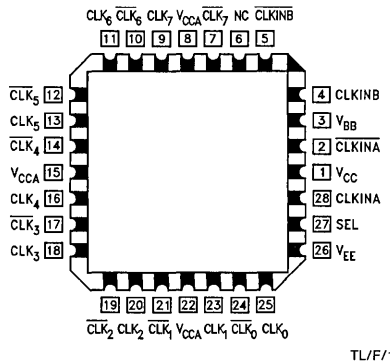
Pin Names	Description
$CLKIN_n$, $\overline{CLKIN}_n$	Differential Clock Inputs
SEL	Select
CLK_{0-7}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKINA	$\overline{\text{CLKINA}}$	CLKINB	$\overline{\text{CLKINB}}$	SEL	CLK_n	$\overline{CLK}_n$
H	L	X	X	L	H	L
L	H	X	X	L	L	H
X	X	H	L	H	H	L
X	X	L	H	H	L	H

Connection Diagram

28-Pin PCC



TL/F/10943–2

National Semiconductor

100311
Low Skew 1:9 Differential Clock Driver

General Description

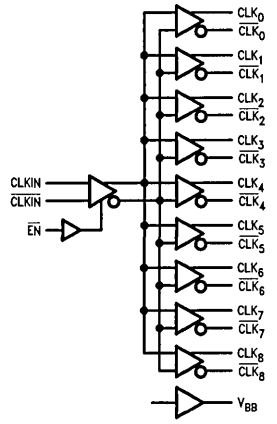
The 100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN, $\overline{CLKIN}$). If a single-ended input is desired, the V_{BB} output pin may be used to drive the remaining input line. A HIGH on the enable pin ($\overline{EN}$) will force a LOW on all of the CLK_n outputs and a HIGH on all of the $\overline{CLK}_n$ output pins. The 100311 is ideal for distributing a signal throughout a system without worrying about the original signal becoming too corrupted by undesirable delays and skew. The 100311 is pin-for-pin compatible with the Motorola 100E111.

Features

- Low output to output skew (≤ 50 ps)
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs

Ordering Code: See Section 4

Logic Symbol



TL/F/10648–1

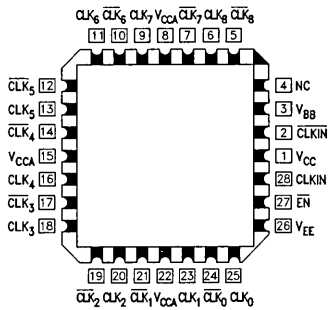
Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
$\overline{EN}$	Enable
CLK_{0-8}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKIN	$\overline{CLKIN}$	$\overline{EN}$	CLK_n	$\overline{CLK}_n$
L	H	L	L	H
H	L	L	H	L
X	X	H	L	H

Connection Diagram

28-Pin PCC



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Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperture (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Industrial	−5.7V to −4.2V

Commercial Version—100311

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Low Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$ $\overline{EN}$			 100 250	μA	V_{IN} = V_{IH} (Max)	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−115		−57	mA	Inputs Open	
V_{PP}	Minimum Input Swing	250			mV		
V_{CMR}	Common Mode Range	−1.6		−0.4	V		

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version—100311 (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay, CLKIN to CLKN Differential Single-Ended	 0.750 0.650	 0.950 1.050	 0.775 0.675	 0.975 1.175	 0.840 0.740	 1.040 1.240	 ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable and Disable to Output	0.75	1.20	0.80	1.25	0.85	1.35	ns	*Figures 1* and *2*
t_R	Release Time $\overline{EN}$ to CLKIN	0.30		0.30		0.30		ns	
t_{skew}	Gate to Gate Skew		50		50		50	ps	
t_s	Setup Time SEL to $CLKIN_N$	250		250		300		ps	
t_h	Hold Time SEL to $CLKIN_N$	0		0		0		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	275	750	275	750	275	750	ps	*Figures 1* and *2*

Note 1: Gate to gate skew is defined as the different in propagation delays between each of the outputs.

Industrial Version—100311

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV		
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −300 μA	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
V_{IH}	Input High Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	

Industrial Version—100311 (Continued)

DC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{IL}	Input Low Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = V_{IL} (Min)
I_{IH}	Input HIGH Current						V_{IN} = V_{IH} (Max)
	CLKIN, $\overline{CLKIN}$		100		100	μA	
	$\overline{EN}$		250		250		
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}
I_{EE}	Power Supply Current	−115	−57	−115	−57	mA	Inputs Open
V_{PP}	Minimum Input Swing	250		250		mV	
V_{CMR}	Common Mode Range	−1.6	−0.4	−1.6	−0.4	V	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

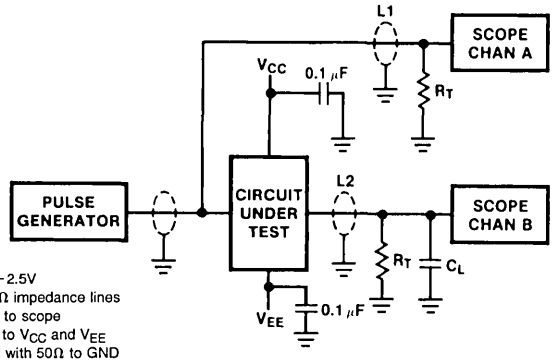
Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Max Toggle Frequency	750		750		750		MHz	
t_{PLH}	Propagation Delay,								
t_{PHL}	CLKIN to CLKN								*Figures 1* and *2*
	Differential	0.725	0.925	0.80	1.00	1.05	1.25	ns	
	Single-Ended	0.625	1.025	0.70	1.20	0.90	1.40		
t_{PLH}	Propagation Delay Enable	0.70	1.20	0.60	1.60	0.60	1.60	ns	*Figures 1* and *2*
t_{PHL}	and Disable to Output								
t_R	Release Time $\overline{EN}$ to CLKIN	0.30		0.30		0.30		ns	
t_{skew}	Gate to Gate Skew		50		50		50	ps	
t_s	Setup Time SEL to $CLKIN_N$	250		200		200		ps	
t_h	Hold Time SEL to $CLKIN_N$	0		0		0		ns	
t_{TLH}	Transition Time	275	750	275	600	275	600	ps	*Figures 1* and *2*
t_{THL}	20% to 80%, 80% to 20%								

Test Circuit

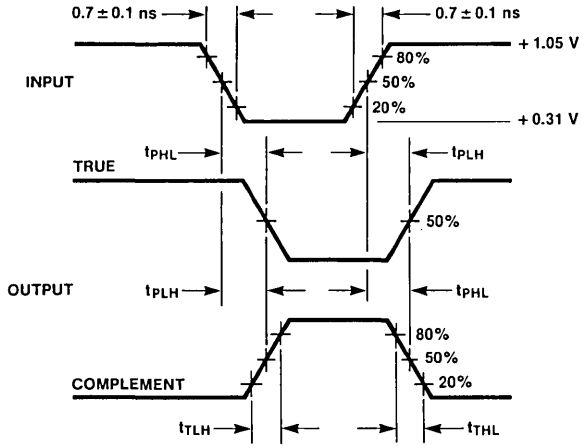


Notes: V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/10648–3

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10648–4

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

100315
Low-Skew Quad Clock Driver

General Description

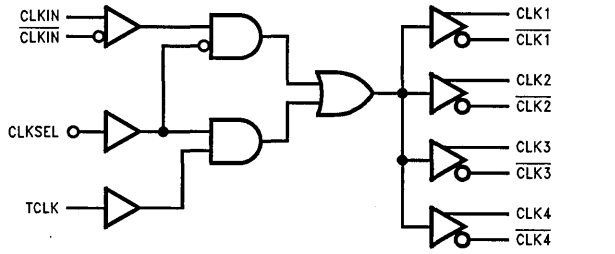
The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Features

- Low output to output skew (≤50 ps)
- Differential inputs and outputs
- Small outline package (SOIC)
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: −4.2V to −5.7V
- Military and industrial grades available

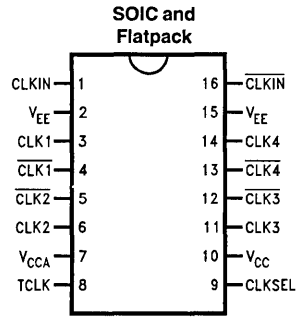
Ordering Code: See Section 4

Logic Diagram



TL/F/10960–1

Connection Diagram



TL/F/10960–2

Pin Names	Description
CLKIN, $\overline{\text{CLKIN}}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input†
CLKSEL	Clock Input Select†

†TCLK and CLKSEL are single-ended inputs, with internal 50 kΩ pulldown resistors.

Truth Table

CLKSEL	CLKIN	$\overline{\text{CLKIN}}$	TCLK	CLK_N	$\overline{CLK_N}$
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Plastic	+150°C
Ceramic	+175°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{CC} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Industrial	−5.7V to −4.2V
Military	−5.7V to −4.2V

Commercial Version—100315

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input High Current					V_{IN} = $V_{IH(Max)}$	
	CLKIN, $\overline{CLKIN}$			150	μA		
	TCLK			250	μA		
	CLKSEL			250	μA		
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V	V		
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−67		−35	mA		
V_{PP}	Minimum Input Swing	250			mV		
V_{CMR}	Common Mode Range	−1.6		−0.4	V		

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version—100315 (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$ Differential Single-Ended	 0.59 0.59	 0.79 0.99	 0.62 0.62	 0.82 1.02	 0.67 0.67	 0.87 1.07	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
t_{PLH} t_{PHL}	Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK_{(1-4)}}$	0.80	1.60	0.80	1.60	0.80	1.60	ns	*Figures 1, 2*
$t_{S\ G-G}$	Skew Gate to Gate (Note 1)		50		50		50	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	*Figures 1, 4*

Note 1: Maximum output skew for any one device.

Industrial Version—100315

DC Electrical Characteristics V_{EE} = −4.2V to −5.7, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{IH}	Single-Ended Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Single-Ended Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	V_{IN} = $V_{IL(Min)}$	
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$ TCLK CLKSEL		 107 300 260		 107 300 260	 μA μA μA	V_{IN} = $V_{IH\ (Max)}$	
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2V		V_{CC} − 0.5V		V		
I_{CBO}	Input Leakage Current	−10		−10		μA	V_{IN} = V_{EE}	
I_{EE}	Power Supply Current	−70	−30	−70	−30	mA		
V_{PP}	Minimum Input Swing	250		250		mV		
V_{CMR}	Common Mode Range	−1.6	0.4	−1.6	−0.4	V		

Industrial Version—100315 (Continued)

AC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$ Differential Single-Ended	 0.59 0.59	 0.99 0.99	 0.62 0.62	 0.82 1.02	 0.67 0.67	 0.87 1.07	ns	*Figures 1, 3*
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns	*Figures 1, 2*
$t_{S\,G-G}$	Skew Gate to Gate (Note 1)		50		50		50	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	

Note 1: Maximum output skew for any one device.

Military Version—100315—Preliminary

DC Electrical Characteristics V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025		−870	mV	0°C to +125°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830		−1620	mV	0°C to +125°C			
		−1830		−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035			mV	0°C to +125°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V	1, 2, 3
		−1085			mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			
V_{DIFF}	Input Voltage Differential	150			mV	−55°C to +125°C	Required for Full Output Swing		1, 2, 3
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V	−55°C to +125°C			1, 2, 3
V_{IH}	Single-Ended Input High Voltage	−1165		−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Single-Ended Input Low Voltage	−1830		−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IH}	Input HIGH Current CLKIN, $\overline{CLKIN}$			120	μA	−55°C to +125°C	V_{IN} = $V_{IH(Max)}$		1, 2, 3
	TCLK			350	μA				
	CLKSEL			300	μA				
I_{CBO}	Input Leakage Current	−10			μA	−55°C to +125°C	V_{IN} = V_{EE}		1, 2, 3
I_{EE}	Power Supply Current, Normal	−90		−30	mA	−55°C to +125°C			1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version—100315—Preliminary (Continued)

AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55°C$		$T_C = +25°C$		$T_C = +125°C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay CLKIN, $\overline{CLKIN}$ to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.61	0.81	0.61	0.81	0.60	0.83	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$	0.50	1.20	0.50	1.20	0.50	1.20	ns		
$t_{S\,G-G}$	Skew Gate to Gate (Note 5)		100		100		100	ps		4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	0.80	0.30	0.75	0.25	0.75	ns		

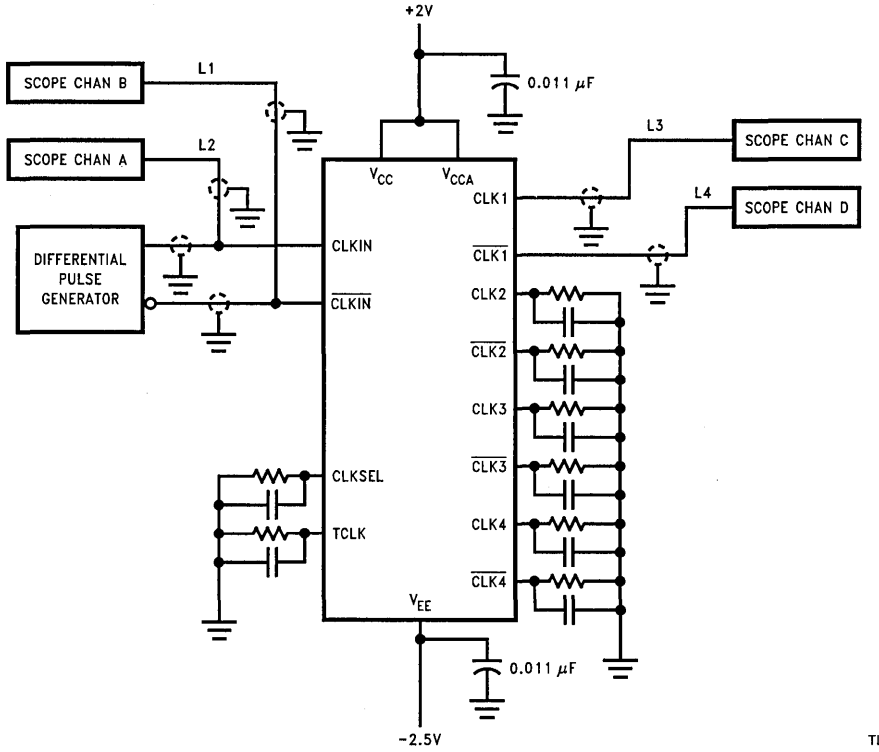
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C, then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Note 5: Maximum output skew for any one device.



TL/F/10960–3

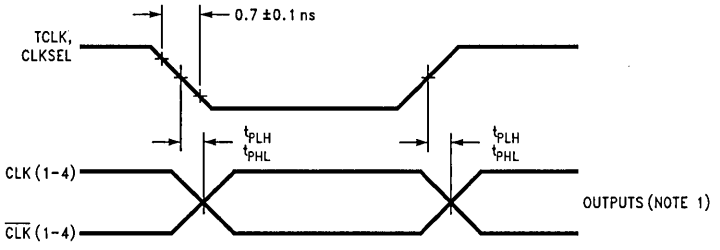
Note 1: Shown for testing CLKIN to CLK1 in the differential mode.

Note 2: L1, L2, L3 and L4 = equal length 50Ω impedance lines.

Note 3: All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.

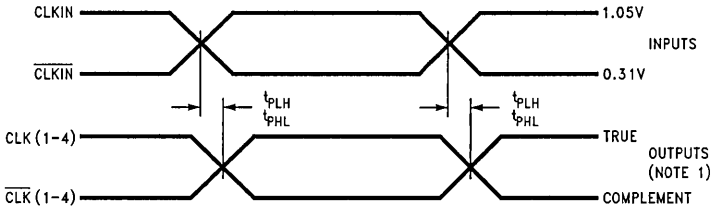
Note 4: Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit



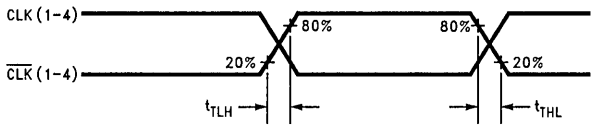
TL/F/10960–4

FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs



TL/F/10960–5

FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs



TL/F/10960–6

FIGURE 4. Transition Times

Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

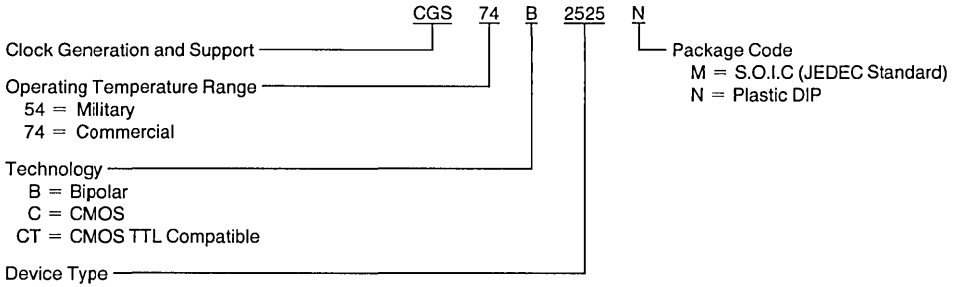
Section 4

Physical Dimensions

Section 4 Contents

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows for Bipolar, CMOS and CMOS TTL compatible CGS parts:

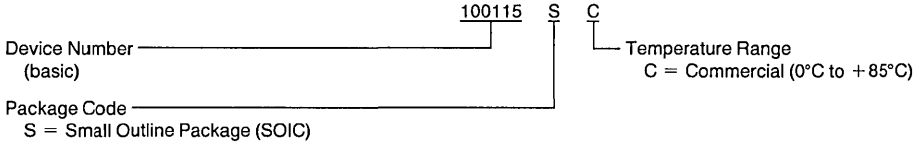


Temperature Information

	Technology	Temperature Range†		
		74-Grade	64-Grade	54-Grade
TTL/CMOS	Bipolar	0°C to 70°C	−40°C to +85°C	−55°C to +125°C
	CMOS	−40°C to +85°C	N/A	−55°C to +125°C
	CMOS/TTL Compatible	−40°C to+85°C	N/A	−55°C to +125°C
	BiCMOS	0°C to +70°C	−40°C to +85°C	−55°C to +125°C

†Typically, 64- and 74-grade are commercial products; and 54-grade may or may not be Mil/Aero product.

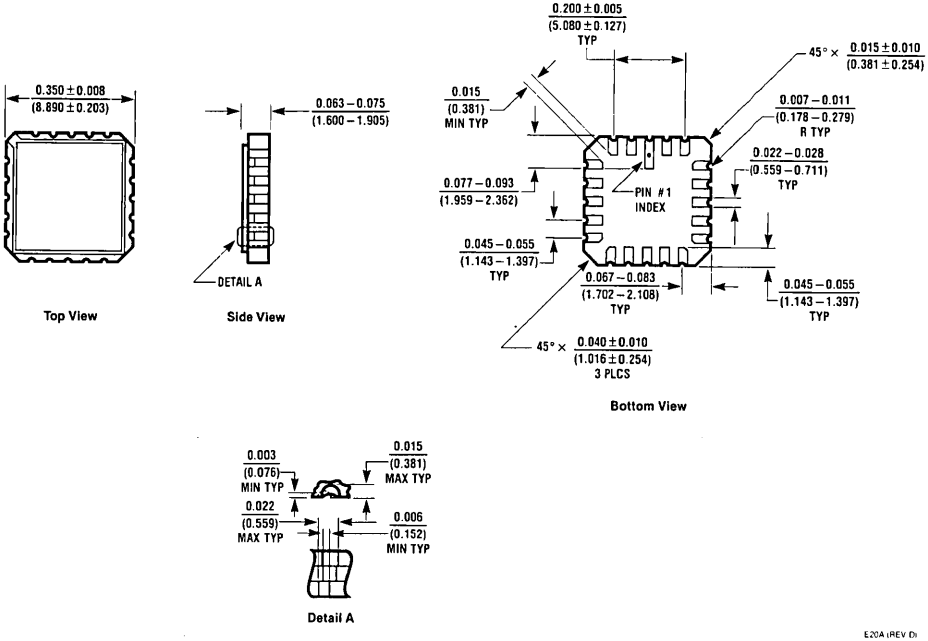
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows for ECL compatible CGS parts:



National Semiconductor

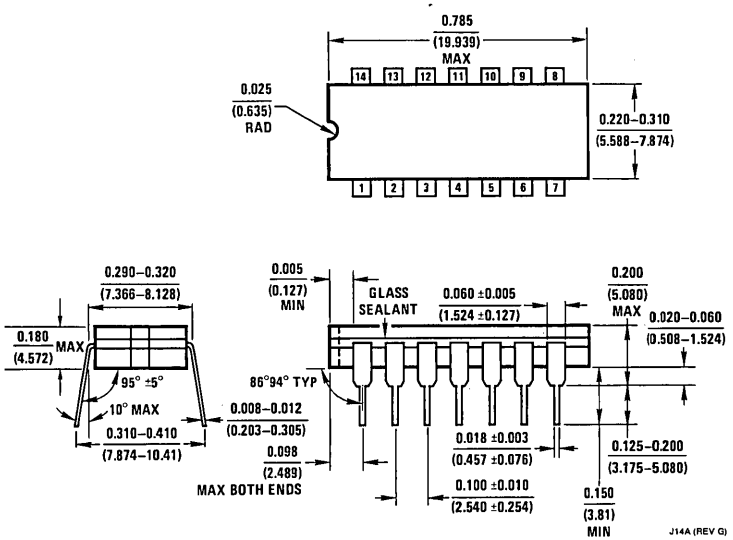
All dimensions are in inches (millimeters)

20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



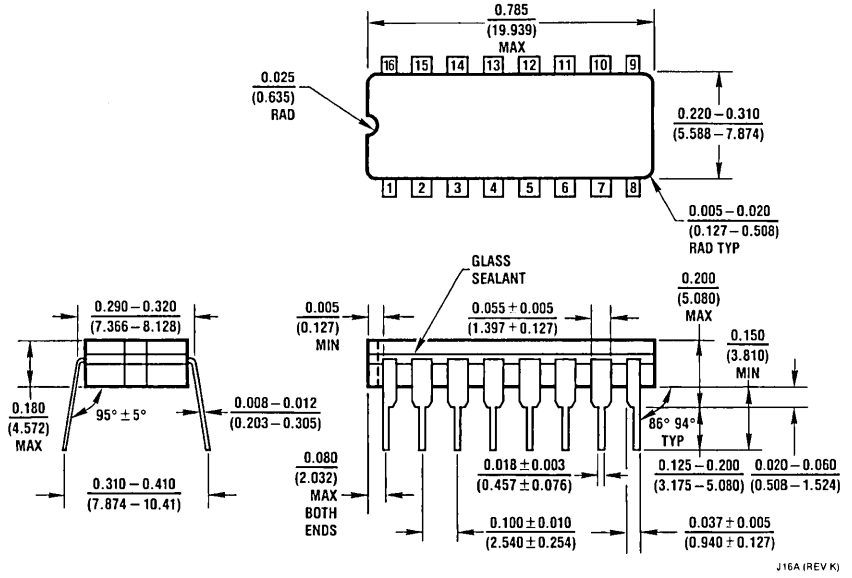
E20A (REV D)

14 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A



J14A (REV G)

16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



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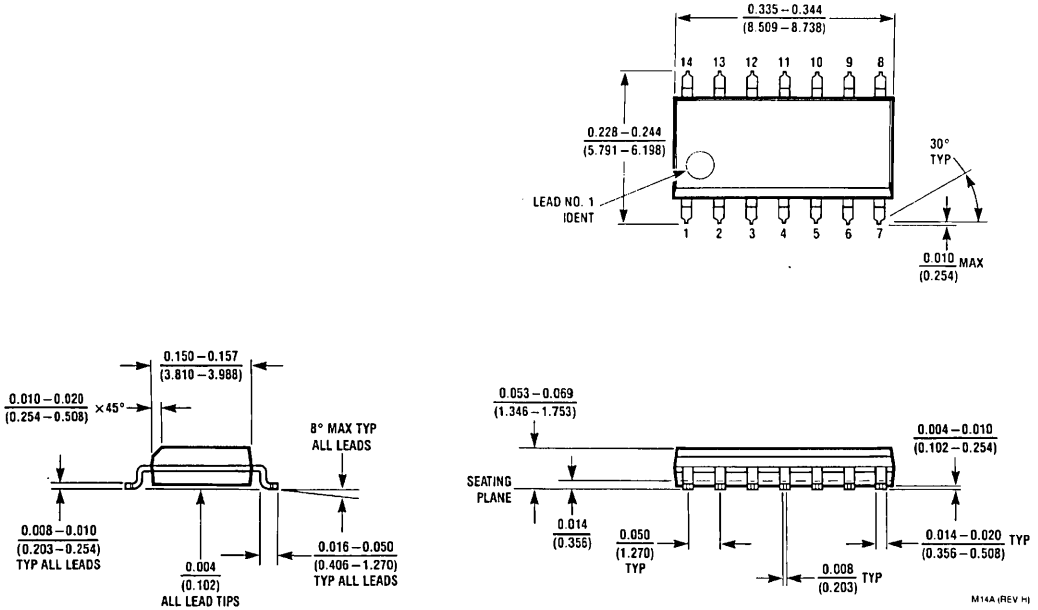
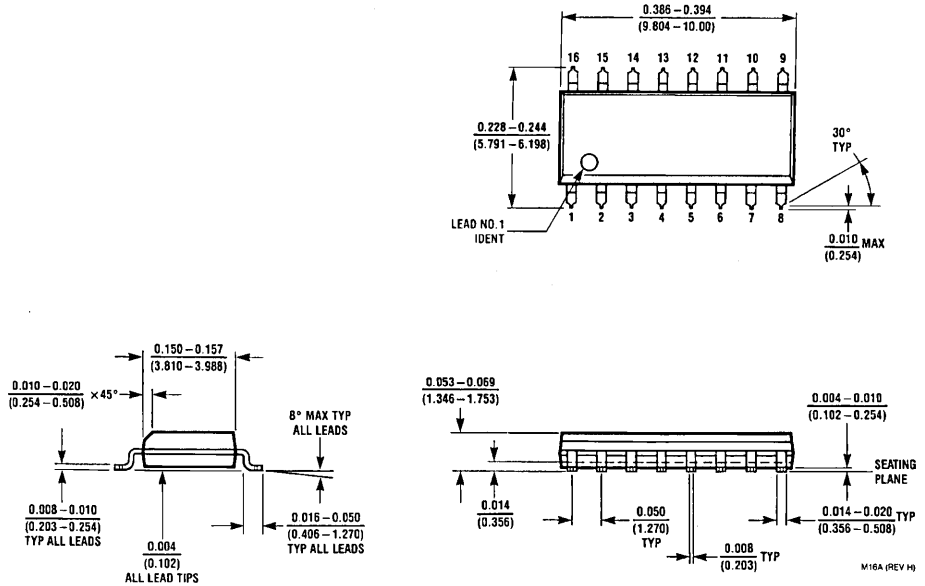
14 Lead Small Outline Integrated Circuit (S)
NS Package Number M14A



M14A (REV H)

16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A



14 Lead Plastic Dual-In-Line Package (P)
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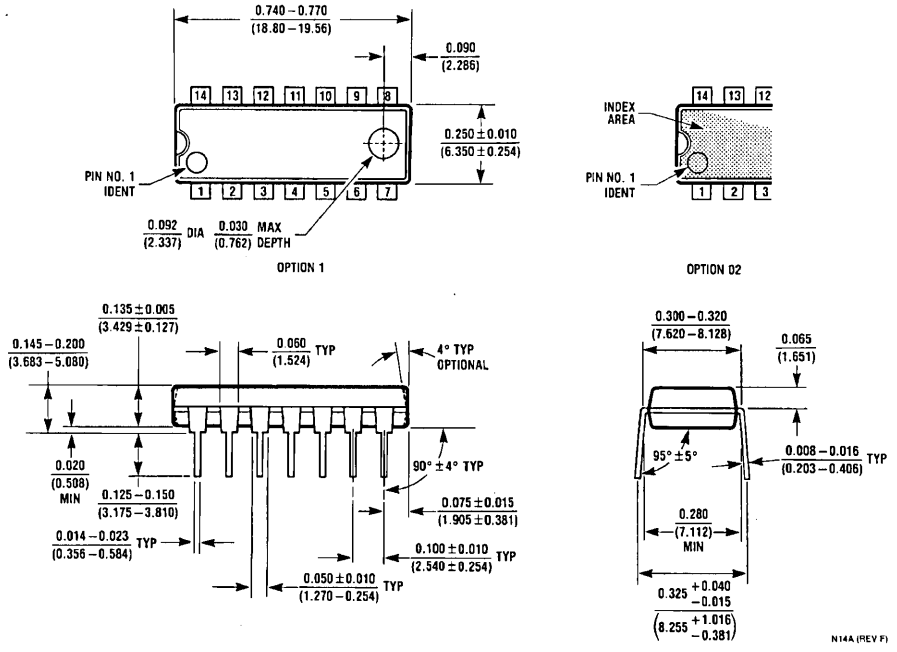
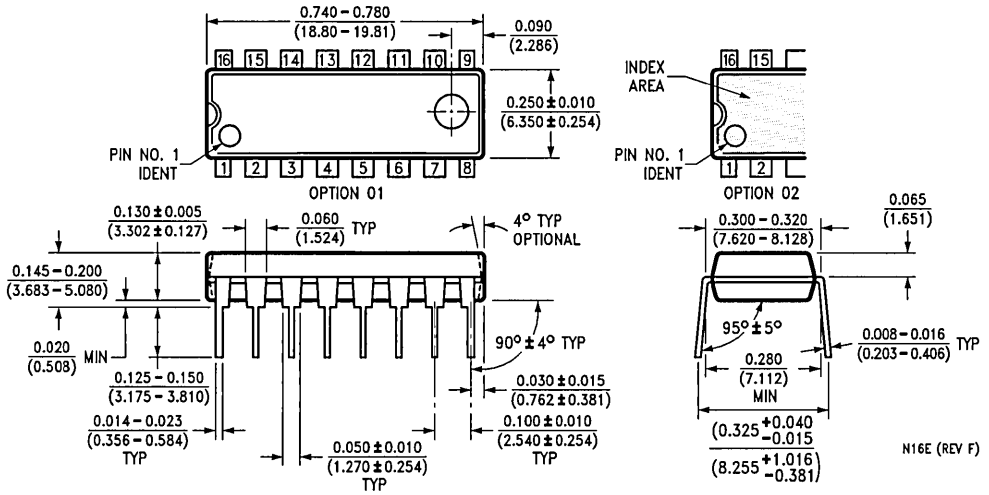
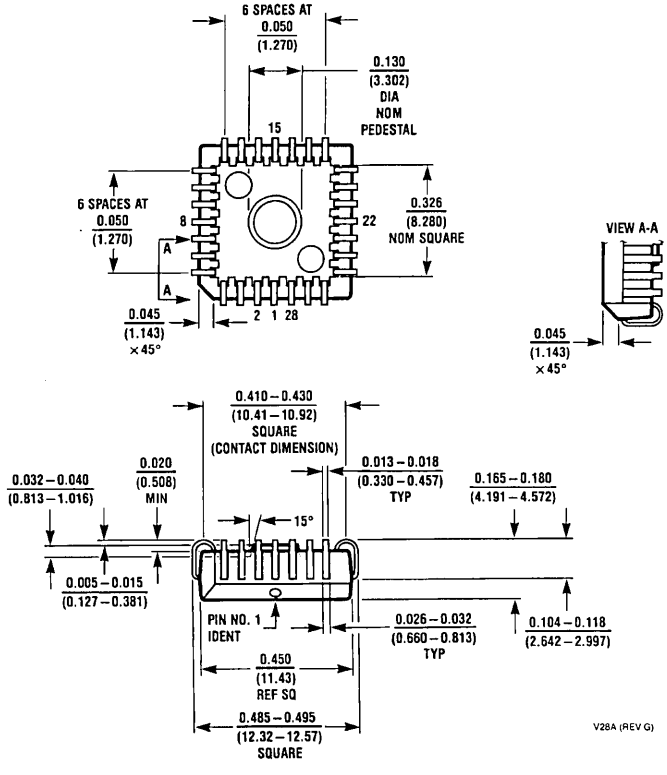


16 Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E



28 Lead Plastic Chip Carrier (Q)
NS Package Number V28A



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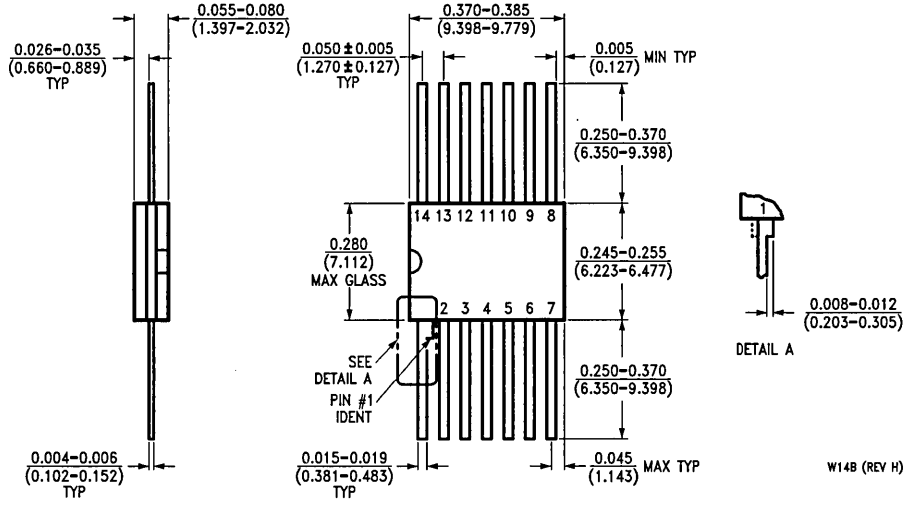
NS Package Number W14B



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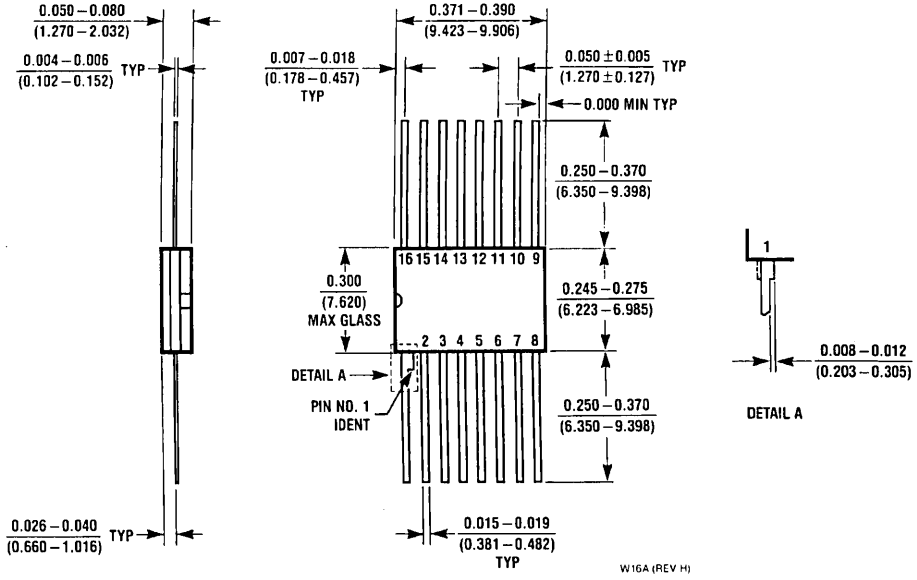

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