Section 2

Rigid Disk Data Separators/Synchronizers and ENDECs

Section 2 Contents

National Semiconductor

DP8461/65 Data Separator
DP8451/55 Data Synchronizer

General Description

DP8461/65

The DP8461/65 Data Separators are designed for applications in disk drive memory systems, and depending on system requirements, may be located either in the drive or in the controller. They receive digital pulses from a pulse detector circuit (such as the DP8464 Disk Pulse Detector) if situated in the drive, or from an ST506 type interface if situated in the controller. After locking on to the frequency of these input pulses, they separate them into synchronized data and clock signals. While in the non-read mode, both of these circuits employ a phase-frequency comparator to keep the VCO locked to the 2F input (this signal may be derived from a crystal or a servo track). The DP8465 switches to a phase only comparator when the read mode is entered. The DP8461 continues to use a phase-frequency comparator until the preamble detection circuit has detected two bytes of preamble. This feature thus restricts the DP8461 to use with codes employing the 1010 . . . preamble. MFM, and certain RLL Codes such as 1,7 and 1,8 employ such a preamble. If a Run Length Limited code is used or if the user wishes to do his own data separation, the synchronized data output is available to allow external circuitry to perform the data decoding function.

All of the digital input and output signals are TTL compatible and only a single +5V supply is required. The chip is housed in a narrow 24-pin dual-in-line package (DIP) and is fabricated using Advanced Schottky bipolar analog and digital circuitry. This high speed I.C. process allows the chip to work with data rates up to 20 Mbit/sec. There are two versions of the chip, each having a different decode window error specification. These two versions (−3, −4) are designed to operate from 2 to 20 Mbit/sec and are tested for their respective window tolerances, as specified in the Electrical Characteristics Table.

The DP8461/65 feature a phase-lock-loop (PLL) consisting of a phase-frequency comparator, pulse gate (to allow for phase-only operation in the read mode), charge pump, buffering amplifier, and voltage-controlled-oscillator (VCO). Pins are provided for the user to select the values of the external filtering components required for the VCO, and two current setting resistors for the charge pump. The DP8461/65 have been designed to be capable of locking onto the incoming preamble data pattern within the first two bytes, using an available high rate of charge pump current. Once lock-on has been achieved, the charge pump can be switched to a lower rate (both rates being determined by the external resistors) to improve bit-jitter immunity for the remainder of the read operation. At this time the READ CLOCK OUTPUT switches, without glitching, from half the 2F-CLOCK frequency to half the VCO CLOCK frequency. After lock-on, with soft sectored disks, the MISSING CLOCK DETECTED output indicates when a missing clock occurs so the controller can align byte boundaries to begin deserialization of the incoming data.

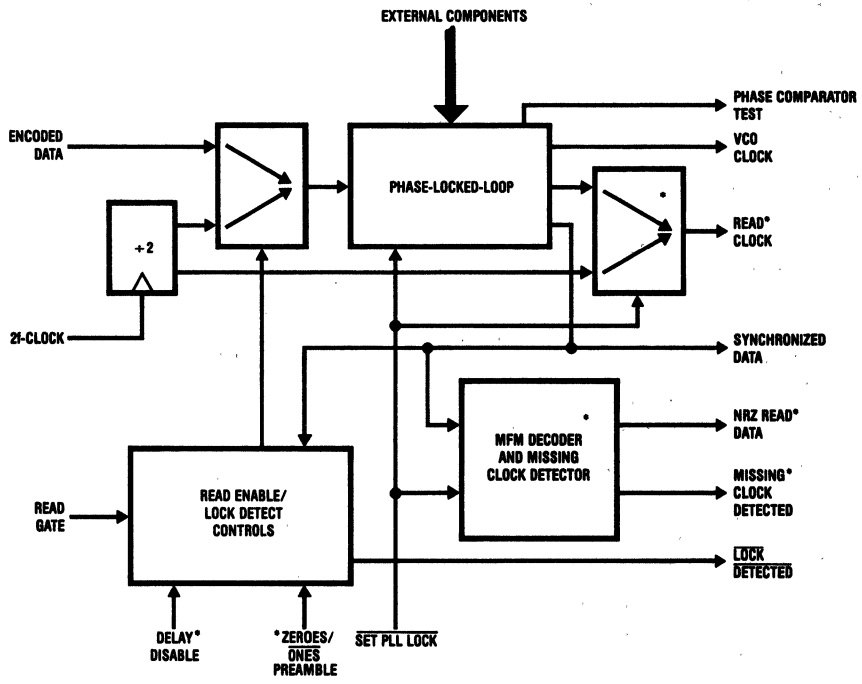
DP8451/55

The DP8451/55 perform the same data synchronization function of the DP8461/65 with no MFM related circuitry. As with the DP8461, the DP8451 continues in the phase-frequency comparison mode until two bytes of preamble are detected. The DP8451/55, which are packaged in 20 pin DIPs or 20-pin PCC's, exclude the READ CLOCK generating circuitry along with the MFM Decoder, Missing Clock Detector, and Read Enable Delay. Users who require only the SYNCHRONIZED DATA OUTPUT and VCO CLOCK OUTPUT can use the DP8451/55 as alternatives to the DP8461/65.

Features

- Operates at data rates up to 20 Mbit/sec
- Phase-Frequency comparison in non-read mode
- Phase-Frequency comparison in preamble—DP8461/51
- Separates MFM data into read clock and serial NRZ data (DP8461/65)
- 4 byte preamble-lock indication capability
- Preamble recognition of MFM encoded "0"s or "1"s
- User-determined PLL loop filter network
- PLL charge pump has two user-determined tracking rates
- External control of track rate switchover
- No glitch on READ CLOCK at switchover (DP8461/65)
- Synchronized data provided as an output (for RLL codes) (all four devices)
- ORed phase comparator outputs for monitoring bit-shift
- Missing clock detected for soft sectored disks
- Less then ½W power consumption
- Standard narrow 24-pin DIP or 28 pin Plastic Chip Carrier Package
- Single +5V supply

Simplified Block and Connection Diagrams



*Available only on DP8461/65

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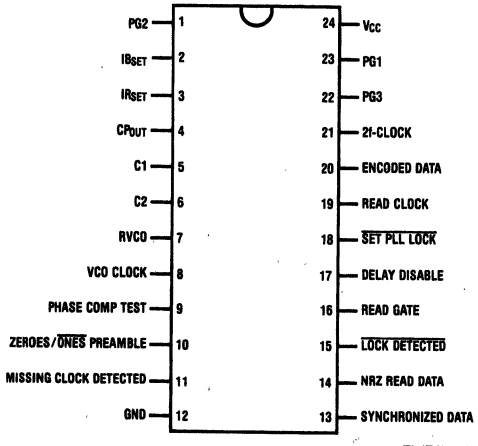
DP8461/65
Dual-In-Line Package

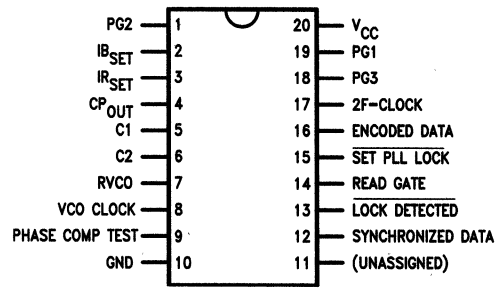


Top View

TL/F/8445–2

Order Number DP8461/65J or N
See NS Package Number J24F or N24C

DP8451/55
Dual-In-Line Package



Top View

TL/F/8445–3

Order Number DP8451/55N
See NS Package Number N20A

Pin Descriptions*

Power Supply

24 V_{CC} +5V ±5%

12 Ground

TTL Level Logic Inputs

16 READ GATE: This is an active high input signal that sets the DP8461/65 Data Separator into the Read Mode.

17 DELAY DISABLE: This input determines the delay from READ GATE going high to the time the DP8461/65 enters the Read Mode. If DELAY DISABLE is set high, this delay is within one cycle of the V_{CO}-CLOCK signal. If DELAY DISABLE is set low, the delay is thirty two-cycles of the VCO CLOCK, as shown in *Figure 1.*

18 $\overline{\text{SET PLL LOCK}}$: This input allows the user to control the on-chip PLL track rate. A high level at this input results in the PLL being in the high track rate. If this input is connected to the $\overline{\text{LOCK DETECTED}}$ output, the PLL will go into the low track rate mode immediately after lock is detected. A low level on this pin is also used to enable the MFM Decoder, the Missing Clock Detector, and to switch the Read Clock Multiplexer from half-2F-CLOCK to half-VCO.

10 ZEROES/$\overline{\text{ONES}}$ PREAMBLE: A high level on this input enables the MFM Decoder circuit to recognize an All Zeros data preamble. A low level results in the recognition of an All Ones data preamble.

20 ENCODED DATA: This input is connected to the output of the head amplifier/pulse-detecting network located in the disk drive. Each positive edge of the ENCODED DATA waveform identifies a change of flux on the disk. In the case of MFM encoded data, the input will be raw MFM.

21 2f-CLOCK: This is a system clock input, which is either a signal generated from the servo track (for systems utilizing servo tracks), or a signal buffered from a crystal. 2f CLOCK MUST ALWAYS BE APPLIED TO THIS INPUT FOR PROPER OPERATION.

TTL Level Logic Outputs

8 VCO CLOCK: This is the output of the on-chip VCO, transmitted from an Advanced Schottky-TTL buffer. It is synchronized to the MFM data output.

15 $\overline{\text{LOCK DETECTED}}$: This output goes active low only after both PLL Lock has occurred and 16 pulses of the preamble pattern have been recognized. It remains low until READ GATE goes inactive.

14 NRZ READ DATA: This is the NRZ (decoded MFM) data output, whose leading edges coincide with the trailing edge of READ CLOCK.

13 SYNCHRONIZED DATA: This output is the same encoded data that is input to the chip, but is synchronous with the negative edge of the VCO CLOCK.

11 MISSING CLOCK DETECTED: When an MFM missing clock is detected, this output will be a single pulse (of width equal to one cycle of READ CLOCK) occurring as shown in *Figure 2.*

19 READ CLOCK: This is half VCO CLOCK frequency when $\overline{\text{SET PLL LOCK}}$ is low; it is half 2f-CLOCK frequency at all other times. A deglitcher is utilized to ensure that no short clock periods occur during either switchover.

9 PHASE COMP TEST: This output is the logical "OR" of the Phase Comparator outputs, and may be used as a bit-shift indicator on for PLL analysis purpose.

Analog Signals

23, 22, PG1, PG3: The external capacitors and resistor of the Pulse Gate filter are connected to these pins. PG1 should be connected directly to the ground pin, pin 12.

1 PG2: This is the Pulse Gate current supply.

3 IRSET: The current into the rate set pin (V_{BE}/R_{RATE}) is used to set the charge pump output current for the low tracking rate.

2 IBSET: The current into the boost set pin (V_{BE}/R_{BOOST}) is used to set the amount by which the charge pump current is increased for the high tracking rate. (I_{INPUT} = I_{RATE} Set + I_{BOOST} Set).

4 CPOUT: CHARGE PUMP OUT/BUFFER AMP IN is available for connection of external filter components for the phase-lock-loop. In addition to being the charge pump output node, this pin is also the noninverting input to the Buffer Amplifier.

7 RVCO: The current at this pin determines the operating currents within the VCO.

5, 6 VCO C1, C2: An external capacitor connected between these pins sets the nominal VCO frequency.

*Pin Number Designations apply only to the DP8461/65. See Connection Diagram for DP8451/55.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
TTL Inputs	7V
Output Voltages	7V
Input Current (CPOUT, IRSET, IBSET, RVCO)	2 mA
Storage Temperature	−65°C to 150°C

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
T_A	Ambient Temperature		0	25	70	°C
I_{OH}	High Logic Level Output Current	VCO Clock Others			−2000 −400	μA
I_{OL}	Low Logic Level Output Current	VCO Clock Others			20 8	mA

Operating Conditions (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{DATA}	Input Data Rate		2.0		20	Mbit/sec
t_{WCK}	Width of 2f-CLOCK, High or Low		10			ns
t_{WPD}	Width of ENCODED DATA Pulse, (Note 2)	HIGH	5 ns + 0.10t			ns
		LOW	0.4t			
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level Input Voltage				0.8	V
t_{SETUP} (READ Gate)	Min. Amount of Time Which a Positive Edge of READ Gate Must Precede a Negative Edge of a VCO (Pin 8)		20			ns
t_{HOLD} (READ Gate)	Min. Time Required for a Positive Edge of a READ Gate to be Held after a Negative Edge of a VCO (Pin 8)		10			ns

DC Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min., I_{OH} = Max.	V_{CC}−2V	V_{CC}−1.6V		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = Max.			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V			−200	μA
I_O	Output Drive Current (Note 1)	V_{CC} = Max., V_O = 2.125V	−12		−110	mA
I_{CC}	Supply Current	V_{CC} = Max.			100	mA
I_{OUT}	Charge Pump Output Current	500 μA ≤ I_{RSET} + I_{BSET} ≤ 2000 μA 200 μA ≤ I_{RSET} + I_{BSET} < 500 μA	I_{TYP} − .18 (I_R + I_B) − 30 μA I_{TYP} − .08 (I_R + I_B) − 80 μA	1.95 (I_{RSET} + I_{BSET}) − 70 μA 1.95 (I_{RSET} + I_{BSET}) − 70 μA	I_{TYP} + .18 (I_R + I_B) + 30 μA I_{TYP} + .08 (I_R + I_B) + 80 μA	μA

Note 1: This value has been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

Note 2: t is defined as the period of the encoded MFM data, or two times the VCO period.

AC Electrical Characteristics Over Recommended V_{CC} and Operating Temperature Range.

(All Parts unless stated otherwise) (t_R = t_F = 2.0 ns, V_{IH} = 3.0V, V_{IL} = 0V)

Symbol	Parameter	Min	Typ	Max	Units
t_{READ}	Positive READ CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE low)		16	17	—
t_{READ}	Positive READ CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE high)		1	1	—
$t_{DECODE\ NRZ}$	Number of READ CLOCK cycles required to output each decoded MFM data bit (Note 3, 4)	—	2	3	T-clock
$t_{TRANSMIT\ MFM}$	Positive READ CLOCK transitions required to transmit input MFM to output	1	2	3	—

Note: For Further Information Refer to Application Notes AN-414, AN-415, and AN-416.

AC Electrical Characteristics Over Recommended V_{CC} and Operating Temperature Range. (Continued)

(All Parts unless stated otherwise) ($t_R = t_F = 2.0$ ns, $V_{IH} = 3.0V$, $V_{IL} = 0V$)

Symbol	Parameter	Min	Typ	Max	Units
$t_{READ\ ABORT}$	Number of READ CLOCK cycles after READ GATE set low to read operation abort			2	T-clock
t_{WINDOW}	Variance of center of decode window from nominal (Note 7) DP84XX-3 / DP84XX-4			6 / 10	ns
$\phi_{LINEARITY}$	Phase range for charge pump output linearity (Note 2)	$-\pi$		$+\pi$	Radians
K_1	Phase Comparator—Charge Pump gain constant (Note 5) ($N = f_{VCO}/f_{INPUT\ DATA}$, $2 \le N \le 4$ for MFM)		$\frac{1.78V_{BE}}{N2\pi R}$		Amps/rad
$V_{CONTROL}$	Charge pump output voltage swing from nominal		± 100		mV
K_{VCO} ($=A \times K_2$)	VCO gain constant (ω_{VCO} = VCO center frequency in rad/s) (Note 1, 6)	$\frac{1.20\omega_C}{V_{BE}}$	$\frac{1.40\omega_C}{V_{BE}}$	$\frac{1.60\omega_C}{V_{BE}}$	rad/sec. V
f_{VCO}	VCO center frequency variation over temperature and V_{CC}	-5		$+5$	%
$f_{MAX\ VCO}$	VCO maximum frequency		60		MHz
t_{HOLD}	Time READ CLOCK is held low during changeover after lock detection has occurred (Note 3)			1½	T-clock
t_{PHL}	Prop. Delay. VCO Neg. Edge to Synchronized Data Neg. Edge		15	30	ns
t_{PLH}	Prop. Delay. VCO Negative Edge to Synchronized Data Positive Edge		10	25	ns
$t_{2F/RC}$	Delay from 2F positive edge to READ CLOCK positive on negative edge ($\overline{\text{SET PLL LOCK}}$ high)	10		35	ns

Note 1: A sample calculation of frequency variation vs. control voltage: $V_{IN} = \pm 0.1V$;

$$K_{VCO} = \frac{\omega OUT}{V_{IN}} = \frac{0.4\omega_C}{0.2V} = \frac{2.0\omega_C}{V} \frac{(rad/sec)}{(volt)}$$

Note 2: $-\pi$ to $+\pi$ with respect to 2f VCO CLOCK

Note 3: T-clock is defined as the time required for one period of the READ CLOCK to occur.

Note 4: This number remains fixed after PLL Lock occurs.

Note 5: With respect to VCO CLOCK; $I_{PUMP\ OUT} = 1.9\ I_{SET}$

$$I_{SET} = \frac{V_{BE}}{R_{SET}}$$

Note 6: Although specified as the VCO gain constant, this is the gain from the Buffer Amplifier input to the VCO output.

Note 7: This specification is guaranteed only for the conditions under which the parts were tested. However, significant variation from the formula is not expected for other data rates and filters. The filter values below were chosen for operation in an automatic test system (static window) environment. Different criteria may apply for choosing filter values in a disk system. See Loop Filter section for sample calculations of other filter values.

Static Window Margin Test Loop Filter Component Values

Part Type	Data Rate Tested	C_1	C_2	R_1	R_{RATE}	R_{BOOST}
DP8451/55/61/65-4	5 Mbit/Sec	0.02 μF	150 pF	200Ω	750Ω	1.6 kΩ
DP8451/55/61/65-3	10 Mbit/Sec	.082 μF	1600 pF	27Ω	820Ω	619Ω

External Component Selection (All Parts) (Note 1)

Symbol	Component	Min	Typ	Max	Units
R_{VCO}	VCO Frequency Setting Resistor (Note 2)	990		1010	Ω
C_{VCO}	VCO Frequency Setting Capacitor (Note 3, 4)	20		245	pF
R_{RATE}	Charge Pump I_{RATE} Set Resistor (Note 6)	0.4		4.0	kΩ
R_{BOOST}	Charge Pump (High Rate) I_{BOOST} Resistor (Note 6)	0.5		∞	kΩ
C_R	I_{RATE} Bypass Capacitor (Note 5)	.01			μF
C_B	I_{BOOST} Bypass Capacitor (Note 5)	.01			μF

Note 1: External component values for the Loop Filter and Pulse Gate are shown in tables 1 & 2.

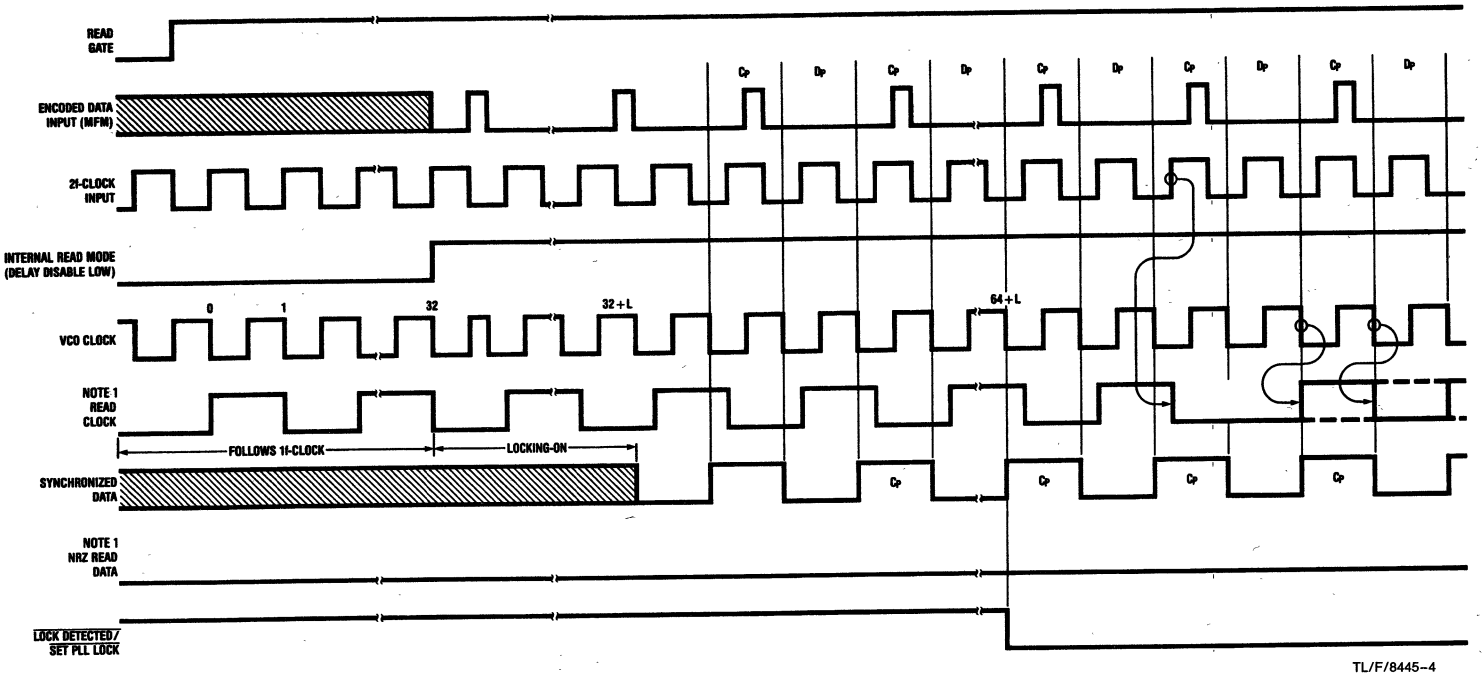
Note 2: A 1% Component Tolerance is Required.

Note 3: These MIN and MAX values correspond to the MAX and MIN data rates respectively.

Note 4: The Component Tolerance is system dependent on how much center frequency deviation can be tolerated.

Note 5: Component Tolerance 15%.

Note 6: The minimum value of the parallel combination of R_{RATE} and R_{BOOST} is 350Ω.



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Note 1: Not included on the DP8451/55.

C_P, D_P = preamble clock and preamble data bits respectively.

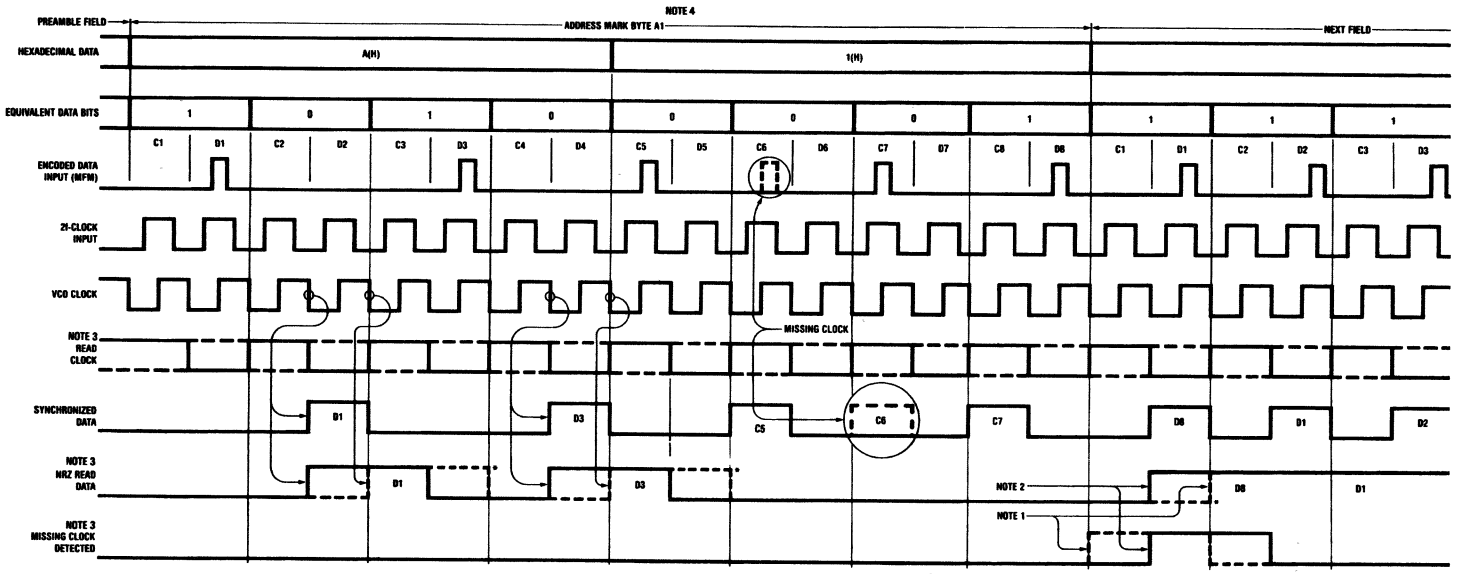
L = Number of 2f-clock cycles required for VCO to lock, determined by external loop filter component values

At 32 + L, VCO has just locked.

At 64 + L, circuit has confirmed lock (has been in lock for 16 MFM clock bits). This sequence shows the MFM all-zeros preamble pattern.

For DP8451/55 delay disable does not exist and part functions as if this input is always high.

FIGURE 1. Lock-on Sequence Waveform Diagram



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* READ CLOCK and NRZ READ DATA may be delayed by one VCO clock period depending on the phase of the internal clock at activation of READ GATE input.

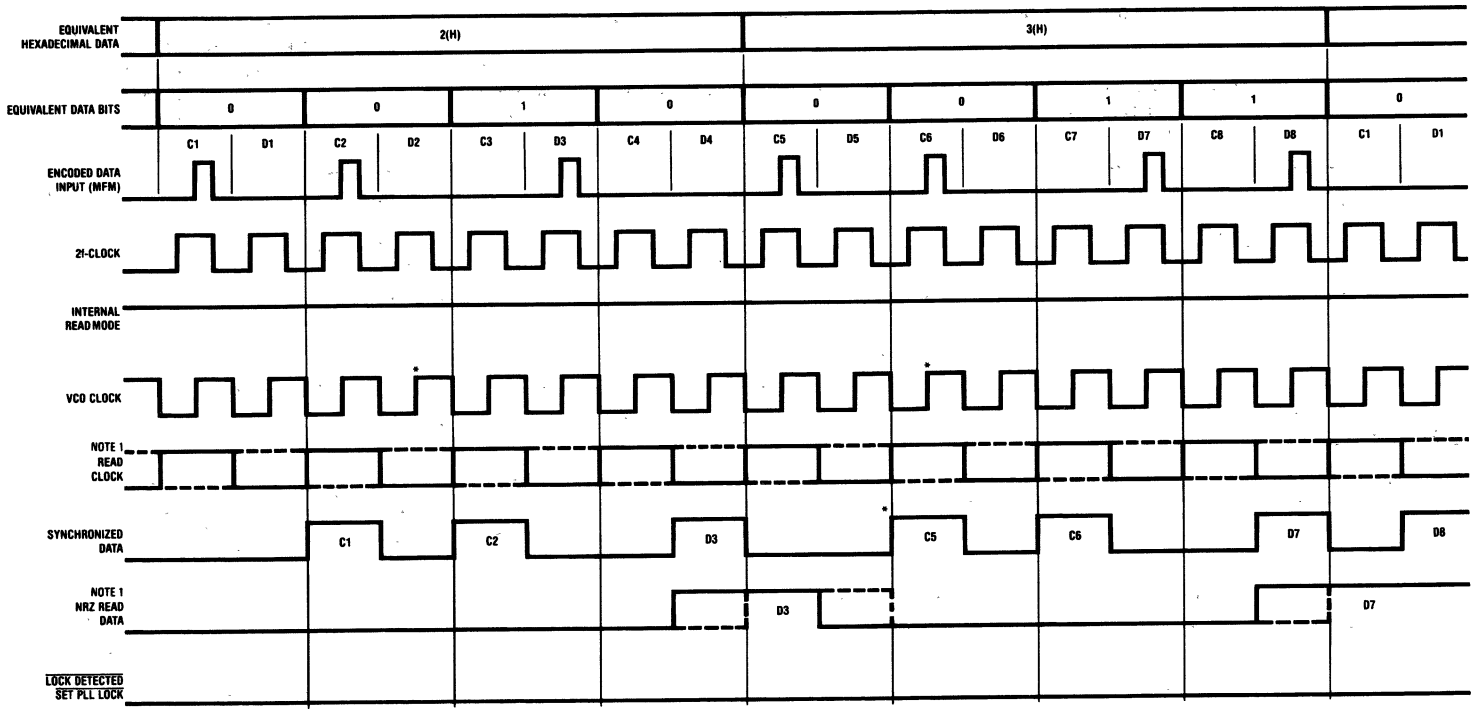
① MISSING CLOCK DETECTED is one READ CLOCK period ahead of the chip issuing D8 on the NRZ READ DATA output when READ CLOCK is delayed by one VCO clock period.

② MISSING CLOCK DETECTED is synchronous with the chip issuing D8 on the NRZ READ DATA Output when READ CLOCK is not delayed.

③ Not included on the DP8451/55.

④ The AI byte is shown only as an example address mark byte. *Any* missing clock bit which is framed by two existing clock bits will produce a missing clock detected pulse.

FIGURE 2. Missing Clock Detection Waveform Diagram



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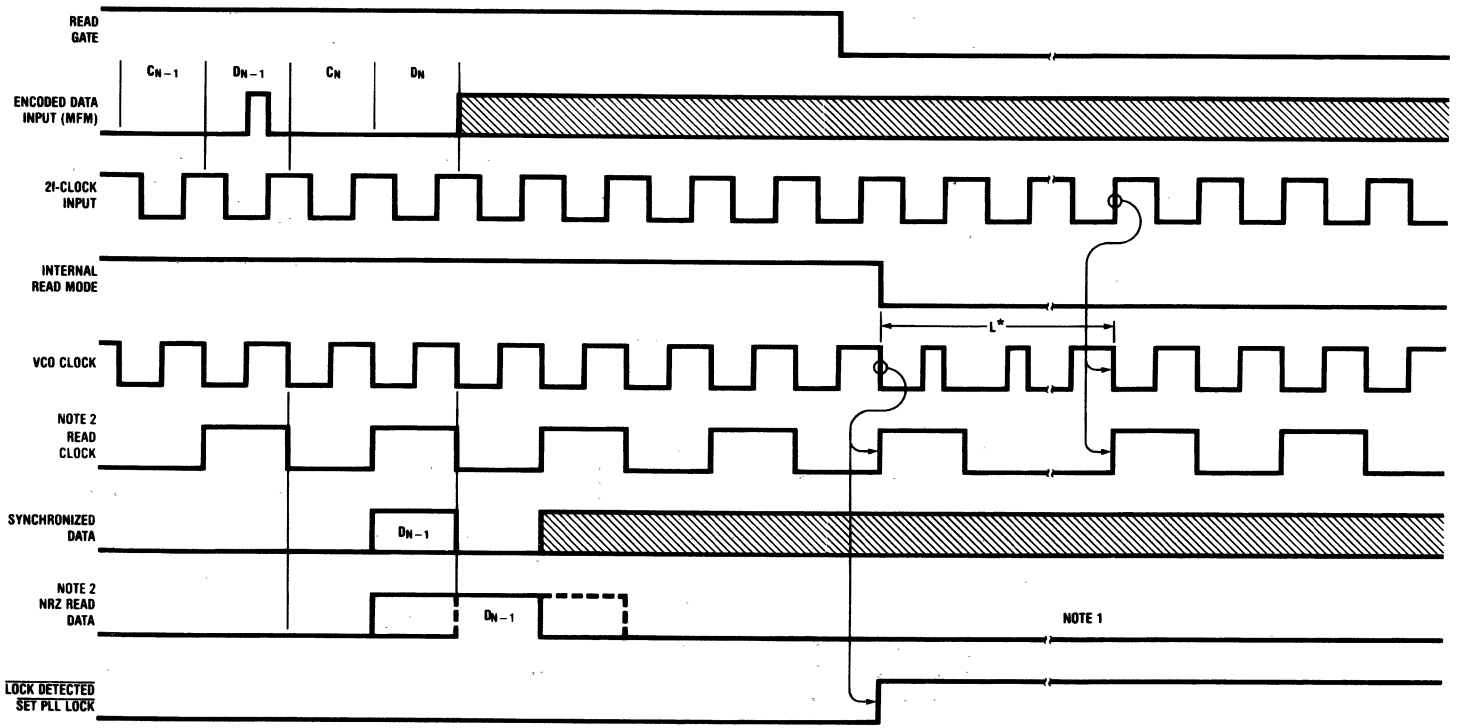
* **READ CLOCK and NRZ READ DATA may be delayed by one VCO clock period with respect to Synchronized Data depending on the phase of the internal clock at activation of READ GATE input.**

Note 1: Not included on the DP8451/55.

FIGURE 3. Locked-On Waveform Diagram



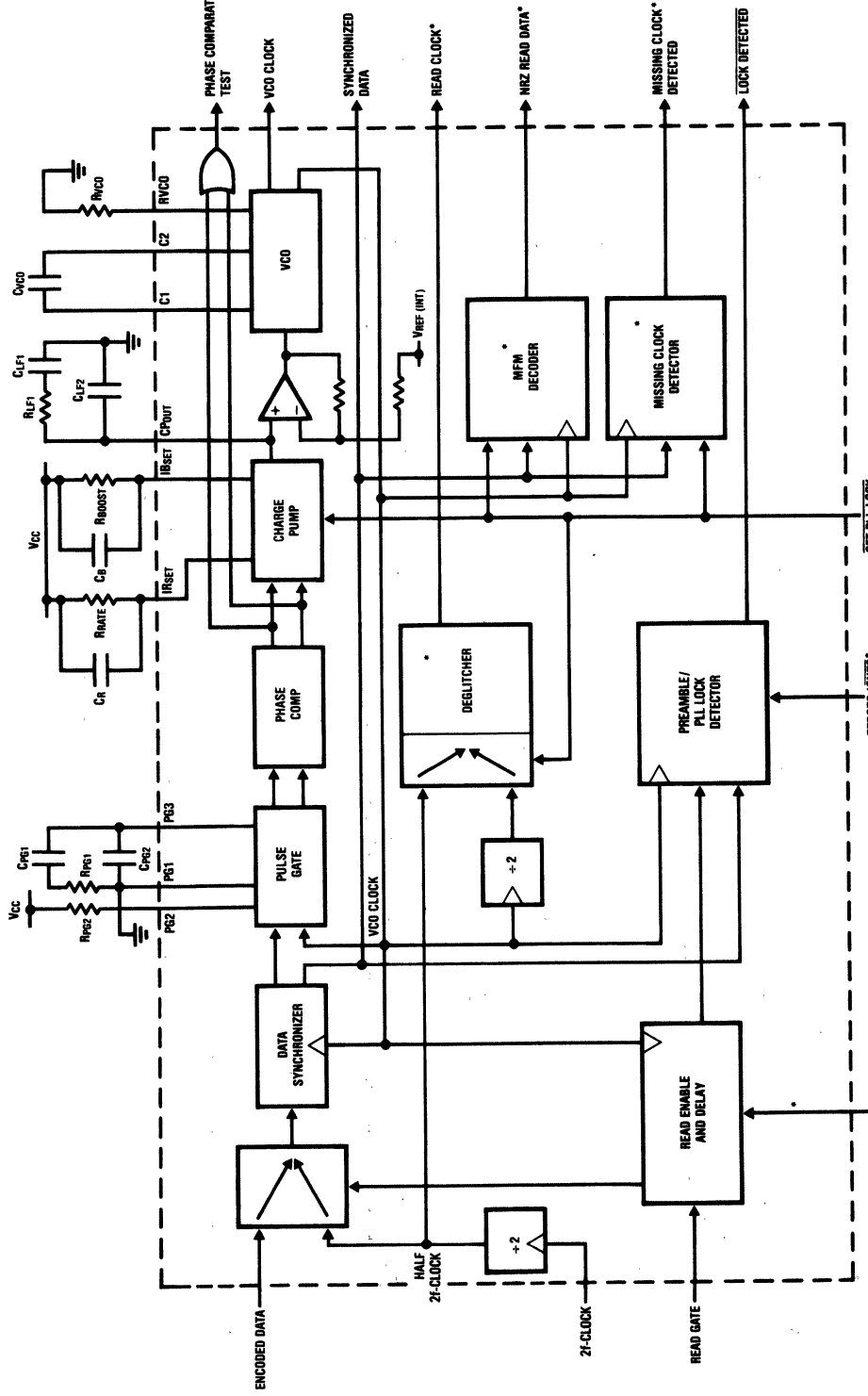
* **L indicates the number of cycles required for the VCO to lock to the 2f-CLOCK.**

Note 1: READ GATE going low will always result in NRZ READ DATA going low regardless of the state of the last bit.

Note 2: Not included on the DP8451/55.

FIGURE 4. Lock-Ending Sequence Waveform Diagram

Detailed Block Diagram



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*Not included on the DP8451/55

Circuit Operation

When the READ GATE input goes high, the DP8461/65 will enter the read mode after a period determined by the state of the DELAY DISABLE pin. This may be either one or thirty two VCO CLOCK cycles. Once in the read mode the DP8465 switches from using a phase-frequency comparator to a phase-only comparator, i.e. the pulse gate is activitated. At this time, however, the DP8461 continues to use a phase-frequency comparator. Referring to *Figure 1*, as the read mode is entered, the phase-locked-loop reference signal is switched from 2F-CLOCK INPUT to the ENCODED DATA. The PLL, initially in the high-tracking rate mode, then attempts to lock onto the incoming encoded data stream. As soon as two bytes of the selected preamble are detected, (the selection is determined by the ZEROES/$\overline{\text{ONES}}$ PREAMBLE pin) the $\overline{\text{LOCK DETECTED}}$ OUTPUT goes low. At this time the DP8461 switches from using a phase-frequency comparator to using the pulse gate, thus beginning phase only comparisons. In a typical MFM disk drive application, the $\overline{\text{LOCK DETECTED}}$ OUTPUT is directly connected to the $\overline{\text{SET PLL LOCK}}$ INPUT. With this connection, track rate selection, clock output switchover, and data output enabling will occur after two consecutive preamble bytes have been detected by the chip. Typically it takes less than one byte time for the VCO to lock to the data sufficiently for preamble detection to begin following the start of the Read operation.

A low level on the $\overline{\text{SET PLL LOCK}}$ causes the PLL Charge Pump to switch from the high to low tracking rate. At the same time, the source of the READ CLOCK signal is switched from half the frequency of the 2F-CLOCK to half the VCO CLOCK. The MFM decoder also becomes enabled and begins to output decoded NRZ data. If a zeroes data preamble is present, the NRZ READ DATA OUTPUT will remain low until the end of the preamble. It will then output whatever NRZ data is present after the preamble field has ended, as shown in *Figures 2* and *3*.

When the READ GATE goes low, signifying the end of a read operation, the DP8461/65 will return to phase-frequency comparator operation. *Figure 4* shows the sequence when READ GATE goes low. The PLL reference signal is switched back to half the 2F-CLOCK and the $\overline{\text{LOCK DETECTED}}$ OUTPUT (and therefore the $\overline{\text{SET PLL LOCK}}$ INPUT) goes high. The PLL then returns to the high track rate, and the output signals return to their initial conditions. The 2F-CLOCK MUST BE APPLIED AT ALL TIMES to the DP8461/65 and DP8451/55 for proper operation.

Since the DP8461/51 employs a phase-frequency comparator until two bytes of the preamble (actually any 16 pulses within a 1010 . . . pattern) have been detected, care must be taken to ensure that when using this circuit the READ GATE is applied only within a field containing the 1010 . . . pattern. In soft sectored drives the head may be positioned anywhere on the track when initiating a read operation. Therefore, either a controller which only issues READ GATE when a high frequency synchronization field is present, or a simple external circuit between the controller and DP8461/51 to qualify the READ GATE, must be used.

CIRCUIT DESCRIPTION

1. Read Enable and Delay (DP8461/65 only): If the DELAY DISABLE input is connected low, then thirty two VCO CLOCK cycles after READ GATE goes active, the DP8461/65 will go into the read mode. If the DELAY DISABLE input is connected high, the chip will go into the read mode one VCO CLOCK cycle after READ GATE goes active. (The 32 cycle delay is permanently disabled in the DP8451/55).

2. Pulse Gate, including Multiplexer and Data Synchronizer: The Input Multiplexer selects the input to the phase-lock-loop. While the chip is in the bypassed (non-read) mode, the VCO frequency is phase and frequency locked to the 2F-CLOCK INPUT frequency. In the read mode the Input Multiplexer switches to the ENCODED DATA signal and the VCO CLOCK then begins to synchronize with the ENCODED DATA signal. Also, as soon as the read mode is entered, the DP8455/65 cease phase and frequency comparisons by employing the Pulse Gate.

In the DP8461/51 option, switchover from the phase-frequency comparator to the pulse gate (phase-only comparator) occurs after two bytes of the 1010 . . . pattern have been detected by the preamble pattern detector.

The Pulse Gate allows a reference pulse from the VCO into the Phase Comparator only after an ENCODED DATA bit has arrived. It utilizes a scheme which delays the incoming data by one-half the period of the 2F-CLOCK. This optimizes the position of the decode window and allows input jitter of approximately half the 2F-CLOCK period. The decode window error can be determined from the specification in the Electrical Characteristics Table.

3. Phase Comparator: The Phase Comparator receives its inputs from the Pulse Gate, and is edge-triggered from these inputs to provide charge-up and charge-down outputs.

4. Charge Pump: The high speed charge pump consists of a switchable constant current source and sink. The charge pump constant current is set by connecting external resistors to V_{CC} from the charge current rate set (IRSET) and current boost set (IBSET) pins. Before lock is indicated, the PLL is in the high tracking rate and the parallel combination of the resistors determines the current. In the low tracking rate after lock-on, only the IRSET resistor determines the charge pump current. The output of the charge pump subsequently feeds into external filter components and the Buffer Amplifier.

5. Buffer Amplifier: The input of the Buffer Amplifier is connected to the charge pump's constant current source/sink output as well as the external Loop Filter components. The Buffer Amplifier is configured as a high input impedance amplifier which allows for the connection of external PLL filter components to the Charge Pump output pin CPOUT. The output of the Buffer Amplifier is internally connected to the VCO control input.

6. VCO: The Voltage-Controlled-Oscillator requires a resistor from the RVCO pin to ground and a capacitor between pins C1 and C2, to set the center frequency. The VCO frequency can be varied from nominal by approximately ±20%, as determined by its control input voltage.

7. PLL Lock-on/Preamble Pattern Detector: To recognize preamble, the preamble pattern from the disk must consist exclusively of either MFM data bit zeroes (encoded into ..10.. MFM clock pulses) when the ZEROES/$\overline{\text{ONES}}$ PREAMBLE pin is set high, or MFM data bit ones (encoded into ..01.. MFM pulses) when set low (DP8461/65 only). The preamble pattern must be long enough to allow the PLL to lock, and subsequently for the Preamble Pattern Detector circuit to detect two complete bytes.

Once the chip is in the read mode, the VCO proceeds to lock on to the incoming data stream. The Preamble Pattern

Circuit Operation (Continued)

Detector then searches for a continuous pattern of 16 consecutive pulses at one-half the VCO frequency to indicate lock has been achieved.

The $\overline{\text{LOCK DETECTED}}$ output then goes low. At this time, in the DP8461/51 option, the PLL switches from using a phase-frequency comparator to employing a pulse gate and thus doing only phase comparisons. Any deviation from the above-mentioned one-zero pattern at any time before PLL Lock is detected will reset the PLL Lock Detector. The lock detection procedure will then start again.

8. MFM Decoder (DP8461/65 only): The MFM Decoder receives synchronized MFM data from the Pulse Gate and converts it to NRZ READ DATA. For run-length-limited codes the MFM Decoder and Missing Clock Detector will not be used.

9. Missing Clock Detector (DP8461/65 only): This block is only required for soft-sectored drives, and is used to detect a missing clock violation of the MFM pattern. The missing clock is inserted when writing to soft-sectored disks to indicate the location of the Address Mark in both the ID and the Data fields of each sector. Once PLL Lock has been indicated, the Missing Clock Detector circuit is enabled. MISSING CLOCK DETECTED will go active if at any time the incoming data pattern contains one suppressed clock bit framed by two adjacent clock bits. (This condition is not constrained to any particular byte pattern such as "A1.") The output signal goes high for one cycle of READ CLOCK.

10. Clock Multiplexer and Deglitcher (DP8461/65 only): When the $\overline{\text{SET PLL LOCK}}$ input changes state this circuit switches the source of the READ CLOCK signal between the half 2f-CLOCK frequency and the half VCO CLOCK frequency. A deglitcher circuit is utilized to ensure that no short clock periods occur during either switchover.

BIT JITTER TOLERANCE

The spec, t-window, as defined in the AC Electrical Characteristics table, describes the distance from the optimum window boundary a single shifted data bit may be placed (following complete PLL lock and stabilization) before it risks being interpreted as residing in the adjacent synchronization window. This is known as the **static window measurement**, which combines all contributing factors of window jitter and displacement within the data separator into a single specification.

The two options of the DP8451/55/61/65, the −4 and −3 offer decreasing static window errors (respectively) so that the parts may be selected for different data rates (up to 20 Mbit/sec). The −4 part will be used in most low data rate applications. As an example, at the 5 Mbit/sec MFM data rate of most 5¼ inch drives, the chip contributes up to ±10 ns of window error, out of the total available window of 100 ns. This allows the disk drive to have a margin of 40 ns of jitter from nominal bit position before an error will occur.

ANALOG CONNECTIONS

External passive components are required for the Pulse Gate, Charge Pump, Loop Filter and VCO as shown in *Figure 5*. The information provided here is for guidelines only. The user should select values according to his own system requirements. Phase-Locked Loops are complex circuits that require detailed knowledge of the specific system. Factors such as loop gain, stability, response to change of signal, lock-on time, etc are all determined by the external components. In many disk systems these factors are critical, and National Semiconductor recommends the designer be knowledgeable of phase-locked-loops, or seek the advice of an expert. Inaccurate design will probably result in excessive disk error rates. The phase-locked-loop in the DP8461/65 has many advantages over all but the most sophisticated discrete designs, and if the component values are selected correctly, it will offer significant performance advantages. This should result in a reduction of disk error rates over equivalent discrete designs. Please refer to the National Semiconductor Application Note AN-414, Precautions for Disk Data Separator Designs, AN-415, Designing with the DP8461, AN-416, Designing with the DP8465, and to the Disk Interface Design Guide and User's Manual, Chapter 1.

Circuit Operation (Continued)

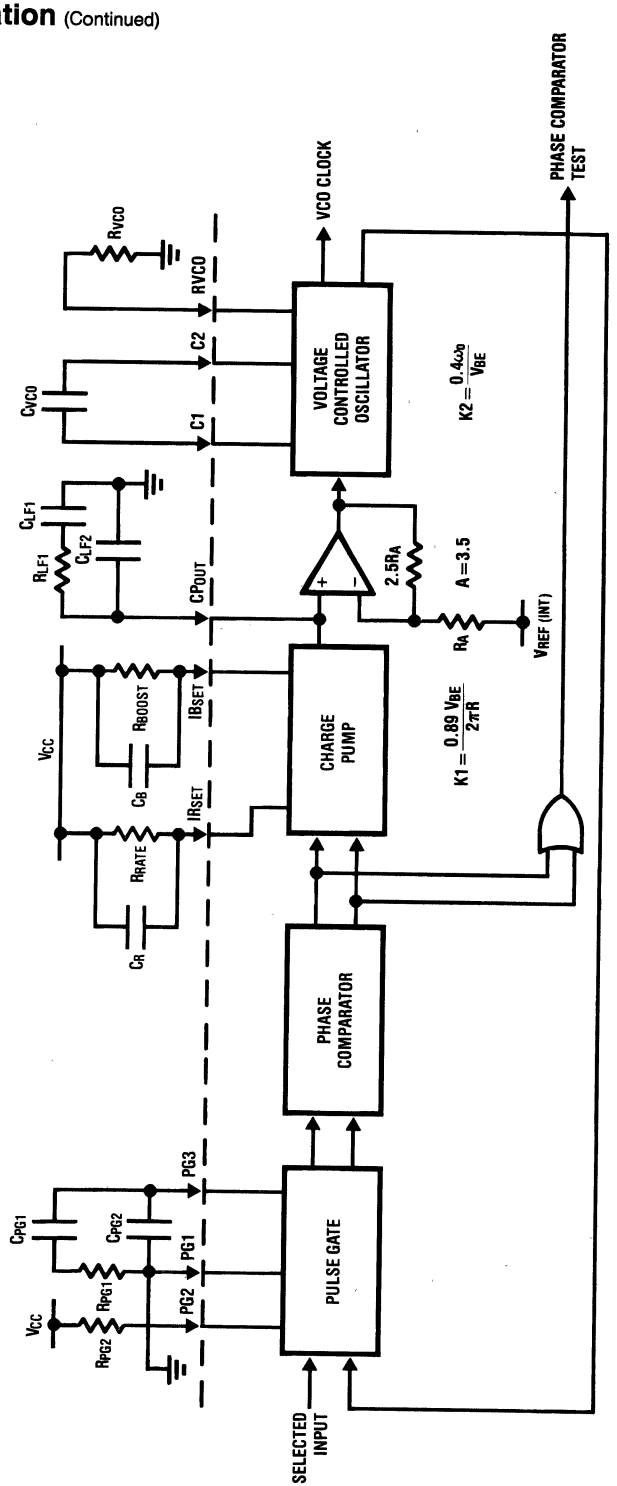

FIGURE 5. Phase-Locked-Loop Section

2

Circuit Operation (Continued)

Pulse Gate

There are four external components connected to the Pulse Gate as shown in *Figure 6* with the associated internal components. The values of R_{PG1}, R_{PG2}, C_{PG1}, and C_{PG2} are dependent on the data rate. C_{PG1} and C_{PG2} are proportional to the data rate, while R_{PG1} and R_{PG2} are inversely proportional. Table I shows component values for the data rates given. Component values are calculated by selecting R_{PG2} from Table I. Next calculate

$$C_{PG1} = \left(\frac{2.12 \times 10^5}{890 + R_{PG2}}\right)\left(\frac{1}{100 \times R_S}\right)^2$$

$$C_{PG2} = \frac{1}{10} C_{PG1}, \text{ and } R_{PG1} = \left(\frac{890 + R_{PG2}}{2.38 \times 10^5}\right)(100 \times R_S).$$

In the above equations R_S is the rotational speed and, for 3600 RPM, R_S = 60 Hz. A rotational speed of 3600 RPM was assumed for the calculations in Table I. For data rates not listed, R_{PG2} may be approximated as (30 kΩ/f_{DATA}) − 1.20 kΩ = R_{PG2} where f_{DATA} is the data rate in Megabits/second.

TABLE I. Pulse Gate Component Selection Chart
Components with 10% tolerance will suffice

Data Rate	R_{PG2}	R_{PG1}	C_{PG1}	C_{PG2}
2 Mbit/sec	15 kΩ	430Ω	.39 μF	.039 μF
5 Mbit/sec	4.7 kΩ	150Ω	1 μF	0.1 μF
10 Mbit/sec	1.8 kΩ	68Ω	2.2 μF	.22 μF
15 Mbit/sec	750Ω	39Ω	3.9 μF	.39 μF

Charge Pump

Resistors R_{RATE} and R_{BOOST} determine the charge pump current. The Charge Pump bidirectional output current is approximately 1.9 × the input current (See DC Electrical Characteristics for exact relationship). In the high tracking rate with $\overline{\text{SET PLL LOCK}}$ high, the input current is I_{BSET} + I_{RSET}, i.e., the sum of the currents through R_{BOOST} and R_{RATE} from V_{CC}. In the low tracking rate, with $\overline{\text{SET PLL LOCK}}$ low, this input current is I_{RSET} only.

A recommended approach for selecting values for R_{RATE} and R_{BOOST} is described in the design example in the Loop Filter Section. A typical loop gain change of 2:1 for high to low tracking rate would require R_{BOOST} = R_{RATE}. Selecting R_{RATE} to be 820Ω would then result in R_{BOOST} equaling 820Ω. Referring to *Figure 7*, the input current is effectively V_{BE}/R_{RATE} in the low tracking rate, where V_{BE} is an internal voltage. This means that the current into or out of the loop filter is approximately (1.95 × V_{BE}/820) − 70 μA = 1.72 mA. Note that although it would seem the overall gain is dependant on V_{BE}, this is not the case. The VCO gain is altered internally by an amount inversely proportional to V_{BE}, as detailed in the section on the Loop Filter. This means that as V_{BE} varies with temperature or device spread, the gain will remain constant for a particular fixed set of values of R_{RATE} and R_{BOOST}. This alleviates the need for potentiometers to select values for each device. The tolerance required for these two resistors will depend on the total loop gain tolerance allowed, but 5% would be typical. Also V_{CC} bypass capacitors are required for these two resistors. A value of .01 μF is suitable for each.

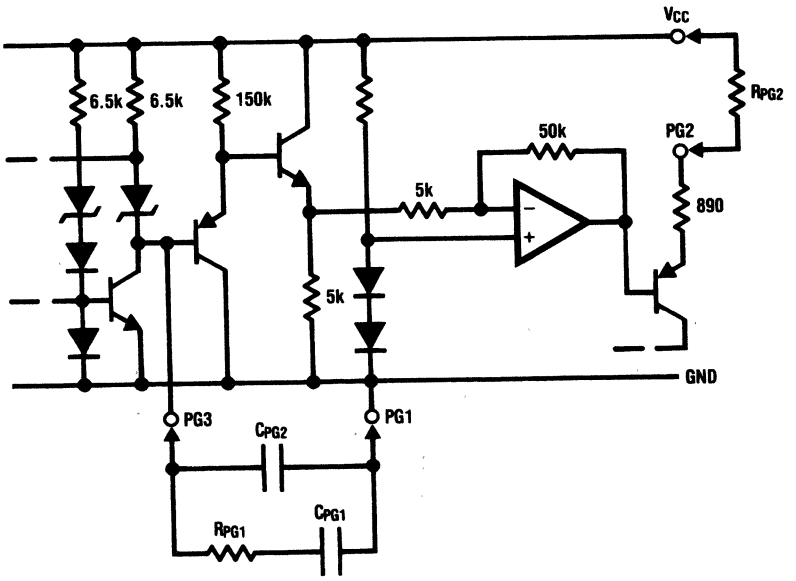

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FIGURE 6. Pulse Gate Controls

Circuit Operation (Continued)

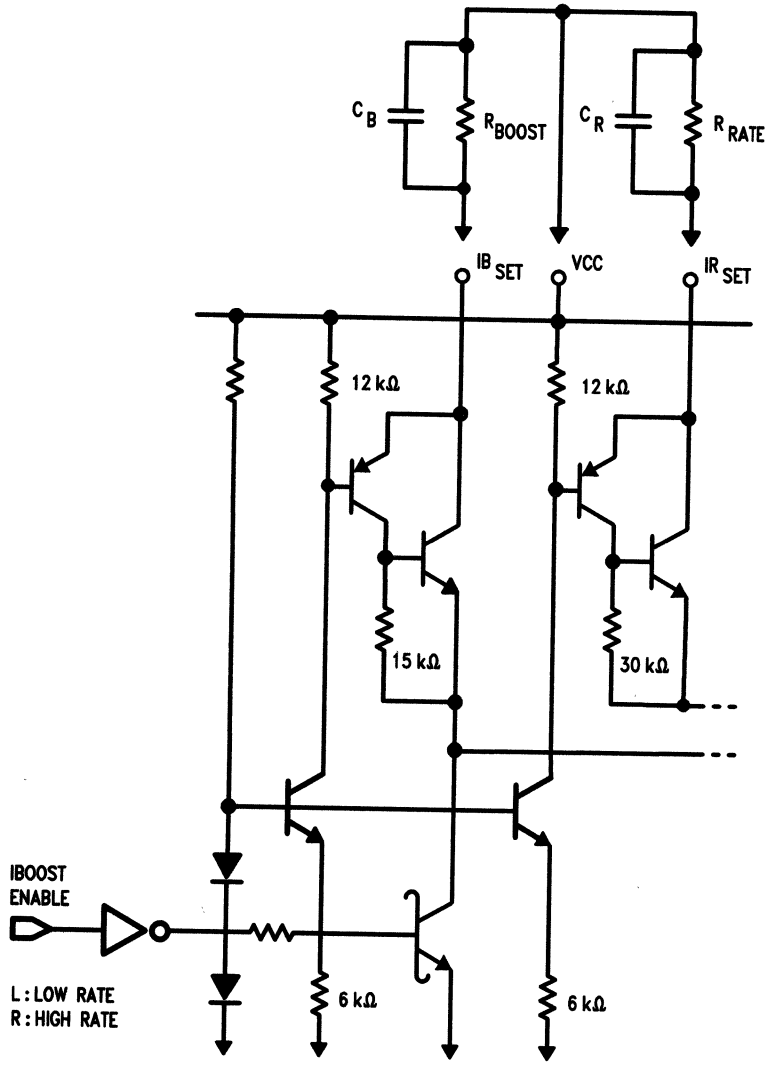

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FIGURE 7. I_{RATE} Set and I_{BOOST} Set

Circuit Operation (Continued)

VCO

The value of R_{VCO} is fixed at 1 kΩ ±1% in the External Component Limits table. *Figure 8* shows how R_{VCO} is connected to the internal components of the chip. This value was fixed at 1 kΩ to set the VCO operating current such that optimum performance of the VCO is obtained for production device spreads. This means fixed value components will be adequate to set the VCO center frequency for production runs. The value of C_{VCO} can therefore be determined from the VCO frequency f_{VCO}, using the equation: $C_{VCO} = [1/(R_{VCO})(f_{VCO})] - 5$ pF where f_{VCO} is twice the input data rate. As an example, for a 5 Mbit/sec data rate, $f_{VCO} = 10$ MHz, requiring that $C_{VCO} = 95$ pF. This does not take into account any inter-lead capacitance on the printed circuit board; the user **must** account for this. The amount of toler ance a particular design can afford on the center frequency will determine the capacitor tolerance. The capacitor is connected to internal circuitry of the chip as shown in *Figure 9*.

As the data rate increases and C_{VCO} gets smaller, the effects of unwanted internal parasitic capacitances influence the frequency. As a guide the graph of *Figure 10* shows approximately the value of C_{VCO} for a given data rate.

The VCO control input operational range (pin 4) lies at approximately 1.4 volts with a control swing of ±100 millivolts. The VCO itself is constrained to swing a maximum of approximately ±20% of its center frequency, and will remain clamped if the voltage at pin 4 exceeds its operational limit. The VCO center frequency may then be determined by: 1) holding pin 4 at ground potential and measuring the VCO frequency (−20% value); 2) holding pin 4 at approximately 3 volts and measuring the VCO frequency (+20% value); 3) averaging the two measured frequencies for the equivalent center frequency.

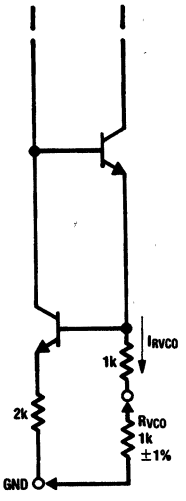

FIGURE 8. VCO Current Setting Resistor

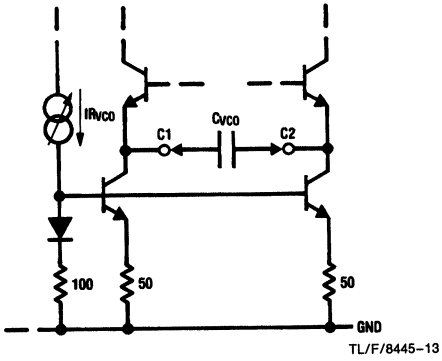

FIGURE 9. VCO Capacitor

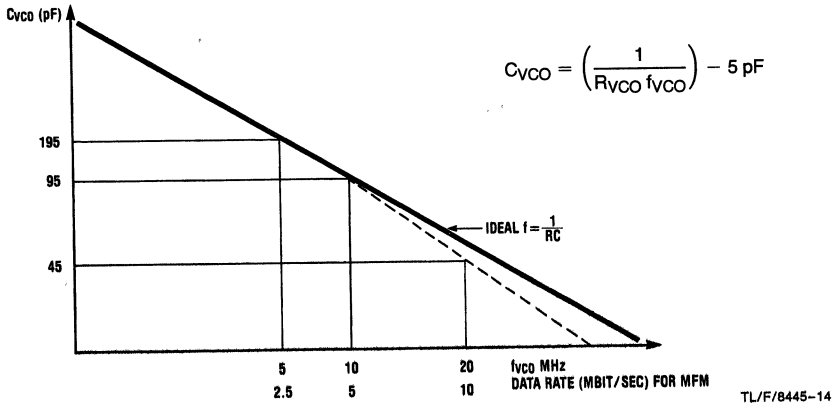

FIGURE 10. VCO Capacitor Value for Disk Data Rates

Circuit Operation (Continued)

Loop Filter

The input current into the Buffer Amplifier is offset by a matched current out of the Charge Pump, and even so is much less than the switching current in or out of the Charge Pump. It can therefore be assumed that all the Charge Pump switching current goes into the Loop Filter components R_1 and C_1 and C_2. The tolerance of these components should be the same as R_{RATE} and R_{BOOST}, and will determine the overall loop gain variation. The three components connected to the Charge Pump output are shown in *Figure 11*. Note the return current goes to analog GND, which should be electrically very close to the GND pin itself.

The value of capacitor C_1 determines loop bandwidth ... the larger the value the longer the loop takes to respond to an input change. If C_1 is too small, the loop will track any jitter on the ENCODED DATA input and the VCO output will follow this jitter, which is undesirable. The value of C_1 should therefore be large enough so that the PLL is fairly immune to phase jitter but not large enough that the loop won't respond to longer term data rate changes that occur on the disk drive.

The damping resistor R_1 is required to regulate the second-order behavior of the closed-loop system (overshoot). A value of R_1 that would give a phase margin of around 45 degrees would be a reasonable starting point.

The main function of the capacitor C_2 is to smooth the action of the charge pump at the VCO input. Typically its value will be less than one tenth of C_1. Further effects of C_2 will be discussed later.

Figure 12 shows the relevant phase-locked-loop blocks that determine system response, namely the Phase Detector, Filter/Buffer Amplifier, and VCO. The Phase Detector (Phase Comparator and Charge Pump) produces an aggregate output current i which is proportional to the phase difference between the input signal and the VCO signal. The constant (K_1) is

$$\frac{1.78\ V_{BE}}{N2\pi R} \text{ amps per radian, where } N = \frac{f_{VCO}}{f_{DATA}}.$$

R is either R_{RATE} or $R_{RATE} \parallel R_{BOOST}$. The amplified aggregate current feeds into or out of the filter impedance (Z), producing a voltage to the VCO that regulates the VCO frequency. The VCO gain constant is 0.4 ω_{VCO}/V_{BE} radians per second per volt. Under steady state conditions, i will be zero and there will be no phase difference between the input signal and the VCO. Any change of input signal will pro-

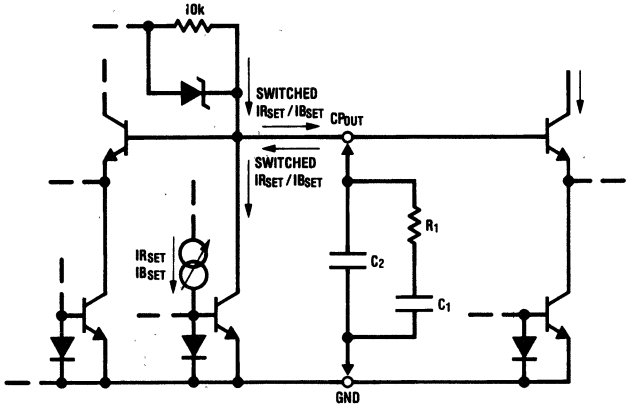

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FIGURE 11. Charge Pump Out

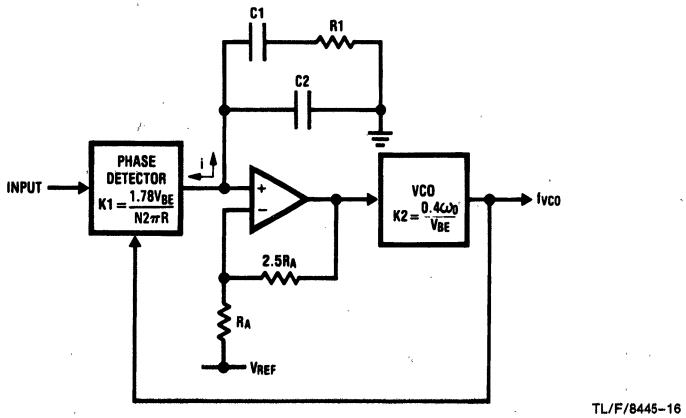

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FIGURE 12. Loop Response Components

Circuit Operation (Continued)

duce a change in VCO frequency that is determined by the loop gain equation. This equation is determined from the gain constants K_1, A and K_2 and the filter v/i response.

The impedance Z of the filter is:

$$\frac{1}{sC_2} \left\| \left(\frac{1}{sC_1} + R_1 \right) \right. = \frac{1 + sC_1R_1}{sC_1 \left(1 + \frac{C_2}{C_1} + sC_2R_1 \right)}$$

If $C_2 \ll C_1$ then the impedance Z approximates to:

$$\frac{1 + sC_1R_1}{sC_1 (1 + sC_2R_1)}$$

The overall loop gain is then

$$G(s) = \frac{K_1AK_2}{s} \times \frac{1 + sC_1R_1}{sC_1(1 + sC_2R_1)}$$

Let $G_{(K)} = K_1 A K_2$

$$F(s) = \frac{1 + SC_1R_1}{SC_1 (1 + SC_2R_1)}$$

The Overall Closed Loop Gain is:

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{G_{(K)} F(s)}{s + G_{(K)} F(s)}$$

Substituting, We Get

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{G_{(K)} (SC_1R_1 + 1)}{S^3 R_1 C_1 C_2 + S^2 C_1 + GK (SC_1R_1 + 1)}$$

$$= \frac{(G_{(K)}/C_1) (SR_1C_1 + 1)}{S^3R_1C_2 + S^2 + SG_{(K)}R_1 + G_{(K)}/C_1}$$

If $C_2 \ll C_1$, we can ignore the 3rd Order Component introduced by C_2 then:

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{(G_{(K)}/C_1) (SR_1C_1 + 1)}{S^2 + SG_{(K)}R_1 + G_{(K)}/C_1}$$

This is a second Order Loop and can be solved as follows:

$$S^2 + SG_{(K)}R_1 + G_{(K)}/C_1 = S^2 + 2\zeta \omega_n S + \omega_n^2$$

$$\therefore C_1 = \frac{G_{(K)}}{\omega_n^2}$$

$$R_1 = \frac{2\zeta\omega_n}{G_{(K)}}$$

$\zeta = 1.0$ For Critically Damped Response

From the above equations:

$$\omega = \sqrt{\frac{G_{(K)}}{C_1}}$$

$$G_{(K)} = K_1 A K_2 = \frac{0.89 \times V_{BE}}{2\pi R} \times \frac{0.4 \times \omega_{VCO}}{V_{BE}} \times 3.5$$

MFM encoded data has a two to one frequency range within the data field. The expression $K = (0.89 \times V_{BE} / 2\pi R)$ is valid when the MFM data pattern is at its maximum frequency. In order to make this equation more general, it may be written as follows: $K = (1.78 \times V_{BE} / 2\pi RN)$ where N is defined as the V_{CO} frequency divided by the encoded data frequency, or, N is equal to F_{VCO}/F_{DATA} (N = 2 for maximum data rate i.e., MFM = 101010 ... and N = 4 for minimum data rate) i.e., MFM = 100010001 .... Now $G_{(K)}$ can be written as follows:

$$G_{(K)} = \frac{1.78 \times V_{BE}}{2\pi RN} \times \frac{0.4 \times \omega_{VCO}}{V_{BE}} \times 3.5$$

$$= \frac{2.5 \times F_{VCO}}{RN}$$

$$\omega_n = \sqrt{\frac{2.5 \times F_{VCO}}{C_1RN}}$$

$R = R_{RATE}$ in the low track rate

$R = R_{RATE} // R_{BOOST}$ in the high track rate

From the above equations:

$$\omega_n = \frac{R_1 G_{(K)}}{2\zeta}$$

$$G_{(K)} = C_1 \omega_n^2$$

$$\zeta = \text{(damping factor)} = \frac{R_1 \omega_n C_1}{2}$$

The damping factor should approach, but not fall below, 0.5 when ω_n is minimum. Response to bit shift is minimized when the damping factor is small; however, if the damping factor drops much below 0.5, the system tends to be oscillatory (underdamped).

Additionally, loop performance is poor (excessive phase acquisition times) if the damping factor becomes significantly greater than 1.0. Any increase in loop bandwidth (due to R decreasing in the high track rate) produces a proportional increase in the damping factor, and this should be limited to the point where the maximum damping factor does not significantly exceed 1.0. With the damping factor range established, loop design can now proceed. The following design example is for a 5 Mbit/sec MFM system.

A 1550 Krads/sec bandwidth in the non read mode results in a wide capture range; a 4% frequency difference between the crystal and recorded data would not cause an acquisition problem. (This bandwidth may seem excessive to some and if the user does not think it is necessary, he may design his filter with a more desirable bandwidth. For an in-depth discussion of this point, it is suggested that the reader refer to the Disk Interface Design Guide and User's Manual, chapter 1, sections 1.3 through 1.7.

This design example assumes that the $\overline{\text{SET PLL LOCK}}$ pin is tied to the $\overline{\text{PLL LOCK DETECTED}}$ pin. This results in the track rate being switched from high to low after two bytes of preamble are detected. As an alternative, the $\overline{\text{SET PLL LOCK}}$ pin may be tied to an inverted READ GATE signal, resulting in the track rate switching immediately to low when READ GATE is asserted. This is discussed further in the above mentioned reference material.

TABLE II.

Data Rate (NRZ)	Non-Read		Read		Charge Pump		Loop Filter		
	$\omega_{n(MAX)}$ rads/sec	ζ	$\omega_{n(MIN)}$ Rads/sec	ζ	R_{RATE} Ω	R_{BOOST} Ω	R_1 Ω	C_1 μF	C_2 pF
5 Mbit/sec	1550K	1.12	797K	0.55	820	820	120	0.012	300
5 Mbit/sec	903K	0.99	435K	0.48	1500	1300	100	0.022	390
5 Mbit/sec	659K	1.55	248K	0.52	1500	590	69	0.068	1500

Circuit Operation (Continued)

In the non read mode or high track rate.

$$\omega_n = \sqrt{\frac{2.5 \times F_{VCO}}{C_1 RN}}$$

Choose $R = R_{RATE} // R_{BOOST} = 410$

In the non-read mode $N = 2$

$$1550 \text{ Krads/sec} = \sqrt{\frac{2.5 \times 10^7}{C_1 \times 410 \times 2}}$$

$C_1 = 0.012\ \mu F$

In the preamble, after two bytes are detected and $\overline{\text{PLL LOCK DETECT}}$ goes low

$$\omega_n = \sqrt{\frac{2.5 \times F_{VCO}}{C_1 RN}}$$

$R = R_{RATE} = 820$

$N = 2$

$\omega_n = 1127$ Krads/sec

Again, in the data field, the minimum data frequency is equal to one half the preamble frequency. This means that $N = 4$ in the bandwidth equation. This reduces the bandwidth to:

$$\omega_{n(min)} = \frac{1}{\sqrt{2}} \times 1107 \text{ Krads/sec} = 797 \text{ Krads/sec}$$

Before, we stated that the minimum value of ζ should be 0.5; knowing $\omega_{n(min)}$ we can now solve for R_1

$$\zeta = \frac{\omega_n R_1 C_1}{2}$$

Choose $\zeta_{(min)} = 0.55$

$$R_1 = \frac{2\zeta}{\omega_n C_1}$$

$R_1 = 115\Omega$ (choose 120Ω)

The maximum damping value occurs in the high track rate;

$\zeta_{(max)} = \omega_{n(max)} R_2 C_1/2$

$= 1550 \text{ Krads/sec} \times 120 \times 0.012\ \mu F/2$

$\zeta_{(max)} = 1.12$

The maximum damping value in the read mode is as follows:

$\zeta_{(max-read)} = 1127 \text{ Krads/sec} \times 120 \times 0.012\ \mu F/2$

$\zeta_{(max-read)} = 0.81$

The continuous behavior (non-quantized) approximation used to predict loop performance assumes that the phase detector output is constantly proportional to the input phase difference. In reality, the phase detector output is a pulse applied for a period of time equal to the phase difference. The function of C_2 is to smooth the phase detector output (VCO control voltage) over each cycle. C_2 also adds a second pole to the filter transfer function. This pole should be far enough outside the loop bandwidth (at least one order of magnitude) that its phase and amplitude contribution is negligible in the loop bandwidth. If:

$C_2 = C_1/50 = 240$ pF (choose 300 pF)

The final loop component is R_{BOOST}. Since R_{RATE} and the parallel combination of R_{RATE} and R_{BOOST} are known, we can calculate R_{BOOST}.

$R_{BOOST} = (R_P)(R_{RATE}) / (R_{RATE} - R_P) = 820\Omega$

The above filter values and those for other bandwidths are listed on preceding page.

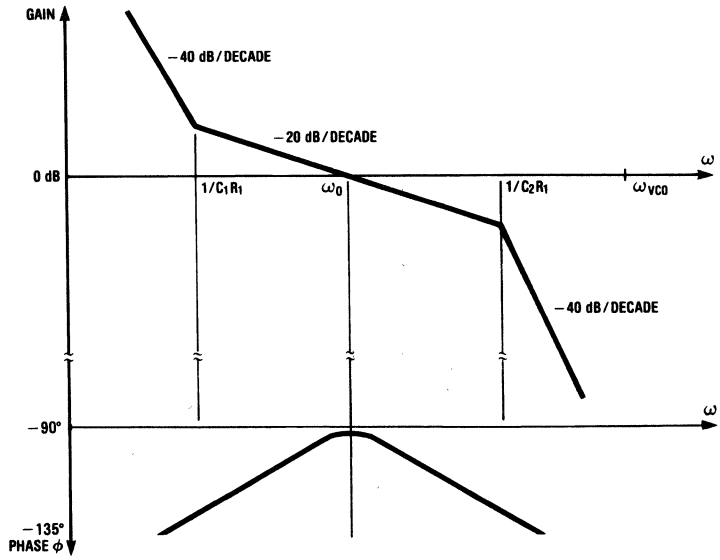

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FIGURE 13. Bode Plot of Loop Response

Circuit Operation (Continued)

The calculated values are only a guide, the user should then empirically test the loop and determine stability, lock-on time, jitter tolerance, etc.

The desired Bode plot of gain and phase is shown in *Figure 13*, with 20 dB/decade slope at ω_0 for stability at unity gain.

Capacitor C_2 governs the PLL's ability to reject instantaneous bit jitter. As C_2 increases in value, the effective jitter rejection will also increase. However, as the frequency of the pole R_1 and C_2 produce (while increasing C_2) decreases, loop stability will decrease, and the second-order approximation used to analyze the circuit becomes inaccurate. Thus, it is recommended that C_2 remain one tenth (or less) the value of C_1.

The value of resistor R_1 inversely effects the break frequencies on the Bode plot, and directly effects the loop's damping ratio (overshoot response). The capacitor C_1 governs the bandwith of the loop. Too high a value will slow down the response time, but make the PLL less prone to jitter or frequency shift whereas too low a value will improve response time while tending to increase the PLL's reaction to jitter.

Other filter combinations may be used, other than R_1 in series with C_1, all in parallel with C_2. For example the filter shown in *Figure 14* will also perform similarly, and in fact for some systems it will yield superior performance.

DIGITAL CONNECTIONS TO THE DP8461/65

Figure 17 shows a connection diagram for the DP8461/65 in a typical application. All logic inputs and outputs are TTL compatible as shown in *Figure 15* and *16*. The VCO CLOCK output is 74AS compatible. All other outputs are 74ALS compatible. All inputs are 74ALS compatible and therefore can be driven easily from any 74 series devices. The raw MFM from the pulse detector in the drive is connected to the ENCODED DATA input. The DELAY DISABLE input determines whether attempting lock-on will begin immediately after READ GATE is set or after 2 bytes. Typically in a hard-sectored drive, READ GATE is set active as the sector pulse appears, meaning a new sector is about to pass under the head. Normally the preamble pattern does not begin immediately, because gap bytes from the preceding sector usually extend just beyond the sector pulse. Allowing 2 bytes to pass after the sector pulse helps ensure that the PLL will begin locking on to preamble, and will not be chasing non-symmetrical gap bits. Thus DELAY DISABLE should be set low for this kind of disk drive.

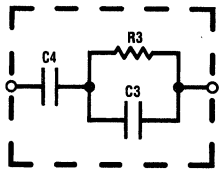

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FIGURE 14. Alternate Loop Filter Configuration

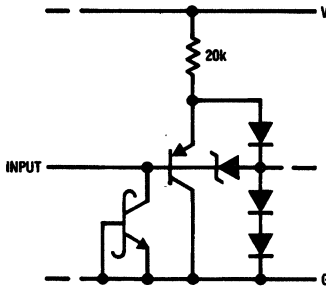

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FIGURE 15. Logic Inputs

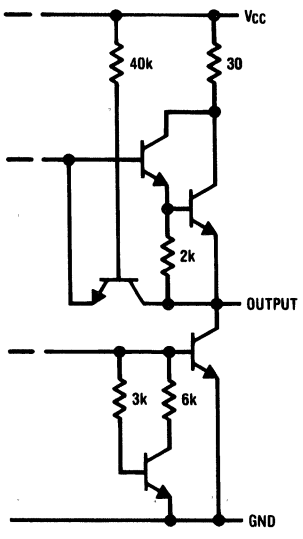

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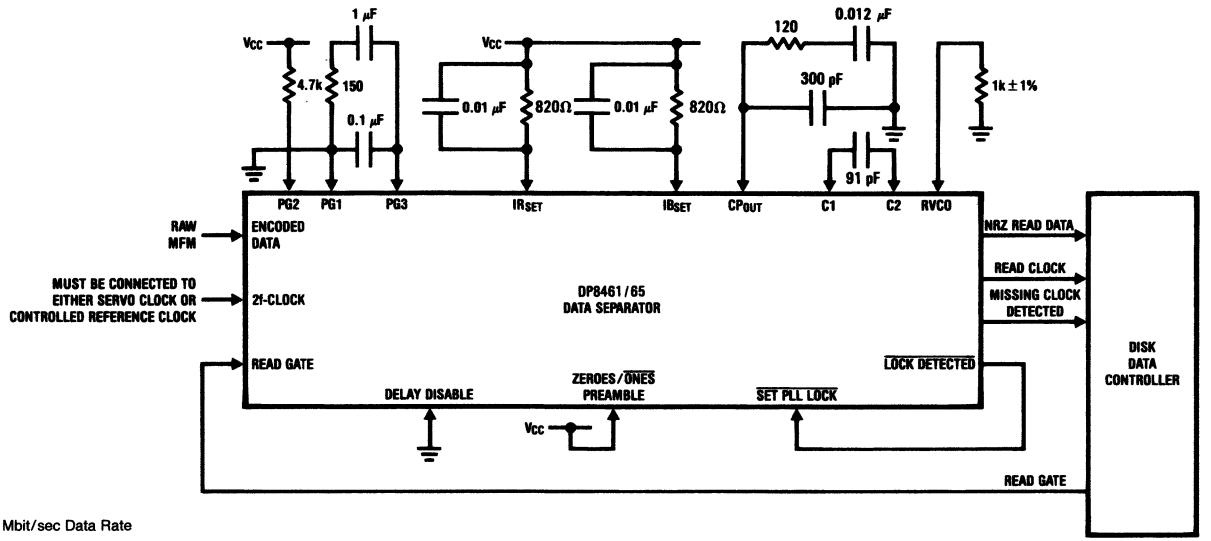
FIGURE 16. Logic Outputs



1) MFM Data Input, 5 Mbit/sec Data Rate
2) 32 Bit Delay to Enable
3) All Zeroes (NRZ) Preamble

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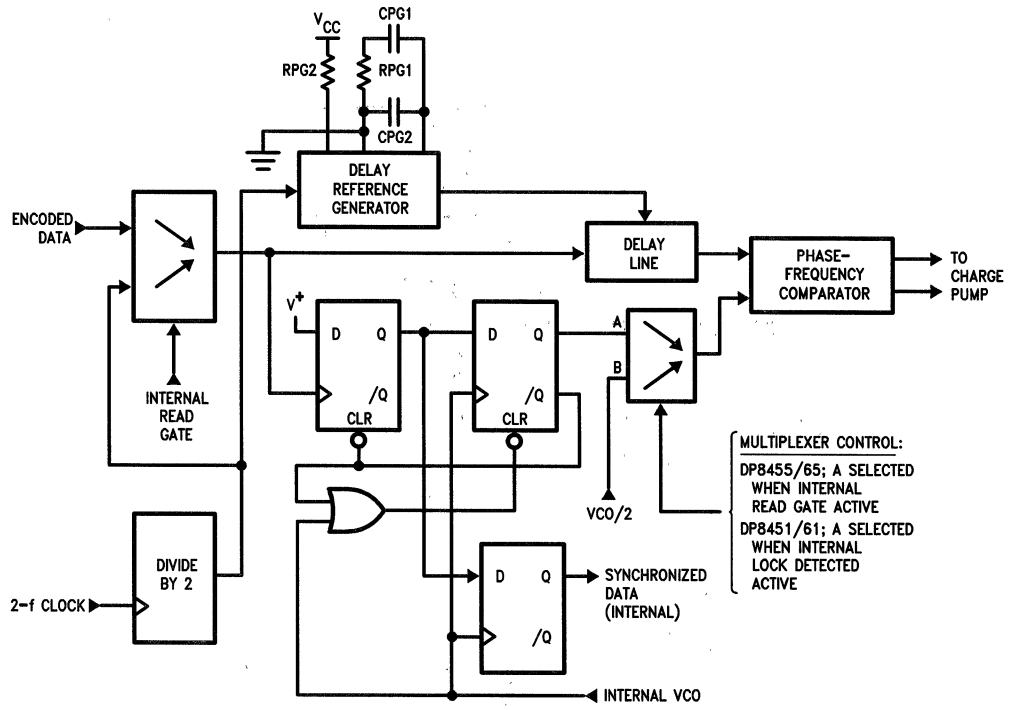
FIGURE 17. Typical Connection to DP8461/65

Block Diagram



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Circuit Operation (Continued)

For soft sectored drives, the controller normally will not wait for the index pulse before it attempts lock-on, so that READ GATE may go active at any time. Chances are the head will not be over a preamble field and therefore there is no need to wait 2 bytes before attempting lock-on. DELAY DISABLE can therefore be set high. If a non-preamble field is passing by as READ GATE goes active, the DP8461/65 will not indicate lock, and no data decoding will occur nor will MISSING CLOCK DETECTED go active. Normally, if lock-on has not been achieved after a certain time limit, the controller will de-activate READ GATE and then try again.

For MFM encoded disk drives, the $\overline{\text{LOCK DETECTED}}$ output will be connected back to the $\overline{\text{SET PLL LOCK}}$ input. As the PLL achieves lock-on, the DP8461/65 will automatically switch to the lower tracking rate and decoded data will appear at the NRZ READ DATA output. Also the READ CLOCK output will switch from half the 2F-CLOCK frequency to the disk data rate frequency. If a delay is required before the changeover occurs, a time delay may be inserted between the two pins.

Some drives have an all-ONES data preamble instead of all-ZEROES and the DP8461/65 must be set to the type being used before it can properly decode data. The ZEROES/$\overline{\text{ONES}}$ PREAMBLE input selects which preamble type the chip is to base its decoding phase on.

USE WITH RUN-LENGTH-LIMITED CODES (RLL)

If the drive uses a Run-Length-Limited Code (RLL) such as 1,7 or 1,8 instead of MFM, the user might choose to use the DP8451/55. These circuits contain the PLL portion of the DP8461/65 and thus perform the data synchronization function. RAW DATA is input to pin 16 and the 2F-CLOCK is applied to pin 17. Instead of supplying NRZ DATA, SYNCHRONIZED DATA OUTPUT is issued at pin 12. The VCO CLOCK, pin 8, is used to clock this data into external decoding circuitry. As long as the high frequency pattern of . . . 1010 . . . is used for the preamble, the user may choose the DP8451 if he desires to have the circuit perform phase and frequency comparisons until two bytes of preamble are detected by the on chip preamble pattern detector.

If a 2,7 code is being used the DP8465/55 may be used. Again, since the DP8465 MFM decoding function will not be used, the user may choose to use the DP8455. However, the National Semiconductor DP8462 is designed specifically for the 2,7 code. It is recommended that the user reviews the DP8462 specification for the added advantages the circuit offers with the 2,7 format.

Applications of the DP8461/65 Data Separator

The DP8461/65 are the first integrated circuits to place on one chip a PLL with features that offer the improved speed and reliability required by the disk industry. Not only does each chip simplify disk system design, but also provides fast lock-on to the incoming preamble. Once locked on, the loop is set into a more stable mode. This inherent loop stability allows for a sizeable amount of jitter on the data stream, such as is encountered in many disk systems. Once in the stable tracking rate, the SYNCHRONIZED DATA output represents the incoming ENCODED DATA and is synchronous with VCO CLOCK. If the disk is MFM encoded, then the chip can decode the synchronized data into NRZ READ DATA and READ CLOCK. These are available as outputs from the chip allowing the NRZ READ DATA to be deserialized using the READ CLOCK.

The DP8461/65 are capable of operating at up to 20 Mbits/sec data rates and so are compatible with a wide assortment of disk drives. The faster data rates of the 8-inch and 14-inch disk drives will mandate the selection of the DP8461/65–3 parts with their narrower window margins on the incoming data stream. This will also be the case when 5¼-inch drives achieve higher data rates. Some 8-inch and 14-inch disk drives incorporate the functions of the DP8461/65, but use many discrete ICs. In these cases, replacing these components with the DP8461/65 will offer reduced P.C. board area, lower cost, and improved performance while simplifying circuit testing.

Most 5¼-inch and many 8-inch and 14-inch disk drives manufactured at present do not incorporate any of the functions of the DP8461/65. This is so primarily because the PLL function is difficult to design and implement and requires circuitry which covers a large area of the printed circuit card. This is undesirable both from the drive size aspect and from the cost aspect (the cost includes soldering, testing, and adjusting the components). Consequently, most smaller disk drives output MFM encoded data so that the phase-locked-loop and data separation have to be performed by the controller. The DP8461/65 will therefore replace these functions in controller designs, as shown in *Figure 18*.

System design criteria has become more flexible because the DP8461/65 provide a one-chip solution, requiring only a few external passive components with fixed values. Each operates from a +5V supply, typically consumes about 0.3W, and is housed in a narrow 24-pin package. The circuitry has been designed so that the external resistors and capacitors need not be adjustable; the user chooses the values according to the disk drive requirements. Once selected, they will be fixed for that particular drive type. These features make it possible to transfer these functions to the disk drive, as shown in *Figure 19*. Apart from a slight increase in board area, the advantages outweigh the disadvantages. First, the components selected are fixed for each type of drive and this facilitates the problem of interchangeability of drives. At present, controllers are adjusted to function with each specific drive; with the DP8461/65 in the drive, component adjustment will no longer be required. Second there is often a problem of reliability of data transfer. The data returning from the disk drive is susceptible to noise, bit shift, etc. Soft errors will occur when the incoming disk data bit position is outside the Pulse Gate window as it is being synchronized to the VCO clock in the phase-locked-loop. Obviously, the nearer the PLL is to the data source, the less chance there is that extraneous noise or transmission line imbalances will cause errors to occur. Thus placing the DP8461/65 in the drive will increase the reliability of data transfer within the system.

A third advantage is data rate upgrading. Most 5¼-inch drives have 5 Mbit/sec data rate because the early drives were made with this data rate. This meant the controllers had to be designed with PLLs which operate at this data rate. It is therefore difficult for drive manufacturers to introduce new drives that are not compatible with existing controllers. Since no new standard data rate has emerged, they must continue to produce drives at this data rate to be compatible with the controllers on the market. With the DP8461/65 in the drive, and associated components set for the drive's data rate, it no longer becomes a problem to increase the data rate, assuming the controllers digital circuitry can accommodate the change. This will allow the manufactures to increase the bit density and therefore the capacity of their drives.

Applications of the DP8461/65 Data Separator (Continued)

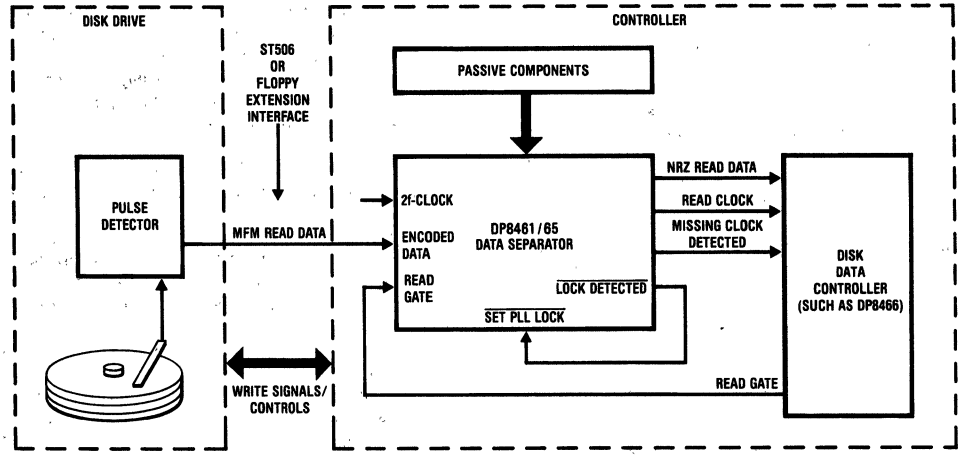

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FIGURE 18. DP8461/65 in the Controller

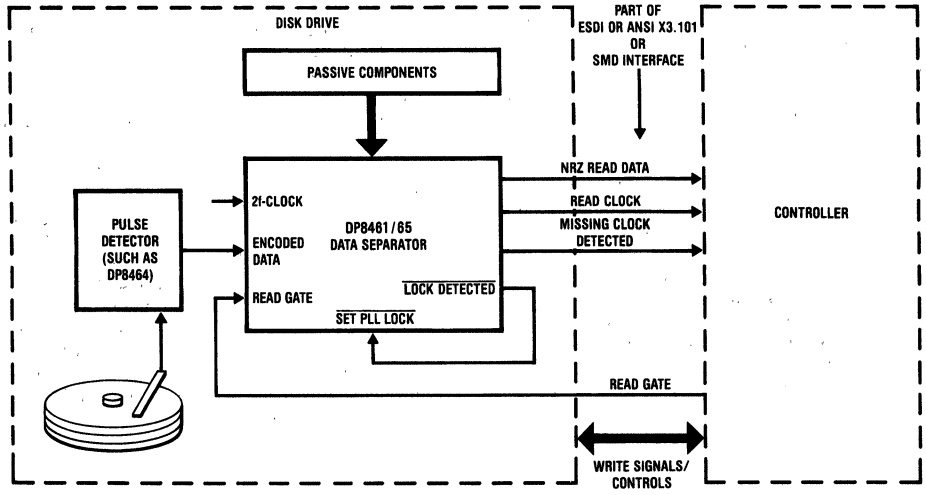

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FIGURE 19. DP8461/65 in the Disk Drive

PRECAUTIONS IN BREADBOARDING AND PCB LAYOUT

The DP8461/65 contains a high performance analog PLL and certain precautions must be taken when breadboarding or designing a PCB layout. The following guidelines should be adhered to when working with the DP8461/65:

1) Do not wire wrap.
2) Keep component lead lengths short, place components as close to pins as possible.This applies to R1, C1, R2, C_{VCO}, R_{RATE}, R_{BOOST}, C_{RATE}, C_{BOOST}, RPG1, RPG2, and CPG1.
3) Provide a good ground plane and use a liberal amount of supply bypassing. The quieter a PLL's environment, the happier it is.
4) Avoid routing any digital leads within the vicinity of the analog leads and components.
5) Keep inter-pin capacitance to a minimum; i.e., avoid running traces or planes between pins.
6) Minimize digital output pin capacitive loading to reduce current transients.

NSC has used a PC board approach to breadboarding the DP8461/65 that gives an excellent ground plane and keeps component lead lengths very short. With this setup very stable and reliable operation has been observed. Illustration of component layout is shown in *Figure 20*.

Applications of the DP8461/65 Data Separator (Continued)

ADDITIONAL NOTES

1. PG1 should be grounded to improve noise immunity.
2. 2F clock must be applied at all times; without the 2F clock, the pulse gate circuitry will not operate properly making it impossible to lock onto the incoming data stream.
3. The programming capacitor for the V_{CO} can be calculated as:

$$C_{VCO} = 1/(f_{VCO} \times R_{VCO}) - 5\ pF$$

The 5 pF value is due to parasitic and pin to pin capacitance. An additional accomodation must also be made for PC board capacitance.

4. Care must be taken in final PC board layout to minimize pin to pin capacitance, particularly in multi-layer printed circuit boards.
5. Please refer also to Precautions for Disk Data Separator Designs, NSC Application Note AN-414.

Connection Diagrams

DP8461/65

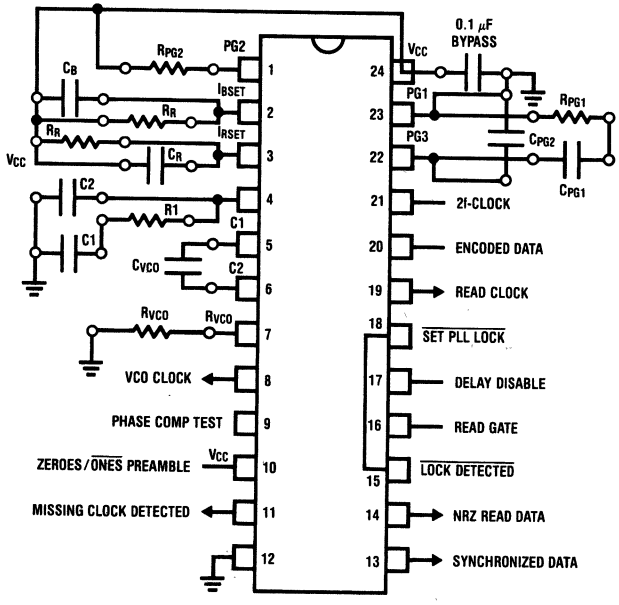

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FIGURE 20. Recommended Component Layout

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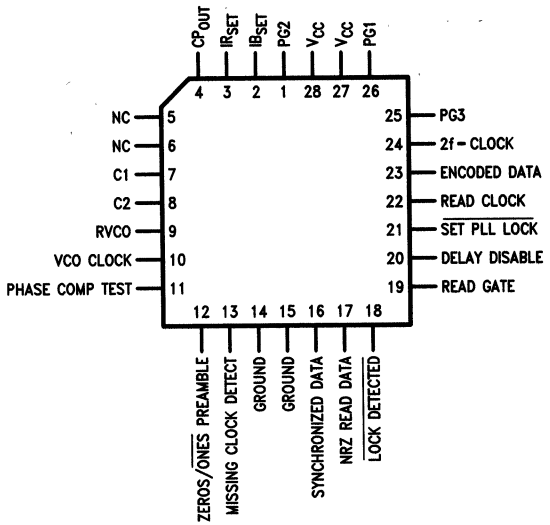
Connection Diagrams (Continued)

Plastic Chip Carrier



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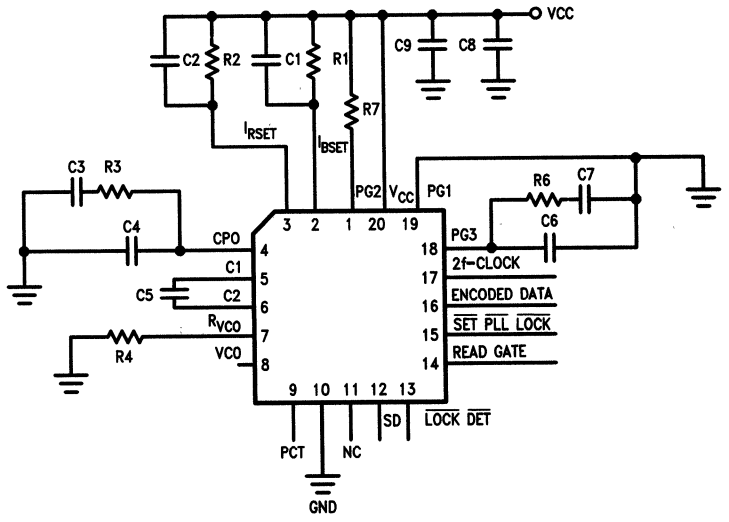
Order Number DP8461V or DP8465V
See NS Package Number V28A

DP8451/DP8455



TL/F/8445–27

National Semiconductor

DP8459 All-Code Data Synchronizer

General Description

The DP8459 Data Synchronizer is an integrated phase locked loop circuit which has been designed for application in magnetic hard disk, flexible (floppy) disk, optical disk, and tape drive memory systems for data re-synchronization and clock recovery with any standard recording code, operating to 25 Mb/s. The DP8459 is provided in a 28-pin PCC package. Zero phase start is employed during both data and reference clock lock sequences for rapid acquisition. An optional (Customer-controlled) synchronization field frequency-acquisition feature guarantees lock, accommodating the preamble types used with GCR (Group Code Recording), MFM (Modified Frequency Modulation), the [1,N] run length limited (RLL) codes, and either of the standard 2,7 RLL codes. Precise synchronization window generation is achieved via an internal, self-aligning delay line which remains accurate independent of temperature, power supply, external component and IC process variations. The DP8459 also incorporates a digitally controlled (MICROWIRE™ bus compatible) strobe function with 5-bit resolution which allows for margin testing, error recovery routines, and precise window calibration. The PLL filter resides external to the chip, with two ports provided to allow significant design flexibility. Synchronization pattern detection circuitry issues a PREAMBLE DETECTED signal when a pre-determined length of the user-selected pattern is encountered. All digital input and output signals are TTL compatible and a single, +5V power supply is required. The DP8459V is offered as a DP8459V-10 (250 Kbit/sec thru 10 Mbits/sec) or DP8459V-25 (250 Kbits/sec thru 25 Mbit/sec), see AC Electrical Characteristics.

Features

- Fully integrated dual-gain PLL
- Zero phase start lock sequence
- 250 Kbit/sec–25 Mbit/sec data rate range
- Frequency lock capability (optional) for all standard recording codes
- Digital window strobe control, 5-bit resolution
- Two-port PLL filter network
- PLL free-run (Coast) control for optical disk defects
- Synchronization pattern (preamble lock) detection
- Non-glitching multiplexed read/write clock output
- +5V supply
- DP8459 supplied in 28-pin plastic chip carrier (PCC) and 40-pin TapePak packages

Connection Diagrams

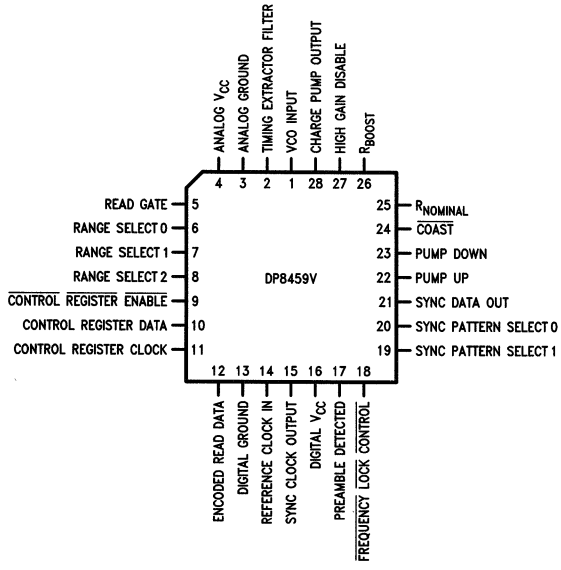


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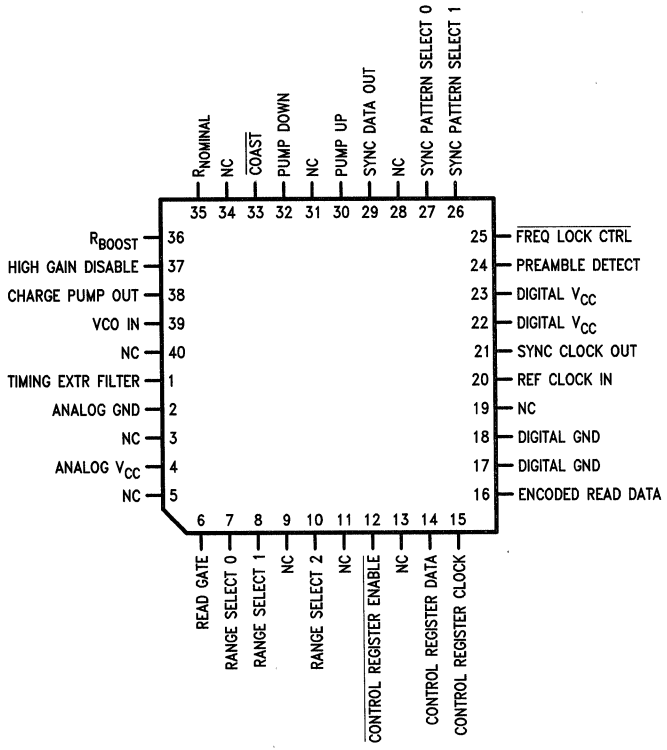
FIGURE 1. DP8459 in 28-Pin Plastic Chip Carrier (PCC) V-Type Package Order Number DP8459V-10 or DP8459V-25

Contents

Connection Diagrams (Continued)

TapePak®



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Top View

Order Number DP8459TP-10 or DP8459TP-25
See NS Package TP40A

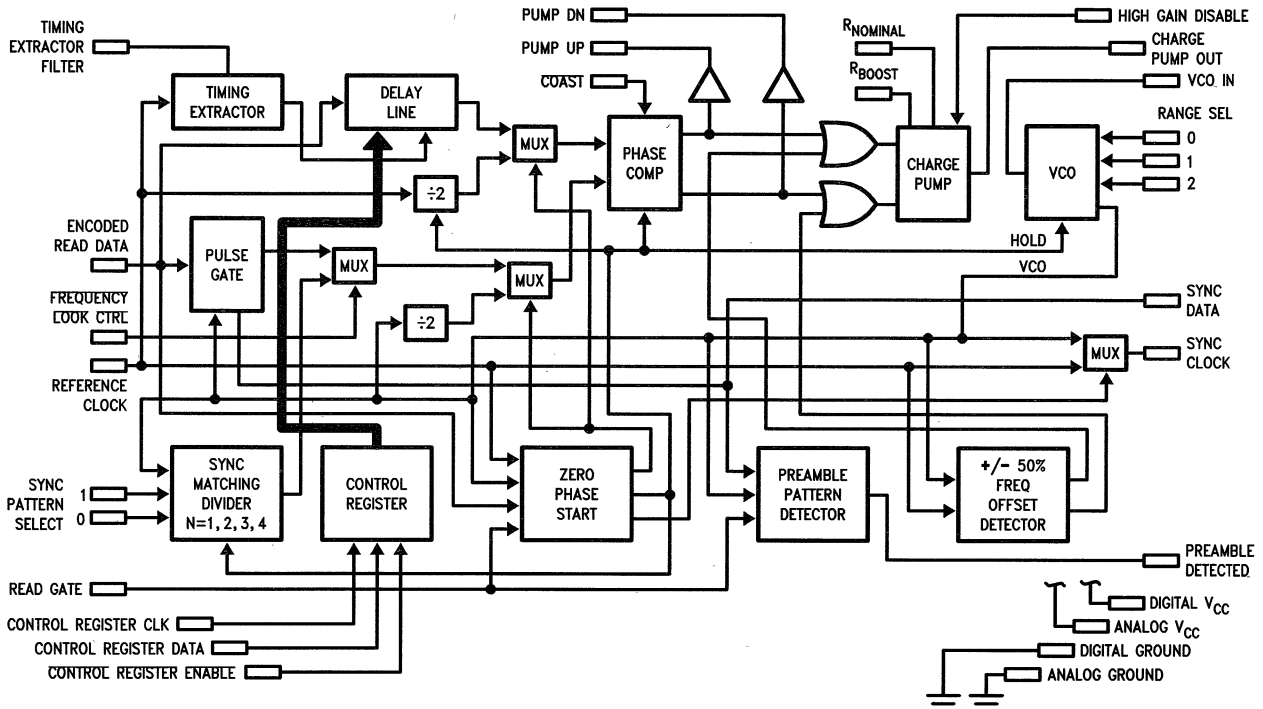

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FIGURE 2. DP8459 System Block Diagram

1.0 Pin Descriptions

DP8459 28-pin PCC package

Pin #	
POWER SUPPLY	
16	**DIGITAL V_{CC}:** 5.0V ±5%. (Note 1)
4	**ANALOG V_{CC}:** 5.0V ±5%. (Note 1)
13	**DIGITAL GROUND.**
3	**ANALOG GROUND.**
TTL LEVEL LOGIC INPUTS	
5	**READ GATE (RG):** Read mode control input, active high (logical-one). Assertion causes the PLL to lock to the ENCODED READ DATA, employing a zero phase start routine. Deassertion causes the PLL to lock the REFERENCE CLOCK input, also employing a zero phase start routine. READ GATE timing is allowed to be fully asynchronous.
6, 7, 8	**RANGE SELECT 0, 1, 2 (RS0, RS1, RS2):** Control the operating frequency range of the VCO. A 2:1 continuously variable sub-range is available within each of 6 allowed selections, enabling the VCO to operate at any frequency within a 96:1 range from 500 kHz to 50 MHz.
9	**$\overline{\text{CONTROL REGISTER ENABLE}}$ ($\overline{\text{CRE}}$):** A logical Low level allows the CONTROL REGISTER CLOCK to clock data into the Control Register via the CONTROL REGISTER DATA input; a logical HIGH level latches the register data and issues the information to the appropriate circuitry.
10	**CONTROL REGISTER DATA (CRD):** Control Register data input.
11	**CONTROL REGISTER CLOCK (CRC):** Negative edge triggered Control Register clock input.
12	**ENCODED READ DATA (ERD):** Incoming TTL-level data derived from the storage media; issued from a pulse detector circuit. Each positive edge represents a single recorded code bit.
14	**REFERENCE CLOCK (RFC):** A reference frequency input **required** for DP8459 operation. The RFC frequency must be accurate and highly stable (crystal or servo derived) and equivalent to the 2F frequency for the MFM or [2,7] codes (i.e., equal to, but not derived from the VCO frequency).
18	**$\overline{\text{FREQUENCY LOCK CONTROL}}$ ($\overline{\text{FLC}}$):** Selects or de-selects the frequency lock function during a READ operation. Has no effect with READ GATE deasserted; frequency lock is automatically employed for the full duration of time READ GATE is deasserted regardless of the level of the $\overline{\text{FLC}}$ input. With READ GATE high and $\overline{\text{FLC}}$ low (logical-zero) the PLL is forced to lock to the pattern frequency selected via the SYNC PATTERN SELECT inputs. When high (logical-one) frequency lock action is terminated and the PLL employs a pulse gate to accommodate random disk data patterns. $\overline{\text{FLC}}$ may be tied to PREAMBLE DETECTED output pin for self-regulated frequency lock control. $\overline{\text{FLC}}$ timing is allowed to be fully asynchronous.
20 19	**SYNC PATTERN SELECT 0, 1 (SP0, SP1):** Control inputs for selection of the preamble type being employed. These inputs determine the pattern to which the PLL will frequency-lock during preamble acquisition (if frequency lock is employed) and for which the PREAMBLE DETECTED circuitry searches.
24	**$\overline{\text{COAST}}$ ($\overline{\text{CST}}$):** Control for Coast function. The Coast function may be activated when READ GATE is either high or low. When the $\overline{\text{COAST}}$ input is low (logical-zero), the phase comparator is disabled and held in a cleared state, allowing the VCO to coast regardless of ENCODED READ DATA input activity (READ GATE high) or REFERENCE CLOCK input activity (READ GATE low). No other circuit functions are disturbed. When high (logical-one), the phase comparator operates normally.
27	**HIGH-GAIN DISABLE (HGD):** Charge Pump gain switch control. When low (logical-zero), the charge pump input current is the combined value of the currents at both R_{BOOST} and $R_{NOMINAL}$ pins. When high (logical-one), charge pump input current is taken from the $R_{NOMINAL}$ pin only. HGD may be tied either to READ GATE or PREAMBLE DETECTED for self-regulated gain control.

Note 1: These pins should *always* be tied together; they are not intended to be used with separate power supplies.

1.0 Pin Descriptions (Continued)

DP8459 28-pin PCC package

Pin #	
TTL LEVEL LOGIC OUTPUTS	
15	**SYNCHRONIZED CLOCK (SCK):** Issues the VCO signal following READ GATE assertion and completion of zero phase start sequence; issues REFERENCE CLOCK input signal when READ GATE is deasserted. Multiplexer switching is achieved without glitches.
17	**PREAMBLE DETECTED (PDT):** Issues a high level (logical-one) following assertion of READ GATE, completion of the zero phase start sequence, and the detection of approximately 32 sequential pulses of 1T, 2T or 3T period preamble, or 16 sequential pulses of 4T period preamble, depending on state of SYNC PATTERN SELECT inputs (T = VCO period). Following preamble detection, the output remains latched high until de-assertion of READ GATE. The PDT output will be at a logical zero state whenever READ GATE is inactive.
21	**SYNCHRONIZED DATA (SD):** A reconstructed replica of the ENCODED READ DATA signal, time-stabilized and synchronized to the SYNCHRONIZED CLOCK output.
22	**PUMP UP (PU):** Active HIGH whenever the phase comparator issues a pump-up signal to the charge pump. The PU pin is an open-emitter output requiring an external passive pull down resistor whenever in active use. The output should be allowed to float when not needed.
23	**PUMP DOWN (PD):** Active HIGH whenever the phase comparator issues a pump-down signal to the charge pump. The PD pin is an open-emitter output requiring an external passive pull down resistor whenever in active use. The output should be allowed to float when not needed.
ANALOG SIGNAL PINS	
28	**CHARGE PUMP OUTPUT:** The output of the high-speed, switching bi-directional current source circuitry of the charge pump. The external, passive PLL filter network is established between this pin, the VCO INPUT pin, and ground.
1	**VCO INPUT:** The high-impedance control voltage input to the voltage controlled oscillator (VCO). The external, passive PLL filter network is established between this pin, the CHARGE PUMP OUTPUT pin, and ground.
2	**TIMING EXTRACTOR FILTER:** A pin for the connection of external, passive components employed to stabilize the delay line timing extraction circuitry. Delay accuracy is not a function of external component values or tolerances.
25	**$R_{NOMINAL}$:** A resistor is tied between this pin and V_{CC} to set the charge pump *nominal* operating current. The current is internally multiplied by 2 for charge pump use.
26	**R_{BOOST}:** A resistor is tied between this pin and V_{CC} to set the charge pump *boost* (or adder) current. The R_{BOOST} resistor is effectively paralleled with the $R_{NOMINAL}$ resistor when the HIGH GAIN DISABLE input is inactive (logical-zero); thus the sum of the resistor currents sets the total input current. The input current is multiplied by 2 within the charge pump circuitry.

2.0 Circuit Operation

In the non-Read mode, the DP8459 PLL is locked to the REFERENCE CLOCK signal. This permits the VCO to remain at a frequency very close to the encoded data clock rate while the PLL is "idling" and thus will minimize the frequency step and associated lock time encountered at the initiation of lock to ENCODED READ DATA. Frequency acquisition is employed in the non-Read mode to ensure lock.

Note: The REFERENCE CLOCK signal is employed by circuitry which sets the time delay of the internal delay line. This requires the REFERENCE CLOCK signal to be present *at all times* at a stable and accurate frequency for proper DP8459 operation.

At the assertion of READ GATE, which is allowed to be done asynchronously (no timing requirements), and following the completion of two subsequent VCO cycles, the DP8459 VCO is stopped momentarily and restarted in accurate phase alignment with the second data bit which arrives following the VCO pause. This minimization of phase misalignment between the ENCODED READ DATA and the VCO (referred to as zero phase start, or ZPS) significantly reduces data lock acquisition time.

The DP8459 incorporates a preamble-specific frequency acquisition feature which may be employed at the user's option. The frequency acquisition feature is intended specifically for use within hard or pseudo-hard sectored systems where READ GATE is asserted only within a preamble. With the READ GATE active (logical-one) and the $\overline{\text{FREQUENCY LOCK CONTROL}}$ ($\overline{\text{FLC}}$) input active (logical-zero), the DP8459 will be forced to lock to the exact preamble frequency selected at the SYNC PATTERN SELECT inputs. The frequency discriminating action of the PLL provided in this mode produces a lock-in range equivalent to the available VCO operating range and thus eliminates the possibility of fractional-harmonic lock. Windowing (pulse gate action; see Pulse Gate, Section 2.1) is not employed in the frequency acquisition mode and thus quadrature lock is prevented (see National Semiconductor Application Note AN-414, APPS Mass Storage Handbook #1, 1986, for an explanation of typical false lock modes). The DP8459 will remain in the frequency acquisition mode until the $\overline{\text{FLC}}$ input is deactivated (logical-one). In ordinary hard sectored or pseudo-hard sectored operation, the PREAMBLE DETECTED (PDT) output is tied to the $\overline{\text{FLC}}$ input for automatic switching from frequency acquisition to phase lock following internal detection of the selected preamble by the DP8459. The Customer may choose to intervene in this path and extend the frequency lock period. However, the DP8459 *must* be placed in the phase lock mode ($\overline{\text{FLC}}$ deactivated—logical-one) prior to encountering the end of the preamble, or loss of lock will result. Switching of the $\overline{\text{FLC}}$ input may be done asynchronously (no set-up or hold timing requirements).

The PREAMBLE DETECTED (PDT) output will become active (logical-one) following READ GATE assertion, completion of the ZPS sequence and the subsequent detection of approximately 32 ENCODED READ DATA (ERD) pulses of the 1T, 2T or 3T preamble types, or 16 ENCODED READ DATA (ERD) pulses of the 4T preamble type (see specification tables), and will remain active (logical-one) until deassertion of READ GATE.

The Customer has the option of employing an elevated PLL bandwidth during preamble acquisition (or at any other time) for an extended capture range. An R_{BOOST} pin is provided to allow for an increase in charge pump gain above the level set by the $R_{NOMINAL}$ pin. When the HIGH GAIN DISABLE pin (HGD) is inactive (logical-zero), the R_{BOOST} resistor is electrically paralleled with the $R_{NOMINAL}$ for an elevated charge pump gain. When HIGH GAIN DISABLE is active (logical-one), only the $R_{NOMINAL}$ resistor is employed to set the pump current. The Charge Pump throughput gain is $I_{CPO} = 2 \times I_{Rp}$ where $I_{Rp} = 0.25V_{CC}/R_p$, $R_p = R_{NOM}$ with HGD high, and $R_p = R_{NOM} || R_{BOOST}$ with HGD low. The Customer may choose to configure the system for high gain prior to DP8459 preamble detection by tying the HGD pin to the PDT output pin, or for high gain only during REFERENCE CLOCK lock by tying the HGD pin to the READ GATE pin. Other configurations may be employed, if desired.

The DP8459 issues a clock waveform from the SYNCHRONIZED CLOCK output which is derived from the REFERENCE CLOCK input when the READ GATE is inactive (logical-zero), and from the VCO signal following READ GATE assertion (logical-one) and completion of the zero phase start sequence. The REFERENCE CLOCK signal is issued from the SYNCHRONIZED CLOCK output during non-Read activity and may be used as a write clock, if desired. Once data lock is achieved and the SYNCHRONIZED CLOCK output is issuing VCO, the SYNCHRONIZED DATA output and the SYNCHRONIZED CLOCK output are held in a fixed, specified timing relationship for use by decoding/deserializing circuitry. The SYNCHRONIZED CLOCK output multiplexer switching is achieved without glitches, i.e., no pulse is narrower than 50% of the VCO or REFERENCE CLOCK period.

The DP8459 provides a $\overline{\text{COAST}}$ control input which serves to clear the phase comparator and disable charge pump action whenever taken to an active, logical-zero level. This function is made available to allow the PLL to be set to free-run, undisturbed, while a detectable defect is being read from the media in a region where re-initiation of the lock procedure is impractical (e.g., data field). External data controller circuitry is responsible for the detection of the defect and issuance of the $\overline{\text{COAST}}$ command. The primary application of this feature is expected to be optical disk bright-spot avoidance, though it will lend itself to other applications as well.

As in the previous family of National Semiconductor data separators/synchronizers, the DP8459 provides phase comparator activity information to the Customer. The phase comparator's pump-up and pump-down outputs are brought out to separate pins, PUMP UP (PU) and PUMP DOWN (PD). The outputs are of the open-emitter type, requiring an external "pull-down" resistor when in active use. These outputs serve to indicate the relative displacement of the current data bit with respect to the internal VCO phase (window center). When in completely stabilized lock with no bit displacement, the output(s) will issue a pulse of a finite, minimum-valued width for each arriving data pulse. If any data pulse is displaced with respect to the VCO phase, the corresponding output pulse will widen by an amount equivalent to the bit displacement. These output signals may be integrat-

2.0 Circuit Operation (Continued)

ed over time and employed to determine the average magnitude of media bit shift. Additionally, the pulse widening/narrowing effect bit displacement has on the PU/PD outputs produces an amplitude modulation of the output's waveform. The waveform envelope, when observed with a relatively slow oscilloscope time base, can be employed for observation of PLL dynamics. This is particularly useful if intrusive probing of the PLL filter nodes is not desirable.

It is strongly recommended that the PU/PD outputs be left "floating" (unconnected to any net or circuit element, including the output pull-down resistor) in any application where they are not specifically needed. This will serve to minimize unnecessary, spurious digital switching transients in the vicinity of the DP8459, and thus improve noise performance.

The DP8459 provides a wide operating data rate range to facilitate use within a broad base of applications, including multiple data rate systems or constant density recording (CDR). In order to achieve the specified 250 kbit /sec to 25 Mbit/sec span, the operation of the VCO has been divided into 6 contiguous frequency sub-ranges, with approximately a 2:1 ratio between adjacent range selections. Three inputs are provided for selecting of the sub-ranges, RANGE SELECT 0, 1 and 2. Some code type restrictions have been placed on the higher ranges of operating VCO frequency. See *Figure 3* for the operating data rate truth table and allowed code type versus VCO range selection.

The DP8459 allows for flexible synchronization window strobe control. The inputs CONTROL REGISTER DATA (CRD), CONTROL REGISTER CLOCK (CRC), and CONTROL REGISTER ENABLE ($\overline{CRE}$) are configured to permit interfacing of the DP8459 to the MICROWIRE™ (or equivalent) bus for entry of strobe information. Information is serially shifted into the CONTROL REGISTER via the CRD and CRC pins whenever the $\overline{CRE}$ pin is active (logical-zero). When the $\overline{CRE}$ pin is inactive (logical-one), CRD and CRC are ignored. The strobe function allows the Customer to shift the synchronization window in 31 equal steps of magnitude $t_S = M \times [1.8\% \times \tau_{VCO}]$ from approximately 27% early to 27% late with respect to nominal window position. This function may be employed for margin testing (eg., approximately ±12%) or error recovery read re-try operations (eg., approximately ±2% to ±3%). Additionally, this feature allows the Customer to align the center of the synchronization window to within one half strobe step of ideal, regardless of the initial performance or specification of the DP8459. This window centering function may be performed completely within the drive system itself (auto-alignment) given the employment of an intelligent window alignment routine. Such a routine would be configured to determine the maximum error free early and late window positions via the strobe function, and then would fix the DP8459 window in the arithmetic mean position (Section 4.3.3). See *Figure 4* for a window strobe truth table.

Note: In all DP8459 applications, provision must be made to load the appropriate information into the Control Register.

RANGE SELECT Input (Note 1)			VCO Range MHz	Equivalent NRZ Data Rate	Minimum N (Allowed Code Type)			
2	1	0		MFM or 2,7 (Mbit/sec)	1 (GCR)	2 (MFM; 1, N)	3 (2,7)	4 (2,7)
1	1	X	0.50 ≤ Fvco ≤ 1.25	0.250≤ Fnrz ≤ 0.625	√	√	√	√
1	0	1	1.25 < Fvco ≤ 2.5	0.625< Fnrz ≤ 1.25	√	√	√	√
1	0	0	2.5 < Fvco ≤ 5	1.25< Fnrz ≤ 2.5	√	√	√	√
0	1	1	5 < Fvco ≤ 10	2.5< Fnrz ≤ 5	√	√	√	√
0	1	0	10 < Fvco ≤ 20	5< Fnrz ≤ 10	N/A	√	√	√
0	0	X	20 < Fvco ≤ 50 (Note 3)	10< Fnrz ≤ 25	N/A	√	√	√

Note 1: N/A—Not Allowed.

Note 2: Operation slightly beyond listed range boundaries may be acceptable in some applications. At or near range boundaries, range selection should be made to place the operating frequency near the UPPER boundary; e.g., use RS2 = 0, RS1 = 1, and RS0 = 0 for 10 Mb/s.

Note 3: 20 MHz < Fvco ≤ 38 MHz for 1, N codes.

FIGURE 3. Code Type Allowance Versus VCO Frequency Range

2.0 Circuit Operation (Continued)

Strobe Bit					Strobe	Window Strobe
4	3	2	1	0	Word M	T_S (Typical)
0	1	1	1	1	−15	$-0.270 \times \tau_{VCO}$
0	1	1	1	0	−14	$-0.252 \times \tau_{VCO}$
0	1	1	0	1	−13	$-0.234 \times \tau_{VCO}$
0	1	1	0	0	−12	$-0.216 \times \tau_{VCO}$
0	1	0	1	1	−11	$-0.198 \times \tau_{VCO}$
0	1	0	1	0	−10	$-0.180 \times \tau_{VCO}$
0	1	0	0	1	−9	$-0.162 \times \tau_{VCO}$
0	1	0	0	0	−8	$-0.144 \times \tau_{VCO}$
0	0	1	1	1	−7	$-0.126 \times \tau_{VCO}$
0	0	1	1	0	−6	$-0.108 \times \tau_{VCO}$
0	0	1	0	1	−5	$-0.090 \times \tau_{VCO}$
0	0	1	0	0	−4	$-0.072 \times \tau_{VCO}$
0	0	0	1	1	−3	$-0.054 \times \tau_{VCO}$
0	0	0	1	0	−2	$-0.036 \times \tau_{VCO}$
0	0	0	0	1	−1	$-0.018 \times \tau_{VCO}$
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	1	1	$0.018 \times \tau_{VCO}$
1	0	0	1	0	2	$0.036 \times \tau_{VCO}$
1	0	0	1	1	3	$0.054 \times \tau_{VCO}$
1	0	1	0	0	4	$0.072 \times \tau_{VCO}$
1	0	1	0	1	5	$0.090 \times \tau_{VCO}$
1	0	1	1	0	6	$0.108 \times \tau_{VCO}$
1	0	1	1	1	7	$0.126 \times \tau_{VCO}$
1	1	0	0	0	8	$0.144 \times \tau_{VCO}$
1	1	0	0	1	9	$0.162 \times \tau_{VCO}$
1	1	0	1	0	10	$0.180 \times \tau_{VCO}$
1	1	0	1	1	11	$0.198 \times \tau_{VCO}$
1	1	1	0	0	12	$0.216 \times \tau_{VCO}$
1	1	1	0	1	13	$0.234 \times \tau_{VCO}$
1	1	1	1	0	14	$0.252 \times \tau_{VCO}$
1	1	1	1	1	15	$0.270 \times \tau_{VCO}$

FIGURE 4. Window Strobe Truth Table

Customers who employ the DP8459 in a system without a MICROWIRE™ (or functionally equivalent) bus configuration and who wish to fix the synchronization window in the nominal position while deselecting the test mode need only load all-zero's into the Control Register following power-up; this may be easily achieved in some system configurations (requiring no additional hardware) by tying $\overline{CRE}$ to RG, tying CRC to ERD and tying CRD to ground, providing the necessary waveforms are present for register loading prior to the first read operation.

The DP8459 provides two pins for PLL filtering purposes, CHARGE PUMP OUTPUT (CPO) and VCO INPUT (VCOI). These provide the Customer with great flexibility in fliter design, permitting high-order filter functions for optimization of PLL lock characteristics and bit jitter rejection. For basic 3rd order applications, CPO and VCOI may be tied together (single-node) with a simple lead-lag, $C||(R+C)$ filter tied between these pins and ground. More esoteric filter designs may be implemented if the pins are electrically separated and a two-port filter network is established between CPO, VCOI, and ground. National Semiconductor supplies initial PLL filter recommendations for the single-node configuration within this data sheet with the qualifying statement that they are very general in nature, intended primarily for production testing of static window margin, and are NOT optimized for any particular disk system. For optimum performance, the Customer should pursue a filter design which is individualized and tailored to the requirements of the specific system involved. This is particularly true for the two-port filtering technique. See *Figure 5* for initial single-node filter design recommendations.

2.0 Circuit Operation (Continued)

Code	MFM	MFM	MFM	2,7	2,7	Units
Rate	0.500	2	5	10	20	Mbit/sec
VCO freq.	1	4	10	20	40	MHz
Sync bytes	12	12	12	12	12	bytes
pulses/byte	8	8	8	4	4	flux tran's
sync length	192	48	19.2	9.6	4.8	μs
sync freq	0.500	2	5	5	10	MHz
N_{sync}	2	2	2	4	4	none
N_{max}/N_{min}	4/2	4/2	4/2	8/3	8/3	none
ζ_{min}	0.5	0.5	0.5	0.5	0.5	none
ζ_{max}	0.7	0.7	0.7	0.8	0.8	none
ζ_{sync}	0.7	0.7	0.7	0.7	0.7	none
ω_{sync}	35	144	353	606	1230	Krad/sec
C1	0.5	0.12	0.05	0.018	8200 pF	μF*
R1	82	82	82	150	150	Ω
C2	0.01 μF	2700	1000	510	200	pF

Note 1: Preamble (sync) natural frequency chosen yields phase error ≤ 0.01 radians at sync field end, given a 1% frequency step at READ GATE assertion. Rnom = Rboost = 2.4k for all above loop filter selections. HGD is tied to RG, $\overline{FLC}$ is tied to PD and CPO is tied to VCOI as well as to the loop filter components.

Note 2: Component values are listed for purposes of window specification testing and correlation. These values do not necessarily yield optimum performance in actual system applications. PLL dynamics and code characteristics are presented for Customer information and convenience only. See Section 3.1.

*Unless otherwise noted.

FIGURE 5. Test Conditions and Component Values for Static Window Truncation Testing

The DP8459 VCO is constrained at all times to operate within a frequency swing of approximately ±50% of the frequency present at the REFERENCE CLOCK input. Internal frequency detector/comparator circuitry senses when the VCO overruns the 50% boundary and forces the charge pump to move the VCO back toward the REFERENCE CLOCK frequency until the 50% constraint is again satisfied—thus preventing VCO runaway in the event of loss of lock or during extended periods where ENCODED READ DATA is not present. Additionally, this technique causes the filter node voltage to behave as if a voltage clamp were present at the Charge Pump Output, preventing the control voltage, in the event of loss of lock, from drifting outside of its operating range and inadvertently extending lock recovery time.

A special test mode feature has been incorporated into the DP8459 which allows a specific input pin to change function and act as an excitation source (substitute VCO) for clocking internal logic circuitry. When the last bit in the CONTROL REGISTER is taken to a logical ONE, the VCO is stopped, and the HGD input is redirected to act as a clock source for the VCO divider circuitry. Additionally, the Delay Line and Timing Extractor blocks are disabled when the Test Mode is entered, and thus the device will not function normally and should not be operated in this mode for purposes other than internal gate exercising. Further information regarding application of the Test Mode will be furnished at the Customer's request: contact National Semiconductor Logic Marketing Group or Logic Applications Group.

2.1 Functional Block Description

PULSE GATE

The function of the Pulse Gate within the DP8459 is twofold. First, the block contains the ECL flip-flop which captures each arriving ENCODED READ DATA bit and transmits the bit to the SYNCHRONIZED DATA output. The very high switching speed of the bit-capture ECL flip-flop minimizes the portion of window margin loss caused by flip-flop metastability at window boundaries. Second, the Pulse Gate regulates the transmission of the VCO waveform into the Phase Comparator, allowing only one VCO pulse to pass with each arriving ENCODED READ DATA pulse. See *Figure 6* for a simplified logical representation of the Pulse Gate block. The one-to-one data/VCO pulse ratio produced by the Pulse Gate permits the multiple-harmonic nature of encoded data to be accommodated by the phase/frequency comparator. During the non-Read mode or during the portion of the Read mode within which the Customer has set the $\overline{FREQUENCY\ LOCK\ CONTROL}$ pin to a logical-zero (low), the Pulse Gate is inactive (bypassed) and the VCO frequency is divided as appropriate to match the incoming frequency source (ENCODED READ DATA or the REFERENCE CLOCK input).

2.1 Functional Block Description (Continued)

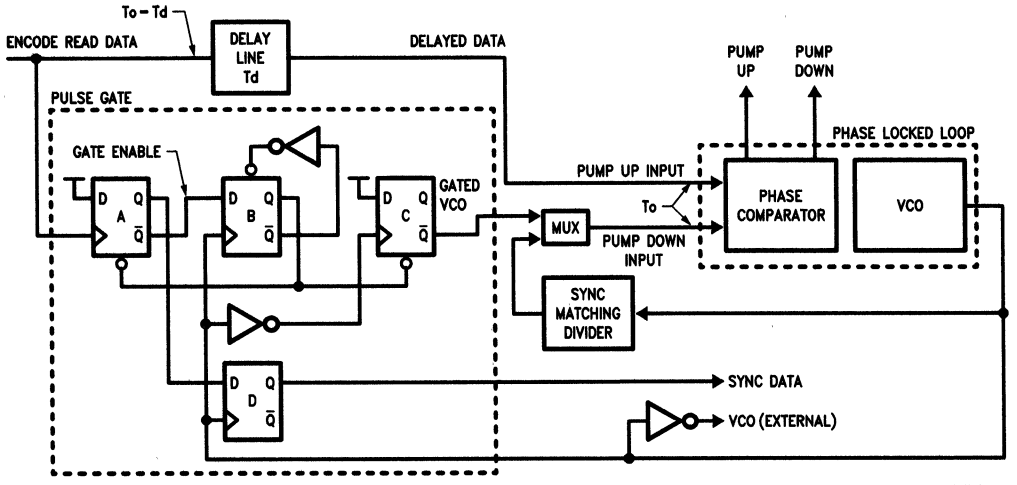

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FIGURE 6. Simplified Diagram of Window Generation Circuitry

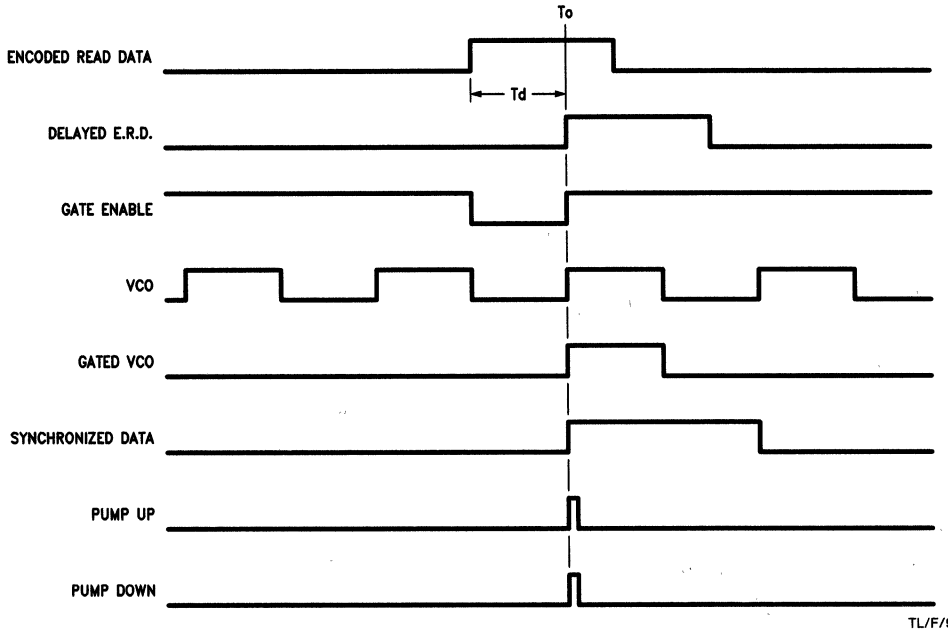

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FIGURE 7. Capture of Nominally Positioned ENCODED READ DATA Pulse

2.1 Functional Block Description (Continued)

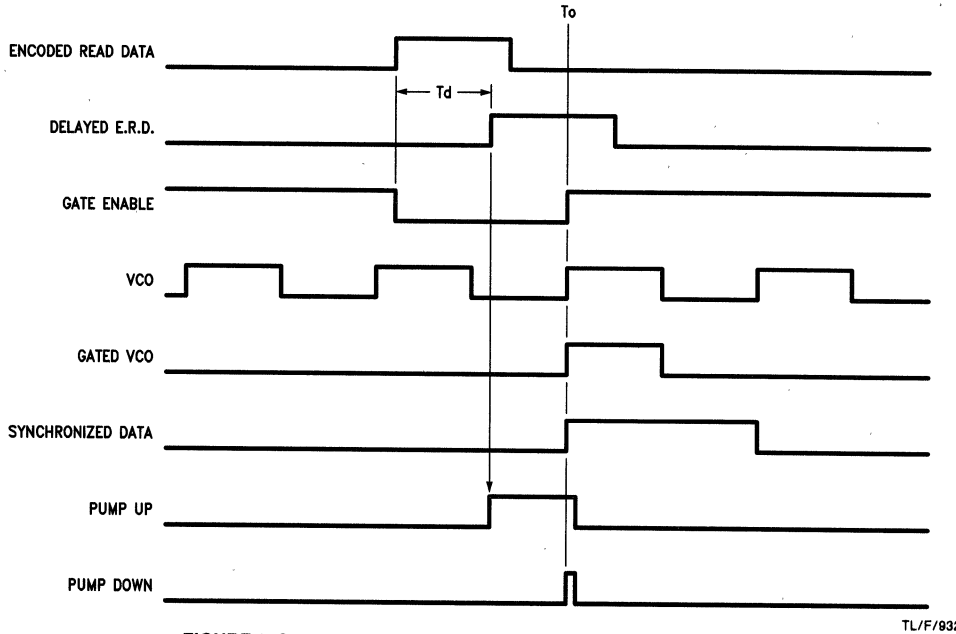

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FIGURE 8. Capture of Early-Shifted ENCODED READ DATA Pulse

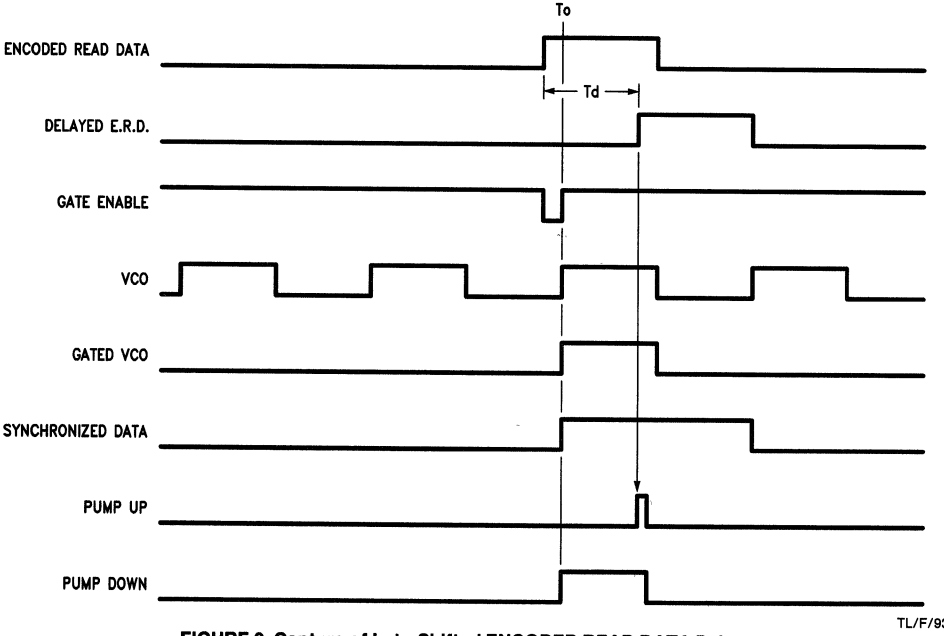

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FIGURE 9. Capture of Late-Shifted ENCODED READ DATA Pulse

2.1 Functional Block Description (Continued)

DELAY LINE

The DP8459 employs an internal silicon delay line to establish synchronization window alignment. The delay is nominally equivalent to one half of the period of the REFERENCE CLOCK waveform, and is variable in fine increments via the Control Register in order to achieve the window strobe function. The Timing Extractor circuitry derives realtive timing information soley from the REFERENCE CLOCK signal and regulates the magnitude of the delay within the Delay Line. The Delay Line thus remains insensitive to the external components associated with the extractor as well as to supply voltage, temperature, and IC process variations.

TIMING EXTRACTOR

This block extracts timing information from the REFERENCE CLOCK input for use by the variable silicon delay line. External passive components (tied to the Timing Extractor Filter pin) are associated with this block, although the accuracy of the circuit's function remains independent of the general value and tolerance of the components. The resistor-capacitor net is employed by the Timing Extractor for stabilization purposes—no monostable multivibrator (one-shot) circuitry is employed by the DP8459. Note that the performance of the delay line is directly dependent upon the accuracy of the REFERENCE CLOCK input waveform. Either a crystal reference generator or a stable servo clock source must be applied to this input. Multiplexing of the REFERENCE CLOCK waveform between read operations (within multiple data rate systems) is acceptable, although sufficient Timing Extractor stabilization time must be allowed following any perturbation at this pin before a read operation may be performed (see *Figure 10* for timing table).

PHASE COMPARATOR

The DP8459 employs a digital Phase Comparator (non-harmonic discriminator circuit) which has the capability of forcing the frequency of the PLL VCO toward the frequency of the reference input regardless of the magnitude of the frequency difference. The function of the Phase Comparator circuit can be represented in a diagrammatically simplified form as in *Figure 11*.

The Phase Comparator's action can be disabled at any time (cleared) via the $\overline{\text{COAST}}$ input pin, allowing the VCO to free-run.

CHARGE PUMP

The Charge pump is a high speed, switching, dual-gain, bi-directional current source whose current flow is controlled by the digital Phase Comparator circuit. The current pulses at the CHARGE PUMP OUTPUT (CPO) pin thus reflect the magnitude and sign of the phase error seen at the input of the Phase Comparator. The CPO pin is connected externally to a passive component network whose impedance translates the aggregate current into a voltage for the VCO INPUT while providing a low-pass filter function for the PLL. The matched source and sink current generators' operating currents are set via the $R_{NOMINAL}$ and R_{BOOST} pins, which are supplied current from V_{CC} through external resistors. The bias voltages at the $R_{NOMINAL}$ and R_{BOOST} pins are set to $0.75 \times V_{CC}$; the current into each of these pins is internally multiplied by 2 for Charge Pump use. The CPO current is defined as follows:

$$I_{CPO} = (V_{CC}/2)/R_{NOM}$$

HIGH GAIN DISABLE high (logical-one)

$$I_{CPO} = (V_{CC}/2)/(R_{NOM} \| R_{BOOST})$$

HIGH GAIN DISABLE low (logical-zero)

RFC Frequency	1	4	10	20	40	MHz
CT1	0.82	0.2	0.082	0.056	0.027	μF
RT1	68	68	68	68	68	Ω
Settling Time	192	96	19.2	9.6	4.6	μs

Values may be interpolated for intermediate data rates. Timing Extractor settling times are given which indicate time required for the DP8459 to accommodate a change of Strobe setting from nominal selection to either extreme (early/late), or vice versa, to within approximately 1% of final value.

FIGURE 10. TIMING EXTRACTOR FILTER Component Values for Various Data Rates

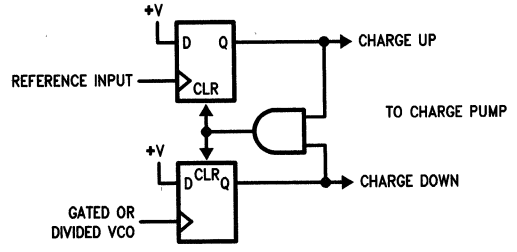

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FIGURE 11. Simplified Digital Phase-Frequency Comparator

2.1 Functional Block Description (Continued)

VOLTAGE CONTROL OSCILLATOR (VCO)

The DP8459 VCO is comprised of two portions—a self contained, high frequency oscillator (no external components) whose frequency is regulated by the voltage at the VCO INPUT pin, and a programmable modulus digital divider. The oscillator is only required to operate over approximately a 2:1 frequency range; the divider modulus is programmable in factors of 2. The two blocks work in conjunction to achieve a continuous range of equivalent VCO operating frequencies from 500 kHz to 50 MHz. (See *Figure 12.*)

CONTROL REGISTER

Within the DP8459, the Control Register is a MICROWIRE compatible, 6-bit shift register block with bits 0 through 4 employed to control the window strobe function and bit 5 employed to regulate the device test mode (see *Figures 13* and *14*). Information is serially shifted into the Control Register via the CRD and CRC (negative edge clock) pins whenever the $\overline{CRE}$ pin is active (logical-zero). When the $\overline{CRE}$ pin is inactive (logical-one), CRD and CRC are ignored. *Figure 3* shows the truth table for the VCO range select function; *Figure 4* shows the truth table for the window strobe function.

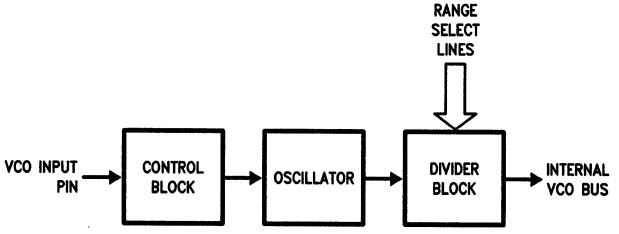

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FIGURE 12

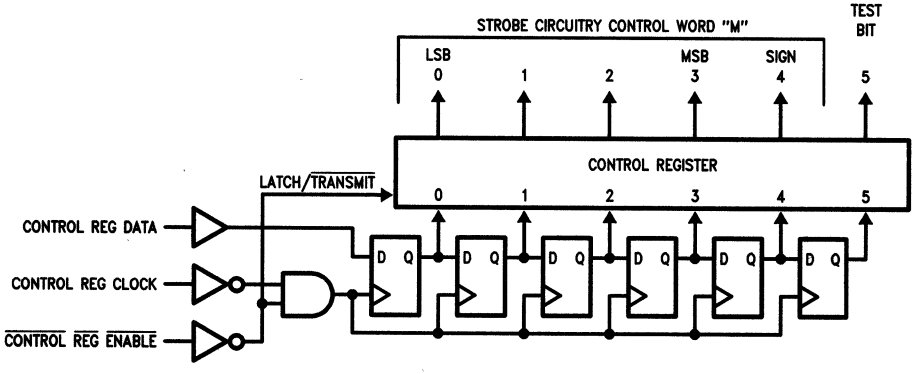

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FIGURE 13. Control Register

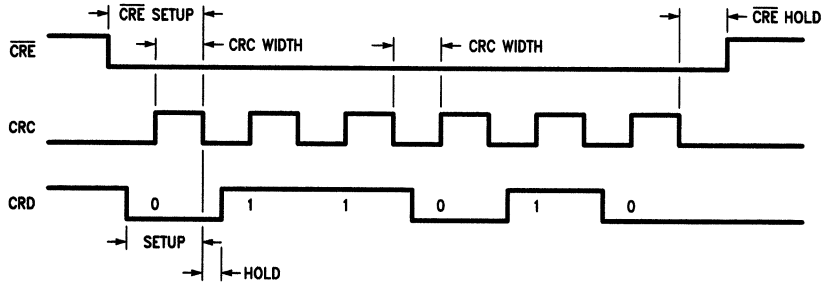

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FIGURE 14. Microwire Compatible Control Register Serial Load Timing Diagram

2.1 Functional Block Description (Continued)

SYNCHRONIZATION FIELD MATCHING DIVIDER

The Synchronization field Matching Divider is a programmable modulus counter employed for implementation of the preamble frequency lock function. It is placed in the VCO feedback path to match the relative frequency of the VCO seen at the Phase Comparator to the frequency of the ENCODED READ DATA (preamble) during the read operation whenever the FREQUENCY LOCK CONTROL input is active (logic-zero). The modulus of the divider, M, is determined by the states of the SYNC PATTERN SELECT 0 and 1 inputs, as defined by the table in *Figure 15*.

Sync Pattern Select		Sync Matching Divider Modulus M	Expected Code Preamble
1	0		
0	0	1	GCR
0	1	2	MFM; 1,N
1	0	3	2,7
1	1	4	2,7

FIGURE 15. SYNC PATTERN SELECT Input Truth Table

Prior to the assertion of READ GATE, the divider is held in a known count state and is enabled at the end of the zero phase start sequence in correct phase relationship with the ENCODED READ DATA. Re-assertion (logical zero) of the FREQUENCY LOCK CONTROL pin within a read operation (following the normal FLC deassertion after lock is achieved) is permissible; however, it should be noted that the initial phase error of the Synchronization Field Matching Divider with respect to the ENCODED READ DATA at FREQUENCY LOCK CONTROL re-assertion may be as large as $M \times \tau_{VCO}$ in magnitude, possibly resulting in an extended PLL settling time.

ZERO PHASE START

The function of the zero phase start (ZPS) block is to clear the Phase Comparator and freeze the VCO in a known phase when a transition occurs at the READ GATE input (either high or low), and restart the VCO in a precise, controlled phase with respect to the newly selected input (ENCODED READ DATA or REFERENCE CLOCK ÷ 2, respectively). The ZPS circuit also resets the count state of the Synchronization field Matching Divider in anticipation of locking to specific preamble information (when frequency lock is being employed), and controls the operation of the REFERENCE CLOCK multiplexer. ZPS operation at READ GATE assertion is aimed at optimizing initial window alignment and thus minimizing initial phase step and the resulting phase lock acquisition time. ZPS is also employed at deassertion of READ GATE; however, the ZPS phase alignment for the REFERENCE CLOCK signal at READ GATE deassertion has been made less stringent than for ENCODED READ DATA at READ GATE assertion.

PREAMBLE PATTERN DETECTOR

The Preamble Pattern Detector block has a pattern-specific recognition circuit keyed to search the ENCODED READ DATA for the pattern selected at the SYNC PATTERN SELECT inputs. The pattern search begins following the assertion of READ GATE and the completion of the zero phase start sequence, and continues until approximately 32 uninterrupted ENCODED READ DATA pulses of the 1T, 2T or 3T pattern have been detected, or until 16 uninterrupted ENCODED READ DATA pulses of the 4T pattern have been detected (see specification tables). When this event occurs, the PREAMBLE DETECTED output becomes active high (logical-one). The output will then remain latched in the high state until READ GATE is deasserted. The PREAMBLE DETECTED output may be tied to the HIGH GAIN DISABLE input to regulate the gain of the PLL during the preamble lock sequence, and/or tied to the FREQUENCY LOCK CONTROL input for self-regulation of frequency acquisition in hard or pseudo-hard sectored systems.

±50% VCO FREQUENCY OFFSET DETECTOR

The Frequency Offset Detector is employed to constrain the VCO frequency swing, preventing VCO runaway associated with standard, wide-range voltage controlled oscillators. The circuitry will sense the relative difference between the REFERENCE CLOCK frequency and the VCO frequency, sending a "charge-up" signal to the Charge Pump to correct the VCO should a limit of approximately −50% in frequency differential (VCO w.r.t. REF CLOCK) be exceeded, and sending a "charge-down" signal to the Charge Pump to correct the VCO should a limit of approximately +50% in frequency differential be exceeded. The resulting voltage-clamping action at the filter node(s) also prevents out-of-range control voltage straying and thus speeds lock recovery.

SYNCHRONIZATION CLOCK OUTPUT MULTIPLEXER

This block issues the VCO signal following READ GATE assertion and completion of the zero phase start sequence, and issues the REFERENCE CLOCK input signal when the READ GATE is deasserted. Multiplexer switching is achieved without glitches. The output is intended to be used both for read and write clock purposes. (Please note output loading recommendations for this pin in Section 6.)

2.2 SPECIFICATION TABLES

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
TTL Inputs	7V
Output Voltages	7V
Input Current (R_{NOM}, R_{BOOST}, CPO, VCOI, TEF)	2 mA
Storage Temperature	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
ESD Susceptibility (Note 3)	1500V

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
T_A	Ambient Temperature		0	25	70	°C
I_{OH}	High Logic Level Output Current	SYNC CLOCK Others			−2000 −400	μA
I_{OL}	Low Logic Level Output Current (Note 1)	SYNC CLOCK Others			20 8	mA
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level Input Voltage				0.8	V
f_{NRZ}	Operating Data Rate Range		0.25		25	Mb/s
$t_{PW\text{-}RFC}$	Width of REFERENCE CLOCK, High or Low		8			ns
$t_{PW\text{-}ERD}$	Width of ENCODED READ DATA		12 High 18 Low			ns
$t_{PW\text{-}CRE}$	Width of CONTROL REGISTER ENABLE, High or Low (Note 2)		40			ns
$t_{SU\text{-}CRD}$	CONTROL REGISTER DATA Set-Up Time with Respect to CRC (Note 2)		20			ns
$t_{H\text{-}CRD}$	CONTROL REGISTER DATA Hold Time with Respect to CRC (Note 2)		10			ns
$t_{SU\text{-}\overline{CRE}}$	CONTROL REGISTER ENABLE Set-Up Time with Respect to CRC (Note 2)		20			ns
$t_{H\text{-}\overline{CRE}}$	CONTROL REGISTER ENABLE Hold Time with Respect to CRC (Note 2)		20			ns
$t_{PW\text{-}CRC}$	CONTROL REGISTER CLOCK Pulse Width Positive or Negative (Note 2)		40			ns
I_{CPIN}	Combined R_{NOM} & R_{BOOST} Input Current				1000	μA

Note 1: PUMP UP and PUMP DOWN outputs have no current sinking capability and thus are excluded from this specification.

Note 2: Parameter guaranteed by correlation to characterization data. No outgoing test performed.

Note 3: Human body model; 120 picofarads through 1.5 kΩ.

AC Electrical Characteristics Over recommended V_{CC} and operating temperature range.

Symbol	Parameter	Min	Typ	Max	Units
t_{STOP}	SYNC CLOCK Negative Transitions following READ GATE until Data Lock ZPS Sequence Begins (VCO Freezes)		2	3	—
$t_{RESTART}$	Positive ENCODED READ DATA Transitions following VCO Freeze until VCO Restarts		2		—
$t_{READ\ ABORT}$	Number of REF CLOCK Cycles following READ GATE Deactivation until REF CLOCK Lock ZPS Sequence Begins			4	—
t_T	Window Truncation (Half Window Loss); **DP8459V-10** 10 Mbit/sec (Note 1) **DP8459V-25** 20 Mbit/sec (Note 2)		 3% × τ_{VCO} 4% × τ_{VCO}	 3.0 2.5	 ns ns
ϕ Linearity	Phase Range for Charge Pump Linearity (wrt VCO)		$\pm\pi$		Radians
K_{VCO}	VCO Gain Constant	1.0 ω_O	1.2 ω_O	1.6 ω_O	Rad/Sec V
$f_{MAX\ VCO}$	VCO Maximum Frequency; RS0 = RS1 = RS2 = Logical ZERO	70			MHz
t_{SD0}	Time Skew between SYNC CLOCK Negative Edge and SYNC DATA Negative Edge	0		10	ns
t_{SD1}	Time Skew between SYNC CLOCK Negative Edge and SYNC DATA Positive Edge	0		10	ns
t_{ZPSR}	Zero Phase Start Trigger Bit Targeting Accuracy, READ GATE Activation (READ) (Note 4)		2		ns
t_{PWPC}	Width of PCT, PU or PD Outputs in Fully Stabilized Lock (ERD Free of Jitter); R-Pull-Down = 510Ω		10		ns
$\Delta f_{VCO}/f_{RFC}$	Automatic f_{VCO} Range Limiting		50		%
t_{HOLD}	SYNC CLOCK Rest Period (Logical One) at Assertion or De-Assertion of READ GATE	½		3	T_{VCO}
t_{PDT}	SCK Negative Edge to PREAMBLE DETECTED Positive Edge at End of Detection Sequence			25	ns
L_{PDT1}	Length of Valid 1T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	33	34	35	ERD Pulses
L_{PDT2}	Length of Valid 2T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	32	33	34	ERD Pulses
L_{PDT3}	Length of Valid 3T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	31	32	33	ERD Pulses
L_{PDT4}	Length of Valid 4T Preamble Pattern Required for Occurrence of PREAMBLE DETECTED	15	16	17	ERD Pulses
t_S	Window Strobe Time Step (M = Hex Value of Bits 0–3 in CONTROL REGISTER; Bit 4 = Sign Bit)		M × (1.8%) × t_{RFC}		ns
$t_{RFC-SCK1}$	Positive Transition Propagation Delay from REF CLOCK INPUT to SYNC CLOCK OUTPUT, READ GATE Low			15	ns
$t_{RFC-SCK0}$	Negative Transition Propagation Delay from REF CLOCK INPUT to SYNC CLOCK OUTPUT, READ GATE Low			15	ns

Note 1: The DP8459V-10 static window specification, t_T, applies only to the factory-tested 2,7-code data rate of 10 Mb/s (with RS0,1,2 = 010) and with the component values as listed in *Figures 5* and *10*, test configuration as shown in *Figure 23*, test procedure as shown in *Figure 24*, and strobe word M = −2. Significant variation in t_T as a percentage of the VCO period due to the use of other filters and data rates is not expected.

Note 2: The DP8459V-25 static window specification, t_T, incorporates the DP8459V-10 window specification and, in addition, the factory-tested 2,7-code data rate of 20 Mb/s (with RS0, 1, 2, = 000), with the component values as listed in *Figures 5* and *10*, test configuration as shown in *Figure 23*, test procedure as shown in *Figure 24*, and strobe word M = −3. Significant variation in t_T as a percentage of the VCO period due to the use of other filters and data rates is not expected.

Note 3: $I_{IN} = V_{CC}/(4 \times R_{IN})$. $R_{IN} = R_{NOM}$ (HGD High) or $R_{NOM} || R_{BOOST}$ (HGD Low).

Note 4: t_{ZPSR} (ZPS Read) gauges the accuracy with which the ZPS circuitry aligns the VCO to the triggering ERD bit internally (i.e., initial phase step) at the completion of a ZPS operation following READ GATE assertion.

DC Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	V_{CC}−2V	V_{CC}−1.6V		V
V_{OL}	Low Level Output Voltage (Note 4)	V_{CC} = Min, I_{OL} = Max			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−200	μA
I_O	Output Drive Current (Note 1)	V_{CC} = Max, V_O = 2.125V	−12		−110	mA
I_{CPO}	Charge Pump Output Current (K1)	100 ≤ I_{Rp} ≤ 1000 (Note 2)	1.7 I_{Rp}	2.0 I_{Rp}	2.5 I_{Rp}	μA
$I_{CPO-OFF}$	Charge Pump Output Inactive Current	100 ≤ I_{Rp} ≤ 1000 (Note 2)	−0.85		+0.85	μA
I_{VCOI}	VCOI Offset Current	VCOI Voltage 1.5V	−0.25		+0.25	μA
V_{RNOM}	Voltage across R-NOM Resistor	1.2 kΩ ≤ R-NOM ≤ 12 kΩ	Typ. −18%	0.26 V_{CC}	Typ. +18%	V
V_{RBST}	Voltage across R-BOOST Resistor	1.2 kΩ ≤ R-BOOST ≤ 12 kΩ	Typ. −18%	0.26 V_{CC}	Typ. +18%	V
I_{CC1}	Supply Current, Nominal Strobe	V_{CC} = Max (Note 3)			190	mA

Note 1: This value has been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

Note 2: $I_{Rp} = I_{NOM} + I_{BOOST}$.

Note 3: I_{CC1} is measured with the window strobe set at nominal timing (Strobe Bits 0 through 5 = 0,0,0,0,0,0); VCO operating at maximum allowed frequency within any given range selection. I_{CC} typically increases by 30 mA when the strobe is set at the maximum early position (M = −15). This is not a linear increase per step. Most of the increase occurs as the −15 step is approached. I_{CC} decreases as the window is moved late.

Note 4: PUMP UP and PUMP DOWN outputs have no current sinking capability and thus are excluded from this specification.

External Component Selection

Symbol	Parameter	Min	Typ	Max	Units
R_{NOM}	Charge Pump Nominal Operating Current Setting Resistor (Note 1)	1.2		12	kΩ
R_{BOOST}	Charge Pump Boost Current Setting Resistor (Note 1)	1.2		∞	kΩ
C_{NOM}	R_{NOM} Bypass Capacitor (Note 2)	0.01			μF
C_{BOOST}	R_{BOOST} Bypass Capacitor (Note 2)	0.01			μF
R_{PU}	PUMP UP Open Emitter Output Pull-Down Resistor	510			Ω
R_{PD}	PUMP DOWN Open Emitter Output Pull-Down Resistor	510			Ω

Note 1: The minimum allowed value for the parallel combination of R_{NOM} and R_{BOOST} is 1.2 kΩ.

Note 2: C_{NOM} and C_{BOOST} should be high quality, high frequency type.

3.0 PLL Applications: Loop Filter Design

In order to maintain greatest design flexibility for the Customer, all PLL filter components and Charge Pump gain setting elements reside external to the DP8459. All PLL dynamics are thus under the control of the system designer. The following is a brief analysis of the DP8459 PLL; Section 3.1 contains a derivation of component values based on projected requirements within an example hard disk drive system.

Figure 16 represents the DP8459 PLL in simplified form.

Mathematical gain representations for each block are:

$K_{PG} = 1/N$ Pulse Gate equivalent gain

$K_{PC} = 1/(2\pi)$ Phase Comparator gain

$K_{CP} = V_{CC}/2R_p$ Charge Pump gain where

$R_p = R_{NOM}$, HGD high;

$R_p = R_{NOM} || R_{BOOST}$, HGD low

$K_{VCO} = 1.2\ \omega_O$ VCO gain (ω_O = operating center frequency)

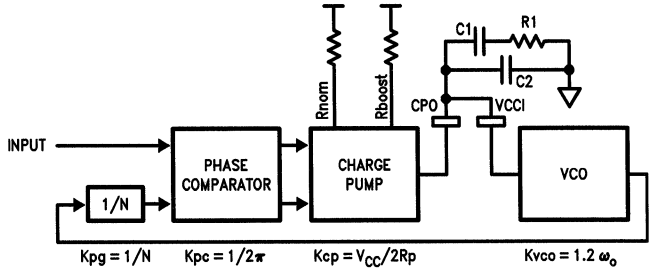

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FIGURE 16. Basic DP8459 Phase Locked Loop Block Diagram

3.0 PLL Applications: Loop Filter Design (Continued)

N is defined as the number VCO cycles per recorded ENCODED READ DATA pulse, or conversely, the ratio of the VCO frequency to the ENCODED READ DATA frequency. The aggregate block gain equation (excluding the loop filter) can be written as:

$$K_B = 1.2\, V_{CC}\, f_O/(2R_pN)$$

The impedance of the loop filter is

$$Z(s) = \frac{1}{sC_2} \| \left(\frac{1}{sC_1} + R_1\right) = \frac{1 + sR_1C_1}{sC_1(1 + C_2/C_1 + sR_1C_2)}$$

The open loop system response G(s) is given by

$$G(s) = \frac{K_B}{s} \times \frac{1 + sR_1C_1}{sC_1\,(1 + C_2/C_1 + sR_1C_2)}$$

This last equation reveals the PLL with this filter configuration is a third order system, which is typically difficult to analyze. However, if $C_2 << C_1$, it can be argued that the behavior of the third order loop closely resembles that of a second order system, allowing for a greatly simplified analysis.

If $C_2 << C_1$, the impedance Z(s) approximates to

$$\frac{1 + sR_1C_1}{sC_1}$$

The overall open loop gain (including the filter) is then

$$G(s) = \frac{K_B}{s} \times \frac{1 + sR_1C_1}{sC_1}$$

Substituting K_B into the equation,

$$G(s) = \frac{1.2\, f_o\, V_{CC}}{s2N} \times \frac{1 + sR_1C_1}{sR_pC_1}$$

$\tau_1 = R_pC_1$ and $\tau_2 = R_1C_1$ are the pole and zero, respectively, which govern the system response. The closed loop gain H(s) is

$$H(s) = \frac{\phi_{OUT}}{\phi_{IN}} = \frac{G(s)}{1 + G(s)}$$

Substituting,

$$H(s) = \frac{K_B\,(sR_1C_1 + 1)}{s^2C_1 + K_B\,(sR_1C_1 + 1)}$$

$$= \frac{(K_B/C_1)(sR_1C_1 + 1)}{s^2 + sK_BR_1 + K_B/C_1}$$

The second order characteristic equation can be written as follows:

$$s^2 + sK_BR_1 + K_B/C_1 = s^2 + s2\zeta\omega_n + \omega_n^2$$

Extracting the component values from these results,

$$C_1 = \frac{K_B}{\omega_n^2} = \frac{1.2\, V_{CC}\, f_o/(2R_pN)}{\omega_n^2}$$

$$R_1 = \frac{2\zeta\omega_n}{K_B} = \frac{2\zeta\omega_n}{1.2\, V_{CC}\, f_o/(2R_pN)}$$

$$C_2 \leq (1/10)\, C_1$$

Thus, one is able to select component values in accordance with specific system requirements, i.e., with given VCO center frequency (equivalent to REFERENCE CLOCK frequency), R_p (in either high or low gain mode), N (the ratio of the VCO frequency to the ENCODED READ DATA frequency), the desired natural frequency of the loop, and the desired damping ratio.

The natural frequency and the damping ratio may be extracted from the component values to determine system behavior under various conditions (differing data patterns, i.e., varying N value; high gain or low gain; read or non-read mode):

$$\omega_n = [1.2\, V_{CC}\, f_o/2R_pNC_1)]^{0.5} \quad \text{Natural frequency}$$

$$\zeta = \omega_n R_1C_1/2 \quad \text{Damping ratio}$$

3.1 2,7 CODE, 10 MBIT/SEC LOOP FILTER DESIGN EXAMPLE

Initial Requirements and Definitions

This example illustrates a 10 MBit/sec 2,7 hard disk system employing a 4T preamble field (recorded at ¼ the VCO frequency, i.e., N = 4). The component derivations are not meant to produce values which will be optimum for all systems employing this data rate, code, and preamble type; this exercise is for exemplary purposes only. (See National Semiconductor Advanced Peripheral Processing Solutions Mass Storage Handbook #1, 1986, AN-413, section 3.4, pages 1-43 through 1-48 for additional information regarding disk system PLL filter design.)

Although the DP8459 provides a frequency acquisition feature intended for use within the preamble, this design example will be approached so as to achieve PLL dynamics which will avoid the cycle-slipping phenomenon frequency-lock action is normally employed to accommodate. Thus, the design will be valid both for systems which do employ frequency lock as well as for those which do not. Advantages gained by the use of frequency-lock beyond that of extended lock-in range, however, such as harmonic false lock avoidance and quadrature lock avoidance, make the use of this feature strongly advisable even with the intrinsic lock-in range achieved by design in this example.

The DP8459 is configured here with the $\overline{\text{FREQ LOCK CONTROL}}$ input tied to the PREAMBLE DETECTED output, the HIGH GAIN DISABLE input tied to the READ GATE input, and the CHARGE PUMP OUTPUT tied to the VCO INPUT pin as well as to the external loop filter components (see *Figure 17*). This establishes self-regulated frequency lock control, READ GATE regulated Charge Pump gain, and single node loop filtering.

3.0 PLL Applications: Loop Filter Design (Continued)

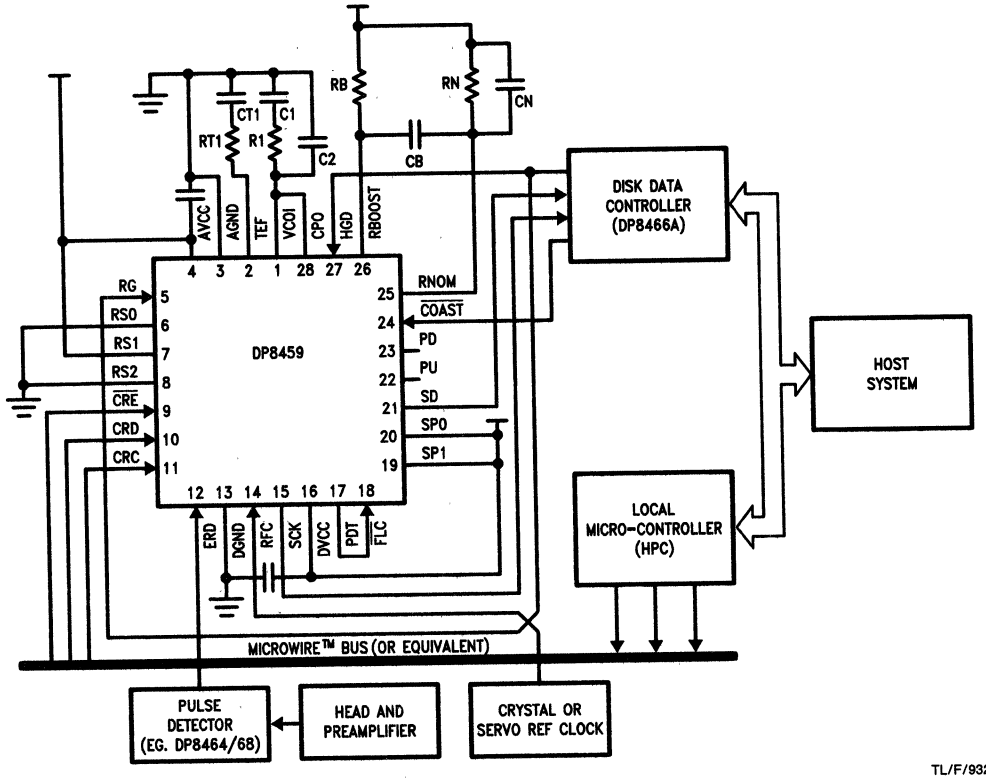

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FIGURE 17. DP8459 in a Typical System Configuration

3.0 PLL Applications: Loop Filter Design (Continued)

System constraints:

$f_{NRZ\ DATA}$ = 10 Mbit/sec

f_{VCO} = 20 MHz

$f_{REFERENCE\ CLOCK}$ = 20 MHz

Code type = ½ (2, 7)

N_{min} = 3 (highest recorded frequency)

N_{max} = 8 (lowest recorded frequency)

$N_{preamble}$ = 4 ($f_{preamble}$ = 5 MHz)

Preamble Length = 11 NRZ bytes (ESDI min.) = 8.8 μs (44 recorded pulses)

Disk formatting = pseudo hard sectored

The DP8459 provides a zero phase start function which minimizes the initial phase step encountered at the start of preamble lock acquisition and thus the phase stabilization time within the preamble is significantly reduced with respect to a fully random-phase lock sequence. However, the PLL will encounter a finite frequency step at the start of preamble acquisition due to variations in disk rotational velocity which may be as large as ±1% (more pronounced in exchangable media systems). The lock-in range of the PLL at the time of preamble acquisition must then be at least ±0.01 x $f_{preamble}$. Given that the PLL lock sequence involves only an adjustment to a frequency step, the following requirements will be set for final PLL dynamics within the filter design procedure:

1. Residual phase error θ_e at the end of the preamble (a full 11 NRZ bytes allowed for PLL stabilization) will be 2 ns or less (4% of the total synchronization window).
2. The lock-in range $\Delta\omega_L$ must be at least 1.5 times the expected frequency step range.
3. The minimum 3 dB bandwidth $\omega_{-3\ dB}$ in the data field must be twice the expected maximum mechanical vibration frequency (10 kHz).
4. The natural frequency of the loop ω_n and damping ratio ζ will be minimized in the data field in order to achieve a high level of jitter rejection. (Minimum damping ratio ζ will be 0.5 (phase margin of 52°) for adequate stability).
5. Re-lock time to the REFERENCE CLOCK will be minimized.

First, some definitions will be established. Regarding requirement #1, the equations for phase error due to a frequency step are[1]:

$$\theta_e(t) = [\Delta\omega/\omega_n]\,[1/(1-\zeta^2)^{0.5}\sin(1-\zeta^2)^{0.5}\omega_n t]\exp(-\zeta\omega_n t) \quad \text{for } \zeta < 1;$$

$$\theta_e(t) = [\Delta\omega/\omega_n]\,[\omega_n t]\exp(-\omega_n t) \text{ for } \zeta = 1;$$

$$\theta_e(t) = [\Delta\omega/\omega_n]\,[1/(\zeta^2-1)^{0.5}\sinh(\zeta^2-1)^{0.5}\omega_n t]\times \exp(-\zeta\omega_n t) \text{ for } \zeta > 1.$$

These equations are plotted in *Figure 18*. The equations for phase error due to a phase step are[1]:

$$\theta_e(t) = \Delta\theta\{\cos(1-\zeta^2)^{0.5}\omega_n t$$

$$-[\zeta/(1-\zeta^2)^{0.5}]\sin(1-\zeta^2)^{0.5}\omega_n t\}\exp(-\zeta\omega_n t) \text{ for } \zeta<1;$$

$$\theta_e(t) = \Delta\theta[1-\omega_n t]\exp(-\omega_n t) \text{ for } \zeta = 1;$$

$$\theta_e(t) = \Delta\theta\{\cosh(\zeta^2-1)^{0.5}\omega_n t-$$

$$[\zeta/(\zeta^2-1)^{0.5}]\sinh(\zeta^2-1)^{0.5}\omega_n t\}\exp(-\zeta\omega_n t) \text{ for } \zeta>1.$$

(These equations are plotted in *Figure 19* and are supplied for informational purposes only; an ideal zero phase start function would not produce a phase step at lock initiation.)

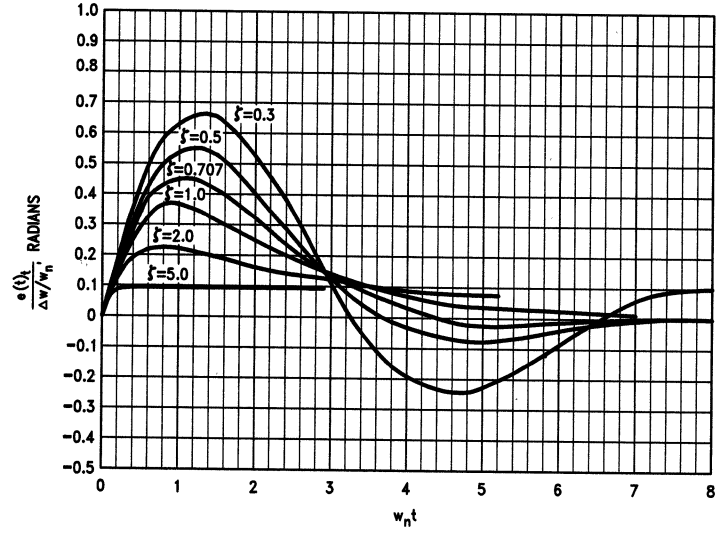

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FIGURE 18. Transient Phase-Error Versus the Dimensionless Parameter $\omega_n t$ Due to a Step in Frequency for Various Loop Damping Factors, ζ (from Ref. 4 by Permission of L. A. Hoffman)

3.0 PLL Applications: Loop Filter Design (Continued)

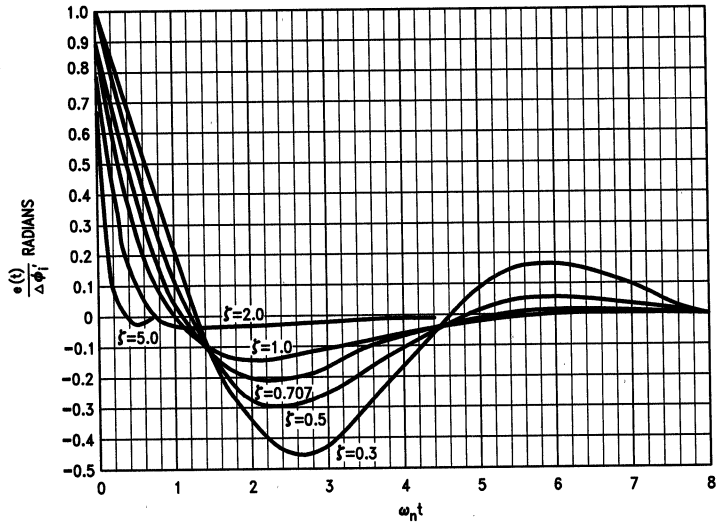

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FIGURE 19. Phase-Error Versus the Dimensionless Parameter $\omega_n t$ Due to a Step in Phase for Various Loop Damping Factors, ζ (from Ref. 4 by Permission of L. A. Hoffman)

Note that the phase error θ_e is measured with respect to the divided (or gated) VCO phase, i.e., 2π radians = N/(20 MHz) = 200 ns in this example.

Regarding requirement #2, the lock-in range (with no cycle-slipping) can be shown to be equal to the open loop transfer function multiplied by the loop filter impedance evaluated at infinite frequency[2]:

$$\Delta\omega_L \approx \pm K_B Z_f(s)|_{s \to \infty}$$

The 3 dB bandwidth for requirement #3 is defined by the equation[3]:

$$\omega_{-3\,dB} = \omega_n [2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{0.5}]^{0.5}$$

Requirement #4 has been established in order to maximize the available window margin via PLL dynamics. Conceptually, window margin is preserved if the loop phase response to individually displaced bits (jitter) is not allowed to cause subsequent windows to be readily shifted from the "average" position. Any window movement from nominal position can readily degrade the window margin. It can be seen from *Figure 19* that systems employing low values of damping ratio exhibit a reduced instantaneous response to phase step and thus display improved jitter rejection with respect to higher damping ratio systems. Damping ratio, fortunately, is easily regulated by loop filter design. It also follows that a low natural frequency and its associated "slower" instantaneous phase response will assist in achieving the goal of jitter rejection. However, the minimum natural frequency limit for the PLL may actually be imposed on the system by the $\theta_e(t)$ settling time requirement, the $\Delta\omega_L$ requirement, or the $\omega_{-3\,dB}$ requirement. Whichever of these produces the highest minimum ω_n value must, by necessity, dominate in the design. The goal of minimizing the natural frequency in order to maximize jitter rejection, therefore, may have to defer to one of these other three criteria.

Requirement #5 is addressed in three ways: 1) the DP8459 itself engages the frequency discriminating action of the Phase Comparator whenever the READ GATE is deasserted and the PLL locks to the REFERENCE CLOCK signal, thus guaranteeing re-lock regardless of the initial frequency step; 2) tying the HIGH GAIN DISABLE pin to the READ GATE input places the Charge Pump in the high gain mode whenever the PLL is locked to the REFERENCE CLOCK, producing an elevated natural frequency and a more rapid locking action; 3) N = 2 whenever the READ GATE is deasserted, which, in this example, effectively increases the loop gain by another factor of 2 with respect to the gain within the preamble, where N = 4.

Determining PLL Response Characteristics

It is expected that the minimum value of ω_n will be determined by the residual phase error requirement of #1 rather

3.0 PLL Applications: Loop Filter Design (Continued)

than the lock-in range requirement of #2 or the $\omega_{-3\ dB}$ requirement of #3. This assumption will be checked at the end of the analysis. System requirements then are as follows:

1. $\theta_e(t) \leq (2\ ns) \times (2\pi\ rad/\ 200\ ns) = 0.063$ radians, where t = preamble length 8.8 μs
2. $\Delta\omega_L \approx \pm K_B Z_f(s)|_{s \rightarrow \infty} \geq 0.015 \times 5\ MHz \times 2\pi = 471\ Krad/sec$
3. $\omega_{-3\ dB} = \omega_n[2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{0.5}]^{0.5}$
   $\geq 2 \times 10\ kHz \times 2\pi = 126\ Kr/s$

Requirement #1 calls for $\theta_e(8.8\ \mu s) \leq 0.063$ radians. Damping ratio ζ varies as the inverse square root of N (see the equation for Damping Ratio in Section 3.0) such that $\zeta_{PREAMBLE} = \sqrt{(N_{MAX}/N_{PREAMBLE})} \times \zeta_{MIN} = \sqrt{2} \times 0.5 = 0.707$. Solving the appropriate equation for $\theta_e(t)$ for various values of ω_n with $\zeta = 0.707$, t = 8.8 μs and an expected frequency step of $0.01 \times 5\ MHz \times 2\pi = 314\ Kr/s$:

ω_n	θ_e (8.8 μs)	$\lvert t_e \rvert$
200 Kr/s	0.606 rad	19.29 ns
300 Kr/s	0.219 rad	6.97 ns
400 Kr/s	0.056 rad	1.78 ns
500 Kr/s	0.0012 rad	0.038 ns
600 Kr/s	−0.0098 rad	0.312 ns
700 Kr/s	−0.008 rad	0.026 ns

$\theta_e(8.8\mu s)|_{400\ Kr/s} = 0.056$ radian < 0.063 radian

$t_e = 0.056$ radian $\times$ 200 ns/2π radian $= 1.78$ ns < 2 ns

Thus 400 Kr/s is chosen as the desired natural frequency within the preamble to satisfy requirement #1.

If the assumption that $\theta_e(t)$ dominates the minimum natural frequency requirement is correct, then the $\Delta\omega_L$ requirement of #2 and the $\omega_{-3\ dB}$ requirement of #3 should be met by the ω_n obtained above. First, examining requirement #2,

$$Z_f(s)|_{s \rightarrow \infty} = R_1 \text{ } (C_2 \text{ neglected}).$$

Thus,

$$\Delta\omega_L = K_B R_1$$

Rearranging for R_1:

$$R_1 = \Delta\omega_L / K_B$$

The equation for R_1 previously derived shows

$$R_1 = 2\zeta\ \omega_n / K_B$$

Thus,

$$\Delta\omega_L / K_B = 2\zeta\omega_n / K_B$$

$$\Delta\omega_L = 2\ \zeta\omega n$$

In this case, $\omega_n = 400$ Kr/s and $\zeta = 0.707$ (preamble), thus

$\Delta\omega_L = 400\ Kr/s \times 2 \times 0.707 = 566\ Kr/s > 471\ Kr/s$

Thus, requirement #2 is met.

Examining requirement #3, where $\omega_{-3\ dB} \geq 2 \times 10\ kHz \times 2\pi$ when N equals its maximum value of 8 (minimum frequency data pattern; $\zeta = 0.5$):

$\omega_n(min) = \omega_n(preamble) \times 1/\sqrt{(N_{MAX}/N_{PREAMBLE})}$

$= 400\ Kr/s \times 1/\sqrt{2} = 283\ Kr/s$

$\omega_{-3\ dB} = \omega_{n(min)}\ [2\zeta^2 + 1 + \{(2\zeta^2 + 1)^2 + 1\}^{0.5}]^{0.5}$

$= 283\ Kr/s \times 1.817 = 514\ Kr/s$

$514\ Kr/s \div 2\pi = 82\ kHz > 2 \times 10\ kHz$

Thus requirements #1 through #3 are met, and #4 defers to the minimum ω_n established by #1.

Regarding requirement #5, the DP8459 has been configured externally in this example such that when the READ GATE is deasserted, the loop gain will be increased by a factor of 2 due to the Charge Pump gain switching ($R_{NOM} = R_{BOOST}$; HGD tied to RG) and by an additional factor of 2 due to the decrease in N from 4 (preamble) to a fixed internal value of 2. The resulting factor of 4 effective gain elevation results in an increase in both the natural frequency, ω_n, and the damping ratio, ζ, by $\sqrt{4} = 2$. Thus, when READ GATE is deasserted,

$$\omega_n = 2 \times 400\ Kr/s = 800\ Krad/s$$

$$\zeta = 2 \times 0.707 = 1.414$$

$$\Delta\omega_L = 2\zeta\omega_n = 2 \times 1.414 \times 800\ Krad/s = 2.3\ Mr/s$$

COMPONENT CALCULATIONS

The formulae for the filter components, derived previously, are

$$C_1 = \frac{K_B}{\omega_n^2} = \frac{1.2\ V_{CC}\ f_o/(2R_pN)}{\omega_n^2}$$

$$R_1 = \frac{2\zeta\omega_n}{K_B} = \frac{2\zeta\omega_n}{1.2\ V_{CC}\ f_o/(2R_pN)}$$

$$C_2 \leq (1/10)\ C_1$$

A 2:1 ratio of high-to-low Charge Pump gain was chosen for the derivation of R_{NOM} and R_{BOOST}. To achieve the 2:1 gain ratio, R_{NOM} must be equal to R_{BOOST} while the parallel combination $R_{NOM} \| R_{BOOST}$ must be equal to or greater than 1.2 kΩ as per specification. Note that in the equation for C_1 above, the capacitor value is inversely proportional to R_p. Thus, external field interference immunity can be achieved if C_1 is maximized through the minimizing of R_p. The selection of $R_{NOM} = R_{BOOST} = 2.4$ kΩ satisfies the requirements for the Charge Pump resistors and the gain ratio. R_p will be equal to R_{NOM} with READ GATE high, and thus

$C_1 = [1.2 \times 5 \times 20\ MHz/(2 \times 2.4k \times 4)]/(400\ Kr/s)^2$

$= 0.039\ \mu F$

R_1 can now be calculated:

$$\frac{2 \times 0.707 \times 400\ Kr/s}{1.2 \times 5 \times 20\ MHz/(2 \times 2.4k \times 4)} = 90\Omega$$

A standard value of 100Ω is chosen. Since $C_2 \leq 0.1 \times C_1$, C_2 will be chosen to be 510 pF. A table listing the dynamics of the PLL under standard operation conditions and with component values adjusted to industry standards is shown in *Figure 20*.

3.0 PLL Applications: Loop Filter Design (Continued)

Field	Preamble	Min Freq Data	Max Freq Data	Ref Clock
N	4	8	3	2
CP Gain	Low	Low	Low	High
Natural Freq. ω_n	400 Krad/s	283 Krad/s	462 Krad/s	800 Krad/s
Damping Ratio ζ	0.7	0.5	0.8	1.4

FIGURE 20. 2,7 Code, 10 Mbits/Sec Design Example PLL Dynamics

4.0 Window Margin and Bit Jitter Tolerance

A key performance specification for the DP8459 involves the integrity of the synchronization window. The **synchronization window** is defined as a continuously repeating time cell, nominally equal in span to the period of the VCO, within which an ENCODED READ DATA pulse will be recognized (captured) regardless of its position within the window (see *Figure 21*). The captured ERD bit is then transmitted to the SYNCHRONIZED DATA output on the next occurring SYNC CLOCK negative edge. The SYNCHRONIZED DATA and the SYNC CLOCK are held in a fixed, specified timing relationship for use by the data controller in deserialization and decoding. The synchronization window (with strobe setting at nominal position) is centered about the mean location of the ERD pulses via the delay line and the time-averaging action of the PLL. National Semiconductor specifies the **static window truncation** (t_T) of the DP8459 data synchronizer as the maximum expected loss of the synchronization window seen adjacent to the ideal window boundary following complete PLL stabilization with the strobe control setting at the M = −2 position (see *Figure 22*). Static lock conditions are defined as having been achieved when the PLL has been allowed to establish fully stabilized lock to a consistent preamble-type pattern of nominally positioned, non-shifted ERD pulses.

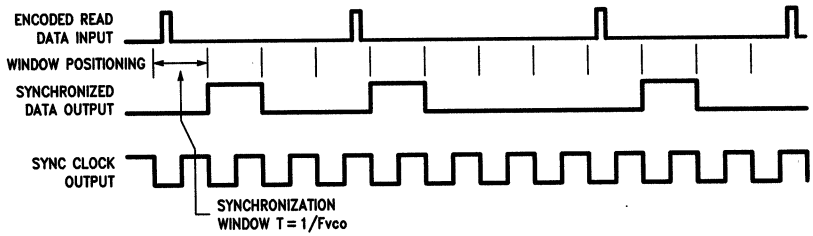

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FIGURE 21. Synchronization Window

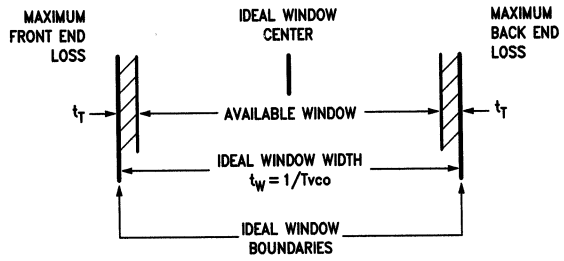

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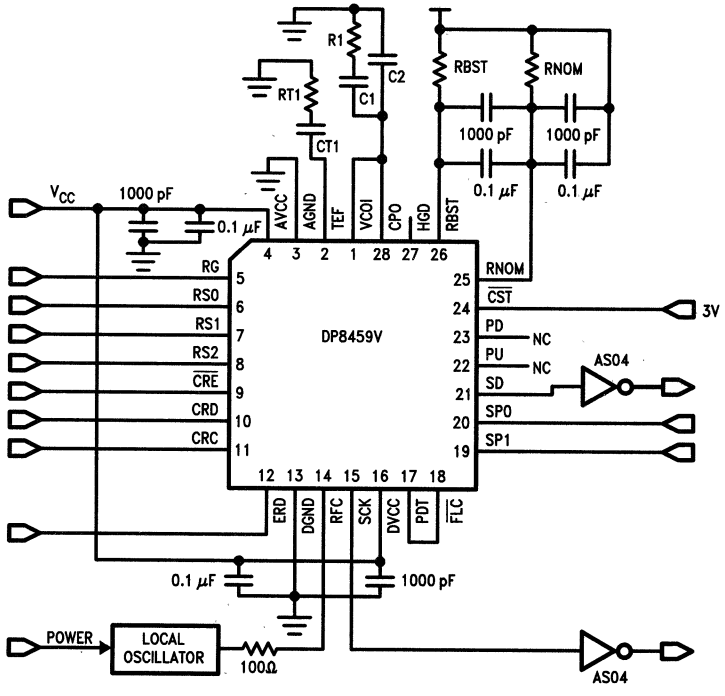
Figure 22. Window Specification Diagram

4.0 Window Margin and Bit Jitter Tolerance (Continued)

4.1 SYNCHRONIZATION WINDOW GENERATION

The DP8459 employs a pulse gate-delay line scheme in the generation of the synchronization window. *Figure 6* shows a simplified block diagram of the pulse gate and delay line circuitry coupled with the phase locked loop. All elements except the delay line are assumed to be delayless for simplicity of analysis. The pulse gate allows a single VCO edge to be transmitted to the pump down input of the phase comparator for each arriving ENCODED READ DATA pulse, while the delay line allows the ENCODED READ DATA pulse to open (enable) the pulse gate at a predetermined time (t_d) prior to the arrival of the ERD pulse at the pump up input of the phase comparator. *Figures 7, 8* and *9* show waveform diagrams of the capture of nominal, early and late ERD pulses, respectively. In normal operation where stable lock has been achieved, the time-integrating action of the PLL has established time alignment between the waveforms at the phase comparator inputs, i.e., both events occur at t_o, on average. If t_d is set equal to $0.5 \times \tau_{VCO}$, the nominal or average ERD pulse will open the pulse gate at $t_o - 0.5 \times \tau_{VCO}$, precisely the midpoint between VCO edges. ERD pulses are then free to shift to any position (ideally) between VCO edges, that is, they have an allowed displacement of $\pm 0.5\ \tau_{VCO}$ from the mean, while yet opening the pulse gate for the passing of the appropriate VCO edge to the phase comparator and at the same time being properly captured by the data synchronization latch (flip-flop D, *Figure 6*). The $\pm 0.5\ \tau_{VCO}$ region is referred to as the synchronization (capture) window.

Any variation in the value of the time delay t_d causes the time at which the pulse gate is enabled ($t_o - t_d$) to shift away from the VCO waveform midpoint, and thus produces a corresponding shift in the position of the synchronization (capture) window. This action, when done in a controlled fashion, is known as window strobing and is useful for purposes of window skew compensation, determination of system window margin, and recovery routines for non-readable data (see Section 4.3).



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Notes: SD and SCK outputs are buffered by Advanced Schottky gates to provide standardized, typical loading conditions.

CRC, CRD, CRE, RG, and ERD are driven by a pattern generator providing the appropriate sequences both to load the control register with the appropriate strobe position information and to cycle the RG and ERD test routine as per *Figure 24*.

FIGURE 23. DP8459 Window Measurement Configuration

4.0 Window Margin and Bit Jitter Tolerance (Continued)

4.2 WINDOW TRUNCATION TESTING

The DP8459 static window truncation specification is an aggregate figure within which the window margin loss contributions from all relevant blocks in the data synchronization chain are combined into the single parameter, t_T.

The preliminary DP8459 static window specification, t_T, applies only to the factory-tested data rates of 10 Mb/s (with RS0,1,2 = 010) and 20 Mb/s (with RS0,1,2 = 000), with the component values as listed for each corresponding data rate in *Figures 5,* and *10,* test configuration as shown in *Figure 23,* test procedure as shown in *Figure 24,* and strobe word M = −2 for 10 Mbits/sec and M = −3 for 20 Mbits/sec. Significant variation in t_T due to the use of other filters and data rates is not expected.

The test algorithm employed in the outgoing factory measurement (screening) of t_T emulates an ENCODED READ DATA stream consisting of a long synchronization field with a single, movable test bit at its end. This method is referred to as *static* window testing, since the window in which the test bit is inserted is fully stabilized and unable to react instantaneously to the phase step introduced by the displaced bit. The standard screening procedure employed for determining DP8459 static window truncation is divided into two portions, one which determines the location of the leading (front) window boundary and one which determines the trailing (back) window boundary. The DP8459 is made to cycle through the read operation many times as a variable bit is moved, once per read cycle, from outside the target window across the ideal leading boundary and into the window. The bit is advanced toward the center of the target window until it resides in a position where it is able to be detected a large number of times consecutively, guaranteeing VCO jitter immunity. The time displacement between the bit's valid detection position and the ideal leading window boundary is recorded as t_{Tf} (front). (This value may be negative if the actual window boundary resides outside the ideal window.) The variable bit is then placed outside the trailing window boundary and the variable bit is again moved, once per read cycle, from outside the target window across the ideal boundary and into the window. The bit continues to advanced toward the center of the recognition region until it is in a position where it is able to be read a large number of times consecutively. The time displacement between the bit's valid detection position and the ideal trailing window boundary is recorded as t_{Tb} (back). (Again, the value may be negative if the actual window boundary resides outside the ideal window due to window encroachment.) The larger (more positive) of the two (t_{Tf}, t_{Tb}) values is taken as t_T. A flow chart of the test sequence is shown in *Figure 24.* Tables of external component values used for production screening of the DP8459 at various data rates are shown in *Figures 5* and *10.*

Window truncation evaluated within data patterns containing shifted bits is a direct function of PLL dynamics which are under Customer control, and thus is neither tested nor specified.

4.3 WINDOW STROBE

The DP8459 incorporates a window strobe function capable of shifting the synchronization window either early or late with respect to its nominal position in small, specified steps. The strobe step t_S is defined as the controlled time displacement of the DP8459 synchronization window from its nominal (strobe centered) position and is typically

$$t_S = M \times [1.8\% \times \tau_{VCO}]$$

where M is the value of the strobe control word (−15 through +15; see *Figure 4*) set by the first 5 bits within the Control Register. (Note that M is equivalent to the hexidecimal value of the five strobe control bits where bits 0 through 3 are the LSB through MSB and bit 4 is the sign bit.)

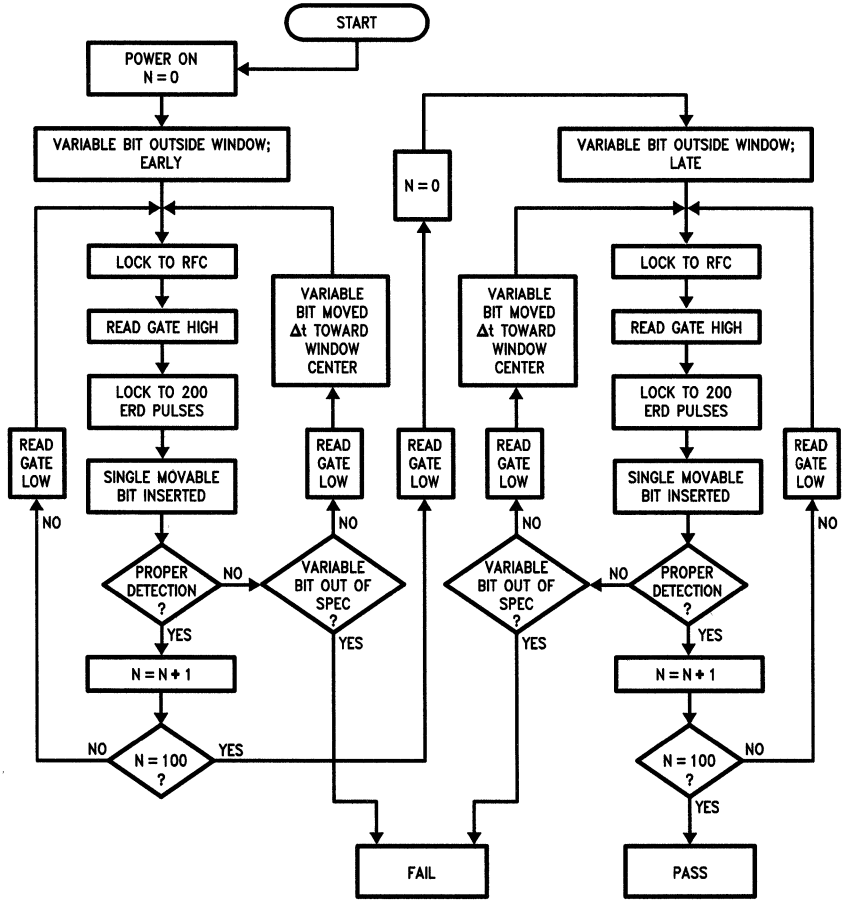
The changing of the strobe value t_S is not an instantaneous event following the changing of the control word in the Control Register. The response time of the strobe control circuitry to any change in strobe setting is a function of the timing elements connected to the TIMING EXTRACTOR FILTER pin and the data rate at which the device is being operated. A finite settling time must be allowed for the delay circuitry to respond following the loading and latching of the new control word (latching occurs and strobe changes begin at de-assertion of CONTROL REGISTER ENABLE, i.e., at transition to logical ONE). It is recommended that any changes to the strobe setting be done with READ GATE deasserted and with a sufficient allowance for settling time prior to the initiation of a subsequent read operation. Approximate settling times are given in *Figure 10* for various TEF component values at specific data rates. (Please refer to AN-578 Window Strobe Function.)

4.3.1 MARGIN TESTING

The read channel window margin of a disk/tape memory system is the portion of the synchronization window remaining after the subtraction of all possible sources of degradation such as media bit shift, head-amplifier anomalies, pulse detector anomalies, cable-induced skew, synchronizer losses, and extraneous noise. The remaining margin must be sufficient to allow the system to perform with an acceptable media error rate under all operating conditions. Acceptable media error rates will vary between systems depending on ECC codes, data redundancy, and other factors. The measured value of the synchronization window margin is often used as a performance criteria for HDA (head-disk assembly) and read channel qualification, and for gauging the probability of encountering data errors on the media.

The DP8459 strobe function can be readily used to measure the window margin within a drive system. Margin tests have been most frequently employed only during outgoing factory tests of storage media systems with specialized and costly test apparatus employed for the purpose; however, the DP8459 allows media/system qualification at any time in the factory or the field during the system's operational life, given the incorporation of an appropriate margin test algorithm within the disk system controller. The algorithm may be configured first to record the most bit-interactive (shift-producing) pattern possible with the recording code being employed (eg., a repeating hex **6D B6** pattern in MFM) in an area of the media where recording density is its highest (inner-most track in constant-angular velocity or constant data rate disk systems), and secondly to read the track repeatedly while incrementally advancing the degree of window "strobe" (controlled shift) first in the early direction until the data error rate crosses a pre-determined threshold and then in the late direction until the same threshold is again crossed. The smaller of the two DP8459 window strobe measurements (either the early or the late value) determined at the error rate threshold crossing points is then equal to the read channel window margin.

4.0 Window Margin and Bit Jitter Tolerance (Continued)



TL/F/9322–25

FIGURE 24. DP8459 Static Window Truncation Test Flow Chart

4.0 Window Margin and Bit Jitter Tolerance (Continued)

4.3.2 ERROR-BOUND SECTOR/TRACK DATA RECOVERY

A standard technique exists for attempting to recover illegible data from a sector or track within a disk system which involves the re-reading of the bad data while shifting the data synchronizer window a small amount early/late with respect to the nominal position. A typical early/late strobe value for data retrieval is in the range from approximately 2% to 3% of the total window width. The strobe step size produced by the DP8459 window control circuitry easily allows for this type of data recovery procedure, and is in fact small enough to feasibly permit more than one degree of window movement within the data recovery algorithm.

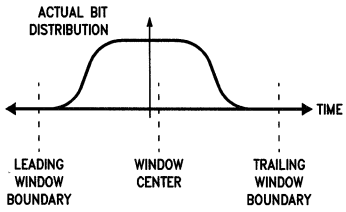
4.3.3 AUTO WINDOW ALIGNMENT (DE-SKEW ROUTINE)

It is possible to configure an intelligent drive system to employ the DP8459 strobe feature in a window auto-calibration (de-skew) routine implemented to center the detection window about the mean position of the bit distribution curve. The de-skew routine would maximize the read channel window margin and correspondingly minimize the bit error rate (BER). The auto-calibration routine would be configured as an extension of the window margin routine (Section 4.3.1), where the early and late strobe values determined at the error rate threshold crossing points would be numerically combined to determine the window center skew. For example, if at 10 Mb/s the strobe-until-error value in the "early" direction were found to be M = −8 and the "late" value M = 4, window skew would be determined as follows:

$$t_{skew} = 1.8 \times \tau_{VCO} \times [M_{early} + M_{late}]/2$$
$$= 0.9\ ns \times [-8 + 4]/2$$
$$= -1.8\ ns$$

The window has an apparent shift of 1.8 ns in the late direction. The strobe setting in the DP8459 would then be set to compensate for the skew, centering the synchronization window and maximizing the available read channel window margin. In this case, the strobe setting would be M = −2. This routine could be executed at system power-up and perhaps on a regular, specified time schedule during system operation to maintain a fine-tuning of the read channel timing characteristics under varying operating conditions (conceivably eliminating the need for an error-strobe routine).

Original Window Position



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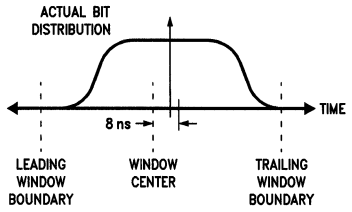
Early Strobe Window Position



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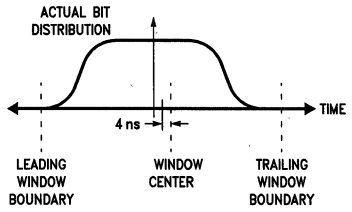
Late Strobe Window Position



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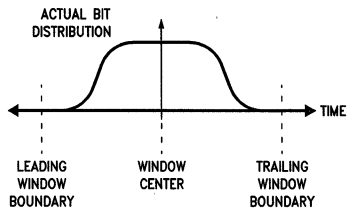
De-Skewed Window Position



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5.0 Multiple Data Rate Applications

The DP8459 may be rapidly and easily switched from one data rate to another, conceivably from its highest to its lowest specified data rate and vice versa, with a minimum of adaptation effort. This capacity facilitates the employment of the DP8459 for stepped data rate disk applications (constant density recording, or CDR), or for the employment of a single data synchronizer for multiple-media controllers as a cost and space conserving measure, e.g., allowing a controller to address tape, floppy disk and hard disk read channels on a multiplexed basis while employing a single data separator. DP8459 data rate changes require only the appropriate new REFERENCE CLOCK frequency be applied and the necessary new RANGE SELECT information be presented to the chip in cases where the Customer chooses to employ compromise loop and Timing Extractor filters. The Customer may alternatively choose to employ a transmission gate technique to multiplex between appropriate filter elements for various operating data rates should the frequencies be sufficiently different (e.g., streaming tape drive versus hard disk drive).

6.0 PC Board Layout Recommendations

The DP8459 data synchronizer circuit has been designed to minimize the sensitivities normally associated with phase locked loops which operate within digital environments, and in particular those within disk and tape memory systems. A list of recommendations and precautions is made available here for the Customer, however, such that the DP8459 environment can be optimized and the best possible performance achieved with the device.

1. A localized V_{CC} supply net or island should be established for the device and all its associated passive components, supplied by but separated from the main V_{CC} plane. The local V_{CC} net should be tied to the main V_{CC} plane at only one point and bypassed to the ground plane at that point.
2. The DP8459 V_{CC} pins should be bypassed to ground through the shortest electrical path possible between the supply pins the ground pins themselves. Bypassing should be achieved with a 0.1 μF ceramic capacitor in parallel with a 1000 pF silver mica capacitor.
3. The main digital ground plane should be used for all grounding associated with the device. Both Analog and Digital ground pins should be tied to this plane.
4. All passive components associated with the DP8459 should be located as close to their respective device pins as possible. Lead length should be minimized.
5. External passive components should be oriented so as to minimize the length of the ground-return path between the component's ground plane tie point and the DP8459 Analog ground pin.
6. In order to minimize pin parasitic capacitances, planing (supply or ground) should not be placed between device pin eyelets.
7. Digital signal lines should not be run adjacent to external passive analog components associated with the device. Digital signal lines should not be run between analog signal pins or traces associated with the device.
8. Digital input noise experience by the device should be minimized, i.e., it may be advisable to condition input waveforms in order to reduce transient noise. This may be done with a series damping resistor at the REFERENCE CLOCK input (and perhaps at the ENCODED READ DATA input) in high frequency systems. This would terminate board traces and thus prevent underdamped, noise-producing switching transients at the device inputs.
9. Digital output loading should be minimized, i.e., if outputs must drive large loads or long traces, employ buffering. Pre-termination of PC traces driven by the SYNCHRONIZED CLOCK and SYNC DATA outputs may be advisable in high frequency systems (i.e., include series resistance equivalent to the characteristic impedance of the PC board trace).
10. All unused digital output pins should be allowed to float, unconnected to any trace.
11. The device should not be located in a region of the PC board where large V_{CC} or ground plane currents are expected, or where strong electric or magnetic fields may be present. The lowest ambient noise region of the board should be chosen for device location.
12. If device socketing is desired, a low-profile, low mutual capacitance, low resistance, forced-insertion socket type should be employed.
13. Wire-wrapping should not be employed, even in an evaluation set-up.
14. Capacitors used for the loop filter, the Timing Extractor filter, and all bypassing purposes should be ultra-stable monolithic ceramic capacitors or equivalent timing quality capacitors. Silver-mica capacitors should be employed for values 1000 pF and below.
15. In order to achieve very close proximity of passive components to the DP8459 device, it is acceptable to have axial-lead resistors standing upright; however, the shorter component lead should be connected to the device pins to obviate noise induction into sensitive nodes.

7.0 Application Support

It is National Semiconductor's policy to offer and maintain a high level of direct Customer support on all of its mass storage products. National's experience in supporting the disk data memory industry has allowed the DP8459 to be designed to directly address the unique challenges of serial data synchronization within the areas of magnetic and optical media data storage and local area networks, facilitating straightforward use of the device in a diverse range of applications. In the event that questions arise regarding the use of the DP8459 or any other associated NSC mass storage device, the Customer is encouraged to contact the Logic Applications Group or Logic Marketing Group at

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Telephone (408) 721-5000

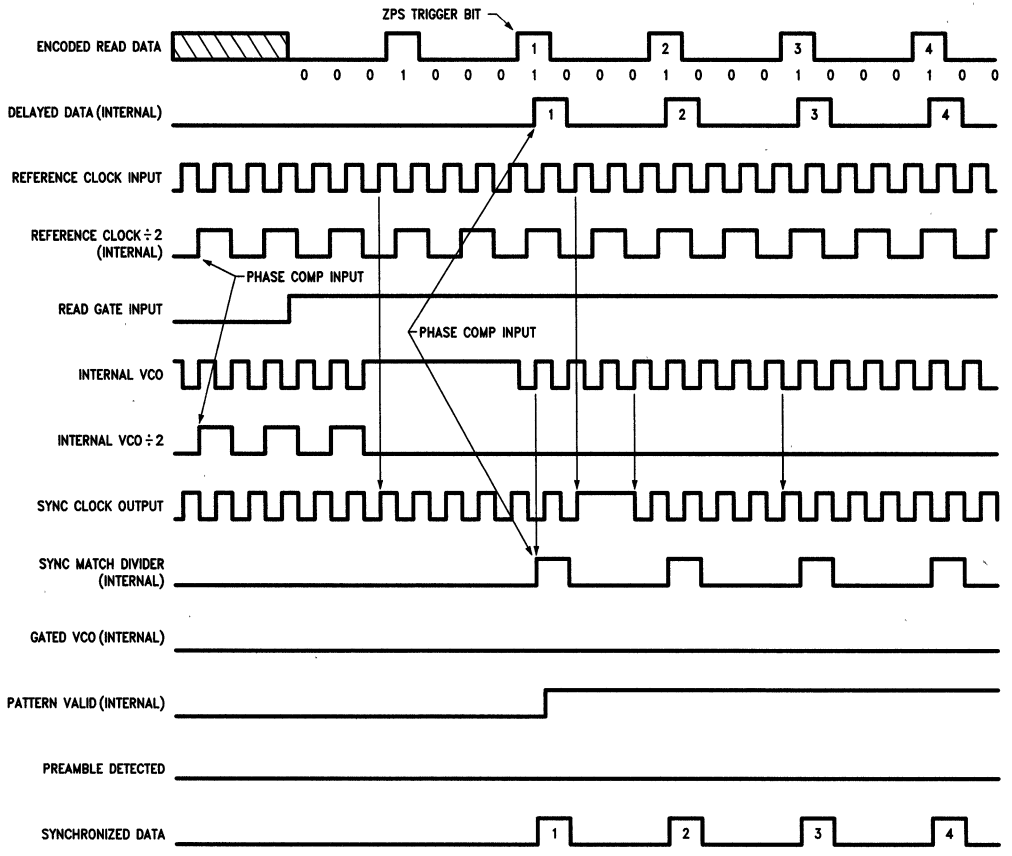

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FIGURE 25. Zero Phase Start Lock Acquistion Sequence and Start of Preamble Detection; Frequency Lock Employed, 4T Pattern

7.0 Application Support (Continued)

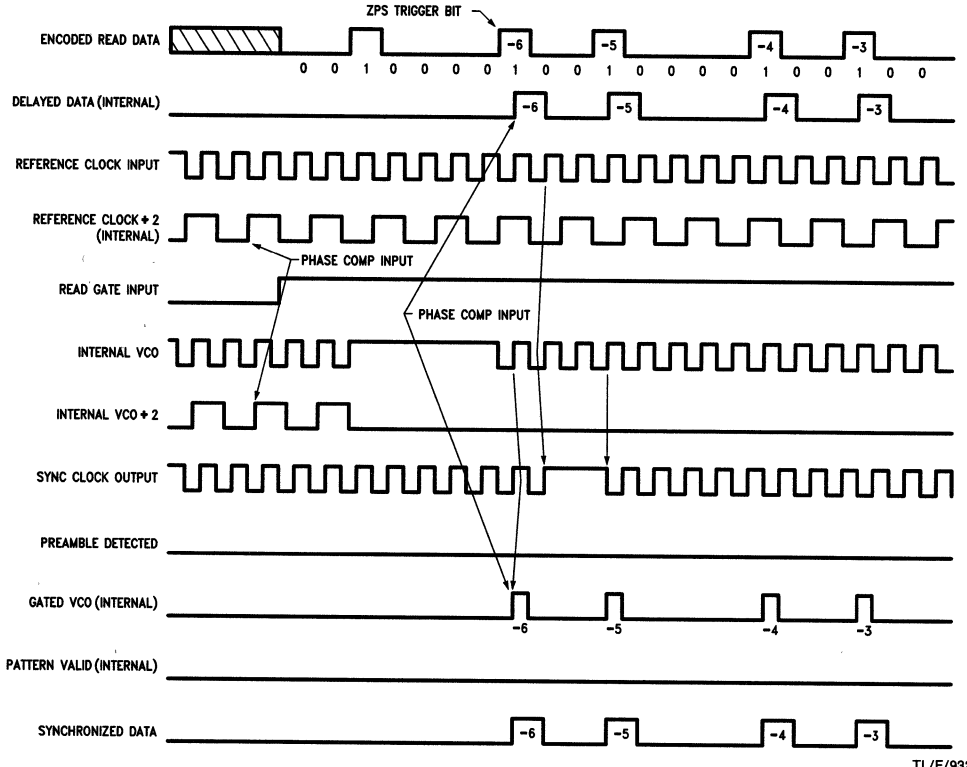

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FIGURE 26. Zero Phase Start Lock Acquisition Sequence, Frequency Lock not Employed (Soft Sectoring)

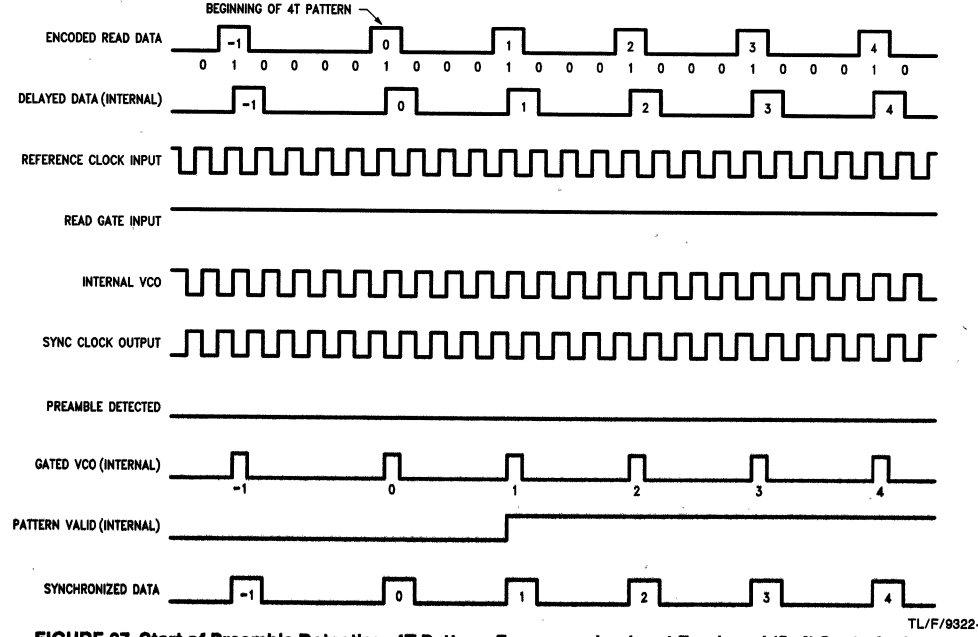

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FIGURE 27. Start of Preamble Detection; 4T Pattern, Frequency Lock not Employed (Soft Sectoring)

7.0 Application Support (Continued)

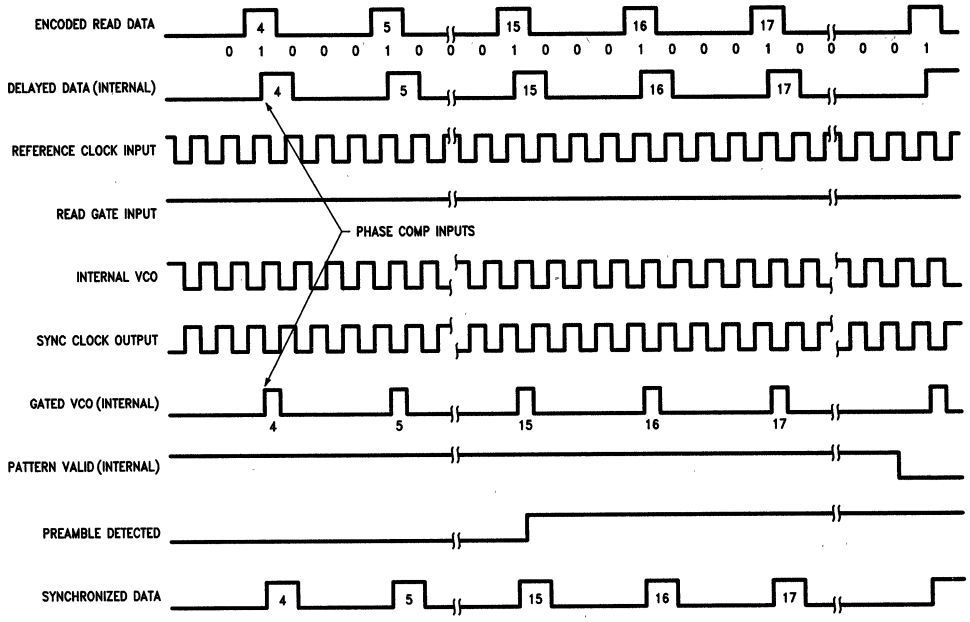

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FIGURE 28. Occurrance of Preamble Detection; 4T Pattern, Frequency Lock not Employed (Soft Sectored)

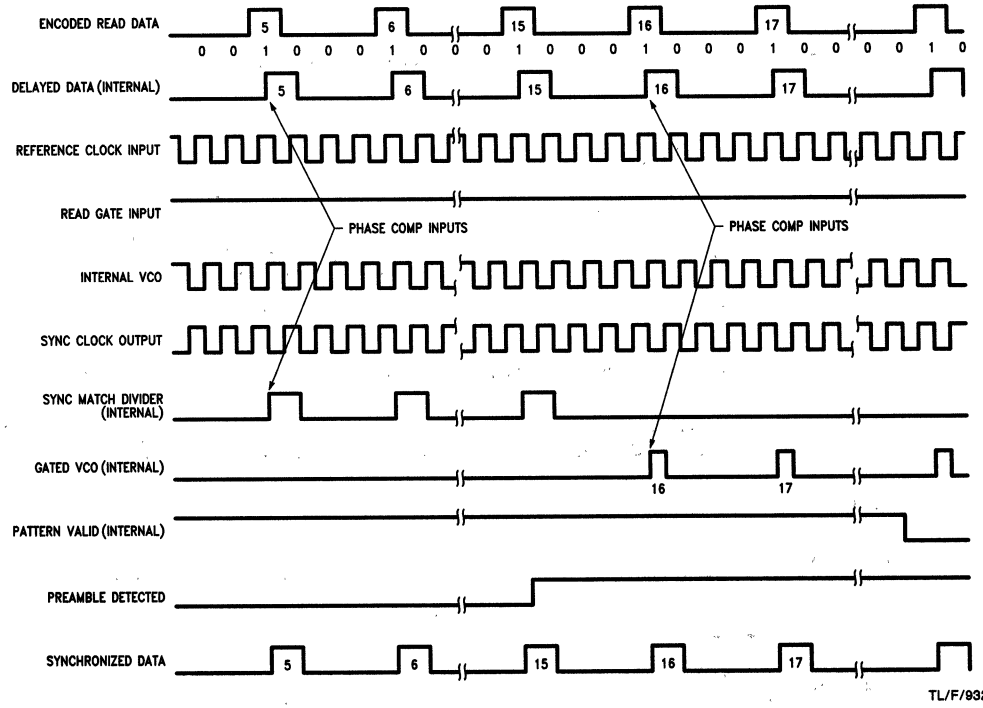

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FIGURE 29. Occurrance of Preamble Detection, Frequency Lock Employed

7.0 Application Support (Continued)

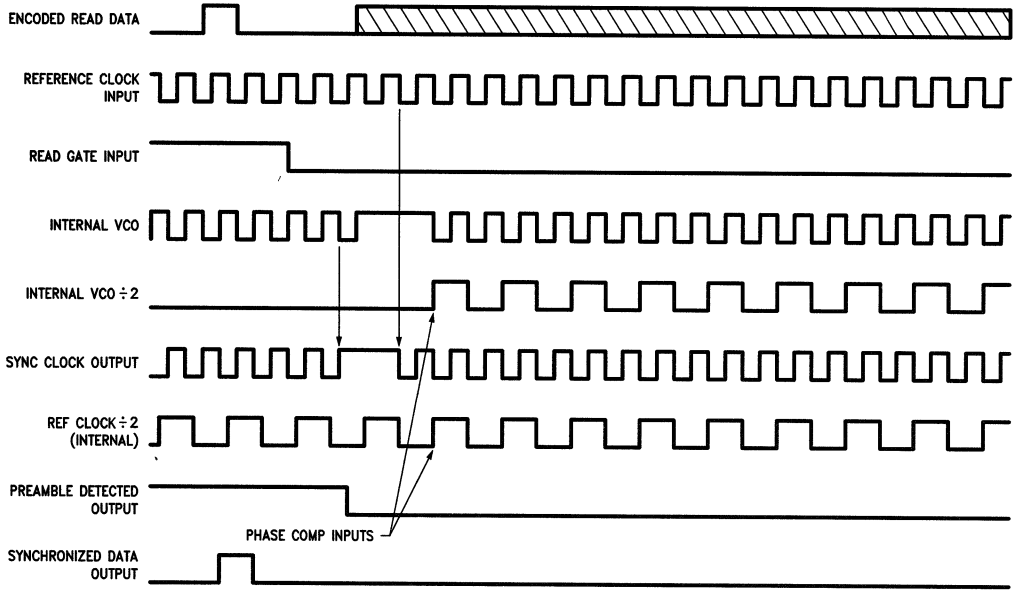

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FIGURE 30. End of Read Cycle; REFERENCE CLOCK Lock Sequence

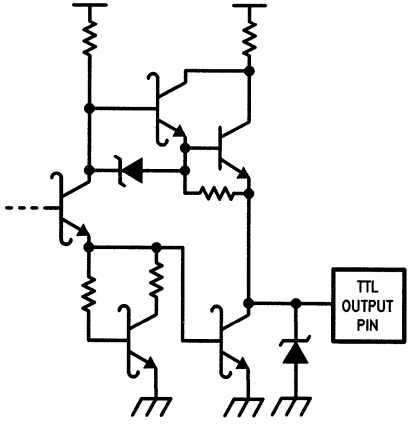

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FIGURE 31. Typical TTL Digital Output

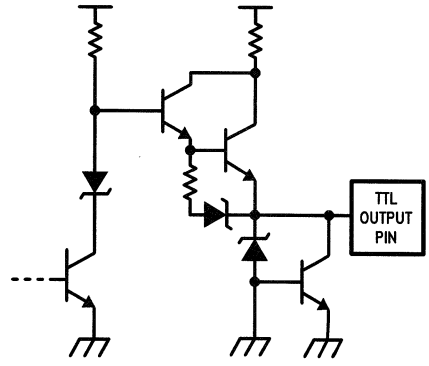

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FIGURE 32. Open Emitter TTL Output (PU and PD Outputs)

7.0 Application Support (Continued)

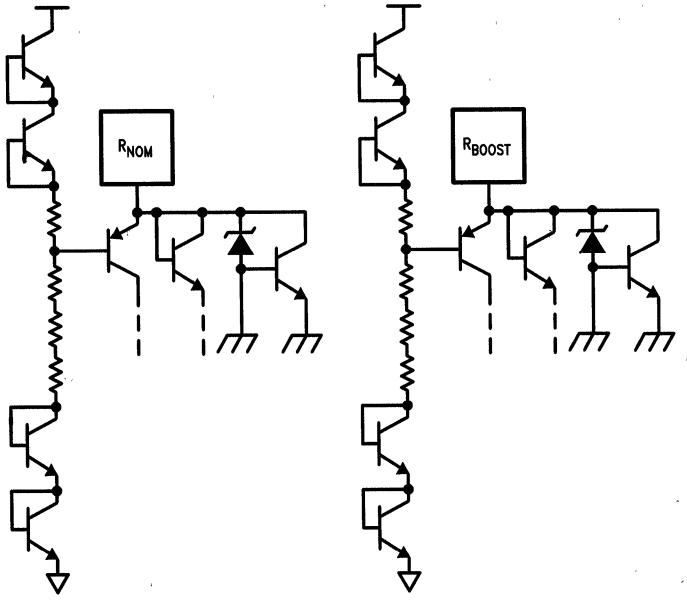

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FIGURE 33. $R_{NOMINAL}$ and R_{BOOST} Pin Configurations

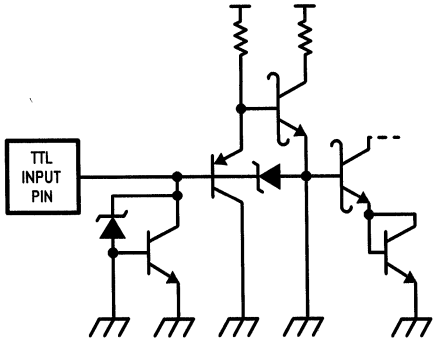

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FIGURE 34. Typical TTL Digital Input

7.0 Application Support (Continued)

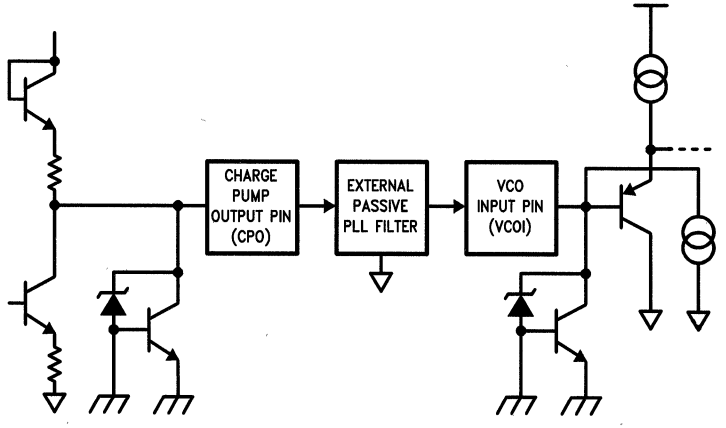

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FIGURE 35. Charge Pump Output and VCO Input Circuit Configurations

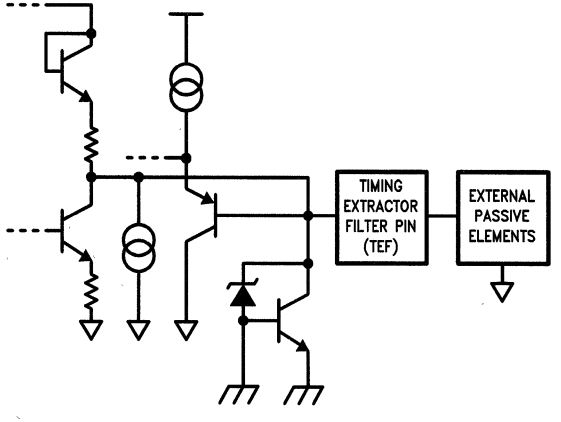

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FIGURE 36. Timing Extractor Filter Pin Circuit Configurations

References

1. *Phaselock Techniques*, Floyd M. Gardner, Second Edition, John Wiley & Sons, 1979, pp. 48.
2. ibid, pp. 70.
3. ibid, pp. 14.
4. *Receiver Design and the Phase Locked Loop*, L.A. Hoffman, Aerospace Corporation, El Segundo, Ca., May 1963.

National Semiconductor

DP8462 2,7 Code Data Synchronizer

General Description

The DP8462 Data Synchronizer is designed for application in disk drive memory systems employing Run Length Limited Codes using 1-0-0 or 1-0-0-0 preamble patterns, and depending on system requirements, may be located either in the drive or in the controller. It receives digital pulses from a pulse detector circuit (such as the DP8464 Disk Pulse Detector) if the DP8462 is situated in the drive, or from an interface if it is situated in the controller. In the read mode, the circuit locks onto and detects either a 100 or 1000 preamble pattern depending on the state of the pattern select input pin. The synchronized data and clock are then available for decoding and deserialization by a decoder circuit. All of the digital input and output signals are TTL compatible and only a single +5V supply is required. Although separate Analog and Digital V_{CC} and Ground pins are provided, they are expected to be tied together by the user. The chip is housed in a standard narrow 24-pin dual-in-line package (DIP) and is fabricated using Advanced Schottky bipolar analog and digital circuitry. This high speed I.C. process allows the chip to work with data rates up to 20 Mbits/sec. There are two versions of the chip, each having a different decode window error specification. These two versions (-3 and -4) will operate from 4 to 20 Mbits/sec, with respectively increasing window errors, as specified in the Electrical Characteristics Table.

The DP8462 features a phase-locked-loop (PLL) consisting of a pulse gate, phase comparator, charge pump, buffering amplifier, and voltage-controlled-oscillator (VCO). Pins are provided for the user to select the values of the external filtering components required for the pulse gate and PLL, the frequency setting components required for the VCO, two current setting resistors for the charge pump, and current setting resistors for the pulse gate that control the delay line.

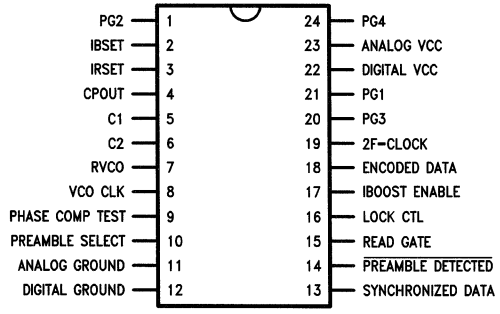
The on-board PLL's phase comparator has two modes of operation: phase and frequency comparison or phase only comparison. In the non-read mode, the comparator performs phase and frequency comparison, but once in the read mode, it switches to phase only comparison. The user selects whether this mode change occurs as soon as read mode is entered or after the preamble pattern is detected. The charge pump also has two modes of operation: high track rate—intended to be used in the non-read mode and in the read mode while acquiring lock, and low track rate—intended to be used in the read mode to retain lock. Both track rates are selected by the user with external components; the user is given control over when the track rate switch takes place.

Features

- Phase-Frequency PLL in non-read mode and during preamble if desired
- Operates at data rates up to 20 Mbit/sec
- Detects either 1-0-0 or 1-0-0-0 preamble patterns
- User determined PLL loop filter network
- PLL charge pump has two user-determined tracking rates
- External control of track-rate switchover
- External control of phase comparator switchover
- Delay line may be externally adjusted if desired
- ORed phase comparator outputs for monitoring bit-shift
- Standard narrow 24-pin DIP or 28-pin Plastic Chip Carrier package
- Less than ½W power consumption
- Single +5V supply

Connection Diagrams

Dual-In-Line Package



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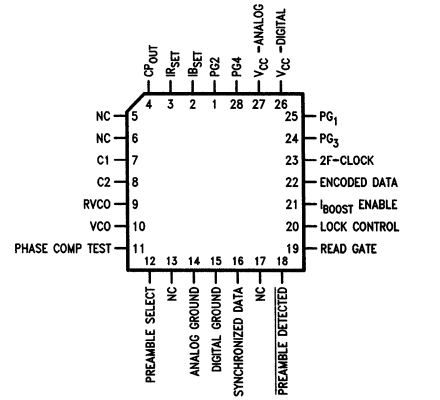
Top View

Order Number DP8462N
See NS Package Number N24C

Plastic Chip Carrier

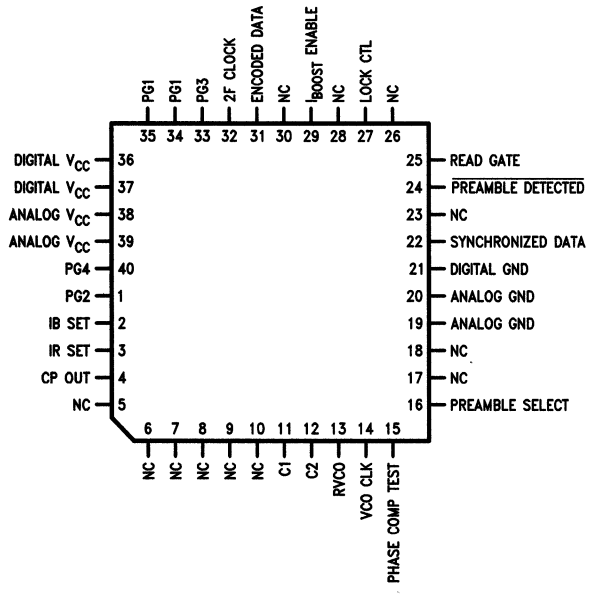


TL/F/8418-24

Order Number DP8462V
See NS Package Number V28A

Connection Diagrams (Continued)

TapePak®



TL/F/8418–25

Top View

Order Number DP8462TP
See NS Package Number TP40A

Pin Descriptions*

POWER SUPPLY

22,23 Digital and Analog V_{CC} = +5V ±5%
Should be tied together and bypassed by user.

11,12 Analog and Digital Ground
Should be tied together by user.

TTL Level Logic Inputs

15 READ GATE: When asserted, this signal sets the DP8462 into the Read Mode. The PLL then begins to lock onto the encoded data.

10 PREAMBLE SELECT: A high level on this input enables the circuit to recognize a 1-0-0-0 pattern while a low level results in the recognition of a 1-0-0 pattern. Also, in the non-read mode, if 1-0-0 is selected VCO/3 will lock onto 2F/3 while if 1-0-0-0 is selected VCO/4 will lock onto 2F/4.

16 LOCK CTL: This input allows the user to determine when the circuit will switch from Phase-Frequency comparison to Phase only comparison once in the Read Mode. A low level on this pin causes the circuit to switch from the phase-frequency comparison mode as soon as READ GATE is asserted while a high level means that the circuit will switch after 4 bytes of preamble have been detected and PREAMBLE DETECTED output has been asserted. (See the Truth Table at the end of this Section.)

17 IBOOST ENABLE: This input allows the user to control the PLL's track rate by turning Iboost current on and off. A high level at this input causes Iboost to be added to Irate—placing the PLL in the high track rate. In a typical system IBOOST ENABLE may be tied to READ GATE or PREAMBLE DETECTED.

18 ENCODED DATA: This input is for the incoming encoded data from the output of the head amplifier/pulse-detecting network located on the disk drive. Each positive edge of the ENCODED DATA waveform identifies a flux reversal on the disk.

19 2F-CLOCK: This is a system clock input, which is either a signal generated from the servo track, or a signal buffered from a crystal. It operates at twice the NRZ DATA rate. 2F-CLOCK MUST ALWAYS BE APPLIED TO THIS INPUT FOR PROPER OPERATION.

TTL Level Logic Outputs

8 VCO CLOCK: This is the output of the on-chip VCO, transmitted from an Advanced Schottky TTL buffer. It is synchronized to the SYNCHRONIZED DATA output so that it can be used by the encoder/decoder circuitry.

13 SYNCHRONIZED DATA: This is the same encoded data that is input to the chip, but is synchronous with the VCO CLOCK.

*Pin Number Designations apply for the 24 Pin DIP. See Connection Diagram for the Plastic Chip Carrier Pin Designations.

Pin Descriptions (Continued)

14 $\overline{\text{PREAMBLE DETECTED}}$: After READ GATE is asserted, this output goes low after detecting approximately 4 bytes of preamble and remains low until READ GATE goes inactive.

9 PHASE COMP TEST: This output is the logical "OR" of the Phase Comparator outputs, and may be used for the testing of the disk media.

Analog Signals

21,20 PG1, PG3: The external capacitors and resistor of the Pulse Gate filter are connected to these pins. PG1 should be tied directly to ground.

1 PG2: This is the Pulse Gate delay reference pin. The delay reference generator establishes a voltage at this pin; thereby producing the bias current for the Pulse Gate delay section in the resistor tied between this pin and V_{CC} for the DP8462-4 and in the current splitting network for the DP8462-3.

24 PG4: This is the Pulse Gate delay control pin. This pin can be tied to the PG2 pin if the user desires to adhere to the DP8462-4 standard synchronization window specification. For the DP8462-3 it should be tied to PG2 and V_{CC} through a "current splitting" network (see *Figure 6*) for optimal window positioning.

3 IRSET: The current into the rate set pin (Vbe/Rrate) is approximately half the charge pump output current for the low tracking rate.

2 IBSET: The current into the boost set pin (Vbe/Rboost) is approximately half the amount by which the charge pump current is increased for the high tracking rate.
(I_{hirate} = I_{rate} Set + I_{boost} Set).

4 CPOUT: This pin is the output node of the charge pump and also the noninverting input of the Buffer Amplifier. It is made available for connection of external filter components for the phase-locked-loop.

5,6 VCO C1, C2: An external capacitor connected across these pins sets the nominal frequency.

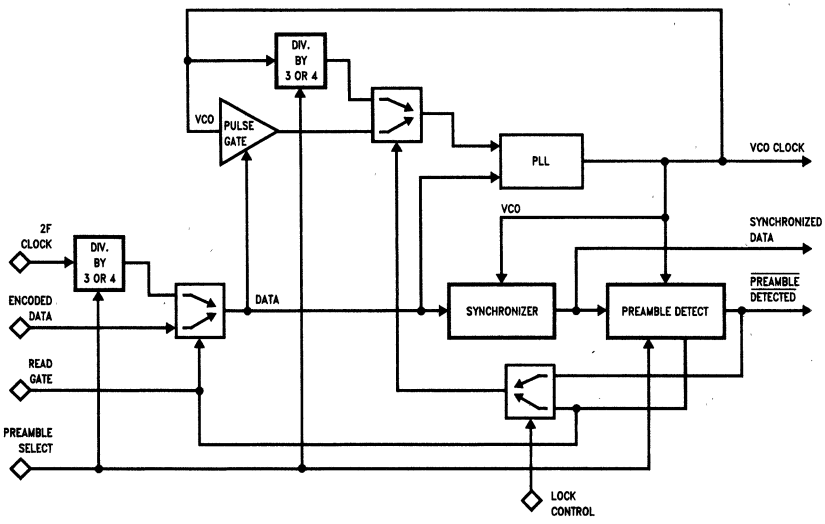
7 RVCO: The current into this pin determines the operating currents within the VCO.

Note: ANALOG and DIGITAL V_{CC} pins must be tied together by the user.
ANALOG and DIGITAL GND pins must also be tied together by the user.

Truth Table of Pulse-Gate's Modes

LOCK CTL (Pin 16)	READ GATE (Pin 15)	$\overline{\text{PREAMBLE DETECTED}}$ (Pin 14)	Pulse-Gate Comparison Mode	Comments
LO	LO	LO	N/A	N/A
LO	LO	HI	Phase and Frequency	Non-Read Mode
LO	HI	HI	Phase only	Read Mode
LO	HI	LO	Phase only	Read Mode
HI	LO	LO	N/A	N/A
HI	LO	HI	Phase and Frequency	Non-Read Mode
HI	HI	HI	Phase and Frequency	Read Mode
HI	HI	LO	Phase Only	Read Mode

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
TTL Inputs	7V
Output Voltages	7V
Input Current (CPOUT, IRSET, IBSET, RVCO)	2 mA
Storage Temperature	−65°C to +150°C
Operating Temperature Range	0°C to +70°C

ESD Rating is to be determined.

Operating Conditions

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage			4.75	5.00	5.25	V
T_A	Ambient Temperature			0	25	70	°C
I_{OH}	High Logic Level Output Current		V_{CO} Clock Others			−2000 −400	μA
I_{OL}	Low Logic Level Output Current		V_{CO} Clock Others			20 8	mA
f_{DATA}	Input Data Rate			4.0		20	Mbit/sec
t_{WCK}	Width of 2f-CLOCK, High or Low			10			ns
t_{WPD}	Width of ENCODED DATA Pulse (Note 1)	High		18			ns
		Low		0.4t			ns
V_{IH}	High Logic Level Input Voltage			2			V
V_{IL}	Low Logic Level Input Voltage					0.8	V
t_{SU} Read Gate	Min Time Required for a Positive Edge of Read Gate to Occur Before a Negative Edge of VCO			20			ns
t_{HOLD} Read Gate	Min Time Required for a High Level on Read Gate to be Held After a Negative Edge of VCO			10			ns

Note 1: t is defined as the period of the NRZ data ($t = 2/F_{VCO}$).

DC Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	V_{CC} −2V	V_{CC} −1.6V		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−200	μA
I_O	Output Drive Current (Note 1)	V_{CC} = Max, V_O = 2.125V	−12		−110	mA
I_{CC}	Supply Current	V_{CC} = Max			85	mA
I_{OUT}	Charge Pump Output Current	$200 \le I_{RATE} + I_{BOOST} \le 2000$	$0.9\ I_{TYP} - 25$	$2.0\ (I_{RATE} + I_{BOOST})$	$1.1\ I_{TYP} + 25$	μA

Note 1: This value has been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

AC Electrical Characteristics Over Recommended V_{CC} and Operating Temperature Range

(All Parts unless stated otherwise) ($t_R = t_F = 2.0$ ns, $V_{IH} = 3.0V$, $V_{IL} = 0V$) (Note 1)

Symbol	Parameter	Min	Typ	Max	Units
t_{READ}	Positive VCO CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE high)		1	1	—
$t_{TRANSMIT}$	Positive VCO CLOCK transitions required to transmit input encoded data to output	1	2	3	—
$t_{READ\ ABORT}$	Number of VCO CLOCK cycles after READ GATE set low to read operation abort (Note 3)			2	T-clock
t_{WINDOW}	Variance of center of decode window from nominal (Note 6) DP8462-3 / DP8462-4			6 / 10	ns
ϕLINEARITY	Phase range for charge pump output linearity (Note 2)	$-\pi$		$+\pi$	Radians
K_1	Phase comparator—Charge Pump gain constant ($N = f_{VCO}/f$ input data) (Note 4)		$\frac{1.78\ V_{BE}}{N2\pi R}$		Amps/rad
$V_{CONTROL}$	Charge pump output voltage swing from nominal		± 100		mV
K_{VCO} ($= A \times K_2$)	VCO gain constant (ω_{VCO} = VCO center frequency in rad/s) (Note 5)	$\frac{1.20\ \omega_C}{V_{BE}}$	$\frac{1.40\ \omega_C}{V_{BE}}$	$\frac{1.60\ \omega_C}{V_{BE}}$	rad/sec V
f_{VCO}	VCO center frequency variation over temperature and V_{CC}	-2		$+2$	%
$f_{MAX\ VCO}$	VCO maximum frequency		60		MHz
t_{PHL}	Propagation delay from VCO negative edge to synchronous DATA negative edge	2		18	ns
t_{PLH}	Propagation delay from VCO negative edge to synchronous DATA positive edge	4		20	ns

Note 1: A sample calculation of frequency variation vs. control voltage: $V_{IN} = \pm 0.1V$;

$$K_{VCO} = \frac{\omega OUT}{V_{IN}} = \frac{0.4\ \omega_C}{0.2V} = \frac{2.0\ \omega_C\ (rad/sec)}{V\ \ (volt)}.$$

Note 2: $-\pi$ to $+\pi$ with respect to 2f VCO CLOCK.

Note 3: T-clock is defined as the time required for one period of the VCO CLOCK to occur.

Note 4: With respect to VCO CLOCK; $I_{PUMP\ OUT} = 1.9\ I_{SET}$

$$I_{SET} = \frac{V_{BE}}{R_{SET}}$$

Note 5: Although specified as the VCO gain constant, this is the gain from the Buffer Amplifier input to the VCO output.

Note 6: This specification is guaranteed only for the conditions under which the parts were tested. However, significant variation from formula is not expected for other data rates and filters. The DP8462-4 specification is for the condition when PG2 and PG4 are tied together. The DP8462-3 specification is for the condition when a 330Ω resistor is tied from PG2 to PG4 and a 1.5 kΩ resistor is tied from PG4 to V_{CC}. External adjustment can be used to optimize the window as described in the pulse gate section. The filter values below were chosen for operation in an automatic test system (static window) environment. Different criteria may apply for choosing filter values in a disk system. See Loop Filter Section for sample calculations of other filter values.

Part Type	Data Rate Tested	Filter				
		C_1	C_2	R_1	R_{RATE}	R_{BOOST}
DP8462-4	5 Mbit/sec	0.03 μF	600 pF	100Ω	820Ω	1.5 kΩ
DP8462-3	10 Mbit/sec	0.022 μF	510 pF	81Ω	800Ω	1.8 kΩ

Note: For further informtion refer to Application Note AN-414

External Component Selection (All Parts) (Note 1)

Symbol	Component	Min	Typ	Max	Units
R_{VCO}	VCO Frequency Setting Resistor (Note 2)	990		1010	Ω
C_{VCO}	VCO Frequency Setting Capacitor (Notes 3,4)	20		120	pF
R_{RATE}	Charge Pump I_{RATE} Set Resistor (Note 6)	0.4		4.0	kΩ
R_{BOOST}	Charge Pump (High Rate) I_{BOOST} Resistor (Note 6)	0.5		∞	kΩ
C_R	I_{RATE} Bypass Capacitor (Note 5)	0.01			μF
C_B	I_{BOOST} Bypass Capacitor (Note 5)	0.01			μF

Note 1: External component values for the Loop Filter and Pulse Gate are given in Table II and Table I respectively.

Note 2: A 1% Component Tolerance is Required.

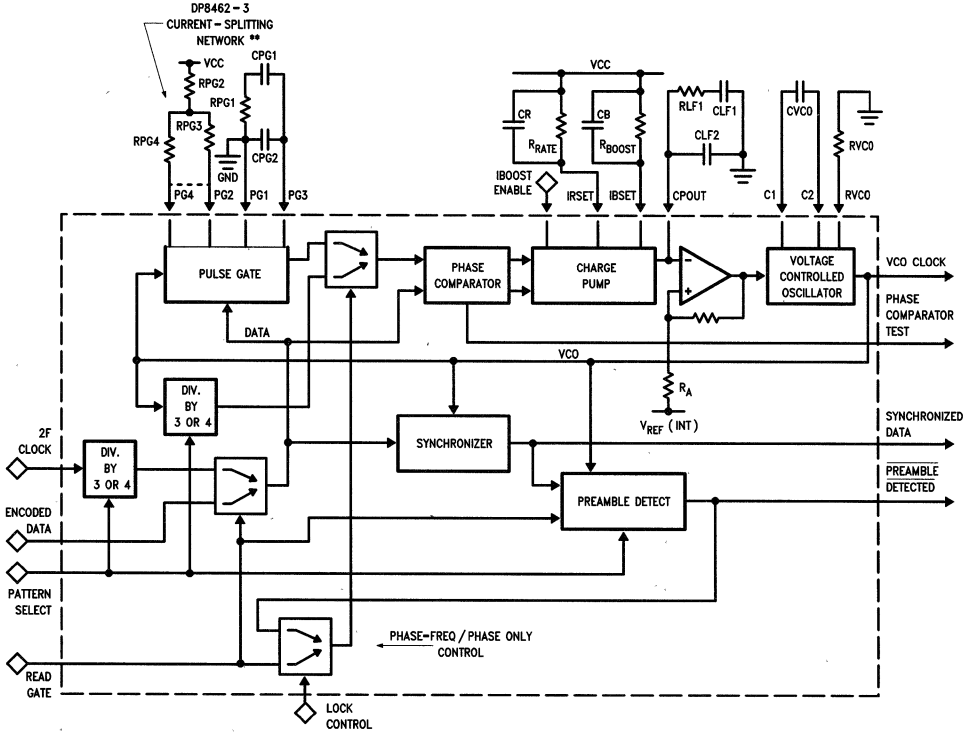
Note 3: These MIN and MAX values correspond to the MAX and MIN data rates respectively.

Note 4: The Component Tolerance is system dependent on how much center frequency deviation can be tolerated.

Note 5: Component Tolerance 15%.

Note 6: The minimum value of the parallel combination of R_{RATE} and R_{BOOST} is 350Ω.

Detailed Block Diagram



TL/F/8418–3

**For DP8462-4 window testing, RPG3 = RPG4 = 0Ω and RPG2 = 4.7 kΩ. For DP8462-3 window testing RPG4 = 0Ω, RPG3 = 330Ω and RPG2 = 1.5 kΩ.

Circuit Operation

In the non-read mode, the DP8462 Data Separator remains locked to the 2f CLOCK signal divided by 3 or 4 (depending upon the preamble used) in anticipation of a preamble when read mode is entered. When the READ GATE input goes high, the DP8462 enters the read mode after 1 VCO CLOCK cycle. Referring to *Figure 1*, once in the read mode, the PLL reference signal is switched from the 2f-divided-by-3-or-4 signal to the ENCODED DATA input. The PLL is at this point in the high-tracking rate mode and also in the Phase and Frequency Comparison mode. The PLL then attempts to

Circuit Operation (Continued)

quickly lock onto the incoming ENCODED DATA stream and starts looking for 16 consecutive preamble pulses—chosen by the user to be either 100 (PATTERN SELECT: LO) or 1000 (PATTERN SELECT: HI). If the user has chosen to switch to Phase Only Comparison as soon as read operation begins (LOCK CTL: LO), then the Phase Comparator will start to compare ENCODED DATA with VCO-gated-by-DATA immediately (see *Figure 2*); otherwise, it will keep comparing ENCODED DATA with VCO divided by 3 or 4—i.e., remain in Phase and Frequency Comparison mode until after 16 consecutive preamble pulses have been detected. At this time, $\overline{\text{PREAMBLE DETECTED}}$ output goes low and the circuit now starts to compare ENCODED DATA with VCO-gated-by-DATA (see *Figure 1*).

The user is given control over when to switch the charge-pump current rate through the use of the IBOOST ENABLE input. One way the user can accomplish this is by tying $\overline{\text{PREAMBLE DETECTED}}$ output to the IBOOST ENABLE input directly. Thus, once $\overline{\text{PREAMBLE DETECTED}}$ is asserted, the circuit will go into low track rate and Phase Only Comparison mode (if LOCK CTL: HI) so that a more stable lock can be retained. The incoming ENCODED DATA stream is now synchronized with the VCO CLOCK and appears at the SYNCHRONIZED DATA output (see *Figure 3*). (If the user wishes to switch to low track rate as soon as the circuit enters the read mode, then the READ GATE signal should be inverted and applied to the IBOOST ENABLE input).

Figure 4 shows the sequence when READ GATE goes low, signifying the end of a read operation. The PLL reference signal is switched back to 2f divided by 3 or 4 input and the $\overline{\text{PREAMBLE DETECTED}}$ output goes high (causing the charge-pump to go to the high tracking rate, if $\overline{\text{PREAMBLE DETECTED}}$ is tied to the IBOOST ENABLE input). Also, the Phase Comparator goes back to Phase and Frequency Comparison mode and the circuit attempts to lock onto the 2f divided by 3 or 4 signal, thus returning to the initial conditions.

CIRCUIT DESCRIPTION

1. Divide by 3 or 4: Depending on the preamble pattern being used, these circuits divide 2f CLOCK and internal VCO CLOCK signals by 3 or 4. During the non-read mode, the VCO remains phase and frequency locked to these divided signals so that when read mode is entered, the PLL can quickly acquire lock because the data stream that consists of the preamble pattern is very close in frequency to the VCO divided by 3 or 4.

2. Pulse Gate: Once in the read mode, the PLL has to lock the VCO CLOCK to the ENCODED DATA stream; outside of the preamble, however, the data signal is not cyclic like the VCO CLOCK and therefore cannot be frequency compared to the VCO. It is for this reason that the Pulse Gate is used to allow a reference signal from the VCO into the Phase Comparator only when an ENCODED DATA bit is valid. The Pulse Gate also utilizes a scheme which delays the incoming data by one-half the period of the 2f-CLOCK. This optimizes the position of the decode window and allows input jitter up to ± half the 2f-CLOCK period, assuming no error in the decode window position. The decode window error can be determined from the specification in the Electrical Characteristics Table.

3. Multiplexers at the Phase Comparator's inputs: These multiplexers are used to determine which signals the Phase Comparator will compare during different modes of operation. Either 2F divided by 3 or 4 or ENCODED DATA is compared with either VCO divided by 3 or 4 (Phase and Frequency Lock) or with VCO gated by DATA (Phase Only Lock).

4. Phase Comparator: The Phase Comparator receives its inputs from the Multiplexers mentioned above, and is edge-triggered from these inputs to provide charge-up and charge-down outputs.

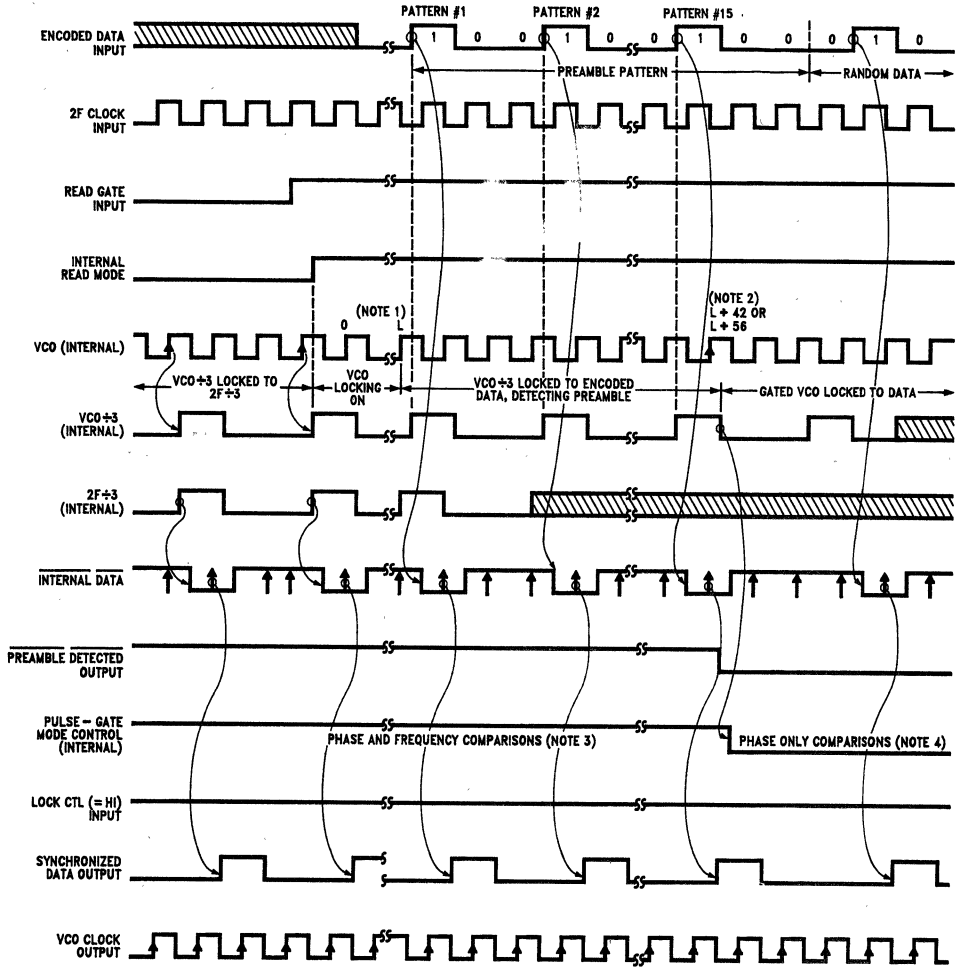
5. Charge Pump: The high speed charge pump consists of a switchable constant current source and sink. The charge pump constant current is set by connecting external resistors to V_{CC} from IRSET and IBSET pins. With IBOOST ENABLE HIGH, the PLL is in the high tracking rate and both resistors determine the current. With IBOOST ENABLE LOW, the PLL is in the low tracking rate and only the IRSET resistor determines the charge pump current. The output of the charge pump feeds into external filter components and the Buffer Amplifier. Thus, through the use of the IBOOST ENABLE pin, the user can determine when the circuit switches track rates.

6. Buffer Amplifier: The Buffer Amplifier is configured as a high input impedance amplifier which is inserted between the charge pump and the VCO, thus allowing connection of external PLL filter components to the charge pump output pin CPOUT. The output of the Buffer Amplifier is internally connected to the VCO control input.

7. VCO: The Voltage-Controlled-Oscillator requires a resistor from the RVCO pin to ground and a capacitor between pins C1 and C2, to set the center frequency. The VCO frequency can be varied from nominal by approximately ±20%, as determined by its control input voltage (CPOUT).

8. Preamble Pattern Detector: Two types of preamble patterns are commonly used in RLL 2,7 code disk systems—1-0-0 and 1-0-0-0. The user selects the preamble pattern to be used by setting PREAMBLE SELECT input either HI for the 1-0-0-0 pattern or LO for the 1-0-0 pattern. The DP8462 divides 2F Clock and VCO Clock signals by 3 or 4 depending upon whether 1-0-0 or 1-0-0-0 pattern is selected, respectively, and remains locked to this divided pattern in anticipation of a preamble. Once the chip is in the read mode, the VCO proceeds to lock onto the incoming data stream. The Preamble Pattern Detector then searches for 16 consecutive patterns (i.e., 100100100... or 100010001000...) to indicate lock has been achieved. The $\overline{\text{PREAMBLE DETECTED}}$ output then goes low. Any deviation from the above-mentioned continuous stream of patterns before 16 of these are detected will reset the Pattern Detector and the procedure will then start over again.

Circuit Operations (Continued)



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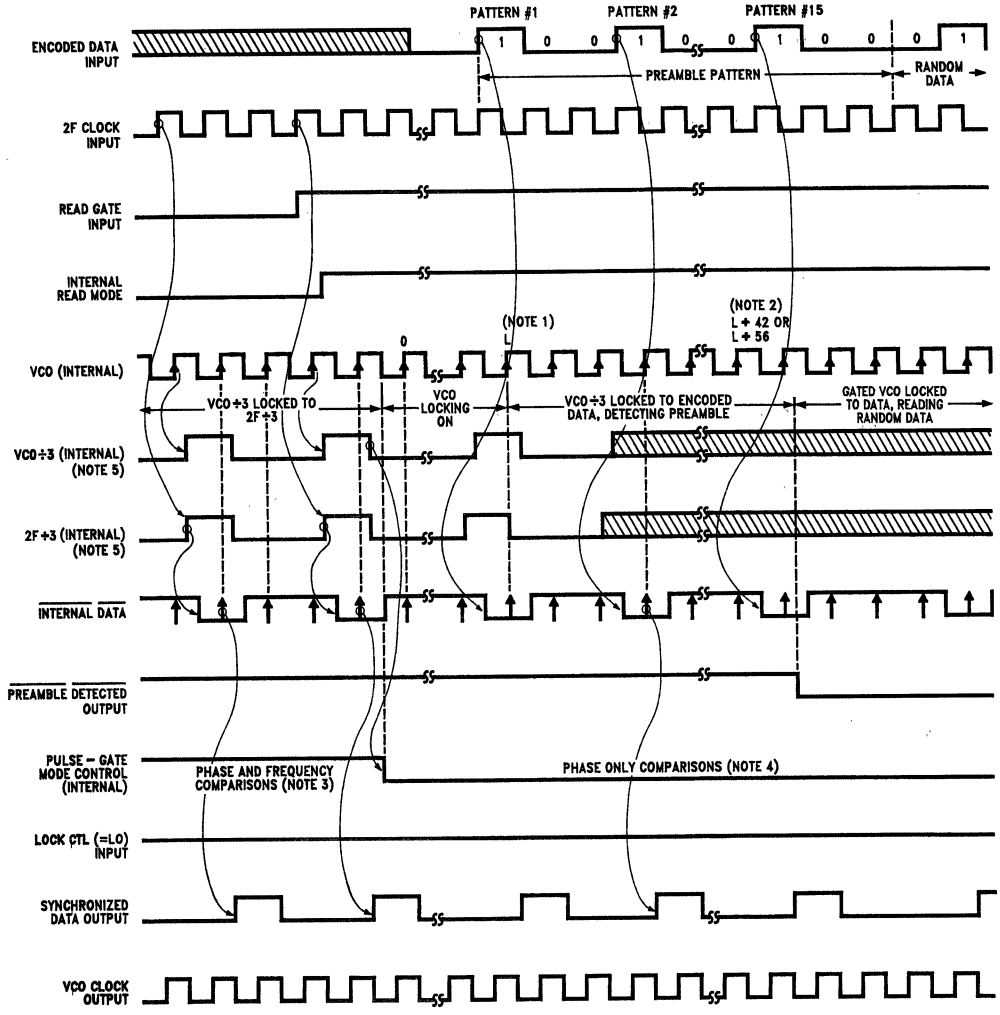
Note 1: L = Number of VCO cycles required for VCO to lock—typically 20 but determined by external component value.
Note 2: At L + 42 (Pattern = 1-0-0) or L + 56 (Pattern = 1-0-0-0), 15 patterns have been detected.
Note 3: VCO ÷3 (or 4) being compared with 2F ÷3 (or 4) in the non-read mode and Preamble in the Read Mode.
Note 4: VCO GATED BY DATA being compared with ENCODED DATA.
Note 5: PREAMBLE SELECT = LO; 100 pattern selected—so 2F & VCO are being divided by 3.

FIGURE 1. Lock-On Sequence Waveform Diagram—Pulse Gate Mode Switches after Preamble Detection

Circuit Operation (Continued)

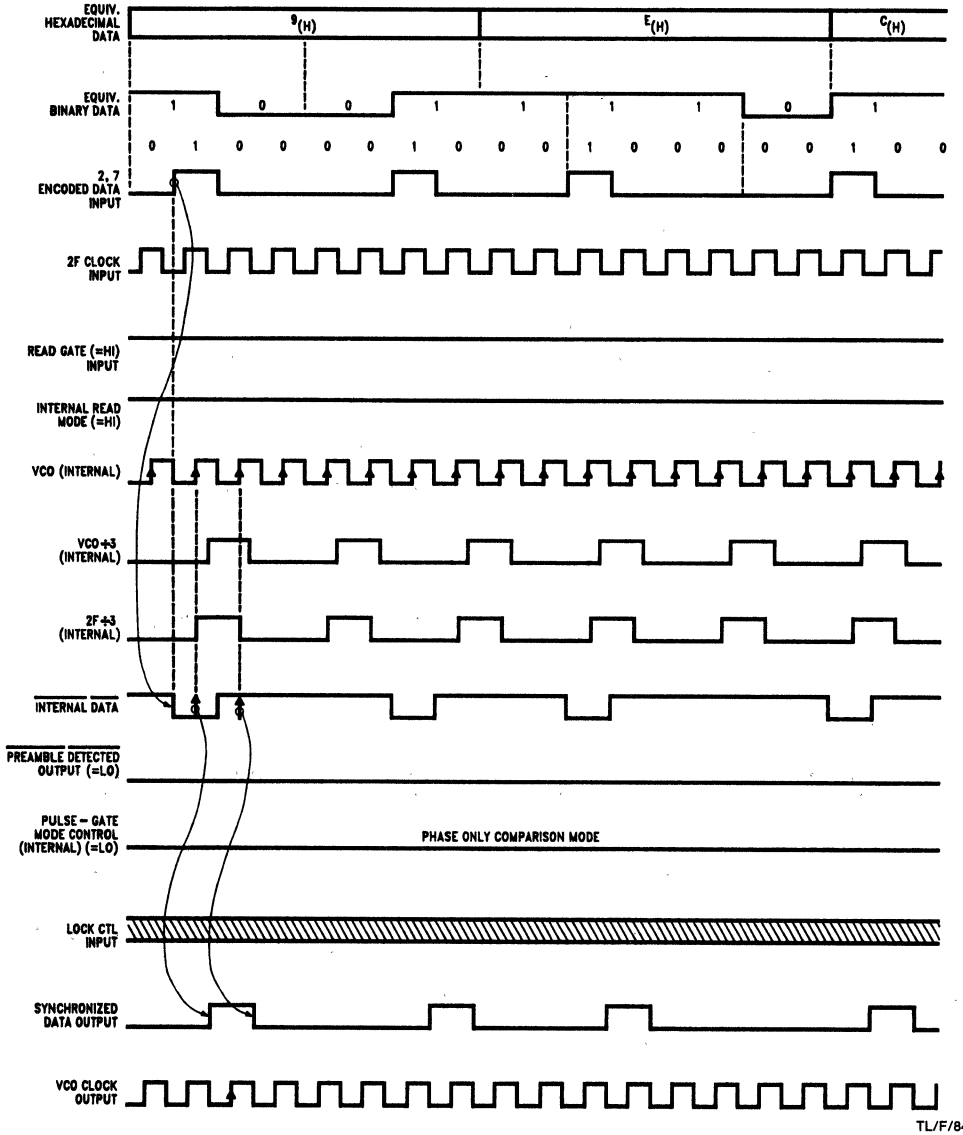


TL/F/8418–5

Note 1: L = Number of VCO cycles required for VCO to lock—typically 20 but determined by external component value.
Note 2: At L + 42 (Pattern = 1-0-0) or L + 56 (Pattern = 1-0-0-0), 15 patterns have been detected.
Note 3: VCO ÷ 3 (or 4) being compared with 2F ÷ 3 (or 4) in the non-read mode.
Note 4: VCO gated by DATA being compared with ENCODED DATA.
Note 5: PREAMBLE SELECT = LO; 1-0-0 pattern selected—so 2F & VCO are being divided by 3.

FIGURE 2. Lock-On Sequence Waveform Diagram—Pulse Gate Mode Switches Immediately After READ GATE is Asserted

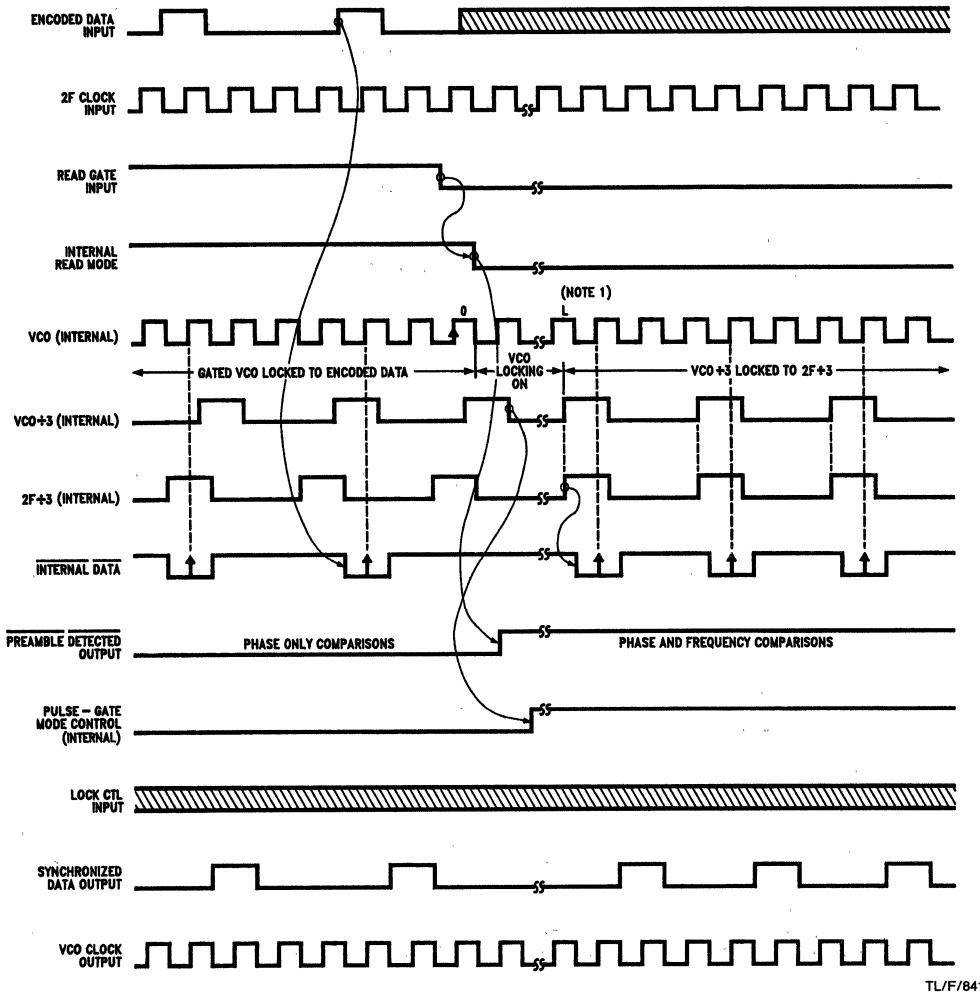
Circuit Operation (Continued)



TL/F/8418–6

FIGURE 3. Locked-On Waveform Diagram

Circuit Operation (Continued)



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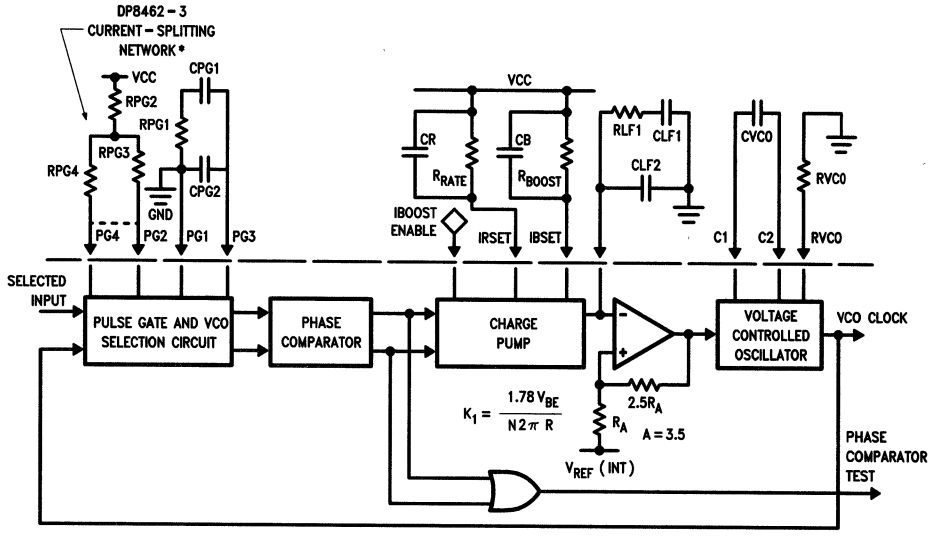
Note 1: L indicates the number of cycles required for the VCO to lock to the 2f-Clock.

Note 2: PREAMBLE SELECT = LO; 1-0-0 Pattern selected—so 2F & VCO being divided by 3.

FIGURE 4. Lock-Ending Sequence Waveform Diagram

Circuit Operation (Continued)



TL/F/8418–8

For DP8462-4 window testing RPG4 = RPG3 = 0Ω and RPG2 = 4.7 kΩ. For DP8462-3 window testing RPG4 = 0Ω, RPG3 = 330Ω and RPG2 = 1.5 kΩ.

FIGURE 5. Phase-Locked-Loop Section

BIT JITTER TOLERANCE

The two options of the DP8462, the -4 and -3 offer decreasing window errors (respectively) so that the parts may be selected for different data rates (up to 20 Mbit/sec). The -4 part will be used in most low data rate applications. As an example, at the 5 Mbit/sec data rate of most 5¼ inch drives, T = 200 ns so that from the Electrical Characteristics Table, t_{WINDOW} = 10 ns. The chip therefore contributes up to 10 ns of window error, out of the total allowable error of 50 ns (half the 2f-clock period of 100 ns). This allows the disk drive to have a margin of 40 ns of jitter on the transition position before an error will occur. The bit jitter tolerance can be improved by adjusting the window center using PG2 and PG4. A current splitting network consisting of RPG3 and RPG4 can be used to adjust the delay line. This adjustment is internally compensated for V_{CC} and temperature variation.

ANALOG CONNECTIONS TO THE DP8462

External passive components are required for the Pulse Gate, Charge Pump, Loop Filter and VCO as shown in *Figure 5*. The information provided here is for guidelines only. The user should select values according to his own system requirements. Phase-Locked Loops are complex circuits that require detailed knowledge of the specific system. Factors such as loop gain, stability, response to change of signal, lock-on time, etc. are all determined by the external components. In many disk systems these factors are critical, and National Semiconductor recommends the designer be knowledgeable of phase-locked-loops, or seek the advice of an expert. Inaccurate design will probably result in excessive disk error rates. The phase-locked-loop in the DP8462 has many advantages over all but the most sophisticated discrete designs, and if the component values are selected correctly, it will offer significant performance advantages. This should result in a reduction of disk error rates over equivalent discrete designs.

PULSE GATE

There are 6 external components connected to the Pulse Gate as shown in *Figure 6* with the associated internal components. Of these, RPG3 and RPG4 are optional and may be omitted if adjustment of the delay line is not desired. The values of RPG1, RPG2, RPG3, RPG4, CPG1, and CPG2 are dependent on the data rate. RPG1 and RPG2 are inversely proportional to the data rate, while CPG1 and CPG2 are proportional. Table I shows component values for the data rates given. Component values are calculated by selecting RPG2′ from Table I [RPG2′ = RPG2 + (RPG3//RPG4)]. If RPG4 = 0Ω, RPG2′ = RPG3 + RPG2. Next calculate

$$CPG1 = \left(\frac{2.12 \times 10^5}{890 + RPG2'}\right)\left(\frac{1}{100 \times Rs}\right)^2$$

$$CPG2 = \frac{1}{10} CPG1, \text{ and}$$

$$RPG1 = \left(\frac{890 + RPG2'}{2.38 \times 10^5}\right)(100 \times Rs).$$

In the above equation Rs is the rotational speed and, for 3600 RPM, Rs = 60 Hz. A rotational speed of 3600 RPM was assumed for the calculations in Table I. For data rates not listed, RPG2 may be approximated as (30 kΩ/fDATA) − 1.2 kΩ = RPG2 where fDATA is the data rate in Megabits per second. RPG3 and RPG4, in conjuction with RPG2, form a "current-splitting-network" that can be used to adjust the delay line; thus adjusting the decode window early or late. RPG2 should be made large with respect to RPG3 and RPG4 and a potentiometer can be used for RPG4—with its value centered around that of RPG3. For example, at Data Rate = 5 Mbits/sec., Table I dictates that RPG2′ should be 4.7k. If the delay line is to be made adjustable, then one could pick RPG2 = 4.3k and RPG3 = 800Ω. Now, using a 1.6 kΩ potentiometer for RPG4, RPG4 = 800Ω would give RPG2′ = 4.7 kΩ and would provide standard window synchronization; varying RPG4 high or low, however, would

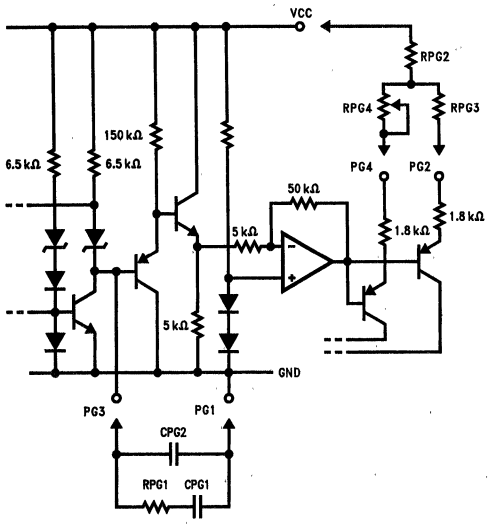
Circuit Operation (Continued)

shift the window late or early, respectively. If no adjustment is desired, then PG2 and PG4 should be tied together and only RPG2 should be used. Components with 5% tolerance will suffice.

TABLE I. Pulse Gate Component Selection Chart

Data Rate	RPG2'	RPG1	CPG1	CPG2
5 Mbit/sec	4.7 kΩ	150Ω	1 μF	0.1 μF
10 Mbit/sec	1.8 kΩ	68Ω	2.2 μF	0.22 μF
15 Mbit/sec	750Ω	39Ω	3.9 μF	0.39 μF

Where [RPG2' = RPG2 + RPG3//RPG4]



TL/F/8418–9

FIGURE 6. Pulse-Gate Controls

CHARGE PUMP

Resistors R_{RATE} and R_{BOOST} determine the charge pump current. The Charge Pump bidirectional output current is related to the input current according to the relationship specified in the DC Electrical Characteristics Table. In the high tracking rate with IBOOST ENABLE high, the input current is $I_{BSET} + I_{RSET}$, i.e., the sum of the currents through R_{BOOST} and R_{RATE} from V_{CC}. In the low tracking rate, with IBOOST ENABLE low, this input current is I_{RSET} only.

A recommended approach would be to select R_{RATE} first. The External Component Limits table allows R_{RATE} to be 0.4 kΩ to 4.0 kΩ, so for simplicity select R_{RATE} = 820Ω. A typical loop gain change of 2:1 for high to low tracking rate would require $R_{BOOST} = R_{RATE}$ or 820Ω. Referring to *Figure 7* the input current is effectively V_{BE}/R_{RATE} in the low tracking rate, where V_{BE} is an internal voltage. This means that the current into or out of the loop filter is approximately 2.0 V_{BE}/R_{RATE}, or in this example approximately 1.8 mA. Note that although it would seem the overall gain is dependent on V_{BE}, this is not the case. The VCO gain is altered internally by an amount inversely proportional to V_{BE}, as detailed in the section on the Loop Filter. This means that as V_{BE} varies with temperature or device spread, the gain will remain constant for a particular fixed set of values of R_{RATE} and R_{BOOST}. This alleviates the need for potentiometers to select values for each device. The tolerance required for these two resistors will depend on the total loop gain tolerance allowed, but 5% would be typical. Also V_{CC} by-pass capacitors are required for these two resistors. A value of 0.01 μF is suitable for each.

VCO

The value of R_{VCO} is fixed at 1 kΩ ± 1% in the External Component Limits table. *Figure 8* shows how R_{VCO} is connected to the internal components of the chip. This value was fixed at 1 kΩ to set the VCO operating current such that optimum performance of the VCO is obtained for production device spreads. This means fixed value components will be adequate to set the VCO center frequency for production runs. The value of C_{VCO} can therefore be determined from the VCO frequency f_{VCO}, using the equation: $C_{VCO} = [1/(R_{VCO})(f_{VCO})] - 5$ pF where f_{VCO} is twice the input data rate. As an example, for a 5 Mbit/sec data rate, f_{VCO} = 10 MHz, requiring that C_{VCO} = 95 pF. This does not take into account any lead capacitance on the printed circuit board; the user must account for this. The amount of tolerance a particular design can afford on the center frequency will determine the capacitor tolerance. The capacitor is connected to the internal circuitry of the chip as shown in *Figure 9*.

As the data rate increases and C_{VCO} gets smaller, the effects of unwanted parasitic capacitances influence the fre-

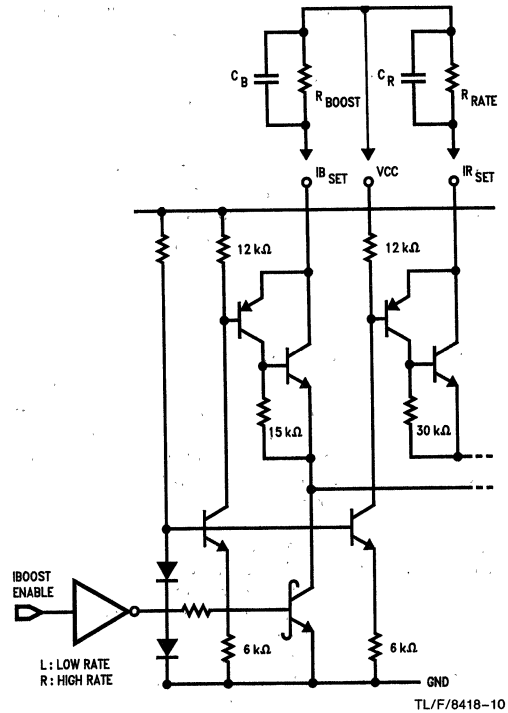


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FIGURE 7. I_{RATE} Set and I_{BOOST} Set

Circuit Operation (Continued)

quency. As a guide the graph of *Figure 10* shows approximately the value of C_{VCO} for a given data rate.

The VCO center frequency may be determined by: 1) holding pin 4 at ground potential and measuring the VCO frequency (−20% value); 2) holding pin 4 at approximately 3 volts and measuring the VCO frequency (+20% value); 3) averaging the two measured frequencies for the equivalent center frequency.

LOOP FILTER

The input current into the Buffer Amplifier is offset by a matched current out of the Charge Pump, and even so is much less than the switching current in or out of the Charge Pump. It can therefore be assumed that all the Charge Pump switching current goes into the Loop Filter components R_1 and C_1 and C_2. The tolerance of these compo-

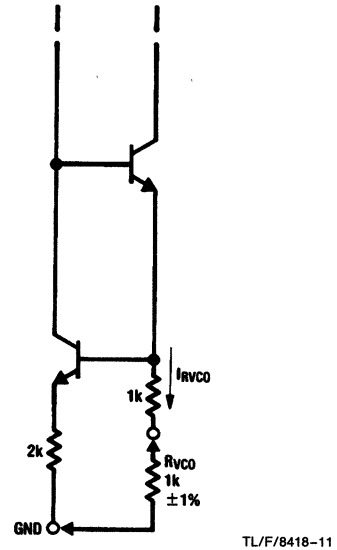

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FIGURE 8. VCO Current Setting Resistor

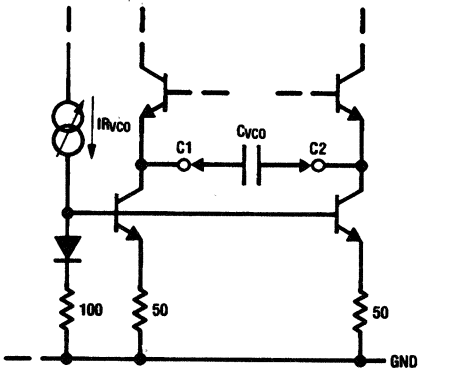

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FIGURE 9. VCO Capacitor

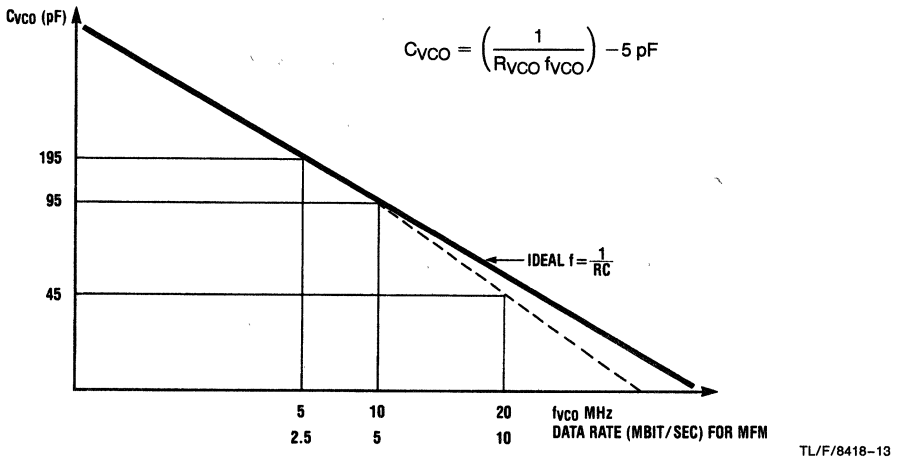

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FIGURE 10. VCO Capacitor Value for Disk Data Rates

Circuit Operation (Continued)

nents should be the same as R_{RATE} and R_{BOOST}, and will determine the overall loop gain variation. The three components connected to the Charge Pump output are shown in *Figure 11*. Note the return current goes to analog GND, which should be electrically very close to the GND pin itself.

The value of capacitor C_1 determines loop bandwidth—the larger the value the longer the loop takes to respond to an input change. If C_1 is too small, the loop will track any jitter on the ENCODED DATA input and the VCO output will follow this jitter, which is undesirable. The value of C_1 should therefore be large enough so that the PLL is fairly immune to phase jitter but not large enough that the loop won't respond to longer term data rate changes that occur on the disk drive.

The damping resistor R_1 is required to damp any oscillation on the VCO input that would otherwise occur due to step function changes on the input. A value of R_1 that would give a phase margin of around 45 degrees would be a reasonable starting point.

The main function of the capacitor C_2 is to "smooth" the VCO input voltage. Typically its value will be less than one tenth of C_1.

Figure 12 shows the relevant phase-locked-loop blocks that determine system response, namely the Phase Detector, Filter/Buffer Amplifier, and VCO. The Phase Detector (Phase Comparator and Charge Pump) produces an aggregate output current i which is proportional to the phase difference between the input signal and the VCO signal. The constant (K_1) is $\frac{1.78\ V_{BE}}{2\pi RN}$ amps per radian where $N = \frac{f_{VCO}}{f_{DATA}}$. R is either R_{RATE} or $R_{RATE} \parallel R_{BOOST}$. This aggregate current feeds into or out of the filter impedance (Z), producing a voltage to the VCO that regulates the VCO frequency. The VCO gain constant is 0.4 ω_{VCO}/V_{BE} radians per second per volt. Under steady state conditions, i will be zero and there will be no phase difference between the input signal and the VCO. Any change of input signal will produce a change in VCO frequency that is determined by the loop gain equation. This equation is determined from the gain constants K_1, A and K_2 and the filter v/i response.

The impedance Z of the filter is:

$$\frac{1}{sC_2} \parallel \left(\frac{1}{sC_1} + R_1\right) = \frac{1 + sC_1R_1}{sC_1\left(1 + \frac{C_2}{C_1} + sC_2R_1\right)}$$

If $C_2 < C_1$ then the impedance Z approximates to:

$$\frac{1 + sC_1R_1}{sC_1\,(1 + sC_2R_1)}$$

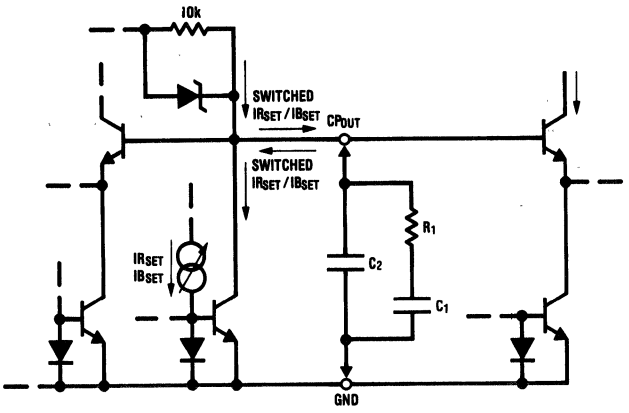

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FIGURE 11. Charge Pump Out

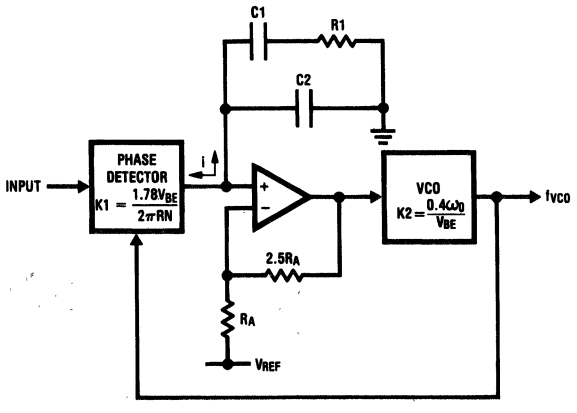

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FIGURE 12. Loop Response Components

Circuit Operation (Continued)

The overall loop gain is then

$$G(s) = \frac{K_1 A K_2}{s} \times \frac{1 + sC_1R_1}{sC_1(1 + sC_2R_1)}$$

Let $G_{(K)} = K_1 A K_2$

$$F(s) = \frac{1 + SC_1R_1}{SC_1(1 + SC_2R_1)}$$

The Overall Closed Loop Gain is:

$$\frac{\phi OUT}{\phi IN} = \frac{G_{(K)} F(s)}{s + G_{(K)} F(s)}$$

Substituting, We Get

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{G_{(K)}(SC_1R_1 + 1)}{S^3 R_1 C_1 C_2 + S^2 C_1 + GK(SC_1R_1 + 1)}$$

$$= \frac{(G_{(K)}/C_1)(SR_1C_1 + 1)}{S^3 R_1C_2 + S^2 + SG_{(K)}R_1 + G_{(K)}/C_1}$$

If $C_2 \ll C_1$, we can ignore the 3rd Order Component introduced by C_2 then:

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{(G_{(K)}/C_1)(SR_1C_1 + 1)}{S^2 + SG_{(K)}R_1 + G_{(K)}/C_1}$$

This is a second Order Loop and can be solved as follows:

$$S^2 + SG_{(K)}R_1 + G_{(K)}/C_1 = S^2 + 2\zeta\omega_n S + \omega_n^2$$

$$\therefore C_1 = \frac{G_{(K)}}{\omega_n^2}$$

$$R_1 = \frac{2\zeta\omega_n}{G_{(K)}}$$

From the above equations:

$$\omega = (G(K)/C1)^{1/2}$$

$$G(K) = K1 \times A \times K2 =$$

$$[(0.89 \times V_{BE})/(2 \times Pi \times R)] \times [(0.4 \times W_{VCO})/V_{BE}] \times [3.5]$$

2,7 coded data has a 2.67 to 1.0 frequency range within the data field. The expression $K = (0.89 \times V_{BE}/2 \times Pi \times R)$ is valid when the VCO frequency is twice the ENCODED DATA frequency. In order to make this equation more general, it may be written as follows: $K = (1.78 \times V_{BE})/(2 \times Pi \times R \times N)$ where N is defined as the VCO frequency divided by the encoded data pulse frequency, or $N = F_{VCO}/F_{DATA}$ ($N = 3$ for maximum data rate and $N = 8$ for minimum data rate). Now G(K) can be written as follows:

$$G(K) = [(1.78 \times V_{BE})/(2 \times Pi \times R \times N)] \times [(0.4 \times \omega_{VCO})/V_{BE}] \times [3.5]$$

$$= (2.5 \times F_{VCO})/(R \times N)$$

$$\omega n = [(2.5 \times F_{VCO})/(C1 \times R \times N)]^{1/2}$$

where,

$R = R_{RATE}$ in the low track rate;

$R = (R_{RATE}//R_{BOOST})$ in the high track rate.

From the above equations:

$$\omega_N = (R1 \times G(K))/(2\zeta)$$

$$G(K) = C1 \times (\omega_N^2)$$

$$\zeta = \text{(damping factor)} = (R1 \times \omega_N \times C1)/2$$

The damping factor should be approximately 0.5 when ω_N is minimum. Response to bit shift is minimized when the damping factor is small; however, if the damping factor drops much below 0.5, the system tends to be oscillatory (underdamped). Additionally, loop performance is poor (excessive phase-acquisition times) if the damping factor becomes much larger than 1.0. Any increase in loop bandwidth (due to R decreasing in the high track rate) produces a proportional increase in the damping factor, and should be limited to the point where the maximum damping factor is 1.0. With the damping factor range established, loop design can proceed.

From the Disk Interface Design Guide And User's Manual Chapter 1, Section 1.3–1.7, it is shown that a 946 krads/sec loop bandwidth during acquisition results in a 7 byte crystal reference clock acquisition and data frequency acquisition (VCO settled to within 2 ns of window center). We recommend that these design guide sections be reviewed in conjunction with the DP8462 data sheet in order to obtain a more detailed explanation of the loop bandwidth selection used here, as well as for disk system PLLs in general.

This design example is for a 10 MBit/sec data rate and assumes that the IBOOST ENABLE pin is tied to the $\overline{\text{PREAMBLE DETECTED}}$ pin. This results in the track rate being switched from high to low after four bytes of preamble are detected. As an alternative, the IBOOST ENABLE pin may be tied to an inverted READ GATE signal, resulting in the track rate switching immediately to low when READ GATE is asserted. This is discussed further in the Design Guide.

We will assume a 1-0-0-0 . . . preamble. During acquisition we are in the high track rate and thus ω_N is at maximum value. In the read mode the highest frequency pattern we can encounter is 1-0-0 . . . ; however, ω_N will be lower since we will be in the low track rate.

$$\omega_N = [(2.5 \times F_{VCO})/(C1 \times R \times N)]^{1/2}$$

Choose $R_P = R_{RATE} // R_{BOOST} = 575\Omega$*

$$946 \times 10^3 = [(2.5 \times 20 \times 10^6)/(C1 \times 575 \times 4)]^{1/2}$$

$C1 = 0.028\ \mu F$ Choose $C1 = 0.022\ \mu F$

We don't want ζ to exceed 1.0. Therefore,

$$\zeta = \frac{\omega_N \times R1 \times C1}{2}$$

$$1.0 = \frac{(946 \times 10^3 \times R1) \times 0.022 \times 10^{-6}}{2}$$

$R1 = 96\Omega$

Choose $R1 = 100\Omega$

***Note:** Designing a PLL is an iterative procedure. For the DP8462, design values for R_{RATE} and R_{BOOST} typically range from 700Ω to 1.5 kΩ. The application note provides a more thorough discussion for choosing these values.

The continuous-behavior (non-quantized) approximation used to predict loop performance assumes that the phase detector output is constantly proportional to the input phase difference. In reality, the phase detector output is a pulse applied for a period of time equal to the phase difference. The function of C2 is to "smooth" the phase detector output (VCO control voltage) over each cycle. C2 also adds a second pole to the filter transfer function. This pole should be far enough outside the loop bandwidth (at least one order of magnitude) that its phase and amplitude contribution is negligable in the loop bandwidth. If

$$C2 = C1/50 = 390\ pF$$

the acquisition performance and the margin loss are not significantly changed from the predictions. If a larger C2 is used, the margin loss can be reduced at the expense of the acquisition time. This may be desirable for some systems. Please see the Disk Interface Design Guide And User's Manual Chapter 1, Sections 1.3–1.7 for a discussion of the function of C2.

Circuit Operation (Continued)

As soon as the PREAMBLE DETECTED output goes low we switch to the low track rate. To maintain stability we must ensure that $\zeta_{min} \geq 0.5$.

ζ_{min} occurs when ω_N is minimum; i.e., when we have seven consecutive zeroes (N = 8).

$$\zeta_{min} = \frac{(\omega_{Nmin} \times R1 \times C1)}{2}$$

$$0.5 = \frac{(\omega_{Nmin} \times 100 \times 0.022 \times 10^{-6})}{2}$$

$$\omega_{Nmin} = 454.5 \text{ krads/sec}$$

We can now calculate R_{RATE}

$$\omega_{Nmin} = [(2.5 \times F_{VCO})/(C1 \times R_{RATE} \times N)]^{1/2}$$

$$454.5 \times 10^3 = [(2.5 \times 20 \times 10^6)/(0.022 \times 10^{-6} \times R_{RATE} \times 8)]^{1/2}$$

Therefore, $R_{RATE} = 1.375\ k\Omega$

Choose, $R_{RATE} = 1.2\ k\Omega$

Now we calculate ω_{Nmax} and ζ_{max} in the low track rate

$$\omega_{Nmax} = [(2.5 \times 20 \times 10^6)/(0.022 \times 10^{-6} \times R_{RATE} \times 3)]^{1/2}$$

$$\omega_{Nmax} = 794 \text{ krads/sec}$$

$$\zeta_{max} = \frac{(\omega_{Nmax} \times R1 \times C1)}{2}$$

$$\zeta_{max} = 0.87$$

The final component to be determined is R_{BOOST}

$$\text{Since, } Rp = \frac{R_{BOOST} \times R_{RATE}}{R_{BOOST} + R_{RATE}}$$

$$575 = \frac{R_{BOOST} \times 1.2 \times 10^3}{R_{BOOST} + 1.2 \times 10^3}$$

Therefore, $R_{BOOST} = 1.1\ k\Omega$

DIGITAL CONNECTIONS TO THE DP8462

Figure 16 shows a connection diagram for the DP8462 in a typical application. All logic inputs and outputs are TTL compatible as shown in *Figure 14* and *15*. The VCO Clock output is 74AS compatible. All other outputs are 74ALS compatible. All inputs are 74ALS compatible and therefore can be driven easily from any 74 series devices.

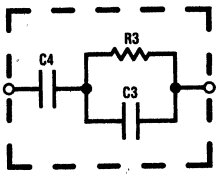

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FIGURE 13. Alternate Loop Filter Configuration

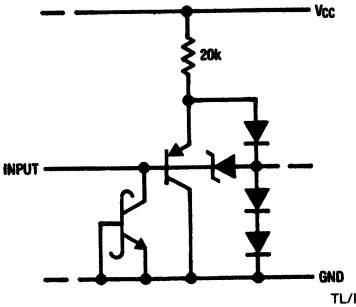

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FIGURE 14. Logic Inputs

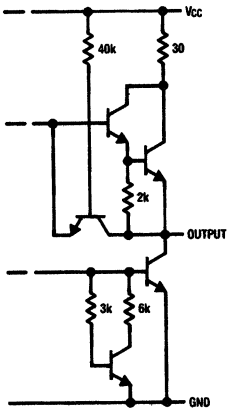

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FIGURE 15. Logic Outputs

TABLE II. Loop Filter External Component Values

Data Rate (NRZ)	Pulse Gate Components (Note 3)				Charge Pump (Note 1)		Loop Filter (Note 2)		
	R_{PG2}	R_{PG1}	C_{PG1}	C_{PG2}	R_{RATE}	R_{BOOST}	R_1	C_1	C_2
5 Mbit/sec	4.7k	150Ω	1.0 μF	0.1 μF	820Ω	1.5 kΩ	100Ω	0.03 μF	600 pF
10 Mbit/sec	1.8k	68Ω	2.2 μF	0.22 μF	1.2 kΩ	1.1 kΩ	100Ω	0.022 μF	390 pF
15 Mbit/sec	0.75k	39Ω	3.9 μF	0.39 μF	820Ω	2.7 kΩ	33Ω	0.082 μF	1600 pF

Note 1: Component tolerances are system dependent, they depend on how much loop gain deviation can be tolerated.

Note 2: Component tolerances are typically 5% but they depend on the amount of Loop Bandwidth tolerance that can be accepted.

These values have been altered from calculated values based on empirical tests of the loop.

Note 3: Component tolerances typically 10%, not critical.

Circuit Operation (Continued)

The incoming data from the pulse detector in the drive is connected to the ENCODED DATA input. PREAMBLE SELECT input is tied high or low depending on whether the user's system is employing 1000 or 100 preamble pattern. The LOCK CTL input is to be tied high or low depending on whether or not it is desired to keep the PLL in Phase and Frequency comparison mode while detecting preamble. Phase and Frequency comparison lock while detecting preamble will eliminate the chances of the PLL locking onto a harmonic of the preamble frequency when Read mode is first entered. (Susceptibility to a harmonic lock is increased when using the 1000 preamble). Since a high level on IBOOST ENABLE input puts the PLL in high track rate, it should be held high during Non-Read (standby) mode so that a quick lock is achieved upon entering Read mode. Once the PLL is locked onto the incoming data, however, this input should be taken low. Although the user is free to do this anytime, one possible method is to tie this input to the $\overline{\text{PREAMBLE DETECTED}}$ output of the chip—as shown in *Figure 16*. The READ GATE input is used to place the chip in and out of Read mode and therefore should be tied to the controller and/or a 2, 7 code Encoder/Decoder).

As for the outputs, SYNCHRONIZED DATA and VCO CLOCK may be tied to the Encoder/Decoder—which in turn would deseriallize and decode the data before sending it to the controller. $\overline{\text{PREAMBLE DETECTED}}$ output can be tied to the controller and/or the Encoder/Decoder to provide an indication when 4 consecutive bytes of preamble pattern have been detected. The only output that is not shown in *Figure 16* is the PHASE COMPARATOR TEST output. This output is the logical OR of the Phase Comparator's outputs (Charge-Up and Charge-Down inputs of the Charge-Pump). As such, pulses generated at this output provide information about the loop filter's behavior in that the envelope of the pulses generated at this output is a waveform that represents the loop filter's response to any phase difference detected by the Phase Comparator.

Finally, to improve noise immunity, Digital and Analog VCC pins should be tied together and also the Digital and Analog Ground pins should be tied together. PG1 pin should also be grounded.

Applications of the DP8462 Data Synchronizer

The DP8462 is part of National Semiconductor's DP8460 Series Disk Chip Set and therefore, is designed to work in conjunction with other members of this family; such as DP8464—the pulse detector, and DP8466—the disk data controller. A typical system application employing these components is shown in *Figure 17*. The DP8462 is based upon the proven circuitry of the DP8465 (Data synchronizer and separator for the MFM code)—the first integrated circuit to place on one chip a PLL with features that offer the improved speed and reliability required by the disk industry. Not only does the chip simplify disk system design, but also provides fast lock-on to the incoming preamble. Once locked on, the loop is set into a lower bandwidth mode. This inherent loop stability allows for a sizable amount of jitter on the data stream, such as is encountered in many disk systems. Once in the stable tracking rate, the SYNCHRONIZED DATA output represents the incoming ENCODED DATA and is synchronous with VCO CLOCK. This synchronized data is then deserialized by the ENDEC using the VCO CLOCK.

The DP8462 is capable of operating at up to a 20 Mbits/sec data rate and so is compatible with a wide assortment of disk drives. The faster data rates of the 8-inch and 14-inch disk drives will mandate the selection of the DP8462-3 parts with narrower window margin on the incoming data stream. This will also be the case when 5¼-inch drives achieve higher data rates. Some 8-inch and 14-inch disk drives incorporate the functions of the DP8462, but use many discrete ICs. In these cases, replacing these components with the DP8462 will offer reduced P.C. board area, lower cost, and improved performance while simplifying circuit testing.

Most 5¼-inch and many 8-inch and 14-inch disk drives manufactured at present do not incorporate any of the functions of the DP8462. This is so primarily because the PLL function is difficult to design and implement and requires circuitry which covers a large area of the printed circuit card. This is undesirable both from the drive size aspect and from the cost aspect (the cost includes soldering, testing, and adjusting the components). Consequently, most smaller disk drives output RLL encoded data so that the phase-locked-loop and data separation have to be performed by the controller. The DP8462 will therefore replace these functions in controller designs, as shown in *Figure 18a*.

System design criteria may now change because the DP8462 is a one-chip solution, requiring only a few external passive components with fixed values. It operates from a +5V supply, consumes about 0.5W, and is housed in a narrow 24-pin package. The circuitry has been designed so that the external resistors and capacitors need not be adjustable; the user chooses the values according to the disk drive requirements. Once selected, they will be fixed for that particular drive type. These features make it possible to transfer these functions to the disk drive, as shown in *Figure 18b*. Apart from a slight increase in board area, the advantages outweigh the disadvantages. First, the components selected are fixed for each type of drive and this facilitates the problem of interchangeability of drives. At present, components in the controller are adjusted to function with each specific drive; with the DP8462 in the drive, component adjustment will no longer be required. Second, there is often a problem of reliability of data transfer. The incoming data signal is susceptible to noise, bit shift, etc. Soft errors will occur when the incoming disk data bit position is outside the Pulse Gate window as it is being synchronized to the VCO clock in the phase-locked-loop. Obviously, the nearer the PLL is to the data source, the less chance there is that errors will occur. Thus placing the DP8462 in the drive will increase the reliability of data transfer within the system.

Applications of the DP8462 Data Synchronizer (Continued)

A third advantage is data rate upgrading. Most 5¼-inch drives have 5 Mbit/sec data rate because the early drives were made with this data rate. This meant the controllers had to be designed with PLLs which operate at this data rate. It is therefore difficult for drive manufacturers to introduce new drives that are not compatible with existing controllers. Since no new standard data rate has emerged, they must continue to produce drives at this data rate to be compatible with the controllers on the market. With the DP8462 in the drive, and its associated components set for the drive's data rate, it no longer becomes a problem to increase the data rate, assuming the controller's digital circuitry can accommodate the change. This will allow the manufacturers to increase the bit density and therefore the capacity of their drives.

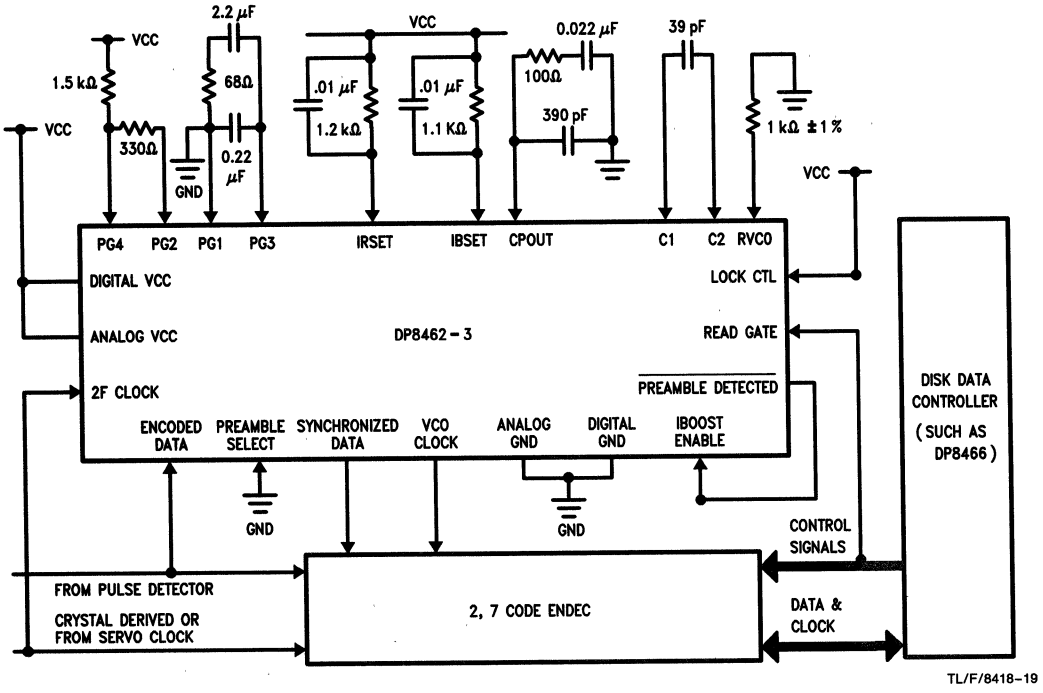

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FIGURE 16. Typical Connection to DP8462 For:

1) RLL (2,7 Code) Data Input, 10 Mbit/sec Data Rate
2) 1-0-0 Preamble Pattern
3) PLL to stay in Phase-Frequency Comparison mode until 4 bytes of Preamble Detected
4) PLL to stay in high Track Rate until $\overline{\text{PREAMBLE DETECTED}}$ asserted
5) Delay line left unadjusted (PG2 & PG4 shorted together)

Applications of the DP8462 Data Synchronizer (Continued)

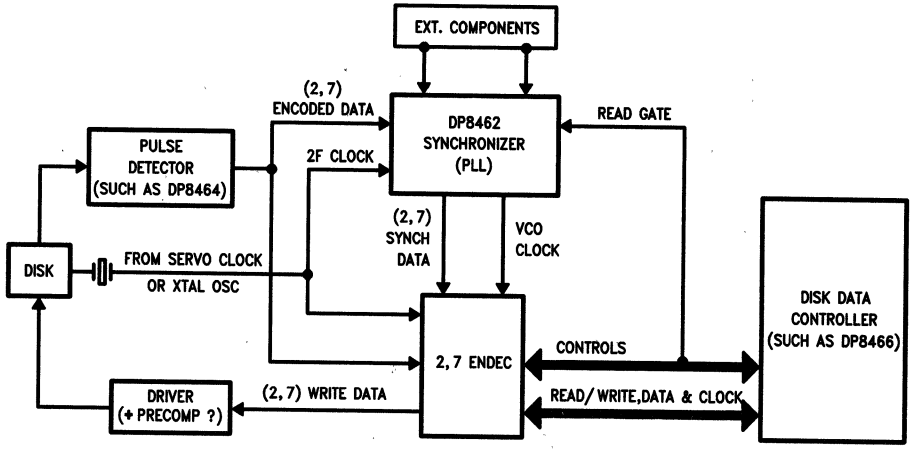

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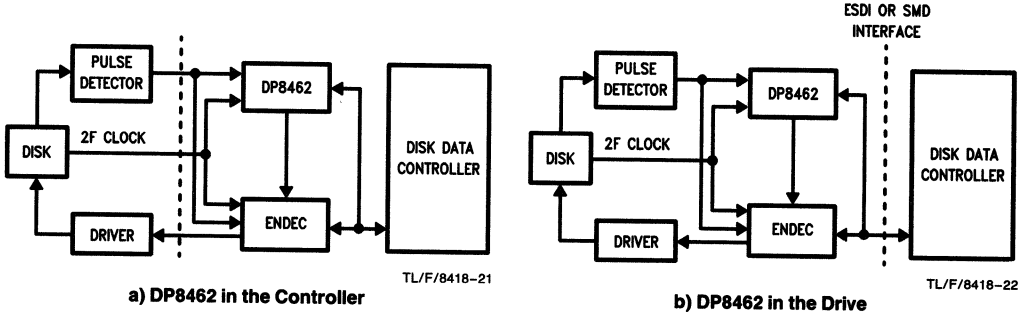
FIGURE 17. Typical Application of DP8462 in a System Employing RLL (2,7) Code



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a) DP8462 in the Controller

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b) DP8462 in the Drive

FIGURE 18. Two Different Methods of Utilizing DP8462

PRECAUTIONS IN BREADBOARDING AND PCB LAYOUT

The DP8462 contains a high performance analog PLL and certain precautions must be taken when breadboarding or designing a PCB layout. The following guidelines should be adhered to when working with the DP8462:

1) Do not wire wrap.
2) Keep component lead lengths short, place components as close to pins as possible. This applies to R1, C1, R2, C_{VCO}, R_{RATE}, R_{BOOST}, C_{RATE}, C_{BOOST}, RPG1, RPG2, and CPG1.
3) Provide a good ground plane and use a liberal amount of supply bypassing. The quieter a PLL's environment, the happier it is.
4) Avoid routing any digital leads within the vicinity of the analog leads and components.

We have used a PC board approach to breadboarding the DP8462 that gives us an excellent ground plane and keeps component lead lengths very short. With this setup we have found very stable and reliable operation. Illustrations of component layout is shown in *Figure 19*. Note that the board layout is a recommendation not a requirement.

ADDITIONAL NOTES

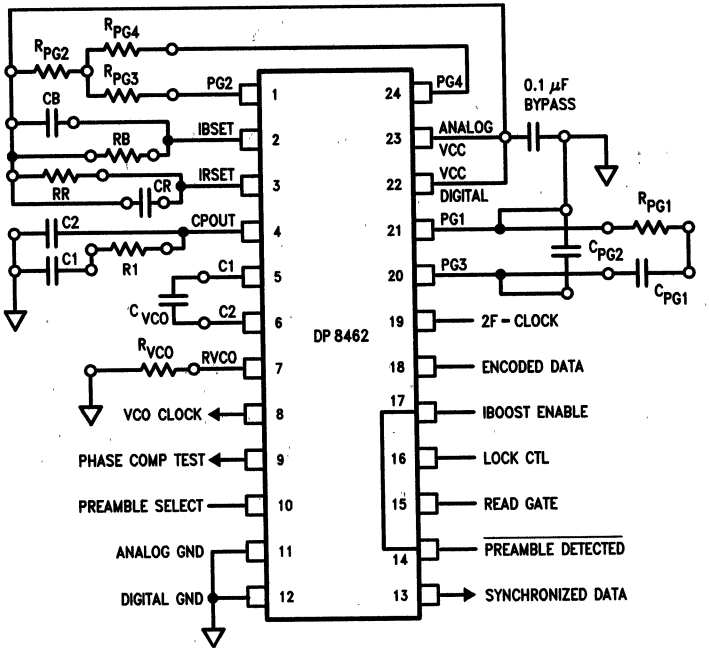
1) PG1 should be grounded to improve noise immunity.
2) 2F clock must be applied at all times; without the 2F clock, the pulse gate circuitry will not operate properly making it impossible to lock onto the incoming data stream.
3) The programming capacitor for the V_{CO} can be calculated as:

$$C_{VCO} = 1/(f_{VCO} * R_{VCO}) - 5\,pF$$

The 5 pF value is due to parasitic internal device capacitance.

4) Care must be taken in final PC board layout to minimize pin to pin capacitance, particularly in multi-layer printed circuit boards.
5) Please refer also to Precaution For Disk Data Separator Designs, NSC Application Note AN-414.

Connection Diagrams (Continued)



TL/F/8418–23

FIGURE 19. Recommended Component Layout

National Semiconductor

DP8463B (2,7) ENDEC

General Description

The DP8463B (2,7) ENDEC performs the encoding and decoding for a disk memory system using a (2,7) Run-Length-Limited (RLL) code. This code gives a disk system the ability to record up to 50% more message data in the same media space without any increase in the Flux Changes per Inch (FCI) density, when compared to a system using Modified Frequency Modulation (MFM) coding. The DP8463B also performs other functions of writing or reading format segments that can not be done by a disk data controller. These additional functions include the writing and reading of Preambles (PLL synchronization fields) and various soft-sector format Address Marks that are compatible with (2,7) RLL code. The user may also select different lengths of preamble to count before the DP8463B issues a Lock Detect signal. The encoded CODE OUT output is automatically resynchronized to the 2f CRYSTAL/SERVO CLOCK for perfect periodic writing regardless of the duty cycle of the WRITE CLOCK input and regardless of the phase relationship between the WRITE CLOCK and the 2f CRYSTAL/SERVO CLOCK. The READ/REFERENCE CLOCK output is switched between clock sources without generating any short pulses. In addition to the detecting of standard ESDI and SMD Address Marks, there is an optional noise tolerant mode that allows the recognizing of an address mark gap even with a bit or two of noise.

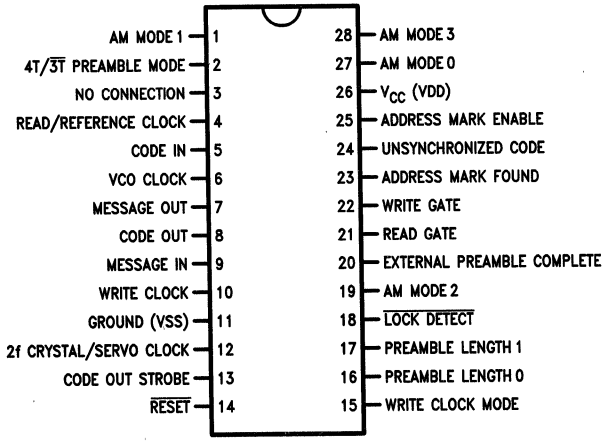
The DP8463B is compatible with the Storage Module Drive (SMD) and Enhanced Small Device Interface (ESDI) functional specifications, and has a format mode similar to the one used in ST-506 devices. The Input/Output (I/O) of the DP8463B are active-high, except LOCK DETECT, so inverting line drivers should be used for interfacing with the active-low I/O of ESDI. The term "Message" is used to designate unencoded data, also referred to as NRZ Data in disk literature. The term "Code" designates the encoded data.

Features

- Up to 50% increase in message data density over MFM
- Encodes and decodes using IBM (2,7) Message/Code Table
- Programmable Formats
  - — Hard Sector
  - — Soft Sector with Address Mark preceding Preamble
  - — Soft Sector with Address Mark following Preamble
- Programmable Address Marks
  - — ESDI 3-Byte transitionless gap, preceding Preamble
  - — ESDI 3-Byte transitionless gap, noise tolerant
  - — SMD 3-Byte transitionless gap, preceding Preamble
  - — SMD 3-Byte transitionless gap, noise tolerant
  - — IBM 2-Byte gap with three transitions, preceding Preamble
  - — N7V 2-Byte Address Mark with code word not in message/code table that does not violate (2,7) code constraints, following Preamble
    (Above gap lengths are in message-bytes)
- Programmable Preamble length counted before LOCK DETECT issued
  - — Externally determined (e.g., from DP8462 Data Synchronizer)
  - — 6 Message Bytes
  - — 8 Message Bytes
- Code output is resynchronized to 2f CRYSTAL/SERVO CLOCK
- Glitchless Multiplexer is used to switch between READ/REFERENCE CLOCK sources
- Strobe available to clock CODE OUT output into external register
- ADDRESS MARK FOUND appears after first "1" bit following Address Mark
- Message Data Rate to 20 Megabits/second (Code rate = 40 Mb/s)
- Compatible with ESDI
- Compatible with SMD
- Compatible with DP8462 Data Synchronizer
- Compatible with DP8466 Disk Data Controller
- 2-micron dual metal CMOS
- Single +5V Supply
- Packages
  - — 28-pin Dual-In-Line Package
  - — 28-pin Plastic Chip Carrier

Connection Diagrams

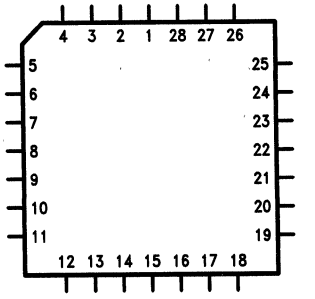
Dual-In-Line Package (DIP)



TL/F/9058–1

Order Number DP8463BN
See NS Package Number N28B

Plastic Chip Carrier
(Signal Assignments to the Pin Numbers are Identical to DIP)



TL/F/9058–2

Order Number DP8463BV
See NS Package Number V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	−0.5V to +7.0V
Input or Output Voltage	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C
Lead Temperature	260°C

Recommended Operating Conditions

Temperature Range (T_A)	+0.0°C to +70°C

ESD rating is to be determined.

DC Electrical Characteristics

V_{CC} = +5V ±10%; Min./Max. limits apply across temperature range T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		2.25		V
V_{IL}	Low Level Input Voltage			0.65	V
V_{OH1}	High Level Output Voltage	V_I = V_{CC} or GND I_O = 20 μA	V_{CC} − 0.1		V
V_{OH2}	High Level Output Voltage	V_I = V_{CC} or GND I_{OH} = −4.0 mA	3.5		V
V_{OL1}	Low Level Output Voltage	V_I = V_{CC} or GND I_O = 20 μA		0.1	V
V_{OL2}	Low Level Output Voltage	V_I = V_{CC} or GND I_{OL} = +4 mA		0.4	V
I_{IH}	High Level Input Current	V_I = V_{CC}		+10	μA
I_{CC} DY	Supply Current, Dynamic	V_I = V_{CC} or GND T_A = 25°C, f_{VCO} = 40 Mb/s		60	mA
I_{CC} SB	Supply Current, Standby	V_I = V_{CC} or GND T_A = 25°C, f_{VCO} = 1Mb/s		10	mA

AC Electrical Characteristics

(V_{CC} = 5V ±10%; Min./Max. limits apply across temperature unless otherwise specified. Output Load = 50 pF.)

Symbol	Parameter	Part No.	Min	Typ	Max	Units
f_{DATA}	Maximum Message Data Frequency (NRZ Data)	DP8463B-12	12			Mb/s
f_{VCO} $f_{C/S}$	Maximum VCO Frequency Maximum CRYSTAL/SERVO CLOCK frequency	DP8463B-12	24			Mb/s
t_{MISU}	Set-Up Time of MESSAGE IN Before WRITE CLOCK Positive Edge		10			ns
t_{MIH}	Hold Time of MESSAGE IN After WRITE CLOCK Positive Edge		10			ns
t_{MOSU}	Set-Up Time of MESSAGE OUT Before READ/REFERENCE CLOCK Positive Edge		24			ns
t_{MOH}	Hold Time of MESSAGE OUT After READ/ REFERENCE CLOCK Positive Edge		14			ns
t_{CISU}	Set-Up Time of CODE IN Before VCO CLOCK Positive Edge		7			ns
t_{CIH}	Hold Time of CODE IN After VCO CLOCK Positive Edge		10			ns
t_{COSU}	Set-Up Time of CODE OUT Before CODE OUT STROBE Positive Edge		10			ns
t_{COH}	Hold Time of CODE OUT After CODE OUT STROBE Positive Edge		5			ns
t_{PWUC}	Pulse Width of UNSYNCHRONIZED CODE		10			ns
t_{PWPC}	Pulse Width of EXTERNAL PREAMBLE COMPLETE		4			VCO Clock Periods
t_{pdIE}	Propagation Delay of IBM Encoder from WRITE CLOCK Positive Edge to CODE OUT		7		7	Code Bits
			+5		+45	ns
t_{pdIDC}	Propagation Delay of IBM Decoder from VCO CLOCK Postive Edge to READ/REFERENCE CLOCK Positive Edge		5.5		5.5	Code Bits
			+5		+62	ns
WCL	WRITE CLOCK Low		20%		80%	WRITE CLOCK Period
WCH	WRITE CLOCK High		20%		80%	

Note 1. Mb/s = Megabits/second

Code bit = period of 2f or VCO Clock

Pin Descriptions

Pin No	Description
POWER	
11	**GROUND (V_{SS})**
26	**V_{CC} (V_{DD})**
INPUT SIGNALS	
5	**CODE IN.** This is the encoded data output of the data synchronizer (e.g., DP8462). Each flux transition on the disk is a high level signal here with a width of one VCO clock period. The CODE IN is read by the DP8463B at the time of the positive going edge of the VCO CLOCK.
6	**VCO CLOCK.** This is the VCO clock output of the data synchronizer (e.g., DP8462). During the read mode, the VCO CLOCK is phase locked to the flux transitions on the disk.
9	**MESSAGE IN.** This is the unencoded "write data" from the disk data controller (e.g., DP8466). MESSAGE IN is read into the DP8463B by the positive going edge of the WRITE CLOCK input.
10	**WRITE CLOCK.** This clock strobes the MESSAGE IN "write data" into the encoder.
12	**2f CRYSTAL/SERVO CLOCK (2f C/S CLOCK).** This is the clock output of a disk drive's dedicated servo track or the buffered output of a crystal oscillator. This signal is the reference clock for generating the CODE OUT signal when the WRITE CLOCK MODE pin is low.
14	**$\overline{\text{RESET}}$.** An active low input resets various flip-flops when the next 2f C/S CLOCK positive edge occurs, so RESET should have a pulse width of two 2f C/S CLOCK periods. The DP8463B should be reset after each time power is applied.
20	**EXTERNAL PREAMBLE COMPLETE.** With PL1 and PL0 both low, an "active" level on this pin signals the DP8463B that the reading of the preamble, for phase locking purposes, is complete. The DP8463B then switches into its normal decoding mode and issues an active low LOCK DETECT signal. This mode could be used for short preamble lengths in conjunction with the DP8462. The DP8462 Lock Detect output would be connected to the EXTERNAL PREAMBLE COMPLETE (observing polarities, see pin 28). The DP8462 will issue a "Lock Detect" after counting 16 code ones (3 to 4 Message Bytes depending upon which preamble pattern is used, 3T or 4T). The DP8463B must receive at least two 4T preamble patterns before an EXTERNAL PREAMBLE COMPLETE signal is received. The "active" level of this pin is determined by the state of pin 28, ADDRESS MODE 3.
21	**READ GATE.** An active high level input places the DP8463B in the read mode. During this mode: the source of the READ/REFERENCE CLOCK is switched to the VCO CLOCK/2, the address mark is searched for (if selected), the length of the preamble is counted as programmed, and the CODE IN signal is decoded and output as MESSAGE OUT at the appropriate time per the programming of the mode pins.
22	**WRITE GATE.** An active high level input places the DP8463B in the write mode. During this mode: the MESSAGE IN data is encoded and output as CODE OUT, and during the programmed time (when selected), the preamble and address marks appear at CODE OUT.
24	**UNSYNCHRONIZED CODE.** This is the encoded data output of the pulse detector (e.g., DP8464B). A flux transition on the disk produces an active high pulse for this pin. This input is used to detect the ESDI, SMD, and IBM address marks.
25	**ADDRESS MARK ENABLE (AME).** An active high level, while WRITE GATE is also active high, will write the address mark prescribed by the AM MODE pins. The AME must be high for the complete address mark. An active high level of AME while WRITE GATE and READ GATE are both low causes the 8463B to search for an Address Mark when in the ESDI Mode (AM2 & AM1 low). An active high level of AME when READ GATE is active high causes the 8463B to search for an AM when in the SMD Mode (AM2 low, AM1 high).
PROGRAMMING INPUTS	
1	**ADDRESS MARK MODE 1 (AM MODE 1).** Defined in Table I. A logic "1" is a high level.
2	**4T/$\overline{\text{3T}}$ PREAMBLE MODE.** A high level places the DP8463B in the mode to generate and detect "4T" preamble patterns (i.e., 1000 in code which is four time periods). In this mode, the MESSAGE IN input is inverted in the DP8463B before being encoded so that a 4T preamble can be generated from an all zeros MESSAGE IN data stream. The output of the decoder is also inverted in this mode so the double inversion is transparent to the user. The double inversion is always done in this mode, not just during the preamble. A low level input on this pin places the DP8463B in the mode to accept the "3T" pattern as the preamble (3T pattern is 100 in code). The Input/Output is not inverted in this mode. If the 3T preamble pattern is used with the IBM code, a non-zero three-bit repeating input pattern is required which

Pin Descriptions (Continued)

Pin No	Description
PROGRAMMING INPUTS (Continued)	
2 (Cont.)	is typically impossible for a disk data controller to generate. Therefore there is a special mode during which the disk data controller's input to MESSAGE IN is ignored by the encoder section and the DP8463B internally generates a 3T code output; as long as the MESSAGE IN input is all zeros. This 3T preamble starts after the initiation of WRITE GATE going active (high) and continues until the first "1" is seen at the MESSAGE IN pin. This mode of internally generating a 3T preamble with IBM code is activated by having high levels on the two PREAMBLE LENGTH 0 and PREAMBLE LENGTH 1 pins (16 & 17).
3	**NO CONNECTION.** This pin must be left open-circuited or tied to V_{CC}.
15	**WRITE CLOCK MODE.** A low level enables the automatic resynchronization circuitry for the IBM encoder. The WRITE CLOCK is resynchronized to the 2f C/S CLOCK and used for clocking the IBM encoder. The same 2f C/S is used to clock a flip-flop that provides the CODE OUT signal. A high level WRITE CLOCK MODE input allows the WRITE CLOCK to directly clock the IBM encoder. In this mode the CODE OUT signal comes directly from the encoder and does not get strobed out by the 2f C/S CLOCK.
16	**PREAMBLE LENGTH 0 (PL0).** This input and PREAMBLE LENGTH 1 (PL1) determine the length of preamble that is read before an active low LOCK DETECT signal is issued. These two pins also control the internal generation of a 3T preamble pattern for use with an all zeros MESSAGE IN input.

PL1	PL0	LENGTH OF PREAMBLE/ OTHER FUNCTION
0	0	Length Set by External Preamble Complete
0	1	6 Message Bytes
1	0	8 Message Bytes
1	1	6 Message Bytes/Generate 3T Preamble Internally

17	**PREAMBLE LENGTH 1 (PL1).** See pin 16.
19	**ADDRESS MODE 2.** Defined in Table I.
27	**ADDRESS MODE 0.** Defined in Table I.
28	**ADDRESS MODE 3.** Defined in Table I. The level of this pin also determines the active level polarity of the pin 20 EXTERNAL PREAMBLE COMPLETE input. This is possible since the Table 1 function is a Don't Care for all except one type of the N7V Address Mark. If ADDRESS MODE 3 is high or open-circuited, then pin 20 is active high. If ADDRESS MODE 3 is low, then pin 20 is active low.

Pin No	Description
OUTPUT SIGNALS	
4	**READ/REFERENCE CLOCK.** This is the clock that is provided to the disk data controller where it is typically labelled "read clock". It is, however, necessary for both reading and writing. The source of the clock is different during reading compared to writing. When READ GATE is active (high) the READ/REFERENCE CLOCK is the VCO CLOCK divided-by-two. The MESSAGE OUT data is read by the disk data controller using the positive going edge of READ/REFERENCE CLOCK. When READ GATE is inactive (low), the READ/REFERENCE clock is the 2f C/S CLOCK divided-by-two. This clock is used by the disk data controller as the timing source for its WRITE DATA and WRITE CLOCK outputs.
7	**MESSAGE OUT.** This is the "Read Data" input to the disk data controller. A high level represents a "one" of decoded (NRZ) data. It is read by the controller using the positive going edge of the READ/REFERENCE CLOCK. MESSAGE OUT is held at a low level when READ GATE is inactive (low) and other intervals specified in Table I.
8	**CODE OUT.** A high level for a 2f clock period is output for each "1" in code that is to be written on the disk as a flux transition by a write amplifier containing a write flip-flop that changes state every time a positive going pulse edge is received. Since (2,7) code always has at least two zeros between adjacent ones, this output is a Return-to-Zero (RZ) code. If the CODE OUT is to be sent to another register, instead of directly to the Write Amplifier, it can be clocked out by using the CODE OUT STROBE.
13	**CODE OUT STROBE.** The positive going edge of this signal should be used as the clock input to an external shift register for applications where the CODE OUT is transformed before being sent to the Write Amplifier, e.g., for precompensation of some code patterns on some tracks.
18	**$\overline{\text{LOCK DETECT}}$.** A low level signifies that a minimum, uninterrupted length of the programmed preamble pattern has been read. The length of the preamble read is programmed by PREAMBLE LENGTH 0 and 1. The LOCK DETECT level returns to a high when READ GATE goes inactive (low).
23	**ADDRESS MARK FOUND (AMF).** A high level appears when an address mark has been sensed and, depending upon programming, other conditions may also be required before the AMF goes active (high). Table I specifies the various conditions under which AMF becomes active and inactive. Also see the Address Mark section under "Description of Format and Circuit Characteristics".

TABLE I. Address Mark Modes

AM Mode	Program Inputs				AM Written	AM Read	Inputs		Output	
	AM 3	AM 2	AM 1	AM 0			Read Gate During AM Search	AME During AM Search	AMF Goes Active When:	AMF Returns Inactive When:
ESDI, Fully Compatible	X	0	0	0	ESDI	ESDI	Inactive (L)	Active (H)	AM Found & 1st Code "1" Following AM	AME Goes Inactive
ESDI, Noise Tolerant	X	0	0	1	ESDI	ESDI or IBM	Inactive (L)	Active (H)		
SMD, Fully Compatible	X	0	1	0	SMD	SMD	Active (H)	Active (H)		
SMD, Noise Tolerant	X	0	1	1	SMD	SMD or IBM	Active (H)	Active (H)		
Hard Sector	X	1	0	0	None (ESDI/SMD Signals)	None	Don't Care	Don't Care	NA	NA
ESDI/SMD (8466 Comp.)	X	1	0	1	ESDI = SMD	ESDI = SMD	Don't Care	Don't Care	AM Found & 1st Code "1" Following AM	2nd Code "1" Following AM is Read
IBM	X	1	1	0	IBM	IBM	Don't Care	Don't Care		
N7V-A (Note 1)	1	1	1	1	N7V (In Header & Data Segments)	N7V (In Header & Data Segments)	Active (H)	Don't Care	AM Found & 1st Message "1" Following AM	Read Gate Goes Inactive (L)
N7V-B	0	1	1	1	N7V (In Header Only)	N7V (In Header Only)	Active (H)	Active (H)		

X = Don't Care NA = Not Applicable

(Continued on next page)

TABLE I. Address Mark Modes (Continued)

AM Mode	Program Inputs AM 3	AM 2	AM 1	AM 0	Phase Sync (Byte) Requirements:	Byte Sync (Byte) Requirements	MESSAGE OUT = 0 Until: (& Phase Sync Mode Ends) (Note 2)
ESDI, Fully Compatible	X	0	0	0	1. With 4T Preamble: Function done by all zeros preamble. 2. With 3T Preamble: Recommend writing 10111100 which is read as 00000000.	1. With 4T Preamble: Must have one or more "1"s; with one in leading position, preferably. 2. With 3T Preamble: Must have one or more "1"s; Leading two bits should be zeros.	1. With 4T Preamble: After 6 or Programmed number of bytes of preamble are read. 2. With 3T Preamble: After two 4T patterns in phase sync byte are read.
ESDI, Noise Tolerant	X	0	0	1			
SMD, Fully Compatible	X	0	1	0			
SMD, Noise Tolerant	X	0	1	1			
Hard Sector	X	1	0	0			
ESDI/SMD = (8466 Comp.)	X	1	0	1			
IBM	X	1	1	0			
N7V-A (Note 1) N7V-B	1 0	1 1	1 1	1 1	1. With 4T Preamble: Write 8 zeros. 2. With 3T Preamble: Write 8 ones.	3. With 4T Preamble: Use 00000010 & 00000011. Same as 1 and 2 Above.	[N7V AM is Detected] (N7V AM Detected • AME) + N7V AM Detected • $\overline{\text{AME}}$ For Header / For Data Segment (Note 3)

X = Don't Care NA = Not Applicable

Note 1. Use only for 8463A compatibility where there is an N7V AM in both header & data segments.

Note 2. After the time MESSAGE OUT = 0, MESSAGE OUT = Decoded CODE IN

Note 3. Data segment has no AM

TABLE II. Message Data/Code Tables

IBM (2,7,1,2,3) Message Data/Code Table

Normal Message Data		Inverted Message Data		Code	
MSB	LSB	MSB	LSB	MSB	LSB
000		111		000100	
10		01		0100	
010		101		100100	
0010		1101		00100100	
11		00		1000	
011		100		001000	
0011		1100		00001000	

Most Significant Bit (MSB) is read/written first.

Use the Normal Message Data column when 4T/$\overline{3T}$ PREAMBLE MODE (pin 2) is low.

Use the Inverted Message Data column when 4T/$\overline{3T}$ PREAMBLE MODE is high.

NOTE: The IBM (2,7,1,2,3) Code and some implementations of it are patented by IBM. National Semiconductor Corporation (NSC) has a license agreement with IBM enabling NSC to incorporate a particular implementation of the IBM (2,7) Endec in an integrated circuit for sale to others. Also see the Patent Indemnification section in NSC's Standard Terms and Conditions for Sales.

Note: Definition of (2,7,1,2,3):

2 = minimum number of zeros between adjacent code ones

7 = maximum number of zeros between adjacent code ones

1 = ratio of message data bits to code bits with first number (1)

2 = being the number of message bits

3 = number of different lengths of message data words

Description of Format and Circuit Characteristics

1. Address/Sector Marks

1A. Hard Sector Format—Sector Mark

In this format the sector mark signal from the disk drive is sent directly to the disk data controller and the DP8463B is not involved.

1B. Soft Sector Format—Address Mark (AM)

1B-1. ESDI Address Mark

This is a gap on the disk without any flux transitions for a length of three message bytes. The gap appears at the start of each sector. It is written by having the ADDRESS MARK ENABLE (AME) active (high) for 3 message bytes while WRITE GATE is also active (high). The AM is detected when an interval of 16 message bit times passes without a flux transition. Table I shows three different modes for using the ESDI AM. The "ESDI, FULLY COMPATIBLE" is the fully-compatible-with-ESDI specifications mode where AME is active (high) while READ GATE and WRITE GATE are inactive (low) when looking for an AM. When the AM is found, ADDRESS MARK FOUND (AMF) goes active (high), the disk data controller receives this and responds by having READ GATE go active (high) and AME go inactive (low). The AME going inactive will cause the 8463B's AMF to go inactive (low). A second mode "ESDI, NOISE TOLERANT" has the ability to accept a few noise bits in the AM gap and still output an AMF. (See Noise Tolerant ESDI/SMD AM section for full explanation). A third mode of ESDI AM has the state of the AME, during an AM search, as a "don't care" for compatibility with the DP8466 controller. In all these modes, the AMF appears only after both the AM is sensed and the first code "1" bit of the preamble is detected.

1B-2. SMD Address Mark

This AM is the same 3 message byte gap as ESDI. The difference is the state of READ GATE during the search for an AM. For SMD compatibility, READ GATE must be active (high) during the AM search. The three SMD modes shown in Table I are analogous to the three ESDI modes.

1B-3. IBM Address Mark:

This AM is a gap of 32 code bits which has no flux transitions except for two transitions in bit positions 8 and 20. The first 7 bit positions are "don't cares" per IBM's definition. The DP8463B writes a "1" (transition) in positions 3, 8 and 20. The DP8463B detects these AMs by detecting two gaps of 10 bits with a "1" between the two gaps. If the first gap is larger than 16 bits, the detector will reset and begin again.

1B-4. Noise Tolerant ESDI/SMD AM:

These modes will accept a perfect 2-message-byte ESDI or SMD gap or a gap which contains some noise bits. The ESDI/SMD AM gap detector is ORed with the IBM AM detector so an AMF will appear if either a 2-message-byte gap (32 code bits), or two 10-code-bit gaps with a "1" in between, is detected in the 3-message-byte (48 code bits) gap. The 16-bit limit on the first gap of the IBM AM detector is disabled.

1B-5. N7V Address Mark (N7V = Non 7 Violation):

This AM is a unique code word that does not violate the (2,7) RLL constraints but can not be generated by any message input to the IBM encoder. The N7V AM is a two-message-byte AM that must follow the preamble, since the decoder must be in phase sync to read the AM properly. The first byte of the AM consists of 4T phase sync patterns, the second byte is the unique N7V pattern. If the disk data controller randomly asserts READ GATE, the possibility of the N7V AM being detected in the write splice or in the data, before phase sync has been achieved, must be avoided. This can be done by not routing the CODE IN input to the 8463B until several bytes of the preamble have been detected externally. For example, this is done simply with the DP8462 by ANDing its SYNCHRONIZED DATA output with its inverted LOCK DETECT output, since the LOCK DETECT only appears after 3 or 4 bytes of the preamble have been read.

See Table I for more detail of Inputs/Outputs during AM reading and writing.

Description of Format and Circuit Characteristics (Continued)

2. Phase Sync Pattern

The decoder must be able to distinguish between the odd and even code bits to decode properly. This is impossible to do with the maximum frequency "3T" code pattern (100) in a preamble because the "1" alternates between odd and even positions. The "4T" code pattern (1000) must be used, along with the knowledge of what message pattern was used to generate it. A "3T" preamble can be used if it is followed by two "4T" patterns before data is read. See *Figure 1* formats for examples, and Table II for encode/decode definitions.

3. Byte Sync Pattern:

The purpose of the Byte Sync (or Sync Byte) is to define the message byte boundary for the disk data controller. The Byte Sync message byte should consist of one or more "1"s. With "4T" preambles, the Byte Sync should, preferably, have a "1" in the leading bit position. With "3T" preambles, the Byte Sync should have zeros in the two leading positions (to buffer it in time from the phase sync byte).

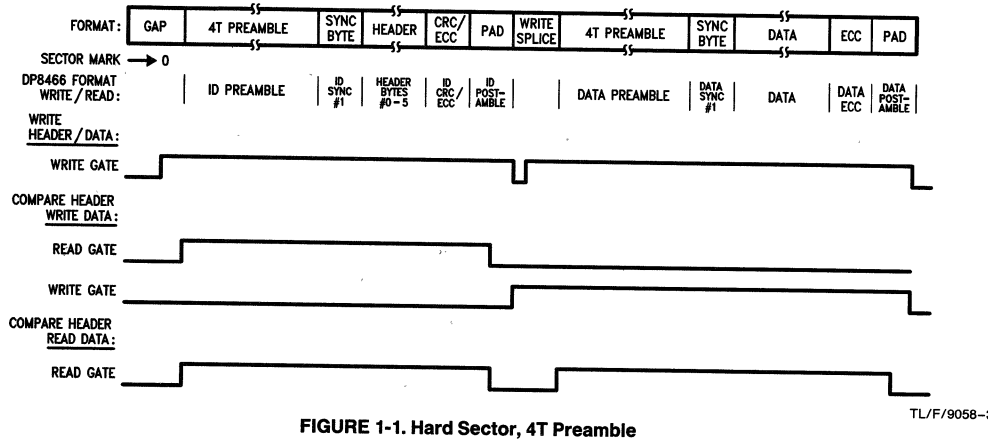
4. Error Propagation:

Since a single bit-shift error in a code word may be decoded as a different message word, there is error propagation. The longest error burst found for the IBM Code is 5 message bits. Therefore, the disk system must have Error Checking and Correcting (ECC) circuitry capable of correcting these errors.

5. Format Examples:

Figure 1 illustrates the sector formats and timing of various control signals for each of the Address Mark Modes and Preamble types for both reading and writing.

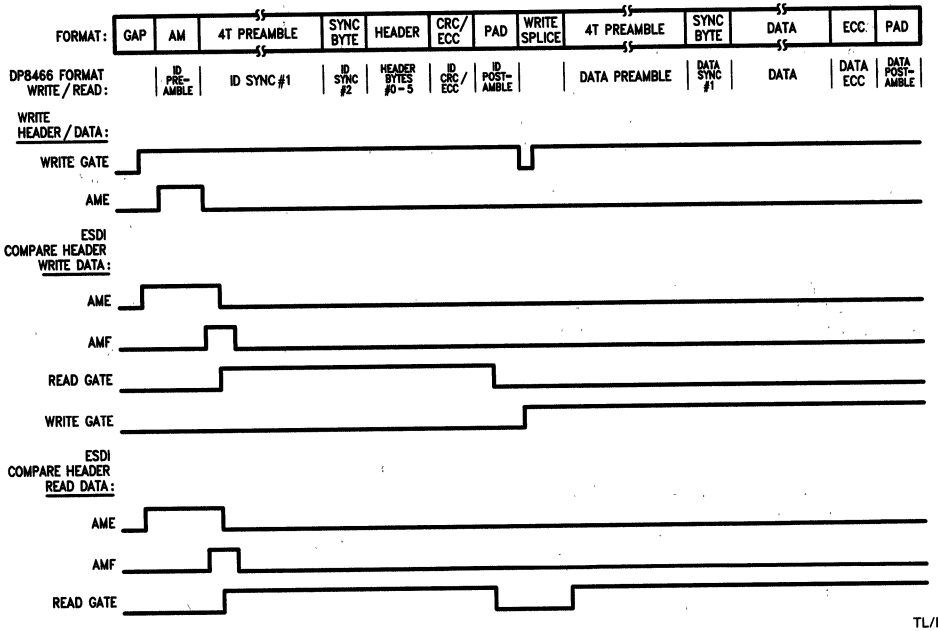
Formats



TL/F/9058–3

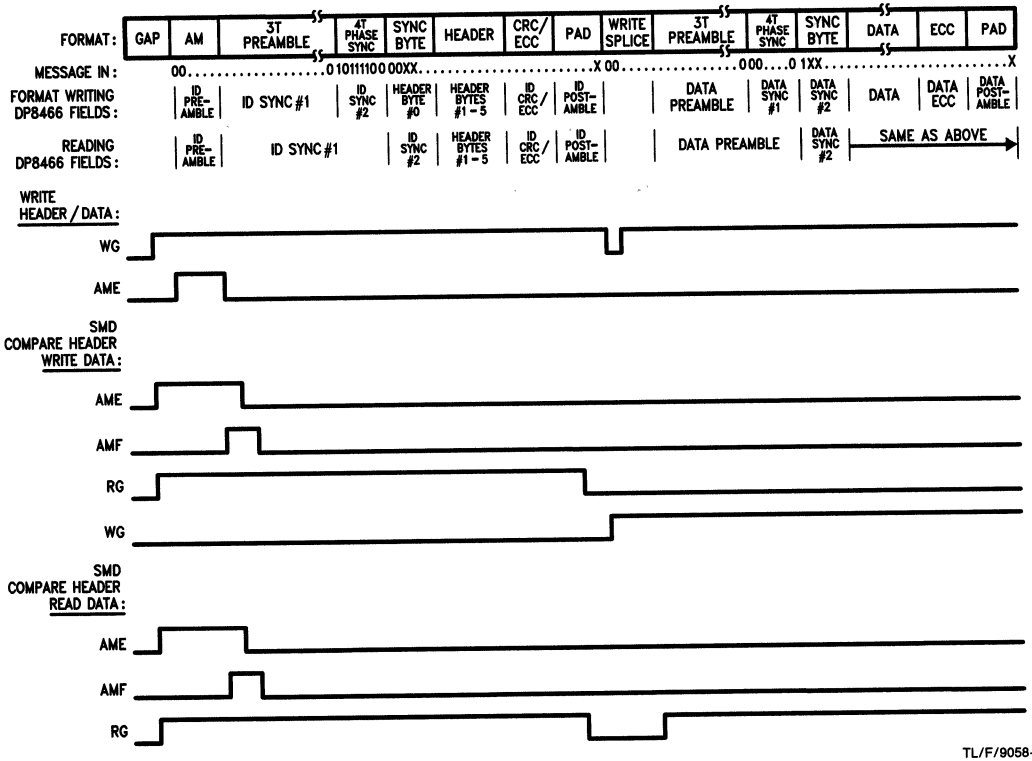
FIGURE 1-1. Hard Sector, 4T Preamble

Formats (Continued)



TL/F/9058-4

FIGURE 1-2. SMD, ESDI, IBM Address Mark, 4T Preamble



TL/F/9058-5

FIGURE 1-3I. ESDI, SMD, or IBM AM, 3T Preamble

Formats (Continued)

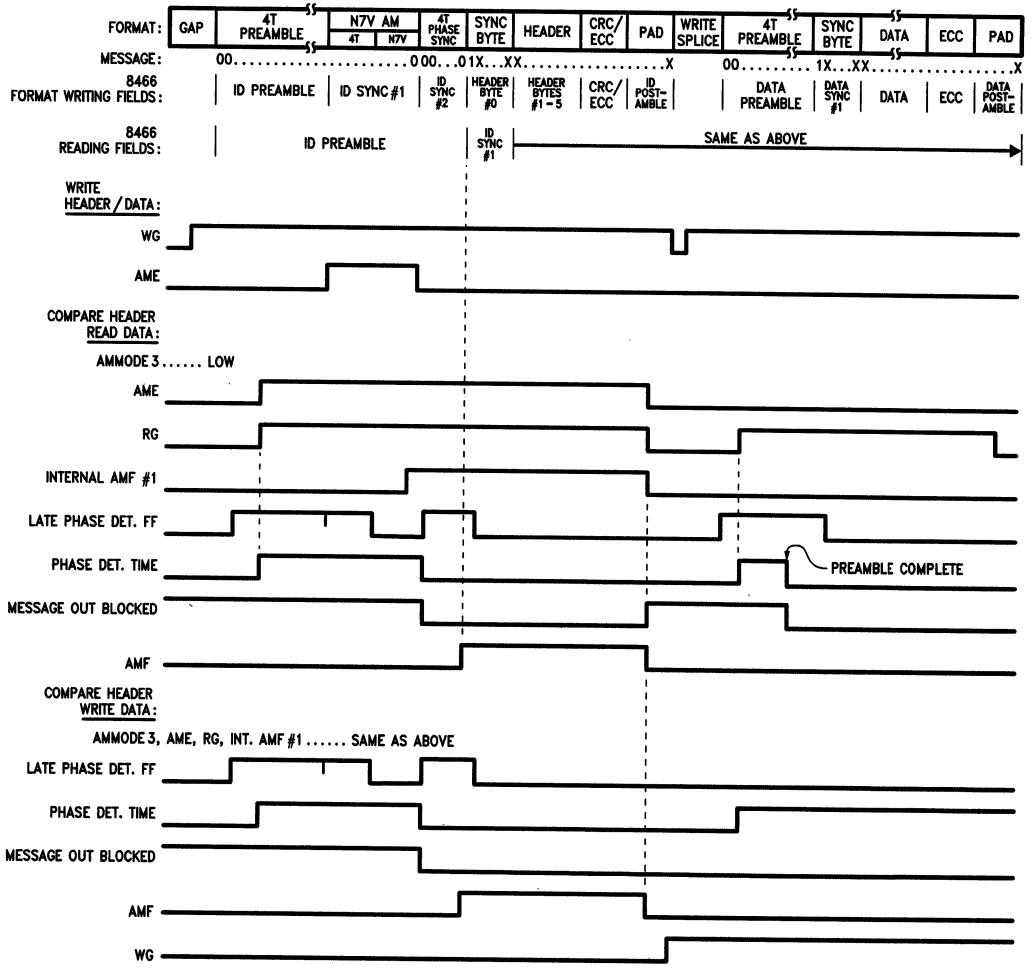


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FIGURE 1-4. 4T Preamble, N7V AM (N7V-B Mode)

Formats (Continued)

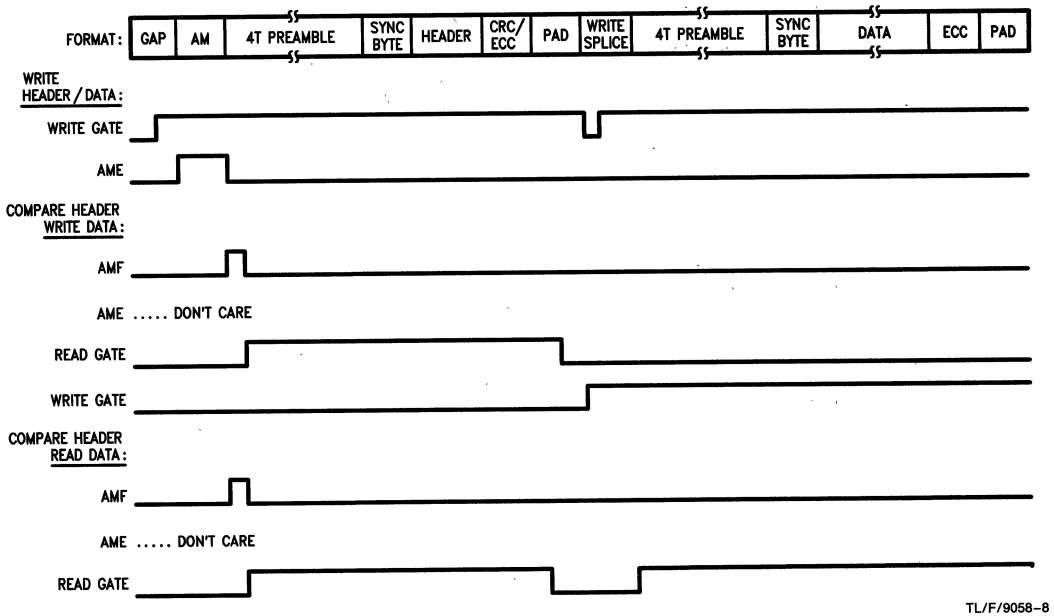

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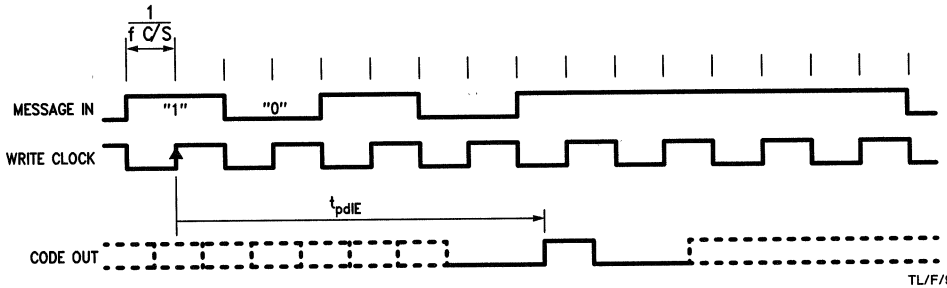
FIGURE 1-5. ESDI, SMD, or IBM AM; 4T Preamble (with Read Gate & AME as "don't cares" during search for AM)

Timing Waveforms

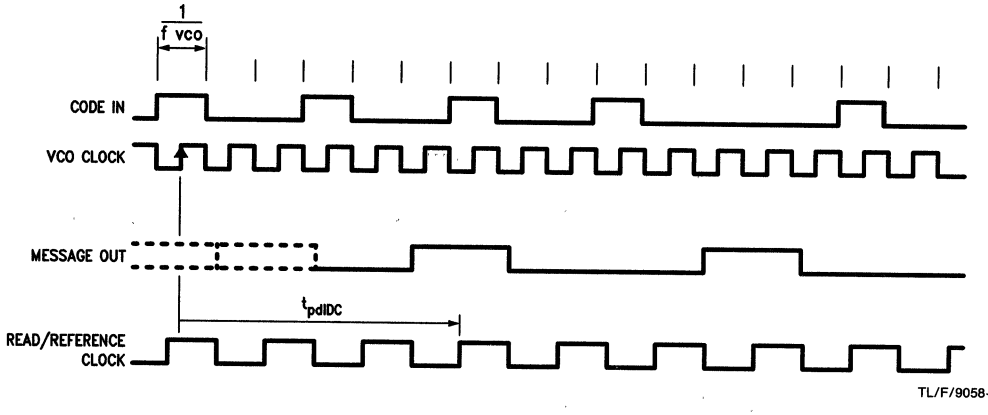
IBM Encoder



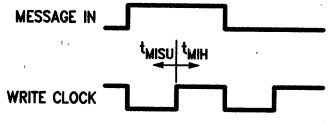
TL/F/9058–14

Timing Waveforms (Continued)

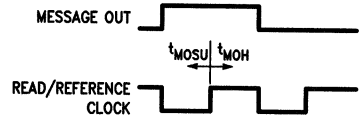
IBM Decoder



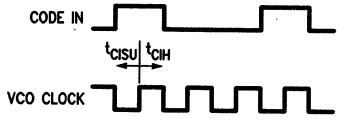
TL/F/9058–15



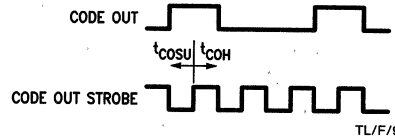
TL/F/9058–16



TL/F/9058–17



TL/F/9058–18



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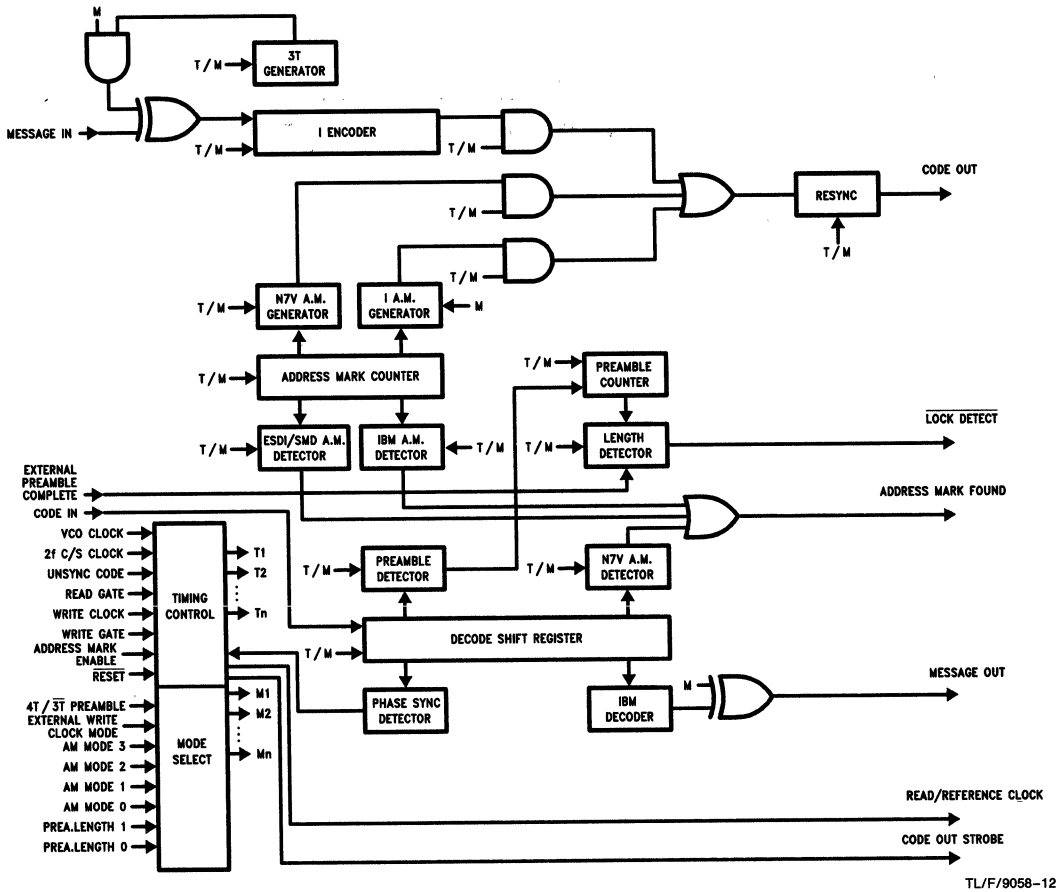
2

Typical Applications

DP8463B (2, 7) Endec Block Diagram



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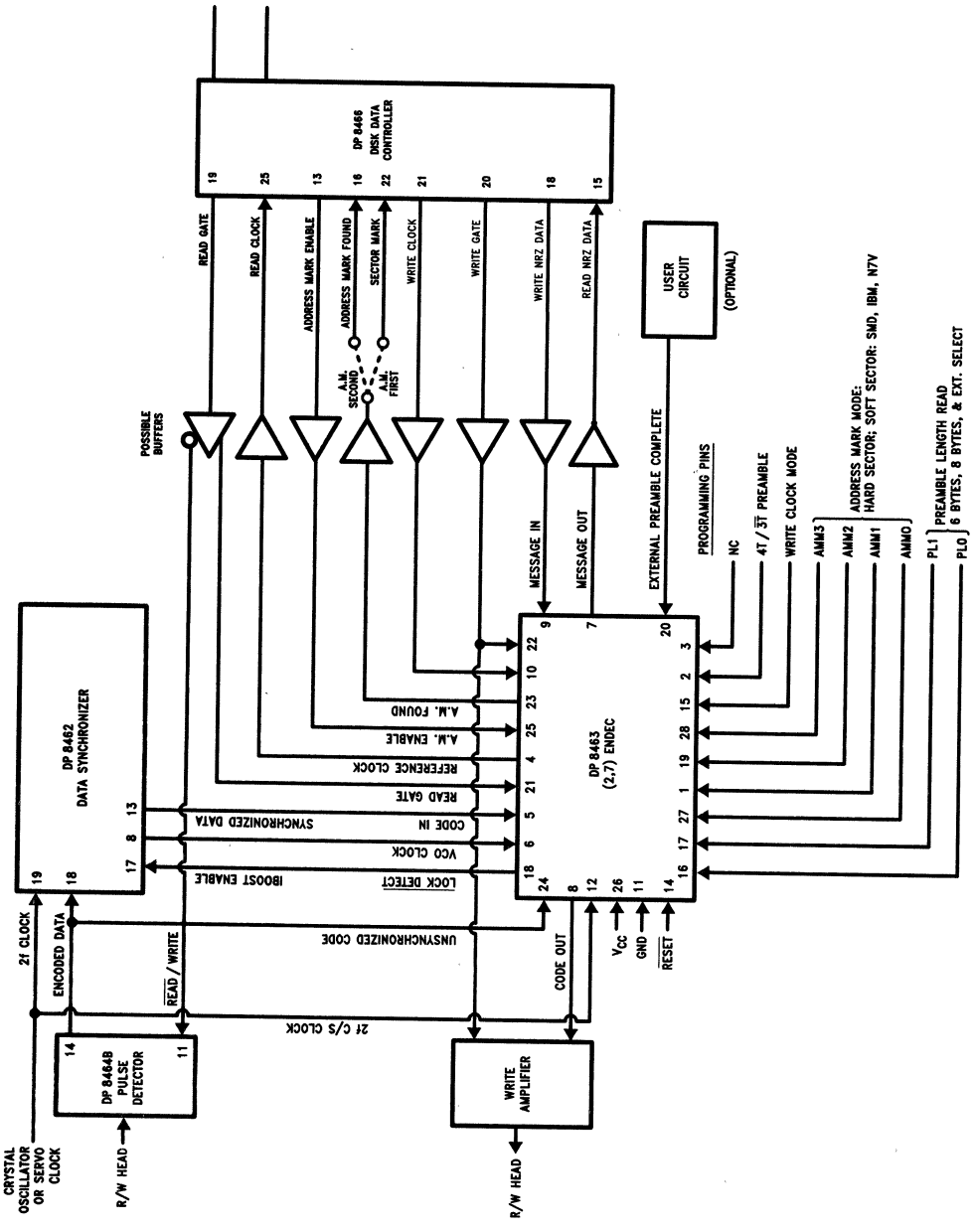
Typical Applications (Continued)

Hard Disk Chip Set with (2, 7) RLL Codes



TL/F/9058–13

National Semiconductor

PRELIMINARY

DP8469 Synchronizer/2,7 Endec

General Description

The DP8469 data synchronizer/2,7 endec is intended for use in magnetic disk, optical disk, or tape drives during reading and writing operations. The device utilizes a fully integrated PLL to synchronize 2,7 serial code and convert data between one of several hard and soft sectored versions of 2,7 RLL (Run Length Limited) and serial NRZ code format. The DP8469 synchronizer/endec incorporates both the DP8459 synchronizer and the DP8463 2,7 code endec functions together in a 28-pin PCC package.

In the read mode, the device receives 2,7 RLL coded data from the drive's pulse detector, resynchronizes it, and then decodes the data to NRZ format for output to the controller.

In the write mode, the device receives NRZ data from the disk controller, encodes it in one of nine different 2,7 RLL hard/soft sectored formats, and then sends the data out to the drive with optional 3T precompensation adjustments.

The device generates and recognizes the following 2,7 address mark formats; ESDI, ESDI noise tolerant, SMD, SMD noise tolerant, ST506(A), hard sector and three variations of ESDI, IBM, & ST506(B) optimized for the DP8466 controller. The address mark format is selected by 4 bits in a control register. A user defined variable-length preamble pattern can be used with any of the address mark modes. The pattern type, 3T or 4T, is set with one control register bit, and the preamble length is defined by the input NRZ data.

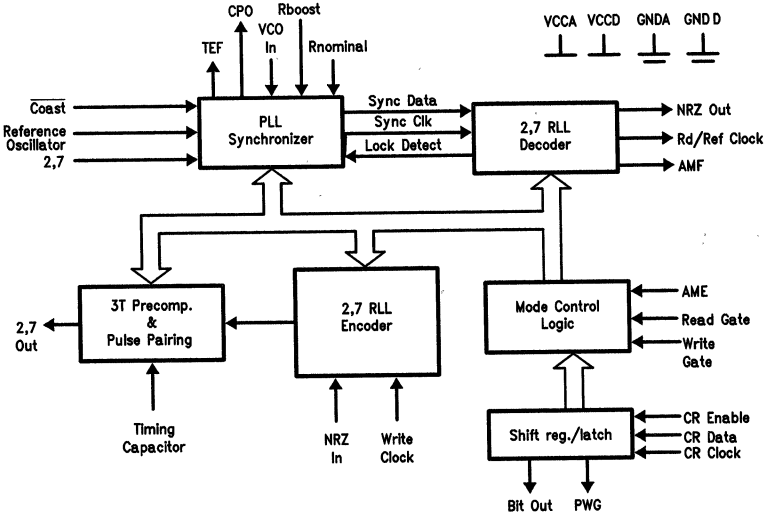
The synchronizer provides a dual gain phase locked loop which offers a high bandwidth mode for preamble lock acquisition and a low bandwidth mode for reading data. Two ports are provided for the PLL filter to enable use of higher order filter designs. The synchronizer has a Zero-Phase-Start feature which helps to minimize acquisition time in both read and write modes. A PHASE COMPARATOR TEST function is also provided for observation of PLL loop dynamics and determination of average media bit shift. The 2,7 OUTPUT pin provides the logical OR of the phase comparator's pump up and down outputs when programmed for Test Mode 1 operation. (Continued)

Features

- NRZ to 2,7 RZ RLL encoding/decoding
- 3T and 4T preamble generation/detection
- 1.5 Mbit/s to 24 Mbit/s data rates
- User specified preamble length
- ESDI, SMD, and ST506 soft sectoring
- Hard sectoring
- Fully integrated dual-gain PLL
- Zero-Phase-Start lock sequence
- Digitally controlled window strobe
- Digital write precompensation
- TTL compatible inputs and outputs
- +5V supply
- Packaging availability:
  — 28-pin Plastic Chip Carrier (PCC)
  — 40-pin TapePak

Block Diagram

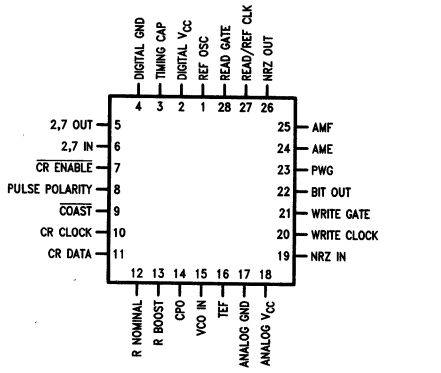
DP8469 Synchronizer/2,7 Endec



TL/F/9386–2

Connection Diagrams

PCC

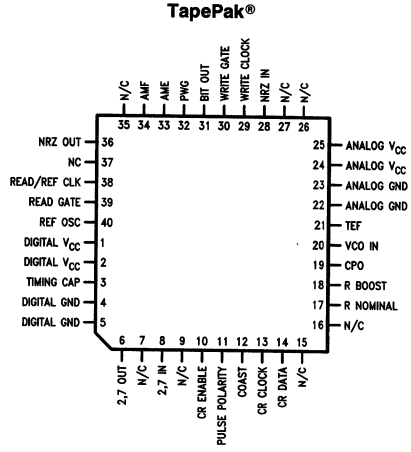


TL/F/9386–34

Top View

Order Number DP8469V
See NS Package Number V28A

TapePak®



TL/F/9386–1

Top View

Order Number DP8469TP
See NS Package Number TP40A

General Description (Continued)

A precise synchronization window is provided on chip using a self-aligned silicon delay line which remains accurate independent of temperature, power supply, external components and IC process variations. A strobe early/late function is provided which allows the synchronization window to be digitally adjusted to allow for error recovery or margin testing. The window can be shifted up to 20% in steps of 1.25% by 5 bits in a control register.

The synchronizer's data rate range is 1.5 Mbit/s to 24 Mbit/s. This range is divided into four operating regions each providing a 2 to 1 span in VCO frequency. Selection of one of the four data rate regions is controlled by two bits in a control register.

The READ/REFERENCE CLOCK provides both a read and write clock source for the controller. In read mode, once READ GATE has gone active and the Zero-Phase-Start sequence has been completed, the READ/REFERENCE CLOCK outputs the VCO divided by two. In the non-read mode, READ/REFERENCE CLOCK outputs REFERENCE OSCILLATOR divided by two. The circuitry incorporates a non-glitching multiplexer to ensure no erroneous clock pulses occur during the switch between input sources.

A digital precompensation feature is provided for write operations to compensate for bit shift due to data crowding on the media. The device will precompensate 3T code which is adjacent to greater than 3T code by selecting 1 of 6 bit shifted steps determined externally on the TC pin with an RC time constant set by the user.

The BIT-OUT output directly follows the logic level programmed in Control Register bit #10. By connecting BIT-OUT to the TC pin through a resistor, it is possible to have the controller select different pre-comp ranges via the control register.

Pin Descriptions

POWER SUPPLIES

ANALOG V_{CC}: Analog positive 5V supply, ±5%.

DIGITAL V_{CC}: Digital positive 5V supply, ±5%.

ANALOG GND: Analog negative supply pin.

DIGITAL GND: Digital negative supply pin.

INPUTS FROM CONTROLLER

NRZ IN (NRZI): NRZI input from the controller. Data is encoded and written to the disk in 2,7 format on the positive edge of WRITE CLOCK. NRZI is held LOW during the Preamble and Address fields, and transitioned HI at the start of data encoding.

Non-ST506 modes: NRZI must remain LOW throughout the address mark field and transition HI for a minimum of two NRZ bits to terminate preamble and start the controller sync byte.

ST506 modes: NRZI must remain LOW through both the address mark and preamble fields, and then transition HI for a minimum of one NRZ bit to start the controller sync byte.

WRITE CLOCK: Clock input from the controller synchronized with the NRZ IN data.

WRITE GATE (WG): A mode control input from the controller which allows the writing of header and data to the disk when active HI and prohibits writing of header or data when LOW.

ADDRESS MARK ENABLE (AME): AME must be held HI while writing an Address Mark. During an ESDI or SMD read operation, the AME pin must be held HI to search for an address mark. Termination of the AME HI level will reset AMF to the LOW state. The AME logic is not relevant during non ESDI and SMD read operations.

Pin Descriptions (Continued)

INPUTS FROM CONTROLLER (Continued)

READ GATE (RG): A mode control input from the disk controller. In ESDI and IBM modes, RG should not be transitioned HI until AMF is active HI. In SMD and ST506 modes, RG is qualified to the synchronizer internally as follows:

ST506: device must recognize 4 consecutive 3T or 4T preamble patterns.

SMD: AMF goes active HI.

In Hard Sector mode, RG should not be transitioned HI until the Index Sector Gap is found. After RG goes HI, the synchronizer locks to the 2,7 INPUT data rate using a Zero Phase Start frequency lock routine. When RG goes LOW, the synchronizer locks to the Reference Oscillator (REG OSC) using a Zero Phase Start frequency lock routine. RG timing is allowed to be fully asynchronous.

OUTPUTS TO CONTROLLER

ADDRESS MARK FOUND (AMF): An active HI output for the controller to indicate the first 2,7 pulse beyond a valid address mark has been found. In the ESDI and SMD modes, AMF remains HI until AME transitions LOW. In the ST506A mode, AMF stays HI until RG is deasserted. In the DP8466 modes, ESDI, IBM and ST506B, AMF returns LOW after the second 2,7 pulse is encountered.

NRZ OUTPUT (NRZO): Decoded output data for the controller that is strobed on the positive transition of READ REF CLK. Control register bit 11 selects either TRI-STATE® or totem pole output. Bit 11 = LOW sets NRZO to active totem pole output, and Bit 11 = HI sets NRZO to TRI-STATE output.

READ REF CLK (R/RCLK): This supplies the controller clock source. In read mode, after the Zero Phase Start sequence is completed, R/RCLK issues the VCO divided by two signal. The NRZO is synchronized with this clock. In the non-read mode, R/RCLK will issue the REF CLK input signal divided by two.

INPUTS/OUTPUTS TO DRIVE

2,7 OUTPUT: Output 2,7 Return-to-Zero (RZ) data for recording onto the storage media. Each positive edge represents a single recorded code bit. The 2,7 OUTPUT active transition edge can be shifted by specific controllable time steps by setting control register bits 7,6,5. Only certain minimum 3T patterns are affected.

2,7 INPUT: Incoming data derived from the storage media, issued from a pulse detector circuit. Each positive edge represents a single recorded bit.

PULSE POLARITY (PP): Input derived from DP8464/8 pulse detector's channel polarity output telling the pulse pairing circuitry which pulse to shift.

EXTERNAL SOURCES

REFERENCE OSCILLATOR (REF OSC): A reference frequency input *required* for DP8469 operation. The signal must be crystal or servo derived (accurate and highly stable), and at a frequency approximately equal to the 2,7 code rate (i.e., twice the NRZ data rate).

$\overline{\text{CR ENABLE}}$ ($\overline{\text{CRE}}$): When active LOW, $\overline{\text{CRE}}$ permits the loading of mode information via CRD and CRC. Data is latched into the part when $\overline{\text{CRE}}$ is transitioned HI. This input is also used to set test mode conditions as described in the Test Mode Operation section.

$\overline{\text{COAST}}$ ($\overline{\text{CST}}$): The control input for a coast function which may be activated when RG is either HI or LOW. When the $\overline{\text{CST}}$ input is LOW, the phase comparator is disabled and held in a cleared state, allowing the VCO to coast regardless of the 2,7 code input or reference oscillator activity. No other circuit functions are disturbed. When the $\overline{\text{CST}}$ is inactive HI, the synchronizer operates normally.

CR CLOCK (CRC): Positive edge triggered clock for the 24-bit control register. This input is also used to set test mode conditions as described in the Test Mode Operation section.

CR DATA (CRD): Data input for the 24 bit control register that selects the strobe window, precompensation and pulse pairing bit shift, data rate range, and address mark modes. This input is also used to set test mode conditions as described in the Test Mode Operation section.

ANALOG SIGNAL PINS

RNOMINAL (R_{NOM}): A resistor is tied from this pin to V_{CC} to set the *nominal* operating current. The current is internally multipled by 2 for charge pump use. This pin is also used to load the test modes as described in the Test Mode Operating section.

RBOOST (R_{BST}): A resistor is tied from this pin to V_{CC} to set the chrage pump *boost* (or adder) current, which is multiplied by 2 internally for use by the charge pump. The R_{BST} resistor is electrically paralleled with the R_{NOM} resistor until either RG is passed to the synchronizer, or preamble lock is acquired. This selection is made with control bit 18;

Bit 18 = HI: forces synchronizer switch to Low Gain on assertion of RG.

Bit 18 = LOW: forces synchronizer switch to Low Gain when preamble lock is acquired.

RBOOST (R_{BST}) (Continued): ST506 operating modes are special in that the switch to Low Gain is forced on the assertion of RG regardless of the state of bit 18. If no boost current is desired, a high value resistor must be tied to this pin to ensure its level is not allowed to drop below V_{IH} = 2V and activate the production test mode circuitry. This pin is also used for the test modes as described in the Test Mode Operating section.

CHARGE PUMP OUT (CPO): The output of the high-speed bi-directional current source switching circuitry of the charge pump. The external, passive PLL filter network is established between this pin, the VCO Input and ground.

VCO IN (VCOI): The high-impedance control voltage input to the voltage controlled oscillator (VCO). The external, passive PLL filter network is established between this pin, CPO pin and ground.

Pin Descriptions (Continued)

ANALOG SIGNAL PINS (Continued)

TIMING EXTRACTOR FILTER (TEF): Connection pin for external, passive components employed to stabilize the delay line timing extraction circuitry.

Note: The delay line accuracy *is not* a function of external component values or tolerances.

OTHER OUTPUTS

RC ADJ: An open collector Bipolar output which can be used to adjust the precompensation or pulse pairing external RC time constants. By connecting a resistor between the RC ADJ pin and the TC pin, a different RC timing constant can be used between precompensation and pulse pairing. RC ADJ is the logical true or complement of WG depending on the state of register bit 8:

Bit 8 = HI: RC ADJ is inverted from WG.

Bit 8 = LOW: RC ADJ follows WG.

BIT OUT: An undedicated open collector Bipolar output whose state is set using bit 10 in the control register. This output can be used for any purpose, including adding extra RC ranges to the precompensation and pulse pairing circuitry. Window strobe adjustments can be performed by connecting a resistor between BIT OUT and the CPO output pin.

Circuit Operation

CONTROL REGISTER OPERATION

The DP8469 is initialized by loading the desired mode selections, such as address mark format and 3T/4T Preamble pattern, via the CR DATA (CRD), CR CLOCK (CRC) and CR ENABLE ($\overline{CRE}$) inputs. Loading is accomplished by taking $\overline{CRE}$ active LOW, and clocking in the mode selection data on the positive going edge of CRC. The modes are latched in when $\overline{CRE}$ is transitioned HI. The selections are indicated in the 24-Bit Control Register section. The test modes are also loaded using CRD, $\overline{CRE}$, CRC as explained in the special Test Mode Operation section.

SYNCHRONIZER OPERATION

In non-read mode, the DP8469 PLL is locked to the REFERENCE OSCILLATOR signal (REF OSC). This permits the VCO to remain at a frequency very close to the media bit-rate while the PLL is "idling" and thus will minimize the frequency step and associated lock time requirement encountered at the initiation of lock to 2,7 INPUT data. When READ GATE is transitioned LOW to terminate the Read mode, a Zero-Phase-Start and frequency acquisition sequence is employed to insure lock. The REF OSC signal is also used during this time to set the time delay of the internal delay line. Note that this requires the REF OSC signal to be present *at all times* at a stable and accurate frequency for proper DP8469 operation.

In non-ST506 modes of operation, after the assertion of READ GATE (fully asynchronous, with no timing requirements), and following the completion of two subsequent VCO cycles, the DP8469 VCO is stopped momentarily. The VCO is then restarted in accurate phase alignment with the second data bit which arrives subsequent to the VCO pause. This minimization of phase misalignment between the 2,7 READ DATA and the VCO (referred to as Zero-Phase-Start or ZPS) significantly reduces the data lock acquisition time.

The DP8469 incorporates a preamble-specific acquisition feature which is employed for all non-ST506 modes of operation where READ GATE is asserted only within a preamble. In these modes, after READ GATE is asserted HI, the device will be forced to lock to the exact 3T or 4T selected preamble frequency. The frequency discriminating action of the PLL provided in these modes produces a lock-in range equivalent to the available VCO operating range and thus eliminates the possibility of fractional-harmonic lock. Windowing (pulse-gate action; see Pulse Gate section) is prevented. (Application Note AN-414 has an explanation of typical false lock modes.)

In the ST506 modes of operation, at the assertion of READ GATE, the 2,7 IN data pattern is first sampled asynchronously and the synchronizer ZPS lock-on sequence is prevented until eight preamble patterns are recognized. The synchronizer only operates Low Bandwidth Gain, and in a phase lock mode (pulse gate action) during the ST506 operation.

In the non-ST506 modes, the user is provided, the option of an elevated PLL bandwidth during preamble acquisition for an extended capture range. An R_{BOOST} pin is provided to allow for an increase in charge pump gain over and above the level set by the $R_{NOMINAL}$ pin. The net current through either $R_{NOMINAL}$ or $R_{BOOST}//R_{NOMINAL}$ is multipled internally by 2 for use by the charge pump. The user should connect a high value resistor to R_{BOOST} if an elevated PLL bandwidth is not desired to ensure the pin does not fall below the 2V test inactive HI logic threshold.

The READ/REFERENCE CLOCK (R/R CLK) issues a waveform derived from the REF OSC input during the non-read mode (i.e., READ GATE inactive). In the read mode, following the assertion of READ GATE, the completion of the ZPS sequence, and in the case of ST506 modes, the recognition of a short 3T or 4T preamble pattern, R/R CLK issues a waveform derived from the VCO signal. Once data lock is achieved in the read mode and the first bit of the controller Byte Sync field is encountered, the NRZ OUT and R/R CLK outputs are held in a fixed, specified timing relationship. The R/R CLK output switches between input sources without glitches.

The DP8469 provides a $\overline{COAST}$ control input which serves to clear the phase comparator and disable charge pump action whenever taken to an active, logical-zero level. This function is made available to allow the PLL to be set to free-

Circuit Operation (Continued)

run, undisturbed, while a detectable defect is being read from the media in a region where re-initiation of the lock procedure is impractical (e.g., data field). External data controller circuitry is responsible for the detection of the defect and issuance of the $\overline{\text{COAST}}$ command. For a more detailed explanation of the synchronizer, and loop filter design, please see the DP8459 datasheet.

ENDEC OPERATION

2,7 Encoder: The data encoding path is responsible for generating an address field, preamble field, and the data field. This allows synchronous generation of preamble and data in all cases, insuring the fastest possible PLL lock during readback. The encoder has two modes of operation, ST506 and non-ST506 mode. The primary difference between these two modes is the placement of the fields:

Preamble Field	Address Field	Data Field

ST-506 Mode (Synchronous Type Address Mark)

Address Field	Preamble Field	Data Field

Non ST-506 Mode (Gap Type Address Mark)

In the ST506 modes, the controller issues a WRITE GATE (WG) command to begin the preamble generation. During the Preamble and Address Mark fields, NRZ IN is blanked. Preamble length is user defined since the ENDEC will continue to generate preamble until Address Mark Enable (AME) is asserted. Assertion of AME terminates the preamble, generates a Phase Sync (for decoding), and begins the N7V address mark. In both ST506 modes, the AME input *must be held high for exactly one Byte* (8 bits). The N7V address mark is one byte in length, does not violate the 2,7 code rules, and cannot be generated by the encoder. Immediately following the completion of the Address Mark, NRZ IN is unblanked, and encoded as data. This data must be the controller's sync byte. If the controller requires more then one byte of AME, then both AME and NRZ IN *must be held LOW* during the second byte to insure that during readback the first non-zero data presented to the controller will be a valid Sync Byte. The Sync Byte must begin with a leading "1", however the user has total freedom of the last 7 bits (1------). The encoder continues to encode the data according to the 2,7 code rules until WG is deasserted.

In non-ST506 modes, the controller issues WG to begin the header generation. Normally AME is also issued at the same time. If there is a delay between the assertion of WG and AME, the encoder will begin generating a preamble pattern. Assertion of AME generates the address gap. ESDI and SMD address marks require 3 bytes of AME while the IBM mark only requires 2 bytes of AME. Immediately upon the deassertion of AME, the encoder will begin generating the preamble field. NRZ IN is blanked while AME is asserted. The first non-zero NRZ data following the deassertion of AME *must be the controller's Sync Byte* as any NRZ IN data presented to the encoder after deassertion of AME terminates the preamble, and is encoded. The Sync Byte restrictions are as follows:

3T: 1-------

4T: 11------

For 3T preamble, the Customer has total freedom of the last 7 bits of the Sync Byte, however in the 4T preamble, the Customer has total freedom of only the last 6 bits.

NRZ IN data is internally blanked while AME is asserted as the DP8469 generates its own address mark data depending upon the type of address mark selected in control register bits 15 to 12. In the ST506 case, NRZ data presented to the DP8469 *immediately after* deassertion of AME *will* be encoded as data, while in the non-ST506 modes, the encoder will return to preamble generation *until the first non-zero* NRZ data following deassertion of AME. The preamble pattern is selected in control register bit 9; HIGH for 3T and LOW for 4T. Once the pattern is selected, it is transparent to the user.

2,7 Decoder: The data readback path is responsible for detecting the address field, preamble field, and finally the data field. The controller issues an active READ GATE (RG) to initiate clock synchronization and 2,7 decoding.

In ST506 mode, the controller first issues RG for the detection of the preamble field. The DP8469 employs a two phase preamble prequalifier on the internal RG. The prequalifier must first find several bytes of valid preamble pattern before it passes RG to the synchronizer and enables the standard preamble detector. In the event there is enough valid looking data to qualify as a preamble, the synchronizer is switched into phase-only low gain mode on the assertion of RG to guarantee that it can pass through any subsequent Write Splice without problems. The synchronizer employs a Zero Phase Start circuit to minimize its lock time.

Once preamble has been located (thirty-one 3T patterns or fifteen 4T patterns) the decoder begins searching for the N7V address mark. Phase-sync and address mark detection are accomplished at the same time, and the decoder then unblanks the NRZ OUT at the start of Controller's Sync Byte.

The non-ST506 modes (commonly called "Gap Type") breakdown into two groups:

a) ESDI and IBM modes where the controller does not assert RG until after AMF signifies the start of the Preamble.

b) SMD mode where the controller asserts RG prior to AMF, and the ENDEC is responsible for blocking RG to the synchronizer until the Preamble field has been found.

In both cases, the address mark precedes the preamble field. The controller instructs the DP8469 to search for the address mark, a 2 NRZ byte gap, transitionless ESDI and SMD gaps and an IBM gap with 3 specific transitions. Once the gap has been located, the AMF output signals the controller, and the controller responds with assertion of RG in ESDI and IBM. In the SMD mode, RG is internally qualified with AMF, providing the same function.

Once RG has been passed to the synchronizer, the same thirty-one 3T or fifteen 4T preamble pattern requirements must be met before the decoder can look for the Phase Sync, and unblank. The first non-zero NRZ OUT data is the controller's Sync Byte.

Circuit Operation (Continued)

Both the encoder and decoder follow the encoding rules as shown in the table below:

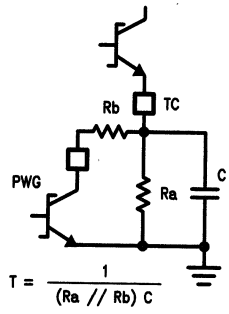
IBM 2,7 Conversion Table

NRZ				2,7 Code						
	0	0	0			0	0	0	1	0	0
		1	0					0	1	0	0
	0	1	0			1	0	0	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0
		1	1					1	0	0	0
	0	1	1			0	0	1	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0

2 = Minimum # of Zeros between adjacent Ones
7 = Maximum # of Zeros between adjacent Ones
1 = NRZ bits for relative conversion ratio
2 = Code bits for relative conversion
3 = # of different length code words

Precompensation

The Precomp circuitry uses the same basic delay-line technique to provide controllable time-delay steps. The user applies the necessary external RC components to the TC pin to provide the desired time step sizes. By using the BIT OUT and PWR outputs, different RC values can be used for different circumstances ... Programming Bit 8 = LOW sets the PWG output to follow WRITE GATE, while programming Bit 8 = HI sets PWG to the logical inverse of WRITE GATE. This allows complete freedom in setting the precomp time constants independently for different Write channel anomolies such as inner vs outer track recording densities.



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Bit-crowding on the disk results in a maximum frequency pattern (3T) timing error to the data written on the disk. Whenever the 3T pattern is adjacent to a non-3T pattern, the two 3T bits are pushed apart, resulting in a time skew during readback. The precompensation feature allows the user to adjust the 3T pattern on a cycle-by-cycle basis to correct for this problem.

Precompensation Bit Patterns

Bit t−3	Bit t−2	Bit t−1	Target Bit t	Bit t+1	Bit t+2	Bit t+3
0	0	0	No Shift	0	0	0
1	0	0	No Shift	0	0	1
1	0	0	Shift Early	0	0	0
0	0	0	Shift Late	0	0	1

Test Mode Operation

The DP8469 provides 7 special test modes. With the exception of the Phase Comparator Test (PCT), SYNC DATA and SYNC CLK, these special test modes are used for production testing. The PCT data is the logical OR'ing between charge Pump Up and charge Pump Down, and can be used to examine the locking action of the PLL. The SYNC DATA and SYNC CLK outputs allow window strobe measurements. All together, they will allow the user to fine tune the application to insure minimum jitter during readback. The PCT function is present on the AMF output in test mode 1 (load 001, MSB first). SYNC DATA and SYNC CLK are present in test mode 7 (load 111, MSB first) on the READ/REF CLK and OUTPUT 2,7 outputs respectively.

The test modes are set by a 3 bit test register that is accessed via the R_{BOOST} and $R_{NOMINAL}$ inputs. In an application, both R_{BOOST} and $R_{NOMINAL}$ are held above the 2V threshold clearing the test register to mode 0, and allowing both HI and LOW gain PLL action. This insures that the device will always power-up in the normal operating mode. By pulling R_{BOOST} below the 2V threshold, the test register can now accept 3 bits of data that will decode to one of seven test modes (the eighth mode, 000, is normal operation). The $R_{NOMINAL}$ input is used to select between loading the 24 bit control register and the 3 bit test register; $R_{NOMINAL}$ = HI sends the data to the 24 bit register while $R_{NOMINAL}$ = LOW sends the data to the 3 bit test register. The test register is then loaded using $\overline{CRE}$, CRC, and CRD. After loading the test register, first return $\overline{CRE}$ = HI *to protect the data in both the Control Register, as well as the data in the Test Register.* It is required to set $\overline{CRE}$ = HI *before changing the state of any other control input* (including both $R_{NOMINAL}$ and R_{BOOST}) in order to prevent any internal switching from generating false clocks and changing the state of any register data. Next, return $R_{NOMINAL}$ HI to allow normal synchronizer operation. Maintain R_{BOOST} LOW to preserve the test mode. This combination will only allow low gain PLL action during testing. CRD and CRC must also be returned LOW, and held there during testing as they are used as special testing inputs.

The action of pulling $R_{NOMINAL}$ low disables the charge pump, and drives the VCO to the lower clamp limit. For any test where the PLL loop needs to run, such as window strobe tests, the test mode must be loaded before the loop is locked. First, load the test register and return $\overline{CRE}$ HI, and then $R_{NOMINAL}$ HI. Then reload the control register, and return $\overline{CRE}$ HI. Finally, exercise the device starting with RG deasserted, and running the device through the complete Read cycle. Note that for the device to remain in test mode, R_{BOOST} must be held low, and this eliminates the high gain mode of operation for the synchronizer. To observe the synchronizer in a high gain mode, replace $R_{NOMINAL}$ with a resistor equivalent to the parallel combination of $R_{NOMINAL}$ and $R_{NOMINAL}$. Do not exceed the 1 mA maximum total input current specification for the $R_{NOMINAL}$ pin.

DP8469 24 Bit Control Register

Control Register is Loaded MSB (Bit 23) First, and LSB (Bit 0) Last.

23 MSB 22 21 20 19	18	17 16	15 14 13 12	11	10	9	8	7 6 5	4	3	2 1 0 LSB
Window Strobe	Gain Control	VCO Frequency Range Select	Address Mark Mode Select	NRZ Hi-Z Enable	Bit Out Hi	3T Preamble	RC Adjust	Precomp Step Select	Invert 2,7 Out	Edge Polarity	Pulse Pairing Step Select

Pulse Pairing Delay Steps

3*	Pulse Pairing Early/Late 2	1	0	Delay Step % Bit Shift
X	0	0	0	Bypassed
X	0	0	1	0.0
0 / 1	0	1	0	± 2.5*
0 / 1	0	1	1	± 5.0*
0 / 1	1	0	0	± 7.5*
0 / 1	1	0	1	±10.0*
0 / 1	1	1	0	±12.5*
0 / 1	1	1	1	±15.0*

*Bit 3 selects which flux change from the Pulse Detector is Pulse Pairing Corrected.

Precomp Delay Steps

Precomp Early/Late 2	1	0	Delay Step % Bit Shift
0	0	0	Bypassed
0	0	1	0.0
0	1	0	± 2.5*
0	1	1	± 5.0*
1	0	0	± 7.5*
1	0	1	±10.0*
1	1	0	±12.5*
1	1	1	±15.0*

Control Register Bit Definitions for Bits 4, 8, 9, 10, 11, 18

Bit 4	2,7 Output	0	True
		1	Inverted
Bit 8	RC ADJ Follows	0	$\overline{\text{WRT GATE}}$
		1	WRT GATE
Bit 9	3T/4T Preamble	0	4T
		1	3T
Bit 10	BIT OUT	0	Active LOW
		1	Inactive HI
Bit 11	NRZ OUT	0	Totem Pole
		1	TRI-STATE
Bit 12	PLL Switch to Low Gain	0	READ GATE
		1	LOCK DETECT

Control Register # / Address Mark Mode

15	14	13	12	Address Mark Mode
0	0	0	0	ESDI
0	0	0	1	SMD
0	0	1	0	ESDI*
0	0	1	1	N/A
0	1	0	0	ST506A
0	1	0	1	ST506B
0	1	1	0	HARD
0	1	1	1	IBM*
1	0	0	0	ESDI NT
1	0	0	0	SMD NT

*DP8466 Compatible

VCO Freq Range

Bits 15	14	Freq Range (Mbits/sec)
0	0	1.5–3
0	1	3–6
1	0	6–12
1	1	12–24

Control Register # 23	22	21	20	19	Strobe Word	Typical Window Strobe
0	1	1	1	1	−15	$-0.270\times T_{vco}$
0	1	1	1	0	−14	$-0.252\times T_{vco}$
0	1	1	0	1	−13	$-0.234\times T_{vco}$
0	1	1	0	0	−12	$-0.216\times T_{vco}$
0	1	0	1	1	−11	$-0.198\times T_{vco}$
0	1	0	1	0	−10	$-0.180\times T_{vco}$
0	1	0	0	1	−9	$-0.162\times T_{vco}$
0	1	0	0	0	−8	$-0.144\times T_{vco}$
0	0	1	1	1	−7	$-0.126\times T_{vco}$
0	0	1	1	0	−6	$-0.108\times T_{vco}$
0	0	1	0	1	−5	$-0.090\times T_{vco}$
0	0	1	0	0	−4	$-0.072\times T_{vco}$
0	0	0	1	1	−3	$-0.054\times T_{vco}$
0	0	0	1	0	−2	$-0.036\times T_{vco}$
0	0	0	0	1	−1	$-0.018\times T_{vco}$
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	1	1	$0.018\times T_{vco}$
1	0	0	1	0	2	$0.036\times T_{vco}$
1	0	0	1	1	3	$0.054\times T_{vco}$
1	0	1	0	0	4	$0.072\times T_{vco}$
1	0	1	0	1	5	$0.090\times T_{vco}$
1	0	1	1	0	6	$0.108\times T_{vco}$
1	0	1	1	1	7	$0.126\times T_{vco}$
1	1	0	0	0	8	$0.144\times T_{vco}$
1	1	0	0	1	9	$0.162\times T_{vco}$
1	1	0	1	0	10	$0.180\times T_{vco}$
1	1	0	1	1	11	$0.198\times T_{vco}$
1	1	1	0	0	12	$0.216\times T_{vco}$
1	1	1	0	1	13	$0.234\times T_{vco}$
1	1	1	1	0	14	$0.252\times T_{vco}$
1	1	1	1	1	15	$0.270\times T_{vco}$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	−0.5V to +7.0V
Inputs (Note 1)	
TTL	−0.5V to +7.0V
CMOS	−0.5V to +5.5V
Outputs (Note 1)	
TTL	−0.5V to +7.0V
CMOS	−0.5V to +5.5V
Input Current Maximum ($R_{NOMINAL}$, R_{BOOST}, CPO, VCOI, TEF)	±2 mA
Storage Temperature	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
ESD Susceptibility	1500V

Recommended Operating Conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{CC}	Supply Voltage			4.75	5.00	5.25	V
T_A	Ambient Temperature			0	25	70	°C
V_{IH}	High Logic Level Input Voltage			2.0			V
V_{IL}	Low Logic Level Input Voltage					0.8	V
I_{OH}	High Logic Level Output Current	I_{OH1}	2,7 Output			−400	μA
		I_{OH2}	AMF, NRZ OUT, RD/REF CLK			−2.0	mA
		I_{OH3}	AMF, NRZ OUT, RD/REF CLK			−20	μA
I_{OL}	Low Logic Level Output Current	I_{OL1}	2,7 Output			20	mA
		I_{OL2}	RC ADJ, BITOUT			8.0	mA
			AMF, NRZ OUT, RD/REF CLK			4.0	mA
		I_{OL3}	AMF, NRZ OUT, RD/REF CLK			20	μA
$I_{RC\ ADJ}$	Pulse-Pairing/Pre-Compensation Maximum External Load Current			0.0		−16	mA
f_{NRZ}	Operating Data Rate Range			1.5		24	Mb/s
t_{mpwr}	Minimum Pulse Width of REF CLK, HIGH or LOW			10			ns
t_{mpwi}	Minimum Pulse Width of INPUT 2,7, HIGH			20			ns
t_{mpww}	Minimum Pulse Width of WRT CLK, HIGH or LOW			20			ns
t_{mpwcc}	Minimum Pulse Width of CRC, HIGH or LOW			40			ns
t_{mpwc}	CONTROL REGISTER CLOCK Minimum Pulse Width HIGH or LOW (Note 2)			40			ns
t_{scec}	CONTROL REGISTER CLOCK Setup-Time with respect to CRC (Note 2)			80			ns
t_{hcec}	CONTROL REGISTER ENABLE Hold-Time with respect to CRC (Note 2)			80			ns
t_{scdc}	CONTROL REGISTER DATA Setup-Time with respect to CRC (Note 2)			40			ns
t_{hcdc}	CONTROL REGISTER DATA Hold-Time with respect to CRC (Note 2)			40			ns
I_{CPIN}	Combined R_{NOM} and R_{BOOST} Input Current					1000	μA

Note 1: Bipolar Inputs: REF CLK, $\overline{COAST}$, R_{NOM}, R_{BOOST}
Bipolar Outputs: TC, 2,7 OUT, RC ADJ, BITOUT
CMOS Inputs: 2,7 IN, $\overline{CRE}$, CRD, CRC, PULSE POL, NRZ IN, WRT CLK, WRT GATE, AME, READ GATE
CMOS Outputs: AMF, NRZ OUT, RD/REF CLK
Analog Inputs: TEF, CPO, VCO IN

Note 2: Parameter guaranteed by correlation to characterization data. No outgoing test performed.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage (All Inputs)	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH1}	High Level Output Voltage	V_{CC} = Min, I_{OH} = I_{OH1}	V_{CC} − 2V	V_{CC} − 1.6V		V
		V_{CC} = Min, I_{OH} = I_{OH2}	3.5			V
		V_{CC} = Min, I_{OH} = I_{OH3}	V_{CC} − 0.1V			V
V_{OL1}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = I_{OL1}			0.5	V
		V_{CC} = Min, I_{OL} = I_{OL2}			0.4	V
		V_{CC} = Min, I_{OL} = I_{OL3}			0.1	V
I_{OZ}	Maximum TRI-STATE Leakage (Note 1)	V_{CC} = Max, 0.4V ≤ V_O ≤ 2.7V			±2.0	μA
I_{CEX}	Open-Collector Leakage (Note 2)	V_{CC} = Max, V_O = Max			−100	μA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V			−200	μA
I_{IN}	Maximum Input Current (Note 4)	V_{CC} = Max, V_{IN} = V_{CC} or GND	−1		+1	μA
I_O (Note 5)	Output Drive Current OUTPUT 2,7	V_{CC} = Max, V = 2.125V	−12		−110	mA
	TC Pin (Note 6)	V_{CC} = Max, V = 2.125V	−36			mA
I_{CPO}	Charge Pump Output Current (K1)	100 ≤ I_{RP} ≤ 1000 (Note 7)	1.7 I_{RP}	2.0 I_{RP}	2.5 I_{RP}	μA
$I_{CPO-OFF}$	Charge Pump Output Inactive Current	100 ≤ I_{RP} ≤ 1000 (Note 7)	−0.85		+0.85	μA
I_{VCOI}	VCOI Input Leakage Current	VCOI Voltage 1.5V	−0.25		+0.25	μA
V_{RNOM}	Voltage Across R-NOM Resistor	1.2 kΩ ≤ R_{NOM} ≤ 12 kΩ	Typ − 18%	0.26 V_{CC}	Typ + 18%	V
V_{RBST}	Voltage Across R-BOOST Resistor	1.2 kΩ ≤ R_{BOOST} ≤ 12 kΩ	Typ − 18%	0.26 V_{CC}	Typ + 18%	V
I_{CC1}	Supply Current, Nominal Strobe	V_{CC} = Max (Note 8)			190	mA
I_{CC2}	Supply Current, Early Strobe	V_{CC} = Max, (Note 9)			TBD	mA

Note 1: Applies to the TRI-STATE output NRZ OUT with CTRL BIT 11 set HI, and WRT GATE HI.

Note 2: Applies to the Bipolar outputs: RC ADJ, BITOUT.

Note 3: Applies to the Bipolar inputs: REF CLK, $\overline{\text{COAST}}$, R_{NOM}, R_{BOOST}.

Note 4: Applies to the CMOS inputs: INPUT 2,7, $\overline{\text{CRE}}$, CRD, CRC, PULSE POL, NRZ IN, WRT CLK, WRT GATE, AME, READ GATE.

Note 5: This represents approximately one-half of the true short-circuit output current, I.

Note 6: This only applies to the TC Open Emitter output. Do not exceed 100 mA for more than 0.1 sec.

Note 7: I_{RP} = I_{NOM} + I_{BOOST}

Note 8: I_{CC1} is measured with the window strobe set at nominal timing (Register Bits 23 through 19 = 0,0,0,0,0); VCO operating at the maximum allowed frequency within any given range selection.

Note 9: I_{CC2} is measured with the window strobe set to the maximum early timing (Register Bits 23 through 19 = 0,1,1,1,1); VCO operating at the maximum allowed frequency within any given range selection.

External Component Selection

Symbol	Parameter	Min	Typ	Max	Units
R_{NOM}	Charge Pump Nominal Operating Current Setting Resistor (Note 1)	1.2		12	kΩ
R_{BOOST}	Charge Pump Boost Current Setting Resistor (Note 1)	1.2		∞	kΩ
C_{NOM}	R_{NOM} Bypass Capacitor (Note 2)	0.01			μF
C_{BOOST}	R_{BOOST} Bypass Capacitor (Note 2)	0.01			μF
R_{TC}	Pre-Comp/Pulse Pairing Timing Resistor (Note 3)	0.33		10	kΩ
C_{TC}	Pre-Comp/Pulse Pairing Timing Capacitor (Note 3)	33		10000	pF
$R_{RC\ ADJ}$	Secondary Pre-Comp/Pulse Pairing Timing Resistor (Note 4)	0.33		10	kΩ
$R_{BIT\ OUT}$	Secondary Pre-Comp/Pulse Pairing Timing Resistor (Note 4)	0.33		10	kΩ

Note 1: The minimum allowed value for the parallel combination of R_{NOM} and R_{BOOST} is 1.2 kΩ.

Note 2: C_{NOM} and C_{BOOST} should be high quality, high frequency type.

Note 3: R_{TC} and C_{TC} are both used to establish Pulse-Pairing and Pre-Comp timing on the TC pin.

Note 4: R_{RC} ADJ and R_{BIT} OUT modify the external timing on the TC pin for Read vs Write and inner track adjustability.

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{STOP}	READ/REF CLK Positive Transitions after READ GATE until Data Lock ZPS Sequence Begins (VCO Freezes) (Notes 1, 2)		2 (Note 4)	3 (Note 4)	—
$t_{RESTART}$	Positive 2,7 INPUT Transitions following VCO Freeze until the VCO Restarts (Note 2)		2	3	—
$t_{READ\ ABORT}$	Number of REF CLOCK Cycles following READ GATE Deactivation until REF CLOCK Lock ZPS Sequence begins (Note 2)			4	—
t_T	Window Truncation (Half Window Loss); 10 and 20 Mbit/s at Strobe Position M = −2 (Note 3)		4% × T_{VCO}		ns
ϕ Linearity	Phase Range for Charge Pump Linearity (wrt VCO) (Note 2)		±π		Radians
K_{VCO}	VCO Gain Constant (Note 6)	1.0 ω_o	1.2 ω_o	1.7 ω_o	rad/sec V
$f_{MAX\ VCO}$	VCO Maximum Frequency; Control Bits 17,16 = 11	70			MHz
t_{ZPSR}	Zero Phase Start Trigger Bit Targeting Accuracy, READ GATE Activation (READ) (Note 5)		2		ns
$\Delta f_{VCO}/f_{RFC}$	Automatic f_{VCO} Range Limiting (Note 2)		50		%
t_{RRCH}	RD/REF CLK Rest Period at Assertion or Deassertion of READ GATE (Note 2)	½		3	T_{VCO}
Encoder Delay	Serial Delay Time in REF CLK Cycles + ns Delay (Note 7)			10 + 100	Cyc + ns
Decoder Delay	Serial Delay Time in REF CLK Cycles + ns Delay			8 + 100	Cyc + ns

AC Electrical Characteristics (Continued)

Symbol	Parameter		Min	Typ	Max	Units
t_{plh} AMF Assertion Time	ST506A and B; After REF CLK following Address Detection (ESDI, SMD, and IBM Gap Type Address are Asynchronous)		50		100	ns
t_{phl} AMF Deassertion Time	ESDI and SMD (Spec & Noise Tolerant); Falling Edge of AME		50		100	ns
	DP8466 Compatible (ESDI and IBM); 2nd Input 2,7 Pulse		50		100	ns
	ST506A: 2nd Input 2,7 Pulse		50		100	ns
	ST506B; Next REF CLK Positive Edge after Falling RD GATE		50		100	ns
t_{mpw}	REF CLK Minimum Pulse Width t_{mpwr+} t_{mpwr-}		5			ns
	INPUT 2,7 Minimum Input Pulse Width t_{mpwi+}		15			ns
	WRT CLK Minimum Input Pulse Widths t_{mpww+} t_{mpww-}		10			ns
$t_{s1/0}$ $t_{h1/0}$	REF CLK Setup and Hold Times to WRT CLK				10	ns
	WRT CLK Setup and Hold Times to AME, NRZ IN, WRT GATE, READ GATE				20	ns
t_{plh}, t_{phl}	Propagation Delay from REF CLK to OUTPUT 2,7				100	ns
$t_{rfc-rrc}$	Propagation Delay from REF CLOCK to RD/REF CLK, READ GATE LOW				50	ns
$t_{skw\pm}$	RD/REF CLK Negative Edge to NRZ OUTPUT Transition				±5	ns
L_{PDT}	Length of Valid Preamble Pattern Required for Internal PREAMBLE DETECTED (Note 2)	3T Preamble	31	32	33	2,7 Input Pulses
		4T Preamble	15	16	17	
t_{Str}	Window Strobe Time Step (M = Hex Value of Bits 22–19 in CONTROL REGISTER; Bit 23 = Sign Bit			M × (1.8%) × T_{RFC}		ns

Note 1: ST506 and SMD modes utilize a Preamble Prequalification routine to guarantee that the synchronizer only locks to data during a valid Preamble Field. This adds a prequalification time to the T_{STOP} time parameters as follows:
ST506: Adds 8 full preamble fields PRIOR to the T_{STOP} parameter
SMD: Adds the time it takes to locate a valid Address Mark, and output a valid AMF

Note 2: Limits are guaranteed by design or correlation to characterization data; no outing testing is performed.

Note 3: *The preliminary DP8469 static window specification, IT, applies only to the factory-tested data rates of 10 Mb/s (Control Bits 17,16 = 01) and 20 Mb/s (17,16 = 10), with the component values as listed for each corresponding data rate in Figures 7* and *12*, test configuration as shown in *Figure 24*, test procedure as shown in *Figure 25*, and strobe word M = −2. Significant variation in IT due to the use of other filters and data rates is not expected.

Note 4: t_{ZPSR} (ZPS Read) gauges the accuracy with which the ZPS circuitry aligns the VCO to the triggering 2,7 INPUT bit internally (i.e., initial phase step) at the completion of a ZPS operation following READ GATE assertion.

Note 5: $I_{IN} = V_{CC}/(4 \times R_{IN})$. $R_{IN} = R_{NOM}$ (HGD High) or $R_{NOM} \| R_{BOOST}$ (HGD Low).

Note 6: Specification for 25°C only. Temperature coefficient = −0.4%/°C.

Note 7: Encoder Serial Delay specified for Pre-Comp set to Bypass Mode (bits 2,1,0 = 000). Non-Bypass Pre-Comp adds 5 REF CLK cycles plus 50 ns.

DP8469 Loop Filter Component Values

Preamble Type	10 Mbit/Sec		20 Mbit/Sec		Units
	3T	4T	3T	4T	
Ref Clk Frequency	20	20	40	40	MHz
NRZ Data Rate	10	10	20	20	Mbit/s
Sync Field Frequency	20	20	40	40	MHz
ζ Min	20	20	40	40	None
ζ Max	20	20	40	40	None
ζ Sync	20	20	40	40	None
Sync Field Frequency	6.7	5	13.3	10	MHz
ω Sync	20	20	40	40	Krad/s
C1 (Main Loop)	0.018	0.018	0.0082	0.082	μF
R1 (Main Loop)	150	150	150	150	Ω
C2 (Main Loop)	510	510	200	200	μF
CT1 (TEF)	0.056	0.056	0.0027	0.027	μF
RT1 (TEF)	68	68	68	68	Ω
TEF Settling Time	9.6	9.6	4.6	4.6	μs

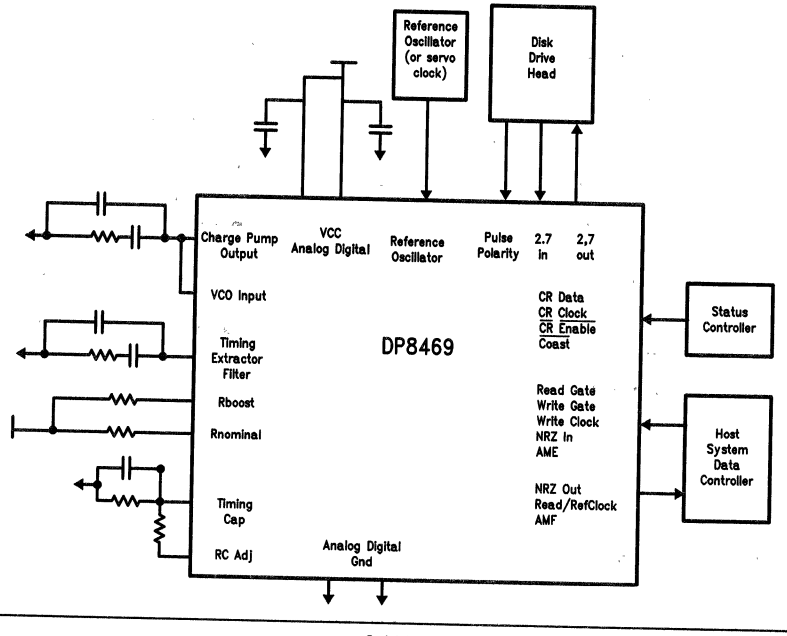
Loop Filter Component Values

Preamble Sync natural frequency has been chosen to yield phase error $\leq$ 0.063 radians (i.e., 1% $\times$ 2π) at sync field end, given a 1% frequency step at READ GATE assertion. $R_{NOM} = R_{BOOST} = 2.4k$ for all loop filter selections. These values apply for Bit 18 = HI, device switches to LOW Gain on assertion of READ GATE.

The TEF settling times are given which indicate time required for the DP8469 to accommodate a change of Strobe setting from nominal selection to either extreme (early/late), or vice versa, to within approximately 1% of final value.

The values listed in the Loop Filter Component Values table are the approximate filter values that are used for Static Window Truncation testing. These values represent a simple solution, yielding only average circuit behavior. Please see National Semiconductor's DP8459 datasheet for a more thorough discussion on loop filter component selection.

Application Diagram



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Encoder Serial Delay Times

Encoder Delay Time Parameter Definitions

t_{es} = Encoder Start time from WRT GATE

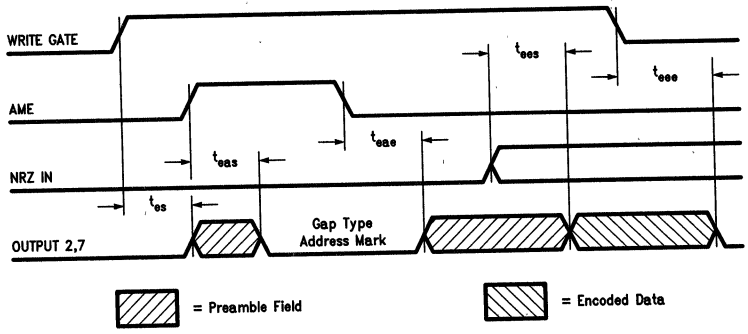
t_{eas} = Encoder Address Mark Start time from assertion of AME

t_{eae} = Encoder Address Mark End time from deassertion of AME

t_{ees} = Encoder Encyrption Start time from first NRZ IN bit

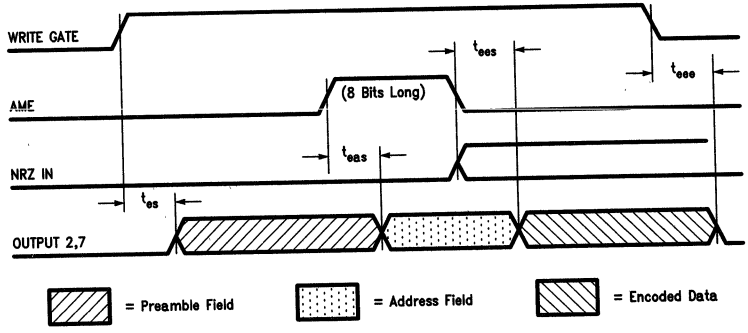
t_{eee} = Encoder Encryption End time from deassertion of WRT GATE

ESDI/SMD/IBM Modes (Gap Type Address Marks)



TL/F/9386–15

ST506A and B Modes (Synchronous Address Marks)



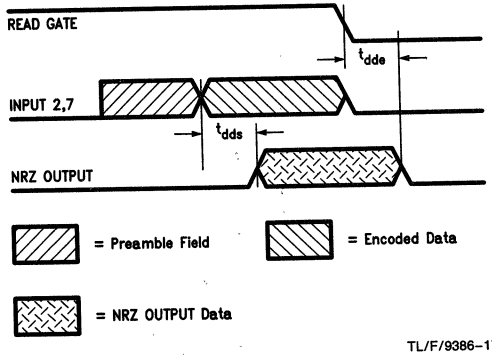
TL/F/9386–16

Decoder Serial Delay Times

Decoder Delay Time Parameter Definitions

t_{dds} = Decoder Decryption Start time from INPUT 2,7 data

t_{dde} = Decoder Decryption End Time from deassertion of READ GATE

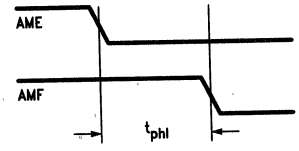


TL/F/9386–17

This parameter defines the time delay for a specific INPUT 2,7 pattern to enter the device, and its resulting NRZ output to be present at the NRZ OUTPUT pin.

AMF Assertion Delay Times by Mode

ESDI/SMD Spec and Noise Tolerant Modes

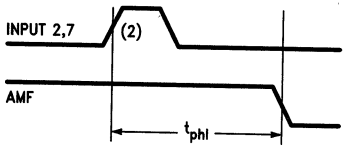


TL/F/9386–18

AMF deasserts on the FALLING edge of READ GATE.

AMF Assertion Delay Times by Mode (Continued)

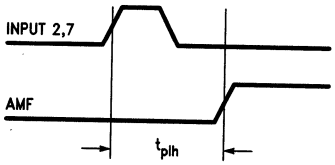
DP8466 Compatible Modes (ESDI and IBM)



TL/F/9386–19

AMF deasserts on the SECOND INPUT 2,7 pulse after assertion

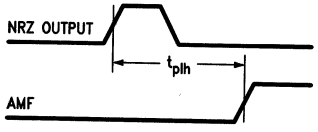
IBM and All ESDI/SMD Modes



TL/F/9386–20

AMF asserts on the FIRST INPUT 2,7 pulse after valid Address Mark

ST506 A and B Modes

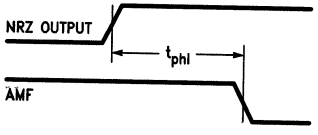


TL/F/9386–22

AMF asserts on the FIRST NRZ OUTPUT pulse after valid Address Mark

ESDI/SMD Spec and Noise Tolerent Modes

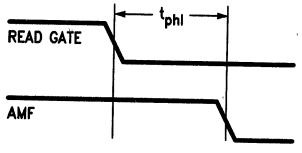
ST506A Mode



TL/F/9386–21

AMF deasserts on the SECOND NRZ OUTPUT pulse after assertion.

ST506B Mode

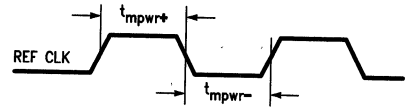


TL/F/9386–23

AMF deasserts on the FALLING edge of READ GATE.

Input Minimum Pulse Widths

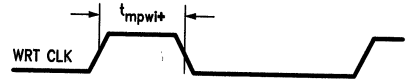
REF CLK Min Pulse Widths



TL/F/9386–24

REF CLK requires minimum input positive and negative pulse width times; including both mpw+ and t_{mpw-}

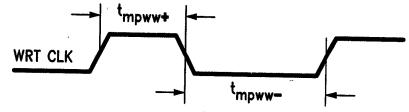
Input 2,7 Min Pulse Widths



TL/F/9386–26

INPUT 2,7 requires a minimum positive pulse width: t_{mpwi+}; there is no minimum negative pulse width spec.

WRT CLK Minimum Pulse Widths

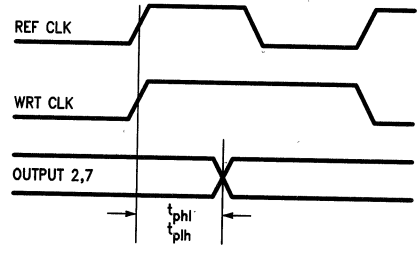


TL/F/9386–27

WRT CLK Input Minimum Positive and Negative Pulse Widths, t_{mpww+} and t_{mpww-}.

Output Propagation Delay Times

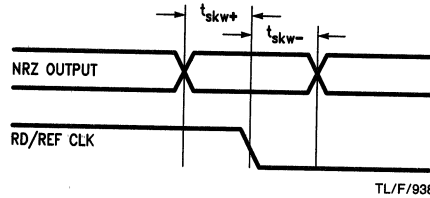
REF CLK to OUTPUT 2,7 Propagation Delay Time



TL/F/9386–25

REF CLK to OUTPUT 2,7 for t_{plh} and t_{phl}. Delay time is specified in both REF CLK cycles and ns of delay. WRT CLK edges coincident with REF CLK.

NRZ OUTPUT vs RD/REF CLK T_{skew} for all Read Modes

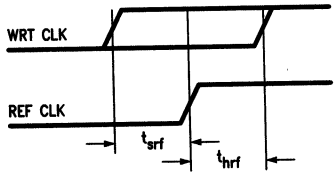


TL/F/9386–28

T_{skw+} defines data changing prior to the clock.
T_{skw-} defines data changing after the clock.

Input Setup and Hold Times

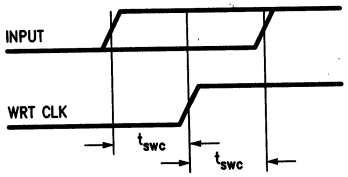
REF CLK Setup and Hold Times



TL/F/9386–29

Setup and Hold Times (t_{srf} and t_{hrf}) from REF CLK to WRT CLK.

WRT CLK Setup and Hold Times NRZ IN, AME, WRT GATE, READ GATE

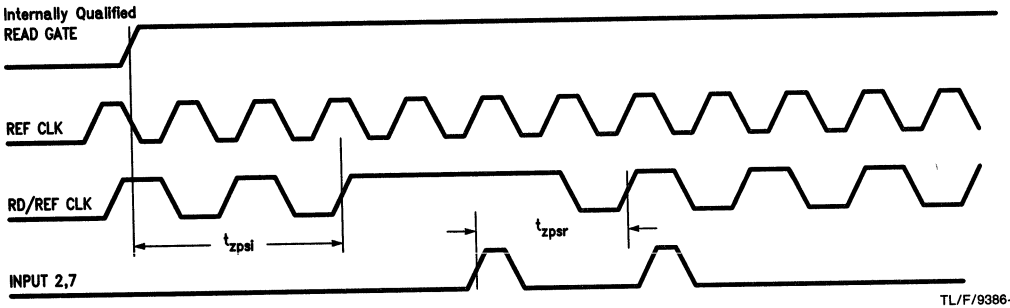


TL/F/9386–30

Setup and Hold Times (t_{swc} and t_{swc}) for the four inputs: AME, WG, RG and NRZ IN.

Zero Phase Start Timing Sequence

ZPS Stop and Restart Delay Time



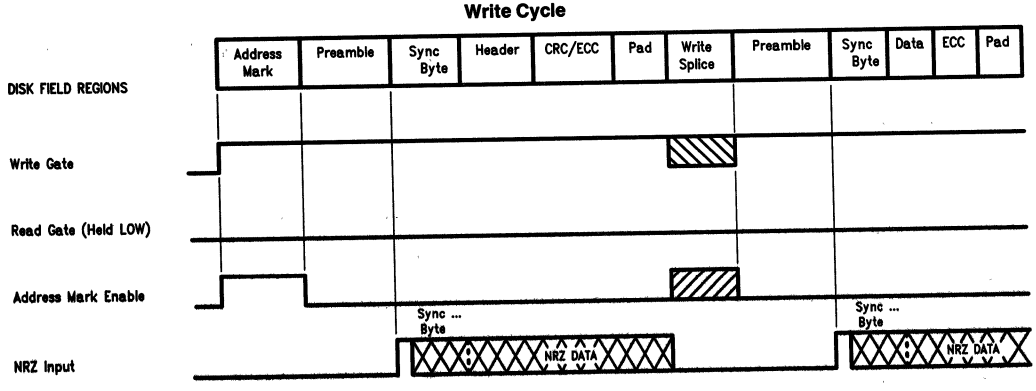
TL/F/9386–31

ZPS Delay Time measures the number of REF CLK cycles that pass from the time READ GATE is passed to the Synchronizer, until Zero Phase Start interrupts the VCO and stops RD/REF CLK. READ GATE is internally qualified in all SMD and ST506 modes to prevent the Synchronizer from attempting to lock when there is no data present (outside the Preamble Field). The basic t_{zpsi} and t_{zpsr} delay times are listed for the ESDI and IBM modes, while the SMD and ST506 modes have prequalifier adders. Delay times t_{zpsi} measures the time to interrupt the VCO, and t_{dzpsr} measure the time to Restart the VCO.

Address Mode	RG Qualified On:	t_{dzpsi} (in REF CLK) Cycles)	t_{dzpsr}
All ESDI Modes	N/A	≤3	≤ 4 after Falling RG
All SMD Modes	AMF Assertion	≤3 + AMF Detection	≤ 4 after Falling RG
All ST506 Modes	Preamble	≤3 + 12 Preamble Patterns	≤ 4 after Falling RG

ESDI (Std and Nt) MODE Control Waveforms

Write Cycle

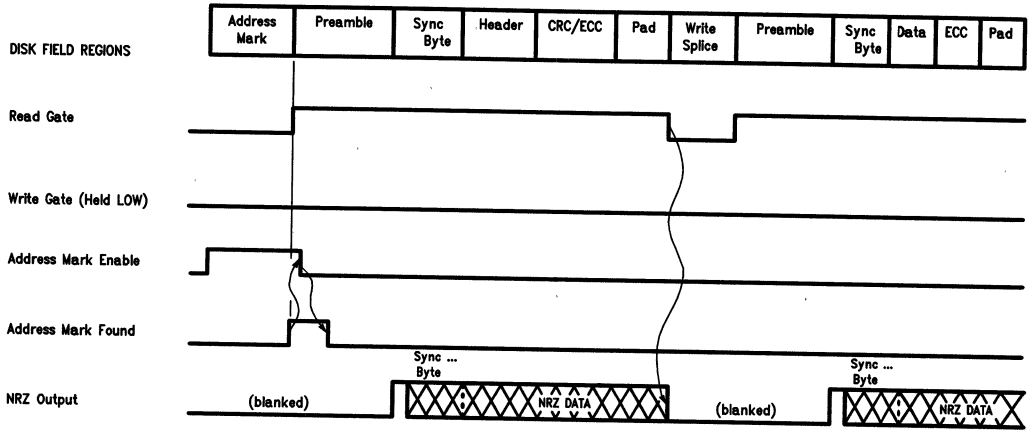


Note: Cycling either Write Gate, ▨ or AME ▨ resets the encoder, and starts the Preamble again.

TL/F/9386–4

ESDI (Std and Nt) MODE Control Waveforms (Continued)

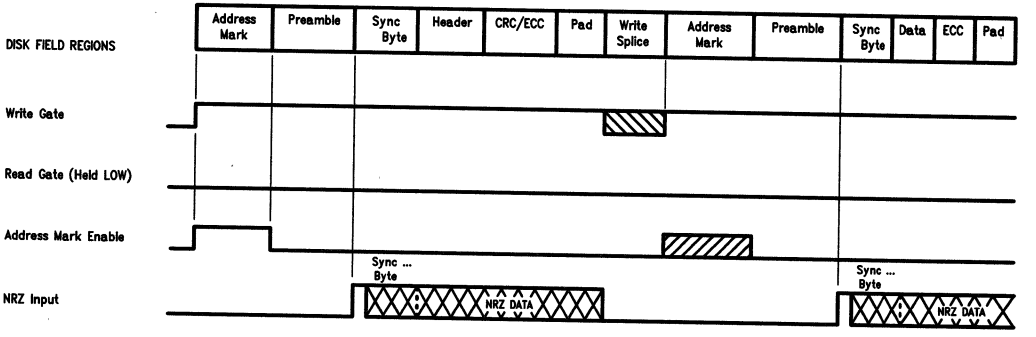
Read Cycle



TL/F/9386–5

SMD (Std and Nt) MODE Control Waveforms

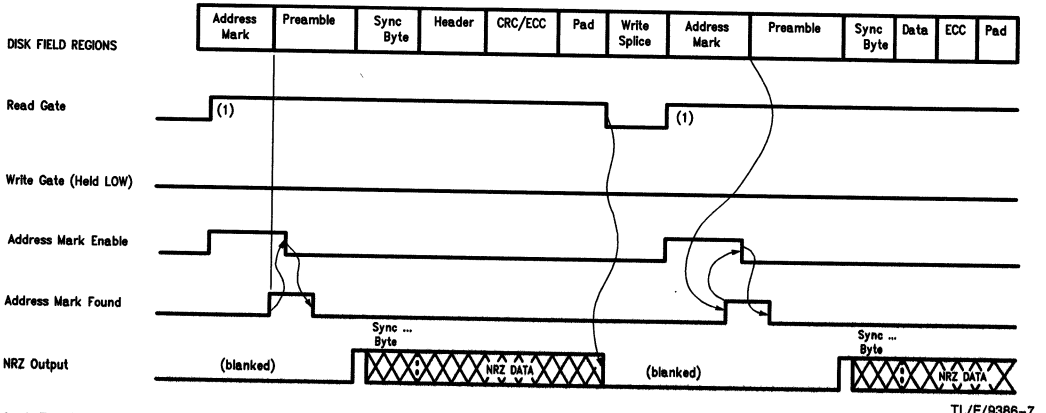
Write Cycle



Note: Cycling either Write Gate, ▨ or AME ▨ resets the encoder, and starts the Preamble again.

TL/F/9386–6

Read Cycle

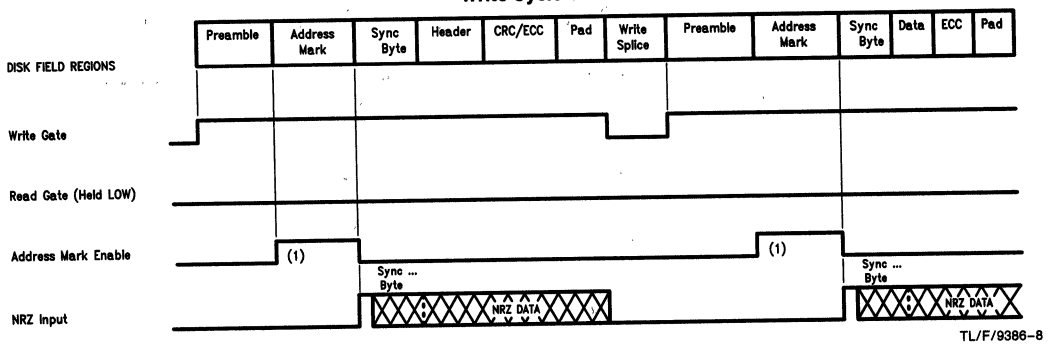


TL/F/9386–7

Note 1: Read Gate to the Synchronizer is internally qualified with AMF.

ST506A MODE Control Waveforms

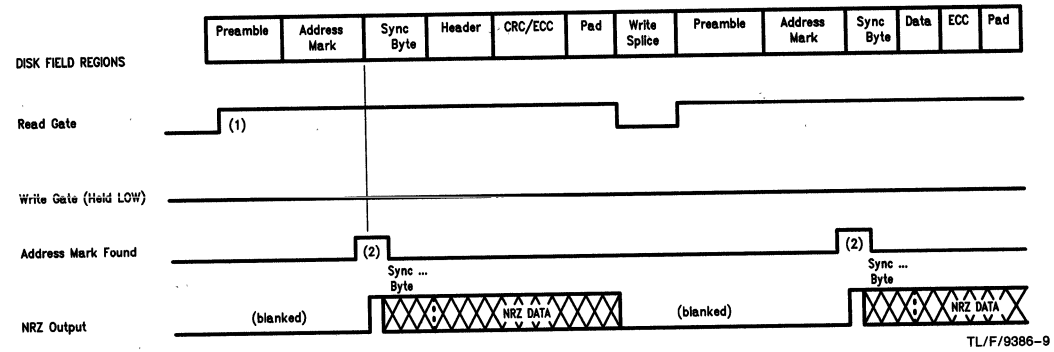
Write Cycle



TL/F/9386-8

Note 1: AME must be exactly 8 NRZ bits.

Read Cycle



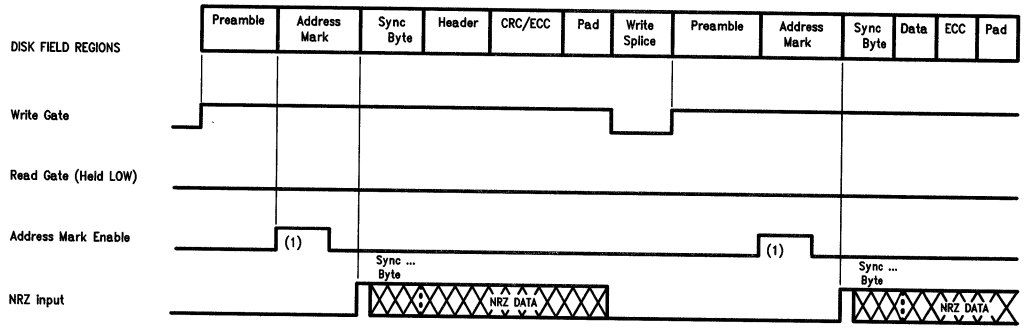
TL/F/9386-9

Note 1: The DP8469 employs a Preamble Prequalifier to ensure that the Read Gate is only passed to the synchronizer after the Preamble field has been found.

Note 2: AMF Terminated by the Second NRZ OUTPUT bit after NRZ OUTPUT unblanks.

ST506B MODE Control Waveforms

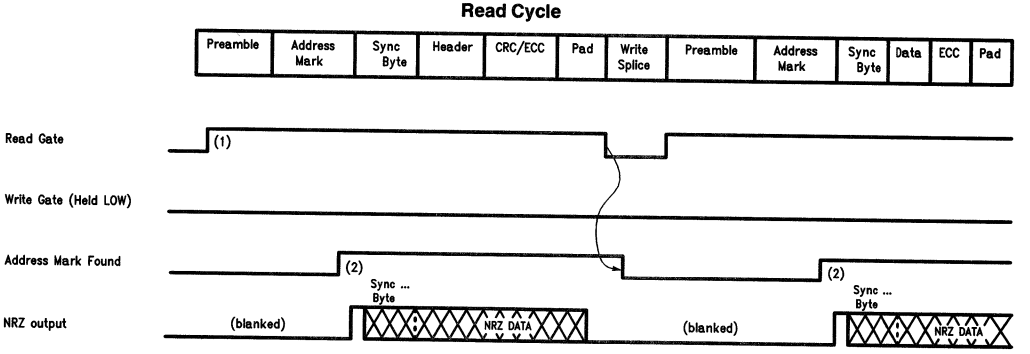
Write Cycle



TL/F/9386–10

Note 1: AME must be exactly NRZ bits.

Read Cycle

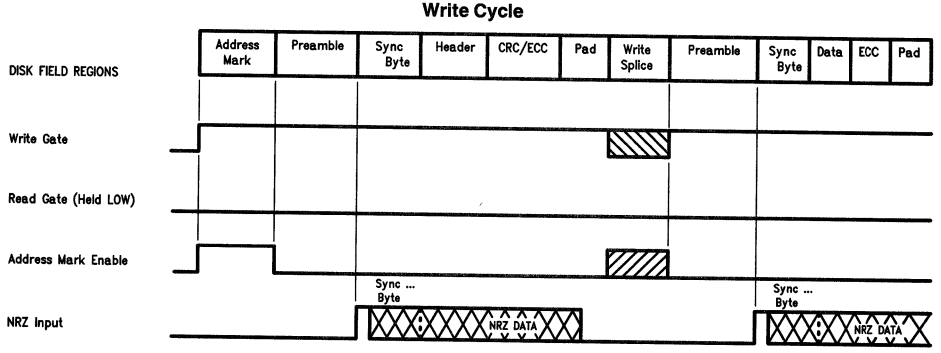


TL/F/9386–11

Note 1: The DP8469 employs a Preamble Prequalifier to ensure that the Read Gate is only passed to the synchronizer after the Preamble field has been found.
Note 2: AMF terminated by the deassertion of Read Gate.

IBM and DP8466 ESDI Mode Control Waveforms

Write Cycle



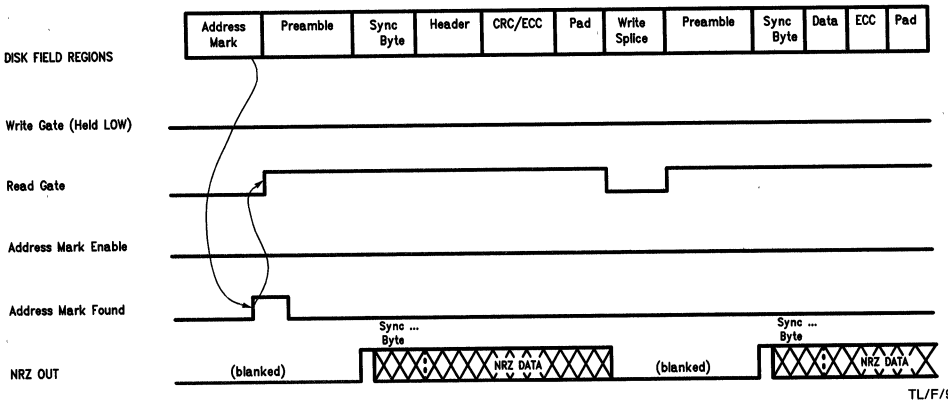
Note: Cycling either Write Gate, ▨ or AME ▨ resets the encoder, and starts the Preamble again.

IBM Address Mark is written as a 2 byte gap with 3 transitions, DP8466 ESDI uses standard 3 byte transitionless ESDI gap

TL/F/9386–32

IBM and DP8466 ESDI Mode Control Waveforms (Continued)

Read Cycle

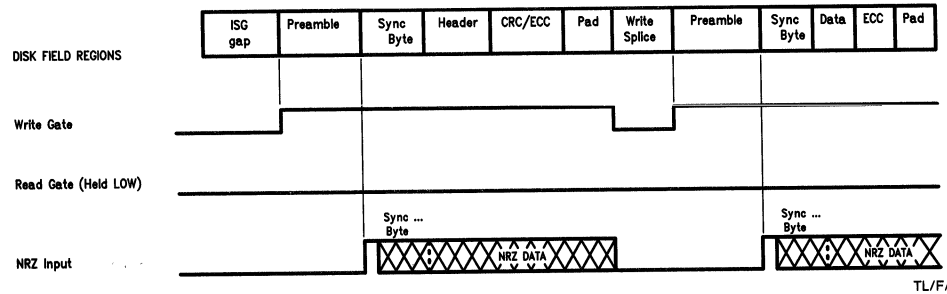


TL/F/9386–33

Note: AME is a DON'T CARE during Read Mode.

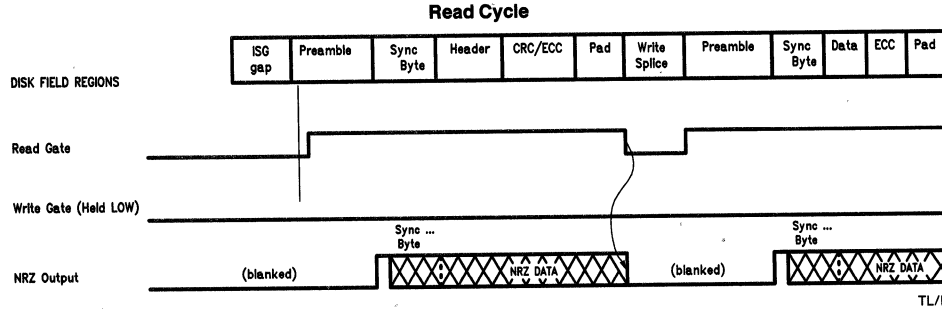
Hard Sector MODE Control Waveforms

Write Cycle



TL/F/9386–12

Read Cycle



TL/F/9386–13

Precautions for Disk Data Separator (PLL) Designs—How to Avoid Typical Problems

National Semiconductor
Application Note 414
William Llewellyn

The disk data separator/synchronizer PLL is subject to a unique set of concerns, all of which can be accommodated when adequate precautions are taken in system design.

FRACTIONAL HARMONIC LOCK

The frequency discrimination capacity of the digital phase detector within the data separator/synchronizer is suppressed whenever a pulse gate technique is employed. Although this pulse gating technique is a standard in disk drive applications and is necessary in order to allow the PLL to remain phase locked to randomly spaced disk data bits, it essentially causes the phase detector to behave as would an analog quadrature multiplier, i.e., the capture range of the loop takes on the finite value related to the loop bandwidth. Under ordinary circumstances, this is quite acceptable; however, it does permit the PLL to become susceptible to a form of quasi-stable false lock to fractional harmonics of the input frequency. (For example, a typical lock null for this phenomenon would be where the VCO stabilizes at 5/6 or 6/5 of its nominal frequency.) The conditions for occurrence of this are:

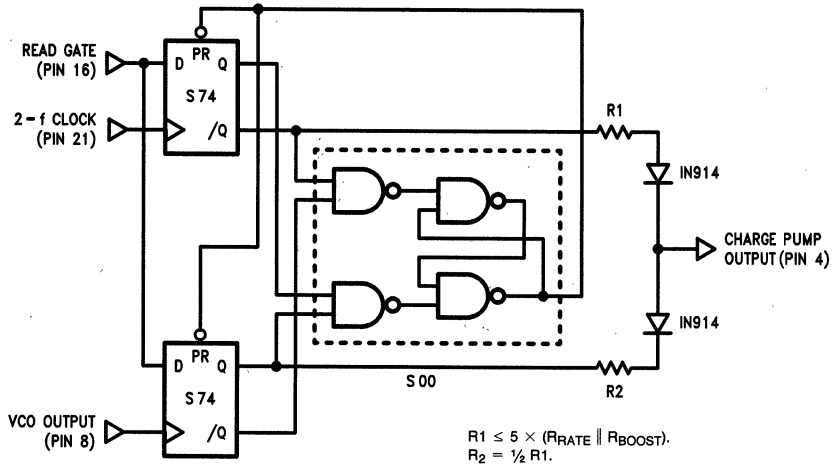
1) Pulse gate in use;
2) Periodic pattern is present (i.e., preamble);
3) Perturbation occurs either during or just prior to the periodic pattern, causing the VCO to swing outside of the dynamic capture range of the loop.

Since the capture range in a typical disk PLL configuration is on the order of ±2% of the data rate, it can be seen that harmonic lock could easily occur given an adequate perturbation of the loop. Typical causes of perturbations would be media defects and spurious noise pulses, among others, but the most commonly seen occurrence within soft-sectored systems is where an attempt is made to "read" through the write splice region on the disk (zone where the head write current is either switched on or off) during a sector search operation. Typical system-level symptoms of fractional harmonic lock are "sector not found" and "address mark not found" errors. Data (CRC or ECC) errors rarely are seen here because the phenomenon occurs primarily during the sector search routine.

Recovery from harmonic lock will occur readily when the read operation is terminated if:

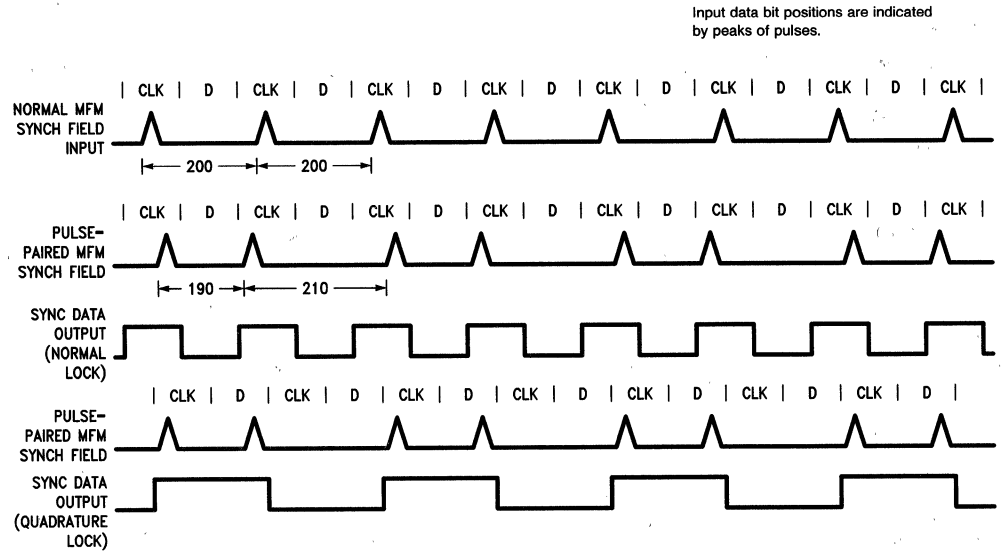
1) frequency discrimination is re-introduced as the PLL is re-locked to the reference clock, or
2) the PLL bandwidth is raised to a higher value (capture range is extended) as the PLL is re-locked to the reference clock, or
3) the phase transient experienced by the PLL as its input is switched back to the reference clock is enough simply to jar the PLL back to the correct frequency.

Item #1 is incorporated within all of National's current hard disk data separator/synchronizer circuits (the DP8460/50 are excepted, being replaced by the DP8465/55). Item #2 (user optional) is incorporated within all of National's hard disk PLL's. Systems which incorporate the frequency lock function (#1) along with a suitable sector search algorithm will rarely, if ever, encounter difficulty in this area. If the



TL/F/8598–1

FIGURE 1. External Phase-Frequency Comparator Circuit for the DP8460



TL/F/8598–2

FIGURE 2. Timing Diagram of PLL Quadrature Lock Within a Symmetrically Pulse-Paired Synch Field

system employs a PLL which does not incorporate frequency acquisition when locked to the reference signal (such as the DP8460/50 predecessor of the DP8465/55), either a simple external circuit may be added if desired to achieve the function (see *Figure 1*), or the PLL can be updated by inclusion of the DP8465 or DP8455. The DP8461 or DP8451 would provide the most reliable solution (frequency aquisition of both preamble and reference clock), but may be used only within hard or psuedo-hard sectored systems. (Note that the resistor values given in *Figure 1* are initial recommendations only; values may need to be adjusted to optimize system performance.)

Within systems where it becomes evident that the reading of write splices is consistently producing sector-not-found errors, while at the same time it is not possible to either modify the sector search algorithm (in order to avoid the splices) or to incorporate the lock support circuitry of *Figure 1*, the PLL can be made less sensitive to the write splice disturbance by the lowering of the loop bandwidth. This is recommended only as an interim solution until firmware or hardware accommodations can be made.

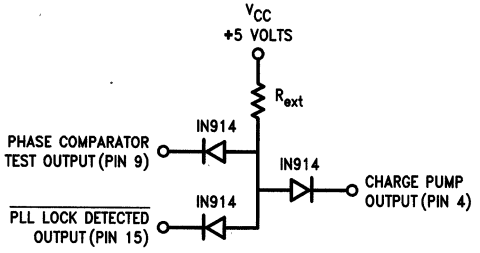
QUADRATURE LOCK

Another form of false lock may also occur (pulse gate in use) within a periodic disk pattern (preamble) given one additional condition; the periodic disk pattern being presented to the PLL exhibits a pulse-pairing phenomenon (typically introduced by the data channel electronics); see *Figure 2*. Within this particular pattern, PLL has the potential to lock to the correct frequency while remaining caught on a phase null 90 degrees from nominal. In this case, each pair of bits is interpreted by the PLL as residing in two directly adjacent windows (actually a violation of all standard disk codes) with the two subsequent windows empty. Although the bits appear to be greatly shifted within these windows, the phase corrections produced complement each other and average to a filtered DC value of zero. This repeating pattern is thus self-sustaining.

Quadrature lock is unique in that it is more likely to occur within a relatively well designed, noise-free system environment. The reason for this is that the randomizing effect noise ordinarily has on the data stream has been minimized, preserving the purity of the pulse paired pattern and thus increasing the probability of this form of lock. Again, this form of lock is generally only seen within the preamble, and may occur within either soft or hard sectored systems. The most typical symptoms are "address mark not found" or "ID error", with "sector not found" occurring, but less frequently. Easily recognized waveform patterns seen at the separator/synchronizer outputs would be (1) the Synchronized Data Output exhibits a 110011001100 . . pattern instead of the standard 1010101010 . . . preamble pattern; (2) the Phase Comparator Test output pulse width consistently remains at approximately half of the VCO period (nominal width should be 7–12 nanoseconds); (3) -Lock Detected does not become active (low).

The most robust solution to this phenomenon (as well as to harmonic false lock, as mentioned above) is to incorporate a hard or pseudo hard-sectored search algorithm in conjunction with a data separator/synchronizer which employs frequency acquisition within the preamble. The frequency acquisition mode allows no residual phase or frequency error within the PLL when locked, and thus the possibility of both quadrature and harmonic lock is eliminated.

Although the modified sector search algorithm of the first solution may be possible, certain system constraints may not allow it to be practical. A second, highly effective solution to quadrature lock involves the inclusion of four passive



TL/F/8598–3

Recommended value for R_{ext}:
$10[R_{rate} \| R_{boost}] \leq R_x \leq 20\ [R_{rate} \| R_{boost}]$

FIGURE 3. External Circuitry Used to Insure Correct PLL Lock to a Pulse-Paired Synchronization Field

elements external to the National disk PLL (see *Figure 3*) which will deliberately force the window to shift away from the 90 degree phase null when (and only when) quadrature lock occurs. The passive network is automatically disabled once the PLL detects preamble lock. Although a recommended value is given for the resistor in this support circuit, some experimenting may be required in determining an optimum value for use within any particular system.

VCO JITTER

The inherent purity of the VCO's operating frequency is a key element in the accuracy of the data separator/synchronizer window generation. Any "jitter" present in the VCO frequency (any modulation of the period of the waveform by noise or any other source) will degrade the performance of the PLL. Within National's initially released DP8460/50 data separators-synchronizers, it has been found that maintaining a value of R_{rate} at or below 820Ω has a stabilizing effect on the jitter performance of the VCO circuitry. Although this is primarily a characteristic of these two devices, we are recommending the following guidelines be followed in the selecting of charge pump resistors and loop filter components for all of the hard disk data separator/synchronizer circuits (see table I):

1) An 820Ω value resistor should be substituted for the originally recommended value of 1.5 kΩ.

2) Although this new R_{rate} value is below the original DP8460 specification limit, a substitute requirement has been placed on both R_{rate} and R_{boost} to maintain proper circuit operation:

$$R_{rate} \| R_{boost} \geq 350\Omega$$

(i.e., the parallel value of R_{rate} and R_{boost} should not fall below 350Ω.)

3) If the inclusion of an 820Ω value for R_{rate} means a component change within an existing system (i.e., the user had been employing some higher value), all other component values associated with the loop filter must also be modified in order to maintain the original PLL response characteristics within the disk data field:

Define: $M = R_{rate}(old)/820$ [eg., (1500/820)]. Then,

$$CLF1' = CLF1 * M$$
$$CLF2' = CLF2 * M$$
$$RLF1' = RLF1 / M$$

4) Additionally, in the cases where the external Phase-Frequency circuitry and/or the Quadrature lock circuitry are in use:

$$R1' = R1 / M$$
$$R2' = R2 / M$$
$$R_{ext}' = R_{ext} / M$$

Table I. Data Separator/Synchronizer Reference List

Device	Synchronized Codes	Separated Codes	Frequency Lock	Delay Trim
DP8461*	MFM; 1, N	MFM	Reference & Data	None
DP8462*	2, 7 MFM;1, N	None	Reference & Data (optional)	Optional
DP8465*	All	MFM	Reference	None
DP8451	MFM; 1, N	None	Reference & Data	None
DP8455	All	None	Reference	None

Note 1: "All" code synchronization does not include GCR.

Note 2: DP846X devices are in the 24-pin, 300 mil. package; DP845X devices are in the 20-pin, 300 mil. package.

Note 3: * Also available in 28-lead plastic chip carrier.

Note 4: DP8461 and DP8451 pinouts match the DP8465 and DP8455, respectively; for use with hard and psuedo-hard sectoring only.

Note 5: DP8462 incorporates optional frequency acquisition for 2, 7 synchronization fields, but may be used as a data synchronizer for any disk code.

Note 6: DP8451 and DP8455 also available in PCC package (20 pin).

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

The phase locked loop is inherently a sensitive device, and thus the environment in which it is operated should be optimized wherever possible to improve reliability. The following list applies for National's family of hard disk data separator/synchronizer circuits:

1) Establish a local V_{cc} island or net, separate from the main V_{CC} plane, to which the device and its associated passive components can be connected. V_{CC} supply filtering should be liberal and in very close proximity to the chip. The electrical lead length of the filter capacitance between the V_{CC} and ground pins themselves should be as short as possible (minimizing lead inductance). Inclusion of a quality high-frequency capacitor, such as a 1000 pF silver-mica capacitor, in parallel with a ceramic 0.1 μF capacitor, is recommended. (Note: the chip is particularly sensitive to inadequately filtered switching supply noise.)
2) Effective capacitive bypassing of the R_{boost} and R_{rate} pins (#2 and #3) directly to the V_{CC} pin is very important. Again, use quality, high-frequency capacitors and maintain the shortest possible electrical lead length.
3) Use the main digital ground plane for all grounding associated with the device. The ground pin and the PG1 pin should tie directly to this plane.
4) Do not locate the chip in a region of the PC board where large ground plane currents are expected.
5) Locate all passive components associated with the chip as close to their respective device pins as possible.
6) Orient the chip's external passive components so as to minimize the length of the ground-return path between each component's ground plane tie point and the chip's ground pin. (Ground noise at the loop filter components, RLF1, CLF1 and CLF2, which is not identically present at the ground pin (common mode), is coupled through the filter components into the VCO control voltage pin.)
7) Include no planing whatsoever (V_{CC} or ground) directly between adjacent pins. This will minimize parasitic capacitance at each pin. Planing between the two pin rows, however, is recommended (directly beneath the package).
8) Avoid running signal traces between pins.
9) Run no digital signal lines between or adjacent to the analog pins or signal traces (pins 1 through 7 and PG3) in order to avoid capacitive coupling of digital transients.
10) Minimize the total lead length of the C_{VCO} capacitor. Inductance in this path degrades VCO performance, as does parasitic pin capacitance.
11) Do not place any bypass filtering at the R_{VCO} pin (minor coupling of the VCO waveform into this pin is normal and acceptable).
12) Eliminate negative-going voltage transients (undershoot) at the digital input pins (pre-termination of driving lines may be necessary) to avoid drawing transient input-clamp-diode current from the device pins.
13) Minimize digital output loading; i.e., if outputs must drive large loads or long lines, employ buffers.
14) Allow unused digital output pins to float, unconnected to any net.
15) Avoid locating the chip within strong electromagnetic fields. If possible, choose the "quietest" region of the board.
16) If chip socketing is desired, use a low-profile, low mutual capacitance, low resistance, forced-insertion type (socket-strips are recommended). Avoid the use of "ZIP-DIP's".
17) Do not use wire-wrap interconnect, even in an evaluation set-up.
18) Make allowance for pin-to-pin capacitance when determining C_{VCO} (Typically 4–5 pF) from data sheet formula.

Designing with the DP8461

National Semiconductor
Application Note 415
Kern Wong

GENERAL DESCRIPTION

The DP8461 is one of the second generation data separator/synchronizer products introduced following the highly successful DP8460 single chip PLL circuit for applications in rotational memory storage systems. The DP8461 consists of the same basic functional blocks as the first generation device (DP8460). It has a proprietary pulse-gate which features an accurate silicon delay line, an edge-triggered digital phase comparator, a high speed matched charge pump, high impedance buffer amplifier, and a temperature compensated stable voltage-controlled-oscillator (VCO). It also contains MFM decoder, missing clock detector, and lock-detect control circuitry for maximum design flexibility.

Like the DP8465, the DP8461 performs PHASE-FREQUENCY COMPARISONS in the non-read mode (READ GATE is "Low"). This enhancement eliminates the possibility of false lock to the reference signal during a power-up sequence or when returning from a read operation. Furthermore, the DP8461 has been designed to allow PHASE-FREQUENCY COMPARISONS to continue into the preamble field during read mode (READ GATE is "High"). This feature eliminates the possibility of a Quadrature Lock or Harmonic Lock problem occurring in the PLL synchronization field. In order to take advantage of phase-frequency comparison during preamble detection, the DP8461 requires a "Qualified Read-Gate" (that is the READ GATE shall be asserted only within the preamble or maximum frequency field span). Since the DP8461 looks for a 1010. . . encoded data pattern while doing PHASE and FREQUENCY COMPARISONS in the read mode, it must be used only with a code employing this preamble such as MFM, (1,7) or (1,8). The DP8461 is pin-for-pin compatible with the DP8460 and DP8465 parts; and is also functionally equivalent to them with the exceptions of extended Phase-Frequency Comparison during preamble and a "Qualified Read-Gate" requirement. The DP8461 can be used as a synchronizer for MFM, (1,7), and (1,8) codes or as a data separator for MFM only. *Figure 1* shows a diagrammatic comparison of the key functional features of the three part types mentioned above.

CIRCUIT OPERATION

The DP8461 is in the non-read mode whenever the READ GATE is deasserted (Low). The 2F REFERENCE CLOCK INPUT is divided by two and transmitted to the READ CLOCK OUTPUT via a multiplexer. In this mode the VCO DIVIDED BY TWO is locked onto the 2F CLOCK DIVIDED BY TWO, keeping the VCO close to the data frequency in anticipation of locking onto the actual data stream. While in the non-read mode, PHASE-FREQUENCY COMPARISONS are always employed to eliminate any possibility of false lock.

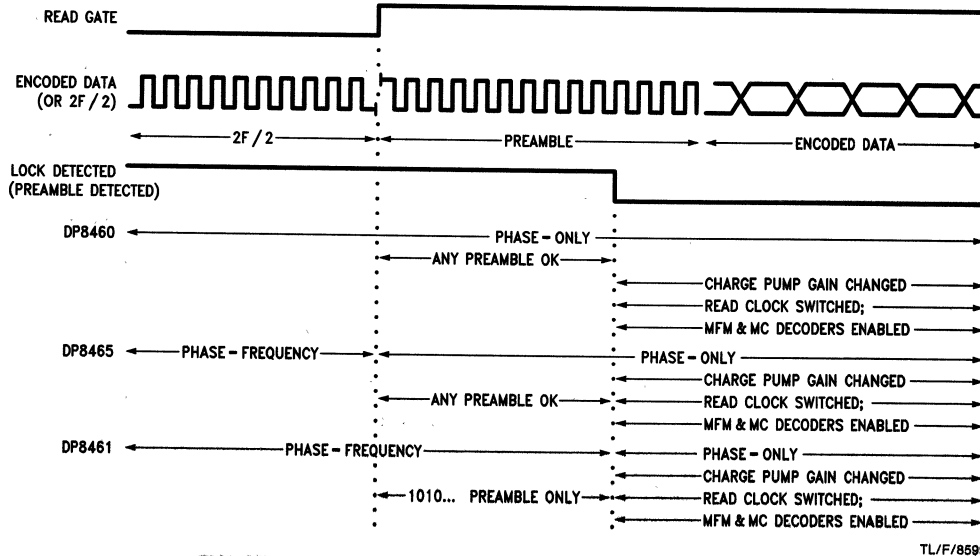


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FIGURE 1. DP8460/65/61 Modes of Operation Comparison Diagram

Since the DP8461 continues to make PHASE-FREQUENCY COMPARISONS when the read mode is entered, the assertion of READ GATE should only occur over a PREAMBLE or 1010... pattern. The DP8461 enters the read mode after a selectable delay time which may be either one or thirty-two VCO cycles. The 2-byte (32 VCO cycles) delay is useful in hard-sectored drives for allowing a gap pattern to pass before the PLL locks onto the data pattern. Soft-sectored drives do not need this delay. Once in the read mode, the PLL reference input is switched from the 2F CLOCK source to the ENCODED DATA INPUT. The PLL remains in the high track rate mode and continues to perform PHASE-FREQUENCY COMPARISONS to quickly lock onto the repetitive encoded preamble.

By careful selection of the loop filter components, it takes less than one byte time for the VCO to lock onto the data stream sufficiently for preamble detection to begin. As soon as 2 bytes (16 consecutive pulses) of the selected (ones or zeroes pattern) preamble are detected, the $\overline{\text{LOCK DETECTED}}$ OUTPUT goes low and this causes the PLL circuit to switch from PHASE-FREQUENCY comparisons to PHASE-ONLY comparisons. In a typical disk drive application, the $\overline{\text{LOCK DETECTED}}$ OUTPUT may be directly connected to the $\overline{\text{SET PLL LOCK INPUT}}$. When a low level is present on the $\overline{\text{SET PLL LOCK INPUT}}$, the CHARGE PUMP changes from a high to low tracking rate, the source of the READ CLOCK signal switches from the 2F CLOCK INPUT to the VCO CLOCK, and the MFM decoder becomes enabled and begins to output decoded NRZ data. If the DP8461 is employed as a data separator for MFM encoded data, the READ CLOCK OUTPUT and the NRZ READ DATA OUTPUT (which is synchronized to the READ CLOCK) should be used. These TTL compatible signals can be connected directly to a Disk Data Controller such as the DP8466 which controls Winchester or floppy disk drives. The MISSING CLOCK DETECTED OUTPUT can also be utilized for MFM-encoded data for soft-sectored disk drives. It should be noted, however, the circuit is designed only to recognize a missing MFM clock-bit which is framed by two existing clock bits. In order to insure the detection of an address mark, simultaneous monitoring of the NRZ output for an "A1" hexidecimal code and the MISSING CLOCK DETECTED OUTPUT for a single pulse within the same byte time is necessary.

When the READ GATE goes low, signifying the end of a read operation, the PLL reference signal is switched back to the 2F CLOCK and the $\overline{\text{LOCK DETECTED}}$ OUTPUT goes high, causing the VCO gating circuitry within the PULSE GATE to be bypassed thus allowing PHASE and FREQUENCY comparisons to occur. The PLL also returns to the high tracking rate and the output signals return to their initial conditions.

If the chip is used as a data-synchronizer (on-chip decoding not necessary) for MFM or other popular RLL codes employing a 1010... preamble, the SYNCHRONIZED DATA OUTPUT and the VCO CLOCK OUTPUT should be used. External decoding can be accomplished either in commercially available controller chips or encoder/decoder circuits, or by the customer's proprietary design.

PHASE ONLY VS. PHASE-FREQUENCY COMPARISON OPERATION

As stated earlier, the function of the PLL is to maintain phase and frequency lock between the reference signal (2F CLOCK or ENCODED DATA) and the feedback signal (VCO). A comparator that performs only phase comparison is mandatory during read-mode in the data field in order to handle the non-periodic nature of various coding schemes. With this type of detector, the phase-locked-loop functions as a feedback loop in which it responds only to the phase differences between the input and the feedback waveforms. As long as the reference and VCO singals have their edges aligned (are in phase lock), the PLL is insensitive to their frequency relationship.

During the non-read mode the PLL is required to lock onto the 2F CLOCK, a specific frequency reference that is close to the data rate. If a disturbance is somehow introduced in the system which results in cycle slipping or prolonged transient behavior of the reference clock, false lock may occur if a PHASE-ONLY comparator is being used. Similarly, in the preamble field during read mode, the PLL tries to lock onto a periodic pattern. If pulse-pairing occurs in this PLL synchronization field due to asymmetry in disk drive electronics, quadrature lock may result if a PHASE-ONLY comparator is being used. Under these circumstances PHASE comparison alone may be inadequate, since it discriminates only phase and not frequency information. A PHASE-FREQUENCY-COMPARATOR, therefore, is recommended during these modes of operation whenever false lock presents a potential problem. The DP8461 implements such a comparator. It performs identically to the PHASE-COMPARATOR in the case when both inputs to the comparator have the same frequency; however, if the inputs exhibit the slightest frequency offset, the PHASE-FREQUENCY-COMPARATOR also provides a frequency-sensitive error correction signal to ensure frequency acquisition.

As mentioned in the device description, the DP8461 requires a "Qualified Read-Gate" for proper operation in soft-sectored environments. This is necessary to accommodate phase-frequency comparison into the preamble field. If the READ GATE is allowed to be asserted randomly, it might be asserted in the data field or in the write-splice area. With the DP8461, prior to preamble detected, the PLL is operating in the phase-frequency mode. If it encounters a low frequency pattern in the data field, the VCO will try to lock onto it and thus shift its frequency. Similarly, if READ GATE becomes active in a write-splice area, the PLL may be pushed to either of its limiting frequency excursions. By employing a "Qualified Read-Gate" with the DP8461, the READ GATE will always be asserted over a repetitive 1010... pattern and thus avoid any of these problems.

PULSE GATE

The PULSE GATE has two important functions. It ensures a continuous PLL lock in the presence of random patterns encountered on the media and in the bit stream. It also provides a precise time delay (independent of process and

external component variations) necessary to align the incoming data with the center of the decoding window. The delay is exactly one-half the period of the 2F CLOCK and the delay generator is referenced to the 2F CLOCK. This allows input bit jitter up to ±one-half the 2F CLOCK period.

The PULSE GATE incorporated in the DP8461 has two multiplexers which allow the circuit to switch from PHASE-FREQUENCY COMPARISON to PHASE-ONLY COMPARISON when the LOCK DETECTED signal becomes active (Low). *Figure 2* is a block diagram of the PULSE GATE which details how this is accomplished. When both the INTERNAL READ GATE and the INTERNAL LOCK DETECTED are inactive (non-read mode) the 2F CLOCK DIVIDED BY TWO and the VCO DIVIDED BY TWO signals are selected by MULTIPLEXER-1 and MULTIPLEXER-2 respectively. In this configuration phase and frequency comparisons are made between them and the possibility for a false lock occurrence is eliminated. When the INTERNAL READ GATE is active while the INTERNAL LOCK DETECTED remains inactive (read-mode, preamble detection) the ENCODED DATA and the VCO DIVIDED BY TWO signals are selected by the multiplexers. Again, PHASE-FREQUENCY COMPARISONS continue to be performed to ensure the PLL locks exactly to the data rate frequency. After sixteen pulses of consecutive preamble pattern are detected, the INTERNAL LOCK DETECTED line becomes active. MULTIPLEXER-2, under the control of the INTERNAL LOCK DETECTED singal, then switches from the VCO DIVIDED BY TWO to the GATED VCO signal. Through the circuit configured by the D-type flip-flops and the OR gate, the comparator effectively performs PHASE-ONLY comparisons (an INTERNAL VCO pulse is allowed to the input of MUX-2 only when an ENCODED DATA pulse is sensed). Thus, the DP8461 guarantees proper frequency lock of the VCO to the 2F REFERENCE CLOCK during the non-read mode and to the preamble synchronization pattern during the read mode. The circuit performs the necessary phase-only comparison in the data field during read mode operation.

DATA SEPARATOR APPLICATION PROBLEMS

Following are some common application problems for many data separator circuit designs. The purpose of this application note is to identify these problems and to propose simple solutions thus enabling our DP8461 users to avoid these potential application problems.

FORMS OF FALSE LOCK

Two types of pseudo-lock can typically occur in a PLL within a disk drive system. A periodic input waveform must be present, such as a disk synchronization field, in conjunction with the suppression of frequency information (pulse-gate type PLL) in order for either to occur.

Pulse Gate Block Diagram

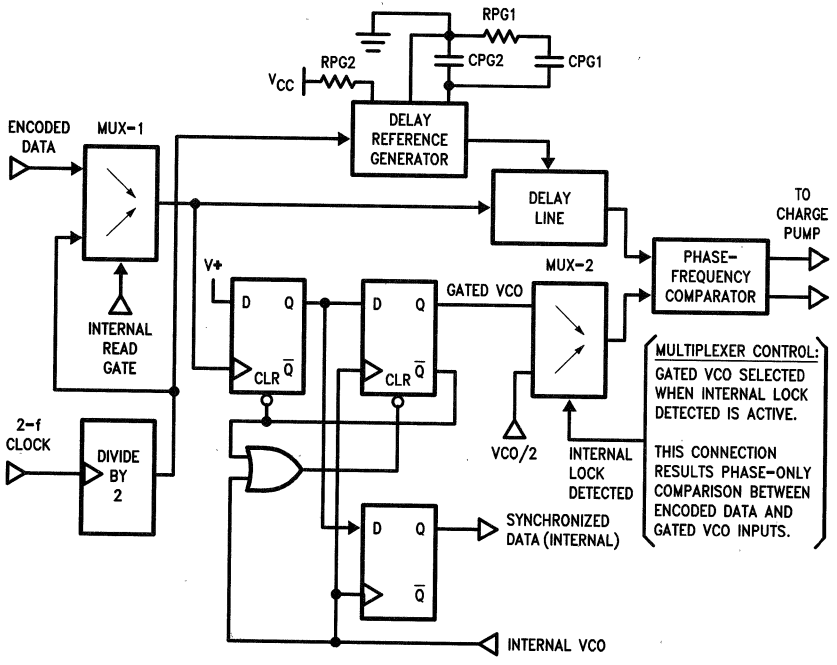

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FIGURE 2

I. The first is herein termed simply "false lock", or more accurately, **fractional harmonic** lock. This occurs when the PLL is disturbed, forcing the VCO outside of the capture range (determined by the loop bandwidth; typically ±2% of the data rate) of the PLL for a period of time. The PLL is then able to acheive a pseudo-lock if (1) the ratio of the VCO frequency vs. the input frequency is an integer fraction, such as 5:6 or 6:5, and (2) the difference frequency between the VCO and the input is greater than the PLL capture range. Ideally, the error signal generated at the VCO control input, which is at the "beat" (difference) frequency of the two signals, would correct the false lock. However, this error signal is suppressed because it lies outside the frequency range of the low pass loop filter. The loop will, however, produce a self-sustaining error signal and thus will remain on the false lock null.

II. The second form of pseudo-lock is called **quadrature lock**. In this case, the PLL is able to lock to the correct frequency, but is caught on a narrow phase null which is positioned 90 degrees (w. r. t. the NRZ data period) from nominal. This phase null can occur only when there exists a pairing of periodic disk data pulses which originates in the disk drive itself (see *Figure 3*). The quadrature lock is perpetuated because the net error signal generated at the VCO input by the displaced, complimentary pulses lies well outside of the loop bandwidth and is averaged to a self-sustaining correction signal.

LOSS OF LOCK DURING READ MODE

In some systems the controller asserts the READ GATE randomly along a formatted track. If the READ GATE is asserted over a write splice, which usually contains unintelligible information, the PLL might false lock to some harmonic of the data or it might be pushed to either extreme of its allowed frequency swing. Similarly, when the READ GATE is asserted over a data field the PLL might lock to a harmonic of the data.

This problem can be completely avoided with the DP8461, which is used in conjunction with a "Qualified Read-Gate" technique. As an example, a good PLL controller algorithm that only allows assertion of the READ GATE over a preamble or similar high frequency pattern is listed below.

1) Deassert READ GATE—allow a 4 byte time minimum for the PLL to lock to the 2F-REFERENCE CLOCK.
2) Wait for 2.5 bytes of valid preamble pattern.
3) Assert READ GATE.
4) If valid preamble continues for 5 or more bytes then go to 5; otherwise go to 1.
5) "LOCK DETECTED" becomes active, AM search begins.
6) If AM is found, then continue the read routine; otherwise go to 1.

FALSE LOCK IN THE NON-READ MODE

The DP8461 **has been specifically designed to eliminate the possibility of false lock during the non-read mode.** This is accomplished by the use of a phase-frequency comparator in the non-read mode as was described in the PULSE GATE section.

False lock during the non-read mode can occur by two means in systems using phase-only comparisons in the non-read mode. When the power supply of the PLL circuit is switched on for the first time, the VCO ramps toward the reference frequency. The acquisition process may lock the VCO to some harmonic of the 2F REFERENCE CLOCK if the bandwidth (capture range) is not high enough. False lock can also occur in the non-read mode after an aborted read operation as described above. If the VCO has either lost lock or has been driven far from its center frequency while trying to read, false lock might occur during relock to the crystal if the capture range is narrow.

Example shows 5 Mbit/sec MFM synchronization field.
Input data bit positions are indicated by peaks of pulses.

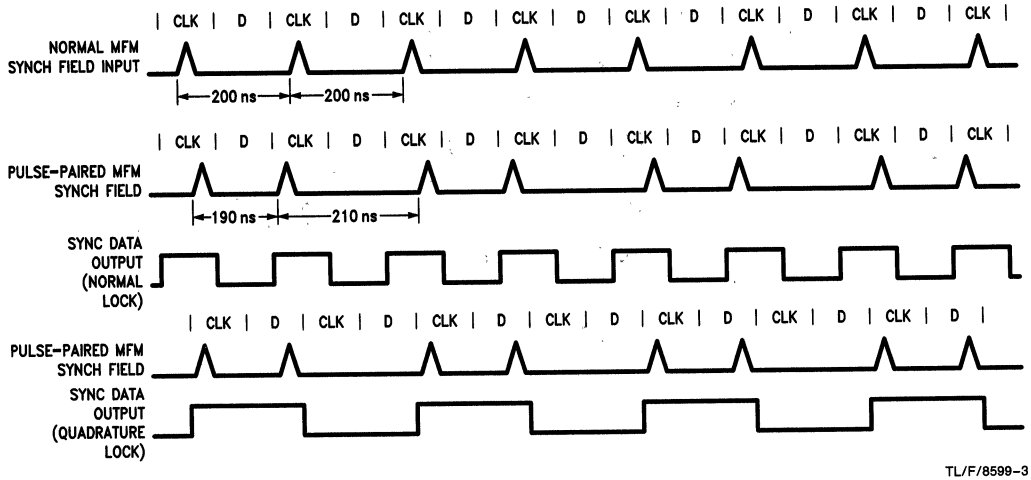

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FIGURE 3. Timing Diagram of PLL Quadrature Lock within a Symetrically Pulse-Paired Synch Field

QUADRATURE LOCK

The DP8461 **has been specifically designed to eliminate the possibility of both quadrature lock and harmonic lock in the preamble field during read mode** by extending the phase-frequency comparison technique during preamble detection in the read mode until LOCK DETECTED occurs.

Within the standard synchronization field which precedes the data field, bits are recorded at a constant frequency for a time sufficient to allow the PLL to acquire lock. With normal recording and read-circuit behavior, this synchronization information reaches the PLL as a continuous, periodic data stream. In some disk drives, if an offset has somehow been induced into the recorded information, or if read-channel asymmetry exists within the drive electronics which skews the flux reversal zero-crossing point, the synchronization field waveform which reaches the PLL may appear in the form of periodic pulse-pairs. This condition only arises when a repetitive pattern is present, giving rise to the possibility of quadrature lock. Note that quadrature lock is actually more prone to occur within systems where a low-noise design has minimized the randomizing effect which noise has on bit position.

MINIMUM PULSE WIDTH REQUIREMENT

The DP8461, as with other members of the DP8460 family of data synchronizers, has a minimum pulse width requirement on the ENCODED DATA input for proper operation. As there is no uniform pulse width specification on "Raw Read Data" outputs from disk and tape drive manufacturers, it has been found that certain drive systems output too narrow a pulse width for the DP8460 family of circuits to accept. Our recommended minimum positive pulse width is 6 ns and the minimum negative pulse width is 80% of the VCO period; this allows a maximum positive pulse width of 120% of the VCO period. Some drives utilize a bidirectional one-shot to shape the read data output pulse. The output pulse width from such drives can be readily readjusted from an RC timing network to attain acceptable minimum pulse width requirements for the PLL circuits.

Note: The chip is particularly sensitive to inadequately filtered switching supply noise.

SUMMARY

The DP8461 is another one of National's second generation single chip high performance PLL circuits for application in disk memory systems. This device features a comparator with both phase-frequency and phase-only comparison capabilities. Additionally, the PHASE-FREQUENCY COMPARISON circuit in the DP8461 has been designed to allow its operation in the preamble field during read mode so that employing it with a "Qualified Read-Gate" will eliminate all potential false and quadrature lock problems associated with soft-sectored systems. The DP8461 offers significant savings of cost and time in production, test, and maintenance since only a few fixed passive components are required for operation. The need to trim any external components has been eliminated and, since no external components determine window accuracy, the performance will not be sensitive to external variations. The chip requires a single +5 volt supply and it is housed in a narrow 24-pin dual-in-line package (also available in 28 pin PCC package). The DP8461 has the same pinout as the DP8460 and the DP8465, and thus, can be used in their designed applications provided the READ GATE has been qualified. The DP8461 can be used as a data synchronizer for MFM or any of the existing RLL codes employing a 1010. . . preamble, or as a data separator for MFM.

For further information, the reader should also refer to the National Semiconductor Application Note 414, Precautions for Disk Data Separator (PLL) Designs.

Designing with the DP8462

National Semiconductor
Application Note 494
Kern Wong

GENERAL DESCRIPTION

This literature assumes the reader has thoroughly read the DP8462 datasheet and is familiar with the basic circuit operation discussed therein. The objective of this note is to give the customer comprehensive application information for the design and testing of the device. It also offers detailed guidance in the selection of appropriate component values, use of optional device features, and considerations for system configuration. The following is a brief description of key features of the device.

The DP8462 is one of National Semiconductor's second generation disc data synchronizers designed for application in disc drive memory storage systems. It features 3T (1-0-0) or 4T (1-0-0-0) preamble detection circuitry which makes it especially convenient for systems employing run-length-limited codes such as the popular 2, 7 code. Of course, it may also be used as a data synchronizer for other conventional coding methods such as MFM, (1, 7), (1, 8), etc., but the internal (3T/4T) preamble detector function will then be bypassed.

This Phase-Locked-Loop (PLL) chip contains three customer programmable input control pins (TLL logic levels) to offer significant design flexibility. The PREAMBLE SELECT programming input determines whether the preamble detector looks for a 3T or 4T preamble pattern. The 4T preamble has been the most widely chosen pattern because of its ability to attain phase-sync naturally (refer to DP8463B (2, 7) ENDEC datasheet for detailed discussion). The LOCK-CONTROL input pin can be set to allow the phase comparator to function in one of two modes of operation: Phase and Frequency comparison or Phase-Only comparison. During non-read mode, phase and frequency comparison is employed within the DP8462 to lock onto the 2F reference clock. However, in the read mode the phase-frequency detection circuitry changes to phase-only comparison. Via the LOCK CONTROL input, the user may select when this mode change occurs, either immediately after Read Gate is asserted or after preamble detection has occurred. The charge pump also has two modes of operation: high track rate is used for fast acquisition to the 2F reference clock in the non-read mode and to the preamble in the read mode; low track rate is used in the read mode to allow smooth, stable lock to the data field. Both track rates are selectable by the customer via the I-BOOST ENABLE input. In a typical design the PREAMBLE DETECTED output may be directly connected to the I-BOOST ENABLE input to accomplish the desired track rate switch-over.

PHASE-ONLY OR PHASE-FREQUENCY COMPARISON

Depending on system characteristics and sector formats employed, such as soft or hard sectoring, encoding method, acquisition time requirement, etc., the system designers may be required to select only one of the two modes of comparison during read (preamble acquisition) or they may be free to choose either comparison mode to achieve optimum system performance. The following discussion illustrates the differences between the harmonic phase detector and the non-harmonic phase detector techniques incorporated in the DP8462 PLL chip.

In the non-read mode the PLL is always set to Phase-Frequency comparison mode (non-harmonic) to guarantee that it will attain frequency lock to the 2F Clock reference signal; thus, the possibility of a false lock occurrence is eliminated. In the read mode, if the Phase-Only comparison mode is chosen (via LOCK CTL: L0), then the phase detector will engage in phase comparison (harmonic mode) between ENCODED DATA and VCO gated by data pulses immediately upon Read Gate assertion. This must be done in a true soft-sectored system where there is no guarantee of Read Gate assertion occurring only within preamble field. Furthermore, the maximum phase step seen by the PLL at the assertion of Read Gate is at most one-half of one decode window period since the Pulse Gate allows the incoming data pulse to be compared with the nearest occurring VCO pulse. However, there is always a probabilistic condition that an initial burst of pulses can occur at the input during Read Gate switching which may violate normal coding methods or nominal pulse width specifications, resulting in synchronization errors. To avoid false lock possibility with Phase-Only mode in synchronization field when Lock Control is set "LO", it is recommended that the loop's natural frequency bandwidth, Wn, be low. Normally the loop filter component values for C1 and R1 will need to be recalculated in accordance with the lower Wn value selected. Optimizing the selection of the Pulse Gate network (RPG2 and RPG4) may also improve the loop's performance as this allows better centering of the data bit position with respect to its decode window and optimizes accurate locking to the data frequency.

The customer may also configure a soft-sectored write, and pseudo-hard sectored read system, which retains the advantages of formatting flexibility while capitalizing on the Phase-Frequency comparison feature in the read mode (with LOCK CTL: HI). Such a system configuration is realized with a Read Gate qualifying technique which ensures Read Gate is asserted only within the preamble field, thus removing any lock problems associated with reading through write-splice gaps or data field induced false address mark (AM) or false preamble patterns. With this method of operation, the PLL remains in the Phase-Frequency comparison mode in the preamble field until 16 consecutive preamble pulses have been successfully detected; then, it switches to Phase-Only mode. Employing a Phase-Frequency comparator during preamble acquisition ensures that the possibility of Quadrature Lock, a form of false lock due to pulse pairing in the read channel, is eliminated. Similarly, a true hard-sectored system will utilize these same techniques to avoid all the potential lock problems mentioned above.

The user should be aware of the fact that when employing frequency lock, the VCO divided by either 3 or 4 is compared with the data pulse. Therefore, depending on the initial logic state of the divider (which is random) and the initial phase difference incurred at the time of Read Gate assertion, the maximum phase error can be 3 or 4 VCO cycles long (depending on whether 3T or 4T preamble is selected) which is 6 or 8 times greater than when the Phase-Only mode is employed. This requires the PLL synchronization

bandwidth to be set adequately high in order to guarantee the phase error has settled to less than one-half of one decode window before the PLL switches out of frequency lock mode. Otherwise, a second phase step is introduced when the device switches out of frequency lock mode which lengthens lock times and may result in synchronization errors.

BANDWIDTH CONSIDERATIONS AND LOOP FILTER SELECTION

The DP8462 PLL is a frequency selective feedback circuit that can synchronize with a selected input signal and track the frequency and/or phase changes associated with it. A finite phase error is necessary to generate a corrective voltage to shift the VCO output frequency in compliance with the input signal variation. Once locked, the synchronizer can track a slowly changing input signal. It rejects transient changes (via loop filter) which tend to disturb the PLL. The phase detector (a bi-directional charge pump) generates a proportional error correction current pulse and is followed by a passive low-pass filter network generally with a sufficiently narrow bandwidth to suppress any noise and high frequency components from the phase-detector and charge pump stages. More importantly, the filter network determines the dynamic performance of the loop which includes capture and lock ranges, bandwidth, and transient response time. Of equal significance, the passive filter also yields the characteristic poles and zeroes for stability. There are numerous approaches to calculate a suitable set of filter component values; they may be estimated from a capture range point of view, from the required time and dynamic response profile of the loop, or from noise bandwidth considerations, etc.

LOOP FILTER COMPONENT VALUE SELECTION

The first step when selecting component values is to determine an appropriate value for the natural angular frequency, Wn, of the PLL. (Wn, commonly referred to as the loop's natural frequency should not be confused with the center frequency, Wo or Fo, of the VCO.) Wn is related to the loop gain and the RC time constants imposed by the low-pass loop filter. It should be noted that if the available loop gain is high and a relatively low natural frequency required, very large time constants will result. The size or value of the passive components for the loop filter may become impractical if not difficult to obtain. Therefore, judicious choice of Wn and filter components is necessary to allow good performance while at the same time using only standard component values. Optimum filter design may involve an iterative engineering effort from empirical data to arrive at the desired results. Recommended values in the datasheet are all valid suggestions but may not be the optimized values for every system.

As suggested in the datasheet, a (degenerated) 2nd order passive filter is quite adequate for most applications. The filter network consists of C1 connected in series with R1 and C2 connected in parallel with R1 and C1. The characteristic equation is 3rd order by inclusion of C2 in the highest order term. In practice, if the pole determined by R1 and C2 is more than a decade above the zero, the 3rd order term can be ignored and the equation can be rewritten as a 2nd order loop (refer to the DP8462 datasheet for details).

Two approaches for the determination of Wn are illustrated; component calculations are the same in each case. These examples allow digital designers to start estimating a loop filter without having to derive its poles/zero, and centroid, or construct Bode plots.

Example #1: 10 Mb/s data rate, (2, 7) encoding, 4T preamble

Assume it is desired to track the information recorded on a rotating or travelling medium being modulated by the spindle or capstan velocity, and assume there will be a 1.5% offset in the motor speed. It has been shown that a capture range greater than the input frequency offset, ΔW, will ensure that lock will occur quickly. Choose Rrate = 820Ω (an optimal value for the charge pump).

The initial frequency offset is then:

$$\Delta W = (1.5\%)\,(10\text{ Mb/s})\,(2\pi) = 942\text{ krad/s}$$

In most system designs, an optimally flat frequency-transfer function of the loop is the objective. The Bode diagram of such a transfer characteristic shows this can be achieved with $\zeta = 0.707$ (see reference: F. Gardner). The expression of capture range $\cong 2\,\zeta Wn$ is a reasonable approximation also found in reference materials (i.e., R. Best). A damping of $\zeta = 0.7$ is chosen as a design criterion for optimal response during the 4T pattern acquisition.

By equating capture range and ΔW for acquisition of 4T data pattern, (that is, one data pulse present within 4 VCO periods):

$2\,\zeta Wn\,(4T) \geq \Delta W$

$Wn\,(4T) \geq \Delta W/(2\zeta) = (942\text{ krad/s})/(2)\,(0.7) = 666\text{ krad/s}$

This is defined as Wn(max) during preamble or Xtal acquisition, where the PLL is locking onto the 4T preamble or the Xtal divided by 4 signal.

Wn is proportional to the square root of the data frequency (Refer to the datasheet:

$Wn = \sqrt{(2.5)\,(Fvco)/(C1)\,(R)\,(N)}$,

where N is defined as Fvco/Fdata (i.e., N = 8/1). R is the effective gain setting resistor which determines the charge pump reference current.)

For minimum data frequency tracking, for example the 8T pattern (which is the lowest allowed data frequency for the 2, 7 RLL code where one data pulse occurs within an 8 VCO clock period span),

$Wn(min) \equiv Wn(8T) = \sqrt{4T/8T}\,[Wn(4T)] = 471\text{ krad/s}$

Similarly at maximum data frequency, as in a 3T pattern, Wn(max) in data field becomes 769 krad/s.

To calculate for the loop filter component values, the above general expression for Wn is transposed to obtain the following equation:

1. $C1 = (2.5)(Fvco)/[(Rrate)(N)(Wn(4T))^2]$
   $= (2.5)(Fvco)/[(820)(4)(666E3)^2]$
   $= 0.034E\text{-}6$
   C1 = 0.03 μF, which is a standard capacitor value.
2. $R1 = 2\,\zeta/(C1)(Wn) = 2[\zeta(4T)]/(C1)[Wn(4T)]$
   $= 2(0.7)/(0.03E-6)(666E3)$
   $= 70.07$
   R1 = 68Ω, is a standard resistor value.
3. Choose $C2 \cong C1/50$. In general, selecting $C1/50 < C2 < C1/10$ will yield non-dominant parasitic pole and still allows C2 to integrate the current pulses. (Capacitor may be film or monolithic ceramic.)
   C2 = 560 pF

4. Recalculate Wn(8T) at minimum data frequency with standard component values: (For loop stability ζ(min) should not be allowed to be less than 0.5. ζ(min) occurs when Wn is at a minimum.)

$$Wn(8T) = \sqrt{(2.5)(20E6)/(820)(8)(0.03E-6)}$$
$$= 504 \text{ krad/s}$$

$$\zeta(8T) = (504E3)(68)(0.03E-6)/2$$
$$= 0.51$$

5. Recalculate Wn(4T) for data frequency in preamble acquisition with standard component values:

$$Wn(4T) = \sqrt{(2.5)(20E6)/(820)(4)(0.03E-6)}$$
$$= 713 \text{ krad/s}$$
$$\zeta(4T) = (713E3)\ (68)\ (0.03E-6)/2$$
$$= 0.73$$

6. Calculate the loop parameters for locking to the crystal frequency divided by 4 signal (N = 4). Normally a higher loop gain is employed. With the use of an additional charge pump current setting resistor (Rb) to boost loop gain during non-read mode, the damping factor may be chosen with $\zeta(4T-Xtal) \cong 1.0$ for critical damping during crystal acquisition.

$$Wn(4T-Xtal) = \zeta(4T-Xtal)(2)/(R1)(C1)$$
$$= (1.0)(2)/(68)(0.03E-6)$$
$$= 980 \text{ krad/s}$$

7. Calculate Rb from Wn(4T − Xtal):

$$Wn(4T-Xtal) = \sqrt{(2.5)(Fvco)/(Rr//Rb)(C1)(N)}$$
$$980E3 = \sqrt{(2.5)(20E6)/(820//Rb)(0.03E-6)(4)}$$
$$820//Rb = (2.5)(20E6)/(0.03E-6)(4)(980E3)^2$$
$$= 433.8$$
$$= (820)(Rb)/(820 + Rb)$$
$$Rb = 921.2$$

choose Rb = 910Ω, a standard resistor value.

Rp = 820//910 = 431.33, the effective charge pump current setting resistor value.

8. Recalculate Wn(4T − Xtal) with standard component values:

$$Wn(4T-Xtal) = \sqrt{(2.5)(20E6)/(431.33)(0.03E-6)(4)}$$
$$= 983 \text{ krad/s}$$
$$\zeta(4T-Xtal) = Wn(4T-Xtal)(Rp)(C1)/2 = 1.02$$

In general the customer may choose any suitable gain ratio between fast lock and stable data tracking. A 2:1 ratio is a popular choice; for example, Rr = Rb = 820Ω. In the above example this will make the damping factor and Wn(max) at crystal reference lock slightly larger. Note that we have chosen zeta, ζ, to be between 0.5 and 1.0 as a general guideline such that the system will not be excessively underdamped nor subject to excessive acquisition times. However, an experienced designer can choose other appropriate design values to tailor toward a specific system's requirements.

Note: There is a minimum value for Rr//Rb (parallel combination value) allowed for the DP8462. A maximum reference current limit for the charge pump is imposed such that Vbe/(Rr//Rb) ≤ 2 mA. This translates to Rr//Rb ≥ Vbe/2 mA ≅ 350Ω, typically, for Vbe ≡ 0.7V.

Hence, the above calculations yield the loop filter component values and their corresponding loop parameters for example #1 as follows:

10 Mb/s (2,7) Code	Rr	Rb	R1	C1	C2
	820Ω	910Ω	68Ω	0.03 μF	560 pF
Wn(8T)	ζ(8T)	Wn(4T)	ζ(4T)	Wn(4T − Xtal)	ζ(4T − Xtal)
504 krad/s	0.51	713 krad/s	0.73	983 krad/s	1.02

Another frequently used method for Wn determination is by graphical means. If damping ratio, ζ, and lock time are given, Wn can be arrived at via the normalized phase error versus Wnt plots. Alternatively, if the desired system response has been defined as specified in the example given below, Wn can also be readily determined.

Example #2: 7.5 Mb/s data rate with (2, 7) encoding and 4T preamble

Maximum peak overshoot $< 30\%$

Settling time $\cong$ 11 μs with phase error $\leq \pm 5\%$

VCO capture range within $\pm 20\%$ of 15 MHz and follow excursion of $\pm 5\%$ of Fo

Charge pump gain ratio = 2:1 between non-read and read modes, (Rr = Rb = 820Ω).

It is helpful to know the initial frequency offset for the derivation of Wn. But this information may be available to the customer and the exact value is not necessary to make a trial estimate for Wn. Fortunately, the maximum velocity variation of commercial drive mechanisms are well within 2% and current disc drives have guaranteed rotational tolerance of less than 1%. Hence, initial frequency step between non-read and read modes in normal operation does not contribute appreciably to the total phase-error transient resulting from a maximum phase step assumed in the calculation.

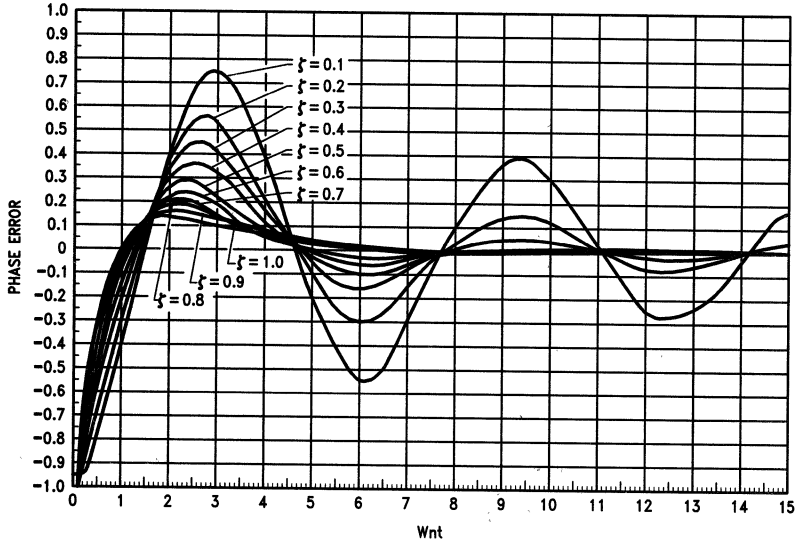
Wn can be derived from the Wnt vs. $\theta e(t)$ curves due to a phase step. *Figure 1* shows that the $\zeta = 0.5$ parametric curve meets the above requirement of maximum peak overshoot less than 30%. The residual phase error will be approximately -5% at Wnt = 6 rad. Therefore, settling to $\pm 5\%$ (or about 3 ns) in t = 11 μs yields:

Wnt = 6.0 rad

Wn(4T) = 6.0 rad/11 μs = 545E3 rad/s

This is the computed BW for preamble acquisition, which is then used to calculate the loop filter component values as in the previous example. The loop filter and parameter values are presented below:

Transient Response of 2nd Order Loop due to a Step in Phase



TL/F/9331–1

FIGURE 1

7.5 Mb/s	Rr	Rb	R1	C1	C2
(2, 7) Code	820Ω	820Ω	68Ω	0.039 μF	820 pF
Wn(8T)	ζ(8T)	Wn(4T)	ζ(4T)	Wn(4T−Xtal)	ζ(4T−Xtal)
383 krad/s	0.51	541 krad/s	0.72	766 krad/s	1.01

Note: The derived Wn value may be checked to verify for adequate capture range in the read mode. The value chosen does satisfy the expression $2\zeta(4T)Wn(4T) > \Delta W$(of 1.5%).

The above techniques are useful in estimating suitable loop filters which satisfy basic capture and lock conditions in non-read mode and read mode in preamble field. The conservatively derived component values should allow good performance in most applications. However, there are situations where significant improvement in system performance may be gained if the loop bandwidth is optimized with respect to a particular system. For example, to accommodate certain sensitivities to cylinder formats, media imperfections, or noise in gaps, etc., it may be necessary to raise or lower Wn considerably from the suggested values used in the above computations. In addition to the NSC suggested values in the datasheet and this note, the customer is strongly encouraged to modify those values or tailor a filter to achieve minimum error-rate.

The following table lists additional sets of loop filter component values which have performed well in the field or have been designed into systems:

LOOP BANDWIDTH OPTIMIZATION AND DESIGN CONSIDERATIONS

Numerous "optimized" loops have long been derived for various types and orders of PLL systems. Optimum loop transfer functions were formulated for different types of input stimuli. It is practically impossible to make a perfect loop as this will require continuous adaptation of the filter to compensate for the input changes as a function of time. The 2nd order loop (due to its ease of analysis) is by far the most popular and of the greatest interest to design engineers. The following list presents some design trade-off issues and several frequently encountered design and device evaluation considerations.

1. Narrow Bandwidth: Most designers will wish to keep loop BW low to improve noise rejection. This will decrease the loop's response to input jitter at the expense of having a smaller capture range. This can be very helpful in soft-sectored reading to desensitize the effect of write-splice induced perturbations.

2. Wide Bandwidth: If capture range exceeds frequency range within which the input signal is expected to vary, it increases the probability of spontaneous lock. Raising the loop's BW is recommended if the input frequency offset is sufficiently large.

3. Damping Factor: It is suggested that this should be set approximately equal to:

   0.5 for Wn(min) in read mode,
   0.7 for Wn(max) in read mode, and
   1.0 for Wn(Xtal) in non-read mode.

   (If a 4T preamble is employed, then Wn(max) in data field of 3T pattern is larger and the damping factor becomes slightly greater than 0.7.)

   A larger damping factor increases capture range which improves the probability of acquiring lock. It also increases total acquisition time.

   A smaller damping factor minimizes response to bit shift, but excessive underdamping will cause instability.

4. The open loop response of the chip can be modelled as a 2nd order PLL (highest power of s=2 in the denominator of the loop transfer function) with a parasitic 3rd pole.

$$G(s) = \frac{2.5(Fvco)\,(1+sR1C1)}{(N)(s^2)(Rr)(C1)(1+sR1C2)}$$

where Fvco = center frequency and N = Fvco/Fdata.

If the chosen physical parameters and component values are faithfully modelled by such an expression, phase-margin of the loop can be reasonably predicted. Phase-margin should be between 30° and 70° at unity gain. 45° is good compromise in general; this is the criterion for loop stability. Larger phase-margin produces a more stable loop, but it slows the response, increases VCO output unwanted sidebands, and reduces loop VCO-noise suppression capability.

TABLE I. Loop Filter Component Values

Data Rate (NRZ)	Rr	Rb	R1	C1	C2
5 Mb/s	820Ω	1.5 KΩ	75Ω	0.056 μF	820 pF
	820	2.2K	95	0.047	820
	370	∞	42	0.10	1600
7.5 Mb/s	820Ω	820Ω	62Ω	0.047 μF	1000 pF
10 Mb/s	820Ω	1.2 KΩ	82Ω	0.020 μF	510 pF
	820	820	62	0.039	820
	910	910	51	0.056	820

5. The effects of the loop filter component values can be summarized as follows for component optimization considerations:

   Increasing C1: (Lowers BW) desensitizes PLL from input bit jitter or frequency shift.

   Reduces possibility of spontaneous transient response to spurious signals in read/write gaps. Slows down loop response time. Reduces capture range.

   Increases loop sensitivity to VCO noise.

   Increasing C2: Reduces the rippling effect of the charge pump switching current which allows less loop response to shifted bits. Reduces stability margin.

   Increases (slightly) loop response to VCO noise. Increases response to write splice perturbation.

   Increasing R1: Increases stability margin. Decreases loop response to VCO noise.

6. An often asked question on PLL design parameters regards lock-up time. There is no simple expression that will adequately predict acquisition or lock times because of many factors that influence them and ambiguity of definition of lock. Lock time may be estimated roughly from "Wnt vs. phase-error" normalized curves if loop parameters are defined or known (see *Figure 1*). The following lists several factors that contribute most to the variation in lock times. This information offers some insight into lock time interaction with respect to the DP8462 PLL and its environment. Customer should be aware of them in order to realize good designs.

   a) Initial phase difference between input & VCO comparison pulses.

   b) Initial state of the VCO divided by 3 or 4 counter.

   c) Initial input frequency offset.

   d) Low pass loop filter characteristics (BW and damping).

   e) Center frequency (VCO) accuracy and symmetry.

   f) VCO noise and sideband signals.

Note: Although customer has no control over a) and b), their impact can be minimized through loop filter design.

7. Another frequently asked question is how to measure lock ranges and capture ranges. A few methods are suggested below:

   Lock range is the maximum input frequency-ramp excursion (upper and lower bound) permissible while the loop still maintains lock. To measure lock range, apply a square wave pulse train of known frequency to the ENCODED DATA input of the PLL chip. Allow the PLL to be stably locked onto the periodic input waveform. While in read mode measure either the SYNCHRONIZED DATA or VCO output for good synchronization to the input as its frequency varies until lock is lost. It is recommended to set Read Gate low momentarily after each measurement.

   For the capture range determination, continuously cycle Read Gate as in above (always allow sufficient time for the PLL to lock to the 2F reference clock). Start with the PLL in lock, gradually increase the frequency of the input data stream until the PLL will not lock, then readjust the frequency towards the center frequency until locking is achieved again at a particular frequency. This frequency is the upper capture frequency. Repeat this procedure for the lower boundary to determine the lower capture frequency.

Note: A noisy analog instrumentation tuning mechanism may produce undersirable transients that disturb the PLL and give false data. Always make very slow and gradual adjustments. Improper toggling of the Read Gate or insufficient deassertion time may result in lock problems during read mode.

OPTIMIZING THE DECODE WINDOW:

In the past, the Twindow A.C. specification in the datasheet was not well understood and has caused misinterpretation by some customers. This specification simply indicates the maximum truncation of the available half decode-window width (one side of nominal window). For a given data rate, an ideal window boundary is defined for the data bit. The entire (ideal) window width can rarely be made available due to noise, device tolerance, and process or other related physical imperfections. The PLL chip, therefore, contributes a total window loss equal to twice the Twindow time stated in the Twindow specification. Basically, there are two mechanisms that are responsible for this loss. First, is the dynamic uncertainty arising from the superposition or modulation of noise and phase movement from internal and external sources that effectively narrows the usable window size. The second, and dominant mechanism, is the deviation of chip produced window center from the theoretical center of the data window. This is caused by non-ideal on-chip device matching due to process related variations during device fabrication. This deviation is sometimes called "window-margin". Our Twindow specification, in effect, lumps all contributing factors of window jitter and displacement within the PLL data synchronizer into a single specification which corresponds to the amount of maximum half-window loss. This figure can be determined empirically using a specific set of external passive components and test conditions following complete PLL lock and stabilization. (This will be explained in the next section.)

As suggested in the datasheet, bit jitter tolerance can be improved by adjusting the window center via the PG2 and PG4 pins. There have been no fewer than 3 different current splitting networks employed to adjust the internal silicon delay line to improve the phase margin. (The adjustments are internally compensated for Vcc and temperature variations.) The various network configurations, whether chosen for test convenience or for layout topolgy reasons, are fundamentally equivalent and achieve the necessary bias. They should yield the same final result of centering the data bits within their respective windows. It should be pointed out that we are by no means requiring the user to employ the extra task of trimming during manufacturing to accomplish margin improvements as may be misinterpreted from drawings depicted in the datasheet. Our intention is to illustrate to the users the fact that by selecting an appropriate resistor (fixed) value for RPG4, as in *Figures 2a* and *2b*, one can obtain better Twindow tolerance than specified in the datasheet. For example, the DP8462-3 part type guarantees at most 6 ns of static window loss at each window boundary. But, via an RPG4 of approximately 2.2k to 3.4 kΩ, the window loss can be significantly reduced by 60% or more.

We do see customers who must regain as much margin as possible from up-stream erosions that may be hard to control or correct. This is particularly the case for OEM customers whose electrical and/or mechanical recording compo-

nents in the read channel are usually off-the-shelf items and their integrated spec may not be as optimal as desired. To alleviate such constraint, an extra, but simple, step is added to perform a fine RPG4 selection. For 10 Mb/s operation, 1.5 ns or less of static window loss from each side (from a 50 ns window width) can be achieved with data bits perfectly centered around the expected data window. The graph in *Figure 3* is a plot (represents several lots of DP8462-3 units) of typical RPG4 values vs. the amount of bit shift allowable. The data rate is 10 Mb/s and (2, 7) code with 4T preamble is used. The chip operates under a specific set of operating conditions and support components. The curves show that the absolute value of the average decode window width is 47 ns (sum of T-early and T-late times for any RPG4 value shown.) The cross-over point indicates where T-early equals T-late. The RPG4 value at this point will allow the data bit to be symmetrically centered about its decoding window.

Note that only the phase-shift is being gauged, that is, the actual deviation of the data pulse under test from the theoretical center of the data window. Hence, the plot also indicates that the customer may "program" (via an external current source or resistors and switches) a wide range of bias conditions on PG4 pin to perform margin tests on the read channel for final test in manufacturing or for Early/Late strobing techniques used in certain data recovery procedures.

In general the RPG configuration for window deskewing as depicted by *Figure 2C* is preferred. RPG2 is fixed at 1.5 kΩ and RPG3 may be selected proximately between 300Ω to 500Ω. This configuration offers optimum component tracking between the RPG resistors.

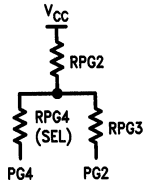


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FIGURE 2a

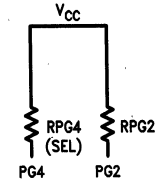

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FIGURE 2b

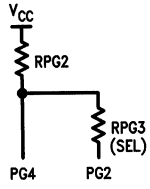

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FIGURE 2c

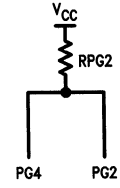

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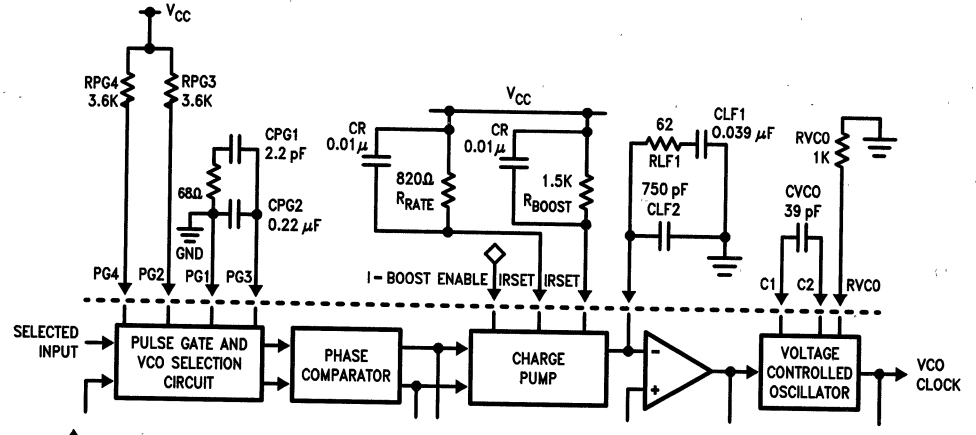
FIGURE 2d



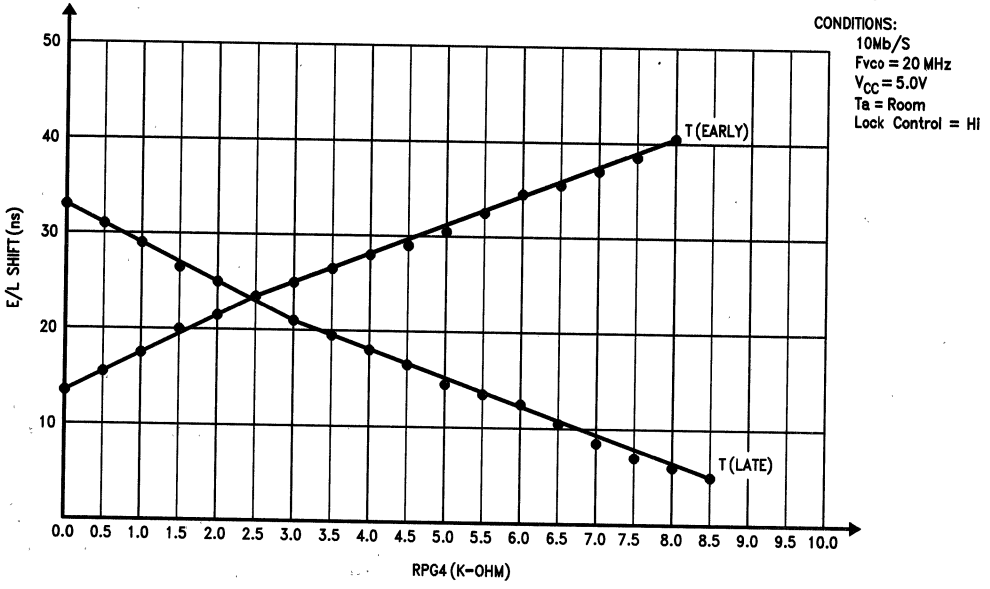


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FIGURE 3. DP8462 Early/Late Window Shift vs RPG4

Note: There is a datasheet change to the DP8462-3 part type (Aug. 1, 1986) which pertains to the test method used to qualify the Twindow spec. The parametric value which appears in the AC Electrical Characteristics table of the datasheet has not been changed. For testing the window, the original configuration required the PG2 and PG4 pins to be tied together and connected to a 1.8 kΩ, RPG2, resistor to Vcc *(Figure 2d)*. This configuration is still used for testing the DP8462-4. For testing the DP8462-3, one 300Ω resistor will be palced between the PG2 and PG4 pins and PG4 will be tied to Vcc through a 1.5 kΩ resistor *(Figure 2c)*. Note 6 in the datasheet will now read:

"This specification is guaranteed only for the conditions under which the parts were tested. However, significant variation from formula is not expected for other data rates and filters. The DP8462-4 specification is for the condition when PG2 and PG4 are tied together. The DP8462-3 specification is for the condition when a 300Ω resistor is tied from PG2 to PG4 and a 1.5 kΩ resistor is tied from PG4 to Vcc. External adjustment can be used to optimize Twindow as described . . . "

PRINTED CIRCUIT BOARD LAYOUT GUIDELINES:

Other than a true Digital Phase Locked Loop (DPLL), any type of analog PLL is inherently a sensitive device. Hence, the environment in which it is operated should be optimized wherever possible to improve reliability. The following is a list of PCB layout recommendations that should help to minimize the effects of VCO jitter or mislock ocurrence that can be caused by various external sources of disturbance:

1. Establish a local Vcc island or net, separate from the main Vcc plane, to which the device and its associated passive components can be connected to remove unwanted noise coupling. Vcc supply filtering should be liberal and in very close proximity to the PLL chip. The device is sensitive to inadequately filtered switching supply noise. All lead lengths of the filter capacitors between Vcc and ground pins should be as short as possible to minimize lead inductance. Inclusion of a quality high-frequency capacitor, such as a 1000 pF silver mica capacitor, in parallel with a 0.1 μF ceramic capacitor is recommended.
2. Effective capacitive bypassing of the Rrate and Rboost pins (#2 and #3) directly to the Vcc pin is very important. Again, use quality high-frequency capacitors and maintain the shortest possible electrical lead length.
3. Use the main digital ground plane for all grounding associated with the device. The ground pins and the PG1 pin should tie directly to this plane.
4. Do not locate the chip in a region of the PC board where large ground plane currents are expected.
5. Locate all passive components associated with the chip as close to their respective device pins as possible.
6. Orient the chip's external passive components so as to minimize the length of the ground-return path between each component's ground plane tie point and the chip's ground pin.
   Note: Ground noise at the loop filter components, R1, C1, and C2 which is not identically present at the ground pin (common mode), is coupled through the filter components into the VCO control voltage pin.
7. Include no planing whatsover (Vccc or ground) directly between adjacent pins. This will minimize parasitic capacitance at each pin. Planing between the two pin rows, however, is recommended (directly beneath the package).
8. Avoid running signal traces between pins to avoid unwanted noise coupling.
9. Run no digital signal lines between or adjacent to the analog pins or signals traces (pins #1 to #7 and PG3) in order to avoid capacitive coupling of digital transients.
10. Minimize the total lead length of the Cvco capacitor. Inductance in the path degrades VCO performance, as does parasitic pin capacitance.
11. Do not place any bypass filtering at the Rvco pin (minor coupling of the VCO waveform into this pin is normal and acceptable).
12. Eliminate negative-going voltage transients (undershoot) at the digital input pins (pre-termination of driving lines may be necessary) to avoid drawing transient input-clamp-diode current from the device pins. Negative undershoot at the 2F Clock and the Encoded Data inputs should be removed to avoid excess VCO phase movement and window margin degradation. A damping resistor in series from the driving circuitry is recommended (typically 200Ω will be sufficient depending on the characteristic impedance of the path).
13. Minimize digital output loading (VCO, Phase Comparator Test, and Synchronized Data); i.e., if such outputs must drive large loads or long lines, employ buffers.
14. Allow unused digital output pins to float, unconnected to any net.
15. Avoid locating the chip within strong electromagnetic fields. If possible, choose the "quietest" region of the PC board.
16. If chip socketing is desired, use a low-profile, low mutual capacitance, low resistance, forced-insertion type (gold plated socket-strips are recommended). In general, avoid the use of "ZIP-DIP", zero-insertion-pressure sockets. If there is a need for them such as in batch testing of devices, the new low-profile "ZIP" sockets may still be used with acceptable results. The supporting passive components must be soldered directly under the socket pins with virtually zero lead length allowed.
17. Do not use wire-wrap interconnect, even in an evaluation set-up. Point-to-point wiring is acceptable, but the prototype board must have (or improvise) a decent ground plane or strips and Vcc nets.
18. Make allowance for pin-to-pin capacitance when determining Cvco (typically 4 pF to 5 pF) from datasheet formula.
19. When using PCC (plastic chip carrier) package, space for passive component connection to the device will be considerably tighter. It is acceptable to have axial-lead resistors (not capacitors) standing upright, but, the shorter lead must be connected to the device pins to obviate noise induction to sensitive nodes.
20. In multi-layer PCB layout, as in miniature board designs for small drive systems, do not allow any power planes to run into the device region to prevent introducing unwanted noise into the chip.
21. The crystal oscillators may be designed with CMOS inverters such as the 74HC04. If the device gain is too high for the circuit, proper oscillation may not occur. As an alternative, use National's unbuffered 74HCU04 instead (which may require different capacitor values for the oscillator).

EVALUATION BOARD FOR THE DP8462

An example of a good PCB layout is portrayed by the artwork for the DP8462 evaluation PC board in *Figure 4*. This hardware simplifies the task wherein customers evaluate and correlate devices. This evaluation/demonstration board is a compact, convenient, self-contained test set-up with the following features:

— Housed in a compact, pocket-sized PCB

— On-Board programmable data pattern generator

— Self-contained movable-bit generator with continuous adjustable bit delay time and pulse width. Operates to 25 Mb/s data rate.

— Two (2) independent 2F frequency oscillator sources on board for 2F Reference Clock and for clocking the data pulses.

— Four (4) selectable Early/Late strobe settings for window shifting tests; one range is made variable for fine tuning experiments.

— Programmable Lock-Control and Preamble-Select (3T/4T) selections.

— Reference bit and sync-bit pulse output for convenient measurement and triggering needs.

— Direct outputs to ratio counter for monitoring during window margin tests.

First, within the following discussion the method used by National for window testing (manufacturing) will be explained. Secondly, it will be shown how this compact hardware has the ability to perform similar evaluations in a laboratory bench set-up.

WINDOW TEST PHILOSOPHY

The test method used to determine the data synchronizer's tolerance to bit shift is explained below. Test procedures and test hardware have been developed to measure the device A.C. performance. These can easily be ascertained and correlated by any customer regardless of their application specifics. In customers' applications, signal sources may be quite different; they can range from magnetic or optical media, to transmission lines (as in token rings). In each case, the method of pulse detection requires different techniques. Therefore, in order for every customer to be able to agree upon a representative figure of merit, we stipulate a "Static Window Margin Test" method. Consequently, for correlation purposes, the window margin test of the PLL chip must not be tested in the system environment. Furthermore, the input signals to the PLL should be supplied from a stable word generator or equivalent source and not from the read outputs of any disc or tape drive system (the PLL chip, not the signal source, is under investigation). In addition, a fixed set of passive components is used for each data rate of interest. In this manner, a controlled condition is established which removes any ambiguity; correlation of Twindow data can thus be performed confidently.

Refer to the timing and test sequence flow diagrams in *Figures 5* and *6*. The A.C. screening test is as follows: The device under test is first powered-on and set in the non-read mode. It will remain in this mode for 200 VCO cycles to allow the PLL to acquire a stable lock to a crystal 2F reference source. The device is then switched to the read mode by asserting the Read Gate input to a logic high level. This causes the internal input multiplexer to switch the PLL input from the crystal 2F reference source to the encoded preamble data pattern which is asynchronously derived from a signal pattern generator. (The preamble pattern is a string of 1-0-0-0 . . . , 4T preamble.) The PLL usually can lock onto the encoded data in less than two bytes of sync pattern. When 16 consecutive preamble bits are validated by the internal detection circuitry, the Preamble-Detected output becomes active-low, indicating lock has been achieved. The preamble continues for a minimum of 200 VCO cycle times after Read Gate assertion to ensure the device will be very stable prior to the window margin test.

When inserting the movable test bits following the last preamble bit, it is necessary to suppress at least as many data pulses (missing bits) as the coding scheme requires before inserting either the Early or Late test bit to avoid interference from an adjacent pulse. The code must not be violated even if the movable bit is allowed to be shifted into an adjacent window. In the 5 Mb/s example, in *Figure 6*, the amount of decode-window loss is determined by shifting a test bit toward the window center starting from 10 ns outside the nominal window boundary. The bit will be moved across the window boundary toward the nominal window center in incremental steps until it resides in a position where it will be recognized by the device under test as being in the appropriate window for a large number of sequential read operations. For a device which passes specification, the movable bit will move no closer to the nominal window center than 40 ns (the ideal half-window width (50 ns) minus the Twindow spec. (10 ns)), before the bit falls into the proper decode window. Hence, the Early test bit begins at 10 ns away from (outside) the left side of the nominal window boundary and moves toward the center of the window by 1 ns increments until the corresponding Synchronized Data output is found at its expected location. Similarly, the Late test bit approaches from the right hand side of the nominal window boundary starting at 10 ns outside the boundary and shifts toward the window center. An automated tester used in manufacturing verifies that the Synchronized Data output and the shifted test bit input waveforms are in their respective valid locations for 100 consecutive successful operations (a test time versus confidence compromise). Parts that exhibit less than 6 ns of window loss from both the front (Early bit) and the back (Late bit) window tests at a 10 Mb/s data rate are designated −3 graded parts. Devices with window truncation of less than 10 ns at 5 Mb/s data rate are designated as the −4 grade part-type.

Device specifications are:

DP8462-4 → Twindow Tolerance = 10.0 ns
DP8462-3 → Twindow Tolerance = 6.0 ns

DP8462 Evaluation PC Board Layout

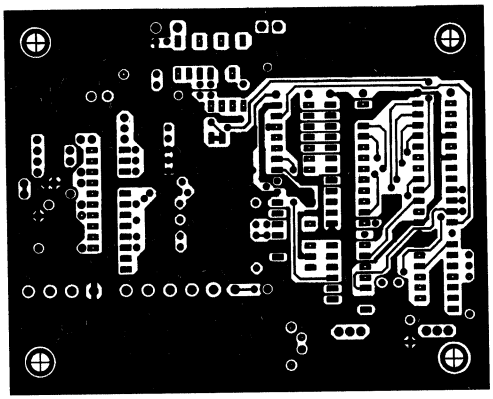

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FIGURE 4a. Component Side with Ground-Plane

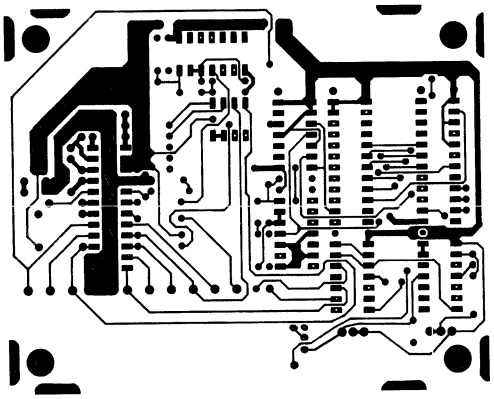

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FIGURE 4b. Trace Side, Bottom View

AC Test Sequence Flow Diagram

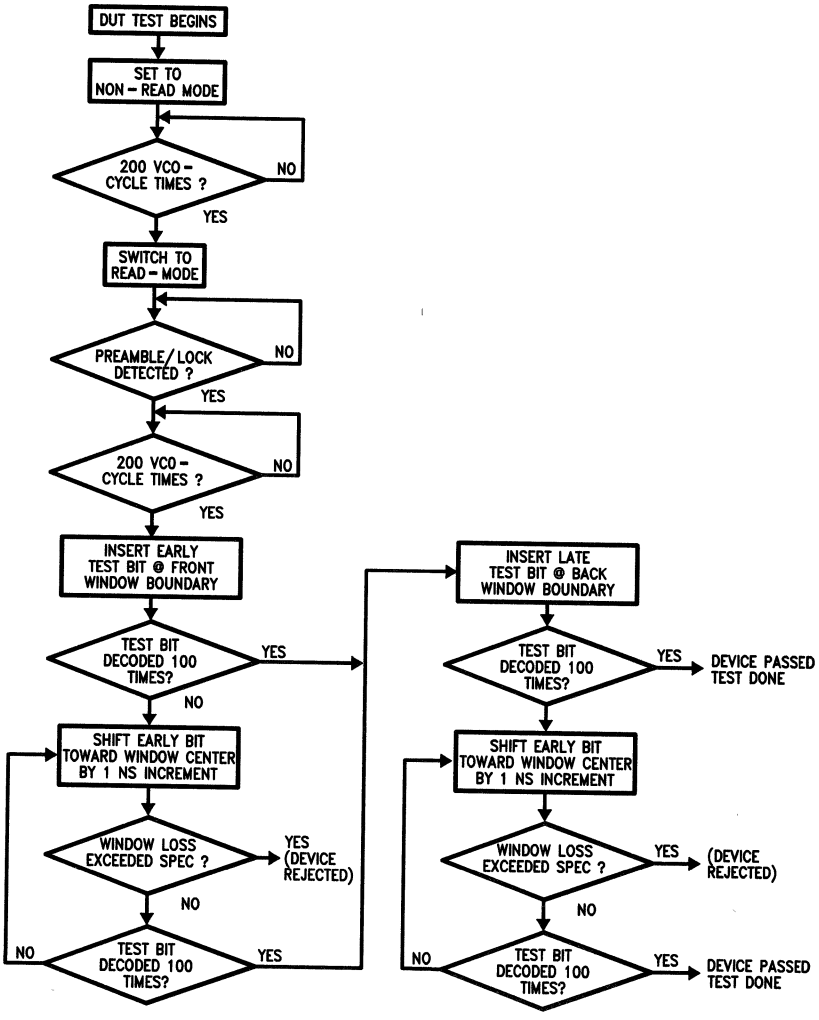

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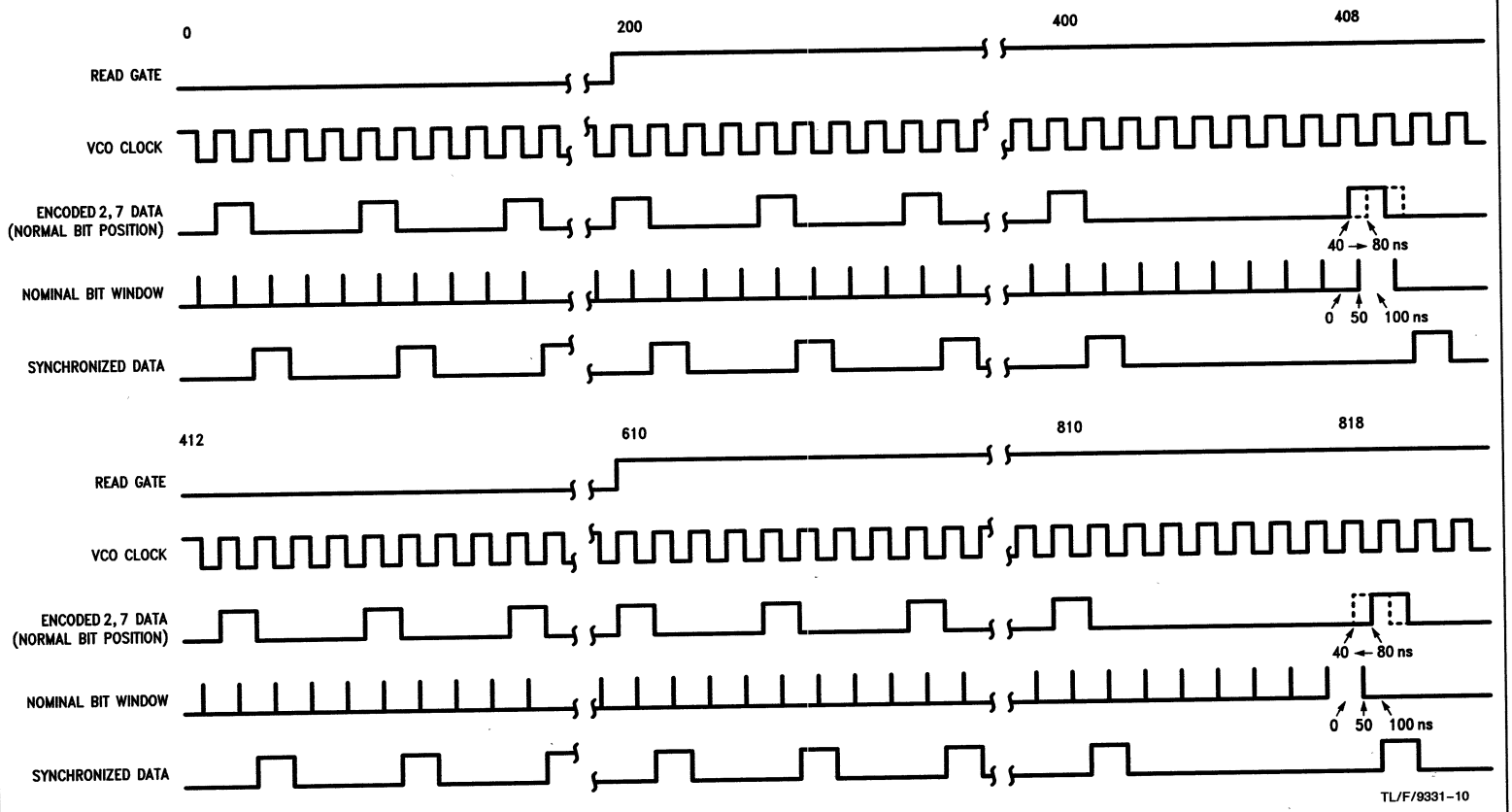
FIGURE 5



***** DP8462 AC TEST TIMING DIAGRAM (5 Mbit/s) *****

VCO = 10 MHz, Preamble is 4T
Rr = 750 Rb = 1600 R1 = 200
C1 = 0.02 μF C2 = 150 pF

FIGURE 6

DP8462 EVALUATION BOARD CIRCUIT OPERATION

The DP8462 evaluation board mentioned above performs the equivalent test sequence as in automatic testers. However, it does not require elaborate pattern generators and measurement systems, or a software contorlled sequencer. Only a calibrated oscilloscope and possibly a digital ratio counter are needed to monitor the device under test. Refer to the schematic diagram in *Figure 7* and the timing diagram in *Figure 8*.

One half of U4 and U6 together form a 9-bit synchronous binary counter to cycle the address lines of U8, a read-only memory that contains all the appropriate test patterns for the Twindow test. U7 is a high speed AS (Advanced Schottky) gate used to buffer and gate the U8 ouputs to the PLL chip. U2 and U5 are CMOS inverters used to construct two crystal oscillators. One oscillator generates the 2F Reference Clock while the other sequences the rest of the logic chips. U9, a monostable multivibrator, is used to set the pulse width of a single movable bit within the Encoded Data pattern string. Q1 and its associated passive components realize a linearly variable threshold adjustment that is capable of continuously skewing the movable bit about its window center position. The other half of U4, with an "OR" gate of U7 and together witth U8, set up a detection window for the synchronized bit associated with the corresponding movable test bit. If the test bit is within the correct decode window position, pin #6 of U7 will yield 2 pulses in every read cycle. If the test bit falls out of its expected window only a single pulse is produced from this output of U7. Hence, this output and Read Gate can be connected to the ratio counter inputs for an accurate display of when the bit is within or outside of its expected window. The time measurement system in a laboratory oscilloscope can provide accurate Twindow readings.

DP8462 Evaluation Board

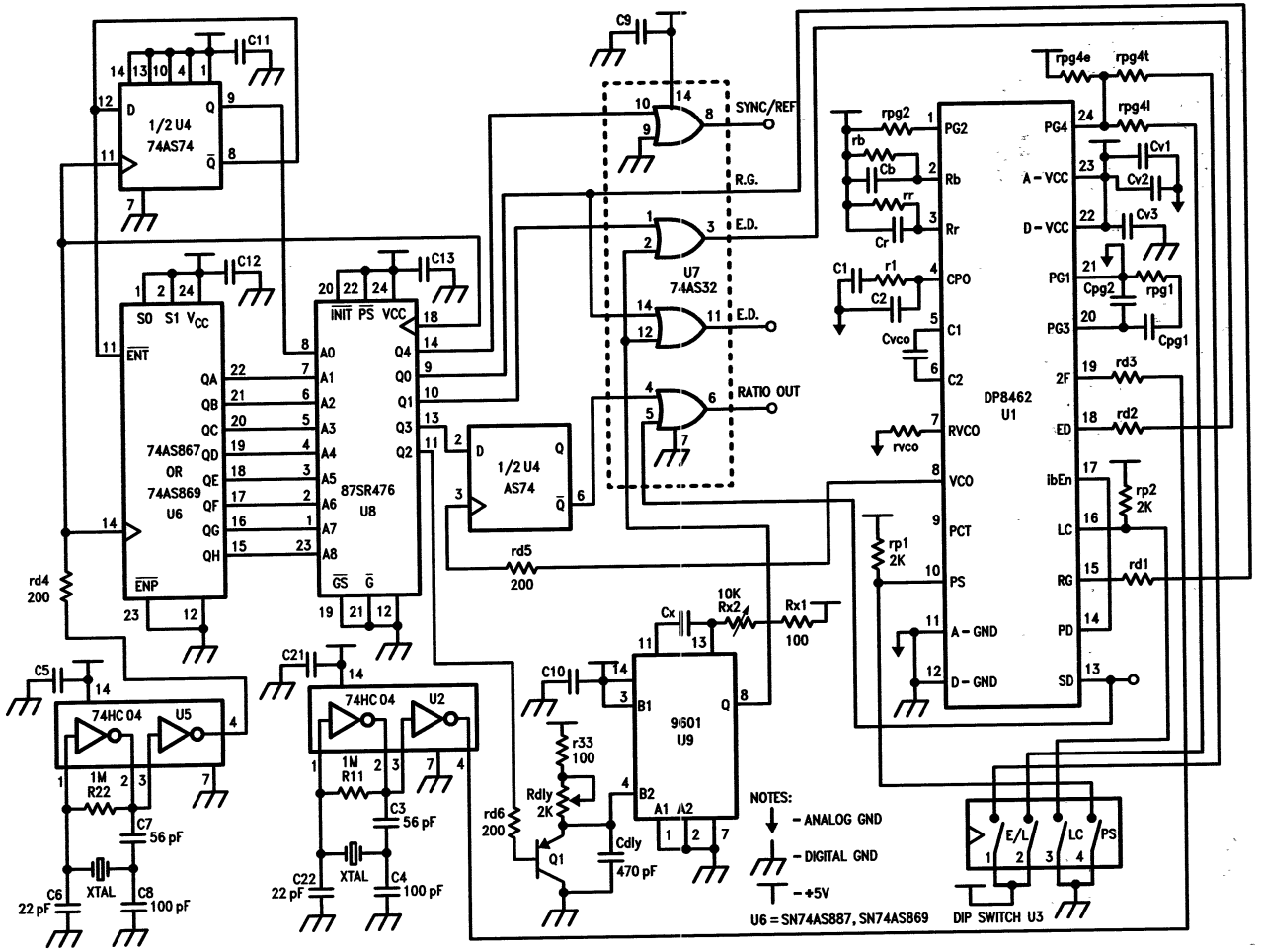


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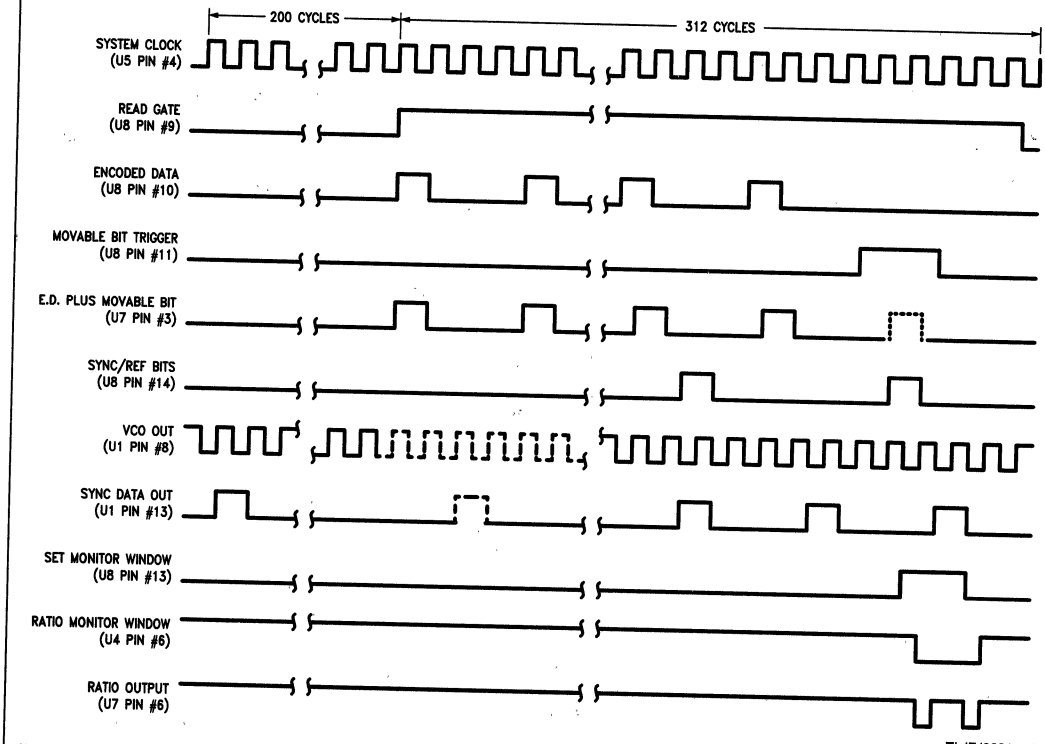
FIGURE 7



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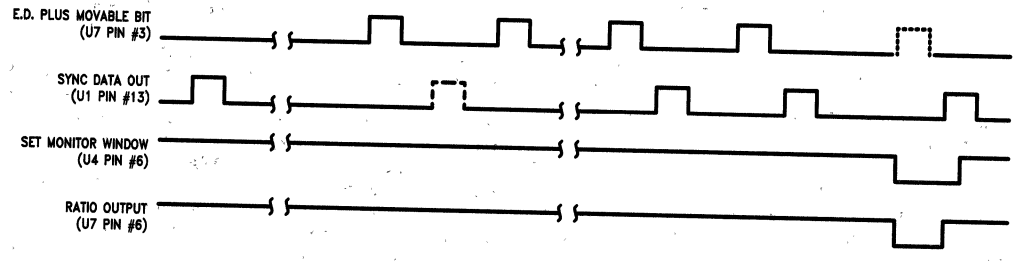
If movable bit is shifted outside of its expected decode window position:



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***Note:** Dotted waveforms depict movable bit signal positions; broken waveforms indicate outputs not yet stabilized after read gate assertion.

FIGURE 8. Essential Waveform Diagramatic Representation of the DP8462 Evaluation Board

The variable resistor, "Rdly", is used to shift the test bit about its window center. "Rx2" is used to adjust the pulse width of the movable bit, which should be set equal to the width of the Encoded Data pulses from the pattern generator ROM. U3 consists of 4 switches used to set Lock Control, Preamble Select, and to select different currents supplied to PG4 to control window centering or to introduce a predetermined amount of early or late shift of the window.

EVALUATION BOARD PREPARATION

Below are listed the component values currently being used by NSC for production testing at 10 Mb/s. (Values may change without notice.)

Rvco = 1.00 kΩ	Rr = 800Ω
Cvco = 39 pF	Rb = 1.8 kΩ
Cv1 = 0.1 μF	R1 = 82Ω
Cv2 = 1000 pF (Silver Mica)	C1 = 0.02 μF
Cv3 = 1000 pF (Silver Mica)	C2 = 510 pF
CPG1 = 2.2 μF	Cr = 0.01 μF
CPG2 = 0.22 μF	Cb = 0.01 μF
RPG1 = 68Ω	
RPG2 = 1.8 kΩ (DP8462-4), = 1.5 kΩ (DP8462-3)	(See *Figures 2c & d*)
RPG3 = 0.0Ω (DP8462-4), = 300Ω (DP8462-3)	
RPG4 = 0.0Ω	

The circuit described in *Figure 7*, for evaluation of the DP8462 PLL, uses the same components as above except for RPG2 = 3.6k, RPG3 = 0, and RPG4 = Rselect. Refer to *Figure 2b*.

The center frequency of the VCO may be checked according to the datasheet (under VCO section description). It can also be conveniently confirmed by another simple technique. First, set CPO (pin #4) at ground potential and measure the VCO frequency (minimum frequency). Then apply approximately 3V to pin #4 and again measure the VCO frequency (maximum frequency). The arithmetic mean of these two measured frequency values yields the equivalent center freqency (choose appropriate Cvco value to ensure proper VCO center frequency).

Before powering up the evaluation board, notice that the circuit has been designed so that it is possible to provide each section of the test circuit, the DP8462 (via Vcc1), the 2F Clock oscillator (Vcc2), and the rest of the digital circuitry (Vcc3), with an independent +5V regulated supply. After power(s) has been on, first check U2 and U5 for proper 2F frequency outputs. If either one or both crystal oscillators appear to exhibit excessive jitter, abnormal oscillation or is being perturbed by the other oscillator, it is possible that the gain of the inverters used is too high. Replace the 74HCO4 device or use the unbuffered device, the 74HCU04, instead; (may require new capacitor values). Next monitor U8 to make certain that all the test patterns are present (refer to *Figure 8*). Trigger an oscilloscope with the SYNC/REF BITS output and display this waveform on the CRT also. Pin #8 of U7 should present two pulses, a sync bit followed by a reference bit from Q4 of U8. Q0 of U8 is the Read Gate sequence, which should be high for 312 2F Clock cycles and low for 200 2F Clock cycles. Pin #3 of U7 outputs the Encoded Data pattern from Q1 of U8. Q1 of U8 consists of a train of 4T patterns starting when Read Gate is asserted. At the end of the 4T patterns there should be an isolated pulse (movable bit). Adjust the Rx2 potentiometer so that the width of this isolated pulse matches those of the 4T pattern (or the reference bit). Also adjusting "Rdly" should be able to shift this pulse. Position this bit such that its leading edge aligns perfectly with the leading edge of the reference bit (refer to *Figure 8*). This alignment procedure puts the movable bit in the nominal center of its decode window. Q5 and Q6 (pins #15 and #16) of U8 are optional sync signals for triggering the oscilloscope to monitor other areas of the test sequence.

TEST PROCEDURES

Set "DIP" switches: SW-3 for LOCK CTL to (H) for phase-frequency mode during preamble acquisition; SW-4 for Preamble Select to (H) for 4T preamble; SW-1 and SW-2 both set to (L), this selects RPG4E = 3 kΩ on the board (or whatever value the user chooses in testing). Check SYNCHRONIZED DATA and VCO outputs, they should be stable and in lock by the arrival of the SYNC/REF bits (at least 200+ VCO cycles after Read Gate assertion).

To test the available half-window width (complement of the half-window loss), begin turning 'Rdly" slowly while monitoring ENCODED DATA, SYNC/REF BITS, SYNCHRONIZED DATA or RATIO OUT. (It is recommended to connect READ GATE and RATIO OUT to a digital ratio counter). The ratio counter normally reads a perfect 2.0000 ratio when the test bit is within its proper decode window. Move the test bit away from its centered position (with respect to the Reference Bit positive edge) in either direction. As long as the test bit remains inside the available decode window, a ratio of two is displayed on the counter. When the test bit begins to fall outside of its decode window even occasionally, the ratio count will deviate from a perfect two ratio, indicating the window boundary has been reached. Measure the time span between the leading edge of the movable bit and that of the reference bit which corresponds to the available half-window width. Subtracting this figure from 25 ns (for 10 Mb/s data rate) yields the Twindow number (half-window truncation). Repeat the same procedure for the other half of the decode window. If a ratio counter is not used one can monitor the SYNCHRONIZED DATA or RATIO OUT node on the oscilloscope screen. As the pulse is shifted towards the adjacent window position it will begin to fade; this is the point where the window measurement should be made. This alternate test also gives a reasonably accurate estimate of the Twindow specification.

Switches #1 and #2 of U3 along with the various RPG4 components have been selected for the user who desires to experiment with early/late strobe or select RPG4 in a system design for minimum window offset. To experiment with these different options this procedure is as follows (for 10 Mb/s transfer rate): Refer to *Figure 9*.

1. Choose RPG4E ≅ 6.2 kΩ, RPG4T ≅ 620Ω, and for RPG4L select a 5.0 kΩ potentiometer. (These values may be slightly different for other data rates.)
2. Set switches #1 and #2 to (H), this selects RPG4E only. With a relatively large resistor value, a low level bias current is allowed to the PG4 pin. This produces a wider LATE window (w.r.t. nominal bit position) and a correspondingly smaller EARLY window.

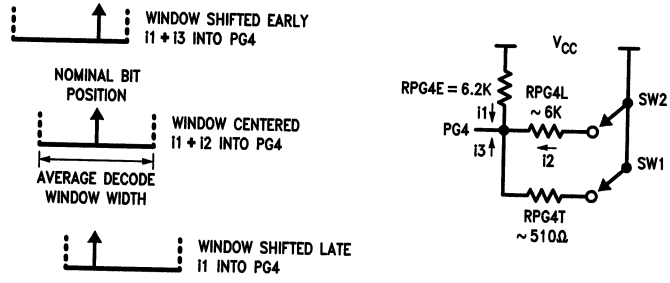


FIGURE 9

3. Set switches #1 to (L) and #2 to (H), this selects RPG4E and RPG4T in parallel. The effective RPG4 value will be the smallest of all the combinations of RPG4 resistors, hence, a larger bias current into PG4. This yields a wider EARLY window and a narrower LATE window (w.r.t. nominal bit position).
4. Set switches #1 to (H) and #2 to (L), this will select RPG4E and RPG4L; the combined value nulls out the window offset (on-time). For an easier set-up, one can utilize a single potentiometer for RPG4L (delete RPG4E and RPG4T) to determine an optimum RPG4 resistor value to nullify any inherent window offset.

SUMMARY

The DP8462 PLL chip is the third circuit in the family of National's second generation high performance data synchronizers. It combines the features of the DP8461 and DP8465 for non-harmonic phase detection in the non-read mode (DP8461 and DP8465) and in read mode during preamble acquisition (DP8461), and harmonic phase detection in read mode. Furthermore, in the DP8462, these mode selections are user controlled. Analog and digital Vcc and ground are brought out to separate device pins which further minimizes phase jitter and internal interference. Window center offset is also reduced or can be nulled out in design with a fixed external resistor. These improvements have significantly eased the task of design and volume production of higher transfer rate systems (data rates of 10 Mb/s to 15 Mb/s), where the data windows are proportionally smaller. The DP8462 device is part of National Semiconductor's DP8460 Series Disc System Data Path Chip Set. It has been designed into many disc drives and controller systems worldwide in conjunction with other members of this family such as the DP8464B pulse detector, the DP8463B (2, 7) ENDEC CHIP; the DP8466 DDC, and the DP8475 SCSI controller.

For further information regarding the DP8462 and the DISK DATA PATH chip set, please refer to National's "APPS Handbook Volume 1: Mass Storage".

ACKNOWLEDGEMENTS:

The author wishes to thank Bill Llewellyn and Pat Tucci for their constructive criticisms and diligent proofreading on this application note.

Designing with the DP8465

National Semiconductor
Application Note 416
Kern Wong

GENERAL DESCRIPTION

The DP8465 is a second generation of the successful DP8460 high performance PLL integrated circuit family of data separators/synchronizers. Like its predecessor, the DP8460, it consists of a proprietary pulse-gate which features an accurate silicon delay line, an edge-triggered digital phase comparator, a high speed matched charge pump, high impedance buffer amplifier, and a temperature compensated stable voltage controlled oscillator (VCO). The DP8465 also contains MFM decoder, missing clock detector, and lock-detect control circuitry for added flexibility to the system designer. There is one difference between the DP8460 and the DP8465. The DP8465 has been designed to perform PHASE FREQUENCY COMPARISONS during the non-read mode and switches to phase comparisons only when in the read mode, whereas the DP8460 employs only phase comparisons in both the read and non-read modes. This enhancement eliminates the possibility of false lock to the reference signal during a power-up sequence or when returning from a read operation. The DP8465 is 100% pin-for-pin and function-for-function compatible with the DP8460. It is a direct replacement for the DP8460 part type.

CIRCUIT OPERATION

The DP8465 is in the non-read mode whenever the READ GATE is deasserted. The 2F REFERENCE CLOCK input is divided by two and transmitted to the READ CLOCK output via a multiplexer. In this mode the VCO is locked onto the 2F CLOCK, keeping the VCO close to the data frequency in anticipation of locking onto the actual data stream. During the non-read mode PHASE-FREQUENCY COMPARISONS are employed, thus eliminating any possibility of false lock.

When the READ GATE input goes high, the DP8465 enters the read mode after a selectable delay time. This may be either one or thirty-two VCO clock cycles. The 2-byte delay is useful in hard-sectored drives for allowing a gap pattern to pass before the PLL locks onto the data. Soft-sectored drives do not need this delay. Once in the read mode, the PLL reference input is switched from the 2F CLOCK source to the ENCODED DATA input. The PULSE GATE allows a reference signal from the VCO into the PHASE COMPARATOR only when an ENCODED DATA bit is valid, thus PHASE-ONLY comparisons are made. The PLL, initially in the high-tracking mode, then attempts to quickly lock onto the repetitive encoded preamble.

By careful selection of the loop filter components, it takes less than one byte time for the VCO to lock onto the data stream sufficiently for preamble detection to begin. As soon as 2 bytes of the selected (ones or zeroes pattern) preamble are detected, the $\overline{\text{LOCK DETECTED}}$ output goes low. In a typical disk drive application, the $\overline{\text{LOCK DETECTED}}$ output may be directly connected to the $\overline{\text{SET PLL LOCK}}$ input. A low level on the $\overline{\text{SET PLL LOCK}}$ input causes the PLL CHARGE PUMP to switch from a high to low tracking-rate. At the same time the source of the READ CLOCK signal is switched from the 2F CLOCK input to the VCO clock. The MFM decoder also becomes enabled and begins to output decoded NRZ data. If the DP8465 is employed as a data-separator for MFM encoded data, the READ CLOCK output and the NRZ READ DATA output (which is synchronized to the READ CLOCK) may be used. These signals can be connected directly to a Disk Data Controller such as the DP8466 which controls Winchester or floppy disk drives. The MISSING CLOCK DETECTED output can also be utilized for MFM-encoded data in soft-sectored disk drives. It should be noted, however, the circuit is designed only to recognize a missing MFM clock-bit which is framed by two existing clock bits. In order to insure the detection of an address mark, simultaneous monitoring of the NRZ output for an "A1" hexidecimal code and the MISSING CLOCK DETECTED output for a single pulse within the same byte time is necessary.

When the READ GATE goes low, signifying the end of a read operation, the PLL reference signal is switched back to the 2F CLOCK, the $\overline{\text{LOCK DETECTED}}$ output goes high, and the VCO gating circuitry within the PULSE GATE is bypassed thus allowing PHASE and FREQUENCY comparisons to occur. The PLL then returns to the high tracking rate and the output signals return to their initial conditions.

If the chip is used as a data-synchronizer for MFM (on-chip data decoding not necessary) or other popular RLL codes, the SYNCHRONIZED DATA OUTPUT and the VCO CLOCK OUTPUT should be used. External decoding can be accomplished either in commercially available controller chips or via an encoder-decoder circuit, or by the customer's proprietary design.

PHASE ONLY VS. PHASE-FREQUENCY COMPARISON OPERATION

As mentioned above, the function of the PLL is to maintain phase and frequency lock between the reference signal (2F CLOCK or ENCODED DATA) and the feedback signal (VCO). A comparator that performs only phase comparison is mandatory during read-mode in order to handle the non-periodic nature of various coding schemes. With this type of detector, the phase-locked-loop functions as a feedback loop in which it responds only to the phase differences between the input and the feedback waveforms. As long as the reference and VCO signals have their edges aligned (are in phase lock) the PLL is insensitive to their frequency relationship.

During the nonread mode the PLL is required to lock onto the 2F CLOCK, a specific frequency reference that is close to the data rate. If a disturbance is somehow introduced in the system which results in cycle slipping or prolonged transient behavior of the reference clock, false lock may occur if a PHASE-ONLY comparator is being used. Under these circumstances PHASE comparison alone may be inadequate, since it discriminates only phase and not frequency information. A PHASE-FREQUENCY-COMPARATOR, therefore is employed within the DP8465 during this mode of operation. This comparator performs identically to the PHASE-COMPARATOR in the case when both inputs to the comparator have the same frequency; however, if the inputs exhibit the slightest frequency offset, the PHASE-FREQUENCY-COMPARATOR also provides a frequency-sensitive error correction signal to ensure frequency aquisition.

The PULSE GATE has two important functions. It ensures a continuous PLL lock in the presence of bit gaps encountered on the media and in the bit stream. It also provides a

precise time delay (independent of process and external component variations) necessary to align the incoming data with the center of the decoding window. The delay is exactly one half the period of the 2F CLOCK and the delay generator is referenced to the 2F CLOCK. This allows input bit jitter up to ±half the 2F CLOCK period.

The PULSE GATE incorporated in the DP8465 has two multiplexers which allow the circuit to switch from PHASE-FREQUENCY comparison to PHASE-ONLY comparison as the circuit switches from non-read mode to read mode. *Figure 1* is a block diagram of the PULSE GATE and details how this is accomplished. The delayed output of MUX-1 is shown to be compared with either the GATED VCO or the VCO DIVIDED BY TWO. The two VCO signals are multiplexed, with the INTERNAL READ GATE as the control signal, and the output is connected to the PHASE-FREQUENCY-COMPARATOR. When INTERNAL READ GATE is inactive (non-read mode) the 2F CLOCK DIVIDED BY TWO and the VCO DIVIDED BY TWO signals are selected by MULTIPLEXER-1 and MULTIPLEXER-2, respectively. In this configuration, phase and frequency comparisons are made between them and the possibility for a false lock occurence is eliminated. When the INTERNAL READ GATE is active (read mode), however, the ENCODED DATA and the GATED VCO signals are selected by the multiplexers. Through the circuit configured by the D-type flip-flops and the OR gate, the comparator effectively performs PHASE-ONLY comparisons (an INTERNAL VCO pulse is allowed to reach the input of MUX-2 only when an ENCODED DATA pulse is sensed). Thus, the DP8465 chip guarantees proper frequency lock of the VCO to the 2F REFERENCE CLOCK during the non-read mode, and it performs the necessary phase-only comparison during the read mode.

DATA SEPARATOR APPLICATION PROBLEMS

Following are some common application problems for many data separator circuit designs. The purpose of this application note is to identify these problems and to propose simple solutions. Thus, our DP8465 users will be able to avoid these potential application problems.

A) Loss of lock during read mode

In some systems the controller asserts the READ GATE randomly along a formatted track. If the READ GATE is asserted over a write splice, which usually contains unintelligible information, the PLL might false lock to some harmonic of the data, or it might be pushed to either extreme of its allowed frequency swing. Similarly, when the READ GATE is asserted over a data field, the PLL might lock to a harmonic of the data.

To recover from this problem a recovery routine must be implemented by the disk controller. This routine should toggle READ GATE so that the PLL can lock back to the 2F REFERENCE CLOCK and, after waiting a sufficient amount of time (to frequency lock to the crystal), activate READ GATE to retry the read operation.

A superior controller PLL algorithm only allows assertion of the READ GATE over a preamble or similar high frequency pattern. An example of such an algorithm is as follows:

1) Deassert READ GATE—allow a 4 byte time minimum for the PLL to lock to the 2F-REFERENCE CLOCK.
2) Wait for 2.5 bytes of valid preamble pattern.
3) Assert READ GATE
4) If valid preamble continues for 5 or more bytes then go to 5; otherwise go to 1.
5) "LOCK DETECTED" becomes active, AM search begins.
6) If AM is found, then continue the read routine; otherwise go to 1.

B) False lock in the non-read mode

The DP8465 **has been specifically designed to eliminate the possibility of false lock during the non-read mode.** This is accomplished by the use of a phase-frequency comparator in the non-read mode as was described in the PULSE GATE section.

False lock during the non-read mode can occur by two means in systems using phase only comparisons in the non read mode. When the power supply of the PLL circuit is switched on for the first time, the VCO ramps toward the reference frequency. The aquisition process may lock the VCO to some harmonic of the 2F REFERENCE CLOCK if the bandwidth (capture range) is not high enough. False lock can also occur in the non-read mode after an aborted read operation as described above. If the VCO has either lost lock or has been driven far from its center frequency while trying to read, then while relocking to the crystal, if the capture range is not wide enough, false lock might occur.

C) Quadrature Lock

Quadrature lock is a phenomenon which may occur when the periodic pulses in the PLL synchronization field become distorted such that they appear as periodic pulse-pairs as shown in *Figure 3*. This phenomenon is usually caused by the read channel electronics or recording components in the disk drive and may give rise to a false lock condition in the PLL known as quadrature lock.

Within the standard synchronization field which precedes the data field, bits are recorded at a constant frequency for a time sufficient to allow the PLL to acquire lock. With normal recording and read-circuit behavior, this synchronization information reaches the PLL as a continuous, periodic data stream. In some disk drives, if an offset has somehow been induced into the recorded information, or if a read-channel asymmetry exists within the drive electronics which skews the flux reversal zero-crossing point, the synchronization field waveform which reaches the PLL may appear in the form of periodic pulse-pairs. This condition only arises when a repetitive pattern is present, and gives rise to the occurance of quadrature lock. Note that quadrature lock is actually more prone to occur within systems where a low-noise design has minimized the randomizing effect which noise has on bit position.

Optional External Quadrature Lock Circuitry

To eliminate the possibility of a quadrature lock condition, a simple circuit (4 passive components) solution may be employed to prevent its occurrence. The circuit shown in *Figure 2* has the effect of forcing a misalignment of the data synchronization window with respect to the input pulse pattern should the quadrature condition occur. This circuit does not affect PLL operation once proper lock has occurred, and it is disabled once PLL LOCK has been detected by the DP8465. Although a recommended value is given for the resistor in the support circuit, some experimentation may be required in determining an optimum value for use within any particular system. *Figure 3* shows a diagrammatic representation of the quadrature lock waveforms.

D) VCO Jitter

The recommended starting value for the charge pump current setting resistor, R_{RATE}, was initially 1.5 kΩ. It has been found that maintaining a value of R_{RATE} at or below 820Ω has a stabilizing effect on the jitter performance of the VCO circuitry. Thus, we recommend that this 820Ω value be substituted for the originally recommended value of 1.5 kΩ.

As shown in the DP8465 data sheet, the minimum value of R_{RATE} is 400Ω. When choosing values for R_{RATE} and R_{BOOST}, the only requirement is that the total charge pump input current is less than or equal to 2 mA. This requirement can be met by adhering to the following requirement on the parallel combination of R_{RATE} and R_{BOOST}.

$$R_{RATE} \| R_{BOOST} \geq 350\Omega$$

(i.e., the parallel value of R_{RATE} and R_{BOOST} should not fall below 350Ω.)

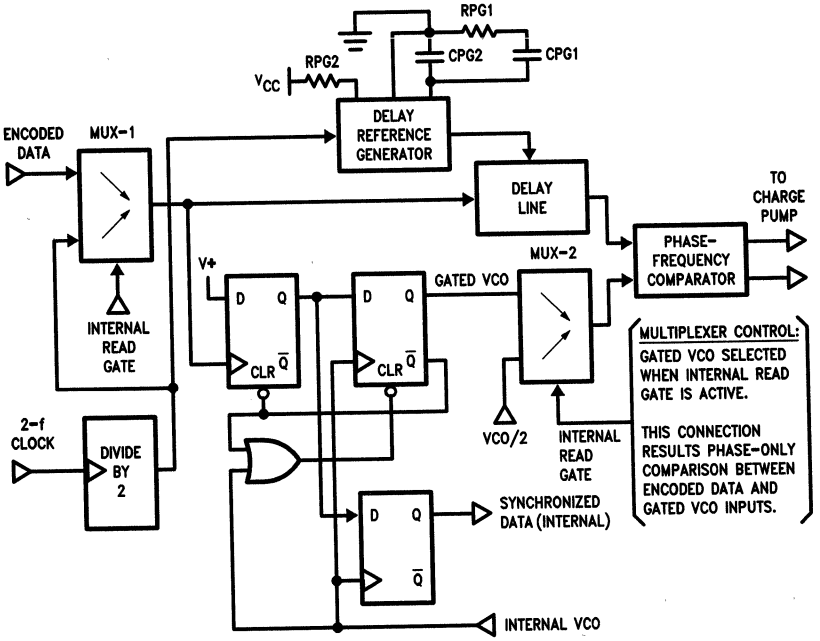
When the R_{RATE} value adjustment is implemented, all other component values associated with the loop filter must also be modified in order to maintain the original PLL response characteristics within the disk data field. The DP8465 Data Sheet shows a sample filter calculation and also several sets of loop filter component values for different values of R_{RATE}.

SUMMARY

The DP8465 is one of National's second generation single-chip high performance PLL circuits for application in disk memory systems. It features a comparator with both phase-frequency and phase-only comparison capabilities. The DP8465 offers significant savings of cost and time in production, test, and maintenance since only a few fixed passive components are required for operation. The need to trim any external components has been eliminated and since no external components determine window accuracy, the performance will not be sensitive to external variations. The chip requires a single +5V supply and it is housed in a narrow 24-pin dual-in line package (also available in 28-pin PCC package). The DP8465 is a direct replacement for the DP8460 and it may be used either as a data synchronizer for MFM or any of the existing Run-Length-Limited codes, or as a data separator for MFM.

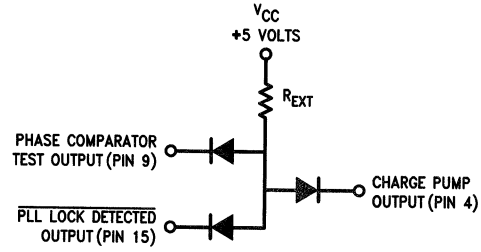
For further information, the reader should also refer to the National Semiconductor Application Note 414, Precautions for Disk Data Separator (PLL) Designs.

Pulse Gate Block Diagram



TL/F/8600–1

FIGURE 1.



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Recommended value for R_{EXT}: 10 $[R_{RATE} \| R_{BOOST}] \leq R_{EXT} \leq 20[R_{RATE} \| R_{BOOST}]$.

Diodes must be carefully chosen for minimal zero-bias capacitance and reverse leakage current (2 pF and 100 nA or better are recommended values, respectively).

Recommended diode types: 1N4448
1N4148
1N914

FIGURE 2. External Circuitry Used to Insure Correct PLL Lock to a Pulse-Paired Synchronization Field

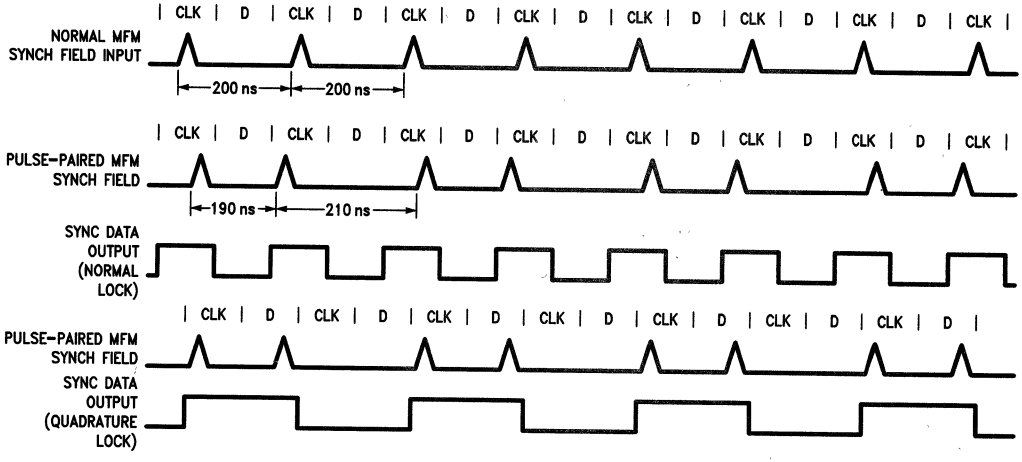

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FIGURE 3. Timing Diagram of PLL Quadrature Lock Within a Symmetrically Pulse-Paired Synch Field

Application Issues for the DP8465 Family of Data Synchronizers

National Semiconductor
Application Note 581
William Llewellyn

This application note covers National's first generation hard disk data synchronizers and separators, i.e., the DP8465, DP8462, DP8461, DP8455 and DP8451, citing some common PLL application concerns and describing some techniques to enhance performance.

FRACTIONAL HARMONIC LOCK

The frequency discrimination capacity of the digital phase detector within the data separator/synchronizer is suppressed whenever a pulse gate technique is employed. Although this pulse gating technique is a standard in disk drive applications and is necessary in order to allow the PLL to remain phase locked to randomly spaced disk data bits, it essentially causes the phase detector to behave as would an analog quadrature multiplier, i.e., the capture range of the loop takes on the finite value related to the loop bandwidth. Under ordinary circumstances, this is quite acceptable; however, it does permit the PLL to become susceptible to a form of quasi-stable false lock to fractional harmonics of the input frequency. (For example, a typical lock null for this phenomenon would be where the VCO stabilizes at 5/6 or 6/5 of its nominal frequency.) The conditions for occurrence of this are:

1) Pulse gate in use;
2) Periodic pattern is present (i.e., preamble);
3) Perturbation occurs either during or just prior to the periodic pattern, causing the VCO to swing outside of the dynamic capture range of the loop.

Since the capture range in a typical disk PLL configuration is on the order of ±2% of the data rate, it can be seen that harmonic lock could easily occur given an adequate perturbation of the loop. Typical causes of perturbations would be media defects and spurious noise pulses, among others, but the most commonly seen occurrence within soft-sectored systems is where an attempt is made to "read" through the write splice region on the disk (zone where the head write current is either switched on or off) during a sector search operation. Although recovery from harmonic lock will occur readily if the read operation is terminated (all National's currently released disk data synchronizers incorporate frequency discrimination when locking to the reference input), systems which exhibit fractional harmonic lock during a sector search may experience extended latency time as the search routine repeatedly tries to find the desired sector.

The soundest solution to harmonic data lock is the incorporation of a sector search routine which asserts Read Gate only within a preamble field, in conjunction with the use of a PLL which employs frequency acquisition during the lock sequence. National's DP8451 and DP8461 are designed for this type of application, employing frequency lock for the standard MFM preamble (2T, when T is equal to the VCO period). The DP8462 allows optional frequency lock for both 2, 7 preamble types (3T or 4T). National's most recent stand-alone data synchronizer, the DP8459, can accommodate frequency lock (also optional) with any standard preamble type (1T, 2T, 3T or 4T). The DP8459 also incorporates zero-phase start at the assertion of Read Gate, minimizing the phase disturbance at the beginning of a read operation.

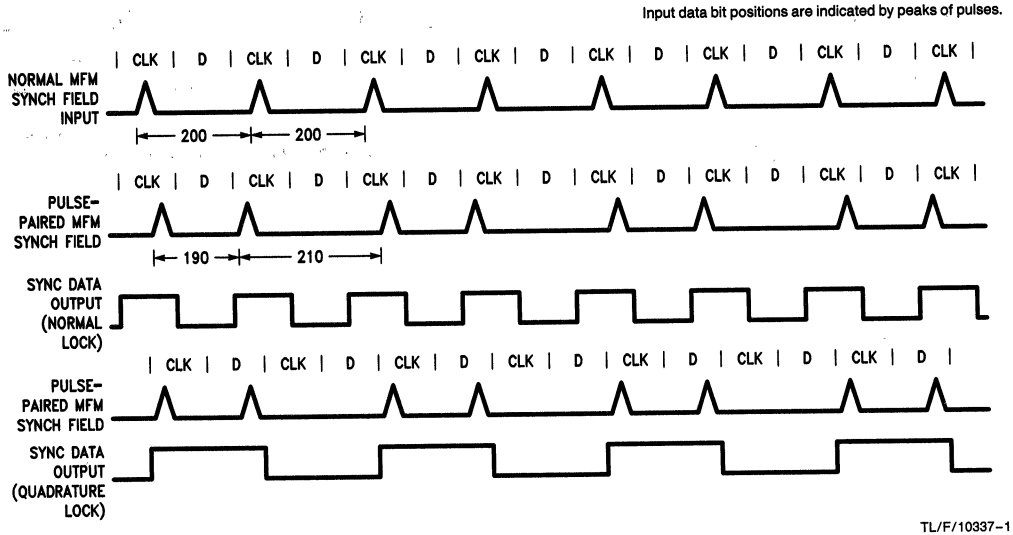

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FIGURE 1. Timing Diagram of PLL Quadrature Lock within a Symmetrically Pulse-Paired Synch Field

Within systems where it becomes evident that the reading of write splices is consistently producing sector-not-found errors, while at the same time it is not possible to either modify the sector search algorithm (in order to avoid the splices) or to make hardware modifications, the PLL can be made less sensitive to the write splice disturbance by the lowering of the loop bandwidth. This is recommended only as an interim solution until firmware or hardware accommodations can be made.

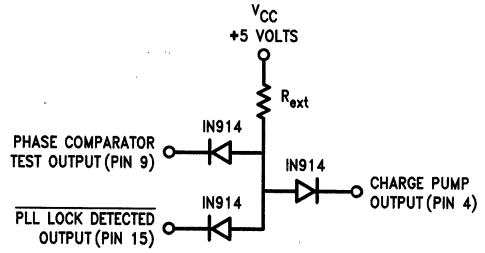
QUADRATURE LOCK

Another form of false lock may also occur (pulse gate in use) within a periodic disk pattern (preamble) given one additional condition; the periodic disk pattern being presented to the PLL exhibits a pulse-pairing phenomenon (typically introduced by the data channel electronics); see *Figure 1*. Within this particular pattern, PLL has the potential to lock to the correct frequency while remaining caught on a phase null 90 degrees from nominal. In this case, each pair of bits is interpreted by the PLL as residing in two directly adjacent windows (actually a violation of most recording codes) with the two subsequent windows empty. Although the bits appear to be greatly shifted within these windows, the phase corrections produced complement each other and average to a filtered DC value of zero. This repeating pattern is thus self-sustaining.

Quadrature lock is unique in that it is more likely to occur within a relatively well designed, noise-free system environment. The reason for this is that the randomizing effect noise ordinarily has on the data stream has been minimized, preserving the purity of the pulse paired pattern and thus increasing the probability of this form of lock. Again, this form of lock is generally only seen within the preamble, and may occur within either soft or hard sectored systems. Easily recognized waveform patterns seen at the separator/synchronizer outputs would be (1) the Synchronized Data Output exhibits a 110011001100 . . pattern instead of the standard 1010101010 . . . preamble pattern; (2) the Phase Comparator Test output pulse width consistently remains at approximately half of the VCO period (nominal width should be 7–12 nanoseconds); (3) -Lock Detected does not become active (low).

The most robust solution to this phenomenon (as in the section on harmonic false lock, above) is to incorporate a hard or pseudo hard-sectored search algorithm in conjunction with a data separator/synchronizer which employs frequency acquisition within the preamble as do the DP8451, DP8461, DP8462 and DP8459. The frequency acquisition mode allows no residual phase or frequency error within the PLL when locked, and thus the possibility of both quadrature and harmonic lock is eliminated.

A "bootstrap" hardware technique to avoid quadrature lock can be incorporated with the DP8465/55 devices, which do not incorporate preamble frequency lock internally (see *Figure 2*). This technique involves the inclusion of four passive elements external to the chip, which will deliberately force the window to shift away from the 90 degree phase null when (and only when) quadrature lock occurs. The passive network is automatically disabled once the PLL detects preamble lock. Although a recommended value is given for the resistor in this support circuit, some experimenting may be required in determining an optimum value for use within any particular system.



Recommended value for R_{ext}:
$10[R_{rate} \| R_{boost}] \leq R_X \leq 20\ [R_{rate} \| R_{boost}]$

FIGURE 2. External Circuitry Used to Insure Correct PLL Lock to a Pulse-Paired Synchronization Field

VCO JITTER

The inherent purity of the VCO's operating frequency is a key element in the accuracy of the data separator/synchronizer window generation. Any "jitter" present in the VCO frequency (any modulation of the period of the waveform by noise or any other source) will degrade the performance of the PLL. Within National's initially released DP8451/55/61/62/65 data separators-synchronizers, it has been found that maintaining a value of R_{rate} at or below 820Ω has a stabilizing effect on the jitter performance of the VCO circuitry. We recommend the following guidelines be followed in the selecting of charge pump resistors and loop filter components for these circuits (see Table I):

1) An 820Ω value resistor should be substituted for the originally recommended value of 1.5 kΩ.
2) Although this new R_{rate} value is below the original DP8451/55/61/62/65 specification limit, a substitute requirement has been placed on both R_{rate} and R_{boost} to maintain proper circuit operation:

$$R_{rate} \parallel R_{boost} \geq 350\Omega$$

(i.e., the parallel value of R_{rate} and R_{boost} should not fall below 350Ω.)

3) If the inclusion of an 820Ω value for R_{rate} means a component change within an existing system (i.e., the user had been employing some higher value), all other component values associated with the loop filter must also be modified in order to maintain the original PLL response characteristics within the disk data field:

Define: $M = R_{rate}(old)/820$ [eg., (1500/820)]. Then,

$$CLF1' = CLF1 * M$$
$$CLF2' = CLF2 * M$$
$$RLF1' = RLF1 / M$$

4) Additionally, in the cases where the Quadrature lock circuitry are in use:

$$R_{ext}' = R_{ext} / M$$

TABLE I. Data Separator/Synchronizer Reference List

Device	Synchronized Codes	Separated Codes	Frequency Lock	Window Centering Trim
DP8461	MFM; 1, N	MFM	Reference & 2T (MFM)	None
DP8462	2, 7 MFM;1, N	None	Reference; 2, 7 (3T or 4T, Optional)	Optional
DP8465	2,7 MFM; 1, N	MFM	Reference	None
DP8451	MFM; 1, N	None	Reference, 2T (MFM)	None
DP8455	2, 7 MFM; 1, N	None	Reference	None
DP8459	1, N; 2, 7; MFM; GCR	None	All (1T–4T, Optional)	5-Bit Digital Strobe

Note 1: DP8461 and DP8451 pinouts match the DP8465 and DP8455, respectively; for use with hard and psuedo-hard sectoring only.

Note 2: DP8462 incorporates optional frequency acquisition for 2, 7 synchronization fields, but may be used as a data synchronizer for any disk code.

Note 3: DP8451 and DP8455 also available in PCC package (20 pin).

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

As with any high-frequency analog circuitry, care should be taken in PC board layout when using the DP8465 family of data synchronizers. The following is a list of practical guidelines intended to help insure sound, trouble-free operation with these devices.

1) Establish a local V_{CC} island or net, separate from the main V_{CC} plane, to which the device and its associated passive components can be connected. V_{CC} supply filtering should be liberal and in very close proximity to the chip. The electrical lead length of the filter capacitance between the V_{CC} and ground pins themselves should be as short as possible (minimizing lead inductance). Inclusion of a quality high-frequency capacitor, such as a 1000 pF silver-mica capacitor, in parallel with a ceramic 0.1 μF capacitor, is recommended. (Note: the chip is particularly sensitive to inadequately filtered switching supply noise.)
2) Effective capacitive bypassing of the R_{boost} and R_{rate} pins directly to the V_{CC} pin is very important. Again, use quality, high-frequency capacitors and maintain the shortest possible electrical lead length.
3) Use the main digital ground plane for all grounding associated with the device. The ground pin and the PG1 pin should tie directly to this plane.
4) Do not locate the chip in a region of the PC board where large ground plane currents are expected.
5) Locate all passive components associated with the chip as close to their respective device pins as possible.
6) Orient the chip's external passive components so as to minimize the length of the ground-return path between each component's ground plane tie point and the chip's ground pin. (Ground noise at the loop filter components, RLF1, CLF1 and CLF2, which is not identically present at the ground pin (common mode), is coupled through the filter components into the VCO control voltage pin.)
7) Include no planing whatsoever (V_{CC} or ground) directly between adjacent pins. This will minimize parasitic capacitance at each pin. Planing between the two pin rows, however, is recommended (directly beneath the package).
8) Avoid running signal traces between pins.
9) Run no digital signal lines between or adjacent to the analog pins or signal traces (pins 1 through 7 and PG3) in order to avoid capacitive coupling of digital transients.
10) Minimize the total lead length of the C_{VCO} capacitor. Inductance in this path degrades VCO performance, as does parasitic pin capacitance.
11) Do not place any bypass filtering at the R_{VCO} pin (minor coupling of the VCO waveform into this pin is normal and acceptable).
12) Eliminate negative-going voltage transients (undershoot) at the digital input pins (pre-termination of driving lines may be necessary) to avoid drawing transient input-clamp-diode current from the device pins.
13) Minimize digital output loading; i.e., if outputs must drive large loads or long lines, employ buffers.
14) Allow unused digital output pins to float, unconnected to any net.
15) Avoid locating the chip within strong electromagnetic fields. If possible, choose the "quietest" region of the board.
16) If chip socketing is desired, use a low-profile, low mutual capacitance, low resistance, forced-insertion type (socket-strips are recommended). Avoid the use of "ZIP-DIP's".
17) Do not use wire-wrap interconnect, even in an evaluation set-up.
18) Make allowance for pin-to-pin capacitance when determining C_{VCO} (Typically 4–5 pF) from data sheet formula.

DP8459 Window Strobe Function

National Semiconductor
Application Note 578
Kern Wong

INTRODUCTION

This note explains in detail the Strobe Function incorporated on the DP8459 ALL-Code Data Synchronizer. It is recommended that the reader reviews the data sheet prior to reading this note. The Strobe Function within the DP8459 chip is considerably more intricate and versatile than any existing Strobe Function on commercially available data synchronizers, thus, this application note is intended to point out the significance of this device feature and to convey important information on the proper use of it. It is also the intent of this writing to offer an explanation on the concept of Strobing and associated terminology for customers who may not be familiar with the subject. Further, the ease with which the Strobe Function can be employed to optimize system performance and to realize cost effective manufacturing of products is discussed.

DESCRIPTION

The Strobe Function implemented in the DP8459 chip provides a powerful and convenient means for the synchronization window to be shifted either Early or Late with respect to its nominal position. By definition the Strobe step, t_S is the digitally programmable time displacement of the (DP8459) synchronization window from its nominal position and is expressed as:

$$t_S = M \times (1.8\% \times t_{VCO})$$

where "M" is the value of the Strobe control word, having a range from −15 to +15. The fine resolution of the individual strobe step (LSB) in conjunction with the thirty-one steps of movement provided by the DP8459 is unprecedented among commercially available devices, which have at most a few fixed strobe positions if any at all. The strobe control word, "M", is set by five of the six binary bits within the Control Register as shown in *Figure 1*. Bit #4 is the sign bit which determines Early or Late strobe movement. The last bit (#5) in the control word is the test bit, which when set to high is used for factory testing. This bit is always the first bit serially loaded into the shift register. The following truth table (refers to Table I) maps "t_S" to the corresponding Strobe word representations.

TABLE I. Window Strobe Truth Table

Strobe Bit					Strobe	Window Strobe
4	3	2	1	0	Word M	t_S (Typical)
0	1	1	1	1	−15	$-0.270 \times \tau_{VCO}$
0	1	1	1	0	−14	$-0.252 \times \tau_{VCO}$
0	1	1	0	1	−13	$-0.234 \times \tau_{VCO}$
0	1	1	0	0	−12	$-0.216 \times \tau_{VCO}$
0	1	0	1	1	−11	$-0.198 \times \tau_{VCO}$
0	1	0	1	0	−10	$-0.180 \times \tau_{VCO}$
0	1	0	0	1	−9	$-0.162 \times \tau_{VCO}$
0	1	0	0	0	−8	$-0.144 \times \tau_{VCO}$
0	0	1	1	1	−7	$-0.126 \times \tau_{VCO}$
0	0	1	1	0	−6	$-0.108 \times \tau_{VCO}$
0	0	1	0	1	−5	$-0.090 \times \tau_{VCO}$
0	0	1	0	0	−4	$-0.072 \times \tau_{VCO}$
0	0	0	1	1	−3	$-0.054 \times \tau_{VCO}$
0	0	0	1	0	−2	$-0.036 \times \tau_{VCO}$
0	0	0	0	1	−1	$-0.018 \times \tau_{VCO}$
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	1	1	$0.018 \times \tau_{VCO}$
1	0	0	1	0	2	$0.036 \times \tau_{VCO}$
1	0	0	1	1	3	$0.054 \times \tau_{VCO}$
1	0	1	0	0	4	$0.072 \times \tau_{VCO}$
1	0	1	0	1	5	$0.090 \times \tau_{VCO}$
1	0	1	1	0	6	$0.108 \times \tau_{VCO}$
1	0	1	1	1	7	$0.126 \times \tau_{VCO}$
1	1	0	0	0	8	$0.144 \times \tau_{VCO}$
1	1	0	0	1	9	$0.162 \times \tau_{VCO}$
1	1	0	1	0	10	$0.180 \times \tau_{VCO}$
1	1	0	1	1	11	$0.198 \times \tau_{VCO}$
1	1	1	0	0	12	$0.216 \times \tau_{VCO}$
1	1	1	0	1	13	$0.234 \times \tau_{VCO}$
1	1	1	1	0	14	$0.252 \times \tau_{VCO}$
1	1	1	1	1	15	$0.270 \times \tau_{VCO}$

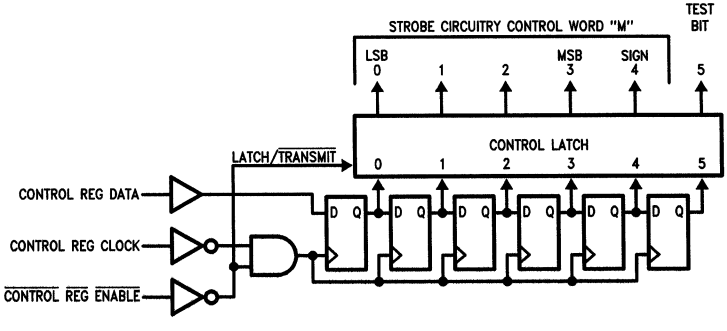


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FIGURE 1. Strobe Control Register Diagram

The Strobe Function is also referred to as Window Strobe, because strobing is used to adjust the relative position of the synchronization window. To better illustrate the relationship of strobe to the synchronization window, please refer to *Figure 2a*. This diagram depicts the concept of synchronization window. The synchronization window is defined as a continuously repeating time cell, which has a nominal time span equal to the period of the VCO. Ideally, an Encoded Read Data pulse will be captured and correctly interpreted regardless of its position within the window boundaries. However, the ideal window width cannot be realized in practice, due to noise and device non-idealities such as VCO jitter. Thus, a small fraction of the usuable window is truncated, leaving a correspondingly narrower available window width. If device mismatch and other asymmetric phenomena are also present, another window eroding phenomenon called window shift results. This phenomenon causes the average data window center to shift with respect to the expected mean bit position. Referring to *Figure 2b*, note that the static window width in this case appears congruent to that in *Figure 2a*. However, early shifted data bits in *Figure 2b* actually have a greater probability of falling outside the window since it is shifted late. The Strobe function is a simple to use, yet powerful feature which, as will be explained later, allows the user to offset, within ½ LSB, the undesirable window shift and improve system performance.

Synchronization Window Diagram

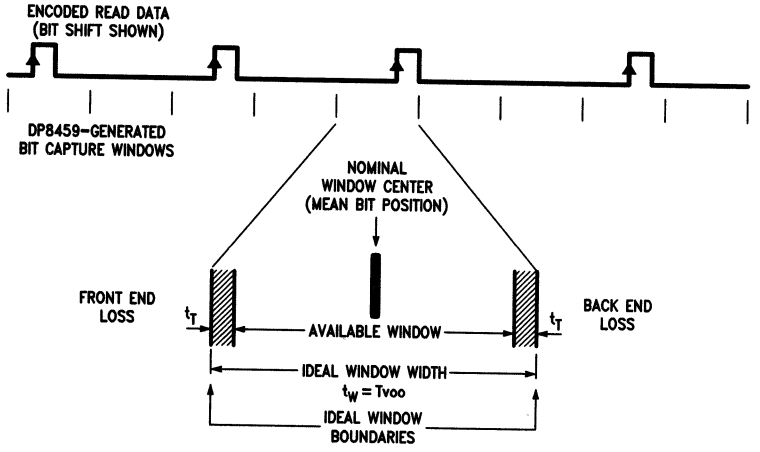

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FIGURE 2a. Synchronization Window

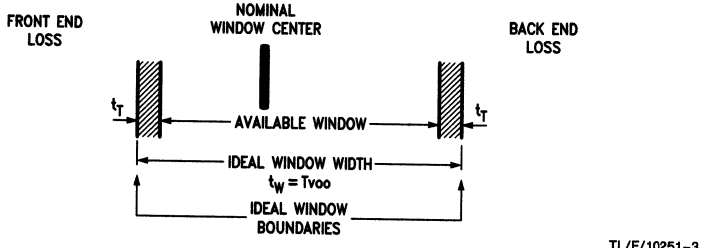

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FIGURE 2b. Window Shifted Late

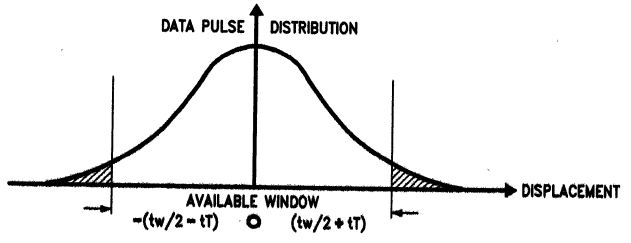

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FIGURE 2c. Bitshirt vs Probability of Its Occurrence

BYPASSING STROBE FEATURE

To fully harness the Strobe feature as in an intelligent interface environment, the MICROWIRE™ bus may be interfaced to a processor or controller function to program the internal control register during initialization or between read operations. The information stored in the control register, bits #0 through #4, defines the amount and sense of window displacement. (Important, bit #5 must be set to "0" for normal operation, since a "1" at this location will place the chip into a test mode used during production testing.) A typical system diagram with the MICROWIRE bus is shown in *Figure 3*.

If the customer does not wish to use the Strobe feature (strobe word may be fixed at the nominal setting of all bits equal to 0), the MICROWIRE bus can be bypassed. By appropriate hardwiring of the control register inputs, as depicted in *Figure 4*, the control register content is always set to the nominal strobe upon Read Gate assertion. Please note that the window truncation is not specified at the "Nominal" Strobe setting. Therefore, optimum window performance may not be realized at this setting. This and similar device configurations are usually employed when the prime interest is to construct a simple setup for general device evaluation purposes. Of course it can also be used in lower data rate systems and, particularly, in tape and floppy drives where the window margin requirement is generally less stringent.

Although the technique just described can serve as a convenient means to set the control register content, it is very important to note that it requires the user to correctly sequence the Read Gate. For example the chip must be powered up in the non-read mode, this is with Read Gate low. Since Read Gate is tied to the "CRE" pin, a logic low enables the shift register portion of the control register to serially enter data while the control latch is held in its previous state. Concurrently, the E.R.D. pulses must be present which serve as clock pulses to shift the all "zeroes" data. Finally, the Read Gate must then be switched to the high state, thus inhibiting data entry into the shift register and allowing the new data just entered into the shift register to be transferred to the latch. Whether loading the control registers with the method as shown in *Figure 4* (this diagram represents a typical system setup where the RG also controls the HDG and CRE pins) or employing the same scheme via external circuitry, if the Read Gate is tied to CRE, the synchronizer chip must be powered up with Read Gate low. After the control data has been loaded, Read Gate must be set high. (The need to pulse the Read Gate was not mentioned in the March 1988 datasheet).

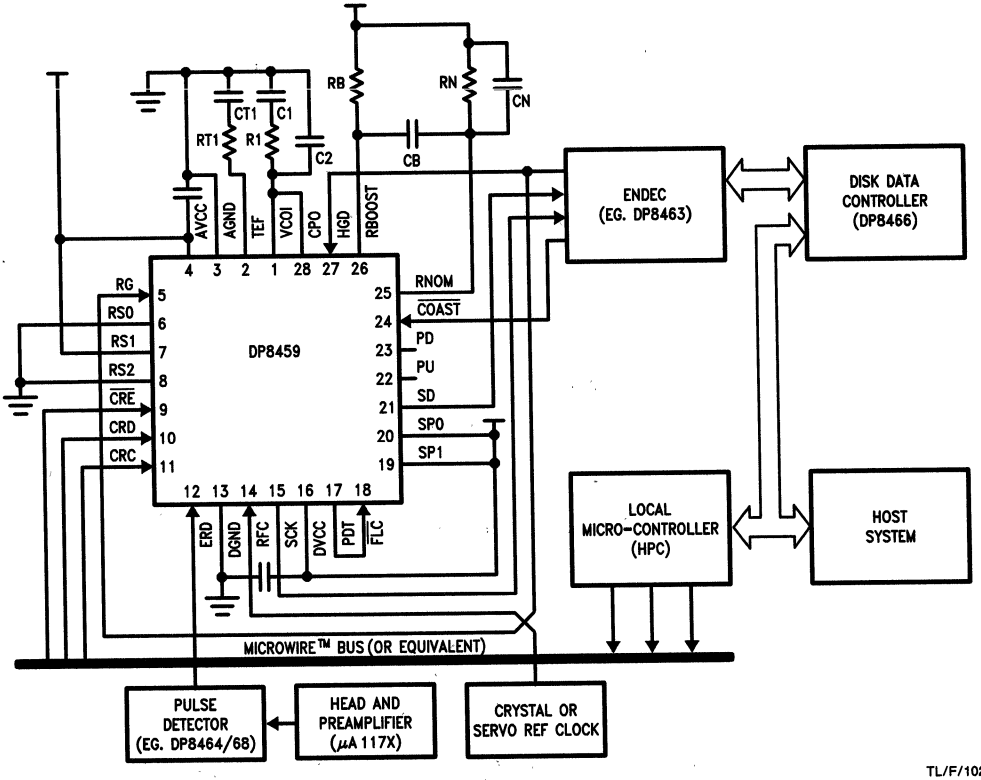

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FIGURE 3. Typical System with the MICROWIRE Bus

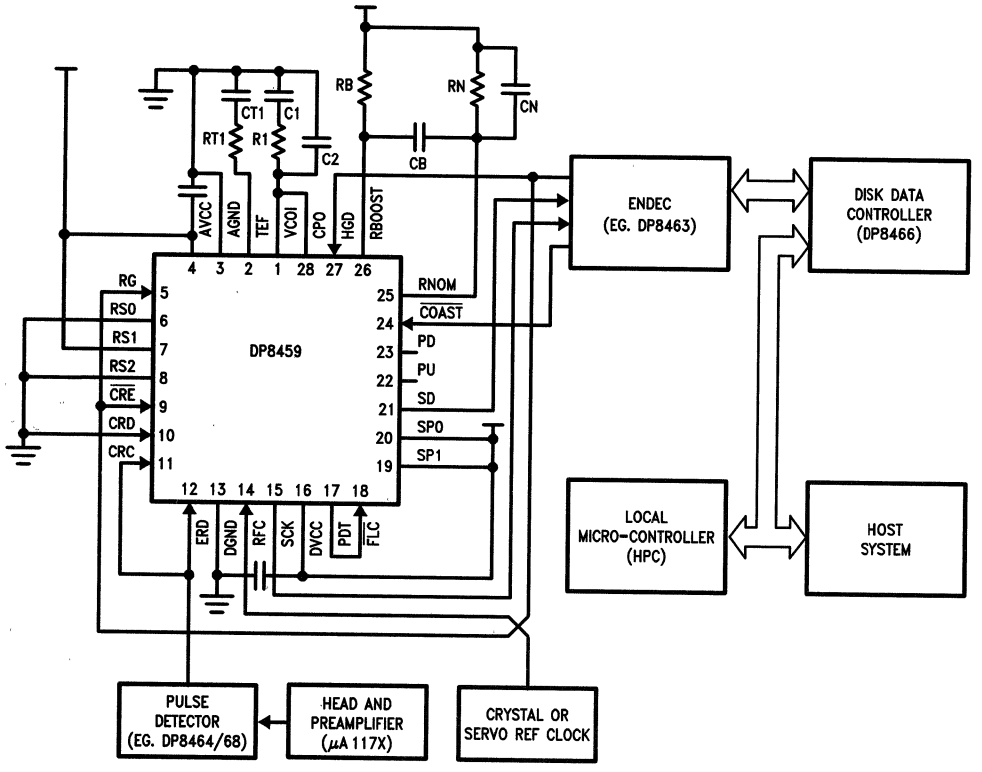

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FIGURE 4. Typical System without the MICROWIRE Bus

WINDOW TRUNCATION SPECIFICATION

The Strobe function is also used to qualify the window truncation specification. For example, the DP8459 half-window loss, "t_T", represents the sum of static window truncations from all relevant circuits and mechanisms in the data synchronizer, e.g. window shift, VCO jitter, etc. At 10 Mb/s, "t_T" is specified as 3.0 ns (6% of VCO period) maximum with M = −2. If the strobe is not used, i.e. M = 0, then "t_T" maximum would typically be 4.8 ns. This, however, is not tested and therefore not guaranteed.

The static window truncation consists of two separate major contributors to window loss, namely "T_S" (which is due to window shift) and "T_N" (which is truncation due to noise and other relevant mechanisms). The window strobe feature can be used to minimize "T_S" to ½ LSB of the strobe step. At 10 Mb/s "T_S" can be minimized to typically 0.45 ns. The remaining loss is due to "T_N".

The DP8459 window specifications are valid over the entire operating temperature and power supply ranges per datasheet. Thus the window specification "T_T" is actually comprised of "T_N", "T_S", temperature guardbanding, and measurement system guardbanding. The "t_T" parameter is tested at 4.75V V_{CC} and 5.25V V_{CC}. The device is checked at 10 Mb/s and 20 Mb/s data rates for window specification compliance as part of the final test in manufacturing. It should be noted that the data sheet recommended strobe position settings are determined by statistical averaging of many units during device characterization. In high performance drive system applications, users can take advantage of this Strobe feature to individually "tune" the synchronizer for optimal detection window symmetry.

STROBE FUNCTION

There are several reasons why one wishes to alter the inherent average window position generated by the phase-locked oscillator within the synchronizer. First, the average data window position may not be perfectly centered about the expected mean data bit position. Second, deliberately skewing the window position can serve to recover malshifted data bits. Third, shifting the window can introduce excessive error rate for testing and calibration purposes.

There could be a substantial amount of random displacement (jitter) of individual bits dependent on the design of the read/write head, media, signal processing electronics, and the result of bit interaction. This is exemplified in *Figure 2c*, which shows that the data bit displacement (also known as bitshift) versus its probability of occurrence is a Gaussian distribution. In bitshift theory, total bitshift refers to the movement of the magnetic transitions with respect to the position where they are recorded. There are three dominant factors which contribute to the loss of window margin, i.e. the difference between the farthest shifted bit and the actual window boundary. The intersymbol interference, which is a function of recording components and code used, the pulse detector imperfection, which is primarily caused by

equalization and differentiation errors, and the phase locked loop accuracy, which involves its inherent window skew and jitter. The first two contribute to bitshift while the last one reduces the effective window width. Fortunately, the fraction of window loss due to the PLL window skew can be substantially nullified, and excessive bitshifts may be compensated during read mode via the strobe function in high performance data synchronizers such as the DP8459.

The first three LSBs of the Strobe Control Word produce strobe steps that have shown to track quite well with respect to the predicted values. For example, at 10 Mb/s data rate, typical characterization data indicates less than one nanosecond deviation between the measured strobe readings and the corresponding calculated strobe values. The data is taken with the Strobe Control Word range from M = 0 to M = ±6 and with the chip operating at 4.75V V_{CC} and 5.25V V_{CC}. It is recommended that this strobe range (M = 0 to M = ±6) be used for applications requiring relatively accurate strobe step control, such as for window alignment, data recovery, and window margin test. The higher strobe ranges are not as accurate due to the cumulative error when more bits of the control word are turned on. Thus for $|M| \geq 7$, this range is perhaps more suitable for inducing excessive soft errors in system analysis and experimentation purposes. System designers can thus perform real time system optimization studies to identify and to correct anomalies within the read channel chain. For example, after creating a significant amount of soft errors, any component within the read channel may be changed or modified to determine if error reduction can be achieved.

DESIGN CONSIDERATIONS

It is important to note that changing the strobe setting requires a finite response time of the control circuitry. In addition to the time required to load the 5-bit Strobe Control Word to the internal register the user must account for the settling time associated with any change of the strobe. This is a function of the Timing Extractor Filter (TEF) components and the data rate at which the data synchronizer is being operated. It is highly recommended that any change to the strobe setting be done with the Read Gate deasserted and with sufficient time allowed for settling prior to the initiation of another read sequence.

The Time Extractor Filter is used in a second PLL, the reference phase-locked loop, within the chip. This loop stably locks to a crystal reference oscillator (or a servo derived) frequency reference and it is responsible for producing a delay time of exactly one-half of the VCO period. Via this delay, the synchronizer data window is accurately centered about the mean bit position such that optimal capturing of the data becomes possible in the presence of jittery data pulses. Furthermore, strobing, which modifies the one-half VCO period delay, is achieved by programming a small amount of change in current (sourcing or sinking) to the current controlled oscillator of the reference phase-locked loop.

The VCO circuit of the reference PLL is constructed identical to that of the primary PLL. To prevent VCO frequency-control-voltage runaway in the primary loop, a comparator circuit is connected between the two loops to sense when the primary oscillator current crosses thresholds, which are placed 50% above and below the reference current. (Please refer to the simplified block diagram in *Figure 5.*) If

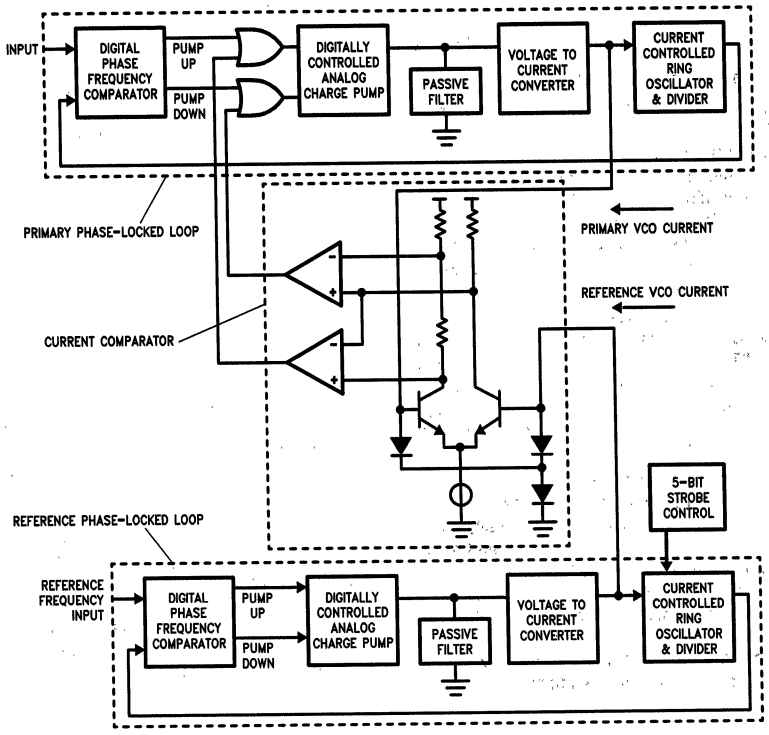

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FIGURE 5. Reference and Primary PLLs within the DP8459

either one of the preset threshold is crossed, the comparator directs a correction signal to the primary PLL and limits further excursion of its VCO control voltage.

Since the reference PLL is part of the feedback loop that regulates the primary PLL, the Time Extractor Filter components also affect the synchronizer performance, but not the strobe step amount. In the (March 1988) DP8459 datasheet, *Figure 10*, presents a table of the estimated settling times due to a phase step for different (TEF) loop component values operating at various data rates. The calculated numbers in that table reflect the idealized settling time of the reference PLL block only. Assumptions made in the calculation, as empirical data was not available at the time of the publication, were no initial frequency offset, the values of the loop gain and the loop's natural frequency were approximately equal, and the effect of any parasitic conditions were neglected. Current lab data shows the TEF settling time from a maximum strobe movement (a step from M = −15 to M = +15) is nearly 15 times longer than the figures projected in the datasheet. [i.e. at RFC = 10 MHz, $T_{SETTLE} \cong 290\ \mu s$ (measured) instead of 19.6 μs as predicted; and at RFC = 20 MHz, T_{SETTLE} measured is approximately 140 μs versus 9.6 μs as calculated.] In practice it is expected that customers would normally use the strobe range of $|M| \leq 6$ for reasons as mentioned in the previous section. Typical lab data for a strobe movement from M = −6 to M = +6 are also included here for reference: with RFC = 10 MHz, $T_{SETTLE} \cong 130\ \mu s$ and at RFC = 20 MHz, $T_{SETTLE} \cong 54\ \mu s$.

Complete settling of the synchronized outputs at the primary loop may require slightly longer time. Although this settling time can be substantially reduced by either raising the bandwidth of the TEF or increasing the damping of the filter via RT1, this usually degrades the static window margin (by up to a few percent of the ideal window width). Since the window margin is an important parameter, it should not be compromised with the settling time. In a multi-data rate system it is recommended to employ the TEF components associated with the lowest data rate. In general the TEF settling time is not a critical parameter except perhaps for test time considerations when multiple strobing is involved (i.e. in margin testing in the production line). Other than the highest performance and the fastest systems, the latency time due to such system factors as soft-sectoring, command instruction delays, error correction/retrys, etc. in typical hard disk storage drives may be much longer than the TEF settling time. Therefore changing strobe settings from sector to sector is not practical in many hard disk environments. It is advisable that even for systems that are not limited by their latency time between read executions to allow a minimum of one revolution time (16.7 ms) between strobing. It should be mentioned also that the customer who wants to change the TEF settling time must observe stability criteria as in any PLL system.

APPLICATIONS

Individual "Trimming" of the PLL

For mass storage systems operating at low data rates (e.g. 5 Mb/s or less), two or three nanoseconds of window loss due to skew may be an acceptable specification. But, at higher data rates, storage systems can not tolerate such figures. As mentioned in the previous section, a portion of the window loss is ascribed to window skew. Although most of this loss may be recovered, undertaking the trimming of the synchronizer block is often an unpleasant manufacturing issue; presently this involves a technician in the assembly line adjusting a potentiometer while monitoring an oscilloscope. In high performance drives it is always desirable to regain as much margin as practical in production. The ability to perform in-system window deskewing is an extremely attractive attribute because it can attain the potential window margin available by optimizing each drive individually. It should be noted that this is superior to having the PLL chip statically adjusted prior to system integration. Of course such an in-system trimming procedure usually tags on a relatively high premium, such as added cost of time, labor, and material. Other than discrete designs, monolithic PLL devices generally afford limited or no adjustment to nullify window skew. The DP8459 synchronizer's Strobe feature presents a viable solution to perform window adjustment easily and inexpensively. The digitally controlled strobing within the chip allows "trimming" of the detection window without the need to "tweak" any external components. As mentioned, its 5-bit resolution strobe function makes it possible to deskew the inherent window offset with subnanosecond precision at 10 Mb/s and higher data rates.

Window Centering Algorithm

Truncation due to inherent window shift can be mostly nullified via the window strobing technique. Hence, an intelligent drive system can greatly benefit from the DP8459 Strobe feature because a window centering algorithm can be installed with no extra hardware or adjustment required. Moreover, the task of window deskewing can be readily automated with the DP8459 via the MICROWIRE bus. For example, some of the industrial interface standards such as the Rev-2 "ESDI" interface standard already supports a 4-step Early/Late strobe option in the command level, independent of the strobe step size to be implemented. The following describes a strobing alogorithm that can be employed for window centering.

A typical window centering routine should establish some higher than nominal error rate thresholds by strobing the data window in the early direction, then repeating the same process in the late direction. The early and late strobe settings which yield the equivalent error distribution are then stored. From the strobe excursion information, the window center skew can thus be determined and the appropriate strobe word is set to correct the window skew. To implement an effective routine one should employ a periodic test pattern such that the average decode window is made more stable. The system error rate can be deliberately made more responsive if some constant (time independent) source of window degradation functions such as maximum bit crowding or reduced signal to noise ratio is introduced during testing, i.e. performing the test at the inner recording cylinders of the Winchester type disk drive. Such a routine could execute during system power-up and produce optimal centering of the window. The system would function like having a built-in tester to perform window auto-calibration at power up or at any scheduled maintenance interval.

Data Recovery

Another valuable application of the DP8459 Strobe function is to service error-bound data recovery. Infrequently, the need arises to rescue vital, but marginally recorded, data

information from a removable data cartridge, and in particular from a (magnetically) damaged or defective storage module. Usually, such an operation requires repetitively reading through one block of data at a time and exhaustively shifting through some range of window strobe steps in an attempt to correctly retrieve the data of interest. However, employing the DP8459 in conjunction with a suitable data retrieval algorithm, could offer any mass storage system a powerful tool for speedy recovery of error-bound data. The DP8459 device is capable of delivering typically a 1.8% window shift resolution, furthermore, its thirty-one steps of strobe setting is programmable via the MICROWIRE bus. Such features make it possible to incorporate sophisticated utility programs such as one for data recovery.

Window Margin Test

The technique of Strobing employed in window margin testing is not a new practice. Shifting the detection window is one of two acceptable means to "marginalize" the window (modify the VCO generated data window) for checking the merit of the read channel. Although it has been gaining popularity in the test equipment sector, the theory behind it may be unfamiliar to some drive users and manufacturers alike. Window margin testing is an extension of the window centering process as discussed above. Please refer to Appendix A for a discussion of window shifting and window narrowing techniques in error-rate analysis.

Window strobing can be a very time-saving method to analyze the drive system's error rate characteristics. Unlike conventional testing, it does not consume hours to transfer data and to perform data integrity comparison. Hence, the DP8459 Strobe Function is very convenient for this purpose. For example, in a manufacturing environment, a new data storage drive system will be thoroughly characterized for its error rate profile with independent test techniques. Then it will be followed by a series of window shift induced error rate tests. The accelerated error rate profile thus generated is next compared to those produced from other test methods. Error distribution, statistical correlation, and acceptable thresholds are thus established. In production then, the correlated error rate figures and their corresponding Strobe settings are stored permanently in the memory of the drive/system during final checkout. These statistics are subsequently utilized as criteria for performance acceptance or rejection such as in QA and incoming inspections. Furthermore, systems in the field can be routinely interrogated for their current window margin status.. This, for example, can take the form of an embedded system maintenance routine to reduce the potential hazard of an unexpected system crash predicament. An effective window margin diagnostic test routine should employ the most bitshift sensitive test pattern and operate at the maximum bit crowding region of the media.

SUMMARY

The Window Strobe feature of National's latest PLL data synchronizer chip, the DP8459, has been presented along with the background information necessary for its utilization. The versatility and power embedded in this digitally controlled Strobe function is unparalleled. Although the prime intent of strobing is to deskew the inherent window asymmetry thus improving the device window margin, it also lends itself to a host of important system applications. They include in-system calibration of window centering which also allows adjustment of the individual drives to maximize their performance margin; system window margin analysis in design optimization and system maintenance; and data recovery on damaged media without the need of dedicated test equipment. The DP8459 strobe feature provides an economic and reliable solution to enhance the value and performance of disk drive designs, at the same time making the products more cost effective to manufacture.

Acknowledgement

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Appendix A

The purpose of this appendix is to present some basic information on a few commonly used tools and methodologies in window margin analysis. It will derive a mathematical expression describing the relationship between window shifting versus error rate probability. It will be shown that this expression is equivalent to that which relates to the window narrowing method, which is a well publicized technique to analyze the detection window margin.

There are two prevalent methods in the industry to qualify the window margin of disk drives, the margin that remains when the worst case jitter on the Encoded Read Data bits is subtracted from the non-ideal window (shifted and/or truncated). One method is to ascertain the average pulse distribution from the encoded data stream output. It usually involves a precision time-interval acquisition apparatus which measures the average pulse separation read from a particular track that has been preconditioned with a worst case data pattern. Another method is to measure the accelerated soft error rate induced by modifying the data window derived from an accurate (discrete designed) PLL circuit. Most disk drive testers employ either one of these methods for window margin test. It should be pointed out that testers used in research and development are usually built with the variable window width design, because they lend more sophisticated testing and render additional useful information such as system signal to noise ratio, media defects, and resolution of the head/disk components. It is also interesting to note that because an external PLL system is required, such a tester is generally not capable of checking the data synchronizer block in a disk data storage system.

Since a PLL system with programmable detection window width is expensive and difficult to build, nearly all commercial disk drive testers for manufacturing and end user applications do not employ such technique. Instead, they employ other methods such as measuring the average pulse distribution or the average synchronization window width. Although strobing is also incorporated in some drive testers, they contain but only a few strobe steps. Therefore, in window margin analysis their result can not be compared to the more extensive data gathered from the variable window width method. This trend, however, is changing as engineers are turning to more sophisticated strobing in both disk drive and drive tester designs. If a window shifting technique can mimic window narrowing in error rate response, it can be applied to window margin analysis also. The following discussion presents an accepted model used in the industry to describe error rate probability versus window width and shows that an equivalent expression also holds for the case of a shifted window.

As mentioned in the Strobe Function section, a Gaussian distribution describes error rates due to bit shift. Two such distributions are needed to define the error probability. One distribution is associated with the positive bitshifts and one is associated with negative bitshifts. This is due to the fact that for adjacent bits, one bit is pushed in the Early direction and one is pushed in the Late direction. The residual bitshift is denoted as offset or "To". The width of each of the distributions is defined as "Tne" which describes the broadening of the distributions due to the random noise of the environment (please refer to *Figure 6*). Hence, the appropriate Gaussian function, defined as N, for the two distributions can be written as:

$$N = \frac{No(K)}{2}\left[\exp\left(-\frac{(t-To^2}{2\,(Tne)^2}\right) + \exp\left(-\frac{(t+To)^2}{2(Tne)^2}\right)\right] \quad (1)$$

where "No" is the number of bits read in a revolution of the disc, "K" is the normalizing constant to normalize each of the resulting error constants to unity when the distributions are integrated, and "t" is the time associated with the bitshift distribution. The equation for the error rate, which is simply the area of the tails of the bitshift distribution beyond the available window width, can be written as:

$$\text{Error Rate (Window-Narrowed)} = \frac{K(No)}{2}\left\{\left[\int_t^{\infty} \exp\left(-\frac{(t-To)^2}{2(Tne)^2}\right)\right] dt \quad (2)$$

$$+ \left[\int_{-\infty}^{t} \exp\left(-\frac{(t+To)^2}{2(Tne)^2}\right)\right] dt\right\}$$

$$= No/2\left\{\text{erfc}\left[\frac{t-To}{Tne}\right] + \text{erfc}\left[\frac{t+To}{Tne}\right]\right\} \quad (3)$$

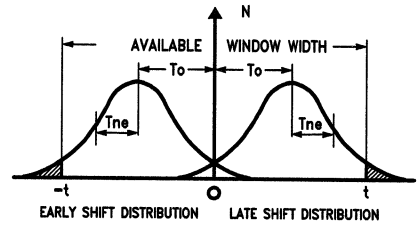

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FIGURE 6. Error Probability from Early/Late Shift Distributions

where "erfc" is the complementary error function and "t" is the half-window width at which the error rate is observed. An error rate versus window width curve takes the form represented in *Figure 7*. This is obtainable for the case where the data window is modified by narrowing the window while keeping it centered about the phase-locked oscillator expected window. This technique is typical of engineering drive testers employing an external PLL system for window margin analysis.

Consider if the window is shifted, instead of being narrowed, the limits on the second integration of equation (2) are changed and the corresponding "erfc" term becomes:

Error Rate
(Shifted Window)

$$= \frac{K(No)}{2}\left\{\int_{t}^{\infty}\left[\exp\left(-\frac{(t'-To)^2}{2(Tne)^2}\right)dt'\right]\right. \quad (4)$$

$$\left.+\int_{-\infty}^{t-T_\omega}\left[\exp\left(-\frac{(t'+To)^2}{2(Tne)^2}\right)dt'\right]\right\}$$

$$= No/2\left\{\text{efrc}\left[\frac{t-To}{Tne}\right]+\text{erfc}\left[\frac{Tw-t+To}{Tne}\right]\right\} \quad (5)$$

This corresponds to the bit error distribution evaluated with the average window having nominal width of "Tw", and "t" being the time position of the window's right-side boundary. In theory, the techniques with window narrowing and that of window shifting are equivalent. Empirical results from these two approaches should correlate if the incremental change in window displacement or window size employed is the same in both cases. Typical error rate versus the amount of shifted window with respect to the mean bit distribution should be similar to the profile depicted in *Figure 7*. A means to implement the shifted window scheme via the DP8459 Strobe function for margin testing is discussed in the text. Unlike the variable PLL-window technique, this method presents a bootstrap test methodology wherein the PLL synchronizer in the system is included in the window margin test.

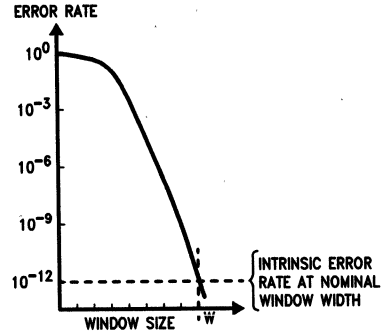

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FIGURE 7. Error Rate Distribution vs Window Width

DP8459 Zoned Bit Recording

National Semiconductor
Application Note 599
Kern Wong

Driven by current progress in micro-processors, small information processing machines with mainframe-like power are rapidly moving toward storage intensive areas such as sophisticated file servers, photorealistic graphics systems, and engineering work stations. Disk drive makers are constantly trying to keep up with the increasing demand for higher capacity modules. The quest to store more and more data within the same hard disk assembly form factor has reached a point where advances in head and disk technology alone are not adequate to raise the areal density as quickly and economically as the industry wants.

Most of the high performance 5¼ in. Winchester drives today employ up to 15 Mb/s data transfer rates (RLL codes) and some even use ultra high resolution head/media in order to achieve a 700+ Mbytes capacity. Nevertheless, disk drive makers continue to seek out new ways and viable techniques to reach even higher capacity storage modules. While new methods of recording and higher performance recording components are being researched, other means of improvement using current disk technology are being investigated. One of these schemes is zoned-bit recording (ZBR) which is showing very respectible results. This method allows for packing more data on a disk surface using conventional head/disk components. The following discussion reviews the basis of ZBR and presents a design application using the DP8459 data synchronizer to simplify ZBR implementation.

ZBR BOOSTS DENSITY BY RECAPTURING VAST DISK AREA INEFFICIENTLY UTILIZED

ZBR came from an earlier idea called constant (linear) density recording, or (CDR) which pioneers of the disk community had toyed with nearly two decades ago. Conventional 5½ in. Winchesters usually employ a single data transfer rate such as 5 Mb/s, 10 Mb/s, 15 Mb/s, etc. The linear density of a given design is dictated by the maximum number of flux transitions that can be placed end-to-end on the inner-most data track of the disk surface. Since the circumferencial length of any track is proportional to its radius, the outer tracks become increasingly more loosely packed with data bits. As a result, a large portion (over 90%) of the disk surface in typical drives is not effectively utilized; i.e., valuable areal density is wasted.

The goal of CDR was to write the same linear bit density (constant flux change per unit length) to every track on the disk data surface. The reading and writing of data occur at frequencies which increase as a function of the diameter of the disk. This requires that multiple data rates be used, with each track operating at a different transfer rate, the outer tracks employing higher data rates than the inner ones. True CDR implementation can bear a substantial design/manufacturing overhead, e.g., sophisticated sector management is required since the number of sectors are different in each track, also non-conventional servo data is needed to accommodate the different data rate used for each track. Such a system demands additional firmware and software design. And because there are as many data rates used as the number of tracks employed in the disk drive, more elaborate tests are involved during manufacturing. Furthermore, the minute gain in recording capacity for using slightly different data rates in adjacent tracks might not be practical from a system's point of view. System overhead for a CDR drive thus might not be cost effective for current disk drive systems.

Zoned Bit Recording, on the other hand, is an engineering compromise to CDR. By adopting a more conservative approach, the ZBR method divides the disk data surface into a number of concentric bands called zones, with each one consisting of several tens to hundreds of tracks. The drive thus writes more data in zones on the outer edge of the disk (employing higher data rates) than in zones toward the spindle center. This is a design compromise where a substantial gain in areal density can be achieved with a much lower design and manufacturing overhead. Please refer to *Figure 1a* and *1b* which depict the bit distribution from a pre-recorded periodic pattern over different tracks.

The reemergence of CDR or ZBR was facilitated by current advances in the LSI read channel electronics. In particular, the monolithic data synchronizer/data separator integrated circuits have been a significant driving factor. About five years ago such a function (for 5 Mb/s data rate only) would have typically occupied a good portion of the electronic card cage in a drive system. Today many chip design houses can produce the core of the data synchronizer function in a single chip. However, few commercially available devices could meet the needs for high performance CDR and ZBR implementations. The DP8459 data synchronizer stands out with unique features specially designed to address this application.

DP8459 INCORPORATES FEATURES FOR ZBR

The key features of the DP8459 which make it ideal for multiple data rate operation reside in the Timing Extractor and VCO sections of the chip. They enable a broad range of data rate operation, plus the external support components require minimal programming. (Please refer to *Figure 2.*)

Conventional synchronizer chips may require a passive delay line to perform the task of window alignment. For ZBR designs that means many delay modules are needed to be multiplexed for operation requiring different data rates. Furthermore, they may have to be custom made to obtain those precise and non-standard delay values. For higher performance data synchronizer circuits and particularly for applications involving higher data rates, some PLL chipmakers use external resistors to control duty cycle of the VCO waveform. This approach utilizes the opposite (rising and falling) edges of the VCO output as a delay line. But, such chips may still require the trimming of an external resistor to attain optimum duty cycle symmetry for the desired delay time. Moreover, they would invariably require the switching of an external bank of precision resistors in ZBR.

The timing extractor block of the DP8459 represents a second PLL operating in tandem with the main PLL of the device. It is an accurate variable active delay line whose function is to establish synchronization window alignment so that the expected data bit is optimally centered about its decode window. The resultant delay is nominally equivalent to one half of the period of the reference clock.

The DP8459's built-in tracking silicon delay line completely obviates the need to switch external components. It takes

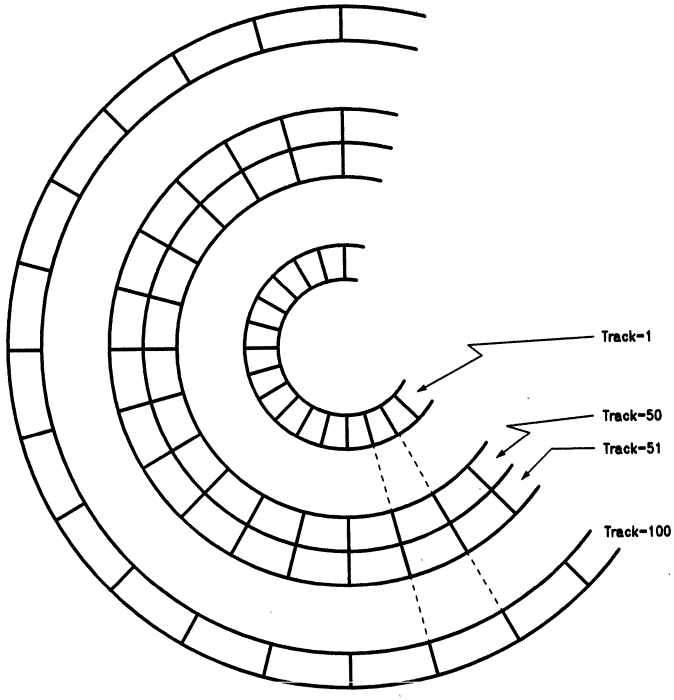

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FIGURE 1a. Single Data Rate

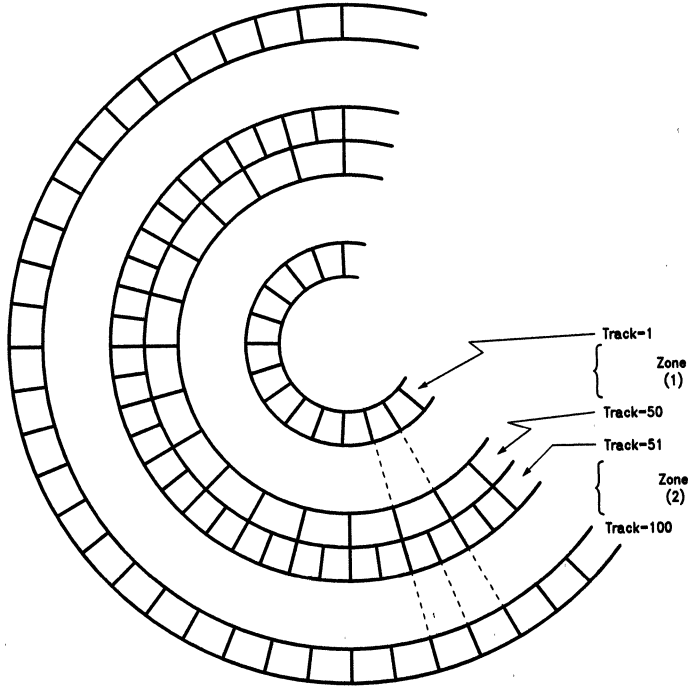

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FIGURE 1b. Multiple Data Rates

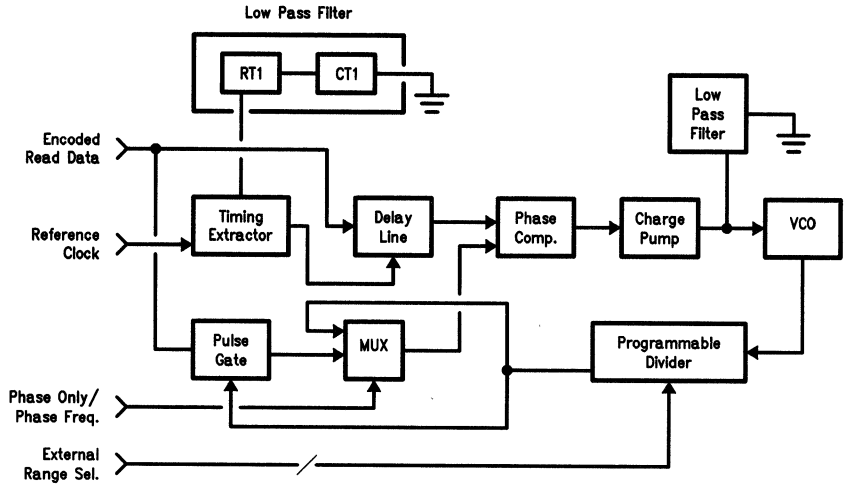

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FIGURE 2. Simplified Block Diagram of the DP8459 PLL

full advantage of the stable timing relationship from the reference clock input. The reference clock can be a crystal oscillator, a closed loop servo clock, or a programmable clock generator chip such as National Semiconductor's DP8531. The resistor-capacitor (Timing Extractor Filter) shown in *Figure 2* is employed for stabilizing the secondary PLL. The delay line performance is strictly a function of the reference clock accuracy, and is insensitive to the external components associated with the extractor as well as to supply voltage, temperature and IC process variations. Furthermore, the Time Extractor Filter (RT1 and CT1) components need not be changed for different data rates in ZBR. Simply choose the manufacturer's suggested values associated with the lowest data rate employed.

The DP8459's unique "auto ranging VCO" design provides another important advantage for ZBR. The reference clock frequency also sets the "center frequency" of the VCO automatically for the selected data rate, thus, no external components are needed for the VCO. The VCO section of the synchronizer consists of a high frequency oscillator and a programmable modulus divider. This arrangement provides a continuous range of VCO operating frequencies from 500 kHz to 50 MHz (range selection is via a 3-bit word input). The data rate range extends from 250 Kb/s to 25 Mb/s with MFM, [2, 7], and [1, 7] codes and from 250 Kb/s to 10 Mb/s for GCR codes. The DP8459 again simplifies multiple data rate applications as it requires no adjustment of any external VCO resistor/capacitor, LRC tank, or separate VCO circuitry. This not only facilitates design and testing of products, it also reduces unwanted noise from coupling to sensitive nodes. In addition, with ZBR designs operating over a 2:1 VCO frequency range, users may not need to change the range select control word, which further simplifies the design.

ZBR DESIGN CONSIDERATIONS

Unlike the controller section of a ZBR design, whose firmware and software can become more complex in order to handle a different system of sectoring, the DP8459 PLL bears practically no additional overhead. Whether one wishes to produce a system with 8 zones or 64 zones, it is important to recognize that the DP8459 synchronizer eases drive system designs by reducing the number of external components required and eliminating the need for trimming and switching critical components. ZBR implementation is simple with the DP8459, as is shown by the system block diagram in *Figure 3*. For ZBR operation, the Reference Clock input frequency must be changed whenever a different data rate (zone) is used. This can be accomplished with a crystal based programmable clock chip, such as National's DP8531. If the input is derived from a PLO (closed loop servo clock) the Reference Clock frequency would automatically update to the proper frequency as the servo head positions to a different zone.

In general it is not necessary to employ different loop filter components for every zone, especially if the adjacent zones are designed to operate over a small range of data rates. A single (compromised) 2nd order low pass loop filter should deliver acceptable performance margins, even when operating with a 2:1 ratio of data rates, for most of the drive designs. Of course there might be some designers who prefer to use more exotic filter configurations and/or to switch several loop filters to optimize system performance. If one requires switching filters, the following discussion is presented for consideration.

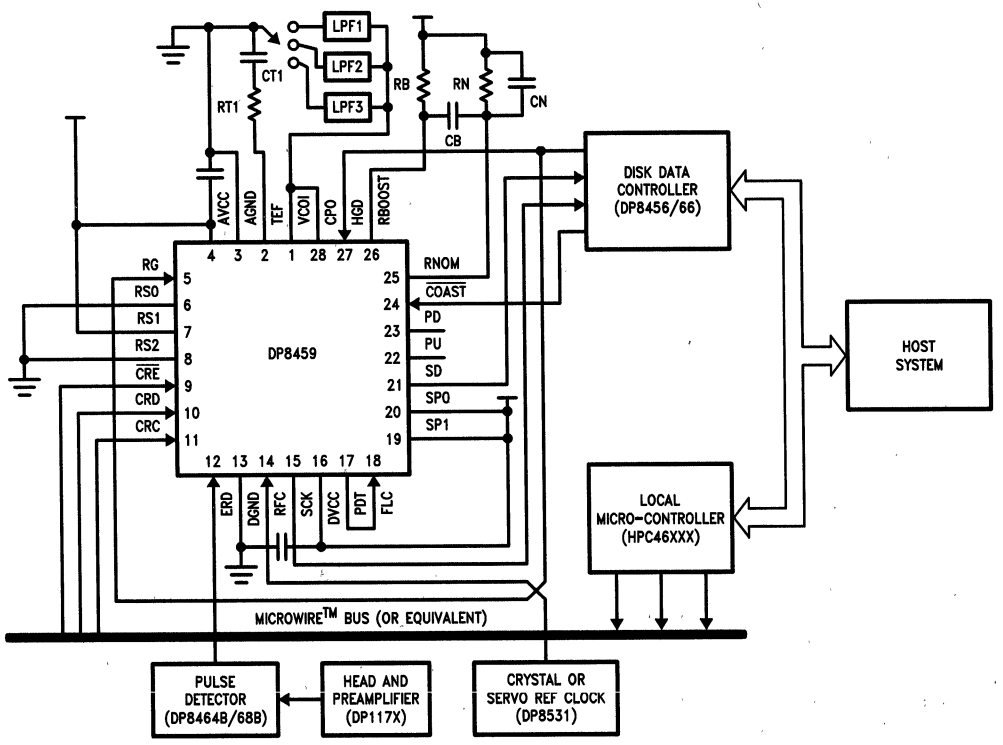

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FIGURE 3. Sample ZBR Drive System Employing the DP8459

Figure 4a shows multiplexing 3 complete sets of simple loop filter components via a switch. Alternatively one can modify the loop filter's characteristic BW or damping by changing only one of its resistor or capacitor values (see *Figure 4b*). Such a configuration can also produce an effective compromised loop filter which can handle a large number of data rates. (This scheme can help trim cost and minimize circuit board real estate.)

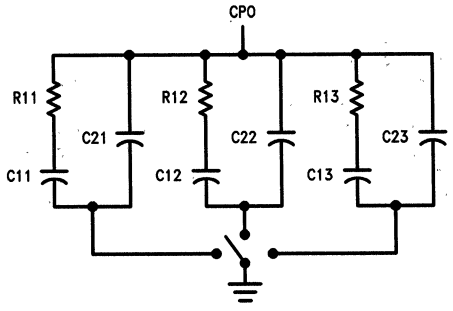

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FIGURE 4a. Switching of 3 Complete Lead-Lag Loop Filters

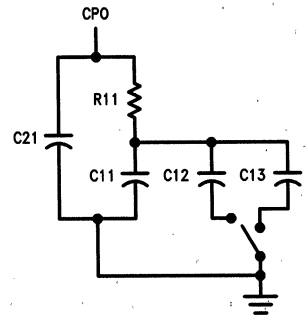

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FIGURE 4b. Modifying a Simple Filter with a Capacitor

Multiplexing several loop filters may be accomplished to advantage with micro-miniature mechanical relays. This is due to their superior isolation, lower leakage, and lower contact resistance compared to electronic switches. However, these advantages must be weighed against their slower response time and the need to suppress the relay coil's back EMF. Although "wet" contact relays are speedier and provide debouncing action, they can cost up to 10 times over conventional types. Analog (FET) switches have certain merits that make them suitable for switching of loop filters; these include long term reliability, fast response time, and high contact density per device. Furthermore, they lack the

back EMF hazards and do not consume much power to maintain closed "contacts". These features make them good candidates for multiplexing a large number of filter networks as in a ZBR application. However, some important device specifications must be examined before making a device selection. Commercial grade analog switches have a typical on-resistance of less than 40Ω, a terminal parasitic capacitance of 20 pF or less, and a leakage current of less than one nano-amp (but this spec can increase up to 50 times at high temperatures!). Nevertheless, they may offer acceptable performance as signal switches. The important issue is to determine the switch's performance under actual drive operating conditions and that typical loop filter characteristics can be maintained in the presence of parasitic elements. Another point to be aware of is that analog switches generally require bipolar power supplies, which may be unavailable in most drive systems. There are some instrumentation solid state relays which offer superior specs with attributes resembling those of mechanical relays, but their cost and contact density per device may not be cost effective for most present drive designs.

Since the DP8459 has provisions for a dual-port PLL filter network, higher order filters and active filter designs may also be used. This provides a third means to alter the loop filter characteristics conveniently via active filter implementation.

ZBR AND SINGLE DATA RATE DESIGN COMPARISON

Presently, high performance 5¼ in. Winchester companies are actively trying, with advanced head/media, to push recording densities to over 30k bit/in., track densities to over 1600 tracks/in., and are employing higher data transfer rates from 20 Mb/s to 24 Mb/s to achieve a Giga-byte capacity drive. It can be shown that without resorting to radically different technology and future generation recording components, this goal can be met by using ZBR techniques with conventional head/media.

The following design example compares a ZBR drive system and one using a single data rate; both assume moderate design parameters that are within current-generation disk technology:

The data rates and number of tracks used in each of the 9 zones for the ZBR design example above is listed below:

Zone	Tracks	Data Rate	Loop Filters
1	71	15.000 Mb/s	LPF1
2	71	15.600 Mb/s	LPF1
3	77	16.224 Mb/s	LPF1
4	80	16.873 Mb/s	LPF2
5	84	17.547 Mb/s	LPF2
6	87	18.249 Mb/s	LPF2
7	91	18.779 Mb/s	LPF3
8	94	19.738 Mb/s	LPF3
9	869	20.528 Mb/s	LPF3

Compared to the 15 Mb/s single data rate design, the ZBR design operating between 15 Mb/s and 20 Mb/s offers approximately a 30% increase in capacity. Operating the same system at a uniform data rate of 20 Mb/s is not feasible because the selected head/media characteristics (resolution limitations) would not have yielded acceptable performance over 40% of the inner tracks. At this increased data rate, higher grade head/media must be used to raise the drive's storage capacity. Although this ZBR design example needs to use higher data rates, the required read channel electronics to handle it are available and bear a lower system overhead compared to choosing the higher cost, grade, and less available (high bit density) media and (higher resolution and lower flying height) recording heads of today to support greater than 15 Mb/s single data rate Winchester disk drives.

Zoned-Bit Recording	RLL Codes	Single Data Rate Design (RLL)
Linear Density	20,404 Bits/In.	20,404 Bits/In. (Max)
Track Density	1,400 Tracks/In.	1,400 Tracks/In.
Data Surfaces	15	15
Data Rates	15 Mb/s to 20 Mb/s	15 Mb/s
Data Rate Spread	4% on Adjacent Zones	Not Applicable
No. of Zones	9 Zones	1 Zone
Loop Filters	3 Sets	1
Unformatted Capacity	1,016.3 Mbytes	721.5 Mbytes

CONCLUSION

The Zone-bit Recording concept is rapidly gaining popularity for the next generation of high capacity disk drive designs. The DP8459 high performance data synchronizer chip is truly designed to address the special needs of ZBR applications. It eases ZBR designs by eliminating cumbersome adjustment and switching of critical resistor/capacitor components for the VCO and delay line sections of the data synchronizer circuit. The combination of using the DP8459 device and ZBR techniques provides an economic and reliable solution to enhance the value and performance of disk drives, making them more cost effective to manufacture. This design methodology can achieve a significant increase in storage capacity while using existing disk technology. The DP8459 can be used in the manufacture of high performance, high capacity, multiple data rate flexible disk, optical disk, and giga-byte capacity 5¼ in. Winchester drives.

DP8459 Evaluation Board

National Semiconductor
Application Note 502
Kern Wong and Michelle Wong

I. INTRODUCTION

This literature describes the hardware and function of a printed circuit board for the evaluation of National Semiconductor's DP8459—All Code PLL Data Synchronizer. The purpose of the board is to assist the user of the chip in becoming familiar with the device features and in understanding its operation. The board is configured (socketed) for the 28-pin PLCC package (DP8459V) device. It contains the necessary connections and circuitry which greatly simplify the set-up of a test apparatus and facilitates the task of device evaluation.

II. CIRCUIT BOARD DESCRIPTION

Please refer to the schematic and layout captions in *Figures 1* to *4*. The circuit board layout follows the general recommendations discussed in Section 5 of the DP8459 data sheet. The entire circuit on the board can be described by the four subsections in the following text.

1. RESET FUNCTION: D1, Q1, Q2, and ½ of U1 (2-input NAND gates) form a single-shot circuit which generates a reset pulse during power-on. This signal clears the shift register, counters, and D-type flip-flops on board. Subsequently, it allows the selected STROBE circuitry control word (bits #0 to #4) and the test bit #5 to be loaded into the PLL's internal control register. The board also provides a manual reset function, which consists of switch SW-1 (SPDT momentary or toggle switch) and the remaining half of U1. It provides a reset signal while the chip is powered on.

2. LOAD AND SHIFT FUNCTION: U2 (2-input NAND gates), U3 (D-type flip-flops connected in toggle mode), U4 (8-bit parallel-in serial-out Shift Register), and U5 (divide-by-6 counter) constitute a 6-bit word programmable data generator. It issues a set of MICROWIRE™ equivalent outputs to program the control register in the PLL. U5 pin #8 is the Control Register Enable (CRE) signal. A logic LOW level allows data to be strobed into the registers. A logic HIGH level latches the register data and issues the information to the appropriate circuitry in the chip. U4 pin #9 to the Control Register Data (CRD) input shifts out a selectable 6-bit word. U3 pin #8 is input to the Control Register Clock (CRC) whose negative edge clocks the CRD pattern into the register.

3. REFERENCE FREQUENCY CLOCK: U6 (CMOS Inverter HC04) and a crystal form a stable reference oscillator which is required by the PLL for proper operation. This signal is applied to the RFC input of the DUT.

4. DIP SWITCHES: Three sets of toggle DIP switches are used to manually program the PLL input pins for the different modes of operation and for the various ranges of data rates and window strobe features.

(i) SW2—Switches #1 to #6 select the 32 combinations or steps of Early/Late window strobe position which is useful for the purpose of window skew compensation or recovery routines of marginally readable data. For normal device operation (non-test mode), the test bit (switch #6) must be set logic LOW.

The control register bit and toggle switch correspondence is shown below. Whenever the reset function is activated, the current SW2 setting is loaded into the control register. For detailed window step vs. strobe bit, refer to *Figure 4* in the data sheet.

SW2: Switches	#1	#2	#3	#4	#5	#6
Control Register Bit:	0	1	2	3	4	Test

(ii) SW3—The top three switches are used to select the VCO frequency range via the Range Select pins RS0, RS1, and RS2. The fourth switch is not used. The relative VCO frequency versus the 3 bit code is tabulated below:

Switch			VCO Range
#3 RS2	#2 RS1	#1 RSO	
1	1	X	0.50 MHz–1.25 MHz
1	0	1	1.25 MHz–2.5 MHz
1	0	0	2.5 MHz–5.0 MHz
0	1	1	5.0 MHz–10.0 MHz
0	1	0	10.0 MHz–20.0 MHz
0	0	X	20.0 MHz–48.0 MHz

Important—If the desired VCO frequency is located at the boundary of 2 ranges (overlapping), select the range which places that frequency at the higher end of the spectrum, (e.g. Fvco = 20.0 MHz, choose RS code = 010). This will optimize the performance of the chip.

(iii) SW4—The functions of the 8 switches are detailed as follows:

Switches #1 to #3 control the Frequency Lock Control (FLC). At most one and only one of the 3 switches should be engaged or closed.

Switch #1 closed—FLC connects to PDT

Switch #2 closed—FLC connects to RG

Switch #3 closed—FLC connects to GND

Switches #4 and #5 program the Sync Pattern Select Pins SP0, SP1 for the internal divider modulus to detect either the 1T, 2T, 3T, or 4T preamble pattern. (T = VC0 period; e.g. 3T = 100100...preamble).

Switch		Sync Matching Divider Modulus M
#5 SP1	#4 SP0	
0	0	1
0	1	2
1	0	3
1	1	4

Switches #6 to #8 control the High Gain Disable (HGD) pin. Again, only one of these 3 switches should be closed at any time.

Switch #6 closed—HGD connects to GND

Switch #7 closed—HGD connects to RG

Switch #8 closed—HGD connects to PDT

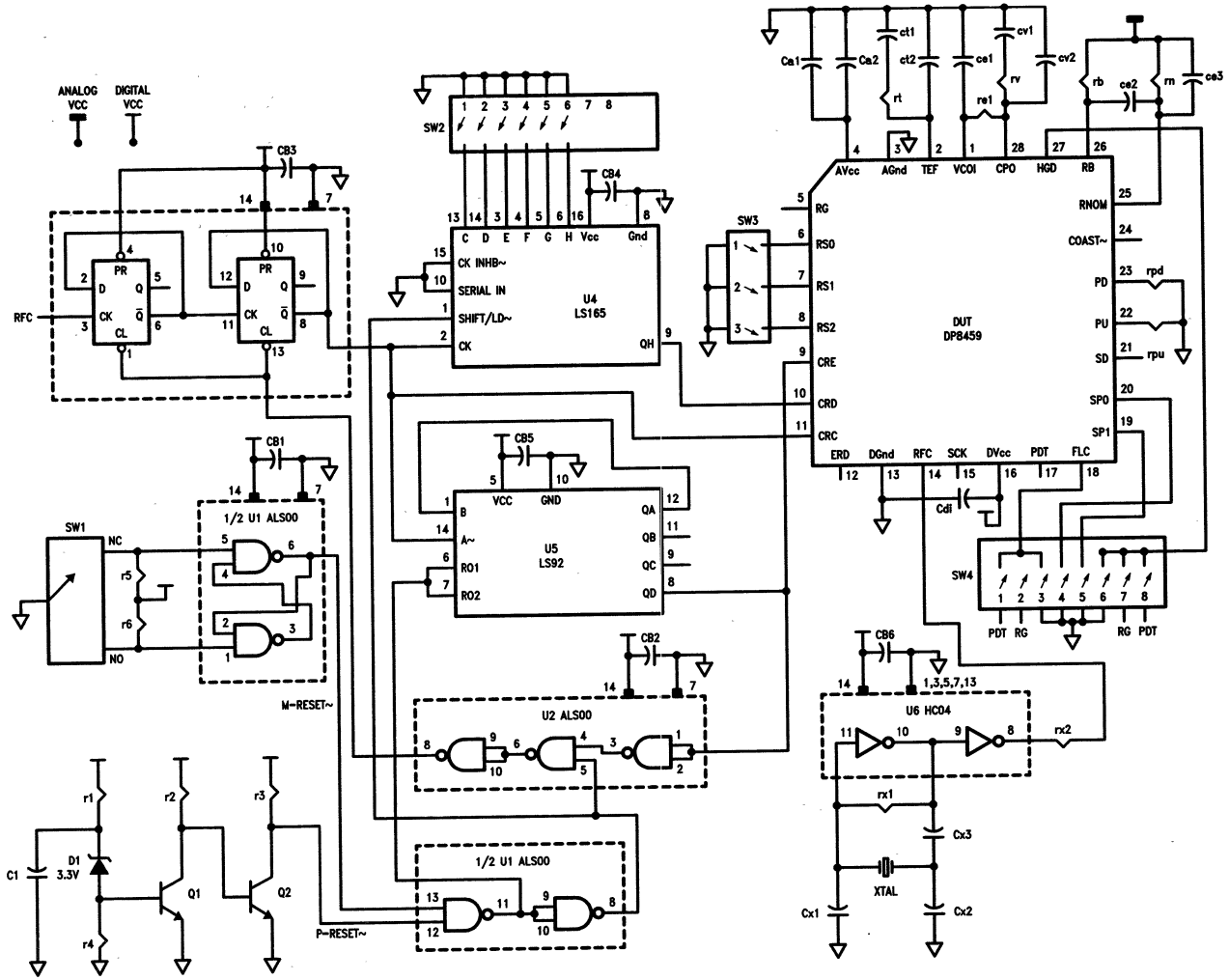

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FIGURE 1

III. TEST HARDWARE

1. EXTERNAL COMPONENTS: All integrated circuits are socket mounted to make it easy for the purpose of interchange or replacement. Passive components for the loop filters, charge pump resistors, and the crystal oscillator sections are also provided with sockets to facilitate alteration of components for different data rates.

2. POWER SUPPLY: Three separate supply terminals are provided on board. One ties to the Analog V_{CC} and a second ties to the Digital V_{CC} of the PLL chip. A third post makes connection to the rest of the digital support circuitry. Normally two +5V supplies are used, one to supply the V_{CC} pins of the PLL device under test, another to power the support circuitry. It should be noted that in order to take advantage of the power on reset function, the power of the PLL chip must be turned on first, then apply power to the support circuitry.

3. ENCODED READ DATA (ERD) AND READ GATE (RG): A word pattern generator is a convenient signal source to provide the desired TTL logic level signals to these inputs.

4. LOOP FILTER COMPONENTS: Normally components "Re1" should be replaced by a short-circuited connection and "Ce1" should be open-circuited for a second order loop filter implementation. These optional components are intended for higher order filter realization.

IV. DP8459 EVALUATION BOARD PARTS LIST: (10 Mbit/s 2, 7 code operation)

DUT = DP8459 (PLCC package)
U1 = 74ALS00
U2 = 74ALS00
U3 = 74ALS74
U4 = 74LS165
U5 = 74LS92
U6 = 74HC04

D1 = Zener Diode (Vz = 3.3V)
Q1 = 2N2369 (NPN)
Q2 = 2N2369 (NPN)

Xtal = 20 MHz

SW1 = SPDT Momentary Switch
SW2 = 16-Pin DIP Toggle Switch
SW3 = 8-Pin DIP Toggle Switch
SW4 = 16-Pin DIP Toggle Switch

Bypass Capacitors:
Cb1 = 0.1 µF
Cb2 = 0.1 µF
Cb3 = 0.1 µF
Cb4 = 0.1 µF
Cb5 = 0.1 µF
Cb6 = 0.1 µF
Ca1 = 0.1 µF
Ca2 = 1000 pF
Cdi = 0.1 µF

Loop Filters:
Ct1 = 0.05 µF
Ct2 = NC*
Rt = 68Ω
Cv1 = 0.022 µF
Cv2 = 510 pF
Rv = 150Ω

Crystal Oscillator:
Cx1 = 22 pF
Cx2 = 100 pF
Cx3 = 56 pF
Rx1 = 1 MΩ
Rx2 = 100Ω

Other External Components:
Ce1 = NC*
Re1 = Short Circuit It
Rn = 2.4 kΩ
Rb = 2.4 kΩ
Ce2 = NC*
Ce3 = 1000 pF
Rpu = 510Ω
Rpd = 510Ω

Reset Circuitry:
R1 = 2 kΩ
R2 = 10 kΩ
R3 = 10 kΩ
R4 = 10 kΩ
R5 = 1 kΩ
R6 = 1 kΩ
C1 = 10 µF

*NC means no component required there (leave nodes open).

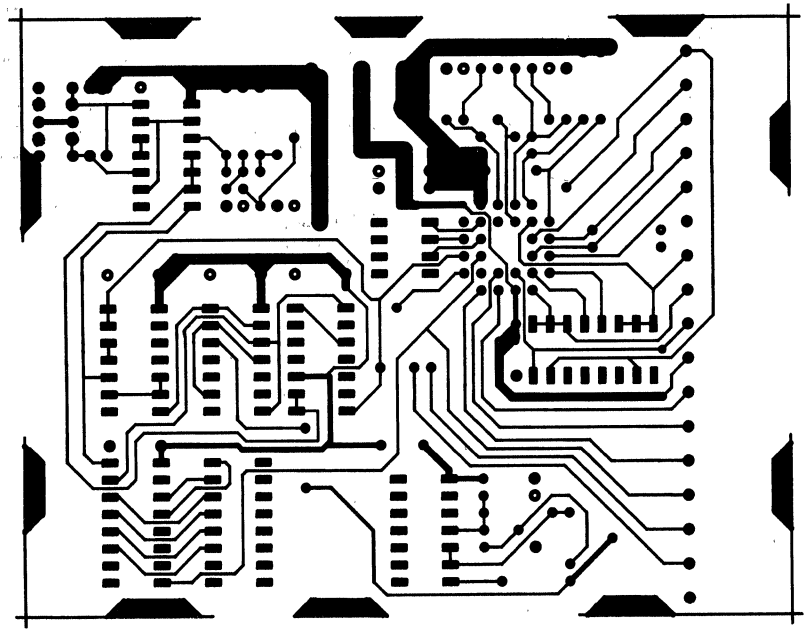

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FIGURE 2. Trace Side (Bottom View)

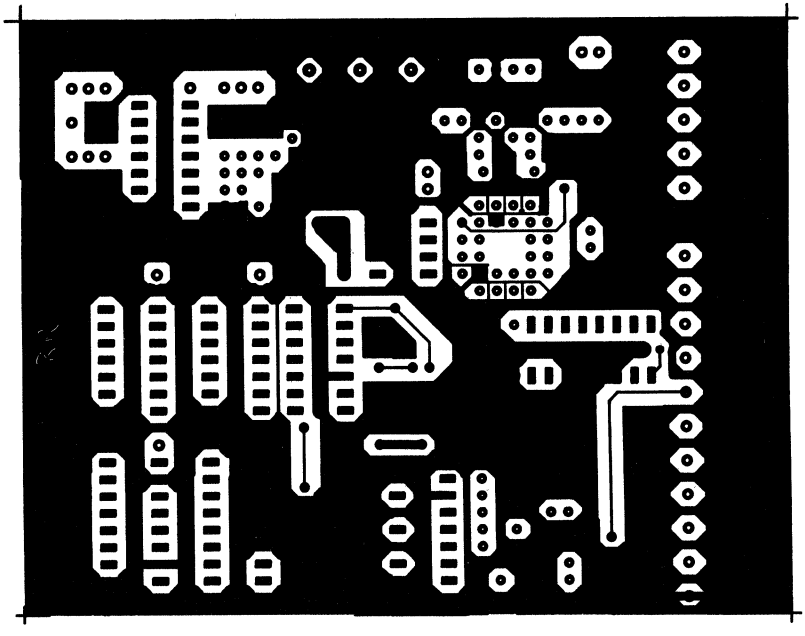

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FIGURE 3. Component Side with Ground Plane

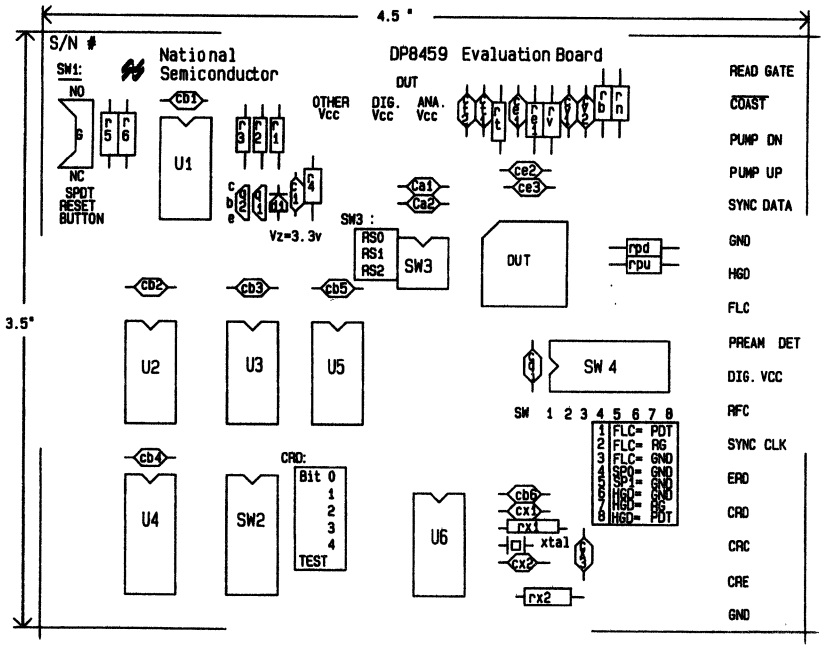

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FIGURE 4. Component Location (Top View)